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Data Catalog 1977

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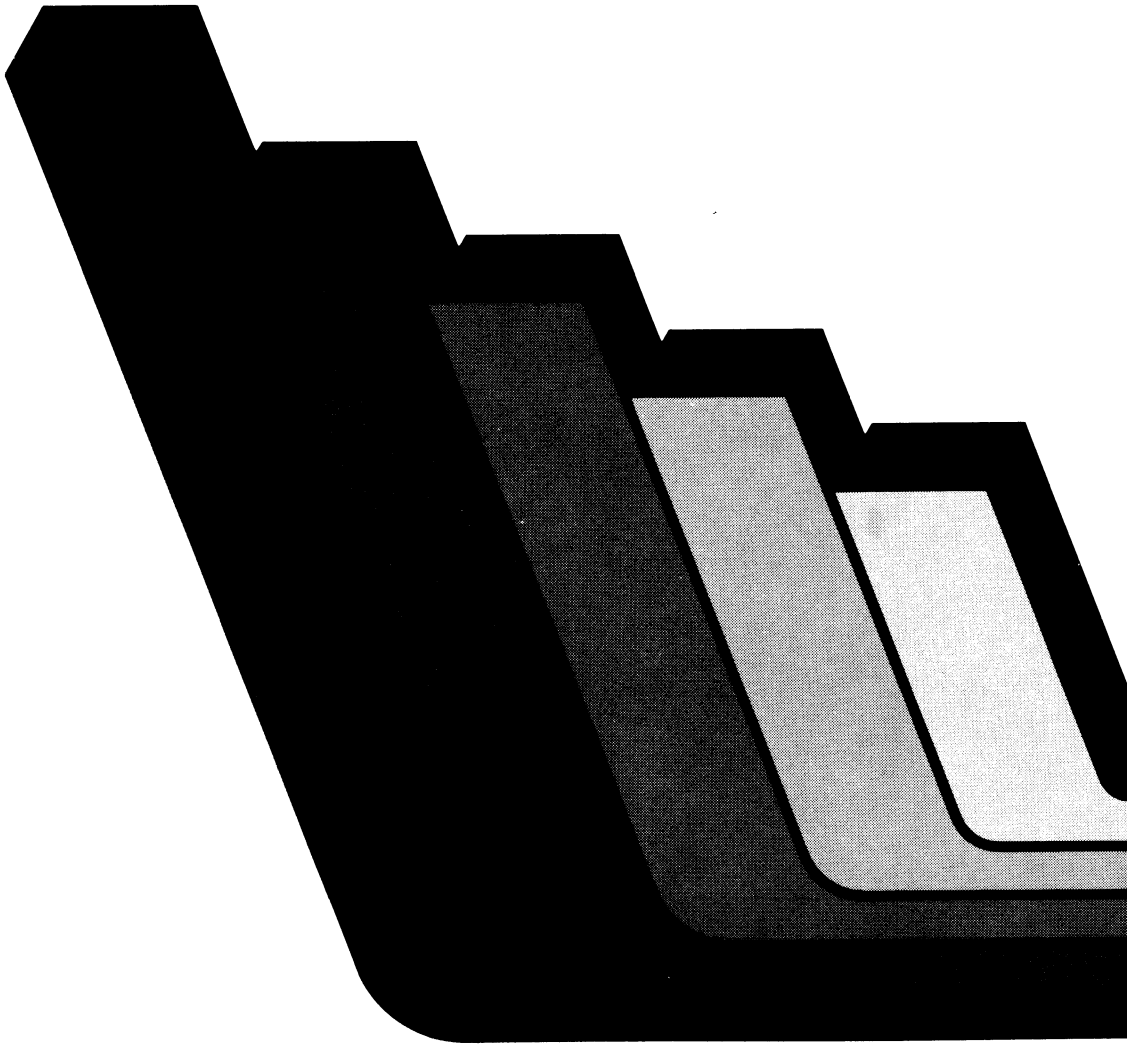

Intel was organized in 1968 to utilize the rapidly expanding technology of Integrated Electronics. During its brief history, Intel has become the world's largest supplier of MOS circuits, and is in the top ten of the world's producers of all semiconductor devices.

This 928-page Data Catalog provides complete specifications on most of Intel standard component, memory system, and microcomputer related products. Margin tabs provide quick guides to major product categories; indexes located in Section 1 and at the beginning of each section allow location of specific circuit types. Ordering, packaging, and product flow information may be found in Section 15.

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1977 Data Catalog

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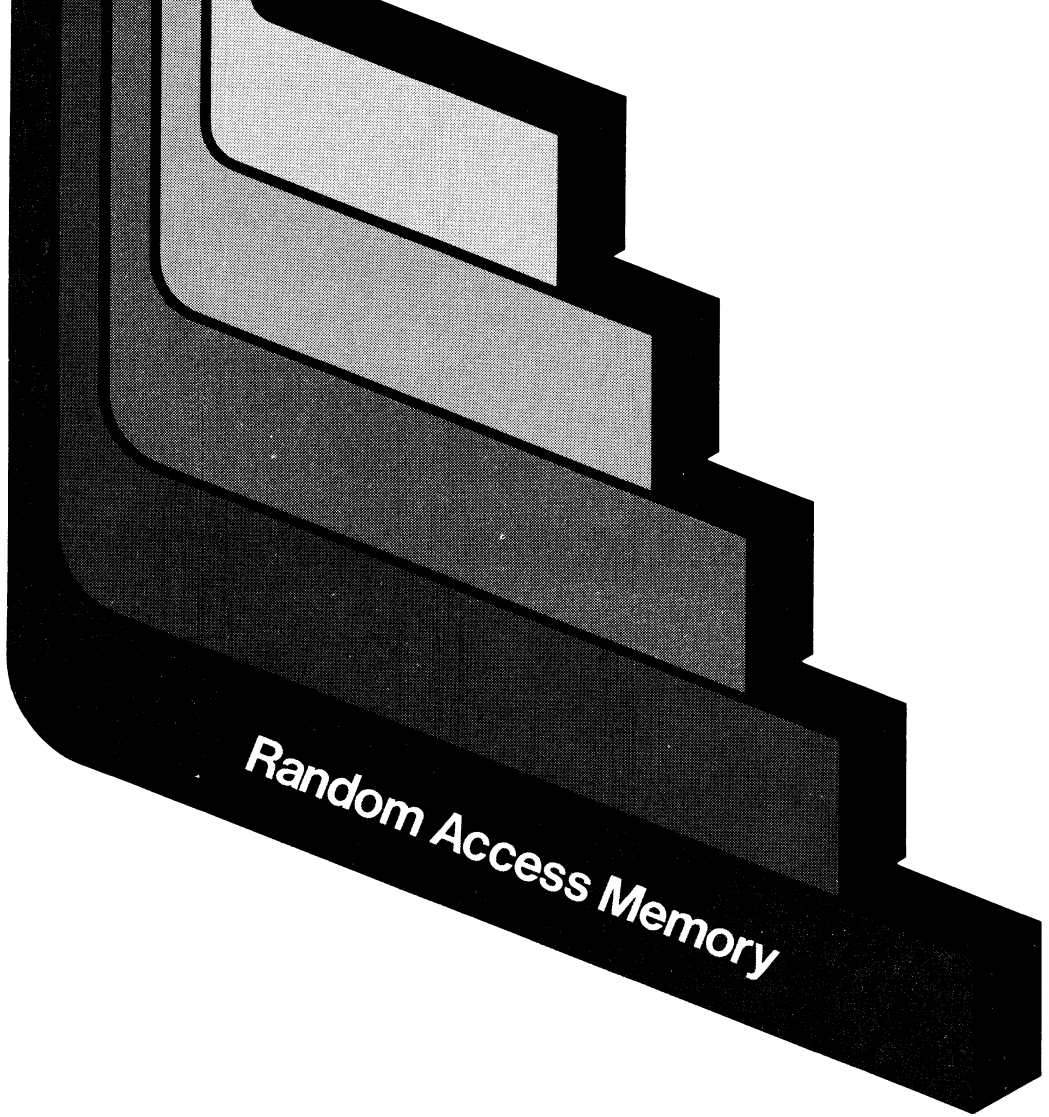
RECOMMENDED PRODUCTS FOR MCS-48/80/85 MICROCOMPUTER APPLICATIONS

Function	Part No.	Page No.	Description	T_{ACC} In ns	8048	8748	8035	8085	8080A	8008
Memory and I/O Expanders for MCS-48/85	8155	10-63	RAM-I/O		X	X	X	X		
	8355	10-75	ROM-I/O		X	X	X	X		
	8755	10-82	EPROM-I/O		X	X	X	X		
RAMs (Static)	8101A-4	10-88	256 x 4	450	X	X	X	X	X	X
	8102A-4	10-91	1K x 1	450	X	X	X	X	X	X
	8111A-4	10-95	256 x 4	450	X	X	X	X	X	X
	5101	2-112	256 x 4 CMOS	450	X	X	X	X	X	X
	2114	2-76	1K x 4	450	X	X	X	X	X	X
RAMs (Dynamic)	2104A-4	2-40	4K x 1	300				X	X	
	2107B-4	2-54	4K x 1	270				X	X	
	2116-4	2-95	16K x 1	300				X	X	
RAM Support Circuits	3222	5-19	Refresh Controller					X	X	
	3232	5-24	Refresh Counter/ Multiplexer					X	X	
	3242	5-28	Refresh Counter/ Multiplexer					X	X	
ROMs	8308	10-98	1K x 8	450	X	X	X	X	X	X
	8316A	10-102	2K x 8	850	X	X	X	X	X	X
	2316E	3-21	2K x 8	450	X	X	X	X	X	X
EPROMs	1702A-2	3-5	256 x 8	650					X	X
	8708	10-105	1K x 8	450	X	X	X	X	X	X
	2708	3-24	1K x 8	450	X	X	X	X	X	X
	2716	3-30	2K x 8	450	X	X	X	X	X	X
Peripherals	8205	10-108	1-8 Decoder		X	X	X	X	X	X
	8212	10-114	8-Bit Latch		X	X	X	X	X	X
	8214	10-128	Priority Unit		X	X	X	X	X	X
	8216	10-135	4-Bit Bus Driver		X	X	X	X	X	X
	8224	10-33	Clock Generator						X	
	8226	10-135	4-Bit Bus Driver		X	X	X	X	X	X
	8228	10-43	System Controller						X	
	8238	10-43	System Controller						X	
	8251	10-143	USART		X	X	X	X	X	X
	8253	10-159	Interval Timer		X	X	X	X	X	X
	8255A	10-170	PPI		X	X	X	X	X	X
	8257	10-195	DMA					X	X	
	8259	10-212	Interrupt		X	X	X	X	X	
	8271	10-228	Floppy Disk		X	X	X	X	X	
	8273	10-232	SDLC		X	X	X	X	X	
	8275	10-236	CRT		X	X	X	X	X	
	8279	10-240	KYBD/Display		X	X	X	X	X	X


Random Access Memory

RANDOM ACCESS MEMORIES

SILICON GATE MOS

Type	No. of Bits	Description	Organization	No. of Pins	Electrical Characteristics Over Temperature				Page No.
					Access Time Max.	Cycle Time Max.	Power Dissipation Max.[1] Operating/Standby	Supplies[V]	
1101A	256	Static Fully Decoded	256x1	16	1500ns	1500ns	685mW/340mW	+5, -9	2-4
1101A1	256	Hi-Speed Static Fully Decoded	256x1	16	1000ns	1000ns	685mW/340mW	+5, -9	
1103	1024	Dynamic Fully Decoded	1024x1	18	300ns	580ns	400mW/64mW	+16, +19	2-8
1103-1	1024	Dynamic Fully Decoded	1024x1	18	150ns	340ns	437mW/76mW	+19, +22	2-13
1103A	1024	Dynamic Fully Decoded	1024x1	18	205ns	580ns	400mW/64mW	+16, +19	2-16
1103A-1	1024	Dynamic Fully Decoded	1024x1	18	145ns	340ns	627mW/10mW	+19, +22	2-21
1103A-2	1024	Dynamic Fully Decoded	1024x1	18	145ns	400ns	570mW/10mW	+19, +22	2-26
2101A	1024	Static, Separate I/O	256x4	22	350ns	350ns	300mW	+5	2-30
2101A-2	1024	Static, Separate I/O	256x4	22	250ns	250ns	350mW	+5	
2101A-4	1024	Static, Separate I/O	256x4	22	450ns	450ns	300mW	+5	
2102A	1024	High Speed Static	1024x1	16	350ns	350ns	275mW	+5	2-34
2102A-2	1024	High Speed Static	1024x1	16	250ns	250ns	325mW	+5	
2102A-4	1024	High Speed Static	1024x1	16	450ns	450ns	275mW	+5	
2102A-6	1024	High Speed Static	1024x1	16	650ns	650ns	275mW	+5	
2102AL	1024	Low Standby Power Static	1024x1	16	350ns	350ns	165mW/35mW	+5	
2102AL-2	1024	Low Standby Power Static	1024x1	16	250ns	250ns	325mW/42mW	+5	
2102AL-4	1024	Low Standby Power Static	1024x1	16	450ns	450ns	165mW/35mW	+5	
M2102A-4	1024	Static, T_A =-55°C to +125°C	1024x1	16	450ns	450ns	350mW	+5	2-38
2104A-1	4096	16 Pin Dynamic	4096x1	16	150ns	320ns	420mW/18mW	+12, +5, -5	2-40
2104A-2	4096	16 Pin Dynamic	4096x1	16	200ns	320ns	384mW/18mW	+12, +5, -5	
2104A-3	4096	16 Pin Dynamic	4096x1	16	250ns	375ns	360mW/18mW	+12, +5, -5	
2104A-4	4096	16 Pin Dynamic	4096x1	16	300ns	425ns	360mW/18mW	+12, +5, -5	
2107A	4096	22 Pin Dynamic	4096x1	22	300ns	700ns	458mW/2mW	+12, +5, -5	2-48
2107A-1	4096	22 Pin Dynamic	4096x1	22	280ns	550ns	516mW/2mW	+12, +5, -5	
2107A-4	4096	22 Pin Dynamic	4096x1	22	350ns	840ns	450mW/2mW	+12, +5, -5	
2107A-5	4096	22 Pin Dynamic	4096x1	22	420ns	970ns	376mW/2mW	+12, +5, -5	
2107B	4096	22 Pin Dynamic	4096x1	22	200ns	400ns	648mW/4mW	+12, +5, -5	2-54
2107B-4	4096	22 Pin Dynamic	4096x1	22	270ns	470ns	648mW/4mW	+12, +5, -5	
2107B-5	4096	22 Pin Dynamic	4096x1	22	300ns	590ns	648mW/5mW	+12, +5, -5	
2108-2	8192	16 Pin Dynamic	8192x1	16	200ns	350ns	828mW/24mW	+12, +5, -5	2-60
2108-4	8192	16 Pin Dynamic	8192x1	16	300ns	425ns	780mW/24mW	+12, +5, -5	
2111A	1024	Static, Common I/O with Output Deselect	256x4	18	350ns	350ns	300mW	+5	2-67
2111A-2	1024	Static, Common I/O with Output Deselect	256x4	18	250ns	250ns	350mW	+5	
2111A-4	1024	Static, Common I/O with Output Deselect	256x4	18	450ns	450ns	300mW	+5	
2112A	1024	Static, Common I/O without Output Deselect	256x4	16	350ns	350ns	300mW	+5	2-71
2112A-2	1024	Static, Common I/O without Output Deselect	256x4	16	250ns	250ns	350mW	+5	
2112A-4	1024	Static, Common I/O without Output Deselect	256x4	16	450ns	450ns	300mW	+5	

RANDOM ACCESS MEMORIES (Continued)

	Type	No. of Bits	Description	Organi-zation	No. of Pins	Electrical Characteristics Over Temperature				Page No.
						Access Time Max.	Cycle Time Max.	Power Dissipation Max.[1] Operating/Standby	Supplies[V]	
SILICON GATE MOS	**2114**	4096	Static, Common I/O	1024x4	18	450ns	450ns	710mW	+5	2-76
	2114-2	4096	Static, Common I/O	1024x4	18	200ns	200ns	710mW	+5	
	2114-3	4096	Static, Common I/O	1024x4	18	300ns	300ns	710mW	+5	
	2114L	4096	Static, Common I/O	1024x4	18	450ns	450ns	370mW	+5	
	2114L-3	4096	Static, Common I/O	1024x4	18	300ns	300ns	370mW	+5	
	2115A	1024	Static, Open Collector	1024x1	16	45ns	45ns	660mW	+5	2-80
	2115A-2	1024	Static, Open Collector	1024x1	16	70ns	70ns	660mW	+5	
	2115AL	1024	Static, Open Collector	1024x1	16	45ns	45ns	395mW	+5	
	2115AL-2	1024	Static, Open Collector	1024x1	16	70ns	70ns	395mW	+5	
	M2115A	1024	Static, Open Collector	1024x1	16	55ns	55ns	690mW	+5	2-85
	M2115AL	1024	Static, Open Collector	1024x1	16	75ns	75ns	415mW	+5	
	2115	1024	Static, Open Collector	1024x1	16	95ns	95ns	525mW	+5	2-90
	2115-2	1024	Static, Open Collector	1024x1	16	70ns	70ns	660mW	+5	
	2115L	1024	Static, Open Collector	1024x1	16	95ns	95ns	345mW	+5	
	2125A	1024	Static, Three-State	1024x1	16	45ns	45ns	660mW	+5	2-80
	2125A-2	1024	Static, Three-State	1024x1	16	70ns	70ns	660mW	+5	
	2125AL	1024	Static, Three-State	1024x1	16	45ns	45ns	395mW	+5	
	2125AL-2	1024	Static, Three-State	1024x1	16	70ns	70ns	395mW	+5	
	M2125A	1024	Static, Three-State	1024x1	16	55ns	55ns	690mW	+5	2-85
	M2125AL	1024	Static, Three-State	1024x1	16	75ns	75ns	415mW	+5	
	2125	1024	Static, Three-State	1024x1	16	95ns	95ns	525mW	+5	2-90
	2125-2	1024	Static, Three-State	1024x1	16	70ns	70ns	660mW	+5	
	2125L	1024	Static, Three-State	1024x1	16	95ns	95ns	345mW	+5	
	2116-2	16384	16 Pin Dynamic	16384x1	16	200ns	350ns	828mW/24mW	+12, +5, -5	2-95
	2116-3	16384	16 Pin Dynamic	16384x1	16	250ns	375ns	816mW/24mW	+12, +5, -5	
	2116-4	16384	16 Pin Dynamic	16384x1	16	300ns	425ns	780mW/24mW	+12, +5, -5	
	2147	4096	High Speed Static	4096x1	18	60-90ns	60-90ns	500mW/50mW (Typical)	+5	2-103
SCHOTTKY BIPOLAR	**3101**	64	Fully Decoded	16x4	16	60ns	60ns	525mW	+5	2-104
	3101A	64	High Speed Fully Decoded	16x4	16	35ns	35ns	525mW	+5	
	3104	16	Content Addressable Memory	4x4	24	30ns	40ns	625mW	+5	2-108
SILICON GATE CMOS	**5101-8**	1024	Static CMOS RAM	256x4	22	800ns	800ns	150mW/2.5mW	+5	2-112
	5101L	1024	Static CMOS RAM	256x4	22	650ns	650ns	135mW/20µW	+5	
	5101L-1	1024	Static CMOS RAM	256x4	22	450ns	450ns	135mW/20µW	+5	
	5101L-3	1024	Static CMOS RAM	256x4	22	650ns	650ns	135mW/1mW	+5	
	M5101-4	1024	Static CMOS RAM (-55°C to 125°C)	256x4	22	800ns	800ns	168mW/1mW	+5	2-116
	M5101L-4	1024	Static CMOS RAM (-55°C to 125°C)	256x4	22	800ns	800ns	168mW/400µW	+5	

1101A, 1101A1

256 x 1 BIT STATIC RAM

- **Access Time -- Typically Below 650 nsec - 1101A1, 850 nsec - 1101A**
- **Low Power Standby Mode**
- **Low Power Dissipation -- Typically less than 1.5 mW/bit during access**
- **Directly DTL and TTL Compatible**
- **Three-state Output -- OR-tie Capability**
- **Simple Memory Expansion -- Chip Select Input Lead**
- **Fully Decoded --On Chip Address Decode and Sense**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Ceramic and Plastic Package -- 16 Pin Dual In-Line Configuration**

The 1101A is an improved version of the 1101 which requires only two power supplies (+5V and −9V) for operation. The 1101A is a direct pin for pin replacement for the 1101.

The Intel®1101A is a 256 word by 1 bit random access memory element using normally off P-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks to operate.

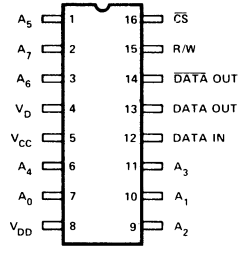
The 1101A is designed primarily for small buffer storage applications where high performance, low cost, and ease of interfacing with other standard logic circuits are important design objectives. The unit will directly interface with standard bipolar integrated logic circuits (TTL, DTL, etc.) The data output buffers are capable of driving TTL loads **directly**. A separate chip select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

For applications requiring a faster access time we recommend the 1101A1 which is a selection from the 1101A and has a guaranteed maximum access time of 1.0 μsec.

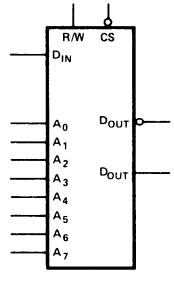
The Intel 1101A is fabricated with **silicon gate technology**. This **low threshold** technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Intel's **silicon gate technology** also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

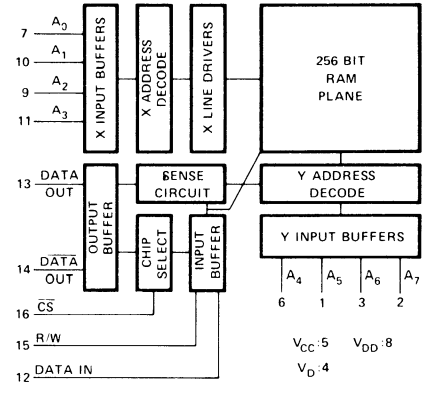
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	$\overline{CS}$	CHIP SELECT
A_0– A_7	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT		

Absolute Maximum Ratings[1]

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +160°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{CC}	+0.5V to −20V
Supply Voltages V_{DD} and V_D with Respect to V_{CC}	−20V
Power Dissipation	1 WATT

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = −9V ± 5%, V_D = −9V ± 5%, unless otherwise specified

SYMBOL	TEST	MIN.	TYP.[2]	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT** (ALL INPUT PINS)		**<1.0**	**500**	**nA**	**V_{IN} = 0.0 V**
I_{LO}	OUTPUT LEAKAGE CURRENT		<1.0	500	nA	V_{OUT} = 0.0 V, $\overline{CS}$ = V_{CC} −2
I_{DD1}	POWER SUPPLY CURRENT, V_{DD}		13	19	mA	T_A = 25°C
I_{DD2}	POWER SUPPLY CURRENT, V_{DD}			25	mA	T_A = 0°C
I_{D1}	POWER SUPPLY CURRENT, V_D		12	18	mA	T_A = 25°C,
I_{D2}	POWER SUPPLY CURRENT, V_D			24	mA	T_A = 0°C,
						Continuous Operation I_{OL} = 0.0 mA
V_{IL}	**INPUT "LOW" VOLTAGE**	**−10**		**V_{CC}−4.5**	**V**	
V_{IH}[3]	**INPUT "HIGH" VOLTAGE**	**V_{CC}−2**		**V_{CC}+0.3**	**V**	
I_{OL1}	OUTPUT SINK CURRENT	3.0	8		mA	V_{OUT} = +0.45 V, T_A = +25°C
I_{OL2}	OUTPUT SINK CURRENT	2.0			mA	V_{OUT} = +0.45 V, T_A = +70°C
I_{CF}	OUTPUT CLAMP CURRENT		6	13	mA	V_{OUT} = −1.0 V
I_{OH1}	OUTPUT SOURCE CURRENT	−3.0	−8		mA	V_{OUT} = 0.0 V, T_A = +25°C
I_{OH2}	OUTPUT SOURCE CURRENT	−2.0	−7		mA	V_{OUT} = 0.0 V, T_A = +70°C
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	I_{OL} = 2.0 mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	+3.5	+4.9		V	I_{OH} = −100μA
C_{IN}[4]	INPUT CAPACITANCE (ALL INPUT PINS)		7	10	pF	V_{IN} = V_{CC}
C_{OUT}[4]	OUTPUT CAPACITANCE		7	10	pF	V_{OUT} = V_{CC}
C_V[4]	V_D POWER SUPPLY CAPACITANCE		20	35	pF	V_D = V_{CC}
						f = 1 MHz, T_A = 25°C

Note 1: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are at nominal voltages and T_A = 25°C.

Note 3: A TTL driving the 1101A, 1101A1 must have its output high ≥ V_{CC}−2 even if it is loaded by other bipolar gates.

Note 4: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_D = −9V ± 5%, V_{DD} = −9V ± 5%

READ CYCLE

SYMBOL	TEST		MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle	1101A	1.5			µsec
		1101A1	1.0			µsec
t_{AC}	Address to Chip Select Delay	1101A			1.2(1)	µsec
		1101A1			0.7(1)	µsec
t_A	Access Time	1101A		0.85	1.5	µsec
		1101A1		0.65	1.0	µsec
t_{OH}	Previous Read Data Valid		0.05			µsec

WRITE CYCLE

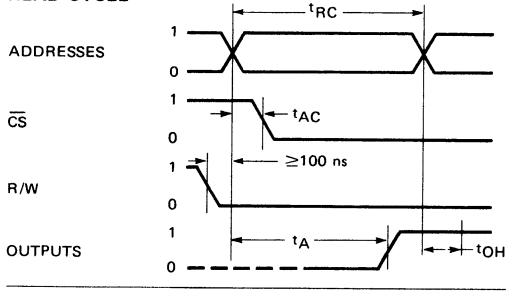
t_{WC}	Write Cycle		0.8			µsec
t_{WD}	Address to Write Pulse Delay		0.3			µsec
t_{WP}	Write Pulse Width		0.4			µsec
t_{DW}	Data Set up Time		0.3			µsec
t_{DH}	Data Hold Time		0.1			µsec

CHIP SELECT AND DESELECT

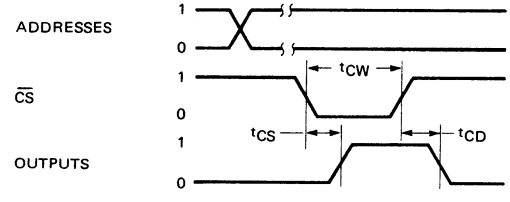
t_{CW}	Chip Select Pulse Width		0.4			µsec
t_{CS}	Access Time Through Chip Select Input			0.2	0.3	µsec
t_{CD}	Chip Deselect Time			0.1	0.3	µsec

CONDITIONS OF TEST:
Input pulse amplitudes: 0 to 5V, Input pulse rise and fall time: 10 nsec. Speed measurements referenced to 1.5V levels (unless otherwise noted). Output load is 1 TTL gate and C_L = 20 pF; measurements made at output of TTL gate ($t_{PD} \leq$ 10 nsec)

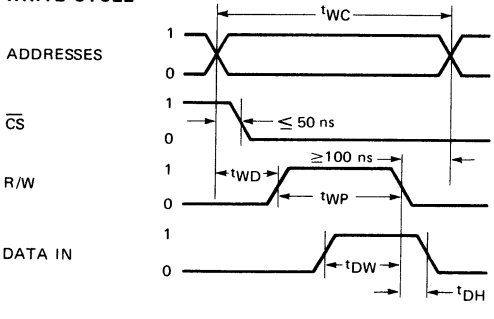
READ CYCLE



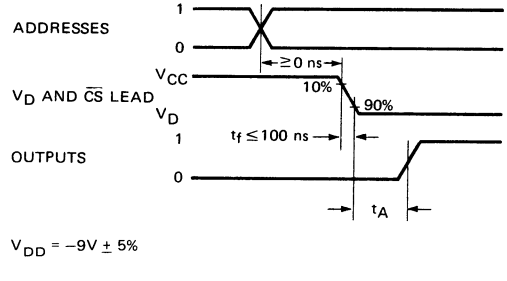
CHIP SELECT AND DESELECT



WRITE CYCLE



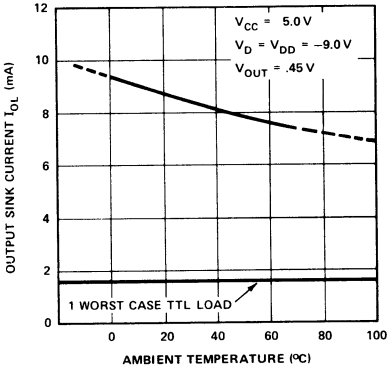
POWER SWITCHING OF V_D



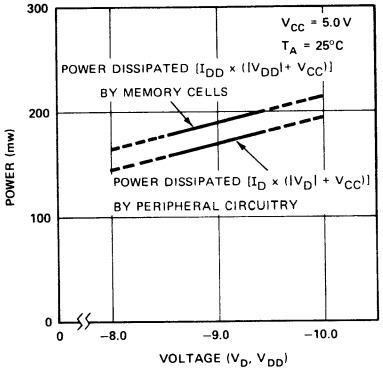
Note 1: Maximum value for t_{AC} measured at minimum read cycle.

Typical D. C. Characteristics

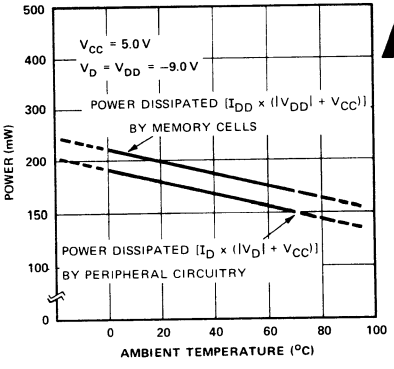
OUTPUT SINK CURRENT VS TEMPERATURE



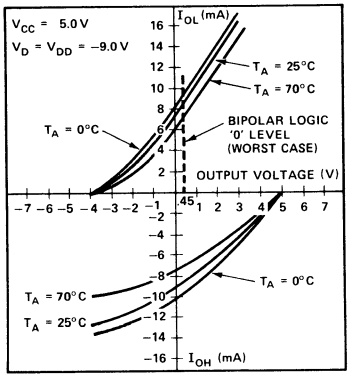
POWER DISSIPATION VS VOLTAGE



POWER DISSIPATION VS TEMPERATURE

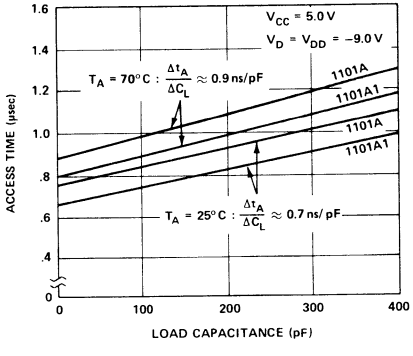


OUTPUT CURRENT VS OUTPUT VOLTAGE

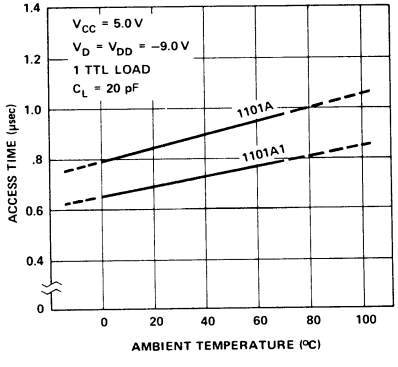


Typical A. C. Characteristics

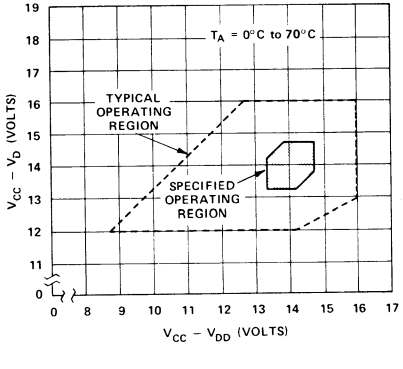
ACCESS TIME VS.
LOAD CAPACITANCE



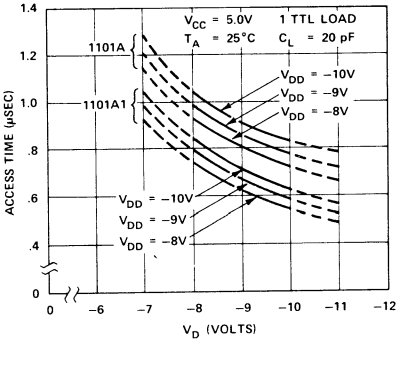
ACCESS TIME VS.
TEMPERATURE



1101A/1101A1
OPERATING REGION



ACCESS TIME VS.
SUPPLY VOLTAGE



RAM

1024 X 1 BIT DYNAMIC RAM

- **Low Power Dissipation — Dissipates Power Primarily on Selected Chips**
- **Access Time — 300 nsec**
- **Cycle Time — 580 nsec**
- **Refresh Period... 2 milliseconds for 0—70° C Ambient**
- **OR-Tie Capability**
- **Simple Memory Expansion — Chip Enable Input Lead**
- **Fully Decoded—on Chip Address Decode**
- **Inputs Protected—All Inputs Have Protection Against Static Charge**
- **Ceramic and Plastic Package -- 18 Pin Dual In-Line Configuration.**

The Intel 1103 is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

It is a 1024 word by 1 bit random access memory element using normally off *P*-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18 pin dual in-line package. It uses dynamic circuitry and primarily dissipates power only during precharge.

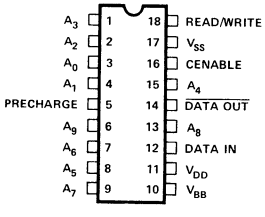
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds.

A separate **cenable** (chip enable) lead allows easy selection of an individual package when outputs are OR-tied.

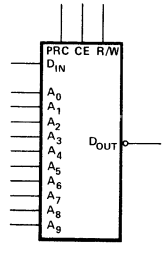
The Intel 1103 is fabricated with **silicon gate technology.** This **low threshold** technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

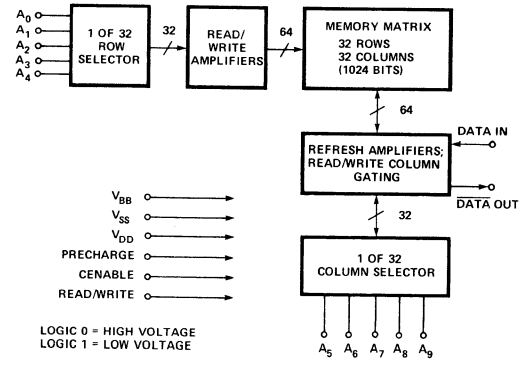
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	PRC	PRECHARGE INPUT
A_0–A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	D_{OUT}	DATA OUTPUT

Maximum Guaranteed Ratings*

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{BB}	−25V to 0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−25V to 0.3V
Power Dissipation	1.0 W

*COMMENT:

Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to +70°C, $V_{SS}^{(1)}$ = 16V ± 5%, $(V_{BB} - V_{SS})^{(6)}$ = 3V to 4V, V_{DD} = 0V unless otherwise specified

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT** (ALL INPUT PINS)			1	μA	V_{IN} = 0V
I_{LO}	OUTPUT LEAKAGE CURRENT			1	μA	V_{OUT} = 0V
I_{BB}	**V_{BB} SUPPLY CURRENT**			100	μA	
$I_{DD1}^{(2)}$	SUPPLY CURRENT DURING T_{PC}		37	56	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = V_{SS}; T_A = 25°C
$I_{DD2}^{(2)}$	SUPPLY CURRENT DURING T_{OV}		38	59	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = 0V; T_A = 25°C
$I_{DD3}^{(2)}$	SUPPLY CURRENT DURING T_{POV}		5.5	11	mA	PRECHARGE = V_{SS} CENABLE = 0V; T_A = 25°C
$I_{DD4}^{(2)}$	SUPPLY CURRENT DURING T_{CP}		3	4	mA	PRECHARGE = V_{SS} CENABLE = V_{SS}; T_A = 25°C
$I_{DD}^{(5)}$AV	**AVERAGE SUPPLY CURRENT**		**17**	**25**	**mA**	**CYCLE TIME = 580 ns; PRECHARGE WIDTH = 190 ns; T_A = 25°C**
$V_{IL1}^{(7)}$	INPUT LOW VOLTAGE (ALL ADDRESS & DATA-IN LINES)	V_{SS}−17		V_{SS}−14.2	V	T_A = 0°C
$V_{IL2}^{(7)}$	INPUT LOW VOLTAGE (ALL ADDRESS & DATA-IN LINES)	V_{SS}−17		V_{SS}−14.5	V	T_A = 70°C
$V_{IL3}^{(7,8)}$	INPUT LOW VOLTAGE (PRECHARGE CENABLE & READ/WRITE INPUTS)	V_{SS}−17		V_{SS}−14.7	V	T_A = 0°C
$V_{IL4}^{(7,8)}$	INPUT LOW VOLTAGE (PRECHARGE CENABLE& READ/WRITE INPUTS)	V_{SS}−17		V_{SS}−15.0	V	T_A = 70°C
$V_{IH1}^{(7)}$	INPUT HIGH VOLTAGE (ALL INPUTS)	V_{SS}−1		V_{SS}+1	V	T_A = 0°C
$V_{IH2}^{(7)}$	INPUT HIGH VOLTAGE (ALL INPUTS)	V_{SS}−0.7		V_{SS}+1	V	T_A = 70°C
I_{OH1}	**OUTPUT HIGH CURRENT**	**600**	**900**	**4000**	μA	T_A = 25°C
I_{OH2}	**OUTPUT HIGH CURRENT**	**500**	**800**	**4000**	μA	T_A = 70°C
I_{OL}	OUTPUT LOW CURRENT	See Note 3				R_{LOAD} = 100Ω (4)
V_{OH1}	OUTPUT HIGH VOLTAGE	60	90	400	mV	T_A = 25°C,
V_{OH2}	OUTPUT HIGH VOLTAGE	50	80	400	mV	T_A = 70°C,
V_{OL}	OUTPUT LOW VOLTAGE	See Note 3				

Note 1: The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.

Note 2: See Supply Current vs. Temperature (p. 3) for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.

Note 3: The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.

Note 4: This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

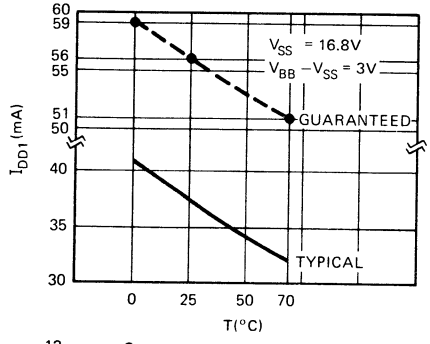
Note 5: This parameter is periodically sampled and is not 100% tested.

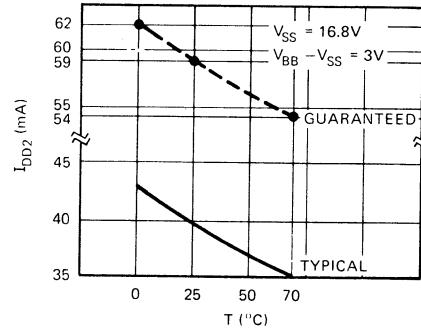
Note 6: $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.

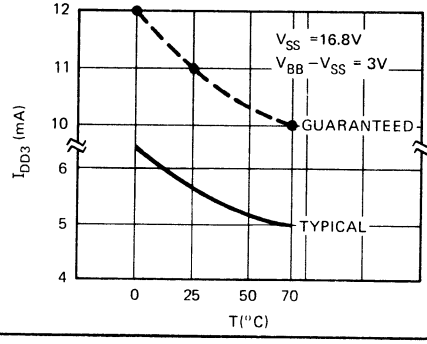
Note 7: The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C. Thus any value in between 0°C and 70°C can be calculated by using a straight-line relationship.

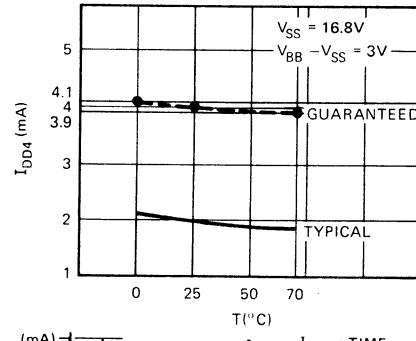
Note 8: The maximum values for V_{IL} (for precharge, cenable & read/write) may be increased to V_{SS}−14.2 @ 0°C and V_{SS}−14.5 @ 70°C (same values as those specified for the address & data-in lines) with a 40ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.

Supply Current vs Temperature

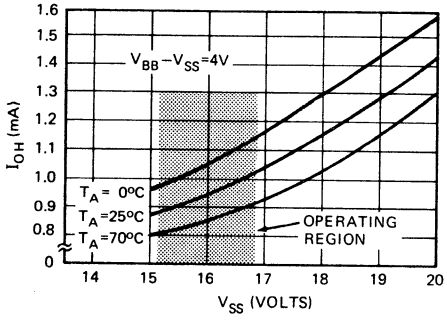


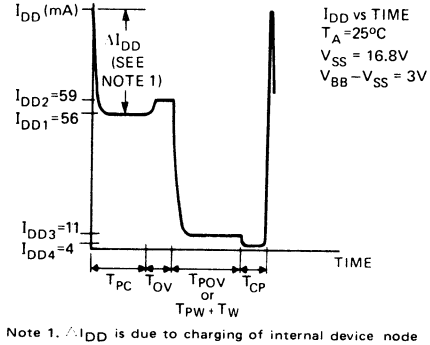






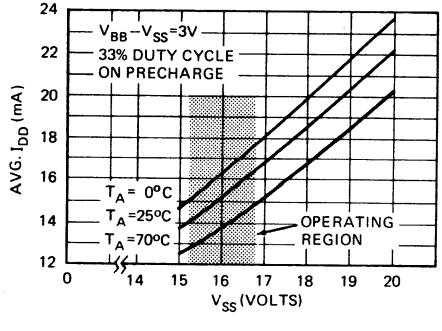
Typical Characteristics

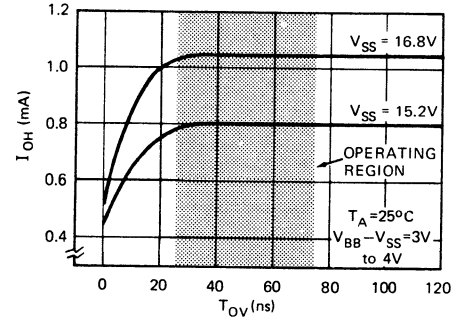




Note 1. ΔI_{DD} is due to charging of internal device node capacitance at precharge

Note 2. These values are taken from a single pulse measurement





AC Characteristics T_A = 0°C to 70°C, V_{SS} = 16 ± 5%, (V_{BB} − V_{SS}) = 3.0V to 4.0V, V_{DD} = 0V

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	**TIME BETWEEN REFRESH**			**2**	**ms**	
t_{AC} (1)	ADDRESS TO CENABLE SET UP TIME	115			ns	
t_{CA}	CENABLE TO ADDRESS HOLD TIME	20			ns	
t_{PC} (1)	PRECHARGE TO CENABLE DELAY	125			ns	
t_{CP}	CENABLE TO PRECHARGE DELAY	85			ns	
t_{OL}	PRECHARGE & CENABLE OVERLAP, LOW	25		75	ns	t_T = 20ns
t_{OH}	PRECHARGE & CENABLE OVERLAP, HIGH			140	ns	t_T = 20ns
t_{OVM}	PRECHARGE & CENABLE OVERLAP, 50% POINTS	45		95	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC} (1)	**READ CYCLE**	**480**			**ns**	
t_{POV}	PRECHARGE TO END OF CENABLE	165		500	ns	
t_{PO}	END OF PRECHARGE TO OUTPUT DELAY			120	ns	
t_{ACC1} (1)	**ADDRESS TO OUTPUT ACCESS**	**300**			**ns**	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2t_T$; **$t_T$ = 20 ns**, C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV
t_{ACC2} (1)	**PRECHARGE TO OUTPUT ACCESS**	**310**			**ns**	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2t_T$

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC} (1)	**WRITE CYCLE**	**580**			**ns**	**t_T = 20 ns**
t_{RWC} (1)	**READ/WRITE CYCLE**	**580**			**ns**	
t_{PW}	PRECHARGE TO READ/WRITE DELAY	165		500	ns	
t_{WP}	READ/WRITE PULSE WIDTH	50			ns	
t_W	READ/WRITE SET UP TIME	80			ns	
t_{DW}	DATA SET UP TIME	105			ns	
t_{DH}	DATA HOLD TIME	10			ns	
t_{PO}	END OF PRECHARGE TO OUTPUT DELAY			120	ns	C_{LOAD} = 100 pF, R_{LOAD} = 100Ω, V_{REF} = 40 mV
t_{CW}	RELATIONSHIP BETWEEN CENABLE AND READ/WRITE			0	ns	

Note 1: These times will degrade by 40 ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS}−14.2V @ 0°C and V_{SS}−14.5V @ 70°C as defined on page 2.

*CAPACITANCE T_A = 25 C

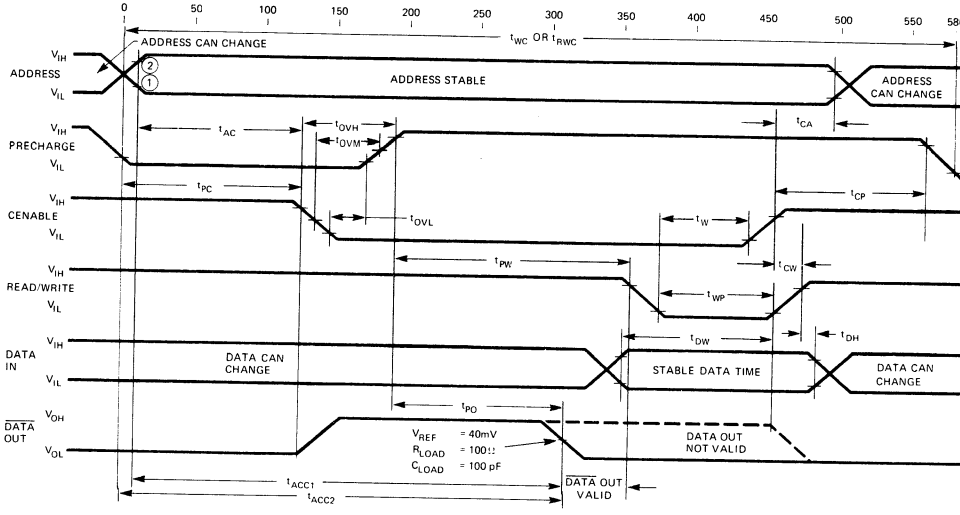
SYMBOL	TEST	TYP.	PLASTIC PKG. MAX.	CERAMIC PKG. MAX.	UNIT	CONDITIONS
C_{AD}	ADDRESS CAPACITANCE	5	7	12	pF	$V_{IN} = V_{SS}$
C_{PR}	PRECHARGE CAPACITANCE	15	18	19.5	pF	$V_{IN} = V_{SS}$
C_{CE}	CENABLE CAPACITANCE	15	18	21	pF	$V_{IN} = V_{SS}$
C_{RW}	READ/WRITE CAPACITANCE	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	DATA INPUT CAPACITANCE	4	5	7.5	pF	CENABLE = 0V, $V_{IN} = V_{SS}$
C_{IN2}	DATA INPUT CAPACITANCE	2	4	6.5	pF	CENABLE = V_{SS}, $V_{IN} = V_{SS}$
C_{OUT}	DATA OUTPUT CAPACITANCE	2	3	7	pF	V_{OUT} = 0V

f = 1 MHz, All Unused Pins Are At A.C. Ground

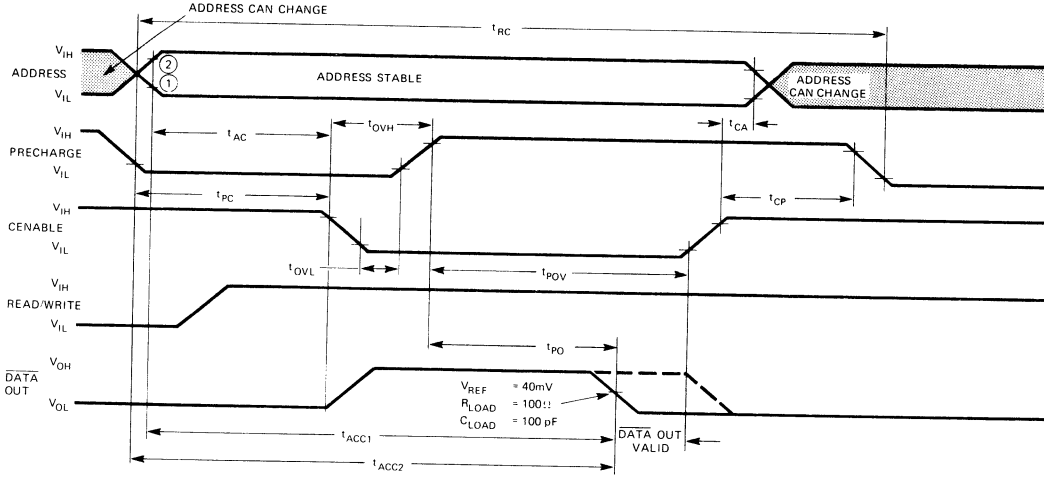
*This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



READ CYCLE



NOTE ① V_{DD} + 2V
NOTE ② V_{SS} 2V
t_T IS DEFINED AS THE TRANSITIONS BETWEEN THESE TWO POINTS
NOTE 3 t_{DW} IS REFERENCED TO POINT ① OF THE RISING EDGE OF CENABLE OR READ WRITE WHICHEVER OCCURS FIRST
NOTE 4 t_{DH} IS REFERENCED TO POINT ② OF THE RISING EDGE OF CENABLE OR READ WRITE WHICHEVER OCCURS FIRST

The Intel®1103-1 is a high speed 1024 bit dynamic random access memory and is the high speed version of the standard 1103. The DC and AC Characteristics for the 1103-1 are given in the following three pages. The absolute maximum ratings for the 1103-1 are the same as for the 1103 on page 2-8.

- **Access Time — 150 nsec**
- **Cycle Time — 340 nsec**

D.C. and Operating Characteristics

(T_A = 0°C to +55°C, V_{SS}[1] = 19V ± 5% ($V_{BB} - V_{SS}$)[6] = 3V to 4V, V_{DD} = 0V unless otherwise specified)

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	**INPUT LOAD CURRENT** (ALL INPUT PINS)			**10**	**μA**	**V_{IN} = 0V**
I_{LO}	OUTPUT LEAKAGE CURRENT			10	μA	V_{OUT} = 0V
I_{BB}	**V_{BB} SUPPLY CURRENT**			**100**	**μA**	
I_{DD1}[2]	SUPPLY CURRENT DURING T_{PC}		45	60	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = V_{SS} T_A = 25°C
I_{DD2}[2]	SUPPLY CURRENT DURING T_{OV}		50	68.5	mA	ALL ADDRESSES = 0V PRECHARGE = 0V CENABLE = 0V T_A = 25°C
I_{DD3}[2]	SUPPLY CURRENT DURING T_{POV}		8.5	11	mA	PRECHARGE = V_{SS} CENABLE = 0V T_A = 25°C
I_{DD4}[2]	SUPPLY CURRENT DURING T_{CP}		3.0	4	mA	PRECHARGE = V_{SS} CENABLE = V_{SS} T_A = 25°C
$I_{DD\,AVG}$[5]	**AVERAGE SUPPLY CURRENT**		20	**23**	**mA**	**CYCLE TIME = 340 ns PRECHARGE WIDTH@50% 105ns, T_A = 25°C**
V_{IL}	INPUT LOW VOLTAGE	V_{SS} − 20		V_{SS} − 18	V	
V_{IH}	INPUT HIGH VOLTAGE	V_{SS} − 1		V_{SS} + 1	V	
I_{OH1}	**OUTPUT HIGH CURRENT**	**1150**	**1300**	**7000**	**μA**	**T_A = 25°C**
I_{OH2}	**OUTPUT HIGH CURRENT**	**900**	**1150**	**7000**	**μA**	**T_A = 55°C**
I_{OL}[3]	OUTPUT LOW CURRENT		See Note 3			**R_{LOAD}[4] = 100 Ω**
V_{OH1}	OUTPUT HIGH VOLTAGE	115	130	700	mV	T_A = 25°C,
V_{OH2}	OUTPUT HIGH VOLTAGE	90	115	700	mV	T_A = 55°C,
V_{OL}[3]	OUTPUT LOW VOLTAGE		See Note 3			

Note 1: The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).

Note 2: See Supply Current vs. Temperature (p. 2-9)for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.

Note 3: The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.

Note 4: This value of load resistance is used for measurement purposes. In applications the resistance may range from 100 Ω to 1 kΩ.

Note 5: This parameter is periodically sampled and is not 100% tested.

Note 6: ($V_{BB} - V_{SS}$) supply should be applied at or before V_{SS}.

AC Characteristics (T_A = 0°C to 55°C, V_{SS} = 19 ± 5%, $V_{BB} - V_{SS}$ = 3.0V to 4.0V, V_{DD} = 0V)

READ, WRITE, AND READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{REF}	**TIME BETWEEN REFRESH**			**1**	**ms**	
t_{AC}	ADDRESS TO CENABLE SET UP TIME	30			ns	
t_{CA}	CENABLE TO ADDRESS HOLD TIME	10			ns	
t_{PC}	PRECHARGE TO CENABLE DELAY	60			ns	
t_{CP}	CENABLE TO PRECHARGE DELAY	40			ns	
t_{OVL}	PRECHARGE & CENABLE OVERLAP, LOW	5		30	ns	t_T = 20ns
t_{OVH}	PRECHARGE & CENABLE OVERLAP, HIGH			85	ns	t_T = 20ns
t_{OVM}	PRECHARGE & CENABLE OVERLAP, 50% POINTS	25		50	ns	

READ CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{RC} (1)	**READ CYCLE**	**300**			**ns**	**t_T = 20 ns**
t_{POV}	PRECHARGE TO END OF CENABLE	115		500	ns	
t_{PO} (1)	END OF PRECHARGE TO OUTPUT DELAY			75	ns	C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV
t_{ACC1} (1)	**ADDRESS TO OUTPUT ACCESS**	**150**			**ns**	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$ C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV
t_{ACC2} (1)	**PRECHARGE TO OUTPUT ACCESS**	**180**			**ns**	$t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\,t_T$ C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV

WRITE OR READ/WRITE CYCLE

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{WC}	**WRITE CYCLE**	**340**			**ns**	**t_T = 20 ns**
t_{RWC} (1)	**READ/WRITE CYCLE**	**340**			**ns**	
t_{PW}	PRECHARGE TO READ/WRITE DELAY	115		500	ns	
t_{WP}	READ/WRITE PULSE WIDTH	20			ns	
t_W	READ/WRITE SET UP TIME	20			ns	
t_{DW}	DATA SET UP TIME	40			ns	
t_{DH}	DATA HOLD TIME	10			ns	
t_{PO} (1)	END OF PRECHARGE TO OUTPUT DELAY			75	ns	C_{LOAD} = 50 pF R_{LOAD} = 100Ω V_{REF} = 80 mV
t_{CW}	RELATIONSHIP BETWEEN CENABLE AND READ/WRITE			0	ns	

NOTE 1: These times will degrade by 35 nsec if a V_{REF} point of*40 mV is chosen instead of the 80 mV point defined in the spec.

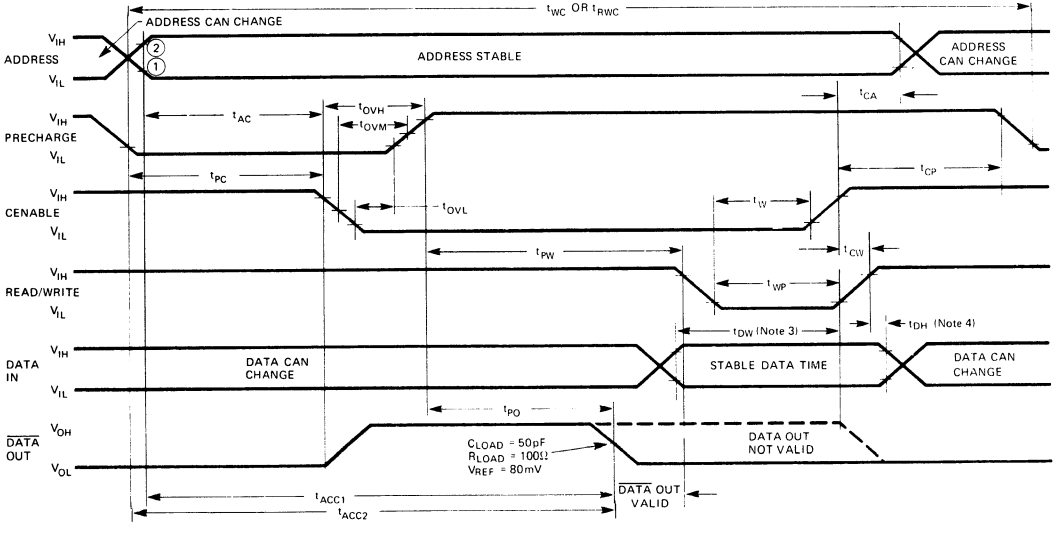
*CAPACITANCE T_A = 25°C

SYMBOL	TEST	TYP.	PLASTIC PKG. MAX.	CERAMIC PKG. MAX.	UNIT	CONDITIONS
C_{AD}	ADDRESS CAPACITANCE	5	7	12	pF	$V_{IN} = V_{SS}$
C_{PR}	PRECHARGE CAPACITANCE	15	18	19.5	pF	$V_{IN} = V_{SS}$
C_{CE}	CENABLE CAPACITANCE	15	18	21	pF	$V_{IN} = V_{SS}$
$C_{R/W}$	READ/WRITE CAPACITANCE	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	DATA INPUT CAPACITANCE	4	5	7.5	pF	CENABLE = 0V $V_{IN} = V_{SS}$
C_{IN2}	DATA INPUT CAPACITANCE	2	4	6.5	pF	CENABLE = V_{SS} $V_{IN} = V_{SS}$
C_{OUT}	DATA OUTPUT CAPACITANCE	2	3	7	pF	V_{OUT} = 0V

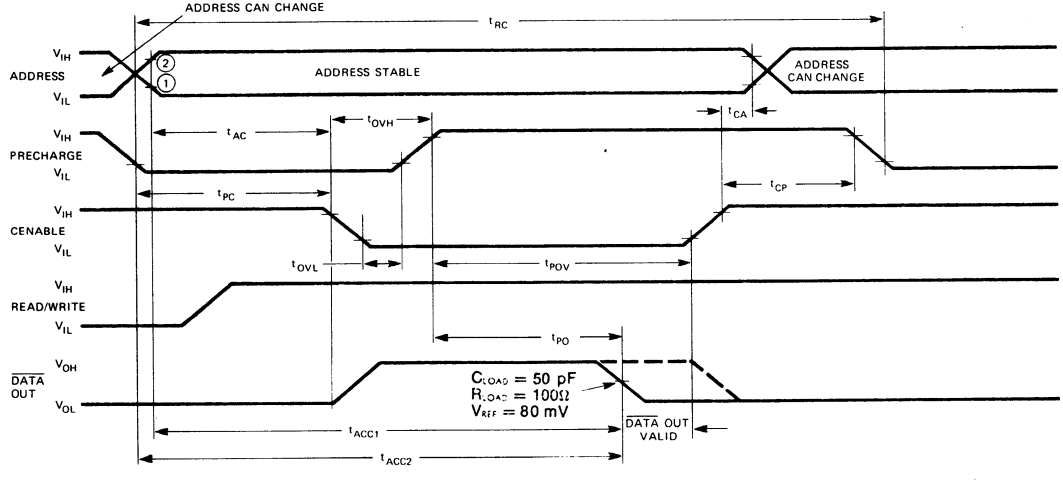
f = 1 MHz All Unused Pins Are At A.C. Ground

*This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions.

WRITE OR READ/WRITE CYCLE



READ CYCLE



NOTE ① V_{DD} + 2V
NOTE ② V_{SS} − 2V
} t_T IS DEFINED AS THE TRANSITIONS BETWEEN THESE TWO POINTS

NOTE 3 t_{DW} IS REFERENCED TO POINT ① OF THE RISING EDGE OF CHIP ENABLE OR READ WRITE WHICHEVER OCCURS FIRST

NOTE 4 t_{DH} IS REFERENCED TO POINT ② OF THE RISING EDGE OF CHIP ENABLE OR READ WRITE WHICHEVER OCCURS FIRST

1103A

1024 x 1 BIT DYNAMIC RAM

- ***No Precharge Required -- Critical Precharge Timing is Eliminated**
- **Electrically Equivalent to 1103 -- Pin-for-Pin/Functionally Compatible**
- **Fast Access Time -- 205ns max.**
- **Low Standby Power Dissipation -- 2 µW/Bit typical**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion -- Chip Enable Input Lead**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Ceramic and Plastic Package -- 18-Pin DIP**

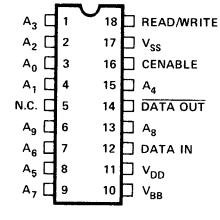
The 1103A is a 1024 word by 1 bit dynamic RAM. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives. The 1103A is electrically equivalent to the 1103.

1103A systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

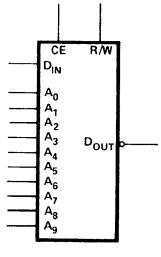
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every two milliseconds. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

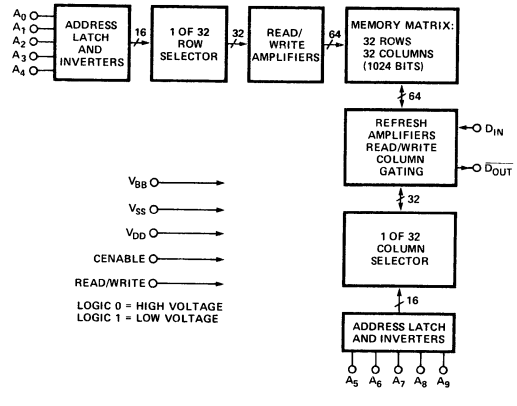
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to 70°C

Storage Temperature ..... −65°C to +150°C

All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} ..... −25V to 0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} ..... −25V to 0.3V

Power Dissipation 1.0W

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

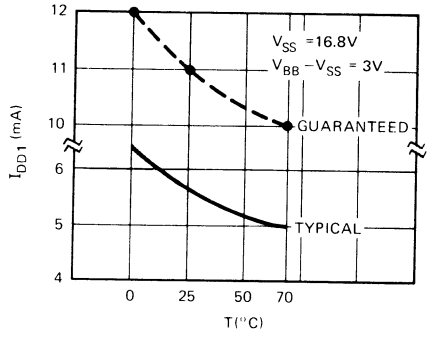
D. C. and Operating Characteristics

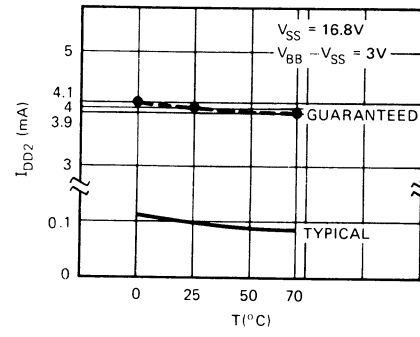
T_A = 0°C to +70°C, V_{SS} [1] = 16V ± 5%, ($V_{BB} - V_{SS}$) [2] = 3V to 4V, V_{DD} = 0V unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			1	μA	V_{IN} = 0V
I_{LO}	Output Leakage Current			1	μA	V_{OUT} = 0V
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}	Supply Current During Cenable On		4	11	mA	Cenable = 0V; T_A = 25°C
I_{DD2}	Supply Current During Cenable Off		0.1	4	mA	Cenable = V_{SS}; T_A = 25°C
I_{DDAV}	Average Supply Current		17	25	mA	Cycle Time = 580ns; T_A = 25°C
V_{IL}	Input Low Voltage	V_{DD} −1		V_{DD} +1	V	
V_{IH}	Input High Voltage	V_{SS} −1		V_{SS} +1	V	
I_{OH1}	Output High Current	600	1800	4000	μA	T_A = 25°C
I_{OH2}	Output High Current	500	1500	4000	μA	T_A = 70°C
I_{OL}	Output Low Current	See Note Three				R_{LOAD} [4] = 100Ω
V_{OH1}	Output High Voltage	60	180	400	mV	T_A = 25°C
V_{OH2}	Output High Voltage	50	150	400	mV	T_A = 70°C
V_{OL}	Output Low Voltage	See Note Three				

NOTES:
1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
2. ($V_{BB} - V_{SS}$) supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

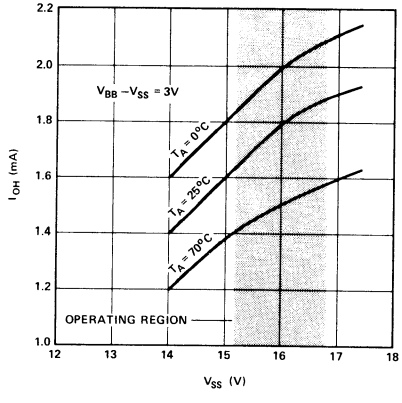
Supply Current vs Temperature



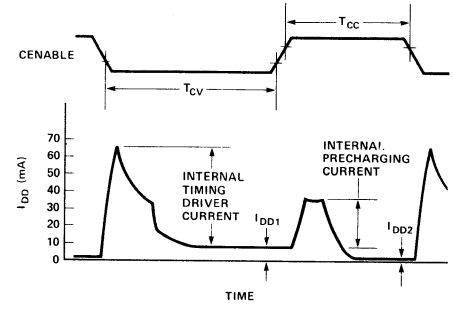


Typical Characteristics

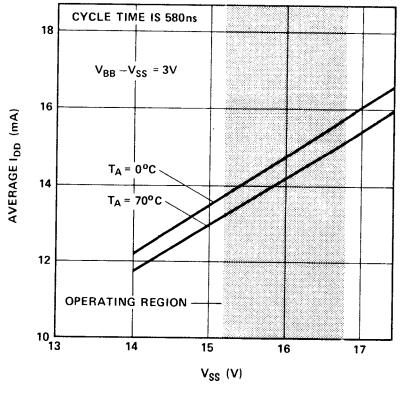
OUTPUT HIGH CURRENT VS. SUPPLY VOLTAGE



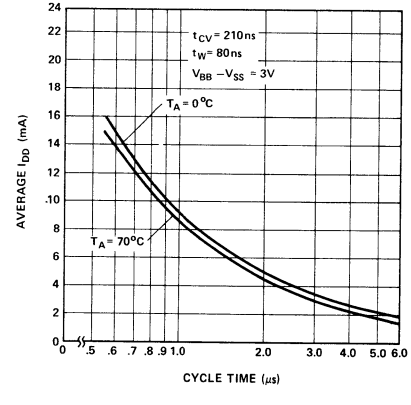
I_{DD} VS. CENABLE



AVERAGE I_{DD} VS. SUPPLY VOLTAGE



AVERAGE I_{DD} VS. 1103A CYCLE TIME



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{SS} = 16V \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$

READ, WRITE, AND READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	230		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	480		ns	$t_T = 20ns$; $C_{LOAD} = 100pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 40mV$
t_{CV}	Cenable on Time	210	500	ns	
t_{CO}	Cenable Output Delay		185	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		205	ns	$t_{ACC} = t_{AC\ MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	580		ns	$t_T = 20ns$
t_{RWC}	Read/Write Cycle	580		ns	
t_{CW}	Cenable to Read/Write Delay	210	500	ns	
t_{WP}	Read/Write Pulse Width	50		ns	
t_W	Read/Write Set Up Time	80		ns	
t_{DW}	Data Set Up Time	105		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		185	ns	$C_{LOAD} = 100pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 40mV$
t_{WC}	Read/Write to Cenable	0		ns	

CAPACITANCE[1] $T_A = 25°C$

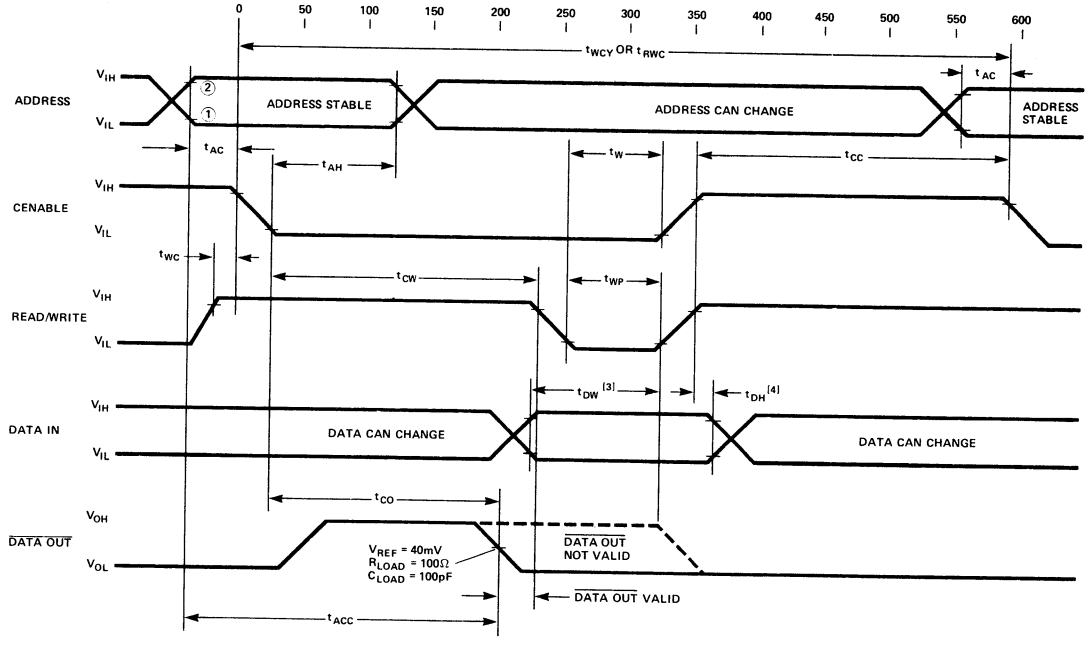
Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V; $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$; $V_{OUT} = 0V$

f = 1MHz. All unused pins are at A.C. ground.

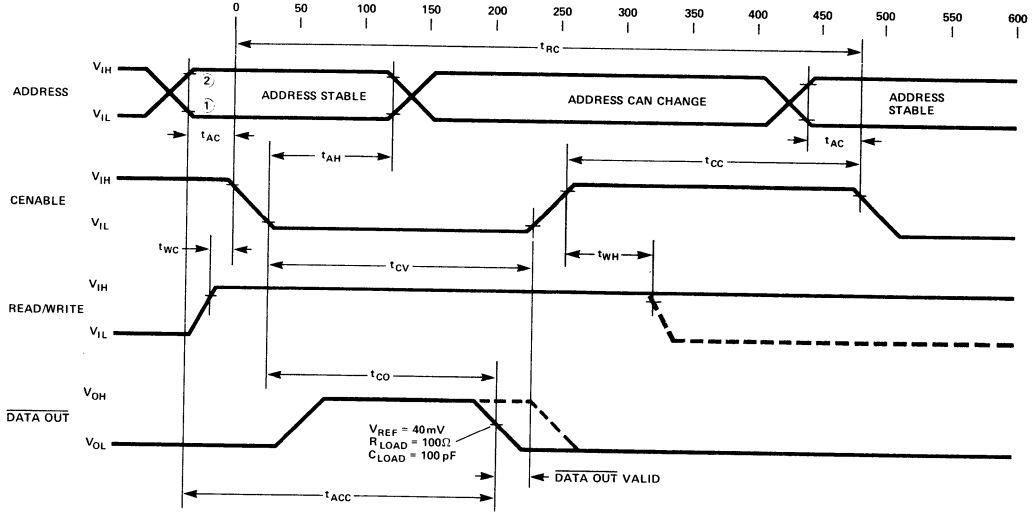
NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



READ CYCLE



NOTES:

(1) V_{DD} + 2V
(2) V_{SS} − 2V
t_T is defined as the transition between these two points.

3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of Read/Write.

1024 x 1 BIT DYNAMIC RAM

- **High Speed 1103A — Access Time — 145 ns / Cycle Time — 340 ns**
- ***No Precharge Required -- Critical Precharge Timing is Eliminated**
- **Low Standby Power Dissipation -- 0.2 µW/Bit Typical**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion -- Chip Enable Input Lead**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

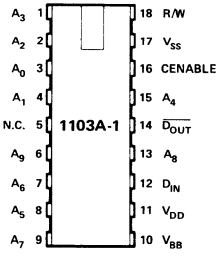
The Intel®1103A-1 is a high speed 1024 bit dynamic random access memory and is the fastest version of the standard 1103A. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

1103A-1 systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

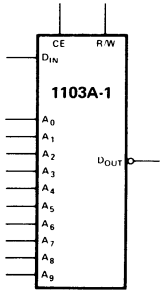
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every one millisecond. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A-1 is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



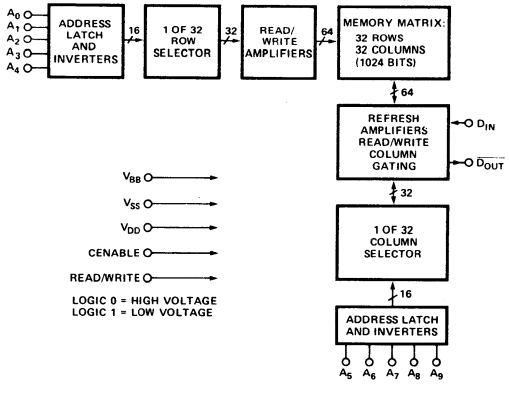
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to 70°C

Storage Temperature ..... −65°C to +150°C

All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} ..... −25V to 0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} ..... −25V to 0.3V

Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

$T_A = 0°C$ to $+55°C$, V_{SS}[1] $= 19V \pm 5\%$, $(V_{BB} - V_{SS})$[2] $= 3V$ to $4V$, $V_{DD} = 0V$ unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			10	μA	$V_{IN} = 0V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 0V$
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}	Supply Current During Cenable On		7	11	mA	Cenable = 0V; $T_A = 25°C$
I_{DD2}	Supply Current During Cenable Off		0.01	0.5	mA	Cenable = V_{SS}; $T_A = 25°C$
I_{DDAV}	Average Supply Current		25	33	mA	Cycle Time = 340ns; $T_A = 25°C$
V_{IL}	Input Low Voltage	$V_{DD}-1$		$V_{DD}+1$	V	
V_{IH}	Input High Voltage	$V_{SS}-1$		$V_{SS}+1$	V	
I_{OH1}	Output High Current	1150	1800	7000	μA	$T_A = 25°C$ ┐
I_{OH2}	Output High Current	900	1600	7000	μA	$T_A = 55°C$ ┤ R_{LOAD}[4] $= 100\Omega$
I_{OL}	Output Low Current	See Note Three				┘
V_{OH1}	Output High Voltage	115	180	700	mV	$T_A = 25°C$
V_{OH2}	Output High Voltage	90	160	700	mV	$T_A = 55°C$
V_{OL}	Output Low Voltage	See Note Three				

NOTES:

1. The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.
2. $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

A.C. Characteristics $T_A = 0°C$ to $55°C$, $V_{SS} = 19V \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$.

READ, WRITE, AND READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	120		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	300		ns	$t_T = 20ns$; $C_{LOAD} = 50pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 80mV$
t_{CV}	Cenable on Time	140	500	ns	
t_{CO}	Cenable Output Delay		125	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		145	ns	$t_{ACC} = t_{AC\ MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	340		ns	$t_T = 20ns$
t_{RWC}	Read/Write Cycle	340		ns	
t_{CW}	Cenable to Read/Write Delay	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		ns	
t_W	Read/Write Set Up Time	20		ns	
t_{DW}	Data Set Up Time	40		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		125	ns	$C_{LOAD} = 50pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 80mV$
t_{WC}	Read/Write to Cenable	0		ns	

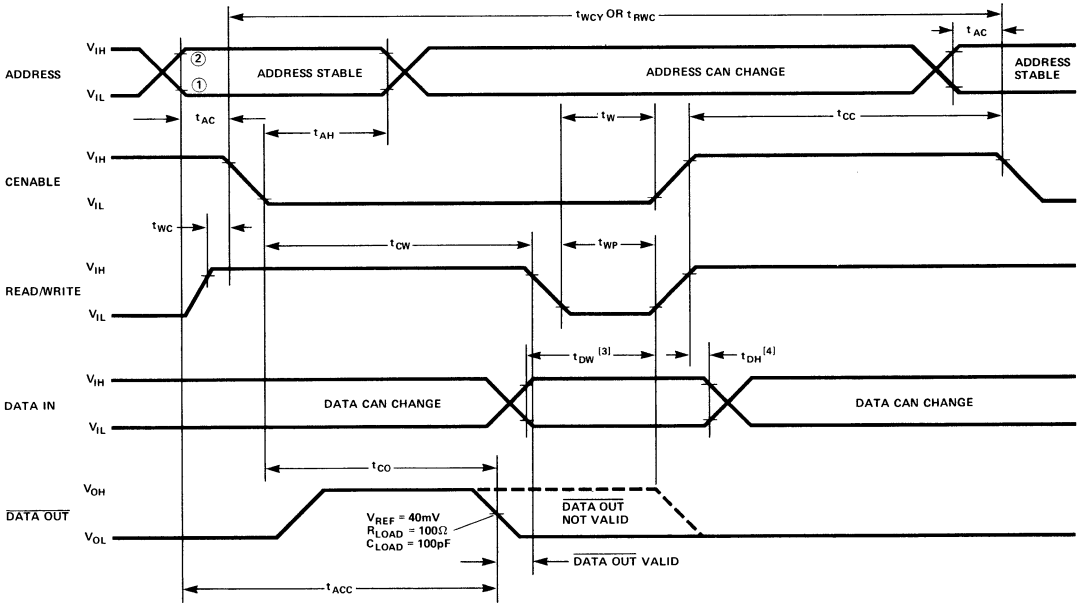
CAPACITANCE[1] $T_A = 25°C$

Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V; $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$; $V_{OUT} = 0V$

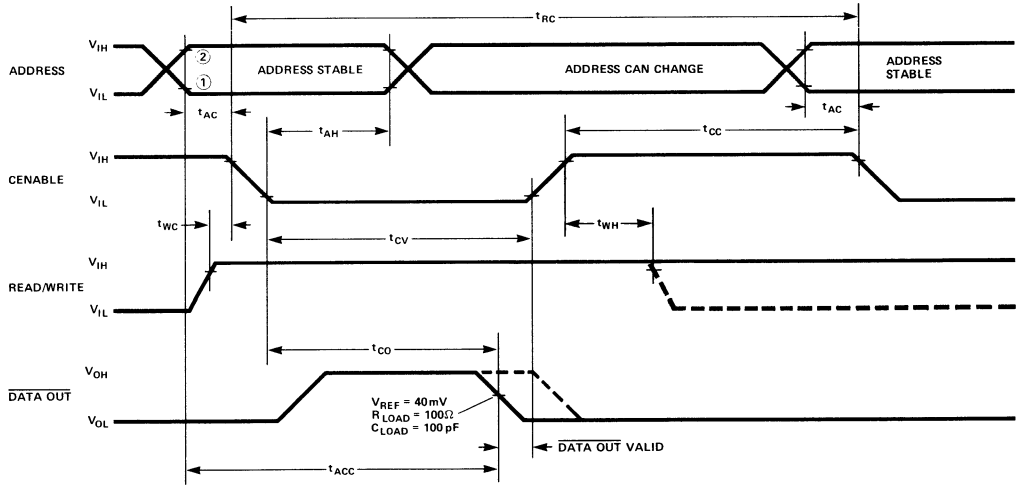
f = 1MHz. All unused pins are at A.C. ground.

NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

WRITE CYCLE OR READ/WRITE CYCLE



READ CYCLE

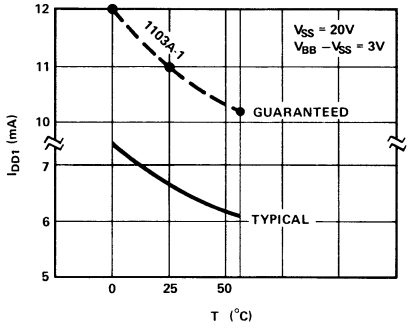


NOTES:
1. V_{DD} + 2V
2. V_{SS} − 2V

t_T is defined as the transition between these two points.

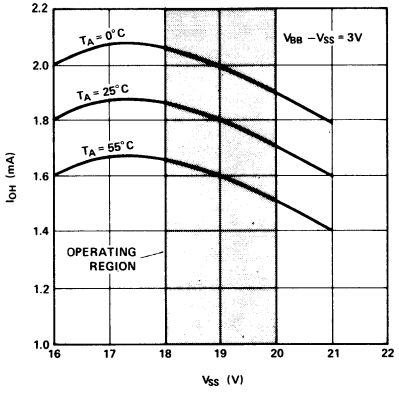
3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of Read/Write.

Supply Current vs Temperature

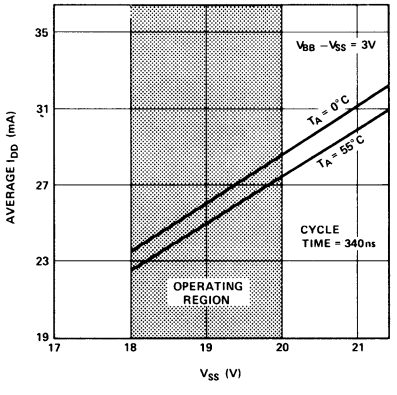


Typical Characteristics

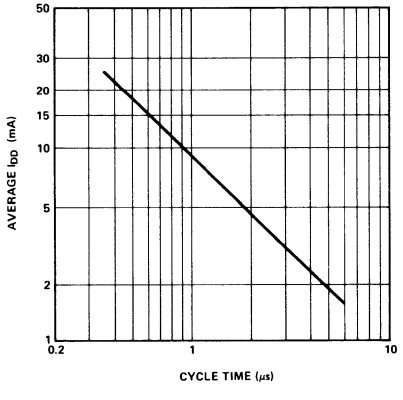
OUTPUT HIGH CURRENT VS. SUPPLY VOLTAGE



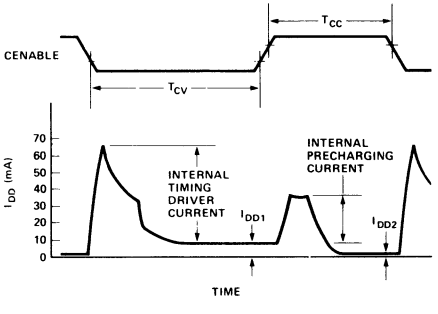
AVERAGE I_{DD} VS. SUPPLY VOLTAGE



AVERAGE I_{DD} VS. CYCLE TIME



I_{DD} VS. CENABLE



1103A-2

1024 x 1 BIT DYNAMIC RAM

- **High Speed 1103A — Access Time — 145 ns / Cycle Time — 400 ns**
- *** No Precharge Required -- Critical Precharge Timing is Eliminated**
- **Low Standby Power Dissipation -- 0.2 µW/Bit Typical**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion -- Chip Enable Input Lead**
- **Inputs Protected -- All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

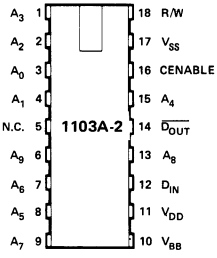
The Intel®1130A-2 is a high speed 1024 bit dynamic random access memory and is the 400 ns cycle time version of the standard 1103A. It is designed primarily for main memory applications where high performance, low cost, and large bit storage are important design objectives.

1103A-2 systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical overlap timing. Only one external clock, CENABLE, is required.

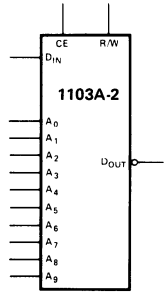
Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every one millisecond. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

The 1103A-2 is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



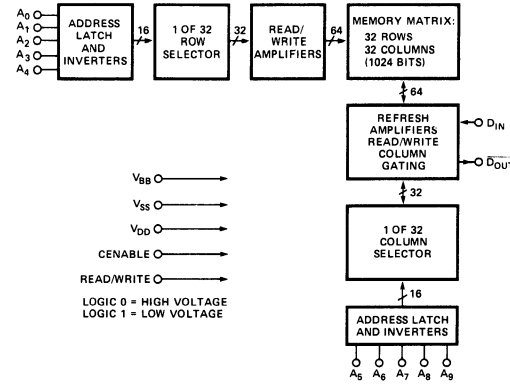
LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (INTERNALLY NOT CONNECTED)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} . . . . . −25V to 0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . . . . . −25V to 0.3V

Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to + 55°C, V_{SS}[1] = 19V ± 5%, (V_{BB} −V_{SS})[2] = 3V to 4V, V_{DD} = 0V unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}	Supply Current During Cenable On		7	11	mA	Cenable = 0V; T_A = 25°C
I_{DD2}	Supply Current During Cenable Off		0.01	0.5	mA	Cenable = V_{SS}; T_A = 25°C
I_{DDAV}	Average Supply Current		22	30	mA	Cycle Time = 400ns; T_A = 25°C
V_{IL}	Input Low Voltage	V_{DD} −1		V_{DD} +1	V	
V_{IH}	Input High Voltage	V_{SS} −1		V_{SS} +1	V	
I_{OH1}	Output High Current	1150	1800	7000	μA	T_A = 25°C
I_{OH2}	Output High Current	900	1600	7000	μA	T_A = 55°C
I_{OL}	Output Low Current	See Note Three				R_{LOAD}[4] = 100Ω
V_{OH1}	Output High Voltage	115	180	700	mV	T_A = 25°C
V_{OH2}	Output High Voltage	90	160	700	mV	T_A = 55°C
V_{OL}	Output Low Voltage	See Note Three				

NOTES:

1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL}).
2. (V_{BB} −V_{SS}) supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

A.C. Characteristics $T_A = 0°C$ to $55°C$, $V_{SS} = 19V \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$.

READ, WRITE, AND READ/WRITE CYCLE

Refer to page 2-23 for definitions.

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	Cenable Off Time	180		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	360		ns	$t_T = 20ns$; $C_{LOAD} = 50pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 80mV$
t_{CV}	Cenable on Time	140	500	ns	
t_{CO}	Cenable Output Delay		125	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		145	ns	$t_{ACC} = t_{AC\ MIN} + t_{CO} + t_T$
t_{WH}	Read/Write Hold Time	30		ns	

WRITE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	400		ns	$t_T = 20ns$
t_{RWC}	Read/Write Cycle	400		ns	
t_{CW}	Cenable to Read/Write Delay	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		ns	
t_W	Read/Write Set Up Time	20		ns	
t_{DW}	Data Set Up Time	40		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		125	ns	$C_{LOAD} = 50pF$; $R_{LOAD} = 100\Omega$; $V_{REF} = 80mV$
t_{WC}	Read/Write to Cenable	0		ns	

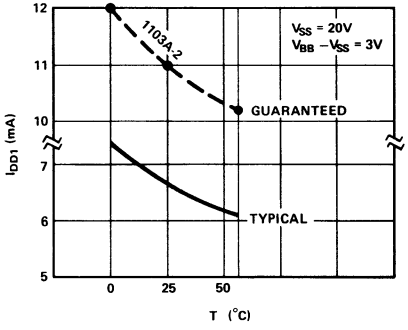
CAPACITANCE[1] $T_A = 25°C$

Symbol	Test	Typ. Plastic	Plastic Pkg. Max.	Ceramic Pkg. Max.	Unit	Conditions
C_{AD}	Address Capacitance	5	7	12	pF	$V_{IN} = V_{SS}$
C_{CE}	Cenable Capacitance	22	25	28	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write Capacitance	11	15	19.5	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input Capacitance	4	5	7.5	pF	Cenable = 0V; $V_{IN} = V_{SS}$
C_{IN2}	Data Input Capacitance	2	4	6.5	pF	Cenable = V_{SS}
C_{OUT}	Data Output Capacitance	2	3	7.0	pF	$V_{IN} = V_{SS}$; $V_{OUT} = 0V$

f = 1MHz. All unused pins are at A.C. ground.

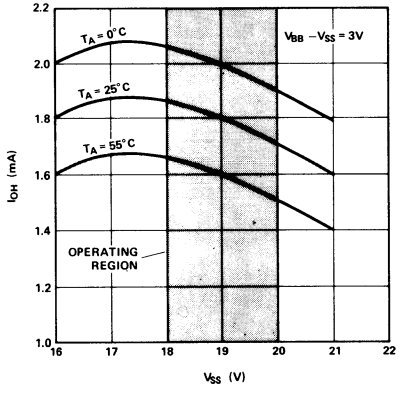
NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.

Supply Current vs Temperature

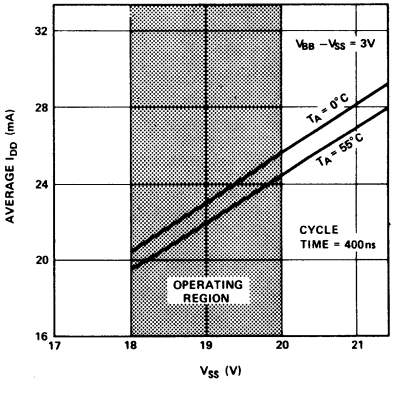


Typical Characteristics

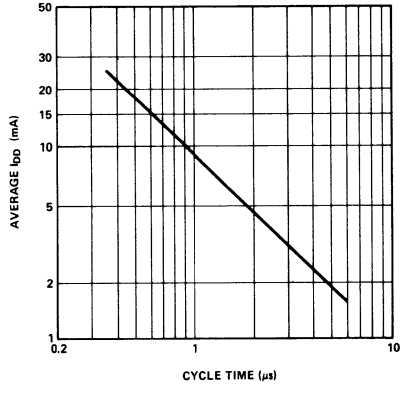
OUTPUT HIGH CURRENT VS. SUPPLY VOLTAGE



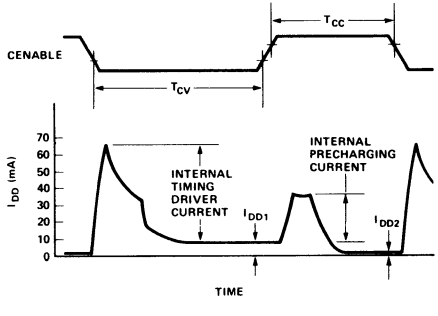
AVERAGE I_{DD} VS. SUPPLY VOLTAGE



AVERAGE I_{DD} VS. CYCLE TIME



I_{DD} VS. CENABLE



2101A

256 X 4 BIT STATIC RAM

2101A-2	250 ns Max.
2101A	350 ns Max.
2101A-4	450 ns Max.

- 256 x 4 Organization to Meet Needs for Small System Memories
- Single +5V Supply Voltage
- Directly TTL Compatible: All Inputs and Output
- Statis MOS: No Clocks or Refreshing Required
- Simple Memory Expansion: Chip Enable Input
- Inputs Protected: All Inputs Have Protection Against Static Charge
- Low Cost Packaging: 22 Pin Plastic Dual In-Line Configuration
- Low Power: Typically 150 mW
- Three-State Output: OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

The Intel® 2101A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

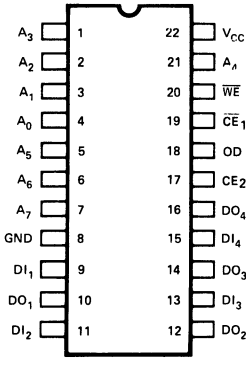
The 2101A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bi-directional logic in a common I/O system.

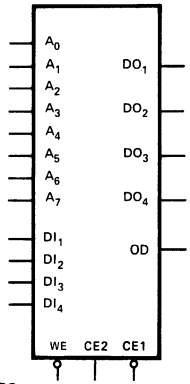
The Intel® 2101A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



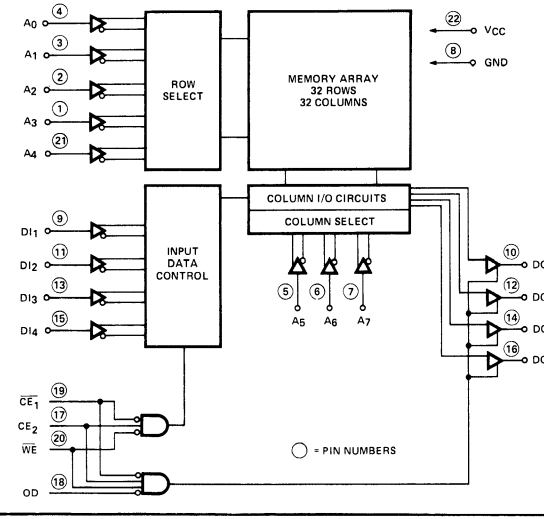
LOGIC SYMBOL



PIN NAMES

DI_1-DI_4	DATA INPUT	$\overline{CE}_2$	CHIP ENABLE 2
A_0-A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	DO_1-DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

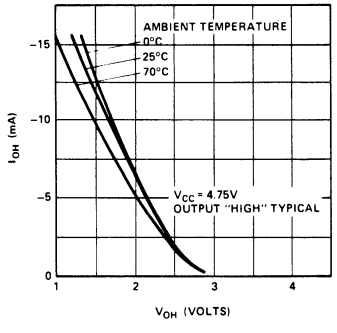
D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

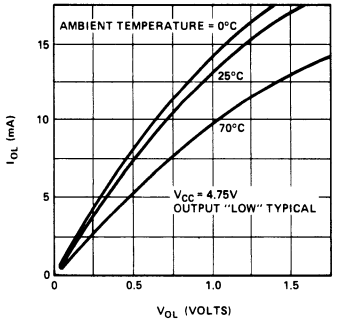
Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	Data Output Leakage Current			1	10	µA	Output Disabled, V_{OUT}=4.0V
I_{LOL}	Data Output Leakage Current			-1	-10	µA	Output Disabled, V_{OUT}=0.45V
I_{CC1}	Power Supply Current	2101A, 2101A-4		35	55	mA	V_{IN} = 5.25V, I_O = 0mA, T_A = 25°C
		2101A-2		45	65		
I_{CC2}	Power Supply Current	2101A, 2101A-4			60	mA	V_{IN} = 5.25V, I_O = 0mA, T_A = 0°C
		2101A-2			70		
V_{IL}	Input "Low" Voltage		-0.5		+0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2101A, 2101A-2	2.4			V	I_{OH} = -200µA
		2101A-4	2.4			V	I_{OH} = -150µA

TYPICAL D.C. CHARACTERISTICS

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2101A-2 (250 ns ACCESS TIME)

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	
t_A	Access Time			250	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			180	ns	Input Levels = 0.8V or 2.0V
t_{OD}	Output Disable To Output			130	ns	Timing Reference = 1.5V
t_{DF}[3]	Data Output to High Z State	0		180	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE

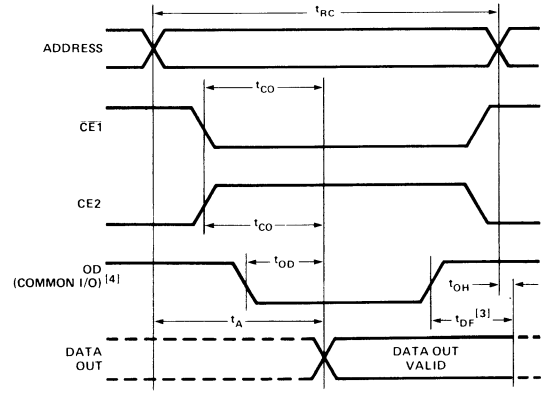
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	
t_{AW}	Write Delay	20			ns	t_r, t_f = 20ns
t_{CW}	Chip Enable To Write	150			ns	Input Levels = 0.8V or 2.0V
t_{DW}	Data Setup	150			ns	Timing Reference = 1.5V
t_{DH}	Data Hold	0			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	150			ns	and C_L = 100pF.
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

CAPACITANCE[2] $T_A = 25°C$, f = 1MHz

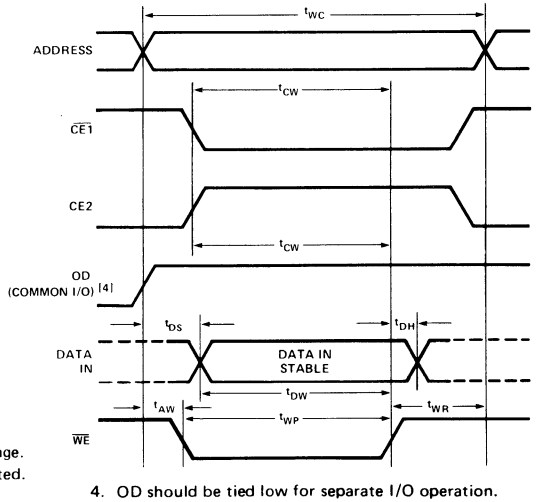
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.
4. OD should be tied low for separate I/O operation.

2101A (350 ns ACCESS TIME)

A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			350	ns	
t_{CO}	Chip Enable To Output			240	ns	
t_{OD}	Output Disable To Output			180	ns	
t_{DF} [2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	220			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	200			ns	
t_{DW}	Data Setup	200			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	200			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

2101A-4 (450 ns ACCESS TIME)

A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.

2102A, 2102AL

1K x 1 BIT STATIC RAM

P/N	Standby Pwr. (mW)	Operating Pwr. (mW)	Access (ns)
2102AL-4	35	174	450
2102AL	35	174	350
2102AL-2	42	342	250
2102A-2	—	342	250
2102A	—	289	350
2102A-4	—	289	450
2102A-6	—	289	650

- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Standby Power Mode (2102AL)**
- **Three-State Output: OR-Tie Capability**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Dual-In-Line Configuration**

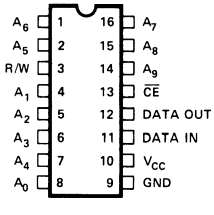
The Intel® 2102A is a high speed 1024 word by one bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. *A low standby power version (2102AL) is also available. It has all the same operating characteristics of the 2102A with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.*

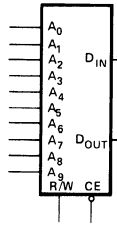
It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



LOGIC SYMBOL



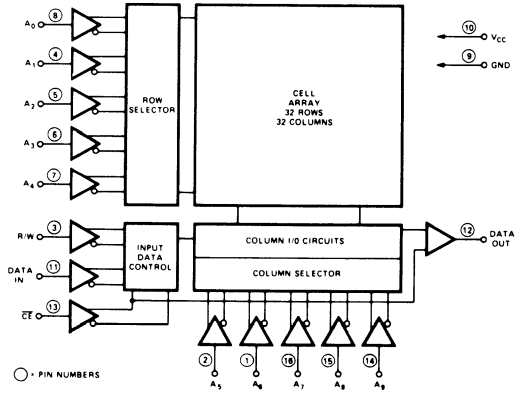
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect To Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	2102A, 2102A-4 2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102A-2, 2102AL-2 Limits Min.	Typ.[1]	Max.	2102A-6 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10		1	10		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current		1	5		1	5		1	5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = V_{OH}
I_{LOL}	Output Leakage Current		-1	-10		-1	-10		-1	-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC}	Power Supply Current		33	Note 2		45	65		33	55	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	-0.5		0.65	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			2.4			2.2			V	I_{OH} = -100μA

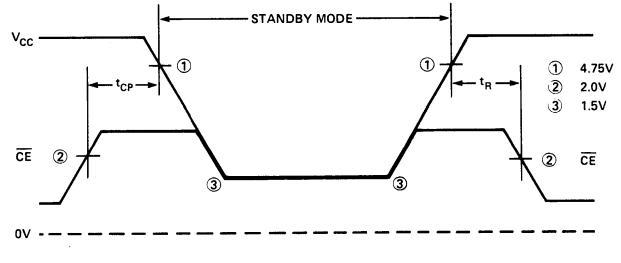
Notes: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. The maximum I_{CC} value is 55mA for the 2102A and 2102A-4, and 33mA for the 2102AL and 2102AL-4.

Standby Characteristics 2102AL, 2102AL-2, and 2102AL-4 (Available only in the Plastic Package)

T_A = 0°C to 70°C

Symbol	Parameter	2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102AL-2 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	1.5			1.5			V	
V_{CES}[2]	$\overline{CE}$ Bias in Standby	2.0			2.0			V	2.0V≤V_{PD}≤V_{CC} Max.
		V_{PD}			V_{PD}			V	1.5V≤V_{PD}< 2.0V
I_{PD1}	Standby Current		15	23		20	28	mA	All Inputs = V_{PD1} = 1.5V
I_{PD2}	Standby Current		20	30		25	38	mA	All Inputs = V_{PD2} = 2.0V
t_{CP}	Chip Deselect to Standby Time	0			0			ns	
t_R[3]	Standby Recovery Time	t_{RC}			t_{RC}			ns	

STANDBY WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min.), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
3. t_R = t_{RC} (READ CYCLE TIME).

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

READ CYCLE

Symbol	Parameter	2102A-2, 2102AL-2 Limits (ns) Min.	Max.	2102A, 2102AL Limits (ns) Min.	Max.	2102A-4, 2102AL-4 Limits (ns) Min.	Max.	2102A-6 Limits (ns) Min.	Max.
t_{RC}	Read Cycle	250		350		450		650	
t_A	Access Time		250		350		450		650
t_{CO}	Chip Enable to Output Time		130		180		230		400
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40		50	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0	

WRITE CYCLE

t_{WC}	Write Cycle	250	350	450	650
t_{AW}	Address to Write Setup Time	20	20	20	200
t_{WP}	Write Pulse Width	180	250	300	400
t_{WR}	Write Recovery Time	0	0	0	50
t_{DW}	Data Setup Time	180	250	300	450
t_{DH}	Data Hold Time	0	0	0	20
t_{CW}	Chip Enable to Write Setup Time	180	250	300	550

A.C. CONDITIONS OF TEST

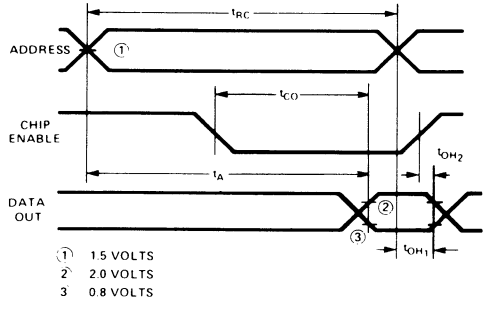
Input Pulse Levels: 0.8 Volt to 2.0 Volt
Input Rise and Fall Times: 10nsec
Timing Measurement Reference Levels: Inputs: 1.5 Volts; Output: 0.8 and 2.0 Volts
Output Load: 1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

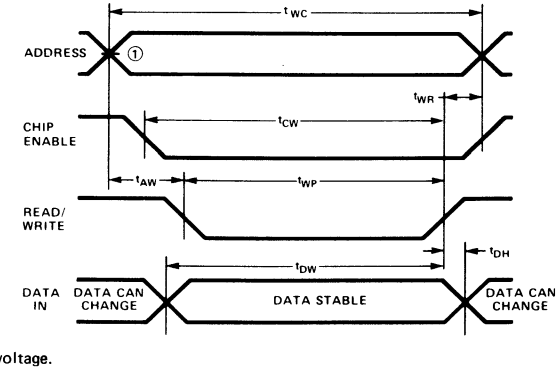
SYMBOL	TEST	LIMITS (pF) TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



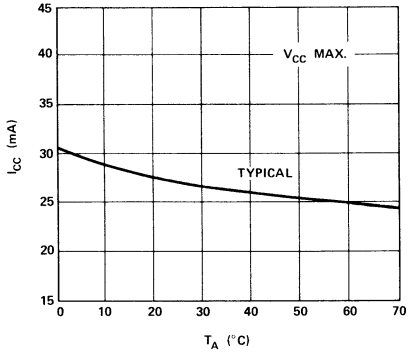
WRITE CYCLE



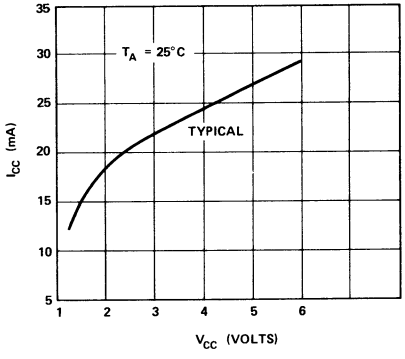
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Typical D. C. and A. C. Characteristics

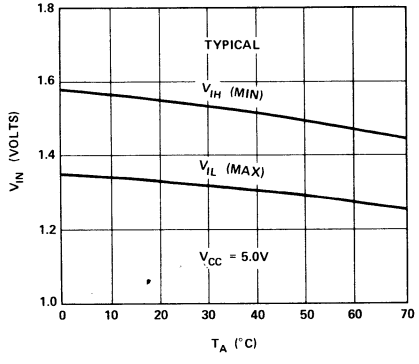
POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



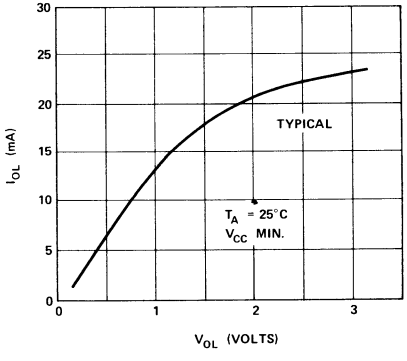
POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



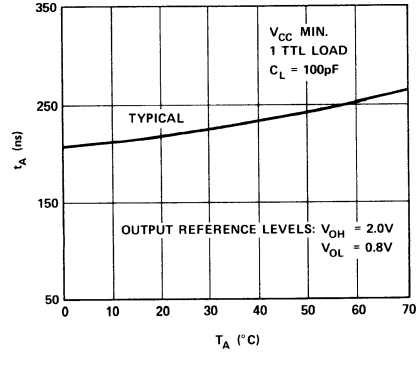
V_{IN} LIMITS VS. TEMPERATURE



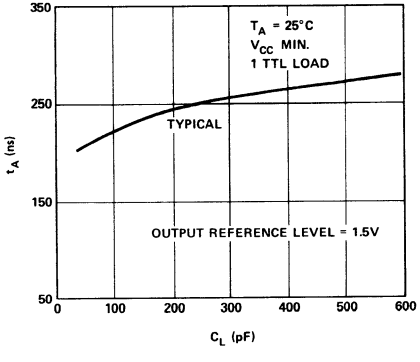
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



M2102A-4

1K x 1 BIT STATIC RAM

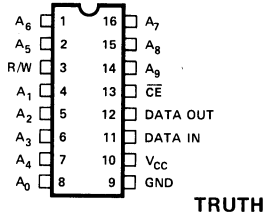
MILITARY TEMP

- 10% V_{CC} Supply Tolerance
- Directly TTL Compatible: All Inputs and Output
- Low Power: 385mW Max.
- Three State Output: OR-Tie Capability
- 16 Pin Hermetic Dual-In-Line Package

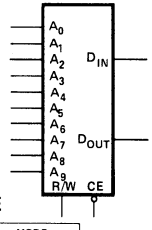
The Intel® M2102A is a high speed 1K x 1 RAM specified over the -55°C to +125°C temperature range. The RAM uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The Intel® M2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



LOGIC SYMBOL



TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . −65°C to +135°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . −0.6V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 0 to 5.5V
I_{LOH}	Output Leakage Current			10	μA	$\overline{CE}$ = Min. V_{IH} , V_{OUT} = V_{OH}
I_{LOL}	Output Leakage Current			-50	μA	$\overline{CE}$ = Min. V_{IH} , V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	All Inputs = 5.5V, Data Out Open, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	All Inputs = 5.5V, Data Out Open, T_A = -55°C
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -100 μA

NOTE 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	M2102A-4 Limits (ns) Min.	Max.
READ CYCLE			
t_{RC}	Read Cycle	450	
t_A	Access Time		450
t_{CO}	Chip Enable to Output Time		230
t_{OH1}	Previous Read Data Valid with Respect to Address	40	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0	
WRITE CYCLE			
t_{WC}	Write Cycle	450	
t_{AW}	Address to Write Setup Time	20	
t_{WP}	Write Pulse Width	300	
t_{WR}	Write Recovery Time	0	
t_{DW}	Data Setup Time	300	
t_{DH}	Data Hold Time	0	
t_{CW}	Chip Enable to Write Setup Time	300	

A.C. CONDITIONS OF TEST

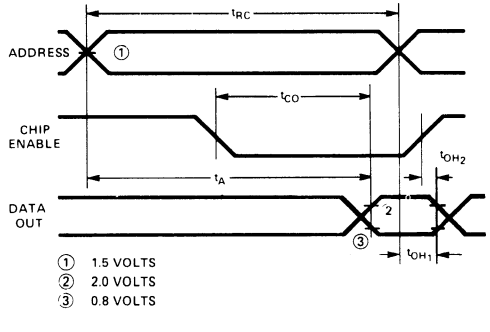
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1 MHz

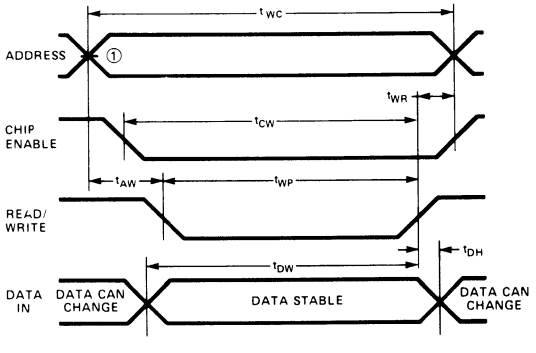
SYMBOL	TEST	LIMITS (pF) TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25° C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

2104A FAMILY
4096 x 1 BIT DYNAMIC RAM

	2104A-1	2104A-2	2104A-3	2104A-4
Max. Access Time (ns)	150	200	250	300
Read, Write Cycle (ns)	320	320	375	425
Max. IDD (mA)	35	32	30	30

- **Highest Density 4K RAM Industry Standard 16 Pin Package**
- **Low Power 4K RAM**
- **All Inputs Including Clocks TTL Compatible**
- **±10% Tolerance on All Power Supplies +12V, +5V, -5V**
- **Refresh Period: 2 ms**
- **On-Chip Latches for Addresses, Chip Select and Data In**
- **Simple Memory Expansion: Chip Select**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **Compatible with Intel® 2116 16K RAM**

The Intel® 2104A is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density.

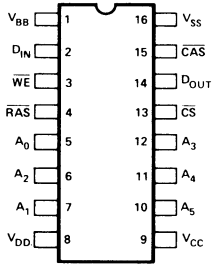
The efficient design of the 2104A allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104A on 6 address input pins. The two 6 bit address words are latched into the 2104A by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

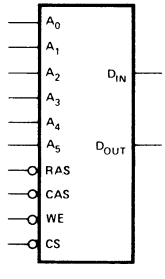
A new unique dynamic storage cell provides high speed along with low power dissipation and wide voltage margins. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2 milliseconds.

The 2104A is designed for page mode operation, "$\overline{RAS}$-only refreshing," and "$\overline{CAS}$-only deselection." Thus it is compatible with the Intel® 2116, 16K RAM.

PIN CONFIGURATION



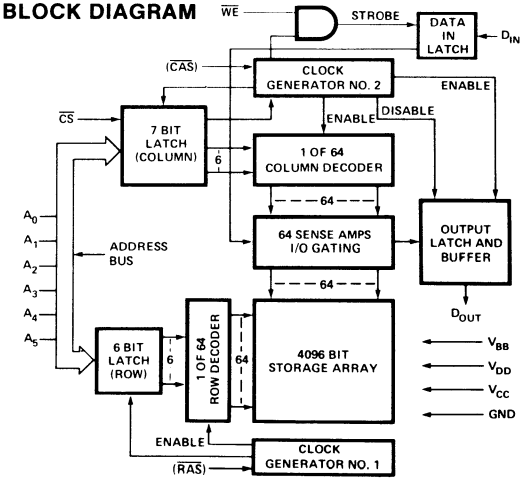
LOGIC DIAGRAM



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	WE	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - $V_{BB} \geq 4.5V$) ..... -0.3V to +20V
Power Dissipation 1.0W
Data Out Current ..... 50 mA

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

T_A = 0° to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions	
		Min.	Typ.[2]	Max.			
I_{LI}	Input Load Current (any input)			10	µA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			10	µA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V	
I_{DD1}[3]	V_{DD} Standby Current		0.7	2	mA	V_{DD} = 13.2V	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip deselected prior to measurement. See Note 5.
			0.7	1.5	mA	V_{DD} = 12.6V	
I_{BB1}	V_{BB} Standby Current		5	50	µA	V_{DD} = 13.2V	
I_{DD2}[3]	Operating V_{DD} Current (Device Selected)		24	35	mA	2104A-1	t_{CYC} = 320 ns
			22	32	mA	2104A-2	t_{CYC} = 320 ns
			20	30	mA	2104A-3, 4	t_{CYC} = 375 ns
I_{BB2}	Operating V_{BB} Current		160	400	µA	Device Selected. Min cycle time.	
I_{CC1}[4]	V_{CC} Supply Current when Deselected			10	µA		
I_{DD3}	Operating V_{DD} Current ($\overline{RAS}$-only cycle)		12	25	mA	2104A-1, 2	t_{CYC} = 320 ns
			10	22	mA	2104A-3, 4	t_{CYC} = 375 ns
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V		
V_{IH}	Input High Voltage	2.4		7.0	V		
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 3.2 mA	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA	

CAPACITANCE[6] T_A = 25°C

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	3	7	pF	V_{IN} = V_{SS}
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{WRITE}$	3	7	pF	V_{IN} = V_{SS}
C_O	Output Capacitance (D_{OUT})	4	7	pF	V_{OUT} = 0V
C_{I3}	Input Capacitance $\overline{CAS}$	6	7	pF	V_{IN} = V_{SS}

Notes: 1. All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycles containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} current flows to V_{SS}.
4. When chip is selected V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.
5. The chip is deselected; i.e., output is brought to high impedance state by $\overline{CAS}$-only cycle or by a read cycle with $\overline{CS}$ at V_{IH}.
6. Capacitance measured with Boonton Meter.

A.C.CHARACTERISTICS[1]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, AND READ MODIFY WRITE CYCLES

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{REF}	Time Between Refresh		2		2		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	100		115		115		125		ns
t_{CP}	$\overline{CAS}$ Precharge Time	60		80		110		110		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	20	50	25	70	35	110	80	135	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	100		130		140		165		ns
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		300		ns
t_{AR}	$\overline{RAS}$ to Address or $\overline{CS}$ Hold Time	95		120		160		215		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		0		ns
t_{ASC}	Column Address or $\overline{CS}$ Set-Up Time	-5		0		0		0		ns
t_{RAH}	Row Address Hold Time	20		25		35		80		ns
t_{CAH}	Column Address or $\overline{CS}$ Hold Time	45		50		50		80		ns
t_T	Rise or Fall Time		50		50		50		50	ns
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	60	0	60	0	80	ns
t_{CAC}[3]	Access Time From $\overline{CAS}$		100		130		140		165	ns
t_{RAC}[3]	Access Time From $\overline{RAS}$		150		200		250		300	ns

READ CYCLE

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		320		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	32000	200	32000	250	32000	300	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		130		140		165		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{RCH}	Read Command Hold Time	0		0		0		0		ns
t_{DOH}	Data Out Hold Time	32		32		32		32		μs

WRITE CYCLE[4]

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		320		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	32000	200	32000	250	32000	300	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		130		140		165		ns
t_{WCS}	Write Command Set-Up Time	0		0		0		0		ns
t_{WCH}	Write Command Hold Time	55		75		75		80		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	105		145		185		215		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	100		130		140		150		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		130		140		150		ns
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		75		75		80		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	105		145		185		215		ns

Notes: 1. All voltages referenced to V_{SS}. Minimum timings do not allow for t_T or skews.

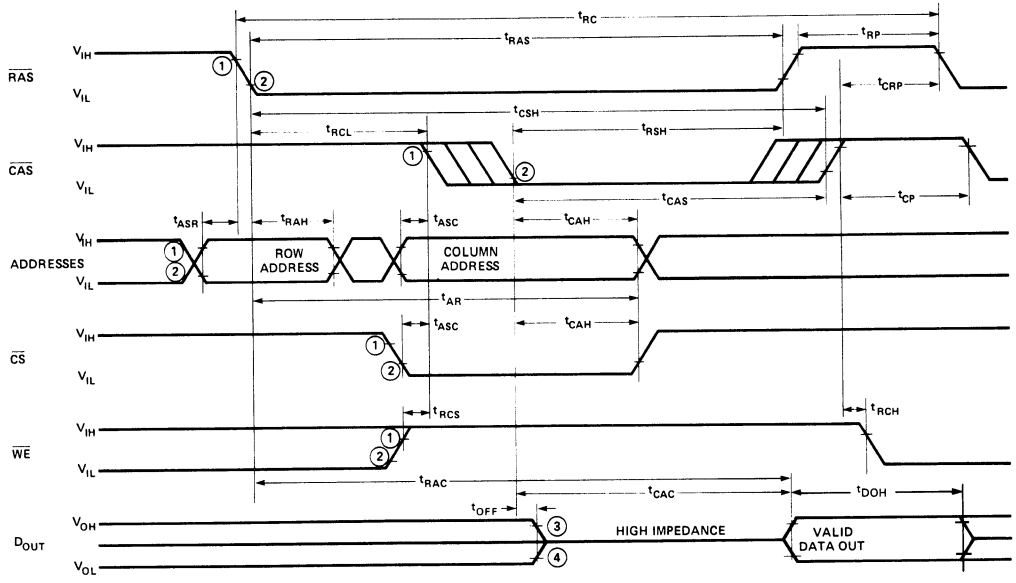
2. $\overline{CAS}$ must remain at V_{IH} a minimum of $t_{RCL\ MIN}$ after RAS switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before t_{RCL} of $t_{RAC} - t_T - t_{CAC}$ as described in the Applications Information on page 2-45. $t_{RCL\ MAX}$ is given for reference only as $t_{RAC} - t_{CAC}$.

3. Load = 2 TTL and 100 pF. See Applications Information.

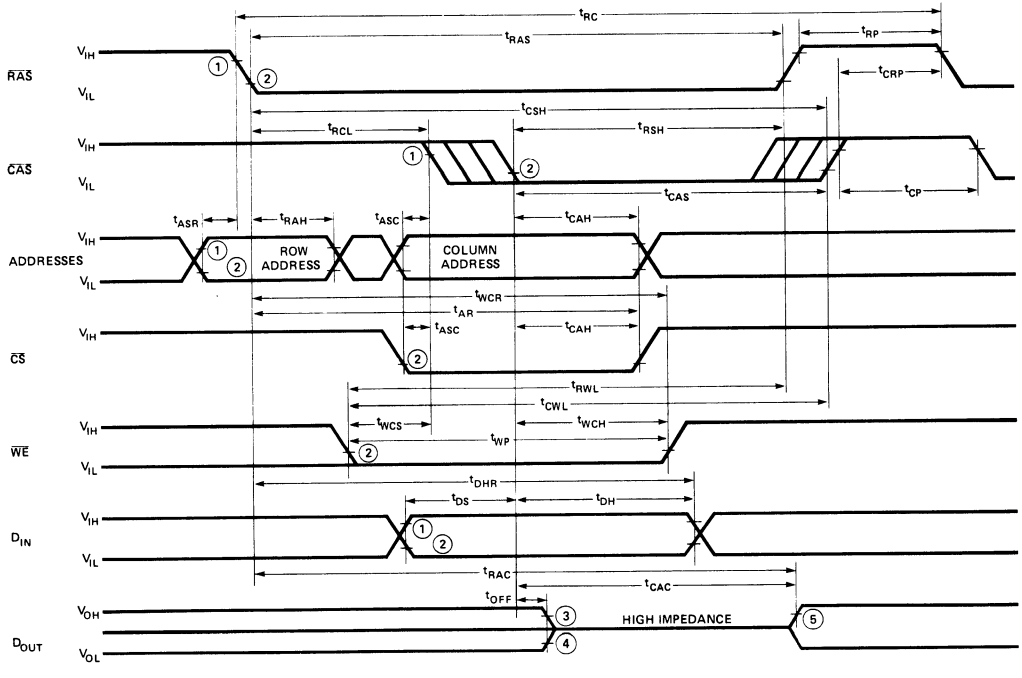
4. In a write cycle D_{OUT} latch will contain data written into cell. In a read-modify-write cycle D_{OUT} latch will contain data read from cell. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} is indeterminate.

WAVEFORMS

READ CYCLE



WRITE CYCLE



(See page 2-44 for notes)

A.C.CHARACTERISTICS[1]

T_A = 0° to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

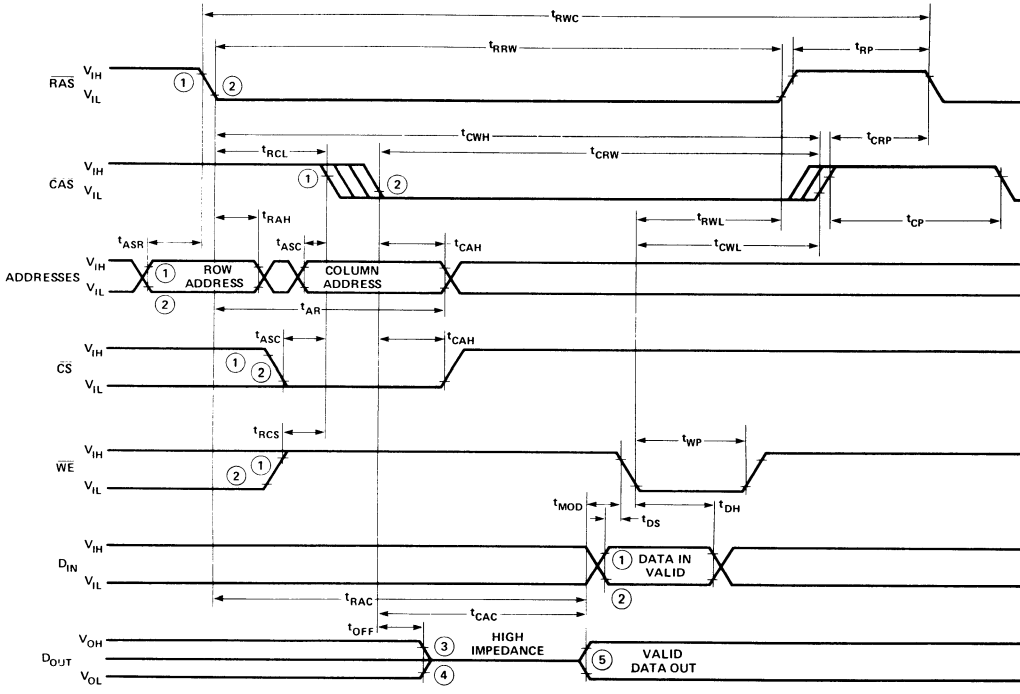
READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2104A-1 Min.	2104A-1 Max.	2104A-2 Min.	2104A-2 Max.	2104A-3 Min.	2104A-3 Max.	2104A-4 Min.	2104A-4 Max.	Unit
t_{RWC}	Read Modify Write Cycle Time[2]	350		445		505		575		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	200		260		280		315		ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	250		330		390		450		ns
t_{RWL}	RMW Cycle $\overline{RAS}$ Lead Time	100		130		140		150		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	250		330		390		450		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		130		140		150		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{MOD}	Modify Time	0	10	0	10	0	10	0	10	μs
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		75		75		80		ns

Notes: 1. All voltages referenced to V_{SS}.
2. The minimum cycle timing does not allow for t_T or skews.

WAVEFORMS

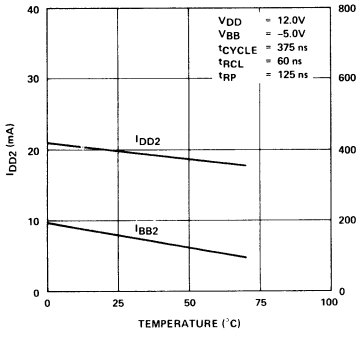
READ-MODIFY-WRITE CYCLE



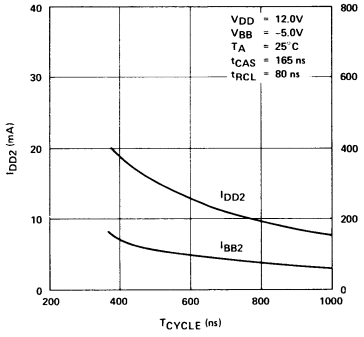
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. In a write cycle D_{OUT} latch will contain data written into cell. In a read-modify-write cycle D_{OUT} latch will contain data read from cell. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} is indeterminate.

TYPICAL CHARACTERISTICS

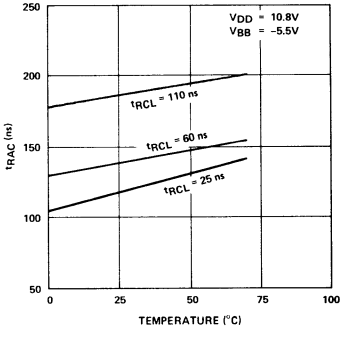
TYPICAL I_{BB2} AND I_{DD2} VS. TEMPERATURE



TYPICAL I_{BB2} AND I_{DD2} VS. CYCLE TIME



TYPICAL ACCESS TIME VS. TEMPERATURE



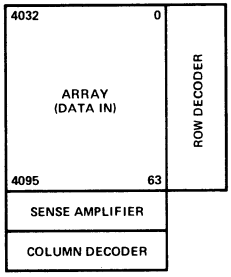
APPLICATIONS

ADDRESSING

Two externally applied negative going TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$), are used to strobe the two sets of 6 addresses into internal address buffer registers. The first clock, $\overline{RAS}$, strobes in the six low order addresses (A_0-A_5) which selects one of 64 rows and begins the timing which enables the column sense amplifiers. The second clock, $\overline{CAS}$, strobes in the six high order addresses (A_6-A_{11}) to select one of 64 column sense amplifiers and Chip Select ($\overline{CS}$) which enables the data out buffer.

An address map of the 2104A is shown below. Address "0" corresponds to all addresses at V_{IL}. All addresses are sequentially located on the chip.

2104A Address Map



DATA CYCLES/TIMING

A memory cycle begins with addresses stable and a negative transition of $\overline{RAS}$. See the waveforms on page 4. It is not necessary to know whether a Read or Write cycle is to be performed until $\overline{CAS}$ becomes valid.

Note that Chip Select ($\overline{CS}$) does not have to be valid until the second clock, $\overline{CAS}$. It is, therefore, possible to start a memory cycle before it is known which device must be selected. This can result in a significant improvement in system access time since the decode time for chip select does not enter into the calculation for access time.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks are TTL compatible and do not require level shifting and driving at high voltage MOS levels. Buffers internal to the 2104A convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104A system access time.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during $\overline{CAS}$. The output pin of a selected device will unconditionally go to a high impedance state immediately following the leading edge of $\overline{CAS}$ and remain in this state until valid data appears at the output at access time. The selected output data is internally latched and will remain valid until a subsequent $\overline{CAS}$ is given to the device by a Read, Write, Read-Modify-Write, $\overline{CAS}$ only or Refresh cycle. Data-out goes to a high impedance state for all non-selected devices.

Device access time, t_{ACC}, is the longer of two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCL} + t_T + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe lead time, t_{RCL}, and transition time, t_T, are system dependent timing parameters. For example, substituting the device parameters of the 2104A-4 and assuming a TTL level transition time of 5 ns yields:

3. $t_{ACC} = t_{RAC}$ = 300ns for 80 nsec $\leqslant t_{RCL} \leqslant$ 130nsec

OR

4. $t_{ACC} = t_{RCL} + t_T + t_{CAC} = t_{RCL}$+170ns for t_{RCL}>130ns.

Note that if 80 nsec $\leq t_{RCL} \leq$ 130 nsec, device access time is determined by equation 3 and is equal to t_{RAC}. If $t_{RCL} >$ 130 nsec, access time is determined by equation 4. This 50ns interval (shown in the t_{RCL} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$. This allowance for a t_{RCL} skew is designed in at the device level to allow minimum access times to be achieved in practical system designs.

WRITE CYCLE

A Write Cycle is generally performed by bringing Write Enable ($\overline{WE}$) low before $\overline{CAS}$. D_{OUT} will be the data written into the cell addressed. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} will be indeterminate.

READ-MODIFY-WRITE CYCLE

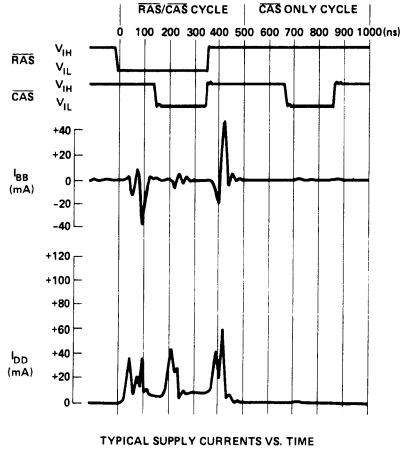
A Read-Modify-Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low after access time, t_{RAC}, with $\overline{RAS}$ and $\overline{CAS}$ low. Data in must be valid at or before the falling edge of $\overline{WE}$. In a read-modify-write cycle D_{OUT} is data read and does not change during the modify-write portion of the cycle.

$\overline{CAS}$ ONLY (DESELECT) CYCLE

In some applications, it is desirable to be able to deselect all memory devices without running a regular memory cycle. This may be accomplished with the 2104A by performing a $\overline{CAS}$-Only Cycle. Receipt of a $\overline{CAS}$ without $\overline{RAS}$ deselects the 2104A and forces the Data Output to the high-impedance state. This places the 2104A in its lowest power, standby condition. I_{DD} will be about twice I_{DD1} for the first cycle of $\overline{CAS}$-only deselection and I_{DD1} for any additional $\overline{CAS}$-only cycles. The cycle timing and $\overline{CAS}$ timing should be just as if a normal $\overline{RAS}$/$\overline{CAS}$ cycle was being performed.

CHIP SELECTION/DESELECTION

The 2104A is selected by driving $\overline{CS}$ low during a Read, Write, or Read-Modify-Write cycle. A device is deselected by 1) driving $\overline{CS}$ high during a Read, Write, or Read-Modify-Write cycle or 2) performing a $\overline{CAS}$ Only cycle independent of the state of $\overline{CS}$.



TYPICAL SUPPLY CURRENTS VS. TIME

REFRESH CYCLES

Each of the 64 rows internal to the 2104A must be refreshed every 2 msec to maintain data. Any data cycle (Read, Write, Read-Modify-Write) refreshes the entire selected row (defined by the low order row addresses). The refresh operation is independent of the state of chip select. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected ($\overline{CS}$ high) if it is desired not to change the state of the selected cell.

$\overline{RAS}$/$\overline{CAS}$ TIMING

The device clocks, $\overline{RAS}$ and $\overline{CAS}$, control operation of the 2104A. The timing of each clock and the timing relationships of the two clocks must be understood by the user in order to obtain maximum performance in a memory system.

The $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle must not begin until the minimum precharge time, t_{RP}, has been met.

PAGE MODE OPERATION

The 2104A is designed for page mode operation and is presently being characterized for that mode. Specifications will be available at a later date.

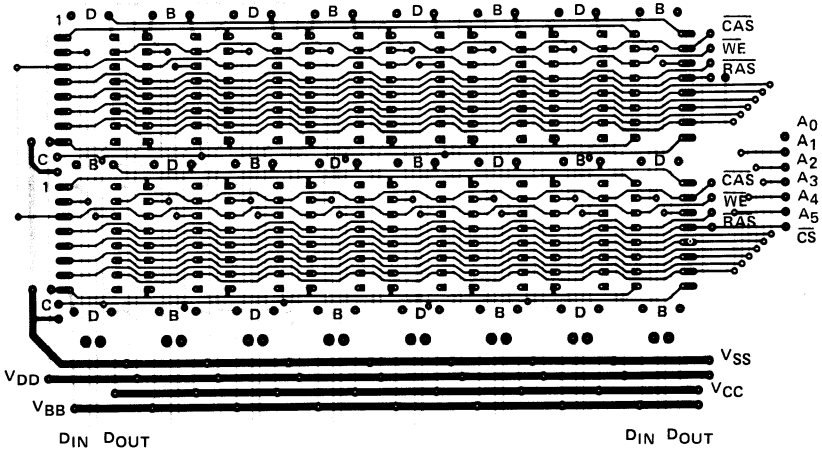
POWER SUPPLY

Typical power supply current waveforms versus time are shown below for both a $\overline{RAS}$/$\overline{CAS}$ cycle and a $\overline{CAS}$ only cycle. I_{DD} and I_{BB} current surges at $\overline{RAS}$ and $\overline{CAS}$ edges make adequate decoupling of these supplies important. Due to the high frequency noise component content of the current waveforms, the decoupling capacitors should be low inductance, ceramic units selected for their high frequency performance.

It is recommended that a 0.1 μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1 μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10 μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

A 0.01 μF ceramic capacitor is recommended between V_{CC} and V_{SS} at every eighth device to prevent noise coupling to the V_{CC} line which may affect the TTL peripheral logic in the system.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double-sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1 μF to V_{DD} TO V_{SS}
B = 0.1 μF V_{BB} TO V_{SS}
C = 0.01 μF V_{CC} TO V_{SS}

2107A

4096 x 1 BIT DYNAMIC RAM

Product	2107A-1	2107A	2107A-4	2107A-5
Access Time	280 ns	300 ns	350 ns	420 ns

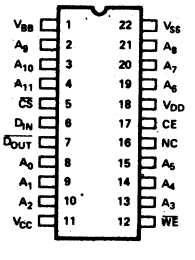
- Low Cost Per Bit
- Low Standby Power
- Easy System Interface
- Only One High Voltage Input Signal – Chip Enable
- Low Level Address, Data, Write Enable, Chip Select Inputs
- Address Registers Incorporated on the Chip
- Simple Memory Expansion: Chip Select Input Lead
- Fully Decoded: On Chip Address Decode
- Output is Three State and TTL Compatible
- Ceramic and Plastic 22-Pin DIPs

The Intel 2107A is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107A uses dynamic circuitry which reduces the operation and standby power dissipation.

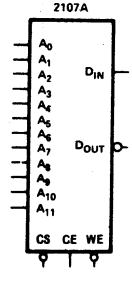
Reading information from the memory is non-destructive. Refreshing is accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107A is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies.

PIN CONFIGURATION



LOGIC SYMBOL

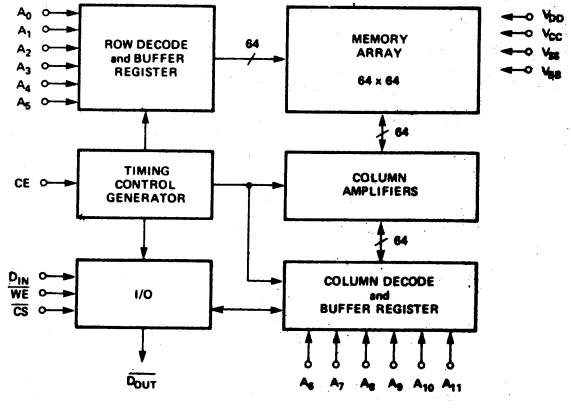


PIN NAMES

D_{IN}	DATA INPUT	CE	CHIP ENABLE
A_0-A_{11}	ADDRESS INPUTS*	$\overline{D_{OUT}}$	DATA OUTPUT
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	NC	NOT CONNECTED

*Refresh Addresses A_0-A_5.

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to 70°C

Storage Temperature ..... −65°C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} ..... +25V to −0.3V

Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} ..... +20V to −0.3V

Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB}[1] = -5V ± 5%, V_{SS} = 0V, unless otherwise notes.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LC}	Input Load Current		.01	10	μA	$V_{IN} = V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	μA	CE = -1V to +.8V or $\overline{CS}$ = 3.5V, V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		.1	100	μA	CE = -1V to +.8V
I_{DD2}	V_{DD} Supply Current during CE on[5]		14	22	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\ AV}$	Average V_{DD} Supply Current	(See Table 1)				T_A = 25°C, Fig. 1,3
I_{CC1}	V_{CC} Supply Current during CE off		.01	10	μA	CE = -1V to +.8V
I_{CC2}	V_{CC} Supply Current during CE on		5	10	mA	CE = V_{IHC}, T_A = 25°C
$I_{CC\ AV}$	Average V_{CC} Supply Current	(See Table 1)				T_A = 25°C, Fig. 2,4
I_{BB}	V_{BB} Supply Current		1	100	μA	
V_{IL}	Input Low Voltage[4]	−1.0		0.8	V	
V_{IH}	Input High Voltage[4]	3.5		V_{CC} +1	V	
V_{ILC}	CE Input Low Voltage[4]	−1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD} −1		V_{DD} +1	V	
V_{OL}	Output Low Voltage[4]	0.0		0.45	V	I_{OL} = 1.7mA, Fig. 6
V_{OH}	Output High Voltage[4]	2.4		V_{CC}	V	I_{OH} = -100μA, Fig. 5

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. Referenced to V_{SS} unless otherwise noted.
5. For 2107A-4 and 2107A-5 I_{DD2} is 25mA max.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameters	2107A		2107A-1		2107A-4		2107A-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{REF} [1]	Time Between Refresh		2		1		2		2	ms
t_{AC}	Address to CE Set Up Time	0		0		0		0		ns
t_{AH}	Address Hold Time	100		100		100		100		ns
t_{CC}	CE Off Time	180		100		200		250		ns
t_T	CE Transition Time		50		50		50		50	ns
t_{CF}	CE Off to Output High Impedance State	0		0		0		0		ns

READ CYCLE

Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{RCY} [2]	Read Cycle Time	500		420		570		690		ns
t_{CER}	CE On Time During Read	280	3000	280	3000	330	3000	400	300	ns
t_{CO}	CE Output Delay		280		260		330		400	ns
t_{ACC} [3]	Address to Output Access		300		280		350		420	ns
t_{WL}	CE to $\overline{WE}$ Low	0		0		0		0		ns
t_{WC}	$\overline{WE}$ to CE on	0		0		0		0		ns

WRITE CYCLE

Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{WCY} [2]	Write Cycle Time	700		550		840		970		ns
t_{CEW}	CE Width During Write	480	3000	410	3000	600	3000	680	3000	ns
t_W	$\overline{WE}$ to CE Off	340		250		400		450		ns
t_{CW}	CE to $\overline{WE}$ High	300		250		—		—		ns
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		0		ns
t_{CD} [4]	CE to D_{IN} Set Up		50		50		50		50	ns
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns
t_{WP}	$\overline{WE}$ Pulse Width	150		150		200		200		ns
t_{WW} [5]	$\overline{WE}$ Wait	0		0		170		200		ns
t_{WC}	$\overline{WE}$ to CE On	0		0		0		0		ns

Capacitance [6] $T_A = 25°C$

Symbol	Test	Plastic And Ceramic Pkg. Typ.	Max.	Unit	Conditions
C_{AD}	Address Capacitance, $\overline{CS}$, $\overline{WE}$, D_{IN}	3	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	3	6	pF	$V_{OUT} = 0V$

Notes:
1. For plastic 2107A-4 and 2107A-5 $t_{REF} = 1mS$.
2. $t_T = 20ns$
3. $C_{LOAD} = 50$ pf; Load = 1 TTL; Ref = 2.0V for high, 0.8V for low; $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$.
4. t_{CD} applies only when $t_W > t_{CEW} - 50ns$.
5. The 2107A and 2107A-1 should not be operated with t_{WW} in the 50 to 170 ns range.
6. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with the current equal to a constant 20mA.

D.C. Characteristics

FIGURE 1
I_{DD} AVERAGE VS. TEMPERATURE

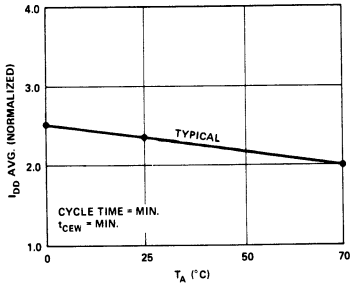


FIGURE 2
I_{CC} AVERAGE VS. TEMPERATURE

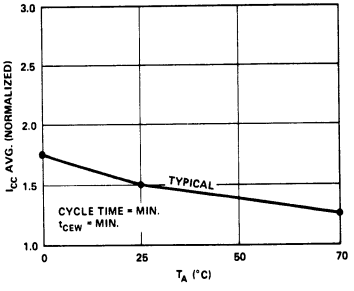


FIGURE 3
TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

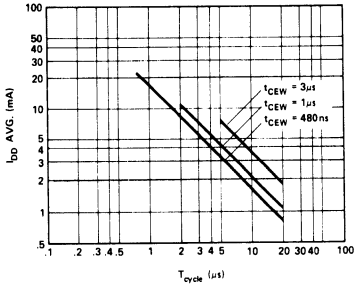


FIGURE 4
TYPICAL I_{CC} AVERAGE VS. CYCLE TIME

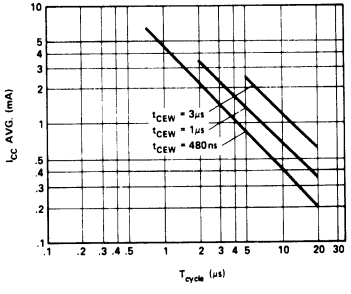


FIGURE 5
TYPICAL I_{OH} VS. V_{OH}

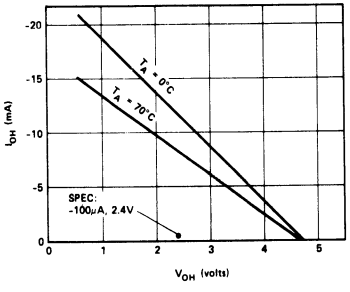


FIGURE 6
TYPICAL I_{OL} VS. V_{OL}

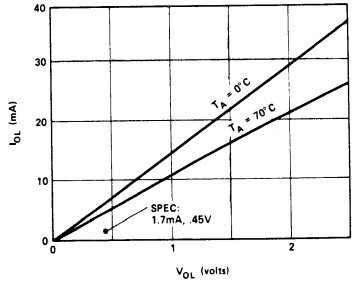


FIGURE 7
TYPICAL REFRESH VS. TEMPERATURE

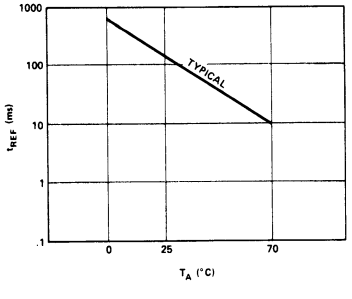


FIGURE 8
TYPICAL ACCESS TIME VS. TEMPERATURE

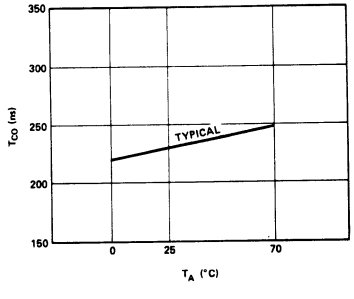


Table 1. I_{DDAV} and I_{CCAV} Characteristics.

Product	I_{DDAV}(Typ)	I_{DDAV}(Max)	I_{CCAV}(Typ)	I_{CCAV}(Max)	Cycle	t_{CEW}
2107A	23mA	34mA	6mA	10mA	700ns	480ns
2107A-1	28mA	38mA	8mA	12mA	550ns	410ns
2107A-4	22mA	33mA	5mA	9mA	840ns	600ns
2107A-5	18mA	28mA	4mA	8mA	970ns	680ns

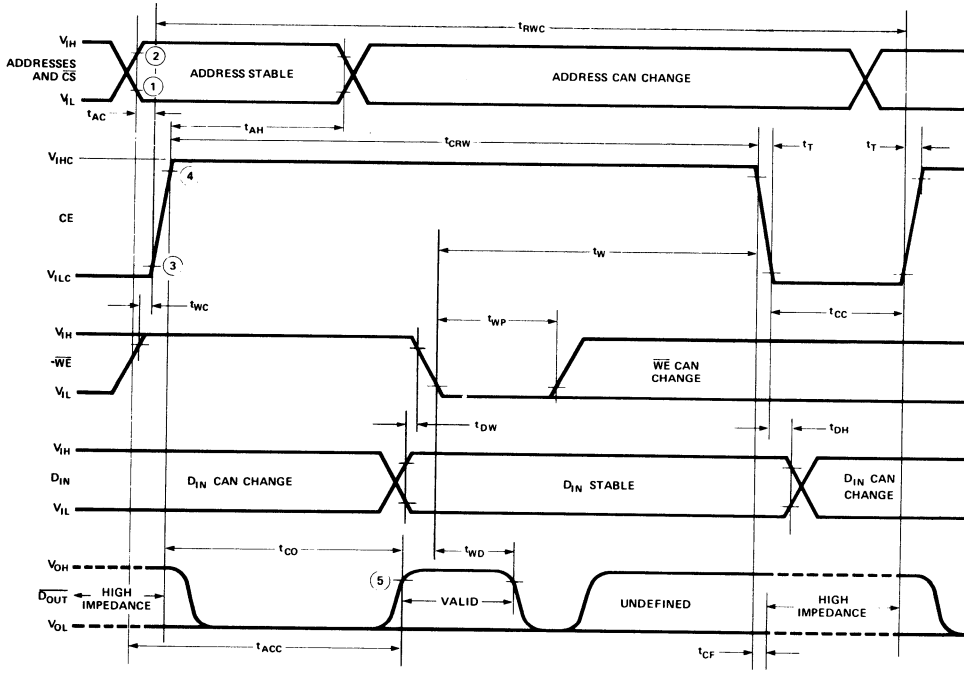
Read Modify Write Cycle

Symbol	Parameters	2107A		2107A-1		2107A-4		2107A-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RWC}[1]	Read Modify Write (RMW) Cycle Time	840		670		970		1140		ns
t_{CRW}[2]	CE Width During RMW	620	3000	530	3000	730	3000	850	3000	ns
t_{WC}	$\overline{WE}$ to CE on	0		0		0		0		ns
t_W	$\overline{WE}$ to CE off	340		250		400		450		ns
t_{WP}	$\overline{WE}$ Pulse Width	150		150		200		200		ns
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		0		ns
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns
t_{CO}	CE to Output Delay		280		260		330		400	ns
t_{ACC}[3]	Access Time		300		280		350		420	ns
t_{WD}	$\overline{D_{OUT}}$ Valid After $\overline{WE}$	0		0		0		0		ns

Notes: 1. t_T = 20ns

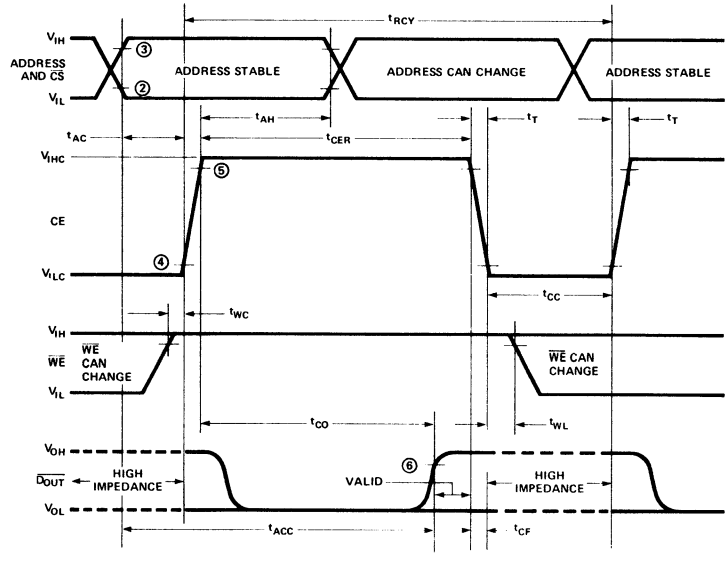
2. $t_{CRW} - t_W = t_{CO}$

3. C_{LOAD} = 50 pf; Load = One TTL Gate; Ref = 2.0V for High, 0.8V for low; $t_{ACC} = t_{AC} + t_{CO}$ + 1 TTL

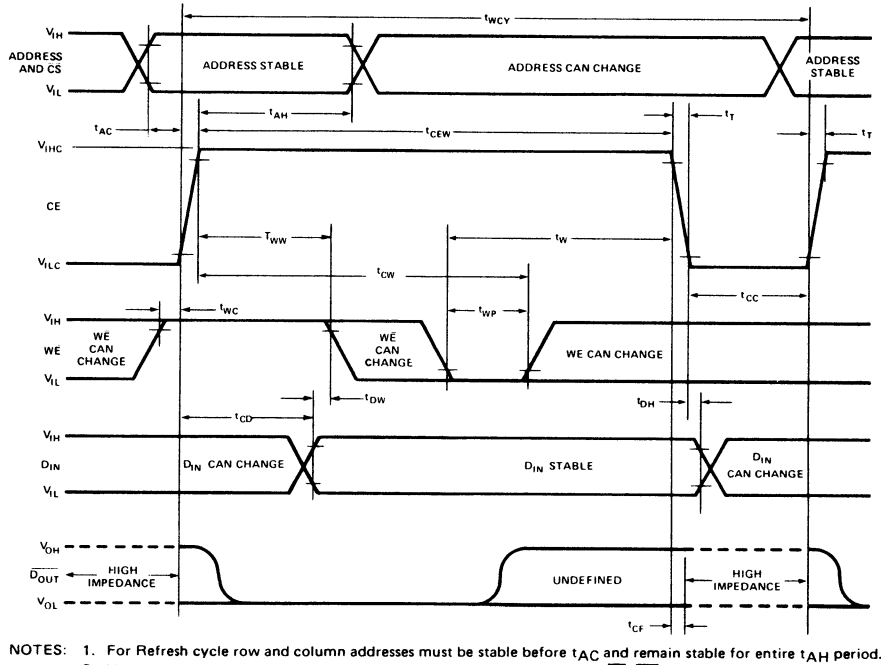


NOTES:
1. V_{SS} + 1.5V is the reference level for measuring timing of the address CS, WE, and D_{IN}.
2. V_{SS} + 3.0V is the reference level for measuring timing of the address, CS, WE, and D_{IN}.
3. V_{SS} + 2.0V is the reference level for measuring timing of CE.
4. V_{DD} -2V is the reference level for measuring timing of CE.
5. V_{SS} + 2.0V is the reference level for measuring the timing of D_{OUT}.

Read and Refresh Cycle [1]



Write Cycle



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{SS} + 1.5V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{SS} + 3.0V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} + 2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} + 2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.

2107B
4096 BIT DYNAMIC RAM

	2107B	2107B-4	2107B-5
Access Time	200ns	270ns	300ns
Read,Write Cycle	400ns	470ns	590ns
RMW Cycle	520ns	590ns	750ns

- **Low Cost Per Bit**
- **Low Standby Power**
- **Easy System Interface**
- **Only One High Voltage Input Signal — Chip Enable**
- **TTL Compatible — All Address, Data, Write Enable, Chip Select Inputs**
- **Refresh Period—2ms for 2107B, 2107B-4, 1ms for 2107B-5 @70°C**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion — Chip Select Input Lead**
- **Fully Decoded — On Chip Address Decode**
- **Output is Three State and TTL Compatible**
- **Industry Standard 22-Pin Configuration**

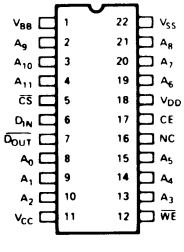
The Intel®2107B is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107B uses dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107B is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107B uses a single transistor cell to achieve high speed and low cost. It is a replacement for the 2107A.

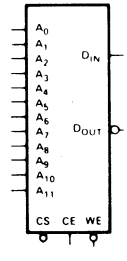
PIN CONFIGURATION

2107B



LOGIC SYMBOL

2107B

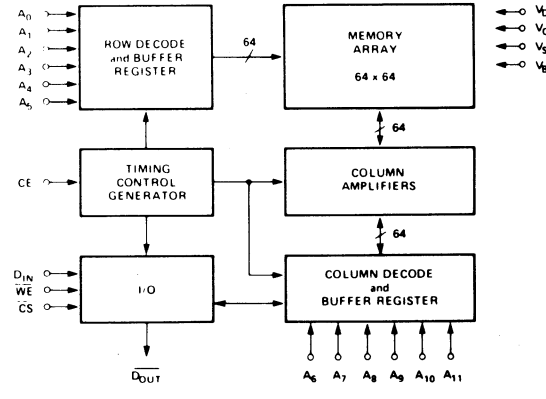


PIN NAMES

A_0-A_{11}	ADDRESS INPUTS*	V_{BB}	POWER (-5V)
CE	CHIP ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	V_{DD}	POWER (+12V)
D_{IN}	DATA INPUT	V_{SS}	GROUND
$\overline{D_{OUT}}$	DATA OUTPUT	$\overline{WE}$	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A_0-A_5.

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . . +25V to −0.3V

Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} . . . . . +20V to −0.3V

Power Dissipation 1.25W

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±10%, V_{BB} [1] = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}[6]	Input Load Current (all inputs except CE)		.01	50	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$ CE = V_{ILC} or V_{IHC}
I_{LC}	Input Load Current		.01	2	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200[5]	μA	CE = -1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on			60	mA	CE = V_{IHC}, $\overline{CS}$ = V_{IL}
$I_{DD\ AV}$	Average V_{DD} Current		38	54	mA	$\overline{CS}$ = V_{IL} ; T_A = 25°C; Min cycle time, Min t_{CE}
I_{CC1}[4]	V_{CC} Supply Current during CE off		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB}	V_{BB} Supply Current		5	400	μA	
V_{IL}	Input Low Voltage	-1.0		0.6	V	t_T = 20ns, V_{ILC} = +1.0V
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	t_T = 20ns
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0mA

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.
5. Maximum I_{DD1} for 2107B-5 is 250 μA.
6. During CE high a current of 0.5mA typical, 1.5mA maximum will be drawn from any address pin which is switched from low to high.

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	2107B		2107B-4		2107B-5		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Time Between Refresh		2		2		1	ms	7
t_{AC}	Address to CE Set Up Time	0		0		10		ns	3
t_{AH}	Address Hold Time	100		100		100		ns	
t_{CC}	CE Off Time	130		130		200		ns	
t_T	CE Transition Time	10	40	10	40	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		0		0		ns	

READ CYCLE

Symbol	Parameter	2107B		2107B-4		2107B-5		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	400		470		590		ns	4
t_{CE}	CE On Time	230	4000	300	4000	350	3000	ns	
t_{CO}	CE Output Delay		180		250		280	ns	5
t_{ACC}	Address to Output Access		200		270		300	ns	6
t_{WL}	CE to $\overline{WE}$	0		0		0		ns	
t_{WC}	$\overline{WE}$ to CE On	0		0		0		ns	

WRITE CYCLE

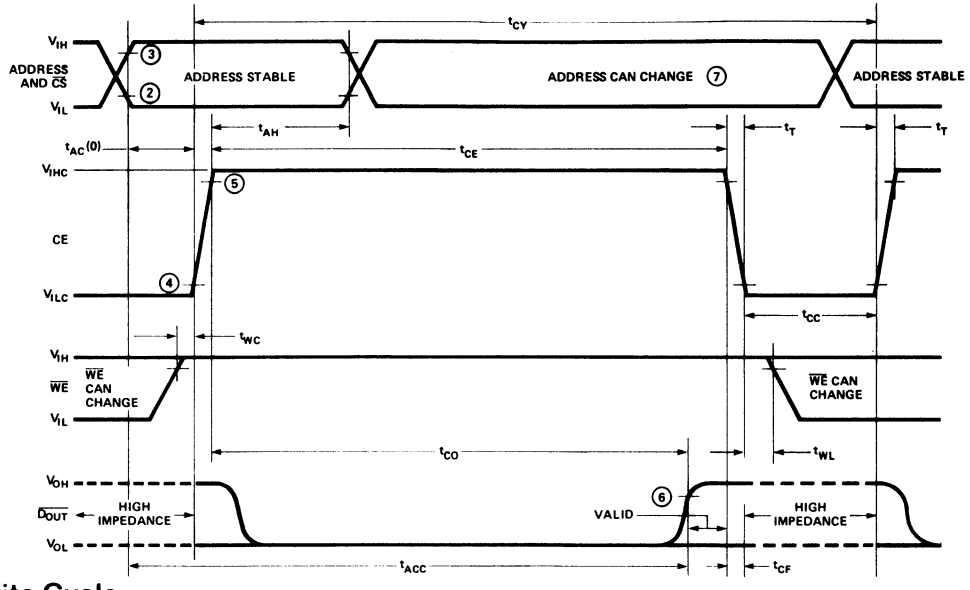
Symbol	Parameter	2107B		2107B-4		2107B-5		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	400		470		590		ns	4
t_{CE}	CE On Time	230	4000	300	4000	350	3000	ns	
t_W	$\overline{WE}$ to CE Off	125		150		200		ns	
t_{CW}	CE to $\overline{WE}$	150		150		150		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		ns	1
t_{DH}	D_{IN} Hold Time	0		0		0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		50		75		ns	
t_{WW}	$\overline{WE}$ Delay	75		75		75		ns	

Capacitance[2] $T_A = 25°C$

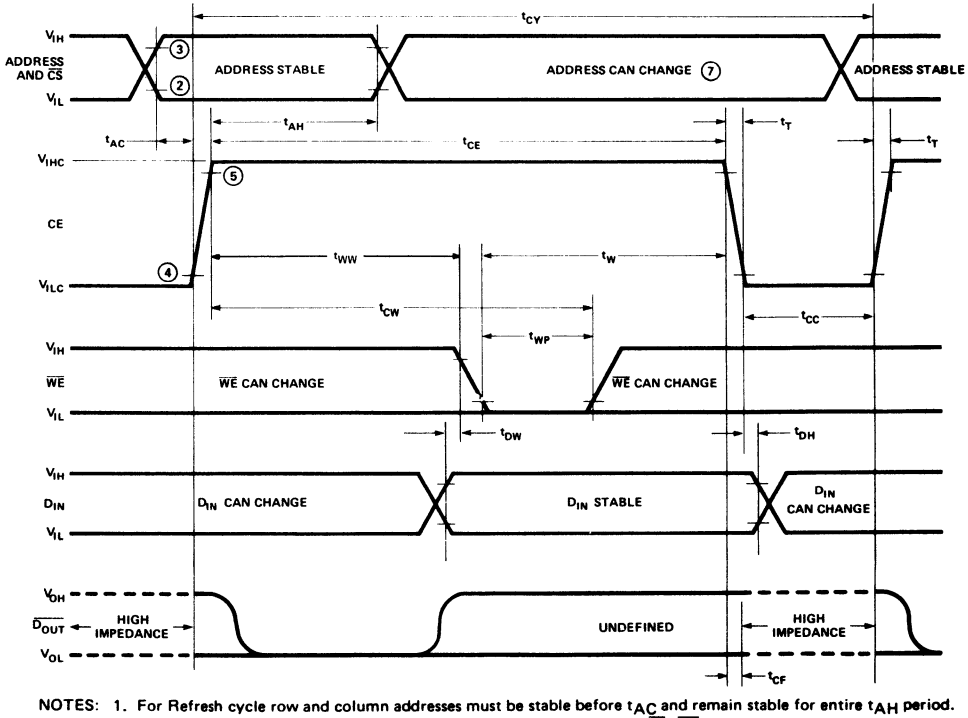
Symbol	Test	Plastic And Ceramic Pkg. Typ.	Max.	Unit	Conditions
C_{AD}	Address Capacitance, $\overline{CS}$	4	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	5	7	pF	$V_{OUT} = 0V$
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	8	10	pF	$V_{IN} = V_{SS}$

Notes:
1. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
2. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation.
   $C = \frac{I\Delta t}{\Delta V}$ with the current equal to a constant 20mA.
3. t_{AC} is measured from end of address transition.
4. $t_T = 20ns$
5. $C_{LOAD} = 50pF$, Load = One TTL Gate, Ref = 2.0V.
6. $t_{ACC} = t_{AC} + t_{CO} + 1t_T$
7. $t_{REF} = 2ms$ at $T_A = 55°$ C for the 2107B-5.

Read and Refresh Cycle [1]



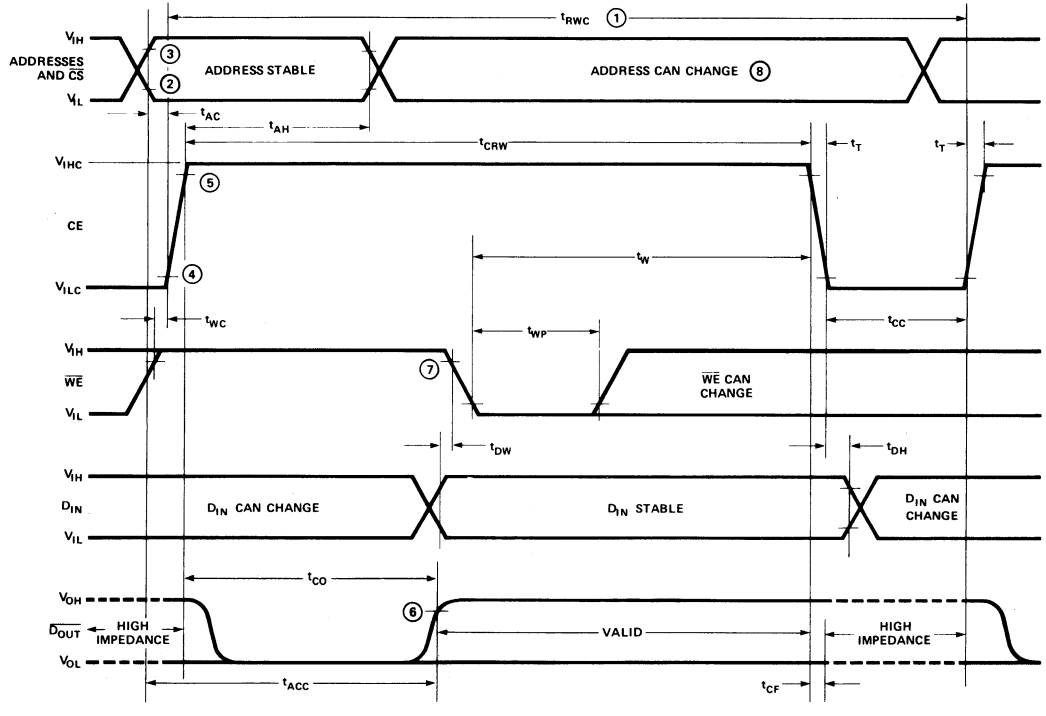
Write Cycle



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Read Modify Write Cycle[1]

Symbol	Parameter	2107B		2107B-4		2107B-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RWC}	Read Modify Write (RMW) Cycle Time	520		590		750		ns
t_{CRW}	CE Width During RMW	350	4000	420	4000	510	3000	ns
t_{WC}	$\overline{WE}$ to CE on	0		0		0		ns
t_W	$\overline{WE}$ to CE off	150		150		200		ns
t_{WP}	$\overline{WE}$ Pulse Width	50		50		100		ns
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		0		0		ns
t_{DH}	D_{IN} Hold Time	0		0		0		ns
t_{CO}	CE to Output Delay		180		250		280	ns
t_{ACC}	Access Time ($t_{ACC} = t_{AC} + t_{CO} + 1t_T$)		200		270		300	ns



NOTES:
1. Minimum cycle timing is based on t_T of 20ns.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$. C_{LOAD} = 50pF. Load = One TTL Gate.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Typical Characteristics

Fig. 1. I_{DD} AV VS. TEMPERATURE

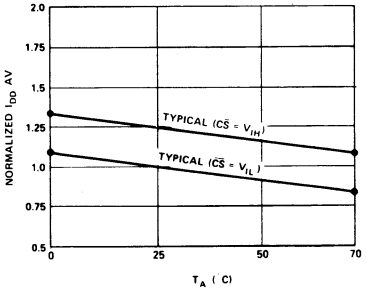


Fig. 2. TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

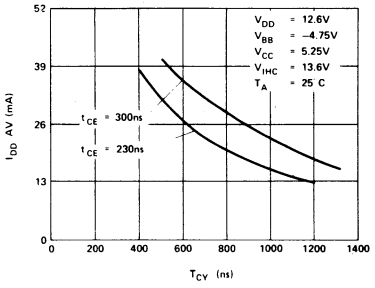


Fig. 3. I_{DD2} VS. TEMPERATURE

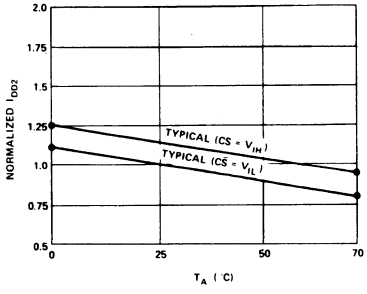
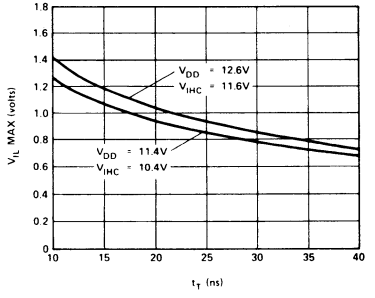
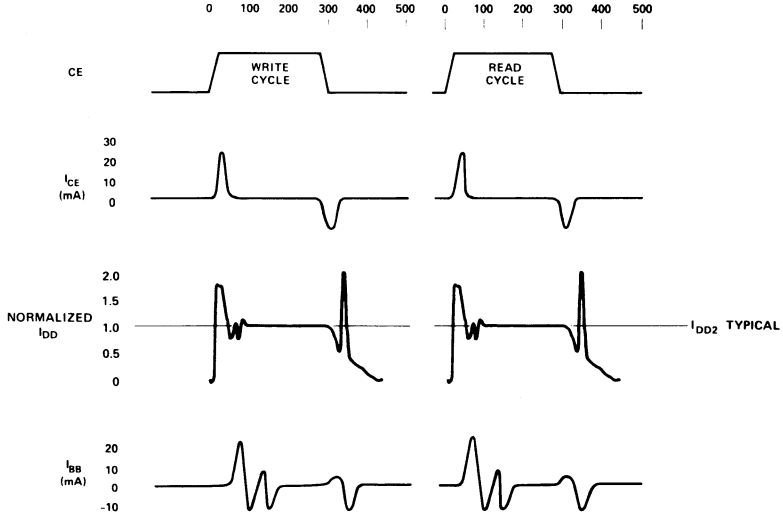


Fig. 4. TYPICAL V_{IL} MAX VS. CE RISE TIME



Typical Current Transients vs. Time



For additional typical characteristics and applications information please refer to Intel Application Note AP-10, "Memory System Design With the Intel 2107B 4K RAM" or Intel's Memory Design Handbook.

2108-2 AND 2108-4
8192 X 1 BIT DYNAMIC RAM

	2108-2	2108-4
	S1572,S1573	S1626,S1627
Max. Access Time (ns)	200	300
Read, Write Cycle (ns)	350	425
Read-Modify-Write Cycle (ns)	400	595

- **8K RAM in Industry Standard 16 Pin Package**
- **Low Standby Power**
- **All Inputs Including Clocks TTL Compatible**
- **Standard Power Supplies +12V, +5V, -5V**
- **Only 64 Refresh Cycles Required Every 2 ms**
- **On-Chip Input Latches**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **Fully Compatible with 4K and 16K Dynamic RAMs**

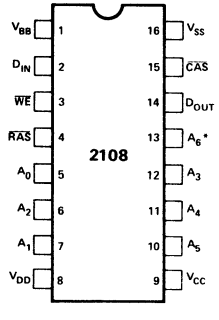
The Intel®2108 is a 8K Dynamic MOS RAM organized as 8192 words by 1 bit. The 2108 employs the same masks and highly reliable, production-proven two layer polysilicon N-MOS technology as the Intel®2116 16K RAM. As shown in the block diagram below, the 2116 is organized as two 8K RAMs on a single silicon die. Each of these 8K RAMs contains its own row decoders, sense amplifiers, and storage cells. The 2108 is fully tested to insure that one 8K RAM meets all AC and DC specifications.

The 2108 is available as either the upper or lower half of the 2116. Address A_6 selects the operating half. For S1572 or S1627, A_6 should be high (V_{IH}) during row address strobe (RAS). For S1573 or S1626, A_6 should be low (V_{IL}) during RAS. The use of the Intel® 3242 Address Multiplexer/Refresh Counter with a 2108 is described on page 2-66. The 2108 is packaged in the industry standard 16-pin DIP which is compatible with widely available automated handling equipment and facilitates easy upgrading from 2104A-type 4K RAM Systems and up to 2116-type 16K RAM Systems.

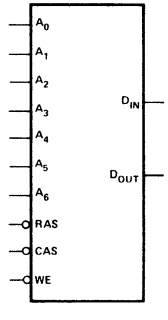
As in the 2104A-type 4K RAM and 2116-type 16K RAM, the 2108 has non-critical clock timing requirements which allow use of addressing multiplexing while maintaining high performance. Three methods of refreshing are permissable; they are described in the applications section of this data sheet.

The 2108 will provide the same reliable operation in its system usage as any Intel product. Information on the details of reliability tests performed on the 2108 and field data on the use of partial devices are available from Intel Corporation.

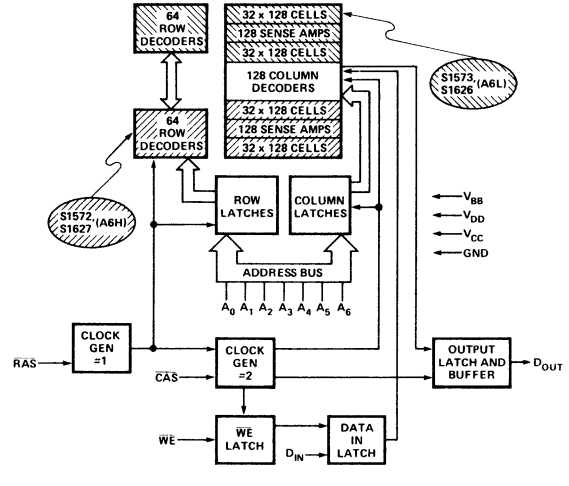
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

*S1572 & S1627: A_6 SHOULD BE AT V_{IH} DURING $\overline{RAS}$
S1573 & S1626: A_6 SHOULD BE AT V_{IL} DURING $\overline{RAS}$

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - V_{BB} ≥ 4V) . . . . . -0.3V to +20V
Power Dissipation 1.25W

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics [1],[2]

T_A = 0°C to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions	
		Min.	Typ.[3]	Max.			
I_{LI}	Input Load Current (any input)			10	µA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$	
$\|I_{LO}\|$	Output Leakage Current for high impedance state		0.1	10	µA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current		1.2	2	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH} or $\overline{CAS}$-only cycle. Chip deselected prior to measurement. See Note 5.	
I_{BB1}	V_{BB} Supply Current		1	50	µA		
I_{DD2}[4]	Operating V_{DD} Current		53	69	mA	2108-2 t_{CYC} = 350 ns	T_A = 25°C Device selected. See Note 6.
			49	65	mA	2108-4 t_{CYC} = 425 ns	
I_{BB2}	Operating V_{BB} Current		120	400	µA	Device selected	
I_{CC1}[7]	V_{CC} Supply Current when deselected			10	µA		
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V		
V_{IH}	Input High Voltage (any input)	2.4		V_{CC}+1	V		
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 4.1 mA (Read Cycle Only)	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA (Read Cycle Only)	

Capacitance [8] T_A = 25°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{I1}	Address, Data In & $\overline{WE}$ Capacitance	4	7	pF	V_{IN} = V_{SS}
C_{I2}	$\overline{RAS}$ Capacitance	3	5	pF	V_{IN} = V_{SS}
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF	V_{IN} = V_{SS}
C_O	Data Output Capacitance	3	7	pF	V_{OUT} = 0V

Notes:
1. All voltages referenced to V_{SS}. No power supply sequencing is required but V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}.
2. To avoid self-clocking, $\overline{RAS}$ should not be allowed to float.
3. Typical values are for T_A = 25°C and nominal power supply voltages.
4. For $\overline{RAS}$-only refresh I_{DD} = 0.78 I_{DD2}. For $\overline{CAS}$-before-$\overline{RAS}$ (64 cycle refresh) I_{DD} = 0.96 I_{DD2}.
5. The chip is deselected (i.e., output is brought to high impedance state) by $\overline{CAS}$-only cycle or by $\overline{CAS}$-before-$\overline{RAS}$ cycle. The current flowing in a selected (i.e., output on) chip with $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} is approximately twice I_{DD1}.
6. See Page 2-62 for typical I_{DD} characteristics under other conditions.
7. When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
8. Capacitance measured with Boonton Meter.

TYPICAL CHARACTERISTICS

I_{BB2} AND I_{DD2} VS. TEMPERATURE

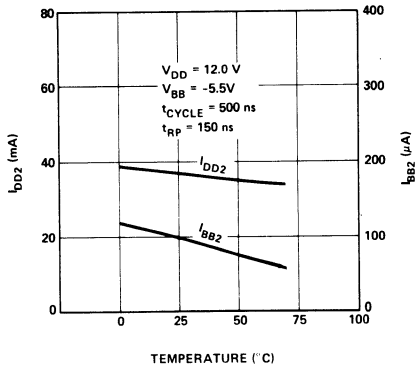


Figure 1.

I_{DD2} VS. CYCLE TIME

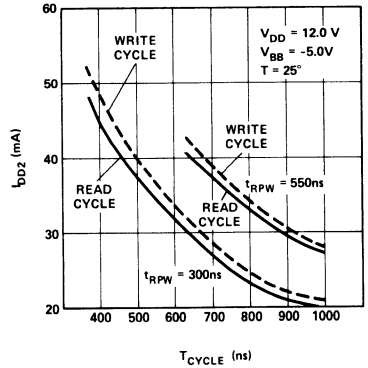


Figure 2.

Standby Power Calculations:

$$P_{REF} = P_{OP}\left(N\frac{t_{CYC}}{t_{REF}}\right) + P_{SB}\left(1 - N\frac{t_{CYC}}{t_{REF}}\right) \text{ where}$$

P_{OP} = Power dissipation — continuous operation = $V_{DD} \times I_{DD2}$.

N = Number of refresh cycles (64).

t_{CYC} = Cycle time for a refresh cycle.

t_{REF} = Time between refreshes

P_{SB} = Standby power dissipation = $V_{DD} \times I_{DD1} + |V_{BB}| \times I_{BB}$

Note that I_{DD2} depends upon refresh as follows:

1. For ($\overline{RAS}$ before $\overline{CAS}$) use I_{DD2} from Figures 1 and 2.
2. For ($\overline{CAS}$ before $\overline{RAS}$) multiply I_{DD2} determined in (1) by 0.96.
3. For ($\overline{RAS}$ only) multiply I_{DD2} determined in (1) by 0.78.

Examples of typical calculations for V_{BB} = -5.0V, V_{DD} = 12.0V, T_A = 25°C, t_{CYC} = 0.425 μs, t_{RAS} = 0.3 μs. t_{REF} = 2000 μs:

1. 128 cycle ($\overline{RAS}$ before $\overline{CAS}$): P_{OP} = 12.0V x 43 mA = 516 mW

$$P_{REF} = 516\left(128\frac{0.425}{2000}\right) + (12x1.2+5x0.001)\left(1-128\frac{0.425}{2000}\right)$$

P_{REF} = 28.0 mW

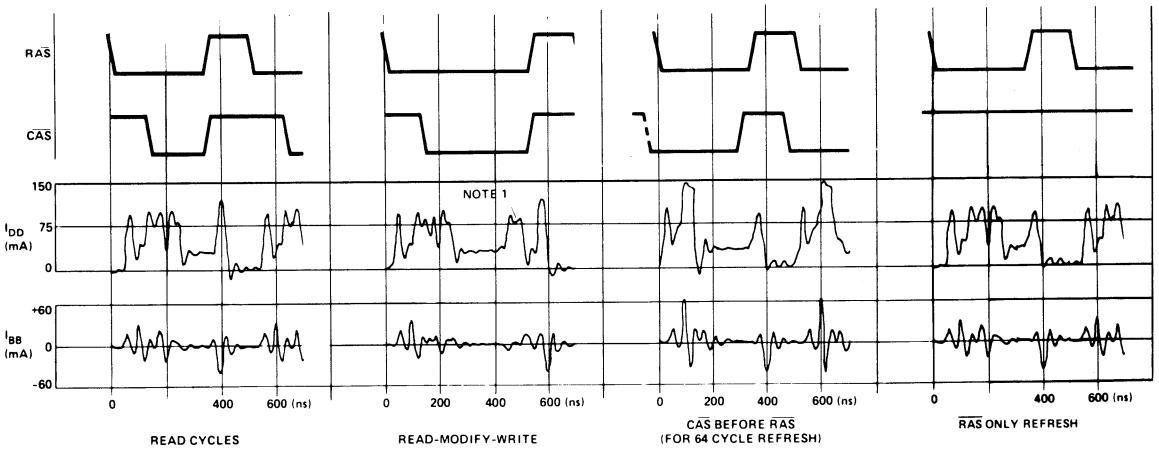
2. 64 cycle ($\overline{CAS}$ before $\overline{RAS}$); P_{OP} = 12.0V x 43 (0.96) mA = 495 mW.

$$P_{REF} = 495\left(64\frac{0.425}{2000}\right) + (12x1.2+5x0.001)\left(1-64\frac{0.425}{2000}\right) =$$

P_{REF} = 20.9 mW

3. 128 cycle ($\overline{RAS}$ only): P_{OP} = 12.0V x 43 (0.78) mA = 402 mW

P_{REF} = 25.0 mW



Note 1: Increase in current due to $\overline{WE}$ going low. Width of this current pulse is independent of $\overline{WE}$ pulse width.

Figure 3. Supply Current Waveforms.

A.C. Characteristics[1]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{REF}	Time Between Refresh		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	75		95		ns
t_{CP}	$\overline{CAS}$ Precharge Time	100		125		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	45	75	60	110	ns
t_{CRP}[3]	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	160		220		ns
t_{CSH}	$\overline{CAS}$ Hold Time	200		300		ns
t_{ASR}	Row Address Set-Up Time	0		0		ns
t_{ASC}	Column Address Set-Up Time	-10		-10		ns
t_{AH}	Address Hold Time	45		60		ns
t_T	Transition Time (Rise and Fall)		50		50	ns
t_{OFF}	Output Buffer Turn Off Delay	0	60	0	80	ns
t_{CAC}[4]	Access Time From $\overline{CAS}$		125		190	ns
t_{RAC}[4]	Access Time From $\overline{RAS}$		200		300	ns

READ AND REFRESH CYCLES

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{CYC}[5]	Random Read Cycle Time	350		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	3000	190	3000	ns
t_{CH}	$\overline{CAS}$ Hold Time for $\overline{RAS}$-Only Refresh	30		30		ns
t_{CPR}	$\overline{CAS}$ Precharge for 64 Cycle Refresh	30		30		ns
t_{RCH}	Read Command Hold Time	20		20		ns
t_{RCS}	Read Command Set-Up Time	0		0		ns
t_{DOH}	Data-Out Hold Time	32		32		μs

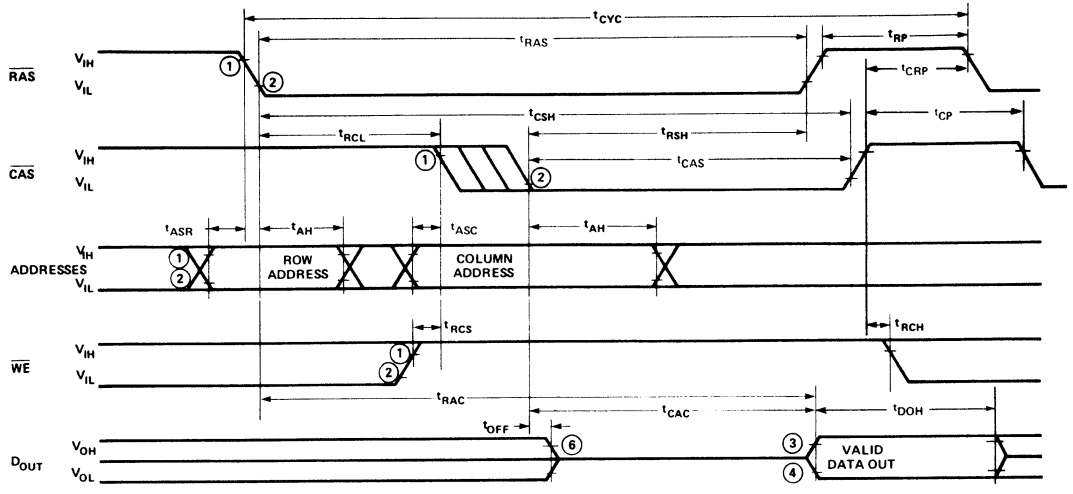
WRITE CYCLE

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{CYC}[5]	Random Write Cycle Time	350		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	10000	190	10000	ns
t_{WCH}	Write Command Hold Time	75		100		ns
t_{WP}	Write Command Pulse Width	50		100		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		160		ns
t_{DS}[6]	Data-In Set-Up Time	0		0		ns
t_{DH}[6]	Data-In Hold Time	100		125		ns

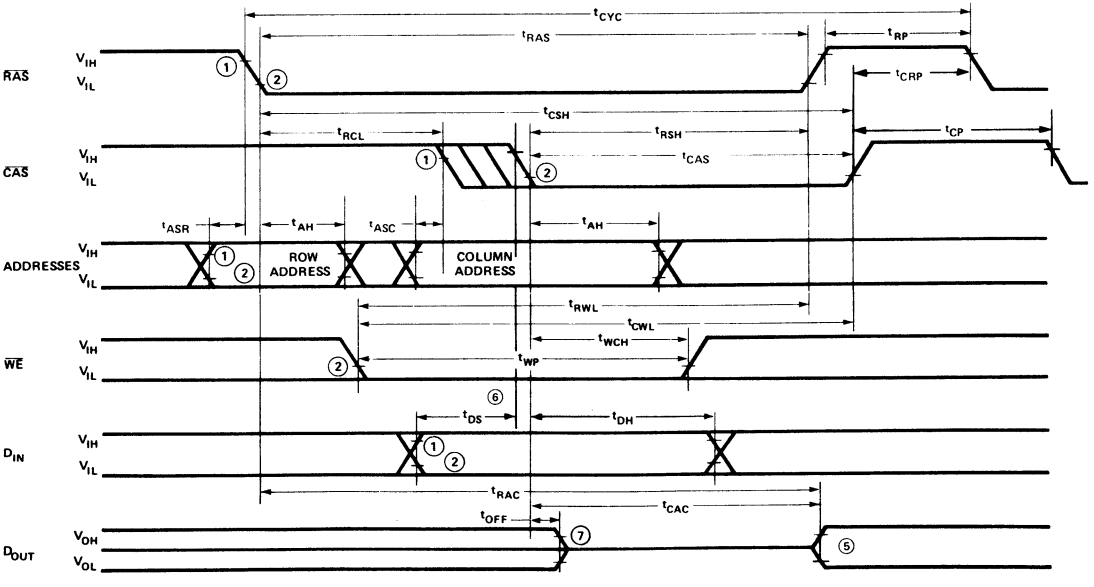
Notes: 1. All voltages referenced to V_{SS}.
2. $\overline{CAS}$ must remain at V_{IH} a minimum of $t_{RCL\ MIN}$ after $\overline{RAS}$ switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before t_{RCL} (MAX) = t_{RAC} -t_{CAC}. Device operation is not guaranteed for t_{RCL}>2 μs.
3. The t_{CRP} specification is less restrictive than the t_{CRL} range which was specified in the 2108 preliminary data sheet.
4. Load = 1 TTL and 50 pF.
5. The minimum cycle timing does not allow for t_T or skews.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

Waveforms

READ CYCLE



WRITE CYCLE



Notes:
1,2. V_{IH} MIN and V_{IL} MAX are reference levels for measuring timing of input signals.
3,4. V_{OH} MIN and V_{OL} MAX are reference levels for measuring timing of D_{OUT}.
5. D_{OUT} follows D_{IN} when writing, with $\overline{WE}$ before $\overline{CAS}$.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

A.C. Characteristics

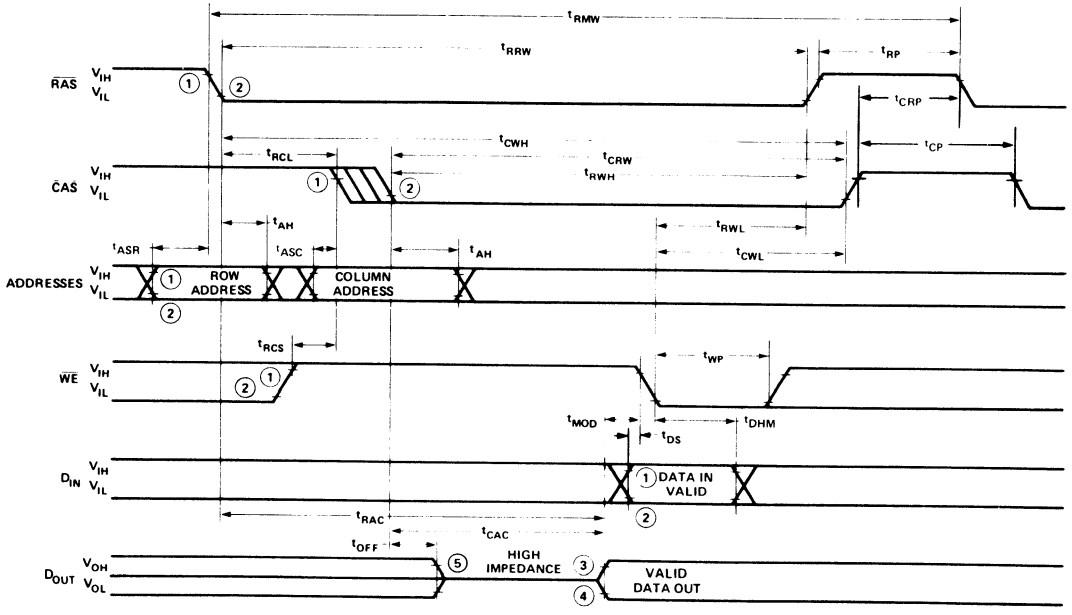
T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%, V_{SS} = 0V, unless otherwise noted.

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{RMW}	Read-Modify-Write Cycle Time	400		595		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	225	3000	350	3000	ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	325	32000	500	32000	ns
t_{RWH}	RMW Cycle $\overline{RAS}$ Hold Time	250		390		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	300		460		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		160		ns
t_{WP}	Write Command Pulse Width	50		100		ns
t_{RCS}	Read Command Set-Up Time	0		0		ns
t_{MOD}	Modify Time	0	10	0	10	μs
t_{DS}	Data-In Set-Up Time	0		0		ns
t_{DHM}	Data-In Hold Time (RMW Cycle)	50		125		ns

Waveforms

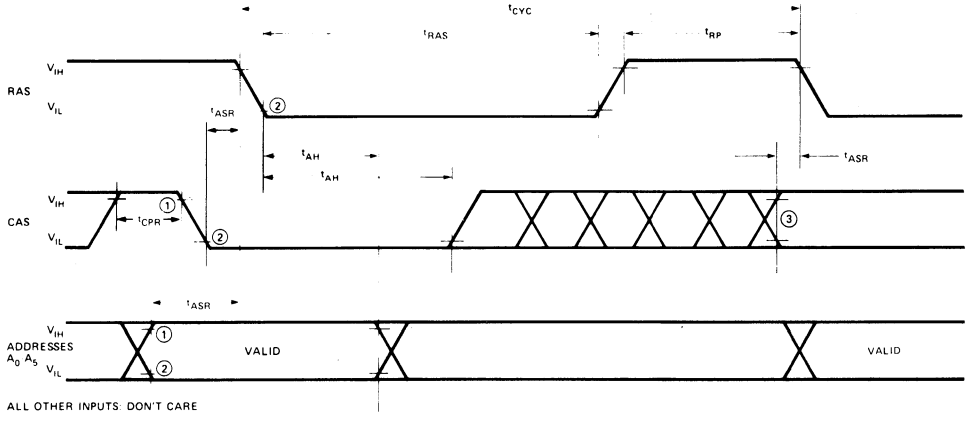
READ MODIFY WRITE CYCLE



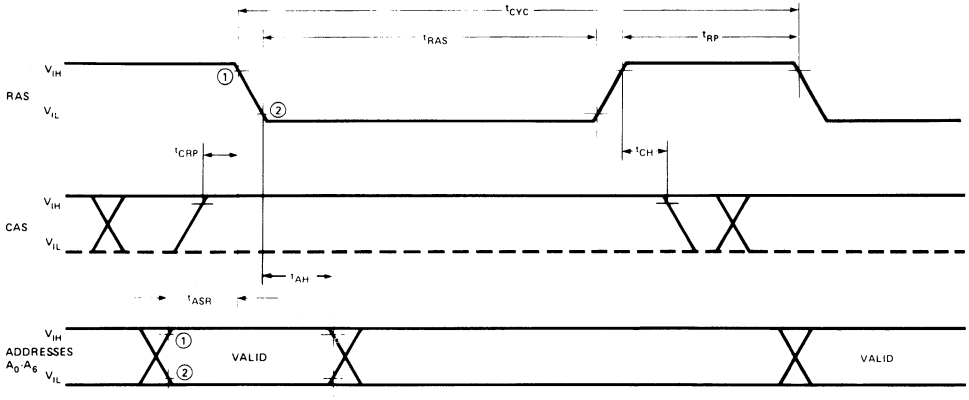
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

Refresh Cycle Waveforms

$\overline{CAS}$ BEFORE $\overline{RAS}$ CYCLES. (64 CYCLE REFRESH)



$\overline{RAS}$ ONLY CYCLES (128 CYCLE REFRESH)



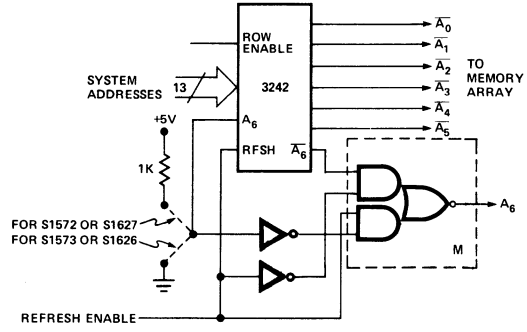
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3. $\overline{CAS}$ must be high or low as appropriate for the next cycle.

Applications Information

The 2108 may be refreshed in any of three modes: read cycles with $\overline{RAS}$ before $\overline{CAS}$ timing as shown on page 5, $\overline{RAS}$ only cycles (page 7), or $\overline{CAS}$ before $\overline{RAS}$ cycles (page 7). In all three modes A_6 must be held high for the S1572 and S1627 or low for the S1573 and S1626. The row addressed by A_0 through A_5 is refreshed. Therefore, 64 cycles are required to refresh the stored data.

The $\overline{CAS}$-before-$\overline{RAS}$ mode is useful in the 2116 as a technique for increasing memory availability and minimizing standby power dissipation by requiring only 64 refresh cycles every 2 ms. Systems employing the 2108 in a $\overline{CAS}$-before-$\overline{RAS}$ refresh mode can be easily upgraded to the most efficient 16K RAM capability.

Since the 2108 input pin A_6 supplies two system addresses (A_6 and A_{13}) to the internal memory array, it is not possible to simply tie this input high or low. The 2108 input A_6 must be tied to the appropriate level only during row address strobe ($\overline{RAS}$) and then used to supply the high order system address A_{13} during column address strobe ($\overline{CAS}$). Control of A_6 in a system may be implemented. as shown at right. In this circuit the output A_6 of multiplexer M supplies the appropriate high or low level (determined by S1572, S1627, S1573, or S1626) during $\overline{RAS}$ for both a memory cycle and refresh cycle. During $\overline{CAS}$, system address A_{13} is multiplexed on A_6 as shown. See the 2116 section for additional applications information.



Power Supply Decoupling/ Distribution

Power supply current waveforms for the 2108 are shown in Figure 3. The V_{DD} supply provides virtually all of the operating current for the 2108. The V_{DD} supply current, I_{DD}, has two components: transient current peaks when the clocks change state and a DC component while the clocks are active (low). When selecting the decoupling capacitors for the V_{DD} supply, the characteristics of capacitors as well as the current waveform must be considered. Suppression of transient or pulse currents require capacitors with small physical size and low inherent inductance. Monolithic and other ceramic capacitors exhibit these desirable characteristics. When the current waveform indicates a DC component, bulk capacity must be located near the current load to supply the load power. Inductive effects of PC board traces and bus bars preclude supplying the DC component from bulk capacitors at the periphery of a memory matrix without voltage droop during the active portion of a memory cycle. This means that some bulk capacity in the form of electrolytic or large ceramic capacitors should be distributed around or within the memory matrix.

The V_{BB} supply current, I_{BB}, has high transient current peaks, with essentially no DC component (less than 400 microamperes). The V_{BB} capacitors should be selected for transient suppression characteristics. The following capacitance values and locations are recommended for the 2108:

1. A 0.33 μF ceramic capacitor between V_{DD} and V_{SS} (ground) at every other device.
2. A 0.1 μF ceramic capacitor between V_{BB} and V_{SS} at every other device (preferably alternate devices to the V_{DD} decoupling above).
3. A 4.7 μF electrolytic capacitor between V_{DD} and V_{SS} for each eight devices and located adjacent to the devices.

The V_{CC} supply is connected only to the 2108 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is usually only the input high level current to a TTL gate and the output leakage currents of any OR-tied 2108 (typically 100 μA or less total). Intel recommends that a 0.1 or 0.01 μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight devices to preclude coupled noise from affecting the TTL devices in the system.

Intel recommends a power supply distribution system such that each power supply is grided both horizontally and vertically at each memory device. This technique minimizes the power distribution system impedance and enhances the effect of the decoupling capacitors.

Output Data Latch

The 2108 contains an output data latch eliminating the need for an external system data latch and the timing circuitry required to strobe an external latch. The output latch operates identically to the 16-pin 4K RAM (Intel 2104) output latch enhancing the system compatibility of the 16K and 4K devices.

Operation of the output latch is controlled by $\overline{CAS}$. The data output will go to the high-impedance state immediately following the $\overline{CAS}$ leading edge during each data cycle and will either go to valid data at access time on selected devices (devices receiving both $\overline{RAS}$ and $\overline{CAS}$) or will remain in the high impedance state on unselected devices (devices receiving only $\overline{CAS}$). During $\overline{RAS}$-only refresh cycles, the data output remains in the state it was prior to the $\overline{RAS}$-only cycle. This unique feature of latched output RAMs allows a refresh cycle to be hidden among data cycles without impacting data availability. For instance, a $\overline{RAS}$-only refresh cycle could follow each data cycle in a microprocessor system but the accessed data would remain at the device output and the microprocessor could take the data at any time within the cycle. Non-latched output devices do not provide this type of hidden refresh capability since their data output would go to the high impedance state at the end of the data cycle.

Page Mode Operation

The 2108 is designed for page mode operation and is presently being characterized for that mode. Specifications will be available at a later date.

2111A
256 x 4 STATIC RAM

2111A-2	250 ns Max.
2111A	350 ns Max.
2111A-4	450 ns Max.

- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 18 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150 mW**
- **Three-State Output: OR-Tie Capability**

The Intel® 2111A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

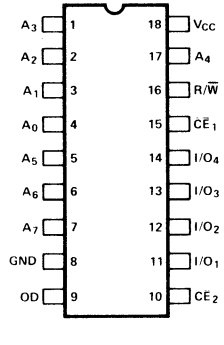
The 2111A is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

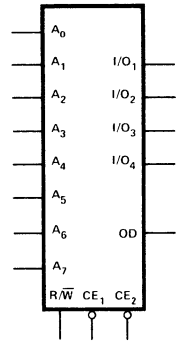
The Intel® 2111A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



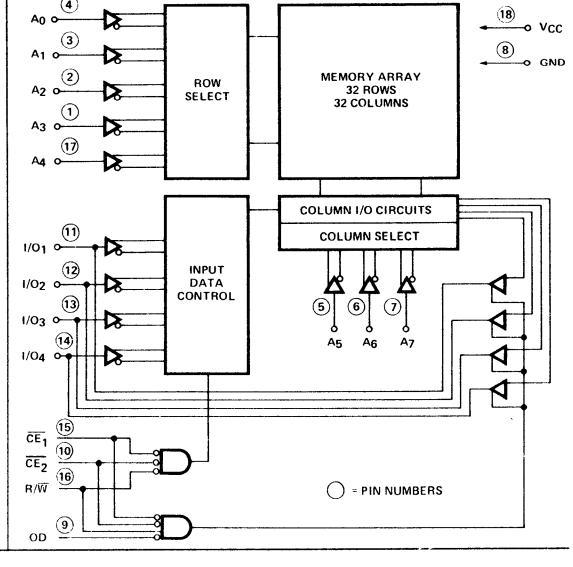
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
$R/\overline{W}$	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
$\overline{CE}_2$	CHIP ENABLE 2
I/O_1-I/O_4	DATA INPUT/OUTPUT

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

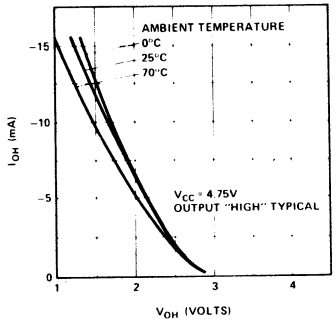
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

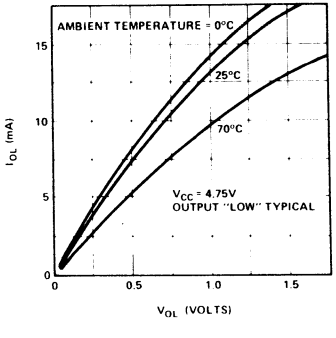
T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current		1	10	µA	Output Disabled, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current		-1	-10	µA	Output Disabled, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current 2111A, 2111A-4		35	55	mA	V_{IN} = 5.25V
	Power Supply Current 2111A-2		45	65		$I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current 2111A, 2111A-4			60	mA	V_{IN} = 5.25V
	Power Supply Current 2111A-2			70		$I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage 2111A, 2111A-2	2.4			V	I_{OH} = -200µA
	Output High Voltage 2111A-4	2.4			V	I_{OH} = -150µA

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2111A-2 (250 ns ACCESS TIME)

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			250	ns	
t_{CO}	Chip Enable To Output			180	ns	
t_{OD}	Output Disable To Output			130	ns	
t_{DF} [3]	Data Output to High Z State	0		180	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

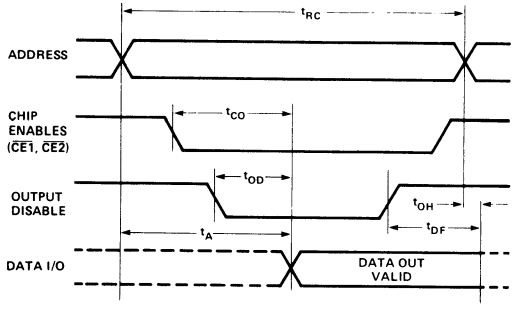
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	150			ns	
t_{DW}	Data Setup	150			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	150			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

CAPACITANCE[2] T_A = 25°C, f = 1MHz

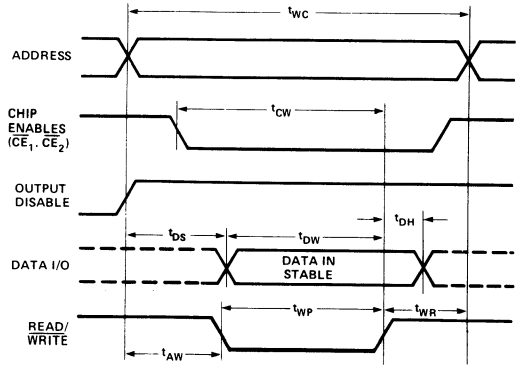
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.

2111A (350 ns ACCESS TIME)

A.C. CHARACTERISTICS

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			350	ns	
t_{CO}	Chip Enable To Output			240	ns	
t_{OD}	Output Disable To Output			180	ns	
t_{DF} [2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	220			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	200			ns	
t_{DW}	Data Setup	200			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	200			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

2111A-4 (450 ns ACCESS TIME)

A.C. CHARACTERISTICS

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.

2112A
256 X 4 BIT STATIC RAM

2112A-2	250 ns Max.
2112A	350 ns Max.
2112A-4	450 ns Max.

- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150 mW**
- **Three-State Output: OR-Tie Capability**

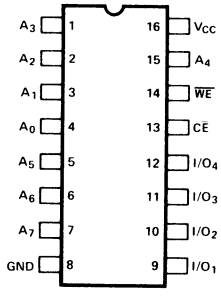
The Intel® 2112A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2112A is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

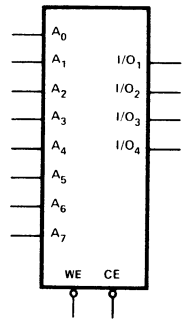
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2112A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



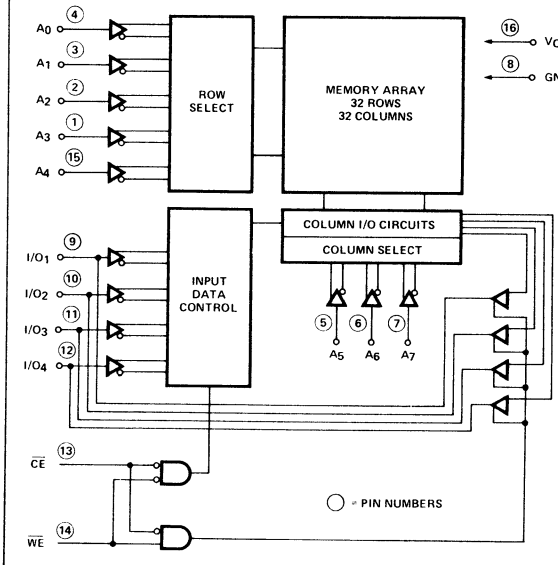
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

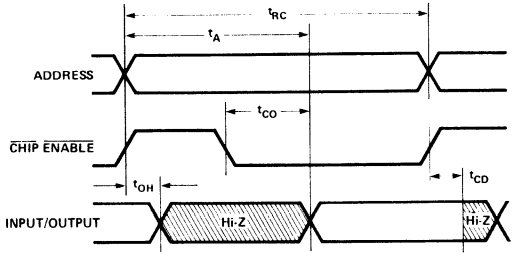
Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			1	10	µA	Output Disabled, $V_{I/O}$=4.0V
I_{LOL}	I/O Leakage Current			-1	-10	µA	Output Disabled, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current	2112A, 2112A-4		35	55	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
		2112A-2		45	65		
I_{CC2}	Power Supply Current	2112A, 2112A-4			60	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
		2112A-2			70		
V_{IL}	Input "Low" Voltage		-0.5		0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2112A, 2112A-2	2.4			V	I_{OH} = -200µA
		2112A-4	2.4			V	I_{OH} = -150µA

A.C. CHARACTERISTICS FOR 2112A-2

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	t_r, t_f = 20ns
t_A	Access Time			250	ns	
t_{CO}	Chip Enable To Output Time			180	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		120	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

READ CYCLE WAVEFORMS



CAPACITANCE[2] T_A = 25°C, f = 1 MHz

Symbol	Test	Limits (pF) Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS FOR 2112A-2 (Continued)

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

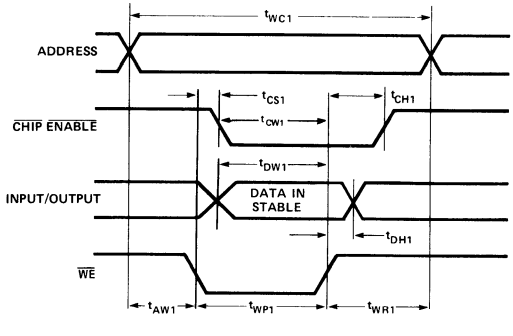
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	200			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	180			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	180			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable To Write Setup Time	180			ns	

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

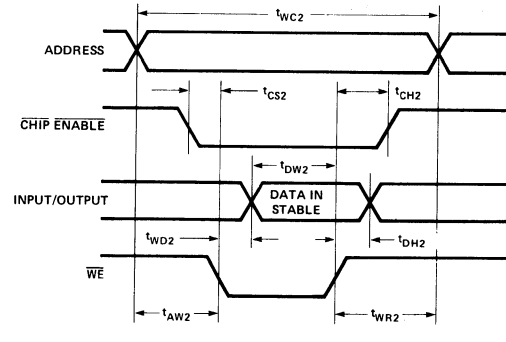
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	320			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	180			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	120			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

WRITE CYCLE WAVEFORMS

WRITE CYCLE #1



WRITE CYCLE #2



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2112A

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns
t_A	Access Time			350	ns	Input Levels = 0.8V or 2.0V
t_{CO}	Chip Enable To Output Time			240	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		200	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	270			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	250			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	250			ns	

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	470			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	200			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2112A-4

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns
t_A	Access Time			450	ns	Input Levels = 0.8V or 2.0V
t_{CO}	Chip Enable To Output Time			310	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		260	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	320			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	300			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	300			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	300			ns	

WRITE CYCLE #2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	580			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	300			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	260			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

RAM

2114
1024 X 4 BIT STATIC RAM

	2114-2	2114-3	2114	2114L3	2114L
Max. Access Time (ns)	200	300	450	300	450
Max. Power Dissipation (mw)	710mw	710mw	710mw	370mw	370mw

- **High Density 18 Pin Package**
- **Identical Cycle and Access Times**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **Pin-Out Compatible with 3605 and 3625 Bipolar PROMs**

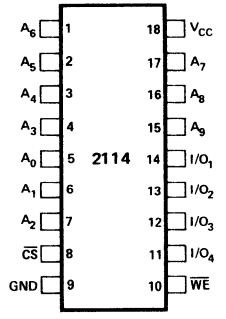
The Intel® 2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The 2114 is placed in an 18-pin package for the highest possible density.

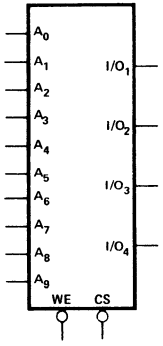
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

The 2114 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

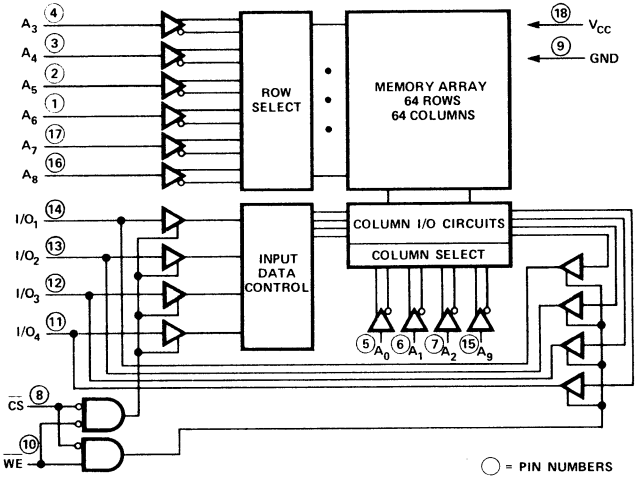
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . -0.5V to +7V
Power Dissipation 1.0W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.

SYMBOL	PARAMETER	2114-2, 2114-3, 2114 Min.	Typ.	Max.	2114L3, 2114L Min.	Typ.	Max.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10			10	μA	V_{IN} = 0 to 5.25V
$\|I_{LO}\|$	I/O Leakage Current			10			10	μA	$\overline{CS}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		80	120			65	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current		90	135			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	2.4		V_{CC}	V	I_{OH} = -1.0 mA

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = OV
C_{IN}	Input Capacitance	5	pF	V_{IN} = OV

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2114-2 Min.	2114-2 Max.	2114-3, 2114L3 Min.	2114-3, 2114L3 Max.	2114, 2114L Min.	2114, 2114L Max.	UNIT
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{CO}	Chip Selection to Output Valid		70		100		100	ns
t_{CX}	Chip Selection to Output Active	0		0		0		ns
t_{OTD}	Output 3-state from Deselection	0	40	0	80	0	100	ns
t_{OHA}	Output Hold from Address Change	10		10		10		ns

WRITE CYCLE [2]

SYMBOL	PARAMETER	2114-2 Min.	2114-2 Max.	2114-3, 2114L3 Min.	2114-3, 2114L3 Max.	2114, 2114L Min.	2114, 2114L Max.	UNIT
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	100		150		200		ns
t_{WR}	Write Release Time	20		0		0		ns
t_{OTW}	Output 3-state from Write	0	40	0	80	0	100	ns
t_{DW}	Data to Write Time Overlap	100		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

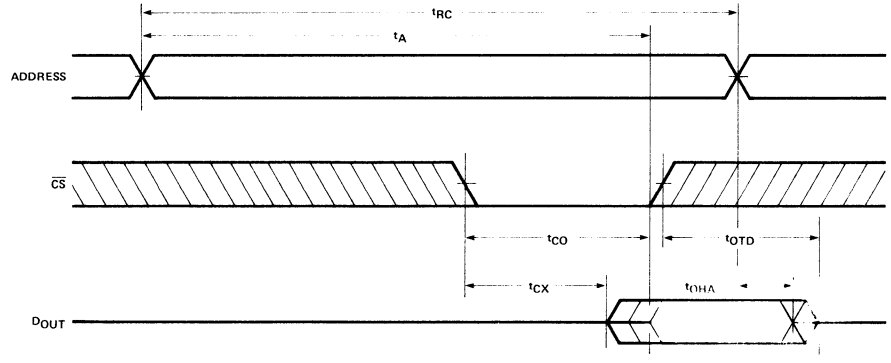
NOTES: 1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

A.C. CONDITIONS OF TEST

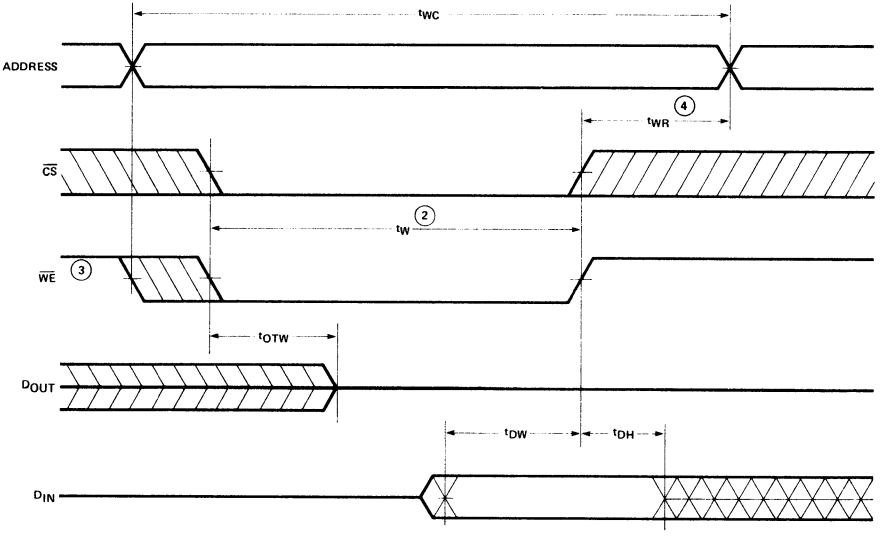
Input Pulse Levels . . . . . 0.8 Volt to 2.4 Volt
Input Rise and Fall Times . . . . . 10 nsec
Input and Output Timing Levels . . . . . 1.5 Volts
Output Load . . . . . 1 TTL Gate and C_L = 50 pF

WAVEFORMS

READ CYCLE ①



WRITE CYCLE



NOTES:
① $\overline{WE}$ is high for a Read Cycle.
② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to $\overline{WE}$ going high.
③ $\overline{WE}$ must be high during all address transitions.
④ t_{WR} is referenced to the high transition of $\overline{WE}$.

DATA STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the address, Chip Select, or data I/O voltage levels and timing transitions. The block diagram also shows data storage cannot be affected by $\overline{WE}$, the addresses, nor the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ by itself — or in conjunction with the other — can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during a Write time — defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{WR}.

Internal delays on the 2114 are established such that address decoding propagates ahead of data inputs (keyed by the Write time). Therefore, it is permissable to establish the addresses coincident to the selection of a Write time, but no later. If the Write time precedes the addresses, the data in the previously addressed locations, or some other location, may be inadvertently changed.

While it is important that the addresses remain stable for the entire Write cycle, the data inputs are not required to remain stable. Appropriate voltage levels will be written into the cells as long as the data is stable for t_{DW} at the end of the Write time.

1024 X 1 HIGH SPEED STATIC RAM

	2115-2, 2125-2	2115, 2125	2115L, 2125L
Typ. T_{AA} (ns)	55	75	75
Typ. I_{CC} (mA)	80	75	50

- **Fully Pin Compatible to 93415 (2115) and 93425 (2125)**
- **Low Operating Power Dissipation: Typical 0.2mW/bit (2115L, 2125L)**
- **TTL Inputs and Output**
- **Single +5V Supply**
- **Uncommitted Collector* (2115) and Three-State (2125) Output**
- **Non-Inverting Data Output**
- **Standard 16 Pin Dual In-Line Package**

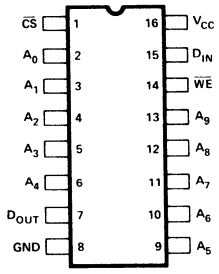
The Intel® 2115 and 2125 family are fully static read/write random access memories organized as 1024 words by 1 bit. These RAMs are designed for buffer control storage and high performance main memory applications. They are compatible with TTL logic families in all respects: inputs, output, and a single +5V supply. Both uncommitted collector* and three-state output are available.

The 2115 and 2125 family offers high performance, low power dissipation, and system cost savings. Fast system speed is achieved by using the 2115-2 and 2125-2. The 2115L and 2125L gives low system power dissipation, only 0.2mW/bit typical. The 2115 and 2125 are ideal for slower performance systems where cost is a prime factor.

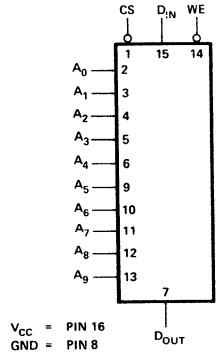
The 2115 and 2125 family is fabricated with N-channel MOS silicon gate technology. This technology allows the design and production of high speed MOS RAMs which are compatible to the performance of bipolar RAMs, but offering the advantage of lower power dissipation and cost.

*The 2115 is a MOS device and the output is actually an uncommitted drain.

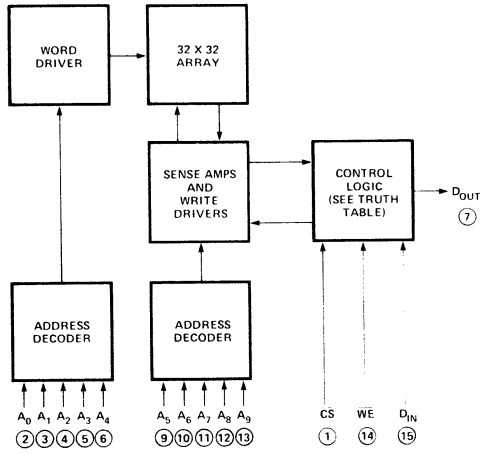
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

TRUTH TABLE

INPUTS			OUTPUT 2115 FAMILY	OUTPUT 2125 FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	HIGH Z	NOT SELECTED
L	L	L	H	HIGH Z	WRITE "0"
L	L	H	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
All Output or Supply Voltages . . . . . -0.5 to +7 Volts
All Input Voltages . . . . . -0.5 to +5.5 Volts
D.C. Output Current 20mA

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics [1] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
V_{OL1}	2115-2 Output Low Voltage			0.45	V	I_{OL} = 16mA
V_{OL2}	2115, 2115L Output Low Voltage			0.45	V	I_{OL} = 12mA
V_{OL3}	2125 Family Output Low Voltage			0.45	V	I_{OL} = 7mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		-1	-40	μA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input High Current		1	40	μA	V_{CC} = Max., V_{IN} = 4.5V
I_{CEX}	2115 Family Output Leakage Current		10	100	μA	V_{CC} = Max., V_{OUT} = 4.5V
$\|I_{OFF}\|$	2125 Family Output Current (High Z)		10	50	μA	V_{CC} =Max., V_{OUT} = 0.5V/2.4V
I_{OS} [2]	2125 Family Current Short Circuit to Ground			-100	mA	V_{CC} = 4.5V
V_{OH}	2125 Family Output High Voltage	2.4			V	I_{OH} = -3.2mA
I_{CCL}	2115L, 2125L Power Supply Current		50	65	mA	All Inputs Grounded, Output Open
I_{CC1}	2115, 2125, Power Supply Current		75	100	mA	All Inputs Grounded, Output Open
I_{CC2}	2115-2, 2125-2 Power Supply Current		80	125	mA	All Inputs Grounded, Output Open

Notes:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (@ 400 f_{PM} air flow) = 45°C/W
   θ_{JA} (still air) = 60°C/W
   θ_{JC} = 25°C/W.
2. Duration of short circuit current should not exceed 1 second.

2115 Family A.C. Characteristics[1] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

READ CYCLE

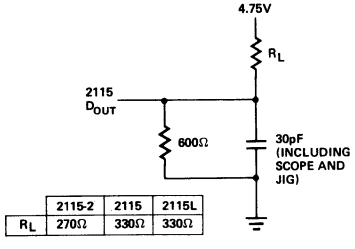
Symbol	Test	2115-2 Limits Min.	Typ.	Max.	2115 Limits Min.	Typ.	Max.	2115L Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5		40	5		45	5		50	ns
t_{RCS}	Chip Select Recovery Time			40			40			40	ns
t_{AA}	**Address Access Time**		55	70		75	95		75	95	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			ns

WRITE CYCLE

Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{WS}	Write Enable Time			40			40			40	ns
t_{WR}	Write Recovery Time	5		45	5		45	5		50	ns
t_W	Write Pulse Width	50			50			50			ns
t_{WSD}	Data Set-Up Time Prior to Write	5			5			15			ns
t_{WHD}	Data Hold Time After Write	5			5			15			ns
t_{WSA}	Address Set-Up Time	15			30			30			ns
t_{WHA}	Address Hold Time	5			5			15			ns
t_{WSCS}	Chip Select Set-Up Time	5			5			15			ns
t_{WHCS}	Chip Select Hold Time	5			5			15			ns

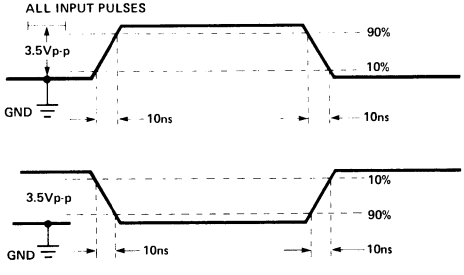
TEST CONDITIONS

A.C. AND D.C. LOADING CONDITIONS

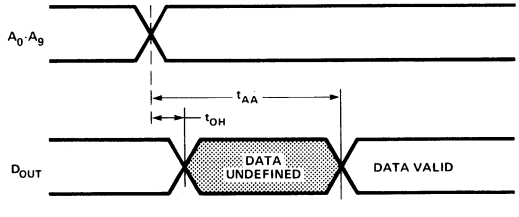


	2115-2	2115	2115L
R_L	270Ω	330Ω	330Ω

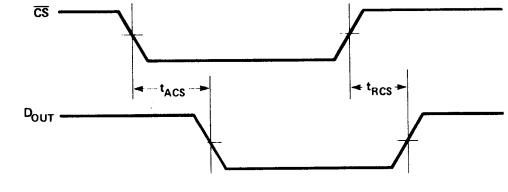
ALL INPUT PULSES



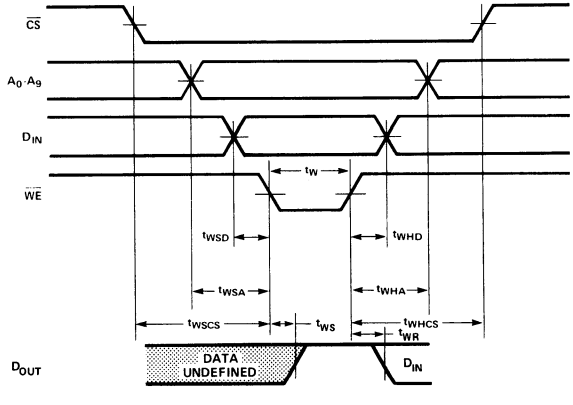
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

2125 Family A.C. Characteristics[1] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

READ CYCLE

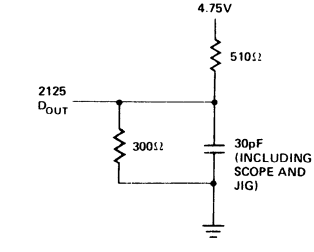
Symbol	Test	2125-2 Limits Min.	Typ.	Max	2125 Limits Min.	Typ.	Max.	2125L Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5		40	5		45	5		50	ns
t_{ZRCS}	Chip Select to HIGH Z			40			40			40	ns
t_{AA}	Address Access Time		55	70		75	95		75	95	ns
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			ns

WRITE CYCLE

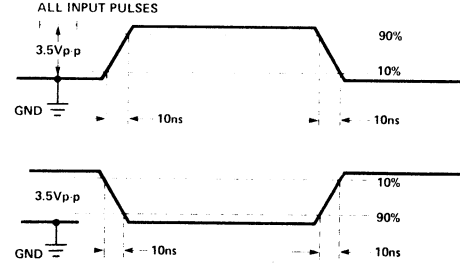
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{ZWS}	Write Enable to HIGH Z			40			40			40	ns
t_{WR}	Write Recovery Time	5		45	5		45	5		50	ns
t_W	Write Pulse Width	50			50			50			ns
t_{WSD}	Data Set-Up Time Prior to Write	5			5			15			ns
t_{WHD}	Data Hold Time After Write	5			5			15			ns
t_{WSA}	Address Set Up Time	15			30			30			ns
t_{WHA}	Address Hold Time	5			5			15			ns
t_{WSCS}	Chip Select Set-Up Time	5			5			15			ns
t_{WHCS}	Chip Select Hold Time	5			5			15			ns

TEST CONDITIONS

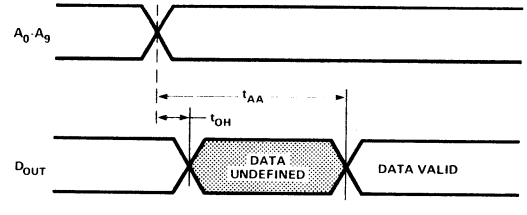
A.C. LOADING CONDITIONS



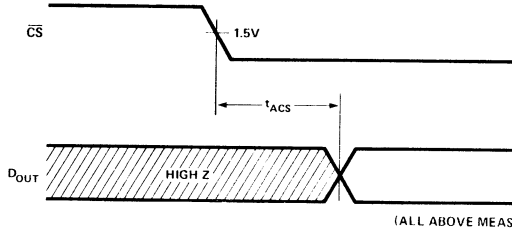
ALL INPUT PULSES



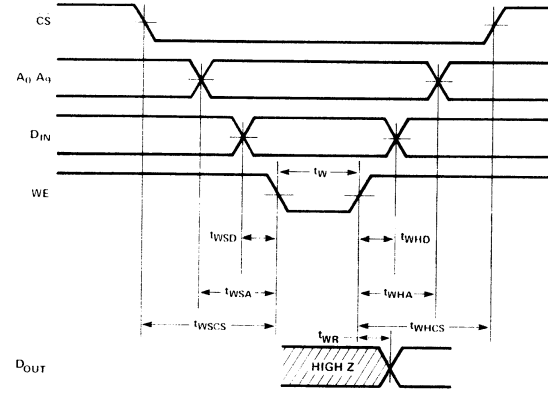
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT

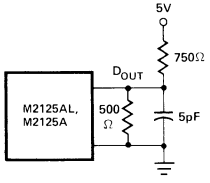


WRITE CYCLE

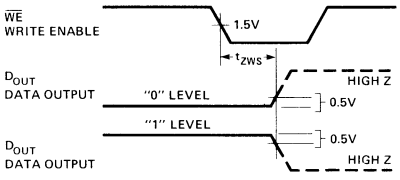


(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

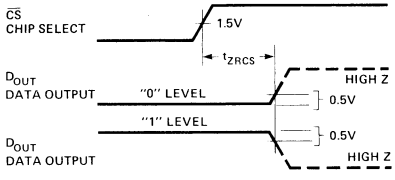
2125 FAMILY WRITE ENABLE TO HIGH Z DELAY



LOAD 1



2125 FAMILY PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(All t_{ZXXX} parameters are measured at a delta of 0.5V from the logic level and using Load 1.)

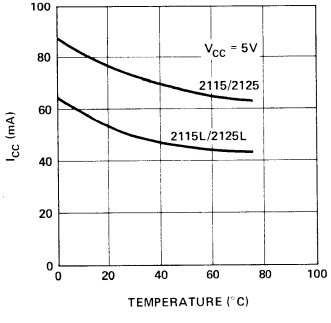
2115/2125 FAMILY CAPACITANCE* V_{CC} = 5V, f = 1 MHz, T_A = 25°C

Symbol	Test	2115 Family Limits Typ.	2115 Family Limits Max.	2125 Family Limits Typ.	2125 Family Limits Max.	Units	Test Conditions
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	$\overline{CS}$=5V, All other inputs = 0V, Output Open

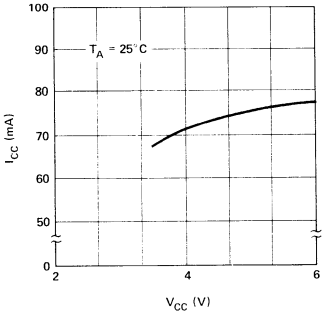
*This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

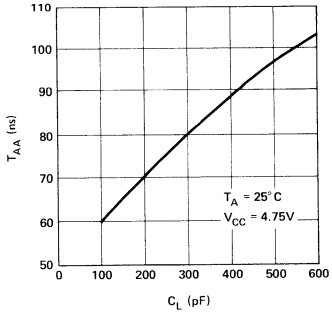
I_{CC} VS. TEMPERATURE



I_{CC} VS. V_{CC}



ACCESS TIME VS. CAPACITANCE



2115A, 2125A FAMILY
HIGH SPEED 1K X 1 BIT STATIC RAM

	2115AL 2125AL	2115A 2125A	2115AL-2 2125AL-2	2115A-2 2125A-2
Max. T_{AA}(ns)	45	45	70	70
Max. I_{CC}(mA)	75	125	75	125

- **Pin Compatible To 93415A (2115A) And 93425A (2125A)**
- **Fan-Out Of 10 TTL (2115A Family) -- 16mA Output Sink Current**
- **Low Operating Power Dissipation --Max. 0.39mW/Bit (2115AL, 2125AL)**
- **TTL Inputs And Outputs**
- **Single +5V Supply**
- **Uncommitted Collector (2115A) And Three-State (2125A) Output**
- **Standard 16-Pin Dual In-Line Package**

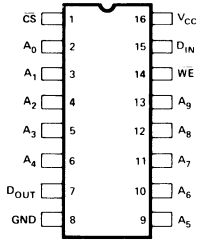
The Intel® 2115A and 2125A families are high-speed, 1024 words by 1 bit random access memories. Both open collector (2115A) and three-state output (2125A) are available. The 2115A and 2125A use fully DC stable (static) circuitry throughout – in both the array and the decoding and, therefore, require no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data.

The 2115AL/2125AL at 45 ns maximum access time and the 2115AL-2/2125AL-2 at 70 ns maximum access time are fully compatible with the industry-produced 1K bipolar RAMs, yet offer a 50% reduction in power of their bipolar equivalents. The power dissipation of the 2115AL/2125AL and 2115AL-2/2125AL-2 is 394 mW maximum as compared to 814 mW maximum of their bipolar equivalents. For systems already designed for 1K bipolar RAMs, the 2115A/2125A and the 2115A-2/2125A-2 at 45 ns and 70 ns maximum access times, respectively, offer complete compatibility with a 20% reduction in maximum power dissipation.

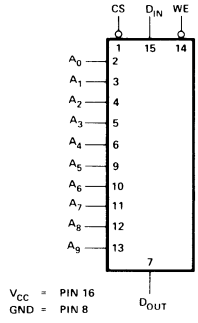
The devices are directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

The 2115A and 2125A families are fabricated with Intel's N-channel MOS Silicon Gate Technology.

PIN CONFIGURATION



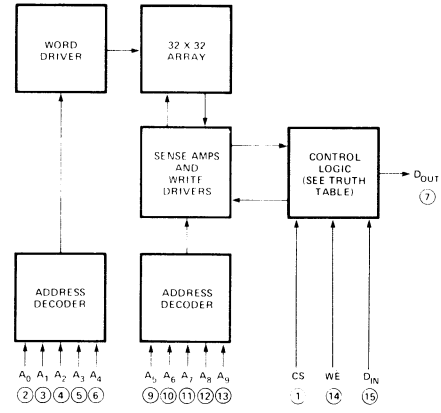
LOGIC SYMBOL



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT 2115A FAMILY	OUTPUT 2125A FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	HIGH Z	NOT SELECTED
L	L	L	H	HIGH Z	WRITE "0"
L	L	H	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -10°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
All Output or Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -0.5V to +5.5V
D.C. Output Current . . . . . 20 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1,2]

V_{CC} = 5V ±5%, T_A = 0°C to 75°C

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
V_{OL1}	2115A Family Output Low Voltage			0.45	V	I_{OL} = 16 mA
V_{OL2}	2125A Family Output Lot Voltage			0.45	V	I_{OL} = 7 mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		-0.1	-40	μA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max., V_{IN} = 4.5V
I_{CEX}	2115A Family Output Leakage Current		0.1	100	μA	V_{CC} = Max., V_{OUT} = 4.5V
$\|I_{OFF}\|$	2125A Family Output Current (High Z)		0.1	50	μA	V_{CC} = Max., V_{OUT} = 0.5V/2.4V
I_{OS}[3]	2125A Family Current Short Circuit to Ground			-100	mA	V_{CC} = Max.
V_{OH}	Family Output High Voltage	2.4			V	I_{OH} = -3.2 mA
I_{CC}	Power Supply Current: I_{CC1}: 2115AL, 2115AL-2, 2125AL, 2125AL-2		60	75	mA	All Inputs Grounded, Output Open
	I_{CC2}: 2115A, 2115A-2, 2125A, 2125A-2		100	125	mA	

NOTES:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (@ 400 f_{PM} air flow) = 45°C/W
   θ_{JA} (still air) = 60°C/W
   θ_{JC} = 25°C/W

2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and maximum loading.
3. Duration of short circuit current should not exceed 1 second.

2115A FAMILY A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

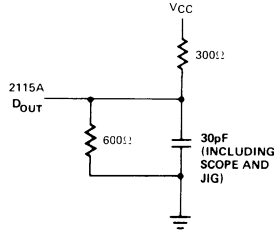
READ CYCLE

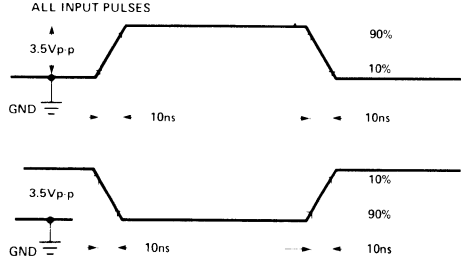
Symbol	Test	2115AL Limits Min.	Typ.	Max.	2115A Limits Min.	Typ.	Max.	2115AL-2 Limits Min.	Typ.	Max.	2115A-2 Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{RCS}	Chip Select Recovery Time		10	30		10	30		10	30		10	40	ns
t_{AA}	**Address Access Time**		**30**	**45**		**30**	**45**		**40**	**70**		**40**	**70**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			10			ns

WRITE CYCLE

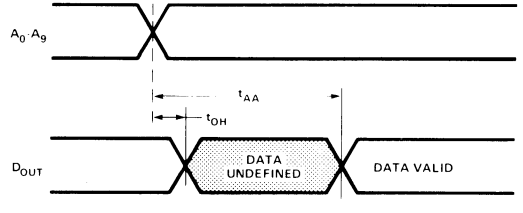
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{WS}	Write Enable Time		10	25		10	30		10	25		10	40	
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	15		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	−5		5	−5		0	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

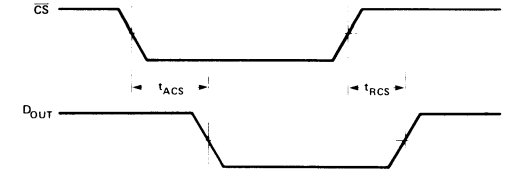




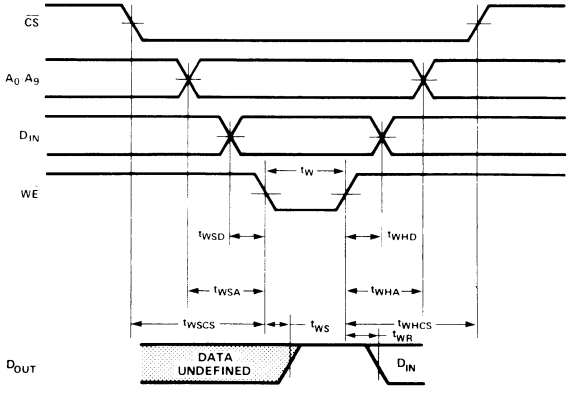
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

2125A FAMILY A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

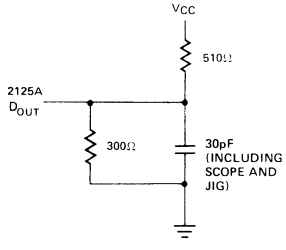
READ CYCLE

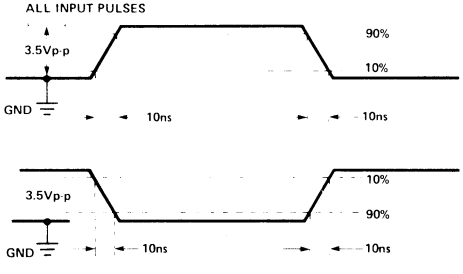
Symbol	Test	2125AL Limits Min.	Typ.	Max.	2125A Limits Min.	Typ.	Max.	2125AL-2 Limits Min.	Typ.	Max.	2125A-2 Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{ZRCS}	Chip Select to HIGH Z		10	30		10	30		10	30		10	40	ns
t_{AA}	**Address Access Time**		**30**	**45**		**30**	**45**		**40**	**70**		**40**	**70**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			10			ns

WRITE CYCLE

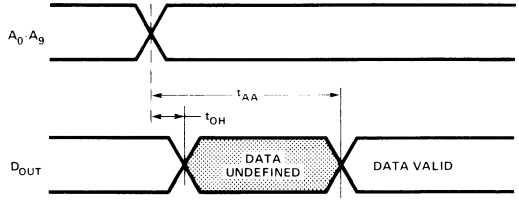
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{ZWS}	Write Enable to HIGH Z		10	25		10	30		10	25		10	40	ns
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	10		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	−5		5	−5		0	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

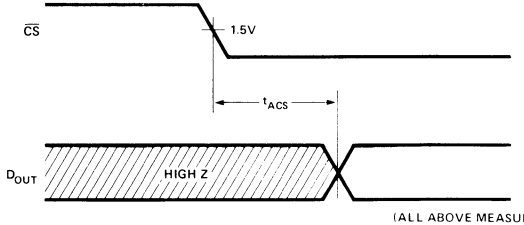




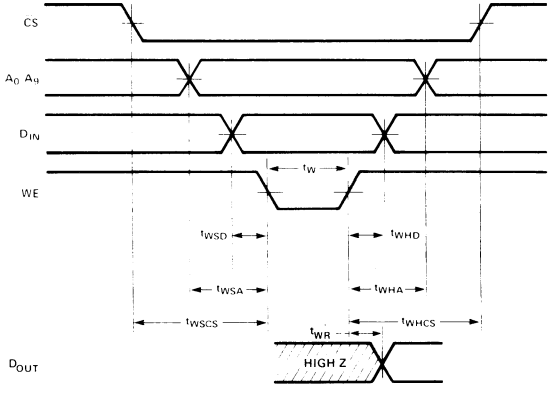
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT

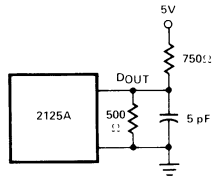


WRITE CYCLE

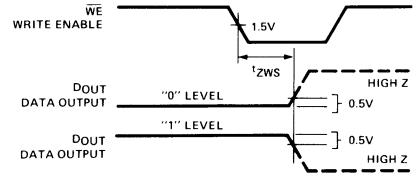


(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

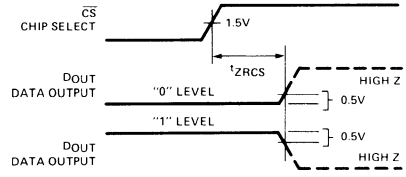
2125A FAMILY WRITE ENABLE TO HIGH Z DELAY



LOAD 1



2125A FAMILY PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(ALL t_{ZXXX} PARAMETERS ARE MEASURED AT A DELTA OF 0.5V FROM THE LOGIC LEVEL AND USING LOAD 1.)

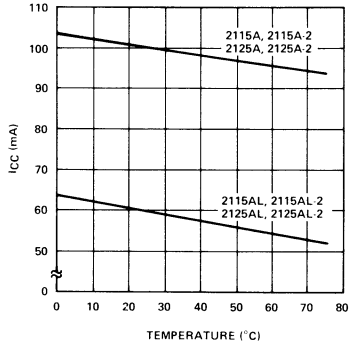
2115A/2125A FAMILY CAPACITANCE* V_{CC}= 5V, f = 1 MHz, T_A = 25°C

SYMBOL	TEST	2115A Family LIMITS		2125A Family LIMITS		UNITS	TEST CONDITIONS
		TYP.	MAX.	TYP.	MAX.		
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	$\overline{CS}$ = 5V, All Other Inputs = 0V, Output Open

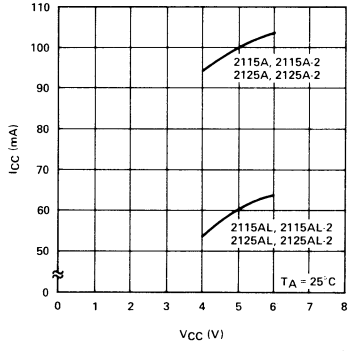
*This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

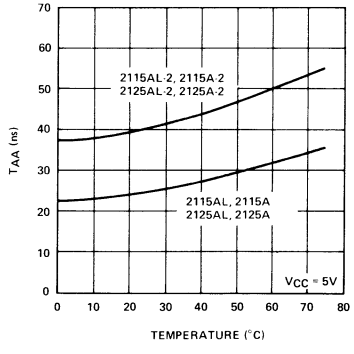
I_{CC} VS. TEMPERATURE



I_{CC} VS. V_{CC}



ACCESS TIME VS. TEMPERATURE



M2115A, M2125A, FAMILY
HIGH SPEED 1K X 1 BIT STATIC RAM

	M2115AL, M2125AL	M2115A, M2125A
Max. T_{AA} (ns)	75	55
Max. I_{CC} (mA)	75	125

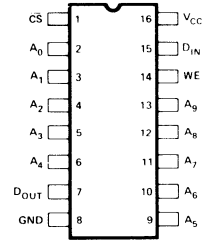
- **Low Operating Power Dissipation 413mW (M2115AL, M2125AL)**
- **Fast Access Time Over −55°C to 125°C --55ns Maximum (M2115A, M2125A)**
- **Single 5V Supply With ±10% Tolerance**
- **TTL Inputs and Output**
- **Uncommitted Collector (M2115A, M2115AL) and Three State (M2125A, M2125AL) Output**
- **Non-Inverting Data Output**
- **Hermetic 16 Pin Dual In-Line Package**

The Intel® M2115A and M2125A families are fully static, random access memories (RAMs) organized as 1024 words by 1 bit, which operate over a −55°C to +125°C ambient temperature range. Both open collector (M2115A) and three-state (M2125A) outputs are available. The M2115A and M2125A use fully DC stable (static) circuitry throughout in both the array and the decoding, and, therefore, require no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

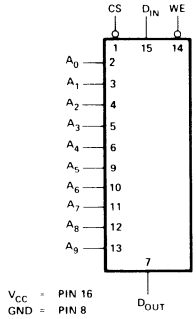
The M2125AL/M2125AL is ideal for high-performance systems where speed and power dissipation are significant design considerations. They have a maximum access time of 75 ns, while power dissipation is only 413 mW maximum. The M2115A/M2125A at 55 ns maximum should be considered for applications in which speed is a primary design objective.

The devices are directly TTL compatible in all respects: inputs, outputs and a single +5V supply. A separate chip select lead allows easy selection of an individual package when outputs are OR-tied.

PIN CONFIGURATION



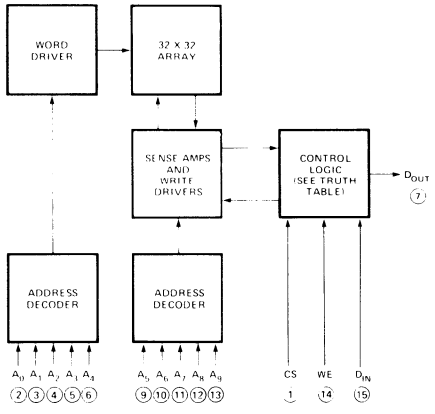
LOGIC SYMBOL



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT 2115A FAMILY	OUTPUT 2125A FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	HIGH Z	NOT SELECTED
L	L	L	H	HIGH Z	WRITE "0"
L	L	H	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −65°C to +135°C
Storage Temperature . . . . . −65°C to +150°C
All Output or Supply Voltages. . . . . −0.5V to +7V
All Input Voltages . . . . . −0.5V to +6V
D.C. Output Current . . . . . 20 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1,2]

V_{CC} = 5V ±10%, T_A = −55°C to +125°C

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
V_{OL1}	M2115A, M2115AL Output Low Voltage			0.45	V	I_{OL} = 10 mA
V_{OL2}	M2125A, M2125AL Output Low Voltage			0.45	V	I_{OL} = 5 mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		−0.1	−40	μA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max., V_{IN} = 4.5V
I_{CEX}	M2115A, M2115AL Output Leakage Current		0.1	100	μA	V_{CC} = Max., V_{OUT} = 4.5V
$\|I_{OFF}\|$	M2125A, M2125AL Output Leakage Current (High Z)		0.1	50	μA	V_{CC} = Max., V_{OUT} = 0.5V/2.4V
I_{OS}[3]	M2125A, M2125AL Current Short Circuit to Ground			−100	mA	V_{CC} = Max.
V_{OH}	M2115A, M2115AL Output High Voltage	2.4			V	I_{OH} = −3.2 mA
I_{CC1}	M2115AL, M2125AL Power Supply Current		60	75	mA	All Inputs Grounded, Output Open
I_{CC2}	M2115A, M2125A Power Supply Current		100	125	mA	All Inputs Grounded, Output Open

NOTES:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (@ 400 f_{PM} air flow) = 45°C/W
   θ_{JA} (still air) = 60°C/W
   θ_{JC} = 25°C/W

2. Typical limits are at V_{CC} = 5V, T_A = +25°C and maximum loading.
3. Duration of short circuit current should not exceed 1 second.

M2115AL, M2115A A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±10%, T_A = −55°C to +125°C

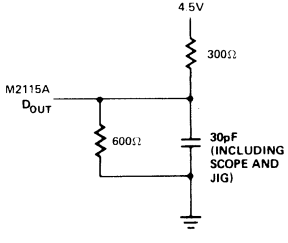
READ CYCLE

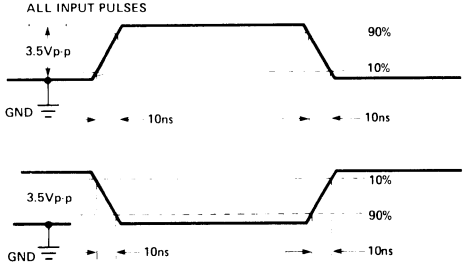
Symbol	Test	M2115AL Limits			M2115A Limits			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{ACS}	Chip Select Time	5		45	5		45	ns
t_{RCS}	Chip Select Recovery Time			50			35	ns
t_{AA}	**Address Access Time**		**40**	**75**		**35**	**55**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			ns

WRITE CYCLE

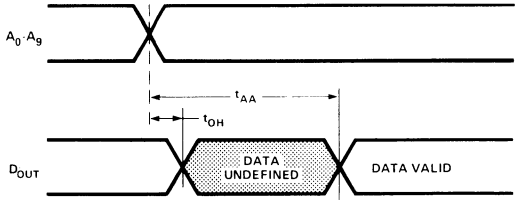
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{WS}	Write Enable Time			45			35	ns
t_{WR}	Write Recovery Time	0		50	0		35	ns
t_W	Write Pulse Width	55	10		40	10		ns
t_{WSD}	Data Setup Time Prior to Write	5	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		ns
t_{WSA}	Address Setup Time	15	0		5	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		ns
t_{WSCS}	Chip Select Setup Time	5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		ns

A.C. TEST CONDITIONS

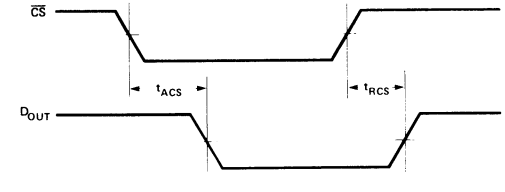




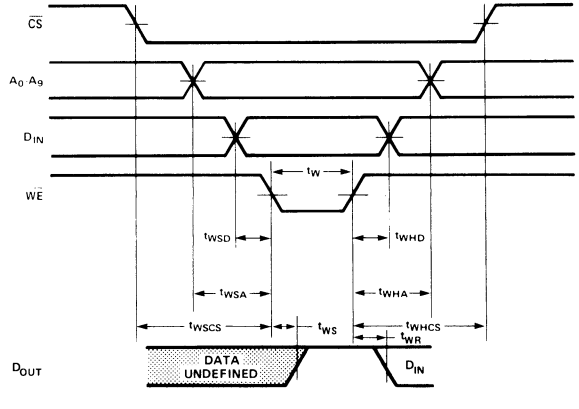
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

M2125AL, M2125A A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±10%, T_A = −55°C to +125°C

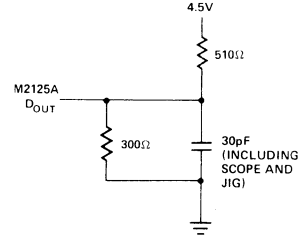
READ CYCLE

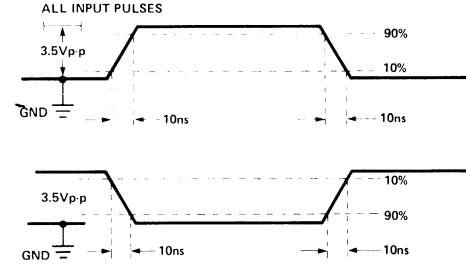
Symbol	Test	M2125AL Limits Min.	Typ.	Max.	M2125A Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5		45	5		45	ns
t_{ZRCS}	Chip Select to HIGH Z			50			35	ns
t_{AA}	**Address Access Time**		**40**	**75**		**25**	**55**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			ns

WRITE CYCLE

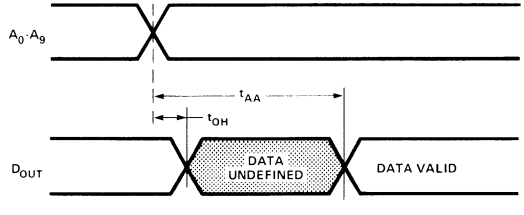
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{ZWS}	Write Enable to HIGH Z			45			35	ns
t_{WR}	Write Recovery Time	0		50	0		35	ns
t_W	Write Pulse Width	55	10		40	10		ns
t_{WSD}	Data Setup Time Prior to Write	5	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		ns
t_{WSA}	Address Setup Time	15	0		5	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		ns
t_{WSCS}	Chip Select Setup Time	5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		ns

A.C. TEST CONDITIONS

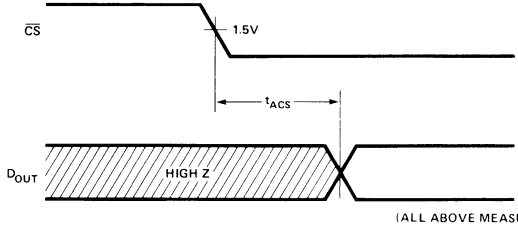




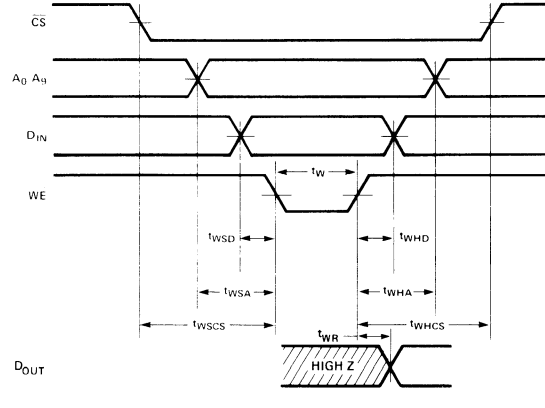
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT

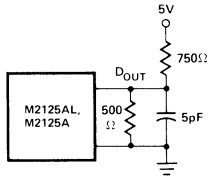


WRITE CYCLE

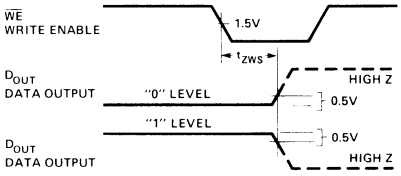


(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

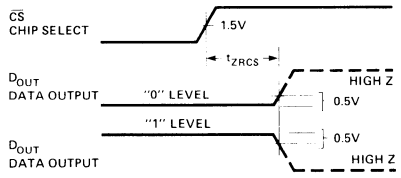
M2125AL, M2125A WRITE ENABLE TO HIGH Z DELAY



LOAD 1



M2125AL, M2125A PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(All t_{ZXX} parameters are measured at a delta of 0.5V from the logic level and using Load 1.)

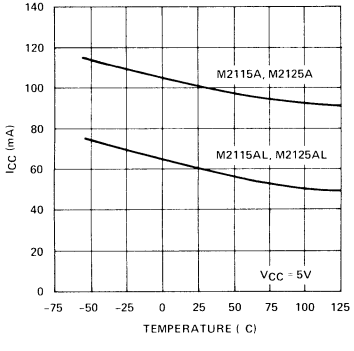
CAPACITANCE* V_{CC} = 5V, f = 1 MHz, T_A = 25°C

Symbol	Test	M2115AL, M2115A Limits		M2125AL, M2125A Limits		Units	Test Conditions
		Typ.	Max.	Typ.	Max.		
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	CS = 5V, All other inputs = 0V, Output Open

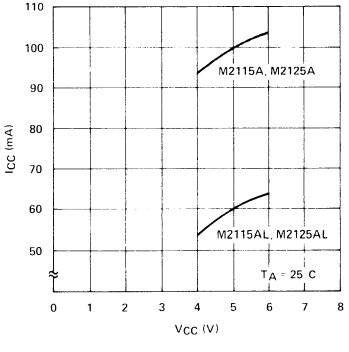
*This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

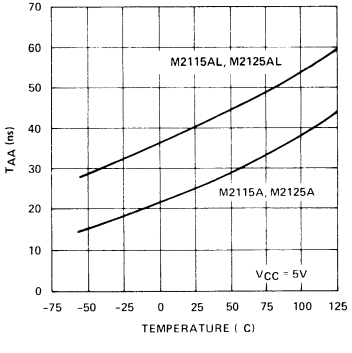
I_{CC} vs. TEMPERATURE



I_{CC} vs. V_{CC}



ACCESS TIME vs. TEMPERATURE



2116 FAMILY

16,384 X 1 BIT DYNAMIC RAM

	2116-2	2116-3	2116-4
Max. Access Time (ns)	200	250	300
Read, Write Cycle (ns)	350	375	425
Read-Modify-Write Cycle (ns)	400	525	595

- **Highest Density 16K RAM: Industry Standard 16 Pin Package**
- **Low Standby Power**
- **All Inputs Including Clocks TTL Compatible**
- **±10% Tolerance on all Power Supplies +12V, +5V, −5V**
- **On-Chip Latches for Address and Data In**
- **Only 64 Refresh Cycles Required Every 2 ms**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**

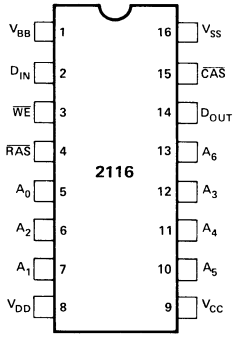
The Intel® 2116 is a 16,384 word by 1 bit MOS RAM fabricated with two layer polysilicon N-MOS technology — a production-proven process for high performance, high reliability, and high functional density. The 2116 uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2116 allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment. The 2116 is designed to facilitate upgrading of 2104A-type 4K RAM systems to 16K capabilities.

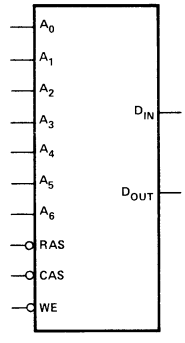
The use of the 16 pin package is made possible by multiplexing the 14 address bits (required to address 1 of 16,384 bits) into the 2116 on 7 address input pins. The two 7 bit address words are latched into the 2116 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention. Refreshing can be accomplished every 2 ms by any one of the three following methods: (1) $\overline{CAS}$ before $\overline{RAS}$ cycles on 64 addresses, A_0–A_5, (2) $\overline{RAS}$-only cycles on 128 address, A_0–A_6, or (3) normal read or write cycles on 128 addresses, A_0–A_6. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed. The output is brought to a high impedance state by a $\overline{CAS}$-only cycle or by a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

PIN CONFIGURATION



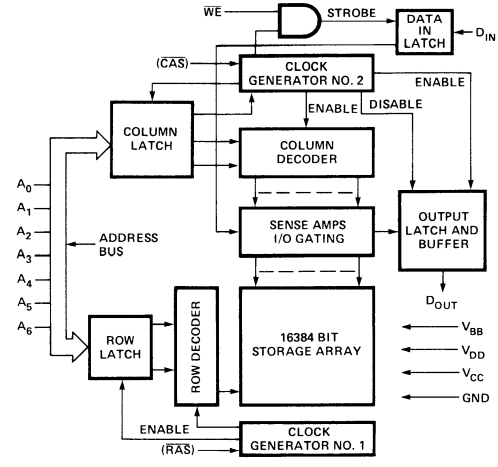
LOGIC SYMBOL



PIN NAMES

A_0 - A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - V_{BB} ⩾ 4V) ..... -0.3V to +20V
Power Dissipation 1.25W

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics [1],[2]

T_A = 0°C to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions	
		Min.	Typ.[3]	Max.			
I_{LI}	Input Load Current (any input)			10	µA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$	
$\|I_{LO}\|$	Output Leakage Current for high impedance state		0.1	10	µA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current		1.2	2	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH} or $\overline{CAS}$-only cycle. Chip deselected prior to measurement. See Note 5.	
I_{BB1}	V_{BB} Supply Current		1	50	µA		
I_{DD2}[4]	Operating V_{DD} Current		53	69	mA	2116-2 t_{CYC} = 350 ns	T_A = 25°C Device selected. See Note 6.
			51	68	mA	2116-3 t_{CYC} = 375 ns	
			49	65	mA	2116-4 t_{CYC} = 425 ns	
I_{BB2}	Operating V_{BB} Current		120	400	µA	Device selected	
I_{CC1}[7]	V_{CC} Supply Current when deselected			10	µA		
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V		
V_{IH}	Input High Voltage (any input)	2.4		V_{CC}+1	V		
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 4.1 mA (Read Cycle Only)	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA (Read Cycle Only)	

Capacitance [8]

T_A = 25°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{I1}	Address, Data In & $\overline{WE}$ Capacitance	4	7	pF	V_{IN} = V_{SS}
C_{I2}	$\overline{RAS}$ Capacitance	3	5	pF	V_{IN} = V_{SS}
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF	V_{IN} = V_{SS}
C_O	Data Output Capacitance	3	7	pF	V_{OUT} = 0V

Notes:
1. All voltages referenced to V_{SS}. No power supply sequencing is required but V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}.
2. To avoid self-clocking, $\overline{RAS}$ should not be allowed to float.
3. Typical values are for T_A = 25°C and nominal power supply voltages.
4. For $\overline{RAS}$-only refresh I_{DD} = 0.78 I_{DD2}. For $\overline{CAS}$-before-$\overline{RAS}$ (64 cycle refresh) I_{DD} = 0.96 I_{DD2}.
5. The chip is deselected (i.e., output is brought to high impedance state) by $\overline{CAS}$-only cycle or by $\overline{CAS}$-before-$\overline{RAS}$ cycle. The current flowing in a selected (i.e., output on) chip with $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} is approximately twice I_{DD1}.
6. See Page 2-98 for typical I_{DD} characteristics under other conditions.
7. When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
8. Capacitance measured with Boonton Meter.

Typical Characteristics

I_{BB2} AND I_{DD2} VS. TEMPERATURE

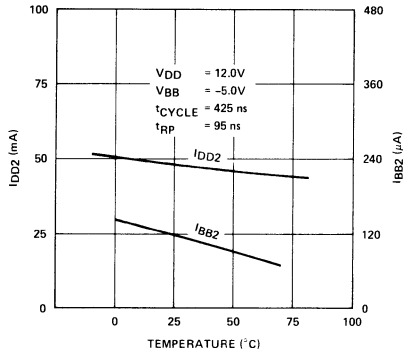


Figure 1.

I_{DD2} VS. CYCLE TIME

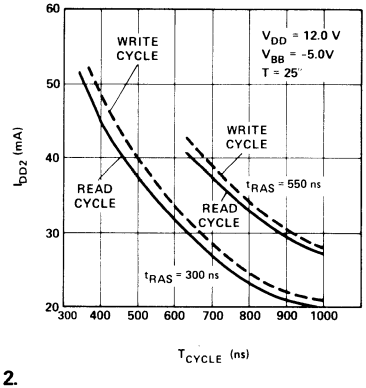


Figure 2.

Standby Power Calculations:

$$P_{REF} = P_{OP}\left(N\frac{t_{CYC}}{t_{REF}}\right) + P_{SB}\left(1 - N\frac{t_{CYC}}{t_{REF}}\right) \text{ where}$$

P_{OP} = Power dissipation (continuous operation) $\cong V_{DD} \times I_{DD2}$.

N = Number of refresh cycles (64 or 128)

t_{CYC} = Cycle time for a refresh cycle.

t_{REF} = Time between refreshes

P_{SB} = Standby power dissipation = $V_{DD} \times I_{DD1} + |V_{BB}| \times I_{BB}$

Note that I_{DD2} depends upon refresh as follows:

1. For 128 cycle ($\overline{RAS}$ before $\overline{CAS}$) use I_{DD2} from Figures 1 and 2.
2. For 64 cycle ($\overline{CAS}$ before $\overline{RAS}$) multiply I_{DD2} determined in (1) by 0.96.
3. For 128 cycle ($\overline{RAS}$ only) multiply I_{DD2} determined in (1) by 0.78.

Examples of typical calculations for V_{BB} = -5.0V, V_{DD} = 12.0V, $T_A = 25°C$, $t_{CYC} = 0.425\ \mu s$, $t_{RAS} = 0.3\ \mu s$. $t_{REF} = 2000\ \mu s$:

1. 128 cycle ($\overline{RAS}$ before $\overline{CAS}$): P_{OP} = 12.0V x 43 mA = 516 mW

   $$P_{REF} = 516\left(128\ \frac{0.425}{2000}\right) + (12x1.2+5x0.001)\left(1-128\ \frac{0.425}{2000}\right)$$

   P_{REF} = 28.0 mW

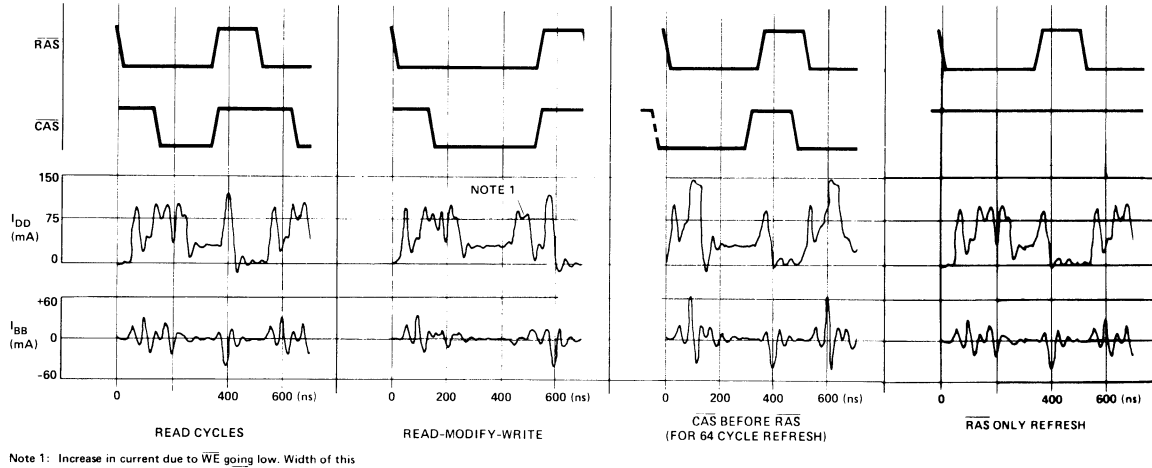
2. 64 cycle ($\overline{CAS}$ before $\overline{RAS}$); P_{OP} = 12.0V x 43 (0.96) mA = 495 mW.

   $$P_{REF} = 495\left(64\ \frac{0.425}{2000}\right) + (12x1.2+5x0.001)\left(1-64\ \frac{0.425}{2000}\right) =$$

   P_{REF} = 20.9 mW

3. 128 cycle ($\overline{RAS}$ only): P_{OP} = 12.0V x 43 (0.78) mA = 402 mW

   P_{REF} = 25.0 mW



Note 1: Increase in current due to $\overline{WE}$ going low. Width of this current pulse is independent of $\overline{WE}$ pulse width.

Figure 3. Supply Current Waveforms.

A.C. Characteristics[1]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=−5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2116-2 Min.	2116-2 Max.	2116-3 Min.	2116-3 Max.	2116-4 Min.	2116-4 Max.	Unit
t_{REF}	Time Between Refresh		2		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	75		75		95		ns
t_{CP}	$\overline{CAS}$ Precharge Time	100		125		125		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	45	75	50	110	60	110	ns
t_{CRP}[3]	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	160		200		220		ns
t_{CSH}	$\overline{CAS}$ Hold Time	200		250		300		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		ns
t_{ASC}	Column Address Set-Up Time	−10		−10		−10		ns
t_{AH}	Address Hold Time	45		50		60		ns
t_T	Transition Time (Rise and Fall)		50		50		50	ns
t_{OFF}	Output Buffer Turn Off Delay	0	60	0	60	0	80	ns
t_{CAC}[4]	Access Time From $\overline{CAS}$		125		150		190	ns
t_{RAC}[4]	Access Time From $\overline{RAS}$		200		250		300	ns

READ AND REFRESH CYCLES

Symbol	Parameter	2116-2 Min.	2116-2 Max.	2116-3 Min.	2116-3 Max.	2116-4 Min.	2116-4 Max.	Unit
t_{CYC}[5]	Random Read Cycle Time	350		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	300	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	10000	150	10000	190	10000	ns
t_{CH}	$\overline{CAS}$ Hold Time for $\overline{RAS}$-Only Refresh	30		30		30		ns
t_{CPR}	$\overline{CAS}$ Precharge for 64 Cycle Refresh	30		30		30		ns
t_{RCH}	Read Command Hold Time	20		20		20		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{DOH}	Data-Out Hold Time	32		32		32		μs

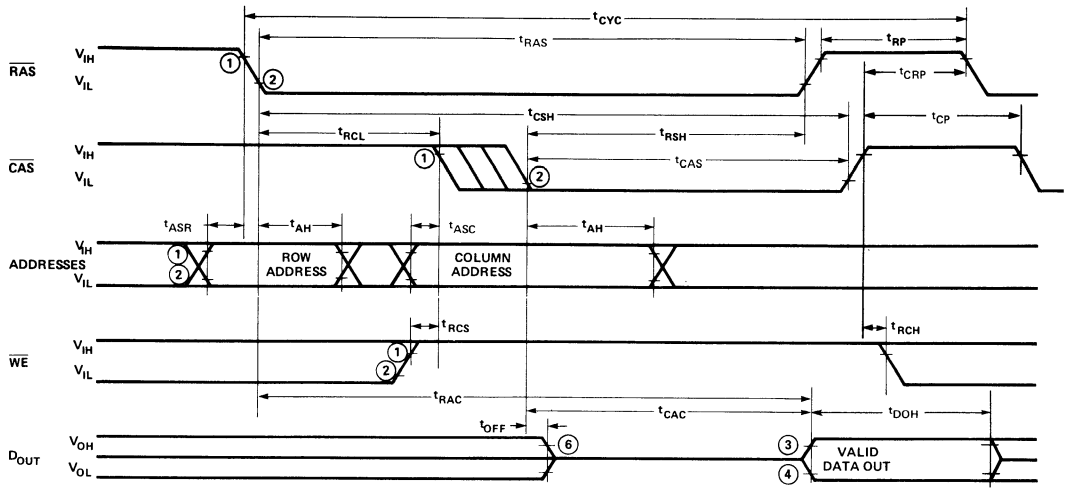
WRITE CYCLE

Symbol	Parameter	2116-2 Min.	2116-2 Max.	2116-3 Min.	2116-3 Max.	2116-4 Min.	2116-4 Max.	Unit
t_{CYC}[5]	Random Write Cycle Time	350		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	300	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	10000	150	10000	190	10000	ns
t_{WCH}	Write Command Hold Time	75		100		100		ns
t_{WP}	Write Command Pulse Width	50		100		100		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		150		160		ns
t_{DS}[6]	Data-In Set-Up Time	0		0		0		ns
t_{DH}[6]	Data-In Hold Time	100		100		125		ns

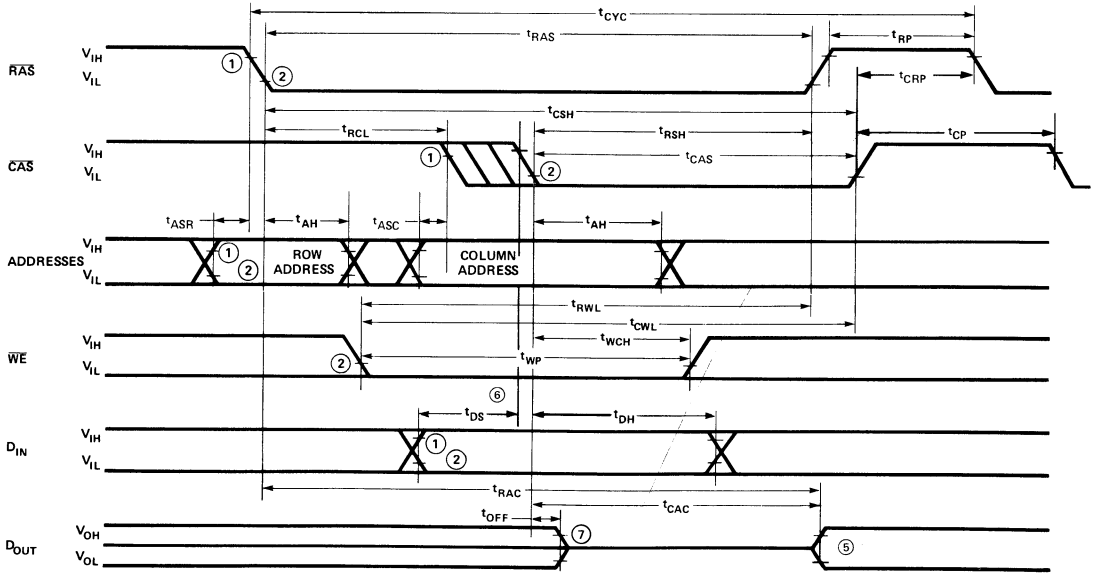
Notes:
1. All voltages referenced to V_{SS}.
2. $\overline{CAS}$ must remain at V_{IH} a minimum of $t_{RCL\ MIN}$ after $\overline{RAS}$ switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before $t_{RCL\ (MAX)} = t_{RAC} - t_{CAC}$. Device operation is not guaranteed for $t_{RCL} > 2$ μs.
3. The t_{CRP} specification is less restrictive than the t_{CRL} range which was specified in the 2116 preliminary data sheet.
4. Load = 1 TTL and 50 pF.
5. The minimum cycle timing does not allow for t_T or skews.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

Waveforms

READ CYCLE



WRITE CYCLE



Notes:
1,2. V_{IH} MIN and V_{IL} MAX are reference levels for measuring timing of input signals.
3,4. V_{OH} MIN and V_{OL} MAX are reference levels for measuring timing of D_{OUT}.
5. D_{OUT} follows D_{IN} when writing, with $\overline{WE}$ before $\overline{CAS}$.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

A.C. Characteristics

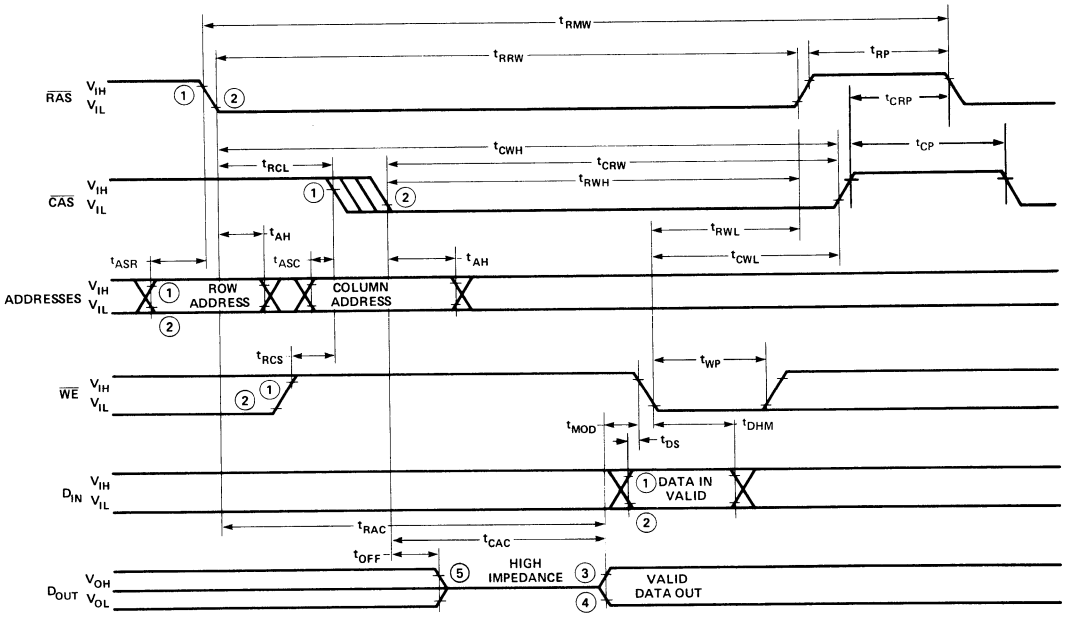
T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%, V_{SS} = 0V, unless otherwise noted.

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2116-2 Min.	2116-2 Max.	2116-3 Min.	2116-3 Max.	2116-4 Min.	2116-4 Max.	Unit
t_{RMW}	Read-Modify-Write Cycle Time	400		525		595		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	225	10000	310	10000	350	10000	ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	325	32000	450	32000	500	32000	ns
t_{RWH}	RMW Cycle $\overline{RAS}$ Hold Time	250		350		390		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	300		410		460		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		160		160		ns
t_{WP}	Write Command Pulse Width	50		100		100		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{MOD}	Modify Time	0	10	0	10	0	10	µs
t_{DS}	Data-In Set-Up Time	0		0		0		ns
t_{DHM}	Data-In Hold Time (RMW Cycle)	50		100		125		ns

Waveforms

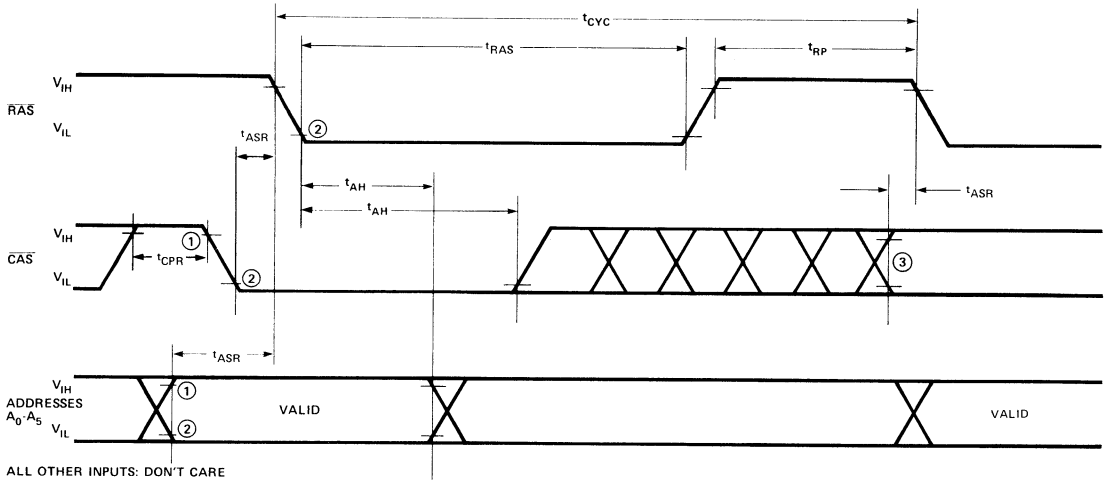
READ MODIFY WRITE CYCLE



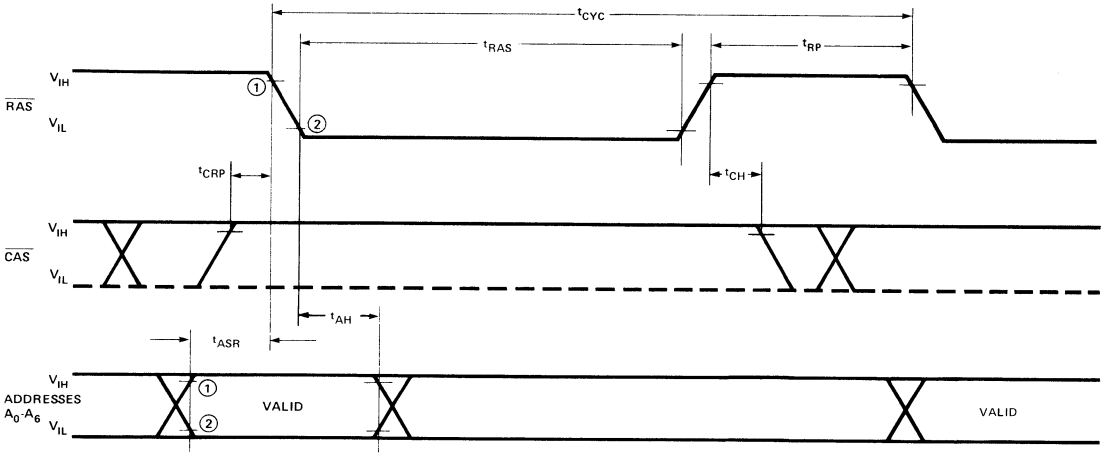
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.

Refresh Cycle Waveforms

$\overline{CAS}$ BEFORE $\overline{RAS}$ CYCLES. (64 CYCLE REFRESH)



$\overline{RAS}$ ONLY CYCLES (128 CYCLE REFRESH)



Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3. $\overline{CAS}$ must be high or low as appropriate for the next cycle.

Applications Information

REFRESH MODES

The 2116 may be refreshed in any of three modes. Read/Refresh cycles and $\overline{RAS}$-only cycles refresh the row addressed by A_0 through A_6 and therefore require 128 cycles to refresh the stored data. Assuming a 500 nsec system cycle time, the refresh operations require 64 μsec out of each 2.0 msec refresh period or 3.2% of the available memory time. The third 2116 refresh mode, $\overline{CAS}$-before-$\overline{RAS}$, allows refresh of the stored data in only 64 cycles and requires only 32 μsec or 1.6% of the available memory time (equal to the 64-cycle refresh 4K RAMs). While some 2116 aplications would not be impacted by the 3.2% memory lockout time using 128 cycle refresh, most large mainframe memory applications would suffer throughput degradation in that refresh mode. Intel designed the 2116 to allow either 128-cycle or 64-cycle refresh, allowing the system designer to choose the refresh mode which fits his system needs. In addition to allowing higher memory throughput, the $\overline{CAS}$-before-RAS 64-cycle refresh mode dissipates approximately 14% less power than the 128-cycle $\overline{RAS}$-only mode and 23% less power than the 128-cycle Read/Refresh mode (refer to the Standby Power Calculation section).

POWER SUPPLY DECOUPLING/ DISTRIBUTION

Power supply current waveforms for the 2116 are shown in Figure 3. The V_{DD} supply provides virtually all of the operating current for the 2116. The V_{DD} supply current, I_{DD}, has two components: transient current peaks when the clocks change state and a DC component while the clocks are active (low). When selecting the decoupling capacitors for the V_{DD} supply, the characteristics of capacitors as well as the current waveform must be considered. Suppression of transient or pulse currents require capacitors with small physical size and low inherent inductance. Monolithic and other ceramic capacitors exhibit these desirable characteristics. When the current waveform indicates a DC component, bulk capacity must be located near the current load to supply the load power. Inductive effects of PC board traces and bus bars preclude supplying the DC component from bulk capacitors at the periphery of a memory matrix without voltage droop during the active portion of a memory cycle. This means that some bulk capacity in the form of electrolytic or large ceramic capacitors should be distributed around or within the memory matrix.

The V_{BB} supply current, I_{BB}, has high transient current peaks, with essentially no DC component (less than 400 microamperes). The V_{BB} capacitors should be selected for transient suppression characteristics. The following capacitance values and locations are recommended for the 2116:

1. A 0.33 μF ceramic capacitor between V_{DD} and V_{SS} (ground) at every other device.
2. A 0.1 μF ceramic capacitor between V_{BB} and V_{SS} at every other device (preferably alternate devices to the V_{DD} decoupling above).
3. A 4.7 μF electrolytic capacitor between V_{DD} and V_{SS} for each eight devices and located adjacent to the devices.

The V_{CC} supply is connected only to the 2116 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is usually only the input high level current to a TTL gate and the output leakage currents of any OR-tied 2116s (typically 100 μA or less total). Intel recommends that a 0.1 or 0.01 μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight devices to preclude coupled noise from affecting the TTL devices in the system.

Intel recommends a power supply distribution system such that each power supply is grided both horizontally and vertically at each memory device. This technique minimizes the power distribution system impedance and enhances the effect of the decoupling capacitors.

OUTPUT DATA LATCH

The 2116 contains an output data latch eliminating the need for an external system data latch and the timing circuitry required to strobe an external latch. The 2116 output latch operates identically to the output latch found on all industry standard 16-pin, 4K RAMs and enhances the system compatibility of the 16K and 4K devices.

Operation of the output latch is controlled by $\overline{CAS}$. The data output will go to the high-impedance state immediately following the $\overline{CAS}$ leading edge during each data cycle and will either go to valid data at access time on selected devices (devices receiving both $\overline{RAS}$ and $\overline{CAS}$) or will remain in the high impedance state on unselected devices (devices receiving only $\overline{CAS}$). During $\overline{RAS}$-only refresh cycles, the data output remains in the state it was prior to the $\overline{RAS}$-only cycle. This unique feature of latched output RAMs allows a refresh cycle to be hidden among data cycles without impacting data availability. For instance, a $\overline{RAS}$-only refresh cycle could follow each data cycle in a microprocessor system but the accessed data would remain at the device output and the microprocessor could take the data at any time within the cycle. Non-latched output devices do not provide this type of hidden refresh capability since their data output would go to the high impedance state at the end of the data cycle.

PAGE MODE OPERATION

The 2116 is designed for page mode operation and is presently being characterized for that mode. Specifications will be available at a later date.

ADVANCE INFORMATION
Characteristics are Subject to Change Without Notice

2147
4096 X 1 BIT STATIC RAM

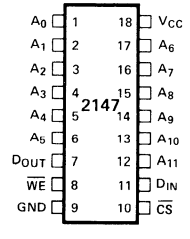
- **60 to 90 ns Access Time**
- **Low Operating Power Dissipation 500 mW Typical**
- **Low Standby Power Dissipation 50 mW Typical**
- **Single +5V Supply**
- **High Density 18-Pin Package**
- **Identical Cycle and Access Times**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Separate Data Input and Output**
- **Three-State Output**

The Intel® 2147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using N-channel Silicon-Gate MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

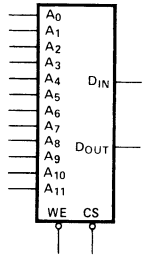
$\overline{CS}$ controls the power down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the 2147 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. There is no minimum $\overline{CS}$ high time for device operation, although it will determine the length of time in the power down mode. When $\overline{CS}$ goes low — selecting the 2147 — the 2147 automatically powers up with no performance penalty. The access time from Chip Select is equivalent to the access time from an address transition with the chip selected.

The 2147 is placed in an 18-pin package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

PIN CONFIGURATION



LOGIC SYMBOL



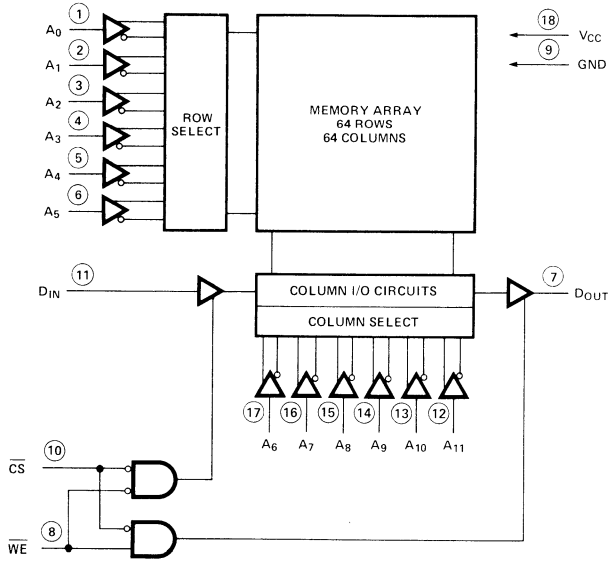
PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

BLOCK DIAGRAM



3101, 3101A

16 x 4 BIT HIGH SPEED RAM

- **Fast Access Time -- 35 nsec. max. over 0-75° C Temperature Range.** (3101A)
- **Simple Memory Expansion through Chip Select Input -- 17 nsec. max. over 0-75° C Temperature Range.** (3101A)
- **DTL and TTL Compatible -- Low Input Load Current: 0.25mA. max.**
- **OR-Tie Capability -- Open Collector Outputs.**
- **Fully Decoded -- on Chip Address Decode and Buffer.**
- **Minimum Line Reflection -- Low Voltage Diode Input Clamp.**
- **Ceramic and Plastic Package -- 16 Pin Dual In-Line Configuration.**

The Intel® 3101 and 3101A are high speed fully decoded 64 bit random access memories, organized 16 words by 4 bits. Their high speed makes them ideal in scratch pad applications. An unselected chip will not generate noise at its output during writing of a selected chip. The output is held high on an unselected chip regardless of the state of the read/write signal.

The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices with gold diffusion processes.

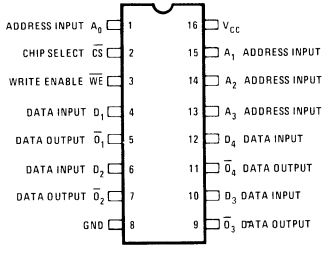
The Intel 3101 and 3101A are packaged in either hermetically sealed 16 pin ceramic packages, or in low cost silicone packages, and their performance is specified over a temperature range from 0° C to 75° C.

The storage cells are addressed through an on chip 1 of 16 binary decoder using four input address leads.

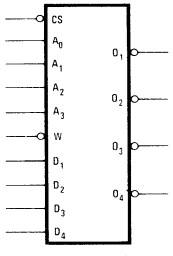
A separate Chip Select lead allows easy selection of an individual package when outputs are OR-tied.

In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.

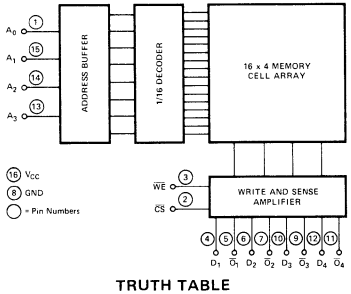
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_1–D_4	DATA INPUTS	$\overline{CS}$	CHIP SELECT INPUT
A_0–A_3	ADDRESS INPUTS	$\overline{O}_1$–$\overline{O}_4$	DATA OUTPUTS
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)

TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
LOW	LOW	WRITE	HIGH
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
HIGH	LOW	–	HIGH
HIGH	HIGH	–	HIGH

Absolute Maximum Ratings*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		100 mA

*COMMENT:

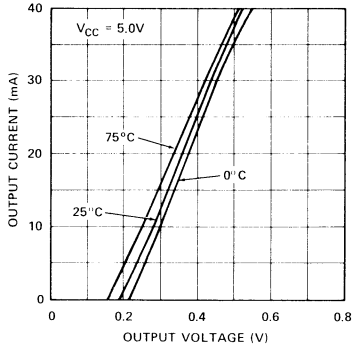
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

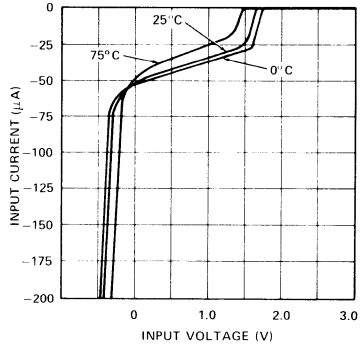
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_A =0.45V
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_D =0.45V
I_{FW}	WRITE INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_W =0.45V
I_{FS}	CHIP SELECT INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_S =0.45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT		10	µA	V_{CC} =5.25V, V_A =5.25V
I_{RD}	DATA INPUT LEAKAGE CURRENT		10	µA	V_{CC} =5.25V, V_D =5.25V
I_{RW}	WRITE INPUT LEAKAGE CURRENT		10	µA	V_{CC} =5.25V, V_W =5.25V
I_{RS}	CHIP SELECT INPUT LEAKAGE CURRENT		10	µA	V_{CC} =5.25V, V_S =5.25V
V_{CA}	ADDRESS INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_A =−5.0 mA
V_{CD}	DATA INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_D =−5.0 mA
V_{CW}	WRITE INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_W =−5.0 mA
V_{CS}	CHIP SELECT INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_S =−5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} =4.75V, I_{OL} = 15 mA Memory Stores "Low"
I_{CEX}	OUTPUT LEAKAGE CURRENT		100	µA	V_{CC} =5.25V, V_{CEX} =5.25V V_S =2.5V
I_{CC}	POWER SUPPLY CURRENT		105	mA	V_{CC} =5.25V, V_A =V_S =V_D =0V
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} =5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} =5.0V

Typical Characteristics

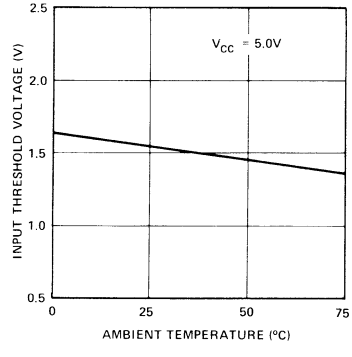
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



INPUT CURRENT VS. INPUT VOLTAGE



INPUT THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE



Switching Characteristics

Conditions of Test:

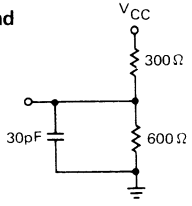
Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

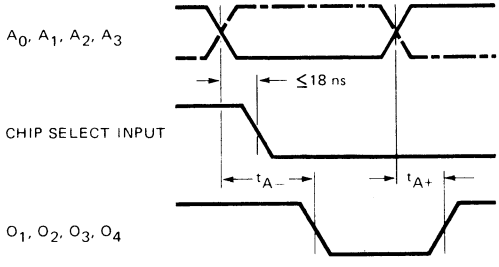
Output loading is 15mA and 30 pF

15 mA Test Load

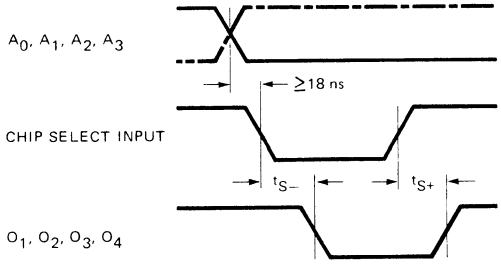


READ CYCLE

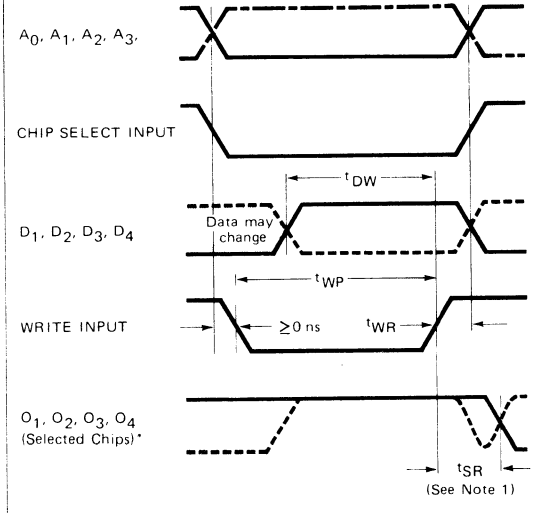
Address to Output Delay



Chip Select to Output Delay



WRITE CYCLE



*Outputs of unselected chips remain high during write cycle.

NOTE 1: t_{SR} is associated with a read cycle following a write cycle and does not affect the access time.

A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

READ CYCLE					
SYMBOL	PARAMETER	3101A LIMITS (ns) MIN.	3101A LIMITS (ns) MAX.	3101 LIMITS (ns) MIN.	3101 LIMITS (ns) MAX.
t_{S+}, t_{S-}	Chip Select to Output Delay	5	17	5	42
t_{A-}, t_{A+}	Address to Output Delay	10	35	10	60

WRITE CYCLE					
SYMBOL	TEST	3101A LIMITS (ns) MIN.	3101A LIMITS (ns) MAX.	3101 LIMITS (ns) MIN.	3101 LIMITS (ns) MAX.
t_{SR}	Sense Amplifier Recovery Time		35		50
t_{WP}	Write Pulse Width	25		40	
t_{DW}	Data-Write Overlap Time	25		40	
t_{WR}	Write Recovery Time	0		5	

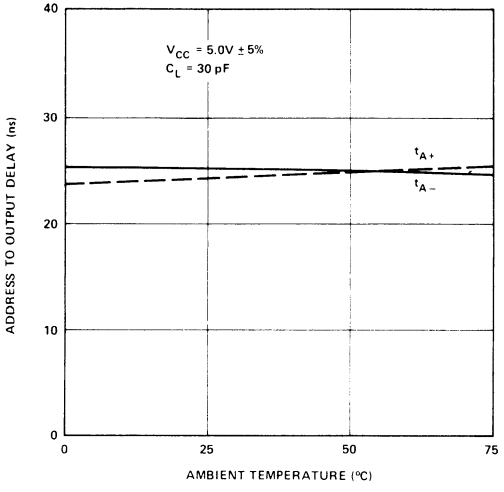
CAPACITANCE(2) T_A = 25° C

C_{IN}	INPUT CAPACITANCE (All Pins)	10 pF maximum
C_{OUT}	OUTPUT CAPACITANCE	12 pF maximum

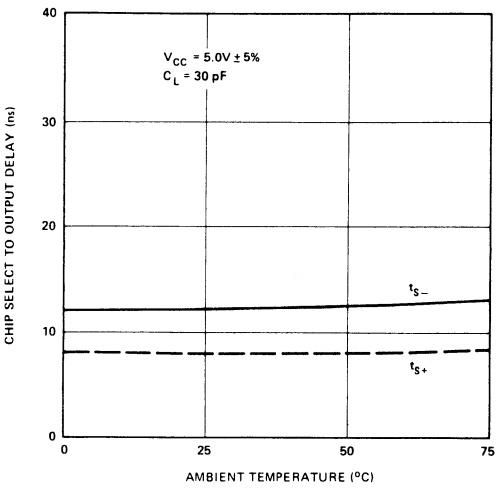
NOTE 2: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and T_A = 25°C.

Typical A.C. Characteristics

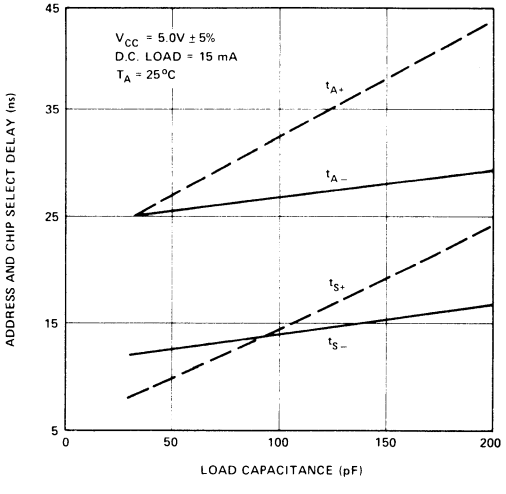
ADDRESS TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



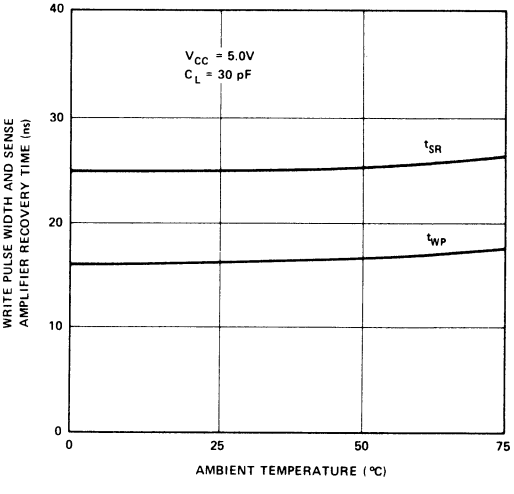
CHIP SELECT TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



ADDRESS & CHIP SELECT TO OUTPUT DELAY
VS.
LOAD CAPACITANCE



WRITE PULSE WIDTH & SENSE
AMPLIFIER RECOVERY TIME
VS. AMBIENT TEMPERATURE

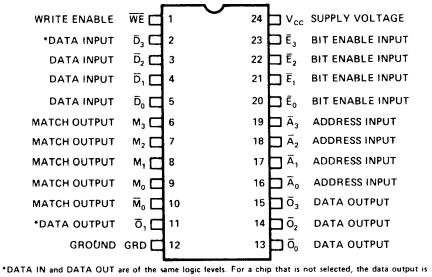


16 BIT CONTENT ADDRESSABLE MEMORY

- **Organization – 4 Words x 4 Bits**
- **Max. Delay of 30 nsec Over 0° C to 75° C Temperature**
- **Open Collector Outputs – OR Tie Capability**
- **High Current Sinking Capability – 15 mA max.**
- **Low Input Load Current – 0.25 mA max.**
- **DTL & TTL Compatible**
- **Bit Enable Input – Bit Masking**
- **Standard 24 Pin Dual In-Line**

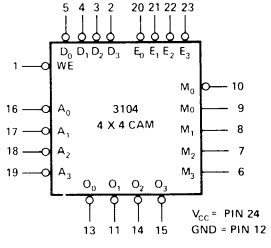
The Intel®3104 is a high speed 16 bit Content Addressable Memory (CAM). It is a linear select 4 word by 4 bit array which is designed to compare data on its inputs with data already stored in its memory and to indicate a match when these data are identical. This equality search is performed on all bits in parallel. The 3104 can also be used as a read/write RAM with linear selection addressing.

PIN CONFIGURATION

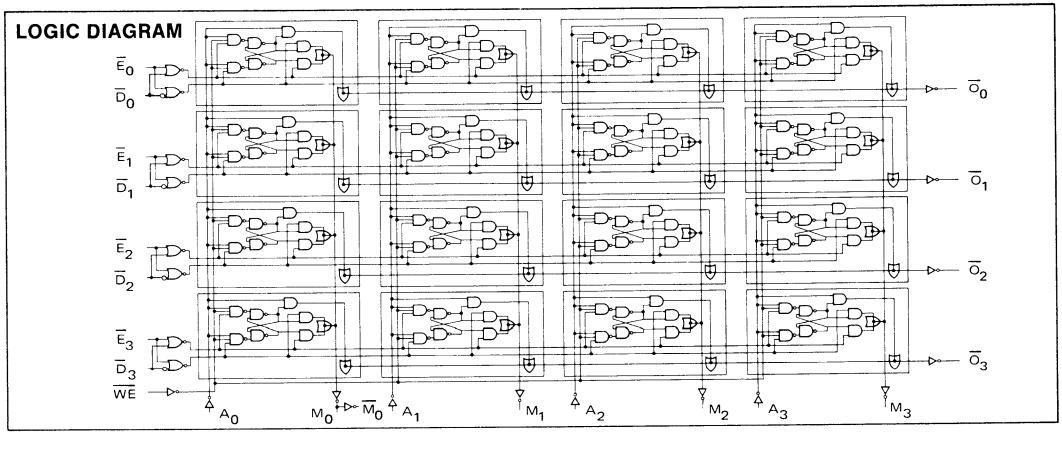


*DATA IN and DATA OUT are of the same logic levels. For a chip that is not selected, the data output is at a high level.

LOGIC SYMBOL



LOGIC DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	−65°C to +125°C
Storage Temperature	−65°C to +160°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

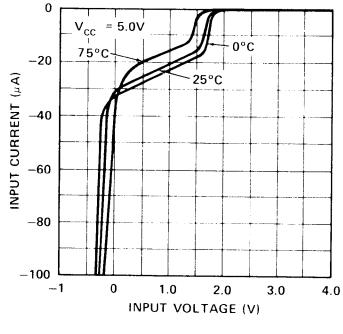
D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT			−0.25	mA	V_{CC} = 5.25V V_A = .45V
I_{FE}	BIT ENABLE INPUT LOAD CURRENT			−0.25	mA	V_{CC} = 5.25V V_E = .45V
I_{FW}	WRITE ENABLE INPUT LOAD CURRENT			−0.25	mA	V_{CC} = 5.25V V_W = .45V
I_{FD}	DATA INPUT LOAD CURRENT			−0.25	mA	V_{CC} = 5.25V V_D = .45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT			10	μA	V_{CC} = 5.25V V_A = 5.25V
I_{RE}	BIT ENABLE INPUT LEAKAGE CURRENT			10	μA	V_{CC} = 5.25V V_E = 5.25V
I_{RW}	WRITE ENABLE INPUT LEAKAGE CURRENT			10	μA	V_{CC} = 5.25V V_W = 5.25V
I_{RD}	DATA INPUT LEAKAGE CURRENT			10	μA	V_{CC} = 5.25V V_D = 5.25V
I_{CEX}	OUTPUT LEAKAGE CURRENT (ALL OUTPUTS)			50	μA	V_{CC} = 5.25V V_{CEX} = 5.25V
V_{OL}	OUTPUT "LOW" VOLTAGE (ALL OUTPUTS)			0.45	V	V_{CC} = 4.75V I_{OL} = 15mA
V_{IL}	INPUT "LOW" VOLTAGE (ALL INPUTS)			0.85	V	V_{CC} = 5V
V_{IH}	INPUT "HIGH" VOLTAGE (ALL INPUTS)	2.0			V	V_{CC} = 5V
I_{CC}	POWER SUPPLY CURRENT			125	mA	V_{CC} = 5.25V OUTPUTS HIGH
C_{IN}**	INPUT CAPACITANCE		5		pF	V_{IN} = +2.0V, V_{CC} = 0.0V f = 1 MHz
C_{OUT}**	OUTPUT CAPACITANCE		8		pF	V_{OUT} = +2.0V, V_{CC} = 0.0V f = 1 MHz

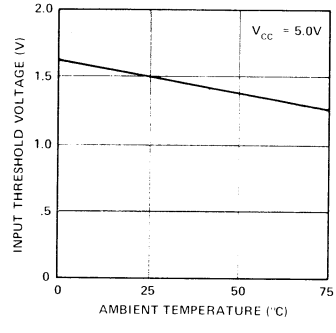
**This parameter is periodically sampled and is not 100% tested.

Typical D.C. Characteristics

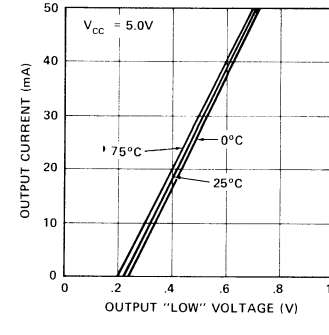
INPUT CURRENT VS. INPUT VOLTAGE



INPUT THRESHOLD VOLTAGE VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



Switching Characteristics

Conditions of Test:

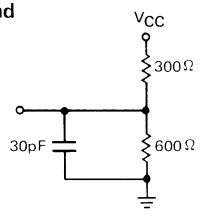
Input Pulse amplitudes · · 2.5V

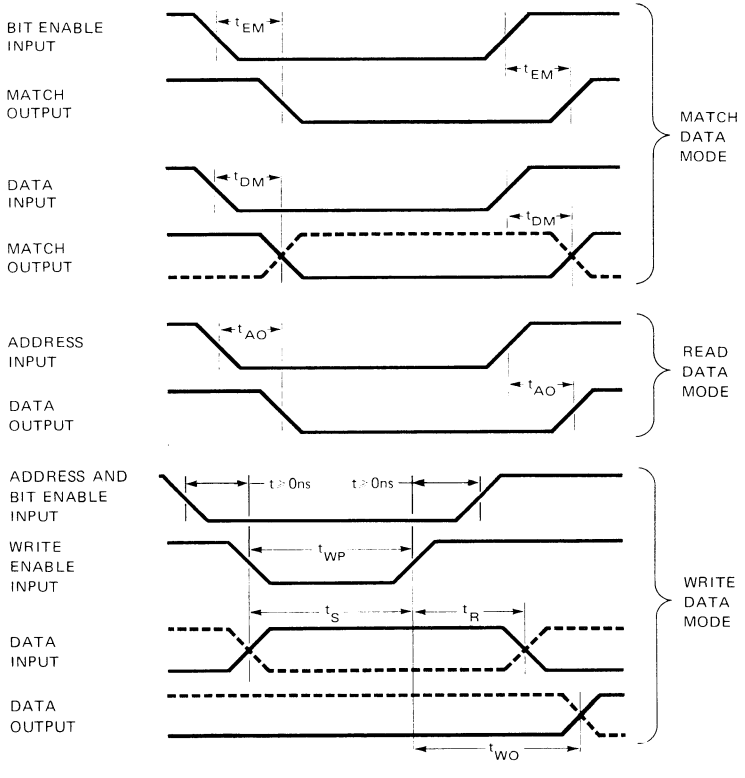
Input pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

Output loading is 15 mA and 30 pF

15mA Test Load





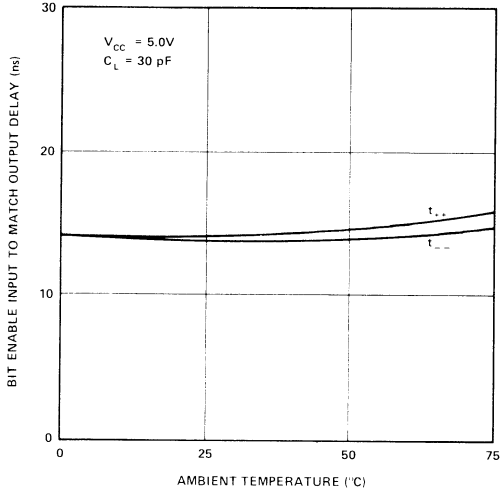
A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_{EM}	BIT ENABLE INPUT TO MATCH OUTPUT DELAY		15	30	ns
t_{DM}	DATA INPUT TO MATCH OUTPUT DELAY		16	30	ns
t_{AO}	ADDRESS INPUT TO OUTPUT DELAY		14	30	ns
t_{WP}	WRITE ENABLE PULSE WIDTH	40	25		ns
t_{WO}	WRITE ENABLE TO OUTPUT DELAY		–	40	ns
t_S	SET-UP TIME ON DATA INPUT		–	40	ns
t_R	RELEASE TIME ON DATA INPUT	0	–		ns

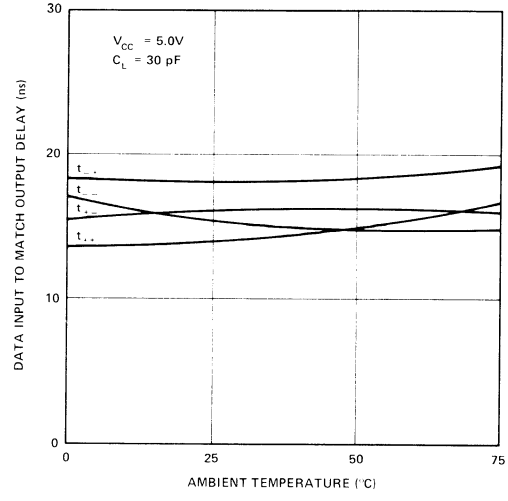
Note 1. Typical values are at nominal voltages and T_A = 25°C.

Typical A.C. Characteristics

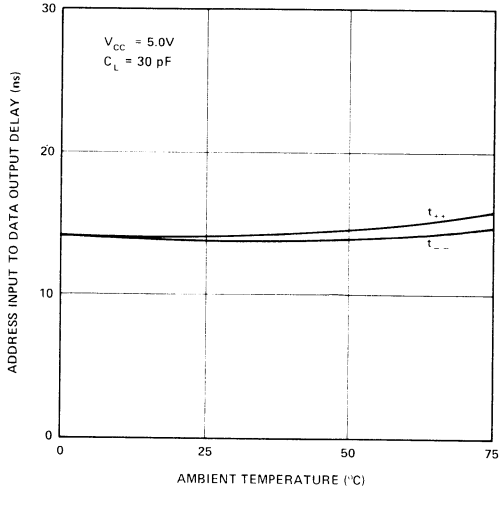
BIT ENABLE INPUT TO MATCH OUTPUT DELAY VS. TEMPERATURE



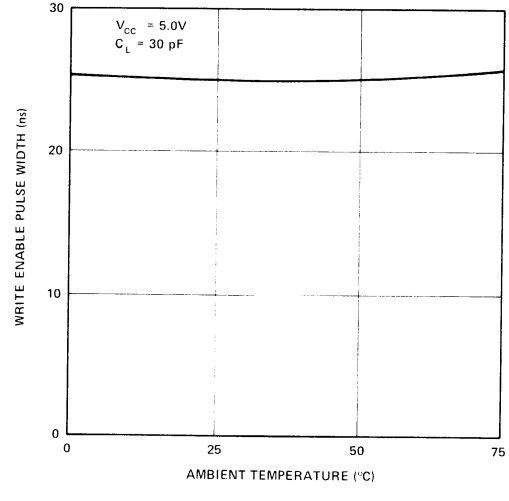
DATA INPUT TO MATCH OUTPUT DELAY VS. TEMPERATURE



ADDRESS INPUT TO DATA OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE PULSE WIDTH VS. TEMPERATURE



5101 FAMILY
256 X 4 BIT STATIC CMOS RAM

P/N	Typ. Current @ 2V (μA)	Typ. Current @ 5V (μA)	Max Access (ns)
5101L	0.14	0.2	650
5101L-1	0.14	0.2	450
5101L-3	0.70	1.0	650
5101-8	——	10.0	800

- **Single +5V Power Supply**
- **Ideal for Battery Operation (5101L)**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Three-State Output**

The Intel® 5101 is an ultra-low power 1024-bit (256 words X 4 bits) static RAM fabricated with an advanced ion-implanted silicon gate CMOS technology. The device has two chip enable inputs. Minimum standby current is drawn by this device when CE2 is at a low level. When deselected the 5101 draws from the single 5-volt supply only 10 microamps. This device is ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

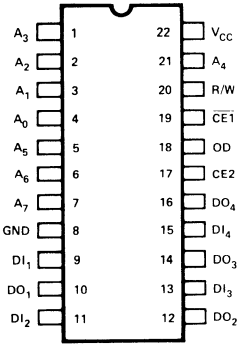
The 5101 uses fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 has separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

The 5101L has the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.

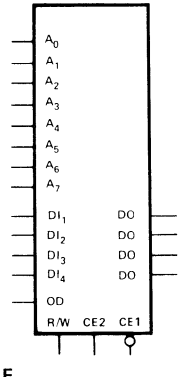
A pin compatible N-channel static RAM, the Intel® 2101A, is also available for low cost applications where a 256 X 4 organization is needed.

The Intel ion-implanted, silicon gate, Complementary MOS (CMOS) process allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION



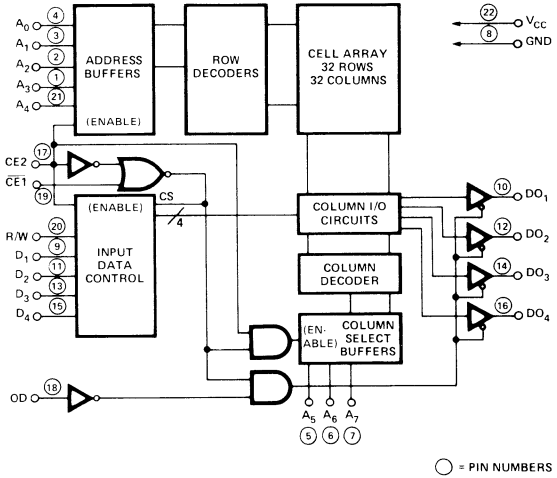
LOGIC SYMBOL



TRUTH TABLE

$\overline{CE_1}$	CE_2	OD	R/W	D_{IN}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{IN}	Write
L	H	L	H	X	D_{OUT}	Read

BLOCK DIAGRAM



Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . . .–10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . -0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	5101L and 5101L-1 Limits Min.	Typ.[1]	Max.	5101L-3 Limits Min.	Typ.[1]	Max.	5101-8 Limits Min.	Typ.[1]	Max.	Units	Test Conditions
I_{L2}[2]	Input Current		5			5			5		nA	
$\|I_{LO}\|$[2]	Output Leakage Current			1			1			2	μA	$\overline{CE1}$=2.2V, V_{OUT}= 0 to V_{CC}
I_{CC1}	Operating Current		9	22		9	22		11	25	mA	V_{IN}=V_{CC}, Except $\overline{CE1} \leqslant$ 0.65V, Outputs Open
I_{CC2}	Operating Current		13	27		13	27		15	30	mA	V_{IN}=2.2V, Except $\overline{CE1} \leqslant$ 0.65V, Outputs Open
I_{CCL}[2]	Standby Current			10			200			500	μA	CE2 ⩽ 0.2V, T_A= 70° C
V_{IL}	Input Low Voltage	-0.3		0.65	-0.3		0.65	-0.3		0.65	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4	V	I_{OL}=2.0 mA
V_{OH}	Output High Voltage	2.4			2.4			2.4			V	I_{OH}= -1.0 mA

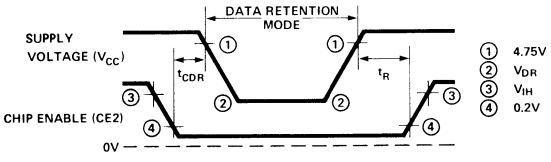
Low V_{CC} Data Retention Characteristics (For 5101L, 5101L-1 and 5101L-3) T_A = 0° C to 70° C

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	CE2 ⩽ 0.2V	
I_{CCDR1}	5101L or 5101L-1 Data Retention Current		0.14	10	μA		V_{DR}=2.0V, T_A=70° C
I_{CCDR2}	5101L-3 Data Retention Current		0.70	200	μA		V_{DR}=2.0V, T_A=70° C
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[3]			ns		

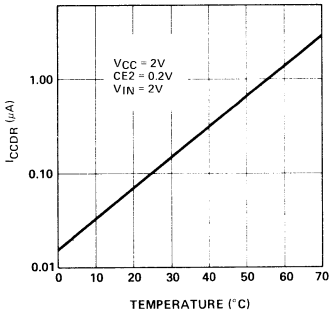
NOTES:

1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL} measurement.
3. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Typical I_{CCDR} Vs. Temperature



A.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

READ CYCLE

Symbol	Parameter	5101L-1 Limits (ns) Min.	5101L-1 Limits (ns) Max.	5101L and 5101L-3 Limits (ns) Min.	5101L and 5101L-3 Limits (ns) Max.	5101-8 Limits (ns) Min.	5101-8 Limits (ns) Max.
t_{RC}	Read Cycle	450		650		800	
t_A	Access Time		450		650		800
t_{CO1}	Chip Enable ($\overline{CE}$ 1) to Output		400		600		800
t_{CO2}	Chip Enable (CE 2) to Output		500		700		850
t_{OD}	Output Disable to Output		250		350		450
t_{DF}	Data Output to High Z State	0	130	0	150	0	200
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0		0		0	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0	

WRITE CYCLE

t_{WC}	Write Cycle	450	650	800
t_{AW}	Write Delay	130	150	200
t_{CW1}	Chip Enable ($\overline{CE}$ 1) to Write	350	550	650
t_{CW2}	Chip Enable (CE 2) to Write	350	550	650
t_{DW}	Data Setup	250	400	450
t_{DH}	Data Hold	50	100	100
t_{WP}	Write Pulse	250	400	450
t_{WR}	Write Recovery	50	50	100
t_{DS}	Output Disable Setup	130	150	200

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and C_L = 100pF

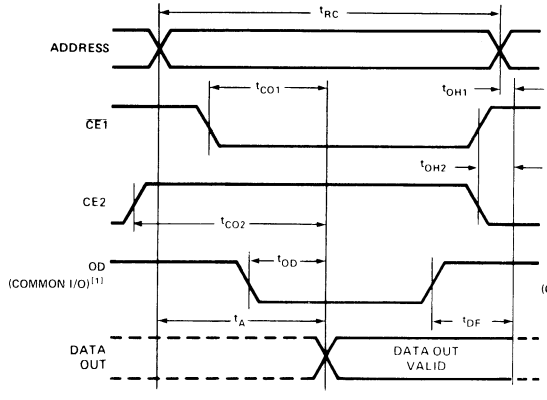
Capacitance[2] T_A = 25°C, f = 1MHz

Symbol	Test	Limits (pF) Typ.	Limits (pF) Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

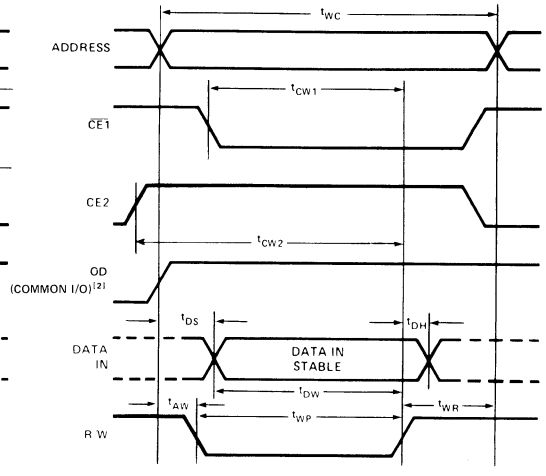
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Waveforms

READ CYCLE



WRITE CYCLE



NOTES:

1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

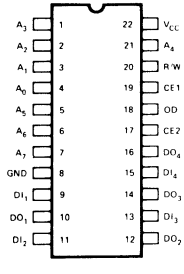
M5101-4, M5101L-4
256 x 4 BIT STATIC CMOS RAM

- **Military Temperature Range: −55°C to +125°C**
- **Ultra Low Standby Current: 200 nA/Bit**
- **Fast Access Time—800ns**
- **Single +5V Power Supply**
- **CE2 Controls Unconditional Standby Mode**
- **Three-State Output**

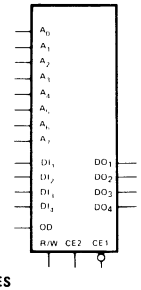
The Intel® M5101 is an ultra-low power 256 X 4 CMOS RAM specified over the −55°C to +125°C temperature range. The RAM uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. When deselected with CE2 low, the M5101 draws from the single 5-volt supply only 200 microamps at 125°C.

The Intel® M5101 is fabricated with an ion-implanted, silicon gate, Complementary MOS (CMOS) process. This technology allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION
5101



LOGIC SYMBOL
5101



PIN NAMES

DI_1, DI_4	DATA INPUT	OD	OUTPUT DISABLE
A_0 – A_7	ADDRESS INPUTS	DO_1 – DO_4	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . −65°C to 135°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . −0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics for M5101-4, M5101L-4

T_A = −55°C to 125°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}[2]	Input Current		8		nA	V_{IN} = 0 to 5.25V
I_{LOH}[2]	Output High Leakage			2	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = V_{CC}
I_{LOL}[2]	Output Low Leakage			2	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = 0.0V
I_{CC1}	Operating Current		11	25	mA	V_{IN} = V_{CC} Except $\overline{CE1}$ ≤0.01V Outputs Open
I_{CC2}	Operating Current		20	32	mA	V_{IN} = 2.2V Except $\overline{CE1}$ ≤0.5V Outputs Open
I_{CCL}[2]	Standby Current		2	200	μA	V_{IN} = 0 to V_{CC}, Except CE2 ≤ 0.2V
V_{IL}	Input "Low" Voltage	-0.3		0.5	V	
V_{IH}	Input "High" Voltage	V_{CC}-2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	V_{CC}-2.0			V	I_{OH} = 1.0mA

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in I_{CCL}.

MILITARY TEMP

RAM

Low V_{CC} Data Retention Characteristics (For M5101L-4) T_A = -55°C to 125°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	CE2 ≤ 0.2V	
I_{CCDR}	Data Retention Current		2	200	μA		V_{DR} = 2.0V
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[2]			ns		

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.
2. t_{RC} = Read Cycle Time.

A.C. Characteristics for M5101-4, M5101L-4

READ CYCLE T_A = -55°C to 125°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	800			ns	(See below)
t_A	Access Time			800	ns	
t_{CO1}	Chip Enable ($\overline{CE1}$) to Output			700	ns	
t_{CO2}	Chip Enable (CE2) to Output			850	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}	Data Output to High Z State	0		150	ns	
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0			ns	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	800			ns	(See below)
t_{AW}	Write Delay	150			ns	
t_{CW1}	Chip Enable ($\overline{CE1}$) To Write	550			ns	
t_{CW2}	Chip Enable (CE2) To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

A. C. CONDITIONS OF TEST

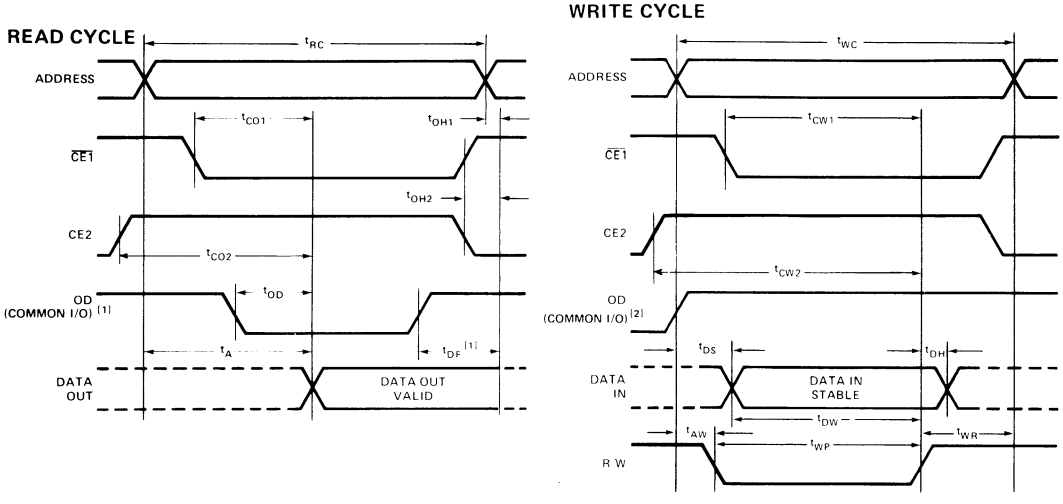
Input Pulse Levels: 0.5 Volt to V_{CC}-2.0 Volt
Input Pulse Rise and Fall Times: 20nsec
Timing Measurement Reference Level: 1.5 Volt
Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[3] T_A = 25°C, f = 1MHz

Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

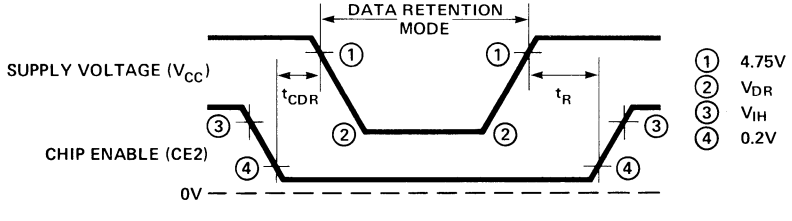
NOTE: 3. This parameter is periodically sampled and is not 100% tested.

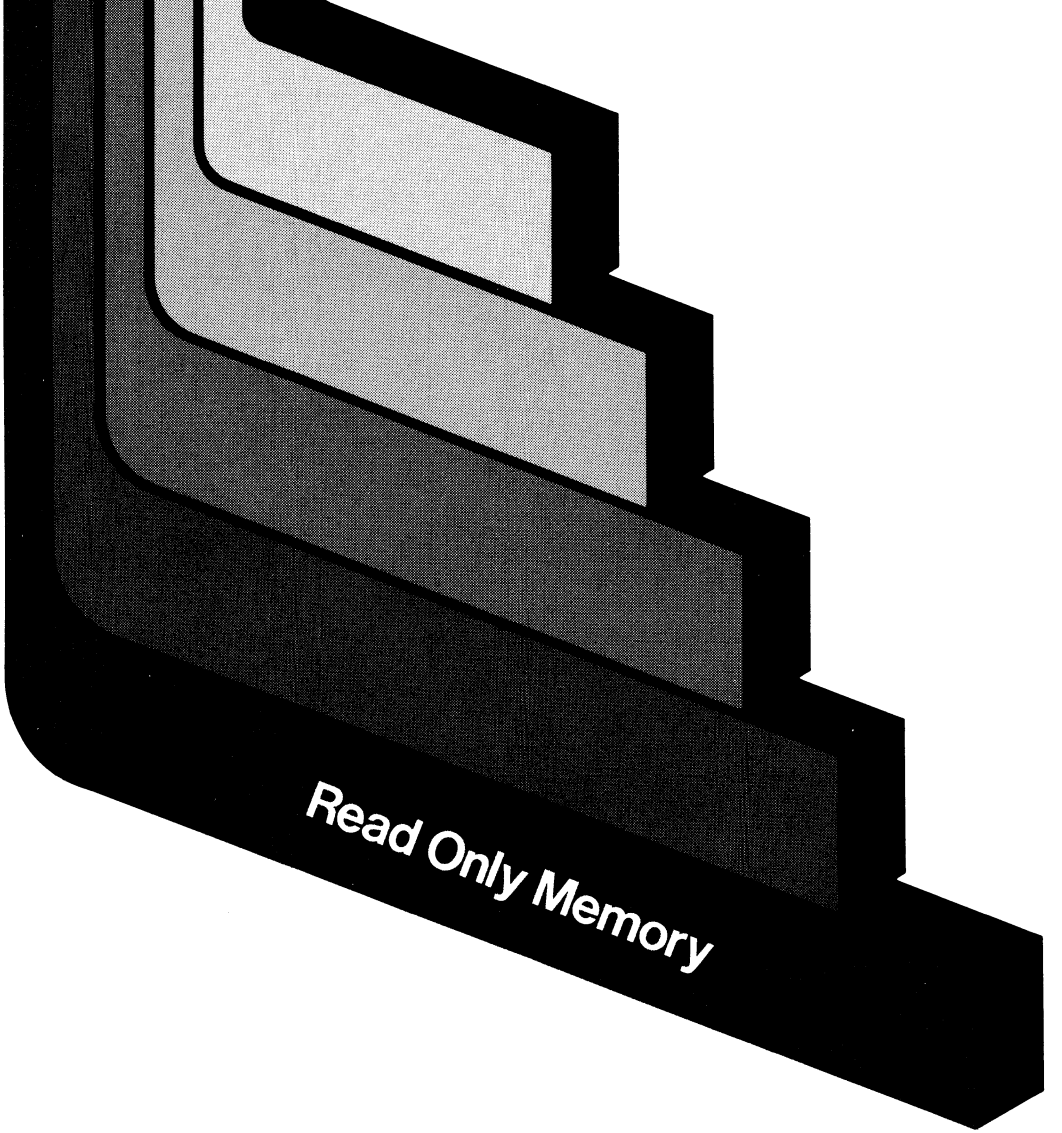
Waveforms



NOTES: 1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

Low V_{CC} Data Retention




Read Only Memory

MOS ROM AND PROM FAMILY

	Type	No. of Bits	Organization	No. of Pins	Output[1]	Maximum Access (ns)	Maximum Power Dissipation (mW)	Operating Temperature Range (°C)	Power Supply (V)	Page No.
SILICON GATE MOS ROM	**2308**	8192	1024x8	24	T.S.	450	840	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%	3-14
	2316A	16384	2048x8	24	T.S.	850	515	0 to 70	5V ± 5%	3-18
	2316E	16384	2048x8	24	T.S.	450	630	0 to 70	5V ± 10%	3-21
SILICON GATE MOS PROM	**1702A**	2048	256x8	24	T.S.	1μs	885	0 to 70	5V ± 5% -9V ± 5%	3-5
	1702A-2	2048	256x8	24	T.S.	650	959	0 to 70	5V ± 5% -9V ± 5%	
	1702A-6	2048	256x8	24	T.S.	1.5 μs	885	0 to 70	5V ± 5% -9V ± 5%	
	M1702A	2048	256x8	24	T.S.	850	960	-55 to 100	5V ± 10% -9V ± 10%	3-9
	1702AL	2048	256x8	24	T.S.	1 μs	221	0 to 70	5V ± 5% -9V ± 5%	3-11
	1702AL-2	2048	256x8	24	T.S.	650	221	0 to 70	5V ± 5% -9V ± 5%	
	2704	4096	512x8	24	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%	3-24
	2708	8192	1024x8	24	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%	3-24
	2708-1	8192	1024x8	24	T.S.	350	800	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%	
	M2708	8192	1024x8	24	T.S.	450	750	-55 to 100	5V ± 10% 12V ± 10% -5V ± 10%	3-27
	2716	16384	2048x8	24	T.S.	450	525/132[2]	0 to 70	5V ± 5%	3-30

Notes: 1. O.C. and TS are open collector and three-state output respectively.
2. The 2716 has a standby power down feature.

ROM and PROM Programming Instructions	3-55

BIPOLAR PROM FAMILY

Type	No. of Bits	Organization	No. of Pins	Output[1]	Maximum Access (ns)	Maximum Power Dissipation (mW)	Operating Temperature Range (°C)	Power Supply (V)	Page No.
3601	1024	256x4	16	O.C.	70	685	0 to 75	5V ±5%	3-34
3601-1	1024	256x4	16	O.C.	50	685	0 to 75	5V ± 5%	
3621	1024	256x4	16	T.S.	70	685	0 to 75	5V ± 5%	
3621-1	1024	256x4	16	T.S.	50	685	0 to 75	5V ± 5%	
M3601	1024	256x4	16	O.C.	90	685	-55 to 125	5V ± 5%	3-38
3602A	2048	512x4	16	O.C.	70	735	0 to 75	5V ± 5%	3-40
3602A-2	2048	512x4	16	O.C.	60	735	0 to 75	5V ± 5%	
3602	2048	512x4	16	O.C.	70	735	0 to 75	5V ± 5%	
3622A	2048	512x4	16	T.S.	70	735	0 to 75	5V ± 5%	
3622A-2	2048	512x4	16	T.S.	60	735	0 to 75	5V ± 5%	
3622	2048	512x4	16	T.S.	70	735	0 to 75	5V ± 5%	
3604A	4096	512x8	24	O.C.	70	998	0 to 75	5V ± 5%	3-43
3604A-2	4096	512x8	24	O.C.	60	998	0 to 75	5V ± 5%	
3604AL	4096	512x8	24	O.C.	90	630/105[2]	0 to 75	5V ± 5%	
3604	4096	512x8	24	O.C.	70	998	0 to 75	5V ± 5%	
3604-4	4096	512x8	24	O.C.	90	998	0 to 75	5V ± 5%	
3604L-6	4096	512x8	24	O.C.	90	735/240[2]	0 to 75	5V ± 5%	
3624A	4096	512x8	24	T.S.	70	998	0 to 75	5V ± 5%	
3624A-2	4096	512x8	24	T.S.	60	998	0 to 75	5V ± 5%	
3624	4096	512x8	24	T.S.	70	998	0 to 75	5V ± 5%	
3624-4	4096	512x8	24	T.S.	90	998	0 to 75	5V ± 5%	
M3604	4096	512x8	24	O.C.	90	1045	-55 to 125	5V ± 10%	3-46
M3624	4096	512x8	24	T.S.	90	1045	-55 to 125	5V ± 10%	
3605	4096	1024x4	18	O.C.	70	787	0 to 75	5V ± 5%	3-48
3605-2	4096	1024x4	18	O.C.	60	787	0 to 75	5V ± 5%	
3625	4096	1024x4	18	T.S.	70	787	0 to 75	5V ± 5%	
3625-2	4096	1024x4	18	T.S.	60	787	0 to 75	5V ± 5%	
3608	8192	1024x8	24	O.C.	80	998	0 to 75	5V ± 5%	3-51
3608-4	8192	1024x8	24	O.C.	100	998	0 to 75	5V ± 5%	
3628	8192	1024x8	24	O.C.	80	998	0 to 75	5V ± 5%	
3628-4	8192	1024x8	24	O.C.	100	998	0 to 75	5V ± 5%	

Notes: 1. O.C. and T.S. are open collector and three-state output respectively.
2. The 3604AL and 3604L-6 have a low power dissipation feature.

BIPOLAR PROM CROSS REFERENCE

Part Number	Prefix and Manufacturer	Organization	Intel Part Number	
			Direct Replacement	For New Designs[1]
1024-4	HPROM—Harris	256 x 4	3621	
1024A-2	HPROM—Harris	256 x 4	M3601	
1024A-5	HRPOM—Harris	256 x 4	3601	
27S10C	AMD	256 x 4	3601	
27S10M	AMD	256 x 4	M3601	
27S11C	AMD	256 x 4	3621	
27S11M	AMD	256 x 4	M3621	
5300-1	MMI	256 x 4	M3601	
5340-1	MMI	512 x 8	M3604	
5341-1	MMI	512 x 8	M3624	
54S387	SN—TI	256 x 4	M3601	
54S387	DM—National	256 x 4	M3601	
5603AC	IM—Intersil	256 x 4	3601	
5603AM	IM—Intersil	256 x 4	M3601	
5604C	IM—Intersil	512 x 4	3602A	
5605C	IM—Intersil	512 x 8	3604A	
5623C	IM—Intersil	256 x 4	3621	
5624C	IM—Intersil	512 x 4	3622A	
5625C	IM—Intersil	512 x 8	3624A	
6300-1	MMI	256 x 4	3601-1	
6301-1	MMI	256 x 4	3621-1	
6305-1	MMI	512 x 4	3602A-2	
6306-1	MMI	512 x 4	3622A-2	
6340-1	MMI	512 x 8	3604A	
6341-1	MMI	512 x 8	3624A	
6352-1	MMI	1024 x 4	3605-2	
6353-1	MMI	1024 x 4	3625-2	
6380-1	MMI	1024 x 8	3608	
6381-1	MMI	1024 x 8	3628	
74S287	SN—TI	256 x 4	3621-1	
74S287	DM—National	256 x 4	3621-1	
74S387	SN—TI	256 x 4	3601-1	
74S387	DM—National	256 x 4	3601-1	
74S472	TI	512 x 8		3624
74S473	TI	512 x 8		3604
74S474	TI	512 x 8	3624A	
74S475	TI	512 x 8	3604A	
74S570	National	512 x 4	3602A	
74S571	National	512 x 4	3622A	
7573	DM—National	256 x 4	M3601	
7610-2	HM—Harris	256 x 4		M3601
7610-5	HM—Harris	256 x 4	3601-1	
7611-5	HM—Harris	256 x 4	3621-1	
7620-5	HM—Harris	512 x 4	3602A	
7621-5	HM—Harris	512 x 4	3622A	
7640-2	HM—Harris	512 x 8		M3604
7640-5	HM—Harris	512 x 8	3604A	
7641-2	HM—Harris	512 x 8		M3624
7641-5	HM—Harris	512 x 8	3624A	
7642-5	HM—Harris	1024 x 4	3605	
7643-5	HM—Harris	1024 x 4	3625	
7644-5	HM—Harris	1024 x 4		3625

Part Number	Prefix and Manufacturer	Organization	Intel Part Number	
			Direct Replacement	For New Designs[1]
82S115	N—Signetics	512 x 8		3624
82S115	S—Signetics	512 x 8		M3624
82S126	N—Signetics	256 x 4	3601-1	
82S126	S—Signetics	256 x 4		M3601
82S129	N—Signetics	256 x 4	3621-1	
82S130	N—Signetics	512 x 4		3602
82S131	N—Signetics	512 x 4		3622
82S140	N—Signetics	512 x 8	3604A	
82S141	N—Signetics	512 x 8	3624A	
82S136	N—Signetics	1024 x 4	3605-2	
82S137	N—Signetics	1024 x 4	3625-2	
82S180	N—Signetics	1024 x 8		3608
82S181	N—Signetics	1024 x 8		3628
82S184	N—Signetics	2048 x 4		3608
82S185	N—Signetics	2048 x 4		3628
8573	DM—National	256 x 4	3601	
8574	DM—National	256 x 4	3621	
87S295	National	512 x 8	3604A	
87S296	National	512 x 8	3624A	
93416C	Fairchild	256 x 4	3601	
93416M	Fairchild	256 x 4		M3601
93426C	Fairchild	256 x 4	3621	
93436C	Fairchild	512 x 4		3602
93438C	Fairchild	512 x 8		3604
93438M	Fairchild	512 x 8		M3604
93446C	Fairchild	512 x 4		3622
93448C	Fairchild	512 x 8		3624
93448M	Fairchild	512 x 8		M3624
93452C	Fairchild	1024 x 4	3605-2	
93453C	Fairchild	1024 x 4	3625-2	

NOTE: 1. The Intel® PROMs have the same pin configuration and differ only in access time from the PROMs in the first column. The exceptions are the 6350, 6351 82S115, and 82S184/85 which have different pin configurations.

1702A

2K (256 x 8) UV ERASABLE PROM

1702A-2	0.65 us Max.
1702A	1.0 us Max.
1702A-6	1.5 us Max.

PROM/ROM

- **Fast Access Time: Max. 650 ns (1702A-2)**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Static MOS: No Clocks Required**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

The 1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The 1702A undergoes complete programming and functional testing prior to shipment, thus insuring 100% programmability.

Initially all 2048 bits of the 1702A are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702A to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

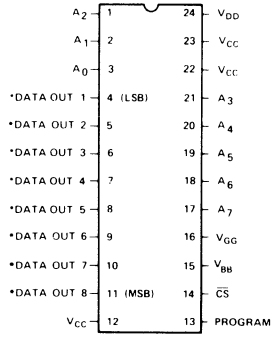
The circuitry of the 1702A is completely static. No clocks are required. Access times from 650ns to 1.5μs are available. A 1702AL family is available (see 1702AL data sheets for specifications) for those systems requiring lower power dissipation than the 1702A.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is also available for large volume production runs of systems initially using the 1702A.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

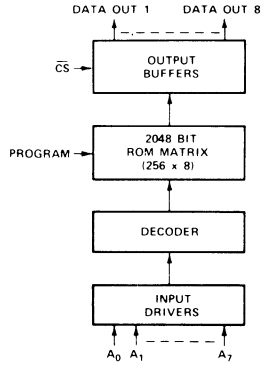


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702A differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the ROM and PROM Programming instructions section, page 3-55.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5%, V_{GG} = -9V ±5%, unless otherwise noted.

READ OPERATION

Symbol	Test	1702A, 1702A-6 Limits Min.	Typ.[1]	Max.	1702A-2 Limits Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{IH2}
I_{DD1}[1]	Power Supply Current		35	50		40	60	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		37	55	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		43	65	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		7	13	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		6	12	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH1}	Addr. Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
V_{IH2}	Chip Sel. Input High Volt.	V_{CC}-2		V_{CC}+0.3	V_{CC}-1.5		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

Note 1: Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0° C to +70° C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

Symbol	Test	1702A Limits Min.	1702A Limits Max.	1702A-2 Limits Min.	1702A-2 Limits Max.	1702A-6 Limits Min.	1702A-6 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6		0.66	MHz
t_{OH}	Previous Read Data Valid		0.1		0.1		0.1	μs
t_{ACC}	Address to Output Delay		1		0.65		1.5	μs
t_{CS}	Chip Select Delay		0.1		0.3		0.6	μs
t_{CO}	Output Delay From $\overline{CS}$		0.9		0.35		0.9	μs
t_{OD}	Output Deselect		0.3		0.3		0.3	μs

Capacitance * T_A = 25°C

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$ — All unused pins
C_{OUT}	Output Capacitance	10	15	pF	$V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — are at A.C. ground

*This parameter is periodically sampled and is not 100% tested.

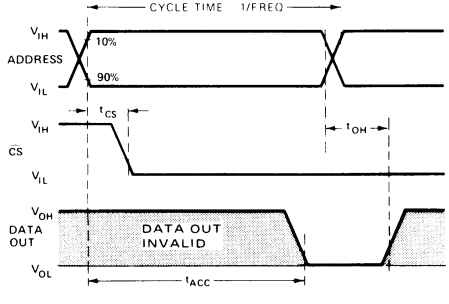
Switching Characteristics

Conditions of Test:

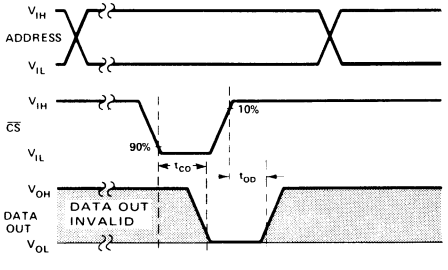
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L=15pF

A) READ OPERATION

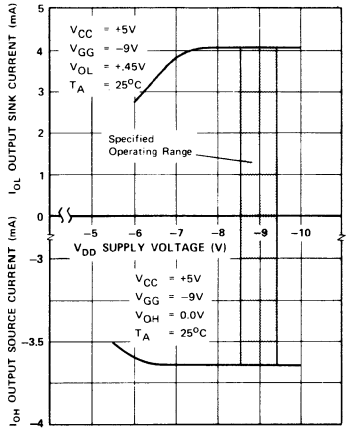


B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION

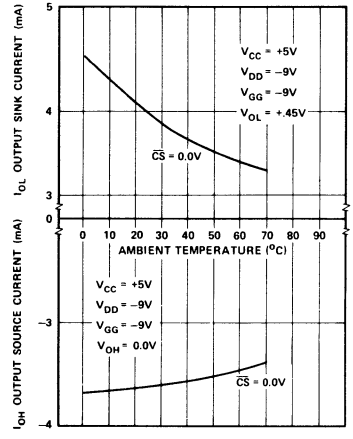


Typical Characteristics

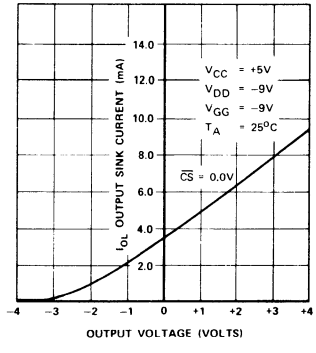
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



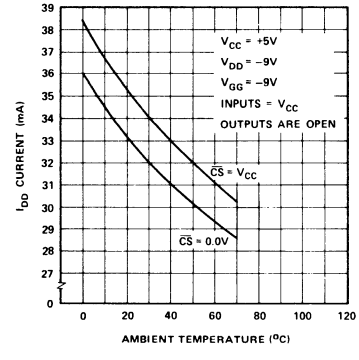
OUTPUT CURRENT VS. TEMPERATURE



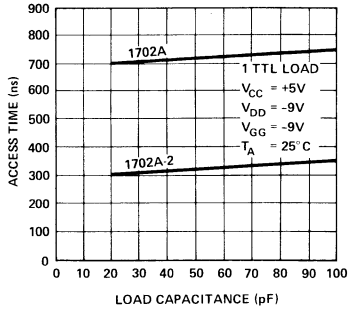
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



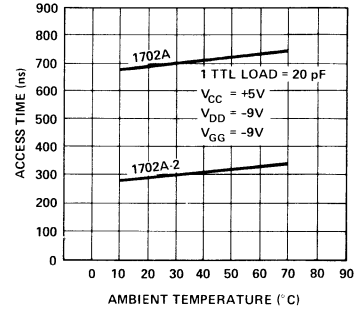
I_{DD} CURRENT VS. TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE



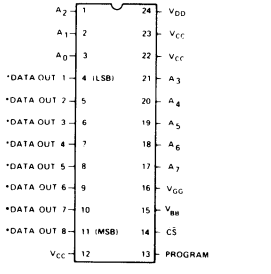
M1702A 2K (256 × 8) UV ERASABLE PROM

−55°C to +100°C OPERATION

- **Fast Access Time: Max. 850 ns**
- **Completely Static**
- **Inputs and Outputs DTL and TTL Compatible**
- **All 2048 Bits Factory Tested Prior to Shipment**
- **Three-State Output**
- **24 Pin Dip**

The Intel® M1702A is a 256-word by 8-bit ultraviolet light erasable and electrically reprogrammable EPROM which is specified over the −55°C to +100°C temperature range. The M1702A has a transparent lid which allows the user to expose the M1702A to UV light to erase the bit pattern. A new pattern can then be written into the device.

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

*REFER TO THE 1702A DATA SHEET FOR PIN CONNECTIONS DURING READ AND PROGRAM

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . −65°C to 110°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

READ OPERATION

T_A = −55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = −9V ±10%, V_{GG} = −9V ±10% unless otherwise noted.

Symbol	Test	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			10	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{IH2}
I_{DD1}[1]	Power Supply Current		35	50	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	65	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = −55°C, Continuous
I_{CF}	Output Clamp Current		8	11	mA	V_{OUT} = −1.0V, T_A = −55°C, Continuous
I_{GG}	Gate Supply Current			10	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V	
V_{IH1}	Address Input High Voltage	V_{CC}-2		V_{CC}+0.3	V	
V_{IH2}	Chip Select Input High Voltage	V_{CC}-1.5		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −200μA

Note 1. Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = -55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = -9V ±10%, V_{GG} = -9V ±10% unless otherwise noted.

Symbol	Test	Limits Min.	Limits Max.	Unit
Freq.	Repetition Rate		1.2	MHz
t_{OH}	Previous Read Data Valid		0.1	μs
t_{ACC}	Address to Output Delay		0.85	μs
t_{CS}	Chip Select Delay		0.5	μs
t_{CO}	Output Delay From $\overline{CS}$		0.35	μs
t_{OD}	Output Deselect		0.3	μs

Capacitance * T_A = 25°C

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	$V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground

*This parameter is sampled and is not 100% tested.

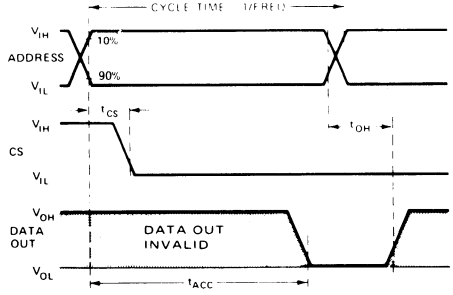
Switching Characteristics

Conditions of Test:

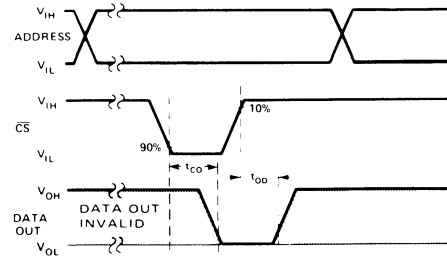
Input pulse amplitudes: 0 to 4V; t_R, $t_F \leq 50$ ns

Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leq 15$ ns), $C_L = 15$pF

A) READ OPERATION



B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION



ERASING AND PROGRAMMING PROCEDURE

The erasing and programming procedure of the M1702A is the same as the 0°C to 70°C 1702A. The procedure is discussed in Section III, page 3-55, of the data catalog.

1702AL, 1702AL2

2K (256 x 8) UV ERASABLE LOW POWER PROM

Part No.	MAXIMUM ACCESS (μs)	t_{DVGG} (μs)
1702AL	1.0	0.4
1702AL-2	0.65	0.3

- **Clocked V_{GG} Mode for Low Power Dissipation**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

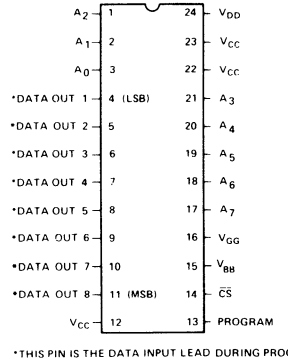
The 1702AL is a 256 word by 8 bit electrically programmable ROM and is the same chip as the industry standard 1702A. The programming and erasing specifications are identical to the 1702A. The 1702AL operates with the V_{GG} clocked to reduce the power dissipation.

Initially all 2048 bits of the 1702AL are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702AL is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702AL to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The 1702AL is fabricated with silicon gate technology. This low threshold technology allows the design and production of high performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

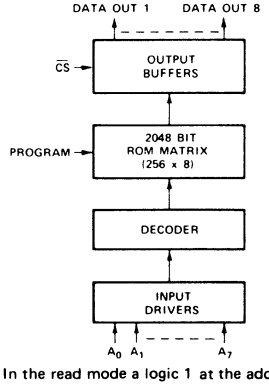


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702AL differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the ROM and PROM Programming Instructions section, pages 3-55.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 (CS)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	Clocked V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

READ OPERATION

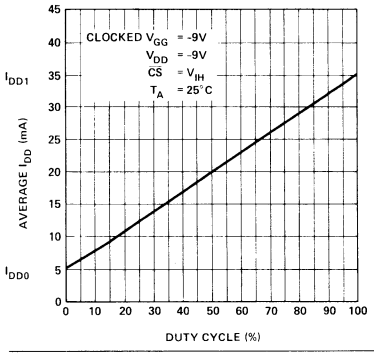
T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5%, V_{GG}[1] = -9V ±5%, unless otherwise noted.

Symbol	Test	1702AL Limits Min.	Typ.[2]	Max.	1702AL-2 Limits Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC}-2
I_{DDO1}[1]	Power Supply Current		7	10		7	10	mA	T_A=25°C $\overline{CS}$=V_{IH}, V_{GG}=V_{CC},
I_{DDO2}	Power Supply Current			15			15	mA	T_A=0°C I_{OL}=0.0mA
I_{DD1}[1]	Power Supply Current		35	50		35	50	mA	$\overline{CS}$ = V_{CC} -2, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		32	46	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		38	60	mA	$\overline{CS}$ = V_{CC} -2, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		5.5	8	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		5	7	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

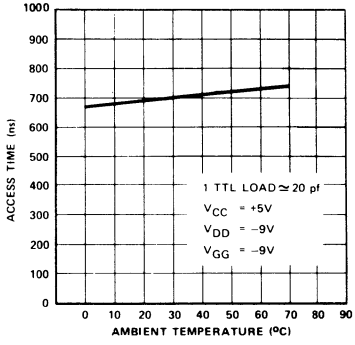
NOTES: 1. The 1702AL is operated with the V_{GG} clocked to obtain low power dissipation. The average I_{DD} will vary between I_{DDO} and I_{DD1} (at 25°C) depending on the V_{GG} duty cycle (see curve opposite). 2. Typical values are at nominal voltage and T_A = 25°C.

Typical Characteristics

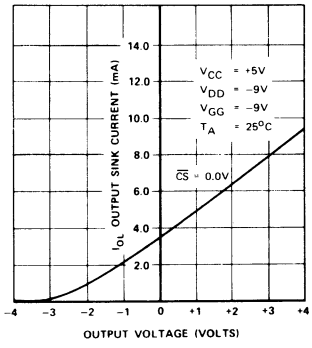
AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



ACCESS TIME VS. TEMPERATURE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$ unless otherwise noted

Symbol	Test	1702AL Limits Min.	1702AL Limits Max.	1702AL-2 Limits Min.	1702AL-2 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6	MHz
t_{ACC}	Address to output delay		1		0.65	μs
t_{DVGG}	Clocked V_{GG} set up	0.4		0.3		μs
t_{CS}	Chip select delay		0.1		0.3	μs
t_{CO}	Output delay from $\overline{CS}$		0.9		0.35	μs
t_{OD}	Output deselect		0.3		0.3	μs
t_{OHC}	Data out hold in clocked V_{GG} mode		5		5	μs

Capacitance $T_A = 25°C$

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Note 1)		30	pF	

*This parameter is periodically sampled and is not 100% tested.

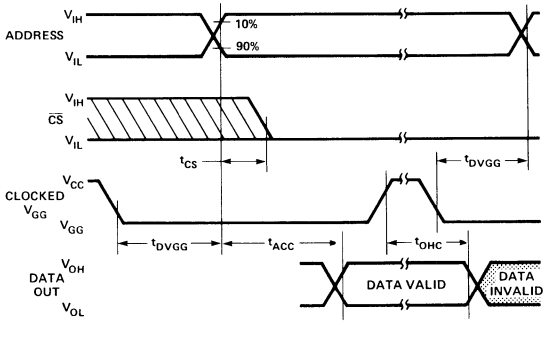
Switching Characteristics

Conditions of Test:

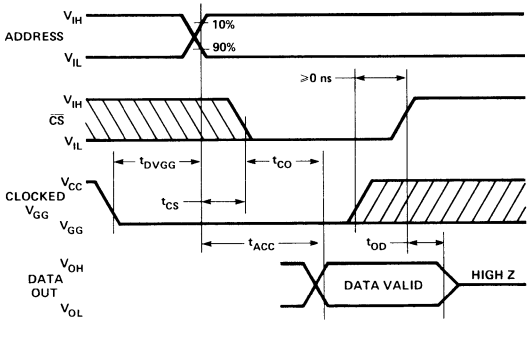
Input pulse amplitudes: 0 to 4V; t_R, $t_F \leqslant 50$ ns

Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leqslant 15$ ns), C_L = 15pF

A. READ OPERATION



B. DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION



8192 BIT STATIC MOS READ ONLY MEMORY

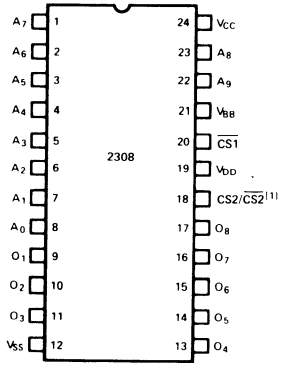
- **Fast Access Time: 450 ns**
- **Standard Power Supplies: +12V, ±5V**
- **TTL Compatible: All Inputs and Outputs**
- **Programmable Chip Select Input for Easy Memory Expansion**
- **Three-State Output: OR-Tie Capability**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Pin Compatible to 2708 PROM**

The Intel 2308 is a 8192 bit static MOS read only memory organized as 1024 words by 8-bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

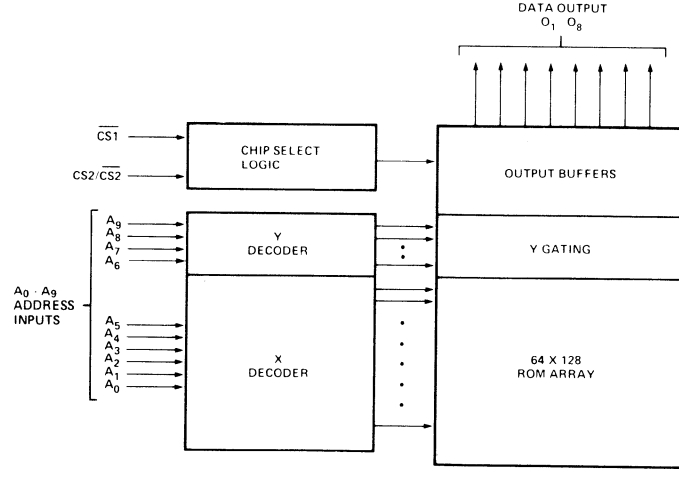
The inputs and outputs are TTL compatible. The chip select input (CS2/$\overline{CS2}$) is programmable. An active high or low level chip select input can be defined by the designer and the desired chip select logic level is fixed at Intel during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion. The pin compatible UV erasable 2708 PROM is available for initial system prototyping.

The 2308 read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS_1}$	CHIP SELECT INPUT
CS2/$\overline{CS2}$[1]	PROGRAMMABLE CHIP SELECT INPUT

NOTE 1. The CS2/$\overline{CS2}$ LOGIC LEVELS MUST BE SPECIFIED BY THE USER AS EITHER A LOGIC 1 (V_{IH}) OR LOGIC 0 (V_{IL}). A LOGIC 0 SHOULD BE SPECIFIED IN ORDER TO BE COMPATIBLE WITH THE 2708.

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect
To V_{BB} . . . . . -0.3V to 20V
Power Dissipation . . . . . 1.0 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

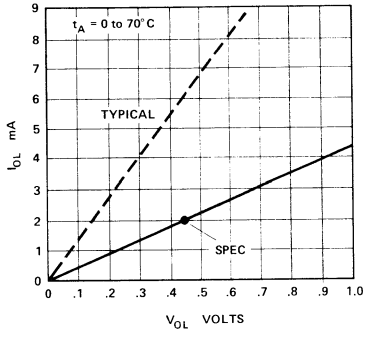
D.C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%; V_{DD} = 12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V Unless Otherwise Specified.

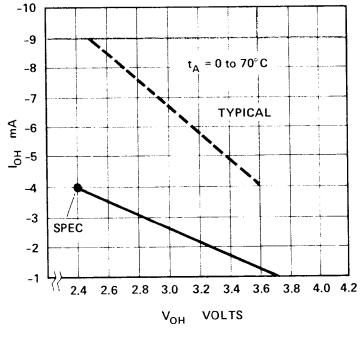
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins Except $\overline{CS}_1$)		1	10	μA	V_{IN} = 0 to 5.25V
I_{LCL}	Input Load Current on $\overline{CS}_1$			1.6	mA	V_{IN} = 0.45V
I_{LPC}	Input Peak Load Current on $\overline{CS}_1$			4	mA	0.8V ≤ V_{IN} < 3.3V
I_{LKC}	Input Leakage Current on $\overline{CS}_1$			10	μA	V_{IN} = 3.3V to 5.25V
I_{LO}	Output Leakage Current			10	μA	Chip Deselected
V_{IL}	Input "Low" Voltage	V_{SS}-1		0.8V	V	
V_{IH}	Input "High" Voltage	3.3		V_{CC}+1.0	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2mA
V_{OH1}	Output "High" Voltage	2.4			V	I_{OH} = -4mA
V_{OH2}	Output "High" Voltage	3.7			V	I_{OH} = -1mA
I_{CC}	Power Supply Current V_{CC}		10	15	mA	
I_{DD}	Power Supply Current V_{DD}		32	60	mA	
I_{BB}	Power Supply Current V_{BB}		10μA	1	mA	
P_D	Power Dissipation		460	840	mW	

NOTE 1: Typical values for T_A = 25°C and nominal supply voltage

D.C. OUTPUT CHARACTERISTICS



D.C. OUTPUT CHARACTERISTICS



A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%; V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Specified.

Symbol	Parameter	Limits[2]		Unit
		Typ.	Max.	
t_{ACC}	Address to Output Delay Time	200	450	ns
t_{CO1}	Chip Select 1 to Output Delay Time	85	160	ns
t_{CO2}	Chip Select 2 to Output Delay Time	125	220	ns
t_{DF}	Chip Deselect to Output Data Float Time	125	220	ns

NOTE 2: Refer to conditions of Test for A.C. Characteristics. Add 50 nanoseconds (worst case) to specified values at V_{OH} = 3.7V @ I_{OH} = -1mA, C_L = 100pF.

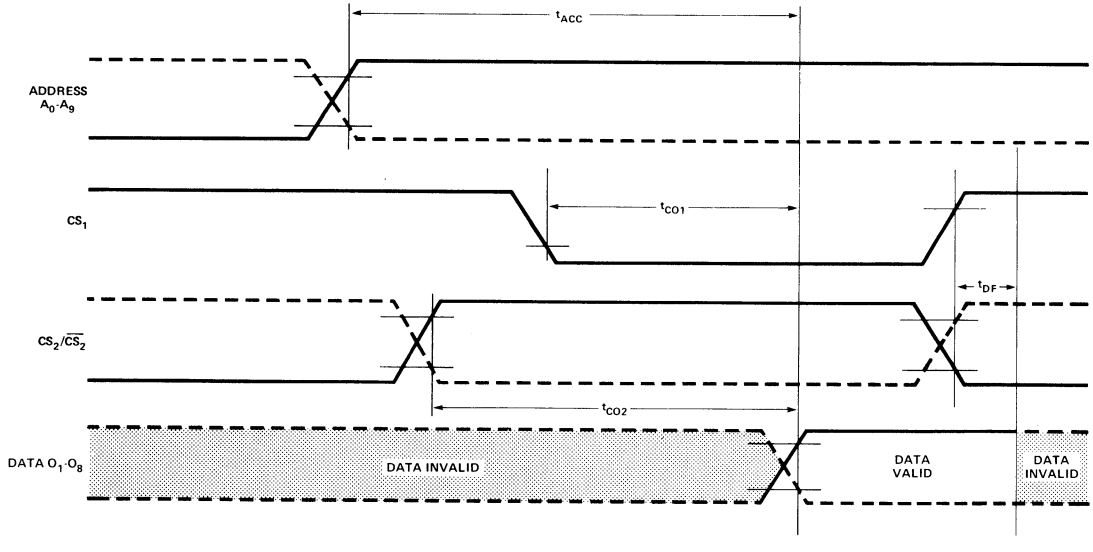
CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . . . 1 TTL Gate, and C_{LOAD} = 100pF
Input Pulse Levels . . . . . .65V to 3.3V
Input Pulse Rise and Fall Times . . . . . 20 nsec
Timing Measurement Reference Level
. . . . . 2.4V V_{IH}, V_{OH}; 0.8V V_{IL}, V_{OL}

CAPACITANCE* T_A = 25°C, f = 1 MHz, V_{BB} = -5V, V_{DD}, V_{CC} and all other pins tied to V_{SS}.

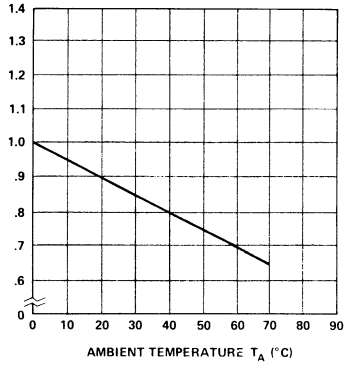
Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	Input Capacitance		6pF
C_{OUT}	Output Capacitance		12pF

*This parameter is periodically sampled and is not 100% tested.

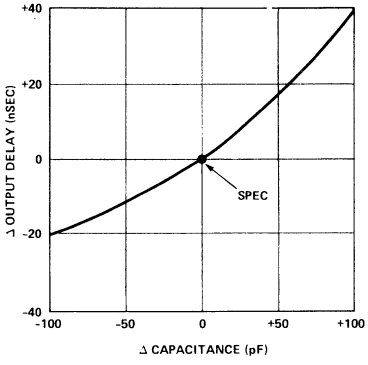


Typical Characteristics (Nominal supply voltages unless otherwise noted.)

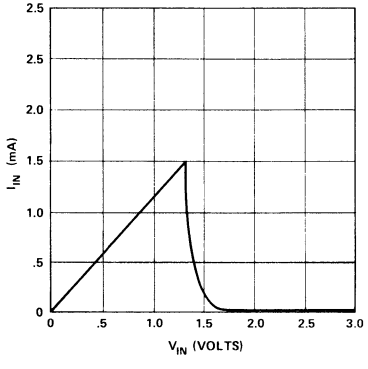
I_{DD} VS. TEMPERATURE (NORMALIZED)



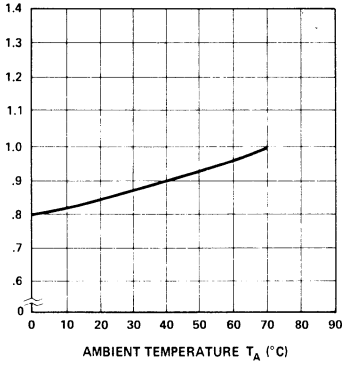
Δ OUTPUT CAPACITANCE VS. Δ OUTPUT DELAY



$\overline{CS_1}$ INPUT CHARACTERISTICS



T_{ACC} VS. TEMPERATURE (NORMALIZED)



PROM/ROM

2316A

16,384 BIT STATIC MOS READ ONLY MEMORY

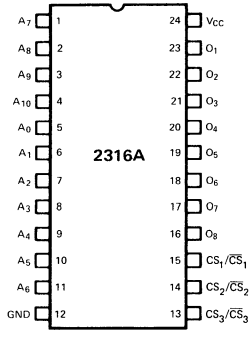
- **Single +5 Volts Power Supply Voltage**
- **Guaranteed 850ns Access Time**
- **Directly TTL Compatible—All Inputs and Outputs**
- **Three Programmable Chip Select Inputs for Easy Memory Expansion**
- **Three-State Output—OR-Tie Capability**
- **Fully Decoded—On Chip Address Decode**
- **Inputs Protected—All Inputs Have Protection Against Static Charge**

The Intel 2316A is a 16,384 bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

The 2316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

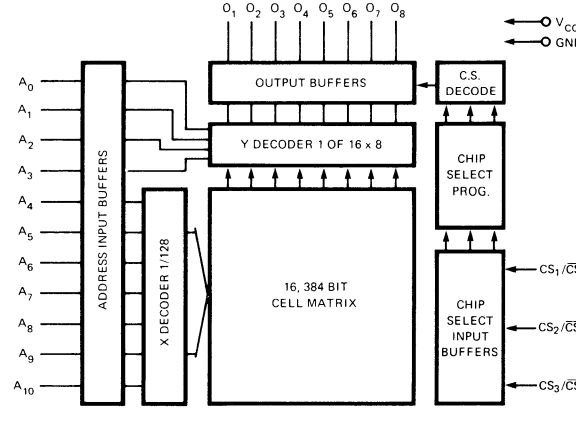
PIN CONFIGURATION



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
CS_1-CS_3	PROGRAMMABLE CHIP SELECT INPUTS

BLOCK DIAGRAM



Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect To Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1.0 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

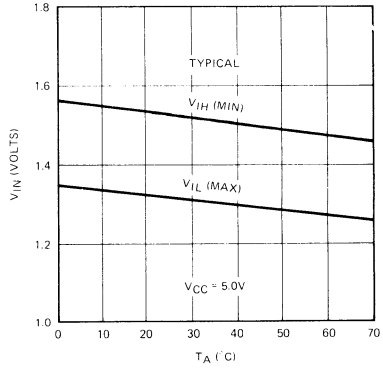
D.C. and Operating Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	μA	CS = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			-20	μA	CS = 2.2V, V_{OUT} = 0.45V
I_{CC}	Power Supply Current		40	98	mA	All inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}+1.0V	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -100 μA

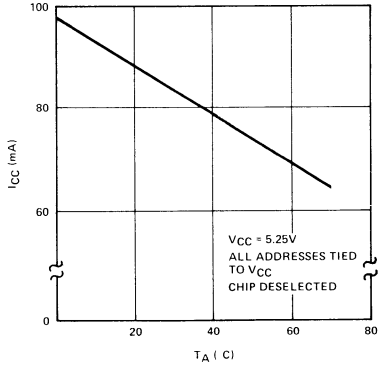
(1) Typical values for $T_A = 25°C$ and nominal supply voltage.

Typical D.C. Characteristics

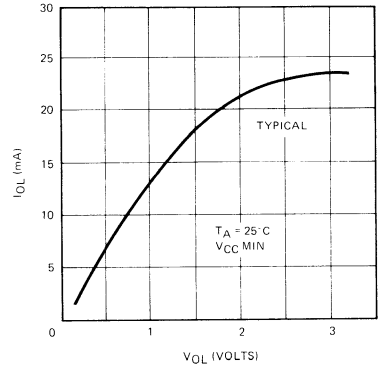
V_{IN} LIMITS VS. TEMPERATURE



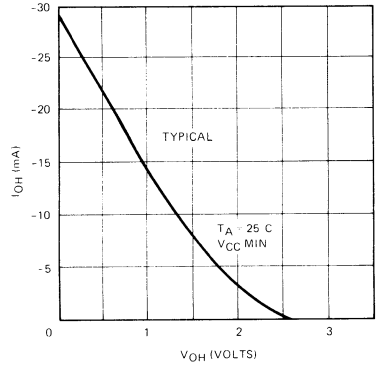
STATIC I_{CC} VS. AMBIENT TEMPERATURE WORST CASE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_A	Address to Output Delay Time		400	850	nS
t_{CO}	Chip Select to Output Enable Delay Time			300	nS
t_{DF}	Chip Deselect to Output Data Float Delay Time	0		300	nS

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

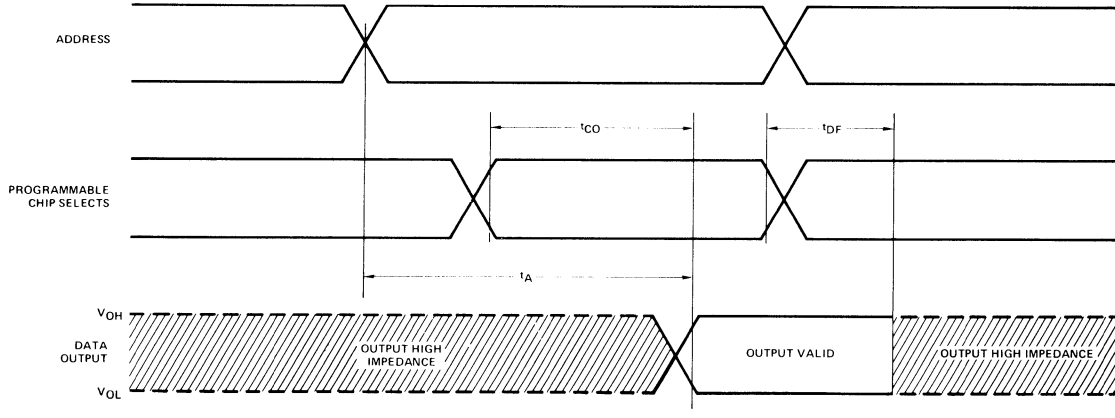
Output Load . . . 1 TTL Gate, and $C_{LOAD} = 100$ pF
Input Pulse Levels . . . . . 0.8 to 2.0V
Input Pulse Rise and Fall Times . (10% to 90%) 20 nS
Timing Measurement Reference Level
Input 1.5V
Output . . . . . 0.45V to 2.2V

CAPACITANCE(2) $T_A = 25°C$, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	4 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	8 pF	15 pF

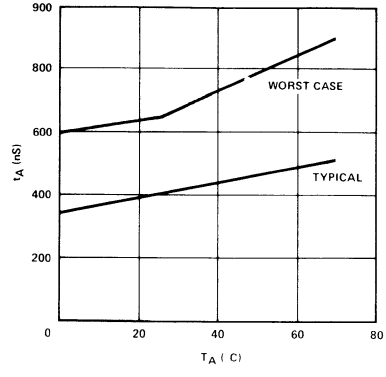
(2) This parameter is periodically sampled and is not 100% tested.

A.C. Waveforms

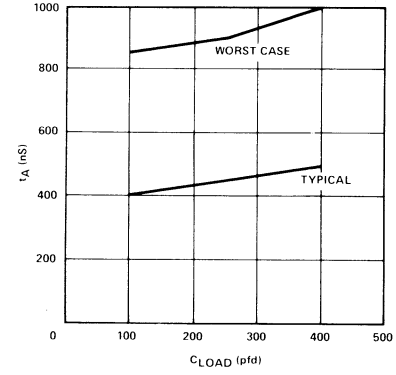


Typical A.C. Characteristics

ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



intel®

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

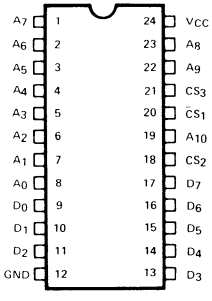
2316E
16,384 BIT STATIC ROM

- **Fast Access Time—450 ns Max.**
- **Single +5V ± 10% Power Supply**
- **Intel MCS 80 and 85 Compatible**
- **Three Programmable Chip Selects for Simple Memory Expansion and System Interface**
- **EPROM/ROM Pin Compatible for Cost-Effective System Development**
- **Completly Static Operation**
- **Inputs and Outputs TTL Compatible**
- **Three-State Output for Direct Bus Interface**

The Intel® 2316E is a 16,384-bit static, N-channel MOS read only memory (ROM) organized as 2048 words by 8 bits. Its high bit density is ideal for large, non-volatile data storage applications such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common system bus structures. The 2316E single +5V power supply and 450 ns access time are both ideal for usage with high performance microcomputers such as the Intel MCS™-80 and MCS™-85 devices.

A cost-effective system development program may be implemented by using the pin compatible Intel 2716 16K UV EPROM for prototyping and the lower cost 2316E ROM for production. The 2716 is fully compatible to the 2316E in all respects. The three 2316E programmable chip selects may be defined by the user and are fixed during the masking process. To simplify the conversion from 2716 prototyping to 2316E production, it is recommended that the 2316E programmable chip select logic levels be defined the same as that shown in the below data sheet pin configuration. This pin configuration and these chip select logic levels are the same as the 2716.

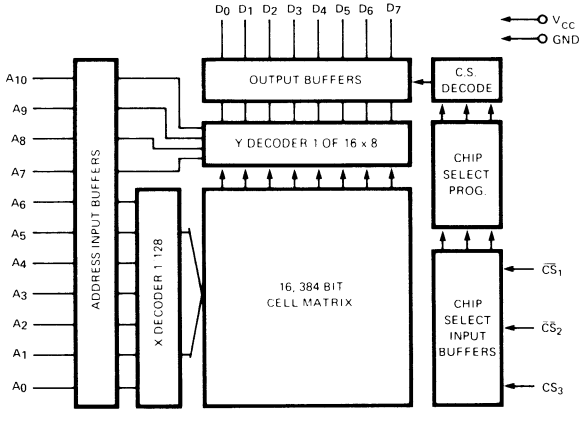
PIN CONFIGURATION



PIN NAMES

A_0–A_{10}	ADDRESS INPUTS
O_7–O_0	DATA OUTPUTS
CS_1–CS_3	CHIP SELECT INPUTS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . .–10°C to 80°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage On Any Pin With Respect
to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . .1.0 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)			10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	µA	Chip Deselected, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			–20	µA	Chip Deselected, V_{OUT} = 0.4V
I_{CC}	Power Supply Current		70	120	mA	All Inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	–0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.4		V_{CC}+1.0V	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = – 400 µA

NOTE: 1. Typical values for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
t_A	Address to Output Delay Time		450	ns
t_{CO}	Chip Select to Output Enable Delay Time		120	ns
t_{DF}	Chip Deselect to Output Data Float Delay Time	10	100	ns

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . . . 1 TTL Gate and C_L = 100 pF
Input Pulse Levels . . . . . .0.8 to 2.4V
Input Pulse Rise and Fall Times (10% to 90%) . . . . . 20 ns
Timing Measurement Reference Level
Input . . . . . 1V and 2.2V
Output . . . . . .0.8V and 2.0V

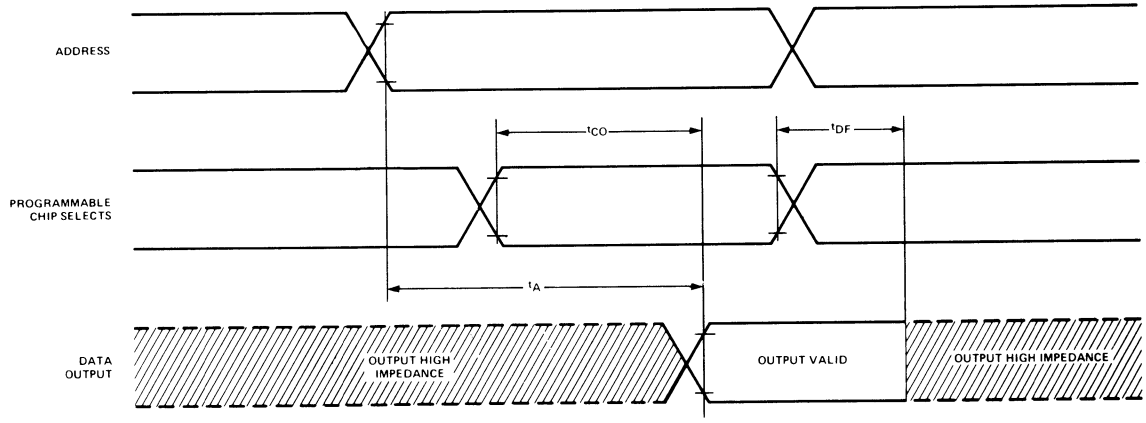
CAPACITANCE(2) T_A = 25°C, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	5 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	10 pF	15 pF

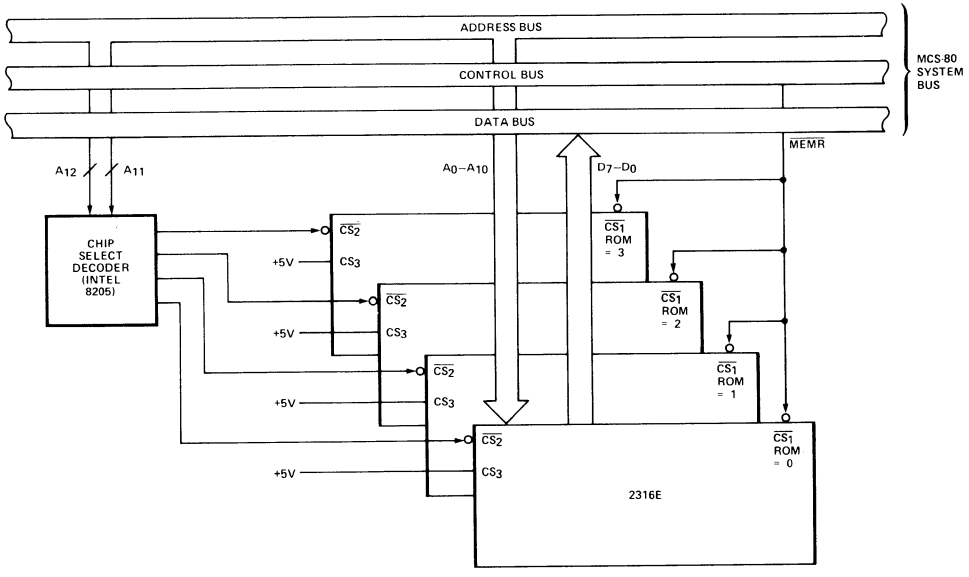
NOTE: 2. This parameter is periodically sampled and is not 100% tested.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. Waveforms



Typical System Application (8K × 8 ROM Memory)



2708 FAMILY
8K AND 4K UV ERASABLE PROM
2708 1K×8 Organization

- **Fast Access Time--350ns Max. (2708-1)**
- **Pin Compatible to 8K and 16K ROMs For Low Cost Production**
- **Fast Programming-- Typ. 100 sec For All 8K Bits**
- **Static--No Clocks Required**
- **2704--512×8 Organization**
- **Data Inputs and Outputs TTL Compatible During Both Real and Program Modes**
- **Three-State Outputs--or-Tie Capability**

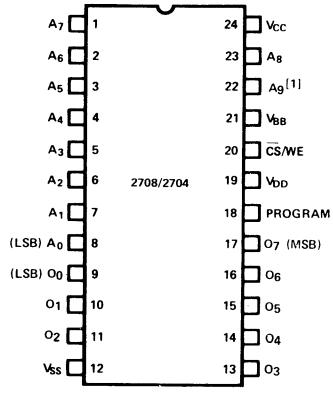
The Intel® 2708 is a 8192-bit ultraviolet light erasable and electrically reprogrammable EPROM ideally suited where fast turnaround and pattern experimentation are important requirements. The electrical characteristics of the 2708 are specified over the 0°C to 70°C operating temperature range and with 5% power supply variation. All data inputs and outputs are TTL compatible during both the read and program mode. Furthermore, the three-state outputs allow for direct interface with common system bus structures. The 2708 is specified at a maximum access time of 450 ns. A higher speed 2708-1 is also available at 350 ns maximum access time.

A pin for pin mask programmed ROM, the Intel® 2308, is available for large volume production runs of systems initially using the 2708. For systems requiring higher bit density, the 2316E Intel 16K ROM with a 420 ns maximum access time is also available.

The 2704 is a 4096-bit UV EPROM organized as 512 words by 8 bits. It has all the same operating, programming, and erasing specifications of the 2708.

The 2708/2704 is fabricated with the time-proven reliable N-channel silicon gate and FAMOS technology. They are available in a 24-pin dual in-line package.

PIN CONFIGURATION

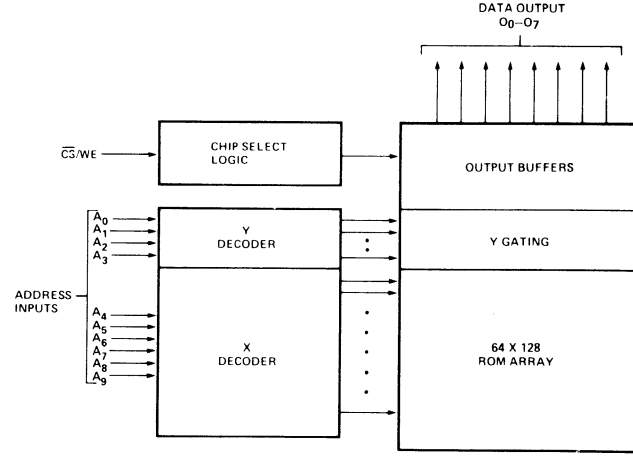


NOTE 1: PIN 22 MUST BE CONNECTED TO V_{SS} FOR THE 2704.

PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

BLOCK DIAGRAM



PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1-8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED ⌿6V	+12	V_{IHW}	-5	+5

PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 3-55.

Absolute Maximum Ratings*

Temperature Under Bias	−25°C to +85°C
Storage Temperature	−65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to −0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to −0.3V
All Input or Output Voltages With Respect to V_{BB} During Read	+15V to −0.3V
$\overline{CS}$/WE Input With Respect to V_{BB} During Programming	+20V to −0.3V
Program Input With Respect to V_{BB}	+35V to −0 3V
Power Dissipation	1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

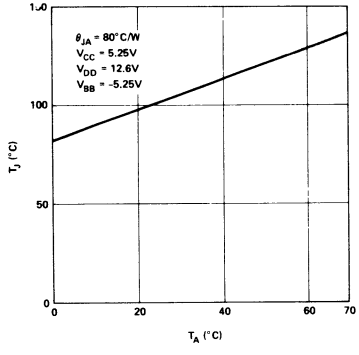
T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB}[1] = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	V_{IN} = 5.25V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10	μA	V_{OUT} = 5.5V, $\overline{CS}$/WE = 5V
I_{DD}[3]	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}[3]	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}[3]	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = −100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = −1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

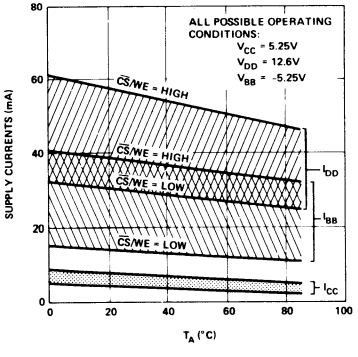
NOTES: 1. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. The total power dissipation of the 2704/2708 is specified at 800 mW. It is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

Typical Characteristics

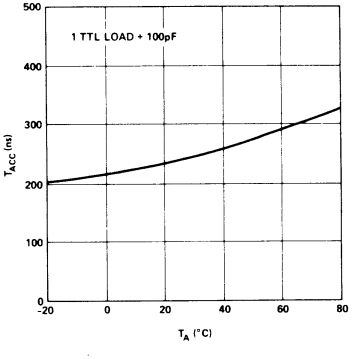
MAXIMUM JUNCTION TEMPERATURE VS. AMBIENT TEMPERATURE



RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



ACCESS TIME VS. TEMPERATURE



A. C. Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	2708-1 Limits			2708 Limits			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{ACC}	Address to Output Delay		280	350		280	450	ns
t_{CO}	Chip Select to Output Delay		60	120		60	120	ns
t_{DF}	Chip Deselect to Output Float	0		120	0		120	ns
t_{OH}	Address to Output Hold	0			0			ns

CAPACITANCE[1] T_A = 25°C, f = 1 MHz

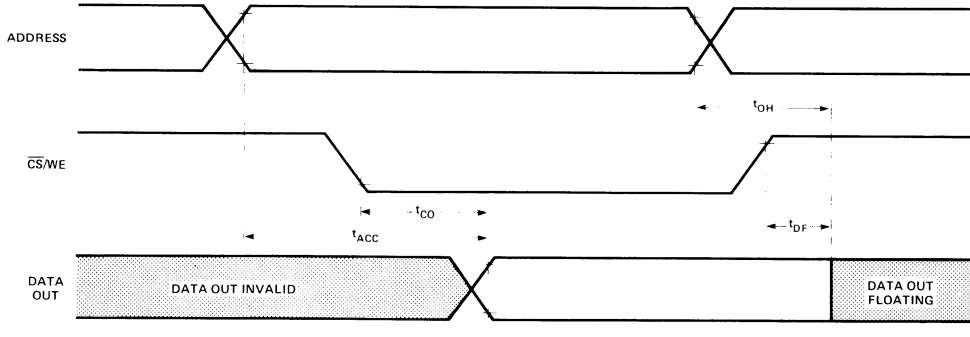
Symbol	Parameter	Typ.	Max.	Unit.	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is periodically sampled and is not 100% tested.

A.C. TEST CONDITIONS:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs.
Input Pulse Levels: 0.65V to 3.0V

Waveforms



ERASURE CHARACTERISTICS

The erasure characteristics of the 2708 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2708 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2708 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2708 window to prevent unintentional erasure.

The recommended erasure procedure (see page 3-55) for the 2708 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2708 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

8K (1K x 8) UV ERASABLE PROM

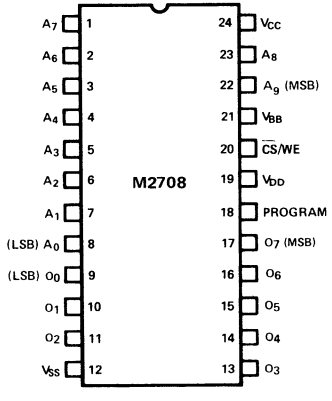
- **Extended Temperature Range: -55°C to 100°C**
- **Fast Programming: Typ. 100 sec. For All 8K Bits**
- **Low Power During Programming**
- **Access Time: 450 ns Max.**
- **Standard Power Supplies: +12V, +5V, -5V**
- **Static: No Clocks Required**
- **Inputs and Outputs TTL Compatible During Both Read and Program Modes**
- **Three-State Output: OR-Tie Capability**
- **Hermetic Package: 24 Pin DIP**

The Intel M2708 is a high speed 8192 bit erasable and electrically reprogrammable ROM (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

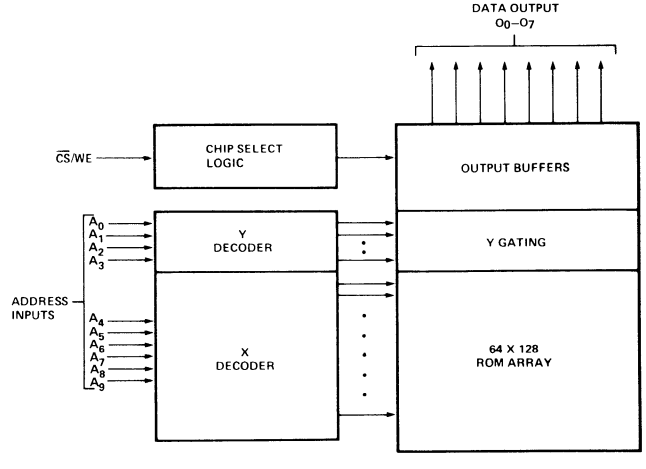
The M2708 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices.

The M2708 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1-8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED V_{IHP}	+12	V_{IHW}	-5	+5

Absolute Maximum Ratings*

Temperature Under Bias	-65°C to 110°C
Storage Temperature	-65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to -0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to -0.3V
All Input or Output Voltages With Respect to V_{BB} During Read	+15V to -0.3V
$\overline{CS}$/WE Input With Respect to V_{BB} During Programming	+20V to -0.3V
Program Input With Respect to V_{BB}	+35V to -0 3V
Power Dissipation	1.8W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

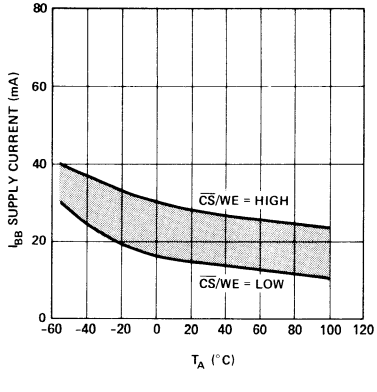
T_A = -55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = +12V ±10%, V_{BB}[1] = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	V_{IN} = 5.5 V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10	μA	V_{OUT} = 5.5 V, $\overline{CS}$/WE = 5V
I_{DD}[3]	V_{DD} Supply Current		50	80	mA	Worst Case Supply Currents:
I_{CC}[3]	V_{CC} Supply Current		6	15	mA	All Inputs High
I_{BB}[3]	V_{BB} Supply Current		30	60	mA	$\overline{CS}$/WE = 5V; T_A = -55°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			750	mW	T_A = 100°C

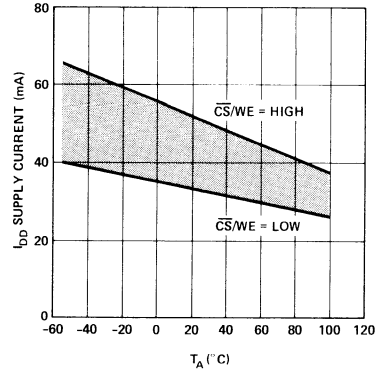
NOTES: 1. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. The total power dissipation of the 2704/2708 is specified at 750 mW. It is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

Typical D.C. Characteristics

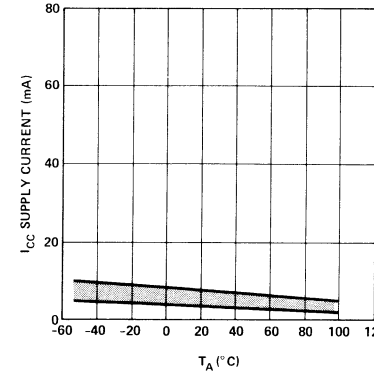
I_{BB} CURRENT VS. TEMPERATURE



I_{DD} CURRENT VS. TEMPERATURE



I_{CC} CURRENT VS. TEMPERATURE



A.C. Characteristics

T_A = -55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = +12V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
t_{CO}	Chip Select to Output Delay		60	120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance[1] T_A = 25°C, f = 1MHz

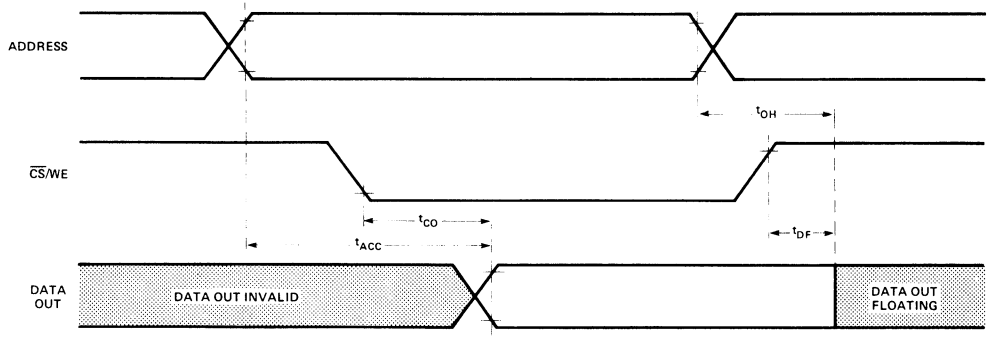
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN}=0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT}=0V

Note 1. This parameter is sampled and not 100% tested.

A.C. TEST CONDITIONS:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

Waveforms



ERASURE CHARACTERISTICS

The erasure characteristics of the M2708 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical M2708 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the M2708 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the M2708 window to prevent unintentional erasure.

The recommended erasure procedure (see page 3-55) for the M2708 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The M2708 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

2716
16K (2K×8) UV ERASABLE PROM

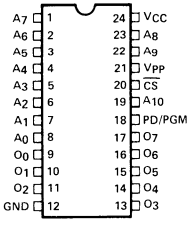
- **Single +5V Power Supply**
- **Simple Programming Requirements**
  Single Location Programming
  Programs With One 50ms Pulse
- **Low Power Dissipation**
  525mW Max. Active Power
  132mW Max. Standby Power
- **Pin Compatible To Intel 2316E ROM**
- **Fast Access Time: 450ns Max.**
- **Inputs and Outputs TTL**
  Compatible During Read
  And Program

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static power down mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2716 user can convert rapidly to Intel's new pin-for-pin compatible 16K ROM, the 2316E.

Since the 450-nsec 2716 operates from a single 5-volt supply, it is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8048. The 2716 is also the first EPROM with a static power down mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Now, it is possible to program on-board, in the system, in the field. Program any location at any time — either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



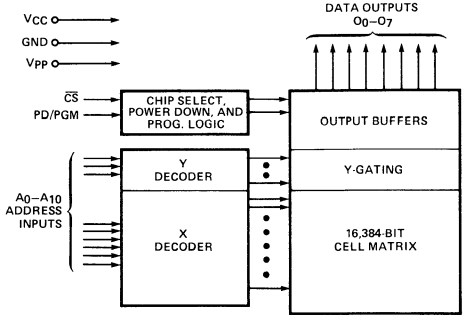
PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 3-55.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
All Input or Output Voltages with Respect to Ground . . . . . +6V to -0.3V
V_{PP} Supply Voltage with Respect to Ground . . . . . +28V to -0.3V

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

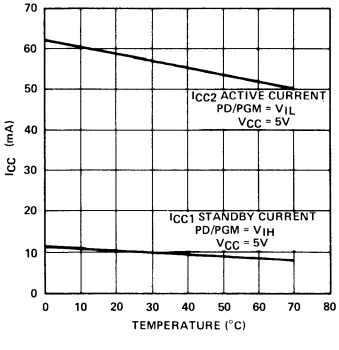
T_A = 0°C to 70°C, V_{CC}[1,2] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[4]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.85V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	PD/PGM = V_{IH}, $\overline{CS}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{CS}$ = PD/PGM = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.2		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

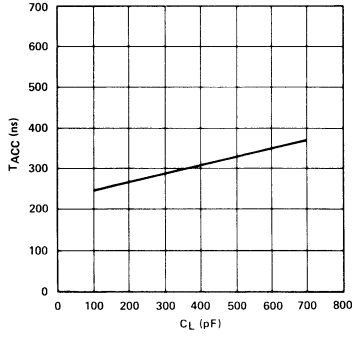
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for T_A = 25°C and nominal supply voltages.
5. This parameter is only sampled and is not 100% tested.
6. t_{ACC2} is referenced to PD/PGM or the addresses, whichever occurs last.

Typical Characteristics

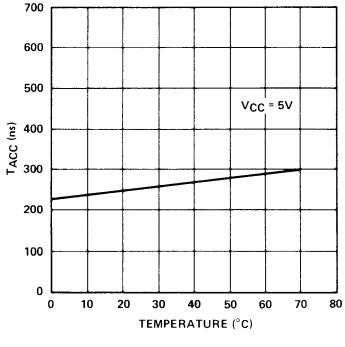
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. Characteristics

$T_A = 0°C$ to $70°C$, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[4]	Max.		
t_{ACC1}	Address to Output Delay		250	450	ns	PD/PGM = $\overline{CS}$ = V_{IL}
t_{ACC2}	PD/PGM to Output Delay		280	450	ns	$\overline{CS}$ = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PF}	PD/PGM to Output Float	0		100	ns	$\overline{CS}$ = V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM = V_{IL}
t_{OH}	Address to Output Hold	0			ns	PD/PGM = $\overline{CS}$ = V_{IL}

Capacitance[5] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

NOTE: Please refer to page 2 for notes.

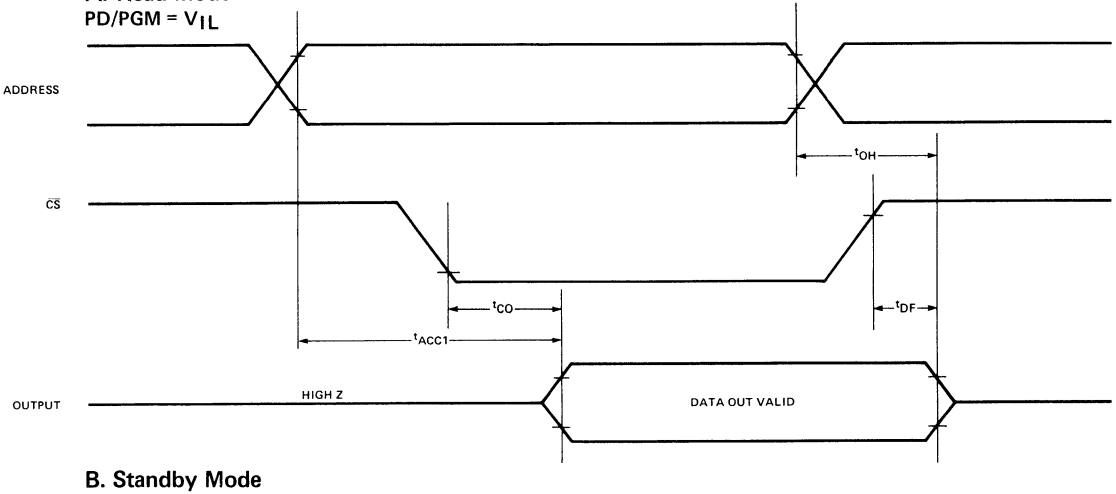
A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

WAVEFORMS

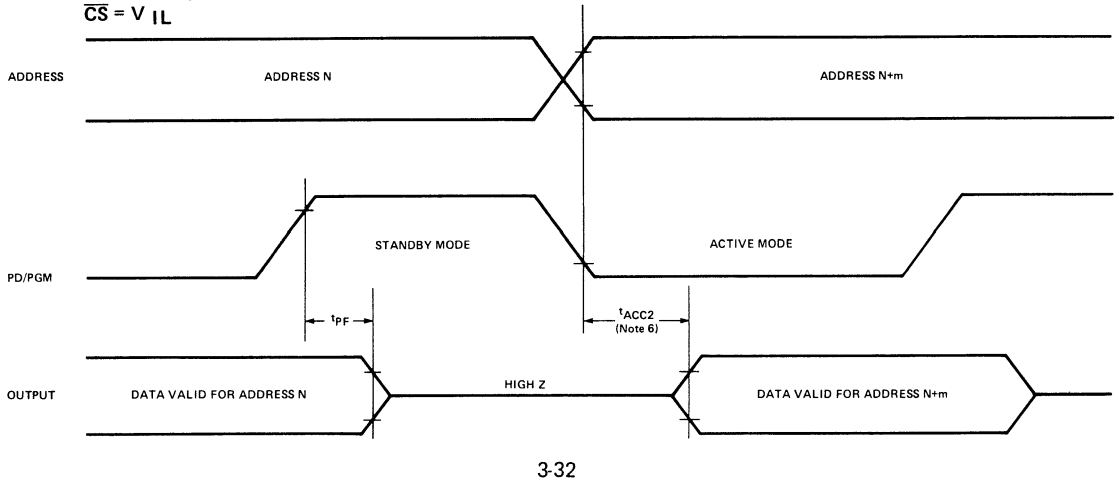
A. Read Mode

PD/PGM = V_{IL}



B. Standby Mode

$\overline{CS}$ = V_{IL}



ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see page 3-55) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The six modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other three modes.

TABLE I. MODE SELECTION

MODE \ PINS	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

Data is available at the outputs in the read mode. Data is available 450 ns (t_{ACC}) from stable addresses with $\overline{CS}$ low or 120 ns (t_{CO}) from $\overline{CS}$ with addresses stable.

DESELECT MODE

The outputs of two or more 2716s may be OR-tied together on the same data bus. Only one 2716 should have its outputs selected ($\overline{CS}$ low) to prevent data bus contention between 2716s in this configuration. The outputs of the other 2716s should be deselected with the $\overline{CS}$ input at a high TTL level.

POWER DOWN MODE

The 2716 has a power down mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. Power down is achieved by applying a TTL high signal to the PD/PGM input. In power down the outputs are in a high impedance state, independent of the $\overline{CS}$ input.

PROGRAMMING

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{CS}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the addresses and data are stable, a 50 msec, active high, TTL program pulse is applied to the PD/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the PD/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the PD/PGM input programs the paralleled 2716s.

PROGRAM INHIBIT

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for PD/PGM, all like inputs (including $\overline{CS}$) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's PD/PGM input with V_{PP} at 25V will program that 2716. A low level PD/PGM input inhibits the other 2716s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed wth V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

3601, 3621

256 x 4 HIGH SPEED PROM

3601-1, 3621-1	50 ns Max.
3601, 3621	70 ns Max.

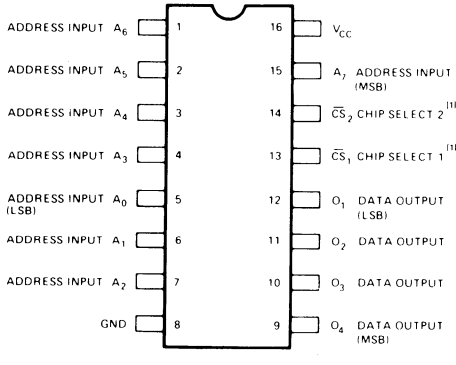
- **Low Power Dissipation: 0.5 mW/Bit Typical**
- **Open Collector (3601) and Three-State Outputs (3621)**
- **Fast Programming: 1 ms/Bit Typically**
- **Polycrystalline Silicon Fuse**
- **16 Pin Dual In-Line Hermetic Package**

The Intel® 3601/3621 is a 1024 bit PROM ideally suited for uses where fast turnaround and pattern experimentations are important, such as in prototypes or in small productions volume systems. The 3601 is manufactured with all outputs low, and logic high output levels can be electrically programmed in selected bit locations. The 3621 has its outputs initially high and logic low output levels are programmed. The same address inputs are used for both programming and reading.

A higher system performance is achieved by using the 3601-1 or 3621-1. These PROMs give a 25% system speed improvement over the 3601 or 3621.

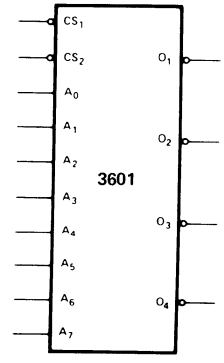
The 3601/3621 is manufactured with the highly reliable polycrystalline silicon fuse and the fast switching Schottky barrier diode technology.

PIN CONFIGURATION

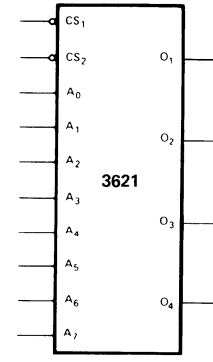


NOTE 1. DURING PROGRAMMING, THE PROGRAM PULSE MAY BE APPLIED TO EITHER $\overline{CS}_1$ OR $\overline{CS}_2$ FOR THE 3621 FAMILY. THE PROGRAM PULSE IS APPLIED TO $\overline{CS}_2$ FOR THE 3601 FAMILY.

LOGIC SYMBOL



LOGIC SYMBOL



PIN NAMES

A_0–A_7	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$	CHIP SELECT INPUTS
O_1–O_4	DATA OUTPUTS

Absolute Maximum Ratings*

Temperature Under Bias	−65°C to +125°C
Storage Temperature	−65°C to +160°C
Output or Supply Voltages	−0.5V to 7 Volts
All Input Voltages	-1.6V to 5.5V
Output Currents	100mA
Programming Only:	

	3601	3621
Output or V_{CC} Voltages	10.25V	13V
$\overline{CS}_2$ Voltage	15.5V	15.5V
$\overline{CS}_2$ Current	100mA	150mA
V_{CC} Current	500mA	600mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C Unless Otherwise Specified.

Symbol	Parameter	Limits Min.	Limits Typ.[1]	Limits Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15mA
I_{CC}	Power Supply Current		90	130	mA	V_{CC}=5.25V, $V_{A0} \rightarrow V_{A7}$ = 0V $\overline{CS}_1 = \overline{CS}_2$ = 0V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

FOR 3621, 3621-1 ONLY

Symbol	Parameter	Limits Min.	Limits Typ.[1]	Limits Max.	Unit	Test Conditions
I_O	Output Leakage for High Impedance Stage			40	μA	V_O = 5.25V or 0.45V, V_{CC} = 5.25V, $\overline{CS}_1 = \overline{CS}_2$ = 2.4V
I_{SC}[2]	Output Short Circuit Current			-60	mA	V_{CC} = 5.00V, T_A = 25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to + 75°C

SYMBOL	PARAMETER	MAXIMUM LIMITS			UNIT	CONDITIONS
		0°C	25°C	75°C		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	3601-1 and 3621-1 Address to Output Delay	50	50	50	ns	Both C.S. lines must be at ground potential to activate the PROM.
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	3601 and 3621 Address to Output Delay	70	60	70	ns	
t_{S++}, t_{S--}	Chip Select to Output Delay	25	25	25	ns	

Capacitance [1] T_A = 25°C

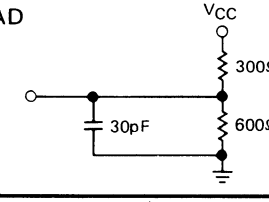
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V	V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

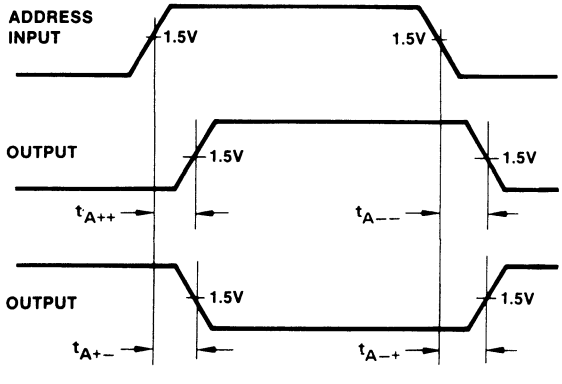
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

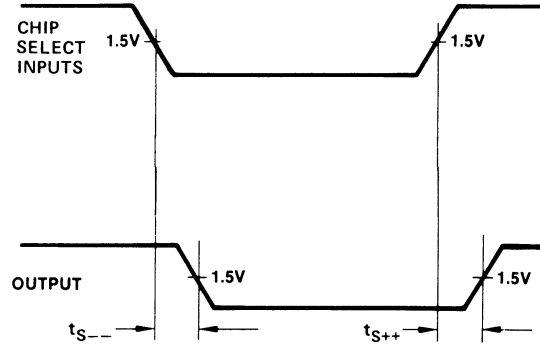


Waveforms

ADDRESS TO OUTPUT DELAY

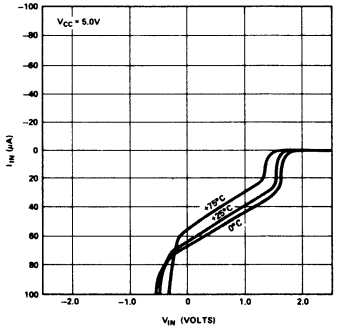


CHIP SELECT TO OUTPUT DELAY

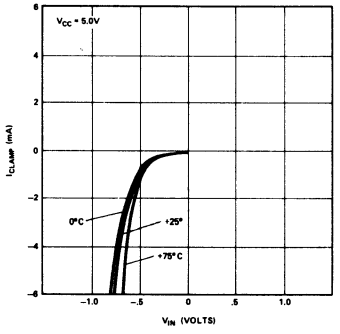


Typical D. C. Characteristics

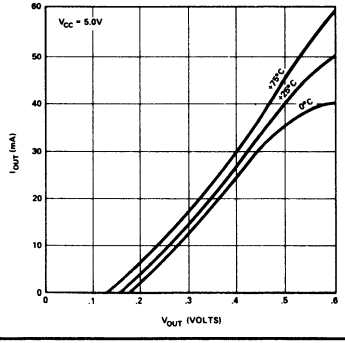
INPUT CURRENT
VS. INPUT VOLTAGE



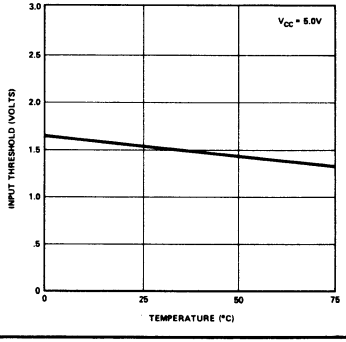
INPUT CLAMP CURRENT
VS. INPUT VOLTAGE



OUTPUT CURRENT
VS. OUTPUT "LOW" VOLTAGE

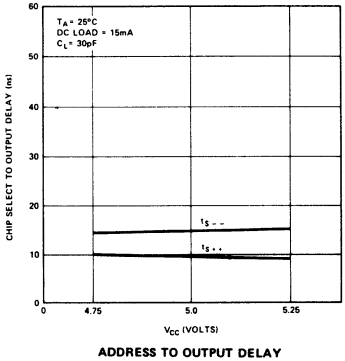


INPUT THRESHOLD
VS. TEMPERATURE

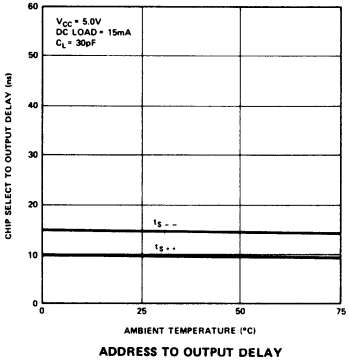


Typical A. C. Characteristics

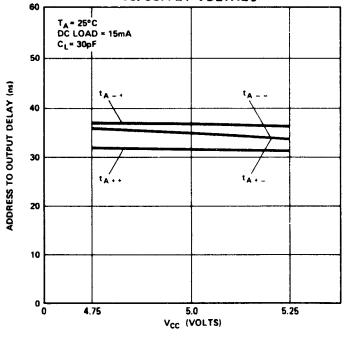
SELECT TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



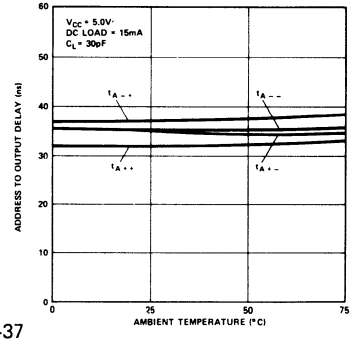
SELECT TO OUTPUT DELAY
VS. AMBIENT TEMPERATURE



ADDRESS TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



ADDRESS TO OUTPUT DELAY
VS. AMBIENT TEMPERATURE



M3601

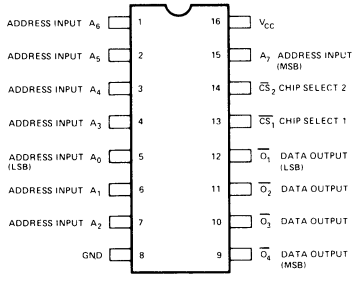
MILITARY TEMP.

HIGH SPEED ELECTRICALLY PROGRAMMABLE 1024 BIT READ ONLY MEMORY

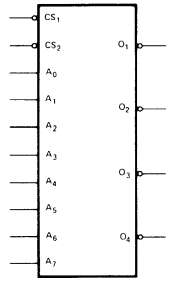
- **Military Temperature Range −55°C to +125°C**
- **Fast Access Time — 90 nsec Maximum**
- **Fast Programming — 1 ms/bit Typically**
- **Open Collector Outputs**
- **Standard Packaging — 16 Pin Hermetic Dual In-Line Lead Configuration**

The M3601 is a military temperature range PROM, organized as 256 words by 4-bits. The PROM is manufactured with all outputs low and logic output high levels can be electrically programmed in selected bit locations. The M3601 is pin compatible with the Intel metal mask ROM M3301A.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-65° C to +150° C
Storage Temperature	-65° C to +160° C
Output or Supply Voltages	-0.5V to 7 Volts
All Input Voltages	-1.3 to 5.5V
Output Currents	100mA
Programming Only:	
Output or V_{CC} Voltages	10.25V
CS_2 Voltage	15.25V
V_{CC} Current	500mA
CS_2 Current	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

All limits apply for V_{CC} = +5.0V ±5%, T_A = -55°C to +125°C, unless otherwise specified.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.7	-1.2	V	V_{CC} = 4.75V, I_A = -5.0mA
V_{CS}	Chip Select Input Clamp Voltage		-0.7	-1.2	V	V_{CC} = 4.75V, I_S = -5.0mA
V_{CS}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 10mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 5.25V, V_{CE} = 5.25V V_{CC} = 5.25V,
I_{CC}	Power Supply Current		90	130	mA	$V_{A0} \rightarrow V_{A7}$ = 0V, $V_{S0} = V_{S1}$ = 0V
V_{IL}	Input "Low" Voltage			0.80	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.1			V	V_{CC} = 5.0V

NOTE 1: Typical values are at 25° C and at nominal voltage.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = -55°C to +125°C

SYMBOL	PARAMETER	MAX. LIMIT	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	90	ns	Both C.S. lines must be at ground potential to activate the PROM.
t_{S++}, t_{S--}	Chip Select to Output Delay	35	ns	

Capacitance [1] T_A = 25°C

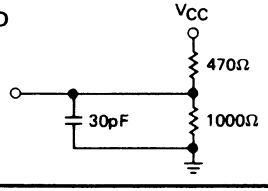
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V	V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

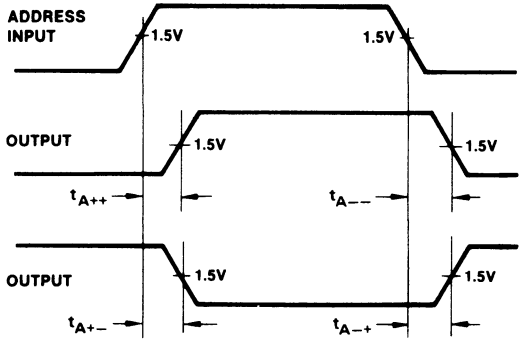
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test - 2.5 MHz

10 mA TEST LOAD

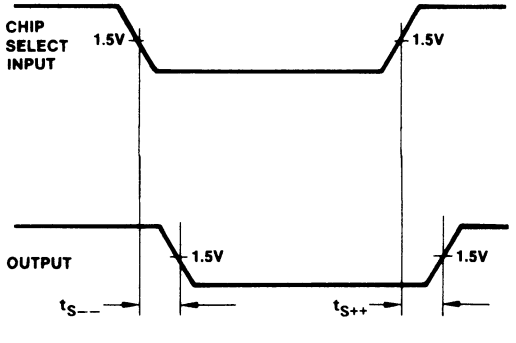


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3602A, 3622A FAMILY
3602, 3622 FAMILY
2048 BIT (512×4) HIGH SPEED PROM

	3602A-2 3622A-2	3602A 3622A	3602 3622
Typ. T_A(ns)	45	55	60
Max. T_A(ns)	60	70	70

- **Low Power Dissipation --0.3mW/Bit**
- **Open Collector (3602A, 3602) or Three State (3622A, 3622) Outputs**
- **Simple Memory Expansion-- Chip Select Input Lead**
- **Replaces Two 256×4 PROMs Without Increasing Board Area**
- **Polycrystalline Silicon Fuse For Higher Reliability**
- **Hermetic 16-Pin DIP**

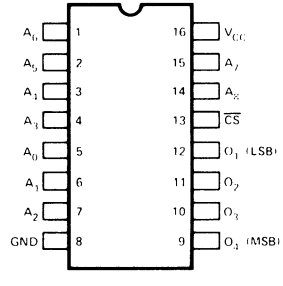
The Intel® 3602A/3622A and 3602/3622 device families are 2048-bit bipolar PROMs organized as 512 words by 4 bits. The fast second generation 3602A/3622A joins its Intel predecessor, the 3602/3622, featuring 70 ns. A higher speed version, the 3602A-2/3622A-2, is now available at 60 ns. All 3602A/3622A specifications, except programming, are the same as the 3602/3622. Once programmed, the 3602A/3622A are interchangeable with the 3602/3622.

The PROMs are manufactured with all outputs initially logically high. Logic low levels can be electrically programmed in selected bit locations. Both open collector and three-state outputs are available. The power dissipation is typically 0.3 mW/bit.

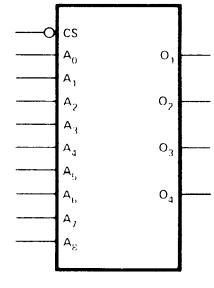
The pin configuration of the PROMs is the same as the popular 1K bit, 256 X 4 PROMs with the exception that CS_2 (pin 14) is address A_8. The bit density of existing 256 X 4 PROM systems can be easily doubled without an increase in area with the 3602A/3622A or 3602/3622. These PROMs, like the 256 X 4 PROMs, are in 16-pin dual in-line package.

A pin compatible, mask programmable 3302/3322 ROM is available for large volume production systems initially using the 3602/3622. Please contact Intel directly for details on these ROMs.

PIN CONFIGURATION



LOGIC SYMBOL



PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 3-55.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6V to 5.6V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15mA
I_{CEX}	Output Leakage Current			40	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC}	Power Supply Current		110	140	mA	V_{CC}=5.25V, V_{A0}→V_{A8} = 0V $\overline{CS}$ = 0V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

3622A, 3622A-2, 3622 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			40	μA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC}=4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMIT			UNIT	CONDITIONS
		3602A-2 3622A-2	3602A 3622A	3602 3622		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	70	70	ns	$\overline{CS}$ = V_{IL} to Select the PROM
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	30	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

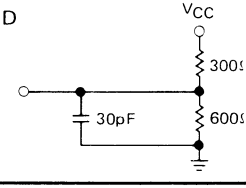
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

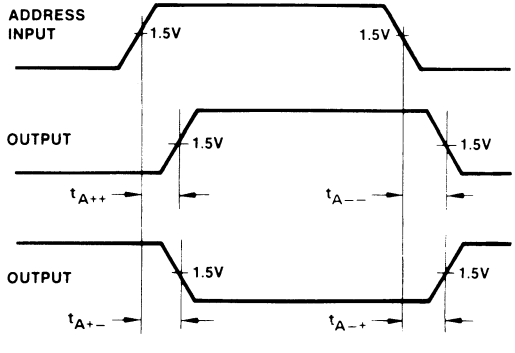
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

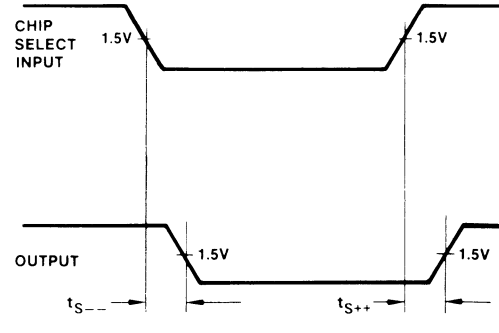


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3604A, 3624A AND 3604, 3624 FAMILY
4096 BIT (512×8) HIGH SPEED PROM

	3604A-2 3624A-2	3604A 3624A	3604AL	3604 3624	3604-4 3624-4	3604L-6
Max. T_A(ns)	60	70	90	70	90	90
Max. I_{CC}(mA)	175	175	130/25*	190	190	140/45*

*Standby Current When The Chip is Deselected.

- **Fast Access Time --60ns Max (3604A-2, 3624A-2)**
- **Low Standby Power Dissipation (3604AL) --32μW/Bit Max**
- **Open Collector (3604A, 3604) or Three State (3624A, 3624) Outputs**
- **Four Chip Select Inputs For Easy Memory Expansion**
- **Polycrystalline Silicon Fuse For Higher Reliability**
- **Hermetic 24 Pin DIP**

The Intel® 3604A/3624A and 3604/3624 device families are 4096-bit bipolar PROMs organized as 512 words by 8 bits. The fast second generation 3604A/3624A joins its Intel predecessor, the 3604/3624, featuring 70 ns. Higher speed PROMs, the 3604A-2/3624A-2, are now available at 60 ns. The 3604A/3624A families are lower in power dissipation than the 3604/3624 families. All 3604A/3624A specifications, except programming, are the same as or better than the 3604/3624. Once programmed, the 3604A/3624A are interchangeable with the 3604/3624.

The PROMs are manufactured with all outputs initially logically high. Logic low levels can be electrically programmed in selected bit locations. Both open collector and three-state outputs are available. Low standby power dissipation can be achieved with either the 3604AL or 3604L-6. The standby power dissipation is approximately 15% of the active power dissipation.

The 3604A/3624A and 3604/3624 families are available in a hermetic 24-pin dual in-line package. These PROMs are manufactured with the time-proven polycrystalline silicon fuse technology. A pin compatible, mask programmable ROM is available for large volume production of systems initially using the 3604/3624. Please contact Intel directly for details on these ROMs.

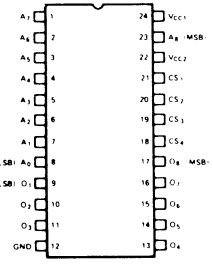
Mode/Pin Connection		Pin 22	Pin 24
READ:	3604A, 3604A-2, 3604, 3604-4, 3624A, 3624A-2, 3624, 3624-4	No Connect or 5V	5V
	3604AL, 3604L-6	+5V	Must be Left Open
PROGRAM:	3604A, 3604A-2, 3604, 3604-4, 3624A, 3624A-2, 3624, 3624-4	Pulsed 12.5V	Pulsed 12.5V
	3604AL, 3604L-6	Pulsed 12.5V	Pulsed 12.5V
STANDBY:	3604AL, 3604L-6	Power dissipation is automatically reduced whenever the 3604AL or 3604L-6 is deselected.	

PIN NAMES

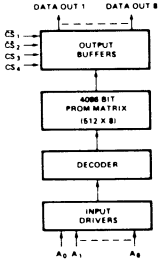
A_0–A_8	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$, CS_3–CS_4 [1]	CHIP SELECT INPUTS
O_1–O_8	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = \overline{CS}_2 = 0$ and $CS_3 = CS_4 = 1$.

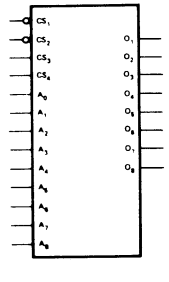
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 3-55.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6 to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10 mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10 mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15 mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC1}	Power Supply Current (3604A, 3604A-2, 3624A, and 3624A-2)		130	175	mA	V_{CC1} = 5.25V, V_{A0}→V_{A8} = 0V, $\overline{CS}_1$ = $\overline{CS}_2$ = 0V, CS_3 = CS_4 = 5.25V
I_{CC2}	Power Supply Current (3604, 3604-4, 3624, and 3624-4)		160	190	mA	V_{CC1} = 5.25V, V_{A0}→V_{A8} = 0V, $\overline{CS}_1$ = $\overline{CS}_2$ = 0V, CS_3 = CS_4 = 5.25V
I_{CC3}	Power Supply Current (3604AL) Active		100	130	mA	V_{CC2} = 5.25V, V_{CC1} = Open $\overline{CS}_1$ = $\overline{CS}_2$ = 0.45V, CS_3 = CS_4 = 2.4V
	Standby		15	25	mA	$\overline{CS}_1$ = $\overline{CS}_2$ = 2.5V
I_{CC4}	Power Supply Current (3604L-6) Active			140	mA	V_{CC2} = 5.25V, V_{CC1} = Open $\overline{CS}_1$ = $\overline{CS}_2$ = 0.45V, CS_3 = CS_4 = 2.4V
	Standby			45	mA	$\overline{CS}_1$ = $\overline{CS}_2$ = 2.5V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

3624A AND 3624 FAMILY ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	μA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1$=$\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	3604A, 3624A FAMILY MAXIMUM LIMITS (ns)			3064, 3624 FAMILY MAXIMUM LIMITS (ns)		
		3604A-2 3624A-2	3604A 3624A	3604AL	3064 3624	3604-4 3624-4	3604L-6
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	70	90	70	90	90
t_{S++}	Chip Select to Output Delay	30	30	30	30	30	30
t_{S--}	Chip Select to Output Delay	30	30	120	30	30	120

Capacitance [1] T_A = 25°C, f = 1 MHz

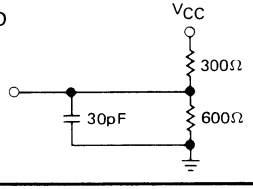
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V	V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

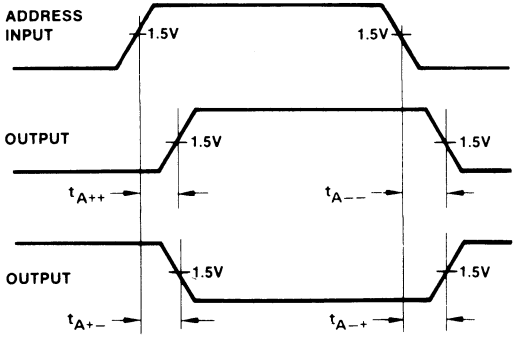
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

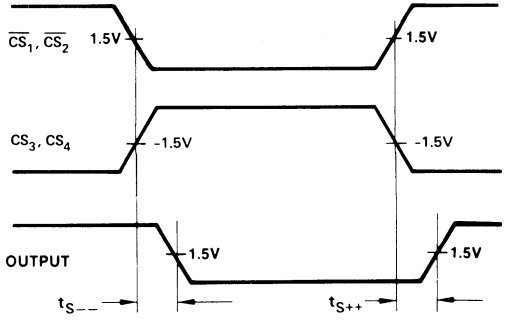


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



M3604, M3624 HIGH SPEED ELECTRICALLY PROGRAMMABLE 4096 BIT READ ONLY MEMORY

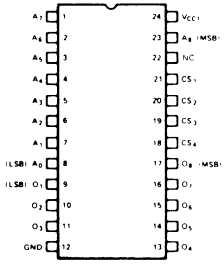
MILITARY TEMP.

PROM/ROM

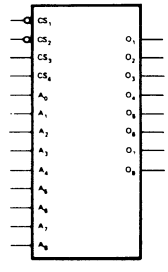
- Military Temperature Range −55°C to +125°C
- Fast Access Time—90nsec Maximum
- Open Collector (M3604) or Three-State (M3624) Outputs
- Four Chip Select Inputs For Easy Memory Expansion
- Polycrystalline Silicon Fuse For Higher Reliability
- Standard Packaging—24Pin Hermetic Dual In-Line Lead Configuration

The M3604 and M3624 are military temperature range PROMs organized as 512 words by 8 bits. They are manufactured with all outputs high and logic output low levels can be electrically programmed in selected bit locations. Both open collector (M3604) and three-state (M3624) outputs are available.

PIN CONFIGURATION



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias	−65°C to +135 C
Storage Temperature	−65°C to +160°C
Output or Supply Voltages	−0.5V to 7 Volts
All Input Voltages	−1.6V to 5.6V
Output Currents	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics V_{CC} = +5.0V ±10%, T_A = −55°C to +125°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}= Max, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}= Max, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC}= Max, V_A= Max
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC}= Max, V_S= Max
V_{CA}	Address Input Clamp Voltage		-0.9	−1.5	V	V_{CC}= Min, I_A= −10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	−1.5	V	V_{CC}= Min, I_S= −10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}= Min, I_{OL}= 10mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC}= Max, V_{CE}= Max
I_{CC1}	Power Supply Current (M3604)			190	mA	V_{CC1}= Max, V_{A0}→V_{A8}=0V, $\overline{CS_1}$=$\overline{CS_2}$=0V, CS_3=CS_4= 5.5V
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC}= 5.0V, T_A=25°C
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}= 5.0V, T_A=25°C

M3624 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	μA	V_O= Max or 0.45V, V_{CC}= Max, $\overline{CS_1}$=$\overline{CS_2}$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 5V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5.0V ±10%, T_A = −55°C to +125°C

SYMBOL	PARAMETER	LIMITS TYP.[1]	LIMITS MAX.	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	90	ns	$CS_1 = CS_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to Select the PROM
t_{S++}	Chip Select to Output Delay	20	45	ns	
t_{S--}	Chip Select to Output Delay	20	45	ns	

PROM/ROM

Capacitance[2] T_A = 25°C, f = 1 MHz

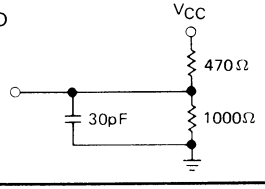
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTES: 1. Typical values are at 25°C and nominal voltage.
2. This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

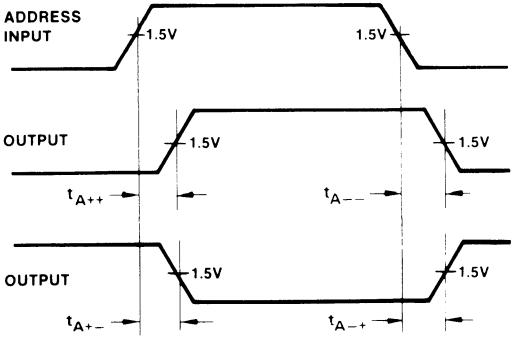
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test - 2.5 MHz

10 mA TEST LOAD

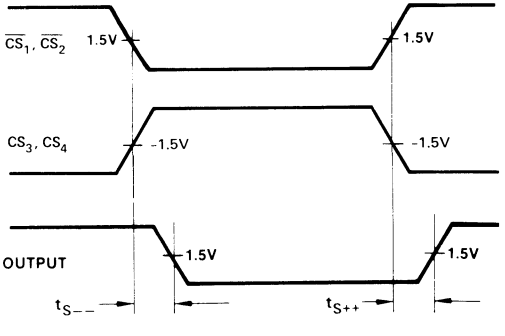


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3605, 3625
HIGH SPEED 1K x 4 PROM

3605-2, 3625-2	60 ns Max.
3605, 3625	70 ns Max.

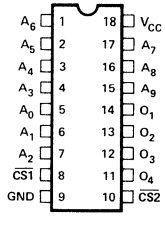
- **Fast Access Time: 45ns Typically**
- **Low Power Dissipation: 0.14mW/Bit Typically**
- **Simple Memory Expansion Two Chip Select Inputs**
- **Open Collector (3605) and Three-State(3625) Outputs**
- **Polycrystalline Silicon Fuse For Higher Reliability**
- **Hermetic 18 Pin DIP**

The Intel® 3605 and 3625 families are high density, 4096-bit bipolar PROMs organized as 1024 words by 4 bits. The 1024 by 4 organization gives ideal word or bit modularity for memory array expansion. The 3605 has open collector outputs and the 3625 has three-state outputs. The 3605 and 3625 are fully specified over the 0°C to 75°C temperature range with ±5% power supply variation. Maximum access times of 60 ns (3605-2/3625-2) and 70 ns (3605/3625) are available. The typical power dissipation is 0.14 mW/bit.

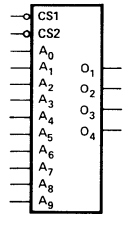
The 3605/3625 are packaged in an 18-pin dual in-line hermetic package with 300 milli-inch centers. Thus, twice the bit density can be achieved with the 3605/3625 in the same memory board area as 512 by 8-bit PROMs in 24-pin packages.

The highly reliable polycrystalline silicon fuse technology is used in the manufacturing of the 3605 and 3625 families. All outputs are initially a logical high and logic low levels can be electrically programmed in selected bit locations.

PIN CONFIGURATION



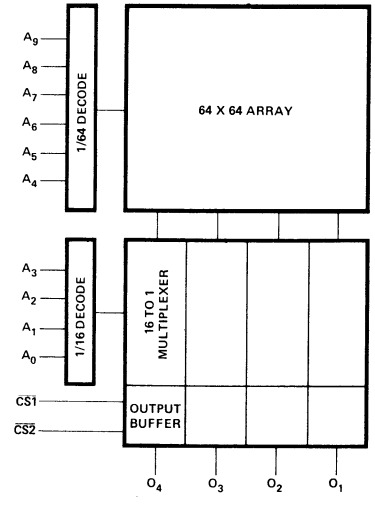
LOGIC SYMBOL



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
$O_1 - O_4$	OUTPUTS

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 3-55.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC}=5.25V, V_A=5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC}=5.25V, V_S=5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_A=-10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_S=-10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}=4.75V, I_{OL}=15mA
I_{CEX}	3605 Output Leakage Current			40	μA	V_{CC}=5.25V, V_{CE}=5.25V
I_{CC}	Power Supply Current		110	150	mA	V_{CC}=5.25V, V_{A0}→V_{A9}=0V, $\overline{CS}_1$=$\overline{CS}_2$=V_{IH}
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC}=5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}=5.0V

3625, 3625-2 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			40	μA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1$=$\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Max. Limits 3605-2 3625-2	Max. Limits 3605 3625	Unit	Conditions
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	70	ns	$\overline{CS}_1=\overline{CS}_2=V_{IL}$ to select the PROM.
t_{S++}	Chip Select to Output Delay	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

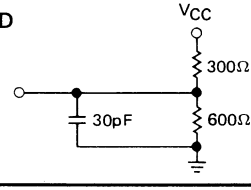
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

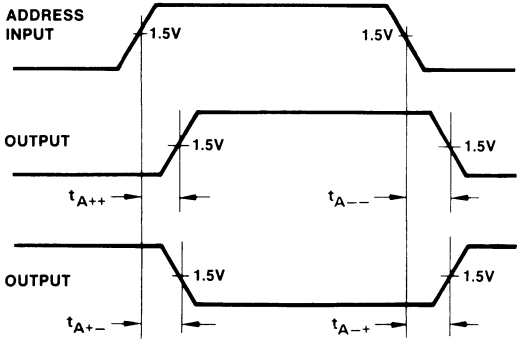
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15mA TEST LOAD

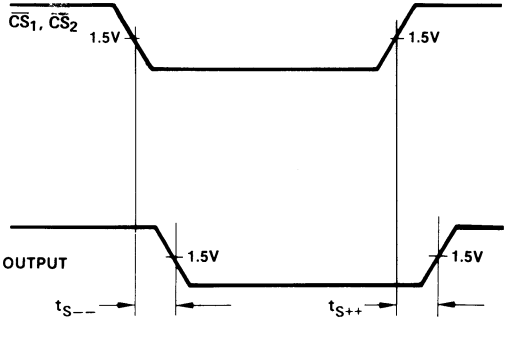


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

3608, 3628
8K (1K X 8) BIPOLAR PROM

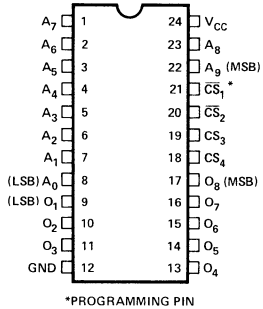
3608, 3628	80 ns Max.
3608-4, 3628-4	100 ns Max.

- **Fast Access Time: 65 ns Typically**
- **Low Power Dissipation: 0.09mW/Bit Typically**
- **Four Chip Select Inputs for Easy Memory Expansion**
- **Open Collector (3608) and Three-State (3628) Outputs**
- **Hermetic 24-Pin DIP**
- **Polycrystalline Silicon Fuses for Higher Fuse Reliability**

The Intel® 3608/3628 are fully decoded 8192-bit PROMs organized as 1024 words by 8 bits. The worst case access time of 80 ns is specified over the 0°C to 75°C temperature range and 5% V_{CC} power supply tolerances. There are four chip selects provided to facilitate expanding 3608/3628s into larger PROM arrays. The PROMs use Schottky clamped TTL technology with polycrystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

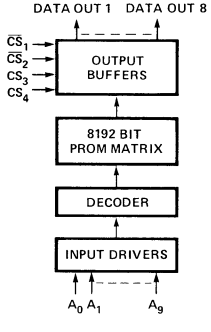
Prior to the 8192 bit 3608/3628, the highest density bipolar PROM available was 4096 bits. The high density of the 3608/3628 now easily doubles the capacity without an increase in area on existing designs currently using 512 words by 8 bit PROMs. There is also little, if any, penalty in power since the 3608/3628 power/bit is approximately one-half that of 4K PROMs. The 3608/3628 are packaged in a hermetic 24-pin dual in-line package.

PIN CONFIGURATION

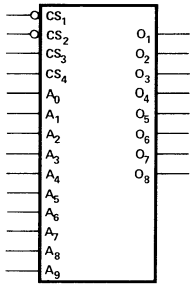


*PROGRAMMING PIN

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$\overline{CS}_1 - \overline{CS}_2$, $CS_3 - CS_4$	CHIP SELECT INPUTS[1]
$O_1 - O_8$	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = \overline{CS}_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 3-55.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS: All Limits Apply for V_{CC}= +5.0V ±5%, T_A= 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	µA	V_{CC}=5.25V, V_A=5.25V
I_{RS}	Chip Select Input Leakage Current			40	µA	V_{CC}=5.25V, V_S=5.0V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_A=-10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_S=-10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}=4.75V, I_{OL}= 10mA
I_{CEX}	3608 and 3608-4 Output Leakage Current			100	µA	V_{CC}=5.25V, V_{CE}=5.25V
I_{CC}	Power Supply Current		150	190	mA	V_{CC} =5.25V, V_{A0}→V_{A9}=0V, PROM deselected
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC}=5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}=5.0V

3628,3628-4 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance State			100	µA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1$=$\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-20	-25	-80	mA	V_O = 0V
V_{OH}	Output High Voltage	2.4	3.4		V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

A.C. CHARACTERISTICS V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMITS 3608 3628	MAX. LIMITS 3608-4 3628-4	UNIT	CONDITIONS
t_A	Address to Output Delay	80	100	ns	$\overline{CS}_1 = \overline{CS}_2 = V_{IL}$
t_{EN}	Output Enable Time	40	45	ns	and $CS_3 = CS_4 = V_{IH}$
t_{DIS}	Output Disable Time	40	45	ns	to select the PROM.

CAPACITANCE [1] T_A = 25°C, f = 1 MHz

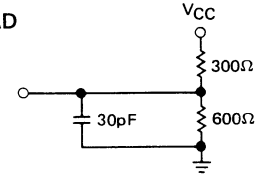
SYMBOL	PARAMETER	TYP. LIMITS TYP.	TYP. LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

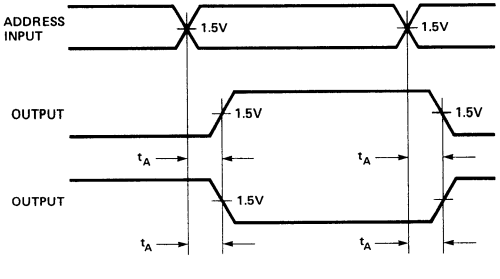
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15mA TEST LOAD

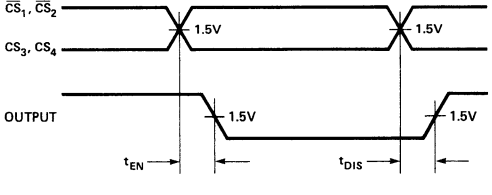


WAVEFORMS

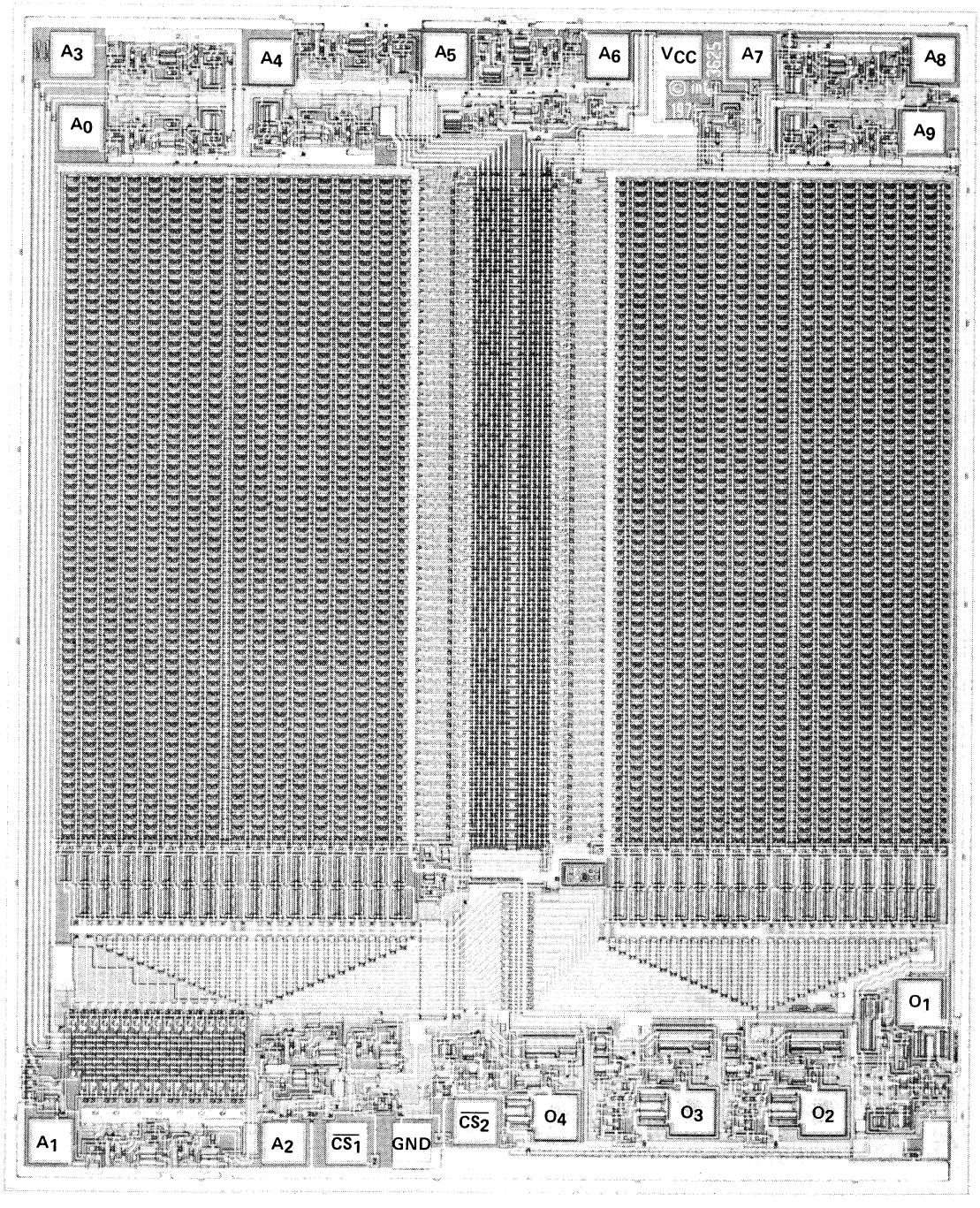
ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3625 4K BIPOLAR PROM



PROM AND ROM PROGRAMMING INSTRUCTIONS

TABLE OF CONTENTS

Page No.

I. PROM AND ROM INPUT FORMATS

A. General Information

Intel can accept programming and masking information for PROMs, EPROMs, or ROMs in the form of punched paper tape, a master device from which to copy, or computer punched cards. The allowable paper tape and computer punched card formats are given in Table I. The preferred formats are the Intel Intellec Hex and BPNF since these formats are defined to allow detection of errors.

It is desirable that two, preferably different, input media for each customer code be sent so Intel can perform a code verification to detect any errors between the two inputs. This procedure, if followed, can avoid errors due to a mispunched tape/card or sending a defective or improper master device.

All orders must be accompanied by a customer PROM/ROM order form. A copy of the form is contained in this section and additional copies are available from Intel Literature Department, 3065 Bowers Ave., Santa Clara, California 95051.

Table I. Acceptable Paper Tape and Computer Card Formats

Paper Tape	Computer Card
Intellec Hex BPNF Hex	Intellec Hex PN

B. Paper Tape Format

The paper tape which should be used is 1" wide paper using 7 or 8-bit ASCII code (such as a Model 33 ASR Teletype produces). The three paper tape formats which should be sent are described in Sections B1 through B3.

B1. Intellec Hex Paper Tape Format

In the Intel Intellec Hex Format, a data field can contain either 8 or 4-bit data. *Two* ASCII hexadecimal characters must be used to represent *both* 8 and 4-bit data. In the case of 4-bit data, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form.

Preceding the first data field and following the last data field there must be a leader/trailer length of at least 25 null characters. Comments (except for a colon) may be placed on the tape leader.

The format described below is readily generated by the Intel Intellec Microcomputer Development System or by systems programmed by the user.

1. RECORD MARK FIELD: Frame 0

   The ASCII code for a colon (:) is used to signal the start of a record.

2. RECORD LENGTH FIELD: Frames 1 and 2

   The number of data bytes in the record is representated by two ASCII hexadecimal digits in this field. The high-order digit is in frame 1. The maximum number of data bytes in a record is 255 (FF in hexadecimal). An end-of-file record contains two ASCII zeros in this field.

3. LOAD ADDRESS FIELD: Frames 3–6

   The four ASCII hexadecimal digits in frames 3–6 give the address at which the data is loaded. The high-order digit is in frame 3, the lower-order digit in frame 6. The first data byte is stored in the location indicated by the load address; successive bytes are stored in successive memory locations. This field in an end-of-file record contains zeros or the starting address of the program.

4. RECORD TYPE FIELD: Frames 7 and 8

   The two ASCII hexadecimal digits in this field specify the record type. The high-order digit is in frame 7. All data records are type 0; end-of-file records are type 1. Other possible values for this field are reserved for future expansion.

5. DATA FIELD: Frames 9 to 9+2*(record length)–1

   A data byte is represented by two frames containing the ASCII characters 0–9 or A–F, which represent a hexadecimal value between 0 and FF (0 and 255 decimal). The high-order digit is in the first frame of each pair. If the data is 4-bit, then either the high or low-order digit represents the data and the other digit of the pair may be any ASCII hexadecimal digit. There are no data bytes in an end-of-file record.

6. CHECKSUM FIELD: Frames 9+2*(record length) to 9+2*(record length)+1

   The checksum field contains the ASCII hexadecimal representation of the two's complement of the 8-bit sum of the 8-bit bytes that result from converting each pair of ASCII hexadecimal digits to one byte of binary, from the record length field to and including the last byte of the data field. Therefore, the sum of all the ASCII pairs in a record after converting to binary, from the record length field to and including the checksum field, is zero.

Intellec Hex Example:

```
: 10310000311A320E03117E31CD40003A9231B7C2EE
: 1031100060310E00117031CD40003A9231B7C2607B
: 10312000312A7E31227A310E03117E31CD40003AB0
: 103130009231B7C260312A8C317CB5CA50310E044D
: 10314000118831CD40003A9231B7C26031C3273186
: 103150000E01117A31CD40000E09119031CD4000A1
: 103160000E0C119231CD40000E09119031CD40006E
: 0A3170007E3196310100000092311B
: 10317C0092310100963180008C31923100009631F1
: 04318E0092319231B7
: 02319400923176
: 00310001CE
```

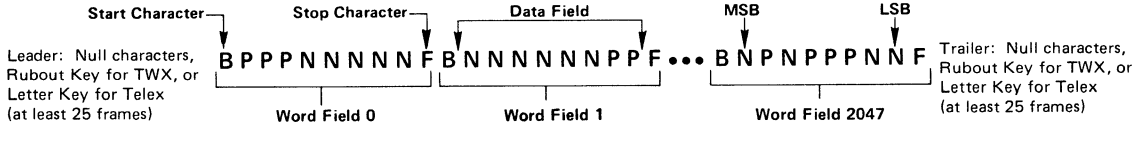

B2. BPNF Paper Tape Format

The format requirements are as follows:

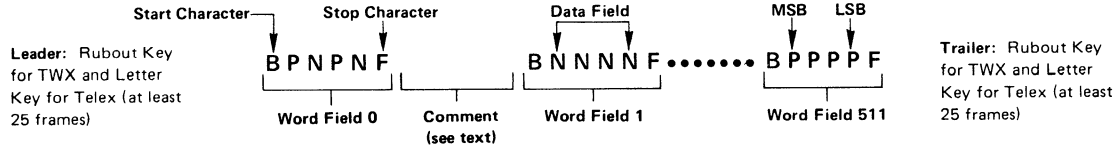
1. All data fields are to be punched in consecutive order, starting with data field 0 (all addresses low). There must be exactly N data fields for a N x 8 or N x 4 device organizations.
2. Each data field must begin with the start character B and end with the stop character F. There must be exactly 8 or 4 data characters between the B and F for a N x 8 or N x 4 organization, respectively.

   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A DATA FIELD. If in preparing a tape an error is made, the entire data field, including the B and F must be rubbed out. Within the data field, a P results in a high level output, and an N results in a low level output.
3. Preceding the first data field and following the last data field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes) or null characters.
4. Between data fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") after each 72 characters. When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the device pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

Example of BPNF 2048 x 8 format (N = 2048):



Example of 512 x 4 format (N = 512):



B3. Non-Intellec Hex Paper Tape Format

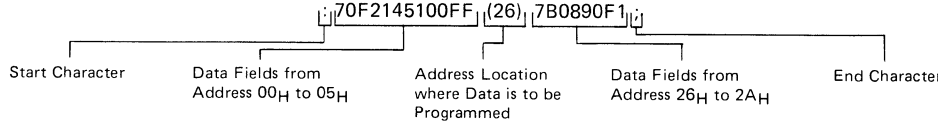
For the non-Intellec Hex Format, a data field can contain either 8 or 4-bit data. *Two* ASCII hexadecimal characters must be used to represent *both* 8 and 4-bit data. In the case of 4-bit data, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form.

Parity is allowed; however, it is not checked. Preceding the first data field and following the last data field there must be a leader/trailer length of at least 25 null characters or rubout punches.

The format requirements are as follows:

1. The start of the first data field is indicated by a colon. After the last data field, a semicolon must be punched to indicate the end. All data fields are to be punched in consecutive order, starting with data field 00_H (all addresses low).
2. *Two* hex characters must be used to represent the data field of both N word x 8-bit and N word x 4-bit devices. For an 8-bit data field, the high order data is represented by the left justified character of the pair. Either character of the pair may be used to represent the word field of a N word x 4-bit device, however, it must be consistent throughout the word field. The other character may be any hex character.

   A field of "don't care" data is allowed. Data after a field of "don't care" will be programmed starting at an address location enclosed in parentheses. In the following example, data is entered in addresses 00_H to 05_H, followed with "don't care" from addresses 06_H to 25_H, data being entered again starting at address location 26_H, and followed with "don't care" data to the last address location.



3. The x character may be used to rubout any erroneous character(s). The # character may be used to rubout an entire line up to the previous carriage return.
4. Spaces are allowed only between *separate* word fields.
5. After each 72 characters, a carriage return followed by a line feed should be punched to allow a print-out of the tape.
6. Comments must be placed only between the tape leader and the start of the first data field.

C. Computer Punched Card Format

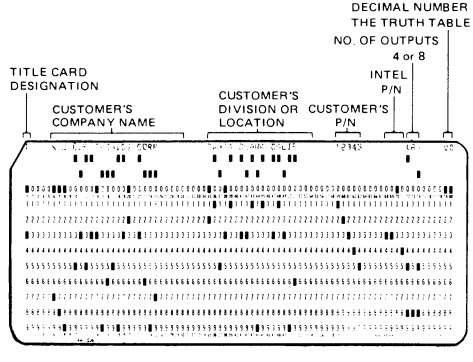
The following general format is applicable to the programming information sent on computer punched cards:

1. An 80 column Hollerith card (interpreted) punched on an IBM 026 or 029 keypunch should be submitted.
2. A single deck must consist of a Title Card followed by the data cards. There will be N/8 or N/14 data cards for N words x 8-bit and N words x 4-bit devices, respectively, in the PN format.

   For the Intellec Hex format, there will be N/32 data cards for both N words x 8-bit and N words x 4-bit devices, and one end of file card.

C1. Intellec Hex Computer Punched Card Format

Two hex characters must be used to represent data for both a N word x 8-bit and N word x 4-bit device. For the latter, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form. The entire data field for all bits must be punched even if it is "don't care".



Column	Data
1	Punch a T
2–3	Blank
4–28	Customer Company Name
29–30	Blank
31–50	Customer's Company Division or location
51–52	Blank
53–61	Customer Part Number
62–63	Blank
64–72	Punch the Intel 4-digit basic part number and in ( ) the number of output bits; e.g., 2708 (8), 2316 (8), or 3605 (4)
73–74	Blank
75–76	Chip number for ROMs with programmable chip select inputs. If not applicable, leave blank.
77–78	Blank
79–80	Punch a 2-digit decimal number to indicate truth table number. The first truth table will be 00, second 01, third 02, etc.

a. N word x 8-bit device

Column	Data
1	Record mark: A colon is used to signal the start of a record.
2–3	Record length: This is the count of the actual data bytes in the record. Column 2 contains the high order digit of the count, Column 3 contains the low order digit. A record length of zero indicates end of file. All frames containing data will have a maximum record length of 10_{Hex} bytes (32 decimal).
4–7	Load address: The four characters starting addresses at which the following data will be loaded. The high order digit of the load address is in Column 4 and the low order digit is in Column 7. The first data byte is stored in the location indicated by the load address. Successive data bytes are stored in successive memory locations. ROMs containing more than 32 bytes of data will use two or more records or cards to transmit the data. Although the load address for the beginning record need not be 0000, each subsequent load address should be "10_H" (32 decimals) greater than the last.
8–9	Record type: A 2-digit code in this field specifies the type of this record. The high order digit of this code is located in Column 8. Currently, all data records are type 0. End-of-file records will be type 1; they are distinguished by a zero RECORD LENGTH field (see above). Other possible values for this field are reserved for future expansion.
10–73	Data
75–75	Checksum: Same as paper tape format.
76–78	Blank
79–80	Punch same 2-digit decimal number as in Title Card.

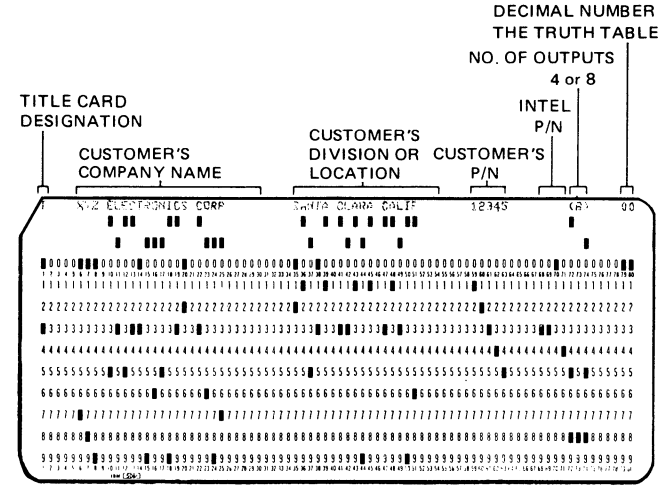
b. N word x 4-bit device

This format is identical to the previously documented 8-bit hexadecimal format with the following exceptions:

Column	Data
10–73	Each memory location is represented by two columns containing the characters 0–9, A–F. Since this is 4-bit data, the user must indicate which character of each pair is to be used as valid data. A single deck must be submitted without mixing first and second characters of the pair.

C2. PN Computer Punched Card Format

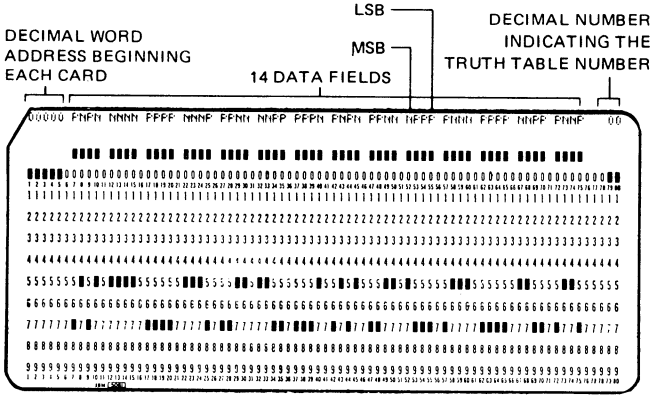
A word field consists of only P's and N's. A punched P will result in an output high level and a punched N in an output low level. The B and F characters, unlike the paper tape format, are illegal characters. The entire data field for all bits must be punched even if it is "don't care". The data field must begin in consecutive order, starting with address 0 (all addresses logically low).



Column	Data
1	Punch a T
2–3	Blank
4–28	Customer Company Name
29–30	Blank
31–50	Customer's Company Division or location
51–52	Blank
53–61	Customer Part Number
62–63	Blank
64–72	Punch the Intel 4-digit basic part number and in ( ) the number of output bits; e.g., 2708 (8), 2316 (8), or 3605 (4)
73–74	Blank
75–76	Chip number for ROMs with programmable chip select inputs. If not applicable, leave blank.
77–78	Blank
79–80	Punch a 2-digit decimal number to indicate truth table number. The first truth table will be 00, second 01, third 02, etc.

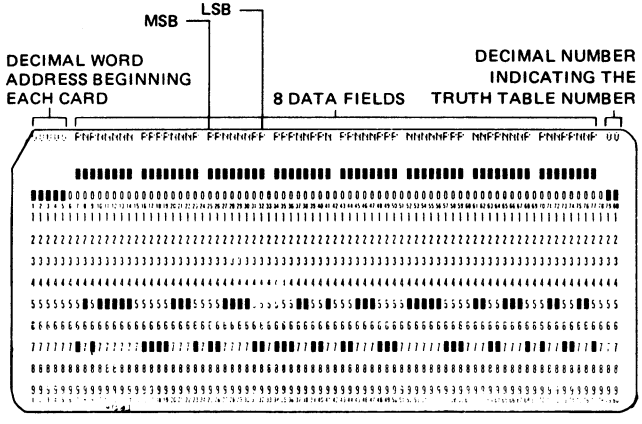
Title Card Format.

For a N words X 4-bit organization only, cards 2 and those following should be punched as shown. Each card specifies the 4-bit output of 14 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØ14, ØØØ28, etc.
6	Blank
7-10	Data Field
11	Blank
12-15	Data Field
16	Blank
17-20	Data Field
21	Blank
22-25	Data Field
26	Blank
27-30	Data Field
31	Blank
32-35	Data Field
36	Blank
37-40	Data Field
41	Blank
42-45	Data Field
46	Blank
47-50	Data Field
51	Blank
52-55	Data Field
56	Blank
57-60	Data Field
61	Blank
62-65	Data Field
66	Blank
67-70	Data Field
71	Blank
72-75	Data Field
76-78	Blank
79-80	Punch same 2 digit decimal number as in title card.

For a N words X 8-bit organization only, cards 2 and those following should be punched as shown. Each card specifies the 8-bit output of 8 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØØ8, ØØØ16, etc.
6	Blank
7-14	Data Field
15	Blank
16-23	Data Field
24	Blank
25-32	Data Field
33	Blank
34-41	Data Field
42	Blank
43-50	Data Field
51	Blank
52-59	Data Field
60	Blank
61-68	Data Field
69	Blank
70-77	Data Field
78	Blank
79-80	Punch same 2 digit decimal number as in title card.

D. Custom PROM/ROM Order Forms

All orders for PROMs/ROMs which are to be electrically or mask programmed at Intel must be submitted with the order forms shown on the following pages. Additional forms are available from Intel Literature Department, 3065 Bowers Ave., Santa Clara, California 95051. The ROM Order Forms for the 4001 and 4308 are shown on pages 8-97 and 8-108, respectively.

The order forms for the individual PROMs/ROMs are listed in Table II below.

Table II

PROM/ROM Part Number	Order Form Number
MOS EPROMs	A
8748, 8755	A
2316E, 8316A, 8316AL	B
8048	C
8308	D
8355	E
Bipolar PROMs/ROMs	F

CUSTOMER EPROM ORDER FORM A

1702A/4702A/8702A Family
2708/8708/2704 Family
2716, 8748, 8755

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Intel Device P/N _____

For Intel Use Only

S# _____

STD _____

APP _____

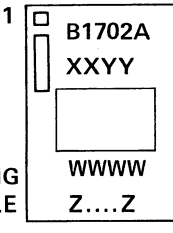
Date _____

All custom MOS EPROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel Logo, the product and package type (B1702A), the 4-digit Intel pattern number (WWWW), an internal manufacturing traceability code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.

1702A MARKING EXAMPLE



CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	**Intel Pattern Number** (Please Do Not Use)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		

CUSTOMER 16K ROM ORDER FORM B

Company _____ Phone #_____

Company Contact _____ Date_____

P.O. #_____ Intel P/N & Pkg _____

For Intel Use Only

S#_____

STD_____

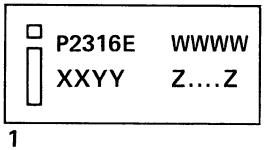
APP_____

Date_____

A custom 16K ROM order must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel Logo, the product and package type (P2316E), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



1

P2316E MARKING EXAMPLE

IMPORTANT MASK OPTION SPECIFICATION

The chip select inputs are mask programmable and must be specified by the user. The chip select logic levels must be specified with one of the below Chip Numbers. The Chip Number will be coded in terms of positive logic where a logic "1" is a high level input. It should be noted that Chip Number 4 for the 2316E is compatible to Intel's 2716 EPROM.

Chip Number	CS3	CS2	CS1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

CUSTOMER PART NUMBER

Customer P/N (Please Fill-In)	Chip Number (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
	1	1
	2	2
	3	3
	4	4
	5	5
	6	6
	7	7
	8	8
	9	9
	10	10
	11	11

CUSTOMER 8048 ROM ORDER FORM C

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Package Type: ☐ Plastic ☐ Cerdip

For Intel Use Only

S# _____

STD _____

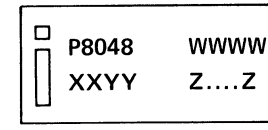
APP _____

Date _____

All custom 8048 orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (P8048), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



1

P8048 MARKING EXAMPLE

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		

CUSTOMER 8308 ROM ORDER FORM D

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Intel P/N & Pkg _____

For Intel Use Only

S# _____

STD _____

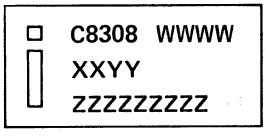
APP _____

Date _____

All custom 8308 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel logo, the product type (C8308), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and a maximum 9-digit number (Z....Z) which is specified by the user. The 9-digit number may be a part number or the 8308 chip number.



1

C8308 MARKING EXAMPLE

IMPORTANT MASK OPTION SPECIFICATION

The CS_2 chip select input is mask programmable and must be specified by the user. The chip select logic level must be specified with one of the below Chip Numbers. The Chip Number will be coded in terms of positive logic where a "1" is a high level input.

Chip Number	$\overline{CS}_1$ (non-programmable)	CS_2 (programmable)
0	0	0
1	0	1

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Chip Number (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			

CUSTOMER 8355 ROM ORDER FORM E

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Package Type: ☐ Plastic ☐ Cerdip

For Intel Use Only

S# _____

STD _____

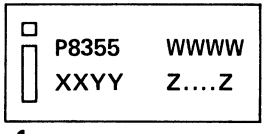
APP _____

Date _____

All custom 8355 orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats described in the Programming Instruction sectin of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (P8355), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



1

P8355 MARKING EXAMPLE

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1		
2		
3		
4		
5		
6		
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18		
19		
20		

CUSTOMER BIPOLAR PROM/ROM ORDER FORM
F

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Intel Device P/N _____

For Intel Use Only

S# _____

STD _____

APP _____

Date _____

All custom bipolar PROM/ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

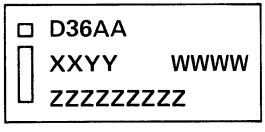
IMPORTANT HEX AND INTELLEC HEX FORMAT INFORMATION

A word field must be 8 bits in the hex format. Consequently for N words by 4-bit devices such as the 3605, it is important that you indicate by checking the box below whether the submitted tape or card deck for programming is right or left justified.

☐ Right Justified ☐ Left Justified

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (D36AA), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



1

D36AA MARKING EXAMPLE

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1		
2		
3		
4		
5		
6		
7		
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II. MOS EPROMs

A. Erasure Procedure

As stated in the EPROM related data sheets, the recommended erasure procedure to use with EPROMs is to illuminate the window with a UV lamp which has a wavelength of 2537 Angstroms (Å). The data sheets specify a distance of 1 inch and erase times of 10–45 minutes, depending on the type of device and UV lamp. Actually, the amount of time required to erase a device can be concisely stated in terms of the amount of UV energy incident to the window, expressed in Watt-seconds per square centimeter (W-sec/cm^2). Table III lists the required integrated dosgae (UV intensity X exposure time) for the EPROMs currently in production by Intel.

Table III. Required Erase Energy for Device Types

Device Type	2537Å Erase Energy
1702A/4702A	6 W-sec/cm^2
2708/8708	15 W-sec/cm^2
2716	15 W-sec/cm^2
8748	15 W-sec/cm^2
8755	15 W-sec/cm^2

The erase energy expressed in Table III includes a guardband to ensure complete erasure of all bits. *It is not sufficient to monitor "first bit" erasure to determine erasure time, as some other bits in the array may not be erased.*

A1. UV Sources

There are several models of UV lamps that can be used to erase EPROMs (see Table IV). The model numbers in the table refer to lamps manufactured by Ultra Violet Products of San Gabriel, California. In addition, there are several other manufacturers, including Data I/O (Issaquah, Wash.), PROLOG (Monterey, Calif.). Prometrics (Chicago, Ill.), and Turner Designs (Mt. View, Calif.). The individual manufacturers should be consulted for detailed product descriptions. Also shown in the table are typical erase times for various combinations of Intel PROMs and lamp intensities.

Table IV.

Model	Power Rating	Minimum Erase Time for Indicated Dosage Without a Filter Over the Bulb	
		6 W-sec 1702A, 4702A	15 W-sec 2708, 8708, 8755 2716, 8748
R-52	13000 μW/cm^2	7.7 min	19.2 min
S-52	12000 μW/cm^2	8.3 min	20.7 min
S-68	12000 μW/cm^2	8.3 min	20.7 min
UVS-54	5700 μW/cm^2	17.5 min	43.8 min
UVS-11	5500 μW/cm^2	18.2 min	45.6 min

According to the manufacturers, the output of the UV lamp bulbs decrease with age. The output of the lamp should be verified periodically to ensure that adequate intensities are maintained. If this is not done, bits may be partially erased which will interfere with later programming and/or operation at high temperature.

For lamps other than those listed, the erase time can be determined by using a UV intensity meter, such as the Ultra Violet Products Model J-225. When a meter is used, the intensity should be measured at the same position (distance from the lamp) as the EPROMs to be erased. This will require careful positioning to insure that the sensor will receive the same amount of UV light that the window of the EPROM will receive.

The sensors used with most UV intensity meters show reduced output with constant exposure to UV light. Therefore, they should not be permanently placed inside the erasure enclosure, they should only be used for periodic measurements.

B. 1702A/1702AL Family Programming

The 1702A/1702AL is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity X exposure time) is 6 W-sec/cm^2. An example of an ultraviolet source which can erase the 1702A/1702AL in 10 to 20 minutes is the Model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the PROM should be placed within 1 inch away from the lamp tubes.

Initially, all 2048 bits of the PROM are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode. All 8 address bits must be in the binary complement state when pulsed V_{CC} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25 μsec after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10 μsec before the program pulse is applied. The addresses should be programmed in the sequence 0 through 255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the 8 bits of each word. A low data input level (–48V) will program a "1" and a high data input level (ground) will leave a "0". All 8 bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals. See page 2 of the data sheet for required pin connections during programming.

1702A, 1702AL

D.C. and Operating Characteristics for Programming Operation

T_A = 25°C, V_{CC} = 0V, V_{BB} = + 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI1P}	Address and Data Input Load Current			10	mA	V_{IN} = -48V
I_{LI2P}	Program and V_{GG} Load Current			10	mA	V_{IN} = -48V
I_{BB}[1]	V_{BB} Supply Load Current		10		mA	
I_{DDP}[2]	Peak I_{DD} Supply Load Current		200		mA	V_{DD} = V_{PROG} = -48V, V_{GG} = -35V
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	-46		-48	V	
V_{IL2P}	Address Input Low Voltage	-40		-48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	-46		-48	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	-35		-40	V	

Notes: 1. The V_{BB} supply must be limited to 100mA max. current to prevent damage to the device.
2. I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μsec. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.

1702A, 1702AL
A.C. Characteristics for Programming Operation

$T_{AMBIENT}$ = 25°C, V_{CC} = 0V, V_{BB} = + 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

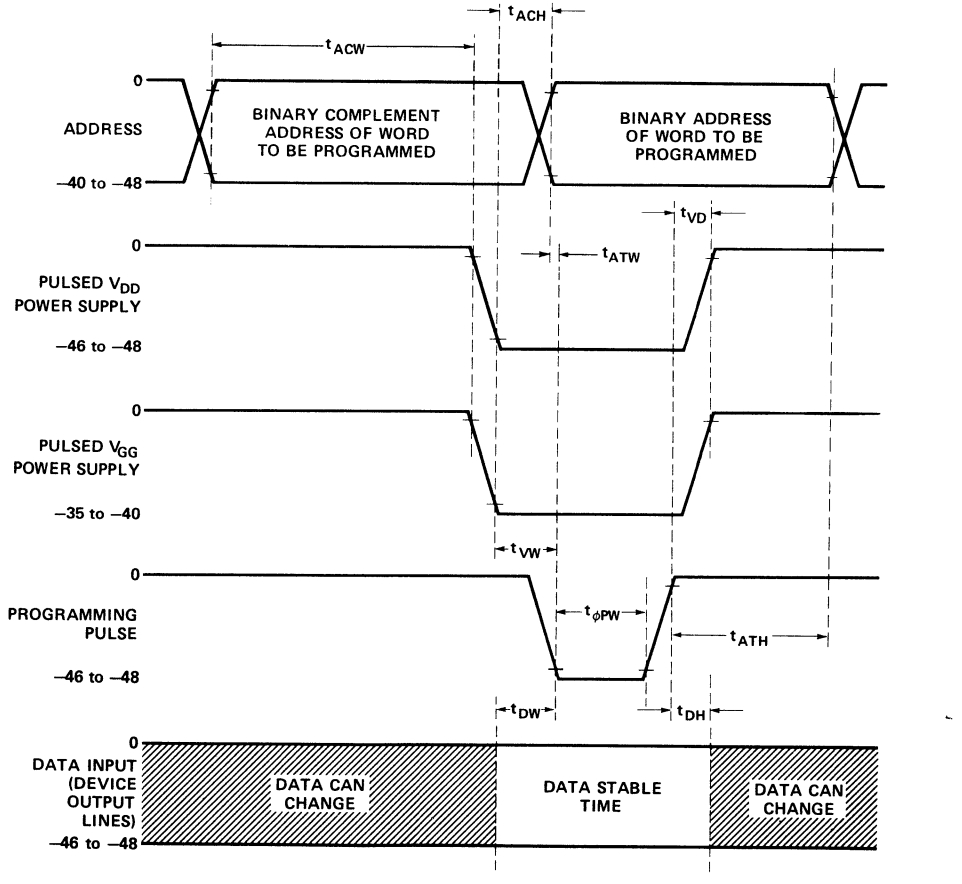
Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
	Duty Cycle (V_{DD}, V_{GG})			20	%	
$t_{\phi PW}$	Program Pulse Width		2	3	ms	V_{GG} = -35V, V_{DD} = V_{PROG} = -48V
t_{DW}	Data Set-Up Time	25			μs	
t_{DH}	Data Hold Time	10			μs	
t_{VW}	V_{DD}, V_{GG} Set-Up	100			μs	
t_{VD}	V_{DD}, V_{GG} Hold	10		100	μs	
t_{ACW}	Address Complement Set-Up	25			μs	
t_{ACH}	Address Complement Hold	25			μs	
t_{ATW}	Address True Set-Up	10			μs	
t_{ATH}	Address True Hold	10			μs	

PROGRAM WAVEFORMS

Conditions of Test:

Input pulse rise and fall times ≤ 1μsec

$\overline{CS}$ = 0V



C. 2708/2704 Family Programming

Initially, and after each erasure, all 8192/4096 bits of the 2708/2704 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the CS/WE input (pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8 bits in parallel, to the data output lines (O_1–O_8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to N x t_{PW} $\geqslant$ 100 ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops throuhg all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The CS/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{ILL}) when CS/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Examples (Using N x t_{PW} $\geqslant$ 100 ms)

Example 1: All 8096 bits are to be programmed with a 0.5 ms program pulse width.

The minimum number of program loops is 200. One program loop consists of words 0 to 1023.

Example 2: Words 0 to 100 and 500 to 600 are to be programmed. All other bits are "don't care". The program pulse width is 0.75 ms.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's.

Example 3: Same requirements as example 2, but the PROM is now to be *updated* to include data for words 750 to 770.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's. Addresses 0 to 100 and 500 to 600 must be re-programmed with their original data pattern.

2704, 2708
PROGRAM CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

D.C. Programming Characteristics

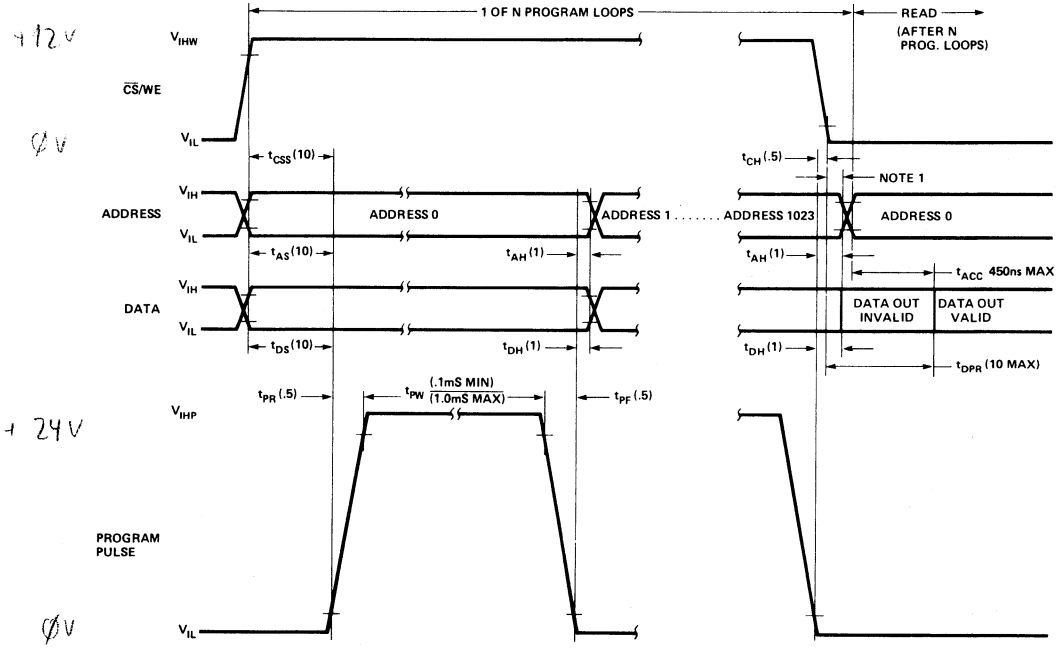
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Address and $\overline{CS}$/WE Input Sink Current			10	μA	V_{IN} = 5.25V
I_{IPL}	Program Pulse Source Current			3	mA	
I_{IPH}	Program Pulse Sink Current			20	mA	
I_{DD}	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents: All Inputs High $\overline{CS}$/WE = 5V; T_A = 0°C
I_{CC}	V_{CC} Supply Current		6	10	mA	
I_{BB}	V_{BB} Supply Current		30	45	mA	
V_{IL}	Input Low Level (except Program)	V_{SS}		0.65	V	
V_{IH}	Input High Level for all Addresses and Data	3.0		V_{CC}+1	V	
V_{IHW}	$\overline{CS}$/WE Input High Level	11.4		12.6	V	Referenced to V_{SS}
V_{IHP}	Program Pulse High Level	25		27	V	Referenced to V_{SS}
V_{ILP}	Program Pulse Low Level	V_{SS}		1	V	V_{IHP} - V_{ILP} = 25V min.

A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	$\overline{CS}$/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	$\overline{CS}$/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	.5		2.0	μs

NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

2704, 2708
Programming Waveforms



NOTE 1. THE $\overline{CS}$/WE TRANSITION MUST OCCUR AFTER THE PROGRAM PULSE TRANSITION AND BEFORE THE ADDRESS TRANSITION.

NOTE 2. NUMBERS IN ( ) INDICATE MINIMUM TIMING IN μS UNLESS OTHERWISE SPECIFIED.

D. 2716 Programming

Initially, and after each erasure, all 16,384 bits of the 2716 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 2716 is programmed by applying a 50 ms, TTL programming pulse to the PD/PGM pin with the $\overline{CS}$ input high and the V_{PP} supply at 25V ±1V. Any location may be programmed at any time – either indvidually, sequentially, or randomly. The programming time for a single bit is only 50 ms and for all 16,384 bits is approximately 100 sec. The detailed programming specifications and timing waveforms are given in the following tables and figures.

CAUTION: The V_{CC} and V_{PP} supplies must be sequenced on and off such that V_{CC} is applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} to prevent damage to the 2716. The maximum allowable voltage during programming which may be applied to the V_{PP} with respect to ground is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding the 26-volt maximum specification. For convenience in programming, the 2716 may be verified with the V_{PP} supply at 25V ±1V. During normal read operation, however, V_{PP} must be at V_{CC}.

2716 PROGRAM CHARACTERISTICS (1)

T_A = 25°C ±5°C, V_{CC}[2] = 5V ±5%, V_{PP}[2,3] = 25V ±1V

D.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Current (for Any Input)			10	μA	V_{IN} = 5.25V/0.45
I_{PP1}	V_{PP} Supply Current			5	mA	PD/PGM = V_{IL}
I_{PP2}	V_{PP} Supply Current During Programming Pulse			30	mA	PD/PGM = V_{IH}
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	-0.1		0.8	V	
V_{IH}	Input High Level	2.2		V_{CC}+1	V	

A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	
t_{AS}	Address Setup Time	2			μs	
t_{CSS}	$\overline{CS}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{CSH}	$\overline{CS}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns	PD/PGM = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTES:
1. Intel's standard product warranty applies only to devices programmed to specifications described herein.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The 2716 must not be inserted into or removed from a board with V_{PP} at 25 ±1V to prevent damage to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

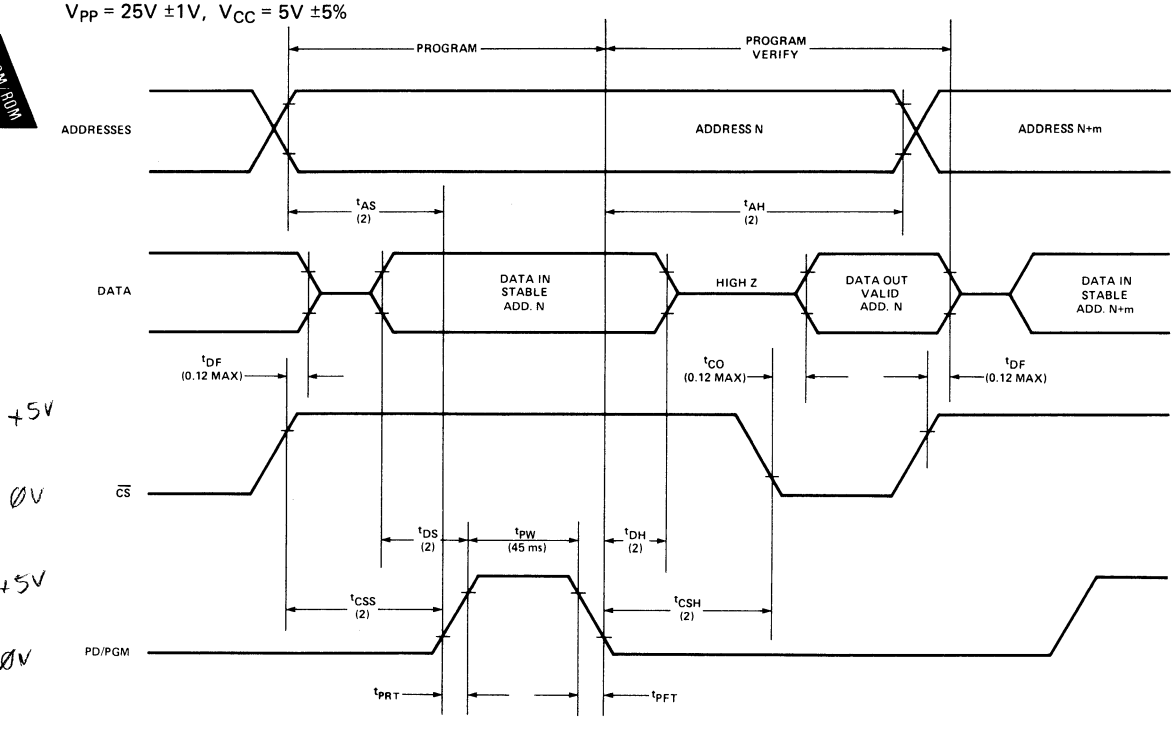
A.C. Conditions of Test:

V_{CC} . . . . . 5V ±5%
V_{PP} . . . . . 25V ±1V
Input Rise and Fall Times (10% to 90%) . . . . . 20 ns

Input Pulse Levels . . . . . 0.8V to 2.2V
Input Timing Reference Level . . . . . 1V and 2V
Output Timing Reference Level . . . . . 0.8V and 2V

PROGRAMMING WAVEFORMS

V_{PP} = 25V ±1V, V_{CC} = 5V ±5%



NOTE: ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE μSEC UNLESS OTHERWISE NOTED.

E. 8748/8755 Programming

Initially, and after each erasure, all bits of the EPROM portions of the 8748 and 8755 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The EPROM portions of the 8748 and 8755 are programmed on the Intel® Universal PROM Programmer (UPP). The UPP and its related personality cards for the 8748 and 8755 are described beginning on page 13-45 of this catalog.

III. BIPOLAR PROM PROGRAMMING

A. 3621, 2K, 4K, and 8K PROM Programming

All Intel bipolar PROMs except for the 3601/3601-1 are programmed with the algorithm described below. (The 3601/3601-1 programming algorithm is described in the below Section IIIB.) This algorithm was developed specifically to program the 3602A/3622A, 3604A/3624A, 3605/3625, and 3608/3628. *The algorithm described in this section must be used on the aforementioned PROMs to insure properly and reliably programmed fuses.* This algorithm may also be used to program the 3621, 3602/3622, and 3604/3624 PROM families. It is preferred over previously published Intel algorithms for these PROMs for increased programming yields.

Initially, all bits are in a logic 1 (high) state. To program a bit to a logic 0 (low) state, it is necessary to force 5 mA into the output to be programmed. A series of program pulses must also be applied to the V_{CC} power supply and to any one of the logically low true chip select ($\overline{CS}$) inputs. The logic level of the other chip selects, in the case of PROMs with multiple chip selects, should be such that the PROM is selected during verification.

Program pulses are applied to all outputs of a word in a cycle time. The program pulses are multiplexed during a cycle time to each output of the word to be programmed. If desired, a N word by 8-bit PROM may have its words programmed in two separate groups — the four lower order bits (O_1 to O_4) and the four higher order bits (O_5 to O_8). The operation in this manner is the same as for a N word by 4-bit PROM. For fastest programming time, it is preferred that all eight outputs be programmed at the same time.

The programming specifications are given in Table V and the programming waveforms are shown in Figure 1. The programming procedure (described with nominal specifications) is as follows:

1. A 5 mA current must be forced into the output to be programmed by a current source. The current source must be clamped to V_{CC} by a silicon diode. All the other outputs must be floating until it is their turn for programming. The V_{CC} power supply and the chip select ($\overline{CS}$) input is pulsed as shown in Figures 1 and 2. The width of V_{CC} is linearly increased from 0.2 μs to 8 μs according to the ramp time shown in Figure 3. The total ramp time for a group of four outputs is 180 ms and 360 ms for a group of eight outputs.

   The V_{CC} program pulses are multiplexed during a cycle time to the outputs of the word to be programmed. The cycle time (t_{CYC}) between the V_{CC} program pulses to the same output will increase as the V_{CC} program pulse width increases from 0.2 μs to 8 μs. The time (t_D) between V_{CC} pulses of two different outputs is constant at 1.8 μs.

2. All outputs must be continuously monitored for programming verification. This verification must occur after V_{CC} has been at 4.5V for 90% of t_D and prior to V_{CC} rising to 12.5V. The program/verification cycles must still be applied (with the pulse width still linearly increasing to a maximum of 8 μs) even though the output has been sensed as being programmed. An additional 128 verifications (i.e., 128 program/verify cycles) on each output must be obtained to insure a correctly programmed output. This additional 128 verification is a minimum number and must occur *after* all the bits of the word are sensed as being programmed. Please refer to Figure 1 for the timing waveforms.

   More than 128 program/verify cycles may be required to achieve the 128 verifications on each bit. The cycles should still continue even if one bit fails, since the verifications are not required to be in consecutive sequence. After the 128 verifications have occurred for all bits, a final V_{CC} and CS pulse at a width of 2.5 ms is simultaneously applied to all outputs. Programming should cease if the 128 verifications are not achieved in 800 ms.
3. A 4 mA ±50% current must also be forced into CS_3 (pin 19) of the 3608/3628 family and into CS_4 (pin 18) of the 3604A/3624A family during programming. If desired for commonality the 4 mA may also be forced into CS_4 of the 3604/3624 family.
4. The 4 mA current into the chip select input may be easily accomplished by using a 1.2K resistor connected to a +15V power supply. The voltage on the chip select input will be approximately 10V with the 1.2K resistor.

Table V. Programming Characteristics

$T_A = 25°C$

Symbol	Parameter	Limits Min.	Nom.	Max.	Units	Conditions
V_{IH1}	V_{CC} Program Pulse Amplitude	12	12.5	13	V	
V_{IH2}	$\overline{CS}$ Program Pulse Amplitude	3	5	5.5	V	
V_{IL1}	V_{CC} During Verify	4.25	4.5	4.75	V	
V_{IH2}	$\overline{CS}$ During Verify	0	0.2	0.4	V	
t_{PW1}	V_{CC} Pulse Width at Beginning of Pulse Train	160	200	240	ns	Measured at 12V
t_{PW2}	V_{CC} Pulse Width at End of Pulse Train	7.2	8	8.8	μs	Measured at 12V
T_{CSS}	Chip Select Setup Time	0			ns	Measured from 1.5V on rising edge of $\overline{CS}$ to 5.0V on rising edge of V_{CC}
T_{CSH}	Chip Select Hold Time	100			ns	Measured from 5.0V on falling edge of V_{CC} to 1.5V on falling edge of $\overline{CS}$
T_R	V_{CC} Rise Time	300	400	500	ns	Measured from 5V to 12V on V_{CC}
T_F	V_{CC} Fall Time	50	100	200	ns	Measured from 12V to 5V on V_{CC}
T_{CYC}	Time Between Pulses to Same Output	9	10		μs	Measured at 5V on V_{CC}
T_{OP}	DC Program Time After Verification Has Been Obtained	2.2	2.5	2.8	ms	Measured at 12V
T_D	Time Between V_{CC} Pulses to Successive Outputs	1.5	1.8		μs	Measured at 5V on V_{CC}
T_{RAMP}	Time During Which V_{CC} Pulse Width is Increased Linearly from t_{PW1} to t_{PW2} — 4 outputs	160	180	200	ms	
	— 8 outputs	320	360	400		
I_{CS}	Current to CS_3 of 3608/3628 or to CS_4 of 3604A/3624A	2	4	6	mA	CS_3 or CS_4 should be driven with a 1.2K resistor from a 15V power supply

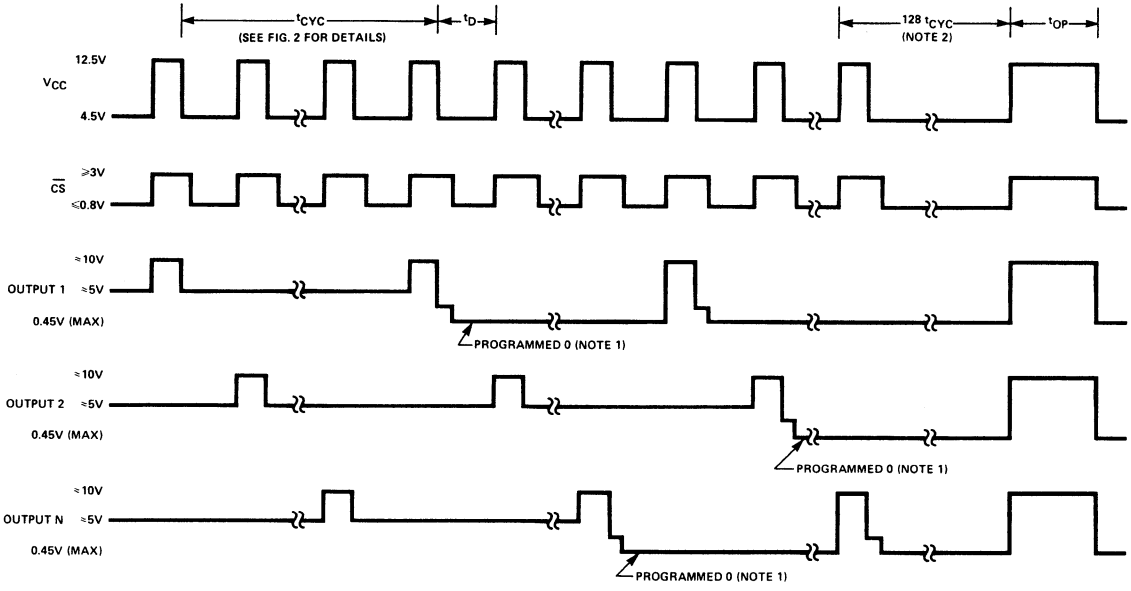


Figure 1. Programming Cycles.

NOTES: 1. PROGRAM VERIFICATION MUST OCCUR AFTER V_{CC} HAS BEEN AT 4.5V FOR 90% OF t_D AND PRIOR TO V_{CC} RISING TO 12.5V. THE PROGRAMMED OUTPUT IS ≤0.45V WHEN $\overline{CS}$ ≤0.8V AND FLOATING WHEN $\overline{CS}$ ≥ 3V.

2. AFTER THE LAST BIT HAS BEEN PROGRAMMED, 128 ADDITIONAL VERIFICATIONS ARE REQUIRED FOR EACH OUTPUT TO BE CORRECTLY PROGRAMMED.

3. AFTER THE 128 PROGRAM VERIFICATIONS, A FINAL 2.5 ms V_{CC} AND $\overline{CS}$ PULSE SHOULD BE APPLIED WHILE SIMULTANEOUSLY ENABLING THE CURRENT SOURCES TO ALL OUTPUTS WHICH ARE TO BE PROGRAMMED.

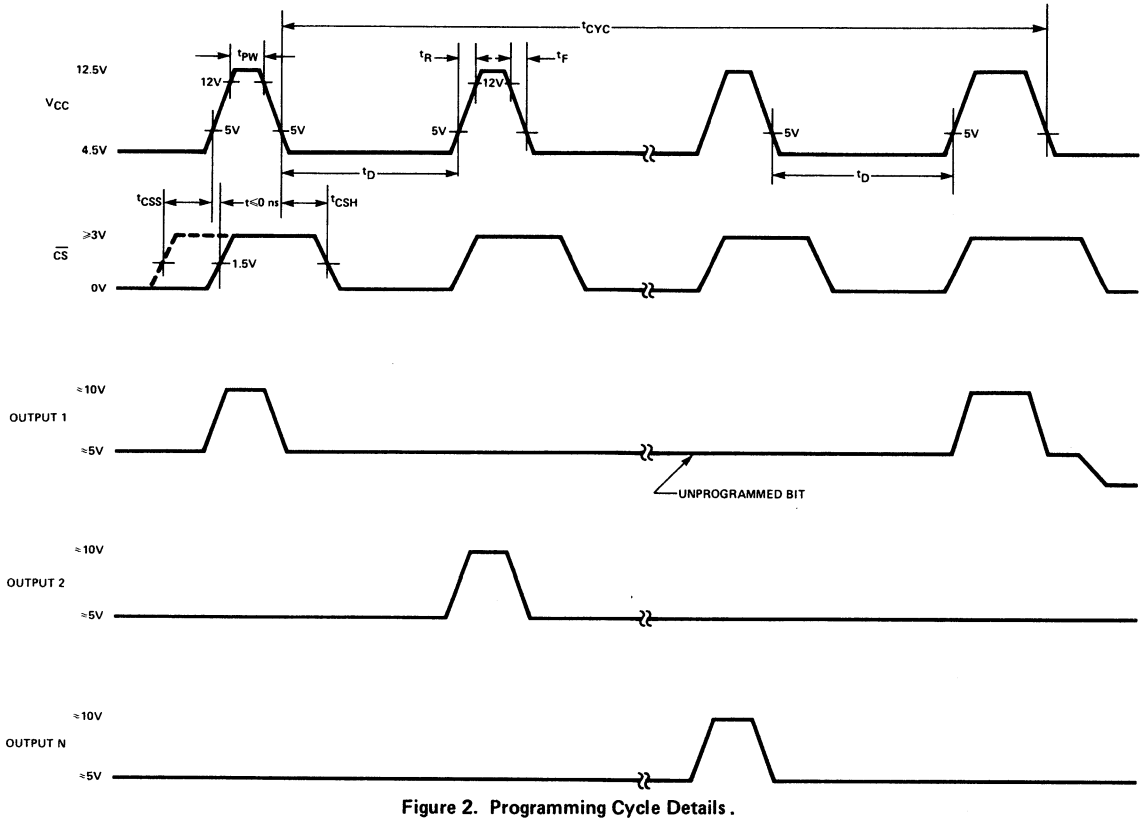


Figure 2. Programming Cycle Details.

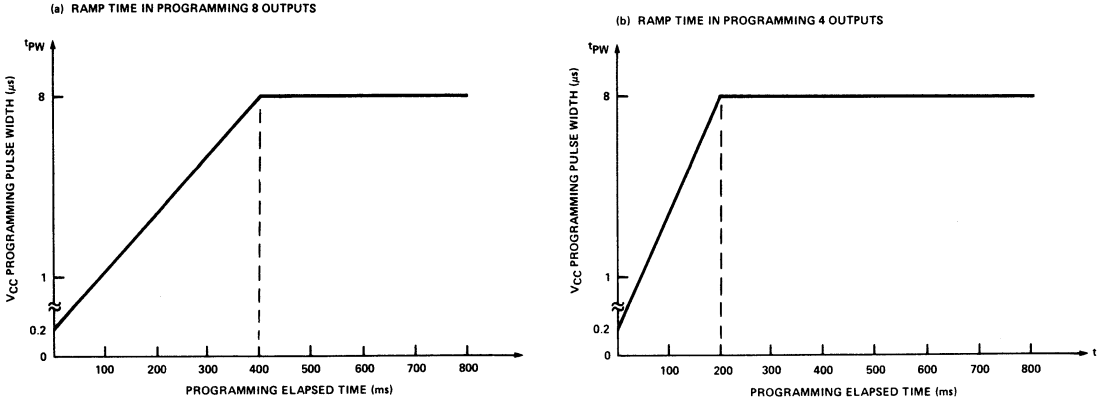


Figure 3. V_{CC} Pulse Width vs. Programming Time.

B. 3601 Programming

The 3601 may be programmed using the basic circuit of Figure 1. Address inputs are at standard TTL levels. Only one output may be programmed at a time. The output to be programmed must be connected to V_{CC} through a 300Ω resistor. This will force the proper programming current (3–6 mA) into the output when the V_{CC} supply is later raised to 10V. All other outputs must be held at a TTL low level (0.4V).

The programming pulse generator produces a series of pulses to the 3601 V_{CC} and CS_2 leads. V_{CC} is pulsed from a low of 4.5 ±0.25V to a high of 10 ±0.25V, while CS_2 is pulsed from a low of ground (TTL logic 0) to a high of 15 ±0.5V. It is important to accurately maintain these voltage levels, otherwise, improper programming may result. The pulses applied must maintain a duty cycle of 50 ±10% and start with an initial width of 1 (±10%) μs, and increase linearly over a period of approximately 100 ms to a maximum width of 8 (±10%) μs. Typical devices have their fuse blown within 1 ms, but occasionally a fuse may take up to 400 ms. During the application of the program pulse, current to CS_2 must be limited to 100 mA. The output of the 3601 is sensed when CS_2 is at a TTL low level output. A programmed bit will have a TTL high output. After a fuse is blown, the V_{CC} and CS_2 pulse trains must be applied for another 500 μs. The characteristics of the pulse train are shown in Figure 2.

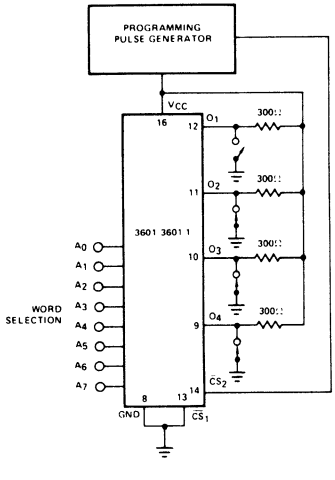


Figure 4. 3601 Programming.

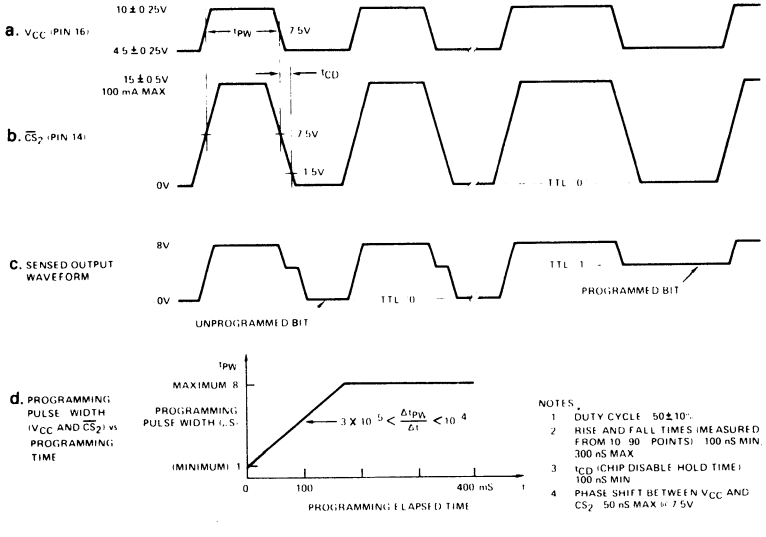


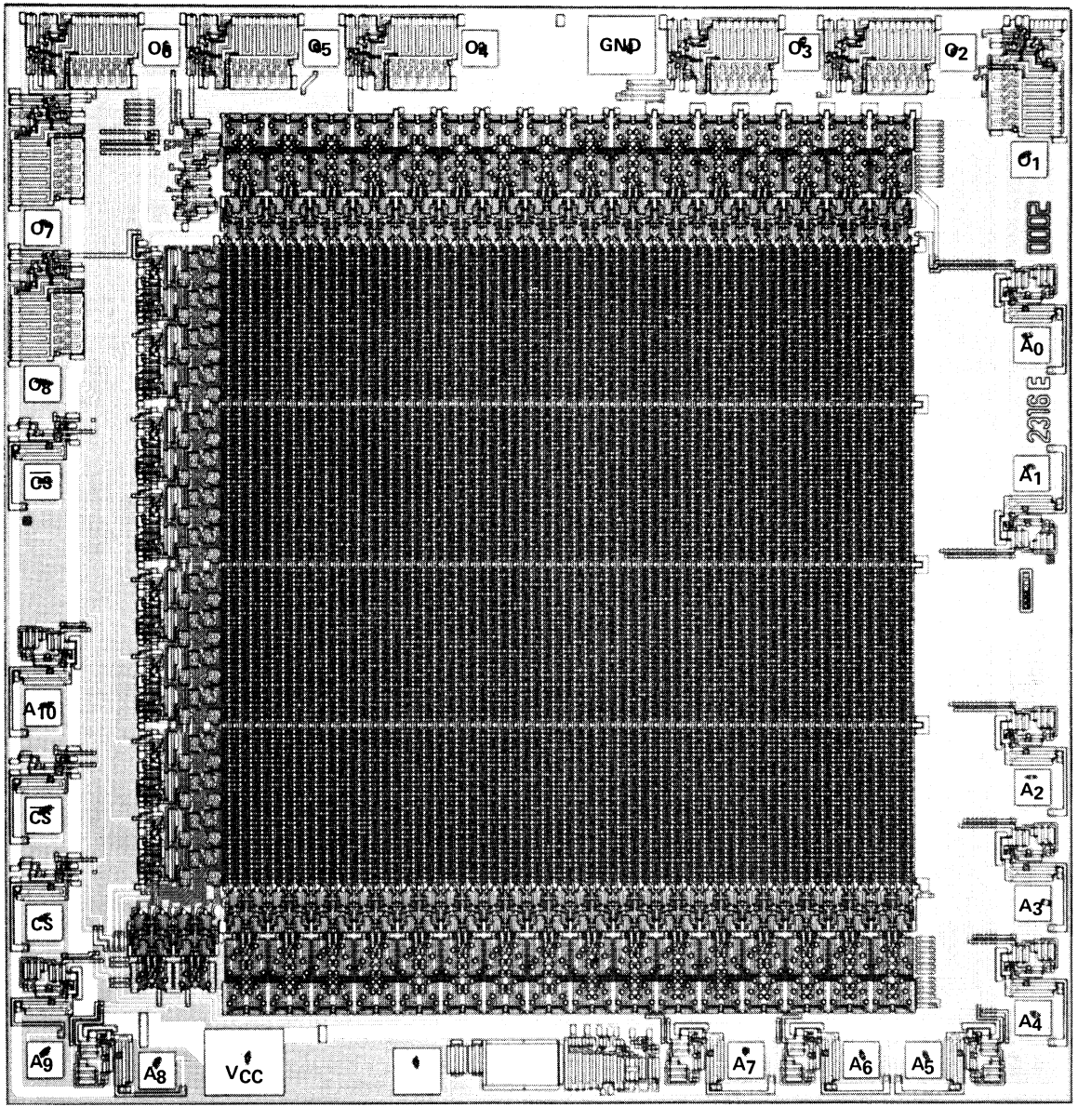
Figure 5. Pulses During Programming.

MOS EPROM AND BIPOLAR PROM LITERATURE

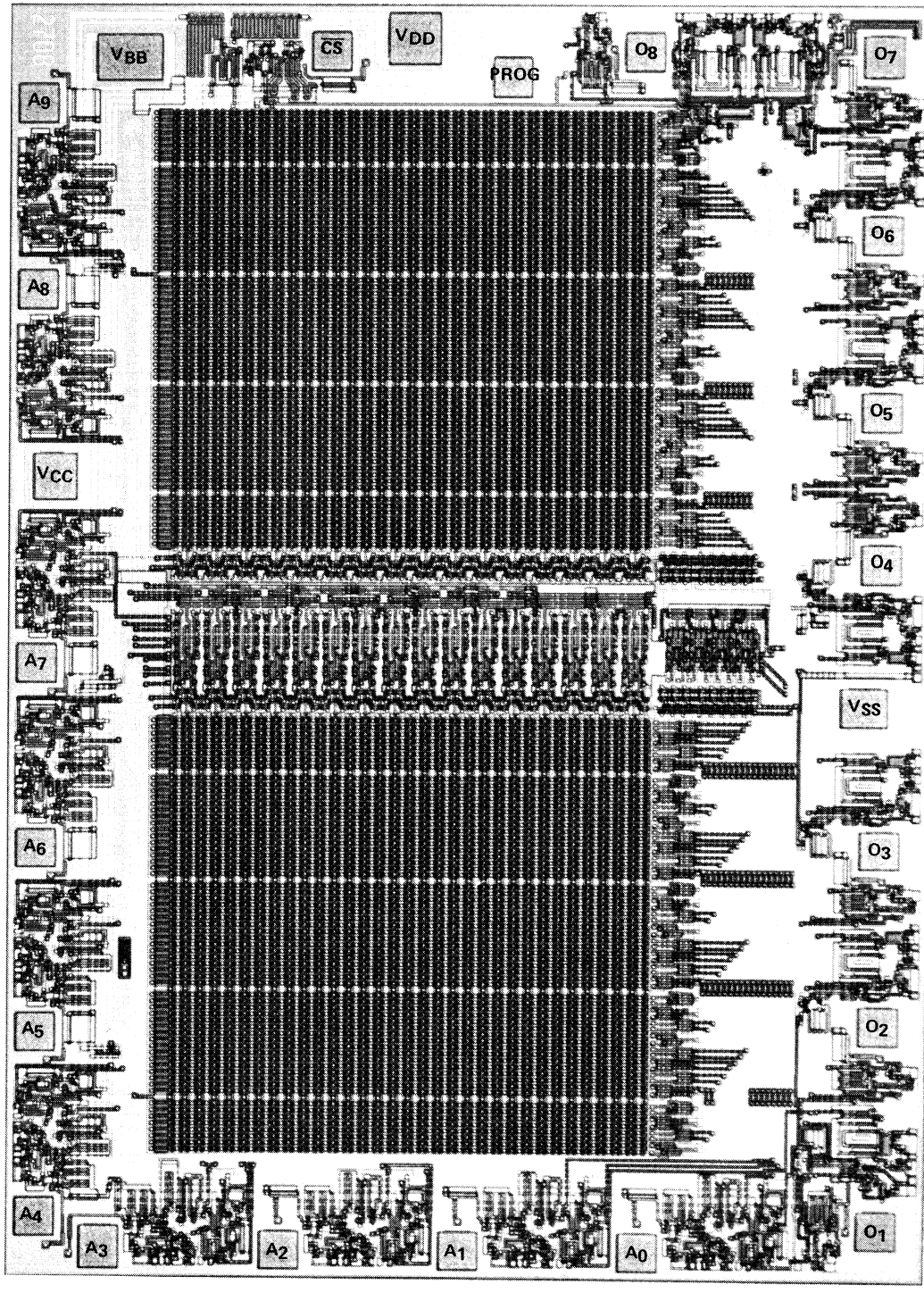
Intel has available reliability and application reports on their MOS EPROMs and bipolar PROMs. These reports may be obtained from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ITEM	DESCRIPTION	LITERATURE NUMBER
1702A Silicon Gate MOS 2K PROM	Reliability Report	RR-6
Polysilicon Fuse Bipolar PROMs	Reliability Report	RR-8
Intel 2708 8K UV Erasable PROM	Reliability Report	RR-12
Application of the Intel 2708 8K Erasable PROM	Application Note	AP-17
The Biggest Erasable PROM Yet — Puts 16,384 Bits On A Chip	Article Reprint from Electronics Magazine	AR-20

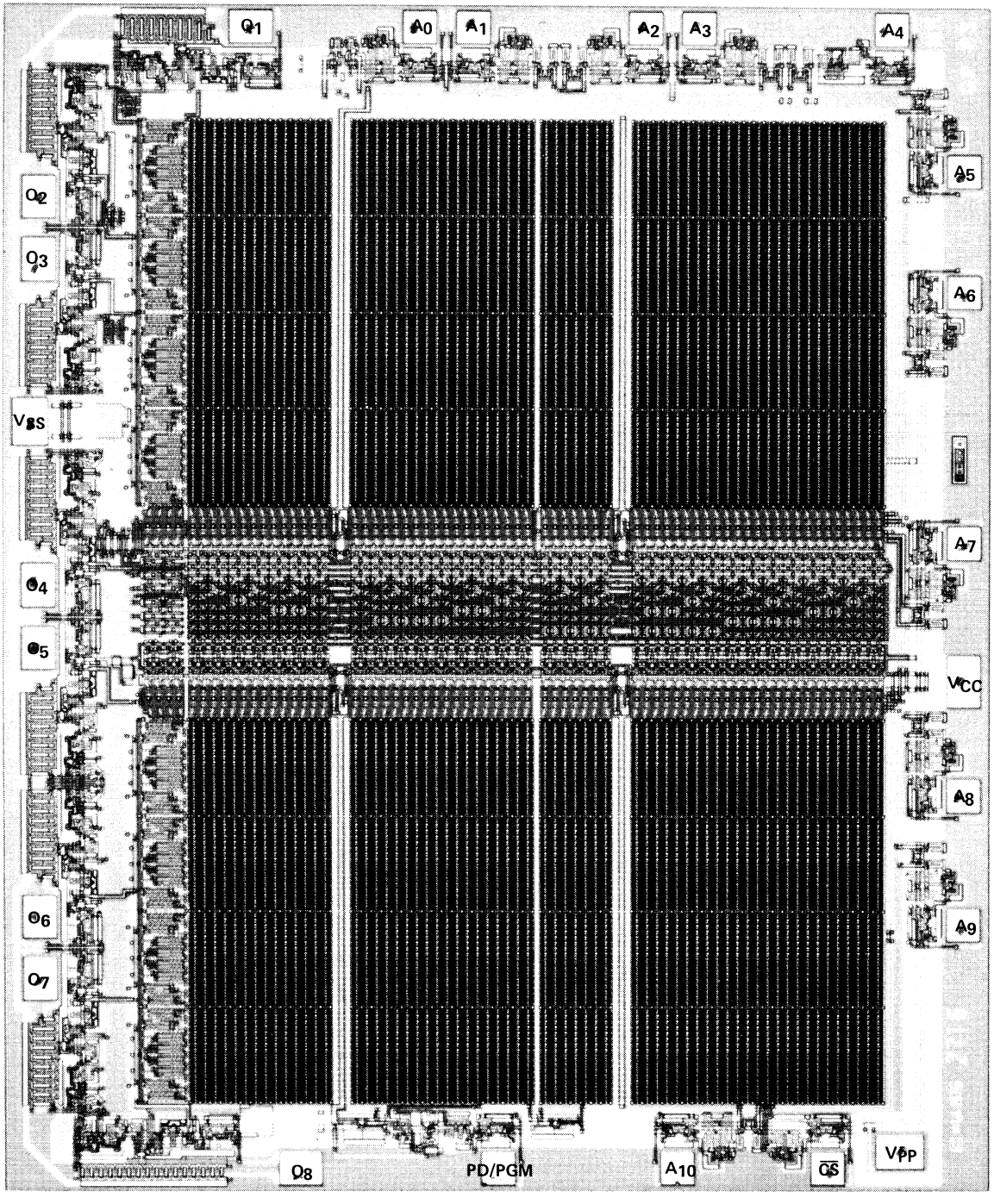
2316E 16K ROM

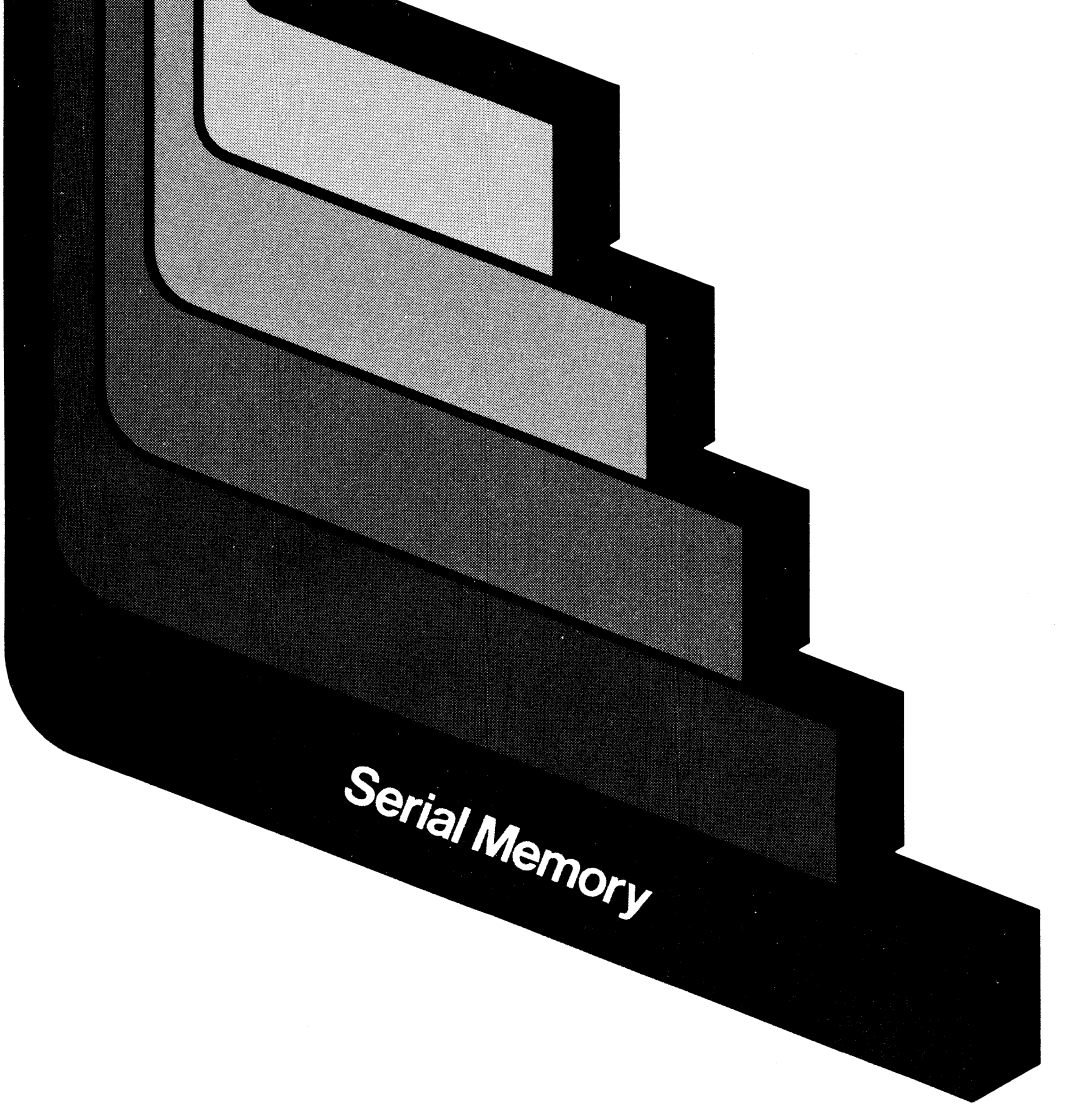


2708 8K UV EPROM



2716 16K EPROM




Serial Memory

SERIAL MEMORIES

	Type	No. of Bits	Description	No. of Pins	Electrical Characteristics Over Temperature						Page No.
					Data Rep. Rate		Power Dissipation Max.[1]	Input Output Levels	Clock Levels	Supplies[V]	
					Min.	Max.					
SILICON GATE MOS	**1402A**	1024	Quad 256-Bit Dynamic	16	10kHz	5MHz	500mW	TTL	MOS/TTL	5, -5 or 5, -9	4-3
	1403A	1024	Dual 512-Bit Dynamic	8	10kHz	5MHz	500mW	TTL	MOS/TTL	5, -5 or 5, -9	
	1404A	1024	1024-Bit Dynamic	8	10kHz	5MHz	500mW	TTL	MOS/TTL	5, -5 or 5, -9	
	1405A	512	Dynamic Recirculating	10	10kHz	2MHz	400mW	TTL	MOS/TTL	5, -5 or 5, -9	4-7
	2401	2048	Dual 1024-Bit Dynamic Recirculating	16	25kHz	1MHz	350mW	TTL	TTL	+5	4-11
	2405	1024	1024-Bit Dynamic Recirculating	16	25kHz	1MHz	350mW	TTL	TTL	+5	
	2416	16,384	CCD Serial Memory	18	125kHz	2MHz	300mW	TTL	MOS	+12, -5	4-15

Note: Power Dissipation calculated with maximum power supply current and nominal supply voltages.

1402A, 1403A, 1404A

1024 BIT DYNAMIC SHIFT REGISTER

- **Guaranteed 5 MHz Operation over Temperature Range**
- **Low Power Dissipation --.1 mW/bit at 1 MHz**
- **DTL, TTL Compatible**
- **Low Clock Capacitance -- 140 pF**
- **Low Clock Leakage -- ≤ 1 μA**
- **Inputs Protected Against Static Charge**
- **Standard Packaging -- 8 Lead Metal Can, 16 Pin Ceramic Dual In-Line**
- **Three Standard Configurations -- Quad 256 Bit -- 1402A, Dual 512 Bit -- 1403A, Single 1024 Bit -- 1404A**

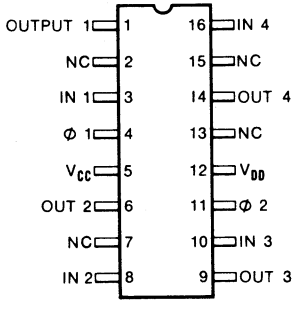
The 1402A/1403A/1404A are direct pin for pin replacements for the 1402/1403/1404. Due to "on chip" multiplexing the data rate is twice the clock rate. Data is shifted one bit on each clock pulse (both ϕ_1 and ϕ_2).

The 1402A/1403A/1404A family is ideally suited for usage in low cost serial memories or delay line applications. A high speed data rate of 5 MHz is easily obtained at the power supplies of +5V and −5V. The 1402A/3A/4A are capable of operating at the power supply voltages of +5V, −9V as well as +5V, −5V.

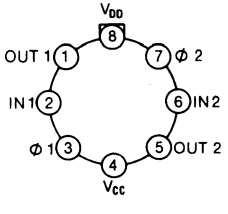
The input to the shift register can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The design of the output stage provides driving capability for both MOS and bipolar IC's.

Use of low threshold **silicon gate technology** allows high speed (5 MHz guaranteed) while reducing power dissipation by a factor of **two** and clock input capacitance by a factor of **three** compared to equivalent products manufactured by conventional technologies.

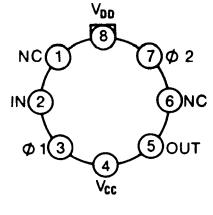
PIN CONFIGURATION



C1402A/P1402A



M1403A



M1404A

Absolute Maximum Ratings[1]

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +160°C
Power Dissipation[2]	1 Watt

Data and Clock Input Voltages and Supply Voltages with respect to V_{CC} +0.5V to −20V

D.C. Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified

V_{DD} = −5V ±5% or −9V ±5%

SYMBOL	TEST	MIN.	TYP[3]	MAX.	UNIT	CONDITIONS
I_{LI}	Input Load Current		< 10	500	nA	T_A =25°C
I_{LO}	Output Leakage Current		<10	1000	nA	V_{OUT}=0.0V, T_A =25°C
I_{LC}	Clock Leakage Current		10	1000	nA	Max. V_{ILC}, T_A =25°C
V_{IL}	Input "Low" Voltage	V_{CC}−10		V_{CC}−4.2	V	
V_{IH}	Input "High" Voltage	V_{CC}−1.5		V_{CC}+.3	V	

V_{DD} = −5V ±5%

I_{DD1}	Power Supply Current		40	50	mA	T_A=25°C Output at Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, V_{ILC}=V_{CC} −17V
I_{DD2}	Power Supply Current			56	mA	T_C=0°C
V_{ILC}	Clock Input Low Voltage	V_{CC} −17		V_{CC}−15	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−1		V_{CC}+.3	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1}=3K to V_{DD}, I_{OL}= 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1}=3K to V_{DD}, I_{OH}= −100 µA
V_{OH2}	Output High Voltage Driving MOS	V_{CC}−1.4	V_{CC}−1		V	R_{L2}=4.7K to V_{DD} (See p. 6 for connection)

V_{DD} = −9V ±5%

I_{DD3}	Power Supply Current		30	40	mA	T_A =25°C Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, V_{ILC}=V_{CC} −14.7V
I_{DD4}	Power Supply Current			45	mA	T_C =0°C
V_{ILC}	Clock Input Low Voltage	V_{CC} −14.7		V_{CC} −12.6	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−1		V_{CC}+.3	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1} =4.7K to V_{DD}, I_{OL} = 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1}=4.7K to V_{DD}, I_{OH}=−100µA
V_{OH2}	Output High Voltage Driving MOS	V_{CC}−1.4	V_{CC}−1		V	R_{L2} =6.2K to V_{DD}, R_{L3} =3.9K to V_{CC} (See p. 6 for connection)

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The 1 watt dissipation is not to be construed as an operating rating (see note 1). For operating at elevated temperatures the device must be derated based as shown on page 3. When operating at V_{DD} = −5V±5% the maximum duty cycle is 33% and at V_{DD}=−9V+5% the maximum duty cycle is 26%. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = $[t_{\phi PW} + \frac{1}{2}(t_R + t_F)]$x clock rate.

Note 3: Typical values are at T_A = 25°C and at nominal voltages.

A. C. Characteristics T_A = 0°C to 70°C; V_{CC} = +5V ±5%

SYMBOL	TEST	V_{DD} = −5V ±5% (Test Load 1)		V_{DD} = −9V ±5% (Test Load 2)		UNIT
		MIN.	MAX.	MIN.	MAX.	
Frequency	Clock Rep Rate		2.5		1.5	MHz
Frequency	Data Rep Rate	Note 1	5.0	Note 1	3.0	MHz
$t_{\phi PW}$	Clock Pulse Width	.130	10	.170	10	µsec
$t_{\phi D}$	Clock Pulse Delay	10	Note 1	10	Note 1	nsec
t_R, t_F	Clock Pulse Transition		1000		1000	nsec
t_{DW}	Data Write Time (Set Up)	30		60		nsec
t_{DH}	Data To Clock Hold Time	20		20		nsec
t_{A+}, t_{A-}	Clock To Data Out Delay		90		110	nsec

CAPACITANCE[2] V_{CC} = +5V ±5%, V_{DD} = −5V ±5% or −9V ±5%, T_A = 25°C

SYMBOL	TEST	TYP.	MAX.	CONDITIONS
C_{IN}	Input Capacitance	5 pF	10 pF	V_{IN} = V_{CC}
C_{OUT}	Output Capacitance	5 pF	10 pF	V_{OUT} = V_{CC}
C_{ϕ}	Clock Capacitance	110 pF	140 pF	V_{ϕ} = V_{CC}
$C_{\phi 1\,\phi 2}$	Clock to Clock Capacitance	11 pF	16 pF	V_{ϕ} = V_{CC}

f = 1 MHz

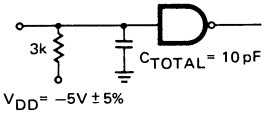
Note 1: See page 5 for guaranteed curve. Note 2: This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test

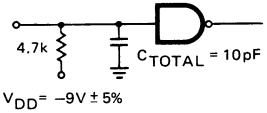
Input rise and fall times: 10 nsec
Output load is 1 TTL gate

TEST LOAD 1



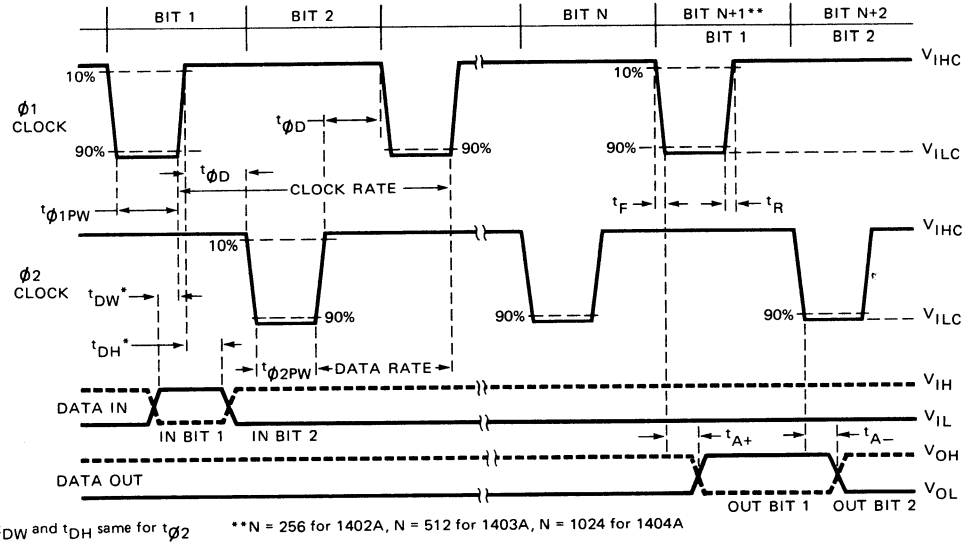
V_{DD} = −5V ± 5%

TEST LOAD 2



V_{DD} = −9V ± 5%

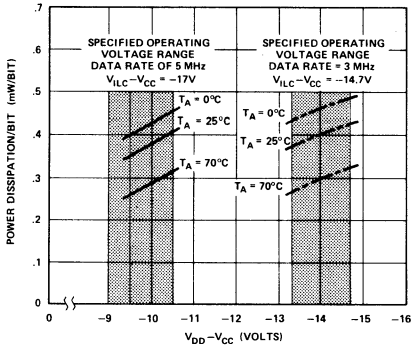
Timing Diagram



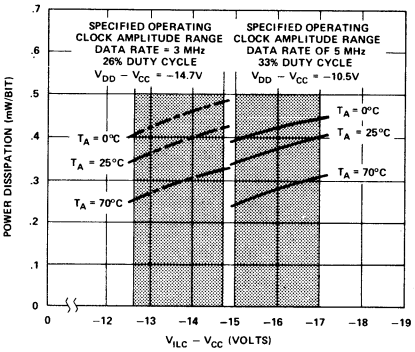
*t_{DW} and t_{DH} same for $t_{\phi 2}$ **N = 256 for 1402A, N = 512 for 1403A, N = 1024 for 1404A

Typical Characteristics

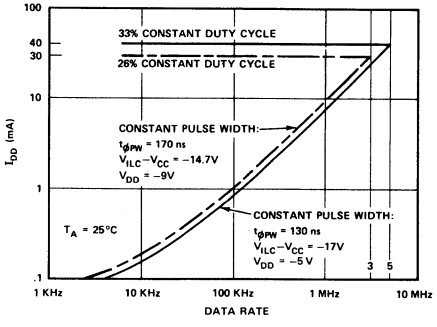
POWER DISSIPATION / BIT VS SUPPLY VOLTAGE



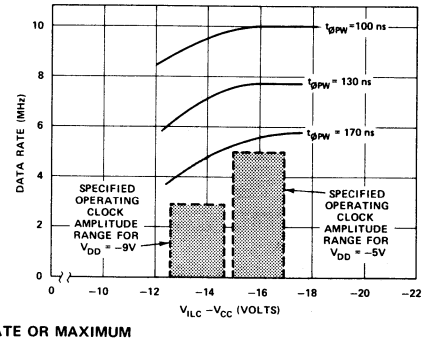
POWER DISSIPATION / BIT VS CLOCK AMPLITUDE



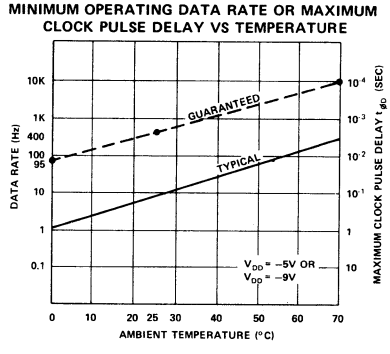
I_{DD} CURRENT VS DATA RATE



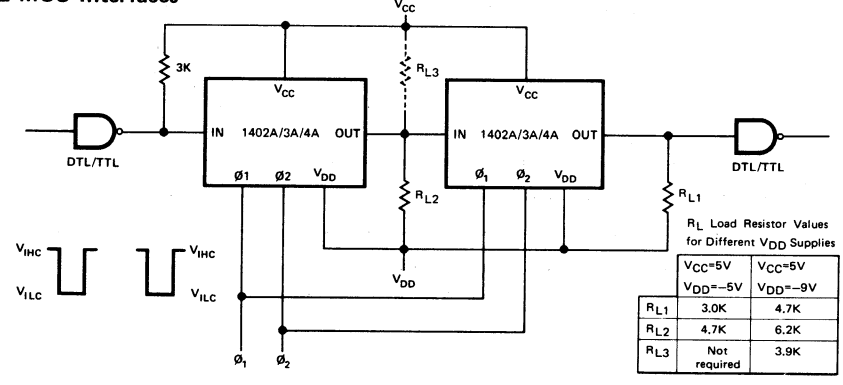
MAXIMUM DATA RATE VS CLOCK AMPLITUDE



MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS TEMPERATURE



DTL/TTL MOS Interfaces



R_L Load Resistor Values for Different V_{DD} Supplies

	V_{CC}=5V V_{DD}=−5V	V_{CC}=5V V_{DD}=−9V
R_{L1}	3.0K	4.7K
R_{L2}	4.7K	6.2K
R_{L3}	Not required	3.9K

512 BIT DYNAMIC RECIRCULATING SHIFT REGISTER

- **High Frequency Operation -- 2 MHz Guaranteed over Temperature.**
- **DTL, TTL Compatible**
- **Write/Recirculate and Read Controls Incorporated on the Chip**
- **Low Power Dissipation--.3 mW/bit at 1 MHz**
- **Low Clock Capacitance--85 pF**
- **Low Clock Leakage -- ≤1 uA at –17 V**
- **Simple Two Dimensional Memory Matrix Organization -- 2 Chip Select Controls**
- **Inputs Protected Against Static Charge**
- **Standard Packaging--10 Lead Low Profile TO-99**

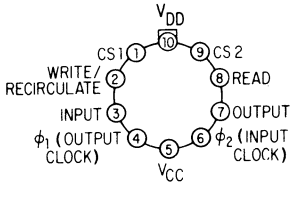
The 1405A is a 512 bit dynamic recirculating shift register and is a direct pin replacement for the 1405. The 1405A is capable of operating at power supply voltages of +5V, –9V as well as +5V, –5V. A high speed recirculating data rate of 2 MHz over the temperature is easily obtained at the +5, –5 power supplies.

Write/recirculate and read controls eliminate the need for external logic elements when recirculating data. In addition, any number of devices can be combined to form a multi-dimensional memory array. For this purpose **two** chip select controls have been provided.

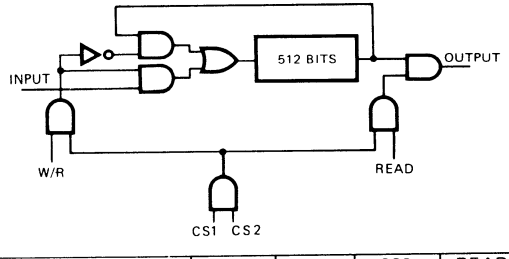
These registers can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the output stage provides driving capability for both MOS and bipolar IC's as well as OR-tieing of shift registers. The 1405A is ideally suited for usage in low cost memories or delay line applications.

Use of low threshold **silicon gate technology** allows high speed (2 MHz guaranteed) while reducing power dissipation by a factor of **two** and clock input capacitance by a factor of **three** over equivalent products manufactured by conventional technologies.

PIN CONFIGURATION



LOGIC DIAGRAM



MODE \ PIN	W/R (2)	CS1 (1)	CS2 (9)	READ (8)
WRITE	1	1	1	1 or 0
RECIRCULATE(1)	1 or 0	1 or 0	1 or 0	1 or 0
READ	1 or 0	1	1	1

Note 1: Either W/R, CS1, or CS2 must be a "0" during Recirculation.
A logic 1 is defined as a high input and a logic 0 as a low input.

Maximum Guaranteed Ratings *

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +160°C
Power Dissipation(1)	600 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+.3V to −20V

* COMMENT:

Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified

V_{DD} = −5V ± 5%

SYMBOL	TEST	MIN.	TYP.(2)	MAX.	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	1000	nA	$V_{IN} = V_{IH}$ to V_{IL}
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	V_{OUT} = 0.0V
I_{LC}	CLOCK LEAKAGE CURRENT		10	1000	nA	$V_{ILC}=V_{CC}-17V$
I_{DD1}	POWER SUPPLY CURRENT		25	40	mA	T_A=25°C, Output at Logic "0", 2 MHz Data Rate, 40% Duty Cycle, Continuous Operation,
I_{DD2}	POWER SUPPLY CURRENT			45	mA	T_C=0°C, $V_{ILC}=V_{CC}-17V$
V_{ILC1}	CLOCK INPUT LOW VOLTAGE	$V_{CC}-17$		$V_{CC}-14.5$	V	
V_{IHC}	CLOCK INPUT HIGH VOLTAGE	$V_{CC}-1$		$V_{CC}+.3$	V	
V_{IL}	INPUT "LOW" VOLTAGE	$V_{CC}-10$		$V_{CC}-4.2$	V	
V_{IH1}	INPUT "HIGH" VOLTAGE	$V_{CC}-1.5$		$V_{CC}+.3$	V	
V_{OL}	OUTPUT LOW VOLTAGE		−.3	0.5	V	R_{L1}=3K to V_{DD}, I_{OL}= 1.6 mA
V_{OH}	OUTPUT HIGH VOLTAGE DRIVING TTL	2.4	3.5		V	R_{L1}=3K to V_{DD}, I_{OH}= −100 μA
V_{OH1}	OUTPUT HIGH VOLTAGE DRIVING MOS	$V_{CC}-1.4$	$V_{CC}-1$		V	R_{L2}=5.6K to V_{DD} (see p. 6 for connection)

V_{DD} = −9V ± 5%

I_{LI}	INPUT LOAD CURRENT		10	1000	nA	$V_{IN} = V_{IH}$ to V_{IL}
I_{LO}	OUTPUT LEAKAGE CURRENT		10	1000	nA	V_{OUT} = 0.0V
I_{LC}	CLOCK LEAKAGE CURRENT		10	1000	nA	$V_{ILC}=V_{CC}-14.7V$
I_{DD3}	POWER SUPPLY CURRENT		20	31	mA	T_A=25°C, Output at Logic "0", 1.5 MHz Data Rate, 36% Duty Cycle, Continuous Operation,
I_{DD4}	POWER SUPPLY CURRENT			36	mA	T_C=0°C, $V_{ILC}=V_{CC}-14.7V$
V_{ILC2}	CLOCK INPUT LOW VOLTAGE	$V_{CC}-14.7$		$V_{CC}-12.6$	V	
V_{IHC}	CLOCK INPUT HIGH VOLTAGE	$V_{CC}-1$		$V_{CC}+.3$	V	
V_{IL}	INPUT "LOW" VOLTAGE	$V_{CC}-10$		$V_{CC}-4.2$	V	
V_{IH2}	INPUT "HIGH" VOLTAGE	$V_{CC}-1.5$		$V_{CC}+.3$	V	
V_{OL}	OUTPUT LOW VOLTAGE		−.3	0.5	V	R_{L1}=5.6K to V_{DD} I_{OL}= 1.6 mA
V_{OH}	OUTPUT HIGH VOLTAGE DRIVING TTL	2.4	3.5		V	R_{L1}=5.6K to V_{DD}, I_{OH}=−100 μA
V_{OH1}	OUTPUT HIGH VOLTAGE DRIVING MOS	$V_{CC}-1.4$	$V_{CC}-1$		V	R_{L2}=6.2K to V_{DD} (See p. 6 for R_{L3}=3.9K to V_{CC} connection)

Note 1: For operating at elevated temperatures the device must be derated based as shown on page 3. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = $[t_{\phi PW} + \frac{1}{2}(t_R + t_F)]$ x clock rate.

Note 2: Typical values are at T_A = 25°C and at nominal voltages.

A.C. Characteristics T_A = 0°C to +70°C; V_{CC} = +5V ±5%; C_L = 20pF; 1 TTL Load

SYMBOL	TEST	V_{DD} = −5V ± 5% V_{ILC}=V_{CC}−14.5 to V_{CC}−17 R_L = 3 K		V_{DD} = −9V ± 5% V_{ILC}=V_{CC}−12.6 to V_{CC}−14.7 R_L = 5.6 K		UNIT
		MIN.	MAX.	MIN.	MAX.	
Frequency	CLOCK DATA REP RATE	200 Hz @ 25°C(1)	2	200Hz @ 25°C(1)	1.5	MHz
$t_{\phi PW}$	CLOCK PULSE WIDTH	0.200	10	.240	10	μsec
$t_{\phi D}$	CLOCK PULSE DELAY	30	Note 1	30	Note 1	nsec
Duty Cycle(2)	CLOCK DUTY CYCLE		40		36	%
t_R;t_F	CLOCK PULSE TRANSITION		1		1	μsec
t_{DW}	DATA WRITE (SETUP) TIME	100		100		nsec
t_{DH}	DATA TO CLOCK HOLD TIME	20		20		nsec
t_{A+}; t_{A-}	CLOCK TO DATA OUT DELAY		250		250	nsec
t_{R-}; t_{CS-}; t_{WR-}	CLOCK TO "READ" OR "CHIP SELECT" OR "WRITE/ RECIRCULATE" TIMING	0		0		nsec
t_{R+}; t_{CS+}; t_{WR+}	CLOCK TO "READ" OR "CHIP SELECT" OR "WRITE/ RECIRCULATE" TIMING	0		0		nsec

CAPACITANCE(3) V_{CC} = 5V ± 5%, V_{DD} = −5V ± 5% or −9V ± 5%, T_A = 25°C

SYMBOL	TEST	TYP.	MAX.	CONDITIONS
C_{IN}	INPUT CAPACITANCE	3	5 pF	V_{IN} = V_{CC}
C_{OUT}	OUTPUT CAPACITANCE	2	5 pF	V_{OUT} = V_{CC}
C_ϕ	CLOCK CAPACITANCE	75	85 pF	V_ϕ = V_{CC}
$C_{\phi_1\text{-}\phi_2}$	CLOCK TO CLOCK CAPACITANCE	6	10 pF	V_ϕ = V_{CC}

f = 1 MHz

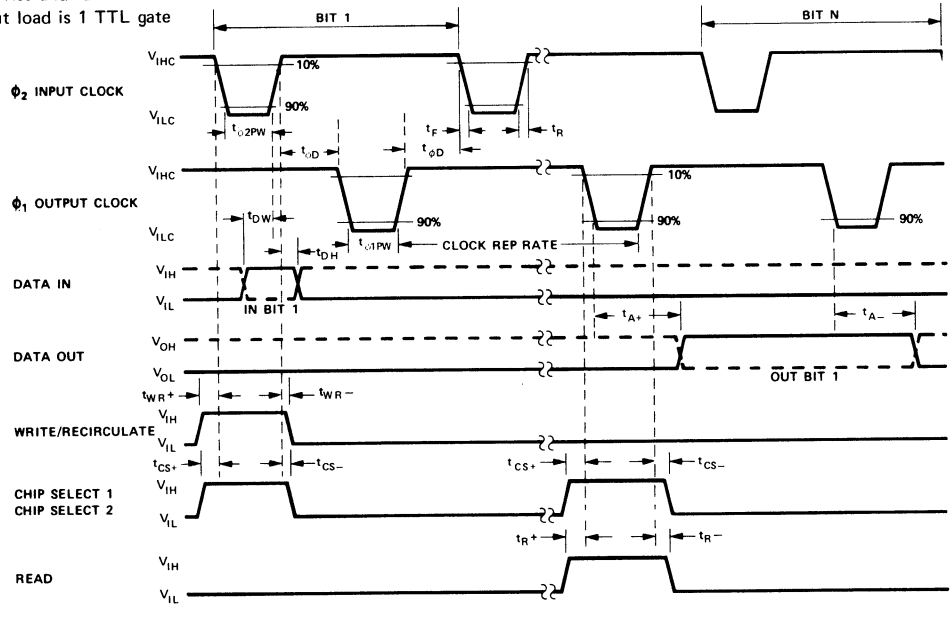
Note 1: See curve of Min Data Rate, and Max Clock Delay vs. Temp. on page 5. Note 2: Duty Cycle = $[t_{\phi PW} + ½(t_R + t_F)]$ x clock rate.
Note 3: This parameter is periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test

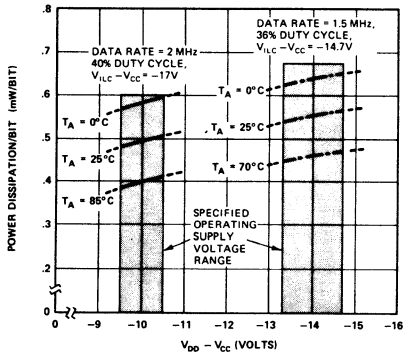
Input rise and fall times: 10nsec
Output load is 1 TTL gate

Timing Diagram

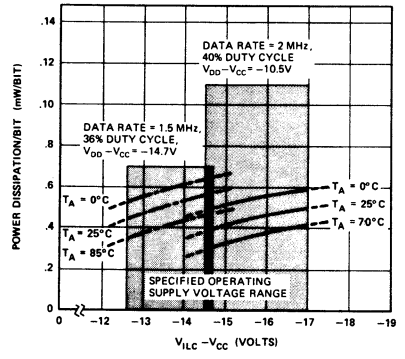


Typical Characteristics

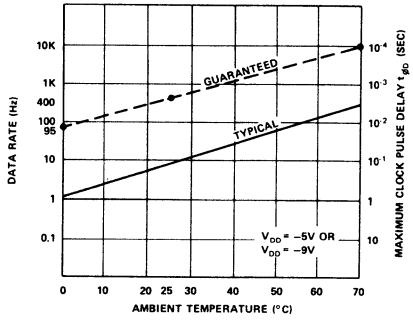
POWER DISSIPATION/BIT VS. SUPPLY VOLTAGE



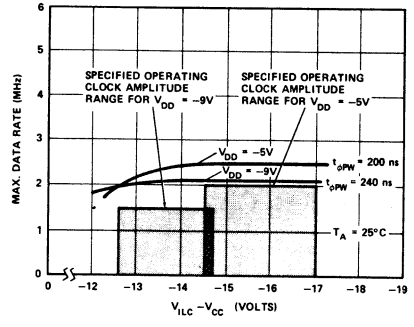
POWER DISSIPATION/BIT VS. CLOCK AMPLITUDE



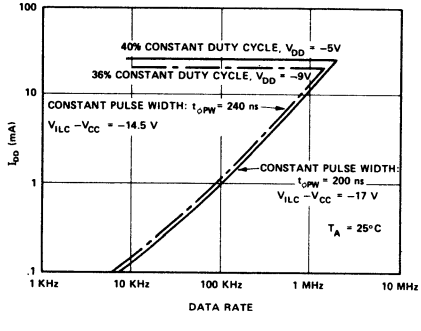
MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS TEMPERATURE



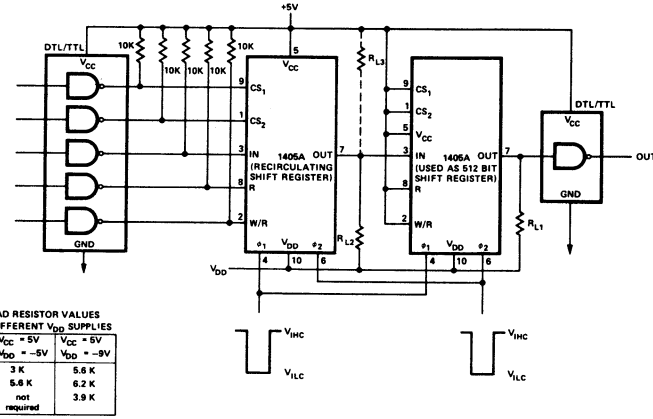
MAXIMUM DATA RATE VS. CLOCK AMPLITUDE



I_{DD} CURRENT VS. DATA RATE



DTL/TTL/MOS Interfaces



R_L LOAD RESISTOR VALUES FOR DIFFERENT V_{DD} SUPPLIES

	V_{CC} = 5V, V_{DD} = −5V	V_{CC} = 5V, V_{DD} = −9V
R_{L1}	3 K	5.6 K
R_{L2}	5.6 K	6.2 K
R_{L3}	not required	3.9 K

2048/1024 BIT DYNAMIC RECIRCULATING SHIFT REGISTERS

- **Single Supply Voltage -- +5 Volts**
- **Fully TTL Compatible -- Inputs, Outputs and Clock**
- **Single Phase Clock**
- **Guaranteed 1 MHz Operation with 100 pF Load, over Temperature Range**
- **Low Power Dissipation -- 120 μw/bit typically at 1 MHz**
- **Low Clock Capacitance -- 7 pF**
- **Write/Recirculate and Chip Select Logic Incorporated on Chip**
- **Standard Configurations -- Dual 1024 Bit -- 2401 Single 1024 Bit -- 2405**

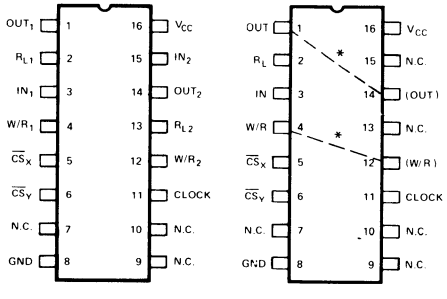
The 2401/2405 are 2048/1024 bit dynamic recirculating shift registers. They are directly TTL compatible in all respects: inputs, outputs, clock and a single +5 volt power supply.

Write/recirculate controls are provided to eliminate the need for external logic elements when recirculating data.

Two chip select inputs have been provided to allow easy selection of an individual package when outputs of several devices have been "OR-tied". A separate internal "pullup" resistor (R_L) is provided which can be externally connected to the output pin to achieve full signal swing.

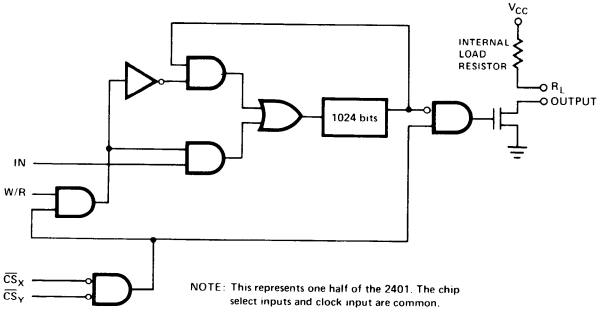
This Intel shift register family is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy to use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible, including clocks.

PIN CONFIGURATIONS



* DASH LINES INDICATE NECESSARY EXTERNAL PRINTED CIRCUIT BOARD CONNECTIONS FOR PROPER OPERATION OF THE 2405. (SEE APPLICATION SECTION)

LOGIC DIAGRAM



NOTE: This represents one half of the 2401. The chip select inputs and clock input are common.

PIN NAMES

IN	DATA INPUT	OUT	DATA OUTPUT
W/R	WRITE/RECIRCULATE CONTROL	R_L	INTERNAL LOAD RESISTOR
$\overline{CS}_X$, $\overline{CS}_Y$	CHIP SELECT INPUT	N.C.	NO CONNECTION

TRUTH TABLE

FUNCTION	PIN SYMBOL W/R	$\overline{CS}_X$	$\overline{CS}_Y$
WRITE MODE	H	L	L
RECIRCULATE	L	X	X
	X	H	X
	X	X	H
READ MODE	X	L	L

H = Logic High Level L = Logic Low Level
X = Don't Care Condition

Absolute Maximum Ratings*

Ambient Temperature Under Bias: 0° C to 70° C
Storage Temperature: −65° C to +150° C
Power Dissipation: 1W
Voltage on Any Pin with Respect to Ground: −0.5V to +7V

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

T_A = 0°to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

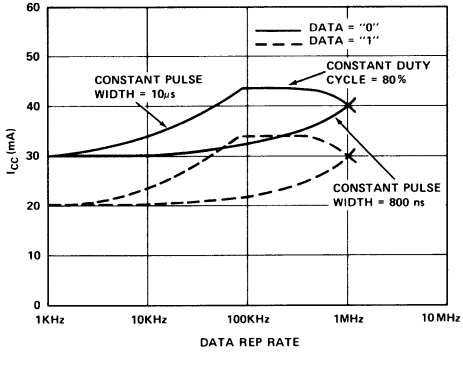
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.[1]	LIMITS MAX.	UNITS	TEST CONDITIONS
I_{LI}	INPUT LEAKAGE			10	µA	V_{IN} = 5.25V
I_{LO}	OUTPUT LEAKAGE			100	µA	V_{OUT} = 5.25V
I_{CC}	POWER SUPPLY CURRENT		45 50	70 80	mA mA	T_A = 25°C T_A = 0°C V_{CC} = 5.25V; 80% DUTY CYCLE
V_{IH}	INPUT HIGH LEVEL VOLTAGE (ALL INPUTS)	2.2		5.25	V	
V_{IL}	INPUT LOW LEVEL VOLTAGE (ALL INPUTS)	-0.3		0.65	V	
V_{OH}	OUTPUT HIGH LEVEL VOLTAGE	2.4		V_{CC}	V	I_{OH} = -1mA, R_L = 1.5K ± 5% ohms, external
V_{OL}	OUTPUT LOW LEVEL VOLTAGE	0		0.45	V	I_{OL} = 5.0mA, R_L = 1.5K ± 5% ohms, external[2]

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. The following was used to calculate I_{OL}.

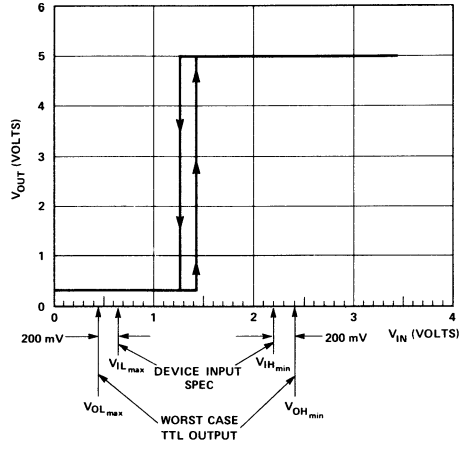
$$I_{OL} = \frac{V_{CC}\ (max.) - V_{OL}\ (max.)}{R_L\ (min.)} + I_{LI}\ (TTL\ device) = \frac{5.25 - 0.45}{1.425} + 1.6 = 4.97mA.$$

Also note that the internal load resistor, R_{LI}, has a value ranging from 500 ohms minimum to 2,200 ohms maximum. The internal load resistor can be used when driving from one 2401/2405 to another 2401/2405 or to other MOS inputs.

POWER SUPPLY CURRENT (I_{CC}) VS. DATA REP RATE



EFFECTIVE INPUT CHARACTERISTIC



A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

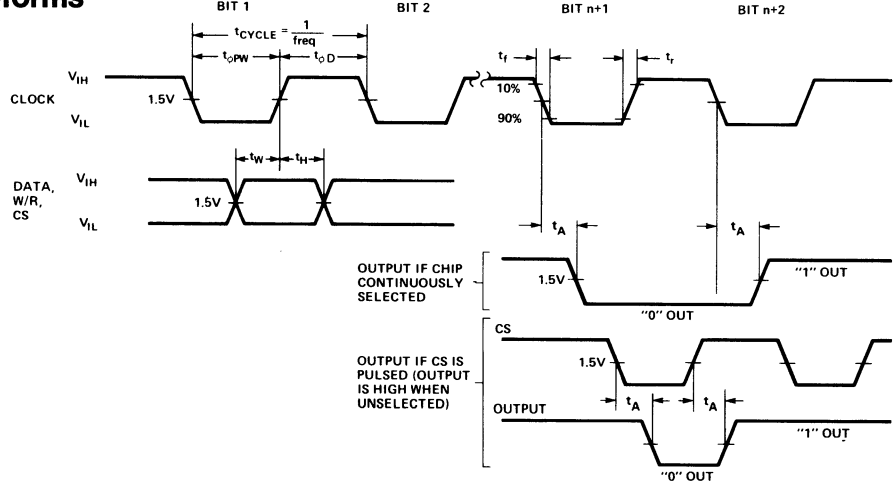
SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
FREQ. MAX.	MAX. DATA REP. RATE			1	MHz	
FREQ. MIN.	MIN. DATA REP. RATE	1 25[1]			KHz KHz	T_A = 25° C T_A = 70° C
$t_{\phi PW}$	CLOCK PULSE WIDTH	0.80		10	μs	
$t_{\phi D}$	CLOCK PULSE DELAY	0.20 0.20		1000 40	μs μs	T_A = 25° C T_A = 70° C
t_r , t_f	CLOCK RISE AND FALL TIME			50	ns	
t_W	WRITE TIME	200			ns	
t_H	HOLD TIME	150			ns	
t_A	ACCESS TIME FROM CLOCK OR CHIP SELECT		250	500	ns	R_L = 1.5K ± 5% ohm, EXTERNAL C_L = 100pF ONE TTL LOAD

NOTE: 1. 100 kHz in plastic (P) package.

Capacitance T_A = 25° C

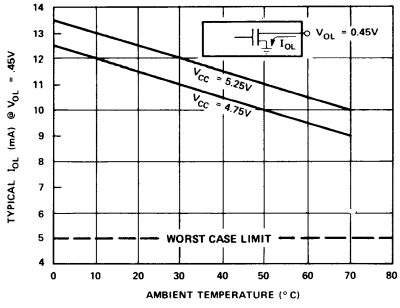
SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
C_{IN}	DATA, W/R & CS INPUT CAPACITANCE		4	7	pF	ALL PINS AT AC GROUND; 250 mV PEAK TO PEAK, 1 MHz
C_{OUT}	OUTPUT CAPACITANCE		10	14	pF	
C_ϕ	CLOCK CAPACITANCE		4	7	pF	

Waveforms

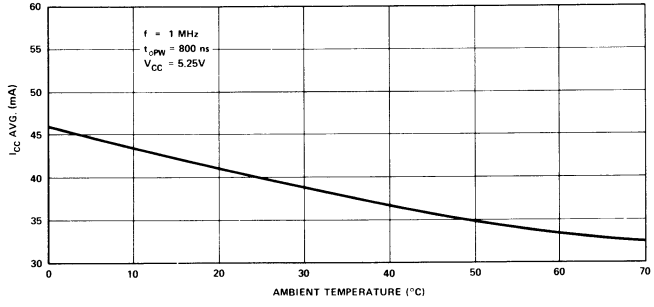


D. C. Characteristics

TEMPERATURE DEPENDENCE OF OUTPUT LOW LEVEL SINK CAPABILITY

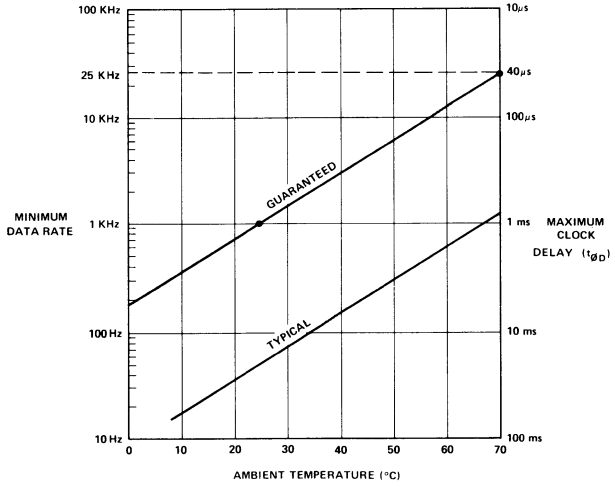


POWER SUPPLY CURRENT (I_{CC}) VS. AMBIENT TEMPERATURE (°C)

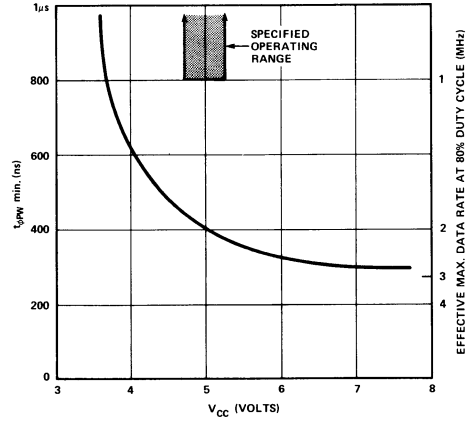


A. C. Characteristics

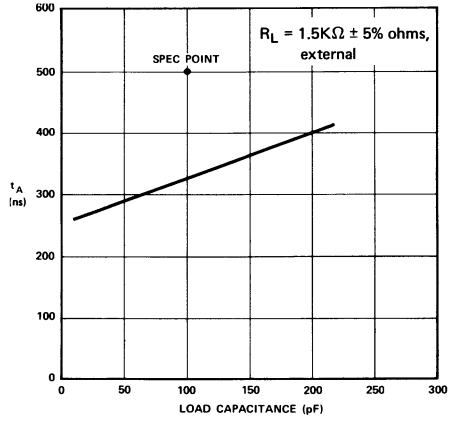
MINIMUM DATA RATE AND MAXIMUM CLOCK DELAY VS. AMBIENT TEMPERATURE FOR CERAMIC (C) PACKAGE



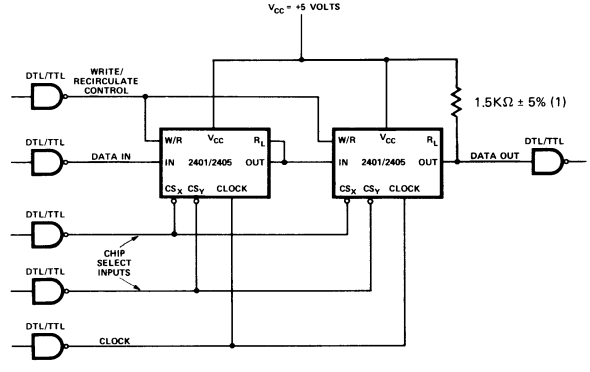
MINIMUM CLOCK PULSE WIDTH AND EFFECTIVE MAXIMUM DATA RATE AT 80% DUTY CYCLE VS. POWER SUPPLY VOLTAGE (V_{CC})



ACCESS TIME VS. LOAD CAPACITANCE



Typical Application Of TTL Compatible Shift Registers



NOTE (1): The 2401/2405 is directly compatible device to device. An external 1.5KΩ ± 5% load resistor is recommended for driving one TTL load with the 2401/2405 output.

2416

16,384 BIT CCD SERIAL MEMORY

▪ Organization: 64 Recirculating Shift Registers of 256 Bits Each

- **Avg. Latency Time Under 100 μs**
- **Max. Serial Data Transfer Rate —2 mega bits/sec.**
- **Address Registers Incorporated on Chip**
- **Standard Power Supplies— +12V, −5V**
- **Open Drain Output**
- **Combined Read/Write Cycles Allowed**
- **Compatible to Intel® 5244 CCD Driver**

SERIAL MEMORY

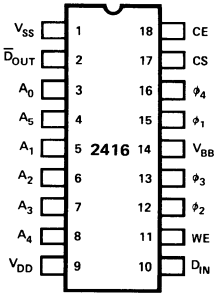
The Intel® 2416 is a 16,384 bit CCD serial memory designed for low-cost memory applications requiring average latency times to under 100 μs. To achieve low latency time the memory was organized in the form of 64 independent recirculating shift registers of 256 bits each. Any one of the 64 shift registers can be accessed by applying an appropriate 6-bit address input.

The shift registers recirculate data automatically as long as the four-phase CCD clocks (ϕ_1 . . . ϕ_4) are continuously applied and no write command is given. A one-bit shift is initiated in all 64 registers following a low-to-high transition of either ϕ_2 or ϕ_4. After the shift operation the contents of the 64 registers at the bit location involved are available for non-destructive reading, and/or for modification. I/O functions are accomplished in a manner similar to that of a 64-bit dynamic RAM. At the next shift cycle, the contents of the 64 accessible bits (whether modified or not) are transferred forward into the respective registers and the contents of the next bit of each register become accessible. No I/O function can be performed during the shift operation itself.

The Intel 2416 generates and uses an internal reference voltage which requires some time to stabilize after the power supplies and four phase clocks have been turned on. No I/O functions should be performed until the four-phase CCD clocks have executed at least 4000 shift cycles with power supplies at operating voltages. After this start-up period, no special action is needed to keep the internal reference voltage stable.

The 2416 is fabricated using Intel's advanced high voltage N-channel Silicon Gate MOS process.

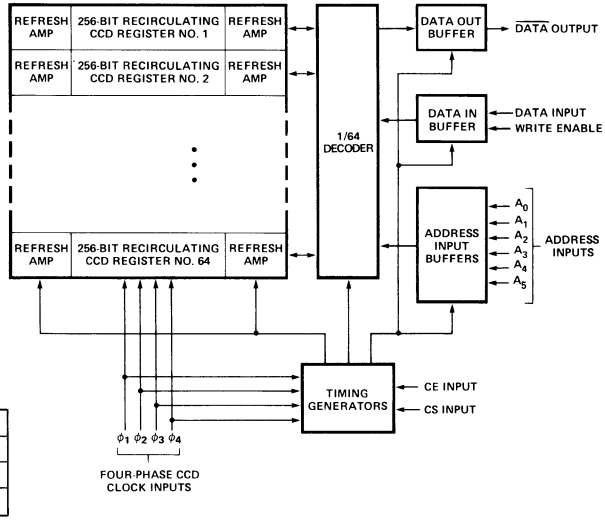
PIN CONFIGURATION



PIN NAMES

A_0-A_5	ADDRESS INPUTS	CE	CHIP ENABLE INPUT
D_{IN}	DATA INPUT	ϕ_1-ϕ_4	CCD CLOCK INPUTS
WE	WRITE ENABLE INPUT	V_{DD}, V_{SS}, V_{BB}	POWER SUPPLIES
CS	CHIP SELECT INPUT	$\overline{D}_{OUT}$	$\overline{DATA}$ OUTPUT

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . . +25V to -0.3V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . . . . . +20V to -0.3V
Power Dissipation 1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{BB}[1] = -5V ±5%, V_{SS} = 0V, unless otherwise specified.

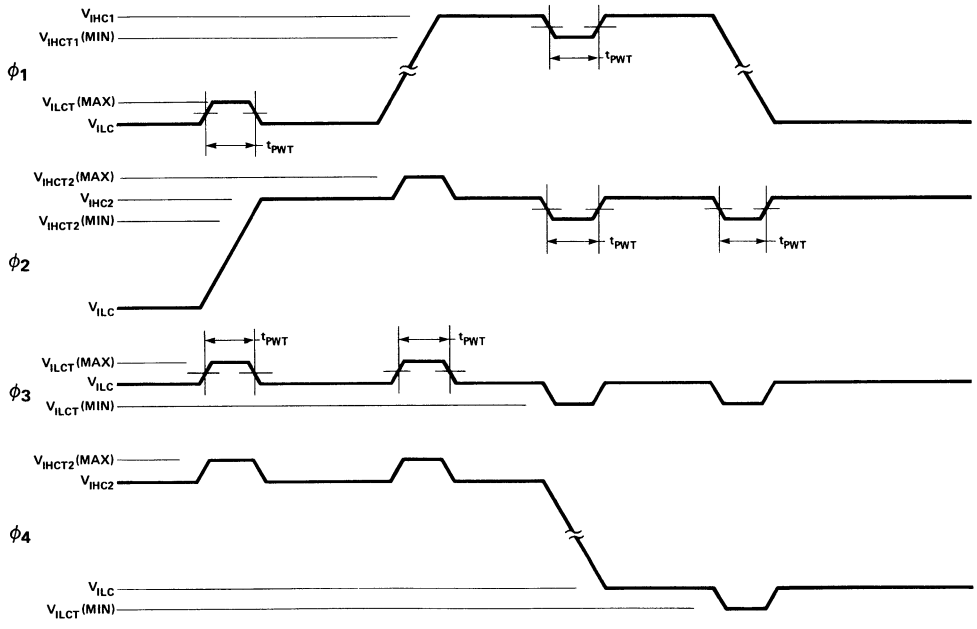
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Leakage Current		1	10	µA	V_{IN} = 0V
I_{LO}	Output Leakage Current		1	10	µA	CE = 0V, V_{OUT} = 0V
I_{OL}	Output Low Current	3			mA	V_{OL} = .45V
I_{OH}	Output High Current			10	µA	V_{OH} = +5V
I_{DDAV1}	Average V_{DD} Supply Current for Shift Cycles Only			Note 2	mA	
I_{DDAV2}[3]	Average V_{DD} Supply Current		15	25	mA	
I_{BB}	Average V_{BB} Supply Current		100	200	µA	
V_{IL}	Input Low Voltage, All Inputs Except $\phi_1 \ldots \phi_4$	-1.0		0.8	V	
V_{IH1}	Input High Voltage, All Inputs Except D_{IN} and $\phi_1 \ldots \phi_4$	V_{DD}-1		V_{DD}+1	V	
V_{IHD}	D_{IN} Input High Voltage	3.5		V_{DD}+1	V	
V_{ILC}[4]	$\phi_1 \ldots \phi_4$ Input Low Voltage dc	-2.0		0.6	V	
V_{ILCT}	$\phi_1 \ldots \phi_4$ Input Low Voltage w/Coupling	-2.0[5]		1.2[6]	V	
V_{IHC1}	ϕ_1 and ϕ_3 Input High Voltage dc	V_{DD}-1		V_{DD}+2	V	
V_{IHCT1}	ϕ_1 and ϕ_3 Input High Voltage w/Coupling	V_{DD}-1.6[6]		V_{DD}+2[5]	V	
V_{IHC2}	ϕ_2 and ϕ_4 Input High Voltage dc	V_{DD}-0.6		V_{DD}+2	V	
V_{IHCT2}	ϕ_2 and ϕ_4 Input High Voltage w/Coupling	V_{DD}-1.2[6]		V_{DD}+2[5]	V	
t_{PWT}	Cross Coupling Voltage Pulse Width			Note 7	ns	Pulse width measured at 0.8V and V_{DD}-1.2V (ϕ_1 and ϕ_3) or V_{DD}-0.8V (ϕ_2 and ϕ_4)

Notes: 1. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB}.

2. For shift only mode $I_{DD} = 2.0mA + \frac{15mA}{t_{\phi/2}\ (\text{in } \mu s)}$

3. I_{DDAV2} is for combined shift and data I/O cycles.
4. The difference in the low level reference voltages between all four clock phases must not exceed 0.5 volts.
5. These voltage levels with coupling are within the specified dc range and are not, therefore, subject to t_{PWT} restrictions.
6. These voltage levels with coupling are outside specified dc ranges and must be restricted to t_{PWT} pulse widths.
7. The maximum clock cross coupled pulse width is the sum of the clock transition time (t_T) plus 20ns.

$\phi_1 \ldots \phi_4$ CROSS-COUPLING



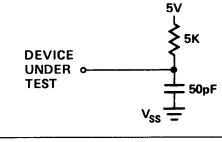
SERIAL MEMORY

A.C. Characteristics T_A = 0°C to 70°C, V_{DD} = 12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, unless otherwise specified.

SHIFT ONLY CYCLES

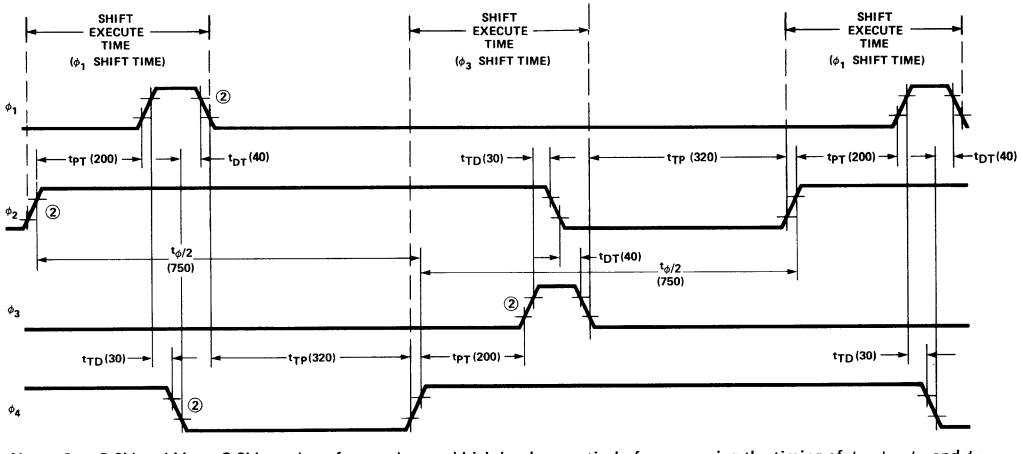
Symbol	Parameter	Min.	Max.	Unit	Conditions
$t_{\phi}/2$	Half Clock Period for $\phi_1 \ldots \phi_4$	750[1]	10,000	ns	t_T = 40nsec
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
t_{TP}	ϕ_1 Off to ϕ_4 On, ϕ_3 Off to ϕ_2 On	320		ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	

$\overline{D}_{OUT}$ TEST LOAD



Note: 1. The 750ns Half Clock Period will be met for 30ns ≤ t_T ≤ 40ns. Values of t_T > 40ns lengthen $t_{\phi}/2$.

WAVEFORMS (Numbers in parentheses are for minimum cycle timing in ns)



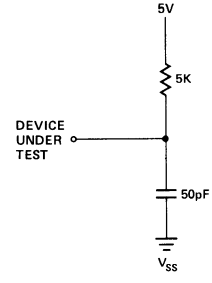
Note: 2. +2.0V and V_{DD}-2.0V are the reference low and high level respectively for measuring the timing of ϕ_1, ϕ_2, ϕ_3 and ϕ_4.

A.C. Characteristics

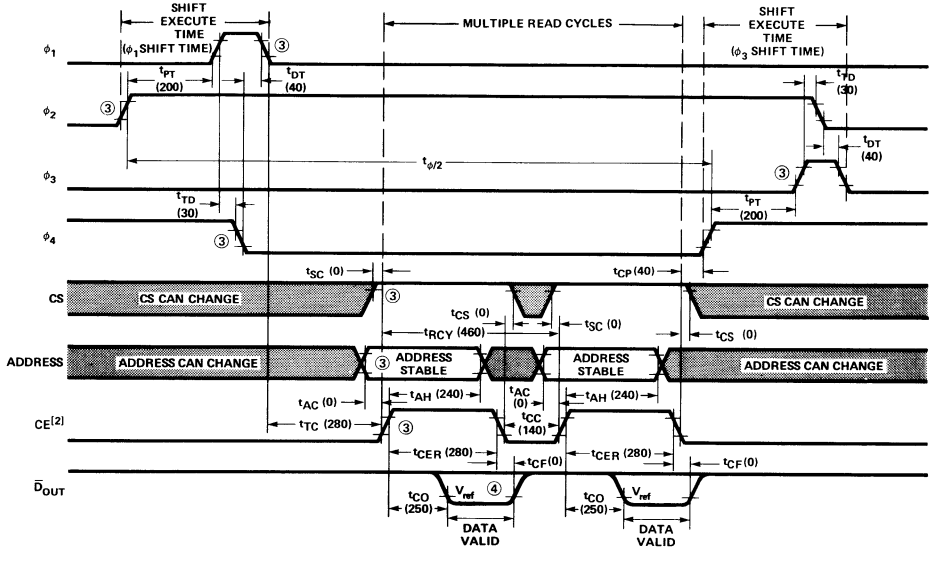
SHIFT–READ–READ–...–READ–SHIFT CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	READ Cycle Time	460		ns	
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	t_T = 40ns
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	t_{T1} = 20ns
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$		10,000	ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	
t_{T1}	Transition Times for Inputs Other Than $\phi_1 \ldots \phi_4$		100	ns	
t_{TC}	ϕ_1 or ϕ_3 Off to CE On	280		ns	
t_{SC}	CS to CE Set-Up Time	0		ns	
t_{AC}	Address to CD Set-Up Time	0		ns	
t_{AH}	Address Hold Time	240		ns	
t_{CS}	CE to CS Hold Time	0		ns	
t_{CC}	CE Off Time	140		ns	
t_{CP}	CE Off to ϕ_2 or ϕ_4 On	40		ns	
t_{CER}	CE On Time	280		ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	
t_{CO}	CE to $\overline{D}_{OUT}$ Valid	250		ns	

$\overline{D}_{OUT}$ TEST LOAD



WAVEFORMS[1] (Numbers in parentheses are for minimum cycle timing in ns)



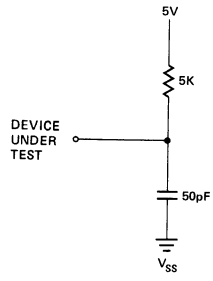
NOTES:
1. WE must be continuously low during the READ cycle.
2. When CE is off, the 2416 output level is determined by the external output termination.
3. +2.0V and V_{DD}-2.0V are the reference low and high level respectively for measuring the timing of $\phi_1 \ldots \phi_4$, CE, CS and addresses.
4. +0.8V is the reference level for measuring the timing of $\overline{D}_{OUT}$.

A.C. Characteristics

SHIFT–WRITE–WRITE–...–WRITE–SHIFT CYCLE

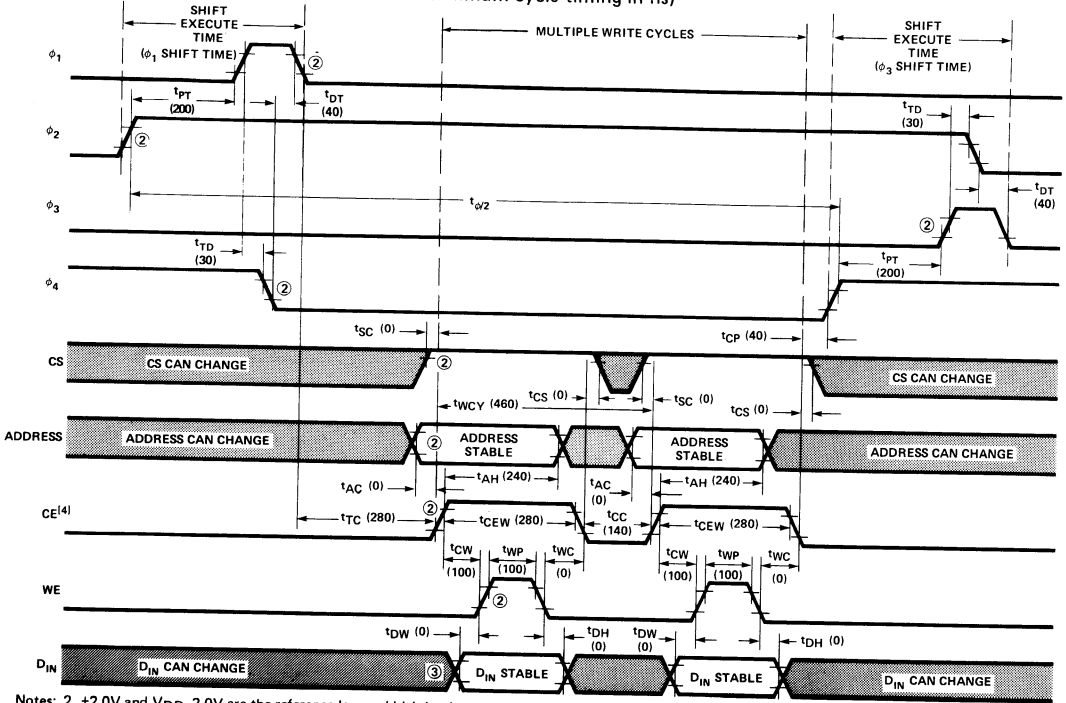
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	WRITE Cycle Time	460		ns	
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	t_T = 40ns
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	t_{T1} = 20ns
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$		10,000	ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	
t_{T1}	Transition Times for Inputs Other Than $\phi_1 \ldots \phi_4$		100	ns	
t_{TC}	ϕ_1 or ϕ_3 Off to CE On	280		ns	
t_{SC}	CS to CE Set-Up Time	0		ns	
t_{AC}	Address to CE Set-Up Time	0		ns	
t_{AH}	Address Hold Time	240		ns	
t_{CS}	CE to CS Hold Time	0		ns	
t_{CC}	CE Off Time	140		ns	
t_{CP}	CE Off to ϕ_2 or ϕ_4 On	40		ns	
t_{CEW}	CE On Time	280[1]		ns	
t_{CW}	CE to WE Set-Up Time	100[1]		ns	
t_{DW}	D_{IN} to WE Set-Up	0		ns	
t_{WP}	WE Pulse Width	100[1]		ns	
t_{WC}	WE Off to CE Off	0[1]		ns	
t_{DH}	D_{IN} Hold Time	0		ns	

$\bar{D}_{OUT}$ TEST LOAD



Note: 1. The minimum t_{CW}, t_{WP} and t_{WC} times with appropriate transitions do not necessarily add up to the minimum t_{CEW}. This allows the user flexibility in setting the WE Pulse Width edges without affecting either t_{CEW} or the WRITE Cycle Time, t_{WCY}.

WAVEFORMS (Numbers in parentheses are for minimum cycle timing in ns)

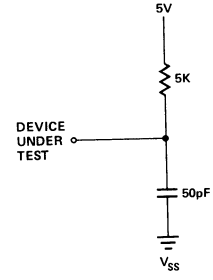


Notes: 2. +2.0V and V_{DD}-2.0V are the reference low and high level respectively for measuring the timing of $\phi_1 \ldots \phi_4$, CE, CS, WE, and addresses.
3. +1.5V and +3.0V are the reference low and high level respectively for measuring the timing of D_{IN}.

A.C. Characteristics SHIFT–RMW–RMW– . . . –RMW–SHIFT CYCLE

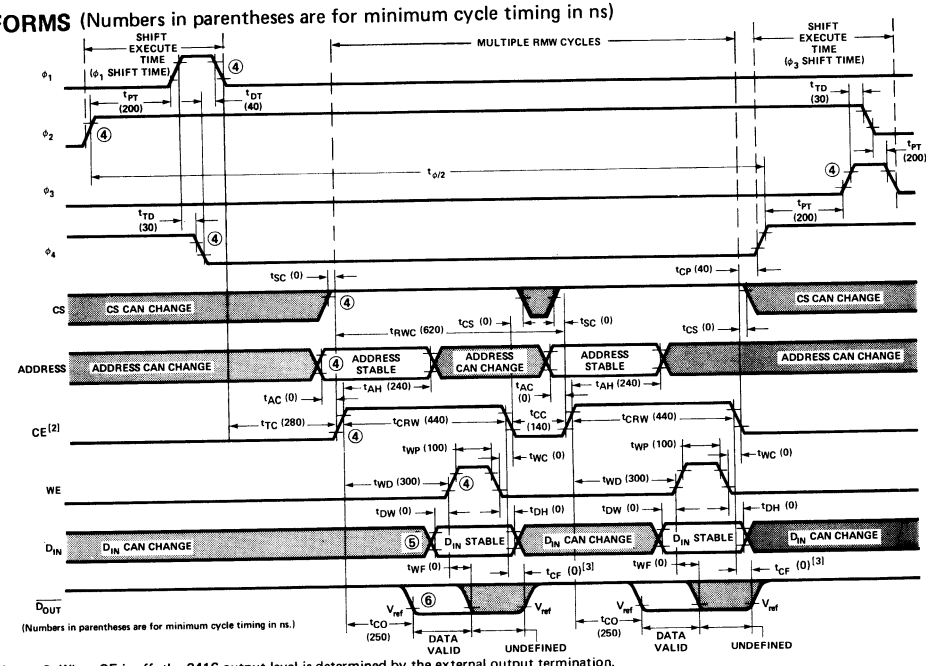
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	READ-MODIFY-WRITE Cycle Time	620		ns	
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time	200		ns	t_T = 40ns
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap	30		ns	t_{T1} = 20ns
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time	40		ns	
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$		10,000	ns	
t_T	Transition Times for $\phi_1 \ldots \phi_4$	30	200	ns	
t_{T1}	Transition Times for Inputs Other Than $\phi_1 \ldots \phi_4$		100	ns	
t_{TC}	ϕ_1 or ϕ_3 Off to CE On	280		ns	
t_{SC}	CS to CE Set-Up Time	0		ns	
t_{AC}	Address to CE Set-Up Time	0		ns	
t_{AH}	Address Hold Time	240		ns	
t_{CS}	CE to CS Hold Time	0		ns	
t_{CC}	CE Off Time	140		ns	
t_{CP}	CE Off to ϕ_2 or ϕ_4 On	40		ns	
t_{CRW}	CE On Time	440[1]		ns	
t_{CO}	CE On to $\overline{D}_{OUT}$ Valid	250		ns	
t_{DW}	D_{IN} to WE Set-Up Time	0		ns	
t_{WP}	WE Pulse Width	100[1]		ns	
t_{WC}	WE Off to CE Off	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WD}	CE On to WE On	300[1]		ns	
t_{WF}	WE to $\overline{D}_{OUT}$ Undefined	0		ns	

$\overline{D}_{OUT}$ TEST LOAD



Note: 1. The minimum t_{WD} and t_{WP} times with appropriate transitions do not necessarily add up to the minimum t_{CRW}. This allows the user flexibility in setting the WE Pulse Width edges without affecting either t_{CRW} or the READ-MODIFY-WRITE Cycle Time, t_{RWC}.

WAVEFORMS (Numbers in parentheses are for minimum cycle timing in ns)



Notes: 2. When CE is off, the 2416 output level is determined by the external output termination.
3. The parameter t_{CF} is the same as in the Shift-Read-Shift Cycle on page 4.
4. +2.0V and V_{DD}–2.0V are the reference low and high level respectively for measuring the timing of $\phi_1 \ldots \phi_4$, CE, CS, WE, and addresses.
5. +1.5V and +3.0V are the reference low and high level respectively for measuring the timing of D_{IN}.
6. +0.8V is the reference level for measuring the timing of $\overline{D}_{OUT}$.

A.C. Characteristics

CAPACITANCE [1] $T_A = 25°C$

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Address, D_{IN}, CS, CE, WE Capacitance	4	6	pF	$V_{IN} = V_{SS}$
C_{OUT}	$\overline{D}_{OUT}$ Capacitance	3	5	pF	$V_{OUT} = V_{SS}$
$C_{\phi1}$ [1], $C_{\phi3}$ [2]	ϕ_1, ϕ_3 Input Capacitance	350	500	pF	$V_\phi = V_{SS}$
$C_{\phi2}$ [1], $C_{\phi4}$ [2]	ϕ_2, ϕ_4 Input Capacitance	480	700	pF	$V_\phi = V_{SS}$
$C_{\phi1-\phi2}$	Clock ϕ_1 To Clock ϕ_2 Capacitance	120	175	pF	$V_\phi = V_{SS}$
$C_{\phi1-\phi4}$	Clock ϕ_1 To Clock ϕ_4 Capacitance	150	200	pF	$V_\phi = V_{SS}$
$C_{\phi3-\phi2}$	Clock ϕ_3 To Clock ϕ_2 Capacitance	150	200	pF	$V_\phi = V_{SS}$
$C_{\phi3-\phi4}$	Clock ϕ_3 To Clock ϕ_4 Capacitance	120	175	pF	$V_\phi = V_{SS}$

Notes: 1. This parameter is periodically sampled and is not 100% tested.
2. The $C_{\phi1}$ .... $C_{\phi4}$ input clock capacitance includes the clock to clock capacitance. The equivalent input capacitance is given below.

SERIAL MEMORY

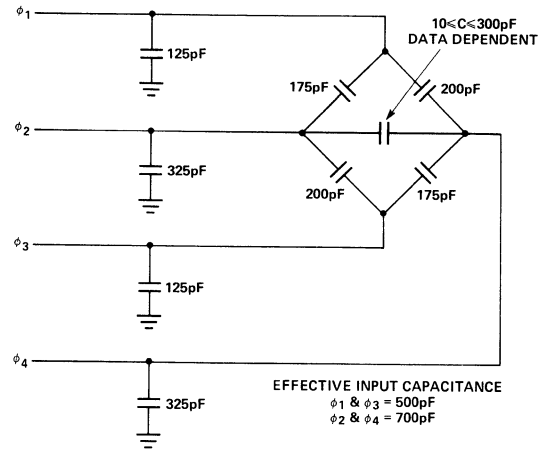
Four-Phase Clock Inputs

The four-phase clock inputs are internally connected to long electrodes used for several thin-oxide gates, resulting in high capacitance to the substrate on the clock inputs. In addition, considerable cross-coupling between adjacent clock exists due to the overlapping structure of the electrodes. The figure to the right shows the circuit equivalent of the clock inputs, indicating maximum capacitance values.

The equivalent circuit suggests two opposed clock driver requirements:

1. Ability to drive high-capacitance loads quickly.
2. Ability to suppress cross-coupled current transients.

The first requirement could ordinarily be met rather easily, if it weren't for the fact that the cross-coupled current, I, is proportional to the rate of change of the voltage, i.e., $I = C\frac{dv}{dt}$. For the quiescent driver to hold the coupled voltage to a minimum, the driver must have very low output impedance. However, when this driver becomes active the low output impedance increases the slope of the transitions which in turn increases coupling currents to the other drivers. This suggests that a driver have a controlled output transition time and a low output impedance characteristic in the quiescent state (high or low level). The Intel® 5244 meets these requirements.



5244 — CCD Clock Driver

The Intel® 5244 is a CMOS implemented fully TTL input compatible high voltage MOS driver, designed especially for the four phase clock inputs of the 2416. The device features very low DC power dissipation from a single +12V supply with output characteristics directly compatible with the 2416 clock input requirements.

The 5244 uses internal circuitry to control the cross-coupled voltage transients between the clock phases generated by the 2416. This internal circuitry limits the transition time to a specified range so that excessively fast transitions (<30ns) do not occur on the clock line. The entire operation is transparent to the user.

The 5244 is designed to drive four 2416s, but can drive fewer devices when loaded with additional capacitance to prevent a speedup in the transition times. Additional information on this and other aspects of the 5244 can be found on the 5244 data sheet.

Application Information

The Intel® 2416 is a charge coupled device (CCD) containing 16,384 bits of dynamic shift register storage available in a standard 18 pin plastic package. To minimize latency time (access time to any given bit in the device), the 2416 has been organized as 64 registers containing 256 bits each and, therefore, any bit can be accessed with a maximum of 255 shift operations. Since the minimum shift cycle requires 750 ns, the maximum latency time for the 2416 is less than 200μsec.

Access to the 64 recirculating registers is performed in a random access mode. A six bit address selects one of the 64 registers for read, write, or read/modify/write operations. These random access operations are performed between shift operations, and can be performed in any number or sequence as long as the basic shift frequency is maintained.

Because of substrate leakage currents the charge coupled storage mechanism is dynamic in nature. To satisfy the refresh requirements of the 2416, one shift operation must be performed every ten microseconds. A shift operation is completed on the falling edge of clock phase ϕ_1 or ϕ_3 and random access cycles may occur only between (1) the falling edge of ϕ_1 and the rising edge of ϕ_4 or (2) the falling edge of ϕ_3 and the rising edge of ϕ_2. This refresh requirement limits the number of random access cycles between successive shift operations to a maximum of 16.

Random access operations are performed in a manner which is very similar to any random access memory (RAM). All random access cycles are initiated with the rising edge and terminated with the falling edge of CE (Chip Enable). Read operations are performed when WE (Write Enable) remains low throughout a CE cycle. Data is strobed into the memory whenever WE is strobed high during a CE cycle as illustrated in the appropriate timing diagrams. CS (Chip Select) controls only the input and output circuits and is only effective when CE is high.

Typical Current Transients vs. Time

The oscilloscope photos in Figures 1 and 2 show typical I_{DD} current transients during shift and I/O cycles. The typical I_{BB} current during a shift cycle is shown in Figure 3.

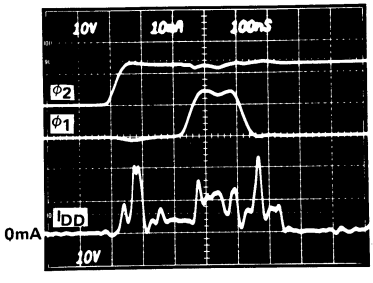


Figure 1. I_{DD} transient current during shift cycles.
I_{DD} scale: 10mA/div.

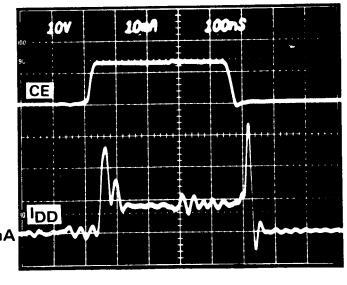


Figure 2. I_{DD} transient current during I/O cycles.
I_{DD} scale: 10mA/div.

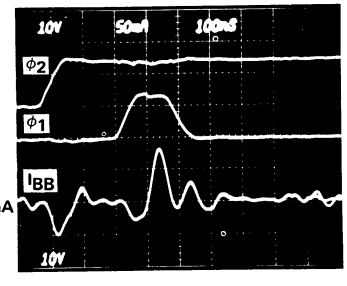


Figure 3. I_{BB} transient current during a shift cycle.
I_{BB} scale: 50mA/div.

5

Memory Support Circuits

MEMORY SUPPORT CIRCUITS

	Type	Description	No. of Pins	Electrical Characteristics Over Temperature		Supplies[V]	Page No.
				Input to Output Delay Max.	Power Dissipation[1] Maximum		
SCHOTTKY BIPOLAR	**3205**	1 of 8 Binary Decoder	16	18ns	350mW	+5	5-3
	3207A	Quad Bipolar to MOS Level Shifter and Driver	16	25ns	900mW	+5, +16, +19	5-7
	3207A-1	Quad Bipolar to MOS Level Shifter and Driver	16	25ns	1040mW	+5, +19, +22	5-11
	3208A	Hex Sense Amp for MOS Memories	18	20ns	600mW	+5	5-13
	3222	4K Dynamic RAM Refresh Controller	22	—	600mW	+5	5-19
	3232	4K Dynamic RAM Address Multiplexer and Refresh Counter	24	20ns	750mW	+5	5-25
	3242	16K Dynamic RAM Address Multiplexer and Refresh Counter	28	20ns	825mW	+5	5-29
	3245	Quad TTL to MOS Driver for 4K RAMs	16	32ns	388mW	+12, +5	5-33
	3404	High Speed 6-Bit Latch	16	12ns	375mW	+5	5-3
	3408A	Hex Sense Amp and Latch for MOS Memories	18	25ns	625mW	+5	5-13
CMOS	**5235**	Quad Low Power TTL to MOS Driver for 4K RAMs	16	125ns	240mW	12	5-37
	5235-1	High Speed Quad Low Power TTL to MOS Driver for 4K RAMs	16	95ns	240mW	12	
	5244	Quad CCD Driver	16	90ns	1260mW	12	5-41

Note 1. Power Dissipation calculated with maximum power supply current and nominal supply voltages.

3205 HIGH SPEED 1 OUT OF 8 BINARY DECODER
3404 HIGH SPEED 6-BIT LATCH

- **18ns Max. Delay Over 0°C to 75°C Temperature: 3205**
- **12ns Max. Data to Output Delay Over 0°C to 75°C Temperature: 3404**
- **Directly Compatible With DTL and TTL Logic Circuits**
- **Totem-Pole Output**
- **Low Input Load Current: .25mA Max., 1/6 Standard TTL Input Load**
- **Minimum Line Reflection: Low Voltage Diode Input Clamp**
- **Outputs Sink 10mA Min.**
- **16-Pin Dual In-Line Package**
- **Simple Expansion: Enable Inputs**

3205

The 3205 decoder can be used for expansion of systems which utilize memory components with active low chip select input. When the 3205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 3205 allow easy memory expansion. For very large memory systems, 3205 decoders can be cascaded such that each decoder can drive 8 other decoders for arbitrary memory expansions.

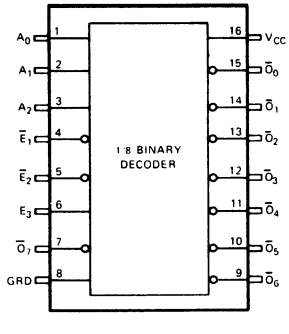
3404

The Intel 3404 contains six high speed latches organized as independent 4-bit and 2-bit latches. They are designed for use as memory data registers, address registers, or other storage elements. The latches act as high speed inverters when the "Write" input is "low".

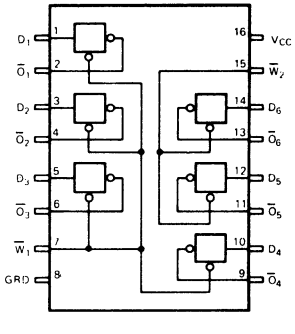
The Intel 3404 is packaged in a standard 16-pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION

3205



3404



Absolute Maximum Ratings*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		125 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

3205, 3404

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT		−0.25	mA	V_{CC} = 5.25V, V_F = 0.45V
I_R	INPUT LEAKAGE CURRENT		10	µA	V_{CC} = 5.25V, V_R = 5.25V
V_C	INPUT FORWARD CLAMP VOLTAGE		−1.0	V	V_{CC} = 4.75V, I_C = −5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} = 4.75V, I_{OL} = 10.0 mA
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	V_{CC} = 4.75V, I_{OH} = −1.5 mA
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} = 5.0V
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	−40	−120	mA	V_{CC} = 5.0V, V_{OUT} = 0V
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	V_{CC} = 5.0V, I_{OX} = 40 mA

3205 ONLY

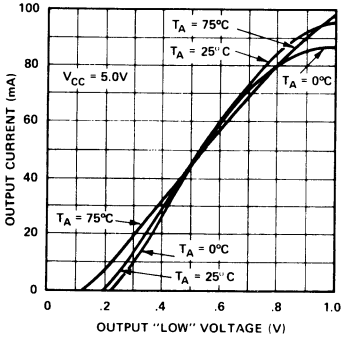
I_{CC}	POWER SUPPLY CURRENT		70	mA	V_{CC} = 5.25V, Outputs Open

3404 ONLY

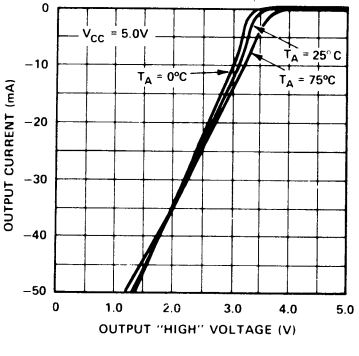
I_{CC}	POWER SUPPLY CURRENT		75	mA	V_{CC} = 5.25V, Outputs Open
I_{FW1}	WRITE ENABLE LOAD CURRENT PIN 7		−1.00	mA	V_{CC}=5.25V, V_W=0.45V
I_{FW2}	WRITE ENABLE LOAD CURRENT PIN 15		−0.50	mA	V_{CC}=5.25V, V_W=0.45V
I_{RW}	WRITE ENABLE LEAKAGE CURRENT		10	µA	V_R=5.25V

Typical Characteristics

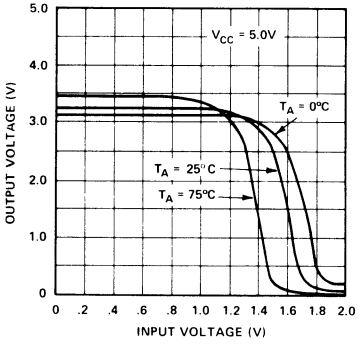
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



DATA TRANSFER FUNCTION



3205 - HIGH SPEED 1 OUT OF 8 BINARY DECODER

Switching Characteristics

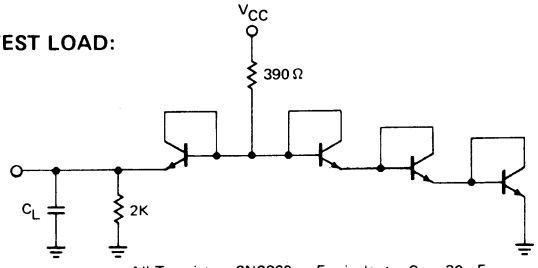
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

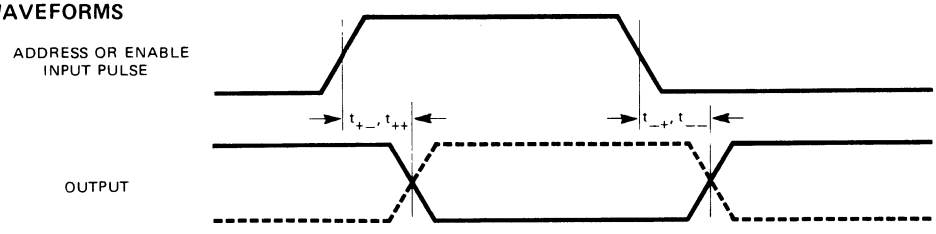
Measurements are made at 1.5V

TEST LOAD:



All Transistors 2N2369 or Equivalent. C_L = 30 pF

TEST WAVEFORMS



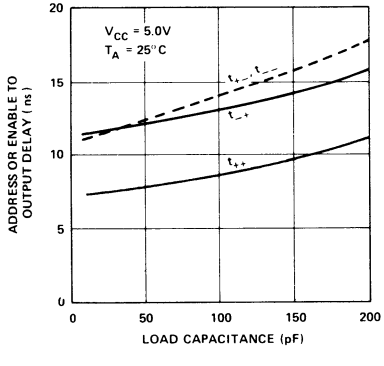
A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5% unless otherwise specified.

SYMBOL	PARAMETER		MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY		18	ns	
t_{-+}			18	ns	
t_{+-}			18	ns	
t_{--}			18	ns	
C_{IN} (1)	INPUT CAPACITANCE	P3205	4(typ.)	pF	f = 1 MHz, V_{CC} = 0V
		C3205	5(typ.)	pF	V_{BIAS} = 2.0V, T_A = 25°C

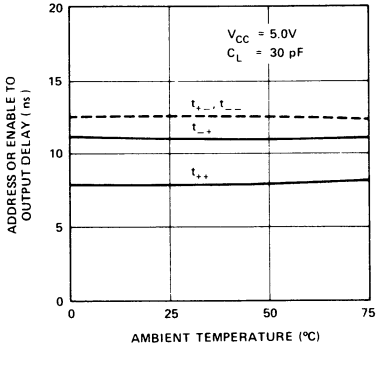
1. This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

ADDRESS OR ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



3404 - 6-BIT LATCH

Switching Characteristics

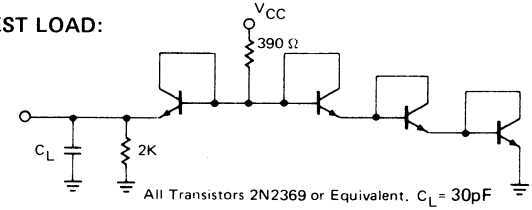
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

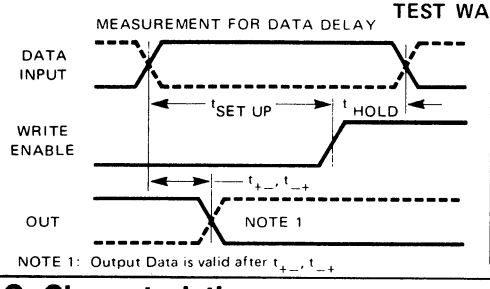
Input rise and fall times: 5 nsec between 1V and 2V

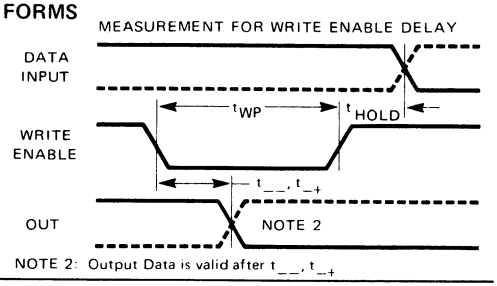
Measurements are made at 1.5V

TEST LOAD:



TEST WAVEFORMS





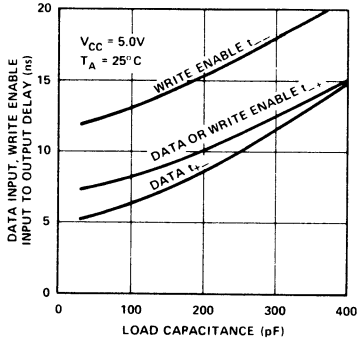
A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
t_{+-}, t_{-+}	DATA TO OUTPUT DELAY				12	ns	
t_{--}, t_{-+}	WRITE ENABLE TO OUTPUT DELAY				17	ns	
$t_{SET\ UP}$	TIME DATA MUST BE PRESENT BEFORE RISING EDGE OF WRITE ENABLE		12			ns	
t_{HOLD}	TIME DATA MUST REMAIN AFTER RISING EDGE OF WRITE ENABLE		8			ns	
t_{WP}	WRITE ENABLE PULSE WIDTH		15			ns	
C_{IND}(3)	DATA INPUT CAPACITANCE	P3404		4		pF	f = 1 MHz, V_{CC} = 0V
		C3404		5		pF	V_{BIAS} = 2.0V, T_A = 25°C
C_{INW}(3)	WRITE ENABLE CAPACITANCE	P3404		7		pF	f = 1 MHz, V_{CC} = 0V
		C3404		8		pF	V_{BIAS} = 2.0V, T_A = 25°C

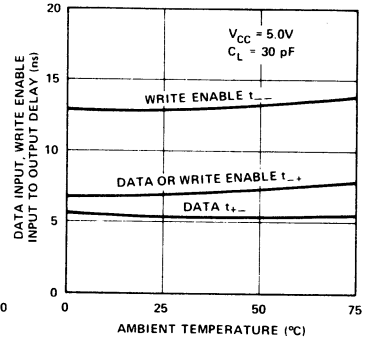
NOTE 3: This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

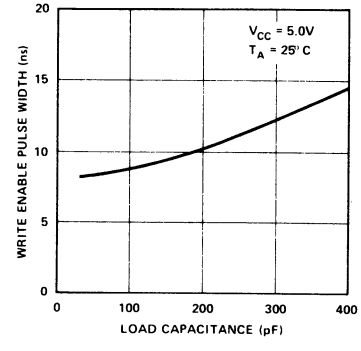
DATA INPUT, WRITE ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA INPUT, WRITE ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



WRITE ENABLE PULSE WIDTH VS. LOAD CAPACITANCE



3207A
QUAD BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER

- **High Speed, 45 nsec Max.-- Delay + Transition Time Over Temperature with 200 pF Load**
- **TTL & DTL Compatible Inputs**
- **1103 and 1103A Memory Compatible at Output**
- **Simplifies Design -- Replaces Discrete Components**
- **Easy to Use -- Operates from Standard Bipolar and MOS Supplies**
- **Minimum Line Reflection -- Input and Output Clamp Diodes**
- **High Input Breakdown Voltage -- 19 Volts**
- **CerDIP Package -- 16 Pin DIP**

MEMORY SUPPORT

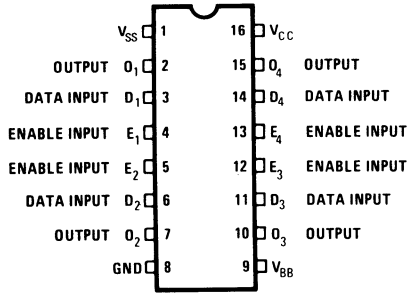
The 3207A is a Quad Bipolar-to-MOS level shifter and driver which accepts TTL and DTL input signals, and provides high output current and voltage suitable for driving MOS circuits. It is particularly suitable for driving the 1103 and 1103A memory chips. The circuit operates from a 5 volt TTL power supply, and V_{SS} and V_{BB} power supplies from the 1103 and 1103A.

The device features two common enable inputs per pair of devices which permits some logic to be done at their inputs, such as cenable and precharge decoding for the 1103 and 1103A.

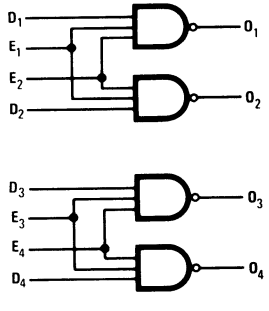
For the TTL inputs a logic "1" is V_{IH} and a logic "0" is V_{IL}. The 3207A outputs correspond to a logic "1" as V_{OL} and a logic "0" as V_{OH} for driving MOS inputs.

The 3207A is packaged in a hermetically sealed 16 pin ceramic dual-in-line package. The device performance is specified over the same temperature range as the 1103 and 1103A, i.e. from 0°C to +70°C.

PIN CONFIGURATION



LOGIC SYMBOL



Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature..... −65°C to +160°C
All Input Voltages and V_{SS}..... −1.0 to +21V
Supply Voltage V_{CC} ..... −1.0 to +7V
All Outputs and Supply Voltage
V_{BB} with respect to GND ..... −1.0 to +25V
Power Dissipation at 25°C..... 2 Watts (1)

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) Refer to the graph of Junction Temperature versus Total Power Dissipation on page 5-10 for other temperatures.

D. C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 16V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	$V_D = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{FE}	ENABLE INPUT LOAD CURRENT		−0.50	mA	$V_E = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{RD}	DATA INPUT LEAKAGE CURRENT		20	μA	$V_D = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{RE}	ENABLE INPUT LEAKAGE CURRENT		20	μA	$V_E = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 16V$, $V_{BB} = 19V$
V_{OL}	OUTPUT "LOW" VOLTAGE		.8 .7 .6	V(0°C) V(25°C) V(70°C)	$I_{OL} = 500\mu A$, $V_{CC} = 4.75V$ $V_{SS} = 16V$, $V_{BB} = 19V$ All Inputs at 2.0V
V_{OH} (MIN.)	OUTPUT "HIGH" VOLTAGE	$V_{SS} - .7$ $V_{SS} - .6$ $V_{SS} - .5$		V(0°C) V(25°C) V(70°C)	$I_{OH} = -500\mu A$, $V_{CC} = 5.0V$ $V_{SS} = 16V$, $V_{BB} = 19V$ All Inputs at 0.85V
V_{OH} (MAX.)			$V_{SS} + 1.0$	V	$I_{OH} = 5mA$, $V_{CC} = 5.0V$ $V_{SS} = 16V$, $V_{BB} = 19V$
I_{OL}	OUTPUT SINK CURRENT	100		mA	$V_O = 4V$, $V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$, $V_E = V_D = 2.0V$
I_{OH}	OUTPUT SOURCE CURRENT	−100		mA	$V_O = V_{SS} - 4V$, $V_{CC} = 5.0V$, $V_{SS} = 16V$ $V_{BB} = 19V$, $V_E = V_D = 0.85V$
V_{IL}	INPUT "LOW" VOLTAGE		1.0	V	$V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$
C_{IN}	INPUT CAPACITANCE	8(Typical)		pF	$V_{BIAS} = 2.0V$, $V_{CC} = 0V$

POWER SUPPLY CURRENT DRAIN:

All Outputs "Low"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		83	mA	$V_{CC} = 5.25V$, $V_{SS} = 16.8V$, $V_{BB} = 20.8V$ All Inputs Open
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		21	mA	
P_{TOTAL}	Total Power Dissipation		900	mW	

All Outputs "High"

I_{CC}	Current from V_{CC}		33	mA	$V_{CC} = 5.25V$, $V_{SS} = 16.8V$, $V_{BB} = 20.8V$ All Inputs Grounded
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		3	mA	
P_{TOTAL}	Total Power Dissipation		250	mW	

Standby Condition with $V_{CC} = 0V$, $V_{SS} = V_{BB}$

I_{CC}	Current from V_{CC}		0	mA	$V_{CC} = 0V$, $V_{SS} = 16.8V$, $V_{BB} = 16.8V$
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		250	μA	
P_{TOTAL}	Total Power Dissipation		10	mW	

Switching Characteristics

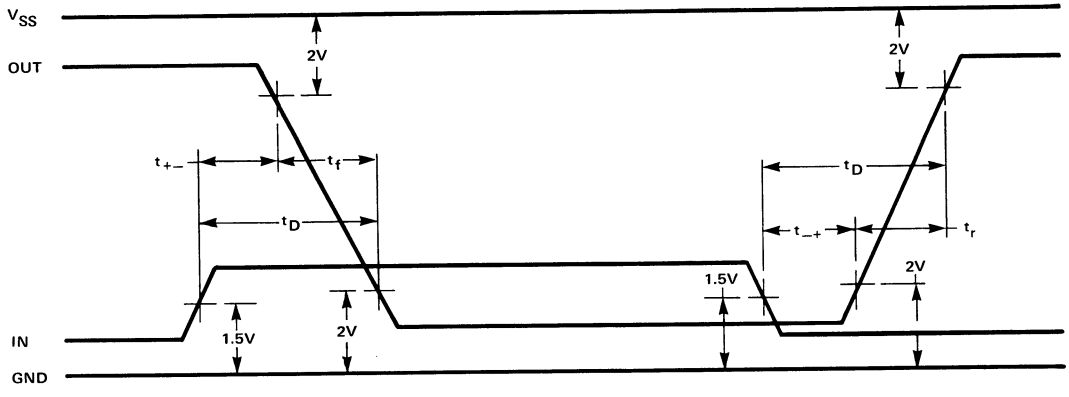
A.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 16V ±5%, V_{BB} = V_{SS} +3 to 4V, f = 2 MHz, 50% Duty Cycle

SYMBOL	TEST	LIMITS (ns)				
		C_L = 100 pF		C_L = 200 pF		DELAY DIFFERENTIAL (1) C_L = 200 pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	20	10	30	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

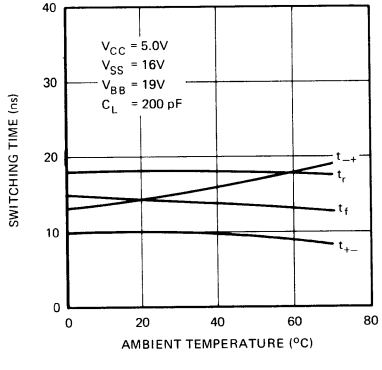
(1) This is defined as the maximum skew between any output in the same package, eg., all the input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

Waveforms

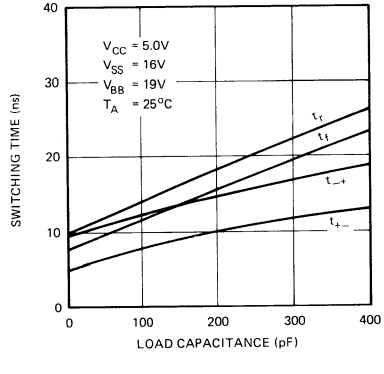


Typical Characteristics

SWITCHING TIME VS. AMBIENT TEMPERATURE

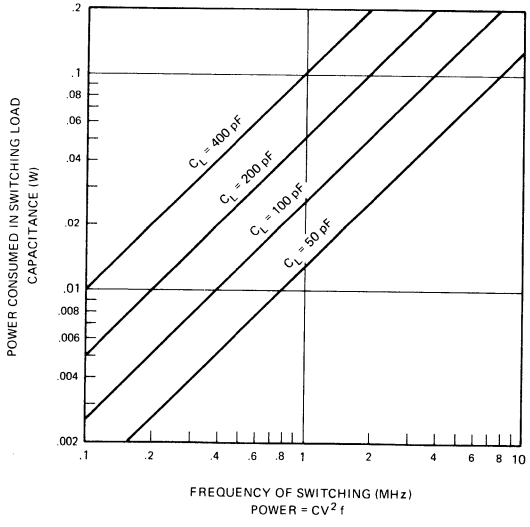


SWITCHING TIME VS. LOAD CAPACITANCE

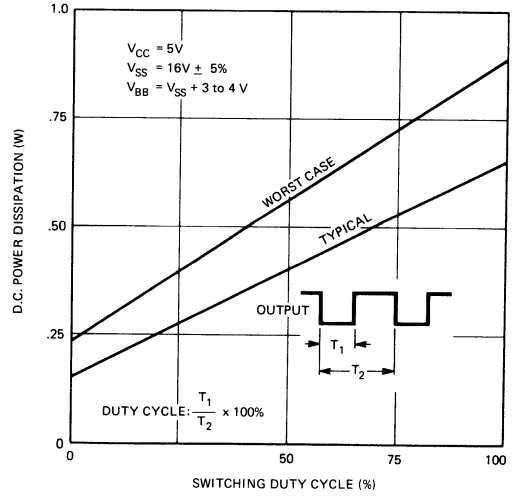


Power and Switching Characteristics

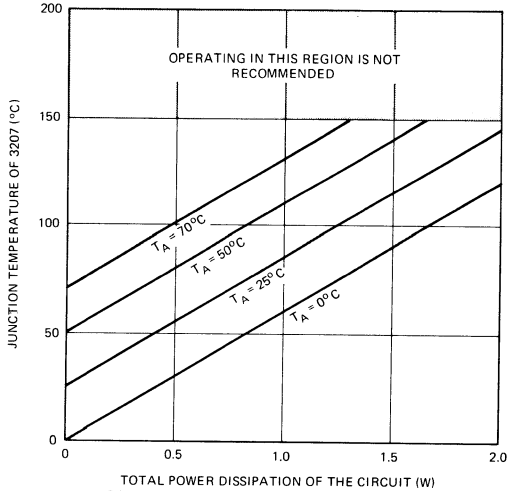
POWER CONSUMED IN CHARGING AND DISCHARGING LOAD CAPACITANCE OVER 0V TO 16V INTERVAL



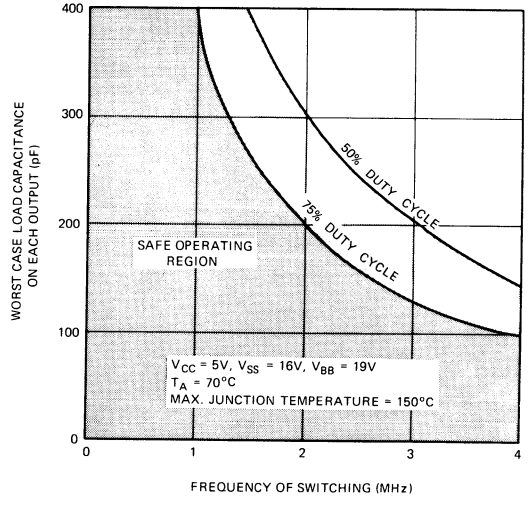
NO LOAD D.C. POWER DISSIPATION VS. OPERATING DUTY CYCLE



JUNCTION TEMPERATURE VS. TOTAL POWER DISSIPATION OF THE CIRCUIT



WORST CASELOAD CAPACITANCE ON EACH OUTPUT VS. FREQUENCY OF SWITCHING

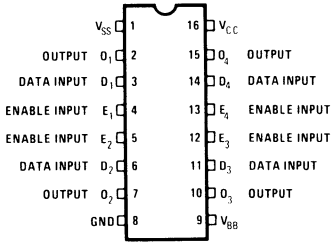


3207A-1
QUAD BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER

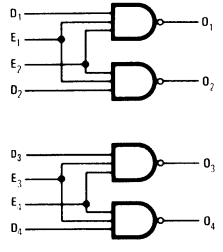
- **Power Supply Voltage Compatible with the High Voltage 1103-1**
- **1103-1 Memory Compatible at Output**

The Intel 3207A-1 is the high voltage version of the standard 3207A, and is compatible with the 1103-1. The 3207A-1 has all the same features as the standard 3207A. The absolute maximum ratings and pin configuration are repeated below for convenience, while the DC and AC characteristics appear below and on the next page.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to +55°C
Storage Temperature . . . . . −65°C to +160°C
All Input Voltages . . . . . −1.0 to +21 Volts
Supply Voltage V_{CC} . . . . . −1.0 to +7.0 Volts
All Outputs and Supply Voltages V_{BB} and V_{SS} with respect to GND . . . . . −1.0 to +25 Volts
Power Dissipation at 25°C . . . . . 2 Watts

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics $T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	$V_D = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 19V$, $V_{BB} = 23V$
I_{FE}	ENABLE INPUT LOAD CURRENT		−0.50	mA	$V_E = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 19V$, $V_{BB} = 23V$
I_{RD}	DATA INPUT LEAKAGE CURRENT		20	μA	$V_D = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 19V$, $V_{BB} = 23V$
I_{RE}	ENABLE INPUT LEAKAGE CURRENT		20	μA	$V_E = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 19V$, $V_{BB} = 23V$
V_{OL}	OUTPUT "LOW" VOLTAGE		0.8 0.7 0.6	V(0°C) V(25°C) V(55°C)	$I_{OL} = 500\mu A$, $V_{CC} = 4.75V$ $V_{SS} = 19V$, $V_{BB} = 23V$ All Inputs at 2.0V
V_{OH} (MIN.)	OUTPUT "HIGH" VOLTAGE	$V_{SS} - 0.7$ $V_{SS} - 0.6$ $V_{SS} - 0.5$		V(0°C) V(25°C) V(55°C)	$I_{OH} = -500\mu A$, $V_{CC} = 5.0V$ $V_{SS} = 19V$, $V_{BB} = 23V$ All Inputs at 0.85V
V_{OH} (MAX.)			$V_{SS} + 1.0$	V	$I_{OH} = 5mA$, $V_{CC} = 5.0V$ $V_{SS} = 19V$, $V_{BB} = 23V$
I_{OL}	OUTPUT SINK CURRENT	100		mA	$V_O = 4V$, $V_{CC} = 5.0V$, $V_{SS} = 19V$, $V_{BB} = 23V$, $V_E = V_D = 2.0V$
I_{OH}	OUTPUT SOURCE CURRENT	−100		mA	$V_O = V_{SS} - 4V$, $V_{CC} = 5.0V$, $V_{SS} = 19V$ $V_{BB} = 23V$, $V_E = V_D = 0.85V$
V_{IL}	INPUT "LOW" VOLTAGE		1.0	V	$V_{CC} = 5.0V$, $V_{SS} = 19V$, $V_{BB} = 23V$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0V$, $V_{SS} = 19V$, $V_{BB} = 23V$
C_{IN}	INPUT CAPACITANCE		8(Typical)	pF	$V_{BIAS} = 2.0V$, $V_{CC} = 0V$

D.C. Characteristics (Continued) $T_A = 0°C$ to $+55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

POWER SUPPLY CURRENT DRAIN:

All Outputs "Low"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		83	mA	$V_{CC} = 5.25V$, $V_{SS} = 20V$, $V_{BB} = 24V$ All Inputs Open
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		25	mA	
P_{TOTAL}	Total Power Dissipation		1040	mW	

All Outputs "High"

I_{CC}	Current from V_{CC}		33	mA	$V_{CC} = 5.25V$, $V_{SS} = 20V$, $V_{BB} = 24V$ All Inputs Grounded
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		5	mA	
P_{TOTAL}	Total Power Dissipation		297	mW	

Standby Condition with $V_{CC} = 0V$, $V_{SS} = V_{BB}$

I_{CC}	Current from V_{CC}		0	mA	$V_{CC} = 0V$, $V_{SS} = 20V$, $V_{BB} = 20V$
I_{SS}	Current from V_{SS}		500	μA	
I_{BB}	Current from V_{BB}		500	μA	
P_{TOTAL}	Total Power Dissipation		15	mW	

MEMORY SUPPORT

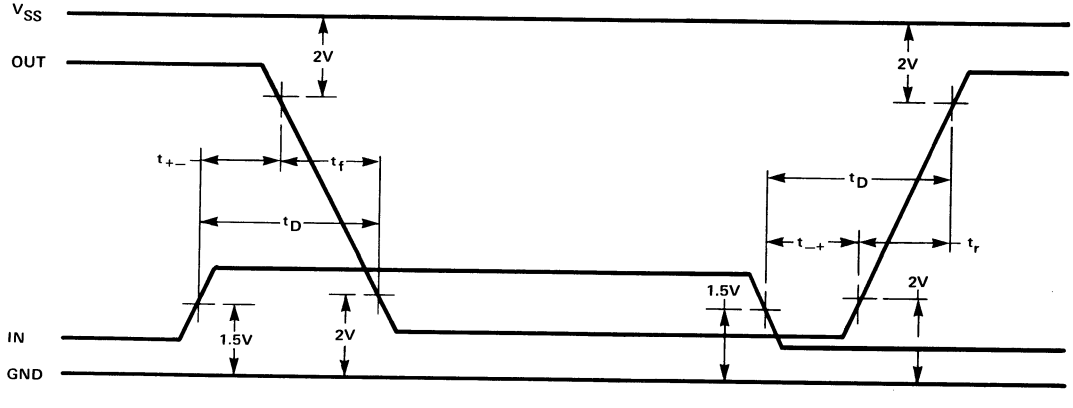
A.C. Characteristics

$T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} = V_{SS} + 3$ to $4V$, $f = 2$ MHz, 50% Duty Cycle

SYMBOL	TEST	LIMITS (ns)				
		$C_L = 100$ pF		$C_L = 200$ pF		DELAY DIFFERENTIAL (1) $C_L = 200$ pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	25	10	35	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

(1) This is defined as the maximum skew between any output in the same package, eg., all the input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

Waveforms



HEX BIPOLAR SENSE AMPLIFIERS FOR MOS CIRCUITS

3208A HEX SENSE AMPLIFIER
3408A HEX SENSE AMPLIFIER WITH LATCHES

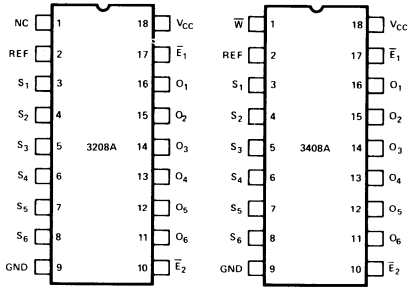
- **High Speed—20 nsec. max.**
- **Wire-OR Capability— Open Collector Output..3208A Three-State Output 3408A**
- **Single 5 V Power Supply**
- **Input Level Compatible with 1103 Output**
- **Two Enable Inputs**
- **Minimum Line Reflection .... Low Voltage Diode Input Clamp**
- **Plastic 18 Pin Dual In-Line Package**
- **Schottky TTL**

The Intel 3208A is a high speed hex sense amplifier designed to sense the output signals of the 1103 memory. The device features two separate enable inputs each controlling the output state of three sense amplifiers, and a common voltage reference input. OR-tie capability is available with the 3208A open collector TTL compatible output.

The 3408A is a hex sense amplifier with a latch circuit connected to each amplifier. The sensed data may be stored in the latches through application of a write pulse. The 3408A has three-state TTL outputs, hence in the non-enabled state the outputs float allowing wire-OR memory expansion. The latches may be bypassed by grounding the write input pin. Under this condition, the 3408A functions as a hex sense amplifier.

The 3208A and 3408A operate from a single +5 volt power supply. Device performance is specified over the complete ambient temperature range of 0°C to 70°C and over a V_{CC} supply voltage range of 5 volts ±5%. The 3208A and 3408A are packaged in an 18 pin plastic dual in-line package.

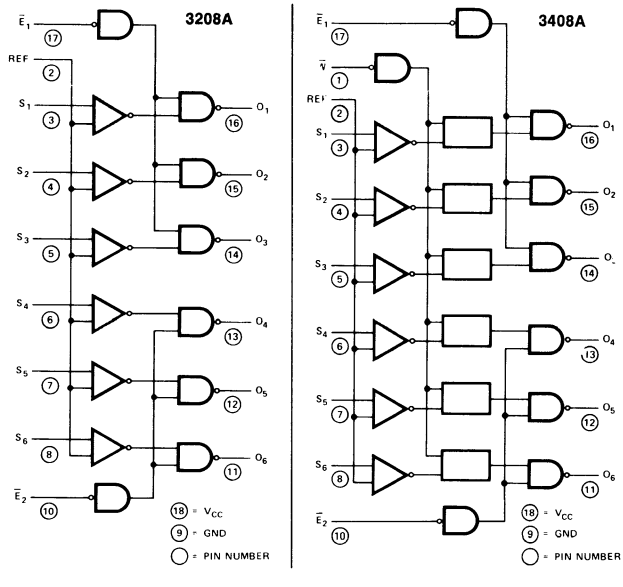
PIN CONFIGURATIONS



PIN NAMES

$S_1, S_2, S_3, S_4, S_5, S_6$	SENSE AMP INPUTS
$\bar{E}_1, \bar{E}_2$	ENABLE INPUTS
REF	REFERENCE INPUT
$O_1, O_2, O_3, O_4, O_5, O_6$	OUTPUTS (Non-inverting)
$\bar{W}$	WRITE INPUT (3408A only)

BLOCK DIAGRAMS



Absolute Maximum Ratings*

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +160°C
All Outputs or Supply Voltage	−0.5 to +7 Volts
All TTL Input Voltages	−1 to +5.5 Volts
All Sense Input Voltages	−1 to +1 Volt
Output Currents Total	300mA
Input Current	125mA

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at this or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics for 3208A T_A = 0°C to 70°C, V_{CC} = 5V ±5%

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
I_{FE}	INPUT LOAD CURRENT ON ENABLE INPUT			−0.25	mA	V_{CC} = 5.25V V_F = 0.45V
I_{RE}	INPUT LEAKAGE CURRENT ON ENABLE INPUT			20	μA	V_{CC} = 4.75V V_R = 5.25V
V_{IH}	INPUT "HIGH" VOLTAGE ON ENABLE INPUT	2.0			V	V_{CC} = 5.0V
V_{IL}	INPUT "LOW" VOLTAGE ON ENABLE INPUT			0.85	V	V_{CC} = 5.0V
V_{OL}	OUTPUT "LOW" VOLTAGE			0.45	V	V_{CC} = 4.75V I_{OL} = 10mA
I_{CEX}	OUTPUT LEAKAGE CURRENT			100	μA	V_{CC} = 5.25V V_{CEX} = 5.25V
I_{REF}	INPUT CURRENT ON REFERENCE INPUT			−150	μA	V_{CC} = 5.25V V_{REF} = 100mV
I_S	INPUT CURRENT ON SENSE AMP INPUT			−25	μA	V_{CC} = 5.25V V_S = 100mV
V_{SH}	INPUT "HIGH" VOLTAGE FOR SENSE AMP INPUT	V_{REF}			mV	V_{CC} = 4.75 to 5.25V V_{REF} = 100 to 200mV
V_{SL}	INPUT "LOW" VOLTAGE FOR SENSE AMP INPUT			V_{REF} −50	mV	V_{CC} = 4.75 to 5.25V V_{REF} = 100 to 200mV
V_{REF}	OPERATING RANGE OF REFERENCE VOLTAGE	100		200	mV	V_{CC} = 4.75 to 5.25V
I_{CC}	POWER SUPPLY CURRENT			120	mA	V_{CC} = 5.25V
V_C	INPUT CLAMP VOLTAGE ON ALL INPUTS			−1.0	V	V_{CC} = 4.75V I_C = −5.0mA
V_{SD}	SENSE INPUT CLAMP DIODE VOLTAGE			1.0	V	V_{CC} = 5.0V I_D = 5.0mA

3208A TRUTH TABLE

INPUTS		OUTPUT
Sense Amp	Enable	
$<V_{REF}$ −50mV	L	L
$>V_{REF}$	L	H
X	H	H

X = Don't care

D. C. Characteristics for 3408A $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
I_{FE}	INPUT LOAD CURRENT ON ENABLE INPUT			−0.25	mA	$V_{CC} = 5.25V$ $V_F = 0.45V$
I_{RE}	INPUT LEAKAGE CURRENT ON ENABLE INPUT			20	μA	$V_{CC} = 4.75V$ $V_R = 5.25V$
I_{FW}	INPUT LOAD CURRENT ON WRITE INPUT			−0.25	mA	$V_{CC} = 5.25V$ $V_F = 0.45V$
I_{RW}	INPUT LEAKAGE CURRENT ON WRITE INPUT			20	μA	$V_{CC} = 4.75V$ $V_R = 5.25V$
V_{IH}	INPUT "HIGH" VOLTAGE ON ENABLE AND WRITE INPUT	2.0			V	$V_{CC} = 5.0V$
V_{IL}	INPUT "LOW" VOLTAGE ON ENABLE AND WRITE INPUT			0.85	V	$V_{CC} = 5.0V$
V_{OL}	OUTPUT "LOW" VOLTAGE			0.45	V	$V_{CC} = 4.75V$ $I_{OL} = 10mA$
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.4			V	$V_{CC} = 4.75V$ $I_{OH} = -1.5mA$
$\lvert I_O \rvert$	OUTPUT LEAKAGE CURRENT FOR HIGH IMPEDANCE STATE			100	μA	$V_{CC} = 5.25V$ $V_O = 0.45V/5.25V$
I_{SC}	OUTPUT SHORT CIRCUIT CURRENT	−40		−100	mA	$V_{CC} = 5.0V$ $V_O = 0V$
I_{REF}	INPUT CURRENT ON REFERENCE INPUT			−150	μA	$V_{CC} = 5.25V$ $V_{REF} = 100mV$
I_S	INPUT CURRENT ON SENSE INPUT			−25	μA	$V_{CC} = 5.25V$ $V_S = 100mV$
V_{SH}	INPUT "HIGH" VOLTAGE FOR SENSE AMP INPUT	V_{REF}			mV	$V_{CC} = 4.75$ to $5.25V$ $V_{REF} = 100$ to $200mV$
V_{SL}	INPUT "LOW" VOLTAGE FOR SENSE AMP INPUT			V_{REF} −60	mV	$V_{CC} = 4.75$ to $5.25V$ $V_{REF} = 100$ to $200mV$
V_{REF}	OPERATING RANGE OF REFERENCE VOLTAGE	100		200	mV	$V_{CC} = 4.75$ to $5.25V$
I_{CC}	POWER SUPPLY CURRENT			125	mA	$V_{CC} = 5.25V$
V_C	INPUT CLAMP VOLTAGE ON ALL INPUTS			−1.0	V	$V_{CC} = 4.75V$ $I_C = -5.0V$
V_{SD}	SENSE INPUT CLAMP DIODE VOLTAGE			1.0	V	$V_{CC} = 5.0V$ $I_D = 5.0mA$

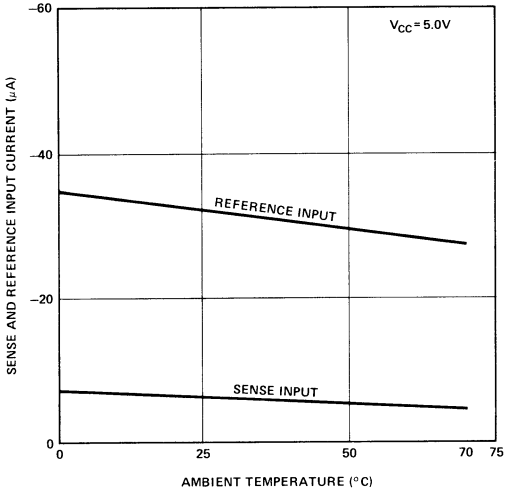
3408A TRUTH TABLE

INPUTS			OUTPUT
Sense Amp	Enable	Write	
$< V_{REF}$ −60mV	L	L	L
$> V_{REF}$	L	L	H
X	L	H	Previous Data Stored
X	H	X	High Z*

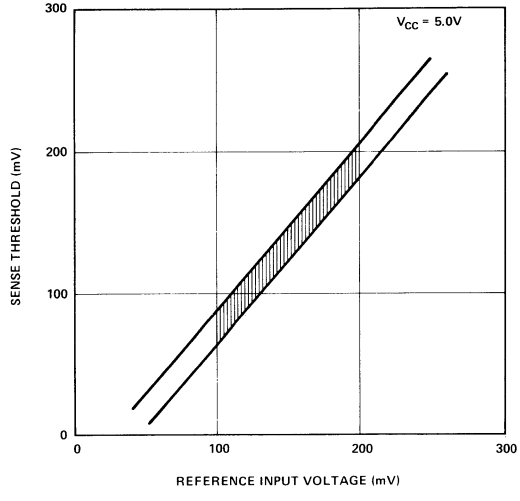
X = Don't care
*The output of the 3408A is three-state, hence when not enabled the output is a high impedance.

Typical D. C. Characteristics for 3208A/3408A

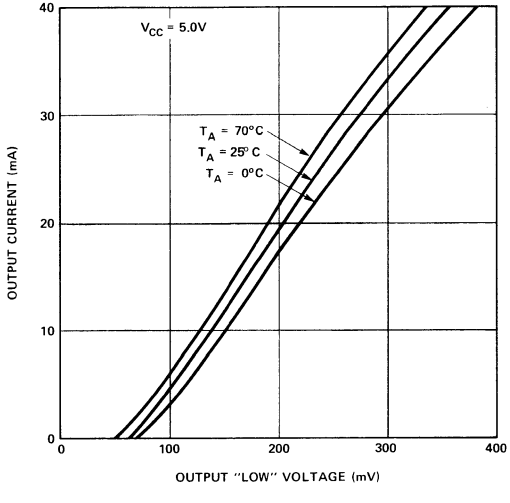
SENSE AND REFERENCE INPUT CURRENT VS. AMBIENT TEMPERATURE



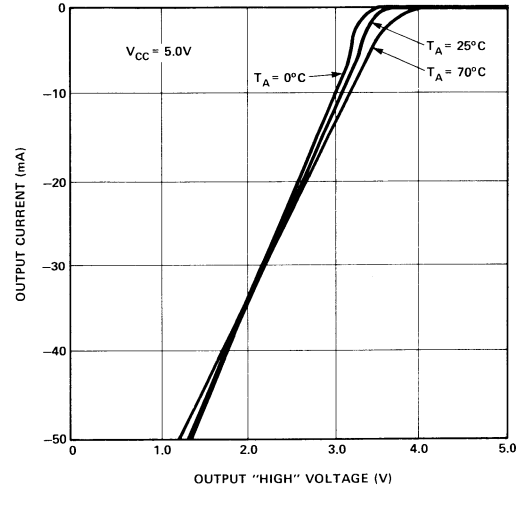
SENSE THRESHOLD VS. REFERENCE INPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

3208A

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
t_{S-}	SENSE AMP INPUT TO OUTPUT DELAY			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E-}	ENABLE INPUT TO OUTPUT DELAY			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E+}				25		

3408A

t_{WP}	WRITE PULSE WIDTH	30			ns	D.C. LOAD = 10mA C_L = 30pF
t_{S-}	SENSE AMP INPUT TO OUTPUT DELAY			25	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E-}	ENABLE INPUT TO OUTPUT DELAY, LATCH STORES "LOW"			20	ns	D.C. LOAD = 10mA C_L = 30pF
t_{E+}	ENABLE INPUT TO OUTPUT DELAY, LATCH STORES "HIGH"			25	ns	D.C. LOAD = 10mA C_L = 30 pF

Capacitance[1] $T_A = 25°C$, f = 1 MHz

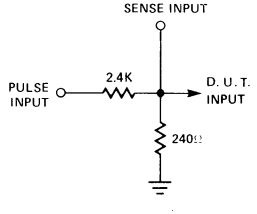
SYMBOL	TEST	LIMITS TYP.	LIMITS MAX.
C_O	V_{CC} = 0V, V_{BIAS} = 2.0V	8	12
C_{INE}	ENABLE INPUT V_{CC} = 0V, V_{BIAS} = 2.0V	6	10
C_{INS}	SENSE INPUT V_{CC} = 0V, V_{BIAS} = 0V	6	10

(1) This parameter is periodically sampled and is not 100% tested.

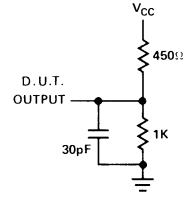
Switching Characteristics

CONDITIONS OF TEST

- Input Pulse amplitude: 2.5V for all TTL compatible inputs and 2.5V through a resistor network as shown below for sense input.
- Input Pulse rise and fall times: 5ns.
- Speed measurements are made at 1.5V for all TTL compatible inputs and outputs, and for sense input, see network and waveforms below. V_{REF} is set at 150mV.

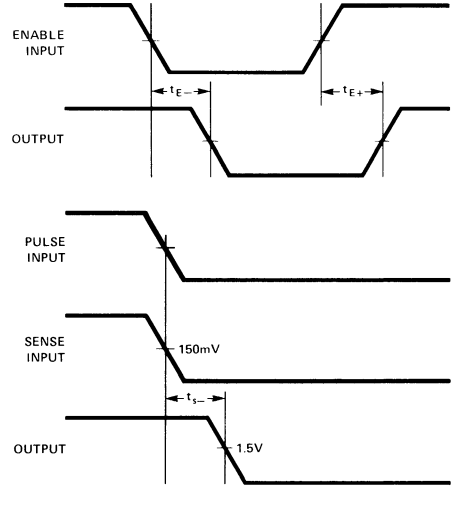


10mA TEST LOAD

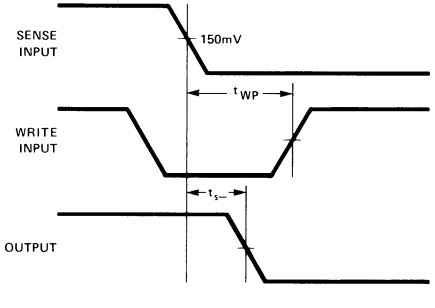


Waveforms

3208A/3408A



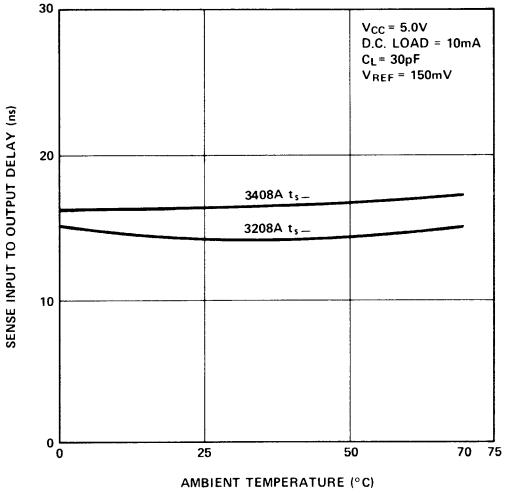
3408A ONLY



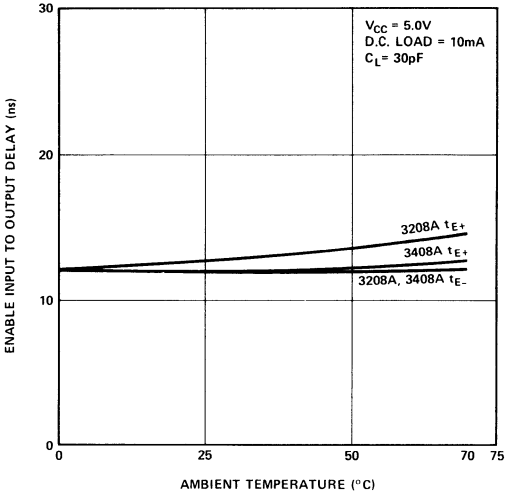
MEMORY SUPPORT

Typical A. C. Characteristics

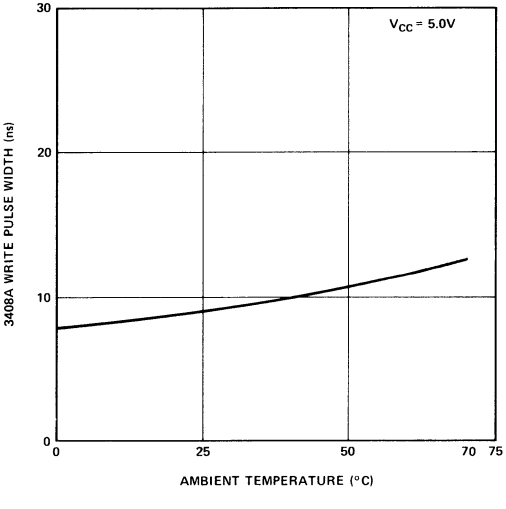
SENSE INPUT TO OUTPUT DELAY
VS. AMBIENT TEMPERATURE



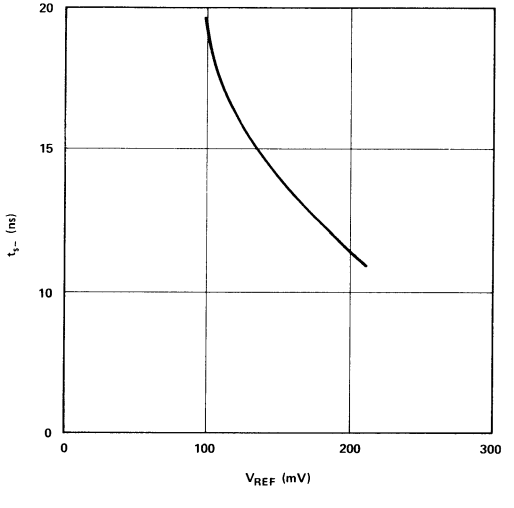
ENABLE INPUT TO OUTPUT DELAY
VS. AMBIENT TEMPERATURE



3408A WRITE PULSE WIDTH VS.
AMBIENT TEMPERATURE



SENSE INPUT TO OUTPUT DELAY
VS. REFERENCE INPUT VOLTAGE



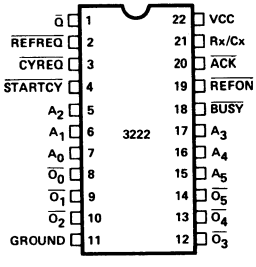
REFRESH CONTROLLER FOR 4K DYNAMIC RANDOM ACCESS MEMORIES

- **Ideal for use in 2107A, 2107B Systems**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 22-Pin DIP**
- **Adjustable Refresh Timing Oscillator**
- **6-Bit Address Multiplexer**
- **6-Bit Refresh Address Counter**
- **Refresh Cycle Controller**

The Intel® 3222 is a refresh controller for dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). The device contains an accurate refresh timer (whose frequency can be set by an external resistor and capacitor), plus all necessary control and I/O circuitry to provide for the refresh requirements of dynamic RAMs. The chip's high performance makes it especially suitable for use with high speed N-channel RAMs like the Intel® 2107B. The 3222 is well suited for asynchronous dynamic memory systems.

The 3222 operates from a single +5 volt power supply and is specified for operation over a 0°C to 75°C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process.

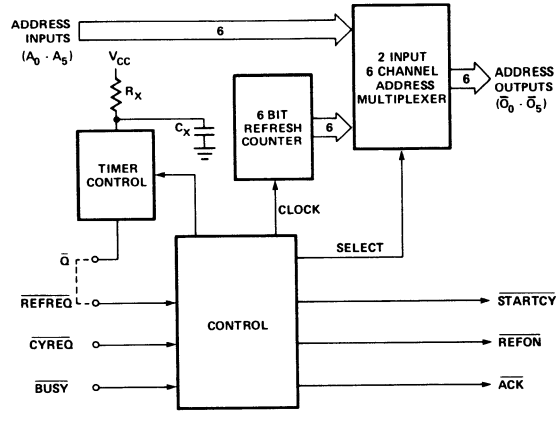
PIN CONFIGURATION



PIN NAMES

$A_0 - A_5$	ADDRESS INPUTS	$\overline{O}_0 - \overline{O}_5$	ADDRESS OUTPUTS
$\overline{ACK}$	ACKNOWLEDGE OUTPUT	$\overline{Q}$	INTERNAL REFRESH REQUEST LATCH OUTPUT
BUSY	BUSY INPUT	REFON	REFRESH ON OUTPUT
CYREQ	CYCLE REQUEST INPUT	REFREQ	REFRESH REQUEST INPUT
		RxCx	RC TIE POINT
		STARTCY	START CYCLE OUTPUT
		V_{CC}	+5V SUPPLY

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65° to +125°C
Storage Temperature . . . . . -65° to +160°C
All Input, Output or Supply Voltages . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 100 mA
Power Dissipation . . . . . 1 W

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{FB}	Input Load Current $\overline{BUSY}$		0.40	1	mA	V_{IN} = 0.45V
I_{FO}	Input Load Current All Other Inputs		0.05	0.25	mA	V_{IN} = 0.45V
I_{RB}	Input Leakage Current $\overline{BUSY}$		<1	50	μA	V_{IN} = V_{CC}
I_{RO}	Input Leakage Current All Other Inputs		<1	20	μA	V_{IN} = 5.25V
V_{CLAMP}	Input Clamp Voltage		-0.76	-1	V	I_C = -5.0mA
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{CC}	Power Supply Current		91	120	mA	V_{CC} = 5.25V
I_{SC}	Output High Short Circuit Current		-48	-70	mA	V_{OUT} = 0V V_{CC} = 5.25V
V_{OL}	Output Low Voltage		0.32	0.45	V	I_{OL} = 5mA
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_5$)	2.6	3.1		V	I_{OH} = -1mA V_{CC} = 4.75V
V_{OH1}	Output High Voltage (All Other Outputs)	2.4	3.0		V	I_{OH} = -1mA V_{CC} = 4.75V

Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

Capacitance[2], T_A = 25°C

Symbol	Test	Limits (pF)		Conditions
		Typ.	Max.	
C_{IN} (Address)	Input Capacitance	5	10	V_{bias} = 2.0V
C_{IN} ($\overline{CYREQ}$)	Input Capacitance	6	10	V_{CC} = 0V
C_{IN} ($\overline{BUSY}$)	Input Capacitance	20	30	f = 1MHz

Note 2: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics

All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C. Load = 1 TTL, C_L = 15pF.
Conditions of Test: Input pulse amplitude: 3V, Input rise and fall times: 5ns between 1V and 2V. Measurements are made at 1.5V.

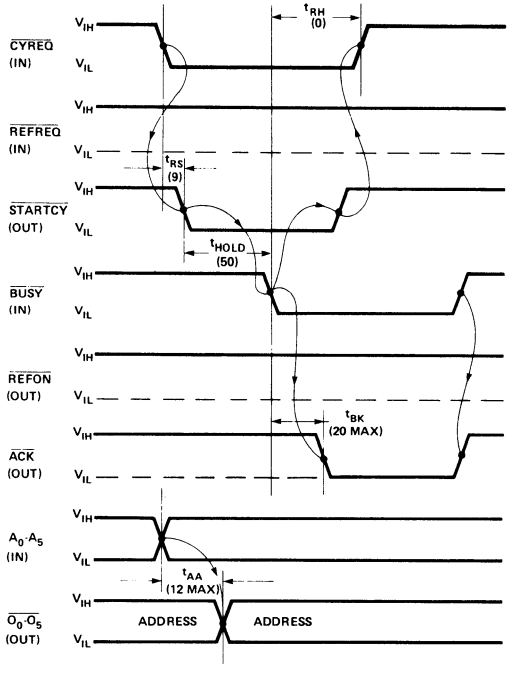
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
t_{AA}	Address In to Address Out		7	12	ns	$\overline{BUSY}$ = V_{IH}
t_{BAM}	$\overline{BUSY}$ In to Address Out		21	28	ns	
t_{BAR}	$\overline{BUSY}$ In to Counter Out		18	27	ns	
t_{BK}	$\overline{BUSY}$ In to $\overline{ACK}$ Out		14	20	ns	$\overline{REFREQ}$ = V_{IH}, $\overline{CYREQ}$ = V_{IL}
t_{BR}	$\overline{BUSY}$ In to $\overline{REFON}$ Out		15	24	ns	
t_{BS}	$\overline{BUSY}$ In to $\overline{STARTCY}$ Out	4	7	14	ns	$\overline{CYREQ}$ = V_{IL}
t_{HOLD}	$\overline{BUSY}$ Hold Time	50			ns	External Delay between $\overline{STARTCY}$ and $\overline{BUSY}$
t_{RH}	$\overline{CYREQ}$ or $\overline{REFREQ}$ Hold Time	0			ns	External Delay after $\overline{BUSY}$
t_{RR}	$\overline{REFREQ}$ to $\overline{REFON}$		18	26	ns	$\overline{CYREQ}$ and $\overline{BUSY}$ = V_{IH}, No priority contention between $\overline{REFREQ}$ and $\overline{CYREQ}$
t_{RRC}	$\overline{REFREQ}$ to $\overline{REFON}$		33	45	ns	$\overline{BUSY}$ = V_{IH}
t_{RS}	$\overline{CYREQ}$ or $\overline{REFREQ}$ In to $\overline{STARTCY}$ Out	9	14	21	ns	$\overline{BUSY}$ = V_{IH}
t_{Setup}	$\overline{BUSY}$ Setup Time	120			ns	$\overline{BUSY}$ = V_{IL} During Refresh

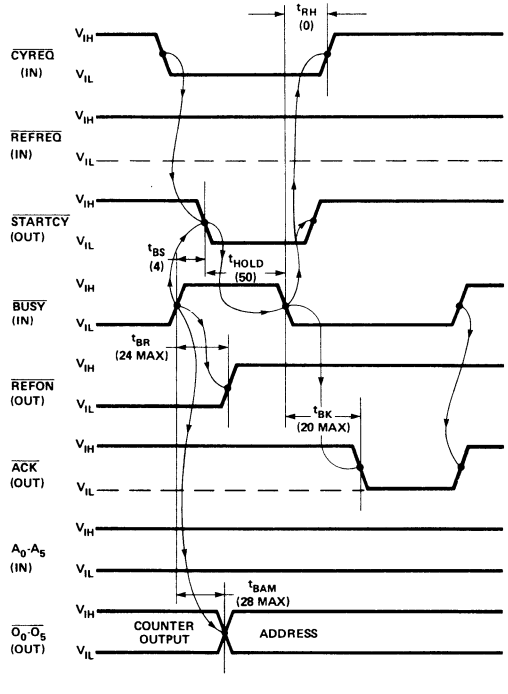
Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

A. SYSTEM MEMORY CYCLE WITH MEMORY NOT BUSY

B. SYSTEM MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING REFRESH CYCLE)

(Numbers in parentheses are minimum values in ns unless otherwise specified.)

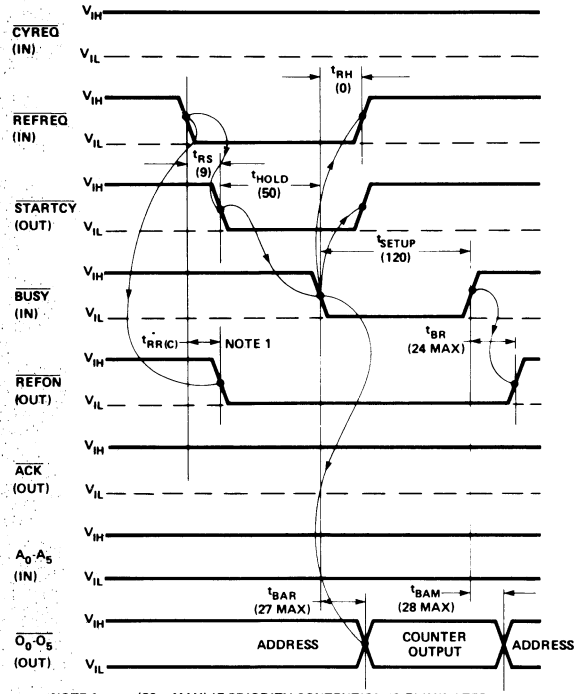




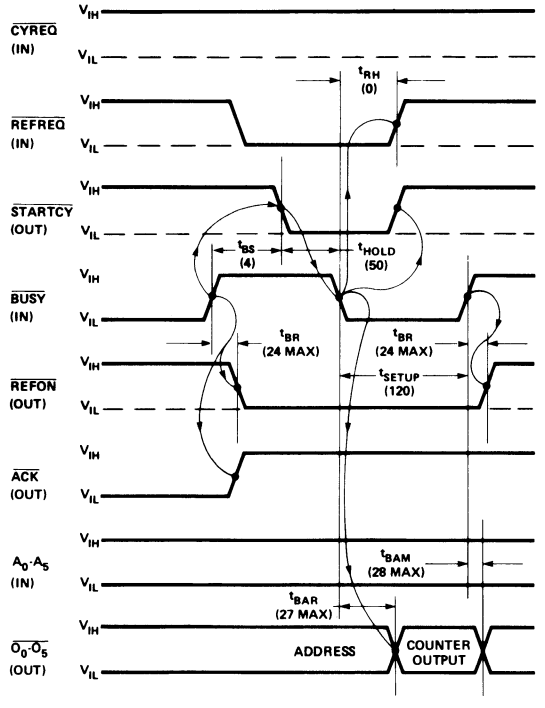
C. REFRESH MEMORY CYCLE WITH MEMORY NOT BUSY

D. REFRESH MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING SYSTEM CYCLE)

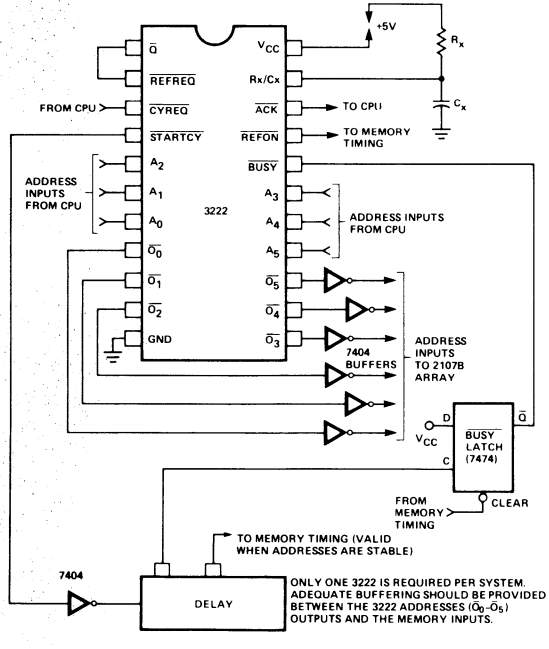
(Numbers in parentheses are minimum values in ns unless otherwise specified.)



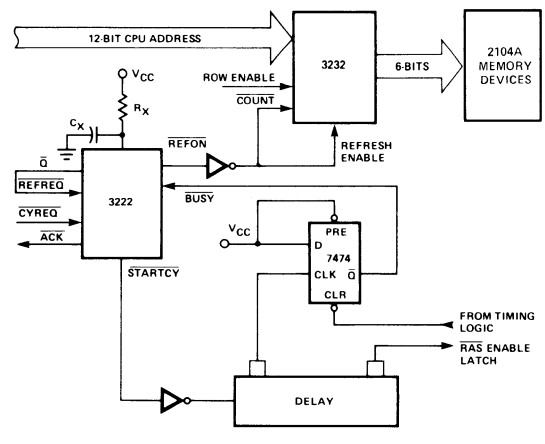
NOTE 1: t_{RR} (26ns MAX) IF PRIORITY CONTENTION IS ELIMINATED; t_{RRC}



E. TYPICAL APPLICATION OF 3222 REFRESH CONTROLLER IN A 2107B SYSTEM



F. USE OF 3222 FOR REFRESH TIMING AND CONTROL IN A 2104A SYSTEM



PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{Q}$	Output of the internal Refresh Request latch. This pin may be connected to the Refresh Request input ($\overline{REFREQ}$) directly for asynchronous sequential mode refresh or indirectly through control logic for burst mode or synchronous mode refresh (see text).
2	$\overline{REFREQ}$	Refresh Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a system cycle request did not occur first.
3	$\overline{CYREQ}$	System Memory Cycle Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a refresh request did not occur first.
4	$\overline{STARTCY}$	Output signal indicating to external circuitry that a memory cycle (system or refresh) is to begin. See text for timing considerations for a refresh cycle.
5-7 15-17	A_0-A_5	Low order system address inputs. These addresses are multiplexed to the address output pins ($\overline{O}_0$-$\overline{O}_5$) during a system cycle.
8-10	$\overline{O}_0$-$\overline{O}_5$	Low order memory address outputs. During a system cycle these outputs give the low order (A_0-A_5) address of a memory access. During a refresh cycle these outputs give the refresh address (generated internal to the 3222).
11	GROUND	Ground.
18	$\overline{BUSY}$	An externally generated signal which the 3222 monitors to determine memory system status. If $\overline{BUSY}$ is high the memory is not busy and a system or refresh cycle may begin. If $\overline{BUSY}$ is low the memory is being accessed for a data I/O or refresh cycle and no other cycle may begin.
19	$\overline{REFON}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a refresh cycle (Refresh On).
20	$\overline{ACK}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a system cycle (system cycle request accepted and acknowledged).
21	RX/CX	Connection point for the RC network which determines the refresh period for sequential refresh mode. (See Refresh Control section).
22	V_{CC}	+5 volt supply.

FUNCTIONAL DESCRIPTION

The Intel® 3222 performs the four basic functions of a refresh controller by:

1. Providing a refresh timing oscillator.
2. Generating six bit refresh addresses.
3. Multiplexing refresh and system addresses to the six low order address inputs ($\overline{O}_0$-$\overline{O}_5$).
4. Providing control signals for both refresh and memory cycle accesses.

As shown in the pin configuration figure, the 3222 has as inputs the six low order (A_0-A_5) system addresses. These addresses are internally multiplexed with six internally generated refresh addresses. The output of these multiplexers provide the six low order addresses to the memory array.

The block diagram shows the four main circuit categories of the 3222. An explanation of the workings of each of these categories is given in the Device Operation section from a users point of view.

DEVICE OPERATION

Operation of the Intel® 3222 Refresh Controller is most easily explained by considering five conditions presented by the three input control lines Cycle Request ($\overline{CYREQ}$), Refresh Request ($\overline{REFREQ}$), and System Busy ($\overline{BUSY}$). These conditions are:

1. System memory cycle request — memory not busy ($\overline{BUSY}$ = High)
2. System memory cycle request — memory busy ($\overline{BUSY}$ =Low)
3. Refresh cycle request — memory not busy ($\overline{BUSY}$ = High)
4. Refresh cycle request — memory busy ($\overline{BUSY}$ =Low)
5. Simultaneous system memory cycle and refresh cycle requests.

Condition 5 is actually a subset of the four previous conditions and is included for completeness.

As is implied in the five conditions, the response of the 3222 to both refresh and memory cycles is dependent on the state of the $\overline{BUSY}$ input. The $\overline{BUSY}$ signal is generated externally to the 3222 and, when low, defines the time when the memory is performing a cycle (refresh or memory access). It is important to assure that $\overline{BUSY}$ is low for the *entire* memory cycle time. Interference may occur in asynchronous memory systems if the $\overline{BUSY}$ input goes high prematurely. (An asynchronous memory system is one in which the refresh and memory cycle requests occur independent of each other.)

System Memory Cycle Request — Memory Not Busy

This section details operation of the 3222 when the memory is not busy and a request for a system memory cycle is made (See Figure A for timing sequences). The request for a memory cycle is made by the $\overline{CYREQ}$ input going low. The Start Cycle output $\overline{STARTCY}$ goes low at t_{RS} after $\overline{CYREQ}$. $\overline{STARTCY}$ is used for two purposes:

1. To set the external $\overline{BUSY}$ latch. (See Figure E.)
2. To initiate memory system timing (after appropriate delay).

The required delay time depends on system configuration and associated delay paths for both Chip Enable (2107B input signal) and system addresses.

The low going $\overline{BUSY}$ input causes the internally generated Start Cycle output to go high and the Acknowledge output $\overline{ACK}$ to go low (after t_{BK} time). The Acknowledge output confirms that the requested system memory cycle has been accepted by the 3222. Note that the cycle request input may be returned to the high state when the $\overline{BUSY}$ input goes low. However, at the designer's discretion, the cycle request line may remain low until "just prior" to $\overline{BUSY}$ returning high. (If $\overline{BUSY}$ goes high before $\overline{CYREQ}$ goes high, another memory access may inadvertently be started.)

When the memory is not busy and a cycle request has been made, the low order system address delay through the 3222 is t_{AA} nsec. When the 3222 is not busy, the low order system addresses (A_0-A_5) are gated through to the output ($\overline{O}_0$-$\overline{O}_5$) independent of any other input.

System Memory Cycle Request — Memory Busy

The major differences between a system memory cycle request when the system is busy and when it is not busy (as previously described) are:

1. The Start Cycle output $\overline{STARTCY}$ does not go low until t_{BS} after the rising edge of the $\overline{BUSY}$ input. (Even though the $\overline{CYREQ}$ input is low.)
2. Output addresses $\overline{O}_0$-$\overline{O}_5$ change at or before t_{AA} time if the previous cycle was a system cycle request and change at or before t_{BAM} if the previous cycle was a Refresh Cycle request. (Note that the longer delay is after a refresh cycle.) See Figure B for definition of terms.

Note that for a system memory cycle following a refresh cycle, the refresh on output $\overline{REFON}$ goes high at or before t_{BR} relative to $\overline{BUSY}$ going high. Since the Acknowledge output $\overline{ACK}$ can not go low until after t_{HOLD} there is no ambiguity between $\overline{REFON}$ and $\overline{ACK}$. The memory is always defined as being in a refresh cycle, system cycle or no cycle.

Refresh Cycle — Memory Not Busy

Operation of the 3222 for a refresh request with the memory not busy (see Figure C) is similar to a system cycle request under the same condition. A refresh cycle is initiated by the Refresh Request input ($\overline{REFREQ}$) going low. This low going input causes both the Start Cycle output, $\overline{STARTCY}$, and Refresh On output, $\overline{REFON}$, to go low at t and t_{RRC} (or t_{RR}) time respectively. The low going edge of $\overline{STARTCY}$ is used to set the external $\overline{BUSY}$ latch low. As in the previous two cases, the $\overline{BUSY}$ input must remain low for the entire cycle required by the memory. As in the previous two cases, the low going $\overline{BUSY}$ drives the $\overline{STARTCY}$ output high.

Refresh Cycle — Memory Busy

For this condition, it is assumed that the previous cycle was a system access cycle. Timing conditions for this operation are shown in Figure D. Here, the $\overline{STARTCY}$ input goes low t_{BS} after $\overline{BUSY}$ returns high from the previous cycle. As before, $\overline{REFON}$ goes low t_{BR} after $\overline{BUSY}$ goes high. After t_{HOLD}, relative to $\overline{STARTCY}$, $\overline{BUSY}$ again goes low and places the low order refresh addresses on the address outputs ($\overline{O}_0$-$\overline{O}_5$) after t_{BAR} time. Internal refresh timing is performed in a manner identical to that described in Refresh Cycle-Memory Not Busy section.

Simultaneous Refresh and Memory System Cycle Request

The simultaneous request for a refresh and memory system access is almost a certainty in asynchronous systems. It is, therefore, necessary to have circuitry in any refresh controller capable of resolving the attendent ambiguity with minimum additional delay. The Intel® 3222 Refresh Controller has just such a circuit. (All timing parameters specified for asynchronous operation assume that a refresh and memory system request can occur at the same time.) A latch internal to the 3222 decides which signal ($\overline{CYREQ}$ or $\overline{REFREQ}$) it will accept if both occur simultaneously, and conditions the other control circuits appropriately. If a refresh cycle was accepted, $\overline{REFON}$ will go low at the appropriate time. If a memory system access was accepted then $\overline{ACK}$ will go low at the appropriate time.

Refresh Control

The 3222 controls both burst and distributed refresh modes. The burst refresh mode requires that $\overline{REFREQ}$ be generated externally to the 3222 since refresh is completed in 64 consecutive cycles every 2ms. A system requiring distributed refresh timing, however can be controlled either by the 3222 or by external circuitry. If refresh timing is to be controlled by the 3222 the output $\overline{Q}$ is tied to the $\overline{REFREQ}$ input. Timing is controlled by an oscillator internal to the 3222. The desired refresh timing interval is determined by:

1. $\frac{t_{REF}}{r} = .63\ R_xC_x$

   Where:

   t_{REF} = the total time between refreshes (e.g. 2msec) in msec.

   r = the number of rows to be refreshed on the memory device (for the 2107B r = 64).

   R_x = external timing resistance in KΩ (3K to 10K)

   C_x = external timing capacitance in μf. (0.005μf to 0.02μf)

The 3222's oscillator stability is guaranteed to be ±2% for a given part and ±6% from part to part, both over the ranges $0°C \leq T_A \leq 75°C$ and $V_{CC} = 5.0V \pm 5\%$.

Figure F shows how the 3222 may be used to control refresh in a 2104A system.

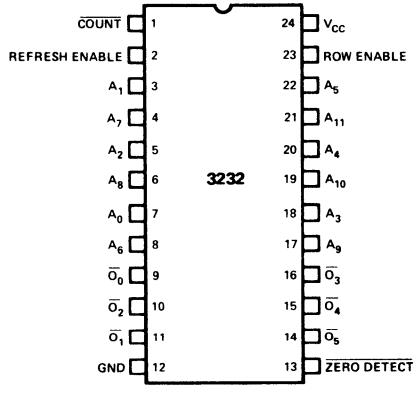
ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 4K DYNAMIC RAMs

- **Ideal For 2104A**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 24-Pin DIP**
- **Address Input to Output Delay: 9ns Maximum Driving 15pF, 25ns Maximum Driving 250pF**
- **Suitable For Either Distributed Or Burst Refresh**
- **Single Power Supply: +5 Volts ±10%**

The Intel® 3232 contains an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). It multiplexes twelve bits of system supplied address to six output address pins. The device also contains a 6 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3232 makes it especially suitable for use with high speed N-channel RAMs like the 2104A.

The 3232 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range.

PIN CONFIGURATION



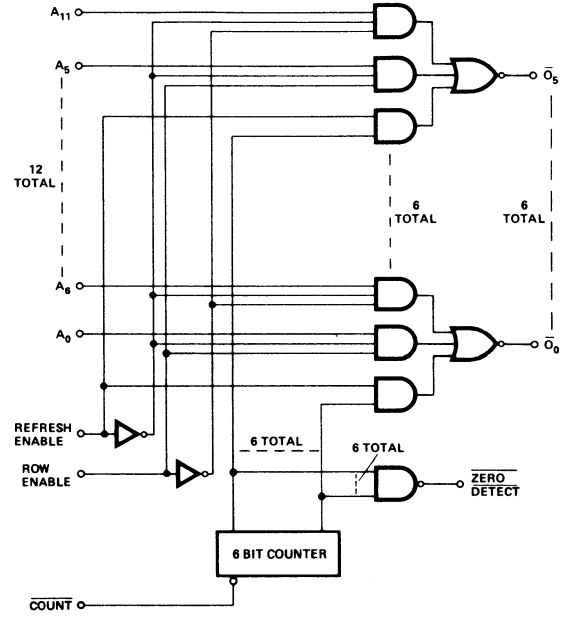
NOTE: A_0 THROUGH A_5 ARE ROW ADDRESSES.
A_6 THROUGH A_{11} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_5)
L	L	COLUMN ADDRESS (A_6 THROUGH A_{11})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES A ZERO IN THE REFRESH ADDRESS (USED IN BURST REFRESH MODE).

LOGIC DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias ..... -65° to +125°C
Storage Temperature ..... -65° to +160°C
All Input, Output, or
Supply Voltages .....-0.5V to +7 Volts
Output Currents 100mA
Power Dissipation 1W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

All Limits Apply for V_{CC} = 5.0V ±10%, T_A = 0°C to + 75°C

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	V_{IN} = 0.45V
I_R	Input Leakage Current		0	10	μA	V_{IN} = 5.5V
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	I_{OL} = 5mA
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_5$)	2.8	4.0		V	I_{OH} = −1mA
V_{OH1}	Output High Voltage ($\overline{Zero\ Detect}$)	2.4	3.3		V	I_{OH} = −1mA
I_{CC}	Power Supply Current		100	150	mA	V_{CC} = 5.5V

Note 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

A.C. Characteristics

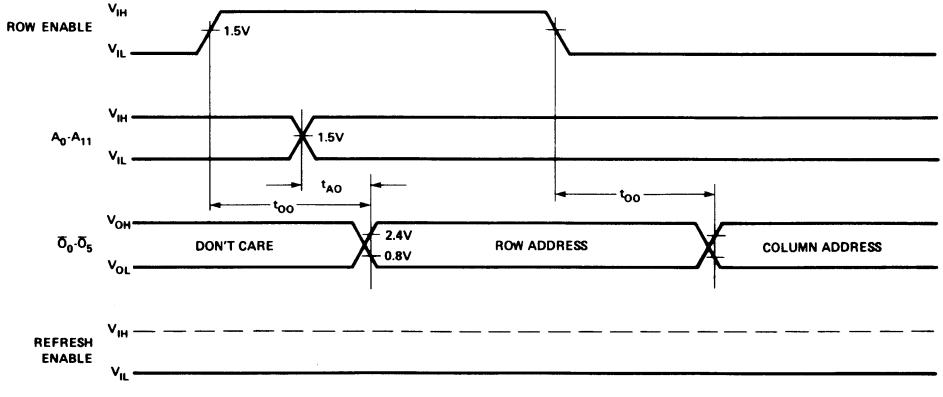
All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

SYMBOL	PARAMETER	MIN.	TYP.[1]	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low[1] [2]
t_{AO1}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	27	ns	Refresh Enable = Low[1] [2]
t_{OO1}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	27	ns	Note 1, 2
t_{EO1}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	$\overline{Count}$ to Output	15	40	60	ns	Refresh Enable = High[1] [2]
t_{CO1}	$\overline{Count}$ to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency	5			MHz	
t_{CPW}	$\overline{Count}$ Pulse Width	35			ns	
t_{CZ}	$\overline{Count}$ to $\overline{Zero\ Detect}$	15		70	ns	Note 2

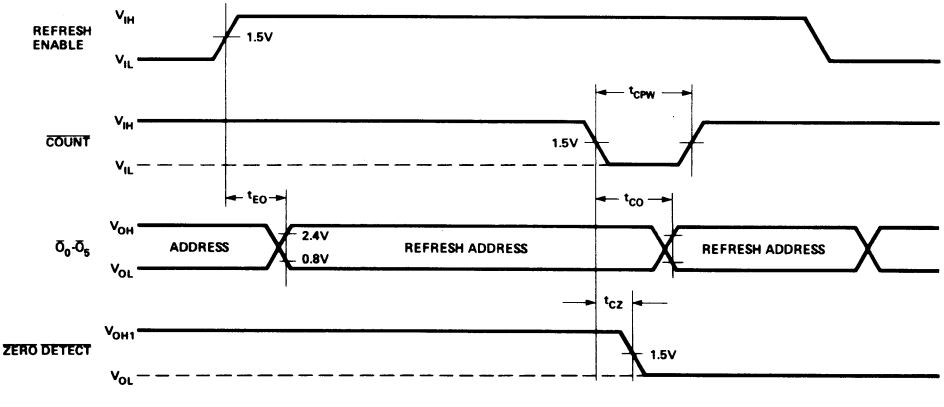
Note 1: V_{CC} = 5.0V, T_A = 25°C
2: C_L = 15pF

A.C. TIMING WAVEFORMS (Typically used with 2104A)

NORMAL CYCLE



REFRESH CYCLE



PIN NAMES AND FUNCTIONS

Pin. No.	Pin Name	Function
1	$\overline{\text{Count}}$ Input	Active low input increments internal six bit counter by one for each count pulse in.
2	Refresh Enable Input	Active high input which determines whether the 3232 is in refresh mode (H) or address enable (L).
7,3,5,18, 20,22	A_0-A_5 Inputs	Row Address inputs.
8,4,6,17, 19,21	A_6-A_{11} Inputs	Column address inputs.
9,11,10, 16,15,14	$\overline{O}_0$-$\overline{O}_5$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
12	GND	Power supply ground.
13	$\overline{\text{Zero}}$ $\overline{\text{Detect}}$ Output	Active low output which senses that all six bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
23	Row Enable Input	High input selects row, low input selects column addresses of the driven memories.
24	V_{CC}	+5V power supply input.

DEVICE OPERATION

The Intel® 3232 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter)
2. Row addresses (A_0 through A_5)
3. Column addresses (A_6 through A_{11})

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the 6 outputs of the internal 6 bit counter. At each $\overline{\text{Count}}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0$-$\overline{O}_5$) through all 64 row addresses. When the counter sequences to all zeros, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output goes low signaling the end of the refresh sequence. Due to counter decoding spikes, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output is valid only after t_{CZ} following the low going edge of $\overline{\text{Count}}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of rows in the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2104A $t_{REFRESH}$ = 2msec and n = 64, therefore one row is refreshed each 31 μsec. Following the refresh cycle at row n_x, the Count input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The Count input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All twelve system address lines are applied to the inputs of the 3232. When Refresh Enable is low and Row Enable is high, input addresses A_0-A_5 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_6-A_{11} are gated to the outputs and applied to the driven memories.

Figure 1 shows a typical connection between the 3232 and the 2104A 4K dynamic RAM. When the memory devices are driven directly by the 3232, the address applied to the memory devices is the inverse of the address at the 3232 inputs due to the inverted outputs of the 3232. This should be remembered when checking out the memory system.

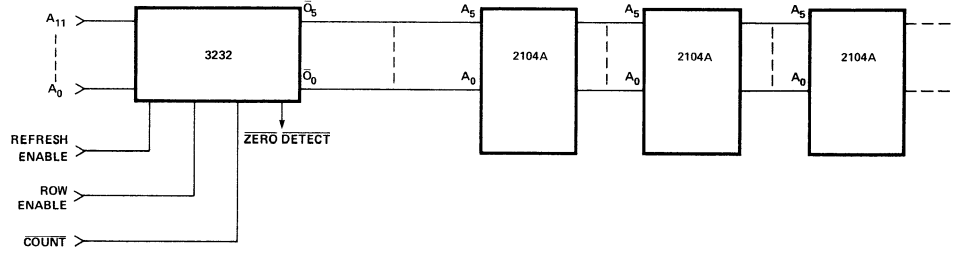


Figure 1. Typical Connection of 3232 and 2104 Memories.

3242
ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 16K DYNAMIC RAMs

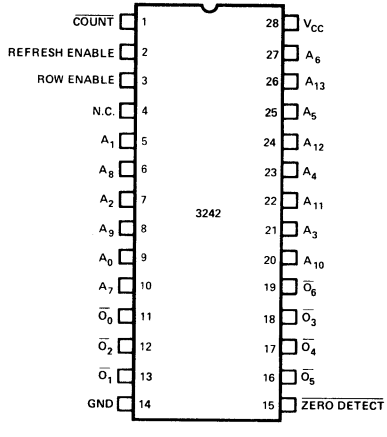
- **Ideal For 2116**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 28-Pin DIP**
- **Suitable For Either Distributed Or Burst Refresh**
- **Single Power Supply: +5 Volts ±10%**
- **Address Input to Output Delay: 9ns Driving 15 pF, 25ns Driving 250pF**

MEMORY SUPPORT

The Intel® 3242 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of 64 or 128 cycles. It multiplexes 14 bits of system supplied address to 7 output address pins. The device also contains a 7 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3242 makes it especially suitable for use with high speed N-channel RAMs like the 2116.

The 3242 operates from a single +5 volt power supply and is specified for operation over a 0 to +75° C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process and is packaged in a hermetically sealed 28 pin Type D package.

PIN CONFIGURATION



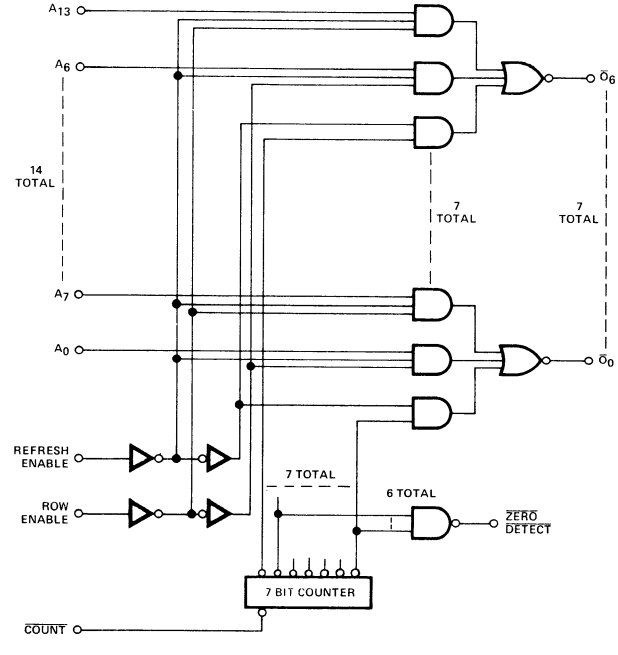
NOTE: A_0 THROUGH A_6 ARE ROW ADDRESSES.
A_7 THROUGH A_{13} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_6)
L	L	COLUMN ADDRESS (A_7 THROUGH A_{13})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES ZERO IN THE FIRST 6 SIGNIFICANT REFRESH COUNTER BITS (USED IN BURST REFRESH MODE)

LOGIC DIAGRAM



A.C. Characteristics

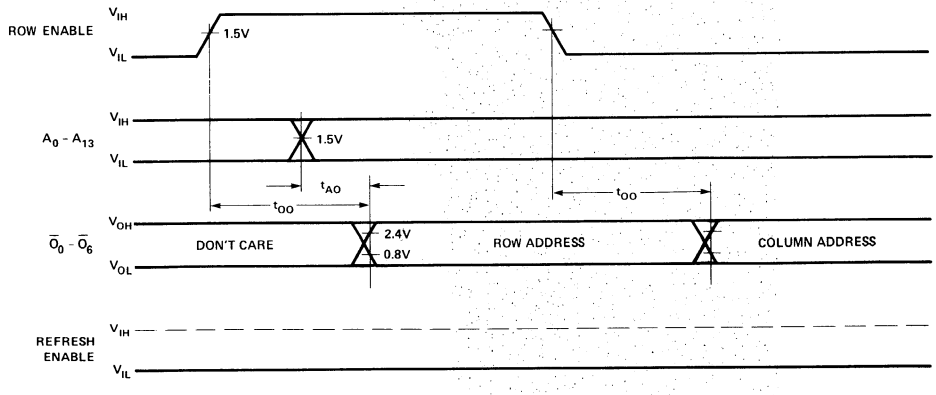
All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low(2)(3)
t_{AO1}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	27	ns	Refresh Enable = Low(2)(3)
t_{OO1}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	27	ns	Notes 2, 3
t_{EO1}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	$\overline{Count}$ to Output	15	40	60	ns	Refresh Enable = High(2)(3)
t_{CO1}	$\overline{Count}$ to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency			5	MHz	
t_{CPW}	$\overline{Count}$ Pulse Width	35			ns	
t_{CZ}	$\overline{Count}$ to $\overline{Zero\ Detect}$	15		70	ns	Note 3

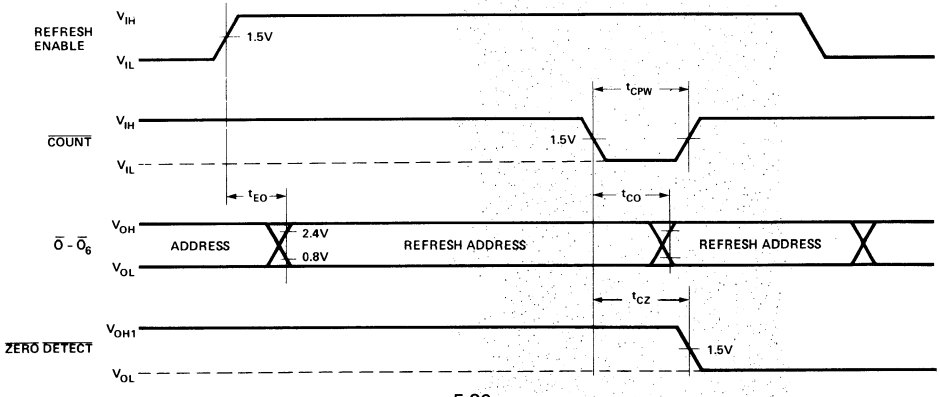
Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. T_A = 25°C, V_{CC} = 5.0V.
3. C_L = 15 pF.

A.C. TIMING WAVEFORMS (Typically used with 2116)

NORMAL CYCLE



REFRESH CYCLE



Absolute Maximum Ratings*

Temperature Under Bias ..... -10° to +85°C
Storage Temperature ..... -65° to +150°C
All Input, Output, or
Supply Voltages .....-0.5V to +7 Volts
Output Currents 100mA
Power Dissipation 1W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

All Limits Apply for V_{CC} = 5.0V ±10%, T_A = 0°C to + 75°C

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. (1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	V_{IN} = 0.45V, Note 2
I_R	Input Leakage Current		0.01	10	μA	V_{IN} = 5.5V
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	I_{OL} = 8mA
V_{OH}	Output High Voltage ($\overline{O_0}$-$\overline{O_6}$)	3.0	4.0		V	I_{OH} = −1mA
V_{OH1}	Output High Voltage ($\overline{\text{Zero Detect}}$)	2.4	3.3		V	I_{OH} = −1mA
I_{CC}	Power Supply Current		105	165	mA	V_{CC} = 5.5V

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Inputs are high impedance, TTL compatible, and suitable for bus operation.

MEMORY SUPPORT

PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{\text{Count}}$ Input*	Active low input increments internal 7-bit counter by one for each count pulse in.
2	Refresh Enable Input*	Active high input which determines whether the 3242 is in refresh mode (H) or address enable (L).
9,5,7,21, 23,25,27	A_0–A_6 Inputs*	Row address inputs.
10,6,8,20, 22,24,26	A_7–A_{13} Inputs*	Column address inputs.
11,13,12, 18,17,16, 19	$\overline{O}_0$–$\overline{O}_6$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
14	GND	Power supply ground.
15	$\overline{\text{Zero}}$ $\overline{\text{Detect}}$ Output	Active low output which senses that the six low order bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
3	Row Enable Input*	High input selects row, low input selects column addresses of the driven memories.
28	V_{CC}	+5V power supply input.

*The inputs are high impedance, TTL compatible, and suitable for bus operation.

DEVICE OPERATION

The Intel® 3242 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing.
2. Address Counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter).
2. Row addresses (A_0 through A_6).
3. Column addresses (A_7 through A_{13}).

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the seven outputs of the internal 7-bit counter. At each $\overline{\text{Count}}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0$–$\overline{O}_6$) through 128 row addresses. When the first six significant bits of the counter sequence to all zeros, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output goes low, signaling the end of the refresh sequence. Due to counter decoding spikes, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output is valid only after t_{CZ} following the low-going edge of $\overline{\text{Count}}$. The $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output used in this manner signals the completion of 64 refresh cycles. To use the 128-cycle burst refresh mode, an external flip-flop must be driven by the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of refresh cycles required for the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2116 $t_{REFRESH}$ = 2 msec and n = 128 or 64, therefore, one row is refreshed each 15.5 or 31 μsec, respectively. Following the refresh cycle at row n_x, the $\overline{\text{Count}}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The $\overline{\text{Count}}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All 14 system address lines are applied to the inputs of the 3242. When Refresh Enable is low and Row Enable is high, input addresses A_0–A_6 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_7–A_{13} are gated to the outputs and applied to the driven memories.

Figure 1 shows a typical connection between the 3242 and the 2116 16K dynamic RAM. When the memory devices are driven directly by the 3242, the address applied to the memory devices is the inverse of the address at the 3242 inputs due to the inverted outputs of the 3242. This should be remembered when checking out the memory system.

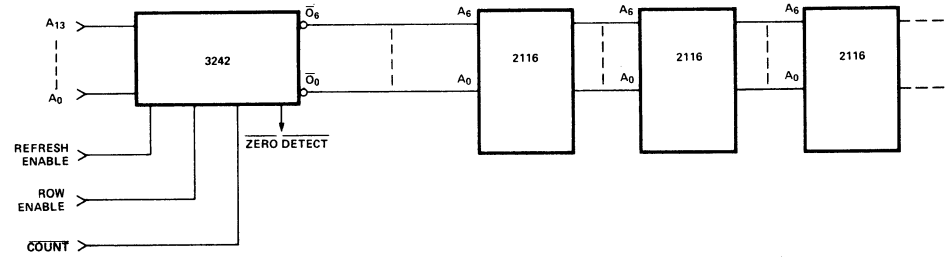


Figure 1. Typical Connection of 3242 and 2116 Memories.

QUAD TTL-TO-MOS DRIVER

For 4K N-Channel MOS RAMs

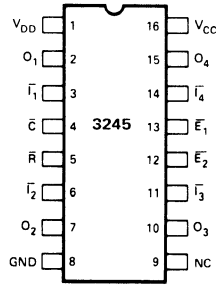
- **Fully Compatible With 4K RAMs Without Requiring Extra Supply Or External Devices**
- **High Speed, 32 nsec Max. — Delay + Transition Time**
- **Low Power — 75mW Typical Per Channel**
- **High Density — Four Drivers in One Package**
- **TTL & DTL Compatible Inputs**
- **CerDIP Package — 16 Pin DIP**
- **Only +5 and +12 Volt Supplies Required**

The Intel® 3245 is a Quad Bipolar-to-MOS driver which accepts TTL and DTL input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107B. The circuit operates from two power supplies which are 5 and 12 volts. Input and output clamp diodes minimize line reflections.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system designs. The internal gating structure of the 3245 eliminates gating delays and minimizes package count.

The 3245 is fabricated by means of Intel's highly reliable Schottky bipolar process and is specified for operation over a 0 to +75°C ambient temperature range.

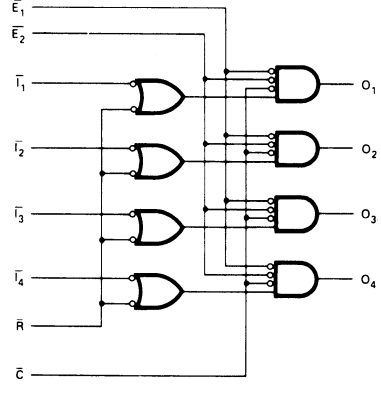
PIN CONFIGURATION



PIN NAMES

$\overline{I}_1$-$\overline{I}_4$	SELECT INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{E}_1$, $\overline{E}_2$	ENABLE INPUTS	V_{CC}	+5V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT	NC	NOT CONNECTED

LOGIC DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 85°C
Storage Temperature. . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 to +7V
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
All Input Voltages . . . . . -1.0 to V_{DD}
Outputs for Clock Driver . . . . . -1.0 to V_{DD} +1V
Power Dissipation at 25°C 2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$		-0.25	mA	V_F = 0.45V
I_{FE}	Input Load Current, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$		-1.0	mA	V_F = 0.45V
I_{RD}	Data Input Leakage Current		10	μA	V_R = 5.0V
I_{RE}	Enable Input Leakage Current		40	μA	V_R = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5mA, V_{IH} = 2V
		-1.0		V	I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.50		V	I_{OH} = -1mA, V_{IL} = 0.8V
			V_{DD}+1.0	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs		0.8	V	
V_{IH}	Input High Voltage, All Inputs	2		V	

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions — Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	23	30	mA	High	
I_{DD}	Current from V_{DD}	19	26	mA		
P_{D1}	Power Dissipation	365	485	mW		
	Power Per Channel	91	121	mW		V_{CC} = 5.25V
I_{CC}	Current from V_{CC}	29	39	mA	Low	V_{DD} = 12.6V
I_{DD}	Current from V_{DD}	12	15	mA		
P_{D2}	Power Dissipation	300	388	mW		
	Power Per Channel	75	97	mW		

A.C. Characteristics $T_A = 0°$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	5	11		ns	$R_{SERIES} = 0$
t_{DR}	Delay Plus Rise Time		20	32	ns	$R_{SERIES} = 0$
t_{+-}	Input to Output Delay	3	7		ns	$R_{SERIES} = 0$
t_{DF}	Delay Plus Fall Time		18	32	ns	$R_{SERIES} = 0$
t_T	Output Transition Time	10	17	25	ns	$R_{SERIES} = 20\Omega$
t_{DR}	Delay Plus Rise Time		27	38	ns	$R_{SERIES} = 20\Omega$
t_{DF}	Delay Plus Fall Time		25	38	ns	$R_{SERIES} = 20\Omega$

NOTES:
1. $C_L = 150pF$
2. $C_L = 200pF$
3. $C_L = 250pF$

These values represent a range of total stray plus clock capacitance for nine 4K RAMs.

4. Typical values are measured at 25°C.

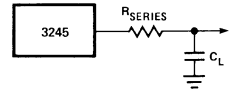
Capacitance* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$	5	8	pF
C_{IN}	Input Capacitance, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$	8	12	pF

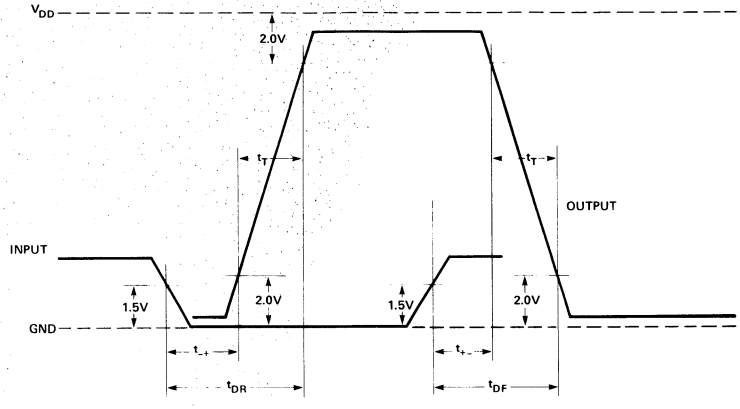
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 3.0V
Input Pulse Rise and Fall Times: 5 ns between 1 volt and 2 volts
Measurement Points: See Waveforms

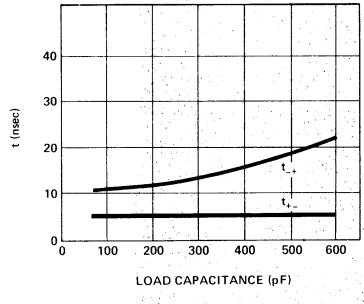


Waveforms

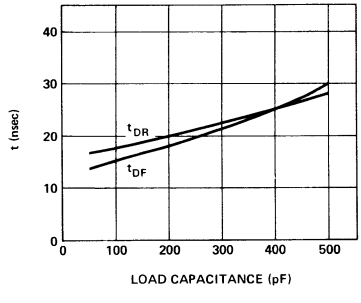


Typical Characteristics

INPUT TO OUTPUT DELAY VS. LOAD CAPACITANCE

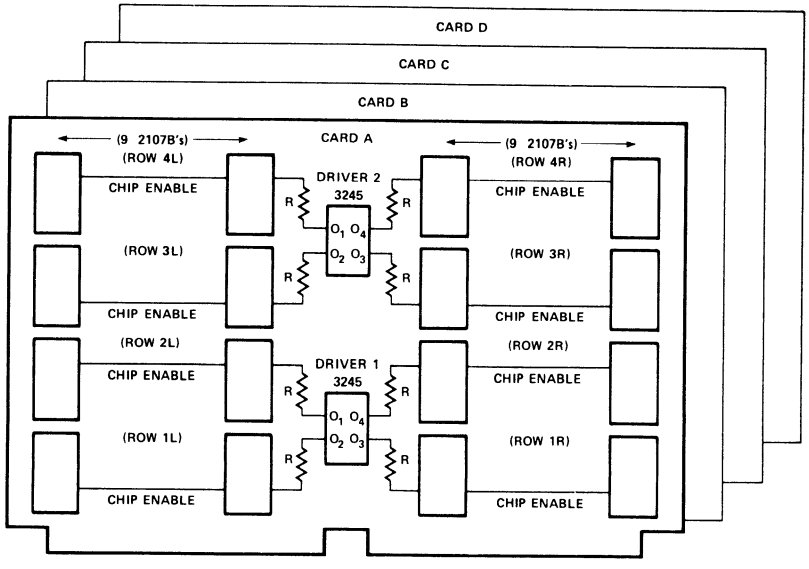


DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE



Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 3245 quad high voltage driver for the chip enable inputs. A single 3245 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



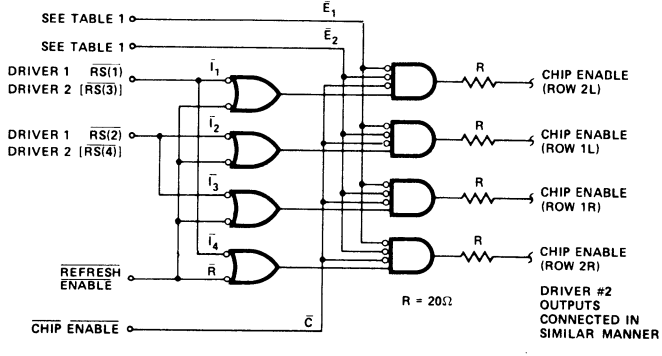
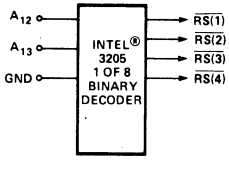
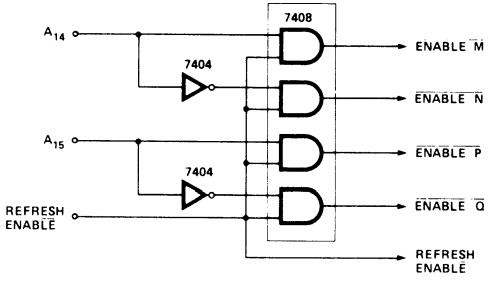


TABLE 1.

CARD	INPUTS $\bar{E}_1$	INPUTS $\bar{E}_2$
A	ENABLE M	ENABLE P
B	ENABLE M	ENABLE Q
C	ENABLE N	ENABLE P
D	ENABLE N	ENABLE Q





5235, 5235-1
QUAD TTL-TO-MOS DRIVER
For 4K N-Channel MOS RAMs

- **CMOS Technology for Very Low Power: Suitable for Battery Backup**
- **High Density: Four Drivers in One Package**
- **Internal Gating Structure Minimizes Package Count**
- **TTL & DTL Compatible Inputs**
- **CerDIP Package: 16 Pin DIP**
- **Only One Power Supply Required, +12V (±10%)**

MEMORY SUPPORT

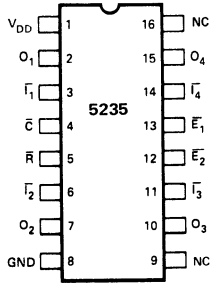
The Intel® 5235 and 5235-1 are Low Power Quad TTL-to-MOS drivers which accept TTL and DTL input levels. They provide high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107A or 2107B. The circuit operates from a single 12 volt power supply.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system design.

The 5235-1 is a selection of the 5235 and is guaranteed for 95ns maximum delay plus transition time while driving a 250pF load.

The Intel ion-implanted, silicon gate Complementary MOS (CMOS) process allows the design and production of very low power drivers.

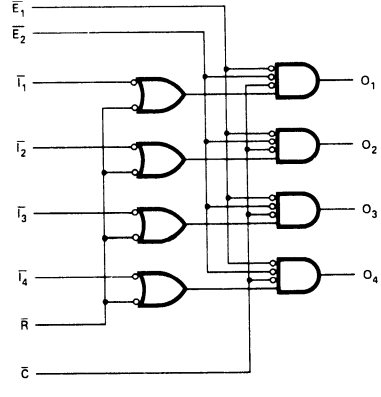
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	SELECT INPUTS	$\overline{C}$	CLOCK CONTROL INPUT
$\overline{E_1}$, $\overline{E_2}$	ENABLE INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
		NC	NOT CONNECTED

LOGIC DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
All Input Voltages . . . . . -0.5 to (V_{DD}+0.5V)
Outputs for Clock Driver . . . . . -0.5 to (V_{DD}+0.5V)
Power Dissipation at 25°C 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to 70°C, V_{DD} = 12V ±10%.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_{LI}\|$	Input Load Current		0.1	10	µA	V_{IN} = ≤0.4V or ≥2.4V
V_{OL}	Output Low Voltage		0.15	0.4	V	I_{OL} = 5mA
		-1.0	-0.15		V	I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.4	V_{DD}-0.15		V	I_{OH} = -5mA
			V_{DD}+0.15	V_{DD}+0.5	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs			0.8	V	
V_{IH}	Input High Voltage, All Inputs	2.0			V	
I_{DD0}	Supply Current		1.0	2.0	mA	f = 0MHz; V_{DD}=13.2V, V_{IN}≤0.4V or V_{IN}≥2.4V, C_L = 0pf.
I_{DD1}	Supply Current		12	20	mA	f = 1MHz (See Figure 1); V_{DD}=13.2V, V_{IN}≤0.4V or V_{IN}≥2.4V, C_L = 0pf.

Note 1: Typical values are at 25°C and nominal voltage.

Typical Characteristics

Figure 1.
POWER SUPPLY CURRENT VS. FREQUENCY (ALL 4 CHANNELS SWITCHING)

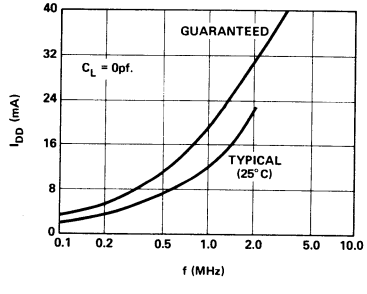


Figure 2.
DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE

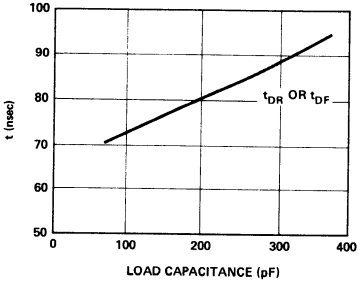


Figure 3.
DELAY PLUS TRANSITION TIME VS. INPUT VOLTAGE

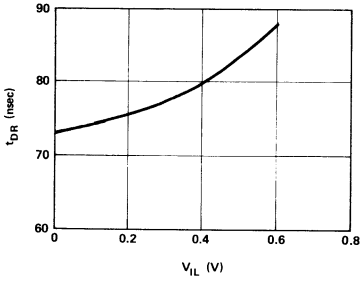
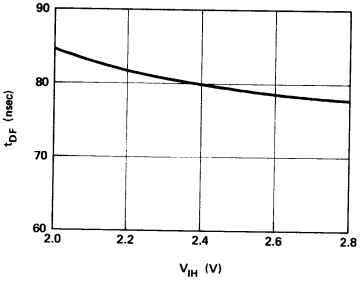


Figure 4.
DELAY PLUS TRANSITION TIME VS. INPUT VOLTAGE



A.C. Characteristics $T_A = 0°$ to $70°C$, $V_{DD} = 12V \pm 10\%$.

Symbol	Parameter	5235-1			5235			Unit
		Min.[1]	Typ.[2,4]	Max.[3]	Min.[1]	Typ.[2,4]	Max.[3]	
t_{-+}	Input to Output Delay	20	55		20	70		ns
t_{DR}	Delay Plus Rise Time		75	95		95	125	ns
t_{+-}	Input to Output Delay	20	55		20	70		ns
t_{DF}	Delay Plus Fall Time		75	95		95	125	ns
t_T	Transition Time	10	20	40	10	25	40	ns

NOTES: 1. $C_L = 150pF$ ┐
2. $C_L = 200pF$ ├ These values represent a range of total stray plus clock capacitance for nine 4K RAMs.
3. $C_L = 250pF$ ┘
4. Typical values are measured at 25°C, and nominal voltage.

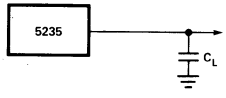
Capacitance* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance	8	14	pF

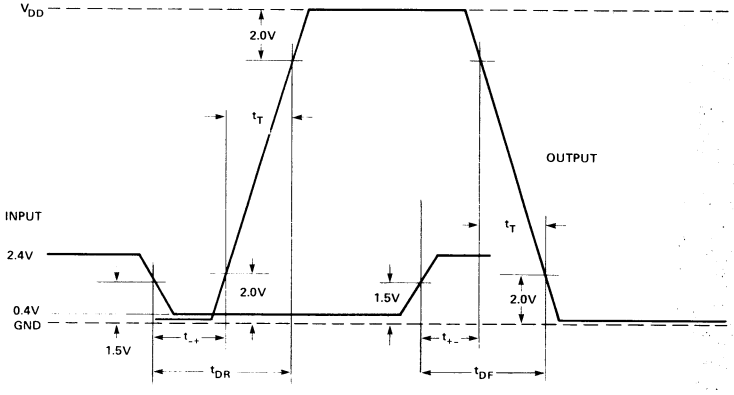
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 2.0V
Input Pulse Rise and Fall Times: 5ns between 0.9 volt and 1.9 volts
Measurement Points: See Waveforms

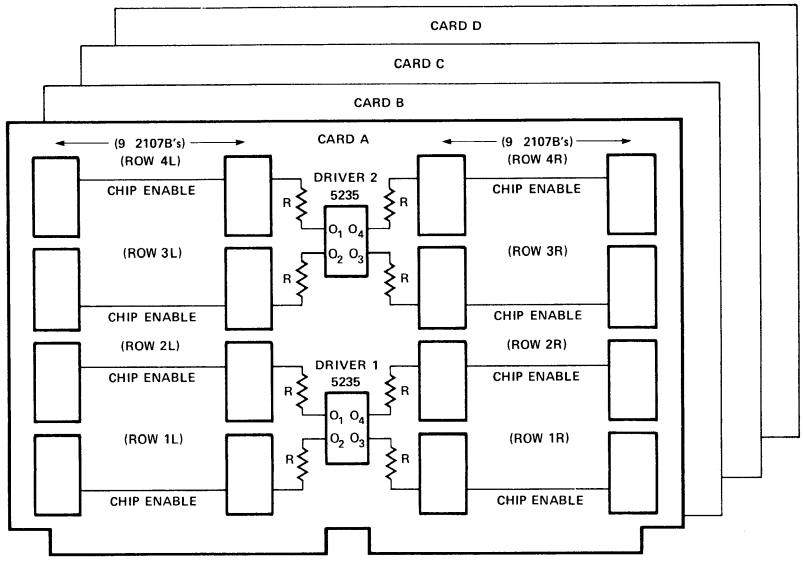


Waveforms



Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 5235 quad high voltage driver for the chip enable inputs. A single 5235 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



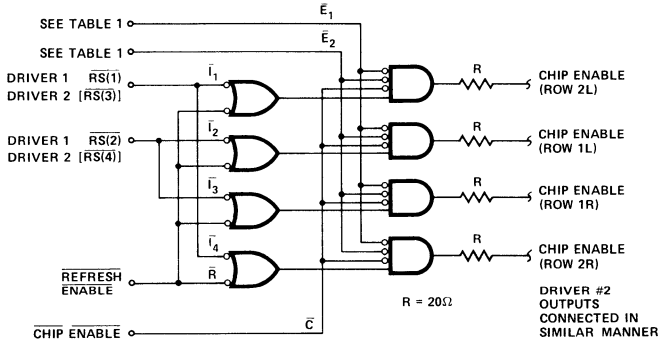
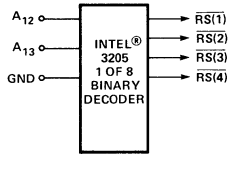
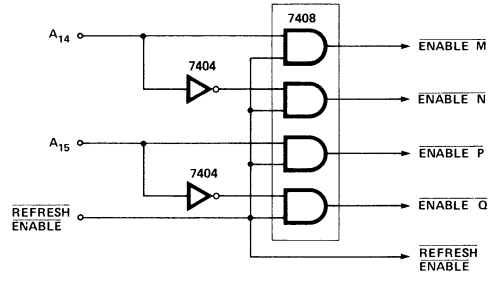


TABLE 1.

CARD	INPUTS $\bar{E}_1$	INPUTS $\bar{E}_2$
A	ENABLE M	ENABLE P
B	ENABLE M	ENABLE Q
C	ENABLE N	ENABLE P
D	ENABLE N	ENABLE Q





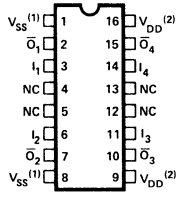
QUAD CCD CLOCK DRIVER

- **Internal Circuitry Minimizes CCD Clock Cross-Coupling Voltage Transients**
- **Drives Four 2416s**
- **Low Standby Power Dissipation: 24mW Typically**
- **TTL Inputs**
- **Single +12V Supply**
- **Standard 16 Pin Dual In-Line Package**

The 5244 is a quad clock driver which provides high capacitive drive suitable for driving charge coupled memories. The 5244 features very low D.C. power dissipation from a single 12V supply with output characteristics directly compatible with the 2416 clock input requirements. Internal circuitry controls the cross-coupled voltage transients between the clock phases generated by the 2416 and limits the transition time so that excessively fast transitions do not occur on the clock line.

The 5244 is fabricated using an advanced ion-implanted, silicon gate, CMOS process.

PIN CONFIGURATION

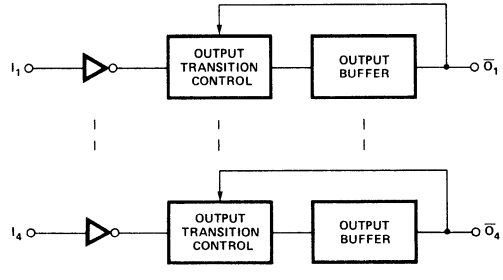


NOTES: 1. BOTH PIN 1 AND 8 MUST BE CONNECTED TO V_{SS}.
2. BOTH PIN 9 AND 16 MUST BE CONNECTED TO V_{DD}.

PIN NAMES

$I_1 - I_4$	TTL INPUT
$\overline{O}_1 - \overline{O}_4$	DRIVER OUTPUT
V_{DD}	+12V POWER SUPPLY
NC	NOT CONNECTED
V_{SS}	GROUND

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to +150°C
Supply Voltage with Respect to V_{SS}	-0.5 to +14V
All Input Voltages	-0.5 to (V_{DD}+1V)
Outputs	-1V to (V_{DD} +1)
Power Dissipation	1.35W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{SS} = 0V

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{IL}	Low Level Input Current	-10	±0.1	10	μA	$V_{IN} \leqslant V_{IL}$
I_{IH}	High Level Input Current	-10	±0.1	10	μA	$V_{IN} \geqslant V_{IH}$
V_{IL}	Input Low Voltage		+1.2	+0.85	V	
V_{IH}	Input High Voltage	+2.0	+1.5	V_{DD}+1.0	V	
V_{OL}	Output Low Voltage	0	0.03	+0.1	V	I_{OL} = 5mA
V_{OH}	Output High Voltage	V_{DD}-0.1	V_{DD}-.03	V_{DD}	V	I_{OH} = -5mA
I_{DD0}	Standby Current		2.0	4.0	mA	$V_{IN} \geqslant V_{IH}$, $V_{IN} \leqslant V_{IL}$, f = 0 MHz
I_{DD1}	Operating Current		75	105[3]	mA	$V_{IN} \geqslant V_{IH}$ or $V_{IN} \leqslant V_{IL}$, f=0.67MHz [2]

A.C. Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{SS} = 0V, Note 2

Symbol	Parameter	Limits Driving 4 2416's Min.	Typ.	Max.	Units
V_{OLT}	Transient Cross-Coupled Output Low Voltage	-0.8	±0.5	+0.8	V
V_{OHT}	Transient Cross-Coupled Output High Voltage	V_{DD}-0.8	V_{DD}±0.5	V_{DD}+0.8	V
t_{PWT}	Transient Cross-Coupled Output Pulse Width			Note 1	ns
Δt_D	Differential Delay of t_{DLH} and t_{DHL} for Drivers in the Same Package			15	ns
t_{DLH1}	Input Low to Output High Delay Time, ϕ_1 or ϕ_3	30	50		ns
t_{DHL1}	Input High to Output Low Delay Time, ϕ_1 or ϕ_3	30	50		ns
t_{TLH1}	Output Rise Time, ϕ_1 or ϕ_3	30	50	75	ns
t_{THL1}	Output Fall Time, ϕ_1 or ϕ_3	30	50	75	ns
t_{PLH1}	Input to Output Delay Plus Rise Time, ϕ_1 or ϕ_3		100	160	ns
t_{PHL1}	Input to Output Delay Plus Fall Time, ϕ_1 or ϕ_3		100	150	ns
t_{DLH2}	Input Low to Output High Delay Time, ϕ_2 or ϕ_4	30	55		ns
t_{DHL2}	Input High to Output Low Delay Time, ϕ_2 or ϕ_4	30	55		ns
t_{TLH2}	Output Rise Time, ϕ_2 or ϕ_4	30	55	85	ns
t_{THL2}	Output Fall Time, ϕ_2 or ϕ_4	30	55	90	ns
t_{PLH2}	Input to Output Delay Plus Rise Time, ϕ_2 or ϕ_4		110	175	ns
t_{PHL2}	Input to Output Delay Plus Fall Time, ϕ_2 or ϕ_4		110	170	ns

Notes: 1. The maximum t_{PWT} is the sum of the output transition time (rise or fall) plus 5ns.
2. Output Load = four 2416 clock inputs or equivalent per Figure 2.
3. $I_{DD1} = 4.0\ mA + \frac{75.4\ mA}{t_{\phi/2}\ (in\ \mu s)}$

CAPACITANCE* $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	8	14	pf	f = 1 MHz, V_{bias} = 2V, V_{DD} = 0V

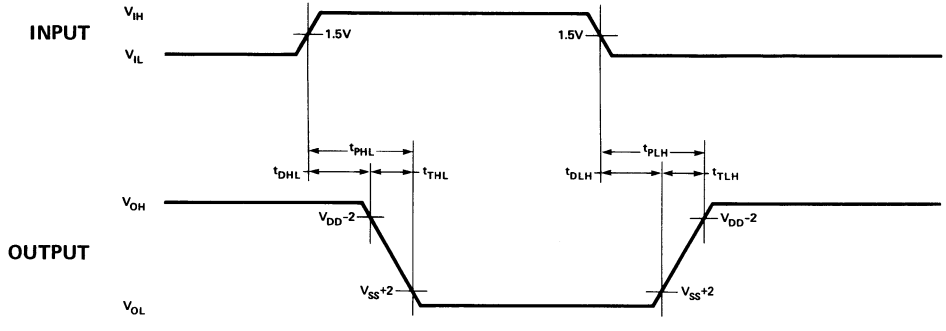
*This parameter is periodically sampled and is not 100% tested.

A.C. Test Conditions

1. TTL Input Levels = 0.4V to 2.4V.
2. Input Rise and Fall Times = 5 ns between 0.9V and 1.9V.
3. Output Load = Four 2416 clock inputs or equivalent per Figure 2.
4. Cross Coupled Voltage Pulse Width measured at ±0.4V and V_{DD} ±0.4V.

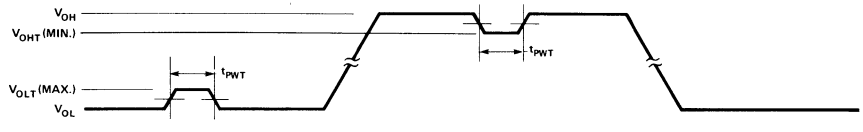
Waveforms

A. INPUT TO OUTPUT DELAY

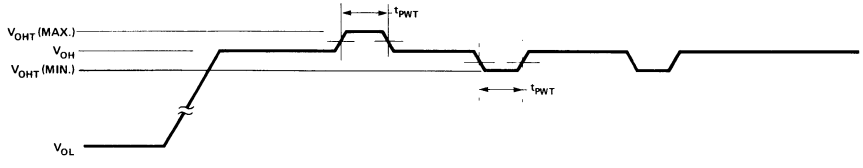


B. 5244 OUTPUT CROSS-COUPLED VOLTAGE (DRIVING FOUR 2416'S)

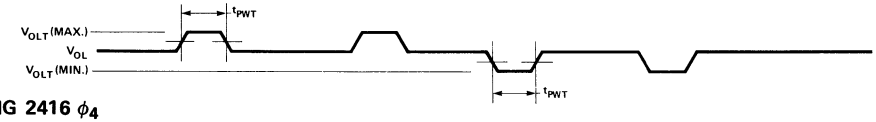
5244 OUTPUT DRIVING 2416 ϕ_1



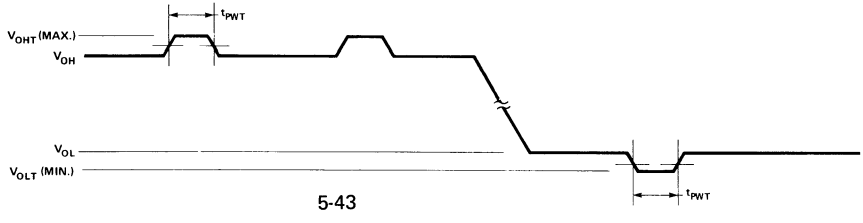
5244 OUTPUT DRIVING 2416 ϕ_2



5244 OUTPUT DRIVING 2416 ϕ_3

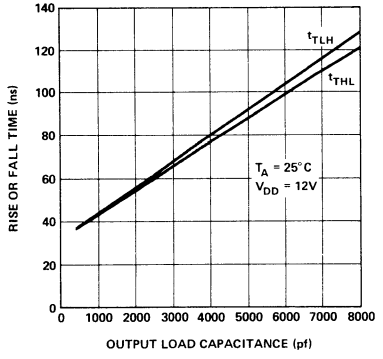


5244 OUTPUT DRIVING 2416 ϕ_4

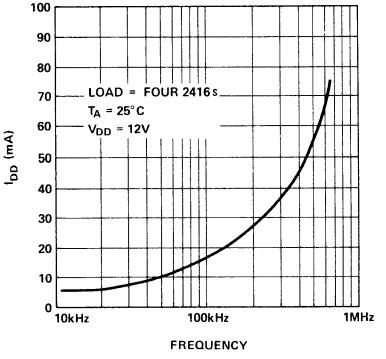


Typical Characteristics

OUTPUT RISE AND FALL TIME VS. CAPACITANCE



I_{DD} VS. FREQUENCY



MEMORY SUPPORT

Application Information

The 5244 is a TTL to MOS level converter designed to drive very high capacitive loads with no required additional external components. Its primary application is to drive the clock phase inputs of the Intel ® 2416, a 16,384 word x 1 bit charge coupled device.

DRIVING THE 2416

The 5244 is designed to drive the clock phase inputs of four 2416s and meet or exceed the electrical specifications of these inputs. The 2416 clock specifications of special interest to the system designs are:

1. Clock transition time.
2. Clock to clock voltage coupling.

Clock Transition Control

The 5244 will meet the min/max clock transition time requirement of the 2416 when driving four 2416s. However, when driving less than four 2416s an external capacitor (C_{ext}) must be added to assure that the minimum clock transition time (30ns) is adhered to. The maximum clock transition time for the 5244 will not be exceeded if C_{ext} is chosen according to the recommendations in Figure 1.

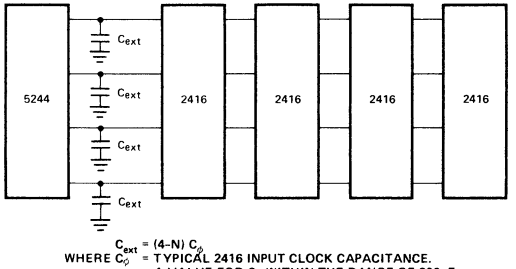


Figure 1. External Loading Requirements When Driving Fewer Than Four 2416s.

Clock Skews

The differential delay of t_{DLH} or t_{DHL} for driver elements in the same package is specified to be Δt_D (15 ns max.). This provides assurance to the system designer that the maximum skew introduced by a 5244 driver package will be limited to Δt_D. As an example, if the fastest t_{DLH} (or t_{DHL}) occurs for I_1 to $\overline{O}_1$ and this is measured to be 45 ns, the output delays for I_2 to $\overline{O}_2$, I_3 to $\overline{O}_3$ or I_4 to $\overline{O}_4$ will be no greater than 60 ns. This should be taken into consideration when designing the TTL source of the four phases required for 2416 operation. To minimize system skew, the four phases associated with any given group of 2416s should be provided from the same 5244 package.

Clock to Clock Voltage Coupling

The equivalent circuit of the 2416 clock phase inputs is shown in Figure 2. The magnitude and duration of the cross-coupling are graphically presented in Waveform B and specified in the A.C. Characteristics. Figure 3, on the next page, shows the noise margin between these specifications and the 2416 input requirements.

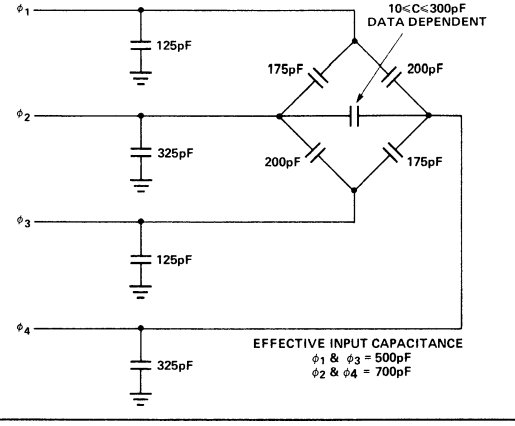


Figure 2. 2416 Equivalent Capacitance Circuit. (Maximum values shown.)

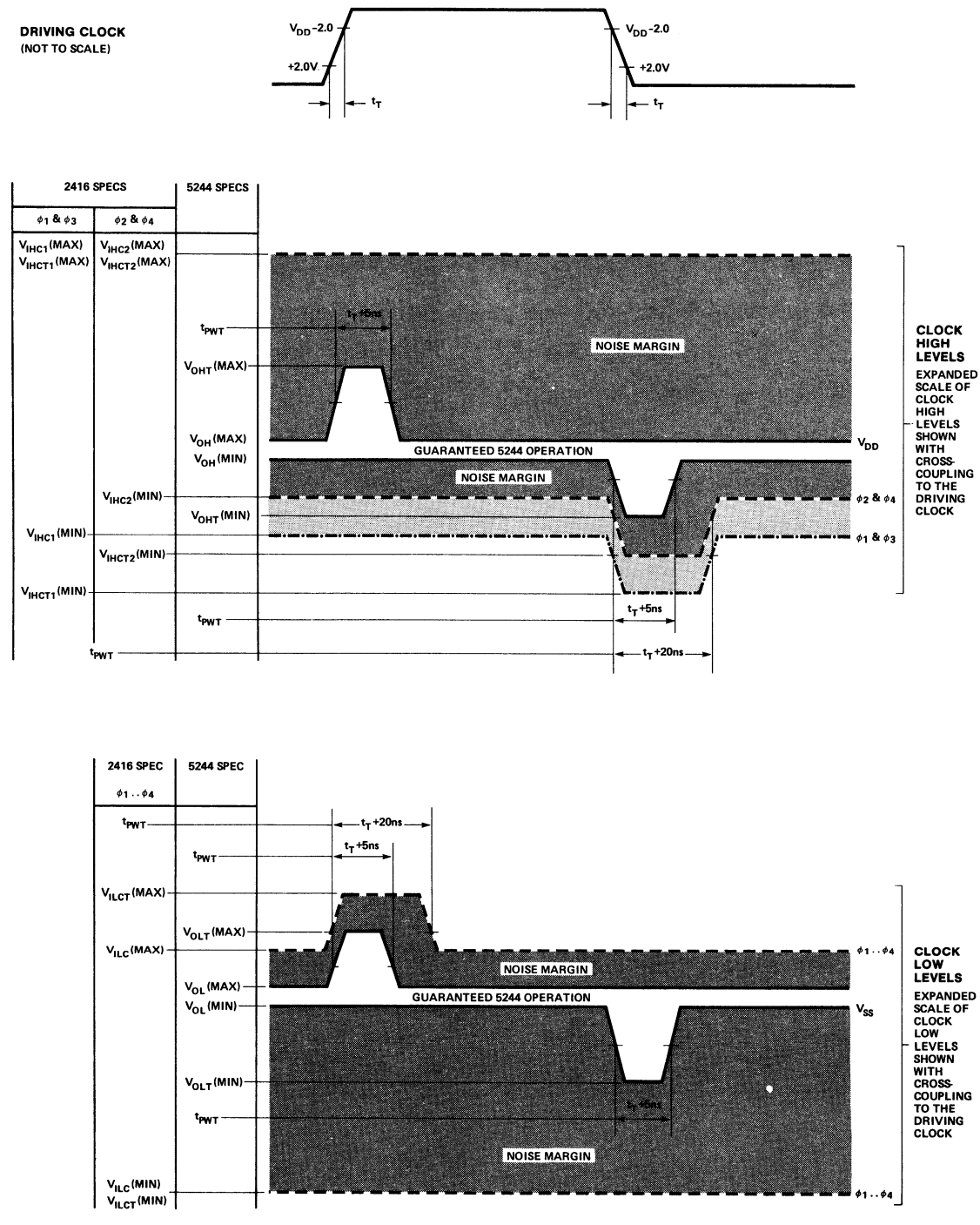
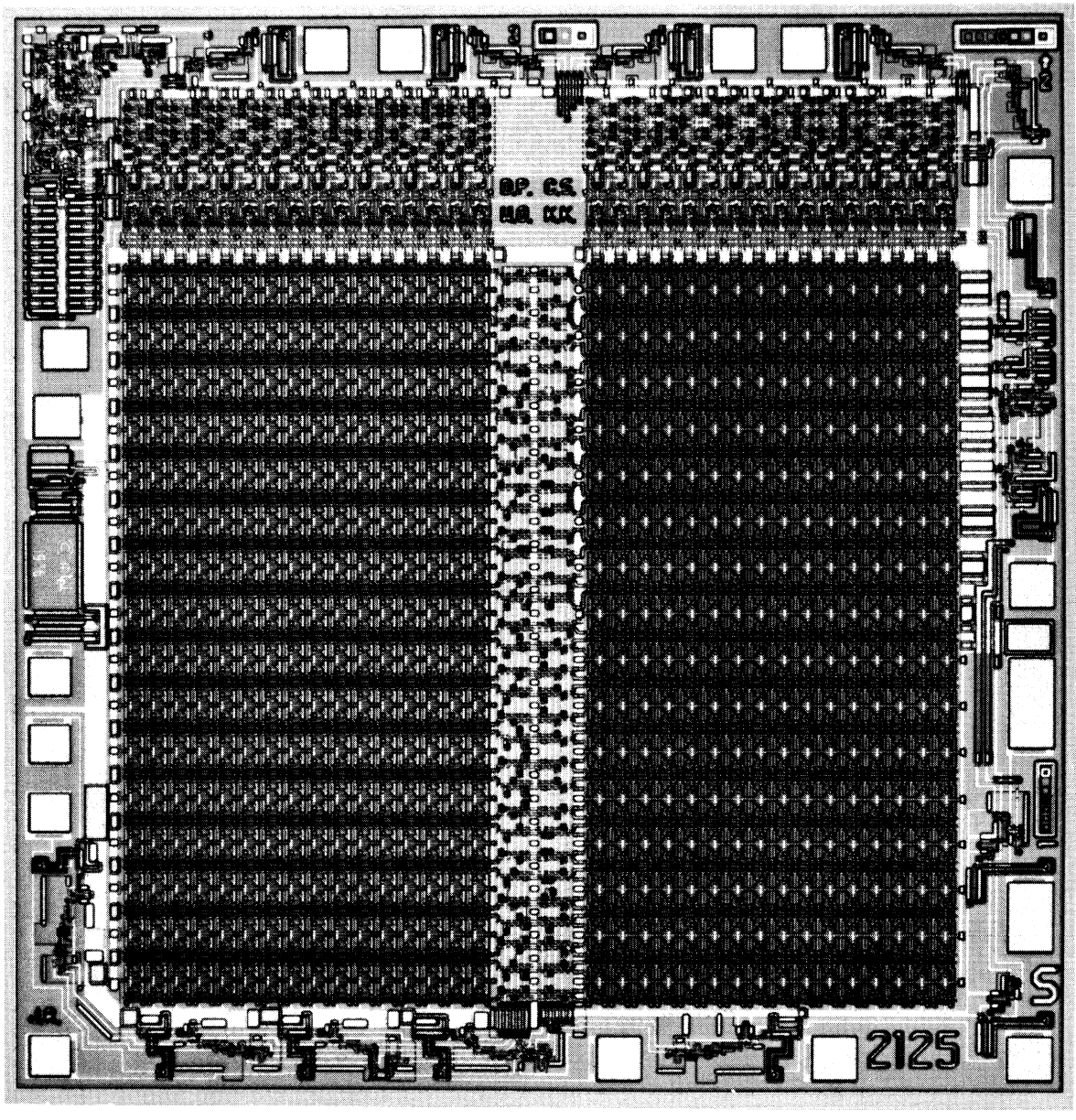
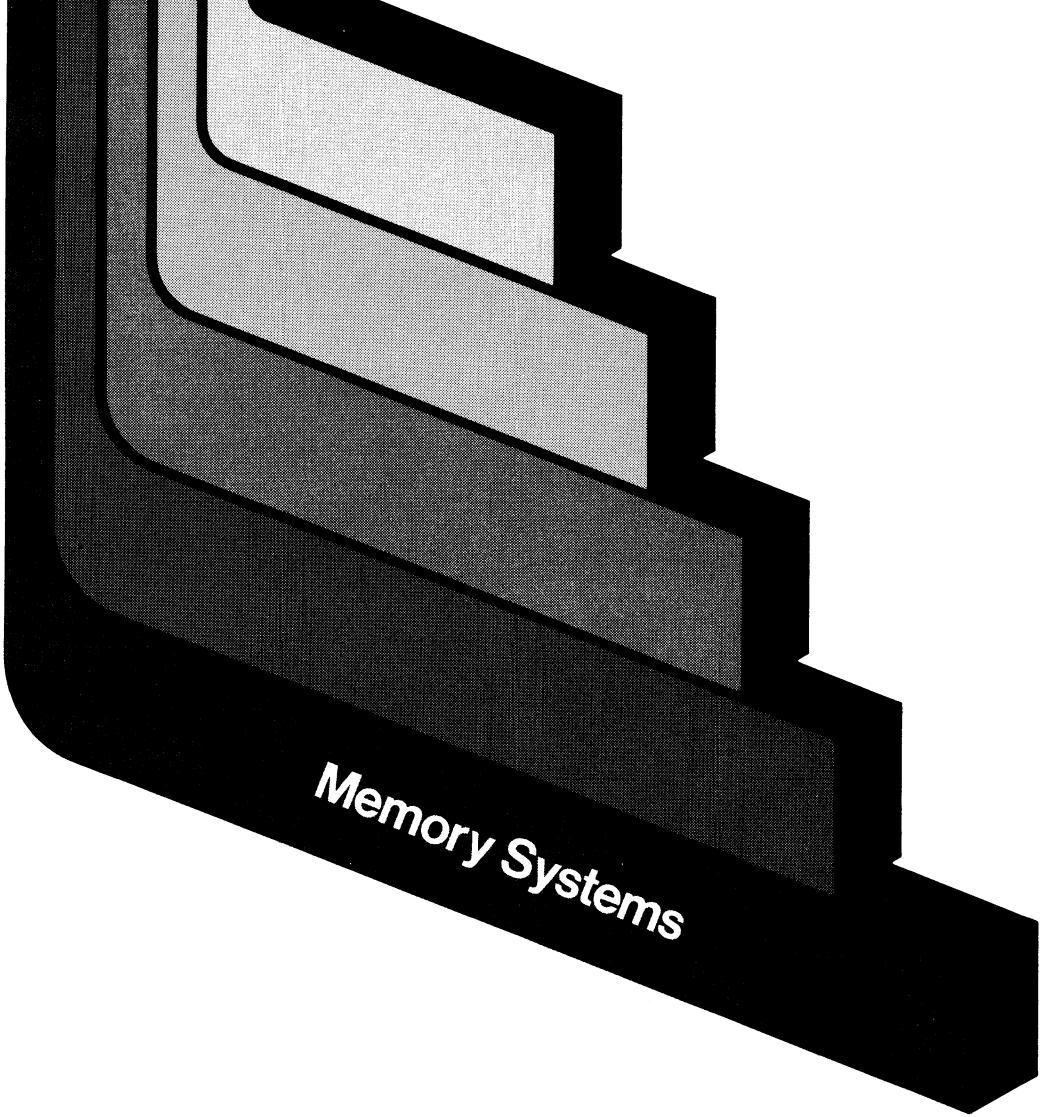


Figure 3. Noise Margins Between 5244 Output Specs and 2416 ϕ_1 . . . ϕ_4 Input Requirements.

2125A 1K, 45ns STATIC RAM




Memory Systems

MEMORY SYSTEMS

INTRODUCTION

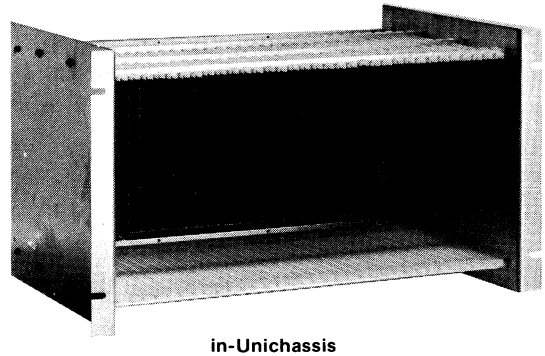
Intel Memory Systems offers standard and custom memory systems ranging from single board assemblies to multimegabyte systems. Advanced 4K, 8K and 16K RAMs and 16K CCD serial memory components are utilized for highest performance and lowest cost.

TABLE OF CONTENTS

in-26A Series
GENERAL PURPOSE
RANDOM ACCESS MEMORY SYSTEM

CAPACITY: To 4K x 10 Per Card
To 32K x 10, 16K x 20, 8K x 40 Per 7" Minichassis, Including Power
To 128K x 10 Through 16K x 80 Per 10-1/2" Unichassis

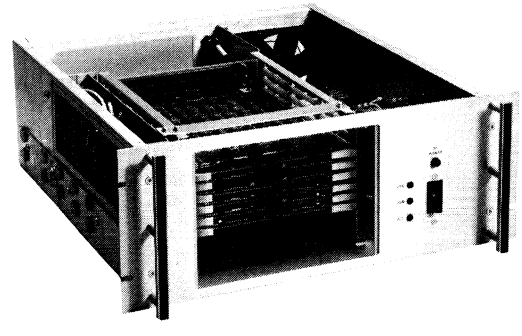
The in-26A is an extremely easy memory system to use. The in-26A is a static memory system designed to meet the high reliability and low cost requirements of random access buffer storage applications. Featuring a complete memory system on a single PC board, this memory board has a maximum capacity of 4K x 10 and multiple cards can be used to configure systems up to a maximum capacity of 65K x 10. It can also be provided in smaller capacities by de-populating the memory boards. The compact size of this system makes it ideal for use as buffer storage for various computer peripheral applications. This memory system can be easily modified to interface with the Intel 4- and 8-bit microprocessors, the 4004, 4040, 8008 and 8080.



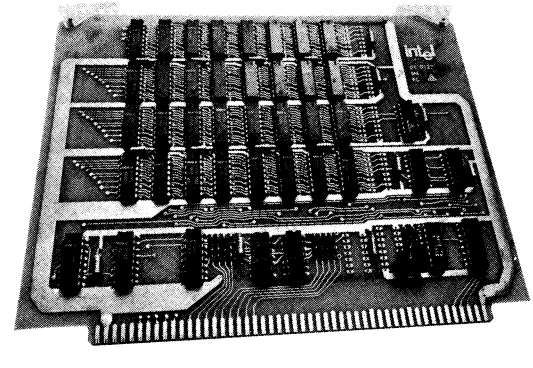
in-Unichassis

Features

- Low Cost Memory
- High Reliability
- Modular Expandability
- Module Interchangeability
- Fast Cycle Time
- Low Power Requirements
- TTL Compatible
- Compact Size
- Field Expandable
- One Power Supply Voltage
- Address Registers
- Single Board System
- Board Select
- Two Chassis Systems



in-Minichassis



Product Characteristics

Capacity:	4096 words expandable to 65K words by the addition of memory cards
Word Length:	8,9,10 bits per card. Longer words can be made by adding additional memory cards
Cycle/Access Times:	in-26A-1 — 650 nanoseconds in-26A-2 — 475 nanoseconds in-26A-3 — 375 nanoseconds
Dimensions:	
Memory Board (4K x 10)	8.175 inches High 6.0 inches Deep 0.5 inch mounting centers
Mating Connectors:	Amp 1-67878-0 Sylvania 7900-0281-X Winchester HW50D0111 Viking 3VH50/1CN5 Stanford Applied Engineering CP8000-100 CDC VPB01C50E00A1
Operational Modes:	READ (NDRO) WRITE
Interface Characteristics:	TTL-compatible-Open Collector (S/N 7438) or three-state (S/N DM 8094). Byte Select (5-bit)
DC Power Requirements:	in-26A = +5.0V ± 5% 1.25A Typical 3.0A Maximum
Temperature:	0°C to +50°C operating ambient -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating

Memory Operation

The in-26A memory system is capable of performing in the following modes: READ (NDRO) and WRITE.

Read (NDRO)

With the READ/WRITE line at 0V, the memory will perform a READ operation from the selected word and transfer the data to the output bus. The contents of the word location is not changed.

Write

With the READ/WRITE line at +V, the memory will perform a WRITE operation into the selected word. Data on the input bus will be clocked into the Data Register and stored in the Selected Word.

Standard Input Lines

The following lines carry input information to the memory system. All timing relationships are measured at the 1.5V level of the leading edge of all signals. All input signals are TTL level compatible, loading is different and will be specified for each individual input. A low input is <0.8V. A high input is > 2.0V.

Cycle Initiate

$\overline{\text{A CYREQ}}$ is required at the beginning of each cycle. $\overline{\text{CYREQ}}$ is an active low signal and should have the following characteristics:

Rise and fall times (1V-2V):	20 ns maximum
Duration (1.5V-1.5V):	100 ns
Loading:	250 µA

Read

No special signal is required to indicate a READ operation. The READ mode is mutually exclusive with the WRITE mode, hence a low input on the WRITE line at t_0 is indicative of a READ operation. Data will be available on the output bus, delayed from t_0 by the access time, associated with the address provided.

Byte Lines

Two byte control lines are provided for 5-bit byte operation. Enabling $\overline{\text{BYTE 1}}$ will write into the lower 5-bits. Enabling $\overline{\text{BYTE 2}}$ will write into the higher 5-bits.

Timing — Same as write, but opposite polarity.

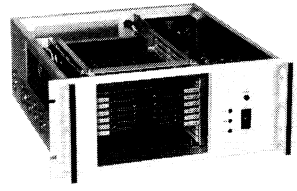
Options

- Minichassis
- UT-26/50 Series Interface Boards
- EX-26/50 Extender Boards

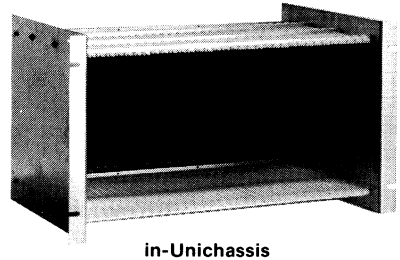
in-40 Series
GENERAL PURPOSE
RANDOM ACCESS MEMORY SYSTEM

CAPACITY: To 16K x 18/32K x 9 Per Card, Separate Control Card Drives Up to 8 Memory Cards To 256K x 9, 128K x 18 or 64K x 36 Per 7" Minichassis, Including Power To 768K x 9, 384K x 18, 256K x 36, 128K x 54 or 96K x 72 Per 10-1/2" Unichassis

The Intel® in-40/42/44 Semiconductor Memory System is available as a basic card set or mounted in a card chassis with connectors and back panel wiring. The basic system consists of three cards called the Memory Unit Card (MU), the Control Unit Card (CU), and the Buffer Unit Card (BU). This system provides 16K x 18 or 32K x 9 per card set and can be expanded to 128K x 18 or 256K x 9 by the addition of Memory Unit Cards. A single Control Unit Card is capable of addressing 128K x 18 or 256K x 9. Module selection is done internally in the memory system.



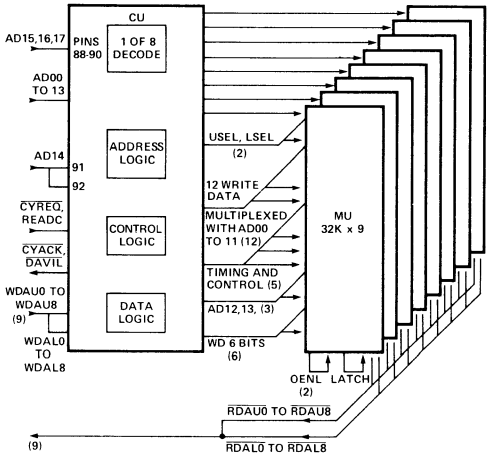
in-Minichassis
Dimensions: 7"H x 19"W x 17"D



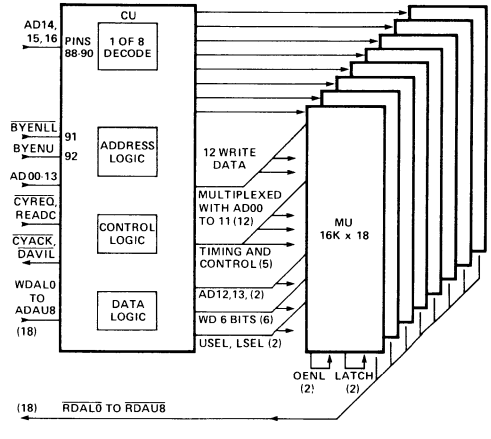
in-Unichassis
Dimensions: 10.5"H x 19"W x 12.5"D (Large)
10.5"H x 19"W x 8.5"D (Small)

Features:

- Low Cost Memory
- High Reliability
- High Density
- Modular Expandability
- Module Interchangeability
- Automatic Refresh
- Fast Cycle Time
- TTL Compatible
- Low Power Requirements
- Compact Size
- Field Expandable
- Byte Control
- Module Select
- Address Register
- Data Register (Optional)
- Basic Module Available As 16K x 18 or 32K x 9
- Two Chassis Systems



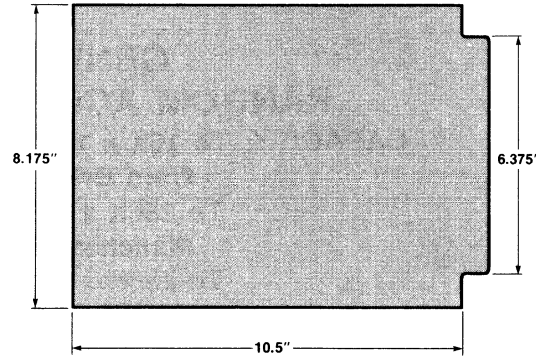
in-40 Series Block Diagram (Word Length Less Than 9-Bits)



in-40 Series Block Diagram (Word Length More Than 9-Bits)

Product Characteristics

Storage Capacity:	4096, 8192, 16,384, 32,768 words, expandable to 128K x 18 or 256K x 9
Word Length:	8,9,10,12,16 or 18-bits per memory card. Longer words are made by combining memory cards.
Cycle Time:	in-40 — 500 nanoseconds in-42 — 550 nanoseconds in-44 — 875 nanoseconds
Access Time:	in-40 — 330 nanoseconds in-42 — 400 nanoseconds in-44 — 480 nanoseconds
Retention Time:	in-40 — 2 milliseconds in-42 — 2 milliseconds in-44 — 1 millisecond
Modes of Operation:	Write Read (NDRO) Data Save R/M/W Refresh
Input/Output:	TTL Compatible
Address Input:	12-18 lines, binary (Single-ended)
Data Input:	Up to 18 lines, (Single-ended)
Data Output:	Up to 18 lines, (Single-ended)
Input Controls:	4 lines (cycle request, read/write, byte control), Single-ended
Output Controls:	2 lines (cycle acknowledge, data available), Single-ended
Temperature:	0°C to +50°C operating ambient -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating
Interface:	TTL levels all inputs and outputs
Input:	
Logic Low	-1.0 to +0.7V @ ⩽ 2 mA
Logic High	+2.2 to +5.5V @ ⩽ 100 µA
Output:	
Logic Low	-0.5 to +0.5V @ ⩽ 16 mA
Logic High	+2.4 to 5.25V @ ⩽ 200 µA
Dimensions:	Each Card, MU and CU, is ⩽0.45" thick and has the outline dimensions as shown:



Weight:	Each card weighs less than 1 pound
Optional Items:	Built-in data register which permits write data to be sampled earlier in the cycle than would normally be required.

Module D.C. Power Requirements

MU-40/42/44:

SELECTED		
Voltage	Current (Max.)	Regulation
V_{DD} +12.0V	1.3 Amps	±5%
V_{CC1} +5.0V	0.35 Amps	±5%
V_{CC2} +5.0V	0.65 Amps	±5%
V_{BB} -5.0V	<10.0 Milliamps	±5%
UNSELECTED		
Voltage	Current (Max.)	Regulation
V_{DD} +12.0V	0.20 Amps	±5%
V_{CC1} +5.0V	0.35 Amps	±5%
V_{CC2} +5.0V	0.65 Amps	±5%
V_{BB} -5.0V	<10.0 Milliamps	±5%

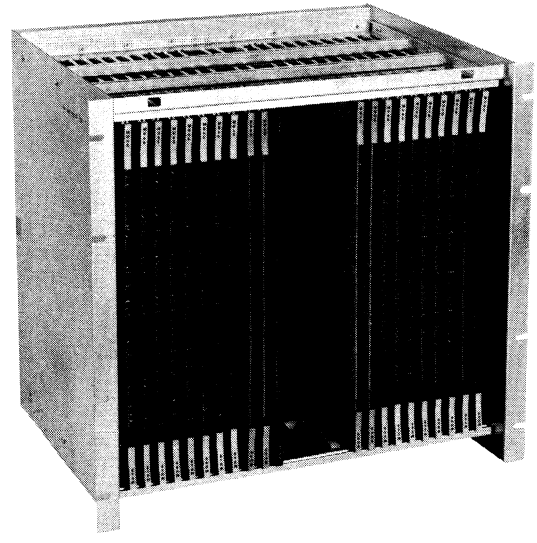
CU-40/42/44:

Voltage	Current (Max.)	Regulation
V_{CC1} +5.0V	2.00 Amps	±5%
*V_{CC2} +5.0V	0.55 Amps	±5%
V_{BB} -5.0V	0.30 Amps	±5%

*< 1.0 mA during Data Save.

in-65
GENERAL PURPOSE BORAM MEMORY SYSTEM
CAPACITY: 128K Bytes Per MU-65 Card
2 Megabytes Per Megachassis™

The in-65 is a general purpose and a very economical CCD memory system designed around the Intel® 2416 component. This product is best described and utilized as a Block-Oriented Random Access Memory. The system can be used to randomly address blocks of data and then transfer data sequentially within the data block at very high data rates. The system is available as a basic card set which consists of the CU-65, MU-65 and BU-65. The CU-65 provides all interface, timing and control logic for up to 8 MU-65's. The MU-65 contains all the memory components (2416's) and associated driver and buffer circuits. The BU-65 is synchronized to the CU-65 and provides for word length expansion. The system is available as a basic card set or mounted in a card chassis, the "Megachassis™" with connectors and backpanel wiring. Entire systems with power supplies, racks and cooling fans can also be provided. The standard system modules can be organized into many different system configurations and capacities, ranging from 1 Megabit to hundreds of Megabits. The large capacity, high performance characteristics and economy of the in-65 make it ideally suited for disc and drum replacement and data rate buffer applications.

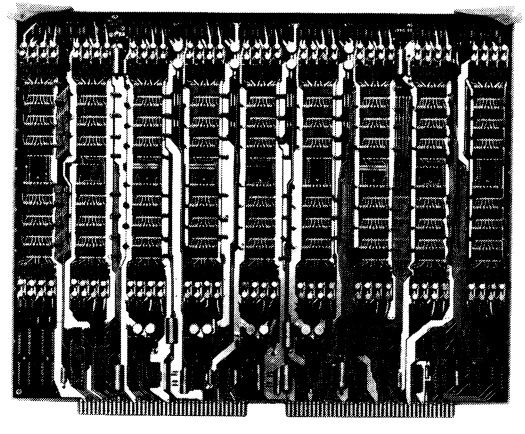


in-Megachassis™

MEMORY SYSTEMS

Features:

- Reduced Latency (150 µs average)
- Improved Reliability and Maintainability
- Modular Design
- Module Expandability and Interchangeability
- High Data Transfer Rates
- Block and Word Modes of Operation
- Low Cost
- Simple Asynchronous Interface
- Fully Buffered
- Options
  - — Byte Parity
  - — ECC
  - — Error Logger



Product Characteristics

Storage Capacity: (Maximum)	MU-65 — 128K Bytes Megachassis — 2 Megabytes (16 MU-65 cards)
Byte Length:	7,8, or 9-bits. The 9th bit can be either a parity or data bit.
Word Length:	1 to 8 bytes
Modes of Operation:	Block (Read, Write) Random or Word (Read, Write) Seek Standby/Refresh
Data Rates (Parallel Data):	.2 to 1.78 Megawords per second
Latency:	300 µs maximum, 150 µs average
Temperature:	0°C to 50°C operating ambient, -40°C to +125°C non-operating
Humidity:	Up to 90% non-condensating
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating
Cooling:	For multiple card installation, a cooling air flow of 300 cubic feet per minute is recommended.
Card Dimensions: (MU-, BU-, CU and and UT-65)	15.00 inches High 12.00 inches Deep 0.625 inch mounting centers Card Cage Clearance: 0.125 inches along the 12" card edge.
Weight (Typical):	Cards — 2 lbs. each Megachassis™ — 20 lbs. each (2 backplanes)—less boards
DC Power Requirements:	Four regulated power supply voltages are required

	Maximum	Typical
MU-65	35W	9.5W
CU-65	28W	28W
BU-65	9W	9W

Memory Operation

Interface

The standard in-65 system provides an asynchronous type interface. All interfacing to the in-65 system is to either the CU-65 or BU-65. The user does not interface directly to the MU-65. All CU-65 and BU-65 interface signals are TTL compatible and capable of driving about 3 to 4 foot interface cables. The I/O connectors used for the in-65 system card assemblies are 80-pin, double-sided connectors with 125 mil centers and 0.025 square inch wire-wrap posts. The connectors are an integral part of the backplane assembly.

Options

Parity Option -001: The in-65 has a number of possible parity options:

a. Checks byte or word parity on data transmitted from user prior to storage. The parity bit(s) may or may not be stored.
b. Generates byte or word parity on data transmitted from user for storage, or on stored data for transmittal to user.
c. Checks byte or word parity of stored data against stored parity bit(s) or (b) above.

In case of either a transmitted parity failure (a) or a storage parity failure (c), a parity error signal is returned to the user. Parity is normally calculated on an 8-bit data byte, but may be "chained" to calculate parity on longer data words, with a slight degradation in access and cycle times.

Error Correction Option -002: The in-65 memory system can be provided with error correction circuits for those systems requiring improved system reliability. The typical error correction circuits utilized with the in-65 system correct single-bit errors and detect double-bit errors.

Error Log Option -003: The in-65 system can be provided with error logging circuits to enhance system maintainability. The error log option is used in conjunction with the error correction option and stores information concerning single-bit failures.

Utility Card (UT-65) Option -004: A utility card with wire-wrap sockets for integrated circuits is available in the same form factor as the MU-65, CU-65 and BU-65. This card can be used for special customer interfaces.

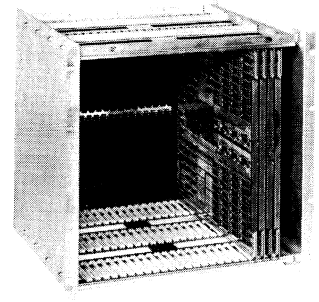
Maintenance Philosophy

The in-65 memory system requires minimal periodic maintenance or adjustments except to clean filters or fan assemblies and adjust voltages on the system power supplies. A module replacement maintenance philosophy is recommended.

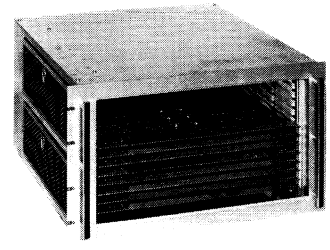
in-477
CRT REFRESH/SPECIAL PURPOSE MEMORY SYSTEM
CAPACITY: 16K x 16 (256K x 1) Per Card

The in-477 memory card is designed for storage and retrieval of digital video image data. Each card has a capacity of 256K (K=1024) bits, which will store a 512 x 512 CRT image. Cards may be operated in parallel to create a gray-scale or multi-color displays. The card may be operated in a single bit per cycle serial mode, or a sixteen bit parallel mode. The card contains a sixteen bit parallel-to-serial register with external clocking and loading, to permit a serial bit readout at higher speeds than the normal card cycle time.

Refreshing of the data in the N-Channel MOS RAM's is normally achieved by sequential scanning of the memory for CRT display refresh purposes. For special applications, the card can be refreshed externally at a rate of 64 times every 2 milliseconds, rather than 256 times every 2 milliseconds during the normal display refresh scan. This is accomplished by refreshing one row in all 64 RAM's on the card at once. A clear memory mode allows setting all memory locations to either a one or zero state in a simplified manner, if desired for Initialize, Reset, Erase or other purposes.



VCRT CHASSIS

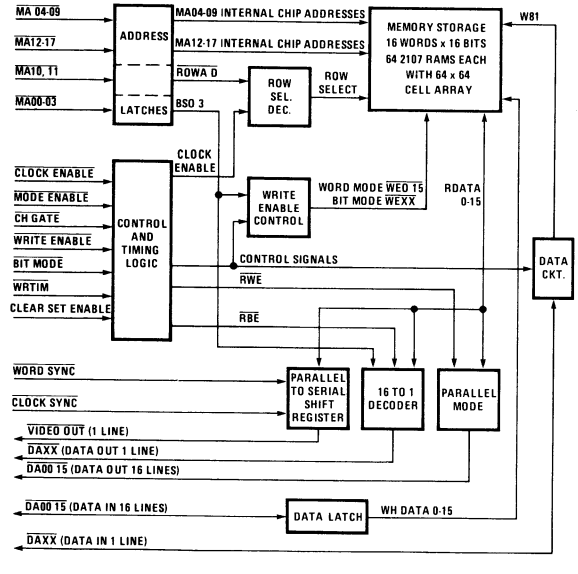


HCRT CHASSIS

MEMORY SYSTEMS

Features:

- Single Card Memory
- Designed for use with a 512 x 512 display matrix, accomplishing a complete 512-bit line refresh and update in approximately 52 microseconds
- Automatic or customer-controlled refresh
- Allows "RANDOM INSTANTANEOUS" updating of data
- Single boards can be used for "CHARACTER/GRAPHIC" displays
- Multiple boards can be used for "GRAY-SCALE AND COLOR" displays
- Two speeds are available
- Uses Intel 2107B 4K Dynamic RAM components
- Operates in parallel word, serial word, and single bit modes



Memory Block Diagram

Product Characteristics

Storage Capacity:	256K bits, addressable as a 16K word by 16-bit memory, or as a 256K word by 1-bit memory.
Cycle Time:	in-477 650 nanoseconds in-477-1 450 nanoseconds
Access Time:	in-477 350 nanoseconds in-477-1 280 nanoseconds
Retention Time:	2 milliseconds
Split Cycle:	(R/M/W Cycle) in-477 950 nanoseconds in-477-1 750 nanoseconds
Serial Data Rate:	10 megahertz, maximum
Modes of Operation:	Write Word (Parallel 16-bit data word transfer) Read Word (Parallel 16-bit data word transfer) Write Bit (Single-bit data transfer) Read Bit (Single-bit data transfer) Read Word (Serial 16-bit data word transfer) Clear Set
Interface Signals:	
Address Input:	18 lines (TTL)
Data Input/Output:	16 lines for parallel word modes, 1 line for serial word mode, plus 1 line for single-bit modes, all open collector, bi-directional lines
Clock Input Lines:	Clock Enable Write Enable Word/Bit Select Mode Enable Card Select Write Time Gate Clear Memory Enable Shift Register Load Serial Shift Clock
Logic Levels:	TTL levels for all inputs and outputs.
Temperature:	0°C to +50°C operating ambient, -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	Up to 10,000 feet operating. Up to 50,000 feet non-operating
Card Dimensions:	15 inches long by 15 inches wide, with 0.5 inch mounting centers
Power Requirements:	+5V ±5% @ 3.0A, maximum +12V ±5% @ 1.5A, maximum -5V ±5% @ 0.05A, maximum
Interface Connectors:	Interface connections for the memory can be made via two 100-pin edge connectors on the memory card which mate with any of the following connectors:

Intel	46-0010-001	CDC	VPB01C50E00A1
Viking	3VH50/1CN5	Sylvania	7900-0281-X
Amp	1-67878-0		

Memory Operation

Read Operation

Read and Write can be combined for Read/Modify/Write operation. During a parallel read operation, the full data word (16-bits) is placed on 16 bi-directional lines and transferred from memory.

At the same time, all 16 data bits read out from memory may be transferred out serially on a single line. These bits are used to refresh a video display. Serial data is transferred out via parallel-to-serial shift registers enabled by word sync and clock sync inputs.

During a single-bit read operation, the 16-bit data word is read out from memory, but only one of the 16-bits is transferred out on a single output line. Single-bit read operation can occur simultaneously with serial read out. but not simultaneously with parallel operations.

Write Operation

During parallel write mode, 16 data bits are received at the memory interface and stored. In single-bit write operations, only one selected data bit is transferred into the memory and stored. Single-bit write and parallel write operations are mutually exclusive.

Clear Set Operation

The memory may be initialized, reset or erased by means of the clear set operation which forces all 16-bits of the data word selected to a "1" or "0" level, via a single input line.

Refresh Operation

The in-477 refresh operation takes place automatically during serial read operations for video refresh. Address bits 4-11 are toggled, allowing a complete refresh operation in 256 cycles. Address lines 4-11 must be connected to the lowest order video scan address lines. No special provisions are necessary during horizontal or vertical retrace. However, if vertical retrace exceeds 1.4 milliseconds, then a refresh address counter is needed. This can be supplied by the low order bits of the video scan address counter.

The refresh enable jumper option allows an externally controlled refresh operation, which is completed in 64 cycles.

Optional Features

A number of optional features are available with the in-477 memory. These options are implemented by installing or removing certain jumpers.

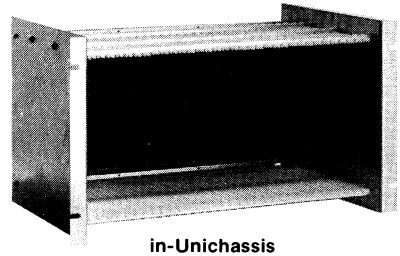
in-477 Chassis

	Maximum Capacity	Dimensions	Cooling Provided
HCRT	12 Cards	10.5"H x 19"W x 19"D	Yes
VCRT	24 Cards	17.5"H x 19"W x 19"D	No

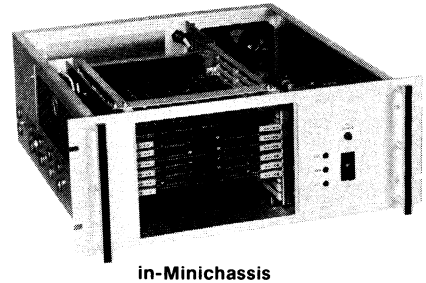
in-1600
GENERAL PURPOSE
RANDOM ACCESS MEMORY SYSTEM

CAPACITY: To 64K x 18/128K x 9 Per Card, Separate Control Card Drives Up to 8 Memory Cards
To 1024K x 9, 512K x 18 or 256K x 36 Per 7" Minichassis, Including Power
To 3072K x 9, 1536K x 18, 1024K x 36, 512K x 54 or 384K x 72 Per 10-1/2" Unichassis

The Intel® in-1600/1620 Semiconductor Memory System is available as a basic card set or mounted in a card chassis with connectors and back panel wiring. The basic system consists of three cards called the Memory Unit Card (MU), the Control Unit Card (CU), and the Buffer Unit Card (BU). This system provides 64K x 18 or 128K x 9 per card set and can be expanded to 512K x 18 or 1024K x 9 by the addition of Memory Unit Cards. A single Control Unit Card is capable of addressing 512K x 18 or 1024K x 9. Module selection is done internally in the memory system.



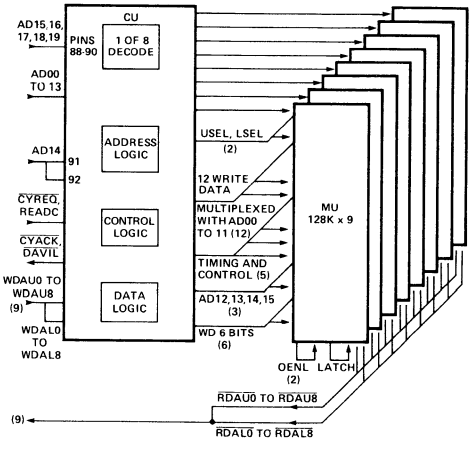
in-Unichassis
Dimensions: 10.5"H x 19"W x 12.5"D (Large)
10.5"H x 19"W x 8.5"D (Small)



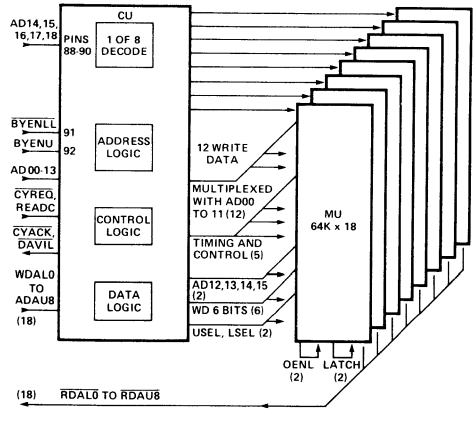
in-Minichassis
Dimensions: 7"H x 19"W x 17"D

Features:

- Low Cost Memory
- High Reliability
- High Density
- Modular Expandability
- Module Interchangeability
- Automatic Refresh
- Fast Cycle Time
- TTL Compatible
- Low Power Requirements
- Compact Size
- Field Expandable
- Byte Control (2 Zones Maximum)
- Module Select
- Address Register
- Data Register (Optional)
- Basic Module Available as 64K x 18 or 128K x 9
- Two Chassis Systems



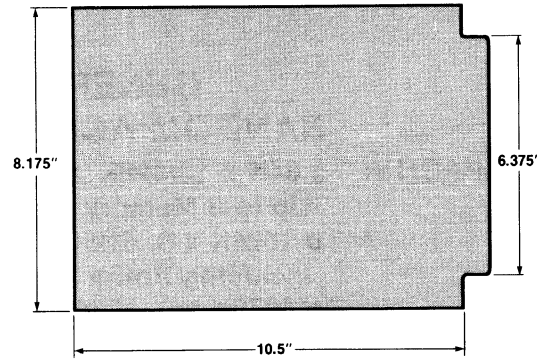
in-1600 Series Block Diagram (Word Length Less Than 9-Bits)



in-1600 Series Block Diagram (Word Length More Than 9-Bits)

Product Characteristics

Storage Capacity:	16,384, 32,768, 65,536, 131,072 words expandable to 1024K x 18 or 2048K x 9
Word Length:	8,9,10,12,16 or 18-bits per memory card. Longer words are made by combining memory cards
Cycle Time:	in-1600 — 500 nanoseconds in-1620 — 550 nanoseconds
Access Time:	in-1600 — 330 nanoseconds in-1620 — 400 nanoseconds
Retention Time:	in-1600 — 2 milliseconds in-1620 — 2 milliseconds
Modes of Operation:	Write Read (NDRO) Refresh
Input/Output:	TTL Compatible
Address Input:	14-20 lines, binary, (Single-ended)
Data Input:	Up to 18 lines, (Single-ended)
Data Output:	Up to 18 lines, (Single-ended)
Input Controls:	3 lines (cycle request, read/write, byte control), Single-ended
Output Controls:	3 lines (cycle acknowledge, memory busy, data available), Single-ended
Temperature:	0°C to +50°C operating ambient -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating
Interface:	TTL levels all inputs and outputs
Input:	
Logic Low	-1.0 to +0.5V @ $\leqslant$ 2 mA
Logic High	+2.0 to +5.5V @ $\leqslant$ 100 μA
Output:	
Logic Low	-0.5 to +0.5V @ $\leqslant$ 15 mA
Logic High	+2.4 to 5.25V @ $\leqslant$ 200 μA
Dimensions:	Each Card, MU and CU, is $\leqslant$ 0.45" thick and has the outline dimensions as shown:



Weight:	Each card weighs less than 1 pound
Optional Items:	Built-in data register which permits write data to be sampled earlier in the cycle than would normally be required.

Module D.C. Power Requirements

MU-1600/1620:

SELECTED		
Voltage	Current (Max.)	Regulation
V_{DD} +12.0V	1.6 Amps	±5%
V_{CC1} +5.0V	0.85 Amps	±5%
V_{CC2} +5.0V	1.15 Amps	±5%
V_{BB} -5.0V	13.0 Milliamps	±5%
UNSELECTED		
Voltage	Current (Max.)	Regulation
V_{DD} +12.0V	0.26 Amps	±5%
V_{CC1} +5.0V	0.85 Amps	±5%
V_{CC2} +5.0V	1.15 Amps	±5%
V_{BB} -5.0V	13.0 Milliamps	±5%

CU-1600/1620:

Voltage	Current (Max.)	Regulation
V_{CC1} +5.0V	3.00 Amps	±5%
V_{CC2} +5.0V	0.55 Amps	±5%
V_{BB} -5.0V	0.30 Amps	±5%

in-3000
GENERAL PURPOSE AND MINICOMPUTER RANDOM ACCESS MEMORY SYSTEM

CAPACITY: To 64K x 22 Per Card
To 256K x 22 or 128K x 44 Per 5-1/4" HMS Chassis, Including Power

Presently available memory systems can be updated to higher densities and better performance with the in-3000 series which is available as:

1. A single printed circuit card memory system with its own control, optional error correction and detection. The in-3000 memory card (MU-30XX) contains all the required memory interface logic and up to 64K words x 22 bits of 16K x 1-bit (or 8K x 1) Dynamic RAMs.
2. Up to 4 printed circuit memory cards (MU-30XX) horizontally-mounted in a chassis complete with connector, back plane wiring, self test card, optional interface card, and power supply.

Features:

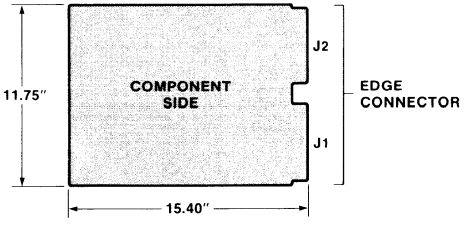
- Stand-alone memory system
- Automatic refresh or customer controlled refresh
- Variable memory size per board
- Single board as a memory system
- Variable bit length per word
- Fast Cycle Time
- Fast Access Time
- High Reliability
- Modular Expandability
- Field Expandable
- ECC Option
- ±15V Option
- TTL Compatible
- Optional termination on the board
- Self-Test card with microprogrammable control
- EMM μ3000 system compatible

Interface — Memory System Single Card

Pin No.	Edge Connector J1	Edge Connector J2	Pin. No.	Edge Connector J1	Edge Connector J2
01	0V	0V	41	0V	0V
02	+5V	DI06	42	+5V	DI01
03	-5V	DI07	43	-5V	DI00
04	0V	DI05	44	0V	DI08
05	+12V	DI04	45	+12V	DI17
06	+V TERM	D006	46	AI08	D003
07		D007	47	AI07	D002
08		D005	48	AI06	D001
09		D004	49	AI11	D000
10		DI03	50	AI10	D008
11		DI02	51	0V	D017
12			52	AI09	DI16
13			53	AI03	D016
14			54	0V	D015
15			55	AI04	0V
16			56	AI05	DI15
17			57	0V	DI14
18			58	AI00	D014
19			59	AI01	D013
20			60	0V	0V
21			61	AI02	DI13
22			62	AI12	DI12
23			63	GR	D012
24	AI15		64	COOP	0V
25			65	WP	0V
26			66	0V	0V
27	SC	D020	67	0V	0V
28	MS3	DB ERR	68	DI18	0V
29	MS2	D021	69	DI19	D011
30	MS1		70	AI14	DI11
31	BCL2	DISA ECC	71	D018	DI10
32	ADOP	ECHK	72	D019	D010
33	MB	DI20	73	XA 1	D009
34	AI13	DI21	74		DI09
35	BCL1	0V	75	XA 2	+V TERM
36	DA	+12V	76		+12V
37	TIOP	0V	77		0V
38	MEM PROTECT	-5V	78	XA 3	-5V
39		+5V	79	RP	+5V
40	0V	0V	80	0V	0V

Product Characteristics

Storage Capacity:	16,384, 32,768, 65,536 words per board expandable to 256K x 22 or 512K x 11 per system with multiple boards
Word Length:	16 or 22-bits per memory card. Longer words are made by combining memory cards
Cycle Time:	450 nanoseconds
Access Time:	275 nanoseconds
Note: With ECC option -001, add 50 ns to the access time.	
Retention Time:	2 milliseconds
Modes of Operation:	Write Read (NDRO) Read-Modify-Write Refresh
Input/Output:	TTL Compatible
Address Input:	14-20 lines, binary (Single-ended)
Data Input:	Up to 22 lines, (Single-ended)
Data Output:	Up to 22 lines, (Single-ended)
Input Controls:	11 lines, Single-ended, Initiate, Byte Control$_1$, Byte Control$_2$, Split Cycle, Write Pulse, General Reset, address option, timing option, ECC check, ECC disable, memory protect
Output Controls:	5 lines (memory busy, double error, write parity, memory protect, data available). Single-ended
Temperature:	0°C to +50°C operating ambient -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating
Interface:	TTL levels all inputs and outputs
Input:	
Logic '1'	-1.0 to +0.7 Volts @ $\leq$ 2 mA
Logic '0'	+2.2 to +5.5 Volts @ $\leq$ 2 μA
Output:	
Logic '1'	-0.5 to +0.5 Volts @ $\leq$ 60 mA
Logic '0'	+2.4 to 5.25 Volts @ $\leq$ 1 μA
Dimensions:	Each printed circuit card has the outline dimensions: 11.75 x 15.40 inches, as shown:

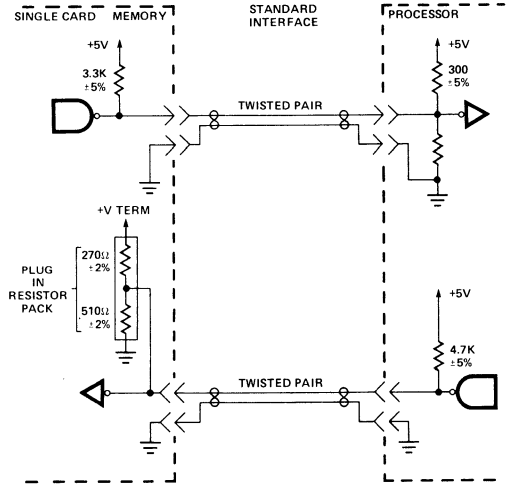


Weight:	Each card weighs less than 2 pounds
Optional Items:	
-001	ECC
-003	±15V option
-004	Termination on board
-005	Extender Card
-006	Chassis with Power Supply
-007	Self-Test Card
-008	Custom Interface Card
D.C. Power Requirements:	
*Single Memory Cards:	+12V ±5% — 1.7 Amps max. +5V ±5% — 6.0 Amps max. -5V ±5% — 0.08 Amps max.
Termination Voltage:	+5V ±5% — 0.7 Amps max.

*Large systems with a self-test card/optional interface card add 10 amps (max.) to +5V D.C.

Interfacing and Pin Assignments

The in-3000 series single printed circuit memory card is designed to use two (2) 80-pin edge connectors with pins on 0.125 inch centers. All signals between the processor and the single printed circuit memory card must be carried on twisted pair transmission lines.



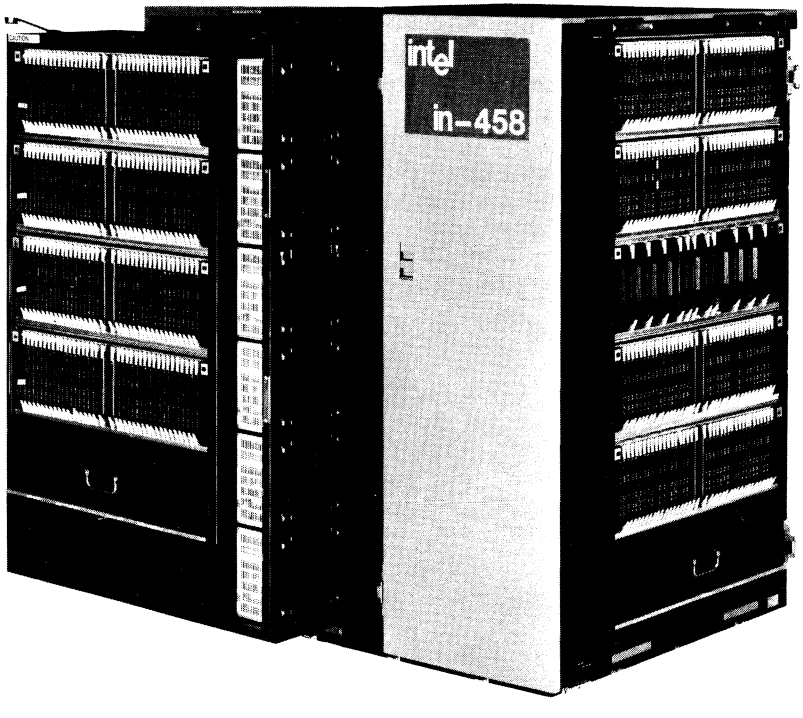
Memory To Processor Interface Circuitry

in-4580
BORAM OR RANDOM EXTENSION MEMORY SYSTEM
CAPACITY: 1 Megaword by 60 or 64 Bits Plus 8 Error Correction Code Bits

The Intel® in-4580 is a monolithic memory system capable of storing a minimum of 262K words and a maximum of 1 Megaword of information. The Intel® in-4580 can be used to extend the CPU storage or as a swapping storage media for virtual operating systems. The system consists of a frame, power supplies, basic storage modules, cooling fans, interface unit and cables.

Features:

- Free-standing unit
- 1,048,576 words x 60 or 64 bits plus 8 additional bits of error detection/correction information
- Single channel access to storage
- Single-bit error correction and double-bit error detection
- Automatic error logging to tally single and double-bit errors for later preventive maintenance
- Field-expandable
- ECL-compatible interface
- Uses 2107B — 4K MOS Dynamic RAM Component
- Refresh — 2 milliseconds — transparent to user
- 100 ns maximum sequential accesses
- 600 ns maximum random accesses
- Minimum block length (16 words)



Product Characteristics

Input Power Requirements:	Voltage: 208V/230V ±10% Frequency: 3-phase 60 Hz
Physical Dimensions:	60 inches High 40 inches Wide 37 inches Deep
Cycle Time (16K words):	Write — 1.6 µs Read — 1.6 µs
Access Time:	600 ns first transfer, 100 ns on subsequent transfers
Ambient Temperature:	0°C to 45°C Operating -18°C to +85°C Non-operating
Humidity:	0 to 90% with no condensation
Altitude:	10,000 feet operating, 30,000 feet non-operating

System Description

Mechanical

The frame incorporates two gates, a fixed gate on the right and swing-out gate on the left. The fixed gate on the right contains the interface unit and has room for four (4) BSM's each containing up to 1/8 Megaword. The swing-out frame on the left contains four (4) BSM's. Each gate has its individual cooling fans and filters.

Storage Element

The basic storage element is the Intel® 2107B device which is a 4096 bit MOS N-Channel Random Access Memory (RAM). This device is TTL-compatible with 200 ns access time and a cycle time of 400 ns. Sixty four (64) of these devices are organized on a printed circuit memory module in 32K x 8 organization. Either 18 or 36 of the above modules are used to make up the Basic Storage Module (BSM).

Power Supplies

The in-4580 memory system is built with modular power supplies. The power supplies receive their "raw" AC from a power distribution unit.

Power Distribution Unit (PDU)

The PDU can be operated either locally or in a remote power control mode. The PDU contains power sequencing circuitry and over and under voltage sensing. If any of the DC voltages deviate from the specified tolerances, the memory system is "powered down" and LED indicators display when a particular voltage has failed.

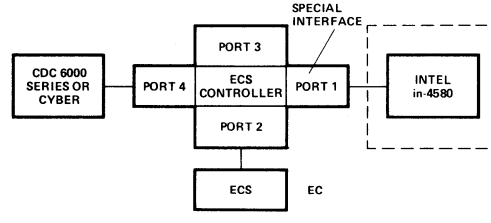
Cooling Unit

The cooling unit consists of 4 fans placed at the bottom of each gate. The cooling unit will force 1000 cubic feet per minute of computer room air through the BSM's. No under-floor cooling air is required.

Interface Unit

The custom-built interface unit contains all transmitters, receivers, data, address and control logic elements necessary to operate the memory.

Typical Application

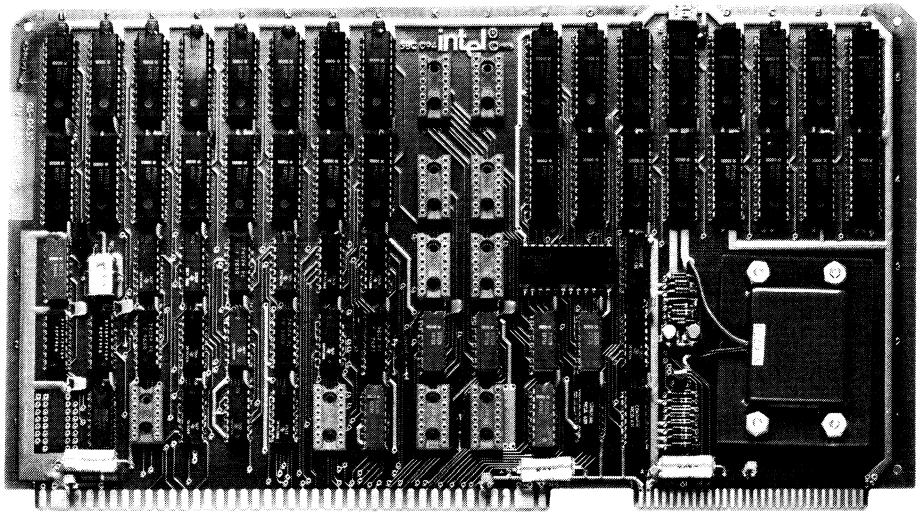


in-8100
INTEL NON-VOLATILE RANDOM ACCESS MEMORY SYSTEM
CAPACITY: 2048 x 16 or 4096 x 8

The Intel® in-8100 Series is a single card memory designed to meet non-volatile requirements of Random Access Memory (RAM) Systems. The memory system retains the data integrity for 96 hours after the loss of main input power. The in-8100 Series RAM system is supplied with an on-card battery — Nickel-Cadmium. Battery charging capability is included. Extended backup time can be achieved by external battery connection. The maximum storage capability is 4096 x 8 words per board. A large RAM system can be configured with multiple cards.

Features:

- Single board memory
- Single +5V voltage
- Battery backup — Non-volatility
- No refresh
- Modular expandability
- TTL compatible
- Low power requirement
- Basic system available 4096 x 8
- High Reliability
- Module Select
- Field Expandability



Product Characteristics

Storage Capacity/ Board:	2048 x 16 or 4096 x 8 bits
Word Length:	8-bits or 16-bits via reconfiguration jumpers
Access/Cycle Time:	720/770 ns
Modes of Operation:	Read (NDRO) Write
Interface Signals:	TTL Compatible
Address Lines:	16 lines, single-ended
Data Input/Output Lines:	Up to 16 lines, bi-directional
Input Control Lines:	Memory Read, Memory Write, Inhibit, Reset (all active low) — Primary AC Low (Active High), Power Fail Sense Reset (Active Low) - Battery Backup
Output Control Lines:	Transfer Acknowledge, Advanced Acknowledge (Both Active Low) — Primary Power Fail Sense, Power Fail Interrupt (Both Active Low) — Battery Backup
Internal Control Line:	Memory Protect
Input Power:	+5V ±5%, 1.7A worst-case operating
Battery Backup:	Standby power for memory array and associated backup logic. Data integrity guaranteed for 96 hours
Temperature:	0°C to 55°C operating ambient (no moving air) -40°C to +125°C non-operating
Relative Humidity:	Up to 90% non-condensating
Altitude:	Up to 10,000 feet operating Up to 50,000 feet non-operating
Form Factor:	The memory is packaged on a single PC board 12.00" x 6.75" which is designed to be mounted in a card cage on 0.6" centers

Memory Operation

The memory will perform READ (NDRO) and WRITE operations and also support battery backup.

Read (NDRO)

With the Memory Read Command line at 0V, the memory will perform a READ operation from the selected word and transfer the data to the data bus. An Acknowledge signal will also be generated on the bus. The contents of the word location are not changed.

Write

With the Memory Write Command line at 0V, the memory will accept data from the data bus and perform a write operation into the selected word. An Acknowledge signal will also be generated on the bus.

Battery Backup

In the event that main power fails, on-board batteries supply power to the memory array and thus assure data integrity. Rechargeable 150 mA Hr Ni-Cad batteries are used. The batteries are mounted on the PC board in a small case which is field replaceable. The batteries are capable of supporting the memory array for a minimum of 96 hours. There is an on-board fuse protecting the on-board charging circuit for the batteries. There is also a switch which switches the batteries off and on; thereby disconnecting them from the load.

Device

The board uses the Intel® 5101 CMOS 1K RAM's to implement the memory array. These devices provide minimum power dissipation, minimum cost and minimum access time.

Base Address Selection

For 4K x 8 configuration, base address selection is on 4K boundaries. For the 2K x 16 configuration, base address selection is on 2K boundaries.

memory system applications

Applications for memory systems are numerous and require a variety of speeds, organizations and features. The Intel product line is designed to meet these needs; and new products, incorporating the latest technology, are being added continuously.

in-26A-General Purpose RAM Memory System

Requirement

CRT refresh of a 512 line by 256-bit or 256 line by 256-bit display is required. Effective access time is zero nanoseconds and effective Read/Modify/Write cycle time is 200ns,

Solution

Thirty two (32) in-26A memory boards with two (2) address cards and one (1) control card are needed. Eight-way interleave of blocks of four MU's to achieve cycle time and a look-ahead address scheme which, along with the interleave, effects a zero nanosecond access time after the initial 800ns latency time.

in-40-General Purpose RAM Memory System

Requirement

A memory system is needed which will accept a real time digitized signal, store consecutvie time blocks of this signal, and read out the time blocks at data rates of 10, 100, or 1000 times the input data rate. The process yields three modes of time compression of the input signal. Since the time compressed signal is processed by a sequential framing device (much like a television system), the data can be repeated on a frame-by-frame basis. The frame rate for this system will be 30Hz or 33.3 milliseconds in length. The analog bandwidth is 10MHz which will require a minimum of 23×10^6 words/second data rate.

Solution

Five (5) CU-40's and twenty (20) MU-40's configured as a 64K x 88 (90) memory is provided. The I/O and control boards serially shift eleven (11) 8-bit bytes for a parallel, 88-bit load. A number of read cycles take place, equal to the compression factor (10, 100, 1000), for each write cycle with one of each eleven bytes of read data accumulating per read cycle, allowing 10 bytes to be shifted out during the write.

in-1600-Computer Main Memory

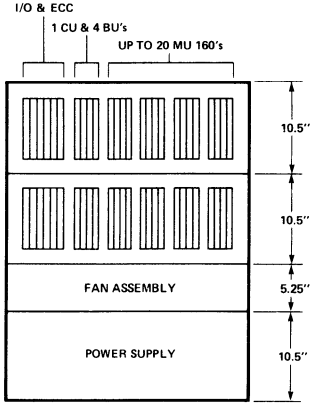
Requirement

A main memory is required for a large computer system. Modularity, maintainability, density and high reliability are of primary importance; and very fast supplier delivery of both prototypes and production units is needed. Each memory has capacities from 128K to 512K 4-byte words and it would be desirable to have two 512K word memories in one cabinet.

Solution

A truly up-to-date and superior solution is the in-1600 Series memory system, which is a 16K RAM version of the versatile 4K RAM in-40 Series. The in-1600 uses the in-40 hardware and accessories, thus allowing for fast prototyping and transfer to production. The basic building block is a 64K x

16/18 (128K x 8/9) memory module which, when used in conjunction with Control Units (CU's) and Buffer Units (BU's), can be assembled into virtually any large capacity configuration of memory. ECC, if desired, is easily done on a system-level basis. Assuming ECC is used, each 512K word memory consists of twenty (20) MU-160 (128K x 8 each), 1 CU-160 and 4 BU-160 cards. De-population of 128K word segments is done by removing five (5) MU-160 cards. This results in 40-bit words, allowing for a 32-bit data word, seven (7) bits of ECC, plus 1 extra bit. Port interface control and ECC require up to seven (7) more cards, depending on complexity, per memory. The two memories are mounted in two standard 33-slot Unichassis, taking less than 40" of chassis space with fans and power supplies included. Intel sales personnel are prepared to discuss this and other approaches to organizing large memory systems.



in-1600 – DUAL 524K x 32 PLUS ECC

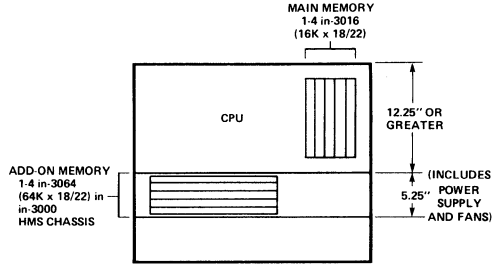
in-3000-Minicomputer Memory

Requirement

A special-purpose processor, requiring 500 ns cycle time memory in capacities of 16K to 64K of 18-bit word, (with parity) with some applications needing an additional 64K to 256K words of memory. The customer is concerned with memory reliability for larger systems. Main memory must be partitioned on 16K word boundaries, add-on memory at 64K words.

Solution

Use the in-3000 as a plug-in card for main memory, and a 5-1/4" chassis, complete with power supplies, for add-on memory. Use one through four 16K x 18 in-3016 modules for main memory and one through four 64K x 18 in-3064 modules in an in-3000 HMS Chassis for add-on memory. For systems where highest reliability is desired, incorporate the in-3000 ECC option in either or both the in-3016 and in-3064. Ask your Intel representative to discuss the high reliability of the in-3000 Series and the trade-offs concerning ECC.



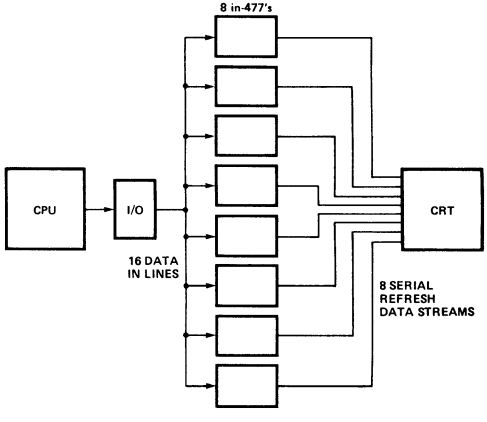
in-477-CRT Refresh

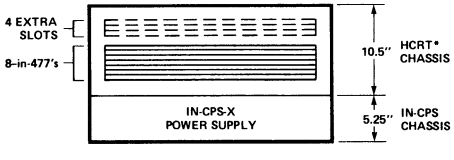
Requirement

Image processing of digitally-transmitted photographs on a CRT screen in a 512 x 512 matrix. Thirty two (32) levels of gray-scale for resolution and three (3) bits of control are required with random updating of one or more bits of each pixel. Data to be transferred in 16-bit words.

Solution

Use eight (8) in-477 memory cards, each with 16K x 16 (256K x 1) of memory and control required to take 16-bit words and refresh eight (8) bit pixels on a 512 x 512 CRT screen. Five (5) bits (5 in-477's) of each pixel to be used for 32 levels of gray scale, the remaining three bits (3 in-477's) of each pixel for control functions. Mount the in-477 cards in an HCRT chassis, which has 12 slots free to do special control and I/O logic. The UT-477, with space for over 100 DIP sockets, simplifies wire-wrap of extra logic required. Your Intel representative can assist you in defining your unique CRT refresh application and can quote individual in-477 cards or fully-interfaced systems.





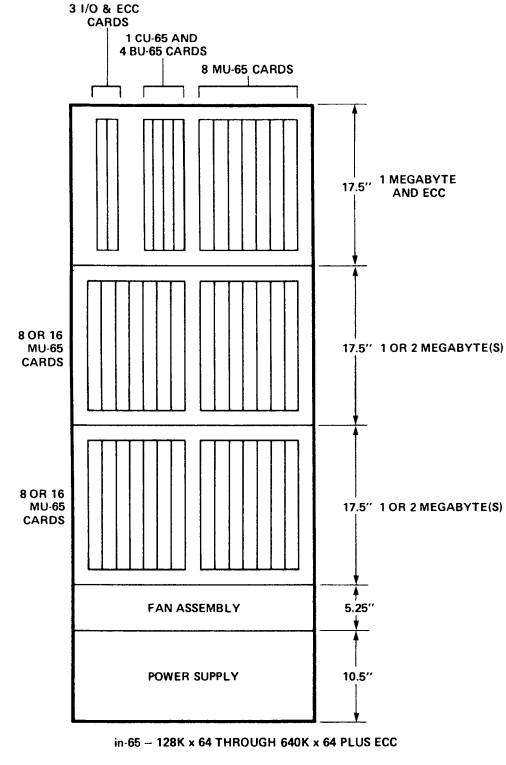
in-65-Disc Replacement Memory

Requirement

A replacement for a fixed-head per track disc memory is required to improve system reliability and maintainability and drastically reduce latency time. The disc being replaced has a capacity of 5 megabytes, but many applications are less than 5 megabytes.

Solution

Use a modular in-65 system that has a maximum capacity of 5 megabytes, but can be de-populated in 1 megabyte increments. Organization of the MU-65 (128K x 8/9) permits efficient incorporation of ECC if each megabyte is organized as 128K x 64 data bits (8 bytes), plus 8-bits of ECC. The first megabyte of storage, I/O and ECC are located in one in-65 Megachassis™, with additional memory added in either one or two megabyte chassis. Interface can be 16, 32 or 64 data bits wide. The Intel representative in your area can assist you in defining a solid-state disc replacement for your application.



in-65 – 128K x 64 THROUGH 640K x 64 PLUS ECC

MEMORY SYSTEMS

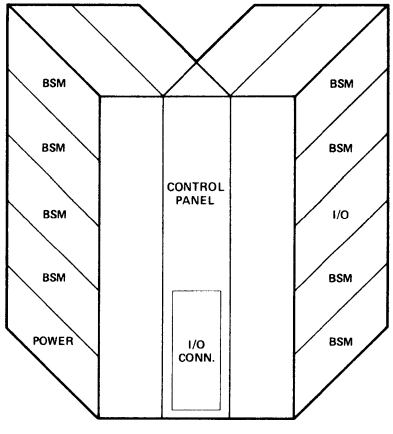
in-458-BORAM Extension Memory

Requirement

A customer with a large computer system must add additional extension memory to an existing add-on core memory system. Since very fast data transfer is required, a 64-bit data word every 100ns, a Block-Oriented Random Access Memory (BORAM) mode of operation is acceptable.

Solution

Memory in 1024K (1 million) word segments per cabinet is supplied with the in-458 BORAM or RAM system. Since the data transfer rate requirement is so high, the memory is best used in the BORAM mode and organized as 64K x 1024-bits (16 words of 64-bits each), plus 128 ECC bits (16 ECC words of 8-bits each) for a total of 1152-bits per data transfer. Even taking refresh into consideration, since a dynamic memory device is used, a data transfer rate of 100ns or faster per word is accomplished. Dynamic MOS memory results in the most cost-effective and lowest power consumption solution. The memory consists of 8 BSM's (Basic Storage Modules) of 64K x 144-bits each mounted into an easily-maintainable computer-type cabinet. All power supplies, interface and cooling is self-contained with the memory. If your application is for a lot of expansion memory, contact your local Intel representative.



in-8100-Process Control Memory

Requirement

A manufacturer of process control equipment needs to locate relatively small amounts of 16-bit memory distributed throughout a plant, and since operational integrity is essential, localized battery backup is a necessity.

Solution

Using the 2K x 16 in-8100 CMOS memory card, easy-to-use static memory can be placed wherever storage capacity is required. Each in-8100 card has its own rechargeable battery backup system mounted directly with the memory. Data is retained up to 96 hours with the self-contained battery, with additional capacity easily added remotely. Ask your local Intel sales representative how to solve your memory problems.

Conclusion

These are only eight memory applications that fit existing Intel Memory Systems' capability. Our experience is a historical encyclopedia of semiconductor memory technology and accomplishments. We are writing today's chapter — and your application should be part of it.

memory system accessories

Memory Cabinets

The in-Series Memory Cards are available as individual units or as complete systems. Intel features a number of memory cabinets that can accomodate a variety of memory capacities. The in-CAB Series of cabinets are designed to allow customers maximum freedom in specifying memory configurations. These cabinets contain power supplies, cooling fans and interface connections. The in-CAB is a standard RETMA 19" rail configuration, including lockable casters, convenience outlets and intra-cabinet cabling. Heights available up to 7 feet.

in-BA Blower Assembly

Standard 5-1/4"H x 19"W x 13"D rack-mountable six-fan blower assembly for use with all in-Series Memory Systems.

MT-10 Memory Tester

A full five-pattern memory tester for maintenance, trouble-shooting, incoming tests, etc. For use with in-40/42/44 Series Memory Systems.

UT-10 Utility Socket Board

A standard sized board with room for approximately 100 14 or 16 pin sockets for use in assembling custom interfaces to use with in-40/42/44, in-65, in-477. Specify UT-80 for in-40/42/44 or other memory systems requiring a mix of sockets with from 14 to 40 pins.

EX-10 Extender Boards

Permits trouble-shooting and maintenance to be performed on individual cards.

EX-10 for all 8"x10" cards
EX-50 for all 6"x8" cards
EX-65 for in-65 cards
EX-477 for in-477 cards

Unichassis Backplane Interface Connector

Provides fast, reliable interconnection to the in-Series memory system via the backplane wire-wrap pins. (Interfaces to 100 pin-connector)

PCB Mating Connector

100-pin mating connector for use with the following standard Intel memory boards — in-26A, in-40, in-477, in-481.

Chassis

The in-Series Memory Systems are designed in modular form for ease of conversion into a variety of sizes and configurations. These standard chassis were designed to accommodate specific customer applications. These are described below. Your local Intel sales representative can help you with your particular application.

Power Supplies

The in-Series Memory Systems are designed in modular form allowing conversion into a variety of sizes and configurations. To accomodate these various memory sizes, Intel has designed standard power supply modules for use in configuring these systems. Contact your local Intel Memory Systems representative for the one that fits your particular application.

The in-MINICHASSIS memory chassis is designed to accommodate up to 8 memory cards. The memory cards are mounted horizontally with room for a control card and 1 UT-10/40 interface card. This Minichassis is 7" high and includes power supplies and cooling fans. It is mounted on slides for ease of movement in and out. All connections are made from the rear of the unit and it can be mounted in a 19" relay rack. Front panel includes a circuit breaker and power indicator lights. This unit features the use of a PC backplane for all power and ground connections.

in-MPS Power Supply

The minichassis power supply provides the optimum solution for all in-40/42/44 and in-1600/1620 systems having capacities shown in the charts below. The MPS is included in the minichassis.

A +5V only version of the in-MPS is included for all minichassis versions of the in-26A.

in-26 WORDS

BITS	4K	8K	16K	32K	40K
10	X	X	X	X	X
20	X	X	X		
30	X	X			
40	X	X			

in-40 WORDS

BITS	16K	32K	64K	128K	256K
9	X	X	X	X	X
18	X	X	X	X	
27	X	X	X		
36	X	X	X		

The in-UNICHASSIS memory chassis is designed to accommodate up to 33 memory and control cards for mounting in a 19" relay rack. This chassis features the use of a full PC backplane with internal power and ground. The chassis can be wired for a number of memory sizes and configurations, and also be used in multiples for even larger memory configurations. It is 10.5" high, 12" deep and can be used with the in-Series cabinets. Use the in-SPS or in-LPS series of power supplies.

in-SPS Power Supply

For in-26A memory systems only +5V is required. The in-SPS power supply is used for memory capacities above the minichassis.

RETMA dimensions: 7"H x 19"W x 21"D

Model
in-SPS-1
in-SPS-2
in-SPS-3
in-SPS-4
in-SPS-5
in-SPS-6
in-SPS-7
* in-SPS-8

in-26 WORDS

BITS	4K	8K	16K	32K	64K
9	-1	-1	-2	-3	-4
18	-1	-2	-3	-4	-5
27	-2	-3	-4	-5	-6
36	-2	-3	-4	-6	-7
72	-3	-4	-5	-7	-8

*in-SPS-8 Requires 19" Drawer.

in-LPS Power Supply

For in-40/42/44 and in-1600/1620 memory systems above the capacity of the minichassis, use the in-LPS.

RETMA dimensions: 7"H x 19"W x 21"D

Model	Dwrs.
in-LPS-1	1
in-LPS-2	1
in-LPS-3	1
in-LPS-4	1
in-LPS-5	2
in-LPS-6	2
in-LPS-7	2

WORDS

BITS	16K	32K	64K	128K	256K	512K
9	-1	-1	-1	-1	-1	-2
18	-1	-1	-1	-1	-2	-3
36	-1	-1	-2	-2	-3	-5
72	-2	-2	-3	-4	-5	
144	-4	-4	-5	-6	-7	

The in-JUMBOCHASSIS is designed for memory systems that may be mounted in a 24" cabinet. With integral power supplies and fan assemblies, it measures only 14"H x 24"W x 24"D. Thirty three (33) card slots are available to house thousands of combinations of standard-sized Intel memory cards. For example, a 512K x 8 or 1024K x 9 in-40 system can be housed with seven I/O slots left over for address and buffers or for other custom logic.

The in-MEGACHASSIS™ will accomodate one or two each 11-slot PC backplanes. Each backplane will handle up to 8 MU-65's, 2 CU-65's and/or BU-65's, plus one I/O slot for a UT-65 (socket card). Power supplies and cooling fans are not included in this chassis. Dimensions are 17.5"H x 19"W x 14"D. Use the in-GPS series of power supplies.

in-GPS Power Supply

For the in-65 Megachassis™, use the in-GPS Series of power supplies.

RETMA dimensions: 7"H x 19"W x 21"D

MU-65 Qty.	Model	Power Supply Drawers
1-8	in-GPS-1	2
9-16	in-GPS-2	2

Note: Consult factory for confirmation of in-GPS power.

The in-HCRT is a 12-slot chassis, including cooling fans, used for a combination of in-477 CRT Refresh Memories and custom control interface cards mounted horizontally. A UT-477 is available for custom logic. Dimensions of the in-HCRT are 10.5"H x 19"W x 19"D. Use the in-CPS series of power supplies.

The in-VCRT is similar to the in-HCRT Horizontal Chassis, except in-477 boards are mounted vertically. Up to 24 in-477 boards can be mounted in the in-VCRT. The UT-477 can also be used for custom logic. Power supplies and cooling fans are not included. Dimensions of the in-VCRT are 17.5"H x 19"W x 19"D. Use the in-CPS Series of power supplies, and the in-BA Blower Assembly.

in-CPS Power Supply

For the two new chassis for the in-477 CRT Refresh memory board, the in-CPS provides the best power supply solutions. The horizontal mount (in-HCRT) has space for up to 12 in-477 boards and the vertical mount (in-VCRT) has space for up to 24.

in-477 Qty.	Model	Power Supply Drawers
1-4	in-CPS-1	1
5-8	in-CPS-2	1
9-16	in-CPS-3	1
17-24	in-CPS-4	1

Note: Specify if power is to be other than 110VAC, 50/60 Hz.

Megachassis
(in-65 Boards Only)
Board Allocation Guide

WORDS	CU = 1		CU = 1		CU = 1				CU = 1				CU = 1			
	BU = 0		BU = 1		BU = 2				BU = 3				BU = 4			
	8	9	16	18	24	27	32	36	40	45	48	54	56	63	64	72
128K	1A	1B	2A	2B	3A	3B	4A	4B	5A	5B	6A	6B	7A	7B	8A	8B
256K	2A	2B	4A	4B	6A	6B	8A	8B	10A	10B	12A	12B	14A	14B	16A	16B
384K	3A	3B	6A	6B	9A	9B	12A	12B	15A	15B						
512K	4A	4B	8A	8B	12A	12B	16A	16B								
640K	5A	5B	10A	10B	15A	15B										
768K	6A	6B	12A	12B												
896K	7A	7B	14A	14B												
1024K	8A	8B	16A	16B												

MU = 128 X 8. . . . . A
MU = 128 X 9. . . . . .B

CHASSIS WITH ONE BACKPLANE ☐
CHASSIS WITH TWO BACKPLANES ☐

Minichassis/Unichassis*
(For in-26A in-40/42/44 and in-1600/1620 Boards)
Board Allocation Guide

	WORDS	CU's = N						CU's = N				CU's = N		CU's = N	
								BU's = N				BU's = 2N		BU's = 3N	
		8	9	10	12	16	18	24	27	32	36	40	48	64	72
N = 1	16K	1F	1E	1D	1C	1B	1A	2C		2B	2A		3B	4B	4A
	32K	1B	1A	2D	2C	2B	2A	4C		4B	4A		6B	8B	8A
	48K	3F	3E	3D	3C	3B	3A	6C		6B	6A		9B	12B	12A
	64K	2B	2A	4D	4C	4B	4A	8C		8B	8A		12B	16B	16A
	80K	5F	5E	5D	5C	5B	5A	10C		10B	10A		15B	20B	20A
	96K	3B	3A	6D	6C	6B	6A	12C		12B	12A		18B	24B	24A
	112K	7F	7E	7D	7C	7B	7A	14C		14B	14A		21B		
	128K	4B	4A	8D	8C	8B	8A	16C		16B	16A		24B		
N = 2	160K	5B	5A	9D	9C	9B	9A	18C		18B	18B				
	192K	6B	6A	10D	10C	10B	10A	20C		20B	20B				
	224K	7B	7A	11D	11C	11B	11A	22C		22B	22B				
	256K	8B	8A	12D	12C	12B	12A	24C		24B	24B				
N = 3	283K	9B	9A	13D	13C	13B	13A								
	320K	10B	10A	14D	14C	14B	14A								
	352K	11B	11A	15D	15C	15B	15A								
	384K	12B	12A	16D	16C	16B	16A								
N = 4	416K	13B	13A	17D	17C	17B	17A								
	448K	14B	14A	18D	18C	18B	18A								
	480K	15B	15A	19D	19C	19B	19A								
	512K	16B	16A	20D	20C	20B	20A								
N = 5	576K	18B	18A	22D	22C	22B	22A								
	640K	20B	20A	24D	24C	24B	24A								
N = 6	704K	22B	22A												
	768K	24B	24A												

MU CAPACITY

A = 16K X 18 C = 16K X 12 E = 16K X 9 (use 8K X 18)
B = 16K X 16 D = 16K X 10 F = 16K X 8 (use 8K X 16)

MINICHASSIS ☐
UNICHASSIS ☐ + ☐

*For in-1600/1620 multiply word capacity shown by a factor of four (4) for chassis capacity.

MEMORY SYSTEMS

custom memory systems

Since 1971 well over 100 different memory modules have been designed, many of these designed exactly to the specifications of custom requirements. Devices ranging from 256-bit to 16K bit RAM's, numerous shift register and 16K CCD's have been used, as required, in best meeting the specific needs of our customers.

Presently, we have design knowledge and experience in each of the following Intel memory types, plus all of the latest driver and other support devices. Of particular note is our unique experience designing with the 2104A/2108/2116 inter-compatibility line of dynamic 4K, 8K and 16K devices.

Devices

Types	Organization	Pins/Package
Dynamic		
2107	4K x 1	22
2104A	4K x 1	16
2108	8K x 1	16
2116	16K x 1	16
*		
Static		
2115/2125	1K x 1	16
2102A	1K x 1	16
2114	1K x 4	18
5101	256 x 4	22
*		
CCD		
2416	16K x 1	18
*		

*New Devices Added When Available.

7

Add-On Memory

ADD-ON/ADD-IN MEMORIES

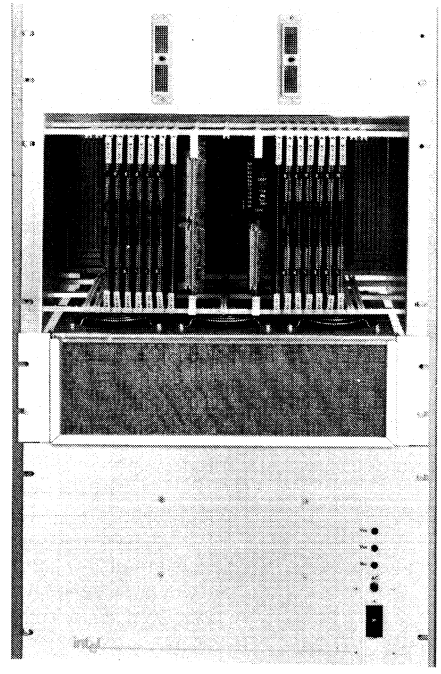
INTRODUCTION

Intel Memory Systems provides a number of memories for popular computers. To best fit specific applications, both add-in and add-on memory systems are available. Because Intel is the largest independent manufacturer of semiconductor memory, we provide low cost and fast delivery.

TABLE OF CONTENTS

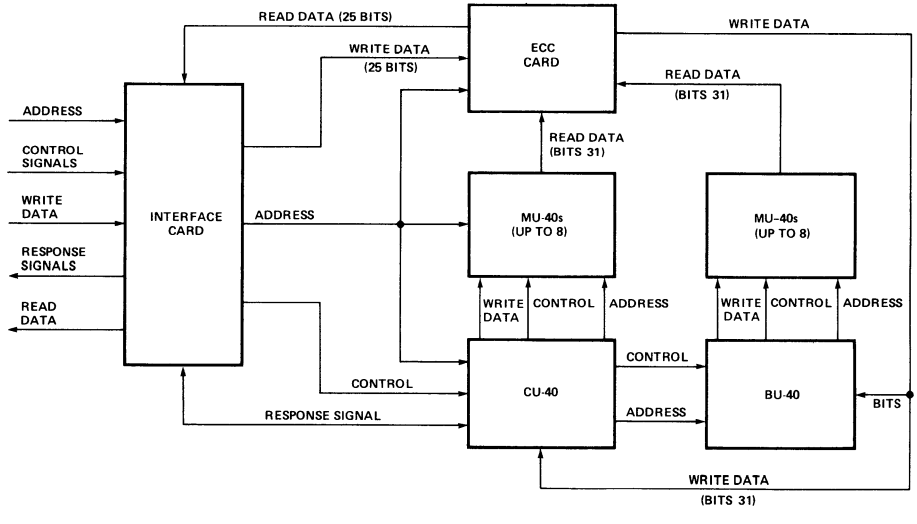
in-400
INTEL ADD-ON MEMORY SYSTEM FOR THE HONEYWELL/GE 400 COMPUTER SYSTEM
CAPACITY: 32K to 128K Words Per System

The Intel® in-400 Semiconductor Memory System is designed to upgrade or replace the present core memory technology used in the Honeywell/General Electric GE-400 Computer. A single processor system (in-400SP) is available and a dual processor system (in-400DP) is planned. The system includes error detection, correction and logging circuits which enhance the system reliability. The Intel standard in-42 Series Memory boards are used as the basic memory modules in the in-400 Memory System.



Features:

- Single Bit Error Correction
- Double Bit Error Detection
- Error Correction Inhibit
- Error Log Feature (stores first bit on each memory device)
- Error Log Interrogation does not interrupt System Operation
- Manual Control of Error Log
- Operationally Compatible with standard GE/HONEYWELL 400 memory interface
- 128K x 25 with power and cooling mounts easily in single GE/HONEYWELL door
- Less than 4.0 Amps at 115V
- Fully simulates core operation



SYSTEM BLOCK DIAGRAM

Product Characteristics

Capacity:	32K words to 128K words
Word Length:	24 data bits, 1 parity bit and 6 ECC bits Notes: 1. ECC bits are transparent to the user. 2. The 24 data and 1 parity bit are treated as one 25-bit data word by the ECC circuits
Speed:	Compatible with GE-400 computer. (Note: Combination of faster memory and asynchronous interface increases computer throughput 10 to 15%)
Interface:	Functionally compatible with the GE-400 computer, but requires different mating connectors
Power:	500 watts for 128K words. This compares to 8,000 watts for the equivalent 128K of core memory.
Size:	3 cubic feet for 128K words. This compares to 200 cubic feet for an equivalent 128K of core memory
Weight:	100 pounds for 128K words. This compares to 2600 pounds for 128K of core memory
Floor Space:	None required if mounted in the host processor.
Configuration:	The system utilizes the Intel standard in-40 series board set. A 128K word system utilizes the following card types: 1. MU-40 16 each 2. CU-40 1 each 3. BU-40 1 each 4. ECC and error logger card 1 each 5. I/O card 1 each

ADD-ON MEMORY

Error Correction Code (ECC)

By incorporating error detection and correction, the in-400 provides significant improvements in system reliability. The ECC provides single-bit correct and double-bit detect capability. All single-bit errors are transparent to the user. Error information is stored in a static RAM included in the error logger card. During preventive maintenance periods, this information can be manually displayed and decoded to point to a specific failed memory component. The net result of the ECC is an improvement in system reliability (MTBF) of 15 to 100 times.

Dual Port Option

The dual-processor system will incorporate dual-port logic which will accomplish the following basic tasks:

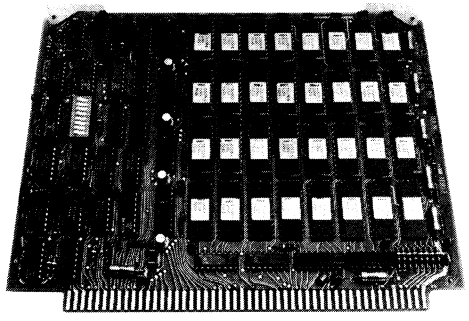
1. Establish priority in the event both ports attempt to access the same 16K address boundaries. Since this is a dynamic memory, refresh will be given the first of three priorities.
2. Allows both ports to cycle the memory simultaneously within different 16K boundaries.
3. Steer data and control signals allowing either port access to any 16K module.

in-481

INTEL ADD-IN MEMORY MODULE FOR INTEL® 8008 AND 8080 BASED MICROCOMPUTER SYSTEMS

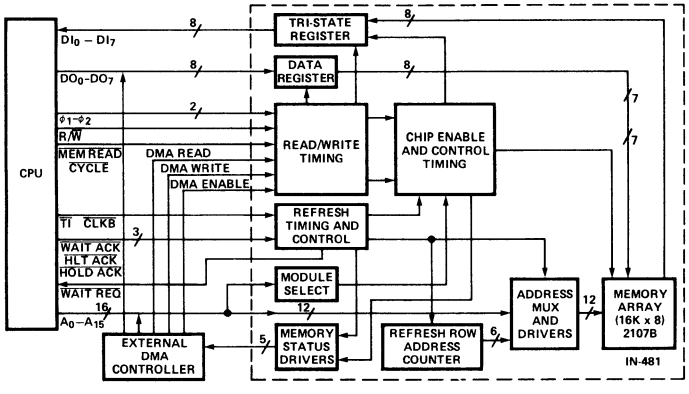
CAPACITY: 16K x 8 Per Module

The in-481 is a 16K x 8 Random Access Memory that utilizes the Intel® 2107B 4K Dynamic RAM Component. The memory and all refresh and control circuitry are on one PC board. The in-481 is expandable to a maximum of 64K x 8 by the use of four memory cards. The in-481 card is designed to interface directly with the Intel® IMM8-82 and the IMM8-83 CPU cards. Since the characteristics of these two cards are governed by either the 8008 or the 8080 microprocessors, it is also possible to use the in-481 with any CPU using these devices. The physical size of the in-481 is the same as the IMM Series. The address, data I/O, and power pin-outs are the same as the Intel IMM6-28, 4K x 8 Memory.



Features:

- IMM8-82 and IMM8-83 Compatible
- Automatic Refresh
- Modular Expandability
- Module Interchangeability
- High Density
- Board Select
- On Board 4K Address Select
- On Board 4K Enable/ Disable
- Input and output Data Registers
- Low Standby Power



ADD-ON MEMORY

Interface Connector Pin Assignments

PIN NO.	8008	8080
1		
2		
3	GND	GND
4	GND	GND
5	WAIT ACK	WAIT ACK
6	TI	CLK 8
7	DMA READ	DMA READ
8	PWR RESET	PWR RESET
9	*WE	*WE
10	NC	φ2
11	MAD 0	MAD 0
12	MAD 1	MAD 1
13	MAD 2	MAD 2
14	MAD 3	MAD 3
15	MAD 4	MAD 4
16	MAD 5	MAD 5
17	MAD 6	MAD 6
18	MAD 7	MAD 7
19	MAD 8	MAD 8
20	MAD 9	MAD 9
21	WAIT REQ	WAIT REQ
22		
23	MDI 0	MDI 0
24	DB 0	DB 0
25	MDI 1	MDI 1
26	DB 1	DB 1
27	MDI 3	MDI 3
28	DB 3	DB 3
29	MDI 2	MDI 2
30	DB 2	DB 2
31	MDI 5	MDI 5
32	DB 5	DB 5
33	MDI 4	MDI 4
34	DB 4	DB 4

PIN NO.	8008	8080
35	MDI 7	MDI 7
36	DB7	DB7
37	MDI 6	MDI 6
38	DB 6	DB 6
39	SYS ENC	SYS ENC
40		
41	ADD ENA	ADD ENA
42	ADD ENB	ADD ENB
43	–9V	–9V
44	–9V	–9V
45	DMA READ ENABLE	DMA READ ENABLE
46	HOLD ACK	HOLD ACK
47		
48		
49	+12V	+12V
50	+12V	+12V
51		
52		
53		
54		
55		
56		
57		
58		
59	MAD 13	MAD 13
60	MAD 12	MAD 12
61		
62		
63	MA 14	MA 14
64		
65	MAD 15	MAD 15
66	MAD 14	MAD 14
67	DB IN	MEM READ CYC
68	MA 15	MA 15
69		

PIN NO.	8008	8080
70		
71	*READ	*READ
72		
73	HALT ACK	HALT ACK
74	SYNCA	DMA φ2 DISABLE
75		
76		
77		
78		
79		
80		
81		
82		
83		
84		
85	*REF	*REF
86		
87	*BUSY	*BUSY
88	*ENREF	*ENREF
89		
90		
91	GND	GND
92	GND	GND
93		
94	MAD 11	MAD 11
95	R/W	R/W
96	MAD 10	MAD 10
97		
98	φ1	φ1
99	+5	+5
100	+5	+5

*Status signals from in-481.

Product Characteristics

Capacity:	16K x 8 expandable to 64K x 8 by use of four memory cards
Cycle Time:	
in-481	1100 nanoseconds
in-481-1	600 nanoseconds
Access Time:	
in-481	650 nanoseconds
in-481-1	450 nanoseconds
Power:	
+5V	1.0A
+12V	0.25A
* -9V	30 mA

*(-9V is zenered to -5V; optional -5VDC at 5 mA)

Operational Modes:	Read (NDRO) Write
Dimensions:	8.00 inches High 6.18 inches Deep 0.5 inch mounting centers
Temperature:	0°C to +50°C operating ambient -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating
Connector Type:	
Amp	1-67878-0
Winchester	HW50D0111
Viking	3VH50/ICN5
Sylvania	7900-0281-X

ADD-ON MEMORY

*Applications

8008

When using the in-481 in an 8008 or 8008-1 microprocessor based system, the access and cycle times are such that WAIT states need not be entered. All refresh, write and read cycle requests are synchronized to specific CPU states and requests. This means that the in-481 is totally transparent to the CPU.

During normal CPU operation all refreshing is done during the T_1 state of the 8008; during a HALT or HOLD state the memory refresh is synchronized to the ϕ_1 clock and occurs every 7.5 µsec. It should be noted that a power-up reset circuit initializes all control circuitry on the in-481.

8080

When using the in-481 in an 8080A microprocessor based system, the memory components used are faster in both cycle and access times in order to minimize the total number of WAIT cycle requests. All refresh, read and write cycle requests are again synchronized to specific CPU states or requests. Because of the 2.0 µsec instruction cycle time of the 8080, a single WAIT state or a possible double WAIT state is required during memory refresh. A memory refresh is initiated once every 31 µsec and it is synchronized to the positive edge of SYNC during the T_1 state. Normally a single WAIT state between T_2 and T_3 states is required if the memory is in the process of performing a read operation. If, however, a write cycle had been initiated during T_3 of the previous subcycle a double WAIT state is requested by the in-481. During the HOLD and HALT states, the refresh requests are synchronized to the ϕ_1 clock and they occur with a period of 25 µsec. It should be noted again that the power-up reset circuit initializes all control circuitry.

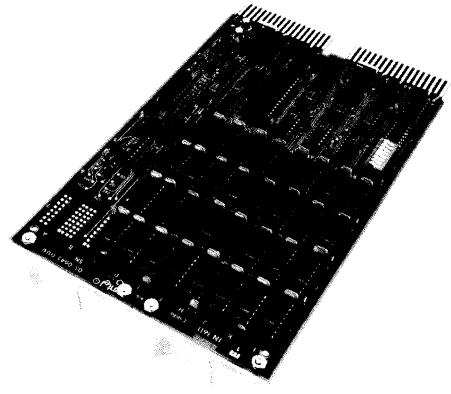
DMA

A DMA option is made possible in both 8008 and 8080 systems by means of the HOLD features. The HOLD ACK signal in both the IMM8-82 and IMM8-83 frees the control lines of the in-481 and the in-481-1. This signal is also used by the in-481 to disable the MEM READ CYCLE control input thereby enabling DMA control of the memory. Since refresh is synchronized to the ϕ_1 clock, and since additional state lines are brought out from the in-481, an access control circuit can be implemented to perform DMA. After completion of DMA, the HOLD and WAIT requests to the CPU card are disabled, and memory operation proceeds as normal.

*While the in-481 and in-481-1 are designed to work with the IMM8-82 and IMM8-83, they are not intended for use in the INTELLEC® 8/MOD8 or INTELLEC® 8/MOD80 since the current requirements of the in-481 and in-481-1 exceed the 60 mA capacity of the INTELLEC® +12V power supply.

in-1611
INTEL ADD-IN MEMORY SYSTEM FOR THE DEC LSI-11 AND PDP-11/03 MINICOMPUTER FAMILY
CAPACITY: 8K, 16K, or 24K Words Per Card

The Intel® in-1611 MOS Dynamic RAM Semiconductor Memory Card has capacity of 8K, 16K, or 24K words with 16 bits/word. The card is compatible with the DEC® LSI-11 and PDP-11/03 microcomputers.



Features:
- Double Connector Width (i.e., "2-wide" card)
- Requires only one backplane position
- Highest density available
- Address selection
- Low power requirement
- Totally compatible with LSI-11 hardware and software

General
The Intel® in-1611 is designed for use in the LSI-11 (PDP-11/03) microcomputer. The system is compatible with the LSI-11 bus and consists of a single "2-wide" PC card. This saves valuable chassis positions since the in-1611 is one half the size of the standard "quad-wide" card.

The memory card has a capacity of 8K, 16K or 24K 16-bit words. An on-card DIP switch allows the card to be positioned on any 4K boundary. Any 4K block within the card's address space can be disabled allowing the card to work in conjunction with a PROM/ROM memory board.

Power Interface

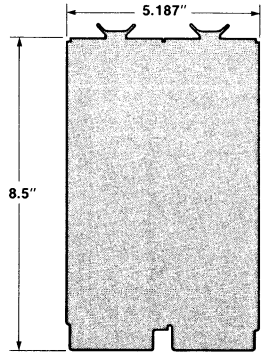
Item	Signal	DEC Pin		
1	+5V V_{CC}	AA2 BA2 BV1		
2	+12V V_{DD}	AD2 BD2		
3	GND V_{SS}	AC2 AJ1 AM1	AT1 BC2 BJ1	BM1 BT1

Interface Pin Assignments

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
AA2	+5 (V_{CC})	AA1		BA2	+5 (V_{CC})	BA1	
AB2		AB1		BB2		BB1	
AC2	GND	AC1		BC2	GND	BC1	
AD2	+12 (V_{DD})	AD1		BD2	+12 (V_{DD})	BD1	
AE2	BDOUT L (write sync)	AE1		BE2	BDAL 2 L	BE1	
AF2	BRPLY L (slave reply)	AF1		BF2	BDAL 3 L	BF1	
AH2	BDIN L (Read sync)	AH1		BH2	BDAL 4 L	BH1	
AJ2	BSYNC L (adr sync)	AJ1	GND	BJ2	BDAL 5 L	BJ1	GND
AK2	BWTBT L (byte select)	AK1		BK2	BDAL 6 L	BK1	
AL2		AL1		BL2	BDAL 7 L	BL1	
AM2	BIAK1 L	AM1	GND	BM2	BDAL 8 L	BM1	GND
AN2	BIAK0 L	AN1		BN2	BDAL 9 L	BN1	
AP2		AP1		BP2	BDAL 10 L	BP1	
AR2	BDMG1 L	AR1	BREF L (Refresh Control)	BR2	BDAL 11 L	BR1	
AS2	BDMG0 L	AS1		BS2	BDAL 12 L	BS1	
AT2		AT1	GND	BT2	BDAL 13 L	BT1	GND
AU2	BDAL 0 L	AU1		BU2	BDAL 14 L	BU1	
AV2	BDAL 1 L	AV1		BV2	BDAL 15 L	BV1	+5V (V_{CC})

Product Characteristics

Storage Capacity:	8K, 16K or 24K per card
Word Length:	16-bits per memory card
Read Access Time:	400 nanoseconds
Write Access Time:	200 nanoseconds
Cycle Time:	Compatible with LSI-11 bus
Retention Time:	2 ms
Modes of Operation:	Read Word Write Word Write Byte Read (word) modify write (byte or word)
Input/Output:	TTL compatible
Data Input:	16 lines (Single-ended)
Data Output:	16 lines (Single-ended)
Input Controls:	5 lines, BDIN L, BSYNC L, BWTBT L, BDOUT L, BREF L (Single-ended)
Address Input:	16 lines, binary, (Single-ended) multiplexed with data bus
Output Controls:	1 line, BRPLY L
Temperature:	0°C to 50°C operating ambient, 40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating.
Input Power:	+5.0V +5% at 1.0 Amps +12V +5% at 0.6 Amps
Power Dissipation:	12.2 Operating 6.8 Standby
Weight:	1 lb.
Dimensions:	Each card requires an LSI-11 "2-wide" slot and a depth of .375".



Other Intel DEC Compatible Memories:
in-4711—PDP-11 Add-In
in-4011—PDP-11 Add-On
in-1670—PDP-11/70 Add-On

Memory Operation

The memory card is capable of operating in the following modes: Read (Non-Destructive), Write, and Read Modify Write.

Read

A Read Cycle is begun when the DBIN signal is asserted. The contents of the memory location will not be altered.

Write

A write cycle is begun when the DBOUT signal is asserted. If it is to be a byte write only the BWTBT signal is asserted during DBOUT. The upper byte is specified when A0 = 1, the lower when A0 = 0.

Read Modify Write

A read modify write cycle occurs when the processor following a read cycle but before BSYNC is cleared, asserts BDOUT. Upper or lower bytes for byte writes are specified by A0 as in a write cycle (see above).

Refresh

Since data is stored in dynamic memory devices (2116, 2108) it must be periodically refreshed. This refresh is performed automatically every 1.6 milliseconds by micro-code on the microcomputer module.

Input Requirements

Address, Data Inputs:	The address and data signals are time multiplexed on a single 16 line bus
Input Controls:	5 lines, (Single-ended) BDIN L, BSYNC L, BDOUT L, BREF L
Input Logic Levels:	Low = -1.0 to +0.7V @ 2 mA High = +2.5 to +5.5 @100 μA

Output Specifications

Data Output:	16 lines (Single-ended), time multiplexed with address
Output Controls:	1 line (Single-ended), BRPLY L
Output Logic Levels:	Low = -0.5 to +0.7V @ 2 mA High = Open Collector

Power Requirements, Maximum

	V_{CC}	V_{DD}
Voltage	+4.75 to 5.25	11.4 to 12.6
Amps/Selected Card	0.7A	1.0A
Amps/Standby Card	0.7A	0.2A

in-1670
INTEL ADD-ON MEMORY SYSTEM FOR THE DEC PDP-11/70 COMPUTER SYSTEM
CAPACITY: 128 Bytes to 1024 Bytes Per Memory Module

The Intel® in-1670 is a monolithic memory system for the DEC PDP-11/70. All components are engineered to meet or exceed the specifications of similar DEC components. The Intel® in-1670 is used in the PDP-11/70 computer systems. It is a direct replacement for the memory module (MJ-11) supplied by DEC. The in-1670 uses the identical interface signals (control, address, data) and cables as the DEC memory module. The only power required is 115V AC or 230V AC.

The in-1670 is fully hardware and software compatible with the DEC CPU and provides for upgrades from 128K bytes to 4 megabytes of total storage. The in-1670 is installed in the CPU memory cabinet.

No software changes are necessary to the operating system or application program. No changes are made to the CPU and no modifications are required to the memory bus or I/O structure.

A fully expanded in-1670 memory module contains 1024K bytes. Each memory module may be interleaved with any other memory module of equal capacity.

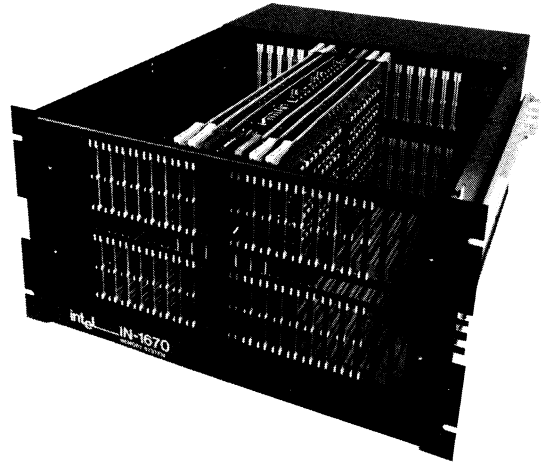
The unit is easily field upgradable to larger capacities by the simple addition of the memory cards or a memory rack containing cards. Since one memory rack contains four times the memory in the same space required by PDP-11/70 memory, the in-1670 eliminates the bus cable length limitations and allows the user access to the full 3,932,160 byte address space.

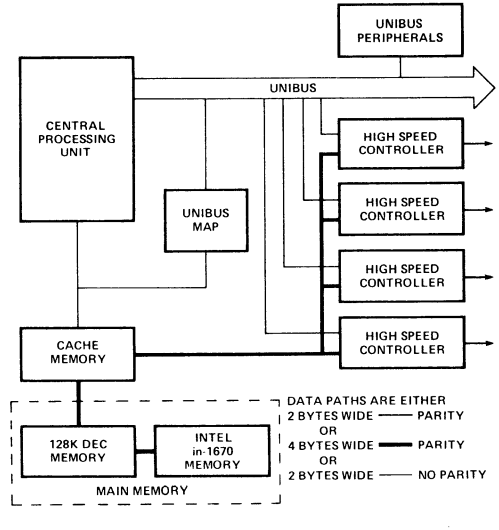
Features:

- Starting address of memory module is selected by setting of DIP switches
- Two-way interleaving between identical size memory modules
- Each memory module contains its own power supply and cooling
- Higher memory density of the in-1670 over the DEC memory module reduces cabinet space and power requirements
- Compatible with computer manufacturer supplied memory management unit
- PDP-11/70 memory may be incremented to 4 megabytes using in-1670 memory modules
- Single bit error correction and double bit error detection
- Compatible cycle times to DEC memory
- User access to the full PDP-11/70 address space at 3,932,160 bytes

The in-1670 memory system consists of MOS semiconductor memory modules that are byte addressable and expandable in 128K byte increments.

During data transfer each byte has one parity bit associated with it. Data is stored with additional error correction check bits which will detect and correct single bit errors and detect double bit errors.





SYSTEM BLOCK DIAGRAM

Product Characteristics

Storage Capacity:	128K, 256K, 512K and 1024K bytes
Word Length:	32-bits (4 bytes) per memory word plus 8-bits of parity check
Average Cycle Time:	790 nanoseconds
Access Time: (Data Ready)	585 nanoseconds
Partial Write Time: (1 or 2 bytes)	950 nanoseconds
Mode of Operation:	Write Read Partial Write (1 or 2 bytes)
Input/Output:	TTL Compatible
Address Input:	23 lines, binary, (Single-ended)
Data Input:	Up to 36 lines, bi-directional
Data Output:	Up to 36 lines, bi-directional
Temperature:	0°C to +50°C operating ambient -40°C to +85°C non-operating
Relative Humidity:	10% to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating
Input Power:	95V AC to 135V AC or 180V AC to 260V AC at 45 to 63 Hz single phase, 690VA (max per memory module)
Dimensions:	Each memory module is 17.12"W x 10.50"H x 25.00"D
Weight:	⩽ 70 pounds

ADD-ON MEMORY

Memory Operation

The memory module is capable of operating in the following modes: Read (Non-Destructive), Write, and Partial Write (1 or 2 bytes).

Read

Read cycles are determined by the status of MAIN C control lines. With both control lines high, (the data stored previously at the address specified by the address inputs will be transferred to the output bus.

Write and Partial Write

Write cycles are determined by the status of the MAIN C control lines. With the C1 control line low, the data on the input bus will be written into the address specified by the address inputs. One, two or four bytes (8 data bits) may be written into the memory word without disturbing the adjacent data bytes. A partial write is the writing of one or two bytes.

Refresh

Since data is stored in dynamic memory devices, it must be periodically refreshed. This is accomplished automatically by the in-1670 system and is transparent to PDP-11/70.

Error Correction Code (ECC)

The Intel® in-1670 memory system includes Error Correction Coding (ECC) as a standard feature. The ECC logic detects single bit memory errors and automatically corrects a single bit failure during a READ operation. Since most memory errors are due to single bit failures, ECC provides a 10 to 25 times improvement in memory system reliability over systems with parity checking only. A double bit error in the READ word will not be corrected. For double bit errors, parity bits sent to the CPU will be forced to the error state. This allows the CPU to process double bit errors as a parity error. An error log records the bit location of single bit errors in 2K memory segments. The address location of any double or multiple bit error is recorded in a 32 position error log register. This system is used to diagnose and correct potential failures during preventive maintenance.

Maintainability Features

The in-1670 memory system provides convenient controls, reconfiguration switches, and status indicator as standard maintainability features.

The following controls are located on the rear panel of the memory module:

- AC circuit breaker.
- Three power supply output voltage adjustments.

The following controls are located on the control card or error logger card:

- Address select switches to set the starting address for the memory bank.
- Memory on-line/off-line switch to disconnect the in-1670 from the PDP-11/70 memory bus.
- Reset logic switch.
- Error logger on/off switch.
- Lamp test.
- ECC on/off switch.
- Error logger scan switch.

The following indicators are provided on the control card or error logger card:

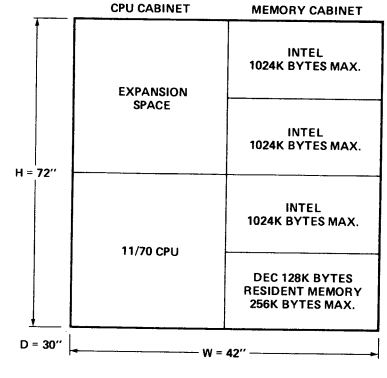
- Address parity error indicator.
- Mismatch error indicator.
- Write data parity error indicator.
- Address display.
- Syndrome bits display.
- Single bit mode or double bit mode indicator.
- On-line/off-line mode indicator.

Installation Requirements

- All cables and connectors supplied by Intel.
- 1 DEC Memory Cabinet (21"W x 30"D x 72"H).
- 1 in-1670 Memory Module.

Notes:

1. Installation can be done by the customer or purchased from Intel.
2. Maintenance contracts are available from Intel.



in-4011
INTEL ADD-ON MEMORY SYSTEM FOR THE DEC PDP-11 MINICOMPUTER FAMILY
CAPACITY: 32K to 128K Words Per 7" High Chassis

The Intel® in-4011 semiconductor memory system for the PDP-11 is configured from standard memory cards designed around a 4096 x 1 NMOS Dynamic RAM. Each memory card provides storage for 16K words at PDP-11 main memory. The in-4011 can be configured with up to eight memory cards for a total capacity of 128K words.

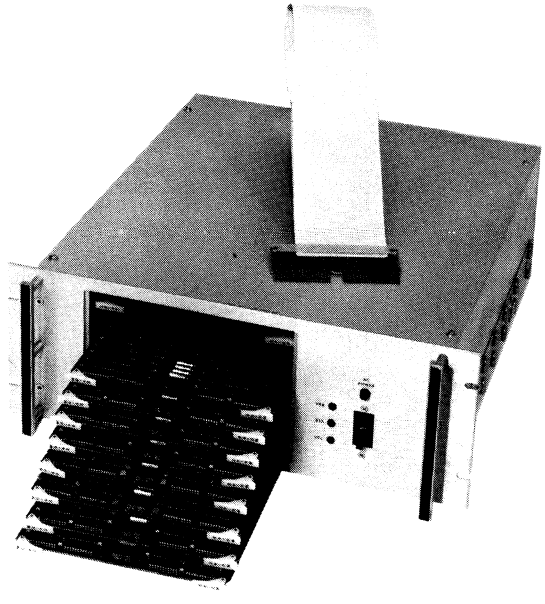
The in-4011 is totally hardware and software compatible with the PDP-11 system. No hardware modifications to the computer system, no wiring changes to the in-4011, and no equipment not already a part of the standard in-4011 system are required to install and operate the memory system with the PDP-11 computer.

The in-4011 system includes parity generation and checking. Control signals include parity error detect and DC voltage low detect. The interface card and cable are Unibus-compatible.

The in-4011 memory card is a field-proven memory design with 3,000 installed memory modules. The system features 100% burn-in of all memory cards. This field-proven design, complete system test and burn-in, and the extended warranty on all systems, assure each in-4011 user of a successful and reliable PDP-11 memory system.

Features:

- Low Cost Memory
- High Reliability
- High Density
- Total Hardware and Software Compatibility
- Integral Parity Registers
- Field Proven
- Field Expandable Up to 128K x 18



ADD-ON MEMORY

Other Intel DEC Compatible Memories:
in-1611—LSI-11 and PDP-11/03
in-4711—PDP-11 Add-In
in-1670—PDP-11/70 Add-On

Product Characteristics

Storage Capacity:	32,768 words, expandable to 128K words in 16K increments
Word Length:	16-bits per memory word
Check Bits:	2 parity bits per memory word
Cycle Time:	650 nanoseconds
Access Time:	500 nanoseconds
Modes of Operation:	WRITE READ
Input/Output:	TTL Compatible
Address Input:	18 lines, binary, (Single-ended)
Data Input/Output:	16 lines, bi-directional (Single-ended)
Input Controls:	3 lines, (Single-ended)
Output Controls:	1 line, (Single-ended)
Temperature:	0°C +50°C operating ambient, -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating. Up to 50,000 feet non-operating
Interface:	TTL levels all inputs and outputs ("UNIBUS" compatible with 1 bus load)
Dimensions:	7.0 inches High 19.0 inches Wide 17.0 inches Deep
Weight:	Less than 70 lbs.

in-4711
INTEL ADD-IN MEMORY SYSTEM FOR THE DEC PDP-11 MINICOMPUTER FAMILY
CAPACITY: 8K or 16K Words Per Card

The Intel® in-4711 is a 16K x 16-bit add-in replacement memory designed for use in all models of the DEC PDP-11 computer family. The in-4711 is both hardware and software compatible with the PDP-11 system. No modifications are required for installation. It utilizes the Intel® 2107B 4K dynamic RAM component. The 16K word memory with optional parity bits and control circuitry are contained on a single PC card.

Features:

- Low Cost Memory
- Fast Cycle Time
- Low Power Requirements
- High Reliability
- Module Interchangeability
- Modular Expandability
- Compact Size
- Byte Operation
- Address Select Switches
- Two Way Interleave (16K Boundaries)
- Compatible with Both DEC PDP-11 Memory Management and Byte Parity Options

Read and write cycle times of 620 nanoseconds allow significant speed improvement. Interleave operation with two memories is possible for maximum throughput.

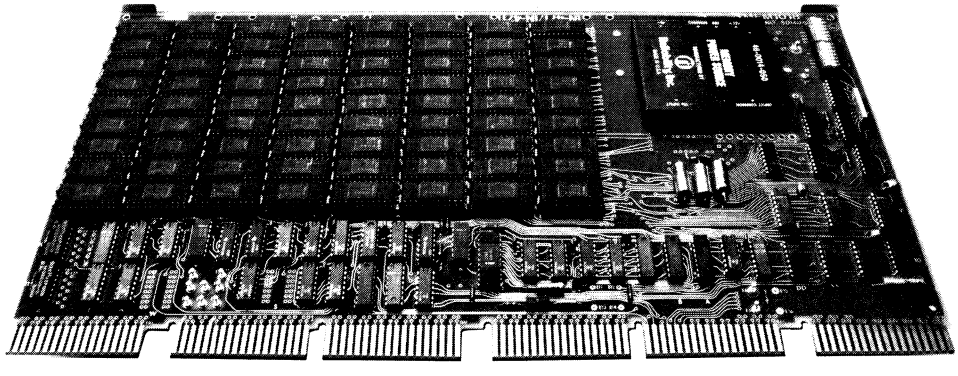
Quick address select changes are possible through the use of on-board DIP switches. Also, byte operation is standard.

in-4711 Add-In Compatibility

The in-4711 may be installed into any of the three different types of PDP-11 systems:

- Any PDP-11/05, 11/10, 11/15, 11/35, 11/40, 11/45, 11/50 and 11/55 with an MF11-L or MF11-LP backpanel.
- Any PDP-11/04, 11/34 with semiconductor memory supplied by DEC.
- Any PDP-11/04, 11/34 with core memory supplied by DEC.

The in-4711 may not be installed into any PDP-11/05, 11/10, 11/15, 11/20, 11/35, 11/40, 11/45, 11/50 or 11/55 with an MF11-U or MF11-UP backpanel. For these systems, an in-4011 Add-On Memory System should be used to expand the PDP-11 memory.



Product Characteristics

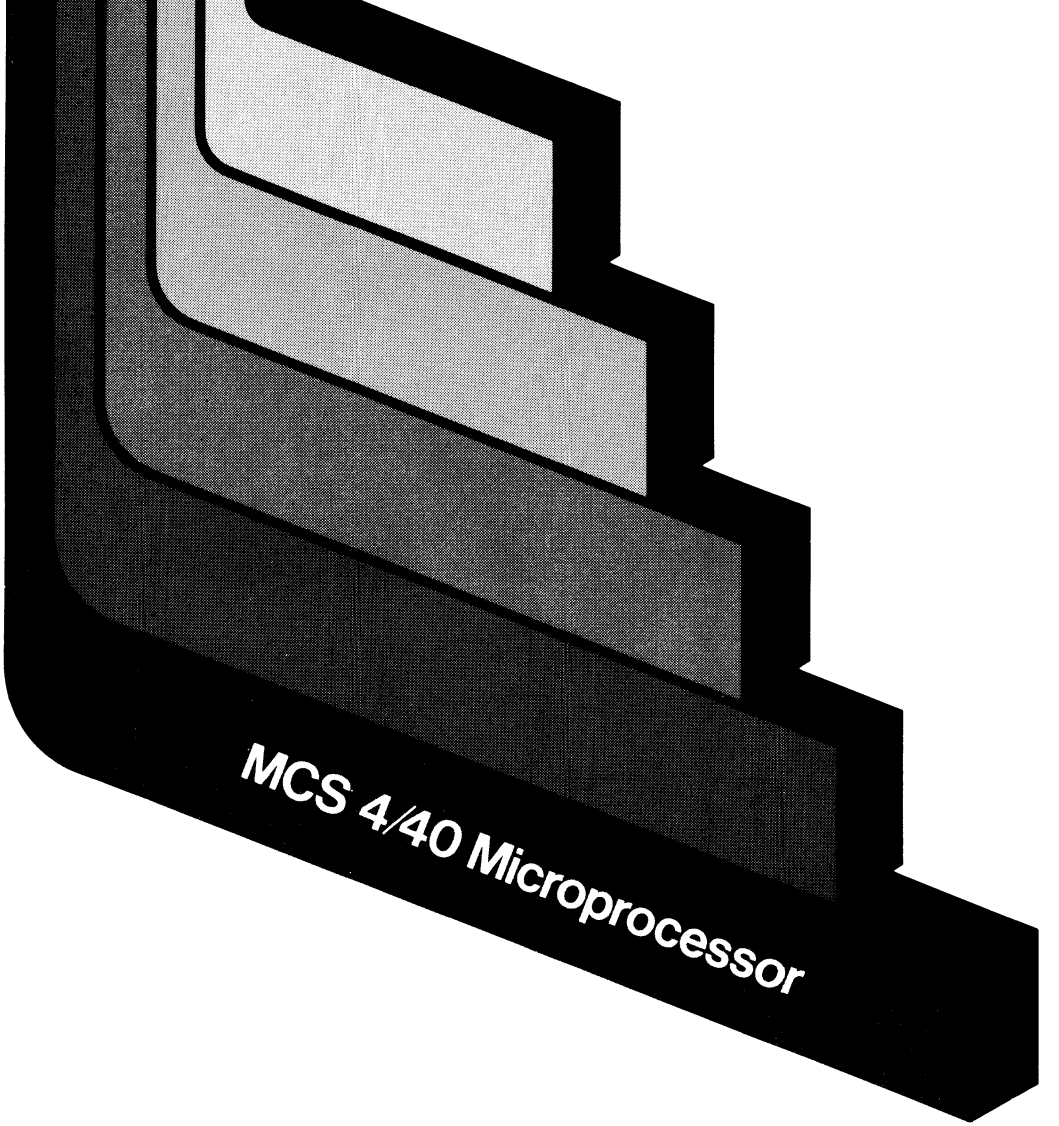
Capacity:	8K* and 16K words per board
Word Length:	16-bits
Cycle Time:	
Read	620 nanoseconds
Write	620 nanoseconds
Access Time:	
Read	450 nanoseconds
Write	250 nanoseconds
Dimensions:	
Memory Board (Hex):	15.4 inches High 8.5 inches Deep 0.375 inches Wide
Operational Modes:	Read Word Write Word Read Byte Write Byte
Interface Characteristics:	Unibus Compatible
TTL Compatible Logic Standard Input Controls:	Cycle Initiate (MSYN) Byte Select (CO) Read/Write (CI) Address Lines (A0-A17) Data Lines (D0-D15) Slave Sync (SSYN)

D.C. Power Requirements:	16.5 Watts Typ. 26.0 Watts Max.
Temperature:	0°C to +50°C operating ambient -40°C to +125°C non-operating
Relative Humidity:	Up to 90% with no condensation
Altitude:	0 to 10,000 feet operating Up to 50,000 feet non-operating

*Note: 8K available only for orders of 25 units or more.

ADD-ON MEMORY

Other Intel DEC Compatible Memories:
in-1611—LSI-11 and PDP-11/03
in-4011—PDP-11 Add-On
in-1670—PDP-11/70 Add-On


MCS 4/40 Microprocessor

MCS-40® MICROCOMPUTER SYSTEM

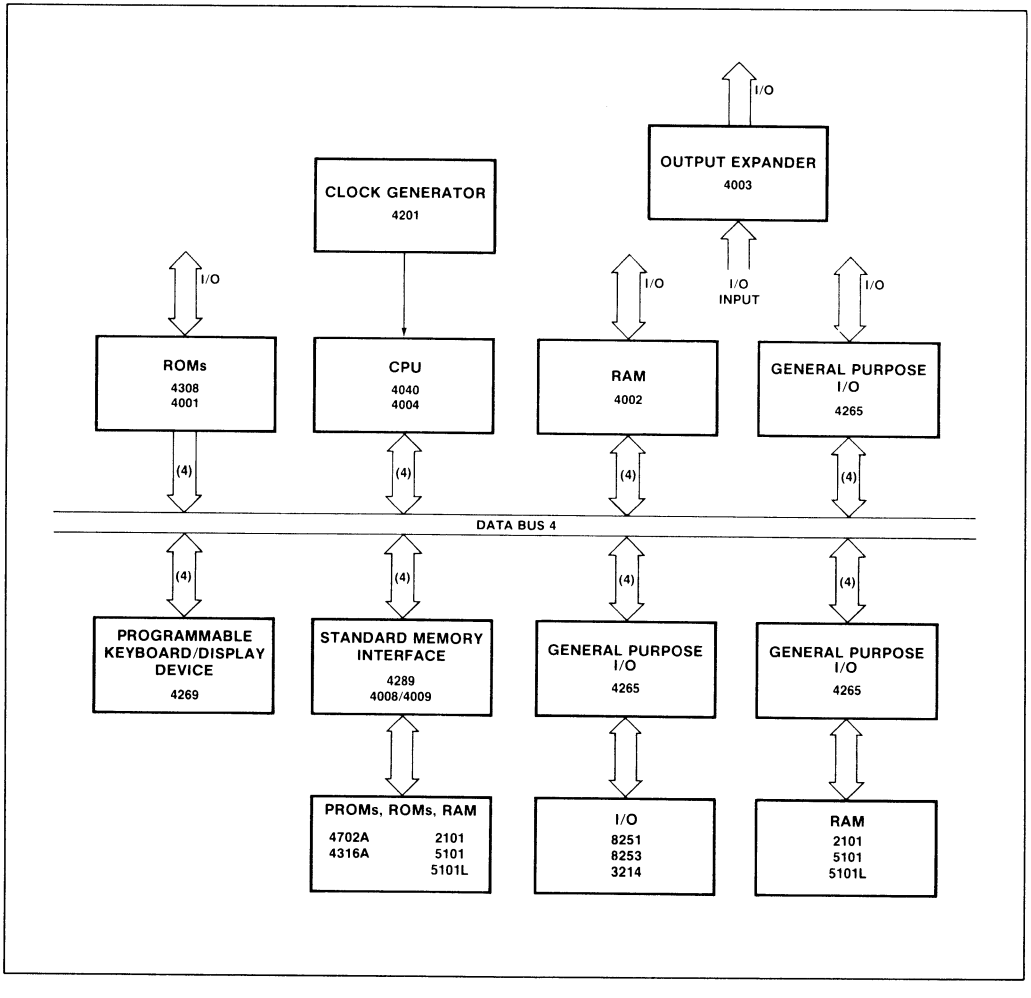
TABLE OF CONTENTS

INTRODUCTION

The MCS-40 microcomputer family (the expanded MCS-4 family) is the world's largest selling family of microcomputers. This family of components has been in use for a wide variety of computer and control applications since 1971. The MCS-40 is a system which provides its users with an advanced generation of components geared for random logic replacement and all designs which require the unique advantage of a general purpose computer. The MCS-40 comes with a comprehensive product development program consisting of hardware and software development aids and a large network of regional application engineers to draw upon.

The 4004 and 4040 are complete 4-bit parallel central processing units (CPUs). The 4040 has a complete instruction set of 60 instructions, including Arithmetic, Interrupt, Logical Operations, I/O instructions, Register Instructions, ROM Bank Switching, Register Bank Switching, Interrupt Disable and Enable. The 4004 has a total of 46 instructions all of which are part of the 4040 instruction set and are mutually compatible.

MCS-40™ SYSTEM



4040

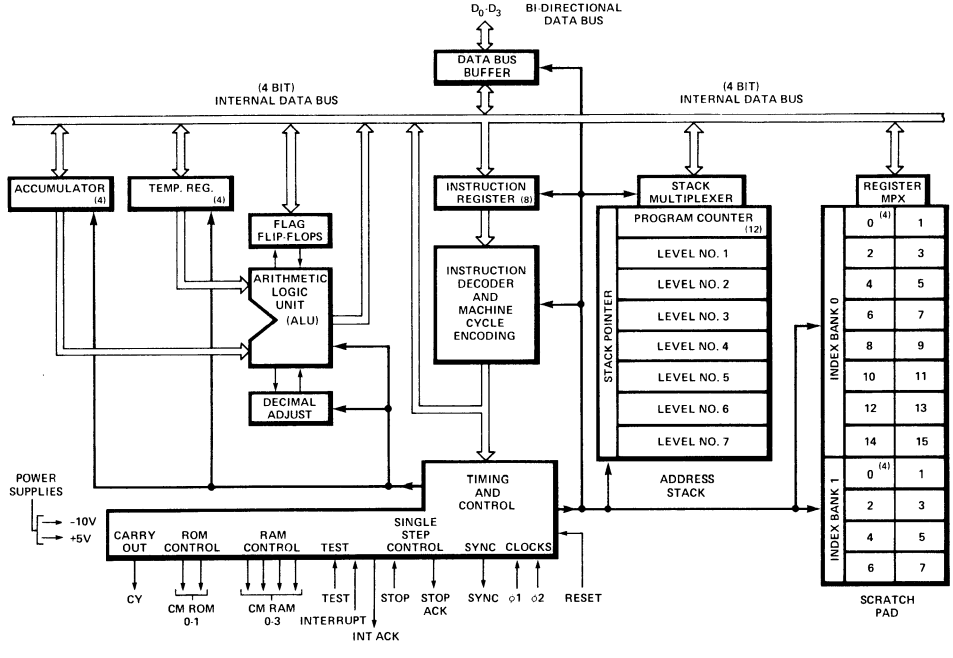
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- **Functionally and Electrically Upward Compatible to 4004 CPU**
- **14 Additional Instructions (60 total) Including Logical Operations and Read Program Memory**
- **Interrupt Capability**
- **Single Step Operation**
- **8K Byte Memory Addressing Capability**
- **24 Index Registers**
- **Subroutine Nesting to 7 Levels**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

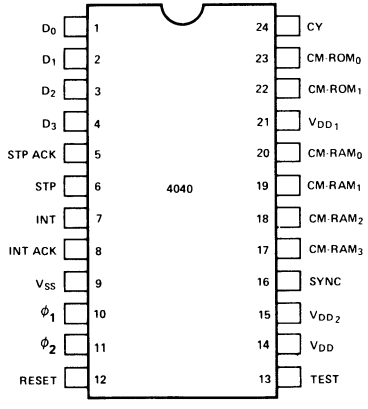
The Intel® 4040 is a complete 4-bit parallel central processing unit (CPU). The CPU can directly address 4K eight bit instruction words or 8K with a bank switch. Seven levels of subroutine nesting, including interrupt, and 24 randomly accessable index registers (24x4) are provided as convenient facilities for the designer. The index registers may be used for addressing or for scratch pad memory for storing computation results. The interrupt feature permits a normal program sequence to be interrupted, with normal program execution continuing after the interrupt service routine is completed. Provisions have also been made to permit single-stepping the CPU using the STOP and ACKNOWLEDGE signals.

The 4040 is an enhanced version of the 4004 and as such retains all the functional capability of that device. It will execute all the 4004 instructions, and is also electrically compatible with all components used with a 4004 CPU.

BLOCK DIAGRAM



Pin Description



D_0-D_3

BIDIRECTIONAL DATA BUS. All address and data communication between the processor and the RAM and ROM chips occurs on these 4 lines.

STP

STOP input. A logic "1" level on this input causes the processor to enter the STOP mode.

STPA

STOP ACKNOWLEDGE output. This signal is present when the processor is in the stopped state. Output is "open drain" requiring pull-down resistor to V_{DD}.

INT

INTERRUPT input. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.

INTA

INTERRUPT ACKNOWLEDGE output. This signal acknowledges receipt of an INTERRUPT signal and prevents additional INTERRUPTS from entering the processor. It remains active until cleared by the execution of the new BRANCH BACK and SRC (BBS) instruction. The output is "open drain" requiring a pull-down resistor to V_{DD}.

RESET

RESET input. A logic "1" level at this input clears all flag and status registers and forces the program counter to zero. To completely clear all address and index registers, RESET must be applied for 96 clock cycles (12 machine cycles).

TEST

TEST input. The logical state of this signal may be tested with the JCN instruction.

SYNC

SYNC output. Synchronization signal generated by the processor and sent to ROM and RAM chips. It indicates the beginning of an instruction cycle.

$CM\text{-}RAM_0$ – $CM\text{-}RAM_3$

CM-RAM outputs. These are bank selection signals for the 4002 RAM chips in the system.

$CM\text{-}ROM_0$ – $CM\text{-}ROM_1$

CM-ROM outputs. These are bank selection signals for program ROM chips in the system.

CY

CARRY output. The state of the carry flip-flop is present on this output and updated each X_1 time. Output is "open-drain" requiring pull down resistor to V_{DD}.

ϕ_1, ϕ_2	Two phase clock inputs
V_{SS}	Most positive voltage
V_{DD}	V_{SS}–15V ±5% – Main supply voltage
*V_{DD_1}	V_{SS}–15V ±5% – Timing supply voltage
**V_{DD_2}	– Output buffer supply voltage

*For low power operation
**May vary depending on system interface

Instruction Set Format

A. Machine Instructions

- 1 word instruction – 8-bits requiring 8 clock periods (1 instruction cycle)
- 2 word instruction – 16-bits requiring 16 clock periods (2 instruction cycles)

Each instruction is divided into two 4-bit fields. The upper 4-bits is the OPR field containing the operation code. The lower 4-bits is the OPA field containing the modifier. For two word instructions, the second word contains address information or data.

The upper 4-bits (OPR) will always be fetched before the lower 4-bits (OPA) during M_1 and M_2 times respectively.

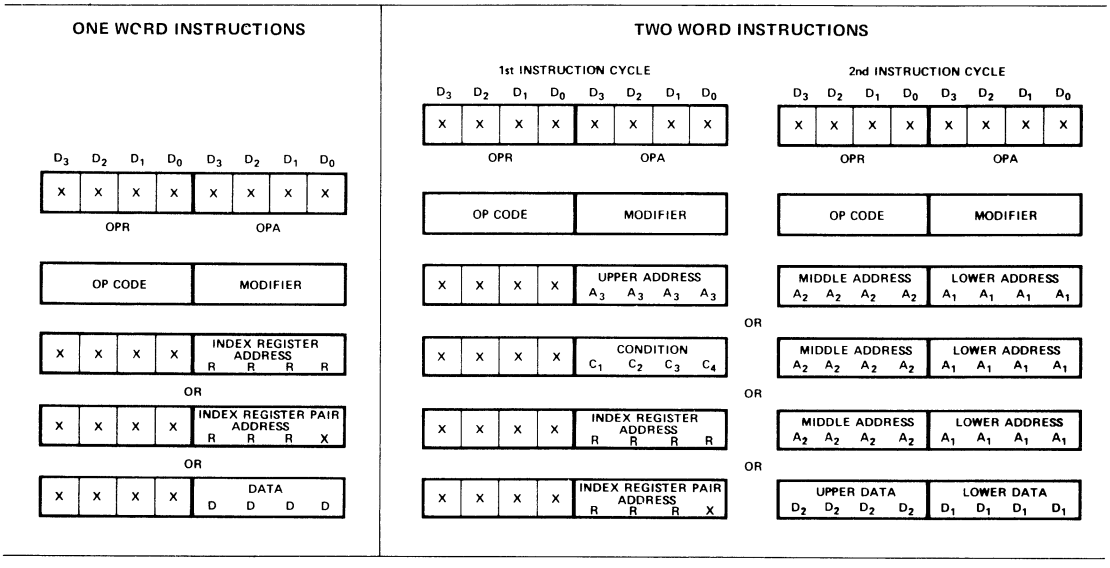


Table I. Machine Instruction Format.

B. Input/Output and RAM Instructions and Accumulator Group Instructions

In these instructions (which are all single word) the OPR contains a 4-bit code which identifies either the I/O instruction or the accumulator group instruction and the OPA contains a 4-bit code which identifies the operation to be performed. Table II illustrates the contents of each 4-bit field.

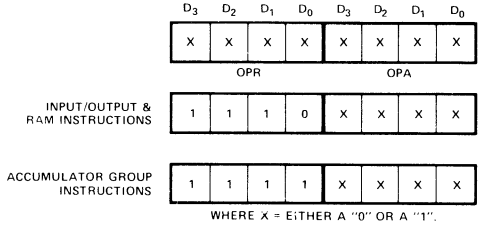


Table II. I/O and Accumulator Group Instruction Formats.

4040 Instruction Set

BASIC INSTRUCTIONS (* = 2 Word Instructions)

Hex Code	MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
00	NOP	0 0 0 0	0 0 0 0	No operation.
1 - -	*JCN	0 0 0 1 $A_2 A_2 A_2 A_2$	$C_1 C_2 C_3 C_4$ $A_1 A_1 A_1 A_1$	Jump to ROM address $A_2 A_2 A_2 A_2$, $A_1 A_1 A_1 A_1$ (within the same ROM that contains this JCN instruction) if condition $C_1 C_2 C_3 C_4$ is true, otherwise go to the next instruction in sequence.
2 - -	*FIM	0 0 1 0 $D_2 D_2 D_2 D_2$	R R R 0 $D_1 D_1 D_1 D_1$	Fetch immediate (direct) from ROM Data $D_2 D_2 D_2 D_2 D_1 D_1 D_1 D_1$ to index register pair location RRR.
3 -	FIN	0 0 1 1	R R R 0	Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR.
3 -	JIN	0 0 1 1	R R R 1	Jump indirect. Send contents of register pair RRR out as an address at A_1 and A_2 time in the instruction cycle.
4 - -	*JUN	0 1 0 0 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump unconditional to ROM address $A_3 A_3 A_3 A_3 A_2 A_2 A_2 A_2$ $A_1 A_1 A_1 A_1$.
5 - -	*JMS	0 1 0 1 $A_2 A_2 A_2 A_2$	$A_3 A_3 A_3 A_3$ $A_1 A_1 A_1 A_1$	Jump to subroutine ROM address $A_3 A_3 A_3 A_3 A_2 A_2 A_2 A_2$ $A_1 A_1 A_1 A_1$, save old address (up 1 level in stack.)
6 -	INC	0 1 1 0	R R R R	Increment contents of register RRRR.
7 - -	*ISZ	0 1 1 1 $A_2 A_2 A_2 A_2$	R R R R $A_1 A_1 A_1 A_1$	Increment contents of register RRRR. Go to ROM address $A_2 A_2 A_2 A_2$ $A_1 A_1 A_1 A_1$ (within the same ROM that contains this ISZ instruction) if result $\neq 0$, otherwise go to the next instruction in sequence.
8 -	ADD	1 0 0 0	R R R R	Add contents of register RRRR to accumulator with carry.
9 -	SUB	1 0 0 1	R R R R	Subtract contents of register RRRR to accumulator with borrow.
A -	LD	1 0 1 0	R R R R	Load contents of register RRRR to accumulator.
B -	XCH	1 0 1 1	R R R R	Exchange contents of index register RRRR and accumulator.
C -	BBL	1 1 0 0	D D D D	Branch back (down 1 level in stack) and load data DDDD to accumulator.
D -	LDM	1 1 0 1	D D D D	Load data DDDD to accumulator.
F0	CLB	1 1 1 1	0 0 0 0	Clear both. (Accumulator and carry)
F1	CLC	1 1 1 1	0 0 0 1	Clear carry.
F2	IAC	1 1 1 1	0 0 1 0	Increment accumulator.
F3	CMC	1 1 1 1	0 0 1 1	Complement carry.
F4	CMA	1 1 1 1	0 1 0 0	Complement accumulator.
F5	RAL	1 1 1 1	0 1 0 1	Rotate left. (Accumulator and carry)
F6	RAR	1 1 1 1	0 1 1 0	Rotate right. (Accumulator and carry)
F7	TCC	1 1 1 1	0 1 1 1	Transmit carry to accumulator and clear carry.
F8	DAC	1 1 1 1	1 0 0 0	Decrement accumulator.
F9	TCS	1 1 1 1	1 0 0 1	Transfer carry subtract and clear carry.
FA	STC	1 1 1 1	1 0 1 0	Set carry.
FB	DAA	1 1 1 1	1 0 1 1	Decimal adjust accumulator.
FC	KBP	1 1 1 1	1 1 0 0	Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
FD	DCL	1 1 1 1	1 1 0 1	Designate command line.

4040 ONLY INSTRUCTIONS

Hex Code	MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
01	HLT	0 0 0 0	0 0 0 1	Executes Halt until interrupt received.
02	BBS	0 0 0 0	0 0 1 0	Return from subroutine and restore SRC.
03	LCR	0 0 0 0	0 0 1 1	Data RAM and ROM bank status loaded into ACC.
04	OR4	0 0 0 0	0 1 0 0	OR accumulator with IR4.
05	OR5	0 0 0 0	0 1 0 1	OR accumulator with IR5.
06	AN6	0 0 0 0	0 1 1 0	AND accumulator with IR6.
07	AN7	0 0 0 0	0 1 1 1	AND accumulator with IR7.
08	DB0	0 0 0 0	1 0 0 0	Select ROM bank 0.
09	DB1	0 0 0 0	1 0 0 1	Select ROM bank 1.
0A	SB0	0 0 0 0	1 0 1 0	Select IR bank 0.
0B	SB1	0 0 0 0	1 0 1 1	Select IR bank 1.
0C	EIN	0 0 0 0	1 1 0 0	Enable interrupt detection.
0D	DIN	0 0 0 0	1 1 0 1	Disable interrupt detection.
0E	RPM	0 0 0 0	1 1 1 0	Load accumulator from 4289-controlled program RAM.

4001/4002/4008/4009/4289 INPUT/OUTPUT AND RAM INSTRUCTIONS

Hex Code	MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
2 -	SRC	0 0 1 0	R R R 1	Send register control. Send the address (contents of index register pair RRR) to ROM and RAM at X_2 and X_3 time in the instruction cycle.
E0	WRM	1 1 1 0	0 0 0 0	Write the contents of the accumulator into the previously selected RAM main memory character.
E1	WMP	1 1 1 0	0 0 0 1	Write the contents of the accumulator into the previously selected RAM output port. (Output Lines)
E2	WRR	1 1 1 0	0 0 1 0	Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)
E3	WPM	1 1 1 0	0 0 1 1	Write the contents of the accumulator into the previously selected half byte of read/write program memory (used with 4008/4009 or 4289 only)
E4	WR0	1 1 1 0	0 1 0 0	Write the contents of the accumulator into the previously selected RAM status character 0.
E5	WR1	1 1 1 0	0 1 0 1	Write the contents of the accumulator into the previously selected RAM status character 1.
E6	WR2	1 1 1 0	0 1 1 0	Write the contents of the accumulator into the previously selected RAM status character 2.
E7	WR3	1 1 1 0	0 1 1 1	Write the contents of the accumulator into the previously selected RAM status character 3.
E8	SBM	1 1 1 0	1 0 0 0	Subtract the previously selected RAM main memory character from accumulator with borrow.
E9	RDM	1 1 1 0	1 0 0 1	Read the previously selected RAM main memory character into the accumulator.
EA	RDR	1 1 1 0	1 0 1 0	Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)
EB	ADM	1 1 1 0	1 0 1 1	Add the previously selected RAM main memory character to accumulator with carry.
EC	RD0	1 1 1 0	1 1 0 0	Read the previously selected RAM status character 0 into accumulator.
ED	RD1	1 1 1 0	1 1 0 1	Read the previously selected RAM status character 1 into accumulator.
EE	RD2	1 1 1 0	1 1 1 0	Read the previously selected RAM status character 2 into accumulator.
EF	RD3	1 1 1 0	1 1 1 1	Read the previously selected RAM status character 3 into accumulator.

4040 INSTRUCTION CODES

Hex	Mnemonic		Hex	Mnemonic			Hex	Mnemonic		Hex	Mnemonic	
00	NOP		40	JUN			80	ADD	0	C0	BBL	0
01	HLT		41	JUN			81	ADD	1	C1	BBL	1
02	BBS		42	JUN			82	ADD	2	C2	BBL	2
03	LCR		43	JUN			83	ADD	3	C3	BBL	3
04	OR4		44	JUN			84	ADD	4	C4	BBL	4
05	OR5		45	JUN			85	ADD	5	C5	BBL	5
06	AN6		46	JUN			86	ADD	6	C6	BBL	6
07	AN7		47	JUN			87	ADD	7	C7	BBL	7
08	DB0		48	JUN			88	ADD	8	C8	BBL	8
09	DB1		49	JUN			89	ADD	9	C9	BBL	9
0A	SB0		4A	JUN			8A	ADD	10	CA	BBL	10
0B	SB1		4B	JUN			8B	ADD	11	CB	BBL	11
0C	EIN		4C	JUN			8C	ADD	12	CC	BBL	12
0D	DIN		4D	JUN			8D	ADD	13	CD	BBL	13
0E	RPM		4E	JUN		Second hex	8E	ADD	14	CE	BBL	14
0F	–		4F	JUN		digit is part	8F	ADD	15	CF	BBL	15
10	JCN	CN=0	50	JMS		of jump	90	SUB	0	D0	LDM	0
11	JCN	CN=1 also JNT	51	JMS		address.	91	SUB	1	D1	LDM	1
12	JCN	CN=2 also JC	52	JMS			92	SUB	2	D2	LDM	2
13	JCN	CN=3	53	JMS			93	SUB	3	D3	LDM	3
14	JCN	CN=4 also JZ	54	JMS			94	SUB	4	D4	LDM	4
15	JCN	CN=5	55	JMS			95	SUB	5	D5	LDM	5
16	JCN	CN=6	56	JMS			96	SUB	6	D6	LDM	6
17	JCN	CN=7	57	JMS			97	SUB	7	D7	LDM	7
18	JCN	CN=8	58	JMS			98	SUB	8	D8	LDM	8
19	JCN	CN=9 also JT	59	JMS			99	SUB	9	D9	LDM	9
1A	JCN	CN=10 also JNC	5A	JMS			9A	SUB	10	DA	LDM	10
1B	JCN	CN=11	5B	JMS			9B	SUB	11	DB	LDM	11
1C	JCN	CN=12 also JNZ	5C	JMS			9C	SUB	12	DC	LDM	12
1D	JCN	CN=13	5D	JMS			9D	SUB	13	DD	LDM	13
1E	JCN	CN=14	5E	JMS			9E	SUB	14	DE	LDM	14
1F	JCN	CN=15	5F	JMS			9F	SUB	15	DF	LDM	15
20	FIM	0	60	INC	0		A0	LD	0	E0	WRM	
21	SRC	0	61	INC	1		A1	LD	1	E1	WMP	
22	FIM	2	62	INC	2		A2	LD	2	E2	WRR	
23	SRC	2	63	INC	3		A3	LD	3	E3	WPM	
24	FIM	4	64	INC	4		A4	LD	4	E4	WR0	
25	SRC	4	65	INC	5		A5	LD	5	E5	WR1	
26	FIM	6	66	INC	6		A6	LD	6	E6	WR2	
27	SRC	6	67	INC	7		A7	LD	7	E7	WR3	
28	FIM	8	68	INC	8		A8	LD	8	E8	SBM	
29	SRC	8	69	INC	9		A9	LD	9	E9	RDM	
2A	FIM	10	6A	INC	10		AA	LD	10	EA	RDR	
2B	SRC	10	6B	INC	11		AB	LD	11	EB	ADM	
2C	FIM	12	6C	INC	12		AC	LD	12	EC	RD0	
2D	SRC	12	6D	INC	13		AD	LD	13	ED	RD1	
2E	FIM	14	6E	INC	14		AE	LD	14	EE	RD2	
2F	SRC	14	6F	INC	15		AF	LD	15	EF	RD3	
30	FIN	0	70	ISZ	0		B0	XCH	0	F0	CLB	
31	JIN	0	71	ISZ	1		B1	XCH	1	F1	CLC	
32	FIN	2	72	ISZ	2		B2	XCH	2	F2	IAC	
33	JIN	2	73	ISZ	3		B3	XCH	3	F3	CMC	
34	FIN	4	74	ISZ	4		B4	XCH	4	F4	CMA	
35	JIN	4	75	ISZ	5		B5	XCH	5	F5	RAL	
36	FIN	6	76	ISZ	6		B6	XCH	6	F6	RAR	
37	JIN	6	77	ISZ	7		B7	XCH	7	F7	TCC	
38	FIN	8	78	ISZ	8		B8	XCH	8	F8	DAC	
39	JIN	8	79	ISZ	9		B9	XCH	9	F9	TCS	
3A	FIN	10	7A	ISZ	10		BA	XCH	10	FA	STC	
3B	JIN	10	7B	ISZ	11		BB	XCH	11	FB	DAA	
3C	FIN	12	7C	ISZ	12		BC	XCH	12	FC	KBP	
3D	JIN	12	7D	ISZ	13		BD	XCH	13	FD	DCL	
3E	FIN	14	7E	ISZ	14		BE	XCH	14	FE	–	
3F	JIN	14	7F	ISZ	15		BF	XCH	15	FF	–	

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to Vss	+0.5V to -20V
Power Dissipation	1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

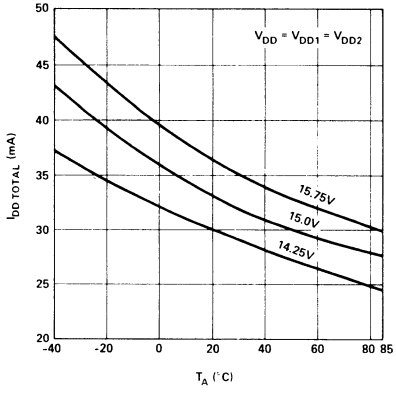
T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; 4040 V_{DD1} = V_{DD2} = V_{DD}; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}): Unless Otherwise specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{SB}	Standby Supply Current (V_{DD1} + V_{DD2})		3	5	mA	T_A = 25°C, V_{DD} = V_{SS}
I_{DD} (total)	Supply Current (V_{DD} + V_{DD1} + V_{DD2})		40	60	mA	T_A = 25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	µA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	4040 TEST and INT inputs
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS						
I_{LO}	Data Bus Output Leakage Current			10	µA	V_{OUT}=-12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT}=V_{SS}
I_{OL}	CM-ROM Sinking Current	6.5	12		mA	V_{OUT}=V_{SS}
I_{OL}	CM-RAM Sinking Current	2.5	6		mA	V_{OUT}=V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL}=0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT}=V_{SS}-.5V
R_{OH}	CM-ROM Output Resistance, Data Line "0" Level		320	600	Ω	V_{OUT}=V_{SS}-.5V
R_{OH}	CM-RAM Output Resistance, Data Line "0" Level		1.1	1.8	kΩ	V_{OUT}=V_{SS}-.5V
R_{OH}	INTA, CY, STPA Output Resistance "0" Level		1.1	1.8	kΩ	V_{OUT}=V_{SS}-.5V
CAPACITANCE						
C_{ϕ}	Clock Capacitance		17	25	pF	V_{IN}=V_{SS}
C_{DB}	Data Bus Capacitance		7	10	pF	V_{IN}=V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN}=V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN}=V_{SS}

Typical D.C. Characteristics

4040 I_{DD} VS. TEMPERATURE



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{SS} - V_{DD} = 15V \pm 5\%$

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Times			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_{WRPM}	Data-In Hold Time-RPM Instruction (X_2 state)	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{HRPM}	Data-In Write Time-RPM Instruction (X_2 state)	40	20		ns	
t_H[3]	Data Bus Hold Time During $X_2 - X_3$ Transition (I/O Read Instruction only)	150			ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}[5]	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	Data Lines			700	ns	200pF Data Lines[4]
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT}=20pF
t_{DEL}	CY, STPACK, INTACK Delay			2.0	μsec	

NOTES:
1. t_H measured with $t_{\phi R}$ = 10nsec.
2. t_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to the 4040 at X_2 always enter a float state until the 4040 takes over the data bus at X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. $C_{DATA\ BUS}$ = 200pF if 4008 and 4009 or 4289 is used.
5. The 4040 accumulator is gated out at X_1 time at ϕ_1 leading edge, and the t_{ACC} is 930 nsec + $t_{\phi D2}$.

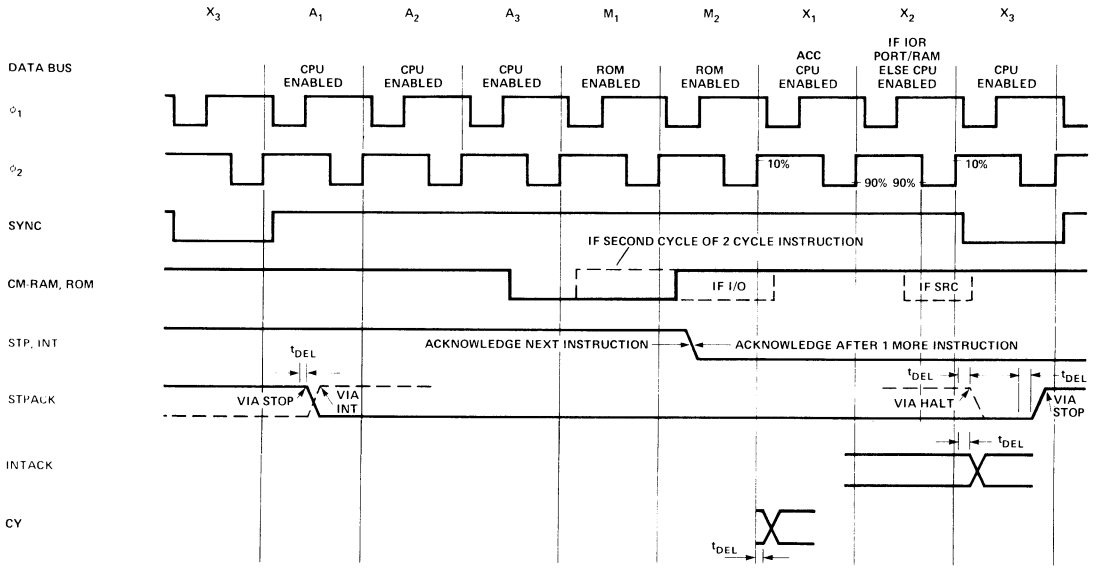


Figure 1. Timing Diagram.

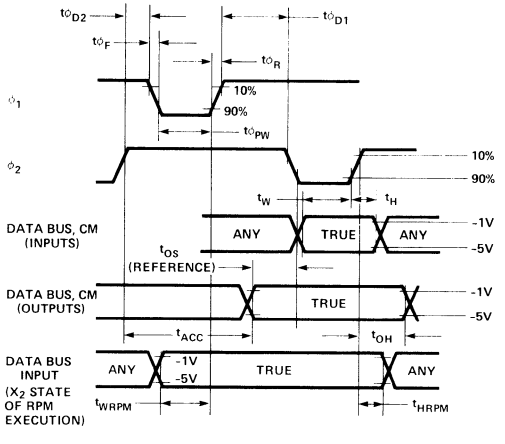


Figure 2. Timing Detail.

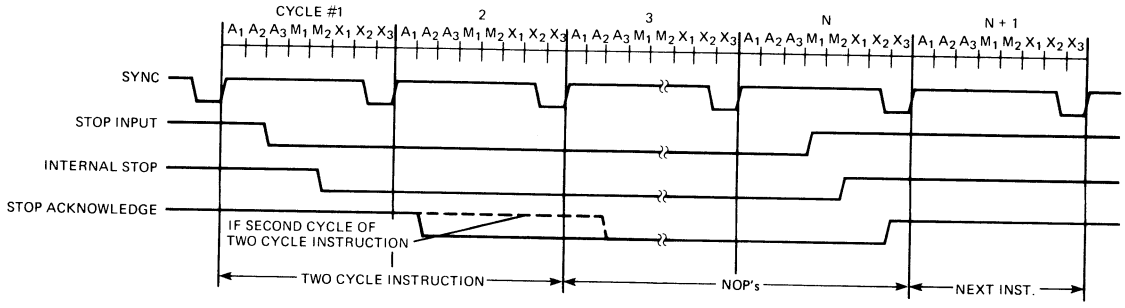


Figure 3. Stop Timing.

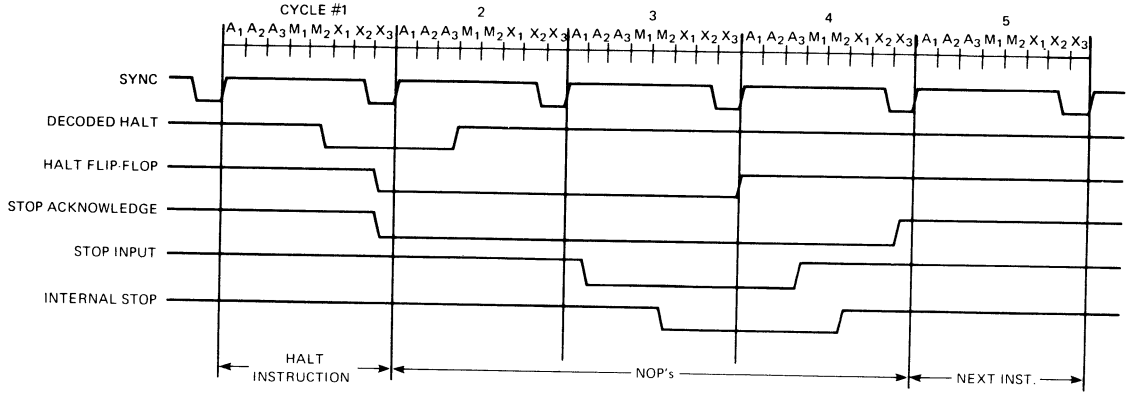


Figure 4. Halt Timing (Exit Using Stop Input).

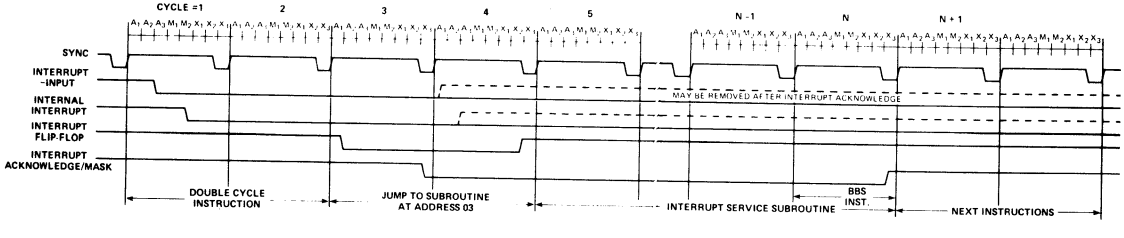


Figure 5. Interrupt Timing.

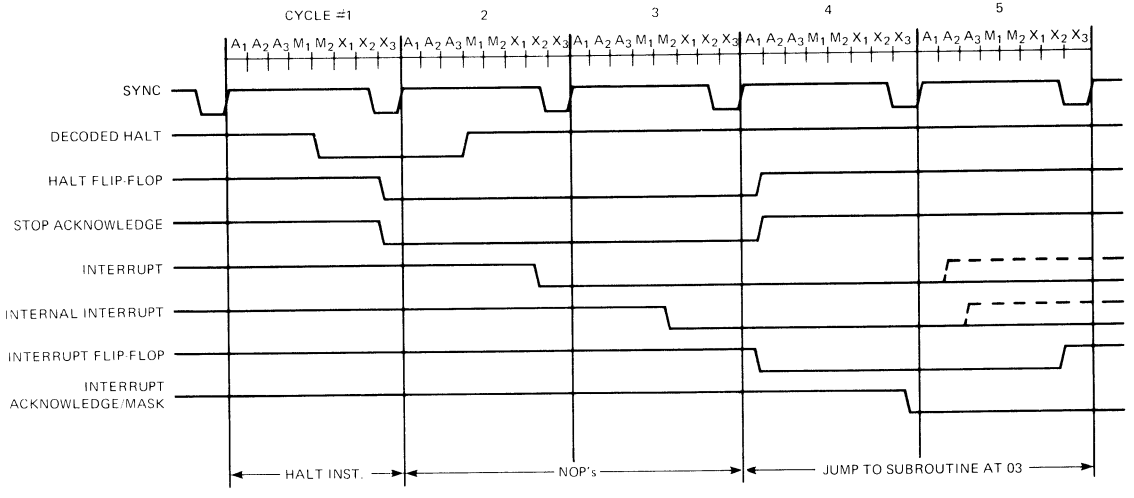


Figure 6. Halt Timing (Exit Using Interrupt).

4004
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

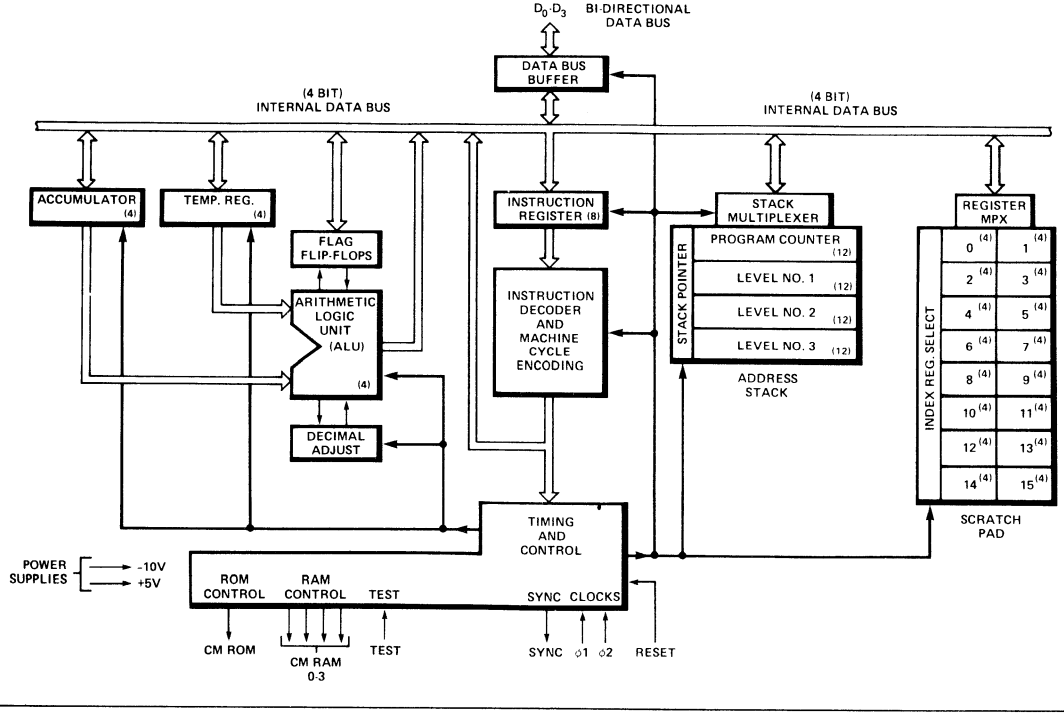
- 4-Bit Parallel CPU With 46 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes
- 10.8 Microsecond Instruction Cycle
- CPU Directly Compatible With MCS-40 ROMs and RAMs
- Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM
- Standard Operating Temperature Range of 0° to 70°C
- Also Available With -40° to +85°C Operating Range

The Intel® 4004 is a complete 4-bit parallel central processing unit (CPU). The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

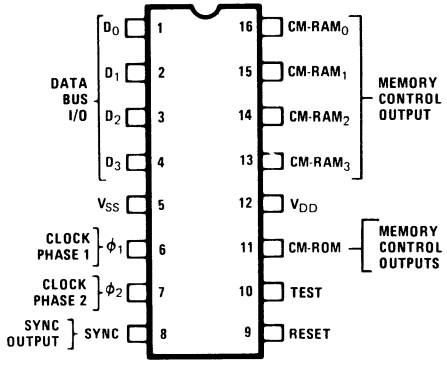
The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.

MCS 4/40



Pin Description



D_0-D_3

BIDIRECTIONAL DATA BUS. All address and data communication between the processor and the RAM and ROM chips occurs on these 4 lines.

RESET

RESET input. A logic "1" level at this input clears all flags and status registers and forces the program counter to zero. To completely clear all address and index registers, RESET must be applied for 64 clock cycles (8 machine cycles).

TEST

TEST input. The logical state of this signal may be tested with the JCN instruction.

SYNC

SYNC output. Synchronization signal generated by the processor and set to the ROM and RAM chips. It indicates the beginning of an instruction cycle.

CM-ROM

CM-ROM output. This is the ROM selection signal sent out by the processor when data is required from program memory.

CM-RAM$_0$ – CM-RAM$_3$

CM-RAM outputs. These are the bank selection signals for the 4002 RAM chips in the system.

ϕ_1, ϕ_2

Two phase clock inputs.

V_{SS}

Most positive voltage.

V_{DD}

V_{SS} -15 ±5% main supply voltage.

Instruction Set Format

A. Machine Instructions

- 1 word instruction – 8-bits requiring 8 clock periods (instruction cycle).
- 2 word instruction – 16-bits requiring 16 clock periods (2 instruction cycles).

Each instruction is divided into two four-bit fields. The upper 4-bits is the OPR field containing the operation code. The lower 4-bits is the OPA field containing the modifier. For two word instructions, the second word contains address information or data.

The upper 4-bits (OPR) will always be fetched before the lower 4-bits (OPA) during M_1 and M_2 times respectively.

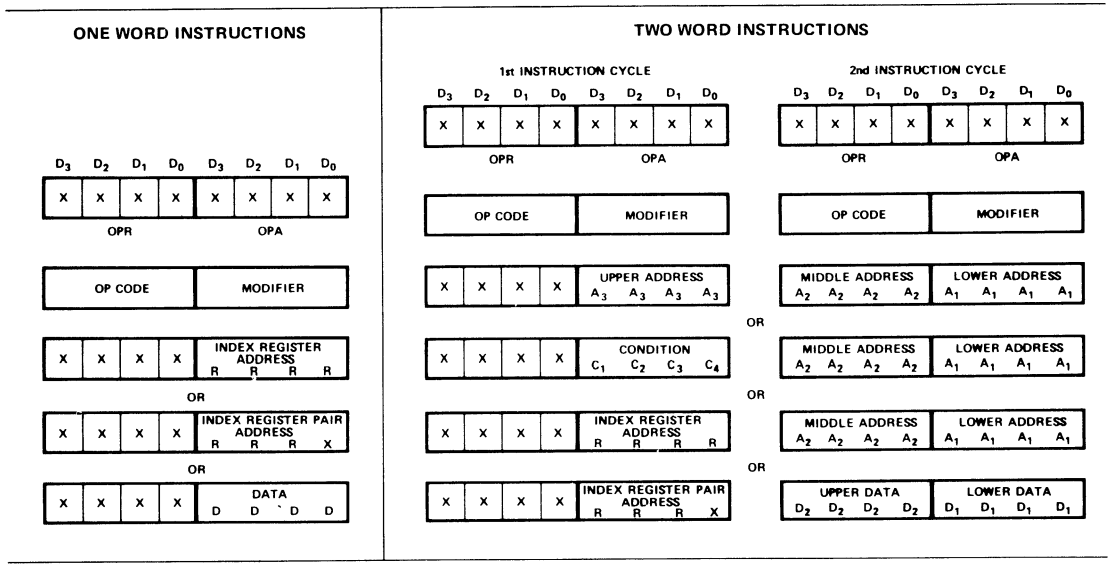


Table I. Machine Instruction Format

B. Input/Output and RAM Instructions and Accumulator Group Instructions

In these instructions (which are all single word) the OPR contains a 4-bit code which identifies either the I/O instruction or the accumulator group instruction and the OPA contains a 4-bit code which identifies the operation to be performed. Table II illustrates the contents of each 4-bit field.

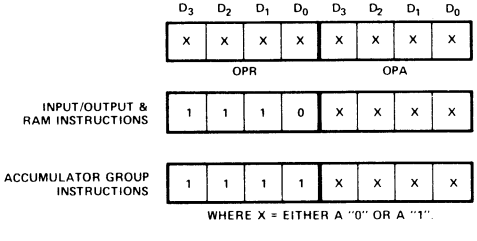


Table II. I/O and Accumulator Group Instruction Formats

4004 Instruction Set

BASIC INSTRUCTIONS (* = 2 Word Instructions)

Hex Code	MNEMONIC	OPR $D_3 D_2 D_1 D_0$	OPA $D_3 D_2 D_1 D_0$	DESCRIPTION OF OPERATION
00	NOP	0 0 0 0	0 0 0 0	No operation.
1 -	*JCN	0 0 0 1	$C_1 C_2 C_3 C_4$	Jump to ROM address $A_2 A_2 A_2 A_2$, $A_1 A_1 A_1 A_1$ (within the same ROM that contains this JCN instruction) if condition $C_1 C_2 C_3 C_4$ is true, otherwise go to the next instruction in sequence.
- -		$A_2 A_2 A_2 A_2$	$A_1 A_1 A_1 A_1$	
2 -	*FIM	0 0 1 0	R R R 0	Fetch immediate (direct) from ROM Data $D_2 D_2 D_2 D_2 D_1 D_1 D_1 D_1$ to index register pair location RRR.
- -		$D_2 D_2 D_2 D_2$	$D_1 D_1 D_1 D_1$	
3 -	FIN	0 0 1 1	R R R 0	Fetch indirect from ROM. Send contents of index register pair location 0 out as an address. Data fetched is placed into register pair location RRR.
3 -	JIN	0 0 1 1	R R R 1	Jump indirect. Send contents of register pair RRR out as an address at A_1 and A_2 time in the instruction cycle.
4 -	*JUN	0 1 0 0	$A_3 A_3 A_3 A_3$	Jump unconditional to ROM address $A_3 A_3 A_3 A_3 A_2 A_2 A_2 A_2$ $A_1 A_1 A_1 A_1$.
- -		$A_2 A_2 A_2 A_2$	$A_1 A_1 A_1 A_1$	
5 -	*JMS	0 1 0 1	$A_3 A_3 A_3 A_3$	Jump to subroutine ROM address $A_3 A_3 A_3 A_3 A_2 A_2 A_2 A_2$ $A_1 A_1 A_1 A_1$, save old address (up 1 level in stack.)
- -		$A_2 A_2 A_2 A_2$	$A_1 A_1 A_1 A_1$	
6 -	INC	0 1 1 0	R R R R	Increment contents of register RRRR.
7 -	*ISZ	0 1 1 1	R R R R	Increment contents of register RRRR. Go to ROM address $A_2 A_2 A_2 A_2$ $A_1 A_1 A_1 A_1$ (within the same ROM that contains this ISZ instruction) if result $\neq 0$, otherwise go to the next instruction in sequence.
- -		$A_2 A_2 A_2 A_2$	$A_1 A_1 A_1 A_1$	
8 -	ADD	1 0 0 0	R R R R	Add contents of register RRRR to accumulator with carry.
9 -	SUB	1 0 0 1	R R R R	Subtract contents of register RRRR to accumulator with borrow.
A -	LD	1 0 1 0	R R R R	Load contents of register RRRR to accumulator.
B -	XCH	1 0 1 1	R R R R	Exchange contents of index register RRRR and accumulator.
C -	BBL	1 1 0 0	D D D D	Branch back (down 1 level in stack) and load data DDDD to accumulator.
D -	LDM	1 1 0 1	D D D D	Load data DDDD to accumulator.
F0	CLB	1 1 1 1	0 0 0 0	Clear both. (Accumulator and carry)
F1	CLC	1 1 1 1	0 0 0 1	Clear carry.
F2	IAC	1 1 1 1	0 0 1 0	Increment accumulator.
F3	CMC	1 1 1 1	0 0 1 1	Complement carry.
F4	CMA	1 1 1 1	0 1 0 0	Complement accumulator.
F5	RAL	1 1 1 1	0 1 0 1	Rotate left. (Accumulator and carry)
F6	RAR	1 1 1 1	0 1 1 0	Rotate right. (Accumulator and carry)
F7	TCC	1 1 1 1	0 1 1 1	Transmit carry to accumulator and clear carry.
F8	DAC	1 1 1 1	1 0 0 0	Decrement accumulator.
F9	TCS	1 1 1 1	1 0 0 1	Transfer carry subtract and clear carry.
FA	STC	1 1 1 1	1 0 1 0	Set carry.
FB	DAA	1 1 1 1	1 0 1 1	Decimal adjust accumulator.
FC	KBP	1 1 1 1	1 1 0 0	Keyboard process. Converts the contents of the accumulator from a one out of four code to a binary code.
FD	DCL	1 1 1 1	1 1 0 1	Designate command line.

4001/4002/4008/4009/4289 INPUT/OUTPUT AND RAM INSTRUCTIONS

Hex Code	MNEMONIC	OPR D_3 D_2 D_1 D_0	OPA D_3 D_2 D_1 D_0	DESCRIPTION OF OPERATION
2 -	SRC	0 0 1 0	R R R 1	Send register control. Send the address (contents of index register pair RRR) to ROM and RAM at X_2 and X_3 time in the instruction cycle.
E0	WRM	1 1 1 0	0 0 0 0	Write the contents of the accumulator into the previously selected RAM main memory character.
E1	WMP	1 1 1 0	0 0 0 1	Write the contents of the accumulator into the previously selected RAM output port. (Output Lines)
E2	WRR	1 1 1 0	0 0 1 0	Write the contents of the accumulator into the previously selected ROM output port. (I/O Lines)
E3	WPM	1 1 1 0	0 0 1 1	Write the contents of the accumulator into the previously selected half byte of read/write program memory (used with 4008/4009 or 4289 only)
E4	WR0	1 1 1 0	0 1 0 0	Write the contents of the accumulator into the previously selected RAM status character 0.
E5	WR1	1 1 1 0	0 1 0 1	Write the contents of the accumulator into the previously selected RAM status character 1.
E6	WR2	1 1 1 0	0 1 1 0	Write the contents of the accumulator into the previously selected RAM status character 2.
E7	WR3	1 1 1 0	0 1 1 1	Write the contents of the accumulator into the previously selected RAM status character 3.
E8	SBM	1 1 1 0	1 0 0 0	Subtract the previously selected RAM main memory character from accumulator with borrow.
E9	RDM	1 1 1 0	1 0 0 1	Read the previously selected RAM main memory character into the accumulator.
EA	RDR	1 1 1 0	1 0 1 0	Read the contents of the previously selected ROM input port into the accumulator. (I/O Lines)
EB	ADM	1 1 1 0	1 0 1 1	Add the previously selected RAM main memory character to accumulator with carry.
EC	RD0	1 1 1 0	1 1 0 0	Read the previously selected RAM status character 0 into accumulator.
ED	RD1	1 1 1 0	1 1 0 1	Read the previously selected RAM status character 1 into accumulator.
EE	RD2	1 1 1 0	1 1 1 0	Read the previously selected RAM status character 2 into accumulator.
EF	RD3	1 1 1 0	1 1 1 1	Read the previously selected RAM status character 3 into accumulator.

4004 Instruction Codes

Hex	Mnemonic		Hex	Mnemonic			Hex	Mnemonic		Hex	Mnemonic	
00	–		40	JUN			80	ADD	0	C0	BBL	0
01	–		41	JUN			81	ADD	1	C1	BBL	1
02	–		42	JUN			82	ADD	2	C2	BBL	2
03	–		43	JUN			83	ADD	3	C3	BBL	3
04	–		44	JUN			84	ADD	4	C4	BBL	4
05	–		45	JUN			85	ADD	5	C5	BBL	5
06	–		46	JUN			86	ADD	6	C6	BBL	6
07	–		47	JUN			87	ADD	7	C7	BBL	7
08	–		48	JUN			88	ADD	8	C8	BBL	8
09	–		49	JUN			89	ADD	9	C9	BBL	9
0A	–		4A	JUN			8A	ADD	10	CA	BBL	10
0B	–		4B	JUN			8B	ADD	11	CB	BBL	11
0C	–		4C	JUN			8C	ADD	12	CC	BBL	12
0D	–		4D	JUN			8D	ADD	13	CD	BBL	13
0E	–		4E	JUN		Second hex	8E	ADD	14	CE	BBL	14
0F	–		4F	JUN		digit is part	8F	ADD	15	CF	BBL	15
10	JCN	CN=0	50	JMS		of jump	90	SUB	0	D0	LDM	0
11	JCN	CN=1 also JNT	51	JMS		address.	91	SUB	1	D1	LDM	1
12	JCN	CN=2 also JC	52	JMS			92	SUB	2	D2	LDM	2
13	JCN	CN=3	53	JMS			93	SUB	3	D3	LDM	3
14	JCN	CN=4 also JZ	54	JMS			94	SUB	4	D4	LDM	4
15	JCN	CN=5	55	JMS			95	SUB	5	D5	LDM	5
16	JCN	CN=6	56	JMS			96	SUB	6	D6	LDM	6
17	JCN	CN=7	57	JMS			97	SUB	7	D7	LDM	7
18	JCN	CN=8	58	JMS			98	SUB	8	D8	LDM	8
19	JCN	CN=9 also JT	59	JMS			99	SUB	9	D9	LDM	9
1A	JCN	CN=10 also JNC	5A	JMS			9A	SUB	10	DA	LDM	10
1B	JCN	CN=11	5B	JMS			9B	SUB	11	DB	LDM	11
1C	JCN	CN=12 also JNZ	5C	JMS			9C	SUB	12	DC	LDM	12
1D	JCN	CN=13	5D	JMS			9D	SUB	13	DD	LDM	13
1E	JCN	CN=14	5E	JMS			9E	SUB	14	DE	LDM	14
1F	JCN	CN=15	5F	JMS			9F	SUB	15	DF	LDM	15
20	FIM	0	60	INC	0		A0	LD	0	E0	WRM	
21	SRC	0	61	INC	1		A1	LD	1	E1	WMP	
22	FIM	2	62	INC	2		A2	LD	2	E2	WRR	
23	SRC	2	63	INC	3		A3	LD	3	E3	WPM	
24	FIM	4	64	INC	4		A4	LD	4	E4	WR0	
25	SRC	4	65	INC	5		A5	LD	5	E5	WR1	
26	FIM	6	66	INC	6		A6	LD	6	E6	WR2	
27	SRC	6	67	INC	7		A7	LD	7	E7	WR3	
28	FIM	8	68	INC	8		A8	LD	8	E8	SBM	
29	SRC	8	69	INC	9		A9	LD	9	E9	RDM	
2A	FIM	10	6A	INC	10		AA	LD	10	EA	RDR	
2B	SRC	10	6B	INC	11		AB	LD	11	EB	ADM	
2C	FIM	12	6C	INC	12		AC	LD	12	EC	RD0	
2D	SRC	12	6D	INC	13		AD	LD	13	ED	RD1	
2E	FIM	14	6E	INC	14		AE	LD	14	EE	RD2	
2F	SRC	14	6F	INC	15		AF	LD	15	EF	RD3	
30	FIN	0	70	ISZ	0		B0	XCH	0	F0	CLB	
31	JIN	0	71	ISZ	1		B1	XCH	1	F1	CLC	
32	FIN	2	72	ISZ	2		B2	XCH	2	F2	IAC	
33	JIN	2	73	ISZ	3		B3	XCH	3	F3	CMC	
34	FIN	4	74	ISZ	4		B4	XCH	4	F4	CMA	
35	JIN	4	75	ISZ	5		B5	XCH	5	F5	RAL	
36	FIN	6	76	ISZ	6		B6	XCH	6	F6	RAR	
37	JIN	6	77	ISZ	7		B7	XCH	7	F7	TCC	
38	FIN	8	78	ISZ	8		B8	XCH	8	F8	DAC	
39	JIN	8	79	ISZ	9		B9	XCH	9	F9	TCS	
3A	FIN	10	7A	ISZ	10		BA	XCH	10	FA	STC	
3B	JIN	10	7B	ISZ	11		BB	XCH	11	FB	DAA	
3C	FIN	12	7C	ISZ	12		BC	XCH	12	FC	KBP	
3D	JIN	12	7D	ISZ	13		BD	XCH	13	FD	DCL	
3E	FIN	14	7E	ISZ	14		BE	XCH	14	FE	–	
3F	JIN	14	7F	ISZ	15		BF	XCH	15	FF	–	

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

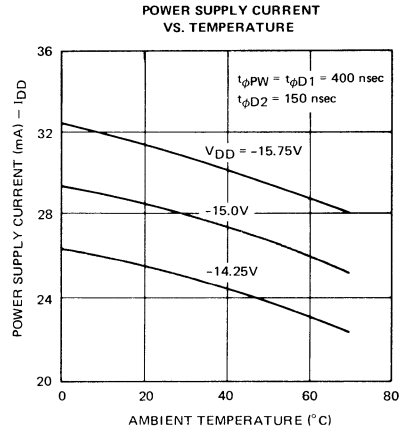
D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ± 5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		30	40	mA	T_A=25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	V_{IL}=V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	4004 TEST Input
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT}=-12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitance Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT}=V_{SS}
I_{OL}	CM-ROM Sinking Current	6.5	12		mA	V_{OUT}=V_{SS}
I_{OL}	CM-RAM Sinking Current	2.5	6		mA	V_{OUT}=V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL}=0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT}=V_{SS}-.5V
R_{OH}	CM-ROM Output Resistance, Data Line "0" Level		320	600	Ω	V_{OUT}=V_{SS}-.5V
R_{OH}	CM-RAM Output Resistance, Data Line "0" Level		1.1	1.8	kΩ	V_{OUT}=V_{SS}-.5V
CAPACITANCE						
C_{ϕ}	Clock Capacitance		14	20	pF	V_{IN}=V_{SS}
C_{DB}	Data Bus Capacitance		7	10	pF	V_{IN}=V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN}=V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN}=V_{SS}

Typical D.C. Characteristics



A.C. Characteristics

T_A=0°C to 70°C, V_{SS}-V_{DD} = 15V ±5%

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t_{\phi R}$	Clock Rise Time			50	ns	
$t_{\phi F}$	Clock Fall Times			50	ns	
$t_{\phi PW}$	Clock Width	380		480	ns	
$t_{\phi D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t_{\phi D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_H[3]	Data Bus Hold Time During M_2-X_1 and and X_2-X_3 Transition.	150			ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	Data Lines			700	ns	200pF Data Lines[4]
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT}=20pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to the 4004 at M_2 and X_2 always enter a float state until the 4004 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. $C_{DATA\ BUS}$ = 200pF if 4008 and 4009 or 4289 is used.

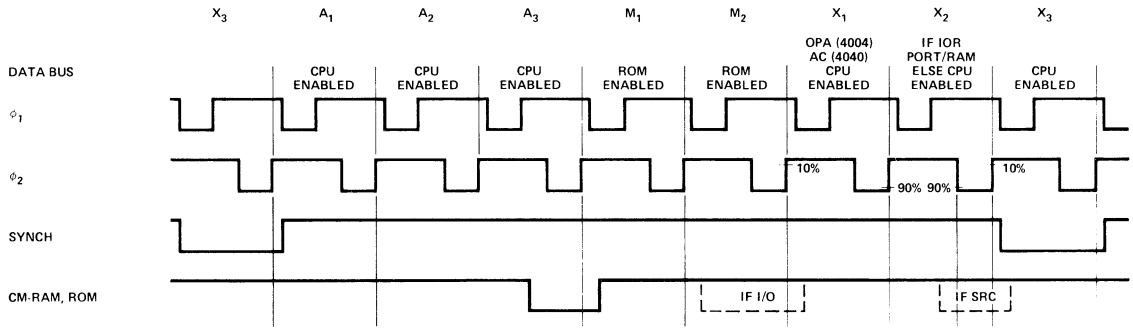


Figure 1. Timing Diagram.

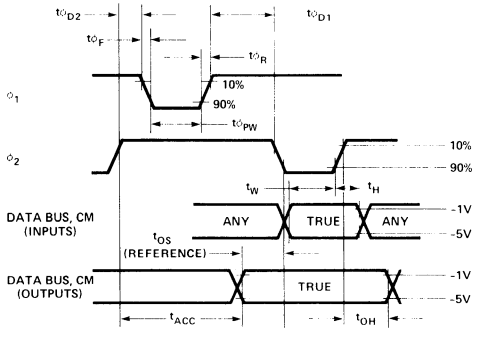


Figure 2. Timing Detail.

4003

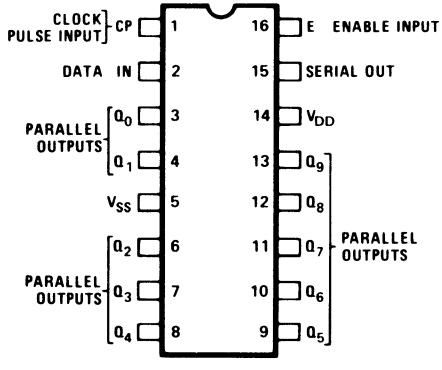
10 BIT SHIFT REGISTER/OUTPUT EXPANDER

- **10 Bit Serial-In/Parallel Out**
- **Serial-Out Capability for Additional I/O Expansion**
- **16 Pin Dual-In-Line Package**
- **Easy Expansion of I/O Output Capability**
- **Enable Output Control**
- **Standard Operating Temperature Range of 0° to 70°C**

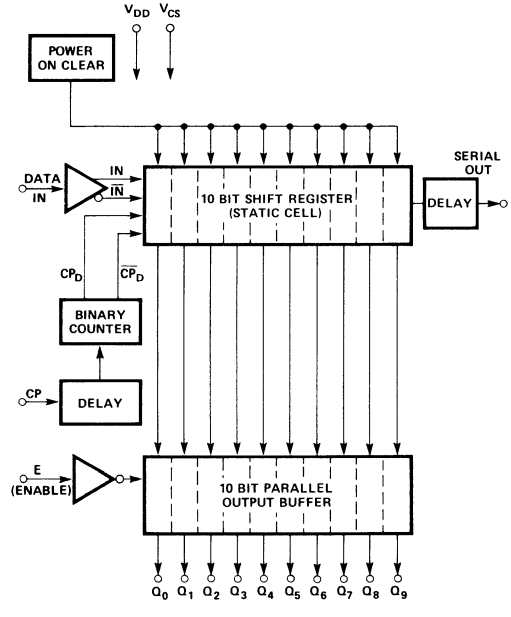
The 4003 is a 10 bit serial-in, parallel-out, serial-out shift register with enable logic. The 4003 is used to expand the number of ROM and RAM I/O ports to communicate with peripheral devices such as keyboards, printers, displays, readers, teletypewriters, etc.

The 4003 is a single phase static shift register; however, the clock pulse (CP) maximum width is limited to 10 msec. Data-in and CP can be simultaneous. To avoid race conditions, CP is internally delayed.

PIN CONFIGURATION



BLOCK DIAGRAM



Pin Description

Pin No.	Designation	Description of Function
1	CP	The clock pulse input. A "0" (V_{SS}) to "1" (V_{DD}) transition will shift data in.
2	DATA IN	Serial data input line.
3	O_0	Parallel data output lines, when enabled. Each pin may be made TTL compatible with a 5.6K pull-down resistor to V_{DD}.
4	O_1	
6	O_2	
7	O_3	
8	O_4	
9	O_5	
10	O_6	
11	O_7	
12	O_8	
13	O_9	
5	V_{SS}	Most positive supply voltage.
14	V_{DD}	Main supply voltage value must be V_{SS} - 15.0V ± 5% (-10v for TTL operation)
15	Serial out	Serial data output.
16	E	Enable, when E = "1" (V_{DD}) the output lines contain valid data. When E = "0" (V_{SS}) the output lines are at V_{SS}.

Functional Description

The 4003 is designed to be typically appended to an MCS-40 I/O port. This can be the I/O port of a 4001, 4002, 4289, 4308, or a 4265. One I/O line is assigned to be the Enable (E), another the Clock (CP), and still another the Serial Data-Input. For example, to access the 4003 a subroutine of sequential outputs consisting of Data, clock pulse on, Enable — followed by an output of clock pulse off and Enable, will serially load the 4003.

Data is loaded serially and is available in parallel on 10 output lines which are accessed through enable logic. When enabled (E = 1 -- V_{DD}), the shift register contents are read out; when not enabled (E = 0 -- V_{SS}), the parallel-out lines are at Logic "0" (V_{SS}). The serial-out line is not affected by the enable logic to allow longer word cascading.

Data is also available serially permitting an indefinite number of similar devices to be cascaded together to provide shift register length multiples of 10.

The data shifting is controlled by the CP signal. An internal power-on-clear circuit will clear the shift register (outputs = 0 or V_{SS}) between the application of the supply voltage and the first CP signal.

The 4003 output buffers are useful for multiple key depression rejection when a 4003 is used in conjunction with a keyboard. In this mode if up to three output lines are connected together, the state of the output is high (Logic "0" or V_{SS}) if at least one line is high.

Another typical application of the 4003 is for Keyboard or Display Scanning where a single bit of Logic "1" is shifted through the 4003 and is used to activate the various digits, keyboard rows, etc.

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to V_{SS} ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

T_A = 0°C to +70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec, $t_{\phi D2}$ = 150 nsec, unless otherwise specified.

Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}), Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}).

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Limit Typ.[1]	Limit Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		5.0	8.5	mA	t_{WL} = t_{WH} = 8μsec; T_A = 25°C
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage	V_{SS}-1.5		V_{SS}+.3		
V_{IL}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
I/O OUTPUT CHARACTERISTICS						
I_{OL}	Parallel Out Pins Sinking Current, "1" Level	0.6	1.0		mA	V_{OUT} = 0V. For TTL compatibility a 5.6KΩ (±10%) resistor between output and V_{DD} should be added.[2]
I_{OL}	Serial Out Sinking Current, "1" Level	1.0	2.0		mA	V_{OUT} = 0V
V_{OL}	Output Low Voltage	V_{SS}-11	V_{SS}-7.5	V_{SS}-6.5	V	I_{OL} = 10μA
R_{OH}	Parallel-Out Pins Output Resistance "0" Level		400	750	Ω	V_{OUT} = -0.5V
R_{OH}	Serial Out Output Resistance "0" Level		650	1200	Ω	V_{OUT} = -0.5V

Notes: 1. Typical values are to T_A = 25°C and Nominal Supply Voltages.

2. For TTL compatibility on the I/O lines the supply voltages should be V_{DD} = -10V ±5%; V_{SS} = +5V ±5%.

MCS 4/40

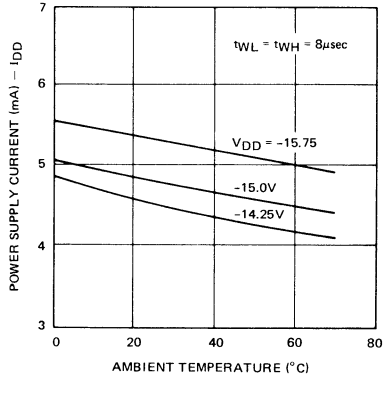
CAPACITANCE

f = 1 MHz; V_{IN} = 0V; T_A = 25°C; Unmeasured Pins Grounded.

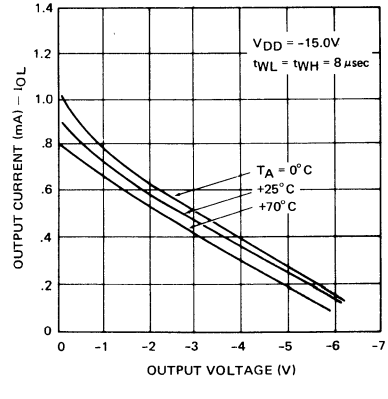
Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF

Typical D.C. Characteristics

POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT VOLTAGE



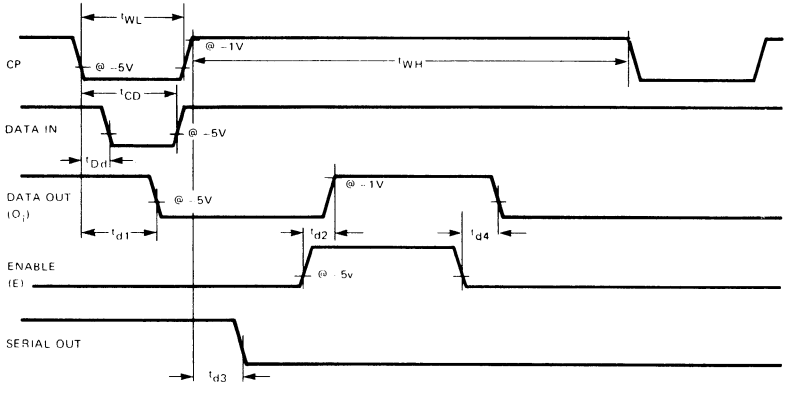
A.C. Characteristics

$T_A = 0°C$ to $+70°C$; $V_{DD} = -15 \pm 5\%$, $V_{SS} = GND$

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
t_{WL}	CP Low Width	6		10,000	μsec	
t_{WH}[1]	CP High Width	6			μsec	
t_{CD}	Clock-On to Data-Off Time	3			μsec	
t_{Dd}[2]	CP to Data Set Delay			250	nsec	
t_{d1}	CP to Data Out Delay	250		1750	nsec	
t_{d2}	Enable to Data Out Delay			350	nsec	C_{OUT} = 20pF
t_{d3}	CP to Serial Out Delay	200		1250	nsec	C_{OUT} = 20pF
t_{d4}	Enable to Data Out Delay			1.0	μsec	C_{OUT} = 20pF

Notes: 1. t_{WH} can be any time greater than 6μsec.
2. Data can occur prior to CP.

Timing Diagram



4265
PROGRAMMABLE GENERAL PURPOSE I/O DEVICE

- **Multi-Mode 14 Operating Modes**
- **16 Lines of I/O Capability**
- **Bit Set/Reset**
- **Multiplexable Outputs**
- **Eight Bit Transfer Mode**
- **Interfaces to 8080 Peripherals**
- **Synchronous and Asynchronous Interface**
- **Strobed Buffer Inputs and Outputs**
- **TTL Interface**
- **Up to Eight 4265s Per System**
- **Interface to Standard RAMs**
- **28 Pin Dual-In-Line Package**
- **Interface to Standard RAMs**
- **28 Pin Dual-In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available with -40° to +85°C Operating Range**

The 4265 is a general purpose I/O device designed to interface with the MCS-40™ microcomputer family. This device provides four software programmable 4-bit I/O ports which can be configured to allow any one of fourteen unique operating modes for interfacing to data memory or a variety of user peripheral devices.

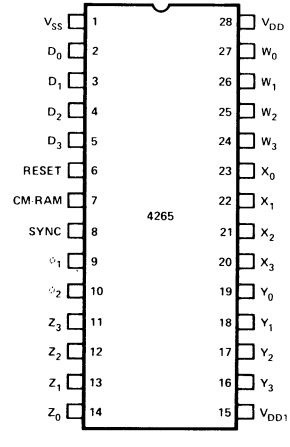
A single MCS-40 system can accomodate up to four 4265s (one per CM-RAM) without external logic or up to eight 4265s with one external decoder.

The 4265 resides on the MCS-40 data bus and uses the same selection procedure as 4002 RAM device. A valid compare selects the 4265 for MCS-40 I/O commands. As in the case of the 4002 or any MCS-40 peripheral circuit, selection occurs only when the proper SRC code and the CM signal are present simultaneously.

The 4265 provides an extremely flexible, general purpose I/O system capable of handling 4- or 8-bit input or output data. One of fourteen basic operating modes can be selected (software programmable) as described below.

Port Z is TTL compatible with any TTL device. Ports W, X, and Y are low-power TTL compatible.

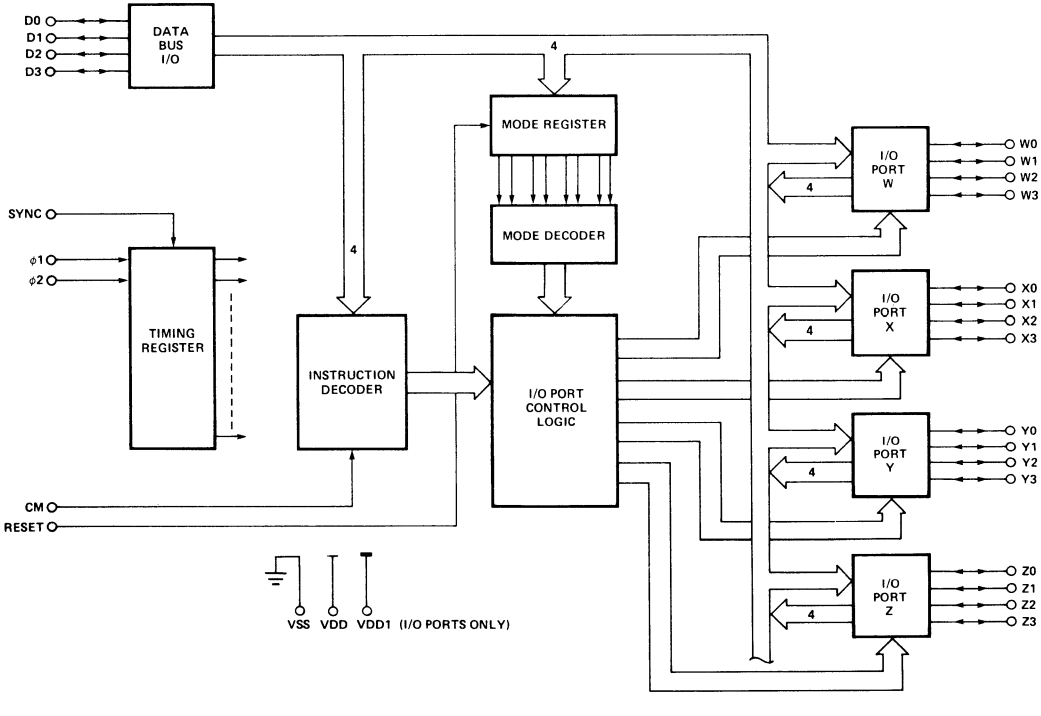
PIN CONFIGURATION



Pin Description

Pin No.	Designation	Function
2-5	D0-D3	Bi-directional data bus. All address, instruction and data communication between processor and I/O ports are transferred on this port.
6	RESET	A negative level (V_{DD}) applied to this pin clears all storage elements, places the 4265 in the Reset Mode and deselects the device.
7	CM	Command input driven by a CM-RAM output of the processor. Used for decoding SRC, RDM, WRM, WMP, SBM, ADM, WR0-3 and RD0-3.
9-10	ϕ1-ϕ2	Non-overlapping clock signals which determine timing.
8	SYNC	Synchronization signal generated by the processor; indicates the beginning of an instruction.
24-27 20-23 16-19 11-14	W3-W0 X3-X0 Y3-Y0 Z3-Z0	Four programmable I/O ports having different functional designation depending on 4265 mode of operation. A data bus "1" negative true (V_{DD}) will appear on a port as a "1" positive true (V_{SS}). These ports are TTL compatible.
28	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.
15	V_{DD1}	Supply voltage foı I/O ports.
1	V_{SS}	Most positive supply voltage (V_{DD1} = 0V, V_{SS} = 5V for TTL I/O ports. V_{DD1} = V_{DD} for MOS loads only).
28 = TOTAL PINS		

4265 HARDWARE BLOCK DIAGRAM



4265 PROGRAMMABLE MODES

OPERATING MODES

- Mode 1 – 8-Bit Asynchronous I/O Port (Bidirectional)
  4-Bit Input Port (Unbuffered)
- Mode 2 – 8-Bit Asynchronous I/O Port (Bidirectional)
  4-Bit Output Port
- Mode 3 – 8-Bit Synchronous I/O Port (Bidirectional)
  4-Bit Synchronous Output Port
- Mode 4 – Four 4-Bit Output Ports
- Mode 5 – Three 4-Bit Output Ports
  One 4-Bit Input Port (Unbuffered)
- Mode 6 – Two 4-Bit Output Ports
  Two 4-Bit Input Ports (Unbuffered)
- Mode 7 – One 4-Bit Output Port
  Three 4-Bit Input Ports (Unbuffered)
- Mode 8 – Three 4-Bit Synchronous Output Ports
- Mode 9 – Two 4-Bit Synchronous Output Ports
  One 4-Bit Asynchronous Input Port

OPERATING MODES

- Mode 10 – One 4-Bit Synchronous Output Port
  Two 4-Bit Asynchronous Input Ports
- Mode 11 – Three 4-Bit Asynchronous Input Ports
- Mode 12 – 8-Bit Address Port
  4-Bit Synchronous I/O Port (Bidirectional)
  2 Device Selection Control Signals
- Mode 13 – 8-Bit Address Port
  4-Bit Asynchronous I/O Port (Bidirectional)

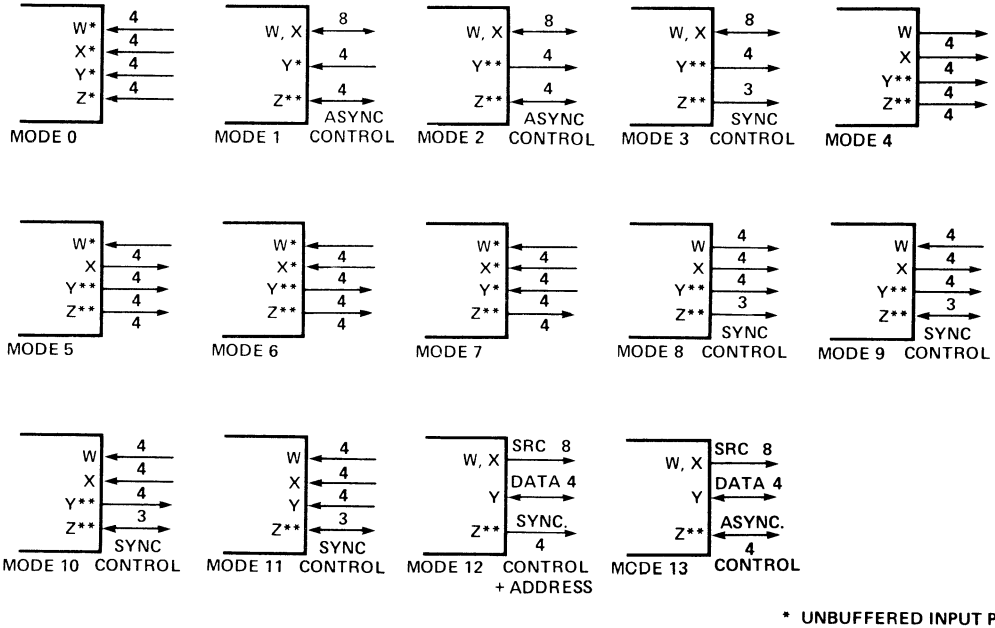
CONTROL AND OPERATING MODE

- Mode 0 – Four 4-Bit Input Ports (Unbuffered)
  Resets I/O Buffers

CONTROL MODES

- Mode 14 – Disables all output buffers, allowing another 4265 to be multiplexed at the port level.
- Mode 15 – Enables output buffers, previous mode restored.

4265 MODE DIAGRAM



* UNBUFFERED INPUT PORTS.

**THE LINES ON THESE PORTS ARE SUBJECT TO THE BIT SET COMMAND.

Functional Description

Control Functions: Two types of operations are possible with the 4265. The device (once selected) can be programmed to one of fourteen basic operating modes. This is accomplished by executing a WMP instruction which sends the 4-bit content of the CPU's Accumulator to the 4265 where it is decoded and used to logically configure the device. A second Control operation makes use of the WRM instruction to select one of eight output lines (Port Y or Z) and perform a SET or RESET operation on that line. This is accomplished by interpreting the 4-bit Accumulator value as follows: The upper three bits select one of eight output latches; the least significant bit determines whether a SET or RESET operation is to be performed.

Data Transfer Functions: The remaining eleven instructions provide four WRITE operations (WR0, WR1, WR2, WR3) and seven READ operations (RD0, RD1, RD2, RD3, ADM, SBM, RDM). These allow data in 4-bit or 8-bit format to be transmitted between the 4265 and external I/O devices or memory devices (all transfers between processor and 4265 are 4-bit transfers).

The sixteen lines of the 4265 are grouped into four ports, four bits each referred to as W, X, Y and Z. The ports can be interrogated by a RD0-3 corresponding to ports W - Z respectively. This means that even when a port is designated as a control port or an output port, the state of the port can be inputted by a RD0-3 instruction (except in modes 12 and 13). The WR0-3 instruction will load the ports W - Z designated outputs. When a port is specifically designated as an input port, it will not respond to an output type instruction (WR0-3, WRM, etc.). See specific mode selection for details.

When port Y or Z is designated an output, regardless of the mode, then it will respond to the Bit Set command. The Bit Set Command allows the user to set the polarity of a single bit without affecting any other bit. This is particularly useful when the output port of interest drives control lines tied to the user system. The user can selectively alter the bit polarity. To alter a bit, the MCS-40 WRM command is utilized.

The 4265 is selected via the CM-RAM line and an appropriate MCS-40™ SRC command. The upper two bits of data at X2 of an SRC instruction with the CM-RAM signal are compared with an address code internal to the 4265. One standard code is available, a code of 2. This allows one 4265 per CM-RAM or up to four per system without additional logic. By using one external decoder and the ability of the DCL (Designate Command Line) instruction to code the CM-RAM lines, up to eight 4265s can be used in a system. Other peripheral devices can share a CM-RAM line with the 4265 (except Mode 12 and 13). For example, a CM-RAM line can contain three 4002 RAMs and one 4265.

The operating modes of the 4265 are selected under program control by the processor. When a 4265 is designed into a specific application, one functional mode is selected. With the possible exception of RESET, ENABLE, and DISABLE, a functional change in mode would not normally be initiated by the software once the part is designed into a specific application. Since mode selection is done with software, the system's "power up" software routine should sequentially establish the mode of each 4265 prior to "main body" program initiation. The mode selection is accomplished with the accumulator operand of the WMP command.

MODE DEFINITION AND TIMING

Detailed Description of Operating Modes

Table 1 provides a listing of the basic operating modes and the appropriate port configuration as determined by the Accumulator value sent to the 4265 during execution of the WMP instruction. A description of each mode is found in the following sections.

Table 1. Detailed Description of 4265 Operating Modes.

Mode	Port W	Port X	Port Y	Port Z			
0	Input port, unbuffered	Input port, unbuffered	Input port, unbuffered	Input port, unbuffered			
1	Bi-directional; Outputs enabled by signal Z0; When enabled output assumes value loaded by WR0.	Bi-directional; Outputs enabled by signal Z0; When enabled output assumes value loaded by WR1.	Unbuffered input port	Bit 0 Asynchronous input used to enable data out on Ports W, X.	Bit 1 Asynchronous input used to load data to Port W, X input buffers.	Bit 2 Output signal which is normally at V_{SS}. Goes to V_{DD1} on execution of WR 1. Returns to V_{SS} on trailing edge of Z0.	Bit 3 Output signal which is normally at V_{SS}. Goes to V_{DD1} on trailing edge of Z1 and remains at V_{DD1} until execution of RD1.
2	Bi-directional; Output enabled by signal Z0; When enabled output assumes value loaded by WR0.	Bi-directional; Outputs enabled by signal Z0; When enabled output assumes value loaded by WR1.	Buffered output port				
3	Bi-directional; Outputs enabled during WR1 cycle. Output assumes value loaded by WR0.	Bi-directional; Outputs enabled during WR1 cycle. Output assumes value loaded by WR1.	Buffered output port	Synchronous output. Normally at V_{SS}; goes to V_{DD1} during execution of WR 1.	Synchronous output. Normally at V_{SS}; goes to V_{DD1} during RD1 instructions.	Synchronous output. Normally at V_{SS}; goes to V_{DD1} during WR2 instructions.	Unassigned. Line is an output and can be set with WRM. Normally at V_{SS} after mode 3 set.
4	Buffered output port	Buffered output port	Buffered output port	Buffered output port			
5	Unbuffered input port	Buffered output port	Buffered output port	Buffered output port			
6	Unbuffered input port	Unbuffered input port	Buffered output port	Buffered output port			
7	Unbuffered input port	Unbuffered input port	Unbuffered input port	Buffered output port			
8	Buffered output port	Buffered output port	Buffered output port	Output signal normally at V_{SS}; goes to V_{DD1} during WR0.	Output signal normally at V_{SS}; goes to V_{DD1} during WR 1.	Output signal normally at V_{SS}; goes to V_{DD1} during WR2.	Unassigned output. Normally at V_{SS} after mode 8 set.
9	Buffered input port, loaded by signal Z0.	Buffered output port	Buffered output port	Input signal used to load Port W asynchronously.	Output signal normally at V_{SS}; goes to V_{DD1} during WR1.	Output signal normally at V_{SS}; goes to V_{DD1} during WR2.	Unassigned output. Normally at V_{SS} after mode 9 set.
10	Buffered input port, loaded by signal Z0.	Buffered input port, loaded by signal Z1.	Buffered output port	Input signal used to load Port W asynchronously.	Input signal used load Port X asynchronously.	Output signal normally at V_{SS}; goes to V_{DD1} during WR2.	Unassigned output. Normally at V_{SS} after mode 10 set.
11	Buffered input port, loaded by signal Z0.	Buffered input port, loaded by signal Z1.	Buffered input port, loaded by signal Z2.	Input signal used to load Port W asynchronously.	Input signal used to load Port X asynchronously.	Input signal used to load Port Y asynchronously.	Unassigned output. Normally at V_{SS} after mode 11 set.
12	Buffered output port, loaded by SRC instructions—contains upper 4-bits of SRC data.	Buffered output port, loaded by SRC instructions—contains lower 4-bits of SRC data.	Bi-directional; Outputs enabled at any WR instruction; input port unbuffered.	Output signal normally at V_{SS}; goes to V_{DD1} during any WR instruction.	Output signal normally at V_{SS}; goes to V_{DD1} during any RD instruction.	Output signal which is loaded with address bit corresponding to WR or RD operation.	Output signal which is loaded with address bit corresponding to WR or RD operation.
13	Buffered output port, loaded by SRC instructions—contains upper 4-bits of SRC data.	Buffered output port, loaded by SRC instructions—contains lower 4-bits of SRC data.	Bi-directional; Outputs enabled by signal Z0; Inputs loaded by signal Z1.	Asynchronous input used to enable data out on Port Y.	Asynchronous input used to load data to Port Y input buffers.	Output signal normally at V_{SS}; goes to V_{DD1} on execution of WR instruction. Returns to V_{SS} on trailing edge of Z0.	Output signal normally at V_{SS}; goes to V_{DD1} on trailing edge of Z1 and remains at V_{DD1} until execution of RD instruction.
14	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.
15	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.

a. Reset Mode – Mode 0

WMP Operand – 0000

Mode Description: The Reset Mode provides for a programmable reset. Reset will clear all I/O buffers; however, reset will not clear the chip select flip-flop. Hence, the 4265 will remain selected and enabled after a programmable reset. A negative 1 level (V_{DD}) on the RESET pin will cause a response similar to the Reset Mode. The only difference is that the 4265 will be enabled but deselected.

Port Description: Ports W, X, Y, and Z are unbuffered input. Hence, they can be read with RD0-3, transferring the state of the port lines into the accumulator. A positive "1" (V_{SS}) will appear in the accumulator as a negative true "1" (V_{DD}). Port Y will also respond to the RDM, SBM and ADM instructions.

b. 8-Bit Asynchronous I/O Mode with Input – Mode 1

WMP Operand – 0001

Mode Description: The 8-bit I/O mode is used to transfer bi-directional data bytes between the MCS-40™ and the peripheral circuits. Four control lines (Port Z) allow an asynchronous information transfer. Two signals are associated with the input function and two with the output function. Port Y is defined as an unbuffered input.

Port Description

Port W, X — These two ports are combined to transfer 8-bits of I/O under asynchronous control of Port Z. Port W will be loaded with a WR0 and Port X will be loaded with WR1. The WR1 will initiate the write "handshake" on Port Z. When the two ports are interrogated, a sequential RD0 and RD1 will cause the IA line to be deactivated.

Port Y — This port is an unbuffered input, interrogated with an RD2, RDM, ADM or SBM instruction.

Port Z

Z0 OA — Output acknowledge to the 4265 from the users logic. This signal is activated by the users logic (made negative) in response to the OI signal. The OA signal will enable the 4265 output buffer onto Ports W and X. It should be sufficiently long to allow the transfer.

Z2 OI — Output initiate from the 4265. This signal will be generated when Port X has been loaded via a WR1. Port W and Port X should be loaded in the WR0-WR1 sequence. When the OI signal is active, the external device will request data with the OA. The trailing edge of OA will cause the 4265 to remove the OI. If no OA response is received, OI will be active until the next WR0, where it will be removed until the next WR1.

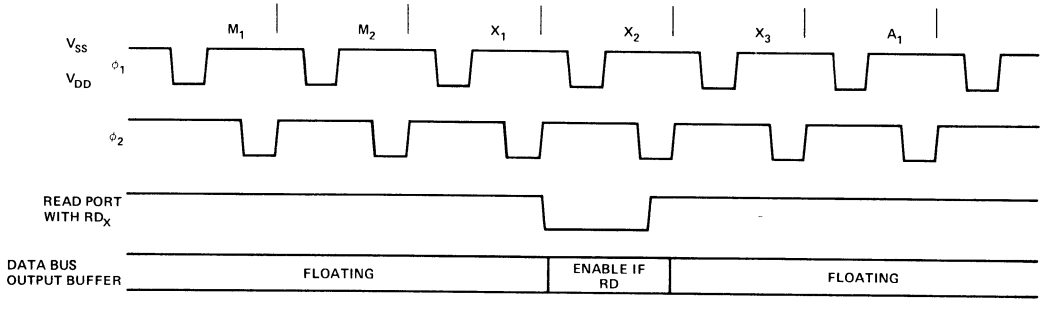


Figure 1. 4265 Mode 0 Timing.

Z1 II Input initiate to the 4265 from the users logic. The signal will be used as a strobe signal to latch the 8-bit contents of the Port W, X lines into the respective buffers. Data is transferred on the negative to the positive transition. This transition will cause the IA signal to be set.

Z3 IA Output from the 4265.
The IA signal will transition to the positive state when an RD1 command is executed. This indicates that the processor has interrogated Port W, X buffer. The processor should read the data in the sequence of RD0 followed by an RD1.

c. 8-Bit Asynchronous I/O Mode with Output – Mode 2

WMP Operand – 0010

Mode Description: Same as for Mode 1, except Port Y is a buffered output port.

Port Description: Port W, X, Z; same as for Mode 1. Port Y: This port is a buffered output port which can be loaded with a WR2 instruction and can be read by an RD2, RDM, ADM, and SBM.

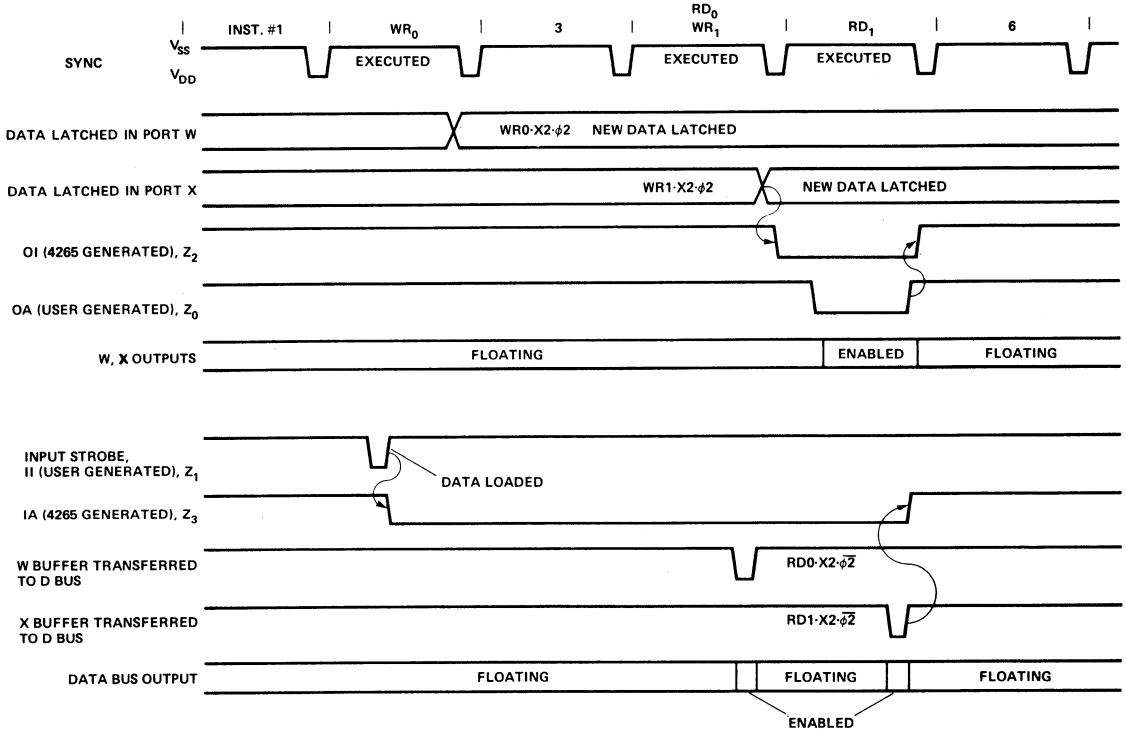


Figure 2. 4265 Modes 1 and 2 Timing.

d. 8-Bit Synchronous I/O Mode with Output – Mode 3

WMP Operand – 0011

Mode Description: This mode is functionally similar to Modes 1 and 2 in terms of its byte transfer feature. However, the transfer control is synchronous. Port W, X are buffered outputs or unbuffered inputs, depending on the direction of transfer. Port Z provides the synchronous strobe control. Port Y is a buffered output port.

Port Description

Port W, X — These two ports are combined to transfer bi-directional 8-bit information under synchronous control. Output data should be loaded into Ports W, X with the WR0-WR1 sequence. The input of information should be sequentially read with an RD0 followed by an RD1.

Port Y — This port is a 4-bit output port. Information is valid during the output strobe of a WR2 command. The output strobe is the Z2 line of the Z port. This port may also be read with an RD2, RDM, ADM and SBM.

Port Z

Z0 OS — Output strobe from 4265. This line is valid during a WR1 command. Information from the output buffers of Ports W and X is present at Ports W and X output lines only during the signal.

Z1 IS — Input strobe from 4265. This line is valid during an RD0 command. Information is taken off the Port W, X lines and is latched in the Port W, X buffers. The RD0 will read the information pertaining to Port W. RD1 will input information pertaining to Port X. The ports must be read by RD0 followed by an RD1. Data will be latched in the W and X Ports with the RD0. Information should be valid at the trailing edge of IS.

Z2 YS — Port Y output strobe from the 4265. This line is valid during a WR2 command. Information will be valid at the Port Y output buffer during this strobe.

Z3 — This line is not used. It can be bit set/reset under program control.

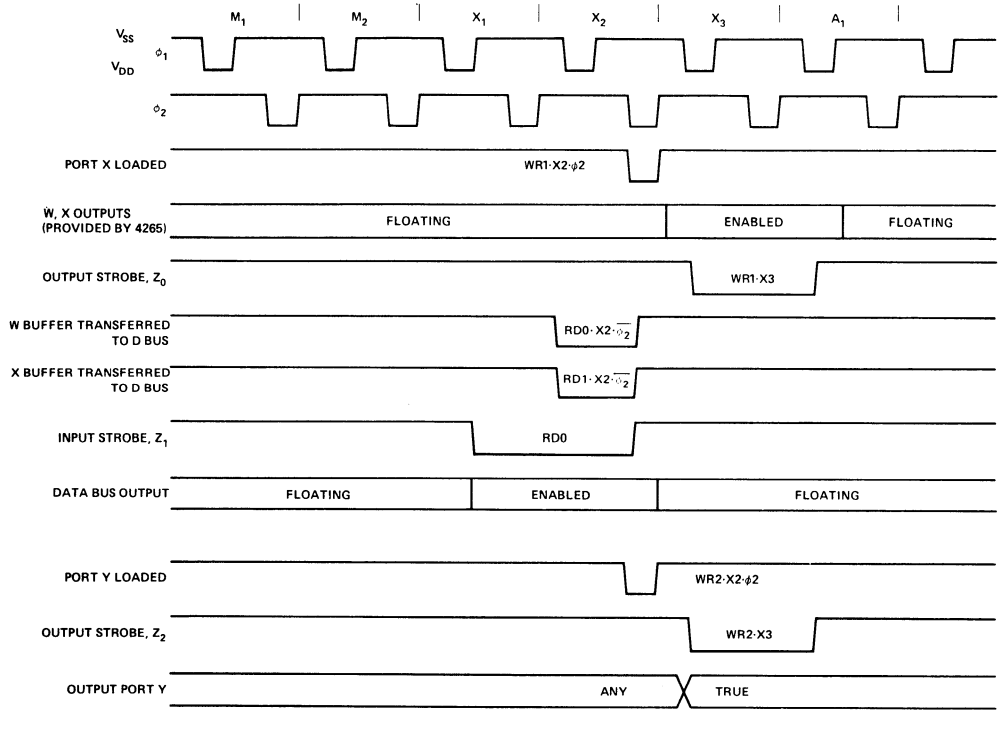


Figure 3. 4265 Mode 3 Timing.

e. Four Port Programmable I/O Modes – Modes 4-7

WMP Operand – 0100-0111

Mode Description: These modes consist of four combinations of static buffered outputs and unbuffered inputs. When combined with the Reset Mode, all combinations of inputs and outputs on four ports are possible.

Port Description: The following five modes have static buffered outputs (0) or unbuffered inputs (I).

WMP	Port:	W	X	Y	Z
0100		0	0	0	0
0101		I	0	0	0
0110		I	I	0	0
0111		I	I	I	0
0000 (reset mode)		I	I	I	I

Those ports of Y and Z designated outputs are subject to bit set/reset capability. All output buffers may be read with the respective RDx (RD0-RD3). Port Y will respond to RDM, ADM and SBM in addition to RD2.

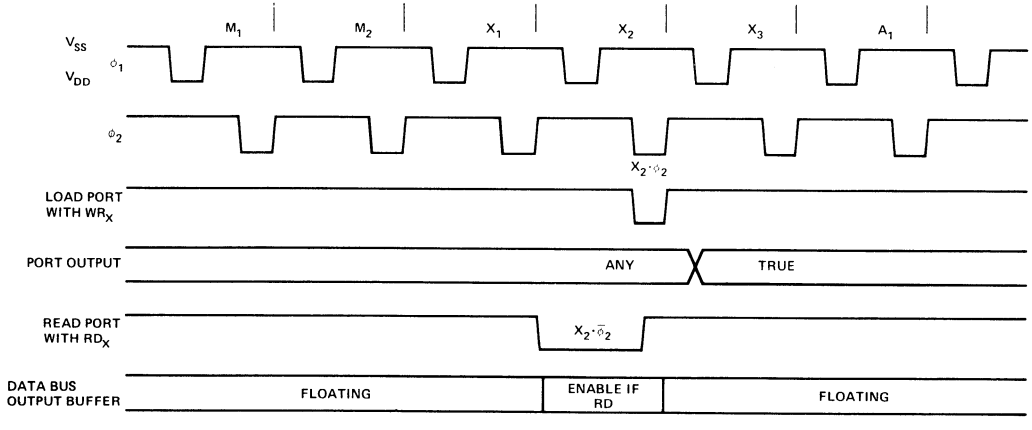


Figure 4. 4265 Modes 4-7 Timing.

f. Three Port Programmable I/O Mode with Synchronous Output and Asynchronous Input Port – Modes 8-11

WMP Operand – 1000-1011

Mode Description: Each 4-bit port can be configured as a buffered input or buffered output port and each has its own control line for synchronizing data transfers. As an example, if in Mode 8, when the processor executes a WR0 instruction, 4-bits of data are transferred to the Port W output buffer and subsequently to the Port W output lines. Output Strobe Z0 serves as a data valid signal which can be used by external logic to latch the data. In Mode 11, Input Strobe Z0 is used to latch the 4-bit data appearing on the Port W lines into the Port W input buffer. The Input Strobe is user generated.

Port Description: The following five modes have synchronous outputs (0) or asynchronous inputs (1):

WMP	Port:	W	X	Y	Z0	Z1	Z2	Z3
1000		0	0	0	W	W	W	X
1001		I	0	0	R	W	W	X
1010		I	I	0	R	R	W	X
1011		I	I	I	R	R	R	X

Where: R = input strobe independent of instruction executed
W = output strobe (WR0-2) from 4265
X = not used

Port Y will respond to RDM, SBM and ADM in the same way as an RD2. Z3 is unused and may be bit set/reset. All output buffers may also be read with the respective RDx.

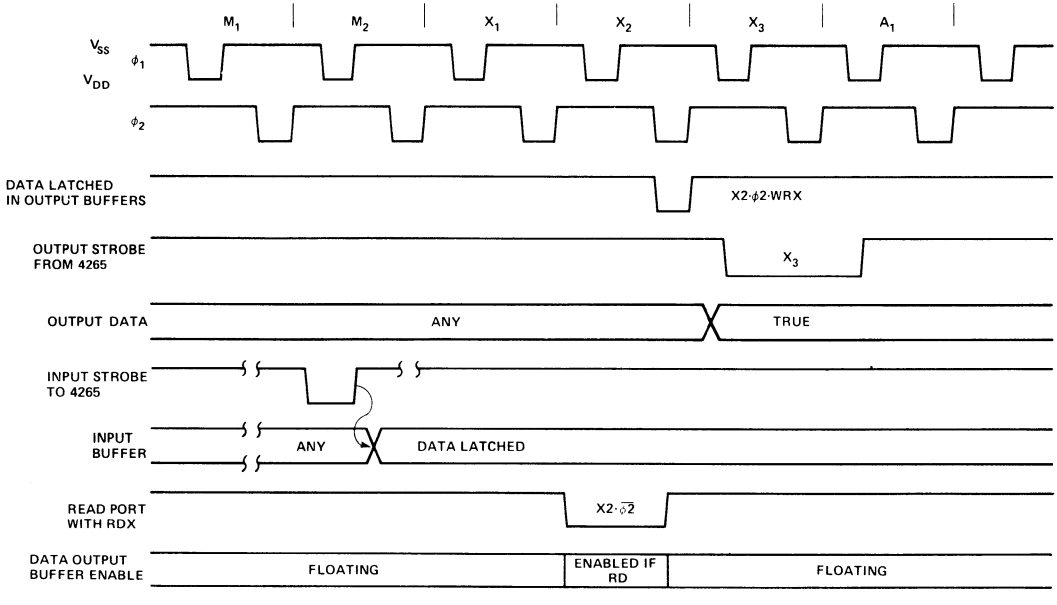


Figure 5. 4265 Modes 8-11 Timing.

g. 4-Bit I/O with 8-Bit SRC Address and 4-Bit Synchronous Control Port – Mode 12

WMP Operand – 1100

Mode Description: In this mode, the most recent 8-bit SRC operand is displayed on Port W and X. The 4265 will treat all SRC instructions as being valid as long as the CM-RAM line for this 4265 has been selected by an appropriate DCL (Designate Command Line) instruction. Ports W and X will change each time they receive an SRC and CM-RAM. The 4-bit data port (Port Y) will perform bi-directional synchronous I/O. The port output buffer may be loaded with a WR0-3 and the port input buffer will be read with RD0-RD3, RDM, SBM or ADM. The control port will provide mutually exclusive input or output strobes depending on the current instruction. Two of the control lines may be used for device selection. This mode can be used to interface up to 1K of external storage (RAM-2111, 4101, 5101) or a multitude of external I/O devices. Once this mode is programmed, all SRC values will not be treated as 4265 selection or deselection instructions.

Port Description

Port W, X — This port will display the most recent SRC and will be altered with each SRC when selected. Otherwise, the output is static.

Port Y — This is a bi-directional data port that will latch data with a RD0-RD3, RDM, ADM, and SBM. The port will output data with a WR0-WR3.

Port Z

Z0 $\overline{OS}$ — Output strobe from 4265. Active during WR0-WR3. Data will be valid during this strobe.

Z1 IS — Input strobe from 4265. Active during RD0-RD3, RDM, SBM, and ADM. The leading edge of this strobe will cause the user to provide valid data to be latched by Port Y by the trailing edge of IS.

Z2, Z3 — 2-bit address port used for memory or device selection. Both lines will be preset to 00 by selection of this mode. They will retain the value of the previous RDx or WRx instruction so that each selection can respond to RDM, SBM and ADM. If, for example an I/O sequence consists of an RD3 followed by an ADM, Z3 and Z2 will be at 11 state by the RD3 and remain in that state for the ADM command. If the third I/O command is a WR0, the Z3 and Z2 will be placed to the 00 state.

Effect of RDx and WRx Instructions:

Z3	Z2	
0	0	RD0, WR0
0	1	RD1, WR1
1	0	RD2, WR2
1	1	RD3, WR3
No Change		RDM, ADM, SBM

(Positive True)

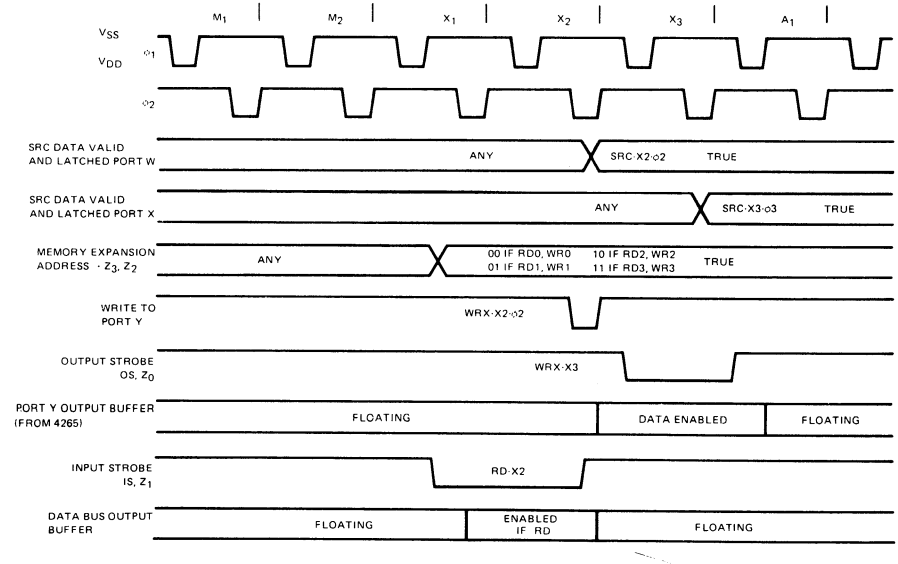


Figure 6. 4265 Mode 12 Timing.

h. 4-Bit I/O Mode with 8-Bit Address Port and 4-Bit Asynchronous Control Port – Mode 13

WMP Operand – 1101

Mode Description: This mode is functionally similar to Mode 12. Port W, X are loaded with the SRC value. Port Y is a bi-directional data port. Port Z is a 4-bit asynchronous control port similar to Mode 1 and 2.

Port Description

Port W, X		Same as Mode 12.
Port Y		Bi-directional port similar to Port W and Port X in mode 1.
Port Z		
Z0	OA*	Output acknowledge to 4265.
Z2	OI*	Output initiate from 4265, active during WRx.
Z1	II*	Input initiate to 4265.
Z3	IA*	Input acknowledge from 4265 active during RDx, RDM, ADM or SBM.

*Refer to Mode 1, Port Z. Note that in mode 13, Port Z controls data transmission in Port Y, not Ports W and X.

i. Disable/Enable

WMP Operands 1110 and 1111 do not cause mode change; they disable or enable the 4265 GP I/O.

WMP 1110 - chip disable:

a. All output buffers are disabled - I/O lines are in floating conditions.
b. The 4265's status (mode, chip select FF, data buffers) is not changed. Hence:
   1. Previous buffered inputs can be read by the CPU from designated ports (a disabled 4265 cannot have its input buffers loaded).
   2. Data on unbuffered inputs can be read directly from external lines.
   3. Previous buffered outputs can be changed on designated ports.
   4. Bit set/reset can be initiated.
   5. Any mode change can be initiated.
   6. The chip can be deselected by an SRC or by a RESET signal.

WMP 1111 - chip enable:
Restoration of normal operation, according to existing mode.

Note: When the 4265 is transferred from reset mode to any other mode, the chip is automatically enabled, so that no programmed enabling is required after reset.

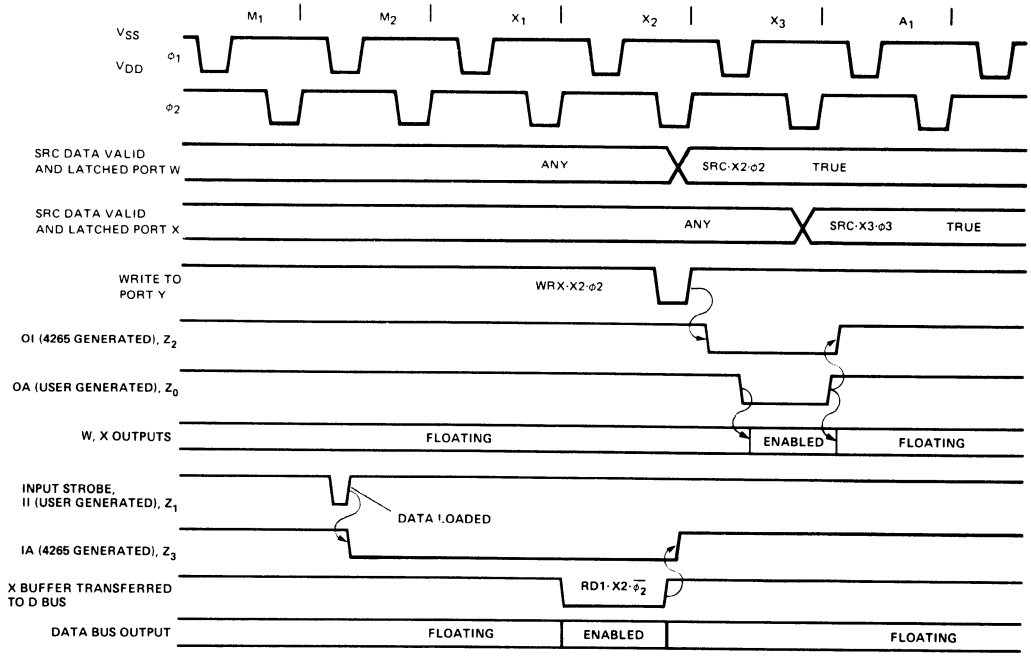


Figure 7. 4265 Mode 13 Timing.

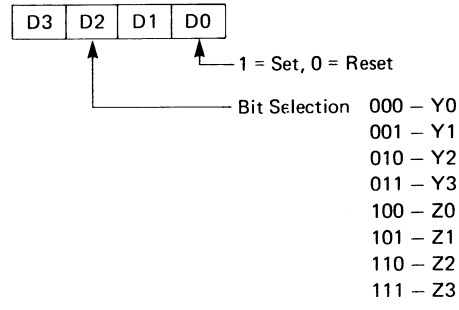
An unselected 4265 can have its input buffers loaded by a user generated strobe if it is in a buffered input mode. A disabled 4265 cannot have its input buffers loaded. Execution of a RDx instruction will result in transfer of the contents of the appropriate input or output buffer for a previously buffered port regardless of whether the 4265 is enabled. If the input was previously unbuffered and the 4265 is disabled, the contents of the port I/O lines will be transferred to the CPU with an RDx. DISABLE and ENABLE do not cause a change from a previously designated mode.

4265 States After Reset and Mode Change

A reset 4265 is automatically enabled and is in Mode 0. If reset occurs by means of external RESET signal, the 4265 will also be deselected. Any mode change which changes Port Z to a control port will reset the Port Z output buffers to their "off" state (V_{SS}). Z_2 and Z_3 in mode 12 are an exception in that these lines go to an inactive state of V_{DD1}. Note that Port Z is a control port in all modes except modes 4-7 and RESET mode. Any mode change which leaves Port Z in a non-control port will leave Port Z output buffers in their previous state.

Bit Set/Reset Operation

This function is performed by decoding the accumulator operand of the WRM instruction. This function can be used in any output port of the programmed configurations and allows individual bit control on Ports Y and Z. Decoding of the WRM operand is as follows:



Care should be taken when bit setting and resetting control bits of Port Z as these bits will also be changing as a function of their synchronous or asynchronous control functions.

4265 I/O Instructions

Table 2 provides a summary of MCS-40 I/O instructions used with the 4265.

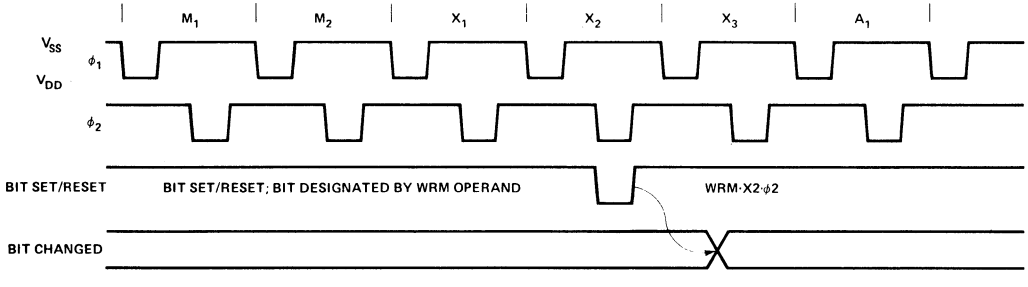


Figure 8. Bit Set/Reset Operation Timing.

Table 2. 4265 I/O Instruction.

Hex Code	MNEMONIC	OPR D_3 D_2 D_1 D_0	OPA D_3 D_2 D_1 D_0	DESCRIPTION OF OPERATION		
				Mode Independent Operations		
E0	WRM	1 1 1 0	0 0 0 0	The port Y or port Z bit designated by D_3 D_2 D_1 of the accumulator is set or reset according to D_0 (1=set, 0=reset).[1]		
E1	WMP	1 1 1 0	0 0 0 1	Sets the mode of the 4265 to the value contained in the accumulator.[2]		
				Mode Dependent Operations		
				Mode 1-3	**Mode 0, 4-11**	**Mode 12 and 13**
2-	SRC	0 0 1 0	R R R 1	For modes 0-11, the contents of register pair RRR are used to select the 4265 chip (first two bits of first register will contain 10 or 11, depending on chip address)		(RRR_{even})→ Port W (RRR_{odd})→ Port X
E4	WR0	1 1 1 0	0 1 0 0	(ACC)→ Port W	(ACC)→ Port W[1]	(ACC)→ Port Y
E5	WR1	1 1 1 0	0 1 0 1	(ACC)→ Port X	(ACC)→ Port X[1]	(ACC)→ Port Y
E6	WR2	1 1 1 0	0 1 1 0	(ACC)→ Port Y[1]	(ACC)→ Port Y[1]	(ACC)→ Port Y
E7	WR3	1 1 1 0	0 1 1 1	—	(ACC)→ Port Z[1,3]	(ACC)→ Port Y
EC	RD0	1 1 1 0	1 1 0 0	(Port W)→ ACC	(Port W)→ ACC	(Port Y)→ ACC
ED	RD1	1 1 1 0	1 1 0 1	(Port X)→ ACC	(Port X)→ ACC	(Port Y)→ ACC
EE	RD2	1 1 1 0	1 1 1 0	(Port Y)→ ACC	(Port Y)→ ACC	(Port Y)→ ACC
EF	RD3	1 1 1 0	1 1 1 1	(Port Z)→ ACC	(Port Z)→ ACC	(Port Y)→ ACC
E9	RDM	1 1 1 0	1 0 0 1	(Port Y)→ ACC	(Port Y)→ ACC	(Port Y)→ ACC
EB	ADM	1 1 1 0	1 0 1 1	(Port Y)+(ACC) +CY→ACC	(Port Y)+ACC +CY→ACC	(Port Y)+ACC +CY→ACC
E8	SBM	1 1 1 0	1 0 0 0	(ACC)−(Port Y) −CY→ACC	(ACC)−(Port Y) −CY→ACC	(ACC)−(Port Y) −CY→ACC

NOTES:
1. Action if Port is designated as Output Port; otherwise, no action.
2. WMP 1110 disables all I/O ports. WMP 1111 enables all I/O ports. In both cases, the mode is not changed.
3. No action in Modes 8-11.

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400nsec; $t_{\phi D2}$ = 150nsec; V_{DD1} = V_{SS} -5V; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Supply Current		35	50	mA	T_A = 25°C

INPUT CHARACTERISTICS

I_{LI}	Input Leakage Current			10	µA	
V_{IHD}	Data Bus Inputs	V_{SS}-1.5		V_{SS}+.3	V	
V_{IHIO}	I/O Port Inputs	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILD}	Data Bus Inputs	V_{DD}		V_{SS}-5.5	V	
V_{ILIO}	I/O Port Inputs	V_{DD}		V_{SS}-4.2	V	
$V_{IL/R,CM}$	Reset Input, CM-RAM Input	V_{DD}		V_{SS}-4.2	V	
$V_{IH/R,CM}$	Reset Input, CM-RAM Input	V_{SS}-1.5		V_{SS}+.3	V	
V_{IHC}	Input High Voltage Clock	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clock	V_{DD}		V_{DD}-13.4	V	

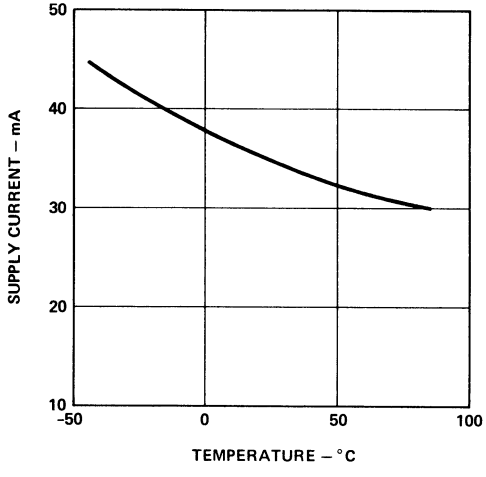
OUTPUT CHARACTERISTICS

V_{OHD}	Data Bus Outputs	V_{SS}-.5	V_{SS}		V	
V_{OHIO}	I/O Port Outputs	V_{SS}-.5			V	I_{OH} = -100µA
V_{OLD}	Data Bus Outputs	V_{SS}-12		V_{SS}-6.5		Capacitive Load
V_{OLIO}	I/O Port W,X,Y Outputs			V_{DD1}+.45		I_{OL} = 500µA
V_{OLZ}	I/O Port Z Outputs			V_{DD1}+.45		I_{OL} = 1.6mA
$R_{OH/D}$	Output Resistance, Data Bus High Level		150	250	Ω	V_{OUT}=V_{SS}-.5V
$R_{OH/IO}$	Output Resistance, I/O Port W,X,Y,Z High Level		1200	2000	Ω	V_{OUT}=V_{SS}-.5V
$I_{OL/WXY}$	I/O Port W,X,Y Sink Current	0.5			mA	V_{OUT}=V_{DD1}+0.45V
$I_{OL/Z}$	I/O Port Z Sink Current	1.6			mA	V_{OUT}=V_{DD1}+0.45V

CAPACITANCE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{ϕ}	Clocks ($\phi1$, $\phi2$)		10	15	pF	$V_{IN} = V_{SS}$. All other pins at V_{SS}.
$C_{D.B.}$	Data Bus		10	15	pF	
C_I	CM, RESET, SYNC		3	10	pF	
C_{WXY}	I/O Ports W,X,Y		5	10	pF	
C_Z	I/O Port Z		10	15	pF	

I_{DD} SUPPLY CURRENT vs. TEMPERATURE



A.C. Characteristics

T_A = 0°C to 70°C, V_{SS} -V_{DD} = 15V ±5%.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Time			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF

I/O Ports ($C_{PORT\ W,X,Y}$ = 100 pF, $C_{PORT\ Z}$ = 50 pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{D0}	Output Settling Time		350	1200	nsec	Static Output Ports [1]
t_{D1}	Output Settling Time		400	1200	nsec	Ports W,X, Mode 1,2
t_{OH0}	Output Hold Time	80	400		nsec	Port Y, Mode 13
t_{D2}	Output Settling Time		400	1200	nsec	Ports W,X, Mode 3
t_{OH2}	Output Hold Time	550			nsec	Port Y, Mode 12
t_{D3}	O. S. Settling Time		300	650	nsec	Modes
t_{OH3}	O. S. Hold Time	550			nsec	3,8,9,10,12
t_{D4}	I. S. Delay		200	400	nsec	Z1, Modes 3,12
t_{DPS}	Page Select, Output Settling Time		250	550	nsec	Z2,Z3, Mode 12
t_{IS0}	Input Set Time	700	450		nsec	Unbuffered Input
t_{IH0}	Input Hold Time	100	-30		nsec	Ports W,X,Y
t_{IS1}	Input Write Time	900			nsec	Buffered Inputs (Ports
t_{IH1}	Input Hold Time	550			nsec	W,X Modes 1,2 Port Y Mode 13)
t_{DSR}	Bit Set/Reset Settling Time			900	nsec	
$t_{DOI/IA}$	OI,IA Delay Time			950	nsec	Z2,Z3, Modes 1,2,13 [2]
t_{PWII}	II Width			450	nsec	Modes 1,2,13
t_{PWIS}	IS Width	650			nsec	Modes 9,10,11 (4265 generated)

Notes: 1. t_{D0}: all output ports, modes 4-10; Y port, modes 2, 3.
2. $t_{DOI/IA}$: the maximum delay of any OI, IA edge with respect to its generating signal (strobe edge, clock edge, etc.). Refer to Figure 11 for generating signals and timing diagram.

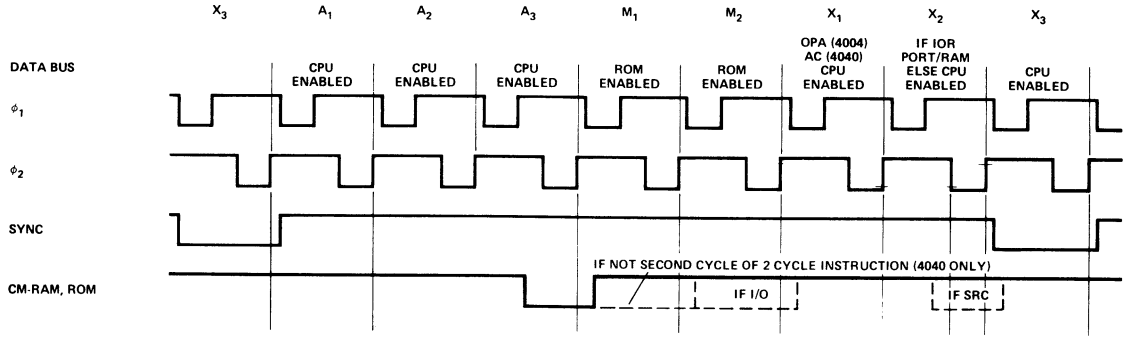


Figure 9. Timing Diagram.

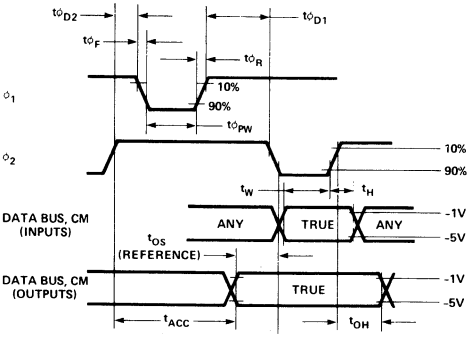


Figure 10. Timing Detail.

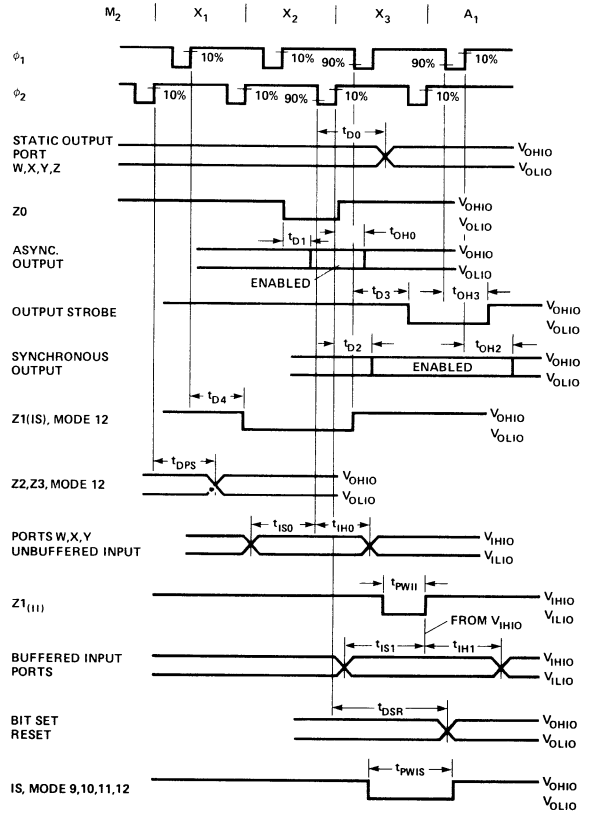


Figure 11. 4265 I/O Timing Diagram.

4269
PROGRAMMABLE KEYBOARD DISPLAY DEVICE

Keyboard Features:

- Programmable to Interface to Encoded Keyboard (8-bit code), 64-Key Scanned Keyboard (expandable to 128 keys) or Sensor Matrix (64 sensors)
- 8 Character FIFO Character Buffer (or RAM in Sensor Mode)
- 2 Key Rollover and Key Debounce
- External Interrupt Line to Indicate When a Character Has Been Entered in Character Buffer

Display Features:

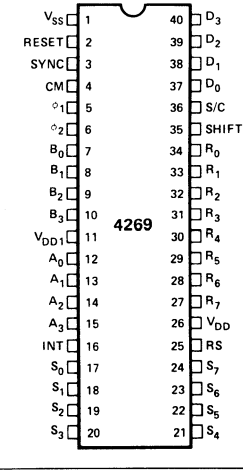
- Programmable to Interface to Individually Scanned Displays or Burrough's Self-Scan* Drive (16, 18, or 20 Characters)
- Two 16 x 4 Display Registers Recirculated Synchronously with Keyboard Scan Lines to Give Automatic Display Refresh
- Display Registers Loadable and Readable Selectively or Sequentially
- 40 Pin Dual In-Line Package
- Standard Operating Temperature Range of 0° to 70°C
- Also Available with -40°C to +85°C Operating Range

The 4269 has two separate and distinct sections: the keyboard section and the display section. The keyboard section can interface to a range of devices from a matrix of toggle or thumb switches such as found on an instrument panel up to a full typewriter style keyboard. The display section can interface to a range of devices from an array of individual LED indicators up to a gas discharge alphanumeric display.

The 4269 Programmable Keyboard Display (PKD) relieves the 4004 or 4040 CPU from continuously scanning a switch array or refreshing a display under software control. This greatly expands the CPU throughput. The 4269 can scan up to an 8 x 8 keyboard or sensor matrix (or a 2 x 8 x 8 keyboard with the use of the shift or control key input). The display portion can continuously refresh either a single 16 x 8 alphanumeric display; a single 8 x 8 alphanumeric display; a dual 16 x 4 digit display; a single 32 x 4 digit display; a 16 x 6, 18 x 6 or 20 x 6 alphanumeric gas discharge display such as the Burroughs Self-Scan*; or an array of 128 indicators.

*Self-Scan is a registered trademark of the Burroughs Corporation.

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Designation	Function
37-40	D0-D3	Bi-directional data bus. All address, instruction and data communication between the CPU and the PKD are transmitted on these 4 pins.
5-6	ϕ_1-ϕ_2	Non-overlapping clock signals which are used to generate the basic chip timing.
2	RESET	RESET input. A low level (V_{DD}) applied to this input resets the PKD.
1	V_{SS}	Most positive supply voltage.
26	V_{DD}	Main power supply pin. Value must be V_{SS} - 15V ±5%.
3	SYNC	Synchronization input signal driven by SYNC output of the CPU.
4	CM	Command input driven by a CM-RAM output of processor.
17-24	S0-S7	These pins are scan outputs which are used for driving either the key switch or sensor matrix and/or for strobing the display digits. Each line is mutually exclusive, active high (V_{SS}), open drain.
25	RS	The RS pin is toggled for each complete scan of the S drive. This allows for the scan of 16 digits of display data. RS=V_{SS} for the last 8 digits. This line is open drain.
12-15 7-10	A0-A3 B0-B3	These two ports provide two 16 x 4 recirculating display register outputs which are synchronized to the S drive scan. In the gas discharge display mode, A3 is reset and A2 is the clock to the gas discharge display. The 16, 18, or 20 recirculating data characters (6 bits wide) are not synchronized with the S drive scan in the gas discharge mode. These lines are active high.
34-28	R0-R7	These pins are the return sense inputs which are connected to the 8 drive lines via the scanned key or sensor matrix. They are pulled to a low state (V_{DD}) in the sensor mode, pulsed low (V_{DD}) in the scanned keyboard mode, and pulled high upon switch closure. They are floating in the encoded keyboard mode.
35	SHIFT	This is the shift input. It is active high (V_{SS}). This pin is functional only in the scanned keyboard mode.
16	INT	This output is used to indicate when a keyboard or sensor character has been entered into the buffer. It is active low (V_{DD1}), open-sourced and may be "OR" -ed with other 4040 interrupt inputs.
11	V_{DD1}	Supply voltage for display register ports A and B and INT.
36	S/C	This pin is the control key input from the keyboard in the scanned mode. In encoded keyboard mode, this pin is used to input the strobe pulse from an external keyboard encoder. The strobe is an active high pulse.

FUNCTIONAL DESCRIPTION

General

The 4269 Programmable Keyboard/Display (PKD) device provides an intelligent interface between an MCS-40 CPU and the keyboard and display portions of an MCS-40 design. The 4269's functions thus allow the use of sophisticated keyboards and displays without placing a large load on the CPU.

The MCS-40 data bus will provide the path for information transfer between the PKD and the 4040 or 4004 CPU. The PKD can be programmed to operate in one of three input modes and one of four output modes as defined by an instruction from the CPU. The modes are:

Input	Sensor, Scanned Keyboard, Scanned Encoded Keyboard
Output	Individually Scanned Display Drive Self-Scan Drive: 16 Characters 18 Characters 20 Characters

The 4269 resides on a CM-RAM line of an MCS-40 system and has a fixed RAM address, #1. Hence, there can be up to four PKD per system without additional logic, one per CM-RAM. The PKD can be accessed with the MCS-40 I/O instruction set to interrogate the keyboard buffer FIFO/sensor RAM and load or read the display registers.

The following is a list of the major keyboard features of the 4269:

1. Switch matrix, organized as an 8 x 8 scanned matrix with shift or control inputs allowing for up to 128 key inputs.
2. Two key roll over; N-key roll over capability if provided by encoded keyboards.
3. Eight character first-in-first-out (FIFO) character buffer (or RAM in the Sensor Mode).
4. External interrupt line to indicate when a character has been entered in the buffer.
5. Fixed key bounce delay of approximately 11 msec in the scanned keyboard mode @ 740 kHz MCS-40 clocks.
6. Status buffer to indicate the number of characters in the keyboard FIFO and keyboard character over-entry.
7. Sensor matrix interface with up to 64 intersections.

The 4269's major display features are:

1. Two 16 x 4 display registers which are recirculated synchronously with keyboard scan lines (at a scan frequency of 180 Hz). This allows for a free standing, scanned readout composed of individual displays.

2. Capability to drive 16, 18, or 20 character gas discharge displays directly via a 20 x 6 display register.
3. Registers are loadable and readable selectively or sequentially.

Mode Selection

The CPU communicates with the 4269 PKD by first selecting it with an SRC (Send Register Control) instruction. The first two bits of the index register pair referenced by the SRC contain 01, the binary address of the 4269 on the CM-RAM line. The 4269 is disabled until it is addressed by a first SRC. After the first SRC, a WR0 instruction is used to set the keyboard and display modes of the 4269 PKD. The CPU's accumulator will contain the information used for setting the PKD modes. The definition of a WR0 as used for a 4269 is given below:

Mnemonic	Instruction Code
WR0	1110 0100

Set the input mode and output mode of the 4269 according to the value contained in the accumulator as follows:

D_3D_2

0 0 Individual, Scanned Displays
0 1 Gas Discharge, 20 Characters
1 0 Gas Discharge, 18 Characters
1 1 Gas Discharge, 16 Characters

D_1D_0

0 0 Sensor, Scanned
0 1 Scanned Keyboard
1 0 Encoded Keyboard, Not Scanned
1 1 Not Used

After the 4269 has been reset by the external RESET signal, the keyboard input mode is set to scanned keyboard mode and the display output mode is set to gas discharge, 16 character mode. Thus, if these modes are the desired input and output modes, it is not necessary to execute the WR0 mode setting instruction.

Internal Display Registers and Pointer

The 4269 has two 16x4 display registers referred to as Display Register A and Display Register B. These two registers can be operated in the individual, scanned display mode as:

1. Two 16 x 4 hexadecimal displays;
2. One 32 x 4 hexadecimal display;
3. One 8 x 8 alphanumeric display;
4. One 16 x 8 alphanumeric display; or
5. An array of 128 indicators.

In the gas discharge modes, the A and B registers are combined and operated as a 6 x 16, 6 x 18 or 6 x 20 register. For a given 6-bit character, the least significant 4-bits will be located in a 4-bit B register location and the two most significant bits in D_1 and D_0 of the corresponding A register location.

For operations on the display registers, the 4269 PKD maintains an internal display register pointer which points to a 4-bit character in the A or B display register.

For the individual, scanned display mode, CPU I/O instructions can be addressed to either Display Register A or Display Register B, according to the register selected by an SRC instruction preceding the I/O instruction. The internal display register pointer can then be set or incremented for addressing characters in either the A or B register.

For gas discharge modes, the internal pointer can be automatically incremented, in an alternating pattern between registers A and B. The alternation pattern is A_0, B_0, A_1, B_1, etc.

In the individual, scanned display mode, the 4-bit characters of Display Register A are outputted on the A_0-A_3 lines. The 4-bit characters of Display Register B are outputted on the B_0-B_3 lines. In the gas discharge modes, the A_0-A_1 and B_0-B_3 lines output the 6-bit character. The A_2 line serves as the clock to the gas discharge display and the A_3 line as the reset to the display.

Synchronization of Scan and Return Lines

In the scanned keyboard and scanned sensor modes a logical one is shifted through a field of zeros in eight Scan(S) lines. Each S Scan line can be used to source a row of eight keys or sensors. All rows of the contact keyboard or sensor matrix will be OR-tied to the eight Return (R) lines. Thus, since only one row will be enabled due to the synchronized ones in the Scan lines, each row of the keyboard or sensor matrix can be read into the Return lines and stored in the Keyboard FIFO/Sensor RAM at the proper RAM location. The 4269 will control all of these operations automatically once it is set to the appropriate keyboard mode.

The Scan Lines are also used in the individual, scanned display mode to select one of eight display characters. The display character itself will be outputted on the A_0-A_3 or B_0-B_3 output lines. The RS output line, which is toggled for each complete scan of the S lines, allows one of sixteen A or B register display characters to be addressed. Again, the 4269 will automatically control the operation of the S and RS lines to continuously read out the characters in the 4269's internal A and B Display Registers and thus continuously refresh the actual display devices.

Note that the Scan lines can be used with both the keyboard and display interfaces since both functions require the same function, i.e., a synchronized shifting of a logical one through a field of zeros.

Software Operation

The WR0 operates on the 4269 PKD completely independent of mode as it actually sets the mode as has already been described. The WR3 is mode independent except for a blanking code and operates as shown below:

WR3

Clears the keyboard/display logic and fills the display RAM with all blanks. The display outputs are also blanked. (Blank code is all logical "1"s for individual, scanned display mode and hex 20 for the gas discharge modes.)

MODE SPECIFIC OPERATIONS

Individual, Scanned Display Mode

The instructions which are used in the individual, scanned display mode are described below:

Mnemonic Instruction Code
SRC 0010 RRR1

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted for individual, scanned display mode as follows:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 0 0	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Display Register A with A outputs continuing to output the contents of Display Register A synchronized with the S Scan lines.
0 1 0 1	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Display Register B with B outputs continuing to output the contents of Display Register B synchronized with the S Scan lines.
0 1 1 0	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Register A and places the A output lines at V_{SS} level (blank). Display RAM contents are not modified.
0 1 1 1	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Register B and places the B output lines at V_{SS} level (blank). Display RAM contents are not modified.

WR1 1110 0101

Resets the internal display register pointer to 0 and forces display memory to blank state. Upper two bits of ACC select length of display as follows:

D_3

0 Display B is 16 nibbles deep.
1 Display B is 8 nibbles deep.

D_2

0 Display A is 16 nibbles deep.
1 Display A is 8 nibbles deep.

WRM 1110 0000

Loads the contents of the register addressed by the internal display register pointer with the contents of ACC; then advances the displayed data by one digit in relation to the scan line timing and increments the display register pointer.

RDM 1110 1001

Loads ACC with the contents of the register addressed by the display register pointer and then increments the display register pointer.

WMP 1110 0001

Loads the contents of the register addressed by the display register pointer with the contents of ACC.

RD3 1110 1111

Loads ACC with the contents of the display register pointed to by the display register pointer.

ADM 1110 1011

Adds the contents of the display register pointed to by the display register pointer to the accumulator with carry.

SBM 1110 1000

Subtracts the contents of the display register pointed to by the display register pointer from the accumulator with borrow.

NOTES:

1. If Display A or B is set to 8 nibbles deep, each digit of the display will have double the ON duty-cycle that it would have in the 16 nibble deep setting (360 Hz scan cycle vs. 180 Hz for 16 nibble deep).
2. External resetting initializes the Display A and Display B configurations to 16 nibbles deep and blanks the display outputs.
3. The displayed nibbles in the 8 deep configuration will be from the least significant 8 characters of the display register. The remaining eight words remain available for random data storage by the CPU.
4. The internal display register pointer will increment through all 16 register words, regardless of the display length (8 or 16) for WRM/RDM instructions unless the pointer is reset by an appropriate SRC instruction. In the WRM case, the Display Register A or B's entire contents (used and unused portions) will be rotated.
5. An interface to a 32 x 4 hexadecimal display requires only that software recognize the A and B Display registers as the upper and lower halves of a single display.
6. An interface to a 16 x 8 alphanumeric display requires that software load the upper and lower 4-bits in the A and B registers in an appropriate alternating pattern. SRC instructions will have to proceed each load or read instruction to select the A or B half of the character.
7. If the LSD of a 16 character display is assigned to be the 15th character scanned ($S_7 = V_{SS}$ and RS = V_{SS}), and the MSD, the first character (#0) scanned ($S_0 = V_{SS}$ and RS = V_{DD}), and if loading is started at display register character 0, successive WRM instructions will shift the display data from the LSD to the MSD as in a calculator. Note that data will then be read back MSD to LSD with the RDM instruction, starting at register 0.

Gas Discharge Modes

The instructions which are used in the gas discharge display modes are described below.

Mnemonic Instruction Code
SRC 0010 RRR1

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted for gas discharge modes as follows:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 0 0	$n_3n_2n_1n_0$	Selects the nth display register character of Display Register A with display outputs continuing to output the contents of Display Registers A and B.
0 1 0 1	$n_3n_2n_3n_0$	Selects the nth display register character of Display Register B with the display outputs continuing to output the contents of Display Registers A and B.
0 1 1 0	$n_3n_2n_1n_0$	Selects the nth display register character of Display Register A and blanks the A and B display output (with hex 20) with no modification of display RAM contents.
0 1 1 1	$n_3n_2n_1n_0$	Selects the nth display register character of Display Register B and blanks the A and B display output (with hex 20) with no modification of display RAM contents.

WR1

Resets the internal display register pointer to Display Register A position 0 and forces the Display Registers to the blank code.

Note: A WR1 should follow a WR0 which changes the display mode.

WRM 1110 0000

Loads the contents of the display register location addressed by the internal display register pointer with the contents of ACC; then advances the displayed data by one digit in relation to the scan line timing, and increments the display register pointer. The display register pointer alternates between the A and B registers.

RDM 1110 1001

Loads ACC with the contents of the display register location addressed by the display register pointer and then increments the display register pointer. The display register pointer alternates between the A and B registers.

WMP 1110 0001

Loads the contents of the display register location addressed by the display register pointer with the contents of ACC.

RD3 1110 1111

Loads ACC with the contents of the display register location pointed to by the display register pointer.

ADM 1110 1011

Adds the contents of the display register pointed to by the display register pointer to the accumulator with carry.

SBM 1110 1000

Subtracts the contents of the display register pointed to by the display register pointer from the accumulator with borrow.

NOTES:

1. The alternation pattern of the display register pointer is Display Register A position 0, Display Register B position 0, Display Register A position 1, etc.
2. The upper two (four) gas discharge characters, 16-17 (16-19), can be addressed only by incrementing the internal display register pointer above 15 by a WRM or RDM instruction in 18 (20) character gas discharge mode. If the internal display register pointer has been incremented above 15, then these characters can be read or written by a RD3 or WMP instruction.
3. Successive WRM commands will shift the output data (see gas discharge display output format below) one character forward in relation to the reset pulse. This will cause a wraparound shift left on the self-scan display. Hence, starting at register 0 and loading the display RAM will give a right-justified display — MSD first.

	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
	RST	CLK	D_5	D_4	D_3	D_2	D_1	D_0
BLANK CODE:	X	X	1	0	0	0	0	0

Figure 1. Gas Discharge Display Output Format.

4. RDM will not cause any display shifting. The read order is MSD to LSD with the MSD stored in display register 0.
5. If the display RAM is used as data RAM by the CPU, all 4 bits of Register A can be read and written, i.e., the A_3 and A_2 RAM positions are not actually modified in the RAM.

Scanned Sensor Mode

The instructions which are used in the scanned sensor mode are described below:

Mnemonic	Instruction Code	
SRC	0010	RRR1

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted for scanned sensor mode as follows:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 X X	$n_3n_2n_1$ X	n_3-n_1 indicates an 8-bit sensor group to be read.

WR2 1110 0110

Clears the FIFO/RAM logic and the INT line.

RD1 1110 1110

Loads into ACC the upper 4 bits of the 8-bit sensor RAM group previously addressed by an SRC instruction.

RD2 1110 1110

Loads into ACC the lower 4 bits of the 8-bit sensor RAM group previously addressed by an SRC instruction.

NOTES:

1. In this mode, the 4269 PKD will continuously input the 64 matrix intersections of the sensor into the FIFO/Sensor RAM, which is organized as a 64-bit RAM.
2. The INT line will become active (V_{DD1}) and remain active whenever at least one intersection remains a logical one in the Sensor RAM.
3. The sensor group number set by the SRC is loaded into the internal display register pointer. Display mode instructions which change the internal display register pointer thus change the sensor group address.

Scanned Keyboard and Encoded Keyboard Modes

The instructions which are used in the scanned keyboard and encoded keyboard modes are described below:

Mnemonic	Instruction Code	
SRC	0010	RRR1

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted as follows for scanned and encoded keyboard modes:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 X X	X X X X	SRC used only to select 4269.

WR2 1110 0110

Clears FIFO/RAM logic, the status buffer, and the INT line.

RD1 1110 1101

Reads the first nibble of the current FIFO register position.

RD2 1110 1110

Reads the second nibble of the current FIFO register position. FIFO register position is incremented to the next position.

RD0 1110 1100

Loads ACC with the FIFO status.

Notes:

1. The 4-bit FIFO status contains the number of valid characters (0-8) in the keyboard FIFO. However, in the event of an overrun, i.e., more than 8 characters entered, the 4-bit status will be set to a value of 15. The first eight characters entered prior to the overrun character will remain in the FIFO until cleared.
2. When a character is entered in the FIFO, the INT output pin wil go to V_{DD1}. When a character is read, the INT will change from V_{DD1} to V_{SS} (open) and back to V_{DD1} until the FIFO has been emptied. If a ninth character is inputted to the PKD before one complete character has been removed, the overrun status will be set. This will cause the INT line to remain active (V_{DD1}) even after all characters have been accessed. Overrun status can only be cleared by a WR2 or WR3 command (although the first eight FIFO characters can be read). This condition allows the user to detect an overrun condition if it occurs between the time the status buffer is checked and the time all characters have been read. It should be noted that an RD2 must be initiated after an RD1 to advance to the next FIFO word even if the second nibble is not desired.
3. For a 16-key Keyboard, successive RD2 instructions will be adequate for inputting the key code.

DESIGN CONSIDERATIONS

Display Modes

General Remarks

Each Display A and Display B output is capable of driving one standard TTL load. This is done by using a V_{SS} = +5, V_{DD} = -10V and V_{DD1} = GND. The V_{DD1} pin allows the PKD to interface to a variety of commercially available display arrays via a specified circuit. Gas discharge, phosphorescent, LED, and incandescent displays can all be used with a 4269. The interface requirements are determined by the selected display device. Current into each of the Display A and Display B output lines should not exceed 1.6mA.

The two 16 x 4 Display Registers A and B provide information in hexadecimal positive logic conventions. Hence, a 0000, negative logic V_{SS} on the data bus, will be 0000 (positive logic V_{DD1}) at the A and B display output. (The above is equivalent to one level inversion between the data outputs of the PKD and the CPU accumulator.)

Note that since the PKD is at address No. 1 on the CM-RAM line and that since the last 2 bits of the even register pair of an SRC instruction cause blanking or unblanking of the display and modification of the internal display register pointer, that addresses 01XX are not available for addressing other I/O ports on the same CM-RAM line as the one containing the PKD.

Individual, Scanned Display Mode

The digit selection is achieved by using the eight scan lines, S_0-S_7, and the display select line RS. The RS output is used to multiplex the eight scan strobes to give sixteen separate strobes for up to 16 digits of display.

It should be noted that the LSD output position of both Display Registers A and B is gated out coincidently with S_0 time of the scan register. Following digit positions are also coincident. This feature allows an interface to 8 x 8 or 16 x 8 displays. For the first eight display digit positions, the RS output is at open drain. The remaining eight of the 16 digit positions are output sequentially with RS at V_{SS}. Sufficient active on-time (V_{SS}) is allowed at the scan strobe line (S_0-S_7) to illuminate the displayed digit. Sufficient time is also allowed between segments to extinguish segment and prevent overlapped illumination. If the 8 digit mode is selected with the WR1 instruction, the LSD will be gated out every S_0 time – not every other time.

For an aesthetic display transition, the display register outputs can be placed into the blank mode (all outputs to V_{SS}) via an SRC during the loading of the display register. The outputs can then be unblanked via another SRC when the display register has been completely loaded.

Gas Discharge Modes (Self-Scan)

An approximate 100 μsec period, 50% duty cycle clock will be provided to the gas discharge display. A reset pulse – one clock period long – will be generated every 112th clock period for the 16/18 digit displays or every 140th clock period for 20 digit displays. Character periods are either seven clock periods long (for 16 or 20 character displays) or six clock periods long (for 18 character displays). For either case, character data is valid for the first five clock periods of the character period. Character 0 (left-most digit) starts upon the rising edge of the reset signal. The blank code is $A_1 = V_{SS}$ and A_0, B_3 - $B_0 = V_{DD1}$, with A_3 and A_2 providing reset and clock functions respectively. For the 18 character gas discharge display mode, the data outputs are blank for the 108th, 109th, and 110th clock periods.

Keyboard Modes

Scanned Sensor Mode

The sensor interface consists of two groups of eight lines, the scan strobe lines (S_0-S_7) and the return sense lines (R_0-R_7). Each scan strobe is used to enable eight return lines, giving 64 total sense strobes for each complete scan. When in the sensor mode, the two key rollover and debounce logic is inhibited. This allows multiple valid intersection connections to be inputted. The SHIFT and S/C (CONTROL) inputs are ignored in this mode.

Each sensor intersection will have a RAM location reserved. The designer should group the sensors in common groups of 4. This mode is intended to be used to scan a matrix of electronic intersections or mechanical contacts. Debouncing is to be performed under software control. The INT line will remain active (V_{DD1}) whenever a valid intersection has been detected. The scan strobe cycle is the same pattern of a logical 1 (V_{SS}) shifted in a field of zeros.

The sense return lines are read out by RD1/RD2 instructions as shown in Figure 2.

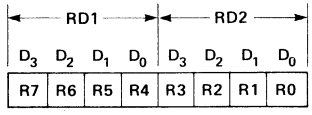


Figure 2. Sense Return.

If scanned sensor mode and individual, scanned display mode are used together, the Scan (S) lines should be electrically isolated by diodes (see Figure 4).

Scanned Keyboard Mode

a. Key Depression Detection

These conditions can occur during the keyboard interrogation by the PKD (see timing diagram below).

1. Simultaneous Key Depression

   Two or more keys depressed within one complete single depression scan (approximately 11ms) is defined as a simultaneous key depression. If this condition occurs, the PKD continues to scan the keyboard and waits until one key remains depressed. It then treats the remaining key as a single key depression, as described below.

2. Single Key Depression

   When any single key (non-simultaneous) is depressed, an internal counter is started. The key code is also stored internally in a PKD temporary register with a code given by the values of the Scan and Return Lines. The PKD will then make four more complete scans of all keys. If no other keys are depressed during the fourth complete scan and the original key detected is still depressed at the end of the fourth scan, the key code is defined as a single key depression. The key code is then entered into the FIFO along with the value of the SHIFT and Control (S/C) input signals. If eight characters are already in the FIFO, the character will not be entered and the overrun will be set. When a character is entered in the FIFO, the INT line is activated to a logical "1" (V_{DD1}). If on the fourth complete scan the original key depressed is no longer depressed, the key is ignored as if it had never been depressed. This delay of four scan times, or approximately 11ms, thus provides the debounce function for the keyboard.

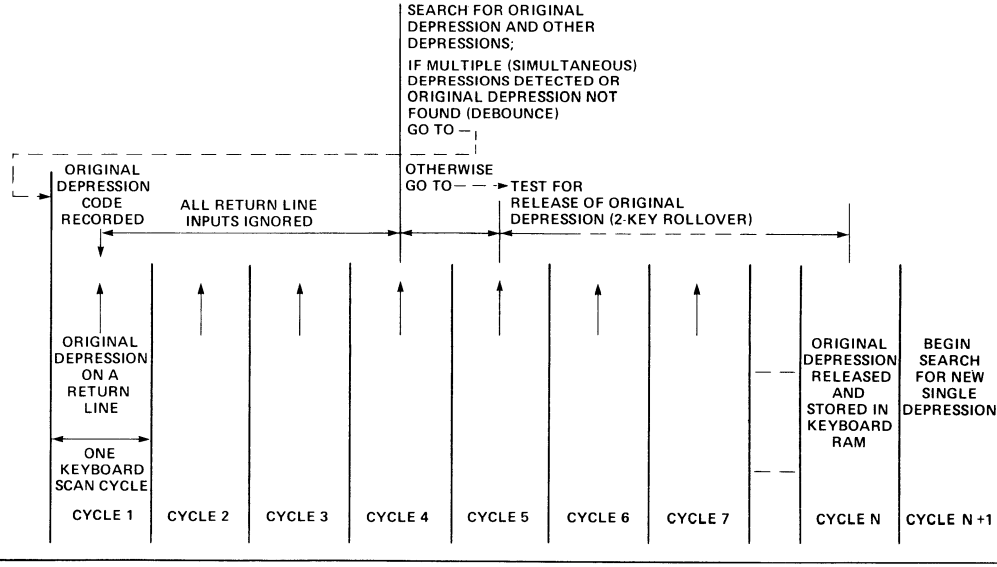


Figure 3. Keyboard Debounce and 2-Key Rollover Timing.

3. Two Key Rollover

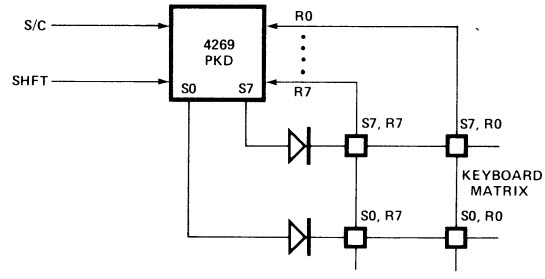
   The two key rollover operates as follows:

   If a second key is depressed after a first key has been accepted by the PKD as a single key depression but the first key has not been released, then the second key will be treated as a new original depression after the first key has been released.

   If a second key is depressed after a first key has been accepted by the PKD as a single key depression and the second key is released before the first key is released, the second key will be ignored.

b. Key Matrix Encoding

   The keyboard matrix hardware configuration and associated matrix encoding is shown in Figures 4, 5, and 6.



NOTE THAT ISOLATION DIODES MUST BE PLACED IN THE SCAN LINES AS SHOWN IF THE SCAN LINES ARE ALSO USED TO STROBE A DISPLAY. IF THE KEYBOARD USED HAS A DIODE AT EACH KEY, THEN THE SCAN LINE ISOLATION DIODES ARE NOT REQUIRED.

Figure 4. Hardware Configuration.

	R_0 000	R_1 001	R_2 010	R_3 011	R_4 100	R_5 101	R_6 110	R_7 111	SHIFT	S/C
S_0 000	0	1	2	3	4	5	6	7	X	X
S_1 001	8	9	10	11	12	13	14	15	X	X
S_2 010	16	17	18	19	20	21	22	23	X	X
S_3 011	24	25	26	27	28	29	30	31	X	X
S_4 100	32	33	34	35	36	37	38	39	X	X
S_5 101	40	41	42	43	44	45	46	47	X	X
S_6 110	48	49	50	51	52	53	54	55	X	X
S_7 111	56	57	58	59	60	61	62	63	X	X

Figure 5. Matrix Configuration.

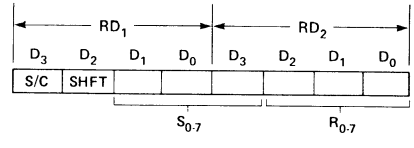


Figure 6. Key Encoding.

c. Expansion to 128 Key Scan

The basic mechanism of the PKD for scanning a 64 key matrix can be expanded to interface to a 128 key matrix. Note that the CONTROL (S/C) and SHIFT inputs cannot be used to directly encode 256 keys since the single key depression logic operates with the 6-bit matrix position code only. However, if full debounce and 2 key roll over control between two 64 key matrices is not necessary, then a configuration such as shown in Figure 7 may be used to add a seventh bit to the 6-bit matrix via the SHIFT or S/C input of the PKD. Alternately, two 4269 PKDs can be used for interfacing to the 128 keys.

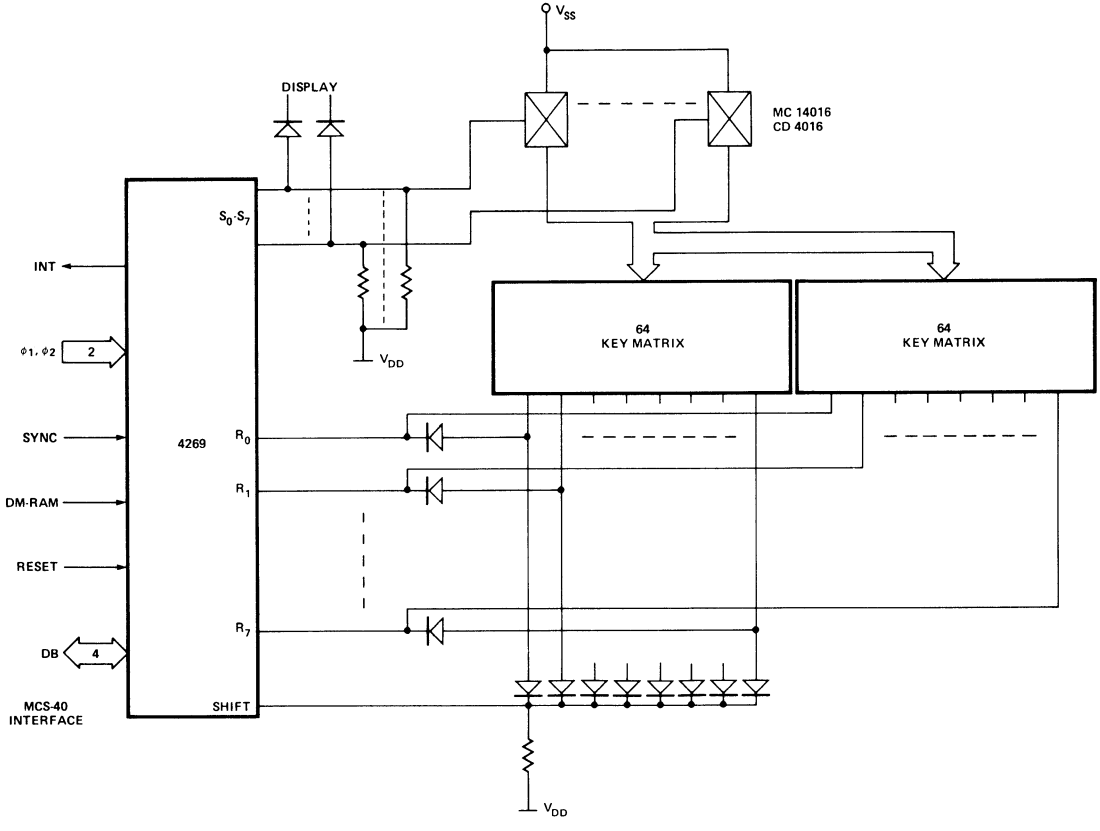


Figure 7. 128 Scanned Input Keys.

Encoded Keyboard Mode

Data Format

In the encoded keyboard mode, the eight return lines are directly loaded into the PKD's keyboard FIFO. For encoded keyboards using less than eight encoded bits, the remaining bits can be any desired signal, such as a multiplex signal between two keyboards or a special key flag.

HARDWARE DESCRIPTION

The following is a description of the major hardware elements of the 4269. Refer to the hardware block diagram shown in Figure 8.

MCS-40 Data Bus/Control Line Interface

The 4269 PKD resides on the MCS-40 data and timing bus. As such it derives its basic timing from the ϕ_1 and ϕ_2 clock signals. Synchronization and chip select information are provided by the SYNC and CM-RAM lines respectively. The Data Bus provides the 4269 with control commands and routes Keyboard/Display data between the 4269 and CPU Accumulator.

Display Registers

The 4269 is provided with RAM storage which is utilized to implement an automatically refreshed display. The display RAM (Display Registers A and B) can be configured in several different organizations under program control, including two 16 x 4 hexadecimal displays, one 32 x 4 hexadecimal display, a single 8 or 16 alphanumeric display, a single 16, 18, or 20 character gas discharge alphanumeric display, or a 128 matrix array of indicators. The display RAM output is available on A_0-A_3 for Display Register A outputs and B_0-B_3 lines for Display Register B outputs. The V_{DD1} line provides a separate negative supply reference for the A and B outputs (and INT).

S/R Counters and Debounce Logic

The S/R counters are two modulo 8 counters used to provide a unique 6-bit code for each of the 64 intersections provided by a matrix of eight Scan (S) Driver and eight Return (R) sense lines. The R counter is counted eight times for each S count. When keys, contacts, or controls are arranged in the matrix, each matrix intersection is examined for closure between the corresponding S and R line. If the 4269 is in the Scanned Keyboard Mode, an approximate 11 msec debounce time will be used to ascertain the validity of the connection. The valid 6-bit code, along with the SHIFT and S/C (control) line, is placed in the FIFO for retrieval by the CPU.

Scan Counter and Scan F/F

For each increment of the modulo 8 S counter, the Scan Counter is advanced. The register shifts a logical 1 (V_{SS}) in a field of logical zeros (open drain). The non-overlapping one is successively moved from S_0 through S_7 and around again. For each complete sequence of shifts, the scan flip-flop is toggled. This flip-flop's initial value, after RESET, is open drain.

Key Return Multiplexer

The return multiplexer selects one of the 8 return lines coming from the key array. The selection code is provided by the modulo 8 R counter. When in the Scanned Sensor Mode, all 8 R lines are entered for each scan line, and pass directly to the Sensor RAM (FIFO).

FIFO and Sensor RAM

This block is a dual function RAM of 64 bits. The RAM can serve as a keyboard character FIFO for eight 8-bit characters or as a sensor RAM to store the status of 64 intersections.

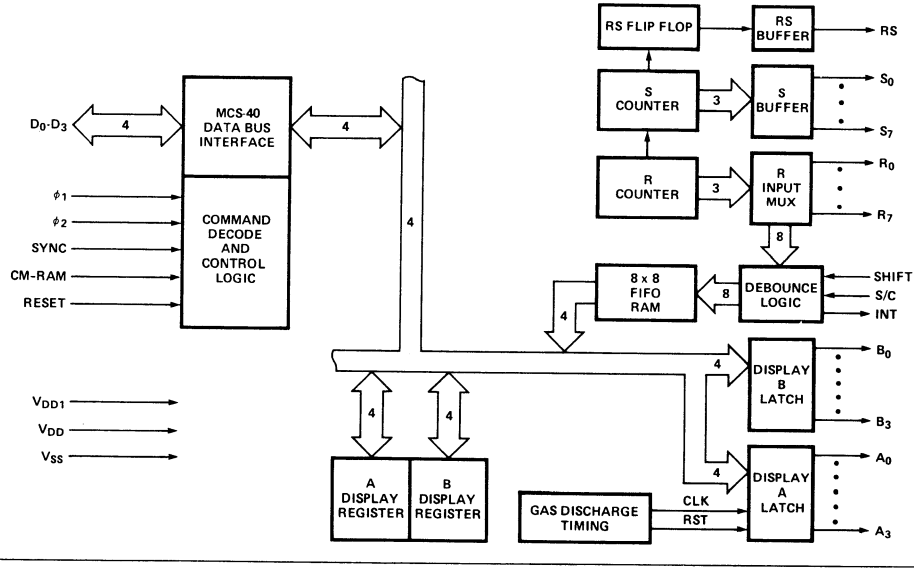


Figure 8. 4269 Hardware Block Diagram.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0° to 70°C; V_{SS} -V_{DD} = 15V ±5%; V_{DD1} = V_{SS} -5V; $t_{\phi PW}$= $t_{\phi D1}$ = 400nsec; $t_{\phi D2}$ = 150nsec; Logic "0" is defined as the more positive voltage (V_{IH},V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL},V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Supply Current		40	65	mA	T_A = 25°C
I_{DD1}	V_{DD1} Current			15	mA	T_A = 25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	µA	V_{IL} = V_{DD}
V_{IL}	Input Low Voltage (Except Clocks, Return Lines, Shift, S/C)			V_{SS}-5.5	V	
V_{IL}	Input Low Voltage (Return Lines, Shift, S/C)	V_{DD}		V_{SS}-4.2	V	
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS						
I_{LO}	Data Bus Output Leakage Current			10	µA	V_{OUT} = -12V
I_{OL}	Data Bus Sinking Current	8	15		mA	V_{OUT} = V_{SS}
I_{OLAB}	A_{0-3}/B_{0-3} Sinking Current	1.6			mA	V_{OUT} = V_{DD1} +.4V
I_{OHAB}	A_{0-3}/B_{0-3} Drive Current	50			µA	V_{OUT} = V_{SS} -2.6V
I_{OLI}	Interrupt Sinking Current	200			µA	V_{OUT} = V_{DD1} +.4V
I_{OHS}	S Lines Driving Current	3.2			mA	V_{OUT} = V_{SS} -1.0V
I_{OHRS}	RS Line Driving Current	2.5			mA	V_{OUT} = V_{SS} -2.6V
R_{OH}	Data Bus Output Resistance		150	250	Ω	V_{OUT} = V_{SS} -.5V

A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%.

Symbol	Parameter	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
t_{CY}	Clock Period	1.35		2	μsec	
$t_{\phi R}$	Clock Rise Time			50	nsec	
$t_{\phi F}$	Clock Fall Time			50	nsec	
$t_{\phi PW}$	Clock Width	380		480	nsec	
$t_{\phi D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	nsec	
$t_{\phi D2}$	Clock Delay ϕ_2 to ϕ_1	150			nsec	
t_W	Data-In, CM, SYNC Write Time	350	100		nsec	
t_H[1,2]	Data-In, CM, SYNC Hold Time	40	20		nsec	
t_{OS}[3]	Set Time (Reference)	0			nsec	C_L = 500 pF
t_{ACC}	Data Bus Access Time			930	nsec	C_L = 500 pF
t_{OH}	Data Bus Hold Time	50			nsec	C_L = 20 pF
t_{RTSK}	Return Line Pull-Down Time		5	16	μs	C = 120pF; Scanned Keyboard Mode
t_{RTSN}	Return Line Pull-Down Time		30	200	μs	C = 120 pF; Sensor Mode

CAPACITANCE

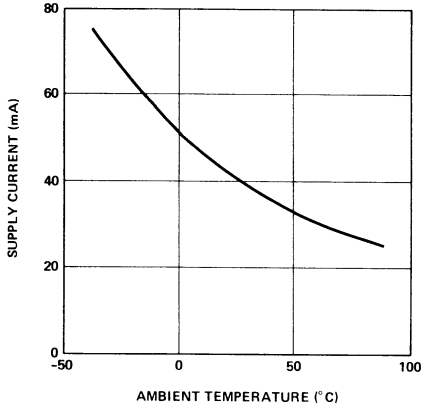
Symbol	Parameter	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
C_ϕ	Clock Capacitance		8	25	pF	V_{IN} = V_{SS}
C_{DB}	Data Bus Capacitance		14	25	pF	V_{IN} = V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN} = V_{SS}
C_{OUT}	Output Capacitance			15	pF	V_{IN} = V_{SS}

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.

2. All MCS-40 components which may transmit instruction on data to a 4004 or 4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

3. t_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} in the same output access time referred to the leading edge of the next ϕ_2 clock pulse.

TYPICAL I_{DD} SUPPLY CURRENT VS. TEMPERATURE



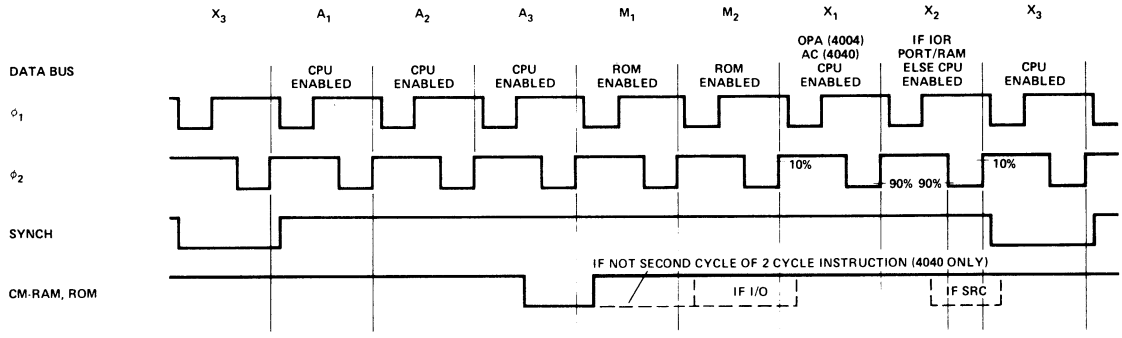


Figure 9. Timing Diagram.

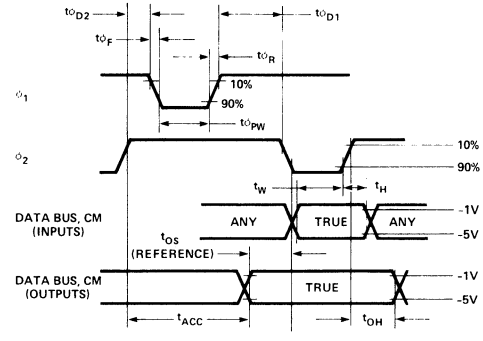


Figure 10. Timing Detail.

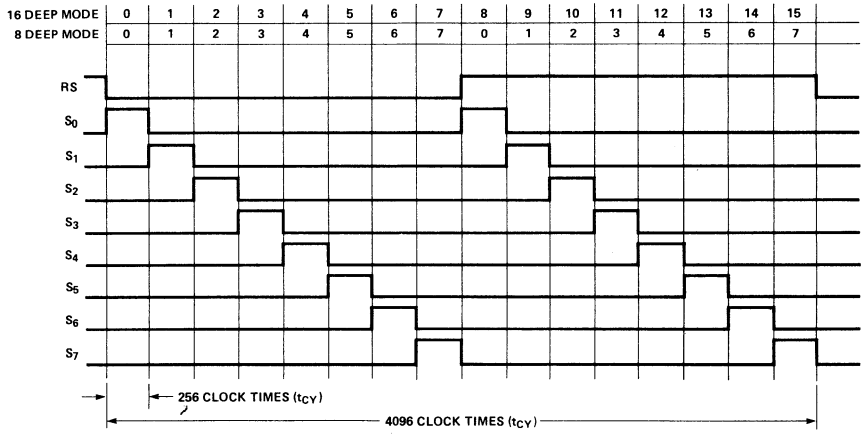


Figure 11. Individually Scanned Display Mode Timing After Execution of 0 or 16 WRM Instruction (or 8 WRMs for 8 Nibbles Deep Mode).

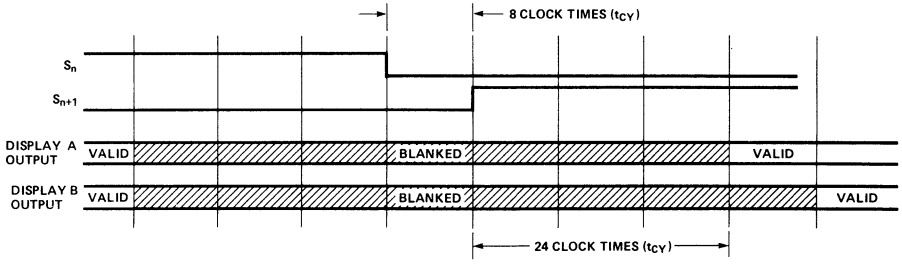


Figure 12. Individually Scanned Display Mode.

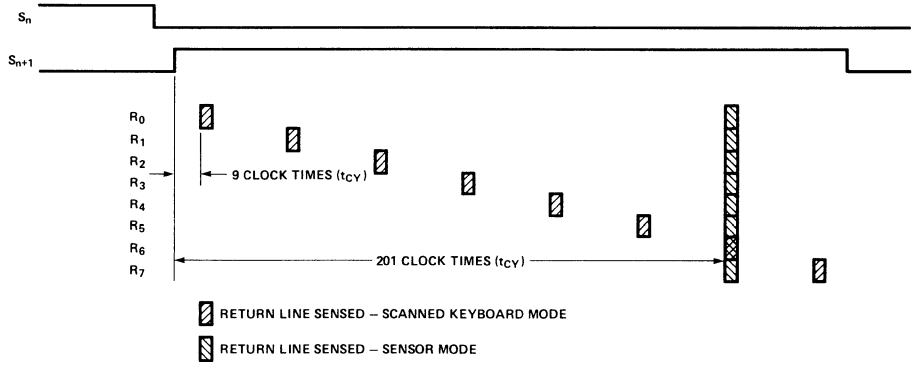


Figure 13. Return Line Timing for Scanned Keyboard and Sensor Mode.

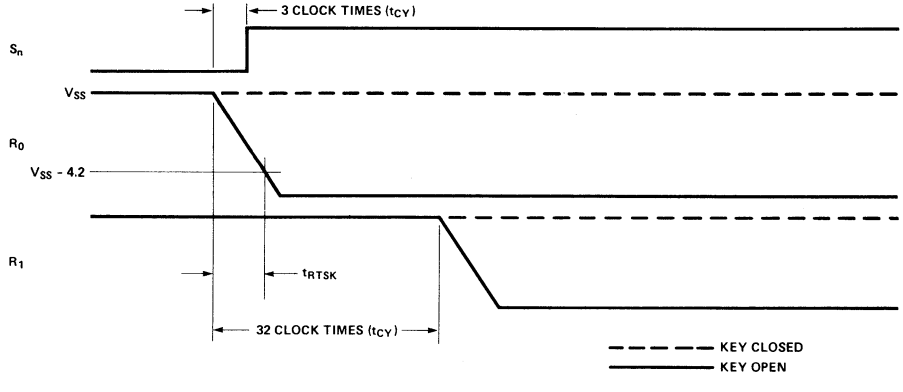


Figure 14. Detailed Timing – Scanned Keyboard Mode.

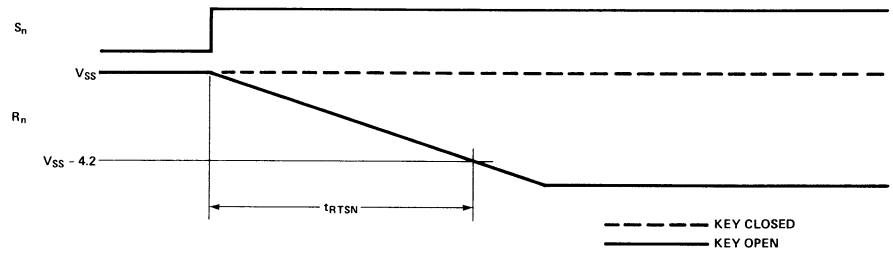


Figure 15. Detailed Timing – Sensor Mode.

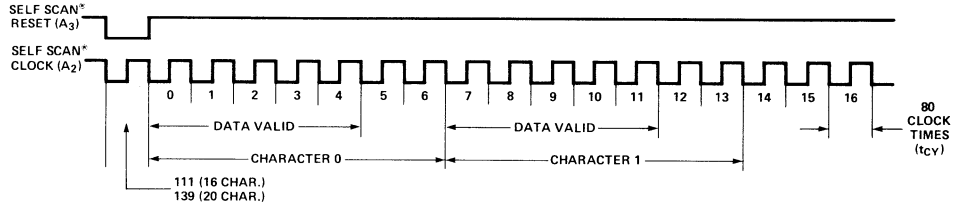


Figure 16. Gas Discharge (Self-Scan®) Mode Timing – 16 or 20 Character Mode.

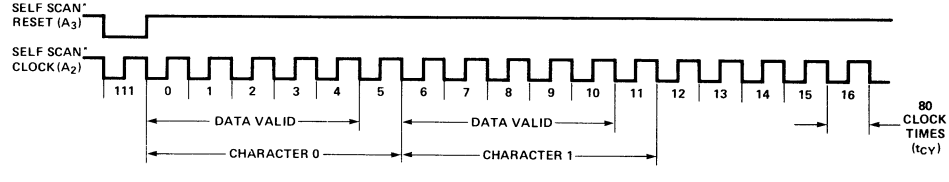


Figure 17. Gas Discharge (Self-Scan®) Mode Timing – 18 Character Mode.

4201A

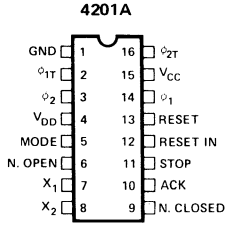
CLOCK GENERATOR

- **Complete Clock Requirements for MCS-40™ Systems**
- **Crystal Controlled Oscillator (XTAL External)**
- **MOS and TTL Level Clock Outputs**
- **Provides MCS-40 Reset Function Signal**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available with -40° to +85°C Operating Range**

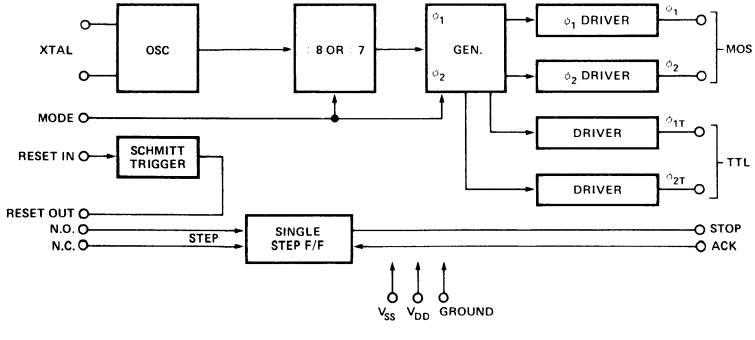
The 4201A is a CMOS integrated circuit designed to fill the clock requirements of the MCS-40 microcomputer family. The 4201A contains a crystal controlled oscillator (XTAL external), clock generation circuitry, and both MOS and TTL level clock driver circuits.

The 4201A also performs the power on reset function required by MCS-40 components and provides the logic necessary to implement the single-step function of the 4040 central processor unit.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Designation	Description of Function
1	GND	Circuit ground potential. This pin can be left floating for low power application. MOS clock output will be operative, TTL clock outputs will not.
2	ϕ_{1T}	Phase 1 TTL level clock output. Positive true.
3	ϕ_2	Phase 2 MOS level clock output. Directly drives all MCS-40 components.
4	V_{DD}	Main Power Supply Pin. $V_{DD} = V_{CC} - 15V \pm 5\%$.
5	MODE	Counter mode control pin. Determines whether counter divides basic frequency by 8 or 7. Mode 1 = $V_{CC} \rightarrow \div 7$ Mode 2 = $V_{DD} \rightarrow \div 8$
6	N. OPEN	Input of single step circuitry to which normally open contact of SPDT switch is connected.
7	X1	External Crystal Connection. This pin may be driven by an external frequency source. X2 should be left unconnected.
8	X2	External Crystal Connection.
9	N. CLOSED	Input of single step circuitry to which normally closed contact of SPDT switch is connected.
10	ACK	Acknowledge input to single step circuitry normally connected to stop acknowledge output of 4040. The ACK input circuitry, contains an internal pull-down resistor, eliminating the need for any external pull-down.
11	STOP	Stop output of single step circuitry normally connected to stop input of 4040. A SPDT toggle switch may be inserted in this line for RUN/HALT control.
12	RESET IN	Input to which RC network is connected to provide power-on reset timing.
13	RESET	Reset signal output which directly connects to all MCS-40 reset inputs. This signal is active low.
14	ϕ_1	Phase 1 MOS level clock output. Directly drives all MCS-40 clock inputs.
15	V_{CC}	Circuit reference potential — most positive supply voltage.
16	ϕ_{2T}	Phase 2 TTL level clock output. Positive true.

FUNCTIONAL DESCRIPTION

The 4201A consists of the following functional blocks:

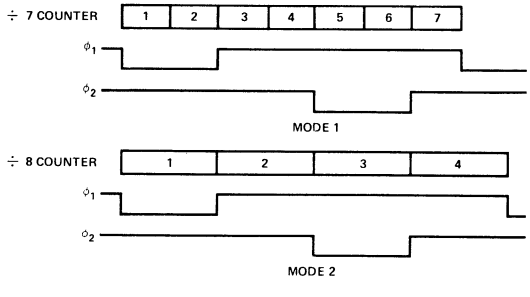
CRYSTAL OSCILLATOR

The oscillator circuit consists of a simple inverter biased in the active region and a crystal phase shift network to provide positive feedback.

PROGRAMMABLE SHIFT REGISTER

The shift register in the 4201A divides the master clock and generates the proper states for generating the desired two-phase clock. The circuit is a seven bit dynamic device which circulates a logical "1" through a field of zeroes. The output of the various states are then combined to provide the proper clock waveforms. This provides a divide by 7 function.

In order to maintain the proper clock timing over the full operating frequency range of the MCS-40™ system, the shift register is programmable (using mode pin) as either a 7 bit or 8-bit device. In the 8-bit mode, the relationship between the phases is equal; that is, ϕ_1 pulse width, ϕ_2 pulse width, ϕ_1 to ϕ_2 and ϕ_2 to ϕ_1 times are all equal.



4201A Shift Register Modes.

PHASE DECODER

A simple gate complex is used to decode the shift register outputs to provide phase 1 and phase 2 clock waveforms. This circuitry is controlled by the mode input to achieve the two sets of timing discussed in the previous section.

OUTPUT BUFFERS

There are two sets of output buffers for the 2 phase clock. One set is the MOS level drivers designed to directly drive a full complement of MSC-40 components. The second set provides TTL compatible outputs which can drive one standard TTL load.

RESET CIRCUIT

The reset circuit is simply a level detector and driver stage. An external RC network connected to the reset input pin of the 4201A as described in the Design Considerations section provides power-on delay. The user's system will determine the required delay.

SINGLE STEP CONTROL

The 4201A contains the necessary circuitry for allowing the 4040 CPU to execute instructions one at a time. Using the stop input and stop acknowledge output of the 4040, the 4201A generates a pulse that allows the 4040 to perform only one instruction. The stop command can be provided by a SPDT pushbutton (break-before-make) directly since debouncing is provided by the 4201A. A SPST toggle switch, in series with the $\overline{\text{STOP}}$ line, provides the Run/Halt feature.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -55°C to 150°C Ambient
Operating Temperature ..... 0°C to 70°C Ambient
Maximum Positive Voltage ..... V_{CC} +.5V
Maximum Negative Voltage ..... V_{DD} -.3V
Maximum Power Dissipation 1.0W
Maximum Supply Voltage V_{CC} -V_{DD} ..... 17V[1]
Maximum Supply Voltage V_{CC} -V_{DD} ..... 17V[2]

Notes: 1. C_{LOAD}, ϕ_1 and $\phi_2 \geq 100pF$.
2. C_{LOAD}, ϕ_1 and ϕ_2 = 0; R_{DD} = 68Ω; Bypass Capacitor at V_{DD} Pin to GND.

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC}-V_{DD} = 15V ±5%; GND = V_{CC} -5V ±5%.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Limit Max.	Units	Conditions
I_{DD}	Supply Current		20	mA	5.185MHz Crystal, C_{LOAD} ϕ_1 and ϕ_2=200pF

INPUT/OUTPUT CHARACTERISTICS

I_{LI}	Input Leakage Current		10	μA	V_{IL} = V_{DD} All inputs except X_1, X_2, N. Open, N. Closed
V_{IH}	Input High Voltage	V_{CC}-1.5	V_{CC}+.5	V	All inputs except X_1, X_2, Reset
V_{IL}	Input Low Voltage	V_{DD}	V_{CC}-13	V	All inputs except X_1, X_2, Reset
V_{OL}	Output Low Voltage	V_{DD}	V_{CC}-13.4	V	Capacitance load only
V_{OH}	Output High Voltage	V_{CC}-1.5	V_{CC}	V	Capacitance load only
V_{OL}	ϕ_{1T}, ϕ_{2T}		GND+.5	V	I_{OL} = 1.6mA
V_{OH}	ϕ_{1T}, ϕ_{2T}	V_{CC}-.75		V	I_{OH} = -400μA
I_{OL}	ϕ_1, ϕ_2 Sink Current	400		mA	V_{OUT} = V_{CC}; Pulse Width ≤1μsec
I_{OL}	ϕ_{1T}, ϕ_{2T} Sink Current	15		mA	V_{OUT} = V_{CC}
I_{OL}	Reset Sink Current	6		mA	V_{OUT} = V_{CC}
I_{OL}	Stop Sink Current	1		mA	V_{OUT} = V_{CC}
I_{OH}	ϕ_1, ϕ_2 Source Current	180		mA	V_{OUT} = V_{DD}
I_{OH}	ϕ_{1T}, ϕ_{2T} Source Current	8		mA	V_{OUT} = V_{DD}
I_{OH}	Reset Source Current	6		mA	V_{OUT} = V_{DD}
I_{OH}	Stop Source Current	1		mA	V_{OUT} = V_{DD}
V_{IL}	Reset Input Low Voltage	V_{DD}	V_{CC}-11	V	
V_{IH}	Reset Input High Voltage	V_{CC}-6.5	V_{CC}+.5	V	
R_1	Pull Up Resistance on N. Open, N. Closed	20	120	KΩ	V_{IN} = V_{DD}

CAPACITANCE

f = 1MHz; T_A = 25°C

Symbol	Parameter	Limit Min.	Limit Max.	Units	Conditions
C_{IN}	Input Capacitance		5	pF	All Inputs except X_1, X_2
C_{OUT}	ϕ_1, ϕ_2 Output Capacitance		40	pF	
C_{OUT}	ϕ_{1T}, ϕ_{2T} Output Capacitance		10	pF	
C_{OUT}	Stop Reset Output Capacitance		5	pF	

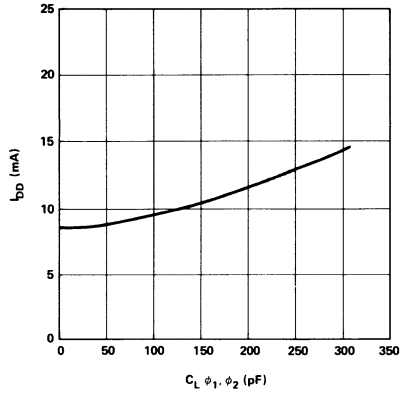
A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} - V_{DD} = 15V \pm 5\%$; $G = V_{CC} - 5V \pm 5\%$

Symbol	Parameter	Limit			Units	Conditions
		Min.	Typ.	Max.		
t_{CY}	Clock Period		t_{XTAL} *7		ns	Mode = V_{CC}
$t_{\phi PW}$	Clock Pulse Width	$(2/7)t_{CY}-10$	$(2/7)t_{CY}$	$(2/7)t_{CY}+10$	ns	
$t_{\phi D1}$	Clock Delay from ϕ_1 to ϕ_2	$(2/7)t_{CY}-10$	$(2/7)t_{CY}$	$(2/7)t_{CY}+10$	ns	
$t_{\phi D2}$	Clock Delay from ϕ_2 to ϕ_1	$(1/7)t_{CY}-10$	$(1/7)t_{CY}$	$(1/7)t_{CY}+10$	ns	
t_{CY}	Clock Period		t_{XTAL} *8		ns	Mode = V_{DD}
$t_{\phi PW}$	Clock Pulse Width	$(1/4)t_{CY}-10$	$(1/4)t_{CY}$	$(1/4)t_{CY}+10$	ns	
$t_{\phi D1}$	Clock Delay from ϕ_1 to ϕ_2	$(1/4)t_{CY}-10$	$(1/4)t_{CY}$	$(1/4)t_{CY}+10$	ns	
$t_{\phi D2}$	Clock Delay from ϕ_2 to ϕ_1	$(1/4)t_{CY}-10$	$(1/4)t_{CY}$	$(1/4)t_{CY}+10$	ns	
$t_{\phi D3}$	TTL Clk to MOS Clk Skew[1]	0		40	ns	
$t_{\phi r}, t_{\phi f}$	Clock Rise and Fall Time			50	ns	C_L=300pF=ϕ_1,ϕ_2; C_L=50pF on ϕ_{1T},ϕ_{2T}
t_D	Delay from Acknowledge to Stop			1	μs	C_L=20pF

Note: 1. See waveforms section for phase relationships between ϕ_1, ϕ_1T, ϕ_2, and ϕ_2T.
2. Proper system operation of all members of the MCS-40™ component family is guaranteed with the 4201 Clock Generator at 1.35 μsec ≤ t_{CY} ≤ 2 μsec.

TYPICAL CHARACTERISTICS

I_{DD} CURRENT VS. LOAD CAPACITANCE



XTAL SPECIFICATIONS

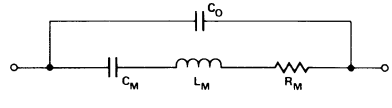
Range: 3.5 - 5.185 MHz

Mode: Series or Parallel Resonant

Recommended: 1. Intel I4801
2. Crystek 5.185 MHz, Spec. No. CY8A
3. CTS Knights MP051

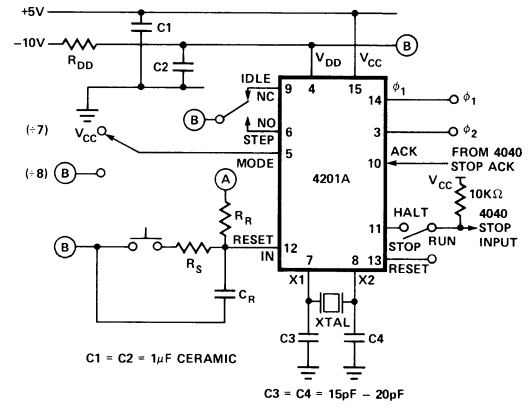
XTAL Capacitance Requirements: 15-20 pF

CTS Knights
XTAL Equivalent Circuit



$C_O \approx$ 3-5pF
$C_M \approx$ 10fF
$R_M \leq 50\Omega$
$L_M \approx \frac{1}{(2\pi f)^2 C_M}$

CLOCK GENERATOR IMPLEMENTATION



DESIGN CONSIDERATIONS

CRYSTALS

Either ÷7 or ÷8 Modes may be used. Mode equals V_{CC} for ÷7, Mode equals V_{DD} for ÷8. The clock frequency range should be between 500 kHz (4 MHz XTAL, ÷8 MODE) and 740 kHz (5.185 MHz XTAL, ÷7 MODE). The crystal may be found as a standard product from Intel distributors, CTS Knights or Crystek.

X1 AND X2 INPUT CAPACITANCE

The XTAL terminals, X1 and X2, should be tied to 15 pF - 20 pF capacitors C3 and C4 to AC system GND.

POWER SUPPLY VOLTAGE CONSIDERATIONS

1. Operation is guaranteed with V_{CC}-V_{DD} = 15V ± 5%. During system power-up or during power supply glitching, the maximum magnitude of (V_{CC}-V_{DD}) must be limited to 17 volts.

   During the power supply rise time (that is, when $|V_{CC}-V_{DD}| < 14.25$ volts), improper ϕ_1, and ϕ_2 output may occur until $|V_{CC}-V_{DD}|$ reaches the 14.25 minimum voltage.

2. With V_{CC} = +5V, V_{DD} = -10V, bypass capacitor C1 of 1 μF and C2 of 1 μF from V_{CC} to GND and V_{DD} to GND, respectively, should provide excellent bypassing. Bypass capacitors should be ceramic or equivalent quality to insure low inductance and low series resistance.

3. The purpose of the current limiting register R_{DD} is both to limit ϕ_1 and ϕ_2 rise times and to drop V_{DD} at the 4201A V_{DD} pin. Values for R_{DD} as a function of ϕ_1, ϕ_2 load capacitance are:
   For C_{LOAD} <50 pF; use R_{DD} = 100Ω.
   For 50 pF <C_{LOAD} <100 pF; use R_{DD} = 68Ω.
   For 100 pF <C_{LOAD} <300 pF; use R_{DD} = 27Ω.
   For C_{LOAD} >300 pF; use R_{DD} = 10Ω.

   All 4201A functions requiring the V_{DD} voltage should use the pin V_{DD} or node (B) on the 4201A side of resistor R_{DD}. Operation with the voltage drop across R_{DD} is guaranteed by Intel testing.

4. Single-Supply System (+15 V or -15)

   Recommended 4201A circuit modifications for single supply systems are:

   1. The 1 μF ceramic capacitor C1 should be between 4201A V_{DD} and V_{CC} pins.
   2. Other capacitors shown as being grounded should be connected to V_{CC}.
   3. Reset R_R is connected to V_{CC}. Reset C_R is connected to V_{DD} pin.
   4. The current limiting resistor R_{DD} is still needed in the V_{DD} line.

5. Power Supply Rise Times

   Intel testing is for power supply rise times between 5 ms and 300 ms. For power supply rise times less than 5 ms, a 200KΩ resistor from X1 to GND and C3 = C4 = 5 pF is recommended.

RESET NETWORK

The Reset input has V_{IL} = V_{CC}-11 volts and V_{IH} = V_{CC} -6.5 volts, with about 1 volt of hysteresis (Schmitt circuit).

Node (A) must be tied to GND or V_{CC} = +5 V; and R_R and C_R selected, such that the negative V_{DD} transition moves the Reset input below V_{IL}.

Tying node (A) to GND and making C_R very large, i.e. >1μF, will allow the greatest freedom in V_{CC} and V_{DD} rise times during turn-on. Tying node (A) to GND will also cause Reset after a V_{DD} glitch to GND.

The purpose of R_S at 510Ω or 1KΩ is to limit Reset input fall time on manual Reset, so that the Reset input does not fall below V_{DD}.

TTL CLOCK OUTPUTS

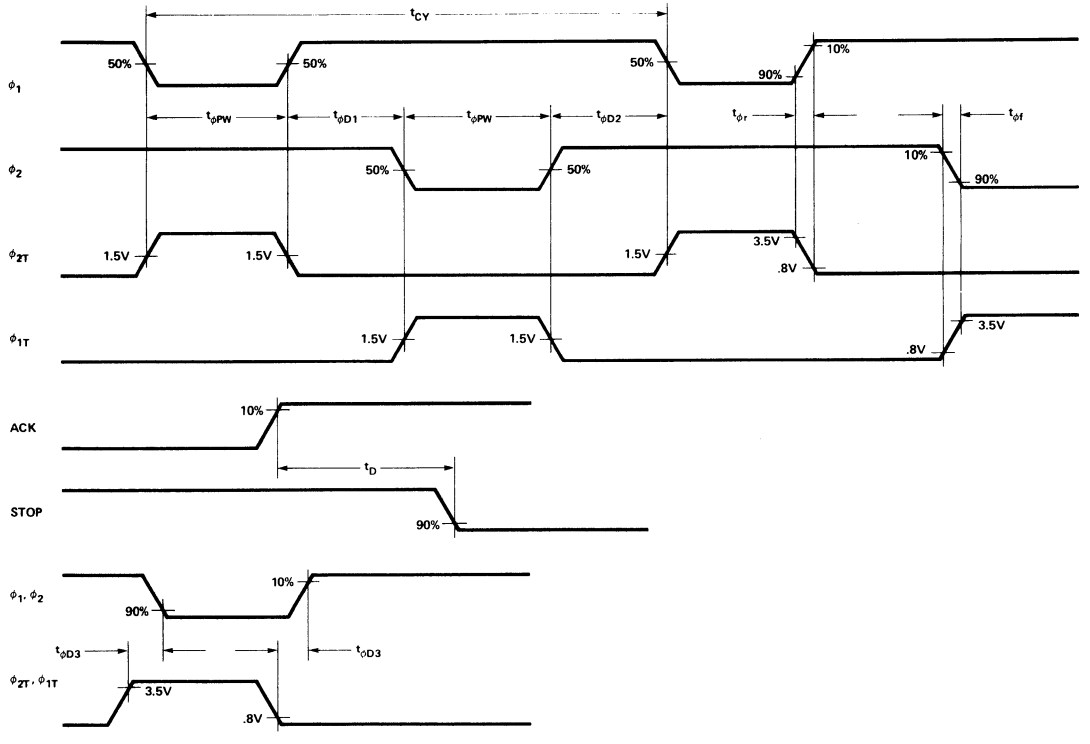
If ϕ_{1T} and ϕ_{2T} are used, GND pin should be tied to logic ground. ϕ_{2T} levels will swing between V_{CC} and GND.

UNUSED FUNCTIONS

If any of the 4201A functions listed below are not used, for power conservation it is recommended that the pins be connected as described below:

1. ϕ_{1T},ϕ_{2T}
   Tie GND pin, ϕ_{1T}, ϕ_{2T} to V_{CC}.
2. Single step
   Tie NO to V_{CC}.
   Tie NC to Node (B) (V_{DD} pin).
   Tie STOP ACK to V_{CC}.
   STOP left open.
3. Reset
   Tie RESET IN, RESET OUT to V_{CC}.

WAVEFORMS

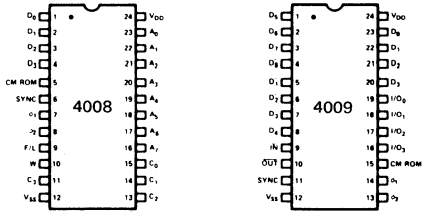

t_{CY}
ϕ_1
50%
$t_{\phi PW}$
$t_{\phi D1}$
$t_{\phi PW}$
$t_{\phi D2}$
$t_{\phi r}$
$t_{\phi f}$
10%
90%
ϕ_2
ϕ_{2T}
1.5V
3.5V
.8V
ϕ_{1T}
ACK
t_D
STOP
ϕ_1, ϕ_2
$t_{\phi D3}$
ϕ_{2T}, ϕ_{1T}

4008/4009
STANDARD MEMORY AND I/O INTERFACE SET

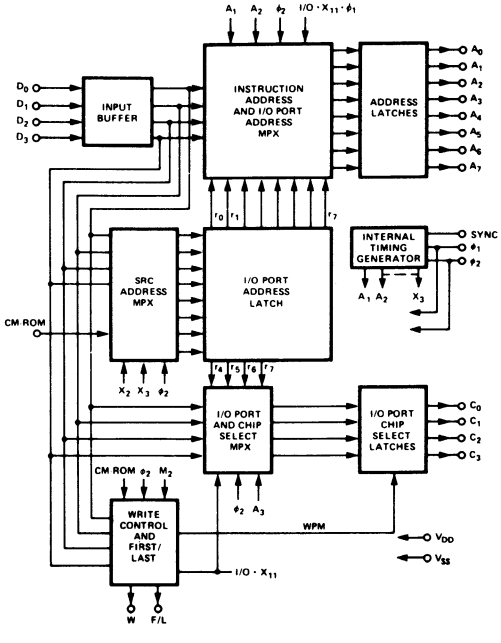
- **Direct Interface to Standard Memories**
- **Allows Write Program Memory**
- **24 Pin Dual In-Line Packages**
- **Standard Operating Temperature Range of 0° to 70 °C**

The standard memory and I/O interface set (4008/4009) provides the complete control functions performed by the 4001 or 4308 in MCS-40™ systems. The 4008/4009 are completely compatible with other members of the MCS-40 family. All activity is still under control of the CPU. One set of 4008/4009 and several TTL decoders is sufficient to interface to 4K words of program memory, sixteen four-bit input ports and sixteen four-bit output ports.

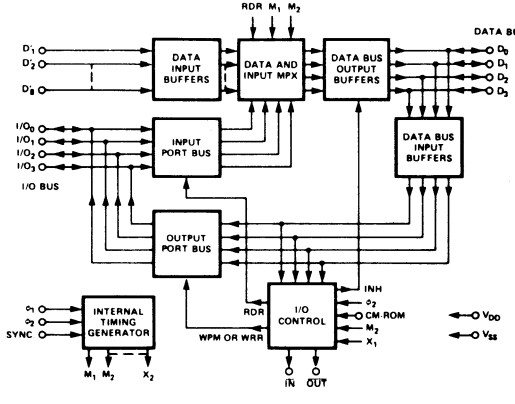
PIN CONFIGURATIONS



4008 BLOCK DIAGRAM



4009 BLOCK DIAGRAM



Pin Description

4008

Pin No.	Designation/ Type of Logic	Description of Function
1-4	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
7-8	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
6	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
5	CM-ROM/Neg.	Command input driven by CM-ROM output of processor. Used for decoding SRC and I/O instructions.
23-16	A_0-A_7/Pos.	Address output buffers. The demultiplexed address values generated by the 4289 from the address data supplied by the processor at A_1 and A_2.
15-13, 11	C_0-C_3/Pos.	Chip select output buffers. The address data generated by the processor at A_3, or during an SRC are transferred here.
9	F/L/Neg.	Output signal generated by the 4008 to indicate which half-byte of PROGRAM MEMORY is to be operated on.
10	W/Pos.	Output signal, active low, generated by the 4008 when the processor executes a WPM instruction.
12	V_{SS}	Most positive supply voltage.
24	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.

4009

Pin No.	Designation/ Type of Logic	Description of Function
23-20	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
5-8, 1-4	D'_1-D'_8/Pos.	The eight bits of instruction from the program memory are transferred on these 4009 pins (most significant bit is D_8).
14-13	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
11	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
15	CM-ROM/Neg.	Command input driven by CM-ROM output of Processor.
9	IN/Neg.	Output signal, active low, generated by the 4289 when the processor executes an RDR instruction.
10	OUT/Neg.	Output signal, active low (V_{DD}), generated by the 4009 when the processor executes a WRR instruction.
19-16	I/O_0-I/O_3/Pos.	Bidirectional I/O data bus. Data to and from I/O ports or data to write PROGRAM MEMORY are transferred via these pins.
23	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.
12	V_{SS}	Most positive supply voltage.

Functional Description

The 4008 is the address latch chip which interfaces the 4004 or 4040 to standard PROMs, ROMs and RAMs used for program memory. The 4008 latches the low order eight bits of the program address sent out by the CPU during A1 and A2 time. During A3 time it latches the high order four bits of the program address from the CPU. The low-order eight bits of the program address are then presented at pins A0 through A7 and the high-order four bit (also referred to as page number) are presented at pins C0 through C3. These four bits must be decoded externally and one page of program memory is selected.

The 4009 then transfers the eight bit instruction from program memory to the CPU four bits at a time at M1 and M2. The command signal sent by the CPU activates the 4009 and initiates this transfer.

When the CPU executes an SRC (Send Register Control) instruction, the 4008 responds by storing the I/O address in its eight bit SRC register. The content of this SRC register is always transferred to the address lines (A0 through A7) and the chip select lines (C0 through C3) at X1 time. The appropriate I/O port is then selected by decoding the chip select lines. The IN and OUT lines of the 4009 indicate whether an input or output operation will occur.

The 4009 is primarily an instruction and I/O transfer device. When the CPU executes an RDR (Read ROM Port) instruction, the 4009 will send an input strobe (pin 9) to enable the selected input port. It also enables I/O input buffers to transfer the input data from the I/O bus to the data bus. When the 4009 interprets a WRR (Write ROM Port) instruction, it transfers output data from the CPU to the I/O bus and sends an output strobe (pin 10) to enable the selected output port.

The WPM (Write Program Memory) instruction is used in conjunction with the 4008/4009 to write data into the RAM program memory. When an instruction is to be stored in RAM program memory, it is written in two four-bit segments. The F/L signal from the 4008 keeps track of which half is being written. When the CPU executes a WPM instruction, the chip select lines of the 4008 are jammed with "1111". In the system design this should be designated as the RAM channel. The W line on the 4008 is also activated by the WPM instruction. The previously selected SRC address on line A0 through A7 of the 4008 becomes the address of the RAM word being written. By appropriately decoding the chip select lines, the W line, and F/L, the write strobes can be generated for the memory.

The F/L line is initially high (V_{SS}) when power comes on. It then pulses low (V_{DD}) when every second WPM is executed. A high (V_{SS}) on the F/L lines means that the first four bits (OPR) are being written, and a low means that the last four bits (OPA) are being written. The 4009 transfers the segment of the instruction to the I/O bus at X2 of the WPM instruction. The SRC address sent to RAM is only 8 bits. When more than one page of RAM (256 bytes) is being written, an output port must be used to supply additional address lines for higher order addresses.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to V_{SS}	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW} = t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
SUPPLY CURRENT						
I_{DD}	Average Supply Current (4008 only)		10	20	mA	T_A = 25°C
I_{DD}	Average Supply Current (4009 only)		13	30	mA	T_A = 25°C
INPUT CHARACTERISTICS–ALL INPUTS EXCEPT I/O PINS						
I_{LI}	Input Leakage Current			10	μA	$V_{IL} = V_{DD}$
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS–ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitance Load
I_{OL}	Data Lines Sinking Current	8	15		mA	$V_{OUT} = V_{SS}$
I_{OL}[1]	Address Line Sinking Current (4008 only)	7	13		mA	$V_{OUT} = V_{SS}$
I_{OL}	In, Out, F/L, Chip Select	1.6	4		mA	$V_{OUT} = V_{SS}$ -4.85
I_{OL}[2]	W Output, Sinking Current (4008 only)	2.5	5		mA	$V_{OUT} = V_{SS}$
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level (4008 only)		150	250	Ω	$V_{OUT} = V_{SS}$ -.5V
R_{OH}	Address, Chip Select Output Resistance, "0" Level (4008 only)		.6	1.2	kΩ	$V_{OUT} = V_{SS}$ -.5V
R_{OH}	Output Resistance, Data Line "0" Level (4009 only)		130	250	Ω	$V_{OUT} = V_{SS}$ -2V
I_{CF}[3]	Address, C/S Output "1" Clamp Current (4008 only)			16	mA	$V_{OUT} = V_{SS}$ -6V
I_{CF}[3]	In, Out "1" Clamp Current (4009 only)			16	mA	$V_{OUT} = V_{SS}$ -6V
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IH}[4]	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (4009 only)	V_{DD}		V_{SS}-4.2	V	
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance (4009 only)		.25	1.0	kΩ	$V_{OUT} = V_{SS}$ -.5
I_{OL}	I/O Output "1" Sink Current (4009 only)	5	12		mA	$V_{OUT} = V_{SS}$ -.5V
I_{OL}	I/O Output "1" Sink Current (4009 only)	1.6	4		mA	$V_{OUT} = V_{SS}$ -4.85V
I_{CF}	I/O Output "1" Clamp Current (4009 only)			16	mA	$V_{OUT} = V_{SS}$ -6V
CAPACITANCE						
C_{ϕ}	Clock Capacitance		8	15	pF	$V_{IN} = V_{SS}$
C_{DB}	Data Bus Capacitance		7	10	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance (4008 only)			10	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance (4009 only)			15	pF	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance			10	pF	$V_{IN} = V_{SS}$

Notes: 1. The address lines will drive a TTL load if a 470Ω resistor is connected in series between the address output and the TTL input.
2. A 6.8kΩ resistor must be connected between Pin W and V_{DD} for TTL capability.
3. Resistors in series with TTL inputs may be required to limit current into V_{DD} or V_{SS} from TTL input clamp diodes.
4. TTL V_{OH} = 2.4V will ensure 4009 $V_{IH} = V_{SS}$ -1.5 via the 4009 latch. Refer to Figure 3.

A.C. Characteristics

T_A = 0°C to 70°C, V_{SS} -V_{DD} = 15V ±5%

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Times			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay $\phi1$ to ϕ_2	400		500	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500 pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{A1}	Address to Output Delay at A_1, X_1 (4008)			580	ns	C_L = 250pF
t_{A2}	Address to Output Delay A_2 (4008)			580	ns	C_L = 250pF
t_{CS}	Chip Select Output Delay at A_3 (4008)			300	ns	C_L = 50pF
t_{WD}	W Output Delay (4008)			600	ns	C_L = 100pF
t_{FD}	F/L Output Delay (4008)	0.1		1	μs	C_L = 100pF
t_{WI}	Data In Write Time (4009)	470			ns	C_L = 200pF on data bus
t_D	I/O Output Delay (4009)			1.0	μs	C_L = 300pF
t_{S1}	IN Strobe Delay (4009)			450	ns	C_L = 50pF
t_{S2}	OUT Strobe Delay (4009)			1.0	μs	C_L = 50pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.

2. t_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.

3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

Timing Diagram

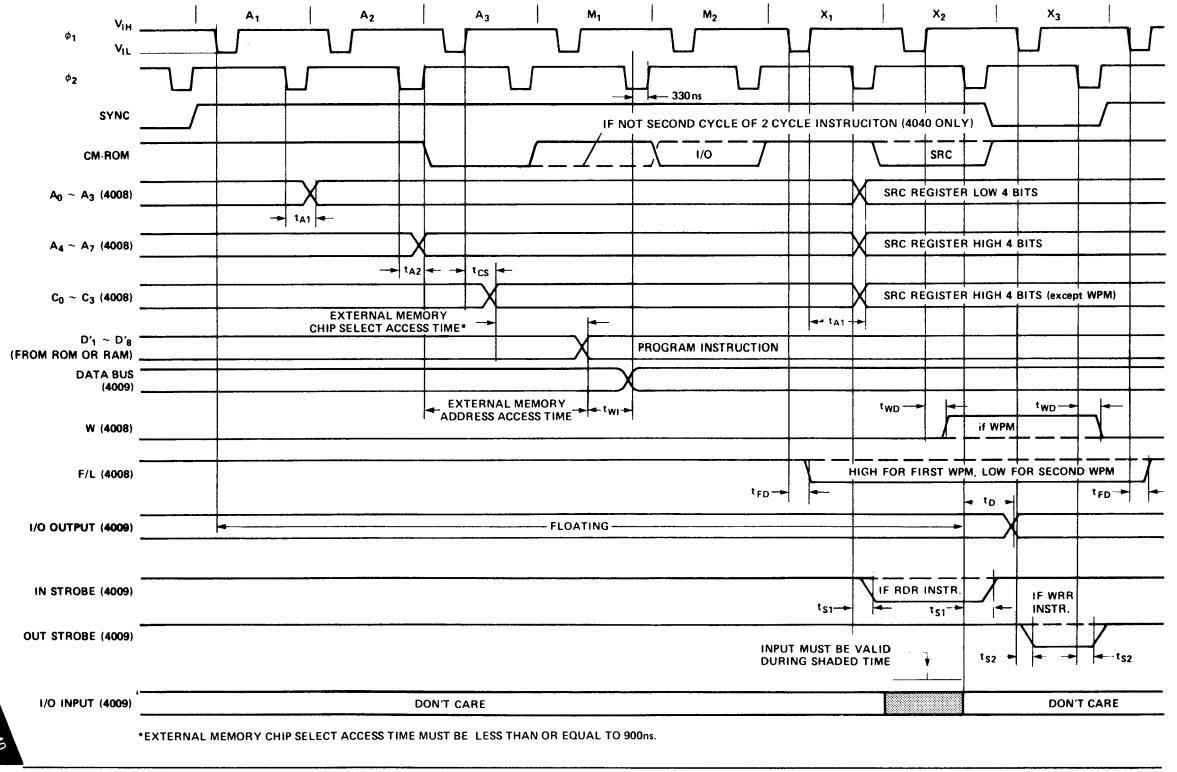


Figure 1. 4008 and 4009 Timing Diagram.

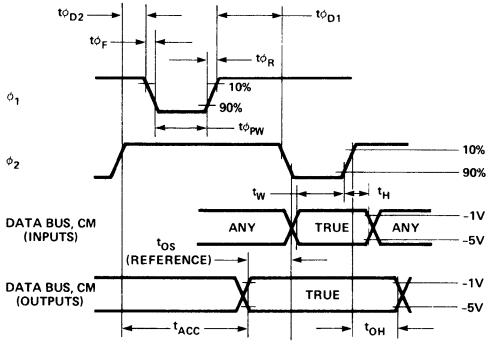
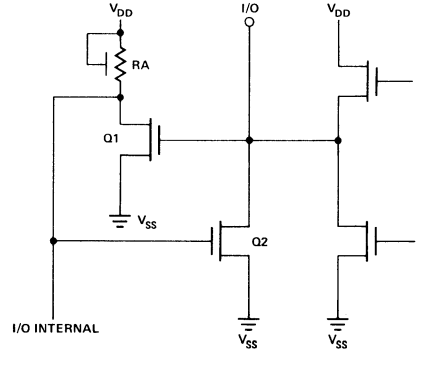


Figure 2. MCS-40 Timing Detail.



EXPLANATION:

WITH V_{SS} = +5V and V_{DD} = -10V, AN EXTERNAL TTL INPUTTING TO THE 4009 ON THE I/O LINE, RAISES THE I/O LINE TO 2.4V. THE Q1-RA INVERTER TURNS "OFF" AND Q2 PULLS THE I/O LINE TO V_{SS}. A LOW TTL SIGNAL OVERRIDES Q2. IF THE TTL OUTPUT GOES TO THE THIRD STATE, THE EXTERNAL I/O LINES REMAIN HIGH THROUGH Q2.

THE PURPOSE OF THIS CIRCUIT IS TO REMOVE RESISTORS TO $V_{CC} = V_{SS}$ ON TTL OUTPUTS, AS R_1 DOES ON 4001/4308 INPUT PORTS.

Figure 3. 4009 I/O Latch.

4289
STANDARD MEMORY INTERFACE

- **Direct Interface to all Standard Memories**
- **Allows Read and Write Program Memory**
- **Single Package Equivalent of 4008/4009**
- **TTL Compatible Address, Chip Select, Program Memory Data Lines**
- **40 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

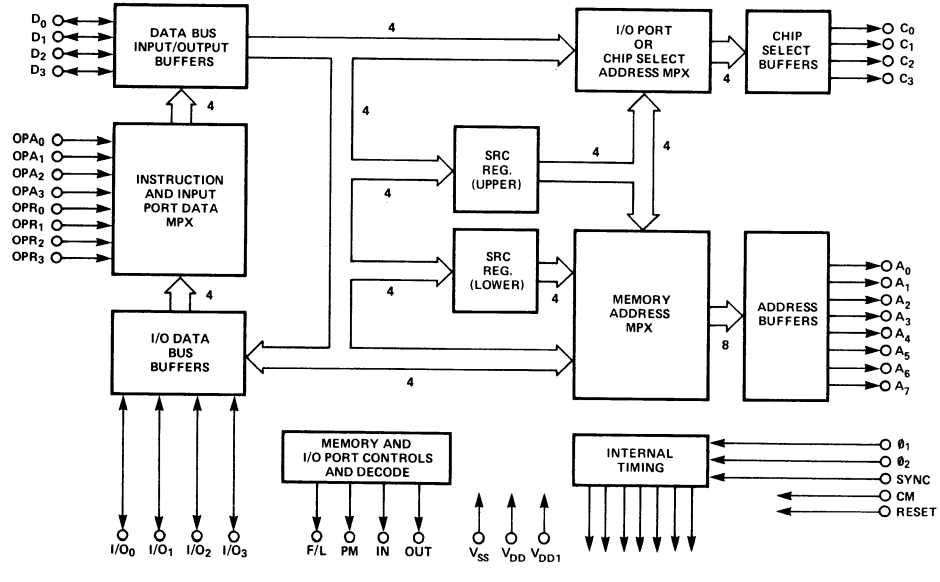
The 4289 standard memory interface and I/O interface enables the CPU devices to utilize standard memory components as program data memory. Notably, PROMs (4702A), RAMs (2102) and ROMs can be arranged in a memory array to facilitate system development. Programs generated using the 4289 interface can be committed to MCS-40™ ROMs (4308 and 4001) with no change to software.

The 4289 also contains a 4 bit bi-directional I/O port and necessary steering logic to multiplex a host of I/O sources to the CPU. The Read and Write Program Memory instruction allows the user to store data and modify program memory. The device directly addresses 4K of program memory. The address is obtained sequentially during A_1-A_3 states of an instruction cycle. The eight bit instruction is presented to the CPU during M_1 and M_2 states of the instruction cycle via the four bit data bus.

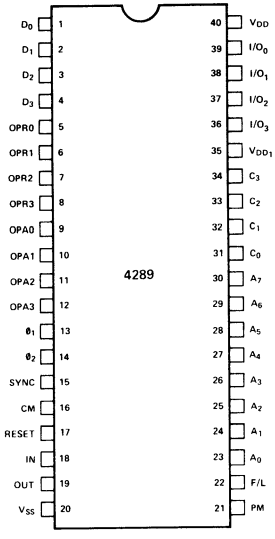
The 4289 stores the SRC instruction operand as an I/O address and responds to the ROM I/O instructions (WRR and RDR) by reading or writing data to and from the processor and 4289 I/O bus.

MCS 4/40

BLOCK DIAGRAM



PIN CONFIGURATION



Pin Description

Pin No.	Designation/ Type of Logic	Description of Function
1-4	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
5-8	OPR_0-OPR_3/Pos.	The high order 4 bits (OPR) of the instruction or data (RPM) from the PROGRAM MEMORY are transferred to the 4289 on these pins.
9-12	OPA_0-OPA_3/Pos.	The low order 4 bits (OPA) of the instruction or data (RPM) are transferred to the 4289 on these pins.
13-14	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
15	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
16	CM/Neg.	Command input driven by CM-ROM output of processor. Used for decoding SRC and I/O instructions.
17	RESET/Neg.	RESET input. A negative logic "1" level (V_{DD}) applied to this input resets the FIRST/LAST flip-flop.
18	IN/Neg.	Output signal, active low (V_{DD}), generated by the 4289 when the processor executes an RDR or RPM instruction.
19	OUT/Neg.	Output signal, active low (V_{DD}), generated by the 4289 when the processor executes a WRR or WPM instruction.
20	V_{SS}	Most positive supply voltage.
21	PM/Neg.	Output signal, active low (V_{DD}), generated by the 4289 when the processor executes an RPM or WPM instruction.
22	F/L/Neg.	Output signal generated by the 4289 to indicate which half-byte of PROGRAM MEMORY is to be operated on (V_{DD} = OPR, V_{SS} = OPA).
23-30	A_0-A_7/Pos.	Address output buffers. The demultiplexed address values generated by the 4289 from the address data supplied by the processor at A_1 and A_2.
31-34	C_0-C_3/Pos.	Chip select output buffers. The address data generated by the processor at A_3 or during an SRC are transferred here.
35	V_{DD1}	Supply voltage for address and chip select buffers.
36-39	I/O_3-I/O_0/Pos.	Bidirectional I/O data port. Data to and from I/O devices or data to write PROGRAM MEMORY are transferred via these pins.
40	V_{DD}	Main power supply pin. Value must be V_{SS} - 15V ± 5%.

Functional Description

The 4289 enables the 4 bit CPU chip (4004 or 4040) to interface to standard memory components. This allows construction of prototype or small volume systems using electrically programmable ROMs or RAMs in place of 4001 or 4308 mask programmable ROMs. Since 4001s or 4308s also contain up to 16 mask programmable I/O ports, the 4289 has provisions for directly addressing 16 channels of 4 bit I/O ports. In its role as a Memory and I/O interface device, the 4289 provides three different types of operation, namely:

a. Interface to Program Memory for instruction fetch operations.
b. Interface to Input/Output ports for storing or fetching data using WRR, RDR instruction.
c. Interface to R/W Program Memory for program alteration using WPM, RPM instructions. This feature may also be used for storing or fetching data, thus allowing the use of standard R/W RAM for data storage via the 4289.

These three basic operations will be discussed in detail in the following paragraphs.

Instruction Execution

The contents of the data bus at A_1, A_2, and A_3 are latched by the 4289 and transferred to the address and chip select output buffers. The low order address at A_1 is transferred to A_0-A_3 outputs, the middle order address at A_2 is transferred to A_4-A_7 outputs and the high order address at A_3 is transferred to C_0-C_3 outputs. These 12 output lines provide the necessary address and chip select signals to interface to a 4K x 8 bit Program Memory.

The 8 bit word selected by A_0-A_7 and C_0-C_3 is transferred to the processor via the $OPR_{0\text{-}3}$, $OPA_{0\text{-}3}$ input lines and the data output buffer. The high order bits (OPR) are transferred at M_1 and the low order 4 bits (OPA) are transferred at M_2.

The 4289 has been designed to work equally well with either the 4004 or 4040 processor elements. Since the 4040 is provided with two CM-ROM controls which allow it to directly address up to 8K x 8 bits of Program Memory (4K x 8 bits selected by each CM-ROM control), two 4289s would be required for full memory capability. In this case, one 4289 would be controlled by CM-ROM0 and the other by CM-ROM1. The 4289 which receives CM at A3 would be enabled to transfer data at M_1 and M_2.

It should be noted that the two CM-ROM controls permit the simultaneous use of 4001, 4308, and 4289 in the same system. The ROM's 4001 and 4308 can be mixed and assigned to one CM-ROM control line while a single 4289 can be assigned to the other. However, within one CM-ROM control line, 4289, 4001, and 4308 cannot be mixed, since the 4289 does respond to a full 4K of memory by its design and thus would overlap program memory address with the 4001 or 4308.

I/O Port Operation

When the processor executes an I/O port instruction (WRR or RDR), a previously selected I/O port (via an SRC instruction) is enabled to receive or transmit 4 bits of data. In the case of WRR, the selected output port receives the 4 bit contents of the processor accumulator, and in the case of RDR, the selected input port transmits 4 bits of data to the processor accumulator. The 4 bit value sent out at X_2 time of the SRC instruction is used as the port address. Since the 4289 is capable of addressing 16 4 bit I/O ports, it must therefore be capable of storing the SRC address sent by the processor and presenting that address to the external I/O port selection logic for WRR or RDR instructions which follow. To accomplish this, the 4289 behaves as follows:

a. When the processor executes an SRC instruction, the 4289 stores the address sent out by the processor at X_2 and X_3. The contents of the upper 4-bits of the SRC register are transferred during every X_1 time to the chip select lines and are available for subsequent I/O instructions' port selection.
b. When the processor then executes a WRR instruction, the 4289 latches the data sent out by the processor at X_2 and transfers this data to the I/O output buffer. This buffer is enabled during X_3 and transmits the data to the selected output port. So that external port logic may be enabled to receive the data, the 4289 generates the OUT strobe signal.
c. When the processor executes an RDR instruction, the 4289 generates the IN strobe. This enables the selected input port to transmit its data to the I/O bus, where it is latched by the 4289 and transferred to the processor at X_2.

Note that in a system using ROMs, the 4 bit port number is decoded by the ROM chip itself. Where a 4289 is used, the 4 bit port number outputted at the chip select lines C_0-C_3 must be externally decoded to select the appropriate I/O device.

Read/Write Program Memory Operations

If the 4289 is used in conjunction with the 4040, both the WRITE and READ PROGRAM MEMORY (WPM/RPM) functions are directly available (only the WPM is available for 4004 systems). To accomplish these operations, the following are required:

a. A program memory address.
b. The proper control signals.
c. A means of transmitting the data to be stored or fetched.

The 4289 provides all of these as described below.

Program Memory Address

The address for an RPM or WPM operation is provided by the 8 bit contents of the SRC register. Note that the RPM or WPM instruction must have been preceded by an SRC instruction which loaded an 8-bit address into the 4289's SRC register. This 8-bit address is the full address of an 8-bit word in one Read/Write Program Memory page (256 bytes). If more than one page of Read/Write Program Memory is desired, these pages must be selected by external logic controlled via other output ports of the system. At X_1 of every instruction cycle the 8 bit value contained in the SRC register is transferred to the address output buffers A_0-A_7. This address will select 1 out of 256 program memory words.

During execution of WPM or RPM, the 4289 does not transfer the high order 4 bits of the SRC register to C_0-C_3.

Instead, it forces all 4 chip select output buffers to a logic "1" state (positive true logic or V_{SS}). This forcing of C_0-C_3 to all "1s" can be used to indicate the execution of a WPM or RPM instruction. The PM output signal is also generated whenever a proper memory operation (WPM or RPM) is being performed. If only one page of R/W memory is required, the 1111 condition on C_0-C_3 or the PM signal can be used to enable that page. If more than one page is required, an additional output port of the system along with external logic will be necessary to provide the 1 out of 16 page select function.

Since the program memory is organized as 8 bit words, and since RPM and WPM are transmitting only 4 bit words, it is also necessary to specify either the upper or lower half-byte of program memory.

This is done automatically by a FIRST/LAST flip-flop and output signal in the 4289. The state of this flip-flop is used to generate the control signal F/L which determines the proper half-byte of program memory. If F/L is a logic "1" state (V_{DD}), OPR is selected. When F/L is a logic "0" (V_{SS}), OPA is selected. The user can directly reset the FIRST/LAST flip-flop to logic "0" (V_{SS}) in the 4289 by applying a RESET signal.

Starting from a "reset" condition the FIRST/LAST flip-flop automatically toggles after executing either an RPM or WPM instruction. Hence, odd numbered program memory operations select OPA and even numbered program memory operations select OPR (starting with #1 from reset). Alternate WPM and RPM instructions should be used with care since this can cause an out of sequence with the F/L line.

The OUT strobe signal is generated only during WRR and WPM instructions. Hence, the combination of the PM signal (or C_0-C_3 = 1111) and the OUT signal can be used as a WRITE ENABLE for R/W program memory.

Program Memory Data Paths

When the processor executes the WPM instruction, the 4289 latches the data sent out at X_2 by the processor and transfers it via the I/O output buffers to the I/O port. The I/O port must be connected to the data input pins of the R/W memory chips. (Refer to Figure 2 which follows.)

If the processor (4040) executes the RPM instruction, then the entire 8 bit program memory word is transferred to the OPR_0-OPR_3 and OPA_0-OPA_3 inputs of the 4289. Depending on the state of the F/L signal, either the OPA or the OPR half-byte is automatically selected by the 4289.

Data Storage

If Read/Write Memory is interfaced to a 4289 and is used for data storage only, the data is accessed via the WPM and RPM instructions just as Read/Write Program Memory would be accessed. The only difference that the chip select lines C_0-C_3 are never used to select the Read/Write Memory in an instruction fetch operation. The PM pulse would be used to select the Read/Write data memory.

Note that the RAM instructions RDM, WRM, WR0-WR3, RD0-RD3, SBM and ADM cannot be used to access this type of data Read/Write memory.

4008/4009 and 4289 Differences

The functional differences between a 4289 and a 4008/4009 Standard Memory Interface component pair are as follows:

1. The PM pulse of the 4289 (negative logic) is inverted in comparison with the W pulse of the 4008 (positive logic).
2. The W pulse of the 4008 begins in X2 and ends in X3. The 4289's PM pulse begins in X1 and ends in A1.
3. The OUT strobe of the 4289 goes to logical 1 (V_{DD}) for the WRR instructions and the WPM instructions. The OUT strobe of the 4009 goes to logical 1 (V_{DD}) for the WRR instruction only.

4289 Applications

The 4289 can be used to form systems of widely varying complexity. Simple systems containing only one page (256 x 8) of PROGRAM MEMORY and few I/O ports, or more complex systems requiring as many as 32 pages (8K x 8) of memory and 32 I/O ports can readily be implemented. Several examples will be described here.

1. Basic PROM Microcomputer System (Figure 1). This system contains:
   a. 1K x 8 bits of PROGRAM MEMORY (4702A PROM)
   b. 1280 bits of DATA MEMORY (4002 RAM) organized as 16 20-character registers
   c. 4 RAM output ports (4002)
   d. 4 I/O ports.

This system uses a 3205 1 out of 8 decoder to decode the input port addressed by the CPU. Two chip select signals (C_0 and C_1) are combined with the IN signal, which is activated low to indicate an input operation, to select one of four input ports. The 3205 enables one DM 7098 three-state buffer.

In a similar manner, one 3205 and the OUT signal, which is activated to indicate an output operation, are used to select one of four output ports.

2. Standard PROM and RAM Memory System (Figure 2). This system again contains 4 pages of PROM storage but, in addition, has one page of RAM storage which can be used for either PROGRAM or DATA storage by using the WPM/RPM instructions. (The RPM instruction is valid only with the 4040.) The RAM storage has been implemented with two 2101's (256 x 4 static RAM). Notice that separate WRITE ENABLE signals must be generated for the upper and lower half-bytes of RAM.

Note that the inputs to the 2101 RAMs are connected to the 4289 I/O port while their outputs are connected directly to the OPR-OPA lines.

The 2101 RAMs can be chip selected through their active low chip select lines in either of two cases:

1. By an address decode of 4 when the RAMs are addressed as Program Memory for instruction fetch.
2. By the PM signal when addressed as a RAM read or write via an RPM or WPM instruction. For write operations, the TTL logic shown selects one of the

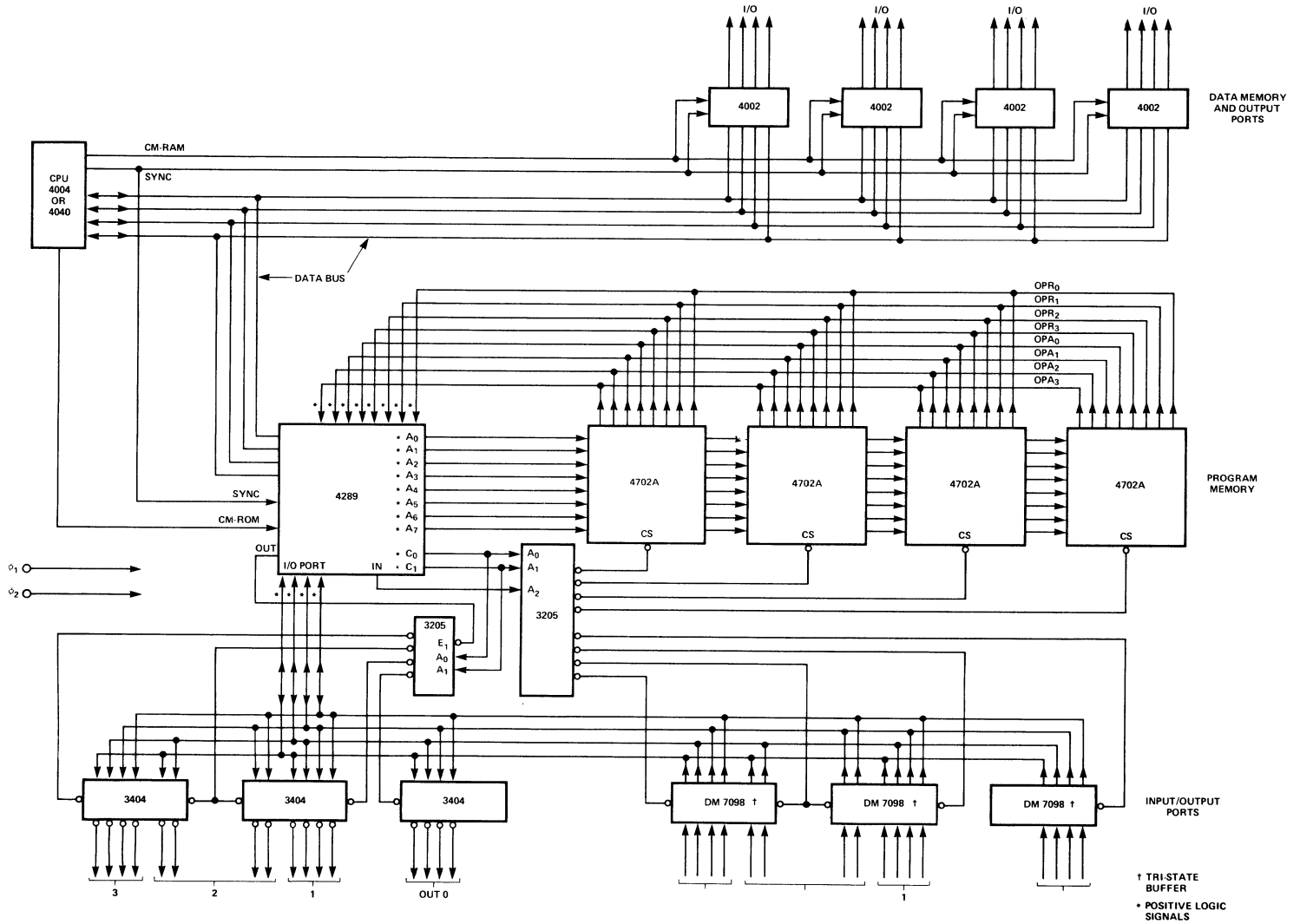


Figure 1. Basic PROM Memory System

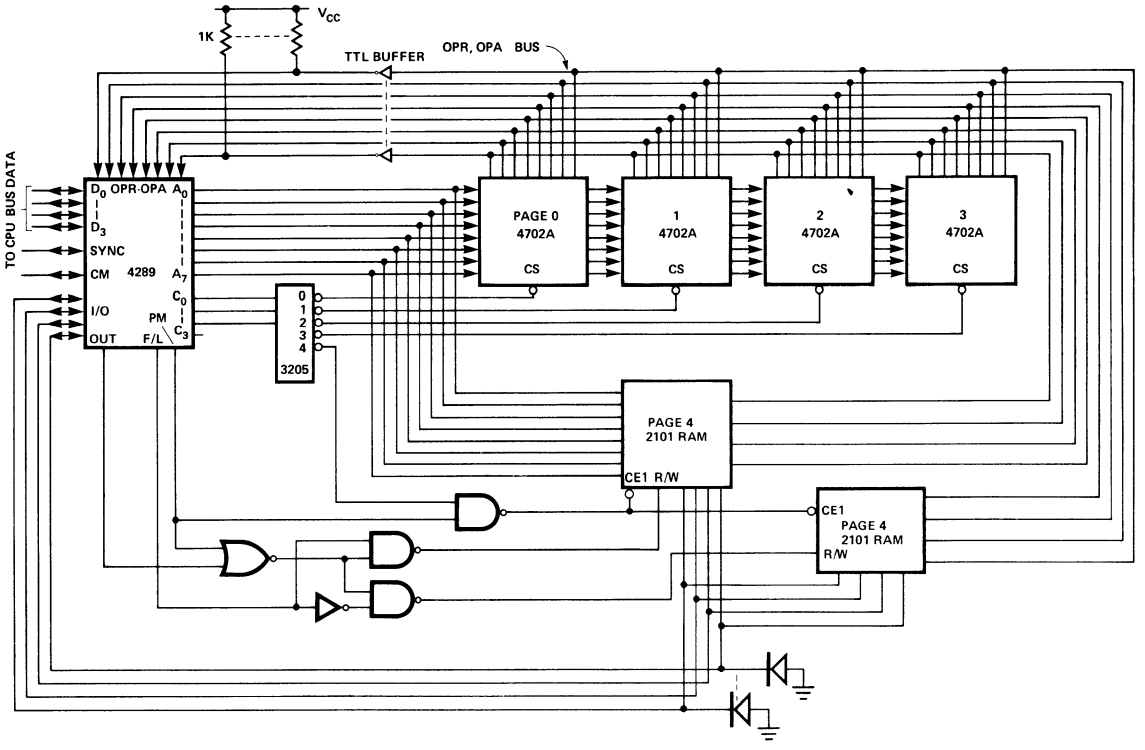


Figure 2. PROM and RAM System.

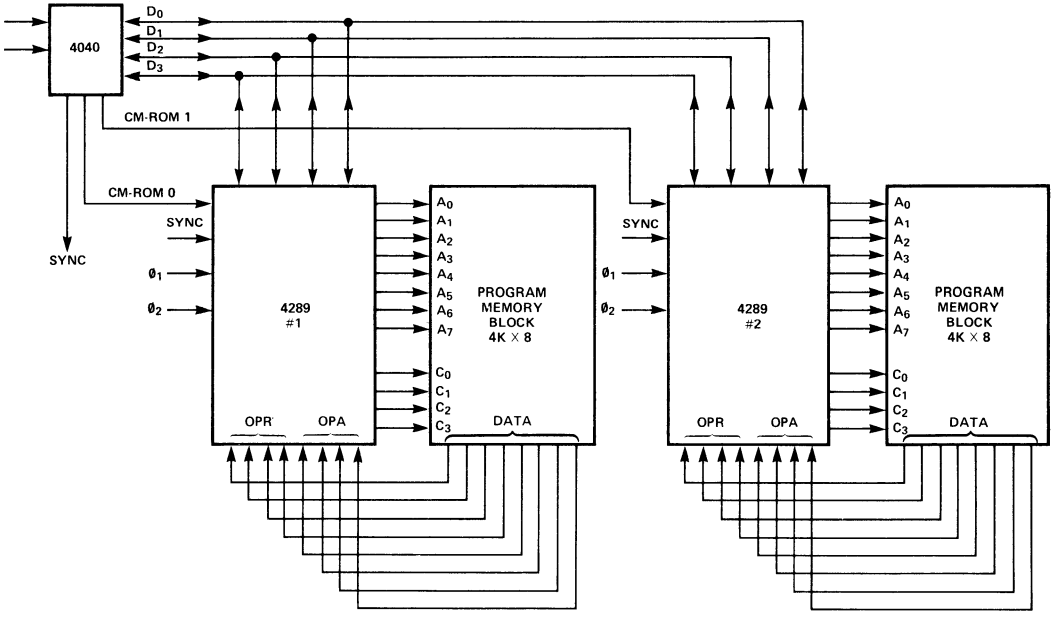


Figure 3. Two Memory Bank System.

two 2101 Read/Write lines according to the F/L signal of the 4289.

The TTL buffers are placed on the data bus to facilitate the compatability between the NMOS RAMs and the PMOS PROMS. The inverters limit the negative excursion of the PROM outputs which may damage the RAMs. The TTL pull-up is required to ensure the V_{IH} threshold level.

3. Two Memory Bank System (Figure 3). Two 4289s are used in this 4040 system giving addressability to a full 8K bytes of PROM memory. In this case each 4289 is controlled from a separate CM-ROM control signal. The CM-ROM$_0$ and CM-ROM$_1$ lines are generated by the 4040. This system cannot be implemented with the 4004.

4289, 4702A System Considerations

1. When utilizing the 4289 with more than six 4702As,a TTL buffer as shown in Figure 4 should be inserted in series with the OPR, OPA lines to achieve maximum clock rate. The buffer may be inverting or non-inverting.

   However, use of a 5.1KΩ resistor on the 4702A output to V_{SS} will allow up to 6 x 4702As to be used without TTL buffers and still achieve maximum clock rate.

2. 4702A access times to meet MCS-40 at $t_{CY} = 1.35\mu$ sec are guaranteed with pure capacitive load of 75pF and with load of 240pF plus a TTL buffer on the 4702A output.

   To operate with more than 6 x 4702A without TTL buffer, the limiting specification is t_{CO} and this increases 5 nsec/pF for capacitance above 75pF; MCS-40 t_{CY} must be increased 2.5ns/pF.

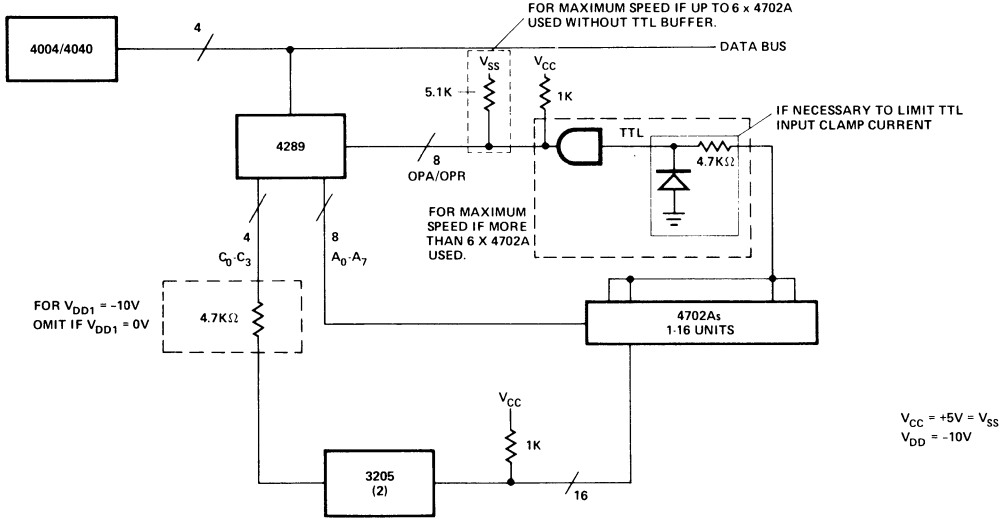


Figure 4. 4289 and 4702A Block Diagram.

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; 4289 V_{DD1} = V_{SS} -5V. Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		30	40	mA	T_A = 25°C

INPUT CHARACTERISTICS—ALL INPUTS EXCEPT I/O PINS

I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	OPR/OPA
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	

OUTPUT CHARACTERISTICS—ALL OUTPUTS EXCEPT I/O PINS

I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
I_{OL}[1]	Address Line Sinking Current	7	13		mA	V_{OUT} = V_{SS}, V_{DD1} = V_{DD}
I_{OL}	In, Out, F/L, PM Sinking Current, Chip Select	1.6	4		mA	V_{OUT} = V_{SS} -4.85 V_{DD1} = V_{DD}
V_{OL}[2]	Chip Select Output Low Voltage			V_{DD1}+.5	V	I_{OL} = .4mA
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT} = V_{SS} -.5V
R_{OH}	Address, Chip Select Output Resistance, "0" Level		.6	1.2	kΩ	V_{OUT} = V_{SS} -.5V

I/O INPUT CHARACTERISTICS

I_{LI}	Input Leakage Current			10	μA	
V_{IH}[3]	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	

I/O OUTPUT CHARACTERISTICS

V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance		.25	1.0	kΩ	V_{OUT} = V_{SS}-.5
I_{OL}	I/O Output "1" Sink Current	5	12		mA	V_{OUT} = V_{SS} -.5
I_{OL}	I/O Output "1" Sink Current	1.6	4		mA	V_{OUT} = V_{SS} -4.85V
I_{CF}	I/O Output "1" Clamp Current			10	mA	V_{OUT} = V_{SS} -6V

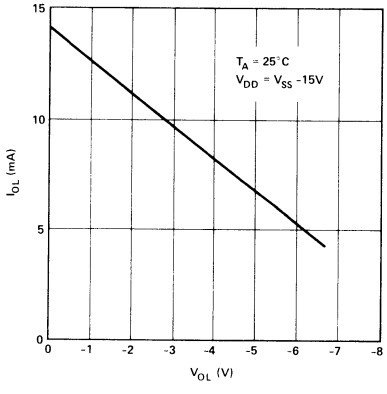
Notes: 1. The address lines will drive a TTL load if a 470Ω resistor is connected in series between the address output and the TTL input.
2. 4289 Address (A_0-A_7) Outputs are also tied to V_{DD1} but are tested with capacitive load only.
3. TTL V_{OH} = 2.4V will ensure 4289 V_{IH} = V_{SS} -1.5V via the 4289 latch. Refer to Figure 5.

D.C. and Operating Characteristics (Continued)

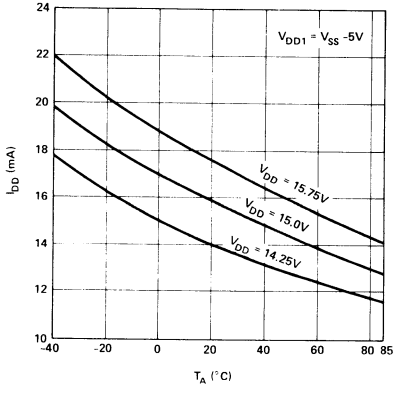
CAPACITANCE

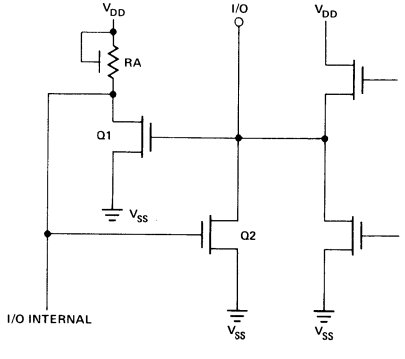
Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
C_ϕ	Clock Capacitance		14	20	pF	$V_{IN} = V_{SS}$
C_{DB}	Data Bus Capacitance		7	10	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance			15	pF	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance			10	pF	$V_{IN} = V_{SS}$

4289 I_{OL} VS. V_{OL} (FOR I/O PINS)



4289 I_{DD} VS. TEMPERATURE





EXPLANATION:

WITH V_{SS} = +5V and V_{DD} = -10V, AN EXTERNAL TTL INPUTTING TO THE 4289 ON THE I/O LINE, RAISES THE I/O LINE TO 2.4V. THE Q1-RA INVERTER TURNS "OFF" AND Q2 PULLS THE I/O LINE TO V_{SS}. A LOW TTL SIGNAL OVERRIDES Q2. IF THE TTL OUTPUT GOES TO THE THIRD STATE, THE EXTERNAL I/O LINES REMAIN HIGH THROUGH Q2.

THE PURPOSE OF THIS CIRCUIT IS TO REMOVE RESISTORS TO $V_{CC} = V_{SS}$ ON TTL OUTPUTS, AS R_I DOES ON 4001/4308 INPUT PORTS.

Figure 5. 4289 I/O Latch.

A.C. Characteristics

T_A = 0°C to 70°C, V_{SS} -V_{DD} = 15V ±5%

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Time			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{A1}[4]	ϕ_1 to Output Delay A_1		400	1000	ns	C_L = 250pF; A_0-A_3
t_{TA1}[4]	Data Bus to Output Delay A_1		500	700	ns	C_L = 250pF; A_0-A_3
t_{A2}[4]	ϕ_1 to Output Delay A_2		400	580	ns	C_L = 250pF; A_4-A_7
t_{TA2}[4]	Data Bus to Output Delay A_2		500	700	ns	C_L = 250pF; A_4-A_7
t_{CS}[4,5]	ϕ_1 to Chip Select Output Delay A_3		150	350	ns	C_L = 50pF
t_{TC}[4,5]	Data Bus to Chip Select Output Delay A_3		250	350	ns	C_L = 50pF
t_{WID}	OPR to Data Bus Delay		250	350	ns	C_{OUT} = 20pF, Data Bus
t_{SRC}	Output Delay at X_1 Time		400	700	ns	C_L = 250pF
t_{S1}	IN Strobe Delay Time			500	ns	C_L = 50pF
t_{S2}	OUT Strobe Delay Time, Falling			500	ns	C_L = 50pF
t_{FD}	F/L and PM Delay Time		300	500	ns	C_L = 100pF
$t_{W,I/O}$	I/O Input Write Time	400	250		ns	
$t_{H,I/O}$	I/O Input Hold Time	40	0		ns	
$t_{D,I/O}$	I/O Output Delay Time		400	1000	ns	C_L = 300pF
t_{WI}	Data In Write Time	350			ns	C_{OUT} = 200pF, Data Bus

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.

2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.

3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

4. t_{A1}, t_{A2}, t_{CS} apply if Data Bus is valid before ϕ_1 trailing edge. t_{TA}, t_{TC} apply if Data Bus becomes valid after ϕ_1 trailing edge.

5. Measured at output of 3205 decoder.

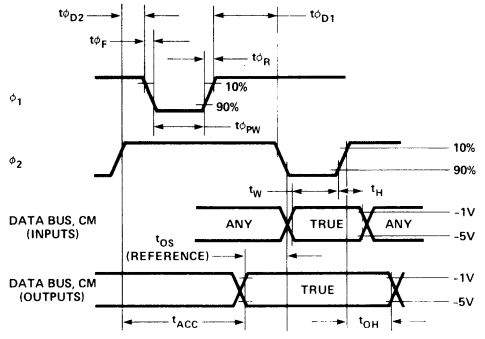


Figure 6. MCS-40 Timing Detail.

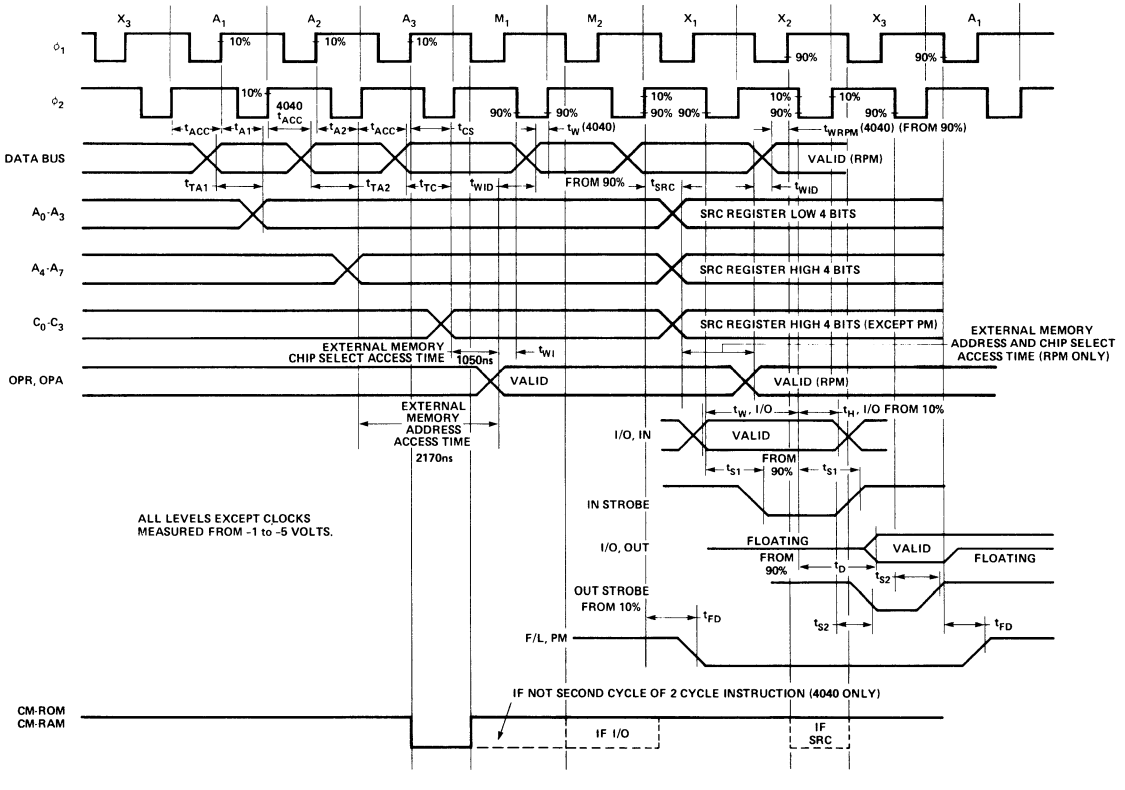


Figure 7. MCS-40 Timing Diagram for 4289.

4002

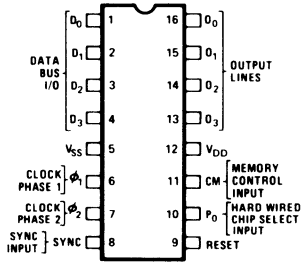
320 BIT RAM AND 4 BIT OUTPUT PORT

- **Four Registers of 20 4 Bit Characters**
- **Direct Interface to MCS-40™ 4 Bit Bus**
- **Output Port Low-Power TTL Compatible**
- **16 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available With -40° to +85°C Operating Range**

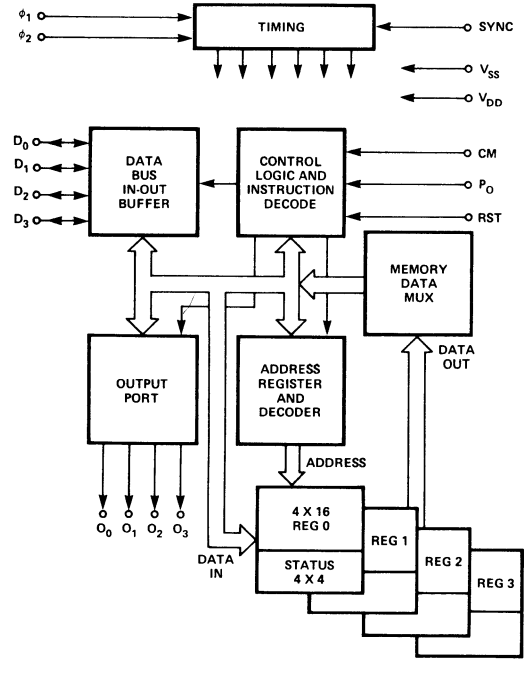
The 4002 performs two distinct functions. As a RAM it stores 320 bits arranged in 4 registers of twenty 4 bit characters each (16 main memory characters and 4 status characters). As a vehicle of communication with peripheral devices, it is provided with 4 output lines and associated control logic to perform output operations. The 4002 is a PMOS device and is compatible with all MCS-40™ components.

The 4002 is available in two options, the 4002-1 and 4002-2. Along with an external pin connected to either V_{DD} or V_{SS}, a two bit chip selection address is provided allowing a maximum of 1280 bits of 4002 RAM on a single MCS-40 CM-RAM line. Thus, the four CM-RAM lines give a maximum of 5120 bits of 4002 RAM in an MCS-40 system.

PIN CONFIGURATION



BLOCK DIAGRAM



Pin Description

Pin No.	Designation	Description of Function
1-4	D_0-D_3	Bidirectional data bus. All address, instruction and data communication between processor and the RAM MEMORY or the output port is transmitted on these 4 pins.
5	V_{SS}	Most positive supply voltage.
6-7	ϕ_1-ϕ_2	Non-overlapping clock signals which are used to generate the basic chip timing.
8	SYNC	Synchronization input signal driven by SYNC output of processor.
9	RESET	RESET input. A logic negative level (V_{DD}) applied to the chip will cause a clear of all output and control static flip-flops and will clear the RAM array. To completely clear the memory, RESET must be applied for at least 32 instruction cycles (256 clock periods) to allow the internal refresh counter to scan the memory. During RESET the data bus output buffers are inhibited (floating condition).
10	Po	The chip number for a 4002 is assigned as follows:

Chip No.	4002 Option	P_0	SRC ADDRESS (RRR EVEN) D_3 D_2
0	4002-1	V_{SS}	0 0
1	4002-1	V_{DD}	0 1
2	4002-2	V_{SS}	1 0
3	4002-2	V_{DD}	1 1

11	CM	Command input driven by CM-RAM output of processor. Used for enabling the device during the decoding SRC and instructions.
12	V_{DD}	Main power supply pin. Value must be V_{SS} - 15V ± 5%.
13-16	O_3-O_0	Four bit output port used for transferring data from the CPU to the users system. The outputs are buffered and data remains stable after the port has been loaded. This port can be made low power TTL compatible by placing a 12K pull-down resistor to V_{DD} on each pin.

Functional Description

The twenty 4 bit characters for each 4002 register are arranged as follows:

1. 16 characters addressable by an SRC instruction. Four 16 character registers constitute the "main" memory.
2. 4 characters addressable by specific RAM instructions. Four 4 character registers constitute the "status character" memory.

The status character location (0 through 3) as well as the operation to be performed on it are selected by the OPA portion of the I/O and RAM instructions.

The RAM Registers Locations, Status Characters, and Output Port are select and accessed with a corresponding RAM Instruction.

There can be up to four RAMS per RAM Bank (CM-RAM). There can be four RAM banks per system without decoding or 8 with decoding.

Bank switching is accomplished by the CPU after receiving a "DCL" (designated command line) instruction. Prior to execution of the DCL instruction the desired CM-RAM code has been stored in the accumulator (for example through an LDM instruction). During DCL the CM-RAM code is transferred from the accumulator to the CM-RAM register. The RAM bank is then selected starting with the next instruction.

If no DCL is executed prior to SRC, the CM-RAM_0 will automatically be activated at the X_2 state of the instruction cycle provided that RESET was applied at least once to the system (most likely at the start-up time).

MCS 4/40

Instruction Execution

An SRC (Send Register Control) instruction is executed to select a RAM and a character within that RAM (for a RAM read or write instruction) prior to the succeeding RAM or I/O instruction's execution.

The eight bits of the register pair addressed by the SRC instruction are interpreted as follows:

a. The first four bits sent out at X_2 time select one out of four chips and one out of four registers. The two higher order bits (D_3, D_2) select the chip and the two lower order bits (D_1, D_0) select the register.

b. The second 4-bits (X_3 time) select one 4-bit character out of 16. The address is stored in the address register of the selected chip (second 4 bits are not used for status character reads or writes or for I/O output instructions).

The following RAM and I/O output instructions are executed by the 4002.

1. RDM Read RAM character

   The content of the previously selected RAM main memory character is transferred to the accumulator. The 4 bit data in memory is unaffected.

2. RDO-3 Read RAM status characters 0-3

   The 4 bits of status characters 0-3 for the previously selected RAM register are transferred to the accumulator.

3. WRM Write accumulator into RAM character

   The accumulator content is written into the previously selected RAM main memory character location.

4. WRO-3 Write accumulator into RAM status characters 0-3

   The content of the accumulator is written into the RAM status characters 0-3 of the previously selected RAM register.

5. WMP Write memory port

   The content of the accumulator is transferred to the RAM output port of the previously selected RAM chip. The data is available on the output pins until a new WMP is executed on the same RAM chip. The content of the ACC and the carry/link are unaffected. (The LSB bit of the accumulator appears on O_0, Pin 16 of the 4002.)

6. ADM Add from memory with carry

   The content of the previously selected RAM main memory character is added to the accumulator with carry. The RAM character is unaffected.

7. SBM Subtract from memory with borrow

   The content of the previously selected RAM character is subtracted from the accumulator with borrow. The RAM character is unaffected.

Timing Considerations

Presence of CM-RAM during X_2 tells 4002's that an SRC instruction was received. For a given combination of data at X_2 on D_2, D_3, only the chip with the proper option and P_0 state will be ready for the I/O or RAM operation that follows.

When an I/O or RAM instruction is received by the CPU, the CPU will activate one CM-RAM line during M_2, in time for the 4002's to receive the OPA (2nd part of the instruction), which will specify the I/O or RAM operation to be performed.

In the I/O mode of operation, the selected 4002 chip (by SRC), after receiving the OPA of an I/O instruction (CM-RAM activated at M_2), will decode the instruction.

If the instruction is WMP, the data present on the data bus during $X_2 \cdot \phi_2$ will set the output flip-flops associated with the I/O pins. That information will be available until next WMP for peripheral devices control.

In the RAM mode, the operation is as follows: When the CPU receives an SRC instruction, it will send out the content of the designated index register pair during X_2 and X_3 and will activate one CM-RAM line at X_2 for the previously selected RAM bank.

All RAM mode instructions will be executed during the X_2 and X_3. The instruction decoding is performed during the M_2 time when the OPA portion of the instruction is decoded. The CM-RAM of the selected Bank is enabled at that time.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to V_{SS}	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

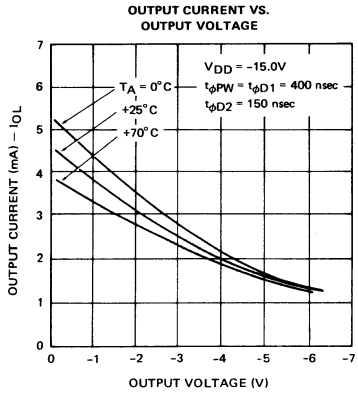
T_A = 0°C to 70°C; V_{SS}-V_{DD} = 15V ±5%; $t_{\phi PW} = t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec. Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless otherwise specified.

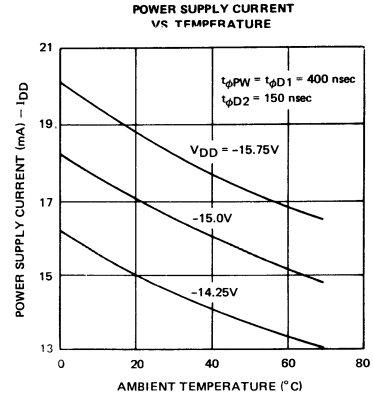
SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		17	33	mA	T_A = 25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	V_{IL}=V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS – ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT}=-12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT}=V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL}=0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT}=V_{SS}-.5V
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT}=0
R_{OH}	I/O Output "0" Resistance		1.2	2	kΩ	V_{OUT}=V_{SS}-.5V
I_{OL}	I/O Output "1" Sink Current	2.5	5		mA	V_{OUT}=V_{SS}-.5V
I_{OL}[1]	I/O Output "1" Sink Current	0.8	3		mA	V_{OUT}=V_{SS}-4.85V
V_{OL}	I/O Output Low Voltage	V_{SS}-12		V_{SS}-6.5	V	I_{OUT}=50μA
CAPACITANCE						
C_{ϕ}	Clock Capacitance		8	15	pF	V_{IN}=V_{SS}
C_{DB}	Data Bus Capacitance		7	10	pF	V_{IN}=V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN}=V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN}=V_{SS}

Note: 1. For TTL compatibility, use 12kΩ external resistor to V_{DD}.

Typical D.C. Characteristics





A.C. Characteristics

T_A = 0°C to 70°C, V_{SS}-V_{DD} = 15V ±5%.

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t_{\phi R}$	Clock Rise Time			50	ns	
$t_{\phi F}$	Clock Fall Times			50	ns	
$t_{\phi PW}$	Clock Width	380		480	ns	
$t_{\phi D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t_{\phi D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT}=20pF
t_D	I/O Output Delay			1500	ns	C_{OUT}=100pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.

2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.

3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

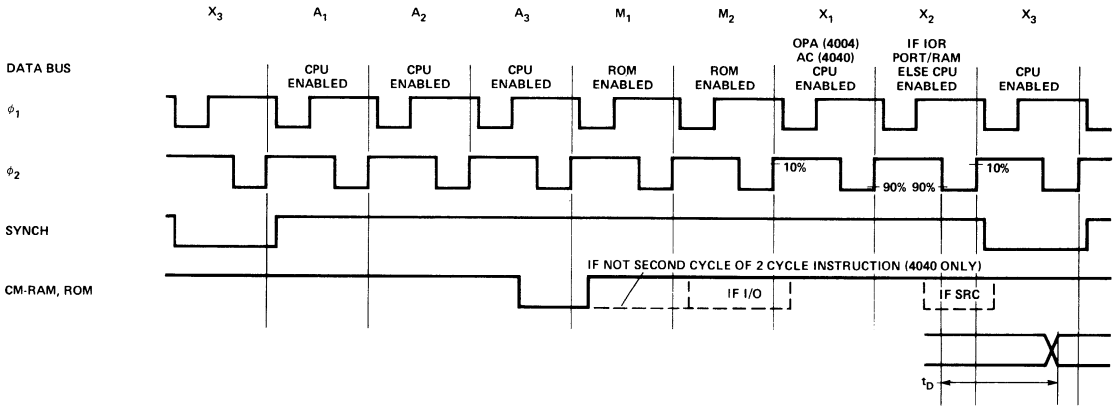


Figure 1. Timing Diagram.

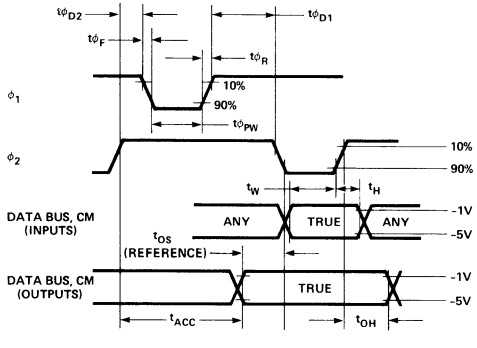


Figure 2. Timing Detail.

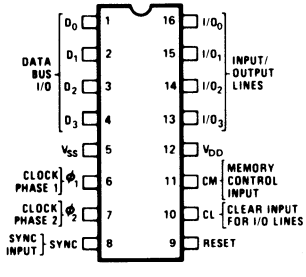
4001

256 x 8 MASK PROGRAMMABLE ROM AND 4 BIT I/O PORT

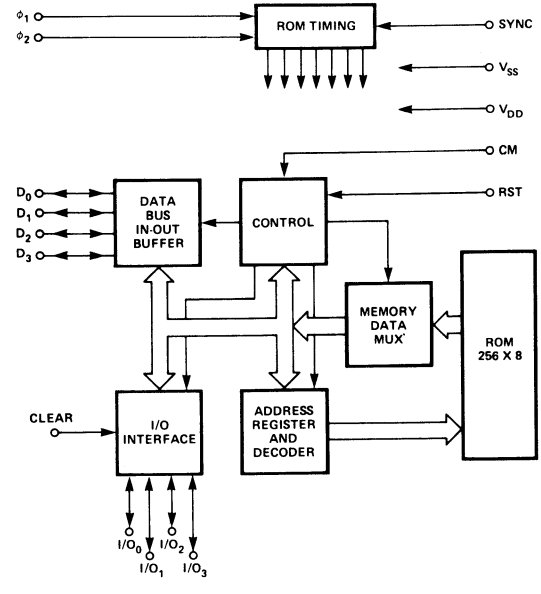
- **Direct Interface to MCS-40™ 4 Bit Data Bus**
- **I/O Port Low-Power TTL Compatible**
- **16 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4001 performs two basic and distinct functions. As a ROM it stores 256 x 8 words of program or data tables; as a vehicle of communication with peripheral devices it is provided with 4 I/O pins and associated control logic to perform input and output operations. The 4001 is a PMOS device, compatible with all other MCS-40™ devices.

PIN CONFIGURATION



BLOCK DIAGRAM



Pin Description

Pin No.	Designation/ Type of Logic	Description of Function
1-4	D_0 -D_3/Neg.	Bidirectional data bus. All address and data communication between the processor and ROM is handled by these lines.
5	V_{SS}	Most positive supply voltage.
6-7	$\phi 1$, $\phi 2$/Neg.	Non-overlapped clock signals which determine device timing.
8	SYNC/Neg.	System synchronization signal generated by processor.
9	RESET/Neg.	Reset input. A negative level (V_{DD}) on this pin will clear internal flip-flops and buffers. The input buffers are not cleared by this signal.
10	CL/Neg.	Clear input for I/O lines. A negative level on this pin will clear the I/O buffers. This pin may be driven by a TTL output and a 1K pull-up to V_{SS}.
11	CM-ROM/Neg.	Chip enable generated by the processor.
12	V_{DD}	Main supply voltage value. Must be V_{SS} – 15.0V ±5%.
13-16	I/O_0-I/O_3/Neg.	A single I/O port consisting of 4 bidirectional and selectable lines.

Functional Description

Address and data are transferred in and out by time multiplexing on 4 data bus lines. Timing is internally generated using two clock signals, ϕ_1 and ϕ_2, and a SYNC signal supplied by the CPU. Addresses are received from the CPU on three time periods following SYNC, and select 1 out of 256 words and 1 out of 16 ROM's. For that purpose, each ROM is identified as #0, 1, 2, through 15, by metal option. A Command ROM Line (CM-ROM) is also provided and it is used to select a ROM bank (group of 16 ROM's).

During the two time periods of the instruction cycle (M_1 & M_2) following the addressing time, information is transferred from the ROM to the data bus lines.

A second mode of operation of the ROM is as an Input/Output control device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O external lines. Each chip has the capability to identify itself for an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and execute the instruction. An external signal (CL) will asynchronously clear the output register during normal operation.

All internal flip flops (including the output register) will be reset when the RESET line goes low (V_{DD}).

I/O Options

Each I/O pin on each ROM can be uniquely chosen to be either an input or output line by metal option. Also each input or output can either be inverted or direct. When the pin is chosen as an input it may have an on-chip resistor connected to either V_{DD} or V_{SS}.

Instruction Execution

The 4001 responds to the following instructions.

1. **SRC Instruction** (Send address to ROM and RAM)

   When the CPU executes an SRC instruction it will send out 8 bits of data during X_2 and X_3 and will activate the CM-ROM and one CM-RAM line at X_2. Data at X_2, (representing the contents of the first register of the register pair addressed by the SRC instruction) with simultaneous presence of CM-ROM, is interpreted by the 4001 as the chip number of the unit that should later perform an I/O operation. Data at X_3 is ignored.

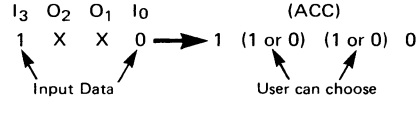
2. **WRR – Write ROM Port**

   The content of the accumulator is transferred to the ROM output port of the previously selected ROM chip. The data is available on the output pins until a new WRR is executed on the same chip. The ACC content and carry/link are unaffected. (The LSB bit of the accumulator appears on I/O_0.) No operation is performed on I/O lines coded as inputs.

3. **RDR – Read ROM Port**

   The data present at the input lines of the previously selected ROM chip is transferred to the accumulator.

   If the I/O option has both inputs and outputs within the same 4 I/O lines, the user can choose to have either "0" or "1" transferred to the accumulator for those I/O pins coded as outputs, when an RDR instruction is executed. For example, given a port with the I/O lines coded with 2 inputs and 2 outputs, when RDR is executed, the transfer is as shown below:



Timing Consideration

In the ROM mode of operation the 4001 will receive an 8 bit address during A_1 and A_2 times of the instruction cycle and a chip number, together with CM-ROM, during A_3 time. When CM-ROM is present, only the chip whose metal option code matches the chip number code sent during A_3 is allowed to send data out during the following two cycles: M_1 and M_2. The activity of the 4001 in the ROM mode ends at M_2.

The 4001 can have a chip number via the metal option from 0 – 15.

In the I/O mode of operation, the selected 4001 (by SRC), after receiving RDR will transfer the information present at its I/O pins to the data bus at X_2. If the instruction received was WRR, the data present on the data bus at $X_2 \cdot \phi_2$ will be latched on the output flip-flops associated with the I/O lines.

Ordering Information

When ordering a 4001, the following information must be specified:

1. Chip number
2. All the metal options for *each* I/O pin.
3. ROM pattern to be stored in each of the 256 locations.

A blank customer truth table is available upon request from Intel. A copy of this table is shown and blank copy can be found following the detailed 4001 characteristics.

EXAMPLES – DESIRED OPTION/CONNECTIONS REQUIRED

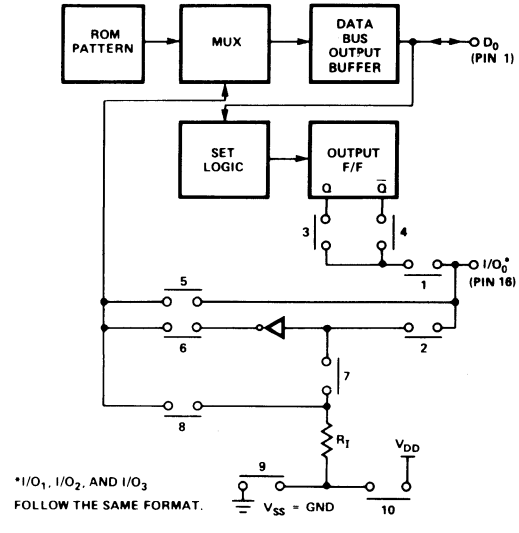
1. Non-inverting output (negative logic output) – 1 and 3 are connected.
2. Inverting output (positive logic output) – 1 and 4 are connected.
3. Non-inverting input (no input resistor – negative logic input) – only 5 is connected.
4. Inverting input (input resistor to V_{SS} – positive logic input) – 2, 6, 7, and 9 are connected.
5. Non-inverting input (input resistor to V_{DD} – negative logic input) – 2, 7, 8, and 10 are connected.
6. If inputs and outputs are mixed on the same port, the pins used as the outputs must have the internal resistor connected to either V_{DD} or V_{SS} (8 and 9 or 8 and 10 must be connected). This is necessary for testing purposes. For example, if there are two inverting inputs (with no input resistor) and 2 non-inverting outputs the connection would be made as follows:

   Inputs – 2 and 6 are connected
   Outputs – 1, 3, 8 and 9 are connected or
   1, 3, 8 and 10 are connected

   If the pins on a port are all inputs or all outputs, the internal resistors do not have to be connected.

It should be noted that all internal logic and processing is performed in negative logic, i.e., "1" equals V_{DD} and "0" equals V_{SS}. For positive logic conversion, the inverted options should be selected.

TTL compatibility is obtained by $V_{DD} = -10V \pm 5\%$ and $V_{SS} = 5V \pm 5\%$. An external 12K resistor should be used on all outputs to insure the logic "0" state (V_{OL}).



4001 Available Metal Option for Each I/O Pin.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to V_{SS}	+0.5V to -20V
Power Dissipation	1.0 Watt

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

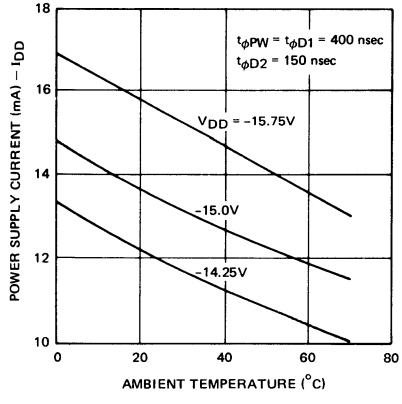
T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
SUPPLY CURRENT						
I_{DD}	Average Supply Current		15	30	mA	T_A = 25°C
INPUT CHARACTERISTICS – ALL INPUTS EXCEPT I/O PINS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS – ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT} = V_{SS} -.5V
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IH}	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage, Inverting Input	V_{DD}		V_{SS}-4.2	V	
V_{IL}	Input Low Voltage, Non-inverting Input	V_{DD}		V_{SS}-6.5	V	
V_{IL}	CL Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
R_I	Input Resistance, if Used	10	18	35	kΩ	R_1 tied to V_{SS}; V_{IN} = V_{SS} -3V
R_1[1]	Input Resistance, if Used	15	25	40	kΩ	R_1 tied to V_{DD}; V_{IN} = V_{SS} -3V
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance		1.2	2	kΩ	V_{OUT} = V_{SS} -.5V
I_{OL}	I/O Output "1" Sink Current	2.5	5		mA	V_{OUT} = V_{SS} -.5V
I_{OL}[2]	I/O Output "1" Sink Current	0.8	3		mA	V_{OUT} = V_{SS} -4.85V
V_{OL}	I/O Output Low Voltage	V_{SS}-12		V_{SS}-6.5	V	I_{OUT} = 50μA
CAPACITANCE						
C_ϕ	Clock Capacitance		8	15	pF	V_{IN} = V_{SS}
C_{DB}	Data Bus Capacitance		9.5	15	pF	V_{IN} = V_{SS}
C_{IN}	Input Capacitance			10	pF	V_{IN} = V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN} = V_{SS}

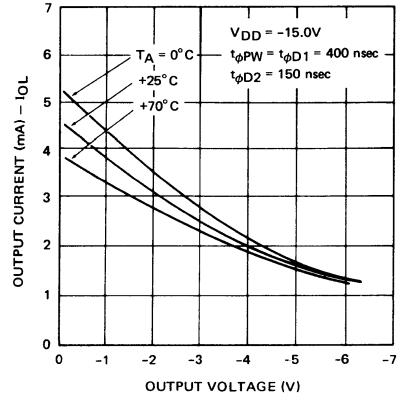
Notes: 1. R_1 is large signal equivalent resistance to (V_{SS}-12) V.
2. For TTL compatibility, use 12kΩ external resistor to V_{DD}.

Typical D.C. Characteristics

POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT CURRENT VS. OUTPUT VOLTAGE



A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{SS} - V_{DD} = 15V \pm 5\%$

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Times			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{IS}	I/O Input Set-Time	50			ns	
t_{IH}	I/O Input Hold-Time	100			ns	
t_D	I/O Output Delay			1500	ns	C_{OUT} = 100pF
t_C[4]	I/O Output Lines Delay on Clear			1500	ns	C_{OUT} = 100pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.

2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.

3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

4. CL on the 4001 is used to asynchronously clear the output flip-flops associated with the I/O lines.

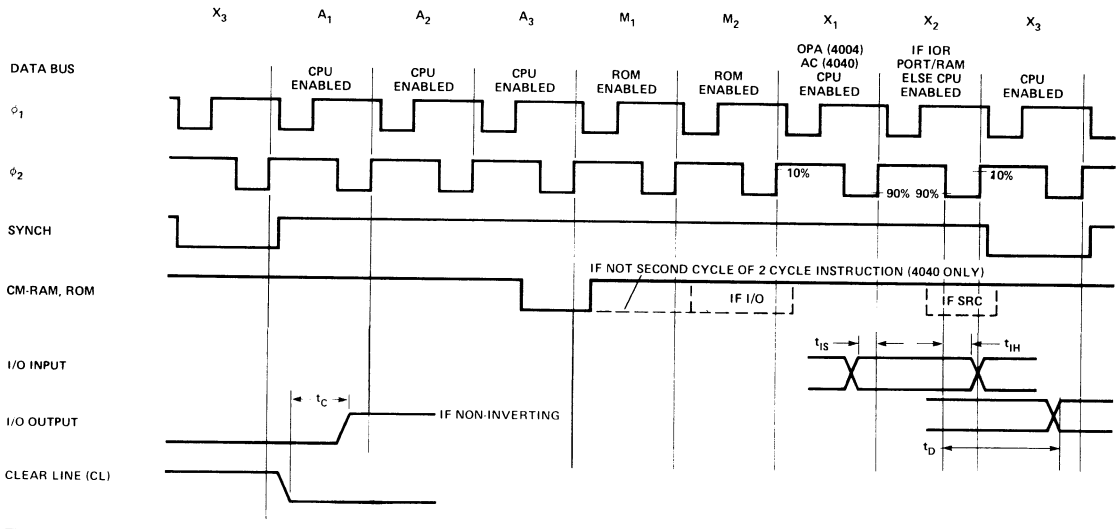


Figure 1. Timing Diagram

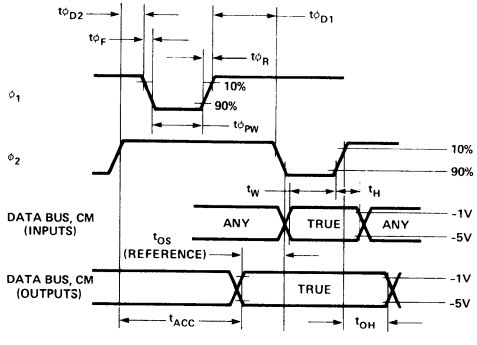


Figure 2. Timing Detail

Programming Instructions

To insure optimum handling of ROM programs and avoid delays, programs should be specified in the following format.

Paper Tape Format*

A 1" wide paper tape using 8 bit ASCII code, such as a model 33ASR teletype produces:

A. Preamble

1. Preceding the first word field and following the last word field, there should be a leader/trailer length of at least 25 characters. This should consist of rubout punches.

2. Included in the tape before the leader, and preceded by another leader, should be the customer's complete telex or twx number and if more than one pattern is being transmitted, the ROM pattern number.

3. The first ROM pattern preamble field is the device type number or ROM number. The field should be framed by an "I" and "–"

   I4001–

   This should be followed by the chip select information encoded in decimal (two digits), and enclosed by "C" and "S", as in

   "ChhS"

   The valid select digits for the 4001 are 0–15

   "C0S" – "C15S"

   Finally, the I/O options would be specified on a port-by-port basis with the connections to be made separated by commas, and enclosed in parentheses:

   "(n1, n2, n3 . . .)".

   where (n1, n2 . . .) are the option numbers associated with one I/O line. Hence, for a 4001 there will be four bracketed collections of I/O options.

   Each I/O pin has a series of 10 possible connections. These connections are consecutively numbered from 1-10. It is these numbers that should be in parentheses for each I/O pin.

   Example: "( )" indicates no connection
   "(1)" indicates only #1
   "(2,5,7)" indicates connections #2, 5 and 7.

   I/O options should be placed on the tape sequentially for the 4001 from I/O0–I/O3(4). Always avoid illegal combinations.

NOTE: Cards may also be submitted.

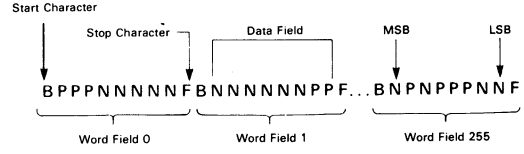
B. ROM Code

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.

2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F. Within the word field, a P results in a high level output (V_{SS} or logic 0 for MCS-40 CPUs) and a N results in a low level output (V_{DD} or logic 1 for MCS-40 CPUs).

   Example of 256 x 8 format (N=256):



3. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. It may be helpful to insert the word number (as a comment) at least every four word fields.

4. Within the ROM pattern words a character, "X", may be used. Where "P" and "N" indicate a "0" and "1" setting respectively, an "X" will indicate a single bit – "Don't Care" setting. This allows the optimum default bit values to be selected by Intel. The bit value will be fixed to allow for testing. The values will be specified to the user on the Verification Listing tape.

   In the place of a standard BPNF word, a "B*nF" word may be used. This indicates that the data in the last BPNF word encountered is to be repeated for the next n words ($1 \leq n \leq 1023$). Note that if a repeat count of 4 is given in word position 10, then words 10, 11, 12, and 13 will be repeats of word 9 (except for Don't Care bits which might conceivably have different assigned values).

   To indicate that an entire block (such as the remainder of a ROM) is not used (i.e., Don't Care), a word of Don't Care data can be followed by the remaining word count in a repeat count form.

MCS® CUSTOM ROM ORDER FORM

4001 ROM

CUSTOMER_____

P.O. NUMBER_____

DATE_____

For Intel use only

S#_____ PPPP_____

STD_____ ZZ_____

_____ DD_____

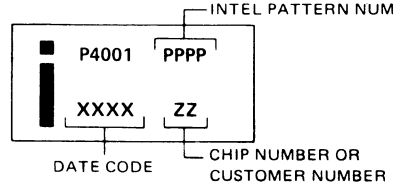
APP_____ DATE_____

All custom 4001 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4001), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).

CUSTOMER NUMBER _____



MCS 4/40

MASK OPTION SPECIFICATIONS

A. CHIP NUMBER _____.
(Must be specified—any number from 0 through 15—DD).

B. I/O OPTION – Specify the connection numbers for each I/O pin (next page). Examples of some of the possible I/O options are shown below:

EXAMPLES – DESIRED OPTION/CONNECTIONS REQUIRED

1. Non-inverting output – 1 and 3 are connected.
2. Inverting output – 1 and 4 are connected.
3. Non-inverting input (no input resistor) – only 5 is connected.
4. Inverting input (input resistor to V_{SS}) – 2, 6, 7, and 9 are connected.
5. Non-inverting input (input resistor to V_{DD}) – 2, 7, 8, and 10 are connected.
6. If inputs and outputs are mixed on the same port, the pins used as the outputs must have the internal resistor connected to either V_{DD} or V_{SS} (8 and 9 or 8 and 10 must be connected). This is necessary for testing purposes. For example, if there are two inverting inputs (with no input resistor) and two non-inverting outputs, the connection would be made as follows:

   Inputs – 2 and 6 are connected
   Outputs – 1, 3, 8, and 9 are connected or
   1, 3, 8, and 10 are connected

   If the pins on a port are all inputs or all outputs, the internal resistors do not have to be connected.

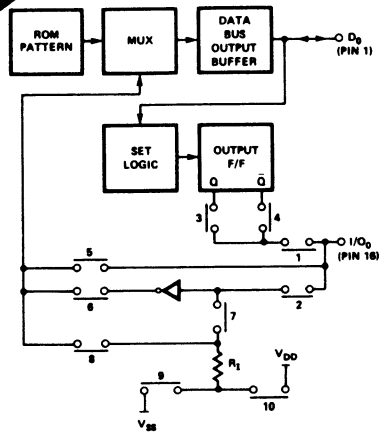
C. 4001 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. Based on the particular customer pattern, the characters should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

Note that:

NOP = BPPPP PPPPF = 0000 0000

4001 I/O Options

SAMPLE

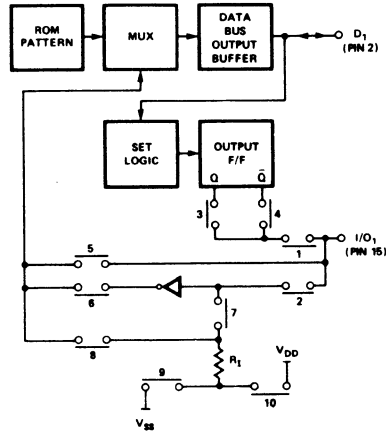


I/O_0 (PIN 16)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

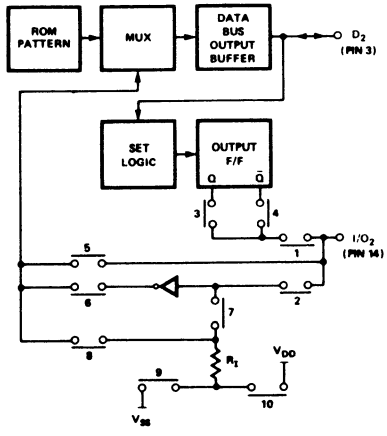


I/O_1 (PIN 15)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

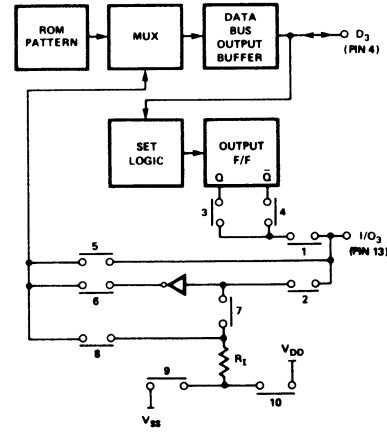


I/O_2 (PIN 14)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).



I/O_3 (PIN 13)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

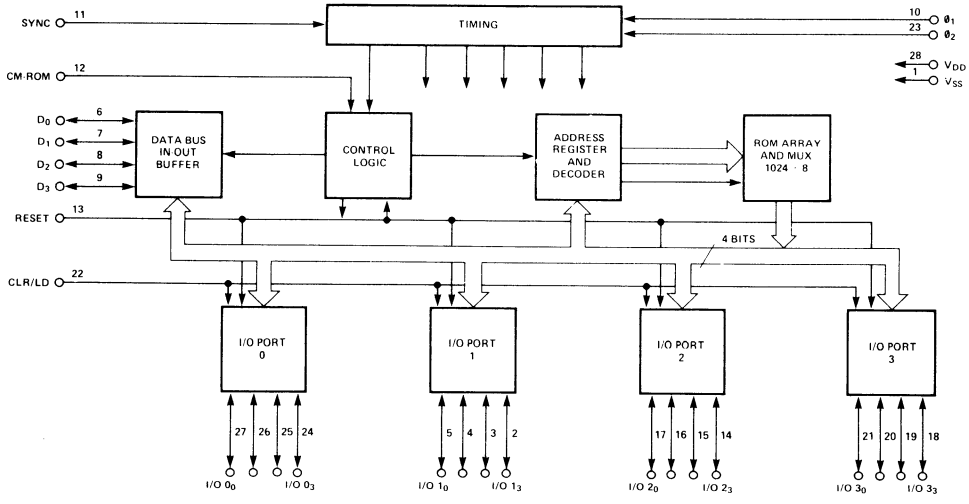
b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

4308
1024 x 8 MASK PROGRAMMABLE ROM AND FOUR 4-BIT I/O PORTS

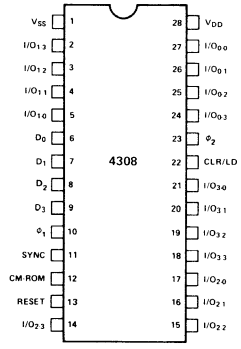
- **Direct Interface to MCS-40™ 4-Bit Data Bus**
- **Equivalent to Four 4001 ROMs**
- **Four Independent 4-Bit I/O Ports**
- **Input I/O Buffer Storage with an Optional Strobe**
- **I/O Ports Low-Power TTL Compatible**
- **28 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4308 is a 1024 x 8 bit word ROM memory with four I/O ports. It is designed for the MCS-40™ system and is operationally compatible with all existing MCS-40 elements. The 4308 is functionally identical to four 4001 chips. The 4308 has 16 I/O lines arranged in four groups of four lines.

BLOCK DIAGRAM



PIN CONFIGURATION



Pin Description

Pin No.	Designation/ Type of Logic	Description of Function
1	V_{SS}	Most positive supply voltage.
2-5 14-17 18-21 24-27	$I/O1_3$-$I/O1_0$/Neg. $I/O2_3$-$I/O2_0$/Neg. $I/O3_3$-$I/O3_0$/Neg. $I/O0_3$-$I/O0_0$/Neg.	Four I/O ports consisting of 4 bidirectional and selectable lines.
6-9	D_0-D_3/Neg.	Bi-directional data bus. All information between processor and device is transmitted to these four pins.
10, 23	$\phi1$, $\phi2$/Neg.	Non-overlapped clock signals which determine device timing.
11	SYNC/Neg.	System synchronization signal generated by processor.
12	CM-ROM/Neg.	Chip enable generated by the processor.
13	RESET/Neg.	Reset input. A negative level (V_{DD}) on this pin will clear internal flip-flops and buffers. The input buffers are not cleared by this signal.
22	CLR/LD/Neg.	Clear/Load input. This pin is a dual function pin. It may be selected as a common Clear for those pins selected as output pins or as a Load for those pins selected as input pins. This pin should be designated for one purpose only per 4308, either Clear or Load. As a Load, a positive (V_{SS}) to negative (V_{DD}) transition will cause the I/O data to be placed in the input latch. A negative to positive transition will cause the data to be latched. The I/O pin state may be altered without changing the contents of the latch when the line is positive. As a Clear, a negative level (V_{DD}) on this line will cause the designated output latches to clear and remain cleared until a positive level (V_{SS}) is placed on the line. This line may be driven by a TTL output with a 1K pull-up resistor to V_{SS}.
28	V_{DD}	Main supply voltage. Value must be V_{SS} -15V ±5%.

Functional Description

The 4308 ROM program memory is arrayed 1024 x 8 bit words. For the program memory mode of operation, the A1 –A3 time periods of the instruction cycle are used to address the ROM contents. The 4308 decodes the first ten bits of the address to select 1 out of the 1024 words, 8 bits wide. The remaining two bits select a particular 4308, which has one of four possible metal option chip select addresses. Instruction information is available in two 4-bit segments during M_1 and M_2 time periods. A 4004 system can accommodate up to four 4308's while a 4040 system can utilize up to eight devices.

A second mode of operation of the ROM is as an Input/Output control device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O external lines. Each chip has the capability to identify itself for an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and execute the instruction.

All internal flip flops (including the output register) will be reset when the RESET line goes low (negative voltage).

Each of the four I/O ports of a 4308 are program selectable. Each of the four lines can be specified as either inputs or outputs via a metal mask option. A complete description of the I/O option capabilities are given below. The 4308 has an input storage buffer for utilization with those I/O pins designated as inputs. A common strobe line (CLR/LD line) allows the loading of data from the I/O lines. The same CLR/LD strobe line can also serve as a clear to the I/O output port buffers when designated. This CLR/LD line is common to all ports on a 4308 and when toggled, will effect those I/O lines connected by the metal mask option. For an input line, if the CLR/LD strobe line is left unconnected, of if it is pulled to (V_{DD}), then the output fo the buffer will follow the input.

NOTE: Since the 4308 is compatible with all components of the MCS-40 system, 4308 and 4001 can be mixed on one memory bank as long as the chip select addresses are mutually exclusive.

The following table shows the chip number relationship between 4308 and 4001.

4308		4001	
Page No.	Chip No.	Page No.	Chip No.
0-3	(0)	0-15	0-15
4-7	(1)		
8-11	(2)		
12-15	(3)		

INSTRUCTION EXECUTION

The 4308 responds to the following instructions.

1. **SRC Instruction** (Send address to ROM and RAM)

   When the CPU executes an SRC instruction it will send out 8 bits of data during X_2 and X_3 and will activate the CM-ROM and one CM-RAM line at X_2. Data at X_2 (representing the contents of the first register of the register pair addressed by the SRC instruction), with simultaneous presence of CM-ROM, is interpreted by the 4308 as the chip number of the unit that should later perform an I/O operation. Data at X_3 is ignored. After an SRC only one CM-ROM and CM-RAM device will be selected.

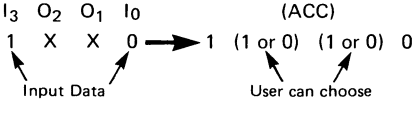
2. **WRR – Write ROM Port**

   The content of the accumulator is transferred to the ROM output port of the previously selected ROM chip. The data is available on the output pins until a new WRR is executed to the same port. The ACC content and carry/link are unaffected. The LSB bit of the accumulator appears on I/O_0.) No operation is performed on I/O lines coded as inputs.

3. **RDR – Read ROM Port**

   The data present at the input lines of the previously selected ROM chip is transferred to the accumulator.

   If the I/O option has both inputs and outputs within the same 4 I/O lines, the user can choose to have either "0" or "1" transferred to the accumulator for those I/O pins coded as outputs, when an RDR instruction is executed. For example, given a port with the I/O lines coded with 2 inputs and 2 outputs, when RDR is executed the transfer is as shown below:



Timing Considerations

At the beginning of each instruction sequence, a SYNC pulse is generated externally to synchronize the processor with the various components of the system. This pulse, along with the clock inputs ϕ_1 and ϕ_2, is used in the 4308 as an input to a timing register.

During time A_1, A_2, and A_3, the address is sequentially accepted from the data bus and decoded. During time A_3, the CM-ROM line will be active, and if the 2 highest order bits of the address sent at A_3 match the metal preprogrammed chip select option, the ROM will respond to the current address.

At time M_1 and M_2, the instruction OPR, OPA will be placed on the data bus for the processor.

After the SRC or Send Register Control instruction, which is used to designate a set of 4 I/O lines (1 port) on a particular ROM which are to be used for subsequent ROM I/O operations, is executed by the processor, the processor sends a 4 bit code to the ROM during X_2, and CM-ROM goes to a "1" (V_{DD}). The first two bits (D_3, D_2) of this code select a group of 1 out of 4 possible 4308, and the last two bits select a particular port (1 of 4 ports). This port remains selected until the next SRC instruction is executed.

In both the RDR and WRR operations, the CM-ROM line will become active during time M_2, and if the ROM has a previously selected I/O port, it will respond to the I/O in two ways. For a WRR accumulator, data will be transferred to an internal ROM selected output port flip-flops during X_2. Data will be available on the I/O line from time $X_3 \cdot \overline{\phi_2}$. The data will remain on the bus until a new WRR occurs, a reset occurs, or a clear (CLR/LD line) is generated. The RDR instruction will transfer information from the input port flip-flops of a previously selected port. Prior to RDR instruction, the user should insure that the input flip-flops have been loaded via the CLR/LD strobe if the load strobe is specified. If the load strobe is not specified, information on the input lines will be loaded into the accumulator at the time of the RDR.

I/O OPTIONS

The 4308 offers the following options on its I/O pins:

1. Input or output.
2. Inverted or direct (for input and output).
3. On-chip resistor connected to either V_{SS} or V_{DD} for input pins.
4. Loading of input buffers via the CLR/LD signal.
5. Clear signal for any or all output ports via the CLR/LD signal.

Referring to the block diagram of the single I/O pin shown below which illustrates the various options available on a 4308, it should be noted that certain pin combinations are mutually exclusive and should not be specified together. There are also certain invalid combinations. The following combinations should be avoided:

8,9
5,6
3,4
10,11 – Both on a single pin and within a single 4308.

Examples of some common desired option/connections are:

a. *I/O pin inputs**

non-inverting	11, 2, 5, 7, 9 (TTL) – 2, 5, 7, 8
inverting	11, 2, 6, 7, 9 (TTL) – 2, 6, 7, 8

b. *I/O pin outputs*

non-inverting	3, 1 (10 optional)
inverting	4, 1 (10 optional)

Other combinations exist and should be used with caution.

**Option 11 need not be specified if an unbuffered input is desired. This is equivalent to a 4001 input.*

NOTE: The 4308 has the following enhancements over the 4001 as far as I/O options are concerned:

1. The capability of clearing any or all outputs with the CLR/LD signal.
2. TTL compatibility of both the inverting and non-inverting input paths for input ports.
3. The capability to select the LD option and have the input buffer become an input flip-flop and to have the CLR/LD signal become a clock for loading data.

For TTL compatibility on the I/O lines, the supply voltage should be V_{DD} = -10V ±5%, V_{SS} = +5V ±5%. External pull-up is required for outputs.

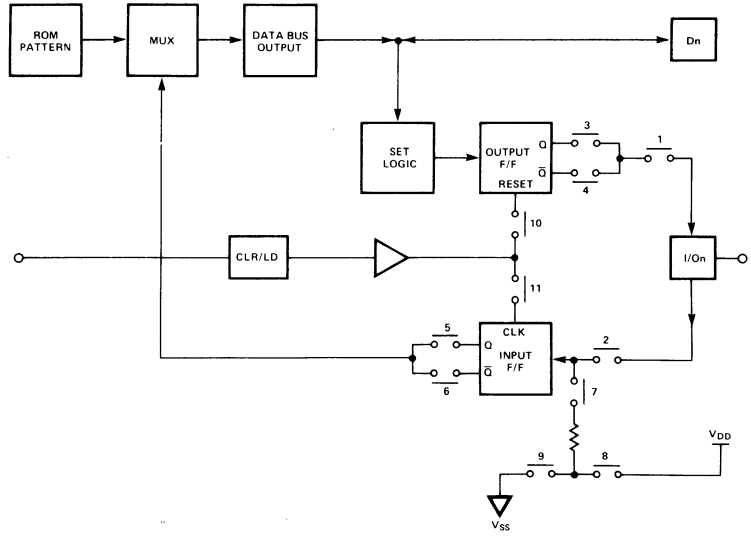


Figure 1. 4308 I/O Pin Options.

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		20	40	mA	T_A = 25°C
INPUT CHARACTERISTICS – ALL INPUTS EXCEPT I/O PINS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	CLR/LD pin
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS – ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		200	300	Ω	V_{OUT} = V_{SS} -.5V
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IH}	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
V_{IL}	CLR/LD Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
R_I	Input Resistance, if Used	10	18	35	kΩ	R_I tied to V_{SS}; V_{IN} = V_{SS} -3V
R_I[1]	Input Resistance, if Used	15	25	40	kΩ	R_I tied to V_{DD}; V_{IN} = V_{SS} -3V
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance		1.2	2	kΩ	V_{OUT} = V_{SS} -.5V
I_{OL}	I/O Output "1" Sink Current	2.5	5		mA	V_{OUT} = V_{SS} -.5V
I_{OL}[2]	I/O Output "1" Sink Current	0.8	3		mA	V_{OUT} = V_{SS} -4.85V
I_{CF}	I/O Output "1" Clamp Current			4	mA	V_{OUT} = V_{SS} -6V; T_A = 70°C
V_{OL}	I/O Output Low Voltage	V_{SS}-12		V_{SS}-6.5	V	I_{OUT} = 50μA

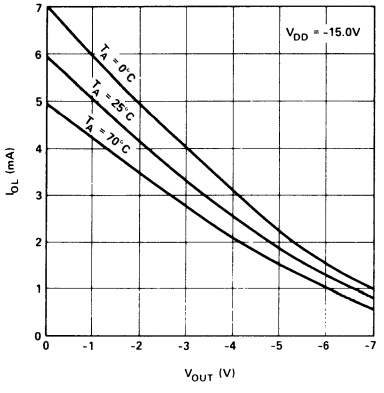
Notes: 1. R_I is large signal equivalent resistance to (V_{SS} -12) V.
2. For TTL compatability, use 12kΩ external resistor to V_{DD}.

D.C. and Operating Characteristics

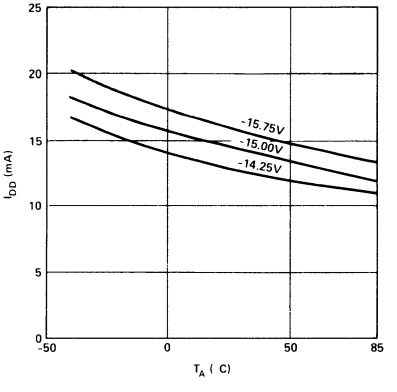
CAPACITANCE

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
C_ϕ	Clock Capacitance		14	20	pF	$V_{IN} = V_{SS}$
C_{DB}	Data Bus Capacitance		7	10	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance			10	pF	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance			10	pF	$V_{IN} = V_{SS}$

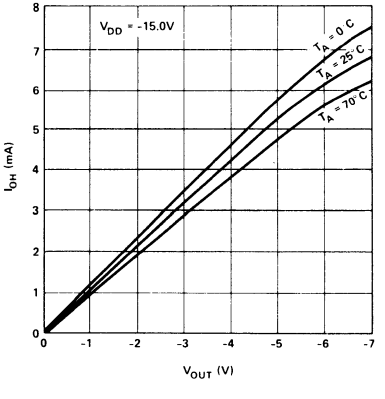
4308 OUTPUT PINS ("1" LEVEL)



4308 SUPPLY CURRENT VS. TEMPERATURE



4308 OUTPUT PINS ("0" LEVEL)



A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{SS} - V_{DD} = 15V \pm 5\%$

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Time			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines[4]
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{IS}	I/O Input Set-Time	50			ns	
t_{IH}	I/O Input Hold-Time	100			ns	
$t_{PW\ I/O}$	C/L Pulse-Width	1000	400		ns	
$t_{W\ C/L}$	C/L Write Time	350	200		ns	
$t_{H\ C/L}$	C/L Hold Time	100			ns	
t_D	I/O Output Delay			1500	ns	C_{OUT} = 100pF
t_C[5]	I/O Output Delay on C/L		750	1500	ns	C_{OUT} = 100pF
$t_{W\ \phi 2F}$[6]	Data In Write Time with Respect to ϕ_2	-30	-60		ns	

Notes:
1. t_H measured with $t_{\phi R}$ = 10nsec.
2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. t_{ACC}, 4308 is guaranteed with $t_{\phi D2}$ = 200 nsec.
5. C/L Clears output buffer when low. C/L enters data into input buffer when low. C/L rising edge latches input buffer. Port Option 10 and 11 are mutually exclusive on any 4308.
6. Data Bus Inputs are guaranteed valid before ϕ_2 falling edge by 4004, 4040 t_{ACC}. If $t_{PW\phi 2}$ is widened, then t_{CY} is increased and Data Bus Inputs remain valid before ϕ_2 falling edge. Thus, $t_{W\phi 2F}$ is not a system constraint.

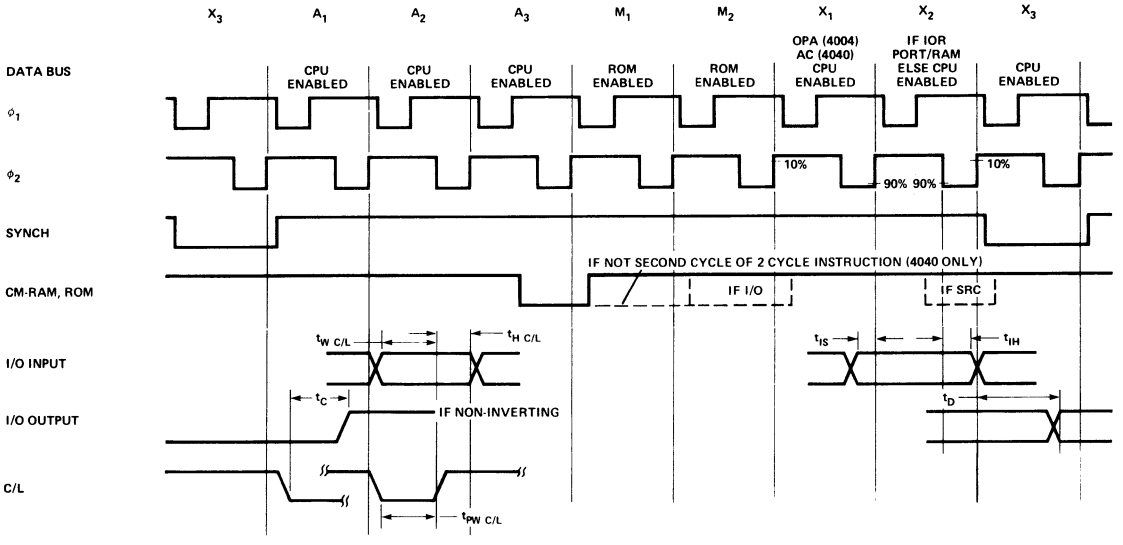


Figure 2. Timing Diagram.

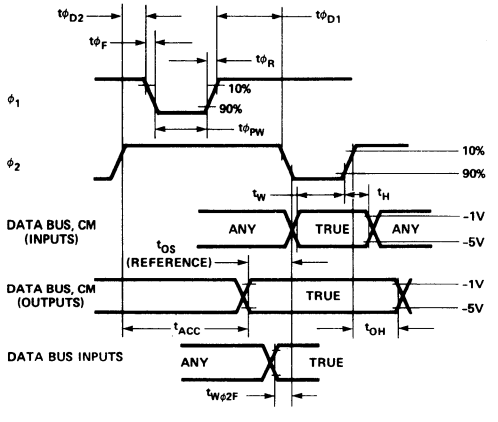


Figure 3. Timing Detail.

Programming Instruction

To insure optimum handling of ROM programs and avoid delays, programs should be specified in the following format.

Paper Tape Format*

A 1" wide paper tape using 8 bit ASCII code, such as a model 33ASR teletype produces:

A. Preamble

1. Preceding the first word field and following the last word field, there should be a leader/trailer length of at least 25 characters. This should consist of rubout punches.
2. Included in the tape before the leader, and preceded by another leader, should be the customer's complete telex or twx number and if more than one pattern is being transmitted, the ROM pattern number.
3. The first ROM pattern preamble field is the device type number or ROM number. The field should be framed by an "I" and "–"

   I4308 –

   This should be followed by the chip select information encoded in decimal (two digits), and enclosed by "C" and "S", as in

   "ChhS"

   The valid select digits for the 4308 are 0–3

   "C0S" – "C3S"

   Finally, the I/O options would be specified on a port-by-port basis with the connections to be made separated by commas, and enclosed in parentheses:

   "(n1, n2, n3 . . .)".

   where (n1, n2 . . .) are the option numbers associated with one I/O line. Hence, for the 4308 there will be sixteen bracketed collections of I/O options.

   Each I/O pin has a series of 11 possible connections. These connections are consecutively numbered from 1-11. It is these numbers that should be in parentheses for each I/O pin.

   Example: "( )" indicates no connection
   "(1)" indicates only #1
   "(2,5,7)" indicates connections #2, 5 and 7.

   I/O options should be placed on the tape sequentially for the 4308, from $I/O0_0$ – $I/O3_3$(16). Always avoid illegal combinations.

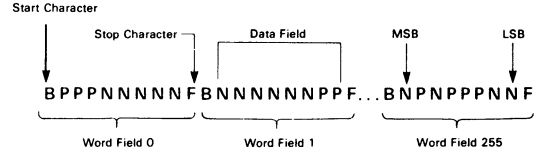
NOTE: Cards may also be submitted.

B. ROM Code

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F. Within the word field, a P results in a high level output (V_{SS} or logic 0 for MCS-40 CPUs) and a N results in a low level output (V_{DD} or logic 1 for MCS-40 CPUs).

   Example of 256 x 8 format (N=256):



3. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. It may be helpful to insert the word number (as a comment) at least every four word fields.
4. Within the ROM pattern words a character, "X", may be used. Where "P" and "N" indicate a "0" and "1" setting respectively, an "X" will indicate a single bit – "Don't Care" setting. This allows the optimum default bit values to be selected by Intel. The bit value will be fixed to allow for testing. The values will be specified to the user on the Verification Listing tape.

   In the place of a standard BPNF word, a "B*nF" word may be used. This indicates that the data in the last BPNF word encountered is to be repeated for the next n words ($1 \leq n \leq 1023$). Note that if a repeat count of 4 is given in word position 10, then words 10, 11, 12, and 13 will be repeats of word 9 (except for Don't Care bits which might conceivably have different assigned values).

   To indicate that an entire block (such as the remainder of a ROM) is not used (i.e., Don't Care), a word of Don't Care data can be followed by the remaining word count in a repeat count form.

CUSTOM ROM ORDER FORM

ROM

CUSTOMER _____

P.O. NUMBER _____

DATE _____

For Intel use only

S# _____ PPPP _____

STD _____ ZZ _____

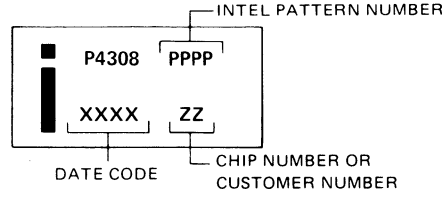
_____ DD _____

APP _____ DATE _____

All custom 4308 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4308), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).



CUSTOMER NUMBER _____

MCS A/40

MASK OPTION SPECIFICATION

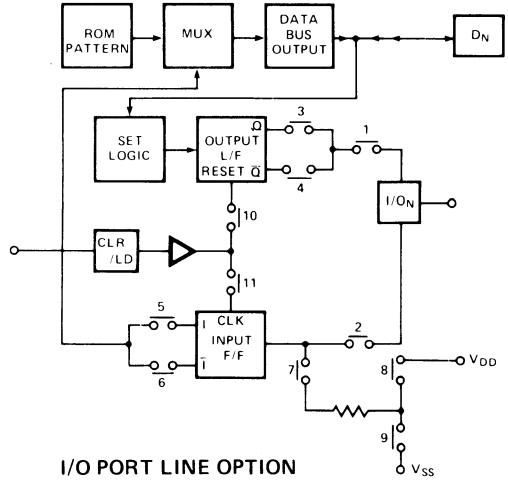
A. CHIP NUMBER _____ (Must be specified).

B. I/O OPTION – Specify the connection numbers for each I/O pin. See table below.

C. 4308 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. Based on the particular customer pattern, the characters should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

Note that: NOP = BPPPP PPPPF = 0000 0000

PIN		OPTION										
I/O 0_0	27	1	2	3	4	5	6	7	8	9	10	11
I/O 0_1	26	1	2	3	4	5	6	7	8	9	10	11
I/O 0_2	25	1	2	3	4	5	6	7	8	9	10	11
I/O 0_3	24	1	2	3	4	5	6	7	8	9	10	11
I/O 1_0	5	1	2	3	4	5	6	7	8	9	10	11
I/O 1_1	4	1	2	3	4	5	6	7	8	9	10	11
I/O 1_2	3	1	2	3	4	5	6	7	8	9	10	11
I/O 1_3	2	1	2	3	4	5	6	7	8	9	10	11
I/O 2_0	17	1	2	3	4	5	6	7	8	9	10	11
I/O 2_1	16	1	2	3	4	5	6	7	8	9	10	11
I/O 2_2	15	1	2	3	4	5	6	7	8	9	10	11
I/O 2_3	14	1	2	3	4	5	6	7	8	9	10	11
I/O 3_0	21	1	2	3	4	5	6	7	8	9	10	11
I/O 3_1	20	1	2	3	4	5	6	7	8	9	10	11
I/O 3_2	19	1	2	3	4	5	6	7	8	9	10	11
I/O 3_3	18	1	2	3	4	5	6	7	8	9	10	11



I/O PORT LINE OPTION

NOTE: Options 10 and 11 cannot both be specified.

4316A
16,384 BIT STATIC MOS READ ONLY MEMORY

Organization: 2048 Words x 8 Bits
Access Time: 850 ns Max.

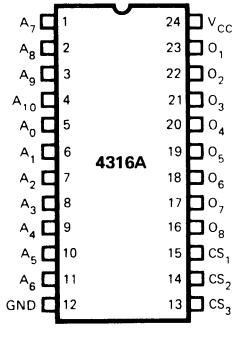
- **Single +5 Volts Power Supply Voltage**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Low Power Dissipation of 31.4 μW/Bit Maximum**
- **Three-State Output — OR-Tie Capability**
- **Fully Decoded — On Chip Address Decode**
- **Interface to 4004/4040 CPU Via 4008/4009 or 4289 Standard Memory Interface**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available with -40° to +85°C Operating Range**

The Intel® 4316A is a 16,384-bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for microcomputer memory applications where high performance, large bit storage, and simple interfacing are important design objectives. It can be used in MCS-40™ systems via the 4008/4009 or 4289 Standard Memory Interface components.

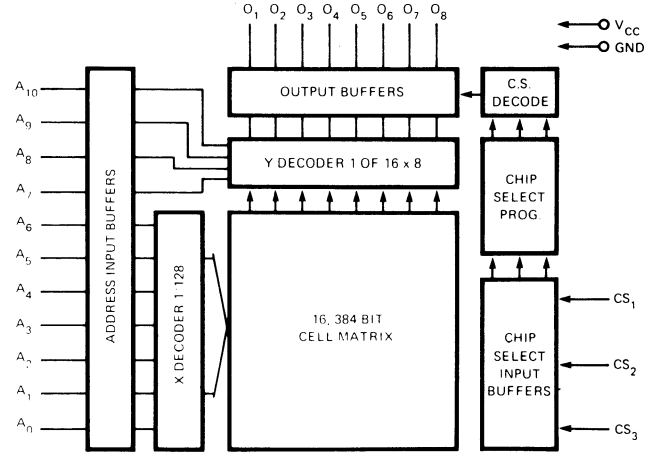
The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and the desired chip select code is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitate easy memory expansion.

The 4316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
CS_1-CS_3	PROGRAMMABLE CHIP SELECT INPUTS

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect
To Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1.0 Watt

***COMMENT:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)			10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	µA	CS = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			-20	µA	CS = 2.2V, V_{OUT} = 0.45V
I_{CC}	Power Supply Current		40	98	mA	All inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}+1.0V	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -100 µA

(1) Typical values for T_A = 25°C and nominal supply voltage.

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_A	Address to Output Delay Time		400	850	nS
t_{CO}	Chip Select to Output Enable Delay Time			300	nS
t_{DF}	Chip Deselect to Output Data Float Delay Time	0		300	nS

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

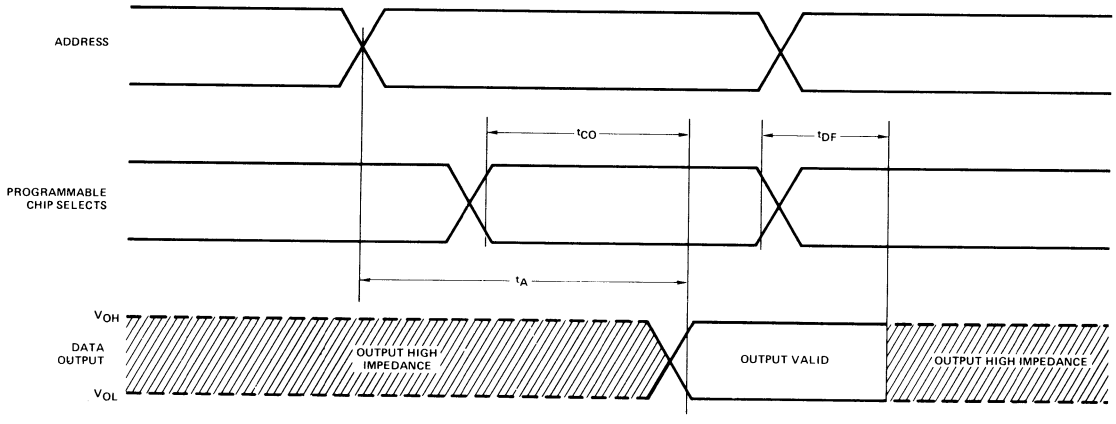
Output Load . . . 1 TTL Gate, and C_{LOAD} = 100 pF
Input Pulse Levels . . . . . 0.8 to 2.0V
Input Pulse Rise and Fall Times . (10% to 90%) 20 nS
Timing Measurement Reference Level
Input 1.5V
Output . . . . . 0.45V to 2.2V

Capacitance(2) T_A = 25°C, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	4 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	8 pF	15 pF

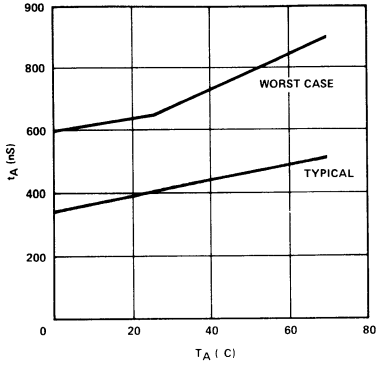
(2) This parameter is periodically sampled and is not 100% tested.

Waveforms

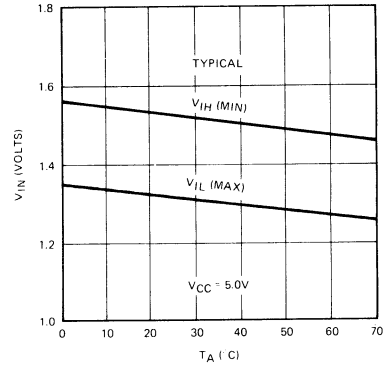

ADDRESS
PROGRAMMABLE CHIP SELECTS
DATA OUTPUT
V_{OH}
V_{OL}
t_{CO}
t_{DF}
t_A
OUTPUT HIGH IMPEDANCE
OUTPUT VALID
OUTPUT HIGH IMPEDANCE

Typical D.C. Characteristics

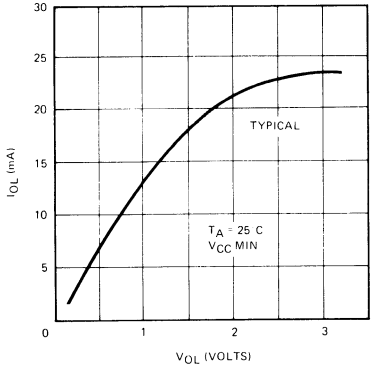
ACCESS TIME VS. AMBIENT TEMPERATURE



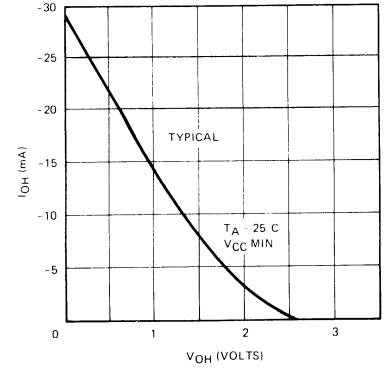
V_{IN} LIMITS VS. TEMPERATURE



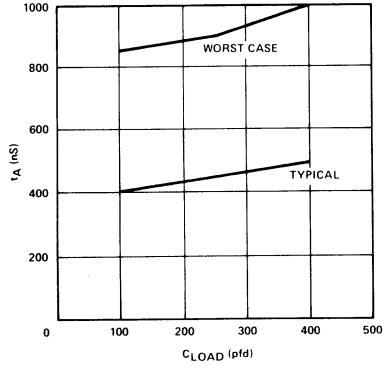
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



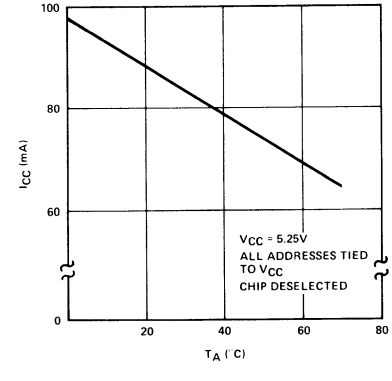
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. LOAD CAPACITANCE



STATIC I_{CC} VS. AMBIENT TEMPERATURE WORST CASE



4702A
REPROGRAMMABLE 2K PROM

- **Access Time: 1.7 usec Max.**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **Ultraviolet Erasable and Electronically Reprogrammable**
- **Fully Decoded, 256 x 8 Organization**
- **Static MOS: No Clocks Required**
- **Inputs and Outputs TTL Compatible**
- **Three-State Output: OR-Tie Capability**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available with -40° to +85° C Operating Range**

The 4702A is a 256 word by 8 bit electrically programmable ROM ideally suited for microcomputer system development where fast turn-around and pattern experimentation are important. The 4702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

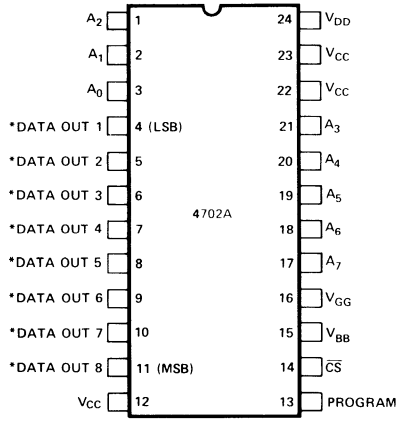
The 4702A is packaged in a 24 pin dual-in-line package with a transparent quartz lid. The transparent quartz lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. This procedure can be repeated as many times as required.

The circuitry of the 4702A is entirely static; no clocks are required.

A pin-for pin metal mask programmed ROM, the Intel® 1302A, is ideal for large volume production runs of systems initially using the 4702A.

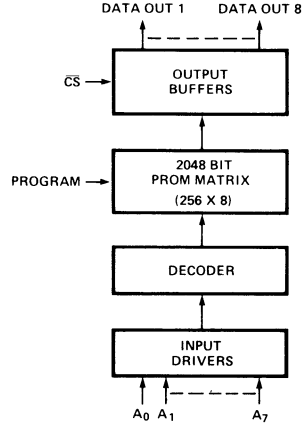
The 4702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD DUPING PROGRAMMING.

BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
DO_1- DO_2	DATA OUTPUTS

Pin Connections

The external lead connections to the **4702A** differ, depending on whether the device is being programmed[1] or used in read mode. (See following table.)

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = -10V±5%, V_{GG} = -10V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP.[2]	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			10	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DD1}	Power Supply Current		39	54	mA	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		36	50	mA	$\overline{CS}$ = 0.0, I_{OL} = 0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		43	63	mA	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0mA, T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = 1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
I_{GG}	Gate Supply Current			10	μA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC} −2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
V_{OL}	Output Low Voltage		.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5			V	I_{OH} = −100 μA

Continuous Operation

Note 1: In the programming mode, the data inputs 1−8 are pins 4−11 respectively. $\overline{CS}$ = GND.
Note 2: Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0° C to +70°C, V_{CC} = +5V ±5%, V_{DD} = -10V ±5%, V_{GG} = -10V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay			1.7	μs
t_{CS}	Chip select delay			800	ns
t_{CO}	Output delay from $\overline{CS}$			900	ns
t_{OD}	Output deselect			300	ns

Capacitance* T_A = 25°C

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance		8	15	pF	$V_{IN}=V_{CC}$, $CS=V_{CC}$, $V_{OUT}=V_{CC}$, $V_{GG}=V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		10	15	pF	

*This parameter is periodically sampled and is not 100% tested.

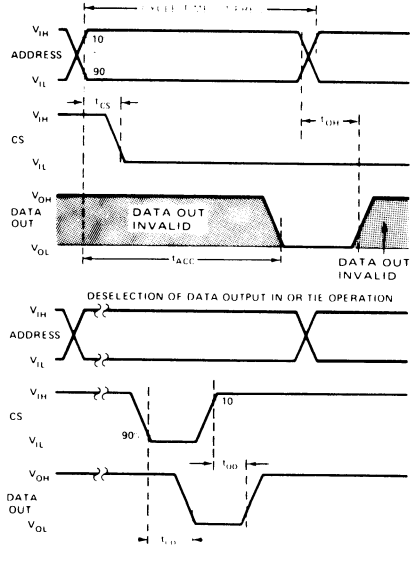
Switching Characteristics

Conditions of Test:

Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns.

a) For output load = 1 TTL gate; measurements made at output of TTL gate (t_{PD} ≤15 ns)

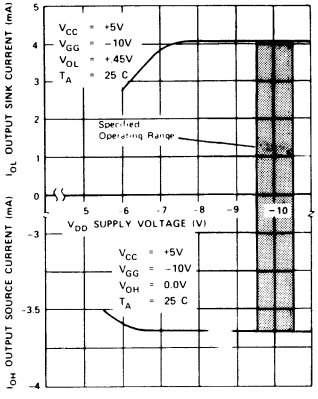
b) For pure capacitive load of 75pf.



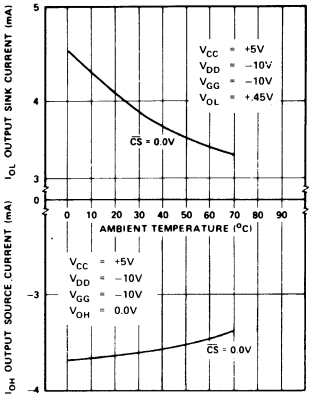
MCS 4/40

Typical Characteristics

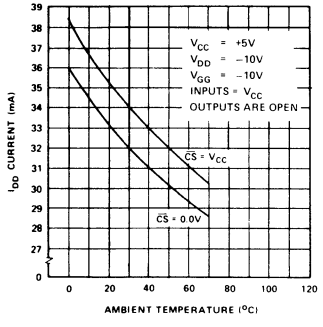
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



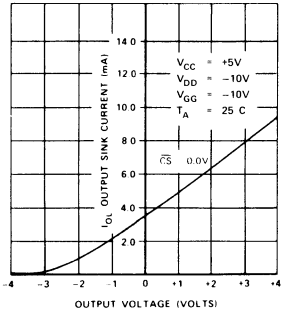
OUTPUT CURRENT VS. TEMPERATURE



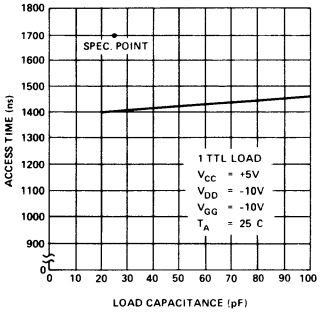
I_{DD} CURRENT VS. TEMPERATURE



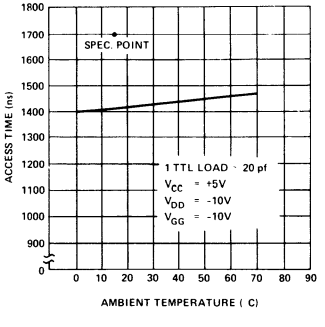
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE



MCS 4/40

PROGRAMMING OPERATION

D.C. and Operating Characteristics for Programming Operation

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = +12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI1P}	Address and Data Input Load Current			10	mA	$V_{IN} = -48V$
I_{LI2P}	Program and V_{GG} Load Current			10	mA	$V_{IN} = -48V$
I_{BB}	V_{BB} Supply Load Current		.05		mA	
I_{DDP}(1)	Peak I_{DD} Supply Load Current		200		mA	$V_{DD} = V_{prog} = -48V$ $V_{GG} = -35V$
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	−46		−48	V	
V_{IL2P}	Address Input Low Voltage	−40		−48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	−46		−48	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	−35		−40	V	

Note 1: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μsec. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.

A.C. Characteristics for Programming Operation

$T_{AMBIENT} = 25°C$, $V_{CC} = 0V$, $V_{BB} = +12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Duty Cycle (V_{DD}, V_{GG})			20	%	
$t_{\phi PW}$	Program Pulse Width			3	ms	$V_{GG} = -35V$, $V_{DD} = V_{prog} = -48V$
t_{DW}	Data Set Up Time	25			μs	
t_{DH}	Data Hold Time	10			μs	
t_{VW}	V_{DD}, V_{GG} Set Up	100			μs	
t_{VD}	V_{DD}, V_{GG} Hold	10		100	μs	
t_{ACW} (2)	Address Complement Set Up	25			μs	
t_{ACH} (2)	Address Complement Hold	25			μs	
t_{ATW}	Address True Set Up	10			μs	
t_{ATH}	Address True Hold	10			μs	

Note 2. All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0 through 255) must be programmed as shown in the timing diagram for a minimum of 32 times.

Switching Characteristics for Programming Operation

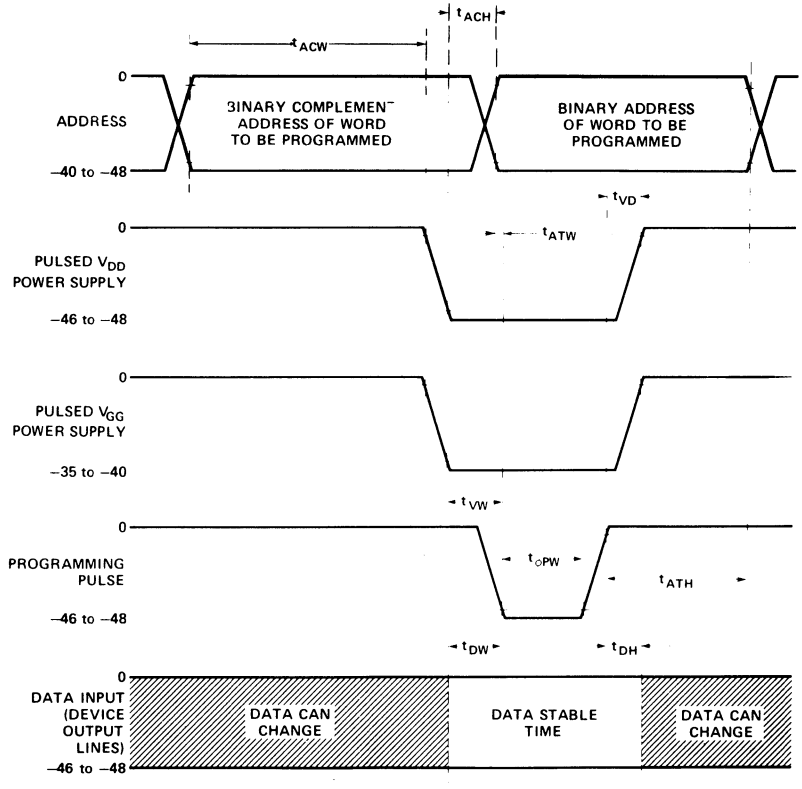
PROGRAM OPERATION

Conditions of Test:

Input pulse rise and fall times $\leq 1\mu$sec

$\overline{CS}$ = 0V

PROGRAM WAVEFORMS



Programming Operation

When the Data Input for the Program Mode is:	Then the Data Output during the Read Mode is:
V_{ILIP} = ~–48V pulsed	Logic 1 = V_{OH} = 'P' on tape
V_{IHP} = ~ 0V	Logic 0 = V_{OL} = 'N' on tape

	ADDRESS							
WORD	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|
255	1	1	1	1	1	1	1	1

Address Logic Level During Read Mode: Logic 0 = V_{IL} (~.3V) Logic 1 = V_{IH} (~3V)

Address Logic Level During Program Mode: Logic 0 = V_{IL2P} (~–40V) Logic 1 = V_{IHP} (~0V)

MCS-40™ Program Memory In 4702A PROMs

Memory address, memory data, I/O bus, and chip select lines from 4289 or a 4008/4009 are defined with respect to positive logic. The MCS-40™ data and control lines from the CPU are defined with respect to negative logic. As a result, in 4702A program memory used with the 4289 or 4009, programs should be coded with logic "1" = high level and logic "0" = low level (i.e., NOP = 0000 0000 = NNNN NNNN).

For 4702A PROM programs which are to be converted to 4001 or 4308 ROM memory, a preferred method is to use negative logic program memory in the 4702A and place inverting buffers at the data inputs of the 4289 or 4008/4009. This allows program code to be consistent with that of the 4001 and 4308 mask programmed ROMs and assures that 4289 or 4008/4009 input capacitance will not limit system speed when using several 4702A PROMs for program storage. (Note that programs are defined for the 4001/4308 ROMs in terms of negative logic such that NOP = 0000 0000 = PPPP PPPP.)

Programming Operation

I. Operation of the 4702A in Program Mode

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table on page 6 for logic levels). All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25 μsec after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10 μsec before the program pulse is applied. The addresses should be programmed in the sequence 0 through 255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (-48V) will program a "1" and a high data input level (ground) will leave a "0" (see table on page 6). All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals.

II. Programming of the 4702A Using Intel Microcomputers

Intel provides low cost program development systems which may be used to program its electrically programmable ROMs. Note that the programming specifications that apply to the 4702A are identical to those for Intel's 1702A.

A. Intellec® 4

The Intellec® 4 program development system is used as a program development tool for the 4004 and 4040 microprocessors. As such, it is equipped with a PROM programmer card and may be used to program Intel's electrically programmable and ultraviolet erasable ROMs.

An ASR-33 teletype terminal is used as the input device. Through use of the Intellec software system monitor, programs to be loaded into PROM may be typed in directly or loaded through the paper tape reader. The system monitor allows the program to be reviewed or altered at will prior to actually programming the PROM. For more complete information on this program development system, refer to the Intel Microcomputer Catalog or the Intellec Specifications.

B. Intellec® MDS

An Intellec® MDS system can also be used with a Universal PROM Programmer (UPP) to program 4702A PROMs. The 1702A/4702A personality card must be plugged into the appropriate PROM programmer card socket of the UPP for this programming operation.

III. 4702A Erasing Procedure

The 4702A may be erased by exposure to high intensity short-wave ultraviolet light. See the EPROM programming section, page 3-55, for details.

4801
CLOCK GENERATOR CRYSTAL

FUNDAMENTAL — TYPE 5.185 MHz
FOR 4004/4201A or 4040/4201A CPU SET

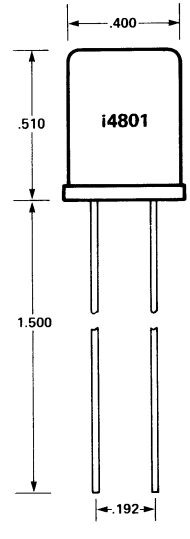
- "AT" Cut Fundamental Frequency
- Room Temperature Frequency Adjusted Within ±.005%
- Used With 4201A in MCS-40™ System
- Temperature Range -55°C to 125°C

The 4801 is a quartz crystal resonator to be used with a 4201A in an MCS-40 microcomputer system. The selection of 5.185 MHz gives a 1.35μs clock period (740 KHz) for a 4004 or 4040 at the ϕ_1 and ϕ_2 outputs.

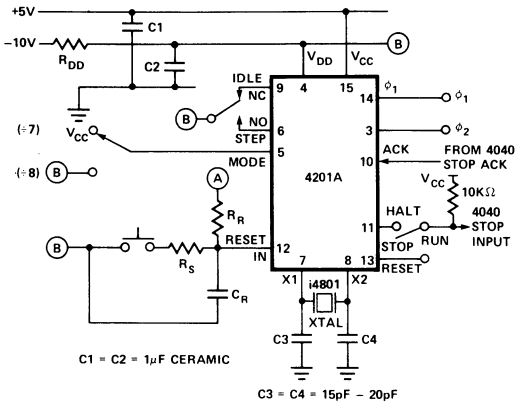
ELECTRICAL CHARACTERISTICS

Recommended Drive Level	10mW
Type of Resonance	Serial
Appr. Equivalent Series Resistance	35 ohms
Maximum Shunt Capacity	7pF
Maximum Frequency Deviation	
0°C to 70°C	±.005%
-55°C to 125°C	±.02%

PACKAGING INFORMATION



CLOCK GENERATOR IMPLEMENTATION



DESIGN CONSIDERATIONS

CRYSTALS

Either ÷7 or ÷8 Modes may be used. Mode equals V_{CC} for ÷7, Mode equals V_{DD} for ÷8. The clock frequency range should be between 500 kHz (4 MHz XTAL, ÷8 MODE) and 740 kHz (5.185 MHz XTAL, ÷7 MODE).

X1 AND X2 INPUT CAPACITANCE

The XTAL terminals, X1 and X2, should be tied to 15 pF - 20 pF capacitors C3 and C4 to AC system GND.

POWER SUPPLY VOLTAGE CONSIDERATIONS

1. Operation is guaranteed with V_{CC}-V_{DD} = 15V ± 5%. During system power-up or during power supply glitching, the maximum magnitude of (V_{CC}-V_{DD}) must be limited to 17 volts.

   During the power supply rise time (that is, when $|V_{CC}-V_{DD}| < 14.25$ volts), improper ϕ_1, and ϕ_2 output may occur until $|V_{CC}-V_{DD}|$ reaches the 14.25 minimum voltage.

2. With V_{CC} = +5V, V_{DD} = -10V, bypass capacitor C1 of 1 μF and C2 of 1 μF from V_{CC} to GND and V_{DD} to GND, respectively, should provide excellent bypassing. Bypass capacitors should be ceramic or equivalent quality to insure low inductance and low series resistance.

3. The purpose of the current limiting register R_{DD} is both to limit ϕ_1 and ϕ_2 rise times and to drop V_{DD} at the 4201A V_{DD} pin. Values for R_{DD} as a function of ϕ_1, ϕ_2 load capacitance are:
   For C_{LOAD} <50 pF; use R_{DD} = 100Ω.
   For 50 pF <C_{LOAD} <100 pF; use R_{DD} = 68Ω.
   For 100 pF <C_{LOAD} <300 pF; use R_{DD} = 27Ω.
   For C_{LOAD} >300 pF; use R_{DD} = 10Ω.

   All 4201A functions requiring the V_{DD} voltage should use the pin V_{DD} or node (B) on the 4201A side of resistor R_{DD}. Operation with the voltage drop across R_{DD} is guaranteed by Intel testing.

4. Single-Supply System (+15 V or -15)

   Recommended 4201A circuit modifications for single supply systems are:

   1. The 1 μF ceramic capacitor C1 should be between 4201A V_{DD} and V_{CC} pins.
   2. Other capacitors shown as being grounded should be connected to V_{CC}.
   3. Reset R_R is connected to V_{CC}. Reset C_R is connected to V_{DD} pin.
   4. The current limiting resistor R_{DD} is still needed in the V_{DD} line.

5. Power Supply Rise Times

   Intel testing is for power supply rise times between 5 ms and 300 ms. For power supply rise times less than 5 ms, a 200KΩ resistor from X1 to GND and C3 = C4 = 5 pF is recommended.

RESET NETWORK

The Reset input has V_{IL} = V_{CC}-11 volts and V_{IH} = V_{CC} -6.5 volts, with about 1 volt of hysteresis (Schmitt circuit).

Node (A) must be tied to GND or V_{CC} = +5 V; and R_R and C_R selected, such that the negative V_{DD} transition moves the Reset input below V_{IL}.

Tying node (A) to GND and making C_R very large, i.e. >1μF, will allow the greatest freedom in V_{CC} and V_{DD} rise times during turn-on. Tying node (A) to GND will also cause Reset after a V_{DD} glitch to GND.

The purpose of R_S at 510Ω or 1KΩ is to limit Reset input fall time on manual Reset, so that the Reset input does not fall below V_{DD}.

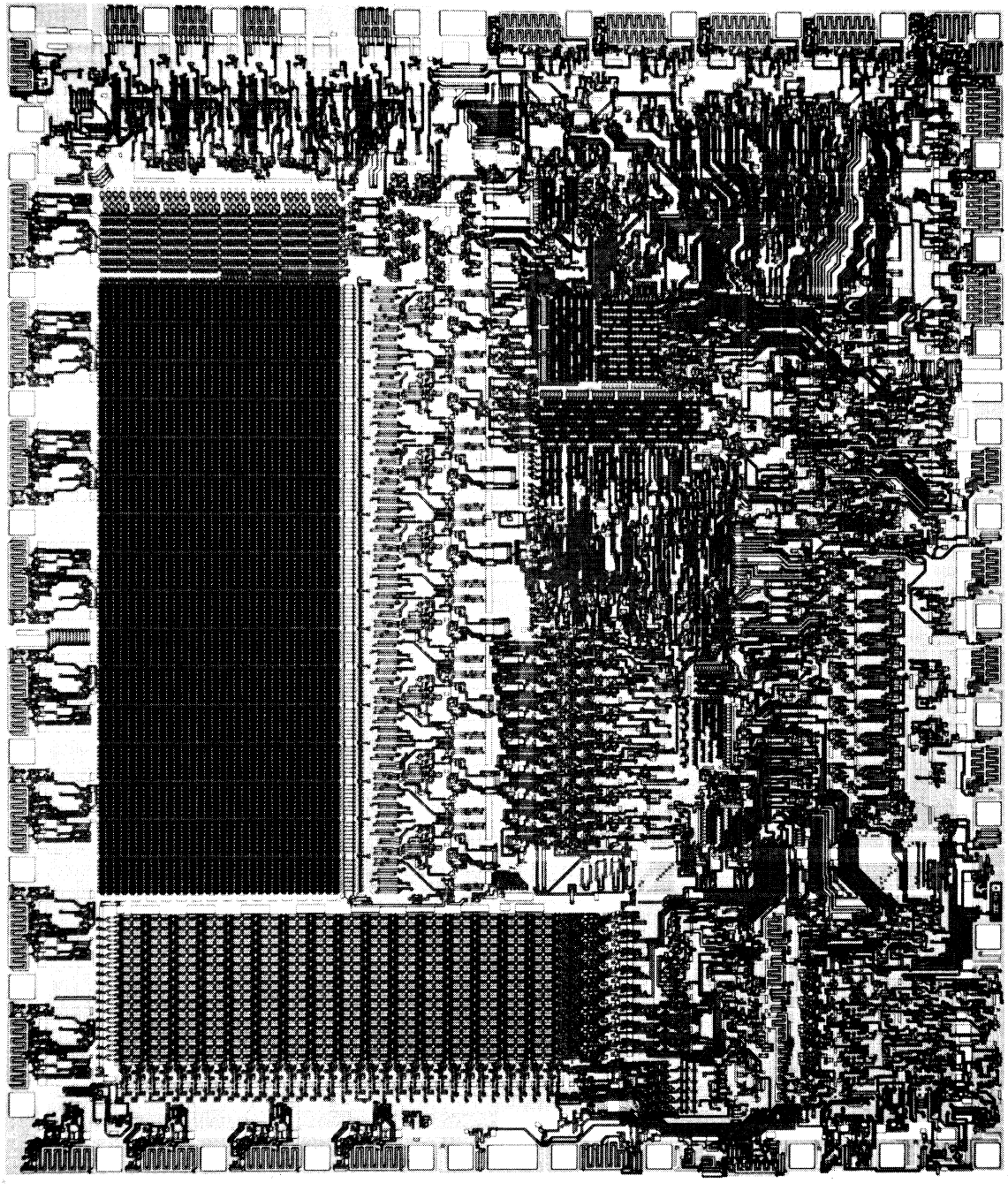
TTL CLOCK OUTPUTS

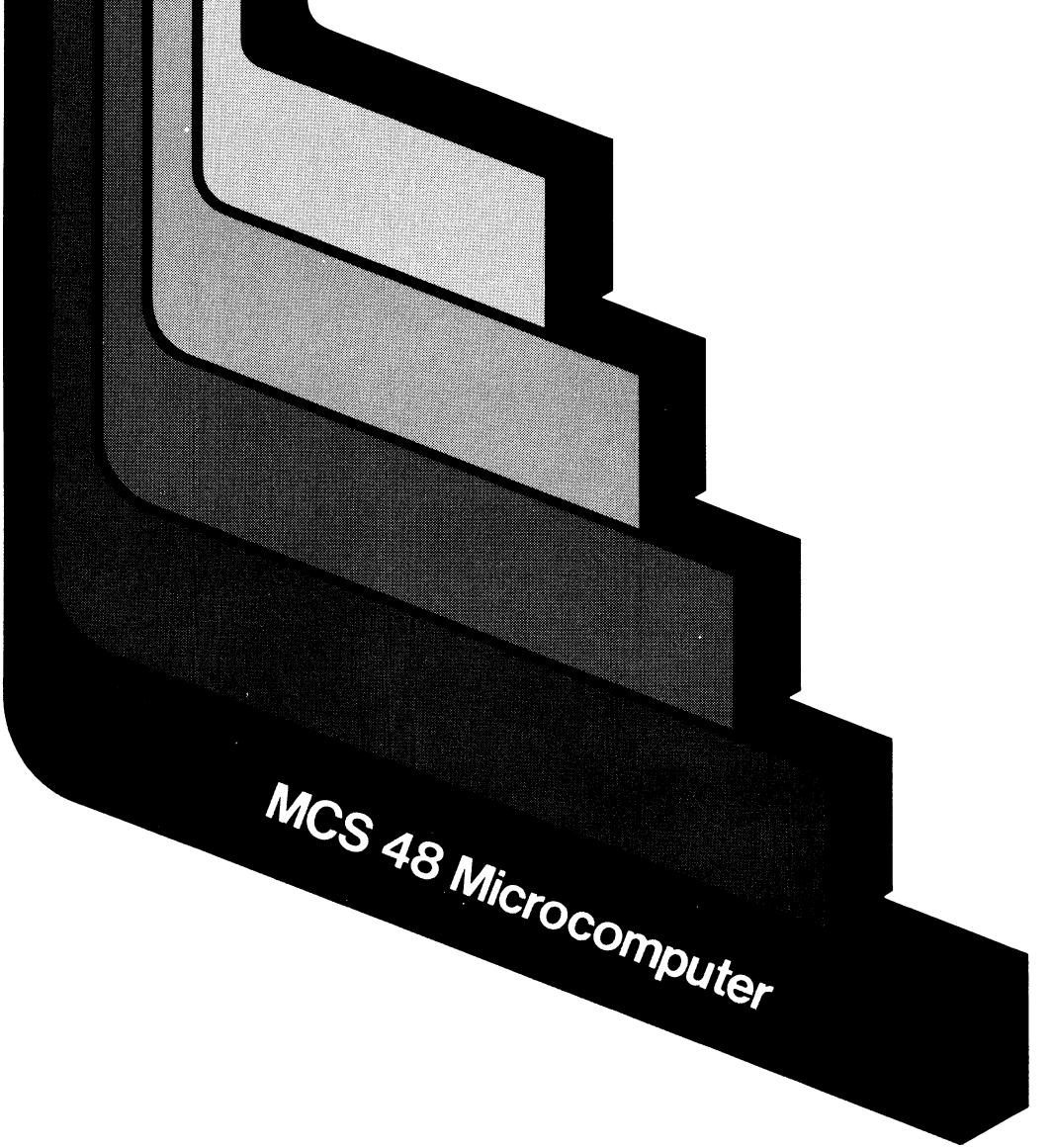
If ϕ_{1T} and ϕ_{2T} are used, GND pin should be tied to logic ground. ϕ_{2T} levels will swing between V_{CC} and GND.

UNUSED FUNCTIONS

If any of the 4201A functions listed below are not used, for power conservation it is recommended that the pins be connected as described below:

1. ϕ_{1T},ϕ_{2T}
   Tie GND pin, ϕ_{1T}, ϕ_{2T} to V_{CC}.
2. Single step
   Tie NO to V_{CC}.
   Tie NC to Node (B) (V_{DD} pin).
   Tie STOP ACK to V_{CC}.
   STOP left open.
3. Reset
   Tie RESET IN, RESET OUT to V_{CC}.




MCS 48 Microcomputer

MCS-48™ MICROCOMPUTER

TABLE OF CONTENTS

INTRODUCTION

The MCS-48™ Microcomputer family is the first family of true single-chip microcomputers. The 8048 contains the following functions in a 40-pin package:

8-bit CPU
1K x 8 ROM Program Memory
64 x 8 RAM Data Memory
27 I/O Lines
8-bit Timer/Event Counter
8-level Stack
Single Level Interrupt

A repertoire of over 90 instructions requiring only one or two clock cycles make the 8048 single chip microcomputer equal in performance to many multichip microprocessors. Only a single 5V power supply is required for operation.

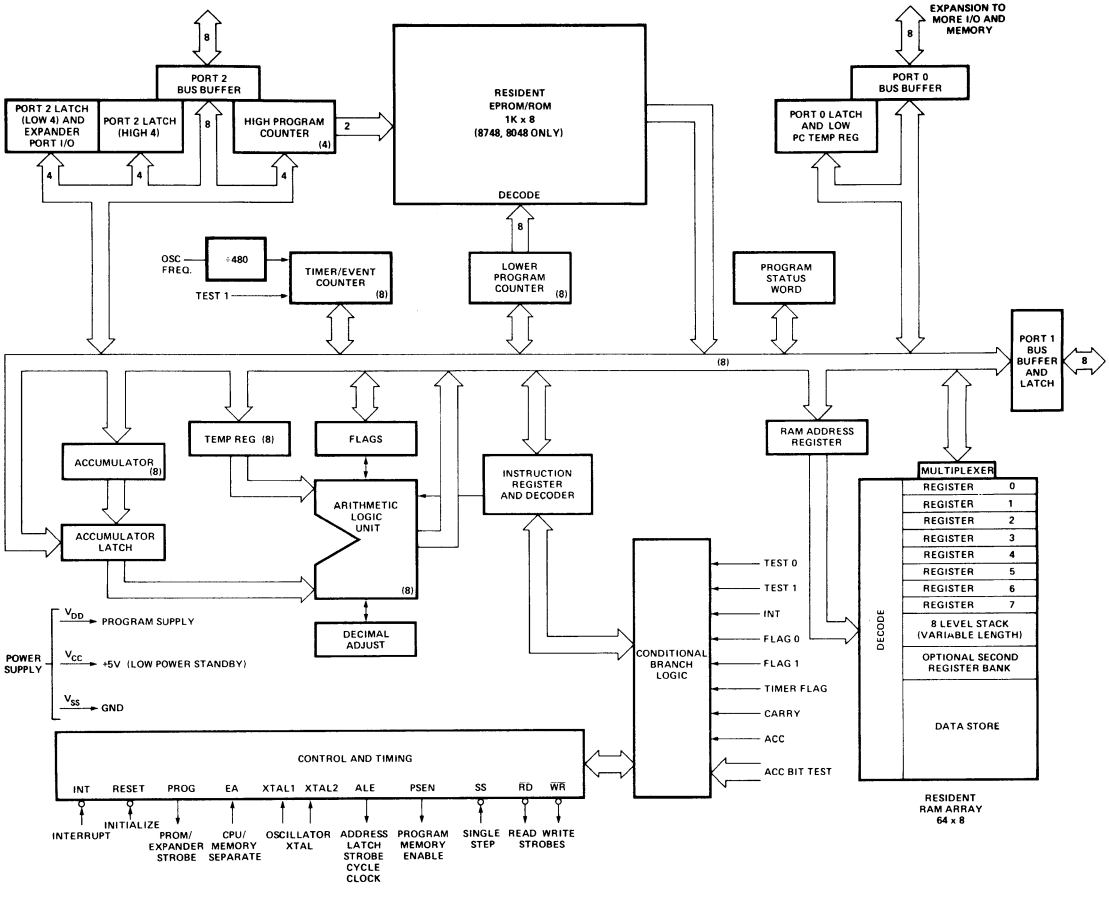
For prototype or low volume applications, the pin and functionally interchangeable 8748 provides user programmable and erasable EPROM Memory in place of the 8048 mask programmable ROM.

The 8035 is an 8048 without internal progam memory which allows the user to match his program memory requirements exactly by using a wide variety of external memories.

To allow the MCS-48 to solve a wide range of problems and to provide for future expansion, all 8048 functions have been made externally expandable using either special expanders or standard memories and peripherals. An efficient low cost means of I/O expansion is provided by the 8243 I/O Expander which provides 16 I/O lines in a 24-pin package. For systems with large I/O requirements multiple 8243's can be used.

For such applications as Keyboards, Displays, Serial communication lines, etc., standard 8000 Series peripheral circuits may be added. Program and data memory may be expanded using standard memories or the 8355 and 8155 memories that also include programmable I/O lines and timing functions.

The 8048 is an efficient control processor as well as an arithmetic processor. The instruction set allows the user to directly set and reset individual lines within its I/O ports as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions make the 8048 efficient in implementing standard logic functions. Special attention was also given to code efficiency, over 70% of the instructions being single byte and all others being only two bytes. Because of this efficiency, many applications requiring 1.5K to 2.0K bytes of program storage in other processors may be compressed into the 1K words resident in the 8048.



8048/8748/8035 BLOCK DIAGRAM

8048/8748/8035
SINGLE COMPONENT 8-BIT MICROCOMPUTER

***8048 Mask Programmable ROM**
***8748 User Programmable/Erasable EPROM**
***8035 External ROM or EPROM**

- **8-Bit CPU, ROM, RAM, I/O in Single Package**
- **Interchangeable ROM and EPROM Versions**
- **Single 5V Supply**
- **2.5 µsec and 5.0 µsec Cycle Versions All Instructions 1 or 2 Cycles.**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 ROM/EPROM 64 x 8 RAM 27 I/O Lines**
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8000 Series Peripherals**
- **Single Level Interrupt**

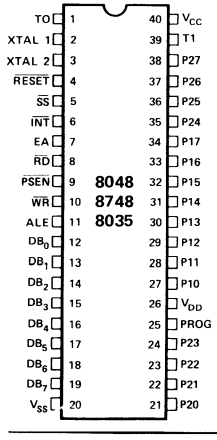
The Intel® 8048/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and 8000 series peripherals. The 8035 is the equivalent of an 8048 without program memory.

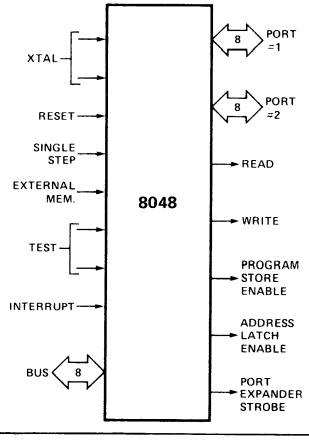
To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the 8048 with factory-programmed mask ROM program memory for low-cost high volume production, and the 8035 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

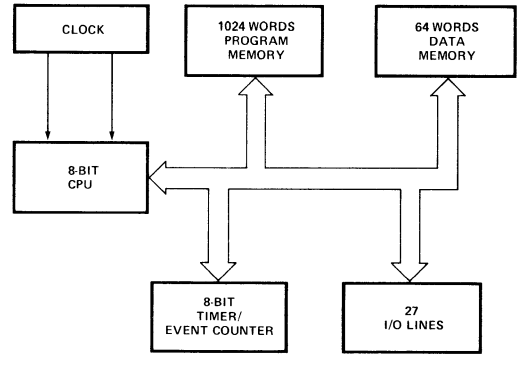
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage On Any Pin With Respect to Ground ..... -0.5V to +7V
Power Dissipation ..... 1.5 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = V_{DD} = +5V ±5%, V_{SS} = 0V

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except XTAL1, XTAL2)	-.5		.8	V	
V_{IH}	Input High Voltage (All Except XTAL1,XTAL2,$\overline{RESET}$)	2.0		V_{CC}	V	
V_{IH1}	Input High Voltage ($\overline{RESET}$,XTAL1)	3.0		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			.45	V	I_{OL} = 2.0mA
V_{OL1}	Output Low Voltage (All Other Outputs Except PROG)			.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	I_{OH} = 100μA
V_{OH1}	Output High Voltage (All Other Outputs)	2.4			V	I_{OH} = 50μA
I_{IL}	Input Leakage Current (T1, EA, $\overline{INT}$)			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{OL}	Output Leakage Current (Bus, T0) (High Impedance State)			-10	μA	$V_{CC} \geqslant V_{IN} \geqslant V_{SS}$ +.45
I_{DD}	V_{DD} Supply Current		10	30	mA	
I_{CC}	V_{CC} Supply Current		80	180	mA	

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = V_{DD} = +5V ±5%, V_{SS} = 0V

Symbol	Parameter	8048/8748/8035		8048-8 8748-8 8035-8		Unit	Conditions (Note 1)
		Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	400		800		ns	
t_{AL}	Address Setup to ALE	150		150		ns	
t_{LA}	Address Hold from ALE	80		80		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	900		1800		ns	
t_{DW}	Data Set-Up Before $\overline{WR}$	500		1000		ns	
t_{WD}	Data Hold After $\overline{WR}$	120		120		ns	C_L = 20pF
t_{CY}	Cycle Time	2.5	15.0	5.0	15.0	μs	6 MHz XTAL (3 MHz XTAL for -8)
t_{DR}	Data Hold	0	200	0	200	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500		1000	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		260		ns	
t_{AD}	Address Setup to Data In		950		1900	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0		0		ns	

Note 1: Control Outputs: C_L = 80 pF, 2.2K to V_{SS}, 4.3K to V_{CC}
BUS Outputs: C_L = 150 pF, 2.2K to V_{SS}, 4.3K to V_{CC} t_{CY} = 2.5μs

MCS 48

8748 ERASURE CHARACTERISTICS

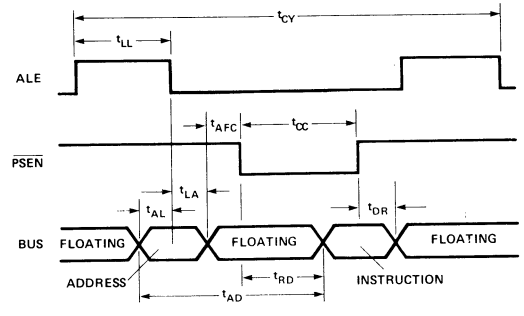
The erasure characteristics of the 8748 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level flourescent lighting could erase the typical 8748 in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8748 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8748 window to prevent unintentional erasure.

The recommended erasure procedure (see page 3-55) for the 8748 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm^2 power rating. The 8748 should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

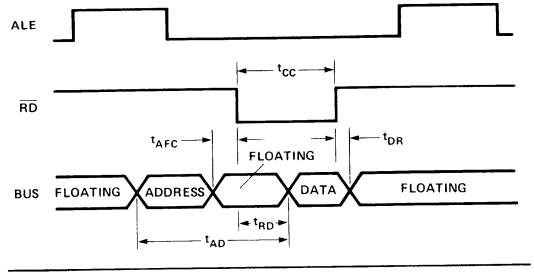
8748 EPROM PROGRAMMING

See the EPROM programming section, page 3-55.

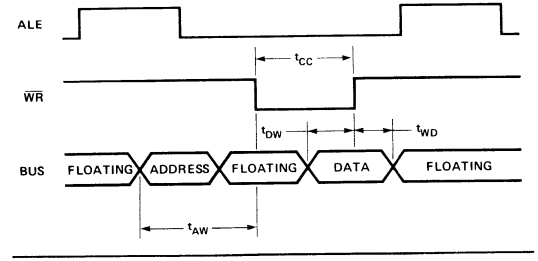
WAVEFORMS



INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL DATA MEMORY

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 ROM version.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+25V) input pin during 8748 programming.
		Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243
DB_0-DB_7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

Designation	Pin #	Function
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
		Used as a Read Strobe to External Data Memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low)
$\overline{WR}$	10	Output strobe during a BUS write. (Active low)(Non TTL V_{IH})
		Used as write strobe to External Data Memory.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle
Accumulator	ADD A, R	Add register to A	1	1
	ADD A, @R	Add data memory to A	1	1
	ADD A, #data	Add immediate to A	2	2
	ADDC A, R	Add register with carry	1	1
	ADDC A, @R	Add data memory with carry	1	1
	ADDC A, #data	Add immediate with carry	2	2
	ANL A, R	And register to A	1	1
	ANL A, @R	And data memory to A	1	1
	ANL A, #data	And immediate to A	2	2
	ORL A, R	Or register to A	1	1
	ORL A, @R	Or data memory to A	1	1
	ORL A, #data	Or immediate to A	2	2
	XRL A, R	Exclusive Or register to A	1	1
	XRL A, @R	Exclusive or data memory to A	1	1
	XRL A, #data	Exclusive or immediate to A	2	2
	INC A	Increment A	1	1
	DEC A	Decrement A	1	1
	CLR A	Clear A	1	1
	CPL A	Complement A	1	1
	DA A	Decimal Adjust A	1	1
	SWAP A	Swap nibbles of A	1	1
	RL A	Rotate A left	1	1
	RLC A	Rotate A left through carry	1	1
	RR A	Rotate A right	1	1
	RRC A	Rotate A right through carry	1	1
Input/Output	IN A, P	Input port to A	1	2
	OUTL P, A	Output A to port	1	2
	ANL P, #data	And immediate to port	2	2
	ORL P, #data	Or immediate to port	2	2
	INS A, BUS	Input BUS to A	1	2
	OUTL BUS, A	Output A to BUS	1	2
	ANL BUS, #data	And immediate to BUS	2	2
	ORL BUS, #data	Or immediate to BUS	2	2
	MOVD A, P	Input Expander port to A	1	2
	MOVD P, A	Output A to Expander port	1	2
	ANLD P, A	And A to Expander port	1	2
	ORLD P, A	Or A to Expander port	1	2
Registers	INC R	Increment register	1	1
	INC @R	Increment data memory	1	1
	DEC R	Decrement register	1	1
Branch	JMP addr	Jump unconditional	2	2
	JMPP @A	Jump indirec	1	2
	DJNZ R, addr	Decrement register and skip	2	2
	JC addr	Jump on Carry = 1	2	2
	JNC addr	Jump on Carry = 0	2	2
	J Z addr	Jump on A Zero	2	2
	JNZ addr	Jump on A not Zero	2	2
	JT0 addr	Jump on T0 = 1	2	2
	JNT0 addr	Jump on T0 = 0	2	2
	JT1 addr	Jump on T1 = 1	2	2
	JNT1 addr	Jump on T1 = 0	2	2
	JF0 addr	Jump on F0 = 1	2	2
	JF1 addr	Jump on F1 = 1	2	2
	JTF addr	Jump on timer flag	2	2
	JNI addr	Jump on $\overline{INT}$ = 0	2	2
	JBb addr	Jump on Accumulator Bit	2	2

	Mnemonic	Description	Bytes	Cycles
Subroutine	CALL	Jump to subroutine	2	2
	RET	Return	1	2
	RETR	Return and restore status	1	2
Flags	CLR C	Clear Carry	1	1
	CPL C	Complement Carry	1	1
	CLR F0	Clear Flag 0	1	1
	CPL F0	Complement Flag 0	1	1
	CLR F1	Clear Flag 1	1	1
	CPL F1	Complement Flag 1	1	1
Data Moves	MOV A, R	Move register to A	1	1
	MOV A, @R	Move data memory to A	1	1
	MOV A, #data	Move immediate to A	2	2
	MOV R, A	Move A to register	1	1
	MOV @R, A	Move A to data memory	1	1
	MOV R, #data	Move immediate to register	2	2
	MOV @R, #data	Move immediate to data memory	2	2
	MOV A, PSW	Move PSW to A	1	1
	MOV PSW, A	Move A to PSW	1	1
	XCH A, R	Exchange A and register	1	1
	XCHA,@R	Exchange A and data memory	1	1
	XCHD A, @R	Exchange nibble of A and register	1	1
	MOVX A, @R	Move external data memory to A	1	2
	MOVX @R, A	Move A to external data memory	1	2
	MOVP A, @A	Move to A from current page	1	2
	MOVP3 A, @A	Move to A from Page 3	1	2
Timer/Counter	MOV A, T	Read Timer/Counter	1	1
	MOV T, A	Load Timer/Counter	1	1
	STRT T	Start Timer	1	1
	STRT CNT	Start Counter	1	1
	STOP TCNT	Stop Timer/Counter	1	1
	EN TCNTI	Enable Timer/Counter Interrupt	1	1
	DIS TCNTI	Disable Timer/Counter Interrupt	1	1
Control	EN I	Enable external interrupt	1	1
	DIS I	Disable external interrupt	1	1
	SEL RB0	Select register bank 0	1	1
	SEL RB1	Select register bank 1	1	1
	SEL MB0	Select memory bank 0	1	1
	SEL MB1	Select memory bank 1	1	1
	ENT0 CLK	Enable Clock output on T0	1	1
	NOP	No Operation	1	1

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

8243
MCS-48™
INPUT/OUTPUT EXPANDER

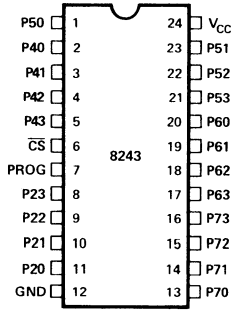
- **Low Cost**
- **Simple Interface to MCS-48™ Microcomputers**
- **Four 4-Bit I/O Ports**
- **AND and OR Directly to Ports**
- **24 Pin DIP**
- **Single 5V Supply**
- **High Output Drive**
- **Direct Extension of Resident 8048 I/O Ports**

The 8243 is an input/output expander designed specifically to provide a low cost means of I/O expansion for the MCS-48 family of single-chip microcomputers. Fabricated in 5 volts NMOS, the 8243 combines low cost, single supply voltage and high drive current capability.

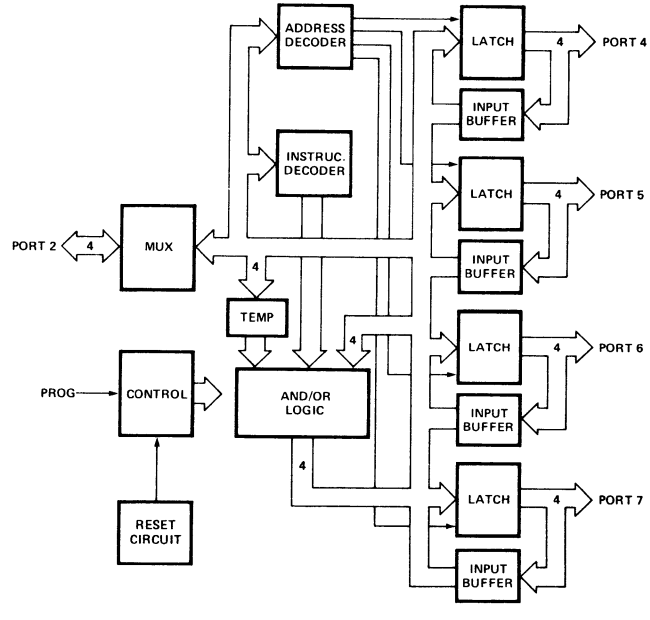
The 8243 consists of four 4-bit bi-directional static I/O ports and one 4-bit port which serves as an interface to the MCS-48 microcomputers. The 4-bit interface requires that only four (4) I/O lines of the 8048 be used for I/O expansion and also allows multiple 8243's to be added to the same bus.

The I/O ports of the 8243 serve as a direct extension of the resident I/O facilities of the MCS-48 microcomputers and are accessed by their own MOV, ANL, and ORL instructions.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Pin No.	Function
PROG*	7	Clock Input. A high to low transistion on PROG signifies that address and control are available on P20-P23, and a low to high transition signifies that data is available on P20-23.
$\overline{CS}$	6	Chip Select Input. A high on CS inhibits any change of output or internal status.
P20-P23	11-8	Four (4) bit bi-directional port contains the address and control bits on a high to low transition of PROG. During a low to high transition contains the data for a selected output port if a write operation, or the data from a selected port before the low to high transition if a read operation.
GND	12	0 volt supply.
P40-P43 P50-P53 P60-P63 P70-P73	2-5 1,23-21 20-17 13-16	Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write) or a tri-state (after read). Data on pins P20-23 may be directly written, ANDed or ORed with previous data.
V_{CC}	24	+5 volt supply.

FUNCTIONAL DESCRIPTION

General Operation

The 8243 contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports:

- Transfer Accumulator to Port.
- Transfer Port to Accumulator.
- AND Accumulator to Port.
- OR Accumulator to Port.

All communication between the 8048 and the 8243 occurs over Port 2 (P20-P23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles:

The first containing the "op code" and port address and the second containing the actual 4-bits of data.

A high to low transition of the PROG line indicates that address is present while a low to high transition indicates the presence of data. Additional 8243's may be added to the 4-bit bus and chip selected using additional output lines from the 8048/8748/8035.

Power On Initialization

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

Write Modes

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi,A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi,A takes new data AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

Read Mode

The device has one read mode. The operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are tri-stated, and the input buffers switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the tri-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the 8243 output.

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%

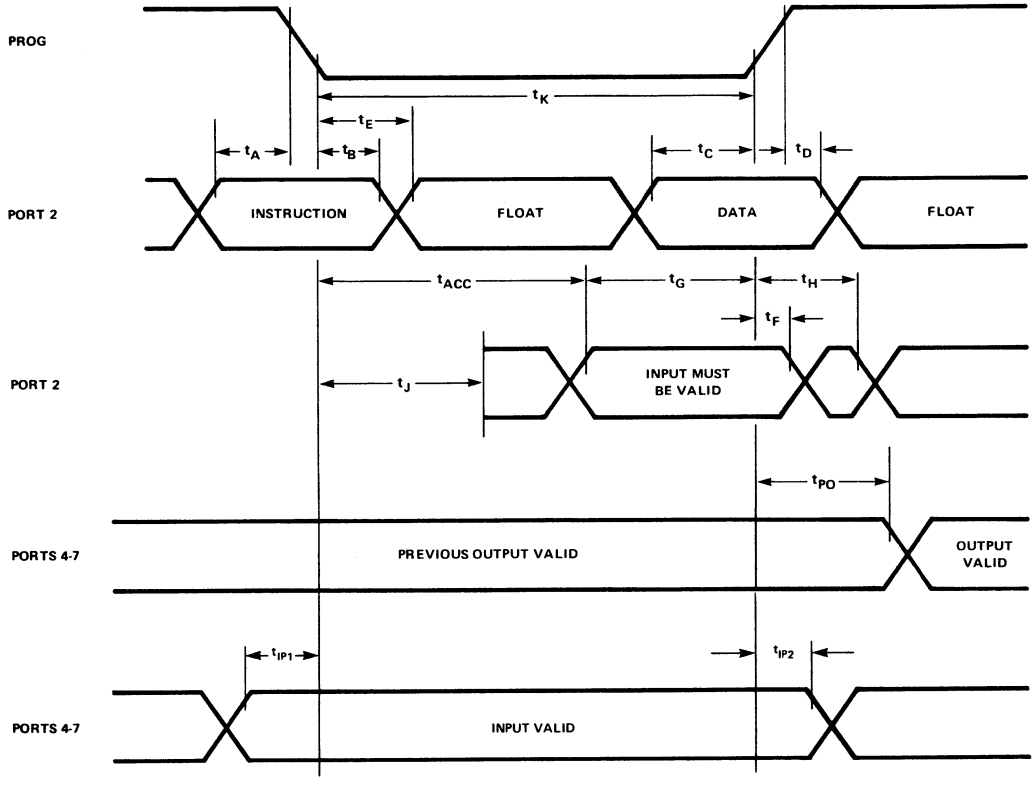
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL1}	Output Low Voltage Ports 4-7		0.45	V	I_{OL} = 10 mA
V_{OL2}	Output Low Voltage Ports 4-7		TBD	V	I_{OL} = 20 mA
V_{OH1}	Output High Voltage Ports 4-7	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage Ports 4-7		TBD	μA	V_{in} = V_{CC} to 0V
V_{OL3}	Output Low Voltage Port 2		.45	V	I_{OL} = 0.8mA
I_{CC}	V_{CC} Supply Current		40	mA	
V_{OH2}	Output Voltage Port 2	2.4			I_{OH} = -200 μA
I_{VSS}	I_{CC} Plus Sum of all I_{OL} from 16 Outputs		120	mA	

A.C. CHARACTERISTICS

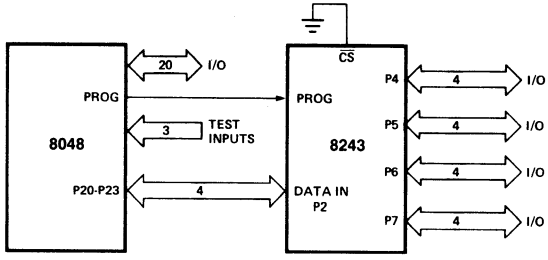
T_A = 0°C to 70°C, V_{CC} = 5V ±5%

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_A	Code Valid Before PROG	70		ns	80 pF Load
t_B	Code Valid After PROG	60		ns	20 pF Load
t_C	Data Valid Before PROG	200		ns	80 pF Load
t_D	Data Valid After PROG	20		ns	20 pF Load
t_E	Float After PROG		700	ns	
t_J	Enabled After PROG	200		ns	
t_G	Data Valid Before PROG	300		ns	80 pF Load
t_F	Data Valid After PROG	20		ns	20 pF Load
t_H	Floating After PROG		100	ns	20 pF Load
t_K	PROG Negative Pulse Width	900		ns	
t_{CP}	CS Valid Before PROG	TBD			
t_{PC}	CS Valid Before PROG	TBD			
t_{PO}	Ports 4-7 Valid After PROG		TBD		100 pF Load
t_{IP1}	Ports 4-7 Valid Before PROG	TBD			
t_{IP2}	Ports 4-7 Valid After PROG	TBD			
t_{ACC}	Port 2 Valid After PROG		600	ns	80 pF Load

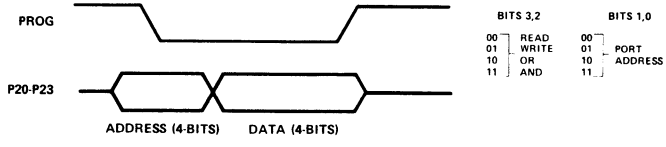
WAVEFORMS

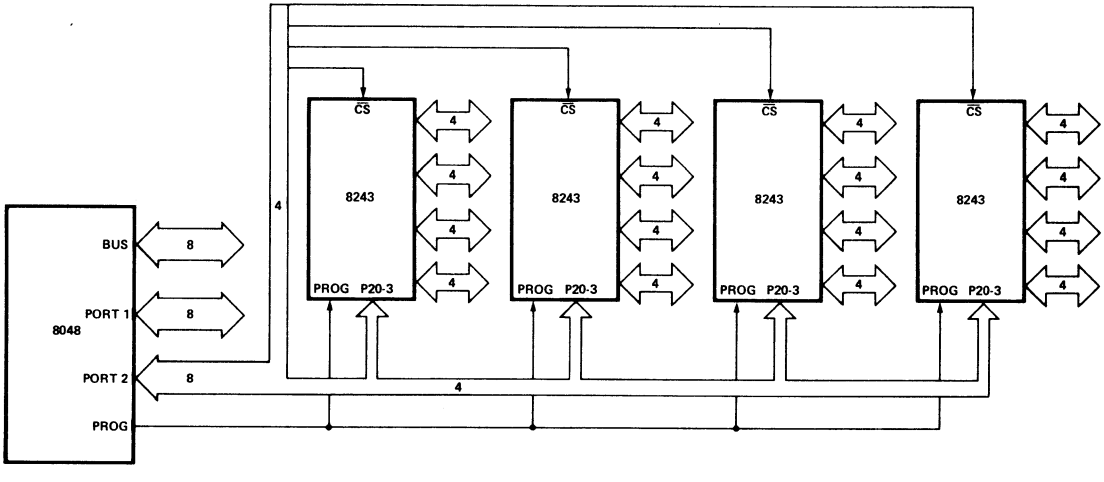


EXPANDER INTERFACE



OUTPUT EXPANDER TIMING





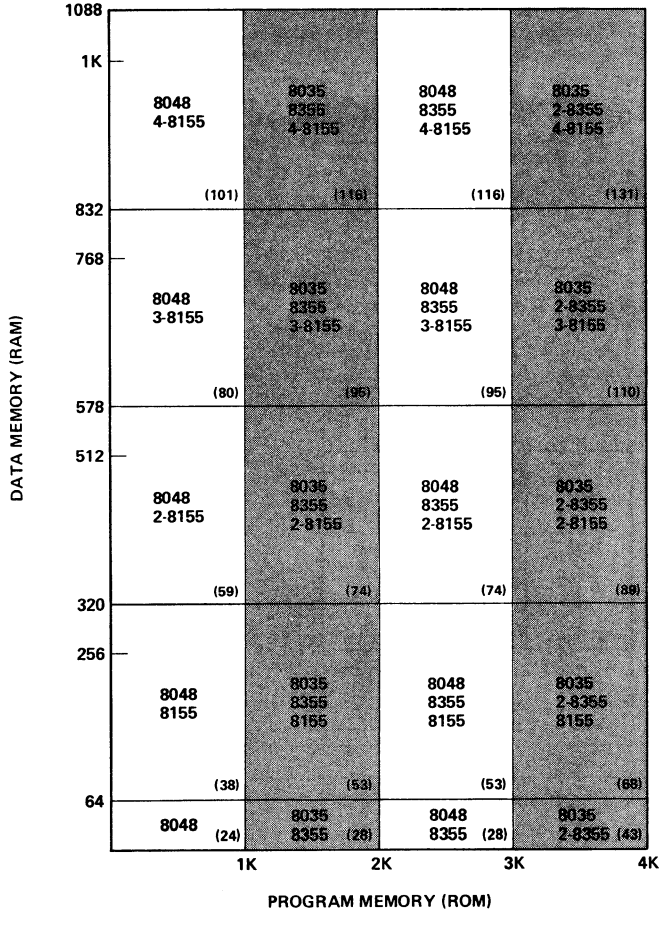
USING MULTIPLE 8243's

EXPANSION OF THE MCS-48™ SYSTEM

The 8048/8748 or the 8035 may use various combinations of the 8355/8755 Program Memory and I/O Expander and the 8155 Data Memory and I/O Expander.

Data Memory can be expanded beyond the resident 64 words in blocks of 256 by adding 8155's. Program Memory can be expanded beyond the resident 1K in blocks of 1K by using the 8355/8755 in combination with the 8035 or 8048. Since the 8355 contains 2K words, the 8035 is needed to fill the "gaps". For program memory of 1K or less use the 8048. For programs in the 1 to 2K range use an 8035/8355 combination and for the 2 to 3K range use an 8048/8355 combination.

For compatible 8000 Series components see page 10-4.



( ) Number of Available I/O Lines

10

MCS-80/85™ MICROPROCESSOR

INTRODUCTION

Intel 8000 Series microprocessor elements may be used to form a variety of microcomputer systems. Powerful 8-bit CPU's such as the 8080A and 8085, combined with general purpose or dedicated peripherals, memories and other LSI blocks, make the Intel 8000 Series the largest and most versatile microcomputer family available.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

RECOMMENDED PRODUCTS FOR MCS-48/80/85 MICROCOMPUTER APPLICATIONS

Function	Part No.	Page No.	Description	T_{ACC} In ns	8048	8748	8035	8085	8080A	8008
Memory and I/O Expanders for MCS-48/85	8155	10-63	RAM-I/O		X	X	X	X		
	8355	10-75	ROM-I/O		X	X	X	X		
	8755	10-82	EPROM-I/O		X	X	X	X		
RAMs (Static)	8101A-4	10-88	256 x 4	450	X	X	X	X	X	X
	8102A-4	10-91	1K x 1	450	X	X	X	X	X	X
	8111A-4	10-95	256 x 4	450	X	X	X	X	X	X
	5101	2-112	256 x 4 CMOS	450	X	X	X	X	X	X
	2114	2-76	1K x 4	450	X	X	X	X	X	X
RAMs (Dynamic)	2104A-4	2-40	4K x 1	300				X	X	
	2107B-4	2-54	4K x 1	270				X	X	
	2116-4	2-95	16K x 1	300				X	X	
RAM Support Circuits	3222	5-19	Refresh Controller					X	X	
	3232	5-24	Refresh Counter/ Multiplexer					X	X	
	3242	5-28	Refresh Counter/ Multiplexer					X	X	
ROMs	8308	10-98	1K x 8	450	X	X	X	X	X	X
	8316A	10-102	2K x 8	850	X	X	X	X	X	X
	2316E	3-21	2K x 8	450	X	X	X	X	X	X
EPROMs	1702A-2	3-5	256 x 8	650					X	X
	8708	10-105	1K x 8	450	X	X	X	X	X	X
	2708	3-24	1K x 8	450	X	X	X	X	X	X
	2716	3-30	2K x 8	450	X	X	X	X	X	X
Peripherals	8205	10-108	1-8 Decoder		X	X	X	X	X	X
	8212	10-114	8-Bit Latch		X	X	X	X	X	X
	8214	10-128	Priority Unit		X	X	X	X	X	X
	8216	10-135	4-Bit Bus Driver		X	X	X	X	X	X
	8224	10-33	Clock Generator						X	
	8226	10-135	4-Bit Bus Driver		X	X	X	X	X	X
	8228	10-43	System Controller						X	
	8238	10-43	System Controller						X	
	8251	10-143	USART		X	X	X	X	X	X
	8253	10-159	Interval Timer		X	X	X	X	X	X
	8255A	10-170	PPI		X	X	X	X	X	X
	8257	10-195	DMA					X	X	
	8259	10-212	Interrupt		X	X	X	X	X	
	8271	10-228	Floppy Disk		X	X	X	X	X	
	8273	10-232	SDLC		X	X	X	X	X	
	8275	10-236	CRT		X	X	X	X	X	
	8279	10-240	KYBD/Display		X	X	X	X	X	X

8008/8008-1
EIGHT-BIT MICROPROCESSOR

- **Instruction Cycle Time — 12.5 μs with 8008-1 or 20 μs with 8008**
- **Directly Addresses 16K x 8 Bits of Memory (RAM, ROM, or S.R.)**
- **Interrupt Capability**
- **48 Instructions, Data Oriented**
- **Address Stack Contains Eight 14-Bit Registers (Including Program Counter) Which Permit Nesting of Subroutines Up To Seven Levels**

The 8008 is a single chip MOS 8-bit parallel central processor unit for the MCS-8 microcomputer system.

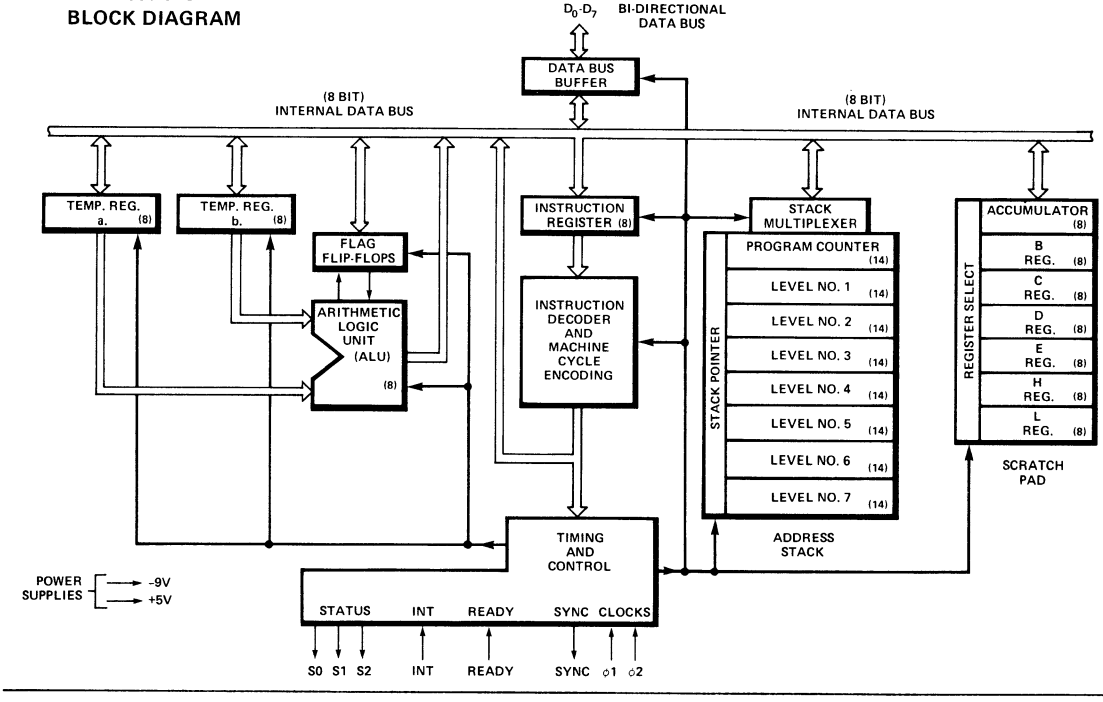
This CPU contains six 8-bit data registers, an 8-bit accumulator, two 8-bit temporary registers, four flag bits (carry, zero, sign, parity), and an 8-bit parallel binary arithmetic unit which implements addition, subtraction, and logical operations. A memory stack containing a 14-bit program counter and seven 14-bit words is used internally to store program and subroutine addresses. The 14-bit address permits the direct addressing of 16K words of memory (any mix of RAM, ROM or S.R.).

The instruction set of the 8008 consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutine.

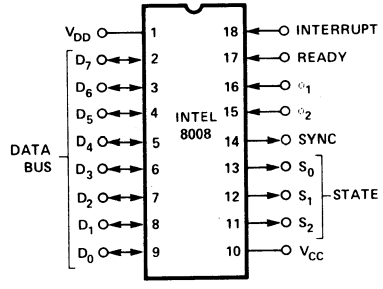
The normal program flow of the 8008 may be interrupted through the use of the INTERRUPT control line. This allows the servicing of slow I/O peripheral devices while also executing the main program.

The READY command line synchronizes the 8008 to the memory cycle allowing any type or speed of semiconductor memory to be used.

8008 CPU
BLOCK DIAGRAM



8008 FUNCTIONAL PIN DESCRIPTION



D_0-D_7

BI-DIRECTIONAL DATA BUS. All address and data communication between the processor and the program memory, data memory, and I/O devices occurs on these 8 lines. Cycle control information is also available.

INT

INTERRUPT input. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.

READY

READY input. This command line is used to synchronize the 8008 to the memory cycle allowing any speed memory to be used.

SYNC

SYNC output. Synchronization signal generated by the processor. It indicates the beginning of a machine cycle.

ϕ_1, ϕ_2

Two phase clock inputs.

S_0, S_1, S_2

MACHINE STATE OUTPUTS. The processor controls the use of the data bus and determines whether it will be sending or receiving data. State signals S_0, S_1, and S_2, along with SYNC inform the peripheral circuitry of the state of the processor.

V_{CC} +5V ±5%

V_{DD} -9V ±5%

BASIC INSTRUCTION SET

Data and Instruction Formats

Data in the 8008 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference, I/O arithmetic or logical, rotate or return instructions
Two Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	Immediate mode instructions
Three Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS	JUMP or CALL instructions
X X D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS*	*For the third byte of this instruction, D_6 and D_7 are "don't care" bits.

For the MCS-8™ a logic "1" is defined as a high level and a logic "0" is defined as a low level.

Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE D_7 D_6	D_5 D_4 D_3	D_2 D_1 D_0	DESCRIPTION OF OPERATION
(1) MOV r_1, r_2	(5)	1 1	D D D	S S S	Load index register r_1 with the content of index register r_2.
(2) MOV r, M	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
MOV M, r	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) MVI r	(8)	0 0 B B	D D D B B B	1 1 0 B B B	Load index register r with data B . . . B.
MVI M	(9)	0 0 B B	1 1 1 B B B	1 1 0 B B B	Load memory register M with data B . . . B.
INR r	(5)	0 0	D D D	0 0 0	Increment the content of index register r (r ≠ A).
DCR r	(5)	0 0	D D D	0 0 1	Decrement the content of index register r (r ≠ A).

Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADD r	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADD M	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0 B B	0 0 0 B B B	1 0 0 B B B	
ADC r	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B from the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ADC M	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0 B B	0 0 1 B B B	1 0 0 B B B	
SUB r	(5)	1 0	0 1 0	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUB M	(8)	1 0	0 1 0	1 1 1	
SUI	(8)	0 0 B B	0 1 0 B B B	1 0 0 B B B	
SBB r	(5)	1 0	0 1 1	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBB M	(8)	1 0	0 1 1	1 1 1	
SBI	(8)	0 0 B B	0 1 1 B B B	1 0 0 B B B	

BASIC INSTRUCTION SET

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7 D_6$	$D_5 D_4 D_3$	$D_2 D_1 D_0$	DESCRIPTION OF OPERATION
ANA r	(5)	1 0	1 0 0	S S S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
ANA M	(8)	1 0	1 0 0	1 1 1	
ANI	(8)	0 0 B B	1 0 0 B B B	1 0 0 B B B	
XRA r	(5)	1 0	1 0 1	S S S	Compute the EXCLUSIVE OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
XRA M	(8)	1 0	1 0 1	1 1 1	
XRI	(8)	0 0 B B	1 0 1 B B B	1 0 0 B B B	
ORA r	(5)	1 0	1 1 0	S S S	Compute the INCLUSIVE OR of the content of index register r, memory register m, or data B . . . B with the accumulator.
ORA M	(8)	1 0	1 1 0	1 1 1	
ORI	(8)	0 0 B B	1 1 0 B B B	1 0 0 B B B	
CMP r	(5)	1 0	1 1 1	S S S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CMP M	(8)	1 0	1 1 1	1 1 1	
CPI	(8)	0 0 B B	1 1 1 B B B	1 0 0 B B B	
RLC	(5)	0 0	0 0 0	0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0	0 0 1	0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0	0 1 0	0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0	0 1 1	0 1 0	Rotate the content of the accumulator right through the carry.
Program Counter and Stack Control Instructions					
(4) JMP	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$.
(5) JNC, JNZ, JP, JPO	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
JC, JZ JM, JPE	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
CALL	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$. Save the current address (up one level in the stack).
CNC, CNZ, CP, CPO	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is false, and save the current address (up one level in the stack.) Otherwise, execute the next instruction in sequence.
CC, CZ, CM, CPE	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
RET	(5)	0 0	X X X	1 1 1	Unconditionally return (down one level in the stack).
RNC, RNZ, RP, RPO	(3 or 5)	0 0	0 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
RC, RZ RM, RPE	(3 or 5)	0 0	1 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0	A A A	1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).
Input/Output Instructions					
IN	(8)	0 1	0 0 M	M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1	R R M	M M 1	Write the content of the accumulator into the selected output port (RRMMM, RR ≠ 00).
Machine Instruction					
HLT	(4)	0 0	0 0 0	0 0 X	Enter the STOPPED state and remain there until interrupted.
	(4)	1 1	1 1 1	1 1 1	

NOTES:

(1) SSS = Source Index Register, DDD = Destination Index Register. These registers, r_i, are designated A(accumulator–000), B(001), C(010), D(011), E(100), H(101), L(110).

(2) Memory registers are addressed by the contents of registers H & L.

(3) Additional bytes of instruction are designated by BBBBBBBB.

(4) X = "Don't Care".

(5) Flag flip-flops are defined by C_4C_3: carry (00-overflow or underflow), zero (01-result is zero), sign (10-MSB of result is "1"), parity (11-parity is even).

MCS 80/85

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−55°C to +150°C
Input Voltages and Supply Voltage With Respect to V_{CC}	+0.5 to −20V
Power Dissipation	1.0 W @ 25°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5% unless otherwise specified. Logic "1" is defined as the more positive level (V_{IH}, V_{OH}). Logic "0" is defined as the more negative level (V_{IL}, V_{OL}).

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
I_{DD}	AVERAGE SUPPLY CURRENT-OUTPUTS LOADED*		30	60	mA	T_A = 25°C
I_{LI}	INPUT LEAKAGE CURRENT			10	μA	V_{IN} = 0V
V_{IL}	INPUT LOW VOLTAGE (INCLUDING CLOCKS)	V_{DD}		V_{CC}−4.2	V	
V_{IH}	INPUT HIGH VOLTAGE (INCLUDING CLOCKS)	V_{CC}−1.5		V_{CC}+0.3	V	
V_{OL}	OUTPUT LOW VOLTAGE			0.4	V	I_{OL} = 0.44mA C_L = 200 pF
V_{OH}	OUTPUT HIGH VOLTAGE	V_{CC}−1.5			V	I_{OH} = 0.2mA

*Measurements are made while the 8008 is executing a typical sequence of instructions. The test load is selected such that at V_{OL} = 0.4V, I_{OL} = 0.44mA on each output.

A.C. CHARACTERISTICS

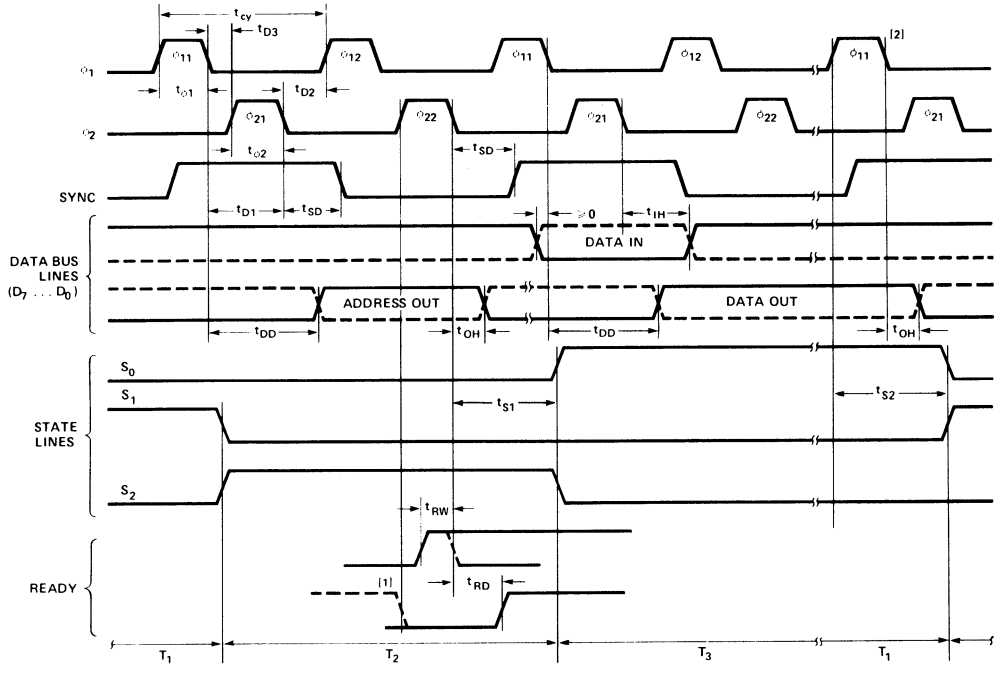
T_A = 0°C to 70°C; V_{CC} = +5V ±5%, V_{DD} = −9V ±5%. All measurements are referenced to 1.5V levels.

SYMBOL	PARAMETER	8008 LIMITS MIN.	8008 LIMITS MAX.	8008-1 LIMITS MIN.	8008-1 LIMITS MAX.	UNIT	TEST CONDITIONS
t_{CY}	CLOCK PERIOD	2	3	1.25	3	μs	t_R,t_F = 50ns
t_R,t_F	CLOCK RISE AND FALL TIMES		50		50	ns	
$t_{\phi 1}$	PULSE WIDTH OF ϕ_1	.70		.35		μs	
$t_{\phi 2}$	PULSE WIDTH OF ϕ_2	.55		.35		μs	
t_{D1}	CLOCK DELAY FROM FALLING EDGE OF ϕ_1 TO FALLING EDGE OF ϕ_2	.90	1.1		1.1	μs	
t_{D2}	CLOCK DELAY FROM ϕ_2 TO ϕ_1	.40		.35		μs	
t_{D3}	CLOCK DELAY FROM ϕ_1 TO ϕ_2	.20		.20		μs	
t_{DD}	DATA OUT DELAY		1.0		1.0	μs	C_L = 100pF
t_{OH}	HOLD TIME FOR DATA BUS OUT	.10		.10		μs	
t_{IH}	HOLD TIME FOR DATA IN	[1]		[1]		μs	
t_{SD}	SYNC OUT DELAY		.70		.70	μs	C_L = 100pF
t_{S1}	STATE OUT DELAY (ALL STATES EXCEPT T1 AND T1I)[2]		1.1		1.1	μs	C_L = 100pF
t_{S2}	STATE OUT DELAY (STATES T1 AND T1I)		1.0		1.0	μs	C_L = 100pF
t_{RW}	PULSE WIDTH OF READY DURING ϕ_{22} TO ENTER T3 STATE	.35		.35		μs	
t_{RD}	READY DELAY TO ENTER WAIT STATE	.20		.20		μs	

[1] t_{IH} MIN ≥ t_{SD}

[2] If the INTERRUPT is not used, all states have the same output delay, t_{S1}.

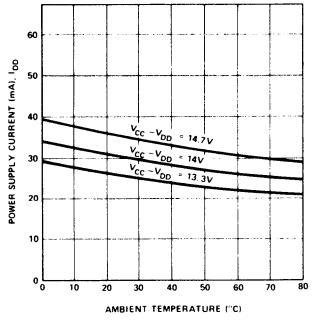
TIMING DIAGRAM



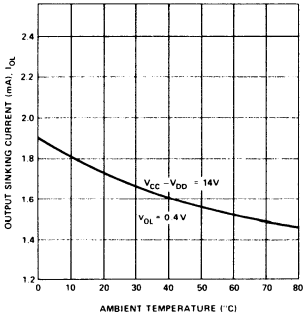
Notes: 1. READY line must be at "0" prior to ϕ_{22} of T_2 to guarantee entry into the WAIT state.
2. INTERRUPT line must not change levels within 200ns (max.) of falling edge of ϕ_1.

TYPICAL D.C. CHARACTERISTICS

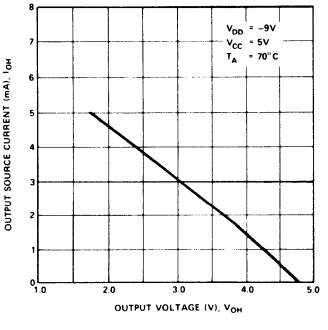
POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT SINKING CURRENT VS. TEMPERATURE

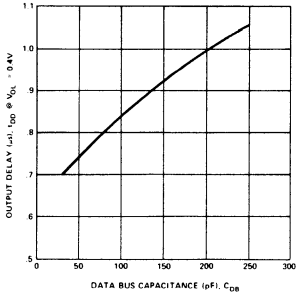


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



TYPICAL A.C. CHARACTERISTICS

DATA OUT DELAY VS. OUTPUT LOAD CAPACITANCE



CAPACITANCE f = 1MHz; T_A = 25°C; Unmeasured Pins Grounded

SYMBOL	TEST	LIMIT (pF)	
		TYP.	MAX.
C_{IN}	INPUT CAPACITANCE	5	10
C_{DB}	DATA BUS I/O CAPACITANCE	5	10
C_{OUT}	OUTPUT CAPACITANCE	5	10

8080A

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

- **TTL Drive Capability**
- **2 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal,Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

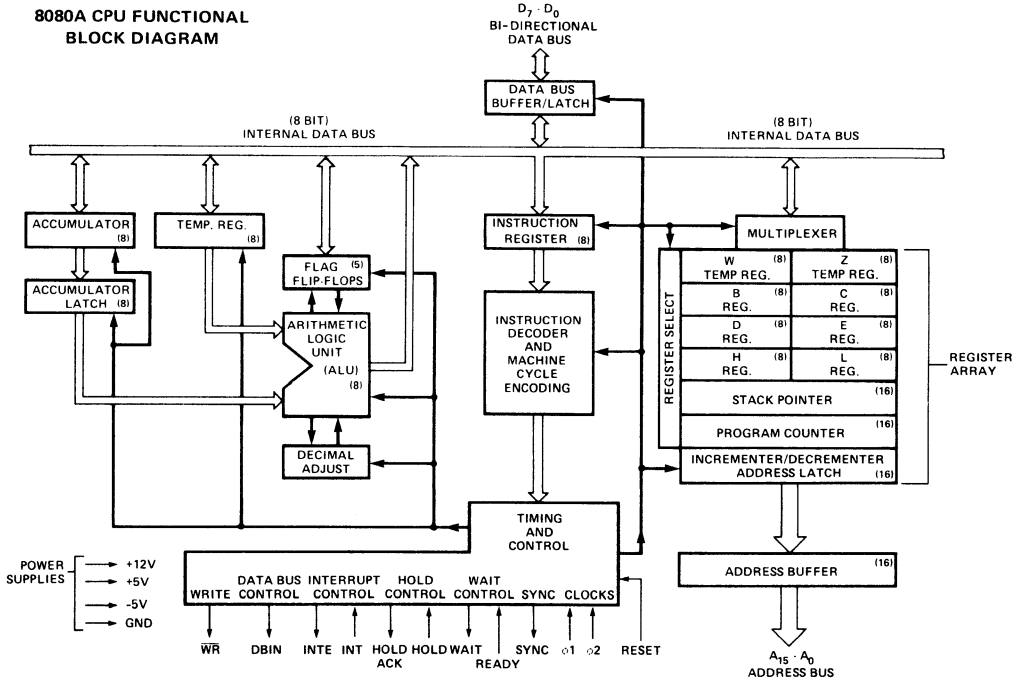
The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.

8080A CPU FUNCTIONAL BLOCK DIAGRAM



8080A FUNCTIONAL PIN DEFINITION

The following describes the function of all of the 8080A I/O pins. Several of the descriptions refer to internal timing periods.

A_{15}-A_0 (output three-state)
ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.

D_7-D_0 (input/output three-state)
DATA BUS; the data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D_0 is the least significant bit.

SYNC (output)
SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)
DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.

READY (input)
READY; the READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)
WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

$\overline{WR}$ (output)
WRITE; the $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR}$ = 0).

HOLD (input)
HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

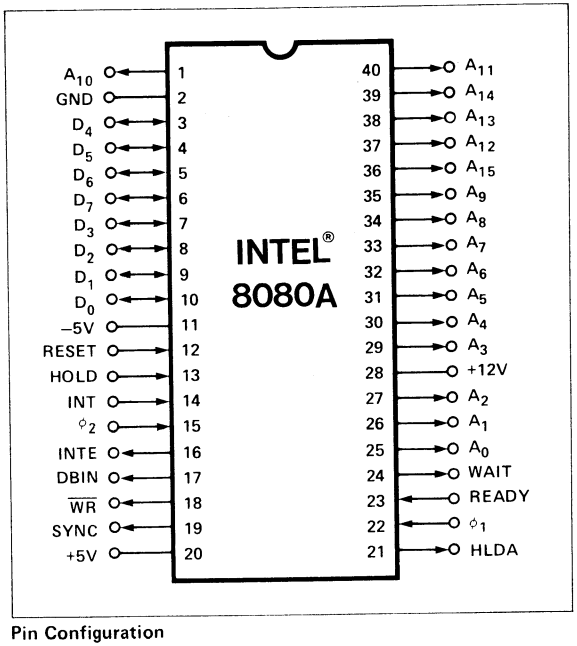
- the CPU is in the HALT state.
- the CPU is in the T2 or TW state and the READY signal is active.

As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)
HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:

- T3 for READ memory or input.
- The Clock Period following T3 for WRITE memory or OUTPUT operation.

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.



Pin Configuration

INTE (output)
INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)
INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input)[1]
RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS}	Ground Reference.
V_{DD}	+12 ± 5% Volts.
V_{CC}	+5 ± 5% Volts.
V_{BB}	-5 ±5% Volts (substrate bias).
ϕ_1, ϕ_2	2 externally supplied clock phases. (non TTL compatible

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70° C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = -150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	T_{CY} = .48 μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}+0.8V$ $V_{SS}+0.8V \leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

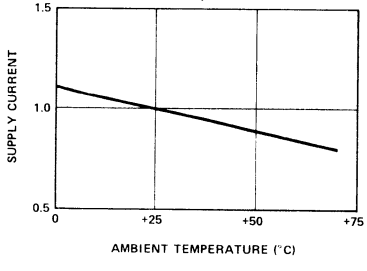
CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

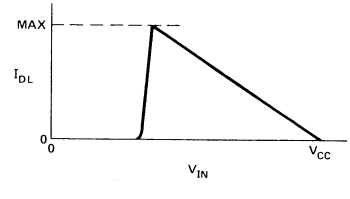
Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED.[3]



DATA BUS CHARACTERISTIC DURING DBIN



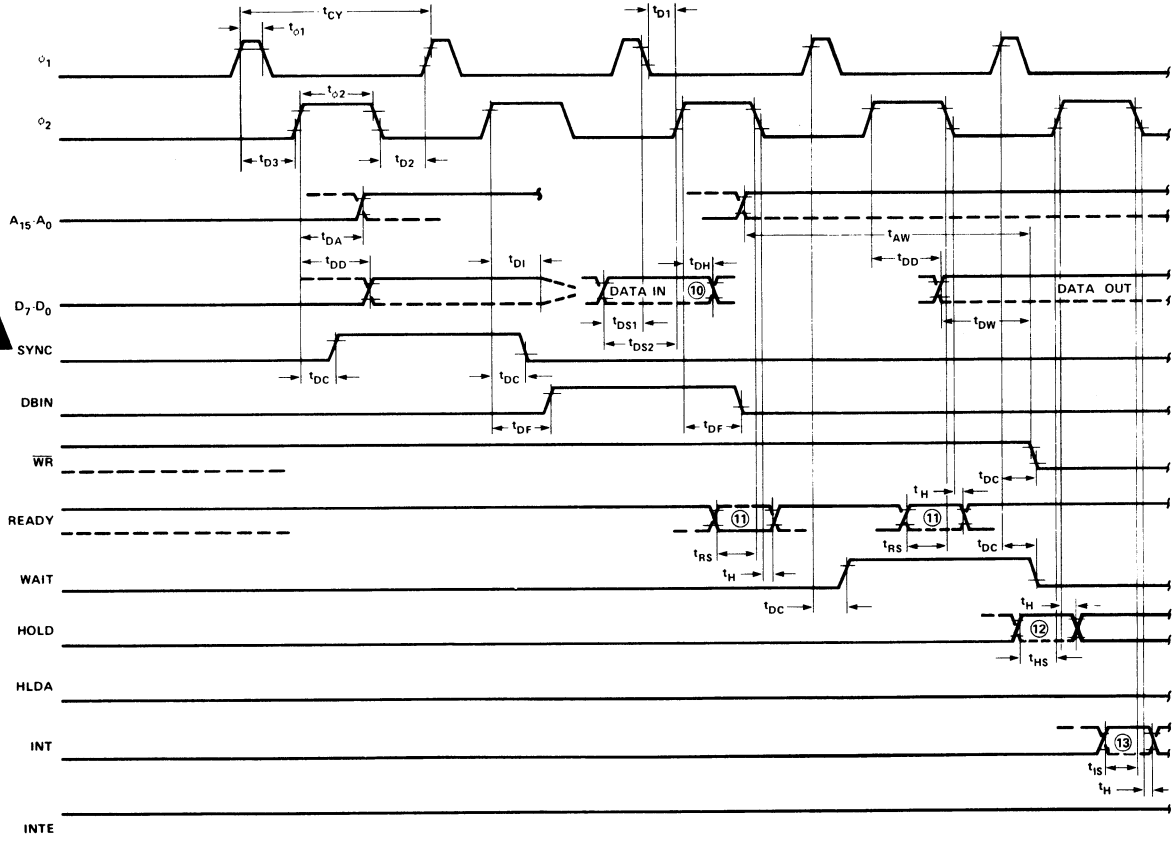
A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	0.48	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	70		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		nsec	
t_{DA} [2]	Address Output Delay From ϕ_2		200	nsec	C_L = 100pf
t_{DD} [2]	Data Output Delay From ϕ_2		220	nsec	C_L = 100pf
t_{DC} [2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		120	nsec	C_L = 50pf
t_{DF} [2]	DBIN Delay From ϕ_2	25	140	nsec	C_L = 50pf
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		nsec	

TIMING WAVEFORMS[14]

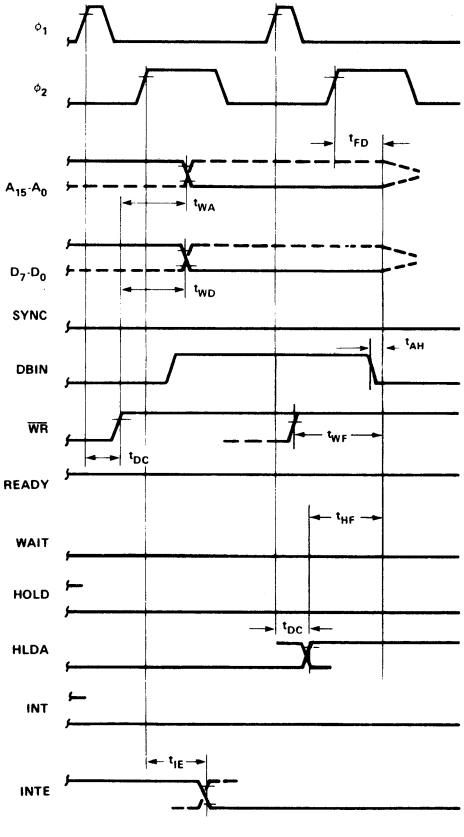
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



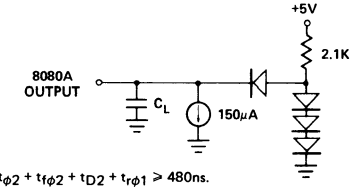
A.C. CHARACTERISTICS (Continued)

$T_A = 0°C$ to $70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	150		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	120		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	120		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L=100pf: Address, Data C_L=50pf: $\overline{WR}$, HLDA, DBIN
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	

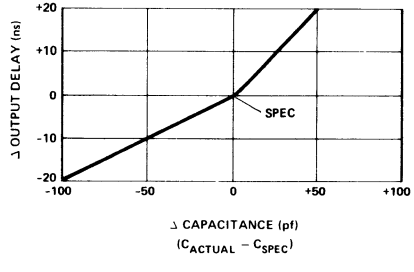


NOTES:
1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480ns$.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 140nsec$.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170nsec$.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10ns$. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50ns$.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10ns$
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080A instruction set.

The following special instruction group completes the 8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the 8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Immediate mode or I/O instructions

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

Jump, call or direct load and store instructions

For the 8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

8080 INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
MOVE, LOAD, AND STORE										
MOVr1,r2	Move register to register	0	1	D	D	D	S	S	S	5
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	11
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10

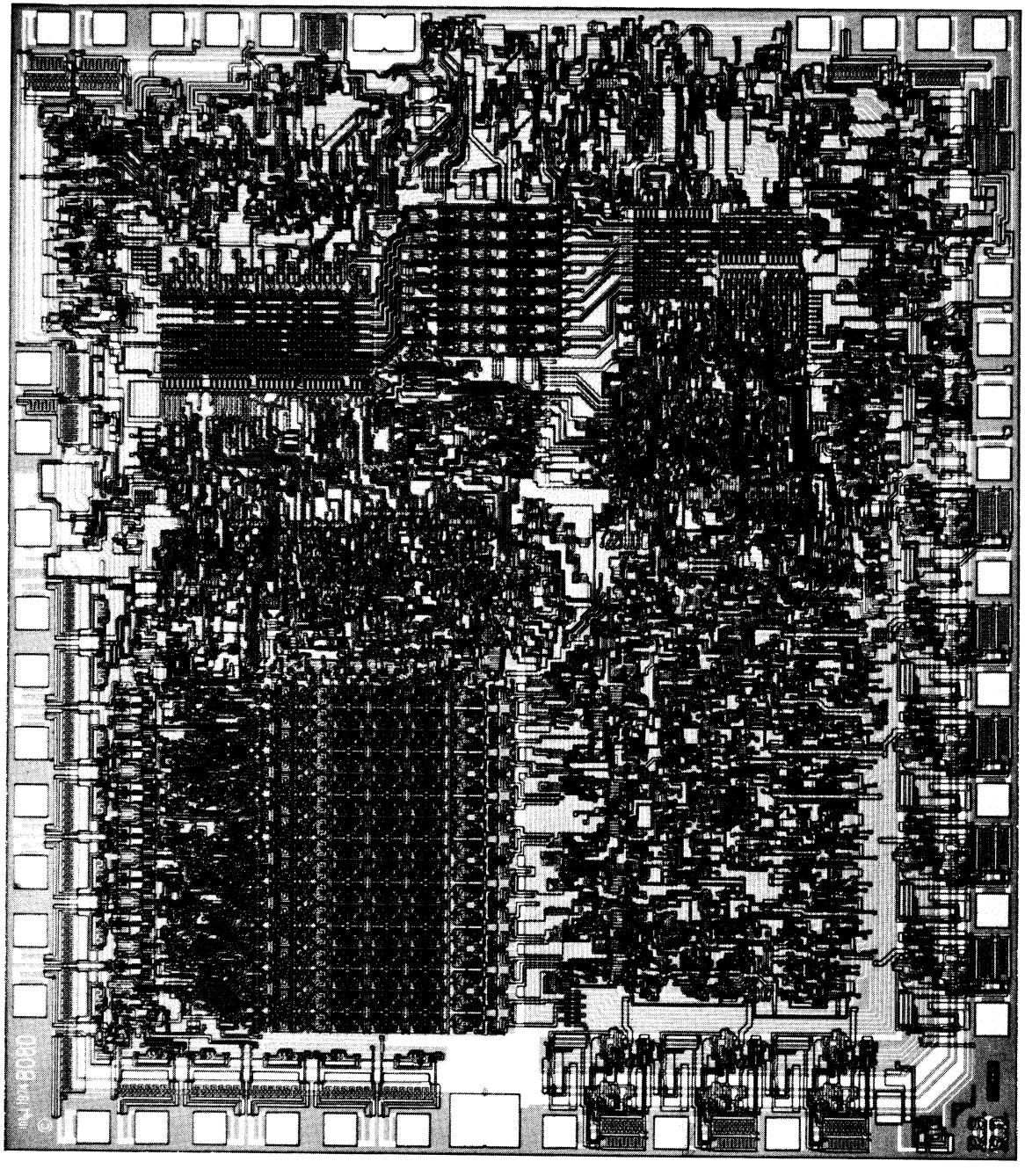
NOTES: 1. DDD or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.
2. Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.

8080 INSTRUCTION SET

Summary of Processor Instructions (Cont.)

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	7

NOTES: 1. DDD or SSS: B=000. C=001. D=010. E=011. H=100. L=101. Memory=110. A=111.
2. Two possible cycle times. (6/12) indicate instruction cycles dependent on condition flags.



8080A-1
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

- **TTL Drive Capability**
- **1.3 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

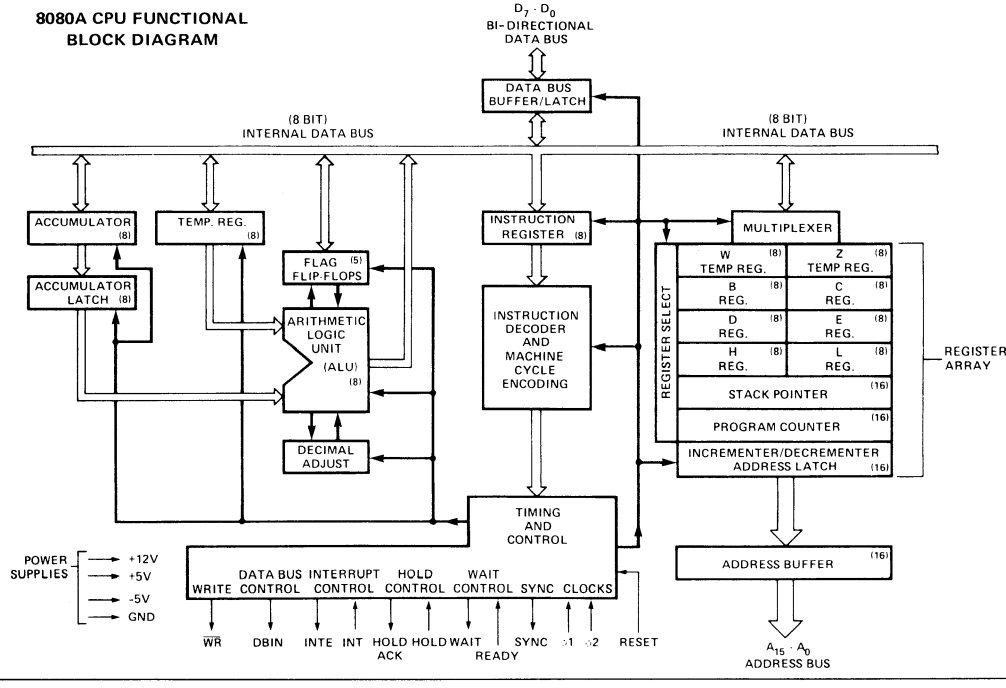
The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.

8080A CPU FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70° C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs, I_{OH} = 150μA.
V_{OH}	Output High Voltage	3.7			V	
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation T_{CY} = .32μsec
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}$ +0.8V V_{SS} +0.8V $\leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

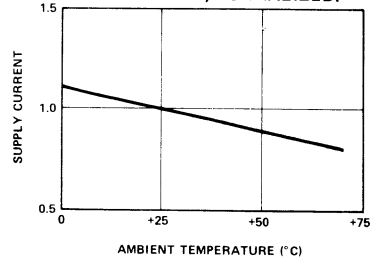
CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

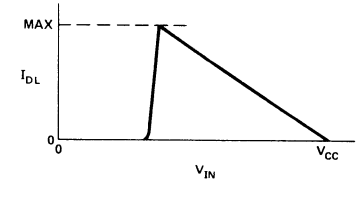
Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED. [3]



DATA BUS CHARACTERISTIC DURING DBIN



A.C. CHARACTERISTICS

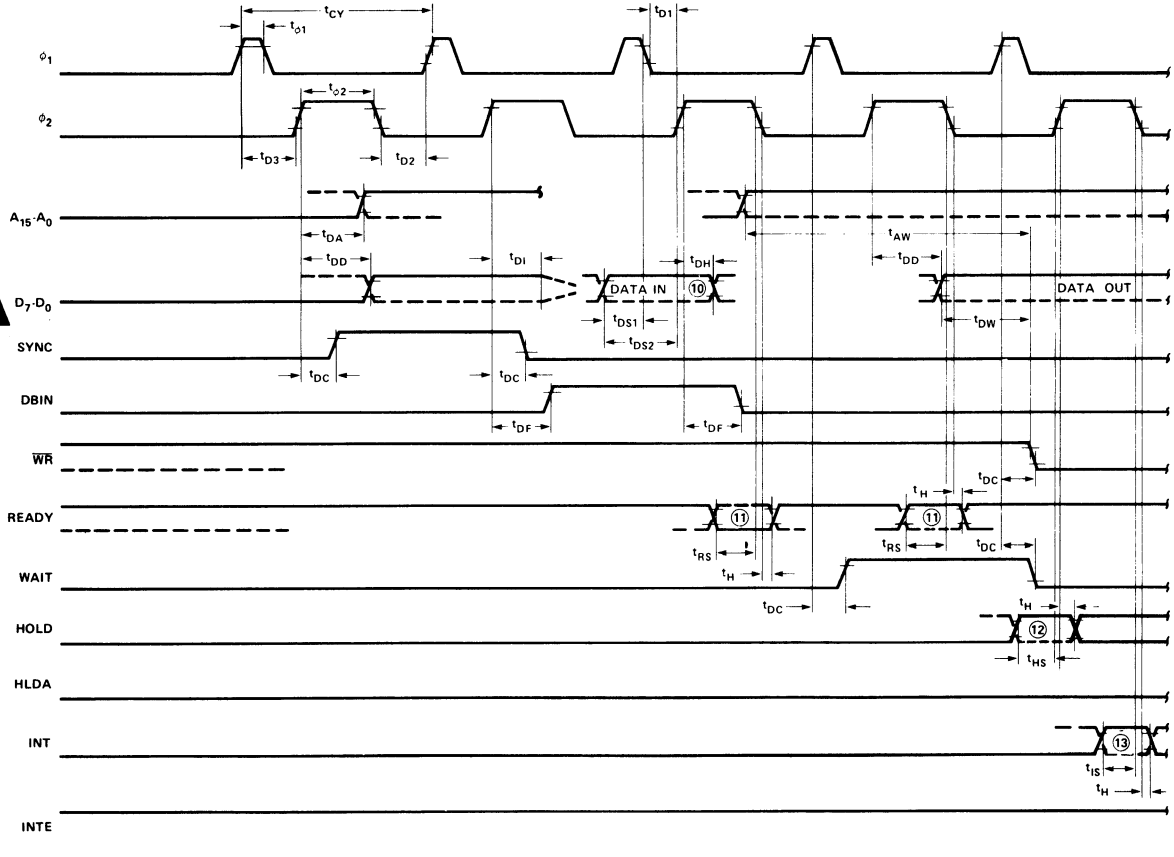
CAUTION: When operating the 8080A-1 at or near full speed, care must be taken to assure precise timing compatibility between 8080A-1, 8224 and 8228.

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	.32	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	25	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	50		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	145		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	60		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	60		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		150	nsec	C_L = 50pf
t_{DD}[2]	Data Output Delay From ϕ_2		180	nsec	
t_{DC}[2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		110	nsec	C_L = 50pf
t_{DF}[2]	DBIN Delay From ϕ_2	25	130	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	10		nsec	

TIMING WAVEFORMS[14]

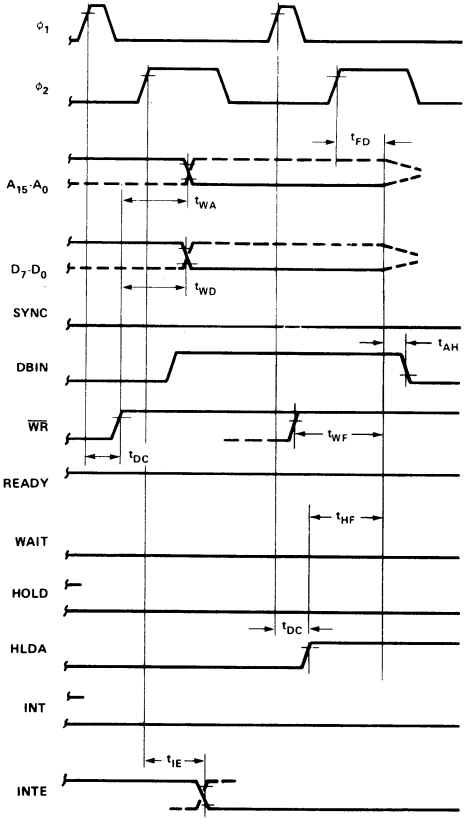
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



A.C. CHARACTERISTICS (Continued)

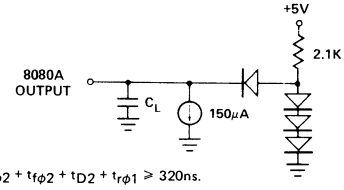
T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	120		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	90		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	120		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	100		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L = 50pf: Address, Data C_L=50pf: $\overline{WR}$, HLDA, DBIN
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	



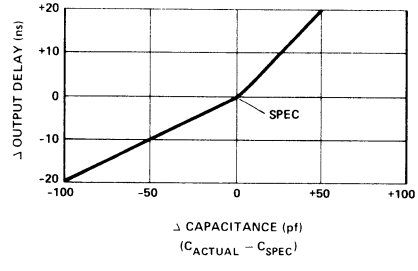
NOTES:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 320$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 110$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 150$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

8080A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

- **TTL Drive Capability**
- **1.5 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal,Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

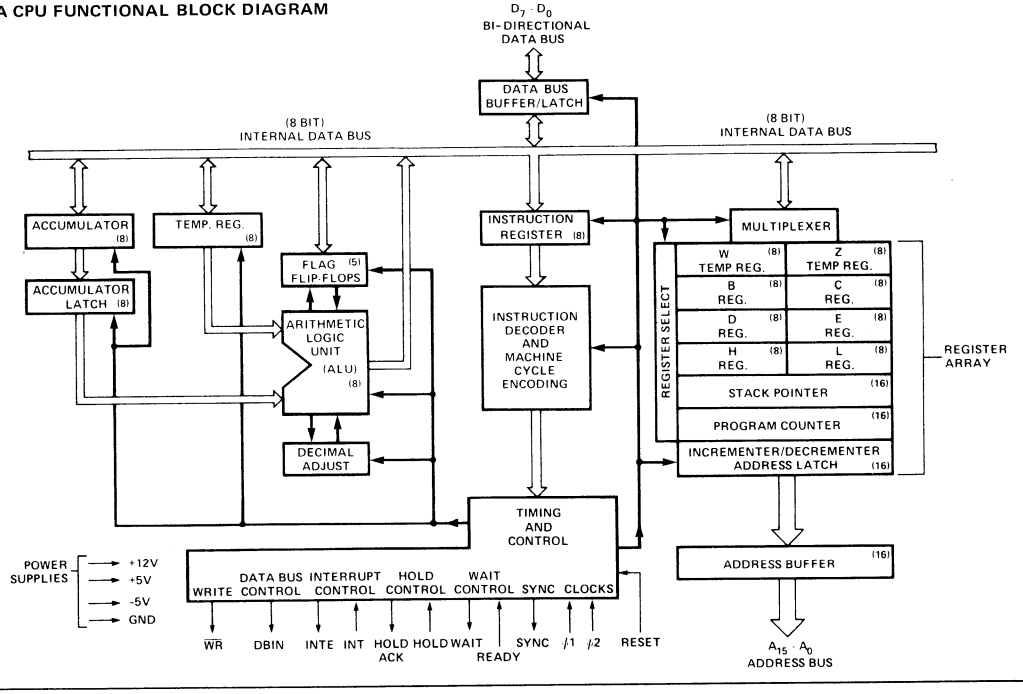
The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.

8080A CPU FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70° C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	T_{CY} = .38μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}$ +0.8V V_{SS} +0.8V $\leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

CAPACITANCE

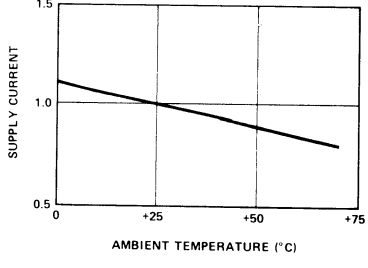
T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

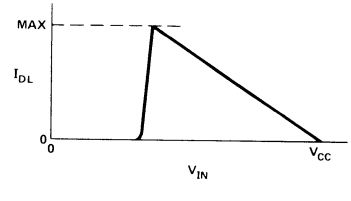
NOTES:

1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED. [3]



DATA BUS CHARACTERISTIC DURING DBIN



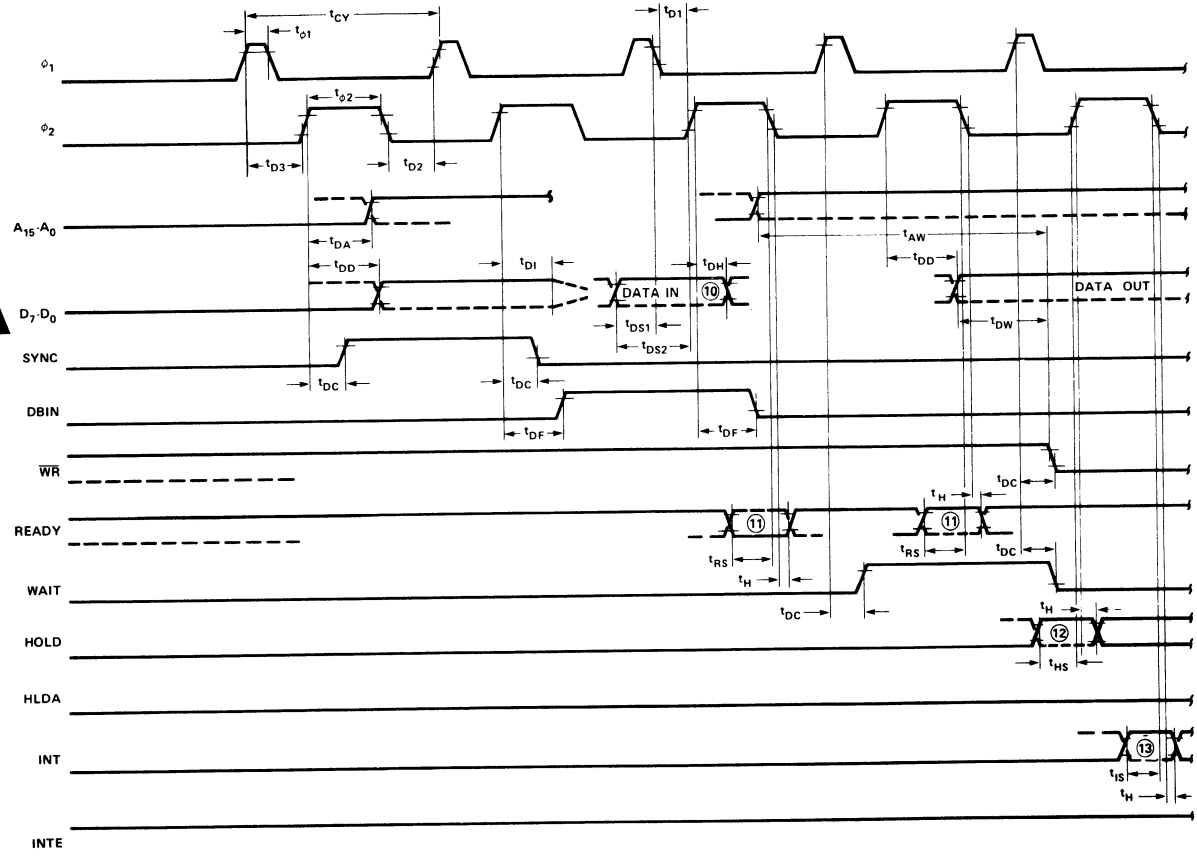
A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	.38	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	175		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	70		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	70		nsec	
t_{DA} [2]	Address Output Delay From ϕ_2		175	nsec	C_L = 100pf
t_{DD} [2]	Data Output Delay From ϕ_2		200	nsec	
t_{DC} [2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		120	nsec	C_L = 50pf
t_{DF} [2]	DBIN Delay From ϕ_2	25	140	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	20		nsec	

TIMING WAVEFORMS[14]

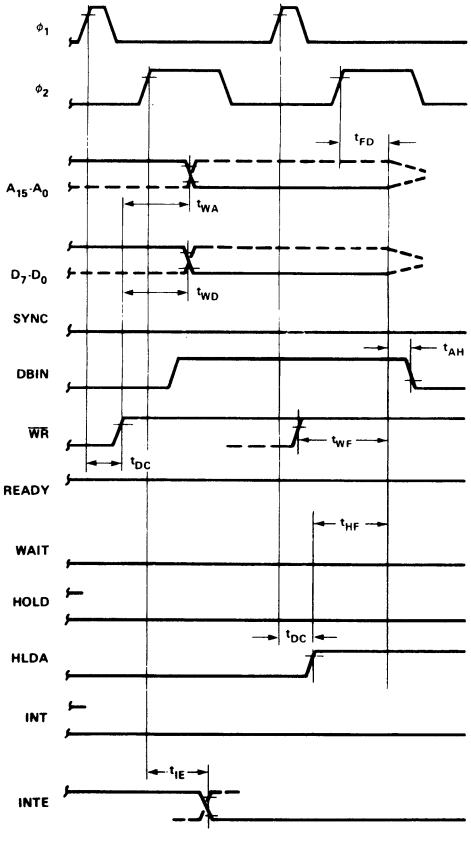
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



A.C. CHARACTERISTICS (Continued)

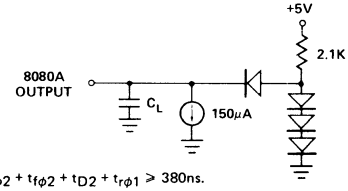
T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	130		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	90		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	120		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	100		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L=100pf: Address, Data C_L=50pf: $\overline{WR}$, HLDA, DBIN
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	



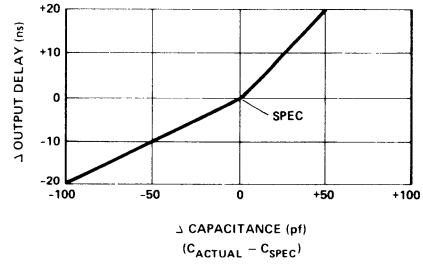
NOTES:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 380$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 130$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

MILITARY TEMP.

M8080A

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The M8080A is functionally compatible with the Intel® 8080.

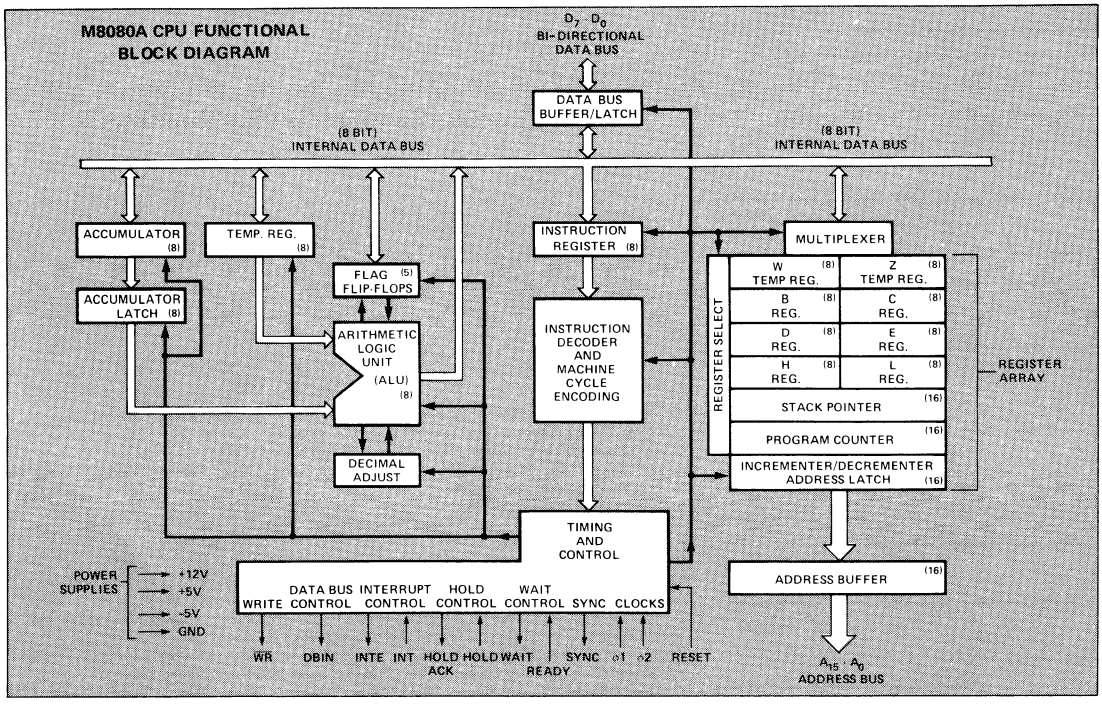
- **Full Military Temperature Range −55°C to +125°C**
- **±10% Power Supply Tolerance**
- **2 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **Six General Purpose Registers and an Accumulator**
- **Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**
- **TTL Drive Capability**

The Intel® M8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The M8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The M8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the M8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the M8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.



MCS 80/85

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.7W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	8.5		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs, I_{OH} = 150μA.
V_{OH}	Output High Voltage	3.7			V	
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		50	80	mA	Operation T_{CY} = .48 μsec
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	100	mA	
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leq V_{IN} \leq V_{SS}+0.8V$ $V_{SS}+0.8V \leq V_{IN} \leq V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

CAPACITANCE

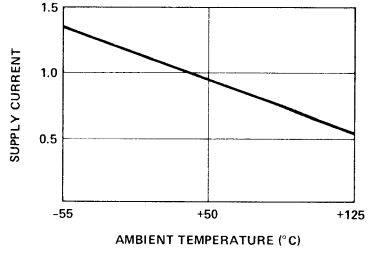
T_A = 25°C $V_{CC} = V_{DD} = V_{SS} = 0V$, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

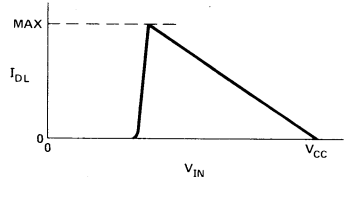
NOTES:

1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED. [3]



DATA BUS CHARACTERISTIC DURING DBIN



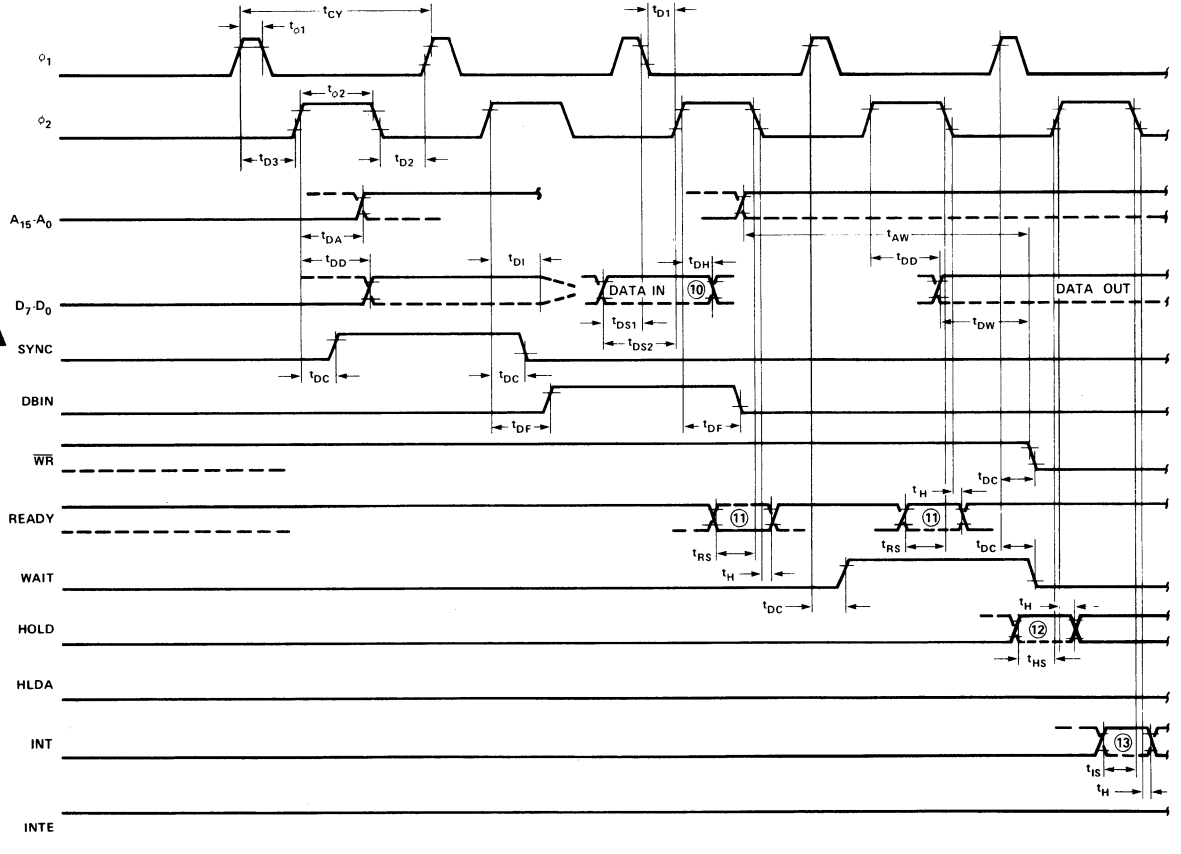
A.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	0.48	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	80		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{DD}[2]	Data Output Delay From ϕ_2		220	nsec	
t_{DC}[2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		140	nsec	
t_{DF}[2]	DBIN Delay From ϕ_2	25	150	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		nsec	

TIMING WAVEFORMS[14]

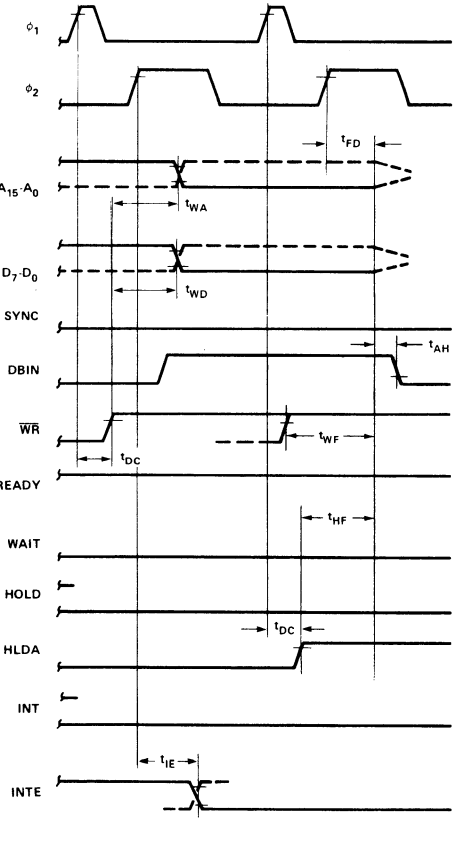
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 7.0V, "0" = 1.0V; INPUTS "1" = 3.0V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



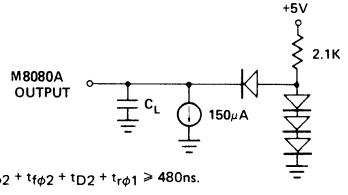
A.C. CHARACTERISTICS (Continued)

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	130		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	120		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		nsec	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	120		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		130	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L = 50pf
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	

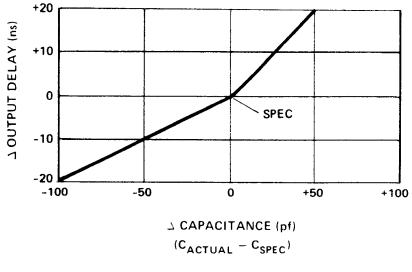


NOTES:
1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the M8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the M8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the M8080A instruction set.

The following special instruction group completes the M8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the M8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Immediate mode or I/O instructions

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

Jump, call or direct load and store instructions

For the M8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

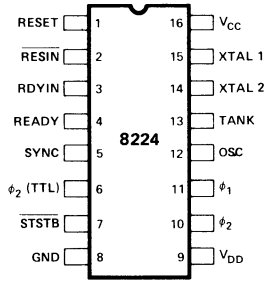
- **Single Chip Clock Generator/Driver for 8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**

The 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

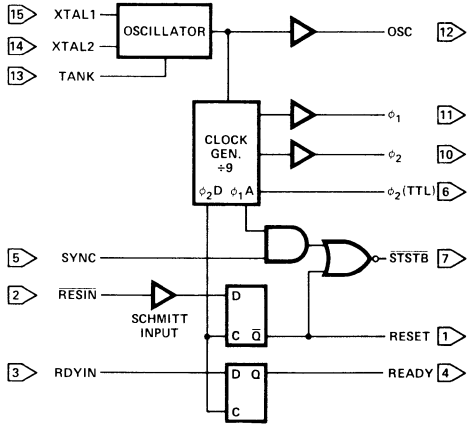
Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
φ1	8080 CLOCKS
φ2	8080 CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
φ2 (TTL)	φ2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . . −0.5V to +7V
Supply Voltage, V_{DD} . . . . . −0.5V to +13.5V
Input Voltage . . . . . −1.5V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = +5.0V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_F	Input Current Loading			-.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.25V
V_C	Input Forward Clamp Voltage			1.0	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.6 2.0			V	Reset Input All Other Inputs
V_{IH}-V_{IL}	RESIN Input Hysteresis	.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage			.45 .45	V V	(ϕ_1,ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} =2.5mA All Other Outputs I_{OL} = 15mA
V_{OH}	Output "High" Voltage ϕ_1 , ϕ_2 READY, RESET All Other Outputs	 9.4 3.6 2.4			 V V V	 I_{OH} = -100μA I_{OH} = -100μA I_{OH} = -1mA
I_{SC}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

CRYSTAL REQUIREMENTS

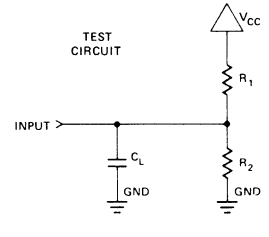
Tolerance: .005% at 0°C -70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Typ.) : 4mW

*With tank circuit use 3rd overtone mode.

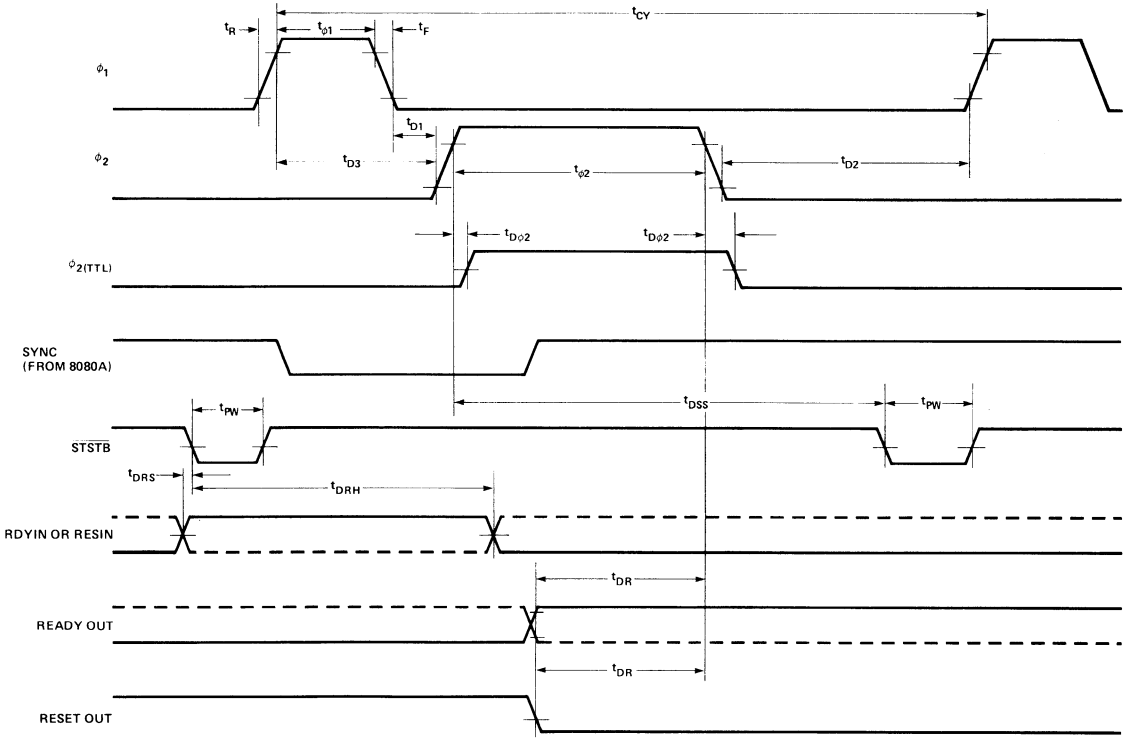
A.C. CHARACTERISTICS

V_{CC} = +5.0V ± 5%; V_{DD} = +12.0V ± 5%; T_A = 0°C to 70°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9}$ - 20ns			ns	C_L = 20pF to 50pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9}$ - 35ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9}$ - 14ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9}$ + 20ns		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2TTL,CL=30 R_1=300Ω R_2=600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9}$ - 30ns		$\frac{6tcy}{9}$		
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9}$ - 15ns				$\overline{STSTB}$, CL=15pF R_1 = 2K R_2 = 4K
t_{DRS}	RDYIN Setup Time to Status Strobe	50ns - $\frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	$\frac{4tcy}{9}$ - 25ns				Ready & Reset CL=10pF R_1=2K R_2=4K
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency			27	MHz	
C_{in}	Input Capacitance			8	pF	V_{CC}=+5.0V V_{DD}=+12V V_{BIAS}=2.5V f=1MHz



WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

EXAMPLE:

A.C. CHARACTERISTICS (For t_{CY} = 488.28 ns)

T_A = 0°C to 70°C; V_{DD} = +5V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY}=488.28ns
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	Ready & Reset Loaded to 2mA/10pF
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5V unless specified otherwise.
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	

M8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

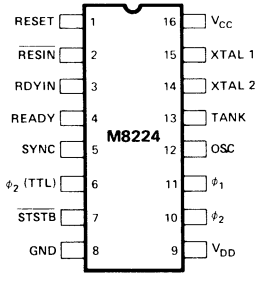
- **Single Chip Clock Generator/Driver for M8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Full Military Temperature Range -55°C to +125°C**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**

The M8224 is a single chip clock generator/driver for the M8080A CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

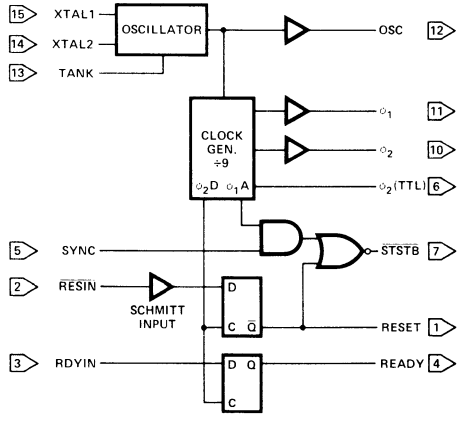
Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The M8224 provides the designer with a significant reduction of packages used to generate clocks and timing for M8080A.

PIN CONFIGURATION



M8224 BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
φ1	8080 CLOCKS
φ2	8080 CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
φ2 (TTL)	φ2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Supply Voltage, V_{CC}	-0.5V to +7V
Supply Voltage, V_{DD}	-0.5V to +13.5V
Input Voltage	-1.0V to +7V
Output Current	100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to 125°C; V_{CC} = +5.0V ±10%; V_{DD} = +12V ±10%.

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_F	Input Current Loading			-.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.5V
V_C	Input Forward Clamp Voltage			-1.2	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage $\overline{RESIN}$ All Other Inputs	2.6 2.0			V	
V_{IH}-V_{IL}	$\overline{RESIN}$ Input Hysteresis	.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage OSC, ϕ2 (TTL) All Other Outputs			.45 .45	V V	I_{OL} = 10mA I_{OL} = 2.5mA
V_{OH}	Output "High" Voltage ϕ_1 , ϕ_2 READY, RESET OSC, ϕ2 (TTL), $\overline{STSTB}$	 9.0 3.3 2.4			 V V V	 I_{OH} = -100μA I_{OH} = -100μA I_{OH} = -1mA
I_{OS}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

CRYSTAL REQUIREMENTS

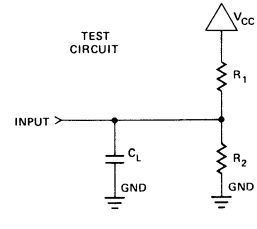
Tolerance: .005% at -55°C to 125°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With tank circuit use 3rd overtone mode.

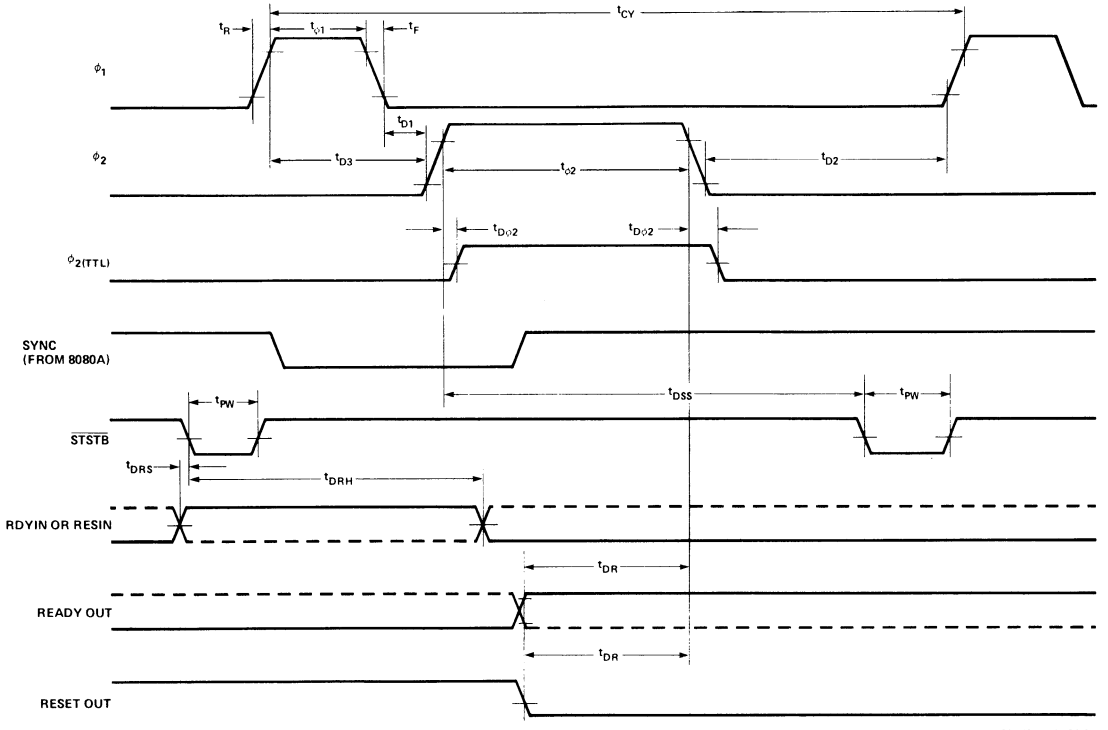
A.C. CHARACTERISTICS

V_{CC} = +5.0 ±10%; V_{DD} = +12.0V ±10%; T_A = -55°C to +125°C

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9}$ - 20ns			ns	C_L = 20pF to 50pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9}$ - 45ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9}$ - 25ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9}$ + 40ns		
t_R	ϕ_1 and ϕ_2 Rise Time			25		
t_F	ϕ_1 and ϕ_2 Fall Time			25		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2TTL,CL=30pF R_1=300Ω R_2=600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9}$ - 30ns		$\frac{6tcy}{9}$		$\overline{STSTB}$, CL=15pF R_1 = 2K R_2 = 4K
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9}$ - 23ns				
t_{DRS}	RDYIN Setup Time to Status Strobe	50ns - $\frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	READY or RESET to ϕ_2 Delay	$\frac{4tcy}{9}$ - 25ns				CL=10pF R_1=2K R_2=4K
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency	27			MHz	
C_{in}	Input Capacitance			8	pF	V_{CC}=+5.0V V_{DD}=+12V V_{BIAS}=2.5V f=1MHz



WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 7.0V. READY, RESET Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

Example:

A.C. CHARACTERISTICS (For t_{CY} = 488.28 ns.)

T_A = -55°C to 125°C; V_{DD} = +5V ±10%; V_{DD} = +12V ±10%.

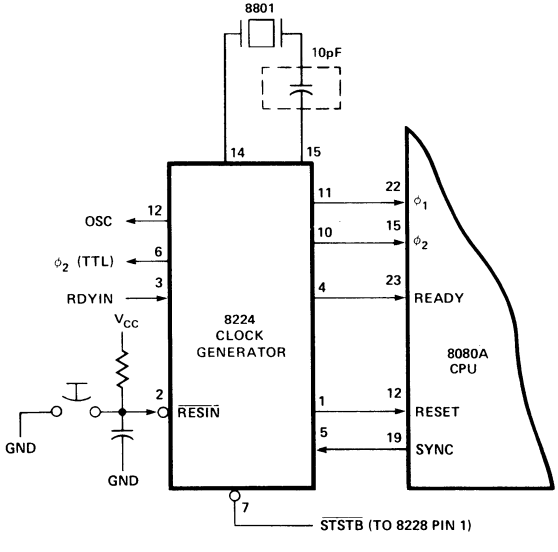
Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY}=488.28ns
$t_{\phi 2}$	ϕ_2 Pulse Width	226			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	84			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		149	ns	
t_r	Output Rise Time			25	ns	
t_f	Output Fall Time			25	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	31			ns	Ready & Reset Loaded to 2mA/10pF
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5V unless specified otherwise.
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	

8801
CLOCK GENERATOR CRYSTAL FOR 8224/8080A

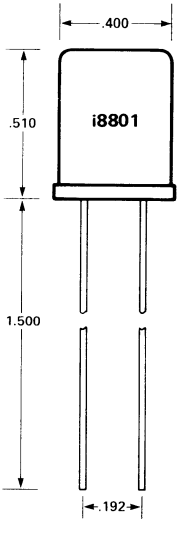
- **Specifically Selected For Intel® 8224**
- **18.432 MHz for 1.95 µs 8080A Cycle**
- **Simple Generation of All Standard Communication Baud Rates**
- **Frequency Deviation ±.005%**
- **Frequency Mode-Fundamental**
- **0 - 70° C Operating Temperature**

The 8801 is a quartz crystal specifically selected to operate with the 8224 clock generator and 8080A. It resonates in the fundamental frequency mode at 18.432 MHz. This frequency allows the 8080A at full speed (T_{CY} = 488 ns) to have a cycle of 1.95 µs and also simplifies the generation of all standard communication baud rates. The 8801 crystal is exactly matched to the requirements of the 8080A/8224 and provides both high-performance and system flexibility for the microcomputer designer.

8801 INTERFACE



PACKAGING INFORMATION

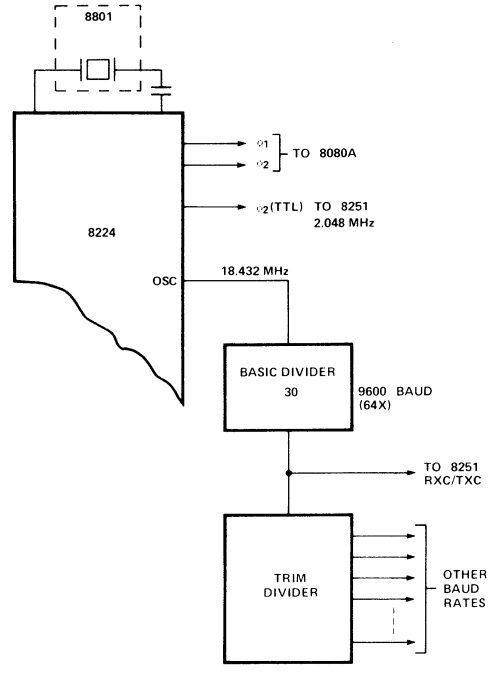


APPLICATIONS

The selection of 18.432 MHz provides the 8080A with clocks whose period is 488ns. This allows the 8080A to operate at very close to its maximum specified speed (480 ns). The 8224, when used with the 8801, outputs a signal on its OSC pin that is an approximately symetrical square wave at a frequency of 18.432 MHz. This frequency signal can be easily divided down to generate an accurate, stable baud rate clock that can be connected directly to the transmitter or receiver clocks of the 8251 USART. This feature allows the designer to support most standard communication interfaces with a minimum of extra hardware.

The chart below (Fig. 1) shows the equivalent baud rates that are generated with the corresponding dividers.

BLOCK DIAGRAM



BAUD RATE 64x	BAUD RATE 16x	FREQUENCY	BASIC DIVIDER	PLUS TRIM DIVIDER
9600		614.4 KH	÷30	–
4800	19.2K	307.2 KH	÷30	÷2
2400	9600	153.6 KH	÷30	÷4
1200	4800	76.8 KH	÷30	÷8
600	2400	38.4 KH	÷30	÷16
300	1200	19.2 KH	÷30	÷32
	600	9.6 KH	÷30	÷64
	300	4.8 KH	÷30	÷128
*109.1		6.982 KH	÷30	÷88

*For 109.1 (64x) Baud rate divide 1200 Baud Frequency (76.8 KH) by 11.

Figure 1. Baud Rate Chart

ELECTRICAL CHARACTERISTICS

Recommended Drive Level	5mW
Type of Resonance	Series
Equivalent Resistance	20 ohms
Maximum Shunt Capacity	7pF
Maximum Frequency Deviation	
0° – 70°C	±.005%
-55°– 125°C	±.002%

ORDERING INFORMATION

Intel Products may be ordered from either your local Intel sales office or stocking Intel distributor.

8228/8238
SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- **Single Chip System Control for MCS-80™ Systems**
- **Built-in Bi-Directional Bus Driver for Data Bus Isolation**
- **Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28 Pin Dual In-Line Package**
- **Reduces System Package Count**
- ***8238 Has Advanced $\overline{IOW}$/$\overline{MEMW}$ for Large System Timing Control**

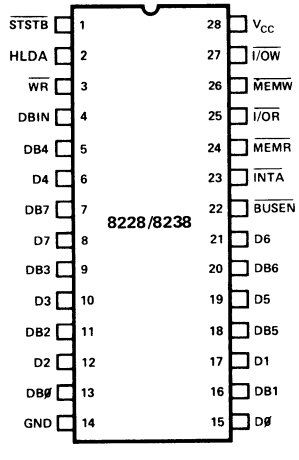
The 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems deisgner to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

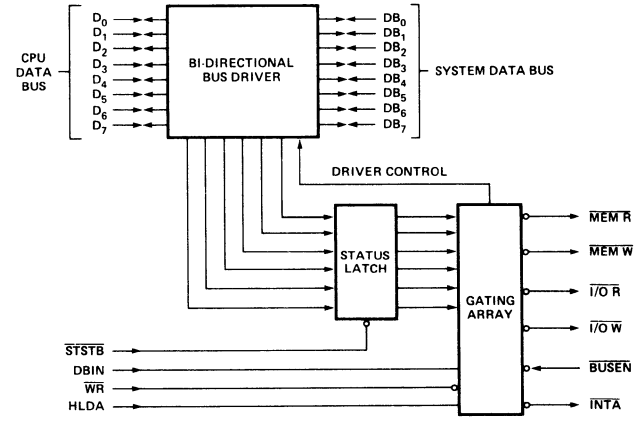
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



8228/8238 BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
$\overline{I/OR}$	I/O READ	$\overline{WR}$	WR (FROM 8080)
$\overline{I/OW}$	I/O WRITE	$\overline{BUSEN}$	BUS ENABLE INPUT
$\overline{MEMR}$	MEMORY READ	$\overline{STSTB}$	STATUS STROBE (FROM 8224)
$\overline{MEMW}$	MEMORY WRITE	V_{CC}	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . . −0.5V to +7V
Input Voltage . . . . . −1.5V to +7V
Output Current 100mA

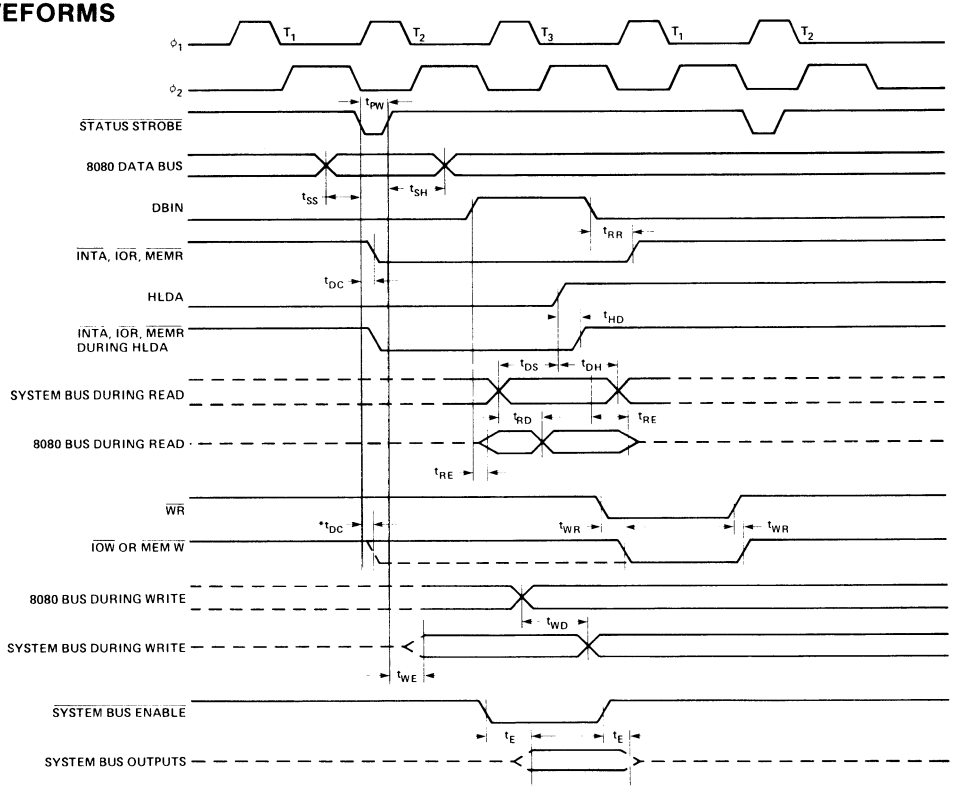
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = 5V ±5%.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		.75	-1.0	V	V_{CC}=4.75V; I_C=-5mA
I_F	Input Load Current, $\overline{STSTB}$			500	μA	V_{CC} = 5.25V
	D_2 & D_6			750	μA	V_F = 0.45V
	D_0, D_1, D_4, D_5, & D_7			250	μA	
	All Other Inputs			250	μA	
I_R	Input Leakage Current $\overline{STSTB}$			100	μA	V_{CC} = 5.25V
	DB_0-DB_7			20	μA	V_R = 5.25V
	All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		140	190	mA	V_{CC}=5.25V
V_{OL}	Output Low Voltage, D_0-D_7			.45	V	V_{CC}=4.75V; I_{OL}=2mA
	All Other Outputs			.45	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0-D_7	3.6	3.8		V	V_{CC}=4.75V; I_{OH}=-10μA
	All Other Outputs	2.4			V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15		90	mA	V_{CC}=5V
$I_{O(off)}$	Off State Output Current, All Control Outputs			100	μA	V_{CC}=5.25V; V_O=5.25
				-100	μA	V_O=.45V
I_{INT}	INTA Current			5	mA	(See Figure below)

Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*ADVANCED $\overline{IOW}$/$\overline{MEMW}$ FOR 8238 ONLY.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$.

Symbol	Parameter	Limits Min.	Limits Max.	Units	Condition
t_{PW}	Width of Status Strobe	22		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	60	ns	C_L = 100pF
t_{RR}	Delay from DBIN to Control Outputs		30	ns	C_L = 100pF
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	C_L = 25pF
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	C_L = 25pF
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	45	ns	C_L = 100pF
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	C_L = 100pF
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	C_L = 100pF
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7		30	ns	C_L = 100pF
t_{HD}	HLDA to Read Status Outputs		25	ns	
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	C_L = 100pF

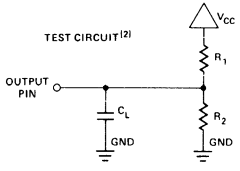
CAPACITANCE

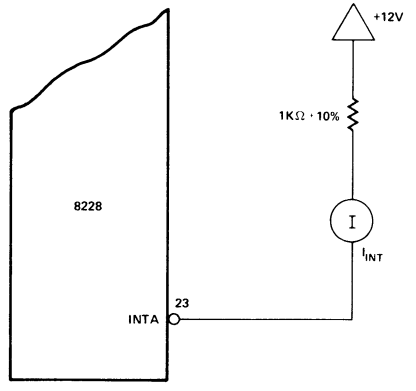
This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

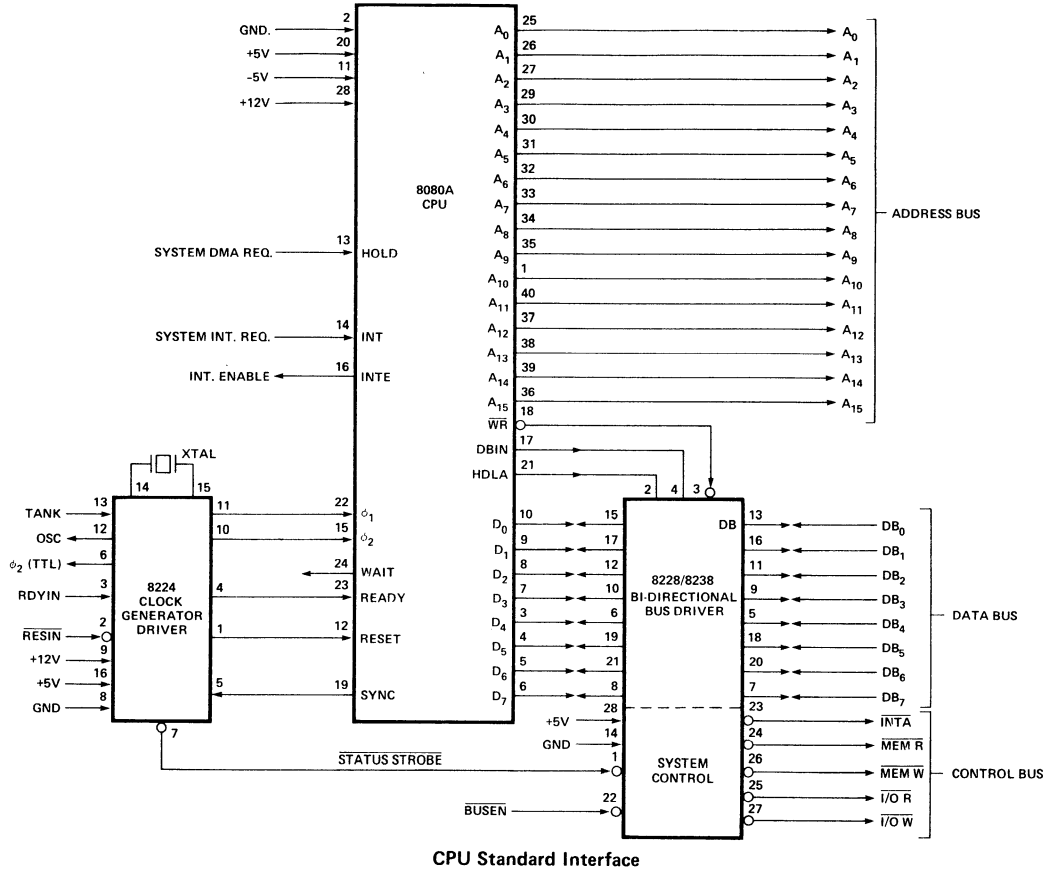
TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, f = 1MHz.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.





INTA Test Circuit (for RST 7)



CPU Standard Interface

MILITARY TEMP.

M8228/M8238
SYSTEM CONTROLLER AND BUS DRIVER FOR M8080A CPU

- **Single Chip System Control for MCS™-80 Systems**
- **Built-in Bi-Directional Bus Driver for Data Bus Isolation**
- **Allows the use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **M8238 has Advanced $\overline{IOW}$/$\overline{MEMW}$ for Large System Timing Control**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28 Pin Dual In-Line Package**
- **Reduces System Package Count**
- **Full Military Temperature Range -55°C to +125°C**
- **±10% Power Supply Tolerance**

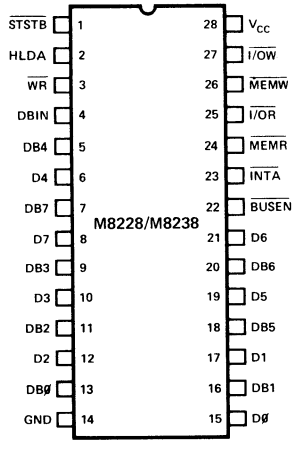
The M8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

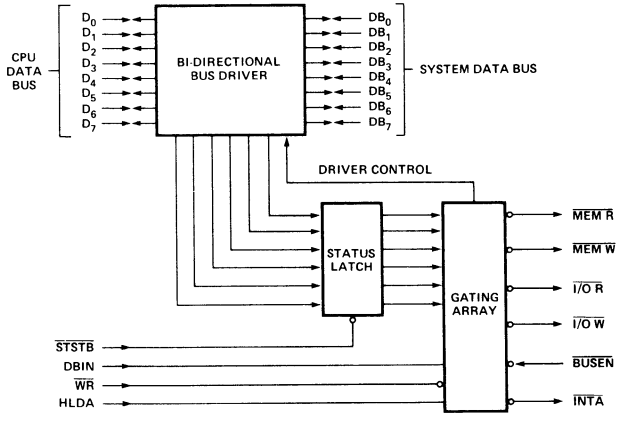
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The M8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the M8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The M8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



M8228/M8238 BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	$\overline{INTA}$	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
$\overline{I/OR}$	I/O READ	$\overline{WR}$	WR (FROM 8080)
$\overline{I/OW}$	I/O WRITE	$\overline{BUSEN}$	BUS ENABLE INPUT
$\overline{MEMR}$	MEMORY READ	$\overline{STSTB}$	STATUS STROBE (FROM 8224)
$\overline{MEMW}$	MEMORY WRITE	V_{CC}	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

MCS 80/85

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -55°C to 125°C
Storage Temperature . . . . . -65°C to 150°C
Supply Voltage, V_{CC} . . . . . -0.5V to +7V
Input Voltage . . . . . -1.0V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = -55°C to 125°C; V_{CC} = 5V ±10%.

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		-1.2	V	I_C = -5mA
I_F	Input Load Current, $\overline{STSTB}$		500	μA	V_F = 0.4V
	D_2, D_6		750	μA	
	D_0, D_1, D_4, D_5, D_7		250	μA	
	All Other Inputs		250	μA	
I_R	Input Leakage Current DB_0 - D_7		20	μA	V_R = 5.5V
	All Other Inputs		100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8	2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		210	mA	
V_{OL}	Output Low Voltage, D_0 - D_7		.5	V	I_{OL} = 2mA
	All Other Outputs		.5	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0 - D_7	3.3		V	I_{OH} = -10μA
	All Other Outputs	2.4		V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15	90	mA	V_{CC} = 5V
$I_{O\ (Off)}$	Off State Output Current, All Controls Outputs		100	μA	V_O = 5.5V
			-100	μA	V_O = .45V
I_{INT}	$\overline{INTA}$ Current		5	mA	(See Figure on page 3)

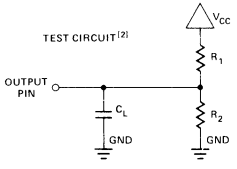
Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

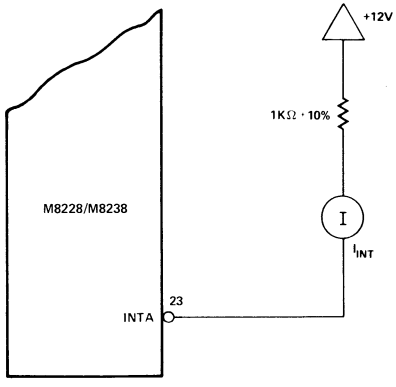
CAPACITANCE This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, f = 1MHz.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.



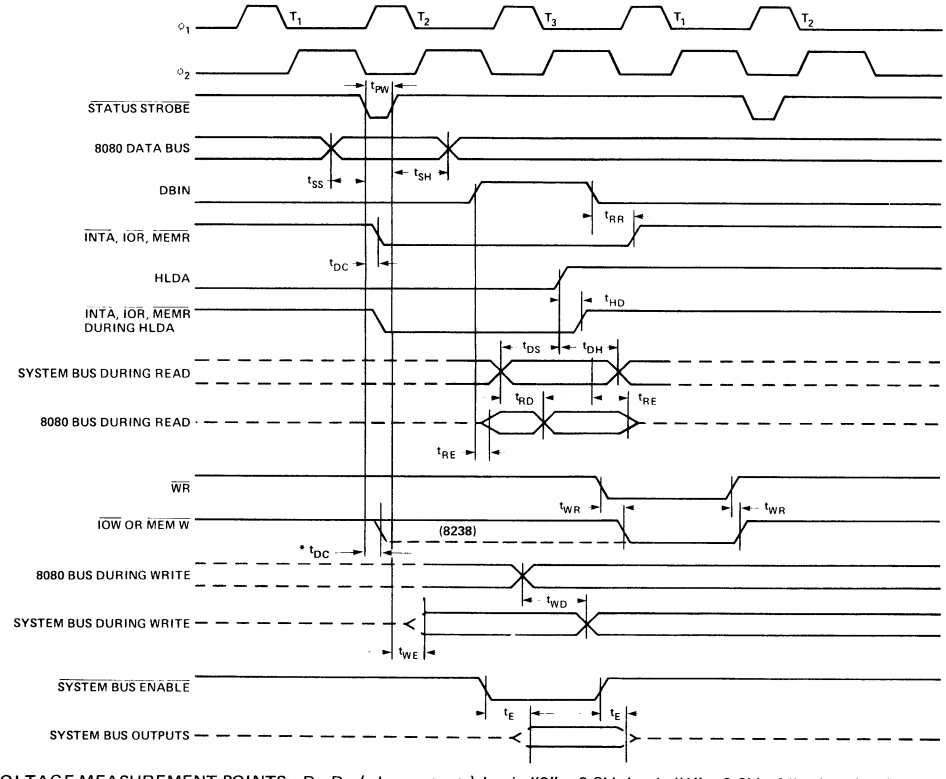


INTA Test Circuit (for RST 7)

A.C. CHARACTERISTICS T_A = -55°C to 125°C; V_{CC} = 5V ±10%.

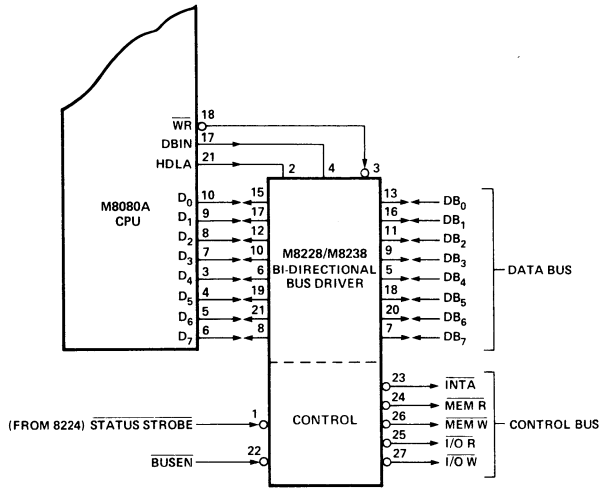
Symbol	Parameter	Limits Min.	Max.	Units	Condition
t_{PW}	Width of Status Strobe	25		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	75	ns	C_L = 100pF
t_{RR}	Delay from DBIN to Control Outputs		30	ns	C_L = 100pF
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	C_L = 25pF
t_{RD}	Delay from System Bus to 8080 Bus during Read		45	ns	C_L = 25pF
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	60	ns	C_L = 100pF
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	C_L = 100pF
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	C_L = 100pF
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7		30	ns	C_L = 100pF
t_{HD}	HLDA to Read Status Outputs		25	ns	C_L = 100pF
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*Advanced $\overline{IOW}/\overline{MEMW}$ for M8238 only.



M8080A CPU Interface

TYPE OF MACHINE CYCLE

	DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE	HALT ACKNOWLEDGE	INTERRUPT ACKNOWLEDGE WHILE HALT
			①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
D_0	INTA	0	0	0	0	0	0	0	1	0	1	
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	1	1	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	
D_5	M_1	1	0	0	0	0	0	0	1	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	
D_7	MEMR	1	1	0	1	0	0	0	0	1	0	

Ⓝ STATUS WORD

CONTROL SIGNALS:
- ⑩ $\overline{INTA}$
- ⑨ (NONE)
- ⑧ $\overline{INTA}$
- ⑦ $\overline{I/O\ W}$
- ⑥ $\overline{I/O\ R}$
- ⑤ $\overline{MEM\ W}$
- ④ $\overline{MEM\ R}$
- ③ $\overline{MEM\ W}$
- ② $\overline{MEM\ R}$
- ① $\overline{MEM\ R}$

Status Word Chart

8085

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

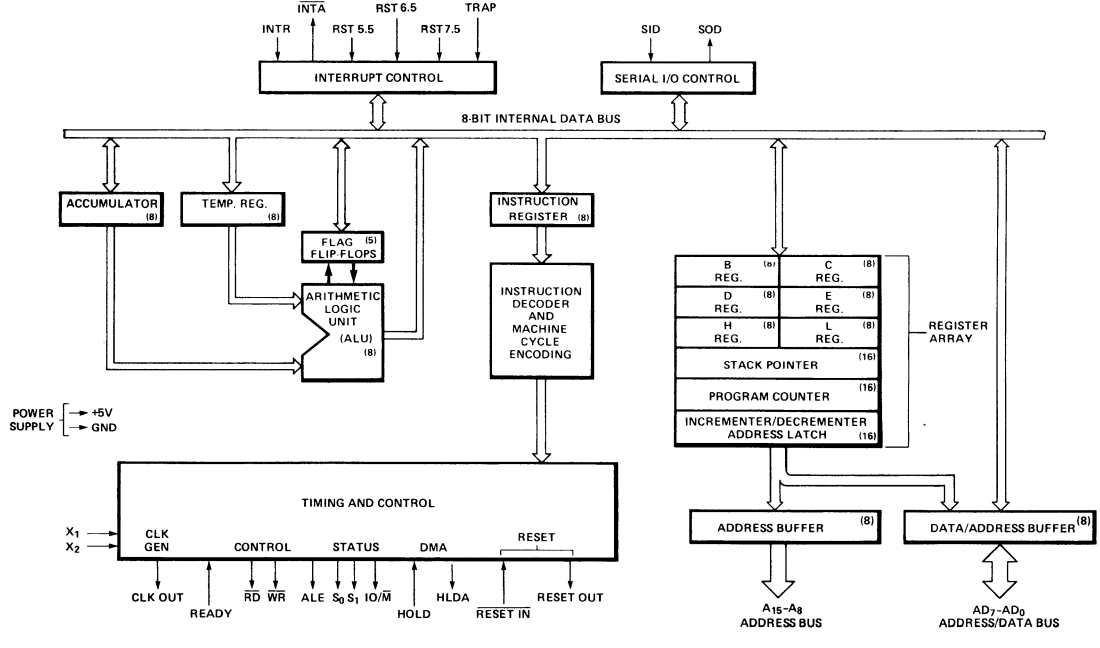
- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3 μs Instruction Cycle**
- **On-Chip Clock Generator (with External Crystal or RC Network)**
- **On-Chip System Controller**
- **Four Vectored Interrupts (One is non-Maskable)**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64K Bytes of Memory**

The Intel® 8085 is a new generation, complete 8 bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's: 8085 (CPU), 8155 (RAM) and 8355/8755 (ROM/PROM).

The 8085 incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080, thereby offering a high level of system integration.

The 8085 uses a multiplexed Data Bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8355/8755 memory products allows a direct interface with 8085.

8085 CPU FUNCTIONAL BLOCK DIAGRAM



8085 FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

A_8-A_{15} (Output 3-State)

Address Bus; The most significant 8-bits of the memory address or the 8-bits of the I/O address, 3-stated during Hold and Halt modes.

AD_{0-7} (Input/Output 3-state)

Multiplexed Address/Data Bus; Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus during the second and third clock cycles.

3-stated during Hold and Halt modes.

ALE (Output 3-state)

Address Latch Enable: It occurs during the first clock cycle of a machine state and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. ALE can also be used to strobe the status information. 3-stated during Hold and Halt modes.

So, S1 (Output)

Data Bus Status. Encoded status of the bus cycle:

S_1	S_0	
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

S_1 can be used as an advanced R/$\overline{W}$ status.

$\overline{RD}$ (Output 3-state)

READ; indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. Tri-stated during Hold and Halt.

$\overline{WR}$ (Output 3-state)

WRITE; indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. Tri-stated during Hold and Halt modes.

READY (Input)

If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

HOLD (Input)

HOLD; indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request, will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue. The processor can regain the buses only after the Hold is removed. When the Hold is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, and ALE lines are tri-stated.

HLDA (Output)

HOLD ACKNOWLEDGE; indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycle after HLDA goes low.

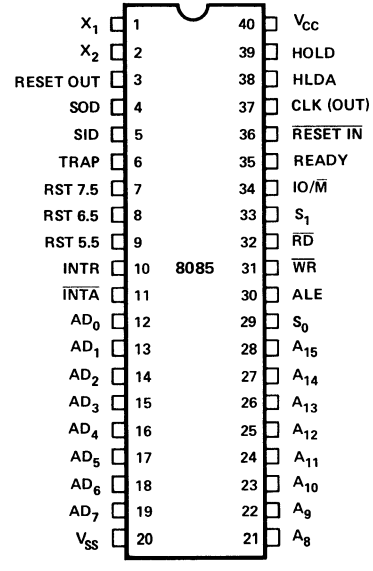


Figure 1. 8085 PINOUT DIAGRAM

INTR (Input)

INTERRUPT REQUEST; is used as a general purpose interrupt. It is sampled only during the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

$\overline{INTA}$ (Output)

INTERRUPT ACKNOWLEDGE; is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.

RST 5.5
RST 6.5
RST 7.5
(Inputs)

RESTART INTERRUPTS; These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

RST 7.5 → Highest Priority
RST 6.5
RST 5.5 → Lowest Priority

The priority of these interrupts is ordered as shown above. These interrupts have a higher priority than the INTR.

TRAP (Input)

Trap interrupt is a nonmaskable restart interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

$\overline{\text{RESET IN}}$ (Input)

Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as Reset is applied.

RESET OUT (Output)

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

X_1, X_2 (Input)

Crystal or R/C network connections to set the internal clock generator. X1 can also be an external clock input instead of a crystal.

CLK (Output)

Clock Output for use as a system clock when a crystal or R/C network is used as an input to the CPU.

IO/$\overline{\text{M}}$ (Output)

IO/$\overline{\text{M}}$ indicates whether the Read/Write is to memory or I/O. Tri-stated during Hold and Halt modes.

SID (Input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

SOD (output)

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

V_{CC}

+5 volt supply.

V_{SS}

Ground Reference.

FUNCTIONAL DESCRIPTION

The 8085 is a complete 8 bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz thus improving on the present 8080's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU, a RAM/IO, and a ROM or PROM/IO chip.

The 8085 uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first cycle the address is sent out. The lower 8-bits are latched into the peripherals by the Address Latch Enable (ALE). During the rest of the machine cycle the Data Bus is used for memory or I/O data.

The 8085 provides $\overline{\text{RD}}$, $\overline{\text{WR}}$, and IO/$\overline{\text{Memory}}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{\text{INTA}}$) is also provided. Hold, Ready, and all Interrupts are synchronized. The 8085 also provides serial input data (SID) and serial output data (SOD) lines for simple serial interface.

In addition to these features, the 8085 has three maskable, restart interrupts and one nonmaskable trap interrupt.

8085 vs. 8080

The 8085 includes the following features on-chip in addition to all of the 8080 functions.

a. Internal clock generator
b. Clock output
c. Fully synchronized Ready
d. Schmitt action on $\overline{\text{RESET IN}}$
e. RESET OUT pin
f. $\overline{\text{RD}}$, $\overline{\text{WR}}$, and IO/$\overline{\text{M}}$ Bus Control Signals
g. Encoded Status information
h. Multiplexed Address and Data
i. Direct Restarts and nonmaskable Interrupt
j. Serial Input/Output lines.

The internal clock generator requires an external crystal or R-C network. It will oscillate at twice the basic CPU operating frequency. A 50% duty cycle, two phase, nonoverlapping clock is generated from this oscillator internally and one phase of the clock ($\phi 2$) is available as an external clock. The 8085 directly provides the external RDY synchronization previously provided by the 8224. The $\overline{\text{RESET IN}}$ input is provided with a Schmitt action input so that power-on reset only requires a resistor and capacitor. RESET OUT is provided for System RESET.

The 8085 provides $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{M}}$ signals for Bus control. An $\overline{\text{INTA}}$ which was previously provided by the 8228 in 8080 system is also included in 8085.

STATUS INFORMATION

Status information is directly available from the 8085. *ALE serves as a status strobe.* The status is partially encoded, and provides the user with advanced timing of the type of bus transfer being done. IO/$\overline{\text{M}}$ cycle status signal is provided directly also. Decoded S_0, S_1 carries the following status information:

	S_1	S_0
HALT	0	0
WRITE	0	1
READ	1	0
FETCH	1	1

S1 can be interpreted as R/$\overline{\text{W}}$ in all bus transfers.

In the 8085 the 8 LSB of address are multiplexed with the data instead of status. The ALE line is used as a strobe to enter the lower half of the address into the memory or peripheral address latch. This also frees extra pins for expanded interrupt capability.

INTERRUPT AND SERIAL I/O

The 8085 has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080 INT. Each of three RESTART inputs, 5.5, 6.5, 7.5, has a programmable mask. TRAP is also a RESTART interrupt except it is a non-maskable interrupt.

The three RESTART interrupts cause the internal execution of RST (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RST independent of the state of the interrupt enable or masks.

Name	RESTART Address (Hex)
TRAP	24_{16}
RST 5.5	$2C_{16}$
RST 6.5	34_{16}
RST 7.5	$3C_{16}$

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive. For RST 7.5, only a pulse is required to set the interrupt request. The request is remembered until the request is serviced or reset by the SIM instruction or by RESET.

All the restart interrupts can be individually masked, and thus be prevented from interrupting the processor. The RST 7.5 request can be set even though the mask is set and the interrupts are disabled. The masks will only be affected by the SIM instruction and RESET.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP - highest priority, RST 7.5, RST 6.5, RST 5.5, INTR - lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt a RST 7.5 routine if the interrupts were re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic errors such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. TRAP must remain high to be acknowledged, but will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

BASIC SYSTEM TIMING

The 8085 has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 2 shows an instruction fetch, memory read and I/O write cycle (OUT). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

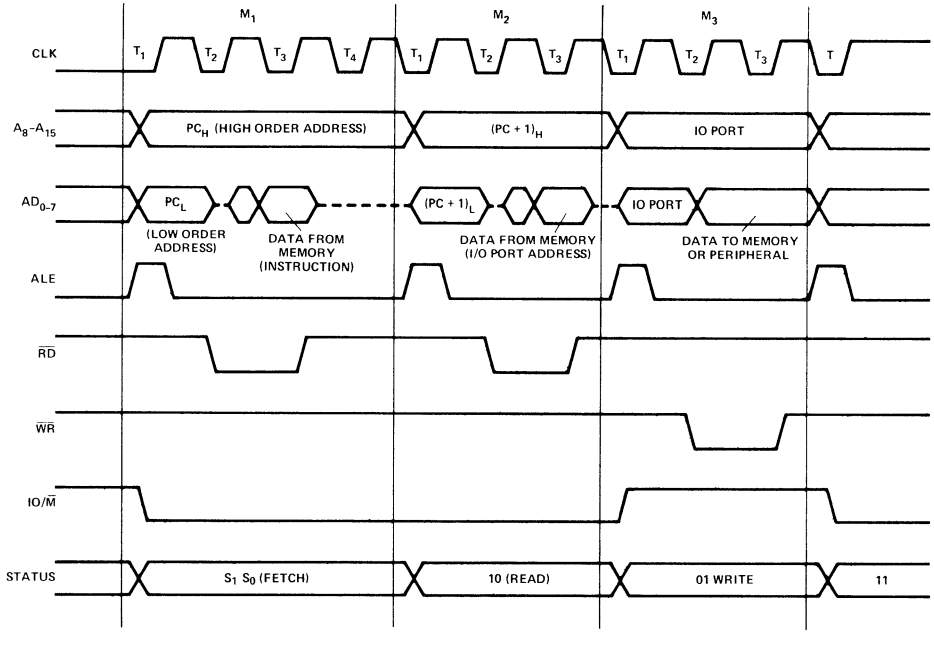


FIGURE 2. 8085 BASIC SYSTEM TIMING.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . -0.3 to +7V
Power Dissipation . . . . . 1.5 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{CC}	Power Supply Current		170	mA	
I_{IL}	Input Leakage		±10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \leqslant V_{out} \leqslant V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} +0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

Bus Timing Specification as a T_{CYC} Dependent

t_{AL}	–	(1/2) T - 50	MIN
t_{LA}	–	(1/2) T - 20	MIN
t_{LL}	–	(1/2) T - 40	MIN
t_{LCK}	–	(1/2) T - 50	MIN
t_{LC}	–	(1/2) T - 30	MIN
t_{AD}	–	(5/2 + N) T - 225	MAX
t_{RD}	–	(3/2 + N) T - 200	MAX
t_{RAE}	–	(1/2) T - 60	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T – 60	MIN
t_{WD}	–	(1/2) T - 80	MIN
t_{CC}	–	(3/2 + N) T - 80	MIN
t_{CL}	–	(1/2) T - 110	MIN
t_{ARY}	–	(3/2) T - 260	MAX
t_{HACK}	–	(1/2) T - 50	MIN
t_{HABF}	–	(1/2) T + 30	MAX
t_{HABE}	–	(1/2) T + 30	MAX
t_{AC}	–	(2/2) T - 50	MIN
t_1	–	(1/2) T - 80	MIN
t_2	–	(1/2) T - 40	MIN
t_{RV}	–	(3/2) T - 80	MIN
t_{INS}	–	(1/2) T + 200	MIN

NOTE: N is equal to the total WAIT states.
T = t_{CYC}.

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
T_{CYC}	CLK Cycle Period	320	2000	ns	See notes 1, 2, 3, 4, 5
t_1	CLK Low Time	80		ns	
t_2	CLK High Time	120		ns	
t_r, t_f	CLK Rise and Fall Time		30	ns	
t_{AL}	Address Valid Before Trailing Edge of ALE	110		ns	
t_{LA}	Address Hold Time After ALE	100		ns	
t_{LL}	ALE Width	120		ns	
t_{LCK}	ALE Low During CLK High	100		ns	
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		ns	
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0	ns	
t_{AD}	Valid Address to Valid Data In		575	ns	
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		280	ns	
t_{RDH}	Data Hold Time After $\overline{READ}$ ($\overline{INTA}$)	0		ns	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	120		ns	T_{CYC} = 320ns; C_L = 150 pF
t_{CA}	Address (A8–A15) Valid After Control	120		ns	
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		ns	
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	80		ns	
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	400		ns	
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		ns	
t_{ARY}	READY Valid From Address Valid		220	ns	
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		ns	
t_{RYH}	READY Hold Time	0		ns	
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		ns	
t_{HABF}	Bus Float After HLDA		190	ns	
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		ns	
t_{AC}	Address Valid to Leading Edge of Control	270		ns	
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		ns	
t_{HDH}	HOLD Hold Time	0		ns	
t_{INS}	INTR Setup Time to Leading Edge of CLK (M1, T1 only). Also RST and TRAP	360		ns	
t_{INH}	INTR Hold Time	0		ns	

NOTES:
1. A8-15 Address Specs apply to IO/$\overline{M}$, S0 and S1.
2. For all output timing where $C_L \neq$ 150pf use the following correction factors:
   25pf $\leq C_L <$ 150pf : −.10 ns/pf
   150pf $< C_L \leq$ 300pf : +.30 ns/pf
3. Output timings are measured with purely capacitive load.
4. All timings are measured at output voltage V_L = .8V, V_H = 2.0V, and 1.5V with 20ns rise and fall time on inputs.
5. To calculate timing specifications at other values of T_{CYC} use the table in Table 2.
6. L.E. = Leading Edge T.E. = Trailing Edge

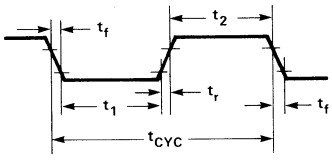
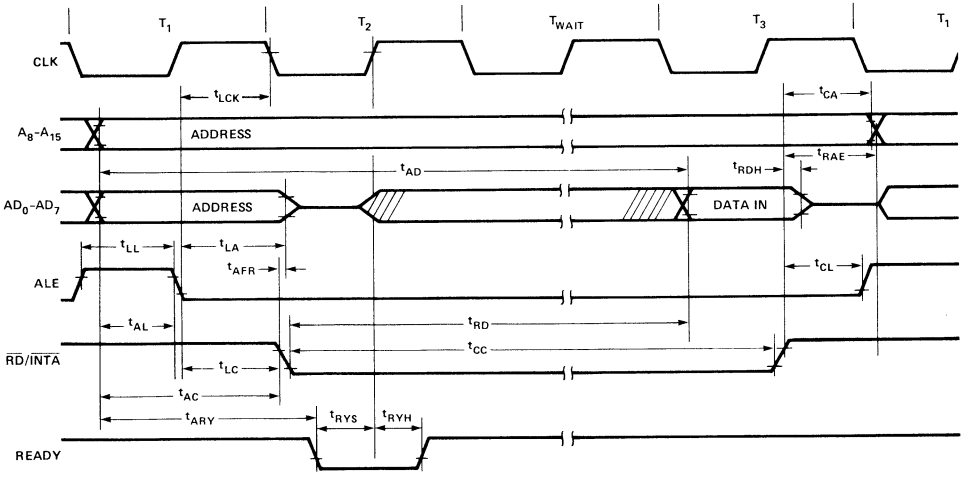


FIGURE 3. CLOCK TIMING WAVEFORM

READ OPERATION



WRITE OPERATION

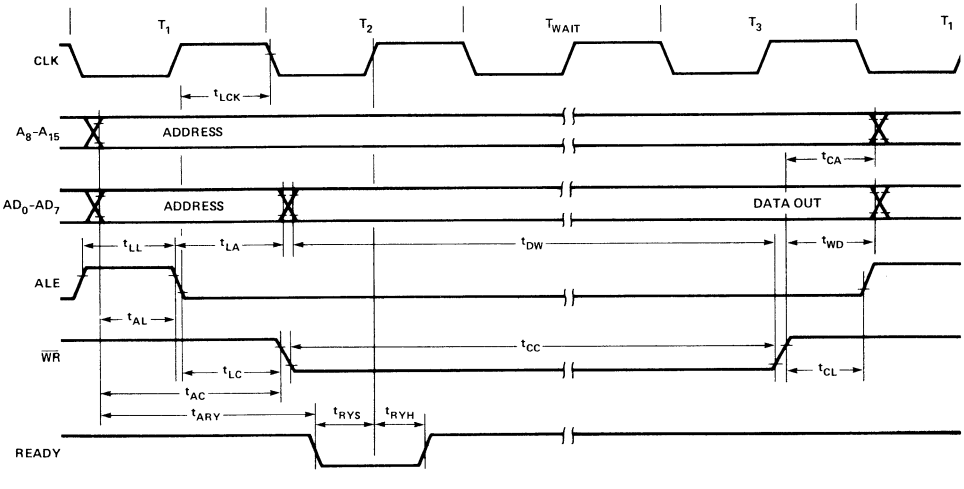


FIGURE 4. 8085 BUS TIMING

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085 can be used with slow memory. Hold causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses. (See Figure 5).

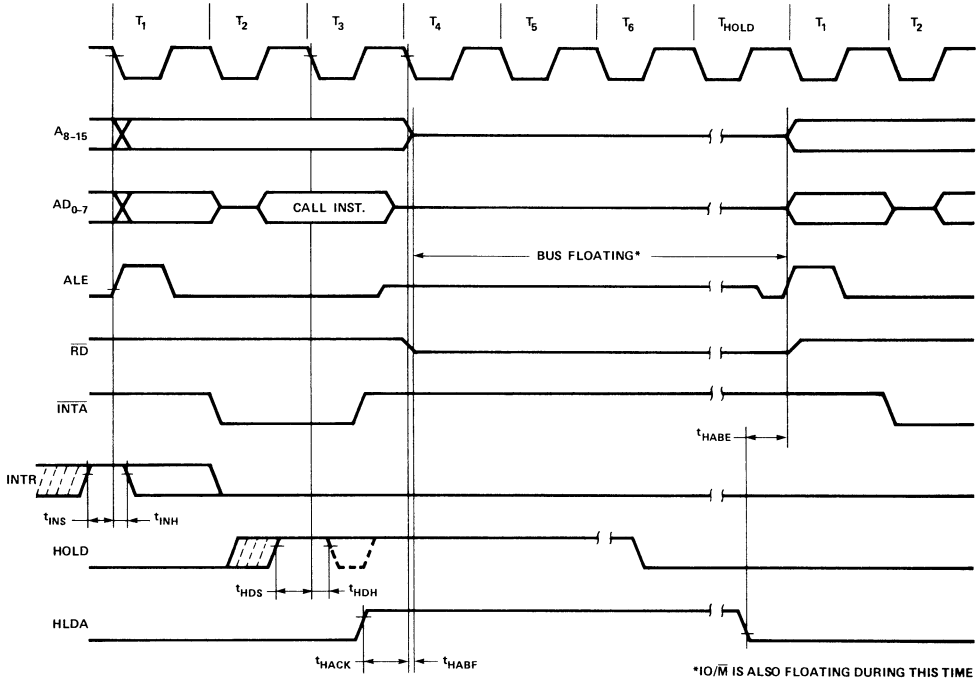


FIGURE 5. 8085 INTERRUPT AND HOLD TIMING

8085 INSTRUCTION SET Summary of Processor Instructions

Mnemonic	Description	Instruction Code[1] D7	D6	D5	D4	D3	D2	D1	D0	Clock[2] Cycles
MOVE, LOAD, AND STORE										
MOVr1,r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4

Mnemonic	Description	Instruction Code[1] D7	D6	D5	D4	D3	D2	D1	D0	Clock[2] Cycles
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6

8085 INSTRUCTION SET Summary of Processor Instructions (Cont.)

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
NEW 8085 INSTRUCTIONS										
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4

NOTES: 1. DDD or SSS: B-000, C-001, D-010, E-011, H-100, L-101, Memory-110, A-111.
2. Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.

SYSTEM INTERFACE

8085 family includes memory components, which are directly compatible to the 8085 CPU. For example, a system consisting of the three chips, 8085, 8155, 8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 6.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 7 shows the system configuration of Memory Mapped I/O using 8085.

The 8085 CPU can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 8.

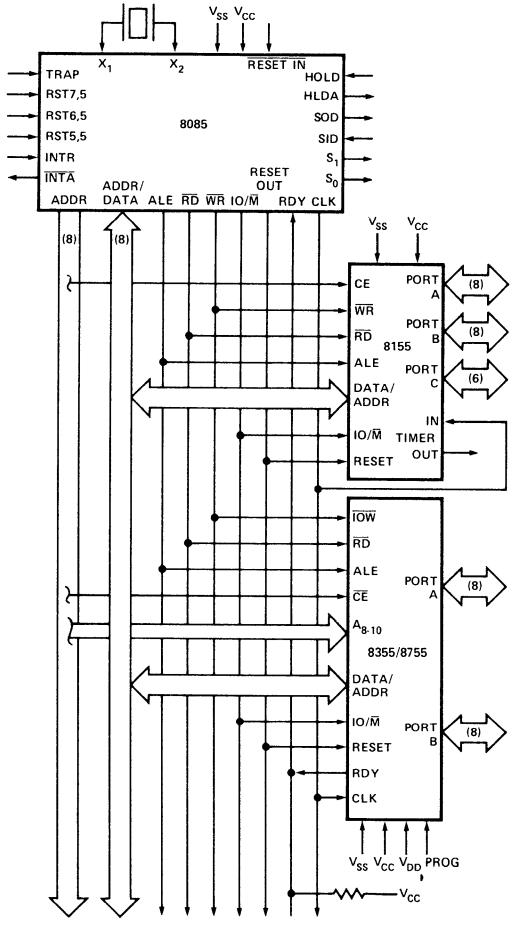


FIGURE 6. 8085 MINIMUM SYSTEM (STANDARD I/O TECHNIQUE)

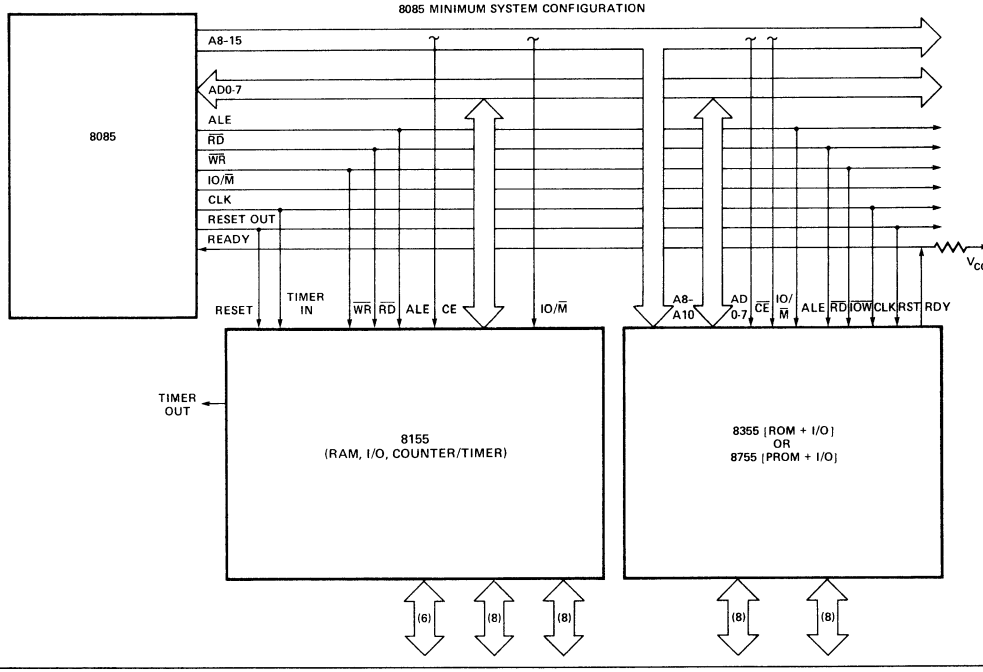


FIGURE 7. MCS-85™ MINIMUM SYSTEM (MEMORY MAPPED I/O)

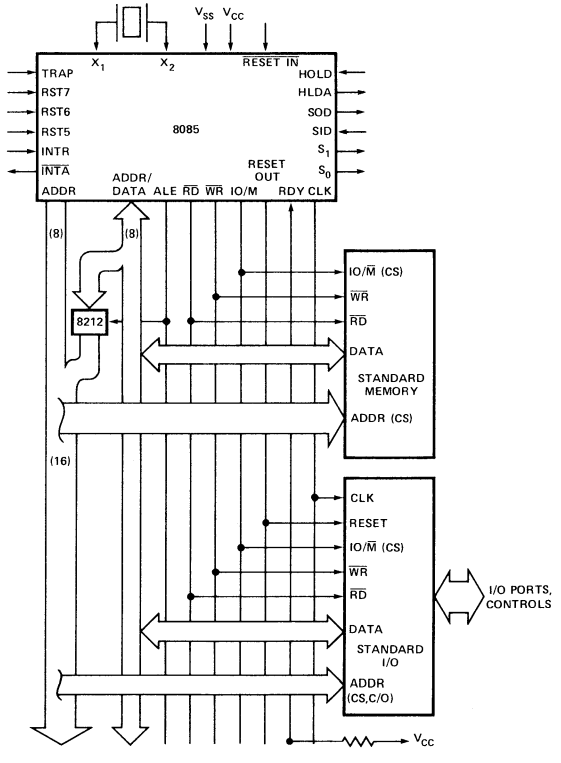


FIGURE 8. MCS-85™ MINIMUM SYSTEM (USING STANDARD MEMORIES)

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

8155

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

*Directly Compatible With 8085 and 8048 CPU

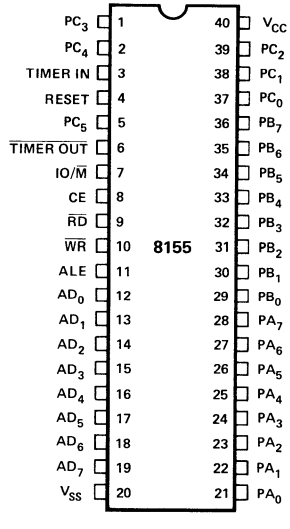
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6 Bit I/O Port
- Programmable 14 Bit Binary Counter/ Timer
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 is a RAM and I/O chip to be used in the MCS-85™ and MCS-48™ microcomputer system. The RAM portion is designed with 2K bit static cells organized as 256 x 8. It has maximum access time of 400 ns to permit use with no wait states in 8085 CPU.

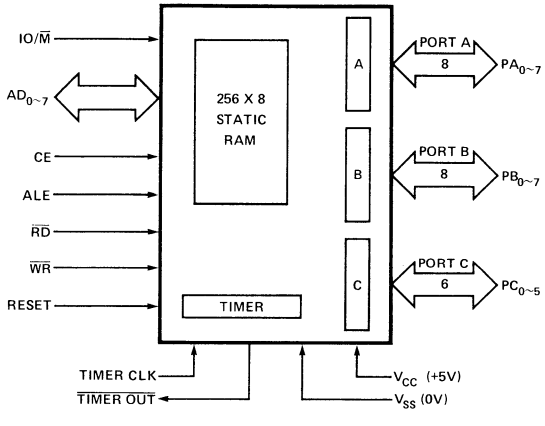
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14 bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system. It operates in binary countdown mode, and its timer modes are programmable.

PIN CONFIGURATION



BLOCK DIAGRAM



MCS 80/85

8155 FUNCTIONAL PIN DEFINITION

The following describes the functions of all of the 8155 pins.

Symbol	Function
RESET	The Reset signal is a pulse provided by the 8085 to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to input mode.
AD_{0-7}	These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch on the falling edge of the ALE. The address can be either for the memory section or the I/O section depending on the polarity of the IO/$\overline{M}$ input signal. The 8-bit data is either written into the chip or Read from the chip depending on the status of $\overline{WRITE}$ or $\overline{READ}$ input signal.
CE or $\overline{CE}$	Chip Enable: Input high on this line enables the chip. The line has bonding option for input Low ($\overline{CE}$).
$\overline{RD}$	Input low on this line and a high on CE enable the AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port will be read to the AD bus.
$\overline{WR}$	Input low on this line and a high on CE cause the data on the AD lines to be written to the RAM or I/O ports depending on the polarity of IO/$\overline{M}$.
ALE	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of CE and IO/$\overline{M}$ onto the chip at the falling edge of ALE.
IO/$\overline{M}$	IO/$\overline{Memory}$ Select: This line selects the memory if low and selects the IO if high.

Symbol	Function
$PA_{0-7}(8)$	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/ Status Register.
$PB_{0-7}(8)$	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/ Status Register.
$PC_{0-5}(6)$	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the C/S Register. When PC_{0-5} are used as control signals, they will provide the following: PC0 — A INTR (Port A Interrupt) PC1 — A BF (Port A Buffer full) PC2 — $\overline{A\ STB}$ (Port A Strobe) PC3 — B INTR (Port B Interrupt) PC4 — $\overline{B\ BF}$ (Port B Buffer Full) PC5 — $\overline{B\ STB}$ (Port B Strobe)
TIMER IN	This is the input to the counter timer.
$\overline{TIMER\ OUT}$	This pin is the timer output. This output can be either a square wave or a pulse depending on the timer mode.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

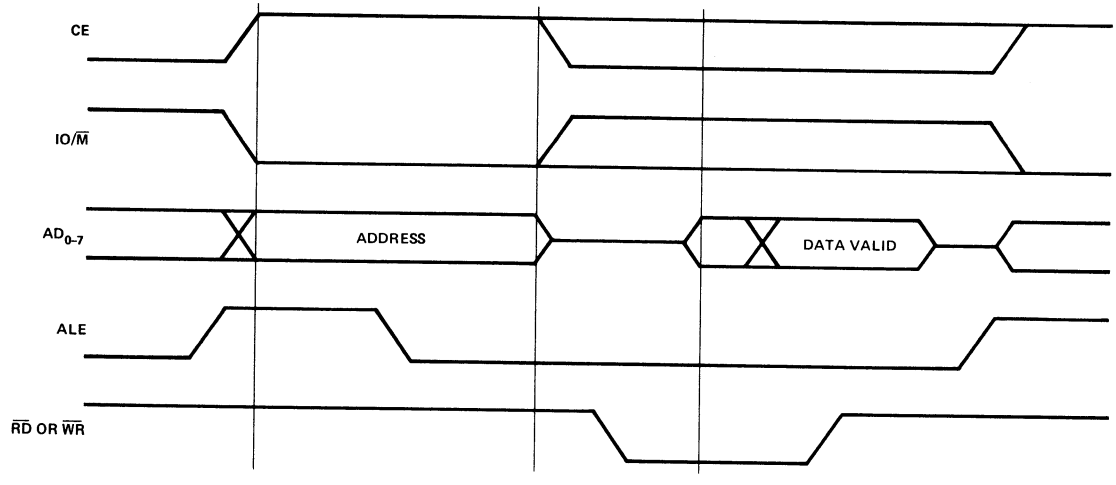
OPERATIONAL DESCRIPTION

The 8155 includes the following operational features:

- 2K Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit binary down counter

The I/O portion contains four registers (Command/Status, PA_{0-7}, PB_{0-7}, PC_{0-5}). The IO/M (IO/Memory Select) pin selects the I/O or the memory (RAM) portion. Detailed descriptions of memory, I/O ports and timer functions will follow.

The 8-bit address on the AD lines, CE, and IO/$\overline{M}$ are all latched on chip at the falling edge of ALE. Therefore the ALE signal should be activated (high) before the transistion of CE and IO/$\overline{M}$ signal, as shown in Figure 1. A low on the IO/$\overline{M}$ must be provided to select the memory section.



NOTE: FOR DETAILED TIMING DIAGRAM INFORMATION, SEE FIGURE 7 AND A.C. CHARACTERISTICS.

FIGURE 1. MEMORY READ/WRITE CYCLE.

PROGRAMMING OF THE COMMAND/ STATUS REGISTER

The command register consists of eight latches one for each bit. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The C/S register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation. The meaning of each bit of the command byte is defined as follows:

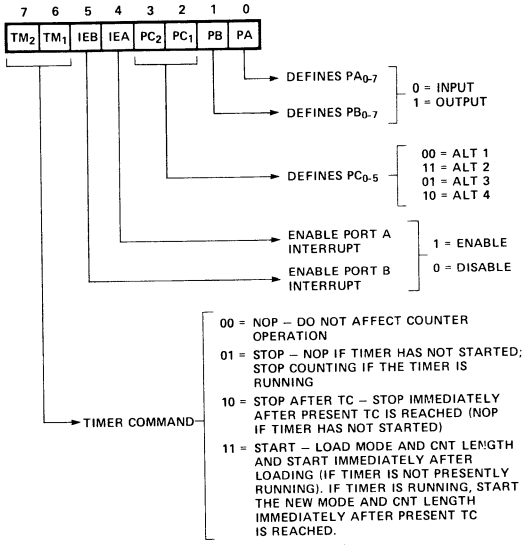


FIGURE 2. COMMAND/STATUS REGISTER BIT ASSIGNMENT.

READING THE COMMAND/STATUS REGISTER

The status register consists of seven latches one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the C/S Register (Address XXXXX000). Status word format is shown below:

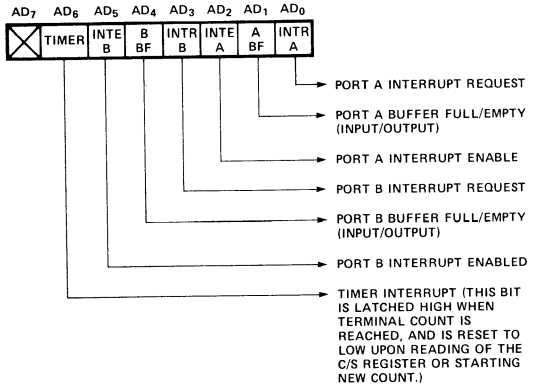


FIGURE 3. COMMAND/STATUS REGISTER STATUS WORD FORMAT.

INPUT/OUTPUT SECTION

The I/O section of the 8155 consists of four registers as described below:

- **Command/Status Register (C/S)** — This register is assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S register is selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer become available on the AD_{0-7} lines.

- **PA Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

- **PB Register** — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.

- **PC Register** — This register has the address XXXXX011 and contains only 6-bits. The 6-bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

  When PC_{0-5} is used as a control port, 3-bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the 8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. See Table 1.

TABLE 1. TABLE OF PORT CONTROL ASSIGNMENT.

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A Strobe)	A $\overline{STB}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B Strobe)

The set and reset of INTR and BF with respect to $\overline{STB}$, $\overline{WR}$ and $\overline{RD}$ timing is shown in Figure 9.

In the summary, the registers' assignments are:

Address	Pinouts	Functions	No. of Bits
XXXXX000	Internal	Command/Status Register	8
XXXXX001	PA0-7	General Purpose I/O Port	8
XXXXX010	PB0-7	General Purpose I/O Port	8
XXXXX011	PC0-5	General Purpose I/O Port or Control Lines	6

When the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
$\overline{STROB}$	Input Control	Input Control

TIMER SECTION

The timer is a 14-bit counter that counts the 'timer input' pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register.

The timer addresses serve a dual purpose. During WRITE operation, a COUNT LENGTH REGISTER (CLR) with a count length (bits 0-13) and a timer mode (bits 14-15) are loaded. During READ operation the contents of the counter (the present count) and the mode bits are read.

To be sure that the right content of the counter is read, it is preferable to stop counting, read it, and then load it again and continue counting.

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 will specify the length of the next count and bits 14-15 will specify the timer output mode.

There are four modes to choose from:

0. Puts out low during second half of count.
1. Square wave
2. Single pulse upon TC being reached
3. Repetitive single pulse everytime TC is readied and automatic reload of counter upon TC being reached, until instructed to stop by a new command loaded into C/S.

Bits 6-7 of Command/Status Register Contents are used to start and stop the counter. There are four commands to choose from:

Note: See the further description on Command/Status Register.

C/S7	C/S6	
0	0	NOP — Do not affect counter operation.
0	1	STOP — NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

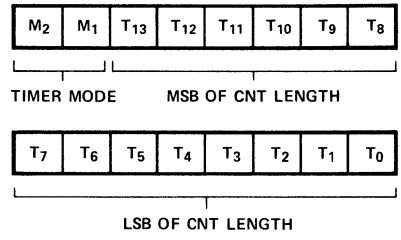
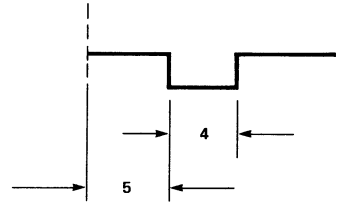


FIGURE 4. TIMER FORMAT

M2 M1 defines the timer mode as follows:

M2	M1	
0	0	Puts out low during second half of count.
0	1	Square wave, i.e., the period of the square wave equals the count length programmed with automatic reload at terminal count.
1	0	Single pulse upon TC being reached.
1	1	Automatic reload, i.e., single pulse everytime TC is reached.

Note: In case of an asymmetric count, i.e. 9, larger half of the count will be high, the larger count will stay active as shown in Figure 5.



Note: 5 and 4 refer to the number of clock cycles in that time period.

FIGURE 5. ASYMMETRIC COUNT.

8085 MINIMUM SYSTEM CONFIGURATION

Figure 6 shows that a minimum system is possible using only three chips:

- 256 Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

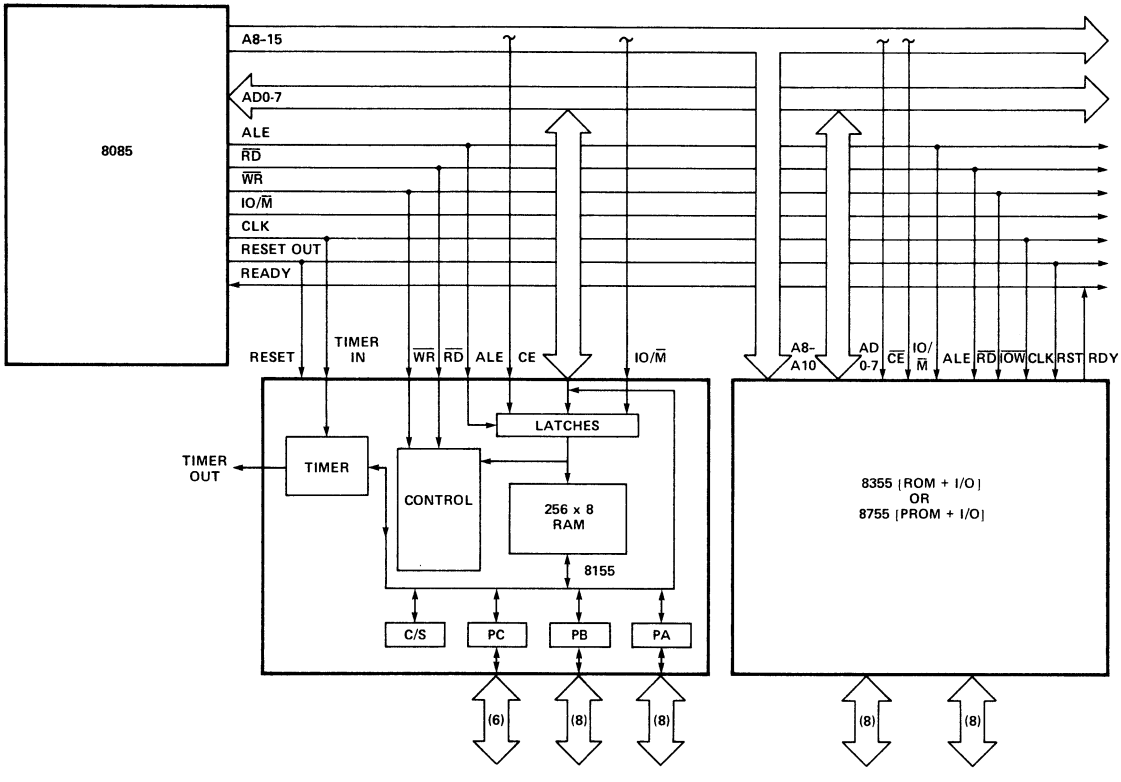


FIGURE 6. 8085 MINIMUM SYSTEM CONFIGURATION.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.3V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{AL}	Address to Latch Set Up Time	50		ns	
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		150	ns	
t_{AD}	Address Stable to Data Out Valid		400	ns	
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float After READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	0		ns	
t_{RV}	Recovery Time Between Controls	300		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Setup Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	150 pF Load
t_{SBF}	Strobe to Buffer Full		400	ns	
t_{SS}	Strobe Width	200		ns	
t_{RBE}	READ to Buffer Empty		400	ns	
t_{SI}	Strobe to INTR On		400	ns	
t_{RDI}	READ to INTR Off		400	ns	
t_{PSS}	Port Setup Time to Strobe Strobe	50		ns	
t_{PHS}	Port Hold Time After Strobe	100		ns	
t_{SBE}	Strobe to Buffer Empty		400	ns	
t_{WBF}	WRITE to Buffer Full		400	ns	
t_{WI}	WRITE to INTR Off		400	ns	
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low	400		ns	
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High	400		ns	
t_{RDE}	Data Bus Enable from READ Control	10		ns	

Note: For Timer Input Specification, see Figure 10.

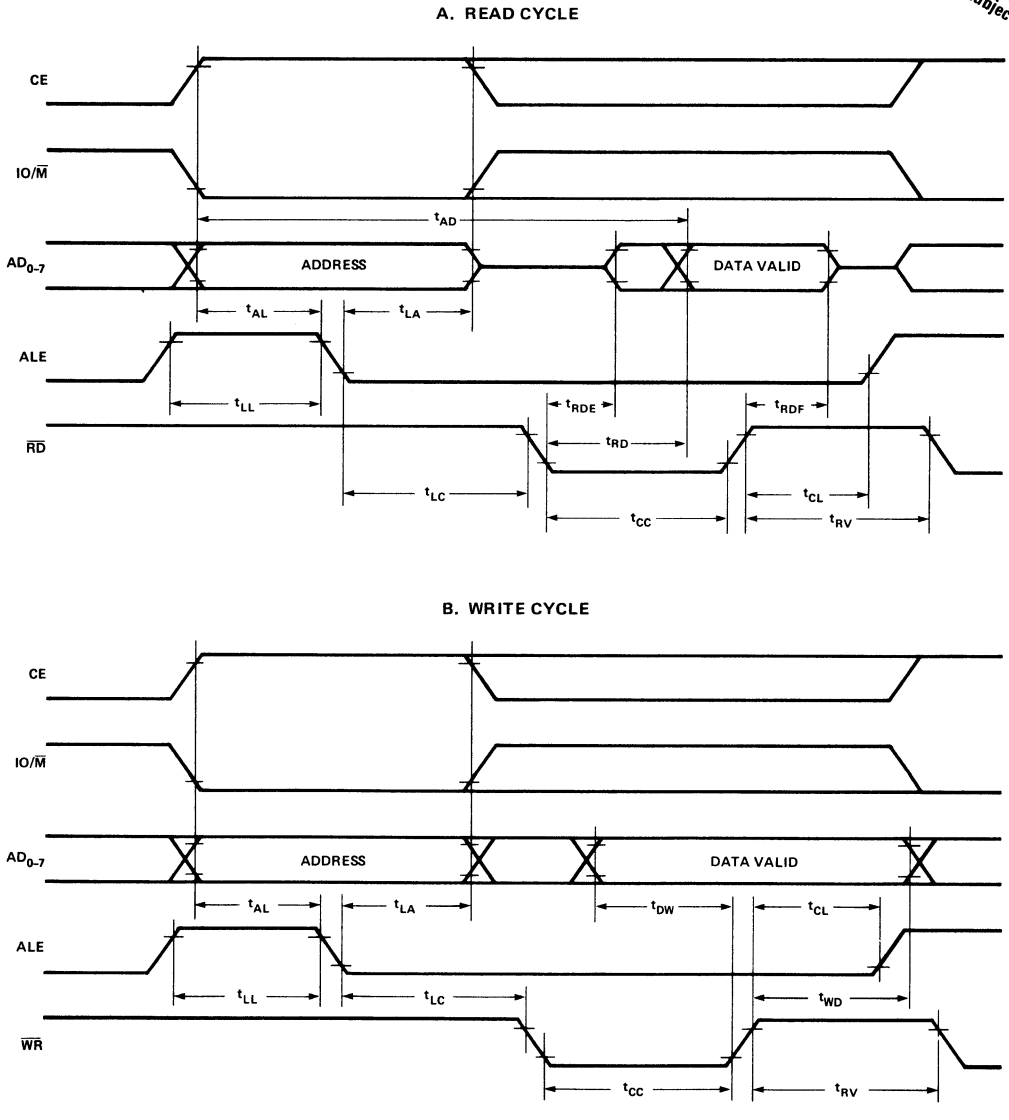


FIGURE 7. 8155 READ/WRITE TIMING DIAGRAM.

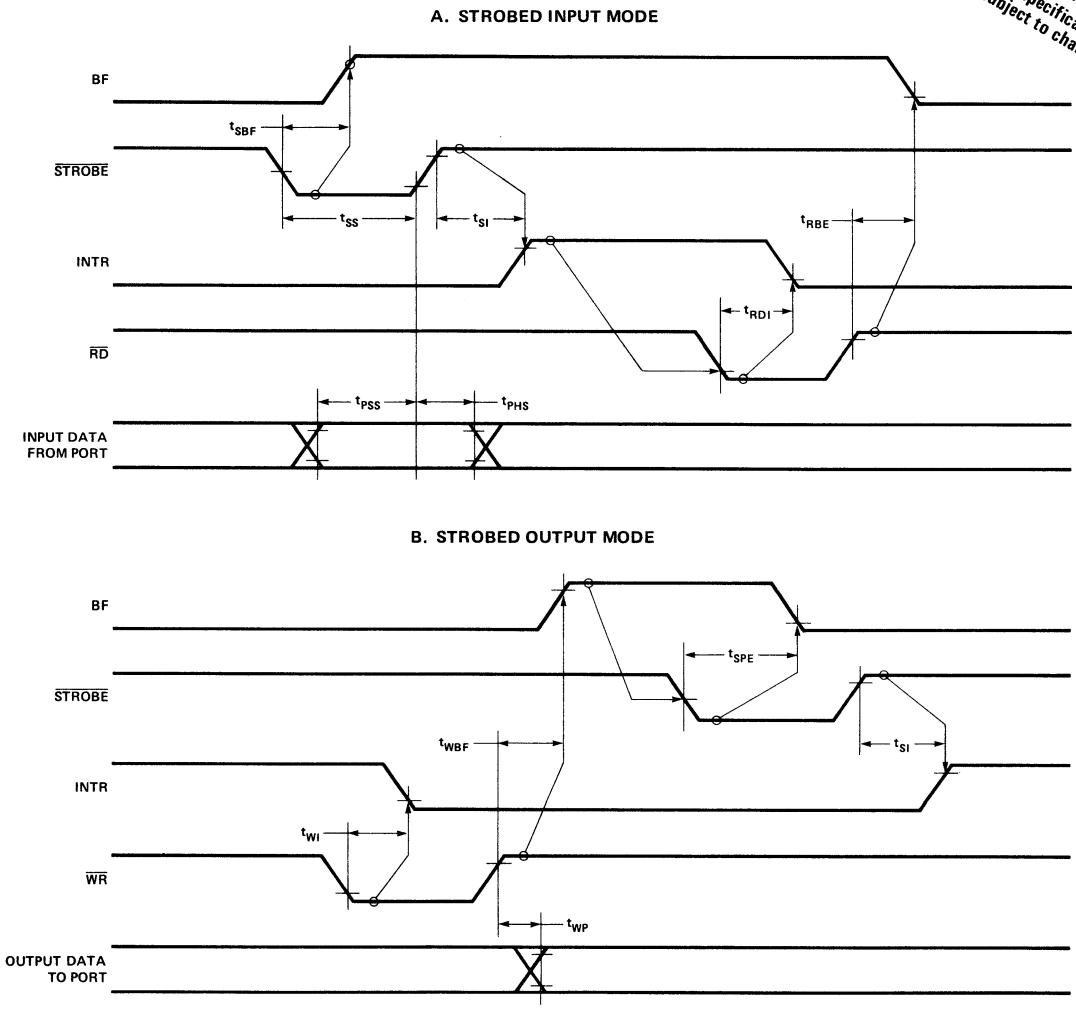


FIGURE 8. BASIC I/O TIMING.

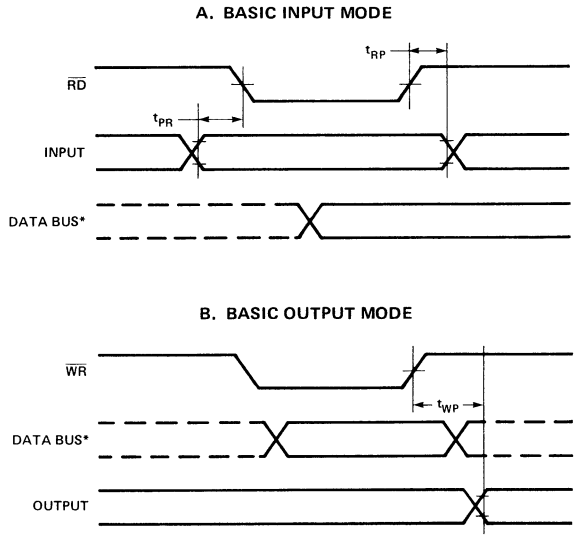
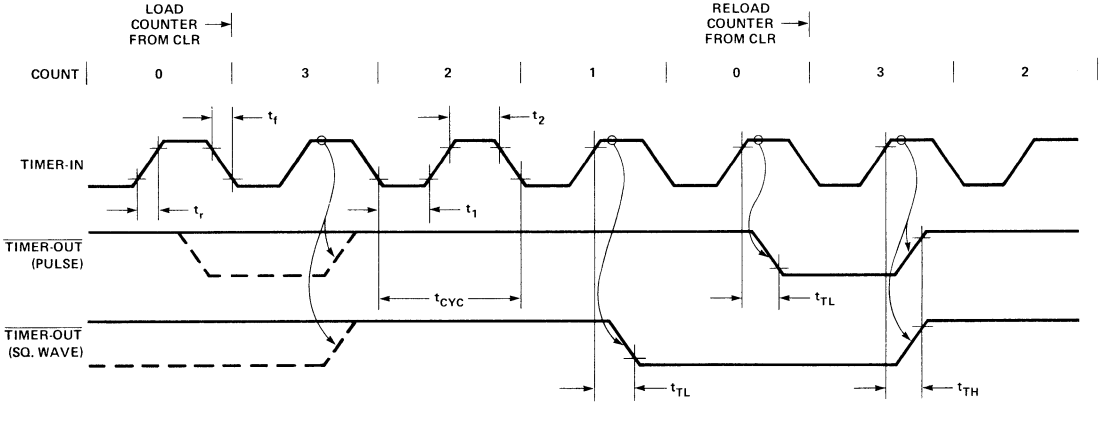


FIGURE 9. STROBED I/O TIMING WAVEFORM.



t_{CYC}	320 ns MIN.
t_{RISE} & t_{FALL}	30 ns MAX.
t_1	80 ns MIN.
t_2	120 ns MIN.
t_{TL}	TIMER-IN TO $\overline{\text{TIMER-OUT}}$ LOW (TO BE DEFINED).
t_{TH}	TIMER-IN TO $\overline{\text{TIMER-OUT}}$ HIGH (TO BE DEFINED).

FIGURE 10. TIMER OUTPUT WAVEFORM.

8355
16,384 BIT ROM WITH I/O

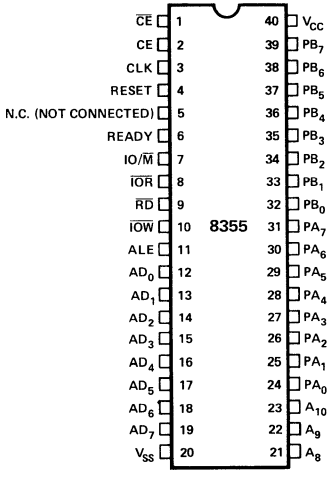
*Directly Compatible With 8085 and 8048 CPU

- 2048 Words x 8 Bits
- Single +5V Power Supply
- Internal Address Latch
- 2 General Purpose 8 Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40 Pin DIP

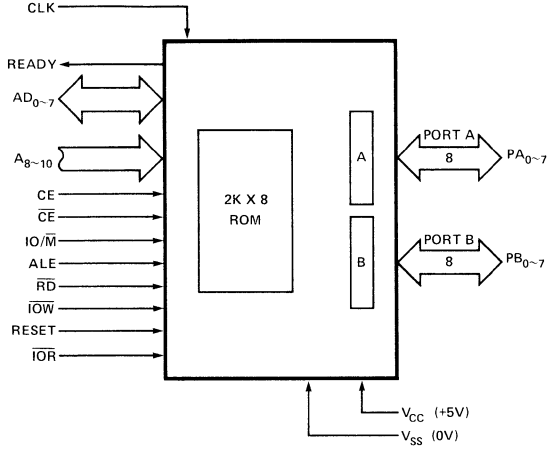
The 8355 is a ROM and I/O chip to be used in the MCS-85™ and MCS-48™ microcomputer system. The ROM portion is organized as 2048 x 8. It has maximum access time of 400 ns to permit use with no wait states in 8085 CPU.

The I/O portion consists of two general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

PIN CONFIGURATION



BLOCK DIAGRAM



8355 FUNCTIONAL PIN DEFINITION

Symbol	Function
ALE	When ALE (Address Latch Enable) is high, AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE, and $\overline{CE}$ enter address latched. The signals (AD, IO/$\overline{M}$, A_{8-10}, CE, $\overline{CE}$) are latched in at the trailing edge of ALE.
AD_{0-7}	Bi-directional Address/Data bus. The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10}	These are the high order bits of the ROM address. They do not affect I/O operations.
$\overline{CE}$ CE	Chip Enable Inputs: $\overline{CE}$ is active low and CE is active high. The 8355 can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_{0-7} and READY outputs will be in a high impedance state.
IO/$\overline{M}$	If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the ROM.
$\overline{RD}$	If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected ROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are tri-stated.
$\overline{IOW}$	If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.

Symbol	Function
CLK	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE}$ low, CE high and ALE high.
READY	Ready is a tri-state output controlled by $\overline{CE}$, CE, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK (see Figure 4).
PA_{0-7}	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0. Read operation is selected by $\overline{IOR}$ low when the Chip is enabled and AD_0 low. Alternately, IO/$\overline{M}$ high and $\overline{RD}$ low may be used in place of $\overline{IOR}$ when the chip is enabled and AD_0 is low to allow reading from a port.
PB_{0-7}	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.
RESET	An input high on RESET causes all pins in Ports A and B to assume input mode.
$\overline{IOR}$	When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination IO/$\overline{M}$ high and $\overline{RD}$ low.
V_{CC}	+5 volt supply.
V_{SS}	0 volt supply.

FUNCTIONAL DESCRIPTION

ROM Section

The ROM section of the chip is addressed by an 11-bit address and the Chip Enables. The address and levels on the Chip Enable pins are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the eight output bits of ROM addressed by the latched address are put out through AD_{0-7} output buffers.

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers in 8355 determine the input/output status of each pin in the corresponding ports. A 0 specifies an input mode, and a 1 specifies an output mode. The table summarizes port and DDR designation. *DDR's cannot be read.*

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD_{0-7} is written into I/O port selected by the latched value of AD_{0-1}.

During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high (glitch free output).

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

System Interface with 8085

A system using the 8355 can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE and $\overline{CE}$. By using a combination of unused address lines A_{11-15} and the Chip Enable inputs, the 8085 system can use up to 5 each 8355's without requiring a CE decoder. See Figure 1.

Note: Use $\overline{CE}$ for the first 8355 in the system, and CE for the other 8355's. Permits up to 5 ea. 8355's in a system without CE decoder.

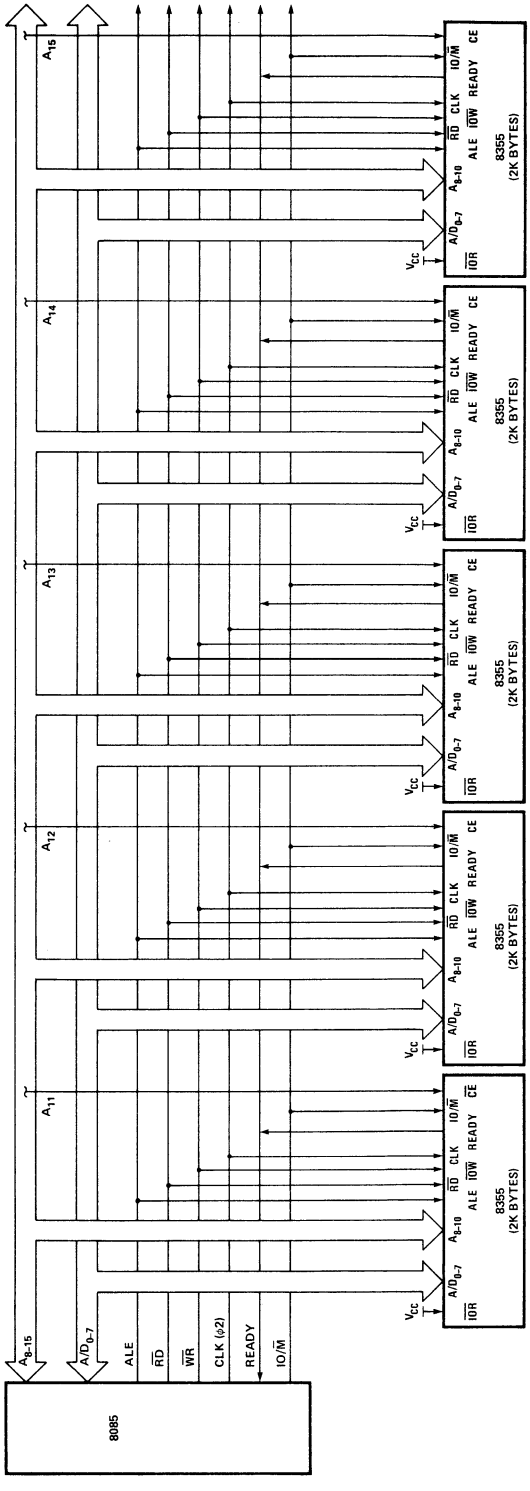


FIGURE 1. 8355 IN 8085 SYSTEM (STANDARD I/O).

If a memory mapped I/O approach is used the 8355 will be selected by the combination of both the Chip Enables and IO/$\overline{M}$ using the $AD_{8\text{-}15}$ address lines. See Figure 2.

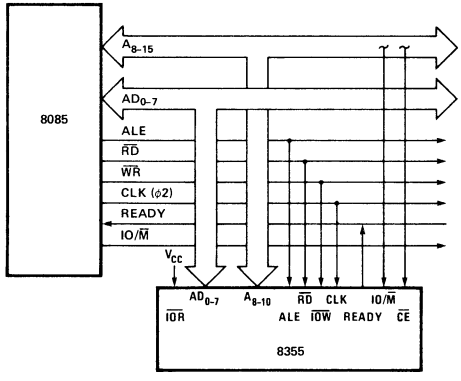


FIGURE 2. 8355 IN 8085 SYSTEM (MEMORY-MAPPED I/O).

System Interface with 8048

The 8355 contains an 8-bit address latch which allows it to interface directly to MCS-48 Microcomputers without additional hardware (Figure 3). Program memory is accessed by applying 11-bits of address to the A_0—A_{10} inputs and a low level on the IO/$\overline{M}$ and $\overline{CE}$ inputs then latching these inputs with ALE. The $\overline{CE}$ input serves to select one of several possible 8355s in a system and the IO/$\overline{M}$ signal indicates that a subsequent read operation will be from program memory. While ALE is high the A_0—A_{10}, IO/$\overline{M}$, and $\overline{CE}$ inputs are allowed into the 8355 and when ALE is brought low, these inputs are latched. If the latched conditions indicate that a program memory fetch is to occur, a low level on $\overline{RD}$ will cause the data to be outputted on the data bus.

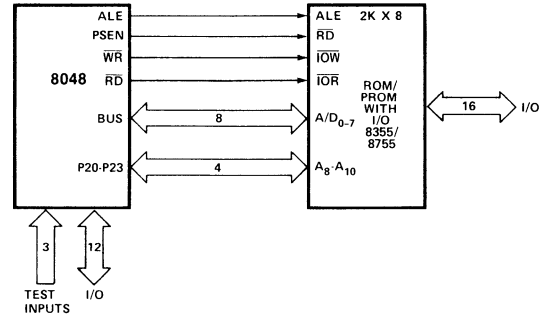


FIGURE 3. INTERFACE TO MCS-48™ MICROCOMPUTERS

Programming

See ROM programming instructions, page 3-55.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.3V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CYC}	Clock Cycle Time	320		ns	
T_1	CLK Pulse Width	80		ns	C_{LOAD} = 150 pF
T_2	CLK Pulse Width	120		ns	(See Figure 3)
t_f,t_r	CLK Rise and Fall Time		30	ns	
t_{AL}	Address to Latch Set Up Time	50		ns	
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		150	ns	
t_{AD}	Address Stable to Data Out Valid		400	ns	150 pF Load
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float after READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	0		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Set Up Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	
t_{RYH}	READY HOLD TIME	0	120	ns	
t_{ARY}	ADDRESS (CE) to READY		160	ns	
t_{RV}	Recovery Time between Controls	300		ns	
t_{RDE}	Data Out Delay from READ Control	10		ns	

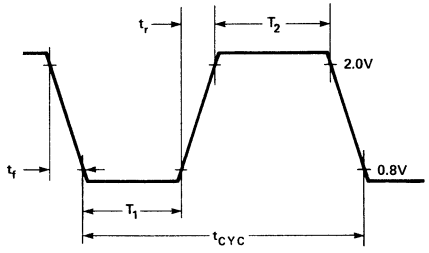


FIGURE 4. CLOCK SPECIFICATION FOR 8355.

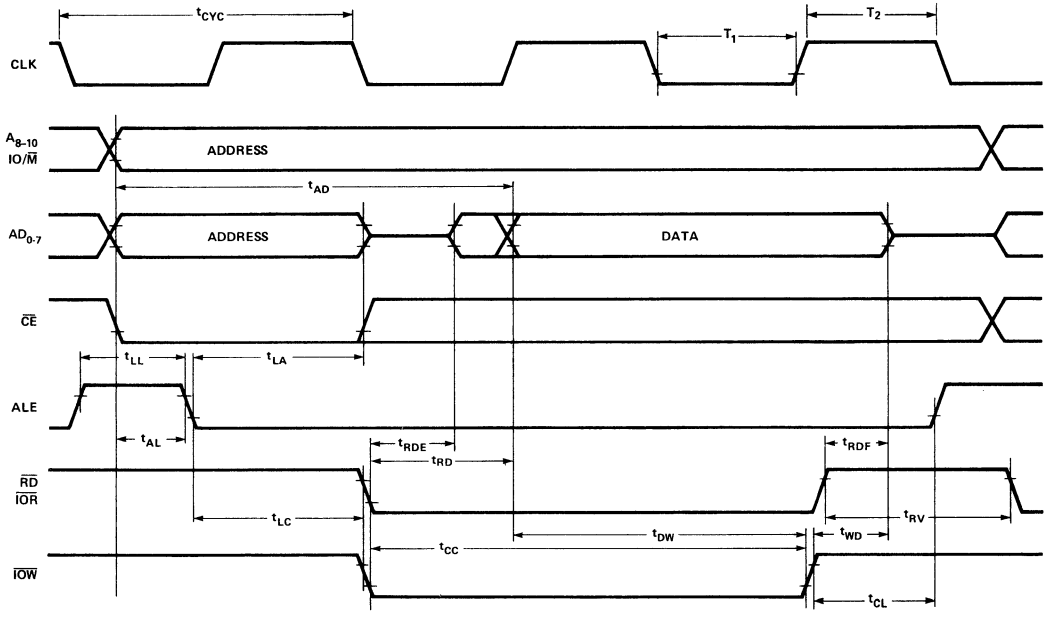


FIGURE 5. ROM READ AND I/O READ AND WRITE.

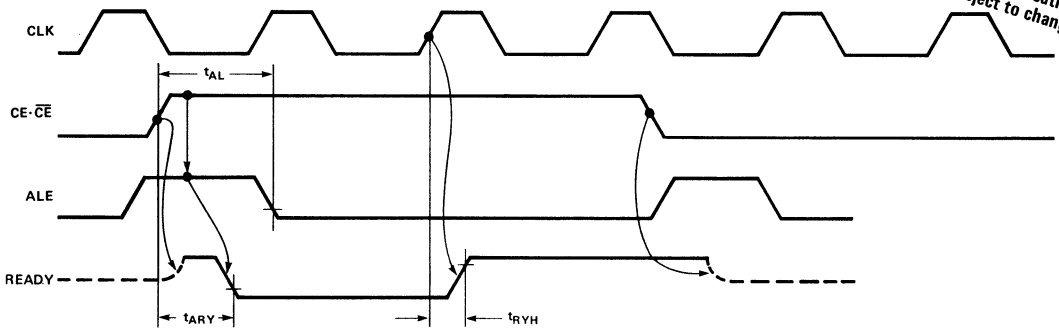
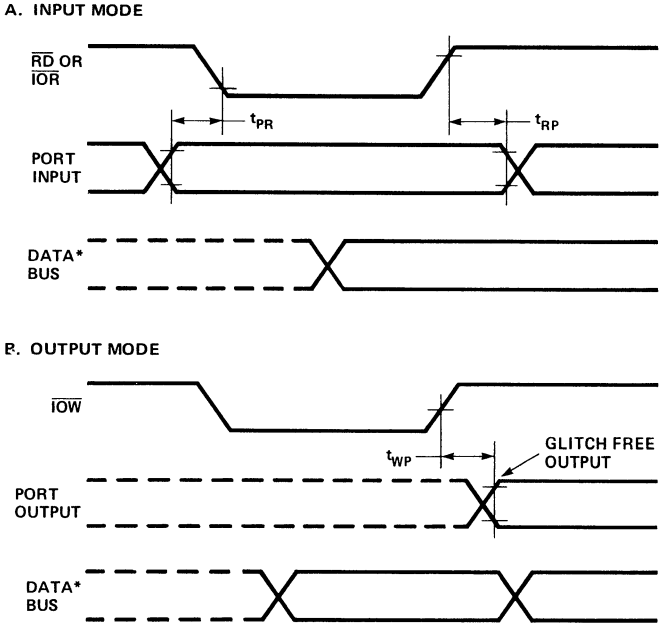


FIGURE 6. WAIT STATE TIMING (READY = 0).



*DATA BUS TIMING IS SHOWN IN FIGURE 3.

FIGURE 7. I/O PORT TIMING.

8755
16,384 BIT EPROM WITH I/O

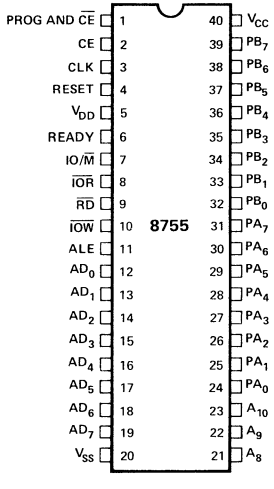
*Directly Compatible With 8085 and 8048 CPU

- 2048 Words x 8 Bits
- Single +5V Power Supply (V_{CC})
- U.V. Erasable and Electrically Reprogrammable
- Internal Address Latch
- 2 General Purpose 8 bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40 Pin DIP

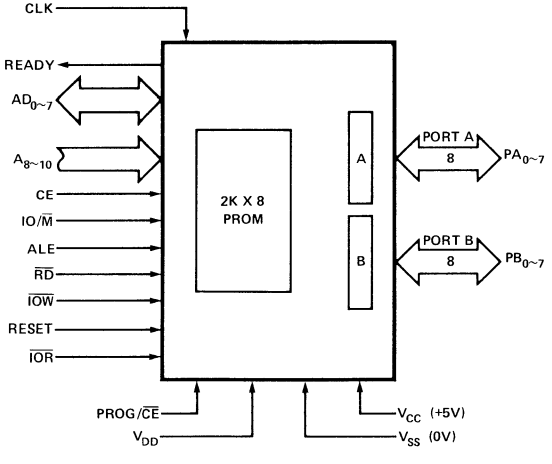
The 8755 is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the MCS-85™ and MCS-48™ microcomputer system. The PROM portion is organized as 2048 x 8. It has maximum access time of 400 ns to permit use with no wait states in 8085 CPU.

The I/O portion consists of two general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

PIN CONFIGURATION



BLOCK DIAGRAM



8755 FUNCTIONAL PIN DESCRIPTION

Symbol	Function
ALE	When Address Latch Enable is high, AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE, and $\overline{CE}$ enter the address latches. The signals (AD, IO/M, A_{8-10}, CE) are latched in at the trailing edge of ALE.
AD_{0-7}	Bi-directional Address/Data bus. The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10}	These are the high order bits of the PROM address. They do not affect I/O operations.
$\overline{CE}$/PROG CE	CHIP ENABLE INPUTS: $\overline{CE}$ is active low and CE is active high. Both chip enables must be active to permit accessing the PROM. $\overline{CE}$ is also used as a programming pin (see section on programming).
IO/$\overline{M}$	If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the PROM.
$\overline{RD}$	If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected PROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are tri-stated.
$\overline{IOW}$	If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.
CLK	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE}$ low, CE high, and ALE high.
READY	READY is a 3-state output controlled by CE, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK (see Figure 2.).
PA_{0-7}	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0. Read operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 low, or IO/$\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 low.
PB_{0-7}	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.
RESET	In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
$\overline{IOR}$	When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} ("1").
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.
V_{DD}	V_{DD} is a programming voltage, and it is normally grounded. For programming, a high voltage is supplied with V_{DD}, = 25V, typical.

FUNCTIONAL DESCRIPTION

PROM Section

The 8755 contains an 8-bit address latch which allows it to interface directly to MCS-48 and MCS-85 Microcomputers without additional hardware.

The PROM section of the chip is addressed by the 11-bit address and CE. The address, $\overline{CE}$ and CE are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the PROM location addressed by the latched address are put out on the AD_{0-7} lines.

I/O Section

The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers determine the input/output status of each pin in the corresponding port. A 0 specifies an input mode, and a 1 specifies an output mode. The table summarizes port and DDR designation. Contents of the DDR's cannot be read.

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD_{0-7} is written into I/O port selected by the latched value of AD_{0-1}. During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high. (glitch free output).

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

ERASURE CHARACTERISTICS

The erasure characteristics of the 8755 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level flourescent lighting could erase the typical 8755 in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8755 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8755 window to prevent unintentional erasure.

The recommended erasure procedure (see page 3-55) for the 8755 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm^2 power rating. The 8755 should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

PROGRAMMING

See the EPROM programming section, page 3-55.

SYSTEM APPLICATIONS

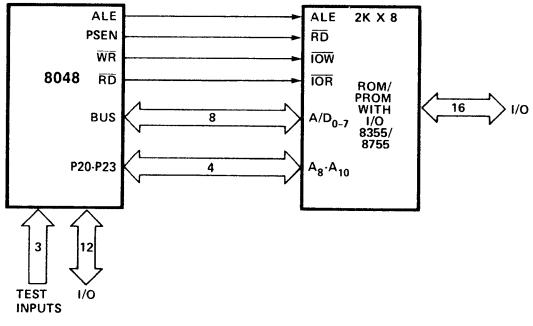
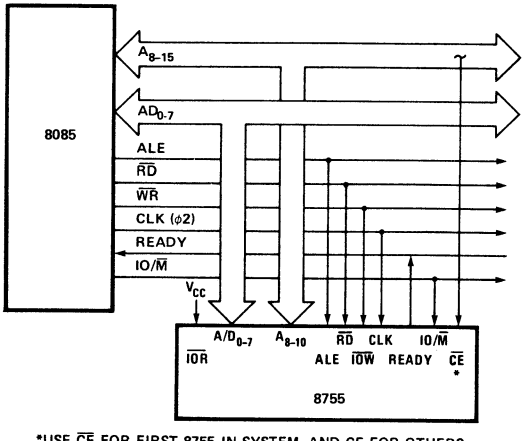


FIGURE 1. INTERFACE TO MCS-48™ MICROCOMPUTERS



*USE $\overline{CE}$ FOR FIRST 8755 IN SYSTEM, AND CE FOR OTHERS. BY CONNECTING CE OF EACH 8755 CHIP TO EACH OF A_{11} THROUGH A_{15}, THE MINIMUM SYSTEM CAN USE 5-8755's (10K BYTES) WITHOUT REQUIRING CE DECODER.

FIGURE 2. 8755 IN 8085 SYSTEM (STANDARD I/O).

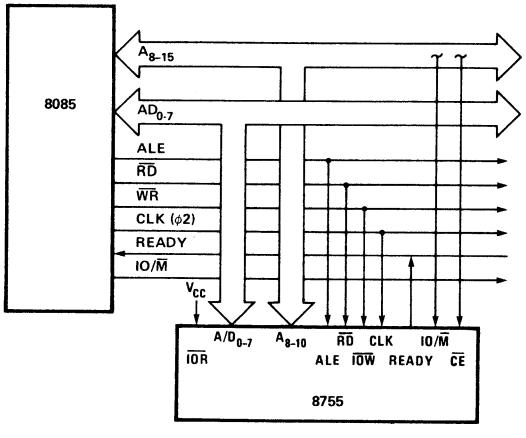


FIGURE 3. 8755 IN 8085 SYSTEM (MEMORY-MAPPED I/O).

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CYC}	Clock Cycle Time	320		ns	
T_1	CLK Pulse Width	80		ns	C_{LOAD} = 150 pF
T_2	CLK Pulse Width	120		ns	(See Figure 3)
t_f,t_r	CLK Rise and Fall Time		30	ns	
t_{AL}	Address to Latch Set Up Time	50		ns	
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		150	ns	
t_{AD}	Address Stable to Data Out Valid		400	ns	150 pF Load
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float after READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	0		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Set Up Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	
t_{RYH}	READY HOLD TIME	0	120	ns	
t_{ARY}	ADDRESS (CE) to READY		160	ns	
t_{RV}	Recovery Time between Controls	300		ns	
t_{RDE}	Data Out Delay from READ Control	10		ns	

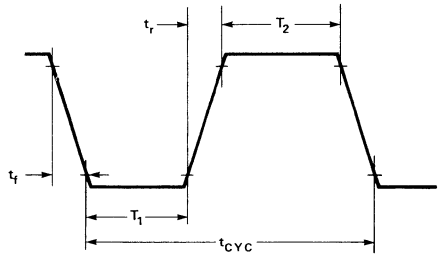


FIGURE 3. CLOCK SPECIFICATION FOR 8755

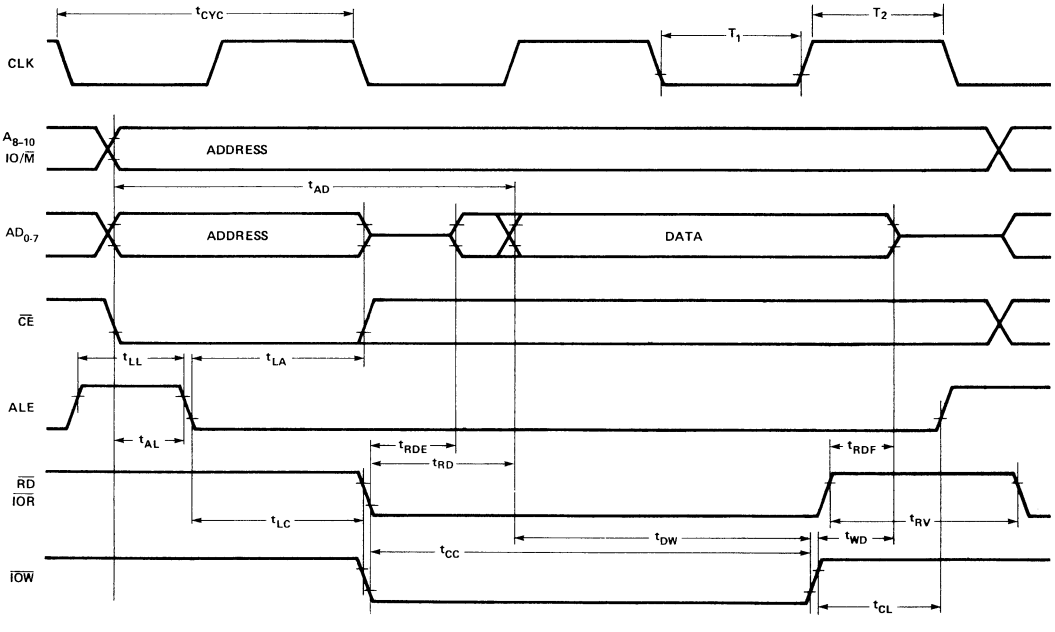
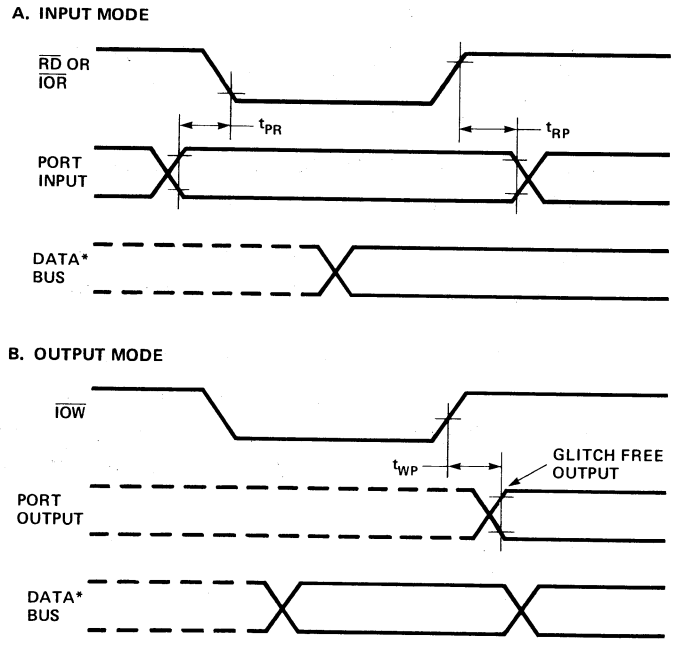


FIGURE 4. PROM READ AND I/O WRITE TIMING.



*DATA BUS TIMING IS SHOWN IN FIGURE 4.

FIGURE 5. I/O PORT TIMING.

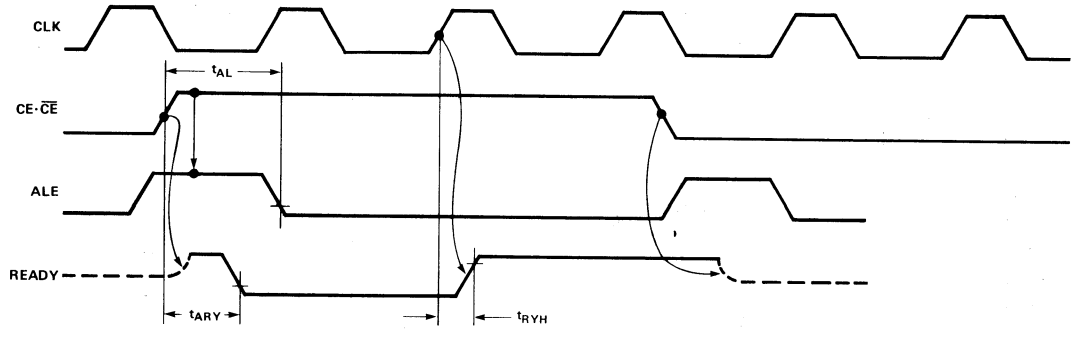


FIGURE 6. WAIT STATE TIMING (READY = 0).

8101A-4
1024 BIT STATIC MOS RAM WITH SEPARATE I/O

* 450 nsec Access Time Maximum
* 256 Word by 4 Bit Organization

- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Powerful Output Drive Capability**
- **Low Cost Packaging: 22 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150mW**
- **Three-State Output: OR-Tie Capability**
- **Output Disable Provided for Ease of Use in Common Data Bus Systems**

The Intel® 8101A-4 is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

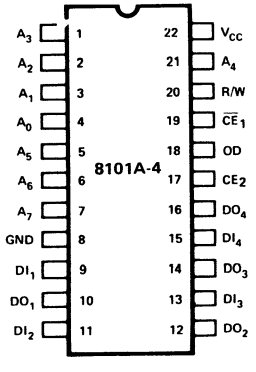
The 8101A-4 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bi-directional logic in a common I/O system.

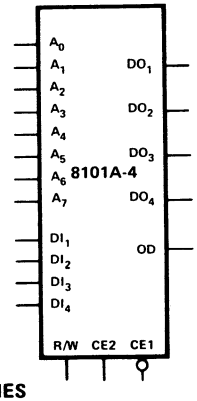
The Intel® 8101A-4 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



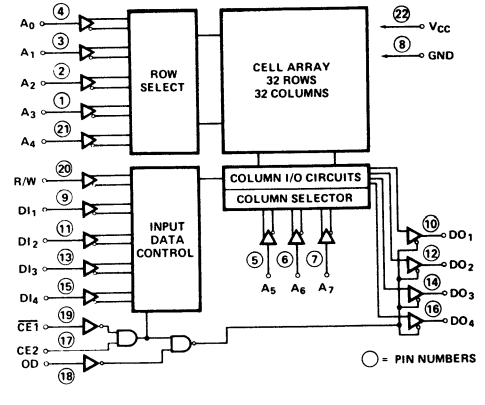
LOGIC SYMBOL



PIN NAMES

DI_1-DI_4	DATA INPUT	$\overline{CE}_2$	CHIP ENABLE 2
A_0-A_7	ADDRESS INPUTS	$\overline{OD}$	OUTPUT DISABLE
R/W	READ/WRITE INPUT	DO_1-DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

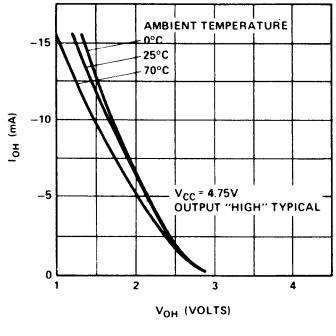
D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

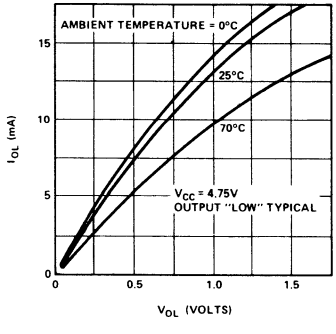
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current[2]		1	10	μA	Output Disabled, V_{OUT}=4.0V
I_{LOL}	I/O Leakage Current[2]		-1	-10	μA	Output Disabled, V_{OUT}=0.45V
I_{CC1}	Power Supply Current		35	55	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			60	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -400μA

TYPICAL D.C. CHARACTERISTICS

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Input and Output tied together.

A.C. CHARACTERISTICS

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	(See Below)
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	(See Below)
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

A.C. CONDITIONS OF TEST

t_r, t_f . . . . . 20 ns
Input Levels . . . . . 0.8V or 2.0V
Timing Reference 1.5V
Load . . . . . 1 TTL Gate and C_L = 100 pF

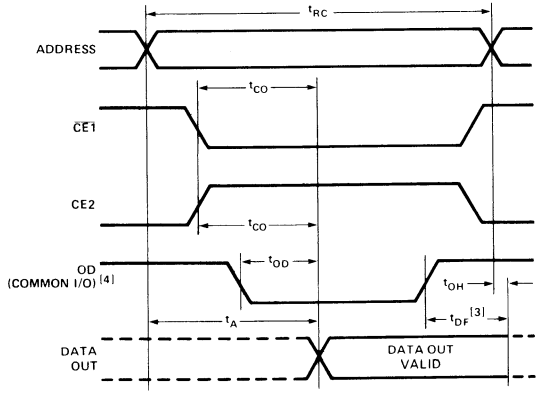
CAPACITANCE[3] T_A = 25°C, f = 1MHz

Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

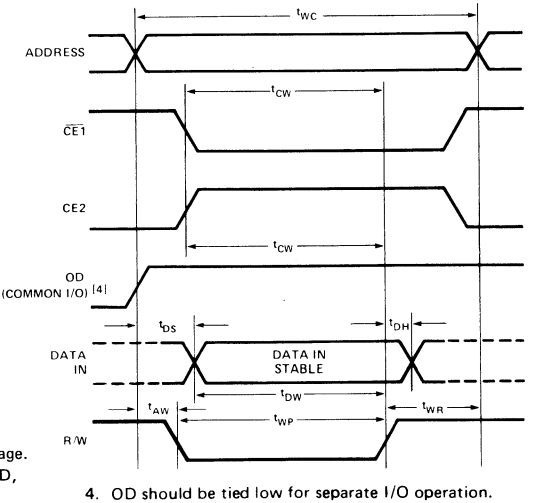
MCS 80/85

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.
3. This parameter is periodically sampled and is not 100% tested.
4. OD should be tied low for separate I/O operation.

8102A-4

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

- **Access Time — 450 ns Max.**
- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible — All Inputs and Output**
- **Static MOS — No Clocks or Refreshing Required**
- **Low Power — Typically 150 mW**
- **Three-State Output — OR-Tie Capability**
- **Simple Memory Expansion — Chip Enable Input**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging — 16 Pin Plastic Dual-In-Line Configuration**

The Intel®8102A-4 is a 1024 word by one bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 8102A-4 is designed for microcomputer memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

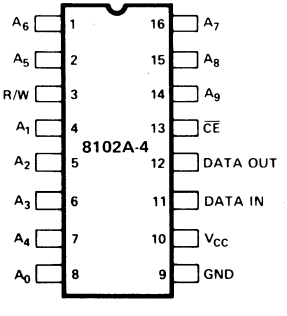
It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel®8102A-4 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

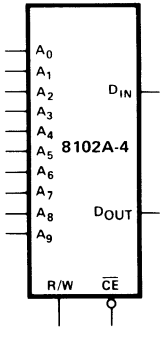
Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

MCS 80/85

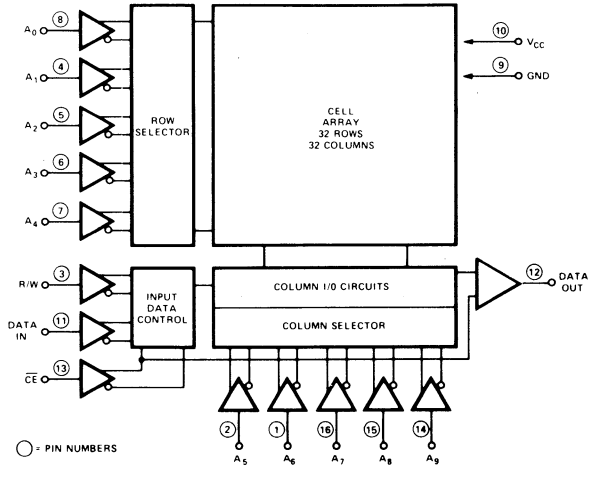
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_{IN}	DATA INPUT	$\overline{CE}$	CHIP ENABLE
A_0-A_9	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	−10°C to 80°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect To Ground	−0.5V to +7V
Power Dissipation	1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

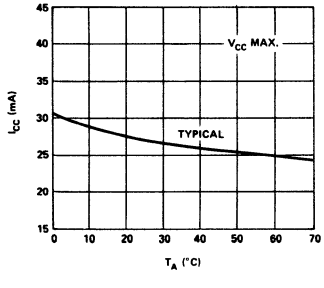
SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	OUTPUT LEAKAGE CURRENT			5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.4 to V_{CC}
I_{LOL}	OUTPUT LEAKAGE CURRENT			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC1}	POWER SUPPLY CURRENT		30	50	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 25°C
I_{CC2}	POWER SUPPLY CURRENT			55	mA	ALL INPUTS = 5.25V DATA OUT OPEN T_A = 0°C
V_{IL}	INPUT "LOW" VOLTAGE	−0.5		0.8	V	
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V_{CC}	V	
V_{OL}	OUTPUT "LOW" VOLTAGE			0.4	V	I_{OL} = 2.1mA
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.4			V	I_{OH} = −100μA

(1) Typical values are for T_A = 25°C and nominal supply voltage.

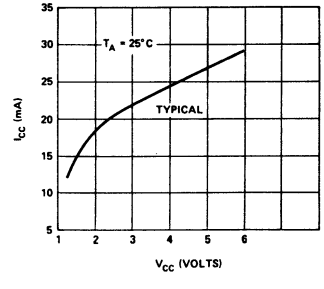
MCS 80/85

TYPICAL D.C. CHARACTERISTICS

POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
READ CYCLE					
t_{RC}	Read Cycle	450			ns
t_A	Access Time			450	ns
t_{CO}	Chip Enable to Output Time			230	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns
WRITE CYCLE					
t_{WC}	Write Cycle	450			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	300			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	300			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	300			ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CONDITIONS OF TEST

Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

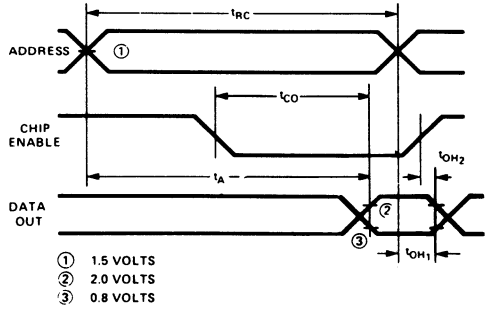
CAPACITANCE [2] T_A = 25°C, f = 1MHz

SYMBOL	TEST	LIMITS (pF)	
		TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

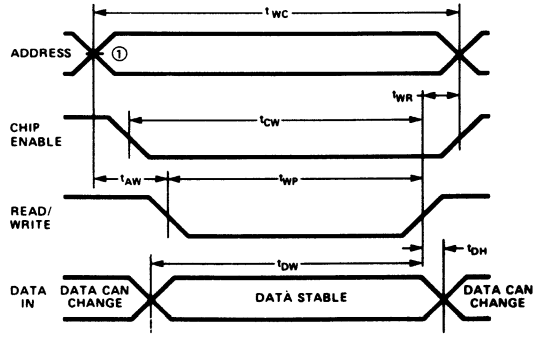
NOTE: 2. This parameter is periodically sampled and is not 100% tested.

WAVEFORMS

READ CYCLE

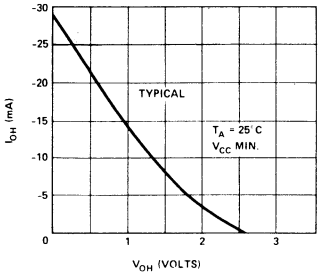


WRITE CYCLE

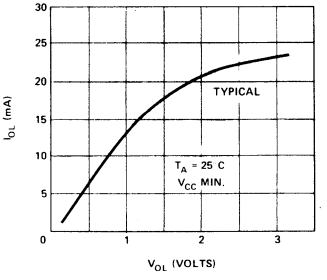


TYPICAL D.C. AND A.C. CHARACTERISTICS

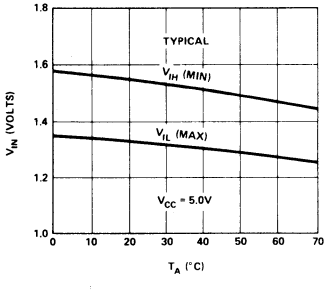
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



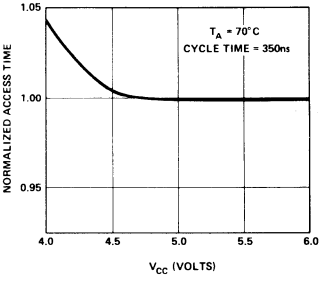
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



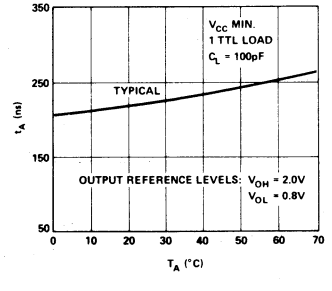
V_{IN} LIMITS VS. TEMPERATURE



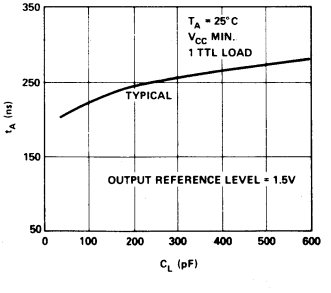
ACCESS TIME VS. V_{CC} NORMALIZED TO V_{CC} = 5.0V



ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



MCS 80/85

8111A-4
1024 BIT STATIC MOS RAM WITH COMMON I/O

* 450 nsec Access Time Maximum
* 256 Word by 4 Bit Organization

- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Powerful Output Drive Capability**
- **Low Cost Packaging: 18 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150mW**
- **Three-State Output: OR-Tie Capability**
- **Output Disable Provided for Ease of Use in Common Data Bus Systems**

The Intel® 8111A-4 is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 8111A-4 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

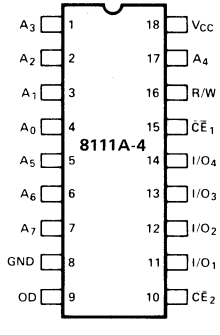
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

The Intel® 8111A-4 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

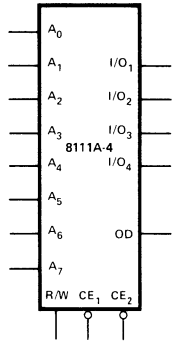
Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

MCS 80/85

PIN CONFIGURATION



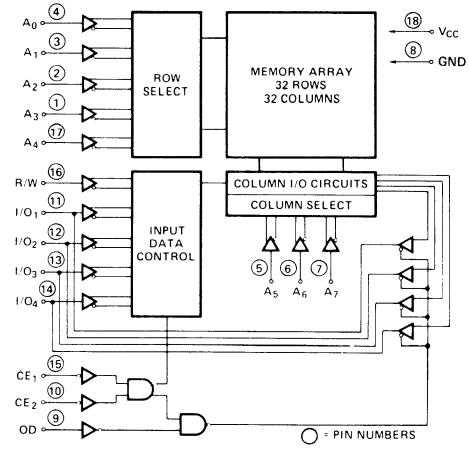
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
$\overline{CE}_2$	CHIP ENABLE 2
I/O_1- I/O_4	DATA INPUT/OUTPUT

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

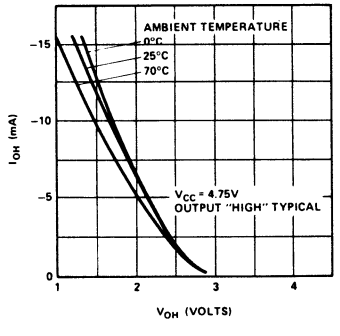
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

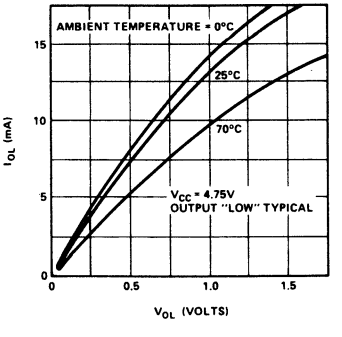
T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current		1	10	µA	Output Disabled, $V_{I/O}$=4.0V
I_{LOL}	I/O Leakage Current		-1	-10	µA	Output Disabled, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current		35	55	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			60	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400µA

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	(See Below)
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	(See Below)
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

A.C. CONDITIONS OF TEST

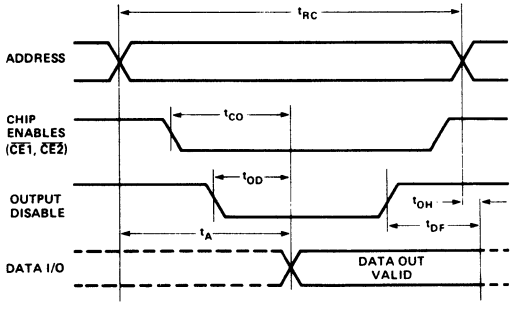
t_r, t_f . . . . . 20 ns
Input Levels . . . . . 0.8V or 2.0V
Timing Reference 1.5V
Load . . . . . 1 TTL Gate and C_L = 100 pF

CAPACITANCE[3] $T_A = 25°C$, f = 1MHz

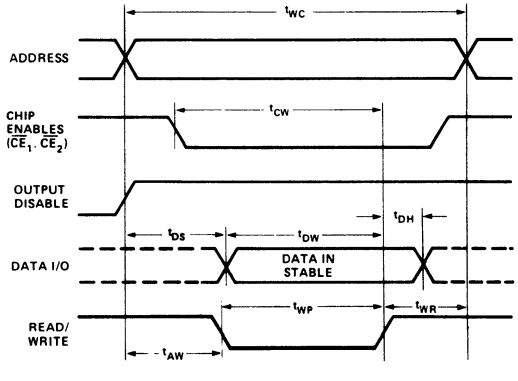
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O} = 0V$	10	15

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.
3. This parameter is periodically sampled and is not 100% tested.

8308
8192 BIT STATIC MOS READ ONLY MEMORY

- **Fast Access Time: 450 ns**
- **Standard Power Supplies: +12V, ±5V**
- **TTL Compatible: All Inputs and Outputs**
- **Programmable Chip Select Input for Easy Memory Expansion**
- **Three-State Output: OR-Tie Capability**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Pin Compatible to 8708 PROM**

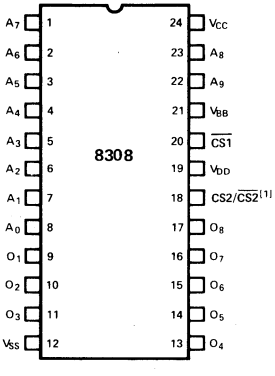
The Intel® 8308 is a 8192 bit static MOS read only memory organized as 1024 words by 8-bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are TTL compatible. The chip select input (CS2/$\overline{CS2}$) is programmable. An active high or low level chip select input can be defined by the designer and the desired chip select logic level is fixed at Intel during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion. The pin compatible UV erasable 8708 PROM is available for initial system prototyping.

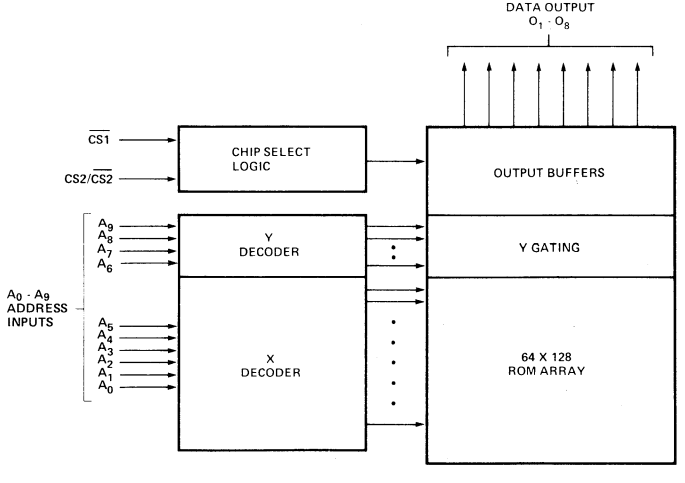
The 8308 read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

MCS 80/85

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}_1$	CHIP SELECT INPUT
CS2/$\overline{CS2}$[1]	PROGRAMMABLE CHIP SELECT INPUT

NOTE 1. The CS2/$\overline{CS2}$ LOGIC LEVELS MUST BE SPECIFIED BY THE USER AS EITHER A LOGIC 1 (V_{IH}) OR LOGIC 0 (V_{IL}). A LOGIC 0 SHOULD BE SPECIFIED IN ORDER TO BE COMPATIBLE WITH THE 8708.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect
To V_{BB} . . . . . -0.3V to 20V
Power Dissipation . . . . . 1.0 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PROGRAMMING

The programming specifications are in the ROM and PROM Programming Instructions (see page 3-55).

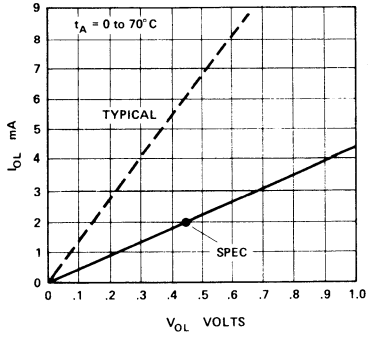
D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5%; V_{DD} = 12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V Unless Otherwise Specified.

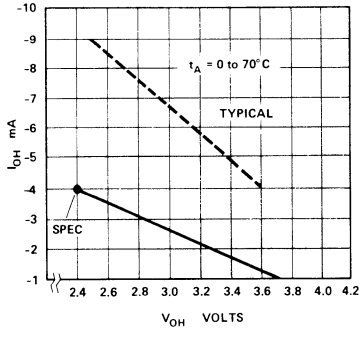
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins Except $\overline{CS_1}$)			±10	μA	V_{IN} = 0 to 5.25V
I_{LCL}	Input Load Current on $\overline{CS_1}$			-1.6	mA	V_{IN} = 0.45V
I_{LPC}	Input Peak Load Current on $\overline{CS_1}$			-4	mA	V_{IN} = 0.8V to 3.3V
I_{LKC}	Input Leakage Current on $\overline{CS_1}$			10	μA	V_{IN} = 3.3V to 5.25V
I_{LO}	Output Leakage Current			10	μA	Chip Deselected
V_{IL}	Input "Low" Voltage	V_{SS}-1		0.8V	V	
V_{IH}	Input "High" Voltage	3.3		V_{CC}+1.0	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2mA
V_{OH1}	Output "High" Voltage	2.4			V	I_{OH} = -4mA
V_{OH2}	Output "High" Voltage	3.7			V	I_{OH} = -1mA
I_{CC}	Power Supply Current V_{CC}		10	15	mA	
I_{DD}	Power Supply Current V_{DD}		32	60	mA	
I_{BB}	Power Supply Current V_{BB}		10μA	1	mA	
P_D	Power Dissipation		460	840	mW	

NOTE 1: Typical values for T_A = 25°C and nominal supply voltage

D.C. OUTPUT CHARACTERISTICS



D.C. OUTPUT CHARACTERISTICS



A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$; $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Specified.

Symbol	Parameter	Limits[2]			Unit
		Min.	Typ.	Max.	
t_{ACC}	Address to Output Delay Time		200	450	ns
t_{CO1}	Chip Select 1 to Output Delay Time		85	160	ns
t_{CO2}	Chip Select 2 to Output Delay Time		125	220	ns
t_{DF}	Chip Deselect to Output Data Float Time		125	220	ns

NOTE 2: Refer to conditions of Test for A.C. Characteristics. Add 50 nanoseconds (worst case) to specified values at $V_{OH} = 3.7V$ @ $I_{OH} = -1mA$, $C_L = 100pF$.

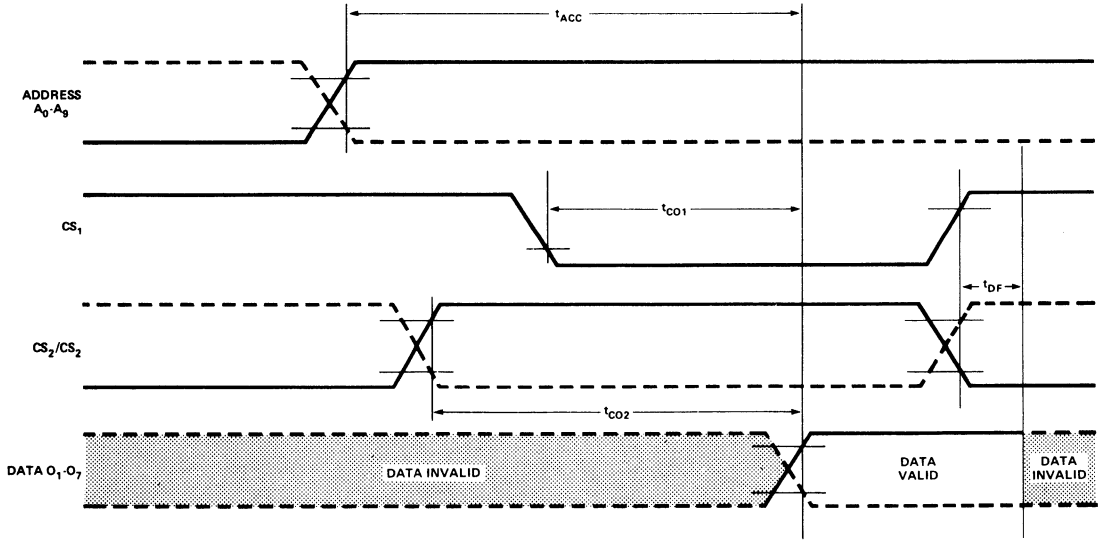
CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . . . 1 TTL Gate, and $C_{LOAD} = 100pF$
Input Pulse Levels . . . . . .65V to 3.3V
Input Pulse Rise and Fall Times . . . . . 20 nsec
Timing Measurement Reference Level
. . . . . 2.4V V_{IH}, V_{OH}; 0.8V V_{IL}, V_{OL}

CAPACITANCE

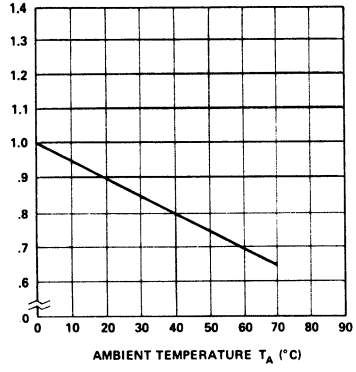
$T_A = 25°C$, f = 1 MHz, $V_{BB} = -5V$, V_{DD}, V_{CC} and all other pins tied to V_{SS}.

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	Input Capacitance		6pF
C_{OUT}	Output Capacitance		12pF

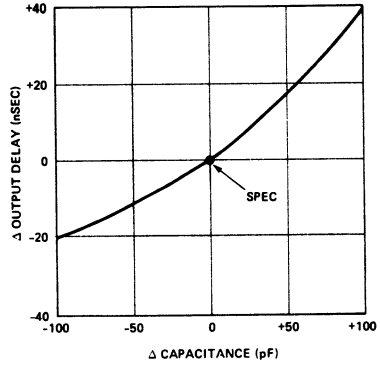


TYPICAL CHARACTERISTICS (Nominal supply voltages unless otherwise noted.)

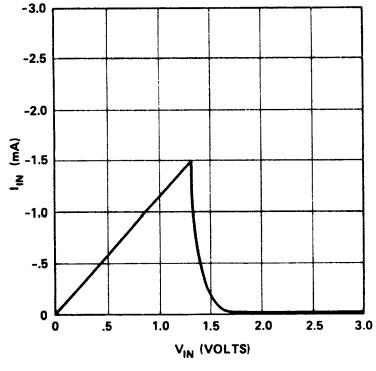
I_{DD} VS. TEMPERATURE (NORMALIZED)



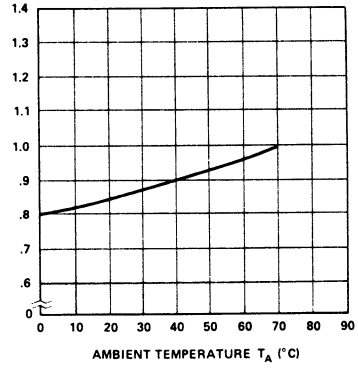
Δ OUTPUT CAPACITANCE VS. Δ OUTPUT DELAY



$\overline{CS_1}$ INPUT CHARACTERISTICS



T_{ACC} VS. TEMPERATURE (NORMALIZED)



8316A
16,384 BIT STATIC MOS READ ONLY MEMORY
Organization—2048 Words x 8 Bits
Access Time-850 ns max

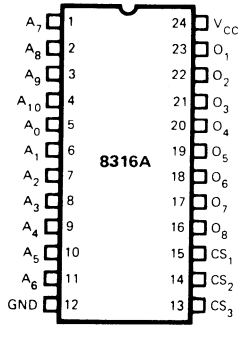
- **Single +5 Volts Power Supply Voltage**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Low Power Dissipation of 31.4 μW/Bit Maximum**
- **Three Programmable Chip Select Inputs for Easy Memory Expansion**
- **Three-State Output — OR-Tie Capability**
- **Fully Decoded — On Chip Address Decode**
- **Inputs Protected — All Inputs Have Protection Against Static Charge**

The Intel® 8316A is a 16,384-bit static MOS read only memory organized as 2048 words by 8 bits. This ROM is designed for microcomputer memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

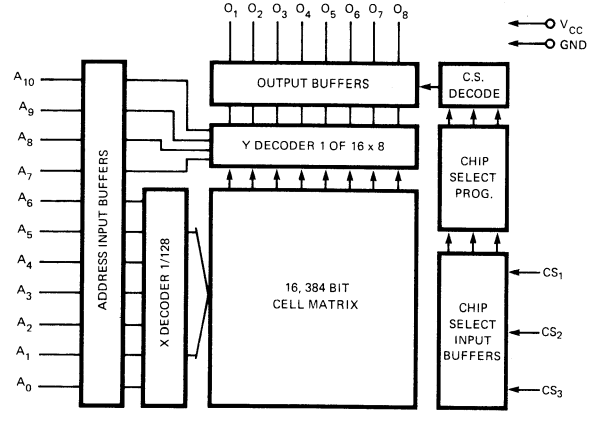
The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and the desired chip select code is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitate easy memory expansion.

The 8316A read only memory is fabricated with N-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single +5V power supply is needed and all devices are directly TTL compatible.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0 A_{10}	ADDRESS INPUTS
O_1 O_8	DATA OUTPUTS
CS_1 CS_3	PROGRAMMABLE CHIP SELECT INPUTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . -0.5V to +7V
Power Dissipation 1.0W

PROGRAMMING: *The programming specifications are in the ROM and PROM Programming Instructions (see page 3-55).*

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

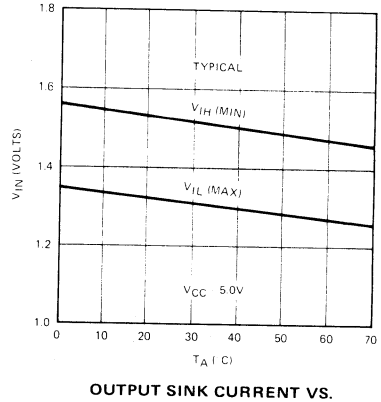
T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	μA	CS = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			-20	μA	CS = 2.2V, V_{OUT} = 0.45V
I_{CC}	Power Supply Current		40	98	mA	All inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}+1.0V	V	
V_{OL}	Output "Low" Voltage			0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -100 μA

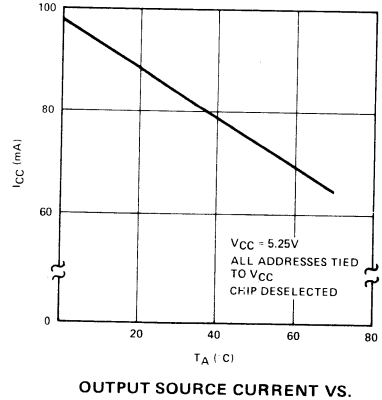
(1) Typical values for T_A = 25°C and nominal supply voltage.

TYPICAL D.C. CHARACTERISTICS

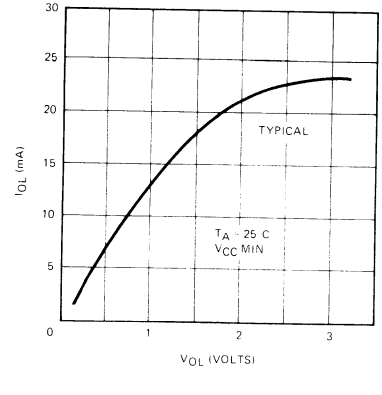
V_{IN} LIMITS VS. TEMPERATURE



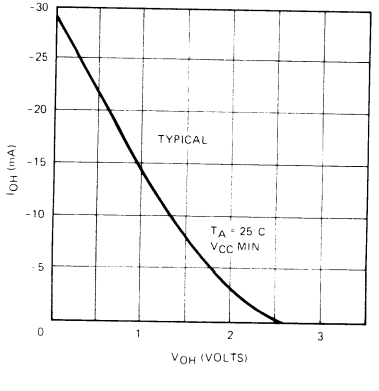
STATIC I_{CC} VS. AMBIENT TEMPERATURE WORST CASE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



A.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = +5V ±5% unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.(1)	MAX.	
t_A	Address to Output Delay Time		400	850	nS
t_{CO}	Chip Select to Output Enable Delay Time			300	nS
t_{DF}	Chip Deselect to Output Data Float Delay Time	0		300	nS

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

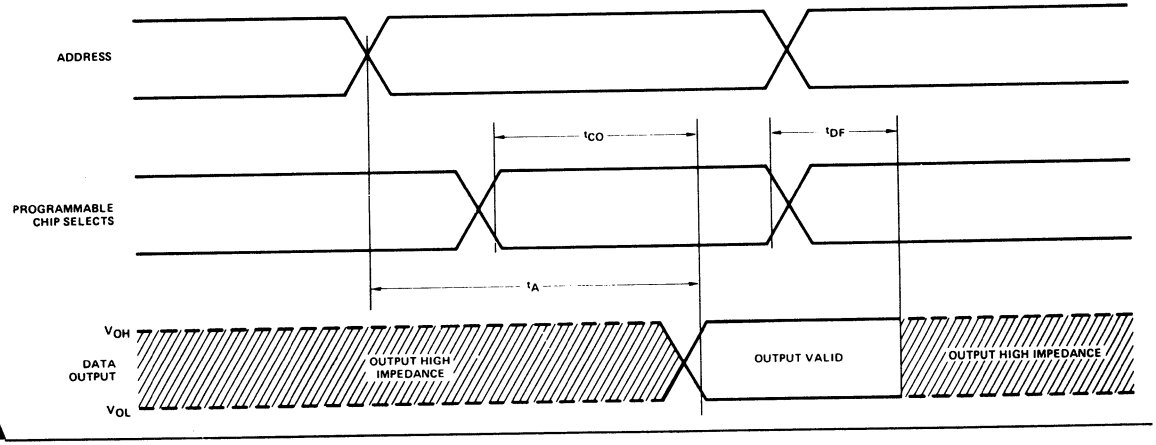
Output Load . . . 1 TTL Gate, and C_{LOAD} = 100 pF
Input Pulse Levels . . . . . 0.8 to 2.0V
Input Pulse Rise and Fall Times .(10% to 90%) 20 nS
Timing Measurement Reference Level
Input 1.5V
Output . . . . . 0.45V to 2.2V

CAPACITANCE (2) T_A = 25°C, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	4 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	8 pF	15 pF

(2) This parameter is periodically sampled and is not 100% tested.

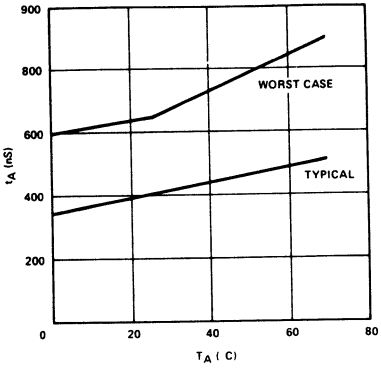
A.C. WAVEFORMS



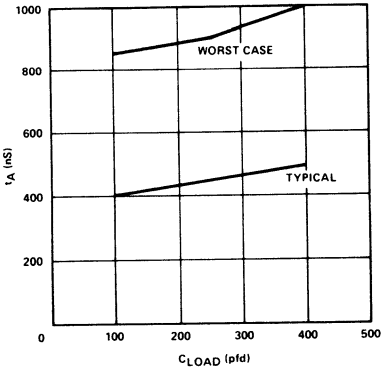
MCS 80 85

TYPICAL A.C. CHARACTERISTICS

ACCESS TIME VS. AMBIENT TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



8708
8192 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

1024x8 Organization

- **Fast Programming — Typ. 100 sec. For All 8K Bits**
- **Low Power During Programming**
- **Access Time — 450 ns**
- **Standard Power Supplies — +12V, ±5V**
- **Static — No Clocks Required**
- **Inputs and Outputs TTL Compatible During Both Read and Program Modes**
- **Three-State Output — OR-Tie Capability**

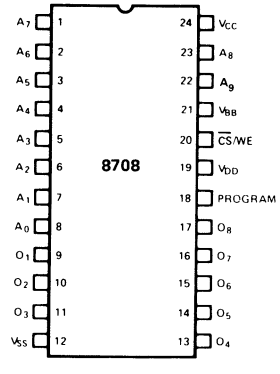
The Intel® 8708 is a high speed 8192 bit erasable and electrically reprogrammable ROM (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

The 8708 is packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

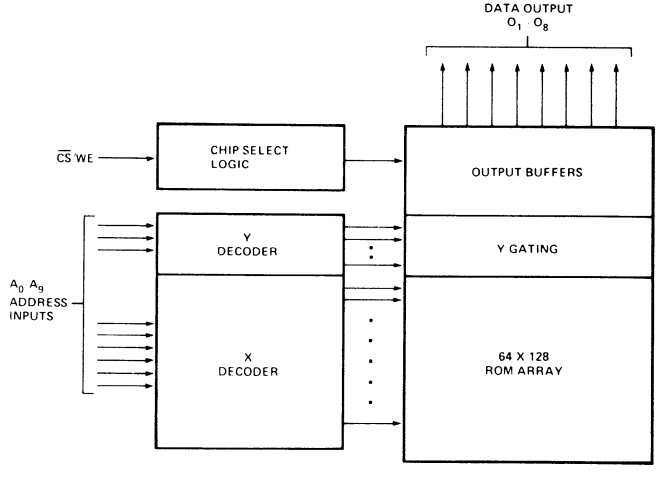
A pin for pin mask programmed ROM, the Intel® 8308, is available for large volume production runs of systems initially using the 8708.

The 8708 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

PIN CONFIGURATION DURING READ OR PROGRAM

	PIN NUMBER						
MODE	9-11, 13-17	12	18	19	20	21	24
READ	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
PROGRAM	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

PROGRAMMING

The programming specifications are identical to those of the 2708. (See ROM and PROM Programming Instructions, page 3-55).

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +125°C
V_{DD} With Respect to V_{BB} . . . . . +20V to -0.3V
V_{CC} and V_{SS} With Respect to V_{BB} . . . . . +15V to -0.3V
All Input or Output Voltages With
Respect to V_{BB} During Read . . . . . +15V to -0.3V
$\overline{CS}$/WE Input With Respect to V_{BB}
During Programming . . . . . +20V to -0.3V
Program Input With Respect to V_{BB} . . . . . +35V to -0 3V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

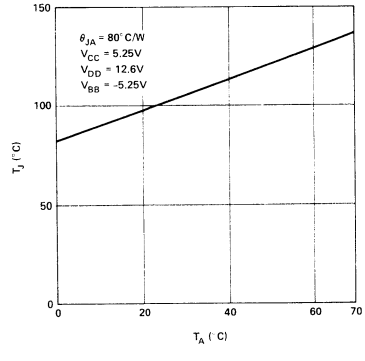
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	V_{IN} = 5.25 V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10	μA	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V
I_{DD}[2]	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}[2]	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}[2]	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. **The total power dissipation of the 8708 is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.**

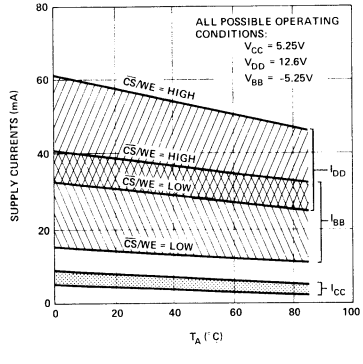
MCS 80/85

TYPICAL D.C. CHARACTERISTICS

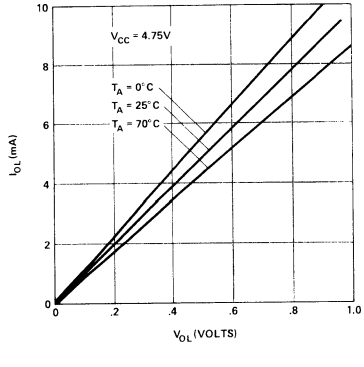
MAXIMUM JUNCTION TEMPERATURE
VS. AMBIENT TEMPERATURE



RANGE OF SUPPLY CURRENTS
VS. TEMPERATURE



OUTPUT SINK CURRENT
VS. OUTPUT VOLTAGE



A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
$t_{\overline{CO}}$	Chip Select to Output Delay		60	120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

CAPACITANCE $T_A = 25°C$, f = 1MHz

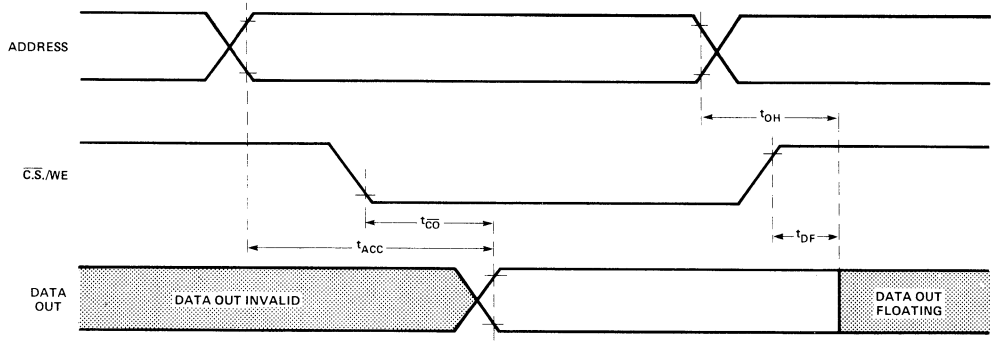
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN}=0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT}=0V$

Note . This parameter is periodically sampled and not 100% tested.

A.C. TEST CONDITIONS

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤20ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

WAVEFORMS



ERASURE CHARACTERISTICS

The erasure characteristics of the 8708 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level flourescent lighting could erase the typical 8708 in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8708 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8708 window to prevent unintentional erasure.

The recommended erasure procedure (see page 3-55) for the 8708 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm^2 power rating. The 8708 should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

8205

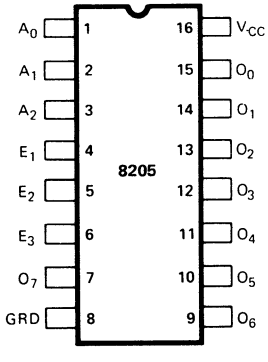
HIGH SPEED 1 OUT OF 8 BINARY DECODER

- **I/O Port or Memory Selector**
- **Simple Expansion — Enable Inputs**
- **High Speed Schottky Bipolar Technology — 18ns Max. Delay**
- **Directly Compatible with TTL Logic Circuits**
- **Low Input Load Current — .25 mA max., 1/6 Standard TTL Input Load**
- **Minimum Line Reflection — Low Voltage Diode Input Clamp**
- **Outputs Sink 10 mA min.**
- **16-Pin Dual-In-Line Ceramic or Plastic Package**

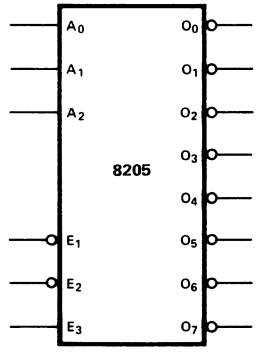
The 8205 decoder can be used for expansion of systems which utilize input ports, output ports, and memory components with active low chip select input. When the 8205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 8205 allow easy system expansion. For very large systems, 8205 decoders can be cascaded such that each decoder can drive eight other decoders for arbitrary memory expansions.

The Intel® 8205 is packaged in a standard 16 pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A_0-A_2	ADDRESS INPUTS
$\overline{E_1}$, $\overline{E_3}$	ENABLE INPUTS
$\overline{O_0}$-$\overline{O_7}$	DECODED OUTPUTS

ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

FUNCTIONAL DESCRIPTION

Decoder

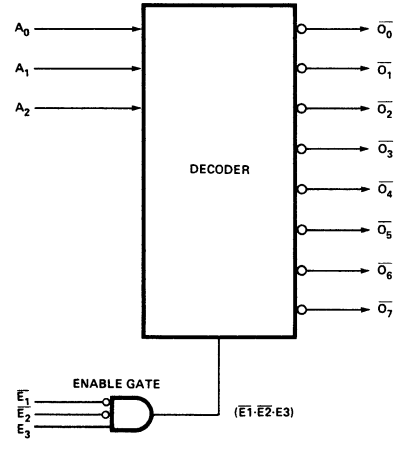
The 8205 contains a one out of eight binary decoder. It accepts a three bit binary code and by gating this input, creates an exclusive output that represents the value of the input code.

For example, if a binary code of 101 was present on the A0, A1 and A2 address input lines, and the device was enabled, an active low signal would appear on the $\overline{O5}$ output line. Note that all of the other output pins are sitting at a logic high, thus the decoded output is said to be exclusive. The decoders outputs will follow the truth table shown below in the same manner for all other input variations.

Enable Gate

When using a decoder it is often necessary to gate the outputs with timing or enabling signals so that the exclusive output of the decoded value is synchronous with the overall system.

The 8205 has a built-in function for such gating. The three enable inputs ($\overline{E1}$, $\overline{E2}$, E3) are ANDed together and create a single enable signal for the decoder. The combination of both active "high" and active "low" device enable inputs provides the designer with a powerfully flexible gating function to help reduce package count in his system.



ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

APPLICATIONS OF THE 8205

The 8205 can be used in a wide variety of applications in microcomputer systems. I/O ports can be decoded from the address bus, chip select signals can be generated to select memory devices and the type of machine state such as in 8008 systems can be derived from a simple decoding of the state lines (S0, S1, S2) of the 8008 CPU.

I/O Port Decoder

Shown in the figure below is a typical application of the 8205. Address input lines are decoded by a group of 8205s (3). Each input has a binary weight. For example, A0 is assigned a value of 1 and is the LSB; A4 is assigned a value of 16 and is the MSB. By connecting them to the decoders as shown, an active low signal that is exclusive in nature and represents the value of the input address lines, is available at the outputs of the 8205s.

This circuit can be used to generate enable signals for I/O ports or any other decoder related application.

Note that no external gating is required to decode up to 24 exclusive devices and that a simple addition of an inverter or two will allow expansion to even larger decoder networks.

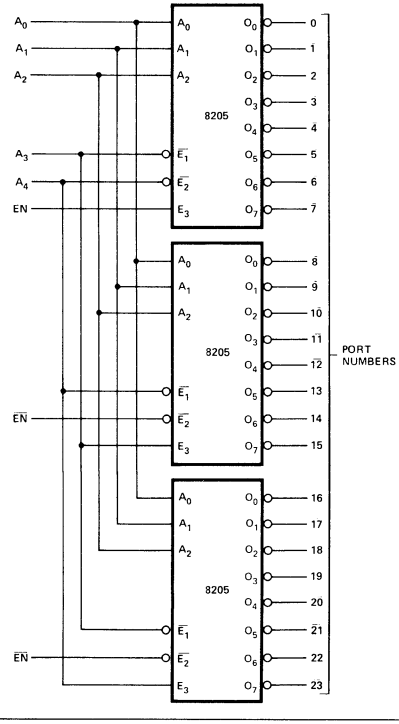
Chip Select Decoder

Using a very similar circuit to the I/O port decoder, an array of 8205s can be used to create a simple interface to a 24K memory system.

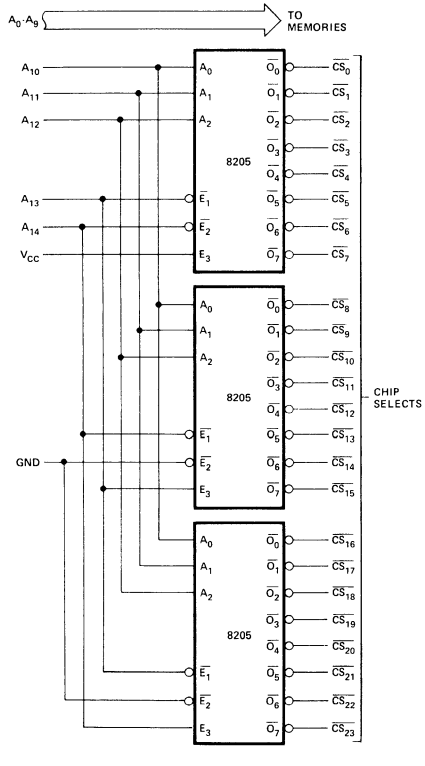
The memory devices used can be either ROM or RAM and are 1K in storage capacity. 8308s and 8102s are the devices typically used for this application. This type of memory device has ten (10) address inputs and an active "low" chip select ($\overline{CS}$). The lower order address bits A0-A9 which come from the microprocessor are "bussed" to all memory elements and the chip select to enable a specific device or group of devices comes from the array of 8205s. The output of the 8205 is active low so it is directly compatible with the memory components.

Basic operation is that the CPU issues an address to identify a specific memory location in which it wishes to "write" or "read" data. The most significant address bits A10-A14 are decoded by the array of 8205s and an exclusive, active low, chip select is generated that enables a specific memory device. The least significant address bits A0-A9 identify a specific location within the selected device. Thus, all addresses throughout the entire memory array are exclusive in nature and are non-redundant.

This technique can be expanded almost indefinitely to support even larger systems with the addition of a few inverters and an extra decoder (8205).



I/O Port Decoder



24K Memory Interface

Logic Element Example

Probably the most overlooked application of the 8205 is that of a general purpose logic element. Using the "on-chip" enabling gate, the 8205 can be configured to gate its decoded outputs with system timing signals and generate strobes that can be directly connected to latches, flip-flops and one-shots that are used throughout the system.

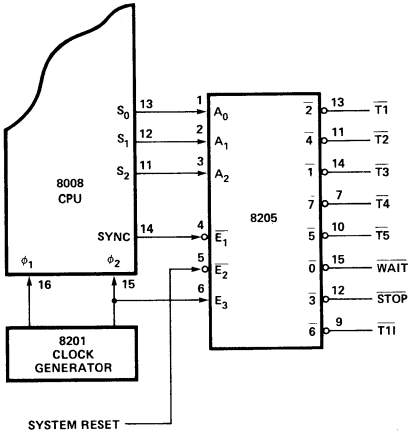
An excellent example of such an application is the "state decoder" in an 8008 CPU based system. The 8008 CPU issues three bits of information (S0, S1, S2) that indicate the nature of the data on the Data Bus during each machine state. Decoding of these signals is vital to generate strobes that can load the address latches, control bus discipline and general machine functions.

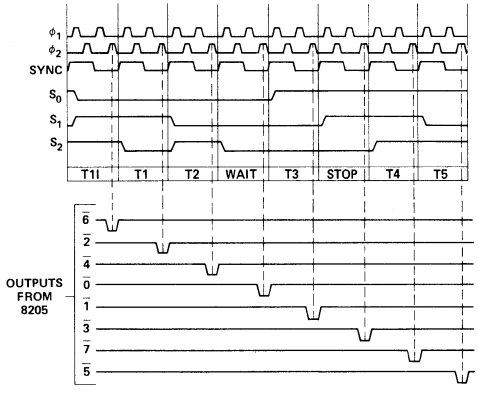
In the figure below a circuit is shown using the 8205 as the "state decoder" for an 8008 CPU that not only decodes the S0, S1, S2 outputs but gates these signals with the clock (phase 2) and the SYNC output of the 8008 CPU. The $\overline{T1}$ and $\overline{T2}$ decoded strobes can connect directly to devices like 8212s for latching the address information. The other decoded strobes can be used to generate signals to control the system data bus, memory timing functions and interrupt structure. RESET is connected to the enable gate so that strobes are not generated during system reset, eliminating accidental loading.

The power of such a circuit becomes evident when a single decoded strobe is logically broken down. Consider $\overline{T1}$ output, the boolean equation for it would be:

$$\overline{T1} = (\overline{S0} \cdot S1 \cdot \overline{S2}) \cdot (\overline{SYNC} \cdot \text{Phase } 2 \cdot \overline{\text{Reset}})$$

A six input NAND gate plus a few inverters would be needed to implement this function. The seven remaining outputs would need a similar circuit to duplicate their function, obviously a substantial savings in components can be achieved when using such a technique.





State Control Coding

S_0	S_1	S_2	STATE
0	1	0	T1
0	1	1	T1I
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOP
1	1	1	T4
1	0	1	T5

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		125 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

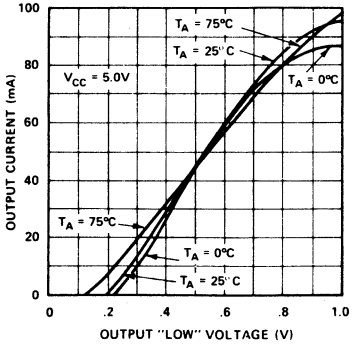
D.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

8205

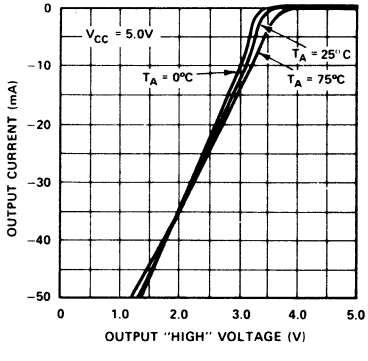
SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT		−0.25	mA	V_{CC} = 5.25V, V_F = 0.45V
I_R	INPUT LEAKAGE CURRENT		10	μA	V_{CC} = 5.25V, V_R = 5.25V
V_C	INPUT FORWARD CLAMP VOLTAGE		−1.0	V	V_{CC} = 4.75V, I_C = −5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} = 4.75V, I_{OL} = 10.0 mA
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	V_{CC} = 4.75V, I_{OH} = −1.5 mA
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} = 5.0V
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	−40	−120	mA	V_{CC} = 5.0V, V_{OUT} = 0V
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	V_{CC} = 5.0V, I_{OX} = 40 mA
I_{CC}	POWER SUPPLY CURRENT		70	mA	V_{CC} = 5.25V

TYPICAL CHARACTERISTICS

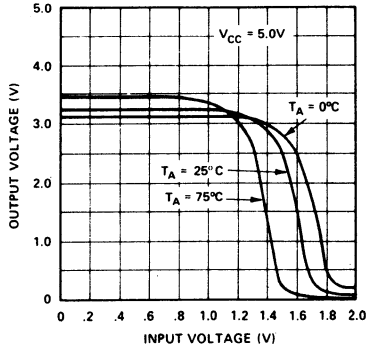
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



DATA TRANSFER FUNCTION



SWITCHING CHARACTERISTICS

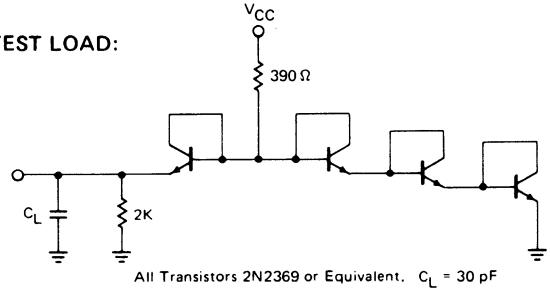
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

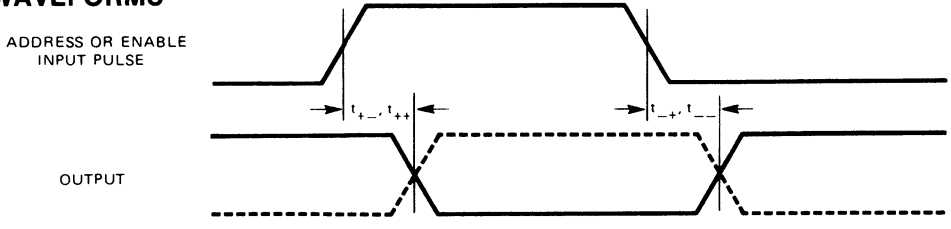
Measurements are made at 1.5V

TEST LOAD:



All Transistors 2N2369 or Equivalent. C_L = 30 pF

TEST WAVEFORMS



A.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = 5.0V ±5% unless otherwise specified.

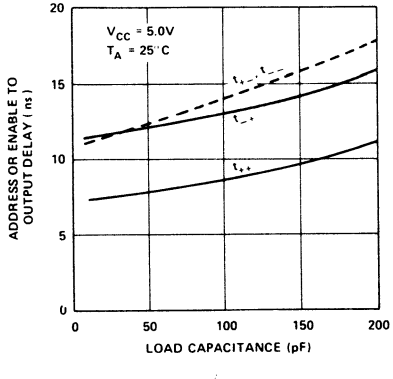
SYMBOL	PARAMETER		MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY		18	ns	
t_{-+}			18	ns	
t_{+-}			18	ns	
t_{--}			18	ns	
C_{IN} (1)	INPUT CAPACITANCE	P8205	4(typ.)	pF	f = 1 MHz, V_{CC} = 0V
		C8205	5(typ.)	pF	V_{BIAS} = 2.0V, T_A = 25°C

1. This parameter is periodically sampled and is not 100% tested.

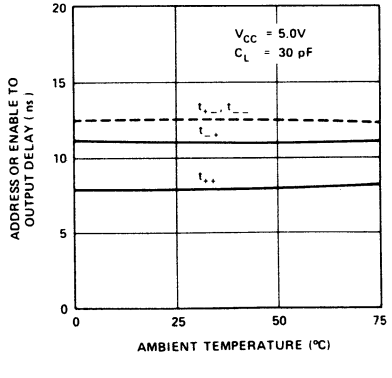
MCS 80/85

TYPICAL CHARACTERISTICS

ADDRESS OR ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



8212

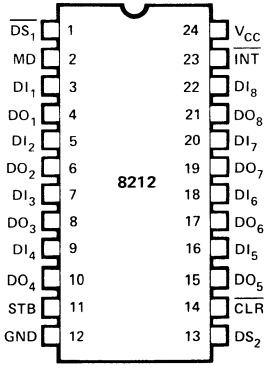
EIGHT-BIT INPUT/OUTPUT PORT

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — .25 mA Max.
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080 CPU or 8008 CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

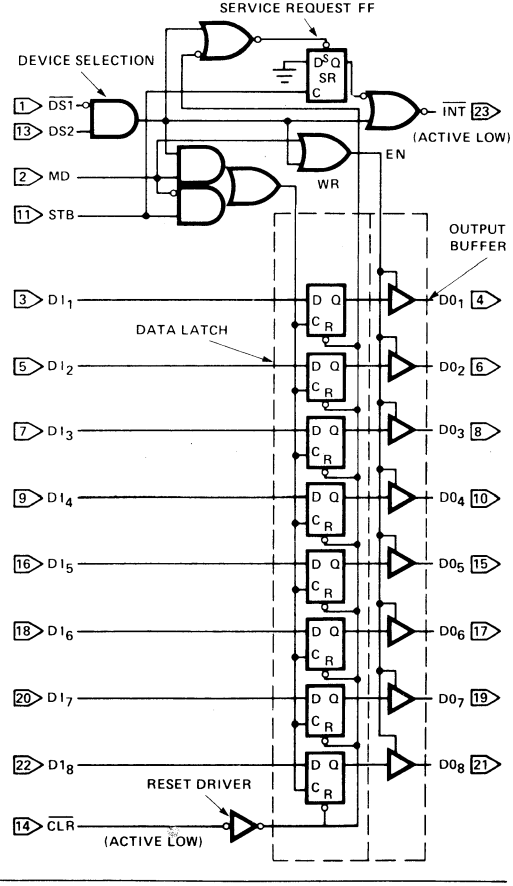
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



MCS 80/85

FUNCTIONAL DESCRIPTION

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

This high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS1}$, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

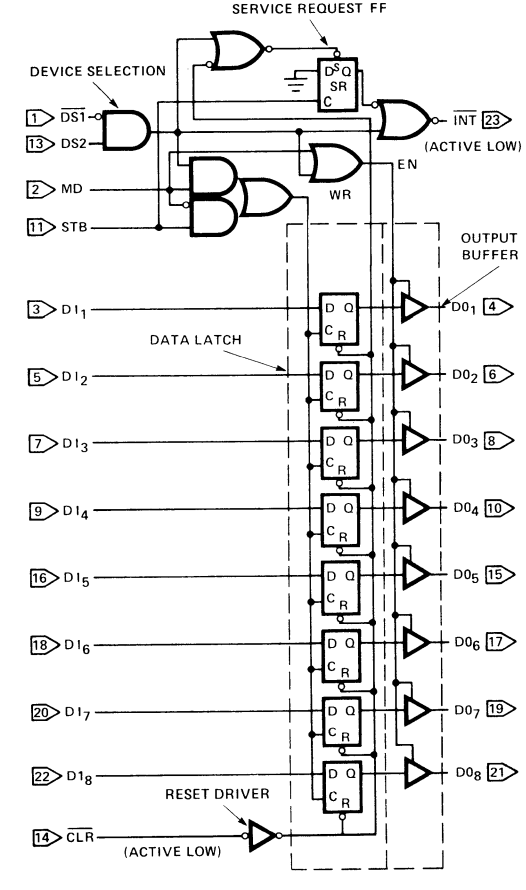
This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS1} \cdot DS2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.



STB	MD	($\overline{DS_1}$·DS_2)	DATA OUT EQUALS
0	0	0	3-STATE
1	0	0	3-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
0	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

CLR	($\overline{DS_1}$·DS_2)	STB	*SR	INT
0	0	0	1	1
0	1	0	1	0
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↓	1	0

*INTERNAL SR FLIP-FLOP

$\overline{CLR}$ – RESETS DATA LATCH
SETS SR FLIP-FLOP
(NO EFFECT ON OUTPUT BUFFER)

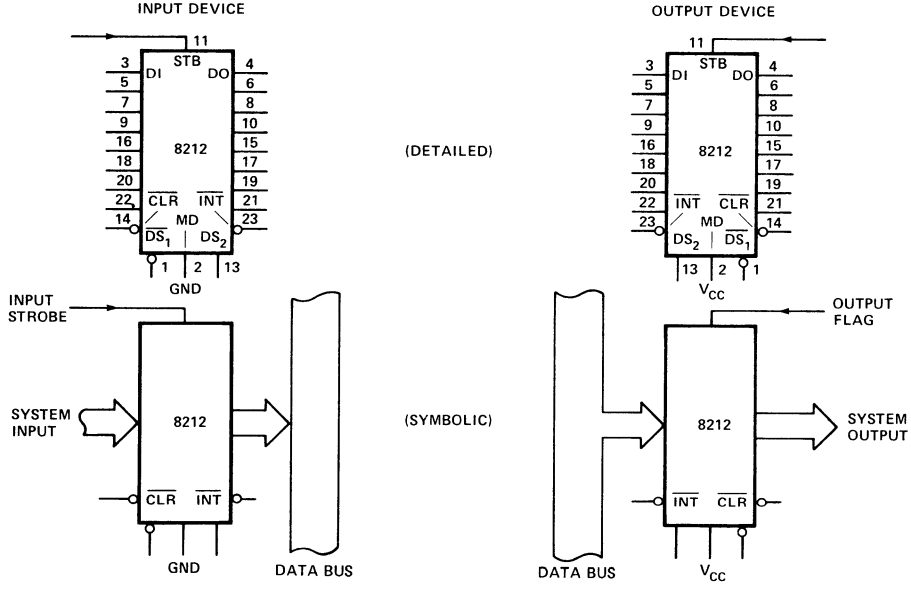
MCS 80/85

Applications Of The 8212 -- For Microcomputer Systems

I. Basic Schematic Symbols

Two examples of ways to draw the 8212 on system schematics—(1) the top being the detailed view showing pin numbers, and (2) the bottom being the symbolic view showing the system input or output as a system bus (bus containing 8 parallel lines). The output to the data bus is symbolic in referencing 8 parallel lines.

BASIC SCHEMATIC SYMBOLS



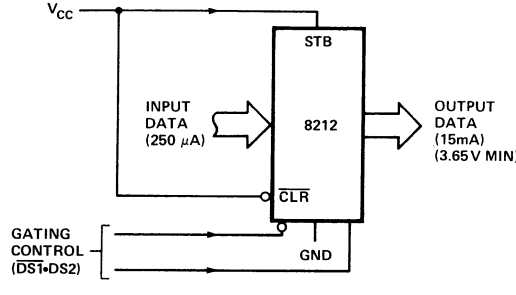
II. Gated Buffer (3 - STATE)

The simplest use of the 8212 is that of a gated buffer. By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS1}$ and DS2.

When the device selection logic is false, the outputs are 3-state.

When the device selection logic is true, the input data from the system is directly transferred to the output. The input data load is 250 micro amps. The output data can sink 15 milli amps. The minimum high output is 3.65 volts.

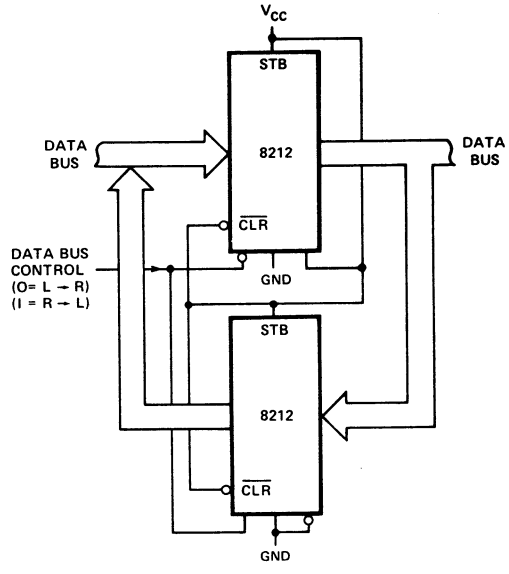
GATED BUFFER
3-STATE



III. Bi-Directional Bus Driver

A pair of 8212's wired (back-to-back) can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS1}$ on the first 8212 and to DS2 on the second. One device is active, and acting as a straight through buffer the other is in 3-state mode. This is a very useful circuit in small system design.

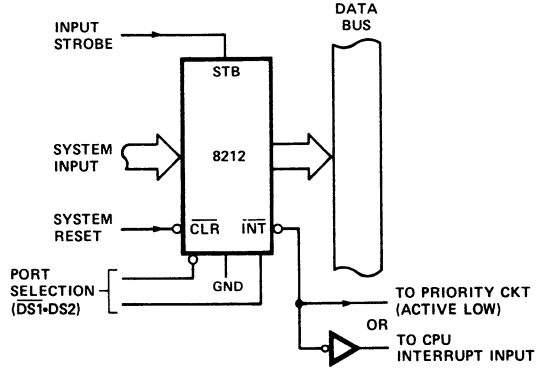
BI-DIRECTIONAL BUS DRIVER



IV. Interrupting Input Port

This use of an 8212 is that of a system input port that accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true — enabling the system input data onto the data bus.

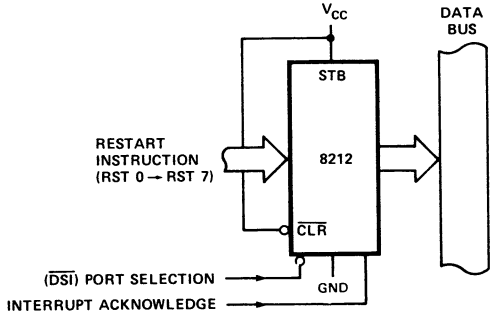
INTERRUPTING INPUT PORT



V. Interrupt Instruction Port

The 8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).

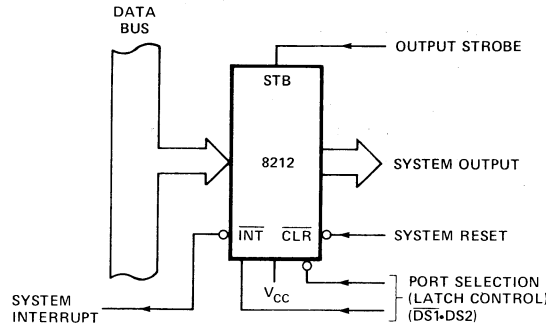
INTERRUPT INSTRUCTION PORT



VI. Output Port (With Hand-Shaking)

The 8212 can be used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of data. The selection of the port comes from the device selection logic. ($\overline{DS1} \cdot DS2$)

OUTPUT PORT (WITH HAND-SHAKING)



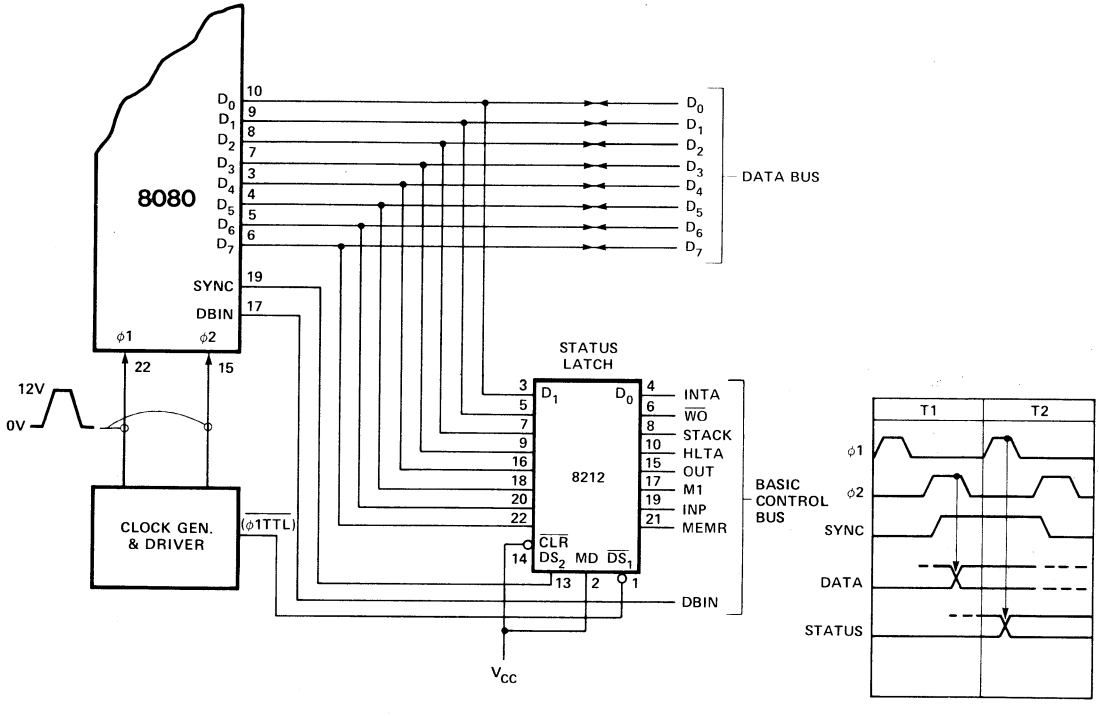
VII. 8080 Status Latch

Here the 8212 is used as the status latch for an 8080 microcomputer system. The input to the 8212 latch is directly from the 8080 data bus. Timing shows that when the SYNC signal is true, which is connected to the DS2 input and the phase 1 signal is true, which is a TTL level coming from the clock generator; then, the status data will be latched into the 8212.

Note: The mode signal is tied high so that the output on the latch is active and enabled all the time.

It is shown that the two areas of concern are the bidirectional data bus of the microprocessor and the control bus.

8080 STATUS LATCH



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias Plastic . . −65°C to +75°C
Storage Temperature . . . . . −65°C to +160°C
All Output or Supply Voltages . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −1.0 to 5.5 Volts
Output Currents . . . . . 125 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

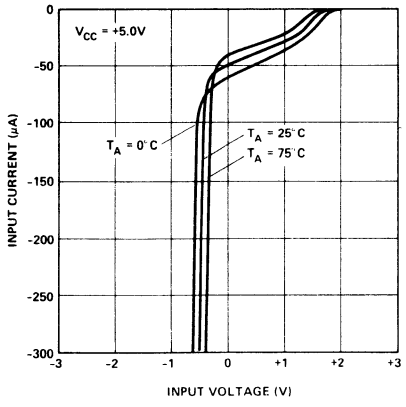
D.C. CHARACTERISTICS

T_A = 0°C to +75°C V_{CC} = +5V ±5%

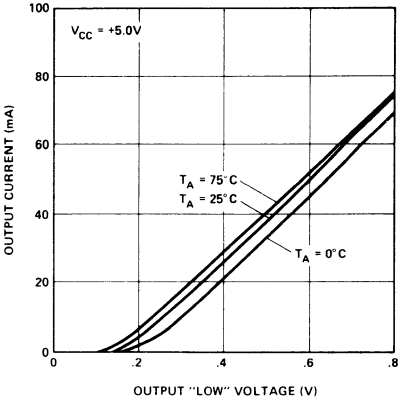
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current ACK, DS_2, CR, DI_1-DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	V_R = 5.25V
I_R	Input Leakage Current MO Input			30	μA	V_R = 5.25V
I_R	Input Leakage Current DS_1 Input			40	μA	V_R = 5.25V
V_C	Input Forward Voltage Clamp			−1	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 15 mA
V_{OH}	Output "High" Voltage	3.65	4.0		V	I_{OH} = −1 mA
I_{SC}	Short Circuit Output Current	-15		-75	mA	V_O = 0 V
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	V_O = .45V/5.25V
I_{CC}	Power Supply Current		90	130	mA	

TYPICAL CHARACTERISTICS

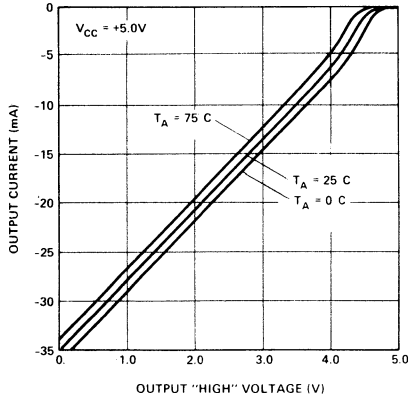
INPUT CURRENT VS. INPUT VOLTAGE



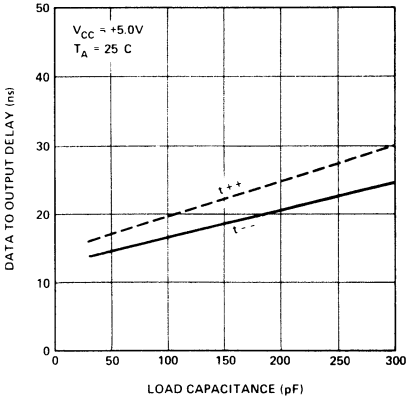
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



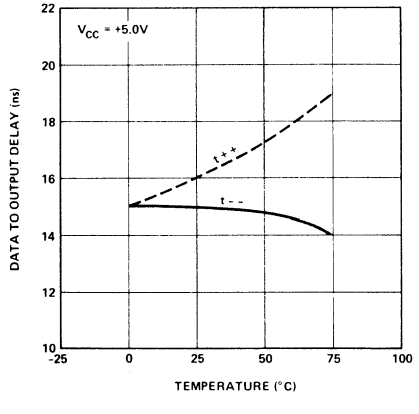
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



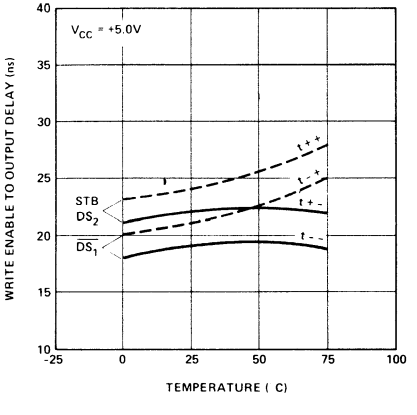
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



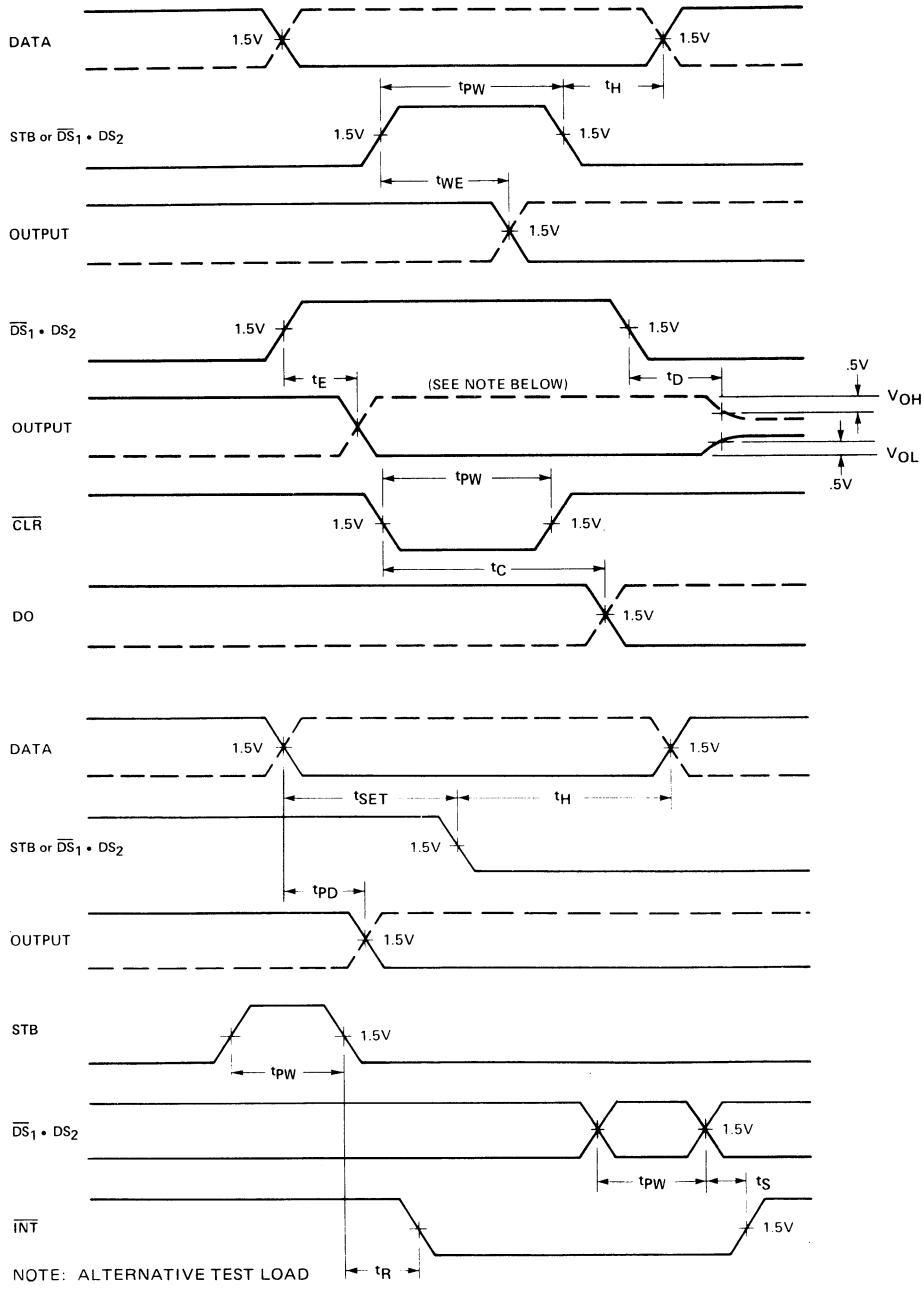
DATA TO OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



TIMING DIAGRAM



A.C. CHARACTERISTICS

T_A = 0°C to +75°C V_{CC} = +5V ± 5%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{pw}	Pulse Width	30			ns	
t_{pd}	Data To Output Delay			30	ns	
t_{we}	Write Enable To Output Delay			40	ns	
t_{set}	Data Setup Time	15			ns	
t_h	Data Hold Time	20			ns	
t_r	Reset To Output Delay			40	ns	
t_s	Set To Output Delay			30	ns	
t_e	Output Enable/Disable Time			45	ns	
t_c	Clear To Output Delay			55	ns	

CAPACITANCE* F = 1 MHz V_{BIAS} = 2.5V V_{CC} = +5V T_A = 25°C

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	DS_1 MD Input Capacitance	9 pF	12 pF
C_{IN}	DS_2, CK, ACK, DI_1-DI_8 Input Capacitance	5 pF	9 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8 pF	12 pF

*This parameter is sampled and not 100% tested.

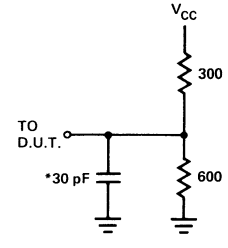
MCS 80/85

SWITCHING CHARACTERISTICS

CONDITIONS OF TEST

Input Pulse Amplitude ≐ 2.5 V
Input Rise and Fall Times 5 ns
Between 1V and 2V Measurements made at 1.5V
with 15 mA & 30 pF Test Load

TEST LOAD
15mA & 30pF



* INCLUDING JIG & PROBE CAPACITANCE

MILITARY TEMP.

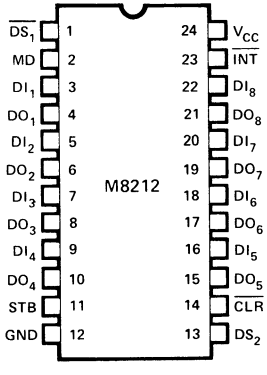
M8212
EIGHT-BIT INPUT/OUTPUT PORT

- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current: .25 mA Max.**
- **Three-State Outputs**
- **Full Military Temperature Range -55°C To +125°C**
- **3.4V Output High Voltage for Direct Interface to M8080A CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches and Multiplexers in Microcomputer Systems**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**
- **24-Pin Dual In-Line Package**

The M8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

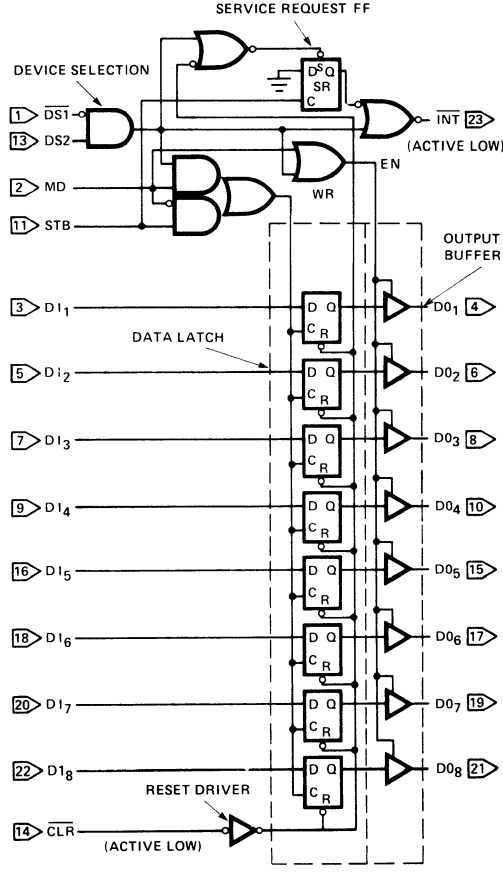
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



MCS-80/85

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +160°C
All Output or Supply Voltages .... −0.5 to +7 Volts
All Input Voltages ..... −1.0 to 5.5 Volts
Output Currents ..... 125 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current ACK, DS_2, CR, DI_1-DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	V_R = V_{CC}
I_R	Input Leakage Current MD Input			30	μA	V_R = V_{CC}
I_R	Input Leakage Current DS_1 Input			40	μA	V_R = V_{CC}
V_C	Input Forward Voltage Clamp			−1.2	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.80	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 10mA
V_{OH}	Output "High" Voltage	3.4	4.0		V	I_{OH} = -.5mA
I_{OS}	Short Circuit Output Current	-15		-75	mA	V_{CC} = 5.0V
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current		90	145	mA	

A.C. CHARACTERISTICS

T_A = -55°C to +125°C V_{CC} = +5V ±10%

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
t_{PW}	Pulse Width	40		ns	
t_{PD}	Data To Output Delay		30	ns	NOTE 1
t_{WE}	Write Enable To Output Delay		50	ns	NOTE 1
t_{SET}	Data Setup Time	20		ns	
t_H	Data Hold Time	30		ns	
t_R	Reset To Output Delay		55	ns	NOTE 1
t_S	Set To Output Delay		35	ns	NOTE 1
t_E	Output Enable/Disable Time		50	ns	NOTE 1
t_C	Clear To Output Delay		65	ns	NOTE 1

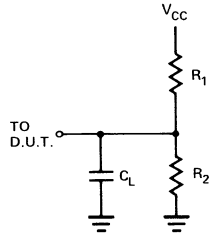
CAPACITANCE F = 1MHz V_{BIAS} = 2.5V V_{CC} = +5V T_A = 25°C

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	$\overline{DS_1}$ MD Input Capacitance	9 pF	12 pF
C_{IN}	DS_2, $\overline{CLR}$, STB, DI_1-DI_8 Input Capacitance	5 pF	9 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8 pF	12 pF

SWITCHING CHARACTERISTICS

CONDITIONS OF TEST
Input Pulse Amplitude = 2.5V
Input Rise and Fall Times: 5 ns between 1V and 2V

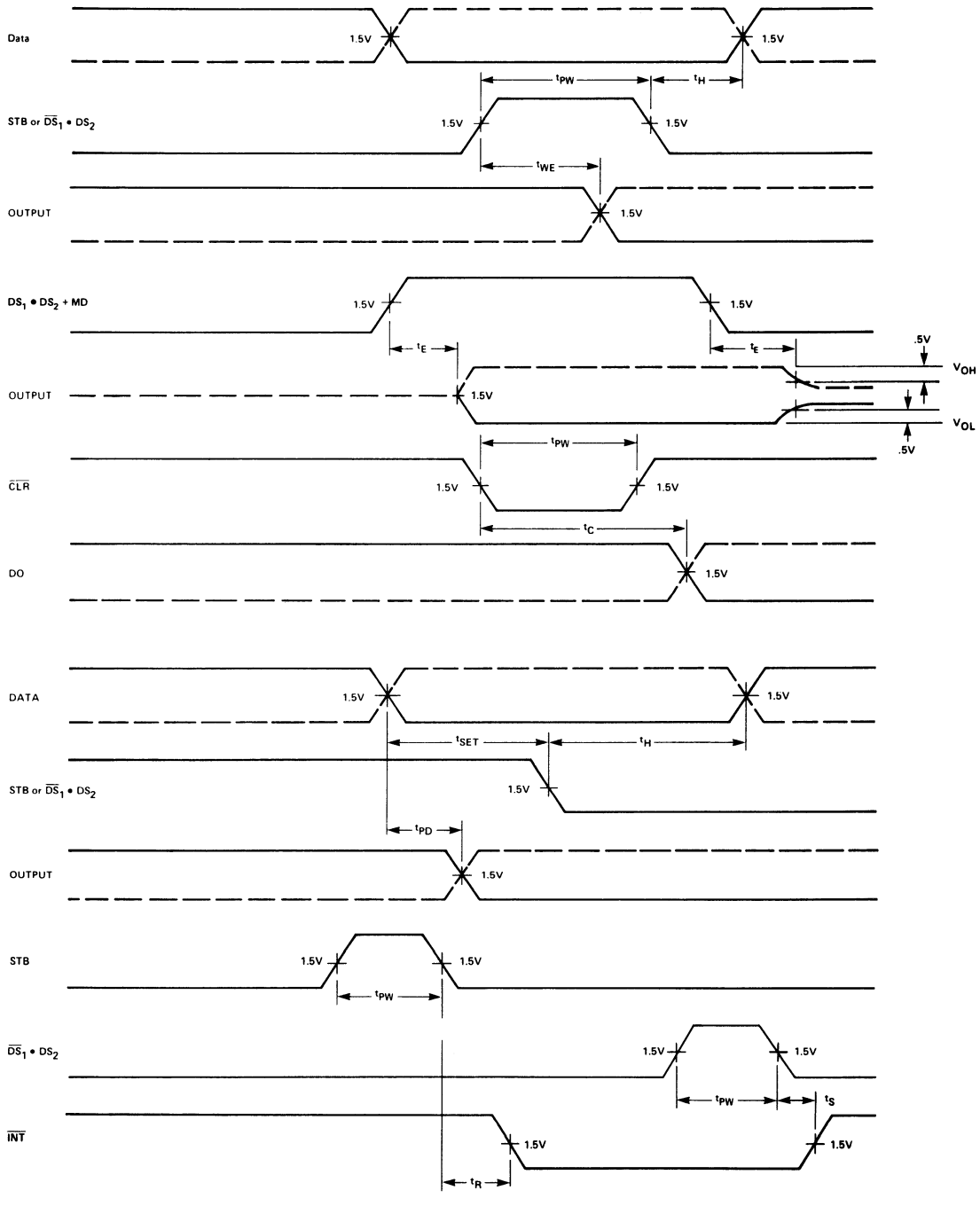
TEST LOAD



NOTE 1:

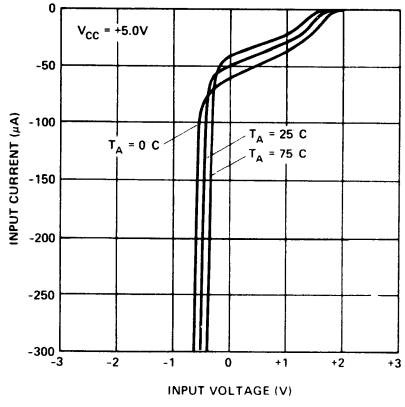
TEST	C_L	R_1	R_2
t_{PD}, t_{WE}, t_R, t_S, t_C	30pF	300Ω	600Ω
t_E, ENABLE↑	30pF	10KΩ	1KΩ
t_E, ENABLE↓	30pF	300Ω	600Ω
t_E, DISABLE↑	5pF	300Ω	600Ω
t_E, DISABLE↓	5pF	10KΩ	1KΩ

TIMING DIAGRAM

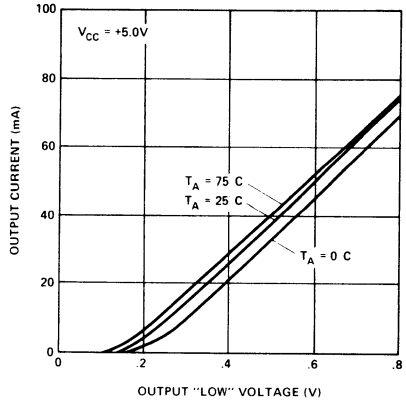


TYPICAL CHARACTERISTICS

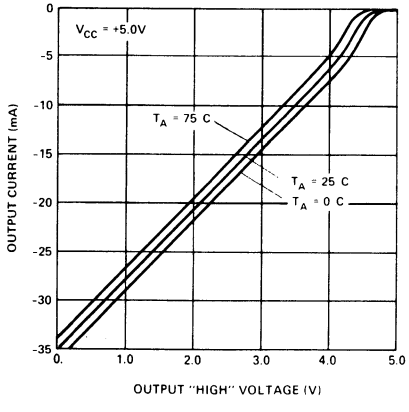
INPUT CURRENT VS. INPUT VOLTAGE



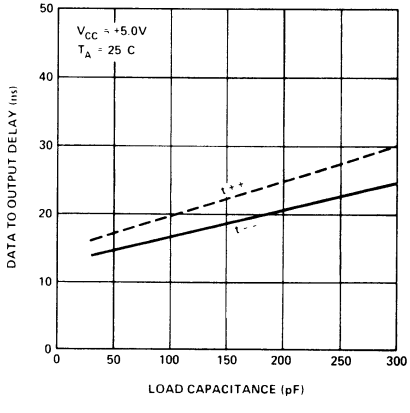
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



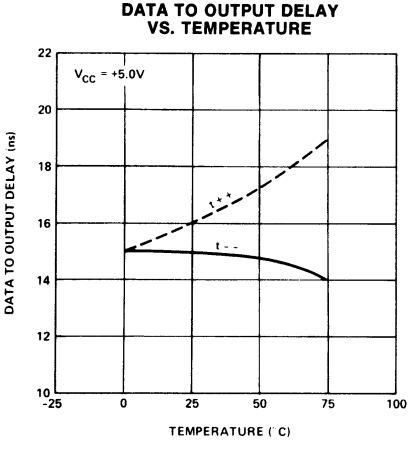
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



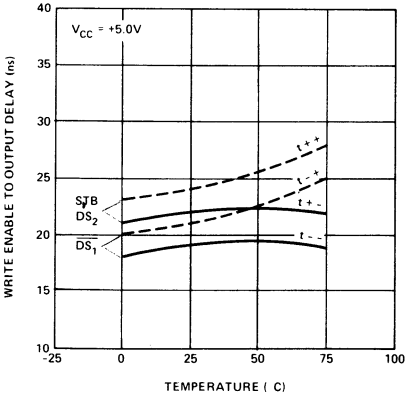
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA TO OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



8214
PRIORITY INTERRUPT CONTROL UNIT

- **Eight Priority Levels**
- **Current Status Register**
- **Priority Comparator**
- **Fully Expandable**
- **High Performance (50ns)**
- **24-Pin Dual In-Line Package**

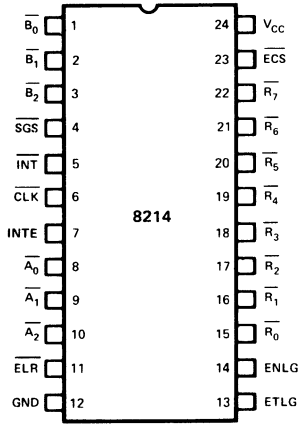
The 8214 is an eight level priority interrupt control unit designed to simplify interrupt driven microcomputer systems.

The PICU can accept eight requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector information to identify the service routine.

The 8214 is fully expandable by the use of open collector interrupt output and vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt driven microcomputer systems.

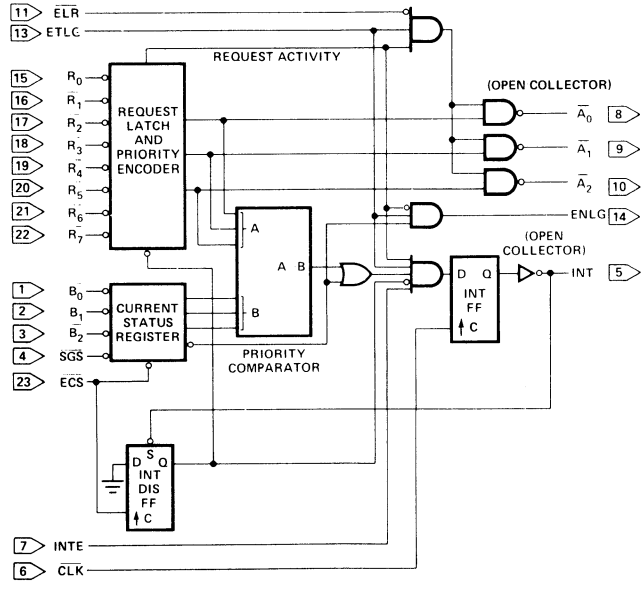
PIN CONFIGURATION



PIN NAMES

INPUTS		
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)	
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS	
$\overline{SGS}$	STATUS GROUP SELECT	
$\overline{ECS}$	ENABLE CURRENT STATUS	
INTE	INTERRUPT ENABLE	
$\overline{CLK}$	CLOCK (INT F-F)	
$\overline{ELR}$	ENABLE LEVEL READ	
ETLG	ENABLE THIS LEVEL GROUP	
OUTPUTS:		
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS	OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT. LOW)	OPEN COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP	

LOGIC DIAGRAM



D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 100 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T_A = 0°C to +70°C, V_{CC} = 5V ±5%.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage (all inputs)			-1.0	V	I_C=-5mA
I_F	Input Forward Current: ETLG input all other inputs		-.15 -.08	-0.5 -0.25	mA mA	V_F=0.45V
I_R	Input Reverse Current: ETLG input all other inputs			80 40	μA μA	V_R=5.25V
V_{IL}	Input LOW Voltage: all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage: all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current		90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage: all outputs		.3	.45	V	I_{OL}=15mA
V_{OH}	Output HIGH Voltage: ENLG output	2.4	3.0		V	I_{OH}=-1mA
I_{OS}	Short Circuit Output Current: ENLG output	-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
I_{CEX}	Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$-$\overline{A_2}$			100	μA	V_{CEX}=5.25V

NOTES:
1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
t_{CY}	$\overline{CLK}$ Cycle Time	80	50		ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	80	50		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	75	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{CLK}$	70	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{CLK}$	90	55		ns
t_{RCH}[3]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	25	ns
t_{RIS}[4]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$-$\overline{R_7}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		100	120	ns
t_{ETA}	ETLG to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{ECS}$	15	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{ECS}$	15	10		ns
t_{REN}	$\overline{R_0}$-$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	25	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	90	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

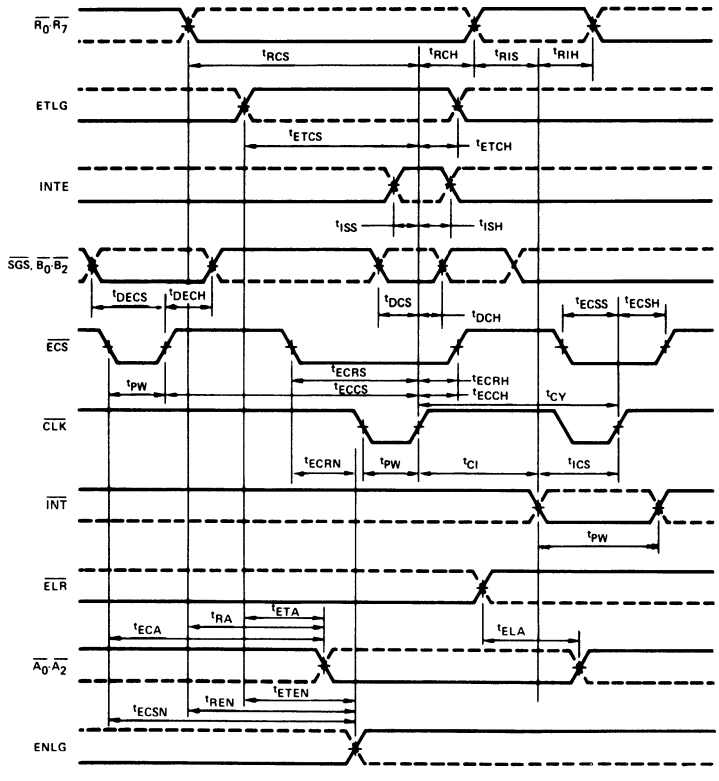
CAPACITANCE[5]

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max	
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		7	12	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5V$, $T_A = 25°C$, f = 1 MHz

NOTE 5. This parameter is periodically sampled and not 100% tested.

WAVEFORMS



NOTES:

(1) Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.

(2) Required for proper operation if ISE is enabled during next clock pulse.

(3) These times are not required for proper operation but for desired change in interrupt flip-flop.

(4) Required for new request or status to be properly loaded.

TEST CONDITIONS:

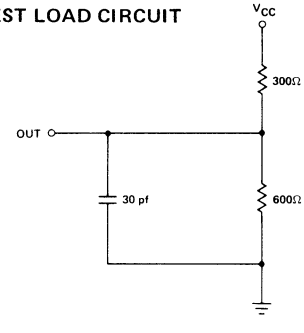
Input pulse amplitude: 2.5 volts.

Input rise and fall times: 5 ns between 1 and 2 volts.

Output loading of 15 mA and 30 pf.

Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT



MILITARY TEMP.

M8214
PRIORITY INTERRUPT CONTROL UNIT

- **Eight Priority Levels**
- **Fully Expandable**
- **Current Status Register**
- **Priority Comparator**
- **24-Pin Dual In-Line Package**
- **Full Military Temperature Range -55°C To +125°C**
- **±10% Power Supply Tolerance**

The M8214 is an eight level priority interrupt control unit designed to simplify interrupt driven microcomputer systems.

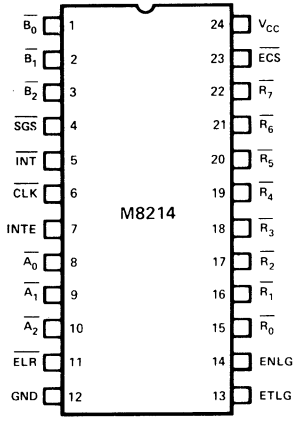
The PICU can accept eight requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector information to identify the service routine.

The M8214 is fully expandable by the use of open collector interrupt output and vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt driven microcomputer systems.

MCS 80/85

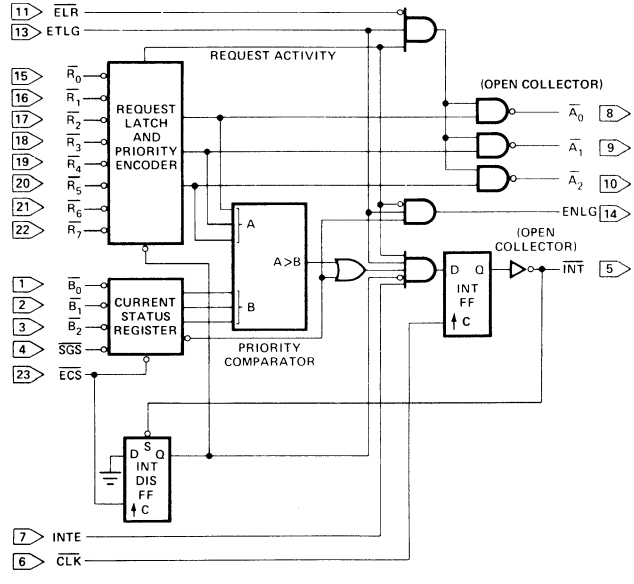
PIN CONFIGURATION



PIN NAMES

INPUTS	
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS
$\overline{SGS}$	STATUS GROUP SELECT
$\overline{ECS}$	ENABLE CURRENT STATUS
INTE	INTERRUPT ENABLE
$\overline{CLK}$	CLOCK (INT F-F)
$\overline{ELR}$	ENABLE LEVEL READ
ETLG	ENABLE THIS LEVEL GROUP
OUTPUTS:	
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS (OPEN COLLECTOR)
$\overline{INT}$	INTERRUPT (ACT. LOW) (OPEN COLLECTOR)
ENLG	ENABLE NEXT LEVEL GROUP

LOGIC DIAGRAM



D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +160°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Output Currents . . . . . 100 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T_A = 55°C to 125°C V_{CC} = 5V ±10%

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage (all inputs)			-1.2	V	I_C=-5mA
I_F	Input Forward Current: ETLG input all other inputs		-.15 -.08	-0.5 -0.25	mA mA	V_F=0.45V
I_R	Input Reverse Current: ETLG input all other inputs			80 40	μA μA	V_R=5.5V
V_{IL}	Input LOW Voltage: all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage: all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current		90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage: all outputs		.3	.45	V	I_{OL}=10mA
V_{OH}	Output HIGH Voltage: ENLG output	2.4	3.0		V	I_{OH}=-1mA
I_{OS}	Short Circuit Output Current: ENLG output	-15	-35	-55	mA	V_{CC}=5.0V
I_{CEX}	Output Leakage Current: $\overline{INT}$, $\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$			100	μA	VCEX=5.5V

NOTES:
1. Typical values are for T_A = 25° C, V_{CC} = 5.0V.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
t_{CY}	$\overline{CLK}$ Cycle Time	85			ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	25		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{CLK}$	90	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{CLK}$	100	55		ns
t_{RCH}[3]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	30	ns
t_{RIS}[4]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$-$\overline{R_7}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		100	130	ns
t_{ETA}	ETLG to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{ECS}$	20	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{ECS}$	20	10		ns
t_{REN}	$\overline{R_0}$-$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	30	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	110	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

WAVEFORMS (See 8214 Waveforms, page 10-131)

CAPACITANCE

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max	
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		7	12	pF

TEST CONDITIONS: V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C, f = 1 MHz

8216/8226
4-BIT PARALLEL BI-DIRECTIONAL BUS DRIVER

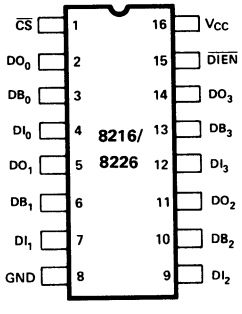
- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current — .25 mA Maximum**
- **High Output Drive Capability for Driving System Data Bus**
- **3.65V Output High Voltage for Direct Interface to 8080 CPU**
- **Three State Outputs**
- **Reduces System Package Count**

The 8216/8226 is a 4-bit bi-directional bus driver/receiver.

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50mA I_{OL} capability.

A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

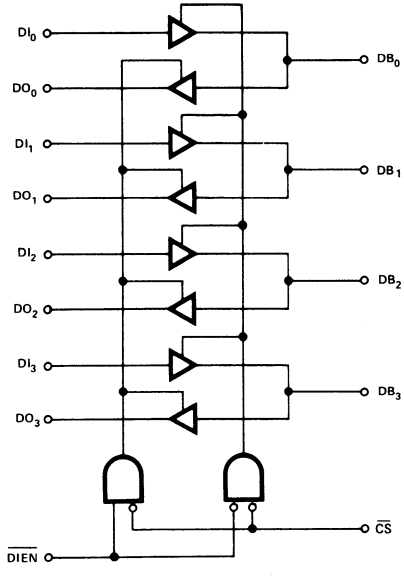
PIN CONFIGURATION



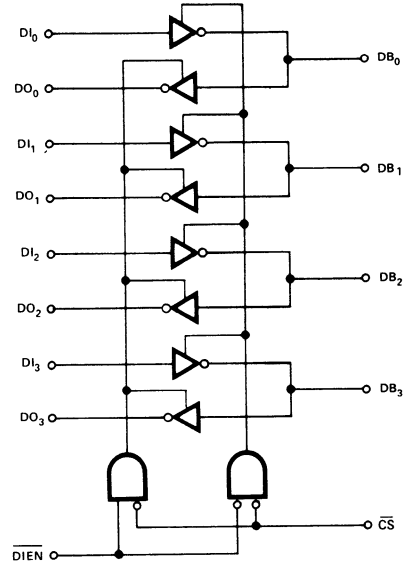
PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM 8216



LOGIC DIAGRAM 8226



FUNCTIONAL DESCRIPTION

Microprocessors like the 8080 are MOS devices and are generally capable of driving a single TTL load. The same is true for MOS memory devices. While this type of drive is sufficient in small systems with few components, quite often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The 8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

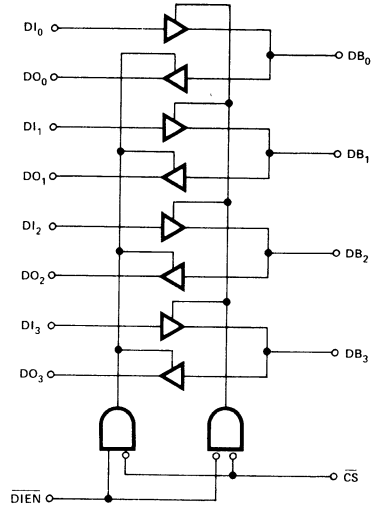
Each buffered line of the four bit driver consists of two separate buffers that are tri-state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is direct TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080 Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080 and 8008 CPUs is achieved with an adequate amount of noise immunity (350mV worst case).

Control Gating $\overline{\text{DIEN}}$, $\overline{\text{CS}}$

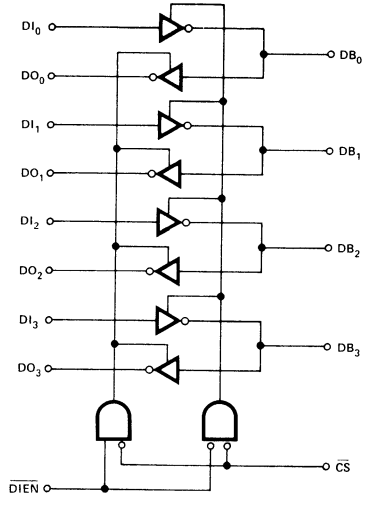
The $\overline{\text{CS}}$ input is actually a device select. When it is "high" the output drivers are all forced to their high-impedance state. When it is at "zero" the device is selected (enabled) and the direction of the data flow is determined by the $\overline{\text{DIEN}}$ input.

The $\overline{\text{DIEN}}$ input controls the direction of data flow (see Figure 1) for complete truth table. This direction control is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

The 8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.



(a) 8216



(b) 8226

$\overline{\text{DIEN}}$	$\overline{\text{CS}}$	
0	0	DI → DB
1	0	DB → DO
0	1	HIGH IMPEDANCE
1	1	

Figure 1. 8216/8226 Logic Diagrams

APPLICATIONS OF 8216/8226

8080 Data Bus Buffer

The 8080 CPU Data Bus is capable of driving a single TTL load and is more than adequate for small, single board systems. When expanding such a system to more than one board to increase I/O or Memory size, it is necessary to provide a buffer. The 8216/8226 is a device that is exactly fitted to this application.

Shown in Figure 2 are a pair of 8216/8226 connected directly to the 8080 Data Bus and associated control signals. The buffer is bi-directional in nature and serves to isolate the CPU data bus.

On the system side, the DB lines interface with standard semiconductor I/O and Memory components and are completely TTL compatible. The DB lines also provide a high drive capability (50mA) so that an extremely large system can be dirven along with possible bus termination networks.

On the 8080 side the DI and DO lines are tied together and are directly connected to the 8080 Data Bus for bi-directional operation. The DO outputs of the 8216/8226 have a high voltage output capability of 3.65 volts which allows direct connection to the 8080 whose minimum input voltage is 3.3 volts. It also gives a very adequate noise margin of 350mV (worst case).

The $\overline{DIEN}$ inputs to 8216/8226 is connected directly to the 8080. $\overline{DIEN}$ is tied to DBIN so that proper bus flow is maintained, and $\overline{CS}$ is tied to $\overline{BUSEN}$ so that the system side Data Bus will be 3-stated when a Hold request has been acknowledged during a DMA activity.

Memory and I/O Interface to a Bi-directional Bus

In large microcomputer systems it is often necessary to provide Memory and I/O with their own buffers and at the same time maintain a direct, common interface to a bi-directional Data Bus. The 8216/8226 has separated data in and data out lines on one side and a common bi-directional set on the other to accomodate such a function.

Shown in Figure 3 is an example of how the 8216/8226 is used in this type of application.

The interface to Memory is simple and direct. The memories used are typically Intel® 8102, 8102A, 8101 or 8107B-4 and have separate data inputs and outputs. The DI and DO lines of the 8216/8226 tie to them directly and under control of the $\overline{MEMR}$ signal, which is connected to the $\overline{DIEN}$ input, an interface to the bi-directional Data Bus is maintained.

The interface to I/O is similar to Memory. The I/O devices used are typically Intel® 8255s, and can be used for both input and output ports. The $\overline{I/O\ R}$ signal is connected directly to the $\overline{DIEN}$ input so that proper data flow from the I/O device to the Data Bus is maintained.

The 8216/8226 can be used in a wide variety of other buffering functions in microcomputer systems such as Address Bus Drivers, Drivers to peripheral devices such as printers, and as Drivers for long length cables to other peripherals or systems.

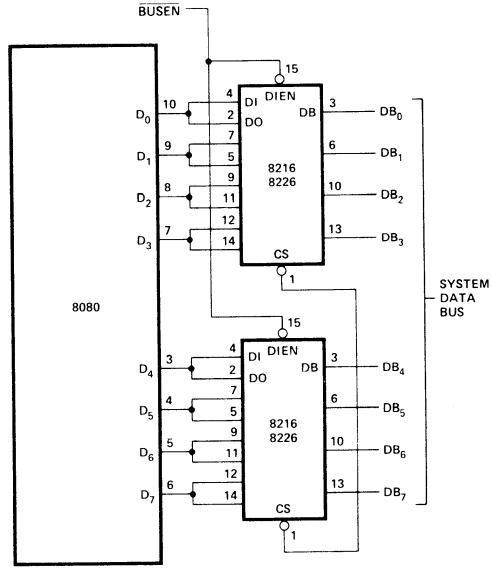


Figure 2. 8080 Data Bus Buffer.

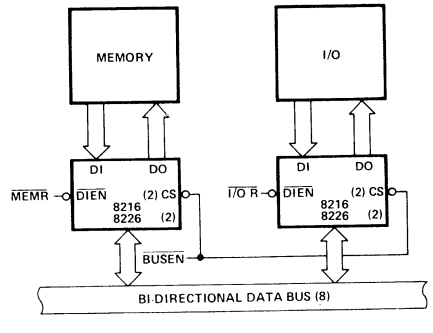


Figure 3. Memory and I/O Interface to a Bi-Directional Bus.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 125 mA

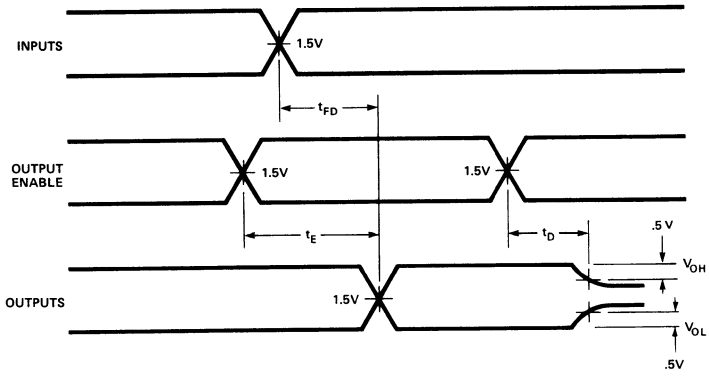
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

T_A = 0°C to +70°C, V_{CC}=+5V ±5%

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit	Conditions
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$			-0.15	-.5	mA	V_F = 0.45
I_{F2}	Input Load Current All Other Inputs			-0.08	-.25	mA	V_F = 0.45
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$				20	μA	V_R = 5.25V
I_{R2}	Input Leakage Current DI Inputs				10	μA	V_R = 5.25V
V_C	Input Forward Voltage Clamp				-1	V	I_C = -5mA
V_{IL}	Input "Low" Voltage				.95	V	
V_{IH}	Input "High" Voltage		2.0			V	
$\|I_O\|$	Output Leakage Current (3-State)	DO DB			20 100	μA	V_O = 0.45V/5.25V
I_{CC}	Power Supply Current	8216		95	130	mA	
		8226		85	120	mA	
V_{OL1}	Output "Low" Voltage			0.3	.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output "Low" Voltage	8216		0.5	.6	V	DB Outputs I_{OL}=55mA
		8226		0.5	.6	V	DB Outputs I_{OL}=50mA
V_{OH1}	Output "High" Voltage		3.65	4.0		V	DO Outputs I_{OH} = -1mA
V_{OH2}	Output "High" Voltage		2.4	3.0		V	DB Outputs I_{OH} = -10mA
I_{OS}	Output Short Circuit Current		-15 -30	-35 -75	-65 -120	mA mA	DO Outputs $V_O \cong 0V$, DB Outputs V_{CC}=5.0V

NOTE: Typical values are for T_A = 25°C, V_{CC} = 5.0V.

WAVEFORMS



A.C. CHARACTERISTICS

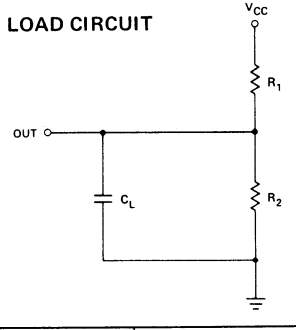
T_A = 0°C to +70°C, V_{CC} = +5V ±5%

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Conditions
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	C_L=30pF, R_1=300Ω R_2=600Ω
T_{PD2}	Input to Output Delay DB Outputs 8216		20	30	ns	C_L=300pF, R_1=90Ω
	8226		16	25	ns	R_2 = 180Ω
T_E	Output Enable Time 8216		45	65	ns	(Note 2)
	8226		35	54	ns	(Note 3)
T_D	Output Disable Time		20	35	ns	(Note 4)

TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT



CAPACITANCE[5]

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		4	8	pF
C_{OUT1}	Output Capacitance		6	10	pF
C_{OUT2}	Output Capacitance		13	18	pF

TEST CONDITIONS: V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz.

NOTES:
1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. DO Outputs, C_L = 30pF, R_1 = 300/10 KΩ, R_2 = 180/1KΩ; DB Outputs, C_L = 300pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
3. DO Outputs, C_L = 30pF, R_1 = 300/10 KΩ, R_2 = 600/1K; DB Outputs, C_L = 300pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
4. DO Outputs, C_L = 5pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ; DB Outputs, C_L = 5pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
5. This parameter is periodically sampled and not 100% tested.

MILITARY TEMP.

M8216
4-BIT PARALLEL BI-DIRECTIONAL BUS DRIVER

- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current: .25 mA Maximum**
- **High Output Drive Capability for Driving System Data Bus**
- **16-Pin Dual In-Line Package**
- **3.40V Output High Voltage for Direct Interface to 8080 CPU**
- **Three-State Outputs**
- **Full Military Temperature Range -55°C To +125°C**
- **±10% Power Supply Tolerance**

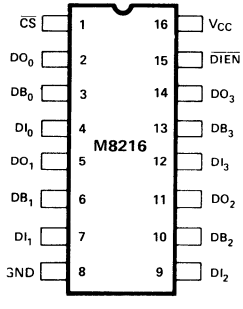
The M8216 is a 4-bit bi-directional bus driver/receiver.

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.40V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50mA I_{OL} capability.

The M8216 is used to meet a wide variety of applications for buffering in microcomputer systems.

MCS 80/85

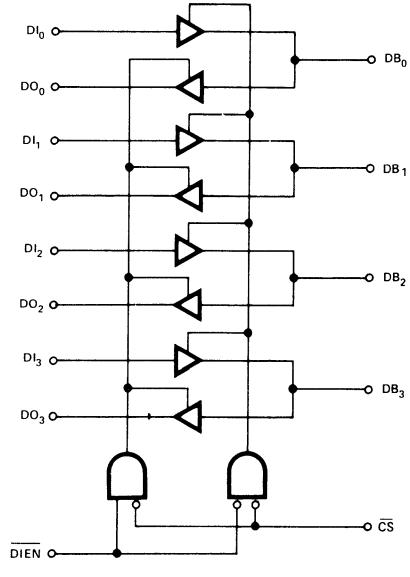
PIN CONFIGURATION



PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM
8216



D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Output Currents . . . . . 125 mA

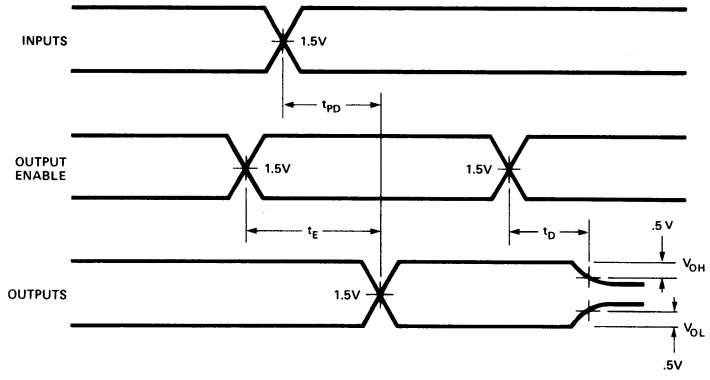
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Conditions
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		-0.15	-.5	mA	V_F = 0.45
I_{F2}	Input Load Current All Other Inputs		-0.08	-.25	mA	V_F = 0.45
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$			20	μA	V_R = 5.5V
I_{R2}	Input Leakage Current DI Inputs			10	μA	V_R = 5.5V
V_C	Input Forward Voltage Clamp			-1.2	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.95	V	V_{CC} = 5V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5V
$\|I_O\|$	Output Leakage Current DO (3-State) DB			20 100	μA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current		95	130	mA	
V_{OL1}	Output "Low" Voltage		0.3	.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output "Low" Voltage		0.5	.6	V	DB Outputs I_{OL}=50mA
V_{OH1}	Output "High" Voltage	3.4	3.8		V	DO Outputs I_{OH} = -.5mA
V_{OH2}	Output "High" Voltage	2.4	3.0		V	DO Outputs I_{OH} = -2mA DB Outputs I_{OH} = -5.0mA
I_{OS}	Output Short Circuit Current	-15 -30	-35 -75	-65 -120	mA mA	DO Outputs V_{CC} = 5.0V DB Outputs V_{CC} = 5.0V

NOTE: Typical values are for T_A = 25°C, V_{CC} = 5.0V.

WAVEFORMS



A.C. CHARACTERISTICS

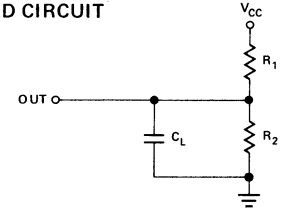
T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Conditions
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	(NOTE 2)
T_{PD2}	Input to Output Delay DB Outputs		20	33	ns	(NOTE 2)
T_E	Output Enable Time		45	75	ns	(NOTE 2)
T_D	Output Disable Time		20	40	ns	(NOTE 2)

TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.

TEST LOAD CIRCUIT



CAPACITANCE

Symbol	Parameter		Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance			4	6	pF
C_{OUT1}	Output Capacitance	DO Outputs		6	10	pF
C_{OUT2}	Output Capacitance	DB Outputs		13	18	pF

TEST CONDITIONS: V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz.

NOTES: 1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.

2.

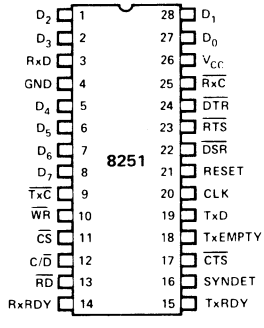
TEST	C_L	R_1	R_2
T_{PD1}	30pF	300Ω	600Ω
T_{PD2}	300pF	90Ω	180Ω
T_E, (DO, ENABLE↑)	30pF	10KΩ	1KΩ
T_E, (DO, ENABLE↓)	30pF	300Ω	600Ω
T_E, (DB, ENABLE↑)	300pF	10KΩ	1KΩ
T_E, (DB, ENABLE↓)	300pF	90Ω	180Ω
T_D, (DO, DISABLE↑)	5pF	300Ω	600Ω
T_D, (DO, DISABLE↓)	5pF	10KΩ	1KΩ
T_D, (DB, DISABLE↑)	5pF	90Ω	180Ω
T_D, (DB, DISABLE↓)	5pF	10KΩ	1KΩ

8251
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    5-8 Bit Characters
    Internal or External Character Synchronization
    Automatic Sync Insertion
  - **Asynchronous:**
    5-8 Bit Characters
    Clock Rate — 1,16 or 64 Times Baud Rate
    Break Character Generation
    1, 1½, or 2 Stop Bits
    False Start Bit Detection
- **Baud Rate —DC to 56k Baud (Sync Mode)**
  DC to 9.6k Baud (Async Mode)
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs Are TTL Compatible**
- **Single 5 Volt Supply**
- **Single TTL Clock**

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.

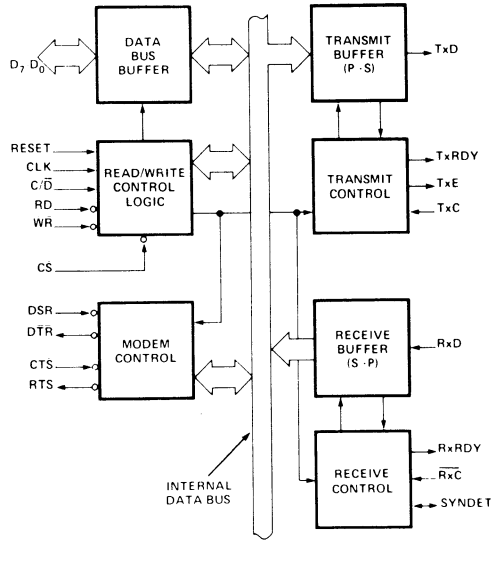
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET	Sync Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



MCS 80/85

8251 BASIC FUNCTIONAL DESCRIPTION

General

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 8080 Microcomputer System. Like other I/O devices in the 8080 Microcomputer System its functional configuration is programmed by the systems software for maximum flexibility. The 8251 can support virtually any serial data technique currently in use (including IBM "bi-sync").

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8251 to the 8080 system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the 8080 CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer.

Read/Write Control Logic

This functional block accepts inputs from the 8080 Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for device functional definition.

RESET (Reset)

A "high" on this input forces the 8251 into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251 to program its functional definition. Minimum RESET pulse width is 6 t_{CY}.

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter clock inputs for synchronous mode (4.5 times for asynchronous mode).

$\overline{WR}$ (Write)

A "low" on this input informs the 8251 that the CPU is outputting data or control words, in essence, the CPU is writing out to the 8251.

$\overline{RD}$ (Read)

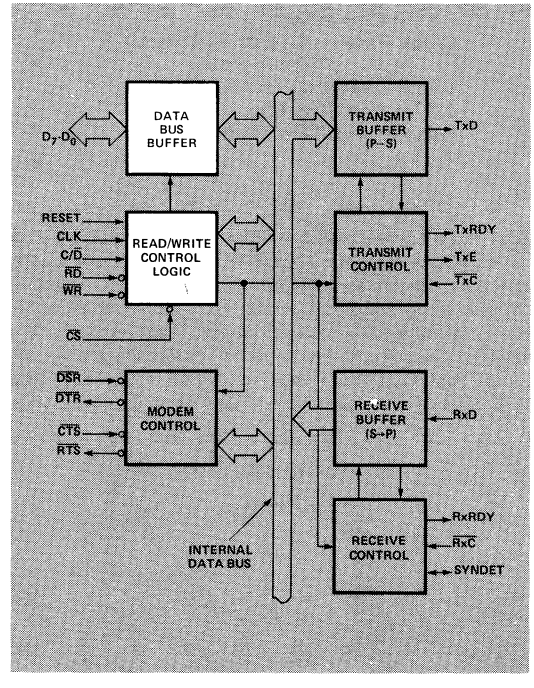
A "low" on this input informs the 8251 that the CPU is inputting data or status information, in essence, the CPU is reading from the 8251.

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs informs the 8251 that the word on the Data Bus is either a data character, control word or status information.
1 = CONTROL 0 = DATA

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8251. No reading or writing will occur unless the device is selected.



C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251 ⇒ DATA BUS
0	1	0	0	DATA BUS ⇒ 8251
1	0	1	0	STATUS ⇒ DATA BUS
1	1	0	0	DATA BUS ⇒ CONTROL
X	1	1	0	DATA BUS ⇒ 3-STATE
X	X	X	1	DATA BUS ⇒ 3-STATE

Modem Control

The 8251 has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The modem control signals are general purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is general purpose in nature. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is general purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is general purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251 to transmit data (serial) if the Tx EN bit in the Command byte is set to a "one."

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

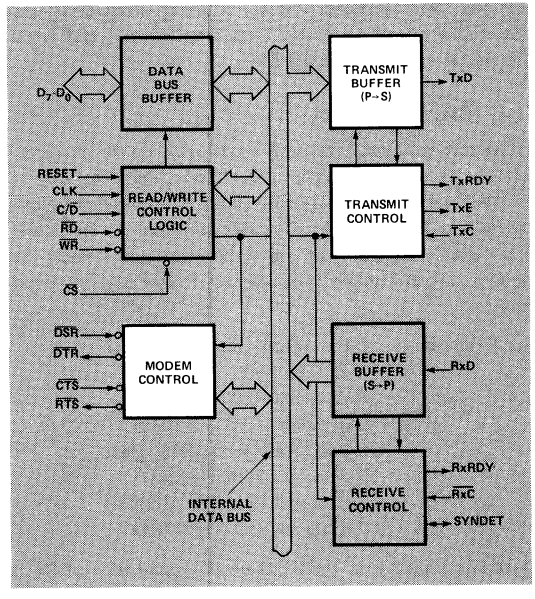
TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. It can be used as an interrupt to the system or for the Polled operation the CPU can check TxRDY using a status read operation. TxRDY is automatically reset when a character is loaded from the CPU.

TxE (Transmitter Empty)

When the 8251 has no characters to transmit, the TxE output will go "high". It resets automatically upon receiving a character from the CPU. TxE can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode. TxE is independent of the TxEN bit in the Command instruction.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be transmitted automatically as "fillers". TxE goes low as soon as the SYNC is being shifted out.



$\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the frequency of $\overline{TxC}$ is equal to the actual Baud Rate (1X). In Asynchronous transmission mode, the frequency of $\overline{TxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x or 64x the Baud Rate.

For Example:

If Baud Rate equals 110 Baud,
$\overline{TxC}$ equals 110 Hz (1x)
$\overline{TxC}$ equals 1.76 kHz (16x)
$\overline{TxC}$ equals 7.04 kHz (64x).

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to the RxD pin.

Receiver Control

This functional block manages all receiver-related activities.

RxRDY (Receiver Ready)

This output indicates that the 8251 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or for Polled operation the CPU can check the condition of RxRDY using a status read operation. RxRDY is automatically reset when the character is read by the CPU.

$\overline{\text{RxC}}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the frequency of $\overline{\text{RxC}}$ is equal to the actual Baud Rate (1x). In Asynchronous Mode, the frequency of $\overline{\text{RxC}}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x or 64x the Baud Rate.

For Example: If Baud Rate equals 300 Baud,
$\overline{\text{RxC}}$ equals 300 Hz (1x)
$\overline{\text{RxC}}$ equals 4800 Hz (16x)
$\overline{\text{RxC}}$ equals 19.2 kHz (64x).
If Baud Rate equals 2400 Baud,
$\overline{\text{RxC}}$ equals 2400 Hz (1x)
$\overline{\text{RxC}}$ equals 38.4 kHz (16x)
$\overline{\text{RxC}}$ equals 153.6 kHz (64x).

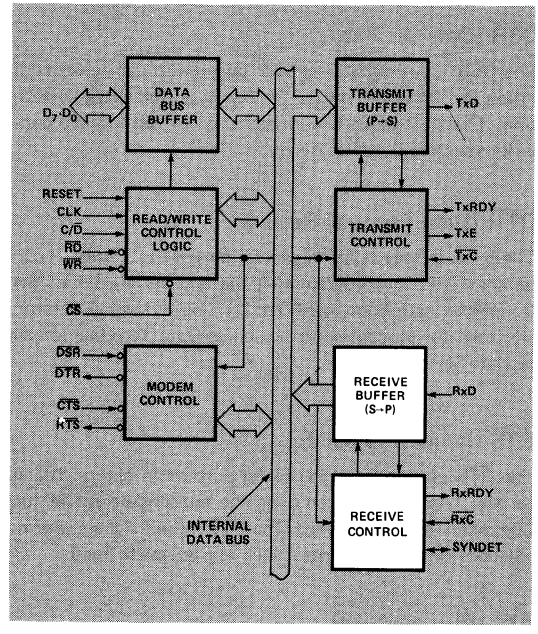
Data is sampled into the 8251 on the rising edge of $\overline{\text{RxC}}$.

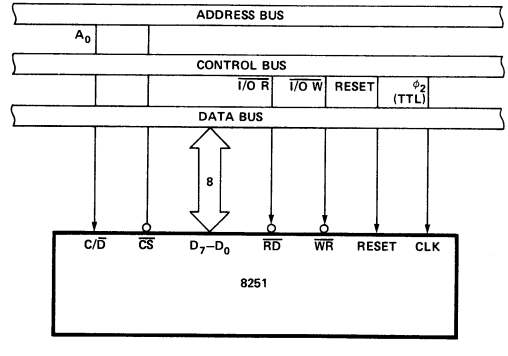
NOTE: In most communications systems, the 8251 will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{\text{TxC}}$ and $\overline{\text{RxC}}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)

This pin is used in SYNChronous Mode only. It is used as either input or output, programmable through the Control Word. It is reset to "low" upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251 has located the SYNC character in the Receive mode. If the 8251 is programmed to use double Sync characters (bi-sync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input, (external SYNC detect mode), a positive going signal will cause the 8251 to start assembling data characters on the falling edge of the next $\overline{\text{RxC}}$. Once in SYNC, the "high" input signal can be removed. The duration of the high signal should be at least equal to the period of $\overline{\text{RxC}}$.





8251 Interface to 8080 Standard System Bus

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize the 8251 to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD PARITY etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251 is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251 is ready to receive a character. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251. On the other hand, the 8251 receives serial data from the MODEM or I/O device, upon receiving an entire character the RxRDY output is raised "high" to signal the CPU that the 8251 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU read operation.

The 8251 cannot begin transmission until the TxEN (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send (CTS) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251

Prior to starting data transmission or reception, the 8251 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251 and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

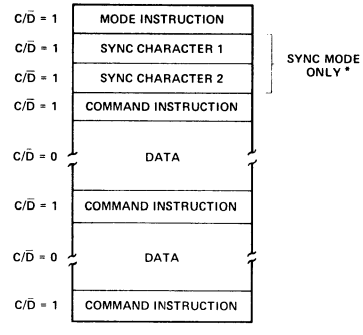
This format defines the general operational characteristics of the 8251. It **must** follow a Reset operation (internal or external). Once the Mode instruction has been written into the 8251 by the CPU, SYNC characters or Command instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251.

Both the Mode and Command instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251 for data communication.

All control words written into the 8251 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251 at any time in the data block during the operation of the 8251. To return to the Mode Instruction format a bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.



*The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

Typical Data Block

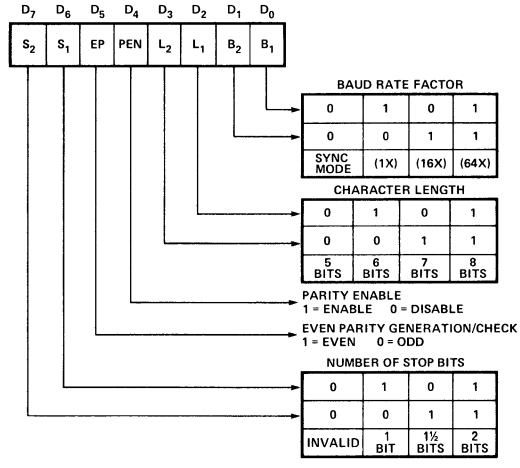
Mode Instruction Definition

The 8251 can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251 the designer can best view the device as two separate components sharing the same package. One Asynchronous the other Synchronous. The format definition can be changed "on the fly" but for explanation purposes the two formats will be isolated.

Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251 automatically adds a Start bit (low level) and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

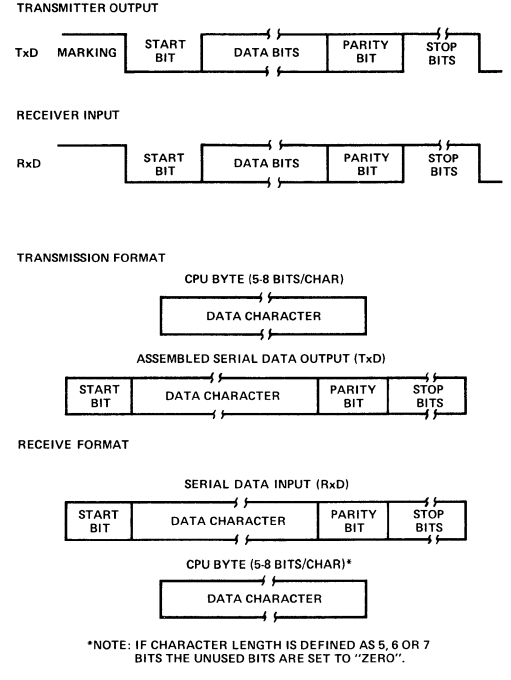
When no data characters have loaded into the 8251 the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.



Mode Instruction Format, Asynchronous Mode

Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center. If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. This character is then loaded into the parallel I/O buffer of the 8251. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN flag is raised (thus the previous character is lost). All of the error flags can be reset by a command instruction. The occurrence of any of these errors will not stop the operation of the 8251.

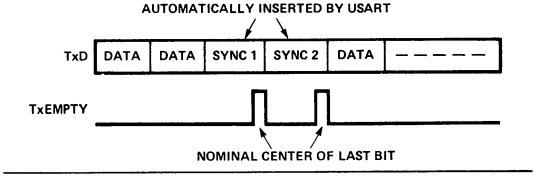


Asynchronous Mode

Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251 which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251 with a character before the 8251 becomes empty, the SYNC characters (or character if in single SYNC word mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251 is empty and SYNC characters are being sent out. TxEMPTY goes low when SYNC is being shifted out (See Figure below). The TxEMPTY pin is internally reset by the next character being written into the 8251.



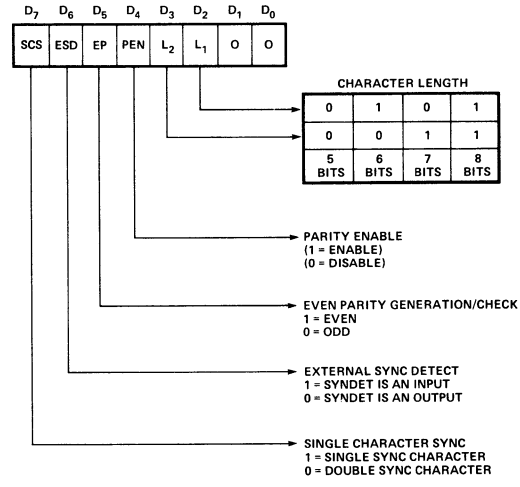
Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the internal SYNC mode has been programmed, the receiver starts in a HUNT mode. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is continuously compared with the first SYNC character until a match occurs. If the 8251 has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ.

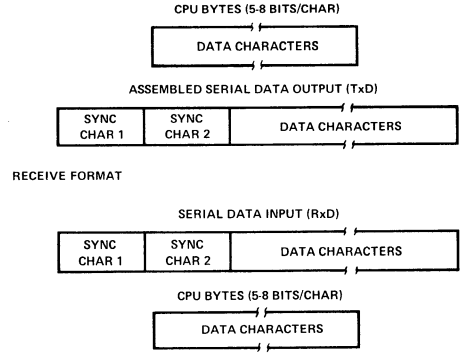
In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin. The high level can be removed after one $\overline{RxC}$ cycle.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost.



Mode Instruction Format, Synchronous Mode

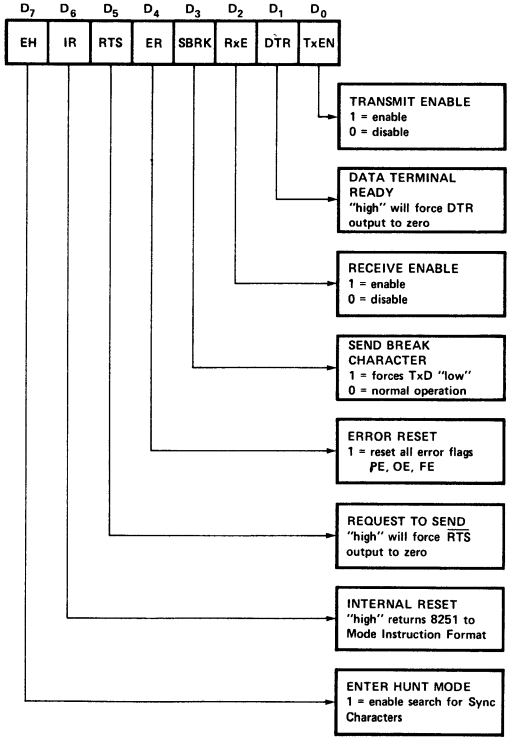


Synchronous Mode, Transmission Format

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251 has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251 and Sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D}$ = 1) will load the Command Instruction. A Reset operation (internal or external) will return the 8251 to the Mode Instruction Format.



Command Instruction Format

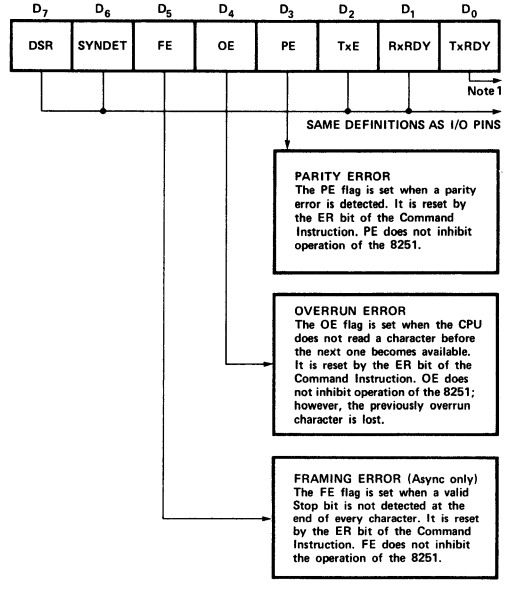
STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251 has facilities that allow the programmer to "read" the status of the device at any time during the functional operation.

A normal "read" command is issued by the CPU with the C/D input at one to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251 can be used in a completely Polled environment or in an interrupt driven environment.

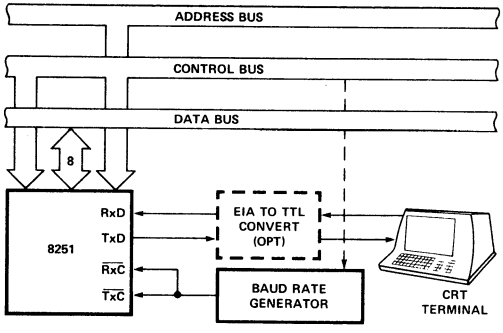
Status update can have a maximum delay of 16 clock periods.



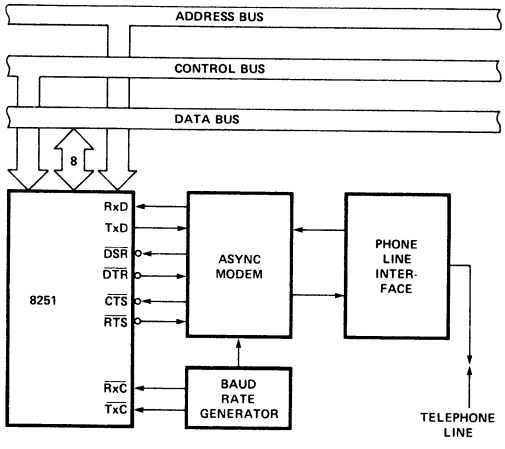
Status Read Format

Note 1: TxRDY status bit has similar meaning as the TxRDY output pin. The former is not conditioned by CTS and TxEN; the latter is conditioned by both CTS and TxEN.
i.e. TxRDY status bit = DB Buffer Empty
TxRDY pin out = DB Buffer Empty • CTS • TxEN

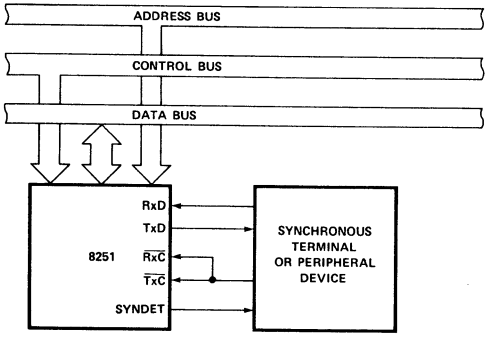
APPLICATIONS OF THE 8251



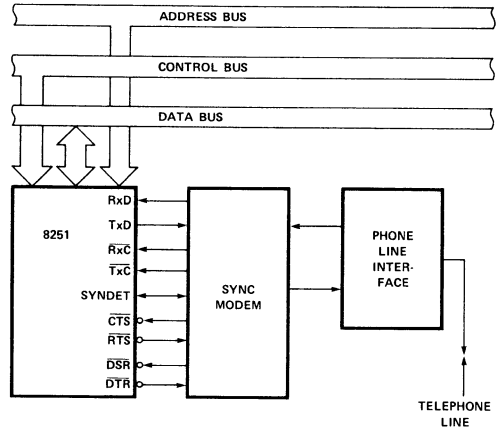
Asynchronous Serial Interface to CRT Terminal, DC-9600 Baud



Asynchronous Interface to Telephone Lines



Synchronous Interface to Terminal or Peripheral Device



Synchronous Interface to Telephone Lines

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100μA
I_{DL}	Data Bus Leakage			–50 10	μA μA	V_{OUT} = .45V V_{OUT} = V_{CC}
I_{IL}	Input Leakage			10	μA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

MCS 80/85

TEST LOAD CIRCUIT:

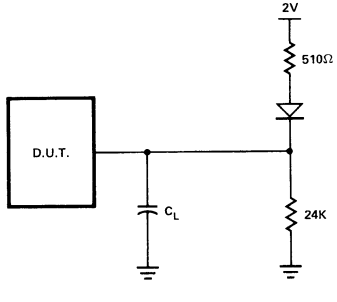
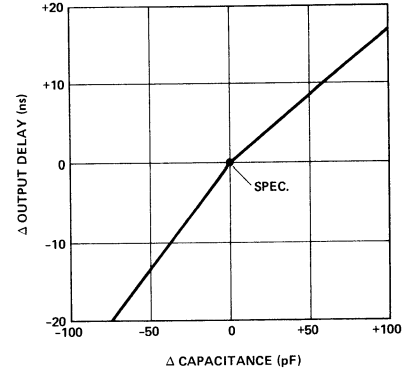


Figure 1.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE (dB)



A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

BUS PARAMETERS: (Note 1)

READ CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/D)	50		ns	
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/D)	5		ns	
t_{RR}	$\overline{READ}$ Pulse Width	430		ns	
t_{RD}	Data Delay from $\overline{READ}$		350	ns	C_L = 100 pF
t_{DF}	$\overline{READ}$ to Data Floating		200	ns	C_L = 100 pF
		25		ns	C_L = 15 pF
t_{RV}	Recovery Time Between WRITES (Note 2)	6		t_{CY}	

WRITE CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AW}	Address Stable Before $\overline{WRITE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	400		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	200		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		ns	

NOTES: 1. AC timings measured at V_{OH} = 2.0, V_{OL} = .8, and with load circuit of Figure 1.
2. This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

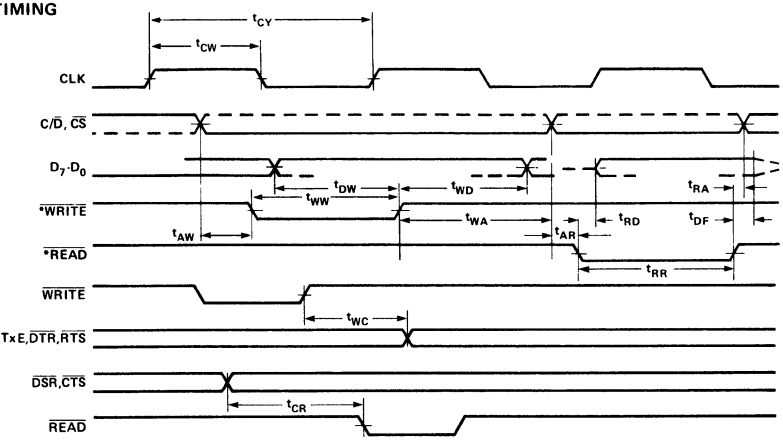
OTHER TIMINGS:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{CY}	Clock Period (Note 3)	.420	1.35	μs	
$t_{\phi W}$	Clock Pulse Width	220	.7 t_{CY}	ns	
t_R, t_F	Clock Rise and Fall Time	0	50	ns	
t_{DTx}	TxD Delay from Falling Edge of TxC		1	μs	C_L = 100 pF
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	C_L = 100 pF
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	C_L = 100 pF
f_{Tx}	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	56	KHz	
	16x and 64x Baud Rate	DC	520	KHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1x Baud Rate	DC	56	KHz	
	16x and 64x Baud Rate	DC	520	KHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
t_{Tx}	TxRDY Delay from Center of Data Bit		16	t_{CY}	C_L = 50 pF
t_{Rx}	RxRDY Delay from Center of Data Bit		20	t_{CY}	
t_{IS}	Internal SYNDET Delay from Center of Data Bit		25	t_{CY}	
t_{ES}	Internal SYNDET Set-Up Time Before Falling Edge of RxC		16	t_{CY}	
t_{TxE}	TxEMPTY Delay from Center of Data Bit		16	t_{CY}	C_L = 50 pF
t_{WC}	Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)		16	t_{CY}	
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		16	t_{CY}	

3. The TxC and RxC frequencies have the following limitations with respect to CLK.
   For 1x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
   For 16x and 64x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$

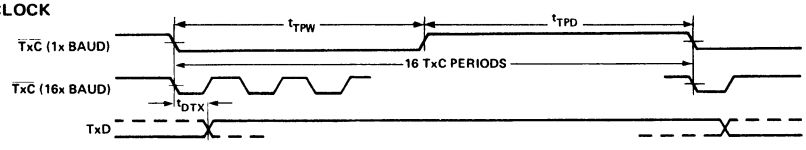
4. Reset Pulse Width = 6 t_{CY} minimum.

READ AND WRITE TIMING

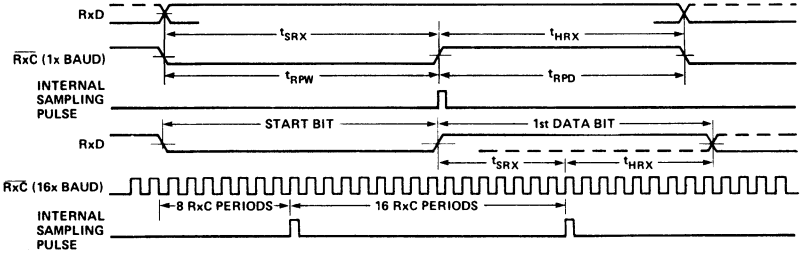


*WRITE AND READ PULSES HAVE NO TIMING LIMITATION WITH RESPECT TO CLK.

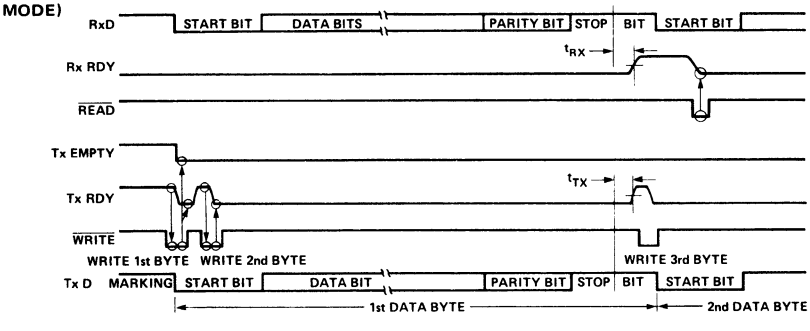
TRANSMITTER CLOCK AND DATA



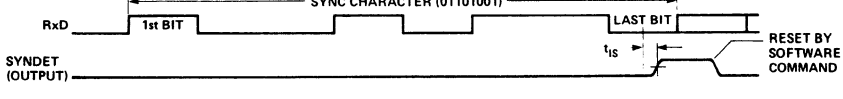
RECEIVER CLOCK AND DATA



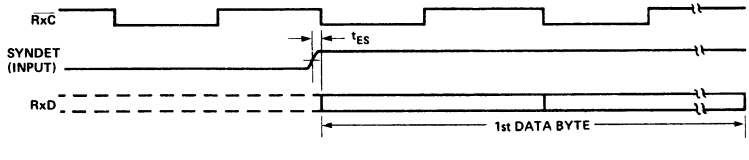
Tx RDY AND Rx RDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT

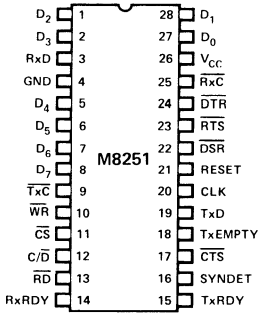


M8251
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    5-8 Bit Characters
    Internal or External Character Synchronization
    Automatic Sync Insertion
  - **Asynchronous:**
    5-8 Bit Characters
    Clock Rate — 1,16 or 64 Times Baud Rate
    Break Character Generation
    1, 1½, or 2 Stop Bits
    False Start Bit Detection
- **Baud Rate — DC to 56k Baud (Sync Mode)**
  DC to 8.1k Baud (Async Mode)
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **All Inputs and Outputs Are TTL Compatible**
- **Full Military Temperature Range -55°C to +125°C**
- **±10% Power Supply Tolerance**

The M8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.

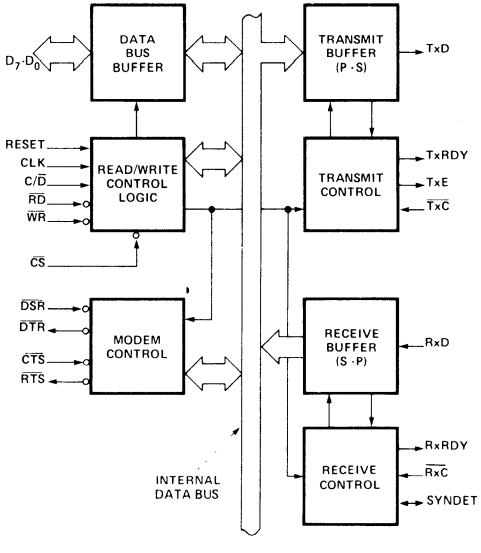
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
VCC	+5 Volt Supply
GND	Ground

M8251 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage On Any Pin
With Respect to GND . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100μA
I_{DL}	Data Bus Leakage			–50 10	μA μA	V_{OUT} = .45V V_{OUT} = V_{CC}
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.5V
I_{CC}	Power Supply Current		45	80		

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

MCS-80/85

TEST LOAD CIRCUIT:

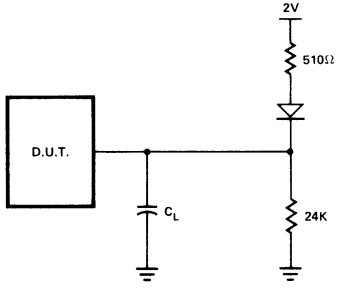
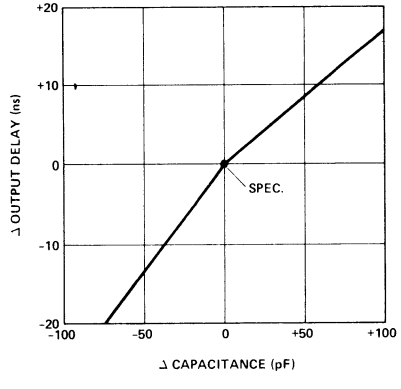


Figure 1.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE (dB)



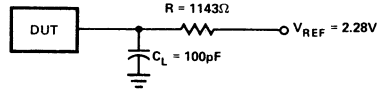
A.C. CHARACTERISTICS [2]

T_A = -55°C to +125°C; V_{CC} = 5.0V ±10% ; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{CY}	Clock Period	.420		1.35	μs	
$t_{\phi W}$	Clock Pulse Width	220			ns	
t_R,t_F	Clock Rise and Fall Time	0		50	ns	
t_{WR}	$\overline{WRITE}$ Pulse Width	400			ns	
t_{DS}	Data Set-Up Time for $\overline{WRITE}$	200			ns	
t_{DH}	Data Hold Time for $\overline{WRITE}$	40			ns	
t_{AW}	Address Stable before $\overline{WRITE}$	20			ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	20			ns	
t_{RD}	READ Pulse Width	430			ns	
t_{DD}	Data Delay from $\overline{READ}$			350	ns	
t_{DF}	$\overline{READ}$ to Data Floating [3]	25		200	ns	C_L=15pF to 100pF
t_{AR}	Address (CE, C/$\overline{D}$) Stable before $\overline{READ}$	50			ns	
t_{RA}	Address (CE, C/$\overline{D}$) Hold Time for $\overline{READ}$	5			ns	
t_{DTx}	TxD Delay from Falling Edge of TxC			1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2			μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2			μs	
f_{Tx} [1]	Transmitter Clock Frequency					
	1X Baud Rate	DC		56	KHz	
	16X and 64X Baud Rate	DC		529	KHz	
f_{Rx} [1]	Receiver Clock Frequency					
	1X Baud Rate	DC		56	KHz	
	16X and 64X Baud Rate	DC		529	KHz	
t_{Tx}	TxRDY Delay from Center of Data Bit			16	CLK Period	
t_{Rx}	RxRDY Delay from Center of Data Bit	15		20	CLK Period	
t_{IS}	Internal Syndet Delay from Center of Data Bit	20		25	CLK Period	
t_{ES}	External Syndet Set-Up Time before Falling Edge of RxC			16	CLK Period	

Note 1: The TxC and RxC frequencies have the following limitation with respect to CLK.
For ASYNC Mode, t_{Tx} or $t_{Rx} \geq 4.5\ t_{CY}$
For SYNC Mode, t_{Tx} or $t_{Rx} \geq 30\ t_{CY}$
2. AC timings are measured at V_{OH} = 2.0V, V_{OL} = 0.8V, and load circuit of Figure 1.
3. Float timings are measured at V_{OH} = 2.48V, V_{OL} = 2.08V

Figure 1. Test Load Circuit.



WAVEFORMS (See 8251 Waveforms, page 10-155)

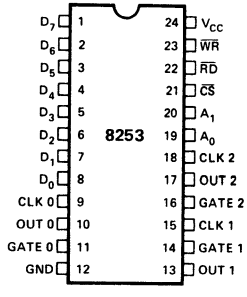
8253
PROGRAMMABLE INTERVAL TIMER

- 3 Independent 16-Bit Counters
- DC to 2 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5V Supply
- 24 Pin Dual-In-Line Package

The 8253 is a programmable counter/timer chip designed for use with microprocessors. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as three independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable by the 8080.

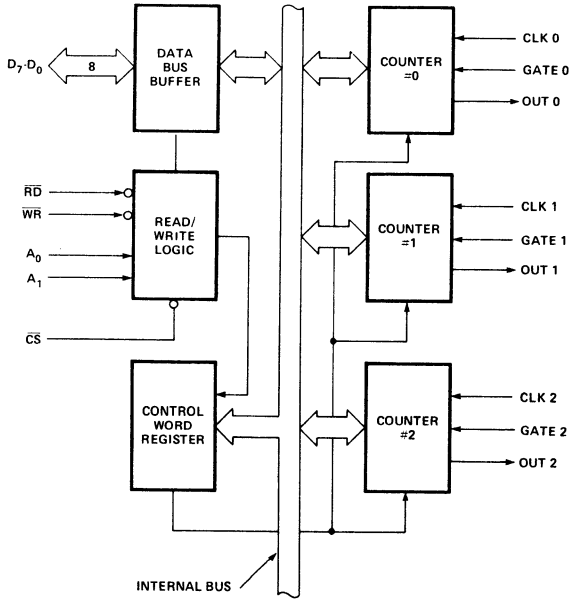
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (8-BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
$\overline{RD}$	READ COUNTER
$\overline{WR}$	WRITE COMMAND OR DATA
$\overline{CS}$	CHIP SELECT
A_0-A_1	COUNTER SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM



8253 BASIC FUNCTIONAL DESCRIPTION

General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel® 8080 Microcomputer system. Its function is that of a general purpose, multi-mode timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the MCS-80™ system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the MCS-80™ system bus and in turn generates control signals for overall device operation. It is enabled or disabled by $\overline{CS}$ so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

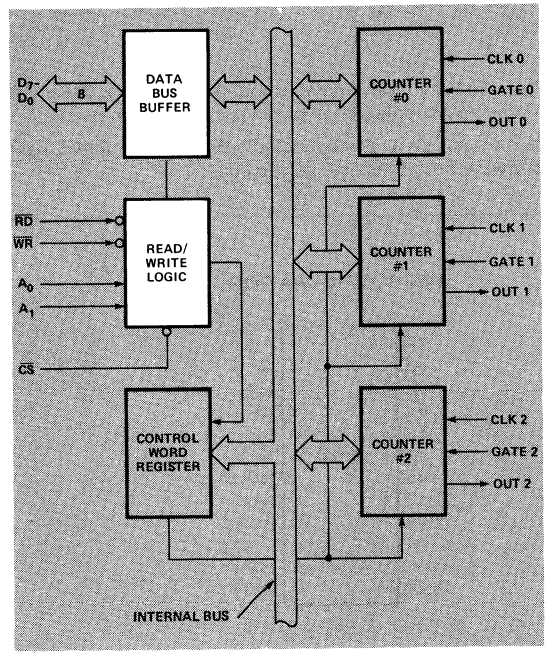
A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0, A1

These inputs are normally connected to the MCS-80™ address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.



8253 BLOCK DIAGRAM

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

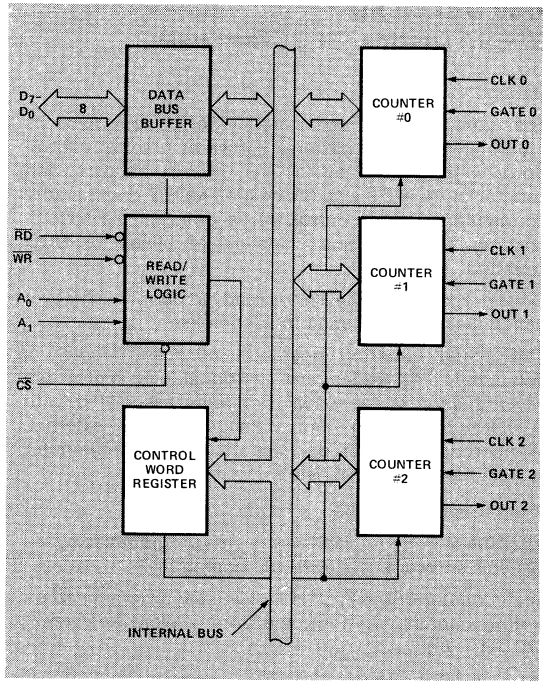
The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

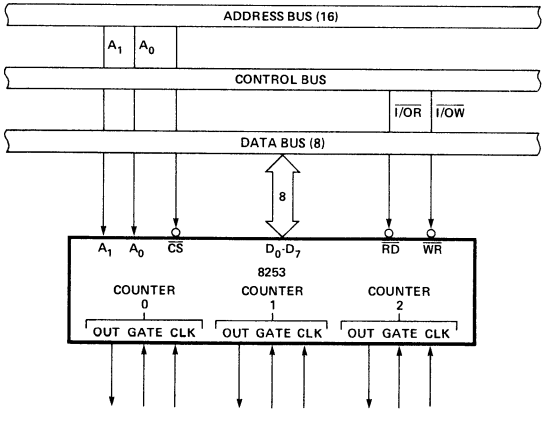


8253 BLOCK DIAGRAM

8253 SYSTEM INTERFACE

The 8253 is a component of the Intel® MCS-80™ System and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems. The $\overline{RD}$ and $\overline{WR}$ inputs are normally connected to the $\overline{IOR}$ and $\overline{IOW}$ outputs of the 8228 but they can be connected to the $\overline{MEMR}$ and $\overline{MEMW}$ signals in a memory mapped I/O configuration so that the full memory operating instructions of the 8080A can be used to initialize and maintain the 8253.



8253 SYSTEM INTERFACE

8253 DETAILED OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control Fields

SC-Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL-Read/Load

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M-MODE

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

MODE Definition

MODE 0: Interrupt on terminal count.
The OUTput will be initially low after the Mode set operation. After the count is loaded into the selected count register, the OUTput will remain low and the counter will count. When terminal count is reached the OUTput will go high and remain high until the selected count register is reloaded with the Mode.

Reloading a counter register during counting results in the following:

(1) Load 1st byte stops the current counting.

(2) Load 2nd byte starts the new count.

The GATE input will enable the counting when high and inhibit counting when low.

MODE 1: Programmable One-Shot.
The OUTput will go low on the count following the rising edge of the GATE input.

The OUTput will go high on the terminal count. If a new count value is loaded while the OUTput is low it will not affect the duration of the One-Shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator

Divide by N counter. The OUTput will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The GATE input, when low, will force the OUTput high. When the GATE input goes high, the counter will start from the initial count. Thus, the GATE input can be used to synchronize the counter.

When this MODE is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator.

Similar to MODE 2 except that the OUTput will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. If the count is odd, the OUTput will be high for (N+1)/2 counts and low for (N-1)/2 counts.

If the counter register is reloaded with a new value during counting, this new value will be reflected immediately after the output transition of the current count.

MODE 4: Software triggered strobe.

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

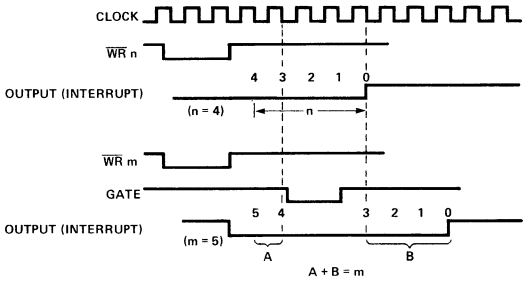
MODE 5: Hardware triggered strobe.

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

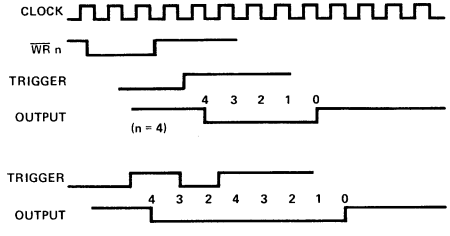
GATE Pin Operations Summary

Modes \ Signal Status	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

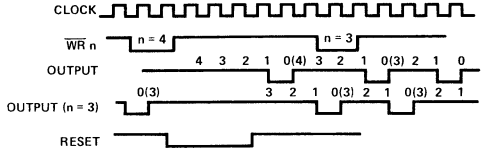
MODE 0



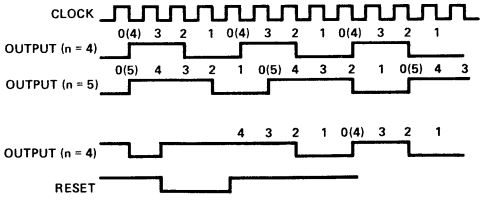
MODE 1



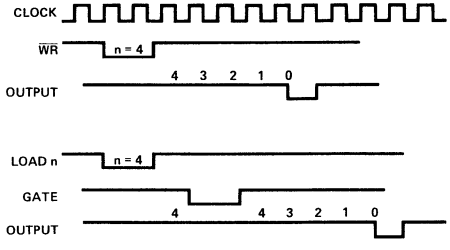
MODE 2



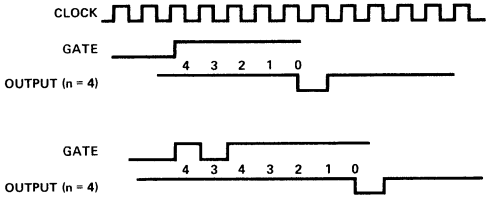
MODE 3



MODE 4



MODE 5



8253 TIMING DIAGRAMS

8253 READ/WRITE PROCEDURE

Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

Programming Format

	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Alternate Programming Formats

Example:

			A1	A0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

8253 READ/WRITE PROCEDURE

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1-11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB).

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

MODE Register for Latching Count

A0, A1 = 11

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1,SC0 — specify counter to be latched.

D5,D4 — 00 designates counter latching operation.

X — don't care.

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5 V to +7 V
Power Dissipation ..... 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-.5	.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+.5V	V	
V_{OL}	Output Low Voltage		.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA
I_{LI}	Input Load Current		10	μA	V_{IN} = V_{CC} to 0V
I_{LOL}	Output Leakage Current		-10	μA	V_{OUT} = 0.45V
I_{LOH}	Output Leakage Current		10	μA	V_{OUT} = V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

BUS PARAMETERS: (Note 1)

READ CYCLE

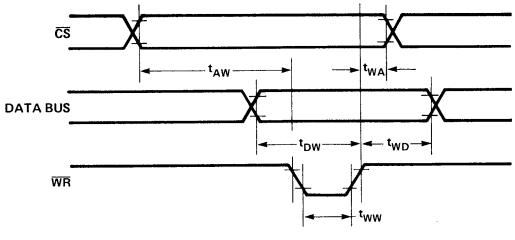
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	Address Stable Before $\overline{READ}$	50		ns	
t_{RA}	Address Hold Time for $\overline{READ}$	5		ns	
t_{RR}	$\overline{READ}$ Pulse Width	420		ns	
t_{RD}	Data Delay from $\overline{READ}$		300	ns	C_L = 100 pF
t_{DF}	$\overline{READ}$ to Data Floating		200	ns	C_L = 100 pF
		25		ns	C_L = 15 pF

WRITE CYCLE

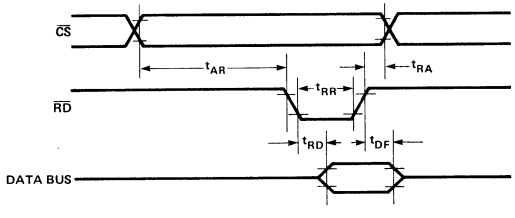
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AW}	Address Stable Before $\overline{WRITE}$	50		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	400		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		ns	
t_{RV}	Recovery Time Between $\overline{WRITES}$	1		μs	

Note 1: AC timings measured at V_{OH} = 2.0, V_{OL} = .8, and with load circuit of Figure 1.

WRITE TIMING



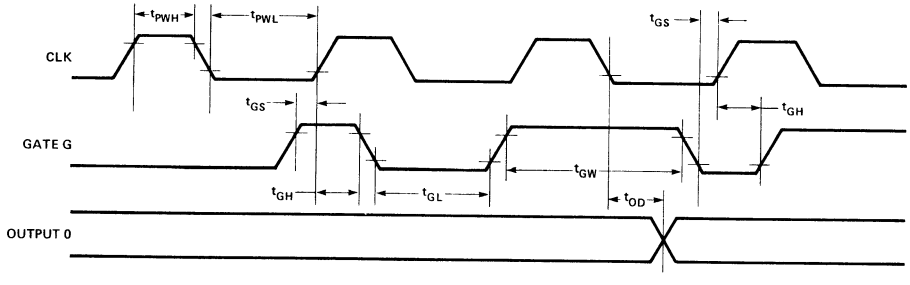
READ TIMING



A.C. CHARACTERISTICS (Cont'd): $T_A = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V

CLOCK AND GATE TIMING

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{CLK}	Clock Period	300	dc	ns	
t_{PWH}	High Pulse Width	200		ns	
t_{PWL}	Low Pulse Width	100		ns	
t_{GW}	Trigger Pulse Width	200		ns	
t_{GS}	Gate Set Up Time To CLK↑	150		ns	
t_{GH}	Gate Hold Time After CLK↑	100		ns	
t_{GL}	Low Gate Width	100		ns	
t_{OD}	Output Delay From CLK↓		300	ns	C_L = 50 pF



IMPROVED

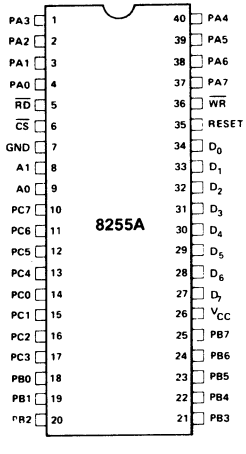
8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with Intel Microprocessor Families**
- **Improved Timing Characteristics**
- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40 Pin Dual-In-Line Package**
- **Reduces System Package Count**
- **Improved DC Driving Capability**

The 8255A is a general purpose programmable I/O device designed for use with microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bi-directional Bus mode which uses 8 lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255A include bit set and reset capability and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

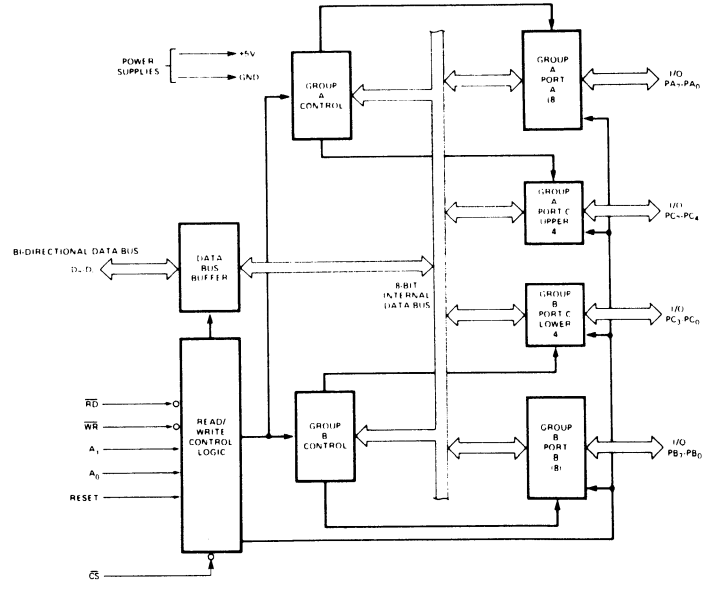
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

BLOCK DIAGRAM



MCS 80/85

8255 BASIC FUNCTIONAL DESCRIPTION

General

The 8255 is a Programmable Peripheral Interface (PPI) device designed for use in 8080 Microcomputer Systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the 8080 system bus. The functional configuration of the 8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bi-directional, eight bit buffer is used to interface the 8255 to the 8080 system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions by the 8080 CPU. Control Words and Status information are also transferred through the Data Bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the 8080 CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select: A "low" on this input pin enables the communication between the 8255 and the 8080 CPU.

($\overline{RD}$)

Read: A "low" on this input pin enables the 8255 to send the Data or Status information to the 8080 CPU on the Data Bus. In essence, it allows the 8080 CPU to "read from" the 8255.

($\overline{WR}$)

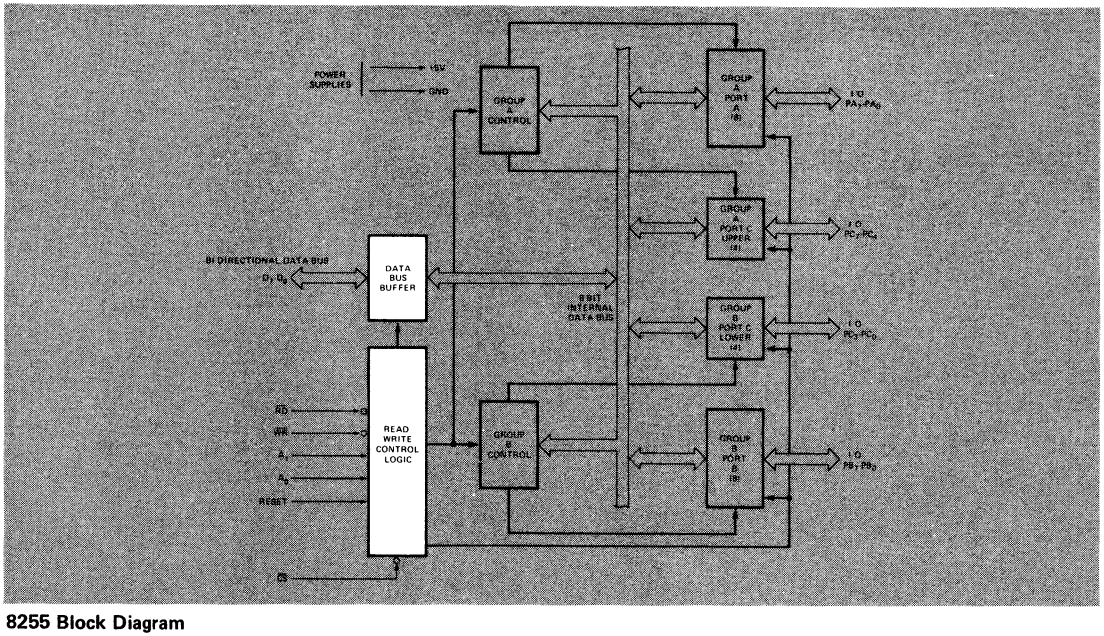
Write: A "low" on this input pin enables the 8080 CPU to write Data or Control words into the 8255.

(A_0 and A_1)

Port Select 0 and Port Select 1: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the Control Word Register. They are normally connected to the least significant bits of the Address Bus (A_0 and A_1).

8255 BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A ⇒ DATA BUS
0	1	0	1	0	PORT B ⇒ DATA BUS
1	0	0	1	0	PORT C ⇒ DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS ⇒ PORT A
0	1	1	0	0	DATA BUS ⇒ PORT B
1	0	1	0	0	DATA BUS ⇒ PORT C
1	1	1	0	0	DATA BUS ⇒ CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS ⇒ 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS ⇒ 3-STATE



8255 Block Diagram

(RESET)

Reset: A "high" on this input clears all internal registers including the Control Register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the 8080 CPU "outputs" a control word to the 8255. The control word contains information such as "mode", "bit set", "bit reset" etc. that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

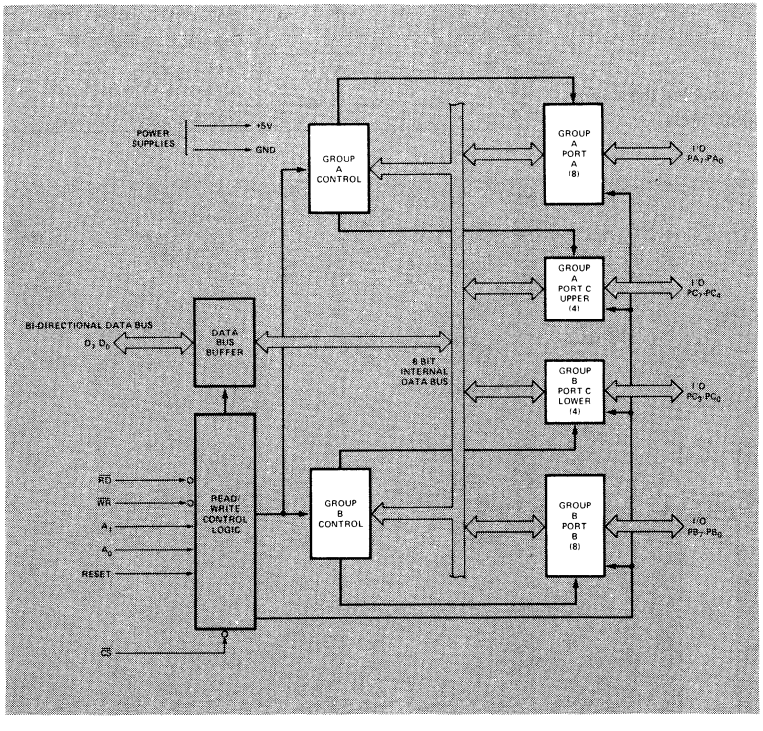
The 8255 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch.

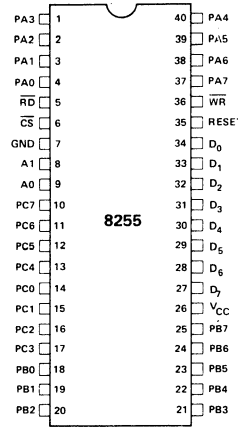
Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B.

8255 BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	Ø VOLTS

8255 DETAILED OPERATIONAL DESCRIPTION

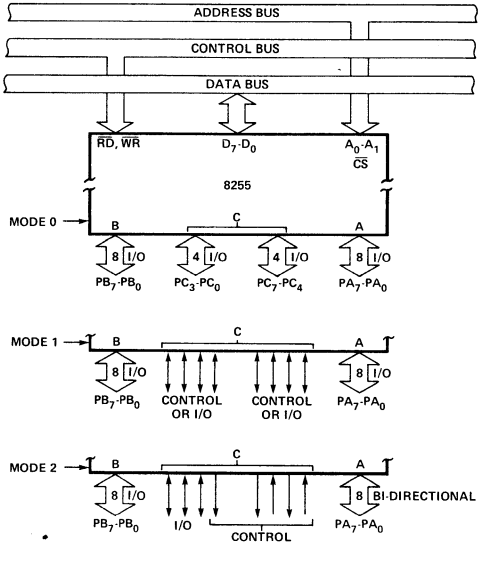
Mode Selection

There are three basic modes of operation that can be selected by the system software:

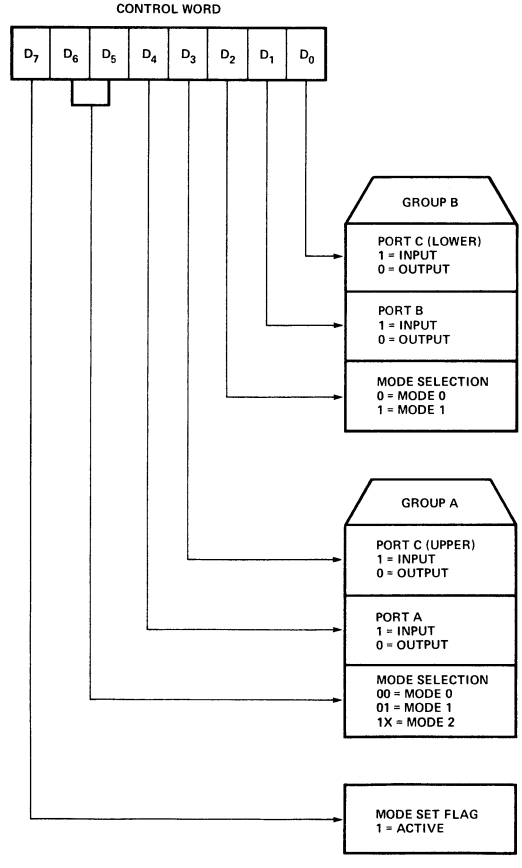
Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the RESET input goes "high" all ports will be set to the Input mode (i.e., all 24 lines will be in the high impedance state). After the RESET is removed the 8255 can remain in the Input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single OUTput instruction. This allows a single 8255 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.



Basic Mode Definitions and Bus Interface

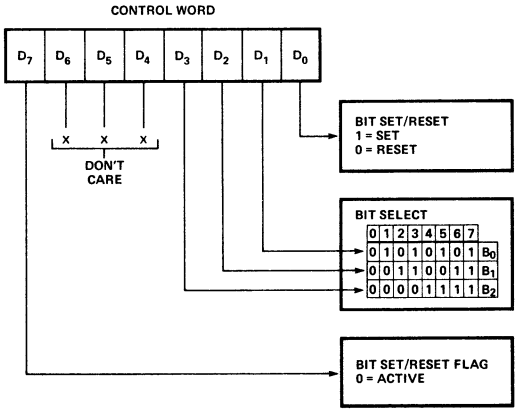


Mode Definition Format

The Mode definitions and possible Mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255 has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.



Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255 is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit set/reset function of Port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

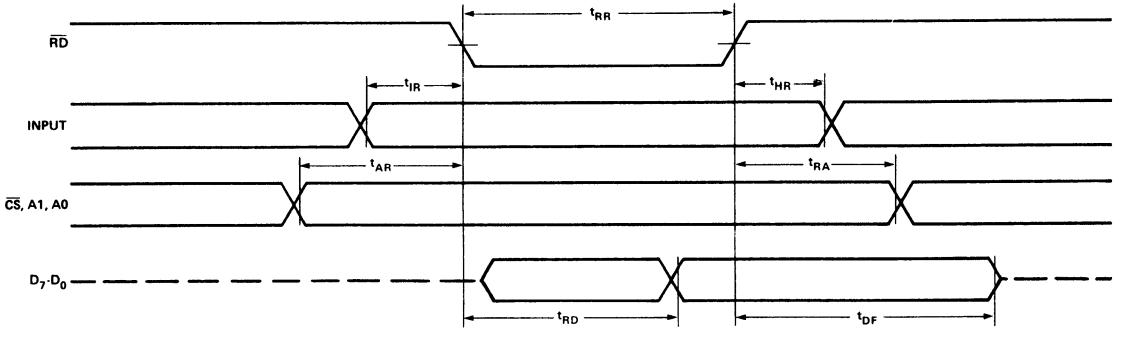
Operating Modes

Mode 0 (Basic Input/Output)

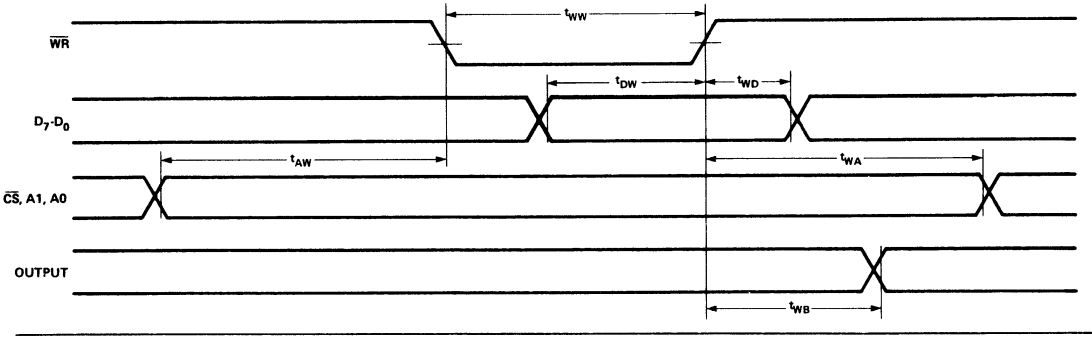
This functional configuration provides simple Input and Output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



Mode 0 (Basic Input)



Mode 0 (Basic Output)

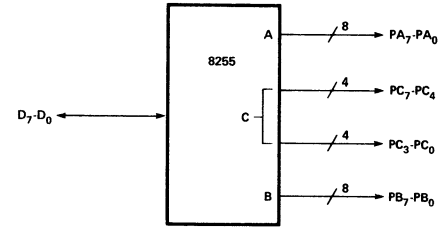
MODE 0 PORT DEFINITION CHART

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 CONFIGURATIONS

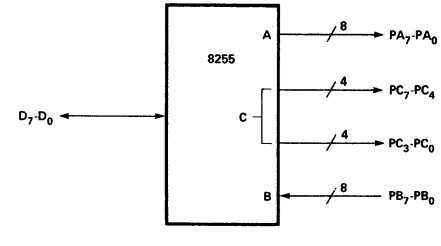
CONTROL WORD #0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0



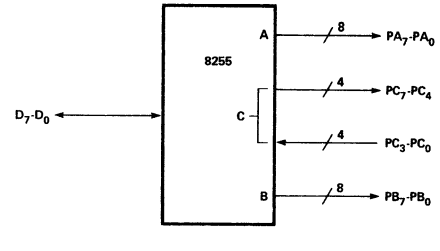
CONTROL WORD #2

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	0



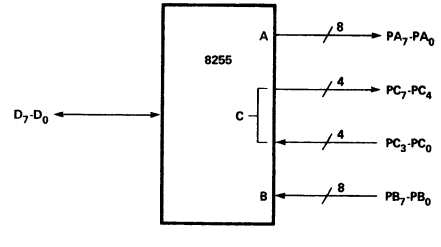
CONTROL WORD #1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	1



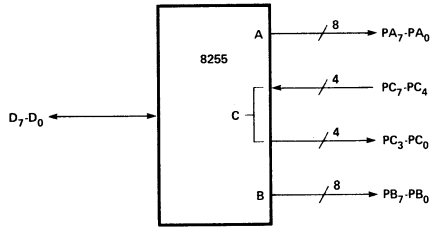
CONTROL WORD #3

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	1



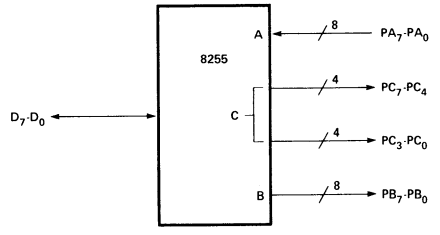
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



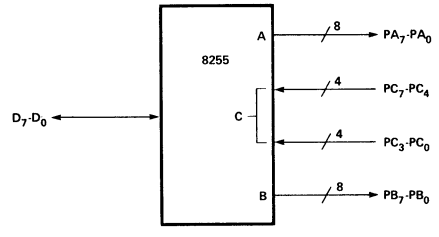
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



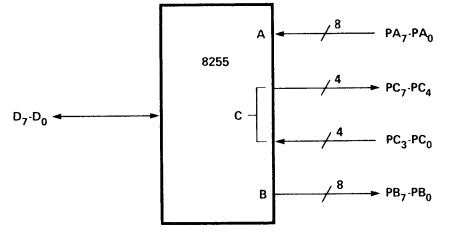
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



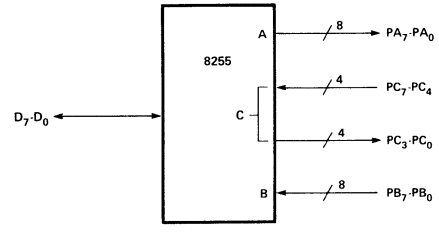
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



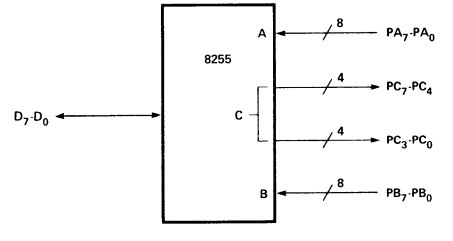
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



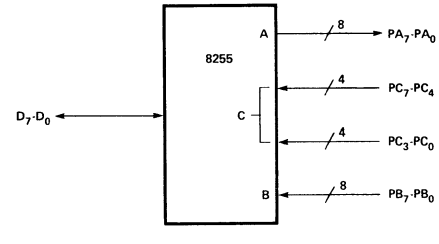
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



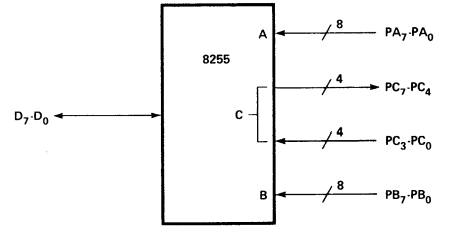
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



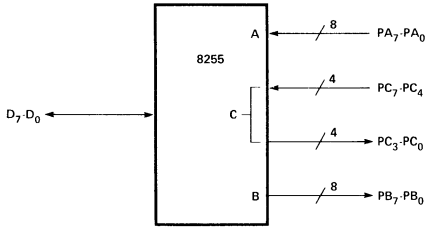
CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1



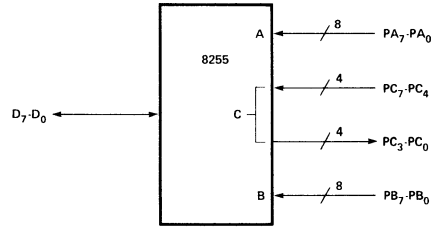
CONTROL WORD #12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	0



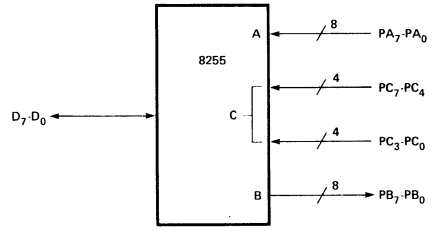
CONTROL WORD #14

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	0



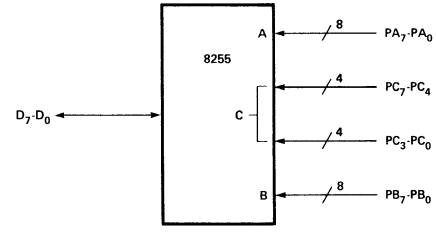
CONTROL WORD #13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	1



CONTROL WORD #15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	1



Operating Modes

Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

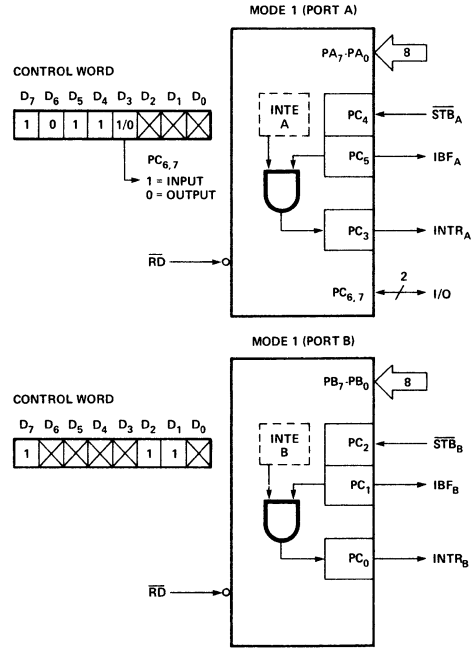
A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

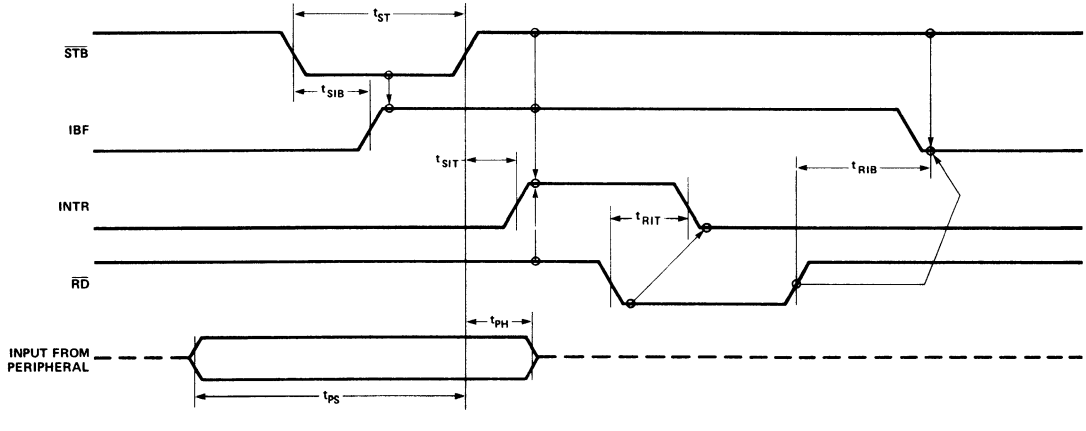
Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.



Mode 1 Input



Mode 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input)

A "low" on this input informs the 8255 that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request)

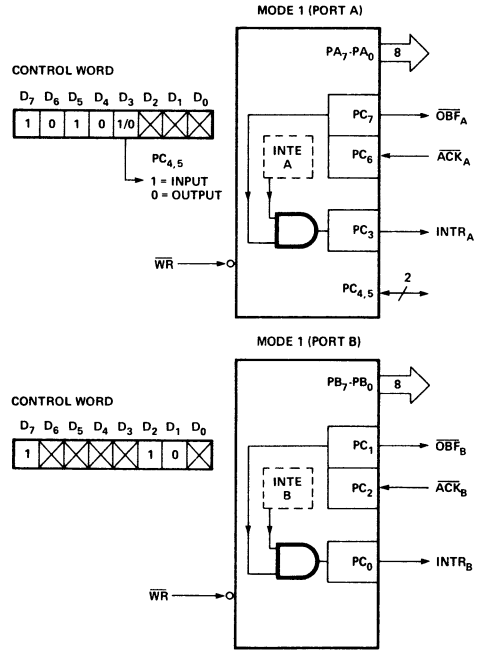
A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set by $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

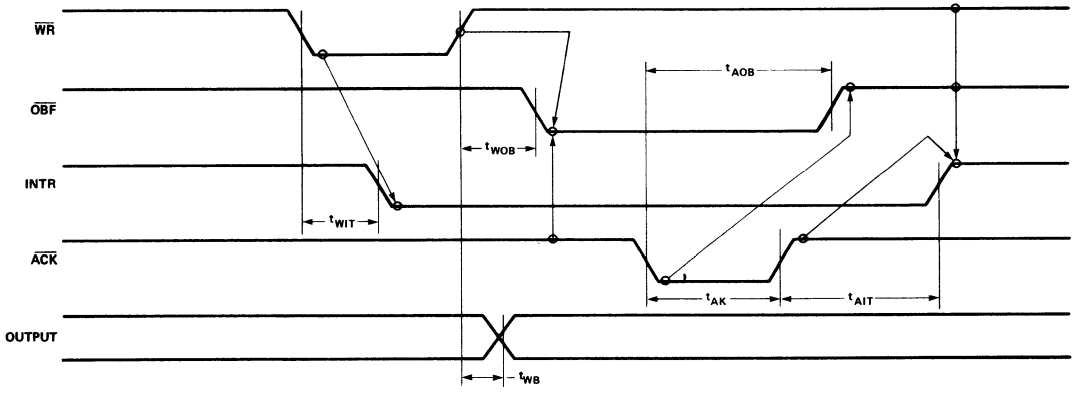
Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.



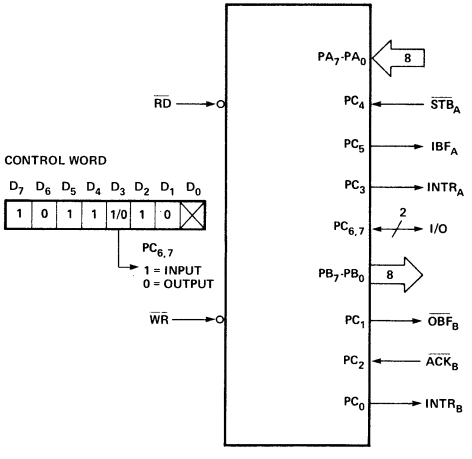
Mode 1 Output



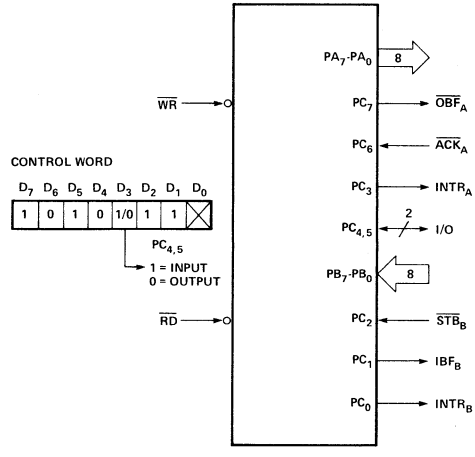
Mode 1 (Strobed Output)

Combinations of Mode 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.



PORT A – (STROBED INPUT)
PORT B – (STROBED OUTPUT)



PORT A – (STROBED OUTPUT)
PORT B – (STROBED INPUT)

Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bi-Directional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge)

A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high-impedance state.

INTE 1 (The INTE Flip-Flop associated with $\overline{OBF}$)

Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input)

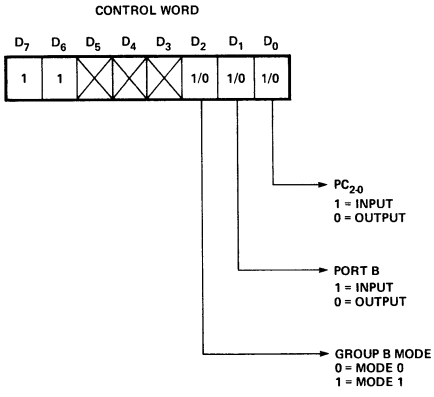
A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

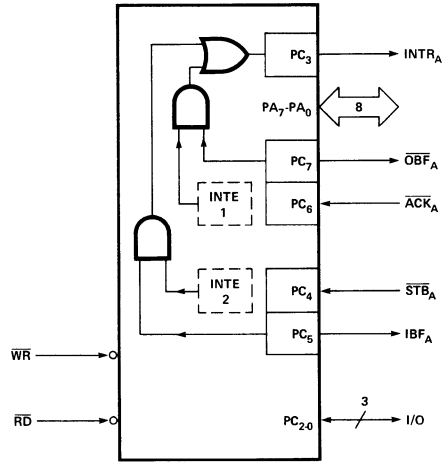
A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop associated with IBF)

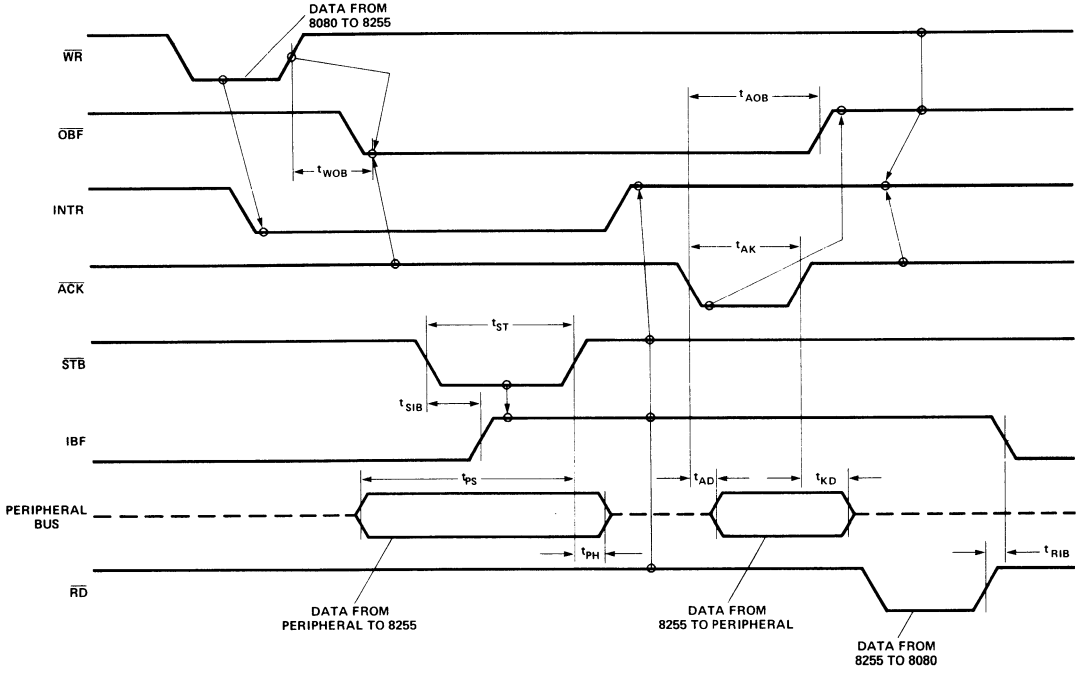
Controlled by bit set/reset of PC_4.



Mode 2 Control Word



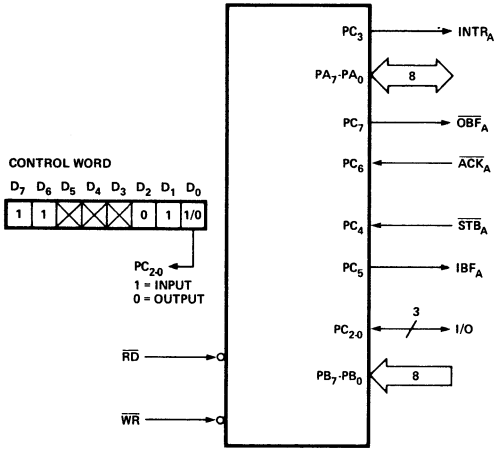
Mode 2



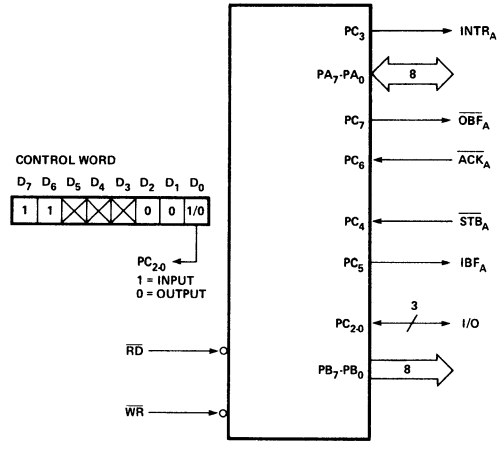
Mode 2 (Bi-directional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

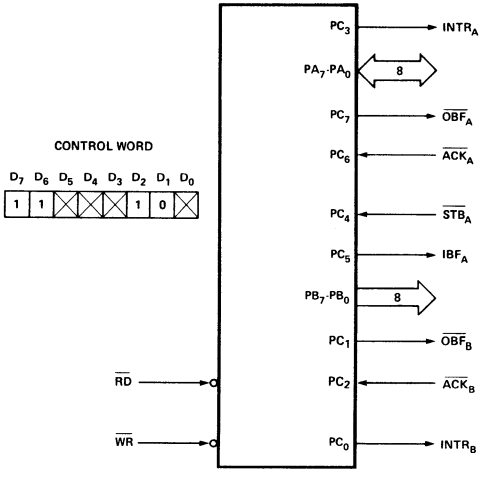
MODE 2 AND MODE 0 (INPUT)



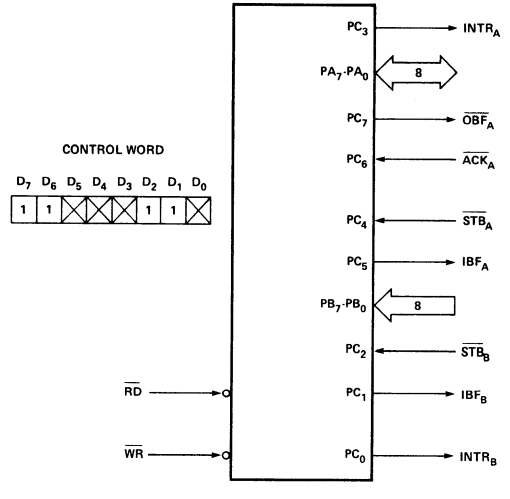
MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)



Mode 2 Combinations

MODE DEFINITION SUMMARY TABLE

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	⟷	
PA_1	IN	OUT	IN	OUT	⟷	
PA_2	IN	OUT	IN	OUT	⟷	
PA_3	IN	OUT	IN	OUT	⟷	
PA_4	IN	OUT	IN	OUT	⟷	
PA_5	IN	OUT	IN	OUT	⟷	
PA_6	IN	OUT	IN	OUT	⟷	
PA_7	IN	OUT	IN	OUT	⟷	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs –
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs –
Bits in C upper (PC_7-PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

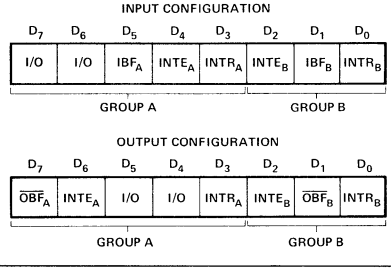
Source Current Capability on Port B and Port C

Any set of **eight** output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

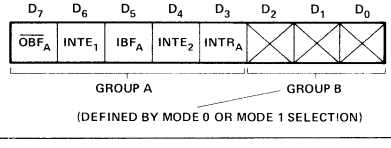
Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.



Mode 1 Status Word Format

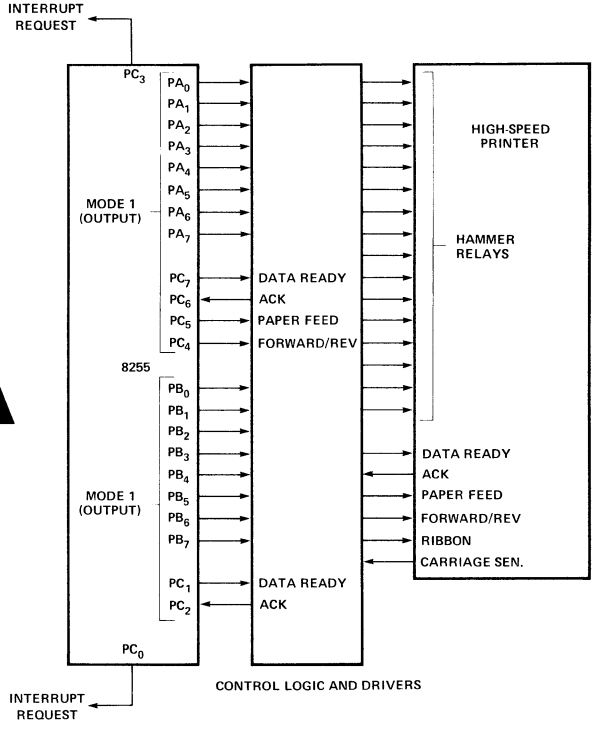


Mode 2 Status Word Format

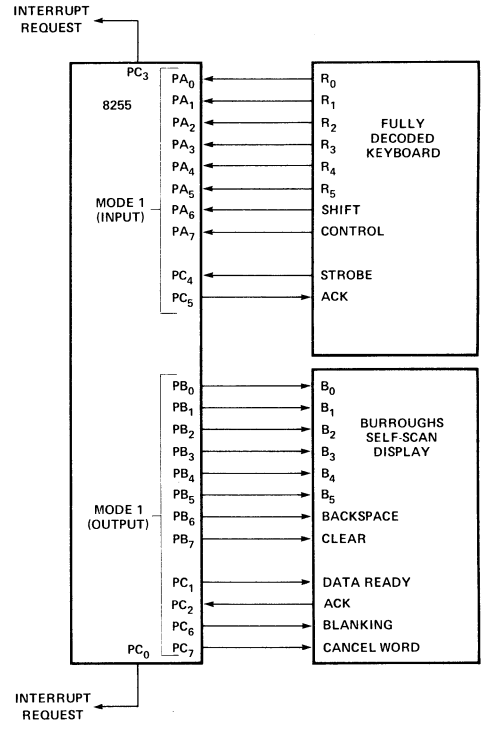
APPLICATIONS OF THE 8255

The 8255 is a very powerful tool for interfacing peripheral equipment to the 8080 microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

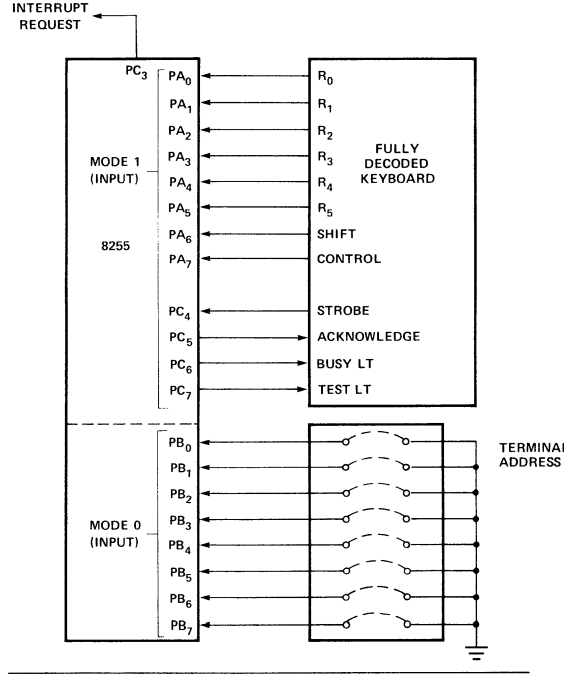
Each peripheral device in a Microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255 is programmed by the I/O service routine and becomes an extension of the systems software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the Detailed Operational Description, a control word can easily be developed to initialize the 8255 to exactly "fit" the application. Here are a few examples of typical applications of the 8255.



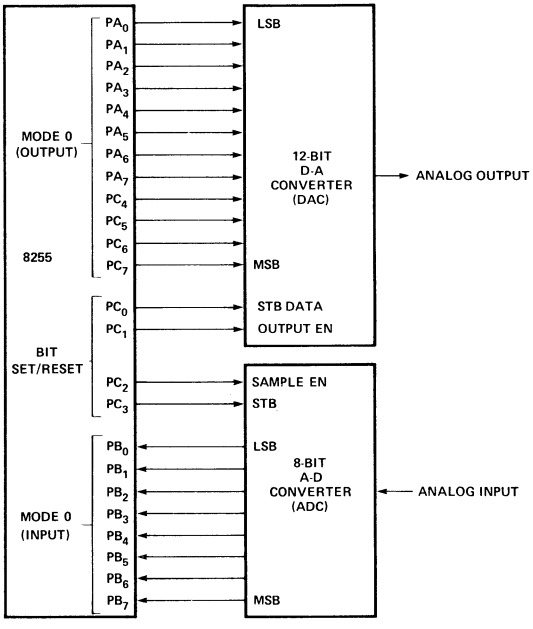
Printer Interface



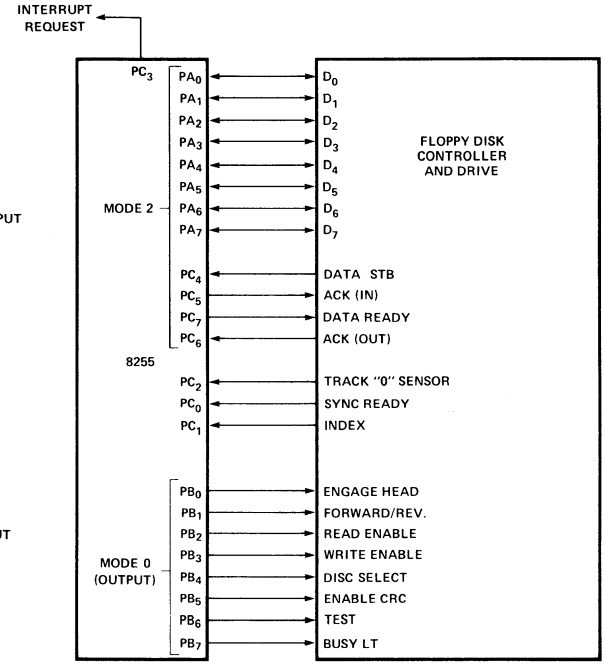
Keyboard and Display Interface



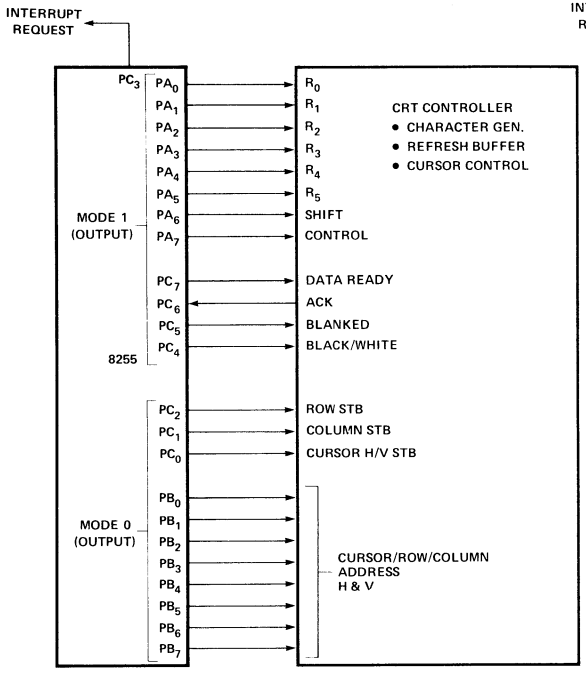
Keyboard and Terminal Address Interface



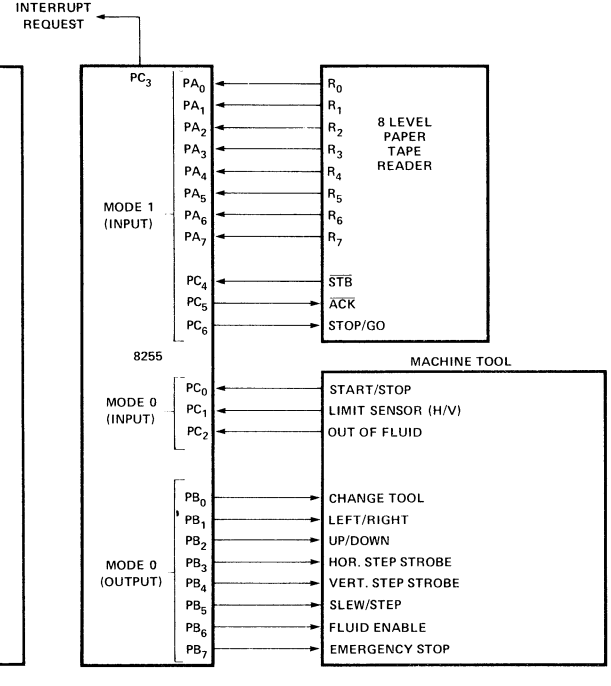
Digital to Analog, Analog to Digital



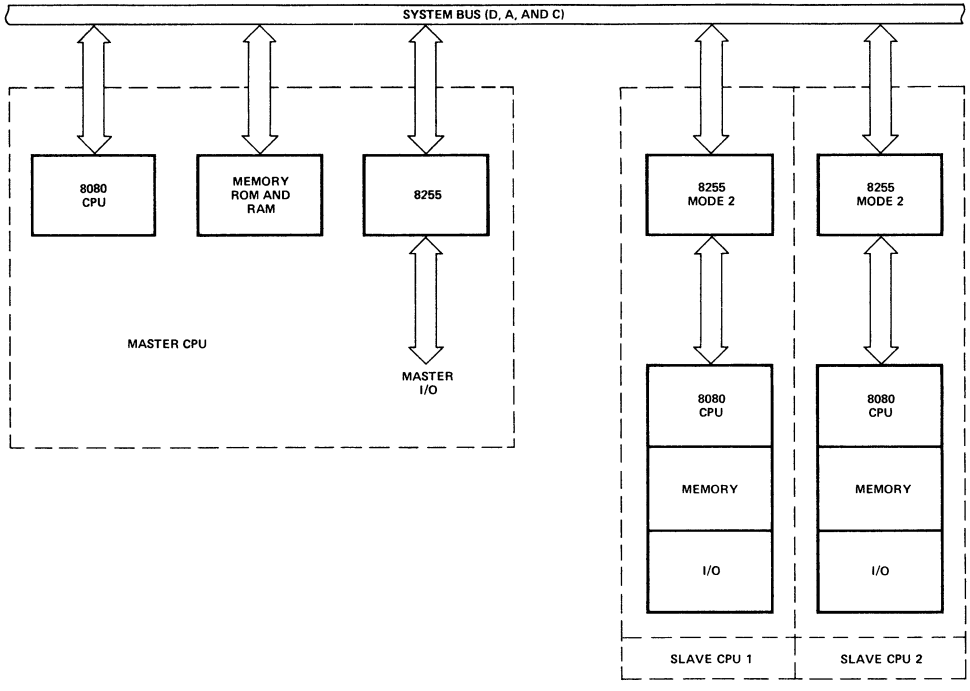
Basic Floppy Disc Interface



Basic CRT Controller Interface



Machine Tool Controller Interface



Distributed Intelligence Multi-Processor Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V ±5%; GND = 0V

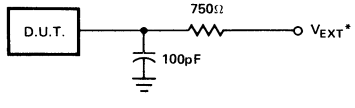
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
I_{OL}(DB)	Output Low Current (Data Bus)	2.5		mA	V_{OL} = 0.45V
I_{OL}(PER)	Output Low Current (Peripheral Port)	1.7		mA	V_{OL} = 0.45V
I_{OH}(DB)	Output High Current (Data Bus)	-400		μA	V_{OH} = 2.4V
I_{OH}(PER)	Output High Current (Peripheral Port)	-200		μA	V_{OH} = 2.4V
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	R_{EXT} = 750Ω; V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC}
I_{OFL}	Output Float Leakage		10	μA	V_{OUT} = GND + 0.45, V_{CC}

Note: 1. Adaptable on any 8 pins from Ports Band C.

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

TEST LOAD CIRCUIT (FOR DB)



* V_{EXT} IS SET AT VARIOUS VOLTAGES DURING TESTING TO GUARANTEE THE SPECIFICATION.

A.C. CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = +5V ±5%; GND = 0V

BUS PARAMETERS:

READ:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	Address Stable Before $\overline{READ}$	0		ns	
t_{RA}	Address Stable After $\overline{READ}$	0		ns	
t_{RR}	$\overline{READ}$ Pulse Width	300		ns	
t_{RD}	Data Valid From $\overline{READ}$		250	ns	CL = 100 pF
t_{DF}	Data Float After $\overline{READ}$		150	ns	CL = 100 pF
		10		ns	CL = 15 pF
t_{RV}	Time Between $\overline{READS}$ and/or $\overline{WRITES}$	850		ns	

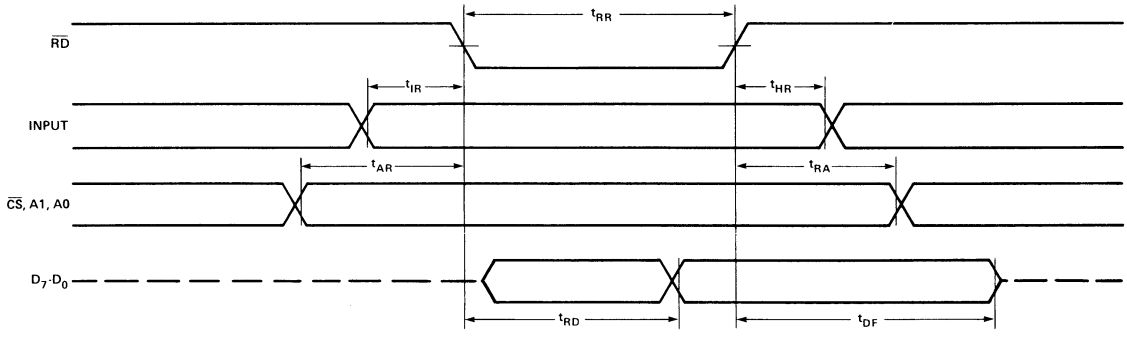
WRITE:

t_{AW}	Address Stable Before $\overline{WRITE}$	0		ns	
t_{WA}	Address Stable After $\overline{WRITE}$	20		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	400		ns	
t_{DW}	Data Valid To $\overline{WRITE}$ (T.E.)	100		ns	
t_{WD}	Data Valid After $\overline{WRITE}$	30		ns	

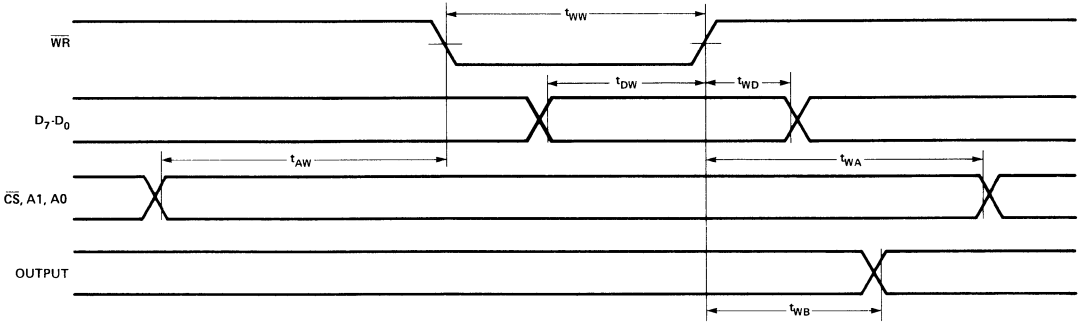
OTHER TIMINGS:

t_{WB}	$\overline{WR}$=1 To Output		350	ns	CL = 100 pF
t_{IR}	Peripheral Data Before $\overline{RD}$	0		ns	
t_{HR}	Peripheral Data After $\overline{RD}$	0		ns	
t_{AK}	$\overline{ACK}$ Pulse Width	300		ns	
t_{ST}	$\overline{STB}$ Pulse Width	500		ns	
t_{PS}	Per. Data Before T.E. Of $\overline{STB}$	0		ns	
t_{PH}	Per. Data After T.E. Of $\overline{STB}$	180		ns	
t_{AD}	$\overline{ACK}$=0 To Output		400	ns	CL = 100 pF
t_{KD}	$\overline{ACK}$=1 To Output Float		250	ns	CL = 100 pF
		20			CL = 15 pF
t_{WOB}	$\overline{WR}$=1 To $\overline{OBF}$=0		650	ns	CL = 100 pF
t_{AOB}	$\overline{ACK}$=0 To $\overline{OBF}$=1		350	ns	CL = 100 pF
t_{SIB}	$\overline{STB}$=0 To IBF=1		300	ns	CL = 100 pF
t_{RIB}	$\overline{RD}$=1 To IBF=0		300	ns	CL = 100 pF
t_{RIT}	$\overline{RD}$=0 To INTR=0		400	ns	CL = 100 pF
t_{SIT}	$\overline{STB}$=1 To INTR=1		300	ns	CL = 100 pF
t_{AIT}	$\overline{ACK}$=1 To INTR=1		350	ns	CL = 100 pF
t_{WIT}	$\overline{WR}$=0 To INTR=0		850	ns	CL = 100 pF

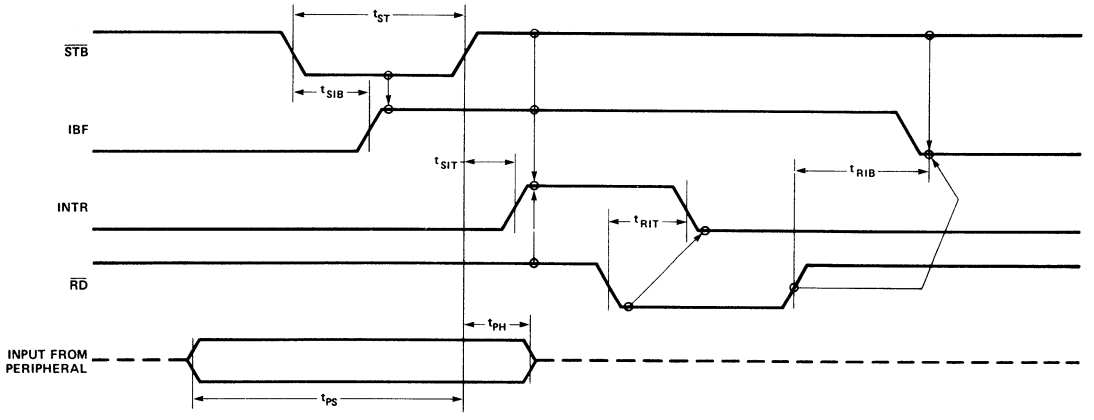
Note: Period of Reset pulse must be at least 50μs during or after power on.
Subsequent Reset pulse can be 500 ns min.



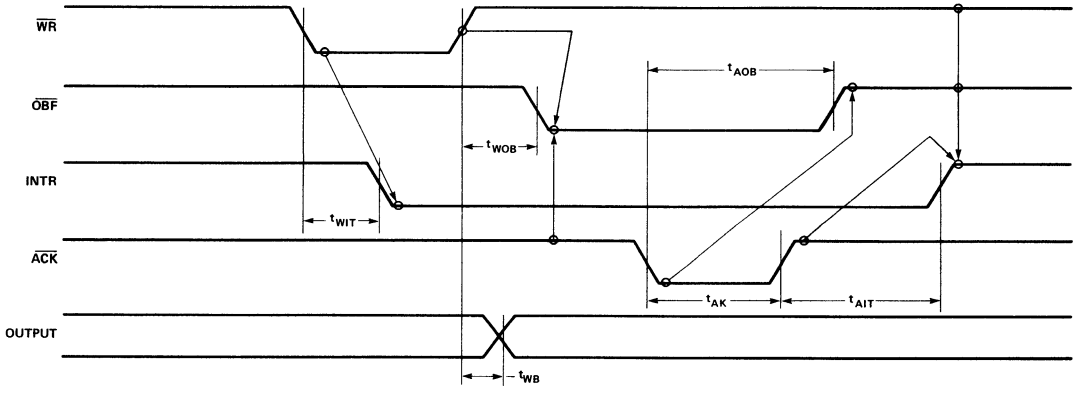
Mode 0 (Basic Input)



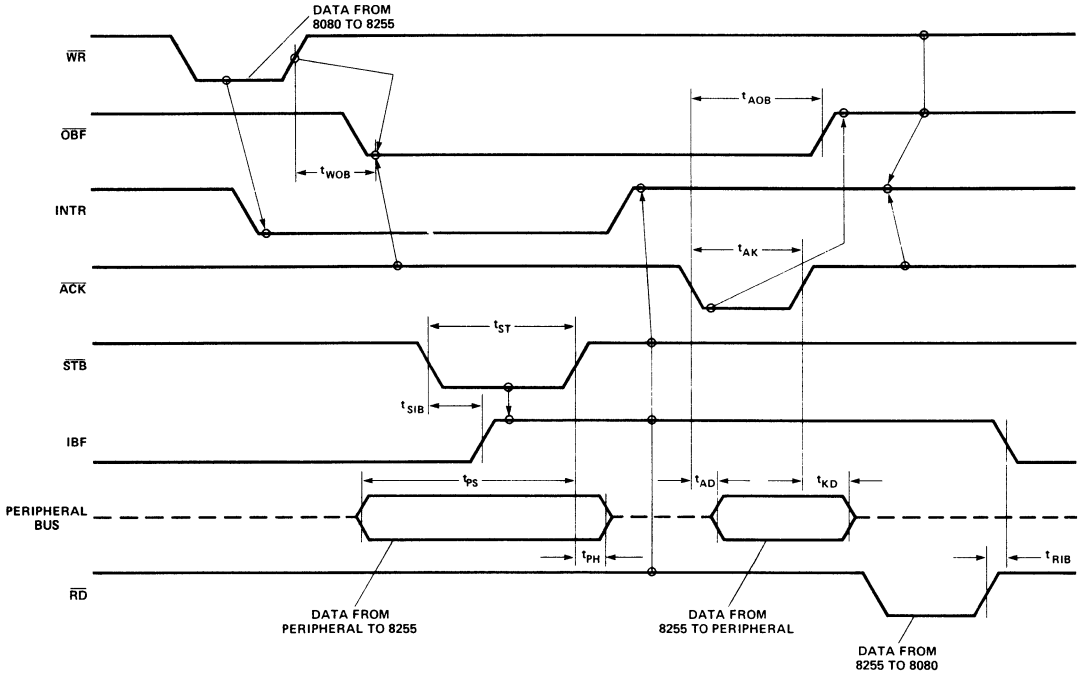
Mode 0 (Basic Output)



Mode 1 (Strobed Input)



Mode 1 (Strobed Output)



Mode 2 (Bi-directional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

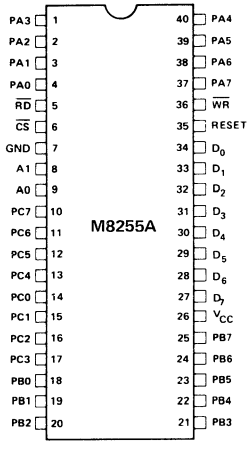
M8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with MCS™-80 Microprocessor Family**
- **Full Military Temperature Range -55° C to +125° C**
- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40 Pin Dual In-Line Package**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**

The M8255A is a general purpose programmable I/O device designed for use with microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bi-directional Bus mode which uses 8 lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the M8255A include bit set and reset capability and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

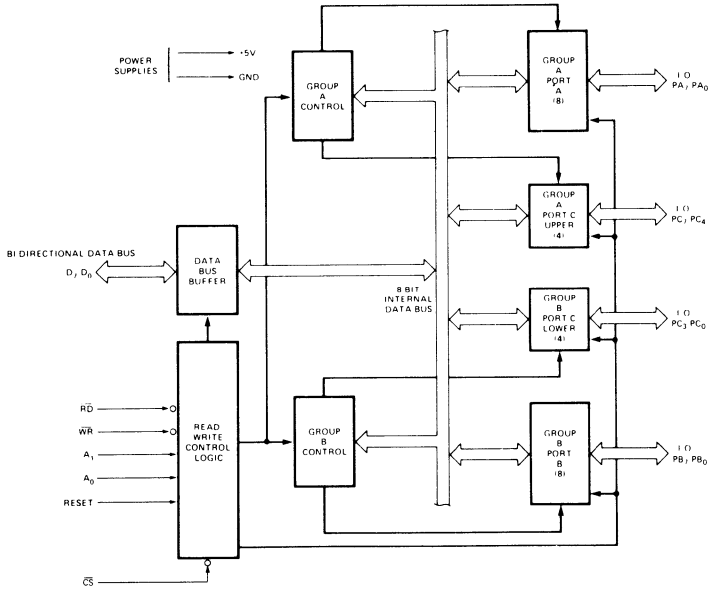
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	Ø VOLTS

M8255A BLOCK DIAGRAM



MCS 80/85

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage On Any Pin
With Respect to GND . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS T_A = -55°C to +125°C; V_{CC} = +5V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-.5		.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL} = 1.7mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -50μA (-100μA for D.B. Port)
I_{OH}[1]	Darlington Drive Current	1.0		4.0	mA	V_{OH} = 1.5V, R_{EXT} = 750Ω
I_{CC}	Power Supply Current			120	mA	
I_{IL}	Input Leakage			10	μA	V_{IN} = V_{CC}
$\|I_{OFL}\|$	Output Float Leakage			10	μA	V_{OUT} = 0.45V/V_{CC}

NOTE:
1. Available on 8 pins only.

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
t_{WP}	Pulse Width of $\overline{WR}$			400	ns	
t_{DW}	Time D.B. Stable Before $\overline{WR}$	50			ns	
t_{WD}	Time D.B. Stable After $\overline{WR}$	35			ns	
t_{AW}	Time Address Stable Before $\overline{WR}$	20			ns	
t_{WA}	Time Address Stable After $\overline{WR}$	20			ns	
t_{CW}	Time $\overline{CS}$ Stable Before $\overline{WR}$	20			ns	
t_{WC}	Time $\overline{CS}$ Stable After $\overline{WR}$	35			ns	
t_{WB}	Delay From $\overline{WR}$ To Output			500	ns	C_L = 50pF
t_{RP}	Pulse Width of $\overline{RD}$	405			ns	
t_{IR}	$\overline{RD}$ Set-Up Time	0			ns	
t_{HR}	Input Hold Time	0			ns	
t_{RD}	Delay From $\overline{RD}$ = 0 To System Bus			295	ns	C_L = 100pF
t_{OD}	Delay From $\overline{RD}$ = 1 To System Bus	10		150	ns	C_L = 15pF/100pF
t_{AR}	Time Address Stable Before $\overline{RD}$	50			ns	
t_{CR}	Time $\overline{CS}$ Stable Before $\overline{RD}$	50			ns	
t_{AK}	Width Of $\overline{ACK}$ Pulse	500			ns	
t_{ST}	Width Of $\overline{STB}$ Pulse	500			ns	
t_{PS}	Set-Up Time For Peripheral	60			ns	
t_{PH}	Hold Time For Peripheral	180			ns	
t_{RA}	Hold Time for A_1, A_0 After $\overline{RD}$ = 1	0			ns	

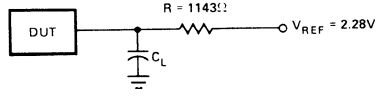
A.C. CHARACTERISTICS (Continued)

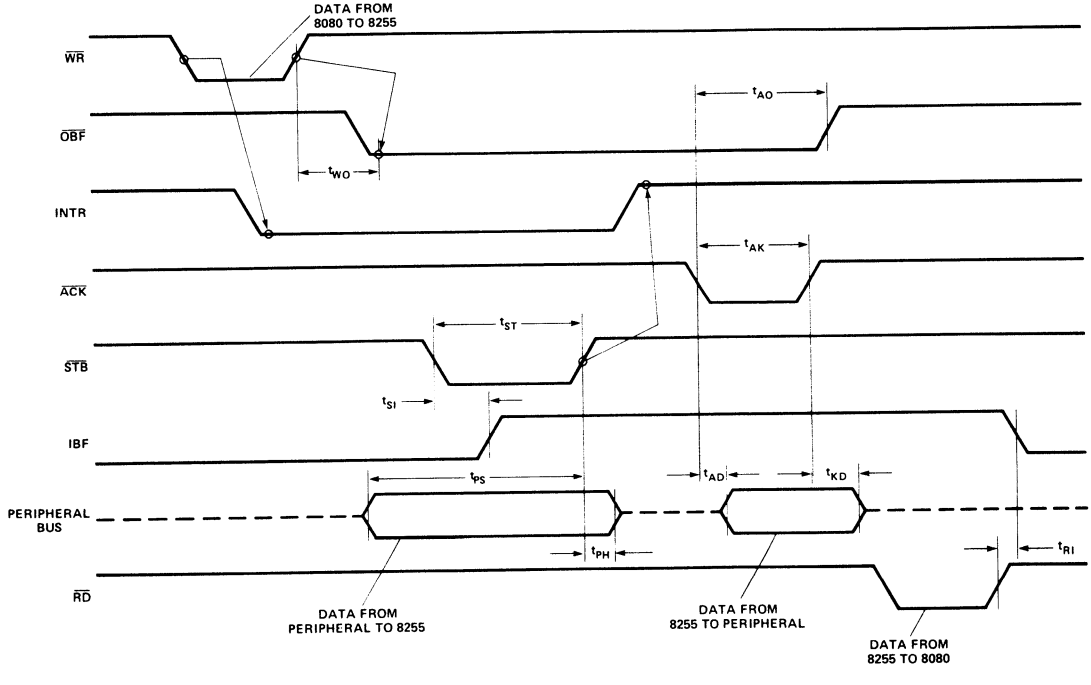
t_{RC}	Hold Time For CS After $\overline{RD}$ = 1	0			ns	
t_{AD}	Time From $\overline{ACK}$ = 0 To Output (Mode 2)			400	ns	C_L = 50pF
t_{KD}	Time From $\overline{ACK}$ = 1 To Output Floating	20		300	ns	C_L = 15pF/50pF
t_{WO}	Time From $\overline{WR}$ = 1 To $\overline{OBF}$ = 0			700	ns	C_L = 50pF
t_{AO}	Time From $\overline{ACK}$ = 0 To $\overline{OBF}$ = 1			450	ns	
t_{SI}	Time From $\overline{STB}$ = 0 To IBF = 1			450	ns	
t_{RI}	Time From $\overline{RD}$ = 1 To IBF = 0			360	ns	

CAPACITANCE $T_A = 25°C$, V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

TEST LOAD CIRCUIT:





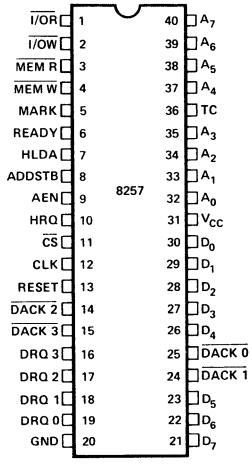
Mode 2 (Bi-directional)

8257
PROGRAMMABLE DMA CONTROLLER

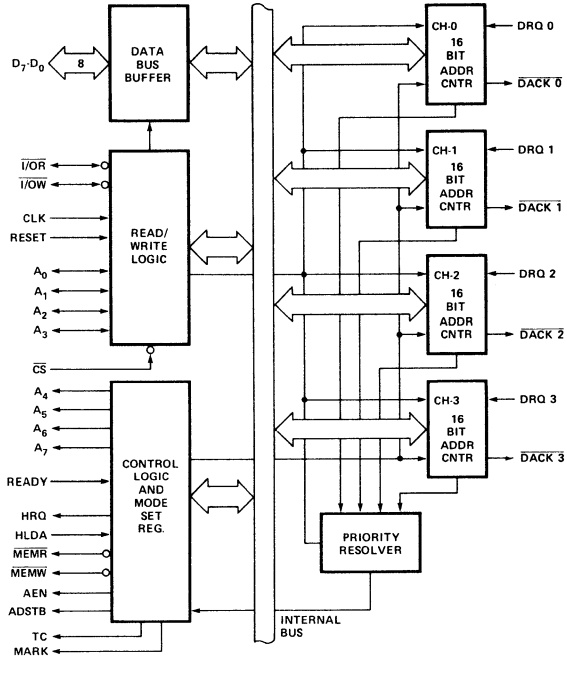
- Four Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Auto Load Mode
- Single TTL Clock
- Single +5V Supply
- Expandable
- 40 Pin Dual-In-Line Package

The 8257 is a four-channel Direct Memory Access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel Microcomputer Systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus is accomplished via the 8080's HOLD function. The 8257 has priority logic that resolves the peripherals requests and issues a composite HOLD request to the 8080. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers and expansion to other 8257 devices for systems that require more than four channels of DMA controlled transfer. The 8257 represents a significant savings in component count for DMA-based 8080 systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D_7-D_0	DATA BUS
A_7-A_0	ADDRESS BUS
$\overline{I/OR}$	I/O $\overline{READ}$
$\overline{I/OW}$	I/O $\overline{WRITE}$
$\overline{MEMR}$	MEMORY $\overline{READ}$
$\overline{MEMW}$	MEMORY $\overline{WRITE}$
CLK	CLOCK INPUT
RESET	RESET INPUT
READY	READY
HRQ	HOLD REQUEST (TO 8080A)
HLDA	HOLD ACKNOWLEDGE (FROM 8080A)

AEN	ADDRESS ENABLE
ADSTB	ADDRESS STROBE
TC	TERMINAL COUNT
MARK	MODULO 128 MARK
DRQ_3-DRQ_0	DMA REQUEST INPUT
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA ACKNOWLEDGE OUT
$\overline{CS}$	CHIP SELECT
V_{CC}	+5 VOLTS
GND	GROUND

These two bits are not modified during a DMA cycle, but can be changed between DMA blocks.

Each channel accepts a DMA Request (DRQn) input and provides a DMA Acknowledge (DACKn) output:

(DRQ 0 - DRQ 3)

DMA Request: These are individual asynchronous channel request inputs used by the peripherals to obtain a DMA cycle. If not in the rotating priority mode then DRQ 0 has the highest priority and DRQ 3 has the lowest. A request can be generated by raising the request line and holding it high until DMA acknowledge. For multiple DMA cycles (Burst Mode) the request line is held high until the DMA acknowledge of the last cycle arrives.

($\overline{\text{DACK 0}}$ - $\overline{\text{DACK 3}}$)

DMA Acknowledge: An active low level on the acknowledge output informs the peripheral connected to that channel that it has been selected for a DMA cycle.

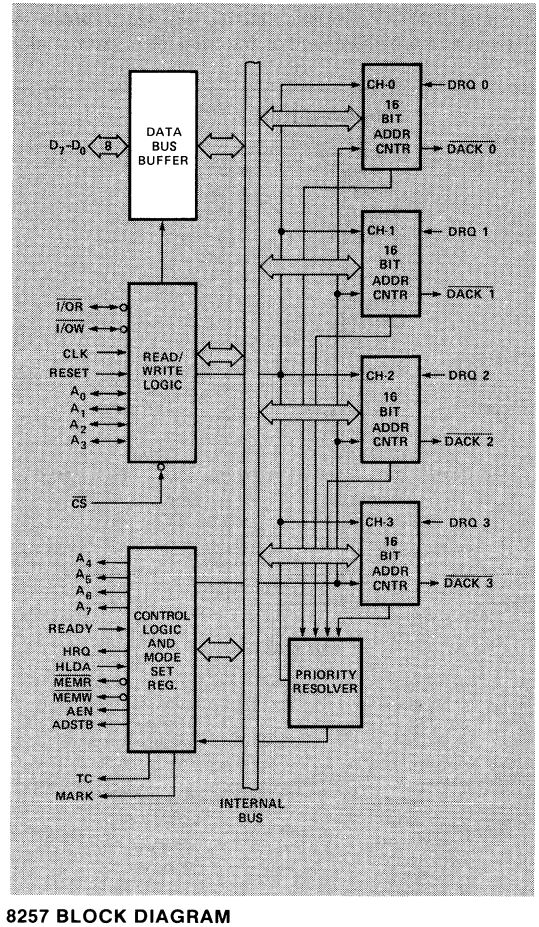
BIT 15	BIT 14	TYPE OF DMA OPERATION
0	0	Verify DMA Cycle
0	1	Write DMA Cycle
1	0	Read DMA Cycle
1	1	(Illegal)

2. Data Bus Buffer

This three-state, bi-directional, eight bit buffer interfaces the 8257 to the 8080 system data bus:

(D_0-D_7)

Data Bus Lines: These are bi-directional three-state lines. When the 8257 is being programmed by the 8080 CPU, eight-bits of data for a DMA address register, a terminal count register or the Mode Set register are received on the data bus. When the 8080 CPU reads a DMA address register, a terminal count register or the Status register, the data is sent to the 8080 over the data bus. During DMA cycles (when the 8257 is the bus master), the 8257 will output the most significant eight-bits of the memory address (from one of the DMA address registers) to the 8212 latch via the data bus. These address bits will be transferred at the beginning of the DMA cycle; the bus will then be released to handle the memory data transfer during the balance of the DMA cycle.



8257 BLOCK DIAGRAM

8257 BASIC FUNCTIONAL DESCRIPTION

General

The 8257 is a programmable, Direct Memory Access (DMA) device which, when coupled with a single Intel® 8212 I/O port device, provides a complete four-channel DMA controller for use in 8080 microcomputer systems. After being initialized by the 8080 program, the 8257 can transfer a block of data, containing up to 16,384 bytes, between memory and a peripheral device directly, without further intervention required of the CPU. Upon receiving a DMA transfer request from an enabled peripheral, the 8257:

- Acquires control of the system bus.
- Acknowledges that requesting peripheral which is connected to the highest priority channel.
- Outputs the least significant eight bits of the memory address onto system address lines A_0-A_7, outputs the most significant eight bits of the memory address to the 8212 I/O port via the data bus (the 8212 places these address bits on lines A_8-A_{15}, and
- Generates the appropriate memory and I/O read/write control signals that cause the peripheral to receive or deposit a data byte directly from or to the addressed location in memory.

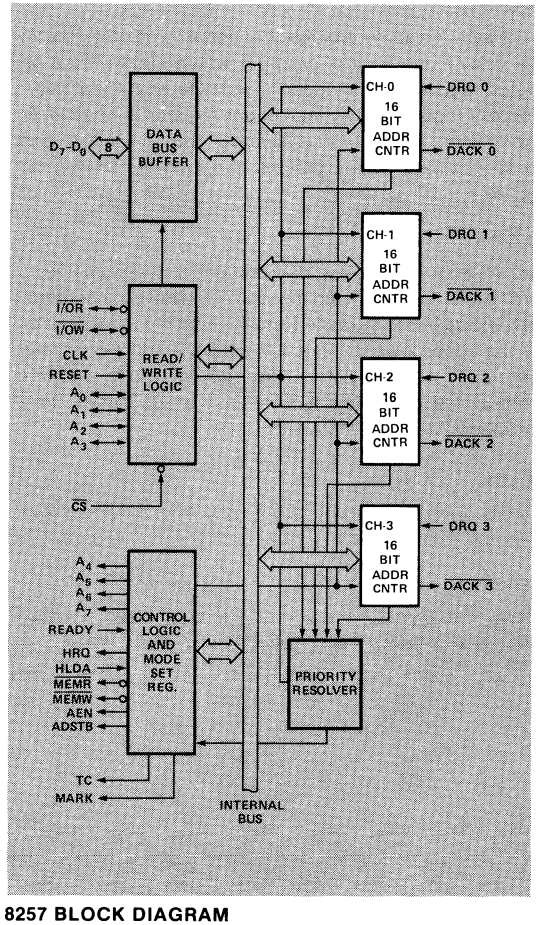
The 8257 will retain control of the system bus and repeat the transfer sequence, as long as a peripheral maintains its DMA request. Thus, the 8257 can transfer a block of data to/from a high speed peripheral (e.g., a sector of data on a floppy disk) in a single "burst". When the specified number of data bytes have been transferred, the 8257 activates its Terminal Count (TC) output, informing the CPU that the operation is complete.

The 8257 offers three different modes of operation: (1) DMA read, which causes data to be transferred from memory to a peripheral; (2) DMA write, which causes data to be transferred from a peripheral to memory; and (3) DMA verify, which does not actually involve the transfer of data. When an 8257 channel is in the DMA verify mode, it will respond the same as described for transfer operations, except that no memory or I/O read/write control signals will be generated, thus preventing the transfer of data. The 8257, however, will gain control of the system bus and will acknowledge the peripheral's DMA request for each DMA cycle. The peripheral can use these acknowledge signals to enable an internal access of each byte of a data block in order to execute some verification procedure, such as the accumulation of a CRC (Cyclic Redundancy Code) checkword. For example, a block of DMA verify cycles might follow a block of DMA read cycles (memory to peripheral) to allow the peripheral to verify its newly acquired data.

Block Diagram Description

1. DMA Channels

The 8257 provides four separate DMA channels (labeled CH-0 to CH-3). Each channel includes two sixteen-bit registers: (1) a DMA address register, and (2) a terminal count register. Both registers must be initialized before a channel is enabled. The DMA address register is loaded with the address of the first memory location to be accessed. The value loaded into the low-order 14-bits of the terminal count register specifies the number of DMA cycles minus one before the Terminal Count (TC) output is activated. For instance, a terminal count of 0 would cause the TC output to be active in the first DMA cycle for that channel. In general, if N = the number of desired DMA cycles, load the value N-1 into the low-order 14-bits of the terminal count register. The most significant two bits of the terminal count register specify the type of DMA operation for that channel:



8257 BLOCK DIAGRAM

3. Read/Write Logic

When the 8080 CPU is programming or reading one of the 8257's registers (i.e., when the 8257 is a "slave" device on the 8080 system bus), the Read/Write Logic accepts the I/O Read ($\overline{I/OR}$) or I/O Write ($\overline{I/OW}$) signal from the 8228 System Controller chip (if Chip Select, CS is true), decodes the least significant four address bits, (A_0-A_3), and either writes the contents of the data bus into the addressed register (if $\overline{I/OW}$ is true) or places the contents of the addressed register onto the data bus (if $\overline{I/OR}$ is true).

During DMA cycles (i.e., when the 8257 is the bus "master"), the Read/Write Logic generates the I/O read and memory write (DMA write cycle) or I/O Write and memory read (DMA read cycle) signals which control the data link with the peripheral that has been granted the DMA cycle.

Note that during DMA transfers Non-DMA I/O devices should be de-selected (disabled) using "AEN" signal to inhibit I/O device decoding of the memory address as an erroneous device address.

($\overline{I/OR}$)

I/O Read: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the 8-bit status register or the upper/lower byte of a 16-bit DMA address register or terminal count register to be read. In the "master" mode, $\overline{I/OR}$ is a control output which is used to access data from a peripheral during the DMA write cycle.

($\overline{I/OW}$)

I/O Write: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the contents of the data bus to be loaded into the 8-bit mode set register or the upper/lower byte of a 16-bit DMA address register or terminal count register. In the "master" mode, $\overline{I/OW}$ is a control output which allows data to be output to a peripheral during a DMA read cycle.

(CLK)

Clock Input: Generally from an Intel® 8224 Clock Generator device. (ϕ2 TTL)

(RESET)

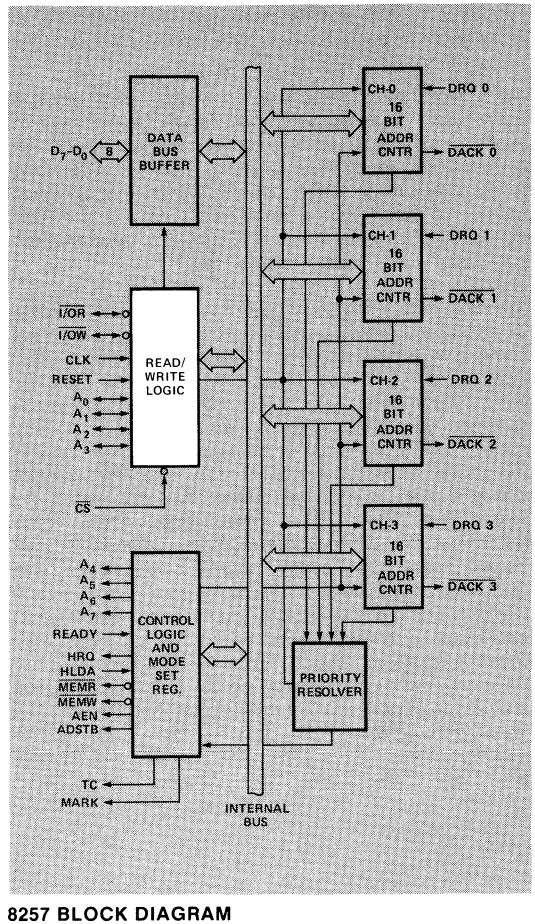
Reset: An asynchronous input (generally from an 8224 device) which clears all registers and control lines.

(A_0-A_3)

Address Lines: These least significant four address lines are bi-directional. In the "slave" mode they are inputs which select one of the registers to be read or programmed. In the "master" mode, they are outputs which constitute the least significant four bits of the 16-bit memory address generated by the 8257.

($\overline{CS}$)

Chip Select: An active-low input which enables the I/O Read or I/O Write input when the 8257 is being read or programmed in the "slave" mode. In the "master" mode, $\overline{CS}$ is automatically disabled to prevent the chip from selecting itself while performing the DMA function.



8257 BLOCK DIAGRAM

4. Control Logic

This block controls the sequence of operations during all DMA cycles by generating the appropriate control signals and the 16-bit address that specifies the memory location to be accessed.

(A_4-A_7)

Address Lines: These four address lines are three-state outputs which constitute bits 4 through 7 of the 16-bit memory address generated by the 8257 during all DMA cycles.

(READY)

Ready: This asynchronous input is used to elongate the memory read and write cycles in the 8257 with wait states if the selected memory requires longer cycles.

(HRQ)

Hold Request: This output requests control of the system bus. In systems with only one 8257, HRQ will normally be applied to the HOLD input on the 8080 CPU.

(HLDA)

Hold Acknowledge: This input from the 8080 indicates that the 8257 has acquired control of the system bus.

($\overline{\text{MEMR}}$)

Memory Read: This active-low three-state output is used to read data from the addressed memory location during DMA Read cycles.

($\overline{\text{MEMW}}$)

Memory Write: This active-low three-state output is used to write data into the addressed memory location during DMA Write cycles.

(ADSTB)

Address Strobe: This output strobes the most significant byte of the memory address into the 8212 device from the data bus.

(AEN)

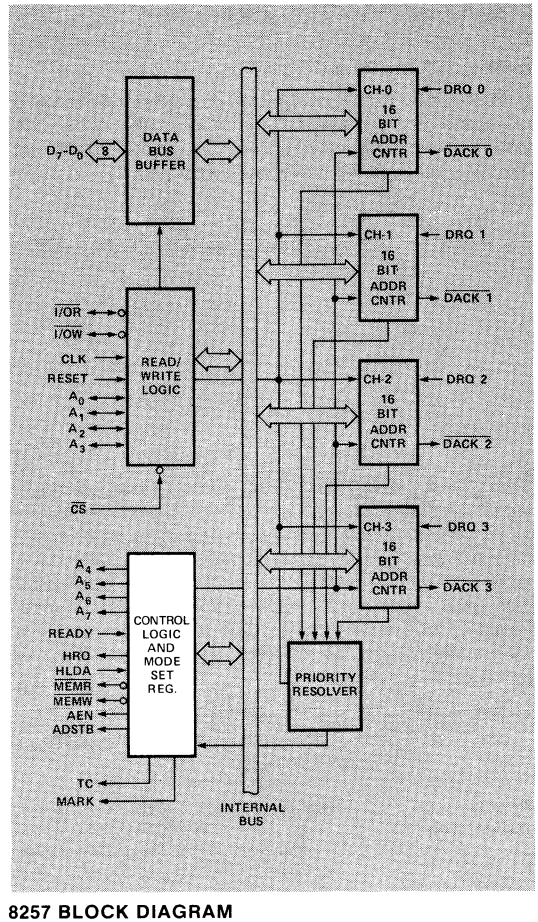
Address Enable: This output is used to disable (float) the System Data Bus and the System Control Bus by use of the Bus Enable input on the Intel® 8228 System Controller chip. It may also be used to disable (float) the System Address Bus by use of an enable on the Address Bus drivers in systems to inhibit non-DMA devices from responding during DMA cycles. It may be further used to isolate the 8257 data bus from the System Data Bus to facilitate the transfer of the 8 most significant DMA address bits over the 8257 data I/O pins without subjecting the System Data Bus to any timing constraints for the transfer. When the 8257 is used in an I/O device structure (as opposed to memory mapped), this AEN output should be used to disable the selection of an I/O device when the DMA address is on the address bus. The I/O device selection should be determined by the DMA acknowledge outputs for the 4 channels.

(TC)

Terminal Count: This output notifies the currently selected peripheral that the present DMA cycle should be the last cycle for this data block. If the TC STOP bit in the Mode Set register is set, the selected channel will be automatically disabled at the end of that DMA cycle. TC is activated when the 14-bit value in the selected channel's terminal count register equals zero. Recall that the low-order 14-bits of the terminal count register should be loaded with the values (n-1), where n = the desired number of the DMA cycles.

(MARK)

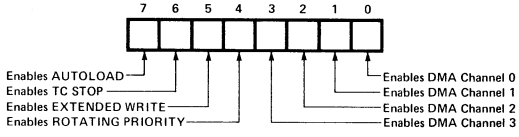
Modulo 128 Mark: This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output. MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block. Only if the total number of DMA cycles (n) is evenly divisable by 128 (and the terminal count register was loaded with n-1), will MARK occur at 128 (and each succeeding multiple of 128) cycles from the beginning of the data block.



8257 BLOCK DIAGRAM

5. Mode Set Register

When set, the various bits in the Mode Set register enable each of the four DMA channels, and allow four different options for the 8257:

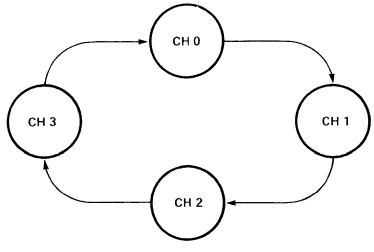


The Mode Set register is normally programmed by the 8080 CPU after the DMA address register(s) and terminal count register(s) are initialized. The Mode Set Register is cleared by the RESET input, thus disabling all options, inhibiting all channels, and preventing bus conflicts on power-up. A channel should not be left enabled unless its DMA address and terminal count registers contain valid values; otherwise, an inadvertent DMA request (DRQn) from a peripheral could initiate a DMA cycle that would destroy memory data.

The various options which can be enabled by bits in the Mode Set register are explained below:

Rotating Priority Bit 4

In the Rotating Priority Mode, the priority of the channels has a circular sequence. After each DMA cycle, the priority of each channel changes. The channel which had just been serviced will have the lowest priority.



If the ROTATING PRIORITY bit is not set (set to a zero), each DMA channel has a fixed priority. In the fixed priority mode, Channel 0 has the highest priority and Channel 3 has the lowest priority. If the ROTATING PRIORITY bit is set to a one, the priority of each channel changes after each DMA cycle (not each DMA request). Each channel moves up to the next highest priority assignment, while the channel which has just been serviced moves to the lowest priority assignment:

	CHANNEL→ JUST SERVICED	CH-0	CH-1	CH-2	CH-3
Priority → Assignments	Highest	CH-1	CH-2	CH-3	CH-0
	↑	CH-2	CH-3	CH-0	CH-1
	↓	CH-3	CH-0	CH-1	CH-2
	Lowest	CH-0	CH-1	CH-2	CH-3

Note that rotating priority will prevent any one channel from monopolizing the DMA mode; consecutive DMA cycles will service different channels if more than one channel is enabled and requesting service. All DMA operations began with Channel 0 initially assigned to the highest priority for the first DMA cycle.

Extended Write Bit 5

If the EXTENDED WRITE bit is set, the duration of both the $\overline{\text{MEMW}}$ and $\overline{\text{I/OW}}$ signals is extended by activating them earlier in the DMA cycle. Data transfers within 8080 microcomputer systems proceed asynchronously to allow use of various types of memory and I/O devices with different access times. If a device cannot be accessed within a specific amount of time it returns a "not ready" indication to the 8257 that causes the 8257 to insert one or more wait states in its internal sequencing. Some devices are fast enough to be accessed without the use of wait states, but if they generate their READY response with the leading edge of the $\overline{\text{I/OW}}$ or $\overline{\text{MEMW}}$ signal (which generally occurs late in the transfer sequence), they would normally cause the 8257 to enter a wait state because it does not receive READY in time. For systems with these types of devices, the Extended Write option provides alternative timing for the I/O and memory write signals which allows the devices to return an early READY and prevents the unnecessary occurrence of wait states in the 8257, thus increasing system throughput.

TC Stop Bit 6

If the TC STOP bit is set, a channel is disabled (i.e., its enable bit is reset) after the Terminal Count (TC) output goes true, thus automatically preventing further DMA operation on that channel. The enable bit for that channel must be re-programmed to continue or begin another DMA operation. If the TC STOP bit is not set, the occurrence of the TC output has no effect on the channel enable bits. In this case, it is generally the responsibility of the peripheral to cease DMA requests in order to terminate a DMA operation.

Auto Load Bit 7

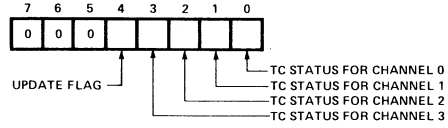
The Auto Load mode permits Channel 2 to be used for repeat block or block chaining operations, without immediate software intervention between blocks. Channel 2 registers are initialized as usual for the first data block; Channel 3 registers, however, are used to store the block re-initialization parameters (DMA starting address, terminal count and DMA transfer mode). After the first block of DMA cycles is executed by Channel 2 (i.e., after the TC output goes true), the parameters stored in the Channel 3 registers are transferred to Channel 2 during an "update" cycle. Note that the TC STOP feature, described above, has no effect on Channel 2 when the Auto Load bit is set.

If the Auto Load bit is set, the initial parameters for Channel 2 are automatically duplicated in the Channel 3 registers when Channel 2 is programmed. This permits repeat block operations to be set up with the programming of a single channel. Repeat block operations can be used in applications such as CRT refreshing. Channels 2 and 3 can still be loaded with separate values if Channel 2 is loaded before loading Channel 3. Note that in the Auto Load mode, Channel 3 is still available to the user if the Channel 3 enable bit is set, but use of this channel will change the values to be auto loaded into Channel 2 at update time. All that is necessary to use the Auto Load feature for chaining operations is to reload Channel 3 registers at the conclusion of each update cycle with the new parameters for the next data block transfer.

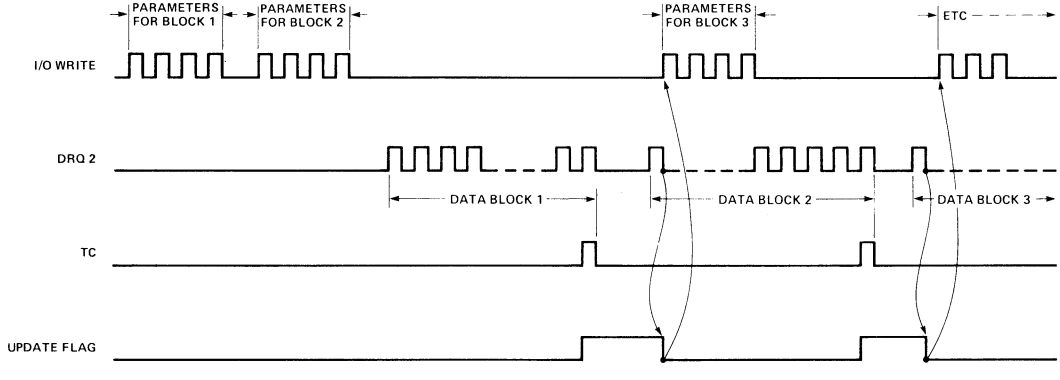
Each time that the 8257 enters an update cycle, the update flag in the status register is set and parameters in Channel 3 are transferred to Channel 2, non-destructively for Channel 3. The actual re-initialization of Channel 2 occurs at the beginning of the next channel 2 DMA cycle after the TC cycle. This will be the first DMA cycle of the new data block for Channel 2. The update flag is cleared at the conclusion of this DMA cycle. For chaining operations, the update flag in the status register can be monitored by the 8080 to determine when the re-initialization process has been completed so that the next block parameters can be safely loaded into Channel 3.

6. Status Register

The eight-bit status register indicates which channels have reached a terminal count condition and includes the update flag described previously.



The TC status bits are set when the Terminal Count (TC) output is activated for that channel. These bits remain set until the status register is read or the 8257 is reset. The UPDATE FLAG, however, is not affected by a status register read operation. The UPDATE FLAG can be cleared by resetting the 8257, by changing to the non-auto load mode (i.e., by resetting the AUTO LOAD bit in the Mode Set register) or it can be left to clear itself at the completion of the update cycle. The purpose of the UPDATE FLAG is to prevent the 8080 from inadvertently skipping a data block by overwriting a starting address or terminal count in the Channel 3 registers before those parameters are properly auto-loaded into Channel 2.



AUTOLOAD TIMING

8257 DETAILED OPERATIONAL SUMMARY

Programming and Reading the 8257 Registers

There are four pairs of "channel registers": each pair consisting of a 16-bit DMA address register and a 16-bit terminal count register (one pair for each channel). The 8257 also includes two "general registers": one 8-bit Mode Set register and one 8-bit Status register. The registers are loaded or read when the 8080 executes a write or read instruction that addresses the 8257 device and the appropriate register within the 8257. The 8228 generates the appropriate read or write control signal (generally $\overline{I/OR}$ or $\overline{I/OW}$ while the 8080 places a 16-bit address on the system address bus, and either outputs the data to be written onto the system data bus or accepts the data being read from the data bus. All or some of the most significant 12 address bits A_4-A_{15} (depending on the systems memory, I/O configuration) are usually decoded to produce the chip select ($\overline{CS}$) input to the 8257. An I/O Write input (or Memory Write in memory mapped I/O configurations, described below) specifies that the addressed register is to be programmed, while an I/O Read input (or Memory Read) specifies that the addressed register is to be read. Address bit 3 specifies whether a "channel register" ($A_3 = 0$) or the Mode Set (program only)/Status (read only) register ($A_3 = 1$) is to be accessed.

The least significant three address bits, A_0-A_2, indicate the specific register to be accessed. When accessing the Mode Set or Status register, A_0-A_2 are all zero. When accessing a channel register bit A_0 differentiates between the DMA address register ($A_0 = 0$) and the terminal count register ($A_0 = 1$), while bits A_1 and A_2 specify one of the four channels. Because the "channel registers" are 16-bits, two program instruction cycles are required to load or read an entire register. The 8257 contains a first/last (F/L) flip flop which toggles at the completion of each channel program or read operation. The F/L flip flop determines whether the upper or lower byte of the register is to be accessed. The F/L flip flop is reset by the RESET input and whenever the Mode Set register is loaded. To maintain proper synchronization when accessing the "channel registers" all channel command instruction operations should occur in pairs, with the lower byte of a register always being accessed first. Do not allow $\overline{CS}$ to clock while either $\overline{I/OR}$ or $\overline{I/OW}$ is active, as this will cause an erroneous F/L flip flop state. In systems utilizing an interrupt structure, interrupts should be disabled prior to any paired programming operations to prevent an interrupt from splitting them. The result of such a split would leave the F/L F/F in the wrong state. This problem is particularly obvious when other DMA channels are programmed by an interrupt structure.

CONTROL INPUT	$\overline{CS}$	$\overline{I/OW}$	$\overline{I/OR}$	A_3
Program Half of a Channel Register	0	0	1	0
Read Half of a Channel Register	0	1	0	0
Program Mode Set Register	0	0	1	1
Read Status Register	0	1	0	1

8257 REGISTER SELECTION

REGISTER	BYTE	ADDRESS INPUTS				F/L	*BI-DIRECTIONAL DATA BUS							
		A_3	A_2	A_1	A_0		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CH-0 DMA Address	LSB	0	0	0	0	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
	MSB	0	0	0	0	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
CH-0 Terminal Count	LSB	0	0	0	1	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	MSB	0	0	0	1	1	Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8
CH-1 DMA Address	LSB	0	0	1	0	0	Same as Channel 0							
	MSB	0	0	1	0	1								
CH-1 Terminal Count	LSB	0	0	1	1	0								
	MSB	0	0	1	1	1								
CH-2 DMA Address	LSB	0	1	0	0	0	Same as Channel 0							
	MSB	0	1	0	0	1								
CH-2 Terminal Count	LSB	0	1	0	1	0								
	MSB	0	1	0	1	1								
CH-3 DMA Address	LSB	0	1	1	0	0	Same as Channel 0							
	MSB	0	1	1	0	1								
CH-3 Terminal Count	LSB	0	1	1	1	0								
	MSB	0	1	1	1	1								
MODE SET (Program only)	—	1	0	0	0	0	AL	TCS	EW	RP	EN3	EN2	EN1	EN0
STATUS (Read only)	—	1	0	0	0	0	0	0	0	UP	TC3	TC2	TC1	TC0

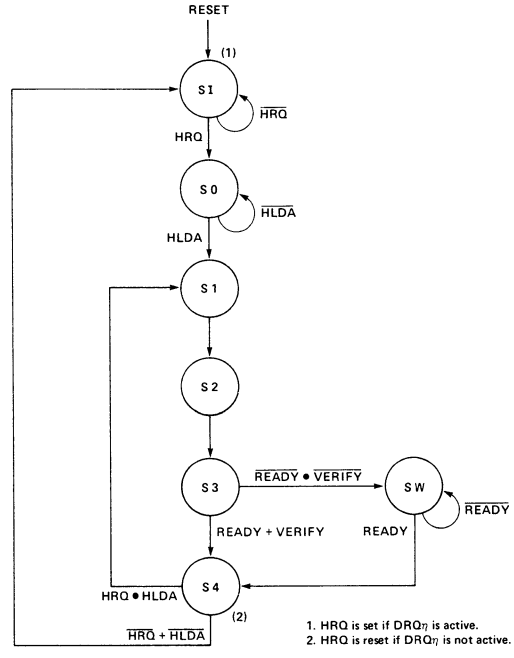
*A_0-A_{15}: DMA Starting Address, C_0-C_{13}: Terminal Count value (N-1), Rd and Wr: DMA Verify (00), Write (01) or Read (10) cycle selection, AL: Auto Load, TCS: TC STOP, EW: EXTENDED WRITE, RP: ROTATING PRIORITY, EN3-EN0: CHANNEL ENABLE MASK, UP: UPDATE FLAG, TC3-TC0: TERMINAL COUNT STATUS BITS.

DMA Operation

Internal 8257 operations may proceed through seven different states. The duration of a state is defined by the clock input. When the 8257 is not executing a DMA cycle, it is in the idle state, S_I. A DMA cycle begins when one or more DMA Request (DRQn) lines become active. The 8257 then enters state S_0, sends a Hold Request (HRQ) to the 8080 and waits for as many S_0 states as are necessary for the 8080 to return a Hold Acknowledge (HLDA). For each S_0 state, the DMA Request lines are again sampled and DMA priority is resolved (according to the fixed or rotating priority scheme). When HLDA is received, the DMA Acknowledge ($\overline{DACK}n$) line for the highest priority requesting channel is activated, thus selecting that channel and its peripheral for the DMA cycle. The 8257 then proceeds to state S_1. Note that the DMA Request (DRQn) input should remain high until either $\overline{DACK}n$ is received for a single DMA cycle service, or until both the $\overline{DACK}n$ and TC outputs are received when transferring an entire data block in a "burst" mode. If the 8257 should lose control of the system bus (i.e., if HLDA goes false), the DMA Acknowledge will be removed after the current DMA cycle is completed and no more DMA cycles will occur until the 8257 again acquires control of the system bus.

Each DMA cycle will consist of at least four internal states: S_1, S_2, S_3, and S_4. If the access time for the memory or I/O devices involved is not fast enough to return the required READY response and complete a byte transfer within the specified amount of time, one or more wait states (SW) are inserted between states S_3 and S_4. Recall that in certain cases the Extended Write option can eliminate the need for a wait state. Note that a READY response is not required during DMA verify cycles. Specified minimum/maximum values for READY setup time (t_{RS}), write data setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) are listed under A.C. CHARACTERISTICS and are illustrated in the accompanying timing diagrams.

During DMA write cycles, the I/O Read ($\overline{I/OR}$) output is generated at the beginning of state S_2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S_3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S_2 and the I/O Write (I/OW) output goes true at the beginning of of state S_3. Recall that no read or write control signals are generated during DMA verify cycles. Extended $\overline{WR}$ for MEM and I/O will be generated in S_2.

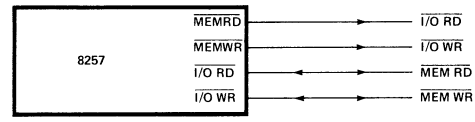


DMA OPERATION STATE DIAGRAM

Memory Mapped I/O Configurations

The 8257 can be connected to the system bus as a memory device instead of as an I/O device for memory mapped I/O configurations by connecting the system memory control lines to the 8257's I/O control lines and the system I/O control lines to the 8257's memory control lines.

This configuration permits use of the 8080's considerably larger repertoire of memory instructions when reading or loading the 8257's registers. Note that with this connection, the programming of the Read (bit 15) and Write (bit 14) bits in the terminal count register will have a different meaning:



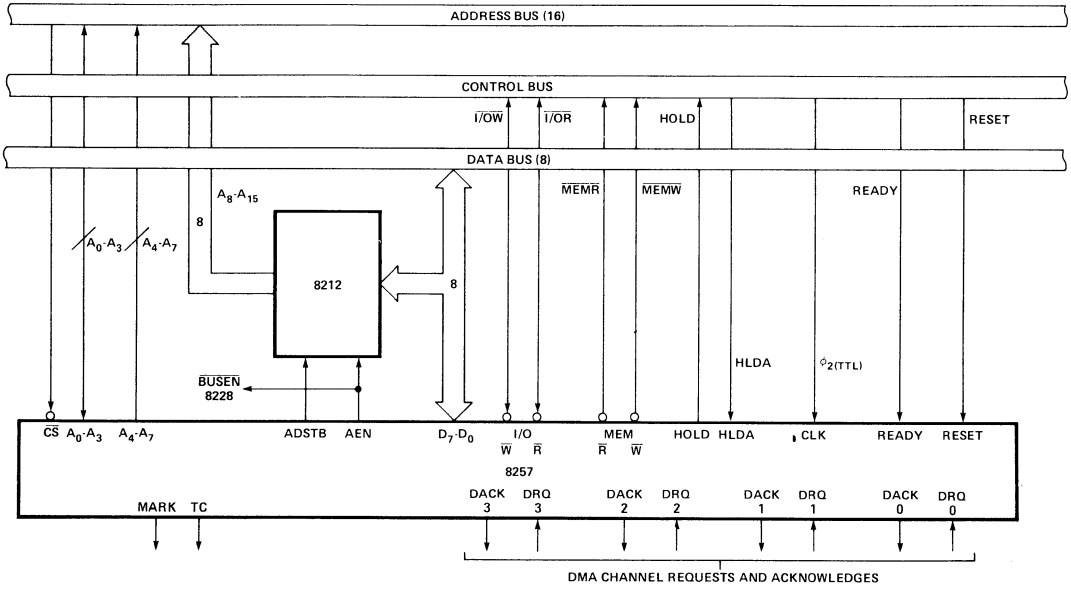
SYSTEM INTERFACE FOR MEMORY MAPPED I/O

BIT 15 READ	BIT 14 WRITE	
0	0	DMA Verify Cycle
0	1	DMA Read Cycle
1	0	DMA Write Cycle
1	1	Illegal

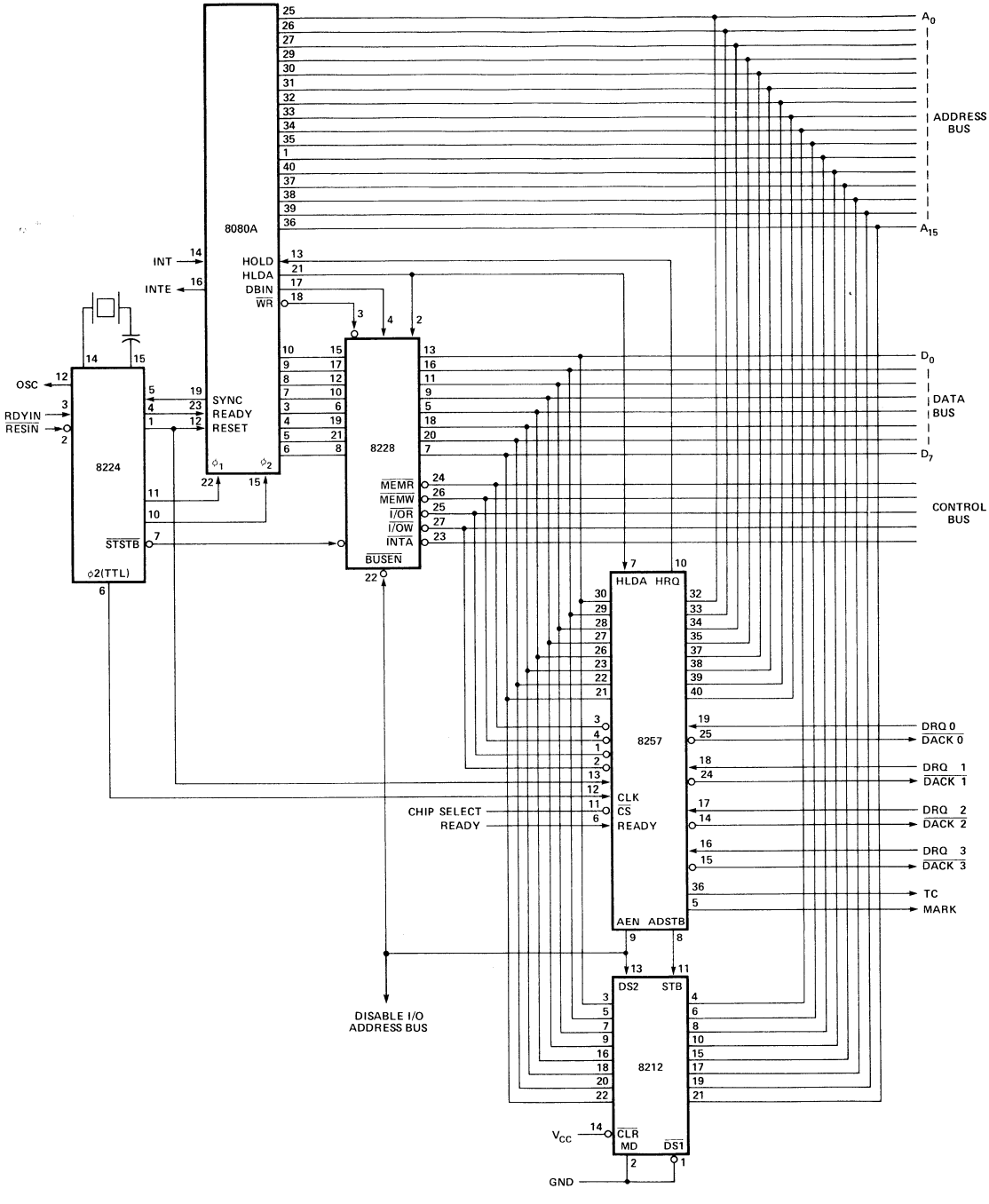
TC REGISTER FOR MEMORY MAPPED I/O ONLY

System Interface

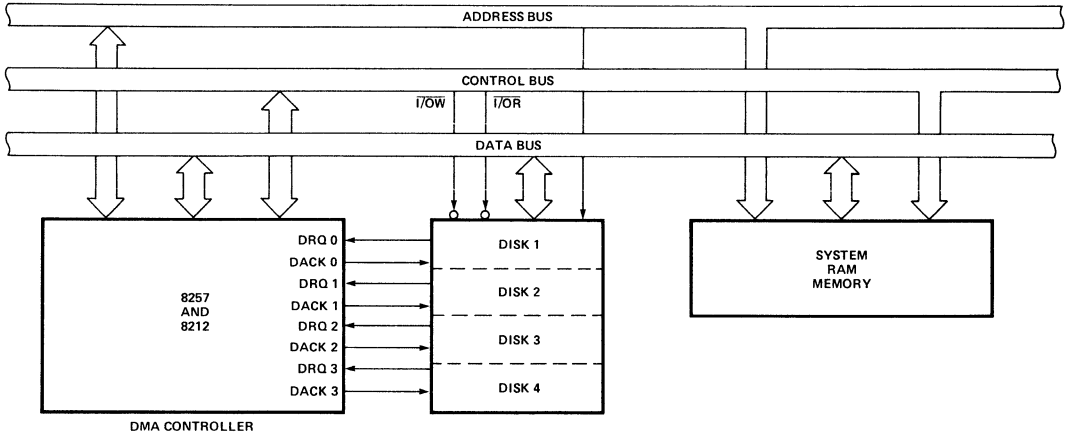
The system interface is similar to the other peripherals of the MCS-80™ but an additional 8212 is necessary to control the entire address bus. A special control signal $\overline{BUSEN}$ is connected directly to the 8228 so that the data bus and control bus will be released at the proper time.



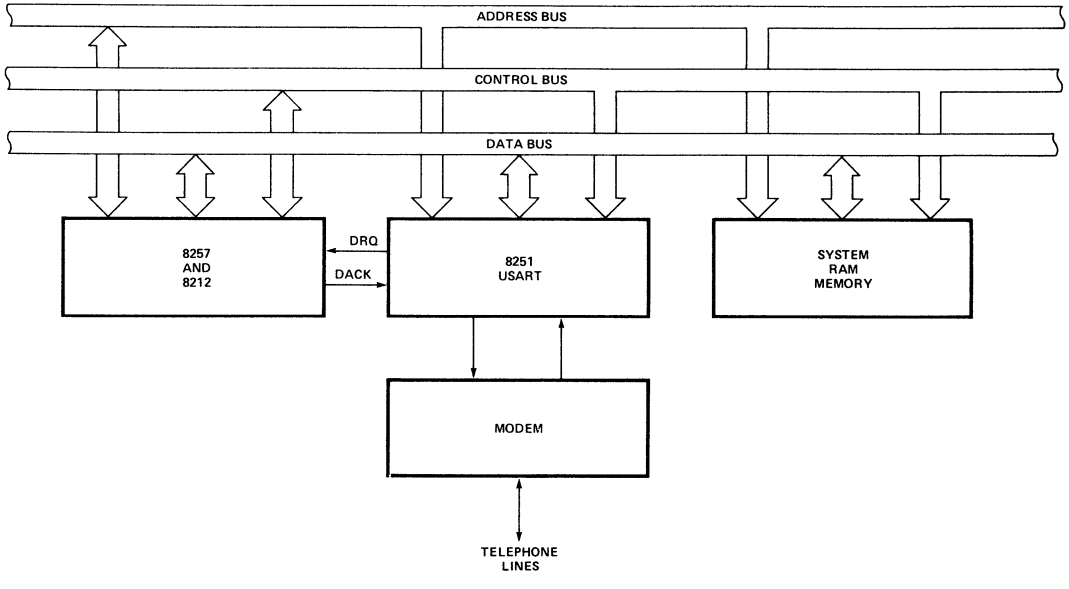
DETAILED SYSTEM INTERFACE SCHEMATIC



SYSTEM APPLICATION EXAMPLES



FLOPPY DISK CONTROLLER (4 DRIVES)



HIGH-SPEED COMMUNICATION CONTROLLER

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	V_{CC}+.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	Volts	I_{OH}=-150μA for AB, DB and AEN I_{OH}=-80μA for others
V_{HH}	HRQ Output High Voltage	3.3	V_{CC}	Volts	I_{OH} = -80μA
I_{CC}	V_{CC} Current Drain		120	mA	
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC}
I_{OFL}	Output Leakage During Float		10	μA	V_{OUT} [1]

Note 1: $V_{CC} > V_{OUT} >$ GND + .45V.

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS: PERIPHERAL (SLAVE) MODE

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%; GND = 0V (Note 1).

8080 BUS PARAMETERS:

READ CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
T_{AR}	Adr or $\overline{CS}\downarrow$ Setup to $\overline{Rd}\downarrow$	50		ns	
T_{RA}	Adr or $\overline{CS}\uparrow$ Hold from $\overline{Rd}\uparrow$	0		ns	
T_{RDE}	Data Access from $\overline{Rd}\downarrow$	0	300	ns	C_L = 100pF
T_{RDF}	DB→Float Delay from $\overline{Rd}\uparrow$		150	ns	C_L = 100pF
		20		ns	C_L = 15pF
T_{RW}	$\overline{Rd}$ Width	300		ns	

WRITE CYCLE:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
T_{CW}	$\overline{CS}\downarrow$ Setup to $\overline{Wr}\downarrow$	300		ns	
T_{WC}	$\overline{CS}\uparrow$ Hold from $\overline{Wr}\uparrow$	20		ns	
T_{AW}	Adr Setup to $\overline{Wr}\downarrow$	20		ns	
T_{WA}	Adr Hold from $\overline{Wr}\uparrow$	20		ns	
T_{DW}	Data Setup to $\overline{Wr}\downarrow$	200		ns	
T_{WD}	Data Hold from $\overline{Wr}\uparrow$	35		ns	
T_{WWS}	$\overline{Wr}$ Width	200		ns	

OTHER TIMING:

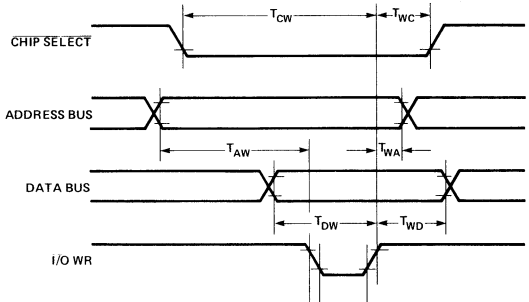
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
T_{RSTW}	Reset Pulse Width	300		ns	
T_{RSTD}	Power Supply↑(V_{CC}) Setup to Reset↓	500		μs	
T_r	Signal Rise Time		20	ns	
T_f	Signal Fall Time		20	ns	
T_{RSTS}	Rese to First $\overline{IOWR}$	2		t_{CY}	

Note 1: All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V
Output "1" at 2.0V, "0" at 0.8V

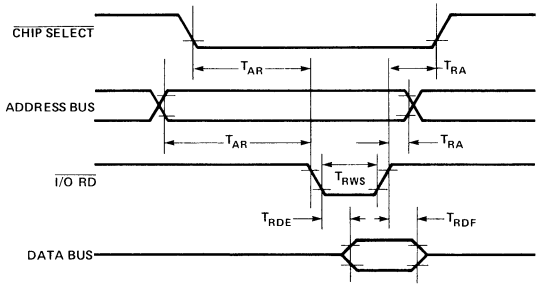
MCS 80/85

8257 PERIPHERAL MODE TIMING DIAGRAM

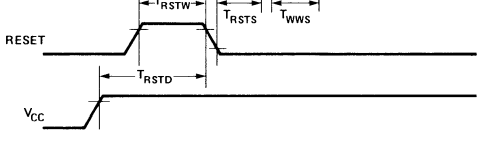
WRITE TIMING:



READ TIMING:



RESET TIMING:

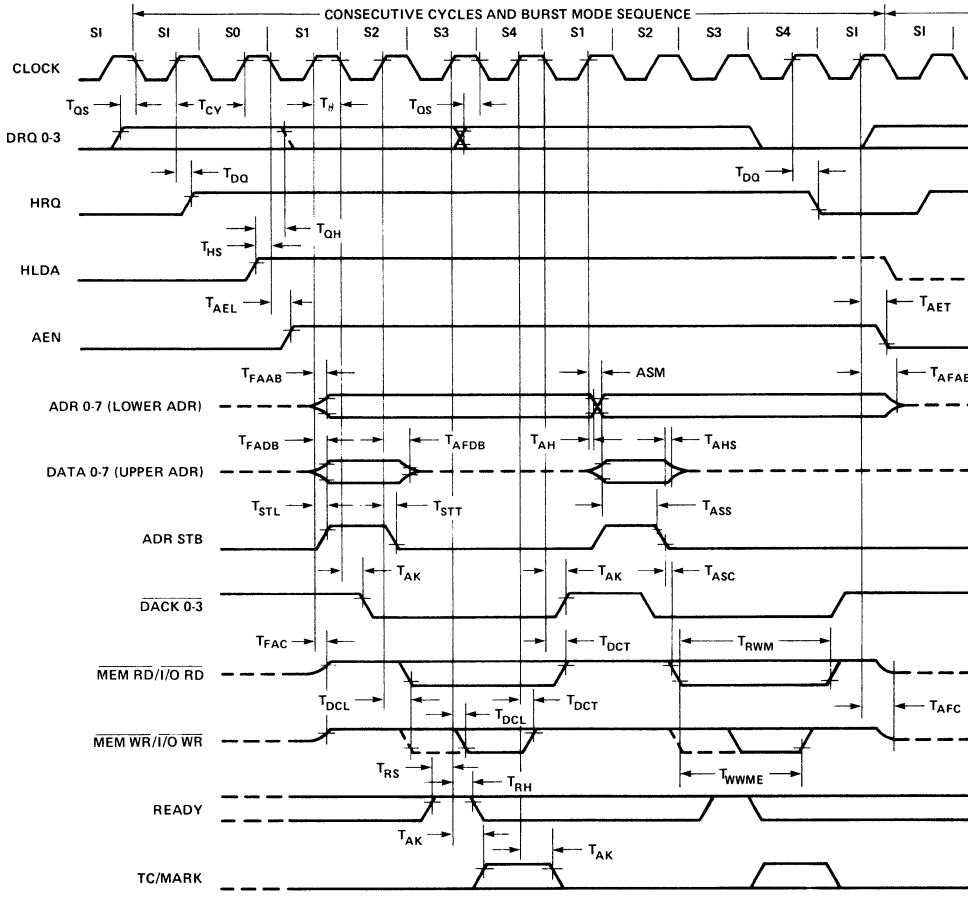


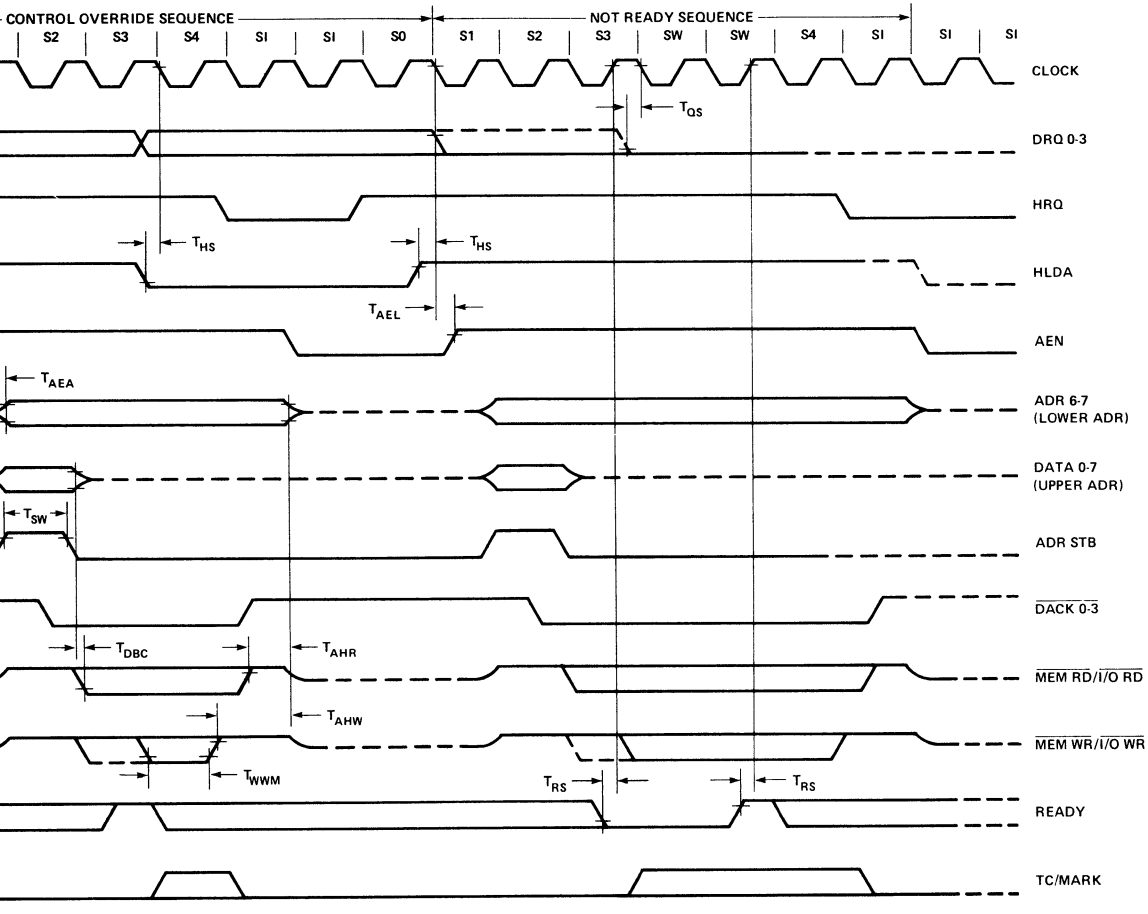
A.C. CHARACTERISTICS: DMA (MASTER) MODE $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
T_{CY}	Cycle Time (Period)	0.330	4	μs	
$T\theta$	Clock Active (High)	150	$.8T_{CY}$	ns	
T_{QS}	DRQ↑ Setup to θ↓(SI,S4)	120			
T_{QH}	DRQ↓ Hold from HLDA↑	0			4
T_{DQ}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 2.0V)		160	ns	1
T_{DQ1}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 3.3V)		250	ns	3
T_{HS}	HLDA↑ or ↓Setup to θ↓(SI,S4)	100		ns	
T_{AEL}	AEN↑ Delay from θ↓(S1)		300	ns	1
T_{AET}	AEN↓ Delay from θ↑(SI)		200	ns	1
T_{AEA}	Adr(AB)(Active) Delay from AEN↑(S1)	20		ns	4
T_{FAAB}	Adr(AB)(Active) Delay from θ↑(S1)		250	ns	2
T_{AFAB}	Adr(AB)(Float) Delay from θ↑(SI)		150	ns	2
T_{ASM}	Adr(AB)(Stable) Delay from θ↑(S1)		250	ns	2
T_{AH}	Adr(AB)(Stable) Hold from θ↑(S1)	T_{ASM}-50			2
T_{AHR}	Adr(AB)(Valid) Hold from $\overline{Rd}$↑(S1,SI)	60		ns	4
T_{AHW}	Adr(AB)(Valid) Hold from $\overline{Wr}$↑(S1,SI)	300		ns	4
T_{FADB}	Adr(DB)(Active) Delay from θ↑(S1)		300	ns	2
T_{AFDB}	Adr(DB)(Float) Delay from θ↑(S2)	T_{STT}+20	250	ns	2
T_{ASS}	Adr(DB) Setup to AdrStb↓(S1-S2)	100		ns	4
T_{AHS}	Adr(DB)(Valid) Hold from AdrStb↓(S2)	50		ns	4
T_{STL}	AdrStb↑ Delay from θ↑(S1)		200	ns	1
T_{STT}	AdrStb↓ Delay from θ↑(S2)		140	ns	1
T_{SW}	AdrStb Width (S1-S2)	T_{CY}-100		ns	4
T_{ASC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from AdrStb↓(S2)	70		ns	4
T_{DBC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from Adr(DB) (Float)(S2)	20		ns	4
T_{AK}	DACK↑ or ↓Delay from θ↓(S2,S1) and TC/Mark↑ Delay from θ↑(S3) and TC/Mark↓ Delay from θ↑(S4)		250	ns	1,5
T_{DCL}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from θ↑(S2) and $\overline{Wr}$↓ Delay from θ↑(S3)		200	ns	2,6
T_{DCT}	$\overline{Rd}$↑ Delay from θ↓(S1,SI) and $\overline{Wr}$↑ Delay from θ↑(S4)		200	ns	2,7
T_{FAC}	$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑(S1)		300	ns	2
T_{AFC}	$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑(SI)		150	ns	2
T_{RWM}	$\overline{Rd}$ Width (S2-S1 or SI)	$2T_{CY} + T_\theta$-50		ns	4
T_{WWM}	$\overline{Wr}$ Width (S3-S4)	T_{CY}-50		ns	4
T_{WWME}	$\overline{Wr}$(Ext) Width (S2-S4)	$2T_{CY}$-50		ns	4
T_{RS}	READY Set Up Time to θ↑ (S3, Sw)	30		ns	
T_{RH}	READY Hold Time from θ↑ (S3, Sw)	20		ns	

Notes: 1. Load = 1 TTL. 2. Load = 1 TTL + 50pF. 3. Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V. 4. Tracking Specification. 5. $\Delta T_{AK} < 50$ ns. 6. $\Delta T_{DCL} < 50$ ns. 7. $\Delta T_{DCT} < 50$ ns.

DMA MODE WAVEFORMS





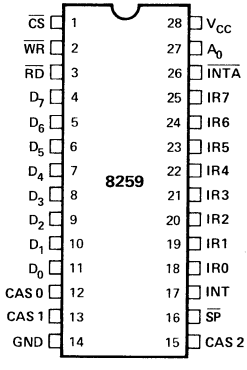
8259
PROGRAMMABLE INTERRUPT CONTROLLER

- **Eight Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes (Algorithms)**
- **Individual Request Mask Capability**
- **Single +5V Supply (No Clocks)**
- **28 Pin Dual-In-Line Package**
- **Fully Compatible with Intel CPUs**

The 8259 handles up to eight vectored priority interrupts for microprocessors. It is cascadable for up to 64 vectored priority interrupts, without additional circuitry. It will be packaged in a 28-pin plastic DIP, uses nMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259 is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

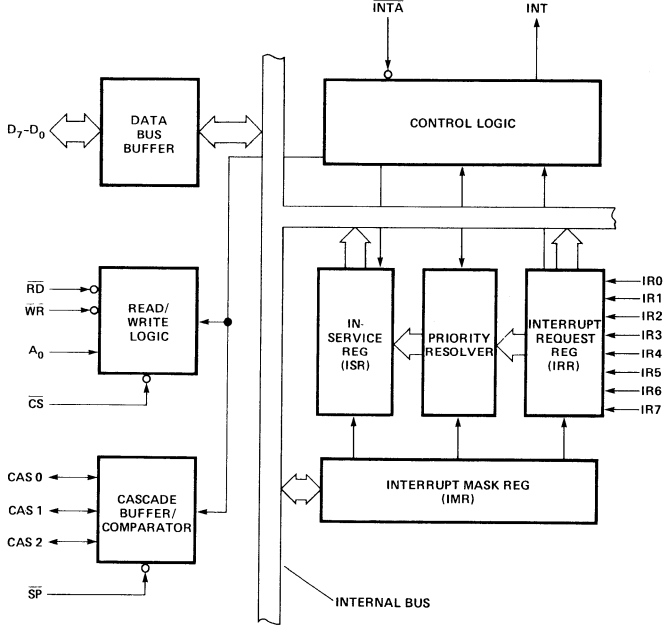
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS1-CAS0	CASCADE LINES
$\overline{SP}$	SLAVE PROGRAM INPUT
INT	INTERRUPT OUTPUT
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE INPUT
IR0-IR7	INTERRUPT REQUEST INPUTS

BLOCK DIAGRAM



INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient method so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

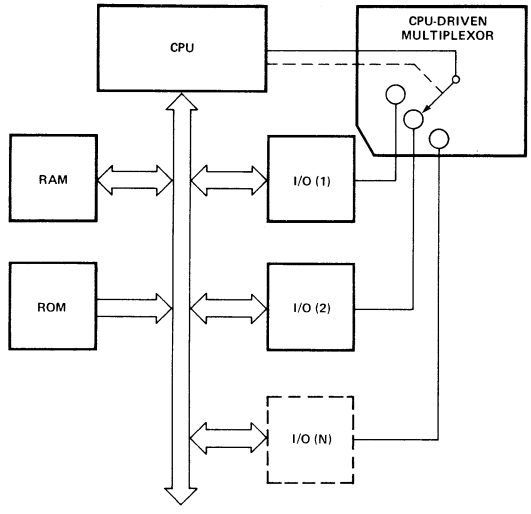
The most common method of servicing such devices is the **Polled** approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuence polling cycle and that such a method would have a serious, detrimental effect on system throughput thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desireable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete however the processor would resume exactly where it left off.

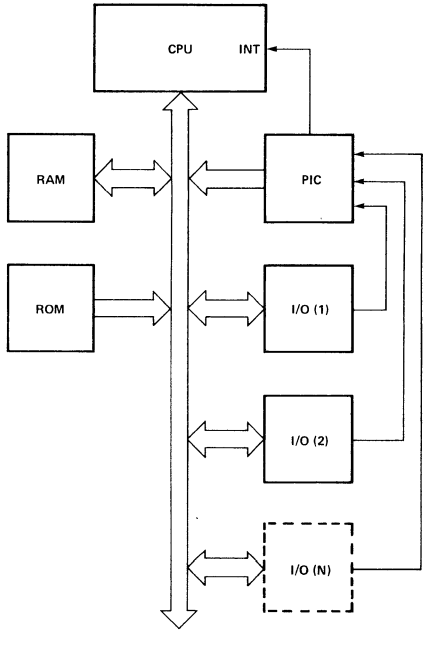
This method is called **Interrupt**. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced and issues an Interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. The PIC does this by providing the CPU with a 3-byte CALL instruction.



POLLED METHOD



INTERRUPT METHOD

8259 BASIC FUNCTIONAL DESCRIPTION

General

The 8259 is a device specifically designed for use in real time, interrupt driven, microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259s (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority algorithms is available to the programmer so that the manner in which the requests are processed by the 8259 can be configured to match his system requirements. The priority assignments and algorithms can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

The IRR bit is set and INT line is raised high whenever there is a positive going edge at the IR input. However, the IR input must be held high until the 1st $\overline{INTA}$ pulse has arrived. More than one bit of the IRR can be set at once as long as they are not masked. The IRR is reset by the $\overline{INTA}$ sequence.

The ISR bit is set by the $\overline{INTA}$ pulse (at the same time the selected IRR bit is reset). This bit remains set during the subroutine until an EOI (End of Interrupt) command is received by the 8259.

The return from the subroutine to the main program may look like this:

```
DI
OUT    OCW2    (Send EOI command)
POP    PSW
EI
RET
```

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

INT (Interrupt)

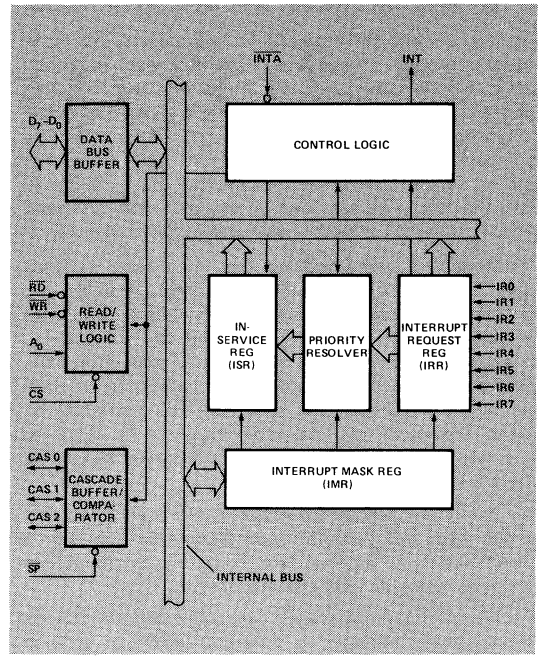
This output goes directly to the 8080 INT input. The V_{OH} level on this line is designed to be fully compatible with the 8080 input level.

$\overline{INTA}$ (Interrupt Acknowledge)

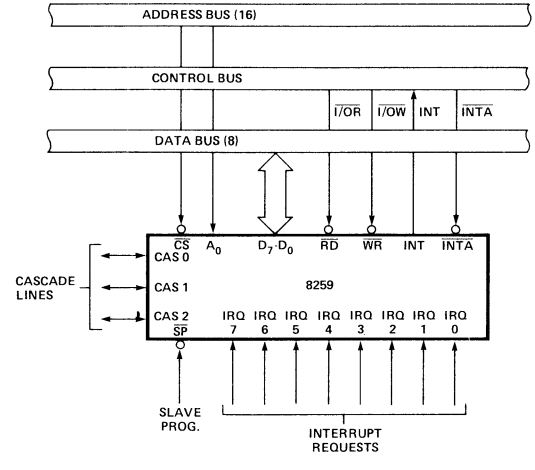
This input generally comes from the 8228 of the CPU group. The 8228 will produce 3 distinct $\overline{INTA}$ pulses. The 3 $\overline{INTA}$ pulses will cause the 8259 to release a 3-byte CALL instruction onto the Data Bus.

Interrupt Mask Register (IMR)

The IMR stores the bits of the interrupt lines to be masked. The IMR operates on both the IRR and the ISR. Masking of a higher priority bit will not affect the interrupt request lines of lower priority.



8259 BLOCK DIAGRAM



8259 INTERFACE TO 8080 STANDARD SYSTEM BUS

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8259 to the 8080 system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic

The function of this block is to accept OUTput commands from the 8080. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259 to be transferred onto the 8080 Data Bus.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8259. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (Write)

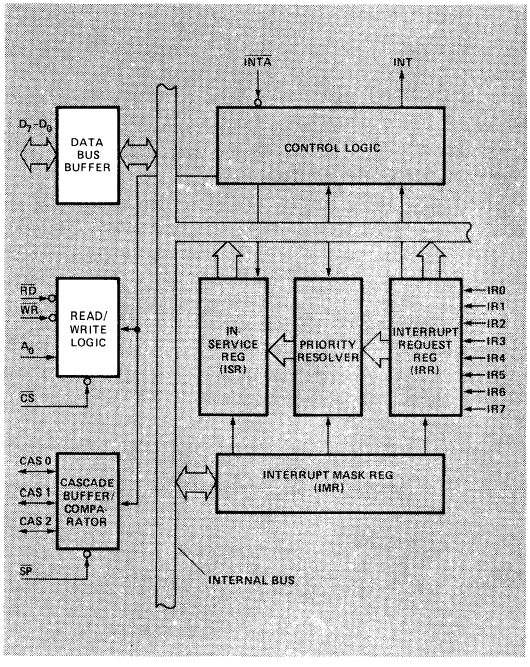
A "low" on this input enables the 8080 CPU to write control words (ICWs and OCWs) to the 8259.

$\overline{RD}$ (Read)

A "low" on this input enables the 8259 to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR) or the BCD of the Interrupt level on to the Data Bus.

A0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers as well as reading the various status registers of the chip. This line can be tied directly to one of the 8080 address lines.



8259 BLOCK DIAGRAM

8259 BASIC OPERATION

A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0			0	1	0	INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or Interrupting Level ⇒ DATA BUS (Note 1)
1			0	1	0	IMR ⇒ DATA BUS
						OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	DATA BUS ⇒ OCW2
0	0	1	1	0	0	DATA BUS ⇒ OCW3
0	1	X	1	0	0	DATA BUS ⇒ ICW1
1	X	X	1	0	0	DATA BUS ⇒ OCW1, ICW2, ICW3 (Note 2)
						DISABLE FUNCTION
X	X	X	1	1	0	DATA BUS ⇒ 3-STATE
X	X	X	X	X	1	DATA BUS ⇒ 3-STATE

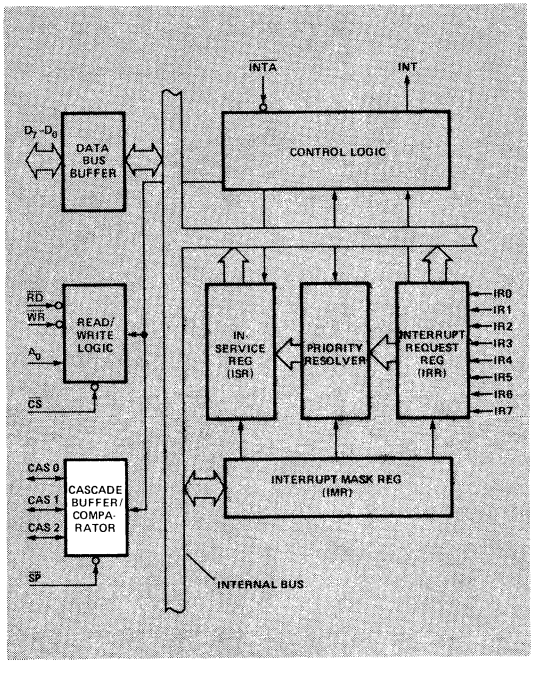
Note 1: Selection of IRR, ISR or Interrupting Level is based on the content of OCW3 written before the READ operation.
Note 2: On-chip sequencer logic queues these commands into proper sequence.

$\overline{SP}$ (Slave Program)

More than one 8259 can be used in the system to expand the priority interrupt scheme up to 64 levels. In such case, one 8259 acts as the master, and the others act as slaves. A "high" on the $\overline{SP}$ pin designates the 8259 as the master, a "low" designates it as a slave.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all 8259 used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259 is used as a master ($\overline{SP}$ = 1), and are inputs when the 8259 is used as a slave ($\overline{SP}$ = 0). As a master, the 8259 sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine addressed onto the Data Bus during next two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 8259".)



8259 BLOCK DIAGRAM

8259 DETAILED OPERATIONAL SUMMARY

General

The powerful features of the 8259 in the 8080 microcomputer system are its programmability and its utilization of the 8080 CALL instruction to jump into any address in the memory map. The normal sequence of events that the 8259 interacts with the CPU is as follows:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high signaling the 8259 that the peripheral equipment(s) are demanding service.
2. The 8259 accepts these requests, resolves the priorities, and sends an INT to the 8080 CPU.
3. The 8080 CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving the $\overline{INTA}$ from the CPU group (8228), the 8259 will release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{INTA}$ pulses to be sent to the 8259 from the CPU group (8228).
6. These two $\overline{INTA}$ pulses allow the 8259 to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 8259. The In-Service Register (ISR) is not reset until the end of the subroutine when an EOI (End of interrupt) command is issued to the 8259.

Programming The 8259

The 8259 accepts two types of command words generated by the CPU:

1. Initialization Command Words (ICWs):
   Before normal operation can begin, each 8259 in the system must be brought to a starting point — by a sequence of 2 or 3 bytes timed by $\overline{WR}$ pulses. This sequence is described in Figure 1.
2. Operation Command Words (OCWs):
   These are the command words which command the 8259 to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

   The OCWs can be written into the 8259 at anytime during operation.

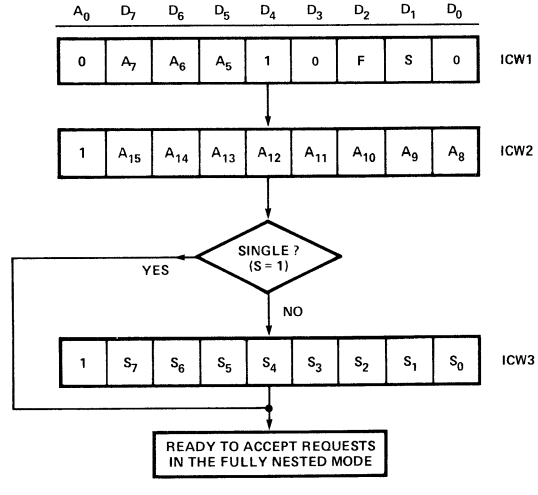


FIGURE 1. INITIALIZATION SEQUENCE

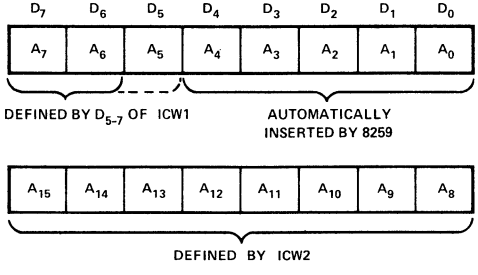
Initialization Command Words 1 and 2: (ICW1 and ICW2)

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1), and initiates the initialization sequence. During this sequence, the following occur automatically:

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low to high transition to generate an interrupt.
b. The interrupt Mask Register is cleared.
c. IR 7 input is assigned priority 7.
d. Special Mask Mode Flip-flop and status Read Flip-flop are reset.

The 8 requesting devices have 8 addresses equally spaced in memory. The addresses can be programmed at intervals of 4 or 8 bytes; the 8 routines thus occupying a page of 32 or 64 bytes respectively in memory.

The address format is:



A0-4 are automatically inserted by the 8259, while A15-6 are programmed by ICW1 and ICW2. When interval = 8, A5 is fixed by the 8259. If interval = 4, A5 is programmed in ICW1. Thus, the interrupt service routines can be located anywhere in the memory space. The 8 byte interval will maintain compatibility with current 8080 RESTART instruction software, while the 4 byte interval is best for compact jump table.

The address format inserted by the 8259 is described in Table 1.

The bits F and S are defined by ICW1 as follows:

F: Call address interval. F = 1, then interval = 4; F = 0, then interval = 8.

S: Single. S = 1 means that this is the only 8259 in the system. It avoids the necesity of programming ICW3.

	INTERVAL = 4								INTERVAL = 8							
	LOWER MEMORY ROUTINE ADDRESS															
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
IR 7	A7	A6	A5	1	1	1	0	0	A7	A6	1	1	1	0	0	0
IR 6	A7	A6	A5	1	1	0	0	0	A7	A6	1	1	0	0	0	0
IR 5	A7	A6	A5	1	0	1	0	0	A7	A6	1	0	1	0	0	0
IR 4	A7	A6	A5	1	0	0	0	0	A7	A6	1	0	0	0	0	0
IR 3	A7	A6	A5	0	1	1	0	0	A7	A6	0	1	1	0	0	0
IR 2	A7	A6	A5	0	1	0	0	0	A7	A6	0	1	0	0	0	0
IR 1	A7	A6	A5	0	0	1	0	0	A7	A6	0	0	1	0	0	0
IR 0	A7	A6	A5	0	0	0	0	0	A7	A6	0	0	0	0	0	0

TABLE 1.

Example of Interrupt Acknowledge Sequence

Assume the 8259 is programmed with F = 1 (CALL address interval = 4), and IR5 is the interrupting level. The 3 byte sequence released by the 8259 timed by the $\overline{INTA}$ pulses is as follows:

	D7	D6	D5	D4	D3	D2	D1	D0	
1st $\overline{INTA}$	1	1	0	0	1	1	0	1	CALL CODE
2nd $\overline{INTA}$	A7	A6	A5	1	0	1	0	0	LOWER ROUTINE ADDRESS
3rd $\overline{INTA}$	A15	A14	A13	A12	A11	A10	A9	A8	HIGHER ROUTINE ADDRESS

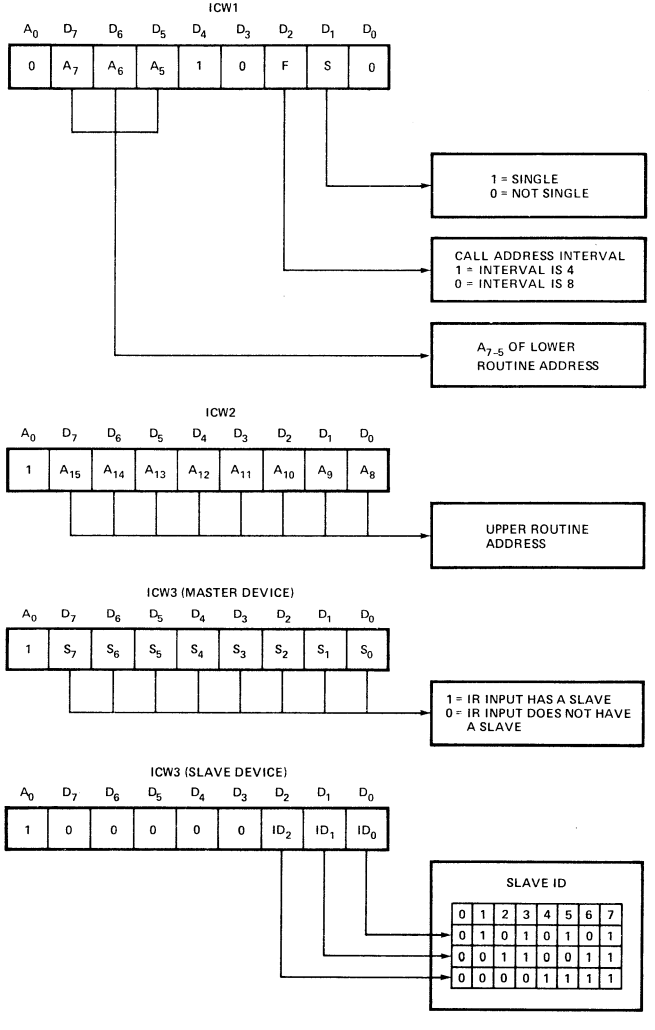
Initialization Command Word 3 (ICW3)

This will load the 8-bit slave register. The functions of this register are as follows:

a. If the 8259 is the master, a "1" is set for each slave in the system. The master then will release byte 1 of the CALL sequence and will enable the corresponding slave to release bytes 2 and 3, through the cascade lines.

b. If the 8259 is a slave, bits 2 - 0 identify the slave. The slave compares its CAS0-2 inputs (sent by the master) with these bits. If they are equal, bytes 2 and 3 of the CALL sequence are released.

If bit S is set in ICW1, there is no need to program ICW3.



INITIALIZATION COMMAND WORD FORMAT

Operation Command Words (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 8259, the chip is ready to accept interrupt requests at its input lines. However, during the 8259 operation, a selection of algorithms can command the 8259 to operate in various modes through the Operation Command Words (OCWs). These various modes and their associated OCWs are described below.

Interrupt Masks

Each Interrupt Request input can be masked individually by the Interrupt Masked Register (IMR) programmed through OCW1.

The IMR will operate on both the Interrupt Request Register and the In-Service Register. Note that if an interrupt is already acknowledged by the 8259 (an $\overline{INTA}$ pulse has occurred), then the Interrupting level, although masked, will inhibit the lower priorities. To enable these lower priority interrupts, one can do one of the two things: (1) Write an End of Interrupt (EOI) command (OCW2) to reset the ISR bit or (2) Set the special mask mode using OCW3 (as will be explained later in the special mask mode.)

Fully Nested Mode

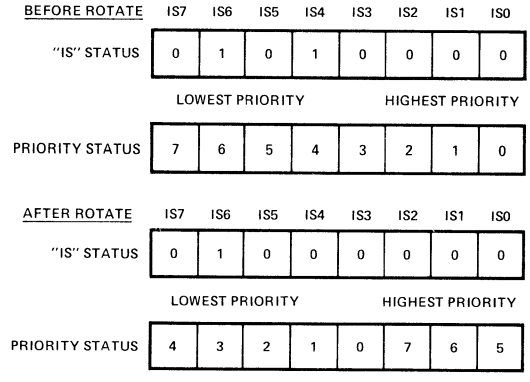
The 8259 will operate in the fully nested mode after the execution of the initialization sequence without any OCW being written. In this mode, the interrupt requests are ordered in priorities from 0 through 7. When an interrupt is acknowledged, the highest priority request is determined and its address vector placed on the bus. In addition, a bit of the Interrupt service register (IS 7-0) is set. This bit remains set until the 8080 issues an End of Interrupt (EOI) command immediately before returning from the service routine. While the IS bit is set, all further interrupts of lower priority are inhibited, while higher levels will be able to generate an interrupt (which will only be acknowledged if the 8080 has enabled its own interrupt input through software).

After the Initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained in the rotating priority mode.

Rotating Priority Modes

The Rotating Priority Modes of the 8259 serves in application of interrupting devices of equal priority such as communication channels. There are two variations of the rotating priority mode: the auto mode and the specific mode.

1. Auto Mode — In this mode, a device after being serviced receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case, until 7 other devices are serviced at most once each. i.e., if the priority and "in service" status is:



   In this example, the In-Service FF corresponding to line 4 (the highest priority FF set) was reset and line 4 became the lowest priority, while all the other priorities rotated correspondingly.

   The Rotate command is issued in OCW2, where: R = 1, EOI = 1, SEOI = 0.

2. Specific Mode — The programmer can change priorities by programming the bottom priority, and by doing this, to fix the highest priority: i.e., if IR5 is programmed as the bottom priority device, the IR6 will have the highest one.

   The Rotate command is issued in OCW2 where: R = 1, SEOI = 1. L2, L1, L0 are the BCD priority level codes of the bottom priority device.

   Observe that this mode is independent of the End of Interrupt Command and priority changes can be executed during EOI command or independently from the EOI command.

End of Interrupt (EOI) and Specific End of Interrupt (SEOI)

An End of Interrupt command word must be issued to the 8259 before returning from a service routine, to reset the appropriate IS bit.

There are two forms of EOI command: Specific and non-Specific. When the 8259 is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a non-Specific EOI command is issued the 8259 will automatically reset the highest IS bit of those that are set, since in the nested mode, the highest IS level was necessarily the last level acknowledged and will necessarily be the next routine level returned from.

However, when a mode is used which may disturb the fully nested structure, such as in the rotating priority case, the 8259 may no longer be able to determine the last level acknowledged. In this case, a specific EOI (SEOI) must be issued which includes the IS level to be reset as part of the command. The End of the Interrupt is issued whenever EOI = "1" in OCW2. For specific EOI, SEOI = "1", and EOI = 1. L2, L1, L0 is then the BCD level to be reset. As explained in the Rotate Mode earlier, this can also be the bottom priority code. Note that although the Rotate command can be issued during an EOI = 1, it is not necessarily tied to it.

OCW1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	M7	M6	M5	M4	M3	M2	M1	M0

INTERRUPT MASK
1 = MASK SET
0 = MASK RESET

OCW2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	R	SEOI	EOI	0	0	L_2	L_1	L_0

BCD LEVEL TO BE RESET OR PUT INTO LOWEST PRIORITY

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

NON-SPECIFIC END OF INTERRUPT
1 = RESET THE HIGHEST PRIORITY BIT OF ISR
0 = NO ACTION

SPECIFIC END OF INTERRUPT
1 = L_2, L_1, L_0 BITS ARE USED
0 = NO ACTION

ROTATE PRIORITY
1 = ROTATE
0 = NOT ROTATE

OCW3

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	—	ESMM	SMM	0	1	P	ERIS	RIS

DON'T CARE

READ IN-SERVICE REGISTER

0	1	0	1
0	0	1	1
NO ACTION		READ IR REG ON NEXT $\overline{RD}$ PULSE	READ IS REG ON NEXT $\overline{RD}$ PULSE

POLLING
A HIGH ENABLES THE NEXT $\overline{RD}$ PULSE TO READ THE BCD CODE OF THE HIGHEST LEVEL REQUESTING INTERRUPT.

SPECIAL MASK MODE

0	1	0	1
0	0	1	1
NO ACTION		RESET SPECIAL MASK	SET SPECIAL MASK

OPERATION COMMAND WORD FORMAT

Special Mask Mode (SMM)

This mode is useful when some bit(s) are set (masked) by the Interrupt Mask Register (IMR) through OCW1. If, for some reason, we are currently in a subroutine which is masked (this could happen when the subroutine intentionally masks itself off). It is still possible to enable the lower priority lines by setting the Special Mask mode. In this mode the lower priority lines are enabled until the SMM is reset. The higher priorities are not affected.

The special mask mode FF is set by OCW3 where ESMM = 1, SMM = 1, and reset where: ESSM = 1 and SMM = 0.

Polled Mode

In this mode, the 8080 disables its interrupt input. Service to devices is achieved by programmer initiative by a Poll command.

The poll command is issued by setting P = "1" in OCW3 during a $\overline{WR}$ pulse.

The 8259 treats the next $\overline{RD}$ pulse as an interrupt acknowledge, sets the appropriate IS Flip-flop, if there is a request, and reads the priority level.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	–	–	–	–	W2	W1	W0

W0 — 2: BCD code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels — so that the $\overline{INTA}$ sequence is not needed (and this saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

	A0	D4	D3		
OCW1	1			M7-M0	IMR (Interrupt Mask Register). $\overline{WR}$ will load it while status can be read with $\overline{RD}$.
OCW2	0	0	0	R SEOI EOI	
				0 0 0	No Action.
				0 0 1	Non-specific End of Interrupt.
				0 1 0	No Action.
				0 1 1	Specific End of Interrupt. L2, L1, L0 is the BCD level to be reset.
				1 0 0	No Action.
				1 0 1	Rotate priority at EOI. (Auto Mode)
				1 1 0	Rotate priority, L2, L1, L0 becomes bottom priority without Ending of Interrupt.
				1 1 1	Rotate priority at EOI (Specific Mode), L2, L1, L0 becomes bottom priority, and its corresponding IS FF is reset.
OCW3	0	1	0	ESMM SMM	
				0 0	Special Mask not Affected.
				0 1	
				1 0	Reset Special Mask.
				1 1	Set Special Mask.
				ERIS RIS	
				0 0	No Action.
				0 1	
				1 0	Read IR Register Status.
				1 1	Read IS Register Status.

Note: The 8080 INT input must be disabled during:

1. Initialization sequence for all the 8259 in the system.
2. Any control command execution.

Reading 8259 Status

The input status of several internal registers can be read to update the user information on the system. The following registers can be read by issuing a suitable OCW and reading with $\overline{RD}$ for the data bus lines:

Interrupt Requests Register (IRR): 8-bit register which contains the priority levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged.

In Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when prior to the $\overline{RD}$ pulse, an $\overline{WR}$ pulse is issued with OCW3, and ERIS = 1, RIS = 0.

The ISR can be read in a similar mode, when ERIS = 1, RIS = 1.

There is no need to write an OCW3 before every status read operation as long as the status read corresponds with the previous one, i.e. the 8259 "remembers" whether the IRR or ISR has been previously selected by the OCW3. On the other hand, for polling operation, an OCW3 must be written before every read.

For reading the IMR, a $\overline{WR}$ pulse is not necessary to preceed the $\overline{RD}$. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0 = 1.

The IMR can be loaded through the data bus when $\overline{WR}$ is active and A0 = 1.

Polling overrides status read when P = 1, ERIS = 1 in OCW3.

Cascading

The 8259 can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

A typical system is shown in Figure 2. The master controls, through the 3 line cascade bus, which one of the slaves will release the corresponding address.

As shown in Figure 2, the slaves interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will release the 8080 CALL code during byte 1 of $\overline{INTA}$ and will enable the corresponding slave to release the device routine address during bytes 2 and 3 of $\overline{INTA}$.

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first $\overline{INTA}$ pulse to the trailing edge of the third pulse. It is obvious that each 8259 in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select ($\overline{CS}$) input of each 8259. The slave program pin ($\overline{SP}$) must be at a "low" level for a slave (and then the cascade lines are inputs) and at a "high" level for a master (and then the cascade lines are outpus).

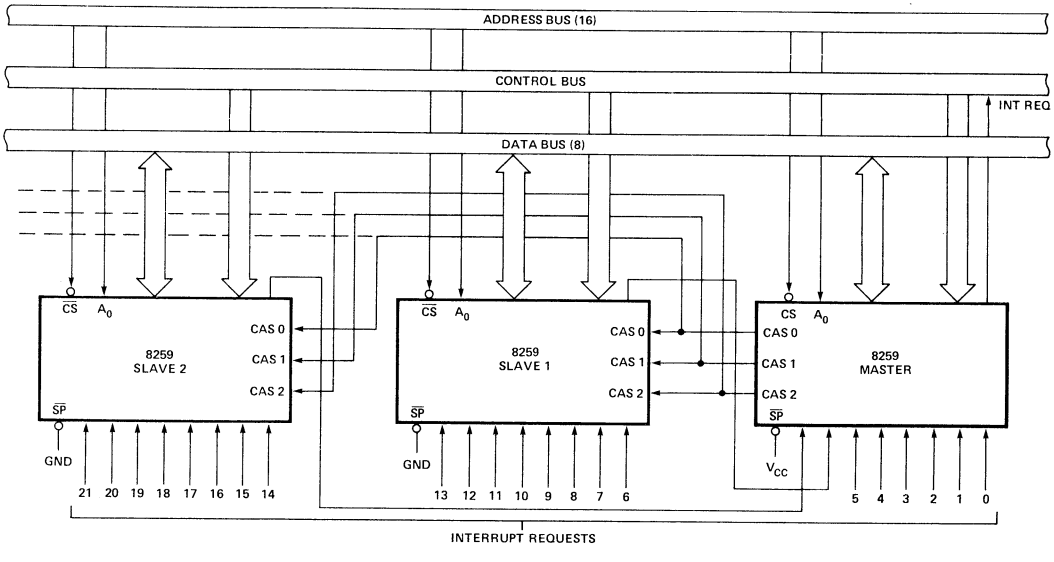


FIGURE 2. CASCADING THE 8259

8259 INSTRUCTION SET

INST. NO.	MNEMONIC	A0	D7	D6	D5	D4	D3	D2	D1	D0	OPERATION DESCRIPTION
1	ICW1 A	0	A7	A6	A5	1	0	1	1	0	Byte 1 initialization, format = 4, single.
2	ICW1 B	0	A7	A6	A5	1	0	1	0	0	Byte 1 initialization, format = 4, not single.
3	ICW1 C	0	A7	A6	A5	1	0	0	1	0	Byte 1 initialization, format = 8, single.
4	ICW1 D	0	A7	A6	A5	1	0	0	0	0	Byte 1 initialization, format = 8, not single.
5	ICW2	1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization (Address No. 2)
6	ICW3 M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization – master.
7	ICW3 S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization – slave.
8	OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask reg, read mask reg.
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non specific EOI.
10	OCW2 SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI. L2, L1, L0 code of IS FF to be reset.
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI (Auto Mode).
12	OCW2 RSE	0	1	1	1	0	0	L2	L1	L0	Rotate at EOI (Specific Mode). L2, L1, L0, code of line to be reset and selected as bottom priority.
13	OCW2 RS	0	1	1	0	0	0	L2	L1	L0	L2, L1, L0 code of bottom priority line.
14	OCW3 P	0	–	0	0	0	1	1	0	0	Poll mode.
15	OCW3 RIS	0	–	0	0	0	1	0	1	1	Read IS register.
16	OCW3 RR	0	–	0	0	0	1	0	1	0	Read requests register.
17	OCW3 SM	0	–	1	1	0	1	0	0	0	Set special mask mode.
18	OCW3 RSM	0	–	1	0	0	1	0	0	0	Reset special mask mode.

Notes:
1. In the master mode $\overline{SP}$ pin = 1, in slave mode $\overline{SP}$ = 0.
2. (–) = do not care.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5 V to +7 V
Power Dissipation ..... 1 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-.5	.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+.5V	V	
V_{OL}	Output Low Voltage		.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA
V_{OH-INT}	Interrupt Output High Voltage	2.4 3.5		V V	I_{OH} = -400 μA I_{OH} = -50 μA
$I_{IL(IR_{0-7})}$	Input Leakage Current for IR_{0-7}		-300 10	μA μA	V_{IN} = 0V V_{IN} = V_{CC}
I_{IL}	Input Leakage Current for Other Inputs		10	μA	V_{IN} = V_{CC} to 0V
I_{LOL}	Output Leakage Current		-10	μA	V_{OUT} = 0.45V
I_{LOH}	Output Leakage Current		10	μA	V_{OUT} = V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = +5V ±5%, GND = 0V)

BUS PARAMETERS

READ

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	$\overline{CS}/A_0$ Stable before $\overline{RD}$ or $\overline{INTA}$	50		ns	
t_{RA}	$\overline{CS}/A_0$ Stable after $\overline{RD}$ or $\overline{INTA}$	50		ns	
t_{RR}	$\overline{RD}$ Pulse Width	420		ns	
t_{RD}	Data Valid from $\overline{RD}/\overline{INTA}$		300	ns	CL = 100 pF
t_{DF}	Data Float after $\overline{RD}/\overline{INTA}$		200	ns	CL = 100 pF
		20			CL = 20 pF

WRITE

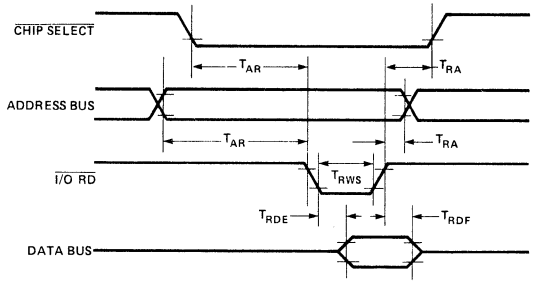
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AW}	A_0 Stable before $\overline{WR}$	50		ns	
t_{WA}	A_0 Stable after $\overline{WR}$	20		ns	
t_{CW}	$\overline{CS}$ Stable before $\overline{WR}$	50		ns	
t_{WC}	$\overline{CS}$ Stable after $\overline{WR}$	20		ns	
t_{WW}	$\overline{WR}$ Pulse Width	400		ns	
t_{DW}	Data Valid to $\overline{WR}$ (T.E.)	300		ns	
t_{WD}	Data Valid after $\overline{WR}$	-40		ns	

OTHER TIMINGS

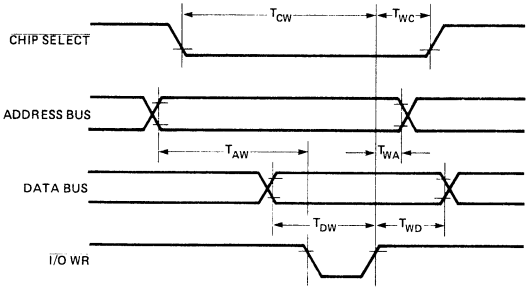
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{IW}	Width of Interrupt Request Pulse	100		ns	
t_{INT}	INT ↑ after IR ↑	250		ns	
t_{IC}	Cascade Line Stable after $\overline{INTA}$ ↑	300		ns	

WAVEFORMS

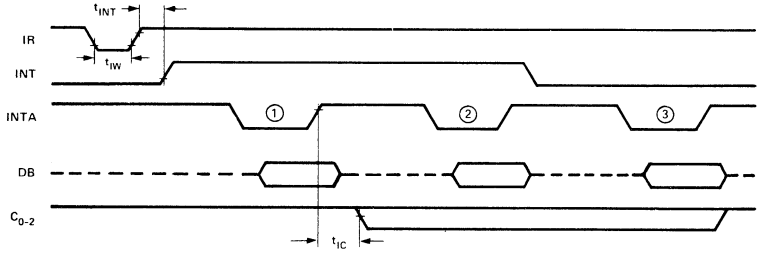
READ TIMING



WRITE TIMING

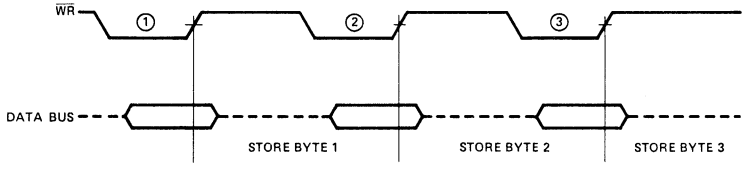


OTHER TIMING

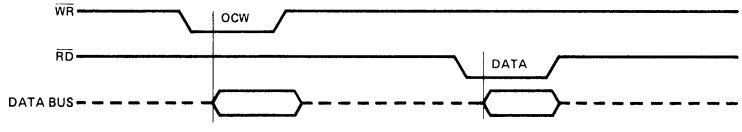


Note: Interrupt acknowledge $\overline{\text{INTA}}$ sequence must remain "HIGH" (at least) until leading edge of first $\overline{\text{INTA}}$.

INITIALIZATION SEQUENCE



READ STATUS/POLL MODE

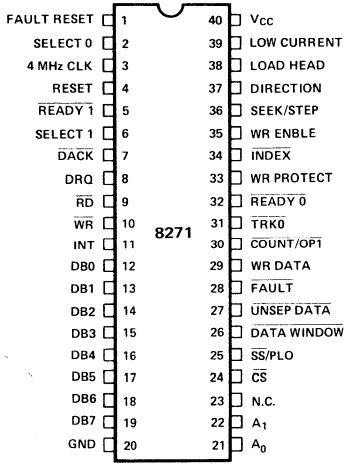


8271
PROGRAMMABLE FLOPPY DISK CONTROLLER

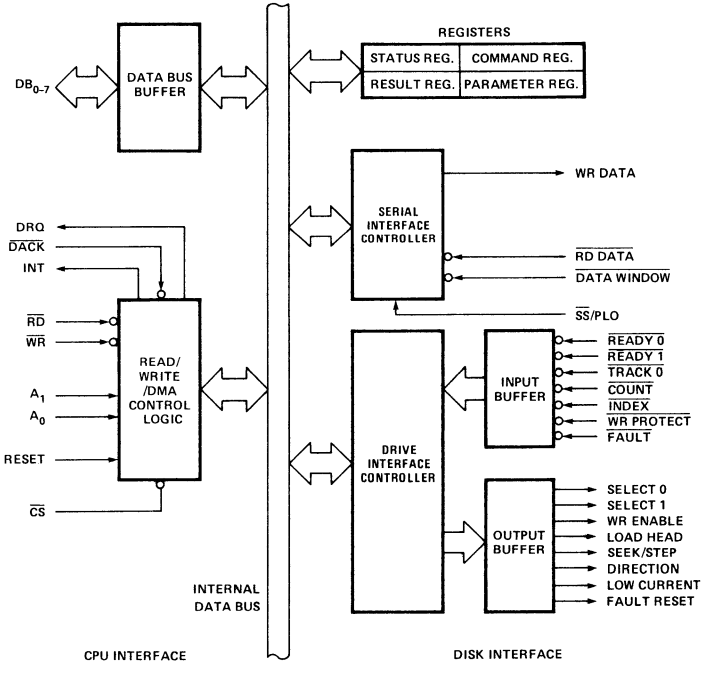
- **IBM 3740 Soft Sectored Format Compatible**
- **Programmable Record Lengths**
- **Multi-Sector Capability**
- **Maintain Dual Drives with Minimum Software Overhead Expandable to 4 Drives**
- **Automatic Read/Write Head Positioning and Verification**
- **Internal CRC Generation and Checking**
- **Programmable Step Rate, Settle-Time, Head Load Time, Head Unload Index Count**
- **Fully Compatible with 8080 CPU**
- **Single +5Volt Supply**
- **40 Pin Package**

The 8271 Floppy Disk Controller (FDC) is a single chip device designed to interface from one to four floppy disk drive to the 8080 microcomputer system. Its powerful control functions minimize both hardware and software overhead normally associated with floppy disk interface.

PIN CONFIGURATION



BLOCK DIAGRAM



General

The 8271 Floppy Disk Controller (FDC) LSI component is designed to interface from one to four floppy disk drives to an eight bit microcomputer.

The FDC supports a soft sectored format that is IBM 3740 compatible. This component is a high level controller that relieves the CPU (and user) of many of the control tasks associated with implementing a floppy disk interface. The FDC supports a variety of high level instructions which allow the user to store and retrieve data on a floppy disk without dealing with the low level details of the disk operation.

In addition to the standard read/write commands a scan command is supported. The scan command allows the user program to specify a data pattern and instruct the FDC to search for that pattern on a track. Any application that is required to search the disk (such as point of sale price lookup, disk directory search, etc.) for information may use the scan command to reduce the CPU overhead. Once the scan operation is initiated, no CPU intervention is required.

Hardware Description

The 8271 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name	I/O	Description
V_{CC}	PWR	+5V supply
GND	PWR	Ground
4MHz Clock	I	A 4MHz ±1% square wave clock
Reset	I	A high signal on the reset input will force the 8271 to an idle state. The 8271 will remain idle until a command is issued by the CPU. The drive interface output signals are forced low.
$\overline{CS}$	I	The I/O Read and I/O Write inputs are enabled by the chip select signal.
DB_7-DB_0	I/O	The Data Bus lines are bidirectional three-state lines (8080 data bus compatible).
$\overline{WR}$	I	The Write signal is used to signal the control logic that a transfer of data from the data bus to the 8271 is required.
$\overline{RD}$	I	The Read signal is used to signal the control logic that a transfer of data from the 8271 to the data bus is required.
INT	O	The interrupt signal indicates that the 8271 requires service.
A_1–A_0	I	These two lines are used to select the destination of source of data to be accessed by the control logic.
DRQ	O	The DMA request signal is used to request a transfer of data between the 8271 and memory.
$\overline{DACK}$	I	The DMA ACK signal notifies the 8271 that a DMA cycle has been granted.
Select 1– Select 0	O	These lines are used to specify the selected drive.
Fault Reset	O	The fault reset line is used to reset an error condition which is latched by the drive.
Write Enable	O	This signal enables the drive write logic.
Seek/Step	O	This multi-function line is used during drive seeks.
Direction	O	The direction line specifies the seek direction.
Load Head	O	The load head line causes the drive to load the Read/Write head load pad against the diskette.
Low Current	O	This line notifies the drive that track 43 or greater is selected.
$\overline{\text{Ready 1}}$, $\overline{\text{Ready 0}}$	I	These two lines indicate that the specified drive is ready.
$\overline{Fault}$	I	This line is used by the drive to specify a file unsafe condition.
$\overline{\text{Count/OP1}}$	I	If the seek / direction / count seek mode is selected, the count pin is pulsed for each track. Otherwise this pin is user specified optional input.
$\overline{\text{Write Protect}}$	I	This signal is used to specify if the drive/diskette may be written.
$\overline{TRK0}$	I	This signal indicates when the R/W head is positioned over track zero.
$\overline{Index}$	I	The index signal gives an indication of the relative position of the diskette.
$\overline{SS/PLO}$	I	This pin is used to specify the type of data separator used.
Write Data	O	Composite write data.
$\overline{\text{Unseparated}}$ $\overline{\text{Data}}$	I	This input is the unseparated data and clocks.
$\overline{\text{Data Window}}$	I	This is a data window established by the single-shot or phase-locked oscillator data separator.

Principles of Operation

The 8271 is fully compatible with the 8080 system Bus. As an 8080 peripheral device, it accepts commands from the CPU, executes these Commands and provides a Result back to the 8080 CPU at the end of execution.

Communication with the CPU are through the activating of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ pins. The A_1,A_0 select the appropriate registers on chip:

A1	A0	CS RD	CS WR
0	0	Status Reg	Command Reg
0	1	Result Reg	Parameter Reg

The FDC chip operation is composed of the following general sequence of events:

The Command Phase

During the Command Phase, the CPU issues a command byte to the 8271. The command byte provides a general description of the type of operation requested. Many operations require more detailed information about the comand. In such case, from zero to five parameters are written following the command byte to provide such information. The various commands that the 8271 can recognize are listed in the Software Operation Section.

The Execution Phase

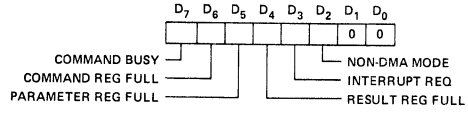
Soon as the last parameter is written into the 8271, the FDC enters the Execution Phase. During this phase there is no need for CPU involvement. The FDC may optionally interface with the 8257 (DMA controller) for high speed data transfers (See System Diagram).

The Result Phase

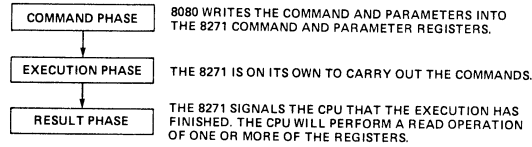
During the Result Phase, the FDC chip notified the CPU of the outcome of the command execution. This phase may be initiated by:

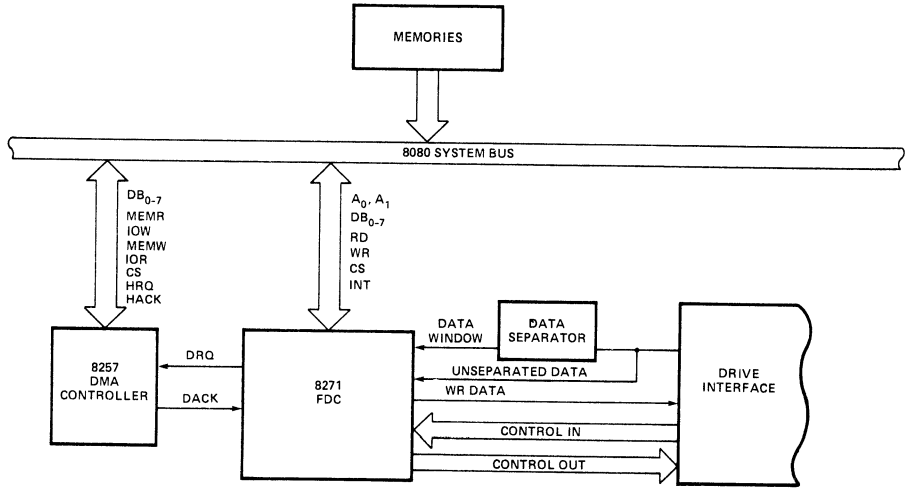
1. The successful completion of an operation.
2. An error detected during an operation.
3. An illegal command or parameter detected during the Command Phase.

In the Result Phase, the CPU Reads the Status Register which provides the following information:



After reading the Status Register, the CPU then Reads the Result Register for more information.





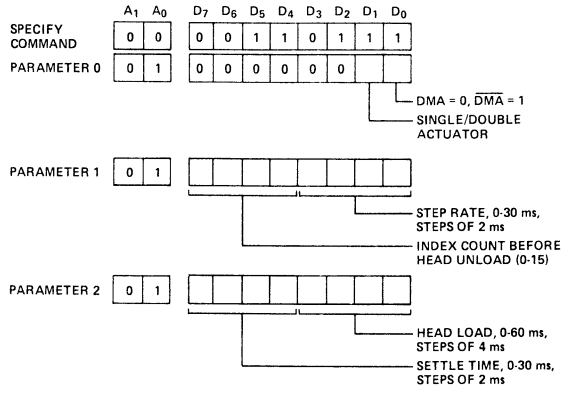
8271 SYSTEM DIAGRAM

Software Operation

The 8271 can accept many powerful commands from the CPU. The following is a list of Basic Commands (associated Parameters not shown).

- SCAN DATA
- SCAN DATA AND DELETED DATA
- WRITE DATA
- WRITE DATA AND DELETED DATA
- READ DATA
- READ DATA AND DELETED DATA
- READ ID
- VERIFY DATA AND DELETED DATA
- FORMAT
- RECALIBRATE
- SEEK
- READ DRIVE STATUS
- LOAD BAD TRACKS
- SPECIFY
- RESET

As an example, the SPECIFY command is associated with 3 parameters:



EXECUTION PHASE BASIC CHARACTERISTICS

The following table summarizes the various commands with corresponding execution phase characteristics.

COMMANDS	1 Deleted Data	2 Head	3 Ready	4 Write/ Protect	5 Seek	6 Seek Check	7 Result	8 Completion Interrupt
SCAN DATA	SKIP	LOAD	√	x	YES	YES	YES	YES
SCAN DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
WRITE DATA	x	LOAD	√	√	YES	YES	YES	YES
WRITE DEL DATA	x	LOAD	√	√	YES	YES	YES	YES
READ DATA	SKIP	LOAD	√	x	YES	YES	YES	YES
READ DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
READ ID	x	LOAD	√	x	YES	NO	YES	YES
VERIFY DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
FORMAT	x	LOAD	√	√	YES	NO	YES	YES
RECALIBRATE	x	–	x	x	YES	NO	YES	YES
SEEK	x	–	x	x	YES	NO	YES	YES
READ DRIVE STAT	x	–	x	x	NO	NO	YES	NO
LOAD BAD TRACKS	x	–	x	x	NO	NO	YES	NO
SPECIFY	x	–	x	x	NO	NO	NO	NO
RESET	x	UNLOAD	x	x	NO	NO	NO	NO

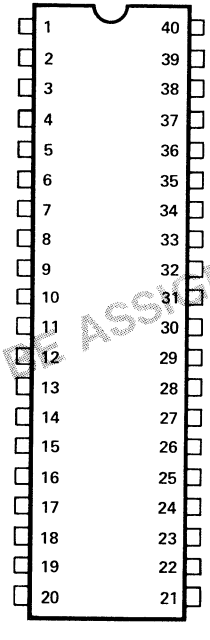
Note: 1. "x" → DON'T CARE
2. "√" → check
3. "–" → No change

8273
SDLC PROTOCOL CONTROLLER

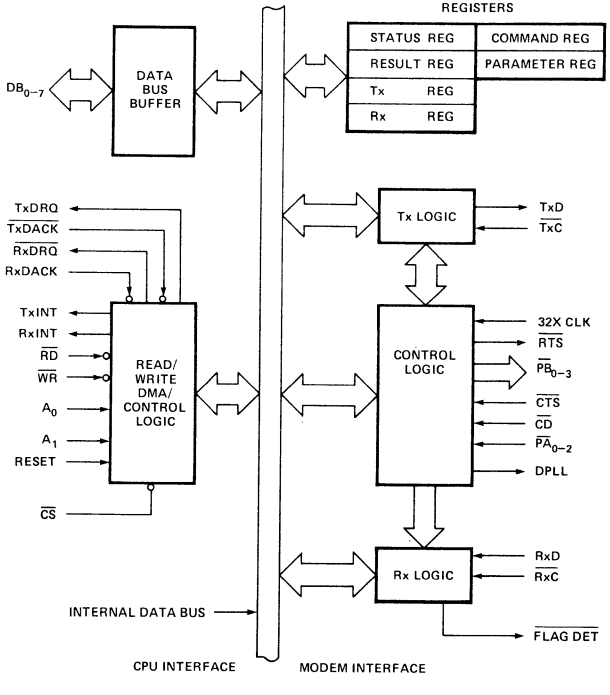
- IBM (SDLC) Compatible
- Full Duplex Operation—56K BAUD
- SDLC Loop Operation
- User Programmable Modem Control Ports
- Programmable NRZI Encode/Decode
- N-Bit Reception Capability
- Digital Phase Locked Loop—Clock Recovery
- Minimum CPU Overhead
- Fully Compatible With 8080 CPU
- Single +5Volt Supply
- 40 Pin Package

The 8273 SDLC (Synchronous Data Link Control) Protocol controller is a single chip device designed to support the SDLC protocol within the 8080 microcomputer system environment. Its internal supervisory instruction set is oriented to frame level (SDLC) functions with a minimum of CPU overhead.

PIN CONFIGURATION



BLOCK DIAGRAM



General

The IBM Synchronous Data Link Control (SDLC) communication protocol is a bit oriented communication protocol vs the BI-SYNC protocol which is character or code oriented. The SDLC protocol greatly reduces the overall CPU software on one hand and increases the throughput on the other because of its ability to go full-duplexed mode.

The 8273 SDLC chip is designed to handle the IBM SDLC protocol with minimum CPU software. The 8273 handles the zero-insertion technique used in SDLC protocol, as well as performing NRZI encoding and decoding for the data. Modem handshake signals are provided so that the CPU intervention is minimized. The FCS (Frame check sequence) is also generated and checked by the SDLC chip as well as Flags (01111110) and Idle characters.

One implementation of SDLC is the Loop-configuration typified by IBM 3650 Retail Store System which can also be handled by the 8273 by going into 1-bit delay mode. In such configuration a two wire pair can be effectively used for data transfer between controllers and loop stations. Digital phase Locked Loop pin-out can be used by the loop station without the presence of an accurate 1X clock.

Hardware Description

The 8273 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name	I/O	Description
GND	PWR	+5V supply
CLK	PWR	Ground
RESET	I	A high signal on this pin will force the 8273 to an idle state. The 8273 will remain idle until a command is issued by the CPU. The modem interface output signals are forced high.
$\overline{CS}$	I	The I/O Read and I/O Write inputs are enabled by the chip.
DB_7-DB_0	I/O	The Data Bus lines are bidirectional three-state line which interface with the 8080 system Data Bus.
$\overline{WR}$	I	The Write signal is used to control the transfer of either a command or data from CPU to the 8273.
$\overline{RD}$	I	The Read signal is used to control the transfer of either a data byte or a status word from the 8273 to the CPU.
TxINT	O	The Transmitter interrupt signal indicates that the transmitter logic requires service.
RxINT	O	The Receiver interrupt signal indicates that the Receiver logic requires service.
TxDRQ	O	The Transmitter DMA Request signal indicates the transmitter Buffer is empty and is ready to transmit another data byte.
RxRDQ	O	The Receiver DMA Request signal indicates the Receiver Buffer is full.
$\overline{TxDACK}$	I	The Transmitter DMA acknowledge signal notifies the 8273 that the TxDMA cycle has been granted.
$\overline{RxDACK}$	I	The Receiver DMA acknowledge signal notifies the 8273 that the RxDMA cycle has been granted.
A_1-A_0	I	These two lines are used to select the destination or source of data to be accessed by the control logic.
TxD	O	The NRZI encoded data are transmitted through the TxD line.
$\overline{TxC}$	I	The transmitter clock controls the TxD BAUD rate.
RxD	I	The Receiver Data line receives the NRZI encoded data from the communication data channel.
$\overline{RxC}$	I	The Receiver clock is the 1X BAUD rate that RxD is received.
$\overline{32X\ CLK}$	I	The 32X clock is used to provide clock recovery when Asynchronous modem is used. In loop configuration the loop station can run without an accurate 1X clock by using the 32X CLK.
$\overline{DPLL}$	O	Digital Phase Locked Loop output can be tied to RxC and/or TxC when 1X clock is not available. DPLL is used with 32X CLK.
$\overline{FLAG\ DET}$	O	Flag Detect signals that a flag (01111110) has been detected.
$\overline{RTS}$	O	Request to send signals the terminal is ready to transmit Data.
$\overline{CTS}$	I	Clear to send signals that the modem is ready to accept data for transmission.
$\overline{CD}$	I	Carrier Detect signals that the line transmission has started and the 8273 may begin sample data on RxD line.
$\overline{PA_{0\text{-}2}}$	I	General Purpose input Ports. The logic levels on these lines can be Read by the CPU through the Data Bus Buffer.
$\overline{PB_{0\text{-}3}}$	O	General Purpose output Ports. The CPU can write these output lines through Data Bus Buffer.

Principles of Operation

The 8273 is fully compatible with the 8080 system Bus. As an 8080 peripheral device, it accepts commands from the CPU, executes these Commands and provides a Result back to the 8080 CPU at the end of execution. Communication with CPU is through the activating of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ pins. The A_1A_0 select the appropriate registers on chip:

A1	A0	CS•RD	CS•WR
0	0	Status Reg	Command Reg
0	1	Result Reg	Parameter Reg
1	0	TX Reg	—
1	1	RX Reg	—

The SDLC chip operation is composed of the following general sequence of events:

The Command Phase

During the Command Phase, the CPU issues a command byte to the 8273. The command byte provides a general description of the type of operation requested. Many operations require more detailed information about the command. In such case, from zero to four parameters are written following the command byte to provide such information. The various commands that the 8273 can recognize are listed in the Software Operation Section.

The Execution Phase

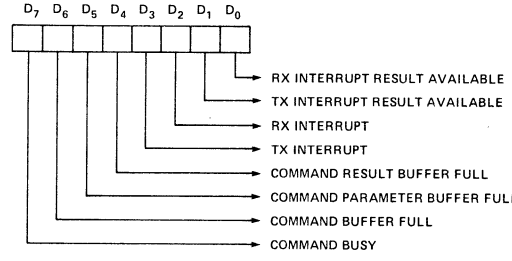
After the last parameter is written into the 8273, the SDLC chip enters the Execution Phase. During this phase there is no need for CPU involvement. The system might interface with the 8257 (DMA controller) if programmed to do so, for high speed data transfers (see System Diagram). On the other hand for low speed data rate communication TxINT and RxINT can be used.

The Result Phase

During the Result Phase, the SDLC chip notifies the CPU of the outcome of the command execution. This phase may be initiated by:

1. The successful completion of an operation.
2. An error detected during an operation.

In the Result Phase, the CPU Reads the Status Register which provides the following information.

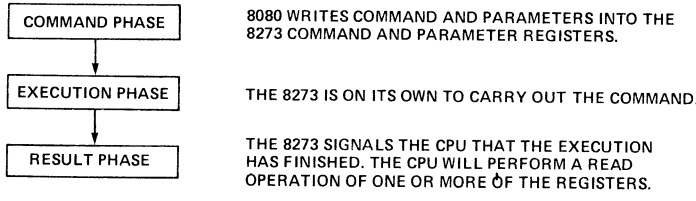


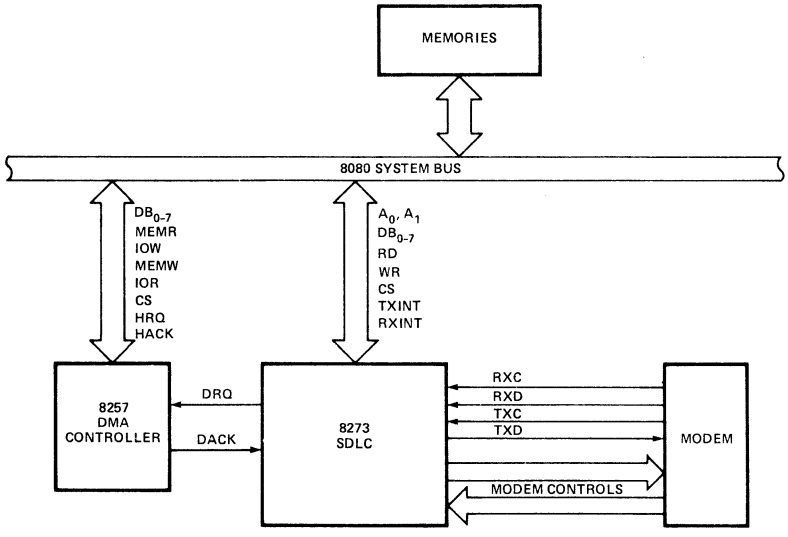
Based on the status of the Status Register, the CPU may Read the Tx Reg, Rx Reg, or Result Register, if more information is needed.

Software Operation

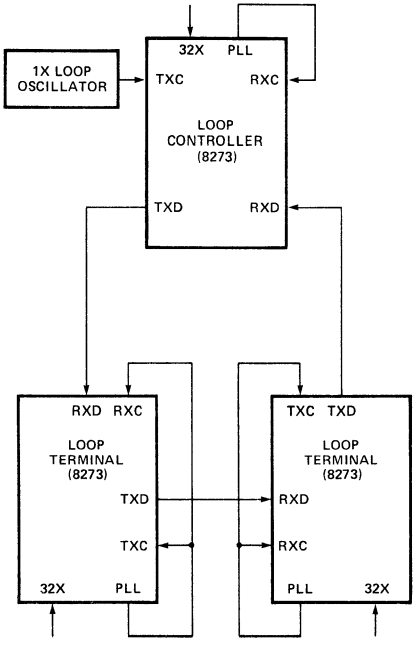
The 8273 can accept many powerful commands from the CPU. The following is a list of such commands (associated parameters not shown).

General Receive
Selective Receive
Selective Loop Receive
End of Polling Search
Receive Disable
Transmit Frame
Loop Transmit
Transparent Transmit
Abort Tx Frame
Abort Loop Tx
Abort Transparent Tx
Read Port A
Read Port B
Set/Reset 1 Bit Delay
Set/Reset Serial I/O
Set/Reset Operating Mode
Set/Reset Port A/B Bit

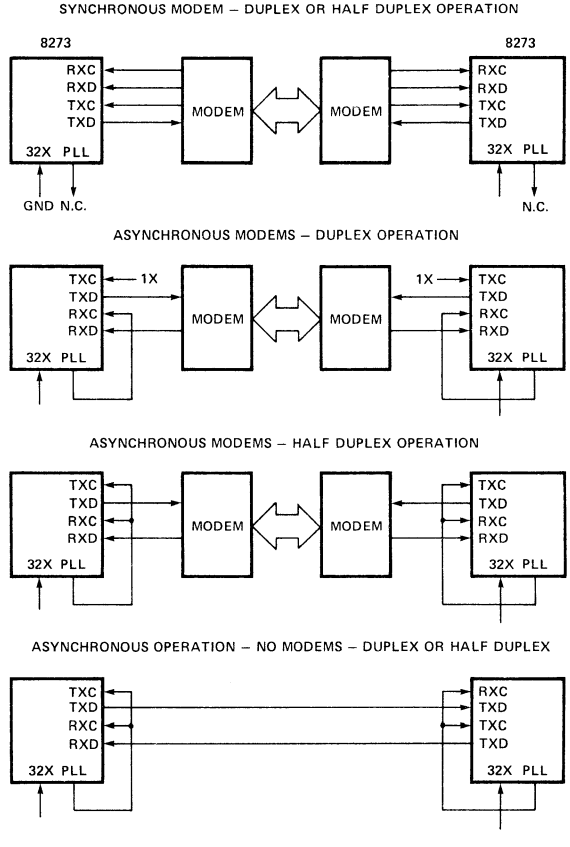




8273 SYSTEM DIAGRAM



SDLC LOOP APPLICATION



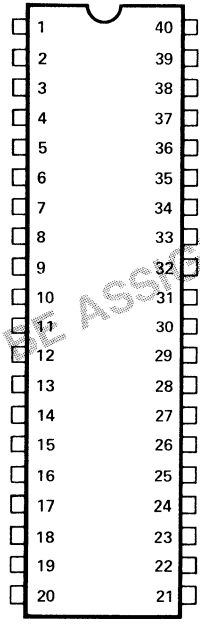
8273 MODEM OPERATION

8275
PROGRAMMABLE CRT CONTROLLER

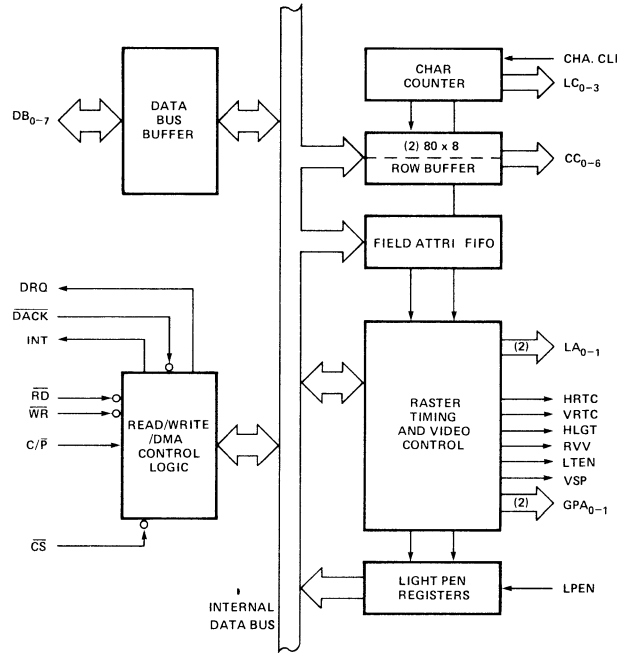
- **Programmable Screen and Character Formats**
- **Six Independent Visual Field Attributes**
- **Eleven Visual Character Attributes (Graphic Capability)**
- **Cursor Control (4 Types)**
- **Light Pen Detection and Register**
- **Dual Row Buffers**
- **Programmable DMA Burst Mode**
- **Single +5 Volt Supply**
- **40 Pin Package**

The 8275 Programmable CRT Controller is a single chip device designed to interface CRT Raster Scan Displays with the 8080 Microcomputer System. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility, designed into the 8275, will allow simple interface to almost any Raster Scan Display with a minimum of external hardware and software overhead.

PIN CONFIGURATION



BLOCK DIAGRAM



General

The CRT Controller (8275) is a single chip, programmable, NMOS-LSI device which is designed to provide an interface for microcomputers to a large class of CRT character displays. The chip provides the display row buffering, raster timing, cursor timing, light pen detection and visual attribute decoding. It is programmable to a large number of different display formats. The controller can be interfaced to standard character generator ROMs for dot matrix decoding.

The controller can generate a screen format size of from 1 to 80 characters per row, 1 to 64 rows per screen and from 1 to 16 horizontal lines per character row.

The device has 7 character code address bits allowing 6 or 7 bit ASCII capability or can be used with other 7 bit codes to generate up to 128 characters.

Hardware Description

The 8275 is Packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name	I/O	Description
V_{cc}	—	+5V power supply
GND	—	Ground
CCLK	I	Character Clock (from dot/timing logic)
DB_7-DB_0	I/O	Bi-directional three-state data bus lines. The outputs are enabled during a read of the C or P ports.
$\overline{CS}$	I	Chip select. The read and write are enabled by $\overline{CS}$.
$\overline{RD}$	I	Read input. A control signal to read registers.
$\overline{WR}$	I	Write input. A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
C/$\overline{P}$	I	Command or data register select. A high input on C/$\overline{P}$ selects the "C" port or command registers and a low input selects the "P" port or parameter registers.
INT	O	Interrupt request. Output signal to the 8080 system indicating that a change of status has occurred.
DRQ	O	DMA request. Output signal to the 8257 DMA controller requesting a DMA cycle.
$\overline{DACK}$	I	DMA acknowledge. Input signal from the 8257 DMA controller acknowledging that the requested DMA cycle has been granted.
LPEN	I	Light pen. Input Signal from the CRT system signifying that a light pen signal has been detected.
HRTC	O	Horizontal retrace. Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
VRTC	O	Vertical retrace. Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
LC0-LC3	O	Line count. Output from the line counter which is used to address the character generator for the line positions on the screen.
CC0-CC6	O	Character codes. Output from the row buffers used for character selection in the character generator.
GPA0, GPA1	O	General purpose attribute codes. Outputs which are enabled by the general purpose field attribute codes.
LA0, LA1	O	Line attribute codes. These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.
HLGT	O	Highlight. Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.
RVV	O	Reverse video. Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
LTEN	O	Light enable. Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by the character attribute codes during generation of graphics display.
VSP	O	Video suppression. Output signal used to blank the video signal to the CRT. This output is active: — during the horizontal and vertical retrace intervals. — at the top and bottom lines of rows if the number of lines/row are greater than or equal to 9. — when an end of row or end of screen code is detected. — when a DMA underrun occurs. — at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for character and field attributes)—to create blinking displays as specified by cursor, character attribute, or field attribute programming.

Principles of Operation

The basic elements of the CRT controller are the two row buffers (80X8), cursor position, light pen position, and visual attribute decode and control logic. The CRT controller is used with the DMA chip (8257) to provide the high speed controlling function of a CRT.

Two row buffers are utilized to provide display row refresh. Each buffer is alternately loaded from main memory and then used to provide characters to the external character generator and internal visual attribute decode logic during row display. Each buffer is loaded from main memory by DMA cycles which are requested by the CRT controller at programmable intervals. The controller can also be programmed to request a single DMA at a time or bursts of 2, 4, or 8 bytes.

Raster Control and Timing

The raster logic provides the proper video scan timing for the CRT. The various parameters of the raster timing are programmable at controller reset. Raster timing is derived from the basic character interval clock which is provided to the controller from the external dot timing logic. The following count functions are performed by the raster logic:

- Character Count
- Horizontal Retrace Interval Count
- Line Count
- Row Count
- Vertical Retrace Interval Count
- Blink Timing

Cursor

The cursor location is determined by the cursor line and character position registers which are loaded by command to the controller. The cursor can be programmed to appear on the display as 1) a blinking underline, 2) a blinking reverse video block, 3) a non-blinking underline, or 4) a non-blinking reverse video block.

Light Pen

When the controller detects a light pen signal, the row and character position coordinates of the raster are stored in a pair of registers. On command to the controller, these registers can be read by the microprocessor. The registers are loaded on the 0-1 transition of the light pen input which is internally synchronized with the character clock. The horizontal address will be off three character positions (more if external delays are present) and has to be corrected in the software. In addition, the controller has a status flag to indicate that the light pen signal was detected.

Visual Attributes

Visual attributes are generated and timed by the CRT controller without the intervention of the external character generator. They are actuated and controlled by special code combinations. These attribute codes can affect the display for just the character position in which they appear (character type) or they may affect a field of characters (field type).

Field Attributes

The field attributes are control codes which will affect the visual characteristics for a field of characters starting at the character following the field attribute code up to the character which precedes the next field attribute code. A field attribute code does not have to occupy a display position. Any of the following field display can be independently selected for a field:

- Blink
- Highlight
- Reverse Video
- Underline

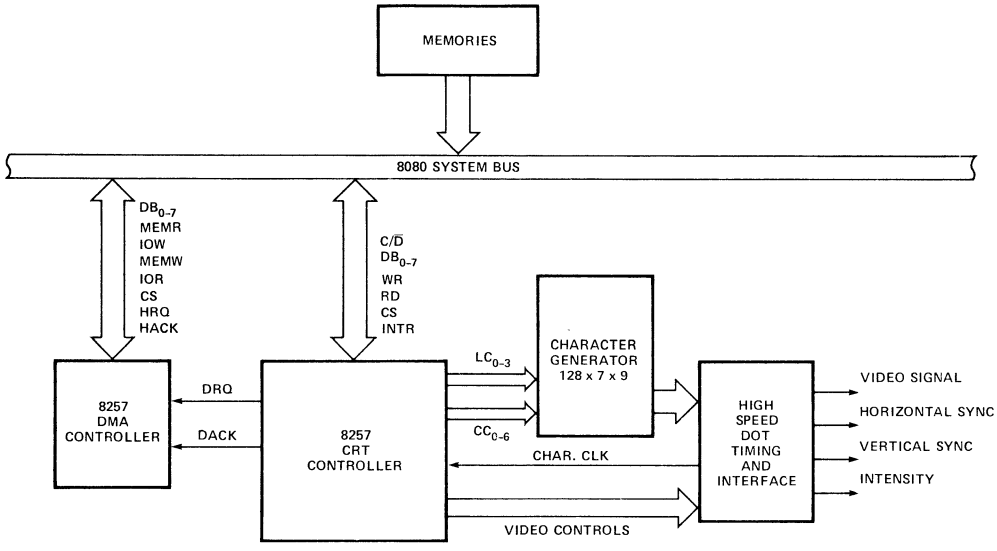
Character Attributes

A character attribute generates a graphics symbol in the character position without the use of an external character generator. A character attribute is generated through the Line Attribute outputs together with the Video Suppress and Light Enable outputs. The external logic then can generate the proper symbol. Character attributes can be programmed to blink or be highlighted.

Software Operation

The 8275 can accept commands from the CPU at any time to perform the CRT controlling functions. A command ($C/\overline{P}$=1) from the CPU to the 8275 chip may be followed by up to 4 bytes of parameters ($C/\overline{P}$=0). The list of commands and their associated parameters are summarized below:

$C/\overline{P}$	DB	
1	0 0 0 X X X X X	RESET & STOP DISPLAY
0	S H H H H H H H	SCREEN COMPOSITION #1
0	V V R R R R R R	SCREEN COMPOSITION #2
0	U U U U L L L L	SCREEN COMPOSITION #3
0	D F C C Z Z Z Z	SCREEN COMPOSITION #4
1	0 0 1 S S S B B	START DISPLAY
1	0 1 0 X X X X X	STOP DISPLAY
1	0 1 1 X X X X X	READ LIGHT PEN (*2 $\overline{RD}$)
1	1 0 0 X X X X X	LOAD CURSOR POSITION
0	X C C C C C C C	CURSOR X-POSITION
0	X X C C C C C C	CURSOR Y-POSITION
1	1 0 1 X X X X X	ENABLE INTERRUPT
1	1 1 0 X X X X X	DISABLE INTERRUPT



8275 SYSTEM DIAGRAM

8279

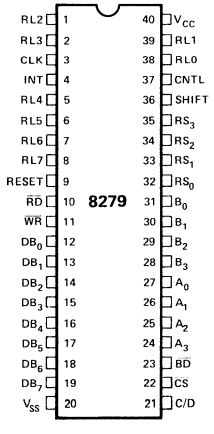
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- Simultaneous Keyboard Display Operations
- Scanned Keyboard Mode
- Scanned Sensor Mode
- Strobed Input Entry Mode
- 8 Character Keyboard FIFO
- 2 Key or N Key Rollover with Contact Debounce
- Dual 8 or 16 Numerical Display
- Single 16 Character Display
- Right or Left Entry 16 Byte Display RAM
- Mode Programmable from CPU
- Programmable Scan Timing
- Interrupt Output on Key Entry

The 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with microprocessors. The keyboard portion can provide a scanned interface to a 64 contact key matrix which can be expanded to 128. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the Hall effect and Ferrite variety. Key depressions can be 2 key or N key rollover. Keyboard entries are debounced and stored in an 8 character FIFO. If more than 8 characters are entered, over run status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has a 16 x 8 display RAM which can be organized into a dual 16 x 4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

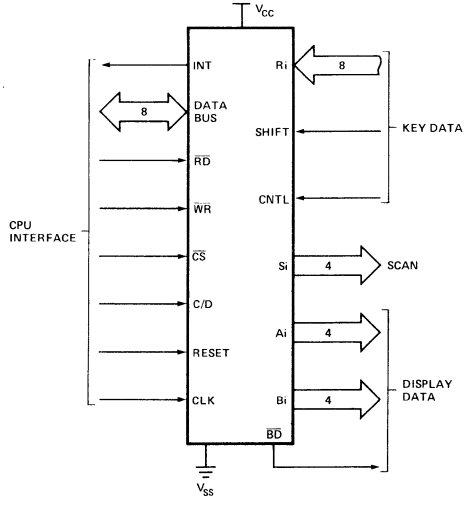
PIN CONFIGURATION



PIN NAMES

DB_{0-7}	DATA BUS (BI-DIRECTIONAL)
CLK	CLOCK INPUT
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
C/D	COMMAND/DATA INPUT
INT	INTERRUPT OUTPUT
S_{0-3}	SCAN OUTPUTS
R_{0-7}	RETURN INPUTS
SHIFT	SHIFT INPUT
CNTL/STB	CONTROL/STROBE INPUT
A_{0-3}	DISPLAY (A) OUTPUTS
B_{0-3}	DISPLAY (B) OUTPUTS
$\overline{BD}$	BLANK DISPLAY OUTPUT

LOGIC SYMBOL



8279 BASIC FUNCTIONAL DESCRIPTION

Introduction

Since data input and display are an integral part of many microprocessor designs, the system designer needs an interface that can control these functions without placing a large load on the CPU. The 8279 provides this function for 8-bit mocroprocessors such as the 8080.

The 8279 has two sections: keyboard and display. The keyboard section can interface to regular typewriter style keyboards or random toggle or thumb switches. The display section drives alphanumeric displays or a bank of indicator lights. Thus the CPU is relieved from scanning the keyboard or refreshing the display.

The 8279 is designed to directly connect to the 8080 bus. The CPU can program all operating modes for the 8279. These modes include:

Input Modes

- Scanned Keyboard — with encoded (8 x 8 x 4 key keyboard) or decoded (4 x 8 x 4 key keyboard) scan lines. A key depression generates a 6-bit encoding of key position. Position and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key or N-key rollover.
- Scanned Sensor Matrix — with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines. Key status (open or closed) stored in RAM addressable by CPU.
- Strobed Input — Data on return lines during control line strobe is transferred to FIFO.

Output Modes

- 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit.
- Right entry or left entry display formats.

Other features of the 8279 include:

- Mode programming from the CPU.
- Programmable clock to match the 8279 scan times to the CPU cycle time.
- Interrupt output to signal CPU when there is keyboard or sensor data available.
- An 8 byte FIFO to store keyboard information.
- 16 byte internal Display RAM for display refresh. This RAM can also be read by the CPU.

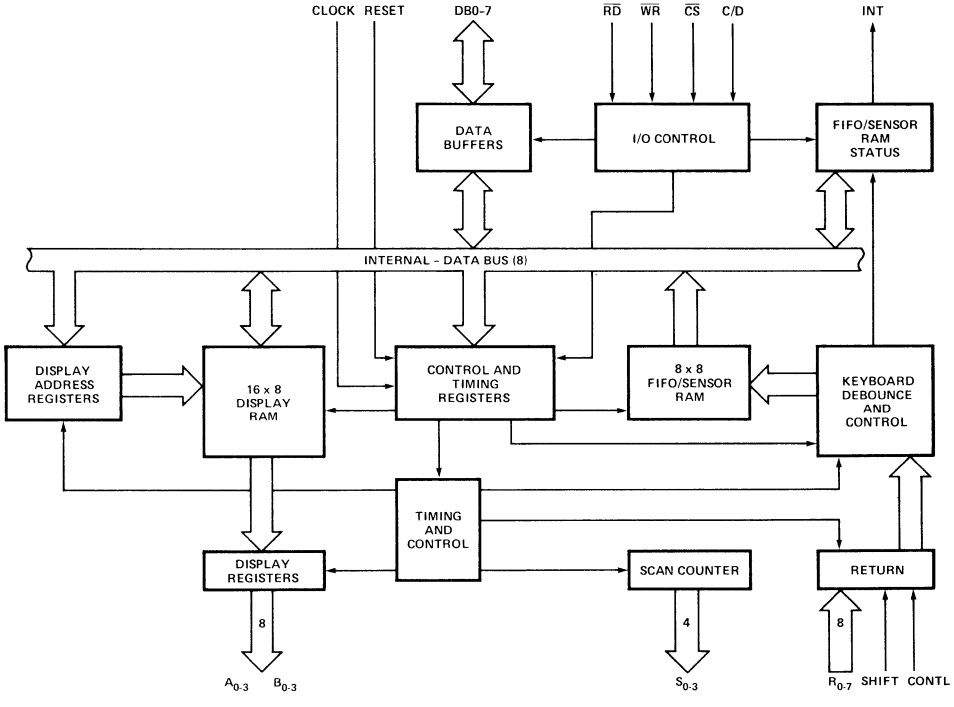


FIGURE 1. 8279 BLOCK DIAGRAM

Hardware Description

The 8279 is packaged in a 40 pin DIP. The following is a functional description of each pin.

No. Of Pins	Designation	Function
8	DB0-DB7	Bi-directional data bus. All data and commands between the CPU and the 8279 are transmitted on these lines.
1	CLK	Clock from system used to generate internal timing.
1	RESET	A high signal on this pin resets the 8279.
1	$\overline{CS}$	Chip Select. A low on this pin enables the interface functions to receive or transmit.
1	C/D	Command/Data. A high on this line indicates the signals in or out are interpreted as a command. A low indicates that they are data.
2	$\overline{RD}$, $\overline{WR}$	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
1	INT	Interrupt Output. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
2	V_{SS}, V_{CC}	Ground and +5 ±10% power supply pins.
4	S0-S3	Scan outputs which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
8	R0-R7	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
1	SHIFT	The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes.
1	CNTL/STB	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in the Strobed Input mode.
4 4	A0-A3 B0-B3	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (S0-S3) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8 bit port.
1	$\overline{BD}$	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.

Principles of Operation

The following is a description of the major elements of the 8279 Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 1.

I/O Control and Data Buffers

The I/O control section uses the CS, C/D, $\overline{RD}$ and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers. All data flow to and from the 8279 is enabled by $\overline{CS}$. The character of the information, given or desired by the CPU, is identified by C/D. A logic one means the information is a command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Buffers. The Data Buffers are bi-directional buffers that connect the internal bus to the external bus. When the chip is not selected ($\overline{CS}$ = 1), the devices are in a high impedance state. The drivers input during WR • CS and output during RD • CS.

Control and Timing Registers and Timing Control

These registers store the keyboard and display modes and other operating conditions programmed by the CPU. The modes are programmed by presenting the proper command on the data lines with C/D = 1 and then sending a $\overline{WR}$. The command is latched on the rising edge of $\overline{WR}$. The command is then decoded and the appropriate function is set. The timing control contains the basic timing counter chain. The first counter is a ÷ N prescaler that can be programmed to match the CPU cycle time to the internal timing. The prescaler is software programmed to a value between 2 and 31. A value which yields an internal frequency of 100 kHz gives a 5.1 ms keyboard scan time and a 10.3 ms debounce time. The other counters divide down the basic internal frequency to provide the proper key scan, row scan, keyboard matrix scan, and display scan times.

Scan Counter

The scan counter has two modes. In the encoded mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the keyboard and display. In the decoded mode, the scan counter decodes the least significant 2 bits and provides a decoded 1 of 4 scan. Note than when the keyboard is in decoded scan so is the display. This means that only the first 4 characters in the Display RAM are displayed.

Return Buffers and Keyboard Debounce and Control

The 8 return lines are buffered and latched by the Return Buffers. In the keyboard mode, these lines are scanned, looking for key closures in that row. If the debounce circuit detects a closed switch, it waits about 10 msec to check if the switch remains closed. If it does, the address of the switch in the matrix plus the status of SHIFT and CONTROL are transferred to the FIFO. In the scanned Sensor Matrix modes, the contents of the return lines is directly transferred to the corresponding row of the Sensor RAM (FIFO) each key scan time. In Strobed Input mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

FIFO/Sensor RAM and Status

This block is a dual function 8 x 8 RAM. In Keyboard or Strobed Input modes, it is a FIFO. Each new entry is written into successive RAM positions and each is then read in order of entry. FIFO status keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or writes will be recognized as an error. The status can be read by an $\overline{RD}$ with $\overline{CS}$ low and C/D high. The status logic also provides an INT signal when the FIFO is not empty. In Scanned Sensor Matrix mode, the memory is a Sensor RAM. Each row of the Sensor RAM is loaded with the status of the corresponding row of sensor in the sensor matrix. In this mode, INT is high if a change in a sensor is detected.

Display Address Registers and Display RAM

The Display Address Registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The Display RAM can be directly read by the CPU after the correct mode and address is set. The addresses for the A and B nibbles are automatically updated by the 8279 to match data entry by the CPU. The A and B nibbles can be entered independently or as one word, according to the mode that is set by the CPU. Data entry to the display can be set to either left or right entry. See Interface Considerations for details.

Software Operation

8279 Commands

The following commands program the 8279 operating modes. The commands are sent on the Data Bus with $\overline{CS}$ low and C/D high and are loaded to the 8279 on the rising edge of $\overline{WR}$.

Keyboard/Display Mode Set

	MSB							LSB
Code:	0	0	0	D	D	K	K	K

Where DD is the Display Mode and KKK is the Keyboard Mode.

DD

0	0	8 8-bit character display — Left entry
0	1	16 8-bit character display — Left entry*
1	0	8 8-bit character display — Right entry
1	1	16 8-bit character display — Right entry

For description of right and left entry, see Interface Considerations. Note that when decoded scan is set in keyboard mode, the display is reduced to 4 characters independent of display mode set.

KKK

0	0	0	Encoded Scan Keyboard — 2 Key Rollover*
0	0	1	Decoded Scan Keyboard — 2-Key Rollover
0	1	0	Encoded Scan Keyboard — N-Key Rollover
0	1	1	Decoded Scan Keyboard — N-Key Rollover
1	0	0	Encoded Scan Sensor Matrix
1	0	1	Decoded Scan Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

Code:	0	0	1	P	P	P	P	P

Where PPPPP is the prescaler value 2 to 31. The programmable prescaler divides the external clock by PPPPP to get the basic internal frequency. Choosing a divisor that yields 100 KHz will give the specified scan and debounce times. Default after a reset pulse (but not a program clear) is 31.

Read FIFO/Sensor RAM

Code:	0	1	0	AI	X	A	A	A	X = Don't Care

Where AI is the Auto-Increment flag for the Sensor RAM and AAA is the row that is going to be read by the CPU. AI and AAA are used only if the mode is set to Sensor Matrix. This command is used to specify that the source of data reads ($CS \bullet RD \bullet \overline{CD}$) by the CPU is the FIFO/Sensor RAM. No additional commands are necessary as long as

**Default after reset.*

data is desired from the FIFO/Sensor RAM. Another command is necessary if reading is desired from a different row than has been selected. If AI is a one, the row select counter will be incremented after each read so the next read will be from the next Sensor RAM row.

In the Auto Increment mode for reading data from the FIFO/Sensor RAM, each read advances the address by one so that the next read is from the next character. This Auto Incrementing has no effect on the display.

Read Display RAM

Code:

0	1	1	AI	A	A	A	A

Where AI is the Auto-Increment flag for the Display RAM and AAAA is the character that the CPU is going to read next. Since the CPU uses the same counter for reading and writing, this command also sets the next write location and Auto-Increment mode. This command is used to specify the display RAM as the data source for CPU data reads. If AI is set, the character address will be incremented after each read (or write) so that the next read (or write) will be from (to) the next character.

Write Display RAM

Code:

1	0	0	AI	A	A	A	A

Where AI is the Auto-Increment flag for the Display RAM and AAAA is the character that the CPU is going to write next. The addressing and Auto-Increment are identical to Read Display RAM. The difference is that Write Display RAM does not affect the source of CPU reads. The CPU will read from whichever RAM (Display or FIFO/Sensor) was last specified. This command will, however, change the location the next Display RAM read will be from if that source was specified.

Display Write Inhibit/Blanking

Code:

1	0	1	X	IW	IW	BL	BL
				A	B	A	B

Where IW is Inhibit Writing (nibble A or B) and BL is Blanking (nibble A or B). If the display is being used as a dual 4-bit display, then it is necessary to mask one of the 4-bit halves so that entries to the Display from the CPU do not affect the other half. The IW flags allow the programmer to do this. It is also useful to be able to blank either half when that half is not to be displayed. The BL flags blank the display. The next command sets the output code to be used as a "blank". Default after reset is all zeros. Note that to blank a display formatted as a single 8-bit output, it is necessary to set both BL flags to entirely blank the display. A "1" sets the flag. Reissuing the command with a "0" resets the flag.

Clear

Code:

1	1	0	C_D	C_D	C_D	C_F	C_A

Where C_D is Clear Display, C_F is Clear FIFO Status (including interrupt), and C_A is Clear All. C_D is used to clear all positions of the Display RAM to a programmable code. All ones, all zeros and hexadecimal 20 are possible. The 2 least significant bits of C_D are also used to specify the blanking code (see below).

C_D C_D	
0 X	All Zeros (X = Don't Care)
1 0	Hex 20 (0010 0000)
1 1	All Ones

Enable clear display when = 1 (or by C_A = 1)

Clearing the display takes one display scan. During this time the CPU cannot write to the Display RAM. The MSB of the FIFO status word will be set during this time.

C_F set the FIFO status to empty and resets the interrupt output line. After execution of a clear command with C_F set, the Sensor Matrix mode RAM pointer will be set to row 0.

C_A has the combined effect of C_D and C_F. C_A uses the C_D clearing code to determine how to clear the Display RAM. C_A also resets the internal timing chain to resynchronize it.

End Interrupt/Error Mode Set

Code:

1	1	1	E	X	X	X	X

X = Don't care.

For the sensor matrix modes this command lowers the INT line and enables further writing into RAM. (The INT line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset.)

For the N-key rollover mode — if the E bit is programmed to "1" the chip will operate in the special Error mode. (For further details, see Interface Considerations Section.)

Status Word

The status word contains the FIFO status, error, and display unavailable signals. This word is read by the CPU when C/D is high and $\overline{CS}$ and $\overline{RD}$ are low. See Interface Considerations for more detail on status word.

Data Read

Data is read when C/D, $\overline{CS}$ and $\overline{RD}$ are all low. The source of the data is specified by the Read FIFO or Read Display commands. The trailing edge of $\overline{RD}$ will cause the address of the RAM being read to be incremented if the Auto-Increment flag is set. FIFO reads always increment (if no error occurs) independent of AI.

Data Write

Data that is written with C/D, $\overline{CS}$ and $\overline{WR}$ low is always written to the Display RAM. The address is specified by the latest Read Display or Write Display command. Auto-Incrementing on the rising edge of $\overline{WR}$ occurs if AI set by the latest display command.

INTERFACE CONSIDERATIONS

A. Scanned Keyboard Mode, 2-Key Rollover

There are three possible combinations of conditions that can occur during debounce scanning. When a key is depressed, the debounce logic is set. A full scan of the keyboard is ignored, then other depressed keys are looked for. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If the FIFO was empty, INT will be set to signal the CPU that there is an entry in the FIFO. If the FIFO was full, the key will not be entered and the error flag will be set. If another closed switch is encountered, no entry to the FIFO can occur. If all other keys are released before this one, then it will be entered to the FIFO. If this key is released before any other, it will be entirely ignored. A key is entered to the FIFO only once per depression, no matter how many keys were pressed along with it or in what order they were released. If two keys are depressed within the debounce cycle, it is a simultaneous depression. Neither key will be recognized until one key remains depressed alone. The last key will be treated as a single key depression.

B. Scanned Keyboard Mode, N-Key Rollover

With N-key Rollover each key depression is treated independently from all others. When a key is depressed, the debounce circuit waits 2 keyboard scans and then checks to see if the key is still down. If it is, the key is entered into the FIFO. Any number of keys can be depressed and another can be recognized and entered into the FIFO. If a simultaneous depression occurs, the keys are recognized and entered according to the order the keyboard scan found them.

C. Scanned Keyboard — Special Error Modes

For N-key rollover mode the user can program a special error mode. This is done by the "End Interrupt/Error Mode Set" command. The debounce cycle and key-validity check are as in normal N-key mode. If during a single debounce cycle, two keys are found depressed, this is considered a simultaneous multiple depression, and sets an error flag. This flag will prevent any further writing into the FIFO and will set interrupt (if not yet set). The error flag could be read in this mode by reading the FIFO STATUS word. (See "FIFO STATUS" for further details.) The error flag is reset by sending the normal CLEAR command with $C_F = 1$.

D. Sensor Matrix Mode

In Sensor Matrix mode, the debounce logic is inhibited. The status of the sensor switch is inputted directly to the Sensor RAM. In this way the Sensor RAM keeps an image of the state of the switches in the sensor matrix. Although debouncing is not provided, this mode has the advantage that the CPU knows how long the sensor was closed and when it was released. A keyboard mode can only indicate a validated closure. To make the software easier, the designer should functionally group the sensors by row since this is the format in which the CPU will read them. The INT line goes high if any sensor value change is detected at the end of a sensor matrix scan. The INT line is cleared by the first Data Read Command if the Auto-Increment flag is set to zero, or by the End Interrupt command if the Auto-Increment flag is set to one.

E. Data Format

In the Scanned Keyboard mode, the character entered into the FIFO corresponds to the position of the switch in the keyboard plus the status of the CNTL and SHIFT lines. CNTL is the MSB of the character and SHIFT is the next most significant bit. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.

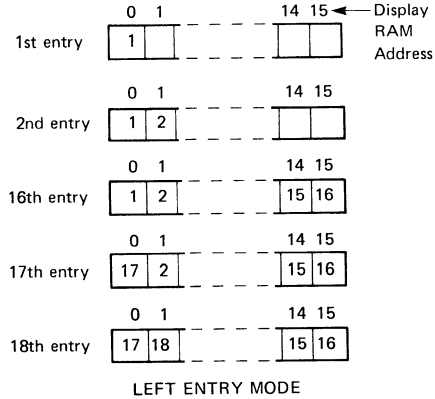
In Sensor Matrix mode, the data on the return lines is entered directly in the row of the Sensor RAM that corresponds to the row in the matrix being scanned. Therefore, each switch postion maps directly to a Sensor RAM position. The SHIFT and CNTL inputs are ignored in this mode. Note that switches are not necessarily the only thing that can be connected to the return lines in this mode. Any logic that can be triggered by the scan lines can enter data to the return line inputs. Eight multiplexed input ports could be tied to the return lines and scanned by the 8279.

In Strobed Input mode, the data is also entered to the FIFO from the return lines. The data is entered by the rising edge of a CNTL/STB line pulse. Data can come from another encoded keyboard or simple switch matrix. The return lines can also be used as a general purpose strobed input.

F. Display

Left Entry

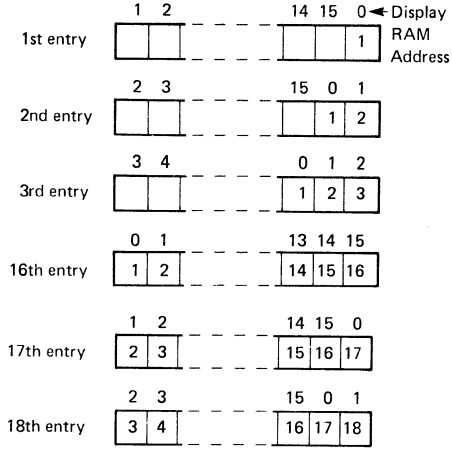
Left Entry mode is the simplest display format in that each display position directly corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 (or address 7 in 8 character display) is the right most display character. Entering characters from position zero causes the display to fill from the left. The 17th (9th) character is entered back in the left most position and filling again proceeds from there.



LEFT ENTRY MODE

Right Entry

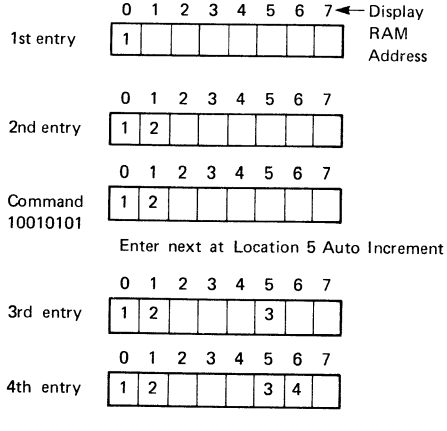
Right entry is the method used by most electronic calculators. The first entry is placed in the right most display character. The next entry is also placed in the right most character after the display is shifted left one character. The left most character is shifted off the end and is lost.



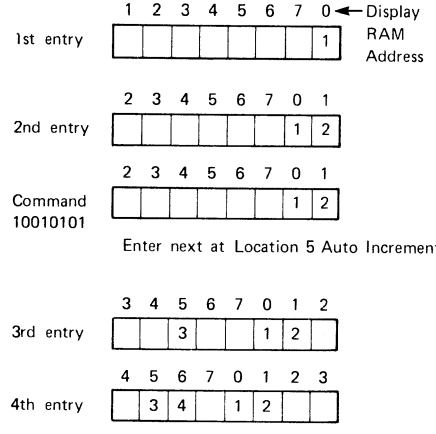
Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended.

Auto Increment

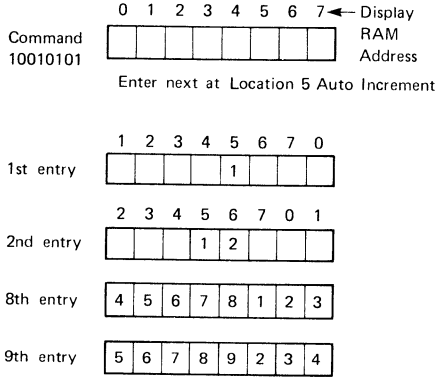
In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Auto Increment mode has no undesirable side effects and the result is predictable:



In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except if the address sequence is interrupted:



Starting at an arbitrary location operates as shown below:



Entry appears to be from the initial entry point.

8/16 Character Display Formats

If the display mode is set to an 8 character display, the on duty-cycle is double what it would be for a 16 character display (e.g., 5.1 ms scan time for 8 characters vs. 10.3 ms for 16 characters with 100 kHz internal frequency).

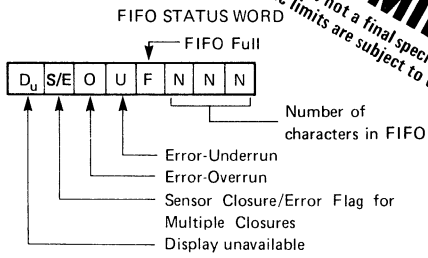
G. FIFO Status

FIFO status is used in the Keyboard and Strobed Input modes to indicate the number of characters in the FIFO and to indicate whether an error has occurred. There are two types of errors possible: overrun and underrun. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO.

The FIFO status word also has a bit to indicate that the Display RAM was unavailable because a Clear Display or Clear All command had not completed its clearing operation.

In a Sensor Matrix mode, a bit is set in the FIFO status word to indicate that at least one sensor closure indication is contained in the Sensor RAM.

In Special Error Mode the S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.



APPLICATIONS

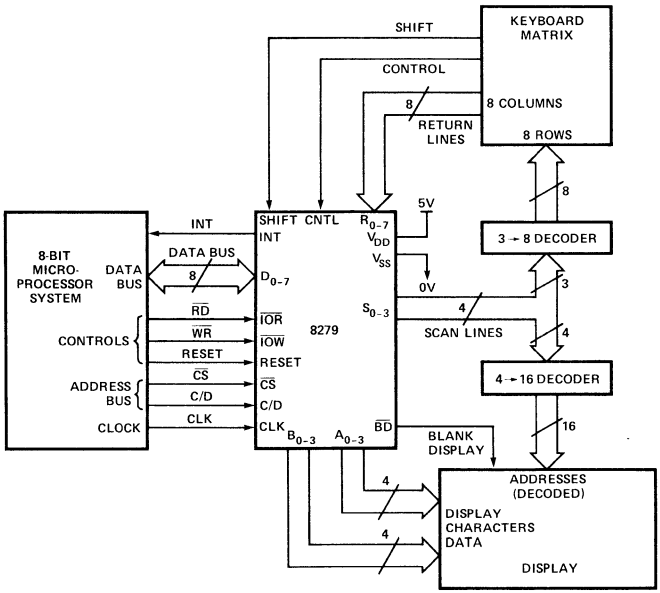


FIGURE 2. GENERAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to 125°C
Voltage on any Pin with
Respect to Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . .1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
V_{OL}	Output Low Voltage			0.45	V	I_{OL}=2.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-400 μA
V_{ILV}	Input Low Voltage (for all inputs but R's)	V_{SS}-0.5		0.8	V	
V_{IL2}	Input Low Voltage for Return Lines	V_{SS}-0.5		1.4	V	
V_{IH}	Input High Voltage	2.0			V	
I_{ILa}	Input Leakage Current			±10	μA	V_{in}=V_{CC}
I_{FL}	Output Float Leakage			±10	μA	V_{in}=V_{CC} or V_{in}=V_{SS}+.45 V
I_{CC}	Power Supply Current			120	mA	
I_{ILL}	Input Leakage Current on Return Lines, Shifts and Control			+10 -100	μA μA	V_{in}=V_{CC} V_{in}=V_{SS}
V_{OHL}	Output High Voltage on Interrupt Line	3.5			V	I_{OH}=-100 μA

A.C. CHARACTERISTICS

$T_A = 0°$ to $70°C$, $V_{CC} = \pm 10\%$, $V_{SS} = 0V$

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{RCY}	Read Cycle Time	1000		nsec	
t_{RD}	$\overline{IOR}$ to Data Out Stable		150	nsec	100 pF on Data Bus
t_{CD}	$\overline{CS}$ to Data Out Stable		250	nsec	100 pF on Data Bus
t_{CR}	C/D to $\overline{IOR}$ Set Up Time	0		nsec	
t_{RC}	C/D to $\overline{IOR}$ Hold Time	0		nsec	
t_{DW}	Data Set Up to $\overline{IOW}$ Trailing Edge	150		nsec	
t_{CW}	C/D Set Up to $\overline{IOW}$	0		nsec	
t_{WW}	$\overline{IOW}$ Pulse Width	250		nsec	
t_{WC}	C/D Hold from $\overline{IOW}$	0		nsec	
t_{WD}	Data Hold from $\overline{IOW}$	-20		nsec	
$t_{\phi W}$	Clock Pulse Width	120		nsec	
t_{CY}	Clock Period	320		nsec	
t_{CSR}	$\overline{CS}$ Stable before $\overline{IOR}$	0		nsec	
t_{RCS}	$\overline{CS}$ Hold after $\overline{IOR}$	0		nsec	
t_{RR}	$\overline{IOR}$ Width	300		nsec	
t_{CDD}	C/D to Data Output Stable		250	nsec	C_L=100 pF
t_{RDF}	Data Float after $\overline{IOR}$		100	nsec	C_L=100 pF
		10		nsec	C_L=15 pF
t_{CSW}	$\overline{CS}$ Stable before $\overline{IOW}$	0		nsec	
t_{WCS}	$\overline{CS}$ Hold from $\overline{IOW}$	0		nsec	

CAPACITANCE

SYMBOL	TEST	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{in}	Input Capacitance	5	10	pF	$V_{in}=V_{CC}$
C_{out}	Output Capacitance	10	20	pF	$V_{out}=V_{CC}$

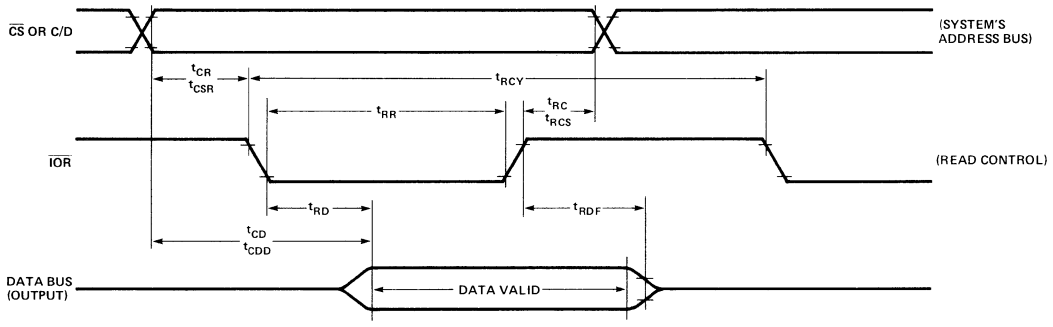
A.C. TEST CONDITIONS

Output Load . . . . . 1 TTL Gate, and C_{LOAD} = 100 pF
Input Pulse Levels . . . . . 0.8 to 2.0V
Input Pulse Rise and Fall Times . . . . . (10% to 90%) 20 nS
Timing Measurement Reference Level
Input 1.5V
Output . . . . . 0.45V to 2.2V

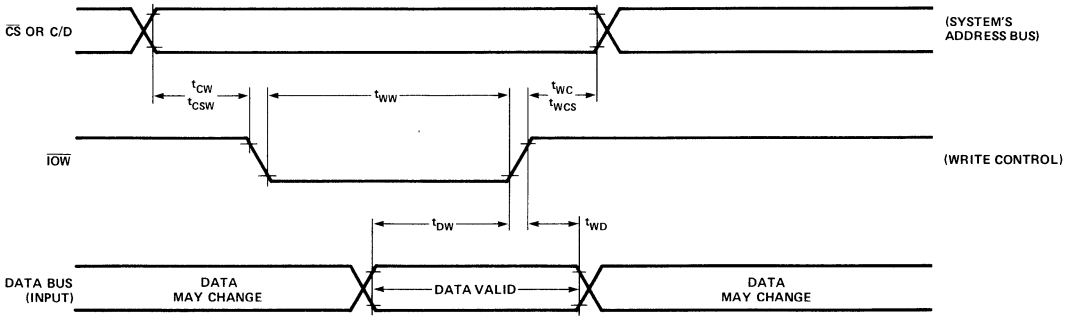
Keyboard Scan Time: 5.1 msec
Keyboard Debounce Time: 10.3 msec
Key Scan Time: 80 μsec
Display Scan Time: 10.3 msec
Digit-on Time: 480 μsec
Blanking Time: 160 μsec
Internal Clock Cycle: 10 μsec

WAVEFORMS

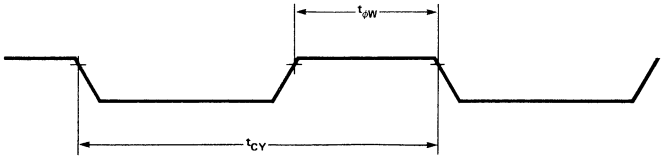
1. Read Operation



2. Write Operation



3. Clock Input



SDK-80
8080 SYSTEM DESIGN KIT

- **Complete Single Board Microcomputer System Including CPU, Memory and I/O**
- **Easy to Assemble Kit-Form**
- **High-Performance (2μs Instruction Cycle)**
- **Interfaces Directly with most Terminals (75-4800 Baud)**
- **Large Wire-Wrap area for Custom Interfaces**
- **Extensive System Monitor Software in ROM**
- **PC Board Format and Power, Compatible with INTELLEC® MDS**
- **Complete MCS-80™ Design Library**

The 8080 System Design Kit (SDK-80) is a complete, single board, microcomputer system in kit form. It contains all necessary components, including resistors, caps, crystal and miscellaneous hardware to complete construction. Included is a pre-programmed ROM that contains the system monitor for general software utilities and system diagnostics.

All that is required for operation are power supplies and a suitable terminal; TTY, CRT, etc., (level conversions and baud rate generation included on board).

The SDK-80 is an inexpensive, high-performance prototype system that has designed-in flexibility for simple interface to the users application.

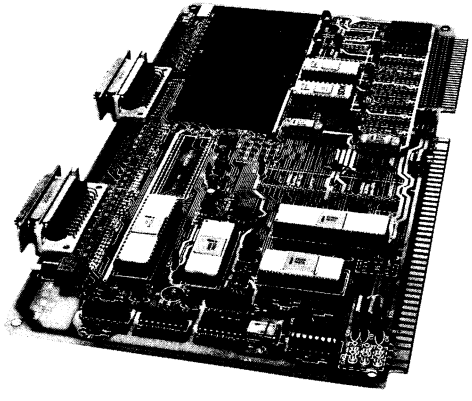
GENERAL

The SDK-80 is a complete 8080 microcomputer system on a single board, in kit form. It contains all necessary components to build a useful, functional system. Such items as resistors, caps, sockets and connectors are included. Assembly time varies from 3 to 5 hours, depending on the skill of the user.

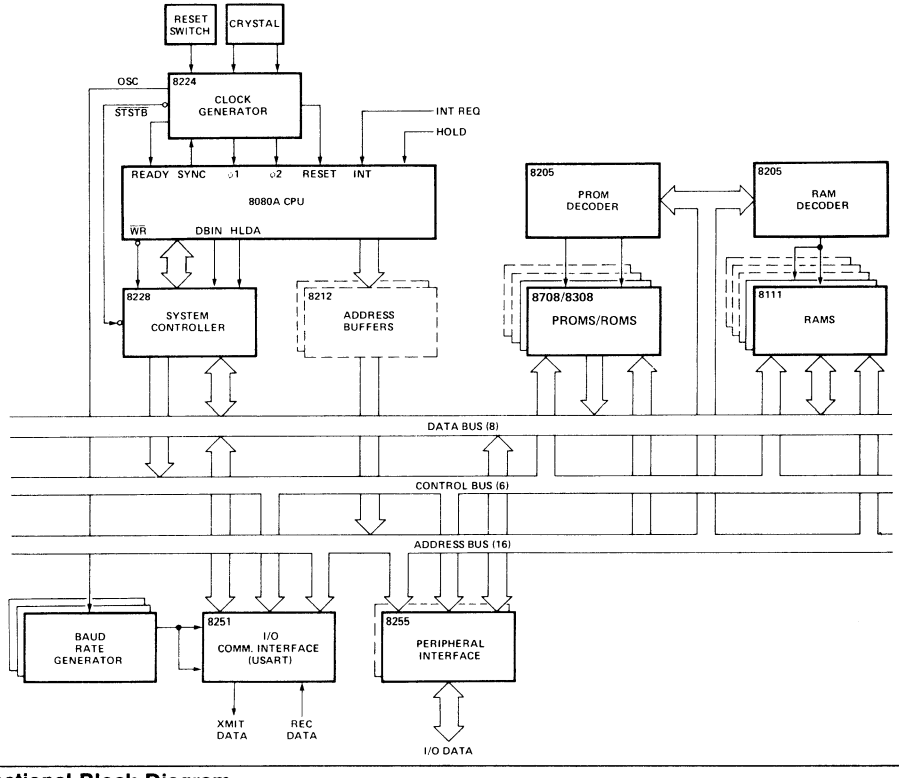
A compact but powerful system monitor is supplied with the SDK-80 to provide general software utilities and system diagnostics. It comes in a pre-programmed ROM.

The SDK-80 communicates with the outside world through the user's console terminal (TTY, CRT, etc.). The interface to most common terminals is direct and the baud rate is jumper selectable for complete flexibility. Both memory and I/O can be easily expanded by simply soldering in additional devices in locations provided for this purpose. A large area of the board (12 sq. in.) is laid out as general purpose wire-wrap for the users custom interfaces.

Only a few simple tools are required for assembly; soldering iron, cutters, screwdriver, etc. Once construction is complete, the user connects his console terminal and power supplies (3) to the SDK-80, lights it off and is ready to go. The monitor starts immediately upon power-on or reset and all commands are available to the user at that time.



Completed Board.



SDK-80 Functional Block Diagram.

SDK-80 SPECIFICATIONS

Central Processor

CPU: 8080A
Instruction Cycle: 1.95 microsecond
Tcy: 488 ns

Memory

ROM: 2K bytes (expandable to 4K bytes) 8708/8308
RAM: 256 bytes (expandable to 1K bytes) 8111
Addressing:
ROM 0000-0FFF
RAM 1000-13FF

Input/Output

Parallel: One 8255 for 24 lines (expandable to 48 lines).
Serial: One 8251 USART.
On-board baud rate generator (jumper selectable).

Baud Rates:	75	1200
	110	2400
	300	4800
	600	

Interfaces

Bus: All signals TTL compatible.
Parallel I/O: All signals TTL compatible.
Serial I/O: RS232C/EIA
20mA current loop TTY
TTL (one TTL load)

Interrupts

Single level: Generates RST7 vector.
TTL compatible input.

DMA

Hold Request: Jumper selectable.

Software

System Monitor: Pre-programmed 8708 or 8308 ROM Addresses; 0000-03FF.
Features:

Display Memory Contents	(D)
Move blocks of memory	(M)
Substitute memory locations	(S)
Insert hex code	(I)
Examine Registers	(X)
Program Control	(G)

Break Point Capability
Power-up start or system reset start.

I/O: Console Device (serial I/O)

Literature

Design Library:
8080 Users Manual
8080 Assembly Language Manual
PL/M Programming Manual
MDS Brochure
Reference Card (Programmers)
SDK-80 User's Guide

Connectors

I/O: 25 pin female (RS232C)
PCB: MDS format

Physical Characteristics (MDS Mechanical format)

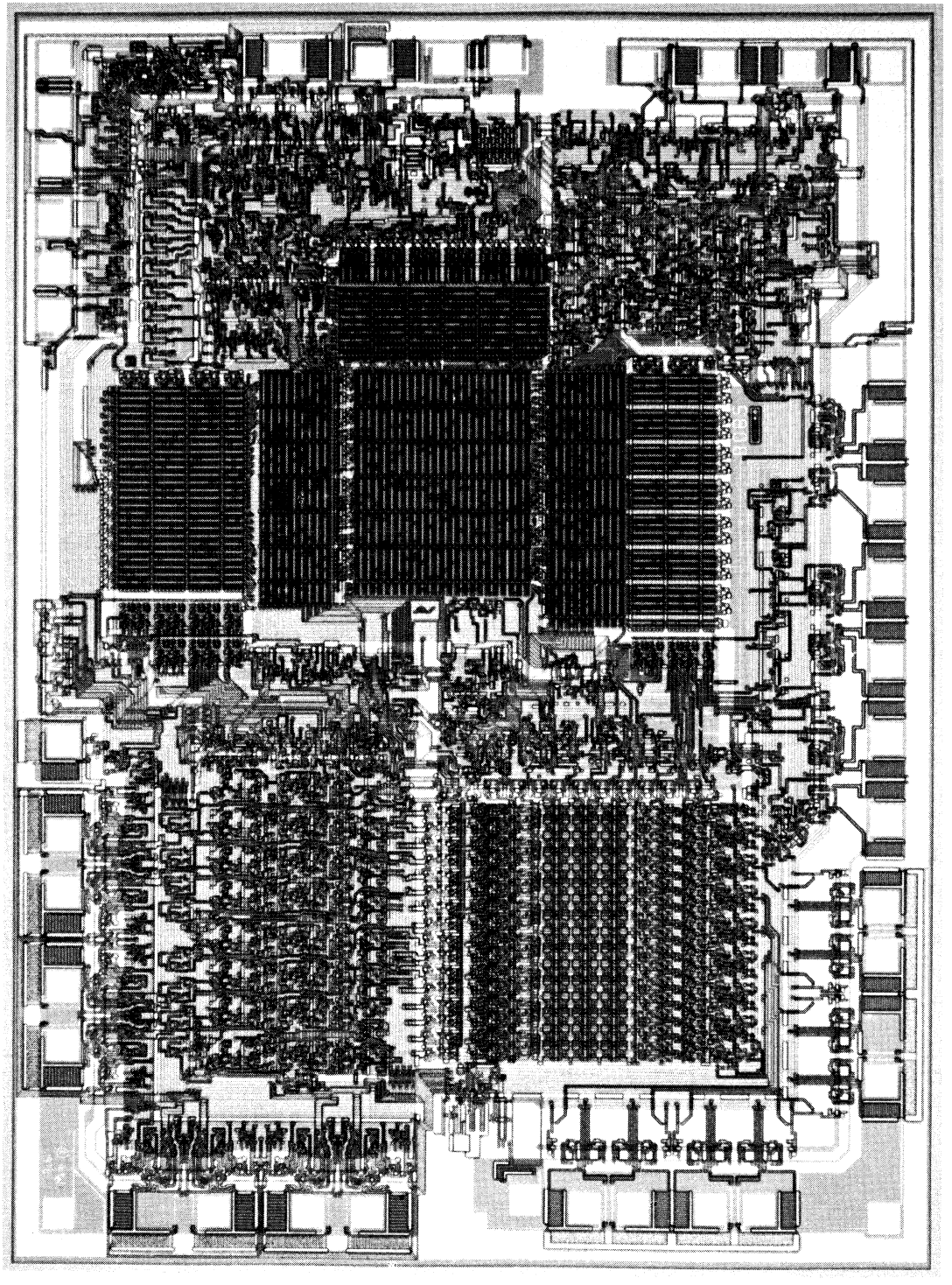
Width: 12.0 in.
Height: 6.75 in.
Depth: 0.50 in.
Weight: approx. 12 oz.

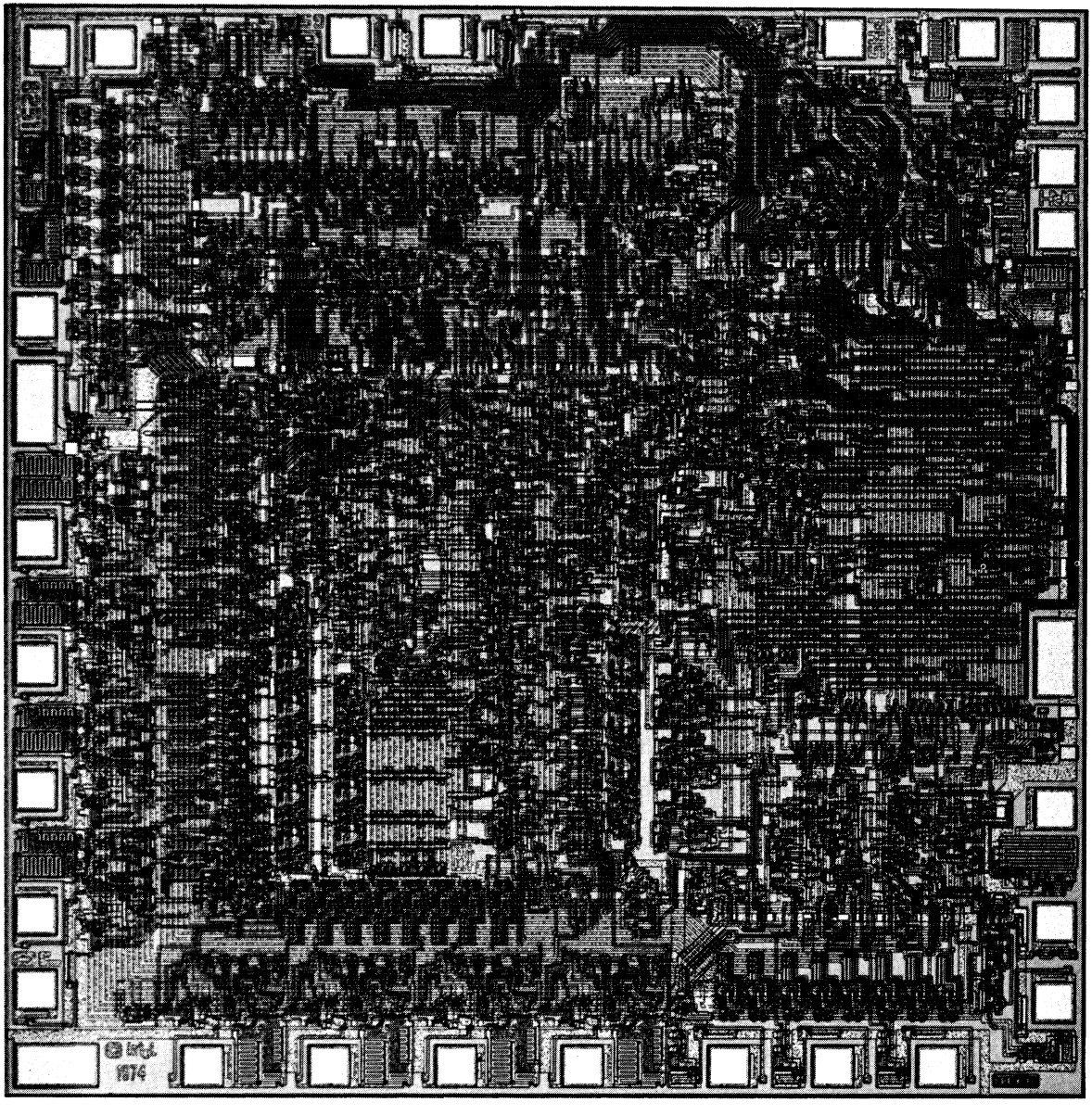
Electrical Characteristics (DC Power)

V_{CC}	5V ±5%	1.3 Amps
V_{DD}	12V ±5%	.35 Amps
V_{BB}	-10V ±5%	.20 Amps
or	-12V ±5%	

Environmental

Operating Temperature: 0-70°C




intel
1974

11

3000 Series Bipolar Microprocessor

SERIES 3000 BIPOLAR MICROCOMPUTER SYSTEM

INTRODUCTION

Since its introduction, the Series 3000 family of computing elements has found acceptance in a wide range of high performance applications from disk controllers to airborne central processors. The Series 3000 offers the flexibility, performance, and system integration necessary for an effective system solution for both high speed controllers and central processors.

The unique multiple bus structure of the 3002 Central Processing Element (CPE) eliminates the need for input data multiplexers or output latches. It also allows the designer to tailor the CPE's to suit his particular processing requirements. The 3001 Microprogram Control Unit (MCU) addresses up to 512 words of microprogram memory and controls both conditional and unconditional jumps within microprogram memory.

The entire component family has been designed to interconnect directly, minimizing the need for ancillary circuitry. It is available in commercial and military temperature range versions. In addition to the components, Intel has also developed a comprehensive support system to assist the user in writing microprograms, debugging hardware and microcode, and programming PROMs for both prototype and production systems.

Thus, with a complete family of components and a power development system, Intel provides a Total System Solution, from development to production.

TABLE OF CONTENTS

3001

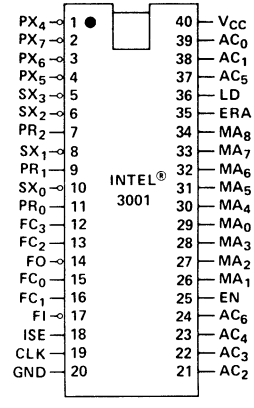
MICROPROGRAM CONTROL UNIT

The INTEL® 3001 Microprogram Control Unit (MCU) controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

- Maintenance of the microprogram address register.
- Selection of the next microinstruction based on the contents of the microprogram address register.
- Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence.
- Saving and testing of carry output data from the central processor (CP) array.
- Control of carry/shift input data to the CP array.
- Control of microprogram interrupts.

- **High Performance – 85 ns Cycle Time**
- **TTL and DTL Compatible**
- **Fully Buffered Three-State and Open Collector Outputs**
- **Direct Addressing of Standard Bipolar PROM or ROM**
- **512 Microinstruction Addressability**
- **Advanced Organization**
  - **9-Bit Microprogram Address Register and Bus**
  - **4-Bit Program Latch**
  - **Two Flag Registers**
- **Eleven Address Control Functions**
  - **Three Jump and Test Latch Functions**
  - **16-way Jump and Test Instruction Bus Function**
- **Eight Flag Control Functions**
  - **Four Flag Input Functions**
  - **Four Flag Output Functions**
- **40 Pin DIP**

PACKAGE CONFIGURATION



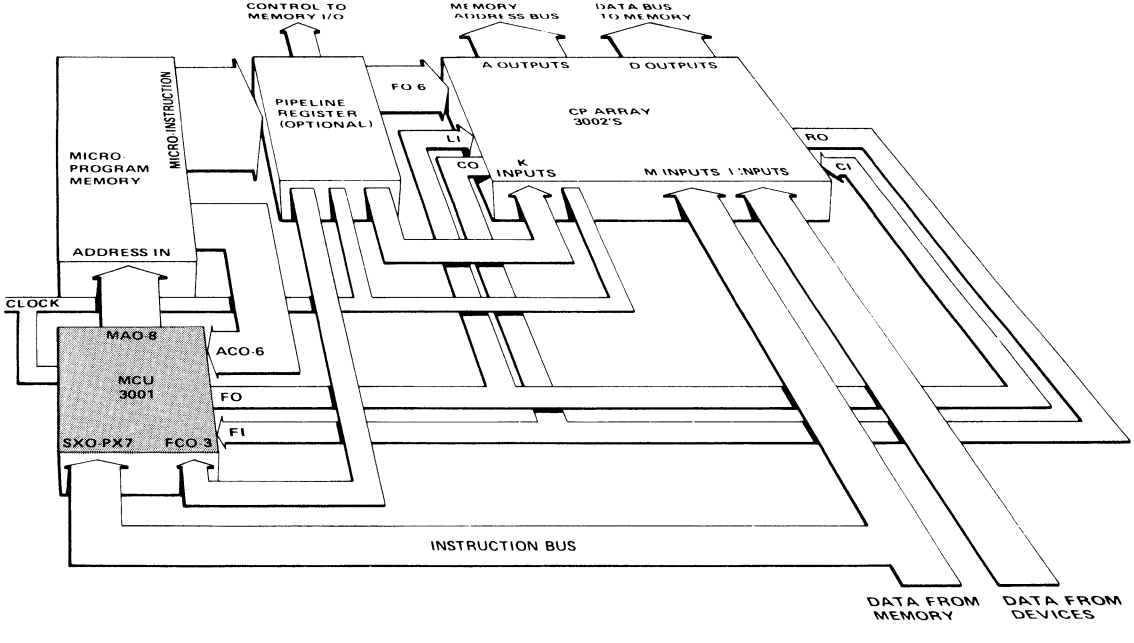


Figure 1. Block Diagram of a Typical System

3000 SERIES MPU

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1-4	PX_4-PX_7	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	active LOW
5, 6, 8, 10	SX_0-SX_3	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	active LOW
7, 9, 11	PR_0-PR_2	PR-Latch Outputs The PR-latch outputs are asynchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	open collector
12, 13, 15, 16	FC_0-FC_3	Flag Logic Control Inputs The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	
14	FO	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	active LOW three-state
17	FI	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: the flag input data is saved in the F-latch when the clock input (CLK) is low.	active LOW
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description, page 6). It can be used to provide the strobe signal required by the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits.	
19	CLK	Clock Input	
20	GND	Ground	
21-24 37-39	AC_0-AC_6	Next Address Control Function Inputs All jump functions are selected by these control lines.	
25	EN	Enable Input When in the HIGH state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26-29	MA_0-MA_3	Microprogram Column Address Outputs	three-state
30-34	MA_4-MA_8	Microprogram Row Address Outputs	three-state
35	ERA	Enable Row Address Input When in the LOW state, the enable row address input independently disables the microprogram row address outputs. It can be used with the INTEL 3214 Priority Interrupt Control Unit or other interrupt circuits to facilitate the implementation of priority interrupt systems.	
36	LD	Microprogram Address Load Input When in the active HIGH state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction busses into the microprogram register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	
40	VCC	+5 Volt Supply	

NOTE:
(1) Active HIGH unless otherwise specified.

LOGICAL DESCRIPTION

The MCU performs two major control functions. First, it controls the sequence in which microinstructions are fetched from the microprogram memory. For this purpose, the MCU contains a microprogram address register and the associated logic for selecting the next microinstruction address. The second function of the MCU is the control of the two flag flip-flops that are included for interaction with the carry input and carry output logic of the CP array. The logical organization of the MCU is shown in Figure 2.

NEXT ADDRESS LOGIC

The next address logic of the MCU provides a set of conditional and unconditional address control functions. These address control functions are used to implement a jump or jump/test operation as part of every microinstruction. That is to say, each microinstruction typically contains a jump operation field that specifies the address control function, and hence, the next microprogram address.

In order to minimize the pin count of the MCU, and reduce the complexity of the next address logic, the microprogram address space is organized as a two dimensional array or matrix. Each microprogram address corresponds to a unit of the matrix at a particular row and column location. Thus, the 9-bit microprogram address is treated as specifying not one, but two addresses – the row address in the upper five bits and the column address in the lower four bits. The address matrix can therefore contain, at most, 32 row addresses and 16 column addresses for a total of 512 microinstructions.

The next address logic of the MCU makes extensive use of this two component addressing scheme. For example, from a particular row or column address, it is possible to jump unconditionally in one operation anywhere in that row or column. It is not possible, however, to jump anywhere in the address matrix. In fact, for a given location in the matrix, there is a fixed subset of microprogram addresses that may be selected as the next address. These possible jump target addresses are referred to as a jump set. Each type of MCU address control (jump) function has a jump set associated with it. Appendix C illustrates the jump set for each function.

FLAG LOGIC

The flag logic of the MCU provides a set of functions for saving the current value of the carry output of the CP array and for controlling the value of the carry input to the CP array. These two distinct flag control functions are called flag input functions and flag output functions.

The flag logic is comprised of two flip-flops, designated the C-flag and the Z-flag, along with a simple latch, called the F-latch, that indicates the current state of the carry output line of the CP array. The flag logic is used in conjunction with the carry and shift logic of the CP array to implement a variety of shift/rotate and arithmetic functions.

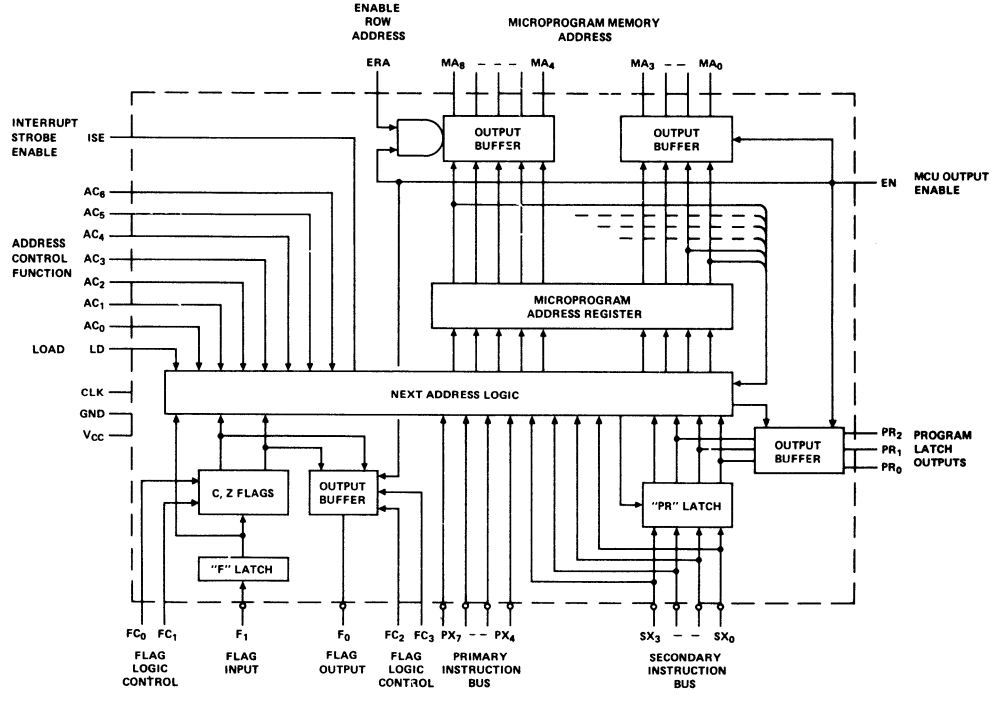


Figure 2. 3001 Block Diagram

FUNCTIONAL DESCRIPTION

ADDRESS CONTROL FUNCTIONS

The address control functions of the MCU are selected by the seven input lines designated AC_0-AC_6. On the rising edge of the clock, the 9-bit microprogram address generated by the next address logic is loaded into the microprogram address register. The next microprogram address is delivered to the microprogram memory via the nine output lines designated MA_0-MA_8. The microprogram address outputs are organized into row and column addresses as:

$$\underline{MA_8\ MA_7\ MA_6\ MA_5\ MA_4}$$
row address

$$\underline{MA_3\ MA_2\ MA_1\ MA_0}$$
column address

Each address control function is specified by a unique encoding of the data on the function input lines. From three to five bits of the data specify the particular function while the remaining bits are used to select part of either the row or column address desired. Function code formats are given in Appendix A, "Address Control Function Summary."

The following is a detailed description of each of the eleven address control functions. The symbols shown below are used throughout the description to specify row and column addresses.

Symbol	Meaning
row_n	5-bit next row address where n is the decimal row address.
col_n	4-bit next column address where n is the decimal column address.

UNCONDITIONAL ADDRESS CONTROL (JUMP) FUNCTIONS

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs to generate the next microprogram address.

Mnemonic	Function Description
JCC	Jump in current column. AC_0-AC_4 are used to select 1 of 32 row addresses in the current column, specified by MA_0-MA_3, as the next address
JZR	Jump to zero row. AC_0-AC_3 are used to select 1 of 16 column addresses in row_0, as the next address.
JCR	Jump in current row. AC_0-AC_3 are used to select 1 of 16 addresses in the current row, specified by MA_4-MA_8, as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7-MA_8, as the next row address. The current column is specified by MA_0-MA_3. The PR-latch outputs are asynchronously enabled.

FLAG CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

Mnemonic	Function Description
JFL	Jump/test F-Latch. AC_0-AC_3 are used to select 1 of 16 row addresses in the current row group, specified by MA_8, as the next row address. If the current column group, specified by MA_3, is col_0-col_7, the F-latch is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the F-latch is used to select col_{10} or col_{11} as the next column address.
JCF	Jump/test C-flag. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. If the current column group specified by MA_3 is col_0-col_7, the C-flag is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the C-flag is used to select col_{10} or col_{11} as the next column address.
JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.

PX-BUS AND PR-LATCH CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The PX-bus jump/test function uses the data on the primary instruction bus (PX_4-PX_7), the current mircoprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

Mnemonic	Function Description
JPR	Jump/test PR-latch. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. The four PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.

Mnemonic	Function Description
JLL	Jump/test leftmost PR-latch bits. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_2 and PR_3 are used to

FUNCTIONAL DESCRIPTION (con't)

select 1 of 4 possible column addresses in col_4 through col_7 as the next column address.

JRL — Jump/test rightmost PR-latch bits. AC_0 and AC_1 are used to select 1 of 4 high-order row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_0 and PR_1 are used to select 1 of 4 possible column addresses in col_{12} through col_{15} as the next column address.

JPX — Jump/test PX-bus and load PR-latch. AC_0 and AC_1 are used to select 1 of 4 row addresses in the current row group, specified by MA_6-MA_8, as the next row address. PX_4-PX_7 are used to select 1 of 16 possible column addresses as the next column address. SX_0-SX_3 data is locked in the PR-latch at the rising edge of the clock.

FLAG CONTROL FUNCTIONS

The flag control functions of the MCU are selected by the four input lines designated FC_0-FC_3. Function code formats are given in Appendix B, "Flag Control Function Summary."

The following is a detailed description of each of the eight flag control functions.

FLAG INPUT CONTROL FUNCTIONS

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line. Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Mnemonic	Function Description
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTIONS

The flag output control functions select the value to which the flag output (FO) line will be forced.

Mnemonic	Function Description
FF0	Force FO to 0. FO is forced to the value of logical 0.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

LOAD AND INTERRUPT STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active HIGH at the rising edge of the clock, the data on the primary and secondary instruction busses, PX_4-PX_7 and SX_0-SX_3, is loaded into the microprogram address register. PX_4-PX_7 are loaded into MA_0-MA_3 and SX_0-SX_3 are loaded into MA_4-MA_7. The high-order bit of the microprogram address register MA_8 is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

The interrupt strobe enable of the MCU is available on the output line designated ISE. The line is placed in the active high state whenever a JZR to col_{15} is selected as the address control function. Customarily, the start of a macroinstruction fetch sequence is situated at row_0 and col_{15} so that the INTEL 3214 Priority Interrupt Control Unit may be enabled at the beginning of the fetch/execute cycle. The priority interrupt control unit may respond to the interrupt by pulling the enable row address (ERA) input line down to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC_0-AC_6. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . –65°C to +160°C

All Output and Supply Voltages . . . . . –0.5V to +7V

All Input Voltages . . . . . –1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to 70°C V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		–0.8	–1.0	V	I_C = –5 mA
I_F	Input Load Current:					
	CLK Input		–0.075	–0.75	mA	V_F = 0.45V
	EN Input		–0.05	–0.50	mA	
	All Other Inputs		–0.025	–0.25	mA	
I_R	Input Leakage Current:					
	CLK			120	µA	V_R = 5.25V
	EN Input			80	µA	
	All Other Inputs			40	µA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current (2)		170	240	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (MA_0-MA_8, ISE, FO)	2.4	3.0		V	I_{OH} = –1 mA
I_{OS}	Output Short Circuit Current (MA_0-MA_8, ISE, FO)	–15	–28	–60	mA	V_{CC} = 5.0V
$I_{O(off)}$	Off-State Output Current:					
	MA_0–MA_8, FO			–100	µA	V_O = 0.45V
	MA_0–MA_8, FO, PR_0–PR_2			100	µA	V_O = 5.25V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) EN input grounded, all other inputs and outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%

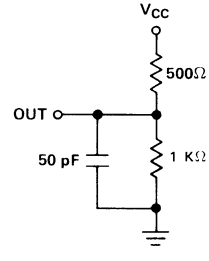
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT
t_{CY}	Cycle Time (2)	85	60		ns
t_{WP}	Clock Pulse Width	30	20		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC_0-AC_6	10	0		ns
t_{SK}	FC_0, FC_1	0			ns
t_{SX}	SX_0-SX_3, PX_4-PX_7	35	25		ns
t_{SI}	FI	15	5		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC_0-AC_6	5	0		ns
t_{HK}	FC_0, FC_1	0			ns
t_{HX}	SX_0-SX_3, PX_4-PX_7	20	5		ns
t_{HI}	FI	20	8		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA_0-MA_8, FO)	10	30	45	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		16	30	ns
t_{FO}	Propagation Delay from Control Inputs AC_0-AC_6 to Latch Outputs (PR_0-PR_2)		26	40	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA_0-MA_8, FO, PR_0-PR_2)		21	32	ns
t_{FI}	Propagation Delay from Control Inputs AC_0-AC_6 to Interrupt Strobe Enable Output (ISE)		24	40	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) $t_{CY} = t_{WP} + t_{SF} + t_{CO}$

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 10 mA and 50 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:



CAPACITANCE(2) T_A = 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance:				
	CLK, EN		11	16	pF
	All Other Inputs		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V and T_A = 25°C.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . –55°C to +125°C

Storage Temperature . . . . . –65°C to +160°C

All Input and Supply Voltages . . . . . –0.5V to +7V

All Input Voltages . . . . . –1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		–0.8	-1.2	V	I_C = –5 mA
I_F	Input Load Current:					
	CLK Input		-75	-750	μA	V_F = 0.45V
	EN Input		-50	-500	μA	
	All Other Inputs		-25	-250	μA	
I_R	Input Leakage Current:					
	CLK			120	μA	V_R = 5.5V
	EN Input			80	μA	
	All Other Inputs			40	μA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current (2)		170	250	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (MA_0-MA_8, ISE, FO)	2.4	3.0		V	I_{OH} = –1 mA
I_{OS}	Output Short Circuit Current (MA_0-MA_8, ISE, FO)	–15	–28	–60	mA	V_{CC} = 5.0V
$I_{O(off)}$	Off-State Output Current:					
	MA_0–MA_8, FO			–100	μA	V_O = 0.45V
	MA_0–MA_8, FO, PR_0–PR_2			100	μA	V_O = 5.5V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) EN input grounded, all other inputs and outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%

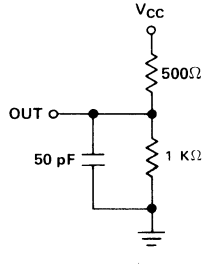
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT
t_{CY}	Cycle Time (2)	95	60		ns
t_{WP}	Clock Pulse Width	40	20		ns
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC_0-AC_6	10	0		ns
t_{SK}	FC_0, FC_1	0			ns
t_{SX}	SX_0-SX_3, PX_4-PX_7	35	25		ns
t_{SI}	FI	15	5		ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC_0-AC_6	5	0		ns
t_{HK}	FC_0, FC_1	0			ns
t_{HX}	SX_0-SX_3, PX_4-PX_7	25	5		ns
t_{HI}	FI	22	8		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA_0-MA_8, FO)	10	30	45	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		16	50	ns
t_{FO}	Propagation Delay from Control Inputs AC_0-AC_6 to Latch Outputs (PR_0-PR_2)		26	50	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA_0-MA_8, FO, PR_0-PR_2)		21	35	ns
t_{FI}	Propagation Delay from Control Inputs AC_0-AC_6 to Interrupt Strobe Enable Output (ISE)		24	40	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) $t_{CY} = t_{WP} + t_{SF} + t_{CO}$

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 10 mA and 50 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:

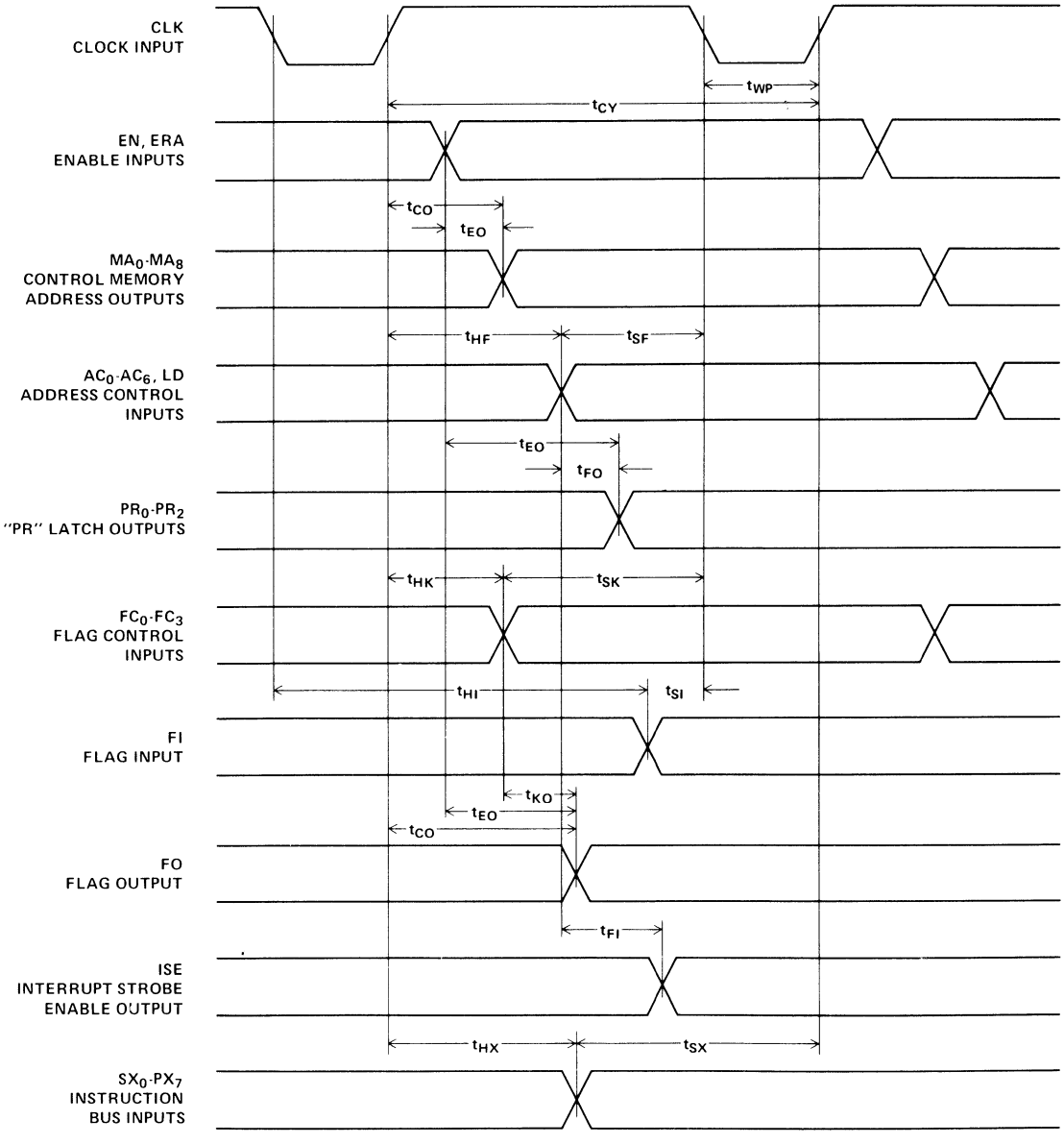


CAPACITANCE(2) T_A = 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance:				
	CLK, EN		11	16	pF
	All Other Inputs		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V and T_A = 25°C.

3001 WAVEFORMS



3002

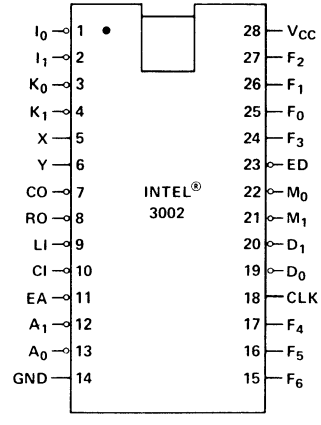
CENTRAL PROCESSING ELEMENT

The INTEL® 3002 Central Processing Element contains all of the circuits that represent a 2-bit wide slice through the data processing section of a digital computer. To construct a complete central processor for a given word width N, it is simply necessary to connect an array of N/2 CPE's together. When wired together in such an array, a set of CPE's provide the following capabilities:

- 2's complement arithmetic
- Logical AND, OR, NOT and exclusive-OR
- Incrementing and decrementing
- Shifting left or right
- Bit testing and zero detection
- Carry look-ahead generation
- Multiple data and address busses

- High Performance – 100 ns Cycle Time
- TTL and DTL Compatible
- N-Bit Word Expandable Multi-Bus Organization
  - 3 Input Data Busses
  - 2 Three-State Fully Buffered Output Data Busses
- 11 General Purpose Registers
- Full Function Accumulator
- Independent Memory Address Register
- Cascade Outputs for Full Carry Look-Ahead
- Versatile Functional Capability
  - 8 Function Groups
  - Over 40 Useful Functions
  - Zero Detect and Bit Test
- Single Clock
- 28 Pin DIP

PACKAGE CONFIGURATION



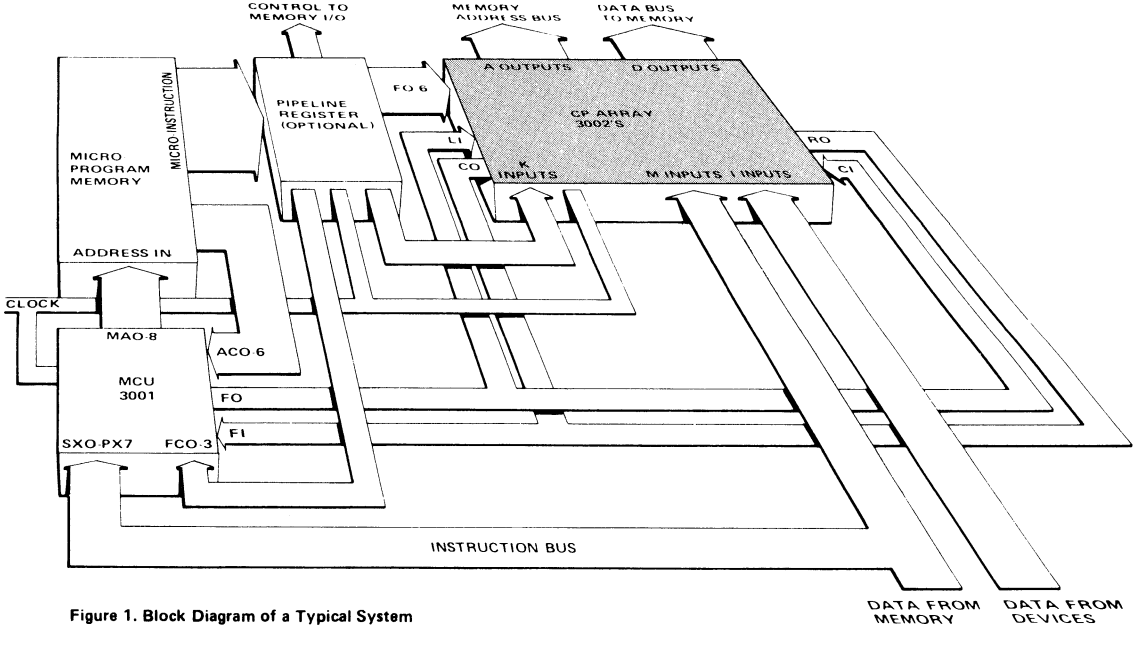


Figure 1. Block Diagram of a Typical System

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1, 2	I_0-I_1	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active LOW
3, 4	K_0-K_1	Mask Bus Inputs The mask bus inputs provide a separate input port for the microprogram memory, to allow mask or constant entry.	Active LOW
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the INTEL 3003 Look-Ahead Carry Generator.	
7	CO	Ripple Carry Output The ripple carry output is only disabled during shift right operations.	Active LOW Three-state
8	RO	Shift Right Output The shift right output is only enabled during shift right operations.	Active LOW Three-state
9	LI	Shift Right Input	Active LOW
10	CI	Carry Input	Active LOW
11	EA	Memory Address Enable Input When in the LOW state, the memory address enable input enables the memory address outputs (A_0-A_1).	Active LOW
12-13	A_0-A_1	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active LOW Three-state
14	GND	Ground	
15-17, 24-27,	F_0-F_6	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	
18	CLK	Clock Input	
19-20	D_0-D_1	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active LOW Three-state
21-22	M_0-M_1	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active LOW
23	ED	Memory Data Enable Input When in the LOW state, the memory data enable input enables the memory data outputs (D_0-D_1)	Active LOW
28	V_{CC}	+5 Volt Supply	

NOTE:
1. Active HIGH, unless otherwise specified.

LOGICAL DESCRIPTION

The CPE provides the arithmetic, logic and register functions of a 2-bit wide slice through a microprogrammed central processor. Data from external sources such as main memory, is brought into the CPE on one of the three separate input busses. Data being sent out of the CPE to external devices is carried on either of the two output busses. Within the CPE, data is stored in one of eleven scratchpad registers or in the accumulator. Data from the input busses, the registers, or the accumulator is available to the arithmetic/logic section (ALS) under the control of two internal multiplexers. Additional inputs and outputs are included for carry propagation, shifting, and micro-function selection. The complete logical organization of the CPE is shown below.

MICRO-FUNCTION BUS AND DECODER

The seven micro-function bus input lines of the CPE, designated F_0-F_6, are decoded internally to select the ALS function, generate the scratchpad address, and control the A and B multiplexers.

M-BUS AND I-BUS INPUTS

The M-bus inputs are arranged to bring data from an external main memory into the CPE. Data on the M-bus is multiplexed internally for input to the ALS.

The I-bus inputs are arranged to bring data from an external I/O system into the CPE. Data on the I-bus is also multiplexed internally, although independently of the M-bus, for input to the ALS Separation of the two busses permits a relatively lightly loaded memory bus even though a large number of I/O devices are connected to the I-bus. Alternatively, the I-bus may be wired to perform a multiple bit shift (e.g., a byte exchange) by connecting it to one of the output busses. In this case, I/O device data is gated externally onto the M-bus.

SCRATCHPAD

The scratchpad contains eleven registers designated R_0 through R_9 and T. The output of the scratchpad is multiplexed internally for input to ALS. The ALS output is returned for input into the scratchpad.

ACCUMULATOR AND D-BUS

An independent register called the accumulator (AC) is available for storing the result of an ALS operation. The output of the accumulator is multiplexed internally for input back to the ALS and is also available via a three-state output buffer on the D-bus outputs. Conventional usage of the D-bus is for data being sent to the external main memory or to external I/O devices.

A AND B MULTIPLEXERS

The A and B multiplexers select the two inputs to the ALS specified on the micro-function bus. Inputs to the A-multiplexer include the M-bus, the scratchpad, and the accumulator. The B-multiplexer selects either the I-bus, the accumulator, or the K-bus. The selected B-multiplexer input is always logically ANDed with the data on the K-bus (see below) to provide a flexible masking and bit testing capability.

ALS AND K-BUS

The ALS is capable of a variety of arithmetic and logic operations, including 2's complement addition, incrementing, and decrementing, plus logical AND, inclusive-OR, exclusive-NOR, and logical complement. The result of an ALS operation may be stored in the accumulator or one of the scratchpad registers. Separate left input and right output lines, designated LI and RO, are available for use in right shift operations. Carry input and carry output lines, designated CI and CO are provided for normal ripple carry propagation. CO and RO data are brought out via two alternately enabled tri-state buffers. In addition, standard look ahead carry outputs, designated X and Y, are available for full carry look ahead across any word length.

The ability of the K-bus to mask inputs to the ALS greatly increases the versatility of the CPE. During non-arithmetic operations in which carry propagation has no meaning, the carry circuits are used to perform a word-wise inclusive-OR of the bits, masked by the K-bus, from the register or bus selected by the function decoder. Thus, the CPE provides a flexible bit testing capability. The K-bus is also used during arithmetic operations to mask portions of the field being operated upon. An additional function of the K-bus is that of supplying constants to the CPE from the microprogram.

MEMORY ADDRESS REGISTER AND A-BUS

A separate ALS output is also available to the memory address register (MAR) and to the A-bus via a three-state output buffer. Conventional usage of the MAR and A-bus is for sending addresses to an external main memory. The MAR and A-bus may also be used to select an external device when executing I/O operations.

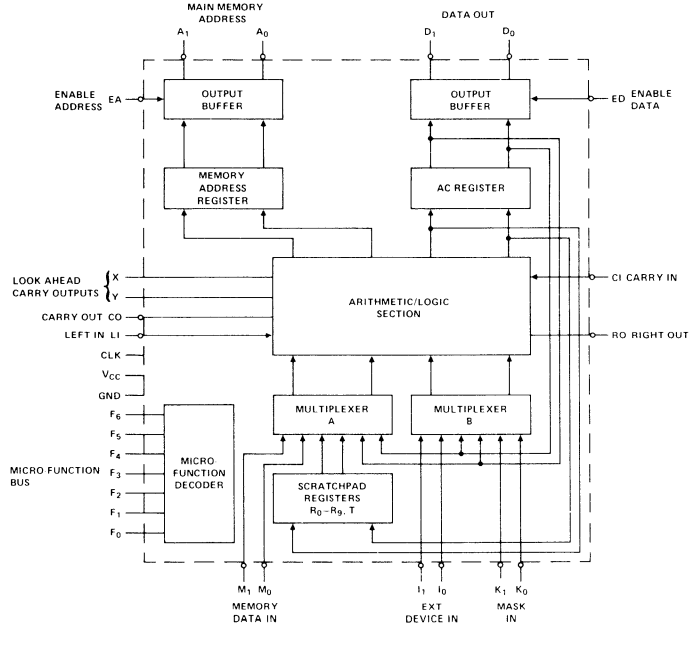


Figure 2. 3002 Block Diagram

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . -65°C to +160°C

All Output and Supply Voltages . . . . . -0.5V to +7V

All Input Voltages . . . . . -1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

		LIMITS				
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.0	V	I_C = -5 mA
I_F	Input Load Current:					
	F_0-F_6, CLK, K_0, K_1, EA, ED		-0.05	-0.25	mA	V_F = 0.45V
	I_0, I_1, M_0, M_1, LI		-0.85	-1.5	mA	
	CI		-2.3	-4.0	mA	
I_R	Input Leakage Current:					
	F_0-F_6, CLK, K_0, K_1, EA, ED			40	μA	V_R = 5.25V
	I_0, I_1, M_0, M_1, LI			60	μA	
	CI			180	μA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current(2)		145	190	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.3	0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (All Output Pins)	2.4	3.0		V	I_{OH} = -1 mA
I_{OS}	Short Circuit Output Current (All Output Pins)	-15	-25	-60	mA	V_{CC} = 5.0V
$I_{O(off)}$	Off State Output Current			-100	μA	V_O = 0.45V
	A_0, A_1, D_0, D_1, CO and RO			100	μA	V_O = 5.25V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage
(2) CLK input grounded, other inputs open.

A.C. CHARACTERISTICS AND WAVEFORMS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%

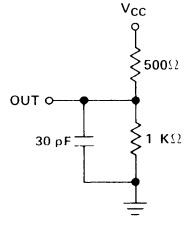
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT
t_{CY}	Clock Cycle Time (2)	100	70		ns
t_{WP}	Clock Pulse Width	33	20		ns
t_{FS}	Function Input Set-Up Time (F_0 through F_6)	60	40		ns
	Data Set-Up Time:				
t_{DS}	I_0, I_1, M_0, M_1, K_0, K_1	50	30		ns
t_{SS}	LI, CI	27	13		ns
	Data and Function Hold Time:				
t_{FH}	F_0 through F_6	5	-2		ns
t_{DH}	I_0, I_1, M_0, M_1, K_0, K_1	5	-4		ns
t_{SH}	LI, CI	15	2		ns
	Propagation Delay to X, Y, RO from:				
t_{XF}	Any Function Input		37	52	ns
t_{XD}	Any Data Input		29	42	ns
t_{XT}	Trailing Edge of CLK		40	60	ns
t_{XL}	Leading Edge of CLK	20			ns
	Propagation Delay to CO from:				
t_{CL}	Leading Edge of CLK	20			ns
t_{CT}	Trailing Edge of CLK		48	70	ns
t_{CF}	Any Function Input		43	65	ns
t_{CD}	Any Data Input		30	55	ns
t_{CC}	CI (Ripple Carry)		14	25	ns
	Propagation Delay to A_0, A_1, D_0, D_1 from:				
t_{DL}	Leading Edge of CLK	5	32	50	ns
t_{DE}	Enable Input ED, EA		12	25	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) $t_{CY} = t_{DS} + t_{DL}$.

TEST CONDITIONS:

Input pulse amplitude: 2.5 V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 10 mA and 30 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:



CAPACITANCE(2) T_A = 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V and T_A = 25°C.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C

Storage Temperature . . . . . −65°C to +160°C

All Input and Supply Voltages . . . . . −0.5V to +7V

All Input Voltages . . . . . −1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%.

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		−0.8	−1.2	V	I_C = −5 mA
I_F	Input Load Current:					
	F_0−F_6, CLK, K_0, K_1, EA, ED		−0.05	−0.25	mA	V_F = 0.45V
	I_0, I_1, M_0, M_1, LI		−0.85	−1.5	mA	
	CI		−2.3	−4.0	mA	
I_R	Input Leakage Current:					
	F_0−F_6, CLK, K_0, K_1, EA, ED			40	μA	V_R = 5.5V
	I_0, I_1, M_0, M_1, LI			100	μA	
	CI			250	μA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	
I_{CC}	Power Supply Current		145	210	mA	
V_{OL}	Output Low Voltage (All Output Pins)		0.3	0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (All Output Pins)	2.4	3.0		V	I_{OH} = −1 mA
I_{OS}	Short Circuit Output Current (All Output Pins)	−15	−25	−60	mA	V_{CC} = 5.0V
$I_{O(off)}$	Off State Output Current			−100	μA	V_O = 0.45V
	A_0, A_1, D_0, D_1, CO and RO			100	μA	V_O = 5.5V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage
(2) CLK input grounded, other inputs open.

A.C. CHARACTERISTICS AND WAVEFORMS

T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%.

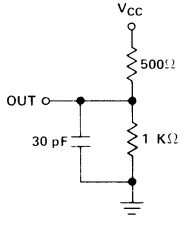
SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT
t_{CY}	Clock Cycle Time [2]	120	70		ns
t_{WP}	Clock Pulse Width	42	20		ns
t_{FS}	Function Input Set-Up Time (F_0 through F_6)	70	40		ns
	Data Set-Up Time:				
t_{DS}	I_0, I_1, M_0, M_1, K_0, K_1	60	30		ns
t_{SS}	LI, CI	30	13		ns
	Data and Function Hold Time:				
t_{FH}	F_0 through F_6	5	-2		ns
t_{DH}	I_0, I_1, M_0, M_1, K_0, K_1	5	-4		ns
t_{SH}	LI, CI	15	2		ns
	Propagation Delay to X, Y, RO from:				
t_{XF}	Any Function Input		37	65	ns
t_{XD}	Any Data Input		29	55	ns
t_{XT}	Trailing Edge of CLK		40	75	ns
t_{XL}	Leading Edge of CLK	22			ns
	Propagation Delay to CO from:				
t_{CL}	Leading Edge of CLK	22			ns
t_{CT}	Trailing Edge of CLK		48	85	ns
t_{CF}	Any Function Input		43	75	ns
t_{CD}	Any Data Input		30	65	ns
t_{CC}	CI (Ripple Carry)		14	30	ns
	Propagation Delay to A_0, A_1, D_0, D_1 from:				
t_{DL}	Leading Edge of CLK	5	32	60	ns
t_{DE}	Enable Input ED, EA		12	35	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) $t_{CY} = t_{DS} + t_{DL}$

TEST CONDITIONS:

Input pulse amplitude: 2.5 V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 10 mA and 30 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:

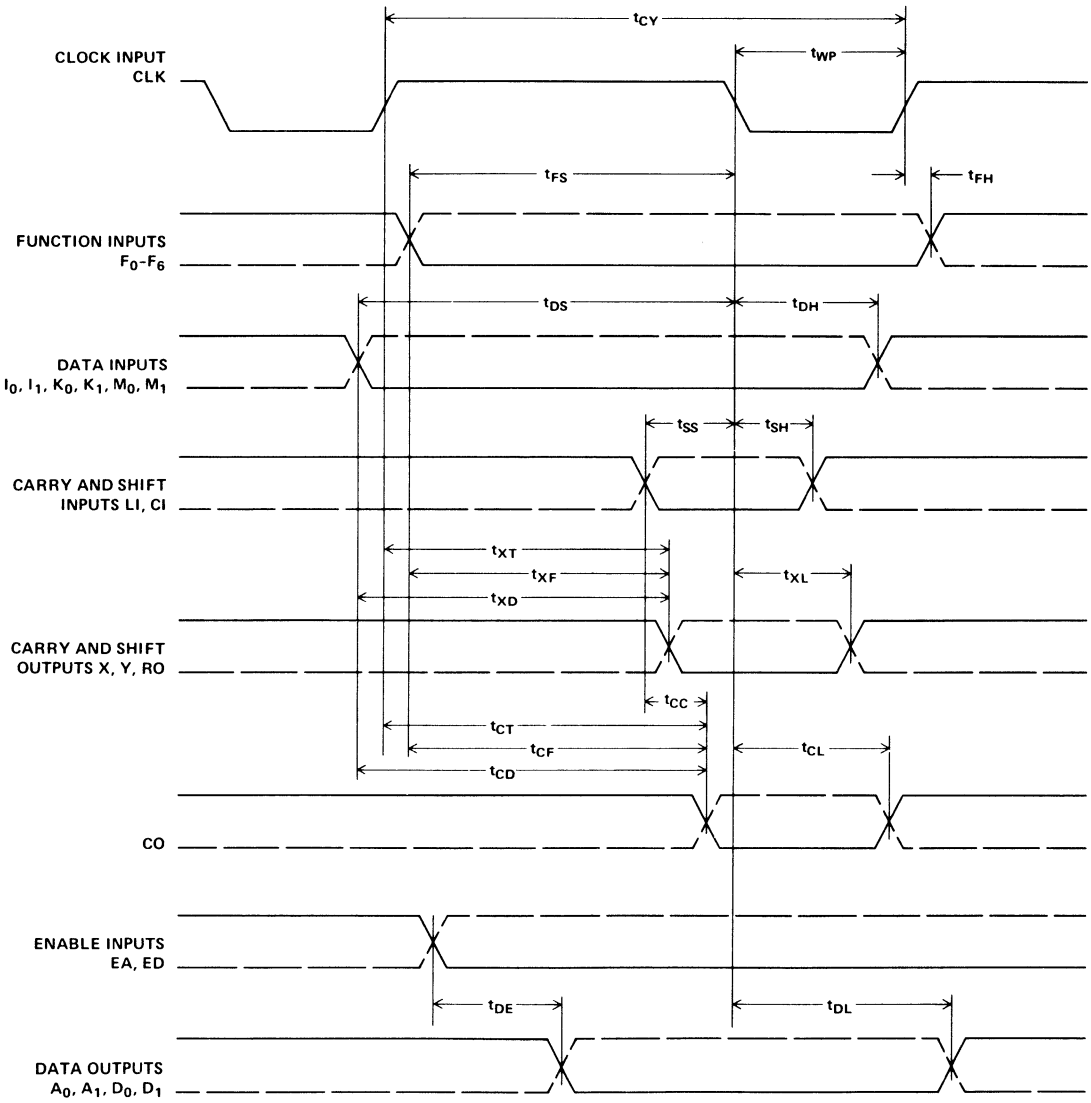


CAPACITANCE(2) T_A = 25°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		6	12	pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V and T_A = 25°C.

3002 WAVEFORMS



3003

LOOK-AHEAD CARRY GENERATOR

The INTEL® 3003 Look-Ahead Carry Generator (LCG) is a high speed circuit capable of anticipating a carry across a full 16-bit 3002 Central Processing Array. When used with a larger 3002 CP Array multiple 3003 carry generators provide high speed carry look-ahead capability for any word length.

The LCG accepts eight pairs of active high cascade inputs (X,Y) and an active low carry input and generates active low carries for up to eight groups of binary adders.

High Performance – 10 ns typical propagation delay

Compatible with INTEL 3001 MCU and 3002 CPE

DTL and TTL compatible

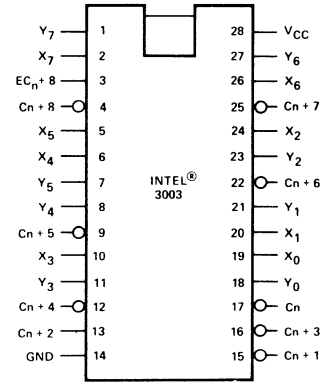
Full look-ahead across 8 adders

Low voltage diode input clamp

Expandable

28-pin DIP

PACKAGE CONFIGURATION



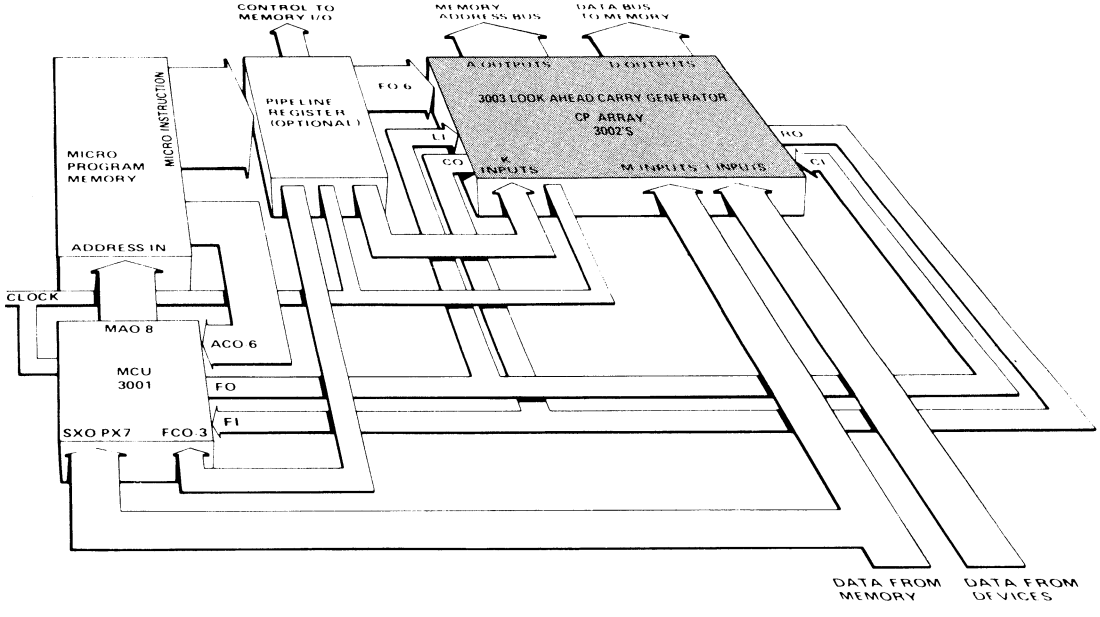
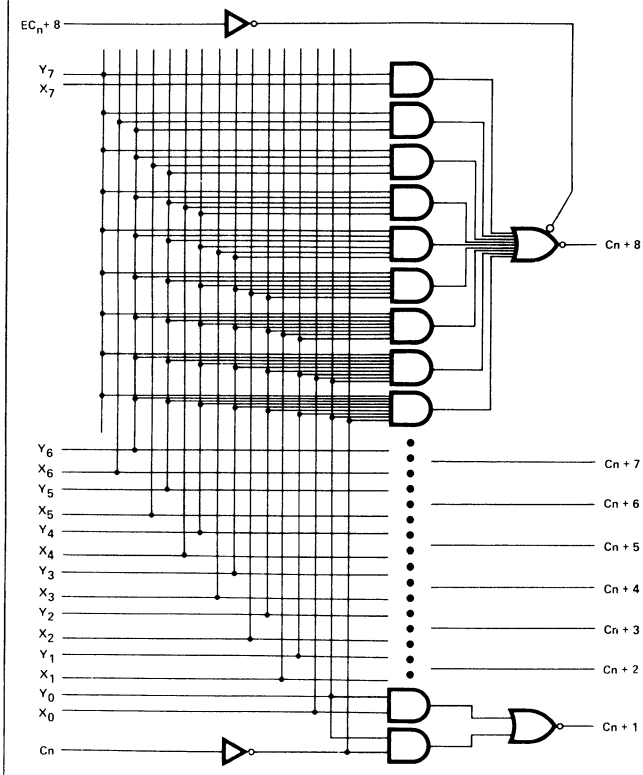


Diagram of a Typical System

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1,7,8,11 18,21,23 27	Y_0-Y_7	Standard carry look-ahead inputs	Active HIGH
2,5,6,10 19,20,24 26	X_0-X_7	Standard carry look-ahead inputs	Active HIGH
17	C_n	Carry input	Active LOW
4,9,12 13,15,16	C_{n+1}- C_{n+8}	Carry outputs	Active LOW
3	EC_{n+8}	C_{n+8} carry output enable	Active HIGH
28	V_{CC}	+5 volt supply	
14	GND	Ground	

LOGIC DIAGRAM



3003 LOGIC EQUATIONS

The 3003 Look-Ahead Generator is implemented in a compatible form for direct connection to the 3001 MCU and 3002 CPE. Logic equations for the 3003 are:

$$\overline{C_{n+1}} = Y_0X_0 + Y_0\overline{C}_n$$

$$\overline{C_{n+2}} = Y_1X_1 + Y_1Y_0X_0 + Y_1Y_0\overline{C}_n$$

$$\overline{C_{n+3}} = Y_2X_2 + Y_2Y_1X_1 + Y_2Y_1Y_0X_0 + Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_{n+4}} = Y_3X_3 + Y_3Y_2X_2 + Y_3Y_2Y_1X_1 + Y_3Y_2Y_1Y_0X_0 + Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_{n+5}} = Y_4X_4 + Y_4Y_3X_3 + Y_4Y_3Y_2X_2 + Y_4Y_3Y_2Y_1X_1 + Y_4Y_3Y_2Y_1Y_0X_0 + Y_4Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_{n+6}} = Y_5X_5 + Y_5Y_4X_4 + Y_5Y_4Y_3X_3 + Y_5Y_4Y_3Y_2X_2 + Y_5Y_4Y_3Y_2Y_1X_1 + Y_5Y_4Y_3Y_2Y_1Y_0X_0 + Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_{n+7}} = Y_6X_6 + Y_6Y_5X_5 + Y_6Y_5Y_4X_4 + Y_6Y_5Y_4Y_3X_3 + Y_6Y_5Y_4Y_3Y_2X_2 + Y_6Y_5Y_4Y_3Y_2Y_1X_1 + Y_6Y_5Y_4Y_3Y_2Y_1Y_0X_0 + Y_6Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n$$

$\overline{C_{n+8}}$ = High Impedance State when $EC_n + 8$ Low

$$\overline{C_{n+8}} = Y_7X_7 + Y_7Y_6X_6 + Y_7Y_6Y_5X_5 + Y_7Y_6Y_5Y_4X_4 + Y_7Y_6Y_5Y_4Y_3X_3 + Y_7Y_6Y_5Y_4Y_3Y_2X_2 + Y_7Y_6Y_5Y_4Y_3Y_2Y_1X_1 + Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0X_0 + Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n \text{ when } EC_n + 8 \text{ high}$$

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -55°C to +125°C

Storage Temperature . . . . . -65°C to +160°C

All Input and Supply Voltages . . . . . -0.5V to +7V

All Input Voltages . . . . . -1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%.

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.2	V	I_C = -5 mA
I_F	Input Load Current:					
	X_6, X_7, Cn, EC_{n+8}		-0.07	-0.25	mA	V_F = 0.45V
	Y_7, X_0-X_5,		-0.200	-0.500	mA	
	Y_o-Y_6		-0.6	-1.5	mA	
I_R	Input Leakage Current:					
	C_n and EC_n + 8			40	µA	V_{CC} = 5.25V, V_R = 5.5V
	All Other Inputs			100	µA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.1			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current		80	130	mA	All Y and EC_n + 8 high, All X and C_n low
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage (All Output Pins)	2.4	3		V	I_{OH} = -1 mA
I_{OS}	Short Circuit Output Current (All Output Pins)	-15	-40	-65	mA	V_{CC} = 5V
$I_{O(off)}$	Off-State Output Current (C_n + 8)			-100	µA	V_O = 0.45V
				+100	µA	V_O = 5.5V

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{CC} = +5.0V ±10%

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT
t_{XC}	X, Y to Outputs	3	10	25	ns
t_{CC}	Carry In to Outputs		13	40	ns
t_{EN}	Enable Time, C_n + 8		20	50	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.

MILITARY TEMP.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . –65°C to +160°C

All Output and Supply Voltages . . . . . –0.5V to +7V

All Input Voltages . . . . . –1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to +70°C V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.0	V	I_C = -5 mA
I_F	Input Load Current:					
	X_6,X_7Cn,EC_n + 8		-0.07	-0.25	mA	V_F = 0.45V
	Y_7,X_0-X_5,		-0.200	-0.500	mA	
	Y_0-Y_6		-0.6	-1.5	mA	
I_R	Input Leakage Current:					
	C_n and EC_n + 8			40	µA	V_R = 5.25V
	All Other Inputs			100	µA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current		80	130	mA	All Y and EC_n + 8 high, All X and C_n low
V_{OL}	Output Low Voltage (All Output Pins)		0.35	0.45	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage (All Output Pins)	2.4	3		V	I_{OH} = -1 mA
I_{OS}	Short Circuit Output Current (All Output Pins)	-15	-40	-65	mA	V_{CC} = 5V
$I_{O(off)}$	Off-State Output Current (C_n + 8)			-100	µA	V_O = 0.45V
				+100	µA	V_O = 5.25V

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.

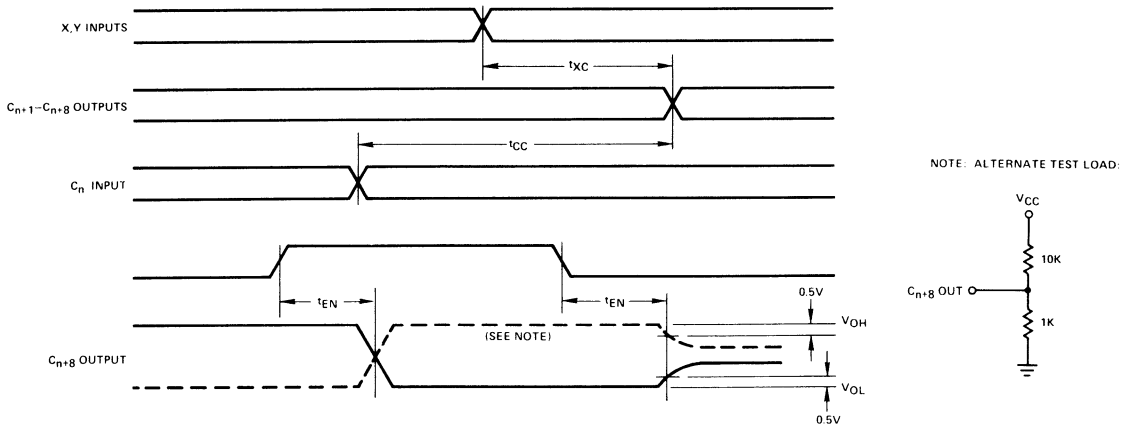
A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT
t_{XC}	X, Y to Outputs	3	10	20	ns
t_{CC}	Carry In to Outputs		13	30	ns
t_{EN}	Enable Time, C_n + 8		20	40	ns

NOTE:
(1) Typical values are for T_A = 25°C and nominal supply voltage.

WAVEFORMS



CAPACITANCE[2] T_A = 25°C

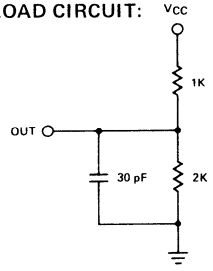
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance	All inputs		12	20	pF
C_{OUT}	Output Capacitance	C_n + 8		7	12	pF

NOTE:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 5.0V, V_{CC} = 5.0V and T_A = 25°C.

TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 30 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:



3212

MULTI-MODE LATCH BUFFER

The INTEL® 3212 Multi-Mode Latch Buffer is a versatile 8-bit latch with three-state output buffers and built-in device select logic. It also contains an independent service request flip-flop for the generation of central processor interrupts. Because of its multi-mode capabilities, one or more 3212's can be used to implement many types of interface and support systems for Series 3000 computing elements including:

- Simple data latches
- Gated data buffers
- Multiplexers
- Bi-directional bus drivers
- Interrupting input/output ports

High Performance – 50 ns Write Cycle Time

Low Input Load Current – 250 μA Maximum

Three-State Fully Buffered Outputs

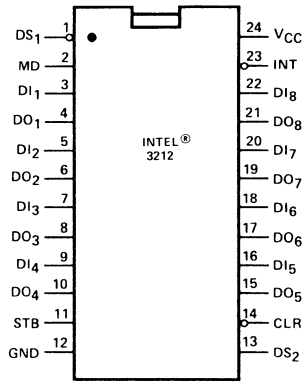
High Output Drive Capability

Independent Service Request Flip-Flop

Asynchronous Data Latch Clear

24 Pin DIP

PACKAGE CONFIGURATION



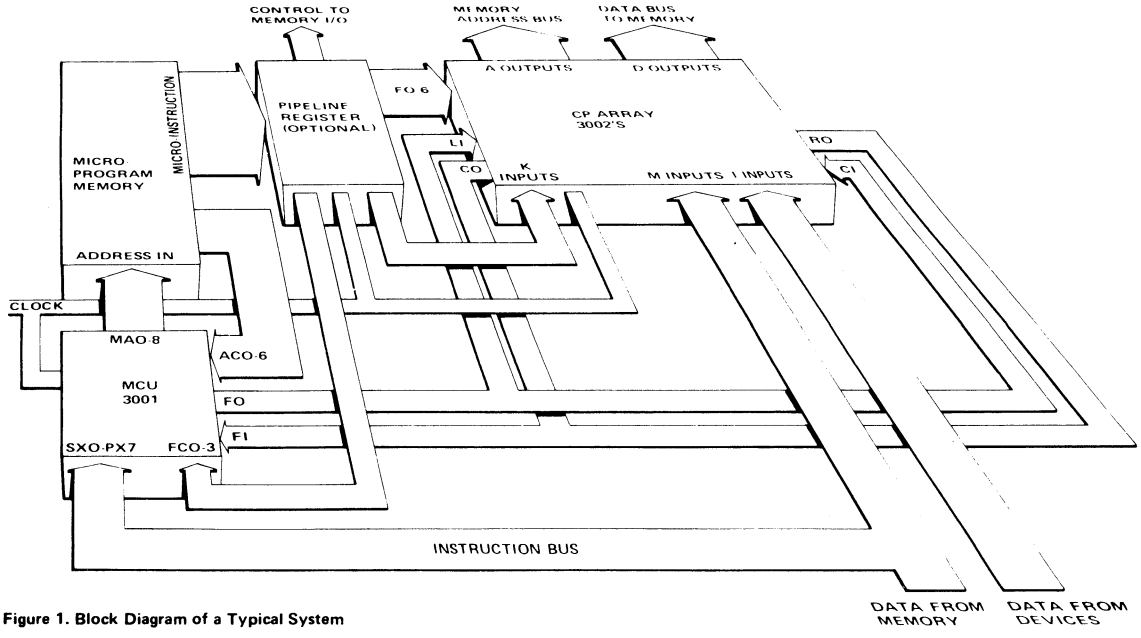


Figure 1. Block Diagram of a Typical System

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1	DS_1	Device Select Input 1	active LOW
2	MD	Mode Input When MD is high (output mode) the output buffers are enabled and the write signal to the data latches is obtained from the device select logic. When MD is low (input mode) the output buffer state is determined by the device select logic and the write signal is obtained from the strobe (STB) input.	
3, 5, 7, 9, 16, 18, 20, 22	DI_1–DI_8	Data Inputs The data inputs are connected to the D-inputs of the data latches.	
4, 6, 8, 10, 15, 17, 19, 21	DO_1–DO_8	Data Outputs The data outputs are the buffered outputs of the eight data latches.	three-state
11	STB	Strobe Input When MD is in the LOW state, the STB input provides the clock input to the data latch.	
12	GND	Ground	
13	DS_2	Device Select Input 2 When DS_1 is low and DS_2 is high, the device is selected.	
14	CLR	Clear	active LOW
23	INT	Interrupt Output The interrupt output will be active LOW (interrupting state) when either the service request flip-flop is low or the device is selected.	active LOW

NOTE:
(1) Active HIGH, unless otherwise specified.

FUNCTIONAL DESCRIPTION

The 3212 contains eight D-type data latches, eight three-state output buffers, a separate D-type service request flip-flop, and a flexible device select/mode control section.

DATA LATCHES

The Q-output of each data latch will follow the data on its corresponding date input line (DI_1–DI_8) while its clock input is high. Data will be latched when the internal write line WR is brought low. The output of each data latch is connected to a three-state, non-inverting output buffer. The internal enable line EN is bussed to each buffer. When the EN is high, the buffers are enabled and the data in each latch is available on its corresponding data output line (DO_0–DO_8).

DEVICE SELECT LOGIC

Two input lines DS_1 and DS_2 are provided for device selection. When DS_1 is low and DS_2 is high, the 3212 is selected.

MODE CONTROL SECTION

The 3212 may be operated in two modes. When the mode input line MD is low, the device is in the input mode. In this mode, the output buffers are enabled whenever the 3212 is selected; the internal WR line follows the STB input line.

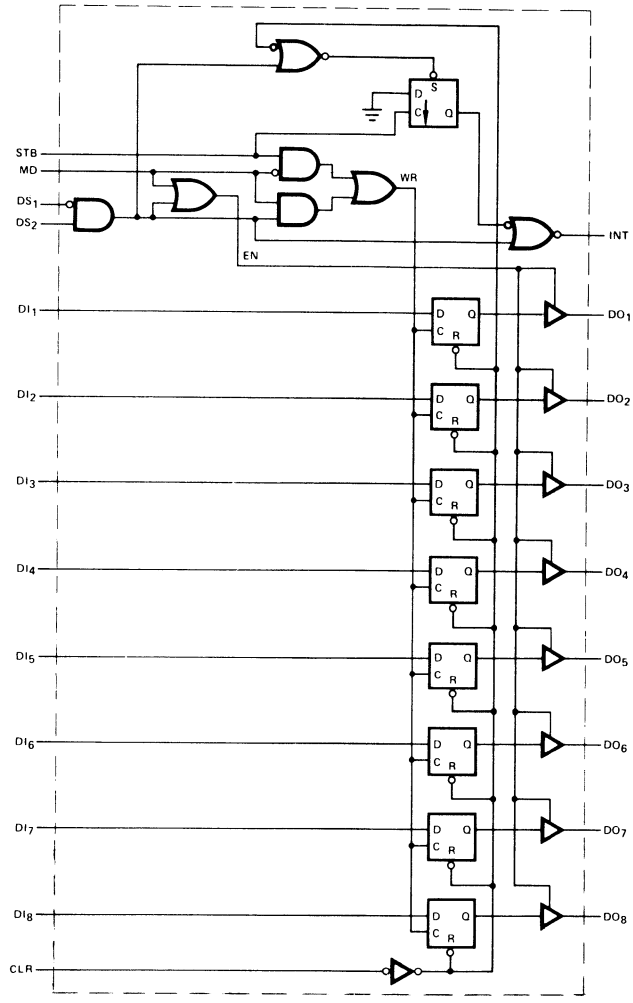
When MD is high, the device is in the output mode and, as a result, the output buffers are enabled. In this mode, the write signal for the data latch is obtained from the device select logic.

SERVICE REQUEST FLIP-FLOP AND STROBE

The service request flip-flop SR is used to generate and control central processor interrupt signals. For system reset, the SR flip-flop is placed in the non-interrupting state (i.e., SR is set) by bringing the CLR line low. This simultaneously clears (resets) the 8-bit data latch.

The Q output of the SR flip-flop is logically ORed with the output of device select logic and then inverted to provide the interrupt output INT. The 3212 is considered to be in the interrupting state when the INT output is low. This allows direct connection to the active LOW priority request inputs of the INTEL®3214 Interrupt Control Unit.

When operated in the input mode (i.e., MD low) the strobe input STB is used to synchronously write data into the data latch and place the SR flip-flop in the interrupting (reset) state. The interrupt is removed by the central processor when the interrupting 3212 is selected.



M3212 Logic Diagram

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +160°C
All Output and Supply Voltages . . . . . –0.5V to +7V
All Input Voltages . . . . . –1.0V to +5.5V
Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to +75°C V_{CC} = +5V ±5%

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_F	Input Load Current STB, DS_2, CLR, DI_1–DI_8 Inputs			–.25	mA	V_F = .45V
I_F	Input Load Current MD Input			–.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			–1.0	mA	V_F = .45V
I_R	Input Leakage Current STB, DS, CLR, DI_1–DI_8 Inputs			10	µA	$V_R \leqslant V_{CC}$
I_R	Input Leakage Current MD Input			30	µA	$V_R \leqslant V_{CC}$
I_R	Input Leakage Current DS_1 Input			40	µA	$V_R \leqslant V_{CC}$
V_C	Input Forward Voltage Clamp			–1	V	I_C = –5 mA
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 15 mA
V_{OH}	Output "High" Voltage	3.65	4.0		V	I_{OH} = –1 mA
I_{SC}	Short Circuit Output Current	–15		–75	mA	V_{CC} = 5.0V
$\|I_O\|$	Output Leakage Current High Impedance State			20	µA	V_O = .45V/5.25V
I_{CC}	Power Supply Current		90	130	mA	

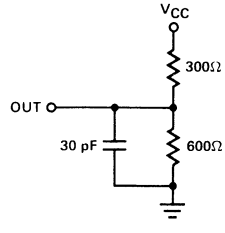
A.C. CHARACTERISTICS $T_A = 0°C$ to $75°C$, $V_{CC} = +5.0V \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	
t_{PW}	Pulse Width	25			ns	
t_{PD}	Data To Output Delay			30	ns	
t_{WE}	Write Enable To Output Delay			40	ns	
t_{SET}	Data Setup Time	15			ns	
t_H	Data Hold Time	20			ns	
t_R	Reset To Output Delay			40	ns	
t_S	Set To Output Delay			30	ns	
t_E	Output Enable Time			45	ns	C_L = 30 pf
t_C	Clear To Output Display			45	ns	

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 15 mA and 30 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:



3000 SERIES

CAPACITANCE[1]

Symbol	Test	LIMITS Min.	Typ.	Max.	Units
C_{IN}	DS_1, MD Input Capacitance		9	12	pf
C_{IN}	DS_2, CLR, STB, DI_1–DI_8 Input Capacitance		5	9	pf
C_{OUT}	DO_1–DO_8 Output Capacitance		8	12	pf

NOTE:
(1) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V and $T_A = 25°C$.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . –55°C to +125°C

Storage Temperature . . . . . –65°C to +160°C

All Input and Supply Voltages . . . . . –0.5V to +7V

All Input Voltages . . . . . –1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_F	Input Load Current STB, DS_2, CLR, DI_1–DI_8 Inputs			–.25	mA	V_F = .45V
I_F	Input Load Current MD Input			–.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			–1.0	mA	V_F = .45V
I_R	Input Leakage Current STB, DS, CLR, DI_1–DI_8 Inputs			10	µA	$V_R \leqslant V_{CC}$
I_R	Input Leakage Current MD Input			30	µA	$V_R \leqslant V_{CC}$
I_R	Input Leakage Current DS_1 Input			40	µA	$V_R \leqslant V_{CC}$
V_C	Input Forward Voltage Clamp			1.2	V	I_C = –5 mA
V_{IL}	Input "Low" Voltage			.80	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 10 mA
V_{OH}	Output "High" Voltage	3.5	4.0		V	I_{OH} = .5 mA
I_{SC}	Short Circuit Output Current	–15		–75	mA	V_{CC} = 5.0V
$\|I_O\|$	Output Leakage Current High Impedance State			20	µA	V_O = .45V/5.5V
I_{CC}	Power Supply Current		90	145	mA	

MILITARY TEMP.

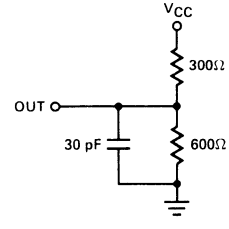
A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min.	Typ.	Max.	Unit	
t_{PW}	Pulse Width	40			ns	
t_{PD}	Data To Output Delay			30	ns	
t_{WE}	Write Enable To Output Delay			50	ns	
t_{SET}	Data Setup Time	20			ns	
t_H	Data Hold Time	30			ns	
t_R	Reset To Output Delay			55	ns	
t_S	Set To Output Delay			35	ns	
t_E	Output Enable Time			50	ns	C_L = 30 pf
t_C	Clear To Output Display			55	ns	

TEST CONDITIONS:

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5 ns between 1 volt and 2 volts.
Output load of 15 mA and 30 pF.
Speed measurements are taken at the 1.5 volt level.

TEST LOAD CIRCUIT:



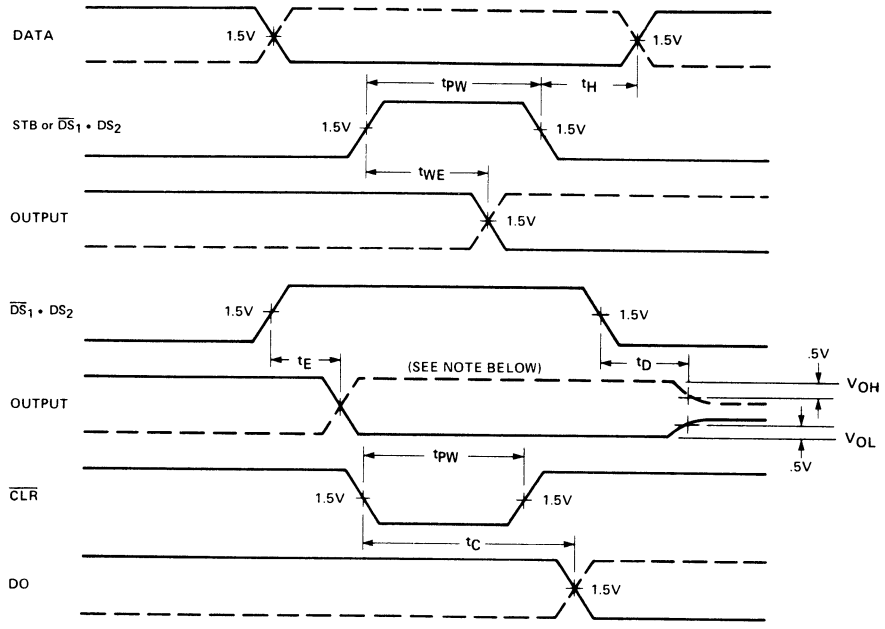
3000 SERIES MPU

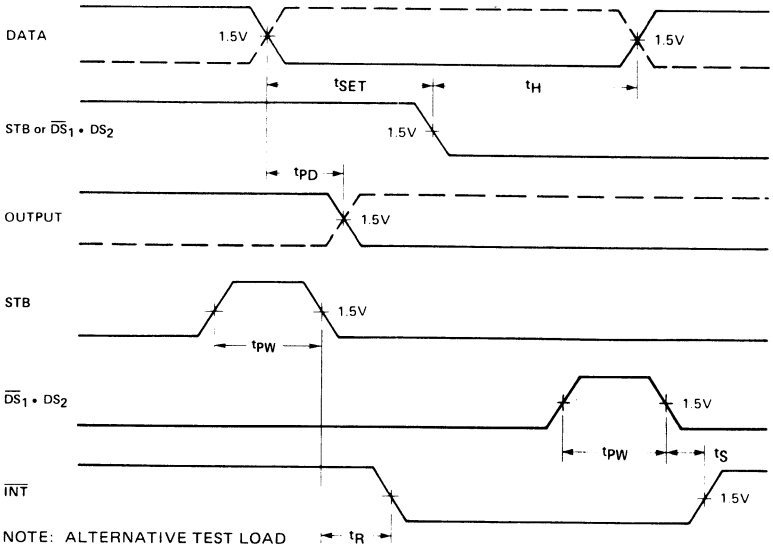
CAPACITANCE[1]

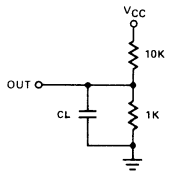
Symbol	Test	LIMITS Min.	Typ.	Max.	Units
C_{IN}	DS_1, MD Input Capacitance		9	12	pf
C_{IN}	DS_2, CLR, STB, DI_1–DI_8 Input Capacitance		5	9	pf
C_{OUT}	DO_1–DO_8 Output Capacitance		8	12	pf

NOTE:
(1) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V and T_A = 25°C.

WAVEFORMS


DATA
1.5V
1.5V
tPW
tH
STB or $\overline{DS}_1 \cdot DS_2$
1.5V
1.5V
tWE
OUTPUT
1.5V
$\overline{DS}_1 \cdot DS_2$
1.5V
1.5V
tE
(SEE NOTE BELOW)
tD
.5V
VOH
OUTPUT
VOL
.5V
tPW
$\overline{CLR}$
1.5V
1.5V
tC
DO
1.5V


DATA
1.5V
1.5V
tSET
tH
STB or $\overline{DS}_1 \cdot DS_2$
1.5V
tPD
OUTPUT
1.5V
STB
1.5V
tPW
$\overline{DS}_1 \cdot DS_2$
1.5V
tPW
tS
$\overline{INT}$
1.5V
NOTE: ALTERNATIVE TEST LOAD
tR


VCC
10K
OUT
CL
1K

3214

INTERRUPT CONTROL UNIT

The Intel®3214 Interrupt Control Unit (ICU) implements multi-level interrupt capability for systems designed with Series 3000 computing elements.

The ICU accepts an asynchronous interrupt strobe from the 3001 Microprogram Control Unit or a bit in microprogram memory and generates a synchronous interrupt acknowledge and an interrupt vector which may be directed to the MCU or CP Array to uniquely identify the interrupt source.

The ICU is fully expandable in 8-level increments and provides the following system capabilities:

- Eight unique priority levels per ICU
- Automatic Priority Determination
- Programmable Status
- N-level expansion capability
- Automatic interrupt vector generation

High Performance – 80 ns Cycle Time

Compatible with Intel 3001 MCU and 3002 CPE

8-Bit Priority Interrupt Request Latch

4-Bit Priority Status Latch

3-Bit Priority Encoder with Open Collector Outputs

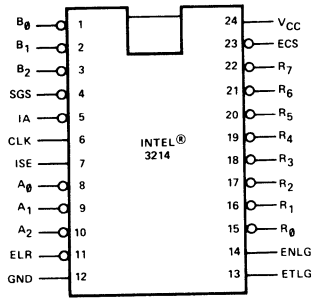
DTL and TTL Compatible

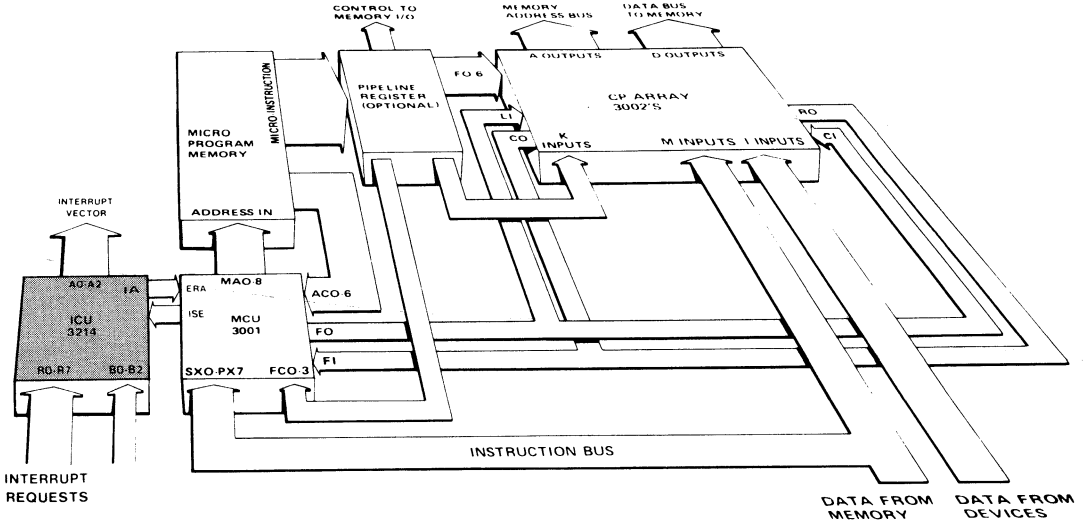
8-Level Priority Comparator

Fully Expandable

24-Pin DIP

PACKAGE CONFIGURATION





3000 SERIES MPU

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE[1]
1–3	B_0–B_2	Current Status Inputs The Current Status inputs carry the binary value modulo 8 of the current priority level to the current status latch.	Active LOW
4	SGS	Status Group Select Input The Status Group Select input informs the ICU that the current priority level does belong to the group level assigned to the ICU.	Active LOW
5	IA	Interrupt Acknowledge The Interrupt Acknowledge Output will only be active from the ICU (multi-ICU system) which has received a priority request at a level superior to the current status. It signals the controlled device (usually the processor) and the other ICUs OR-tied on the Interrupt Acknowledge line that an interrupt request has been recognized. The IA signal also sets the Interrupt Disable flip-flop (it overrides the clear function of the ECS input).	Active LOW Open-Collector Output
6	CLK	Clock Input The Clock input is used to synchronize the interrupt acknowledge with the operation of the device which it controls.	
7	ISE	Interrupt Strobe Enable Input The Interrupt Strobe Enable input informs the ICU that it is authorized to enter the interrupt mode.	
8–10	A_0–A_2	Request Level Outputs When valid, the Request Level outputs carry the binary value (modulo 8) of the highest priority request present at the priority request inputs or stored in the priority request latch. The request level outputs can become active only with the ICU which has received the highest priority request with a level superior to the current status.	Active LOW Open-Collector
11	ELR	Enable Level Read Input When active, the Enable Level Read input enables the Request Level output buffers (A_0–A_2).	Active LOW
12	GND	Ground	
13	ETLG	Enable This Level Group Input The Enable This Level Group input allows a higher priority ICU in multi-ICU systems to inhibit interrupts within the next lower priority ICU (and all the following ICUs).	
14	ENLG	Enable Next Level Group Output The Enable Next Level Group output allows the ICU to inhibit interrupts within the lower priority ICU in a multi-ICU system.	
15–22	R_0–R_7	Priority Interrupt Request Inputs The Priority Interrupt Request inputs are the inputs of the priority Interrupt Request Latch. The lowest priority level interrupt request signal is attached to R_0 and the highest is attached to R_7.	Active LOW
23	ECS	Enable Current Status Input The Enable Current Status input controls the current status latch and the clear function of the Interrupt Inhibit flip-flop.	Active LOW
24	V_{CC}	+5 Volt Supply	

NOTE:
(1) Active HIGH, unless otherwise noted.

FUNCTIONAL AND LOGICAL DESCRIPTION

The ICU adds interrupt capability to suitably microprogrammed processors or controllers. One or more of these units allows external signals called interrupt requests to cause the processor/controller to suspend execution of the active process, save its status, and initiate execution of a new task as requested by the interrupt signal.

It is customary to strobe the ICU at the end of each instruction execution. At that time, if an interrupt request is acknowledged by the ICU, the MCU is forced to follow the interrupt microprogram sequence.

Figure 1 shows the block diagram of the ICU. Interrupt requests pass through the interrupt request latch and priority encoder to the magnitude comparator. The output of the priority encoder is the binary equivalent of the highest active priority request. At the comparator, this value is compared with the Current Status (currently active priority level) contained in the current status latch. A request, if acknowledged at interrupt strobe time, will cause the interrupt flip-flop to enter the "interrupt active" state for one microinstruction cycle. This action causes the interrupt acknowledge (IA) signal to go low and sets the interrupt disable flip-flop.

The IA signal constitutes the interrupt command to the processor. It can directly force entry into the interrupt service routine as demonstrated in the appendix. As part of this routine, the microprogram normally reads the requesting level via the request level output bus. This information which is saved in the request latch can be enabled onto one of the processor input data buses using the enable level read input. Once the interrupt handler has determined the requesting level, it normally writes this level back into the current status register of the ICU. This action resets the interrupt disable flip-flop and acts to block any further request at this level or lower levels.

Entry into a macro level interrupt service routine may be vectored using the request level information to generate a subroutine address which corresponds to the level. Exit from such a macroprogram should normally restore the prior status in the current status latch.

The Enable This Level Group (ETLG) input and the Enable Next Level Group (ENLG) output can be used in a daisy chain fashion, as each ICU is capable of inhibiting interrupts from all of the following ICUs in a multiple ICU configuration.

The interrupt acknowledge flip-flop is set to the active LOW state on the rising edge of the clock when the following conditions are met:

- An active request level (R_0–R_7) is greater than the current status B_0–B_2
- The interrupt mode (ISE) is active
- ETLG is enabled
- The interrupt disable flip-flop is reset

When active, the IA signal asynchronously sets the disable flip-flop and holds the requests in the request latch until new current status information (B_0–B_2, SGS) is enabled (ECS) into the current status latch. The disable flip-flop is reset at the completion of this load operation.

During this process, ENLG will be enabled only if the following conditions are met:

- ETLG is enabled
- The current status (SGS) does not belong to this level group
- There is no active request at this level

The request level outputs A_0–A_2 and the IA output are open-collector to permit bussing of these lines in multi-ICU configuration.

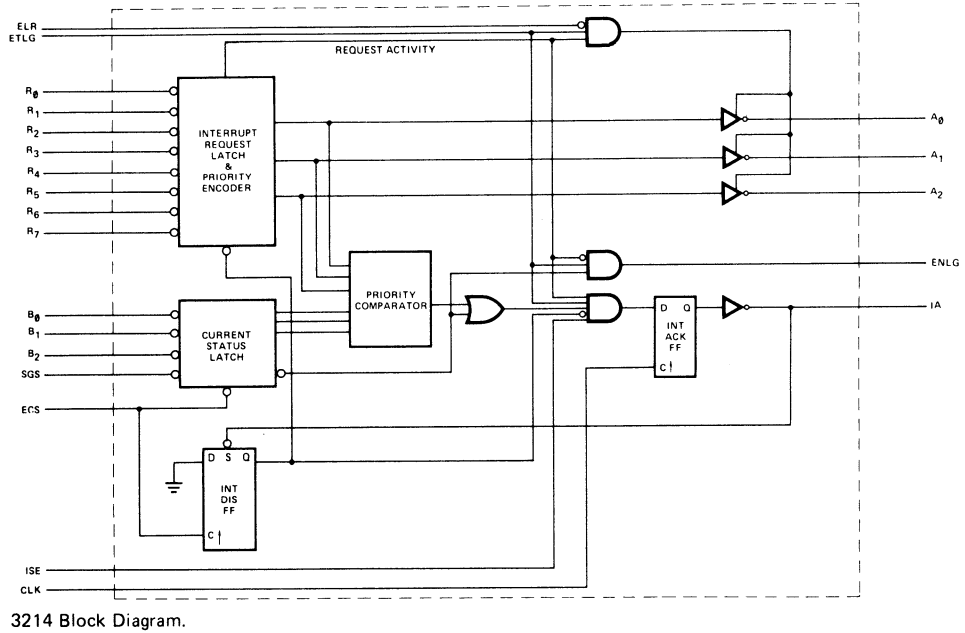


Figure 1. 3214 Block Diagram.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias

Ceramic . . . . . –65°C to +75°C

Plastic . . . . . 0°C to +75°C

Storage Temperature . . . . . –65°C to +160°C

All Output and Supply Voltages. . . . . –0.5V to +7V

All Input Voltages . . . . . –1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP(1)	LIMITS MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (all inputs)				-1.0	V	I_C = −5 mA
I_F	Input Forward Current:	ETLG input		-.15	-0.5	mA	V_F = 0.45V
		all other inputs		-.08	-0.25	mA	
I_R	Input Reverse Current:	ETLG input			80	µA	V_R = 5.25V
		all other inputs			40	µA	
V_{IL}	Input LOW Voltage:	all inputs			0.8	V	V_{CC} = 5.0V
V_{IH}	Input HIGH Voltage:	all inputs	2.0			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current(2)			90	130	mA	
V_{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I_{OL} = 15 mA
V_{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I_{OH} = -1 mA
I_{OS}	Short Circuit Output Current:	ENLG output	-20	-35	-55	mA	V_{CC} = 5.0V
I_{CEX}	Output Leakage Current:	IA and A_0–A_2 outputs			100	µA	V_{CEX} = 5.25V

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) B_0-B_2, SGS, CLK, R_0-R_4 grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS

T_A = 0°C to +75°C, V_{CC} = +5V ± 5%

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP(1)	LIMITS MAX	UNIT
t_{CY}	CLK Cycle Time	80			ns
t_{PW}	CLK, ECS, IA Pulse Width	25	15		ns
	Interrupt Flip-Flop Next State Determination:				
t_{ISS}	ISE Set-Up Time to CLK	16	12		ns
t_{ISH}	ISE Hold Time After CLK	20	10		ns
t_{ETCS}[2]	ETLG Set-Up Time to CLK	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After CLK	20	10		ns
t_{ECCS}[3]	ECS Set-Up Time to CLK (to clear interrupt inhibit prior to CLK)	80	25		ns
t_{ECCH}[3]	ECS Hold Time After CLK (to hold interrupt inhibit)	0			ns
t_{ECRS}[3]	ECS Set-Up Time to CLK (to enable new requests through the request latch)	110	70		ns
t_{ECRH}[3]	ECS Hold Time After CLK (to hold requests in request latch)	0			
t_{ECSS}[2]	ECS Set-Up Time to CLK (to enable new status through the status latch)	75	70		ns
t_{ECSH}[2]	ECS Hold Time After CLK (to hold status in status latch)	0			ns
t_{DCS}[2]	SGS and $B_Ø$-B_2 Set-Up Time to CLK (current status latch enabled)	70	50		ns
t_{DCH}[2]	SGS and $B_Ø$-B_2 Hold Time After CLK (current status latch enabled)	0			ns
t_{RCS}[3]	$R_Ø$-R_7 Set-Up Time to CLK (request latch enabled)	90	55		ns
t_{RCH}[3]	$R_Ø$-R_7 Hold Time After CLK (request latch enabled)	0			ns
t_{ICS}	IA Set-Up Time to CLK (to set interrupt inhibit F.F. before CLK)	55	35		ns
t_{CI}	CLK to IA Propagation Delay		15	25	ns
	Contents of Request Latch and Request Level Output Status Determination:				
t_{RIS}[4]	$R_Ø$-R_7 Set-Up Time to IA	10	0		ns
t_{RIH}[4]	$R_Ø$-R_7 Hold Time After IA	35	20		ns
t_{RA}	$R_Ø$-R_7 to $A_Ø$-A_2 Propagation Delay (request latch enabled)		80	100	ns
t_{ELA}	ELR to $A_Ø$-A_2 Propagation Delay		40	55	ns
t_{ECA}	ECS to $A_Ø$-A_2 Propagation Delay (to enable new requests through request latch)		100	120	ns
t_{ETA}	ETLG to $A_Ø$-A_2 Propagation Delay		35	70	ns

A.C. CHARACTERISTICS (CON'T)

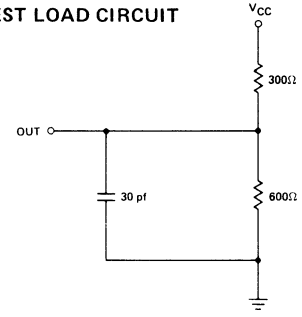
SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
	Contents of Current Priority Status Latch Determination:				
t_{DECS}[4]	SGS and $B_\emptyset$-B_2 Set-Up Time to ECS	15	10		ns
t_{DECH}[4]	SGS and $B_\emptyset$-B_2 Hold Time After ECS	15	10		ns
	Enable Next Level Group Determination:				
t_{REN}	$R_\emptyset$-R_7 to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	25	ns
t_{ECRN}	ECS to ENLG Propagation Delay (enabling new request through the request latch)		85	90	ns
t_{ECSN}	ECS to ENLG Propagation Delay (enabling new SGS through status latch)		35	55	ns

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) Required for proper operation if ISE is enabled during next clock pulse.
(3) These times are not required for proper operation but for desired change in interrupt flip-flop.
(4) Required for new request or status to be properly loaded.
(5) $t_{CY} = t_{ICS} + t_{CI}$

TEST CONDITIONS:

Input pulse amplitude: 2.5 volts.
Input rise and fall times: 5 ns between 1 and 2 volts.
Output loading of 15 mA and 30 pf.
Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT



CAPACITANCE(5)

T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pf
C_{OUT}	Output Capacitance		7	12	pf

TEST CONDITIONS:
V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C, f = 1 MHz

NOTE:
(5) This parameter is periodically sampled and not 100% tested.

MILITARY TEMP

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias

CerDip . . . . . –55°C to +125°C

Storage Temperature . . . . . –65°C to +160°C

All Output and Supply Voltages . . . . . –0.5V to +7V

All Input Voltages . . . . . –1.0V to +5.5V

Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = –55°C to +125°C; V_{CC} = 5.0V ± 10%

SYMBOL	PARAMETER		LIMITS MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (all inputs)				-1.2	V	I_C = –5 mA
I_F	Input Forward Current:	ETLG input		-.15	-0.5	mA	V_F = 0.45V
		all other inputs		-.08	-0.25	mA	
I_R	Input Reverse Current:	ETLG input			80	μA	V_R = 5.5V
		all other inputs			40	μA	
V_{IL}	Input LOW Voltage:	all inputs			0.8	V	V_{CC} = 5.0V
V_{IH}	Input HIGH Voltage:	all inputs	2.0			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current(2)			90	130	mA	
V_{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I_{OL} = 10 mA
V_{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I_{OH} = -1 mA
I_{OS}	Short Circuit Output Current:	ENLG output	-15	-35	-55	mA	V_{CC} = 5.0V
I_{CEX}	Output Leakage Current:	IA and A_0-A_3 outputs			100	μA	V_{CEX} = 5.5V

3000 SERIES

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) B_0-B_2, SGS, CLK, R_0-R_4 grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS

T_A = -55°C to +125°C; V_{CC} = 5.0V ± 10%

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP(1)	LIMITS MAX	UNIT
t_{CY}	CLK Cycle Time(5)	85			ns
t_{PW}	CLK, ECS, IA Pulse Width	25	15		ns
	Interrupt Flip-Flop Next State Determination:				
t_{ISS}	ISE Set-Up Time to CLK	16	12		ns
t_{ISH}	ISE Hold Time After CLK	20	10		ns
t_{ETCS}[2]	ETLG Set-Up Time to CLK	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After CLK	20	10		ns
t_{ECCS}[3]	ECS Set-Up Time to CLK (to clear interrupt inhibit prior to CLK)	85	25		ns
t_{ECCH}[3]	ECS Hold Time After CLK (to hold interrupt inhibit)	0			ns
t_{ECRS}[3]	ECS Set-Up Time to CLK (to enable new requests through the request latch)	110	70		ns
t_{ECRH}[3]	ECS Hold Time After CLK (to hold requests in request latch)	0			
t_{ECSS}[2]	ECS Set-Up Time to CLK (to enable new status through the status latch)	85	70		ns
t_{ECSH}[2]	ECS Hold Time After CLK (to hold status in status latch)	0			ns
t_{DCS}[2]	SGS and $B_\emptyset$-B_2 Set-Up Time to CLK (current status latch enabled)	90	50		ns
t_{DCH}[2]	SGS and $B_\emptyset$-B_2 Hold Time After CLK (current status latch enabled)	0			ns
t_{RCS}[3]	$R_\emptyset$-R_7 Set-Up Time to CLK (request latch enabled)	100	55		ns
t_{RCH}[3]	$R_\emptyset$-R_7 Hold Time After CLK (request latch enabled)	0			ns
t_{ICS}	IA Set-Up Time to CLK (to set interrupt inhibit F.F. before CLK)	55	35		ns
t_{CI}	CLK to IA Propagation Delay		15	30	ns
	Contents of Request Latch and Request Level Output Status Determination:				
t_{RIS}[4]	$R_\emptyset$-R_7 Set-Up Time to IA	10	0		ns
t_{RIH}[4]	$R_\emptyset$-R_7 Hold Time After IA	35	20		ns
t_{RA}	$R_\emptyset$-R_7 to $A_\emptyset$-A_2 Propagation Delay (request latch enabled)		80	100	ns
t_{ELA}	ELR to $A_\emptyset$-A_2 Propagation Delay		40	55	ns
t_{ECA}	ECS to $A_\emptyset$-A_2 Propagation Delay (to enable new requests through request latch)		100	130	ns
t_{ETA}	ETLG to $A_\emptyset$-A_2 Propagation Delay		35	70	ns

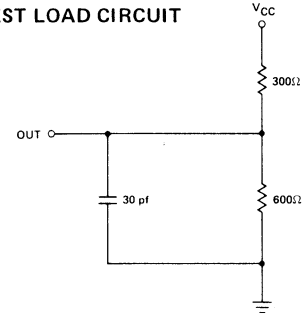
A.C. CHARACTERISTICS (CON'T)

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
	Contents of Current Priority Status Latch Determination:				
t_{DECS}[4]	SGS and $B_\emptyset$-B_2 Set-Up Time to ECS	20	10		ns
t_{DECH}[4]	SGS and $B_\emptyset$-B_2 Hold Time After ECS	20	10		ns
	Enable Next Level Group Determination:				
t_{REN}	$R_\emptyset$-R_7 to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	30	ns
t_{ECRN}	ECS to ENLG Propagation Delay (enabling new request through the request latch)		85	110	ns
t_{ECSN}	ECS to ENLG Propagation Delay (enabling new SGS through status latch)		35	55	ns

NOTES:
(1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) Required for proper operation if ISE is enabled during next clock pulse.
(3) These times are not required for proper operation but for desired change in interrupt flip-flop.
(4) Required for new request or status to be properly loaded.
(5) $t_{CY} = t_{ICS} + t_{CI}$

TEST CONDITIONS:
Input pulse amplitude: 2.5 volts.
Input rise and fall times: 5 ns between 1 and 2 volts.
Output loading of 15 mA and 30 pf.
Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT



CAPACITANCE(5)

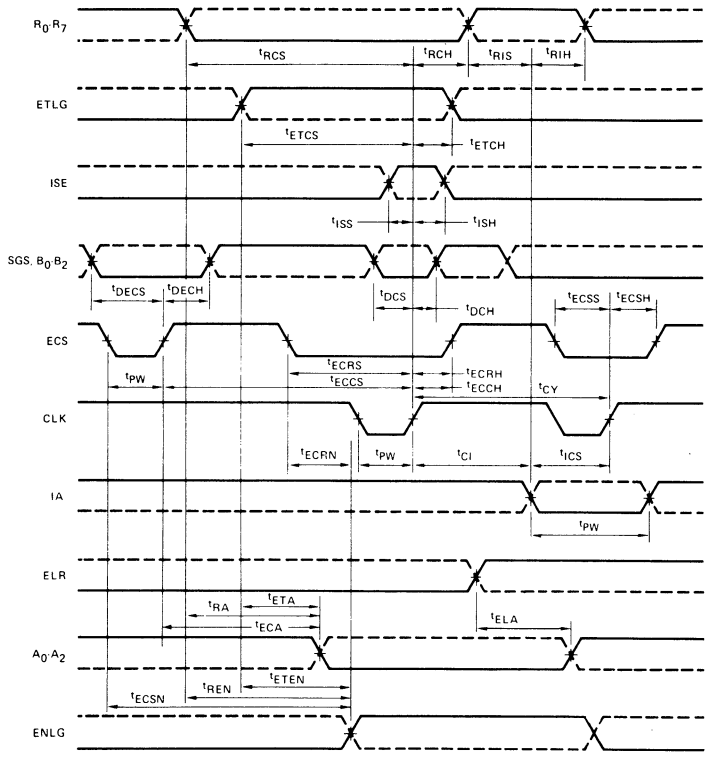
T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	TYP(1)	MAX	UNIT
C_{IN}	Input Capacitance		5	10	pf
C_{OUT}	Output Capacitance		7	12	pf

TEST CONDITIONS:
V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C, f = 1 MHz

NOTE:
(5) This parameter is periodically sampled and not 100% tested.

WAVEFORMS


R0-R7
tRCS
tRCH
tRIS
tRIH
ETLG
tETCS
tETCH
ISE
tISS
tISH
SGS, B0-B2
tDECS
tDECH
tDCS
tDCH
tECSS
tECSH
ECS
tECRS
tECCS
tECRH
tECCH
tPW
tCY
CLK
tECRN
tPW
tCI
tICS
IA
tPW
ELR
tRA
tETA
tECA
tELA
A0-A2
tETEN
tREN
tECSN
ENLG

3216/3226

PARALLEL BIDIRECTIONAL BUS DRIVER

The INTEL® 3216 is a high-speed 4-bit Parallel, Bidirectional Bus Driver. Its three-state outputs enable it to isolate and drive external bus structures associated with Series 3000 systems

The INTEL 3226 is a high-speed 4-bit Parallel, Inverting Bidirectional Bus Driver. Its three-state outputs enable it to isolate and drive external bus structures associated with Series 3000 systems.

The 3216/3226 driver and receiver gates have three state outputs with PNP inputs. When the drivers or receivers are tri-stated the inputs are disabled, presenting a low current load, typically less than 40 μamps, to the system bus structure.

High Performance—25 ns typical propagation delay

Low Input Load Current—0.25 mA maximum

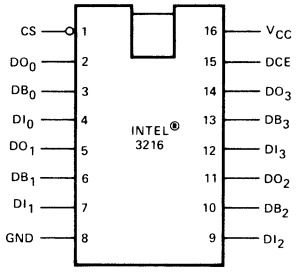
High Output Drive Capability for Driving System Data Busses

Three-State Outputs

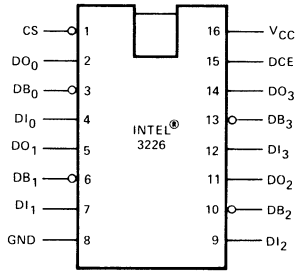
TTL Compatible

16-pin DIP

PACKAGE CONFIGURATION

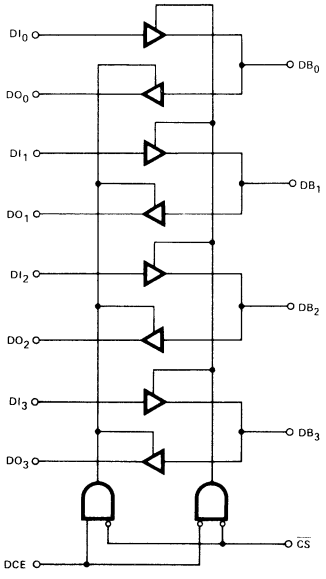


3216

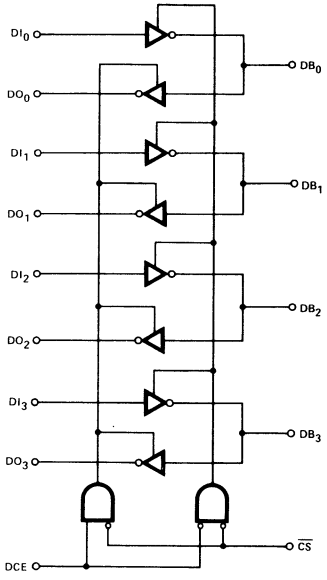


3226

LOGIC DIAGRAM 3216



LOGIC DIAGRAM 3226



3000 SERIES MPU

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias

Ceramic . . . . . –65°C to +75°C

Plastic . . . . . 0°C to +75°C

Storage Temperature . . . . . –65°C to +160°C

All Output and Supply Voltages. . . . . –0.5V to +7V

All Input Voltages . . . . . –1.0V to +5.5V

Output Currents . . . . . 125 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to +75°C, V_{CC} = +5.0V ±5%

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Condition
I_F	Input Load Current					
	DCE, $\overline{CS}$ Inputs		-0.15	-0.5	mA	V_F = 0.45V
	All Other Inputs		-0.08	-0.25	mA	
I_R	Input Leakage Current					
	DCE, $\overline{CS}$ Inputs			80	µA	V_R = 5.25V
	DI Inputs			40	µA	
V_C	Input Clamp Voltage			-1	V	I_C = -5mA
V_{IL}	Input Low Voltage			0.95	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	V_{CC} = 5.0V
V_{OL1}	Output Low Voltage DO, DB Outputs		0.3	0.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output Low Voltage DB Outputs Only		0.5	0.6	V	DB Outputs I_{OL} = 50mA
V_{OH1}	Output High Voltage DO Outputs Only	3.65	4.0		V	I_{OH}=-1mA
V_{OH2}	Output High Voltage DB Outputs Only	2.4	3.0		V	I_{OH}=-10mA
I_{SC}	Output Short Circuit Current					
	DO Outputs	-15	-35	-65	mA	V_{CC} = 5.0V
	DB Outputs	-30	-75	-120	mA	
$\lvert I_O \rvert$	Output Leakage Current High Impedance State					
	DO Outputs			20	µA	V_O = 0.45V/V_{CC}
	DB Outputs			100	µA	
I_{CC}	Power Supply Current 3216		95	130	mA	
	3226		85	120	mA	

NOTE: Typical values are for T_A = 25°C

3000 SERIES MPU

A.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = +5.0V ±5%

Symbol	Parameter		Limit Min.	Typ.	Max.	Unit	Condition
T_{PD1}	Input to Output Delay DO Outputs	3216		15	25	ns	C_L=30pF, R_1=300Ω, R_2=600Ω
		3226		14	25		
T_{PD2}	Input to Output Delay DB Outputs	3216		19	30	ns	C_L=300pF, R_1=90Ω, R_2=180Ω
		3226		16	25		
T_E	Output Enable Time DCE, CS	3216		42	65	ns(2)	DO Outputs: C_L=30pF, R_1=300Ω/10KΩ, R_2=600Ω/1KΩ
		3226		36	54		DB Outputs: C_L=300pF, R_1=90Ω/10KΩ, R_2=180Ω/1KΩ
T_D	Output Disable Time DCE, CS			16	35	ns(2)	DO Outputs: C_L=5pF, R_1=300Ω/10KΩ, R_2=600Ω/1KΩ
							DB Outputs: C_L=5pF, R_1=90Ω/10KΩ, R_2=180Ω/1KΩ

NOTE: (1) Typical values are for T_A = 25°C and nominal supply voltage.

(2) The test load circuit is set for worst case source and sink loading on the outputs. The two resistor values for R1 and R2 correspond to worst case sink and source loading, respectively.

CAPACITANCE(2) T_A = 25°C

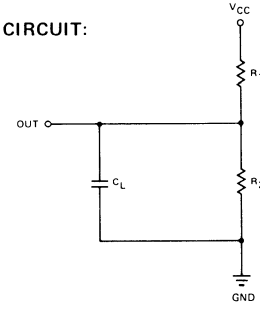
Symbol	Parameter	Limit Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance		4	6	pF
C_{OUT}	Output Capacitance				
	DO Outputs		6	10	pF
	DB Outputs		13	18	pF

Note:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V and T_A = 25°C.

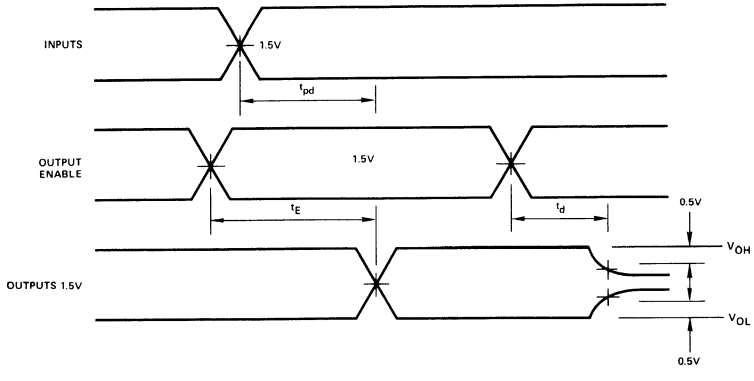
TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:



WAVEFORMS



MILITARY TEMP.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias

Ceramic . . . . . -65°C to +75°C

Storage Temperature . . . . . -65°C to +160°C

All Output and Supply Voltages. . . . . -0.5V to +7V

All Input Voltages . . . . . -1.0V to +5.5V

Output Currents . . . . . 125 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = -55°C to +125°C, V_{CC} = +5.0V ±10%

Symbol	Parameter	Min.	Limit Typ.	Max.	Unit	Condition
I_F	Input Load Current					
	DCE, $\overline{CS}$ Inputs		-0.15	-0.5	mA	V_F = 0.45V
	All Other Inputs		-0.08	-0.25	mA	
I_R	Input Leakage Current					
	DCE, $\overline{CS}$ Inputs			80	μA	V_R = 5.5V
	DI Inputs			40	μA	
V_C	Input Clamp Voltage			-1.2	V	I_C = -5mA
V_{IL}	Input Low Voltage M3216			0.95	V	V_{CC} = 5.0V
	M3226			0.90	V	
V_{IH}	Input High Voltage	2.0			V	V_{CC} = 5.0V
V_{OL1}	Output Low Voltage DO, DB Outputs		0.3	0.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output Low Voltage DB Outputs Only		0.5	0.6	V	DB Outputs I_{OL} = 45mA
V_{OH1}	Output High Voltage DO Outputs Only	3.4	3.8		V	I_{OH}=-0.5mA
V_{OH2}	Output High Voltage DB Outputs Only	2.4	3.0		V	I_{OH}=-5mA
I_{SC}	Output Short Circuit Current					
	DO Outputs	-15	-35	-65	mA	V_{CC} = 5.0V
	DB Outputs	-30	-75	-120	mA	
$\lvert I_O \rvert$	Output Leakage Current High Impedance State					
	DO Outputs			20	μA	V_O = 0.45V/V_{CC}
	DB Outputs			100	μA	
I_{CC}	Power Supply Current M3216		95	130	mA	
	M3226		85	120	mA	

NOTE: Typical values are for T_A = 25°C

3000 SERIES MPU

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = 5.0V ±10%

Symbol	Parameter		Limit Min.	Typ.	Max.	Unit	Condition
T_{PD1}	Input to Output Delay DO Outputs			15	25	ns	C_L=30pF, R_1=300Ω, R_2=600Ω
T_{PD2}	Input to Output Delay DB Outputs	M3216		19	33	ns	C_L=300pF, R_1=90Ω, R_2=180Ω
		M3226		16	25		
T_E	Output Enable Time	M3216		42	75	ns(2)	DO Outputs: C_L=30pF, R_1=300Ω/10KΩ, R_2=600Ω/1KΩ
		M3226		36	62		DB Outputs: C_L=300pF, R_1=90Ω/10KΩ, R_2=180Ω/1KΩ
T_D	Output Disable Time	M3216		16	40	ns(2)	DO Outputs: C_L=5pF, R_1=300Ω/10KΩ, R_2=600Ω/1KΩ
		M3226		16	38		DB Outputs: C_L=5pF, R_1=90Ω/10KΩ, R_2=180Ω/1KΩ

NOTE: (1) Typical values are for T_A = 25°C and nominal supply voltage.

(2) The test load circuit is set for worst case source and sink loading on the outputs. The two resistor values for R1 and R2 correspond to worst case sink and source loading, respectively.

CAPACITANCE(2) T_A = 25°C

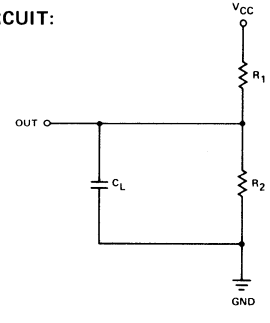
Symbol	Parameter	Limit Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance		4	6	pF
C_{OUT}	Output Capacitance				
	DO Outputs		6	10	pF
	DB Outputs		13	18	pF

Note:
(2) This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V and T_A = 25°C.

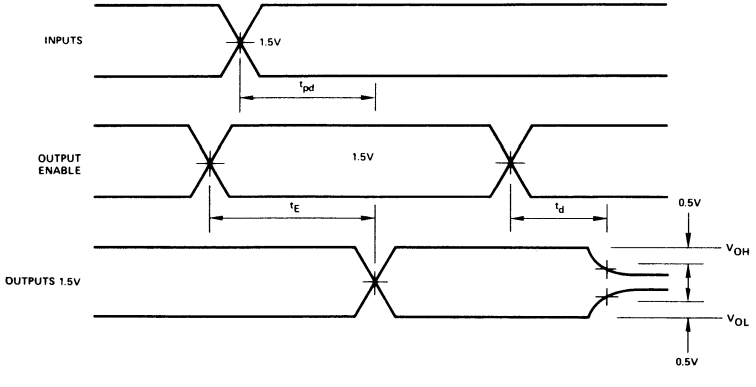
TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT:



WAVEFORMS



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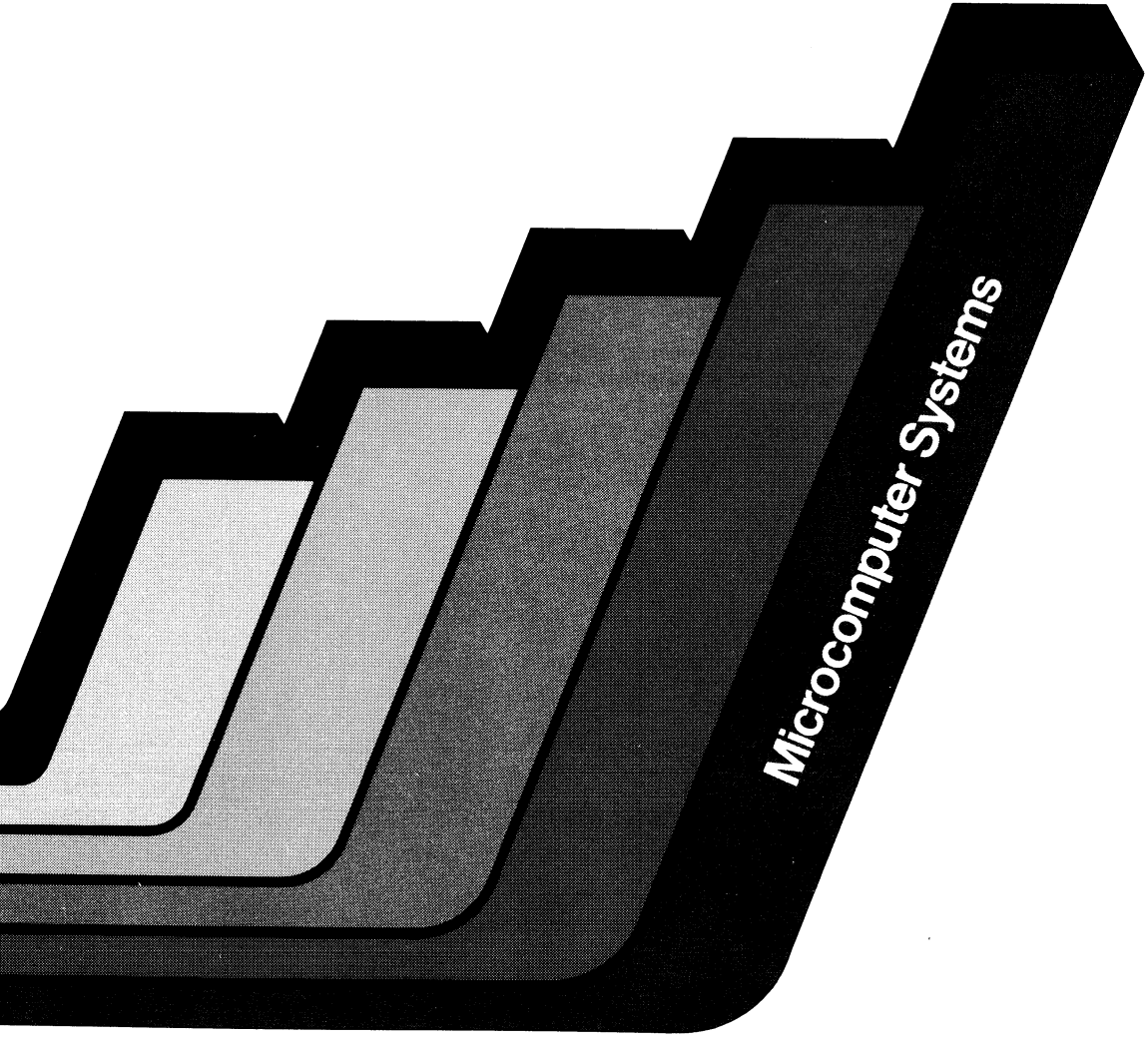


MICROCOMPUTER SYSTEMS

INTRODUCTION

Single Board Computers provide all the resources of a full computer (i.e., CPU, Read/Write Memory, Read Only Memory, Parallel I/O, and Serial I/O) on a single PC board. Intel's System 80/10 and System 80/20 extend these capabilities into a low-cost, fully packaged, RETMA rack-mountable computer. Both the Single Board Computers and packaged Systems are supported by a complete line of memory and I/O expansion boards, peripheral and DMA controllers, prototyping packages, modular backplane/cardcages, and power supplies.

For those applications with unique requirements, unsuited for the standard SBC 80 and System 80 products, Intel offers complete custom design, assembly, and test capability.

TABLE OF CONTENTS

SBC 80/10 SINGLE BOARD COMPUTER

8080A Central Processing Unit

1 K bytes of read/write memory

Sockets for 4K bytes of programmable or masked read-only memory

48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

Programmable Synchronous/Asynchronous communications interface with selectable teletypewriter or RS232C compatibility

Six interrupt request lines

Bus drivers for memory and I/O expansion

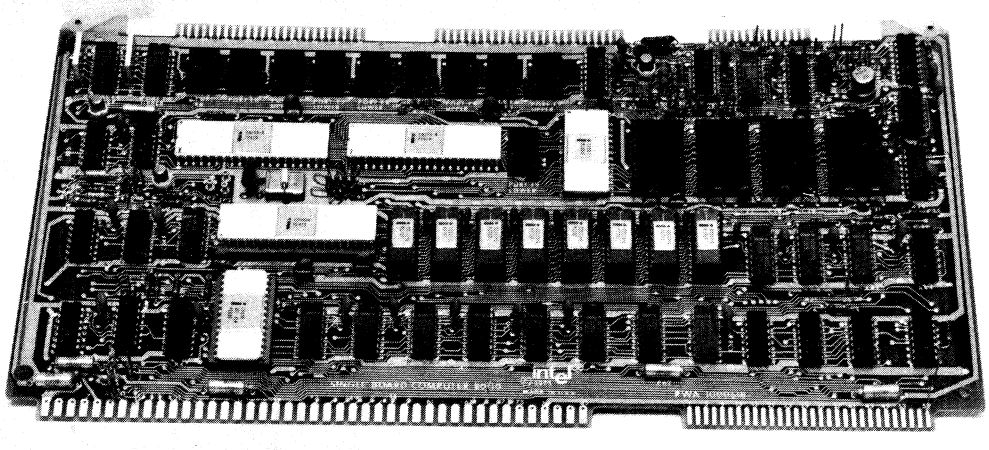
Compatible with optional memory and I/O expansion boards.

The SBC 80/10 is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer based solutions for OEM applications. The SBC 80/10 is a complete computer system on a single 6.75-by-12 inch printed circuit card. The CPU, system clock, read/write memory, non-volatile read-only-memory, I/O ports and drivers, serial communications interface, bus control logic and drivers all reside on the board.

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the SBC 80/10. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators.

The 8080A has a 16-bit program counter which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last in/first out stack to store the contents of the program counter, flags, accumulator and all of the six general purpose registers. A sixteen bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting that is bounded only by memory size.

The SBC 80/10 contains 1K bytes of read/write memory using Intel® 8111 low power static RAM. All on-board RAM read and write operations are performed at maximum processor speed. Sockets for up to 4K bytes of non-volatile read-only memory are provided on the board. Read only memory may be added in 1K byte increments using Intel 8708 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 8308 masked ROMs. All on-board ROM read operations are performed at maximum processor speed.



MICRO-COMPUTER SYSTEMS

The SBC 80/10 contains 48 programmable parallel I/O lines implemented using two Intel 8255 Programmable Peripheral Interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output, and bi-directional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50 pin edge connectors that mate with flat-cable or round-cable.

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A jumper selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e. synchronous or asynchronous), data format, control character format, parity, and asynchronous transmission rate are all under program control. The 8251 provides full duplex, double buffered transmission and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of jumper selectable TTY or RS232C compatible interfaces on the board, in conjunction with the USART provide a direct interface to teletypes, CRTs, RS232 compatible cassettes, asynchronous and synchronous modems. The RS232C or TTY command lines, serial data lines, and signal ground lines are brought out to a 25-pin edge connector that mates with RS232C compatible flat or round cable.

Interrupt requests may originate from six sources. Two jumper selectable interrupt requests can be automatically generated by the Programmable Peripheral Interface when a byte of information is ready to be transferred to the CPU (i.e. input buffer is full) or a byte of information has been transferred to a peripheral device (i.e. output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e. receive channel buffer is full) or a character is ready to be transmitted (i.e. transmit channel data buffer is empty). These four interrupt request lines are all individually maskable under program control. Two interrupt request lines may be interfaced directly to user designated peripheral devices; one via the system bus and the other via the I/O edge connector. The six interrupt request lines share a single CPU interrupt level. When an interrupt request is recognized, a RESTART 7 instruction is generated. The processor responds by suspending program execution and executing a user defined interrupt service routine originating at location 38_{16}.

SBC 80 memory and I/O capacity may be increased by adding standard Intel memory and I/O boards. Memory may be expanded to 64K bytes by adding user specified combinations of SBC-016 16K RAM boards, SBC-416 16K PROM boards, and SBC-406 6K PROM boards. Input/output capacity may be increased to 504 input lines and 504 output lines using SBC-508 I/O boards, containing 32 input lines and 32 output lines per board. Memory and I/O may be increased simultaneously by adding an SBC-104 board containing 4K bytes of RAM, sockets for 4K bytes of PROM, 48 programmable I/O lines and a USART. Modular expandable backplanes and card cages, with a four-board capacity, are available to support multi-board systems.

The development cycle of SBC 80/10 based products may be significantly reduced using the Intellec® Microcomputer Development System. The resident macro-assembler, text editor, and system monitor greatly simplify the design, development, and debug of SBC 80/10 system software. An optional Diskette Operating System allows programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique In-Circuit Emulator (ICE-80) option provides the capability of developing and debugging software directly on the SBC 80/10.

Intel's high-level programming language, PL/M, provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs.

TABLE 1 INPUT/OUTPUT PORT MODES OF OPERATION

PORT	NO. OF LINES	MODE OF OPERATION					
		UNIDIRECTIONAL				BIDIRECTIONAL	CONTROL
		INPUT		OUTPUT			
		UNLATCHED	LATCHED & STROBED	LATCHED	LATCHED & STROBED		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	8	X		X			X[1]
4	8	X		X			
5	8	X		X			
6	4	X		X			
	4	X		X			

1. Note: Port 3 must be used as a control port when either Port 1 or Port 2 are used as a latched and strobed input or a latched and strobed output or Port 1 is used as a bidirectional port.

SPECIFICATIONS

WORD SIZE
Instruction: 8, 16, or 24 bits
Data: 8 bits

CYCLE TIME
Basic Instruction Cycle: 1.95 μsec
Note: Basic instruction cycle is defined as the fastest instruction (i.e. four clock cycles)

MEMORY ADDRESSING
On-Board ROM/PROM: 0–0FFF
On-Board RAM: 3C00-3FFF

MEMORY CAPACITY
On-Board ROM/PROM: 4K bytes (sockets only)
On-Board RAM: 1K bytes
Off-Board Expansion: Up to 65,536 bytes using user specified combinations of RAM, ROM, and PROM

Note: ROM/PROM may be added in 1K byte increments.

I/O ADDRESSING
On-Board Programmable I/O (See Table 1)

Port	8255 No. 1			8255 No. 2			8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O CAPACITY
Parallel: 48 programmable lines (See Table 1)

Note: Expansion to 504 input and 504 output lines can be accomplished using optional I/O boards.

SERIAL BAUD RATES

Frequency (KHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷16	÷64
307.2	–	19200	4800
153.6	–	9600	2400
76.8	–	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	–	110

SERIAL COMMUNICATIONS CHARACTERISTICS
Synchronous:
5–8 bit characters
Internal or external character synchronization
Automatic Sync Insertion
Asynchronous:
5–8 bit characters
Break character generation
1, 1-1/2, or 2 stop bits
False start bit detectors

INTERRUPTS
Single-level with on-board logic that automatically vectors processor to location 38_{16} using RESTART 7 instruction. Interrupt requests may originate from user specified I/O (2) the programmable peripheral interface (2), or USART (2).

INTERFACES
Bus: All signals TTL compatible
Parallel I/O: All signals TTL compatible
Serial I/O: RS232C, or a 20 mil current loop TTY interface (jumper selectable)
Interrupt Requests: All TTL compatible (active low)

SYSTEM CLOCK
2.048 MHz ±0.1%

CONNECTORS

Interface	No. of Double-Sided Pins	Centers (in.)	Mating Connectors	
Bus	86	0.156	CDC VPB01E43D00A1	Wire-Wrap
Parallel I/O (2)	50	0.1	3M 3415-000 or TI H312125	Flat Pins
Serial I/O	26	0.1	3M 3462-0001 or AMP 88106-1	Flat Flat

PHYSICAL CHARACTERISTICS
Width: 12.00 in. (30.48 cm) Depth: 0.50 in.(1.27 cm)
Height: 6.75 in. (17.15 cm) Weight: 14 oz. (484.4 gm)

ELECTRICAL CHARACTERISTICS

DC Power:	w/o PROM[1]	with PROM[2]
V_{CC} = +5 ±5%	I_{CC} = 2.9A max	4.0A
V_{DD} = +12 ±5%	I_{DD} = 140 mA max	400 mA
V_{BB} = –5V ±5%	I_{BB} = 2 mA max	200 mA
V_{AA} = –12V ±5%	I_{AA} = 175 mA max	175 mA

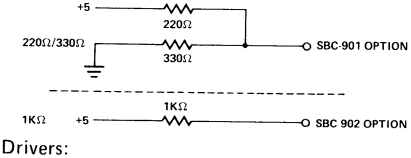
Notes: 1. Does not include power required for optional PROM, I/O drivers, and I/O terminators.
2. With four 2708 PROMs and ten 220/330Ω resistor packs installed, all low.

LINE DRIVERS AND TERMINATORS
I/O Drivers:
The following line drivers and terminators are all compatible with the I/O driver sockets on the SBC 80/10.

Driver	Characteristic	Sink Current (ma)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note: I = inverting, N.I. = non-inverting, O.C. = open collector.

Port 1 has 25 nA totem pole drivers and 1 kΩ terminators.
I/O Terminators:
Terminators: 220Ω/330Ω divider or 1 kΩ pull up

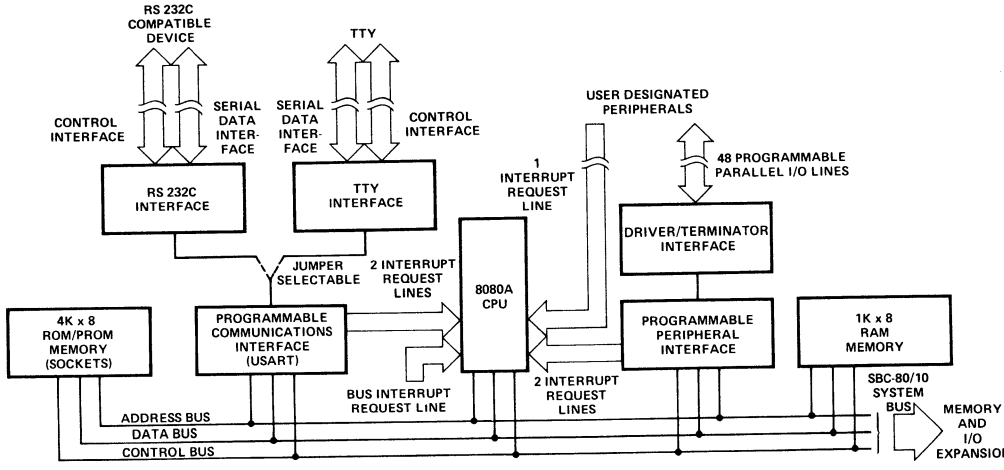


Bus Drivers:

Function	Characteristic	Sink Current (mA)
Data	Tri-State	25
Address	Tri-State	25
Commands	Tri-State	25

ENVIRONMENTAL
Operating Temperature: 0°C to 55°C

COMPATIBLE BOARDS
SBC-016 16K byte RAM
SBC-406 6K byte PROM
SBC-416 16K byte PROM
SBC-508 32 input lines/32 output lines
SBC-104 4K byte RAM, 4K byte PROM, 48 prog. I/O lines, USART



1. Interrupts originating from the Programmable Communications Interface and Programmable Peripheral Interface are jumper selectable.

SBC 80/10 BLOCK DIAGRAM

SBC 80/20 SINGLE BOARD COMPUTER

8080A CPU

2K bytes static read/write memory

Sockets for 4K bytes of erasable reprogrammable or masked Read-Only-Memory

48 programmable parallel I/O lines with sockets for interchangeable line drivers and line terminators

Programmable synchronous/asynchronous RS232C compatible serial interface with fully software-selectable baud rate generation

Full Multi-Master Bus control logic which allows up to 16 masters to share system bus

Eight-level programmable interrupt control

Two programmable 16-bit BCD and binary timers

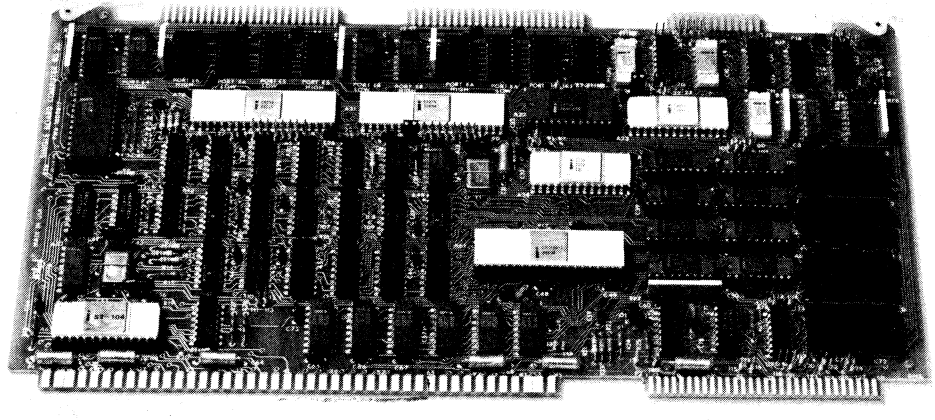
Auxiliary power bus, memory protect, and Power-Fail Interrupt control logic provided for battery back-up RAM requirements

Compatible with optional memory and I/O expansion boards

The SBC 80/20 is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer based solutions for OEM applications. The SBC 80/20 is a complete computer system on a single 6.75 X 12-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read-only-memory, I/O ports and drivers, serial communications interface, priority interrupt logic, two programmable timers, multi-master bus control logic, and bus expansion drivers all reside on the board.

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the SBC 80/20. The 8080A contains six 8-bit general-purpose registers and an accumulator. The six general-purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum instruction execution time is 1.86 μsec.

The 8080A has a 16-bit program counter which allows direct addressing of up to 65,536 bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general-purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting that is bounded only by memory size.

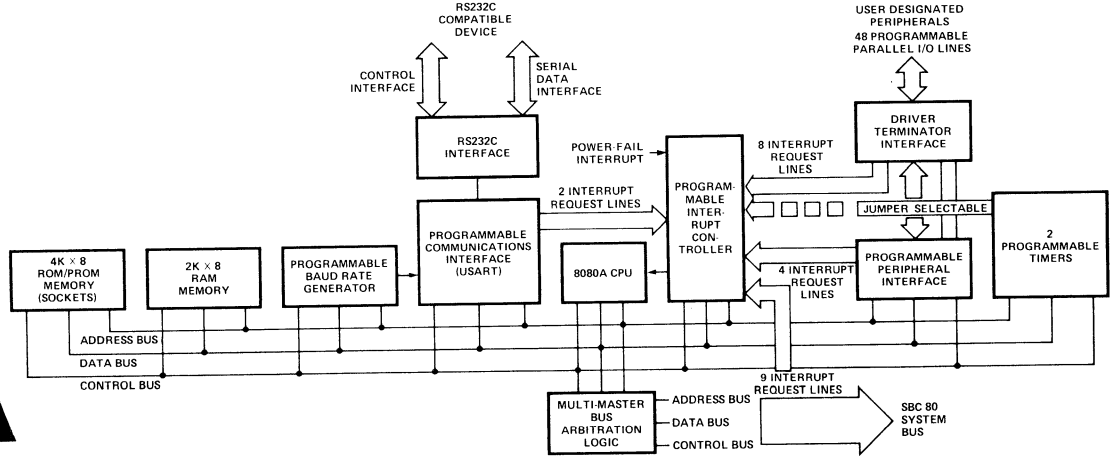


The SBC 80/20 contains 2K bytes of read/write memory using Intel® low-power static RAM. All on-board RAM read and write operations are performed at maximum processor speed. Power for on-board RAM memory is provided on an auxiliary power bus, and memory protect logic is included, for battery back-up RAM requirements. Sockets for up to 4K bytes of nonvolatile read-only-memory are provided on the board. Read-only-memory may be added in 1K byte increments using Intel 8708 Erasable and Electrically Reprogrammable ROMs (EPROMs) or Intel 8308 Masked ROMs. All on-board ROM read operations are performed at maximum processor speed.

The SBC 80/20 contains 48 programmable parallel I/O lines implemented using two Intel 8255 Programmable Peripheral interfaces. The system software is used to configure the I/O lines in any combination of the undirectional input/output, and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, woven, or round-cable.

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on this board. A software selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251 provides full duplex, double-buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface on the board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round-cable.

The SBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The SBC 530 may be used to interface the SBC 80/20 to teletypewriters and other 20 mA current loop equipment.



SBC 80/20 BLOCK DIAGRAM

The SBC 80/20 is a full computer on a single board with resources capable of supporting the majority of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share system tasks with communication over the system bus), the SBC 80/20 provides full bus arbitration control logic.

This control logic allows up to four SBC 80/20's or high-speed controllers to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters may share the system bus with the addition of an external priority network. Once bus control is attained, a bus band width of up to 5 Mbytes/sec may be achieved.

The bus controller provides its own clock which is derived independently from the processor clock. This allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. Once a bus request is granted, single or multiple read/write transfers can proceed at a maximum rate of 5 million data words per second. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high-speed direct-memory-address (DMA) operations and high-speed peripheral control, but are by no means limited to these three.

The SBC 80/20 provides three fully programmable and independent BCD and binary 16-bit interval timers/event counters utilizing an Intel 8253 Programmable Interval Timer. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of each of these counters is jumper-selectable. Each may be independently routed to the programmable interrupt controller, the I/O line drivers and terminators, or outputs from the 8255 Programmable Peripheral Interfaces. The third interval timer in the 8253 provides the programmable baud rate generator for the SBC 80/20 RS232C USART serial port.

In utilizing the SBC 80/20, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Five functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple READ operations for event counting applications, and special commands are included so that the contents of each counter can be used "on the fly".

An Intel 8259 Programmable Interrupt Controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer so that the manner in which requests are processed may be configured to match system requirements. Operating mode and priority assign-

TABLE 1

INPUT/OUTPUT PORT MODES OF OPERATION

PORT	NO. OF LINES	MODE OF OPERATION					
		UNIDIRECTIONAL				BIDIRECTIONAL	CONTROL
		INPUT		OUTPUT			
		UNLATCHED	LATCHED & STROBED	LATCHED	LATCHED & STROBED		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X[2]
	4	X		X			X[2]

NOTES: 1. Part of Port 3 must be used as a control port when either Port 1 or Port 2 are used as a latched and strobed input or a latched and strobed output port or Port 1 is used as a bidirectional port.

2. Part of Port 6 must be used as a control port when either Port 4 or Port 5 are used as a latched and strobed input or a latched and strobed output port or Port 4 is used as a bidirectional port.

TABLE 2

PROGRAMMABLE TIMER FUNCTIONS

FUNCTION	OPERATION
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of REAL-TIME CLOCKS.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Event Counter	On a jumper-selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

ments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked through storage via software, of a single byte to the Interrupt Mask Register of the PIC.

The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32 or 64-byte block may be located to begin at any 32 or 64-byte boundary in the 65,536 byte memory space. A single 8080 JUMP instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt requests may originate from 26 sources. Four jumper-selectable interrupt requests can be automatically generated by the Programmable Peripheral Interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper-selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper-selectable request can be generated by each of the programmable timers. Nine additional interrupt request lines are available to the user for direct interfaces to user designated peripheral devices via the system bus, and eight interrupt request lines may be jumper routed directly from peripherals via the parallel I/O driver/terminator section.

Control logic is also included for generation of a Power-Fail Interrupt which works in conjunction with the AC-low signal from SBC 635 Power Supply or equivalent.

SBC 80 memory and I/O capacity may be increased by adding standard Intel memory, I/O, and combination expansion boards. Memory may be expanded to 65,536 bytes by adding user-specified combinations of SBC 016 16K RAM boards, SBC 416 16K PROM boards, and SBC 406 6K PROM boards. Input/output capacity may be increased to 504 input lines and 504 output lines using SBC 508 I/O boards, containing 32 input lines and 32 output lines per board. Memory and I/O may be increased simultaneously by adding an SBC 104 or SBC 108 Combination Board containing 4K bytes of RAM (8K bytes for SBC 108), sockets for 4K bytes of PROM, 48 programmable I/O lines, and an RS232C USART serial port. SBC 604 and SBC 614 Modular Expandable Backplanes and Cardcages, with a 4-board capacity, are available to support multiboard systems.

The development cycle of SBC 80/20 based products may be significantly reduced using the Intellec® Microcomputer Development System. The resident macro-assembler, text editor, and system monitor greatly simplify the design, development, and debug of SBC 80/20 system software. An optional Diskette Operating System provides a relocating macro assembler, relocating loader and linkage editor, and a library manager. A unique In-Circuit Emulator (ICE-80™) option provides the capability of developing and debugging software directly on the SBC 80/20.

Intel's high-level programming language, PL/M, is also available as a resident Intellec® Microcomputer Development System option. PL/M provides the capability to program in a natural, algorithm language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembler languages.

TABLE 3

PROGRAMMABLE INTERRUPT MODES

MODE	OPERATION
FULLY NESTED	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
AUTO-ROTATING	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
SPECIFIC PRIORITY	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
POLLED	System software examines priority-encoded system interrupt status via Interrupt Status Register.

SPECIFICATIONS

WORD SIZE

Instruction: 8, 16, or 24 bits
Data: 8 bits

CYCLE TIME

Basic Instruction Cycle: 1.86 μsec

Note: Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

MEMORY ADDRESSING

On-Board ROM/PROM: 0–0FFF
On-Board RAM: 2K segments ending at any jumper-selectable address on a 16K boundary (e.g., 0000_H, 4000_H, ... $C000_H$).

MEMORY CAPACITY

On-Board ROM/PROM: 4K bytes (sockets only)
On-Board RAM: 2K bytes
Off-Board Expansion: Up to 65,536 bytes in user-specified combinations of RAM, ROM, and PROM.

Note: ROM/PROM may be added in 1K byte increments.

I/O ADDRESSING

On-Board Programmable I/O (see Table 1).

Port	8255 No. 1			8255 No. 2			8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O CAPACITY

Parallel: 48 programmable lines (see Table 1).

Note: Expansion to 504 input and 504 output lines can be accomplished using optional I/O boards.

SERIAL COMMUNICATIONS CHARACTERISTICS

Synchronous:
- 5–8 bit characters
- Internal or external character synchronization
- Automatic Sync Insertion

Asynchronous:
- 5–8 bit characters
- Break character generation
- 1, 1½, or 2 stop bits
- False start bit detection

Baud Rates:

Frequency (kHz, Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

Note: Frequency selected by I/O write of appropriate 16-bit frequency factor to Baud Rate Register.

Register Address (Hex notation, I/O address space)

Baud Rate Register	DE

Note. Baud Rate Factor (16 bits) is loaded as two sequential output operations to same address (DE_H).

INTERRUPTS

Register Addresses (Hex notation, I/O address space)

Interrupt Request Register	DA
In-Service Register	DA
Mask Register	DB
Command Register	DA
Block Address Register	DB
Status (Polling Register)	DA

Note: Several registers have the same physical address, sequence of access and one data bit of control word determines which register will respond.

TIMERS

Register Addresses (Hex notation, I/O address space)

Control Register	DF
Timer 1	DC
Timer 2	DD

Note: Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies:
Reference: 1.0752 MHz ±0.1% (0.930 μsec period, nominal)
Event Rate: 1.1 MHz max[1]

Note 1. Maximum rate for external events in Mode 4: Event Counter.

Output Frequencies/Timing Intervals:

Mode	Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
		Min	Max	Min	Max
0	Real-Time Interrupt	1.86 μsec	60.948 msec	3.72 μsec	1.109 hrs
1	Programmable One-Shot	1.86 μsec	60.948 msec	3.72 μsec	1.109 hrs
2	Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
3	Square-Wave Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz

INTERFACES

Bus: All signals TTL compatible
Parallel I/O: All signals TTL compatible
Interrupt Requests: All TTL compatible
Timer: All signals TTL compatible
Serial I/O: RS232C compatible, data set configuration

SYSTEM CLOCK (8080A CPU)

2.1504 MHz ±0.1%

ELECTRICAL CHARACTERISTICS

DC Power:

		Without PROM[1]	With PROM[2]	With SBC 530[3]	RAM Only[4]
V_{CC} = +5V ±5%	I_{CC} = 4.7A max	5.6A max	5.6A max	960 mA max	
V_{DD} = +12V ±5%	I_{DD} = 100 mA max	370 mA max	470 mA max	—	
V_{BB} = −5V ±5%	I_{BB} = 1 mA max	180 mA max	180 mA max	—	
V_{AA} = −12V ±5%	I_{AA} = 25 mA max	25 mA max	125 mA max	—	

Note: 1. Does not include power required for optional PROM, I/O drivers, and I/O terminators.
2. With four 8708 EPROMs and eight 220Ω/330Ω input terminators installed, all terminator inputs low.
3. With four 8708 EPROMs, eight 220Ω/330Ω input terminators installed, all terminator inputs low, and SBC 530 Teletypewriter Adapter drawing power from serial port connector.
4. RAM chips powered via Auxiliary Power Bus.

MICRO-COMPUTER SYSTEMS

SPECIFICATIONS (Con't)

AUXILIARY POWER

An Auxiliary Power Bus is provided to allow separate power to RAM for systems requiring battery back-up of read/write memory. Selection of this Auxiliary RAM Power Bus is made via jumpers on the board.

MEMORY PROTECT

An active-low TTL compatible MEMORY PROTECT signal is brought out on the Auxiliary connector which, when asserted, disables Read/Write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

CONNECTORS

Interface	No. of Pins	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 12 oz (340.5 gm)

LINE DRIVERS AND TERMINATORS

I/O Drivers:

The following line drivers are all compatible with the I/O driver sockets on the SBC 80/20.

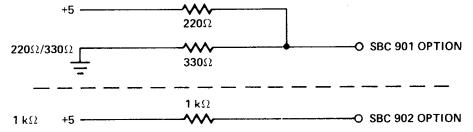
Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note: I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 25 mA totem-pole dividers and 1 kΩ terminators.

I/O Terminators:

Terminators: 220Ω/330Ω divider or 1 kΩ pull-up.



Bus Drivers:

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Address	Tri-State	50
Commands	Tri-State	32

ENVIRONMENTAL

Operating Temperature: 0°C to 55°C

COMPATIBLE BOARDS

SBC 016 16K byte RAM
SBC 104/SBC 108 4K/8K bytes RAM, 4K byte PROM, 48 programmable I/O lines, RS232C Serial Port
SBC 201 Diskette Controller
SBC 406 6K byte PROM
SBC 416 16K byte PROM
SBC 501 DMA Controller
SBC 508 32 Input Lines/32 Output Lines

COMPATIBLE PERIPHERALS

SBC 211 Single Diskette Systems
SBC 212 Dual Diskette Systems

COMPATIBLE HARDWARE

SBC 530 Teletypewriter Adapter
SBC 604/614 Backplanes/Cardcages
SBC 630 Power Supply
SBC 635 Power Supply

SYSTEM 80/10

A completely packaged microcomputer for OEM applications

Processing power from the popular SBC 80/10 Single Board Computer

Multi-source interrupt

Complete power supply with over-voltage protection

Compact, 3½-inch RETMA compatible chassis

Three additional expansion board slots

Software support from Intellec® 800 System

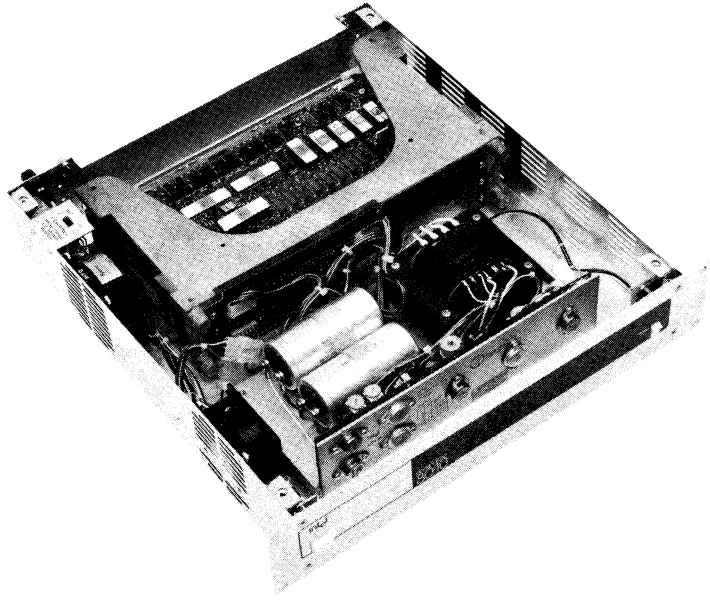
Full 8080A instruction set

Expandable memory capacity
- 1K bytes RAM standard
- Expandable with low-cost 16K RAM, ROM, EPROM Modules

Fully programmable I/O
- Standard asynchronous/synchronous serial I/O port with RS232C and TTY interfaces
- 48 lines parallel I/O standard
- Expandable with low-cost I/O and Combination Modules to 504 input and 504 output lines

Comprehensive System Monitor for loading, execution, and debugging of System 80/10 programs
- Display and alter memory locations
- Read and Write paper tape commands
- CRT or TTY driver

The System 80/10 is a fully packaged microcomputer utilizing the SBC 80/10 Single Board Computer. Ideal for the OEM whose design requires low-cost 19" RETMA compatible rack mountable packaging, the System 80/10 offers easy to use, fully programmable I/O, the computational power of and fully compatible with Intel's SBC 80/10, with both RAM and EPROM memory. The enclosed power supply is designed to support not only the Single Board Computer, but also a full complement of additional slots for expansion boards. The RETMA compatible chassis houses the computer, power supply, fans, and has three additional slots for expansion boards.



The heart of the System 80/10 is the SBC 80/10 Single Board Computer, a complete computer on a single printed circuit board. The SBC 80/10 includes an 8080A CPU, 1K bytes of static RAM memory, sockets for 4K bytes of EPROM memory, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable synchronous/asynchronous communications interface with RS232C and TTY compatibility, a multi-source, single level interrupt network, and bus drivers for memory and I/O expansion.

Read-Only-Memory may be added in 1K byte increments using Intel® 8708 Erasable and Electrically Reprogrammable ROMs (EPROMs) or Intel 8308 Masked ROMs. All on-board OEM read operations are performed at maximum processor speed.

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the SBC 80/10. The 8080A contains six 8-bit general-purpose registers and an accumulator. The six general-purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

The 8080A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/last-out stack to store the contents of the program counter, flags, accumulator, and all of the six general-purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting that is bounded only by memory size.

The System 80/10 contains 48 programmable parallel I/O lines implemented using two Intel® 8255 Programmable Peripheral Interfaces. The system software may be used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat-cable or round-cable.

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A jumper-selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by software to determine the desired asynchronous or synchronous serial data transmission techniques (including IBM Bi-Sync). The mode of data transmission, data format, control character format, parity, and asynchronous transmission rate are all under program control. The 8251 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of jumper-selectable TTY or RS232C compatible interfaces on the board, in teletypewriters, CRTs, RS232 compatible cassettes, asynchronous and synchronous modems. The RS232C or TTY command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat- or round-cable.

TABLE 1

INPUT/OUTPUT PORT MODES OF OPERATION

PORT	NO. OF LINES	MODE OF OPERATION					
		UNIDIRECTIONAL				BIDIRECTIONAL	CONTROL
		INPUT		OUTPUT			
		UNLATCHED	LATCHED & STROBED	LATCHED	LATCHED & STROBED		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	8	X		X			X[1]
4	8	X		X			
5	8	X		X			
6	4	X		X			
	4	X		X			

1. Note: Port 3 must be used as a control port when either Port 1 or Port 2 are used as a latched and strobed input or a latched and strobed output or Port 1 is used as a bidirectional port.

Interrupt requests may originate from six sources. Two jumper-selectable interrupt requests can be automatically generated by the Programmable Peripheral Interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper-selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full) or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). These four interrupt request lines are all individually maskable under program control. Two interrupt request lines may be interfaced directly to user-designated peripheral devices; one via the system bus and the other via the I/O edge connector. The six interrupt request lines share a single CPU interrupt level. When a interrupt request is recognized, a RESTART 7 instruction is generated. The processor responds by suspending program execution and executing a user-defined interrupt service routine originating at location 38_{16}.

System 80/10 memory and I/O capability may be increased by adding standard Intel memory and I/O boards. Memory may be expanded by adding combinations of SBC 016 16K RAM boards and SBC 416 16K PROM boards. Input/output capacity may be increased using SBC 508 I/O boards, containing 32 input lines and 32 output lines per board. Memory and I/O may be increased simultaneously by adding an SBC 104 board containing 4K bytes of RAM, sockets for 4K bytes of PROM, 48 programmable I/O lines, and a USART.

An SBC 604 Modular Cardcage/Backplane is installed in the chassis to house the SBC 80/10 and provide an easily accessible bus interface. The cardcage houses the SBC 80/10 and up to three expansion boards. All SBC 80 bus signals are present on all four mating connectors. Also included are power supply cables which mate with the power supply connectors on the backplane to carry ±5V and ±12V DC.

A comprehensive system monitor, residing in two Intel ROMs, is included to facilitate the loading, execution, and debug of programs. Monitor commands include the ability to read and write hexadecimal paper tapes, execute predefined program segments, display and alter memory contents, and display and alter CPU register contents. Monitor commands and resulting information may be initiated and displayed using a TTY or CRT terminal.

The System 80/10 is designed for easy serviceability and is very modular. The computer boards are accessible from the rear of the package and strain-relief clamps are included to protect the I/O cabling.

Wire-wrap jumpers on the SBC 80/10 select either TTY or RS232C operation, and a jumper-selectable baud rate generator on the SBC 80/10 is used to select the appropriate communications frequency. The System 80/10 is shipped with the jumpers set for TTY operation.

The System 80/10 comes with all in-depth documentation needed to program and interface with the system. An 8080 Assembly Language Manual, PL/M Programming Manual, and a System 80/10 Hardware Reference Manual, are all included to provide clear and concise information relevant to the use of your System 80/10.

The development cycle of System 80/10 based products may be significantly reduced using the Intellec® Microcomputer Development System. The resident macro-assembler, text editor, and system monitor greatly simplify the design, development, and debug of the system software. An optional Diskette Operating System allows programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique In-Circuit Emulator (ICE-80™) option provides the capability of developing and debugging software directly on the System 80/10.

Intel's high-level programming language, PL/M, provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs.

SPECIFICATIONS

WORD SIZE

Instruction: 8, 16, or 24 bits
Data: 8 bits

CYCLE TIME

Basic Instruction Cycle: 1.95 μsec

Note: Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

MEMORY ADDRESSING

On-Board ROM/PROM: 0–0FFF
On-Board RAM: 3C00–3FFF

MEMORY CAPACITY

On-Board ROM/PROM: 4K bytes (sockets only)
On-Board RAM: 1K bytes
Off-Board Expansion: Up to 48K bytes using optional RAM, ROM, and PROM expansion boards.

Note: ROM/PROM may be added in 1K byte increments.

I/O ADDRESSING

On-Board Programmable I/O (see Table 1).

Port	8255 No. 1			8255 No. 2			8255 No. 1 Control	8255 No. 1 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O CAPACITY

Parallel: 48 programmable lines (see Table 1).

Note: Expandable with optional I/O boards.

SERIAL BAUD RATES

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
307.2	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

SERIAL COMMUNICATIONS CHARACTERISTICS

Synchronous:
- 5–8 bit characters
- Internal or external character synchronizatcn
- Automatic Sync Insertion

Asynchronous:
- 5–8 bit characters
- Break character generation
- 1, 1½, or 2 stop bits
- False start bit detectors

INTERRUPTS

Single-level with on-board logic that automatically vectors processor to location 38_{16} using RESTART 7 instruction. Interrupt requests may originate from user-specified I/O (2), the programmable peripheral interface (2), or USART (2).

INTERFACES

Bus:	All signals TTL compatible
Parallel I/O:	All signals TTL compatible
Serial I/O:	RS232C or a 20 mA current loop TTY interface (jumper-selectable)
Interrupt Requests:	All TTL compatible (active-low)

SYSTEM CLOCK

2.048 MHz ±0.1%

CONNECTORS

Interface	No. of Double-Sided Pins	Centers (in.)	Mating Connectors
Parallel I/O (2)	50	0.1	3M 3415-000 Flat
Serial I/O	26	0.1	3M 3462-0001 Flat or AMP 88106-1 Flat

PHYSICAL CHARACTERISTICS

Height: 8.90 cm (3.5 in.)
Width:
- At Front Panel: 48.3 cm (19 in.)
- Behind Front Panel: 43.2 cm (17 in.)

Depth: 50.8 cm (20 in. with all protrusions)
Weight: 37 lb (16.0 kgm)

ELECTRICAL CHARACTERISTICS

Input Power:
- Frequency: 47–63 Hz
- Voltage:
  - Standard: 115 VAC ±10%
  - Option: 230 VAC ±10%

Output Power Available For Expansion Boards:

Voltage	Supply Current	Power Available without PROM & Termination Packs Installed	Power Available with PROM & Termination Packs Installed*	Over-Voltage Protection
+12	2A	1.86A	1.6A	+14 to +16 volts
+5	14A	11.1A	10A	5.8 to 6.6 volts
–5	0.9A	0.898A	0.7A	5.8 to –6.6 volts
–12	0.8A	0.625A	0.625A	–14 to –16 volts

*PROMs are 4 each of 8708's; Termination Packs are 10 each of 220Ω/330Ω.

LINE DRIVERS AND TERMINATORS

I/O Drivers:

The following line drivers and terminators are all compatible with the I/O driver sockets on the SBC 80/10.

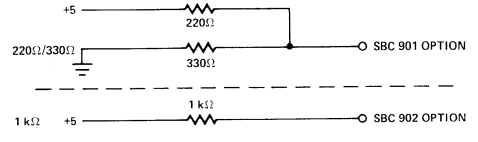
Driver	Characteristic	Sink Current (mA)	Driver	Characteristic	Sink Current (mA)
7438	I,OC	48	7409	NI,OC	16
7437	I	48	7408	NI	16
7432	NI	16	7403	I,OC	16
7426	I,OC	16	7400	I	16

Note: I = inverting; N.I. - non-inverting; O.C. = open collector.

Port 1 has 25 mA totem-pole drivers and 1 kΩ terminators.

I/O Terminators:

Terminators: 220Ω/330Ω divider or 1 kΩ pull-up.



Bus Drivers:

Function	Characteristics	Sink Current (mA)
Data	Tri-state	25
Address	Tri-state	25
Commands	Tri-State	25

ENVIRONMENTAL

Operating Temperature: 0°C to 50°C
Non-operating Temperature: –40°C to 85°C

MICRO-COMPUTER SYSTEMS

SYSTEM MONITOR

Addresses:

0000–0560$_H$ (ROM); 3C00$_H$–3C3F$_H$ (RAM)

Commands:

- Display Memory (D)
- Program Execute (G)
- Insert Instructions into Memory (I)
- Move Memory (M)
- Read Hexadecimal File (R)
- Substitute Memory (S)
- Write Hexadecimal File (W)
- Examine and Modify CPU Registers (X)

Drivers:

- Console Input
- Console Output
- Reader Input
- Punch Output

Breakpoints:

A hardware breakpoint capability may be implemented by an interrupt service routine beginning at RAM location 3C3D$_H$. Typically, a 2-byte call is used. Interrupt generation at the breakpoint may be accomplished by user hardware or by insertion of single byte calls at instruction boundaries.

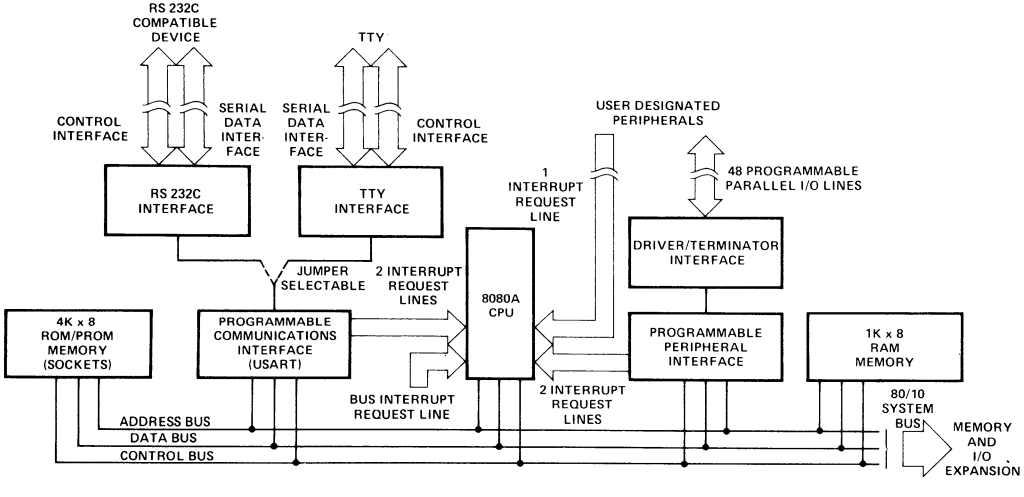
EQUIPMENT SUPPLIED

- System 80/10 Computer with power supply, cardcage, dual fans, and ROM based system monitor
- 115-volt power cable
- 115-volt and 230-volt fuses
- 8080 Assembly Language Manual
- PL/M Programming manual
- System 80/10 Hardware Reference Manual
- SBC 80/10 Schematics

COMPATIBLE EQUIPMENT

- SBC 016 16K byte RAM
- SBC 104 4K bytes RAM, 4K bytes PROM, 48 programmable I/O lines, USART
- SBC 108 8K bytes RAM, 4K bytes PROM, 48 programmable I/O lines, USART
- SBC 201 Flexible Diskette Controller
- SBC 416 16K byte PROM
- SBC 508 32 input lines/32 output lines
- SBC 501 DMA Controller
- SBC 955 Serial I/O Cable Set
- SBC 956 Parallel I/O Cable Set

SYSTEM 80/10 BLOCK DIAGRAM



1. Interrupts originating from the Programmable Communications Interface and Programmable Peripheral Interface are jumper selectable.

SYSTEM 80/20

A rack-mountable, packaged microcomputer for OEM applications

Processing power from the popular SBC 80/20 Single Board Computer.

Full multiprocessor bus control logic allows additional masters to share system bus

Eight-level programmable vectored priority interrupt control

Two programmable 16-bit BCD or Binary Timers

Auxiliary power bus and memory protect control logic provided for battery back-up RAM requirements

Expandable memory capacity

- 2K bytes RAM standard
- Expandable with low-cost 16K RAM, ROM, EPROM, and Combination Modules

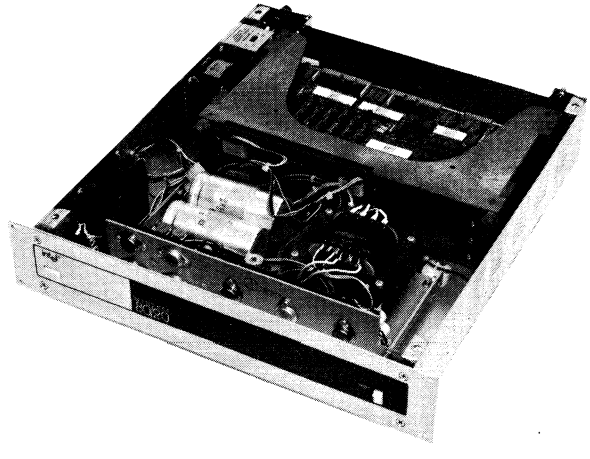
Fully programmable I/O

- Programmable synchronous/asynchronous RS232C compatible serial interface with software selectable baud rate generation
- 48 lines parallel I/O standard
- Expandable with low-cost I/O and Combination Modules

Comprehensive System Monitor for loading, execution, and debugging of System 80/20 programs

- Display and alter memory locations
- Display and alter registers
- Single-step program execution
- Read and Write paper tape commands
- RS232 driver

The System 80/20 is a fully packaged microcomputer utilizing the SBC 80/20 Single Board Computer. Ideal for the OEM whose design requires low-cost 19" RETMA compatible rack mountable packaging. The System 80/20 offers easy to use, fully programmable I/O, the computational power of the SBC 80/20, and has both RAM and EPROM memory. The enclosed power supply is designed to support not only the Single Board Computer, but also a full complement of expansion boards. The RETMA compatible chassis houses the computer, power supply, fans, and has three additional slots for expansion boards.



The heart of the System 80/20 is the SBC 80/20 Single Board Computer, a complete computer on a single printed circuit board. The SBC 80/20 includes an 8080A CPU, 2K bytes of static RAM memory, sockets for 4K bytes of EPROM memory, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable synchronous/asynchronous RS232C communications interface, programmable eight level vectored priority interrupt structure, programmable interval timers, and bus drivers for memory and I/O expansion.

Read-Only-Memory may be added in 1K byte increments using Intel® 8708 Erasable and Electrically Reprogrammable ROMs (EPROMs) or Intel® 8308 Masked ROMs. All on-board memory operations are performed at maximum processor speed.

Intel's powerful 8-bit, N-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the SBC 80/20. The 8080A contains six 8-bit general-purpose registers and an accumulator. The six general-purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

The 8080A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out stack to store the contents of the program counter, flags, accumulator, and all of the six general-purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting that is bounded only by memory size.

The System 80/20 contains 48 programmable parallel I/O lines implemented using two Intel® 8255 Programmable Peripheral interfaces. The system software may configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application.

The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat cable, woven cable, or round cable. The user may design his own cables or order the SBC 955 Serial Cable or the SBC 956 Parallel Cable set.

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A software selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by software to determine the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of data transmission, data format, control character format, parity, and asynchronous transmission rate are all under program control. The 8251 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of the RS232C compatible interface on the board, allows the system to be used directly with CRTs, RS232C compatible cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat- or round-cable. A 20-mil TTY compatible interface may be achieved by using the SBC 530 TTY Adapter.

The System 80/20 is a full computer with resources capable of supporting the majority of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share system tasks with communication over the system bus), the System 80/20

TABLE 1

INPUT/OUTPUT PORT MODES OF OPERATION

PORTS	NO. OF LINES	MODE OF OPERATION					
		UNIDIRECTIONAL				BIDIRECTIONAL	CONTROL
		INPUT		OUTPUT			
		UNLATCHED	LATCHED & STROBED	LATCHED	LATCHED & STROBED		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X[2]
	4	X		X			X[2]

NOTES:

1. Part of Port 3 must be used as a control port when either Port 1 or Port 2 are used as a latched and strobed input or a latched and strobed output port or Port 1 is used as a bidirectional port.
2. Part of Port 6 must be used as a control port when either Port 4 or Port 5 are used as a latched and strobed input or a latched and strobed output port or Port 4 is used as a bidirectional port.

provides full bus arbitration control logic. This control logic allows additional SBC 80/20s or other high-speed controllers to share the system bus in serial (daisy chain) priority fashion, or in parallel priority fashion with the addition of an external priority network. Once bus control is attained, a bus bandwidth of up to 5 Mbytes/sec may be achieved.

The bus controller provides its own clock which is derived independently from the processor clock. This allows different speed controllers to share resources on the same bus, and transfers via the bus to proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. Once a bus request is granted, single or multiple read/write transfers can proceed at a maximum rate of 5 million data bytes per second.

The System 80/20 provides three fully programmable and independent BCD and binary 16-bit interval timers/event counters utilizing an Intel® 8253 Programmable Interval Timer. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of each of these counters is jumper-selectable. Each may be independently routed to the programmable interrupt controller, the I/O line drivers and terminators or outputs from 8255 Programmable Peripheral Interfaces. The third interval timer in the 8253 provides the programmable baud rate generator for the RS232C USART serial port.

The systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timer/event counters select the desired function. Five functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple READ operations for event counting applications, and special commands are included so that the contents of each counter can be used "on the fly."

An Intel® 8259 Programmable Interrupt Controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer so that the manner in which requests are processed may be configured to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked through storage via software, of a single byte to the Interrupt Mask Register on the PIC.

The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32 or 64-byte block may be located to begin at any 32 or 64-byte boundary in the 65,536 byte memory space. A single 8080A JUMP instruction at each of these addresses can then provide linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt requests may originate from 26 sources. Four jumper-selectable interrupt requests can be automatically generated by the Programmable Peripheral Interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper-selectable interrupt requests can be automatically generated by the USART when a character

TABLE 2

PROGRAMMABLE TIMER FUNCTIONS

FUNCTION	OPERATION
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of REAL-TIME CLOCKS.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Event Counter	On a jumper-selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

TABLE 3

PROGRAMMABLE INTERRUPT MODES

MODE	OPERATION
FULLY NESTED	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
AUTO-ROTATING	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
SPECIFIC PRIORITY	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
POLLED	System software examines priority-encoded system interrupt status via Interrupt Status Register.

is ready to be transferred to the CPU (i.e., receive channel buffer is full) or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper-selectable request can be generated by each of the programmable timers. Nine additional interrupt request lines are available to the user for direct interfaces to user designated peripheral devices via the system bus.

System 80/20 memory may be increased by adding combinations of SBC 016 16K RAM boards and SBC 416 16K PROM boards. Input/Output capacity may be increased using the SBC 508 parallel I/O, the SBC 517 programmable serial and parallel I/O, or the SBC 519 programmable parallel I/O board. System resources may be increased simultaneously using SBC 80 combination I/O and memory expansion boards. All combination boards provide 48 lines of programmable parallel I/O, one programmable serial port, and sockets for up to 4K of EPROM. A RAM increment of 4K, 8K, or 16K can be chosen with the SBC 104, 108, or 116, respectively.

Mass storage capacity may be added to the System 80/20 with Intel's Flexible Diskette peripherals. The SBC 201 Diskette Controller is a very powerful and easy to use plug-in module which is compatible with several manufacturers' diskette drives. For a completely tested mass storage peripheral, the SBC 211 Single Drive System and the SBC 212 Dual Drive System are available.

A Modular Cardcage/Backplane is installed in the chassis to house the SBC 80/20 and provide an easily accessible bus interface. The cardcage houses the SBC 80/20 and any additional expansion boards. All SBC 80 bus signals are present on all mating connectors. Also included are power supply cables which mate with the power supply connectors on the backplane to carry ±5V and ±12V DC.

A comprehensive system monitor, residing in two Intel ROMs, is included to facilitate the loading, execution, and debug of programs. Monitor commands include the ability to read and write hexadecimal paper tapes, execute predefined program segments, display and alter memory contents, display and alter CPU register contents, and single step program execution.

Monitor commands and resulting information may be initiated and displayed using a CRT or other RS232 device.

The System 80/20 is designed for easy modular servicing. The computer boards are accessible from the rear of the package and strain relief clamps are included to protect any I/O cabling added by the OEM.

The System 80/20 comes with all in-depth documentation needed to program and interface with the system. An 8080 Assembly Language Manual, PL/M-80™ Programming Manual, and a Hardware Reference Manual, are all included to provide clear and concise information relevant to the use of a System 80/20.

The development cycle of System 80/20 based products may be significantly reduced using the Intellec® Microcomputer Development System. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of the system software. Optional Diskette Operating Software for the Development System programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique In-Circuit Emulator (ICE-80) option provides the capability to use the Development System to develop and debug software directly on the System 80/20.

Intel's high-level resident programming language, PL/M-80, provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M-80 programs can be written in a much shorter time than assembly language programs.

SPECIFICATIONS

WORD SIZE
Instruction: 8, 16, or 24 bits
Data: 8 bits

CYCLE TIME
Basic Instruction Cycle: 1.86 μsec
Note: Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

MEMORY ADDRESSING
On-Board ROM/PROM: $0–0FFF_H$
On-Board RAM: 2K segments ending at any jumper-selectable address on a 16K boundary (e.g., 0000_H, 4000_H, . . . $C000_H$).

MEMORY CAPACITY
On-Board ROM/PROM: 4K bytes (sockets only)
On-Board RAM: 2K bytes
Off-Board Expansion: Up to 65,536 bytes in user-specified combinations of RAM, ROM, and PROM.
Note: ROM/PROM may be added in 1K byte increments.

I/O ADDRESSING
On-Board Programmable I/O (see Table 1).

Port	8255 No. 1			8255 No. 2			8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O CAPACITY
Parallel: 48 programmable lines (see Table 1).
Note: Expandable with optional I/O boards.

SERIAL COMMUNICATIONS CHARACTERISTICS
Synchronous:
5–8 bit characters
Internal or external character synchronization
Automatic Sync Insertion
Asynchronous:
5–8 bit characters
Break character generation
1, 1½, or 2 stop bits
False start bit detectors

SERIAL BAUD RATES

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

Note: Frequency selected by I/O write of appropriate 16-bit frequency factor to Baud Rate Register.

Register Address (Hex notation, I/O address space)

Baud Rate Register	DE

Note: Baud Rate Factor (16 bits) is loaded as two sequential output operations to same address (DE_H).

INTERRUPTS

Register Address (Hex notation, I/O address space)

Interrupt Request Register	DA
In-Service Register	DA
Mask Register	DB
Command Register	DA
Block Address Register	DB
Status (Polling Register)	DA

Note: Several registers have the same physical address, sequence of access and one data bit of control word determines which register will respond.

TIMERS

Register Address Hex notation, I/O address space)

Control Register	DF
Timer 0	DC
Timer 1	DD

Note: Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies:

Reference: 1.0752 MHz ±0.1% (0.930 μsec period, nominal)
Event Rate: 1.1 MHz max

Note: Maximum rate for external events in Mode 4: Event Counter.

Output Frequencies/Timing Intervals:

Mode	Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
		Min.	Max.	Min.	Max.
0	Real-Time Interrupt	1.86 μsec	60.948 msec	3.72 μsec	1.109 hrs
1	Programmable One-Shot	1.86 μsec	60.948 msec	3.72 μsec	1.109 hrs
2	Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
3	Square-Wave Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz

INTERFACES

Bus: All signals TTL compatible
Parallel I/O: All signals TTL compatible
Interrupt Requests: All TTL compatible
Timer: All signals TTL compatible
Serial I/O: RS232C compatible, data set configuration

SYSTEM CLOCK (8080A CPU)

2.154 MHz ±0.1%

COMPATIBLE CONNECTORS

Interface	No. of Double-Sided Pins	Centers (in.)	Mating Connectors
Parallel I/O (2)	50	0.1	3M 3415-000 Flat TI H312125 Flat
Serial I/O	26	0.1	3M 3462-0001 Flat TI H312113

PHYSICAL CHARACTERISTICS

Height: 8.90 cm (3.5 in.)
Width: At Front Panel: 48.3 cm (19 in.)
Behind Front Panel: 43.2 cm (17 in.)
Depth: 50.8 cm (20 in. with all protrusions)

ELECTRICAL CHARACTERISTICS

Input Power:
Frequency: 47–63 Hz
Voltage: Standard: 115 VAC ±10%
Option: 230 VAC ±10%

Output Power Available for Expansion Boards:

Voltage	Supply Current	Power Available without PROM & Termination Packs Installed	Power Available with PROM & Termination Packs Installed*	Over-Voltage Protection	RAM-Only Power Requirements
+12	2A	1.63A	1.45A	+14 to +16 volts	0.96A
+5	14A	9.1A	8.7A	5.8 to 6.6 volts	
−5	0.9A	0.72A	0.54A	5.8 to −6.6 volts	
−12	0.8A	0.77A	0.775A	−14 to −16 volts	

*PROMs are four 8708s; Termination Packs are eight 220Ω/330Ω Terminator Packs.

AUXILIARY POWER

An Auxiliary Power Bus is provided to allow separate power to RAM for systems requiring battery back-up of read/write memory. Selection of this Auxiliary RAM Power Bus is made via jumpers on the board.

MEMORY PROTECT

An active-low TTL compatible MEMORY PROTECT signal is brought out on the Auxiliary connector which, when asserted, disables Read/Write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

LINE DRIVERS AND TERMINATORS

I/O Drivers:

The following line drivers are all compatible with the I/O driver sockets on the SBC 80/20.

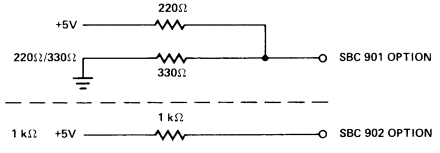
Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note: I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 25 mA totem-pole dividers and 1 kΩ terminators.

I/O Terminators:

Terminators: 220Ω/330Ω divider or 1 kΩ pull-up.



Bus Drivers:

Function	Characteristic	Sink Current (mA)
Data	3-State	50
Address	3-State	50
Commands	3-State	32

ENVIRONMENTAL

Operating Temperature: 0°C to 50°C

SYSTEM MONITOR

Address:
0000–069C$_H$ (ROM), 3F80$_H$–3FFF$_H$ (RAM)
Commands:
Display Memory (D)
Program Execute (G)
Insert Instruction into Memory (I)
Move Memory (M)
Execute Next Instruction (N)
Read Hexadecimal File (R)
Substitute Memory (S)
Write Hexadecimal File (W)
Examine and Modify CPU Registers (X)

Drivers:
- Console Input
- Console Output
- Reader Input
- Punch Output

Breakpoints:

Program BREAKing may occur upon any of up to seven system conditions. BREAKs are implemented via the Programmable Interrupt Controller. When a break occurs, the BREAK level, all CPU registers, and the next instruction (OP CODE) are displayed at the console.

Baud Rate:

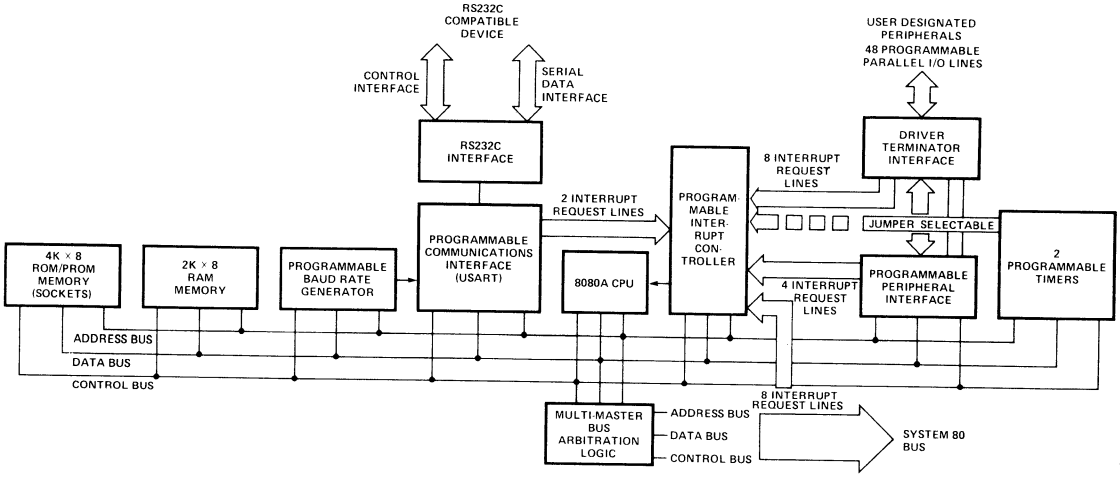
Baud Rate Search Capability automatically sets serial baud rate to that of the system console. Allowable baud rates include 110, 150, 300, 600, 1200, 2400, 4800, and 9600.

EQUIPMENT SUPPLIED
- System 80/20 Computer with power supply, cardcage, dual fans, and ROM based system monitor
- 115-volt power cable
- 115-volt and 230-volt fuses
- 8080 Assembly Language Manual
- PL/M-80 Programming Manual
- System 80/20 Hardware Reference Manual
- SBC 80/20 Schematics

COMPATIBLE BOARDS
- SBC 016 16K byte RAM
- SBC 104 4K bytes RAM, 4K bytes PROM, 48 programmable I/O lines, USART
- SBC 108 8K bytes RAM, 4K bytes PROM, 48 programmable I/O lines, USART
- SBC 116 16K bytes RAM, 4K bytes PROM, 48 programmable I/O lines, USART
- SBC 416 16K byte PROM
- SBC 501 DMA Controller
- SBC 508 32 input lines/32 output lines
- SBC 517 Combination I/O Board
- SBC 519 Programmable Parallel I/O Board
- SBC 955 Serial I/O Cable Set
- SBC 956 Parallel I/O Cable Set

COMPATIBLE PERIPHERALS
- SBC 201 Diskette Controller
- SBC 211 Single Diskette System
- SBC 212 Dual Diskette System

COMPATIBLE HARDWARE
- SBC 530 Teletypewriter Adapter



SYSTEM 80/20 BLOCK DIAGRAM

SBC 016 16K BYTE RAM MEMORY BOARD

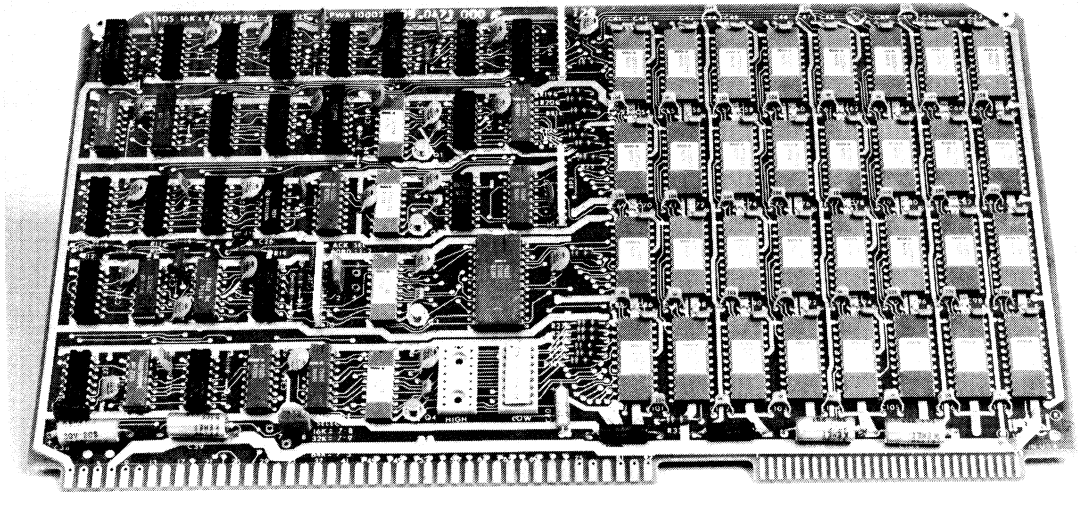
- SBC-80 RAM memory expansion through direct bus interface
- 16K byte read/write memory capacity
- On-board hardware for refresh of all dynamic memory elements
- Jumper selectable starting address for 16K contiguous addresses
- Read/write data buffers
- TTL compatible data, address, and command signal interface

The SBC-016 is a member of Intel's complete line of SBC-80 memory and I/O expansion boards. The SBC-016 interfaces directly to any SBC-80 single board computer, via the system bus, to expand RAM memory capacity.

The board contains 16K bytes of read/write memory, implemented using 32 Intel® 2107 dynamic RAM memory components. On-board refresh hardware refreshes 64 bit positions of all 32 RAM elements every 1.0 milliseconds. Each refresh cycle utilizes memory for 735 nanoseconds. If a read or write cycle is in progress when a refresh cycle is scheduled to begin, the refresh cycle is postponed until the end of the read or write cycle.

The SBC-016 contains a jumper that is used to select contiguous 16K byte address segments that begin in location 0000, 4000, 8000, or C000.

Read/write buffers reside on the board to buffer all data that is written into or read from the memory array. All data, address, and command signals on the bus interface are TTL compatible.



MICRO COMPUTER SYSTEMS

SPECIFICATIONS

WORD SIZE
8 bits

MEMORY SIZE
16,384 bytes

CYCLE TIMES
Read Cycle:	735 ns max
Write Cycle:	1360 ns max
Refresh Cycle:	735 ns max

INTERFACE
All address, data, and command signals are TTL compatible.

ADDRESS SELECTION
Jumper selection of base address of 16K contiguous memory block to reside in locations 0000, 4000, 8000, or C000.

CONNECTOR
86-pin double-sided PC edge connector with 0.156-inch contact centers.

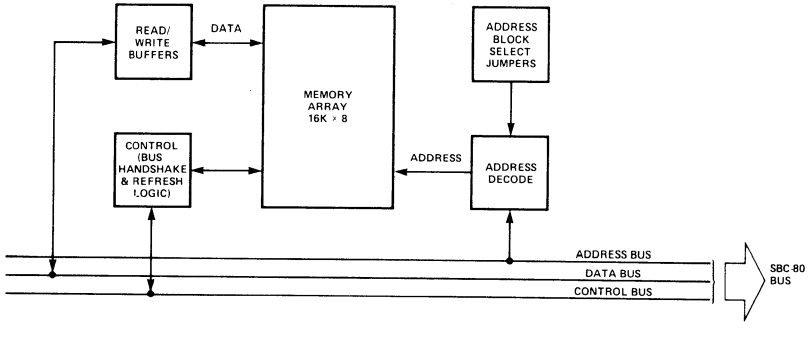
Mating Connector: Control Data VPB01E43A00A1.

PHYSICAL CHARACTERISTICS
Width:	12.00 in.	(30.48 cm)
Height:	6.75 in.	(17.15 cm)
Depth:	0.50 in.	(1.27 cm)
Weight:	12 oz	(415.2 gm)

ELECTRICAL CHARACTERISTICS
DC Power:

V_{CC} = +5 VDC ±5%
I_{CC} = 1.2A typ; 1.5A max
V_{DD} = +12 VDC ±5%
I_{DD} = 0.7A typ; 1.0A max
V_{BB} = −5 VDC ±5%
I_{BB} = 0.2 mA typ; 3.2 mA max

ENVIRONMENT
Operating Temperature: 0°C to 55°C



16K RAM MEMORY EXPANSION BOARD BLOCK DIAGRAM

SBC 104/108/116 COMBINATION MEMORY AND I/O EXPANSION BOARDS

4K, 8K, 16K bytes of read/write memory (SBC 104, SBC 108, SBC 116, respectively)

Sockets for 4K bytes of programmable or masked read-only-memory

Auxiliary power bus and memory protect control logic provided for battery back-up RAM requirements

48 programmable I/O lines with sockets for interchangeable line drivers and terminators

Synchronous/Asynchronous communications interface with RS232C drivers and receivers

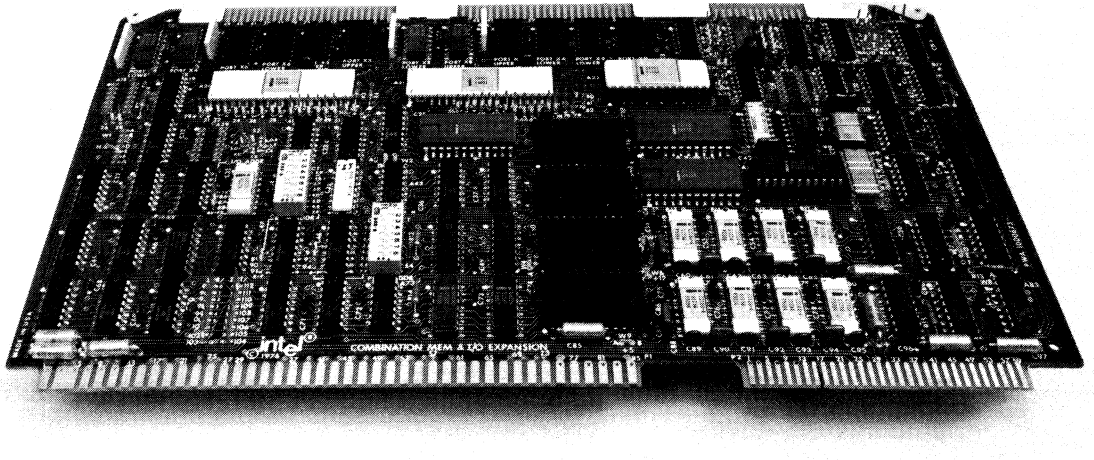
Eight maskable interrupt request lines with a pending interrupt register

1 ms interval timer

The SBC 104, SBC 108, and SBC 116 are members of Intel's complete line of SBC 80 memory and I/O expansion boards. Each board interfaces directly with any SBC 80 Single Board Computer, via the system bus, to expand RAM and ROM memory capacity; serial and parallel I/O capacity.

The SBC 104 contains 4K, the SBC 108 8K, and the SBC 116 16K bytes of RAM memory implemented using Intel dynamic RAM memory components. On-board refresh hardware refreshes a portion of all eight RAM memory elements every 14 microseconds. If a read or write cycle is already in progress when a refresh cycle is scheduled to begin, the refresh cycle is postponed until the end of the read or write cycle. Each refresh cycle utilizes memory for 590 nanoseconds. Typical RAM access time is 485 nanoseconds. Typical Read/Write cycle time is 560 nanoseconds.

Sockets for up to 4K bytes of non-volatile read-only memory reside on the boards. Read-only-memory may be added in 1K byte increments using Intel® 8708 Erasable and Electrically Reprogrammable ROMs (EPROMs) or Intel® 8308 Masked ROMs. Typical ROM/EPROM access time is 440 nanoseconds. Typical ROM/EPROM cycle time is 560 nanoseconds.



MICRO-COMPUTER SYSTEMS

Each combination board contains 48 programmable I/O lines implemented using two Intel® 8255 Programmable Peripheral Interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output, and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, round, or woven cable.

Typical I/O Read access time is 280 nanoseconds. Typical I/O Read cycle time is 600 nanoseconds.

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on each board. A jumper-selectable baud rate generator provides the USART with all common communications frequecies between 75 Hz and 38.4 kHz. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and asynchronous serial transmission rate are all under program control. The 8251 provides full duplex, double-buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of a comprehensive RS232C interface on the boards in conjunction with the USART provides a direct interface to CRTs, RS232C compatible casettes, asynchronous and synchronous modems. The RS232C, serial data lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cables.

The SBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The SBC 530 may be used to interface the SBC 104/108/116 Combination Boards to teletypewriters and other 20 mA current loop equipment.

Interrupt requests may originate from eight sources. Four jumper-selectable interrupt requests can be automatically generated by the Programmable Peripheral Interfaces when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Two jumper-selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). These six interrupt request lines are all maskable under program control. Two interrupt request lines may be interfaced directly from user-designated peripheral devices via the I/O edge connector. An on-board register contains the status of all eight interrupt request lines, and may be interrogated by the CPU. Each interrupt request line is maskable under program control. Routing for the eight interrupt request lines is jumper-selectable. They may be ORed to provide a single interrupt request line for the SBC 80/10, or they may be individually provided to the system bus for use by the SBC 80/20 Priority Interrupt Controller.

Each board contains a jumper-selectable 1 ms interval timer. The timer is enabled by jumpering one of the interrupt request lines from the I/O edge connector to a 1 ms interval interrupt request signal originating from the baud rate generator.

TABLE 1

INPUT/OUTPUT PORT MODES OF OPERATION

PORT	NO. OF LINES	MODE OF OPERATION					
		UNIDIRECTIONAL				BIDIRECTIONAL	CONTROL
		INPUT		OUTPUT			
		UNLATCHED	LATCHED & STROBED	LATCHED	LATCHED & STROBED		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X[2]
	4	X		X			X[2]

NOTES: 1. Part of Port 3 must be used as a control port when either Port 1 or Port 2 are used as a latched and strobed input or a latched and strobed output or Port 1 is used as a bidirectional port.

2. Part of Port 6 must be used as a control port when either Port 4 or Port 5 are used as a latched and strobed input or a latched and strobed output or Port 4 is used as a bidirectional port.

SPECIFICATIONS

MEMORY ADDRESSING

ROM/EPROM

4K segments starting at any jumper-selectable base address on a 4K byte boundary (e.g., 0000_H, 1000_H, ... $F000_H$)

RAM:

4K, 8K, 16K segments starting at any jumper-selectable base address on a 4K byte boundary (e.g., 0000_H, 1000_H, ... $F000_H$)[3]

Note: 3. Base address 7000_H not allowed for SBC 108. Base address $5000_H \rightarrow 7000_H$ not allowed for SBC 116.

MEMORY CAPACITY

ROM/PROM: 4K bytes (sockets only)
RAM: 4K bytes for SBC 104, 8K bytes for SBC 108, 16K bytes for SBC 116.

MEMORY RESPONSE TIME

Memory	Access (ns)	Cycle (ns)
RAM	575 max*	675 max*
EPROM/ROM	465 max	685 max

*Without Refresh Interruption.

I/O ADDRESSING

Port	1	2	3	4	5	6	8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
Address	X4	X5	X6	X8	X9	XA	X7	XB	XC	XD

Note: X is any hex digit assigned by jumper selection.

I/O TRANSFER RATE

Parallel: Read or Write cycle time 760 ns max
Serial: (USART)

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

SERIAL COMMUNICATIONS CHARACTERISTICS

Synchronous:
- 5–8 bit characters
- Internal or external character synchronization
- Automatic Sync Insertion

Asynchronous:
- 5–8 bit characters
- Break characters generation
- 1, 1½, or 2 stop bits
- False start bit detectors

INTERRUPTS

Eight interrupt request lines may originate from the Programmable Peripheral Interface (4 lines), the USART (2 lines) or user specified devices via the I/O edge connector (2 lines) or Interval Timer.

INTERRUPT REGISTER ADDRESSES

Interrupt Mask Register	X1
Interrupt Status Register	X0

Note: X is any hex digit assigned by jumper selection.

TIMER INTERVAL

1.003 ms ±0.1% when 110 Baud Rate is selected
1.042 ms ±0.1% for all other Baud Rates

INTERFACES

Bus: All signals TTL compatible
Parallel I/O: All signals TTL compatible
Serial I/O: RS232C
Interrupt Requests: All TTL compatible

CONNECTORS

Interface	No. of Pins	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Aux Power[4]	60	0.1	AMP PE5-14559 or TI H311130

Note: 4. Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM or MDS packaging.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm) Depth: 0.50 in. (1.27 cm)
Height: 6.75 in. (17.15 cm) Weight: 14 oz (397.3 gm)

ELECTRICAL CHARACTERISTICS[5]

Average DC Current:

		Without EPROM[6]	With EPROM[7]	RAM[8]
V_{CC} = +5V ±5%	I_{CC} = 2.85A max	3.6A max	600 mA max
V_{DD} = +12V ±5%	I_{DD} = 450 mA max	700 mA max	400 mA max
V_{BB} = –5V ±5%	I_{BB} = 3 mA max	180 mA max	3 mA max
V_{AA} = –12V ±5%	I_{AA} = 60 mA max	60 mA max	Not Used

Notes:
5. All current values given here include RAM power.
6. Does not include power required for optional EPROM, I/O drivers, and I/O terminators.
7. With four 8708 EPROMs and eight 220Ω/330Ω Input terminators installed, all terminator inputs low.
8. RAM chips and RAM control logic (powered via Auxiliary Power Bus).

AUXILIARY POWER

An Auxiliary Power Bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this Auxiliary RAM Power Bus is made via jumpers on the board.

MEMORY PROTECT

An active-low TTL compatible MEMORY PROTECT signal is brought out on the Auxiliary connector which, when asserted, disables Read/Write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

LINE DRIVERS AND TERMINATORS

I/O Drivers:

The following line drivers and terminators are all compatible with the I/O driver sockets on the SBC 104/108/116.

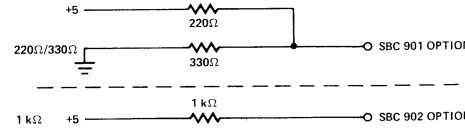
Driver	Characteristic	Sink Current (mA)	Driver	Characteristic	Sink Current (mA)
7438	I,OC	48	7409	NI,OC	16
7437	I	48	7408	NI	16
7432	NI	16	7403	I,OC	16
7426	I,OC	16	7400	I	16

Note: I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 25 mA totem-pole drivers and 1 kΩ terminators.

I/O Terminators:

Terminators: 220Ω/330Ω divider or 1 kΩ pull-up.

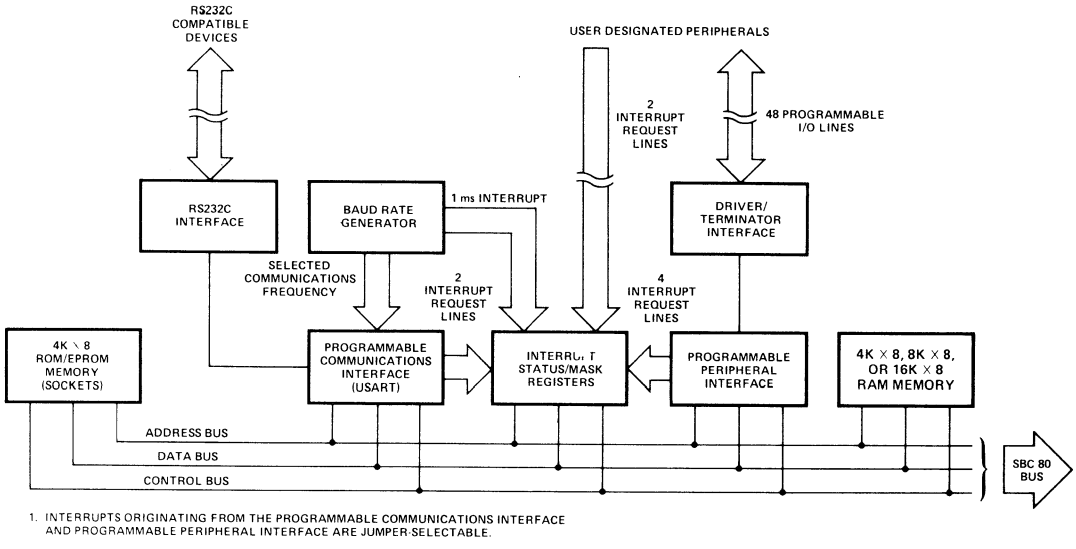


Bus Drivers:

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Commands	Tri-State	25

ENVIRONMENTAL

Operating Temperature: 0°C to +55°C.



1. INTERRUPTS ORIGINATING FROM THE PROGRAMMABLE COMMUNICATIONS INTERFACE AND PROGRAMMABLE PERIPHERAL INTERFACE ARE JUMPER-SELECTABLE.

SBC 104/108/116 BLOCK DIAGRAM

SBC 416 16K PROM EXPANSION BOARD

Allows SBC 80 EPROM/ROM expansion through direct bus interface

Sockets for up to 16K bytes of interchangeable Intel® 8308 maksed ROM or 8708 programmable and erasable PROM

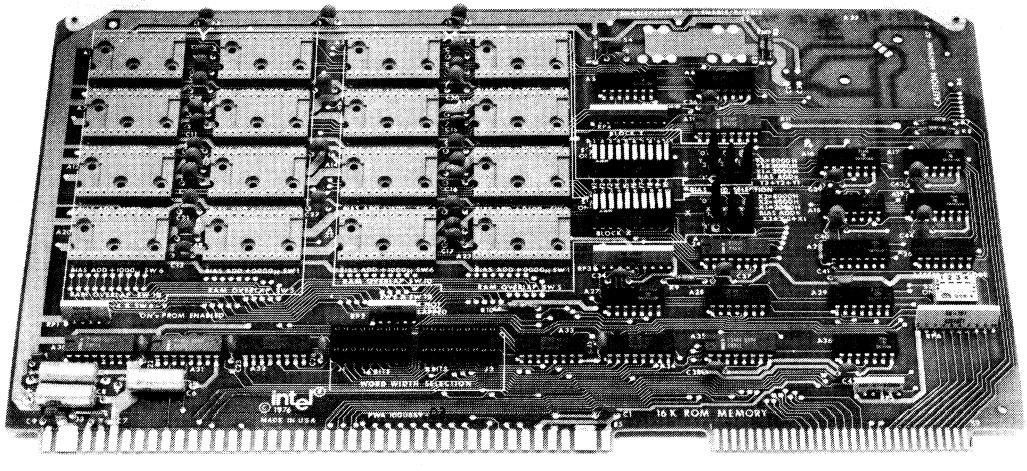
Switches to enable or disable each memory block

Jumper selectable addresses for each 8K block

Buffered address and data lines

The SBC-416 is a member of Intel's complete line of SBC 80 memory and I/O expansion boards. The SBC-416 interfaces directly to any SBC 80 Single Board Computer, via the System bus, to expand ROM/PROM memory capacity.

The board contains 16 sockets that can house either Intel® 8308 masked ROMs or Intel 8708 programmable and erasable EPROMs. ROM/PROM memory can be added in 1K byte increments. The SBC-416 contains a set of jumpers that allow the selection of the base address of independent 8K memory blocks, to begin on any 8K boundary. Switches are used to enable on-board memory in 1K block increments.



MICRO-COMPUTER SYSTEMS

SPECIFICATIONS

WORD SIZE
8 bits

MEMORY SIZE
Sockets for up to 16K bytes. Memory may be added in 1K byte increments.

COMPATIBLE INTEL MEMORY
ROM:
8308
PROM:
8708

INTERFACE
All address, data, and command signals are TTL compatible and SBC 80 Bus compatible.

ADDRESS SELECTION
Switches and jumpers allowing the selection of a base address for each independent 8K block of memory, on any 8K boundaries.

ELECTRICAL CHARACTERISTICS
DC Power:

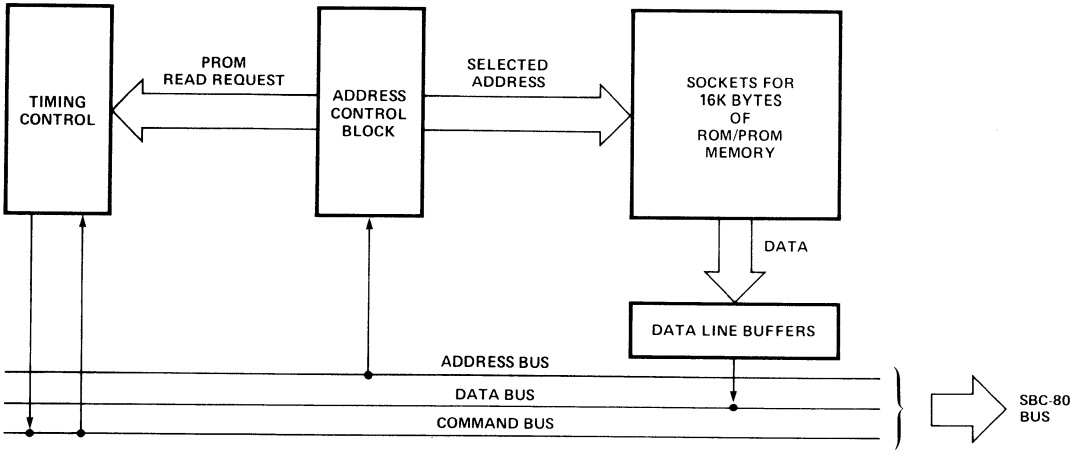
	Without Memory	With 8308		With 8708	
		Typ	Max	Typ	Max
+5V	0.75A	0.77A	0.79A	0.85A	0.91A
-5V	—	0.001A	0.010A	0.48A	0.75A
+12V	—	0.58A	0.96A	0.80A	1.04A

CONNECTOR
86-pin double-sided PC edge connector with 0.156-inch (0.40 cm) contact centers.

Mating Connector: Control Data VPB01E43A00A1.

PHYSICAL CHARACTERISTICS
Width: 12.00 in. (30.40 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 12 oz. (340.5 gm)

ENVIRONMENT
Operating Temperature: 0°C to 55°C



SBC 416 BLOCK DIAGRAM

MICRO-COMPUTER SYSTEMS

SBC 508 I/O EXPANSION BOARD

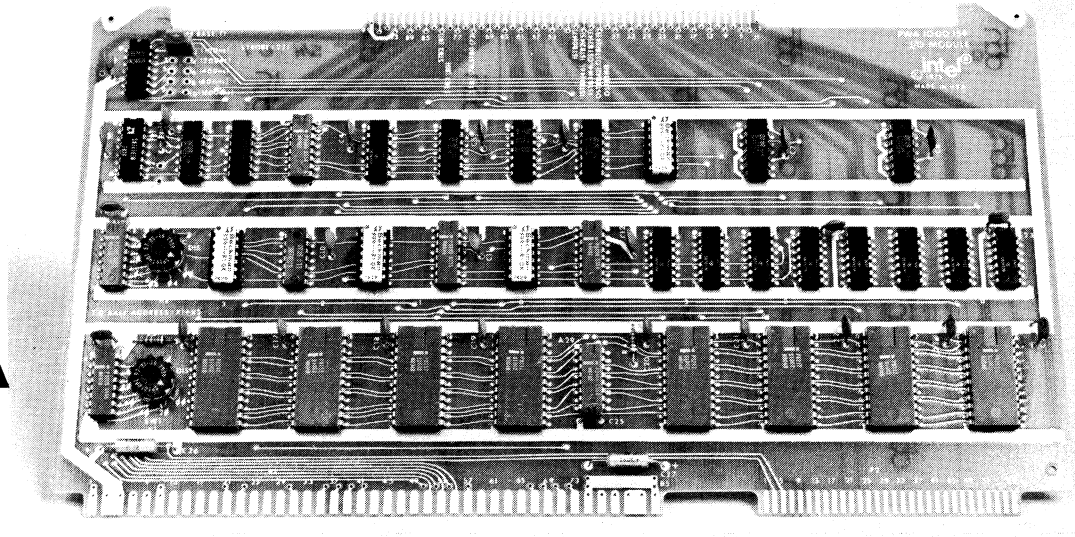
- SBC-80 I/O expansion via direct bus interface
- Four 8-bit terminated input ports
- Four 8-bit output ports with buffered TTL drivers
- Selectable latched or unlatched input ports
- Latched outputs with selectable width strobes
- Switch selectable I/O port addresses

The SBC-508 is a member of Intel's complete line of SBC-80 memory and I/O expansion boards. The SBC-508 interfaces directly to any SBC-80 single board computer, via the system bus, to expand input and output port capacity.

Four 8-bit terminated input ports are contained on the board. Data is gated into the port while the strobe is present and latched if the strobe is removed.

The SBC-508 contains four 8-bit output ports. All output lines are driven by TTL level buffer drivers that reside on the board. Output data is latched. A strobe signal, of jumper selectable width, is sent to the peripheral device during an output operation.

Address selection is accomplished using two resident rotary switches, which select one of sixty-four unique base addresses for all input and output ports. The board operates with a single +5 volt power supply.



SPECIFICATIONS

WORD SIZE
8 bits

CAPACITY
Four 8-bit input ports; four 8-bit output ports.

I/O INTERFACE CHARACTERISTICS
I/O Line Driver Sink Current: 48 mA
I/O Line Terminator Load: 1kΩ pull-up.
Inputs: Data is positive relative to data bus.
Outputs: Data is positive relative to data bus.
Output Strobe: Jumper-selectable to 100, 200, 400, 800 or 1600 ns pulse widths.
All I/O interface data and control signals are TTL levels.

BUS INTERFACE CHARACTERISTICS
All data, address, and control signals are TTL compatible.

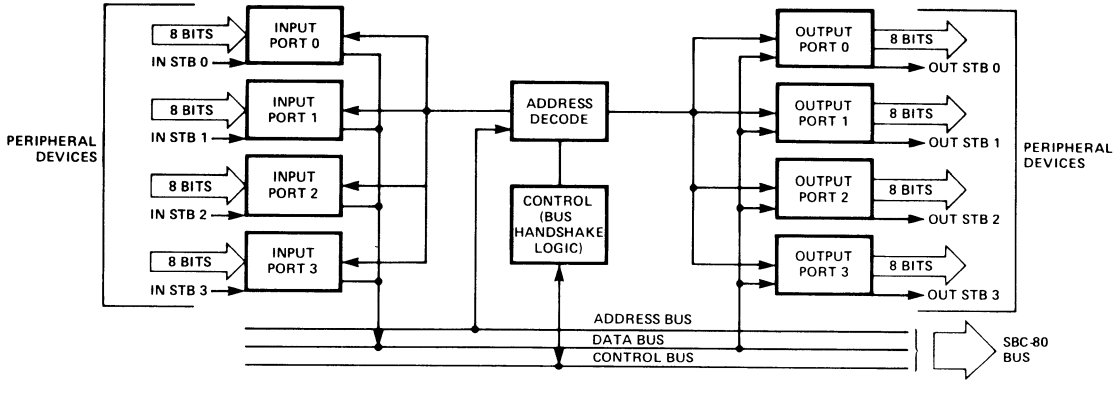
ADDRESS SELECTION
Input and output ports are accessed as four sequential addresses that start in one of 64 switch-selectable locations between 00 and FC_{16}.

CONNECTORS
Bus:
86-pin double-sided PC edge connector with 0.156-inch contact centers.
Mating Connector: Control Data VPB01E43A00A1.
I/O:
100-pin double-sided PC edge connector with 0.1-inch contact centers.
Mating Connector: Viking 3VH50/1JN5.

PHYSICAL CHARACTERISTICS
Width:	12.00 in.	(30.48 cm)
Height:	6.75 in.	(17.15 cm)
Depth:	0.50 in.	(1.27 cm)
Weight:	12 oz.	(415.2 gm)

ELECTRICAL CHARACTERISTICS
DC Power:
V_{CC} = +5V ±5%
I_{CC} = 2.6A max; 1.9A typ.

ENVIRONMENT
Operating Temperature: 0°C to 55°C



I/O EXPANSION BOARD BLOCK DIAGRAM

SBC 517 COMBINATION I/O EXPANSION BOARD

I/O addressing and connectors directly compatible with SBC 104, SBC 108, and SBC 116 Combination Boards

48 programmable I/O lines with sockets for interchangeable line drivers and terminators

Synchronous/Asynchronous communications interface with RS232C drivers and receivers

Eight maskable interrupt request lines with a pending interrupt register

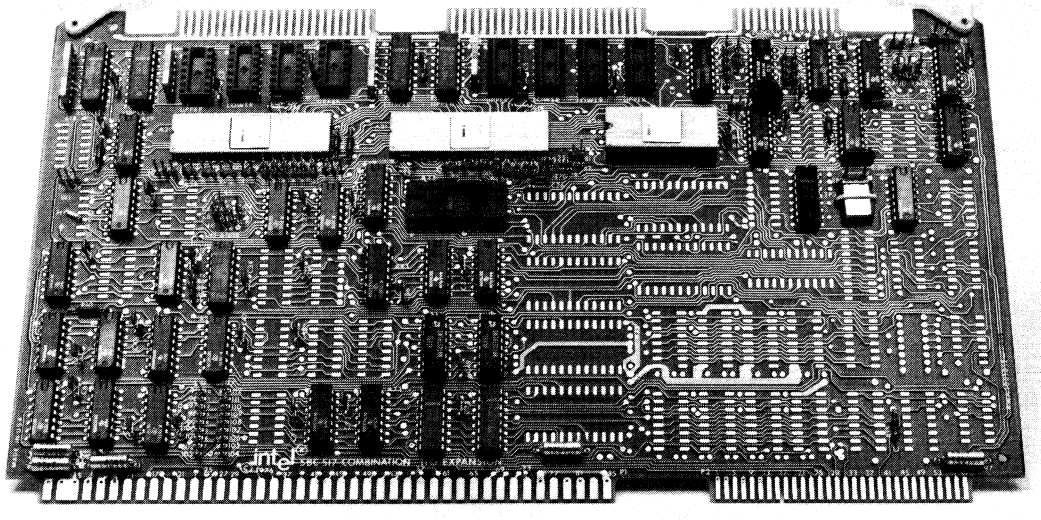
1 ms interval timer

The SBC 517 is a member of Intel's complete line of SBC 80 memory and I/O expansion boards. The board interfaces directly with any SBC 80 Single Board Computer, via the system bus, to expand serial and parallel I/O capacity.

The combination I/O board contains 48 programmable parallel I/O lines. The system software is used to configure the I/O lines to meet a wide variety of system peripheral requirements. The flexibility of the I/O interface is significantly enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application.

A programmable RS232C communications interface is provided on the SBC 517. This interface may be programmed by the system software to provide virtually any asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). A comprehensive RS232C interface to CRTs, RS232C compatible cassettes, and asynchronous and synchronous modems is thus included on the board.

An on-board register contains the status of eight interrupt request lines which may be interrogated from the system bus, and each interrupt request line is maskable under program control. The SBC 517 also contains a jumper-selectable 1 ms interval timer and interface logic for eight interrupt request lines.



The 48 programmable I/O lines on the SBC 517 are implemented utilizing two Intel® 8255 Programmable Peripheral Interfaces. The system software is used to configure these programmable I/O lines in any of the combinations of unidirectional input/output, and bidirectional ports indicated in Table 1. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, round, or woven cable.

Typical I/O Read access time is 280 nanoseconds. Typical I/O Read cycle time is 600 nanoseconds.

The programmable communications interface on the SBC 517 is provided by an Intel® 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART). The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and asynchronous serial transmission rate are all under program control. The 8251 provides full duplex, double-buffered transmit and receive capability, and parity, overrun, and framing error detection are all incorporated in the USART. The comprehensive RS232C interface on the board provides a direct interface to RS232C compatible equipment. The RS232C serial data lines and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cables.

The SBC 530 Teletypewriter Adapter provides an optically isolated interface for those systems requiring a 20 mA current loop. The SBC 530 may be used to interface the SBC 517 Combination I/O Board to teletypewriters and other 20 mA current loop equipment.

Interrupt requests may originate from eight sources. Four jumper-selectable interrupt requests can be automatically generated by the Programmable Peripheral Interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Two jumper-selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). These six interrupt request lines are all maskable under program control. Two interrupt request lines may be interfaced directly from user designated peripheral devices via the I/O edge connector. An on-board register contains the status of all eight interrupt request lines, and may be interrogated by the CPU. Each interrupt request line is maskable under program control. Routing for the eight interrupt request lines is jumper-selectable. They may be ORed to provide a single interrupt request line for the SBC 80/10, or they may be individually provided to the system bus for use by the SBC 80/20 Priority Interrupt Controller.

Each board contains a jumper-selectable 1 ms interval timer. The timer is enabled by jumpering one of the interrupt request lines from the I/O edge connector to a 1 ms interval interrupt request signal originating from the baud rate generator.

TABLE 1

INPUT/OUTPUT PORT MODES OF OPERATION

PORTS	NO. OF LINES	MODE OF OPERATION					
		UNIDIRECTIONAL				BIDIRECTIONAL	CONTROL
		INPUT		OUTPUT			
		UNLATCHED	LATCHED & STROBED	LATCHED	LATCHED & STROBED		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X[2]
	4	X		X			X[2]

NOTES:

1. Part of Port 3 must be used as a control port when either Port 1 or Port 2 are used as a latched and strobed input or a latched and strobed output port or Port 1 is used as a bidirectional port.
2. Part of Port 6 must be used as a control port when either Port 4 or Port 5 are used as a latched and strobed input or a latched and strobed output port or Port 4 is used as a bidirectional port.

SPECIFICATIONS

I/O ADDRESSING

Port	1	2	3	4	5	6	8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
Address	X4	X5	X6	X8	X9	XA	X7	XB	XC	XD

Note: X is any Hex digit assigned by jumper selection.

I/O TRANSFER RATE

Parallel: Read or Write cycle time 760 ns max
Serial: (USART)

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

SERIAL COMMUNICATIONS CHARACTERISTICS

Synchronous:
- 5–8 bit characters
- Internal or external character synchronization
- Automatic Sync Insertion

Asynchronous:
- 5–8 bit characters
- Break characters generation
- 1, 1½, or 2 stop bits
- False start bit detectors

INTERRUPTS

Eight interrupt request lines may originate from the Programmable Peripheral Interface (4 lines), the USART (2 lines) or user specified devices via the I/O edge connector (2 lines) or Interval Timer.

INTERRUPT REGISTER ADDRESSES

Interrupt Mask Register	X1
Interrupt Status Register	X0

Note: X is any Hex digit assigned by jumper selection.

TIMER INTERVAL

1.003 ms ±0.1% when 110 Baud Rate is selected
1.042 ms ±0.1% for all other Baud Rates

INTERFACES

Bus: All signals TTL compatible
Parallel I/O: All signals TTL compatible
Serial I/O: RS232C
Interrupt Requests: All TTL compatible

CONNECTORS

Interface	No. of Pins	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Auxiliary[1]	60	0.1	AMP PE5-14559 or TI H311130

Note 1: Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM or System packaging. Auxiliary connector is used for test purposes only.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 14 oz (397.3 gm)

ELECTRICAL CHARACTERISTICS

Average DC Current:

V_{CC} = +5V ±5% I_{CC} = 2.4 mA max
V_{DD} = +12V ±5% I_{DD} = 40 mA max
V_{AA} = −12V ±5% I_{AA} = 60 mA max

Note: Does not include power required for optional I/O drivers and I/O terminators. With eight 220Ω/330Ω Input terminators installed, all terminator inputs low.

LINE DRIVERS AND TERMINATORS

I/O Drivers:

The following line drivers and terminators are all compatible with the I/O driver sockets on the SBC 517.

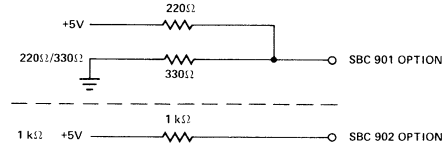
Driver	Characteristic	Sink Current (mA)	Driver	Characteristic	Sink Current (mA)
7438	I,OC	48	7409	NI,OC	16
7437	I	48	7408	NI	16
7432	NI	16	7403	I,OC	16
7426	I,OC	16	7400	I	16

Note: I = inverting; Ni = non-inverting; OC = open collector

Ports 1 and 4 have 25 mA totem-pole drivers and 1 kΩ terminators.

I/O Terminators:

Terminators: 220Ω/330Ω divider or 1 kΩ pull-up.

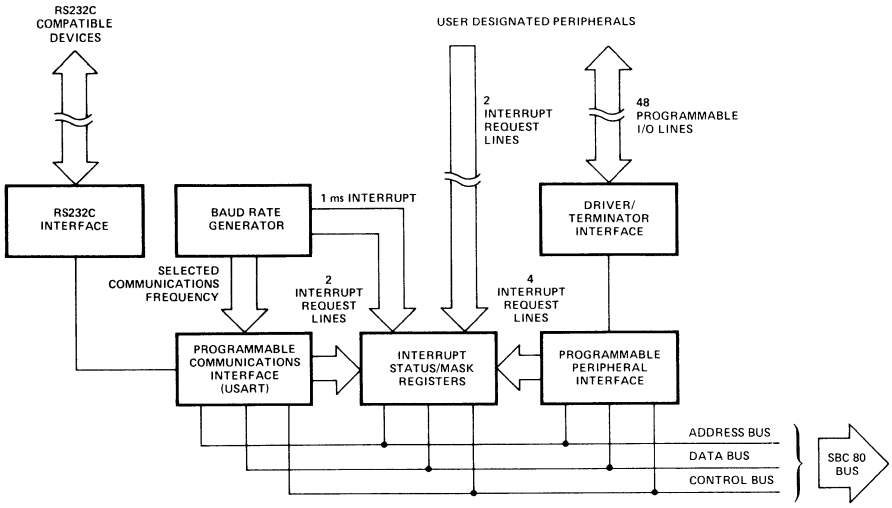


Bus Drivers:

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Commands	Tri-State	25

ENVIRONMENTAL

Operating Temperature: 0°C to +55°C



NOTES: INTERRUPTS ORIGINATING FROM THE PROGRAMMABLE COMMUNICATIONS INTERFACE AND PROGRAMMABLE PERIPHERAL INTERFACE ARE JUMPER-SELECTABLE.

SBC 517 BLOCK DIAGRAM

SBC 519 PROGRAMMABLE I/O EXPANSION BOARD

SBC 80 I/O expansion via direct bus interface

72 programmable I/O lines with sockets for interchangeable line drivers and terminators

Eight maskable interrupt request lines with priority encoded and programmable interrupt algorithms

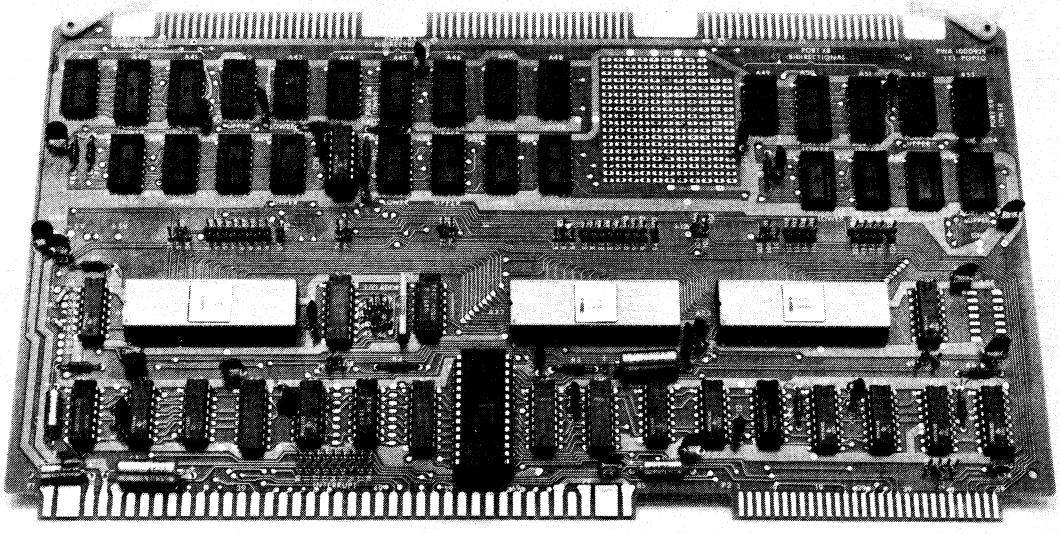
Jumper selectable I/O port addresses

Jumper selectable 0.5, 1.0, 2.0 or 4.0 msec interval timer

The SBC 519 is a member of Intel's complete line of SBC 80 memory and I/O expansion boards. The SBC 519 interfaces directly to any SBC 80 single board computer, via the system bus, to expand input and output port capacity.

The SBC 519 provides 72 programmable I/O lines. The system software is used to configure the I/O lines to meet a wide variety of peripheral requirements. The flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application.

Address selection is accomplished using wire-wrap jumpers which select one of 16 unique base addresses for the input and output ports. The board operates with a single +5 volt power supply.



The 72 programmable I/O lines on the SBC 519 are implemented utilizing three Intel® 8255 Programmable Peripheral Interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output, and bidirectional ports indicated in Table 1. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. The 72 programmable I/O lines and signal ground lines are brought out to three 50-pin edge connectors that mate with flat, round, or woven cable.

Typical I/O Read access time is 350 nanoseconds. Typical I/O Read/Write cycle time is 450 nanoseconds.

An interval timer is provided on the SBC 519 which may be used to generate Real Time Clocking in systems requiring the periodic monitoring of I/O functions. The timing interval is derived from the SBC 80 BUS CCLK (Constant Clock) and the timing interval is jumper selectable. Intervals of 0.5, 1.0, 2.0, and 4.0 milliseconds may be selected when an SBC 80 Single Board Computer is used to generate the CCLK. Other timing intervals may be generated if the user provides a separate CCLK reference in the system.

An Intel® 8259 Programmable Interrupt Controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 2, a selection of three priority processing algorithms is available to the system designer so that the manner in which requests are serviced may be configured to match system requirements. Priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel I/O interfaces, the interval timer, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and if appropriate, issues an interrupt to the System Master. Any combination of interrupt levels may be masked through storage, via software, of a single byte to the Interrupt Mask Register of the PIC.

Interrupt requests may originate from 10 sources. Six jumper selectable interrupt requests can be automatically generated by the Programmable Peripheral Interfaces when a byte of information is ready to be transferred to the System Master (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Three interrupt request lines may be interfaced to the PIC directly from user designated peripheral devices via the I/O edge connectors. One interrupt request may be generated by the interval timer.

The PIC interrupt request output line may be jumper-selected to drive any of the nine interrupt lines on the SBC 80 BUS. Any of the on-board request lines may also drive any SBC 80 BUS interrupt line directly via jumpers and buffers on the board.

TABLE 2

INTERRUPT PRIORITY OPTIONS

ALGORITHM	OPERATION
FULLY NESTED	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
AUTO-ROTATING	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
SPECIFIC PRIORITY	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.

TABLE 1

INPUT/OUTPUT PORT MODES OF OPERATION

PORTS	NO. OF LINES	MODE OF OPERATION					
		UNIDIRECTIONAL				BIDIRECTIONAL	CONTROL
		INPUT		OUTPUT			
		UNLATCHED	LATCHED & STROBED	LATCHED	LATCHED & STROBED		
1,4,7	8	X	X	X	X	X	
2,5,8	8	X	X	X	X		
3,6,9	4	X		X			X[1,2,3]
	4	X		X			X[1,2,3]

NOTES:

1. Part of Port 3 must be used as a control port when either Port 1 or Port 2 are used as a latched and strobed input or a latched and strobed output port or Port 1 is used as a bidirectional port.
2. Part of Port 6 must be used as a control port when either Port 4 or Port 5 are used as a latched and strobed input or a latched and strobed output port or Port 4 is used as a bidirectional port.
3. Part of Port 9 must be used as a control port when either Port 7 or Port 8 are used as a latched and strobed input or a latched and strobed output port or Port 7 is used as a bidirectional port.

SPECIFICATIONS

I/O ADDRESSING

Port	1	2	3	8255 No. 1 Control	4	5	6	8255 No. 2 Control	7	8	9	8255 No. 3 Control
Address	X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	XA	XB

INTERRUPTS

Register Addresses (Hex notation, I/O address space)

Interrupt Request Register	XD
In-Service Register	XC
Mask Register	XD
Command Register	XC
Block Address Register	XD
Status (Polling Register)	XC

Note: Several registers have the same physical address, sequence of access and one data bit of control word determines which register will respond.

Ten interrupt request lines may originate from the Programmable Peripheral Interface (6 lines), or user specified devices via the I/O edge connector (3 lines), or Interval Timer (1 line).

INTERVAL TIMER

Output Register

Timer Interrupt Register output is cleared by an OUTput instruction to I/O address XE or XF.[4]

Timing Intervals

0.500, 1.000, 2.000, and 4.000 msec ±1%; Jumper Selectable.[5]

Notes: 4. X is any Hex digit assigned by jumper selection.

5. Assumes SBC 80 CCLK Frequency of 9.216 MHz ±1%.

INTERFACES

Bus:	All signals TTL compatible
Parallel I/O:	All signals TTL compatible
Interrupt Requests:	All TTL compatible

CONNECTORS

Interface	No. of Pins	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Auxiliary[2]	60	0.1	AMP PE5-14559 or TI H311130

Note 1: Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM or System packaging.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 14 oz (397.3 gm)

ELECTRICAL CHARACTERISTICS[1]

Average DC Current

	Without Termination[6]	With Termination[7]
V_{CC} = +5V ±5%	I_{CC} = 1.5A max	3.5A max

Notes: 6. Does not include power required for optional I/O drivers and I/O terminators.

7. With 18 220Ω/330Ω Input terminators installed, all terminator inputs low.

LINE DRIVERS AND TERMINATORS

I/O Drivers

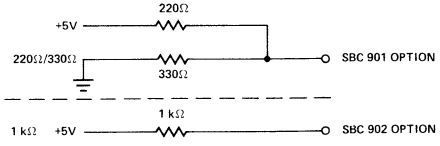
The following line drivers and terminators are compatible with all the I/O driver sockets on the SBC 519.

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note: I = inverting; NI = non-inverting; OC = open-collector.

I/O Terminators

Terminators: 220Ω/330Ω divider or 1 kΩ pull-up.



Ports 1, 4, and 7 may use any of the drivers or terminiators shown above for unidirectional (Input or Output) port configurations. Either terminator and the following bidirectional drivers and terminators may be used for Ports 1, 4, and 7 when these ports are used as bidirectional ports.

Bidirectional Drivers

Driver	Characteristic	Sink Current (mA)
Intel® 8216	NI,TS	25
Intel ® 8226	I,TS	50

Note: I = inverting; NI = non-inverting; TS = three-state.

Terminators (for Ports 1, 4, and 7 when used as bidirectional ports)

Supplier	Product Series
CTS	760-
Dale	LDP14-02
Beckman	899-1

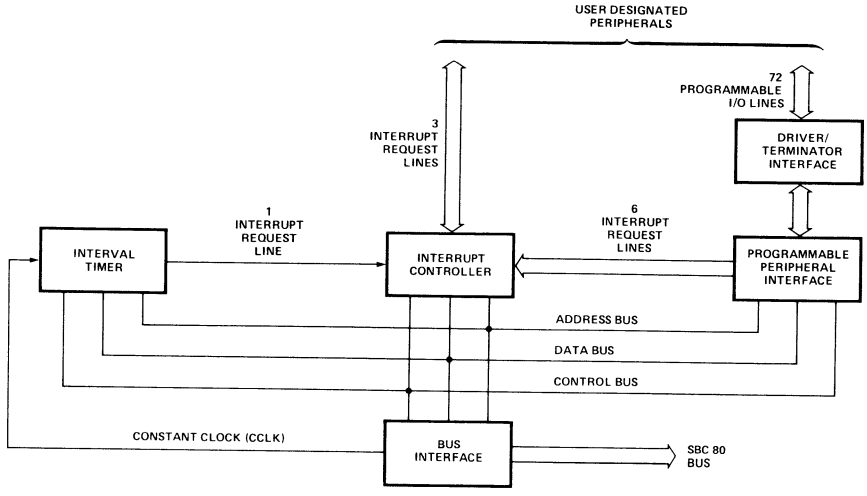
Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Commands	Tri-State	25

ENVIRONMENTAL

Operating Temperature: 0°C to +55°C

MICRO COMPUTER SYSTEMS

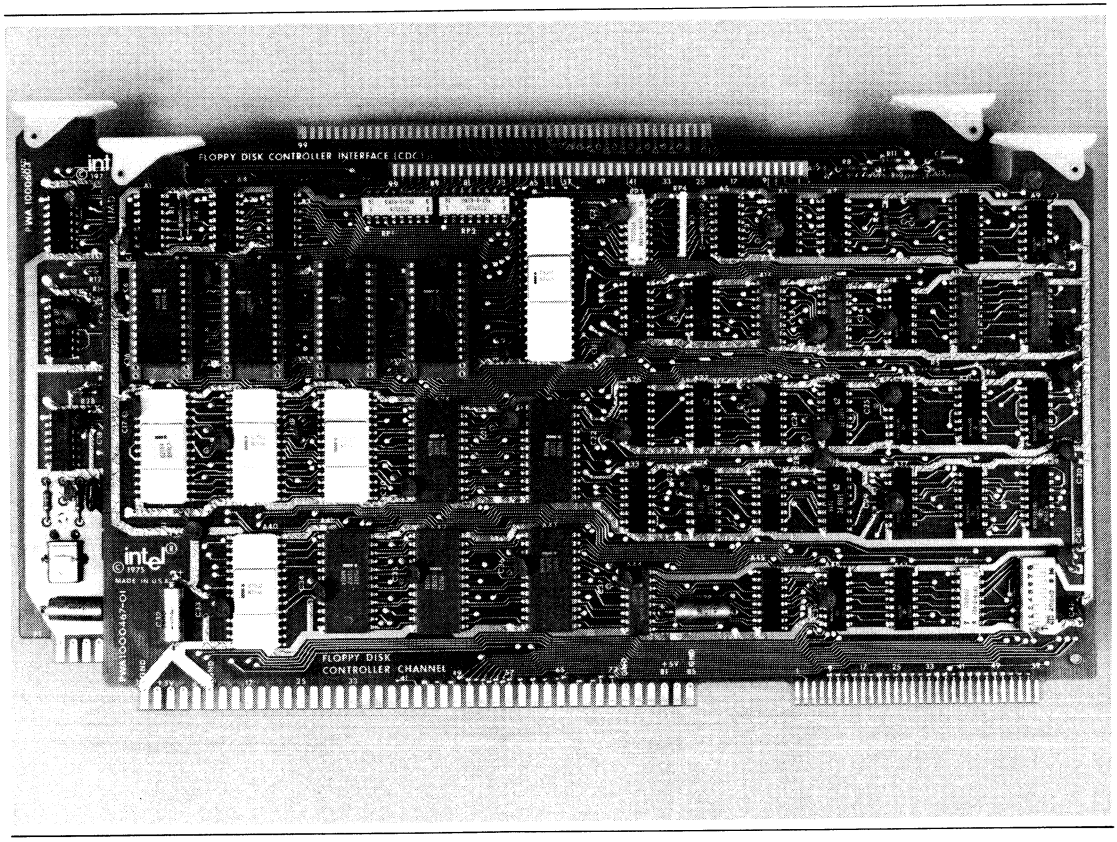


SBC 519 BLOCK DIAGRAM

SBC 201 DISKETTE CONTROLLER

- Provides interface for high-speed random access bulk storage capability for Intel® OEM Computers
- Provides microprocessor control of two flexible diskette drives
- Microprogrammed for maximum flexibility and easy software development
- Compatible with majority of diskette drives, including Shugart and Control Data
- Complete CRC data checking
- Data addressed using IBM soft-sectored format which allows 256K bytes of data capacity per diskette
- SBC bus compatible — plugs into standard System 80 Backplane or SBC 604/614 Cardcage
- Optional Go/No Go Diagnostic

The SBC 201 Diskette Controller is a high-speed, modular set of boards which provides the OEM with a powerful and easy to use control technique for the interfacing of Intel® OEM Computers with industry standard flexible diskettes. The Diskette controller is directly compatible with the entire family of System 80 and SBC 80 OEM computers, and will interface directly with the majority of the flexible diskette drives in use today.



The SBC 201 Diskette Controller provides an easy to use interface for the OEM using Intel's OEM computers and other manufacturer's flexible diskettes. The controller enables the OEM to develop his system software in a simple, straightforward manner. All DMA logic is provided, so no additional boards or circuitry are required, and either one or two flexible diskette drivers may be interfaced to the Intel Computer with each SBC 201. The controller is implemented with Intel's powerful Series 3000 Bipolar Microprocessor Set. The controller facilitates recording all data in the IBM-compatible soft-sector format. The controller consists of two boards which may reside in the System 80 chassis, the SBC 604 or 614 Modular Cardcage, or in the OEM's own custom designed, Intel Bus-compatible Backplane. The Channel Board and the Interface Board are discussed in detail below.

CHANNEL BOARD

The Channel Board is the primary control module within the diskette controller. The Channel Board receives, decodes, and responds to channel commands from the Central Processor Unit (CPU) in the Intel OEM Computer System. The Channel Board can access a block of system memory to determine the particular diskette operations to be performed and fetch the parameters required for the successful completion of the specified operation.

The control functions of the Channel Board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 Central Processing Elements (2-bit slice per CPE), a 3001 Microprogram Control Unit, and 512 X 32 bits of 3604 programmable read-only memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the Channel Board.

INTERFACE BOARD

The Interface Board provides the SBC 201 Diskette Controller with a means of communication with the diskette drives, as well as with the Intel OEM Computer System Bus. Under control of the microprogram being executed on the Channel Board, the Interface Board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), cause the head to move to the proper track and verify successful operation. The Interface Board accepts the data being read off the diskette, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the Channel Board.

During write operations, the Interface Board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

When the diskette controller requires access to the system memory, the Interface Board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The Interface Board also acknowledges I/O commands as required by the Intel OEM Computer Bus.

The diskette controller is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

PROGRAMMING WITH THE SBC FLEXIBLE DISKETTE CONTROLLER

The controller has been designed to make programming very easy, but also with unique capabilities which allow the OEM to generate sophisticated software when required. All diskette operations are initiated by Intel OEM Computer, with standard I/O commands. Once initiated, however, the Diskette Controller completes the specified operation without further intervention on the part of the CPU. From the CPU's point of view, there are only three general steps required to complete any diskette operation:

1. The CPU must prepare and store in system memory an I/O Parameter Block (IOPB) for each operation to be performed. If multiple operations are desired, the IOPBs can be linked together in the proper order.
2. The CPU then passes the memory address of the first (or only) IOPB to the diskette controller.
3. The CPU must process the resultant information from the diskette controller upon completion of the operation(s).

The preparation of the IOPB(s) by the CPU requires no interaction with the diskette controller. The IOPB is prepared as any block of data in memory would be prepared. The 10-byte parameter block must adopt the following format:

Byte	1	Channel Word
	2	Diskette Instruction
	3	Number of Records
	4	Track Address
	5	Sector Address
	6	Buffer Address (Lower)
	7	Buffer Address (Upper)
	8	Block Number
	9	Next IOPB Address (Lower)
	10	Next IOPB Address (Upper)

The channel word or command provides the controller with information which:

1. Determines the method of assigning logical sector addresses
2. Enables or disables a series of possible diskette interrupts
3. Determines if the parameter block is properly prepared
4. Determines the length of the data word to be transferred

COMPATIBLE INTERFACE CABLES

For the convenience of the OEM, Intel provides cables for use with specific manufacturer's drives. The SBC 951 Cable may be used to connect the diskette controller to a Shugart Model 800/800R Flexible Diskette Drive. The SBC 952 may be used to connect the controller to a Control Data Model 9404 Flexible Diskette Drive. The OEM could, of course, fabricate his own cabling for these drives or any other flexible diskette drives.

GO/NO GO DIAGNOSTIC

For the convenience of the OEM, Intel makes available a diskette exerciser and monitor program which facilitates the checkout and debugging of OEM built systems using

Intel OEM Computers and Diskette Controllers. The SBC 915 and SBC 925 Go/No Go Diagnostic programs are available on four 1K byte ROMs which can be installed in the PROM/ROM memory section of the Intel Computer. The programs include commands to display and alter main memory and registers, insert instructions, move main memory, substitute main memory, and to exercise the flexible diskette drives by reading and/or writing individual sectors, reading sequentially sector-to-sector and track-to-track, and writing/reading random sectors and tracks.

The Go/No Go Diagnostic program is designed to give the OEM a convenient means of determining the functionality of his system.

SPECIFICATIONS

MEDIA

Flexible Diskette
One Recording Surface
IBM Soft-Sector Format
77 Tracks/Diskette
26 Sectors/Tracks
128 Bytes/Sector

PHYSICAL CHARACTERISTICS

Mounting: Occupies two slots of System 80 Chassis or SBC 604/614 Cardcage
Height: 6.75 in. (17.15 mm)
Width: 12.00 in. (30.48 mm)
Depth: 0.50 in. each board (1.27 mm)

ELECTRICAL CHARACTERISTICS

DC Power Requirements:
Channel Board: 5V @ 3.75A (typ), 5A (max)
Interface Board: 5V @ 1.5A (typ), 2.5A (max)

ENVIRONMENTAL CHARACTERISTICS

Temperature:
Operating: 0 to 55°C
Non-Operating: -55°C to +85°C
Humidity:
Operating: Up to 90% relative humidity without condensation.
Non-Operating: All conditions without condensation of water or frost.

EQUIPMENT SUPPLIED

FDC Channel Board
FDC Interface Board
Dual Auxiliary Board Connector
Hardware Reference Manual
Reference Schematics

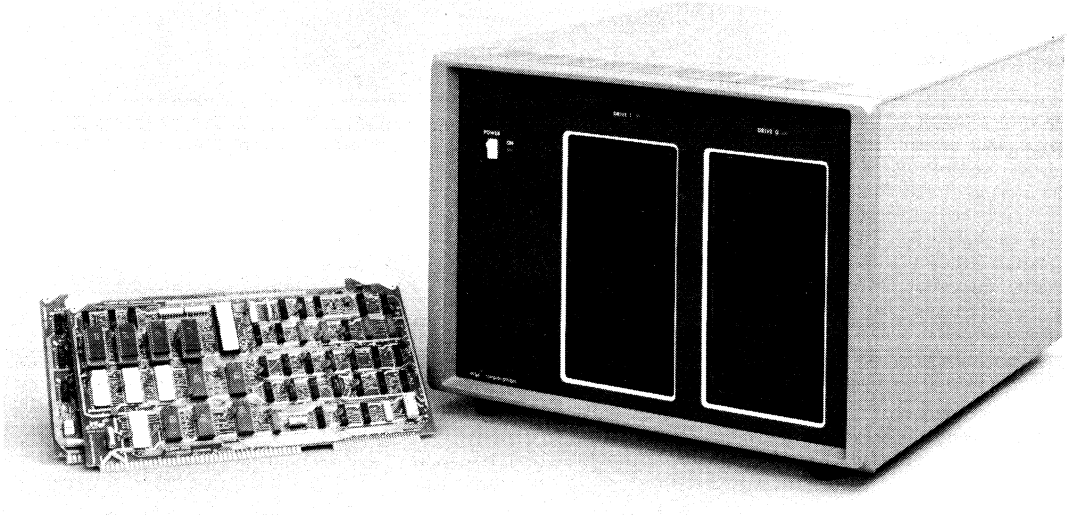
OPTIONAL EQUIPMENT

SBC 915 Go/No Go Diagnostic and Monitor Program for SBC 80/10 and System 80/10
SBC 925 Go/No Go Diagnostic and Monitor Program for SBC 80/20
SBC 951 Cables for Shugart Model 800/800R Diskette Drives
SBC 952 Cables for CDC Model 9404 Diskette Drives

SBC 211/212 DISKETTE HARDWARE SYSTEM

- High-speed, random access bulk storage for Intel's OEM Computer family
- Single-drive or dual-drive packages
- IBM soft-sectored format allowing 256K byte data storage capacity per diskette
- High-speed I/O capability
  - 250 kilobit/sec transfer rate
  - 10 ms track-to-track access time
- Compact chassis design that is RETMA compatible
- Microprogrammed diskette controller allows easy software development
- Complete CRC data checking
- SBC Bus compatible — diskette controller plugs into standard System 80 Backplane or SBC 604/614 Cardcage
- Optional Go/No Go Diagnostic

The SBC 211 and SBC 212 are high-speed, random access bulk storage systems for use with Intel's SBC 80 and System 80 OEM Computers. The SBC 211 is a single-drive diskette system and the SBC 212 is a dual-drive system. Both are complete subsystems with the drives fully packaged in a standard RETMA compatible chassis and with Intel's Diskette Controller. The controller boards simply plug into the System 80 Backplane or the SBC 604/614 Cardcage and interface with standard cable to diskette drives.



HARDWARE

The SBC 211 and 212 Hardware Diskette Systems provide direct access to bulk storage, with an intelligent controller, and up to two diskette drives. Each drive provides 1/4 million bytes of storage with a data transfer rate of 250,000 bits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the Intel® OEM Computer Bus as well as supporting the two diskette drives. The diskette system can record all data in the IBM-compatible soft-sector format.

The SBC diskette controller consists of two boards, the Channel Board and the Interface Board. These two printed circuit boards, residing in the SBC 604/614 Cardcage or System 80, constitute the diskette controller. Each of the system's components are described in more detail in the following paragraphs.

CHANNEL BOARD

The Channel Board is the primary control module within the diskette system. The Channel Board receives, decodes and responds to channel commands from one or more bus masters in this Intel OEM Computer System. The Channel Board can access a block of computer system memory to determine the particular diskette operations to be performed and fetch the parameters required for the successful completion of the specified operation. The control functions of the Channel Board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 Central Processing Elements (2-bit slice per CPE), a 3001 Microprogram Control Unit, and 512 X 32 bits of 3604 programmable read-only memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the Channel Board.

INTERFACE BOARD

The Interface Board provides the SBC 201 Diskette Controller with a means of communication with the diskette drives, as well as with the Intel OEM Computer System Bus. Under control of the microcomputer being executed on the Channel Board, the Interface Board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), cause the head to move to the proper track and verify successful operation. The Interface Board accepts the data being read off the diskette, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the Channel Board.

During write operations, the Interface Board outputs the data clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

When the diskette controller requires access to the system memory, the Interface Board requests and maintains DMA master control of the system bus and generates the appropriate memory command. The Interface Board also acknowledges I/O commands as required by the Intel OEM Computer Bus.

The diskette controller is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

PROGRAMMING WITH THE SBC FLEXIBLE DISKETTE CONTROLLER

The controller has been designed to make programming very easy, but also with unique capabilities which allow the OEM to generate sophisticated software as required.

All diskette operations are initiated by the Intel OEM Computer with standard I/O commands. Once initiated, however, the diskette controller completes the specified operation without further intervention on the part of the CPU. From the CPU's point of view, there are only three general steps required to complete any diskette operation:

1. The CPU must prepare and store in system memory an I/O Parameter Block (IOPB) for each operation to be performed. If multiple operations are desired, the IOPBs can be linked together in the proper order.
2. The CPU then passes the memory address of the first (or only) IOPB to the diskette controller.
3. The CPU must process the resultant information from the diskette controller upon completion of the operation(s).

The preparation of the IOPB(s) by the CPU requires no interaction with the diskette controller. The IOPB is prepared as any block of data in memory would be prepared. The 10-byte parameter block must adopt the following format:

Byte	1	Channel Word
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	3	Number of Records
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	5	Sector Address
	6	Buffer Address (Lower)
	7	Buffer Address (Upper)
	8	Block Number
	9	Next IOPB Address (Lower)
	10	Next IOPB Address (Upper)

The channel word provides the controller with information which:

1. Determines the method of assigning logical sector addresses.
2. Enables or disables a series of possible diskette interrupts.
3. Determines if the parameter block is properly prepared.
4. Determines the length of the data word to be transferred.

GO/NO GO DIAGNOSTIC

For the convenience of the OEM, Intel makes available a diskette exerciser and monitor program which facilitates the checkout and debugging of OEM built systems using Intel® OEM Computers and Diskette Controllers. The SBC 915 and SBC 925 Go/No Go Diagnostic programs are available on four 1K byte ROMs which can be installed in the PROM/ROM memory section of the Intel Computer. The programs include commands to display and alter main memory and registers, insert instructions, move main memory, substitute main memory, and to exercise the flexible diskette drives by reading and/or writing individual sectors, reading sequentially sector-to-sector and track-to-track, and writing/reading random sectors and tracks.

The Go/No Go Diagnostic program is designed to give the OEM a convenient means of determining the functionality of his sytem.

SPECIFICATIONS

ACCESS TIME

Track-to-Track: 10 ms
Head Settling Time: 10 ms
Average Random Positioning Time: 260 ms
Rotational Speed: 360 rpm
Average Latency: 83 ms
Recording Mode: Frequency Modulation

PHYSICAL CHARACTERISTICS

Controller:
- Mounting: Occupies two slots of System 80 Chassis or SBC 604/614 Cardcage
- Height: 6.75 in. (17.15 mm)
- Width: 12.00 in. (30.48 mm)
- Depth: 0.50 in. each board (1.27 mm)

Chassis and Drives:
- Mounting: Table-top or standard 19" RETMA cabinet
- Height: 12.08 in. (30.68 cm)
- Width: 16.88 in. (42.88 cm)
- Depth: 19.0 in. (48.26 cm)
- Weight: 1 drive — 51 lb (23 kg)
  2 drives — 64 lb (29 kg)

ELECTRICAL CHARACTERISTICS

Chassis:
DC Power Supplies:

Voltage	Current
5V	3A ±5%
-5V	600 mA ±5%
24V	4A ±5%

AC Power Requirements:
3-wire input with center conductor (earth ground) tied to chassis.
Single-phase, 115/230 VAC; 50–60 Hz; 160 watts

Controller:
DC Power Requirements:
Channel Board: 5V @ 3.75A (typ), 5A (max)
Interface Board: 5V @ 1.5A (typ), 2.5A (max)

ENVIRONMENTAL CHARACTERISTICS

MEDIA
- Temperature:
  - Operating: 15.6°C to 51.7°C
  - Non-Operating: 5°C to 55°C
- Humidity:
  - Operating: 8 to 8% (wet bulb 29.4°C)
  - Non-Operating: 8 to 90%

DRIVES AND CHASSIS
- Temperatures:
  - Operating: 10°C to 38°C
  - Non-Operating: -35°C to 65°C
- Humidity:
  - Operating: 20% to 90% (wet bulb 26.7°C)
  - Non-Operating: 5% to 95%

CONTROLLER BOARDS
- Temperature:
  - Operating: 0 to 55°C
  - Non-Operating: -55°C to 85°C
- Humidity:
  - Operating: Up to 90% relative humidity without condensation.
  - Non-Operating: All conditions without condensation of water or frost.

EQUIPMENT SUPPLIED

Cabinet, Power Supplies, Line Cord
Diskette Drive(s)
FDC Channel Board
FDC Interface Board
Dual Auxiliary Connector
Flexible Diskette Controller Cable
Peripheral Cable
Hardware Reference Manual
Reference Schematics

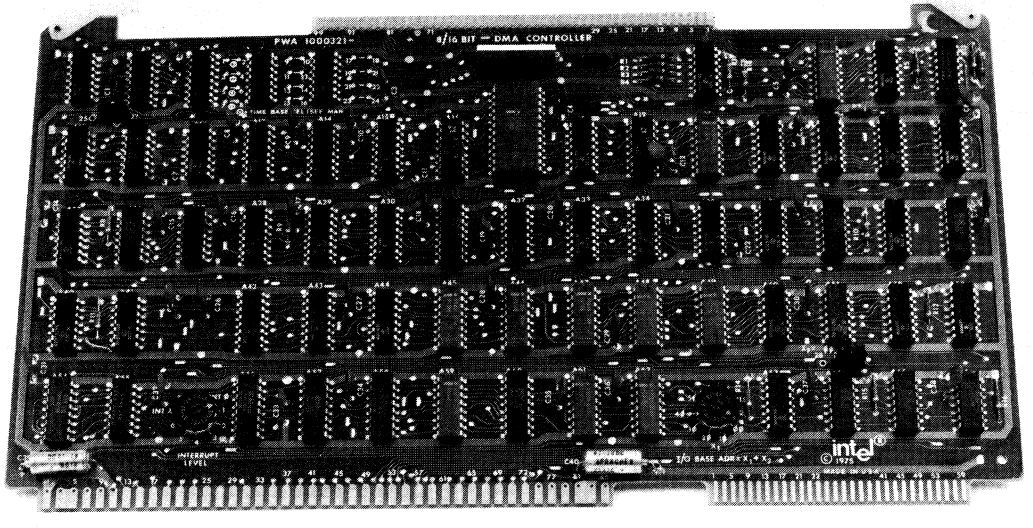
OPTIONAL EQUIPMENT

SBC 915 Go/No Go Diagnostic and Monitor Program for SBC 80/10 and System 80/10
SBC 925 Go/No Go Diagnostic and Monitor Program for SBC 80/20

SBC 501 DIRECT MEMORY ACCESS CONTROLLER

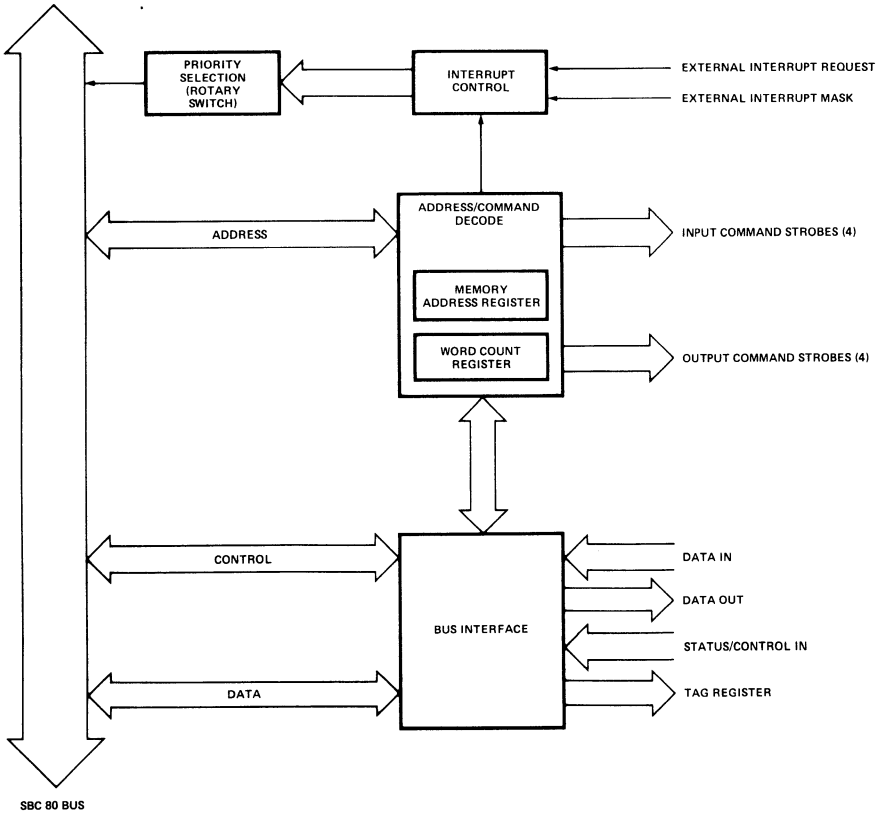
- Directly compatible with Intel® SBC 80 Single Board Computers
- Transfer rate up to 1 million words per second for Block Transfers
- Transfers data up to 330K words per second for Interleaved Transfers
- Block length up to 65,536 words
- Directly addresses up to 65,536 memory locations
- Transfers initialized via software
- Software selectable/maskable interrupt operations
- Interrupt priority switch selectable

The SBC 501 is a member of Intel's complete line of SBC 80 OEM Computer Systems. The SBC 501 interfaces directly with any SBC 80 Single Board Computer based system, via the system bus. High-speed, Direct Memory Access control and interfacing for transfers between SBC 80 expansion board memory and up to 16 peripheral devices is provided.



Block lengths up to 65,536 bytes long may be transferred directly to or from RAM memory in SBC 80 systems at rates up to 1 million words per second. The SBC 501 16-bit addressing capability allows transfers to take place at any location within memory. It is designed to control the direct transfer of data to or from Intel SBC 80 Memory Expansion or Combination Memory and I/O Boards. Two transfer modes of operation are included. System software is used to select the desired mode. Transfer rates up to 330K words per second may be achieved in the Shared Bus Mode, wherein the SBC 501 requests access to the system bus for 600 ns to perform a transfer of one word to or from memory. The second mode, the Override Mode, establishes the DMA Controller as the only master which may access the system bus during the transfer period, thereby providing rapid block transfer capability. This mode provides transfer rates up to 1 million words per second. Either mode may be used with the SBC 80/20 Single Board Computer. The SBC 80/10 Single Board Computer may only interact with the SBC 501 in the Shared Bus Mode.

A 4-bit TAG register is provided which may be used as a device select port to provide selection for four (up to 16 with external decoding) high-speed peripheral devices interfacing through the SBC 501. Four timing strobes are provided for the control of data input transfers and four timing strobes are provided for output transfer operations. Strobes are initiated and selected via system software, and strobe pulses are jumper-selectable to 100, 200, 400, 800, or 1600 ns widths. Interrupt requests originating from the DMA Controller are software maskable, active-low, and switch-selectable to any one of eight priority levels. User-selected DMA Interrupt requests may originate automatically upon completion of a transfer operation, from an external DMA device, or from a software command to the DMA Controller (for system testing purposes).



SBC 501 DMA CONTROLLER BLOCK DIAGRAM

SPECIFICATIONS

WORD SIZE
8 bits

BLOCK SIZE
65,536 words, maximum

ADDRESSING CAPABILITY
65,536 words

TRANSFER RATES

MODE	TRANSFER RATES (K bytes/sec)[1]			
	Memory Read Operations		Memory Write Operations	
	Typical	Worst Case[3]	Typical	Worst Case[3]
SHARED BUS, CPU Halted[2]	330	270	330	270
SHARED BUS, CPU Executing Code[2]	180	160	180	160
OVERRIDE	1000	660	1000	660

Notes: 1. Transfer rates given are to and from RAM memory on SBC 104 or SBC 108 Combination Memory and I/O Boards.
2. Shared Bus Mode may be used with Intel® SBC 80/10 or Intel® SBC 80/20. SBC 80/20 may also operate in Override Mode.
3. Assumes every DMA transfer must wait for RAM REFRESH CYCLE to be completed, worst case memory cycle times.

INTERRUPTS
Interrupt requests originating from the DMA Controller are software maskable, active-low, and switch-selectable to any one of eight priority levels. User-selectable DMA Interrupt requests may originate automatically upon completion of a transfer operation, from an external DMA device, or from a software command to the DMA Controller (for system testing purposes).

KEY REGISTERS
CONTROL REGISTER (6 bits)
The contents of the control register specify the BUSY status of the DMA Board, the type of operation to be performed (transfer or non-transfer), the transfer direction (to or from memory), the interrupt condition (enabled or disabled), and the means by which the DMA Board is using the system bus (Shared Mode or Override Mode).

MEMORY ADDRESS REGISTER (16 bits)
Contains the address of the next memory location to be accessed by the SBC 501. Loaded from the CPU, prior to a transfer operation, with the address of the first memory location to be accessed. The address is gated onto the system address bus during each transfer, and incremented by one for each word transferred.

LENGTH REGISTER (16 bits)
Contents of this register specify the total number of words to be transferred. This word count is decremented by one after each word is transferred. The transfer stops when the word count equals zero.

TAG REGISTER (4 bits)
The contents of the TAG REGISTER are used as control/select lines to the external peripheral devices being interfaced by the SBC 501 (e.g., as the "go" command line to each of four devices), or the TAG REGISTER outputs may be used with external decoding to expand the maximum number of DMA peripherals to 16.

STATUS REGISTER (8 bits)
Provides 4 bits of DMA Controller status: Software Interrupt, Memory READ/WRITE operation requested, External/End-of-Transfer Interrupt, and DMA Controller BUSY. The STATUS REGISTER also provides four status/control bits directly from user peripheral devices.

ADDRESS SELECTION
SBC 501 Registers are located in a Jumper-Selectable Block starting at any 16-word boundary in the I/O address space.

Register locations:

Address[1]	I/O Operation	Function
X0	Output	Output Strobe 0
X1	Output	Output Strobe 1
X2	Output	Output Strobe 2
X3	Output	Output Strobe 3
X4	Output	Output Tag Strobe
X8	Output	Set Interrupt
X9	Output	Reset Interrupt
XA	Output	Load Control Register
XB	Output	Load Tag Register
XC	Output	Load LSB Length Register
XD	Output	Load MSB Length Register
XE	Output	Load LSB Memory Address Register
XF	Output	Load MSB Memory Address Register
X0	Input	Input Command Strobe 0
X1	Input	Input Command Strobe 1
X2	Input	Input Command Strobe 2
X3	Input	Input Command Strobe 3
X4	Input	Read LSB Length Register
X5	Input	Read MSB Length Register
X6	Input	Read DMA Status
X7	Input	Invalid Command

Note: 1. X is any HEX digit, assigned by jumpers.

CONNECTORS

Interface	No. of Pins (Double-Sided)	Centers (in.)	Mating Connectors
BUS	86	0.156	CDC VPB01E43D00A1 Viking 2VH43/1AV5
I/O	100	0.100	Intel® MDS 990 Viking 3VH50/1JN5

INTERFACE CHARACTERISTICS
I/O Line Driver Sink Current: 48 mA
I/O Line Terminator Load: 150Ω pull-up
Inputs: Data positive relative to data bus
Outputs: Data positive relative to data bus
Output Strobes: Jumper-selectable to 100, 200, 400, 800, or 1600 ns pulse widths.
All I/O interface data and control signals are TTL compatible and SBC 80 BUS compatible.

PHYSICAL CHARACTERISTICS
Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 12 oz (340.5 gm)

ELECTRICAL CHARACTERISTICS
DC Power:
V_{CC} = 5V ±5%
I_{CC} = 3.35A max; 2.70A typical

ENVIRONMENT
Operating Temperature: 0°C to 55°C

EQUIPMENT SUPPLIED
SBC 501 DMA Controller Board
SBC 501 Schematic

SBC 80P PROTOTYPE PACKAGE

SBC 80/10 Single Board Computer

SBC 604 Cardcage/Backplane with compatible power supply cables

Comprehensive System Monitor residing on two Intel® 8708 EPROMs

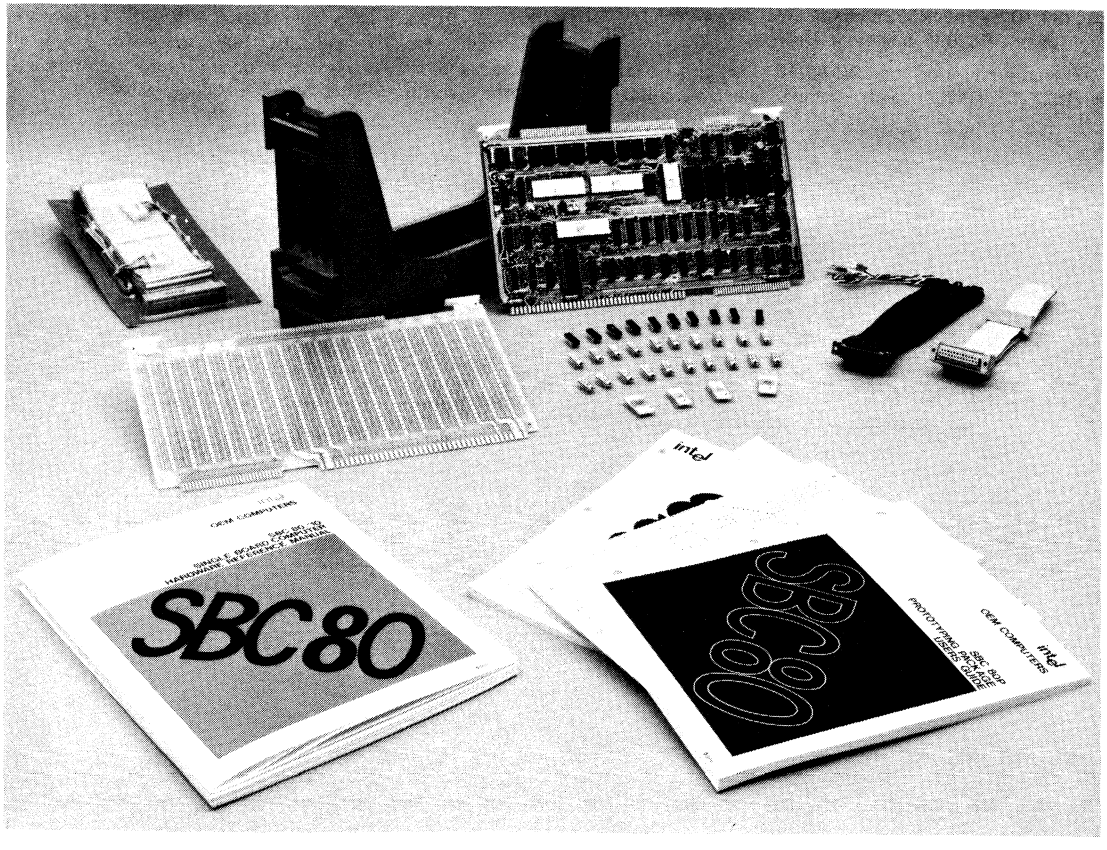
RS232C and TTY cables to interface the SBC 80/10 to any RS232C compatible device or teletypewriter

Two 50-pin unterminated flat cables with connectors that mate with SBC 80/10 parallel I/O PC edge connectors

Full complement of EPROMs, I/O line drivers, and I/O line terminators

SBC 905 Universal Prototype Board for interfacing custom hardware to the SBC 80/10

The SBC 80P Prototype Package contains all the hardware, software, and documentation necessary to evaluate Intel's SBC 80/10 Single Board Computer for OEM applications.



The heart of the SBC 80P Prototype Package is the SBC 80/10 Single Board Computer, a complete computer on a single 6.75-by-12 inch printed circuit board. The SBC 80/10 includes an 8080A CPU, 1K bytes of RAM memory, sockets for 4K bytes of EPROM memory, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable synchronous/asynchronous communications interface with RS232C and teletype compatibility, a multi-source single level interrupt network and bus drivers for memory and I/O expansion.

An SBC 604 Modular Cardcage/Backplane is included to house the SBC 80/10 and provide an easily accessible bus interface. The SBC 604 houses the SBC 80/10 and up to three expansion boards. All SBC 80 bus signals are present on all four mating connectors. Also included are two power supply cables, which mate with the power supply connectors on the backplane, to carry ±5 and ±12 volts DC.

A comprehensive system monitor, residing in two Intel® 8708 EPROMs, is included to facilitate the loading, execution, and debug of SBC 80/10 based programs. Monitor commands include the ability to read and write hexadecimal paper tapes, execute pre-defined program segments, display and alter memory contents, display and alter CPU register contents. Monitor commands and resulting information may be initiated and displayed using a teletype or CRT terminal. Two cables are provided for this purpose. The first interconnects the serial PC edge connector on the SBC 80/10 to any RS232 compatible device. The second connects the RS232C cable to a teletype.

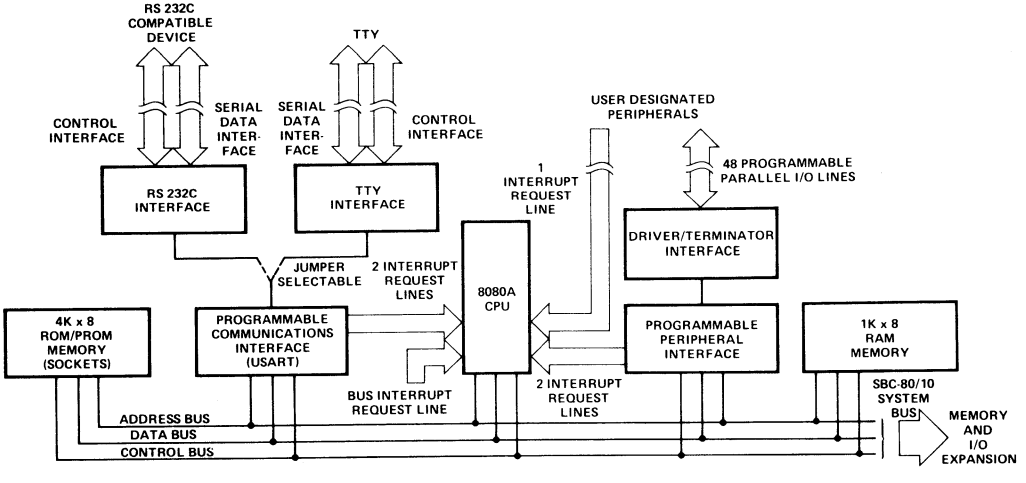
Wire-wrap jumpers on the SBC 80/10 select either teletype or RS232C operation and a jumper selectable baud rate generator on the SBC 80/10 is used to select the appropriate communications frequency.

Two 50-pin unterminated flat cables are included to facilitate interfacing the 48 parallel I/O lines on the SBC 80/10 to user designated I/O devices. The 48 programmable I/O signal lines and corresponding 48 ground lines on the SBC 80/10 are brought out to two 50-pin PC edge connectors where they mate with the two flat cables. The cables are left unterminated to allow the user to provide the appropriate mating connector for any application.

The SBC 80P prototype package includes a full complement of EPROMs, I/O line drivers, and I/O line terminators. Four Intel 8708 EPROMs (1K bytes each) are included. Two EPROMs contain the system monitor and two are unprogrammed. Ten 7437 48-milliamp TTL quad I/O line drivers, ten Intel SBC 901 220Ω/330Ω line terminators, and ten SBC 902 1 kΩ line terminators are included.

An SBC 905 Universal Prototype Board is provided to facilitate the construction of SBC 80/10 customized I/O and/or memory hardware. The SBC 905 plugs directly into the SBC 604 Cardcage/Backplane and can house up to 95 16-pin wire-wrap sockets or an equivalent mix of 14, 16, 18, 22, 24, 28, or 40-pin sockets.

The SBC 80P Prototype contains all the in-depth documentation needed to program and interface the SBC 80/10 Single Board Computer. An 8080 Assembly Language Manual, PL/M Programming Manual, SBC 80/10 Hardware Reference Manual, and SBC 80P User's Guide are all included to provide clear and concise information relevant to the use of the SBC 80/10 in OEM equipment.



1. Interrupts originating from the Programmable Communications Interface and Programmable Peripheral Intertace are jumper selectable.

SBC 80/10 BLOCK DIAGRAM

SPECIFICATIONS

SINGLE BOARD COMPUTER

(1) SBC 80/10 Single Board Computer

CARDCAGE/BACKPLANE

(1) SBC 604 Modular Cardcage/Backplane with capacity for four SBC boards.

CABLES

(2) Power Supply Cables (2 ft long):
Both required for ±5, ±12 volts DC; mate with SBC 604.

(2) 50-wire parallel I/O Flat Cables (5 ft long):
Both mate with SBC 80/10 50-pin parallel I/O PC edge connectors.

(1) RS232C Cable (2 ft long):
Flat cable with 26-pin SBC 80/10 connector on one end and a standard 25-pin RS232C connector on the other end.

(1) TTY Cable (5 ft long):
Interconnects RS232C cable with teletype; 25-pin RS232C mating connector on one side; seven spade lugs on the other end.

I/O LINE DRIVERS AND TERMINATORS

(10) 7437 48 mA totem-pole line drivers
(10) SBC 901 220Ω/330Ω terminators
(10) SBC 902 1 kΩ terminators

UNIVERSAL PROTOTYPE BOARD

(1) SBC 905 Universal Prototype Board with capacity for 95 16-pin wire-wrap sockets or equivalent mix of 14, 16, 18, 22, 24, 28, or 40-pin sockets; compatible with SBC 604 cardcage/backplane.

SYSTEM MONITOR

Addresses:
0000–06FF$_H$ (ROM; 3F80–3FFF$_H$ (RAM)

Commands:
Display Memory (D)
Program Execute (G)
Insert Instructions into Memory (I)
Move Memory (M)
Read Hexadecimal File (R)
Substitute Memory (S)
Write Hexadecimal File (W)
Examine and Modify CPU Registers (X)

Drivers:
Console Input
Console Output
Reader Input
Punch Output

Breakpoints:
A hardware breakpoint capability may be implemented by an interrupt service routine beginning at RAM location 3C3D$_H$. Typically, a 2-byte call is used. Interrupt generation at the breakpoint may be accomplished by user hardware or by insertion of single byte calls at instruction boundaries.

LITERATURE

8080 Assembly Language Manual
SBC 80/10 Hardware Reference Manual
SBC 80P User's Guide
SBC 80/10 Schematics

SBC 80P20 PROTOTYPE PACKAGE

SBC 80/20 Single Board Computer

SBC 604 Cardcage/Backplane with compatible power supply cables

Comprehensive System Monitor residing on two Intel® 8708 EPROMs

RS232C cable to interface the SBC 80/20 to RS232C compatible devices

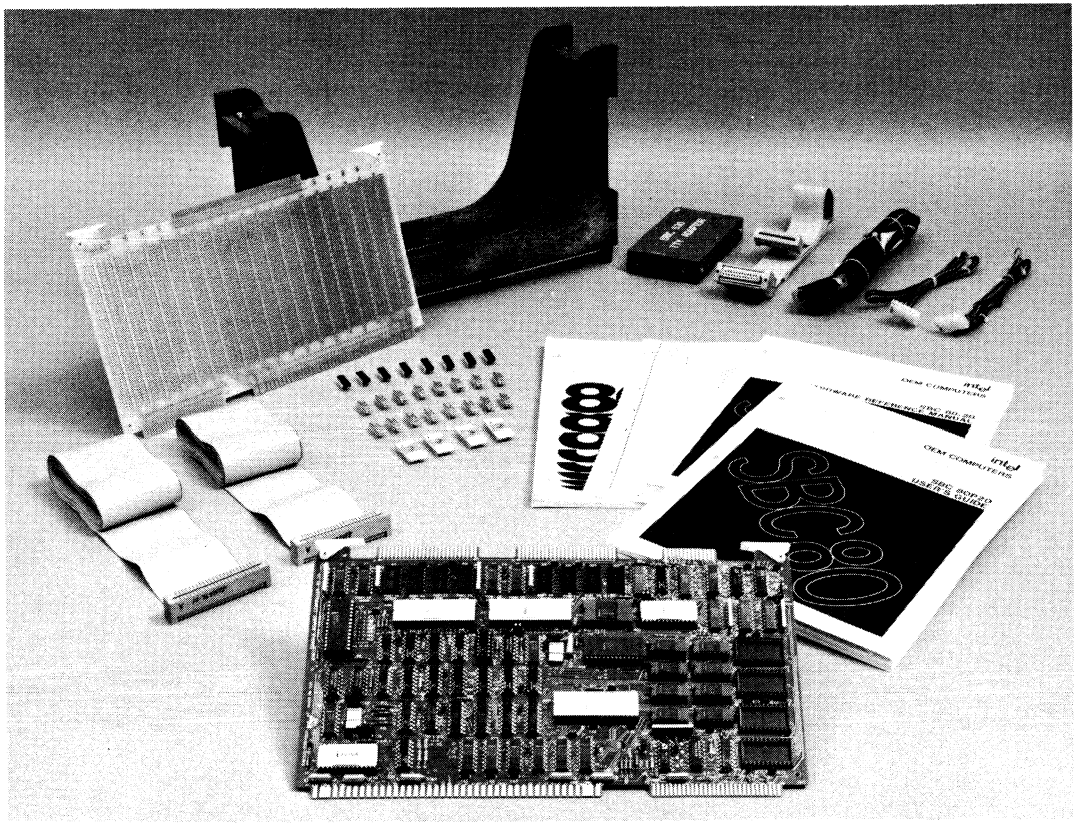
SBC 530 Teletypewriter Adapter and TTY cable to interface the SBC 80/20 to teletypewriters

Two 50-pin unterminated flat cables with connectors that mate with SBC 80/20 parallel I/O PC edge connectors

Full complement of EPROMs, I/O line drivers, and I/O line terminators

SBC 905 Universal Prototype Board for interfacing custom hardware to the SBC 80/20

The SBC 80P20 Prototype Package contains all the hardware, software, and documentation necessary to evaluate Intel's SBC 80/20 Single Board Computer for OEM applications.



MICRO-COMPUTER SYSTEMS

The heart of the SBC 80P20 Prototype Package is the SBC 80/20 Single Board Computer, a complete computer on a single 6.75-by-12 inch printed circuit board. The SBC 80/20 includes an 8080A CPU, 2K bytes of RAM memory, sockets for 4K bytes of EPROM memory, full multi-master bus arbitration logic which allows up to 16 CPU or controller masters to share the SBC 80 system bus, full programmable multi-mode eight-level vectored interrupt, two programmable interval timers which may be used as real-time clocks or for controlled I/O timing, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, and a programmable synchronous/asynchronous communications interface with RS232C compatibility. Baud rates for the communications interface are software programmable. Systems software is used to select the appropriate communications frequency. Bus drivers are also included for memory and I/O expansion.

An SBC 604 Modular Cardcage/Backplane is included to house the SBC 80/20 and provide an easily accessible bus interface. The SBC 604 houses the SBC.80/20 and up to three expansion boards. All SBC 80 bus signals are present on all four mating connectors. Also included are two power supply cables, which mate with the power supply connectors on the backplane, to carry ±5 and ±12 volts DC.

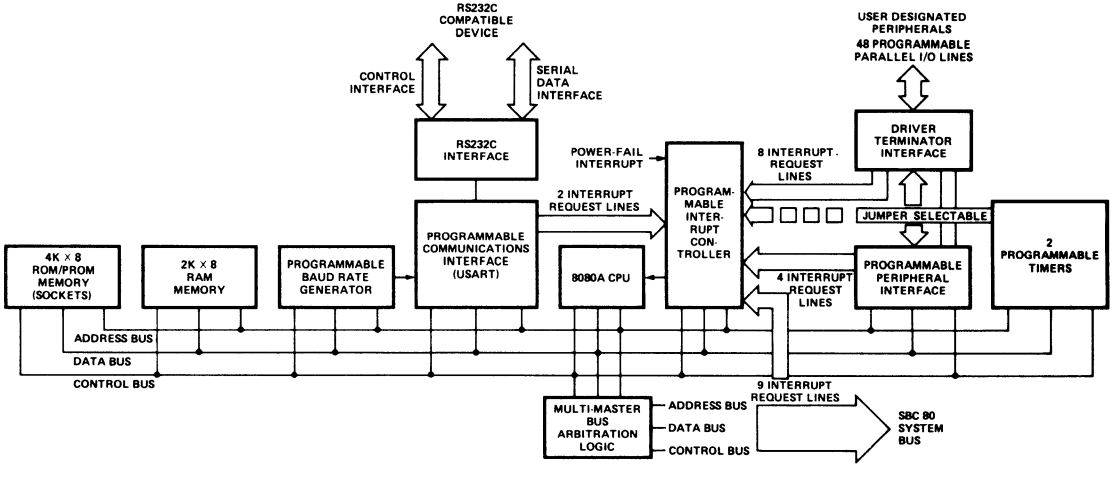
A comprehensive system monitor, residing in two Intel® 8708 EPROMs, is included to facilitate the loading, execution, and debug of SBC 80/20 based programs. Monitor commands include the ability to read and write hexadecimal paper tapes, execute pre-defined program segments, execute single program instructions, BREAK program execution or any of seven system conditions, display, move, and alter memory contents, display and alter CPU register contents, and read and write memory contents from or to paper tape. Monitor commands and resulting information may be initiated and displayed using a teletypewriter or CRT terminal. Two cables and an SBC 530 Teletypewriter Adapter are provided for this purpose. The first interconnects the serial PC edge connector on the SBC 80/20 to any RS232C compatible device. For teletypewriter interfaces, the SBC 530 Teletypewriter Adapter converts RS232C signals from the RS232C cable to a 20 mA current loop interface. The TTY cable then mates these signals directly to a teletypewriter. Any of eight standard baud rates may be used with the Monitor. A special "Baud Rate Search" capability is built into the Monitor which determines the baud rate of terminal used automatically.

Two 50-pin unterminated flat cables are included to facilitate interfacing the 48 parallel I/O lines on the SBC 80/20 to user designated I/O devices. The 48 programmable I/O signal lines and corresponding 48 ground lines on the SBC 80/20 are brought out to two 50-pin PC edge connectors where they mate with the two flat cables. The cables are left unterminated at the user end to allow the user to provide the appropriate mating connector for any application.

The SBC 80P20 Prototype Package includes a full complement of EPROMs, I/O line drivers, and I/O line terminators. Four Intel 8708 EPROMs (1K bytes each) are included. Two EPROMs contain the system monitor and two are unprogrammed. Eight 7437 48-milliamp TTL quad I/O line drivers, eight Intel SBC 901 220Ω/330Ω line terminators, and eight SBC 902 1 kΩ line terminators are included.

An SBC 905 Universal Prototype Board is provided to facilitate the construction of SBC 80/20 customized I/O and/or memory hardware. The SBC 905 plugs directly into the SBC 604 Cardcage/Backplane and can house up to 95 16-pin wire-wrap sockets or an equivalent mix of 14, 16, 18, 22, 24, 28, or 40-pin sockets.

The SBC 80P20 Prototype Package contains all the in-depth documentation needed to program and interface the SBC 80/20 Single Board Computer. An 8080 Assembly Language Manual, PL/M Programming Manual, SBC 80/20 Hardware Reference Manual, and SPC 80P20 User's Guide are all included to provide clear and concise information relevant to the use of the SBC 80/20 in OEM equipment.



SBC 80/20 BLOCK DIAGRAM

SPECIFICATIONS

SINGLE BOARD COMPUTER
(1) SBC 80/20 Single Board Computer

CARDCAGE/BACKPLANE
(1) SBC 604 Modular Cardcage/Backplane with capacity for four SBC 80 boards.

INTERFACE ADAPTER
(1) SBC 530 Teletypewriter Adapter which converts RS232C levels to 20 mA current loop interface.

CABLES
(2) Power Supply Cables (2 ft long):
Both required for ±5, ±12 volts DC; mate with SBC 604.
(2) 50-wire parallel I/O Flat Cables (5 ft long):
Both mate with SBC 80/20 50-pin parallel I/O PC edge connectors, unterminated at user end.
(1) RS232C Cable (2 ft long):
Flat cable with 26-pin SBC 80/20 connector on one end and a standard 25-pin RS232C connector on the other end.
(1) TTY Cable (5 ft long):
Interconnects SBC 530 Teletypewriter Adapter with teletypewriter; 25-pin RS232C mating connector on one end; seven spade lugs on the other end.

I/O LINE DRIVERS AND TERMINATORS
(8) 7437 48 mA totem-pole line drivers
(8) SBC 901 220Ω/330Ω terminators
(8) SBC 902 1 kΩ terminators

UNIVERSAL PROTOTYPE BOARD
(1) SBC 905 Universal Prototype Board with capacity for 95 16-pin wire-wrap sockets or equivalent mix of 14, 16, 18, 22, 24, 28, or 40-pin sockets; compatible with SBC 604 cardcage/backplane.

SYSTEM MONITOR
Addresses:
$0000–069C_H$ (ROM); $3F80–3FFF_H$ (RAM)
Commands:
Display Memory (D)
Execute Program (G)
Insert Instruction or Data into Memory (I)
Move Memory (M)
Execute Next Instruction (i.e., Single Step) (N)
Read Hexadecimal File (R)
Substitute Memory (S)
Write Hexadecimal File (W)
Examine and Modify CPU Registers (X)
Drivers:
Console Input
Console Output
Reader Input
Punch Output
Breakpoints:
Program BREAKing may occur upon any of up to seven system conditions. BREAKs are implemented via the SBC 80/20 Programmable Interrupt Controller. Upon a BREAK; BREAK level, all CPU registers, and the next instruction (Op Code) are displayed at the console.
Baud Rates:
Baud Rate Search capability automatically sets serial baud rate to that of system console. Allowable baud rates include 110, 150, 300, 600, 1200, 2400, 4800, and 9600.

LITERATURE
8080 Assembly Language Manual
SBC 80/20 Hardware Reference Manual
SBC 80P20 User's Guide
SBC 80/20 Schematics
SBC 530 Schematics

SBC 530 TELETYPEWRITER ADAPTER

Compatible with SBC 80/20 Single Board Computer

Compatible with SBC 80 Combination Boards

Jumper-selectable RS232C Data Set or Data Terminal Configuration

Interface opto-isolated for high noise immunity

Provides general-purpose RS232C to 20 mA current loop interface

Compact, easily mounted package with standard connectors

The SBC 530 provides a compact and flexible means for interfacing the Intel® SBC 80/20 Single Board Computer, SBC 80 Combination Memory and I/O Expansion Boards, and most RS232C compatible equipment to teletypewriters and other 20 mA current loop equipment.

The SBC 530 converts RS232C signal levels to an optically isolated 20 mA current loop interface. The SBC 530 provides signal translation for Transmitted Data (Txd), Received Data (RcD), and a teletypewriter paper-tape reader relay. The RS232C interfaces are jumper-selectable, and may be configured to accept signals from an RS232C Data Terminal or Data Set. Threaded holes have been incorporated in the SBC 530 for ease in system chassis design, and multiple units may be mounted together to support multiple serial channels. The units are mountable in any of three planes.

When used with the SBC 80/20 Single Board Computer, power is provided to the SBC 530 directly through its RS232C connector. Power may also be provided through either of two auxiliary power connectors for standard current loop interfacing. The noise immunity benefits of total inter-system power isolation may be achieved through the use of both auxiliary power connectors on the SBC 530.

SPECIFICATIONS

INTERFACE CHARACTERISTICS

RS232C Side:
RS232C Signal Levels in/out[1]
TTY Side:
20 mA optically-isolated current loop

Note 1. RS232C Data Set Ready line controls 20 mA paper-tape reader relay driver line.

POWER

Power connectors for ground, +12V and -12V, are jumper-selectable. Power may be provided via 25-pin RS232C connector or via two separate auxiliary power connectors. Auxiliary connectors allow total power system isolation at SBC 530 Opto-coupler Interface.

Power Requirements:
V_{DD} = +12V ±5% I_{DD} = 98 mA max
V_{AA} = -12V ±5% I_{AA} = 98 mA max

EQUIPMENT SUPPLIED

SBC 530 Teletypewriter Adapter
SBC 530 Schematic
SBC 530 Outline Drawing

PHYSICAL CHARACTERISTICS

Width:	2.876 in.	(7.31 cm), max
Height:	4.850 in.	(12.32 cm), max
Depth:	0.920 in.	(2.34 cm), max
Weight:	9 oz	(255.4 gm)

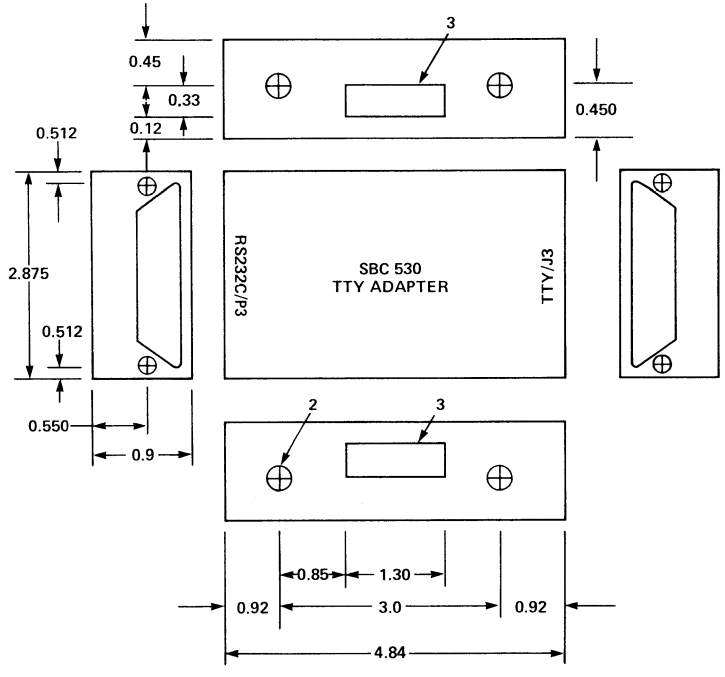
ENVIRONMENT

Operating Temperature: 0°C to 55°C

Mating Connectors

RS232C	Cinch		DB-25S
	ITT Cannon		DB-25S
20 mA (TTY)	Cinch		DB-25P
	ITT Cannon		DB-25P
Auxiliary Power	AMP	Connector	87159-7
		Pin	87023-1
		Polarizing Key	87116-2
	Molex	Connector	09-50-7071
		Pin	08-50-0106
		Polarizing Key	15-04-0219

NOTE:
1. Pins from a given vendor may only be used with connectors from the same vendor.



NOTES: 1. ALL DIMENSIONS IN INCHES.
2. ALL FOUR MOUNTING HOLES THREADED FOR 6-32 MACHINE SCREWS.
3. CUTOUTS FOR AUXILIARY POWER CONNECTORS.

SBC 530 DIMENSIONS

SBC 604/614 MODULAR BACKPLANE AND CARDCAGE

Interconnects and houses up to four Intel® SBC boards.

Connectors allow interconnection of two or more backplanes.

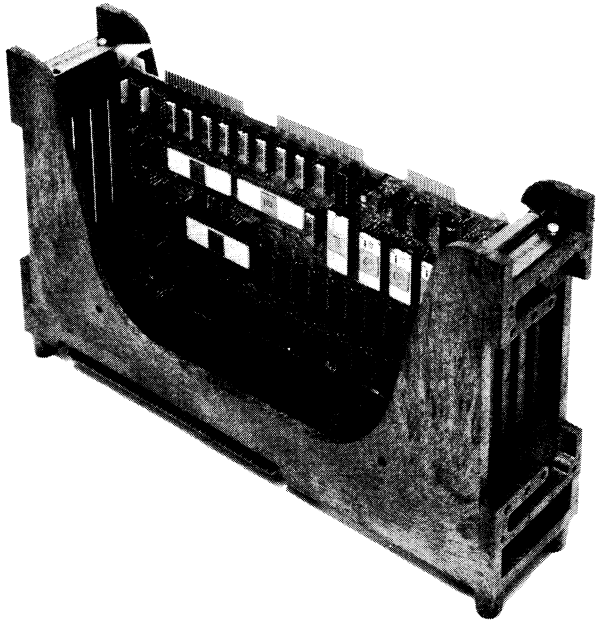
Cardcage mounting holes facilitate the interconnection of two or more units.

Compatible with 3.5 inch RETMA rack mount increments.

Dual backplane power supply connectors.

The SBC-604 and SBC-614 Modular Backplane and Cardcage units provide low-cost, off-the-shelf solutions for OEM products using two or more Intel® SBC boards. Each unit interconnects and houses up to four Intel SBC boards.

The SBC-604 contains a male backplane PC edge connector and bus signal termination circuits. It is suitable for applications requiring a single unit, or may be interconnected with the SBC-614 when more than one backplane/cardcage unit is needed. The SBC-614 contains both male and female backplane connectors, and may be interconnected with the SBC-604 and the other SBC-614 units. Both units are identical with the exception of the backplane connectors and bus signal terminator features. A single unit may be packaged in a 3.5-inch RETMA rack enclosure and two interconnected units may be packaged in a 7-inch enclosure. The units are mountable in any of three planes. The SBC-604 contains power supply connectors.



SPECIFICATIONS

BACKPLANE CHARACTERISTICS

All SBC 80 address, data, and command bus lines are bussed to all four connectors on the Printed Circuit Backplane.

Power connectors for ground, +5, −5, +12, −12, −10V volt power supply lines.

SBC-604:
Bus signal terminators, backplane male PC edge connector only, and power supply headers.

SBC-614:
Backplane male and female connectors.

MATING POWER CONNECTORS:

AMP	Connector	87159-7
	Pin	87023-1
	Polarizing Key	87116-2
Molex	Connector	09-50-7071
	Pin	08-50-0106
	Polarizing Key	15-04-0219

NOTE:

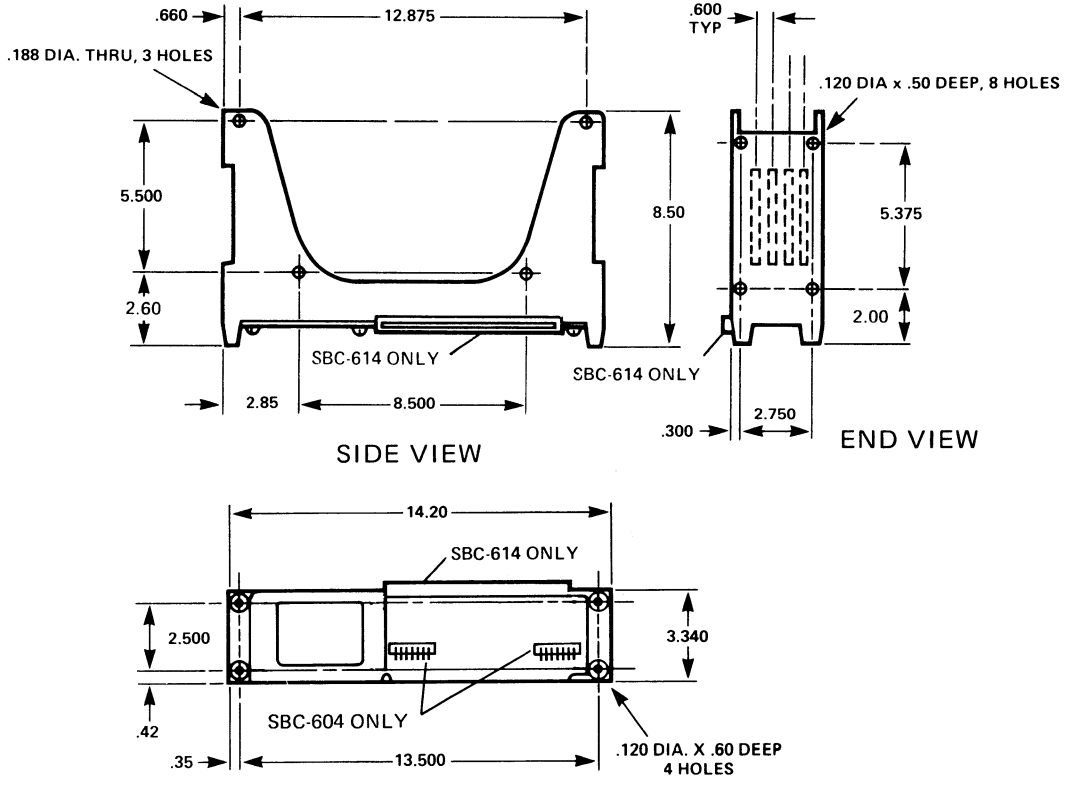
1. Pins from a given vendor may only be used with connectors from the same vendor.

PHYSICAL DIMENSIONS

Height: 8.5 in. (21.59 cm)
Width: 14.2 in. (36.07 cm)
Depth: 3.34 in. (8.48 cm)
Weight: 35 oz. (992.23 gm)

ENVIRONMENTAL

Operating Temperature
0°C to 55°C



SBC 604/614 DIMENSIONS

SBC 630 POWER SUPPLY

Provides ±5 and ±12 volt SBC 80 system voltages.

Sufficient power for a fully loaded Intel® Single Board Compuer plus residual power for user functions.

Compact single chassis.

Provides additional +26.5 volt supply.

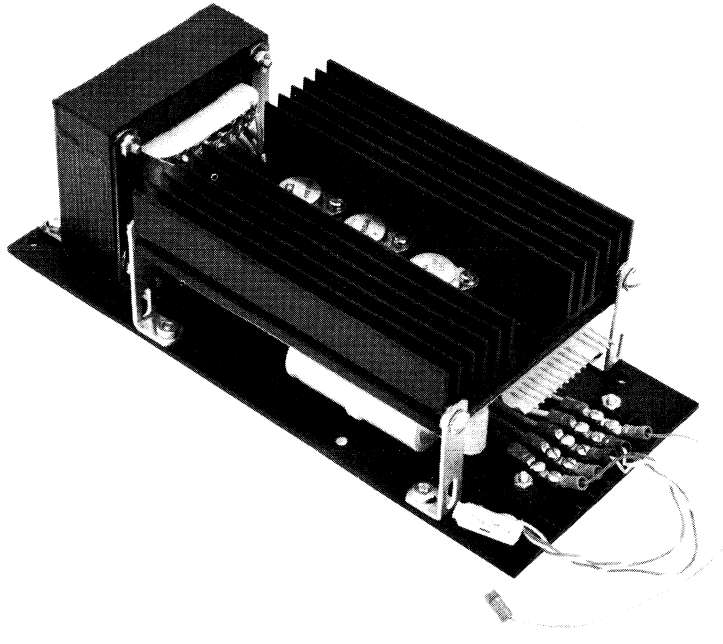
115 and 230 VAC operation.

50 Hz or 60 Hz input.

Keyed standard AC and DC connectors.

The SBC 630 Power Supply provides a low cost, off-the-shelf, single chassis power generation solution for OEM products using Intel® Single Board Computers.

The SBC 630 provides regulated DC output power at +12, +5, −5, and −12 volt levels. The current capabilities of each of these output levels have been chosen to provide power over the temperature range of 0° to +55°C for one Intel Single Board Computer fully loaded with I/O line terminators or drivers and four 8708 EPROMs plus residual capability for additional logic functions in OEM Systems. A +26.5 volt power level has also been provided for use in OEM Products for relay interfaces, displays, and for those OEM products requiring in-system 8708 EPROM programming capability. Current limiting protection is provided on the +12 volt and +5 volt outputs, and over-voltage protection is incorporated on the +5 volt output. Access to AC input and DC output power levels is provided via standard 4-pin and 14-pin keyed connectors, respectively.



SPECIFICATIONS

INPUT POWER

Frequency: 47 to 63 Hz
Voltage: 115 ±10% and 230 ±10% VAC
Current: 1.8 amps max (at 125 VAC)

OUTPUT POWER

Voltage	Output Current (Max)	Accuracy
+26.5	100 mA	±0.5 volt
+12	1.2A	±5%
+5	6A	±5%
-5	300 mA	±5%
-12	300 mA	±5%

MATING CONNECTORS[1]

AC Input

Connector	Molex	03-09-1042 or equivalent
Pin	Molex	02-09-1118 or equivalent (18 to 22 gauge wire)

DC Output

Connector	Molex	09-05-7141
	AMP	1-87159-3
Polarizing Key	Molex	15-04-0219
	AMP	87116-2
Pin	Molex	08-50-0106 (18 to 22 gauge wire)
	AMP	87023-1 (18 to 22 gauge wire)

NOTE:
1. Pins from a given vendor may only be used with connectors from the same vendor.

PHYSICAL CHARACTERISTICS

Height: 3.35 in. (8.51 cm) max
Width: 4.91 in. (12.40 cm) max
Depth: 11.00 in. (27.95 cm) max
Weight: 8.0 lb (3.63 Kgm)

OVER-VOLTAGE PROTECTION

5-volt output: Fixed within the range 6.08 volts to 6.72 volts.

LINE REGULATION

(10% Line Voltage Change)
+5 volt and +12 volt outputs: 0.1%
-5 volt, -12 volt and +26.5 volt outputs: 1%

LOAD REGULATION

(Half Load to Full Load)
+5 volt and +12 volt outputs: 0.1%
-5 volt, -12 volt and +26.5 volt outputs: 1%

OUTPUT RIPPLE AND NOISE

50 mV peak-to-peak on all outputs, maximum

SHORT CIRCUIT CURRENT

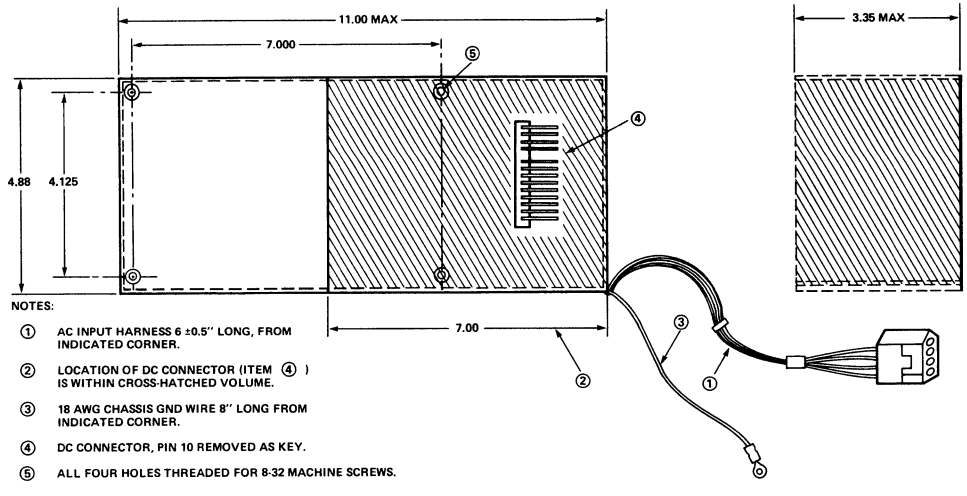
+5 volt output: 7.5 amp max.
+12 volt output: 1.5 amp max.

ENVIRONMENTAL

Operating Temperature: 0°C to +55°C

EQUIPMENT SUPPLIED

SBC 630 Power Supply
SBC 630 User's Manual (includes schematic)



SBC 630 MOUNTING INFORMATION

SBC 635 POWER SUPPLY

Provides ±5 and ±12 volt SBC 80 system power.

Sufficient power for a fully loaded Intel® Single Board Computer plus residual power for up to three Intel SBC Expansion Boards.

Compact single chassis.

"AC Low" Power Failure TTL logic level output provided for System Power-Down Control.

Current limiting and overvoltage protection on all outputs.

100, 115, 215, and 230 VAC operation.

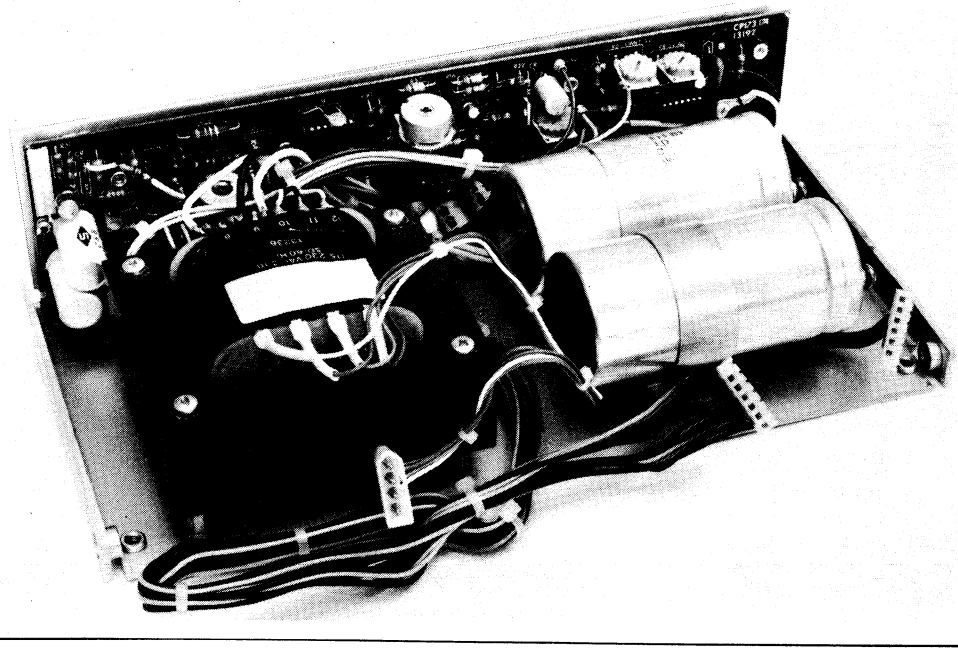
50 Hz or 60 Hz input.

DC Power Cables and connectors mate directly to SBC 604 Backplane/Cardcage Assembly.

The SBC 635 Power Supply provides a low cost, off-the-shelf, single chassis power generation solution for OEM products using Intel® SBC Boards.

The SBC 635 provides regulated DC output power at +12, +5, −5, and −12 volt levels. The current capabilities of each of these output levels have been chosen to provide power over 0° to +55°C temperature range for an Intel Single Board Computer fully loaded with I/O line terminators and drivers, and four 8708 EPROMs plus residual capability for most combinations of up to three SBC memory, I/O, or combination expansion boards.

Current limiting and over-voltage protection is provided on all outputs. Access for AC input is provided via a standard 4-pin keyed connector. DC output power levels are provided on cables with keyed connectors which are directly compatible with the SBC 604 Modular Backplane/Cardcage assembly. The SBC 635 includes logic which senses a system AC power failure and generates a TTL signal for clean system power-down control.



SPECIFICATIONS

INPUT POWER

Frequency: 47 to 63 Hz

Voltage: 100 VAC ±10%, 115 VAC ±10%, 215 VAC ±10%, 230 VAC ±10% via user-provided wiring options

OUTPUT POWER

Voltage	Output Current (Max)	Current Limit (Max)	Over-Voltage Protection
+12	2.0 amp	2.4 amp	+14 to +16 volts
+ 5	14.0 amp	16.8 amp	5.8 to 6.6 volts
- 5	0.9 amp	1.1 amp	- 5.8 to - 6.6 volts
-12	0.8 amp	1.0 amp	-14 to -16 volts

MATING CONNECTORS[1]

AC Input

Connector	Molex	03-09-1042 or equivalent
Pin	Molex	02-09-1118 or equivalent (18 to 22 gauge wire)

DC Output[2]

Header	Molex	09-66-1071
	AMP	87194-6

"AC Low" Control

Connector	Molex	09-50-7071
	AMP	87159-7
Polarizing Key	Molex	15-04-0219
	AMP	87116-2
Pin	Molex	08-50-0106 (18 to 22 gauge wire)
	AMP	87023-1 (18 to 22 gauge wire)

PHYSICAL CHARACTERISTICS

Height: 3.19 in. max (8.11 cm)

Width: 6.03 in. max (15.32 cm)

Depth: 12.65 in. max (32.12 cm)

Weight: 13 lb (5.90 Kgm)

REMOTE SENSING

Sensing provided for +5 volt output.

LINE REGULATION

±0.1% for 10% line change.[3]

LOAD REGULATION

±0.1% for 50% load change.[3]

OUTPUT RIPPLE AND NOISE

10 mV peak-to-peak maximum (DC to 500 kHz).[3]

TRANSIENT RESPONSE

Less than 50 μsec for 50% load change.[3]

OUTPUT VOLTAGE ACCURACY

All outputs adjustable ±5% from nominal.[4]

POWER FAILURE INDICATION

An active HIGH, TTL compatible output logic level is provided when input voltage falls below 103 VAC (RMS)[5] to indicate low AC input voltage conditions. All output voltages will remain within spec for one-half cycle (≈8.3 msec @ 60 Hz) minimum after "AC Low" is asserted.

ENVIRONMENTAL

Operating Temperature: 0°C to +55°C

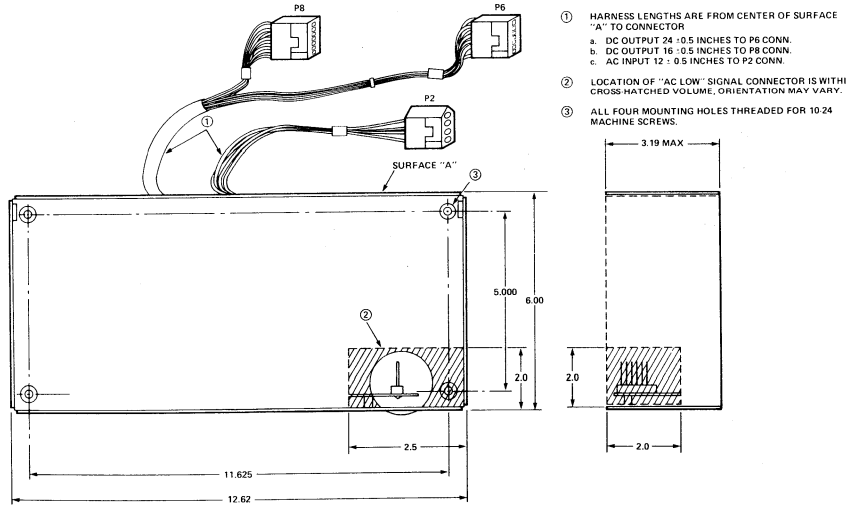
EQUIPMENT SUPPLIED

SBC 635 Power Supply with AC and DC Cables and Connectors attached as shown below.

SBC 635 User's Manual (includes schematic)

NOTES:

1. Pins from a given vendor may only be used with connectors from the same vendor.
2. SBC 635 DC output connectors are directly compatible with power input power connectors on SBC 604 Modular Backplane and Cardcage Assembly.
3. All outputs.
4. All outputs set to nominal voltage (no load) before delivery.
5. 206 VAC (RMS) for 230 VAC (RMS) nominal input operation.



SBC 635 MOUNTING INFORMATION

13

INTELLEC® MICROCOMPUTER DEVELOPMENT SYSTEMS

INTRODUCTION

Intel OEM Computer Systems products and microcomputer components are supported by the most advanced system development tools available today: The Intellec® Microcomputer Development System, its In-Circuit Emulators, and its complement of advanced development software. Software packages available for use directly on the Intellec system include a resident relocatable and linkable macro-assembler, a text editor, operating systems, and utility programs. PL/M, the high-level programming language Intel specifically designed for 8080-based systems, is also available resident on the Intellec system. The PL/M-80 compiler provides the capability to program in a natural, algorithmic language, and eliminates the need to manage register usage or allocate memory.

TABLE OF CONTENTS

DEVELOPMENT SYSTEMS

IN-CIRCUIT EMULATORS

DEVELOPMENT SYSTEMS PERIPHERALS

DESIGN AIDS

INTELLEC®
MICROCOMPUTER DEVELOPMENT SYSTEM

Modular microcomputer development system for development and implementation of MCS™-48, MCS-80, MCS-85, and Series 3000 Microcomputer Systems

Intel® 8080 microprocessor, with 2 μs cycle time and 78 instructions, controls all Intellec functions

Supports assemblers for 8080, 8085, and 8748, and resident complier for PL/M

16K bytes RAM memory expandable to 64K bytes

2K bytes ROM memory expandable with 6K or 16K PROM/ROM boards

Hardware interfaces and software drivers provided for TTY, CRT, line printer, high-speed paper tape reader, high-speed paper tape punch, and Universal PROM Programmer

Universal bus structure with multiprocessor and DMA capabilities

Eight level nested, maskable, priority interrupt system

Optional PROM programmer peripheral capable of programming all Intel PROMs

ICE™ (In-Circuit Emulator) options extend Intellec diagnostic capabilities into user configured system allowing real-time emulation of user processors

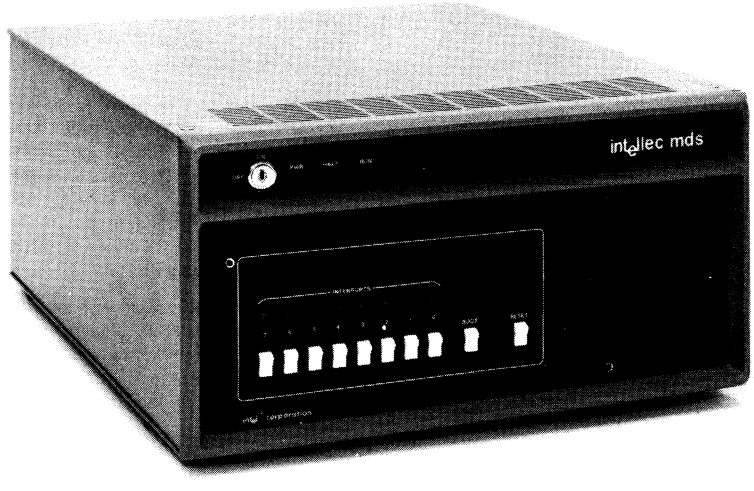
Optional I/O modules expandable in groups of four 8-bit input and output ports to a maximum of 88 ports (all TTL compatible)

ROM resident system monitor includes all necessary functions for program loading, debugging, and execution

RAM resident macro assembler used to assemble all MCS 48, 80, and 85 machine instructions with full macro and conditional assembly capabilities

RAM resident text editor with powerful string search, substitution, insertion, and deletion commands

The Intellec® Development System is a modular microcomputer development system containing all necessary hardware and software to develop and implement Intel microcomputer and microcomputer systems. The addition of options and peripherals provides the user with a complete in-circuit microcomputer development system, supporting product design from program development through prototype debug, to production and field test.



DEVELOPMENT SYSTEMS

INTELLEC HARDWARE

The standard Intellec® System consists of four microcomputer modules (CPU, 16K RAM Memory, Front Panel Control, and Monitor), an interconnecting printed circuit motherboard, power supplies, fans, a chassis, and a front panel. Modular expansion capability is provided by 14 additional sockets on the motherboard.

The CPU module uses Intel's powerful NMOS 8-bit 8080 microprocessor. The 8080's 2 μs cycle time, 78 instructions, unlimited subroutine nesting, vectored interrupt, and DMA capabilities are fully utilized by the Intellec System Bus control logic resolves bus contention conflicts between the CPU module and other modules capable of acquiring control of the bus. The CPU module interfaces with a sixteen line address bus and a bidirectional eight line data bus. 8080 status signals are decoded and utilized for memory and I/O operations. An eight-level, nested interrupt priority system, complete with an interrupt priority push-down stack, resolves contention for 8080 interrupt servicing.

The RAM memory module contains 16K bytes of Intel 2107A dynamic RAM which operates at full processor speed. All necessary address decoding and refresh logic is contained on the module.

The front panel control module provides system initialization, priority arbitration, and real time clock functions. System initialization routines reside in a 256 byte, PROM resident, bootstrap loader. An eight-level priority arbitration network resolves bus contention requests among potential bus masters. A 1 ms interrupt request generator, which can be disabled under program control, provides real time clock functions. A 10 ms automatic time-out feature is also provided to force an interrupt request if nonexistent memory or I/O is addressed.

The Monitor module contains the Intellec system monitor and all Intellec peripheral interface hardware. The system monitor resides in a 2K byte Intel 8316 ROM. The module contains all necessary control and data transfer circuitry to interface with the following Intellec peripherals:

- Teletype
- CRT
- High Speed Paper Tape Reader
- High Speed Paper Tape Punch
- PROM Programmer
- Line Printer

The Intellec universal bus structure enables several CPU and DMA devices to share the bus by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal which is derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure contains provisions for up to 16-bit address and data transfers and is not limited to any one Intel microcomputer family.

The Intellec front panel is intended to augment the primary user interaction medium, the system console. The simplicity of the front panel coupled with the power of the system monitor provides an efficient user/Intellec interface. The front panel contains eight interrupt request switches with corresponding indicators, CPU RUN and HALT status indicators, a bootstrap loader switch, RESET switch, and a POWER ON switch and indicator.

The basic Intellec capabilities may be significantly enhanced by the addition of the following optional features.

ICE™ (In-Circuit Emulator) extends Intellec diagnostic capabilities into user configured systems. The Intellec resident ICE processor operates in conjunction with the host CPU and interfaces to the user system via an external cable. The ICE processor replaces the user system processor providing real time emulation capability. Resident memory and I/O may be substituted for equivalent user system elements; allowing the hardware designer to sequentially develop his system by integrating Intellec and user system hardware. Display and debug hardware eliminate the need for specially constructed user system equivalents. Augmenting these capabilities are such powerful ICE debug functions as setting breakpoints, tracing program flow, single stepping, examining and altering CPU registers and memory locations.

The Universal PROM Programmer is an Intellec peripheral capable of programming and verifying the following Intel PROMs: 1702A, 2704, 2708, 3601, 3604, 3624, 8702A, 8704, 8708, 8748, and 8755. Programming and verification operations are initiated from the Intellec system console and are controlled by programs resident in the Intellec and Universal PROM Programmer.

The addition of a single or dual drive Diskette Operating System significantly reduces program development time. An intelligent controller, constructed around Intel's powerful Series 3000 computing elements, provides diskette interface and control. Intel's software operating system (IDOS) in conjunction with the diskette operating system hardware provides a highly efficient and easy to use method of assembling, editing, and executing programs.

Customized user I/O requirements may be satisfied by adding I/O modules. Each I/O module contains four 8-bit input ports (latched or unlatched), four 8-bit latched output ports (with adjustable strobe pulses), and eight system interrupt lines. All inputs and outputs are TTL compatible. Optional I/O may be expanded to a maximum of 44 input and 44 output ports.

Memory may be expanded by adding RAM or PROM modules in user defined combinations. Up to 64K bytes of RAM may be added in 16K byte increments. PROM (Intel 8702A) may be added in 256 byte increments by adding PROM modules with socket capacity for 6K bytes and populating each module with the desired number of PROMs. Maximum PROM capacity is 12K bytes. RAM/PROM memory overlap is resolved by giving PROM priority.

DMA (direct memory access) modules work in conjunction with the Intellec MDS universal bus to maximize the efficiency of data transfers between MDS memory and selected I/O devices. Each module contains all the necessary control and data transfer logic to implement a complete DMA channel.

A ROM simulator composed of high speed bipolar RAM emulates Series 3000 bipolar microprogram ROM memory. Each ROM simulator module may be used in 512 X 16 or 1024 X 8 configurations.

INTELLEC SOFTWARE

Resident software provided with the Intellec includes the system monitor, 8080 macro assembler and text editor. Used together, these three programs simplify program preparation and speed the debugging task.

The system monitor provides complete control over operation of the Intellec. All necessary functions for program loading and execution are provided. Additional commands provide extensive debug facilities and PROM programming functions. System peripherals may be dynamically assigned either via monitor commands or through calls to the system monitor's I/O subroutines.

Programs may be loaded from the reader device in either BNPF or hexadecimal format. Utility commands which aid in the execution and checkout of programs include:

- initialize memory to a constant
- move a block of memory to another location
- display memory
- modify RAM memory
- examine and modify CPU registers
- set breakpoints
- initiate execution at any given address
- perform hexadecimal arithmetic
- examine and modify the interrupt mask

The Intellec System Monitor contains a powerful and easily expandable input/output system, which is built around four logical device types; console device, reader device, punch device and list device. Associated with each logical device may be any one of four physical devices. The user controls physical device assignment to each logical device through a System command.

Drivers are provided in the system monitor for the Universal PROM Programmer, ASR 33 teletype, high speed paper tape reader, high speed paper tape punch, line printer, and CRT. The user may write his own drivers for other peripheral devices and easily link them to the system monitor.

All system peripherals may be accessed simply by calling I/O subroutines in the system monitor. In addition, the user may dynamically reconfigure his system by monitor commands or by calling system subroutines which can assign a different physical device to each logical device. The user may also determine the current system peripheral configuration, check I/O status and determine the size of available memory.

The monitor is written in 8080 Assembly Language and resides in 2K bytes of ROM memory.

The Intellec Resident Assembler translates symbolic 8080 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation.

Conditional assembly permits the assembler to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

The assembler performs its function in three passes. The first pass builds the symbol table. The second pass produces a source listing and provides error diagnostics. The third pass produces the object code. If the punch and list devices are separate (e.g. a high speed punch or printer is available) passes 2 and 3 may be combined into one pass.

Object code produced by the assembler is in hexadecimal format. It may be loaded directly into the Intellec for execution and debugging or may be converted by the system monitor to BNPF format for ROM programming.

The assembler is written in PL/M-80, Intel's high level systems programming language. It occupies 12K bytes of RAM memory including space for over 800 symbols. The symbol table size may be expanded to a maximum of 6500 symbols by adding RAM memory. All I/O in the assembler is done through the system monitor, enabling the assembler to take advantage of the monitor's I/O system. The assembler is shipped in hexadecimal object format on paper tape or diskette and is standard with each Intellec.

The Intellec editor is a comprehensive tool for the entry and correction of assembly language programs for the Intel 8080 microcomputer. Its command set allows manipulation of either entire lines of text or individual characters within a line.

Programs may be entered directly from the console keyboard or from the system reader device. Text is stored internally in the editor's workspace, and may be edited with the following commands:

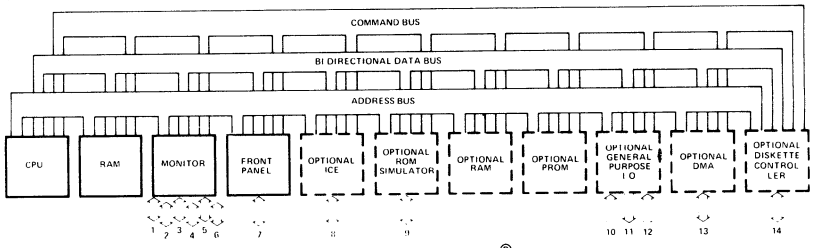
- string insertion or deletion
- string search
- string substitution

To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

The contents of the workspace may be listed to the system console or written to the system list or punch device for future use.

The text editor is written in PL/M-80. It occupies 8K bytes of RAM memory, including over 4500 bytes of workspace. The workspace may be expanded to a maximum of 58K bytes by adding RAM memory. All I/O in the editor is done through the system monitor, enabling the editor to take advantage of the monitor's I/O system. The editor is shipped in hexadecimal object format on paper tape or diskette and is standard with each Intellec.



NOTES
1. PROM PROGRAMMER DATA STATUS COMMANDS
2. HIGH SPEED PUNCH DATA STATUS COMMANDS
3. HIGH SPEED HEADER DATA STATUS COMMANDS
4. PRINTER DATA STATUS COMMANDS
5. CRT DATA STATUS COMMANDS
6. TTY DATA STATUS COMMANDS
7. FRONT PANEL STATUS SWITCH INPUTS
8. USER SYSTEM CPU OR MCU PIN SIGNALS
9. USER SYSTEM ROM PIN SIGNALS
10. EIGHT INTERRUPT LINES
11. FOUR 8 BIT OUTPUT PORTS
12. FOUR 8 BIT INPUT PORTS
13. DMA DEVICE DATA STATUS COMMANDS
14. DISKETTE DRIVE DATA/STATUS/COMMANDS

INTELLEC® BLOCK DIAGRAM

HARDWARE SPECIFICATIONS

WORD SIZE
Host Processor (Intel 8080)
- Data: 8 bits
- Instruction, 8, 16, or 24 bits

MEMORY SIZE
RAM: 16K bytes expandable to 64K bytes using optional modules.

ROM: 2K bytes expandable to 14K bytes in 256 byte increments using optional PROM modules.

PROM: 256 bytes expandable using optional 6K or 16K modules.

Total: RAM, ROM and PROM may be combined in user defined configurations up to a maximum of 64K bytes.

MACHINE CYCLE TIME
Host Processor (Intel 8080): 2.0 μS

BUS TRANSFER RATE
Maximum bus transfer rate of 5 MHz.

SYSTEM CLOCKS
Host Processor (Intel 8080) Clock: Crystal controlled at 2 MHz ±0.1%.

Bus Clock: Crystal controlled at 9.8304 MHz ±0.1%.

I/O INTERFACES
CRT:
- Baud Rates: 110/300/600/1200/2400/4800/9600 (selectable).
- Code Format: 7–12 level code (programmable).
- Parity: Odd/even (programmable).
- Interface: TTL/RS232C (selectable).

TTY:
- Baud Rate: 110
- Code Format:
  - Input: 10 level or greater.
  - Output: 11 level.
  - Parity: Odd.
  - Interface: 20 mA current loop.

High Speed Paper Tape Reader:
- Transfer Rate: 200 cps.
- Control: 2-bit output. 1-bit input.
- Data: 8-bit byte
- Interface: TTL

Punch:
- Transfer Rate: 75 cps
- Control: 2-bit output 1-bit input
- Data: 8-bit byte
- Interface: TTL

Printer:
- Transfer Rate: 165 cps
- Control: 2-bit status input 1-bit output
- Data: ASCII
- Interface: TTL

PROM Programmer:
- Control: 3 strobes for multiplexed output data.
- Data: 8-bit bidirectional
- Interface: TTL

GENERAL PURPOSE I/O (OPTIONAL)
Input Ports: 8-bit TTL compatible (latched or unlatched); expandable in 4 port increments to 44 input ports.

Output Ports: 8-bit TTL compatible (latched); expandable in 4 port increments to 44.

Interrupts: 8 TTL compatible interrupt lines.

INTERRUPT
8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

DIRECT MEMORY ACCESS
Standard capability on Intellec bus; implemented for user selected DMA devices through optional DMA module – maximum transfer rate of 2 MHz.

MEMORY ACCESS TIME
RAM: 450 ns
PROM: 1.3 μs using Intel 8708A PROM.

PHYSICAL CHARACTERISTICS
Dimensions: 8.5" X 19" X 17"
21.6 cm X 48.3 cm X 43.2 cm

Weight: 65 lb (29.5 kg)

ELECTRICAL CHARACTERISTICS

DC POWER SUPPLY (Volts)	POWER SUPPLY CURRENT (Amps)	BASIC SYSTEM CURRENT REQUIREMENTS (Amps)	
		Maximum	Typical
+ 5 ±5%	35.0	9.0	6.6
+12 ±5%	3.0	0.7	0.4
–10 ±5%	3.0	0.2	0.2
–12 ±5%	0.5	––	––

AC POWER REQUIREMENTS
50–60 Hz; 115/230 VAC; 150 Watts

ENVIRONMENTAL CHARACTERISTICS
Operating Temperature: 0 to 55°C

DEVELOPMENT SYSTEMS

SOFTWARE SPECIFICATIONS

CAPABILITIES

System Monitor:

Devices supported include:
- ASR 33 teletype
- Intel high speed paper tape reader
- Paper tape punch
- CRT
- Printer
- Universal PROM programmer
- 4 logical devices recognized
- 16 physical devices maximum allowed

Macro Assembler:

800 symbols in standard system; automatically expandable with additional RAM memory to 6500 symbols maximum.

Assembles all seventy-eight 8080 machine instructions plus 10 pseudo-operators.

Text Editor:

12K bytes of workspace in standard system; automatically expandable with additional RAM memory to 58K bytes.

OPERATIONAL ENVIRONMENTAL

System Monitor:

Required hardware:
- Intellec System
- 331 bytes RAM memory
- 2K bytes ROM memory
- System console

Macro Assembler:

Required hardware:
- Intellec System
- 12K bytes RAM memory
- System console
- Reader device
- Punch device
- List device

Required software:
- System monitor

Text Editor:

Required hardware:
- Intellec System
- 8K bytes RAM memory
- System console
- Reader device
- Punch device

Required software:
- System monitor

Tape Format:

Hexadecimal object format.

OPTIONS

MDS-016	16K Dynamic RAM
MDS-406	6K PROM (sockets and logic)
MDS-416	16K PROM (sockets and logic)
MDS-501	DMA Channel Controller
MDS-504	General Purpose I/O Module
MDS-600	Prototype Module
MDS-610	Extender Module
MDS-620	Rack Mounting Kit

EMULATORS/SIMULATOR

MDS-ICE-30	3001 In-Circuit Emulator
MDS-ICE-80	8080 In-Circuit Emulator
MDS-SIM-100	Bipolar ROM Simulator
MDS-ICE-48	8748 In-Circuit Emulator
MDS-ICE-85	8085 In-Circuit Emulator

PERIPHERALS

MDS-UPP	Universal PROM Programmer
MDS-PTR	High Speed Paper Tape Reader
MDS-DOS	Diskette Operating System

INTERFACE CABLES/CONNECTORS

MDS-920	High Speed Punch Interface Cable
MDS-930	Peripheral Extension Cable
MDS-940	DMA Cable
MDS-950	General Purpose I/O Cable
MDS-960	25-pin Connector Pair
MDS-970	37-pin Connector Pair
MDS-980	60-pin Motherboard Auxiliary Connector
MDS-985	86-pin Motherboard Main Connector
MDS-990	100-pin Connector Hood

EQUIPMENT SUPPLIED

Central Processor Module
RAM Memory Module
Monitor Module (System I/O)
Front Panel Control Module
Chassis with Motherboard
Power Supplies
Finished Cabinet
Front Panel
ROM Resident System Monitor
RAM Resident Macro Assembler
RAM Resident Text Editor
Hardware Reference Manual
Reference Schematics
Operator's Manual
8080 Assembly Language Programming Manual
System Monitor Source Listing
8080 Assembly Language Reference Card
TTY Cable
European AC Adapter
AC Cord
Diagnostic Program & Manual

INTELLEC® 4/MOD40 MICROCOMPUTER DEVELOPMENT SYSTEM

Complete hardware/software development system for the design and implementation of 4040 CPU based microcomputer systems

TTY interfaces, front panel designer's console, and high-speed paper tape reader interface, in conjunction with PROM resident system monitor provide complete program loading, punching, monitoring, interrogation, and alteration capabilities

Program RAM (4K 8-bit bytes) provides a program development medium which lends itself to rapid and facile program monitoring and alteration

Data RAM (320 4-bit bytes expandable to 2560 bytes) provides data storage capacity

Program PROM (expandable to 4K 8-bit bytes) in conjunction with the resident PROM programmer provide capability of simulating final ROM resident program

PROM resident system monitor, RAM resident macro-assembler with edit feature included in standard systems software

Includes such standard program development features as program single-step address search (and pass count), next instruction indication, and program flow verification

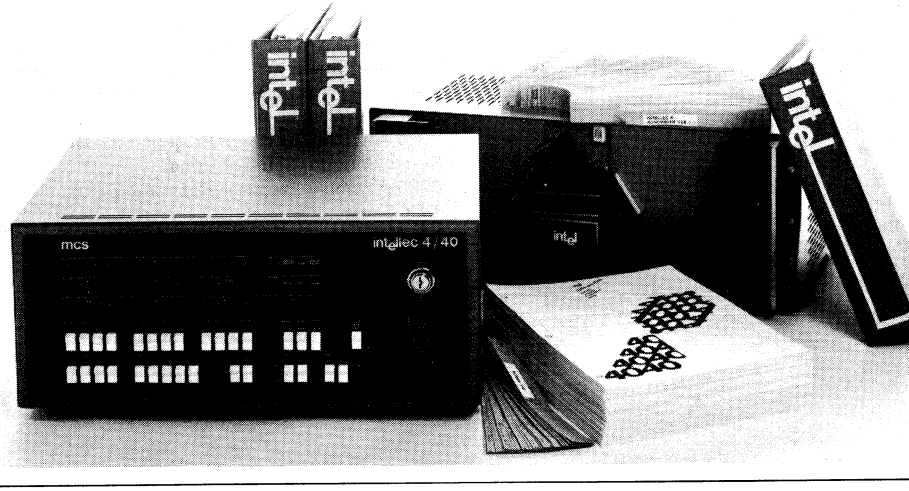
I/O expandable to 16 4-bit input ports and 48 4-bit output ports (all TTL compatible), allowing "hands-on" simulation of entire user system (processor and peripheral devices)

RESET, STOP, INTERRUPT control signals available to user via back panel

Modular design with expansion capability provided for up to 11 optional or user designed modules

The Intellec 4/MOD 40 (imm 4-44A) is a complete, self-contained microcomputer development system designed specifically to support the development and implementation of 4040 CPU based microcomputer systems. Its modular design provides the flexibility to adapt to any size user system and the resident software facilitates the resident software facilitates program development.

The basic Intellec 4/MOD 40 Microcomputer Development System consists of four microcomputer modules (CPU, RAM, MEMORY CONTROL, and PROM PROGRAMMER), power supplies, I/O connectors, console, and displays. The heart of the system is the imm 4-43 Central Processor Module built around Intel's high performance 4-bit 4040 CPU. The imm 4-43 is a complete microcomomputer system containing the system clock, 1K 8-bit bytes of PROM memory, 320 4-bit bytes of data RAM memory, three 4-bit input ports and eight 4-bit output ports. The imm 6-28 Program RAM Memory Module contains a 4K X 8 memory array composed of Intel® 2102 Static Random Access Memory elements. The imm 4-72 Control Module contains the circuitry required to interface the central processor module to the program RAM module. The imm 6-76 PROM Programmer Module provides the capability of programming Intel 1702A PROMs in conjunction with the front panel PROM socket and system monitor. All I/O ports are TTL compatible and accessible from the back panel 37-pin connectors. The front panel designer's console provides a means of monitoring and controlling system operation.



DEVELOPMENT SYSTEMS

The Intellec modular design allows great design system flexibility. Program PROM can be expanded to 4K 8-bit bytes using imm 6-26 or imm 4-22 optional modules. Data RAM can be expanded to 2560 4-bit bytes using imm 4-24 modules. I/O capability can be expanded to 16 4-bit input and 48 4-bit output ports using optional imm 4-60 modules. The Universal Prototype Card (imm 6-70) in conjunction with the 11 optional card sockets (which contain all essential system signals) provide the capability for interfacing custom designed modules.

The user RESET IN/OUT, STOP/STOP ACKNOWLEDGE, and INTERRUPT/INTERRUPT ACKNOWLEDGE control signals are all available at the back panel. Hence, the user can interrupt, halt, and reset the resident CPU via his own interface.

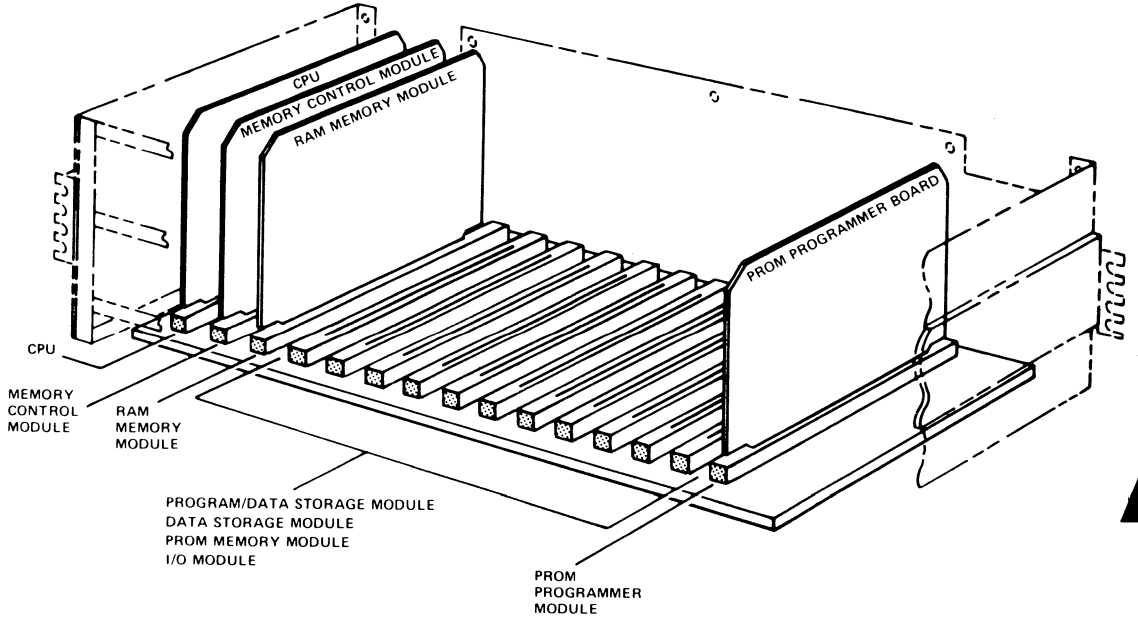
Program interrogation and alteration can be accomplished by using any desired combination of the front panel designer's console, a teletype, the imm 4-90 High-Speed Paper Tape Reader, and other Intellec compatible peripherals. The front panel designer's console provides the capability of manually writing data into memory and displaying memory contents, monitoring CPU bus contents during each processor subcycle, "freezing" system status after execution of a predefined instruction after a specified number of passes, single-stepping the program and verifying program flow. The teletype and reader serve as vehicles to input and output paper tapes and execute the system monitor.

Every Intellec 4/MOD 40 comes with three systems software products – the PROM resident system monitor, the RAM resident macro-assembler. The system software is a powerful application program development tool.

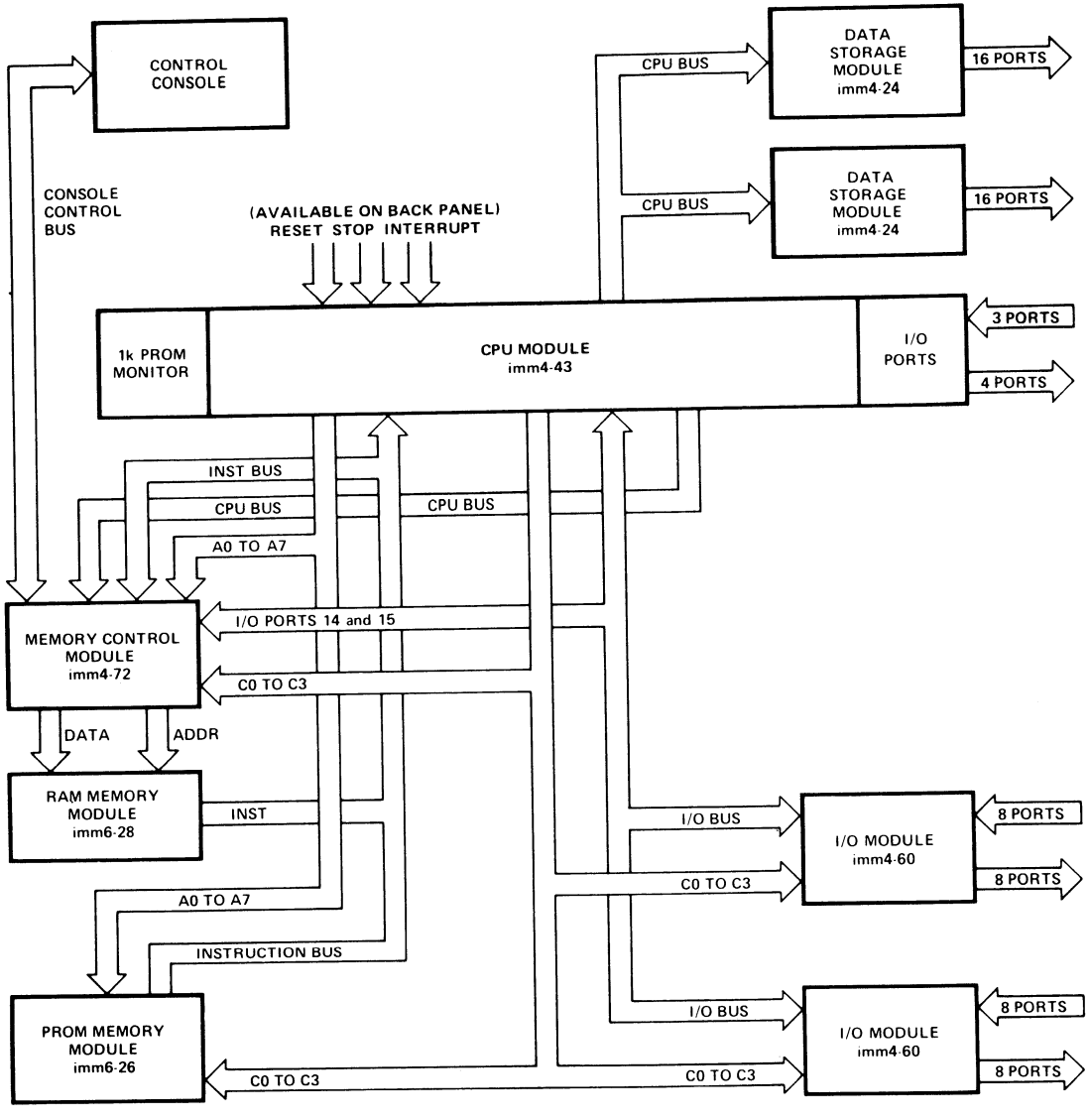
The system monitor provides the capability of displaying and modifying memory contents, reading and punching object tapes, dynamically assigning system peripherals, program and verify PROMs, and perform other functions which significantly reduce program debug and development time.

The Intellec 4/MOD 80 RAM resident macro-assembler translates source code into object code which will execute on the Intellec 4/MOD 40 or any MCS-40™ system. The assembler collects information from the source program, builds an internal symbol table, outputs a listing of the assembled program including error messages, and punches an object program tape. The assembler also contains a paper tape edit feature.

The standard Intellec® 4/MOD 40 comes with the modules shown. Expansion capability of both I/O and Memory to a full MCS-40™ system is provided by using open locations on the motherboard.



INTELLEC® 4/MOD 40 MODULE ASSIGNMENT



*Memory control module selects MONITOR, PROM or RAM for EXECUTION.

SYSTEMS BLOCK DIAGRAM

SPECIFICATIONS

WORD SIZE
Data: 4 bits
Instructions: 8 bits/16 bits

MEMORY SIZE
5K bytes expandable to 12K bytes (combination of PROM, Data RAM, Program RAM) in three 4K byte memories selectable for execution from the front panel.

INSTRUCTION SET
60, including conditionals, binary and decimal arithmetic, and I/O.

MACHINE CYCLE TIME
10.8 μs

SYSTEM CLOCK
Crystal-controlled at nominal 5.185 MHz.

I/O CHANNELS
All ports are 4-line TTL. Three input ports expandable to 16. Eight output ports expandable to 48.

INTERRUPT
Available at back panel.

CONSOLE MEMORY ACCESS
Standard via control console.

MEMORY ACCESS TIME
1 μs with standard memory modules.

ENVIRONMENTAL CHARACTERISTICS
Operating Temperature: 0°C to 55°C.

ELECTRICAL CHARACTERISTICS
DC Power Supplies:
V_{CC} = 5V ±5% I_{CC} = 12A
V_{DD} = −10V ±5% I_{DD} = 1.8A
AC Power Supplies:
MOD 40: 60 Hz, 115 VAC @ 200W
MOD 40/220: 50 Hz, 230 VAC @ 220W

PHYSICAL CHARACTERISTICS
Intellec® 4/40: 7" X 17-1/8" X 12-1/4" (table-top only); optional rack mount available.
Weight: 30 lb (13.61 kg)

OPTIONAL MODULES
Available for the Intellec® 4/MOD 40:
imm 4-22 Instruction/Data Storage Module
imm 4-24 Data Storage Module
imm 4-60 Input/Output Module
imm 6-26 PROM Memory Module
imm 6-28 RAM Memory Modules (additional)
imm 6-36 Rack Mounting Kit
imm 6-70 Universal Prototype Module
imm 6-72 Module Extender
imm 4-80 High-Speed Paper Tape Reader

EQUIPMENT SUPPLIED
imm 4-43 Central Processor Module
imm 6-28 RAM Memory Module
imm 6-76 PROM Programmer Module
Memory Control Module
Chassis with Motherboard
Power Supplies
Control and Display Panel
Finished Cabinet
PROM Resident System Monitor
RAM Resident Assembler
Programmer's Manual
Operator's Manual
Hardware Reference Manual
Module Schematics

ICE-30™
3001 MCU IN-CIRCUIT EMULATOR

Extends the Intellec® diagnostic capabilities into user configured systems, allowing in-circuit emulation of the user system's 3001 MCU

Direct Intellec® System connection to the user configured system is achieved via an external cable with 3001 compatible 40-pin connector

Provides for the display of all 3001 address, status, and control lines for the current micro-instruction executed.

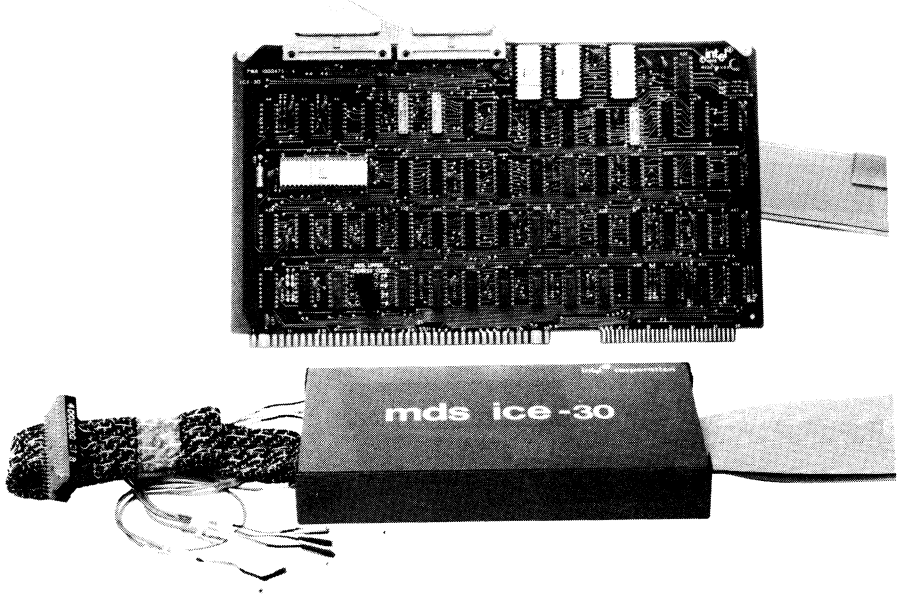
Allows for single-step microprogram execution.

Presets the 9-bit 3001 Microprogram Address Register and sets two independent breakpoints on micro-instruction addresses generated by the 3001

Allows two independent breakpoints to be set on the logical combination of any three TTL compatible signals in the user system via three logic probes

Allows the microprogram word contents to be displayed and modified when used with the optional ROM-SIM modules

ICE-30 is an Intellec resident module that provides the user with direct in-circuit emulation of the 3001 Microprogram Control Unit (MCU) and complete control over the execution of user developed microprograms. Through in-circuit emulation, the designer is able to set microprogram address breakpoints, single-step microprogram execution, and monitor all of the address, status, and control lines of the 3001.

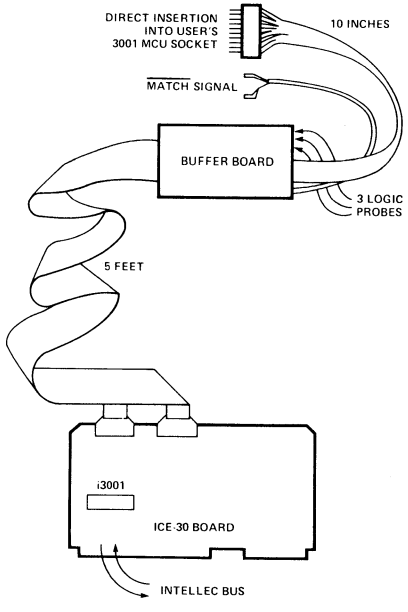


DEVELOPMENT SYSTEMS

HARDWARE

ICE-30 consists of a single PC board that resides in the Intellec System. An external cable from the board, terminating in a 3001 compatible 40-pin connector, forms the interface to the user system. Through the 3001 compatible connector, ICE-30 plugs directly into the user system's 3001 socket and allows the user to completely monitor and control all the activities of the MCU.

The figure below shows the hardware supplied with the ICE-30 package.



ICE-30 MODULE HARDWARE

By inserting the board into the Intellec Bus inside a basic Intellec system, a 3001 MCU chip in the user's system may be emulated. The ICE-30 board contains a 3001 MCU and peripheral logic required to monitor the 3001 operation and store trace information. The external cable carries status and control lines to and from the 3001 compatible 40-pin connector and the three logic probe lines. In addition, a MATCH line is brought out on the external cable which allows ICE-30 to control the user system's master clock and perform microprogram halt and single-step functions.

SOFTWARE

The ICE-30 Software Driver, ICE30SD, is an Intellec Microcomputer Development System RAM-resident program which provides a user interface with the ICE-30 hardware. ICE30SD recognizes a set of commands issued by the user, translates the commands, and places the encoded results into a control block for the hardware. In this fashion, the user can establish a dialogue with the 3001 Microcomputer Control Unit (MCU) which is connected to the system, thus providing the capability to monitor, control or alter its operation.

ICE30SD is capable of operating in conjunction with a RAM-based microprogram in the optional ROM-SIM modules (see ROM-SIM Data Sheet #98-211A). The commands provided by ICE30SD may therefore be divided into three categories: (1) Those commands unique to the optional ROM simulator, (2) Those which support ICE30SD functions, and (3) Those commands which are common to both ROM-SIM and ICE30SD.

ICE30SD FUNCTION COMMANDS

SET	Assign values to the two hardware breakpoint registers, the 9-bit microprogram address register, and the PR latch.
GO	Initiates real-time emulation which continues until an address encountered matches one of the two breakpoint values.
STEP	Causes execution to proceed in a non-real-time single-step micro-instruction mode.
CONTINUE	Resumes step mode execution following a break condition.
ENABLE	Activates or deactivates the two hardware breakpoint registers prior to issuing the 'GO' command.
TRAP	Used to set or remove any of the five-step mode software traps (software breakpoint registers).

COMMON COMMANDS

(Common to ICE30SD and Optional ROM-SIM)

DISPLAY	Displays the contents of a specified address or address range in the simulated control storage.
BASE	Establishes a mode of display of all output data for the 'DISPLAY' command.
RESTART	Reinitializes all program variables, except the ROM-SIM configuration values, and starts execution at the point following the ROM-SIM configuration sequence.
EXIT	Causes ICE30SD to terminate.

ROM-SIM COMMANDS

ICE30SD provides commands necessary to drive the optional Intellec microprogram control storage simulation module, ROM-SIM. For a description of ROM-SIM capabilities, ask for the ROM-SIM Data Sheet #98-211A.

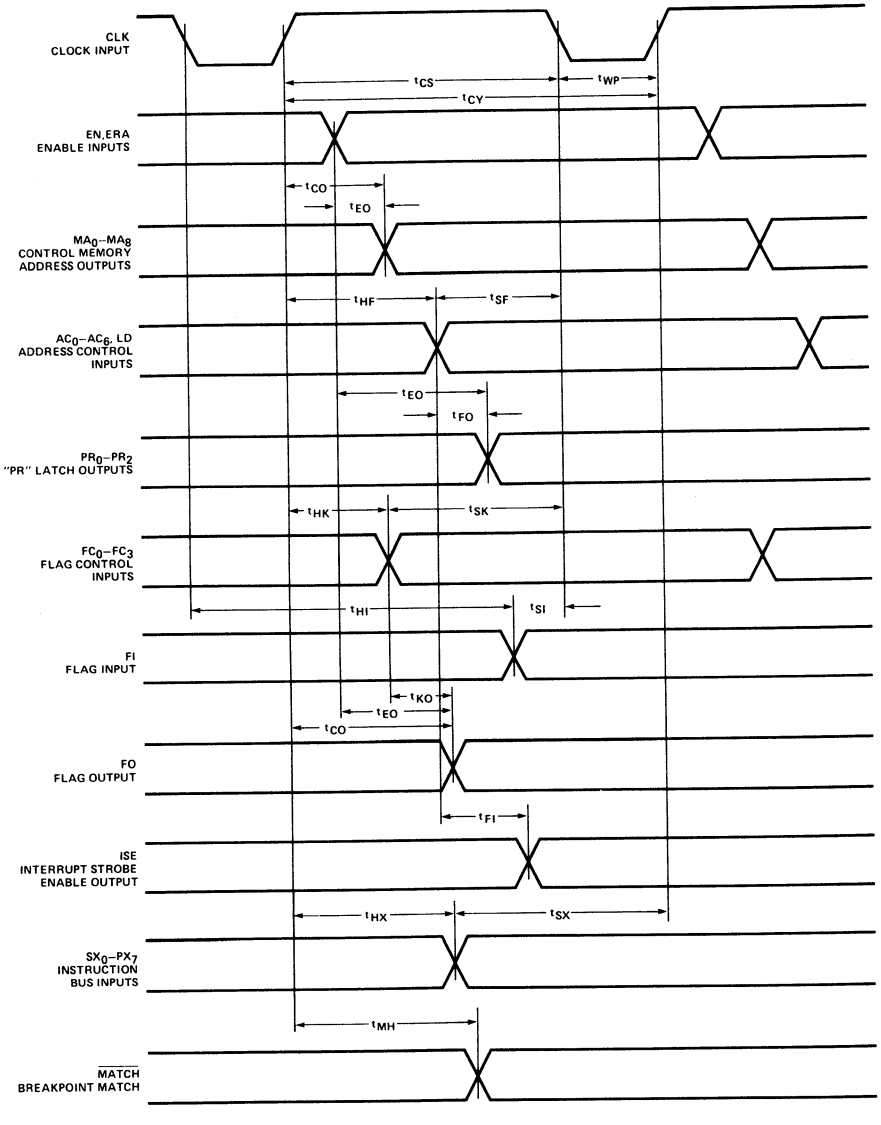
ICE30SD is written in Intel's high-level programming language PL/M and will execute in the minimum 16K RAM Intellec configuration.

OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias . . . . . 0° to 45°C
Storage Temperature . . . . . -20°C to +75°C
All Output and Supply Voltages. . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.



DEVELOPMENT SYSTEMS

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 45°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT	CONDITIONS
V_C	Input Clamp Voltage (All Input Pins)		-0.8	-1.5	V	I_C = -12 mA
I_F	Input Load Current:					
	CLK Input			-2.0	mA	V_F = 0.45V
	Logic Probe Inputs			-3.0	mA	
	All Other Inputs			-0.4	mA	
V_{IL}	Input Low Voltage			0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0			V	V_{CC} = 5.0V
I_{CC}	Power Supply Current			0.0	mA	
V_{OL}	Output Low Voltage					
	PR_0–PR_2		0.35	0.45	V	I_{OL} = 16 mA
	All Other Outputs		0.35	0.45	V	I_{OL} = 40 mA
V_{OH}	Output High Voltage					
	MA_0–MA_8, ISE, FO	2.4	3.0		V	I_{OH} = -2 mA
I_{OS}	Output Short Circuit Current					
	MA_0–MA_8, ISE, FO	-40		-120	mA	V_{CC} = 5.0V(2)
$I_{O(OFF)}$	Off-State Output Current					
	MA_0–MA_8, FO			-100	μA	V_0 = 0.45V
	MA_0–MA_8, FO, PR_0–PR_2			100	μA	V_0 = 5.25V

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Not more than one output should be shorted at one time.

A.C. CHARACTERISTICS

T_A = 0°C to 45°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	MIN	TYP(1)	MAX	UNIT
t_{CY}(2)	Cycle Time	185	120		ns
t_{WP}	Clock Pulse Width	35	20		ns
t_{CS}	Clock Pulse Separation	150			
	Control and Data Input Set-Up Times:				
t_{SF}	LD, AC_0–AC_6	13			ns
t_{SK}	FC_0, FC_1	13			ns
t_{SX}	SX_0–SX_3, PX_4–PX_7	13			ns
t_{SI}	FI	13			ns
	Control and Data Input Hold Times:				
t_{HF}	LD, AC_0–AC_6	15			ns
t_{HK}	FC_0, FC_1	15			ns
t_{HX}	SX_0–SX_3, PX_4–PX_7	15			ns
t_{HI}	FI				
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (MA_0–MA_8, FO)		90	137	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		78	130	ns
t_{FO}	Propagation Delay from Control Inputs AC_0–AC_6 to Latch Outputs (PR_0–PR_2)		98	150	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (MA_0–MA_8, FO, PR_0–PR_2)			50	ns
t_{FI}	Propagation Delay from Control Inputs AC_0–AC_6 to Interrupt Strobe Enable Output (ISE)		86	140	ns
t_{MH}	Propagation Delay from Clock Input (CLK) to Breakpoint Match MATCH			158	ns

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. $t_{CY} = t_{CO} + t_{SF} + t_{WP}$.
3. Pin input capacitance/output capacitance is 50 pF maximum.

SPECIFICATIONS

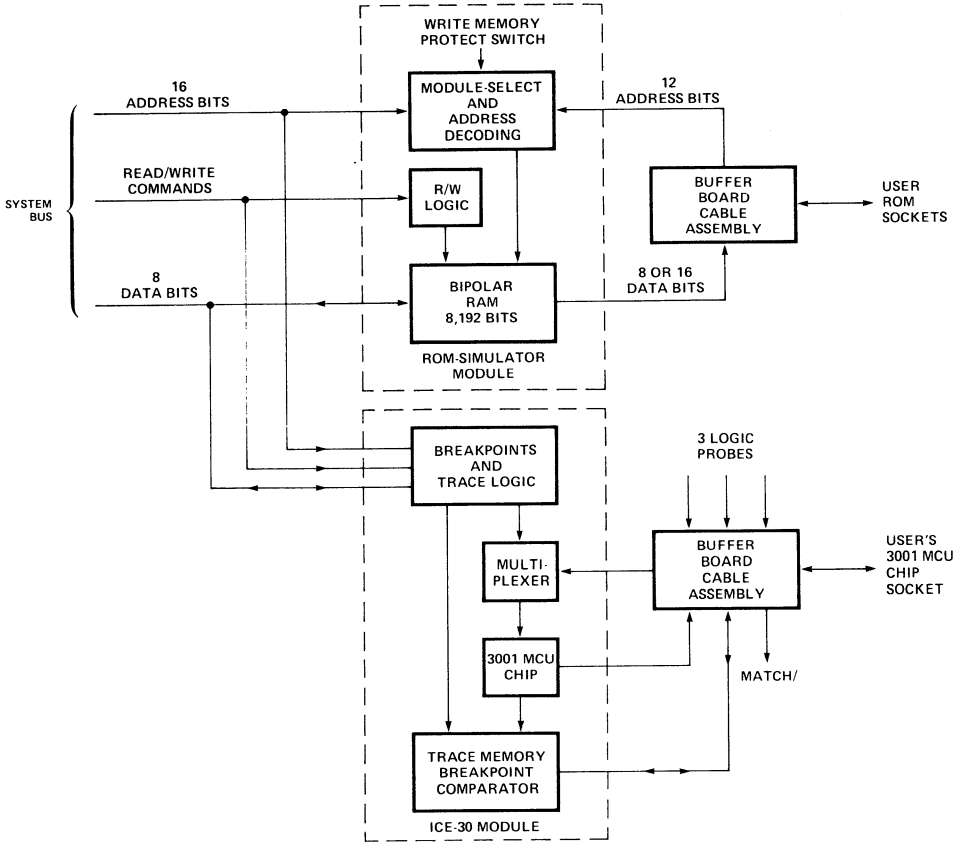
PHYSICAL CHARACTERISTICS
(Printed Circuit Board)

Width: 12.00 in.
Height: 6.75 in.
Depth: 0.50 in.

EQUIPMENT SUPPLIED
Printed Circuit Board
Interface Cables and
Buffer Enclosure Assembly
Reference Manual
Software Paper Tape

ORDERING INFORMATION
PART NUMBER
MDS-30-ICE

DESCRIPTION
3000 Series In-Circuit Emulator



FUNCTIONAL BLOCK DIAGRAM OF ICE-30 MODULE,
OPERATING IN CONJUNCTION WITH
ROM-SIMULATOR MODULE

DEVELOPMENT SYSTEMS

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

ICE-48™
8048 IN-CIRCUIT EMULATOR

- Connects Intellec® Microcomputer Development System to user configured system via an external cable and 40-pin plug, replacing the user 8048
- Emulates user system 8048
- Allows user configured system to borrow static RAM memory for program debug
- Provides hardware comparators for user designated break conditions
- Eliminates the need for extraneous debugging tools residing in the user system
- Collects address, data and 8048 status information on machine cycles emulated
- Provides capability to examine and alter CPU registers, memory, flag values, and to examine pin and port values
- Integrates hardware and software efforts early to save development time

The ICE-48™ Module is an Intellec® System resident module that interfaces to any user configured 8048 system. With an ICE-48 Module as a replacement for a prototype system 8048, the designer can emulate the system 8048 in real time, single-step the system's program, and borrow static RAM memory for user system debugging. Powerful hardware and software debug functions are extended into the user system with minimum impact. The designer may examine and modify his system with symbolic references instead of absolute values.

DEVELOPMENT SYSTEMS

Integrated hardware/software development can begin as soon as there is an 8048 CPU socket for the prototype system. Through the ICE-48 module's mapping capabilities, blocks of static RAM memory can be accessed to allow program modification. An output signal provides a synchronization pulse for an oscilloscope or other test equipment when a break condition is recognized. The user has the option of breaking the emulation or using the signal for hardware diagnosis. Attempting to mesh completed hardware and software products can be costly and frustrating. Hardware and software can help debug each other as they are developed using an ICE-48 module.

The ICE-48 module is a microcomputer system utilizing Intel's 8048 microprocessor as its nucleus. This system communicates with the Intellec system 8080 processor via direct memory access. Host processor commands and ICE-48 status are interchanged through a DMA channel. A parameter block resident in Intellec System main memory contains detailed configuration and status information transmitted at an emulation break.

ICE-48 hardware consists of two PC boards, which reside in the Intellec System chassis, and a cable assembly which interfaces to the user system. A 40-pin socket on the end of the cable assembly plugs directly into the socket provided for the user's 8048.

The ICE-48 software is an Intellec System program which provides the user with flexible, easy-to-use commands for defining breakpoints, initiating emulation, and interrogating and altering user system status recorded during emulation. A broad range of commands provides the user with maximum flexibility in describing the operation to be performed.

SPECIFICATIONS

ICE48SD OPERATING ENVIRONMENT

Paper Tape-Based ICE-48™ Software
Required Hardware:
- Intellec® Microcomputer Development System
- System Console
- Reader Device
- Punch Device
- ICE-48 Module

Required Software:
- System Monitor

Diskette-Based ICE-48 Software
Required Hardware:
- Intellec® Microcomputer Development System
- System Console
- System Diskette Operating System
- ICE-48 Module

Required Software:
- System Monitor
- ISIS-II

EQUIPMENT SUPPLIED

Printed Circuit Boards
Interface Cables and Buffer Module
Hardware Reference Manual
Operator's Manual
Schematic Diagram
ICE-48 Software, paper tape version (ICE-48 Software, diskette-based version, is supplied with MDS-D48 8048 Software Support Package)

ORDERING INFORMATION

Part Number	Description
MDS-48-ICE	8048 CPU In-Circuit Emulator, Cable Assembly and Interactive Software included

ICE-80™
8080 IN-CIRCUIT EMULATOR

Connects Intellec® System to user configured system via an external cable and 40-pin plug, replacing the user 8080

Allows real-time (2 MHz) emulation of the user system 8080

Allows user configured system to share Intellec RAM, ROM and PROM memory and Intellec I/O facilities

Checks for up to three hardware and four software break conditions

Offers full symbolic debugging capabilities

Eliminates the need for extraneous debugging tools residing in the user system

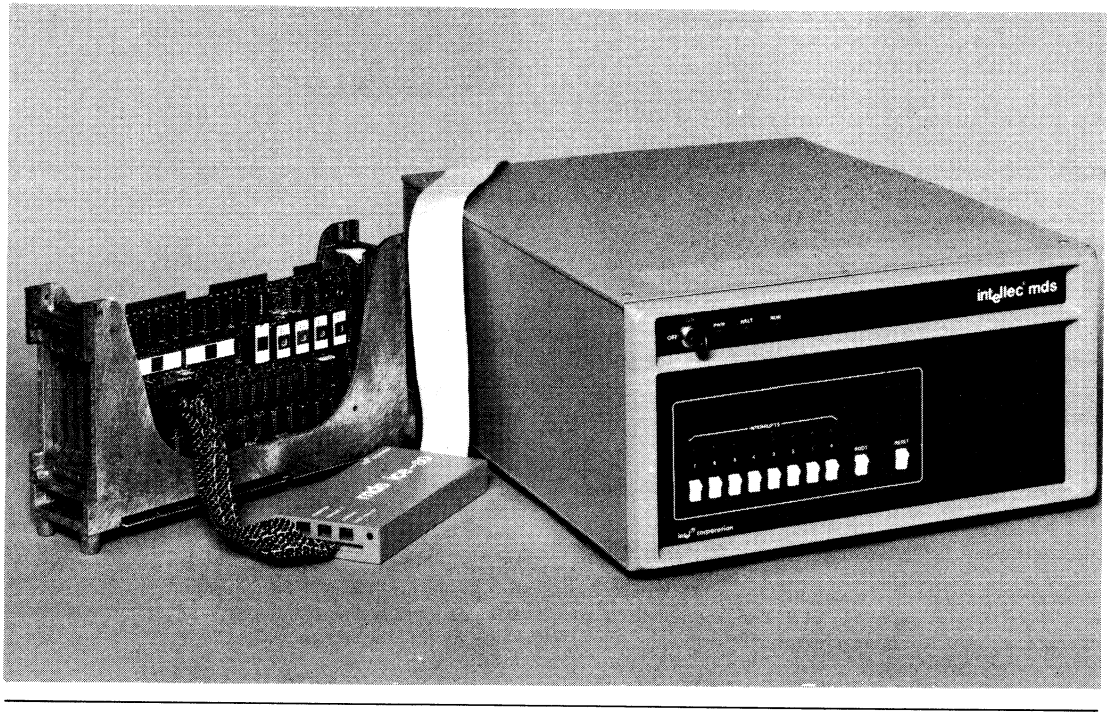
Provides address, data and 8080 status information on last 44 machine cycles emulated

Provides capability to examine and alter CPU registers, main memory, pin and flag values

Integrates hardware and software development efforts

Available in diskette or paper tape versions

The Intellec In-Circuit Emulator/80 (ICE-80) is an Intellec resident module that interfaces to any user configured 8080 system. With ICE-80 as a replacement for a prototype system 8080, the designer can emulate the system's 8080 in real time, single-step the system's program, and substitute Intellec memory and I/O for user system equivalents. Powerful Intellec debug functions are extended into the user system. For the first time the designer may examine and modify his system with symbolic references instead of absolute values.



INTEGRATED HARDWARE/ SOFTWARE DEVELOPMENT

The user prototype need consist of no more than an 8080 CPU socket and a user bus to begin integration of software and hardware development efforts. Through ICE-80 mapping capabilities, system resources can be accessed for missing prototype hardware. Hardware designs can be tested using the system software which will drive the final product.

The system integration phase, which can be so costly and frustrating when attempting to mesh completed hardware and software products, becomes a convenient two-way debug tool when begun early in the design cycle.

SYMBOLIC DEBUGGING

ICE-80 allows the user to make symbolic references to memory addresses and data in his program. Symbols may be substituted for numeric values in any of the ICE-80 commands. The user is relieved from looking up addresses of variables or program subroutines.

The user symbol table generated along with the object file during a PL/M compilation or a MAC80 or resident assembly, is loaded to memory along with the user program which is to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that are found useful during system debugging. By referring to symbolic memory addresses, the user can be assured of examining, changing, or breaking at the intended location.

ICE-80 provides symbolic definition of all 8080 registers, flags, and selected pins. The following symbolic references are also provided for user convenience: TIMER, a 16-bit register containing the number of ϕ_2 clock pulses elapsed during emulation; ADDRESS, the address of the last instruction emulated; INTERRUPTENABLED, the user 8080 interrupt mechanism status; and UPPERLIMIT, the highest RAM address that can be occupied by user memory.

DEBUG CAPABILITY INSIDE USER SYSTEM

ICE-80 provides the user with the ability to debug a full prototype or production system without introducing extraneous hardware or software test tools.

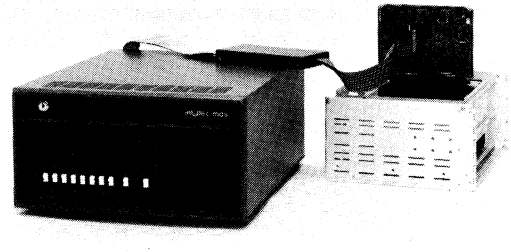
ICE-80 connects to the user system through the socket provided for the user 8080 in the user system. Intellec memory is used for the execution of the ICE-80 software, while I/O provides the user with the ability to communicate with ICE-80 and receive information on the operation of the user system.

MEMORY AND I/O MAPPING

Memory and I/O for the user system can be resident in the user system or "borrowed" from the Intellec System through ICE-80's mapping capability.

ICE-80 separates user memory into 16 4K blocks. User I/O is divided into 16 16-port blocks. Each block of memory or I/O can be defined independently. The user may assign system equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, memory or I/O can be accessed in place of suspect user system devices during prototype or production checkout.

The user can also designate a block of memory or I/O as nonexistent. ICE-80 issues error messages when memory or I/O designated as nonexisting is accessed by the user program.



ICE-80 INSTALLED IN USER SYSTEM

REAL TIME TRACE

ICE-80 captures valuable trace information while the user is executing programs in real time. The 8080 status, the user memory or port addressed, and the data read or written (snap data), is stored for the last 44 machine cycles executed. This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was user initiated or the result of an error condition.

For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multiple-step sequences tailored to system debug needs.

HARDWARE

The heart of ICE-80 is a microcomptuer system utilizing Intel's 8080 microprocessor as its nucleus. This system communicates with the Intellec® host processor via I/O commands. Host processor commands and ICE-80 status are interchanged through registers on the ICE-80 Trace Board. ICE-80 and the system also communicate through a Control Block resident in the Intellec® main memory which contains detailed configuration and status information transmitted at an emulation break.

ICE-80 hardware consists of two PC boards, the Processor and Trace Boards, residing in the Intellec® chassis, and a 6-foot cable which interfaces to the user system. The Trace and Processor Boards communicate with the system on the bus, and also with each other on a separate ICE-80 bus. ICE-80 connects to the user system through a cable that plugs directly into the socket provided for the user's 8080.

TRACE BOARD

The Trace Board talks to the system as a peripheral device. It receives commands to ICE-80 and returns ICE-80 responses.

While ICE-80 is executing the user program, the Trace Board collects data for each machine cycle emulated (snap data). The information is continuously stored in high-speed bipolar memory.

The Trace Board also contains two 24-bit hardware breakpoint registers which can be loaded by the user. While in emulation mode, a hardware comparator is constantly monitoring address and status lines for a match which will terminate an emulation. A user probe is also available which can be attached to any user signal. When this signal goes true a break condition is recognized.

The Trace Board signals the Processor Board when a command to ICE-80 or break condition has been detected. The ICE-80 CPU then sends data stored on the Trace Board to the Control Block in memory. Snap data, along with information on 8080 registers and pin status, and the reason for the emulation break are then available for access during interrogation mode. Error conditions, if present, are transmitted and automatically displayed for the user.

PROCESSOR BOARD

An 8080 CPU resides on the Processor Board. During emulation it executes instructions from the user's program. At all other times it executes instructions from the control program in the Trace Module's ROM.

The Processor Board contains an internal Clock Generator that provides the clocks to the user emulation CPU at 2 MHz. The CPU can alternately be driven by a clock derived from user system signal lines. The clock source is selected by a jumper option on the board. A timer on the Trace Board counts the ϕ_2 clock pulses during emulation and can provide the user with the exact timing of the emulation.

The Processor Board turns on an emulation when ICE-80 has received a RUN command from the system. It terminates emulation when a break condition is detected on the Trace Board, or the user's program attempts to access memory or I/O ports designated as nonexistent in the user system, or the user 8080 is inactive for a quarter of a second.

The Address Map located on the Processor Board stores the assigned location of each user memory or I/O block. During emulation the Processor Board determines whether to send/receive information on the Intellec or User bus by consulting the Address Map. The Processor Board allows the ICE-80 CPU to gain access to the bus as a master to "borrow" Intellec facilities. At an emulation break, the Processor Board stores the status of specified 8080 input and output signals, disables all interaction with the user bus, and commands the Trace Board to send stored information to a Control Block in Intellec memory for access during interrogation mode.

CABLE CARD

The Cable Card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector which plugs into the user system in the socket designed for the 8080 when enabled by the Processor Module's user bus control logic.

SOFTWARE

The ICE-80 software driver (ICE80SD) is a RAM-based program which provides the user with easy-to-use English language commands for defining breakpoints, initiating emulation, and interrogating and altering user system status recorded during emulation. ICE-80 commands are configured with a broad range of modifiers which provide the user with maximum flexibility in describing the operation to be performed.

ICE80SD is available in both paper tape and diskette-based versions. The diskette-based version, which is supplied on a System Diskette for operation with the Intellec Diskette Operating System, provides expanded capabilities for retrieving and storing user programs, as well as the standard peripherals available in the paper tape version.

EMULATION COMMANDS:

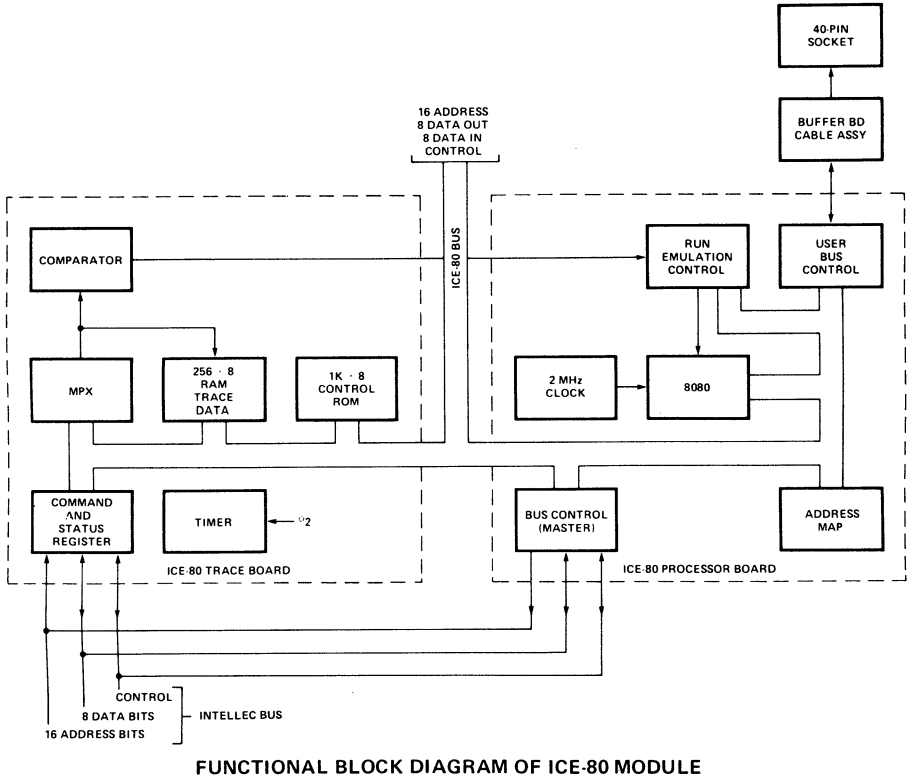
GO	Initiates real-time emulation and allows user to specify breakpoints, data retrieval, and conditions under which emulation should be reinitiated.
STEP	Initiates emulation in single or multiple instruction increments. User may specify a register dump or tailor diagnostic activity to his needs following each step, and define conditions under which stepping should continue.
RANGE	Delimits blocks of instructions for which register dump or tailored diagnostics are to occur.
CONTINUE	Resume real-time emulation.
CALL	Emulate user system interrupt.

INTERROGATION COMMANDS:

BASE	Establish mode of display for output data.
DISPLAY	Print contents of memory, 8080 registers, input ports, 8080 flags, 8080 pins, snap data, symbol table, or other diagnostic data on list device. Can also be used for base-to-base conversion, or addition or subtraction in any base.
CHANGE	Alter contents of memory, register, output port, or 8080 flag.
XFORM	Define memory and I/O status.
SEARCH	Look through memory range for specified value.

UTILITY COMMANDS:

LOAD	Fetch user symbol table and object code from input device.
SAVE	Send user symbol table and object code to output device.
EQUATE	Enter symbol name and value to user symbol table.
FILL	Fill memory range with specified value.
MOVE	Move block of memory data to another area of memory.
TIMEOUT	Enable/disable user CPU 1/4 second wait state timeout.
LIST	Define list device (diskette-based version only).
EXIT	Return program control to monitor.



FUNCTIONAL BLOCK DIAGRAM OF ICE-80 MODULE

SAMPLE, ICE-80 DEBUG SESSION

```
ISIS 8080 MACRO ASSEMBLER, V1.0                    PAGE 1

                ; USER PROGRAM TO OUTPUT A SERIES OF
                ; CHARACTERS TO SDK-80 CONSOLE DEVICE
                ;
1320                    ORG     1320H
01E3            C0      EQU     1E3H    ; SDK-80 CONSOLE OUT DRIVER
                ;
1320 0601       START:  MVI     B,1     ; SET UP B VALUE
1322 3A3613             LDA     DAT1    ; LOAD A WITH DAT1 VALUE
1325 4F         LOOP:   MDV     C,A
1326 CDE301             CALL    C0      ; SEND C VALUE TO CONSOLE
1329 79                 MOV     A,C     ; RESTORE A
132A 93                 SBB     B       ; SUBTRACT B FROM A
132B 323713             STA     RSLT    ; STORE RESULT IN RSLT
132E FE40               CPI     40H     ; LAST VALUE TO PRINT
1330 C22513             JNZ     LOOP    ; LOOP AGAIN IF A>40H
1333 C32013             JMP     START   ; ELSE RESTART WHOLE PROCEDURE
                ;
1336 5A         DAT1:   DB      5AH
1337            RSLT:   DS      1
0000                    END
```

```
ISIS, V1.0      INITIAL ICE-80 SESSION
-ICE80          (Note: The SDK-80 Monitor has already been used to initialize the SDK-80 Board)
ISIS ICE-80, V1.0
① **XFORM MEMORY 0 TO 1 U
  *XFORM IO 0FH U
② *LOAD PROG. HEX
  ERR=067
  STAT=11H TYPE=06H CMND=07H ADDR=1320H GOOD=06H BAD=04H
  *CHANGE MEMORY 1321H=FFH
  ERR=067
  STAT=11H TYPE=06H CMND=07H ADDR=1321H GOOD=FFH BAD=FDH
  *LOAD PROG. HEX
③ *GO FROM START UNTIL RSLT WRITTEN
  EMULATION BEGUN
④ ERR=067
  STAT=11H TYPE=07H CMND=02H
⑤ *DISPLAY CYCLES 5
  STAT=A2H ADDR=1326H DATA=CDH
  STAT=82H ADDR=1327H DATA=E3H
  STAT=82H ADDR=1328H DATA=01H
  STAT=04H ADDR=FFFFH DATA=13H
  STAT=04H ADDR=FFFEH DATA=29H
⑥ *CHANGE DOUBLE REGISTER SP=13FFH
  *BASE HEX
  *EQUATE STOP=1333H
⑦ *GO FROM START UNTIL STOP EXECUTED THEN DUMP
  EMULATION BEGUN
  B=01H C=41H D=00H E=00H H=00H L=00H F=56H A=40H P=1320H *=1333H S=13FFH
  EMULATION TERMINATED AT 1333H
⑧ *EXIT
  *FFFF
```

1. Set up user memory and I/O. The program is set up to execute in block 1 (1000H–1FFFH) of user memory, and requires access to the SDK-80 monitor (block 0) and I/O ports in block 0FH. Both ports and memory are defined as available to the user system. All other memory and I/O is initialized by ICE-80 as nonexistent (guarded).
2. A load command generates an error. The type and command numbers indicate that a data mismatch occurred on a write to memory command. The data to be written to address 1320H should have been 06H. When ICE-80 read the data after writing it, a 04H was detected. A change command to a different memory address hints that bit 1 does not go to 1 anywhere in this memory block. Examination indicates that a pin was shorted on the RAM located at 1300H–13FFH in the prototype system. The problem is fixed and a subsequent load succeeds.
3. A real-time emulation is begun. The program is executed *FROM* 'START' (1320H) and continues *UNTIL* 'RSLT' is written (in location 1328H, the contents of the accumulator is stored in (written into) 'RSLT').
4. An error condition results: TYPE 07, CMND 02 indicate the program accessed a guarded area.
5. The last 5 machine cycles executed are displayed. The last instruction executed was a call (CDH). The fourth and fifth cycles are a push operation (designated by status 04H) to store the program counter before executing the call. The stack pointer was not initialized in the program and is accessing memory location FFFFH.
6. After making a note to initialize the stack pointer in the next assembly, a temporary fix is effected by setting the stack pointer to the top of user available memory.
7. After setting the base for displays to hex and adding the symbol 'STOP' to the symbol table, emulation is started which will terminate when the instruction at 1333H ('STOP') is executed. When emulation terminates, a *DUMP* of the contents of user 8080 registers is requested. One can see that the value of the accumulator is set at 40H, the stack pointer is set at 13FFH, the last address executed (*) is 1333H, and the program counter has been set to 1320H.
8. *EXIT* returns control to the MDS monitor.

ICE80SD OPERATING ENVIRONMENT

Paper Tape-Based ICE80SD

Required Hardware:
- Intellec® System
- System console
- Reader device
- Punch device
- ICE-80

Required Software:
- System monitor

Diskette-Based ICE80SD

Required Hardware:
- Intellec® System
- 32K bytes RAM memory
- System console
- MDS-DOS Diskette Operating System
- ICE-80

Required Software:
- System monitor
- ISIS

EQUIPMENT SUPPLIED

Printed Circuit Modules (2)
Interface Cables and Buffer Board
Hardware Reference Manual
Operator's Manual
Schematic Diagram
ICE-80 Software Driver, paper tape version
(ICE-80 Software Driver, disketted-based version is supplied with Diskette Operating System)

SYSTEM CLOCK

Crystal controlled 2.185 MHz ±0.01%. May be replaced by user clock through jumper selection.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 8.00 lb (3.64 kg)

ELECTRICAL CHARACTERISTICS

DC Power:
- V_{CC} = +5V, ±5%
- I_{CC} = 9.81A maximum; 6.90A typical
- V_{DD} = +12V, ±5%
- I_{DD} = 79 mA maximum; 45 mA typical
- V_{BB} = −9V, ±5%
- I_{BB} = 1 mA maximum; 1 μA typical

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0°C to 40°C
Operating Humidity: Up to 95% relative humidity without condensation

CONNECTORS

Edge Connector: CDC VPB01E32A00A1

ORDERING INFORMATION

Part Number	Description
MDS-80-ICE	8080 CPU In-Circuit Emulator. Cable Assembly and Interactive Software included

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

ICE-85™
8085 IN-CIRCUIT EMULATOR

Connects Intellec® Microcomputer Development System to user configured system via an external cable and 40-pin plug, replacing the user 8085

Emulates user system 8085

Allows user configured system to share Intellec® memory and I/O facilities

Provides capability to examine and alter CPU registers, main memory, flag values, and to examine pin and port values

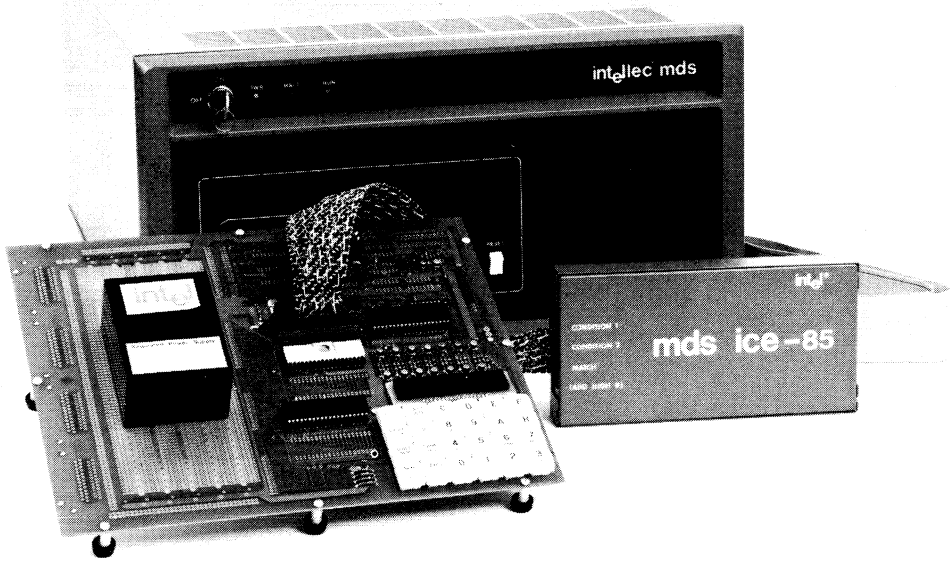
Eliminates the need for extraneous debugging tools residing in the user system

Collects address, data and 8085 status information on machine cycles emulated

Provides hardware comparators for user designated break conditions

Integrates hardware and software development efforts early to save development time

The ICE-85™ module is an Intellec System resident module that interfaces to any user configured 8085 system. With an ICE-85 module as a replacement for a prototype system 8085, the designer can emulate the system 8085, single-step the system's program, and substitute Intellec System memory and I/O for user system equivalents. Powerful hardware and software debug functions are extended into the user system with minimum impact. The designer may examine and modify his system with symbolic references instead of absolute values.



DEVELOPMENT SYSTEMS

Integrated hardware/software development can begin as soon as there is an 8085 CPU socket and a user bus for the prototype system. Through the ICE-85™ module, Intellec System equivalents can be accessed for missing prototype hardware. Hardware designs can be tested as they are developed in a "complete" system. An output signal provides a synchronization pulse for an oscilloscope or other test equipment when a break condition is recognized. The user has the option of breaking the emulation or using the signal for hardware diagnosis. Attempting to mesh completed hardware and software products can be costly and frustrating. Hardware and software can help debug each other as they are developed using an ICE-85 module.

The heart of the ICE-85 module is a microcomputer system utilizing Intel's 8085 microprocessor as its nucleus. Commands from the Intellec System host processor and ICE-85 status are interchanged through a DMA channel. A Parameter Block resident in Intellec System main memory contains detailed configuration and status information transmitted at an emulation break.

ICE-85 hardware consists of two PC boards which reside in the Intellec System chassis and a cable assembly which interfaces to the user system. A 40-pin socket on the end of the cable assembly plugs directly into the socket provided for the user's 8085.

The ICE-85 software is an Intellec System RAM-based program which provides the user with easy-to-use English language commands for defining breakpoints, initiating emulation, and interrogating and altering user system status recorded during emulation. A broad range of command modifiers provides the user with maximum flexibility in describing the operation to be performed.

ICE85 SOFTWARE OPERATING ENVIRONMENT

Paper Tape-Based ICE-85 software

Required Hardware:
- Intellec Microcomputer Development System
- System console
- Reader device
- Punch device
- ICE-85 module

Required Software:
- System monitor

Diskette-Based ICE-85 software

Required Hardware:
- Intellec Microcomputer Development System
- System console
- MDS-DOS Diskette Operating System
- ICE-85 module

Required Software:
- System monitor
- ISIS-II

EQUIPMENT SUPPLIED

Printed Circuit Boards
Interface Cables and Buffer Module
Hardware Reference Manual
Operator's Manual
Schematic Diagram
- ICE-85 Software, paper tape version
- (ICE-85 Software, diskette-based version, is supplied with ISIS-II System Diskette)

ORDERING INFORMATION

Part Number	Description
MDS-85-ICE	8085 CPU In-Circuit Emulator, Cable Assembly and Interactive Software included

INTELLEC® DISKETTE OPERATING SYSTEM

Floppy diskette operating system providing high-speed input/output and data storage for the Intellec® Microcomputer Development System

Supports all existing standard Intellec® peripherals

Data on flexible diskette addressed using IBM soft-sectored format which allows 1/4 million byte data capacity with up to 200 files per diskette

Supports the resident compiler for PL/M-80, Intel's high level programming language

Relocating macro assembler contains full macro and conditional assembly capability

Linker automatically combines separately assembled or compiled programs into a single relocatable module

Library manager for creating and up-dating program libraries

Command file facility allows console commands to be submitted from a diskette file

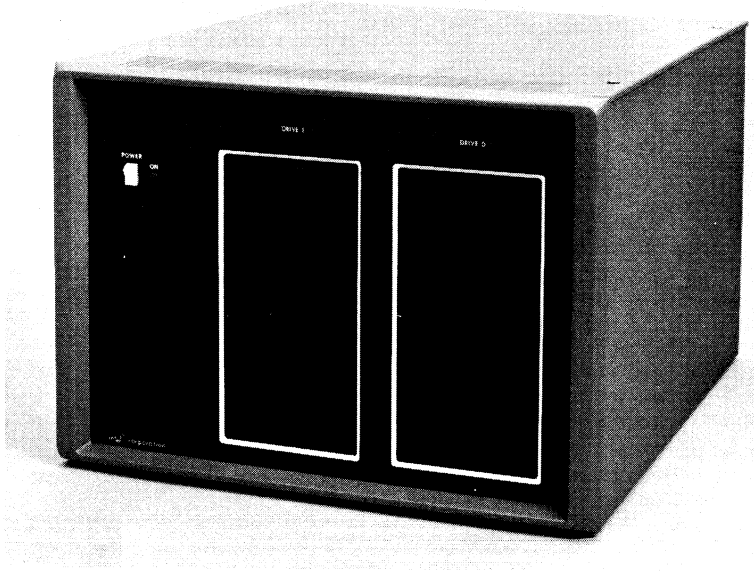
Diskette system text editor with string search, substitution, insertion, and deletion commands

Diskette operating system functions callable from user programs

Access to all Intellec® monitor facilities

Dynamic allocation and deallocation of diskette sectors for variable length files

The Intellec® Diskette Operating System is a sophisticated, general purpose, high speed data handler and file manipulation system for use with the Intellec Microcomputer Development System and its peripherals. The use of a single or dual drive Diskette Operating System significantly reduces program development time. The software system known as ISIS-II (Intel Systems Implementation Supervisor), provides the ability to edit, assemble, compile, link, relocate, execute and debug programs, and performs all file management tasks for the user.



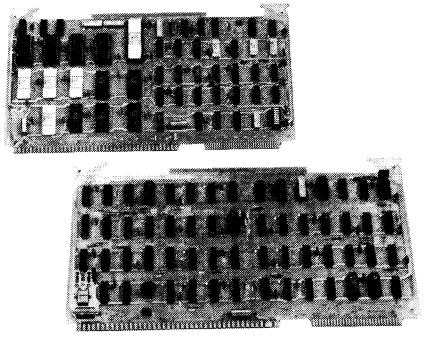
DISKETTE OPERATING SYSTEM DRIVES

DEVELOPMENT SYSTEMS

HARDWARE

The Intellec® diskette system provides direct access bulk storage, intelligent controller, and up to two diskette drives. Each drive provides 1/4 million bytes of storage with a data transfer rate of 250,000 bits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the Intellec System bus, as well as supporting the two diskette drives. The diskette system records all data in the IBM-compatible soft sector format.

The diskette controller consists of two boards, the Channel Board and the Interface Board. These two printed circuit boards reside in the Intellec System chassis and constitute the diskette controller. Each of the systems components is shown in the photograph, and are described in more detail in the following paragraphs.



DOS CHANNEL AND INTERFACE CONTROLLER BOARDS

CHANNEL BOARD

The *Channel Board* is the primary control module within the diskette system. The Channel Board receives, decodes, and responds to channel commands from the 8080 Central Processor Unit (CPU) in the Intellec system. The Channel Board can access a block of Intellec system memory to determine the particular diskette operations to be performed and fetch the parameters required for the successful completion of the specified operation.

The control functions of the Channel Board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 Central Processing Elements (2-bit slice per CPE), a 3001 Microprogram Control Unit, and 512 x 32 bits of 3604 programmable-read-only-memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the Channel Board.

INTERFACE BOARD

The *Interface Board* provides the diskette controller with a means of communication with the diskette drives, as well as with the Intellec system bus. Under control of the microprogram being executed on the Channel Board, the Interface Board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), cause the head to move to the proper track and verify successful operation. The Interface Board accepts the data being read off the diskette, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the Channel Board.

During write operations, the Interface Board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

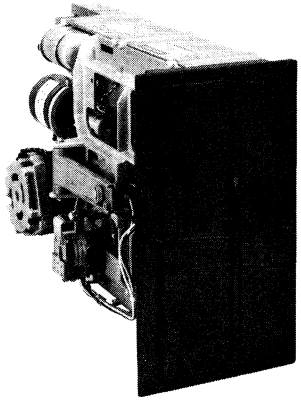
When the diskette controller requires access to Intellec system memory, the Interface Board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The Interface Board also acknowledges I/O commands as required by the Intellec bus.

The Diskette System is capable of performing seven different operations: recalibrate, seek, format track, write data, wire deleted data, read data, and verify CRC.

DISKETTE DRIVE MODULES

Each diskette drive consists of read/write and control electronics, drive mechanisms, read/write head, track positioning mechanism, and the removable floppy diskette platter. These components interact to perform the following functions:

- **Interpret and generate control signals.**
- **Move read/write head to selected track.**
- **Read and write data.**



ADDITIONAL DRIVE UNIT MDS-DRV

SOFTWARE — INTEL SYSTEMS IMPLEMENTATION SUPERVISOR (ISIS-II)

The ISIS-II operating system resides on the system diskette and supports a broad range of user-oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS-II Relocating Macro Assembler, Linker, Object Locator and Library Manager can be loaded from the diskette in seconds. All passes of the assembler can be executed without the need for user intervention. Object code and listings may be directed to any output device, or stored as diskette files.

Powerful system console commands are provided in an easy-to-use English context. Monitor mode can be entered by a special prefix to any system command or program call.

A file is a user-defined collection of information of variable length. ISIS-II also treats each of the standard Intellec® system peripherals as files through preassignment of unique file names to each device. In this manner data can be copied from one device to another (i.e., tape reader to tape punch) using the same command required to copy one diskette data file to another. ISIS-II provides automatic implementation of random access disk files. Each file is identified by a user-chosen name unique on its diskette. Up to 200 files may be stored on each 1/4 million byte diskette.

ISIS-II SYSTEM COMMANDS

The following ISIS-II system commands are designed to provide the user with a powerful, easy-to-use program and file manipulation capability:

ATTRIB	Assigns specified attributes to a file, such as write-protect.
COPY	Creates copies of existing diskette files or transfers files from one device to another.
DELETE	Removes a file from the diskette, thereby freeing space for allocation of other files.
DIR	Lists name, size and attributes of files from a specified diskette directory.
RENAME	Allows diskette files to be renamed.
FORMAT	Initializes a diskette and allows creation of additional system or data diskettes.
DEBUG	Loads a specified program from a diskette into memory and then transfers control to the Intellec monitor for execution and/or debugging.
SUBMIT	Provides the capability to execute a series of ISIS-II commands which have been previously written to a diskette file.

The ATTRIB, DELETE and DIR commands have the additional capability of operating on several files at once via the wildcard file-naming convention. As an example, the command "DELETE * .OBJ" deletes all files in the diskette directory with the suffix ".OBJ".

ISIS-II SYSTEM CALL CAPABILITY

The DELETE, RENAME and ATTRIB system commands, along with a set of file I/O routines are callable from user-written programs. This allows the user to open, close, read and write diskette files, access standard peripheral devices, write error messages and load other programs via simple program call statements.

ISIS-II 8080 MACRO ASSEMBLER

The ISIS-II 8080 Macro Assembler translates symbolic 8080 assembly language instructions into relocatable and/or absolute object code modules. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits the assembler to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

In addition, the user is allowed complete freedom in assigning the location of code, data and stack segments.

The ISIS-II Assembler accepts diskette file input and produces a relocatable object file with corresponding symbol table and assembly listing file, including any error messages. The list file may then be examined from the system console or copied to a specified list device.

The relocatable object file generated by the assembler may be combined with other object programs residing on the diskette to form a single relocatable object module or it can be converted to an absolute form or for subsequent loading and execution.

ISIS-II LINKER

The ISIS-II LINKER provides the capability to combine the outputs of several independently compiled or assembled object modules (files) into a single relocatable object module. The LINKER automatically resolves all external program and data references during the linking process.

Object modules produced from previous link operations may be easily linked to a new module. ISIS-II also provides facilities to ease the generation of overlays.

An optional link map showing the contents and lengths of each segment in the output module can be requested. All unsatisfied external references are also listed.

If requested by the user the ISIS-II LINKER can search a specified set of program libraries for routines to be included in the output module.

ISIS-II OBJECT LOCATOR

The ISIS-II LOCATE program takes output from either the PL/M-80 resident compiler, the macro assembler or the LINKER and transforms that output from a relocatable format to an absolute format which may then be loaded via the standard ISIS-II loader, or loaded into ICE-80™, the 8080 In-Circuit Emulator.

During the LOCATE process, code, data and stack segments can be *separately* relocated, allowing code to be put in areas to be subsequently specified as ROM, while data and the stack can be directed to RAM addresses.

A load map showing absolute load addresses for each code and data segment and a symbol table dump listing symbols, attributes and absolute address can also be requested.

ISIS-II TEXT EDITOR

The ISIS-II Text Editor is a comprehensive tool for the entry and correction of assembly language and PL/M-80 programs for the Intel® 8080 microcomputer. Its command set allows manipulation of either entire lines of text or individual characters within a line.

Programs may be entered from the console keyboard or may be loaded directly. Text is stored internally in the editor's workspace, and may be edited with the following commands:

- string insertion or deletion
- string search
- string substitution

To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

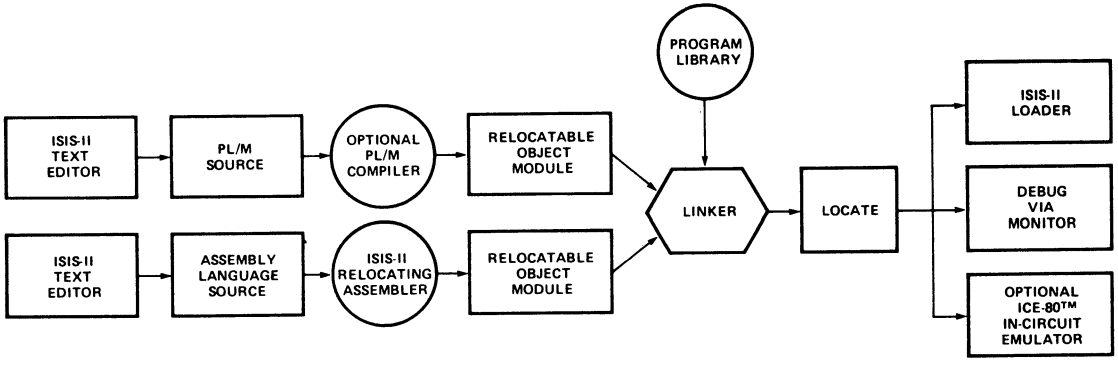
The contents of the workspace are stored on the diskette and can be immediately accessed by ISIS-II commands or other programs such as the ISIS-II 8080 Macro Assembler.

ISIS-II LIBRARY MANAGER

The ISIS-II LIBRARY MANAGER program provides for the creation and maintenance of a program library containing Intel-provided and user-written programs and subroutines. These library routines can be linked to a program using the ISIS-II LINKER. Several libraries, each containing its own set of routines, can be created.

ISIS-I A 16K ABSOLUTE SYSTEM

For owners of Intellec® systems with less than 32K of memory, the limited capability ISIS-I Diskette Operating System, is available. Included in ISIS-I is a text editor and absolute assembler. No relocation or linkage facilities exist with ISIS-I.



PROGRAM DEVELOPMENT FLOW USING ISIS-II DISK OPERATING SYSTEM

ISIS OPERATIONAL ENVIRONMENTAL

ISIS-II

Required hardware:
- Intellec® Microcomputer Development System
- 32K bytes RAM memory
- System console
- Single Floppy Disk Drive

ISIS-I

Required hardware:
- Intellec® Microcomputer Development System
- 16K Bytes RAM memory
- System Console
- Single Floppy Disk Drive

HARDWARE SPECIFICATIONS

MEDIA

Flexible Diskette
One Recording Surface
IBM Soft Sector Format
77 Tracks/Diskette
26 Sectors/Track
128 Bytes/Sector

PHYSICAL CHARACTERISTICS

(Chassis and Drives)

Mounting:	Table-Top or Standard 19" Retma Cabinet
Height:	12.08" (30.68 cm)
Width:	16.88" (42.88 cm)
Depth:	19.0" (48.26 cm)
Weight:	1 Drive 51 lb (23 kg) 2 Drives 64 lb (29 kg)

ELECTRICAL CHARACTERISTICS

Chassis
DC Power Supplies

Voltage	Current
5V	3A ±5%
-5V	600 mA ±5%
24V	4A ±5%

AC Power Requirements
3 wire input with center conductor (earth ground) tied to chassis

Single-phase, 115/230 VAC; 50—60 Hz; 160 watts

Intellec® DOS Controller
DC Power Requirements
Channel Board: 5V @ 3.75A (typ), 5A (max)
Interface Board: 5V @ 1.5A (typ), 2.5A (max)

DISKETTE DRIVE PERFORMANCE SPECIFICATION

Capacity (Unformatted):	
Per Disk	3.1 megabits
Per Track	41 kilobits
Capacity (Formatted):	
Per Disk	2.05 M Bits
Per Track	26.6 K Bits
Data Transfer Rate	250 Kilobits/sec.
Access Time:	
Track-to-Track	10 ms
Head Settling Time	10 ms
Average Random Positioning Time	260 ms
Rotational Speed	360 rpm
Average Latency	83 ms
Recording Mode	Frequency Modulation

ENVIRONMENTAL CHARACTERISTICS

MEDIA

Temperature:	
Operating:	15.6°C to 51.7°C
Non-Operating:	5°C to 55%
Humidity:	
Operating:	8 to 80% (Wet bulb 29.4°C)
Non-Operating:	8 to 90%

DRIVES AND CHASSIS

Temperature:	
Operating:	10°C to 38°C
Non-Operating:	-35°C to 65°C
Humidity:	
Operating:	20% to 80% (Wet bulb 26.7°C)
Non-Operating:	5% to 95%

CONTROLLER BOARDS

Temperature:	
Operating:	0 to 70°C
Non-Operating:	-55°C to 85°C
Humidity:	
Operating:	Up to 90% relative humidity without condensation.
Non-Operating:	All conditions without condensation of water or frost.

EQUIPMENT SUPPLIED

Cabinet, Power Supplies, Line Cord, Single Drive
FDC Channel Board
FDC Interface Board
Dual Auxiliary Board Connector
Floppy Disk Controller Cable
Floppy Disk Peripheral Cable
Hardware Reference Manual
Reference Schematics
ISIS-II System Diskette
ISIS-I System Diskette
ISIS-II System Users Guide

OPTIONAL EQUIPMENT

Rack Mount Kit
MDS-DRV Additional Drive Unit
Blank Diskettes
ISIS-II System Diskette
ISIS-I System Diskette

ORDERING INFORMATION

Part Number	Description
MDS-1DS/110V /220V	Diskette Unit with one drive, controller, and software.
MDS-2DS/110V /220V	Diskette Unit with two drives, controller, and software.
MDS-DRV/110V /220V	Additional drive unit.

PL/M-80
HIGH LEVEL PROGRAMMING LANGUAGE
INTELLEC® RESIDENT COMPILER

Cuts software development and maintenance costs

Speeds project completion

Improves product reliability

Eases enhancements as system capabilities expand

Produces relocatable and linkable object code

Resident operation on Intellec® Microcomputer Development System

Sophisticated code optimization reduces application memory requirements

PL/M-80 is an advanced high level programming language for Intel® 8080 microprocessors, SBC 80 OEM computer systems, and Intellec® Microcomputer Development Systems. PL/M has been substantially enhanced since its introduction in 1973 and has become one of the most effective and powerful microprocessor software systems implementation tools available. It is easy to learn, facilitates rapid program development and debugging, and significantly reduces maintenance costs.

PL/M is a powerful high-level algorithmic language in which program statements can naturally express the algorithm to be programmed. This frees programmers to concentrate on their system development without having to deal with assembly language details (such as register allocation, meanings of assembler mnemonics, etc.).

The PL/M compiler efficiently converts free-form PL/M programs into equivalent 8080 instructions. Substantially fewer PL/M statements are necessary for a given application than if it were programmed at the assembly language or machine code level.

Since PL/M programs are problem oriented and more compact, programming in PL/M results in a high degree of productivity during development efforts. This translates into significant reductions in software development and maintenance costs for the user.

FEATURES

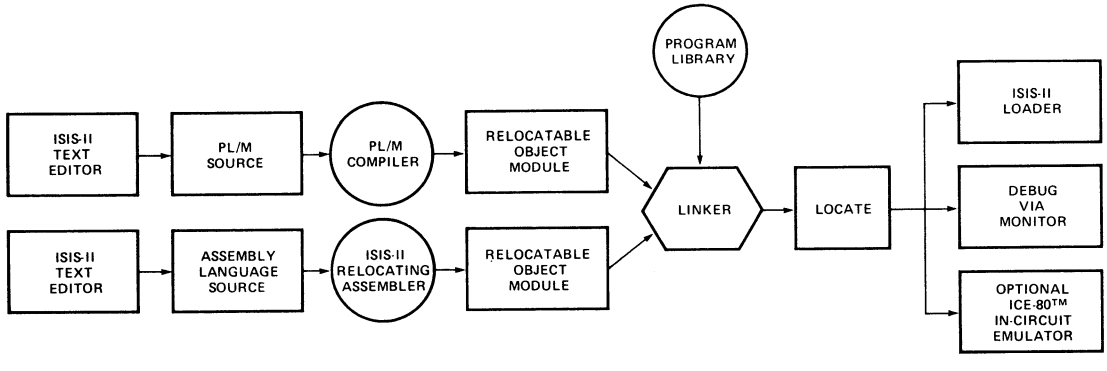
Major features of the Intel PL/M-80 Compiler and programming language include:

- Resident operation on the Intellec® Microcomputer Development System eliminates the need for a large in-house computer or costly timesharing system.
- Generation of relocatable and linkable object code permits PL/M programs to be developed and debugged in small modules. These modules can be easily linked with other modules and/or library routines to form a complete application.
- Extensive code optimization results in generation of short, efficient CPU instruction sequences. Major optimizations include compile time arithmetic, constant subscript resolution, and common subexpression elimination.
- The PL/M-80 Compiler fully supports symbolic debugging with the ICE-80™ In-Circuit Emulator.
- Compile time options include general listing format commands, symbol table listing, cross reference listing, and "innerlist" of generated assembly language instructions.
- Block structure aids in utilization of structured programming techniques.
- High Level PL/M statements provide access to hardware resources (interrupt systems, absolute addresses, CPU input/output ports).
- Complex data structures may be defined at a high level.
- Re-entrant procedures may be specified as a user option.

BENEFITS

PL/M is designed to be an efficient cost-effective solution to the special requirements of microcomputer software development as illustrated by the following benefits of PL/M use:

- **Low learning effort** — PL/M is very easy to learn for even the novice programmer.
- **Earlier project completion** — Critical projects are completed much earlier than otherwise possible because PL/M substantially increases programmer productivity.
- **Lower development cost** — Increases in programmer productivity translate into lower software development costs because less programming resources are required for a given function.
- **Increased Reliability** — PL/M is designed to assist in the development of reliable software (PL/M programs are simple statements of the program algorithm). This substantially reduces the risk of costly correction of errors in systems that have already reached full production status because a simply stated program is more likely to correctly perform its intended function.
- **Easier Enhancements and Maintenance** — Programs written in PL/M are easier to read and easier to understand. This means it is easier to enhance and maintain PL/M programs as system capabilities expand and future products are developed.
- **Simpler Project Development** — The Intellec® Microcomputer Development system, with resident PL/M-80, is all that is needed for development and debugging of software for 8080 microcomputers. This reduces development time and cost because expensive (and remote) timesharing or large computers are not required.



The PL/M compiler is an efficient multiphase compiler that accepts source programs, translates them into object code, and produces requested listings. After compilation, the object program may be linked to other modules, located to a specific area of memory, then executed. The diagram shown above illustrates a program development cycle where the program consists of two modules, one PL/M and the other assembly language.

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

MCS-48™ DISKETTE-BASED SOFTWARE SUPPORT PACKAGE

Extends Intellec® Microcomputer Development System to Support MCS-48™ Development

Takes Advantage of Powerful ISIS-II File Handling and Storage Capabilities

MCS-48 Assembler Provides Conditional Assembly and Macro Capability

Universal PROM Mapper, in Conjunction with the Universal PROM Programmer, Allows for Easy Programming and Verification of 8748 PROMs

The MCS-48™ Diskette-Based Software Support Package (MDS-D48) comes on an Intel® ISIS-II System Diskette and contains the MCS-48 Assembler (ASM48), and the diskette version of the Universal PROM Mapper.(ICE-48™ software will be included with MDS-D48 when ICE-48 modules are available for shipment. All MDS-D48 owners will receive updated diskettes containing ICE-48 software at that time.)

The MCS-48 Assembler (ASM48) translates symbolic 8048 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs when adding or deleting instructions. Conditional assembly permits the programmer to specify portions of the master source document which should be included or deleted in variations on a basic system design, such as the code required to handle optional external devices.

Macro capability allows the programmer to define a routine through the use of a single label. ASM48 will assemble the code required by the reserved routine whenever the Macro label is inserted in the text.

Output from the ASM48 is in standard Intel® Hex format. It may be loaded directly to an ICE-48 module for integrated hardware/software debugging. It may also be loaded into the Intellec Development System for 8748 PROM programming using the Universal PROM Programmer.

The Universal PROM Mapper (UPM) software available on the MDS-D48 Diskette allows the user to program and verify all Intel PROMs, including the PROM in the 8748 and the 8755, while taking full advantage of the Intellec Diskette Operating System's powerful file handling and mass storage capabilities.

DEVELOPMENT SYSTEMS

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

SAMPLE MCS-48™ DISKETTE-BASED ASSEMBLEY LISTING

```
ISIS-II 8048 MACRO ASSEMBLER, V1.0                    PAGE 1

LOC    OBJ          SEQ          SOURCE STATEMENT

                     1  ;DECIMAL ADDITION ROUTINE.  ADD BCD NUMBER
                     2  ;AT LOCATION 'BETA' TO BCD NUMBER AT 'ALPHA' WITH
                     3  ;RESULT IN 'ALPHA.'  LENGTH OF NUMBER IS 'COUNT' DIGIT
                     4  ;PAIRS. (ASSUME BOTH BETA AND ALPHA ARE SAME LENGTH
                     5  ;AND HAVE EVEN NUMBER OF DIGITS OR MSD IS 0 IF
                     6  ;ODD)
                     7  INIT       MACRO     AUGND,ADDND,CNT
                     8             MOV       R0, #AUGND
                     9  L1:        MOV       R1, #ADDND
                    10             MOV       R2, #CNT
                    11             ENDM
                    12  ;
0001E                13  ALPHA      EQU       30
0028                 14  BETA       EQU       40
0032                 15  COUNT      EQU       5
0100                 16             ORG       100H
                     17             INIT      ALPHA, BETA, COUNT
0100   B81E          18+            MOV       R0, #ALPHA
0102   B928          19+L1:         MOV       R1, #BETA
0104   BA32          20+            MOV       R2, #COUNT
0106   97            21             CLR       C
0107   F0            22  LP:        MOV       A, @R0
0108   71            23             ADDC      A, @R1
0109   57            24             DA        A
010A   A1            25             MOV       @R0, A
010B   18            26             INC       R0
010C   19            27             INC       R1
010D   EA07          28             DJNZ      R2, LP
                                    END

USER SYMBOLS
ALPHA 001E    BETA 0028    COUNT 0005    LP 0107
L1    0102

ASSEMBLY COMPLETE, NO ERRORS


ISIS-II ASSEMBLER SYMBOL CROSS REFERENCE, V1.0        PAGE 1

SYMBOL CROSS REFERENCE

ALPHA    13#   17
BETA     14#   17
COUNT    15#   17
INIT      7#   17
L1       19#
LP       22#   28
```

SPECIFICATIONS

MDS-D48

Operating Environment:

Required Hardware
- Intellec® Microcomputer Development System
- System Console
- Intellec Diskette Operating System

Optional Hardware
- Universal PROM Programmer

Documentation Package:
- MCS-48™ Assembly Language Manual
- Universal PROM Mapper Operator's Manual
- ISIS-II System User's Guide

Shipping Media:
- Diskette

DEVELOPMENT SYSTEMS

ORDERING INFORMATION

Part No.	Description
MDS-D48	MCS-48 ISIS-II Based Support Package including ASM48 and Universal PROM Mapper Software

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

MCS-48™
PAPER TAPE BASED ASSEMBLER

Executes on Intellec® Microcomputer Development System

Provides Complete Symbolic Assembly Capability

Conditional Assembly Capability

Powerful Assembler Command Set Gives User Added Flexibility During Assembly

The MCS-48™ Paper Tape-Based Assembler provides symbolic assembly capability for the entire MCS-48 family on the Intellec Development System.

It translates symbolic MCS-48 language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs when adding or deleting instructions. Conditional assembly permits the programmer to specify portions of the master source document which could be included or deleted in variations on a basic system design, such as the code required to handle optional peripheral devices.

Output from the MCS-48 Paper Tape-Based Assembler is in standard Intel® Hex format. It may be loaded directly to an ICE-48™ module for integrated hardware/software debugging. It may also be loaded into the Intellec Development System for 8748 PROM programming using the Universal PROM Programmer and Universal PROM Mapper software.

DEVELOPMENT SYSTEMS

SAMPLE MCS-48™ PAPER TAPE BASED ASSEMBLY LISTING

```
INTELLEC MONITOR 8048 ASSEMBLER, V1.0                    PAGE 1

LOC  OBJ       SEQ        SOURCE STATEMENT

                 0        ;ADD THE BCD NUMBER WHOSE LSD IS AT LOCATION
                 1        ;ALPHA AND STORE RESULT IN ALPHA.  LENGTH OF NUMBER
                 2        ;IS 'COUNT' DIGIT PAIRS.  (ASSUME
                 3        ;BOTH NUMBERS ARE THE SAME LENGTH AND HAVE AN EVEN
                 4        ;NUMBER OF DIGITS, OR THE MOST-SIGNIFICANT DIGIT
                 5        ;IS ZERO, IF ODD).
0000             6        ORG 0
0032             7 ALPHA  EQU 50
0036             8 BETA   EQU 54
0001             9 COUNT  EQU 1
0000 B832       10 ADDBCD: MOV R0, #ALPHA     ;AUGEND, SUM LSD LOCATION IN REG 0
0002 B936       11         MOV R1, #BETA      ;ADDEND LOCATION IN REG 1
0004 BA01       12         MOV R2, #COUNT     ;LOOP COUNTER IN REG 2
0006 97         13         CLR C
0007 F0         14 LOOP:   MOV A, @R0         ;ADD ROUTINE
0008 71         15         ADDC A, @R1
0009 57         16         DA A
000A A0         17         MOV @R0,A          ;STORE SUM
000B 18         18         INC R0             ;DECREMENT ADDRESS REGS
000C 19         19         INC R1
000D EA07       20         DJNZ R2, LOOP      : LOOP CONTROL
                           END

USER SYMBOLS
ADDBCD 0000   ALPHA 0032   BETA 0036   COUNT 0001   LOOP 0017
```

SPECIFICATIONS

MDS-P48

Operating Environment:

Required Hardware
- Intellec® Microcomputer Development System
- System Console
- Reader Device
- Punch Device

Required Software
- System Monitor

Documentation Package:

- MCS-48™ Assembly Language Manual

Shipping Media:

- Paper Tape

DEVELOPMENT SYSTEMS

ORDERING INFORMATION

Part No.	Description
MDS-P48	MCS-48 Paper Tape Assembler for the Intellec® Microcomputer Development System

INTELLEC® SYSTEM CRT KEYBOARD DISPLAY

- Teleprinter compatible CRT terminal with detachable keyboard
- Asynchronous data transfer rates switch selectable up to 9600 baud
- RS232C compatible
- 2000-character capacity in 25 lines of 80 characters each
- Cursor positioning (left, right, up or down) and cursor homing capability
- Each CRT is complete with cable, power supply, and is system tested with the Intellec system

The Intellec System CRT Keyboard Display Unit is fully compatible with the Intellec Microcomputer Development System, Diskette Operating System and the entire range of the Intellec System In-Circuit Emulator design aids.

INTELLEC SYSTEM KEYBOARD DISPLAY
SYSTEM CRT

SPECIFICATIONS

DISPLAY FORMAT
25 lines X 80 characters

DISPLAY SIZE
Approximately 6.5" high X 8.4" wide

CRT SIZE
12" measured diagonally

CHARACTER SIZE
Approximately 0.2" high X 0.1" wide

CHARACTER TYPE
5 X 7 dot matrix – 2 dot spacing between characters, white on black

CHARACTER SET
64-character ASCII

CHARACTER GENERATION
MOS ROM

REFRESH RATE
60 Hz, 50 Hz optional

REFRESH MEMORY
MOS shift register

CURSOR CONTROL
Left, Right, Up, Down, Home, Carriage Return, Line Feed

COMMUNICATIONS INTERFACE
Serial R5232C

TRANSMISSION RATE
Switchable to 9600 baud; Monitor program supports 300, 1200 and 2400 baud

COMMUNICATION MODE
Full duplex, half duplex, 10 or 11-bit word asynchronously only

PARITY
Odd, even mark, space – Transmit and receive check or no check on received data

CHARACTER MODE
Character by character transmission

ERASE MODE
Erase to end of line, erase to end of memory, clear

BELL
Audible alarm when control G is received or 70th character of line

KEYBOARD
Standard TTY keyboard, custom designed, detachable module, color coordinated by Intel

INPUT VOLTAGE
115 VAC ±10% 60 Hz
115 VAC ±10% 50 Hz (optional)
230 VAC ±10% 50 Hz (optional)

OPERATING TEMPERATURE
5°C to 40°C after warm-up

TERMINAL SIZE
Monitor 16.5" W X 14" H X 15" D
Weight approximately 45 lb
Keyboard 16.5" W X 3.5" H X 9.7" D
Weight approximately 7 lb

TERMINAL FINISH
Textured vinyl

OPERATOR CONTROLS
Keyboard – Brightness, On-Line/Local
Rear Panel – Power, Full duplex/Half duplex
I/O baud rate, contrast

ORDERING INFORMATION

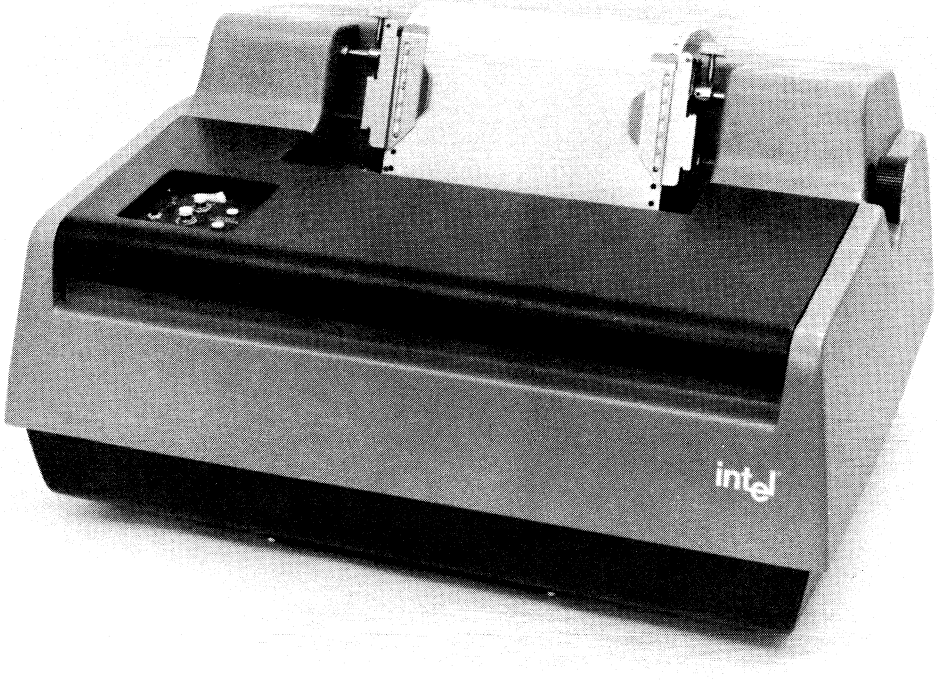
Part Number	Description
MDS-CRT	Keyboard Display Unit

INTELLEC® PRINTER

- **Provides listing of hard-copy output at 55 lines per minute**
- **Switch-selectable to 80 or 132 characters per 8½" line**
- **Employs 5×7 dot matrix with standard 2-channel, vertical control format**
- **Prints up to 4 copies on standard 8½" fanfold paper**
- **Automatic on-off motor switch for quiet operation**
- **Optional finished metal stand and paper take-up tray available**

The Intellec® Printer provides hard copy listings at 10 to 16 times the speed of a teleprinter. Automatic on-off motor control allows the user to maintain a low noise environment and yet send information to the printer from the Intellec system console without additional manipulation of line printer switches. The user can select a column width of 80 characters per line (10 characters per inch) or 132 characters per line (16.5 characters per inch) either manually or under program control. Top of page spacing capability is available under user programmable format control.

The printer uses standard 8½" fanfold paper and can produce up to 4 carbon copies along with the original. Paper can be fed from the bottom or rear of the printer for versatility in any lab environment.



DEVELOPMENT SYSTEMS

SPECIFICATIONS

PRINTING METHOD
Impact, character-by-character printing, one line character buffer

PRINTING RATE
Characters – 100 or 165 characters per second
Full Lines – 55 lines per minute (80 or 132-character line)

TRANSMISSION RATE – PARALLEL
Up to 75,000 characters per second

DATA INPUT
Parallel

CHARACTER STRUCTURE
5 X 7 dot matrix, 10-point type equivalent

CODE
USASCII – 64 characters printed

SWITCH CONTROLS
ON/OFF, SELECT, FORMS OVERRIDE, NORMAL/CONDENSED TOP OF FORM

INDICATORS
PAPER OUT, SELECT

MANUAL CONTROLS
Form Thickness, Paper Advance Knob

BUFFER
One Line Character Buffer

FORMAT
80 or 132 characters maximum per line, 6 lines per inch

PAPER FEED
Sprocket fed, 4 I.P.S. slew, adjustable to 9½" width

PAPER
Standard sprocketed paper

NUMBER OF COPIES
Original and up to four carbon copies

DIMENSIONS
12¾" high, 18¾" deep, 23¼" wide

WEIGHT
66 pounds

ELECTRICAL REQUIREMENTS
115 VAC ±10%, 60 Hz (or 230 VAC ±10%, 50 Hz as option)

TEMPERATURE
Operating – 40° to 100°F
Storage – -40° to 160°F

HUMIDITY
Operating – 5% to 90% (no condensation)
Storage – 0% to 95% (no condensation)

OPTIONS
MDS-STD finished metal stand and paper tray

WARRANTY
The MDS-PRN is warrantied against defects in materials and workmanship for a period of one (1) year on mechanical parts, 90 days on electrical parts, and 45 days on labor.

ORDERING INFORMATION

Part Number	Description
MDS-PRN	Printer Unit
MDS-STD	Stand and Paper Tray

DEVELOPMENT SYSTEMS

INTELLEC® HIGH SPEED PAPER TAPE READER

Loads 16K Intellec® program memory in less than 3 minutes.

20 times faster than standard ASR-33 Teletype reader.

Data transfer at asynchronous rates in excess of 2000 characters per second

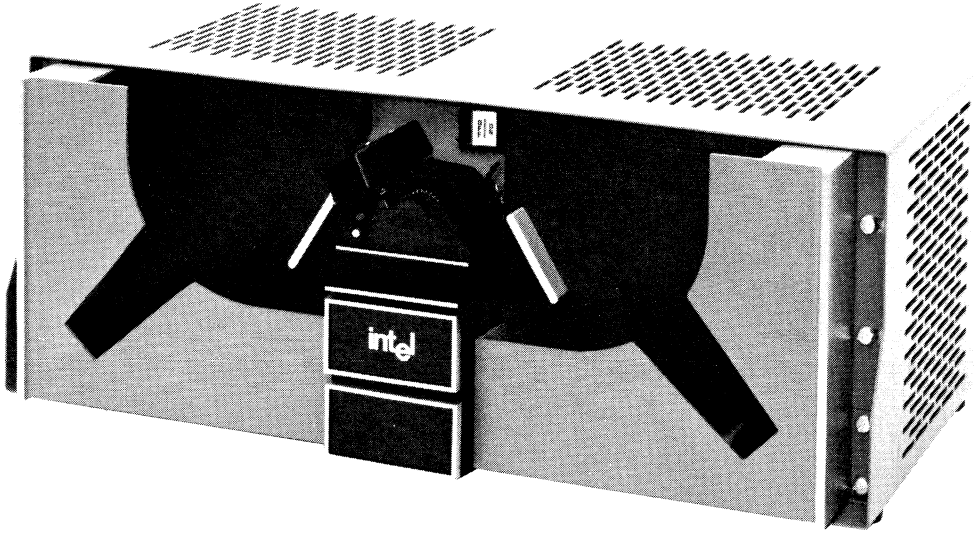
Rack-mountable or stand-alone

The Intellec® High-Speed Paper Tape Reader is an Intellec peripheral that reads paper tape over twenty times faster than the standard ASR-33 Teletype reader. This translates into a significantly faster development cycle due to a marked reduction in the time required for repetitive program loading, assembly, and editing operations.

The monitor software provides two key capabilities which significantly enhance the system's performance of the high-speed reader. A general-purpose paper tape reader driver is included in the Intellec Monitor which enables all system software or user-written application programs to utilize the high-speed reader features. The monitor also provides dynamic I/O reconfiguration, permitting reassignment of the high-speed reader to other logical input devices.

Reader data and command interface hardware is provided with the basic Intellec. A reader/Intellec system interface cable is included with the unit. A fanfold tape guide is also included to provide fanfold punch capability to the ASR-33 Teletype.

The high-speed reader may be used as a table-top unit or mounted in a standard 19" RETMA cabinet.



SPECIFICATIONS

TAPE MOVEMENT

Tape Reader Speed:
0 to 200 characters per second asynchronous
Tape Stopping:
Stops "On Character"

TAPE CHARACTERISTICS

Tape must be prepared to ANSI X 3.18 or EMCA 10 Standards for base materials and perforations.

Reads tape of any material with thickness between 0.0027" and 0.0045" with transmissivity less than or equal to 57% (oiled buff paper tape).

Tape loading: in line

Tape width: 1 inch

PHYSICAL CHARACTERISTICS

Height: 7.75 in. (19.69 cm)
Width: 19.25 in. (48.90 cm)
Depth: 11.62 in. (29.52 cm)
Weight: 13 lb (5.9 kg)

ELECTRICAL CHARACTERISTICS

AC Power Requirements:
3-wire input with center conductor (earth ground) tied to chassis. 100, 115, or 127 VAC, single phase at 3.0 amps or 220 or 240 VAC and 1.5 amps; 47 to 63 Hz.

ENVIRONMENTAL CHARACTERISTICS

Temperature:
Operating: 0 to 55°C (free air)
Non-operating: −55°C to +85°C

Humidity:
Operating: Up to 90% relative humidity without condensation.
Storage: All conditions without condensation of water or frost.

EQUIPMENT SUPPLIED

Paper Tape Reader
Reader Cable
Fanfold Tape Guide
Fanfold Paper Tape
Hardware Manual
Installation and Operations Guide
Fanfold Guide Installation Instructions

ORDERING INFORMATION

Part Number	Description
MDS-PTR	Paper Tape Reader

UPP-101, UPP-102
UNIVERSAL PROM PROGRAMMER

- Intellec® Development System Peripheral for PROM programming and verification
- Personality cards available for programming all Intel® PROM families
- Zero insertion force sockets for both 16-pin and 24-pin PROMs
- Universal PROM Mapper software provides powerful data manipulation and programming commands
- Flexible power source for system logic and programming pulse generation
- Holds 2 personality cards to facilitate programming operations using several PROM types

The Universal PROM Programmer (UPP) is an Intellec® System peripheral capable of programming and verifying the following Intel Programmable ROMs (PROMs): 1702A, 2704, 2708, 2716, 3601, 3602, 3604, 3621, 3622, 3624, 8072A, 8704, 8708. In addition, the UPP programs the PROM memory portions of the 8748 Microcomputer and the 8755 PROM and I/O chip. Programming and verification operations are initiated from the Intellec Development System console and are controlled by the Universal PROM Mapper (UPM) program.

DEVELOPMENT SYSTEMS

FUNCTIONAL DESCRIPTION

The basic UPP consists of a controller module, two personality card sockets, front panel, power supplies, chassis and an Intellec Development System interconnection cable. An Intel 4040-based intelligent controller monitors the commands from the Intellec System and controls the data transfer interface between the selected PROM personality card and the Intellec memory. A unique personality card contains the appropriate pulse generation functions for each Intel PROM family. Programming and verifying any Intel PROM may be accomplished by selecting and plugging in the appropriate personality card. The front panel contains a power-on switch and indicator, reset switch, and two zero-force insertion sockets (one 16-pin and one 24-pin or two 24-pin). A central power supply provides power for system logic and for PROM programming pulse generation.

The Universal PROM Programmer may be used as a table top unit or mounted in a standard 19" RETMA cabinet.

The Universal PROM Mapper (UPM) is the software program which controls transfers of data between paper tape or diskette files and a PROM plugged into the Universal PROM Programmer. It uses Intellec System memory for intermediate storage. The UPM transfers data in 8-bit HEX, BNPF, or binary object format between paper tape or diskette files and the Intellec System memory. While the data is in Intellec System memory, it can be displayed and changed. In addition, word length, bit position, and data sense can be adjusted as required for the PROM to be programmed. PROMs can also be duplicated or altered by copying the PROM contents into the Intellec System memory. Easy-to-use PROGRAM and COMPARE commands give the user complete control over programming and verification operations. The UPM eliminates the need for a variety of personalized PROM programming routines because it contains the programming algorithms for all Intel PROM families.

There are two versions of the UPM: one that runs under Intellec System Monitor (paper tape system), and one that runs under ISIS-II, the Intellec Diskette Operating System (diskette-based system). The paper tape version is included with the Universal PROM Programmer. The diskette-based version of the UPM is available on all ISIS-II system diskettes.

HARDWARE INTERFACE

Data: Two 8-bit unidirectional buses
Commands: 3 Write Commands
2 Read Commands
Initiate Command

PHYSICAL CHARACTERISTICS

Dimensions: 6" x 7" x 17"
14.7 cm x 17.2 cm x 41.7 cm
Weight: 18 lb (8.2 kg)

ELECTRICAL CHARACTERISTICS

AC Power Requirements: 50-60 Hz; 115/230 VAC: 80 Watts

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0°C to 55°C

EQUIPMENT SUPPLIED

Cabinet
Power Supplies
4040 Intelligent Controller Module
Specified Zero Insertion Force Socket Pair
Intellec® Development System Interface Cable
Hardware Reference Manual
Reference Schematics
Universal PROM Mapper Operator's Manual
Universal PROM Mapper program (paper tape version — disk-based version available on ISIS-II diskettes)

ORDERING INFORMATION

Universal PROM Programmer:
UPP-101: with 16-pin/24-pin socket pair
UPP-102: with 24-pin/24-pin socket pair

OPTIONS

Personality Cards:
UPP-361: 3601 Personality Card
UPP-816: 2716 Personality Card
UPP-848: 8748 Personality Card with 40-pin adaptor socket
UPP-855: 8755 Personality Card with 40-pin adaptor socket
UPP-864: 3604/3624 Personality Card
UPP-872: 8702A/1702A Personality Card
UPP-878: 8708/8704/2708/2704 Personality Card

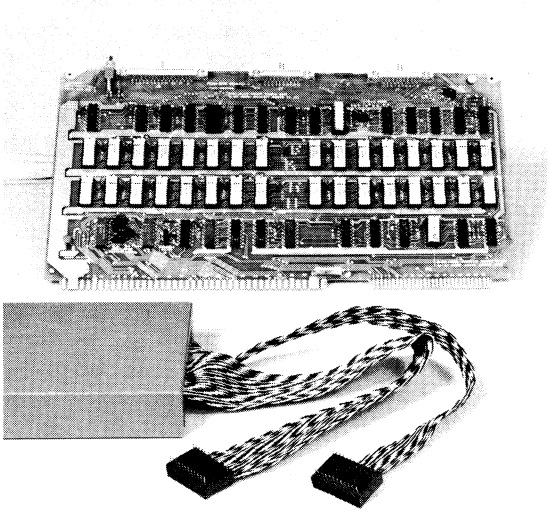
Adaptor Sockets:
UPP-362: 3602/3621/3622 adapter, for use with UPP-864 Personality Card

PROM Programming Sockets:
UPP-501: 16-pin/24-pin socket pair
UPP-502: 24-pin/24-pin socket pair

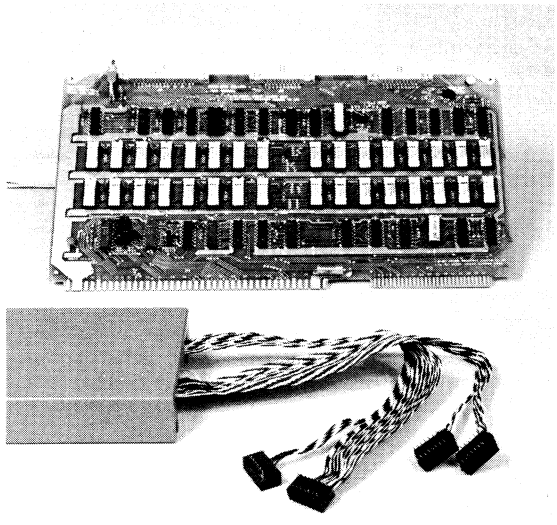
SIM-101, SIM-102, SIM-104
ROM SIMULATOR

- Extends the powerful Intellec diagnostic capabilities into user-configured systems, allowing simulation of the user system's bipolar ROM/PROM memory
- Direct Intellec connection to the user-configured system via external cables and Intel's ROM/PROM compatible dual-in-line connectors
- Simulates Intel's standard bipolar ROMs and PROMs
- Modular design allows the user to configure simulation modules to particular memory space requirements
- Directly load the ROM Simulator modules from the output of the Intel Cross Microassembler, CROMIS
- Access the configured memory space from the console keyboard using simulated ROM addresses
- Examine an entire word regardless of length; i.e., 8 bits, 10 bits, 32 bits etc.
- Modify an entire word in a single operation regardless of length
- Read access time is 130 ns, maximum

Each ROM-SIM module consists of a high-speed, 130-nanosecond 8K bit RAM board, buffer assembly, external cables, and an interactive software program. The ROM-SIM software is a PL/M-80 program that operates in the Intellec system to provide the user interface for the ROM-SIM hardware. The software loads BNPF or hexadecimal files such as those generated by the Cross Microassembler System, CROMIS. The ROM-SIM software has the capability to compare and verify microcode, load, display and modify simulated control store contents, and output new BNPF or hexadecimal files from the simulated ROM memory for ROM/PROM programming.



SIM-101, 102



SIM-104

ROM SIMULATOR HARDWARE

The ROM Simulator Module consists of a memory board mounted in the Intellec system chassis, and an external Buffer Assembly connected to the Memory board by two flat cables for transferring address and data separately. The chip interconnect cables are 10-inch, twisted-pair cables with either two or four connectors, depending on the user's system configuration. These dual-in-line plugs connect directly to ROM chip sockets in the user's system.

The ROM-SIM modules can be configured to fit the user system's memory space. The simulated chips (or their equivalents) are listed below:

PRODUCT	INTEL® SIMULATED CHIP
SIM-101	3601/3301A
SIM-102	3602/3622/3302
SIM-104	3604/3624/3304A/3324A/8604

Simulation of data output drivers can be converted from three-state to open collectors, or open collector to three-state, by replacing the driver IC's inside the Buffer Assembly.

Data from the Intellec System is written into the random-access memory of the ROM Simulator under software control. A user system can read data from ROM Simulator memory by inputting memory addresses, just as if the ROM Simulator was an array of ROM chips in the user system. At any point, the entire memory contents can be displayed and/or modified by the operator, regardless of physical ROM chip boundaries.

One ROM Simulator module simulates a block of memory, either 512 X 16 bits or 1024 X 8 bits. Therefore, each ROM Simulator module can simulate the equivalent capacity of two Intel 3604/3624/3304A/3324A/8604 chips (512 X 8 organization), four Intel 3602/3622/3302 chips (512 X 4 organization), or eight Intel 3601/3301A chips (256 X 4 organization). If additional capacity is needed, additional Simulator modules can be added as required.

The Intellec System can accommodate a maximum of four Simulator modules (the limie of the system power supply) to allow configurations such as 512 words X 64 bits, 1024 words X 32 bits, 2048 words X 16 bits, and 4096 words X 8 bits.

Because of the ROM Simulator's flexibility and its interaction with the Intellec system software, a wide variety of memory configurations can be simulated and software/firmware programs can be readily debugged. When the user is satisfied that the memory configuration and programs are adequate for use in the prototype system, the ROM Simulator, working in conjunction with a paper tape I/O device, creates paper tapes for ROM or PROM programming.

The ROM Simulator uses a buffer module between the user's system and the Simulator to minimize the capacitive loading seen by the user's address drivers. Address signals are brought into the buffer by a cable from one chip; as an option, address signals are propagated to the Simulator memory boards within the Intellec chassis. As a result, effective Simulator access time is significantly improved and the capacitive loading on the user's ROM Simulator closely resembles the actual user ROMs or PROMs.

The interchange among the ROM Simulator products, SIM-104, SIM-102, and SIM-101, is accomplished by replacing the 10-inch chip interface cables.

ROM SIMULATOR SOFTWARE

The ROM Simulator Software provides the user with complete control of the structure and contents of the object code file which resides in the simulated hardware. Microcode such as that generated by Intel's Cross Microassembler System, CROMIS, is handled with the following comprehensive repetoire of System Commands:

- The LOAD command allows BNPF or hexadecimal paper tapes to be loaded into specified areas of the ROM Simulation Hardware.
- The VERIFY command compares data on paper tape with that loaded in memory and identifies any inconsistencies.
- The PUNCH command punches the contents of specified memory modules to paper tape in hexadecimal or BNPF format.
- The INVERT command complements a specified area of simulated memory to compensate for cases of mode incompatibility on input tapes.
- The DISPLAY MEMORY command prints the contents of the specified simulated memory to the terminal.
- The CHANGE MEMORY command allows for user modification of selected memory locations to aid in interactive debugging of user code.
- The BASE and CODE commands allow the user to change the default values for the base of numbers printed and the format of tapes loaded and punched.
- The GROUP command allows for insertion of a special delimeter in memory content displays for improved readability.
- The OFFSET command is used to bias the DISPLAY and CHANGE commands when segments of memory are debugged separately.
- The RESTART and EXIT commands are used to reinitialize a simulation sequence and to return control to the system Monitor upon completion of a simulation.

ROM-SIM software will reside with the monitor in the basic 16K Intellec System. An additional Intellec product designed to assist in the development efforts of users of the Intel 3000 Series elements is ICE-30. This package provides for In-Circuit Emulation of the 3001 Microprogram Control Unit. Users ordering ICE-30 will obtain the ROM-SIM software capabilities as a subset of that package.

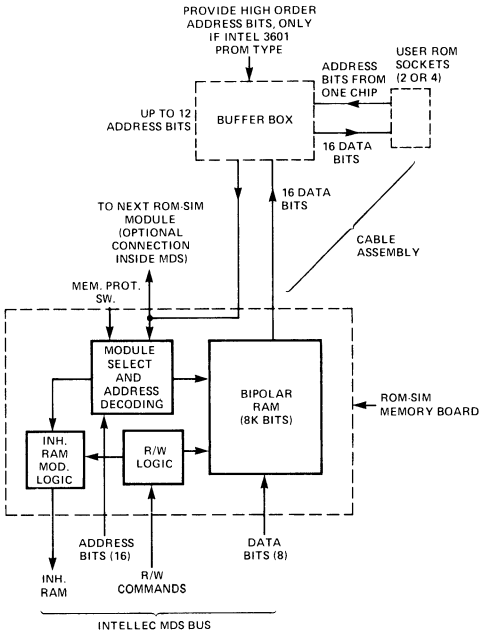


Fig. 1. Data Flow of ROM-SIM Module

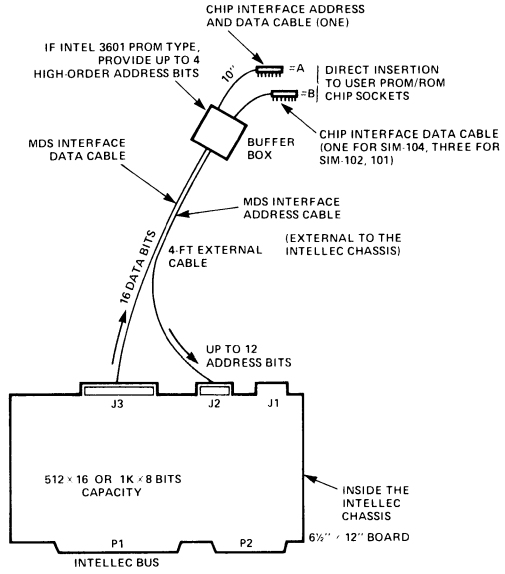


Fig. 2. Cable Connection of ROM-SIM Module

SPECIFICATIONS

DC CHARACTERISTICS

T_A = 0°C to 55°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	LIMITS			TEST CONDITION
		MIN	MAX	UNIT	
I_I	Input Load Current Low Order Addr A0-A8 High Order Addr A9-AB Chip Selects		 -1.6 -2.1 -0.75	 mA	V_{CC} = 5.25V V_{IN} = 0.45V
V_{OL}	Output Low Voltage		0.45	V	V_{CC} = 4.75V, I_{OL} = 16 mA
I_{CC}	User Power Supply Sensing		6	mA	User V_{CC} = 5.25V
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0		V	V_{CC} = 5.0V
V_{OH}	Output High Voltage		2.4	V	V_{CC} = 4.75V
I_{SC}	Output Short Circuit Current at Single Output	-40	-100	mA	V_O = 0V, V_{CC} = 5V
I_{CEX}	Output Leakage Current		±50 250	µA µA	For High Impedance State For Open Collector V_{CC} = 5.25V

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... 0°C to 55°C
Storage Temperature ..... -20°C to 75°C
All Outputs or Supply ..... -0.5V to 7.0V
All Inputs ..... -1.0V to 5.5V

CAPACITANCE LOAD

C_{IN}	Low Order Address, Chip Selects High Order Address (Coaxial)	45 pF max. 50 pF max.
C_{OUT}	Data Outputs	50 pF max.

DEVELOPMENT SYSTEMS

AC CHARACTERISTICS

T_A = 0°C to 55°C, V_{CC} = 5.0 ±5%

SYMBOL	PARAMETER	LIMITS (ns)		
		MIN	TYP	MAX
t_{A-}, t_{A+}	Address to Data Output Delay		90	130
t_{S-}, t_{S+}	Chip Select to Data Output Delay			42

CONDITIONS OF TEST:

Address Input Rise and Fall Times: 10 ns between 0.8V and 2.0V

Measurements made at 1.5-volt level.

INTELLEC® PROMPT 48™
MCS-48™ MICROCOMPUTER DESIGN AID

Complete Design Aid and EPROM Programmer for revolutionary MCS-48™ Single Component Computers including:

CPUs	8-bit MCS-48™: 8748, 8035
Program Memory	1K byte erasable, reprogrammable on-chip (8748), expandable. 1K byte RAM in PROMPT™ system.
Register Memory	64 bytes RAM on-chip, expandable
Data Memory	256 bytes RAM in PROMPT™ system, expandable
I/O	27 TTL compatible I/O lines on-chip, expandable
Control	On-chip clock, internal timer/event counter, two vectored interrupts, eight level stack
Power	Single +5 VDC system

Low Cost

Simplifies microcomputing — enter, run, debug, and save machine language programs with calculator-like ease

Complete with two removable MCS-48™ CPUs:

8748	CPU with erasable, reprogrammable program memory on-chip
8035	CPU program memory is off-chip

Integral keyboard and displays (no teletype-writer or CRT terminal required)

Extensive PROMPT 48™ monitor allows system I/O, bus and memory expansion

Intellec® Microcomputer Development System compatible

Comprehensive Design Library

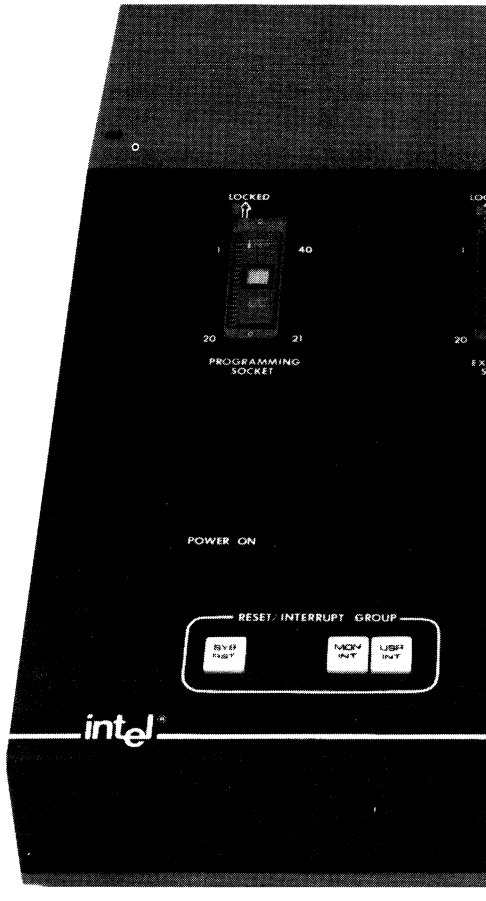
Intellec PROMPT 48 is a low cost, fully-assembled design aid for the revolutionary 8748 single component microcomputer. PROMPT 48 simplifies the programming of MCS-48 systems — programs can be entered and debugged with calculator-like ease on the large, informative display and keyboard panel. The comprehensive design library with tutorial manual is ideal for newcomers to microcomputing.

PROMPT 48's panel connector allows easy access to I/O ports and system bus. Thus users can expand program memory beyond the 1k bytes provided internally. PROMPT 48 can serve as an economical 8748 Specialized PROM Programmer (SPP) peripheral in Intellec Microcomputer Development Systems.

DEVELOPMENT SYSTEMS

The 8748 is the first microcomputer fully integrated on one component. All elements of a computing system are provided, including CPU, RAM, I/O, timer, interrupts and erasable, reprogrammable non-volatile program memory.

PROMPT's **PROGRAMMING SOCKET** programs this revolutionary "smart PROM" – the 8748 – in a highly reliable, convenient manner. A fail-safe interlock ensures the device is properly inserted before applying programming pulses. Each location may be individually programmed, one byte at a time. A read-before-write programming algorithm prevents device damage by inadvertently programming unerased memory.



The **EXECUTION SOCKET** accepts an 8035 or an 8748. Both are supplied with each PROMPT 48, and either can serve as heart of the PROMPT system. There are no processors within the PROMPT 48 mainframe, which instead contains monitor ROM and RAM, user RAM, peripherals, drivers, and sophisticated control circuitry.

Once a processor is seated in the execution socket and power is applied the PROMPT system comes to life. One can select various access modes such as program execution from PROMPT system RAM, or from on-chip PROM. Thus programs can first be executed from PROMPT RAM with the 8035 processor. When debugging is complete, the 8035 (execution socket) processor can program the 8748 (programming socket) processor. Finally, a programmed 8748 processor can be exercised by itself from the execution socket. The execution socket processor runs either monitor or user programs.

SYSTEM RESET initializes the PROMPT system and enters the monitor. **MONITOR INTERRUPT** exits a user program gracefully, preserving system status and entering the monitor. **USER INTERRUPT** causes an interrupt only if the PROMPT system is running a user program.

A comprehensive system monitor resides in four 1K byte read-only memories. It drives the PROMPT keyboard and displays and responds to COMMANDS and FUNCTIONS.

The top 16 bytes of on-chip program memory must be used by the PROMPT system to switch between monitor and user programs. It requires one level of the MCS-48 eight-level stack.

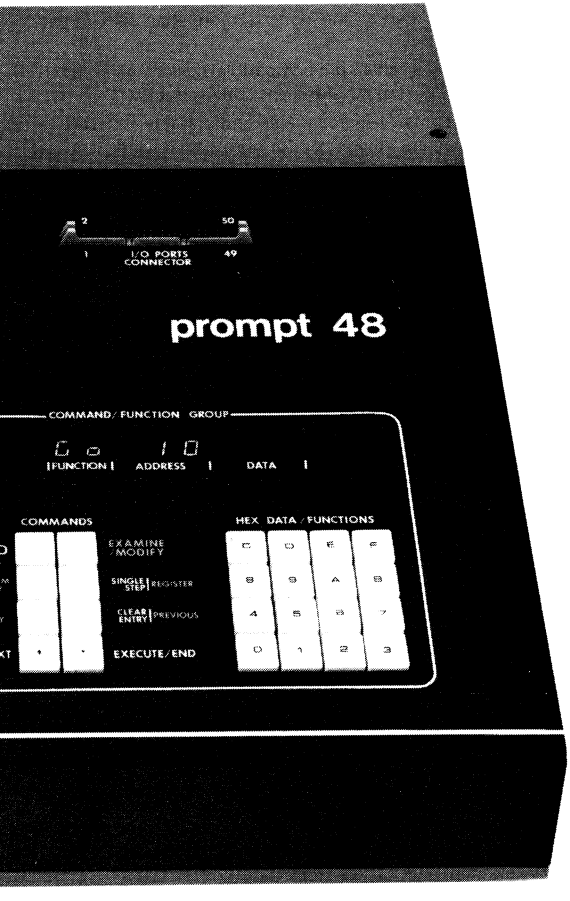
PROMPT 48's **COMMANDS** are grouped and color-coded to simplify access to the 8748's separate program and data memory. You can EXAMINE and MODIFY registers, data memory or program memory.

Then either the NEXT or PREVIOUS register and memory locations can be accessed with one keystroke.

Programs can be exercised in three modes. GO NO BREAK runs in real time. GO WITH BREAK is not real time – after each instruction the MCS-48 program counter is compared against pending breakpoints. If no break is encountered, execution resumes. GO SINGLE STEP exercises one instruction at a time.

Commands are like sentences, with parameters separated by [,] NEXT. Each command ends with [.] EXECUTE/END.

In addition to the PROMPT basic COMMANDs, thirteen functions simplify programming. Each is started merely by pressing a **HEX DATA/FUNCTIONs** key and entering parameters as required.



An optional cable, PROMPT-SER, directly connects the PROMPT system to virtually any terminal via a rear access slot. Another cable, PROMPT-SPP, allows programs and data to be downloaded from the Intellec Microcomputer Development System to the PROMPT system for debugging.

You enjoy easy access to the pins of the executing processor via this **I/O PORTS and BUS CONNECTOR**. Only the EA external access, SS single step and X1, X2 clock inputs are reserved for the PROMPT system.

Thus program or data memory may be expanded beyond that provided on-chip or in the PROMPT system. I/O ports can be expanded, as with the 8243, or peripheral controllers can be memory-mapped. The I/O ports and Bus connector allows the execution socket processor to be directly interfaced to your prototype system, yet be controlled from the PROMPT panel.

The **COMMAND/FUNCTION GROUP** panel keyboard and displays completely control PROMPT 48 – a teletypewriter or CRT terminal is not needed.

A hyphen prompting character appears whenever a command or function can be entered. Addresses and data are shown whenever EXAMINing registers and memory. Parameters for COMMANDs and FUNCTIONs are also shown.

[2] **Port 2 MAP** allows you to specify the direction of each pin on port 2. Port 2 is multiplexed to address external program memory and expand I/O. Thus it must be buffered; the P2 MAP command establishes the direction of buffering.

[3] **Program EPROM** programs 8748 EPROMs.

[4] **Byte Search with optional mask** sweeps through register, data or program memory searching for byte matches. Starting and ending memory addresses are specified.

[5] **Word Search with optional mask** sweeps through register, data or program memory searching for word matches. Starting and ending memory addresses are specified.

[6] **Hex Calculator** computes hexadecimal sums and differences.

[7] **8748 Program for Debug** is similar to Program EPROM, but ensures that the top of program memory contains monitor reentry code for debugging.

[8] **Compare** will verify any portion of EPROM program memory against PROMPT memory.

[9] **Move Memory** allows blocks of register, data or program memory to be moved.

[A] **Access** specifies one of six access modes for PROMPT 48. For example, EPROM, PROMPT RAM or external program memory, and a variety of input/output options may be selected.

[B] **Breakpoint** allows you to set and clear any or all of the eight breakpoints.

[C] **Clears** portions of register, data or program memory.

[D] **Dumps** register, data, or program memory to PROMPT's serial channel, for example a teletypewriter paper tape punch.

[E] **Enter** (reads) register, data or program memory from PROMPT's serial channel.

[F] **Fetches** programs from EPROM to PROMPT RAM.

PROMPT 48™ SIMPLIFIES MICROCOMPUTING

Intellec PROMPT 48 simplifies the programming of MCS-48 systems. Like the 8748 it is radically new, highly integrated, and expandable. Like the MCS-48 family, it is low cost, and ideal for small applications and programs. It is a design aid, not a development system with sophisticated software and peripherals.

"PROMPT" stands for PROgraMming Tool. It is a programmer for 8748 EPROMs, and a versatile aid for debugging MCS-48 programs. Programs can be entered via its integral panel keyboard, programming socket, or serial channel. Almost any terminal can be interfaced to the serial channel, including a teletypewriter, CRT, or the Intellec Microcomputer Development System.

Programs, written first in assembly language, are entered in machine language and debugged with calculator-like ease on the large, informative display and keyboard panel. Most MCS-48 operations can be specified with only two keystrokes.

Once entered, routines can be exercised one instruction (single step) or many instructions at a time. The principal MCS-48 register — the accumulator — is displayed while single-stepping. Programs can be executed in real-time (GO NO BREAK) or with as many as eight different breakpoints (GO WITH BREAK).

PROMPT 48 is a complete, fully assembled and powered microcomputer system including program memory, data memory, I/O and system monitor beyond that available on MCS-48 single component computers. 1K bytes of PROMPT system RAM serve as "writable program memory" — a ROM simulator for the program memory on each MCS-48 computer. 256 bytes of PROMPT system RAM serve as "external data memory," beyond the 64 register bytes on each MCS-48 computer. Users may further expand program or data memory via the panel I/O PORTS and BUS CONNECTOR.

The PROMPT 48 manual includes chapters for the reader with little or no programming experience. Topics treated range from number systems to microcomputer hardware design. A novel, unifying set of tutorial diagrams — MICROMAPs — simplify microcomputer concepts.

PROMPT's handy, pocket-sized reference cardlet can be affixed to the mainframe. Programming pads aid in the organization and documentation of programs. These features, plus a comprehensive design library of manuals, articles and application notes, make the Intellec PROMPT 48 ideal for the newcomer to microcomputing.

THE REVOLUTIONARY MCS 48™ SINGLE COMPONENT COMPUTER

Advances in n-channel MOS technology allow Intel, for the first time, to integrate into one 40-pin component all computer functions:

8-bit CPU
1K x 8-bit EPROM/ROM Program Memory
64 x 8-bit RAM Data Memory
27 Input/Output Lines
8-bit Timer/Event Counter

More than 90 instructions — each one or two cycles — make the single chip MCS-48 equal in performance to most multi-chip microprocessors. The MCS-48 is an efficient controller and arithmetic processor, with extensive bit handling, binary, and BCD arithmetic instructions. These are encoded for minimum program length: 70% are single byte operation codes, and none is more than two bytes.

Three interchangeable, pin-compatible devices offer flexibility and low cost in development and production:

- 8748 with user-programmable and erasable EPROM program memory for prototype and pre-production systems
- 8048 with factory-programmed mask ROM memory for low-cost, high volume production
- 8035 without program memory, for use with external program memories

Each MCS-48 processor operates on a single +5V supply, with internal oscillator and clock driver, and circuitry for interrupts and resets. Extra circuitry is in the 8048 ROM processor to allow low power standby operation: the 64 x 8 RAM data memory can be independently powered.

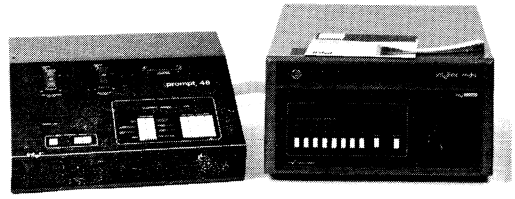
For systems requiring additional compatibility, the MCS-48 can be expanded with the new 8243 I/O expander, 8155 I/O and 256 byte RAM, 8755 I/O and 2K byte EPROM or 8355 I/O and 2K ROM devices. MCS-48 processors readily interface to MCS-80/85 peripherals and standard memories.

PROMPT 48 comes complete with two of these revolutionary MCS-48 processors — an 8748 and an 8035.

EXPANDING PROMPT 48™

PROMPT 48 may be expanded beyond the resources on the MCS-48 single component computer and those in the PROMPT system. External program and data memory may be interfaced and input/output ports added with the 8243 I/O Expander.

The PROMPT panel I/O Ports and Bus Connector allow easy access to all MCS-48 pins except those reserved for control by the PROMPT system, namely EA external access, SS single step, and X1, X2 clock inputs.



A Specialized PROM Programmer Kit, the PROMPT-SPP, allows PROMPT 48 to serve as an economical 8748 Specialized PROM Programmer peripheral in Intellec Microcomputer Development Systems. The PROMPT-SPP cable plugs directly into the rear panel of the Intellec Microcomputer Development System.

PROMPT 48 can be fully controlled either by the panel keyboard and displays, or remotely by a serial channel. Thus a teletypewriter or CRT can be used but neither is required. Full remote control by a serial channel means users can download and debug programs using the PROMPT 48 together with an Intellec Microcomputer Development System.

SPECIFICATIONS

TIMING

Basic Instruction	2.5 μsec
Cycle Time	t_{CY} = 2.5 μsec
Clock	6 MHz ±0.1%

MEMORY BYTES

	Maximum	On Chip	In PROMPT 48
Register	64	64	0
Data	3328	0	256
Program	4096	1024 EPROM	1024 RAM

The 8748 contains 64 bytes of register memory, no external data memory, and 1024 bytes of EPROM program memory. The PROMPT system provides 256 bytes of external data memory, and 1024 bytes of RAM program memory. PROMPT RAM program memory can be used in place of the On-Chip EPROM program memory; thus programs less than 1024 bytes may be designed. For larger programs additional memory can be directly interfaced to the MCS-48 bus via the PROMPT panel I/O Ports and Bus Connector.

I/O PORTS

All MCS-48 I/O Ports are accessible on the PROMPT panel connector.

BUS is a true bidirectional 8-bit port with associated strobes. If the bidirectional feature is not needed, bus can serve as either a statically latched output port or a non-latching input port. Input and output lines cannot be mixed.

PORTS 1 AND 2 are each 8 bits wide. Data written to these ports is latched and remains unchanged until written. As inputs these lines are not latching. The lines of ports 1 and 2 are called quasibidirectional. A special output structure allows each line of port 1 and half of port 2 to serve as an input, an output, or both. Any mix of input, output, and both lines is allowed.

Three pins — T0, T1 and INT — can serve as inputs; T0 can be designated as a clock output. Input/Output can be expanded via the PROMPT panel connector with a special I/O expander (8243) or standard peripherals.

RESET and INTERRUPTS

RESET initializes the PROMPT system and enters the monitor. MONITOR INTERRUPT exits a user program gracefully, preserving system status and entering the monitor. USER INTERRUPT causes an interrupt only if the PROMPT system is running a user program. The processor traps to location 3_{16}. The MCS-48 timer/event counter is not used by the PROMPT system and is available to the user.

Either timer flag or interrupt will signal when overflow has occurred. The timer interrupt can be used only in the GO NO BREAK (real time) mode.

EPROM PROGRAMMING

PROMPT 48 provides a programming socket to directly program 8748s. Programs are loaded into the PROMPT RAM program memory via keyboard, EPROM, teletypewriter, or other serial interface.

A fail-safe interlock ensures programming pulses are applied only if the device is properly inserted. Inadvertent reprogramming is prevented by a read-before-write programming algorithm. Each location may be individually programmed, one byte at a time.

PANEL I/O PORTS and BUS CONNECTORS

All MCS-48 pins, except five, are accessible on the I/O Ports and Bus Connector. The five reserved for PROMPT system control are EA external access, SS single step, X1, X2 crystal inputs, and 5 V.

Due to internal buffering of the MCS-48 bus, access times will be negligibly degraded by the PROMPT system. Since MCS-48 processors do not communicate internal address gate status, bus data must be driven out if neither PSEN nor RD is asserted.

SYSTEM DEVICES

Both user programs and the PROMPT monitor enjoy access to system devices: serial I/O, panel displays and keyboard. These are memory-mapped to program memory addresses beyond 2K.

The SERIAL I/O port (data 820_{16}, control 821_{16}) is defined by software and jumpers for 110 baud, 20 mA current loop, but can easily be jumpered for other baud rates and RS232C levels. Asynchronous or synchronous transmission, data format, control characters, and parity can be programmed.

Software is used to debounce the PANEL KEYBOARD (data 810_{16}). The monitor's input routines (see SOFTWARE DRIVERS) provide this debouncing and can be called from user programs.

Eight display ports (data 810-817_{16}) allow each of the PANEL DISPLAYS to be written from user programs. Data written on a display device will time out after a fixed interval. Displays must be refreshed on a polled or interrupt-driven basis. User programs can call SOFTWARE DRIVERS which provide this capability.

COMMANDS

☐ GO { ☐ Single Step / ☐ With Break / ☐ No Break } ☐ Examine/Modify { ☐ Register / ☐ Data / ☐ Program } Memory

☐ Open Previous/Clear Entry ☑ Next ⊡ Execute/End

FUNCTIONS

[2] Port 2 Map
[3] Program EPROM (8748)
[4] Search (R, D or P)* Memory for 1 byte, optional mask
[5] Search (R, D or P) Memory for 2 bytes, optional mask
[6] Hexadecimal Calculator +, –
[7] 8748 Program EPROM for Debug
[8] Compare EPROM with memory
[9] Move Memory (R, D or P)
[A] Access
[B] Breakpoint
[C] Clear Memory (R, D or P)
[D] Dump Memory (R, D or P)
[E] Enter (Read) Memory (R, D or P)
[F] Fetch EPROM Program Memory

*R, D or P is Register, Data or Program.

SOFTWARE DRIVERS

Panel Keyboard In: KBIN, KDBIN
Panel Display Out: DGS6, DGOUT, HXOUT, BLK, REFS, ENREF
Serial Channel: CI, CO, RI, PO, CSTS

CONNECTORS

Serial I/O: 3M 3462-0001 Flat Crimp/AMP 88106-1 Flat Crimp/TI H312113 Solder/AMP 1-583485-5 Solder.

Panel I/O Ports and Bus Connector: 3M 3425 Flat Crimp. A complete cable set including wirewrap header for prototyping is included with each PROMPT.

EQUIPMENT SUPPLIED

PROMPT 48 mainframe with two MCS-48 processors (8748, 8035), display/keyboard, EPROM Programmer, power supply, cabinet and ROM-based monitor.

110 VAC power cable, 110 or 220 VAC, fuse, Panel I/O Ports and Bus Connector cable set, PROMPT 48 User's Manual, PROMPT 48 Monitor Listing, Reference Cardlet, PROMPT 48 Programming Pads, MCS-48 Microcomputer User's Manuals, MCS-48 Assembly Language Manual, PROMPT 48 Schematics.

ORDERING INFORMATION

PROMPT-48	— Complete PROMPT 48, set 110 VAC
PROMPT-48-220V	— Complete PROMPT 48, set 220 VAC
PROMPT-SER	— Serial cable connects PROMPT to TTY, CRT
PROMPT-SPP	— Specialized PROM Programmer Kit connects PROMPT 48 to Intellec Microcomputer Development System for EPROM programming

Additional PROMPT 48 Programming Pads (98-401) and manuals (98-402) may be ordered from Intel Literature Department.

PHYSICAL CHARACTERISTICS

Maximum Height:	13.5 cm (5.3 in.)
Width:	43.2 cm (17 in.)
Maximum Depth:	43.2 cm (17 in.)
Weight:	9.6 kg (21 lb.)

DEVELOPMENT SYSTEMS

ELECTRICAL REQUIREMENTS

Either 115 or 230 VAC (±10%) may be switch-selected on the mainframe. 1.8 amps max current (at 125 VAC).

Frequency is 47-63 Hz.

ENVIRONMENTAL

Operating Temperature:	0°C to +40°C
Non-Operating Temperature:	–20°C to +65°C

INTELLEC® PROMPT 80™
8080 MICROCOMPUTER DESIGN AID

Simplifies microcomputing

Enter, run, debug and save machine language programs with calculator-like ease

Complete, fully-assembled microcomputer, including:

CPU	Standard 8080A on popular SBC 80/10 Single Board Computer
Memory	1K byte RAM, 3K byte ROM, and two spare 1K byte 8708 EPROMs
I/O	24 programmable parallel I/O (TTL) lines, including two: 8-bit ports, fully implemented switches, displays Programmable serial I/O interfaces directly with most terminals
Power	Only 110 or 230 VAC required

Low Cost

PROM Programmer for 8708/2708/2704 UV Erasable, Electrically Reprogrammable ROMs (EPROMs)

Integral keyboard and 16-digit display (no teletypewriter or CRT terminal required)

Extensive system monitor software in ROM:
- Examine/Display/Modify Registers and Memory
- Enter, Run, Test, Single-Step programs
- Hex Calculator
- Move, Search Memory Blocks

Self-programmable — user can add functions

Comprehensive design library

Intellec® PROMPT 80™ is a low-cost, fully assembled microcomputer design aid. PROMPT 80 simplifies the programming of SBC 80 and System 80 microcomputers, as well as 8080 processors, 8708/2708/2704 EPROMs and 8255/8251 programmable I/O devices. 8080 programs can be entered and debugged with calculator-like ease on the large, informative display and keyboard panel. The comprehensive design library with tutorial manual is ideal for newcomers to microcomputing.

PROMPT 80's SBC 80/10 can be expanded using the SBC modular cardcage. And PROMPT 80 can serve as an economical 8708 Specialized PROM Programmer (SPP) peripheral in Intellec Microcomputer Development Systems.

DEVELOPMENT SYSTEMS

PROMPT SIMPLIFIES MICROCOMPUTING

Intellec PROMPT 80 simplifies the programming of 8080 processors, SBC 80 and System 80 microcomputers, as well as 8708 EPROMs and 8255/8251 programmable I/O devices.

PROMPT is a low-cost programming tool. It is a microcomputer design aid — not a development system with sophisticated software and peripherals.

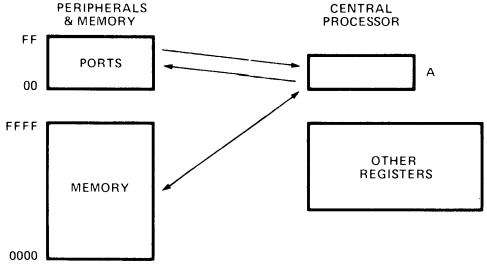
PROMPT encourages the preparation and verification of small, modular routines which together may comprise sizable programs. These are written in assembly language, then entered in machine language and debugged with calculator-like ease on the large, informative display and keyboard panel.

Many 8080 operations can be specified with only two key strokes. Once entered, programs can be exercised one instruction (single step) or many instructions at a time. And, any of the 8080 registers can be watched while single-stepping.

Programs are readily saved and instantly reloaded via UV Erasable, Electrically Reprogrammable ROMs (EPROMs). PROMPT 80 can program the popular 8708 EPROMs in small blocks, so routines can be debugged and saved incrementally. Several programs are pre-recorded as examples on PROMPT's spare 8708 EPROMs.

PROMPT 80 is a complete, fully assembled and powered 8080 microcomputer, including RAM, I/O, and system monitor in ROM. Twenty-four lines of programmable, TTL-compatible, parallel I/O are easily accessed on a panel connector. Two 8-bit ports are fully implemented, one with displays for output, the other with displays and switches for input. PROMPT's programmable serial I/O interfaces directly with most terminals. A teletypewriter or CRT can be used, but neither is required because of PROMPT's built-in keyboard and display.

The PROMPT 80 manual includes chapters for the reader with little or no programming experience. Topics treated range from the number system to microcomputer hardware design. A novel, unifying set of tutorial diagrams — MICROMAP™ — simplify microcomputer concepts.



PROMPT's handy, pocket-sized reference cardlet can be affixed to the mainframe. Programming pads aid in the organization and documentation of programs. These features, plus a comprehensive design library of manuals, articles, and applications notes, make Intellec PROMPT 80 ideal for the newcomer to microcomputing.

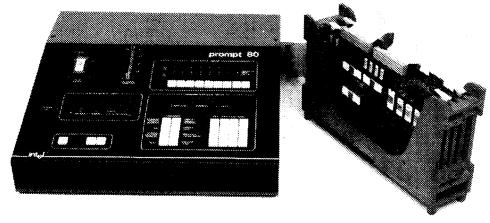
A COMPLETE COMPUTER

The heart of PROMPT 80 is the popular SBC 80/10 Single Board Computer, a complete computer on a single printed circuit board. The SBC 80/10 includes an 8080A, 1K bytes of static RAM memory, and sockets for 4K bytes of EPROM memory. Signals to the SBC 80/10 include 48 programmable, parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable serial channel, a multi-source single level interrupt network, and bus drivers for memory and I/O expansion. Read-only-memory may be added in 1K byte increments using Intel 8708 EPROMs or 8308 ROMs.

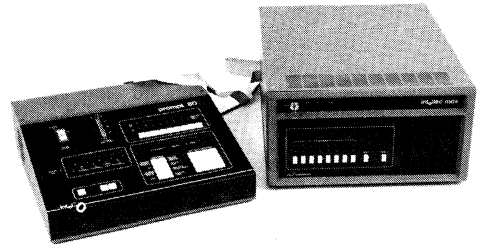
The central processor for PROMPT's SBC 80/10 is Intel's powerful 8-bit n-channel MOS 8080A CPU. The 8080A contains six 8-bit general-purpose registers and an accumulator. The six general-purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

The 8080A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located anywhere in read/write memory, may be used as a last-in/first-out store. The contents of the program counter, accumulator, flags, and all of the general-prupose registers are stacked using a 16-bit pointer. Subroutine nesting is bounded only by memory size.

EXPANDING PROMPT 80™



PROMPT 80's SBC 80/10 can be expanded via the SBC 604 Modular Cardcage. The cardcage houses the SBC 80/10 and up to three expansion boards. Memory and I/O can be added in various combinations. Additional power may be required.

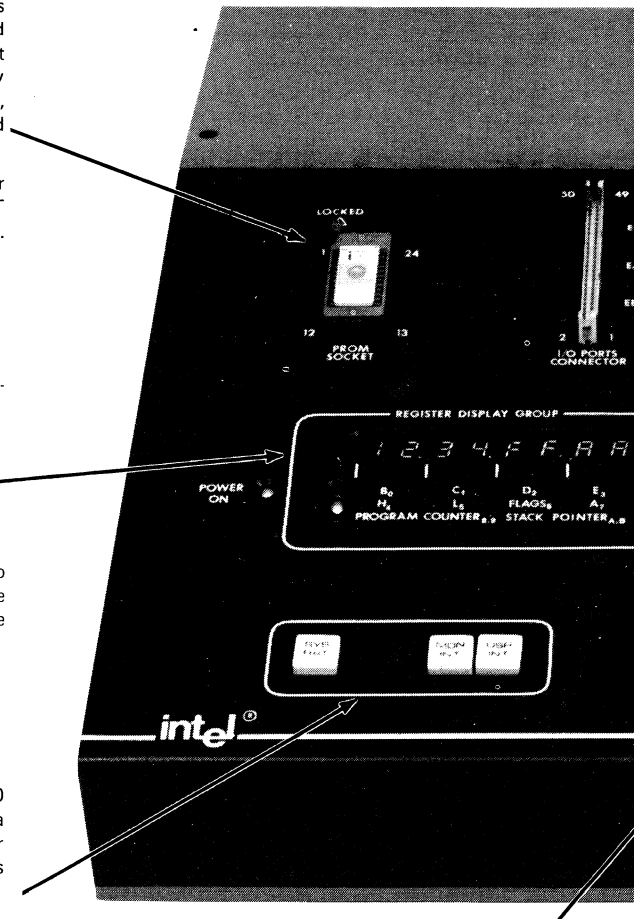


A Specialized PROM Programmer kit, the PROMPT-SPP, allows PROMPT 80 to serve as an economical 8708 Specialized PROM Programmer peripheral in Intellec Microcomputer Development Systems. The PROMPT-SPP cable plugs directly into the rear panel of the Intellec Microcomputer Development System.

PROM PROGRAMMER

8708 UV Erasable, Electrically Reprogrammable ROMs (EPROMs) can be easily programmed, compared, and transferred to RAM using the zero-insertion force socket on the panel. A new technique allows 8708 to be partially programmed in multiple blocks of 16 bytes. Thus, small, modular routines can be entered, tested, and readily saved using EPROM.

EPROMs can also be conveniently duplicated. The master (original) device plugs into the SBC 80/10 inside PROMPT 80, and can be copied to the panel programming socket.



REGISTER/DISPLAY GROUP

All 8080 registers can be displayed, even while single-stepping programs. The registers are shown in three rows:

first row:	B	C	D	E
second row:	H	L	Flags	A
third row:	Program Counter		Stack Pointer	

One register row is visible at a time. Three small LEDs to the left of these rows indicate which row is displayed. The SCROLL REGISTER DISPLAY command displays the next row (first, second, third, etc.)

RESET, INTERRUPTS

SYS RST resets the system, initializes the PROMPT 80 registers and enters the monitor. MON INT interrupts a user program and enters the monitor saving the user registers. USR INT is a user interrupt which traps PROMPT 80 to location $3C02_{16}$.

MONITOR

A comprehensive system monitor resides in three 1K ROMs. It drives PROMPT's keyboard, displays, and responds to COMMANDS and FUNCTIONS. The monitor is modular, organized so that the third ROM may be removed if F FUNCTIONS are not required. This allows sizable user routines – as much as 2K ROM/EPROM and nearly 1K RAM – to be exercised.

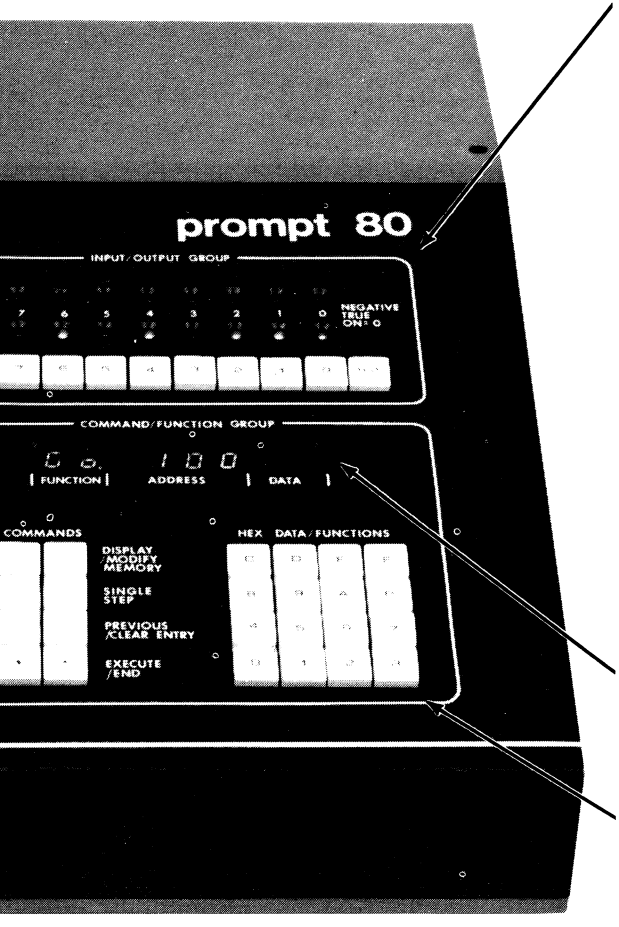
COMMANDS

PROMPT 80 commands are compatible with those used by Intel's SDK, SBC, and Intellec monitors.

You can EXAMINE/MODIFY a REGISTER, or DISPLAY/MODIFY MEMORY. Then either the NEXT or PREVIOUS register and memory locations can be opened with one button.

The GO command executes programs, allowing multiple, optional breakpoints. Or a program can be SINGLE STEPped, executed one instruction at a time.

The SCROLL REGISTER DISPLAY command displays the next row of the REGISTER/DISPLAY GROUP.



INPUT/OUTPUT GROUP

The INPUT/OUTPUT (I/O) GROUP features two fully implemented 8-bit ports, both with displays, and with latch switches for the input port E9. The port addresses are clearly marked E8 and E9. Those two ports and a third, at EA, are easily accessible on the I/O PORTS CONNECTOR. Negative true logic is used throughout the I/O GROUP and PORTS CONNECTOR to enhance noise immunity and allow wire-ANDing.

PARALLEL I/O

The I/O PORTS CONNECTOR provides easy access to 24 parallel, TTL-compatible lines. These lines are addressed as three ports (each 8 lines), port E8, E8, and EA.

These ports can be defined to be input or output by software. Defining control words, tabulated in "Specifications", are sent OUT to port EB, the control word register.

SERIAL I/O

PROMPT's programmable serial I/O readily interfaces with most terminals. Jumpers select either 20 mA teletypewriter (TTY) current loop or RS-232C operation, and the appropriate communications frequency. Asynchronous or synchronous transmission, data format, control characters, parity, and transmission rate can be programmed.

A serial cable kit, PROMPT-SER, connects PROMPT to either a teletypewriter or RS-232C standard (CRT) terminal through a rear chassis access slot. Teletypewriters may require minor reader control modifications.

COMMAND/FUNCTION DISPLAYS

The COMMAND/FUNCTION displays show addresses and data when DISPLAYing MEMORY, and parameters for COMMANDS and FUNCTIONS are entered.

FUNCTIONS

Eight FUNCTIONS are provided by PROMPT. Others may be added by the user. Pressing a HEX DATA/FUNCTIONS key (0–7) starts a function.

[0] is F0 Read Paper Tape
[1] is F1 Write Paper Tape
[2] is F2 Program EPROM, Compare
[3] is F3 Compare EPROM
[4] is F4 Transfer EPROM to RAM
[5] is F5 Move Block Memory
[6] is F6 Hexadecimal Calculator, +, –
[7] is F7 Byte Search Memory, optional mask
[8] is F8 Word Search Memory, optional mask

Commands are entered naturally, like phrases in a sentence: the NEXT parameters are separated bycommas [,] and command sentences end with [.] EXECUTE/END.

The commands do what makes sense. For example:

GO [ ] [1] [0] [0] [.] EXECUTE/END
starts the program at address 100.

GO [ ] [1] [0] [0] [,] NEXT [2] [0] [0] [.] EXECUTE/END
starts the program at 100, but stops if you get to 200, a breakpoint.

GO [ ] [.] EXECUTE/END
starts the program where you last stopped.

SPECIFICATIONS

WORD SIZE

Instruction: 8, 16, or 24 bits
Data: 8 bits

TIMING

Basic Instruction: 1.95 μsec
Cycle Time: t_{CY} = 488 nsec
Clock: 2.058 MHz ± 0.1%

MEMORY BYTES	Addressing	On Board	Monitor Uses
ROM/PROM	$0–0FFF_{16}$	4096	2048 or 3072
RAM	$3C00–3FFF_{16}$	1024	114

Up to 48K bytes may be added using optional RAM, ROM, or PROM expansion boards and the SBC 604 Cardcage.

I/O ADDRESSING

Ports E4 to E7 are dedicated to PROMPT's display/keyboard groups. Ports E8 to EB drive the panel I/O PORTS CONNECTOR and PROM SOCKET.

	Dedicated to Display/Keyboard				I/O Ports Connector/ PROM Socket				Serial I/O USART	
	A	B	C	Control	A	B	C	Control	Data	Control
PORT	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED

PARALLEL I/O

The panel I/O ports can be defined input or output by OUTputing control words to port address EB.

HEX Control Word (OUT this to EB)	Port E8 Bits 7–0	Port E9 Bits 7–0	Port EA Bits 7–4	Port EA Bits 3–0
80	OUTPUT	OUTPUT	OUTPUT	OUTPUT
81	OUTPUT	OUTPUT	OUTPUT	INPUT
82	OUTPUT	INPUT	OUTPUT	OUTPUT
83	OUTPUT	INPUT	OUTPUT	INPUT
84 or 85	OUTPUT	STROBED OUTPUT	OUTPUT	Bits 2, 1, 0 are strobes
86 or 87	OUTPUT	STROBED INPUT	OUTPUT	

All input ports are TTL-compatible. Ports E8 and EA are one-load fully TTL-compatible as output. Port E9 is ordinarily used as input. When used as output, E9 can sink at least one low-power TTL load.

SERIAL I/O

The serial I/O port is defined by software and jumpers. PROMPT is configured at the factory for 20 mA current loop TTY interface, but can easily be jumpered for RS-232C levels.

Asynchronous or synchronous transmission, data format, control characters, parity and transmission rate can be programmed.

INTERRUPTS

PROMPT 80 provides a panel user interrupt to $3C02_{16}$. The SBC 80/10 supports single level vectoring to location 38_{16}. Requests may originate from user-specified I/O (2), the parallel ports (2), or serial port (2).

EPROM PROGRAMMING

8708/2708/2704 EPROMs can be programmed in multiple blocks of 16 bytes. Starting and ending memory address need only differ by a multiple of 16, and starting EPROM address end XX0 hexadecimal (X = don't care). Programming time is 115 sec for 1K byte, 3 sec for 16 bytes.

The 8708 may be erased by exposure to high intensity shortwave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (UV intensity X exposure time) is 10 W-sec/cm^2.

SYSTEM MONITOR

Resides in three 8308 ROMs, 0 to $3FF_{16}$, 400_{16} to $7FF_{16}$, and 800_{16} to BFF_{16}. The third ROM implements F FUNCTIONS, and can be removed. PROMPT has an unused ROM/EPROM socket at address $C00_{16}$ to FFF_{16}.

COMMANDS

Examine/Modify Register	Display/Modify Memory
Go (with optional breakpoints)	Single Step
Scroll Register Display	Open Previous/Clear Entry
Next .	. Execute/end

FUNCTIONS

0 Read Tape
1 Write Tape
2 Program EPROM, Compare
3 Compare EPROM
4 Transfer EPROM to RAM
5 Move Block Memory
6 Hexadecimal Calculator, +, –
7 Byte Search Memory, optional mask
8 Word Search Memory, optional mask

SOFTWARE DRIVERS

Panel Keyboard Input	Panel Display Output
Console Terminal Input	Console Terminal Output
TTY Reader Input	TTY Punch Output

CONNECTORS

PROMPT Panel I/O Ports	3M 3425 Flat
SBC 80/10 Parallel I/O	3M 3415 Flat
SBC 80/10 Serial I/O	3M 3462 Flat
SBC 80/10 Bus	CDC VPB01E43D00A1
SBC 80/10 Auxiliary Bus	TI H312130

EQUIPMENT SUPPLIED

PROMPT 80 mainframe with SBC 80/10, display/keyboard, PROM Programmer, power supply, cabinet, and ROM-based system monitor
(2) 8708 EPROMs with pre-recorded example programs
110 VAC power cable, 110 or 220 VAC fuse
PROMPT 80 User's Manual, PROMPT 80 Monitor Listing
PROMPT 80 Reference Cardlist, PROMPT 80 Programming Pads
8080 Systems User's Guide, 8080 Assembly Language Manual
System 80/10 Hardware Reference Manual
Design Library of Application Notes, Article Reprints
PROMPT 80 Schematics

ORDERING INFORMATION, COMPATIBLE EQUIPMENT

PROMT-80 – Complete PROMPT 80 set 110 VAC
PROMT-80-220V – Complete PROMPT 80 set 220 VAC
PROMT-SER – Serial Cable connects PROMPT to TTY, CRT
PROMT-SPP – Specialized PROM Programmer Kit connects PROMPT 80 to Intellec® Microcomputer Development Systems for 8708 EPROM programming.
All SBC products (additional memory, I/O, wire-wrap, and other boards) are compatible with PROMPT's SBC 80/10.
Additional PROMPT 80 Programming Pads can be ordered from Intel Literature Department.

PHYSICAL CHARACTERISTICS

Maximum Height:	13.5 cm	(5.3 in.)
Width:	43.2 cm	(17 in.)
Maximum Depth:	43.2 cm	(17 in.)
Weight:	9.6 kg	(21 lb)

ELECTRICAL REQUIREMENTS

Either 115 or 230 VAC (±10%) may be switch-selected on the mainframe. 1.8 amps max current (at 125 VAC)
Frequency is 47–63 Hz.

Voltage	Internal PROMPT 80 Supply	PROMPT 80 Requires
+26.5	0.1A	0.03A
+12	1.2A	0.5A
+ 5	6.0A	5.0A
– 5	0.3A	0.1A
–12	0.3A	0.2A

Fixed over-voltage protect on 5V supply 6.2–6.7 volts.

ENVIRONMENTAL

Operating Temperature: 10°C to 40°C
Non-operating Temperature: –20°C to 65°C

DEVELOPMENT SYSTEMS

14

Software and Training

SOFTWARE AND TRAINING

INTRODUCTION

Insite™, the Intel Software Index and Technology Exchange with over 200 contributed 8-bit programs facilitates the use of Intel Microcomputer products. This section provides information describing Insite and includes partial listings of the 4-bit and 8-bit program libraries. An Insite program submittal form is also included.

Intel Cross Product Software programs are written in FORTRAN IV and are designed to run on a large computer system for the purpose of code generation or microcomputer simulation. Intellec® System resident assemblers and compilers are detailed in Section 13.

Intel provides complete training for all of its system related products. Courses are given regularly at Intel's Santa Clara, California; Boston, Massachussetts; and Chicago, Illinois Training Centers. These centers are staffed by highly trained and experienced instructors. This section provides outlines for several of the courses offered by Intel. These courses are also available for on-site courses at your facility.

TABLE OF CONTENTS

USERS PROGRAM LIBRARY

Over 200 8-bit programs

Over 100 4-bit programs

Source Paper Tapes and Listings available for all programs

Updates of new programs sent every other month

Five free tapes sent with new membership

One-year free membership or five free Source Tapes for each accepted program submittal

Insite™, Intel's Software Index and Technology Exchange, is a collection of programs, subroutines, procedures and macros written by users of Intel's 4004, 4040, 8008 and 8080 microcomputers, SBC 80 OEM computer systems, and Intellec® development systems. Thanks to customer contributions to Insite™, Intel is able to make these programs available to all users of Intel® microcomputers. By taking advantage of the availability of these general-purpose routines, the microcomputer design engineer and programmer can save many hours of programming and debugging time. The library of programs also serves as a good learning tool for those unfamiliar with Intel assembly language or PL/M, Intel's high-level language for the 8008 and 8080 microcomputers.

LIBRARY PROGRAMS AVAILABLE ON PAPER TAPE

PROGRAM LIBRARY MANUAL

Each member will be sent the Program Library Manual which is a collection of source listings of library programs 3 pages and under. Longer programs are represented by an abstract which indicates the function of the routine, the required hardware and software, and memory requirements.

User's Library members will be updated regularly with new programs submitted to Insite during the subscription period.

Here is a sampling of the types of programs contained in Insite:

Floating Point Packages
Transcendental and Trig Function
BASIC Compiler
Software and Hardware Debugging Routines
Multiple Precision Arithmetic Routines
Peripheral Interfaces and Drivers
Disassemblers
Cross Assemblers for Mini-Computers
Games

SOURCE PAPER TAPES AND LISTINGS

Source paper tapes and listings are available for most programs in Insite.™ A small handling fee will be charged for each source tape and listing. Ordering information can be found in the Program Library Manual. With your subscription, Insite™ will send you at no charge five free source tapes of your choice.

MEMBERSHIP

Membership in Insite is available on an annual basis. Users may become a member through program contribution or a membership fee. The membership fee is $100 a year and is processed by purchase order or check. Please use the attached order form.

PROGRAM SUBMITTAL

Programs submitted for our review must follow the guidelines listed below:

1. Programs must be written in a standard Intel Assembly Language or PL/M. These languages are documented in the following manuals:
   a. 8008 Assembly Programming Manual #98-019B
   b. 8080 Assembly Language Programming Manual #98-004C
   c. 4004/4040 Assembly Language Programming Manual #98-025A
   d. 8008/8080 PL/M Programming Manual #98-108A

PROGRAM SUBMITTAL (Cont)

2. A source listing of the program must be included. This must be the output listing of a compile or assembly. All accepted programs should assemble or compile correctly with no syntax errors. No consideration will be given to partial programs or duplication of existing programs.

3. A test program which assures the validity of the contributed program must be included. This must show the correct operation of the program.

4. A source paper tape or diskette of the contributed program is required. This will be used for the reproduction of tapes for other members.

Complete the Submittal Form as follows: (please type or print)

a. Processor (check appropriate box).

b. Program title: Name or brief description of program function.

c. Function: Detailed description of operations performed by the program.

d. Required hardware:

   For example: TTY on Port 0 and 1
   Interrupt Circuitry
   I/O Interface
   Machine line and configuration for cross products

e. Required software:

   For example: TTY Driver
   Floating Point Package
   Support software required for cross products

f. Input parameters: Description of register values, memory areas or values accepted from input ports.

g. Output results: Values to be expected in registers, memory areas or on output ports.

h. Program details (for resident products only):
   (1) Register modified
   (2) RAM required (bytes)
   (3) ROM required (bytes)
   (4) Maximum subroutine nesting level

i. Assembler/Compiler used:

   For example: PL/M
   Intellec® Macro Assembler
   IBM 370 Fortran IV

j. Programmer company and address.

insite™

PARTIAL PROGRAM INDEX – 8-BIT USER'S LIBRARY

TITLE

3-Byte Positive Fractional Multiply
8-Bit Multiply and Divide
8-Bit Random Number Generator
16-Bit 2's Complement Signed Multiplication
16-Bit CRC for Polynomial X16+X12+X5+1
16-Bit Division – 16-Bit Result
16-Bit Division – 16-Bit Result
16-Bit Multiply – 16-Bit Result
16-Bit Multiply – 16-Bit Result
16-Bit Multiply – 32-Bit Result
16-Bit Random Number Generator
16-Bit Square Root Routine
32-Bit Binary to BCD Conversion, Leading Zero Blanking
32-Bit Divide Subroutine
4040 Cross Assembler for Intellec 8/MOD 80 and MDS-800
8008 Cross Assembler for HP 3000
8008 Cross Inverse Assembler for HP 2100
8008 Disassembler
8008 MACRO Definition Set for Assembly on PDP-11
8080 Cross Assembler for HP 3000
8080 Cross Assembler for HP 2100 DOS
8080 Disassembler
8080 Floating Point Extended Math Package
8080 Floating Point Package with BCD Conversion Routine
8080 Idle Analyzer for Approximating CPU Utilization
8080 I/O System Status Display
8080 Least Squares Quadratic Fitting Routine
8080 RAM Memory Test

A/D Converter Routine
Adaptive Game Program
Algebraic Compare Subroutine
APL Graphic Display on a 5 X 7 Dot Matrix
Approximating Routine
ASCII Display
Absorbance Calculation
Assembler Oriented Centronics 306 Line Printer Handler and Error Only Assembler

Banner Print and Punch
BASIC CPU State Vector Maintenance
BASIC Digital Panel Meter Call
BASIC Interpreter
BASIC/M Translator and Interpreter
BCD to BIN Conversion Routine
BCD to/from Binary Conversion
BCD Input and Direct Conversion to Binary Routine
BCD Multiplication
BCD Sum for 8008
BCD Up/Down Counter
BIN to BCD Conversion Routine
Binary to BCD Subroutine
Binary to HEX Routine
Binary Loader for MDS
Binary Multiplication – 24-Bit
Binary Search

TITLE

Binary Search Routine
BINDECBIN – Binary to/from BCD
BINLB – 8080 System Loader
Blackjack
$BLPT
BOOT – Bootstrap Loading and Program Patching

Calendar Subroutine
Character Interpreted Memory Dump
Clock Subroutine
Compare
Compare Object Code Tape with Memory
Control Data Output
CRECH – Cyclic Redundancy Check
Cross Assembler for PDP-11
Cross Assembler for PDP-11
Cross Assembler for Nova 1200
Cross Assembler for Nova 1220, IBM 360/40 and CDC 3300
Cross Assembler for Varian Data Machine
CRTBZ – GET
Cyclic Redundancy Character Generator
Cyclic Redundancy Check
Cyclic Redundancy Check for Data String of 2^{16} Bytes

Data Array Move
Data I/O PROM Processor
Decrement H and L Registers
Delete Comments
Diagnostic 1003 – Memory Validity Check
Digital to Analog Conversion for Eight Outputs
Disassembler
Disk Dump Routine for ICOM F DOS-11/MOD 80 Floppy DOS
Double Precision Integer Arithmetic Package
Double Precision Multiply

Elementary Function Package
ERLIST
Examin

Factorial of a Decimal Number
Fast Floating Point Square Root Routine
Fixed and Floating Point Arithmetic Routines
Fixed Point CHEBYSHEV Sine and Cosine for PL/M Users
Flag Processing Routine
Floating Point Decimal and HEX Format Conversion
Floating Point Format Conversion Package
Floating Point Math Package
Floating Point Package for Intel 8008 and 8080 Microprocessors
Floating Point Procedures
Floating Point Square Root

Gambol (Game)
Game of Life
Generalized Stepper Motor Drive Program
Gray to Binary Conversion

PARTIAL PROGRAM INDEX – 8-BIT USER'S LIBRARY (Continued)

TITLE

Handler for Tally PTP
HEX Convert – Convert Intel HEX Format to Prolog HEX File Converter
HEX to Decimal Conversion
HEX Format Paper Tape Dump for SDK
HEX Tape Loader for SDK
High Speed Paper Tape Reader with Stepper Motor Control

IBM Selectric Output Program
ICE-80 Disassembler
I-Command – Insert Data in HEX Form from TTY into RAM
Input/Output Commands for MDS
Intellec 8/MOD 80 – Silent 700 Interface
Interfacing the MDS and HP 2644A
Interrupt Driven Clock Routine
Interrupt Handler (Re-Entrant)
Interrupt Service Routine
I/O Simulation MACROS

K, Program Trap and Dump Routine
Kalah (Game)

Legible Paper Tape
List
Lewthwaite's Game
List Device Program
List 1 – High Speed List Program for Intellec 8
List/Print/Type "List SRC" on Diskette
Log Base 2

Mastermind (Game)
Match Game
Maze (Game)
Memory Compare
Memory Diagnostic Program
Memory Dump
Memory Test for the 8080
Memory Test Program
Model 101 Centronics Printer Handler
Mon 256 – 256-Byte PROM Monitor
Morse Code Generator
MUL/DIV Multi-Precision Pack for 8080

Natural Logarithm
N-Byte Binary Multiplication and Leading Zero Blanking
Nim (Game)
Nova Cross Assembler – Intel 8080
Numbers

Octal Code Conversion for PDP-11
Octal Debugging Program (ODT) for the MCS-80 Octal Computer
Octal PROM Programming

Page Break for Tektronix 4010 I/O Graphics Terminal
Page Listing Program
Paper Tape Reformatter for SDK
Pass – Parameter Passing Routine

TITLE

PDP-11 Binary File to Intel HEX File Converter
PL/M 80 Pass 3
PL/M Floating Point Interface
PL/M Histogram Procedure and Random Number Generat
PROM Programmer for Intellec 8
Proportional Power Control Image Builder
Punch Binary Tape
Punch Test or TTY Reader/Punch Test

RAM Check
RAM Test Program
RANDOM$BITS
Random Number Generator – RNGEN
Read and Interrupt Modifications for Intellec 8/MOD 80
Reader Test
Read/Write Routines for Interchange Tapes
Real Time Executive
RMSTF – Integration Routine
Run 0

Save/Restore CPU State on an Interrupt
SDK-80 Keyboard Monitor
Shellsorting Routine
Sin X, Cos X Subroutine
SMAL: Symbolic Microcontroller Assembly Language
Software Stack Routines for 8008
Source Paper Tape to Magnetic Cassette
SQRTF – Calculates 8-Bit Root of 16-Bit Number
Stage 2
Structured Assembler for 8080
Subroutine DMULT (Decimal Multiplication)
Subroutine Log – Common Logarithms
Subroutine SQRT
Symbol Table Dump for Intellec 8/MOD 80
Symbol Table List Routine

Tally – Use Tally 2200 Line Printer in Assembly Stage of Programming
Tally R2050 HSPTR Driver
Tape Duplicator
Tape Labeler for MDS
Teleprocessing Buffer Routine
Terminal Editor
Text Storage Program
Tic-Tac-Toe
Time Sharing Communications
TIMIT – Interrupt Driven Real Time Clock Routine
T.I. Silent 700 Interface – Intellec MDS
TRACE – Program Trace and Debugger
Trace Routine
TTY Binary Dump Routine
TTY Binary Load Routine
Type

Quicksort Procedures

Video Driver

Word Game, The

insite™

PARTIAL PROGRAM INDEX – 4-BIT USER'S LIBRARY

TITLE
Cross Assembler on PDP-8
Cross Assembler for NOVA Computer
BNPF Tape Generator for PDP-8
MCS-4 Simulator for PDP-8
MCS–40 Cross Assembler (Intellec® 8/MOD 80)
Intel MCS-40 Cross Assembler and Text Editor (Computer Autonation 16/Alpha-LSI)
A Chebyshev Approximation Package
Parity Checker/Generator (8-Bit)
Parity Generator, ASCII Character
Code Conversion: ASCII to EBCDIC
Delay Subroutines
Bit Manipulation Routine
Universal Logic Subroutines (AND, OR, XOR, XOR)
8-Bit Parity Check Annex
Binary to BCD Converter
Data Compare
Paper Tape Edit

TITLE
IOMEC SERIES THREE (S-3) Cartridge Interface
I/O Test
Bowmar TP 3100 Printer Routine
8-Digit Register Diaplsy
Intellec® 4/MOD 40 – Silent 700 Interface
PROM Dump Utility Program
PRO FORMA
Peripheral Interface Routine for a Thermal Strip Printer
MCS-4/4- Disassembler
Right Justified HEX Data Shifter
Floating Point Arithmetic Subroutine Package
HEXBCD
Fast Binary Multiply: Selectable Bit Precision and Constant Execute Time
Fast Decimal Multiplication Routine
Automatic Digital Integration
Multiply/Divide 8 Decimal Numbers
Binary to BCD Converter

insite™ INTEL® USER'S LIBRARY SUBMITTAL FORM

☐ 4004 ☐ 4040 ☐ 8008 ☐ 8080 ☐ 3000 ☐ Other_____ (use additional sheets if necessary)

Program Title

Function

Required Hardware

Required Software

Input Parameters

Output Results

Registers Modified:	Programmer:
RAM Required:	Company:
ROM Required:	Address:
Maximum Subroutine Nesting Level:	City:
Assembler/Compiler Used:	State:

CROMIS SERIES 3000
CROSS MICROPROGRAMMING SYSTEM

Built-in Series 3000 fields and mnemonics

User definable fields and mnemonics

Hierarchical field defaults

Free field statement format

String macro capability

Extended address generation

Graphical microprogram memory display

Symbolic label reference directory

MCU jump address validation

RAM/ROM/PROM programming file generation

The Intel® Series 3000 Cross Microprogramming System (CROMIS) is an advanced software system that supports the generation of microprograms for custom Series 3000 processor and controller micro-architecture. It provides extensive programming facilities that greatly reduce the time and effort required to develop, debug, and document a microprogram.

CROMIS is designed for use on almost any modern computing system with high-speed I/O and on-line file facilities. It is available in ANSI (standard) FORTRAN IV source form for user illustration or may be immediately accessed on any of several major time-sharing services throughout the world. To insure the long-term reliability and maintainability of CROMIS, all component programs are written in a highly modular, structured programming style with extensive operational documentation.

SPECIFICATIONS

XMAS CAPABILITIES

Translates all 3001 MCU and 3002 CPE mnemonics.

Dynamically allocates storage for labels, values and strings in a user expandable data area.

Accepts microinstruction format definitions of up to 64 total bits.

Provides extended address generation for up to 16K microinstructions.

Includes a 4-level user definable field default mechanism.

XMAP CAPABILITIES

Provides direct or inverted mapping for any bit in any microinstruction field.

Permits explicit 1's or 0's to be specified for unused bit locations.

Generates standard BNPF or hexadecimal programming files.

Accepts memory configuration defintiions from 1 X 1 bits to 16K X 16 bits.;

OPERATIONAL ENVIRONMENT

Required Hardware:

16-bit or larger word size

5 rewindable data files (disc or tapes)

Required Software:

ANSI standard FORTRAN IV compiler

TAPE CONTENTS

TAPE 1

Part 1 of XMAS FORTRAN IV Source

TAPE 2

Part 2 of XMAS FORTRAN IV Source
XMAS Sample Program
XMAP FORTRAN IV Source
XMAP Sample Program
MERGE File Editing Program

SHIPPING MEDIA

Two 2400-foot magnetic tapes.

TAPE FORMAT

9-track	800 bpi
80 byte	unblocked
EBCDIC	unlabeled

DOCUMENTATION

CROMIS Reference Specification
XMAS/XMAP Message Summary
XMAS Installation Guide
(preamble to XMAS FORTRAN IV source)
XMAP Installation Guide
(preamble to XMAP FORTRAN IV source)

```
                    /* 10.2 USEC UNSIGNED 16-BIT INTEGER MULTIPLY
                       ASSUMPTIONS: MULTIPLICAND IS IN PAIR OF 3212'S
                                    BUFFERING M-BUS;
                    */

                    /* CONVENIENT STRING DEFINITIONS */
                    COUNT    STRING 'R8' ; /* LOOP COUNT IN R8 */
                    P.P      STRING 'AC' ; /* PARTIAL PRODUCT IN AC */
                    M.PLIER STRING 'T' ; /* MULTIPLIER IN T */
                    ANDK     STRING 'TZR' ; /* PSEUDO OP AND */

                    /* CONVENIENT IMPLY DEFINITIONS */
                    INR IMPLY FO = 11B ; /* INR IMPLIES INCREMENT */
                    SDR IMPLY FO = 11B ; /* SDR IMPLIES STORE ONLY */

                    /* MASK FIELD DEFINITION */
                    MASK FIELD LENGTH = 2
                              MICROPS( KFFF0 = 10B ) ;  MASK KBUS ;

                    /* INITIALIZE LOOP COUNTER */
90H:                CSR(COUNT) ; /* SET COUNT REG TO ALL 1'S */
91H:                ANDK(COUNT) KFFF0 ; /* FORCE COUNT REG TO -16 */

94H:                CLR(P.P) ; /* CLEAR PARTIAL PRODUCT */
95H:                SRA(M.PLIER) ; /* PLACE LSB OF M'PLIER ON FI LINE */

                    /* MAIN MULTIPLY LOOP */
92H: MPYLOOP:
                    INR(COUNT) /* INCREMENT LOOP COUNT */
                       JFL(ONE, ZERO) /* BRANCH ON M'PLIER BIT */
                          SIZ ; /* SAVE CARRY FOR LOOP EXIT TEST */
0A3H: ONE:             AMA(P.P) ; /* ADD MULTIPLICAND TO PARTIAL PRODUCT */
0A2H:                  SPA(P.P) STZ ; /* SAVE LSB OF PARTIAL PRODUCT IN Z */
0A4H: ZERO:            SRA(M.PLIER) FFZ /* SHIFT & LINK IN P-P BIT FROM Z */
                    JZF( MPYLOOP, EXIT ) ; /*TEST OLD CARRY FOR LOOP EXIT */

 93H: EXIT:         NOP(FO) JMP(EXIT) ;

EOF
```

MCS-40 CROSS ASSEMBLER

Accepts all 4004 and 4040 instructions

Conditional assembly capability

Full macro facility

Hexadecimal or BNPF object code formats

Written in ANSI standard FORTRAN IV

Comprehensive user documentation

Instantly available on worldwide timesharing services

The MCS-40 Cross Assembler, MAC40, is a powerful program development tool for Intel's® 4-bit microcomputers, the 4004 and the new 4040. MAC40 provides extensive capabilities which reduce the time and effort involved in program development, debug and documentation. The cross assembler allows usage of the high speed I/O and text editing capability of a large computer system to further shorten the programming task.

MAC40 translates 4004/4040 machine assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions, or to move the program to another memory location. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits MAC40 to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

Output from MAC40 may be punched to paper tape in hex format for loading into an Intellec® 4 Development System or may be punched in BNPF format to program ROMs.

MAC40 is written in ANSI standard FORTRAN IV and is designed to run on most large scale computing systems with a 32-bit or larger integer format (word size). It is also available for immediate use on several major timesharing services throughout the world.

SPECIFICATIONS

CAPABILITIES:

Accepts all 66 instruction mnemonics plus 10 pseudo-operators.

Allows up to 499 labels in standard configuration; easily expandable.

Allows a total of up to 9 levels of nested conditional assembly and nested macro-calls.

User definable I/O formats.

Batch or interactive mode.

OPERATIONAL ENVIRONMENT:

Hardware required

32-bit or larger word size

12–16K words depending on machine

Software required

ANSI standard FORTRAN IV compiler

SHIPPING MEDIA:

Magnetic tape

TAPE FORMAT:

9 Track	80 Byte unblocked
EBCDIC	records
800 BPI	Unlabeled

TAPE CONTENTS:

MCS-40™ Cross Assembler (FORTRAN IV Source)

MERGE Source File Editing Program (FORTRAN IV Source)

XCNV4 Conversion Program (FORTRAN IV Source)

DOCUMENTATION PACKAGE INCLUDES:

4004/4040 Assembly Language Programming Manual

MAC4 External Reference Specification

Pocket Reference Card

4004/4040 SIMULATOR

Simulates all 4004/4040 machine instructions

Accepts output from MAC40, the Intel® 4004/4040 Cross Assembler

Contains extensive symbolic debugging capabilities

Written in ANSI standard FORTRAN IV

Instantly available on worldwide timesharing services

COMMAND CAPABILITIES:

Set breakpoints

Trace program execution

Dump and modify memory

Examine and modify registers

Examine and set I/O ports

Simulate the 4040 hardware interrupt

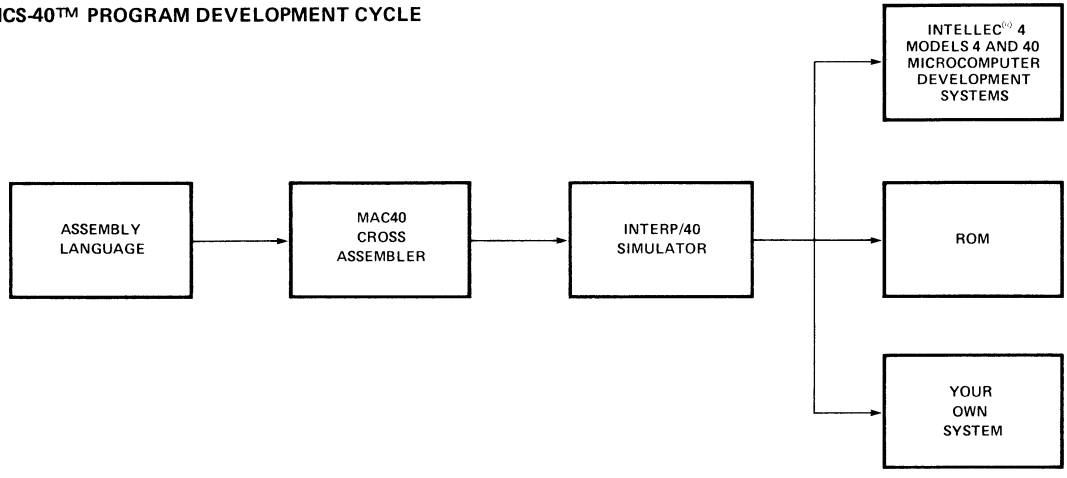
Measure program execution time

The 4004/4040 Simulator, INTERP/40, is a complete simulation and debug program for the Intel® 4004 and 4040 microcomputers. Programs can be run, displayed, stopped, and altered allowing step by step refinement without continuous reassembly of the source program. INTERP/40 provides powerful commands to control the execution of 4004 and 4040 programs. Extensive debug features are built in to help reduce the time and cost involved in program checkout.

INTERP/40 also provides symbolic reference to storage locations and operation codes as well as numeric reference in various number bases.

INTERP/40 is written in FORTRAN IV and is designed to run on most large scale computer systems with a 32-bit or larger integer format (word size). It is also available for immediate use on major timesharing services throughout the world.

MCS-40™ PROGRAM DEVELOPMENT CYCLE



SPECIFICATIONS

CAPABILITIES:

Provides total software simulation of the Intel® 4004 and 4040 CPU's.

Can be run in batch or interactive mode.

OPERATIONAL ENVIRONMENT:

Hardware required

32-bit or larger word size

12-15K words of memory, depending on machine

Software required

FORTRAN IV compiler

SHIPPING MEDIA:

Magnetic tape

TAPE FORMAT:

9-track	80-byte unblocked
EBCDIC	records
800BPI	Unlabeled

TAPE CONTENTS:

4004/4040 Simulator
(FORTRAN IV Source)
MERGE Source File Editing Program
(FORTRAN IV Source)

DOCUMENTATION PACKAGE:

INTERP/40 External Reference Specification

SOFTWARE AND TRAINING

MCS-8™ CROSS ASSEMBLER

Accepts all 8008 instructions

Conditional assembly capability

Full macro facility

Hexadecimal or BNPF object code formats

Written in ANSI standard FORTRAN IV

Comprehensive user documentation

Instantly available on worldwide timesharing services

The MCS-8™ Cross Assembler, MAC8, is a powerful program development tool for Intel's® 8008 microcomputer. MAC8 provides extensive capabilities which reduce the time and effort involved in program development, debug and documentation. The cross assembler allows usage of the high speed I/O and text editing capability of a large computer system to further shorten the programming task.

MAC8 translates symbolic 8008 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions, or to move the program to another memory location. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits MAC8 to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

Output from MAC8 may be loaded directly to the 8008 Simulator (INTERP/8) for interactive, symbolic debugging or may be punched to paper tape in hex format for loading into an Intellec® 8/Mod 8 Development System. It may also be punched in BNPF format to program ROMs.

MAC8 is written in ANSI standard FORTRAN IV and is designed to run on most large scale computing systems with a 32-bit or larger integer format (word size). It is also available for immediate use on several major timesharing services throughout the world.

MCS-8™ ASSEMBLY LANGUAGE PROGRAMMING EXAMPLE:

```
                                ; UMUL – UNSIGNED INTEGER MULTIPLY
                                ; CALL:  ARGUMENTS IN C & D
                                ; EXIT:  HI ORDER PRODUCT IN B
                                ;        LO ORDER PRODUCT IN C
                                ; REGS:  A,B,E AND FLAGS EXCEPT CARRY ALTERED
001E                            UMUL:
001E  0E00                              MVI B,0
0020  2609                              MVI E,9
0022                            UMUL0:
0022  C2                               MOV A,C          ; ROTATE CARRY INTO
0023  1A                               RAR              ; PRODUCT – MULTIPLIER
0024  D0                               MOV C,A          ;  SHARED REGUSTER
0025  21                               DCR E            ;    FORCING NEXT LSB
0026  2B                               RZ               ;      INTO CARRY
0027  C1                               MOV A,B          ; EXIT IF 8TH ITERATION
0028  402C00                           JNC UMUL1        ; IF CARRY SET
002B  83                               ADD D            ; ADD MULTIPLICAND TO
002C                            UMUL1:                  ; PRODUCT
002C  1A                               RAR
002D  C8                               MOV B,A          ; ROTATE MOST SIGNIFICANT
002E  442200                           JMP UMUL0        ;  PRODUCT AND REPEAT LOOP
```

SPECIFICATIONS

CAPABILITIES:

Accepts all 48 instruction mnemonics plus 10 pseudo-operators.

Allows up to 499 labels in standard configuration; easily expandable.

Allows total of up to 9 levels of nested conditional assembly and nested macro-calls.

User definable I/O formats.

Batch or interactive mode.

OPERATIONAL ENVIRONMENT:

Hardware required

- 32-bit or larger word size
- 12–16K words depending on machine

Software required

- ANSI standard FORTRAN IV compiler

SHIPPING MEDIA:

Magnetic tape

TAPE FORMAT:

9 Track	80 Byte unblocked
EBCDIC	records
800 BPI	Unlabeled

TAPE CONTENTS:

MCS-8™ Cross Assembler (FORTRAN IV Source)

MERGE Source File Editing Program (FORTRAN IV Source)

CONV8 Conversion Program (FORTRAN IV Source)

DOCUMENTATION PACKAGE INCLUDES:

8008 Assembly Language Programming Manual

MAC8 External Reference Specification

Pocket Reference Card

8008 SIMULATOR

Simulates all 8008 machine instructions

Accepts output from PL/M compiler or MAC8 cross assembler

Comprehensive debug features

Written in FORTRAN IV

Instantly available on worldwide timesharing services

Comprehensive user documentation

The 8008 Simulator, INTERP/8, is a complete simulation and debug program for the Intel® 8008 microcomputer. INTERP/8 provides powerful commands to control the execution of 8008 programs. Extensive debug features are built-in to help reduce the time and cost involved in program checkout.

INTERP/8 simulates execution of all 8008 machine instructions. Programs either compiled on the PL/M compiler or assembled on the MAC8 Cross Assembler may be loaded directly into INTERP/8 for simulation and checkout.

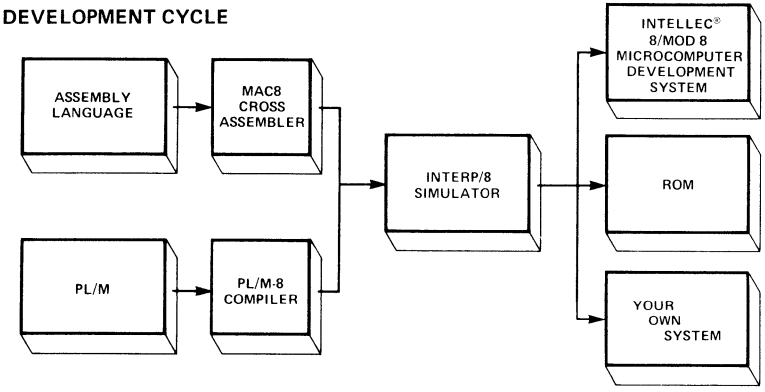
INTERP/8 provides commands to:

- Set Breakpoints
- Trace Program Execution
- Dump and Modify Memory
- Examine and Modify Registers
- Measure Program Timing
- Examine and Set I/O Ports
- Perform Interrupts and Stack Manipulations
- Perform Address Arithmetic

INTERP/8 also provides symbolic debugging capability. Memory locations may be referenced by their symbolic names, either through labels or variable names. This eliminates the need to know the specific absolute address of each variable or label.

INTERP/8 is written in FORTRAN IV and is designed to run on most large-scale computer systems with a 32-bit or larger integer format (word size). It is also available for immediate use on several major timesharing services throughout the world.

MCS-8™ PROGRAM DEVELOPMENT CYCLE



SPECIFICATIONS

CAPABILITIES:
Simulates all 48 machine instructions

Allows full 16K program

Can be run in batch or interactive mode

OPERATIONAL ENVIRONMENT:
Hardware required
32-bit or larger word size
15—20K words of memory, depending on machine
Software required
FORTRAN IV compiler

SHIPPING MEDIA:
Magnetic tape

TAPE FORMAT:

9-track	80-byte unblocked
EBCDIC	records
800 BPI	Unlabeled

TAPE CONTENTS:
8008 Simulator
(FORTRAN IV Source)
MERGE Source File Editing Program
(FORTRAN IV Source)

DOCUMENTATION PACKAGE:
INTERP/8 User's Manual
INTERP/8 Installation Guide

MCS-80™ CROSS ASSEMBLER

Accepts all 8080 instructions

Conditional assembly capability

Full macro facility

Hexadecimal or BNPF object code formats

Written in ANSI standard FORTRAN IV

Comprehensive user documentation

Instantly available on worldwide timesharing services

The MCS-80 Cross Assembler, MAC80, is a powerful program development tool for Intel's® 8080 microcomputer. MAC80 provides extensive capabilities which reduce the time and effort involved in program development, debug and documentation. The cross assembler allows usage of the high speed I/O and text editing capability of a large computer system to further shorten the programming task.

MAC80 translates symbolic 8080 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions, or to move the program to another memory location. Full macro capability eliminates the need to rewrite similar sections of code repeatedly and simplifies program documentation. Conditional assembly permits MAC80 to include or delete sections of code which may vary from system to system, such as the code required to handle optional external devices.

Output from MAC80 may be loaded directly to the 8080 Simulator (INTERP/80) for interactive, symbolic debugging or may be punched to paper tape in hex format for loading into an Intellec® MDS Microcomputer Development System. It may also be punched in BNPF format to program ROMs.

MAC80 is written in ANSI standard FORTRAN IV and is designed to run on most large scale computing systems with a 32-bit or larger integer format (word size). It is also available for immediate use on several major timesharing services throughout the world.

MCS-80™ ASSEMBLY LANGUAGE PROGRAMMING EXAMPLE:

```
                        ;       THIS SUBROUTINE PERFORMS DECIMAL ADDITION
                        ;       FOR 16 DECIMAL DIGITS ON THE INTEL 8080
                        ;       MICROCOMPUTER.
                        ;
                        ;       THE ADDRESS OF THE FIRST OPERAND IS EXPECTED TO BE IN THE
                        ;       D AND E REGISTERS AND THE ADDRESS OF THE
                        ;       SECOND OPERAND SHOULD BE IN THE H AND L
                        ;       REGISTERS.  THE RESULT IS STORED OVER THE
                        ;       FIRST OPERAND.  THE ADDITION IS DONE TWO DIGITS
                        ;       AT A TIME.
                        ;
0000                    DECAD:
0000    0E08                    MVI C,8         ; INITIALIZE DIGIT COUNTER (HALF)
0002    AF                      XRA A           ; CLEAR CARRY BIT
0003                    LOOP:
0003    1A                      LDAX D          ; LOAD TWO DIGITS FROM FIRST OPERAND
0004    8E                      ADC M           ; ADD TWO DIGITS FROM SECOND OPERAND WITH CARRY
0005    27                      DAA             ; DECIMAL ADJUST RESULT
0006    12                      STAX D          ; STORE TWO DIGITS OF RESULTS OVER FIRST OPERAND
0007    23                      INX H           ; INCREMENT ADDRESS OF SECOND OPERAND
0008    13                      INX D           ; INCREMENT ADDRESS OF FIRST OPERAND
0009    0D                      DCR C           ; DECREMENT DIGIT COUNT
000A    C20300                  JNZ LOOP        ; CONTINUE IF MORE DIGITS LEFT
000D    C9                      RET
```

8080 SIMULATOR

Simulates all 8080 machine instructions

Accepts output from PL/M compiler or MAC80 Cross Assembler

Comprehensive debug features

Written in FORTRAN IV

Instantly available on worldwide timesharing services

Comprehensive user documentation

The 8080 Simulator, INTERP/80™, is a complete simulation and debug program for the Intel® 8080 microcomputer. INTERP/80 provides powerful commands to control the execution of 8080 programs. Extensive debug features are built in to help reduce the time and cost involved in program checkout.

INTERP/80 simulates execution of all 8080 machine instructions. Programs either compiled on the PL/M compiler or assembled on the MAC80 Cross Assembler may be loaded directly into INTERP/80 for simulation and checkout.

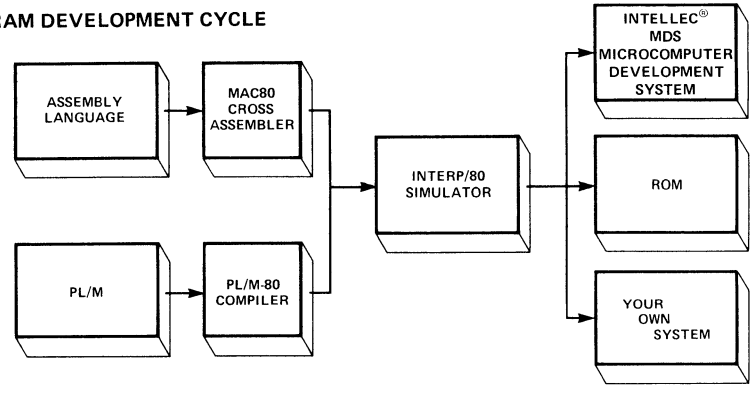
INTERP/80 provides commands to:

- Set Breakpoints
- Trace Program Execution
- Dump and Modify Memory
- Examine and Modify Registers
- Measure Program Timing
- Examine and Set I/O Ports
- Perform Interrupts and Stack Manipulations
- Perform Address Arithmetic

INTERP/80 also provides symbolic debugging capability. Memory locations may be referenced by their symbolic names, either through labels or variable names. This eliminates the need to know the specific absolute address of each variable or label.

INTERP/80 is written in FORTRAN IV and is designed to run on most large-scale computer systems with a 32-bit or larger integer format (word size). It is also available for immediate use on several major timesharing services throughout the world.

MCS-80™ PROGRAM DEVELOPMENT CYCLE



SPECIFICATIONS

CAPABILITIES:
Simulates all 78 machine instructions

Allows 16K program, easily expandable

Can be run in batch or interactive mode

OPERATIONAL ENVIRONMENT:
Hardware required
32-bit or larger word size
15–20K words of memory, depending on machine
Software required
FORTRAN IV compiler

SHIPPING MEDIA:
Magnetic tape

TAPE FORMAT:

9-track	80-byte unblocked
EBCDIC	records
800 BPI	Unlabeled

TAPE CONTENTS:
8080 Simulator
(FORTRAN IV Source)
MERGE Source File Editing Program
(FORTRAN IV Source)

DOCUMENTATION PACKAGE:
INTERP/80 User's Manual
INTERP/80 Installation Guide

SOFTWARE AND TRAINING

PL/M HIGH LEVEL PROGRAMMING LANGUAGE MCS-8™ AND MCS-80™ CROSS COMPILERS

Reduces program development time and cost

Improves product reliability and eases maintenance

Available for 8008 and 8080

Comprehensive user documentation

Hexadecimal or BNPF object code formats

Written in ANSI standard FORTRAN IV

Instantly available on worldwise timesharing services

PL/M is a high-level system programming language, specifically designed to ease the programming task for INTEL's 8-bit microcomputers, the 8008 and the 8080. PL/M is a powerful tool, well suited to the requirements of the microcomputer system designer and implementor. The language has been designed to facilitate the use of modern techniques in structured programming. These techniques can lead to rapid system development and checkout, straightforward maintenance and modification, and high product reliability.

The PL/M compilers convert a free-form symbolic PL/M program into an equivalent 8008 or 8080 object program. The compilers themselves take care of all the details of machine or assembly language programming, which permits the programmer to concentrate entirely on effective software design, and the logical requirements of his system.

Output from the PL/M compiler may be loaded directly into the 8008 or 8080 simulator programs for interactive, symbolic debugging or may be punched to paper tape in hex format for loading into an Intellec® Microcomputer Development System. It may also be punched in BNPF format to program ROMs.

The PL/M compilers are written in ANSI standard FORTRAN IV and are designed to run on any large-scale computer system with a minimum 32-bit integer format (word size). They are also available for immediate use on several worldwide timesharing systems.

PL/M PROGRAMMING EXAMPLE:

```
                                /*  BUBBLE SORT DECLARATION  */
SORT: PROCEDURE (N) ADDRESS;
    /*    N = LENGTH OF A
          COUNT = NR. OF SWITCHES PERFORMED TO-DATE
          SWITCHED = (BOOLEAN) HAVE WE DONE ANY SWITCHING YET ON THIS SCAN?  */
    DECLARE (N, I, SWITCHED) BYTE,
          (TEMP, COUNT) ADDRESS;
    SWITCHED = 1;              /*  SWITCHED = TRUE MEANS NOT DONE YET  */
    COUNT = 0;
    DO WHILE SWITCHED;
          SWITCHED = 0;        /*  BEGIN NEXT SCAN OF A  */
          DO I = 0 TO N-2;
                IF A(I) > A(I+1) THEN
                      DO;                  /*  FOUND A PAIR OUT OF ORDER  */
                      COUNT = COUNT + 1;
                      SWITCHED = 1;        /*  SET SWITCHED = TRUE  */
                      TEMP = A(I);         /*  SWITCH THEM INTO ORDER  */
                      A(I) = A(I+1);
                      A(I+1) = TEMP;
                      END;
          END;
          /*  HAVE NOW COMPLETED A SCAN  */
    END  /*  WHILE  */;
    /*  HAVE NOW COMPLETED A SCAN WITH NO SWITCHING  */
    RETURN COUNT;
END SORT;
```

SPECIFICATIONS

OPERATING ENVIRONMENT:
Required hardware
32-bit or larger word size
20–25K words of memory, depending on machine
Required software
ANSI standard FORTRAN IV compiler

SHIPPING MEDIA:
Magnetic tape

TAPE FORMAT:
9-track EBCDIC
800 BPI 80-byte unblocked records
Unlabeled

DOCUMENTATION PACKAGE:
8008 and 8080 PL/M Programming Manual
8008 (or 8080) PL/M Compiler Operator's Manual

TAPE CONTENTS:
PLM Pass 1 (FORTRAN IV Source)
PLM Pass 2 (FORTRAN IV Source)
MERGE Source File Editing Program (FORTRAN IV Source)
Sample Test Program (PL/M Source)

MICROCOMPUTER TRAINING

MICROCOMPUTER TRAINING

Courses presented at training centers and customer facilities.

Training Centers
- **Boston**
- **Chicago**
- **Santa Clara**

Scheduled on a continuing basis throughout the year.

System demonstrations

On-site courses tuned to customer requirements.

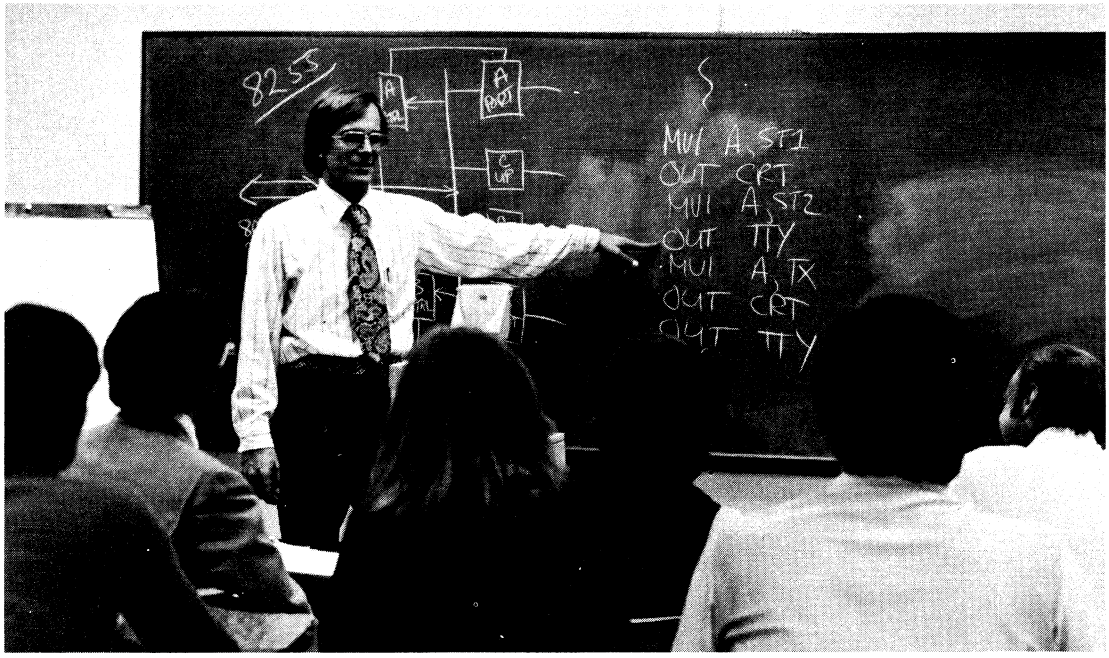
Hands-on laboratory sessions reinforce lecture.

Training center classes limited to 12 attendees.

Intellec® Microcomputer Development Systems with ICE-80 in laboratory.

Microcomputers are being used in hundreds of applications from simple controllers to complex data processing systems. To enable users to bring microcomputers into their applications, Intel offers a selection of workshops that are designed to provide you with the "tools" for making optimum use of Intel microcomputers in system development. The coure prerequisites are a knowledge of binary and hexadecimal number systems and basic logic functions. To attain maximum benefit from course presentation, some background in logic design and computer programming is recommended.

REGISTRATION AND ADDITIONAL INFORMATION: Contact MCD Training at Intel Corporation, Santa Clara, California 95051, (408) 246-7501, or your local Intel sales office.



MCS-80™ SYSTEM WORKSHOP

This workshop will prepare the student to design and develop a system using the Intel® 8080 microprocessor through the use of lecture, demonstration and laboratory "hands-on" experience with the Intellec® MDS development system and ICE-80.

COURSE OUTLINE:

DAY 1

Introduction
a. Microprocessor System
   1. Function
   2. Organization
   3. Programming
b. 8080 Overview
   1. Functional sections
   2. Programming model
   3. Execution Sequence

Assembly Language Instructions
a. Input/Output
b. Register/Memory Reference
c. Arithmetic
d. Logical
e. Rotates

Development System
a. Function
b. System Monitor
c. Paper Tape System
d. Disc Operating System

Macro Assembler and Text Editor
a. Function
b. Operation

System Demonstration

Laboratory
Using the System Monitor, Text Editor, and Macro Assembler

DAY 2

System Timing
a. Instructions
b. State transition
c. Signal relationships
d. Specifications

Subroutines
a. Invocation
b. Stack memory
c. Parameters

Programmed Input/Output
a. Status Request
b. Command
c. Data Transfer

Interrupt System
a. Description
b. RST instruction
c. Service subroutines

Laboratory
a. Using the Disc Operating System
b. Program assembly and execution

DAY 3

Branch Tables
a. Application
b. Construction

Direct Load/Store Instructions

Special Purpose Instructions

Macros
a. Definition
b. Reference
c. Expansion

Programming Examples from the System Monitor

Debugging with the System Monitor
a. Breakpoints
b. Examine registers

Basic System Hardware
a. Bus Structure
b. CPU Set
c. Memory
d. Input/Output

Laboratory
a. Software Debug
b. PROM Programming

DAY 4

System Design Based on SBC 80/10
System Specifications

CPU Section
a. Bus structure
b. System clocks
c. Interrupt structure

Memory Section
a. Memory map
b. PROM/ROM
c. RAM
d. Address decoding
e. Control signals

Parallel Input/Output
a. 8255 Operation
b. Printer interface
c. Reader/punch interface
d. A/D and D/A interface
e. Keyboard/display interface
f. Control line generation

Serial I/O
a. 8251 Operation
b. TTY interface
c. Modem interface

Laboratory
Program assembly and execution

DAY 5

Expansion of System Resources

Complete Design Example of Temperature Monitor System
a. System block diagram
b. I/O interface schematic
c. Software

ICE-80 Emulator
a. Definition
b. System Overview
   1. Memory and I/O sharing
   2. Breakpoint capability
   3. Dynamic tracing
   4. Control block

ICE-80 Software Driver
a. Modes
b. Commands

System Debugging Example

System Demonstration

Laboratory
a. Using ICE-80 commands
b. Debugging

PL/M-80 LANGUAGE WORKSHOP

This workshop will prepare the student for writing and debugging PL/M-80 programs using lecture, demonstration, and laboratory "hands-on" experience with the Intellec® Microcomputer Development System and ICE-80.

COURSE OUTLINE:

DAY 1

Introduction
a. Preview of Course
b. Overview of PL/M, Linking and Relocation
c. Why use a High Level Language

Definitions
a. Symbols
b. Identifiers
c. Reserved Words
d. Comments
e. Data Elements
f. Expressions
g. Statements
h. Declarations

Data Elements
a. Variables
b. Subscripted Variables
c. Data Type
d. Constants

Operators, Operations and Priorities
a. Arithmetic
b. Boolean

Evaluating Expressions

Statements
a. Redefine
b. Basic
c. Conditional

Assignment
a. Implement a Given Algorithm in PL/M (as a class)

DAY 2

ISIS-II Disc Operating System
a. Components of System

ISIS-II File Structure
a. System Files
b. User Files
c. Device Files
d. Directory and File Attributes

ISIS-II Commands
a. CUSPS – Commonly Used System Programs
b. Directory and Attribute Commands
c. Rename and Delete Commands
d. Creating System and User Discs

ISIS-II Editor
a. Definition of Terminology
b. Invoking the Editor
c. Editor Commands
d. Editing Existing Files

ISIS-II PL/M 80 Compiler
a. Invoking PL/M
b. Compiler Options

ISIS-II Locate
a. Invoking Locate

Laboratory
a. Introduction to ISIS-II Disc Operating System
b. Creating a PL/M Source File
c. Compiling a PL/M Program
d. Locating and Executing a PL/M Program

DAY 3

Review

Procedures
a. Declaration
b. Invocation
c. Program Construction

Data References
a. Based Variables
b. Variable Equivalencing

Statement Labels

Unconditional Transfers

Blocks
a. Concept and Use
b. Scope of Declarations
   1. Global and local
   2. Nested and parallel blocks
   3. Public and external attributes
c. Modular Compilation
d. Modular Program

ISIS-II Link
a. Invoking Link
b. Link Options
c. Assembly Object Modules

Laboratory
a. Compile Program Modules
b. Link and Locate Modules
c. Execute Program

DAY 4

Review

ISIS-II Librarian
a. Creating a library
b. Managing a library
   1. Adding modules
   2. Deleting modules

ISIS-II System Interface
a. System Library

ICE-80 Emulator
a. Definition
b. System Overview
   1. Memory and I/O mapping
   2. Breakpoint capability
   3. Dynamic tracing
   4. Control block

ICE-80 Software Driver
a. Modes
b. Commands

System Debugging Examples

System Demonstration

Laboratory
a. Create a library
b. Link object to a library
c. Locate
d. Load and emulate using ICE-80

DAY 5

Review

Interrupt Procedures

Reentrant Procedures

Predeclared Procedures
a. TIME Procedure
b. MOVE Procedure
c. LENGTH, LAST and SIZE Procedures
d. Type Transfers
e. Shifts and Rotates

The Memory Array and STACKPTR Variables

Discussion of Selected Programs

Laboratory
a. Execution and Debugging of Selected Programs

MCS-48™ SYSTEM WORKSHOP

This workshop will prepare the student to design and develop a system using the Intel 8048 microprocessor through the use of lecture, demonstration and laboratory "hands-on" experience with the Intellec® Development System and PROMPT-48.

COURSE OUTLINE:

Day 1

Orientation

Introduction

a. Microprocessor System
   1. Function
   2. Organization
   3. Programming
b. 8048 Overview
   1. Functional Sections
   2. Programming Model
   3. Execution Sequence

Assembly Language Instructions

a. I/O Instructions
b. Data Move Instructions
c. Increment/Decrement Instructions
d. Branch Instructions
e. Worksession No. 1
f. Accumulator Group Instructions
   1. ADD/ADDC
   2. Logicals

PROMPT-48

a. Function
b. Operation

Laboratory Exercise

a. Program Entry and Execution using PROMPT-48

Day 2

Assembly Language Instructions

a. Accumulator Group Instructions
   1. Flags
   2. Rotates
b. Specials (XCH, DA, SWAP)
c. Worksession No. 2
d. Subroutines
   1. Invocation
   2. Stack Operation
e. Interrupt System
   1. Description
   2. Service Subroutines
   3. Multiple Source Systems

Development System

a. Function
b. Disk Operating System

Text Editor and Macro Assembler

a. Function
b. Operation

Laboratory Exercise

a. Bootstrap Procedures
b. Create, Edit and Assemble Source Program
c. Execute Program

Day 3

System Timing

a. Basic Timing and Timer
b. Bus Timing for Peripheral Devices

Peripherals and Design

a. Expanding Memory*
   1. Program Memory (1, 2K ROMs)
   2. Data Memory (RAMs)
b. Expanding Ports (8243)*
   1. Device Characteristics
   2. Software Control of Ports
c. Combination Chips*
   1. 8155 RAM and I/O Chip
   2. 8355,8755 ROM and I/O Chip
d. Peripheral Interfacing (Parallel)*
   1. 8255 Parallel I/O
   2. 8279 Keyboard and Display Interface
      —Keyboard Scanning Techniques
      —Display Refresh

Laboratory Exercise

a. Edit and Assemble Using DOS
b. Execute Using PROMPT-48

Day 4

Peripherals and Design

a. Peripheral Interfacing (Serial)*
   1. Transmission Formats
   2. Asynchronous Operation
   3. RS232C Interface
b. A/D and D/A Interfacing*
   1. Successive Approximation A/D
   2. A/D, D/A Chips
   3. A/D Design

Laboratory Exercises

a. Edit and Assemble Programs
b. Execute Programs

*Each section will consist of a design example including schematic, bus loading calculations, software and timing.

PROGRAMMABLE PERIPHERAL CIRCUITS WORKSHOP

This course will cover the Programmable Peripheral Circuits that are used in a wide variety of application areas such as process control, terminals, communications, numerical control, instrumentation, etc.

Each device is covered in sufficient depth to allow the attendee to define its hardware and software characteristics and evaluate its application areas.

COURSE OUTLINE:

Day 1

Introduction

a. Programmable Concept
   1. Initialization Commands
   2. Operation Commands
b. Addressing Methods
   1. Chip Selection
   2. Memory Mapping
   3. I/O Mapping

8253 Programmable Interval Timer

8257 Programmable DMA Controller

8259 Programmable Interrupt Controller

8279 Programmable Keyboard/Display Interface

a. Chip Descriptions and Applications
b. Programming Requirements
c. Design Examples

Day 2

8271 Programmable Floppy Disc Controller

8273 SDLC Protocol Controller

8275 Programmable CRT Controller

8155/8355/8755 Combination Memory and I/O Ports

a. Chip Descriptions and Applications
b. Programming Examples
c. Design Examples

SOFTWARE AND TRAINING

SERIES 3000 WORKSHOP

This workshop will provide the student with an in-depth understanding of the Series 3000 family through the use of lecture and demonstration. Microprogramming and design examples are presented.

COURSE OUTLINE:

DAY 1

Introduction

a. Introduction to Microprogramming
b. The Series 3000 Component Family
c. Series 3000 System Overview

CPU Design Example

a. CPU System Requirements
b. Architecture of a CPU
c. Developing a Macro-Instruction Set
d. Interrupt Handling
e. Microprogram Mapping

DAY 2

Design Techniques

a. Conditional Clocking
b. K-Bus
c. Micro-Instruction Field Extension
d. Micro-Subroutine
e. Pipelining
f. Timing Analysis

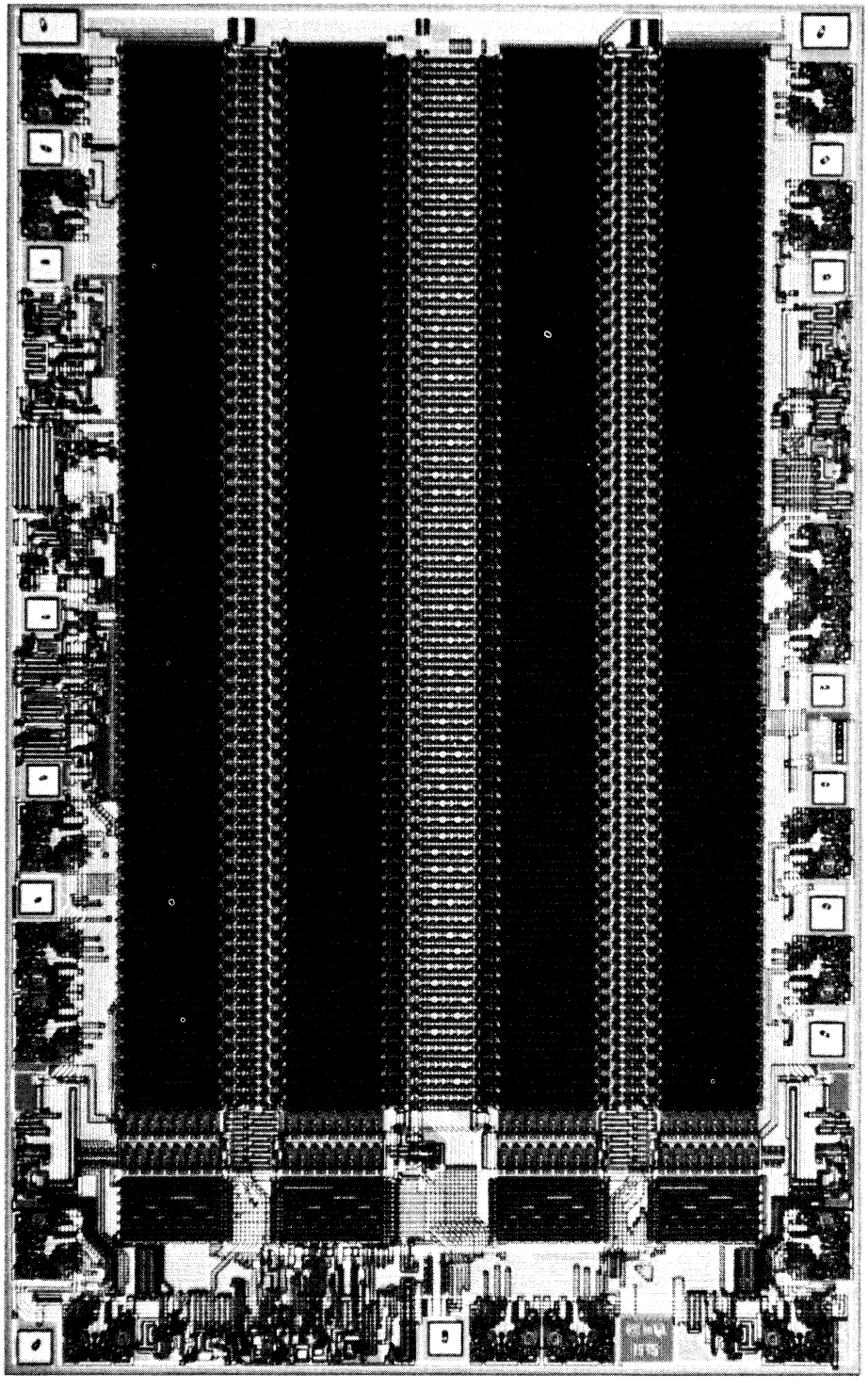
Controller Design Example

a. Disc Controller System Requirements
b. Architecture of a Disc Controller
c. Microprogram Implementation

DAY 3

Development Support

a. Introduction to CROMIS, the Series 3000 Cross Micro-Assembler
b. MDS-800 Microcomputer Development System
c. ICE-30 In-Circuit Emulator
d. ROM Simulator
e. Demonstration



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General Information

GENERAL INFORMATION

TABLE OF CONTENTS

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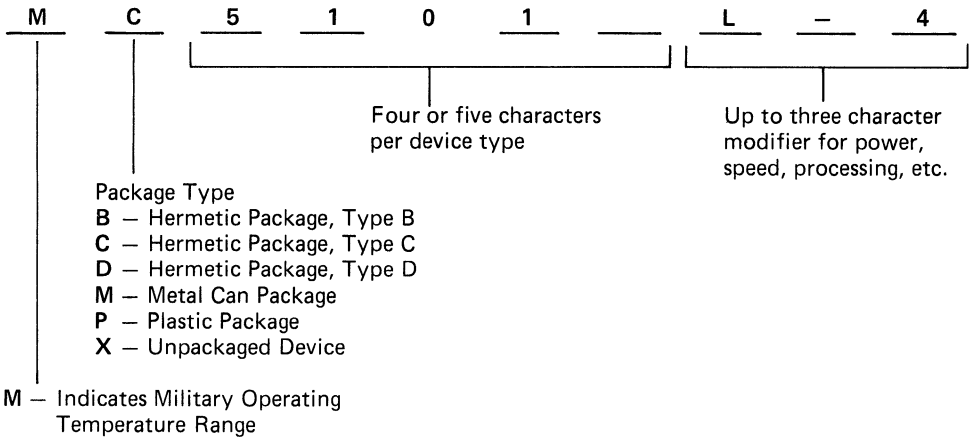

Examples:

P5101L CMOS 256 X 4 RAM, low power selection, plastic package, commercial temperature range.

C8080A2 8080A Microprocessor with 1.5 μs cycle time, hermetic package Type C, commercial temperature range.

MD3604/C 512 X 8 PROM, hermetic package Type D, military temperature range, MIL-STD-883 Level C processing.*

MC8080A/B 8080A Microprocessor, hermetic package Type C, military temperature range, MIL-STD-883 Level B processing.*

Kits, boards and systems may be ordered using the part number designations in this catalog.

The latest Intel OEM price book should be consulted for availability of various options. These may be obtained from your local Intel representative or by writing directly to Intel Corporation, 3065 Bowers Avenue, Santa Clara, CAlifornia 95051.

**On military temperature devices, B suffix indicates MIL-STD-883 Level B processing. Suffix C indicates MIL-STD-883 Level C processing. "S" number suffixes must be specified when entering any order for military temperature devices. All orders requesting source inspection will be rejected by Intel.*

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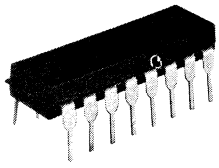

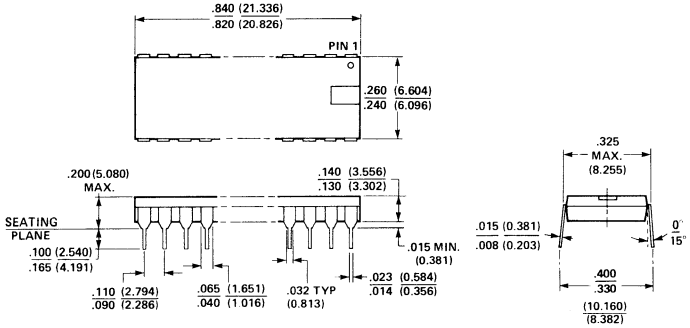

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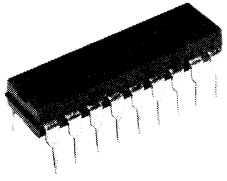

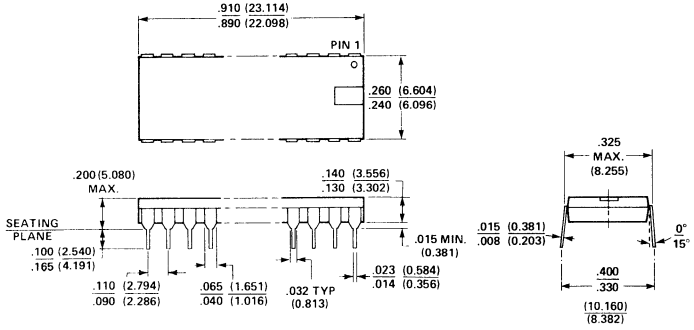

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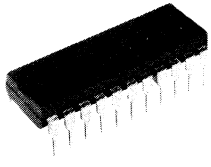

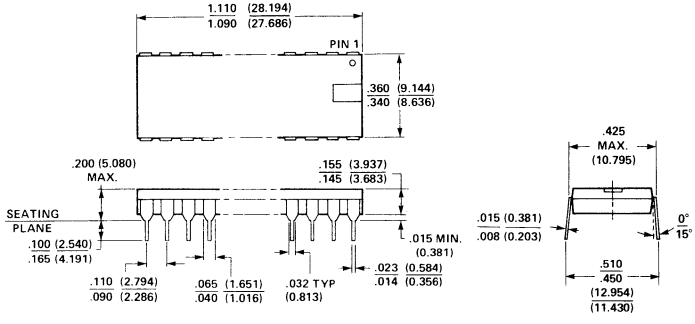

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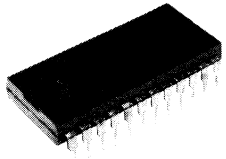

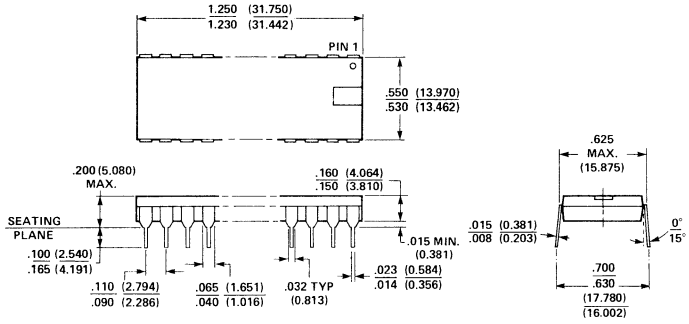

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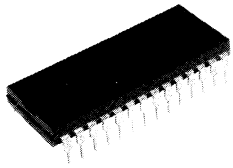

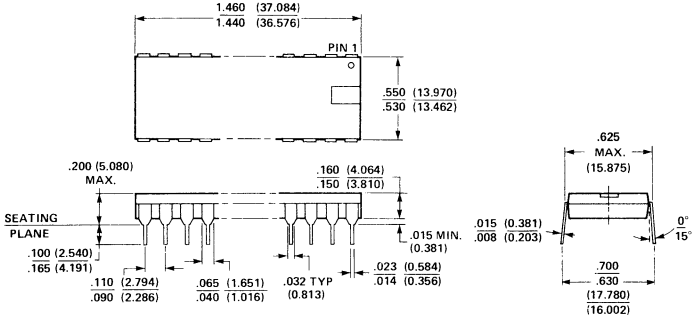

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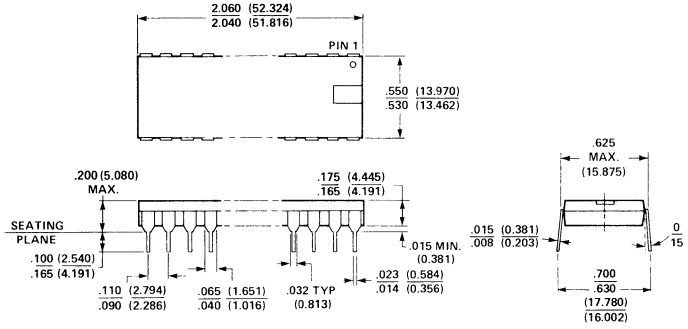

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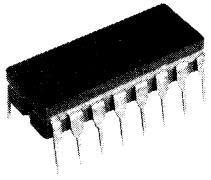

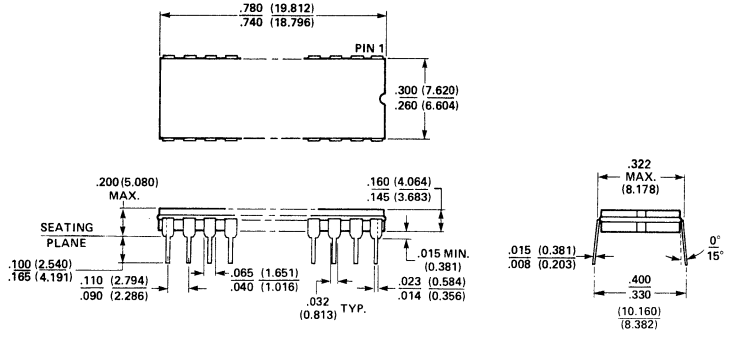

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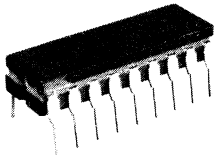

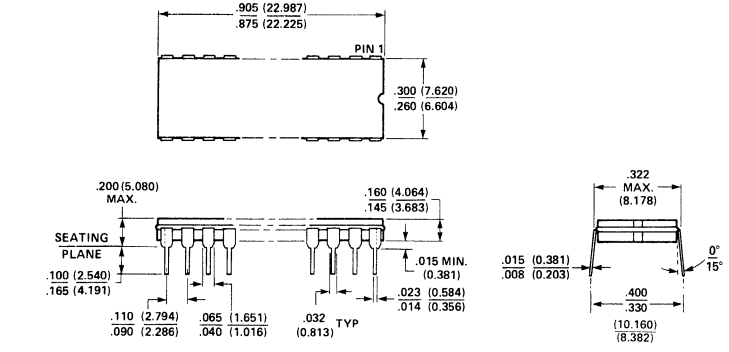

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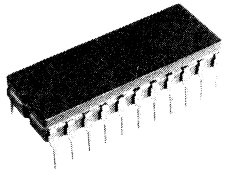

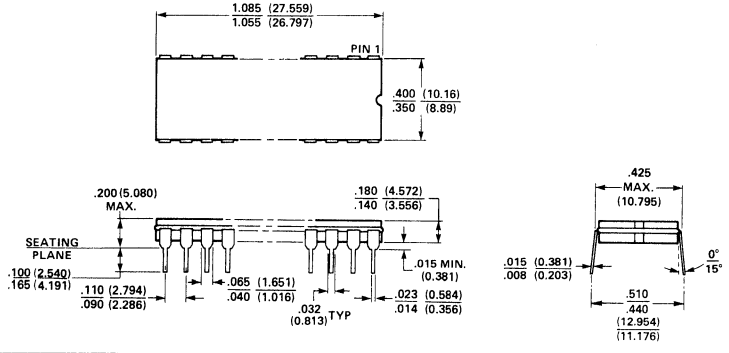

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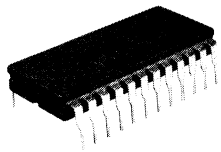

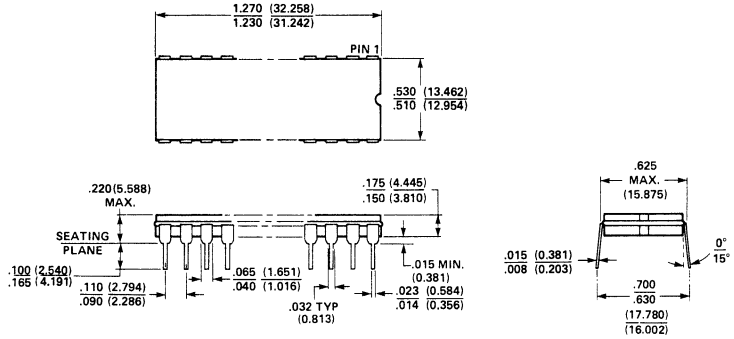

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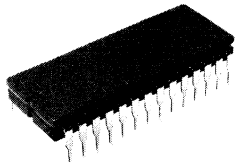

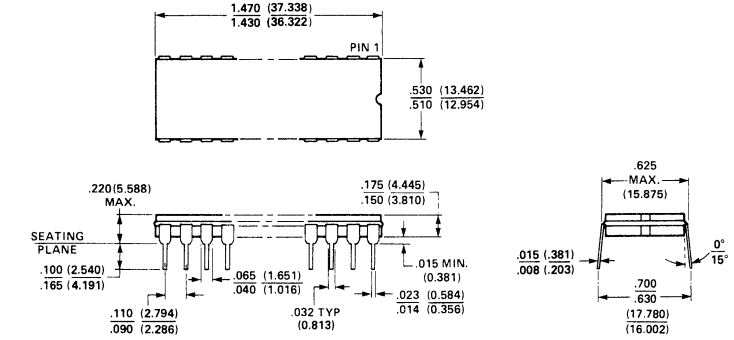

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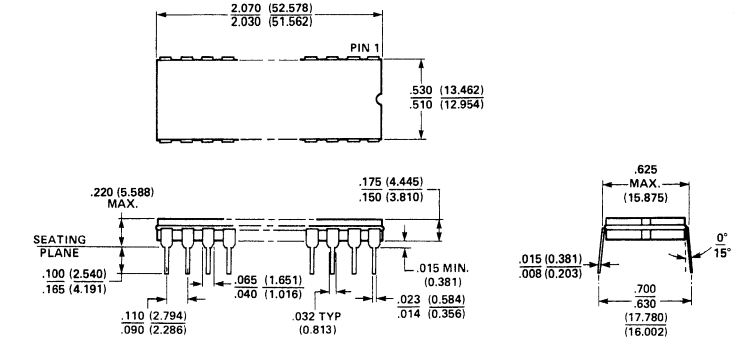

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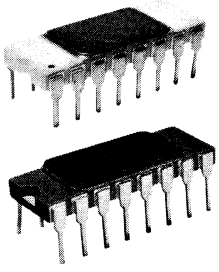

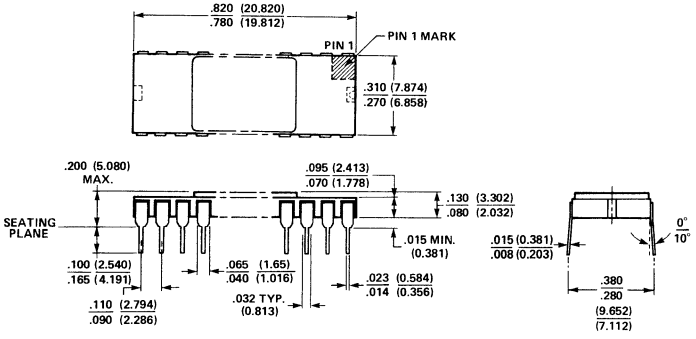

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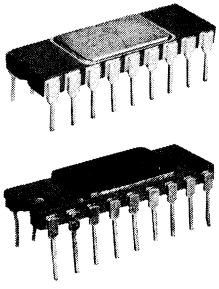

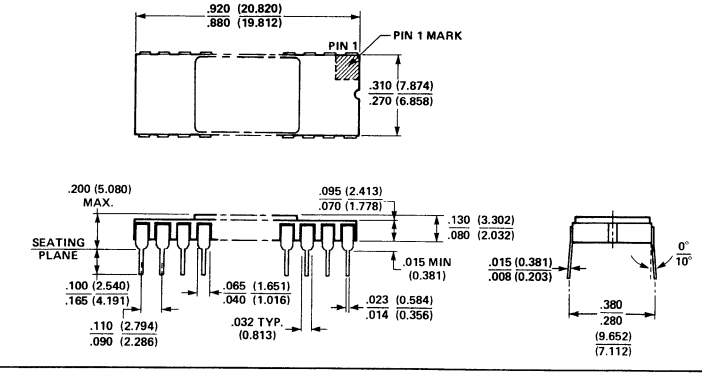

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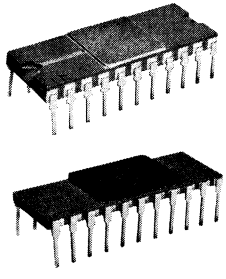

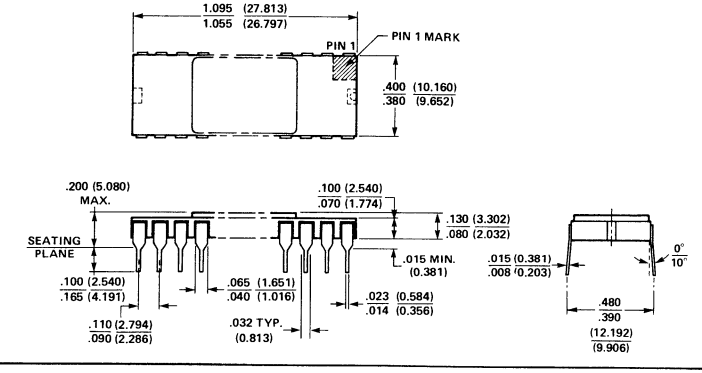

CERAMIC DUAL IN-LINE PACKAGE TYPE C

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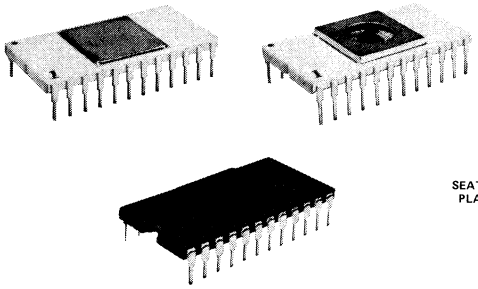

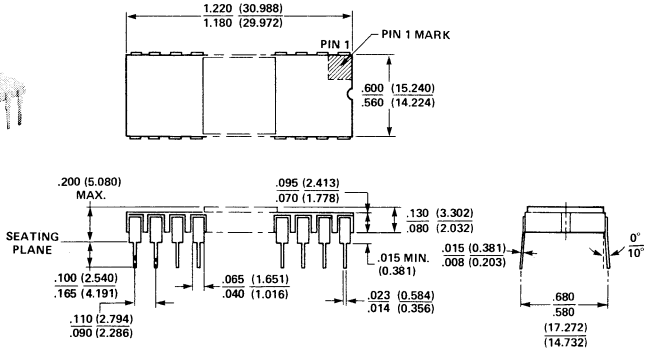

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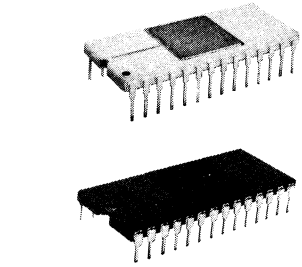

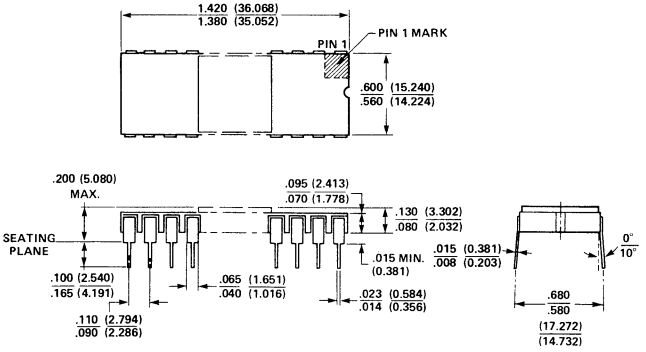

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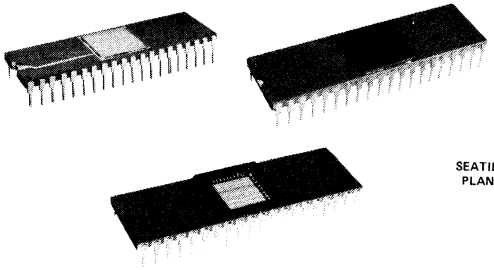

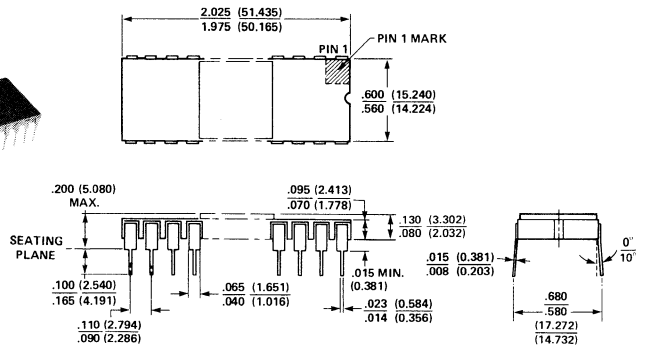

CERAMIC DUAL IN-LINE PACKAGE TYPE B

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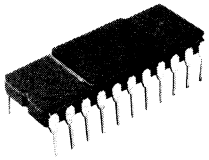

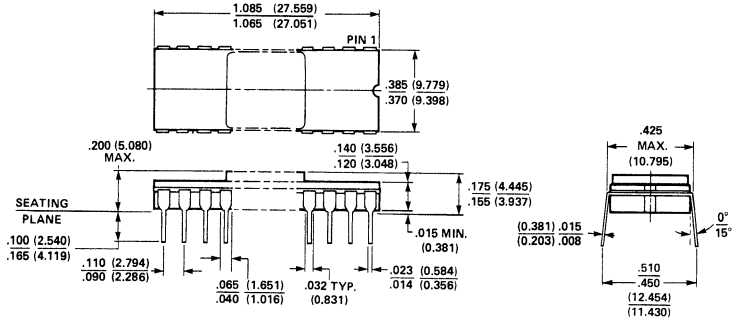

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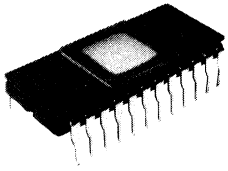
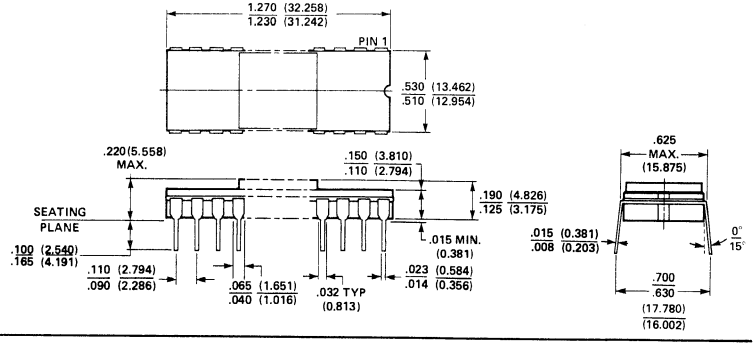
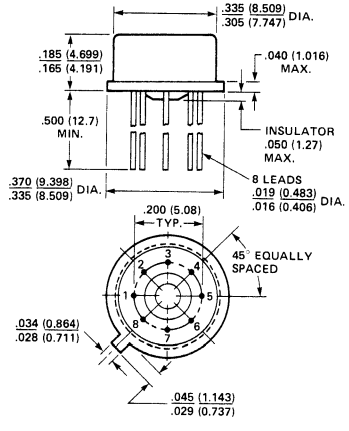




METAL CAN PACKAGE TYPE M

8-LEAD METAL CAN PACKAGE TYPE M



INTEL MILITARY PRODUCTS
IC 38510 PROGRAM

Intel offers selected products in full conformance with requirements for military components. Effort is underway by agencies of the Department of Defense with full Intel cooperation to establish "JAN" standards for several of our products. Intel has led these standards by emulating the anticipated "JAN" processing and lot acceptance requirements with the Intel in-house IC 38510 Program. Intel Specifications are available which document general and detailed requirements for each of the military products. Detail specifications are organized by generic family and provide all information necessary for non-standard parts submissions in accordance with MIL-STD-749, Step I, Step II, and Step III. These documents are available from your local Intel Sales Office or authorized Intel Distributor.

Three levels of product assurance are offered: Level B, Level C, and Military Temperature Only.

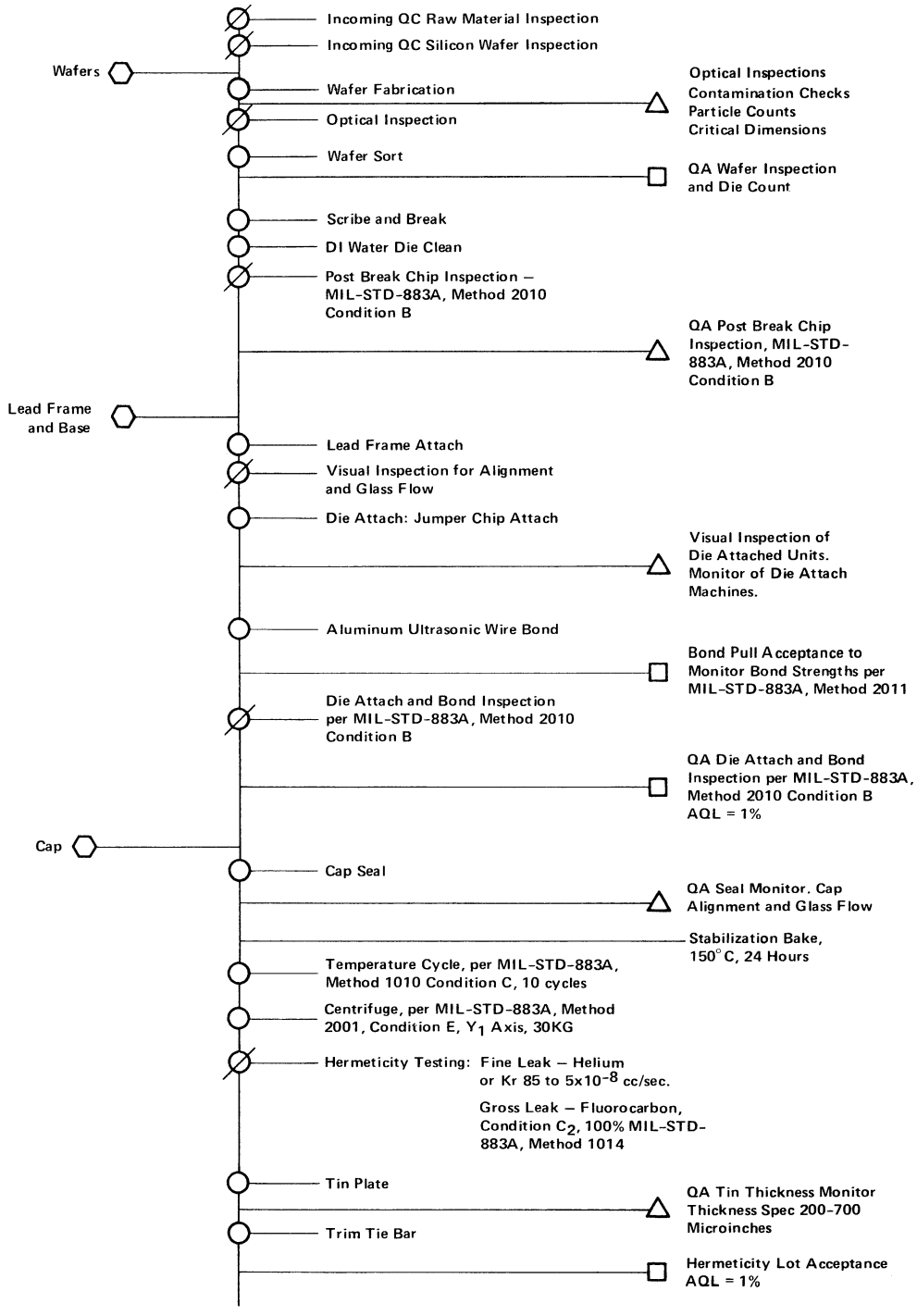
The Military Temperature level products have guaranteed operating characteristics over the specified temperature range and have undergone Intel's rigid product assurance requirements.

Level C and Level B products are in conformance with MIL-STD-883, Method 5004 requirements, and in addition, have a specified maximum rebond criteria (10%) and a specified burn-in PDA (10%), all documented in the detail specifications, consistent with 38510 requirements. Lot conformance tests are performed in accordance with MIL-STD-883A, Method 5005.

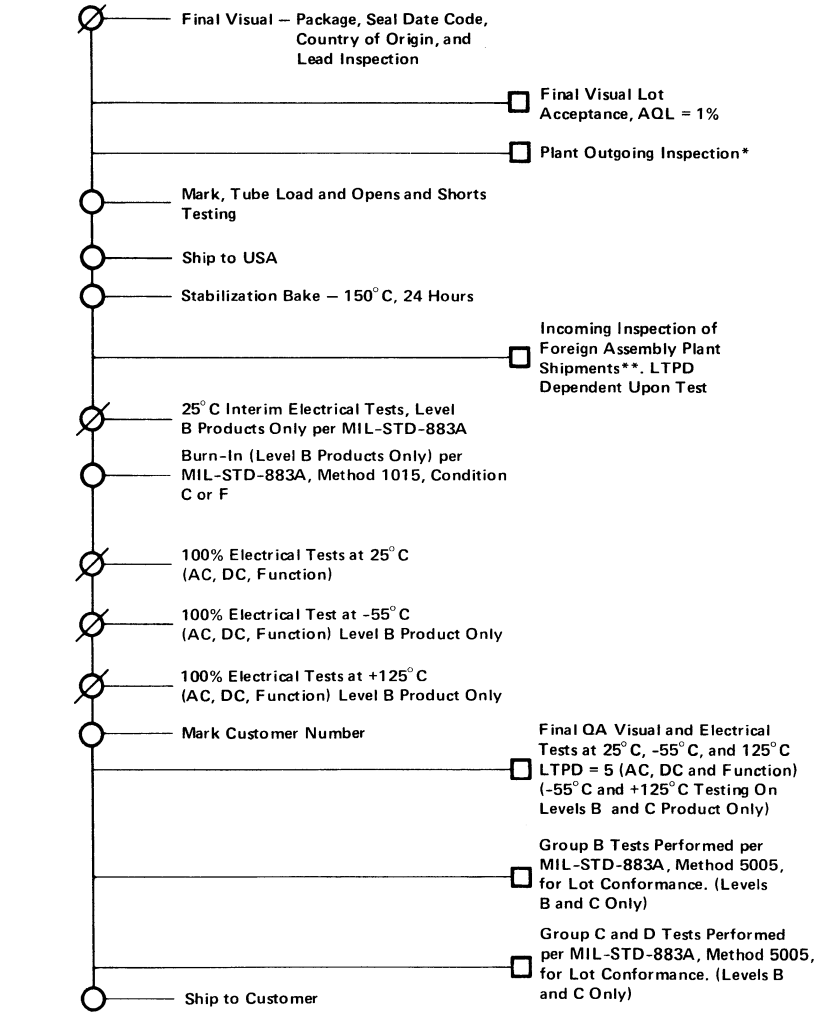
INTEL MILITARY PRODUCT FAMILY

MCS-80	3000 Series	PROMs	RAMs
MC8080A	MD3001	MC1702A	MD2102A-4
MD8102A-4	MD3002	MC2708	MD2115L
MD8212	MD3003	MD3601	MD2125L
MD8214	MD3212	MD3604	MC5101-4
MD8216	MD3214	MD3624	MC5101L-4
MD8224	MD3216		
MD8228			
MC8251			
MC8255			
MC8316A			
MC8702A			
MC8708			

LEVEL B AND C
MILITARY PRODUCTS MANUFACTURING FLOW



LEVEL B AND C
MILITARY PRODUCTS MANUFACTURING FLOW (Cont'd)



PIECE PARTS

MANUFACTURING OPERATION

MANUFACTURING INSPECTION OR TEST

QA MONITOR

QA LOT ACCEPTANCE

*Outgoing Acceptance (Plant Clearance) Inspections:

Test	LTPD	ACC
1. Hermeticity	5	2
2. Centrifuge	5	2
3. X-Ray	7	1
4. Lead Fatigue	20	0
5. Acoustic (Loose Particles) AQL = .04%		

**Incoming Inspection Testing:

Test	LTPD	ACC
1. X-Ray, Die Attach and Seal Quality	7	1
2. External Visual	7	1
3. Opens and Shorts	7	1
4. Hermeticity	7	1
5. Lead Fatigue	20	0
6. Internal Visual	10	0
7. Bond Pull	7	1
8. Acoustic (1000 Particles) AQL = .04%		

Optical inspection criteria based on MIL-STD-883 Method 2010.1B to insure that all devices are free from internal defects which could lead to failure in normal applications. (Monitored by QA)

Hermeticity Testing to eliminate devices which show insufficient hermeticity. (Monitored by QA)
Fine leak C DIPs,CERDIPs, and Metal cans (MIL-STD-883 Method 1014A)* **Gross Leak** C DIPs and Cerdips only (Method 1014C; vacuum omitted and 2 hour pressurization).

Die Attach
(Monitored by QA)

Lead Bonding (Monitored by QA per MIL-STD-883 Method 2011 Test Condition D.)

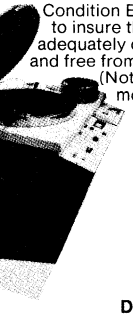
Metal Can
Pneupactor for constant acceleration and mechanical shock (15,000G for 0.5 msec) to insure that all devices are adequately die attached, bonded and free from package defects. (Not 100% screened. Monitored by QA)

Precap Visual Inspection criteria based on MIL-STD-883 Method 2010.1B to insure that after assembly all devices are free from defects which could lead to failure in normal applications. (Each lot must pass a QA acceptance.)

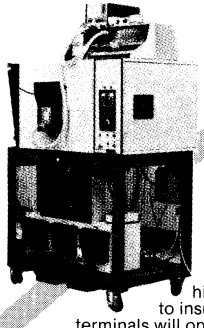
Temperature Cycling per MIL-ST
Method 1010 Test Condition C (1
−65°C to +150°C) to insure that a
are free from metalization, bondi
packaging defects. (Monitored by C

GENERAL INFO

***Fine leak limits:** All devices: 5 x 10^{-7} cc/sec. Quartz lid devices are not tested.



Ceramic DIP and Cerdip Centrifuge for constant acceleration MIL-STD-883 Method 2001 Test Condition E (30,000G Y1 plane) to insure that all devices are adequately die attached, bonded and free from package defects. (Not 100% screened; monitored by QA)



Continuity at high temperature to insure that no terminals will open or short at high temperatures. (Monitored by QA)

Plastic Deflash, trim and form leads. Back fill. (Monitored by QA)

Electrical Testing at 25°C to test conditions and limits which guarantee AC, DC and functional performance over full specified temperature range.

Final QA Acceptance per MIL-STD-883 Method 2009 External Visual, and Electrical AC, DC, Functional Tests at 25°C with correlated limits to guarantee performance over full specified temperature range (AQL 1%)

Intel provides a variety of brochures, application notes, design manuals and other literature. The list below includes the most popular publications available at the time of this publication. If you wish to receive Intel literature, contact your local Intel sales office representative, distributor or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, California 5051. Volume and Educational discounts are available.

International locations also provide selected literature in Japanese, French or German.

Complementary Information

BROCHURES

MCS-48™ Brochure
MCS-80™ Brochure
MCS-85™ Brochure
SBC Single Board Computer Brochure
PL/M Application Brochure
Intellec® Brochure

REFERENCE CARDS

MCS-40™ Assembly Language Reference Card
MCS-48™ Assembly Language Reference Card
MCS-80™ Assembly Language Reference Card

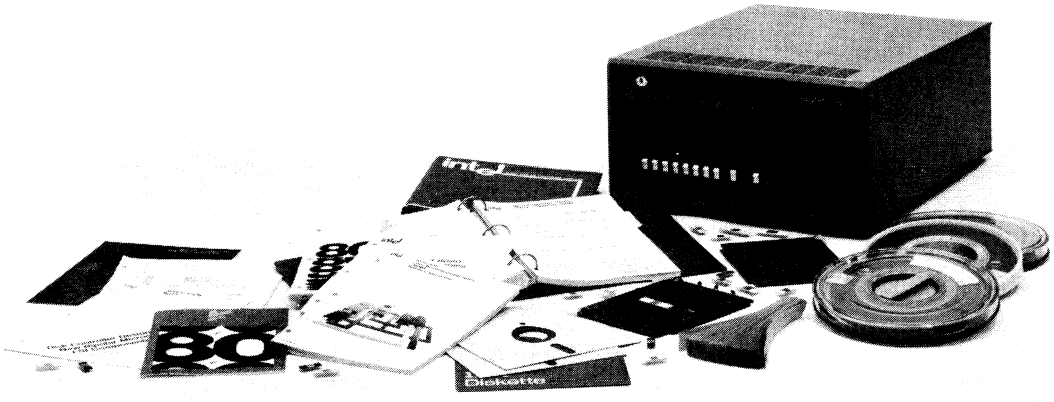
RELIABILITY REPORTS

RR 6 1702A Silicon Gate MOS
RR 7 2107A/2107B
RR 8 Polysilicon Fuse Bipolar PROM
RR 9 MOS Static RAMs
RR 10 8080/8080A Microcomputer
RR 11 2416 16K CCD Memory
RR 12 2708 8K Erasable PROM
RR 14 2115/2125 MOS Static RAMs

APPLICATION NOTES

AP 22 Which Way for 16K?
AP 23 2104A 4K RAM
AP 24 2116 16K RAM

1977 Memory Design Handbook
MCS-40™ User's Manual
MCS-48™ User's Manual
MCS-80™ User's Manual
MCS-85™ User's Manual
Series 3000 Reference Manual
4004/4040 Assembly Language Programming Manual
MCS-48 Assembly Language Programming Manual
8080 Assembly Language Programming Manual
PL/M-80 Programming Manual
Series 3000 Microprogramming Manual
SBC 80/10 Hardware Reference Manual
SBC 80/20 Hardware Reference Manual
Intellec® Development System Operator's Manual
Intellec® Development System Reference Manual



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