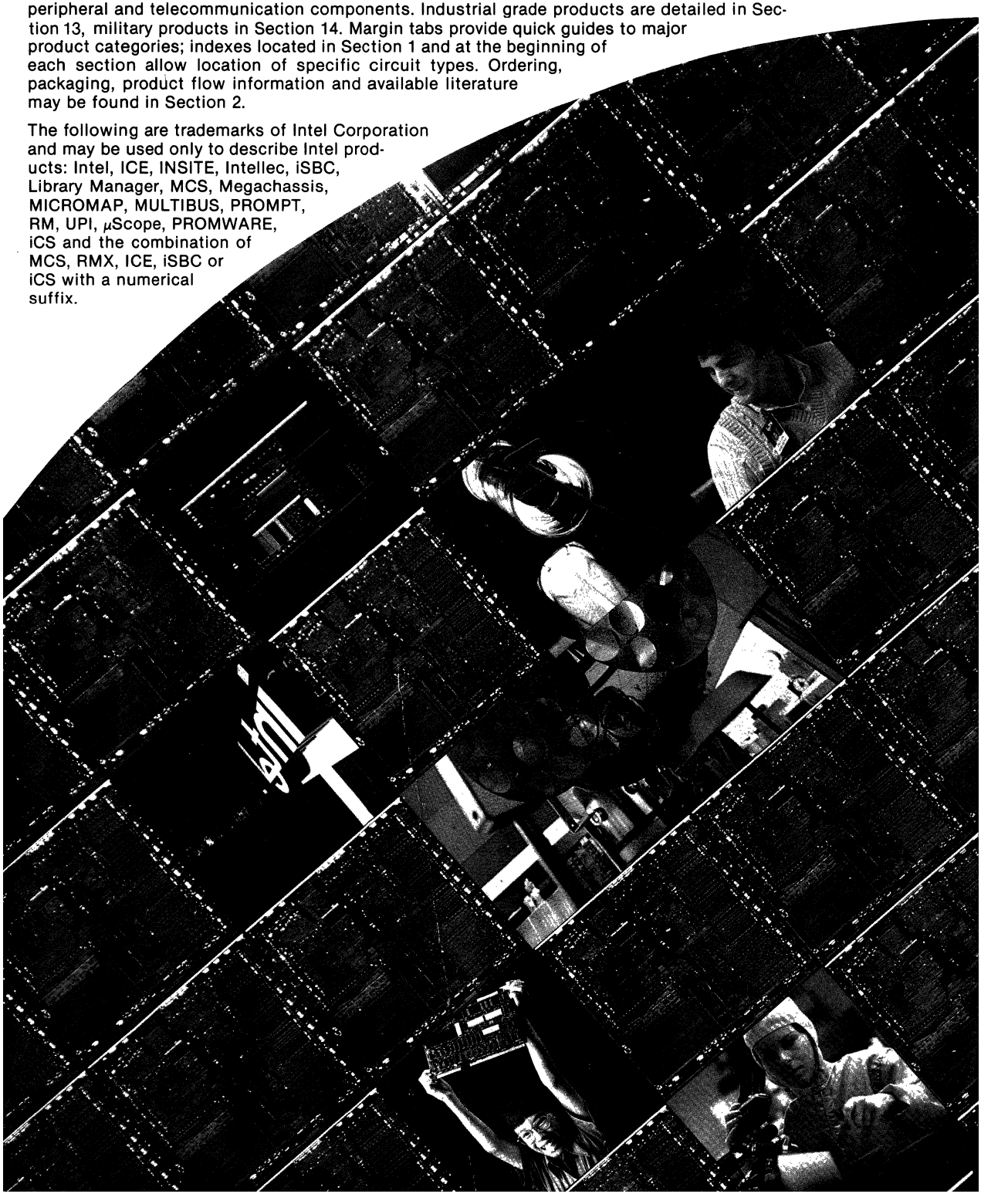
intel Component Data Catalog 1979

Price $5.00

Intel was organized in 1968 to utilize the rapidly expanding technology of Integrated Electronics. During its 10-year history, Intel has become the world's largest supplier of MOS circuits, and is in the top five of the world's producers of all semiconductor devices.

This Component Data Catalog provides complete specifications on most of Intel standard memory, microprocessor, peripheral and telecommunication components. Industrial grade products are detailed in Section 13, military products in Section 14. Margin tabs provide quick guides to major product categories; indexes located in Section 1 and at the beginning of each section allow location of specific circuit types. Ordering, packaging, product flow information and available literature may be found in Section 2.



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Component Data Catalog 1979

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Component Data Catalog

1979

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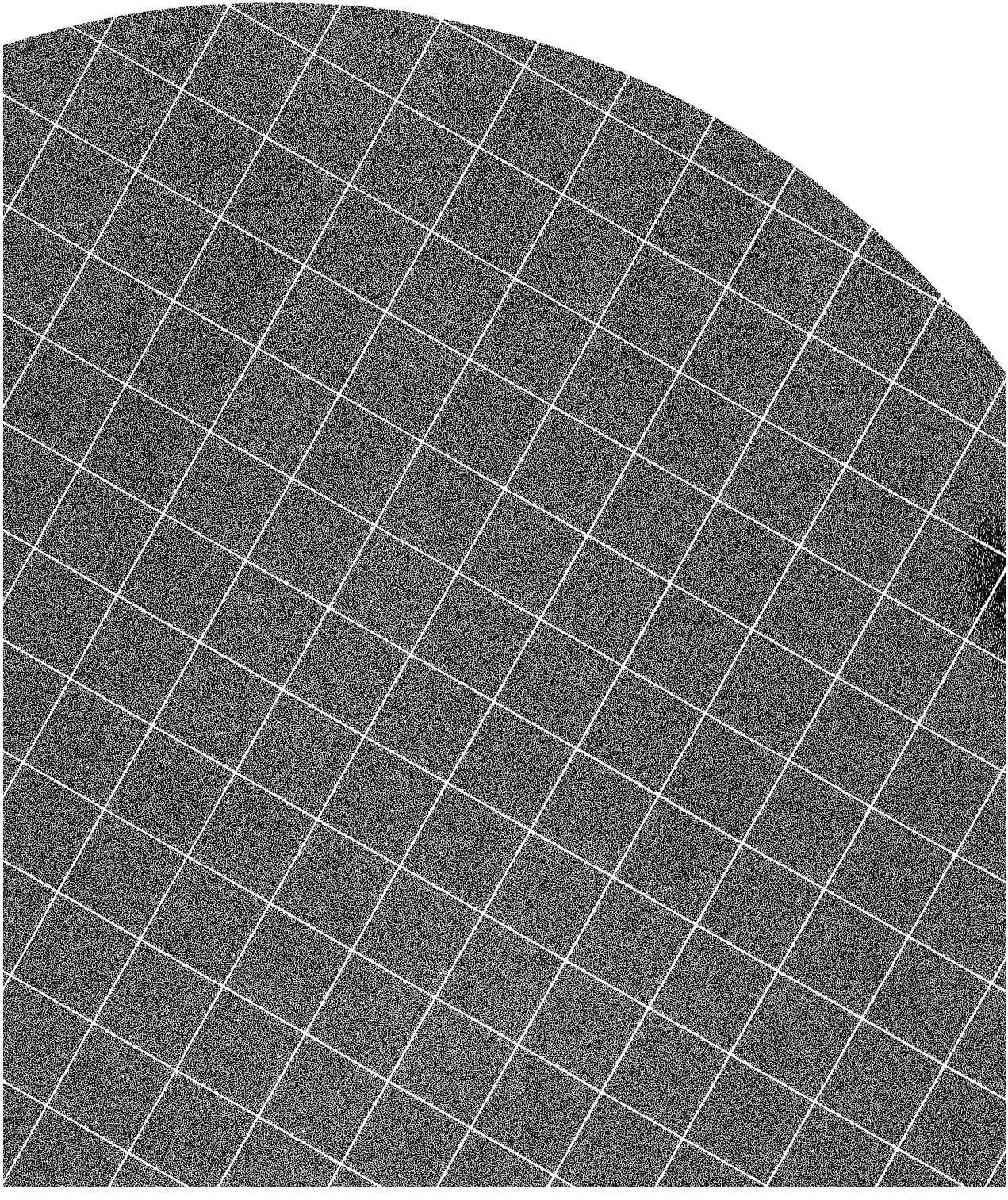

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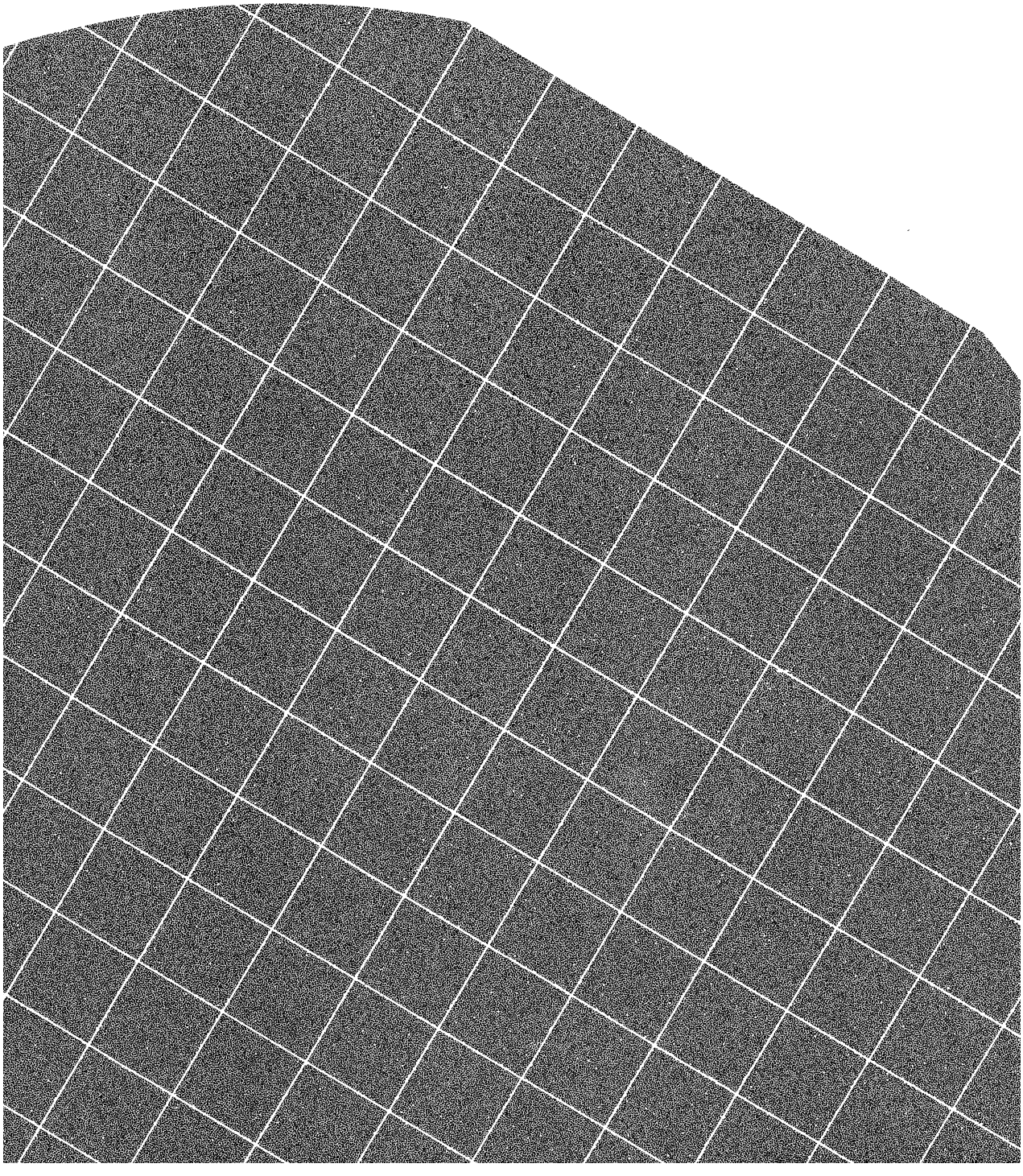

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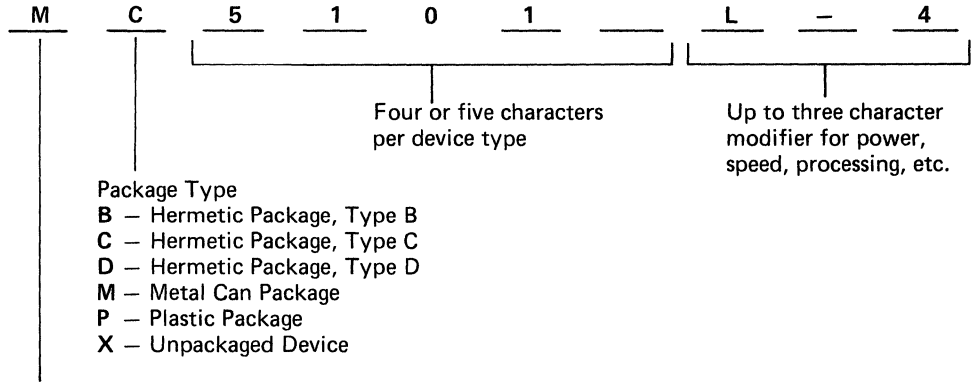

Examples:

P5101L CMOS 256 X 4 RAM, low power selection, plastic package, commercial temperature range.

C8080A2 8080A Microprocessor with 1.5 μs cycle time, hermetic package Type C, commercial temperature range.

MD3604/C 512 X 8 PROM, hermetic package Type D, military temperature range, MIL-STD-883 Level C processing.*

MC8080A/B 8080A Microprocessor, hermetic package Type C, military temperature range, MIL-STD-883 Level B processing.*

Kits, boards and systems may be ordered using the part number designations in this catalog.

The latest Intel OEM price book should be consulted for availability of various options. These may be obtained from your local Intel representative or by writing directly to Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

**On military temperature devices, B suffix indicates MIL-STD-883 Level B processing. Suffix C indicates MIL-STD-883 Level C processing. "S" number suffixes must be specified when entering any order for military temperature devices. All orders requesting source inspection will be rejected by Intel.*

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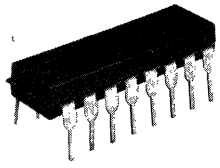

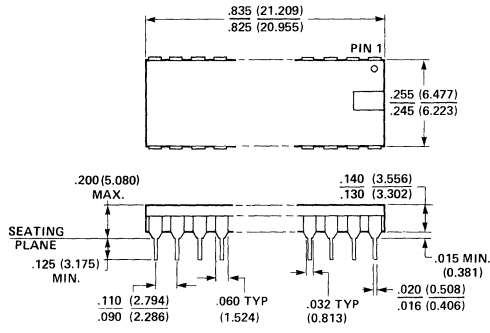

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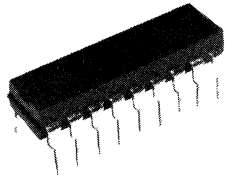

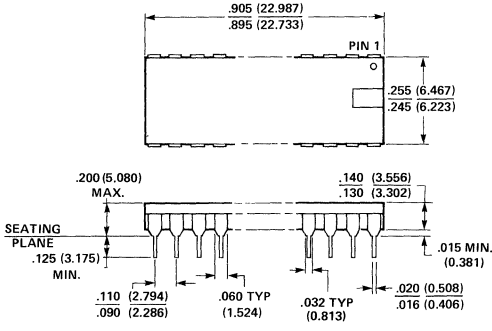

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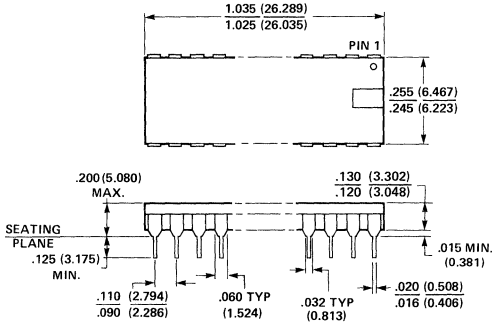

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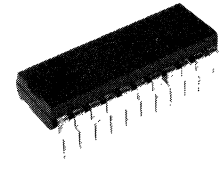

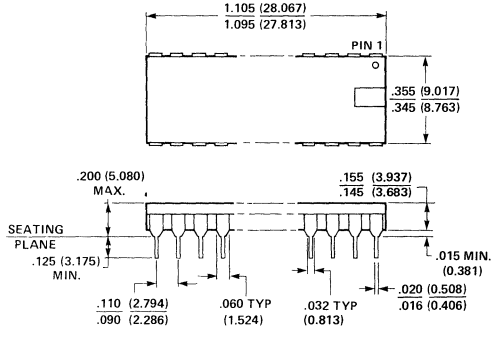

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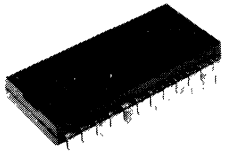

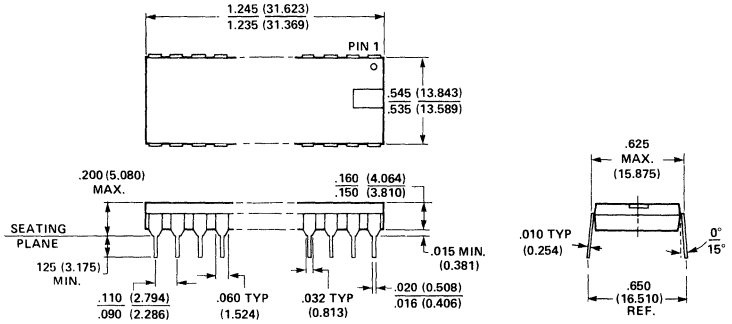

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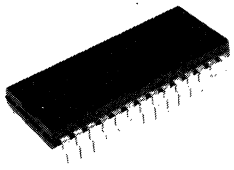

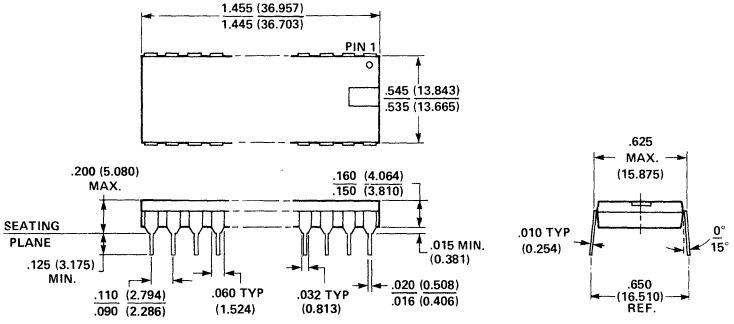

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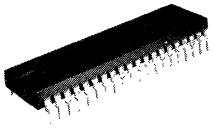

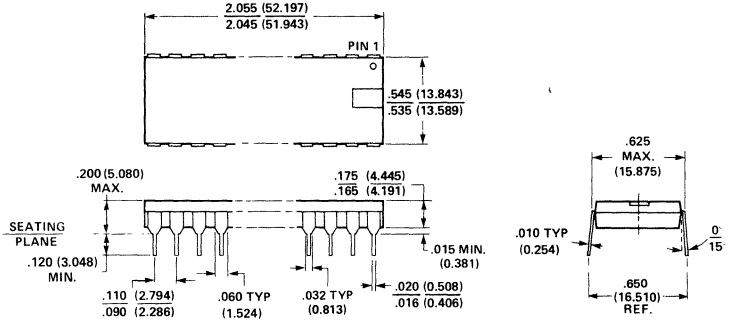

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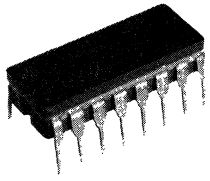

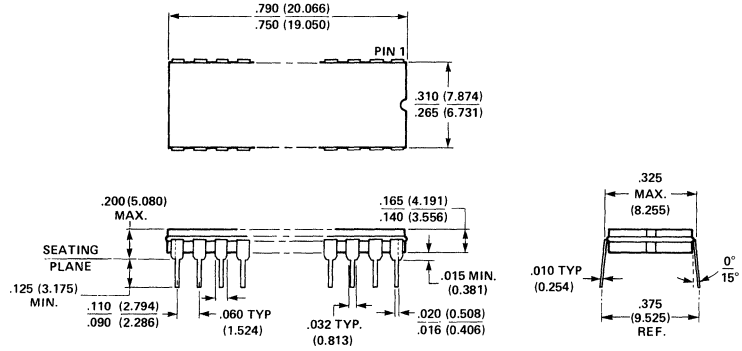

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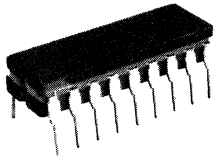

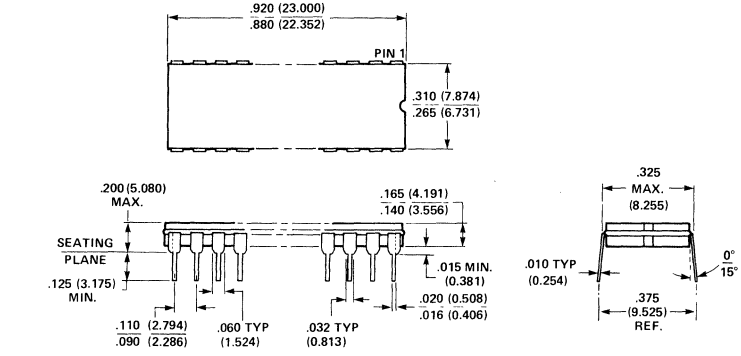

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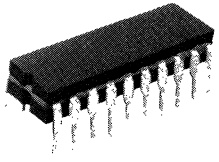

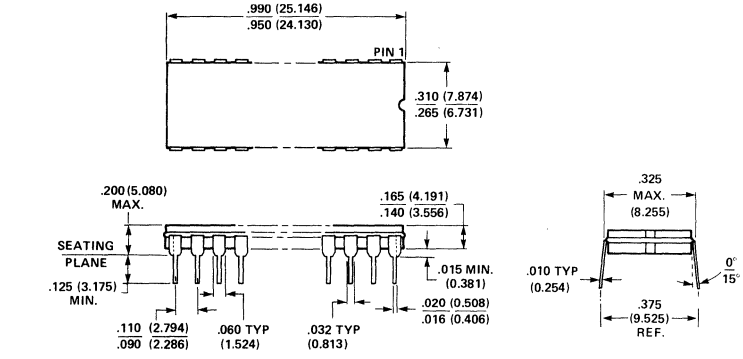

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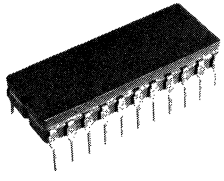

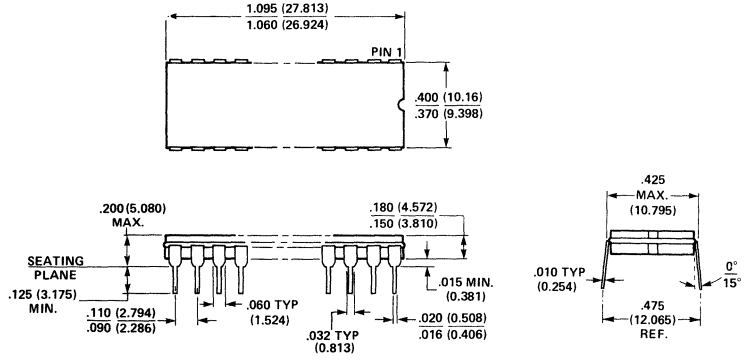

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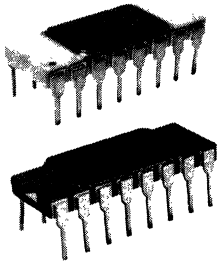

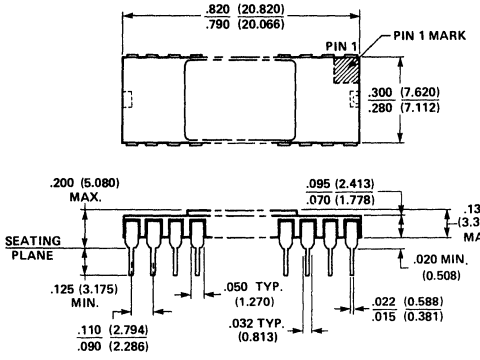

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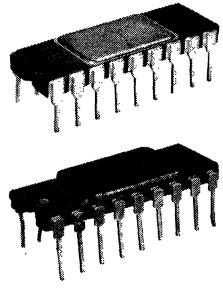

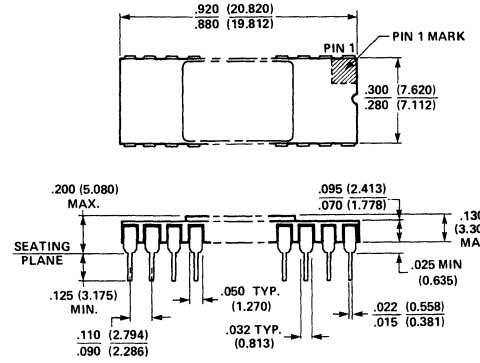

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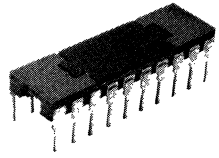

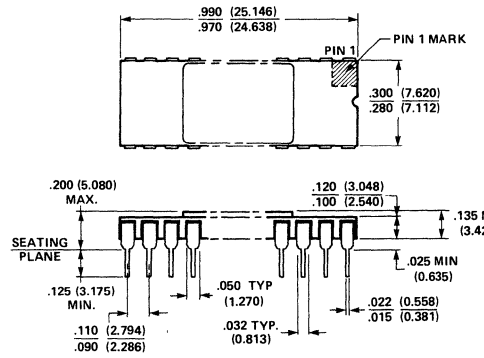

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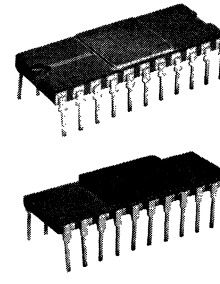

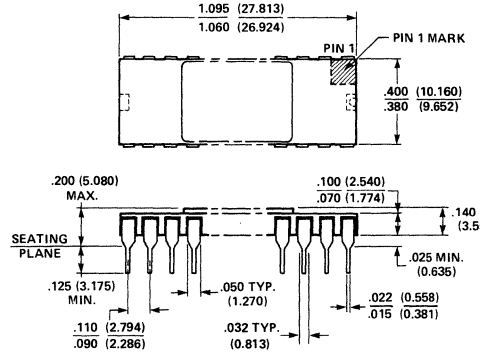

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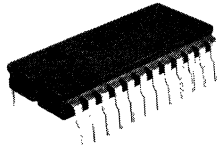

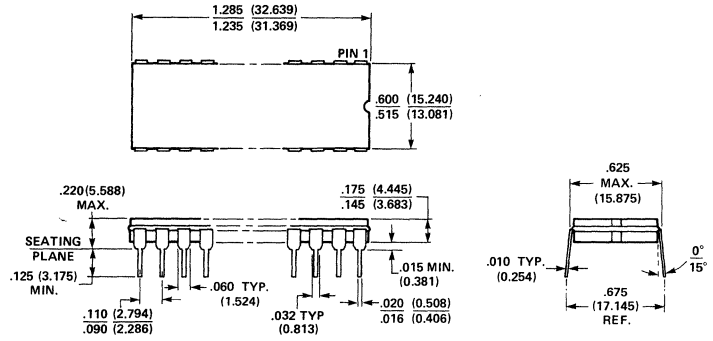

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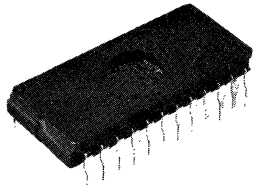

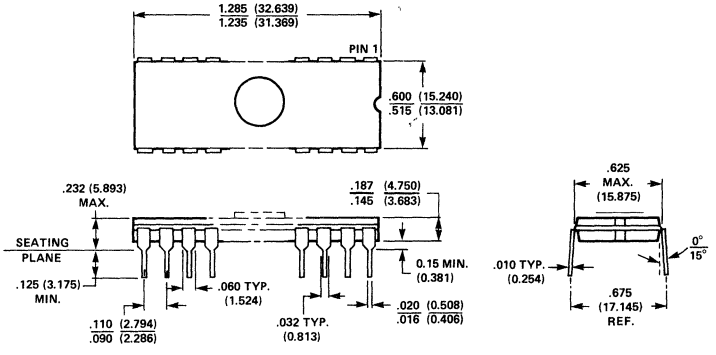

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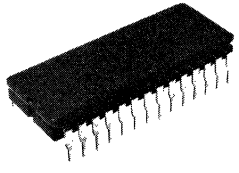

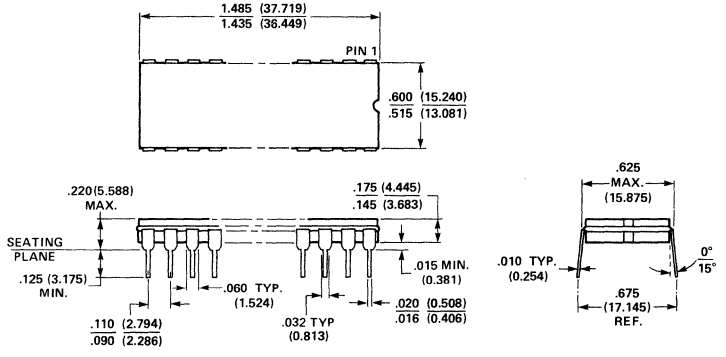

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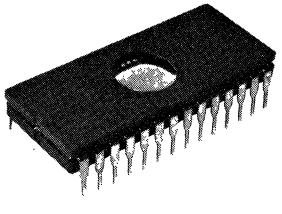

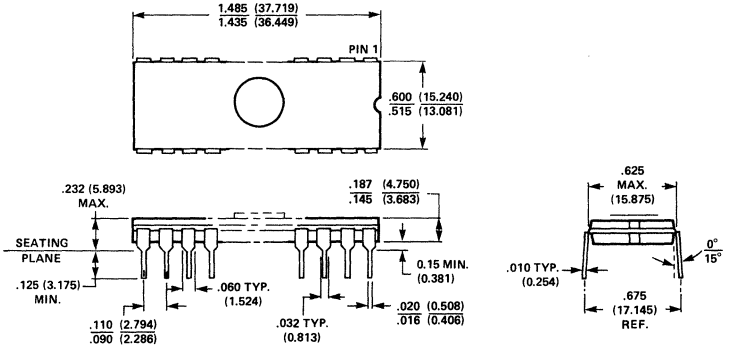

CERAMIC DUAL IN-LINE PACKAGE TYPE D

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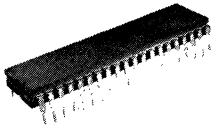

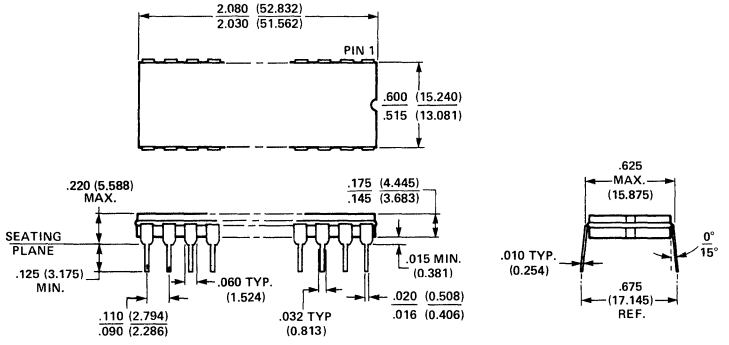

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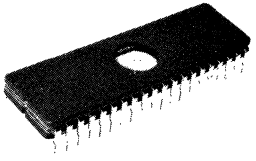

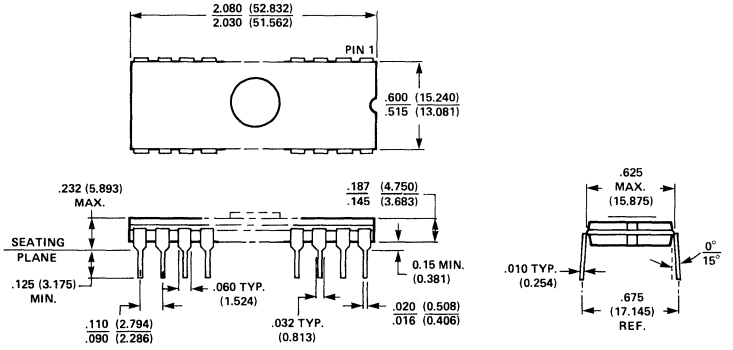

GENERAL

CERAMIC DUAL IN-LINE PACKAGE TYPE C

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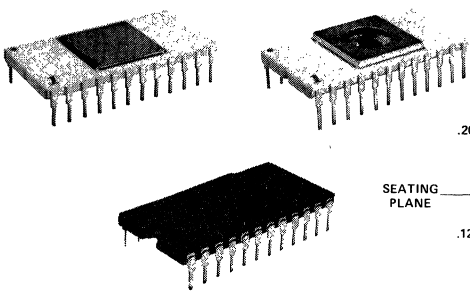

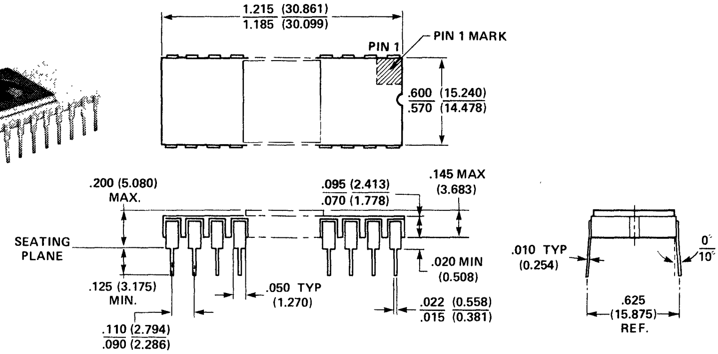

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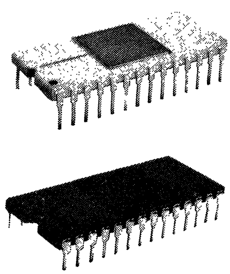

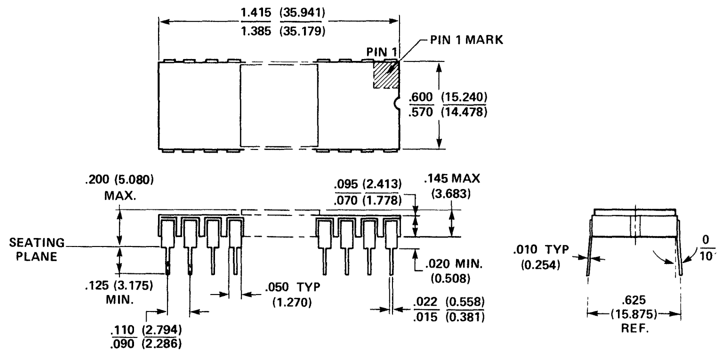

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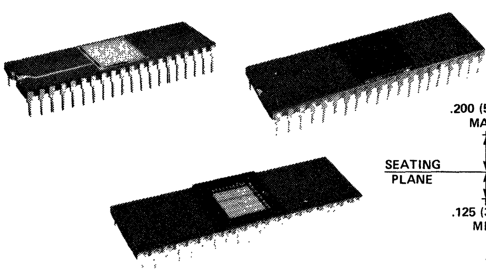

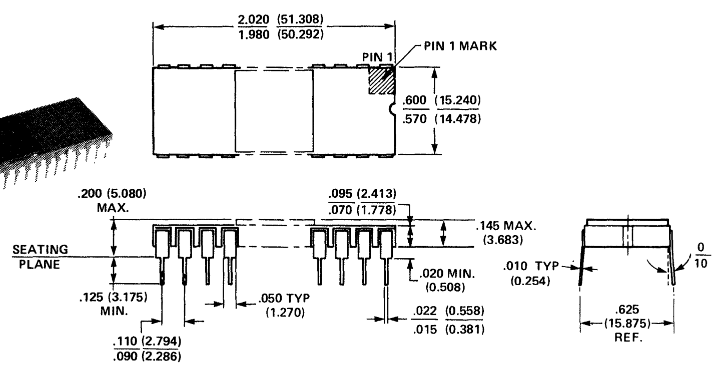

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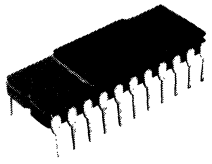

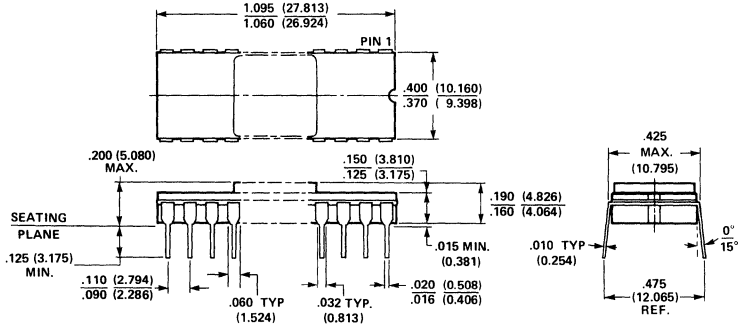

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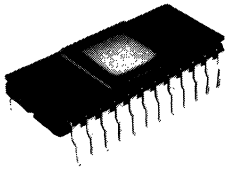

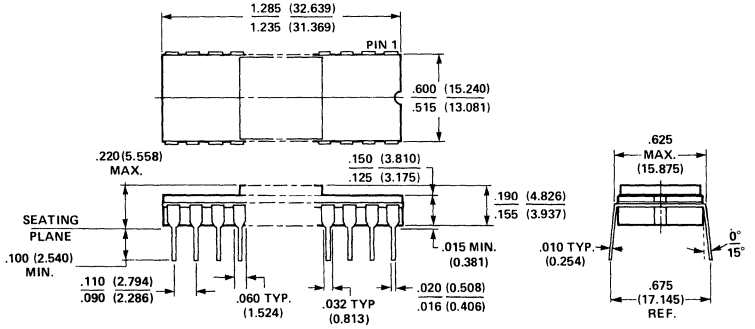

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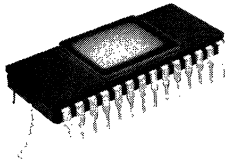

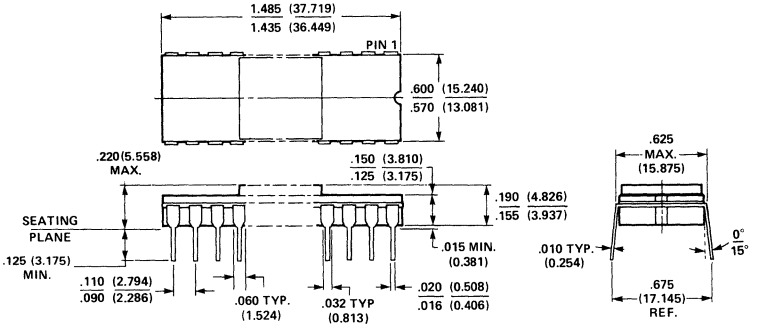

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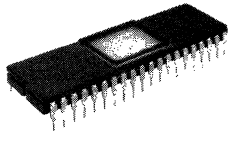
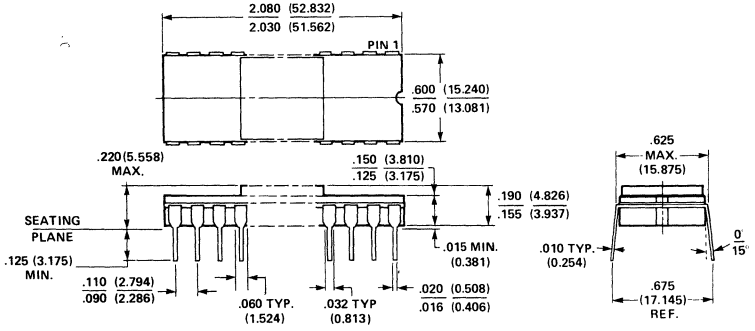
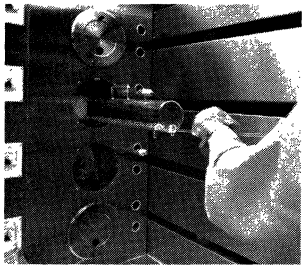






Wafer Fabrication

1st Optical Inspection For Fab Defects

Electrical Wafer Sort

1st Optical Inspection for Sort Defects

Scribe or Saw & Break

2nd Optical Inspection

2nd Optical Inspection QA Gate

Die Attach

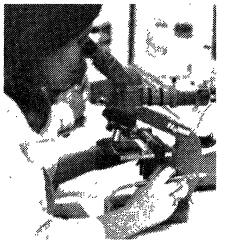
Die Attach Inspection

QA Die Attach Gate

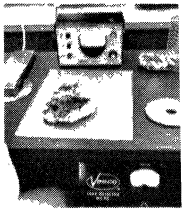
Lead Bond

Lead Band Inspection

Lead Bond Gate



Optical inspection criteria based on MIL-STD-883 Method 2010.3B to insure that all devices are free from internal defects which could lead to failure in normal applications. (Monitored by QA)

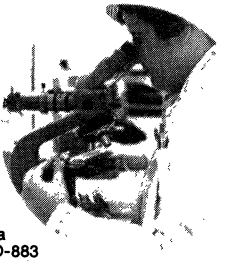


Hermeticity Testing to eliminate devices which show insufficient hermeticity. (Monitored by QA)
Fine leak C DIPs,CERDIPs, and Metal cans (MIL-STD-883 Method 1014.2B).* **Gross Leak** C DIPs and Cerdips only (Method 1014.2C, vacuum omitted and 1 hour pressurization).

Temp Cy

Seal

HERMETIC



Precap Visual Inspection criteria based on MIL-STD-883 Method 2010.3B to insure that after assembly all devices are free from defects which could lead to failure in normal applications. (Each lot must pass a QA acceptance.)

PLASTIC

Mold

Temp Cycle

Deflash, Trim & Form

Solder Dip

Lead Trim

late

***Fine leak limits:** All devices 1 x 10-7 cc•atm/sec

Final Visual

QA Visual Acceptance

QA Outgoing Acceptance

Electrical Testing to test conditions and limits which guarantee AC, DC and functional performance over full specified temperature range.

Final QA Acceptance

Electrical 1% AQL AC, DC
Functional Tests to guarantee performance over full specified temperature range
Visual/Mechanical LTPD 7/2
Solderability LTPD 50/0
Hermeticity LTPD 7/1

Plant Clearance

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The accelerating rate of new developments in microprocessors and memories has created the need for concise, up-to-the-minute design information. To assist customers in maintaining expertise in state of the art systems, Intel provides a variety of sales and technical literature including brochures, data sheets, application notes, handbooks, and technical manuals containing comprehensive information on microprocessors, microcomputers, memories, development systems, and software.

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SALES LITERATURE

Catalogs

610200	1978 System Data Catalog	$2.00

Brochures

	Microcomputer Product Line Brochure	N/C
	Microcomputer Components Brochure	N/C
	Memory Components Brochure	N/C
	Growing Static RAM Family Album	N/C
	MOS RAMs Brochure	N/C
	μScope 820 Brochure	N/C
	1979 Intel Microcomputer Workshops Brochure	N/C

Application Notes

AP-4	2107A Application Note	N/C
AP-12	5101 Application Note	N/C
AP-15	8255 Programmable Peripheral Interface	N/C
AP-16	Using the 8251 Application Note	N/C
AP17	2709 8K Erasable PROM Application Note	N/C
AP-22	Which Way for 16K	N/C
AP-23	2104A 4K RAM	N/C
AP-24	MCS-48 Family—9800413B	N/C
AP-26	iSBC 80/10 & System 80/10	N/C
AP-27	Control With UPI-41	N/C
AP-28	Multibus Interfacing—9800587A	N/C
AP-29	Using The Intel 8085 Serial I/O Lines	N/C
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AP-31	Using the 8259—9800658A	N/C
AP-33	RMX/80—9800577A	N/C
AP-35	CRYSTALS: Specifications—9800652A	N/C
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AP-40	Keyboard/Display Scanning With Intel's MCS-48 Microcomputers	N/C
AP-42	Writing Diagnostics for the μScope	N/C
AP-43	Using the iSBC™ 957 . . . 9800816	N/C
AP-45	Using the 8202 . . . 9800809	N/C

Product Descriptions

9800365	MCS-85 Product Description	N/C
9800600	Peripherals Product Description	N/C
9800606	Intellec Series II Microcomputer Development Systems Functional Description and Specifications	N/C
9800615	MCS-48 Single Chip Family of Microcomputers Product Description	N/C
9800723	MCS-86 Product Description	N/C

Reference Guides

9800774	BASIC 80 Reference Guide	N/C
9800749	MCS-86 Assembly Language Reference Guide	N/C

Reference Cards

9800404	PROMPT 48 Reference Cardlet	$1.50
9800438	8085/8080 Assembly Language Reference Card	N/C
9800547	FORTRAN-80 Reference Card	N/C
9800582	μScope 820 8080A Operator's Reference Card	N/C
9800653	MCS-48 In-Circuit Emulator Reference Card	N/C
9800412	MCS-48 Assembly Language Reference Card	N/C
	UPI-41 Assembly Language Reference Card	N/C

Reliability Reports

RR 7	2107A/2107B 4K Dynamic RAM	N/C
RR 8	Polysilicon Fuse Bipolar PROM	N/C
RR 9	MOS Static RAMs	N/C
RR 10	8080/8080A Microcomputer	N/C
RR 11	2416 16K CCD Memory	N/C
RR 12	2708 8K Erasable PROM	N/C
RR 14	2115/2125 MOS Static RAMs	N/C
RR 15	2104A 4K Dynamic RAM	N/C
RR 16	2116 16K Dynamic RAM	N/C
RR 17	iSBC 80/10 Single Board Computer	N/C
RR 18	HMOS Reliability	N/C

TECHNICAL LITERATURE

User's Guides

9800016	High Speed Paper Tape Reader Installation and Operation Guide	$2.50
9800203	MCS-80 System Design Kit User's Guide	$5.00
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9800707	System 80/30 Documentation Package	$25.00

Handbooks

9800526	μScope 820 Microprocessor System Console Operator's Handbook	$15.00
9800676	Peripheral Design Handbook — 1979	$7.50
111100	Memory Design Handbook	$5.00

Specifications

9800199	External Reference Specification ROM Simulator	$2.50
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9800606	Intellec Series II Microcomputer Development Systems Functional Description and Specifications	N/C

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TWX: 610 562-1906

†Zentronics
141 Catherine Street
Ottawa, Ontario K2P 1C3
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99 Norfinch Dr.
Downsview, Ontario M3N 1W8
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Telex: 02-021694

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St. Laurent H4S 1G2
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Montreal H4P 2L7

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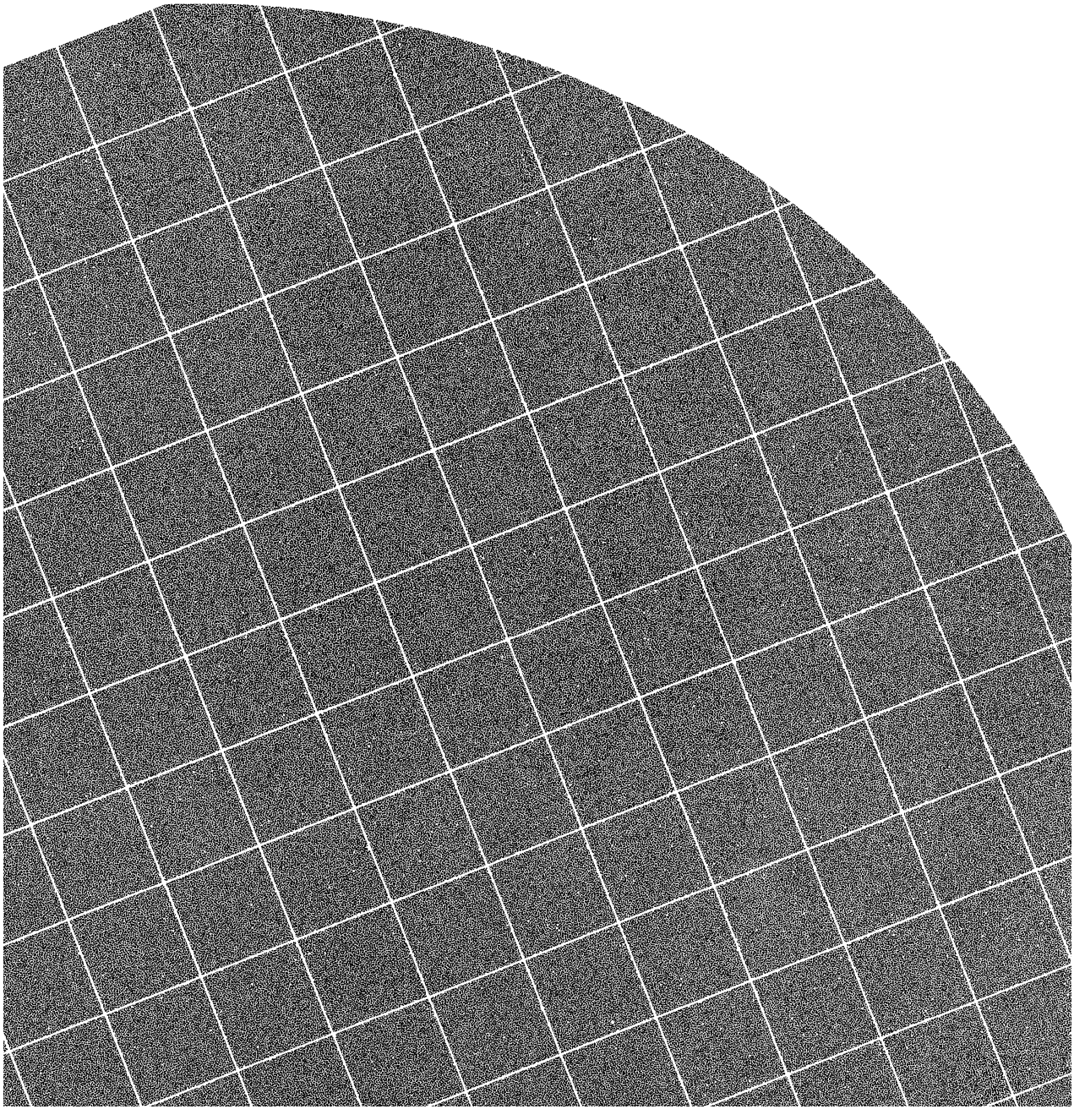
*Microcomputer System Spares Order Point

Random Access Memory 3



RANDOM ACCESS MEMORIES

SILICON GATE NMOS

Type	No. of Bits	Description	Organization	No. of Pins	Electrical Characteristics Over Temperature: Access Time Max. (ns)	Cycle Time Min. (ns)	Power Dissipation Max.[1] Operating/ Standby (mW)	Supplies (V)	Page No.
DYNAMIC RAMS									
2104A	4096	16-Pin Dynamic	4096x1	16	350	350	441/25	+12, +5, -5	3-12
2104A-1	4096	16-Pin Dynamic	4096x1	16	150	320	462/26	+12, +5, -5	
2104A-2	4096	16-Pin Dynamic	4096x1	16	200	375	422/26	+12, +5, -5	
2104A-3	4096	16-Pin Dynamic	4096x1	16	250	375	396/26	+12, +5, -5	
2104A-4	4096	16-Pin Dynamic	4096x1	16	300	425	396/26	+12, +5, -5	
2107C	4096	22-Pin Dynamic	4096x1	22	250	430	396/2.6	+12, +5, -5	3-28
2107C-1	4096	22-Pin Dynamic	4096x1	22	150	380	462/2.6	+12, +5, -5	
2107C-2	4096	22-Pin Dynamic	4096x1	22	200	400	436/2.6	+12, +5, -5	
2107C-4	4096	22-Pin Dynamic	4096x1	22	300	470	396/2.6	+12, +5, -5	
2109-3	8192	16-Pin Dynamic	8192x1	16	200	375	462/20	+12, +5, -5	3-33
2109-4	8192	16-Pin Dynamic	8192x1	16	250	410	436/20	+12, +5, -5	
2117-2	16,384	16-Pin Dynamic	16,384x1	16	150	320	462/20	+12, +5, -5	3-64
2117-3	16,384	16-Pin Dynamic	16,384x1	16	200	375	462/20	+12, +5, -5	
2117-4	16,384	16-Pin Dynamic	16,384x1	16	250	410	436/20	+12, +5, -5	
2117-5	16,384	16-Pin Dynamic	16,384x1	16	300	490	462/20	+12, +5, -5	
2118-2	16,384	16-Pin Dynamic	16,384x1	16	80	200	160/16.5	+5	3-88
2118-3	16,384	16-Pin Dynamic	16,384x1	16	100	235	138/16.5	+5	
2118-4	16,384	16-Pin Dynamic	16,384x1	16	120	270	121/16.5	+5	
2118-7	16,384	16-Pin Dynamic	16,384x1	16	150	320	121/16.5	+5	
STATIC RAMS									
2101A/8101A	1024	Static, Separate I/O	256x4	22	350	350	300	+5	3-4
2101A-2	1024	Static, Separate I/O	256x4	22	250	250	350	+5	
2101A-4	1024	Static, Separate I/O	256x4	22	450	450	300	+5	
2102A/8102A	1024	Static	1024x1	16	350	350	275	+5	3-8
2102A-2	1024	Static	1024x1	16	250	250	325	+5	
2102A-4	1024	Static	1024x1	16	450	450	275	+5	
2102AL	1024	Low Standby Power Static	1024x1	16	350	350	165/35	+5	
2102AL-2	1024	Low Standby Power Static	1024x1	16	250	250	325/42	+5	
2102AL-4	1024	Low Standby Power Static	1024x1	16	450	450	165/35	+5	
2111A/8111A	1024	Static, Common I/O with Output Deselect	256x4	18	350	350	300	+5	3-45
2111A-2	1024	Static, Common I/O	256x4	18	250	250	350	+5	
2111A-4	1024	Static, Common I/O	256x4	18	450	450	300	+5	
2112A	1024	Static, Common I/O without Output Deselect	256x4	16	350	350	300	+5	3-49
2112A-2	1024	Static, Common I/O without Output Deselect	256x4	16	250	250	350	+5	
2112A-4	1024	Static, Common I/O without Output Deselect	256x4	16	450	450	300	+5	
2114	4096	Static, Common I/O	1024x4	18	450	450	525	+5	3-54
2114-2	4096	Static, Common I/O	1024x4	18	200	200	525	+5	
2114-3	4096	Static, Common I/O	1024x4	18	300	300	525	+5	
2114L	4096	Static, Common I/O	1024x4	18	450	450	370	+5	
2114L2	4096	Static, Common I/O	1024x4	18	200	200	370	+5	
2114L3	4096	Static, Common I/O	1024x4	18	300	300	370	+5	

RANDOM ACCESS MEMORIES (Cont.)

	Type	No. of Bits	Description	Organization	No. of Pins	Electrical Characteristics Over Temperature: Access Time Max. (ns)	Cycle Time Min. (ns)	Power Dissipation Max.[1] Operating/ Standby (mW)	Supplies (V)	Page No.
	STATIC RAMS (Continued)									
SILICON GATE NMOS	**M2114**	4096	Static, Common I/O T_A = -55°C to +125°C	1024x4	18	450	450	550	+5	14-7
	2115A	1024	High Speed Static, Open Collector	1024x1	16	45	45	655	+5	3-58
	2115A-2	1024	High Speed Static, Open Collector	1024x1	16	70	70	655	+5	
	2115AL	1024	High Speed Static, Open Collector	1024x1	16	45	45	395	+5	
	2115AL-2	1024	High Speed Static, Open Collector	1024x1	16	70	70	395	+5	
	2125A	1024	High Speed Static, Three State	1024x1	16	45	45	655	+5	3-58
	2125A-2	1024	High Speed Static, Three State	1024x1	16	70	70	655	+5	
	2125AL	1024	High Speed Static, Three State	1024x1	16	45	45	395	+5	
	2125AL-2	1024	High Speed Static, Three State	1024x1	16	70	70	395	+5	
	M2115A	1024	High Speed Static, Open Collector	1024x1	16	55	55	690	+5	14-11
	M2115AL	1024	High Speed Static, Open Collector	1024x1	16	75	75	415	+5	
	M2125A	1024	High Speed Static, Three State	1024x1	16	55	55	690	+5	14-11
	M2125AL	1024	High Speed Static, Three State (-55°C to 125°C)	1024x1	16	75	75	415	+5	
	2115H	1024	High Speed Static, Open Collector	1024x1	16	25-35	25-35	655	+5	3-63
	2125H	1024	High Speed Static, Three State	1024x1	16	25-35	25-35	655	+5	3-63
	2141-2	4096	Static	4096x1	18	120	120	385/110	+5	3-89
	2141-3	4096	Static	4096x1	18	150	150	385/110	+5	
	2141-4	4096	Static	4096x1	18	200	200	303/66	+5	
	2141-5	4096	Static	4096x1	18	250	250	303/66	+5	
	2141L-3	4096	Static	4096x1	18	150	150	220/28	+5	
	2141L-4	4096	Static	4096x1	18	200	200	220/28	+5	
	2141L-5	4096	Static	4096x1	18	250	250	220/28	+5	
	2142	4096	Static, with Output Enable	1024x4	20	450	450	525	+5	3-95
	2142-2	4096	Static, with Output Enable	1024x4	20	200	200	525	+5	
	2142-3	4096	Static, with Output Enable	1024x4	20	300	300	525	+5	
	2142L	4096	Static, with Output Enable	1024x4	20	450	450	375	+5	
	2142L-2	4096	Static, with Output Enable	1024x4	20	200	200	375	+5	
	2142L-3	4096	Static, with Output Enable	1024x4	20	300	300	375	+5	
	2147	4096	High Speed Static	4096x1	18	70	70	880/110	+5	3-99
	2147-3	4096	High Speed Static	4096x1	18	55	55	990/165	+5	
	2147L	4096	High Speed Static	4096x1	18	70	70	770/55	+5	
	2147H	4096	High Speed Static	4096x1	18	35-45	35-45	990/165	+5	3-105
	M2147	4096	High Speed Static(-55°C to 125°C)	4096x1	18	85	85	990/165	+5	14-15
	2148	4096	High Speed Static	1024x4	18	60	60	825/165	+5	3-106
SCHOTTKY BIPOLAR	**3101**	64	Fully Decoded	16x4	16	60	60	525	+5	3-107
	3101A	64	High Speed Fully Decoded	16x4	16	35	35	525	+5	
SILICON GATE CMOS	**5101**	1024	Static CMOS RAM	256x4	22	800	800	150/2.5	+5	3-111
	5101L	1024	Static CMOS RAM	256x4	22	650	650	135/20μW	+5	
	5101L-1	1024	Static CMOS RAM	256x4	22	450	450	135/20μW	+5	
	5101L-3	1024	Static CMOS RAM	256x4	22	650	650	135/1	+5	
	M5101-4	1024	Static CMOS RAM (-55°C to 125°C)	256x4	22	800	800	168/1	+5	14-41
	M5101L-4	1024	Static CMOS RAM (-55°C to 125°C)	256x4	22	800	800	168/400μW	+5	

2101A/8101A-4*

256 X 4 BIT STATIC RAM

2101A-2	250 ns Max.
2101A	350 ns Max.
2101A-4	450 ns Max.

- **256 x 4 Organization to Meet Needs for Small System Memories**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Statis MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 22 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150 mW**
- **Three-State Output: OR-Tie Capability**
- **Output Disable Provided for Ease of Use in Common Data Bus Systems**

The Intel® 2101A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

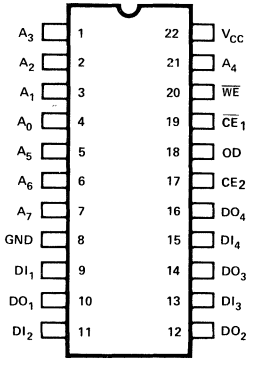
The 2101A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bi-directional logic in a common I/O system.

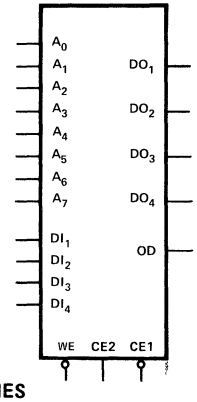
The Intel® 2101A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



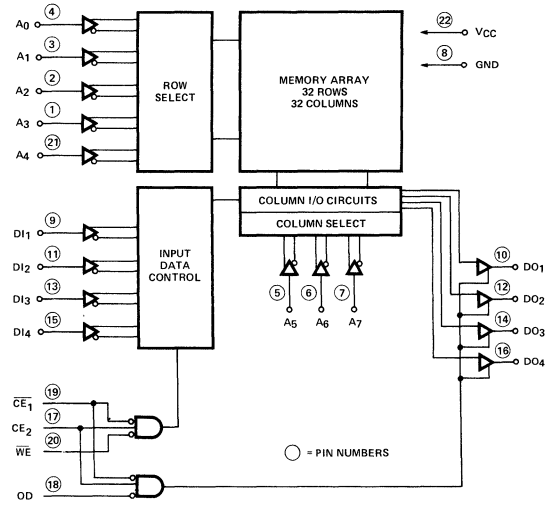
LOGIC SYMBOL



PIN NAMES

DI_1-DI_4	DATA INPUT	$\overline{CE}_2$	CHIP ENABLE 2
A_0-A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	DO_1-DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



*All 8101A-4 specs are identical to the 2101A-4 specs.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

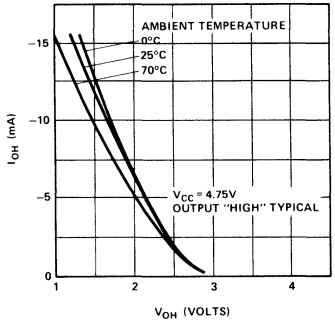
D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

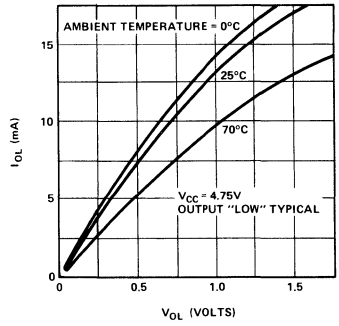
Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Data Output Leakage Current			1	10	μA	Output Disabled, V_{OUT}=4.0V
I_{LOL}	Data Output Leakage Current			-1	-10	μA	Output Disabled, V_{OUT}=0.45V
I_{CC1}	Power Supply Current	2101A, 2101A-4		35	55	mA	V_{IN} = 5.25V, I_O = 0mA, T_A = 25°C
		2101A-2		45	65		
I_{CC2}	Power Supply Current	2101A, 2101A-4			60	mA	V_{IN} = 5.25V, I_O = 0mA, T_A = 0°C
		2101A-2			70		
V_{IL}	Input "Low" Voltage		-0.5		+0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2101A, 2101A-2	2.4			V	I_{OH} = -200μA
		2101A-4	2.4			V	I_{OH} = -150μA

TYPICAL D.C. CHARACTERISTICS

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2101A-2 (250 ns ACCESS TIME)

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	
t_A	Access Time			250	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			180	ns	Input Levels = 0.8V or 2.0V
t_{OD}	Output Disable To Output			130	ns	Timing Reference = 1.5V
t_{DF}[3]	Data Output to High Z State	0		180	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE

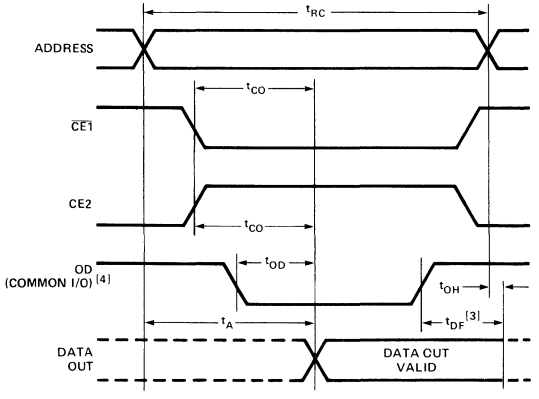
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	
t_{AW}	Write Delay	20			ns	t_r, t_f = 20ns
t_{CW}	Chip Enable To Write	150			ns	Input Levels = 0.8V or 2.0V
t_{DW}	Data Setup	150			ns	Timing Reference = 1.5V
t_{DH}	Data Hold	0			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	150			ns	and C_L = 100pF.
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

CAPACITANCE[2] T_A = 25°C, f = 1MHz

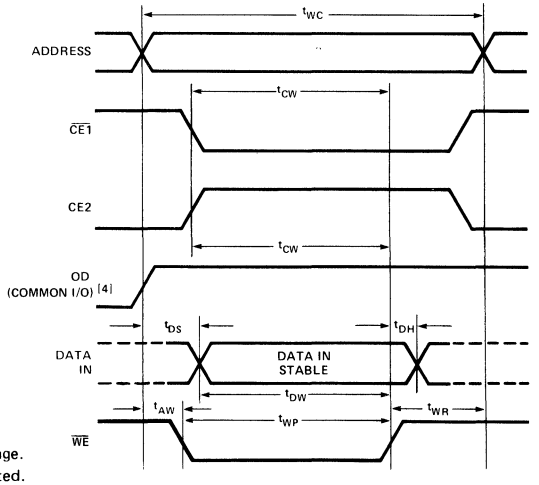
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.
4. OD should be tied low for separate I/O operation.

2101A (350 ns ACCESS TIME)
A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	$t_r, t_f = 20ns$ Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and $C_L = 100pF$.
t_A	Access Time			350	ns	
t_{CO}	Chip Enable To Output			240	ns	
t_{OD}	Output Disable To Output			180	ns	
t_{DF} [2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	220			ns	$t_r, t_f = 20ns$ Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and $C_L = 100pF$.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	200			ns	
t_{DW}	Data Setup	200			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	200			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

2101A-4 (450 ns ACCESS TIME)
A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	$t_r, t_f = 20ns$ Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and $C_L = 100pF$.
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	$t_r, t_f = 20ns$ Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and $C_L = 100pF$.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.

2102A, 2102AL/8102A-4*
1K x 1 BIT STATIC RAM

P/N	Standby Pwr. (mW)	Operating Pwr. (mW)	Access (ns)
2102AL-4	35	174	450
2102AL	35	174	350
2102AL-2	42	342	250
2102A-2	—	342	250
2102A	—	289	350
2102A-4	—	289	450

- **Single +5 Volts Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Standby Power Mode (2102AL)**
- **Three-State Output: OR-Tie Capability**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Dual-In-Line Configuration**

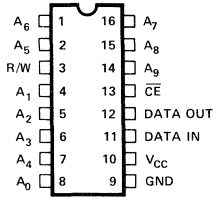
The Intel® 2102A is a high speed 1024 word by one bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. *A low standby power version (2102AL) is also available. It has all the same operating characteristics of the 2102A with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.*

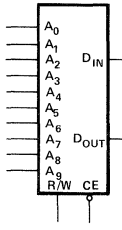
It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2102A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



LOGIC SYMBOL



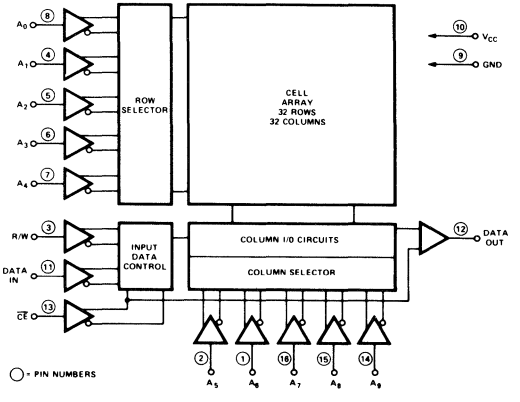
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

BLOCK DIAGRAM



*All 8102A-4 specifications are identical to the 2102A-4 specifications.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect To Ground	−0.5V to +7V
Power Dissipation	1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	2102A, 2102A-4, 2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102A-2, 2102AL-2 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current		1	5		1	5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = V_{OH}
I_{LOL}	Output Leakage Current		-1	-10		-1	-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC}	Power Supply Current		33	Note 2		45	65	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = -100μA

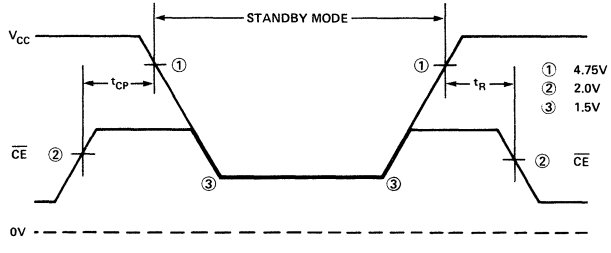
Notes: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. The maximum I_{CC} value is 55mA for the 2102A and 2102A-4, and 33mA for the 2102AL and 2102AL-4.

Standby Characteristics 2102AL, 2102AL-2, and 2102AL-4 (Available only in the Plastic Package)

T_A = 0°C to 70°C

Symbol	Parameter	2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102AL-2 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	1.5			1.5			V	
V_{CES}[2]	$\overline{CE}$ Bias in Standby	2.0			2.0			V	2.0V≤V_{PD}≤V_{CC} Max.
		V_{PD}			V_{PD}			V	1.5V≤V_{PD}< 2.0V
I_{PD1}	Standby Current		15	23		20	28	mA	All Inputs = V_{PD1} = 1.5V
I_{PD2}	Standby Current		20	30		25	38	mA	All Inputs = V_{PD2} = 2.0V
t_{CP}	Chip Deselect to Standby Time	0			0			ns	
t_R[3]	Standby Recovery Time	t_{RC}			t_{RC}			ns	

STANDBY WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min.), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
3. t_R = t_{RC} (READ CYCLE TIME).

A. C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

READ CYCLE

Symbol	Parameter	2102A-2, 2102AL-2 Limits (ns) Min.	Max.	2102A, 2102AL Limits (ns) Min.	Max.	2102A-4, 2102AL-4 Limits (ns) Min.	Max.
t_{RC}	Read Cycle	250		350		450	
t_A	Access Time		250		350		450
t_{CO}	Chip Enable to Output Time		130		180		230
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0	

WRITE CYCLE

t_{WC}	Write Cycle	250	350	450
t_{AW}	Address to Write Setup Time	20	20	20
t_{WP}	Write Pulse Width	180	250	300
t_{WR}	Write Recovery Time	0	0	0
t_{DW}	Data Setup Time	180	250	300
t_{DH}	Data Hold Time	0	0	0
t_{CW}	Chip Enable to Write Setup Time	180	250	300

A. C. CONDITIONS OF TEST

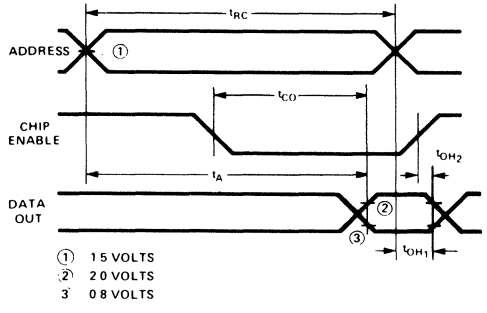
Input Pulse Levels:		0.8 Volt to 2.0 Volt
Input Rise and Fall Times:		10nsec
Timing Measurement Reference Levels	Inputs:	1.5 Volts
	Output:	0.8 and 2.0 Volts
Output Load:		1 TTL Gate and C_L = 100 pF

Capacitance[2] T_A = 25°C, f = 1MHz

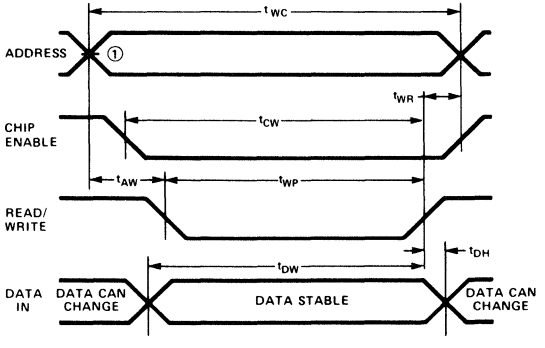
SYMBOL	TEST	LIMITS (pF) TYP.[1]	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) V_{IN} = 0V	3	5
C_{OUT}	OUTPUT CAPACITANCE V_{OUT} = 0V	7	10

Waveforms

READ CYCLE



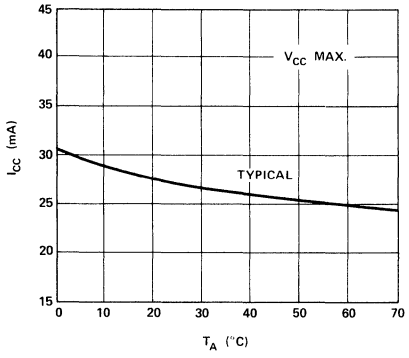
WRITE CYCLE



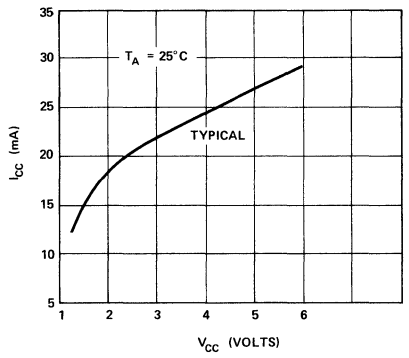
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Typical D. C. and A. C. Characteristics

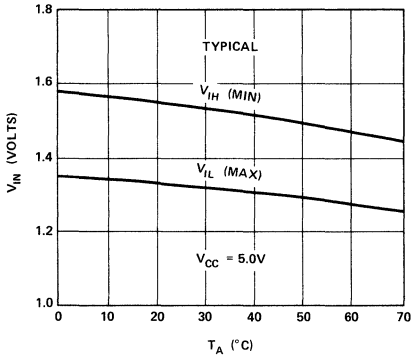
POWER SUPPLY CURRENT VS.
AMBIENT TEMPERATURE



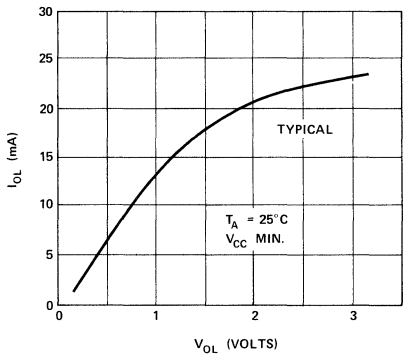
POWER SUPPLY CURRENT VS.
SUPPLY VOLTAGE



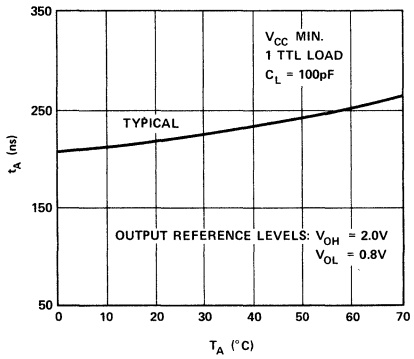
V_{IN} LIMITS VS. TEMPERATURE



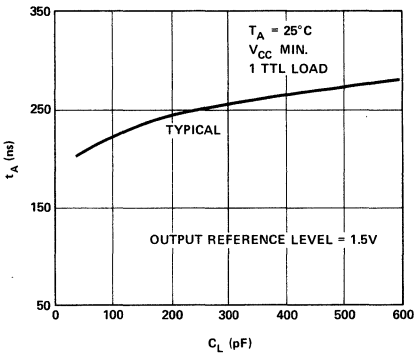
OUTPUT SINK CURRENT VS.
OUTPUT VOLTAGE



ACCESS TIME VS.
AMBIENT TEMPERATURE



ACCESS TIME VS.
LOAD CAPACITANCE



2104A
4096 x 1 BIT DYNAMIC RAM

	2104A
Max. Access Time (ns)	350
Read, Write Cycle (ns)	500
Max. IDD (mA)	35

- **Highest Density 4K RAM Industry Standard 16 Pin Package**
- **Low Power 4K RAM**
- **All Inputs Including Clocks TTL Compatible**
- **Standard Power Supplies: +12V, +5V, -5V**
- **Refresh Period: 2 ms**
- **On-Chip Latches for Addresses, Chip Select and Data In**
- **Simple Memory Expansion: Chip Select**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **Compatible with Intel® 2116 16K RAM**

The Intel® 2104A is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density.

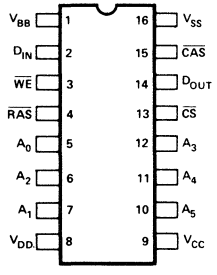
The efficient design of the 2104A allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104A on 6 address input pins. The two 6 bit address words are latched into the 2104A by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

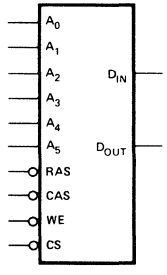
A new unique dynamic storage cell provides high speed along with low power dissipation and wide voltage margins. The memory cell requires refreshing for data retention. Refreshing is easily accomplished by performing any $\overline{RAS}/\overline{CAS}$ cycle with $\overline{CS}$ at V_{IH} for each of the 64 row addresses every 2 milliseconds.

The 2104A is designed for $\overline{CAS}$-only deselect and is compatible with Intel® 2116, 16K RAM.

PIN CONFIGURATION



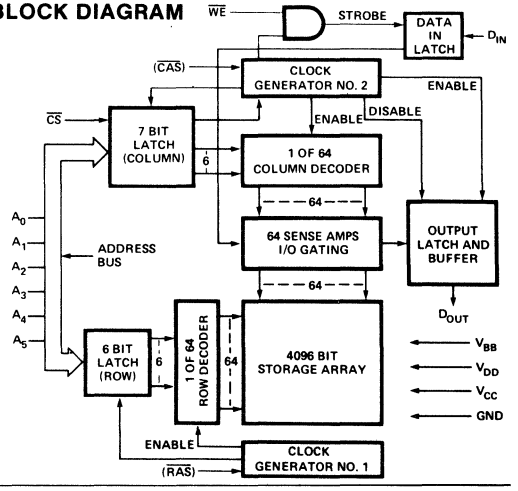
LOGIC DIAGRAM



PIN NAMES

$A_0 - A_5$	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - V_{BB} ≥ 4.5V) ..... -0.3V to +20V
Power Dissipation 1.0W
Data Out Current ..... 50 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (Any Input)			10	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			10	μA	Chip Deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V
I_{DD1}[3]	V_{DD} Standby Current		0.7	2	mA	V_{DD} = 12.6V, $\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip Deselected Prior to Measurement. See Note 5.
I_{BB1}	V_{BB} Standby Current		5	50	μA	
I_{DD2}[3]	Operating V_{DD} Current		25	35	mA	t_{CYC} = 500 ns
I_{BB2}	Operating V_{BB} Current		130	400	μA	t_{RC} = 500ns, T_A = 0°C
I_{CC1}[4]	V_{CC} Supply Current When Deselected			10	μA	
V_{IL}	Input Low Voltage (Any Input)	-1.0		0.8	V	
V_{IH}	Input High Voltage	2.4		7.0	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA

CAPACITANCE[6] T_A = 25°C

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	3	7	pF	V_{IN} = V_{SS}
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{WRITE}$	3	7	pF	V_{IN} = V_{SS}
C_O	Output Capacitance (D_{OUT})	4	7	pF	V_{OUT} = 0V
C_{I3}	Input Capacitance $\overline{CAS}$	6	7	pF	V_{IN} = V_{SS}

Notes:
1. All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycles containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} current flows to V_{SS}.
4. When chip is selected V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.
5. The chip is deselected; i.e., output is brought to high impedance state by $\overline{CAS}$-only cycle or by a read cycle with $\overline{CS}$ at V_{IH}.
6. Capacitance measured with Boonton Meter.

A.C.CHARACTERISTICS[1]

T_A = 0°C to 70°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

READ, WRITE, AND READ MODIFY WRITE CYCLES

Symbol	Parameter	2104A		Unit
		Min.	Max.	
t_{REF}	Time Between Refresh		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	150		ns
t_{CP}	$\overline{CAS}$ Precharge Time	150		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	100	150	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	200		ns
t_{CSH}	$\overline{CAS}$ Hold Time	350		ns
t_{AR}	$\overline{RAS}$ to Address or $\overline{CS}$ Hold Time	250		ns
t_{ASR}	Row Address Set-Up Time	0		ns
t_{ASC}	Column Address or $\overline{CS}$ Set-Up Time	0		ns
t_{RAH}	Row Address Hold Time	100		ns
t_{CAH}	Column Address or $\overline{CS}$ Hold Time	100		ns
t_T	Rise or Fall Time	3	50	ns
t_{OFF}	Output Buffer Turn-Off Delay	0	100	ns
t_{CAC}[3]	Access Time From $\overline{CAS}$		200	ns
t_{RAC}[3]	Access Time from $\overline{RAS}$		350	ns

READ CYCLE

Symbol	Parameter	2104A		Unit
		Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	500		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	350	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	200		ns
t_{RCS}	Read Command Set-Up Time	0		ns
t_{RCH}	Read Command Time	0		ns
t_{DOH}	Data Out Hold Time	32		μs

WRITE CYCLE[4]

Symbol	Parameter	2104A		Unit
		Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	500		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	350	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	200		ns
t_{WCS}	Write Command Set-Up Time	0		ns
t_{WCH}	Write Command Hold Time	100		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	250		ns
t_{WP}	Write Command Pulse Width	100		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	200		ns
t_{DS}	Data-In Set-Up Time	0		ns
t_{DH}	Data-In Hold Time	100		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	250		ns

Notes: 1. All voltages referenced to V_{SS}. Minimum timings do not allow for t_T or skews.

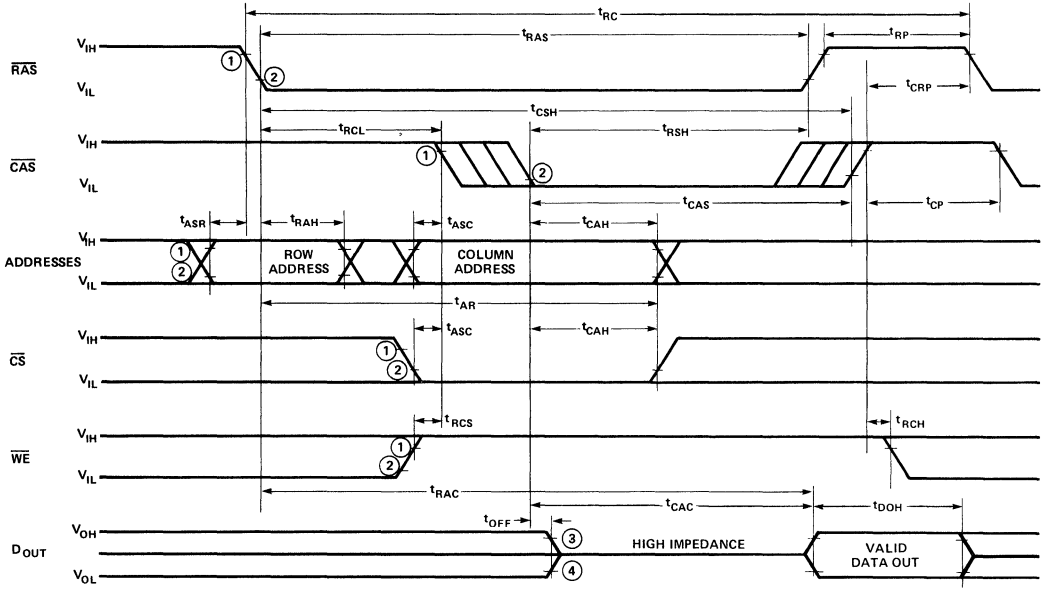
2. $\overline{CAS}$ must remain at V_{IH} a minimum of $t_{RCL\ MIN}$ after $\overline{RAS}$ switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before t_{RCL} of $t_{RAC} - t_T - t_{CAC}$ as described in the Applications Information section. $t_{RCL\ MAX}$ is given for reference only as $t_{RAC} - t_{CAC}$.

3. Load = 2 TTL and 100 pF. See Applications Information.

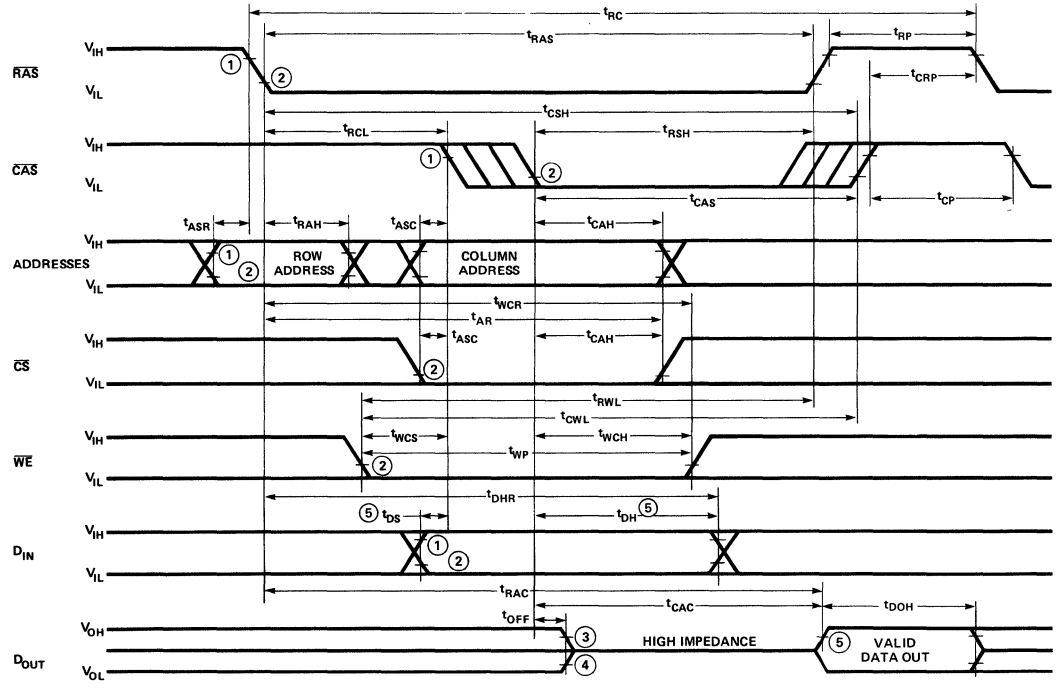
4. In a write cycle D_{OUT} latch will contain data written into cell. In a read-modify-write cycle D_{OUT} latch will contain data read from cell. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} is indeterminate.

WAVEFORMS

READ CYCLE



WRITE CYCLE



(See next page for notes)

A.C.CHARACTERISTICS[1]

T_A = 0°C to 70°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±10%, V_{BB} = –5V ±10%, V_{SS} = 0V, unless otherwise noted.

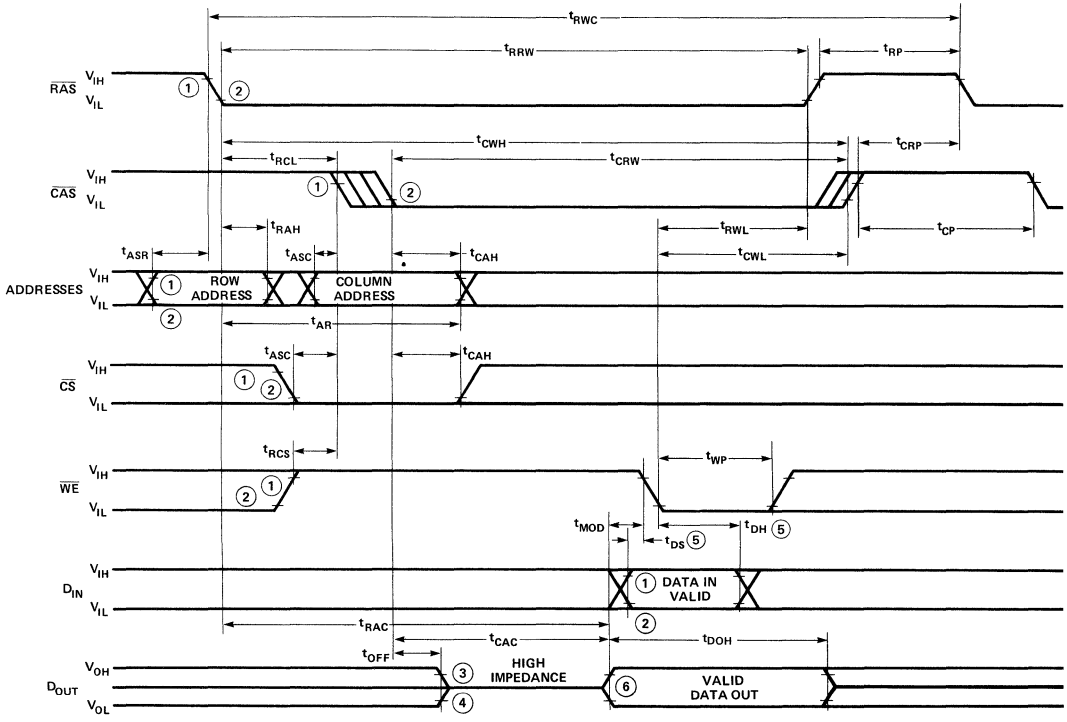
READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2104A		Unit
		Min.	Max.	
t_{RWC}	Read Modify Write Cycle Time[2]	700		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	400		ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	550		ns
t_{RWL}	RMW Cycle $\overline{RAS}$ Lead Time	200		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	550		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	200		ns
t_{WP}	Write Command Pulse Width	100		ns
t_{RCS}	Read Command Set-Up Time	0		ns
t_{MOD}	Modify Time	0	10	μs
t_{DS}	Data-In Set-Up Time	0		ns
t_{DH}	Data-In Hold Time	100		ns

Notes: 1. All voltages referenced to V_{SS}.
2. The minimum cycle timing does not allow for t_T or skews.

WAVEFORMS

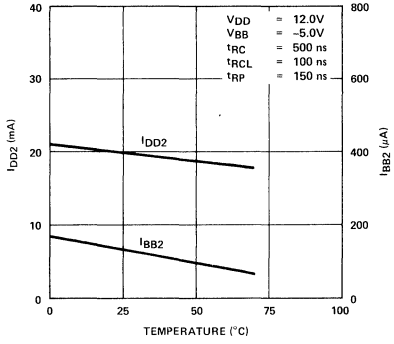
READ-MODIFY-WRITE CYCLE



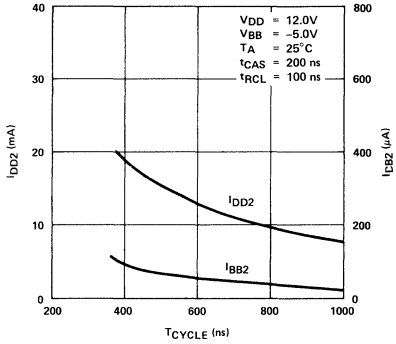
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
6. In a write cycle D_{OUT} latch will contain data written into cell. In a read-modify-write cycle D_{OUT} latch will contain data read from cell. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} is indeterminate.

TYPICAL CHARACTERISTICS

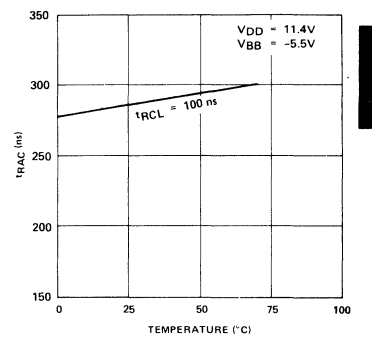
TYPICAL I_{BB2} AND I_{DD2} VS. TEMPERATURE



TYPICAL I_{BB2} AND I_{DD2} VS. CYCLE TIME



TYPICAL ACCESS TIME VS. TEMPERATURE



RAM

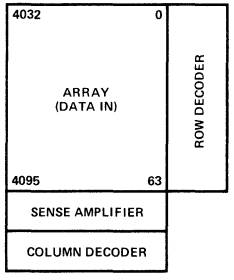
APPLICATIONS

ADDRESSING

Two externally applied negative going TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$), are used to strobe the two sets of 6 addresses into internal address buffer registers. The first clock, $\overline{RAS}$, strobes in the six low order addresses (A_0-A_5) which selects one of 64 rows and begins the timing which enables the column sense amplifiers. The second clock, $\overline{CAS}$, strobes in the six high order addresses (A_6-A_{11}) to select one of 64 column sense amplifiers and Chip Select ($\overline{CS}$) which enables the data out buffer.

An address map of the 2104A is shown below. Address "0" corresponds to all addresses at V_{IL}. All addresses are sequentially located on the chip.

2104A Address Map



DATA CYCLES/TIMING

A memory cycle begins with addresses stable and a negative transition of $\overline{RAS}$. See the waveforms on page 4. It is not necessary to know whether a Read or Write cycle is to be performed until $\overline{CAS}$ becomes valid.

Note that Chip Select ($\overline{CS}$) does not have to be valid until the second clock, $\overline{CAS}$. It is, therefore, possible to start a memory cycle before it is known which device must be selected. This can result in a significant improvement in system access time since the decode time for chip select does not enter into the calculation for access time.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks are TTL compatible and do not require level shifting and driving at high voltage MOS levels. Buffers internal to the 2104A convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104A system access time.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during $\overline{CAS}$. The output pin of a selected device will unconditionally go to a high impedance state immediately following the leading edge of $\overline{CAS}$ and remain in this state until valid data appears at the output at access time. The selected output data is internally latched and will remain valid until a subsequent $\overline{CAS}$ is given to the device by a Read, Write, Read-Modify-Write, $\overline{CAS}$ only or Refresh cycle. Data-out goes to a high impedance state for all non-selected devices.

Device access time, t_{ACC}, is the longer of two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCL} + t_T + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe lead time, t_{RCL}, and transition time, t_T, are system dependent timing parameters. For example, substituting the device parameters of the 2104A and assuming a TTL level transition time of 5 ns yields:

3. $t_{ACC} = t_{RAC} = 350$ ns for 100 nsec $\leqslant t_{RCL} \leqslant$ 145 nsec
   OR
4. $t_{ACC} = t_{RCL} + t_T + t_{CAC} = t_{RCL} + 205$ ns for $t_{RCL} > 145$ ns.

Note that if 100 nsec $\leqslant t_{RCL} \leqslant$ 145 nsec, device access time is determined by equation 3 and is equal to t_{RAC}. If $t_{RCL} >$ 145 nsec, access time is determined by equation 4. This 45 ns interval (shown in the t_{RCL} inequality in equation 3) in which the failing edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$. This allowance for a t_{RCL} skew is designed in at the device level to allow minimum access times to be achieved in practical designs.

WRITE CYCLE

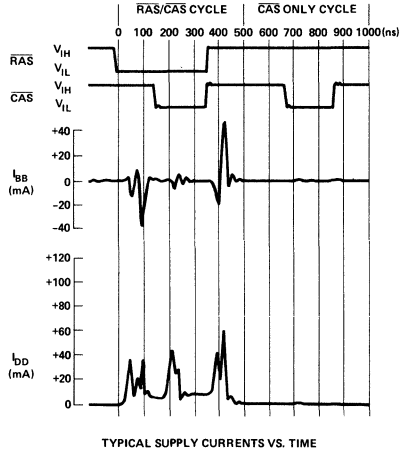
A Write Cycle is generally performed by bringing Write Enable ($\overline{WE}$) low before $\overline{CAS}$. D_{OUT} will be the data written into the cell addressed. If $\overline{WE}$ goes low after $\overline{CAS}$ and prior to t_{CAC}, D_{OUT} will be indeterminate.

READ-MODIFY-WRITE CYCLE

A Read-Modify-Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low after access time, t_{RAC}, with $\overline{RAS}$ and $\overline{CAS}$ low. Data in must be valid at or before the falling edge of $\overline{WE}$. In a read-modify-write cycle D_{OUT} is data read and does not change during the modify-write portion of the cycle.

$\overline{CAS}$ ONLY (DESELECT) CYCLE

In some applications, it is desirable to be able to deselect all memory devices without running a regular memory cycle. This may be accomplished with the 2104A by performing a $\overline{CAS}$-Only Cycle. Receipt of a $\overline{CAS}$ without $\overline{RAS}$ deselects the 2104A and forces the Data Output to the high-impedance state. This places the 2104A in its lowest power, standby condition. I_{DD} will be about twice I_{DD1} for the first cycle of $\overline{CAS}$-only deselection and I_{DD1} for any additional $\overline{CAS}$-only cycles. The cycle timing and $\overline{CAS}$ timing should be just as if a normal $\overline{RAS}/\overline{CAS}$ cycle was being performed.



TYPICAL SUPPLY CURRENTS VS. TIME

CHIP SELECTION/DESELECTION

The 2104A is selected by driving $\overline{CS}$ low during a Read, Write, or Read-Modify-Write cycle. A device is deselected by 1) driving $\overline{CS}$ high during a Read, Write, or Read-Modify-Write cycle or 2) performing a $\overline{CAS}$ Only cycle independent of the state of $\overline{CS}$.

REFRESH CYCLES

Each of the 64 rows internal to the 2104A must be refreshed every 2 msec to maintain data. Any data cycle (Read, Write, Read-Modify-Write) refreshes the entire selected row (defined by the low order row addresses). The refresh operation is independent of the state of chip select. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected ($\overline{CS}$ high) if it is desired not to change the state of the selected cell.

$\overline{RAS}/\overline{CAS}$ TIMING

The device clocks, $\overline{RAS}$ and $\overline{CAS}$, control operation of the 2104A. The timing of each clock and the timing relationships of the two clocks must be understood by the user in order to obtain maximum performance in a memory system.

The $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle must not begin until the minimum precharge time, t_{RP}, has been met.

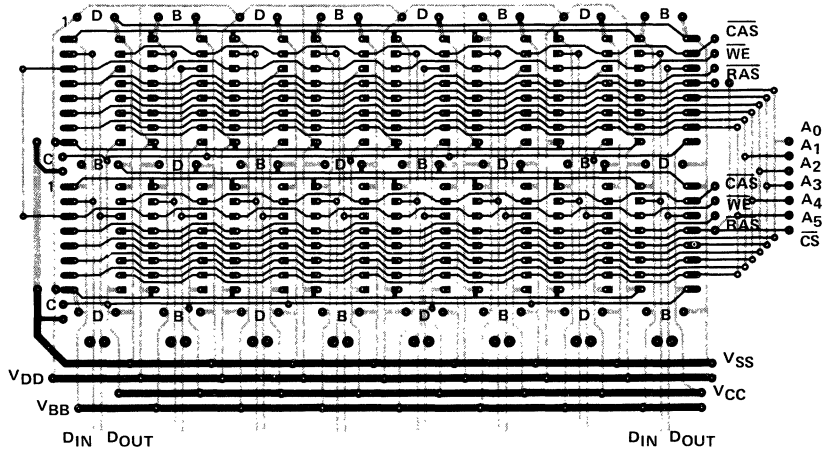
POWER SUPPLY

Typical power supply current waveforms versus time are shown below for both a $\overline{RAS}/\overline{CAS}$ cycle and a $\overline{CAS}$ only cycle. I_{DD} and I_{BB} current surges at $\overline{RAS}$ and $\overline{CAS}$ edges make adequate decoupling of these supplies important. Due to the high frequency noise component content of the current waveforms, the decoupling capacitors should be low inductance, ceramic units selected for their high frequency performance.

It is recommended that a 0.1 μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1 μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10 μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

A 0.01 μF ceramic capacitor is recommended between V_{CC} and V_{SS} at every eighth device to prevent noise coupling to the V_{CC} line which may affect the TTL peripheral logic in the system.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double-sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1 μF to V_{DD} TO V_{SS}
B = 0.1 μF V_{BB} TO V_{SS}
C = 0.01 μF V_{CC} TO V_{SS}

2104A FAMILY
4096 x 1 BIT DYNAMIC RAM

	2104A-1	2104A-2	2104A-3	2104A-4
Max. Access Time (ns)	150	200	250	300
Read, Write Cycle (ns)	320	375	375	425
Max. IDD (mA)	35	32	30	30

- **Highest Density 4K RAM Industry Standard 16 Pin Package**
- **Low Power 4K RAM: 462mW Operating 27mW Standby**
- **All Inputs Including Clocks TTL Compatible**
- **±10% Tolerance on All Power Supplies +12V, +5V, -5V**
- **Refresh Period: 2 ms**
- **On-Chip Latches for Addresses, Chip Select and Data In**
- **Simple Memory Expansion: Chip Select**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **$\overline{RAS}$-Only Refresh Operation**

The Intel® 2104A is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density.

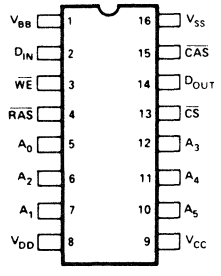
The efficient design of the 2104A allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104A on 6 address input pins. The two 6 bit address words are latched into the 2104A by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

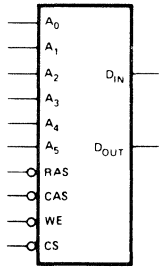
A new unique dynamic storage cell provides high speed along with low power dissipation and wide voltage margins. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a $\overline{RAS}$-only refresh cycle or read cycle at each of the 64 row addresses every 2 milliseconds.

The 2104A is designed for page mode operation, $\overline{RAS}$-only refresh, and $\overline{CAS}$-only deselect.

PIN CONFIGURATION



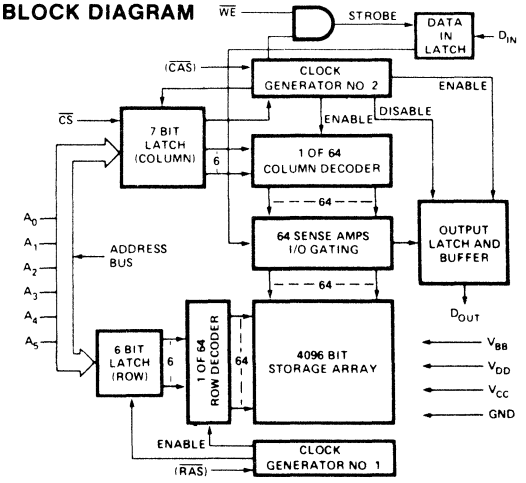
LOGIC DIAGRAM



PIN NAMES

A_0 A_5	ADDRESS INPUTS	WE	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin Relative to V_{BB}
(V_{SS} - V_{BB} ≥ 4.5V) ..... -0.3V to +20V
Power Dissipation 1.0W
Data Out Current ..... 50 mA

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

T_A = 0° to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits Min.	Typ.(2)	Max.	Unit	Conditions
I_{LI}	Input Load Current (any input)			10	µA	V_{IN} = V_{SS} to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			10	µA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH}; V_{OUT} = 0 to 5.5V
I_{DD1}[3]	V_{DD} Standby Current		0.7	2	mA	V_{DD} = 13.2V; $\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip deselected prior to measurement. See Note 5.
			0.7	1.5	mA	V_{DD} = 12.6V
I_{BB1}	V_{BB} Standby Current		5	50	µA	V_{DD} = 13.2V
I_{DD2}[3]	Operating V_{DD} Current		24	35	mA	2104A-1 t_{RC} = $t_{RC\ MIN}$
			22	32	mA	2104A-2 t_{RC} = $t_{RC\ MIN}$
			20	30	mA	2104A-3, 2104A-4 t_{RC} = $t_{RC\ MIN}$
I_{BB2}	Operating V_{BB} Current		130	325	µA	Min cycle time. T_A = 0°C
I_{CC1}[4]	V_{CC} Supply Current when Deselected			10	µA	
I_{DD3}	Operating V_{DD} Current ($\overline{RAS}$-only cycle)		12	25	mA	2104A-1, 2104A-2 t_{RC} = $t_{RC\ MIN}$
			10	22	mA	2104A-3, 2104A-4 t_{RC} = $t_{RC\ MIN}$
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V	
V_{IH}	Input High Voltage (any input)	2.4		7.0	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA

CAPACITANCE[6] T_A = 25°C

Symbol	Test	Typ.	Max.	Unit	Conditions
C_{I1}	Input Capacitance (A_0-A_5, D_{IN}, $\overline{CS}$)	3	7	pF	V_{IN} = V_{SS}
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{WRITE}$)	3	7	pF	V_{IN} = V_{SS}
C_O	Output Capacitance (D_{OUT})	4	7	pF	V_{OUT} = 0V
C_{I3}	Input Capacitance ($\overline{CAS}$)	6	7	pF	V_{IN} = V_{SS}

Notes: 1. All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}. After the application of supply voltages or after extended periods of operation without clocks, the device must perform a minimum of one initialization cycle (any valid memory cycles containing both $\overline{RAS}$ and $\overline{CAS}$) prior to normal operation.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} current flows to V_{SS}.
4. When chip is selected V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.
5. The chip is deselected; i.e., output is brought to high impedance state by $\overline{CAS}$-only cycle or by a read cycle with $\overline{CS}$ at V_{IH}.
6. Capacitance measured with Boonton Meter.

A.C. CHARACTERISTICS[1,2]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, AND READ MODIFY WRITE CYCLES

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{REF}	Time Between Refresh		2		2		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		120		125		ns
t_{CP}	$\overline{CAS}$ Precharge Time	60		80		110		110		ns
t_{RCD}[3]	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	80	135	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		165		ns
t_{AR}	$\overline{RAS}$ to Address or $\overline{CS}$ Hold Time	95		120		160		215		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		0		ns
t_{ASC}	Column Address or $\overline{CS}$ Set-Up Time	-10		-10		-10		-10		ns
t_{RAH}	Row Address Hold Time	20		25		35		80		ns
t_{CAH}	Column Address or $\overline{CS}$ Hold Time	45		55		75		80		ns
t_T	Rise or Fall Time	3	50	3	50	3	50	3	50	ns
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	60	0	60	0	80	ns
t_{CAC}[4,5]	Access Time From $\overline{CAS}$		100		135		165		165	ns
t_{RAC}[4]	Access Time From $\overline{RAS}$		150		200		250		300	ns

READ CYCLE

Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		375		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000	300	10000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		135		165		165		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{RCH}	Read Command Hold Time	0		0		0		0		ns
t_{DOH}	Data Out Hold Time	10		10		10		10		μs

WRITE CYCLE

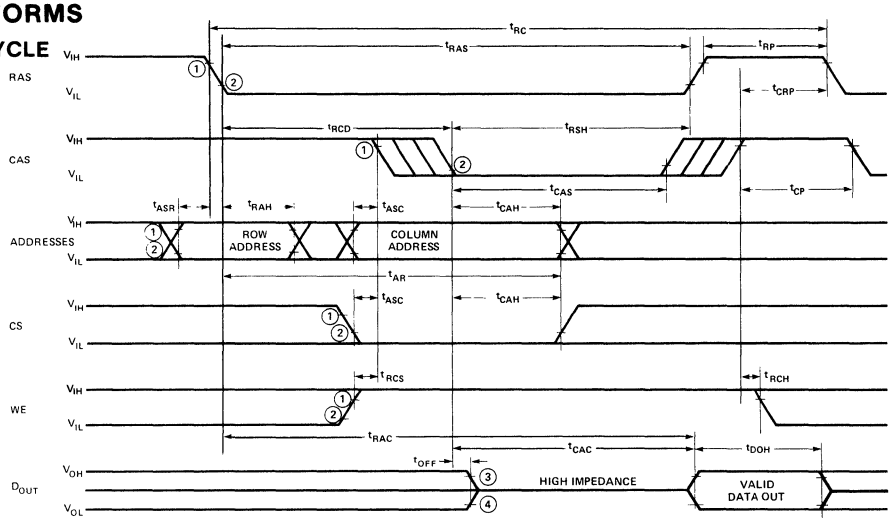
Symbol	Parameter	2104A-1		2104A-2		2104A-3		2104A-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Random Read or Write Cycle Time	320		375		375		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000	300	10000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	100		135		165		165		ns
t_{WCS}[6]	Write Command Set-Up Time	0		0		0		0		ns
t_{WCH}	Write Command Hold Time	45		55		75		80		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		215		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	50		70		85		130		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		70		85		130		ns
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		65		75		80		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		120		160		215		ns

NOTES:

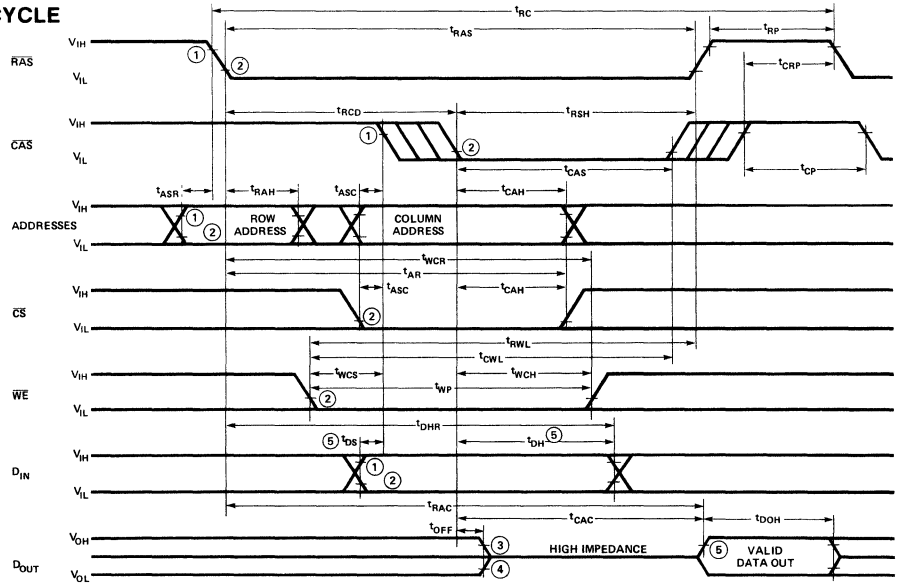
1. All voltages referenced to V_{SS}.
2. A.C. Characteristics assume t_T = 5ns.
3. $t_{RCD(MAX)}$ is specified as a reference point only; if $t_{RCD} \leq t_{RCD(MAX)}$ access time is t_{RAC}, if $t_{RCD} > t_{RCD(MAX)}$ access time is $t_{RCD} + t_{CAC}$.
4. Load = 2 TTL loads and 100pF.
5. Assumes $t_{RCD} \geq t_{RCD(MAX)}$.
6. In a write cycle with $t_{WCS} \geq t_{WCS(MIN)}$ the cycle is an early write cycle and D_{OUT} will be data written into the selected cell ($D_{OUT} = D_{IN}$). If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$ the cycle is a read-modify-write cycle and D_{OUT} will be data from the selected address read. If neither of the above conditions are satisfied, D_{OUT} is indeterminate.

WAVEFORMS

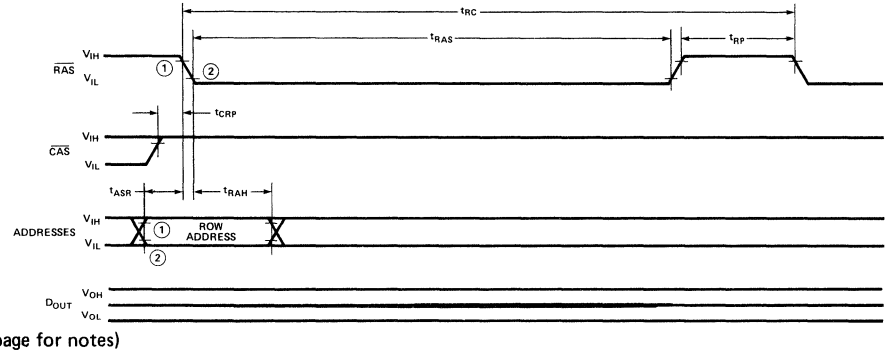
READ CYCLE



WRITE CYCLE



RAS-ONLY REFRESH CYCLE



(See next page for notes)

A.C.CHARACTERISTICS[7,8]

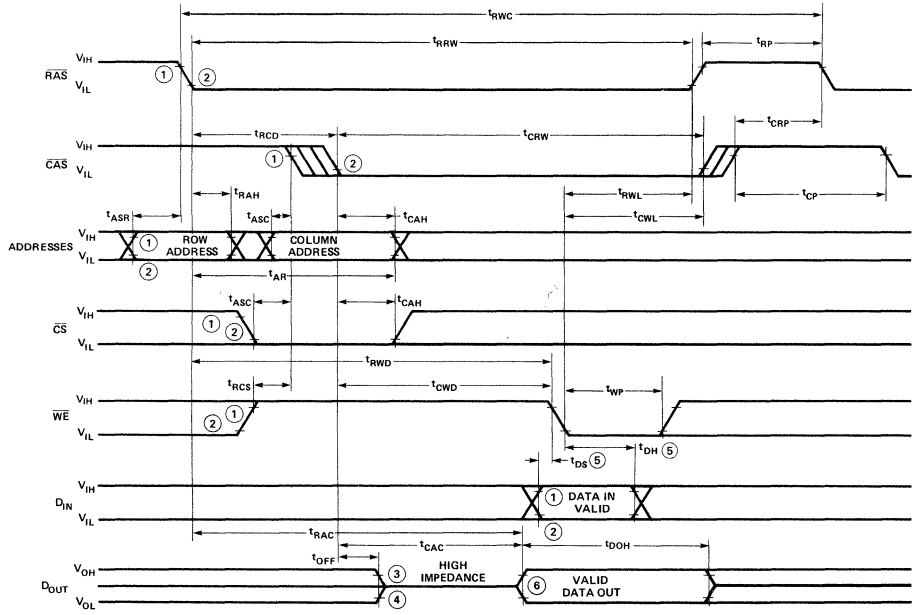
T_A = 0° to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2104A-1 Min.	2104A-1 Max.	2104A-2 Min.	2104A-2 Max.	2104A-3 Min.	2104A-3 Max.	2104A-4 Min.	2104A-4 Max.	Unit
t_{RWC}	Read Modify Write Cycle Time[2]	330		420		480		575		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	115		155		180		250		ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	165	10,000	220	10,000	265	10,000	385	10,000	ns
t_{RWL}	RMW Cycle $\overline{RAS}$ Lead Time	50		70		85		130		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		70		85		130		ns
t_{WP}	Write Command Pulse Width	45		55		75		80		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns
t_{RWD}[6]	$\overline{RAS}$ to $\overline{WE}$ Delay	110		145		175		250		ns
t_{CWD}[6]	$\overline{CAS}$ to $\overline{WE}$ Delay	60		80		90		115		ns
t_{DS}	Data-In Set-Up Time	0		0		0		0		ns
t_{DH}	Data-In Hold Time	55		65		75		80		ns

WAVEFORMS

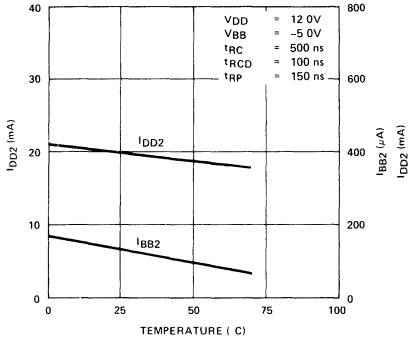
READ-MODIFY-WRITE CYCLE



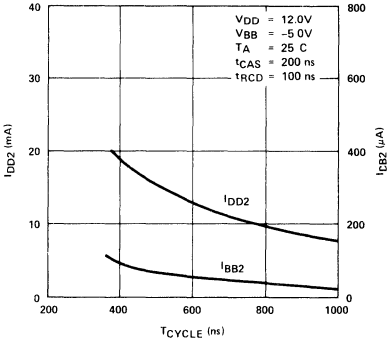
Notes:
1,2. V_{IHMIN} or V_{IHCMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. Referenced to CAS or WE, whichever occurs last.
6. In a write cycle with $t_{WCS} \geq t_{WCS(MIN)}$ the cycle is an early write cycle and D_{OUT} will be data written into the selected cell ($D_{OUT} = D_{IN}$). If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$ the cycle is a read-modify-write cycle and D_{OUT} will be data from the selected address read. If neither of the above conditions are satisfied, D_{OUT} is indeterminate.
7. All voltages referenced to V_{SS}.
8. A.C. Characteristics assume t_T = 5ns.

TYPICAL CHARACTERISTICS

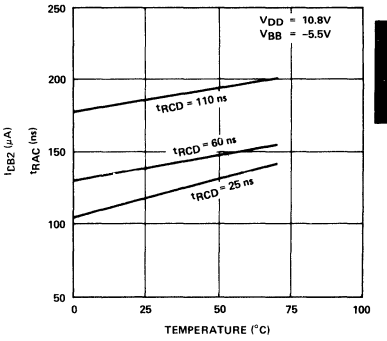
TYPICAL I_{BB2} AND I_{DD2} VS. TEMPERATURE



TYPICAL I_{BB2} AND I_{DD2} VS. CYCLE TIME



TYPICAL ACCESS TIME VS. TEMPERATURE



RAM

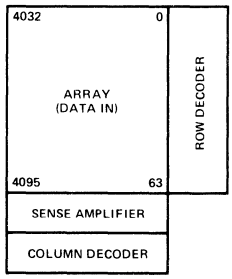
APPLICATIONS

ADDRESSING

Two externally applied negative going TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$), are used to strobe the two sets of 6 addresses into internal address buffer registers. The first clock, $\overline{RAS}$, strobes in the six low order addresses (A_0-A_5) which selects one of 64 rows and begins the timing which enables the column sense amplifiers. The second clock, $\overline{CAS}$, strobes in the six high order addresses (A_6-A_{11}) to select one of 64 column sense amplifiers and Chip Select ($\overline{CS}$) which enables the data out buffer.

An address map of the 2104A is shown below. Address "0" corresponds to all addresses at V_{IL}. All addresses are sequentially located on the chip.

2104A Address Map



DATA CYCLES/TIMING

A memory cycle begins with addresses stable and a negative transition of $\overline{RAS}$. See the waveforms on page 4. It is not necessary to know whether a Read or Write cycle is to be performed until $\overline{CAS}$ becomes valid.

Note that Chip Select ($\overline{CS}$) does not have to be valid until the second clock, $\overline{CAS}$. It is, therefore, possible to start a memory cycle before it is known which device must be selected. This can result in a significant improvement in system access time since the decode time for chip select does not enter into the calculation for access time.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks are TTL compatible and do not require level shifting and driving at high voltage MOS levels. Buffers internal to the 2104A convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104A system access time.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during $\overline{CAS}$. The output pin of a selected device will unconditionally go to a high impedance state immediately following the leading edge of $\overline{CAS}$ and remain in this state until valid data appears at the output at access time. The selected output data is internally latched and will remain valid for at least $t_{DOH\ MAX}$. A subsequent $\overline{CAS}$ must be given to the device either by a Read, Write, Read-Modify-Write, $\overline{CAS}$-only or $\overline{RAS}$/$\overline{CAS}$ refresh cycle.

Device access time, t_{ACC}, is the longer of two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCD} + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. $\overline{RAS}$ to $\overline{CAS}$ delay time, t_{RCD}, is a system dependent timing parameter. For example, substituting the device parameters to the 2104A-4 yields:

3. $t_{ACC} = t_{RAC} = 300ns$ for $80nsec \leq t_{RCD} \leq 135nsec$

OR

4. $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD} + 165ns$ for $t_{RCD} > 135ns$.

Note that if 80nsec ≤ t_{RCD} ≤ 135nsec, device access time is determined by equation 3 and is equal to t_{RAC}. If t_{RCD} > 135ns, access time is determined by equation 4. This 55ns interval (shown in the t_{RCD} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$. This allowance for a t_{RCD} skew is designed in at the device level to allow minimum access times to be achieved in practical system designs.

WRITE CYCLE

A Write Cycle is generally performed by bringing Write Enable ($\overline{WE}$) low before $\overline{CAS}$. D_{OUT} will be the data written into the cell addressed. If $\overline{WE}$ goes low after $\overline{CAS}$ but t_{CWD} < $t_{CWD\ MIN}$ and t_{RWD} < $t_{RWD\ MIN}$, D_{OUT} will be indeterminate.

READ-MODIFY-WRITE CYCLE

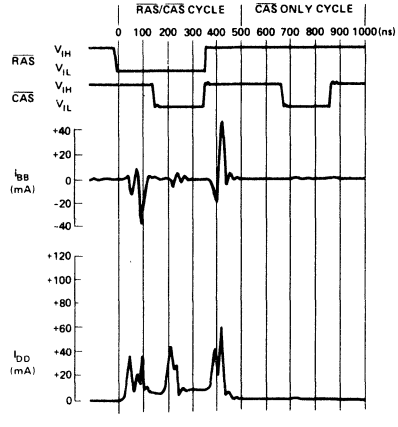
A Read-Modify-Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low during a selected $\overline{RAS}$/$\overline{CAS}$ cycle with $t_{RWD} \geq t_{RWD\ MIN}$ and $t_{CWD} \geq t_{CWD\ MIN}$. Data in must be valid at or before the falling edge of $\overline{WE}$. In a read-modify-write cycle D_{OUT} is data read from the selected cell and does not change during the modify-write portion of the cycle.

$\overline{CAS}$ ONLY (DESELECT) CYCLE

In some applications, it is desirable to be able to deselect all memory devices without running a regular memory cycle. This may be accomplished with the 2104A by performing a $\overline{CAS}$-Only Cycle. Receipt of a $\overline{CAS}$ without $\overline{RAS}$ deselects the 2104A and forces the Data Output to the high-impedance state. This places the 2104A in its lowest power, standby condition. I_{DD} will be about twice I_{DD1} for the first cycle of $\overline{CAS}$-only deselection and I_{DD1} for any additional $\overline{CAS}$-only cycles. The cycle timing and $\overline{CAS}$ timing should be just as if a normal $\overline{RAS}$/$\overline{CAS}$ cycle was being performed.

CHIP SELECTION/DESELECTION

The 2104A is selected by driving $\overline{CS}$ low during a Read, Write, or Read-Modify-Write cycle. A device is deselected by 1) driving $\overline{CS}$ high during a Read, Write, or Read-Modify-Write cycle or 2) performing a $\overline{CAS}$ Only cycle independent of the state of $\overline{CS}$.



TYPICAL SUPPLY CURRENTS VS TIME

REFRESH CYCLES

Each of the 64 rows internal to the 2104A must be refreshed every 2 msec to maintain data. Any cycle (Read, Write, Read-Modify-Write, $\overline{RAS}$-only refresh) refreshes the entire selected row (defined by the low order row addresses). The refresh operation is independent of the state of chip select. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected ($\overline{CS}$ high) if it is desired not to change the state of the selected cell.

$\overline{RAS}$/$\overline{CAS}$ TIMING

The device clocks, $\overline{RAS}$ and $\overline{CAS}$, control operation of the 2104A. The timing of each clock and the timing relationships of the two clocks must be understood by the user in order to obtain maximum performance in a memory system.

The $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle must not begin until the minimum precharge time, t_{RP}, has been met.

PAGE MODE OPERATION

The 2104A is designed for page mode operation. Product tested to page mode operating specifications are available upon request.

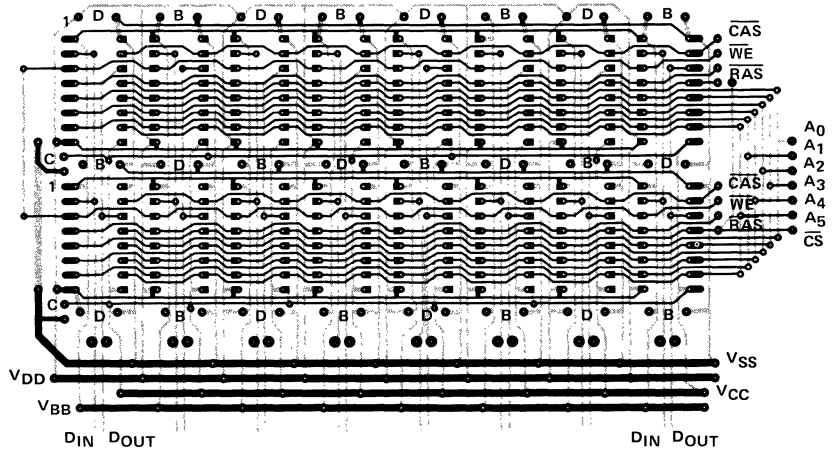
POWER SUPPLY

Typical power supply current waveforms versus time are shown below for both a $\overline{RAS}$/$\overline{CAS}$ cycle and a $\overline{CAS}$ only cycle. I_{DD} and I_{BB} current surges at $\overline{RAS}$ and $\overline{CAS}$ edges make adequate decoupling of these supplies important. Due to the high frequency noise component content of the current waveforms, the decoupling capacitors should be low inductance, ceramic units selected for their high frequency performance.

It is recommended that a 0.1 μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1 μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10 μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

A 0.01 μF ceramic capacitor is recommended between V_{CC} and V_{SS} at every eighth device to prevent noise coupling to the V_{CC} line which may affect the TTL peripheral logic in the system.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double-sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1 μF to V_{DD} TO V_{SS}
B = 0.1 μF V_{BB} TO V_{SS}
C = 0.01 μF V_{CC} TO V_{SS}

2107C FAMILY
4096-BIT DYNAMIC RAM

	2107C-1	2107C-2	2107C	2107C-4
Access Time (ns)	150	200	250	300
Read, Write Cycle (ns)	380	400	430	470
RMW Cycle (ns)	450	500	550	590
Max $I_{DD\ AV}$ (mA)	35	33	30	30

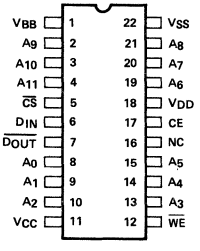
- **Direct Replacement for Industry Standard 22-Pin 4K RAMs**
- **Low Operating Power**
- **Low Standby Power**
- **Only One High Voltage Input Signal-Chip Enable**
- **150 ns Access Time**
- **± 10% Tolerance on all Power Supplies**
- **Output is Three-State and TTL Compatible**
- **TTL Compatible — All Address, Data, Write Enable, Chip Select Inputs**
- **Refresh Period 2 ms**

The Intel® 2107C is a 4096-word by 1-bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. A new unique dynamic storage cell provides high speed and wide operating margins. The 2107C uses dynamic circuitry which reduces the standby power dissipation.

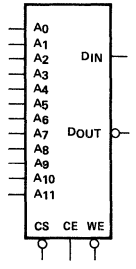
Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107C is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107C is a replacement for the 2107A, 2107B and other industry standard 22-pin 4K RAMs.

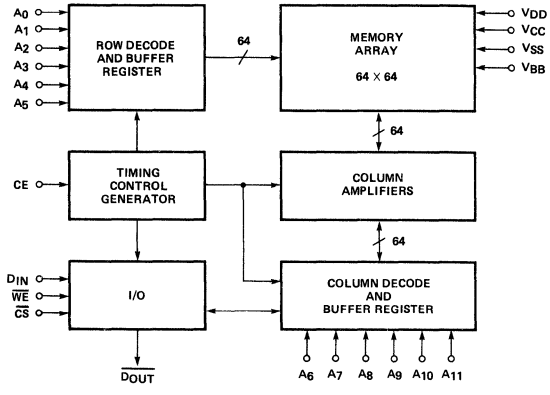
PIN CONFIGURATION
2107C



LOGIC SYMBOL
2107C



BLOCK DIAGRAM



PIN NAMES

A0–A11	ADDRESS INPUTS*	VBB	POWER (–5V)
CE	CHIP ENABLE	VCC	POWER (+5V)
CS	CHIP SELECT	VDD	POWER (+12V)
DIN	DATA INPUT	VSS	GROUND
DOUT	DATA OUTPUT	WE	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A0–A5.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage on any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5$) . . . . . -0.3V to +20V

Power Dissipation 1.00W

**COMMENT:*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB}[1] = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)			10	µA	V_{IN} = 0V to $V_{IH\ MAX}$ CE = V_{ILC} or V_{IHC}
I_{LC}	Input Load Current, CE			2	µA	V_{IN} = 0V to $V_{IHC\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state			10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.5V
I_{DD1}[3]	V_{DD} Supply Current – standby[3]		20	200	µA	CE = -1V to +0.6V
$I_{DD\ AV}$	Average V_{DD} Current – operating		24	35	mA	2107C-1, t_{CYC} = 380
			22	33	mA	2107C-2, t_{CYC} = 400
			20	30	mA	2107C, t_{CYC} = 430
			20	30	mA	2107C-4, t_{CYC} = 470
I_{CC1}[3,4]	V_{CC} Supply Current – standby			10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB1}	V_{BB} Supply Current – standby		5	50	µA	CE = -1V to +0.6V
$I_{BB\ AV}$	Average V_{BB} Current – operating		100	400	µA	Min. cycle time, Min. t_{CE}
V_{IL}	Input Low Voltage	-1.0		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.40	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -2.0 mA

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}.
4. During CE on V_{CC} supply current is dependent on output loading. V_{CC} is connected to output buffer only.

A.C. Characteristics [1]

$T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ, WRITE, AND READ MODIFY/WRITE CYCLE

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max	Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Time Between Refresh		2		2		2		2	ms	
t_{AC}	Address to CE Set-Up Time	0		0		0		0		ns	2
t_{AH}	Address Hold Time	50		50		100		100		ns	
t_{CC}	CE Off Time	130		130		130		130		ns	
t_T	CE Transition Time		40		40		40		40	ns	
t_{CD}	CE Off to Output Disable Time	30		30		30		30		ns	3

READ CYCLE

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	380		400		430		470		ns	3
t_{CE}	CE On Time	210	4000	230	4000	260	4000	300	4000	ns	
t_{CO}	CE Output Delay		130		180		230		280	ns	4
t_{ACC}	Address to Output Access		150		200		250		300	ns	5
t_{WL}	CE to $\overline{WE}$	0		0		0		0		ns	
t_{WC}	$\overline{WE}$ to CE On	0		0		0		0		ns	

WRITE CYCLE

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	380		400		430		470		ns	3
t_{CE}	CE On Time	210	4000	230	4000	260	4000	300	4000	ns	
t_W	$\overline{WE}$ to CE Off	125		125		125		175		ns	
t_{CW}	CE to $\overline{WE}$	150		150		150		200		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set-Up	0		0		0		0		ns	6
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		50		50		100		ns	
t_{WD}	$\overline{WE}$ to Output Disable Time	15		15		15		15			

Capacitance [7] $T_A = 25°C$

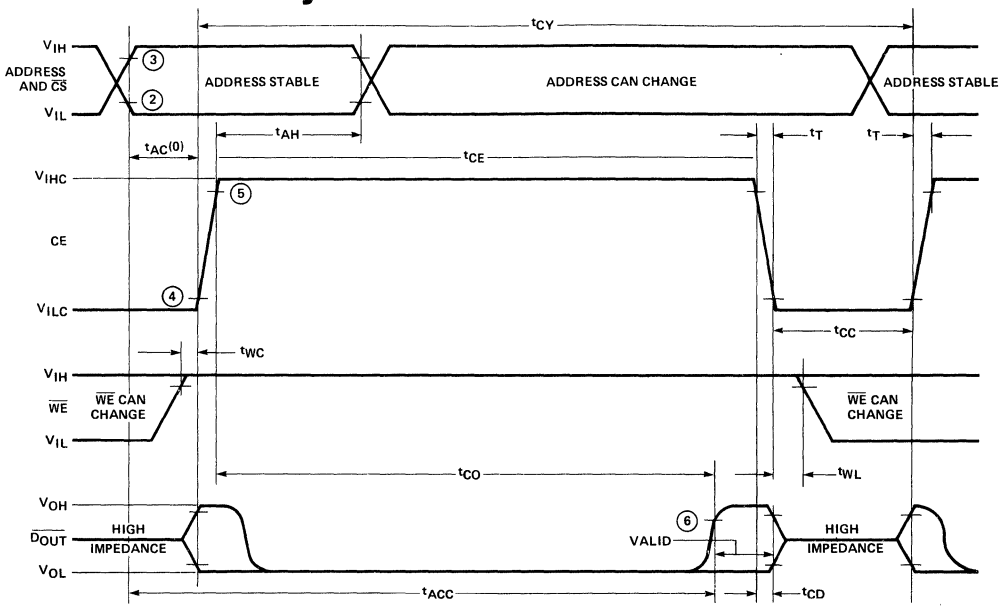
Symbol	Test	Plastic and Ceramic Package		Unit	Conditions
		Typ.	Max.		
C_{AD}	Address Capacitance, $\overline{CS}$, D_{IN}	5	7	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	10	15	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	5	7	pF	$V_{OUT} = 0V$
$C_{\overline{WE}}$	$\overline{WE}$ Capacitance	6	8	pF	$V_{IN} = V_{SS}$

NOTES:

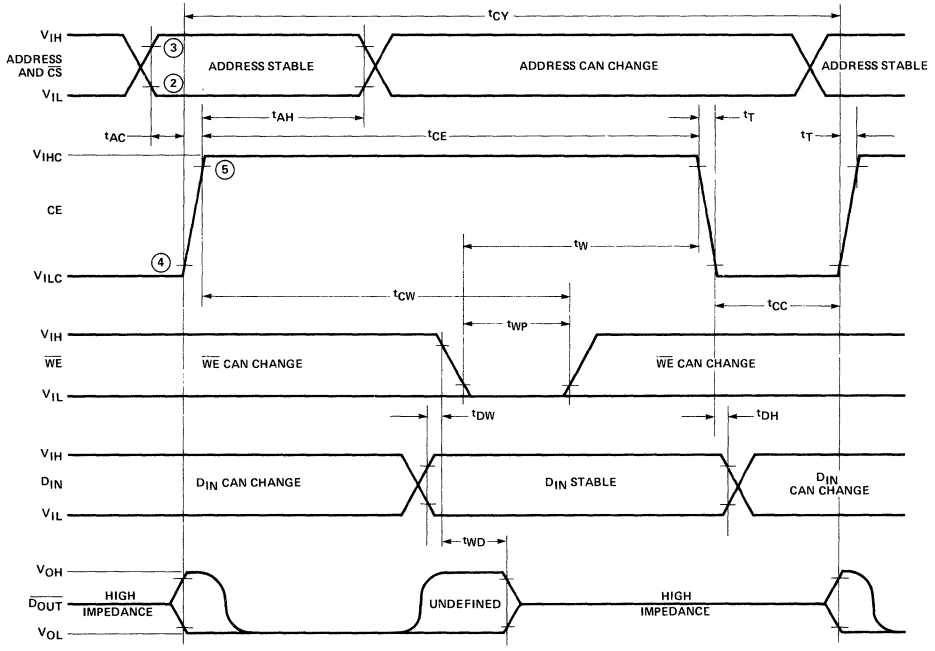
1. After the application of supply voltages or after extended periods of operation without CE, the device must perform a minimum of one initialization cycle (any valid memory cycle or refresh cycle) prior to normal operation.
2. t_{AC} is measured from end of address transition.
3. $t_T = 20$ ns.
4. $C_{LOAD} = 50$ pF, Load = One TTL Gate, Ref = 2.0V.
5. $t_{ACC} = t_{AC} + t_{CO} + 1t_T$.
6. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
7. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I\Delta t}{\Delta V}$$ with the current equal to a constant 20 mA.

Read and Refresh Cycle [1]



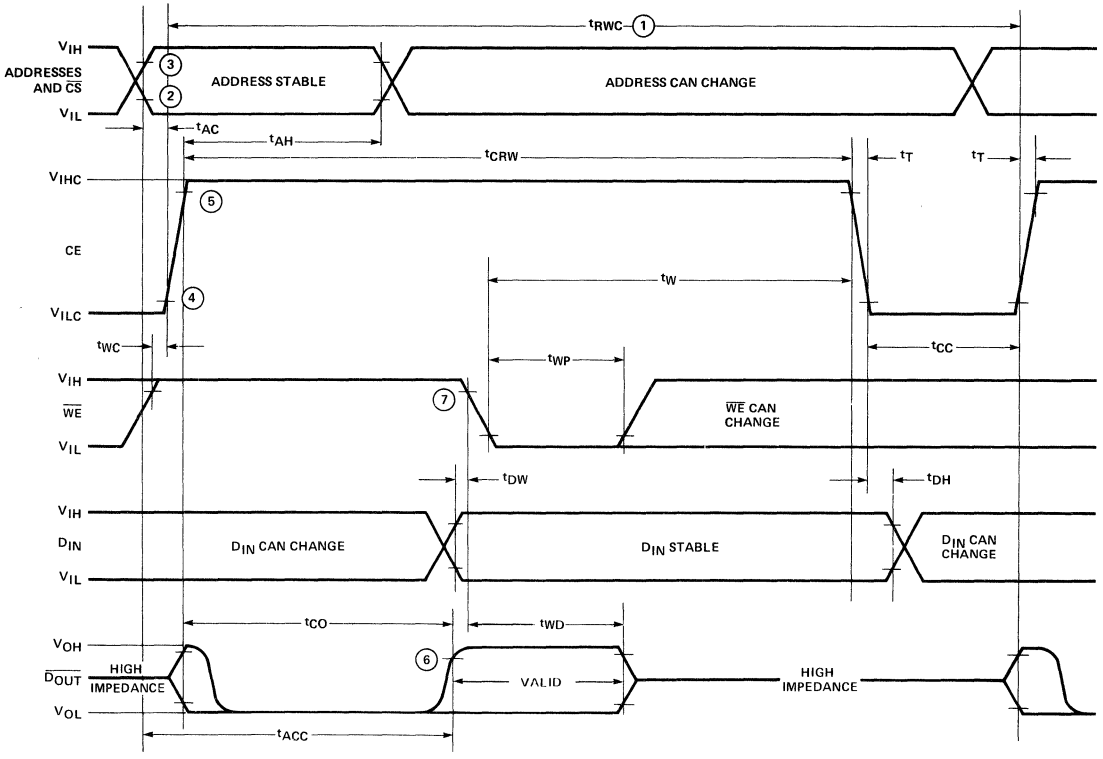
Write Cycle



NOTES:
1. For Refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IN} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} –2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.

Read Modify Write Cycle

Symbol	Parameter	2107C-1		2107C-2		2107C		2107C-4		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RWC}	Read Modify Write (RMW) Cycle	450		500		550		590		ns	1
t_{CRW}	CE Width During RMW	280	4000	330	4000	380	4000	420	4000	ns	
t_{WC}	$\overline{WE}$ to CE On	0		0		0		0		ns	
t_W	$\overline{WE}$ to CE Off	125		125		125		175		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		50		50		100		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Setup	0		0		0		0		ns	
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns	
t_{CO}	CE to Output Delay		130		180		230		280	ns	
t_{ACC}	Access Time		150		200		250		300	ns	
t_{WD}	$\overline{WE}$ to Output Disable Time	15		15		15		15		ns	



NOTES:
1. t_T of 20 ns.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} −2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$. C_{LOAD} = 50 pF. Load = One TTL Gate.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

2109 FAMILY
8,192 x 1 BIT DYNAMIC RAM

	2109-3 S6000,S6001	2109-4 S6002,S6003
Maximum Access Time (ns)	200	250
Read, Write Cycle (ns)	375	410
Read-Modify-Write Cycle (ns)	375	475

- **8K RAM, Industry Std. 16-Pin Package**
- **±10% Tolerance on All Power Supplies: +12V, +5V, -5V**
- **Low Power: 462mW Max. Operating, 20mW Max. Standby**
- **Low I_{DD} Current Transients**
- **All Inputs, Including Clocks, TTL Compatible**
- **Non-Latched Output is Three-State, TTL Compatible**
- **$\overline{RAS}$ Only Refresh**
- **64 Refresh Cycles Required Every 2ms**
- **Page Mode Capability**
- **$\overline{CAS}$ Controlled Output Allows Hidden Refresh**

The Intel® 2109 is a 8,192 word by 1-bit Dynamic MOS RAM which is pin compatible with the industry standard 16K dynamic RAMs. The 2109 is manufactured with the same masks as the Intel® 2117 and is fabricated with Intel's standard two layer polysilicon NMOS technology — a production proven process for high reliability, high performance, and high storage density. As is shown in the block diagram below, the device is organized as two 8K arrays separated by sense amplifiers and column decoders. The selected 8K array is tested for all of the A.C. and D.C. characteristics necessary to permit the 2109 to be considered a functionally compatible 8K version of the 16K device.

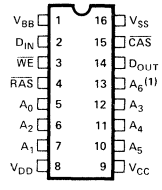
The 2109 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients and ±10% tolerance on all power supplies contribute to the high noise immunity of the 2109 in a system environment.

The 2109 is available as either an "upper" or "lower" half of the 2117. Row Address 6 (A_6) selects the operating half, and is V_{IH} for S6000, S6002, S6064 and S6066 specifications and A_6 is V_{IL} for S6001, S6003, S6065 and S6067 specifications.

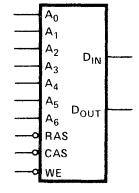
The 2109 three-state output is controlled by Column Address Strobe ($\overline{CAS}$) independent of Row Address Strobe ($\overline{RAS}$). After a valid read or read-modify-write cycle, data is latched on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The 2109 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain latched data while $\overline{RAS}$ is used to execute $\overline{RAS}$-Only refresh cycles.

The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing $\overline{RAS}$-Only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 64 row address combinations of A_0 through A_5. A_6 must be at its proper state (V_{IH} or V_{IL} depending on the device specification) for 64 cycle refresh. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

PIN CONFIGURATION



LOGIC SYMBOL

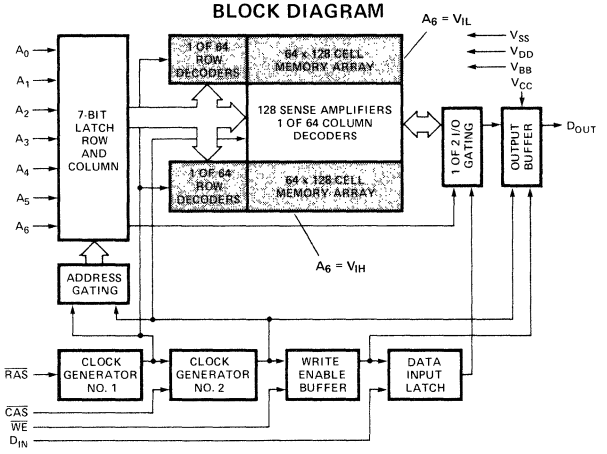


NOTE 1: S6000, S6002: A_6 AT V_{IH} DURING ROW ADDRESS VALID
S6001, S6003: A_6 AT V_{IL} DURING ROW ADDRESS VALID

PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin Relative to V_{BB}
($V_{SS} - V_{BB} \geq 4V$) ..... -0.3V to +20V
Data Out Current 50mA
Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

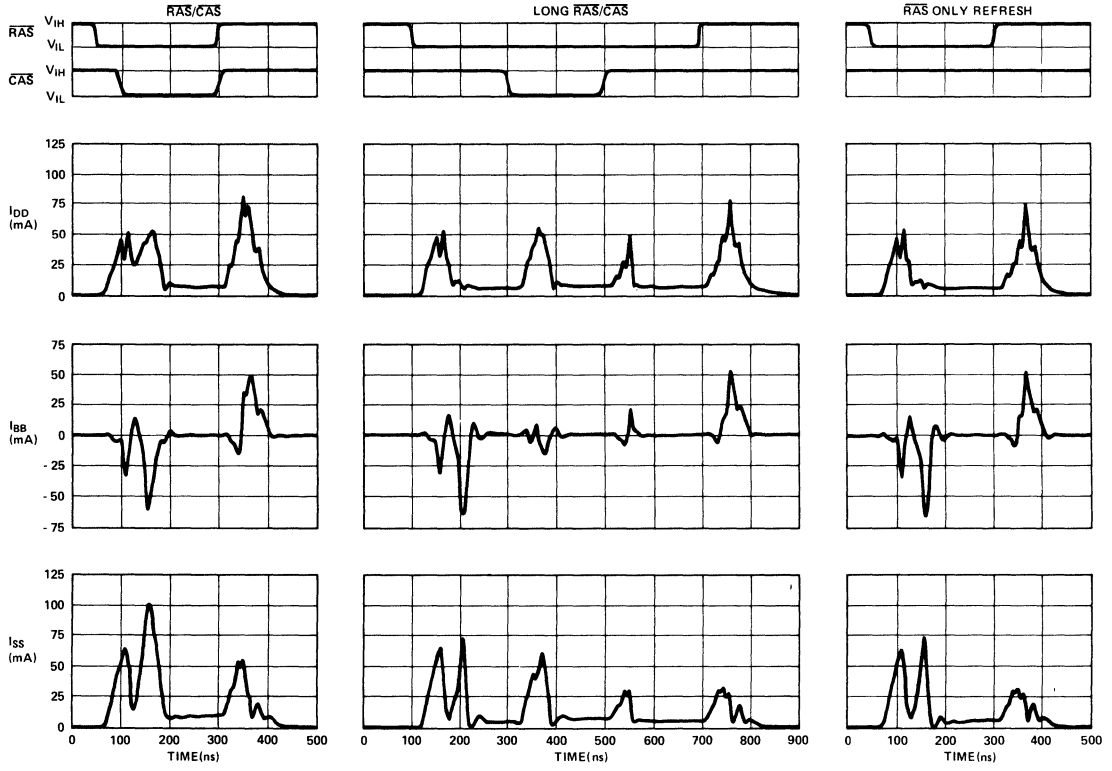
D.C. AND OPERATING CHARACTERISTICS[1,2]

T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits Min.	Typ.[3]	Max.	Unit	Test Conditions	Notes
$\|I_{LI}\|$	Input Load Current (any input)		0.1	10	µA	V_{IN}=V_{SS} to 7.0V, V_{BB}=-5.0V	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State		0.1	10	µA	Chip Deselected: $\overline{CAS}$ at V_{IH}, V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current, Standby			1.5	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	4
I_{BB1}	V_{BB} Supply Current, Standby		1.0	50	µA		
I_{CC1}	V_{CC} Supply Current, Output Deselected		0.1	10	µA	$\overline{CAS}$ at V_{IH}	5
I_{DD2}	V_{DD} Supply Current, Operating			35	mA	2109-3, t_{RC} = 375ns, t_{RAS} = 200ns	4
				33	mA	2109-4, t_{RC} = 410ns, t_{RAS} = 250ns	4
I_{BB2}	V_{BB} Supply Current, Operating, $\overline{RAS}$-Only Refresh, Page Mode		150	300	µA	T_A = 0°C	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh			27	mA	2109-3, t_{RC} = 375ns, t_{RAS} = 200ns	4
				26	mA	2109-4, t_{RC} = 410ns, t_{RAS} = 250ns	4
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		1.5	3	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	
V_{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		
V_{IH}	Input High Voltage (all inputs)	2.4		6.0	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2mA	4
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -5mA	4

NOTES:
1. All voltages referenced to V_{SS}.
2. No power supply sequencing is required. However, V_{DD}, V_{CC} and V_{SS} should never be more negative than -0.3V with respect to V_{BB} as required by the absolute maximum ratings.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. See the Typical Characteristics Section for values of this parameter under alternate conditions.
5. I_{CC} is dependent on output loading when the device output is selected. V_{CC} is connected to the output buffer only. V_{CC} may be reduced to V_{SS} without affecting refresh operation or maintenance of internal device data.

TYPICAL SUPPLY CURRENT WAVEFORMS



Typical power supply current waveforms vs. time are shown for the $\overline{RAS}/\overline{CAS}$ timings of Read/Write, Read/Write (Long $\overline{RAS}/\overline{CAS}$), and $\overline{RAS}$-only refresh cycles. I_{DD} and I_{BB} current transients at the $\overline{RAS}$ and $\overline{CAS}$ edges require adequate decoupling of these supplies. Decoupling recommendations are provided in the Applications section.

The effects of cycle time, V_{DD} supply voltage and ambient temperature on the I_{DD} current are shown in graphs included in the Typical Characteristics Section. Each family of curves for I_{DD1}, I_{DD2}, and I_{DD3} is related by a common point at $V_{DD} = 12.0V$ and $T_A = 25°C$ for two given t_{RAS} pulse widths. The typical I_{DD} current for a given condition of cycle time, V_{DD} and T_A can be determined by combining the effects of the appropriate family of curves.

CAPACITANCE[1]

$T_A = 25°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Typ.	Max.	Unit
C_{I1}	Address, Data In	3	5	pF
C_{I2}	$\overline{RAS}$ Capacitance, $\overline{WE}$ Capacitance	4	7	pF
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF
C_O	Data Output Capacitance	4	7	pF

NOTES:
1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
$C = \frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.

A.C. CHARACTERISTICS[1,2,3]

T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2109-3 S6000,S6001 Min.	2109-3 S6000,S6001 Max.	2109-4 S6002,S6003 Min.	2109-4 S6002,S6003 Max.	Unit	Notes
t_{RAC}	Access Time From $\overline{RAS}$		200		250	ns	4,5
t_{CAC}	Access Time From $\overline{CAS}$		135		165	ns	4,5,6
t_{REF}	Time Between Refresh		2		2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	120		150		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time(non-page cycles)	25		25		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	-20		-20		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	65	35	85	ns	7
t_{RSH}	$\overline{RAS}$ Hold Time	135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	200		250		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	25		35		ns	
t_{ASC}	Column Address Set-Up Time	-10		-10		ns	
t_{CAH}	Column Address Hold Time	55		75		ns	
t_{AR}	Column Address Hold Time, to $\overline{RAS}$	120		160		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{OFF}	Output Buffer Turn Off Delay	0	60	0	70	ns	

READ AND REFRESH CYCLES

t_{RC}	Random Read Cycle Time	375		410		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	200	10000	250	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	135	10000	165	10000	ns	
t_{RCS}	Read Command Set-Up Time	0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		ns	

WRITE CYCLE

t_{RC}	Random Write Cycle Time	375		410		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	200	10000	250	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	135	10000	165	10000	ns	
t_{WCS}	Write Command Set-Up Time	-20		-20		ns	9
t_{WCH}	Write Command Hold Time	55		75		ns	
t_{WCR}	Write Command Hold Time, to $\overline{RAS}$	120		160		ns	
t_{WP}	Write Command Pulse Width	55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	80		100		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	80		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		ns	
t_{DH}	Data-In Hold Time	55		75		ns	
t_{DHR}	Data-In Hold Time, to $\overline{RAS}$	120		160		ns	

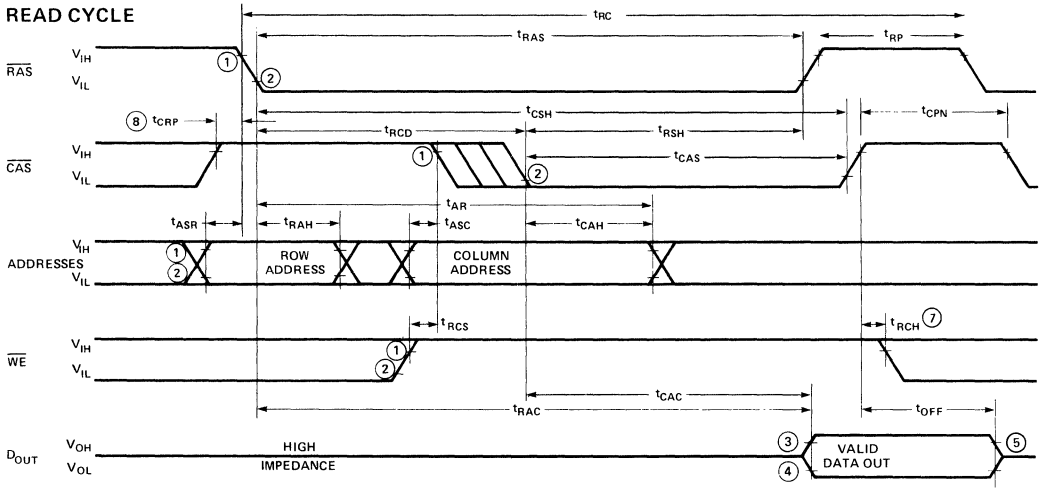
READ-MODIFY-WRITE CYCLE

t_{RWC}	Read-Modify-Write Cycle Time	375		475		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	245	10000	305	10000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	180	10000	230	10000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	160		200		ns	9
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	95		125		ns	9

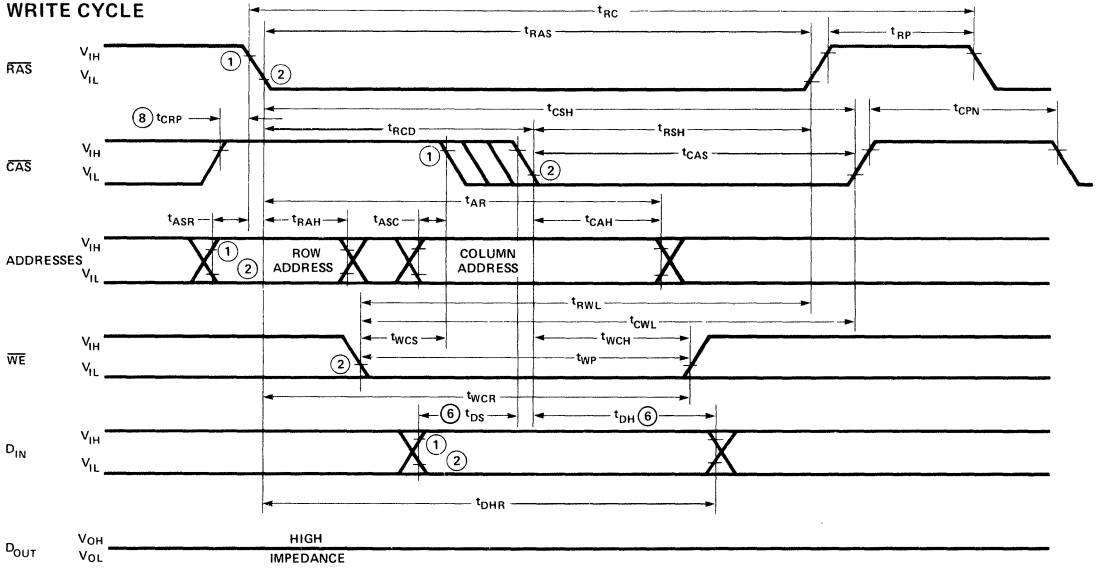
Notes: See following page for A.C. Characteristics Notes.

WAVEFORMS

READ CYCLE



WRITE CYCLE



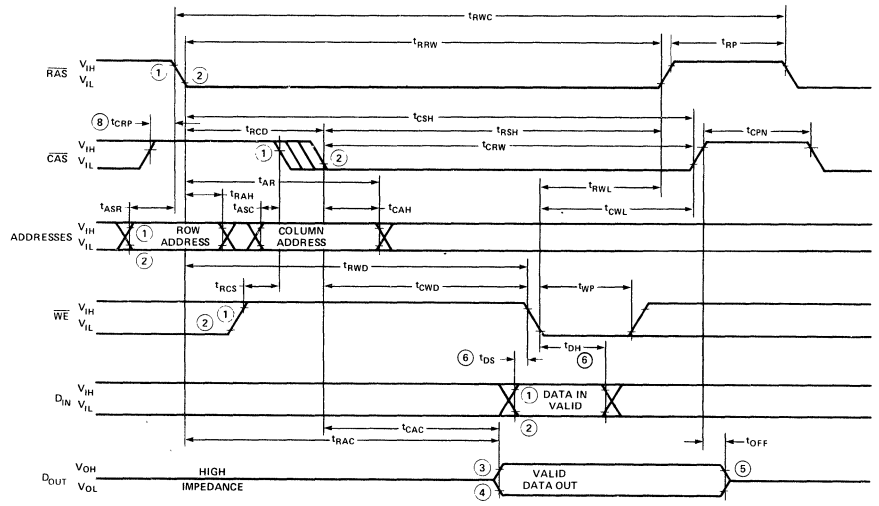
NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

A.C. CHARACTERISTICS NOTES (From Previous Page)

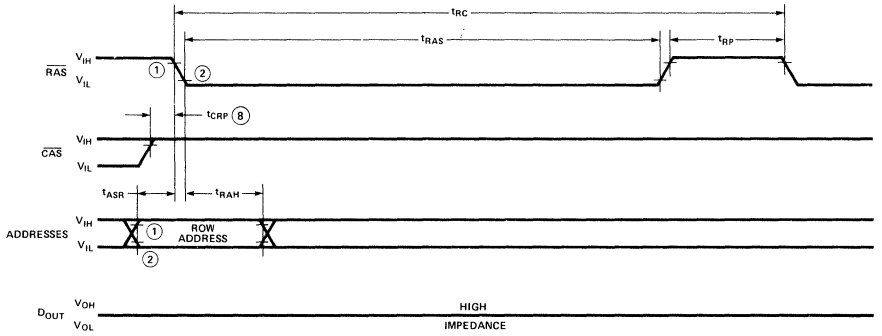
1. All voltages referenced to V_{SS}.
2. Eight cycles are required after power-up or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. A.C. Characteristics assume t_T = 5ns.
4. Assume that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Load = 2 TTL loads and 100pF.
6. Assumes $t_{RCD} \geq t_{RCD}$ (max.).
7. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC}, if t_{RCD} is greater than t_{RCD} (max.) access time is $t_{RCD} + t_{CAC}$.
8. t_T is measured between V_{IH} (min.) and V_{IL} (max.).
9. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

WAVEFORMS

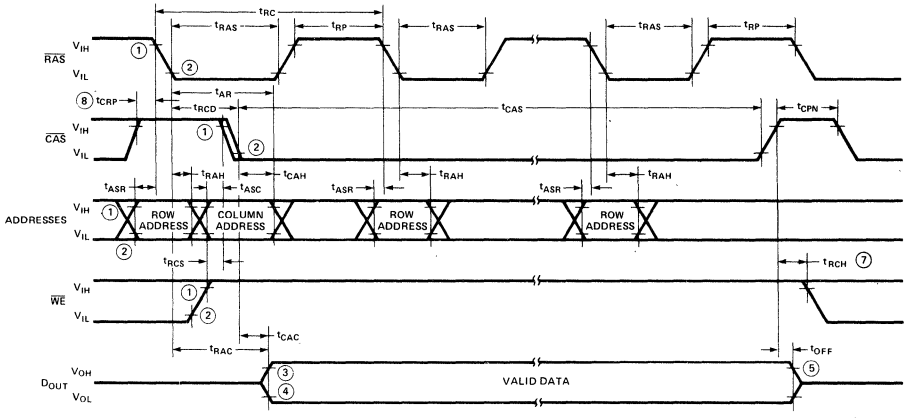
READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



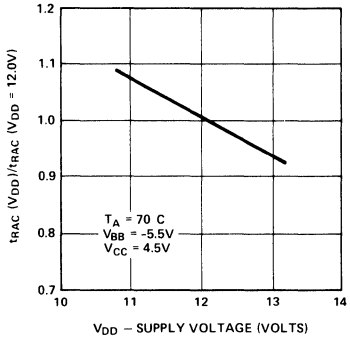
HIDDEN REFRESH CYCLE



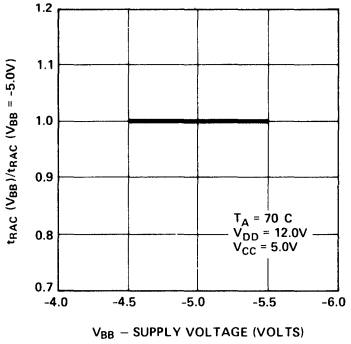
NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $I_{OUT} \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

TYPICAL CHARACTERISTICS[1]

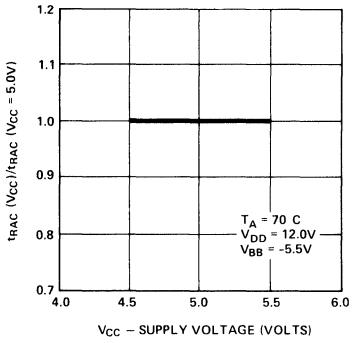
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{DD}



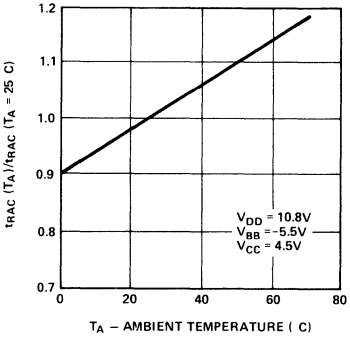
GRAPH 2
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{BB}



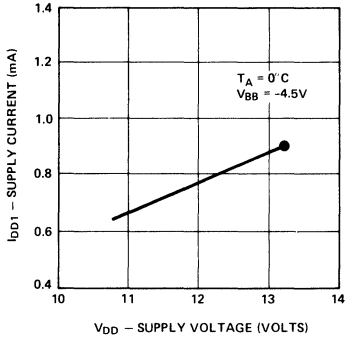
GRAPH 3
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{CC}



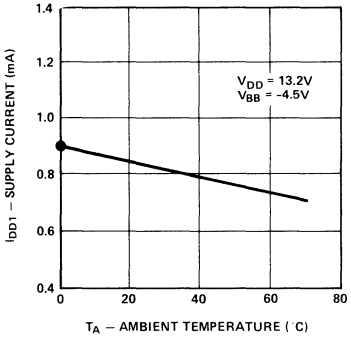
GRAPH 4
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS.
AMBIENT TEMPERATURE



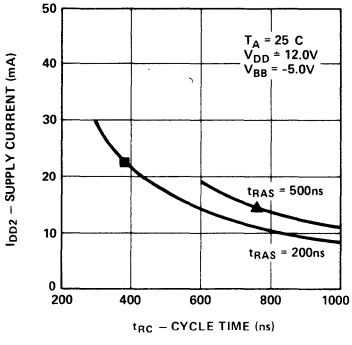
GRAPH 5
TYPICAL STANDBY CURRENT
I_{DD1} VS. V_{DD}



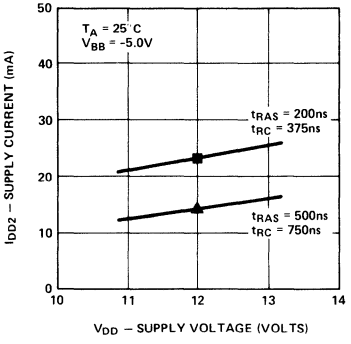
GRAPH 6
TYPICAL STANDBY CURRENT
I_{DD1} VS. AMBIENT TEMPERATURE



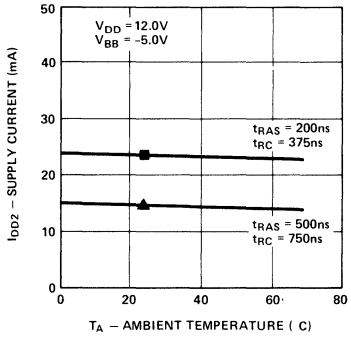
GRAPH 7
TYPICAL OPERATING CURRENT
I_{DD2} VS. t_{RC}



GRAPH 8
TYPICAL OPERATING CURRENT
I_{DD2} VS. V_{DD}



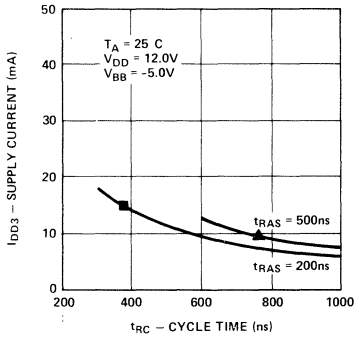
GRAPH 9
TYPICAL OPERATING CURRENT
I_{DD2} VS. AMBIENT TEMPERATURE



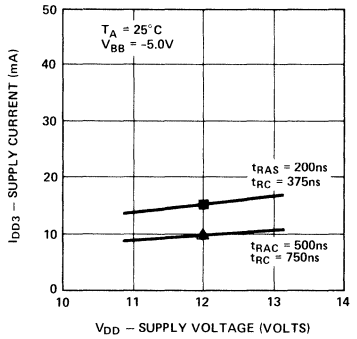
NOTES: See following page for Typical Characteristics Notes.

TYPICAL CHARACTERISTICS [1]

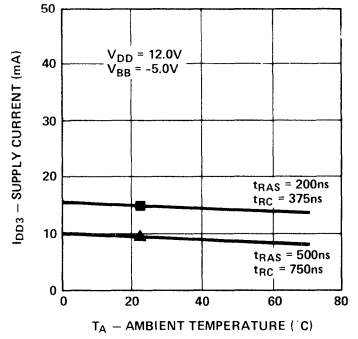
GRAPH 10
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. t_{RC}



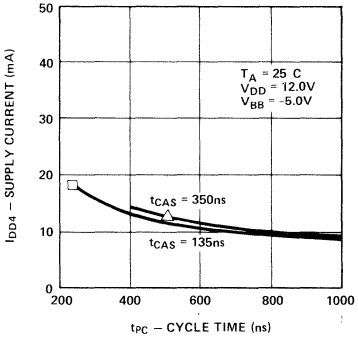
GRAPH 11
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. V_{DD}



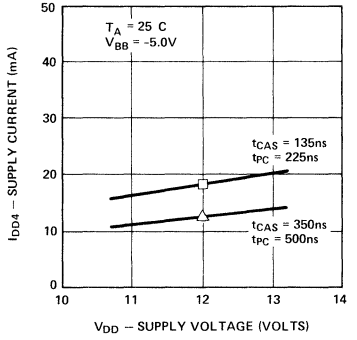
GRAPH 12
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. AMBIENT TEMPERATURE



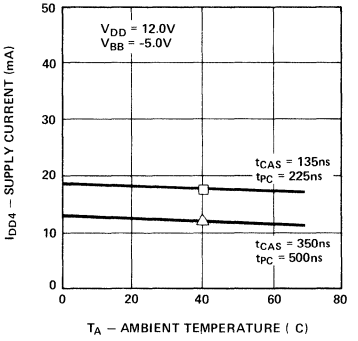
GRAPH 13
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. t_{PC}



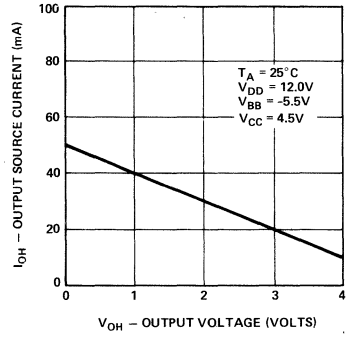
GRAPH 14
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. V_{DD}



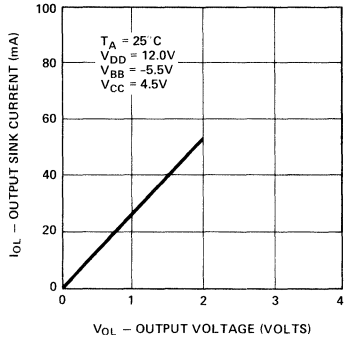
GRAPH 15
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. AMBIENT TEMPERATURE



GRAPH 16
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} VS. OUTPUT VOLTAGE V_{OH}



GRAPH 17
TYPICAL OUTPUT SINK CURRENT
I_{OL} VS. OUTPUT VOLTAGE V_{OL}



NOTES:

1. The cycle time, V_{DD} supply voltage, and ambient temperature dependence of I_{DD1}, I_{DD2}, I_{DD3} and I_{DD4} is shown in related graphs. Common points of related curves are indicated:
   - ● I_{DD1} @ V_{DD} = 13.2V, T_A = 0°C
   - ■ I_{DD2} or I_{DD3} @ t_{RAS} = 200ns, t_{RC} = 375ns, V_{DD} = 12.0V, T_A = 25°C
   - ▲ I_{DD2} or I_{DD3} @ t_{RAS} = 500ns, t_{RC} = 750ns, V_{DD} = 12.0V, T_A = 25°C
   - □ I_{DD4} @ t_{CAS} = 135ns, t_{PC} = 225ns, V_{DD} = 12.0V, T_A = 25°C
   - △ I_{DD4} @ t_{CAS} = 350ns, t_{PC} = 500ns, V_{DD} = 12.0V, T_A = 25°C

   The typical I_{DD} current for a given combination of cycle time, V_{DD} supply voltage and ambient temperature may be determined by combining the effects of the appropriate family of curves.

D.C. AND A.C. CHARACTERISTICS, PAGE MODE [7,8,11]

T_A = 0°C to 70°C, V_{DD} = 12V±10%, V_{CC} = 5V±10%, V_{BB} = -5V±10%, V_{SS} = 0V, unless otherwise noted.

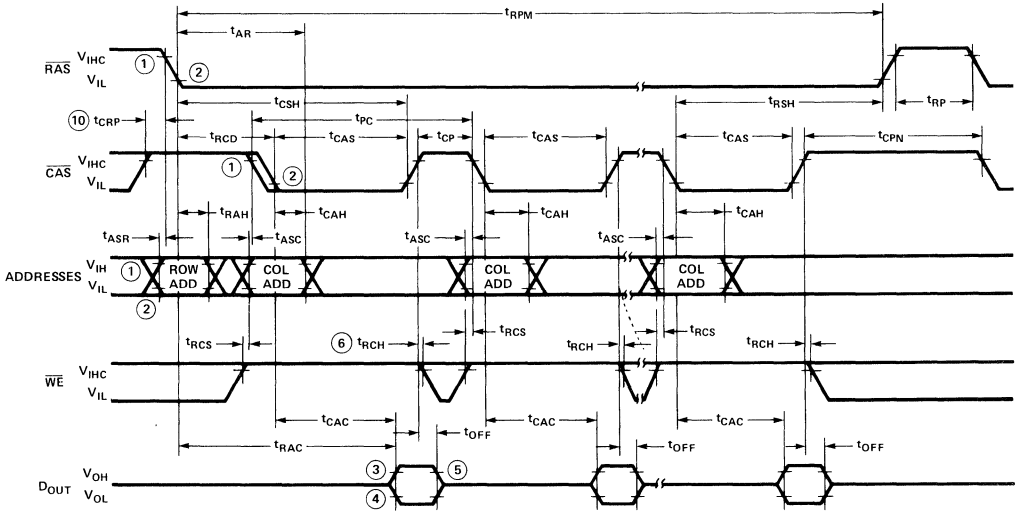
For Page Mode Operation order: 2109-3* S6064, S6065 or 2109-4* S6066, S6067.

Symbol	Parameter	2109-3 S6064,S6065		2109-4 S6066,S6067		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{PC}	Page Mode Read or Write Cycle	225		275		ns	
t_{PCM}	Page Mode Read Modify Write	270		340		ns	
t_{CP}	$\overline{CAS}$ Precharge Time, Page Cycle	80		100		ns	
t_{RPM}	$\overline{RAS}$ Pulse Width, Page Mode	200	10,000	250	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	135	10,000	165	10,000	ns	
I_{DD4}	V_{DD} Supply Current Page Mode, Minimum t_{PC}, Minimum t_{CAS}		30		26	mA	9

***S6064, S6066: A6 at VIH during Row Address Valid.**
S6065, S6067: A6 at VIL during Row Address Valid.

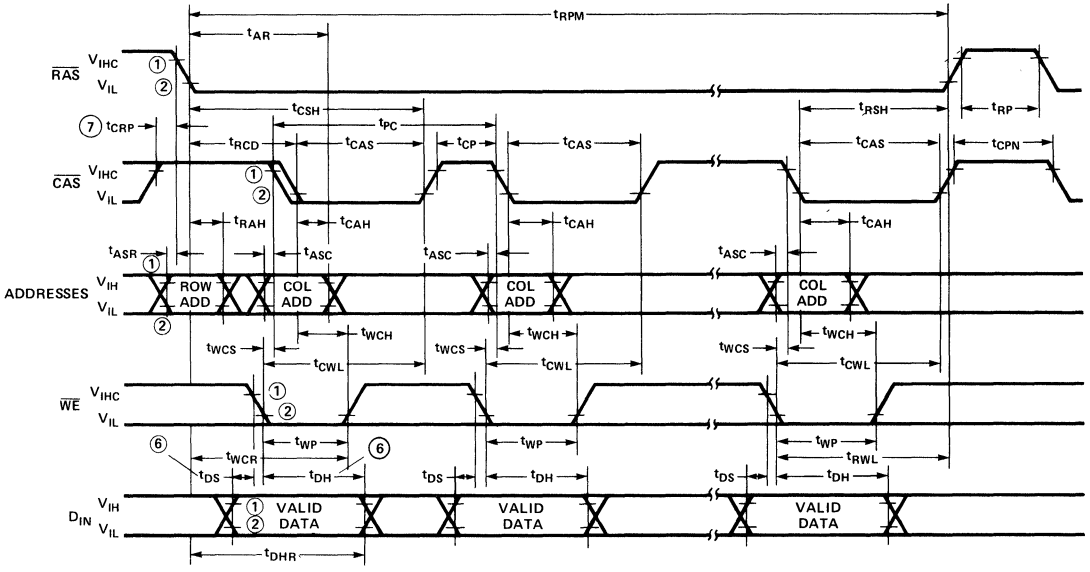
WAVEFORMS

PAGE MODE READ CYCLE

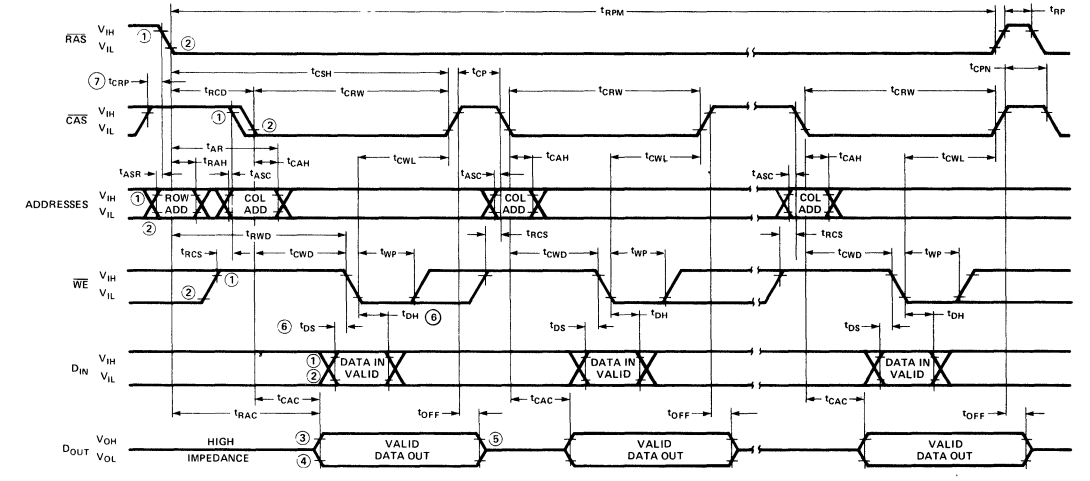


NOTES:
1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
7. ALL VOLTAGES REFERENCED TO V_{SS}.
8. AC CHARACTERISTIC ASSUME t_T = 5ns.
9. SEE THE TYPICAL CHARACTERISTICS SECTION FOR VALUES OF THIS PARAMETER UNDER ALTERNATE CONDITIONS.
10. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).
11. ALL PREVIOUSLY SPECIFIED A.C. AND D.C. CHARACTERISTICS ARE APPLICABLE TO THEIR RESPECTIVE PAGE MODE DEVICE (i.e., 2109-3, S6064 OR S6065 WILL OPERATE AS A 2109-3).

PAGE MODE WRITE CYCLE



PAGE MODE READ-MODIFY-WRITE CYCLE



NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

APPLICATIONS

The 2109 is packaged in a standard 16-pin DIP by multiplexing 14 address bits onto 7 input pins (A_0-A_6). The 7 bit address words are latched into the 2109 by two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Since the 2109 is an 8K memory device, only 13 of the 14 address bits are required and the 14th address bit must be at V_{IH} (for S6000, S6002, S6064 or S6066) or V_{IL} (for S6001, S6003, S6065 or S6067) during Row Address Valid. This means it is not possible to simply tie input pin A_6 high or low, since it supplies two system addresses to the memory array. Input pin A_6 must be at the appropriate level (determined by the "S"-specification) during the row address valid period and then changed to the proper high order address during the column address valid period.

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during a $\overline{RAS}/\overline{CAS}$ operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time.

Device access time, t_{ACC}, is the longer of the two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCD} + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe delay time, t_{RCD}, are system dependent timing parameters. For example, substituting the device parameters of the 2109-3 yields:

3. $t_{ACC} = t_{RAC} = 200$nsec for 25nsec $\leq t_{RCD} \leq$ 65nsec

OR

4. $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD} + 135$ for $t_{RCD} > 65$nsec

Note that if 25nsec $\leq t_{RCD} \leq$ 65nsec device access time is determined by equation 3 and is equal to t_{RAC}. If t_{RCL} >65nsec, access time is determined by equation 4. This 40nsec interval (shown in the t_{RCD} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$.

REFRESH CYCLES

Each of the 64 rows of the 2109 must be refreshed every 2 milliseconds to maintain data. Any memory cycle:

1. Read Cycle
2. Write Cycle (Early Write, Delayed Write or Read-Modify-Write)
3. $\overline{RAS}$-only Cycle

refreshes the selected row as defined by the low order ($\overline{RAS}$) addresses. A_6 must be held at the proper level (V_{IH} or V_{IL} depending on specification) to perform 64 cycle refresh operation, but may be driven high and low for 128 cycle $\overline{RAS}$-only refresh without affecting device data retention. Any Write cycle, of course, may change the state of the selected cell. Using a Read, Write, or Read-Modify-Write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the D_{OUT} in the high impedance state with a typical power reduction of 20% over a Read or Write cycle.

$\overline{RAS}/\overline{CAS}$ TIMING

$\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle can not begin until the minimum precharge time, t_{RP}, has been met.

DATA OUTPUT OPERATION

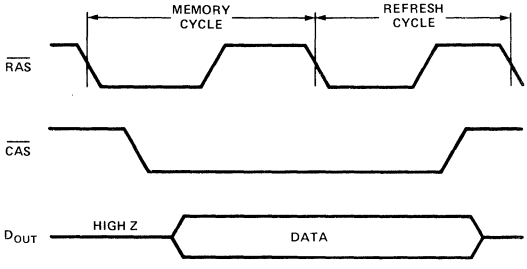
The 2109 Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}) the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

Intel 2109 Data Output Operation for Various Types of Cycles

Type of Cycle	D_{OUT} State
Read Cycle	Data From Addressed Memory Cell
Fast Write Cycle	HI-Z
$\overline{RAS}$-Only Refresh Cycle	HI-Z
$\overline{CAS}$-Only Cycle	HI-Z
Read/Modify/Write Cycle	Data From Addressed Memory Cell
Delayed Write Cycle	Indeterminate

HIDDEN REFRESH

A feature of the 2109 is that refresh cycles may be performed while maintaining valid data at the output pin. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see Figure below).



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

POWER ON

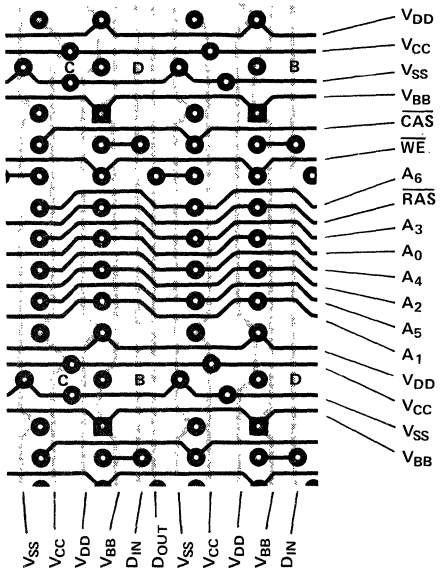
The 2109 requires no power on sequence providing absolute maximum ratings are not exceeded. After the application of supply voltages or after extended periods of bias (greater than 2 milliseconds) without clocks, the device must perform a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock, such as $\overline{RAS}$-Only refresh) prior to normal operation.

POWER SUPPLY DECOUPLING/DISTRIBUTION

It is recommended that a 0.1μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

The V_{CC} supply is connected only to the 2109 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is associated with the input high level current to a TTL gate and the output leakage currents of any OR-tied 2109's (typically 100μA or less total). Intel recommends that a 0.1 or 0.01μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight memory devices.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



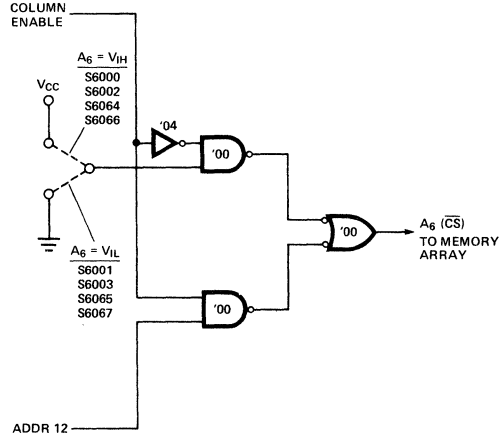
DECOUPLING CAPACITORS
D = 0.1μF TO V_{DD} TO V_{SS}
B = 0.1μF V_{BB} TO V_{SS}
C = 0.01μF V_{CC} TO V_{SS}

SAMPLE P.C. BOARD LAYOUT EMPLOYING VERTICAL AND HORIZONTAL GRIDDING ON ALL POWER SUPPLIES.

8K UPGRADE FOR 4K SYSTEMS

The 2109 can be used to upgrade existing 4K (Intel 2104A) memory systems with minimal redesign. The 2109 maintains many of the features of the 4K RAMs. For example, the latched data output of the 4Ks can be emulated by holding $\overline{CAS}$ low to maintain data out valid. Hidden refresh capability for the 4Ks is also maintained with the 2109. The 64 cycle refresh operation of the 2109 makes it compatible with 4K systems.

To upgrade a 4K system to accept the 2109, an extra memory address multiplexer must be implemented to replace the Chip Select ($\overline{CS}$) input of the 4Ks. The replacement circuitry is shown in the figure below, and involves some gating to control the output of the multiplexer during row and column address valid periods and also some control to handle the multiplexer during refresh operation.



2111A/8111A-4*
256 x 4 BIT STATIC RAM

2111A-2	**250 ns Max.**
2111A	**350 ns Max.**
2111A-4	**450 ns Max.**

- **Common Data Input and Output**
- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Output**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 18 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150 mW**
- **Three-State Output: OR-Tie Capability**

The Intel® 2111A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

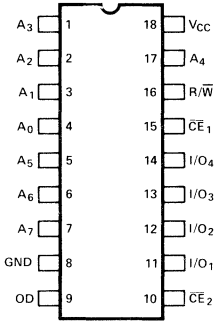
The 2111A is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

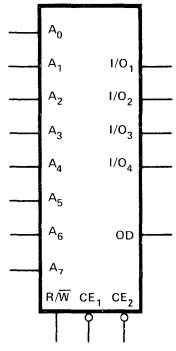
The Intel® 2111A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



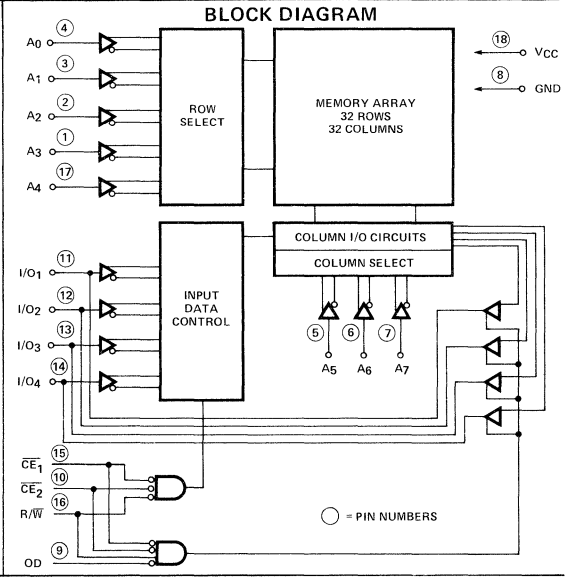
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
$R/\overline{W}$	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
$\overline{CE}_2$	CHIP ENABLE 2
I/O_1- I/O_4	DATA INPUT/OUTPUT

BLOCK DIAGRAM



*All 8111A-4 specifications are identical to the 2111A-4 specifications.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

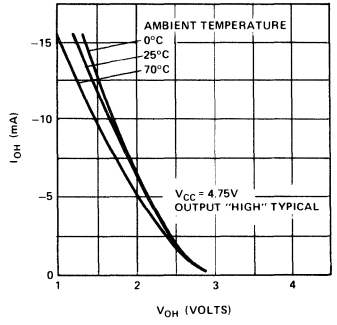
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

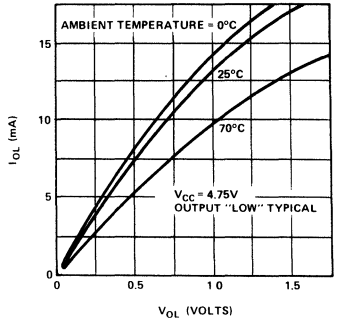
T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current		1	10	μA	Output Disabled, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current		-1	-10	μA	Output Disabled, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current 2111A, 2111A-4		35	55	mA	V_{IN} = 5.25V
	Power Supply Current 2111A-2		45	65		$I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current 2111A, 2111A-4			60	mA	V_{IN} = 5.25V
	Power Supply Current 2111A-2			70		$I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage 2111A, 2111A-2	2.4			V	I_{OH} = -200μA
	Output High Voltage 2111A-4	2.4			V	I_{OH} = -150μA

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2111A-2 (250 ns ACCESS TIME)

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			250	ns	
t_{CO}	Chip Enable To Output			180	ns	
t_{OD}	Output Disable To Output			130	ns	
t_{DF}[3]	Data Output to High Z State	0		180	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

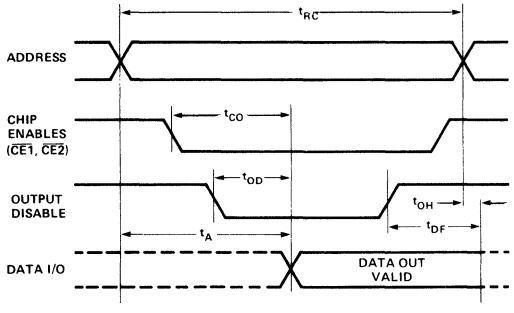
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	150			ns	
t_{DW}	Data Setup	150			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	150			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

CAPACITANCE[2] T_A = 25°C, f = 1MHz

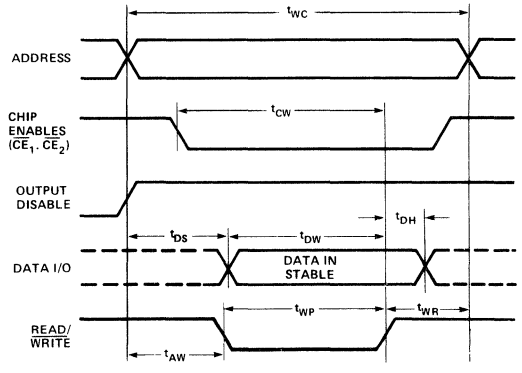
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.

2111A (350 ns ACCESS TIME)

A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			350	ns	
t_{CO}	Chip Enable To Output			240	ns	
t_{OD}	Output Disable To Output			180	ns	
t_{DF} [2]	Data Output to High Z State	0		150	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	220			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	200			ns	
t_{DW}	Data Setup	200			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	200			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

2111A-4 (450 ns ACCESS TIME)

A.C. CHARACTERISTICS

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_A	Access Time			450	ns	
t_{CO}	Chip Enable To Output			310	ns	
t_{OD}	Output Disable To Output			250	ns	
t_{DF} [2]	Data Output to High Z State	0		200	ns	
t_{OH}	Previous Read Data Valid after change of Address	40			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	t_r, t_f = 20ns Input Levels = 0.8V or 2.0V Timing Reference = 1.5V Load = 1 TTL Gate and C_L = 100pF.
t_{AW}	Write Delay	20			ns	
t_{CW}	Chip Enable To Write	250			ns	
t_{DW}	Data Setup	250			ns	
t_{DH}	Data Hold	0			ns	
t_{WP}	Write Pulse	250			ns	
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.

2112A
256 X 4 BIT STATIC RAM

2112A-2	250 ns Max.
2112A	350 ns Max.
2112A-4	450 ns Max.

- **Single +5V Supply Voltage**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Static MOS: No Clocks or Refreshing Required**
- **Simple Memory Expansion: Chip Enable Input**
- **Fully Decoded: On Chip Address Decode**
- **Inputs Protected: All Inputs Have Protection Against Static Charge**
- **Low Cost Packaging: 16 Pin Plastic Dual In-Line Configuration**
- **Low Power: Typically 150 mW**
- **Three-State Output: OR-Tie Capability**

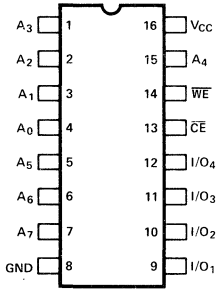
The Intel® 2112A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2112A is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

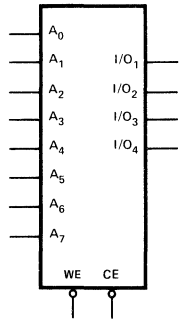
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

The Intel® 2112A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

PIN CONFIGURATION



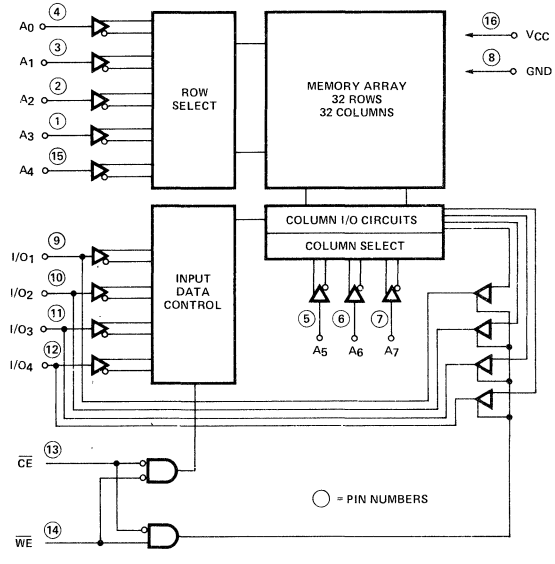
LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V

Power Dissipation . . . . . 1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

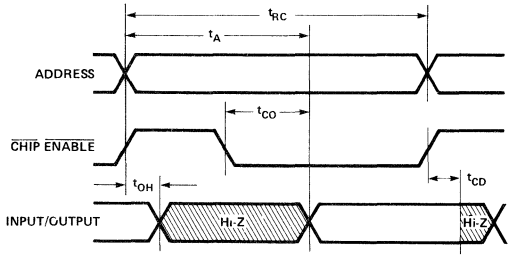
Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			1	10	µA	Output Disabled, $V_{I/O}$=4.0V
I_{LOL}	I/O Leakage Current			-1	-10	µA	Output Disabled, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current	2112A, 2112A-4		35	55	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
		2112A-2		45	65		
I_{CC2}	Power Supply Current	2112A, 2112A-4			60	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
		2112A-2			70		
V_{IL}	Input "Low" Voltage		-0.5		0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output "High" Voltage	2112A, 2112A-2	2.4			V	I_{OH} = -200µA
		2112A-4	2.4			V	I_{OH} = -150µA

A.C. CHARACTERISTICS FOR 2112A-2

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	t_r, t_f = 20ns
t_A	Access Time			250	ns	
t_{CO}	Chip Enable To Output Time			180	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		120	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

READ CYCLE WAVEFORMS



CAPACITANCE[2] T_A = 25°C, f = 1 MHz

Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	15

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS FOR 2112A-2 (Continued)

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

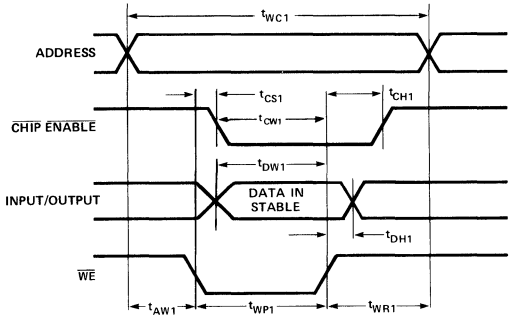
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	200			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	180			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	180			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable To Write Setup Time	180			ns	

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

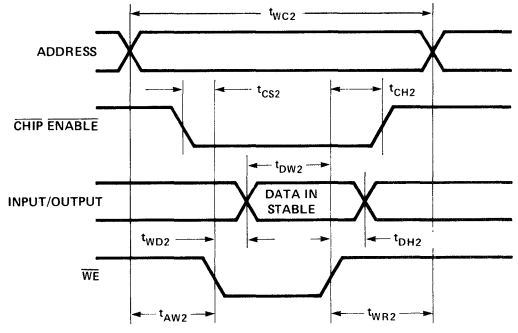
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	320			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	180			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	120			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

WRITE CYCLE WAVEFORMS

WRITE CYCLE #1



WRITE CYCLE #2



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2112A

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns
t_A	Access Time			350	ns	Input Levels = 0.8V or 2.0V
t_{CO}	Chip Enable To Output Time			240	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		200	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	270			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	250			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	250			ns	

WRITE CYCLE #2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	470			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	200			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2112A-4

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	t_r, t_f = 20ns
t_A	Access Time			450	ns	Input Levels = 0.8V or 2.0V
t_{CO}	Chip Enable To Output Time			310	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		260	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	320			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	300			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	300			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	300			ns	

WRITE CYCLE #2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	580			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	300			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	260			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

2114
1024 X 4 BIT STATIC RAM

	2114-2	2114-3	2114	2114L2	2114L3	2114L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Power Dissipation (mw)	525	525	525	370	370	370

- **High Density 18 Pin Package**
- **Identical Cycle and Access Times**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **Pin-Out Compatible with 3605 and 3625 Bipolar PROMs**

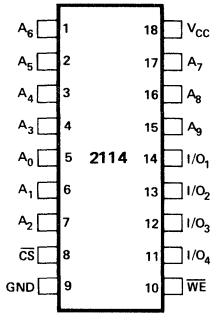
The Intel® 2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The 2114 is placed in an 18-pin package for the highest possible density.

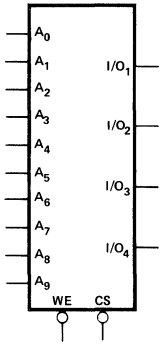
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

The 2114 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

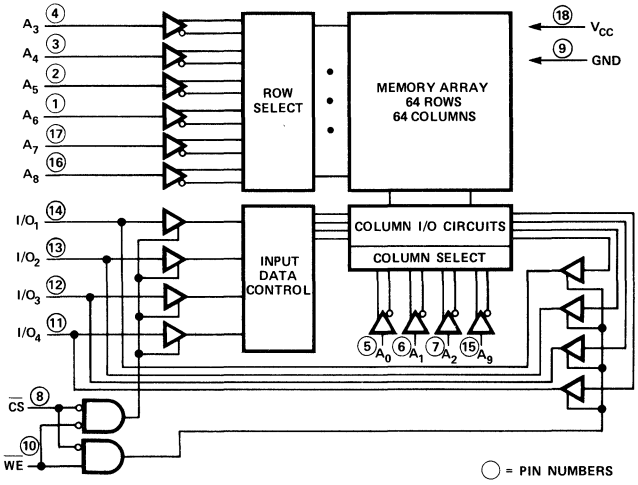
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to 80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.0W
D.C. Output Current 5mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.

SYMBOL	PARAMETER	2114-2, 2114-3, 2114 Min.	Typ.[1]	Max.	2114L2, 2114L3, 2114L Min.	Typ.[1]	Max.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10			10	µA	V_{IN} = 0 to 5.25V
$\|I_{LO}\|$	I/O Leakage Current			10			10	µA	$\overline{CS}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		80	95			65	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current			100			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	6.0		2.1	6.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	-1.0	-1.4		-1.0	-1.4		mA	V_{OH} = 2.4V
I_{OS}[2]	Output Short Circuit Current			40			40	mA	

NOTE: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 30 seconds.

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = OV
C_{IN}	Input Capacitance	5	pF	V_{IN} = OV

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels ..... 0.8 Volt to 2.4 Volt
Input Rise and Fall Times ..... 10 nsec
Input and Output Timing Levels ..... 1.5 Volts
Output Load ..... 1 TTL Gate and C_L = 100 pF

TEST NOTE: This circuit employs a self starting oscillator and a charge pump which require a certain amount of time after POWER ON to start functioning properly. This 2114 circuit is conservatively specified as requiring 500 µsec after V_{CC} reaches its specified limits (4.75V).

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2114-2, 2114L2 Min.	2114-2, 2114L2 Max.	2114-3, 2114L3 Min.	2114-3, 2114L3 Max.	2114, 2114L Min.	2114, 2114L Max.	UNIT
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{CO}	Chip Selection to Output Valid		70		100		120	ns
t_{CX}	Chip Selection to Output Active	20		20		20		ns
t_{OTD}	Output 3-state from Deselection		60		80		100	ns
t_{OHA}	Output Hold from Address Change	50		50		50		ns

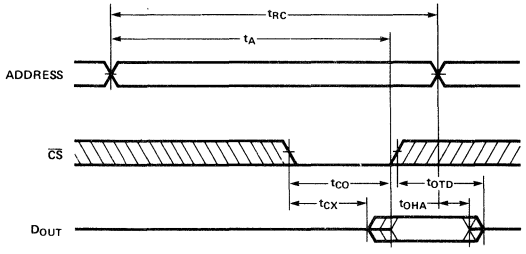
WRITE CYCLE [2]

SYMBOL	PARAMETER	2114-2, 2114L2 Min.	2114-2, 2114L2 Max.	2114-3, 2114L3 Min.	2114-3, 2114L3 Max.	2114, 2114L Min.	2114, 2114L Max.	UNIT
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTW}	Output 3-state from Write		60		80		100	ns
t_{DW}	Data to Write Time Overlap	120		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

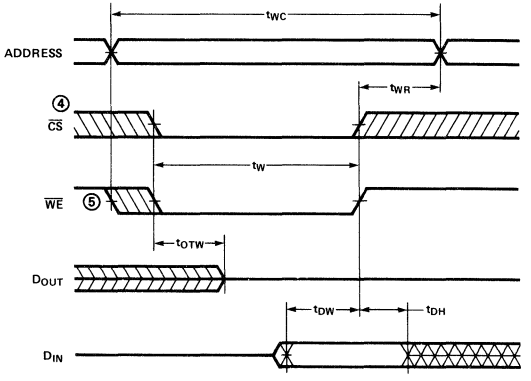
WAVEFORMS

READ CYCLE ③



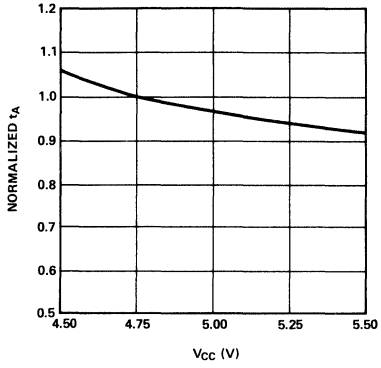
NOTES:
③ $\overline{WE}$ is high for a Read Cycle.
④ If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
⑤ $\overline{WE}$ must be high during all address transitions.

WRITE CYCLE

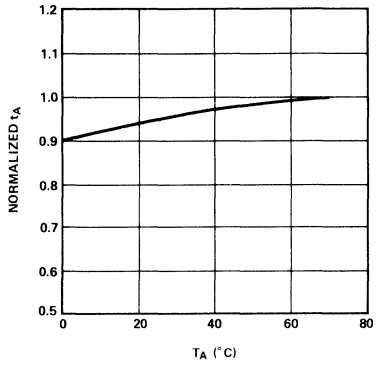


TYPICAL D.C. AND A.C. CHARACTERISTICS

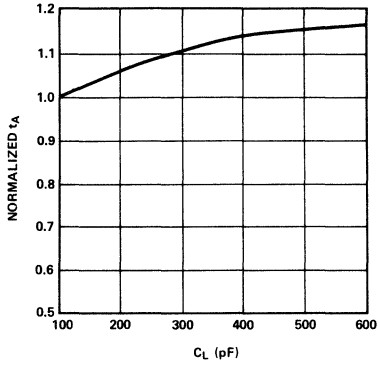
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



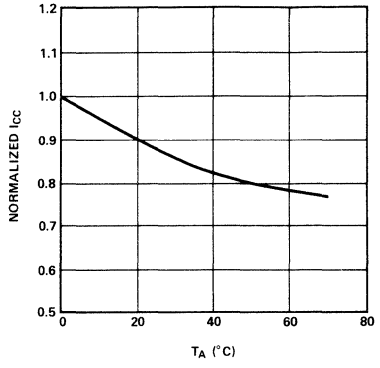
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



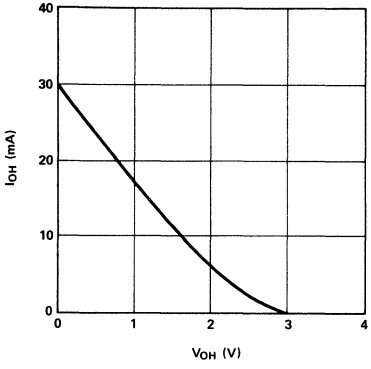
NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



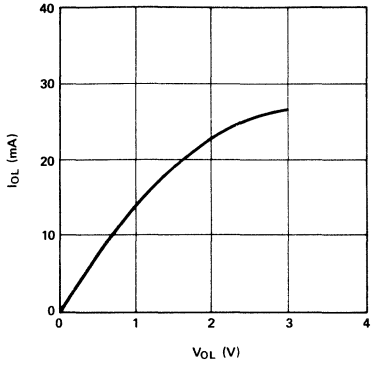
NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



2115A, 2125A FAMILY
HIGH SPEED 1K X 1 BIT STATIC RAM

	2115AL 2125AL	2115A 2125A	2115AL-2 2125AL-2	2115A-2 2125A-2
Max. T_{AA}(ns)	45	45	70	70
Max. I_{CC}(mA)	75	125	75	125

- **HMOS Technology**
- **Pin Compatible To 93415A (2115A) And 93425A (2125A)**
- **Fan-Out Of 10 TTL (2115A Family) -- 16mA Output Sink Current**
- **Low Operating Power Dissipation --Max. 0.39mW/Bit (2115AL, 2125AL)**
- **TTL Inputs And Outputs**
- **Single +5V Supply**
- **Uncommitted Collector (2115A) And Three-State (2125A) Output**
- **Standard 16-Pin Dual In-Line Package**

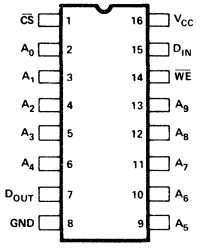
The Intel® 2115A and 2125A families are high-speed, 1024 words by 1 bit random access memories. Both open collector (2115A) and three-state output (2125A) are available. The 2115A and 2125A use fully DC stable (static) circuitry throughout – in both the array and the decoding and, therefore, require no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data.

The 2115AL/2125AL at 45 ns maximum access time and the 2115AL-2/2125AL-2 at 70 ns maximum access time are fully compatible with the industry-produced 1K bipolar RAMs, yet offer a 50% reduction in power of their bipolar equivalents. The power dissipation of the 2115AL/2125AL and 2115AL-2/2125AL-2 is 394 mW maximum as compared to 814 mW maximum of their bipolar equivalents. For systems already designed for 1K bipolar RAMs, the 2115A/2125A and the 2115A-2/2125A-2 at 45 ns and 70 ns maximum access times, respectively, offer complete compatibility with a 20% reduction in maximum power dissipation.

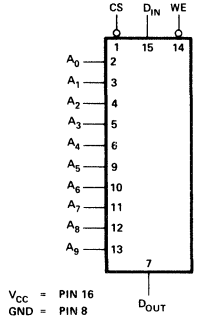
The devices are directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

The 2115A and 2125A families are fabricated with HMOS, Intel's High Speed N-channel MOS Silicon Gate Technology.

PIN CONFIGURATION



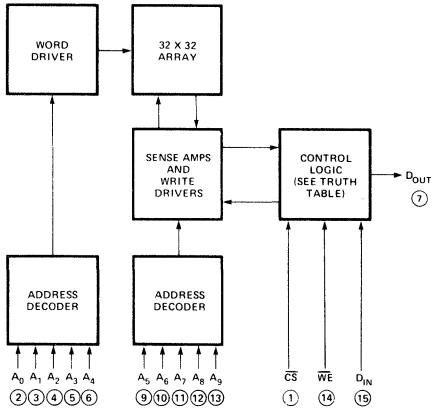
LOGIC SYMBOL



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT 2115A FAMILY	OUTPUT 2125A FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	HIGH Z	HIGH Z	NOT SELECTED
L	L	L	HIGH Z	HIGH Z	WRITE "0"
L	L	H	HIGH Z	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −10°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
All Output or Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −0.5V to +5.5V
D.C. Output Current . . . . . 20 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1,2]

V_{CC} = 5V ±5%, T_A = 0°C to 75°C

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
V_{OL1}	2115A Family Output Low Voltage			0.45	V	I_{OL} = 16 mA
V_{OL2}	2125A Family Output Low Voltage			0.45	V	I_{OL} = 7 mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		−0.1	−40	μA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max., V_{IN} = 4.5V
I_{CEX}	2115A Family Output Leakage Current		0.1	100	μA	V_{CC} = Max., V_{OUT} = 4.5V
$\|I_{OFF}\|$	2125A Family Output Current (High Z)		0.1	50	μA	V_{CC} = Max., V_{OUT} = 0.5V/2.4V
I_{OS}[3]	2125A Family Current Short Circuit to Ground			−100	mA	V_{CC} = Max.
V_{OH}	Family Output High Voltage	2.4			V	I_{OH} = −3.2 mA
I_{CC}	Power Supply Current: I_{CC1}: 2115AL, 2115AL-2, 2125AL, 2125AL-2		60	75	mA	All Inputs Grounded, Output Open
	I_{CC2}: 2115A, 2115A-2, 2125A, 2125A-2		100	125	mA	

NOTES:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (@ 400 f_{PM} air flow) = 45°C/W
   θ_{JA} (still air) = 60°C/W
   θ_{JC} = 25°C/W

2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and maximum loading.
3. Duration of short circuit current should not exceed 1 second.

2115A FAMILY A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

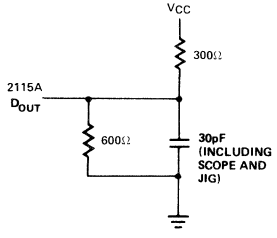
READ CYCLE

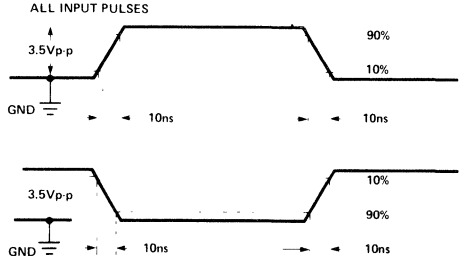
Symbol	Test	2115AL Limits Min.	Typ.	Max.	2115A Limits Min.	Typ.	Max.	2115AL-2 Limits Min.	Typ.	Max.	2115A-2 Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{RCS}	Chip Select Recovery Time		10	30		10	30		10	30		10	40	ns
t_{AA}	**Address Access Time**		**30**	**45**		**30**	**45**		**40**	**70**		**40**	**70**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			10			ns

WRITE CYCLE

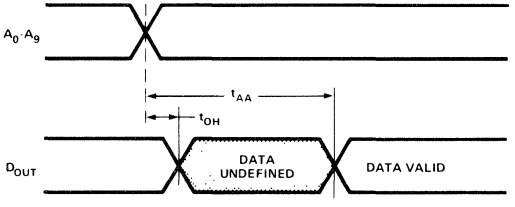
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{WS}	Write Enable Time		10	25		10	30		10	25		10	40	
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	15		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	–5		5	–5		0	–5		5	–5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

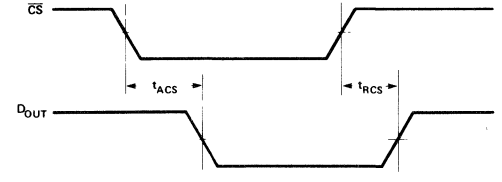




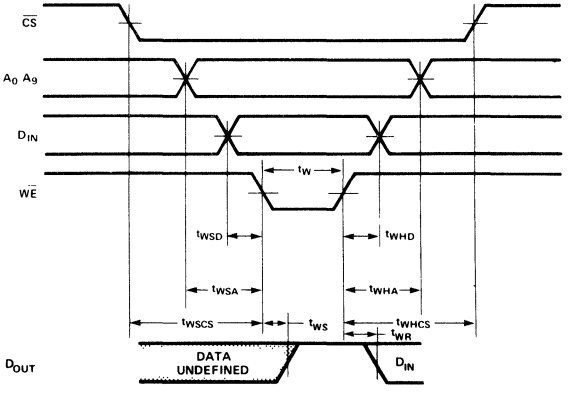
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

2125A FAMILY A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

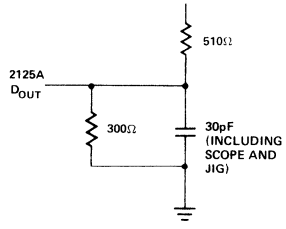
READ CYCLE

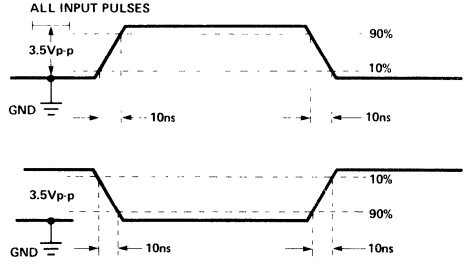
Symbol	Test	2125AL Limits Min.	Typ.	Max.	2125A Limits Min.	Typ.	Max.	2125AL-2 Limits Min.	Typ.	Max.	2125A-2 Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{ZRCS}	Chip Select to HIGH Z		10	30		10	30		10	30		10	40	ns
t_{AA}	**Address Access Time**		**30**	**45**		**30**	**45**		**40**	**70**		**40**	**70**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			10			ns

WRITE CYCLE

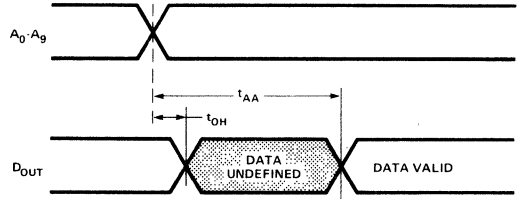
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{ZWS}	Write Enable to HIGH Z		10	25		10	30		10	25		10	40	ns
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	10		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	−5		5	−5		0	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

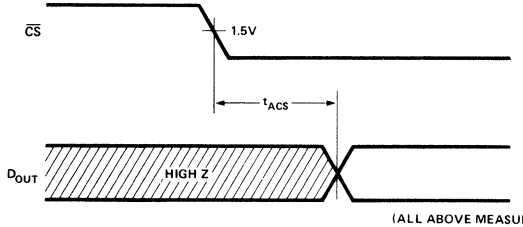




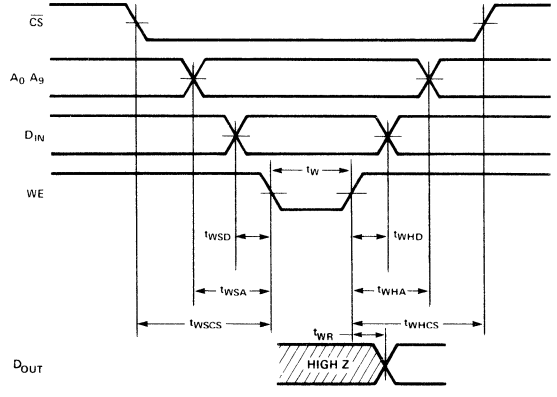
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



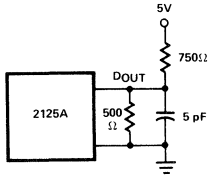
WRITE CYCLE



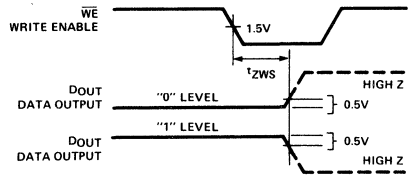
(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

RAM

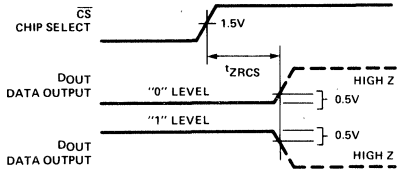
2125A FAMILY WRITE ENABLE TO HIGH Z DELAY



LOAD 1



2125A FAMILY PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(ALL t_{ZXXX} PARAMETERS ARE MEASURED AT A DELTA OF 0.5V FROM THE LOGIC LEVEL AND USING LOAD 1.)

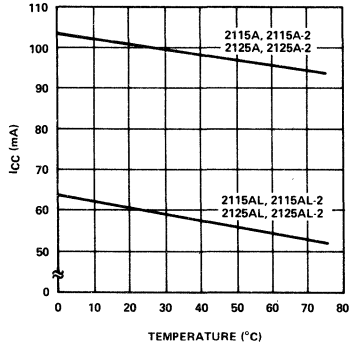
2115A/2125A FAMILY CAPACITANCE* V_{CC}= 5V, f = 1 MHz, T_A = 25°C

SYMBOL	TEST	2115A Family LIMITS		2125A Family LIMITS		UNITS	TEST CONDITIONS
		TYP.	MAX.	TYP.	MAX.		
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	$\overline{CS}$ = 5V, All Other Inputs = 0V, Output Open

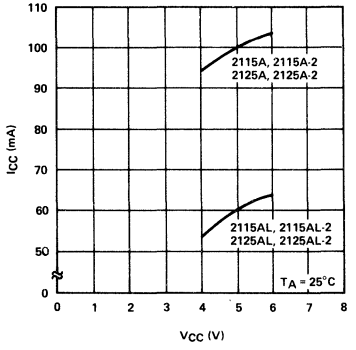
*This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

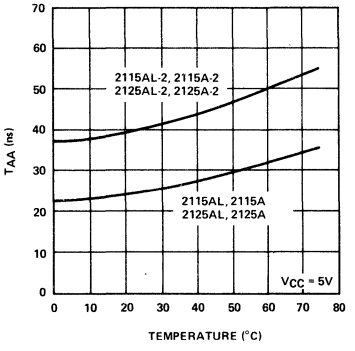
I_{CC} VS. TEMPERATURE



I_{CC} VS. V_{CC}



ACCESS TIME VS. TEMPERATURE



2115H, 2125H FAMILY
HIGH SPEED 1K x 1 BIT STATIC RAM

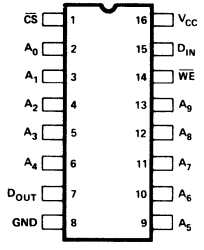
- **HMOS II Technology**
- **25-35ns Maximum Access Time**
- **125mA Maximum I_{CC}**
- **Pin Compatible to 93415A (2115H) and 93425A (2125H)**
- **TTL Inputs and Outputs**
- **Single +5V Supply**
- **Uncommitted Collector (2115H) and Three-State (2125H) Output**
- **Standard 16-Pin Dual In-Line Package**

The Intel® 2115H and 2125H families are high-speed, 1024 words by 1 bit random access memories. Both open collector (2115H), and three-state output (2125H) are available. The 2115H and 2125H use fully DC stable (static) circuitry throughout — in both the array and the decoding and, therefore, require no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data.

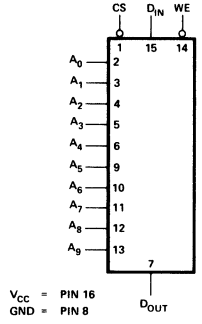
The 2115H and 2125H families are fully compatible with 1K Bipolar Static RAMs yet offer significant reductions in power The devices are directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

The 2115H and 2125H families are fabricated with Intel's N-channel HMOS II Silicon Gate Technology.

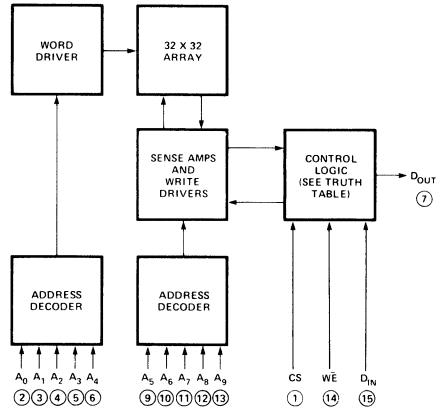
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

TRUTH TABLE

INPUTS			OUTPUT 2115H FAMILY	OUTPUT 2125H FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	HIGH Z	HIGH Z	NOT SELECTED
L	L	L	HIGH Z	HIGH Z	WRITE "0"
L	L	H	HIGH Z	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

2117 FAMILY
16,384 x 1 BIT DYNAMIC RAM

	2117-2	2117-3	2117-4
Maximum Access Time (ns)	150	200	250
Read, Write Cycle (ns)	320	375	410
Read-Modify-Write Cycle (ns)	330	375	475

- **Industry Standard 16-Pin Configuration**
- **±10% Tolerance on All Power Supplies: +12V, +5V, -5V**
- **Low Power: 462mW Max. Operating, 20mW Max. Standby**
- **Low I_{DD} Current Transients**
- **All Inputs, Including Clocks, TTL Compatible**
- **Non-Latched Output is Three-State, TTL Compatible**
- **$\overline{RAS}$ Only Refresh**
- **128 Refresh Cycles Required Every 2ms**
- **Page Mode Capability**
- **$\overline{CAS}$ Controlled Output Allows Hidden Refresh**

The Intel® 2117 is a 16,384 word by 1-bit Dynamic MOS RAM fabricated with Intel's standard two layer polysilicon NMOS technology — a production proven process for high performance, high reliability, and high storage density.

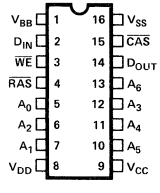
The 2117 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients and ±10% tolerance on all power supplies contribute to the high noise immunity of the 2117 in a system environment.

Multiplexing the 14 address bits into the 7 address input pins allows the 2117 to be packaged in the industry standard 16-pin DIP. The two 7-bit address words are latched into the 2117 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical timing requirements for $\overline{RAS}$ and $\overline{CAS}$ allow use of the address multiplexing technique while maintaining high performance.

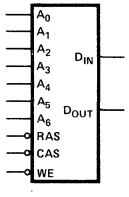
The 2117 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is latched on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The 2117 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain latched data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2ms period. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

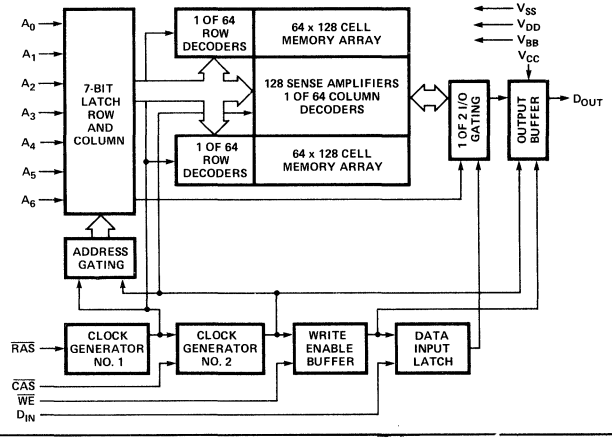
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin Relative to V_{BB}
($V_{SS} - V_{BB} \geq 4V$) ..... -0.3V to +20V
Data Out Current 50mA
Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

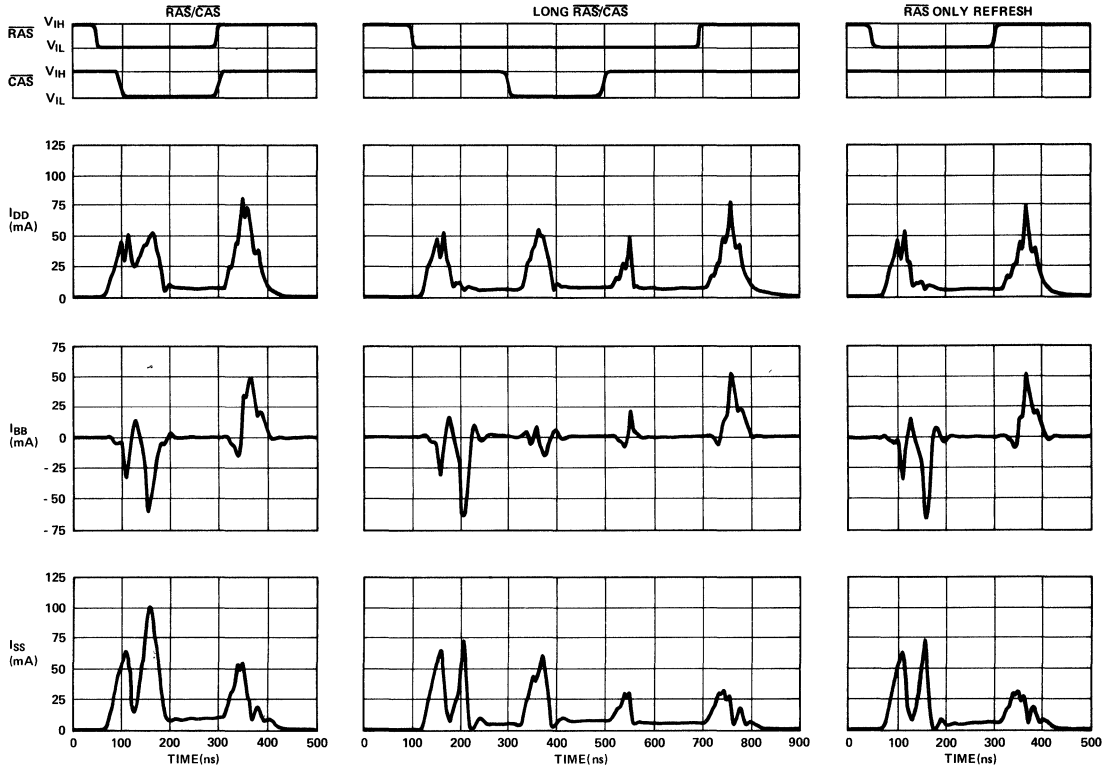
D.C. AND OPERATING CHARACTERISTICS[1,2]

T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits Min.	Typ.[3]	Max.	Unit	Test Conditions	Notes
$\|I_{LI}\|$	Input Load Current (any input)		0.1	10	µA	V_{IN}=V_{SS} to 7.0V, V_{BB}=-5.0V	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State		0.1	10	µA	Chip Deselected: $\overline{CAS}$ at V_{IH}, V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current, Standby			1.5	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	4
I_{BB1}	V_{BB} Supply Current, Standby		1.0	50	µA		
I_{CC1}	V_{CC} Supply Current, Output Deselected		0.1	10	µA	$\overline{CAS}$ at V_{IH}	5
I_{DD2}	V_{DD} Supply Current, Operating			35	mA	2117-2, t_{RC} = 375ns, t_{RAS} = 150ns	4,6
				35	mA	2117-3, t_{RC} = 375ns, t_{RAS} = 200ns	4
				33	mA	2117-4, t_{RC} = 410ns, t_{RAS} = 250ns	4
I_{BB2}	V_{BB} Supply Current, Operating, $\overline{RAS}$-Only Refresh, Page Mode		150	300	µA	T_A = 0°C	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh			27	mA	2117-2, t_{RC} = 375ns, t_{RAS} = 150ns	4,6
				27	mA	2117-3, t_{RC} = 375ns, t_{RAS} = 200ns	4
				26	mA	2117-4, t_{RC} = 410ns, t_{RAS} = 250ns	4
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		1.5	3	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	
V_{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		
V_{IH}	Input High Voltage (all inputs)	2.4		6.0	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2mA	4
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -5mA	4

NOTES:
1. All voltages referenced to V_{SS}.
2. No power supply sequencing is required. However, V_{DD}, V_{CC} and V_{SS} should never be more negative than -0.3V with respect to V_{BB} as required by the absolute maximum ratings.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. See the Typical Characteristics Section for values of this parameter under alternate conditions.
5. I_{CC} is dependent on output loading when the device output is selected. V_{CC} is connected to the output buffer only. V_{CC} may be reduced to V_{SS} without affecting refresh operation or maintenance of internal device data.
6. For the 2117-2 at t_{RC} = 320ns, t_{RAS} = 150ns, I_{DD2} max. is 45mA and I_{DD3} max. is 31mA.

TYPICAL SUPPLY CURRENT WAVEFORMS



Typical power supply current waveforms vs. time are shown for the $\overline{RAS}/\overline{CAS}$ timings of Read/Write, Read/Write (Long $\overline{RAS}/\overline{CAS}$), and $\overline{RAS}$-only refresh cycles. I_{DD} and I_{BB} current transients at the $\overline{RAS}$ and $\overline{CAS}$ edges require adequate decoupling of these supplies. Decoupling recommendations are provided in the Applications section.

The effects of cycle time, V_{DD} supply voltage and ambient temperature on the I_{DD} current are shown in graphs included in the Typical Characteristics Section. Each family of curves for I_{DD1}, I_{DD2}, and I_{DD3} is related by a common point at $V_{DD} = 12.0V$ and $T_A = 25°C$ for two given t_{RAS} pulse widths. The typical I_{DD} current for a given condition of cycle time, V_{DD} and T_A can be determined by combining the effects of the appropriate family of curves.

CAPACITANCE [1]

$T_A = 25°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Typ.	Max.	Unit
C_{I1}	Address, Data In	3	5	pF
C_{I2}	$\overline{RAS}$ Capacitance, $\overline{WE}$ Capacitance	4	7	pF
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF
C_O	Data Output Capacitance	4	7	pF

NOTES:
1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.

A.C. CHARACTERISTICS[1,2,3]

T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

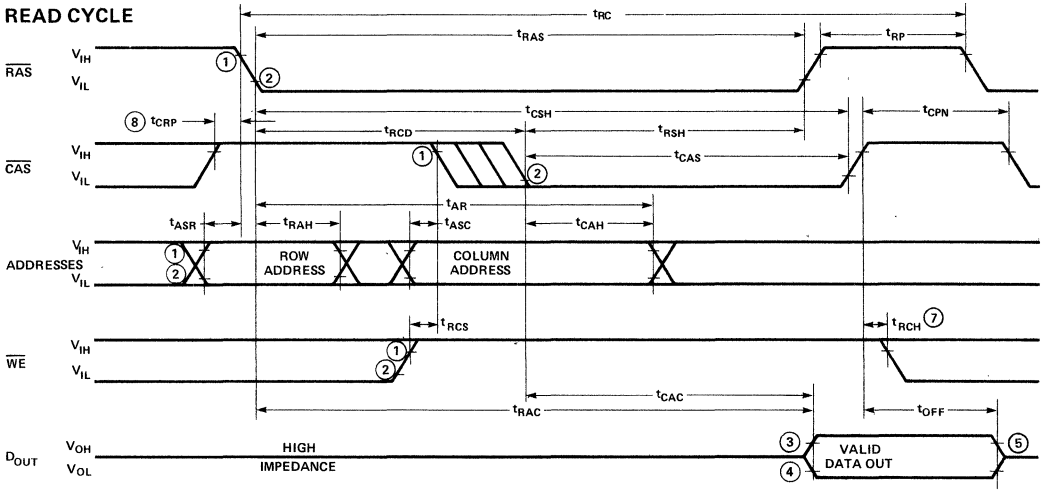
READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2117-2 Min.	2117-2 Max.	2117-3 Min.	2117-3 Max.	2117-4 Min.	2117-4 Max.	Unit	Notes
t_{RAC}	Access Time From $\overline{RAS}$		150		200		250	ns	4,5
t_{CAC}	Access Time From $\overline{CAS}$		100		135		165	ns	4,5,6
t_{REF}	Time Between Refresh		2		2		2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time(non-page cycles)	25		25		25		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	-20		-20		-20		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	ns	7
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-Up Time	-10		-10		-10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time, to $\overline{RAS}$	95		120		160		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{OFF}	Output Buffer Turn Off Delay	0	50	0	60	0	70	ns	
READ AND REFRESH CYCLES									
t_{RC}	Random Read Cycle Time	320		375		410		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10000	135	10000	165	10000	ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
WRITE CYCLE									
t_{RC}	Random Write Cycle Time	320		375		410		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10000	135	10000	165	10000	ns	
t_{WCS}	Write Command Set-Up Time	-20		-20		-20		ns	9
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time, to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		80		100		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		80		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	
t_{DH}	Data-In Hold Time	45		55		75		ns	
t_{DHR}	Data-In Hold Time, to $\overline{RAS}$	95		120		160		ns	
READ-MODIFY-WRITE CYCLE									
t_{RWC}	Read-Modify-Write Cycle Time	330		375		475		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	185	10000	245	10000	305	10000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	135	10000	180	10000	230	10000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		160		200		ns	9
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	70		95		125		ns	9

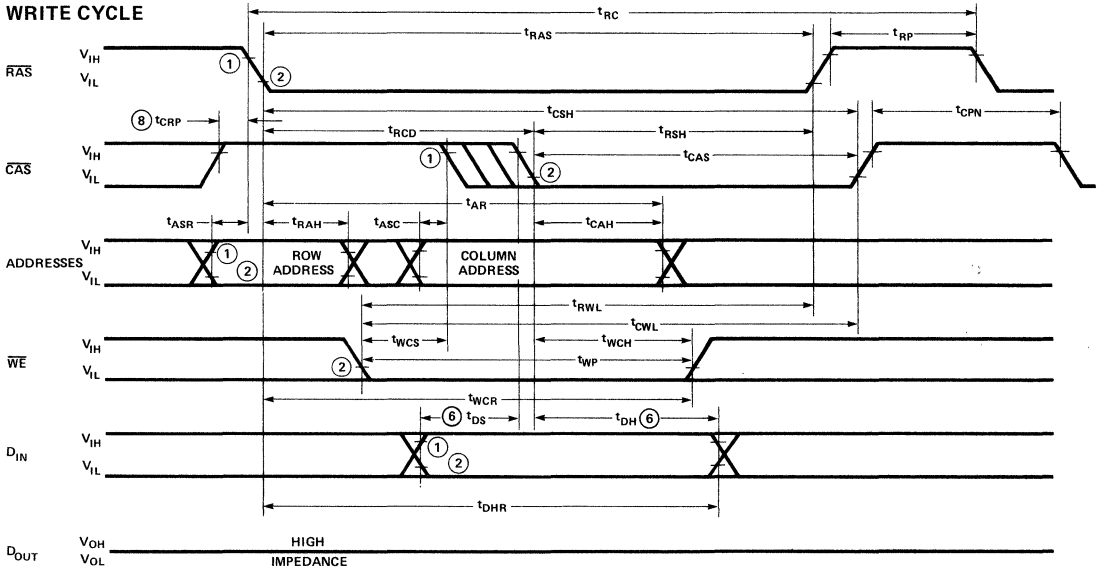
Notes: See following page for A.C. Characteristics Notes.

WAVEFORMS

READ CYCLE



WRITE CYCLE



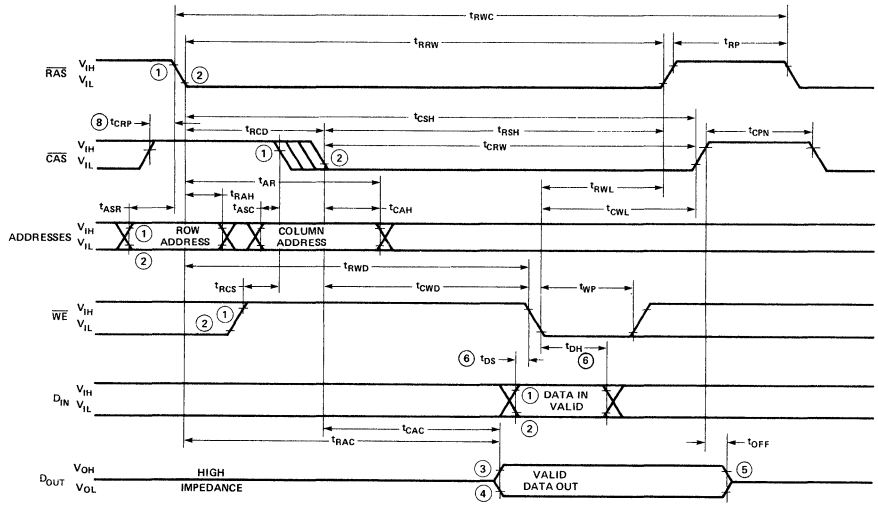
NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

A.C. CHARACTERISTICS NOTES (From Previous Page)

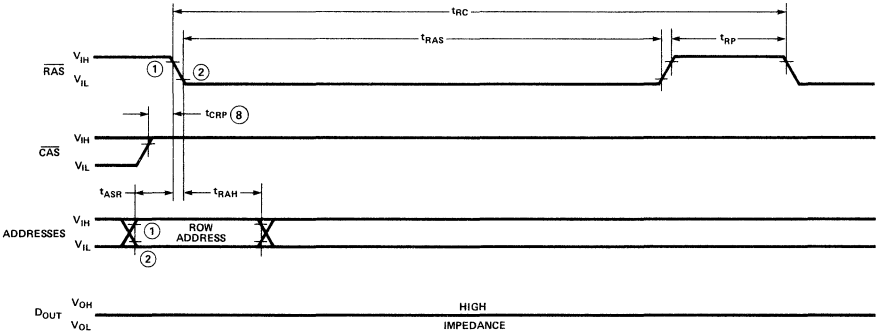
1. All voltages referenced to V_{SS}.
2. Eight cycles are required after power-up or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. A.C. Characteristics assume $t_T = 5ns$.
4. Assume that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Load = 2 TTL loads and 100pF.
6. Assumes $t_{RCD} \geq t_{RCD}$ (max.).
7. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC}, if t_{RCD} is greater than t_{RCD} (max.) access time is $t_{RCD} + t_{CAC}$.
8. t_T is measured between V_{IH} (min.) and V_{IL} (max.).
9. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

WAVEFORMS

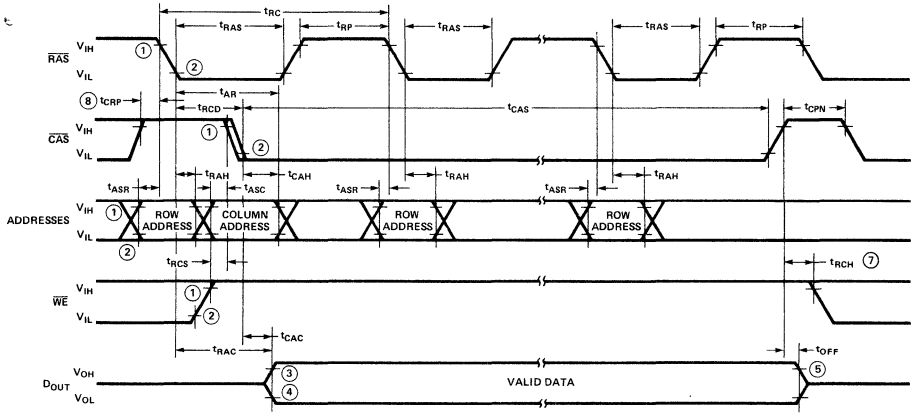
READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



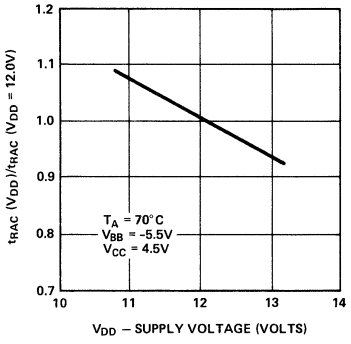
HIDDEN REFRESH CYCLE



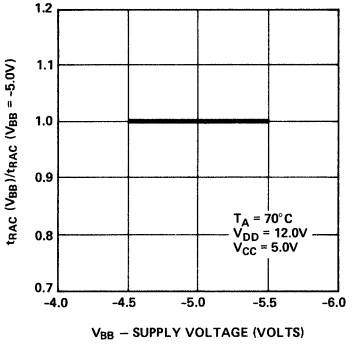
NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

TYPICAL CHARACTERISTICS[1]

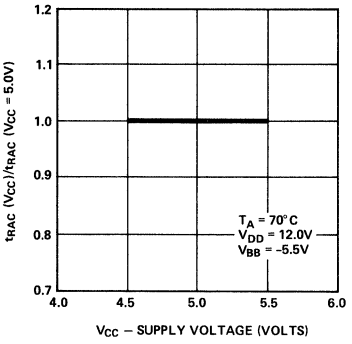
GRAPH 1
TYPICAL ACCESS TIME t_{RAC} (NORMALIZED) VS. V_{DD}



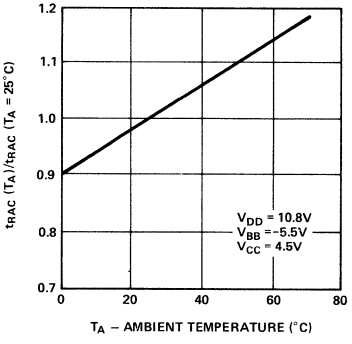
GRAPH 2
TYPICAL ACCESS TIME t_{RAC} (NORMALIZED) VS. V_{BB}



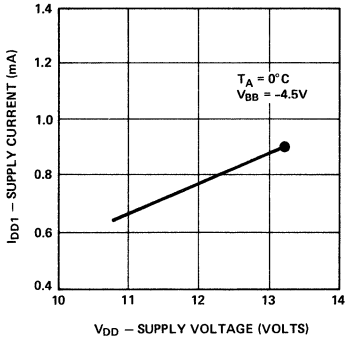
GRAPH 3
TYPICAL ACCESS TIME t_{RAC} (NORMALIZED) VS. V_{CC}



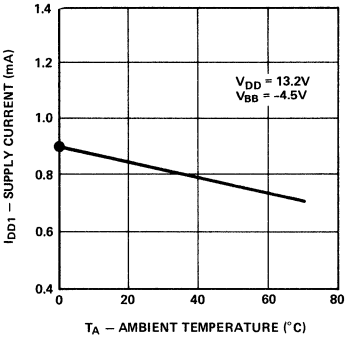
GRAPH 4
TYPICAL ACCESS TIME t_{RAC} (NORMALIZED) VS. AMBIENT TEMPERATURE



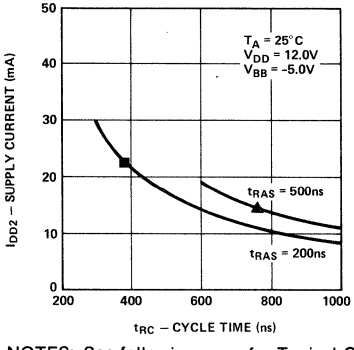
GRAPH 5
TYPICAL STANDBY CURRENT I_{DD1} VS. V_{DD}



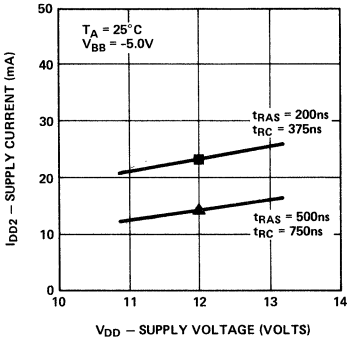
GRAPH 6
TYPICAL STANDBY CURRENT I_{DD1} VS. AMBIENT TEMPERATURE



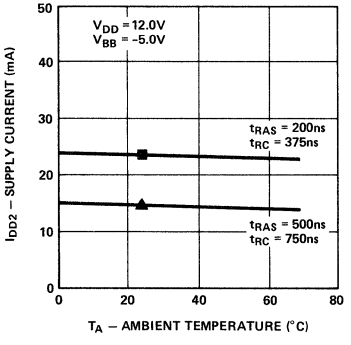
GRAPH 7
TYPICAL OPERATING CURRENT I_{DD2} VS. t_{RC}



GRAPH 8
TYPICAL OPERATING CURRENT I_{DD2} VS. V_{DD}



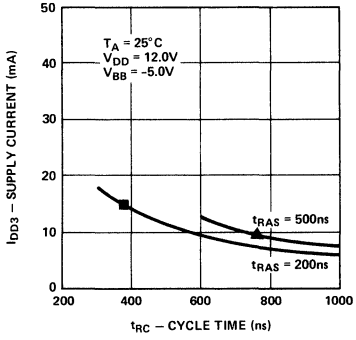
GRAPH 9
TYPICAL OPERATING CURRENT I_{DD2} VS. AMBIENT TEMPERATURE



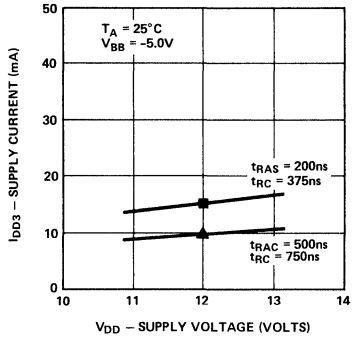
NOTES: See following page for Typical Characteristics Notes.

TYPICAL CHARACTERISTICS [1]

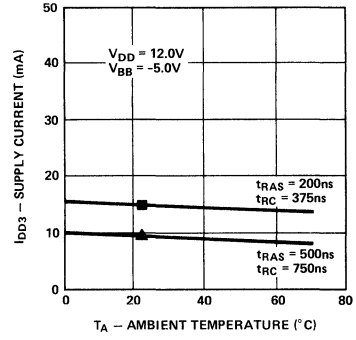
GRAPH 10
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. t_{RC}



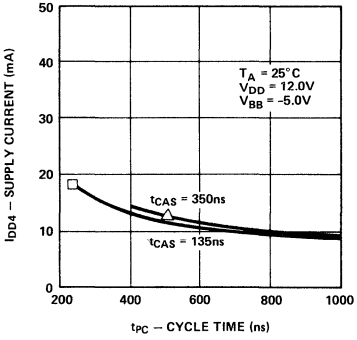
GRAPH 11
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. V_{DD}



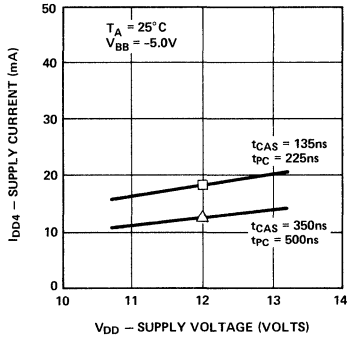
GRAPH 12
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. AMBIENT TEMPERATURE



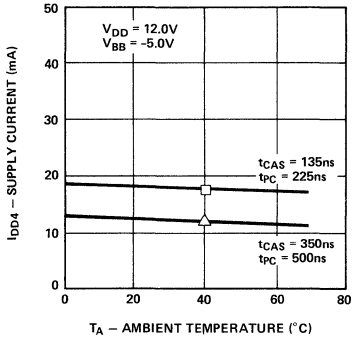
GRAPH 13
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. t_{PC}



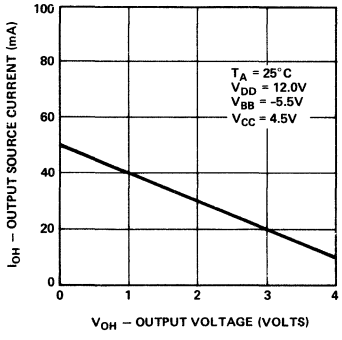
GRAPH 14
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. V_{DD}



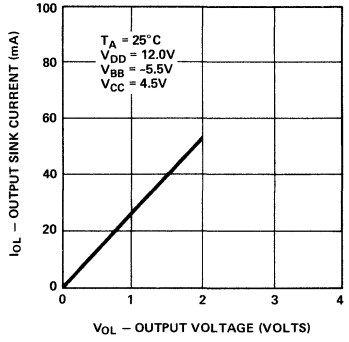
GRAPH 15
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. AMBIENT TEMPERATURE



GRAPH 16
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} VS. OUTPUT VOLTAGE V_{OH}



GRAPH 17
TYPICAL OUTPUT SINK CURRENT
I_{OL} VS. OUTPUT VOLTAGE V_{OL}



NOTES:

1. The cycle time, V_{DD} supply voltage, and ambient temperature dependence of I_{DD1}, I_{DD2}, I_{DD3} and I_{DD4} is shown in related graphs. Common points of related curves are indicated:
   - ● I_{DD1} @ V_{DD} = 13.2V, T_A = 0°C
   - ■ I_{DD2} or I_{DD3} @ t_{RAS} = 200ns, t_{RC} = 375ns, V_{DD} = 12.0V, T_A = 25°C
   - ▲ I_{DD2} or I_{DD3} @ t_{RAS} = 500ns, t_{RC} = 750ns, V_{DD} = 12.0V, T_A = 25°C
   - □ I_{DD4} @ t_{CAS} = 135ns, t_{PC} = 225ns, V_{DD} = 12.0V, T_A = 25°C
   - △ I_{DD4} @ t_{CAS} = 350ns, t_{PC} = 500ns, V_{DD} = 12.0V, T_A = 25°C

   The typical I_{DD} current for a given combination of cycle time, V_{DD} supply voltage and ambient temperature may be determined by combining the effects of the appropriate family of curves.

D.C. AND A.C. CHARACTERISTICS, PAGE MODE [7,8,11]

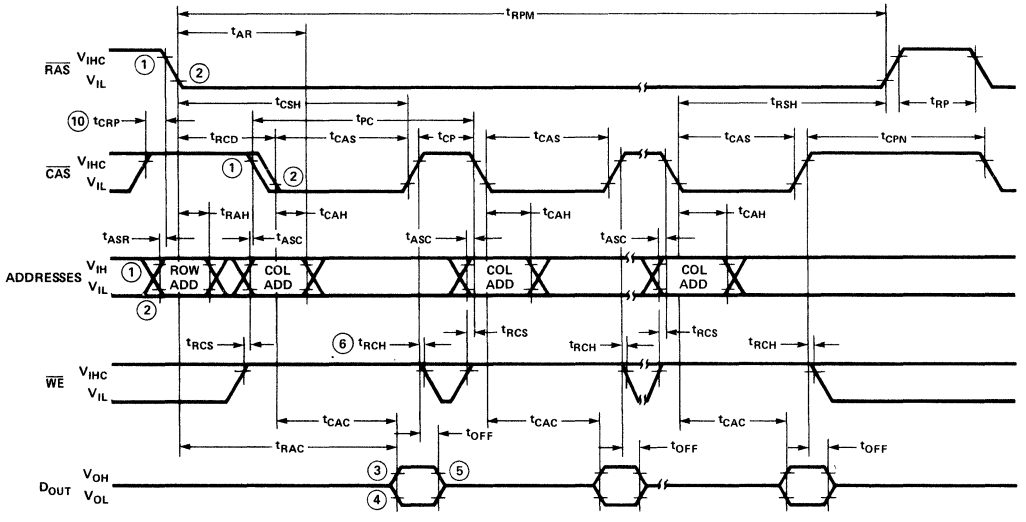
T_A = 0°C to 70°C, V_{DD} = 12V±10%, V_{CC} = 5V±10%, V_{BB} = -5V±10%, V_{SS} = 0V, unless otherwise noted.

For Page Mode Operation order 2117-2 S6053, 2117-3 S6054, or 2117-4 S6055.

Symbol	Parameter	2117-2 S6053		2117-3 S6054		2117-4 S6055		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PC}	Page Mode Read or Write Cycle	170		225		275		ns	
t_{PCM}	Page Mode Read Modify Write	205		270		340		ns	
t_{CP}	$\overline{CAS}$ Precharge Time, Page Cycle	60		80		100		ns	
t_{RPM}	$\overline{RAS}$ Pulse Width, Page Mode	150	10,000	200	10,000	250	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	165	10,000	ns	
I_{DD4}	V_{DD} Supply Current Page Mode, Minimum t_{PC}, Minimum t_{CAS}		38		30		26	mA	9

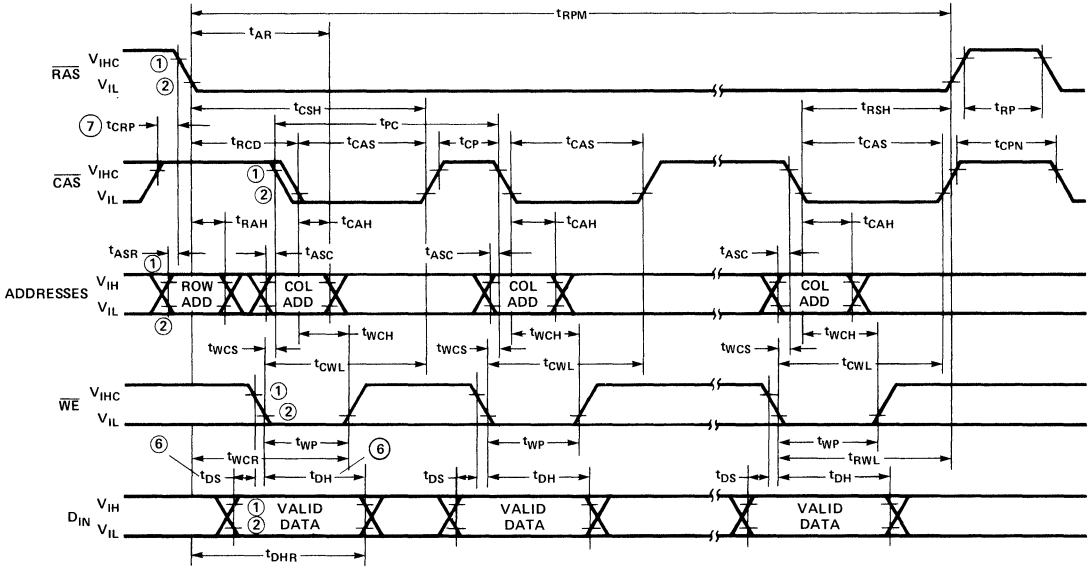
WAVEFORMS

PAGE MODE READ CYCLE

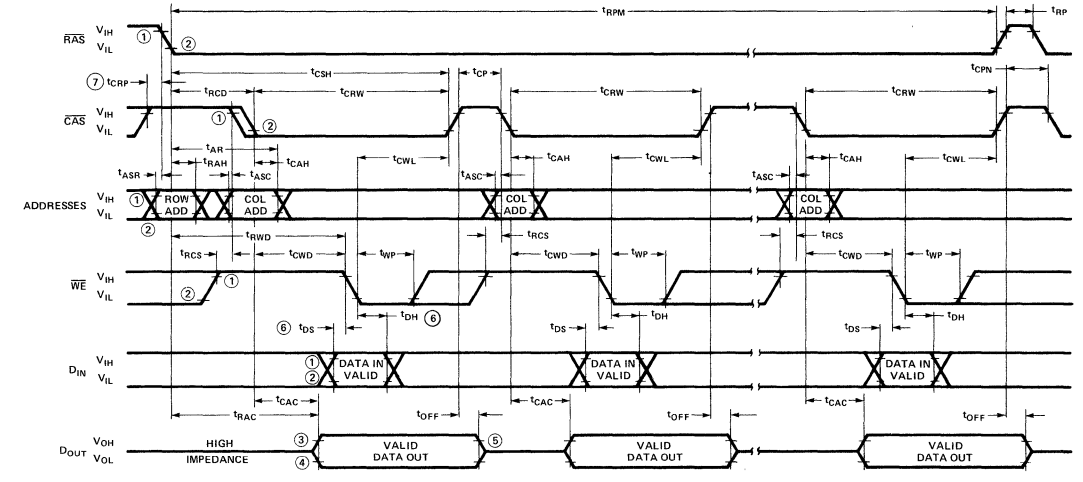


NOTES:
1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
7. ALL VOLTAGES REFERENCED TO V_{SS}.
8. AC CHARACTERISTIC ASSUME t_T = 5ns.
9. SEE THE TYPICAL CHARACTERISTICS SECTION FOR VALUES OF THIS PARAMETER UNDER ALTERNATE CONDITIONS.
10. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).
11. ALL PREVIOUSLY SPECIFIED A.C. AND D.C. CHARACTERISTICS ARE APPLICABLE TO THEIR RESPECTIVE PAGE MODE DEVICE (i.e., 2117-3, S6054 WILL OPERATE AS A 2117-3).

PAGE MODE WRITE CYCLE



PAGE MODE READ-MODIFY-WRITE CYCLE



NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

APPLICATIONS

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during a $\overline{RAS}/\overline{CAS}$ operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time.

Device access time, t_{ACC}, is the longer of the two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCD} + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe delay time, t_{RCD}, are system dependent timing parameters. For example, substituting the device parameters of the 2117-3 yields:

3. $t_{ACC} = t_{RAC} = 200nsec$ for $25nsec \leq t_{RCD} \leq 65nsec$

OR

4. $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD} + 135$ for $t_{RCD} > 65nsec$

Note that if $25nsec \leq t_{RCD} \leq 65nsec$ device access time is determined by equation 3 and is equal to t_{RAC}. If $t_{RCL} > 65nsec$, access time is determined by equation 4. This 40nsec interval (shown in the t_{RCD} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$.

REFRESH CYCLES

Each of the 128 rows of the 2117 must be refreshed every 2 milliseconds to maintain data. Any memory cycle:

1. Read Cycle
2. Write Cycle (Early Write, Delayed Write or Read-Modify-Write)
3. $\overline{RAS}$-only Cycle

refreshes the selected row as defined by the low order ($\overline{RAS}$) addresses. Any Write cycle, of course, may change the state of the selected cell. Using a Read, Write, or Read-Modify-Write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the D_{OUT} in the high impedance state with a typical power reduction of 20% over a Read or Write cycle.

$\overline{RAS}/\overline{CAS}$ TIMING

$\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle can not begin until the minimum precharge time, t_{RP}, has been met.

DATA OUTPUT OPERATION

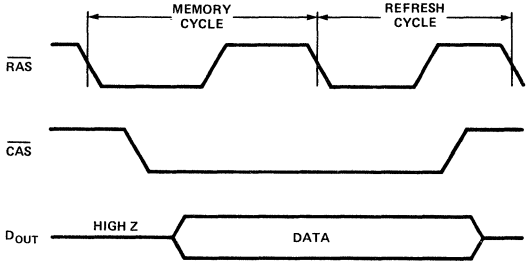
The 2117 Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}) the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

Intel 2117 Data Output Operation for Various Types of Cycles

Type of Cycle	D_{OUT} State
Read Cycle	Data From Addressed Memory Cell
Early Write Cycle	HI-Z
$\overline{RAS}$-Only Refresh Cycle	HI-Z
$\overline{CAS}$-Only Cycle	HI-Z
Read/Modify/Write Cycle	Data From Addressed Memory Cell
Delayed Write Cycle	Indeterminate

HIDDEN REFRESH

A feature of the 2117 is that refresh cycles may be performed while maintaining valid data at the output pin. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see Figure below).



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

POWER ON

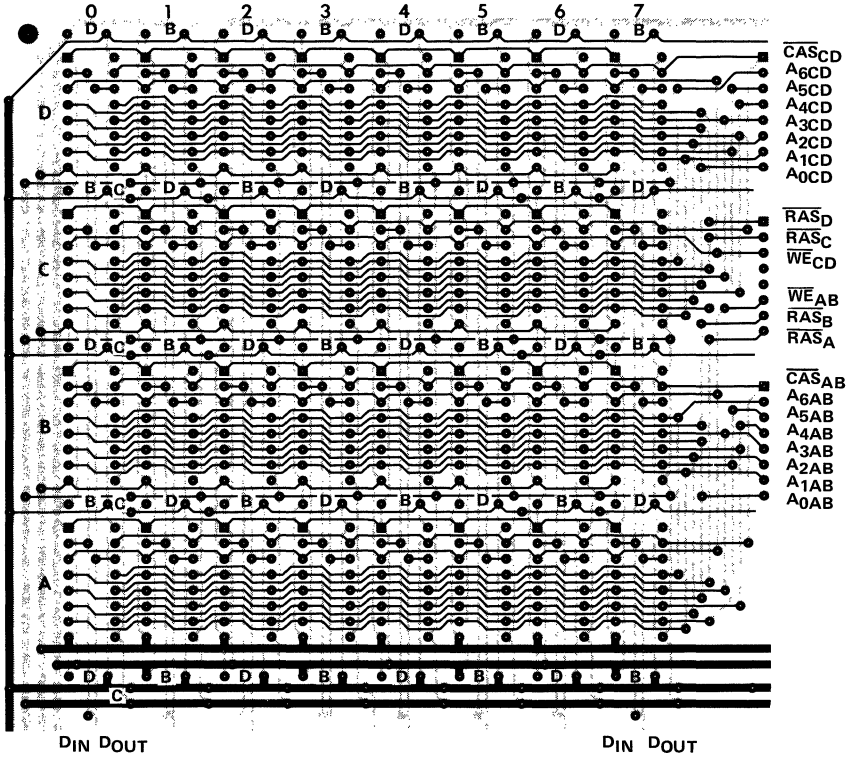
The 2117 requires no power on sequence providing absolute maximum ratings are not exceeded. After the application of supply voltages or after extended periods of bias (greater than 2 milliseconds) without clocks, the device must perform a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock, such as $\overline{RAS}$-Only refresh) prior to normal operation.

POWER SUPPLY DECOUPLING/DISTRIBUTION

It is recommended that a 0.1μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

The V_{CC} supply is connected only to the 2117 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is associated with the input high level current to a TTL gate and the output leakage currents of any OR-tied 2117's (typically 100μA or less total). Intel recommends that a 0.1 or 0.01μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight memory devices.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1μF TO V_{DD} TO V_{SS}
B = 0.1μF V_{BB} TO V_{SS}
C = 0.01μF V_{CC} TO V_{SS}

SAMPLE P.C. BOARD LAYOUT EMPLOYING VERTICAL AND HORIZONTAL GRIDDING ON ALL POWER SUPPLIES.

BOARD ORGANIZATION: 64K WORDS BY 8-BITS.

64K BYTE STORAGE ARRAY LAYOUT

2117-5
16,384 x 1 BIT DYNAMIC RAM

	2117-5
Maximum Access Time (ns)	300
Read, Write Cycle (ns)	490
Read-Modify-Write Cycle (ns)	580

- **Industry Standard 16-Pin Configuration**
- **Low Power: 462mW Max. Operating, 20mW Max. Standby**
- **Low I_{DD} Current Transients**
- **All Inputs, Including Clocks, TTL Compatible**
- **$\overline{RAS}$ Only Refresh**
- **Non-Latched Output is Three-State, TTL Compatible**
- **128 Refresh Cycles Required Every 2ms**
- **Page Mode Capability**
- **$\overline{CAS}$ Controlled Output Allows Hidden Refresh**

The Intel® 2117 is a 16,384 word by 1-bit Dynamic MOS RAM fabricated with Intel's standard two layer polysilicon NMOS technology — a production proven process for high performance, high reliability, and high storage density.

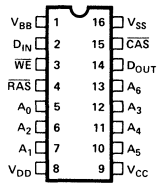
The 2117 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients contribute to the high noise immunity of the 2117 in a system environment.

Multiplexing the 14 address bits into the 7 address input pins allows the 2117 to be packaged in the industry standard 16-pin DIP. The two 7-bit address words are latched into the 2117 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical timing requirements for $\overline{RAS}$ and $\overline{CAS}$ allow use of the address multiplexing technique while maintaining high performance.

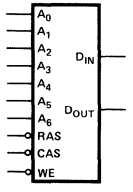
The 2117 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is latched on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The 2117 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain latched data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2ms period. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

PIN CONFIGURATION



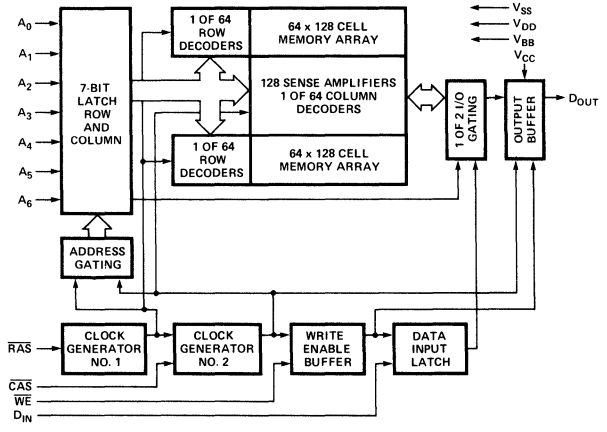
LOGIC SYMBOL



PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin Relative to V_{BB}
($V_{SS} - V_{BB} \geq 4V$) ..... -0.3V to +20V
Data Out Current 50mA
Power Dissipation 1.0W

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

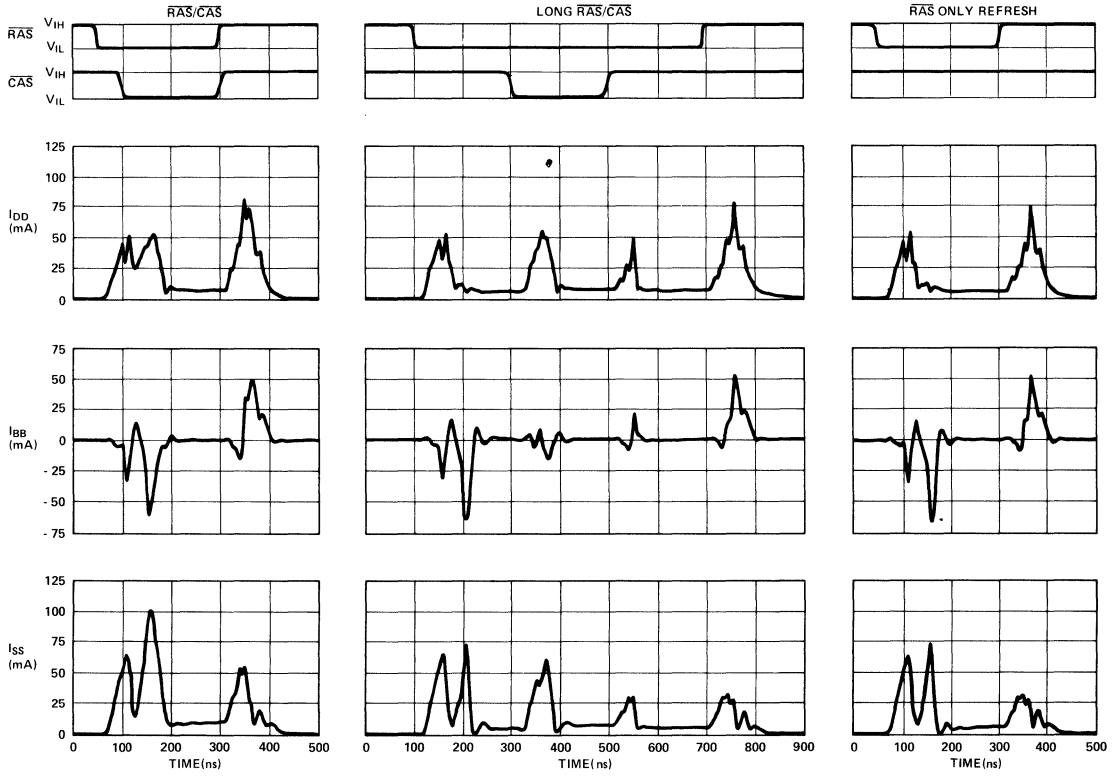
D.C. AND OPERATING CHARACTERISTICS[1,2]

T_A = 0°C to 70°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits Min.	Typ.[3]	Max.	Unit	Test Conditions	Notes
$\|I_{LI}\|$	Input Load Current (any input)		0.1	10	µA	V_{IN}=V_{SS} to V_{IHMAX}, V_{BB}=-5.0V	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State		0.1	10	µA	Chip Deselected: $\overline{CAS}$ at V_{IH}, V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current, Standby			1.5	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	4
I_{BB1}	V_{BB} Supply Current, Standby		1.0	50	µA		
I_{CC1}	V_{CC} Supply Current, Output Deselected		0.1	10	µA	$\overline{CAS}$ at V_{IH}	5
I_{DD2}	V_{DD} Supply Current, Operating			35	mA	2117, t_{RC} = 490ns, t_{RAS} = 300ns	4
I_{BB2}	V_{BB} Supply Current, Operating, $\overline{RAS}$-Only Refresh, Page Mode		150	400	µA	T_A = 0°C	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh			27	mA	2117, t_{RC} = 490ns, t_{RAS} = 300ns	4
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		1.5	3	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	
V_{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		
V_{IH}	Input High Voltage (all inputs)	2.4		6.0	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2mA	4
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -5mA	4

NOTES:
1. All voltages referenced to V_{SS}.
2. No power supply sequencing is required. However, V_{DD}, V_{CC} and V_{SS} should never be more negative than -0.3V with respect to V_{BB} as required by the absolute maximum ratings.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. See the Typical Characteristics Section for values of this parameter under alternate conditions.
5. I_{CC} is dependent on output loading when the device output is selected. V_{CC} is connected to the output buffer only. V_{CC} may be reduced to V_{SS} without affecting refresh operation or maintenance of internal device data.

TYPICAL SUPPLY CURRENT WAVEFORMS



Typical power supply current waveforms vs. time are shown for the $\overline{RAS}/\overline{CAS}$ timings of Read/Write, Read/Write (Long $\overline{RAS}/\overline{CAS}$), and $\overline{RAS}$-only refresh cycles. I_{DD} and I_{BB} current transients at the $\overline{RAS}$ and $\overline{CAS}$ edges require adequate decoupling of these supplies. Decoupling recommendations are provided in the Applications section.

The effects of cycle time, V_{DD} supply voltage and ambient temperature on the I_{DD} current are shown in graphs included in the Typical Characteristics Section. Each family of curves for I_{DD1}, I_{DD2}, and I_{DD3} is related by a common point at $V_{DD} = 12.0V$ and $T_A = 25°C$ for two given t_{RAS} pulse widths. The typical I_{DD} current for a given condition of cycle time, V_{DD} and T_A can be determined by combining the effects of the appropriate family of curves.

CAPACITANCE [1]

$T_A = 25°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Typ.	Max.	Unit
C_{I1}	Address, Data In	3	5	pF
C_{I2}	$\overline{RAS}$ Capacitance, $\overline{WE}$ Capacitance	4	7	pF
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF
C_O	Data Output Capacitance	4	7	pF

NOTES:
1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.

A.C. CHARACTERISTICS[1,2,3]

T_A = 0°C to 70°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

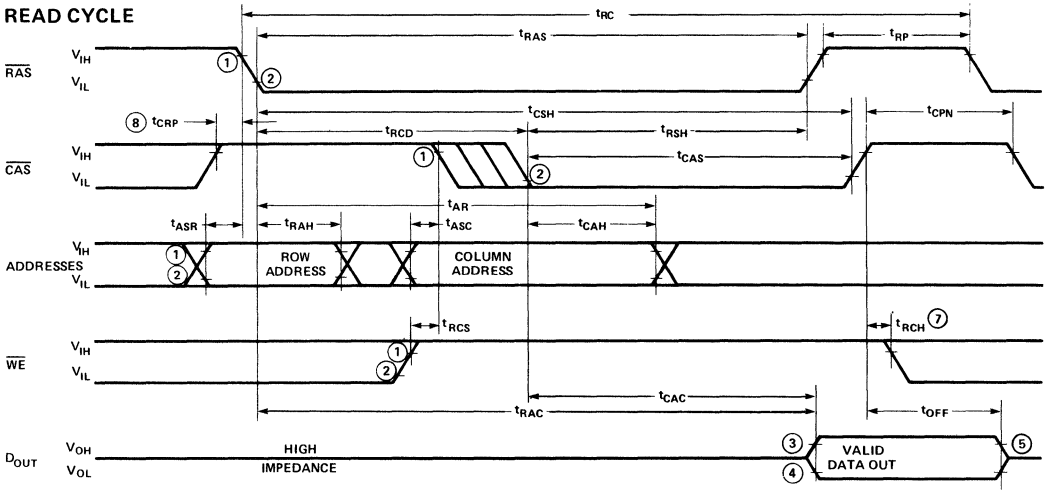
READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2117 Min.	2117 Max.	Unit	Notes
t_{RAC}	Access Time From $\overline{RAS}$		300	ns	4,5
t_{CAC}	Access Time From $\overline{CAS}$		180	ns	4,5,6
t_{REF}	Time Between Refresh		2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	180		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time(non-page cycles)	80		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	-20		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	80	120	ns	7
t_{RSH}	$\overline{RAS}$ Hold Time	180		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	300		ns	
t_{ASR}	Row Address Set-Up Time	0		ns	
t_{RAH}	Row Address Hold Time	80		ns	
t_{ASC}	Column Address Set-Up Time	0		ns	
t_{CAH}	Column Address Hold Time	80		ns	
t_{AR}	Column Address Hold Time, to $\overline{RAS}$	215		ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{OFF}	Output Buffer Turn Off Delay	0	80	ns	
READ AND REFRESH CYCLES					
t_{RC}	Random Read Cycle Time	490		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	300	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	180	10000	ns	
t_{RCS}	Read Command Set-Up Time	0		ns	
t_{RCH}	Read Command Hold Time	0		ns	
WRITE CYCLE					
t_{RC}	Random Write Cycle Time	490		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	300	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	180	10000	ns	
t_{WCS}	Write Command Set-Up Time	0		ns	9
t_{WCH}	Write Command Hold Time	100		ns	
t_{WCR}	Write Command Hold Time, to $\overline{RAS}$	215		ns	
t_{WP}	Write Command Pulse Width	100		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	130		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	130		ns	
t_{DS}	Data-In Set-Up Time	0		ns	
t_{DH}	Data-In Hold Time	80		ns	
t_{DHR}	Data-In Hold Time, to $\overline{RAS}$	215		ns	
READ-MODIFY-WRITE CYCLE					
t_{RWC}	Read-Modify-Write Cycle Time	580		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	390	10000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	275	10000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	260		ns	9
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	140		ns	9

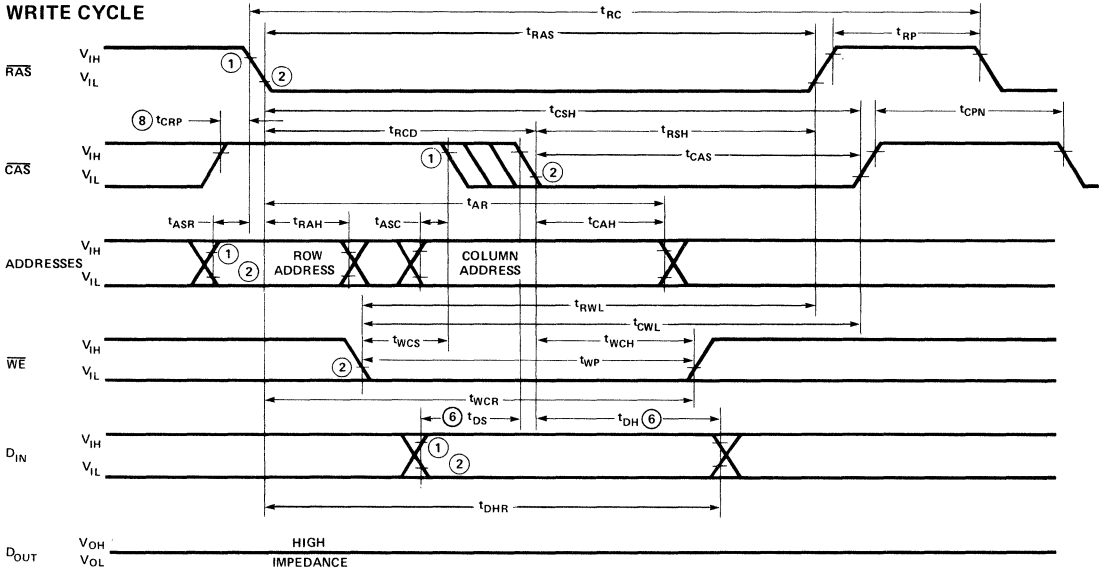
Notes: See following page for A.C. Characteristics Notes.

WAVEFORMS

READ CYCLE



WRITE CYCLE



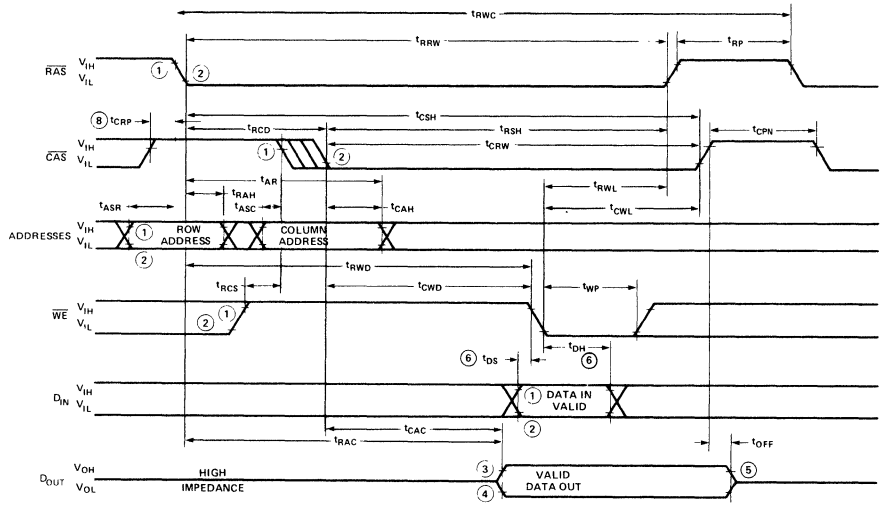
NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

A.C. CHARACTERISTICS NOTES (From Previous Page)

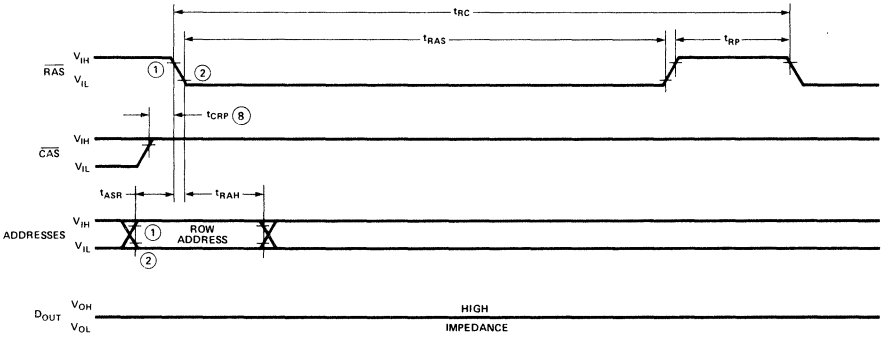
1. All voltages referenced to V_{SS}.
2. Eight cycles are required after power-up or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. A.C. Characteristics assume t_T = 5ns.
4. Assume that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Load = 2 TTL loads and 100pF.
6. Assumes $t_{RCD} \geq t_{RCD}$ (max.).
7. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC}, if t_{RCD} is greater than t_{RCD} (max.) access time is $t_{RCD} + t_{CAC}$.
8. t_T is measured between V_{IH} (min.) and V_{IL} (max.).
9. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

WAVEFORMS

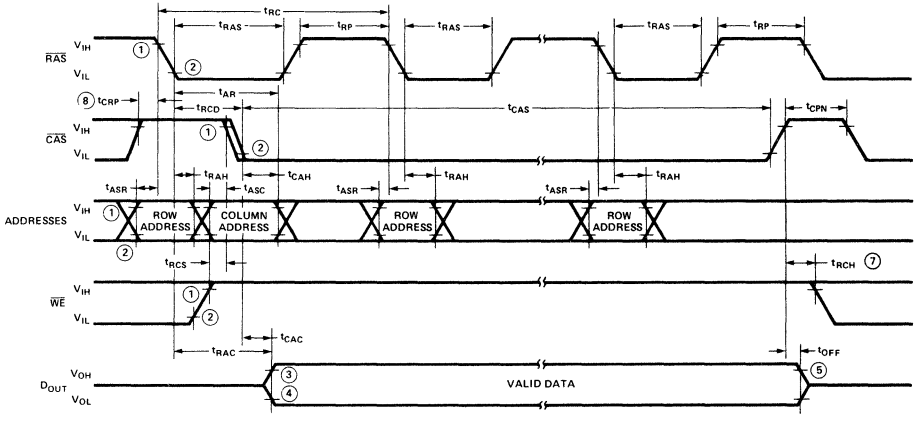
READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



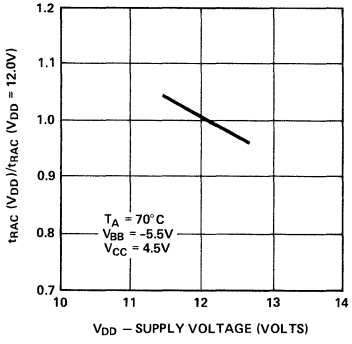
HIDDEN REFRESH CYCLE



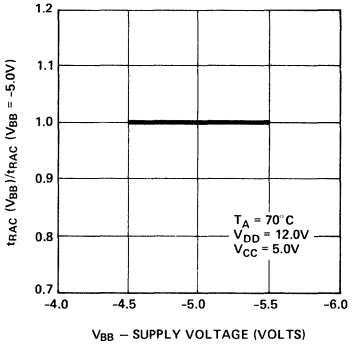
NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

TYPICAL CHARACTERISTICS[1]

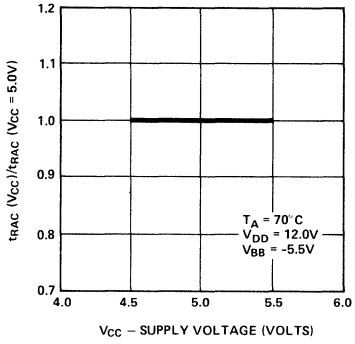
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{DD}



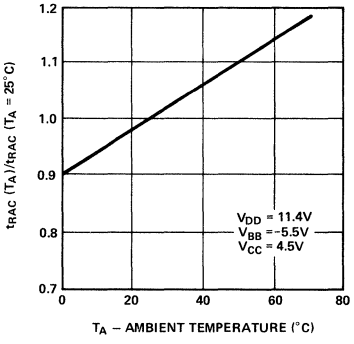
GRAPH 2
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{BB}



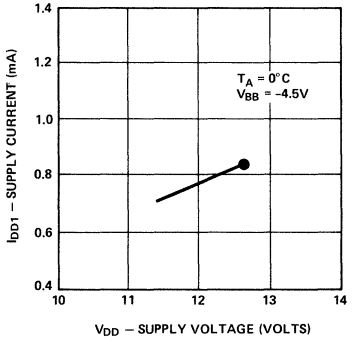
GRAPH 3
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS. V_{CC}



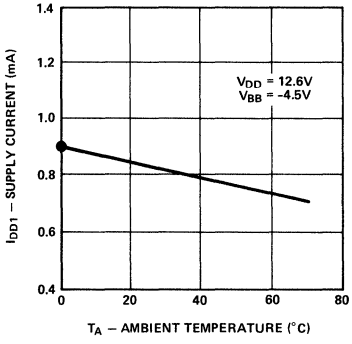
GRAPH 4
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) VS.
AMBIENT TEMPERATURE



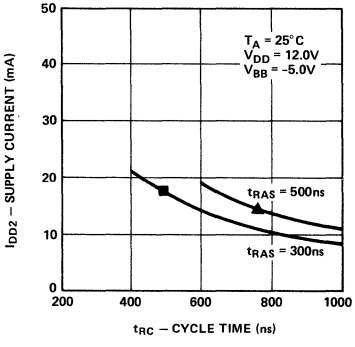
GRAPH 5
TYPICAL STANDBY CURRENT
I_{DD1} VS. V_{DD}



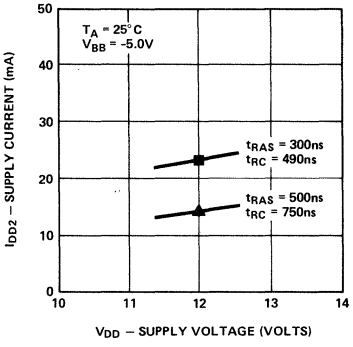
GRAPH 6
TYPICAL STANDBY CURRENT
I_{DD1} VS. AMBIENT TEMPERATURE



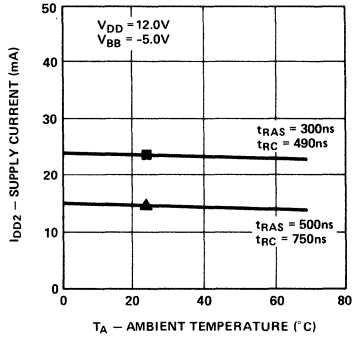
GRAPH 7
TYPICAL OPERATING CURRENT
I_{DD2} VS. t_{RC}



GRAPH 8
TYPICAL OPERATING CURRENT
I_{DD2} VS. V_{DD}



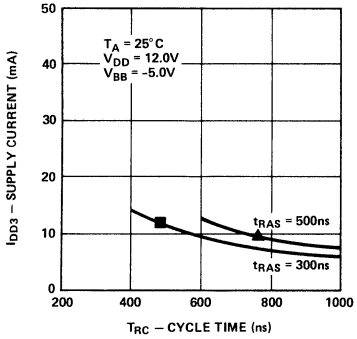
GRAPH 9
TYPICAL OPERATING CURRENT
I_{DD2} VS. AMBIENT TEMPERATURE



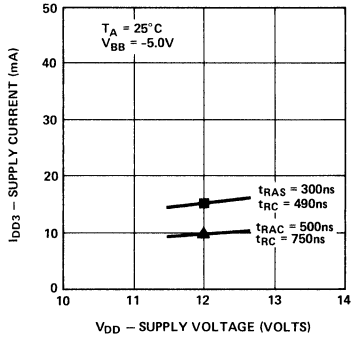
NOTES: See following page for Typical Characteristics Notes.

TYPICAL CHARACTERISTICS [1]

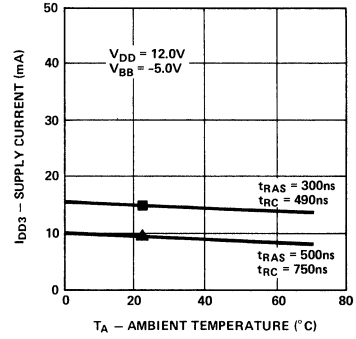
GRAPH 10
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. t_{RC}



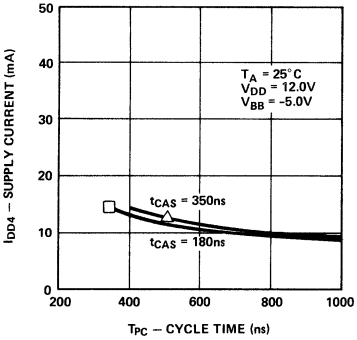
GRAPH 11
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. V_{DD}



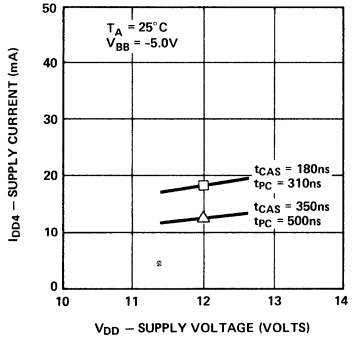
GRAPH 12
TYPICAL $\overline{RAS}$ ONLY
REFRESH CURRENT
I_{DD3} VS. AMBIENT TEMPERATURE



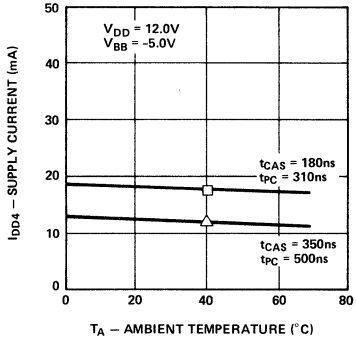
GRAPH 13
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. t_{PC}



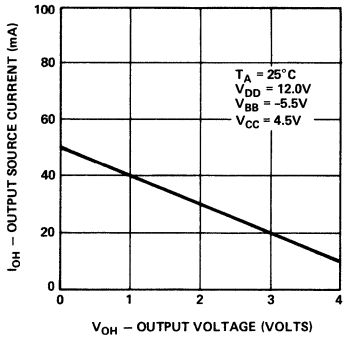
GRAPH 14
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. V_{DD}



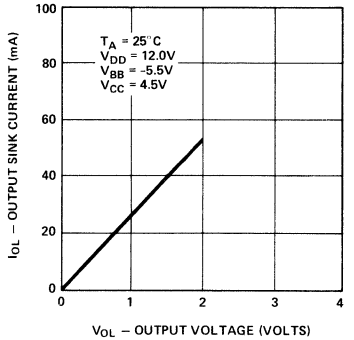
GRAPH 15
TYPICAL PAGE MODE CURRENT
I_{DD4} VS. AMBIENT TEMPERATURE



GRAPH 16
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} VS. OUTPUT VOLTAGE V_{OH}



GRAPH 17
TYPICAL OUTPUT SINK CURRENT
I_{OL} VS. OUTPUT VOLTAGE V_{OL}



NOTES:

1. The cycle time, V_{DD} supply voltage, and ambient temperature dependence of I_{DD1}, I_{DD2}, I_{DD3} and I_{DD4} is shown in related graphs. Common points of related curves are indicated:
   - ● I_{DD1} @ V_{DD} = 12.6V, T_A = 0°C
   - ■ I_{DD2} or I_{DD3} @ t_{RAS} = 300ns, t_{RC} = 490ns, V_{DD} = 12.0V, T_A = 25°C
   - ▲ I_{DD2} or I_{DD3} @ t_{RAS} = 500ns, t_{RC} = 750ns, V_{DD} = 12.0V, T_A = 25°C
   - □ I_{DD4} @ t_{CAS} = 180ns, t_{PC} = 310ns, V_{DD} = 12.0V, T_A = 25°C
   - △ I_{DD4} @ t_{CAS} = 350ns, t_{PC} = 500ns, V_{DD} = 12.0V, T_A = 25°C

   The typical I_{DD} current for a given combination of cycle time, V_{DD} supply voltage and ambient temperature may be determined by combining the effects of the appropriate family of curves.

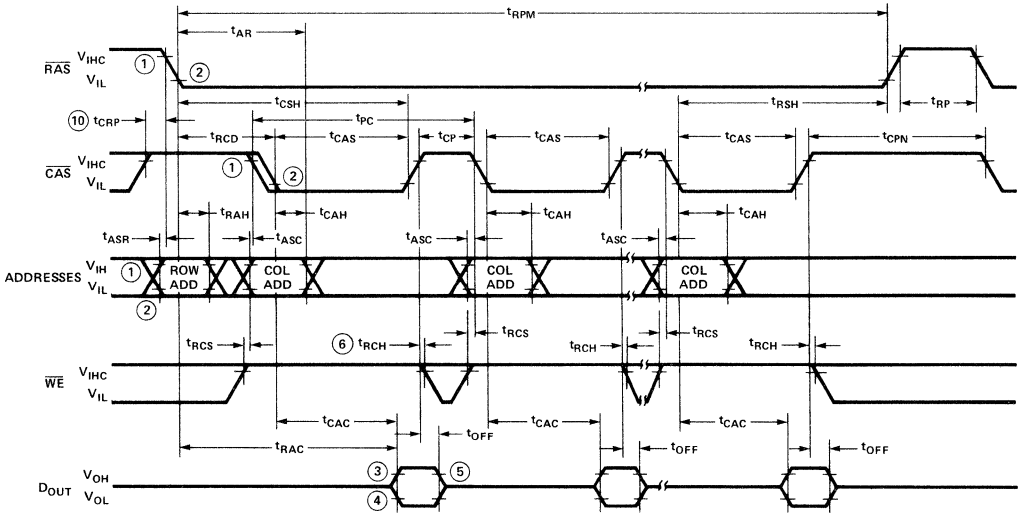
D.C. AND A.C. CHARACTERISTICS, PAGE MODE [7,8,11]

T_A = 0°C to 70°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.
For Page Mode Operation order 2117 S6117.

Symbol	Parameter	2117-5 S6117 Min.	2117-5 S6117 Max.	Unit	Notes
t_{PC}	Page Mode Read or Write Cycle	310		ns	
t_{PCM}	Page Mode Read Modify Write	405		ns	
t_{CP}	$\overline{CAS}$ Precharge Time, Page Cycle	120		ns	
t_{RPM}	$\overline{RAS}$ Pulse Width, Page Mode	300	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	180	10,000	ns	
I_{DD4}	V_{DD} Supply Current Page Mode, Minimum t_{PC}, Minimum t_{CAS}		26	mA	9

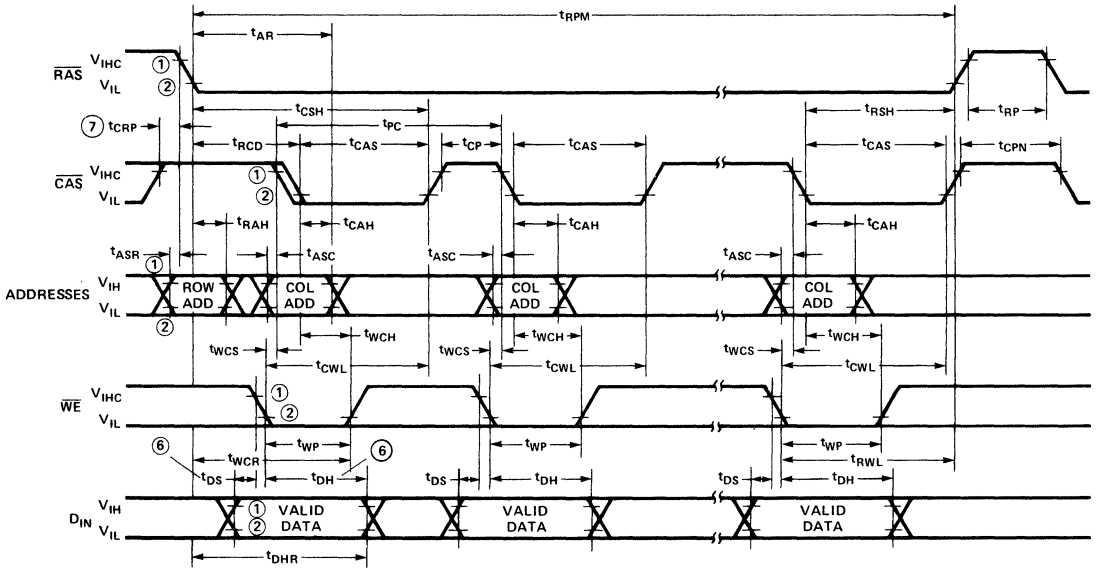
WAVEFORMS

PAGE MODE READ CYCLE

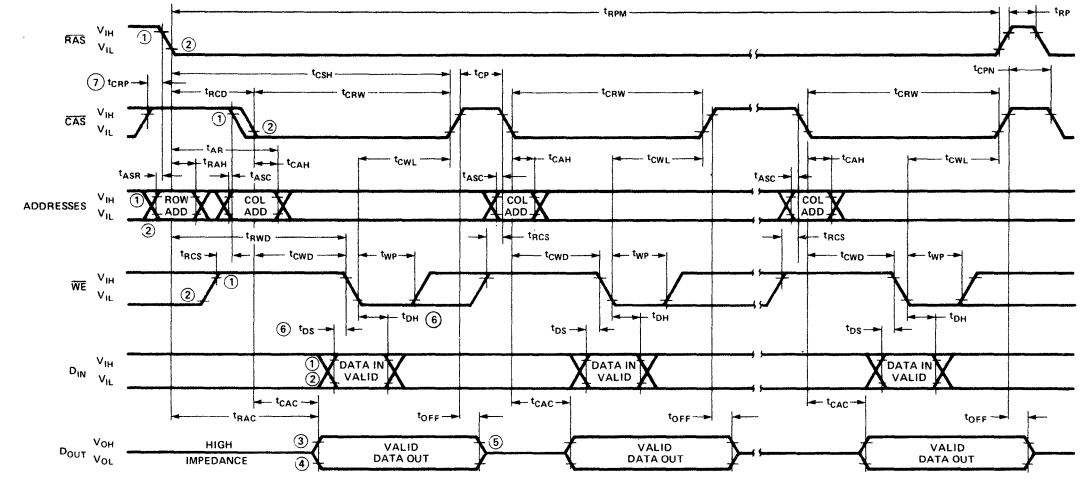


NOTES:
1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
7. ALL VOLTAGES REFERENCED TO V_{SS}.
8. AC CHARACTERISTIC ASSUME t_T = 5ns.
9. SEE THE TYPICAL CHARACTERISTICS SECTION FOR VALUES OF THIS PARAMETER UNDER ALTERNATE CONDITIONS.
10. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).
11. ALL PREVIOUSLY SPECIFIED A.C. AND D.C. CHARACTERISTICS ARE APPLICABLE TO THEIR RESPECTIVE PAGE MODE DEVICE (i.e., 2117-5, S6117 WILL OPERATE AS A 2117-5).

PAGE MODE WRITE CYCLE



PAGE MODE READ-MODIFY-WRITE CYCLE



NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

APPLICATIONS

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during a $\overline{RAS}/\overline{CAS}$ operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time.

Device access time, t_{ACC}, is the longer of the two calculated intervals:

1. $t_{ACC} = t_{RAC}$ OR 2. $t_{ACC} = t_{RCD} + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe delay time, t_{RCD}, are system dependent timing parameters. For example, substituting the device parameters of the 2117 yields:

3. $t_{ACC} = t_{RAC} = 300nsec$ for $80nsec \leq t_{RCD} \leq 120nsec$

OR

4. $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD} + 180$ for $t_{RCD} > 120nsec$

Note that if $80nsec \leq t_{RCD} \leq 120nsec$ device access time is determined by equation 3 and is equal to t_{RAC}. If $t_{RCD} > 120nsec$, access time is determined by equation 4. This 40nsec interval (shown in the t_{RCD} inequality in equation 3) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$.

REFRESH CYCLES

Each of the 128 rows of the 2117 must be refreshed every 2 milliseconds to maintain data. Any memory cycle:

1. Read Cycle
2. Write Cycle (Early Write, Delayed Write or Read-Modify-Write)
3. $\overline{RAS}$-only Cycle

refreshes the selected row as defined by the low order ($\overline{RAS}$) addresses. Any Write cycle, of course, may change the state of the selected cell. Using a Read, Write, or Read-Modify-Write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the D_{OUT} in the high impedance state with a typical power reduction of 20% over a Read or Write cycle.

$\overline{RAS}/\overline{CAS}$ TIMING

$\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle can not begin until the minimum precharge time, t_{RP}, has been met.

DATA OUTPUT OPERATION

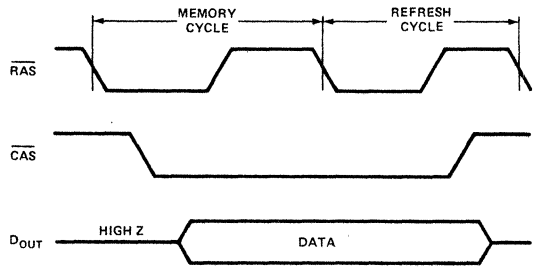
The 2117 Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}) the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

Intel 2117 Data Output Operation for Various Types of Cycles

Type of Cycle	D_{OUT} State
Read Cycle	Data From Addressed Memory Cell
Early Write Cycle	HI-Z
$\overline{RAS}$-Only Refresh Cycle	HI-Z
$\overline{CAS}$-Only Cycle	HI-Z
Read/Modify/Write Cycle	Data From Addressed Memory Cell
Delayed Write Cycle	Indeterminate

HIDDEN REFRESH

A feature of the 2117 is that refresh cycles may be performed while maintaining valid data at the output pin. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see Figure below).



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

POWER ON

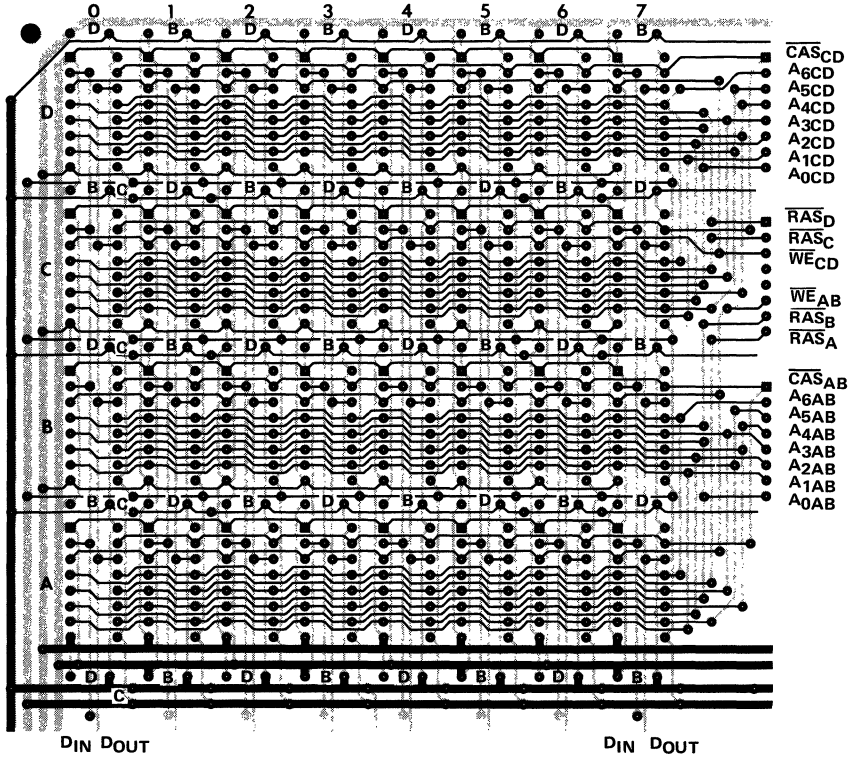
The 2117 requires no power on sequence providing absolute maximum ratings are not exceeded. After the application of supply voltages or after extended periods of bias (greater than 2 milliseconds) without clocks, the device must perform a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock, such as $\overline{RAS}$-Only refresh) prior to normal operation.

POWER SUPPLY DECOUPLING/DISTRIBUTION

It is recommended that a 0.1μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. A 0.1μF ceramic capacitor should also be connected between V_{BB} and V_{SS} at every other device (preferably the alternate devices to the V_{DD} decoupling). For each 16 devices, a 10μF tantalum or equivalent capacitor should be connected between V_{DD} and V_{SS} near the array. An equal or slightly smaller bulk capacitor is also recommended between V_{BB} and V_{SS} for every 32 devices.

The V_{CC} supply is connected only to the 2117 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is associated with the input high level current to a TTL gate and the output leakage currents of any OR-tied 2117's (typically 100μA or less total). Intel recommends that a 0.1 or 0.01μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight memory devices.

Due to the high frequency characteristics of the current waveforms, the inductance of the power supply distribution system on the array board should be minimized. It is recommended that the V_{DD}, V_{BB}, and V_{SS} supply lines be gridded both horizontally and vertically at each device in the array. This technique allows use of double sided circuit boards with noise performance equal to or better than multi-layered circuit boards.



DECOUPLING CAPACITORS
D = 0.1μF TO V_{DD} TO V_{SS}
B = 0.1μF V_{BB} TO V_{SS}
C = 0.01μF V_{CC} TO V_{SS}

SAMPLE P.C. BOARD LAYOUT EMPLOYING VERTICAL AND HORIZONTAL GRIDDING ON ALL POWER SUPPLIES.

BOARD ORGANIZATION: 64K WORDS BY 8-BITS.

64K BYTE STORAGE ARRAY LAYOUT

2118 FAMILY
16,384 x 1 BIT DYNAMIC RAM

	2118-2	2118-3	2118-4	2118-7
Maximum Access Time (ns)	80	100	120	150
Read, Write Cycle (ns)	200	235	270	320
Read-Modify-Write Cycle (ns)	250	295	345	410

- **Single +5V Supply, ±10% Tolerance**
- **HMOS Technology**
- **Low Power: 160mW Max. Operating**
  16mW Max. Standby
- **Low V_{DD} Current Transients**
- **All Inputs, Including Clocks, TTL Compatible**
- **Non-Latched Output is Three-State, TTL Compatible**
- **$\overline{RAS}$ Only Refresh**
- **128 Refresh Cycles Required Every 2ms**
- **Page Mode Capability**
- **$\overline{CAS}$ Controlled Output Allows Hidden Refresh**

The Intel® 2118 is a 16,384 word by 1-bit Dynamic MOS RAM designed to operate from a single +5V power supply. The 2118 is fabricated using HMOS — a production proven process for high performance, high reliability, and high storage density.

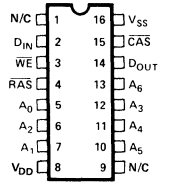
The 2118 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients contribute to the high noise immunity of the 2118 in a system environment.

Multiplexing the 14 address bits into the 7 address input pins allows the 2118 to be packaged in the industry standard 16-pin DIP. The two 7-bit address words are latched into the 2118 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical timing requirements for $\overline{RAS}$ and $\overline{CAS}$ allow use of the address multiplexing technique while maintaining high performance.

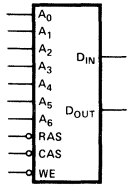
The 2118 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is latched on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The 2118 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain latched data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2ms period. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

PIN CONFIGURATION

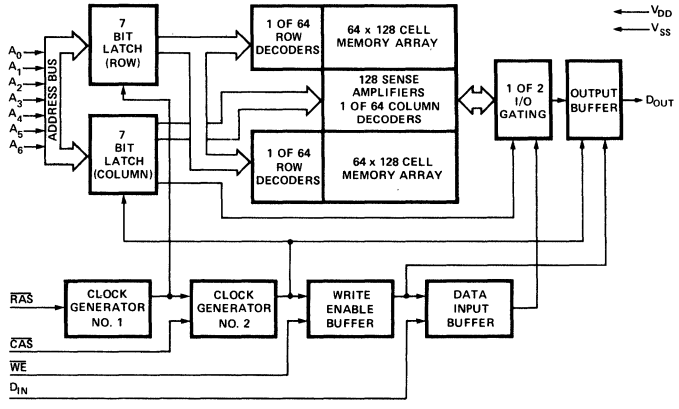


LOGIC SYMBOL



A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
$\overline{RAS}$	ROW ADDRESS STROBE
V_{DD}	POWER (+5V)
V_{SS}	GROUND

BLOCK DIAGRAM



2141
4096 X 1 BIT STATIC RAM

	2141-2	2141-3	2141-4	2141-5	2141L-3	2141L-4	2141L-5
Max. Access Time (ns)	120	150	200	250	150	200	250
Max. Active Current (mA)	70	70	55	55	40	40	40
Max. Standby Current (mA)	20	20	12	12	5	5	5

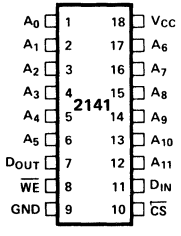
- **HMOS Technology**
- **Industry Standard 2147 Pinout**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Automatic Power-Down**
- **Directly TTL Compatible — All Inputs and Output**
- **Separate Data Input and Output**
- **Three-State Output**
- **High Density 18-Pin Package**

The Intel® 2141 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

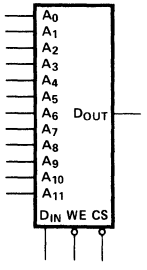
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the 2141 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are de-selected.

The 2141 is placed in an 18-pin package configured with the industry standard pinout, the same as the 2147. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

PIN CONFIGURATION



LOGIC SYMBOL



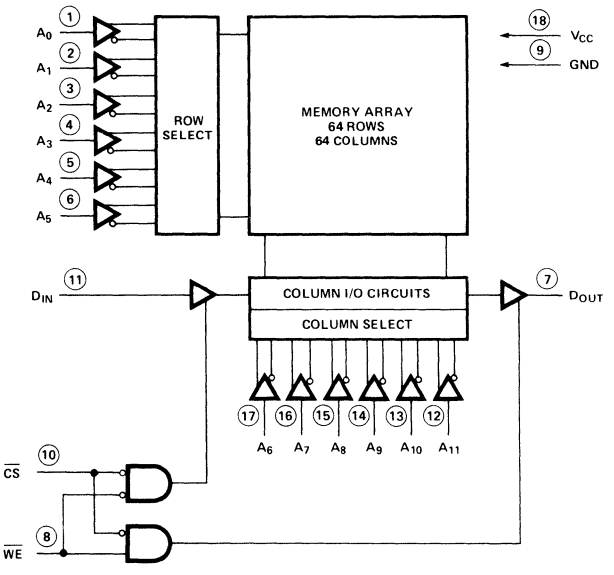
PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to 85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With
Respect to Ground ..... -1.5V to +7V
Power Dissipation 1.2W
D.C. Output Current 20mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±10% unless otherwise noted.

Symbol	Parameter	2141-2/-3 Min.	2141-2/-3 Typ.[1]	2141-2/-3 Max.	2141-4/-5 Min.	2141-4/-5 Typ.[1]	2141-4/-5 Max.	2141L-3/L-4/L-5 Min.	2141L-3/L-4/L-5 Typ.[1]	2141L-3/L-4/L-5 Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)		0.01	10		0.01	10		0.01	10	µA	V_{CC}=Max., V_{IN}= GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	10		0.1	10		0.1	10	µA	$\overline{CS}$=V_{IH}, V_{CC}=Max., V_{OUT}=GND to 4.5V
I_{CC}	Operating Current		45	70		40	55		30	40	mA	V_{CC}=Max., $\overline{CS}$=V_{IL}, Outputs Open
I_{SB}	Standby Current			20			12			5	mA	V_{CC}=Min. to Max., $\overline{CS}$=V_{IH}
I_{PO}[2]	Peak Power-On Current			40			30			18	mA	V_{CC}=GND to V_{CC} Min. $\overline{CS}$=Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	-1.0		0.8	-1.0		0.8	-1.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4	V	I_{OL} = 8.0mA
V_{OH}	Output High Voltage	2.4			2.4			2.4			V	I_{OH} = -4.0mA
I_{OS}[3]	Output Short Circuit Current	-120		120	-120		120	-120		120	mA	V_{OUT}=GND to V_{CC}

Notes: 1. Typical limits are at V_{CC} = 5V, T_A = +25°C, and specified loading.
2. I_{CC} exceeds I_{SB} maximum during power-on, as shown in Graph 7. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.
3. Duration not to exceed one minute.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.5 Volts
Input Rise and Fall Times	10 nsec
Input and Output Timing Reference Levels	1.5 Volts
Output Load	1 TTL Load plus 100pF

CAPACITANCE [4]

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0V

Note 4. This parameter is sampled and not 100% tested.

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V±10%, unless otherwise noted.

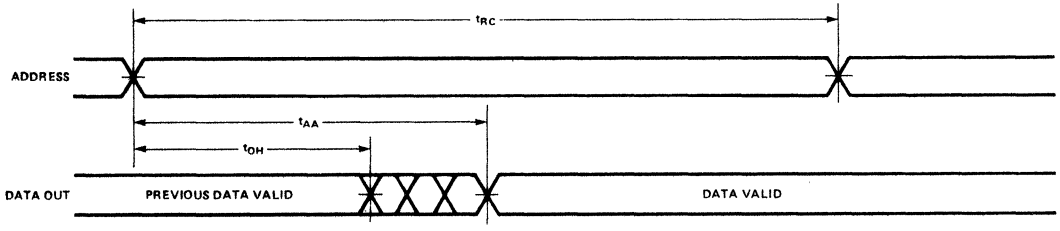
READ CYCLE

Symbol	Parameter	2141-2 Min.	2141-2 Max.	2141-3/L-3 Min.	2141-3/L-3 Max.	2141-4/L-4 Min.	2141-4/L-4 Max.	2141-5/L-5 Min.	2141-5/L-5 Max.	Unit
t_{RC}	Read Cycle Time	120		150		200		250		ns
t_{AA}	Address Access Time		120		150		200		250	ns
t_{ACS1}[1]	Chip Select Access Time		120		150		200		250	ns
t_{ACS2}[2]	Chip Select Access Time		130		160		200		250	ns
t_{OH}	Output Hold from Address Change	10		10		10		10		ns
t_{LZ}[3]	Chip Selection to Output in Low Z	30		30		30		30		ns
t_{HZ}[3]	Chip Deselection to Output in High Z	0	60	0	60	0	60	0	60	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		60		60		60		60	ns

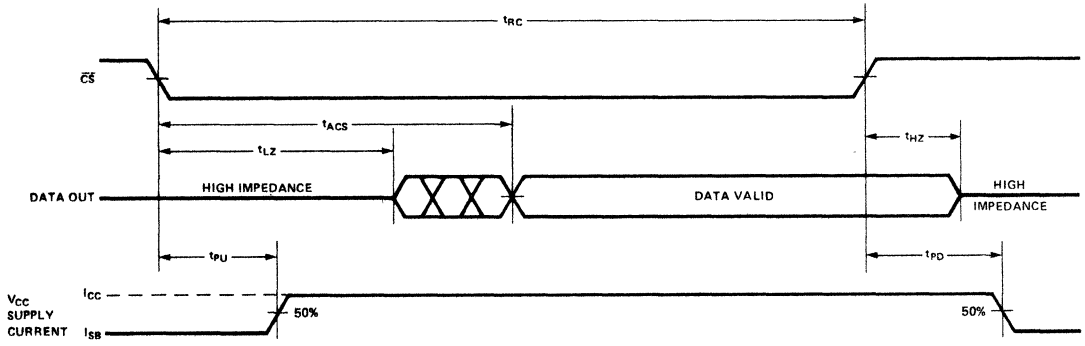
RAM

WAVEFORMS

READ CYCLE NO. 1 [4,5]



READ CYCLE NO. 2 [4,6]



Notes:

1. Chip deselected for greater than 55ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

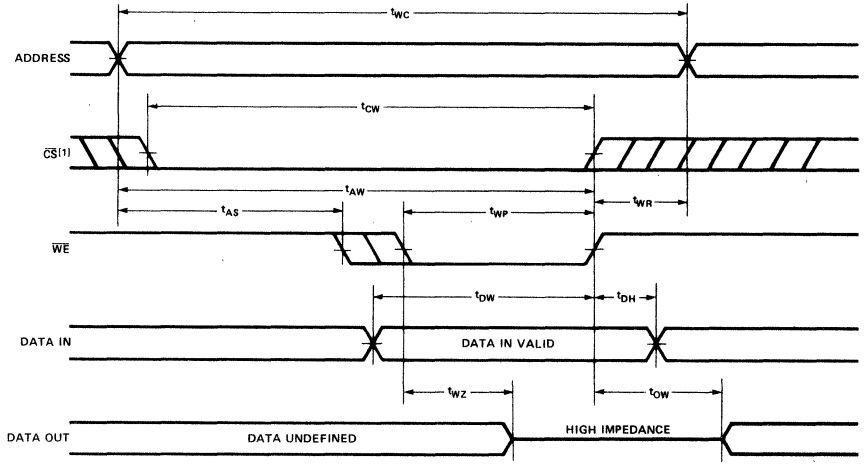
A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise noted.

WRITE CYCLE

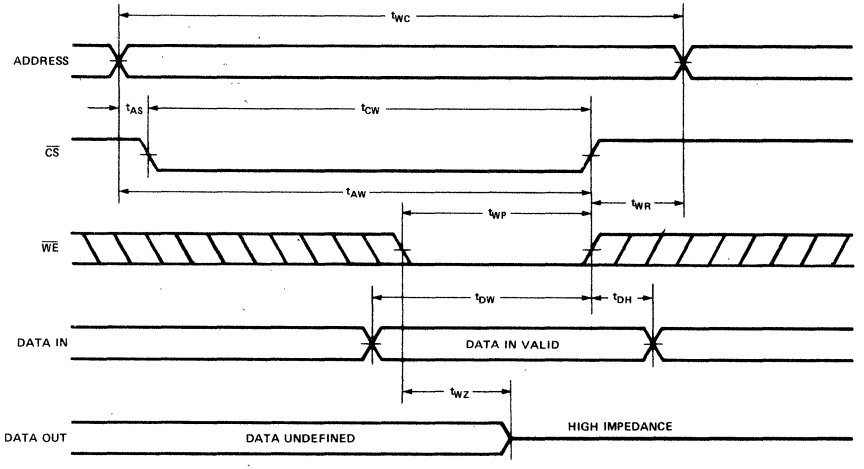
Symbol	Parameter	2141-2 Min.	2141-2 Max.	2141-3/L-3 Min.	2141-3/L-3 Max.	2141-4/L-4 Min.	2141-4/L-4 Max.	2141-5/L-5 Min.	2141-5/L-5 Max.	Unit
t_{WC}	Write Cycle Time	120		150		200		250		ns
t_{CW}	Chip Selection to End of Write	110		135		180		230		ns
t_{AW}	Address Valid to End of Write	110		135		180		230		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	60		60		60		75		ns
t_{WR}	Write Recovery Time	10		15		20		20		ns
t_{DW}	Data Valid to End of Write	50		60		60		75		ns
t_{DH}	Data Hold Time	5		5		5		5		ns
t_{WZ}	Write Enabled to Output in High Z	10	70	10	80	10	80	10	80	ns
t_{OW}	Output Active from End of Write	5		5		5		5		ns

WAVEFORMS

WRITE CYCLE #1 ($\overline{WE}$ CONTROLLED)



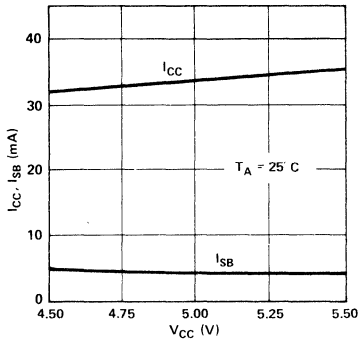
WRITE CYCLE #2 ($\overline{CS}$ CONTROLLED)



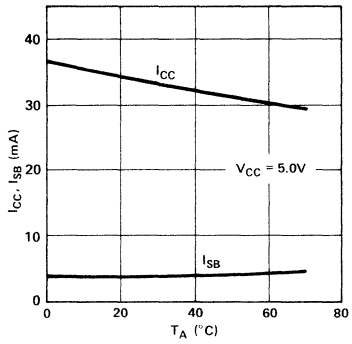
Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

TYPICAL D.C. AND A.C. CHARACTERISTICS

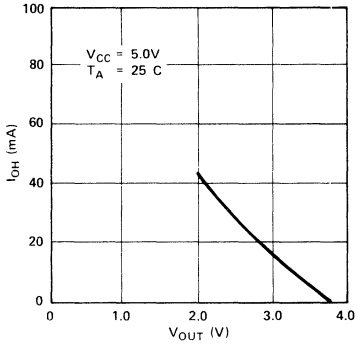
GRAPH 1
SUPPLY CURRENT VS.
SUPPLY VOLTAGE



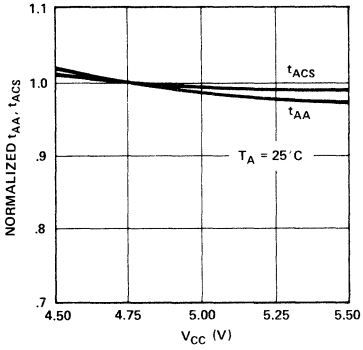
GRAPH 2
SUPPLY CURRENT VS.
AMBIENT TEMPERATURE



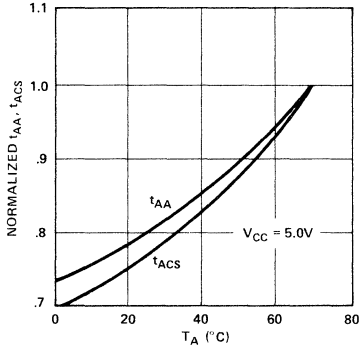
GRAPH 3
OUTPUT SOURCE CURRENT VS.
OUTPUT VOLTAGE



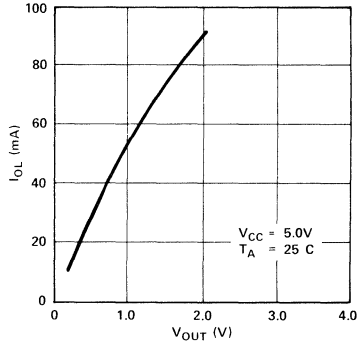
GRAPH 4
NORMALIZED ACCESS TIME
VS. SUPPLY VOLTAGE



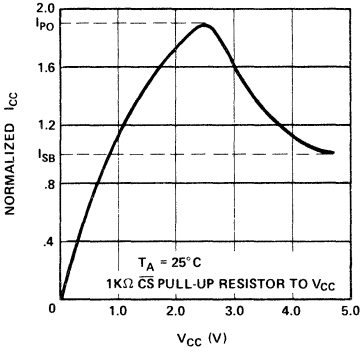
GRAPH 5
NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE



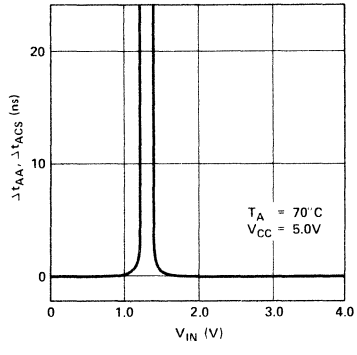
GRAPH 6
OUTPUT SINK CURRENT VS.
OUTPUT VOLTAGE



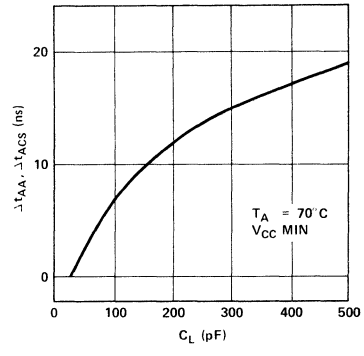
GRAPH 7
TYPICAL POWER-ON CURRENT
VS. POWER SUPPLY VOLTAGE



GRAPH 8
ACCESS TIME CHANGE VS.
INPUT VOLTAGE



GRAPH 9
ACCESS TIME CHANGE VS.
OUTPUT LOADING



DEVICE DESCRIPTION

The 2141 is produced with HMOS, a new high-performance MOS technology which incorporates on-chip substrate bias generation to achieve high-performance. This process, combined with new design ideas, gives the 2141 its unique features. Both low power and ease-of-use have been obtained in a single part. The low-power feature is controlled with the Chip Select input, which is not a clock and does not have to be cycled. Multiple read or write operations are possible during a single select period. Access times are equal to cycle times, resulting in data rates up to 8.3 MHz for the 2141-2. This is considerably higher performance than for clocked static designs.

Whenever the 2141 is deselected, it automatically reduces its power requirements to a fraction of the active power, as shown in Figure 1. This is achieved by switching off the power to unnecessary portions of the internal peripheral circuitry. This feature adds up to significant system power savings. The average power per device declines as system size grows because a continually higher portion of the memory is deselected. Device power dissipation asymptotically approaches the standby power level, as shown in Figure 2.

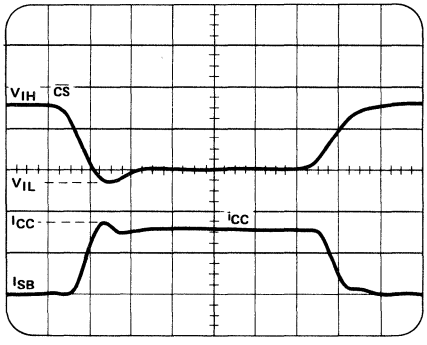


FIGURE 1. i_{CC} WAVEFORM.

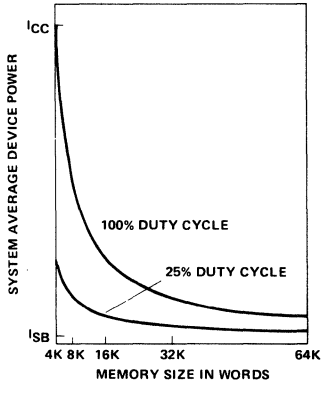


FIGURE 2. AVERAGE DEVICE DISSIPATION VS. MEMORY SIZE.

There is no functional constraint on the amount of time the 2141 is deselected. However, there is a relationship between deselect time and Chip Select access time. With no compensation, the automatic power switch would cause an increase in Chip Select access time, since some time is lost in repowering the device upon selection. A feature of the 2141 design is its ability to compensate for this loss. The amount of compensation is a function of deselect time, as shown in Figure 3. For short deselect times, Chip Select access time becomes slower than address access time, since full compensation typically requires 60ns. For longer deselect times, Chip Select access time actually becomes faster than address access time because the compensation more than offsets the time lost in powering up. The spec accounts for this characteristic by specifying two Chip Select access times, t_{ACS1} and t_{ACS2}.

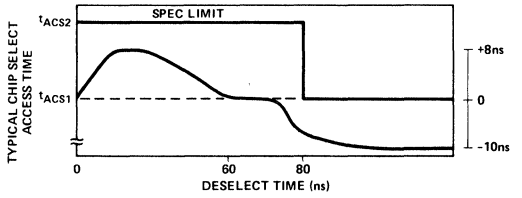


FIGURE 3. t_{ACS} VS. DESELECT TIME.

The power switching characteristic of the 2141 requires more careful decoupling than would be required of a constant power device. It is recommended that a 0.1μF ceramic capacitor be used on every other device, with a 22μF to 47μF bulk electrolytic decoupler every 32 devices. The actual values to be used will depend on board layout, trace widths and duty cycle. Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two-layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 4.

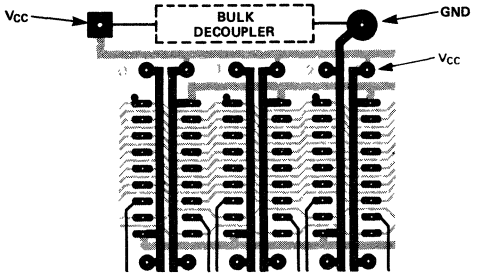


FIGURE 4. PC LAYOUT.

2142
1024 X 4 BIT STATIC RAM

	2142-2	2142-3	2142	2142L2	2142L3	2142L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Power Dissipation (mw)	525	525	525	370	370	370

- **High Density 20 Pin Package**
- **Access Time Selections From 200-450ns**
- **Identical Cycle and Access Times**
- **Low Operating Power Dissipation .1mW/Bit Typical**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**

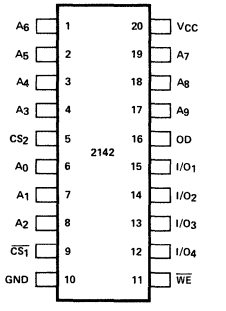
The Intel® 2142 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2142 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply.

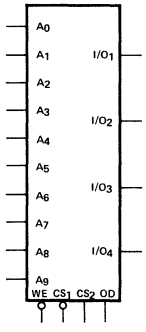
The 2142 is placed in a 20-pin package. Two Chip Selects ($\overline{CS}_1$ and CS_2) are provided for easy and flexible selection of individual packages when outputs are OR-tied. An Output Disable is included for direct control of the output buffers.

The 2142 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

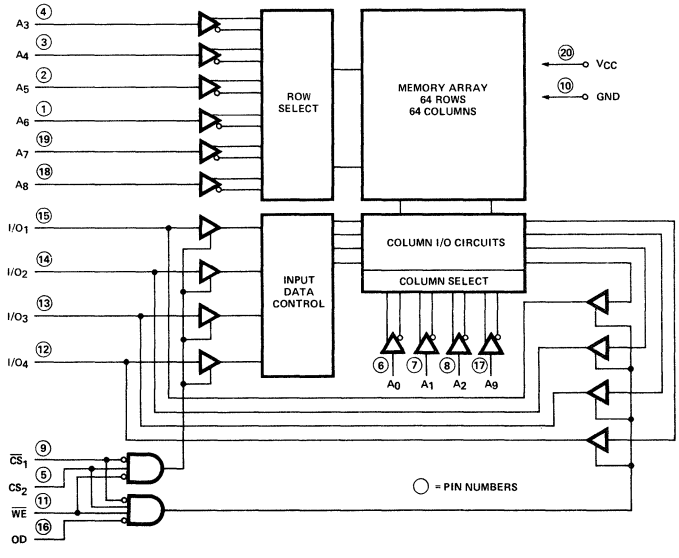
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}_1$, CS_2	CHIP SELECT	GND	GROUND
I/O_1–I/O_4	DATA INPUT/OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to 80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.0W
D.C. Output Current 10mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.

SYMBOL	PARAMETER	2142-2, 2142-3, 2142 Min.	Typ.[1]	Max.	2142L2, 2142L3, 2142L Min.	Typ.[1]	Max.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10			10	µA	V_{IN} = 0 to 5.25V
$\|I_{LO}\|$	I/O Leakage Current			10			10	µA	$\overline{CS}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		80	95			65	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current			100			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	6.0		2.1	6.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	-1.0	-1.4		-1.0	-1.4		mA	V_{OH} = 2.4V
I_{OS}[2]	Output Short Circuit Current			40			40	mA	$V_{I/O}$ = GND to V_{CC}

NOTE: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 30 seconds.

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = OV
C_{IN}	Input Capacitance	5	pF	V_{IN} = OV

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels ..... 0.8 Volt to 2.4 Volt
Input Rise and Fall Times ..... 10 nsec
Input and Output Timing Levels ..... 1.5 Volts
Output Load ..... 1 TTL Gate and C_L = 100 pF

TEST NOTE: This circuit employs a self starting oscillator and a charge pump which require a certain amount of time after POWER ON to start functioning properly. This 2142 circuit is conservatively specified as requiring 500 µsec after V_{CC} reaches its specified limit (4.75V).

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	2142-2, 2142L2 Min.	2142-2, 2142L2 Max.	2142-3, 2142L3 Min.	2142-3, 2142L3 Max.	2142, 2142L Min.	2142, 2142L Max.	UNIT
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{OD}	Output Enable to Output Valid		70		100		120	ns
t_{ODX}	Output Enable to Output Active	20		20		20		ns
t_{CO}	Chip Selection to Output Valid		70		100		120	ns
t_{CX}	Chip Selection to Output Active	20		20		20		ns
t_{OTD}	Output 3-state from Disable		60		80		100	ns
t_{OHA}	Output Hold from Address Change	50		50		50		ns

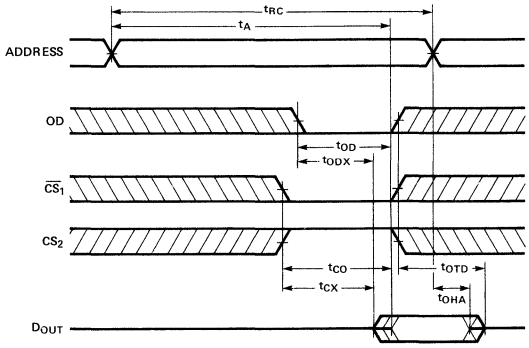
WRITE CYCLE [2]

SYMBOL	PARAMETER	2142-2, 2142L2 Min.	2142-2, 2142L2 Max.	2142-3, 2142L3 Min.	2142-3, 2142L3 Max.	2142, 2142L Min.	2142, 2142L Max.	UNIT
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTD}	Output 3-state from Disable		60		80		100	ns
t_{DW}	Data to Write Time Overlap	120		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

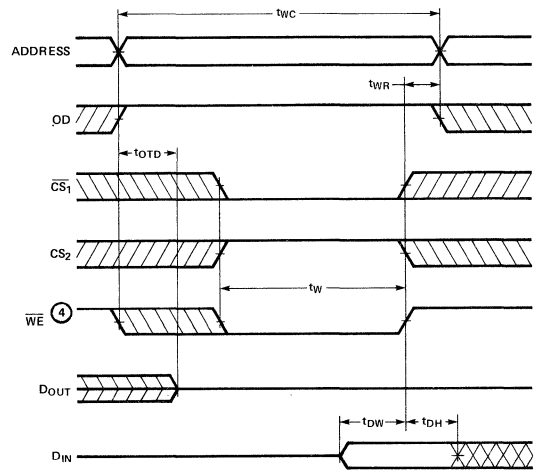
WAVEFORMS

READ CYCLE ③



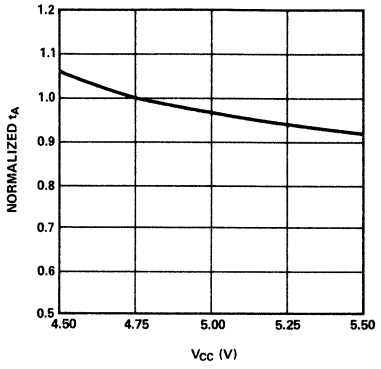
NOTES:
③ $\overline{WE}$ is high for a Read Cycle.
④ $\overline{WE}$ must be high during all address transitions.

WRITE CYCLE

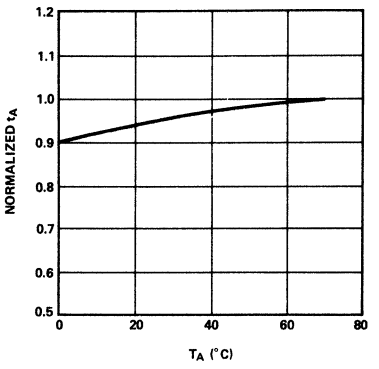


TYPICAL D.C. AND A.C. CHARACTERISTICS

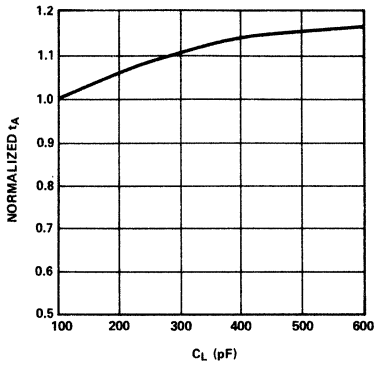
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



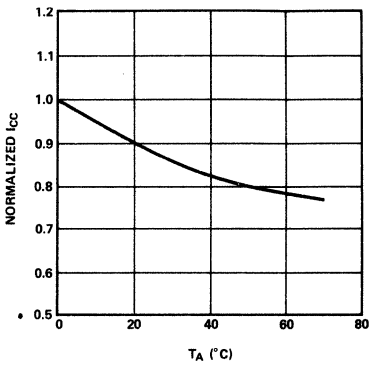
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



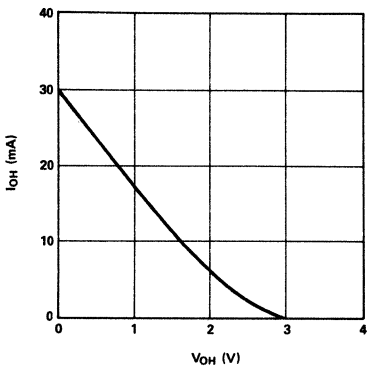
NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



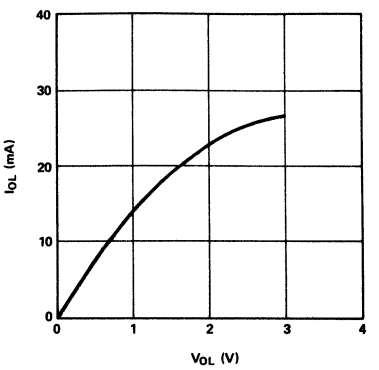
NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



2147
4096 X 1 BIT STATIC RAM

	2147-3	2147	2147L
Max. Access Time (ns)	55	70	70
Max. Active Current (mA)	180	160	140
Max. Standby Current (mA)	30	20	10

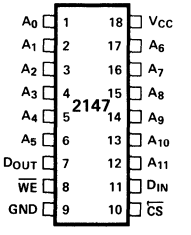
- **HMOS Technology**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Automatic Power-Down**
- **High Density 18-Pin Package**
- **Directly TTL Compatible — All Inputs and Output**
- **Separate Data Input and Output**
- **Three-State Output**

The Intel® 2147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

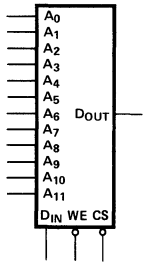
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the 2147 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are de-selected.

The 2147 is placed in an 18-pin package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

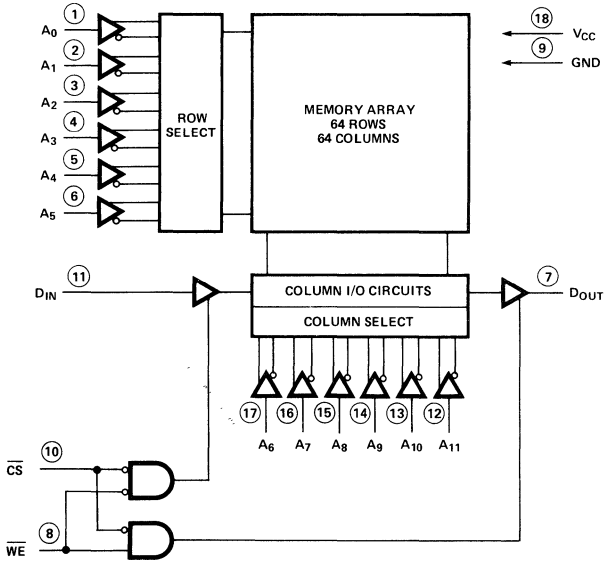
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-10°C to 85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-1.5V to +7V
Power Dissipation	1.2W
D.C. Output Current	20mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS [1]

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, unless otherwise noted.

Symbol	Parameter	2147-3 Min.	2147-3 Typ. [2]	2147-3 Max.	2147 Min.	2147 Typ. [2]	2147 Max.	2147L Min.	2147L Typ. [2]	2147L Max.	Unit	Test Conditions
I_{LI}	Input Load Current (All Input Pins)		0.01	10		0.01	10		0.01	10	µA	V_{CC}=MAX, V_{IN}=GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	50		0.1	50		0.1	50	µA	$\overline{CS}$=V_{IH}, V_{CC}=Max., V_{OUT}=GND to 4.5V
I_{CC}	Operating Current		120	170		100	150		100	135	mA	T_A=25°C; V_{CC}=Max., $\overline{CS}$=V_{IL}, Outputs Open
				180			160			140	mA	T_A=0°C; V_{CC}=Max., $\overline{CS}$=V_{IL}, Outputs Open
I_{SB}	Standby Current		18	30		12	20		7	10	mA	V_{CC}=Min. to Max. $\overline{CS}$=V_{IH}
I_{PO} [3]	Peak Power-On Current		35	70		25	50		15	30	mA	V_{CC}=GND to V_{CC} Min., $\overline{CS}$=Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	-1.0		0.8	-1.0		0.8	-1.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4			2.4			2.4			V	I_{OH} = -4.0mA
I_{OS} [4]	Output Short Circuit Current	-120		120	-120		120	-120		120	mA	V_{OUT}=GND to V_{CC}

Notes:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and specified loading.
3. I_{CC} exceeds I_{SB} maximum during power on, as shown in Graph 7. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.
4. Duration not to exceed one minute.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.5 Volts
Input Rise and Fall Times	10 nsec
Input and Output Timing Reference Levels	1.5 Volts
Output Load	See Figure 1

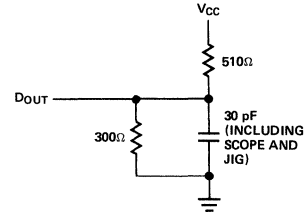


Figure 1. Output Load

CAPACITANCE [5]

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0V

Note 5. This parameter is sampled and not 100% tested.

A.C. CHARACTERISTICS

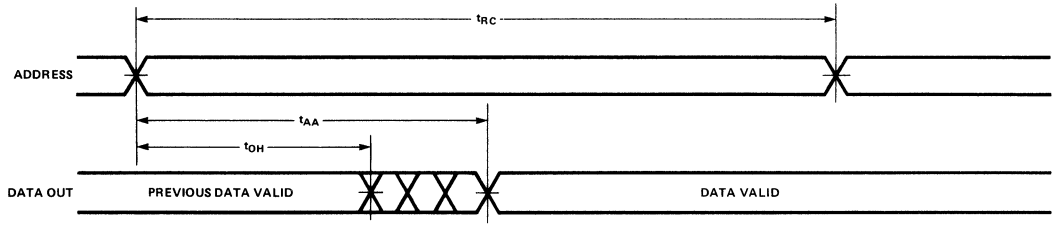
T_A = 0°C to 70°C, V_{CC} = +5V±10%, unless otherwise noted.

READ CYCLE

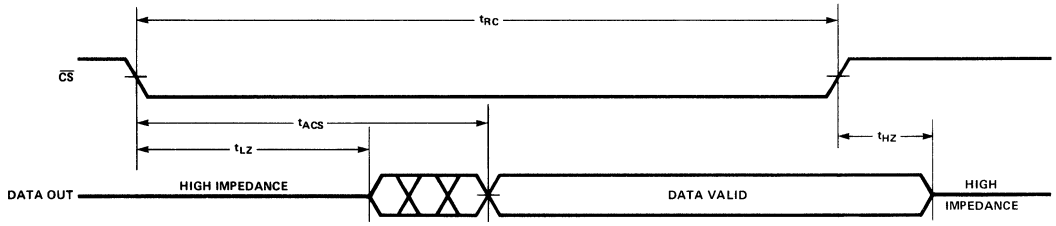
Symbol	Parameter	2147-3 Min.	2147-3 Max.	2147, 2147L Min.	2147, 2147L Max.	Unit	Test Conditions
t_{RC}	Read Cycle Time	55		70		ns	
t_{AA}	Address Access Time		55		70	ns	
t_{ACS1}	Chip Select Access Time		55		70	ns	Note 1
t_{ACS2}	Chip Select Access Time		65		80	ns	Note 2
t_{OH}	Output Hold from Address Change	5		5		ns	
t_{LZ} [3]	Chip Selection to Output in Low Z	10		10		ns	
t_{HZ} [3]	Chip Deselection to Output in High Z	0	40	0	40	ns	
t_{PU}	Chip Selection to Power Up Time	0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		30	ns	

WAVEFORMS

READ CYCLE NO. 1



READ CYCLE NO. 2



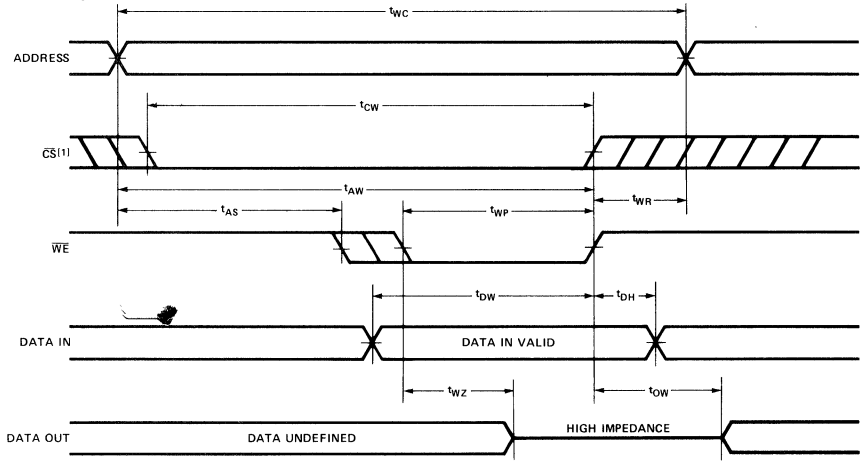
A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

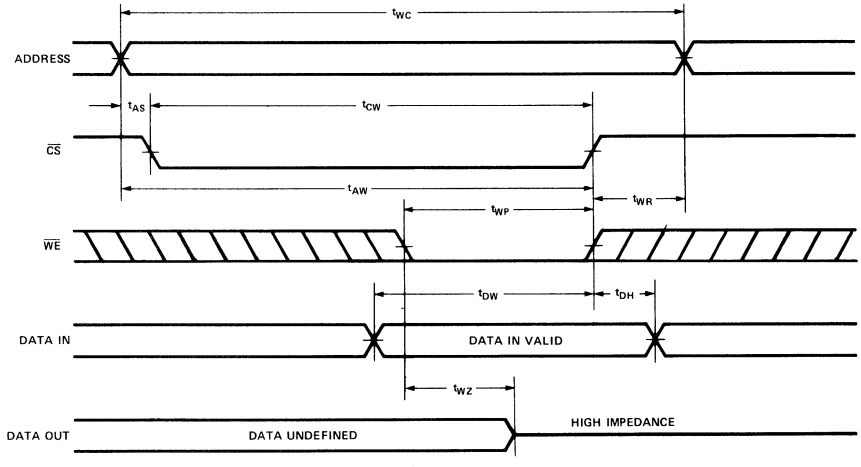
Symbol	Parameter	2147-3 Min.	2147-3 Max.	2147,2147L Min.	2147,2147L Max.	Unit	Test Conditions
t_{WC}	Write Cycle Time	55		70		ns	
t_{CW}	Chip Selection to End of Write	45		55		ns	
t_{AW}	Address Valid to End of Write	45		55		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{WP}	Write Pulse Width	35		40		ns	
t_{WR}	Write Recovery Time	10		15		ns	
t_{DW}	Data Valid to End of Write	25		30		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{WZ}	Write Enabled to Output in High Z	0	30	0	35	ns	
t_{OW}	Output Active from End of Write	0		0		ns	

WAVEFORMS

WRITE CYCLE #1 ($\overline{WE}$ CONTROLLED)



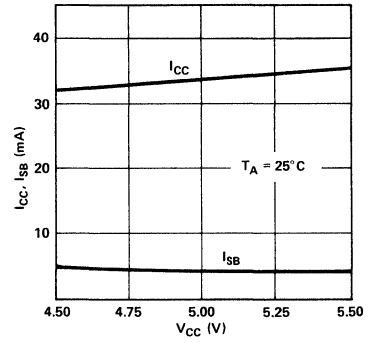
WRITE CYCLE #2 ($\overline{CS}$ CONTROLLED)



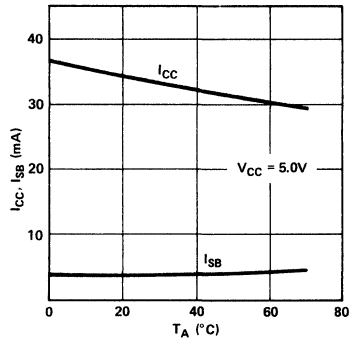
Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

TYPICAL D.C. AND A.C. CHARACTERISTICS

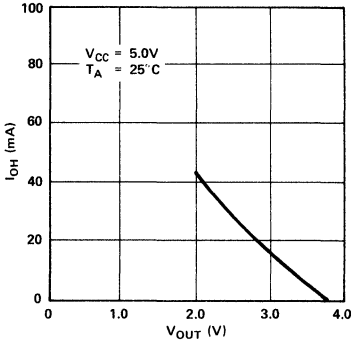
GRAPH 1
SUPPLY CURRENT VS.
SUPPLY VOLTAGE



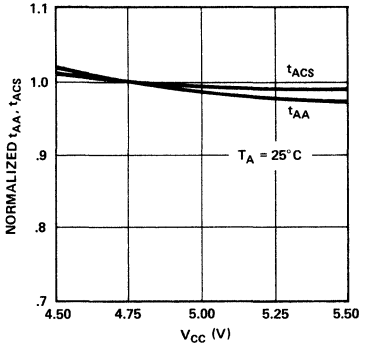
GRAPH 2
SUPPLY CURRENT VS.
AMBIENT TEMPERATURE



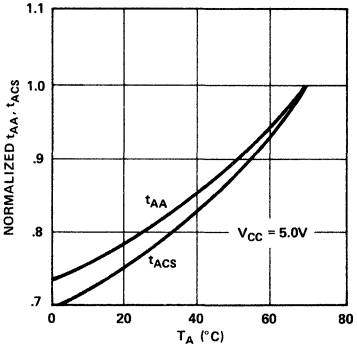
GRAPH 3
OUTPUT SOURCE CURRENT VS.
OUTPUT VOLTAGE



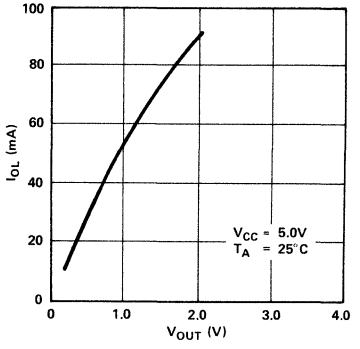
GRAPH 4
NORMALIZED ACCESS TIME
VS. SUPPLY VOLTAGE



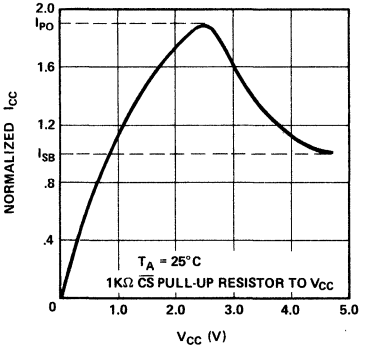
GRAPH 5
NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE



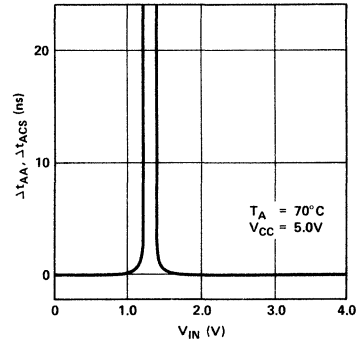
GRAPH 6
OUTPUT SINK CURRENT VS.
OUTPUT VOLTAGE



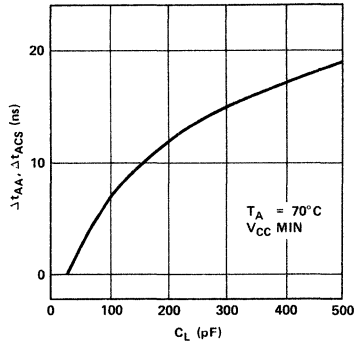
GRAPH 7
TYPICAL POWER-ON CURRENT
VS. POWER SUPPLY VOLTAGE



GRAPH 8
ACCESS TIME CHANGE VS.
INPUT VOLTAGE



GRAPH 9
ACCESS TIME CHANGE VS.
OUTPUT LOADING



Note 1. The supply current curves shown in Graphs 1 and 2 are for the 2147.
The supply current curves for the 2147L and 2147-3 can be calculated by scaling proportionately.

DEVICE DESCRIPTION

The 2147 is produced with HMOS, a new high-performance MOS technology which incorporates on-chip substrate bias generation combined with device scaling to achieve high-performance. The speed-power product of this process has been measured at 1pj, approximately four times better than previous MOS processes.

This process, combined with new design ideas, gives the 2147 its unique features. High speed, low power and ease-of-use have been obtained in a single part. The low-power feature is controlled with the Chip Select input, which is not a clock and does not have to be cycled. Multiple read or write operations are possible during a single select period. Access times are equal to cycle times, resulting in data rates of 14.3 MHz and 18 MHz for the 2147 and 2147-3, respectively. This is considerably higher performance than for clocked static designs.

Whenever the 2147 is deselected, it automatically reduces its power requirements to a fraction of the active power, as shown in Figure 1. This is achieved by switching off the power to unnecessary portions of the internal peripheral circuitry. This feature adds up to significant system power savings. The average power per device declines as system size grows because a continually higher portion of the memory is deselected. Device power dissipation asymptotically approaches the standby power level, as shown in Figure 2.

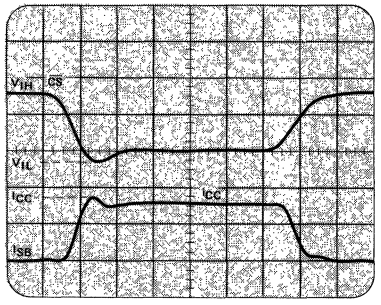


FIGURE 1. i_{CC} WAVEFORM.

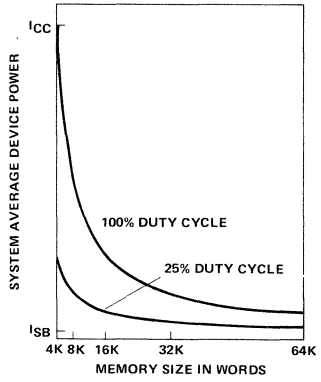


FIGURE 2. AVERAGE DEVICE DISSIPATION VS. MEMORY SIZE.

There is no functional constraint on the amount of time the 2147 is deselected. However, there is a relationship between deselect time and Chip Select access time. With no compensation, the automatic power switch would cause an increase in Chip Select access time, since some time is lost in repowering the device upon selection. A feature of the 2147 design is its ability to compensate for this loss. The amount of compensation is a function of deselect time, as shown in Figure 3. For short deselect times, Chip Select access time becomes slower than address access time, since full compensation typically requires 40ns. For longer deselect times, Chip Select access time actually becomes faster than address access time because the compensation more than offsets the time lost in powering up. The spec accounts for this characteristic by specifying two Chip Select access times, t_{ACS1} and t_{ACS2}.

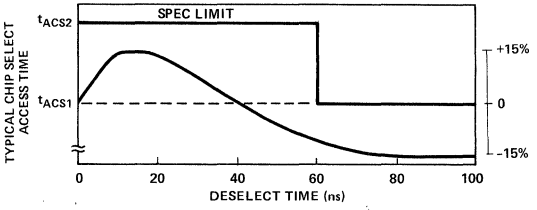


FIGURE 3. t_{ACS} VS. DESELECT TIME.

The power switching characteristic of the 2147 requires more careful decoupling than would be required of a constant power device. It is recommended that a 0.1μF to 0.3μF ceramic capacitor be used on every other device, with a 22μF to 47μF bulk electrolytic decoupler every 16 devices. The actual values to be used will depend on board layout, trace widths and duty cycle. Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two-layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 4.

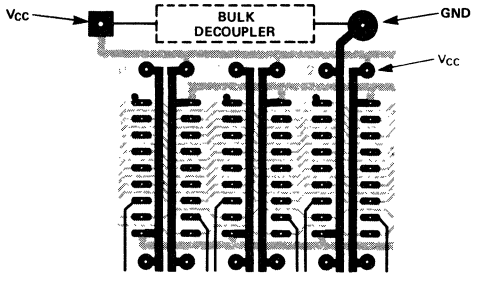


FIGURE 4. PC LAYOUT.

Terminations are recommended on input signal lines to the 2147 devices. In high speed systems, fast drivers can cause significant reflections when driving the high impedance inputs of the 2147. Terminations may be required to match the impedance of the line to the driver. The type of termination used depends on designer preference and may be parallel resistive or resistive-capacitive. The latter reduces terminator power dissipation.

2147H
HIGH SPEED 4096 x 1 BIT STATIC RAM

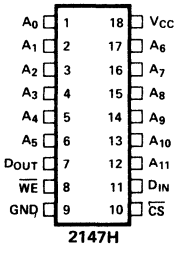
- **HMOS II Technology**
- **35-45ns Maximum Access Time**
- **180mA Maximum I_{CC}**
- **30mA Maximum I_{SB}**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Fully Compatible with Industry Standard 2147**
- **Automatic Power-Down**
- **High Density 18-Pin Package**
- **Directly TTL Compatible — All Inputs and Output**
- **Separate Data Input and Output**
- **Three-State Output**

The Intel® 2147H is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS II, Intel's new high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

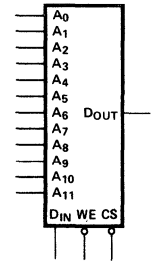
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the 2147H — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The 2147H is placed in an 18-pin package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

PIN CONFIGURATION



LOGIC SYMBOL



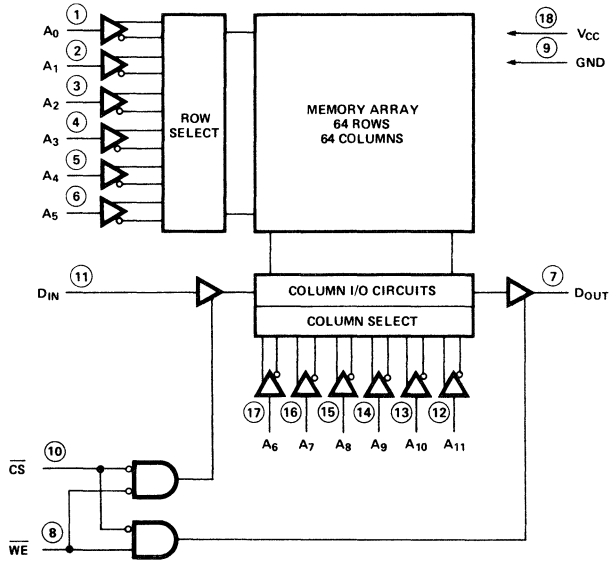
PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

BLOCK DIAGRAM



2148
1024 x 4 BIT STATIC RAM

Max. Access Time (ns)	60
Max. Active Current (mA)	150
Max. Standby Current (mA)	30

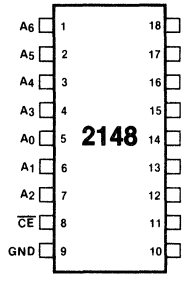
- **HMOS Technology**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Automatic Power-Down**
- **High Density 18-Pin Package**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Common Data Input and Output**
- **Three-State Output**

The Intel® 2148 is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

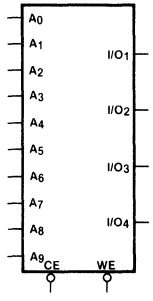
CE controls the power-down feature. In less than a cycle time after CE goes high — deselecting the 2148 — the part automatically reduces its power requirements and remains in this low power standby mode as long as CE remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The 2148 is placed in an 18-pin package configured with the industry standard 1K x 4 pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. Common input and output pins are provided.

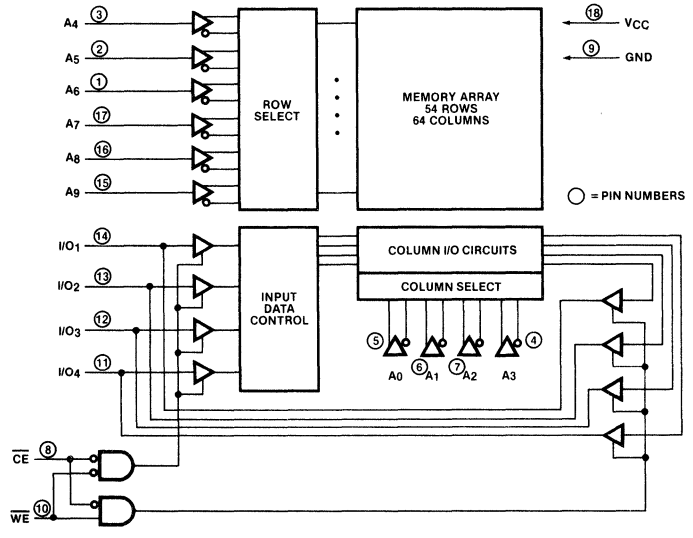
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CE}$	CHIP ENABLE
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)
GND	GROUND

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT ENABLED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

3101, 3101A
16 x 4 BIT HIGH SPEED RAM

- **Fast Access Time — 35 nsec max over 0-75°C Temperature Range (3101A)**
- **Simple Memory Expansion through Chip Select Input — 17 nsec max over 0-75°C Temperature Range (3101A)**
- **DTL and TTL Compatible — Low Input Load Current: 0.25 mA max**
- **OR-Tie Capability — Open Collector Outputs**
- **Fully Decoded — on Chip Address Decode and Buffer**
- **Minimum Line Reflection — Low Voltage Diode Input Clamp**
- **Ceramic and Plastic Package — 16 Pin Dual In-]Line Configuration**

The Intel 3101 and 3101A are high speed fully decoded 64 bit random access memories, organized 16 words by 4 bits. Their high speed makes them ideal in scratch pad applications. An unselected chip will not generate noise at its output during writing of a selected chip. The output is held high on an unselected chip regardless of the state of the read/write signal.

The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices with gold diffusion processes.

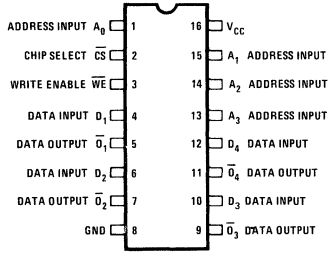
The Intel 3101 and 3101A are packaged in either hermetically sealed 16 pin ceramic packages, or in low cost silicone packages, and their performance is specified over a temperature range from 0°C to 75°C.

The storage cells are addressed through an on chip 1 of 16 binary decoder using four input address leads.

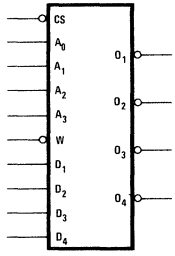
A separate Chip Select lead allows easy selection of an individual package when outputs are OR-tied.

In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.

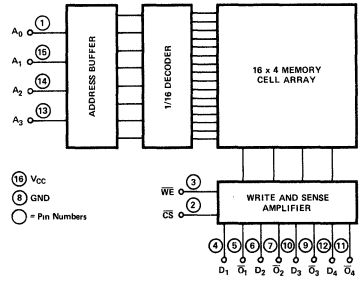
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

D_1–D_4	DATA INPUTS	$\overline{CS}$	CHIP SELECT INPUT
A_0–A_3	ADDRESS INPUTS	$\overline{O}_1$–$\overline{O}_4$	DATA OUTPUTS
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)

TRUTH TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
LOW	LOW	WRITE	HIGH
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
HIGH	LOW	–	HIGH
HIGH	HIGH	–	HIGH

Absolute Maximum Ratings*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		100 mA

*COMMENT:

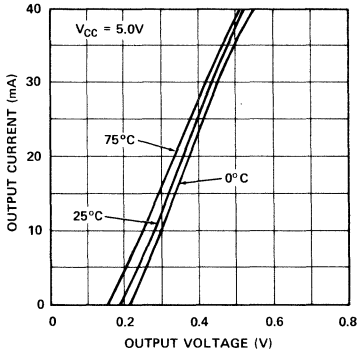
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

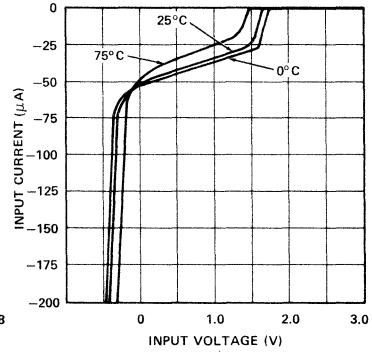
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{FA}	ADDRESS INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_A =0.45V
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_D =0.45V
I_{FW}	WRITE INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_W =0.45V
I_{FS}	CHIP SELECT INPUT LOAD CURRENT		−0.25	mA	V_{CC} =5.25V, V_S =0.45V
I_{RA}	ADDRESS INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_A =5.25V
I_{RD}	DATA INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_D =5.25V
I_{RW}	WRITE INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_W =5.25V
I_{RS}	CHIP SELECT INPUT LEAKAGE CURRENT		10	μA	V_{CC} =5.25V, V_S =5.25V
V_{CA}	ADDRESS INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_A =−5.0 mA
V_{CD}	DATA INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_D =−5.0 mA
V_{CW}	WRITE INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_W =−5.0 mA
V_{CS}	CHIP SELECT INPUT CLAMP VOLTAGE		−1.0	V	V_{CC} =4.75V, I_S =−5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} =4.75V, I_{OL} = 15 mA Memory Stores "Low"
I_{CEX}	OUTPUT LEAKAGE CURRENT		100	μA	V_{CC} =5.25V, V_{CEX} =5.25V V_S =2.5V
I_{CC}	POWER SUPPLY CURRENT		105	mA	V_{CC} =5.25V, V_A =V_S =V_D =0V
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} =5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} =5.0V

Typical Characteristics

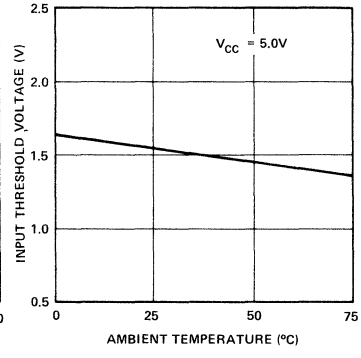
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



INPUT CURRENT VS. INPUT VOLTAGE



INPUT THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE



Switching Characteristics

Conditions of Test:

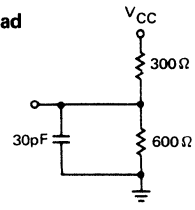
Input Pulse amplitudes: 2.5V

Input Pulse rise and fall times of 5 nanoseconds between 1 volt and 2 volts

Speed measurements are made at 1.5 volt levels

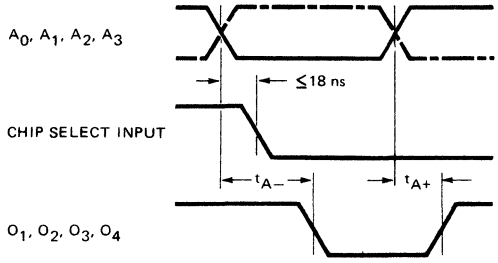
Output loading is 15mA and 30 pF

15 mA Test Load

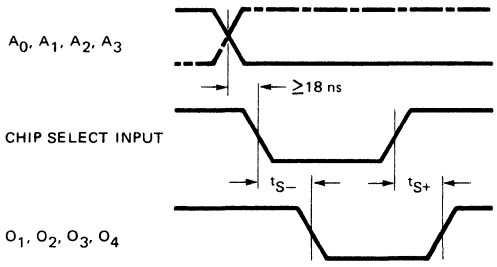


READ CYCLE

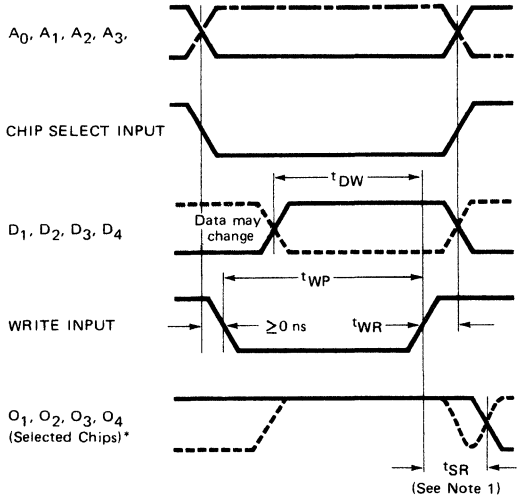
Address to Output Delay



Chip Select to Output Delay



WRITE CYCLE



*Outputs of unselected chips remain high during write cycle.

NOTE 1: t_{SR} is associated with a read cycle following a write cycle and does not affect the access time.

A.C. Characteristics T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

READ CYCLE					
SYMBOL	PARAMETER	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{S+}, t_{S-}	Chip Select to Output Delay	5	17	5	42
t_{A-}, t_{A+}	Address to Output Delay	10	35	10	60

WRITE CYCLE					
SYMBOL	TEST	3101A LIMITS (ns)		3101 LIMITS (ns)	
		MIN.	MAX.	MIN.	MAX.
t_{SR}	Sense Amplifier Recovery Time		35		50
t_{WP}	Write Pulse Width	25		40	
t_{DW}	Data-Write Overlap Time	25		40	
t_{WR}	Write Recovery Time	0		5	

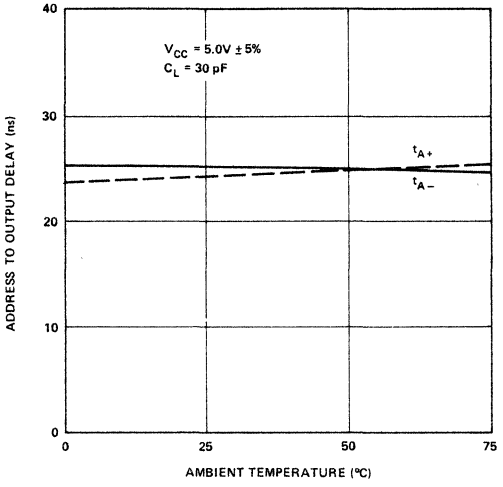
NOTE 2: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{bias} = 2V, V_{CC} = 0V, and T_A = 25°C.

CAPACITANCE[2] T_A = 25° C

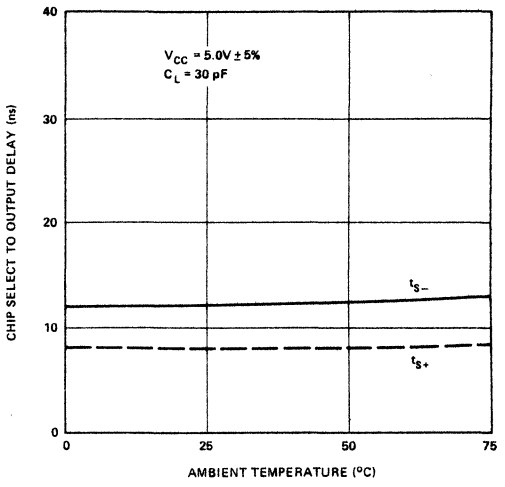
C_{IN}	INPUT CAPACITANCE (All Pins)	10 pF maximum
C_{OUT}	OUTPUT CAPACITANCE	12 pF maximum

Typical A.C. Characteristics

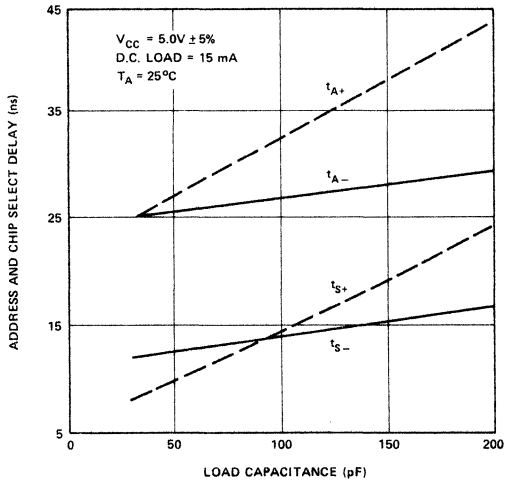
ADDRESS TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



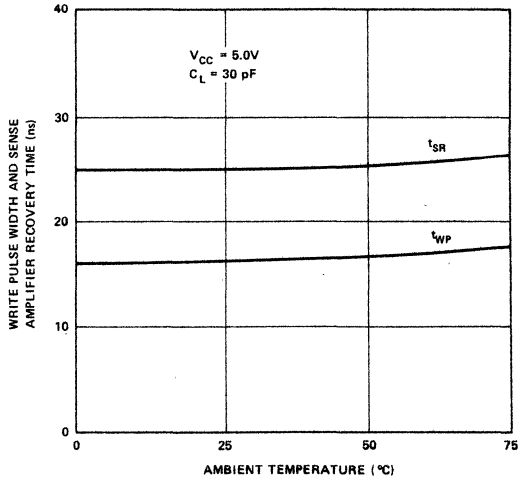
CHIP SELECT TO OUTPUT DELAY
VS.
AMBIENT TEMPERATURE



ADDRESS & CHIP SELECT TO OUTPUT DELAY
VS.
LOAD CAPACITANCE



WRITE PULSE WIDTH & SENSE
AMPLIFIER RECOVERY TIME
VS. AMBIENT TEMPERATURE



5101 FAMILY
256 x 4 BIT STATIC CMOS RAM

P/N	Typ. Current @ 2V (μA)	Typ. Current @ 5V (μA)	Max Access (ns)
5101L	0.14	0.2	650
5101L-1	0.14	0.2	450
5101L-3	0.70	1.0	650

- **Single +5V Power Supply**
- **Ideal for Battery Operation (5101L)**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Three-State Output**

The Intel® 5101 is an ultra-low power 1024-bit (256 words X 4 bits) static RAM fabricated with an advanced ion-implanted silicon gate CMOS technology. The device has two chip enable inputs. Minimum standby current is drawn by this device when CE2 is at a low level. When deselected the 5101 draws from the single 5-volt supply only 10 microamps. This device is ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

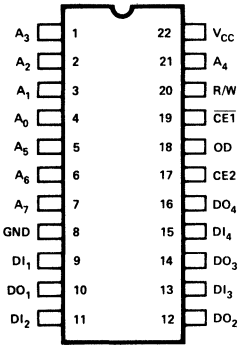
The 5101 uses fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 has separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

The 5101L has the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.

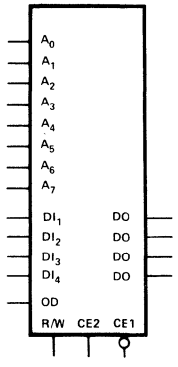
A pin compatible N-channel static RAM, the Intel® 2101A, is also available for low cost applications where a 256 X 4 organization is needed.

The Intel ion-implanted, silicon gate, Complementary MOS (CMOS) process allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION



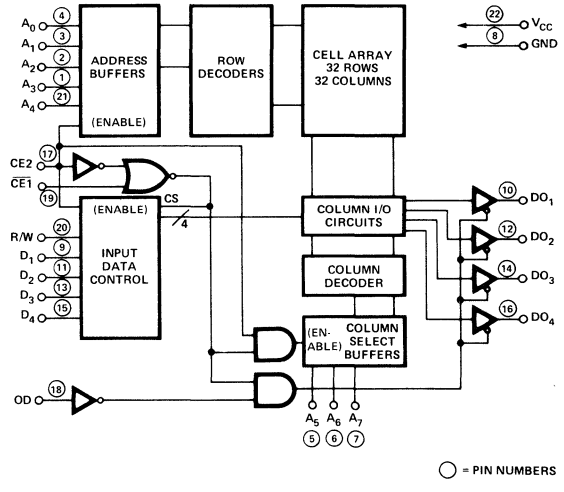
LOGIC SYMBOL



TRUTH TABLE

$\overline{CE_1}$	CE_2	OD	R/W	D_{IN}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{IN}	Write
L	H	L	H	X	D_{OUT}	Read

BLOCK DIAGRAM



Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . -0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	5101L and 5101L-1 Limits Min.	Typ.[1]	Max.	5101L-3 Limits Min.	Typ.[1]	Max.	Units	Test Conditions
I_{L2}[2]	Input Current		5			5		nA	
$\|I_{LO}\|$[2]	Output Leakage Current			1			1	µA	$\overline{CE1}$=2.2V, V_{OUT}= 0 to V_{CC}
I_{CC1}	Operating Current		9	22		9	22	mA	V_{IN}=V_{CC}, Except $\overline{CE1} \leq$ 0.65V, Outputs Open
I_{CC2}	Operating Current		13	27		13	27	mA	V_{IN}=2.2V, Except $\overline{CE1} \leq$ 0.65V, Outputs Open
I_{CCL}[2]	Standby Current			10			200	µA	CE2 ≤ 0.2V, T_A= 70° C
V_{IL}	Input Low Voltage	-0.3		0.65	-0.3		0.65	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL}=2.0 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH}= -1.0 mA

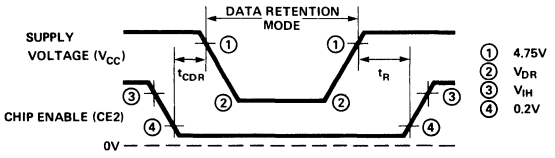
Low V_{CC} Data Retention Characteristics (For 5101L, 5101L-1 and 5101L-3) T_A = 0° C to 70° C

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	CE2 ≤ 0.2V	
I_{CCDR1}	5101L or 5101L-1 Data Retention Current		0.14	10	µA		V_{DR}=2.0V, T_A=70° C
I_{CCDR2}	5101L-3 Data Retention Current		0.70	200	µA		V_{DR}=2.0V, T_A=70° C
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[3]			ns		

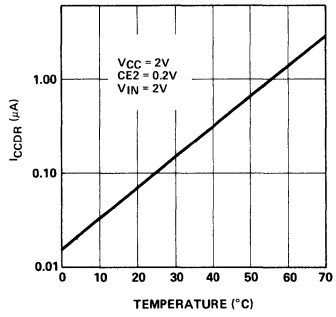
NOTES:

1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL} measurement.
3. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Typical I_{CCDR} Vs. Temperature



RAM

A.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

READ CYCLE

Symbol	Parameter	5101L-1 Limits (ns) Min.	5101L-1 Limits (ns) Max.	5101L and 5101L-3 Limits (ns) Min.	5101L and 5101L-3 Limits (ns) Max.
t_{RC}	Read Cycle	450		650	
t_A	Access Time		450		650
t_{CO1}	Chip Enable ($\overline{CE}$ 1) to Output		400		600
t_{CO2}	Chip Enable (CE 2) to Output		500		700
t_{OD}	Output Disable to Output		250		350
t_{DF}	Data Output to High Z State	0	130	0	150
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0		0	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0	

WRITE CYCLE

t_{WC}	Write Cycle	450		650	
t_{AW}	Write Delay	130		150	
t_{CW1}	Chip Enable ($\overline{CE}$ 1) to Write	350		550	
t_{CW2}	Chip Enable (CE 2) to Write	350		550	
t_{DW}	Data Setup	250		400	
t_{DH}	Data Hold	50		100	
t_{WP}	Write Pulse	250		400	
t_{WR}	Write Recovery	50		50	
t_{DS}	Output Disable Setup	130		150	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and C_L = 100pF

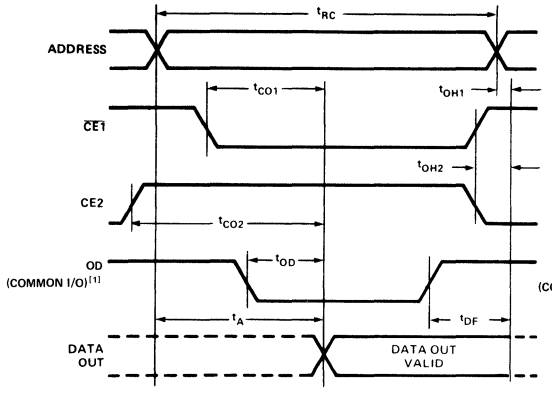
Capacitance[2] T_A = 25°C, f = 1MHz

Symbol	Test	Limits (pF) Typ.	Limits (pF) Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

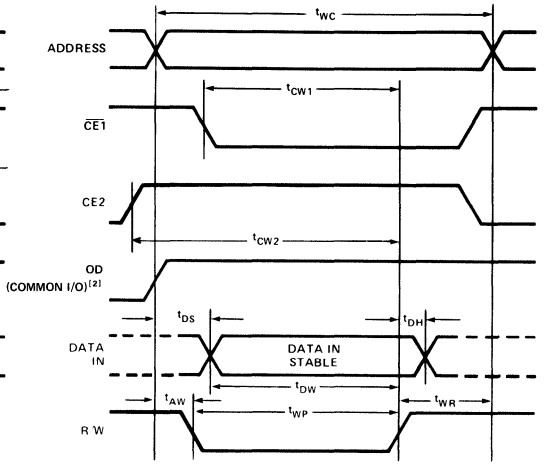
NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.

Waveforms

READ CYCLE



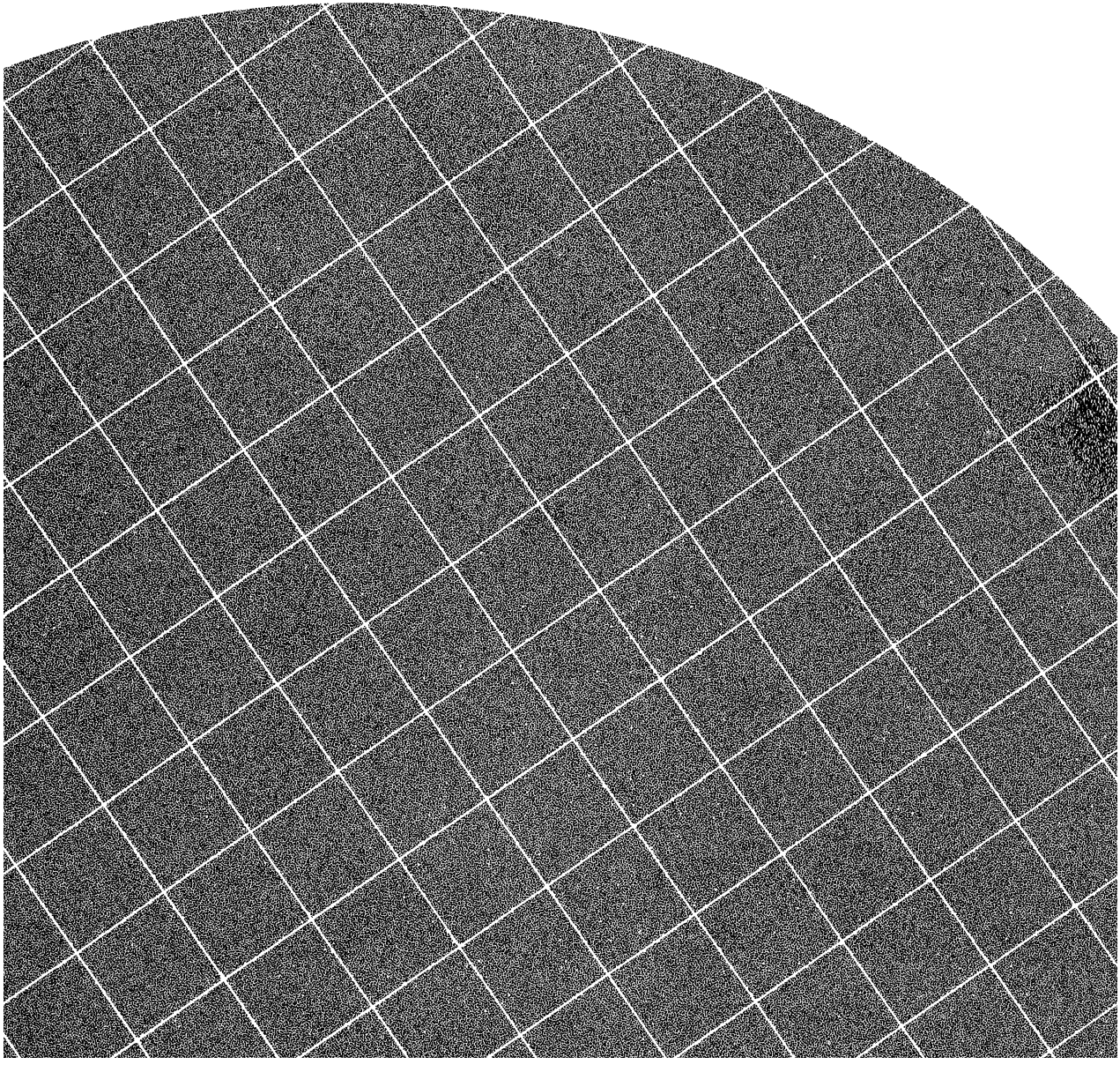
WRITE CYCLE



NOTES:

1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

Read Only Memory 4



MOS EPROM AND ROM FAMILY

	Type	No. of Bits	Organization	No. of Pins	Output[1]	Maximum Access (ns)	Maximum Power Dissipation (mW)	Operating Temperature Range (°C)	Power Supply (V)	Page No.
MOS ROM	**2316E**	16384	2048 x 8	24	T.S.	450	630	0 to 70	5V ± 10%	4-12
MOS ROM	**2332A**	32768	4096 x 8	24	T.S.	TBD	TBD	0 to 70	5V ± 10%	4-15
MOS ROM	**2364A**	65536	8192 x 8	28	T.S.	TBD	TBD	0 to 70	5V ± 10%	4-16
ONE TIME PROGRAMMABLE PROM	**2608**	8192	1024 x 8	24	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% – 5V ± 5%	4-17
MOS EPROM	**1702A**	2048	256 x 8	24	T.S.	1 μs	885	0 to 70	5V ± 5% – 9V ± 5%	4-5
MOS EPROM	1702A-2	2048	256 x 8	24	T.S.	650	959	0 to 70	5V ± 5% – 9V ± 5%	4-5
MOS EPROM	1702A-6	2048	256 x 8	24	T.S.	1.5 μs	885	0 to 70	5V ± 5% – 9V ± 5%	4-5
MOS EPROM	**M1702A**	2048	256 x 8	24	T.S.	850	960	– 55 to 100	5V ± 10% – 9V ± 10%	14-5
MOS EPROM	**1702AL**	2048	256 x 8	24	T.S.	1 μs	221	0 to 70	5V ± 5% – 9V ± 5%	4-9
MOS EPROM	1702AL-2	2048	256 x 8	24	T.S.	650	221	0 to 70	5V ± 5% – 9V ± 5%	4-9
MOS EPROM	**2704**	4096	512 x 8	24	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% – 5V ± 5%	4-20
MOS EPROM	**2708**	8192	1024 x 8	24	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% – 5V ± 5%	4-21
MOS EPROM	2708L	8192	1024 x 8	24	T.S.	450	425	0 to 70	5V ± 5% 12V ± 5% – 5V ± 5%	4-21
MOS EPROM	2708-1	8192	1024 x 8	24	T.S.	350	800	0 to 70	5V ± 5% 12V ± 5% – 5V ± 5%	4-21
MOS EPROM	I2708	8192	1024 x 8	24	T.S.	450	800	– 40 to 85	12V ± 5% – 5V ± 5%	13-4
MOS EPROM	**M2708**	8192	1024 x 8	24	T.S.	450	750	– 55 to 100	12V ± 10% – 5V ± 10%	14-22
MOS EPROM	**2716**	16384	2048 x 8	24	T.S.	450	525/132[2]	0 to 70	5V ± 5%	4-23
MOS EPROM	2716-1	16384	2048 x 8	24	T.S.	350	550/138[2]	0 to 70	5V ± 10%	4-23
MOS EPROM	2716-2	16384	2048 x 8	24	T.S.	390	525/132[2]	0 to 70	5V ± 5%	4-23
MOS EPROM	I2716	16384	2048 x 8	24	T.S.	450	603/165[2]	– 40 to 85	5V ± 5%	13-5
MOS EPROM	**M2716**	16384	2048 x 8	24	T.S.	450	603/165[2]	– 55 to 100	5V ± 10%	14-28
MOS EPROM	**2732**	32768	4096 x 8	24	T.S.	450	788/158[2]	0 to 70	5V ± 5%	4-28
MOS EPROM	**2758**	8192	1024 x 8	24	T.S.	450	525/132[2]	0 to 70	5V ± 5%	4-31

Notes: 1. T.S. is a three state output.
2. Static standby mode feature.

Disk L1, file 819-1

BIPOLAR PROM FAMILY

Type	No. of Bits	Organization	No. of Pins	Output[1]	Maximum Access (ns)	Maximum Power Dissipation (mW)	Operating Temperature Range (°C)	Power Supply	Page No.
3604A	4096	512x8	24	O.C.	70	895	0 to 75	5V ± 5%	4-36
3604A-2	4096	512x8	24	O.C.	60	895	0 to 75	5V ± 5%	
3604AL	4096	512x8	24	O.C.	90	685/135[2]	0 to 75	5V ± 5%	
3624A	4096	512x8	24	T.S.	70	895	0 to 75	5V ± 5%	
3624A-2	4096	512x8	24	T.S.	60	895	0 to 75	5V ± 5%	
M3604A	4096	512x8	24	O.C.	90	1045	– 55 to 125	5V ± 10%	14-33
M3624A	4096	512x8	24	T.S.	90	1045	– 55 to 125	5V ± 10%	
3605A	4096	1024x4	18	O.C.	60	735	0 to 75	5V ± 5%	4-39
3605A-1	4096	1024x4	18	O.C.	50	735	0 to 75	5V ± 5%	
3625A	4096	1024x4	18	T.S.	60	735	0 to 75	5V ± 5%	
3625A-1	4096	1024x4	18	T.S.	50	735	0 to 75	5V ± 5%	
M3625A	4096	1024x4	18	T.S.	60	998	0 to 75	5V ± 5%	14-35
3628	8192	1024x8	24	T.S.	80	998	0 to 75	5V ± 5%	4-42
3628-4	8192	1024x8	24	T.S.	100	998	0 to 75	5V ± 5%	
3636	16384	2048x8	24	T.S.	80	998	0 to 75	5V ± 10%	4-45
3636-1	16384	2048x8	24	T.S.	65	998	0 to 75	5V ± 10%	
M3636	16384	2048x8	24	T.S.	80	998	– 50 to 125	5V ± 5%	14-38

Notes: 1. O.C. and T.S. are open collector and three-state output respectively.
2. The 3604AL has a low power dissipation feature.

| ROM and PROM Programming Instructions | 4-48 |

BIPOLAR PROM CROSS REFERENCE

Part Number	Prefix and Manufacturer	Organization	Intel Part Number	
			Direct Replacement	For New Designs
5340-1	MMI	512 x 8	M3624A	
5341-1	MMI	512 x 8	M3624A	
5604C	IM—Intersil	512 x 4	3602A	
5605C	IM—Intersil	512 x 8	3604A	
5624C	IM—Intersil	512 x 4	3622A	
5625C	IM—Intersil	512 x 8	3624A	
6305-1	MMI	512 x 4		3604A
6306-1	MMI	512 x 4		3625A
6340-1	MMI	512 x 8	3604A	
6341-1	MMI	512 x 8	3624A	
6352-1	MMI	1024 x 4		3625A
6353-1	MMI	1024 x 4	3625A	
6380-1	MMI	1024 x 8		3628
6381-1	MMI	1024 x 8	3628	
74S472	TI	512 x 8		3624A
74S473	TI	512 x 8		3604A
74S474	TI	512 x 8	3624A	
74S475	TI	512 x 8	3604A	
74S570	National	512 x 4		3604A
74S571	National	512 x 4		3625A
7620-5	HM—Harris	512 x 4		3604A
7621-5	HM—Harris	512 x 4		
7640-2	HM—Harris	512 x 8		M3604A
7640-5	HM—Harris	512 x 8	3604A	
7641-2	HM—Harris	512 x 8		M3624A
7641-5	HM—Harris	512 x 8	3624A	
7642-5	HM—Harris	1024 x 4	3605A	
7643-5	HM—Harris	1024 x 4	3625A	
7644-5	HM—Harris	1024 x 4		3625A
7680-5	HM—Harris	1024 x 8		3628
7681-5	HM—Harris	1024 x 8	3628	
82S115	N—Signetics	512 x 8		3624A
82S115	S—Signetics	512 x 8		M3624A
82S130	N—Signetics	512 x 4		3604A
82S131	N—Signetics	512 x 4		3625A
82S140	N—Signetics	512 x 8	3604A-2	
82S141	N—Signetics	512 x 8	3624A-2	
82S136	N—Signetics	1024 x 4		3625A-1
82S137	N—Signetics	1024 x 4	3625A-1	
82S137	S—Signetics	1024 x 4	M3625A	
82S180	N—Signetics	1024 x 8		3628
82S181	N—Signetics	1024 x 8		3628
82S182	N—Signetics	1024 x 8		3628-1
82S183	N—Signetics	1024 x 8		
82S191	N—Signetics	2048 x 8	3636	
82S191	S—Signetics	2048 x 8	M3636	
87S295	National	512 x 8	3604A	
87S296	National	512 x 8	3624A	
93436C	Fairchild	512 x 4		3604A
93438C	Fairchild	512 x 8		3604A-2
93438M	Fairchild	512 x 8		M3604A
93446C	Fairchild	512 x 4		3625A-1
93448C	Fairchild	512 x 8		3624A-2
93448M	Fairchild	512 x 8		M3624A
93452C	Fairchild	1024 x 4	3625A-1	
93453C	Fairchild	1024 x 4	3625A-1	
93453M	Fairchild	1024 x 4	M3625A	

1702A

2K (256 x 8) UV ERASABLE PROM

1702A-2	0.65 us Max.
1702A	1.0 us Max.
1702A-6	1.5 us Max.

- **Fast Access Time: Max. 650 ns (1702A–2)**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Static MOS: No Clocks Required**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

The 1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The 1702A undergoes complete programming and functional testing prior to shipment, thus insuring 100% programmability.

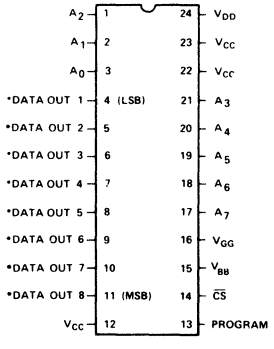
Initially all 2048 bits of the 1702A are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702A to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The circuitry of the 1702A is completely static. No clocks are required. Access times from 650ns to 1.5μs are available. A 1702AL family is available (see 1702AL data sheets for specifications) for those systems requiring lower power dissipation than the 1702A.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

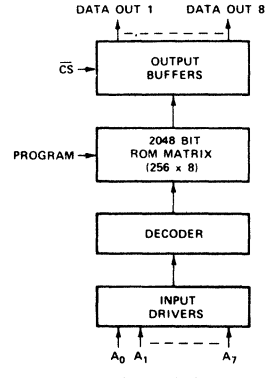


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702A differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the Data Catalog ROM and PROM Programming Instructions section.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5%, V_{GG} = -9V ±5%, unless otherwise noted.

READ OPERATION

Symbol	Test	1702A, 1702A-6 Limits Min.	Typ.[1]	Max.	1702A-2 Limits Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{IH2}
I_{DD1}[1]	Power Supply Current		35	50		40	60	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		37	55	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		43	65	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		7	13	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		6	12	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH1}	Addr. Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
V_{IH2}	Chip Sel. Input High Volt.	V_{CC}-2		V_{CC}+0.3	V_{CC}-1.5		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

Note 1: Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0° C to +70° C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

Symbol	Test	1702A Limits Min.	1702A Limits Max.	1702A-2 Limits Min.	1702A-2 Limits Max.	1702A-6 Limits Min.	1702A-6 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6		0.66	MHz
t_{OH}	Previous Read Data Valid		0.1		0.1		0.1	μs
t_{ACC}	Address to Output Delay		1		0.65		1.5	μs
t_{CS}	Chip Select Delay		0.1		0.3		0.6	μs
t_{CO}	Output Delay From $\overline{CS}$		0.9		0.35		0.9	μs
t_{OD}	Output Deselect		0.3		0.3		0.3	μs

PROM/ROM

Capacitance * T_A = 25°C

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	

*This parameter is periodically sampled and is not 100% tested.

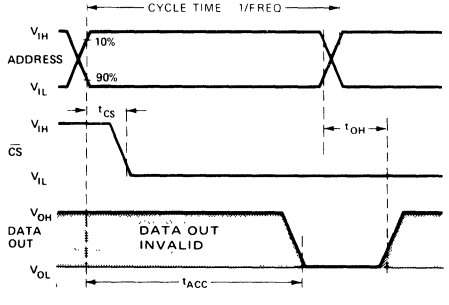
Switching Characteristics

Conditions of Test:

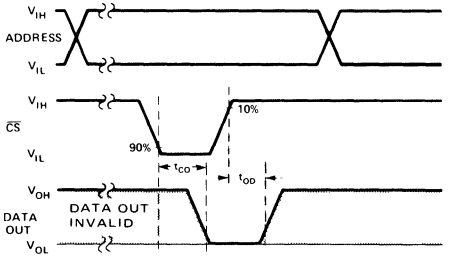
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L=15pF

A) READ OPERATION

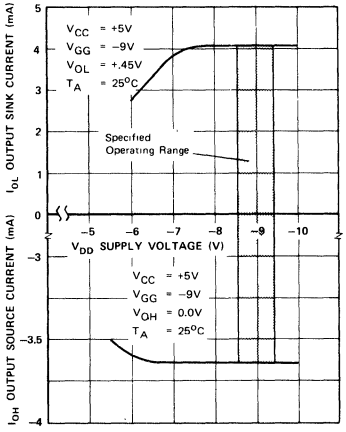


B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION

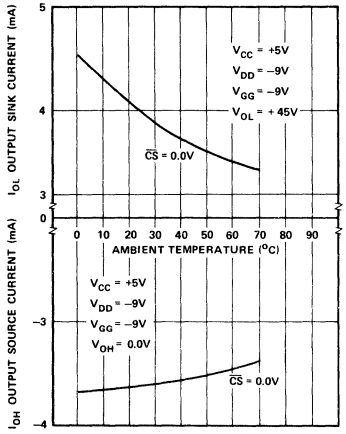


Typical Characteristics

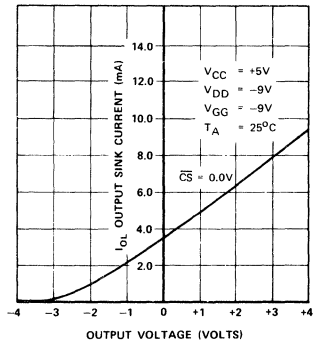
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



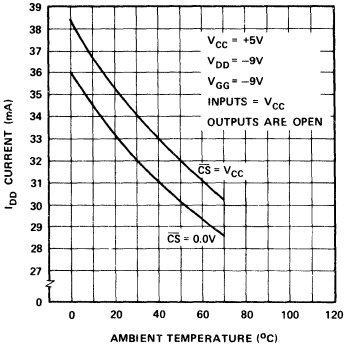
OUTPUT CURRENT VS. TEMPERATURE



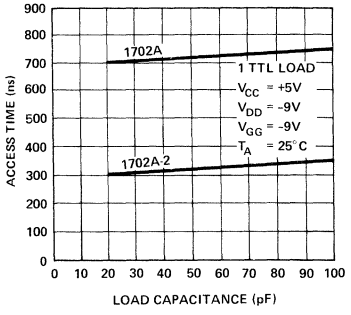
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



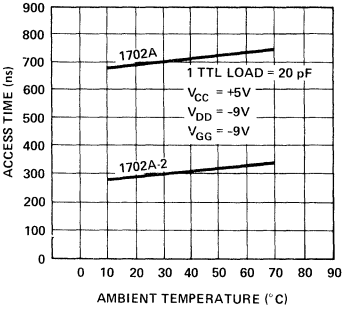
I_{DD} CURRENT VS. TEMPERATURE



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE



2K (256 x 8) UV ERASABLE LOW POWER PROM

Part No.	MAXIMUM ACCESS (μs)	t_{DVGG} (μs)
1702AL	1.0	0.4
1702AL-2	0.65	0.3

- **Clocked V_{GG} Mode for Low Power Dissipation**
- **Fast Programming: 2 Minutes for all 2048 Bits**
- **All 2048 Bits Guaranteed* Programmable: 100% Factory Tested**
- **Inputs and Outputs DTL and TTL Compatible**
- **Three-State Output: OR-tie Capability**

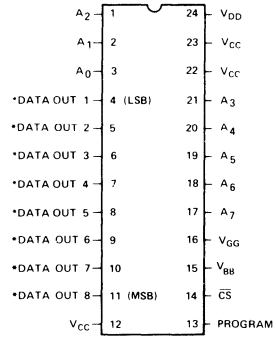
The 1702AL is a 256 word by 8 bit electrically programmable ROM and is the same chip as the industry standard 1702A. The programming and erasing specifications are identical to the 1702A. The 1702AL operates with the V_{GG} clocked to reduce the power dissipation.

Initially all 2048 bits of the 1702AL are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702AL is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702AL to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The 1702AL is fabricated with silicon gate technology. This low threshold technology allows the design and production of high performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONFIGURATION

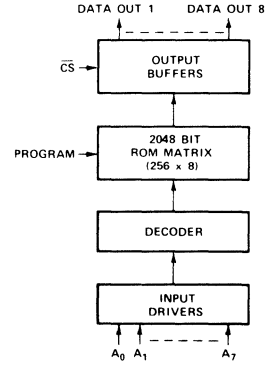


*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

PIN CONNECTIONS

The external lead connections to the 1702AL differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the Data Catalog ROM and PROM Programming Instructions section.*

MODE \ PIN	12 (V_{CC})	13 (Program)	14 (CS)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})	24 (V_{DD})
Read	V_{CC}	V_{CC}	GND	V_{CC}	Clocked V_{GG}	V_{CC}	V_{CC}	V_{DD}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG}	GND	GND	Pulsed V_{DD}

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply
Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

READ OPERATION

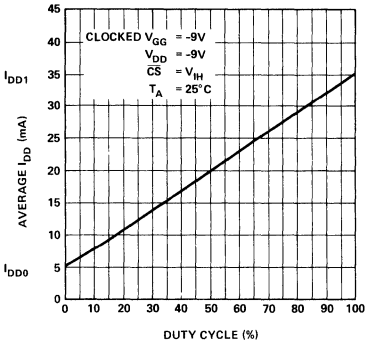
T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = -9V ±5%, V_{GG}[1] = -9V ±5%, unless otherwise noted.

Symbol	Test	1702AL Limits Min.	Typ.[2]	Max.	1702AL-2 Limits Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			1			1	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1			1	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC}-2
I_{DDO1}[1]	Power Supply Current		7	10		7	10	mA	T_A=25°C $\overline{CS}$=V_{IH}, V_{GG}=V_{CC},
I_{DDO2}	Power Supply Current			15			15	mA	T_A=0°C I_{OL}=0.0mA
I_{DD1}[1]	Power Supply Current		35	50		35	50	mA	$\overline{CS}$ = V_{CC} -2, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46		32	46	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	60		38	60	mA	$\overline{CS}$ = V_{CC} -2, I_{OL} = 0.0mA, T_A = 0°C, Continuous
I_{CF1}	Output Clamp Current		8	14		5.5	8	mA	V_{OUT} = -1.0V, T_A = 0°C, Continuous
I_{CF2}	Output Clamp Current		7	13		5	7	mA	V_{OUT} = -1.0V, T_A = 25°C, Continuous
I_{GG}	Gate Supply Current			1			1	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V_{DD}		V_{CC}-6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}-2		V_{CC}+0.3	V_{CC}-2		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		3.5	4.5		V	I_{OH} = -200μA

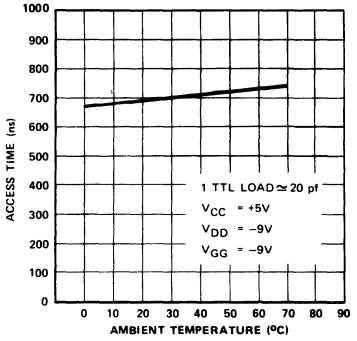
NOTES: 1. The 1702AL is operated with the V_{GG} clocked to obtain low power dissipation. The average I_{DD} will vary between I_{DDO} and I_{DD1} (at 25°C) depending on the V_{GG} duty cycle (see curve opposite). 2. Typical values are at nominal voltage and T_A = 25°C.

TYPICAL CHARACTERISTICS

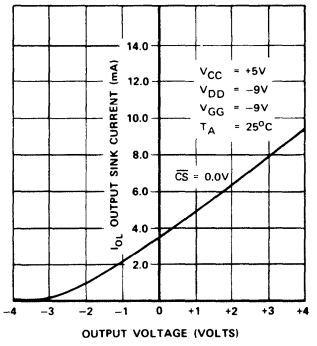
AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



ACCESS TIME VS. TEMPERATURE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



PROM/ROM

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$ unless otherwise noted

Symbol	Test	1702AL Limits Min.	1702AL Limits Max.	1702AL-2 Limits Min.	1702AL-2 Limits Max.	Unit
Freq.	Repetition Rate		1		1.6	MHz
t_{ACC}	Address to output delay		1		0.65	μs
t_{DVGG}	Clocked V_{GG} set up	0.4		0.3		μs
t_{CS}	Chip select delay		0.1		0.3	μs
t_{CO}	Output delay from $\overline{CS}$		0.9		0.35	μs
t_{OD}	Output deselect		0.3		0.3	μs
t_{OHC}	Data out hold in clocked V_{GG} mode		5		5	μs

CAPACITANCE $T_A = 25°C$

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$, $V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance	10	15	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Note 1)		30	pF	

*This parameter is periodically sampled and is not 100% tested.

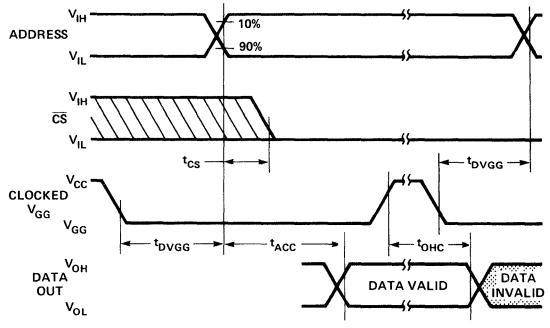
SWITCHING CHARACTERISTICS

Conditions of Test:

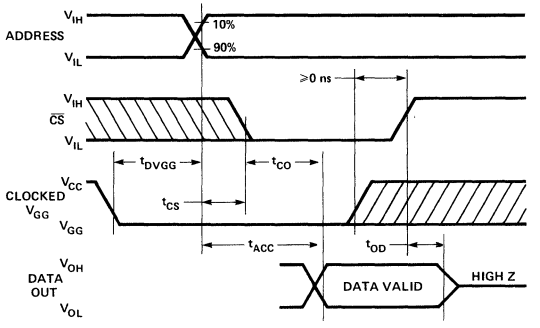
Input pulse amplitudes: 0 to 4V; t_R, $t_F \leqslant 50$ ns

Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leqslant 15$ ns), $C_L = 15$pF

A. READ OPERATION



B. DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION



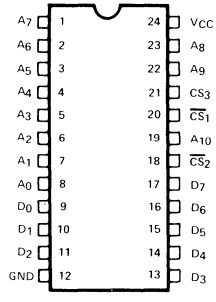
2316E
16K (2K x 8) ROM

- **Fast Access Time—450 ns Max.**
- **Single +5V ± 10% Power Supply**
- **Intel MCS 80 and 85 Compatible**
- **Three Programmable Chip Selects for Simple Memory Expansion and System Interface**
- **EPROM/ROM Pin Compatible for Cost-Effective System Development**
- **Completly Static Operation**
- **Inputs and Outputs TTL Compatible**
- **Three-State Output for Direct Bus Interface**

The Intel® 2316E is a 16,384-bit static, N-channel MOS read only memory (ROM) organized as 2048 words by 8 bits. Its high bit density is ideal for large, non-volatile data storage applications such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common system bus structures. The 2316E single +5V power supply and 450 ns access time are both ideal for usage with high performance microcomputers such as the Intel MCS™-80 and MCS™-85 devices.

A cost-effective system development program may be implemented by using the pin compatible Intel 2716 16K UV EPROM for prototyping and the lower cost 2616 PROM and 2316E ROM for production. The three 2316E programmable chip selects may be defined by the user and are fixed during the masking process. To simplify the conversion from 2716 prototyping to 2316E production, it is recommended that the 2316E programmable chip select logic levels be defined the same as that shown in the below data sheet pin configuration. This pin configuration and these chip select logic levels are the same as the 2716.

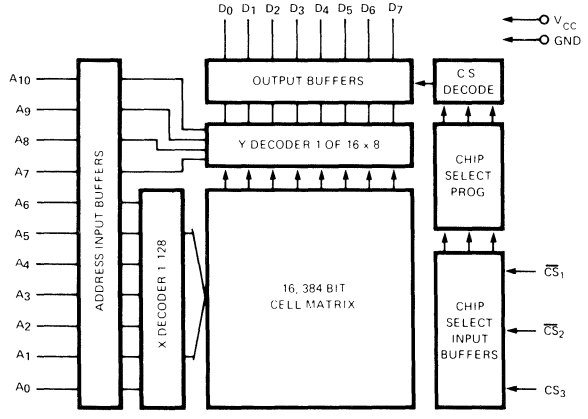
PIN CONFIGURATION



PIN NAMES

A_0–A_{10}	ADDRESS INPUTS
O_7–O_0	DATA OUTPUTS
CS_1–CS_3	CHIP SELECT INPUTS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . -10°C to 80°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin With Respect to Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1.0 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	μA	Chip Deselected, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			-20	μA	Chip Deselected, V_{OUT} = 0.4V
I_{CC}	Power Supply Current		70	120	mA	All Inputs 5.25V Data Out Open
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.4		V_{CC}+1.0V	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -400 μA

NOTE: 1. Typical values for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
t_A	Address to Output Delay Time		450	ns
t_{CO}	Chip Select to Output Enable Delay Time		120	ns
t_{DF}	Chip Deselect to Output Data Float Delay Time	10	100	ns

CONDITIONS OF TEST FOR A.C. CHARACTERISTICS

Output Load . . . . . 1 TTL Gate and C_L = 100 pF
Input Pulse Levels . . . . . 0.8 to 2.4V
Input Pulse Rise and Fall Times (10% to 90%) . . . . . 20 ns
Timing Measurement Reference Level
Input . . . . . 1V and 2.2V
Output . . . . . 0.8V and 2.0V

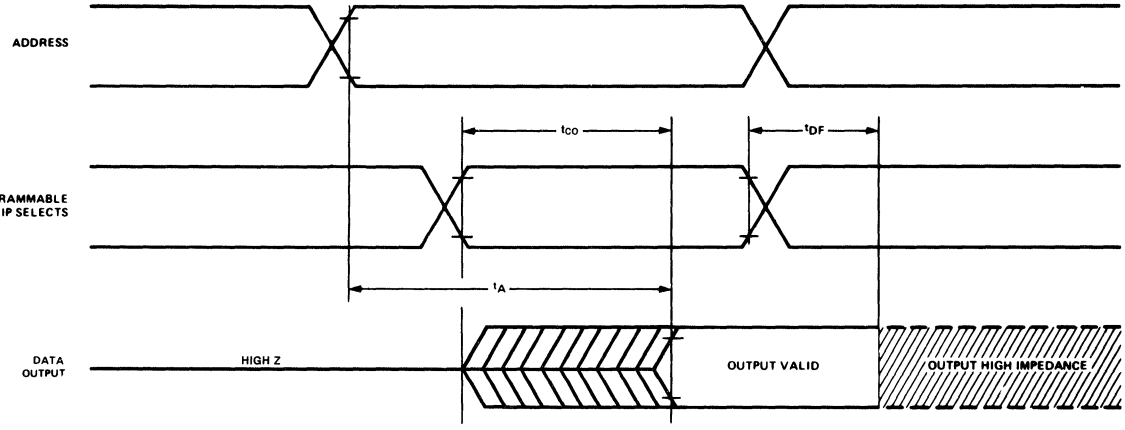
CAPACITANCE(2) T_A = 25°C, f = 1 MHz

SYMBOL	TEST	LIMITS	
		TYP.	MAX.
C_{IN}	All Pins Except Pin Under Test Tied to AC Ground	5 pF	10 pF
C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground	10 pF	15 pF

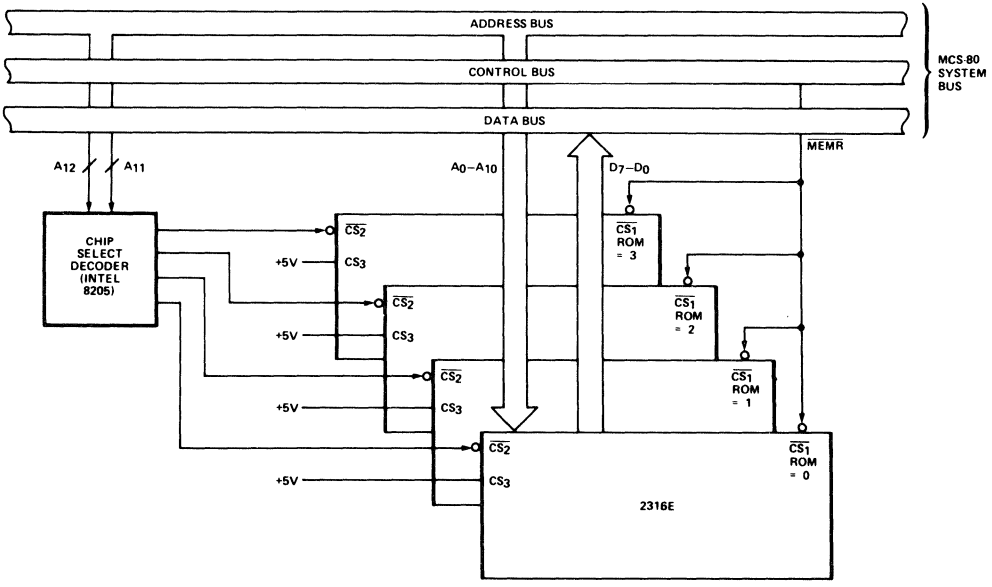
NOTE: 2. This parameter is periodically sampled and is not 100% tested.

PROM/ROM

A.C. Waveforms



Typical System Application (8K × 8 ROM Memory)



2332A
32K (4K x 8) ROM

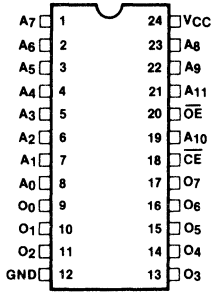
- Single +5V ± 10% Power Supply
- Pin for Pin Compatible with the Intel® 2716 and 2732 EPROMs
- Low Power Dissipation:
  - 150 mA Max Active Current
  - 30 mA Max Standby Current
- Completely Static Operation
- Inputs and Outputs TTL Compatible
- Three-State Output for Direct Bus Interface
- MCS-85™ and MCS-86™ Compatible
- Independent Output Enable Function

The Intel® 2332A is a single +5V supply, 32,768-bit N-channel MOS read only memory organized as 4096 words by 8-bits. The 2332A has a static standby mode which reduces the active power dissipation by more than 75%.

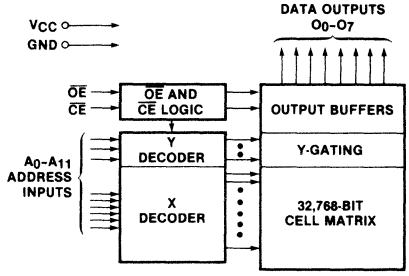
The 2332A is ideal for microprocessor systems, especially those with common input and output bus structures. The separate output control, $\overline{OE}$, eliminates bus contention. Three-state outputs and TTL input/output levels further simplify system design.

A cost effective system development program may be implemented by using the pin compatible Intel® 2732, 32K UV EPROM for prototyping and the 2332A ROM for volume production. The 2732 is pin for pin compatible to the 2332A in all respects.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

$A_0 - A_{11}$	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

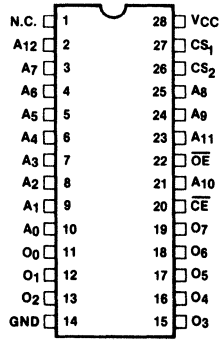
2364A
64K (8K × 8) BIT ROM

- **Single +5V ± 10% Power Supply**
- **Pin Compatible to Intel® 2732 EPROM**
- **Completely Static Operation**
- **Static Standby Mode**
- **Inputs and Outputs TTL Compatible**
- **Independent Output Enable Function**
- **Three-State Output for Direct Bus Interface**
- **MCS-85 and MCS-86 Compatible**

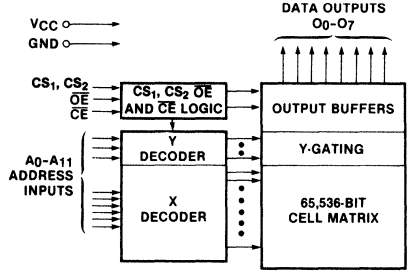
The Intel® 2364A is a single +5V, 65,536-bit N-channel MOS read only memory organized as 8192 words by 8 bits and is pin and function compatible with the 2732 UV EPROM. Its high bit density is ideal for large, non-volatile data storage, such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common bus structures. The 2364A has a static standby mode which reduces the active power dissipation by over 75%.

A cost-effective system development program may be implemented by using the Intel® 2732 32K UV EPROM for prototyping and the 2364A ROM for production. The lower 24 pins of the 2364A are the same as the 2732 to facilitate board designs in making the transition from EPROM to ROM.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

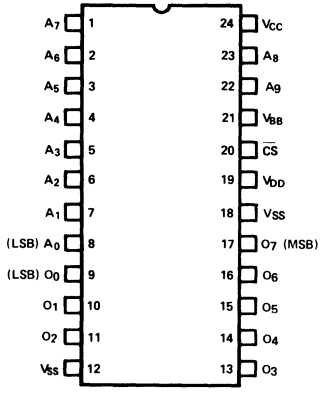
A_0-A_{12}	ADDRESSES
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
CS	CHIP SELECT
N.C.	NO CONNECTION

2608
8K (1K x 8) FACTORY PROGRAMMABLE PROM

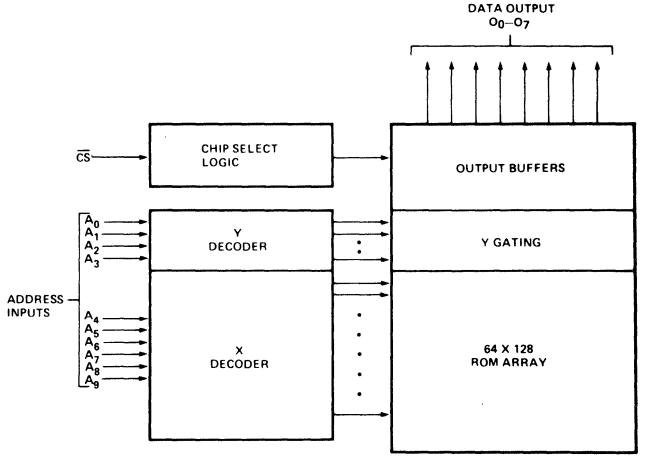
- **Fast Access Time — 450 ns Max.**
- **Pin Compatible to 2708 EPROM**
- **Static — No Clocks Required**
- **Data Inputs and Outputs TTL Compatible**
- **Three-State Outputs — OR-Tie Capability**

The Intel® 2608 is a 8192-bit, one-time factory-programmable MOS PROM organized as 1K words by 8 bits. The electrical characteristics are specified over the 0°C to 70°C operating temperature range with 5% power supply variation. The 2608 features are ideally suited for microprocessor systems: 450 ns maximum access time, three-state outputs for common bussing, and TTL inputs/outputs for easy interfacing. The 2608 is fully compatible to the 2708 in all respects.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$	CHIP SELECT/WRITE ENABLE INPUT

MODE SELECTION

	PIN NUMBER						
MODE	DATA I/O 9-11 13-17	ADDRESS INPUTS 1-8, 22,23	V_{SS} 12	V_{DD} 19	$\overline{CS}$ 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	+12	V_{IH}	-5	+5

Absolute Maximum Ratings*

Temperature Under Bias	-25°C to +85°C
Storage Temperature	-65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to -0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to -0.3V
All Input or Output Voltages With Respect to V_{BB}	+15V to -0.3V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

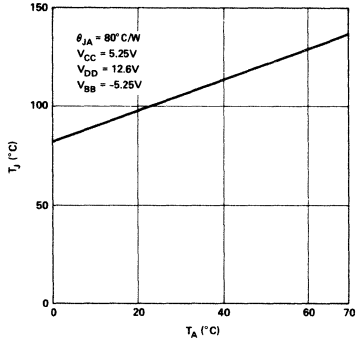
$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, V_{BB}[1] $= -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	$V_{IN} = 5.25V$ or $V_{IN} = V_{IL}$
I_{LO}	Output Leakage Current		1	10	μA	$V_{OUT} = 5.5V$, $\overline{CS}/WE = 5V$
I_{DD}[3]	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}[3]	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}[3]	V_{BB} Supply Current		30	45	mA	$\overline{CS}/WE = 5V$; $T_A = 0°C$
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 1.6mA$
V_{OH1}	Output High Voltage	3.7			V	$I_{OH} = -100\mu A$
V_{OH2}	Output High Voltage	2.4			V	$I_{OH} = -1mA$
P_D	Power Dissipation			800	mW	$T_A = 70°C$

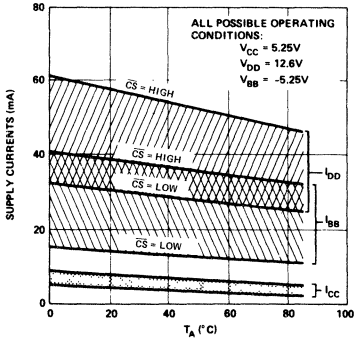
NOTES:
1. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. The total power dissipation is specified at 800 mW. It is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

Typical Characteristics

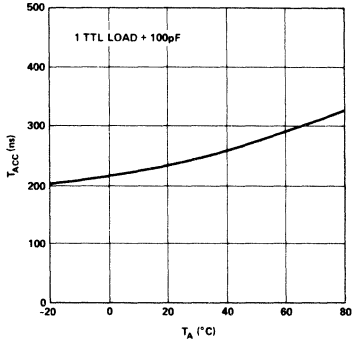
MAXIMUM JUNCTION TEMPERATURE VS. AMBIENT TEMPERATURE



RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



ACCESS TIME VS. TEMPERATURE



A. C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
t_{ACC}	Address to Output Delay		280	450	ns
t_{CO}	Chip Select to Output Delay		60	120	ns
t_{DF}	Chip Deselect to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

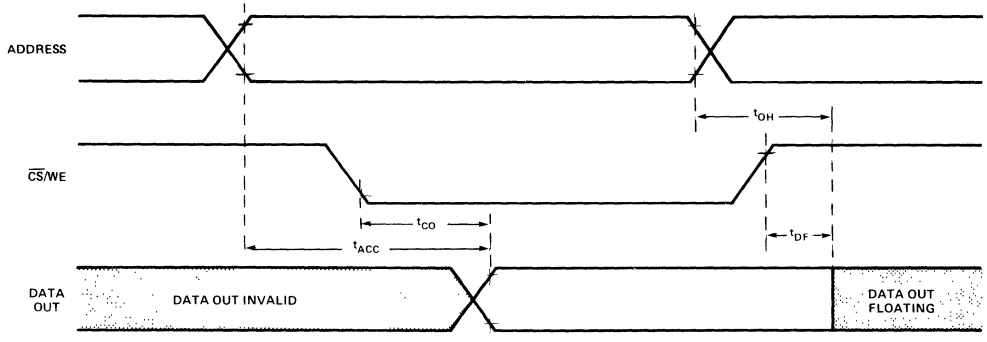
Symbol	Parameter	Typ.	Max.	Unit.	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: 1. This parameter is periodically sampled and is not 100% tested.

A.C. TEST CONDITIONS:

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: $\leqslant 20$ ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs.
Input Pulse Levels: 0.65V to 3.0V

Waveforms



2708/8708*
8K AND 4K UV ERASABLE PROM

	Max. Power	Max. Access	Organization
2708	800 mW	450 ns	1K x 8
2708L	425 mW	450 ns	1K x 8
2708-1	800 mW	350 ns	1K x 8
2704	800 mW	450 ns	512 x 8

- **Low Power Dissipation — 425 mW Max. (2708L)**
- **Fast Access Time — 350 ns Max. (2708-1)**
- **Static — No Clocks Required**
- **Data Inputs and Outputs TTL Compatible during both Read and Program Modes**
- **Three-State Outputs — OR-Tie Capability**

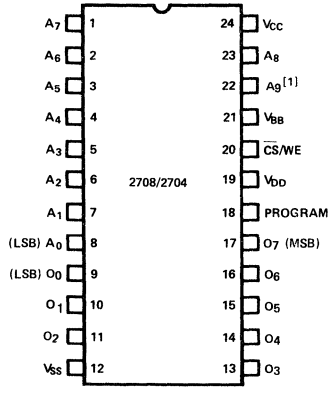
PROM/ROM

The Intel® 2708 is a 8192-bit ultraviolet light erasable and electrically reprogrammable EPROM, ideally suited where fast turnaround and pattern experimentation are important requirements. All data inputs and outputs are TTL compatible during both the read and program modes. The outputs are three-state, allowing direct interface with common system bus structures.

The 2708L at 425 mW is available for systems requiring lower power dissipation than from the 2708. A power dissipation savings of over 50%, without any sacrifice in speed, is obtained with the 2708L. The 2708L has high input noise immunity and is specified at 10% power supply tolerance. A high-speed 2708-1 is also available at 350 ns for microprocessors requiring fast access times. For smaller size systems there is the 4096-bit 2704 which is organized as 512 words by 8 bits. All these devices have the same programming and erasing specifications of the 2708. The 2704 electrical specifications are the same as the 2708.

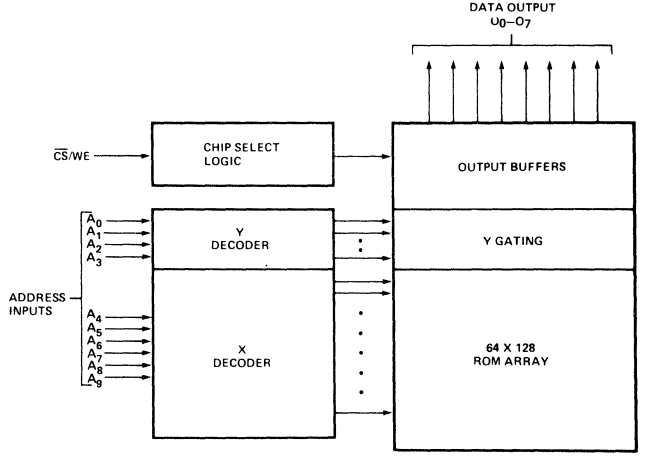
The 2708 family is fabricated with the N-channel silicon gate FAMOS technology and is available in a 24-pin dual in-line package.

PIN CONFIGURATION



NOTE 1: PIN 22 MUST BE CONNECTED TO V_{SS} FOR THE 2704.

BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1-8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED 26V	+12	V_{IHW}	-5	+5

*All 8708 specifications are identical to the 2708 specifications.

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

Absolute Maximum Ratings*

Temperature Under Bias	-25°C to +85°C
Storage Temperature	-65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to -0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to -0.3V
All Input or Output Voltages With Respect to V_{BB} During Read	+15V to -0.3V
$\overline{CS}$/WE Input With Respect to V_{BB} During Programming	+20V to -0.3V
Program Input With Respect to V_{BB}	+35V to -0 3V
Power Dissipation	1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PROM/ROM

DC and AC Operating Conditions During Read

	2708	2708-1	2708L
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C
V_{CC} Power Supply	5V ± 5%	5V ± 5%	5V ± 10%
V_{DD} Power Supply	12V ± 5%	12V ± 5%	12V ± 10%
V_{BB} Power Supply	-5V ± 5%	-5V ± 5%	-5V ± 10%

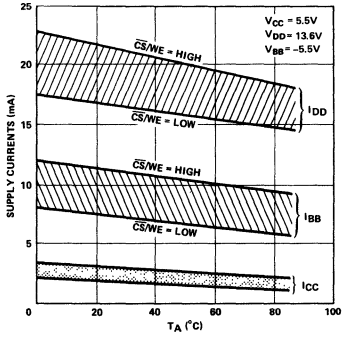
READ OPERATION

D.C. and Operating Characteristics

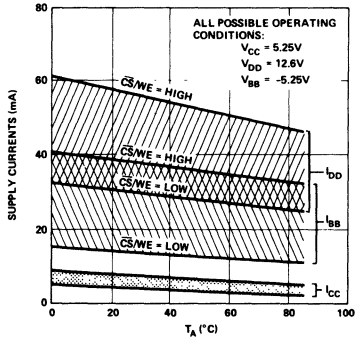
Symbol	Parameter	2708, 2708-1 Limits			2708L Limits			Units	Test Conditions
		Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.		
I_{LI}	Address and Chip Select Input Sink Current		1	10		1	10	μA	V_{IN} = 5.25V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10		1	10	μA	V_{OUT} = 5.5V, CS/WE = 5V
I_{DD}[3]	V_{DD} Supply Current		50	65		21	28	mA	Worst Case Supply Currents[4]
I_{CC}[3]	V_{CC} Supply Current		6	10		2	4	mA	All Inputs High;
I_{BB}[3]	V_{BB} Supply Current		30	45		10	14	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	2.2		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45			0.4	V	I_{OL} = 1.6mA (2708, 2708-1)
									I_{OL} = 2mA (2708L)
V_{OH1}	Output High Voltage	3.7			3.7			V	I_{OH} = -100 μA
V_{OH2}	Output High Voltage	2.4			2.4			V	I_{OH} = -1 mA
PD	Power Dissipation			800			325	mW	T_A = 70°C
							425	mW	T_A = 0°C

NOTES:
1. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. The total power dislipation is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only
4. I_{BB} for the 2708L is specified in the programmed state and is 18 mA maximum in the unprogrammed state.

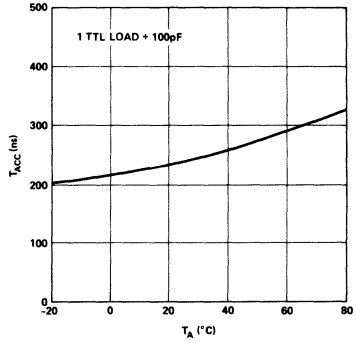
2708L RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



2708 AND 2708-1 RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



ACCESS TIME VS. TEMPERATURE



A. C. Characteristics

Symbol	Parameter	2708-1 Limits Min.	Typ.	Max.	2708, 2708L, Limits Min.	Typ.	Max.	Units
t_{ACC}	Address to Output Delay		280	350		280	450	ns
t_{CO}	Chip Select to Output Delay		60	120		60	120	ns
t_{DF}	Chip Deselect to Output Float	0		120	0		120	ns
t_{OH}	Address to Output Hold	0			0			ns

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

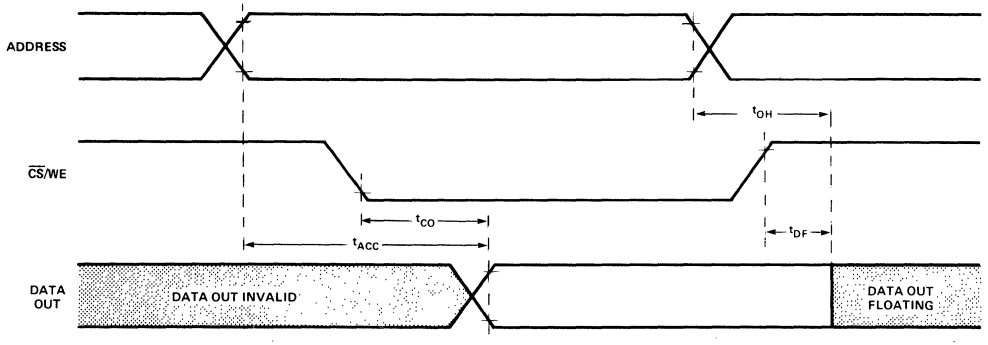
Symbol	Parameter	Typ.	Max.	Unit.	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: 1. This parameter is periodically sampled and is not 100% tested.

A.C. TEST CONDITIONS:

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤20 ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs.
Input Pulse Levels: 0.65V to 3.0V

Waveforms



ERASURE CHARACTERISTICS

The erasure characteristics of the 2708 family are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical device in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2708 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available form Intel which should be placed over the 2708 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog PROM/ROM Programming Instructions Section) for the 2708 family is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

2716
16K (2K x 8) UV ERASABLE PROM

- **Fast Access Time**
  - **— 350 ns Max. 2716-1**
  - **— 390 ns Max. 2716-2**
  - **— 450 ns Max. 2716**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— 525 mW Max. Active Power**
  - **— 132 mW Max. Standby Power**
- **Pin Compatible to Intel® 5V ROMs (2316E, 2332A, and 2364A) and 2732 EPROM**
- **Simple Programming Requirements Single Location Programming Programs with One 50 ms Pulse**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

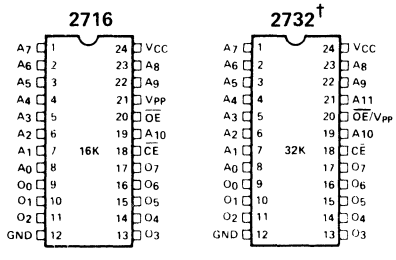
PROM/ROM

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2716 user can convert rapidly to Intel's pin-for-pin compatible 16K ROM (the 2316E) or the new 32K and 64K ROMs (the 2332A and 2364A respectively).

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



†Refer to 2732 data sheet for specifications

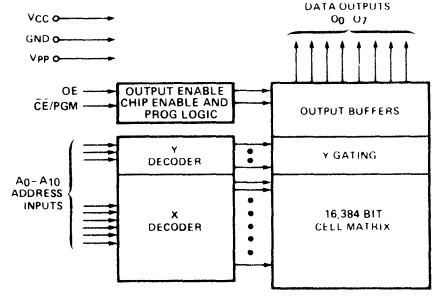
PIN NAMES

A_0–A_{10}	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
All Input or Output Voltages with Respect to Ground . . . . . +6V to -0.3V
V_{PP} Supply Voltage with Respect to Ground During Program . . . . . +26.5V to -0.3V

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PROM/ROM

DC and AC Operating Conditions During Read

	2716	2716-1	2716-2
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C
V_{CC} Power Supply [1,2]	5V ± 5%	5V ± 10%	5V ± 5%
V_{PP} Power Supply [2]	V_{CC}	V_{CC}	V_{CC}

READ OPERATION

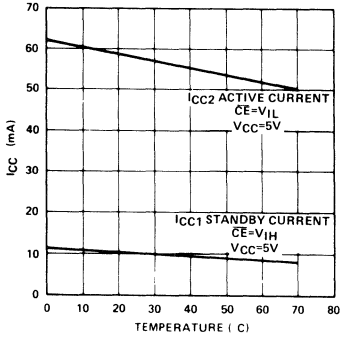
D.C. and Operating Characteristics

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ. [3]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1} [2]	V_{PP} Current			5	mA	V_{PP} = 5.25V
I_{CC1} [2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2} [2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

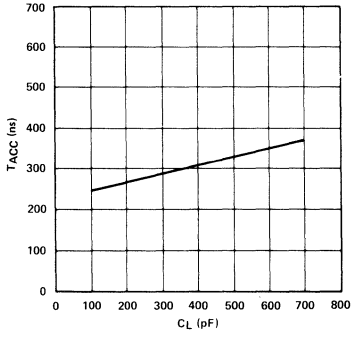
NOTES: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.

Typical Characteristics

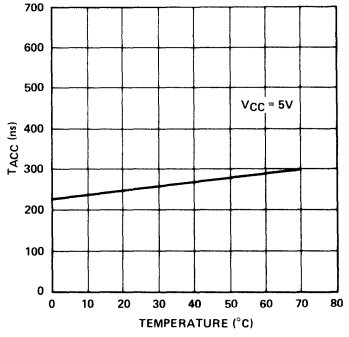
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



A.C. Characteristics

Symbol	Parameter	2716 Limits			2716-1 Limits			2716-2 Limits			Unit	Test Conditions
		Min	Typ[3]	Max	Min	Typ[3]	Max	Min	Typ[3]	Max		
t_{ACC}	Address to Output Delay			450			350			390	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay			450			350			390	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			120			120			120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		100	0		100	0		100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0			0			0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

PROM/ROM

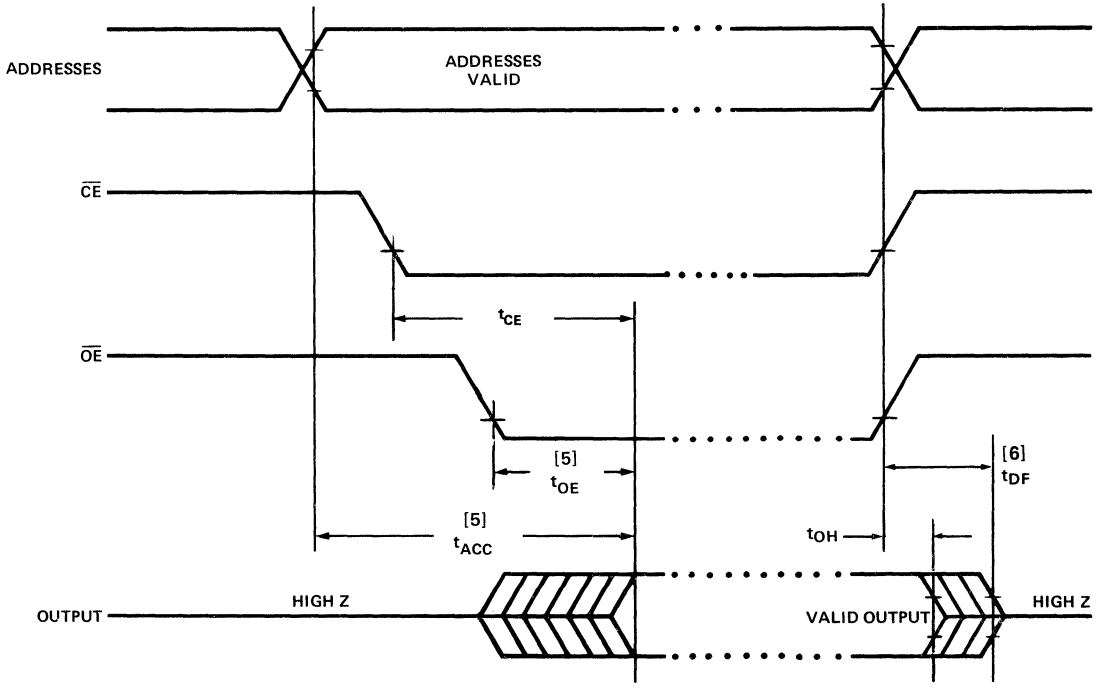
Capacitance[4] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

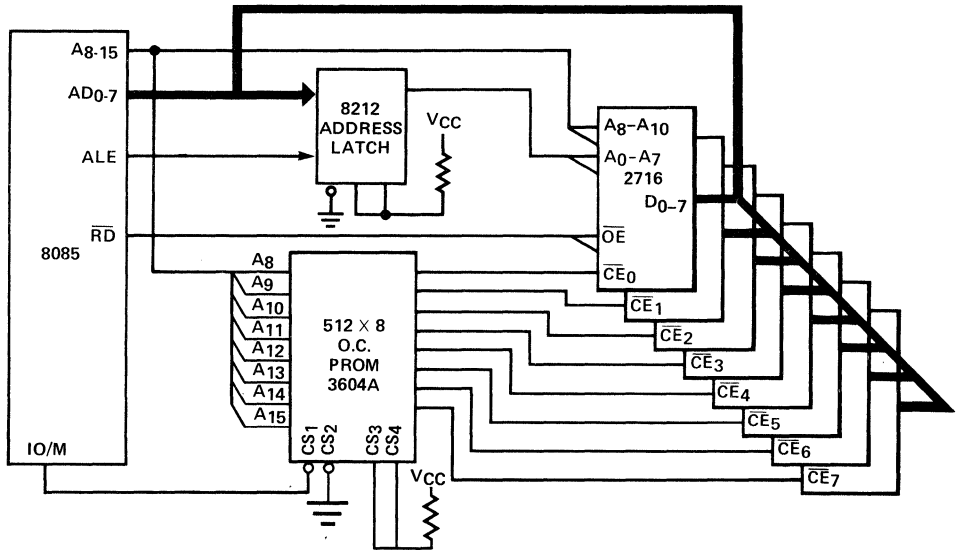
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A. C. Waveforms [1]



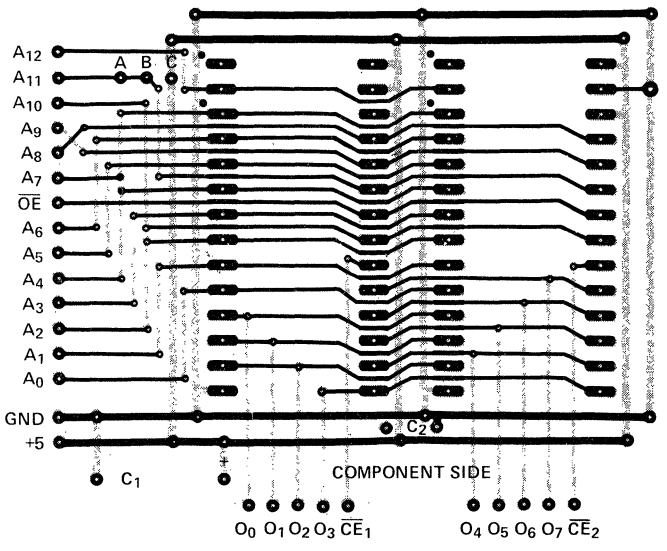
NOTE: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
6. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

TYPICAL 16K EPROM SYSTEM



- This scheme accomplished by using $\overline{CE}$ (PD) as the primary decode. $\overline{OE}$ (CS) is now controlled by previously unused signal. RD now controls data on and off the bus by way of $\overline{OE}$.
- A selected 2716 is available for systems which require $\overline{CE}$ access of less than 450 ns for decode network operation.
- The use of a PROM as a decoder allows for:
  a) Compatibility with upward (and downward) memory expansion.
  b) Easy assignment of ROM memory modules, compatible with PL/M modular software concepts.

8K, 16K, 32K, 64K 5V EPROM/ROM FAMILY PRINTED CIRCUIT BOARD LAYOUT



ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog PROM/ROM Programming Instruction Section) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

TABLE I. MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because 2716's are usually used in larger memory arrays, Intel has provided a 2 line control function that accomodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled 2716s.

PROGRAM INHIBIT

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that 2716. A low level $\overline{CE}$/PGM input inhibits the other 2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed wth V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

2732
32K (4K x 8) UV ERASABLE PROM

- **Single +5V ± 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Fast Access Time: 450ns Max.**
- **Low Power Dissipation:**
  150mA Max. Active Current
  30mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM and 2332/2364 ROMs**
- **Completely Static**
- **Simple Programming Requirements**
  — Single Location Programming
  — Programs with One 50ms Pulse
- **Three-State Output for Direct Bus Interface**

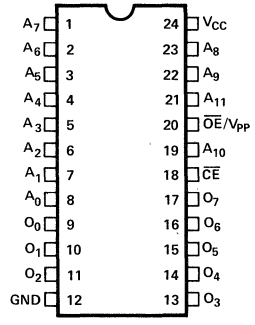
PROM/ROM

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. For production, the pin compatible 2332 and 2364 ROMs are available. The total programming time for all bits is three and a half minutes. All these features make designing with the 2732 in microcomputer systems faster, easier, and more economical.

An important 2732 feature is the separate output control, Output Enable ($\overline{OE}$), from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-30 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's 2716 and 2732 EPROMs. AP-30 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

PIN CONFIGURATION



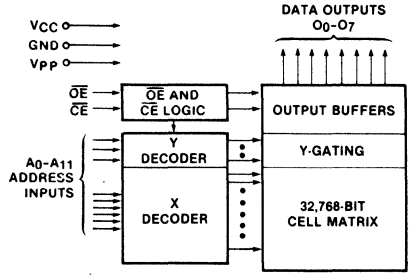
PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +125°C
All Input or Output Voltages with
Respect to Ground ..... +6V to -0.3V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

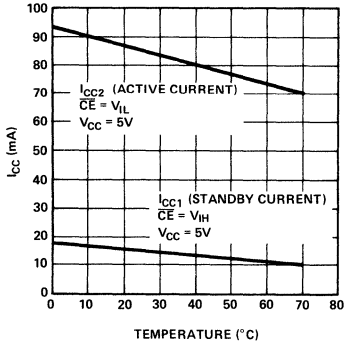
READ OPERATION

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
I_{LI1}	Input Load Current (except $\overline{OE}/V_{PP}$)			10	µA	V_{IN} = 5.25V
I_{LI2}	$\overline{OE}/V_{PP}$ Input Load Current			300	µA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 5.25V
I_{CC1}	V_{CC} Current (Standby)		15	30	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}	V_{CC} Current (Active)		85	150	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400µA

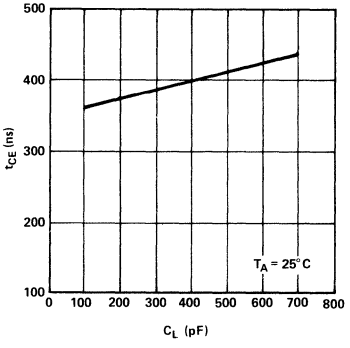
Note: 1. Typical values are for T_A = 25°C and nominal supply voltages.

TYPICAL CHARACTERISTICS

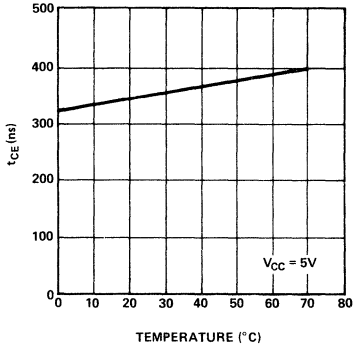
I_{CC} CURRENT VS. TEMPERATURE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. CAPACITANCE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. TEMPERATURE



A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
t_{ACC}	Address to Output Delay			450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay			450	ns	$\overline{OE}$ = V_{IL}
t_{OE}	Output Enable to Output Delay			120	ns	$\overline{CE}$ = V_{IL}
t_{DF}	Output Enable High to Output Float	0		100	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Address to Output Hold	0			ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

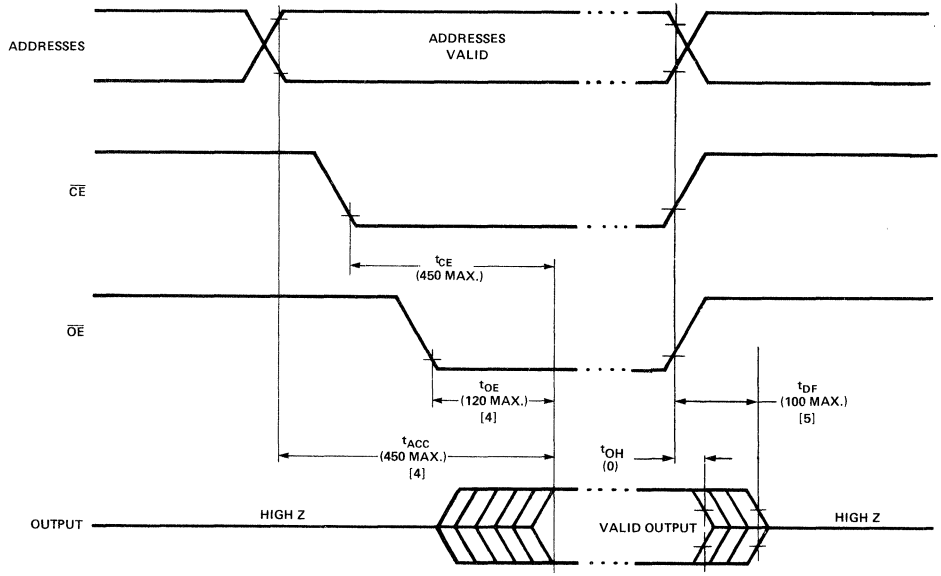
CAPACITANCE [2] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

A.C. TEST CONDITIONS

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. WAVEFORMS [3]



NOTES:
1. TYPICAL VALUES ARE FOR T_A = 25°C AND NOMINAL SUPPLY VOLTAGES
2. THIS PARAMETER IS ONLY SAMPLED AND IS NOT 100% TESTED.
3. ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE NSEC UNLESS OTHERWISE SPECIFIED.
4. $\overline{OE}$ MAY BE DELAYED UP TO 330ns AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
5. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

2758
8K (1K x 8) UV ERASABLE LOW POWER PROM

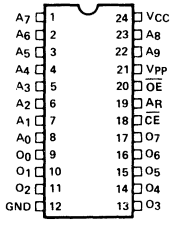
- **Single +5V Power Supply**
- **Simple Programming Requirements**
  Single Location Programming
  Programs with One 50 ms Pulse
- **Low Power Dissipation**
  525 mW Max. Active Power
  132 mW Max. Standby Power
- **Fast Access Time: 450 ns Max. in Active and Standby Power Modes**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**
- **Three-State Outputs for OR-Ties**

The Intel® 2758 is a 8192-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2758 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. The total programming time for all 8192 bits is 50 seconds.

The 2758 has a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW, while the maximum standby power dissipation is only 132 mW, a 75% savings. Power-down is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

A 2758 system may be designed for total upwards compatibility with Intel's 16K 2716 EPROM (see Applications Note 30). The 2758 maintains the simplest and fastest method yet devised for programming EPROMs — single pulse TTL-level programming. There is no need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time — either individually, sequentially, or at random, with the single address location programming.

PIN CONFIGURATION



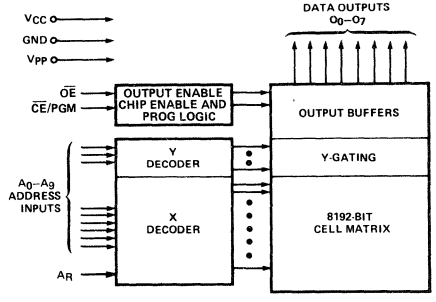
MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	A_R (19)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	V_{IL}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IL}	V_{IH}	+25	+5	High Z

PIN NAMES

A_0–A_9	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS
A_R	SELECT REFERENCE INPUT LEVEL

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions section.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
All Input or Output Voltages with Respect to Ground . . . . . +6V to -0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming . . . . . +26.5V to -0.3V

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

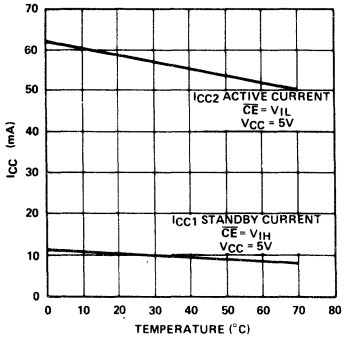
T_A = 0°C to 70°C, V_{CC}[1,2] = +5V ±5%, V_{PP}[2] = V_{CC}

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[3]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.25V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
A_R[4]	Select Reference Input Level	-0.1		0.8	V	I_{IN} = 10 μA
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

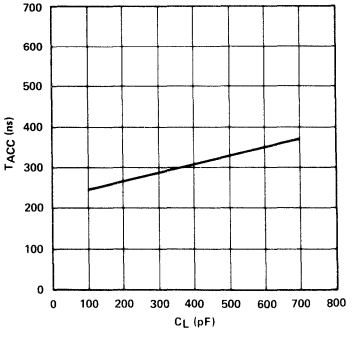
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. A_R is a reference voltage level which requires an input current of only 10 μA. The 2758 S1865 is also available which has a reference voltage level of V_{IH} instead of V_{IL}.

Typical Characteristics

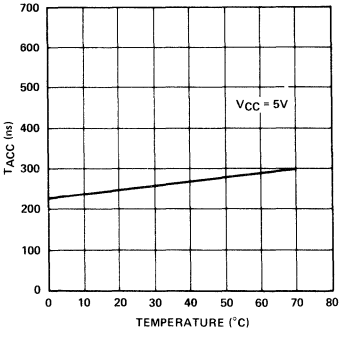
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



A.C. Characteristics

$T_A = 0°C$ to $70°C$, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC}

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[3]	Max.		
t_{ACC}	Address to Output Delay		250	450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		280	450	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			120	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		100	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

Capacitance[4] $T_A = 25°C$, f = 1 MHz

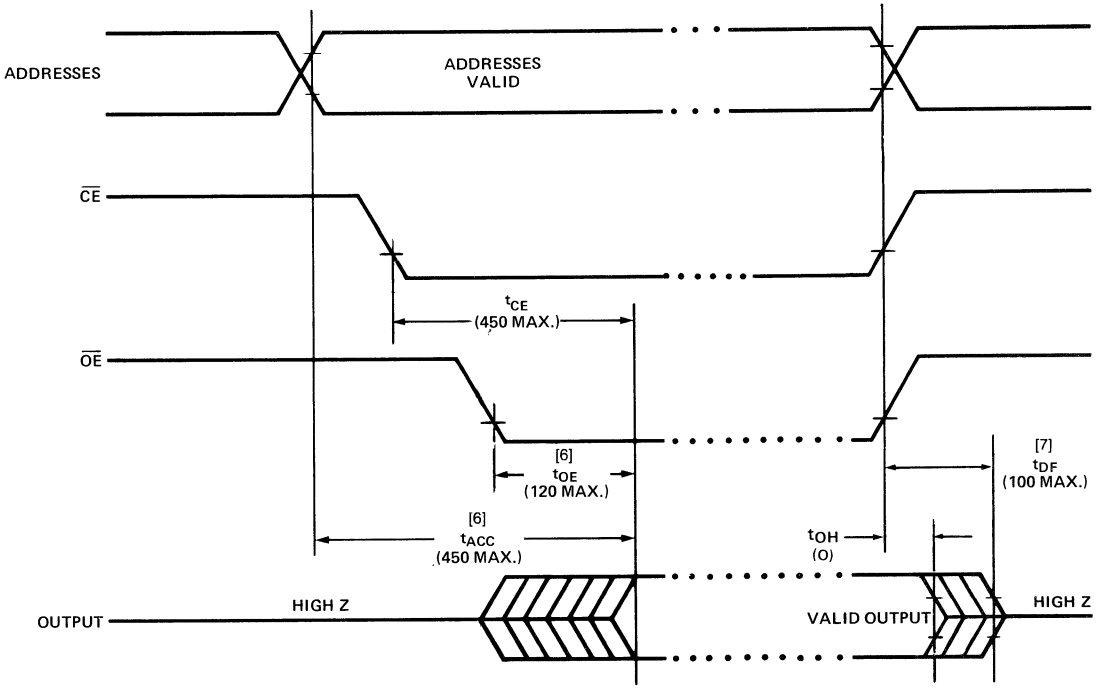
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

NOTE: Please refer to page 2 for notes.

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms[5]



NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. All times shown in parentheses are minimum times and are nsec unless otherwise specified.
6. $\overline{OE}$ may be delayed up to 330 ns after the falling edge of $\overline{CE}$ without impact on t_{ACC}
7. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first

ERASURE CHARACTERISTICS

The erasure characteristics of the 2758 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2758 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2758 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2758 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog Programming Section) for the 2758 is exposure to short-wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated does (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12,000 μW/cm^2 power rating. The 2758 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2758 are listed in Table 1. It should be noted that all inputs for the five modes are at TTL levels. The power supplied required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the two programming modes, and must be at 5V in the other three modes. In all operational modes, A_R must be at V_{IL} (except for the 2758 S1865 which has A_R at V_{IH}).

TABLE I. MODE SELECTION

PINS / MODE	$\overline{CE}$/PGM (18)	A_R (19)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	V_{IL}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The 2758 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2758 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2758 is placed in the standby mode by applying a TTL high signal to $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the OE input.

OUTPUT OR-TIEING

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory Power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING

Initially, and after each erasure, all bits of the 2758 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2758 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec.

The 2758 must be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple 2758s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2758s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled 2758s.

PROGRAM INHIBIT

Programming of multiple 2758s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs(including $\overline{OE}$) of the parallel 2758s may be common. A TTL level program pulse applied to a 2758's $\overline{CE}$/PGM input with V_{PP} at 25V will program that 2758. A low level $\overline{CE}$/PGM input inhibits the other 2758 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

3604A, 3624A FAMILY
4K (512 x 8) HIGH-SPEED PROM

	3604A-2 3624A-2	3604A 3624A	3604AL
Max. T_A(ns)	60	70	90
Max. I_{CC}(mA)	170	170	130/25*

*Standby Current When The Chip is Deselected.

- **Fast Access Time --60ns Max (3604A-2, 3624A-2)**
- **Low Standby Power Dissipation (3604AL) --32 μW/Bit Max**
- **Open Collector (3604A) or Three State (3624A) Outputs**
- **Four Chip Select Inputs For Easy Memory Expansion**
- **Polycrystalline Silicon Fuse For Higher Reliability**
- **Hermetic 24 Pin DIP**

The Intel® 3604A/3624A are 4096-bit bipolar PROMs organized as 512 words by 8 bits. The fast second generation 3604A/3624A replaces its Intel predecessor, the 3604/3624. Higher speed PROMs, the 3604A-2/3624A-2, are now available at 60 ns. All 3604A/3624A specifications, except programming, are the same as or better than the 3604/3624. Once programmed, the 3604A/3624A are interchangeable with the 3604/3624

The PROMs are manufactured with all outputs initially logically high. Logic low levels can be electrically programmed in selected bit locations. Both open collector and three-state outputs are available. Low standby power dissipation can be achieved with the 3604AL. The standby power dissipation is approximately 20% of the active power dissipation.

The 3604A/3624A are available in a hermetic 24-pin dual in-line package. These PROMs are manufactured with the time-proven polycrystalline silicon fuse technology.

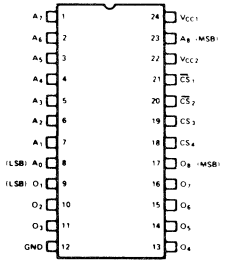
Mode/Pin Connection		Pin 22	Pin 24
READ:	3604A, 3604A-2 3624A, 3624A-2	No Connect or 5V	5V
	3604AL	+5V	Must be Left Open
PROGRAM:	3604A, 3604A-2 3624A, 3624A-2	Pulsed 12.5V	Pulsed 12.5V
	3604AL	Pulsed 12.5V	Pulsed 12.5V
STANDBY:	3604AL	Power dissipation is automatically reduced whenever the 3604AL is deselected.	

PIN NAMES

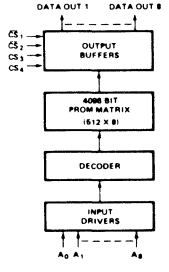
A_0–A_8	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$, CS_3–CS_4 [1]	CHIP SELECT INPUTS
O_1–O_8	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = \overline{CS}_2 = 0$ and $CS_3 = CS_4 = 1$.

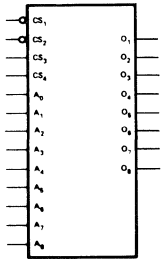
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6 to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10 mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10 mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15 mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC1}	Power Supply Current (3604A, 3604A-2, 3624A, and 3624A-2)		130	170	mA	V_{CC1} = 5.25V, $V_{A0} \rightarrow V_{A8}$ = 0V, $\overline{CS}_1 = \overline{CS}_2$ = 0V, $CS_3 = CS_4$ = 5.25V
I_{CC2}	Power Supply Current (3604AL) Active		100	130	mA	V_{CC2} = 5.25V, V_{CC1} = Open $\overline{CS}_1 = \overline{CS}_2$ = 0.45V, $CS_3 = CS_4$ = 2.4V
	Standby		15	25	mA	$\overline{CS}_1 = \overline{CS}_2$ = 2.5V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

3624A FAMILY ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	μA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1 = \overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-20	-25	-70	mA	V_O = 0V, V_{CC} = 4.75V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAXIMUM LIMITS (ns)			UNIT	TEST CONDITIONS
		3604A-2 3624A-2	3604A 3624A	3604AL		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	70	90	ns	$\overline{CS_1} = \overline{CS_2} = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to Select the PROM
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	120	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

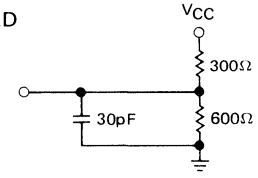
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

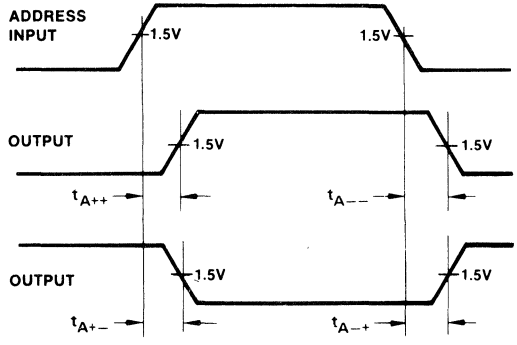
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD

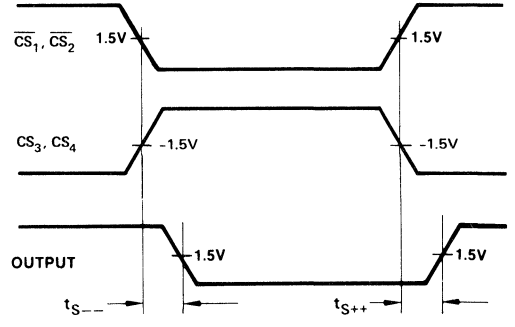


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3605A, 3625A
4K (1K x 4) PROM

3605A-1, 3625A-1	50 ns Max.
3605A, 3625A	60 ns Max.

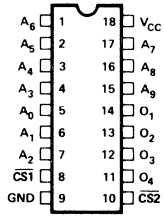
- ± 10% Power Supply Tolerance
- Fast Access Time: 40 ns Typically
- Lower Power Dissipation: 0.14 mW/Bit Typically
- Simple Memory Expansion Two Chip Select Inputs
- Open Collector (3605A) and Three-State (3625A) Outputs
- Polycrystalline Silicon Fuse for Higher Reliability
- Hermetic 18-Pin DIP

The Intel® 3605A and 3625A families are high density, 4096-bit bipolar PROMs organized as 1024 words by 4 bits. The 1024 by 4 organization gives ideal word or bit modularity for memory array expansion. The 3605A has open collector outputs and the 3625A has three-state outputs. The 3605A and 3625A are fully specified over the 0°C to 75°C temperature range with ± 10% power supply variation. Maximum access times of 50 ns (3605A-1/3625A-1) and 60 ns (3605A/3625A) are available at a typical power dissipation of 0.14 mW/bit.

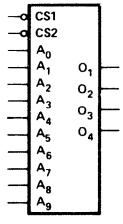
The 3605A/3625A are packaged in an 18-pin dual in-line hermetic package with 300 milli-inch centers. Thus, twice the bit density can be achieved with the 3605A/3625A in the same memory board areas as 512 by 8-bit PROMs in 24-pin packages.

The highly reliable polycrystalline silicon fuse technology is used in the manufacturing of the 3605A and 3625A families. All outputs are initially a logical high and logic low levels can be electrically programmed in selected bit locations.

PIN CONFIGURATION



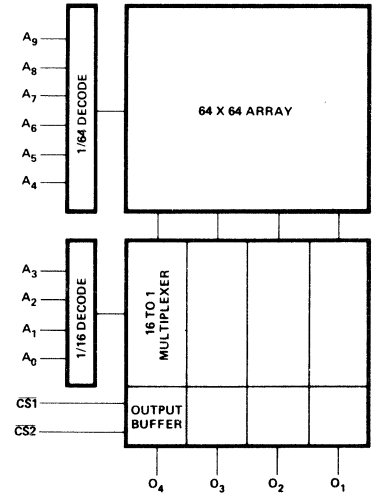
LOGIC SYMBOL



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
$O_1 - O_4$	OUTPUTS

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}=5.5V, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}=5.5V, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC}=5.5V, V_A = 5.5V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC}=5.5V, V_S = 5.5V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.5V, I_A=-10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.5V, I_S=-10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}=4.5V, I_{OL}=15mA
I_{CEX}	3605A Output Leakage Current			40	μA	V_{CC}=5.5V, V_{CE}=5.5V
I_{CC}	Power Supply Current		110	140	mA	V_{CC}=5.5V, $V_{AO}\rightarrow V_{A9}$=0V, $\overline{CS}_1=\overline{CS}_2=V_{IH}$
V_{IL}	Input "Low" Voltage			0.85	V	
V_{IH}	Input "High" Voltage	2.0			V	

3625, 3625-1 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			40	μA	V_O=5.5V or 0.45V, V_{CC}=5.5V, $\overline{CS}_1=\overline{CS}_2$=2.4V
I_{SC}[1]	Output Short Circuit Current	-20	-35	-80	mA	V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -2.4mA, V_{CC} = 4.5V

NOTES: 1. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±10%, T_A = 0°C to +75°C

Symbol	Parameter	Max. Limits 3605A-1 3625A-1	Max. Limits 3605A 3625A	Unit	Conditions
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	50	60	ns	$\overline{CS}_1$=$\overline{CS}_2$=V_{IL} to select the PROM.
t_{S++}	Chip Select to Output Delay	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	ns	

PROM/ROM

Capacitance [1] T_A = 25°C, f = 1 MHz

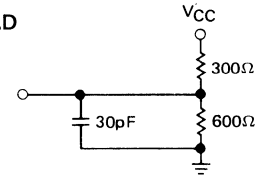
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	3	8	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	4	8	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	5	10	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

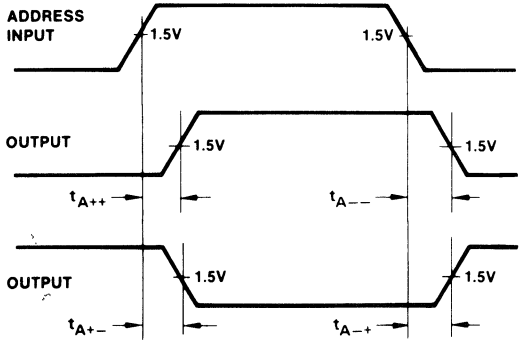
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15mA TEST LOAD

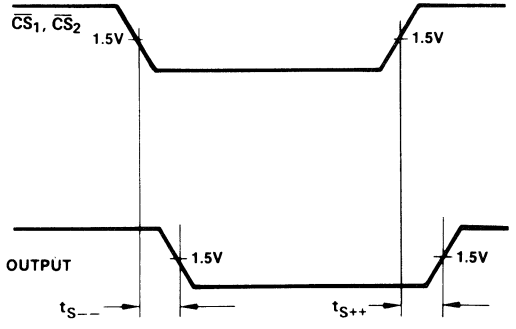


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3628
8K (1K X 8) BIPOLAR PROM

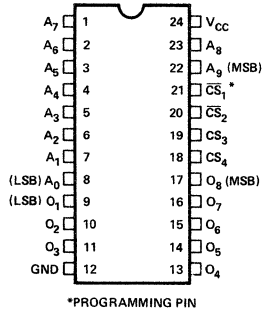
3628	80 ns Max.
3628-4	100 ns Max.

- **Fast Access Time: 65 ns Typically**
- **Low Power Dissipation: 0.09mW/Bit Typically**
- **Four Chip Select Inputs for Easy Memory Expansion**
- **Three-State Outputs**
- **Hermetic 24-Pin DIP**
- **Polycrystalline Silicon Fuses for Higher Fuse Reliability**

The Intel® 3628 is a fully decoded 8192-bit PROM organized as 1024 words by 8 bits. The worst case access time of 80 ns is specified over the 0°C to 75°C temperatue range and 5% V_{CC} power supply tolerances. There are four chip selects provided to facilitate expansion into larger PROM arrays. It uses Schottky clamped TTL technology with poly-crystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

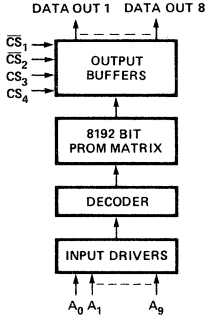
Prior to the 8192 bit 3628, the highest density bipolar PROM available was 4096 bits. The high density of the 3628 now easily doubles the capacity without an increase in area on existing designs currently using 512 words by 8 bit PROMs. There is also little, if any, penalty in power since the 3628 power/bit is approximately one-half that of 4K PROMs. The 3628 is packaged in a hermetic 24-pin dual in-line package.

PIN CONFIGURATION

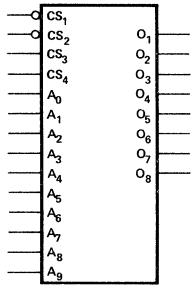


*PROGRAMMING PIN

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A_0 - A_9	ADDRESS INPUTS
$\overline{CS_1}$ - $\overline{CS_2}$, CS_3 - CS_4	CHIP SELECT INPUTS[1]
O_1 - O_8	DATA OUTPUTS

[1] To select the PROM $\overline{CS_1} = \overline{CS_2} = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$

PROGRAMMING

The programming specifications are described in the PROM programming section of the Data Catalog.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS: All Limits Apply for $V_{CC} = +5.0V \pm 5\%$, $T_A = 0°C$ to $+75°C$

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.25V$, $V_A = 0.45V$
I_{FS}	Chip Select Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.25V$, $V_S = 0.45V$
I_{RA}	Address Input Leakage Current			40	μA	$V_{CC} = 5.25V$, $V_A = 5.25V$
I_{RS}	Chip Select Input Leakge Current			40	μA	$V_{CC} = 5.25V$, $V_S = 5.0V$
$\|I_O\|$	Output Leakge for High Impedance State			100	μA	$V_O = 5.25V$ or $0.45V$, $V_{CC} = 5.25V$, $CS_1 = CS_2 = 2.4V$
I_{SC}[2]	Output Short Circuit Current	−20	−25	−80	mA	$V_O = 0V$
V_{CA}	Address Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.75V$, $I_A = -10mA$
V_{CS}	Chip Select Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.75V$, $I_S = -10mA$
V_{OL}	Output Low Voltage		0.3	0.45	V	$V_{CC} = 4.75V$, $I_{OL} = 10mA$
V_{OH}	Output High Voltage	2.4	3.4		V	$I_{OH} = -2.4mA$, $V_{CC} = 4.75V$
I_{CC}	Power Supply Current		150	190	mA	$V_{CC} = 5.25V$, $V_{A0} \rightarrow V_{A9} = 0V$, PROM deselected
V_{IL}	Input "Low" Voltage			0.85	V	$V_{CC} = 5.0V$
V_{IH}	Input "High" Voltage	2.0			V	$V_{CC} = 5.0V$

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2 Unmeasured outputs are open during this test.

A.C. CHARACTERISTICS V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMITS 3628	MAX. LIMITS 3628-4	UNIT	CONDITIONS
t_A	Address to Output Delay	80	100	ns	$\overline{CS}_1 = \overline{CS}_2 = V_{IL}$
t_{EN}	Output Enable Time	40	45	ns	and $CS_3 = CS_4 = V_{IH}$
t_{DIS}	Output Disable Time	40	45	ns	to select the PROM.

CAPACITANCE[1] T_A = 25°C, f = 1 MHz

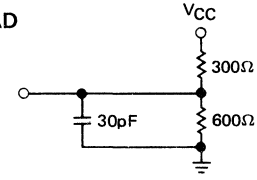
SYMBOL	PARAMETER	TYP. LIMITS TYP.	TYP. LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

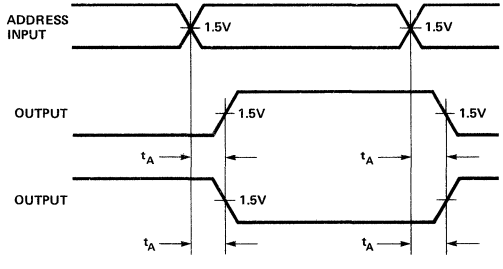
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15mA TEST LOAD

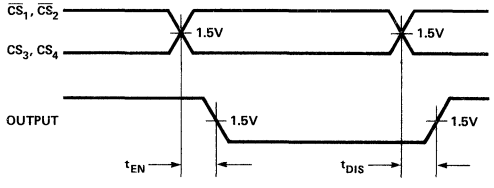


WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



3636
16K (2K x 8) BIPOLAR PROM

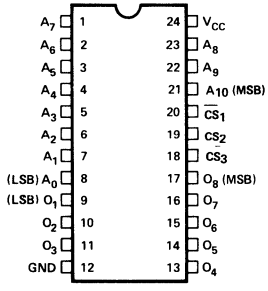
3636-1	65 ns Max.
3636	80 ns Max.

- **Fast Access Time: 50 ns Typically**
- **Low Power Dissipation: 0.05 mW/Bit Typically**
- **Three Chips Select Input for Easy Memory Expansion**
- **Three-State Outputs**
- **Hermetic 24-Pin DIP**
- **Polycrystalline Silicon Fuses for Higher Fuse Reliability**

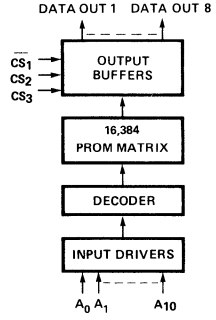
The Intel® 3636 is a fully decoded 16,384 bit PROM organized as 2048 words by 8 bits. The worst case access time of 65 ns is specified over the 0°C to 75°C temperature range and 10% V_{CC} power supply tolerances. There are three chip selects provided to facilitate expansion into larger PROM arrays. The PROMs use the Schottky clamped TTL technology with polycrystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

Prior to the 16,384 bit 3636, the highest density bipolar PROM available was 8192 bits. The high density of the 3636 now easily doubles the capacity without an increase in area on existing designs currently using 1024 by 8 bit PROMs. There is also little, if any, penalty in power since the power/bit is approximately one-half that of 8K PROMs. The 3636 is packaged in a hermetic 24-pin dual in-line package.

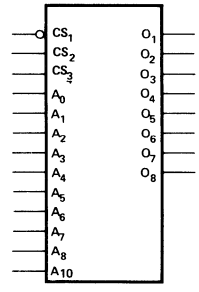
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A_0–A_{10}	ADDRESS INPUTS
$\overline{CS}_1$, CS_2, CS_3	CHIP SELECT INPUTS(1)
O_1–O_8	DATA OUTPUTS

(1) To select the PROM $\overline{CS}_1 = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$

PROGRAMMING

The programming specifications are described in the PROM Programming Section of the Data Catalogue.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS: All Limits Apply for $V_{CC} = +5.0V \pm 10\%$, $T_A = 0°C$ to $+75°C$

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.5V$, $V_A = 0.45V$
I_{FS}	Chip Select Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.5V$, $V_S = 0.45V$
I_{RA}	Address Input Leakage Current			40	μA	$V_{CC} = 5.5V$, $V_A = 5.25V$
I_{RS}	Chip Select Input Leakage Current			40	μA	$V_{CC} = 5.5V$, $V_S = 5.5V$
$\|I_O\|$	Output Leakage for High Impedance State			100	μA	$V_O = 5.5V$ or 0.45V, $V_{CC} = 5.5V$, $CS_1 = 2.4V$
I_{SC}[2]	Output Short Circuit Current	−20	−35	−80	mA	$V_O = 0V$
V_{CA}	Address Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.5V$, $I_A = -10$ mA
V_{CS}	Chip Select Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.5V$, $I_S = -10$ mA
V_{OH}	Output High Voltage	2.4	3.0		V	$I_{OH} = -2.4$ mA, $V_{CC} = 4.5V$
V_{OL}	Output Low Voltage		0.3	0.45	V	$V_{CC} = 4.5V$, $I_{OL} = 10$ mA
I_{CC}	Power Supply Current		150	185	mA	$V_{CC} = 5.5V$
V_{IL}	Input "Low" Voltage			0.85	V	$V_{CC} = 5.0V \pm 10\%$
V_{IH}	Input "High" Voltage	2.0			V	$V_{CC} = 5.0V \pm 10\%$

NOTES: 1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. Unmeasured outputs are open during this test.

A.C. CHARACTERISTICS $V_{CC} = \pm 5V \pm 10\%$, $T_A = 0°C$ to $+75°C$

SYMBOL	PARAMETER	MAX. LIMITS 3636-1	MAX. LIMITS 3636	UNIT	CONDITIONS
t_A	Address to Output Delay	65	80	ns	$\overline{CS_1} = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$ to select the PROM.
t_{EN}	Output Enable Time	40	50	ns	
t_{DIS}	Output Disable Time	40	50	ns	

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

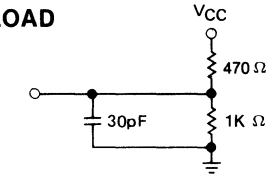
SYMBOL	PARAMETER	TYP. LIMITS TYP.	TYP. LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$ $V_{OUT} = 2.5V$

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

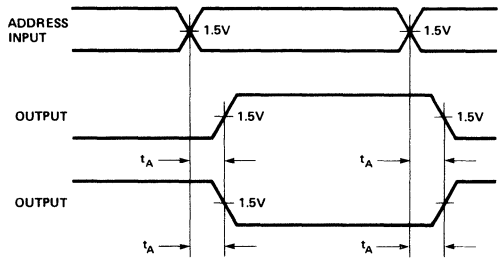
Conditions of Test:
Input pulse amplitudes: 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test: 2.5 MHz

10 mA TEST LOAD

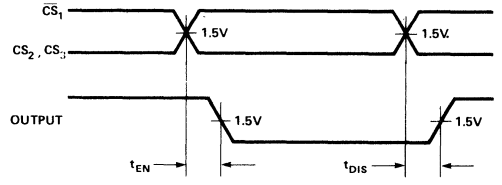


WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



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I. PROM AND ROM INPUT FORMATS

A. Acceptible Formats

Intel can accept programming and masking information for PROMs, EPROMs, or ROMs in the form of floppy disk, punched paper tape, a master device from which to copy, or computer punched cards. The allowable formats are given in Table 1. The preferred formats for the paper tape and computer card input media are the Intel Intellec Hex and BPNF since these formats are defined to allow detection of errors.

It is desirable that two, preferably different, input media for each customer code be sent so Intel can perform a code verification to detect any errors between the two inputs. This procedure, if followed, can avoid errors due to a mispunched tape/card or sending a defective or improper master device.

All orders must be accompanied by a customer PROM/ROM order form. A copy of the form is contained in this section and additional copies are available from Intel Literature Department, 3065 Bowers Ave., Santa Clara, California 95051.

Table I. Acceptable Formats

Floppy Disk	Paper Tape	Computer Card	Master Device
• Intel Microcomputer Development System Single or Double Density Disk	• Intellec Hex • BPNF • Hex	• Intellec Hex • PN	• Same Density and Pin Compatible to Device which is to be Programmed.

A1. Logic Levels

All data field for Intel's EPROMs/PROMs/ROMs are positive logic. The only exceptions are the 4001 and 4308 ROMs which use negative logic. For the 4001/4308, an "0" is a high output and a "1" is a low output. Consequently, because the BPNP format specifies the voltage level at the output of the device, it is necessary to input an "0" and "1" in the 4001/4308 instruction code as a "P" and "N" respectively. However, for the Hex format, the 4001/4308 input should be specified according to the instruction code logic state, i.e., a "1" or "0." The below example shows the corresponding input for 4001 instruction codes. For comparison, the input for an 8080A is also given as an example.

1. 4001 Instruction Code

4001 Instruction Mnemonic	4001 Instruction Code	Intellec Hex Or Non-Intellec Hex Input	BPNF Input
NOP	0000 0000	00	BPPPPPPPPF
WRM	1110 0000	E0	BNNNPPPPPF

2. 8080A Instruction Code

Instruction Mnemonic	Instruction Code	Intellec Hex Or Non-Intellec Hex Input	BPNF Input
JMP	1100 0011	C3	BPPNNNNPPF
Push D	1101 0101	D5	BPPNPNPNPF

B. Paper Tape Format

The paper tape which should be used is 1" wide paper using 7 or 8-bit ASCII code (such as a Model 33 ASR Teletype produces). The three paper tape formats which should be sent are described in Sections B1 through B3.

B1. Intellec Hex Paper Tape Format

In the Intel Intellec Hex Format, a data field can contain either 8 or 4-bit data. *Two* ASCII hexadecimal characters must be used to represent *both* 8 and 4-bit data. In the case of 4-bit data, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form.

Preceding the first data field and following the last data field there must be a leader/trailer length of at least 25 null characters. Comments (except for a colon) may be placed on the tape leader.

The format described below is readily generated by the Intel Intellec Microcomputer Development System or by systems programmed by the user.

1. RECORD MARK FIELD: Frame 0

   The ASCII code for a colon (:) is used to signal the start of a record.

2. RECORD LENGTH FIELD: Frames 1 and 2

   The number of data bytes in the record is representated by two ASCII hexadecimal digits in this field. The high-order digit is in frame 1. The maximum number of data bytes in a record is 255 (FF in hexadecimal). An end-of-file record contains two ASCII zeros in this field.

3. LOAD ADDRESS FIELD: Frames 3–6

   The four ASCII hexadecimal digits in frames 3–6 give the address at which the data is loaded. The high-order digit is in frame 3, the lower-order digit in frame 6. The first data byte is stored in the location indicated by the load address; successive bytes are stored in successive memory locations. This field in an end-of-file record contains zeros or the starting address of the program.

4. RECORD TYPE FIELD: Frames 7 and 8

   The two ASCII hexadecimal digits in this field specify the record type. The high-order digit is in frame 7. All data records are type 0; end-of-file records are type 1. Other possible values for this field are reserved for future expansion.

5. DATA FIELD: Frames 9 to 9+2*(record length)-1

   A data byte is represented by two frames containing the ASCII characters 0–9 or A–F, which represent a hexadecimal value between 0 and FF (0 and 255 decimal). The high-order digit is in the first frame of each pair. If the data is 4-bit, then either the high or low-order digit represents the data and the other digit of the pair may be any ASCII hexadecimal digit. There are no data bytes in an end-of-file record.

6. CHECKSUM FIELD: Frames 9+2*(record length) to 9+2*(record length)+1

The checksum field contains the ASCII hexadecimal representation of the two's complement of the 8-bit sum of the 8-bit bytes that result from converting each pair of ASCII hexadecimal digits to one byte of binary, from the record length field to and including the last byte of the data field. Therefore, the sum of all the ASCII pairs in a record after converting to binary, from the record length field to and including the checksum field, is zero.

Intellec Hex Example:

```
: 10310000311A320E03117E31CD40003A9231B7C2EE
: 1031100060310E00117031CD40003A9231B7C2607B
: 10312000312A7E31227A310E03117E31CD40003AB0
: 103130009231B7C260312A8C317CB5CA50310E044D
: 10314000118831CD40003A9231B7C26031C3273186
: 103150000E01117A31CD40000E09119031CD4000A1
: 103160000E0C119231CD40000E09119031CD40006E
: 0A3170007E31963101000000092311B
: 10317C00923101009631800 08C31923100009631F1
: 04318E0092319231B7
: 02319400923176
: 00310001CE
```

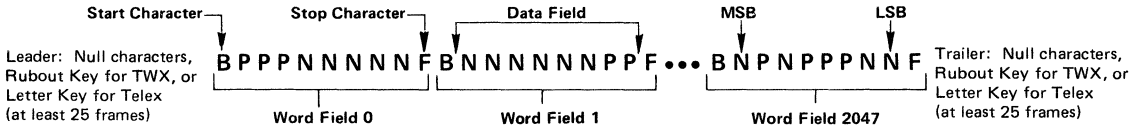

B2. BPNF Paper Tape Format

The format requirements are as follows:

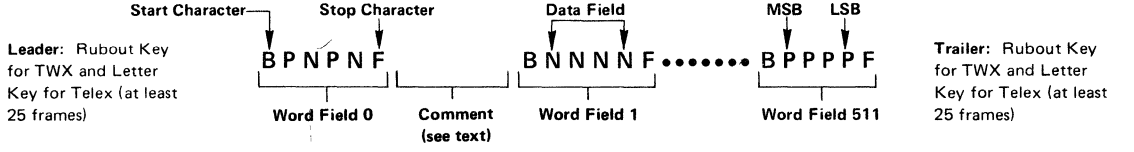
1. All data fields are to be punched in consecutive order, starting with data field 0 (all addresses low). There must be exactly N data fields for a N x 8 or N x 4 device organizations.
2. Each data field must begin with the start character B and end with the stop character F. There must be exactly 8 or 4 data characters between the B and F for a N x 8 or N x 4 organization, respectively.

   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A DATA FIELD. If in preparing a tape an error is made, the entire data field, including the B and F must be rubbed out. *Within the data field, a P results in a high level output, and an N results in a low level output.*
3. Preceding the first data field and following the last data field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes) or null characters.
4. Between data fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") after each 72 characters. When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the device pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

Example of BPNF 2048 x 8 format (N = 2048):



Example of 512 x 4 format (N = 512):



B3. Non-Intellec Hex Paper Tape Format

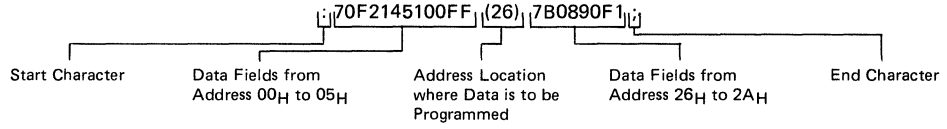
For the non-Intellec Hex Format, a data field can contain either 8 or 4-bit data. *Two* ASCII hexadecimal characters must be used to represent *both* 8 and 4-bit data. In the case of 4-bit data, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form.

Parity is allowed; however, it is not checked. Preceding the first data field and following the last data field there must be a leader/trailer length of at least 25 null characters or rubout punches.

The format requirements are as follows:

1. The start of the first data field is indicated by a colon. After the last data field, a semicolon must be punched to indicate the end. All data fields are to be punched in consecutive order, starting with data field 00_H (all addresses low).
2. *Two* hex characters must be used to represent the data field of both N word x 8-bit and N word x 4-bit devices. For an 8-bit data field, the high order data is represented by the left justified character of the pair. Either character of the pair may be used to represent the word field of a N word x 4-bit device, however, it must be consistent throughout the word field. The other character may be any hex character.

   A field of "don't care" data is allowed. Data after a field of "don't care" will be programmed starting at an address location enclosed in parentheses. In the following example, data is entered in addresses 00_H to 05_H, followed with "don't care" from addresses 06_H to 25_H, data being entered again starting at address location 26_H, and followed with "don't care" data to the last address location.



3. The x character may be used to rubout any erroneous character(s). The # character may be used to rubout an entire line up to the previous carriage return.
4. Spaces are allowed only between *separate* word fields.
5. After each 72 characters, a carriage return followed by a line feed should be punched to allow a print-out of the tape.
6. Comments must be placed only between the tape leader and the start of the first data field.

C. Computer Punched Card Format

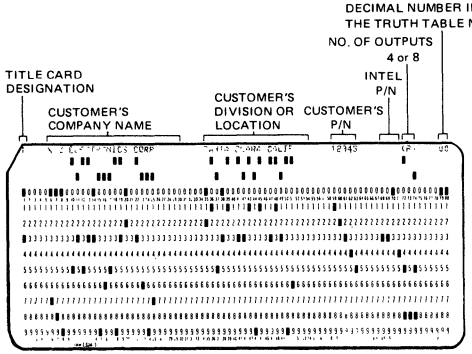
The following general format is applicable to the programming information sent on computer punched cards:

1. An 80 column Hollerith card (interpreted) punched on an IBM 026 or 029 keypunch should be submitted.
2. A single deck must consist of a Title Card followed by the data cards. There will be N/8 or N/14 data cards for N words x 8-bit and N words x 4-bit devices, respectively, in the PN format.

   For the Intellec Hex format, there will be N/32 data cards for both N words x 8-bit and N words x 4-bit devices, and one end of file card.

C1. Intellec Hex Computer Punched Card Format

Two hex characters must be used to represent data for both a N word x 8-bit and N word x 4-bit device. For the latter, only one of the characters is meaningful and must be specified on the Intel PROM/ROM Order Form. The entire data field for all bits must be punched even if it is "don't care".



Column	Data
1	Punch a T
2–3	Blank
4–28	Customer Company Name
29–30	Blank
31–50	Customer's Company Division or location
51–52	Blank
53–61	Customer Part Number
62–63	Blank
64–72	Punch the Intel 4-digit basic part number and in ( ) the number of output bits, e.g., 2708 (8), 2316 (8), or 3605 (4)
73–74	Blank
75–76	Chip number for ROMs with programmable chip select inputs. If not applicable, leave blank.
77–78	Blank
79–80	Punch a 2-digit decimal number to indicate truth table number. The first truth table will be 00, second 01, third 02, etc.

a. N word x 8-bit device

Column	Data
1	Record mark: A colon is used to signal the start of a record.
2–3	Record length: This is the count of the actual data bytes in the record. Column 2 contains the high order digit of the count, Column 3 contains the low order digit. A record length of zero indicates end of file. All frames containing data will have a maximum record length of 10_{HEX} bytes (16 decimal).
4–7	Load address: The four characters starting addresses at which the following data will be loaded. The high order digit of the load address is in Column 4 and the low order digit is in Column 7. The first data byte is stored in the location indicated by the load address. Successive data bytes are stored in successive memory locations. ROMs containing more than 16 bytes of data will use two or more records or cards to transmit the data. Although the load address for the beginning record need not be 0000, each subsequent load address should be "10_H" (16 decimals) greater than the last.
8–9	Record type: A 2-digit code in this field specifies the type of this record. The high order digit of this code is located in Column 8. Currently, all data records are type 0. End-of-file records will be type 1; they are distinguished by a zero RECORD LENGTH field (see above). Other possible values for this field are reserved for future expansion.
10–73	Data
75–75	Checksum: Same as paper tape format.
76–78	Blank
79–80	Punch same 2-digit decimal number as in Title Card.

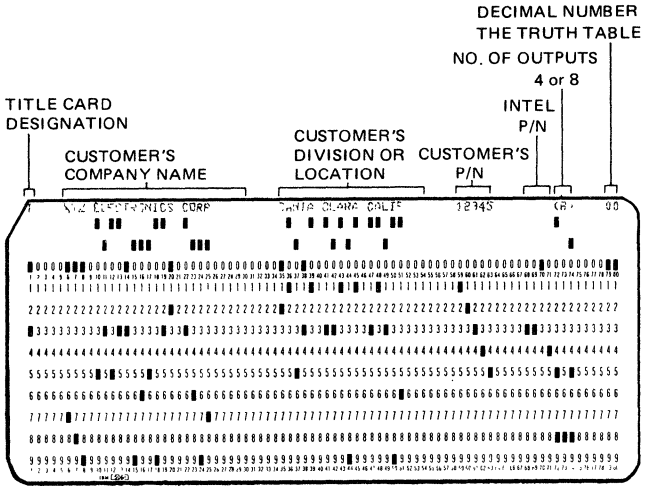
b. N word x 4-bit device

This format is identical to the previously documented 8-bit hexadecimal format with the following exceptions:

Column	Data
10–73	Each memory location is represented by two columns containing the characters 0–9, A–F. Since this is 4-bit data, the user must indicate which character of each pair is to be used as valid data. A single deck must be submitted without mixing first and second characters of the pair.

C2. PN Computer Punched Card Format

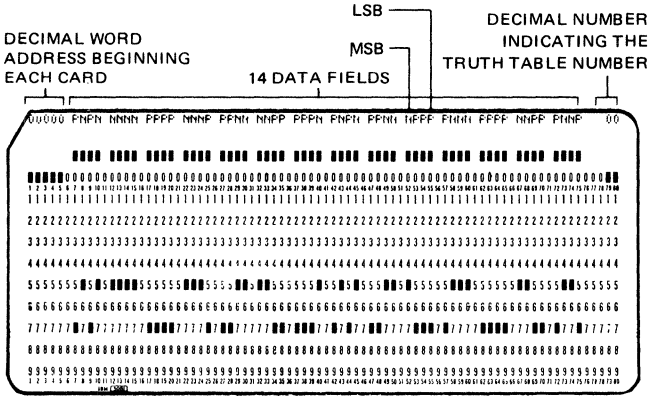
A word field consists of only P's and N's. A punched P will result in an output high level and a punched N in an output low level. The B and F characters, unlike the paper tape format, are illegal characters. The entire data field for all bits must be punched even if it is "don't care". The data field must begin in consecutive order, starting with address 0 (all addresses logically low).



Column	Data
1	Punch a T
2–3	Blank
4–28	Customer Company Name
29–30	Blank
31–50	Customer's Company Division or location
51–52	Blank
53–61	Customer Part Number
62–63	Blank
64–72	Punch the Intel 4-digit basic part number and in ( ) the number of output bits; e.g., 2708 (8), 2316 (8), or 3605 (4)
73–74	Blank
75–76	Chip number for ROMs with programmable chip select inputs. If not applicable, leave blank.
77–78	Blank
79–80	Punch a 2-digit decimal number to indicate truth table number. The first truth table will be 00, second 01, third 02, etc.

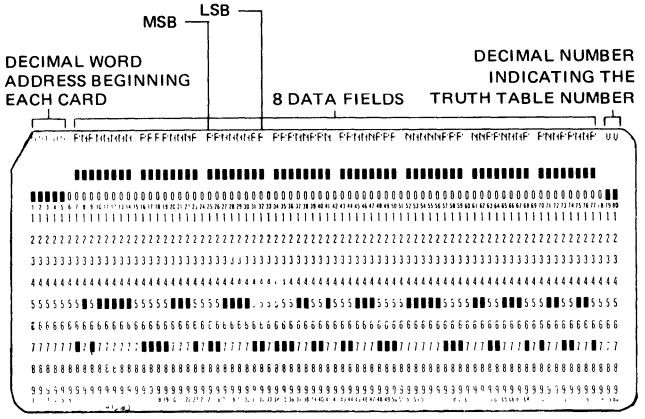
Title Card Format.

For a N words X 4-bit organization only, cards 2 and those following should be punched as shown. Each card specifies the 4-bit output of 14 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØ14, ØØØ28, etc.
6	Blank
7-10	Data Field
11	Blank
12-15	Data Field
16	Blank
17-20	Data Field
21	Blank
22-25	Data Field
26	Blank
27-30	Data Field
31	Blank
32-35	Data Field
36	Blank
37-40	Data Field
41	Blank
42-45	Data Field
46	Blank
47-50	Data Field
51	Blank
52-55	Data Field
56	Blank
57-60	Data Field
61	Blank
62-65	Data Field
66	Blank
67-70	Data Field
71	Blank
72-75	Data Field
76-78	Blank
79-80	Punch same 2 digit decimal number as in title card.

For a N words X 8-bit organization only, cards 2 and those following should be punched as shown. Each card specifies the 8-bit output of 8 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØØ8, ØØØ16, etc.
6	Blank
7-14	Data Field
15	Blank
16-23	Data Field
24	Blank
25-32	Data Field
33	Blank
34-41	Data Field
42	Blank
43-50	Data Field
51	Blank
52-59	Data Field
60	Blank
61-68	Data Field
69	Blank
70-77	Data Field
78	Blank
79-80	Punch same 2 digit decimal number as in title card.

D. Custom PROM/ROM Order Forms

All orders for PROMs/ROMs which are to be electrically or mask programmed at Intel must be submitted with the order forms shown on the following pages. Additional forms are available from Intel Literature Department, 3065 Bowers Ave., Santa Clara, California 95051.

The order forms for the individual PROMs/ROMs are listed in Table II below.

Table II

PROM/ROM Part Number	Order Form Number
MOS EPROMs	A
8741, 8748, 8755	A
2316E, 2616	B
8041, 8048, 8049	C
2608	D
8355	E
Bipolar PROMs	F
4001	G
4308	H
8021	I
8022	J

CUSTOMER EPROM ORDER FORM A

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Intel Device P/N _____

For Intel Use Only

S# _____

STD _____

APP _____

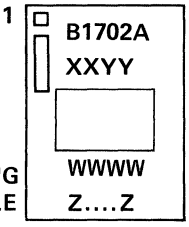
Date _____

All custom MOS EPROM orders must be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel Logo, the product and package type (B1702A), the 4-digit Intel pattern number (WWWW), an internal manufacturing traceability code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.

1702A MARKING EXAMPLE



FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			
19.			

CUSTOMER 16K ROM ORDER FORM B

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Intel P/N & Pkg _____

For Intel Use Only

S# _____

STD _____

APP _____

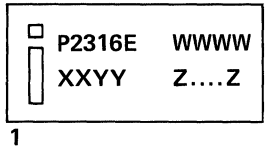
Date _____

A custom 16K ROM order must be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel Logo, the product and package type (P2316E), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.

When authorized by the customer to ship 2616 PROMs against a 2316E order, the PROMs are marked with the dual part number 2616/2316E.



1

P2316E MARKING EXAMPLE

IMPORTANT MASK OPTION SPECIFICATION

The 2316E, 8316A, and 8316AL chip select inputs are mask programmable and must be specified by the user. The chip select logic levels must be specified with one of the below Chip Numbers. The Chip Number will be coded in terms of positive logic where a logic "1" is a high level input. It should be noted that Chip Number 4 for the 2316E is compatible to Intel's 2716 EPROM and 2616 PROM.

Chip Number	CS3	CS2	CS1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	16K ROM Chip Number (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				

CUSTOMER 8041, 8048, 8049 ROM ORDER FORM
C

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Package Type: ☐ Plastic ☐ Cerdip

For Intel Use Only

S# _____

STD _____

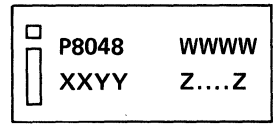
APP _____

Date _____

All custom 8041, 8048 and 8049 orders be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (P8048), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



1

P8048 MARKING EXAMPLE

FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			
19.			
20.			

CUSTOMER 2608 ORDER FORM D

Company _____ Phone #_____

Company Contact _____ Date _____

P.O. #_____ Intel Device P/N _____

For Intel Use Only

S#_____

STD _____

APP _____

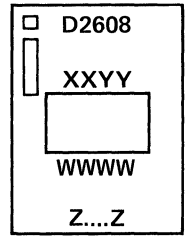
Date _____

All custom 2608 orders must be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

The marking will consist of the Intel Logo, the product and package type (D2608), the 4-digit Intel pattern number (WWWW), an internal manufacturing traceability code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.

MARKING EXAMPLE



FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			
19.			

CUSTOMER 8355 ROM ORDER FORM
E

Company _____ Phone # _____

Company Contact _____ Date _____

P.O. # _____ Package Type: ☐ Plastic ☐ Cerdip

For Intel Use Only

S# _____

STD _____

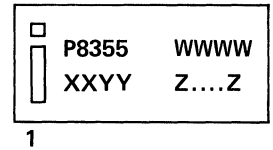
APP _____

Date _____

All custom 8355 orders must be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (P8355), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



1

P8355 MARKING EXAMPLE

FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			
16.			
17.			
18.			
19.			
20.			

CUSTOMER BIPOLAR PROM ORDER FORM F

Company _____ Phone #_____

Company Contact _____ Date_____

P.O. #_____ Intel Device P/N _____

For Intel Use Only

S#_____

STD_____

APP_____

Date _____

All custom bipolar PROM orders must be submitted on this form. Programming information should be sent per the formats described in the Programming Instruction section of the Intel Data Catalog. Additional forms are available from Intel.

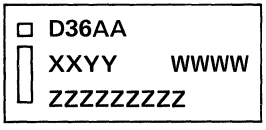
IMPORTANT HEX AND INTELLEC HEX FORMAT INFORMATION

A word field must be 8 bits in the hex format. Consequently for N words by 4-bit devices such as the 3625A, it is important that you indicate by checking the box below whether the submitted tape or card deck for programming is right or left justified.

☐ Right Justified ☐ Left Justified

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (D36AA), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



1
D36AA MARKING EXAMPLE

FLOPPY DISK

Programming information may be sent on Intel Microcomputer Development System Floppy Disk. When using this input medium the floppy disk file name should be indicated in the Customer Part Number Section below. The type of floppy disk sent should also be indicated by checking one of the appropriate boxes:

☐ Single Density ☐ Double Density

CUSTOMER PART NUMBER

	Customer P/N (Please Fill-In)	Floppy Disk File Name (Please Fill-In)	Intel Pattern Number (Please Do Not Use)
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			
11.			
12.			
13.			
14.			
15.			

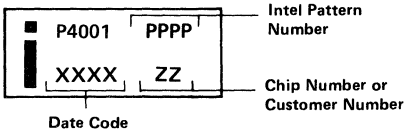
INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, CA 95051 (408) 246-7501

CUSTOMER 4001 ROM ORDER FORM G

All custom ROM orders must be submitted on forms provided by Intel. Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. Refer to MCS-40™ User's Manual for complete pattern specifications. Alternatively, the accompanying truth table may be used. Additional forms are available from Intel.

	(Intel use only)	
Customer _____	S# _____	PPPP _____
P.O. Number _____	STD _____	ZZ _____
	APP _____	DD _____
Date _____	Date _____	

The marking as shown at right must contain the Intel logo, the product type (P4001), the four-digit Intel pattern number (PPPP), a date code (XXXX), and the two-digit chip number (DD). A customer identification number (maximum 6 characters or spaces) may be substituted for the chip number (ZZ).



Customer Identification Number _____

MASK OPTION SPECIFICATIONS

A. **Chip Number (DD)**_____(must be specified – any number from 1 through 15)

B. **I/O Option** – Specify the connection numbers for each I/O pin (see next page). Examples of some of the possible I/O options are shown below:

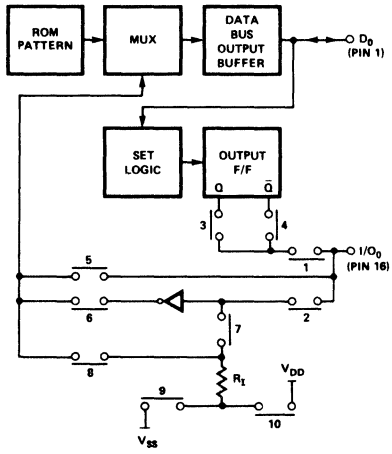
DESIRED OPTION – CONNECTIONS REQUIRED

1. Non-inverting output – 1 and 3 are connected.
2. Inverting output – 1 and 4 are connected.
3. Non-inverting input (no input resistor) – only 5 is connected.
4. Inverting input (input resistor to V_{SS}) – 2, 6, 7, and 9 are connected.
5. Non-inverting input (input resistor to V_{DD}) – 2, 7, 8, and 10 are connected.
6. If inputs and outputs are mixed on the same port, the pins used as the outputs must have the internal resistor connected to either V_{DD} or V_{SS} (8 and 9 or 8 and 10 must be connected). This is necessary for testing purposes. For example, if there are two inverting inputs (with no input resistor) and 2 non-inverting outputs, the connection would be made as follows:
   Inputs – 2 and 6 are connected.
   Outputs – 1, 3, 8, and 9 are connected or 1, 3, 8, and 10 are connected.
   If the pins on a port are all inputs or all outputs the internal resistors do not have to be connected.

C. **4001 Custom ROM Pattern** – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. Refer to Intel's Data Catalog for complete pattern specifications. Alternatively, the accompanying truth table may be used. Based on the particular customer pattern, the characters should be written as a "P" for a high level output = n-logic "0" (negative logic "0") or an "N" for a low level output = n-logic "1" (negative logic "1").

Note that NOP = BPPPP PPPPF = 0000 0000.

4001 I/O Options

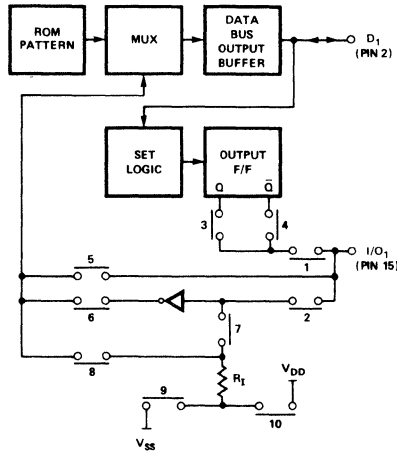


I/O_0 (PIN 16)

CONNECTIONS DESIRED: _____
(List numbers and circle connections on schematic.)

a. For T^2L compatibility on the I/O lines, the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$.

b. If non-inverting input option is used, $V_{IL} = -6.5V$ maximum (not TTL).

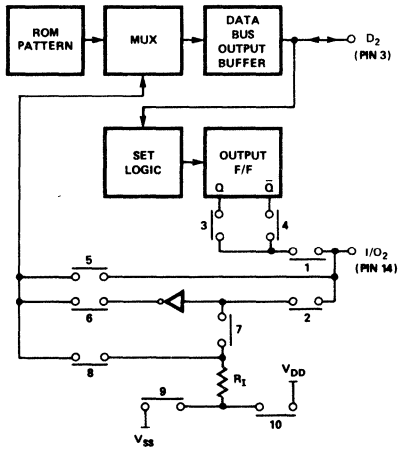


I/O_1 (PIN 15)

CONNECTIONS DESIRED: _____
(List numbers and circle connections on schematic.)

a. For T^2L compatibility on the I/O lines, the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$.

b. If non-inverting input option is used, $V_{IL} = -6.5V$ maximum (not TTL).

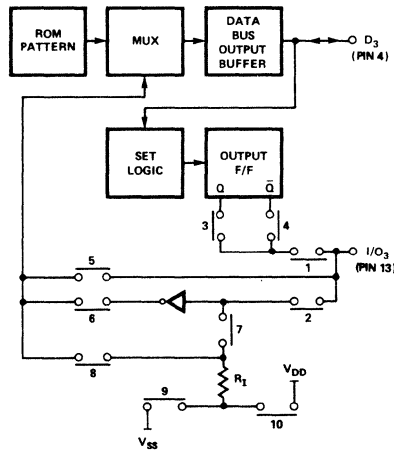


I/O_2 (PIN 14)

CONNECTIONS DESIRED: _____
(List numbers and circle connections on schematic.)

a. For T^2L compatibility on the I/O lines, the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$.

b. If non-inverting input option is used, $V_{IL} = -6.5V$ maximum (not TTL).



I/O_3 (PIN 13)

CONNECTIONS DESIRED: _____
(List numbers and circle connections on schematic.)

a. For T^2L compatibility on the I/O lines, the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$.

b. If non-inverting input option is used, $V_{IL} = -6.5V$ maximum (not TTL).

INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, CA 95051 (408) 246-7501

CUSTOMER 4308 ROM ORDER FORM H

4308 METAL MASKED ROM

All custom ROM orders must be submitted on forms provided by Intel. Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. Refer to the 4308 Data Catalog for complete pattern specifications. Additional forms are available from Intel.

	(Intel use only)	
Customer _____	S # _____	PPPP _____
Address _____	STD _____	ZZ _____
_____	APP _____	DD _____
P.O. Number _____ Date _____	Date _____	

INTEL STANDARD MARKING

The marking as shown at right must contain the Intel logo, the product type (P4308), the four-digit Intel pattern number (PPPP), a date code (XXXX), and the two-digit chip number (DD). A customer identification number (maximum 6 characters or spaces) may be substituted for the chip number (ZZ).

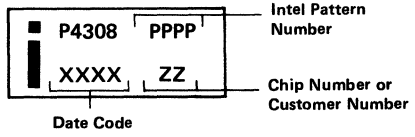
Customer Identification Number _____

ROM DESCRIPTION

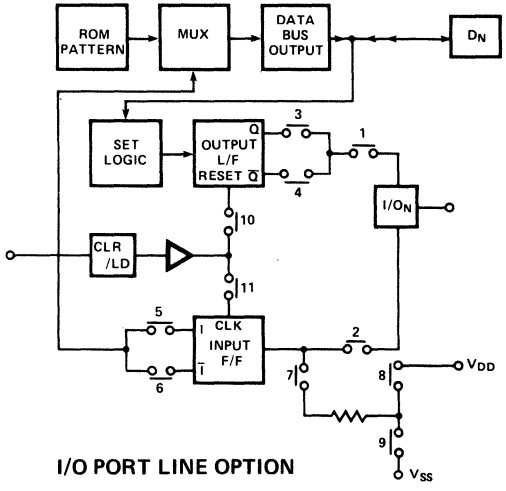
Chip Select Value (0 - 3)_____ (must be specified)

In the table below, select the connections which should be made for each of the 16 I/O port input lines. Avoid the use of illegal options – refer to the MCS-40™ User's Manual.

Mark the appropriate box for an option connection. Leave a blank for a no connection.



PIN		OPTION										
I/O 0_0	27	1	2	3	4	5	6	7	8	9	10	11
I/O 0_1	26	1	2	3	4	5	6	7	8	9	10	11
I/O 0_2	25	1	2	3	4	5	6	7	8	9	10	11
I/O 0_3	24	1	2	3	4	5	6	7	8	9	10	11
I/O 1_0	5	1	2	3	4	5	6	7	8	9	10	11
I/O 1_1	4	1	2	3	4	5	6	7	8	9	10	11
I/O 1_2	3	1	2	3	4	5	6	7	8	9	10	11
I/O 1_3	2	1	2	3	4	5	6	7	8	9	10	11
I/O 2_0	17	1	2	3	4	5	6	7	8	9	10	11
I/O 2_1	16	1	2	3	4	5	6	7	8	9	10	11
I/O 2_2	15	1	2	3	4	5	6	7	8	9	10	11
I/O 2_3	14	1	2	3	4	5	6	7	8	9	10	11
I/O 3_0	21	1	2	3	4	5	6	7	8	9	10	11
I/O 3_1	20	1	2	3	4	5	6	7	8	9	10	11
I/O 3_2	19	1	2	3	4	5	6	7	8	9	10	11
I/O 3_3	18	1	2	3	4	5	6	7	8	9	10	11



I/O PORT LINE OPTION

INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, California 95051 (408) 987-8080

CUSTOMER 8021 ROM ORDER FORM

I

Company _____ Phone No. _____

Company Contact _____ Date _____

P.O. No. _____ Package Type: □ Plastic □ Cerdip

For Intel Use Only

S No. _____

STD _____

APP _____

DATE _____

All custom 8021 orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats described in the Programming Instruction section of the Intel Data Catalog. 8748's may also be used to input programming information for the 8021. Additional forms are available from Intel.

PROM/ROM

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (P8021), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.

P8021 MARKING EXAMPLE

CUSTOMER PART NUMBER

Customer P/N
(Please Fill-In)

Intel Pattern Number
(Please Do Not Use)

I/O Mask Options

Specify the desired connection for each I/O line on Port 0 and for the T1 input by marking only one box for each pin.

PIN		OPTION 1	OPTION 2
P00	4		
P01	5		
P02	6		
P03	7		
P04	8		
P05	9		
P06	10		
P07	11		
T1	13		

Port 0:

Option 1 deletes the pullup resistor on the I/O line providing true open drain outputs.

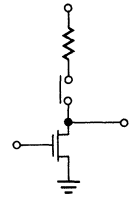
Option 2 includes the pullup resistor on the I/O line providing a quasi-bidirectional line.

T1:

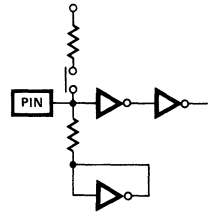
Option 1 deletes the pullup resistor for use as a zero cross detection input.

Option 2 includes the pullup resistor for use with an external switch or standard TTL.

OPTIONAL PULLUP RESISTOR



OPTIONAL PULLUP RESISTOR



INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, California 95051 (408) 987-8080

CUSTOMER 8022 ROM ORDER FORM
J

Company _____ Phone No. _____

Company Contact _____ Date _____

P.O. No. _____ Package Type: ☐ Plastic ☐ Cerdip

For Intel Use Only

S No. _____

STD _____

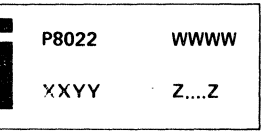
APP _____

DATE _____

All custom 8022 orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats described in the Programming Instruction section of the Intel Data Catalog. 8755's may also used to input programming information for the 8022. Additional forms are available from Intel.

MARKING

All devices will be marked as shown at the right figure. The marking will consist of the Intel Logo, the product and package type (P8022), the 4-digit Intel pattern number (WWWW), a date code (XXYY), and the customer part number (Z....Z). The customer part number is limited to a maximum of 9 digits or spaces.



P8022 MARKING EXAMPLE

CUSTOMER PART NUMBER

Customer P/N
(Please Fill-In)

└┴┴┴┴┴┴┴┴┴┘

Intel Pattern Number
(Please Do Not Use)

└┴┴┴┴┴┴┴┴┴┘

I/O Mask Options

Specify the desired connection for each I/O line on Port 0 and for the T1 input by marking only one box for each pin.

PIN		OPTION 1	OPTION 2
P00	10		
P01	11		
P02	12		
P03	13		
P04	14		
P05	15		
P06	16		
P07	17		
T1	19		

Port 0:

Option 1 deletes the pullup resistor on the I/O line providing true open drain outputs.

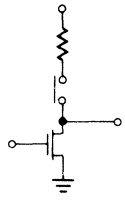
Option 2 includes the pullup resistor on the I/O line providing a quasi-bidirectional line.

T1:

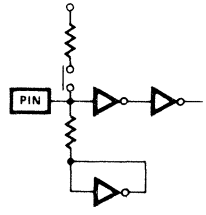
Option 1 deletes the pullup resistor for use as a zero cross detection input.

Option 2 includes the pullup resistor for use with an external switch or standard TTL.

OPTIONAL PULLUP RESISTOR



OPTIONAL PULLUP RESISTOR



II. MOS EPROMs

A. Erasure Procedure

As stated in the EPROM related data sheets, the recommended erasure procedure to use with EPROMs is to illuminate the window with a UV lamp which has a wavelength of 2537 Angstroms (Å). The data sheets specify a distance of 1 inch and erase times of 10–45 minutes, depending on the type of device and UV lamp. Actually, the amount of time required to erase a device can be concisely stated in terms of the amount of UV energy incident to the window, expressed in Watt-seconds per square centimeter (W-sec/cm^2). Table III lists the required integrated dosage (UV intensity X exposure time) for the EPROMs currently in production by Intel.

Table III. Required Erase Energy for Device Types

Device Type	2537Å Erase Energy
1702A/4702A	6 W-sec/cm^2
All other Intel EPROMs or EPROMs with I/O ports	15 W-sec/cm^2

The erase energy expressed in Table III includes a guardband to ensure complete erasure of all bits. *It is not sufficient to monitor "first bit" erasure to determine erasure time, as some other bits in the array may not be erased.*

A1. UV Sources

There are several models of UV lamps that can be used to erase EPROMs (see Table IV). The model numbers in the table refer to lamps manufactured by Ultra Violet Products of San Gabriel, California. In addition, there are several other manufacturers, including Data I/O (Issaquah, Wash.), PROLOG (Monterey, Calif.). Prometrics (Chicago, Ill.), and Turner Designs (Mt. View, Calif.). The individual manufacturers should be consulted for detailed product descriptions. Also shown in the table are typical erase times for various combinations of Intel PROMs and lamp intensities.

Table IV.

Model	Power Rating	Minimum Erase Time for Indicated Dosage Without a Filter Over the Bulb	
		6 W-sec 1702A, 4702A	15 W-sec All Intel EPROMs or EPROMs with I/O Ports Except the 1702A/4702A
R-52	13000 μW/cm^2	7.7 min	19.2 min
S-52	12000 μW/cm^2	8.3 min	20.7 min
S-68	12000 μW/cm^2	8.3 min	20.7 min
UVS-54	5700 μW/cm^2	17.5 min	43.8 min
UVS-11	5500 μW/cm^2	18.2 min	45.6 min

According to the manufacturers, the output of the UV lamp bulbs decrease with age. The output of the lamp should be verified periodically to ensure that adequate intensities are maintained. If this is not done, bits may be partially erased which will interfere with later programming and/or operation at high temperature.

For lamps other than those listed, the erase time can be determined by using a UV intensity meter, such as the Ultra Violet Products Model J-225. When a meter is used, the intensity should be measured at the same position (distance from the lamp) as the EPROMs to be erased. This will require careful positioning to insure that the sensor will receive the same amount of UV light that the window of the EPROM will receive.

The sensors used with most UV intensity meters show reduced output with constant exposure to UV light. Therefore, they should not be permanently placed inside the erasure enclosure, they should only be used for periodic measurements.

B. 1702A/1702AL Family Programming

The 1702A/1702AL is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity X exposure time) is 6 W-sec/cm^2. An example of an ultraviolet source which can erase the 1702A/1702AL in 10 to 20 minutes is the Model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the PROM should be placed within 1 inch away from the lamp tubes.

Initially, all 2048 bits of the PROM are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode. All 8 address bits must be in the binary complement state when pulsed V_{CC} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25 μsec after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10 μsec before the program pulse is applied. The addresses should be programmed in the sequence 0 through 255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the 8 bits of each word. A low data input level (–48V) will program a "1" and a high data input level (ground) will leave a "0". All 8 bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals. See page 4-12 for required pin connections during programming.

1702A, 1702AL

D.C. and Operating Characteristics for Programming Operation

T_A = 25°C, V_{CC} = 0V, V_{BB} = + 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI1P}	Address and Data Input Load Current			10	mA	V_{IN} = -48V
I_{LI2P}	Program and V_{GG} Load Current			10	mA	V_{IN} = -48V
I_{BB}[1]	V_{BB} Supply Load Current		10		mA	
I_{DDP}[2]	Peak I_{DD} Supply Load Current		200		mA	V_{DD} = V_{PROG} = -48V, V_{GG} = -35V
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	-46		-48	V	
V_{IL2P}	Address Input Low Voltage	-40		-48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	-46		-48	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	-35		-40	V	

Notes: 1. The V_{BB} supply must be limited to 100mA max. current to prevent damage to the device.
2. I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μsec. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.

1702A, 1702AL
A.C. Characteristics for Programming Operation

$T_{AMBIENT}$ = 25°C, V_{CC} = 0V, V_{BB} = + 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

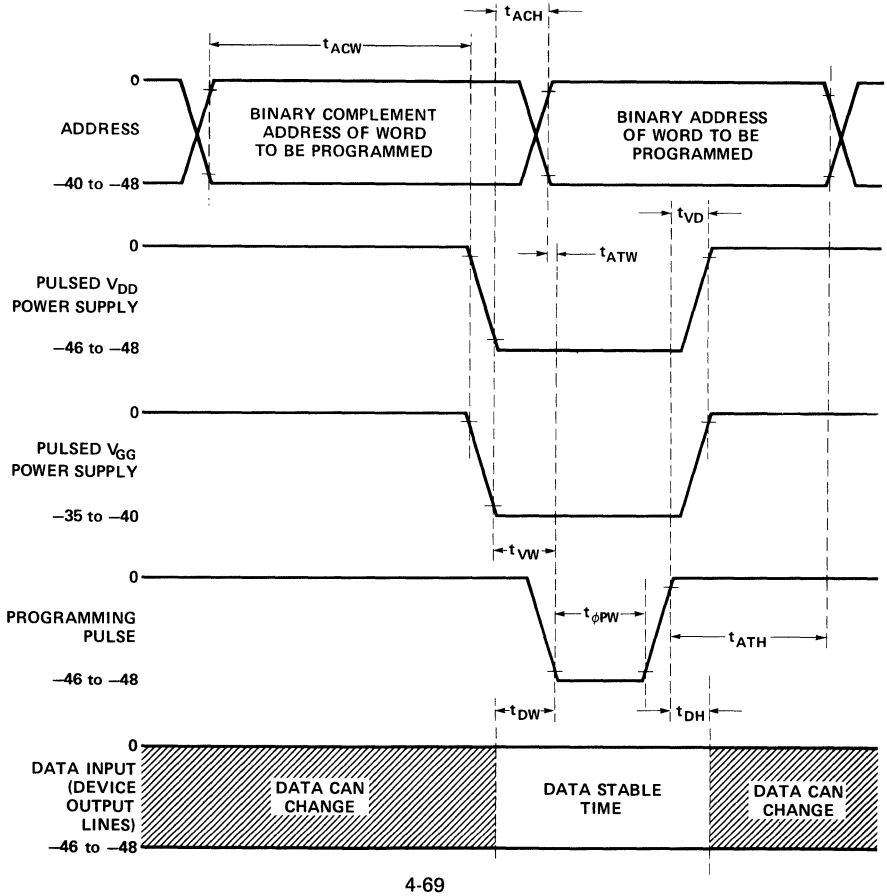
Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
	Duty Cycle (V_{DD}, V_{GG})			20	%	
$t_{\phi PW}$	Program Pulse Width		2	3	ms	V_{GG} = -35V, V_{DD} = V_{PROG} = -48V
t_{DW}	Data Set-Up Time	25			μs	
t_{DH}	Data Hold Time	10			μs	
t_{VW}	V_{DD}, V_{GG} Set-Up	100			μs	
t_{VD}	V_{DD}, V_{GG} Hold	10		100	μs	
t_{ACW}	Address Complement Set-Up	25			μs	
t_{ACH}	Address Complement Hold	25			μs	
t_{ATW}	Address True Set-Up	10			μs	
t_{ATH}	Address True Hold	10			μs	

PROGRAM WAVEFORMS

Conditions of Test:

Input pulse rise and fall times ≤ 1μsec

$\overline{CS}$ = 0V



C. 2708/2704 Family Programming

Initially, and after each erasure, all 8192/4096 bits of the 2708/2704 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the CS/WE input (pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8 bits in parallel, to the data output lines (O_1–O_8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to N x t_{PW} $\geqslant$ 100 ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops throuhg all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The CS/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{ILL}) when CS/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Examples (Using N x t_{PW} $\geqslant$ 100 ms)

Example 1: All 8096 bits are to be programmed with a 0.5 ms program pulse width.

The minimum number of program loops is 200. One program loop consists of words 0 to 1023.

Example 2: Words 0 to 100 and 500 to 600 are to be programmed. All other bits are "don't care". The program pulse width is 0.75 ms.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's.

Example 3: Same requirements as example 2, but the PROM is now to be *updated* to include data for words 750 to 770.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's. Addresses 0 to 100 and 500 to 600 must be re-programmed with their original data pattern.

2704, 2708 Family
PROGRAM CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

D.C. Programming Characteristics

Symbol	Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Address and CS/WE Input Sink Current				10	μA	V_{IN} = 5.25V
I_{IPL}	Program Pulse Source Current				3	mA	
I_{IPH}	Program Pulse Sink Current				20	mA	
I_{DD}	V_{DD} Supply Current	2708, 2704		50	65	mA	Worst Case Supply Currents[1]: All Inputs High CS/WE = 5V; T_A = 0°C
		2708L		21	28	mA	
I_{CC}	V_{CC} Supply Current	2708, 2704		6	10	mA	
		2708L		2	4	mA	
I_{BB}	V_{BB} Supply Current	2708, 2704		30	45	mA	
		2708L		10	14	mA	
V_{IL}	Input Low Level (except Program)		V_{SS}		0.65	V	
V_{IH}	Input High Level For all Addresses and Data	2708, 2704	3.0		V_{CC} + 1	V	
		2708L	2.2		V_{CC} + 1	V	
V_{IHW}	CS/WE Input High Level		11.4		12.6	V	Referenced to V_{SS}
V_{IHP}	Program Pulse High Level		25		27	V	Referenced to V_{SS}
V_{ILP}	Program Pulse Low Level		V_{SS}		1	V	$V_{IHP} - V_{ILP}$ 25V min.

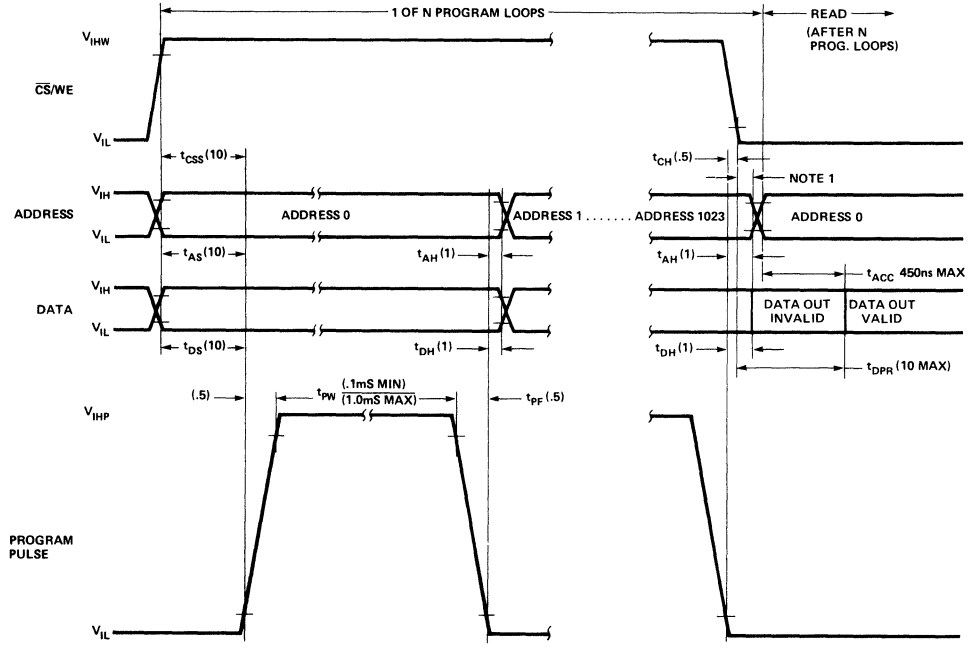
Note 1. I_{BB} for the 2708L is specified in the programmed state and is 18 mA maximum in the unprogrammed state.

A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	$\overline{CS}$/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	$\overline{CS}$/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	.5		2.0	μs

NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

2704, 2708 Family
Programming Waveforms



NOTE 1. THE $\overline{CS}$/WE TRANSITION MUST OCCUR AFTER THE PROGRAM PULSE TRANSITION AND BEFORE THE ADDRESS TRANSITION.

NOTE 2. NUMBERS IN ( ) INDICATE MINIMUM TIMING IN μS UNLESS OTHERWISE SPECIFIED.

D. 2716 And 2758 Programming

Initally, and after each erasure, all bits of the 2716/2758 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 2716/2758 is programmed by applying a 50 ms, TTL programming pulse to the $\overline{CE}$/PGM pin with the $\overline{OE}$ input high and the V_{PP} supply at 25V ±1V. Any location may be programmed at any time — either individually, sequentially, or randomly. The programming time for a single bit is only 50 ms and for all bits is approximately 100 and 50 seconds for the 2716 and 2758 respectively. The detailed programming specifications and timing waveforms are given in the following tables and figures.

CAUTION: The V_{CC} and V_{PP} supplied must be sequenced on and off such that V_{CC} is applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} to prevent damage to the 2716/2758. The maximum allowable voltage during programming which may be applied to the V_{PP} with respect to ground is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding the 26-volt maximum specification. For convenience in programming, the 2716/2758 may be verified with the V_{PP} supply at 25V ±1V. During normal read operation, however, V_{PP} must be at V_{CC}.

2716 AND 2758 PROGRAM CHARACTERISTICS(1)

T_A = 25°C ±5°C, V_{CC}[2] = 5V ±5%, V_{PP}[2,3] = 25V ±1V

D.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Current (for Any Input)			10	μA	V_{IN} = 5.25V/0.45
I_{PP1}	V_{PP} Supply Current			5	mA	$\overline{CE}$/PGM = V_{IL}
I_{PP2}	V_{PP} Supply Current During Programming Pulse			30	mA	$\overline{CE}$/PGM = V_{IH}
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	-0.1		0.8	V	
V_{IH}	Input High Level	2.0		V_{CC}+1	V	

A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	$\overline{OE}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Output Enable to Output Float Delay	0		120	ns	$\overline{CE}$/PGM = V_{IL}
t_{OE}	Output Enable to Output Delay			120	ns	$\overline{CE}$/PGM = V_{IL}
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTES:
1. Intel's standard product warranty applies only to devices programmed to specifications described herein.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The 2716/2758 must not be inserted into or removed from a board with V_{PP} at 25 ±1V to prevent damage to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

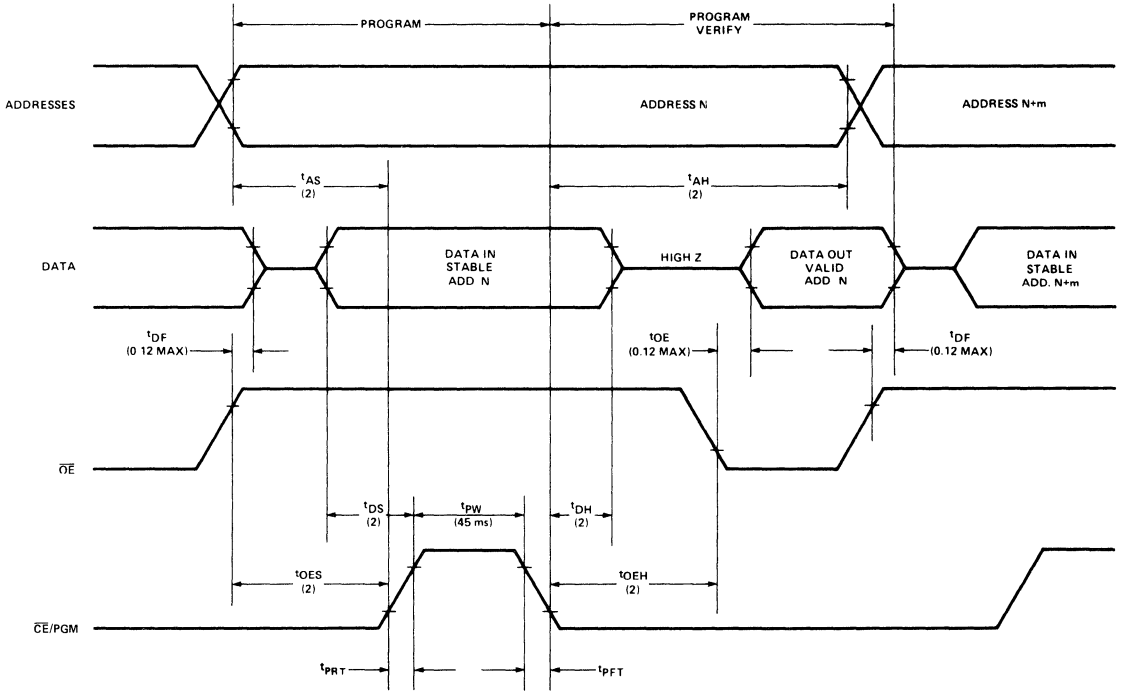
A.C. Conditions of Test:

V_{CC} ..... 5V ± 5%
V_{PP} ..... 25V ± 1V
Input Rise and Fall Times (10% to 90%) ..... 20 ns

Input Pulse Levels ..... 0.8V to 2.2V
Input Timing Reference Level ..... 1V and 2V
Output Timing Reference Level ..... 0.8V and 2V

PROGRAMMING WAVEFORMS

V_{PP} = 25V ±1V, V_{CC} = 5V ±5%



NOTE ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE μSEC UNLESS OTHERWISE NOTED

E. 2732 Programming

Initially, and after each erasure, all bits of the 2732 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2732 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732s.

Program Inhibit

Programming of multiple 2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2732s may be common. A TTL level program pulse applied to a 2732's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25V will program that 2732. A high level $\overline{CE}$ input inhibits the other 2732s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%).....20 ns
Input Pulse Levels.....0.8V to 2.2V
Input Timing Reference Level.....1V and 2V
Output Timing Reference Level.....0.8V and 2V

PROGRAMMING[1]

D.C. PROGRAMMING CHARACTERISTICS: $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$

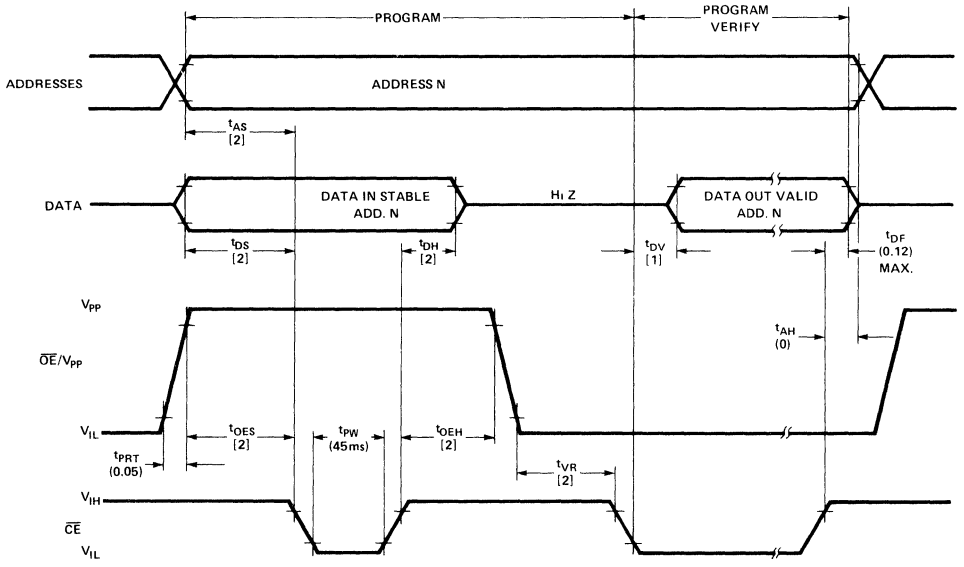
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_{LI}	Input Current (All Inputs)			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{OL}	Output Low Voltage During Verify			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4			V	$I_{OH} = -400$ μA
I_{CC}	V_{CC} Supply Current		85	150	mA	
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level (All Inputs Except OE/V_{PP})	2.0		$V_{CC}+1$	V	
I_{PP}	V_{PP} Supply Current			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$

A.C. PROGRAMMING CHARACTERISTICS: $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{OEH}	OE Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Chip Enable to Output Float Delay	0		120	ns	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$
t_{PW}	$\overline{CE}$ Pulse Width During Programming	45	50	55	ms	
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming	50			ns	
t_{VR}	V_{PP} Recovery Time	2			μs	

Note: 1. When programming the 2732, a 0.1 μF capacitor is required across OE/V_{PP} and ground to suppress spurious voltage transients which may damage the device.

PROGRAMMING WAVEFORMS



1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 1V FOR A V_{IL} AND 2V FOR A V_{IH}.

III. BIPOLAR PROM PROGRAMMING

All Intel bipolar PROMs are programmed with the algorithm described below. This algorithm was developed specifically to program Intel PROMs and must be used to insure properly and reliably programmed fuses.

Initially, all bits are in a logic 1 (high) state. To program a bit to a logic 0 (low) state, it is necessary to force 5 mA into the output to be programmed. A series of program pulses must also be applied to the V_{CC} power supply and to any one of the logically low true chip select ($\overline{CS}$) inputs. The logic level of the other chip selects, in the case of PROMs with multiple chip selects, should be such that the PROM is selected during verification.

Program pulses are applied to all outputs of a word in a cycle time. The program pulses are multiplexed during a cycle time to each output of the word to be programmed. If desired, a N word by 8-bit PROM may have its words programmed in two separate groups – the four lower order bits (O_1 to O_4) and the four higher order bits (O_5 to O_8). The operation in this manner is the same as for a N word by 4-bit PROM. For fastest programming time, it is preferred that all eight outputs be programmed at the same time.

The programming specifications are given in Table V and the programming waveforms are shown in Figure 1. The programming procedure (described with nominal specifications) is as follows:

1. A 5 mA current must be forced into the output to be programmed by a current source. The current source must be clamped to V_{CC} by a silicon diode. All the other outputs must be floating until it is their turn for programming. The V_{CC} power supply and the chip select ($\overline{CS}$) input is pulsed as shown in Figures 1 and 2. The width of V_{CC} is linearly increased from 0.2 μs to 8 μs according to the ramp time shown in Figure 3. The total ramp time for a group of four outputs is 180 ms and 360 ms for a group of eight outputs.

   The V_{CC} program pulses are multiplexed during a cycle time to the outputs of the word to be programmed. The cycle time (t_{CYC}) between the V_{CC} program pulses to the same output will increase as the V_{CC} program pulse width increases from 0.2 μs to 8 μs. The time (t_D) between V_{CC} pulses of two different outputs is constant at 1.8 μs.
2. All outputs must be continuously monitored for programming verification. This verification must occur after V_{CC} has been at 4.5V for 90% of t_D and prior to V_{CC} rising to 12.5V. The program/verification cycles must still be applied (with the pulse width still linearly increasing to a maximum of 8 μs) even though the output has been sensed as being programmed. An additional 128 verifications (i.e., 128 program/verify cycles) on each output must be obtained to insure a correctly programmed output. This additional 128 verification is a minimum number and must occur *after* all the bits of the word are sensed as being programmed. Please refer to Figure 1 for the timing waveforms.

   More than 128 program/verify cycles may be required to achieve the 128 verifications on each bit. The cycles should still continue even if one bit fails, since the verifications are not required to be in consecutive sequence. After the 128 verifications have occurred for all bits, a final V_{CC} and CS pulse at a width of 2.5 ms is simultaneously applied to all outputs. Programming should cease if the 128 verifications are not achieved in 800 ms.
3. A 4 mA ±50% I_{CS} current must also be forced into an appropriate chip select. I_{CS} is forced into CS_4 (pin 18) of 3604A/3624A, CS_2 (pin 10) of 3605A/3625A, CS_3 (pin 19) of 3608/3628, and CS_2 (pin 19) of 3636. The 4 mA current into the chip select input may be easily accomplished by using a 1.2K resistor connected to a +15V power supply. The voltage on the chip select input will be approximately 10V with the 1.2K resistor.
4. The 4 mA current into the chip select input may be easily accomplished by using a 1.2K resistor connected to a +15V power supply. The voltage on the chip select input will be approximately 10V with the 1.2K resistor.

Table V. Programming Characteristics

$T_A = 25°C$

Symbol	Parameter	Limits Min.	Nom.	Max.	Units	Conditions
V_{IH1}	V_{CC} Program Pulse Amplitude	12	12.5	13	V	
V_{IH2}	$\overline{CS}$ Program Pulse Amplitude	3	5	5.5	V	
V_{IL1}	V_{CC} During Verify	4.25[1]	4.5	4.75	V	
V_{IH2}	$\overline{CS}$ During Verify	0	0.2	0.4	V	
t_{PW1}	V_{CC} Pulse Width at Beginning of Pulse Train	160	200	240	ns	Measured at 12V
t_{PW2}	V_{CC} Pulse Width at End of Pulse Train	7.2	8	8.8	μs	Measured at 12V
T_{CSS}	Chip Select Setup Time	0			ns	Measured from 1.5V on rising edge of $\overline{CS}$ to 5.0V on rising edge of V_{CC}
T_{CSH}	Chip Select Hold Time	100			ns	Measured from 5.0V on falling edge of V_{CC} to 1.5V on falling edge of $\overline{CS}$
T_R	V_{CC} Rise Time	300	400	500	ns	Measured from 5V to 12V on V_{CC}
T_F	V_{CC} Fall Time	50	100	200	ns	Measured from 12V to 5V on V_{CC}
T_{CYC}	Time Between Pulses to Same Output	9	10		μs	Measured at 5V on V_{CC}
T_{OP}	DC Program Time After Verification Has Been Obtained	2.2	2.5	2.8	ms	Measured at 12V
T_D	Time Between V_{CC} Pulses to Successive Outputs	1.5	1.8		μs	Measured at 5V on V_{CC}
T_{RAMP}	Time During Which V_{CC} Pulse Width is Increased Linearly from t_{PW1} to t_{PW2} — 4 outputs	160	180	200	ms	
	8 outputs	320	360	400		
I_{CS}	Chip Select Input Current (See Programming Instruction 3 for Details)	2	4	6	mA	I_{CS} should be generated using a 1.2K resistor from a 15V power supply

NOTE: 1. The minimum V_{IL1} for the 3604AL (low power) is 4.5V.

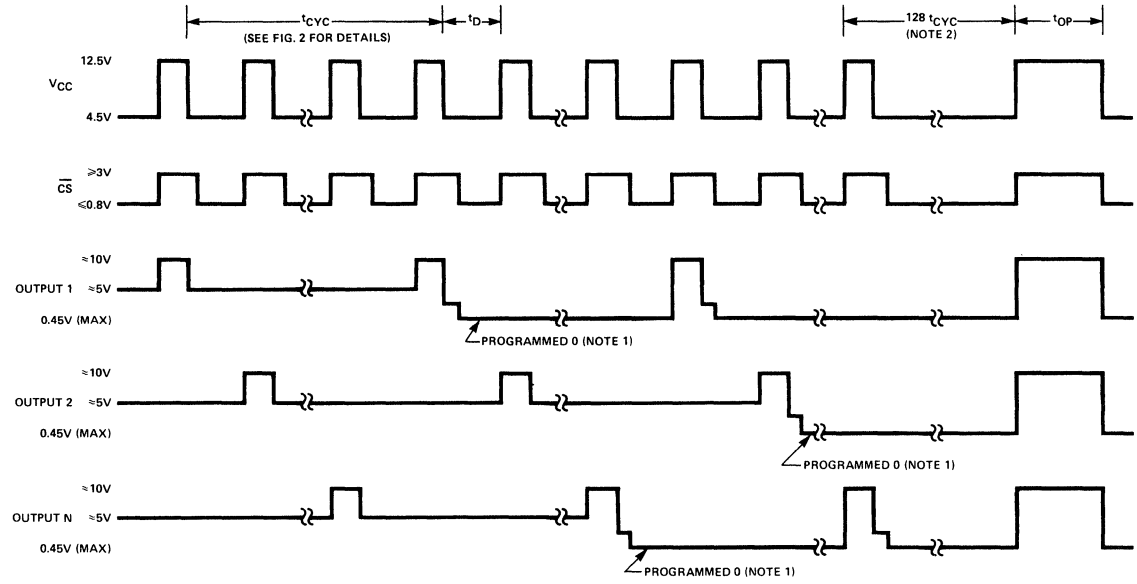


Figure 1. Programming Cycles.

NOTES: 1. PROGRAM VERIFICATION MUST OCCUR AFTER V_{CC} HAS BEEN AT 4.5V FOR 90% OF t_D AND PRIOR TO V_{CC} RISING TO 12.5V. THE PROGRAMMED OUTPUT IS ≤0.45V WHEN $\overline{CS}$ ≤0.8V AND FLOATING WHEN $\overline{CS}$ ≥ 3V.

2. AFTER THE LAST BIT HAS BEEN PROGRAMMED, 128 ADDITIONAL VERIFICATIONS ARE REQUIRED FOR EACH OUTPUT TO BE CORRECTLY PROGRAMMED.

3. AFTER THE 128 PROGRAM VERIFICATIONS, A FINAL 2.5 ms V_{CC} AND $\overline{CS}$ PULSE SHOULD BE APPLIED WHILE SIMULTANEOUSLY ENABLING THE CURRENT SOURCES TO ALL OUTPUTS WHICH ARE TO BE PROGRAMMED.

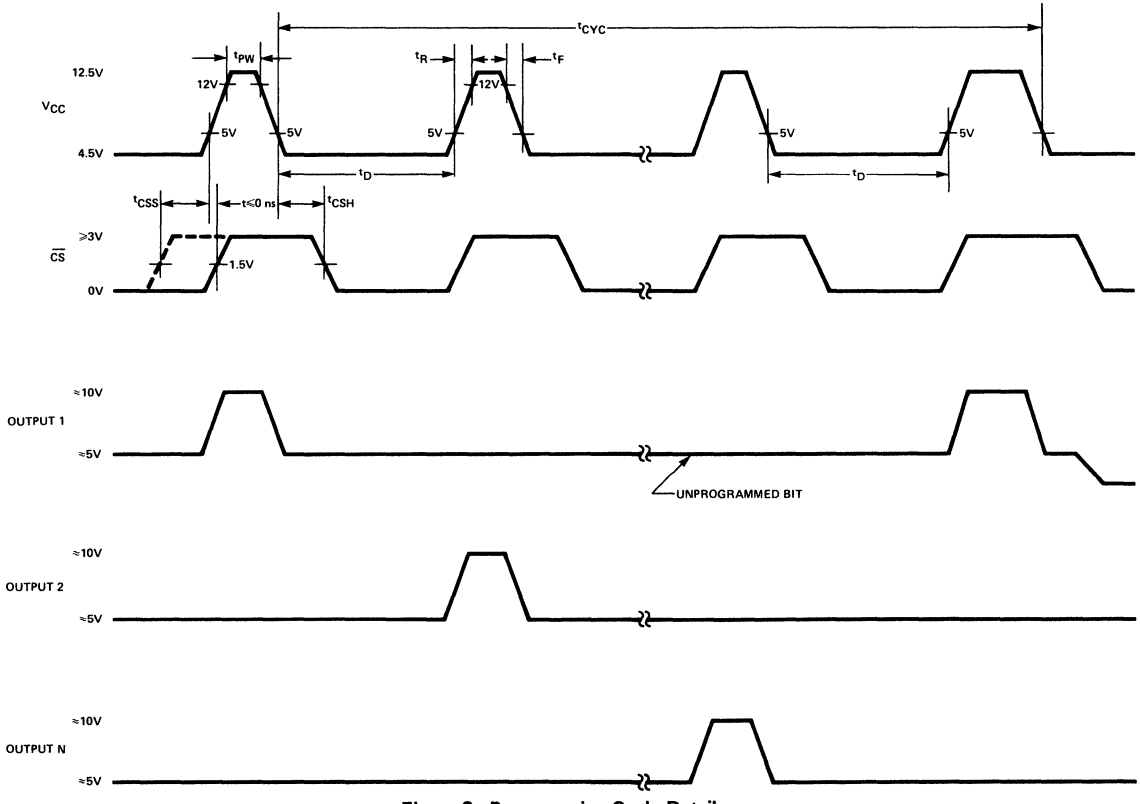


Figure 2. Programming Cycle Details.

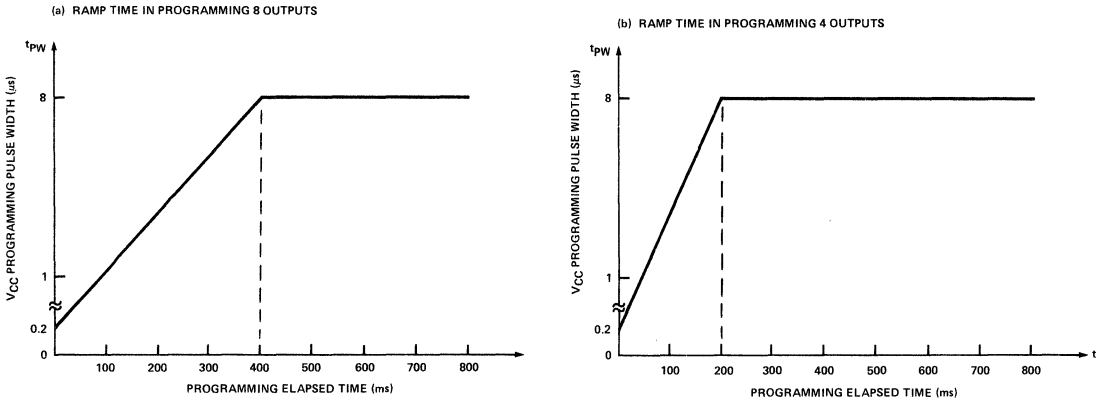
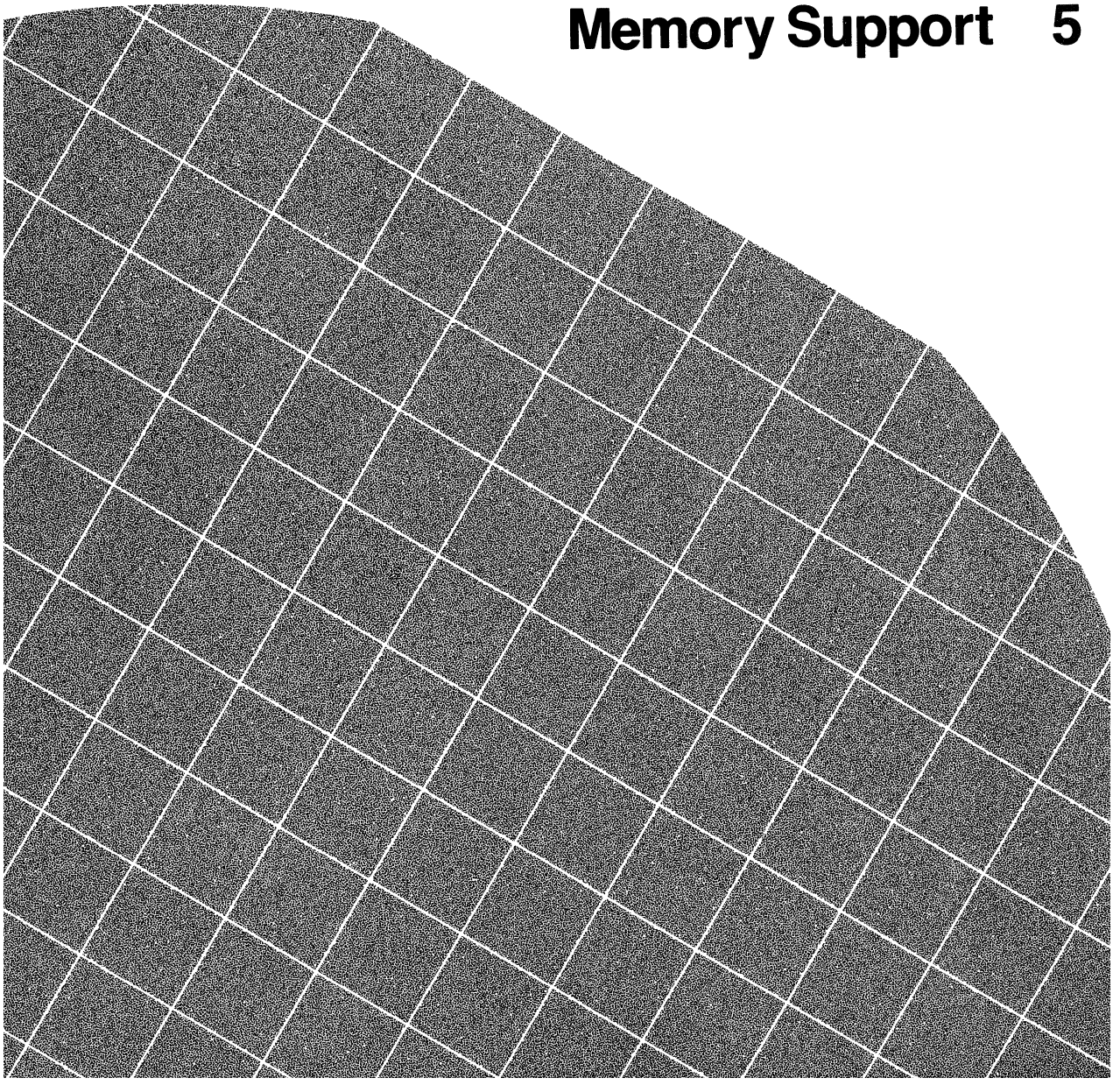


Figure 3. V_{CC} Pulse Width vs. Programming Time.

Memory Support 5



MEMORY SUPPORT CIRCUITS

Type	Description	No. of Pins	Electrical Characteristics Over Temperature		Supplies, V	Page No.
			Input to Output Delay Max.	Power Dissipation[1] Maximum		
3205	1 of 8 Binary Decoder	16	18 ns	350 mW	+5	5-3
3207A	Quad Bipolar to MOS Level Shifter and Driver	16	25 ns	900 mW	+5, +16, +19	5-7
3207A-1	Quad Bipolar to MOS Level Shifter and Driver	16	25 ns	1040 mW	+5, +19, +22	5-11
3222	4K Dynamic RAM Refresh Controller	22	—	600 mW	+5	5-13
3232	4K Dynamic RAM Address Multiplexer and Refresh Counter	24	20 ns	750 mW	+5	5-19
3242	16K Dynamic RAM Address Multiplexer and Refresh Counter	28	20 ns	825 mW	+5	5-23
3245	Quad TTL to MOS Driver for 4K RAMs	16	32 ns	388 mW	+12, +5	5-27
3404	High Speed 6-Bit Latch	16	12 ns	375 mW	+5	5-3

Note 1. Power Dissipation calculated with maximum power supply current and nominal supply voltages.

3205, 3404
3205 HIGH SPEED 1 OUT OF 8 BINARY DECODER
3404 HIGH SPEED 6-BIT LATCH

- **18ns Max. Delay Over 0°C to 75°C Temperature: 3205**
- **12ns Max. Data to Output Delay Over 0°C to 75°C Temperature: 3404**
- **Directly Compatible With DTL and TTL Logic Circuits**
- **Totem-Pole Output**
- **Low Input Load Current: .25mA Max., 1/6 Standard TTL input Load**
- **Minimum Line Reflection: Low Voltage Diode Input Clamp**
- **Outputs Sink 10mA Min.**
- **16-Pin Dual In-Line Package**
- **Simple Expansion: Enable Inputs**

MEMORY SUPPORT

3205

The 3205 decoder can be used for expansion of systems which utilize memory components with active low chip select input. When the 3205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 3205 allow easy memory expansion. For very large memory systems, 3205 decoders can be cascaded such that each decoder can drive 8 other decoders for arbitrary memory expansions.

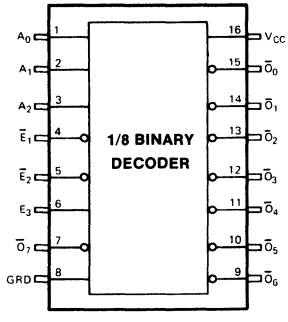
3404

The Intel 3404 contains six high speed latches organized as independent 4-bit and 2-bit latches. They are designed for use as memory data registers, address registers, or other storage elements. The latches act as high speed inverters when the "Write" input is "low".

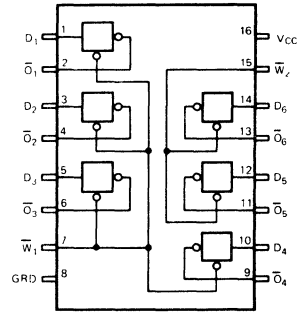
The Intel 3404 is packaged in a standard 16-pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION

3205



3404



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		125 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

3205, 3404

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT		−0.25	mA	V_{CC} = 5.25V, V_F = 0.45V
I_R	INPUT LEAKAGE CURRENT		10	µA	V_{CC} = 5.25V, V_R = 5.25V
V_C	INPUT FORWARD CLAMP VOLTAGE		−1.0	V	V_{CC} = 4.75V, I_C = −5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} = 4.75V, I_{OL} = 10.0 mA
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	V_{CC} = 4.75V, I_{OH} = −1.5 mA
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} = 5.0V
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	−40	−120	mA	V_{CC} = 5.0V, V_{OUT} = 0V
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	V_{CC} = 5.0V, I_{OX} = 40 mA

3205 ONLY

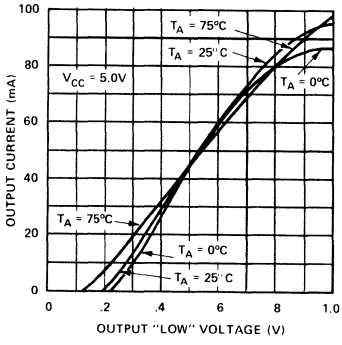
I_{CC}	POWER SUPPLY CURRENT		70	mA	V_{CC} = 5.25V, Outputs Open

3404 ONLY

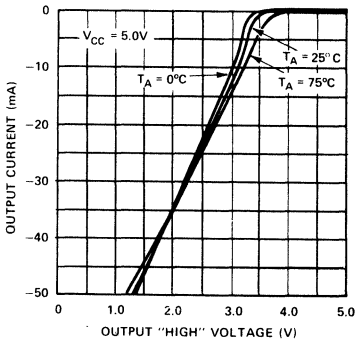
I_{CC}	POWER SUPPLY CURRENT		75	mA	V_{CC} = 5.25V, Outputs Open
I_{FW1}	WRITE ENABLE LOAD CURRENT PIN 7		−1.00	mA	V_{CC}=5.25V, V_W=0.45V
I_{FW2}	WRITE ENABLE LOAD CURRENT PIN 15		−0.50	mA	V_{CC}=5.25V, V_W=0.45V
I_{RW}	WRITE ENABLE LEAKAGE CURRENT		10	µA	V_R=5.25V

TYPICAL CHARACTERISTICS

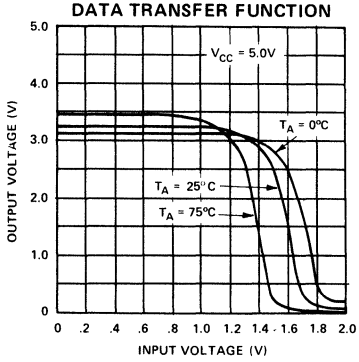
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



DATA TRANSFER FUNCTION



3205 HIGH SPEED 1 OUT OF 8 BINARY DECODER

SWITCHING CHARACTERISTICS

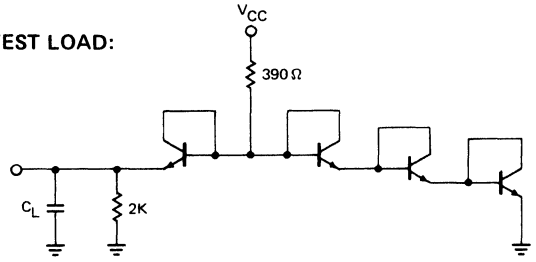
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

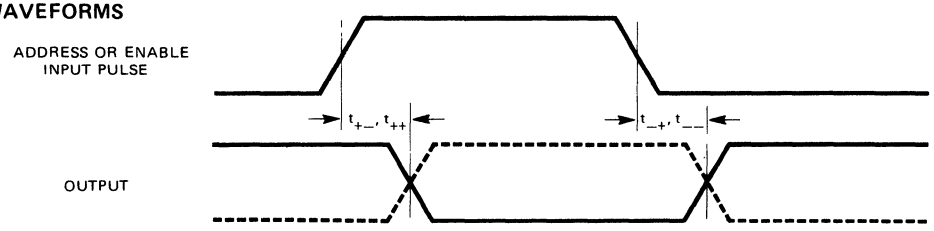
Measurements are made at 1.5V

TEST LOAD:



All Transistors 2N2369 or Equivalent. C_L = 30 pF

TEST WAVEFORMS



A.C. CHARACTERISTICS

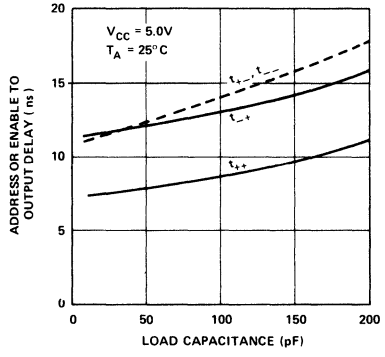
T_A = 0°C to +75°C, V_{CC} = 5.0V ±5% unless otherwise specified.

SYMBOL	PARAMETER		MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY		18	ns	
t_{-+}			18	ns	
t_{+-}			18	ns	
t_{--}			18	ns	
C_{IN} (1)	INPUT CAPACITANCE	P3205	4(typ.)	pF	f = 1 MHz, V_{CC} = 0V
		C3205	5(typ.)	pF	V_{BIAS} = 2.0V, T_A = 25°C

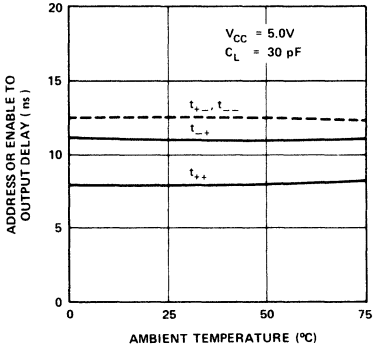
1. This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

ADDRESS OR ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



3404 6-BIT LATCH

SWITCHING CHARACTERISTICS

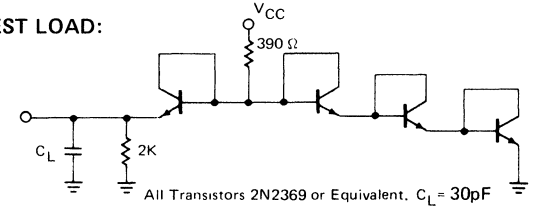
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

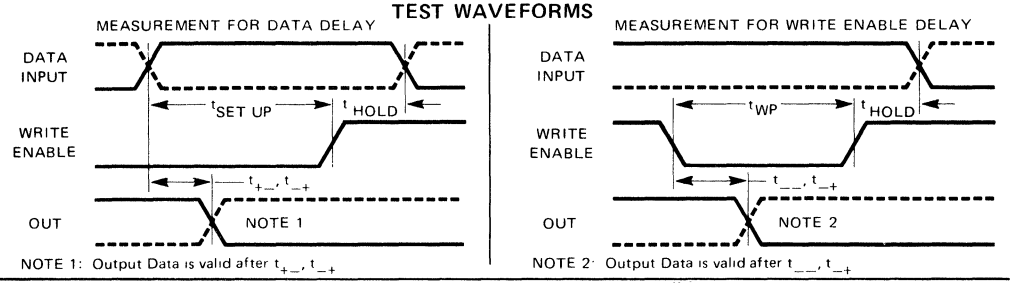
Input rise and fall times: 5 nsec between 1V and 2V

Measurements are made at 1.5V

TEST LOAD:



TEST WAVEFORMS



NOTE 1: Output Data is valid after t_{+-}, t_{-+}

NOTE 2: Output Data is valid after t_{--}, t_{-+}

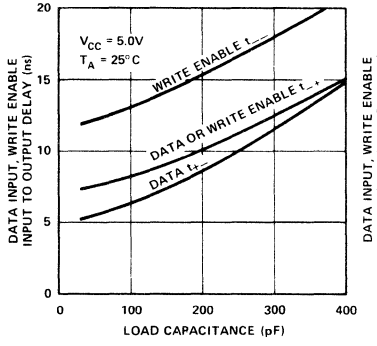
A.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%; unless otherwise specified.

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
t_{+-},t_{-+}	DATA TO OUTPUT DELAY				12	ns	
t_{--},t_{-+}	WRITE ENABLE TO OUTPUT DELAY				17	ns	
$t_{SET\ UP}$	TIME DATA MUST BE PRESENT BEFORE RISING EDGE OF WRITE ENABLE		12			ns	
t_{HOLD}	TIME DATA MUST REMAIN AFTER RISING EDGE OF WRITE ENABLE		8			ns	
t_{WP}	WRITE ENABLE PULSE WIDTH		15			ns	
C_{IND}(3)	DATA INPUT CAPACITANCE	P3404		4		pF	f = 1 MHz, V_{CC} = 0V
		C3404		5		pF	V_{BIAS} = 2.0V, T_A = 25°C
C_{INW}(3)	WRITE ENABLE CAPACITANCE	P3404		7		pF	f = 1 MHz, V_{CC} = 0V
		C3404		8		pF	V_{BIAS} = 2.0V, T_A = 25°C

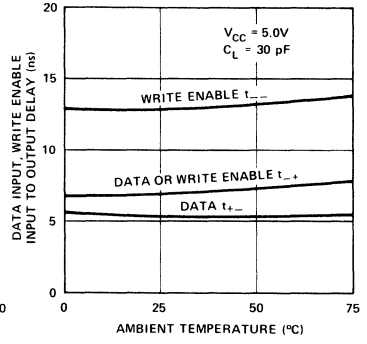
NOTE 3: This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

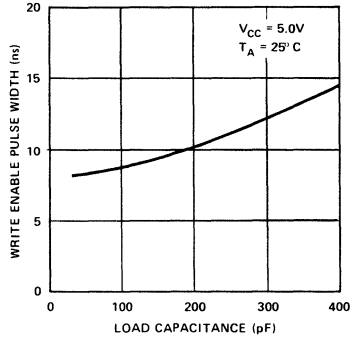
DATA INPUT, WRITE ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA INPUT, WRITE ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



WRITE ENABLE PULSE WIDTH VS. LOAD CAPACITANCE



3207A
QUAD BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER

- **High Speed, 45 nsec Max. — Delay + Transition Time Over Temperature with 200 pF Load**
- **TTL and DTL Compatible Inputs**
- **1103 and 1103A Memory Compatible at Output**
- **Simplifies Design — Replaces Discrete Components**
- **Easy to Use — Operates from Standard Bipolar and MOS Supplies**
- **Minimum Line Reflection — Input and Output Clamp Diodes**
- **High Input Breakdown Voltage — 19 Volts**
- **CerDIP Package — 16 Pin DIP**

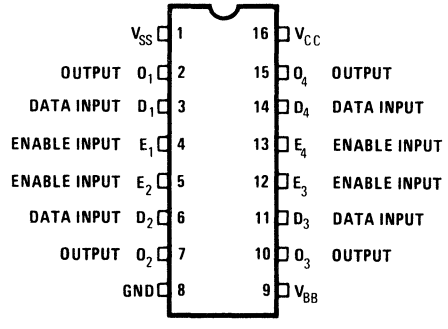
The 3207A is a Quad Bipolar-to-MOS level shifter and driver which accepts TTL and DTL input signals, and provides high output current and voltage suitable for driving MOS circuits. It is particularly suitable for driving the 1103 and 1103A memory chips. The circuit operates from a 5 volt TTL power supply, and V_{SS} and V_{BB} power supplies from the 1103 and 1103A.

The device features two common enable inputs per pair of devices which permits some logic to be done at their inputs, such as cenable and precharge decoding for the 1103 and 1103A.

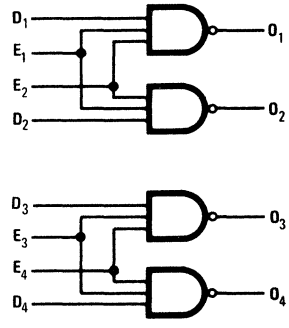
For the TTL inputs a logic "1" is V_{IH} and a logic "0" is V_{IL}. The 3207A outputs correspond to a logic "1" as V_{OL} and a logic "0" as V_{OH} for driving MOS inputs.

The 3207A is packaged in a hermetically sealed 16 pin ceramic dual-in-line package. The device performance is specified over the same temperature range as the 1103 and 1103A, i.e. from 0°C to +70°C.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature..... −65°C to +160°C
All Input Voltages and V_{SS}..... −1.0 to +21V
Supply Voltage V_{CC} ..... −1.0 to +7V
All Outputs and Supply Voltage
V_{BB} with respect to GND ..... −1.0 to +25V
Power Dissipation at 25°C..... 2 Watts (1)

*COMMENT
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) Refer to the graph of Junction Temperature versus Total Power Dissipation on page 5-10 for other temperatures.

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 16V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	$V_D = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{FE}	ENABLE INPUT LOAD CURRENT		−0.50	mA	$V_E = .45V$, $V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{RD}	DATA INPUT LEAKAGE CURRENT		20	μA	$V_D = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 16V$, $V_{BB} = 19V$
I_{RE}	ENABLE INPUT LEAKAGE CURRENT		20	μA	$V_E = 19V$, $V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 16V$, $V_{BB} = 19V$
V_{OL}	OUTPUT "LOW" VOLTAGE		.8 .7 .6	V(0°C) V(25°C) V(70°C)	$I_{OL} = 500\mu A$, $V_{CC} = 4.75V$ $V_{SS} = 16V$, $V_{BB} = 19V$ All Inputs at 2.0V
V_{OH} (MIN.)	OUTPUT "HIGH" VOLTAGE	$V_{SS} - .7$ $V_{SS} - .6$ $V_{SS} - .5$		V(0°C) V(25°C) V(70°C)	$I_{OH} = -500\mu A$, $V_{CC} = 5.0V$ $V_{SS} = 16V$, $V_{BB} = 19V$ All Inputs at 0.85V
V_{OH} (MAX.)			$V_{SS} + 1.0$	V	$I_{OH} = 5mA$, $V_{CC} = 5.0V$ $V_{SS} = 16V$, $V_{BB} = 19V$
I_{OL}	OUTPUT SINK CURRENT	100		mA	$V_O = 4V$, $V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$, $V_E = V_D = 2.0V$
I_{OH}	OUTPUT SOURCE CURRENT	−100		mA	$V_O = V_{SS} - 4V$, $V_{CC} = 5.0V$, $V_{SS} = 16V$ $V_{BB} = 19V$, $V_E = V_D = 0.85V$
V_{IL}	INPUT "LOW" VOLTAGE		1.0	V	$V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0V$, $V_{SS} = 16V$, $V_{BB} = 19V$
C_{IN}	INPUT CAPACITANCE	8(Typical)		pF	$V_{BIAS} = 2.0V$, $V_{CC} = 0V$

POWER SUPPLY CURRENT DRAIN:

All Outputs "Low"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		83	mA	$V_{CC} = 5.25V$, $V_{SS} = 16.8V$, $V_{BB} = 20.8V$ All Inputs Open
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		21	mA	
P_{TOTAL}	Total Power Dissipation		900	mW	

All Outputs "High"

I_{CC}	Current from V_{CC}		33	mA	$V_{CC} = 5.25V$, $V_{SS} = 16.8V$, $V_{BB} = 20.8V$ All Inputs Grounded
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		3	mA	
P_{TOTAL}	Total Power Dissipation		250	mW	

Standby Condition with $V_{CC} = 0V$, $V_{SS} = V_{BB}$

I_{CC}	Current from V_{CC}		0	mA	$V_{CC} = 0V$, $V_{SS} = 16.8V$, $V_{BB} = 16.8V$
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		250	μA	
P_{TOTAL}	Total Power Dissipation		10	mW	

SWITCHING CHARACTERISTICS

A.C. CHARACTERISTICS

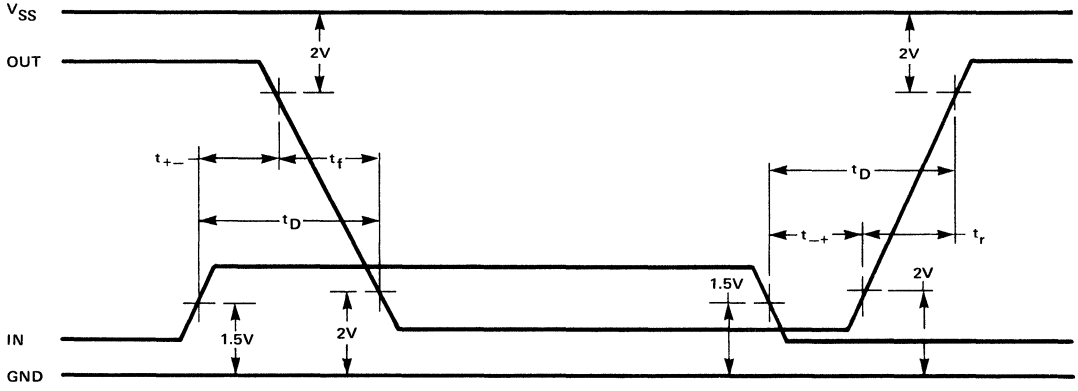
T_A = 0°C to 70°C, V_{CC} = 5V ±5%, V_{SS} = 16V ±5%, V_{BB} = V_{SS} +3 to 4V, f = 2 MHz, 50% Duty Cycle

SYMBOL	TEST	LIMITS (ns)				
		C_L = 100 pF		C_L = 200 pF		DELAY DIFFERENTIAL (1) C_L = 200 pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	20	10	30	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

(1) This is defined as the maximum skew between any output in the same package, eg., all the input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

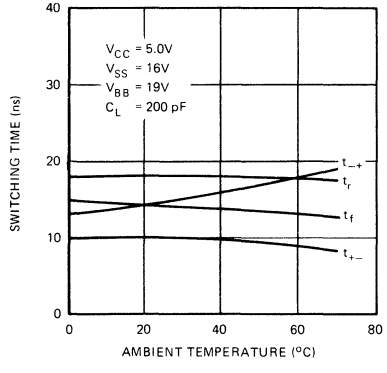
MEMORY SUPPORT

WAVEFORMS

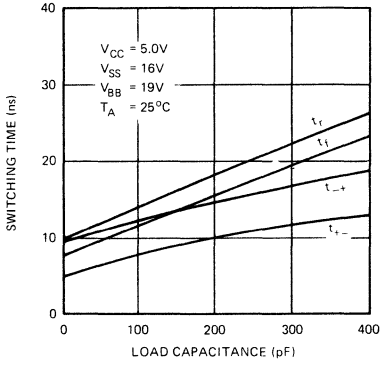


TYPICAL CHARACTERISTICS

SWITCHING TIME VS. AMBIENT TEMPERATURE

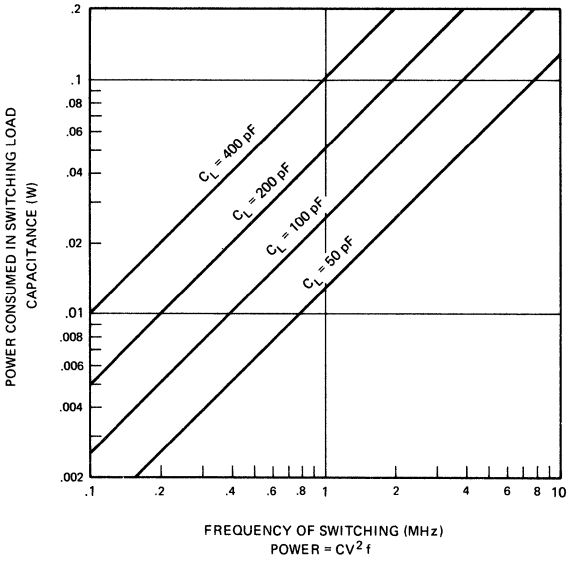


SWITCHING TIME VS. LOAD CAPACITANCE

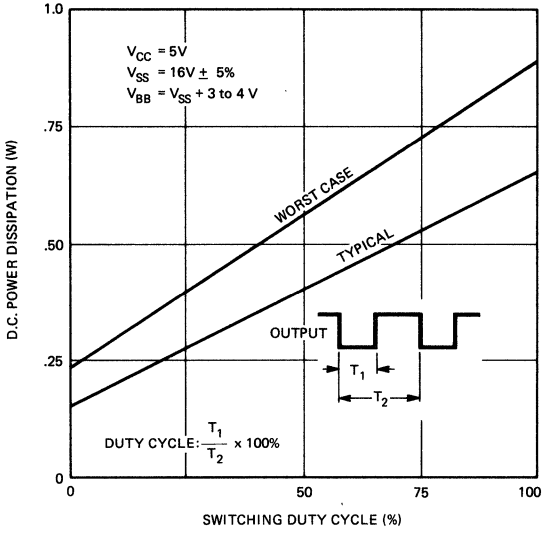


POWER AND SWITCHING CHARACTERISTICS

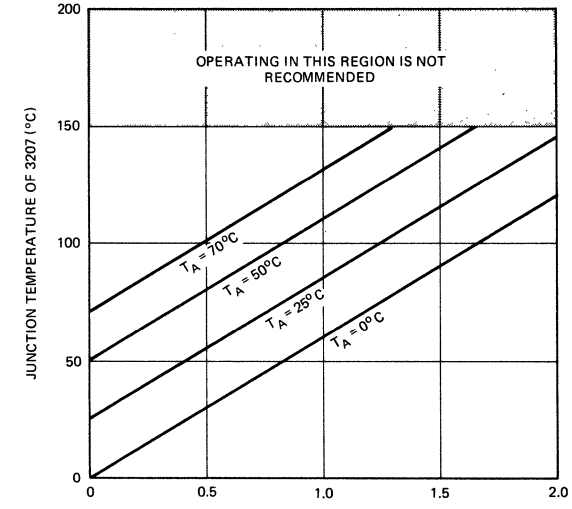
POWER CONSUMED IN CHARGING AND DISCHARGING LOAD CAPACITANCE OVER 0V TO 16V INTERVAL



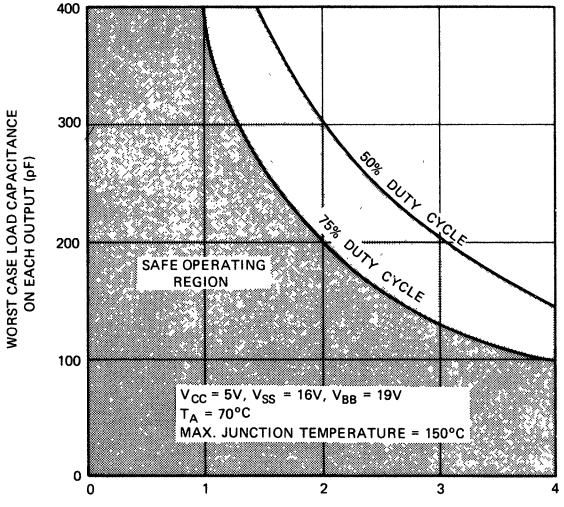
NO LOAD D.C. POWER DISSIPATION VS. OPERATING DUTY CYCLE



JUNCTION TEMPERATURE VS. TOTAL POWER DISSIPATION OF THE CIRCUIT



WORST CASELOAD CAPACITANCE ON EACH OUTPUT VS. FREQUENCY OF SWITCHING

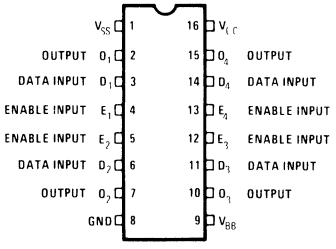


3207A-1
QUAD BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER

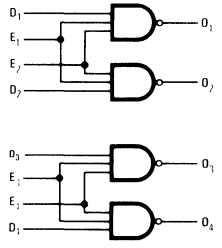
- **Power Supply Voltage Compatible with the High Voltage 1103-1**
- **1103-1 Memory Compatible at Output**

The Intel 3207A-1 is the high voltage version of the standard 3207A, and is compatible with the 1103-1. The 3207A-1 has all the same features as the standard 3207A. The absolute maximum ratings and pin configuration are repeated below for convenience, while the DC and AC characteristics appear below and on the next page.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to +55°C
Storage Temperature . . . . . −65° C to +160°C
All Input Voltages . . . . . −1.0 to +21 Volts
Supply Voltage V_{CC} . . . . . −1.0 to +7.0 Volts
All Outputs and Supply Voltages V_{BB} and V_{SS} with respect to GND . . . . . −1.0 to +25 Volts
Power Dissipation at 25°C . . . . . 2 Watts

COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $T_A = 0°C$ to $55°C, V_{CC} = 5V \pm 5\%, V_{SS} = 19V \pm 5\%, V_{BB} - V_{SS} = 3.0V$ to $4.0V$

SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
I_{FD}	DATA INPUT LOAD CURRENT		−0.25	mA	$V_D = .45V, V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 19V, V_{BB} = 23V$
I_{FE}	ENABLE INPUT LOAD CURRENT		−0.50	mA	$V_E = .45V, V_{CC} = 5.25V$, All Other Inputs at 5.25V, $V_{SS} = 19V, V_{BB} = 23V$
I_{RD}	DATA INPUT LEAKAGE CURRENT		20	μA	$V_D = 19V, V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 19V, V_{BB} = 23V$
I_{RE}	ENABLE INPUT LEAKAGE CURRENT		20	μA	$V_E = 19V, V_{CC} = 5.0V$, All Other Inputs Grounded, $V_{SS} = 19V, V_{BB} = 23V$
V_{OL}	OUTPUT "LOW" VOLTAGE		0.8 0.7 0.6	V(0°C) V(25°C) V(55°C)	$I_{OL} = 500\mu A, V_{CC} = 4.75V$ $V_{SS} = 19V, V_{BB} = 23V$ All Inputs at 2.0V
V_{OH} (MIN.)	OUTPUT "HIGH" VOLTAGE	$V_{SS} - 0.7$ $V_{SS} - 0.6$ $V_{SS} - 0.5$		V(0°C) V(25°C) V(55°C)	$I_{OH} = -500\mu A, V_{CC} = 5.0V$ $V_{SS} = 19V, V_{BB} = 23V$ All Inputs at 0.85V
V_{OH} (MAX.)			$V_{SS} + 1.0$	V	$I_{OH} = 5mA, V_{CC} = 5.0V$ $V_{SS} = 19V, V_{BB} = 23V$
I_{OL}	OUTPUT SINK CURRENT	100		mA	$V_O = 4V, V_{CC} = 5.0V, V_{SS} = 19V$, $V_{BB} = 23V, V_E = V_D = 2.0V$
I_{OH}	OUTPUT SOURCE CURRENT	−100		mA	$V_O = V_{SS} - 4V, V_{CC} = 5.0V, V_{SS} = 19V$ $V_{BB} = 23V, V_E = V_D = 0.85V$
V_{IL}	INPUT "LOW" VOLTAGE		1.0	V	$V_{CC} = 5.0V, V_{SS} = 19V, V_{BB} = 23V$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0V, V_{SS} = 19V, V_{BB} = 23V$
C_{IN}	INPUT CAPACITANCE		8(Typical)	pF	$V_{BIAS} = 2.0V, V_{CC} = 0V$

D.C. CHARACTERISTICS (Cont'd) $T_A = 0°C$ to $+55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} - V_{SS} = 3.0V$ to $4.0V$

POWER SUPPLY CURRENT DRAIN:

All Outputs "Low"

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{CC}	Current from V_{CC}		83	mA	$V_{CC} = 5.25V$, $V_{SS} = 20V$, $V_{BB} = 24V$ All Inputs Open
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		25	mA	
P_{TOTAL}	Total Power Dissipation		1040	mW	

All Outputs "High"

I_{CC}	Current from V_{CC}		33	mA	$V_{CC} = 5.25V$, $V_{SS} = 20V$, $V_{BB} = 24V$ All Inputs Grounded
I_{SS}	Current from V_{SS}		250	μA	
I_{BB}	Current from V_{BB}		5	mA	
P_{TOTAL}	Total Power Dissipation		297	mW	

Standby Condition with $V_{CC} = 0V$, $V_{SS} = V_{BB}$

I_{CC}	Current from V_{CC}		0	mA	$V_{CC} = 0V$, $V_{SS} = 20V$, $V_{BB} = 20V$
I_{SS}	Current from V_{SS}		500	μA	
I_{BB}	Current from V_{BB}		500	μA	
P_{TOTAL}	Total Power Dissipation		15	mW	

MEMORY SUPPORT

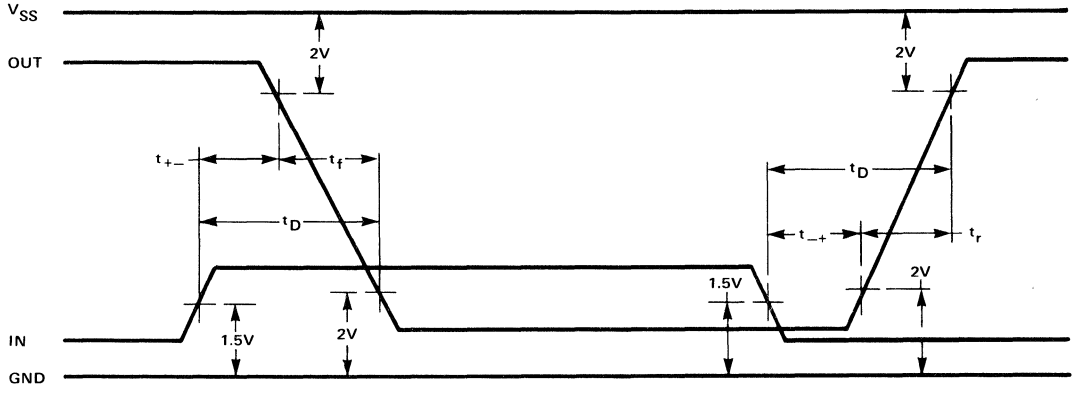
A.C. CHARACTERISTICS

$T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 19V \pm 5\%$, $V_{BB} = V_{SS} + 3$ to $4V$, $f = 2$ MHz, 50% Duty Cycle

SYMBOL	TEST	LIMITS (ns)				
		$C_L = 100$ pF		$C_L = 200$ pF		DELAY DIFFERENTIAL (1) $C_L = 200$ pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	25	10	35	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

(1) This is defined as the maximum skew between any output in the same package, eg., all the input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

WAVEFORMS



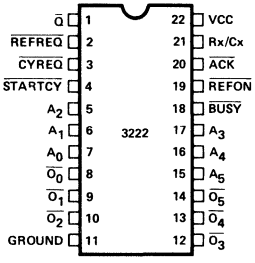
3222
REFRESH CONTROLLER FOR 4K DYNAMIC RANDOM ACCESS MEMORIES

- **Ideal for use in 2107A, 2107C Systems**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 22-Pin DIP**
- **Adjustable Refresh Timing Oscillator**
- **6-Bit Address Multiplexer**
- **6-Bit Refresh Address Counter**
- **Refresh Cycle Controller**

The Intel® 3222 is a refresh controller for dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). The device contains an accurate refresh timer (whose frequency can be set by an external resistor and capacitor), plus all necessary control and I/O circuitry to provide for the refresh requirements of dynamic RAMs. The chip's high performance makes it especially suitable for use with high speed N-channel RAMs like the Intel® 2107C. The 3222 is well suited for asynchronous dynamic memory systems.

The 3222 operates from a single +5 volt power supply and is specified for operation over a 0°C to 75°C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process.

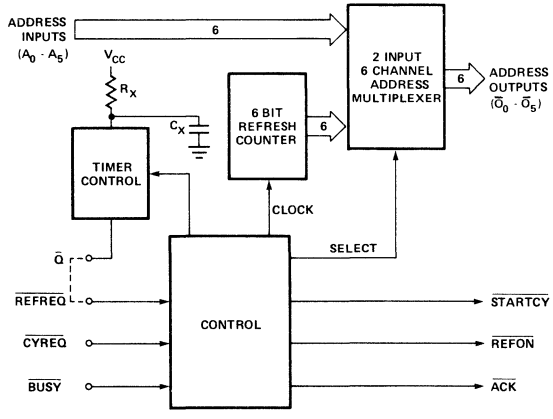
PIN CONFIGURATION



PIN NAMES

$A_0 - A_5$	ADDRESS INPUTS	$\overline{O}_0 - \overline{O}_5$	ADDRESS OUTPUTS
ACK	ACKNOWLEDGE OUTPUT	$\overline{Q}$	INTERNAL REFRESH REQUEST LATCH OUTPUT
BUSY	BUSY INPUT	REFON	REFRESH ON OUTPUT
CYREQ	CYCLE REQUEST INPUT	REFREQ	REFRESH REQUEST INPUT
		RxCx	RC TIE POINT
		STARTCY	START CYCLE OUTPUT
		V_{CC}	+5V SUPPLY

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65° to +125°C
Storage Temperature . . . . . -65° to +160°C
All Input, Output or Supply Voltages . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 100 mA
Power Dissipation . . . . . 1 W

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{FB}	Input Load Current $\overline{BUSY}$		0.40	1	mA	V_{IN} = 0.45V
I_{FO}	Input Load Current All Other Inputs		0.05	0.25	mA	V_{IN} = 0.45V
I_{RB}	Input Leakage Current $\overline{BUSY}$		<1	50	μA	V_{IN} = V_{CC}
I_{RO}	Input Leakage Current All Other Inputs		<1	20	μA	V_{IN} = 5.25V
V_{CLAMP}	Input Clamp Voltage		-0.76	-1	V	I_C = -5.0mA
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{CC}	Power Supply Current		91	120	mA	V_{CC} = 5.25V
I_{SC}	Output High Short Circuit Current		-48	-70	mA	V_{OUT} = 0V V_{CC} = 5.25V
V_{OL}	Output Low Voltage		0.32	0.45	V	I_{OL} = 5mA
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_5$)	2.6	3.1		V	I_{OH} = -1mA V_{CC} = 4.75V
V_{OH1}	Output High Voltage (All Other Outputs)	2.4	3.0		V	I_{OH} = -1mA V_{CC} = 4.75V

Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

Capacitance[2], T_A = 25°C

Symbol	Test	Limits (pF)		Conditions
		Typ.	Max.	
C_{IN} (Address)	Input Capacitance	5	10	V_{bias} = 2.0V
C_{IN} ($\overline{CYREQ}$)	Input Capacitance	6	10	V_{CC} = 0V
C_{IN} ($\overline{BUSY}$)	Input Capacitance	20	30	f = 1MHz

Note 2: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics

All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C. Load = 1 TTL, C_L = 15pF.
Conditions of Test: Input pulse amplitude: 3V, Input rise and fall times: 5ns between 1V and 2V. Measurements are made at 1.5V.

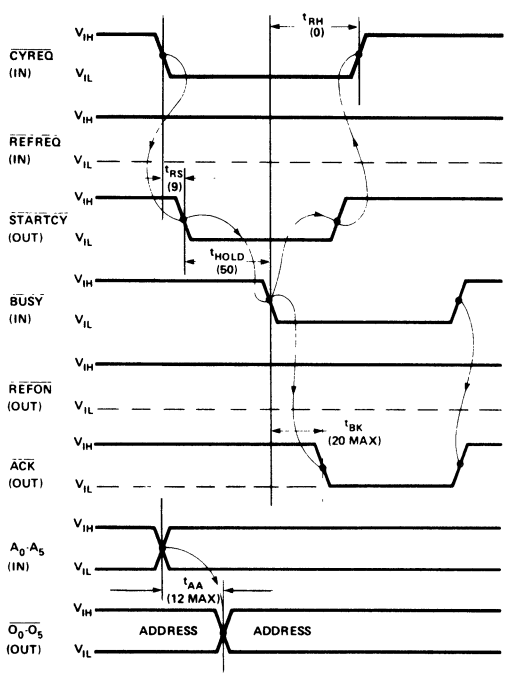
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
t_{AA}	Address In to Address Out		7	12	ns	$\overline{BUSY}$ = V_{IH}
t_{BAM}	$\overline{BUSY}$ In to Address Out		21	28	ns	
t_{BAR}	$\overline{BUSY}$ In to Counter Out		18	27	ns	
t_{BK}	$\overline{BUSY}$ In to $\overline{ACK}$ Out		14	20	ns	$\overline{REFREQ}$ = V_{IH}, $\overline{CYREQ}$ = V_{IL}
t_{BR}	$\overline{BUSY}$ In to $\overline{REFON}$ Out		15	24	ns	
t_{BS}	$\overline{BUSY}$ In to $\overline{STARTCY}$ Out	4	7	14	ns	$\overline{CYREQ}$ = V_{IL}
t_{HOLD}	$\overline{BUSY}$ Hold Time	50			ns	External Delay between $\overline{STARTCY}$ and $\overline{BUSY}$
t_{RH}	$\overline{CYREQ}$ or $\overline{REFREQ}$ Hold Time	0			ns	External Delay after $\overline{BUSY}$
t_{RR}	$\overline{REFREQ}$ to $\overline{REFON}$		18	26	ns	$\overline{CYREQ}$ and $\overline{BUSY}$ = V_{IH}, No priority contention between $\overline{REFREQ}$ and $\overline{CYREQ}$
t_{RRC}	$\overline{REFREQ}$ to $\overline{REFON}$		33	45	ns	$\overline{BUSY}$ = V_{IH}
t_{RS}	$\overline{CYREQ}$ or $\overline{REFREQ}$ In to $\overline{STARTCY}$ Out	9	14	21	ns	$\overline{BUSY}$ = V_{IH}
t_{Setup}	$\overline{BUSY}$ Setup Time	120			ns	$\overline{BUSY}$ = V_{IL} During Refresh

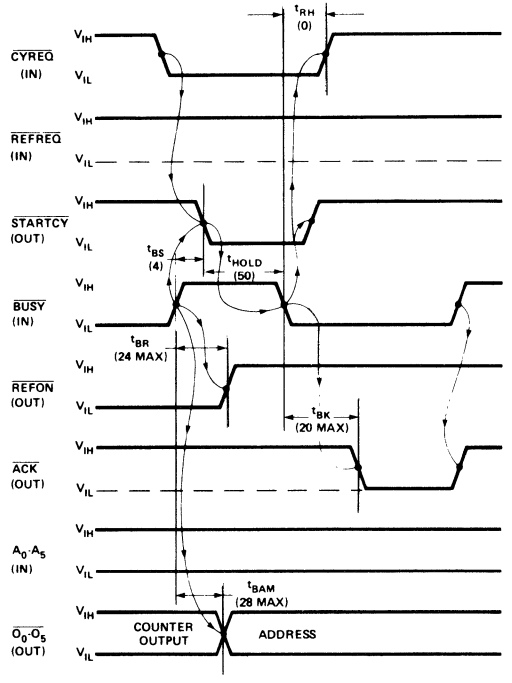
Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

A. SYSTEM MEMORY CYCLE WITH MEMORY NOT BUSY

B. SYSTEM MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING REFRESH CYCLE)

(Numbers in parentheses are minimum values in ns unless otherwise specified.)

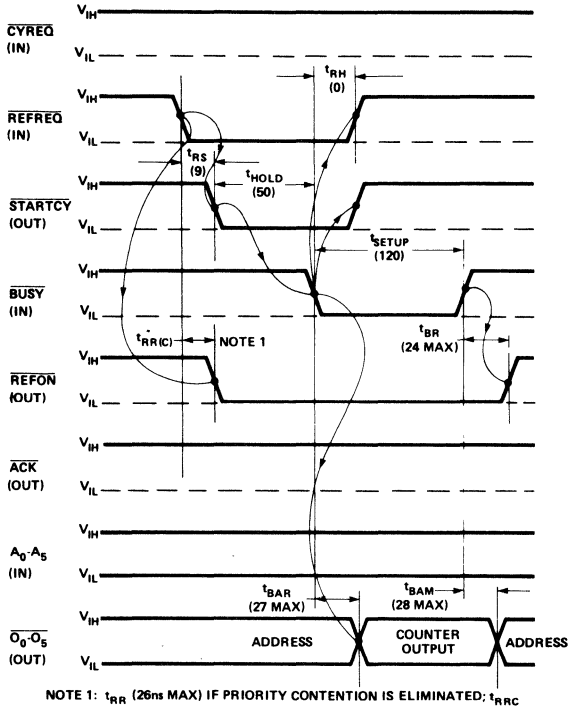




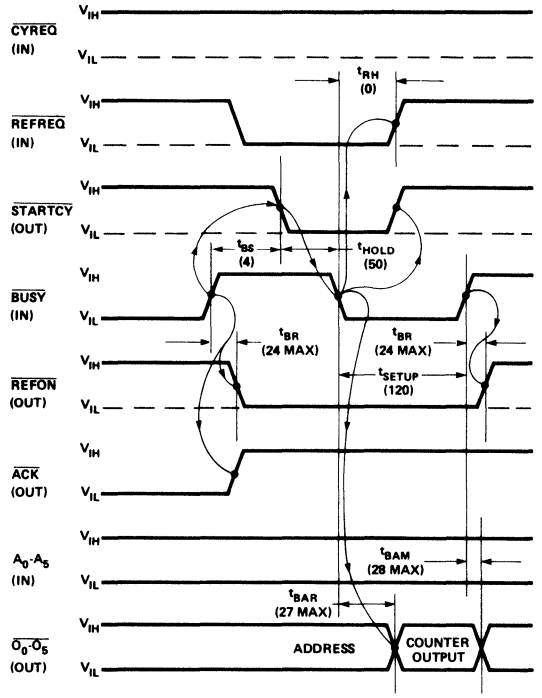
C. REFRESH MEMORY CYCLE WITH MEMORY NOT BUSY

D. REFRESH MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING SYSTEM CYCLE)

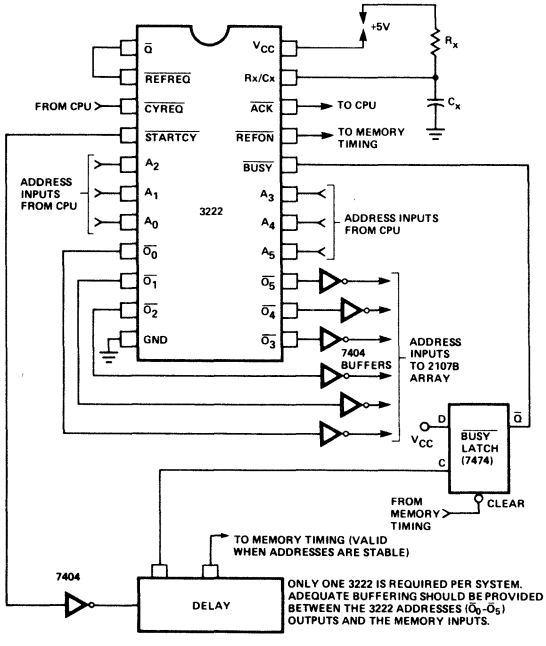
(Numbers in parentheses are minimum values in ns unless otherwise specified.)



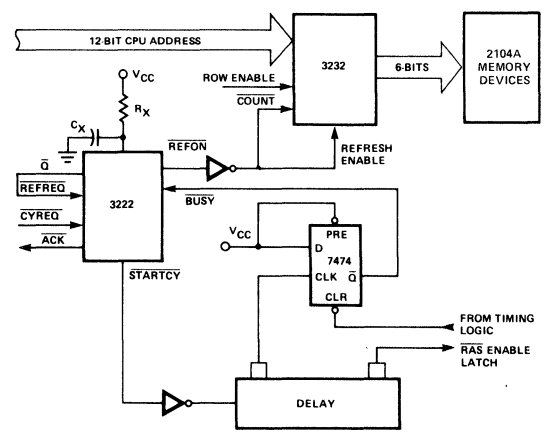
NOTE 1: t_{RR} (26ns MAX) IF PRIORITY CONTENTION IS ELIMINATED; t_{RRC}



E. TYPICAL APPLICATION OF 3222 REFRESH CONTROLLER IN A 2107C SYSTEM



F. USE OF 3222 FOR REFRESH TIMING AND CONTROL IN A 2104A SYSTEM



PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{Q}$	Output of the internal Refresh Request latch. This pin may be connected to the Refresh Request input ($\overline{REFREQ}$) directly for asynchronous sequential mode refresh or indirectly through control logic for burst mode or synchronous mode refresh (see text).
2	$\overline{REFREQ}$	Refresh Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a system cycle request did not occur first.
3	$\overline{CYREQ}$	System Memory Cycle Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a refresh request did not occur first.
4	$\overline{STARTCY}$	Output signal indicating to external circuitry that a memory cycle (system or refresh) is to begin. See text for timing considerations for a refresh cycle.
5-7 15-17	A_0-A_5	Low order system address inputs. These addresses are multiplexed to the address output pins ($\overline{O}_0$-$\overline{O}_5$) during a system cycle.
8-10	$\overline{O}_0$-$\overline{O}_5$	Low order memory address outputs. During a system cycle these outputs give the low order (A_0-A_5) address of a memory access. During a refresh cycle these outputs give the refresh address (generated internal to the 3222).
11	GROUND	Ground.
18	$\overline{BUSY}$	An externally generated signal which the 3222 monitors to determine memory system status. If $\overline{BUSY}$ is high the memory is not busy and a system or refresh cycle may begin. If $\overline{BUSY}$ is low the memory is being accessed for a data I/O or refresh cycle and no other cycle may begin.
19	$\overline{REFON}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a refresh cycle (Refresh On).
20	$\overline{ACK}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a system cycle (system cycle request accepted and acknowledged).
21	RX/CX	Connection point for the RC network which determines the refresh period for sequential refresh mode. (See Refresh Control section).
22	V_{CC}	+5 volt supply.

FUNCTIONAL DESCRIPTION

The Intel® 3222 performs the four basic functions of a refresh controller by:

1. Providing a refresh timing oscillator.
2. Generating six bit refresh addresses.
3. Multiplexing refresh and system addresses to the six low order address inputs ($\overline{O}_0$-$\overline{O}_5$).
4. Providing control signals for both refresh and memory cycle accesses.

As shown in the pin configuration figure, the 3222 has as inputs the six low order (A_0-A_5) system addresses. These addresses are internally multiplexed with six internally generated refresh addresses. The output of these multiplexers provide the six low order addresses to the memory array.

The block diagram shows the four main circuit categories of the 3222. An explanation of the workings of each of these categories is given in the Device Operation section from a users point of view.

DEVICE OPERATION

Operation of the Intel® 3222 Refresh Controller is most easily explained by considering five conditions presented by the three input control lines Cycle Request ($\overline{CYREQ}$), Refresh Request ($\overline{REFREQ}$), and System Busy ($\overline{BUSY}$). These conditions are:

1. System memory cycle request — memory not busy ($\overline{BUSY}$ = High)
2. System memory cycle request — memory busy ($\overline{BUSY}$ =Low)
3. Refresh cycle request — memory not busy ($\overline{BUSY}$ = High)
4. Refresh cycle request — memory busy ($\overline{BUSY}$ =Low)
5. Simultaneous system memory cycle and refresh cycle requests.

Condition 5 is actually a subset of the four previous conditions and is included for completeness.

As is implied in the five conditions, the response of the 3222 to both refresh and memory cycles is dependent on the state of the $\overline{BUSY}$ input. The $\overline{BUSY}$ signal is generated externally to the 3222 and, when low, defines the time when the memory is performing a cycle (refresh or memory access). It is important to assure that $\overline{BUSY}$ is low for the *entire* memory cycle time. Interference may occur in asynchronous memory systems if the $\overline{BUSY}$ input goes high prematurely. (An asynchronous memory system is one in which the refresh and memory cycle requests occur independent of each other.)

System Memory Cycle Request — Memory Not Busy

This section details operation of the 3222 when the memory is not busy and a request for a system memory cycle is made (See Figure A for timing sequences). The request for a memory cycle is made by the $\overline{CYREQ}$ input going low. The Start Cycle output $\overline{STARTCY}$ goes low at t_{RS} after $\overline{CYREQ}$. $\overline{STARTCY}$ is used for two purposes:

1. To set the external $\overline{BUSY}$ latch. (See Figure E.)
2. To initiate memory system timing (after appropriate delay).

The required delay time depends on system configuration and associated delay paths for both Chip Enable (2107B input signal) and system addresses.

The low going $\overline{BUSY}$ input causes the internally generated Start Cycle output to go high and the Acknowledge output $\overline{ACK}$ to go low (after t_{BK} time). The Acknowledge output confirms that the requested system memory cycle has been accepted by the 3222. Note that the cycle request input may be returned to the high state when the $\overline{BUSY}$ input goes low. However, at the designer's discretion, the cycle request line may remain low until "just prior" to $\overline{BUSY}$ returning high. (If $\overline{BUSY}$ goes high before $\overline{CYREQ}$ goes high, another memory access may inadvertently be started.)

When the memory is not busy and a cycle request has been made, the low order system address delay through the 3222 is t_{AA} nsec. When the 3222 is not busy, the low order system addresses (A_0-A_5) are gated through to the output ($\overline{O}_0$-$\overline{O}_5$) independent of any other input.

System Memory Cycle Request — Memory Busy

The major differences between a system memory cycle request when the system is busy and when it is not busy (as previously described) are:

1. The Start Cycle output $\overline{STARTCY}$ does not go low until t_{BS} after the rising edge of the $\overline{BUSY}$ input. (Even though the $\overline{CYREQ}$ input is low.)
2. Output addresses $\overline{O}_0$-$\overline{O}_5$ change at or before t_{AA} time if the previous cycle was a system cycle request and change at or before t_{BAM} if the previous cycle was a Refresh Cycle request. (Note that the longer delay is after a refresh cycle.) See Figure B for definition of terms.

Note that for a system memory cycle following a refresh cycle, the refresh on output $\overline{REFON}$ goes high at or before t_{BR} relative to $\overline{BUSY}$ going high. Since the Acknowledge output $\overline{ACK}$ can not go low until after t_{HOLD} there is no ambiguity between $\overline{REFON}$ and $\overline{ACK}$. The memory is always defined as being in a refresh cycle, system cycle or no cycle.

Refresh Cycle — Memory Not Busy

Operation of the 3222 for a refresh request with the memory not busy (see Figure C) is similar to a system cycle request under the same condition. A refresh cycle is initiated by the Refresh Request input ($\overline{REFREQ}$) going low. This low going input causes both the Start Cycle output, $\overline{STARTCY}$, and Refresh On output, $\overline{REFON}$, to go low at t_{RS} and t_{RRC} (or t_{RR}) time respectively. The low going edge of $\overline{STARTCY}$ is used to set the external $\overline{BUSY}$ latch low. As in the previous two cases, the $\overline{BUSY}$ input must remain low for the entire cycle required by the memory. As in the previous two cases, the low going $\overline{BUSY}$ drives the $\overline{STARTCY}$ output high.

Refresh Cycle — Memory Busy

For this condition, it is assumed that the previous cycle was a system access cycle. Timing conditions for this operation are shown in Figure D. Here, the $\overline{STARTCY}$ input goes low t_{BS} after $\overline{BUSY}$ returns high from the previous cycle. As before, $\overline{REFON}$ goes low t_{BR} after $\overline{BUSY}$ goes high. After t_{HOLD}, relative to $\overline{STARTCY}$, $\overline{BUSY}$ again goes low and places the low order refresh addresses on the address outputs ($\overline{O}_0$-$\overline{O}_5$) after t_{BAR} time. Internal refresh timing is performed in a manner identical to that described in Refresh Cycle-Memory Not Busy section.

Simultaneous Refresh and Memory System Cycle Request

The simultaneous request for a refresh and memory system access is almost a certainty in asynchronous systems. It is, therefore, necessary to have circuitry in any refresh controller capable of resolving the attendent ambiguity with minimum additional delay. The Intel® 3222 Refresh Controller has just such a circuit. (All timing parameters specified for asynchronous operation assume that a refresh and memory system request can occur at the same time.) A latch internal to the 3222 decides which signal ($\overline{CYREQ}$ or $\overline{REFREQ}$) it will accept if both occur simultaneously, and conditions the other control circuits appropriately. If a refresh cycle was accepted, $\overline{REFON}$ will go low at the appropriate time. If a memory system access was accepted then $\overline{ACK}$ will go low at the appropriate time.

Refresh Control

The 3222 controls both burst and distributed refresh modes. The burst refresh mode requires that $\overline{REFREQ}$ be generated externally to the 3222 since refresh is completed in 64 consecutive cycles every 2ms. A system requiring distributed refresh timing, however can be controlled either by the 3222 or by external circuitry. If refresh timing is to be controlled by the 3222 the output $\overline{Q}$ is tied to the $\overline{REFREQ}$ input. Timing is controlled by an oscillator internal to the 3222. The desired refresh timing interval is determined by:

1. $\frac{t_{REF}}{r} = .63\ R_X C_X$

   Where:

   t_{REF} = the total time between refreshes (e.g. 2msec) in msec.

   r = the number of rows to be refreshed on the memory device (for the 2107C r = 64).

   R_X = external timing resistance in KΩ (3K to 10K)

   C_x = external timing capacitance in μf. (0.005μf to 0.02μf)

The 3222's oscillator stability is guaranteed to be ±2% for a given part and ±6% from part to part, both over the ranges $0°C \leqslant T_A \leqslant 75°C$ and $V_{CC} = 5.0V \pm 5\%$.

Figure F shows how the 3222 may be used to control refresh in a 2104A system.

3232
ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 4K DYNAMIC RAMs

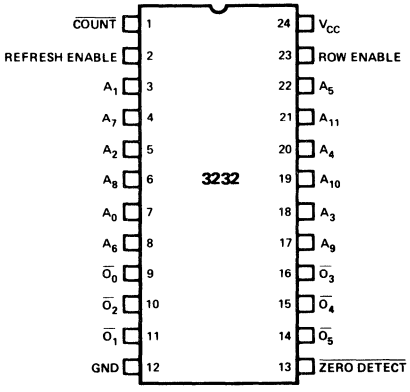
- **Ideal for 2104A**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 24-Pin DIP**
- **Address Input to Output Delay: 9ns Maximum Driving 15pF, 25ns Maximum Driving 250pF**
- **Suitable for Either Distributed or Burst Refresh**
- **Single Power Supply: +5 Volts ±10%**

MEMORY SUPPORT

The Intel® 3232 contains an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). It multiplexes twelve bits of system supplied address to six output address pins. The device also contains a 6 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3232 makes it especially suitable for use with high speed N-channel RAMs like the 2104A.

The 3232 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range.

PIN CONFIGURATION



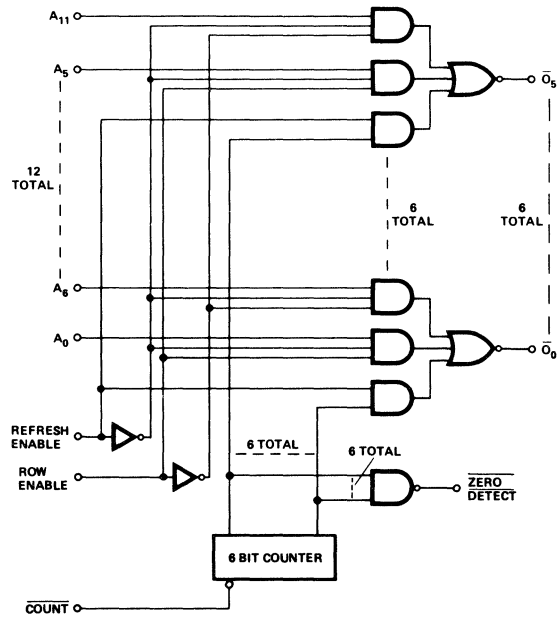
NOTE: A_0 THROUGH A_5 ARE ROW ADDRESSES.
A_6 THROUGH A_{11} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_5)
L	L	COLUMN ADDRESS (A_6 THROUGH A_{11})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES A ZERO IN THE REFRESH ADDRESS (USED IN BURST REFRESH MODE).

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -65° to +125°C
Storage Temperature ..... -65° to +160°C
All Input, Output, or
Supply Voltages .....-0.5V to +7 Volts
Output Currents 100mA
Power Dissipation 1W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

All Limits Apply for V_{CC} = 5.0V ±10%, T_A = 0°C to + 75°C

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.(1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	V_{IN} = 0.45V
I_R	Input Leakage Current		0	10	μA	V_{IN} = 5.5V
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	I_{OL} = 5mA
V_{OH}	Output High Voltage ($\overline{O_0}$-$\overline{O_5}$)	2.8	4.0		V	I_{OH} = −1mA
V_{OH1}	Output High Voltage ($\overline{Zero\ Detect}$)	2.4	3.3		V	I_{OH} = −1mA
I_{CC}	Power Supply Current		100	150	mA	V_{CC} = 5.5V

Note 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

A.C. CHARACTERISTICS

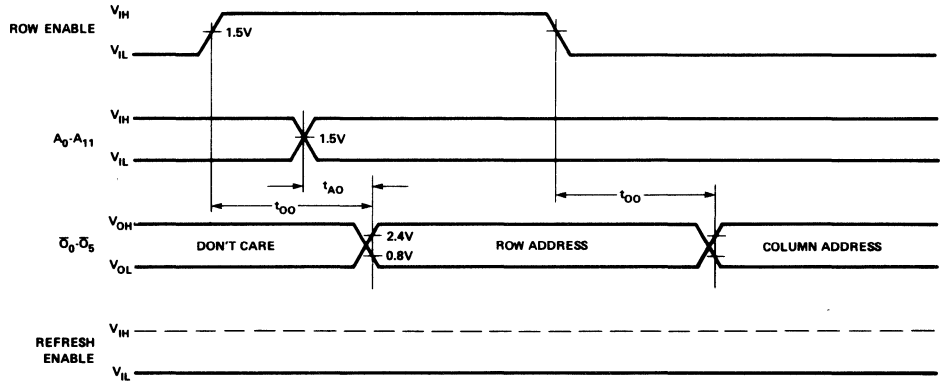
All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low(1) (2)
t_{AOI}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	27	ns	Refresh Enable = Low(1) (2)
t_{OOI}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	27	ns	Note 1, 2
t_{EOI}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	$\overline{\text{Count}}$ to Output	15	40	60	ns	Refresh Enable = High(1) (2)
t_{COI}	$\overline{\text{Count}}$ to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency	5			MHz	
t_{CPW}	$\overline{\text{Count}}$ Pulse Width	35			ns	
t_{CZ}	$\overline{\text{Count}}$ to $\overline{\text{Zero Detect}}$	15		70	ns	Note 2

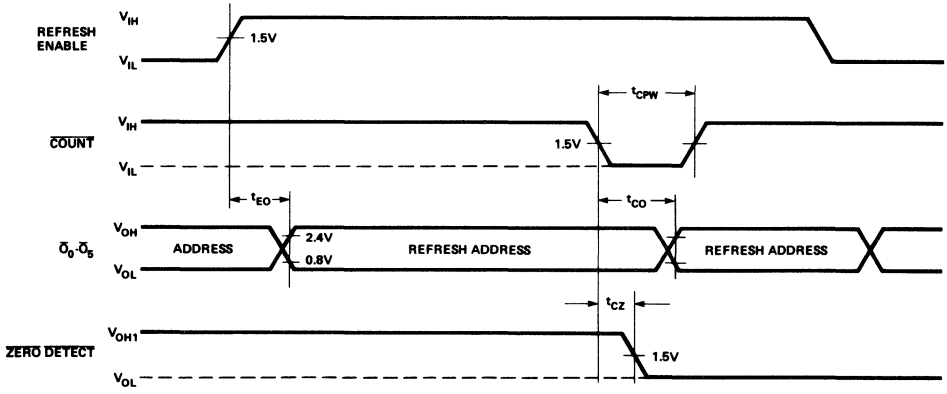
Note 1: V_{CC} = 5.0V, T_A = 25°C
2: C_L = 15pF

A.C. TIMING WAVEFORMS (Typically used with 2104A)

NORMAL CYCLE



REFRESH CYCLE



PIN NAMES AND FUNCTIONS

Pin. No.	Pin Name	Function
1	$\overline{\text{Count}}$ Input	Active low input increments internal six bit counter by one for each count pulse in.
2	Refresh Enable Input	Active high input which determines whether the 3232 is in refresh mode (H) or address enable (L).
7,3,5,18, 20,22	A_0-A_5 Inputs	Row Address inputs.
8,4,6,17, 19,21	A_6-A_{11} Inputs	Column address inputs.
9,11,10, 16,15,14	$\overline{O}_0$-$\overline{O}_5$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
12	GND	Power supply ground.
13	$\overline{\text{Zero}}$ $\overline{\text{Detect}}$ Output	Active low output which senses that all six bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
23	Row Enable Input	High input selects row, low input selects column addresses of the driven memories.
24	V_{CC}	+5V power supply input.

DEVICE OPERATION

The Intel® 3232 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter)
2. Row addresses (A_0 through A_5)
3. Column addresses (A_6 through A_{11})

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the 6 outputs of the internal 6 bit counter. At each $\overline{\text{Count}}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0$-$\overline{O}_5$) through all 64 row addresses. When the counter sequences to all zeros, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output goes low signaling the end of the refresh sequence. Due to counter decoding spikes, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output is valid only after t_{CZ} following the low going edge of $\overline{\text{Count}}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of rows in the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2104A $t_{REFRESH}$ = 2msec and n = 64, therefore one row is refreshed each 31 μsec. Following the refresh cycle at row n_x, the Count input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The Count input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All twelve system address lines are applied to the inputs of the 3232. When Refresh Enable is low and Row Enable is high, input addresses A_0-A_5 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_6-A_{11} are gated to the outputs and applied to the driven memories.

Figure 1 shows a typical connection between the 3232 and the 2104A 4K dynamic RAM. When the memory devices are driven directly by the 3232, the address applied to the memory devices is the inverse of the address at the 3232 inputs due to the inverted outputs of the 3232. This should be remembered when checking out the memory system.

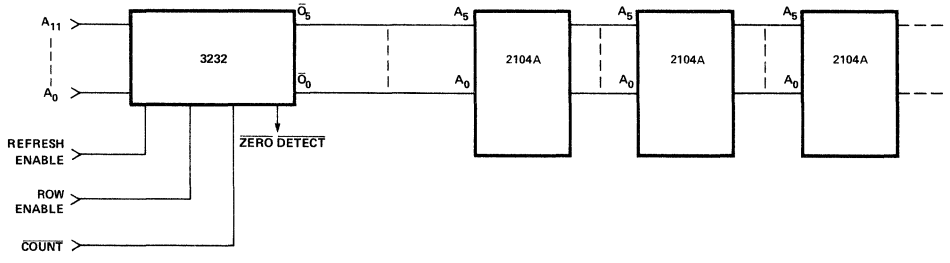


Figure 1. Typical Connection of 3232 and 2104 Memories.

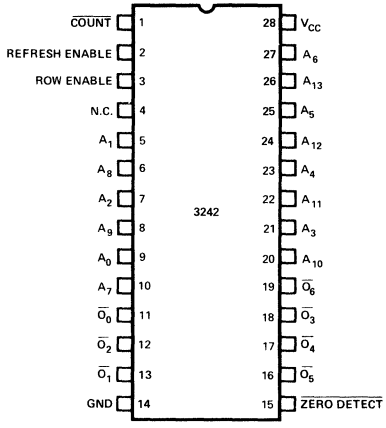
3242
ADDRESS MULTIPLEXER AND REFRESH COUNTER FOR 16K DYNAMIC RAMs

- **Ideal For 2116**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 28-Pin DIP**
- **Suitable For Either Distributed Or Burst Refresh**
- **Single Power Supply: +5 Volts ±10%**
- **Address Input to Output Delay: 9ns Driving 15 pF, 25ns Driving 250pF**

The Intel® 3242 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of 64 or 128 cycles. It multiplexes 14 bits of system supplied address to 7 output address pins. The device also contains a 7 bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 3242 makes it especially suitable for use with high speed N-channel RAMs like the 2116.

The 3242 operates from a single +5 volt power supply and is specified for operation over a 0 to +75°C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process and is packaged in a hermetically sealed 28 pin Type D package.

PIN CONFIGURATION



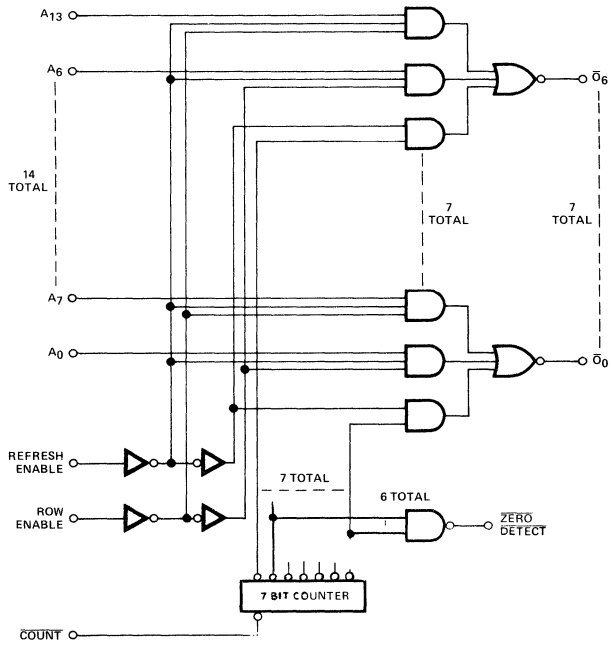
NOTE: A_0 THROUGH A_6 ARE ROW ADDRESSES.
A_7 THROUGH A_{13} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_6)
L	L	COLUMN ADDRESS (A_7 THROUGH A_{13})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES ZERO IN THE FIRST 6 SIGNIFICANT REFRESH COUNTER BITS (USED IN BURST REFRESH MODE)

LOGIC DIAGRAM



A.C. Characteristics

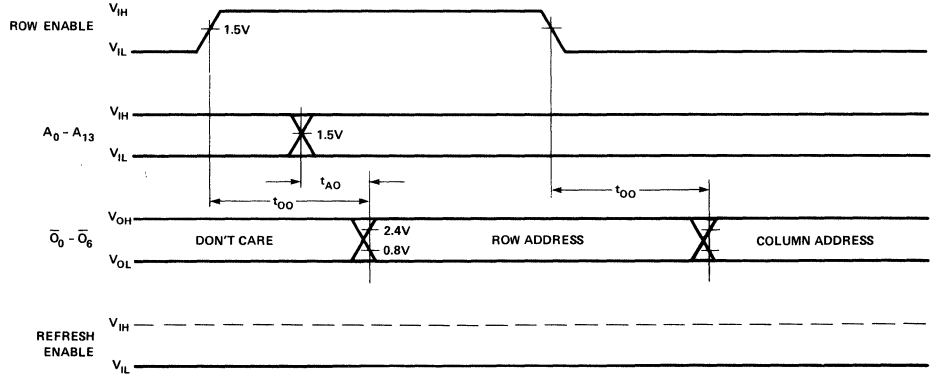
All Limits Apply for V_{CC} = +5.0V ±10%, T_A = 0°C to 75°C, Load = 1 TTL, C_L = 250pF, Unless Otherwise Specified.

SYMBOL	PARAMETER	MIN.	TYP.(1)	MAX.	UNIT	CONDITIONS
t_{AO}	Address Input to Output Delay		6	9	ns	Refresh Enable = Low(2)(3)
t_{AO1}	Address Input to Output Delay		16	25	ns	Refresh Enable = Low
t_{OO}	Row Enable to Output Delay	7	12	27	ns	Refresh Enable = Low(2)(3)
t_{OO1}	Row Enable to Output Delay	12	28	41	ns	Refresh Enable = Low
t_{EO}	Refresh Enable to Output Delay	7	14	27	ns	Notes 2, 3
t_{EO1}	Refresh Enable to Output Delay	12	30	45	ns	
t_{CO}	$\overline{\text{Count}}$ to Output	15	40	60	ns	Refresh Enable = High(2)(3)
t_{CO1}	$\overline{\text{Count}}$ to Output	20	55	80	ns	Refresh Enable = High
f_C	Counting Frequency			5	MHz	
t_{CPW}	$\overline{\text{Count}}$ Pulse Width	35			ns	
t_{CZ}	$\overline{\text{Count}}$ to $\overline{\text{Zero}}$ $\overline{\text{Detect}}$	15		70	ns	Note 3

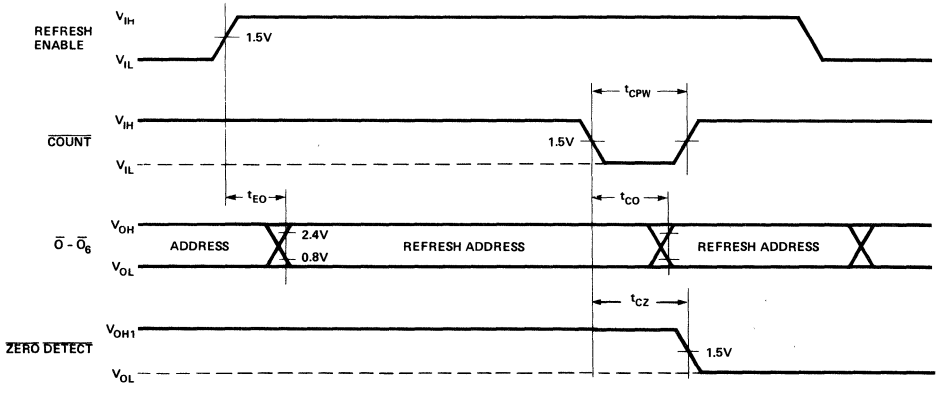
Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. T_A = 25°C, V_{CC} = 5.0V.
3. C_L = 15 pF.

A.C. TIMING WAVEFORMS (Typically used with 2116)

NORMAL CYCLE



REFRESH CYCLE



Absolute Maximum Ratings*

Temperature Under Bias ..... -10° to +85°C
Storage Temperature ..... -65° to +150°C
All Input, Output, or
Supply Voltages .....-0.5V to +7 Volts
Output Currents 100mA
Power Dissipation 1W

COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

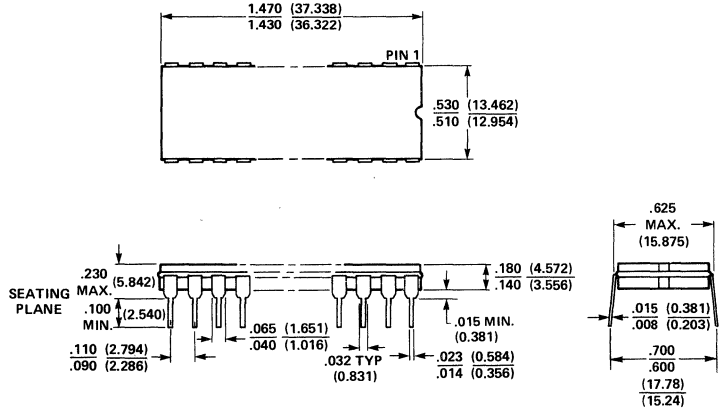
All Limits Apply for V_{CC} = 5.0V ±10%, T_A = 0°C to + 75°C

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. (1)	MAX.		
I_F	Input Load Current		-0.04	-0.25	mA	V_{IN} = 0.45V, Note 2
I_R	Input Leakage Current		0.01	10	μA	V_{IN} = 5.5V
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OL}	Output Low Voltage		0.25	0.40	V	I_{OL} = 8mA
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_6$)	3.0	4.0		V	I_{OH} = −1mA
V_{OH1}	Output High Voltage ($\overline{Zero\ Detect}$)	2.4	3.3		V	I_{OH} = −1mA
I_{CC}	Power Supply Current		105	165	mA	V_{CC} = 5.5V

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Inputs are high impedance, TTL compatible, and suitable for bus operation.

Packaging Information

28 LEAD HERMETIC DUAL IN-LINE PACKAGE
TYPE D



PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{\text{Count}}$ Input*	Active low input increments internal 7-bit counter by one for each count pulse in.
2	Refresh Enable Input*	Active high input which determines whether the 3242 is in refresh mode (H) or address enable (L).
9,5,7,21, 23,25,27	A_0–A_6 Inputs*	Row address inputs.
10,6,8,20, 22,24,26	A_7–A_{13} Inputs*	Column address inputs.
11,13,12, 18,17,16, 19	$\overline{O}_0$–$\overline{O}_6$ Outputs	Address outputs to memories. Inverted with respect to address inputs.
14	GND	Power supply ground.
15	$\overline{\text{Zero}}$ $\overline{\text{Detect}}$ Output	Active low output which senses that the six low order bits of refresh address in the counter are zero. Can be used in the burst mode to sense refresh completion.
3	Row Enable Input*	High input selects row, low input selects column addresses of the driven memories.
28	V_{CC}	+5V power supply input.

*The inputs are high impedance, TTL compatible, and suitable for bus operation.

DEVICE OPERATION

The Intel® 3242 Address Multiplexer/Refresh Counter performs the following functions:

1. Row, Column and Refresh Address multiplexing.
2. Address Counting for burst or distributed refresh.

These functions are controlled by two signals: Refresh Enable and Row Enable, both of which are active high TTL inputs. The truth table on page 1 shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter).
2. Row addresses (A_0 through A_6).
3. Column addresses (A_7 through A_{13}).

Burst Refresh Mode

When refresh is requested, the refresh enable input is high. This input is ANDed with the seven outputs of the internal 7-bit counter. At each $\overline{\text{Count}}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0$–$\overline{O}_6$) through 128 row addresses. When the first six significant bits of the counter sequence to all zeros, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output goes low, signaling the end of the refresh sequence. Due to counter decoding spikes, the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output is valid only after t_{CZ} following the low-going edge of $\overline{\text{Count}}$. The $\overline{\text{Zero}}$ $\overline{\text{Detect}}$ output used in this manner signals the completion of 64 refresh cycles. To use the 128-cycle burst refresh mode, an external flip-flop must be driven by the $\overline{\text{Zero}}$ $\overline{\text{Detect}}$.

Distributed Refresh Mode

In the distributed refresh mode, one row is selected for refresh each ($t_{REFRESH}/n$) time where n = number of refresh cycles required for the device and $t_{REFRESH}$ is the specified refresh rate for the device. For the 2116 $t_{REFRESH}$ = 2 msec and n = 128 or 64, therefore, one row is refreshed each 15.5 or 31 μsec, respectively. Following the refresh cycle at row n_x, the $\overline{\text{Count}}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n_{x+1}. The $\overline{\text{Count}}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address

All 14 system address lines are applied to the inputs of the 3242. When Refresh Enable is low and Row Enable is high, input addresses A_0–A_6 are gated to the outputs and applied to the driven memories. Conversely, when Row Enable is low (with Refresh Enable still low), input addresses A_7–A_{13} are gated to the outputs and applied to the driven memories. Figure 1 shows a typical connection between the 3242 and the 2116 16K dynamic RAM. When the memory devices are driven directly by the 3242, the address applied to the memory devices is the inverse of the address at the 3242 inputs due to the inverted outputs of the 3242. This should be remembered when checking out the memory system.

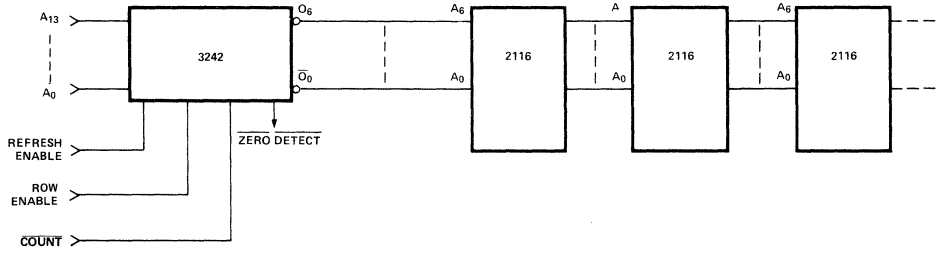


Figure 1. Typical Connection of 3242 and 2116 Memories.

3245
QUAD TTL-TO-MOS DRIVER
FOR 4K N-CHANNEL MOS RAMs

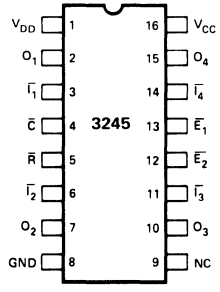
- **Fully Compatible with 4K RAMs Without Requiring Extra Supply or External Devices**
- **High Speed, 32 nsec Max. — Delay + Transition Time**
- **Low Power — 75mW Typical Per Channel**
- **High Density — Four Drivers in One Package**
- **TTL and DTL Compatible Inputs**
- **CerDIP Package — 16 Pin DIP**
- **Only +5 and +12 Volt Supplies Required**

The Intel® 3245 is a Quad Bipolar-to-MOS driver which accepts TTL and DTL input signals. It provides high output current and voltage suitable for driving the clock inputs of N-channel MOS memories such as the 2107B. The circuit operates from two power supplies which are 5 and 12 volts. Input and output clamp diodes minimize line reflections.

The device features two common enable inputs, a refresh select input, and a clock control input for simplified system designs. The internal gating structure of the 3245 eliminates gating delays and minimizes package count.

The 3245 is fabricated by means of Intel's highly reliable Schottky bipolar process and is specified for operation over a 0 to +75°C ambient temperature range.

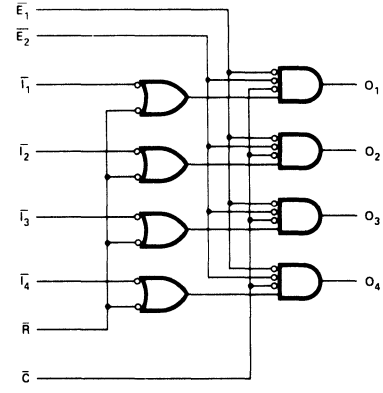
PIN CONFIGURATION



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	SELECT INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{E_1}$, $\overline{E_2}$	ENABLE INPUTS	V_{CC}	+5V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT	NC	NOT CONNECTED

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -10°C to 85°C
Storage Temperature. . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 to +7V
Supply Voltage, V_{DD} . . . . . -0.5 to +14V
All Input Voltages . . . . . -1.0 to V_{DD}
Outputs for Clock Driver . . . . . -1.0 to V_{DD} +1V
Power Dissipation at 25°C 2W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$		-0.25	mA	V_F = 0.45V
I_{FE}	Input Load Current, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$		-1.0	mA	V_F = 0.45V
I_{RD}	Data Input Leakage Current		10	μA	V_R = 5.0V
I_{RE}	Enable Input Leakage Current		40	μA	V_R = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5mA, V_{IH} = 2V
		-1.0		V	I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.50		V	I_{OH} = -1mA, V_{IL} = 0.8V
			V_{DD}+1.0	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs		0.8	V	
V_{IH}	Input High Voltage, All Inputs	2		V	

POWER SUPPLY CURRENT DRAIN AND POWER DISSIPATION

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions — Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	23	30	mA	High	V_{CC} = 5.25V V_{DD} = 12.6V
I_{DD}	Current from V_{DD}	19	26	mA		
P_{D1}	Power Dissipation	365	485	mW		
	Power Per Channel	91	121	mW		
I_{CC}	Current from V_{CC}	29	39	mA	Low	
I_{DD}	Current from V_{DD}	12	15	mA		
P_{D2}	Power Dissipation	300	388	mW		
	Power Per Channel	75	97	mW		

A.C. CHARACTERISTICS $T_A = 0°$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	5	11		ns	$R_{SERIES} = 0$
t_{DR}	Delay Plus Rise Time		20	32	ns	$R_{SERIES} = 0$
t_{+-}	Input to Output Delay	3	7		ns	$R_{SERIES} = 0$
t_{DF}	Delay Plus Fall Time		18	32	ns	$R_{SERIES} = 0$
t_T	Output Transition Time	10	17	25	ns	$R_{SERIES} = 20\Omega$
t_{DR}	Delay Plus Rise Time		27	38	ns	$R_{SERIES} = 20\Omega$
t_{DF}	Delay Plus Fall Time		25	38	ns	$R_{SERIES} = 20\Omega$

NOTES: 1. $C_L = 150pF$ ┐
2. $C_L = 200pF$ ├ These values represent a range of total stray plus clock capacitance for nine 4K RAMs.
3. $C_L = 250pF$ ┘
4. Typical values are measured at 25°C.

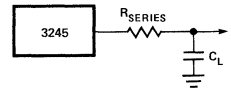
CAPACITANCE * $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance, $\overline{I}_1, \overline{I}_2, \overline{I}_3, \overline{I}_4$	5	8	pF
C_{IN}	Input Capacitance, $\overline{R}, \overline{C}, \overline{E}_1, \overline{E}_2$	8	12	pF

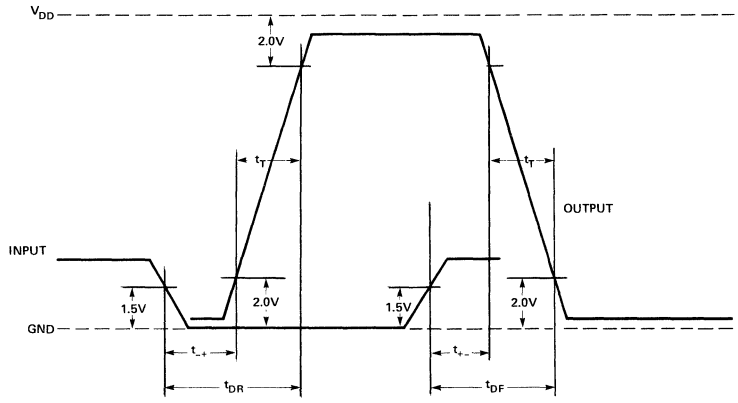
*This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{bias} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

A.C. CONDITIONS OF TEST

Input Pulse Amplitudes: 3.0V
Input Pulse Rise and Fall Times: 5 ns between 1 volt and 2 volts
Measurement Points: See Waveforms

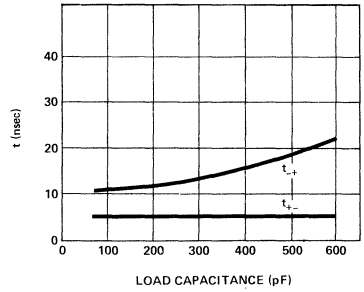


WAVEFORMS

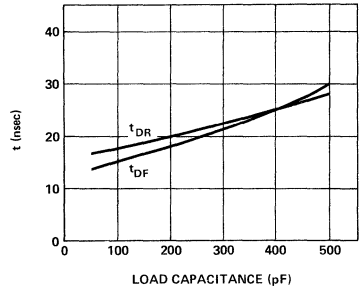


TYPICAL CHARACTERISTICS

INPUT TO OUTPUT DELAY VS. LOAD CAPACITANCE

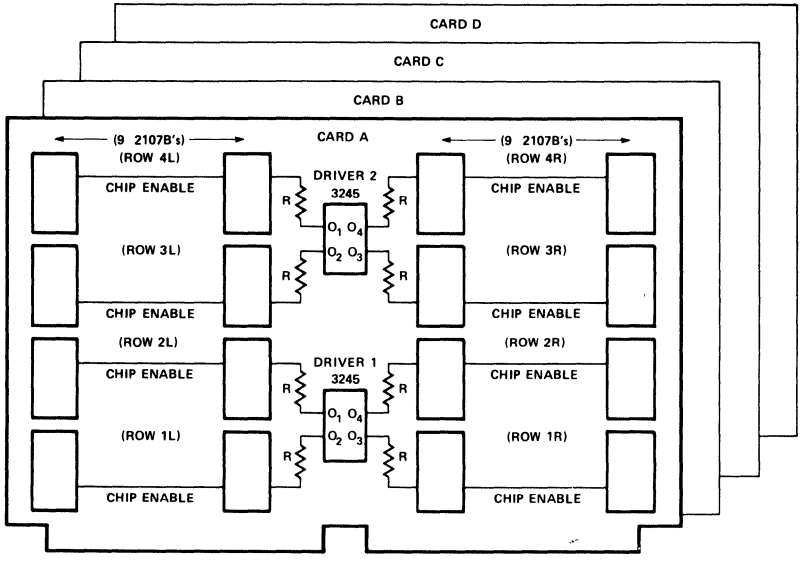


DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE



Typical System

Below is an example of a 64K x 18 bit memory system (each card is 16K x 18) employing the 3245 quad high voltage driver for the chip enable inputs. A single 3245 package drives 16K x 9 bits. A_0 through A_{11} are 2107B addresses.



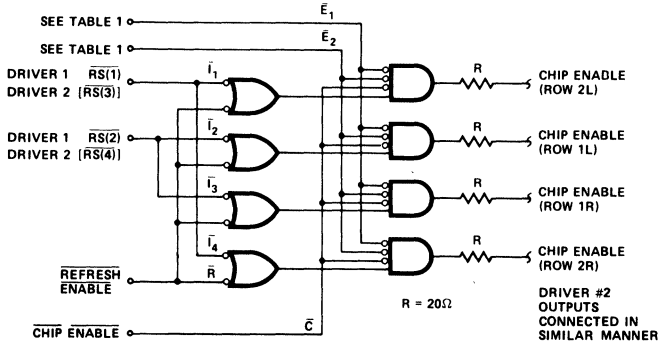
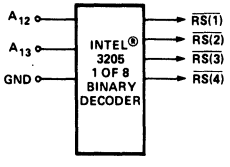
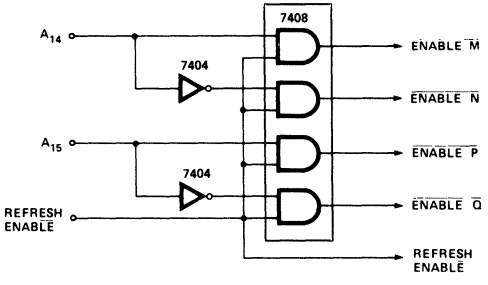
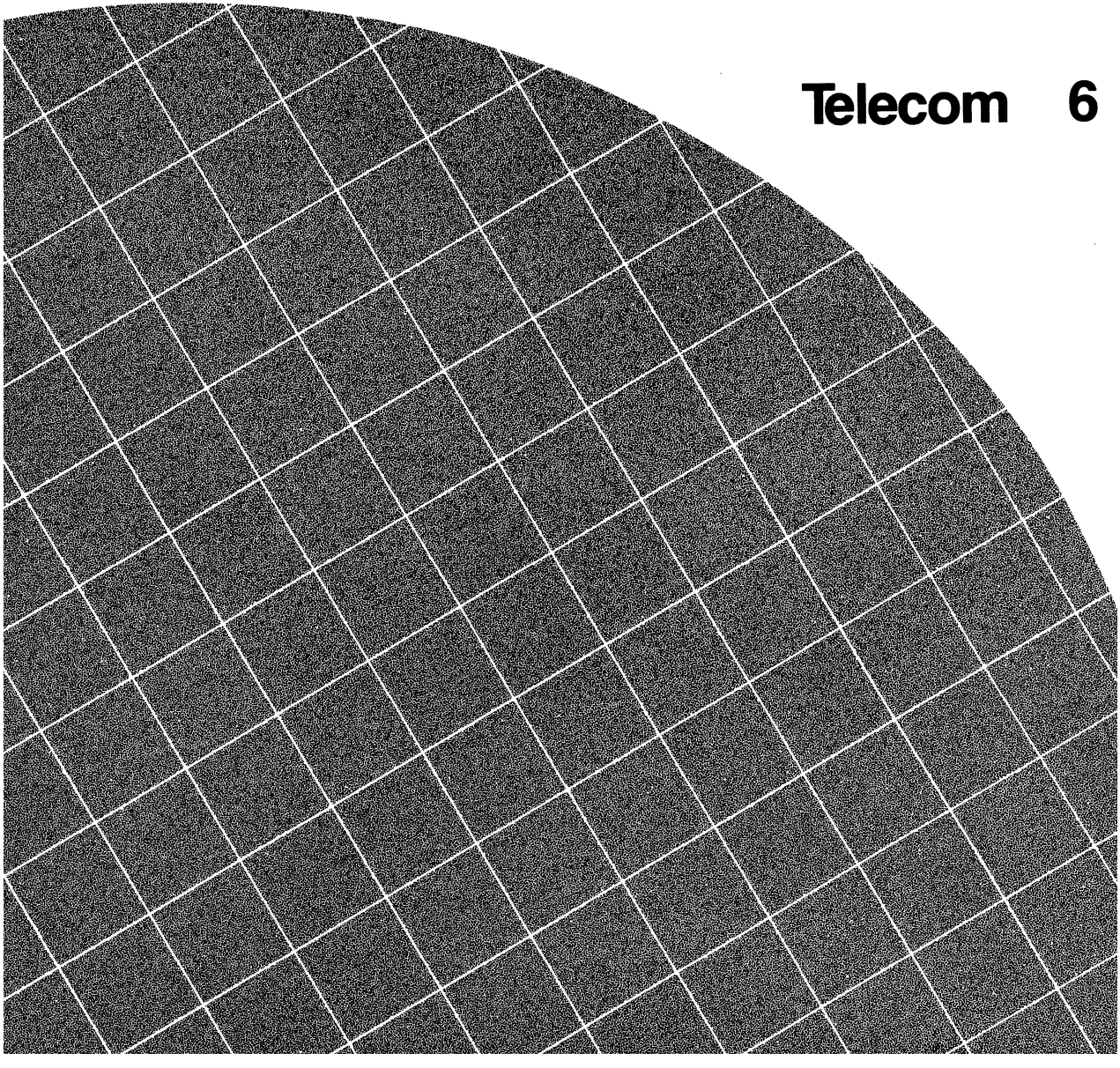


TABLE 1.

CARD	INPUTS $\bar{E}_1$	INPUTS $\bar{E}_2$
A	ENABLE M	ENABLE P
B	ENABLE M	ENABLE Q
C	ENABLE N	ENABLE P
D	ENABLE N	ENABLE Q







Telecom 6

TELECOMMUNICATIONS

INTRODUCTION

The 2910 and 2911 Codecs (Coder-Decoder) are the first members of a family of advanced Telecommunication components. High density LSI fabrication techniques are used allowing sample and hold, digital to analog converter, and comparitors to be integrated on a single chip along with digital logic necessary to interface a full duplex PCM (Pulse Code Modulation) link.

The 2912 Line Filters are designed to interface directly to the Codecs to perform the filtering function required in PCM Systems. The 2912 is a fully integrated monolithic device that contains the transmit and receive filters, a 50/60 Hertz notch, power amplifiers, and features necessary to interface directly to the Codec.

The primary applications of the Codecs and Filters are in telephone systems for the transmission, switching and concentration of voice communications in PCM Systems.

TABLE OF CONTENTS

2910 PCM CODEC — μLAW 6-3
2911 PCM CODEC — A LAW 6-14
2912 PCM LINE FILTERS 6-26

2910
PCM CODEC-μLAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G733 Compatible. ATT T1 Compatible with 8th Bit Signaling**
- **Microcomputer Interface with On-Chip Time-Slot Computation**
- **78dB Dynamic Range, with Resolution Equivalent to 12-Bit Linear Conversion Around Zero**
- **$\pm$5% Power Supplies: +12V, +5V, -5V**
- **Precision On-Chip Voltage Reference**
- **Low Power Consumption 230mW Typ. Standby Power 110mW Typ.**
- **All Digital Inputs and Outputs TTL Compatible**
- **Fabricated with Reliable N-Channel MOS Process**

TELECOM

The Intel® 2910 is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link and provide in-band signaling.

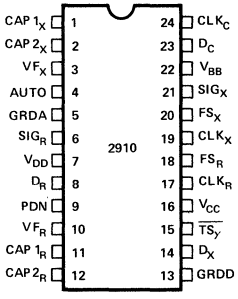
The primary applications are in telephone systems:

- Transmission — T1 Carrier
- Switching — Digital PBX's and Central Office Switching Systems
- Concentration — Subscriber Carrier/Concentrators

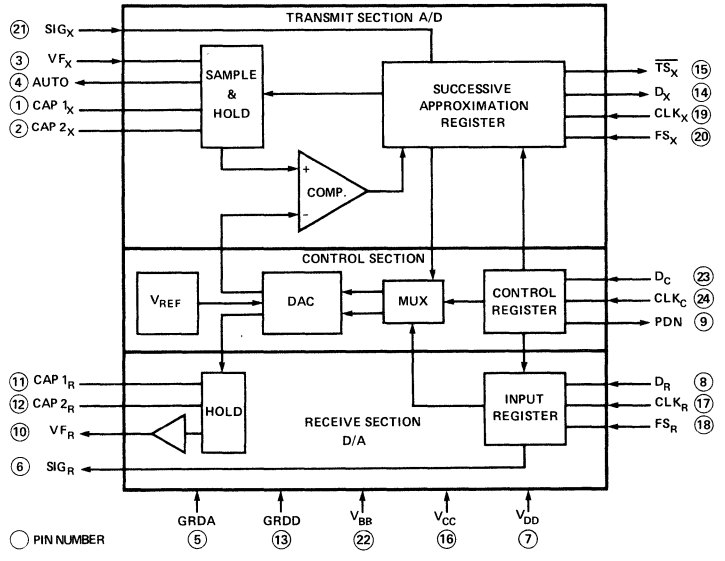
The wide dynamic range of the 2910 (78dB) and the minimal conversion time (80 μsec minimum) make it an ideal product for other applications, like:

- Data Acquisition
- Telemetry
- Secure Communications Systems
- Signal Processing Systems

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Function	Description
1	$CAP1_X$	Hold	Connections for the transmit holding capacitor. Refer to Applications Section.
2	$CAP2_X$		
3	VF_X	Input	Analog input to be encoded into a PCM word. The signal on this lead is sampled at the same rate as the transmit frame synchronization pulse FS_X, and the sample value is held in the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads until the encoding process is completed.
4	AUTO	Output	Most significant bit of the encoded PCM word (+5V for negative, -5V for positive inputs). Refer to the Codec Applications section.
5	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally.
6	SIG_R	Output	Signaling output SIG_R is updated with the 8th bit of the receive PCM word on signaling frames, and is latched between two signaling frames. TTL interface.
7	V_{DD}	Power	+12V, ±5%; referenced to GRDD or GRDA, depending upon system grounding considerations.
8	D_R	Input	Receive PCM highway (serial bus) interface. The Codec serially receives a PCM word (8-bits) through this lead at the proper time defined by FS_R, CLK_R, D_C, and CLK_C.
9	PDN	Output	Active high when Codec is in the power down state. TTL interface. Open drain output.
10	VF_R	Output	Analog output. The voltage present on VF_R is the decoded value of the PCM word received on lead D_R. This value is held constant between two conversions.
11	$CAP1_R$	Hold	Connections for the receive holding capacitor. Refer to the Applications section.
12	$CAP2_R$		
13	GRDD	Ground	Ground return common to the DC power supplies; V_{BB}, V_{CC}, and V_{DD}.
14	D_X	Output	Output of the transmit side onto the send PCM highway (serial bus). The 8-bit PCM word is serially sent out on this pin at the proper time defined by FS_X, CLK_X, D_C, and CLK_C. TTL three-state output.
15	$\overline{TS_X}$	Output	Normally high, this signal goes low while the Codec is transmitting an 8-bit PCM word on the D_X lead. (Time-slot information used for diagnostic purposes and also to gate the data on the D_X lead.) TTL interface, open drain output.
16	V_{CC}	Power	+5V, ±5%, referenced to GRDD.
17	CLK_R	Input	Master receive clock defining the bit rate on the receive PCM highway. Typically 1.544 Mbps for a T1 carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.
18	FS_R	Input	Frame synchronization pulse for the receive PCM highway. Resets the on-chip time slot counter for the receive side. Maximum repetition rate 12 KHz. Also used to differentiate between non-signaling frames and signaling frames for the receive side. TTL interface.
19	CLK_X	Input	Master transmit clock defining the bit rate on the transmit PCM highway. Typically 1.544 Mbps for a T1 carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.
20	FS_X	Input	Frame synchronization pulse for the transmit PCM highway. Resets the on-chip time slot counter for the transmit side. Maximum repetition rate 12 KHz. Also used to differentiate between non-signaling frames on the transmit side.
21	SIG_X	Input	Signaling input. This digital input is transmitted as the 8th bit of the PCM word on the D_X lead, on signaling frames. TTL interface.
22	V_{BB}	Power	-5V, ±5%, referenced to GRDD or GRDA, depending upon system grounding considerations.
23	D_C	Input	Data input to program the Codec for the chosen mode of operation. TTL interface.
24	CLK_C	Input	Clock input to clock in the data on the D_C lead in order to define the mode of operation of the Codec. TTL interface.

FUNCTIONAL DESCRIPTION

The 2910 PCM Codec provides the analog-to-digital and the digital-to-analog conversions necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system.

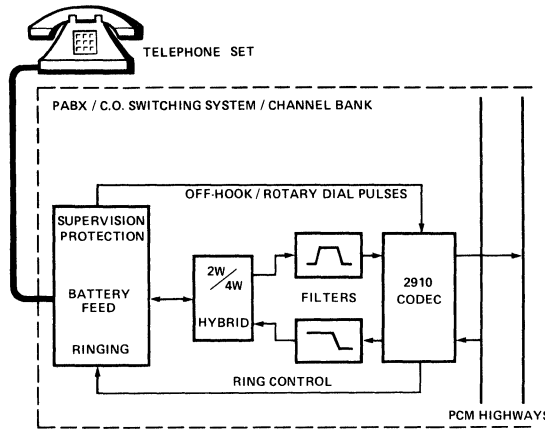
In a typical telephone system the Codec is used between the PCM highways and the line filters.

The Codec provides two major functions:

- Encoding and decoding of analog signals (voice and call progress tones)
- Encoding and decoding of the signaling and supervision information

On a non-signaling frame, the Codec encodes the incoming analog signal at the frame rate (FS_X) into an 8-bit PCM word which is sent out on the D_X lead at the proper time. Similarly, on a non-signaling frame of the receive link, the Codec fetches an 8-bit PCM word from the receive highway (D_R lead) and decodes an analog value which will remain constant on lead VF_R until the next receive frame. Transmit and receive frames are independent. They can be asynchronous (transmission) or synchronous (switching) with each other.

On a signaling frame, the Codec transmit side will encode the incoming analog signal as previously described and substitute the signal present on lead SIG_X for the least significant bit of the encoded PCM word. Similarly, on a receive signaling frame, the Codec will decode the 7 most significant bits according to the CCITT G733 recommendation and will output the least significant bit value on the SIG_R lead until the next signaling frame. Signaling frames on the send and receive sides are independent of each other.



Typical line Termination

The 2910 Codec is intended to be used on line and trunk terminations. The call progress tones (dial tone, busy tone, ring-back tone, re-order tone), and the pre-recorded announcements, can be sent through the voice-path, while signaling (off hook and disconnect supervision, rotary dial pulses, ring control) is sent through the signaling path.

Circuitry is provided within the Codec to internally define the transmit and receive time-slots in order to minimize the common equipment. This feature can be bypassed and discrete time-slots sent to each Codec within a system.

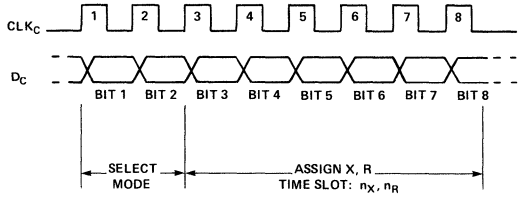
In the power-down mode, most functions of the Codec are disabled to reduce power dissipation to a minimum.

TELECOM

CODEC OPERATION

Codec Control

The operation of the 2910 is defined by serially loading an 8-bit word through the D_C lead (data) and the CLK_C lead (clock). The loading is asynchronous with the other operations of the Codec, and takes place whenever transitions occur on the CLK_C lead. The D_C input is loaded in during the trailing edge of the CLK_C input.



The control word contains two fields:

Bit 1 and Bit 2 define whether the subsequent 6 bits apply to both the transmit and receive side (00), the transmit side only (01), the receive side only (10) or whether the Codec should go into the standby, power-down mode (11). In the latter case (11), the following 6 bits are irrelevant.

The last 6 bits of the control word define the time-slot assignment, from 000000 (time-slot 1) to 111111 (time-slot 64). Bit 3 is the most significant bit and bit 8 the least significant bit and last into the Codec.

Bit 1	Bit 2	Mode
0	0	X & R
0	1	X
1	0	R
1	1	Standby

Bit 3 8	Time Slot
0 0 0 0 0 0	1
0 0 0 0 0 1	2
.	.
.	.
.	.
.	.
1 1 1 1 1 1	64

The Codec will retain the control word (or words) until a new word is loaded in or until power is lost. This feature permits dynamic allocation of time-slots for switching applications.

Microcomputer Control Mode

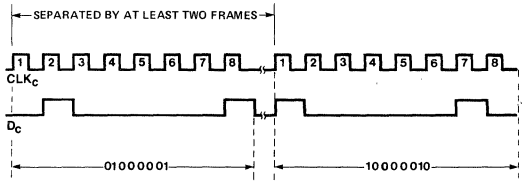
In the microcomputer mode, each Codec performs its own time-slot computation independently for the transmit and receive channels by counting clock pulses (CLK_X and CLK_R). All Codec's tied to the same data bus receive identical framing pulses (FS_X and FS_R). The framing pulses reset the on-chip time-slot counters every frame; hence the time-slot counters of all devices are synchronized. Each Codec is programmed via CLK_C and D_C for the desired transmit and receive time-slots according to the description in the Codec Control Section. All Codec's tied to the same D_R bus will, in general, have different receive time-slots, although that is not a device requirement. There may be separate busses for transmit and receive or all Codec's may transmit and receive over the same bus, in which case the transmit and receive channels must be synchronous ($CLK_X = CLK_R$). There are no other restrictions on time-slot assignments; a device may have the same transmit and receive timeslot even if a single bus is used.

There are several requirements for using the CLK_C-D_C interface in the microcomputer mode.

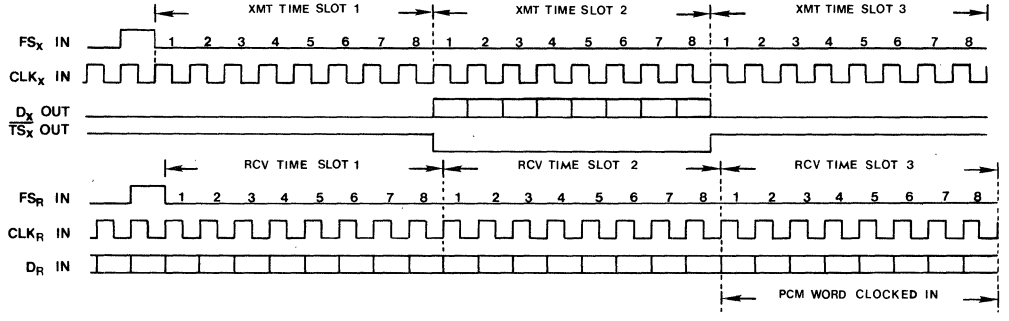
1. A complete time-slot assignment, consisting of eight negative transitions of CLK_C, must be made in less than one frame period. The assignment can overlap a framing pulse so long as all 8 control bits are clocked in within a total span of 125 μsec (for an 8KHz frame rate). CLK_C must be left at a TTL low level when not assigning a time-slot.
2. A dead period of two frames must always be observed between successive time-slot assignments. The two frame delay is measured from the rising edge of the first CLK_C transition of the previous time-slot assigned.
3. When the device is in the power-down state, an initialization time-slot assignment is required prior to the assignment of the desired time-slots. That is, the first assignment brings the device out of power-down but does not register the time-slot information in the lower six bits of the control word. Once the initialization time-slot assignment has been completed, the desired time-slots may be assigned according to the descriptions above. The two frame delay between the initialization and the time-slot assignment must be observed.

Example of Microcomputer Control Mode:

The two words 01000001 and 10000010 have been loaded into the Codec. The transmit side is now programmed for time-slot 2 and the receive side for time-slot 3. The Codec will output a PCM word on the transmit PCM highway (bus) during the time-slot 2 of the transmit frame, and will fetch a PCM word from the receive PCM highway during time-slot 3.



In this example the Codec interface to the PCM highway then functions as shown below (FS_X and FS_R may be asynchronous).



Direct Control Mode

In the Direct Mode, unlike the microcomputer mode, the Codec time-slots bear a fixed phase relationship to the framing pulses (FS_X, FS_R). Frame pulses become time-slot strobes. Devices tied to the same D_X bus must get different FS_X pulses; all devices tied to the same D_R bus will, in general, receive different FS_R pulses, although that is not a device requirement. Again the D_X and D_R busses may be the same bus in synchronous systems, and there are no restrictions on the relationship between the transmit and receive time-slots of a given Codec. The direct mode is a special case of the microcomputer mode in that the device always operates in the first time-slot and hence transmits and receives its data in the eight clock periods which begin with the first clock (CLK_X or CLK_R) rising edge following the rising edge of the framing pulse (FS_X or FS_R). That is, bit 1 of each time-slot is delayed one clock cycle from the leading edge of the respective framing pulse.

The essential difference between the direct mode and microcomputer mode is that in the direct mode, the control words always consist either of all 1's (for assigning power-down) or all 0's (for powering up the device and assigning the first time-slot). Hence there are fewer timing constraints on D_C and CLK_C. In particular, it is possible to define a continuous clock which can be tied to CLK_C and

which makes the device behave as if the D_C lead is an active low chip select. Whenever selected, the device assumes the first time-slot in both the transmit and receive directions. The characteristics of the continuous clock used for CLK_C are:

a) The clock must contain at least 8 pulses per frame.

b) The transitions must occur only during the 8th bit of any transmit time-slot. CLK_C transitions may not occur during the first through seventh bits of any transmit time-slot. This requirement is unique to the case when the direct mode is implemented with a continuous clock on CLK_C. Commonly, the external timing circuitry which is used to generate the time-slot strobes for the direct mode control, will contain a clock which marks the 8th bit of each transmit time-slot (for example, a signaling bit marker).

c) The microcomputer mode requirement that successive time-slot assignments be separated by two frames does not apply when a continuous clock with these characteristics is used for CLK_C.

General Control Requirements

All bit and frame clocks should be applied whenever the device is active. In particular, an unused channel cannot be de-activated by removal of its associated frame or bit clock while the other channel of the same device remains active. A single channel can be removed from service in the microcomputer mode by assigning an excess time-slot to that channel.

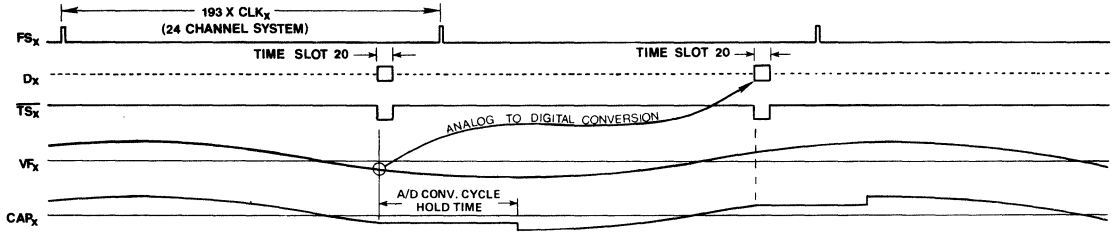
Since the time-slot counters contain 6-bits they can count to 64 time-slots. Therefore, a channel assigned an excess time-slot (e.g. time-slot 48 in a 32 channel system) will remain idle.

A single channel cannot be deactivated in the direct control mode except by physical disconnection of the data lead (D_X or D_R) from the system data bus. A device (both transmit and receive channels) may be de-activated in either control mode by powering down the device. Both channels are always powered down together.

TELECOM

Encoding

The VF signal to be encoded is input on the VF_X lead. An internal switch samples the signal and the hold function is performed by the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads. The sampling and conversion is synchronized with the transmit time-slot (worst case conversion time is 20 time-slots). The PCM word is then output on the D_X lead at the proper time-slot occurrance of the following frame. The A/D converter saturates at approximately ±2.2 volts rms (±3.1 volts peak).



Decoding

The PCM word is fetched by the D_R lead from the PCM highway at the proper time-slot occurrence. The decoded value is held on the external capacitor connected to the $CAP1_R$ and $CAP2_R$ leads.

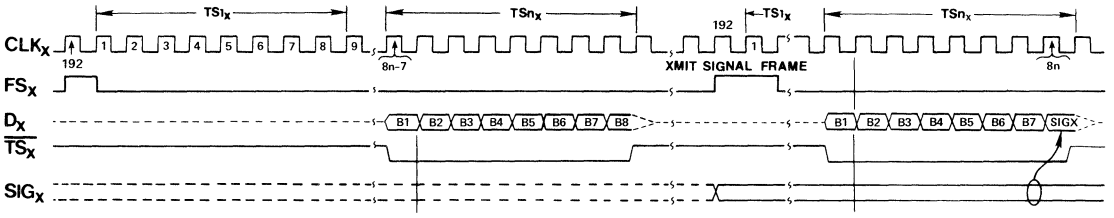
The buffered non-return to zero output signal on the VF_R lead is equal to the stored voltage on CAP_R. The output signal on lead VF_R has a dynamic range of approximately ±2.2 volts rms (±3.1 volts peak).

Signaling

The duration of the FS_X and FS_R pulses defines whether a frame is an information frame or a signaling frame:

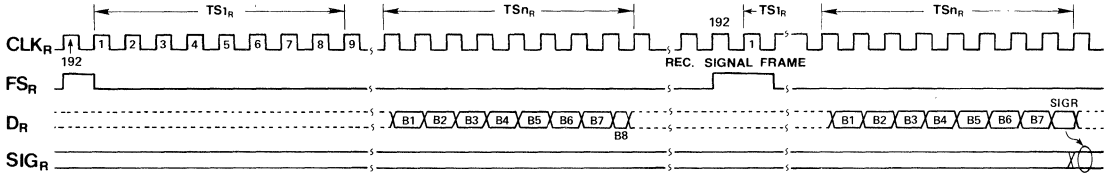
- A frame synchronization pulse which is a full clock period in duration (CLK_X period for FS_X, CLK_R period for FS_R) designates a non-signaling frame.
- A frame synchronization pulse which is two full clock periods in duration (two CLK_X periods for FS_X, two CLK_R periods for FS_R) designates a signaling frame.

On the encoding side, when the FS_X pulse is widened, the 8th bit of the PCM word will be replaced by the value on the SIG_X input at the time when the 8th bit is output on the D_X lead.



On the decoding side, when the FS_R pulse is widened, the 8th bit of the PCM word is detected and transmitted on the SIG_R lead. That output is latched until the next receiving signaling frame.

The remaining 7-bits are decoded according to the value given in the CCITT G733 recommendation. The SIG_R lead is reset to a TTL low level whenever the Codec is in the power-down state.



D3 Framing

The number of clock pulses (CLK_X, CLK_R) delivered to the Codec per frame must be a multiple of 8. In the case of the D3 framing format (193 bits/frame), one clock pulse per frame must be suppressed (blanked) from the 1.544 Mb/s bit clocks CLK_X and CLK_R. It is generally easiest to blank the framing (193rd) bit in both cases. This pulse suppression may be performed once at the system level, with the same bit clock distributed to all Codec's, whether the microcomputer control mode or the direct control mode is employed.

The framing pulse widths are always defined relative to Codec bit clock transitions; whenever a pulse is blanked in a Codec bit clock, any framing pulse which spans that blanked bit clock interval must be extended beyond the next bit clock transition.

Standby Mode — Power Down

To minimize power consumption and dissipation in large systems, a standby mode is provided by loading a control word (D_C) with a "1" in bits 1 and 2 locations. Most of the Codec functions thereby become disabled, with the exception of the interface to the D_C and CLK_C leads, to allow the Codec to be reactivated.

The power consumption in the standby mode is typically 110mW.

Power-On Clear

Whether the device is used in the direct or microcomputer mode, an internal reset (power-on clear) is generated whenever either of the two positive device power supplies (V_{DD} or V_{CC}) are removed or applied. The Codec thus assumes the power-down state upon application of the positive power supplies and must be initialized in the normal way for operation.

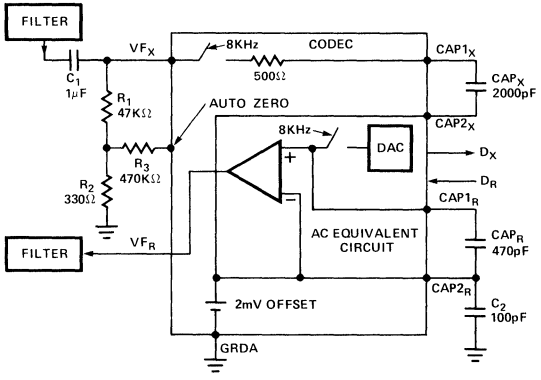
Precision Voltage Reference for the D/A Converter

The voltage reference is generated on the chip and is calibrated during the manufacturing process. The technique uses the difference in sub-surface charge density between two suitably implanted MOS devices to derive a temperature stable and bias stable reference voltage.

A gain setting op amp, programmed during manufacturing, "trims" the reference voltage source to the final precision voltage reference value provided to the D/A converter. The precision voltage reference determines the initial gain and dynamic range characteristics described in the A.C. Transmission Specification Section.

APPLICATIONS

Circuit Interface



Holding Capacitors

For an 8KHz sampling system the transmit holding capacitor CAP_X should be 2000pF, 20%. The receive holding capacitor CAP_R should be 470pF, 20% for 32 time-slots and 8KHz sample rate or 560pF, 20% for 24 time-slots and 8KHz sample rate. An additional capacitor C_2 of 100pF, is required from the $CAP2_R$ lead to GRDA.

Auto Zero

The auto zero output (most significant bit or sign bit of the A/D conversion) integrated over a long time constant will compensate for the DC offset inside the Codec (voltage difference between the bottom of the DAC and GRDA). The above drawing shows a possible connection between the VF_X and Auto leads. The recommended values of the auto zero components are:

C_1 of 1μF, R_1 of 47kΩ, R_2 of 330Ω, and R_3 of 470kΩ.

Filters Interface

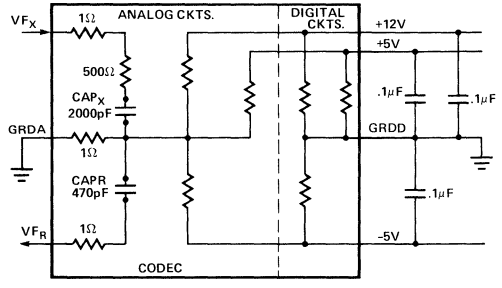
The filters may be interfaced as shown in the circuit interface diagram. Note that the output pulse stream is of the non-return to zero type.

D_X Buffering

For optimum idle channel noise performance it is recommended that the D_X output of each Codec be buffered from the system PCM bus with an external three-state or open collector buffer. Each buffer can be enabled with the appropriate Codec generated $\overline{TS_X}$ signal. The $\overline{TS_X}$ signal may be used to activate zero code suppression logic on the PCM bus.

TELECOM

Grounding and Decoupling Recommendations



Grounding

Analog grounding is connected to the GRDA lead. The GRDA and GRDD leads are not connected inside the 2910. An external connection is thus necessary outside the Codec to tie all the analog ground lines to the common return of the system GRDD.

To minimize the injection of digital logic noise into the analog signal path the GRDA and GRDD external connection should be made as close as practical to the system supply ground.

Decoupling

A 0.1μF bypassing capacitor from each power supply to digital ground is generally recommended at each device. This decoupling may be reduced based on actual board design and performance.

Sufficient board level decoupling must be provided to guarantee that power supply transients (including turn on and off) do not exceed the absolute maximum ratings of the device. A minimum of 1μF is recommended once per board for each power supply. A pair of small switching diodes (in opposite directions) between analog and digital ground on a once-per-board basis is recommended to maintain the two ground levels near the same value during board insertion and removal.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
All Input or Output Voltages
with Respect to V_{BB} ..... -0.3 to +20V
V_{CC}, V_{DD} and V_{SS} with
Respect to V_{BB} ..... -0.3 to +20V
Power Dissipation 1.35W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

DIGITAL INTERFACE

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{IL}	Low Level Input Current			10	μA	$V_{IN} < V_{IL}$
I_{IH}	High Level Input Current			10	μA	$V_{IN} > V_{IH}$
V_{IL}	Input Low Voltage			+0.6	V	
V_{IH}	Input High Voltage	+2.2			V	
V_{OL}	Output Low Voltage			0.4	V	D_X, I_{OL}=3.2mA
						SIG_R, I_{OL}=0.5mA
						$\overline{TS_X}$, I_{OL}=1.6mA, open drain
						PDN, I_{OL}=0.5mA, open drain
V_{OH}	Output High Voltage	2.4			V	D_X, I_{OH}=30mA
						SIG_R, I_{OH}=0.6mA

ANALOG INTERFACE

A_{IZ}	Input Impedance when Sampling, VF_X	125	300	500	Ω	In Series with CAP_X to GRDA, -3.1V < V_{IN} < 3.1V
A_{OZ}	Output Impedance, VF_R	100	180	300	Ω	-3.1V < V_{OUT} < 3.1V
V_{OL}	Output Low Voltage, Auto		V_{BB}	V_{BB}	V	400kΩ to GRDA
V_{OH}	Output High Voltage, Auto	V_{CC}	V_{CC}		V	
R_1	Auto Zero Component	42	47	52	kΩ	47kΩ Recommended[2]
R_2	Auto Zero Component	290	330	360	Ω	330Ω Recommended[2]
R_3	Auto Zero Component	420	470	520	kΩ	470kΩ Recommended[2]
C_1	Auto Zero Component	1.0			μF	
CAP_X	Holding Capacitor, Transmit	1600	2000	2400	pF	8kHz Sampling, 2000pF Recommended[2]
CAP_R	Holding Capacitor, Receive	390	470	560	pF	8kHz Sampling, 32 Time-Slots, 470pF Recommended[2]
		450	560	670	pF	8kHz Sampling, 24 Time-Slots, 560pF Recommended[2]
C_2	Bypass Capacitor	80		120	pF	100pF Recommended[2]

POWER DISSIPATION

I_{DDO}	Standby Current		6	9	mA	V_{DD} = 12.6V V_{CC} = 5.25V V_{BB} = -4.75V Clock Frequency 2.048MHz
I_{CCO}	Standby Current		5	8	mA	
I_{BBO}	Standby Current		2	4	mA	
I_{DDI}	Operating Current		11	16	mA	
I_{CCI}	Operating Current		13	21	mA	
I_{BBI}	Operating Current		4	6	mA	

NOTES: 1. Typical Values are for T_A = 25°C and nominal power supply values.
2. See Applications Circuit Interface for component connections.

A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

TRANSMISSION (Any two 2910 Codec's, end-to-end)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
S/D	Signal/Total Distortion Ratio, C-message Weighted (See Figure 1)	Fig. 1	Fig. 1		dB	V_{FX}=1.02KHz, Sinusoid
ΔG	Gain Tracking Error (See Figure 2)	-0.3		0.3	dB	V_{FX}=1.02KHz Sinusoid -37dBm0≤V_{FX}<0dBm0
		-0.7		0.7	dB	-50dBm0≤V_{FX}<-37dBm0
		-2.1		2.1	dB	-55dBm0≤V_{FX}<-50dBm0
N_{IC1}	Idle Channel Noise, C-message Weighted		8	14	dBrnc0	With Auto-Zero, No Signaling[2]
N_{IC2}	Idle Channel Noise, C-message Weighted		10	16	dBrnc0	With Auto-Zero; with 6th and 12th Frame Signaling
HD	Harmonic Distortion (2nd or 3rd)		-48	-44	dB	V_{FX}=1.02KHz, 0dBm0; Measured at Decoder Output, V_{FR}

Notes:
1. Typical Values are for $T_A = 25°C$ and nominal power supply values.
2. If all Auto-Zero components are removed and VF_X is direct coupled, the encoder tends to bias itself away from a decision level (hysteresis). The idle channel noise is then typically 2 dBrnc0, but will be dependent on the D.C. offset of the PCM transmit filter output provided to VF_X.

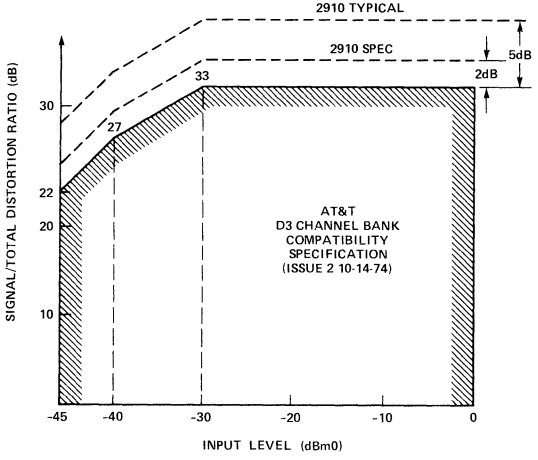


Figure 1. Signal/Total Distortion Ratio.

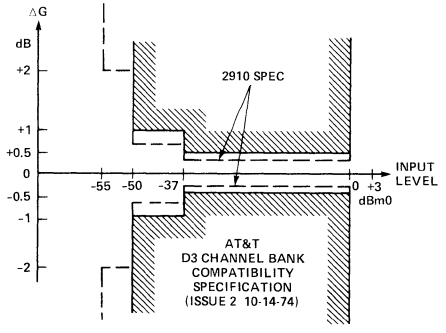


Figure 2. Gain Tracking Error (ΔG) vs. Signal Level Reference Level 0dBm0.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Limits			Units	Comments
		Min.	Typ.[1]	Max.		
DmW	Digital Milliwatt Response	5.55	5.63	5.71	dBm	23°C, Nominal Supplies[2]
DmW_T	DmW_0 Variation with Temperature		-.0005	-.0009	dB/°C	Relative to 23°C[2]
DmW_S	DmW_0 Variation with Supplies			±.07	dB	Supplies ±5%[2]
A_{OR}	Output Dynamic Range, VF_R	2.14	2.16	2.18	V_{RMS}	23°C, Nominal Supplies
A_{ORT}	A_{OR} Variation with Temperature			-.22	mV_{RMS}/°C	Relative to 23°C
A_{ORS}	A_{OR} Variation with Supplies			±18	mV_{RMS}	Supplies ±5%
G_{SL}	Self Loop Gain	-.24	-.20	-.16	dB	V_{FX}=-dBm0, 1.02KHz[3]
G_{EE}	End-to-End Codec Gain	-.4	-.3	-.2	dB	23°C, Nominal Supplies[4]
G_{EET}	G_{EE} Variation with Temperature		.0010	.0018	dB/°C	Relative to 23°C[4]
G_{EES}	G_{EE} Variation with Supplies		±.07	±.13	dB	Supplies ±5%[4]
G_{FR}	Decoder Frequency Response Departure from Ideal (Sinx)/x, VF_R			±.05	dB	300 Hz < f < 3800 Hz V_{FX} = 0dBm0[5]

SUPPLY REJECTION AND CROSSTALK

$PSRR_1$	V_{DD} Power Supply Rejection Ratio	50	60		dB	Encoder Alone[6]
$PSRR_2$	V_{BB} Power Supply Rejection Ratio	50	60		dB	Encoder Alone[6]
$PSRR_3$	V_{CC} Power Supply Rejection Ratio	50	80		dB	Encoder Alone[6]
$PSRR_4$	V_{DD} Power Supply Rejection Ratio	40	50		dB	Digital Loop Back[7]
$PSRR_5$	V_{BB} Power Supply Rejection Ratio	40	45		dB	Digital Loop Back[7]
$PSRR_6$	V_{CC} Power Supply Rejection Ratio	50	80		dB	Digital Loop Back[7]
CT	Cross Talk Isolation	75	>80		dB	Note 8

NOTES:
1. Typical Values are for T_A = 25°C and nominal power supply values.
2. D_R of Device Under Test (D.U.T.) driven with repetitive digital word sequence specified in CCITT recommendation G.711. Measurement made at VF_R output.
3. D.U.T. acts as both encoder and decoder (D_X=D_R) in a digital loop-back configuration. Specified gain is in addition to normal (Sinx)/x insertion loss.
4. Any 2910 as encoder; any other 2910 as decoder; both D.U.T.'s with separate supplies and at independent temperatures. Specified gain is in addition to normal (Sinx)/x insertion loss.
5. (Sinx)/x with $x = \frac{\text{Measurement Frequency } (f) \times \pi}{\text{Sampling Frequency}}$
6. D.U.T. Encoder; impose 200mV p-p, 1.02KHz on appropriate supply; measurement made at remote decoder output; encoder in idle channel conditions.
7. D.U.T. acts as encoder and decoder; impose 200mV p-p, 1.02KHz on appropriate supply; measurement made at co-located decoder output; encoder in idle channel conditions.
8. V_{FX} of D.U.T. encoder = 1.02KHz, 0dBm0. Co-located D.U.T. decoder under quiet channel conditions; measurement made at co-located decoder output.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

TIMING SPECIFICATION

CLOCK SECTION

Symbol	Parameter	Limits Min.	Limits Max.	Units	Comments
t_{CY}	Clock Period	485		ns	CLK_X, CLK_R (2.048MHz systems), CLK_C
t_r, t_f	Clock Rise and Fall Time	5	30	ns	CLK_X, CLK_R, CLK_C
t_{CLK}	Clock Pulse Width	215		ns	CLK_X, CLK_R, CLK_C
t_{CDC}	Clock Duty Cycle ($t_{CLK} \div t_{CY}$)	45	55	%	CLK_X, CLK_R

TRANSMIT SECTION

t_{VFX}	Analog Input Conversion	20		Time Slot	From Leading Edge of Transmit Time Slot[1]
t_{DZX}	Data Enabled on TS Entry	50	180	ns	$0 < C_{LOAD} < 100pF$
t_{DHX}	Data Hold Time	80	230	ns	$0 < C_{LOAD} > 100pF$
t_{HZX}	Data Float on TS Exit	75	205	ns	$C_{LOAD} = 0$
t_{SON}	Time Slot X to Enable	30	220	ns	$0 < C_{LOAD} < 100pF$
t_{SOFF}	Time Slot X to Disable	70	185	ns	$C_{LOAD} = 0$
t_{SS}	Signal Setup Time	0		ns	Relative to Bit-7 Falling Edge
t_{SH}	Signal Hold Time	100		ns	Relative to Bit-8 Falling Edge
t_{FSD}	Frame Sync Delay	15	100	ns	FS_X

RECEIVE AND CONTROL SECTIONS

t_{VFR}	Analog Output Update	6	6	Time Slot	From the Leading Edge of the Channel Time Slot
t_{DSR}	Receive Data Setup	20		ns	
t_{DHR}	Receive Data Hold	50		ns	
t_{SIGR}	SIG_R Update		300	ns	From the Trailing Edge of the Channel Time Slot
t_{FSD}	Frame Sync Delay	15	100	ns	
t_{DSC}	Control Data Setup	100		ns	
t_{DHC}	Control Data Hold	100		ns	

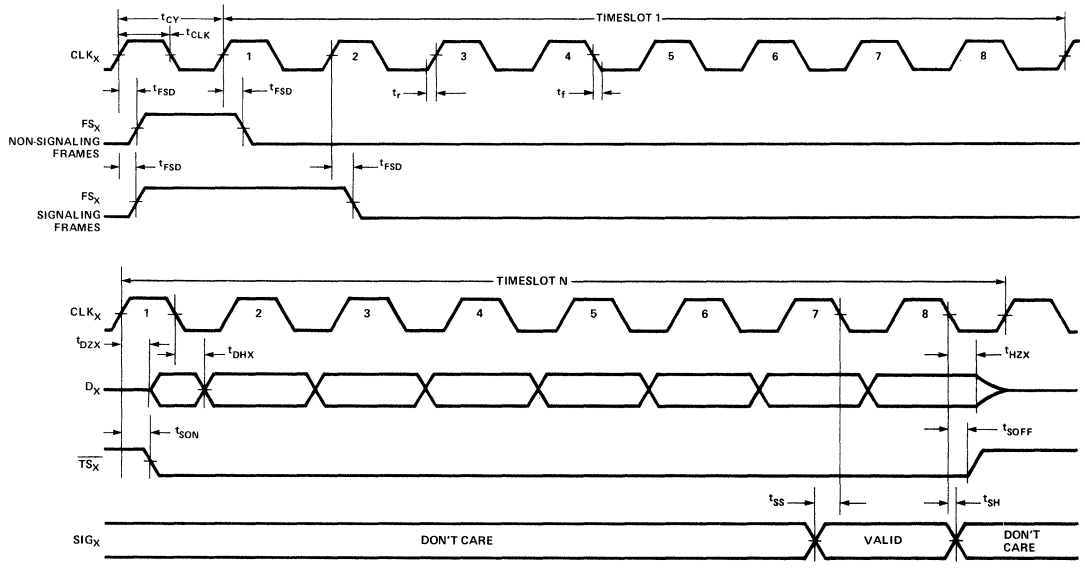
NOTE:

1. The 20 time slot minimum insures that the complete A/D conversion will take place under any combination of receive interrupt or asynchronous operation of the Codec. If the transmit channel only is operated the A/D conversion can be completed in a minimum of 11 time slots. Refer to the Codec Control General Requirement section for instructions on setting a channel in an idle condition.

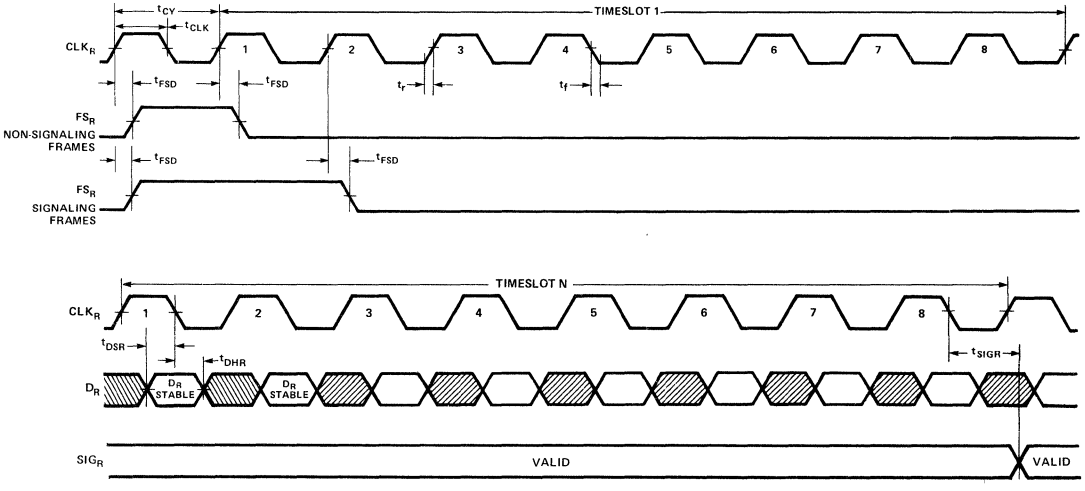
TELECOM

TIMING WAVEFORMS[1]

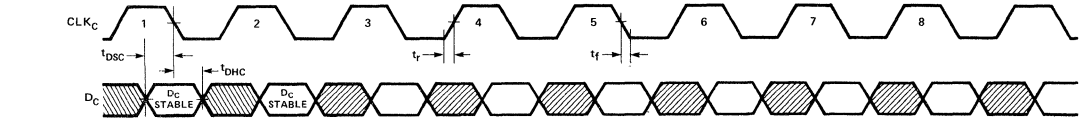
TRANSMIT TIMING



RECEIVE TIMING



CONTROL TIMING



Notes: 1. All timing parameters referenced to 2.0V, except t_{HZX} and t_{SOFF} which reference a high impedance state.

2911
PCM CODEC — A LAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G732 Compatible. Even Order Bits Inversion Included**
- **Microcomputer Interface with On-Chip Time-Slot Computation**
- **66dB Dynamic Range, with Resolution Equivalent to 11-Bit Linear Conversion Around Zero**
- **±5% Power Supplies: +12V, +5V, -5V**
- **Precision On-Chip Voltage Reference**
- **Low Power Consumption: 230mW Typ. Standby Power: 110mW Typ.**
- **All Digital Inputs and Outputs TTL Compatible**
- **Fabricated with Reliable N-Channel MOS Process**

TELECOM

The Intel® 2911 is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link.

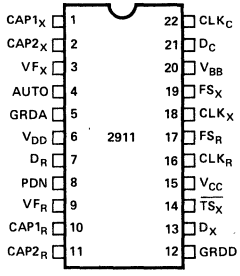
The primary applications are in telephone systems:

- Transmission — 30/32 Channel Systems at 2.048 Mbps
- Switching — Digital PBX's and Central Office Switching Systems
- Concentration — Subscriber Carrier/Concentrators

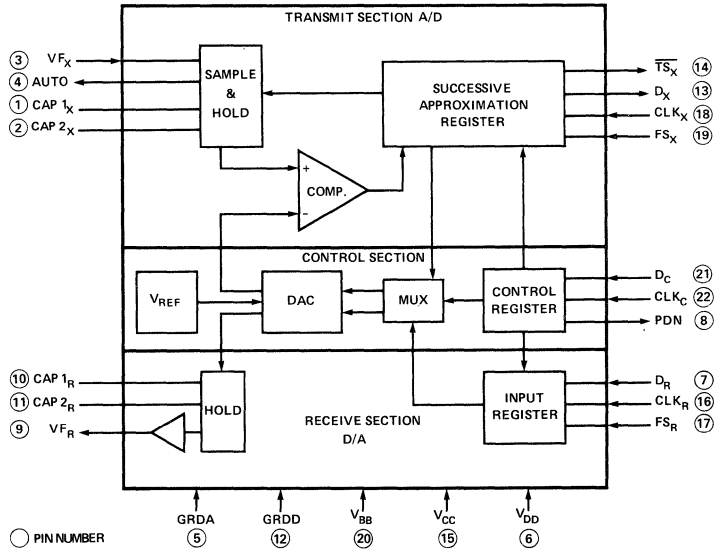
The wide dynamic range of the 2911 (66 dB) and the minimal conversion time (80 μsec minimum) make it an ideal product for other applications, like:

- Data Acquisition
- Telemetry
- Secure Communications Systems
- Signal Processing Systems

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Function	Description
1	$CAP1_X$	Hold	Connections for the transmit holding capacitor. Refer to Applications Section.
2	$CAP2_X$		
3	VF_X	Input	Analog input to be encoded into a PCM word. The signal on this lead is sampled at the same rate as the transmit frame synchronization pulse FS_X, and the sample value is held in the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads until the encoding process is completed.
4	AUTO	Output	Most significant bit of the encoded PCM word (+5V for negative, -5V for positive value). Refer to the Codec Applications Section.
5	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally.
6	V_{DD}	Power	+12V, ±5%, referenced to GRDD or GRDA, depending upon system grounding considerations.
7	D_R	Input	Receive PCM highway (serial bus) interface. The Codec serially receives a PCM word (8-bits) through this lead at the proper time defined by FS_R, CLK_R, D_C, and CLK_C.
8	PDN	Output	Active high when the Codec is in the power down mode. TTL interface. Open drain output.
9	VF_R	Output	Analog output. The voltage present on VF_R is the decoded value of the PCM word received on lead D_R. This value is held constant between two conversions.
10	$CAP1_R$	Hold	Connections for the receive holding capacitor. Refer to the Applications Section.
11	$CAP2_R$		
12	GRDD	Ground	Ground return common to the DC power supplies; V_{BB}, V_{CC}, and V_{DD}.
13	D_X	Output	Output of the transmit side onto the send PCM highway (serial bus). The 8-bit PCM word is serially sent out on this pin at the proper time defined by FS_X, CLK_X, D_C, and CLK_C. TTL three-state output.
14	$\overline{TS_X}$	Output	Normally high, this signal goes low while the Codec is transmitting an 8-bit PCM word on the D_X lead. (Time-slot information used for diagnostic purposes and also to gate the data on the D_X lead.) TTL interface, open drain output.
15	V_{CC}	Power	+5V, ±5%, referenced to GRDD.
16	CLK_R	Input	Master receive clock defining the bit rate on the receive PCM highway. Typically 2.048 Mbps for a carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL compatible.
17	FS_R	Input	Frame synchronization pulse for the receive PCM highway. Resets the on-chip time-slot counter for the receive side. Maximum repetition rate 12 kHz. TTL interface.
18	CLK_X	Input	Master transmit clock defining the bit rate on the transmit PCM highway. Typically 2.048 Mbps for a carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.

Pin No.	Symbol	Function	Description
19	FS_X	Input	Frame synchronization pulse for the transmit PCM highway. Resets the on-chip time-slot counter for the transmit side. Maximum repetition rate 12 kHz. TTL interface.
20	V_{BB}	Power	-5V, ±5%, referenced to GRDD or GRDA, depend-upon system grounding considerations.
21	D_C	Input	Data input to program the Codec for the chosen mode of operation. TTL interface.
22	CLK_C	Input	Clock input to clock in the data on the D_C lead in order to define the mode of operation of the Codec. TTL interface.

FUNCTIONAL DESCRIPTION

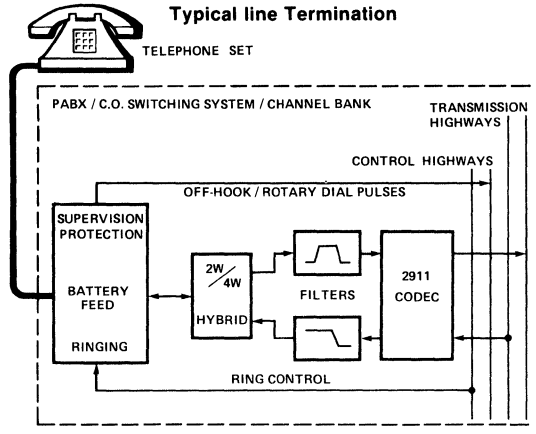
The 2911 PCM Codec provides the analog-to-digital and the digital-to-analog conversions necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. The Codec is intended to be used on line and trunk terminations.

In a typical telephone system the Codec is located between the PCM highways and the channel filters.

The Codec encodes the incoming analog signal at the frame rate (FS_X) into an 8-bit PCM word which is sent out on the D_X lead at the proper time. Similarly, on the receive link, the Codec fetches an 8-bit PCM word from the receive highway (D_R lead) and decodes an analog value which will remain constant on lead VF_R until the next receive frame. Transmit and receive frames are independent. They can be asynchronous (transmission) or synchronous (switching) with each other.

Circuitry is provided within the Codec to internally define the transmit and receive time-slots in order to minimize the common equipment. This feature can be bypassed

Typical line Termination



and discrete time-slots sent to each Codec within a system.

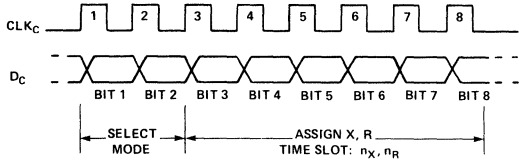
In the power-down mode, most functions of the Codec are disabled to reduce power dissipation to a minimum.

TELECOM

CODEC OPERATION

Codec Control

The operation of the 2911 is defined by serially loading an 8-bit word through the D_C lead (data) and the CLK_C lead (clock). The loading is asynchronous with the other operations of the Codec, and takes place whenever transitions occur on the CLK_C lead. The D_C input is loaded in during the trailing edge of the CLK_C input.



The control word contains two fields:

Bit 1 and Bit 2 define whether the subsequent 6 bits apply to both the transmit and receive side (00), the transmit side only (01), the receive side only (10) or whether the Codec should go into the standby, power-down mode (11). In the latter case (11), the following 6 bits are irrelevant.

The last 6 bits of the control word define the time-slot assignment, from 000000 (time-slot 1) to 111111 (time-slot 64). Bit 3 is the most significant bit and bit 8 the least significant bit and last into the Codec.

Bit 1	Bit 2	Mode
0	0	X & R
0	1	X
1	0	R
1	1	Standby

Bit 3 8	Time Slot
0 0 0 0 0 0	1
0 0 0 0 0 1	2
•	•
•	•
•	•
•	•
1 1 1 1 1 1	64

The Codec will retain the control word (or words) until a new word is loaded in or until power is lost. This feature permits dynamic allocation of time-slots for switching applications.

Microcomputer Control Mode

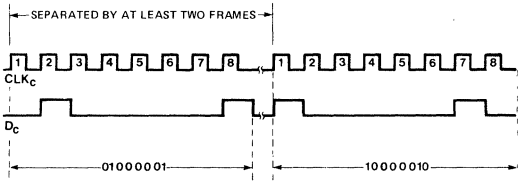
In the microcomputer mode, each Codec performs its own time-slot computation independently for the transmit and receive channels by counting clock pulses (CLK_X and CLK_R). All Codec's tied to the same data bus receive identical framing pulses (FS_X and FS_R). The framing pulses reset the on-chip time-slot counters every frame; hence the time-slot counters of all devices are synchronized. Each Codec is programmed via CLK_C and D_C for the desired transmit and receive time-slots according to the description in the Codec Control Section. All Codec's tied to the same D_R bus will, in general, have different receive time-slots, although that is not a device requirement. There may be separate busses for transmit and receive or all Codec's may transmit and receive over the same bus, in which case the transmit and receive channels must be synchronous ($CLK_X = CLK_R$). There are no other restrictions on time-slot assignments; a device may have the same transmit and receive timeslot even if a single bus is used.

There are several requirements for using the CLK_C-D_C interface in the microcomputer mode.

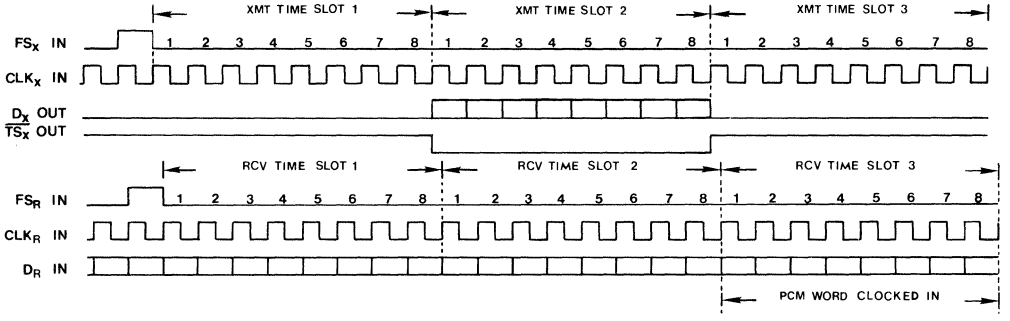
1. A complete time-slot assignment, consisting of eight negative transitions of CLK_C, must be made in less than one frame period. The assignment can overlap a framing pulse so long as all 8 control bits are clocked in within a total span of 125 μsec (for an 8KHz frame rate). CLK_C must be left at a TTL low level when not assigning a time-slot.
2. A dead period of two frames must always be observed between successive time-slot assignments. The two frame delay is measured from the rising edge of the first CLK_C transition of the previous time-slot assigned.
3. When the device is in the power-down state, an initialization time-slot assignment is required prior to the assignment of the desired time-slots. That is, the first assignment brings the device out of power-down but does not register the time-slot information in the lower six bits of the control word. Once the initialization time-slot assignment has been completed, the desired time-slots may be assigned according to the descriptions above. The two frame delay between the initialization and the time-slot assignment must be observed.

Example of Microcomputer Control Mode:

The two words 01000001 and 10000010 have been loaded into the Codec. The transmit side is now programmed for time-slot 2 and the receive side for time-slot 3. The Codec will output a PCM word on the transmit PCM highway (bus) during the time-slot 2 of the transmit frame, and will fetch a PCM word from the receive PCM highway during time-slot 3.



In this example the Codec interface to the PCM highway then functions as shown below (FS_X and FS_R may be asynchronous).



Direct Control Mode

In the Direct Mode, unlike the microcomputer mode, the Codec time-slots bear a fixed phase relationship to the framing pulses (FS_X, FS_R). Frame pulses become time-slot strobes. Devices tied to the same D_X bus must get different FS_X pulses; all devices tied to the same D_R bus will, in general, receive different FS_R pulses, although that is not a device requirement. Again the D_X and D_R busses may be the same bus in synchronous systems, and there are no restrictions on the relationship between the transmit and receive time-slots of a given Codec. The direct mode is a special case of the microcomputer mode in that the device always operates in the first time-slot and hence transmits and receives its data in the eight clock periods which begin with the first clock (CLK_X or CLK_R) rising edge following the rising edge of the framing pulse (FS_X or FS_R). That is, bit 1 of each time-slot is delayed one clock cycle from the leading edge of the respective framing pulse.

The essential difference between the direct mode and microcomputer mode is that in the direct mode, the control words always consist either of all 1's (for assigning power-down) or all 0's (for powering up the device and assigning the first time-slot). Hence there are fewer timing constraints on D_C and CLK_C. In particular, it is possible to define a continuous clock which can be tied to CLK_C and

which makes the device behave as if the D_C lead is an active low chip select. Whenever selected, the device assumes the first time-slot in both the transmit and receive directions. The characteristics of the continuous clock used for CLK_C are:

a) The clock must contain at least 8 pulses per frame.

b) The transitions must occur only during the 8th bit of any transmit time-slot. CLK_C transitions may not occur during the first through seventh bits of any transmit time-slot. This requirement is unique to the case when the direct mode is implemented with a continuous clock on CLK_C. Commonly, the external timing circuitry which is used to generate the time-slot strobes for the direct mode control, will contain a clock which marks the 8th bit of each transmit time-slot (for example, a signaling bit marker).

c) The microcomputer mode requirement that successive time-slot assignments be separated by two frames does not apply when a continuous clock with these characteristics is used for CLK_C.

General Control Requirements

All bit and frame clocks should be applied whenever the device is active. In particular, an unused channel cannot be de-activated by removal of its associated frame or bit clock while the other channel of the same device remains active. A single channel can be removed from service in the microcomputer mode by assigning an excess time-slot to that channel.

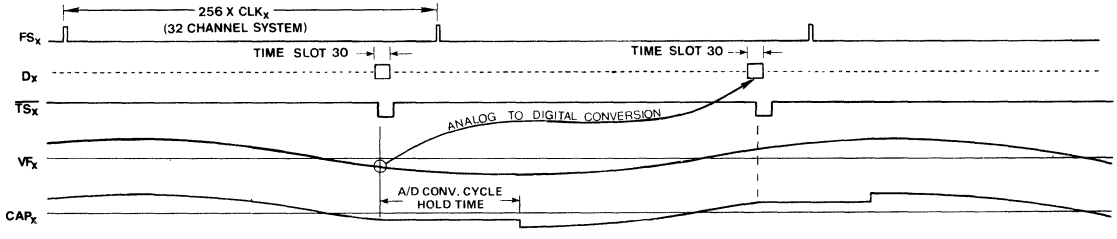
Since the time-slot counters contain 6-bits they can count to 64 time-slots. Therefore, a channel assigned an excess time-slot (e.g. time-slot 48 in a 32 channel system) will remain idle.

A single channel cannot be deactivated in the direct control mode except by physical disconnection of the data lead (D_X or D_R) from the system data bus. A device (both transmit and receive channels) may be de-activated in either control mode by powering down the device. Both channels are always powered down together.

TELECOM

Encoding

The VF signal to be encoded is input on the VF_X lead. An internal switch samples the signal and the hold function is performed by the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads. The sampling and conversion is synchronized with the transmit time-slot (worst case conversion time is 20 time-slots). The PCM word is then output on the D_X lead at the proper time-slot occurrance of the following frame. The A/D converter saturates at approximately ±2.2 volts rms (±3.1 volts peak).



Decoding

The PCM word is fetched by the D_R lead from the PCM highway at the proper time-slot occurrence. The decoded value is held on the external capacitor connected to the $CAP1_R$ and $CAP2_R$ leads.

The buffered non-return to zero output signal on the VF_R lead is equal to the stored voltage on CAP_R. The output signal on lead VF_R has a dynamic range of ±2.2 volts rms (±3.1 volts peak).

Standby Mode — Power Down

To minimize power consumption and dissipation in large systems, a standby mode is provided by loading a control word (D_C) with a "1" in bits 1 and 2 locations. Most of the Codec functions thereby become disabled, with the exception of the interface to the D_C and CLK_C leads, to allow the Codec to be reactivated.

The power consumption in the standby mode is typically 110mW.

Power-On Clear

Whether the device is used in the direct or microcomputer mode, an internal reset (power-on clear) is generated whenever either of the two positive device power supplies (V_{DD} or V_{CC}) are removed or applied. The Codec thus assumes the power-down state upon application of the positive power supplies and must be initialized in the normal way for operation.

Precision Voltage Reference for the D/A Converter

The voltage reference is generated on the chip and is calibrated during the manufacturing process. The technique uses the difference in sub-surface charge density between two suitably implanted MOS devices to derive a temperature stable and bias stable reference voltage.

A gain setting op amp, programmed during manufacturing, "trims" the reference voltage source to the final precision voltage reference value provided to the D/A converter. The precision voltage reference determines the initial gain and dynamic range characteristics described in the A.C. Transmission Specification Section.

CONVERSION LAW

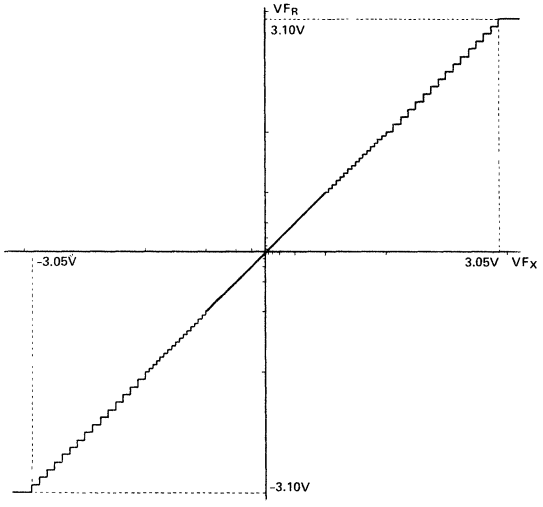
The conversion law is commonly referred to as the A Law.

The Codec provides a piecewise linear approximation of the logrithmic law through 13 segments. Each segment is made of 16 steps with the exception of the first segment which has 32 steps. In adjacent segments the step sizes are in a ratio of two to one. Within each segment, the step size is constant.

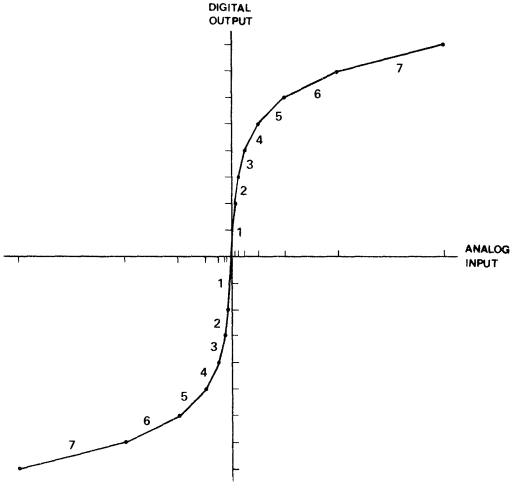
The output levels are midway between the corresponding decision levels. The output levels Y_n are related to the input levels X_n by the expression:

$$Y_n = \frac{X_{n-1} + X_n}{2} \qquad 0 < n \leq 128$$

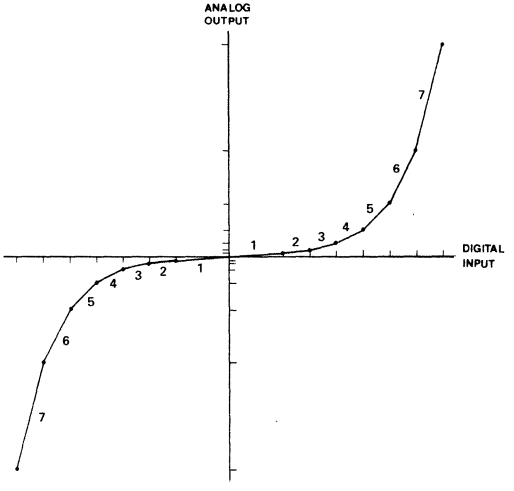
CODEC TRANSFER CHARACTERISTIC



CODER TRANSFER CHARACTERISTIC
(A/D CONVERSION)



DECODER TRANSFER CHARACTERISTIC
(D/A CONVERSION)



THEORETICAL A LAW – POSITIVE INPUT VALUES

(For Negative Input Values, Invert Bit 1)

1	2	3	4	5	6								7	8
Segment No.	No. of Steps x Step Size	Value at Segment End Points	Decision Value No. n	Decision Value X_n (1)	PCM Word(4) Bit Number 1	2	3	4	5	6	7	8	Normalized Value at Decoder Output Y_n (5)	Decoder Output Value No.
		4096(3)	(128)	(4096)	1	1	1	1	1	1	1	1	4032	128
7	16 x 128		127	3968							(2)			
			113	2176										
		2048	112	2048	1	1	1	1	0	0	0	0	2112	113
6	16 x 64										(2)			
			97	1088										
		1024	96	1024	1	1	1	0	0	0	0	0	1056	97
5	16 x 32										(2)			
			81	544										
		512	80	512	1	1	0	1	0	0	0	0	528	81
4	16 x 16										(2)			
			65	272										
		256	64	256	1	1	0	0	0	0	0	0	264	65
3	16 x 8										(2)			
			49	136										
		128	48	128	1	0	1	1	0	0	0	0	132	49
2	16 x 4										(2)			
			33	68										
		64	32	64	1	0	1	0	0	0	0	0	66	33
1	32 x 2										(2)			
			1	2										
			0	0	1	0	0	0	0	0	0	0	1	1

NOTES:

(1) 4096 normalized value units correspond to the value of the on-chip voltage reference.

(2) The PCM word corresponding to positive input values between two successive decision values numbered n and n+1 (see column 4) is (128+n) expressed as a binary number.

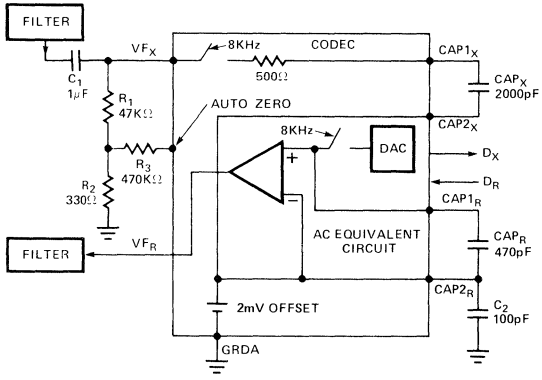
(3) X_{128} is a virtual decision value.

(4) The PCM word on the highways is the same as the one shown in column 6, with the even order bits inverted. The 2911 provides for the inversion of the even order bits on both the send and receive sections. The sign bit is inverted on the encoder side only.

(5) The voltage output on the VF_R lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15mV.

APPLICATIONS

Circuit Interface



Holding Capacitors

For an 8KHz sampling system the transmit holding capacitor CAP_X should be 2000pF, 20%. The receive holding capacitor CAP_R should be 470pF, 20% for 32 time-slots and 8KHz sample rate or 560pF, 20% for 24 time-slots and 8KHz sample rate. An additional capacitor C_2 of 100pF, is required from the $CAP2_R$ lead to GRDA.

Auto Zero

The auto zero output (most significant bit or sign bit of the A/D conversion) integrated over a long time constant will compensate for the DC offset inside the Codec (voltage difference between the bottom of the DAC and GRDA). The above drawing shows a possible connection between the VF_X and Auto leads. The recommended values of the auto zero components are:

C_1 of 1μF, R_1 of 47kΩ, R_2 of 330Ω, and R_3 of 470kΩ.

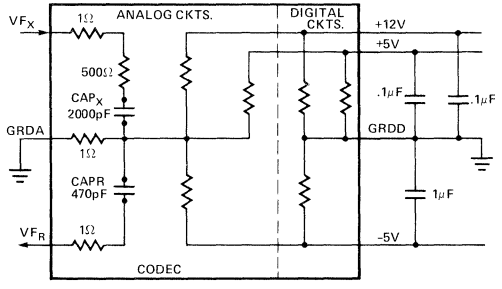
Filters Interface

The filters may be interfaced as shown in the circuit interface diagram. Note that the output pulse stream is of the non-return to zero type.

D_X Buffering

For optimum idle channel noise performance it is recommended that the D_X output of each Codec be buffered from the system PCM bus with an external three-state or open collector buffer. Each buffer can be enabled with the appropriate Codec generated $\overline{TS_X}$ signal.

Grounding and Decoupling Recommendations



Grounding

Analog grounding is connected to the GRDA lead. The GRDA and GRDD leads are not connected inside the 2911. An external connection is thus necessary outside the Codec to tie all the analog ground lines to the common return of the system GRDD.

To minimize the injection of digital logic noise into the analog signal path the GRDA and GRDD external connection should be made as close as practical to the system supply ground.

Decoupling

A 0.1μF bypassing capacitor from each power supply to digital ground is generally recommended at each device. This decoupling may be reduced based on actual board design and performance.

Sufficient board level decoupling must be provided to guarantee that power supply transients (including turn on and off) do not exceed the absolute maximum ratings of the device. A minimum of 1μF is recommended once per board for each power supply. A pair of small switching diodes (in opposite directions) between analog and digital ground on a once-per-board basis is recommended to maintain the two ground levels near the same value during board insertion and removal.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
All Input or Output Voltages
with Respect to V_{BB} ..... -0.3 to +20V
V_{CC}, V_{DD} and V_{SS} with
Respect to V_{BB} ..... -0.3 to +20V
Power Dissipation 1.35W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

DIGITAL INTERFACE

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{IL}	Low Level Input Current			10	µA	$V_{IN} < V_{IL}$
I_{IH}	High Level Input Current			10	µA	$V_{IN} > V_{IH}$
V_{IL}	Input Low Voltage			+0.6	V	
V_{IH}	Input High Voltage	+2.2			V	
V_{OL}	Output Low Voltage			0.4	V	D_X, I_{OL}=3.2mA
						$\overline{TS_X}$, I_{OL}=1.6mA, open drain
						PDN, I_{OL}=0.5mA, open drain
V_{OH}	Output High Voltage	2.4			V	D_X, I_{OH}=30mA

ANALOG INTERFACE

A_{IZ}	Input Impedance when Sampling, VF_X	125	300	500	Ω	In Series with CAP_X to GRDA, -3.1V < V_{IN} < 3.1V
A_{OZ}	Output Impedance, VF_R	100	180	300	Ω	-3.1V < V_{OUT} < 3.1V
V_{OL}	Output Low Voltage, Auto		V_{BB}		V	400kΩ to GRDA
V_{OH}	Output High Voltage, Auto		V_{CC}		V	
R_1	Auto Zero Component	42	47	52	kΩ	47kΩ Recommended[2]
R_2	Auto Zero Component	290	330	616	Ω	330Ω Recommended[2]
R_3	Auto Zero Component	420	470	520	kΩ	470kΩ Recommended[2]
C_1	Auto Zero Component	1.0			µF	
CAP_X	Holding Capacitor, Transmit	1600	2000	2400	pF	8kHz Sampling, 2000pF Recommended[2]
CAP_R	Holding Capacitor, Receive	390	470	560	pF	8kHz Sampling, 32 Time-Slots, 470pF Recommended[2]
		450	560	670	pF	8kHz Sampling, 24 Time-Slots, 560pF Recommended[2]
C_2	Bypass Capacitor	80	100	120	pF	100pF Recommended[2]

POWER DISSIPATION

I_{DDO}	Standby Current		6	9	mA	V_{DD} = 12.6V V_{CC} = 5.25V V_{BB} = -4.75V Clock Frequency 2.048MHz
I_{CCO}	Standby Current		5	8	mA	
I_{BBO}	Standby Current		2	4	mA	
I_{DDI}	Operating Current		11	16	mA	
I_{CCI}	Operating Current		13	21	mA	
I_{BBI}	Operating Current		4	6	mA	

NOTES: 1. Typical Values are for T_A = 25°C and nominal power supply values.
2. See Applications Circuit Interface for component connections.

TELECOM

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

TRANSMISSION, GAIN AND DYNAMIC RANGE

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
S/D	Signal to Total Distortion Ratio. See Figure 2. CCITT G.712 Method 2 (Sinusoidal method).	35			dB	Signal Level 0dBm0 to -30dBm0
		29			dB	Signal Level -40dBm0
		24			dB	Signal Level -45dBm0
ΔG	Gain Tracking Deviation from Gain at 0dBm0. See Figure 1. CCITT G.712 Method 2 (Sinusoidal method).			±0.3	dB	Signal Level +3dBm0 to -40dBm0
				±0.7	dB	Signal Level -40dBm0 to -50dBm0
				±2.1	dB	Signal Level -50dBm0 to -55dBm0
N_{IC}	Idle Channel Noise			-73	dBmOp	With Auto Zero[2]
A_{OR}	Output Dynamic Range, VF_R	2.14	2.16	2.18	V_{RMS}	23°C, Nominal Supplies
A_{ORT}	A_{OR} Variation with Temperature			-.22	$mV_{RMS}/°C$	Relative to 23°C
A_{ORS}	A_{OR} Variation with Supplies			±18	mV_{RMS}	Supplies ±5%
G_{SL}	Self Loop Gain	-.24	-.20	-.16	dB	VF_X=-dBm0, 1.02KHz[3]
G_{EE}	End-to-End Codec Gain	-.4	-.3	-.2	dB	23°C, Nominal Supplies[4]
G_{EET}	G_{EE} Variation with Temperature		.0010	.0018	dB/°C	Relative to 23°C[4]
G_{EES}	G_{EE} Variation with Supplies		±.07	±.13	dB	Supplies ±5%[4]
G_{FR}	Decoder Frequency Response Departure from Ideal (Sinx)/x, VF_R			±.05	dB	300 Hz < f < 3800 Hz VF_X = 0dBm0[5]
CT	Cross Talk Isolation	75	>80		dB	[6]

NOTES:

1. Typical Values are for $T_A = 25°C$ and nominal power supply values.
2. If all Auto-Zero components are removed and VF_X is direct coupled, the encoder tends to bias itself away from a decision level (hysteresis). The idle channel noise is then typically -85dBmOp, but will be dependent on the D.C. offset of the PCM transmit filter output provided to VF_X.
3. D.U.T. acts as both encoder and decoder (D_X=D_R) in a digital loop-back configuration. Specified gain is in addition to normal (Sinx)/x insertion loss.
4. Any 2911 as encoder; any other 2911 as decoder; both D.U.T.'s with separate supplies and at independent temperatures. Specified gain is in addition to normal (Sinx)/x insertion loss.
5. (Sinx)/x with $x = \frac{\text{Measurement Frequency } (f) \times \pi}{\text{Sampling Frequency}}$
6. VF_X of D.U.T. encoder = 1.02KHz, 0dBm0. Co-located D.U.T. decoder under quiet channel conditions; measurement made at co-located decoder output.

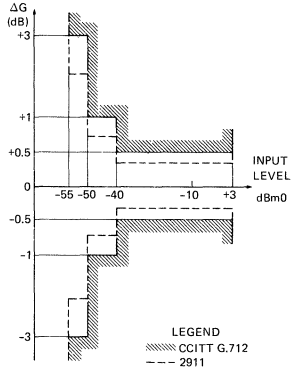


Figure 1. Gain Variation (ΔG) vs. Signal Level Reference Level 0dBm0

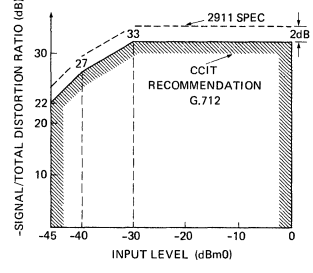


Figure 2. -Signal/Total Distortion Ratio

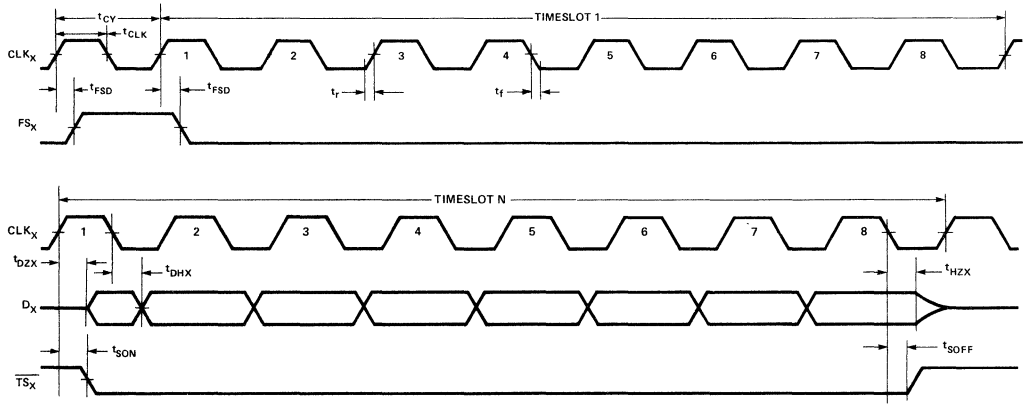
A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

TIMING SPECIFICATIONS AND WAVEFORMS[1]

CLOCK AND TRANSMIT SECTION

Symbol	Parameter	Limits Min.	Limits Max.	Units	Comments
t_{CY}	Clock Period	485		ns	CLK_X, CLK_R (2.048MHz systems), CLK_C
t_r, t_f	Clock Rise and Fall Time	5	30	ns	CLK_X, CLK_R, CLK_C
t_{CLK}	Clock Pulse Width	215		ns	CLK_X, CLK_R, CLK_C
t_{CDC}	Clock Duty Cycle ($t_{CLK} \div t_{CY}$)	45	55	%	CLK_X, CLK_R
t_{VFX}	Analog Input Conversion	20		Time Slot	From Leading Edge of Transmit Time Slot[2]
t_{DZX}	Data Enabled on TS Entry	50	180	ns	0 < C_{LOAD} < 100pF
t_{DHX}	Data Hold Time	80	230	ns	0 < C_{LOAD} > 100pF
t_{HZX}	Data Float on TS Exit	75	205	ns	C_{LOAD} = 0
t_{SON}	Time Slot X to Enable	30	220	ns	0 < C_{LOAD} < 100pF
t_{SOFF}	Time Slot X to Disable	70	185	ns	C_{LOAD} = 0
t_{SS}	Signal Setup Time	0		ns	Relative to Bit-7 Falling Edge
t_{SH}	Signal Hold Time	100		ns	Relative to Bit-8 Falling Edge
t_{FSD}	Frame Sync Delay	15	100	ns	FS_X



Notes:

1. All timing parameters referenced to 2.0V, except t_{HZX} and t_{SOFF} which reference a high impedance state
2. The 20 time slot minimum insures that the complete A/D conversion will take place under any combination of receive interrupt or asynchronous operation of the Codec. If the transmit channel only is operated the A/D conversion can be completed in a minimum of 11 time slots. Refer to the Codec Control General Requirement section for instructions on setting a channel in an idle condition.

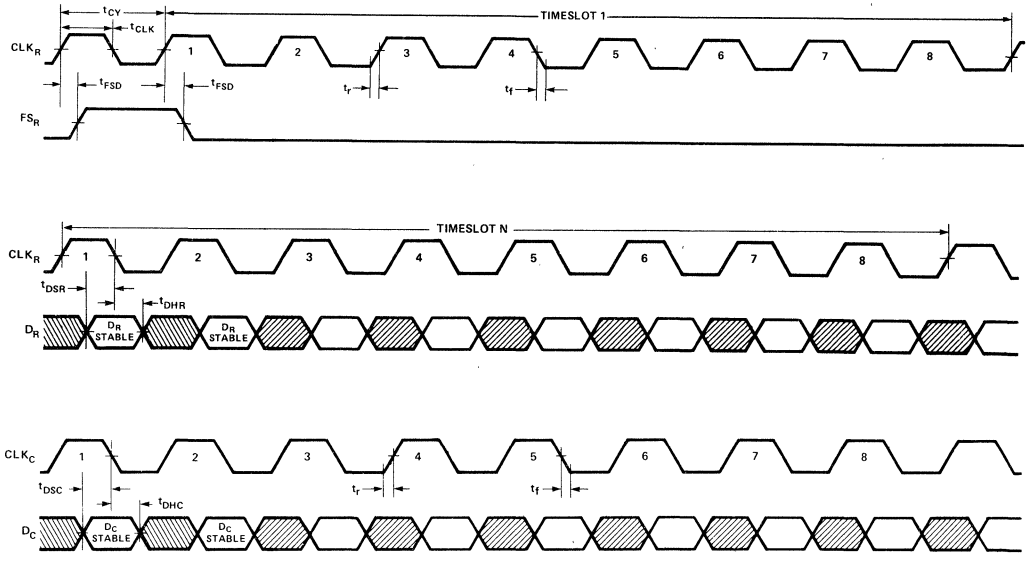
TELECOM

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified.

TIMING SPECIFICATIONS AND WAVEFORMS[1]

RECEIVE AND CONTROL SECTIONS

t_{VFR}	Analog Output Update		8	Time Slot	From the Leading Edge of the Channel Time Slot
t_{DSR}	Receive Data Setup	40		ns	
t_{DHR}	Receive Data Hold	30		ns	
t_{SIGR}	SIG_R Update		300	ns	From the Trailing Edge of the Channel Time Slot
t_{FSD}	Frame Sync Delay	15	100	ns	
t_{DSC}	Control Data Setup	100		ns	
t_{DHC}	Control Data Hold	100		ns	



Notes:
1. All timing parameters referenced to 2.0V, except t_{HZX} and t_{SOFF} which reference a high impedance state.

2912
PCM LINE FILTERS

- **Monolithic Device Includes Both Transmit and Receive Filters**
- **CCITT G712 Compatible AT&T® D3/D4 Compatible**
- **50Hz/60Hz Rejection Included in the Transmit Filter**
- **Gain Adjustment in Both Directions**
- **Direct Interface with Transformer or Electronic Telephone Hybrids**
- **Direct Interface to the Intel® 2910/2911 PCM Codecs Including Stand-By, Power Down Mode**
- **±5% Power Supplies: +5V, -5V**
- **Low Power Consumption:**
  210mW Typical without Power Amplifiers
  280mW Typical with Power Amplifiers
  55mW Typical on Stand-By
- **Fabricated with Reliable N-Channel MOS Process**

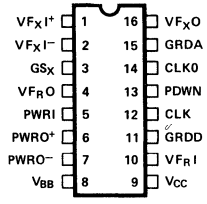
TELECOM

The Intel® 2912 is a fully integrated monolithic device containing the two filters of a PCM line or trunk termination. The device is designed to meet the following objectives:

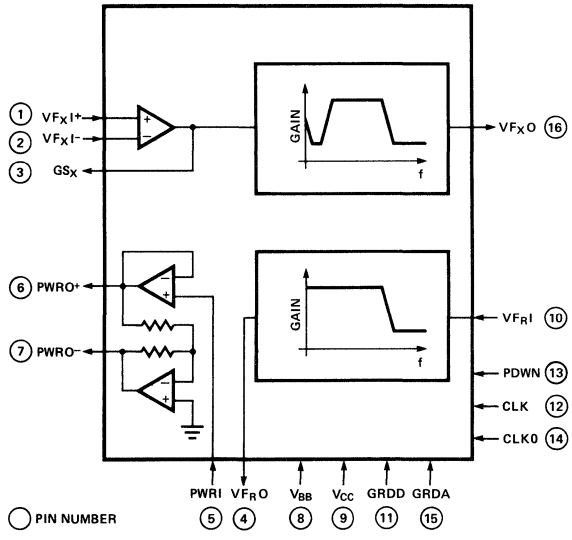
- To meet the digital Class 5 central office switching systems stringent specification
- To minimize power dissipation
- To maximize reliability
- To provide a low cost alternative to hybrid filters

The 2912 is directly compatible with the Intel® 2910 (μ Law) and the Intel® 2911 (A Law) PCM Codecs. The primary application for the 2912 is in telephone systems, for transmission, switching or remote concentration.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

VF_XI^+, VF_XI^-	ANALOG INPUTS	CLK	CLOCK INPUT
GS_X	GAIN CONTROL	CLK0	CLOCK SELECTION
VF_XO	ANALOG OUTPUT	PWDN	POWER DOWN
VF_RI	ANALOG INPUT	V_{CC}	POWER (+5V)
VF_RO	ANALOG OUTPUT	V_{BB}	POWER (-5V)
PWRI	DRIVER INPUT	GRDD	DIGITAL GROUND
$PWRO^+$, $PWRO^-$	DRIVER OUTPUT	GRDA	ANALOG GROUND

PIN DESCRIPTION

Pin No.	Symbol	Function	Description
1	VF_XI^+	Input	Analog input of the transmit filter. The VF_XI^+ signal comes from the 2 to 4 wire hybrid in the case of a 2 wire line and goes through the 50/60Hz notch and the antialiasing filter before being sent to the Codec for encoding.
2	VF_XI^-	Input	Inverting input of the gain adjustment operational amplifier on the transmit filter.
3	GS_X	Output	Output of the gain adjustment operational amplifier on the transmit filter. Used for gain setting of the transmit filter.
4	VF_RO	Output	Analog output of the receive filter. This output provides a direct interface to electronic hybrids. For a transformer hybrid application, VF_RO is tied to PRWI and a dual balanced output is provided on pins $PWRO^+$ and $PWRO^-$.
5	PWRI	Input	Input to the power driver amplifiers on the receive side for interface to transformer hybrids. High impedance input. When tied to V_{BB}, the power amplifiers are powered down.
6	$PWRO^+$	Output	Non-inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
7	$PWRO^-$	Output	Inverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
8	V_{BB}	Power	-5V ± 5% referenced to GRDA
9	V_{CC}	Power	+5V ± 5% referenced to GRDA
10	VF_RI	Input	Analog input of the receive filter, interface to the Codec analog output for PCM applications. The receive filter provides the $\frac{Sinx}{x}$ correction needed for sample and hold type Codec outputs to give unity gain. The input voltage range is directly compatible with the Intel® 2910 and 2911 Codecs.
11	GRDD	Ground	Digital ground return for internal clock generator.
12	CLK[1]	Input	Clock input. Three clock frequencies can be used: 1.536MHz, 1.544MHz or 2.048MHz; pin 14, CLK0, has to be strapped accordingly. High impedance input, TTL voltage levels.
13	PDWN	Input	Control input for the stand-by power down mode. An internal pull up to +5V is provided for interface to the Intel® 2910 and 2911 PDWN outputs. TTL voltage levels.
14	CLK0[1]	Input	Clock (pin 12, CLK) frequency selection. If tied to V_{BB}, CLK should be 1.536MHz. If tied to Ground, CLK should be 1.544 MHz. If tied to V_{CC}, CLK should be 2.048MHz.
15	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally.
16	VF_XO	Output	Analog output of the transmit filter. The output voltage range is directly compatible with the Intel® 2910 and 2911 Codecs.

NOTE:
1. The three clock frequencies are directly compatible with the Intel® 2910 and 2911 Codecs. The following table should be observed in selecting the clock frequency.

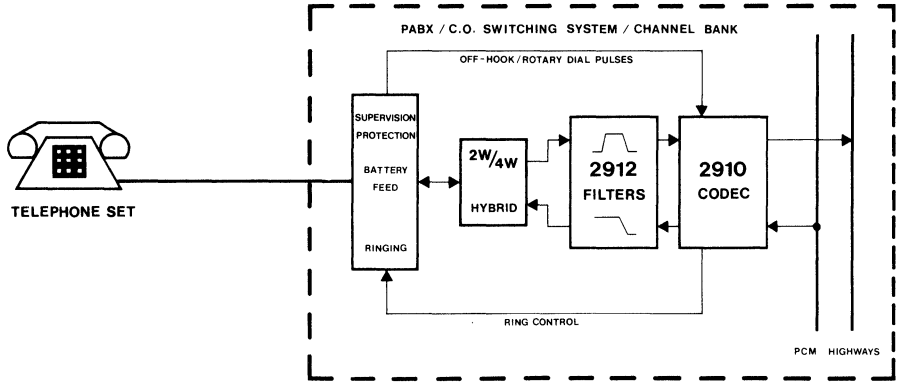
Codec Clock	Clock Bits/Frame	2912 CLK, Pin 12	2912 CLK0, Pin 14
1.536 MHz	192	1.536 MHz	V_{BB} (-5V)
1.544 MHz	193	1.544 MHz	GRDD
2.048 MHz	256	2.048 MHz	V_{CC} (+5V)

FUNCTIONAL DESCRIPTION

The 2912 provides the transmit and receive filters found on the termination of a PCM line or trunk. The transmit filter performs the anti-aliasing function needed for an 8KHz sampling system, and the 50/60Hz rejection. The receive filter has a low pass transfer characteristic and also provides the Sinx/x correction necessary to interface the Intel 2910 (μ Law) and 2911 (A Law) Codecs which have a non-return-to-zero output of the digital to analog conversion. Gain adjustment is provided in the receive and transmit directions.

A stand-by, power down mode is included in the 2912 and can be directly controlled by the 2910/2911 Codecs.

The 2912 can interface directly with a transformer hybrid (2 to 4 wire conversion) or with electronic hybrids; in the latter case the power dissipation is significantly reduced by powering down the output amplifier provided on the 2912.

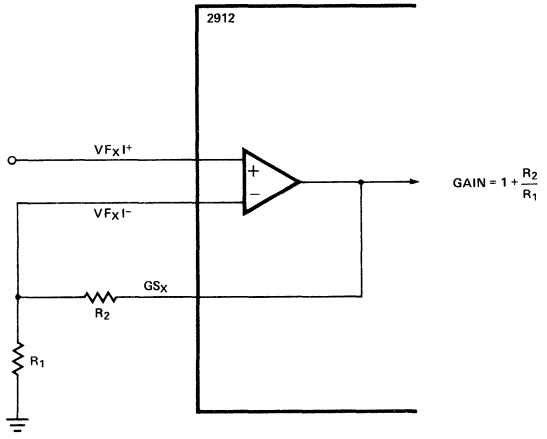


TYPICAL LINE TERMINATION

FILTER OPERATION

Transmit Filter Input Stage

The input stage provides gain adjustment in the passband. The input operational amplifier has a common mode range of ±2.2 volts, a DC offset of less than 25mV, a voltage gain greater than 2000 and a unity gain bandwidth of 2MHz. It can be connected to provide a gain of 20dB without degrading the noise performance of the filter. The load impedance connected to the amplifier output must be greater than 10KΩ in parallel with 20pF. The input signal on lead VF_XI^+ can be either AC or DC coupled. The input Op Amp can also be used in the inverting mode or differential amplifier mode. The remaining portion of the transmit filter provides a gain of +3dB in the pass band.



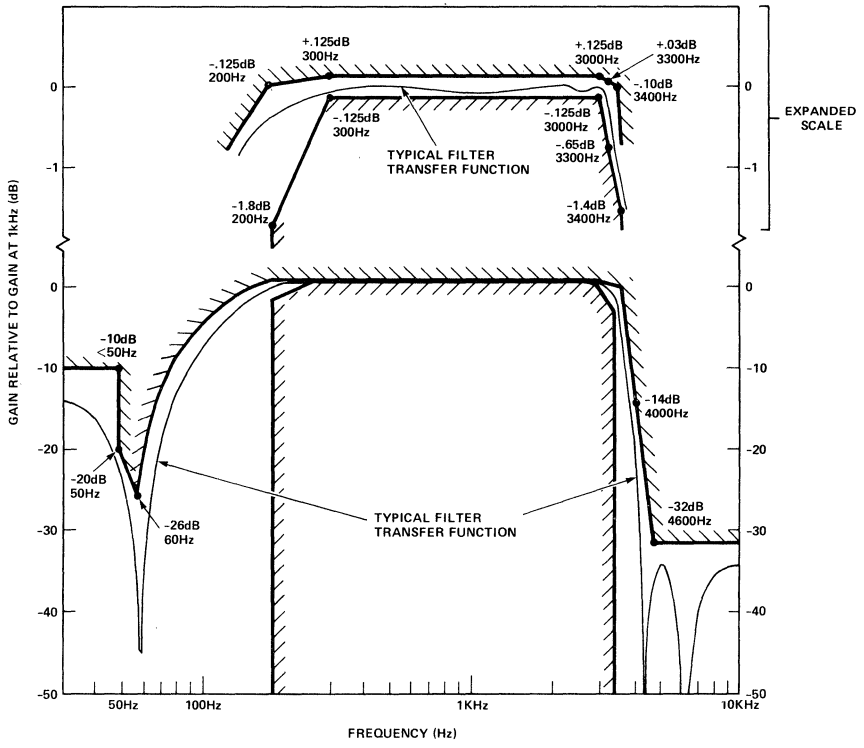
TRANSMIT FILTER GAIN ADJUSTMENT

Transmit Filter Transfer Characteristics

The transmit section of the filter provides a passband flatness and stopband attenuation which exceeds the ATT® D3 and D4 specification and is compatible with the CCITT G712 recommendation. The 2912 specification meets the digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications are shown in the diagram below.

50Hz/60Hz Notch — Transmit Filter

The transmit filter has a notch section to reject 50Hz and 60Hz components of the input signal. A minimum attenuation of 26dB is provided at 60Hz. At 50Hz, the minimum attenuation is 20dB. The gain at 200Hz is between -.125dB and -1.8dB. (All gain figures are relative to the gain at 1kHz).



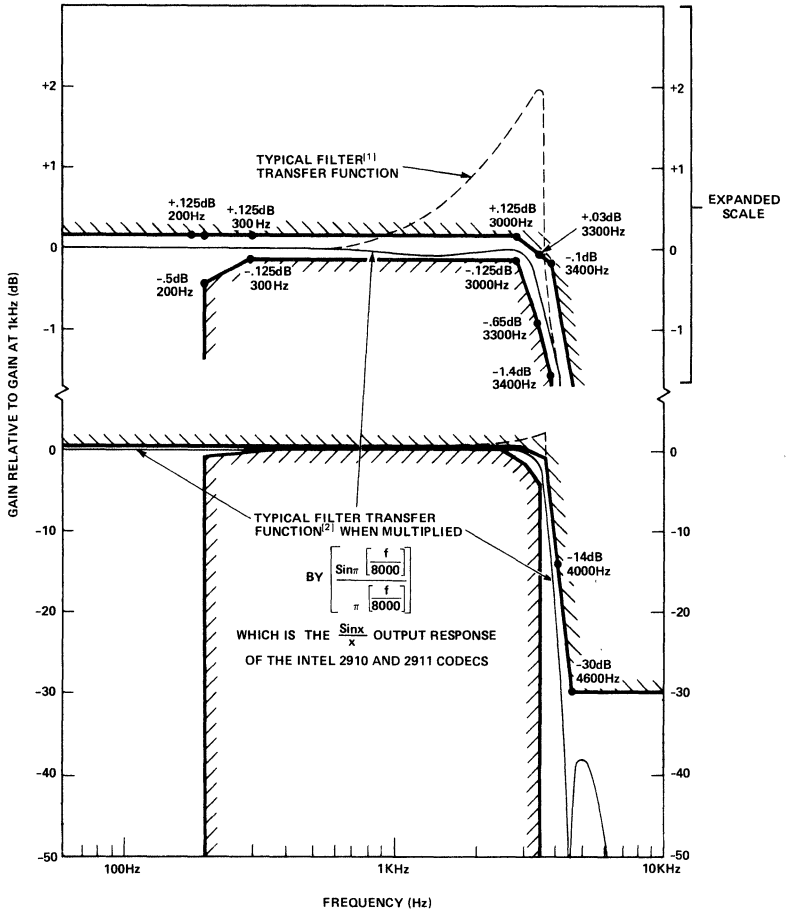
TRANSMIT FILTER TRANSFER CHARACTERISTICS

Transmit Filter Output Stage

The voltage range of the output signal on the VF_XO lead is ±3.2 volts. The DC offset is less than 200mV. It is recommended that the VF_XO output be capacitively coupled to the VF_X input of the Intel®2910 and 2911 Codecs.

Receive Filter Transfer Characteristics

The receive section of the filter provides a passband flatness and stopband rejection which exceeds the ATT® D3/D4 specification and is compatible with the CCITT G712 recommendation when used with a decoder which contains a sample/hold amplifier at its output. The filter contains the required compensation for the $\frac{Sinx}{x}$ response of such decoders. The receive filter transfer characteristics and specifications, including the $\frac{Sinx}{x}$ response of the decoder, as shown in the diagram below.



NOTES:
1. TYPICAL TRANSFER FUNCTION OF THE RECEIVE FILTER AS A SEPARATE COMPONENT.
2. TYPICAL TRANSFER FUNCTION OF THE RECEIVE FILTER DRIVEN BY THE SAMPLE AND HOLD OUTPUT OF THE INTEL 2910 AND 2911 CODECS. THE COMBINED FILTER/CODEC RESPONSE MEETS THE STATED SPECIFICATIONS.

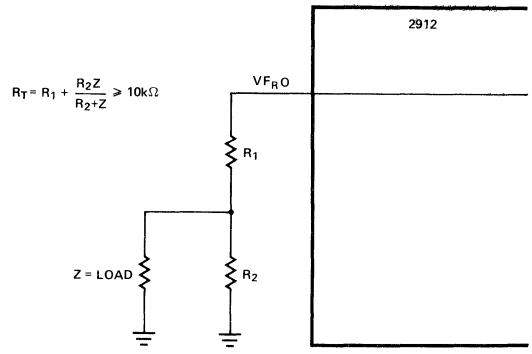
RECEIVE FILTER TRANSFER CHARACTERISTICS

Receive Filter Output

The VF_RO lead is capable of driving high impedance electronic hybrids. The gain of the receive section from VF_RI to VF_RO is:

$$\frac{\pi\left(\frac{f}{8000}\right)}{\text{Sin}\pi\left(\frac{f}{8000}\right)}$$

which when multiplied by the output response of the Intel 2910 and 2911 Codecs results in a 0dB gain in the pass band. The filter gain can be adjusted downward by a resistor voltage divider connected as shown. The total resistive load R_T on VF_RO should not be less than 10kΩ.

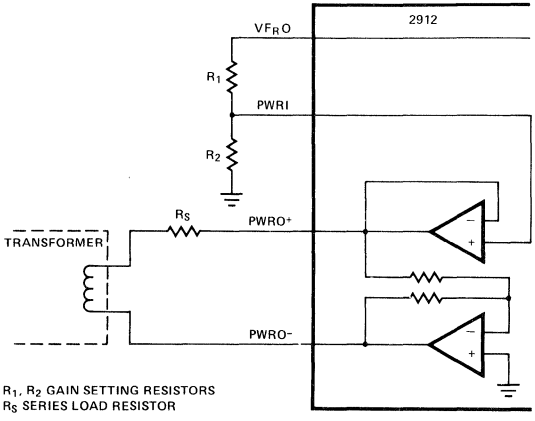


RECEIVE FILTER OUTPUT GAIN ADJUSTMENT

Receive Filter Output Driver Amplifier Stage

A balanced power amplifier is provided in order to drive low-impedance loads in a bridged configuration. The receive filter output VF_RO is connected through gain setting resistors R_1 and R_2 to the amplifier input PWRI. The input voltage range on PWRI is ±3.2 volts and the gain is 6dB for a bridged output. With a 20kΩ load connected between $PWRO^+$ and $PWRO^-$, the maximum voltage swing across the load is ±6.4 volts. With a 600Ω load connected between $PWRO^+$ and $PWRO^-$, the maximum voltage swing across the load is ±5.0 volts. The series combination of R_S and the hybrid transformer must present a minimum A.C. load resistance of 600Ω to the amplifier in the bridged configuration. A typical connection of the output driver amplifiers is shown below. These amplifiers can also be used with loads connected to ground.

The power amplifier should be deactivated when not utilized to save power. This is accomplished by tying the PWRI pin to V_{BB}.



TYPICAL CONNECTION OF OUTPUT DRIVER AMPLIFIER

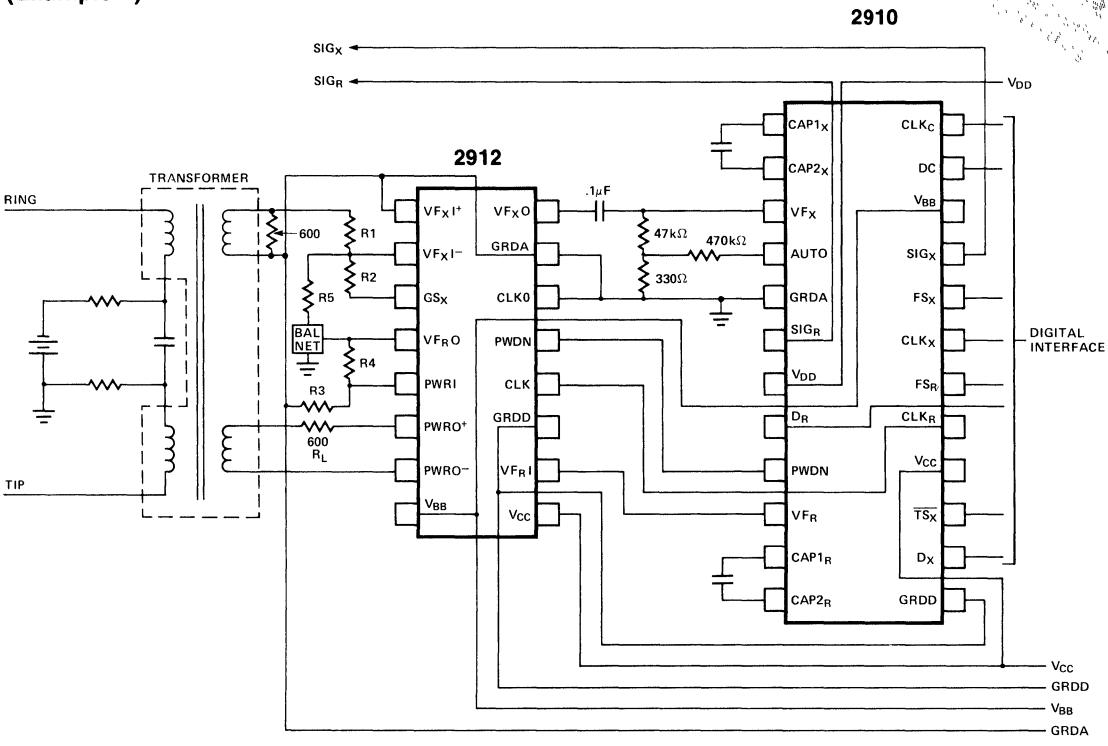
Power Down Mode

Pin 13, PDWN, provides the power down control. When the signal on this lead is brought high, the 2912 goes into a standby, power down mode. Power dissipation is reduced to 55mW. In the stand-by mode, all outputs go into a high impedance state. This features allows multiple 2912's to drive the same analog bus on a time-shared basis.

When power is restored, the settling time of the 2912 is typically 15ms.

The PDWN interface is directly compatible with the Intel 2910 and 2911 PDWN outputs. Only one command from the common control is then necessary to power down both the Codec and the Filters of the line or trunk interface.

APPLICATIONS
Circuit Interface (Example 1)



TYPICAL LINE INTERFACE USING A 2910 CODEC AND 2912 FILTER AND TRANSFORMER-RESISTOR HYBRID.

Codec Interface

The 2912 PCM Filter is designed to directly interface to the 2910 and 2911 Codecs as shown above. The transmit path is completed by connecting the VF_XO output of the 2912 to the coupling capacitor of the auto zero circuit associated with the 2910 and 2911 codecs. The receive path is completed by directly connecting the codec output VF_R to the receive input of the 2912 VF_RI. The PWDN input of the 2912 should be connected to the PWDN output of the codec to allow the filter to be put in the power-down standby mode under control of the codec.

Clock Interface

To assure proper operation, the CLK input of the 2912 should be connected to the same clock provided to the receive bit clock, CLK_R of 2910 or 2911 Codec as shown above. The CLK0 input of the 2912 should be set to the proper voltage depending on the standard clock frequency chosen for the codec and filter. See the clock selection table in the Pin Description section.

Transformer Interface (Example 1)

The diagram above shows a typical interface of the 2912 Filter to a transformer. This connection can provide +8dBm into a 600Ω line. The functions of the resistors in example 1 are as follows:

R_1, R_2 are gain setting resistors for the transmit filter input stage. Transmit gain equals - R_2/R_1. The transmit filter provides an additional 3.0dB of gain.

R_3, R_4 are attenuation setting resistors for the receive filter. Receive gain equals $R_3/(R_3+R_4)$.

R_5 is a resistor which injects the balance network signal into the transmit path to perform the 2/4 wire conversion.

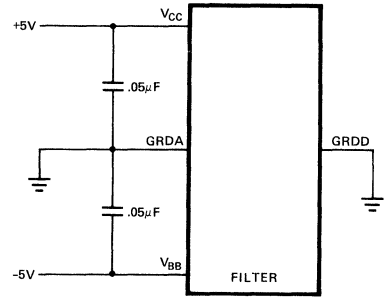
R_L is a 600Ω load resistor through which the balanced driver amplifier stage drives the transformer winding.

Grounding and Decoupling Recommendations

Analog grounding is connected to the GRDA leads. The GRDA and GRDD leads are not connected inside the 2912. An external connection is thus necessary outside the Filter to tie all the analog ground lines to the common return of the system GRDD. To minimize the injection of digital logic noise into the analog signal path the GRDA and GRDD external connection should be made as close as practical to the system supply ground.

The GRDA of the 2912 Filter should be tied to the GRDA of the 2910 or 2911 Codec as shown above. Likewise, the GRDD pins of the Codec and Filter should be connected. Analog gain setting or 2/4 wire circuits associated with the filter should have a ground path to GRDA.

A 0.05μF bypassing capacitor from each power supply to analog ground GRDA is generally recommended at each 2912 device. This decoupling may be reduced based on actual board design and performance. Sufficient board level decoupling must be provided to guarantee that power supply transients (including turn on and turn off) do not exceed absolute maximum ratings of the device. A minimum of 1μF is recommended once per board for each power supply.



TELECOM

Transformer Interface (Example 2)

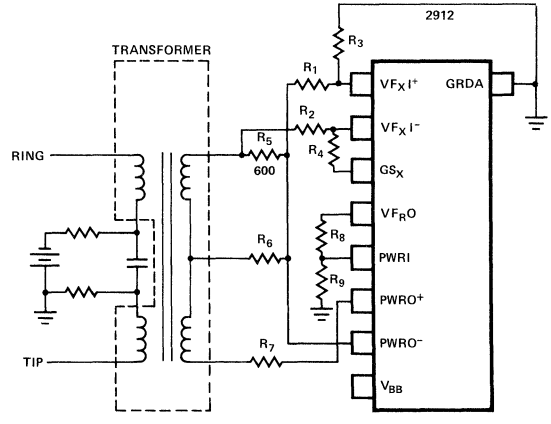
The diagram shows an alternative interface of the 2912 Filter to a transformer. This connection can provide +5.75dBm into a 600Ω line. The functions of the resistors in example 2 are as follows:

$R_1 = R_2$. The matching maintains hybrid balance.

$R_3 = R_4$. The gain setting for the transmit filter input stage is performed by R_2 and R_4. Transmit gain equals $-R_4/R_2$. The transmit filter provides an additional 3.0dB of gain.

$R_5 = R_7 = 2R_6$. Each power amplifier drives a load equal to R_5.

R_8, R_9 are attenuation setting resistors for the receive filter. Receive gain equals $R_9/(R_8+R_9)$.



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10° C to +80° C
Storage Temperature ..... -65° C to +150° C
Supply Voltage with Respect to V_{BB} .. -0.3V to +14.0V
All Input and Output Voltages with
Respect to V_{BB} ..... -0.3V to +14.0V
All Output Currents ..... ±50mA
Power Dissipation ..... 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0° C to +70° C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

DIGITAL INTERFACE

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LIC}	Input Load Current (except PDWN)			10	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LIO}	Input Load Current, CLK0			10	μA	V_{IN} = V_{BB} to $V_{IH\ MAX}$
I_{LIP}	Input Load Current, PDWN			-100	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
V_{IL}	Input Low Voltage (except CLK0)			0.8	V	
V_{IH}	Input High Voltage (except CLK0)	2.2			V	
V_{IL0}	Input Low Voltage, CLK0	V_{BB}		V_{BB}+0.5	V	
V_{II0}	Input Intermediate Voltage, CLK0	GRDD-0.5		0.8	V	
V_{IH0}	Input High Voltage, CLK0	V_{CC}-0.5		V_{CC}	V	

POWER DISSIPATION

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{CC0}	V_{CC} Standby Current		6	9	mA	PDWN = $V_{IH\ MIN}$
I_{BB0}	V_{BB} Standby Current		5	8	mA	PDWN = $V_{IH\ MIN}$
I_{CC1}	V_{CC} Operating Current, Power Amplifiers Inactive		21	33	mA	PWRI = V_{BB}
I_{BB1}	V_{BB} Operating Current, Power Amplifiers Inactive		21	33	mA	PWRI = V_{BB}
I_{CC2}	V_{CC} Operating Current		28	44	mA	
I_{BB2}	V_{BB} operating Current		28	44	mA	

NOTE: 1. Typical values are for T_A = 25° C and nominal power supply values.

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D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

ANALOG INTERFACE, TRANSMIT FILTER INPUT STAGE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{BXI}	Input Leakage Current, VF_XI^+, VF_XI^-			100	nA	-2.2V < V_{IN} < 2.2V
R_{IXI}	Input Resistance, VF_XI^+, VF_XI^-	10			MΩ	
V_{OSXI}	Input Offset Voltage, VF_XI^+, VF_XI^-			25	mV	-2.2V < V_{IN} < 2.2V
$PSRR_1$	Power Supply Rejection, GS_X	45			dB	
CMRR	Common Mode Rejection, VF_XI^+, VF_XI^-	45			dB	-2.2V < V_{IN} < 2.2V
A_{VOL}	DC Open Loop Voltage Gain, GS_X	2000				
f_C	Open Loop Unity Gain Bandwidth, GS_X		2		MHz	
V_{OXI}	Output Voltage Swing, GS_X			±2.5	V	$R_L \geq 10k\Omega$
C_{LXI}	Load Capacitance, GS_X			20	pF	
R_{LXI}	Minimum Load Resistance, GS_X	10			kΩ	Minimum R_L

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ANALOG INTERFACE, TRANSMIT FILTER

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
R_{OX}	Output Resistance, VF_XO			400	Ω	
V_{OSX}	Output DC Offset, VF_XO			200	mV	VF_XI^+ Connected to GRDA, Input Op Amp at Unity Gain
$PSRR_2$	Power Supply Rejection of V_{CC} at 1kHz, VF_XO	30	35		dB	
$PSRR_3$	Power Supply Rejection of V_{BB} at 1kHz, VF_XO	25	30		dB	
C_{LX}	Load Capacitance, VF_XO			20	pF	
R_{LX}	Minimum Load Resistance, VF_XO	10			kΩ	Minimum R_L
V_{OX}	Output Voltage Swing, 1kHz, VF_XO			±3.2	V	$R_L \geq 10k\Omega$ or with 2910 or 2911

ANALOG INTERFACE, RECEIVE FILTER

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{BR}	Input Leakage Current, VF_RI			1	μA	-3.2V < V_{IN} < 3.2V
R_{IR}	Input Resistance, VF_RI	1			MΩ	
R_{OR}	Output Resistance, VF_RO			100	Ω	
V_{OSR}	Output DC Offset, VF_RO			200	mV	VF_RI Connected to GRDA
$PSRR_4$	Power Supply Rejection of V_{CC} at 1kHz, VF_RO	30	35		dB	
$PSRR_5$	Power Supply Rejection of V_{BB} at 1kHz, VF_RO	25	30		dB	
C_{LR}	Load Capacitance, VF_RO			20	pF	
R_{LR}	Minimum Load Resistance, VF_RO	10			kΩ	Minimum R_L
V_{OR}	Output Voltage Swing, VF_RO			±3.2	V	R_L = 10kΩ

NOTE:
1. Typical values for T_A = 25°C and nominal power supply values.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
I_{BRA}	Input Leakage Current, PWRI			3	μA	-3.2V < V_{IN} < 3.2V	
R_{IRA}	Input Resistance, PWRI	10			MΩ		
R_{ORA}	Output Resistance, PWRO+, PWRO−		1		Ω	|I_{OUT}| <10mA -3.0V < V_{OUT} < 3.0V	
V_{OSRA}	Output DC Offset, PWRO+, PWRO−			75	mV	PWRI Connected to GRDA	
C_{LRA}	Load Capacitance, PWRO+, PWRO−			100	pF		
V_{ORA1}	Output Voltage Swing Across R_L, PWRO+, PWRO− Single Ended Connection			±3.2	V	R_L = 10kΩ	R_L Connected to GRDA
				±2.9	V	R_L = 600Ω	
				±2.5	V	R_L = 300kΩ	
V_{ORA2}	Output Voltage Swing, PWRO+, PWRO− Balanced Output Connection			±6.4	V	R_L = 20kΩ	R_L Connected Between PWRO+ and PWRO−
				±5.8	V	R_L = 1200Ω	
				±5.0	V	R_L = 600Ω	

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

Clock Input Frequency: CLK = 1.536MHz ± 0.1%, CLK0 = V_{IL0} (Tied to V_{BB})
CLK = 1.544MHz ± 0.1%, CLK0 = V_{Il0} (Tied to GRDD)
CLK = 2.048MHz ± 0.1%, CLK0 = V_{IH0} (Tied to V_{CC})

TRANSMIT FILTER TRANSFER CHARACTERISTICS (See Transmit Filter Transfer Characteristics description section for graph)

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions
G_{RX}	Gain Relative to Gain at 1kHz					0dBmO Input Signal
	Below 50Hz			-10	dB	Gain Setting Op Amp at
	50Hz			-20	dB	Unity Gain
	60Hz			-26	dB	
	200Hz	-1.8		-0.125	dB	0dBmO Signal ≡ 1.1 V_{RMS}
	300Hz to 3000Hz	-0.125		0.125	dB	Input at VF_XI^-
	3300Hz	-0.65		0.03	dB	
	3400Hz	-1.4		-0.1	dB	0dBmO Signal ≡ 1.6 V_{RMS}
	4000Hz			-14	dB	Output at VF_XO
	4600Hz and Above			-32	dB	
G_{AX}	Absolute Passband Gain at 1kHz, VF_XO	2.9	3.0	3.1	dB	
G_{AXT}	Gain Variation with Temperature at 1kHz		.0005		dB/°C	0dBmO Signal Level
G_{AXS}	Gain Variation with Supplies at 1kHz		.05		dB/V	0dBmO Signal Level, Supplies ±5%
CT_{RT}	Cross Talk, Receive to Transmit, Measured at VF_XO			-60	dB	VF_RI = 1.6 V_{RMS}, 1kHz Input VF_XI^+, VF_XI^- Connected to GS_X, GS_X Connected through 10kΩ to GRDA
N_{CX1}	Total C Message Noise at Output, VF_XO		9	12	dBrnc0 [2]	Gain Setting Op Amp at Unity Gain
N_{CX2}	Total C Message Noise at Output, VF_XO		10	13	dBrnc0 [2]	Gain Setting Op Amp at 20dB Gain
D_{DX}	Differential Envelope Delay, VF_XO 1kHz to 2.6kHz			80	μs	
D_{AX}	Absolute Delay at 1kHz, VF_XO			130	μs	
DP_{X1}	Single Frequency Distortion Products			-48	dB	0dBm Input Signal at 1kHz
DP_{X2}	Single Frequency Distortion Products at Maximum Signal Level of +3dBm0 at VF_XO			-45	dB	0.16 V_{RMS} 1kHz Input Signal at VF_XI^-, Gain Setting Op Amp at 20dB Gain. The +3dBmO signal at VF_XO is 2.24 V_{RMS}.

See next page for NOTES.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified.

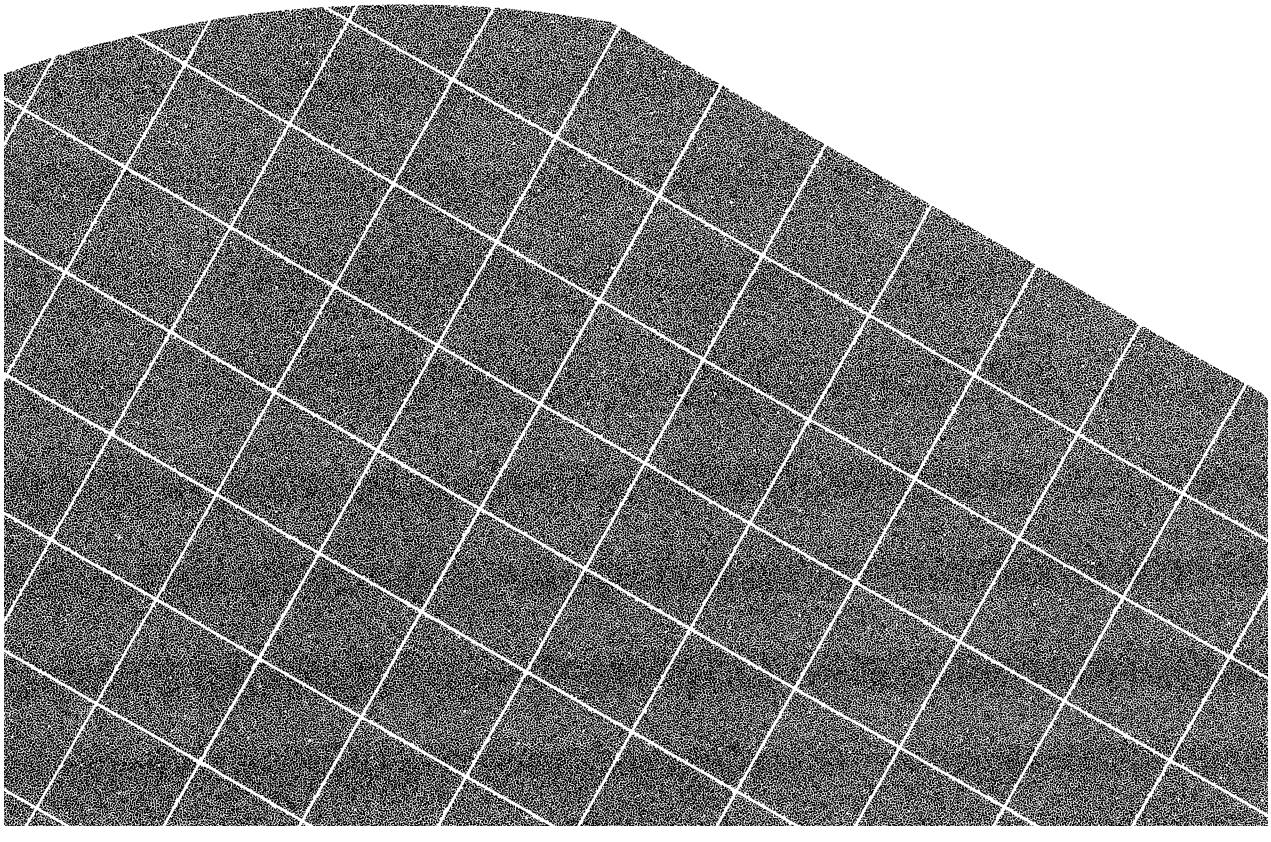
Clock Input Frequency: CLK = 1.536MHz ± 0.1%, CLK0 = V_{IL0} (Tied to V_{BB})
CLK = 1.544MHz ± 0.1%, CLK0 = V_{II0} (Tied to GRDD)
CLK = 2.048MHz ± 0.1%, CLK0 = V_{IH0} (Tied to V_{CC})

RECEIVE FILTER TRANSFER CHARACTERISTICS (See Receive Filter Transfer Characteristics description section for graph)

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions
G_{RR}	Gain Relative to Gain at 1kHz with Sinx/x Correction of 2910 or 2911					0dBmO Input Signal
	Below 200Hz			0.125	dB	0dBmO Signal ≡ 1.6 V_{RMS} x $\left(\text{Sin}\frac{f}{2\pi(8000)}\Big/\frac{f}{2\pi(8000)}\right)$ Input at VF_RI
	200Hz	-0.5		0.125	dB	
	300Hz to 3000Hz	-0.125		0.125	dB	
	3300Hz	-0.65		0.03	dB	
	3400Hz	-1.4		-0.1	dB	
	4000Hz			-14	dB	
	4600Hz and Above			-30	dB	
G_{AR}	Absolute Passband Gain at 1kHz, VF_RO	-0.1	0	+0.1	dB	0dBmO Signal ≡ 1.6 V_{RMS} Output at VF_RO
G_{ART}	Gain Variation with Temperature at 1kHz		.0005	dB/°C	dB/°C	0dBmO Signal Level
G_{ARS}	Gain Variation with Supplies at 1kHz		.05		dB/V	0dBmO Signal Level, Supplies ±5%
CT_{TR}	Cross Talk, Transmit to Receive, Measured at VF_RO			-60	dB	VF_XO = 2.2 V_{RMS}, 1kHz Output. VF_RI Connected to GRDA.
N_{CR}	Total C Message Noise at Output, VF_RO		9	12	dBrnc0 [2]	VF_RO Output or $PWRO^+$ and $PWRO^-$ Connected with Unity Gain
D_{DR}	Differential Envelope Delay, VF_RO, 1kHz to 2.6kHz			100	μs	
D_{AR}	Absolute Delay at 1kHz, VF_RO			130	μs	
DP_{R1}	Single Frequency Distortion Products			-48	dB	0dBm Input Signal at 1kHz
DP_{R2}	Single Frequency Distortion Products at Maximum Signal Level of +3dBmO at VF_RO			-45	dB	+3dBmO Signal Level of 2.24 V_{RMS}, 1kHz Input at VF_RO

NOTES:
1. Typical values are for T_A = 25°C and nominal power supply values.
2. A noise measurement of 18dBrnc into a 600Ω load at the 2912 device is equivalent to 12dBrnc0.

MCS-4/40™ Microprocessor 7



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*Partial data sheets are shown here. For complete specifications, contact Intel Literature Department, Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

4040

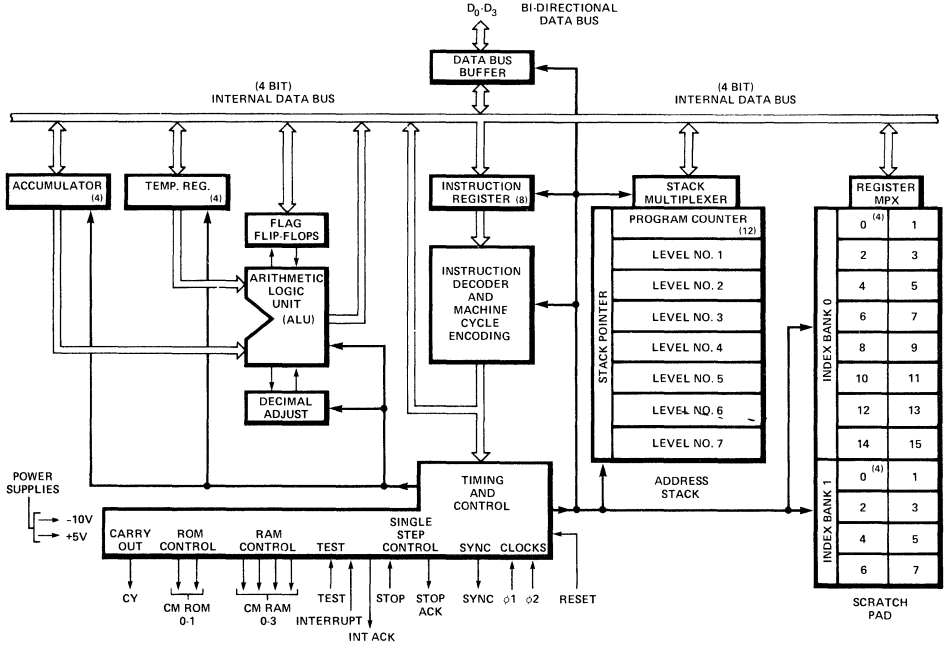
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- **Functionally and Electrically Upward Compatible to 4004 CPU**
- **14 Additional Instructions (60 total) Including Logical Operations and Read Program Memory**
- **Interrupt Capability**
- **Single Step Operation**
- **8K Byte Memory Addressing Capability**
- **24 Index Registers**
- **Subroutine Nesting to 7 Levels**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The Intel® 4040 is a complete 4-bit parallel central processing unit (CPU). The CPU can directly address 4K eight bit instruction words or 8K with a bank switch. Seven levels of subroutine nesting, including interrupt, and 24 randomly accessable index registers (24x4) are provided as convenient facilities for the designer. The index registers may be used for addressing or for scratch pad memory for storing computation results. The interrupt feature permits a normal program sequence to be interrupted, with normal program execution continuing after the interrupt service routine is completed. Provisions have also been made to permit single-stepping the CPU using the STOP and ACKNOWLEDGE signals.

The 4040 is an enhanced version of the 4004 and as such retains all the functional capability of that device. It will execute all the 4004 instructions, and is also electrically compatible with all components used with a 4004 CPU.

BLOCK DIAGRAM



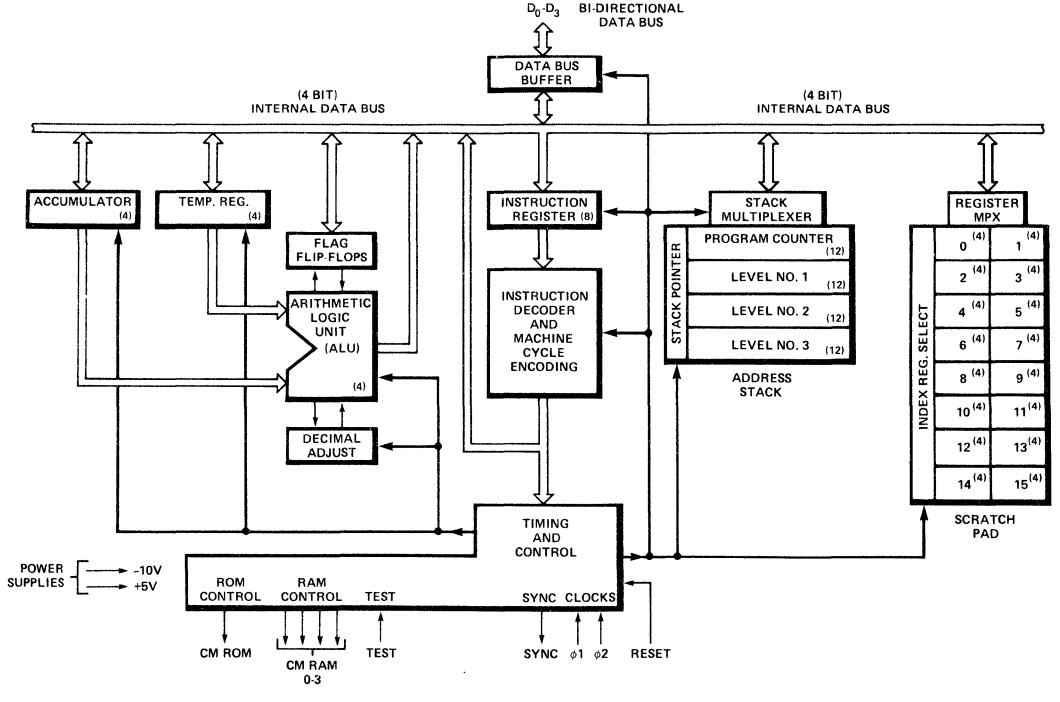
4004
SINGLE CHIP 4-BIT P-CHANNEL MICROPROCESSOR

- **4-Bit Parallel CPU With 46 Instructions**
- **Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching**
- **Binary and Decimal Arithmetic Modes**
- **10.8 Microsecond Instruction Cycle**
- **CPU Directly Compatible With MCS-40 ROMs and RAMs**
- **Easy Expansion—One CPU can Directly Drive up to 32,768 Bits of ROM and up to 5120 Bits of RAM**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available With -40° to +85°C Operating Range**

The Intel® 4004 is a complete 4-bit parallel central processing unit (CPU). The 4004 easily interfaces with keyboards, switches, displays, A-D converters, printers and other peripheral equipment.

The CPU can directly address 4K 8-bit instruction words of program memory and 5120 bits of data storage RAM. Sixteen index registers are provided for temporary data storage. Up to 16 4-bit input ports and 16 4-bit output ports may also be directly addressed.

The 4004 is fabricated with P-channel silicon gate MOS technology.



4003

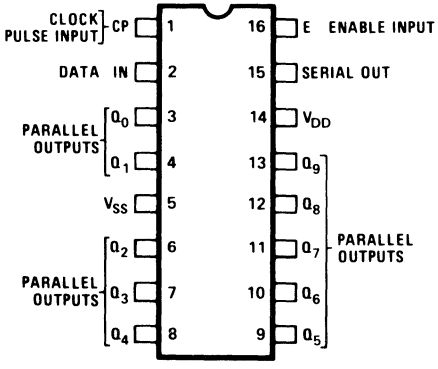
10-BIT SHIFT REGISTER/OUTPUT EXPANDER

- **10 Bit Serial-In/Parallel Out**
- **Serial-Out Capability for Additional I/O Expansion**
- **16 Pin Dual-In-Line Package**
- **Easy Expansion of I/O Output Capability**
- **Enable Output Control**
- **Standard Operating Temperature Range of 0° to 70°C**

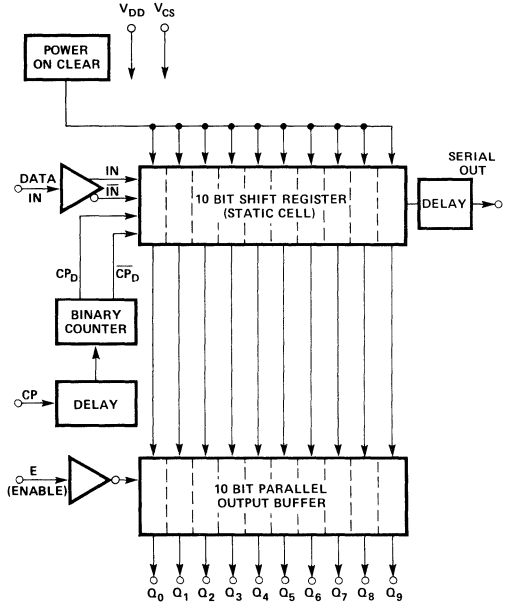
The 4003 is a 10 bit serial-in, parallel-out, serial-out shift register with enable logic. The 4003 is used to expand the number of ROM and RAM I/O ports to communicate with peripheral devices such as keyboards, printers, displays, readers, teletypewriters, etc.

The 4003 is a single phase static shift register; however, the clock pulse (CP) maximum width is limited to 10 msec. Data-in and CP can be simultaneous. To avoid race conditions, CP is internally delayed.

PIN CONFIGURATION



BLOCK DIAGRAM



4265
PROGRAMMABLE GENERAL PURPOSE I/O DEVICE

- **Multi-Mode 14 Operating Modes**
- **16 Lines of I/O Capability**
- **Bit Set/Reset**
- **Multiplexable Outputs**
- **Eight Bit Transfer Mode**
- **Interfaces to 8080 Peripherals**
- **Synchronous and Asynchronous Interface**
- **Strobed Buffer Inputs and Outputs**
- **TTL Interface**
- **Up to Eight 4265s Per System**
- **Interface to Standard RAMs**
- **28 Pin Dual-In-Line Package**
- **Interface to Standard RAMs**
- **28 Pin Dual-In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available with -40° to +85°C Operating Range**

The 4265 is a general purpose I/O device designed to interface with the MCS-40™ microcomputer family. This device provides four software programmable 4-bit I/O ports which can be configured to allow any one of fourteen unique operating modes for interfacing to data memory or a variety of user peripheral devices.

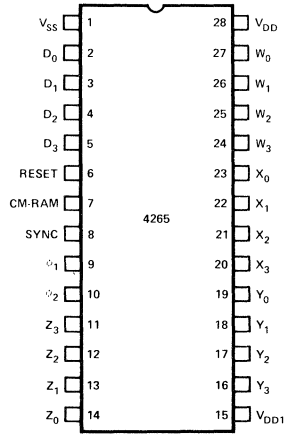
A single MCS-40 system can accomodate up to four 4265s (one per CM-RAM) without external logic or up to eight 4265s with one external decoder.

The 4265 resides on the MCS-40 data bus and uses the same selection procedure as 4002 RAM device. A valid compare selects the 4265 for MCS-40 I/O commands. As in the case of the 4002 or any MCS-40 peripheral circuit, selection occurs only when the proper SRC code and the CM signal are present simultaneously.

The 4265 provides an extremely flexible, general purpose I/O system capable of handling 4- or 8-bit input or output data. One of fourteen basic operating modes can be selected (software programmable) as described below.

Port Z is TTL compatible with any TTL device. Ports W, X, and Y are low-power TTL compatible.

PIN CONFIGURATION



4269
PROGRAMMABLE KEYBOARD DISPLAY DEVICE

Keyboard Features:

- **Programmable to Interface to Encoded Keyboard (8-bit code), 64-Key Scanned Keyboard (expandable to 128 keys) or Sensor Matrix (64 sensors)**
- **8 Character FIFO Character Buffer (or RAM in Sensor Mode)**
- **2 Key Rollover and Key Debounce**
- **External Interrupt Line to Indicate When a Character Has Been Entered in Character Buffer**

Display Features:

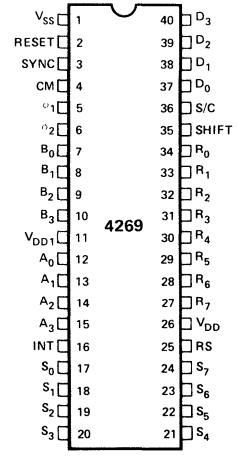
- **Programmable to Interface to Individually Scanned Displays or Burrough's Self-Scan* Drive (16, 18, or 20 Characters)**
- **Two 16 x 4 Display Registers Recirculated Synchronously with Keyboard Scan Lines to Give Automatic Display Refresh**
- **Display Registers Loadable and Readable Selectively or Sequentially**
- **40 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available with -40°C to +85°C Operating Range**

The 4269 has two separate and distinct sections: the keyboard section and the display section. The keyboard section can interface to a range of devices from a matrix of toggle or thumb switches such as found on an instrument panel up to a full typewriter style keyboard. The display section can interface to a range of devices from an array of individual LED indicators up to a gas discharge alphanumeric display.

The 4269 Programmable Keyboard Display (PKD) relieves the 4004 or 4040 CPU from continuously scanning a switch array or refreshing a display under software control. This greatly expands the CPU throughput. The 4269 can scan up to an 8 x 8 keyboard or sensor matrix (or a 2 x 8 x 8 keyboard with the use of the shift or control key input). The display portion can continuously refresh either a single 16 x 8 alphanumeric display; a single 8 x 8 alphanumeric display; a dual 16 x 4 digit display; a single 32 x 4 digit display; a 16 x 6, 18 x 6 or 20 x 6 alphanumeric gas discharge display such as the Burroughs Self-Scan*; or an array of 128 indicators.

*Self-Scan is a registered trademark of the Burroughs Corporation

PIN CONFIGURATION



4201A

CLOCK GENERATOR

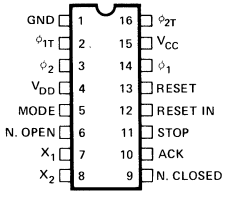
- **Complete Clock Requirements for MCS-40™ Systems**
- **Crystal Controlled Oscillator (XTAL External)**
- **MOS and TTL Level Clock Outputs**
- **Provides MCS-40 Reset Function Signal**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available with -40° to +85°C Operating Range**

The 4201A is a CMOS integrated circuit designed to fill the clock requirements of the MCS-40 microcomputer family. The 4201A contains a crystal controlled oscillator (XTAL external), clock generation circuitry, and both MOS and TTL level clock driver circuits.

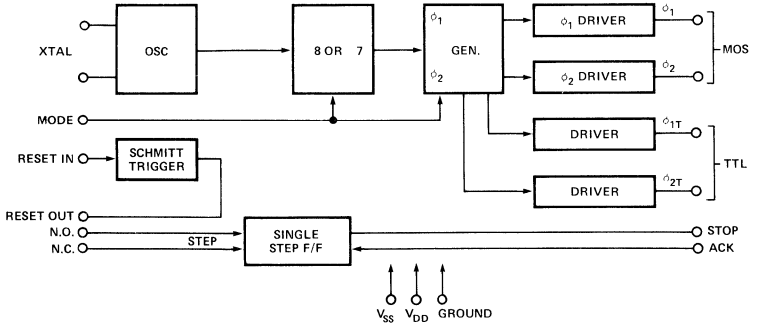
The 4201A also performs the power on reset function required by MCS-40 components and provides the logic necessary to implement the single-step function of the 4040 central processor unit.

PIN CONFIGURATION

4201A



BLOCK DIAGRAM



4289
STANDARD MEMORY INTERFACE

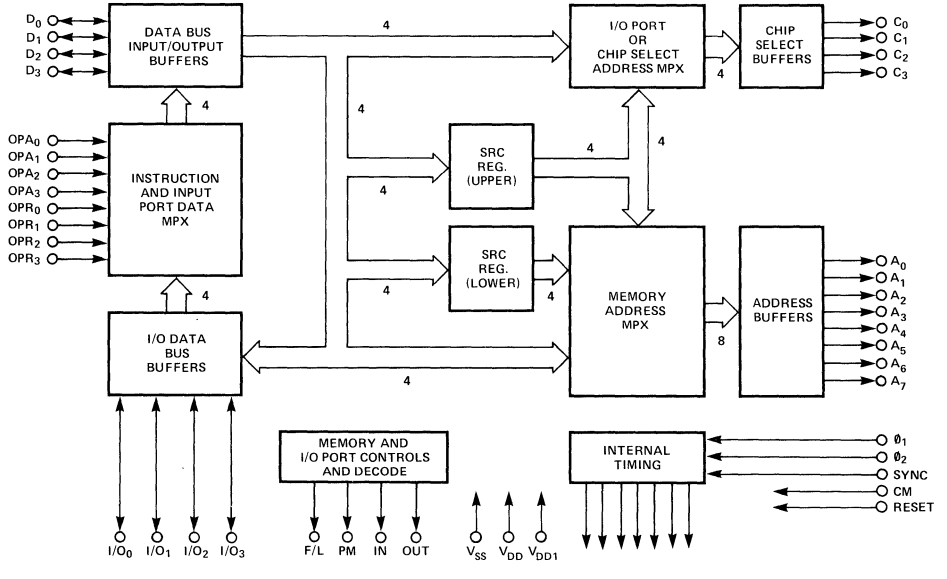
- **Direct Interface to all Standard Memories**
- **Allows Read and Write Program Memory**
- **Single Package Equivalent of 4008/4009**
- **TTL Compatible Address, Chip Select, Program Memory Data Lines**
- **40 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available With -40° to +85°C Operating Range**

The 4289 standard memory interface and I/O interface enables the CPU devices to utilize standard memory components as program data memory. Notably, PROMs (4702A), RAMs (2102) and ROMs can be arranged in a memory array to facilitate system development. Programs generated using the 4289 interface can be committed to MCS-40™ ROMs (4308 and 4001) with no change to software.

The 4289 also contains a 4 bit bi-directional I/O port and necessary steering logic to multiplex a host of I/O sources to the CPU. The Read and Write Program Memory instruction allows the user to store data and modify program memory. The device directly addresses 4K of program memory. The address is obtained sequentially during A_1-A_3 states of an instruction cycle. The eight bit instruction is presented to the CPU during M_1 and M_2 states of the instruction cycle via the four bit data bus.

The 4289 stores the SRC instruction operand as an I/O address and responds to the ROM I/O instructions (WRR and RDR) by reading or writing data to and from the processor and 4289 I/O bus.

BLOCK DIAGRAM



4002

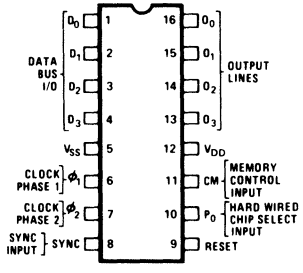
320-BIT RAM AND 4-BIT OUTPUT PORT

- **Four Registers of 20 4 Bit Characters**
- **Direct Interface to MCS-40™ 4 Bit Bus**
- **Output Port Low-Power TTL Compatible**
- **16 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available With -40° to +85°C Operating Range**

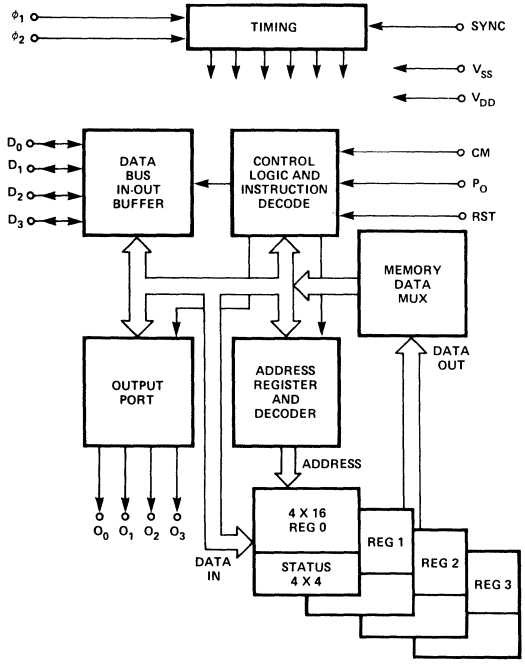
The 4002 performs two distinct functions. As a RAM it stores 320 bits arranged in 4 registers of twenty 4 bit characters each (16 main memory characters and 4 status characters). As a vehicle of communication with peripheral devices, it is provided with 4 output lines and associated control logic to perform output operations. The 4002 is a PMOS device and is compatible with all MCS-40™ components.

The 4002 is available in two options, the 4002-1 and 4002-2. Along with an external pin connected to either V_{DD} or V_{SS}, a two bit chip selection address is provided allowing a maximum of 1280 bits of 4002 RAM on a single MCS-40 CM-RAM line. Thus, the four CM-RAM lines give a maximum of 5120 bits of 4002 RAM in an MCS-40 system.

PIN CONFIGURATION



BLOCK DIAGRAM



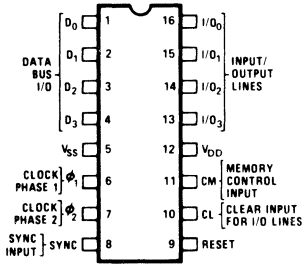
4001

256 x 8 MASK PROGRAMMABLE ROM AND 4-BIT I/O PORT

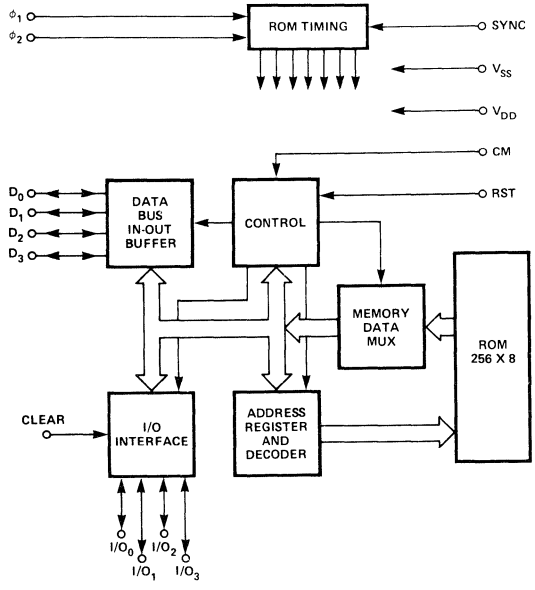
- **Direct Interface to MCS-40™ 4 Bit Data Bus**
- **I/O Port Low-Power TTL Compatible**
- **16 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4001 performs two basic and distinct functions. As a ROM it stores 256 x 8 words of program or data tables; as a vehicle of communication with peripheral devices it is provided with 4 I/O pins and associated control logic to perform input and output operations. The 4001 is a PMOS device, compatible with all other MCS-40™ devices.

PIN CONFIGURATION



BLOCK DIAGRAM



MCS® CUSTOM ROM ORDER FORM

4001 ROM

CUSTOMER_____

P.O. NUMBER_____

DATE_____

For Intel use only

S#_____ PPPP_____

STD_____ ZZ_____

_____ DD_____

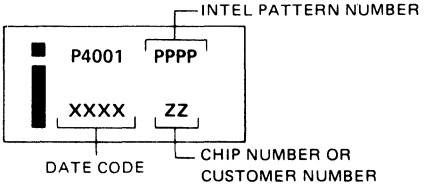
APP_____ DATE_____

All custom 4001 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4001), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).

CUSTOMER NUMBER _____



MASK OPTION SPECIFICATIONS

A. CHIP NUMBER _____.
(Must be specified—any number from 0 through 15—DD).

B. I/O OPTION – Specify the connection numbers for each I/O pin (next page). Examples of some of the possible I/O options are shown below:

EXAMPLES – DESIRED OPTION/CONNECTIONS REQUIRED

1. Non-inverting output – 1 and 3 are connected.
2. Inverting output – 1 and 4 are connected.
3. Non-inverting input (no input resistor) – only 5 is connected.
4. Inverting input (input resistor to V_{SS}) – 2, 6, 7, and 9 are connected.
5. Non-inverting input (input resistor to V_{DD}) – 2, 7, 8, and 10 are connected.
6. If inputs and outputs are mixed on the same port, the pins used as the outputs must have the internal resistor connected to either V_{DD} or V_{SS} (8 and 9 or 8 and 10 must be connected). This is necessary for testing purposes. For example, if there are two inverting inputs (with no input resistor) and two non-inverting outputs, the connection would be made as follows:

   Inputs – 2 and 6 are connected
   Outputs – 1, 3, 8, and 9 are connected or
   1, 3, 8, and 10 are connected

   If the pins on a port are all inputs or all outputs, the internal resistors do not have to be connected.

C. 4001 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. In the BPNF format, the characters should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

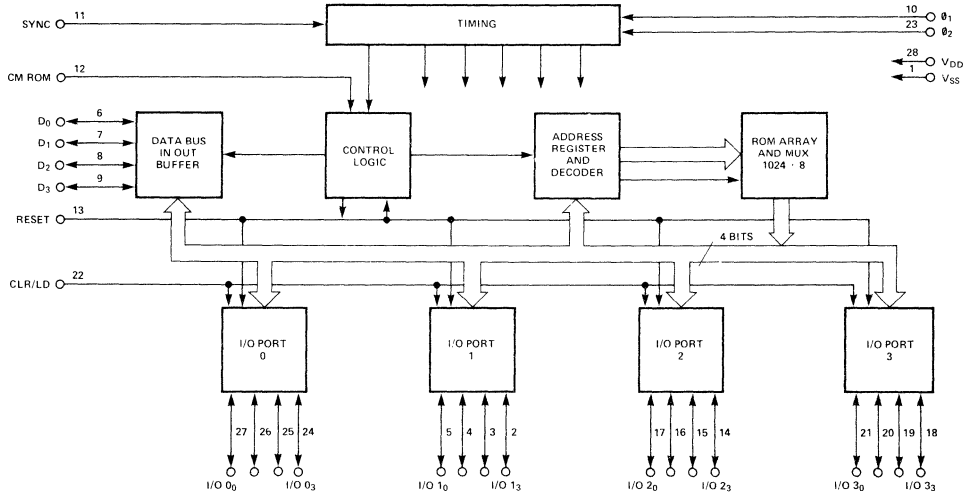
Hex input tapes for the 4001 and 4308 may also be generated by Intellec® Development Systems. These tapes are assumed to be negative logic. This means that a NOP instruction operation code (00000000), for example, would be coded as 00 in the HEX format. This would automatically result in the V_{IH} levels on the MCS 4/40 data bus. When the BPNF format is used, all logic representations must be inverted. Thus, a NOP would be represented as BPPPPPPPPF.

4308
1024 x 8 MASK PROGRAMMABLE ROM AND FOUR 4-BIT I/O PORTS

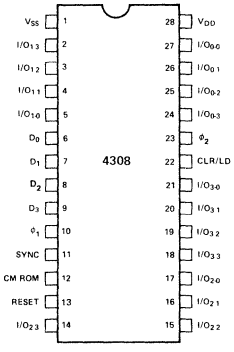
- **Direct Interface to MCS-40™ 4-Bit Data Bus**
- **Equivalent to Four 4001 ROMs**
- **Four Independent 4-Bit I/O Ports**
- **Input I/O Buffer Storage with an Optional Strobe**
- **I/O Ports Low-Power TTL Compatible**
- **28 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4308 is a 1024 x 8 bit word ROM memory with four I/O ports. It is designed for the MCS-40™ system and is operationally compatible with all existing MCS-40 elements. The 4308 is functionally identical to four 4001 chips. The 4308 has 16 I/O lines arranged in four groups of four lines.

BLOCK DIAGRAM



PIN CONFIGURATION



MCS® CUSTOM ROM ORDER FORM

4308 ROM

CUSTOMER _____

P.O. NUMBER _____

DATE _____

For Intel use only

S# _____ PPPP _____

STD _____ ZZ _____

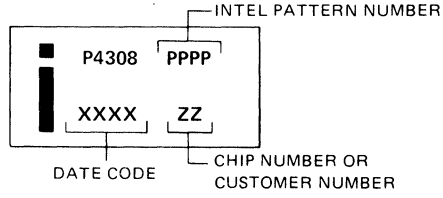
_____ DD _____

APP _____ DATE _____

All custom 4308 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4308), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).



CUSTOMER NUMBER _____

MASK OPTION SPECIFICATION

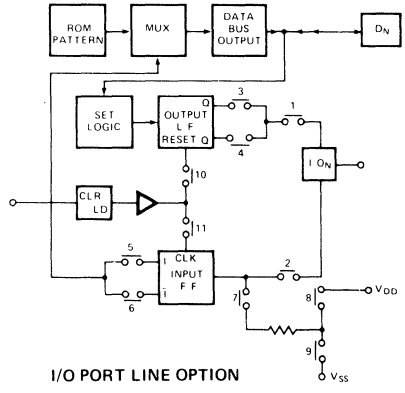
A. CHIP NUMBER _____ (Must be specified).

B. I/O OPTION – Specify the connection numbers for each I/O pin. See table below.

C. 4308 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. In the BPNF format, the characters should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

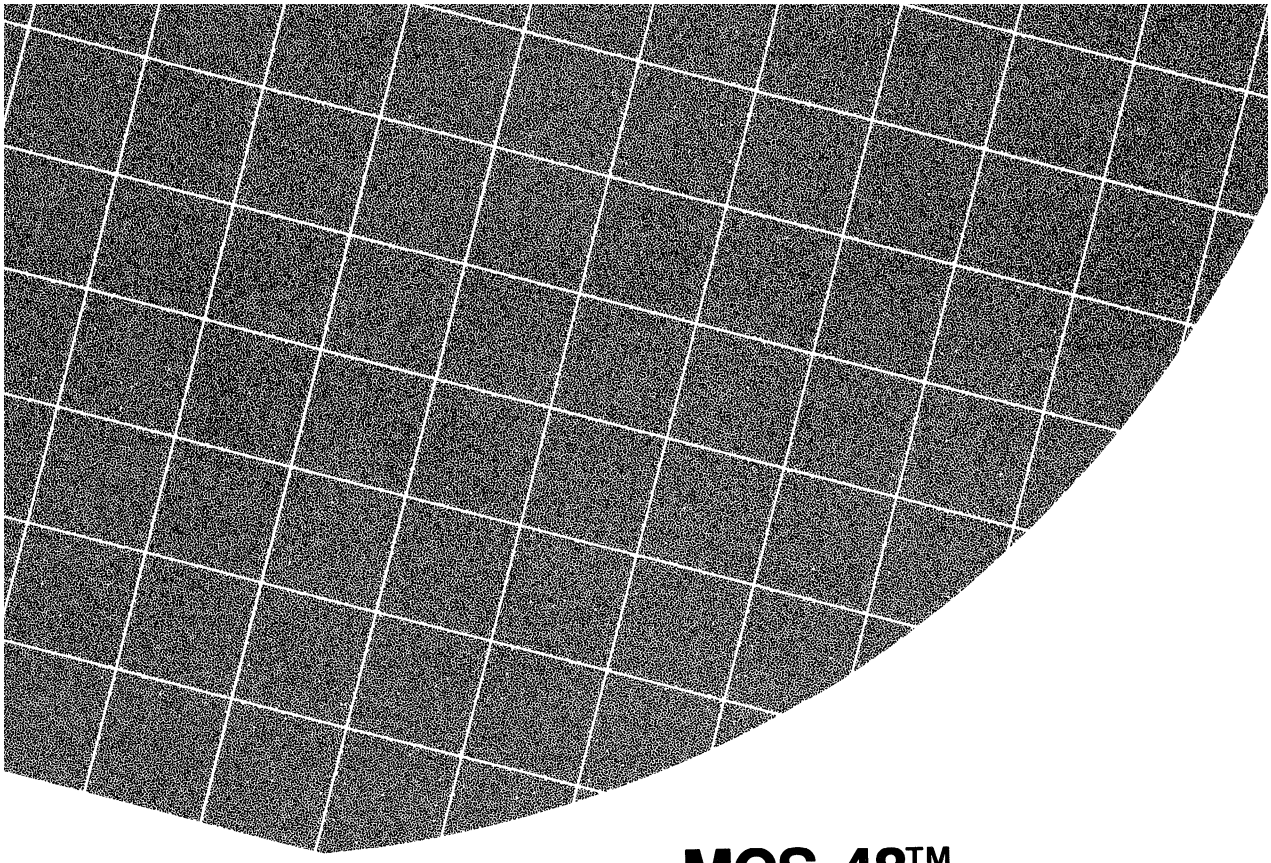
Hex input tapes for the 4001 and 4308 may also be generated by Intellec® Development Systems. These tapes are assumed to be negative logic. This means that a NOP instruction operation code (00000000), for example, would be coded as 00 in the HEX format. This would automatically result in the V_{IH} levels on the MCS 4/40 data bus. When the BPNF format is used, all logic representations must be inverted. Thus, a NOP would be represented as BPPPPPPPPF.

PIN		OPTION										
I/O 0_0	27	1	2	3	4	5	6	7	8	9	10	11
I/O 0_1	26	1	2	3	4	5	6	7	8	9	10	11
I/O 0_2	25	1	2	3	4	5	6	7	8	9	10	11
I/O 0_3	24	1	2	3	4	5	6	7	8	9	10	11
I/O 1_0	5	1	2	3	4	5	6	7	8	9	10	11
I/O 1_1	4	1	2	3	4	5	6	7	8	9	10	11
I/O 1_2	3	1	2	3	4	5	6	7	8	9	10	11
I/O 1_3	2	1	2	3	4	5	6	7	8	9	10	11
I/O 2_0	17	1	2	3	4	5	6	7	8	9	10	11
I/O 2_1	16	1	2	3	4	5	6	7	8	9	10	11
I/O 2_2	15	1	2	3	4	5	6	7	8	9	10	11
I/O 2_3	14	1	2	3	4	5	6	7	8	9	10	11
I/O 3_0	21	1	2	3	4	5	6	7	8	9	10	11
I/O 3_1	20	1	2	3	4	5	6	7	8	9	10	11
I/O 3_2	19	1	2	3	4	5	6	7	8	9	10	11
I/O 3_3	18	1	2	3	4	5	6	7	8	9	10	11



I/O PORT LINE OPTION

NOTE: Options 10 and 11 cannot both be specified.



MCS-48™ Microcomputers 8

MCS-48™ MICROCOMPUTERS

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8049/8039/8039-6 Single Component 8-Bit Microcomputer 8-31

Input/Output

8243 MCS-48™ Input/Output Expander 8-36

INTRODUCTION

Recent advances in NMOS technology have allowed Intel for the first time to place enough capability on a single silicon die to create a true single chip microcomputer containing all the functions required in a digital processing system. This microcomputer, its variations, and its optional peripherals are collectively called the MCS-48 microcomputer family and are fully described in this manual.

The head of the family is the 8048 microcomputer which contains the following functions in a single 40-pin package:

8-Bit CPU
1K x 8 ROM program memory
64 x 8 RAM data memory
27 I/O lines
8-bit timer/event counter

A 2.5 or 5.0 microsecond cycle time and a repertoire of over 90 instructions each consisting of either one or two cycles makes the single chip 8048 the equal in performance of most presently available multi-chip NMOS microprocessors, yet the 8048 is a true "low-cost" microcomputer. A single 5V supply requirement for all MCS-48 components assures that "low cost" also applies to the power supply in your system.

Even with low component costs, however, a project may be jeopardized by high development and rework costs resulting from an inflexible production design. Intel has solved this problem by creating two pin-compatible versions of the 8048 microcomputer: the 8048 with mask programmable ROM program memory for low cost production and the 8748 with user programmable and erasable EPROM program memory for prototype development. The 8478 is essentially a single chip microcomputer "breadboard" which can be modified over and over again during development and pre-production, then simply replaced by the low cost 8048 ROM for volume production. The 8748 provides a very easy transition from development to production and also provides an easy vehicle for temporary field updates while new ROMs are being made.

To allow the MCS-48 to solve a wide range of problems and to provide for future expansion, all 8048 functions have been made externally expandable using either special expanders or standard memories and peripherals. An efficient low cost means of I/O expansion is provided by the 8243 Input/Output Expander which provides 16 I/O lines in a 24-pin package. For systems with large I/O requirements, multiple 8243s can be used.

For such applications as keyboards, displays, serial communication lines, etc., standard MCS-80™ (8080) and MCS-85™ (8085) peripheral circuits may be added. Program and data memory may be expanded using standard memories or the 8355 and 8155 memories that also include programmable I/O lines and timing functions.

The 8035 is an 8048 without internal program memory that allows the user to match his program memory requirements exactly by using a wide variety of external memories. The 8035 allows the user to select a minimum cost system no matter what his program memory requirements.

The 8048 was designed to be an efficient control processor as well as an arithmetic processor with an instruction set which allows the user to directly set and reset individual lines within its I/O ports as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions make the 8048 very efficient in implementing standard logic functions. Special attention was also given to code efficiency with over 70% of the instructions being single byte and all others being only two bytes. This means many functions requiring 1.5K to 2.0K bytes in other processors may very well be compressed into the 1K words resident in the 8048.

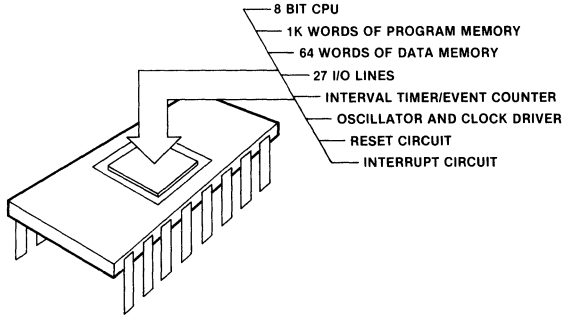


Figure 1. On Chip Features

SPECIAL FEATURES

- **Single 5V Supply**
- **40-Pin DIP**
- **Pin Compatible ROM and EPROM**
- **2.5 and 5.0 μsec Cycle Versions**
- **All Instructions 1 or 2 Cycles**
- **Single Step**
- **8-Level Stack**
- **2 Working Register Banks**
- **RC, XTAL, or External Frequency Source**
- **Clock per Cycle and Optional Clock per State Output**

8021
SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8-Bit CPU, ROM, RAM, I/O in Single 28-Pin Package**
- **Single 5V Supply (+4.5V to 6.5V)**
- **8.38 μsec Cycle With 3.58 MHz XTAL; All Instructions 1 or 2 Cycles**
- **Instructions —8748 Subset**
- **High Current Drive Capability—2 Pins**
- **1K × 8 ROM**
  64 × 8 RAM
  21 I/O Lines
- **Interval Timer/Event Counter**
- **Clock Generated With Single Resistor or Inductor**
- **Zero-Cross Detection Capability**
- **Easily Expandable I/O**

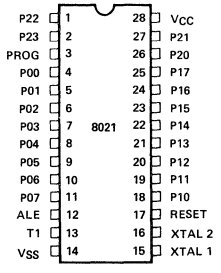
The Intel® 8021 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process. The features of the 8021 include a subset of the 8048 optimized for low cost, high volume applications, plus additional I/O flexibility and power.

The 8021 contains a 1K X 8 program memory, a 64 X 8 data memory, 21 I/O lines, and an 8-bit timer/event counter, in addition to on-board oscillator and clock circuits. For systems that require extra I/O capability, the 8021 can be expanded using the 8243 or discrete logic.

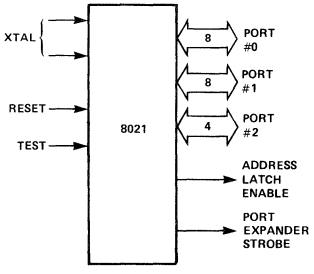
This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8021 has bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

To minimize development problems and maximize flexibility, an 8021 system can be easily designed using the 8021 emulation board, EMB-21. The EMB-21 contains a 40-pin socket which can accommodate either the 8748 shipped with the board or an ICE-48 plug. Also, the necessary discrete logic to reproduce the 8021's additional I/O features is included.

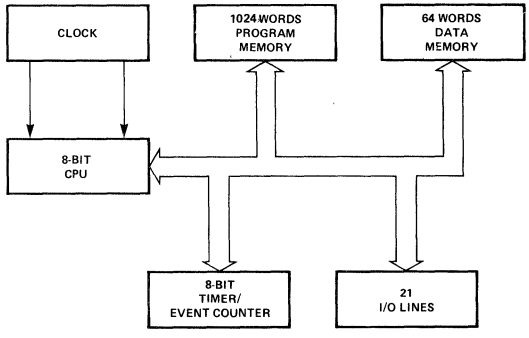
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All except XTAL1, XTAL2)	-0.5		0.8	V	
V_{IH}	Input High Voltage (All except XTAL1, XTAL2)	2.0		V_{CC}	V	$V_{CC} = 5.0V \pm 10\%$
V_{IH_1}	Input High Voltage (All except XTAL1, XTAL2)	3.0		V_{CC}	V	$V_{CC} = 5.5V \pm 1V$
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 1.6$ mA
V_{OL_1}	Output Low Voltage (P10, P11)			2.5	V	$I_{OL} = 7$ mA
V_{OH}	Output High Voltage (All unless Open Drain)	2.4			V	$I_{OH} = 50\,\mu A$
I_{OL}	Output Leakage Current (Open Drain Option — Port 0)			±10	μA	$V_{SS} + 0.45 \leqslant V_{IN} \leqslant V_{CC}$
I_{CC}	V_{CC} Supply Current			100	mA	

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CY}	Cycle Time	8.38	50.0	μsec	3 MHz XTAL = 10 μsec t_{CY}
Δ_F	Oscillator Frequency Variation -Resistor Mode	-20	+20	%	F = 2.5 MHz

A.C. TEST CONDITIONS

Control Outputs: $C_L = 80$ pF

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	14	Circuit GND potential
V_{CC}	28	+5V power supply
PROG	3	Output strobe for 8243 I/O Expander
P00–P07 Port 0	4–11	8-bit quasi-bidirectional port
P10–P17 Port 1	18–25	8-bit quasi-bidirectional port
P20–P23 Port 2	26–27 1–2	4-bit quasi-bidirectional port P20–P23 also serve as a 4-bit I/O expander bus for 8243
T1	13	Input pin testable using the JT1 and JNT1 instructions. Can be designated the timer/event counter input using the STRT CNT instruction. Also allows zero-crossover sensing of slowly moving AC inputs.
RESET	17	Input used to initialize the processor by clearing status flip-flops and setting program counters to zero.
ALE	12	Address Latch Enable. Signal occuring once every 30 input clocks, used as an output clock.
XTAL1	15	One side of crystal, inductor, or resistor input for internal oscillator. Also input for external source. (Not TTL compatible.)
XTAL2	16	Other side of timing control element.

INSTRUCTION SET*

	Mnemonic		Description	Bytes	Cycle
Accumulator	ADD	A,R	Add register to A	1	1
	ADD	A,@R	Add data memory to A	1	1
	ADD	A,#data	Add immediate to A	2	2
	ADDC	A,R	Add with carry	1	1
	ADDC	A,@R	Add with carry	1	1
	ADDC	A,#data	Add with carry	2	2
	ANL	A,R	And register to A	1	1
	ANL	A,@R	And data memory to A	1	1
	ANL	A,#data	And immediate to A	2	2
	ORL	A,R	Or register to A	1	1
	ORL	A,@R	Or data memory to A	1	1
	ORL	A,#data	Or immediate to A	2	2
	XRL	A,R	Exclusive Or register to A	1	1
	XRL	A,@R	Exclusive or data memory to A	1	1
	XRL	A,#data	Exclusive or immediate to A	2	2
	INC	A	Increment A	1	1
	DEC	A	Decrement A	1	1
	CLR	A	Clear A	1	1
	CPL	A	Complement A	1	1
	DA	A	Decimal Adjust A	1	1
	SWAP	A	Swap nibbles of A	1	1
	RL	A	Rotate A left	1	1
	RLC	A	Rotate A left through carry	1	1
	RR	A	Rotate A right	1	1
	RRC	A	Rotate A right through carry	1	1
Input/Output	IN	A,P	Input port to A	1	2
	OUTL	P,A	Output A to port	1	2
	MOVD	A,P	Input Expander port to A	1	2
	MOVD	P,A	Output A to Expander port	1	2
	ANLD	P,A	And A to Expander port	1	2
	ORLD	P,A	Or A to Expander port	1	2
Registers	INC	R	Increment register	1	1
	INC	@R	Increment data memory	1	1
Branch	JMP	addr	Jump unconditional	2	2
	JMPP	@A	Jump indirect	1	2
	DJNZ	R,addr	Decrement register and Jump on R not zero	2	2

	Mnemonic		Description	Bytes	Cycle
Branch	JC	addr	Jump on Carry = 1	2	2
	JNC	addr	Jump on Carry = 0	2	2
	JZ	addr	Jump on A Zero	2	2
	JNZ	addr	Jump on A not Zero	2	2
	JT1	addr	Jump on T1 = 1	2	2
	JNT1	addr	Jump on T1 = 0	2	2
	JTF	addr	Jump on timer flag	2	2
Subroutine	CALL	addr	Jump to subroutine	2	2
	RET		Return	1	2
Flags	CLR	C	Clear Carry	1	1
	CPL	C	Complement Carry	1	1
Data Moves	MOV	A,R	Move register to A	1	1
	MOV	A,@R	Move data memory to A	1	1
	MOV	A,#data	Move immediate to A	2	2
	MOV	R,A	Move A to register	1	1
	MOV	@R,A	Move A to data memory	1	1
	MOV	R,#data	Move immediate to register	2	2
	MOV	@R,#data	Move immediate to data memory	2	2
	XCH	A,R	Exchange A and register	1	1
	XCH	A,@R	Exchange A and data memory	1	1
	XCHD	A,@R	Exchange nibble of A and register	1	1
	MOVP	A,@A	Move to A from current page	1	2
Timer/Counter	MOV	A,T	Read Timer/Counter	1	1
	MOV	T,A	Load Timer/Counter	1	1
	STRT	T	Start Timer	1	1
	STRT	CNT	Start Counter	1	1
	STOP	TCNT	Stop Timer/Counter	1	1
	NOP		No Operation	1	1

*See July, 1978 MCS-48 User's Manual for opcodes.

FUNCTIONAL SPECIFICATIONS

The following is a functional description of the major elements of the 8021.

Program Memory

The 8021 contains 1K X 8 of mask programmable ROM. No external ROM expansion capability is provided.

Data Memory

A 64 X 8 dynamic RAM is located on chip for data storage. All locations are indirectly addressable and eight designated locations are directly addressable. Also, included in the memory is the address stack, addressed by a 3-bit stack pointer.

Memory is organized as shown in Figure 1. The least significant 8 addresses, 0—7, are directly addressable by any of the 11 direct register instructions. The locations are readily accessible for a variety of operations with the least number of instruction bytes required for their manipulation.

Registers 0 and 1 have yet another function, in that they can be used to indirectly address all locations in memory, using the indirect register instructions. These indirect RAM address registers, IRAR's, are especially useful for repetitive-type operations on adjacent memory locations. The indirect register instruction specifies which IRAR to use, and the contents of the IRAR is used to address a location in RAM. The contents of the addressed location is used during the execution of the instruction, and may be modified. A value larger than 63 should not be preset in the IRAR when selected by an indirect register instruction. IRAR's may point to addresses 0—7, if desired.

Locations 8—23 may be used as the address stack. The address stack enables the processor to keep track of the return addresses generated from CALL instructions. A 3-bit stack pointer (SP) supplies the address of the locations to be loaded with the next return address generated. The SP to this pushdown stack is incremented by one after a return address is stored, and decremented by one before an address is fetched during a RET. A total of 8 levels of nesting is possible. The SP is initialized to location 8 upon RESET. Since each address is 10 bits long, two bytes must be used to store a single address. The SP is incremented and decremented by one, but each increment or decrement moves the address pointed to by two. Therefore, only even numbered addresses are pointed to.

If a particular application does not require 8 levels of nesting, the unused portion of the stack may be used as any other indirectly addressable scratchpad location. For example, if only 3 levels of subroutine nesting are used, then only locations 8—15 need be reserved for the address stack, and locations 16—63 can be used for data storage. The actual program counter address is not stored in the address stack. A separate register retains its value.

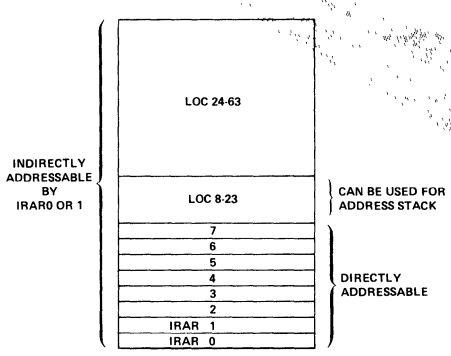


Figure 1. Internal RAM Organization

Oscillator and Clock

The 8021 contains its own onboard oscillator and clock circuit, requiring only an external timing control element. This control element can be a crystal, inductor, resistor, or clock in. The capacitor normally required in resistor or inductor timing control operation is integrated onto the 8021. All internal time slots are derived from the external element, and all outputs are a function of the oscillator frequency. Pins X1 and X2 are used to input the particular control element. An instruction cycle consists of 10 states, and each state is a time slot of 3 oscillator periods. Therefore, to obtain a 10 μsec instruction cycle, a 3 MHz crystal should be used.

Timer/Event Counter

An interval timer is available to enable the user to keep track of time elapsed or number of events occurred, during normal program execution and flow.

By a MOV T,A instruction, the contents of the accumulator are loaded to the timer. At the STRT T command an internal prescaler is zeroed and thereafter increments once each 30 input clocks (once each single cycle instruction, twice each double cycle instruction). The prescaler is a divide by 32. At the (11111) to (00000) transition the timer is incremented. The timer is 8 bits and an overflow (FFH) to (00H) timer flag is set. A conditional branch is available for testing this flag, the flag being reset each test. Total count capacity for the timer is $2^8 \times 2^5 = 8192$ or 81.9 msec at a 10 μsec cycle time. Contents of the timer are moved to the accumulator by the MOV A,T instruction without disturbing the counting process.

The timer may also be used as an event counter. After a STRT CNT command, the chip will respond to a high to low transition on the Test 1 pin by incrementing the timer. Transitions can occur no faster than one each three instruction cycles.

The timer and event functions are exclusive. Counting or timing may be started or stopped (STOP TCNT) at will.

Input/Output Capabilities

The 8021 I/O configurations are highly flexible. A number of different configurations are possible, tailoring an 8021 to a given task. Other than the power supply and dedicated pins, all other pins (20) can be used for input, output, or both, depending on the configuration.

P20–P23 and P10–P17 are quasi-bidirectional, and Test 1 is directly testable through program control. A simplified schematic of the quasi-bidirectional interface is shown in Figure 2. This configuration allows buffered outputs, and also allows external input. When writing a "0" or low value to these ports, the large pulldown device sinks an external TTL load. When writing a "1", a large current is supplied through the large pullup device to allow a fast data transfer. After a short time (less than one instruction cycle), the large device is shut off and the small pullup maintains the "1" level indefinitely. However, in this situtation, an input device capable of overriding the small amount of sustaining current supplied by the pullup device can be read. (Alternatively, the data written can be read). So, by writing a "1" to any particular pin, that pin can serve either as a true high-level latched output pin, or as just a pullup resistor on an input. This allows maximum user flexibility in selecting his input or latched output pins, with a minimum of external components.

Port 00–07 is also quasi-bidirectional, except there is no large pullup device. As outputs, this port is essentially open drain.

By mask option the small pullup devices on P00–P07 may be deleted on any pin providing a true open drain output. This is useful in driving analog circuits and certain loads, such as keyboards.

Also available is the 8243 I/O expander chip, which provides additional I/O capability with a limited number of overhead pins. This chip has 4 directly addressable 4-bit ports. It connects to the PROG pin, which provides a clock, and pins P20–P23, which provide address and data. These ports can be written with a MOVD P,A; ANLD P,A; and ORLD P,A for Ports 4–7. A high to low transition on PROG signifies that address and control are available on P20–P23. The previous data on P20–P23 before an output expander instruction is lost. Therefore, when using an output expander P20–P23 are not useful for general input/output. Reading is via the MOVD A,P. This circuit configuration is shown in Figure 3.

The Test 1 pin has a special bias input that allows zero-crossover sensing of slowly moving inputs. This is especially useful in SCR control of 60 Hz power and in developing time of day routines. As a ROM mask option there is a pullup resistor that is useful for switch contact input or standard TTL. See Figure 4.

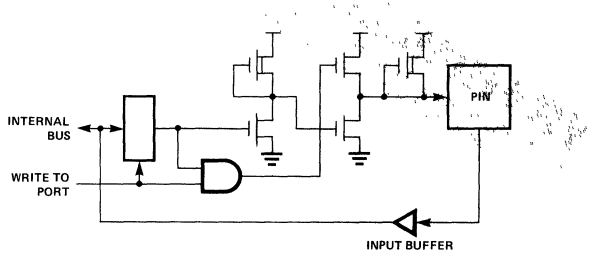


Figure 2. Quasi-Bidirectional Port Structure

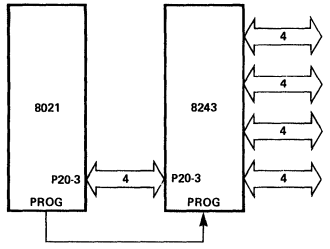


Figure 3. I/O Expander Interface

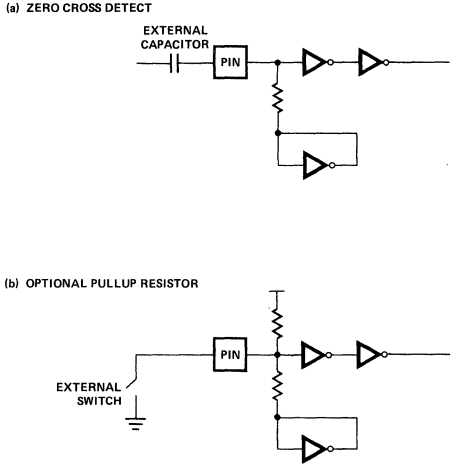


Figure 4. Test 1 Pin

CPU

The 8021 CPU has arithmetic and logical capability. A wide variety of arithmetic and logic instructions may be exercised, which affect the contents of the accumulator, and/or direct or indirect scratchpad locations. Provisions have been made for simplified BCD arithmetic capability through the use of the DAA, SWAP A, and XCHD instructions. In addition, MOVP A,@A allows table lookup for display formating and constants. Jump conditions such as zero, not zero refer to the accumulator contents at the time of the condition.

Reset

The 8021 may see poorly regulated and noisy power supplies. A useful feature is to sense when the power supply dips and do a reset to prevent continued operation with incorrect data. This feature may be implemented on the 8021 by connecting a diode between the RESET node and ground. See Figure 5.

A reset will then be forced if the supply drops approximately 1.5 volts and rapidly recovers. One instruction cycle will reset the 8021 to the initialized state.

By removing the diode and using only the capacitor, voltage drops in V_{CC} will not cause a RESET.

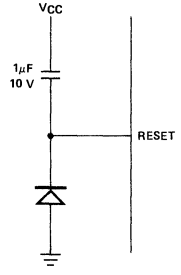


FIGURE 5. POWER ON RESET

Differences Between the 8021 and the 8748

Although the 8021 is basically an electrical and functional subset of the 8748, there are some differences:

1. *Pin Out* — As the 8021 is a 28-pin DIP, some form of adapter must be used to interface the 8021 socket to ICE-48. An emulation board, EM-1, has been designed to perform this function. The EM-1 also accounts for the increased flexibility of some 8021 I/O lines.
2. *Instruction Time* — The 8021 instruction cycle is 30 clock cycles long, the 8748 instruction cycle is 15 clocks long. Where exact timing is important the 8748 breadboard part should be operated at half the 8021 clock rate.
3. *Test 1* — To facilitate developing time of day routines from 60 Hz, and for SCR control, the Test 1 pin without the pullup resistor option will detect zero crossing of a capacitively coupled AC input.
4. *Quasi-Bidirectional Ports* — All 8021 ports are quasi-bidirectional to facilitate stand-alone use. Port 0 has open drain outputs and by mask option it may or may not have pullup resistors.
5. *Oscillator* — The 8021 has on-chip oscillator that is optimized for the single resistor mode. External connection will differ from the 8748.
6. *Dynamic RAM and Logic* — The 8021 utilizes dynamic RAM and some dynamic logic. Input clocking must be maintained above the minimum rate or improper operation may result.
7. *High Current Outputs* — Very high current drive is desirable for minimizing external parts required to do high power control. P10 and P11 have been designated high drive outputs capable of sinking 7 mA at V_{SS} +2.5 volts. (For clarity, this is 7 mA to V_{SS} with a 2.5 volt drop across the buffer.) These pins may, of course, be paralleled for 14 mA drive if the output logic states are always the same.
8. *Reset* — Reset has been modified on the 8021, as previously noted. A reset will be forced if the power supply drops approximately 1.5 volts and rapidly recovers, if a diode is used in the reset circuit. This prevents continued operation with incorrect data caused by a poorly regulated and/or noisy power supply.
9. *Instruction Set* — The following instructions, which are found in the 8748, have been deleted from the 8021 instruction set.

Data Moves	Registers	Branch	Timer	Control	Input/Output
MOV A,PSW	DEC R	JT0 addr	EN TCNTI	EN I	ANL P,#data
MOV PSW,A		JNT0 addr	DIS TCNTI	DIS I	ORL P,#data
MOVX A,@R	**Flags**	JF0 addr		SEL RB0	INS A,BUS *
MOVX @R,A	CLR F0	JF1 addr	**Subroutine**	SEL RB1	OUTL BUS,A *
MOVP3 A,@A	CPL F0	JNI addr	RETR	SEL MB0	ANL BUS,#data
	CLR F1	JBb addr		SEL MB1	ORL BUS,#data
	CPL F1			ENT0 CLK	

*These Instructions have been replaced in the 8021 by IN A,P0 and OUTL P0,A respectively.

8022
SINGLE COMPONENT 8-BIT MICROCOMPUTER WITH ON-CHIP A/D CONVERTER

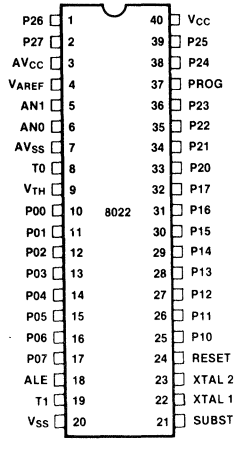
- 8-Bit CPU, ROM, RAM, I/O in Single 40-Pin Package
- On-Chip 8-Bit A/D Converter; Two Input Channels
- 8 Comparator Inputs (Port 0)
- Zero-Cross Detection Capability
- Single 5V Supply (4.5V to 6.5V)
- High Current Drive Capability — 2 Pins
- Two Interrupts — External and Timer
- 2K x 8 ROM, 64 x 8 RAM, 28 I/O Lines
- 8.38 μsec Cycle; All Instructions 1 or 2 Cycles
- Instructions — 8048 Subset
- Interval Timer/Event Counter
- Clock Generated with Single Resistor, Inductor, or Crystal
- Easily Expandable I/O

The Intel® 8022 is the newest member of the MCS-48™ family of single chip 8-bit microcomputers. It is designed to satisfy the requirements of low cost, high volume applications which involve analog signals, capacitive touchpanel keyboards, and/or large ROM space. The 8022 addresses these applications by integrating many new functions on-chip, such as A/D conversion, comparator inputs and zero-cross detection.

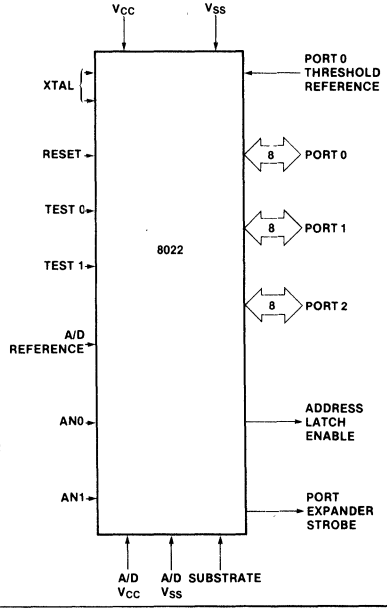
The features of the 8022 include 2K bytes of program memory (ROM), 64 bytes of data memory (RAM), 28 I/O lines, an on-chip 8-bit A/D converter with two input channels, an 8-bit port with comparator inputs for interfacing to low voltage capacitive touchpanels or other non-TTL interfaces, external and timer interrupts, and zero-cross detection capability. In addition, it contains the 8-bit interval timer/event counter, on-board oscillator and clock circuitry, single 5V power supply requirement, and easily expandable I/O structure common to all members of the MCS-48 family.

The 8022 is designed to be an efficient controller as well as an arithmetic processor. It has bit handling capability plus facilities for both binary and BCD arithmetic. Efficient use of program memory results from using the MCS-48 instruction set which consists mostly of single byte instructions and has extensive conditional jump and direct table lookup capability. Program memory usage is further reduced via the 8022's hardware implementation of the A/D converter which simplifies interfacing to analog signals.

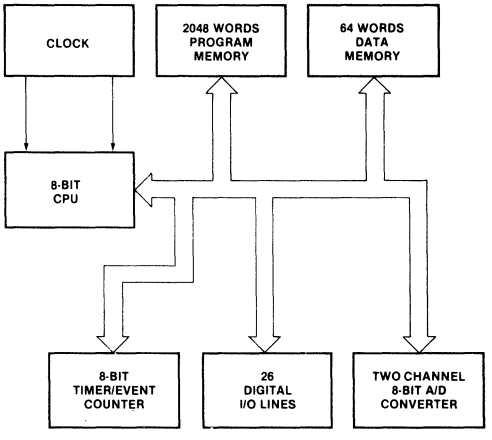
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential.
V_{CC}	40	+5V circuit power supply.
PROG	37	Output strobe for Intel® 8243 I/O expander.
P00-P07 Port 0	10-17	8-bit open-drain port with comparator inputs. The switching threshold is set externally by V_{TH}. Optional pull-up resistors may be added via ROM mask selection.
V_{TH}	9	Port 0 threshold reference pin.
P10-P17 Port 1	25-32	8-bit quasi-bidirectional port.
P20-P27 Port 2	33-36 38-39 1-2	8-bit quasi-bidirectional port. P20-23 also serve as a 4-bit I/O expander for Intel® 8243.
T0	8	Interrupt input and input pin testable using the conditional transfer instructions JT0 and JNT0. Initiates an interrupt following a low level input if interrupt is enabled. Interrupt is disabled after a reset.
T1	19	Input pin testable using the JT1 and JNT1 conditional transfer instructions. Can be designated the timer/event counter input using the STRT CNT instruction. Also serves as the zero-cross detection input to allow zero-crossover sensing of slowly moving AC inputs. Optional pull-up resistor may be added via ROM mask selection.
RESET	24	Input used to initialize the processor by clearing status flip-flops and setting the program counter to zero.
AV_{SS}	7	A/D converter GND Potential. Also establishes the lower limit of the conversion range.
AV_{CC}	3	A/D +5V power supply.
SUBST	21	Substrate pin used with a bypass capacitor to stabilize the substrate voltage and improve A/D accuracy.
V_{AREF}	4	A/D converter reference voltage. Establishes the upper limit of the conversion range.
AN0, AN1	6,5	Analog inputs to A/D converter. Software selectable on-chip via SEL AN0 and SEL AN1 instructions.
ALE	18	Address Latch Enable. Signal occurring once every 30 input clocks (once every cycle), used as an output clock.
XTAL 1	22	One side of crystal, inductor, or resistor input for internal oscillator. Also input for external frequency source. (Not TTL compatible.)
XTAL 2	23	Other side of timing control element. This pin is not connected when an external frequency source is used.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias.....0°C to 70°C
Storage Temperature.....-65°C to +180°C
Voltage on Any Pin with
Respect to Ground.....-0.5V to +7V
Power Dissipation.....1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permenent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All except XTAL 1, XTAL 2, Port 0)	-0.5		0.8	V	
V_{IL1}	Input Low Voltage (Port 0)	-0.5		$V_{TH} - 0.1$	V	
V_{IH}	Input High Voltage (All except XTAL 1, XTAL 2, RESET, Port 0)	2.0		V_{CC}	V	$V_{CC} = 5.0V \pm 10\%$
V_{IH1}	Input High Voltage (All except XTAL 1, XTAL 2, RESET, Port 0)	2.4		V_{CC}	V	$V_{CC} = 6.0V \pm 0.5V$
V_{IH2}	Input High Voltage (Port 0)	$V_{TH} + 0.1$		V_{CC}	V	
V_{IH3}	Input High Voltage (RESET, XTAL 1)	3.0		V_{CC}	V	
V_{TH}	Port 0 Threshold Reference Voltage	0		$V_{CC}/2$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{IL} = 1.6$ mA
V_{OL1}	Output Low Voltage (P10, P11)			2.5	V	$I_{OL} = 7$ mA
V_{OH}	Output High Voltage (All unless Open Drain Option—Port 0)	2.4			V	$I_{OH} = 50\ \mu A$
I_{LI}	Input Leakage Current (T1)			± 10	μA	$V_{IN} = V_{CC}$
I_{LO}	Output Leakage Current (Open Drain Option—Port 0)			± 10	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45V$
I_{CC}	V_{CC} Supply Current			100	mA	
V_{T1}	Zero-Cross Detection Input (T1)	1		3	VACpp	Input through a capacitor

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CY}	Cycle Time	8.38	50.0	μs	3 MHz XTAL = 10 μs t_{CY}
t_{LL}	ALE Pulse Width	4.6	23.0	μs	$t_{CY} = 10\ \mu s$
Δ_F	Oscillator Frequency Variation—Resistor Mode	-20	+20	%	F = 2.5 MHz, R = 15 kΩ
F_{T1}	Zero-Cross Detection Input Frequency (T1)	0.03	1	kHz	

A.C. TEST CONDITIONS

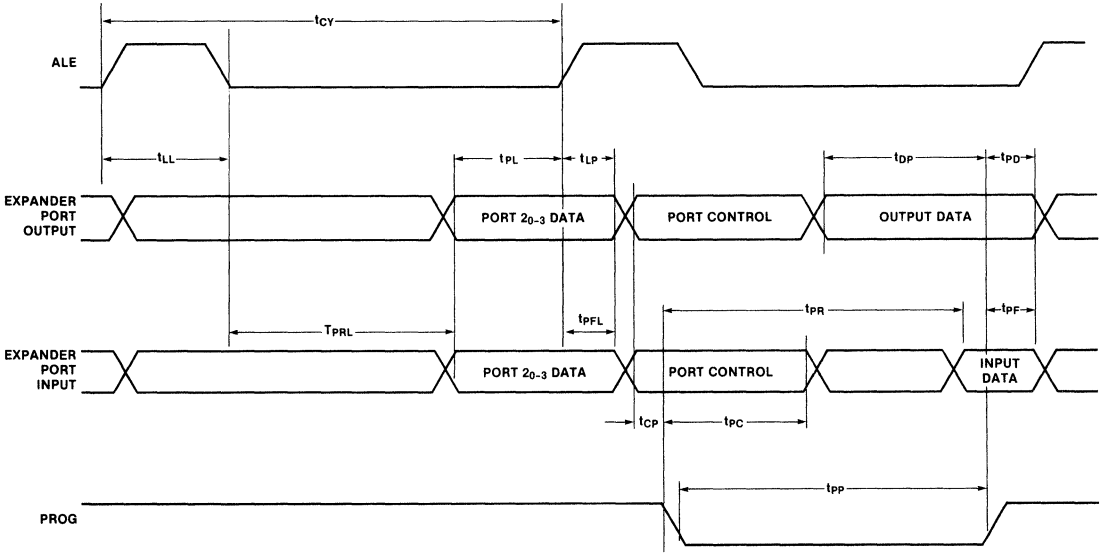
Control Outputs: $C_L = 80$ pF

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

	Symbol	Parameter	Min.	Max.	Unit	Notes
Expander Operation	t_{CP}	Port Control Setup Before Falling Edge of PROG	110		ns	
	t_{PC}	Port Control Hold After Falling Edge of PROG	140		ns	
	t_{PR}	PROG to Time P2 Input Must Be Valid		810	ns	
	t_{DP}	Output Data Setup Time	220		ns	
	t_{PD}	Output Data Hold Time	65		ns	
	t_{PF}	Input Data Hold Time	0	150	ns	
	t_{PP}	PROG Pulse Width	1510		ns	
	t_{PRL}	ALE to Time P2 Input Must Be Valid		810	ns	
Normal Operation	t_{PL}	Output Data Setup Time	400		ns	
	t_{LP}	Output Data Hold Time	150		ns	
	t_{PFL}	Input Data Hold Time	0		ns	

PORT 2 TIMING

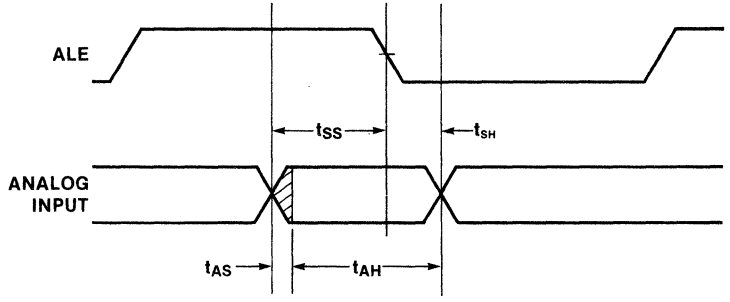


A/D CONVERTER CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$, $AV_{CC} = 5.5V \pm 1V$, $AV_{SS} = 0V$

Parameter	Min.	Typ.	Max.	Unit	Comments
Resolution	8			Bits	
Non-Linearity		± ½		LSB	(Note 1)
Zero Error		0		LSB	(Note 2) $T_A = 25°C$
Full Scale Error		0		LSB	(Note 3) $T_A = 25°C$
Absolute Accuracy		± 1		%	(Note 4)
Conversion Range	AV_{SS}		V_{AREF}	V	
V_{AREF}	$AV_{CC}/2$		AV_{CC}	V	
Input Capacitance (AN0, AN1)		1		pF	
Conversion Time	4		4	t_{CY}	
Sample Hold Time (t_{AS})		0.07		t_{CY}	(Note 5)
Sample Hold Time (t_{AH})		0.23		t_{CY}	(Note 5)
Sample Setup Before Falling Edge of ALE (t_{SS})		0.20		t_{CY}	
Sample Hold After Falling Edge of ALE (t_{SH})		0.10		t_{CY}	

ANALOG INPUT TIMING



MCS-48

NOTES:

1. Non-linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristics.
2. Zero error is the difference between the output of an ideal and the actual A/D for zero input voltage.
3. Full-scale error is the difference between the output of an ideal and the actual A/D for full-scale input voltage.
4. Absolute accuracy describes the difference between the actual input voltage and the full-scale weighted equivalent of the binary output. Included are quantizing and all other errors.
5. The analog input must be maintained at a constant voltage during the sampling time (t_{AS}) and the sample hold time (t_{AH}).

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle	Hexadecimal Opcode
Accumulator	ADD A,R_r	Add register to A	1	1	68-6F
	ADD A,@R	Add data memory to A	1	1	60-61
	ADD A,#data	Add immediate to A	2	2	03
	ADDC A,R_r	Add register with carry	1	1	78-7F
	ADDC A,@R	Add data memory with carry	1	1	70-71
	ADDC A,#data	Add immediate with carry	2	2	13
	ANL A,R_r	And register to A	1	1	58-5F
	ANL A,@R	And data memory to A	1	1	50-51
	ANL A,#data	And immediate to A	2	2	53
	ORL A,R_r	Or register to A	1	1	48-4F
	ORL A,@R	Or data memory to A	1	1	40-41
	ORL A,#data	Or immediate to A	2	2	43
	XRL A,R_r	Exclusive Or register to A	1	1	D8-DF
	XRL A,@R	Exclusive Or data memory to A	1	1	D0-D1
	XRL A,#data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67
Input/Output	IN A, P_p	Input port to A	1	2	08,09,0A
	OUTL P_pA	Output A to port	1	2	90,39,3A
	MOVD A,P_p	Input expander port to A	1	2	0C-0F
	MOVD P_p,A	Output A to expander port	1	2	3C-3F
	ANLD P_p,A	And A to expander port	1	2	9C-9F
	ORLD P_p,A	Or A to expander port	1	2	8C-8F
Registers	INC R_r	Increment register	1	1	18-1F
	INC @R	Increment data memory	1	1	10-11
Branch	JMP addr	Jump unconditional	2	2	04,24,33,64, 84,A4,C4,E4
	JMPP @A	Jump indirect	1	2	B3
	DJNZ R,addr	Decrement register and jump on R not zero	2	2	E8-EF
	JC addr	Jump on carry = 1	2	2	F6
	JNC addr	Jump on carry = 0	2	2	E6
	JZ addr	Jump on A zero	2	2	C6
	JNZ addr	Jump on A not zero	2	2	96
	JT0	Jump on T0 = 1	2	2	36
	JNT0	Jump on T0 = 0	2	2	26
	JT1 addr	Jump on T1 = 1	2	2	56
	JNT1 addr	Jump on T1 = 0	2	2	46
	JTF addr	Jump on timer flag	2	2	16
Subroutine	CALL	Jump to subroutine	1	2	14,34,54,74, 94,B4,D4,F4
	RET	Return	1	2	83
Flags	CLR C	Clear carry	1	1k	97
	CPL C	Complement carry	1	1	A7
Data Moves	MOV A,R_r	Move register to A	1	1	F8-FF
	MOV A,@R	Move data memory to A	1	1	F0-F1
	MOV A,#data	Move immediate to A	2	2	23
	MOV R_r,A	Move A to register	1	1	A8-AF
	MOV @R,A	Move A to data memory	1	1	A0-A1
	MOV R_r,#data	Move immediate to register	2	2	B8-BF
	MOV @R,#data	Move immediate to data memory	2	2	B0-B1
	XCH A,R_r	Exchange A and register	1	1	28-2F
	XCH A,@R	Exchange A and data memory	1	1	20-21
	XCHD A,@R	Exchange nibble of A and register	1	1	30-'31
	MOVP A,@A	Move to A from current page	1	2	A3
Timer/Counter	MOV A,T	Read timer/counter	1	1	42
	MOV T,A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
A/D Converter	RAD	Move conversion result register to A	1	2	80
	SEL AN0	Select analog input zero	1	1	85
	SEL AN1	Select analog input one	1	1	95
Interrupts	EN I	Enable external interrupt	1	1	05
	DIS I	Disable external interrupt	1	1	15
	EN TCNTI	Enable timer/counter interrupt	1	1	2 5
	DIS TCNTI	Disable timer/counter interrupt	1	1	35
	RET I	Return from interrupt	1	2	93
	NOP	No operation	1	1	00

SYMBOLS AND ABBREVIATIONS USED

A	Accumulator
addr	11-Bit Program Memory Address
AN0, AN1	Analog Input 0, Analog Input 1
CNT	Event Counter
data	8-Bit Number or Expression
I	Interrupt
P	Mnemonic for "in-page" Operation
P_p	Port Designator (P = 1, 2 or 4-7)
R_r	Register Designator (r = 0-7)
T	Timer
T0, T1	Test 0, Test 1
#	Immediate Data Prefix
@	Indirect Address Prefix

FUNCTIONAL DESCRIPTION

PROGRAM MEMORY

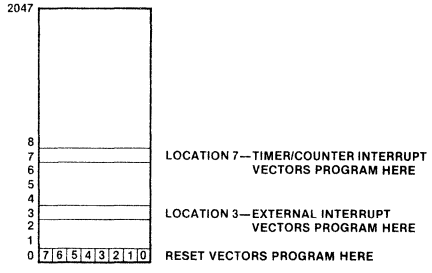
The 8022 program memory consists of 2048 words 8 bits wide which are addressed by the program counter. The memory is ROM which is mask programmable at the factory. No external ROM expansion capability is provided. There are three locations in program memory of special importance.

Location 0: Activating the RESET line of the processor causes the first instruction to be fetched from location 0.

Location 3: Activating the interrupt input line of the processor (if interrupt is enabled) causes a jump to subroutine.

Location 7: A timer/event counter interrupt resulting from a timer/counter overflow causes a jump to subroutine (if timer/counter interrupt is enabled).

Therefore, the first instruction to be executed after initialization is stored in location 0, the first word of an external interrupt service routine is stored in location 3, and the first word of a timer/event counter interrupt service routine is stored in location 7.



PROGRAM MEMORY MAP

Program memory can be used to store constants as well as program instructions. The MOVP instruction allows easy table lookup for constants and display formatting.

DATA MEMORY

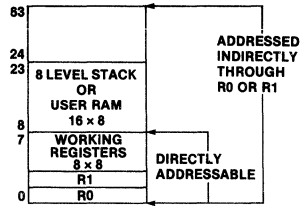
On-chip data memory is organized as 64 words eight bits wide. All locations are indirectly addressable and eight designated locations are directly addressable. Also included in the data memory is the program counter stack, addressed by a 3-bit stack pointer.

The first eight locations (0-7) of the array are designated as working registers and are directly addressable by any of the 11 direct register instructions. These locations are readily accessible for a variety of operations with a minimum number of instruction bytes required for their manipulation. Thus, they are usually used to store frequently accessed intermediate results. The DJNZ instruction makes very efficient use of the working registers as program loop counters by allowing the programmer to decrement and test the register in a single instruction.

Registers 0 and 1 have yet another function in that they can be used to indirectly address all locations in the data memory using the indirect register instructions. These two RAM pointer registers are especially useful for repetitive type operations on adjacent memory locations. The indirect register instruction specifies which pointer register to use and the content of the pointer register is used to address a location in RAM. The contents of the addressed location are used during the execution of the instruction and may be modified. The pointer registers may also point to registers 0-7, if desired.

Locations 8-23 serve a dual role in that they contain the 8-level program counter stack, two RAM locations per level. The program counter stack enables the processor to keep track of the return addresses generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the program counter stack's eight register pairs will be loaded with the next return address generated. The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. The first subroutine jump or interrupt results in the program counter contents being transferred to locations 8 and 9. The stack pointer is then incremented by one and points to locations 10 and 11 in anticipation of another CALL. The end of a subroutine, which is signaled by a return instruction (RET or RETI), causes the stack pointer to be decremented and the contents of the resulting register pair to be transferred to the program counter.

Since the program counter's addresses are 11 bits long, two bytes or registers must be used to store a single address. Thus, the 16-byte program counter stack permits up to a total of 8 levels of subroutine nesting without overflowing the stack. If overflow does occur, the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111. If a particular application does not require 8 levels of nesting, tthe unused portion of the program counter stack may be used as any other indirectly addressable RAM location. For example, if only 3 levels of subroutine nesting are used, then only locations 8-13 need be reserved for the program counter stack, and locations 14-23 can be used for data storage.



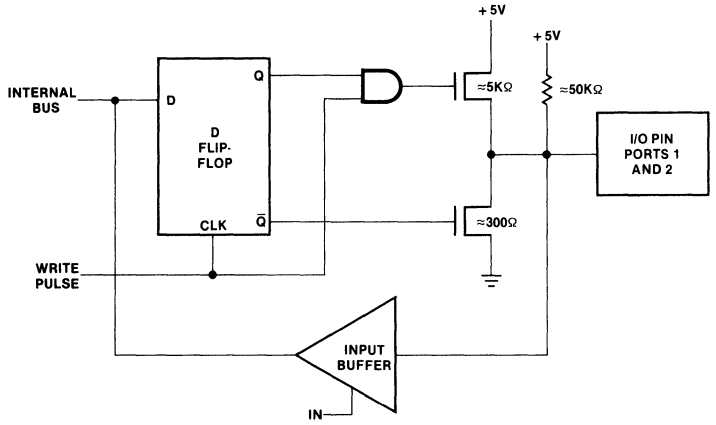
DATA MEMORY MAP

INPUT/OUTPUT

The 8022 has 26 lines which can be used for digital input or output functions. These lines are organized as 3 ports of 8 lines, each of which serve as either inputs, outputs, or bidirectional ports, and 2 test inputs which can alter program sequences when tested by conditional jump instructions.

Ports 1 and 2 have identical operating characteristics and are both quasi-bidirectional. That is, each line may serve as an input, an output, or both. Data written to these ports is statically latched and remains unchanged until rewritten. As inputs, these lines are non-latching; i.e., inputs must be present until read by an input instruction. Inputs are fully TTL compatible and all outputs will drive at least one standard TTL load. Two lines of port 1 (P10 and P11) are designated as high current drive lines and have the ability to sink 7 mA. In addition, these pins may be paralleled for 14 mA output if the output logic states are always the same. The high current output lines eliminate the need for discrete transistors in many applications.

The lines of ports 1 and 2 are quasi-bidirectional because of their output structure which allows them to be used as inputs, outputs, or both, even though as outputs they are statically latched.

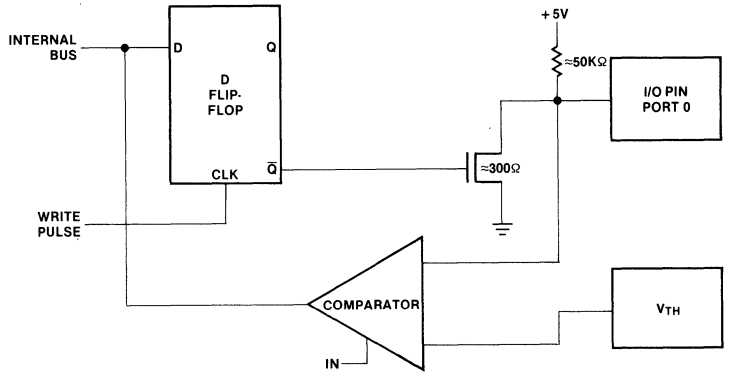


QUASI-BIDIRECTIONAL PORT STRUCTURE

Each line is continuously pulled up to +5V through a relatively high impedance device (~50 kΩ). This pullup is sufficient to provide the source current for a TTL high level, yet can be pulled low by a standard TTL gate, thus allowing the same pin to be used both as an input and output. When writing a "0" or low value to these ports, a low impedance device (~300Ω) overcomes the high pullup and provides TTL current sinking capability. When writing a "1", a large current is momentarily supplied through a relatively low impedance device (~5kΩ) to allow a fast data transfer. After a short time (less than one instruction cycle) the low impedance device is shut off and the small pullup maintains the "1" level indefinitely. In this situation, an input device capable of overriding the small amount of sustaining current supplied by the pullup device can be read. (Alternatively, the data written cn be read.) So, by writing a "1" to any particular pin that pin can serve either as a true high-level latched output pin, or as just a pullup resistor on an input. This allows maximum user flexibility in selecting his input or latched output lines, with a minimum of external components.

PORT 0 COMPARATOR INPUTS

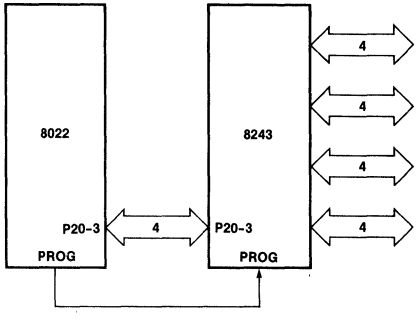
Port 0 has been modified from the standard quasi-bidirectional structure to allow an optional open drain configuration with comparator inputs. The low impedance pullup device has been eliminated and the high impedance pullup is optional. Thus, the user can choose via a mask programmable selection each line of port 0 to be either quasi-bidirectional with a high impedance or true open-drain. The open drain configuration allows the line to sink current through the low impedance pulldown device or to float in the high output state. More importantly, the open drain configuration makes port 0 very easy to drive when it is used as inputs. The input circuitry for each line of port 0 includes a voltage comparator which amplifies the voltage difference between the input port line and the port 0 threshold reference pin (V_{TH}). The voltage gain of the comparator is sufficient to sense a 100 mV input differential within the range V_{SS} to $V_{CC}/2$.



PORT 0 I/O STRUCTURE

If V_{TH} is allowed to float, it will bias itself to the digital switch point of the other ports, and port 0 behaves as a set of normal digital inputs. However, by biasing V_{TH}, the switch point can be both tightly controlled and adjusted. Common uses for this would include high noise margin inputs ($V_{CC}/2$), unusual logic level inputs as from a diode isolated keyboard, analog channel expansion, and direct capacitive touchpanel interface. The comparator action is automatic and the port is read just as any other port.

In addition to the 26 digital I/O lines contained on-board the 8022, a user can obtain additional I/O lines by utilizing the Intel® 8243 I/O expander chip or standard TTL. The 8243 interfaces to 4 port lines of the 8022 (lower half of port 2) and is strobed by the PROG line of the 8022.



I/O EXPANDER INTERFACE

The 8243 contains four 4-bit I/O ports which serve as extensions of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports:

1. Transfer Accumulator to Port
2. Transfer Port to Accumulator
3. And Accumulator to Port
4. Or Accumulator to Port

A 4-bit transfer from a port to the lower half of the accumulator sets the most significant four bits to zero. Each transfer consists of two 4-bit nibbles. The first contains the "opcodes" and port address, and the second contains the actual 4 bits of data. A high-to-low transition of the PROG line indicates that address is present while a low-to-high transition indicates the presence of data.

TEST AND INTERRUPT INPUTS

In addition to the 24 general purpose I/O lines which comprise ports 0, 1, and 2, the 8022 has two inputs which are testable via conditional jump instructions, T0 and T1. These pins allow inputs to cause program branches without the necessity to load an input port into the accumulator. T0 and T1 have other functions as well.

The Test 0 pin serves as an external interrupt input as well as a testable input. An interrupt sequence is initiated by applying a low "0" level input to the T0 pin when external interrupt is enabled. Interrupt is level triggered and active low to allow "WIRE ORING" of several interrupt sources at the input pin. When an interrupt is detected, it causes a "jump to subroutine" at location 3 in program memory as soon as all other cycles of the current instruction are complete. At this time, the program counter contents are saved in the program counter stack, but the remaining status of the processor is not. Unlike the 8048, the 8022 does not contain a program status word. Thus, when appropriate, the carry and auxiliary carry flags are saved in software, as the accumulator is. The routine shown below saves the accumulator and the carry flags in only four bytes.

Instructions	Bytes	Comments
MOV R6,A	1	;save accumulator
CLR A	1	;clear accumulator
DA A	1	;convert carry flags into sixes
MOV R7,A	1	;save status of carry flags

The end of an interrupt service subroutine is marked by the execution of a Return from Interrupt instruction (RETI). Prior to returning from the interrupt subroutine

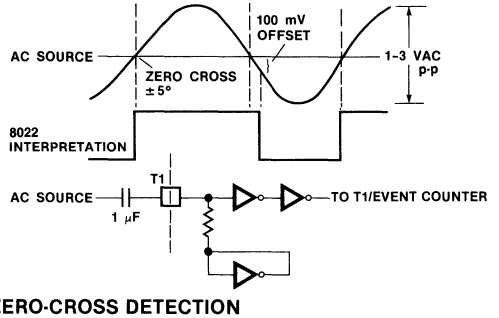
however, the status of the accumulator and the carry flags are restored in software. The following routine restores the status of the accumulator and the carry flags, which was previously saved, in five bytes.

Instructions	Bytes	Comments
MOV A,R7	1	;restore carry flags status to
Add A,#0AAH	2	;accumulator and set/clear carry flags
MOV A,R6	1	;restore accumulator
RETI	1	;return

The interrupt system is single level in that once an interrupt is detected, all further interrupt requests are ignored until execution of a RETI re-enables the interrupt input logic. This sequence holds true also for an internal interrupt generated by timer overflow. If an external interrupt and an internal timer/counter generated interrupt are detected at the same time, the external source will be recognized. If needed, a second external interrupt can be created by enabling the timer/counter interrupt, loading FFH in the counter (one less than terminal count) and enabling the event counter mode. A low-to-high transition on the T1 input will then cause an interrupt vector to location 7.

The Test 1 pin, in addition to being a testable input, serves two other important functions. It can be used as an input pin to the external event counter, as previously mentioned, and it can be used to detect the zero crossing point of slow moving AC signals. Execution of the STRT CNT instruction puts the T1 pin in the counter input mode by connecting T1 to the counter and enabling the counter. Subsequent low-to-high transitions on T1 will cause the counter to increment. Note that this operation differs from the rest of the MCS-48 devices, which increment the counter on high-to-low transitions. This change was made on the 8022 to take advantage of the accuracy of the rising edge detection on the zero cross circuitry. The maximum rate at which the counter may be incremented is once per three instruction cycles (every 30 μs when using a 3 MHz crystal) — there is no minimum frequency.

In addition to serving as a testable input and as the counter input, the T1 pin has special circuitry to detect when an AC signal crosses its average DC level. When driven directly, this pin responds as a normal digital input. To utilize the zero cross detection mode, an AC signal of approximately 1-3 VAC p-p magnitude and a maximum frequency of 1 kHz is coupled through an external capacitor (1 μF) to the T1 pin.



ZERO-CROSS DETECTION

The internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one. This is accomplished by the self-biasing high gain amplifier which is included in the T1 input. This circuit biases the T1 input exactly at its switching point, such that a small change will cause a digital transition to occur. This digital transition takes place within 5 degrees of the zero point. The digital value of T1 remains a one until the falling edge of the AC input drops approximately 100 mV below the switching point of the rising edge (100 mV below the zero point, if the digital transition occurred exactly at the zero point). The 100 mV offset is created by hysteresis and eliminates chattering of the internal signal caused by the external noise.

The zero cross detection capability allows the user to make the 60 Hz power signal the basis for this system timing. All timing routines, including time-of-day, can be implemented using the zero cross detection capability of T1 and its conditional jump instructions. In addition, the zero cross detection feature can be used in conjunction with the timer interrupt to interrupt processing at the zero voltage point. This enables the user to control voltage phase sensitive devices such as triacs and SCRs, and to use the 8022 in applications such as shaft speed and angle measurement.

ANALOG TO DIGITAL CONVERTER

The 8022 contains on-chip a complete hardware implementation of an 8-bit analog to digital (A/D) converter with two multiplexed analog inputs. The A/D converter utilizes a successive approximation technique to provide an updated conversion once every four instruction cycles (i.e., once every 40 μs) with a minimum of required software.

The A/D converter consists of four main parts, the input circuitry, a series string of resistors, a voltage comparator, and the successive approximation logic. The two analog inputs are multiplexed on-chip and selected via software by the SEL AN0 and SEL AN1 instructions. Besides selecting one of the analog inputs, these instructions restart the conversion sequence which operates continuously. Restarting a conversion sequence deletes the conversion in progress but does not effect the result of the previous conversion which is stored in the conversion result register. The continuous operation of the A/D converter saves program space and time by allowing the user obtain multiple readings from a given input with only one select instruction. To obtain a valid conversion reading, the user must provide the analog input signal no later than the beginning of the select instruction cycle. The analog input is then sampled by the A/D converter and maintained internally. This voltage becomes one input to the voltage comparator which amplifies the difference between the analog input and the voltage tap on the series resistor string.

The series resistor string is connected between the A/D reference pin (V_{AREF}) and ground (AV_{SS}). It is comprised of 256 identical resistors which divide the voltage between these two pins into 256 identical voltage steps. This configuration gives the converter its inherent monotonicity. The range of V_{AREF} in which full 8-bit resolution can be provided is between $V_{CC}/2$ and V_{CC}.

Thus, the user is given a minimum voltage range from ground to $V_{CC}/2$ and a maximum range from ground to V_{CC} over which 8-bit resolution is insured.

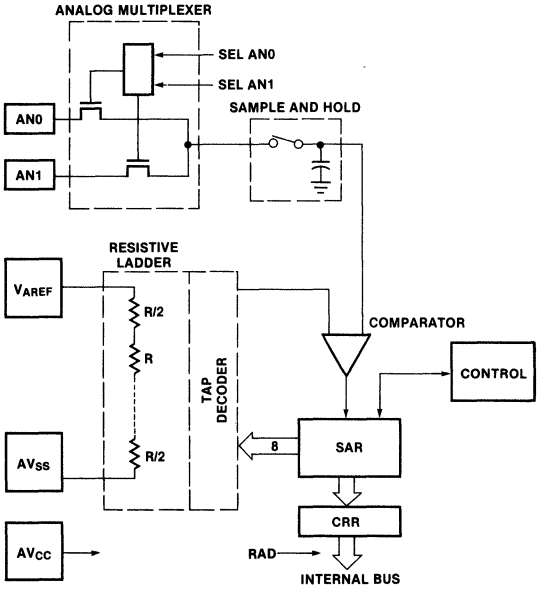
The voltage tap on the series resistor string is selected by the resistor ladder decoder. This decoder is driven by the 8-bit successive approximation register (SAR). Each bit of the SAR is set in succession MSB to LSB and a voltage comparison between the selected resistor ladder voltage and the analog input voltage is performed after the setting of each bit. The result of each comparison determines whether the particular bit will remain set or be reset. All comparisons are performed automatically by the on-chip A/D hardware. At the end of 8 comparisons the SAR contains a valid digital result which is then latched into the conversion result register (CRR). The RAD instruction (read A/D) loads the conversion result from the CRR to the accumulator of the 8022.

As mentioned previously, the software and time required to perform an A/D conversion is optimized by the 8022's on-chip A/D converter configuration. Typical software for reading two sequential A/D conversions and storing them in data memory is shown below:

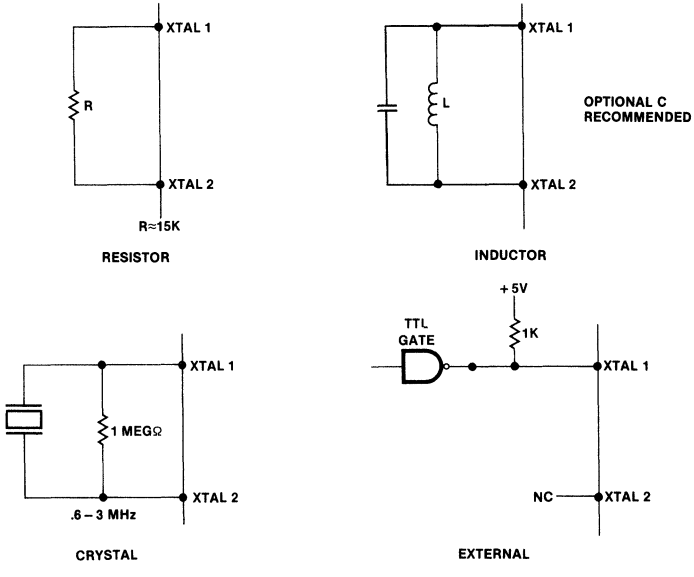
First Conversion	SEL AN0	;Starts conversion of AN0 input
50 μs	MOV R0,#24	;Set up memory pointer
4 bytes	RAD	;First conversion value to accumulator
Second Conversion	MOV @R0,A	;Store first conversion value
	INC R0	;Increment memory location
40 μs	RAD	;Second conversion value to accumulator
3 bytes		

Note that the second conversion occurs without a second select instruction being used. Rather, the continuous operation of the A/D converter provides an updated digital value 4 instruction cycles after the first.

To insure maximum accuracy from the A/D converter, separate power supply pins (AV_{CC} and AV_{SS}) and a substrate pin (SUBST) have been provided. Supplying the power supply pins with a well filtered and regulated voltage supply minimizes the effect of power supply variance and system noise. The substrate pin should be bypassed to ground through a 500 pF to 0.001 μF capacitor.



A/D CONVERTER BLOCK DIAGRAM



FREQUENCY REFERENCE OPTIONS

OSCILLATOR AND CLOCK

The 8022 contains its own on-board oscillator and clock circuit, requiring only an external timing control element. This control element can be a crystal, inductor, resistor, or clock in. The capacitor normally required in resistor or inductor timing control operation is integrated onto the 8022. All internal time slots are derived from the external element, and all outputs are a function of the oscillator frequency. Pins X1 and X2 are used to input the particular control element. An instruction cycle consists of 10 states, and each state is a time slot of 3 oscillator periods. Therefore, to obtain a 10 μs instruction cycle, a 3 MHz crystal should be used.

TIMER/COUNTER

An interval timer/counter is available to enable the user to keep track of time elapsed or number of events occurred during normal program execution and flow.

By a MOV T,A instruction, the contents of the accumulator are loaded to the timer. At the STRT T command an internal prescaler is zeroed and thereafter increments once each 30 input clocks (once each single cycle instruction, twice each double cycle instruction). The prescaler is a divide by 32. At the (11111) to (00000) transition the timer is incremented. The timer is 8 bits and an overflow (FFH) to (00H) timer flag is set along with the timer interrupt, if enabled. A conditional branch instruction (JTF) is available for testing this flag, the flag being reset each test. This instruction must also be used to initialize the timer overflow flag after a RESET instruction, as RESET does not perform this function. Total count capacity for the timer is $2^8 \times 2^5 \doteq 8192$ or 81.9 ms at a 10 μs cycle time. Contents of the timer are moved to the accumulator by the MOV A,T instruction without disturbing the counting process.

The timer may also be used as an event counter. After a STRT CNT command, the 8022 will respond to a low-to-high transition on the Test 1 pin by incrementing the timer. Transitions can occur no faster than once each three instruction cycles.

The timer and event functions are exclusive. Counting or timing may be started or stopped (STOP TCNT) at will.

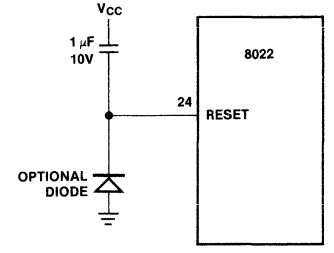
CPU

The 8022 CPU has arithmetic and logical capability. A wide variety of arithmetic and logic instructions may be exercised, which affect the contents of the accumulator, and/or direct or indirect scratchpad locations. Provisions have been made for simplified BCD arithmetic capability through the use of the DAA, SWAP A, and XCHD instructions. In addition, MOVP A,@A allows table lookup for display formatting and constants. Jump conditions such as zero, not zero refer to the accumulator contents at the time of the condition.

RESET

The 8022 may be used in systems with poorly regulated and noisy power supplies. A useful feature is to sense when the power supply dips and quickly recovers, and do a reset to prevent continued operation with incorrect data. This feature may be implemented on the 8022 by connecting a diode between the RESET node and ground.

Including the diode in the reset circuitry forces a reset to occur if the power supply experiences a very sudden voltage glitch. Specifically, if the power supply drops approximately 1.5V and recovers after at least a few nanoseconds, a reset will occur. Without the diode, a power supply interruption of less than 1 ms will not cause a power-on reset.



POWER ON RESET

INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, CA 95051 • (408) 987-8080
Printed in U.S.A./T-244/1078/15K BL

8048/ 8648/ 8748/ 8035

SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8048 Mask Programmable ROM**
- **8648 One-Time Factory Programmable EPROM**
- **8748 User Programmable/Erasable EPROM**
- **8035/8035L External ROM or EPROM**

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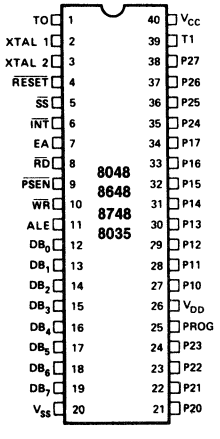
- **1K x 8 ROM/EPROM 64 x 8 RAM 27 I/O Lines**
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Single Level Interrupt**

The Intel® 8048/8648/8748/8035 is a totally self-sufficient, 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

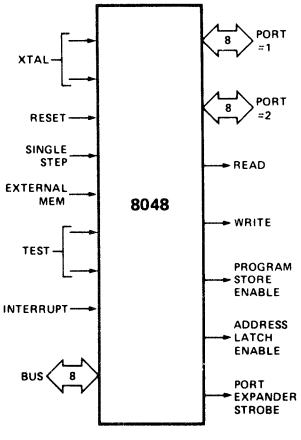
The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8035 is the equivalent of an 8048 without program memory. The 8035L has the RAM power-down mode of the 8048 while the 8035 does not. The 8648 is a one-time programmable (at the factory) 8748 which can be ordered as the first 25 pieces of a new 8048 RAM order. The substitution of 8648's for 8048's allows for very fast turnaround for initial code verification and evaluation units. To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the 8048 with factory-programmed mask ROM program memory for low cost, high volume production, and the 8035 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

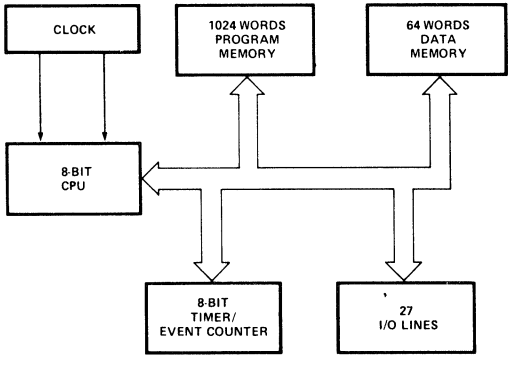
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 and 8035L.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+23V) input pin during 8748 programming.
		Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB_0-DB_7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

Designation	Pin #	Function
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device.
		Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a bus write. (Active low)
		Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle
Accumulator	ADD A, R	Add register to A	1	1
	ADD A, @R	Add data memory to A	1	1
	ADD A, #data	Add immediate to A	2	2
	ADDC A, R	Add register with carry	1	1
	ADDC A, @R	Add data memory with carry	1	1
	ADDC A, #data	Add immediate with carry	2	2
	ANL A, R	And register to A	1	1
	ANL A, @R	And data memory to A	1	1
	ANL A, #data	And immediate to A	2	2
	ORL A, R	Or register to A	1	1
	ORL A, @R	Or data memory to A	1	1
	ORL A, #data	Or immediate to A	2	2
	XRL A, R	Exclusive or register to A	1	1
	XRL A, @R	Exclusive or data memory to A	1	1
	XRL A, #data	Exclusive or immediate to A	2	2
	INC A	Increment A	1	1
	DEC A	Decrement A	1	1
	CLR A	Clear A	1	1
	CPL A	Complement A	1	1
	DA A	Decimal adjust A	1	1
	SWAP A	Swap nibbles of A	1	1
	RL A	Rotate A left	1	1
	RLC A	Rotate A left through carry	1	1
	RR A	Rotate A right	1	1
	RRC A	Rotate A right through carry	1	1
Input/Output	IN A, P	Input port to A	1	2
	OUTL P, A	Output A to port	1	2
	ANL P, #data	And immediate to port	2	2
	ORL P, #data	Or immediate to port	2	2
	INS A, BUS	Input BUS to A	1	2
	OUTL BUS, A	Output A to BUS	1	2
	ANL BUS, #data	And immediate to BUS	2	2
	ORL BUS, #data	Or immediate to BUS	2	2
	MOVD A, P	Input expander port to A	1	2
	MOVD P, A	Output A to expander port	1	2
	ANLD P, A	And A to expander port	1	2
	ORLD P, A	Or A to expander port	1	2
Registers	INC R	Increment register	1	1
	INC @R	Increment data memory	1	1
	DEC R	Decrement register	1	1
Branch	JMP addr	Jump unconditional	2	2
	JMPP @A	Jump indirect	1	2
	DJNZ R, addr	Decrement register and skip	2	2
	JC addr	Jump on carry = 1	2	2
	JNC addr	Jump on carry = 0	2	2
	J Z addr	Jump on A zero	2	2
	JNZ addr	Jump on A not zero	2	2
	JT0 addr	Jump on T0 = 1	2	2
	JNT0 addr	Jump on T0 = 0	2	2
	JT1 addr	Jump on T1 = 1	2	2
	JNT1 addr	Jump on T1 = 0	2	2
	JF0 addr	Jump on F0 = 1	2	2
	JF1 addr	Jump on F1 = 1	2	2
	JTF addr	Jump on timer flag	2	2
	JNI addr	Jump on $\overline{INT}$ = 0	2	2
	JBb addr	Jump on accumulator bit	2	2

	Mnemonic	Description	Bytes	Cycles
Subroutine	CALL addr	Jump to subroutine	2	2
	RET	Return	1	2
	RETR	Return and restore status	1	2
Flags	CLR C	Clear carry	1	1
	CPL C	Complement carry	1	1
	CLR F0	Clear flag 0	1	1
	CPL F0	Complement flag 0	1	1
	CLR F1	Clear flag 1	1	1
	CPL F1	Complement flag 1	1	1
Data Moves	MOV A, R	Move register to A	1	1
	MOV A, @R	Move data memory to A	1	1
	MOV A, #data	Move immediate to A	2	2
	MOV R, A	Move A to register	1	1
	MOV @R, A	Move A to data memory	1	1
	MOV R, #data	Move immediate to register	2	2
	MOV @R, #data	Move immediate to data memory	2	2
	MOV A, PSW	Move PSW to A	1	1
	MOV PSW, A	Move A to PSW	1	1
	XCH A, R	Exchange A and register	1	1
	XCHA, @R	Exchange A and data memory	1	1
	XCHD A, @R	Exchange nibble of A and register	1	1
	MOVX A, @R	Move external data memory to A	1	2
	MOVX @R, A	Move A to external data memory	1	2
	MOVP A, @A	Move to A from current page	1	2
	MOVP3 A, @A	Move to A from page 3	1	2
Timer/Counter	MOV A, T	Read timer/counter	1	1
	MOV T, A	Load timer/counter	1	1
	STRT T	Start timer	1	1
	STRT CNT	Start counter	1	1
	STOP TCNT	Stop timer/counter	1	1
	EN TCNTI	Enable timer/counter interrupt	1	1
	DIS TCNTI	Disable timer/counter interrupt	1	1
Control	EN I	Enable external interrupt	1	1
	DIS I	Disable external interrupt	1	1
	SEL RB0	Select register bank 0	1	1
	SEL RB1	Select register bank 1	1	1
	SEL MB0	Select memory bank 0	1	1
	SEL MB1	Select memory bank 1	1	1
	ENT0 CLK	Enable clock output on T0	1	1
	NOP	No operation	1	1

ABSOLUTE MAXIMUM RATINGS*

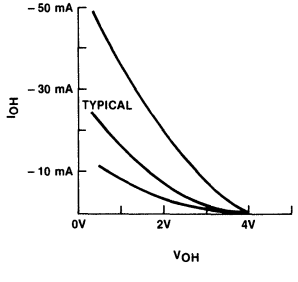
Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage On Any Pin With Respect to Ground ..... -0.5V to +7V
Power Dissipation ..... 1.5 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

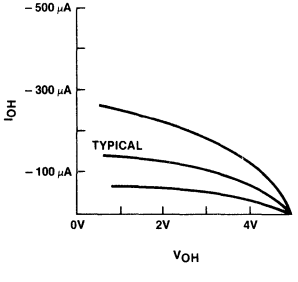
D.C. AND OPERATING CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except $\overline{RESET}$, X1, X2)	−.5		.8	V	
V_{IL1}	Input Low Voltage ($\overline{RESET}$, X1, X2)	−.5		.6	V	
V_{IH}	Input High Voltage (All Except XTAL1, XTAL 2, $\overline{RESET}$)	2.0		V_{CC}	V	
V_{IH1}	Input High Voltage (X1, X2, $\overline{RESET}$)	3.8		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS)			.45	V	$V_{OL} = 2.0$ mA
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			.45	V	$I_{OL} = 1.8$ mA
V_{OL2}	Output Low Voltage (PROG)			.45	V	$I_{OL} = 1.0$ mA
V_{OL3}	Output Low Voltage (All Other Outputs)			.45	V	$I_{OL} = 1.6$ mA
V_{OH}	Output High Voltage (BUS)	2.4			V	$I_{OH} = -400\ \mu A$
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	$I_{OH} = -100\ \mu A$
V_{OH2}	Output High Voltage (All Other Outputs)	2.4			V	$I_{OH} = -40\ \mu A$
I_{LI}	Input Leakage Current (T1, $\overline{INT}$)			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LI1}	Input Leakage Current (P10-P17, P20-P27, EA, $\overline{SS}$)			−500	μA	$V_{SS} + .45 \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current (BUS, TO) (High Impedance State)			±10	μA	$V_{SS} + .45 \leq V_{IN} \leq V_{CC}$
I_{DD}	V_{DD} Supply Current		5	15	mA	
$I_{DD} + I_{CC}$	Total Supply Current		60	135	mA	

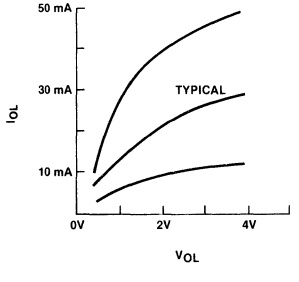
BUS



P1, P2

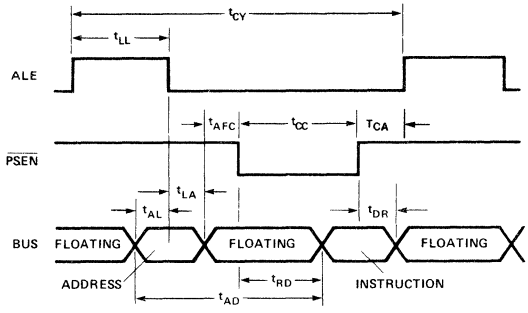


BUS, P1, P2

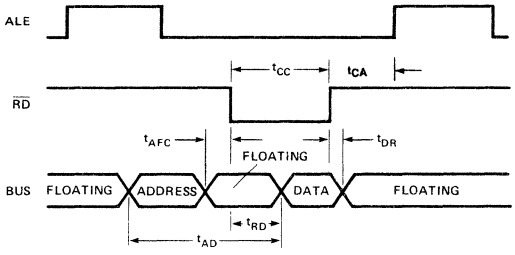


WAVEFORMS

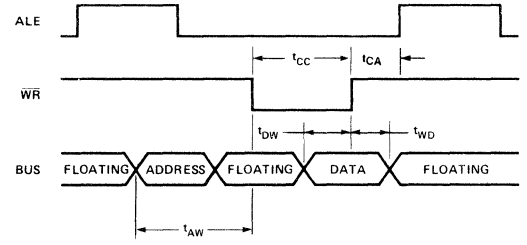
Instruction Fetch From External Program Memory



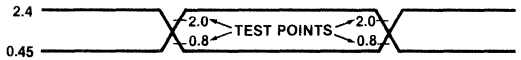
Read From External Data Memory



Write to External Data Memory



Input and Output Waveforms for A.C. Tests



MCS-48

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	8048 8648 8748/8035/8035L		8748-8* 8035-8		Unit	Conditions (Note 1)
		Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	400		600		ns	
t_{AL}	Address Setup to ALE	120		150		ns	
t_{LA}	Address Hold from ALE	80		80		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	700		1500		ns	
t_{DW}	Data Setup before $\overline{WR}$	500		640		ns	
t_{WD}	Data Hold After $\overline{WR}$	120		120		ns	C_L = 20pF
t_{CY}	Cycle Time	2.5	15.0	4.17	15.0	μs	6 MHz XTAL = 2.5 (3.6 MHz XTAL for −8)
t_{DR}	Data Hold	0	200	0	200	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500		750	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		260		ns	
t_{AD}	Address Setup to Data In		950		1450	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0		0		ns	
t_{CA}	Control Pulse to ALE	10		20		ns	

Note 1: Control outputs: $C_L = 80$ pF $t_{CY} = 2.5\ \mu s$ for standard parts
BUS Outputs: $C_L = 150$ pF $= 4.17\ \mu s$ for -8 parts

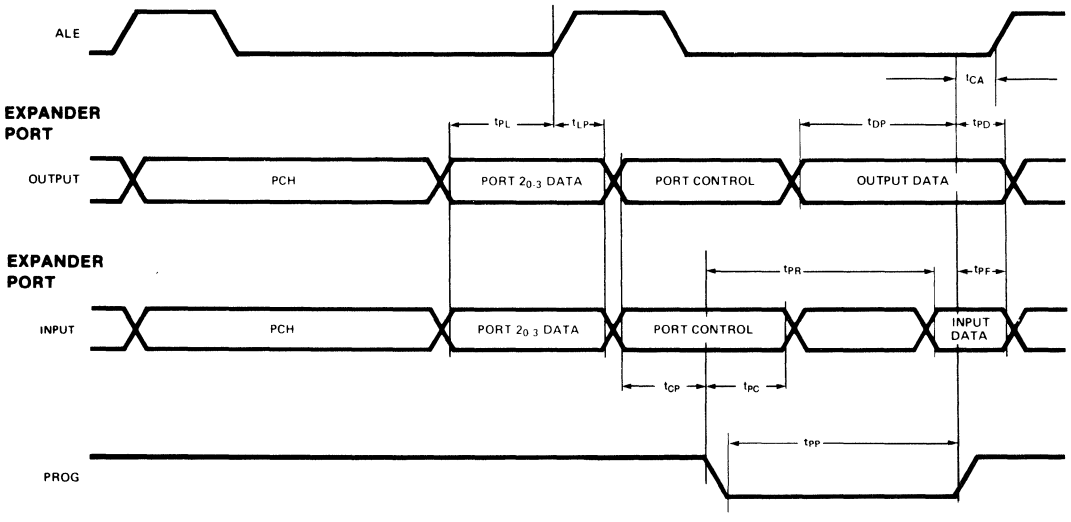
*V_{CC} and V_{DD} for 8748-8 and 8035-8 are $\pm 5\%$.

A.C. CHARACTERISTICS (PORT 2 TIMING)

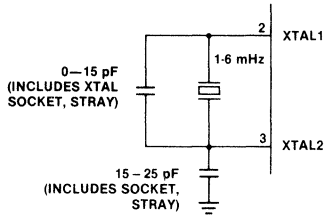
$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CP}	Port Control Setup Before Falling Edge of PROG	110		ns	
t_{PC}	Port Control Hold After Falling Edge of PROG	100		ns	
t_{PR}	PROG to Time P2 Input Must Be Valid		810	ns	
t_{PF}	Input Data Hold Time	0	150	ns	
t_{DP}	Output Data Setup Time	250		ns	
t_{PD}	Output Data Hold Time	65		ns	
t_{PP}	PROG Pulse Width	1200		ns	
t_{PL}	Port 2 I/O Data Setup	350		ns	
t_{LP}	Port 2 I/O Data Hold	150		ns	

PORT 2 TIMING

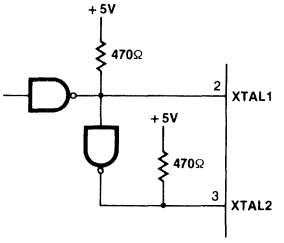


CRYSTAL OSCILLATOR MODE



CRYSTAL SERIES RESISTANCE SHOULD BE <75Ω AT 6 MHz; <180Ω AT 3.6 MHz.

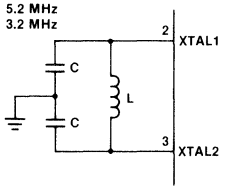
DRIVING FROM EXTERNAL SOURCE



BOTH X1 AND X2 SHOULD BE DRIVEN.
RESISTORS TO V_{CC} ARE NEEDED TO ENSURE $V_{IH} = 3.8V$ IF TTL CIRCUITRY IS USED. THE MINIMUM HIGH AND THE MINIMUM LOW TIMES ARE 45%.

LC OSCILLATOR MODE

L	C	NOMINAL f
45 μH	20 pF	5.2 MHz
120 μH	20 pF	3.2 MHz



$$f \approx \frac{1}{2\pi\sqrt{LC'}}$$

$$C' = \frac{C + 3C_{PP}}{2}$$

$C_{PP} \approx 5 – 10$ pF PIN-TO-PIN CAPACITANCE

EACH C SHOULD BE APPROXIMATELY 20 pF, INCLUDING STRAY CAPACITANCE.

MCS-48

PROGRAMMING, VERIFYING, AND ERASING THE 8748 EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock Input (1 to 6MHz)
$\overline{\text{Reset}}$	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input Data Output During Verify
P20-1	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING:

An attempt to program a missocketed 8748 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. V_{DD} = 5v, Clock applied or internal oscillator operating, $\overline{\text{RESET}}$ = 0v, TEST 0 = 5v, EA = 5v, BUS and PROG floating.
2. Insert 8748 in programming socket
3. TEST 0 = 0v (select program mode)
4. EA = 23V (activate program mode)
5. Address applied to BUS and P20-1
6. $\overline{\text{RESET}}$ = 5v (latch address)
7. Data applied to BUS
8. V_{DD} = 25v (programming power)
9. PROG = 0v followed by one 50ms pulse to 23V
10. V_{DD} = 5v
11. TEST 0 = 5v (verify mode)
12. Read and verify data on BUS
13. TEST 0 = 0v
14. $\overline{\text{RESET}}$ = 0v and repeat from step 5
15. Programmer should be at conditions of step 1 when 8748 is removed from socket.

AC TIMING SPECIFICATION FOR PROGRAMMING

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 25V \pm 1V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Setup Time to $\overline{RESET}$ ↑	4tcy			
t_{WA}	Address Hold Time After $\overline{RESET}$ ↑	4tcy			
t_{DW}	Data in Setup Time to PROG ↑	4tcy			
t_{WD}	Data in Hold Time After PROG ↓	4tcy			
t_{PH}	$\overline{RESET}$ Hold Time to Verify	4tcy			
t_{VDDW}	V_{DD}	4tcy			
t_{VDDH}	V_{DD} Hold Time After PROG ↓	0			
t_{PW}	Program Pulse Width	50	60	mS	
t_{TW}	Test 0 Setup Time for Program Mode	4tcy			
t_{WT}	Test 0 Hold Time After Program Mode	4tcy			
t_{DO}	Test 0 to Data Out Delay		4tcy		
t_{WW}	$\overline{RESET}$ Pulse Width to Latch Address	4tcy			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	5.0		μs	
t_{RE}	$\overline{RESET}$ Setup Time Before EA ↑,	4tcy			

Note: If Test 0 is high t_{DO} can be triggered by $\overline{RESET}$ ↑.

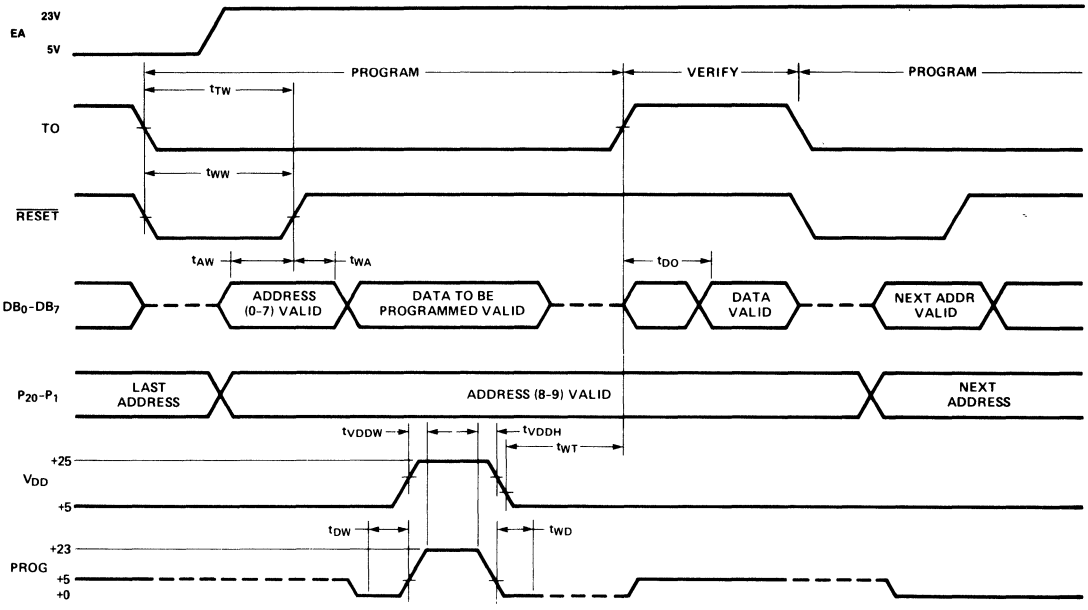
DC SPECIFICATION FOR PROGRAMMING

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 25V \pm 1V$

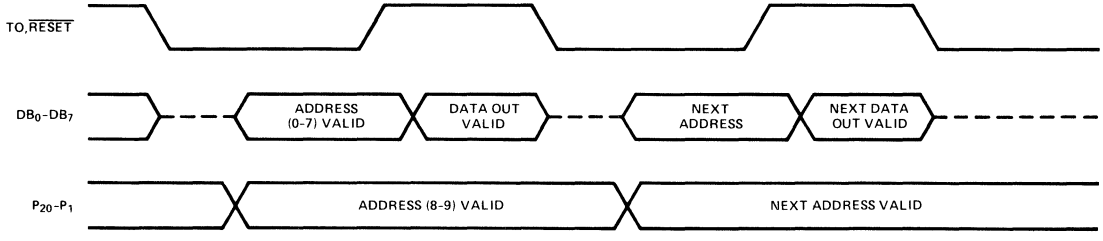
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DOH}	V_{DD} Program Voltage High Level	24.0	26.0	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	21.5	24.5	V	
V_{PL}	PROG Voltage Low Level		0.2	V	
V_{EAH}	EA Program or Verify Voltage High Level	21.5	24.5	V	8748
V_{EAH1}	EA1 Verify Voltage High Level	11.4	12.6	V	8048
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		16.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

WAVEFORMS FOR PROGRAMMING

COMBINATION PROGRAM/VERIFY MODE (EPROM'S ONLY)



VERIFY MODE (ROM/EPROM)



NOTES:
1. PROG MUST FLOAT IF EA IS LOW (i.e., ≠23V), OR IF T0 = 5V FOR THE 8748. FOR THE 8048 PROG MUST ALWAYS FLOAT.
2. X_1 AND X_2 DRIVEN BY 3 MHz CLOCK WILL GIVE 5μsec t_{CY}. THIS IS ACCEPTABLE FOR -8 PARTS AS WELL AS STANDARD PARTS.

The 8748 EPROM can be programmed by either of two Intel products:

1. PROMPT-48 Microcomputer Design Aid, or
2. Universal PROM Programmer (UPP series) peripheral of the Intellec® Development System with a UPP-848 Personality Card.

Note: See the ROM/PROM section for 8048 ROM ordering procedures. To minimize turnaround time on the first 25 pieces 8648 may be specified on the ROM order.

NEW HIGH PERFORMANCE 8049/8039/8039-6 SINGLE COMPONENT 8-BIT MICROCOMPUTER

*8049 Mask Programmable ROM
*8039 External ROM or EPROM
*New 11 MHz Operation

- **8-Bit CPU, ROM, RAM, I/O in Single Package**
- **Single 5V ± 10% Supply**
- **1.36 μsec Cycle; All Instructions 1 or 2 Cycles**
- **Over 90 Instructions: 70% Single Byte**
- **Pin Compatible with 8048/8748**
- **2K x 8 ROM**
  128 x 8 RAM
  27 I/O Lines
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with MCS Memory and I/O**
- **Single Level Interrupt**

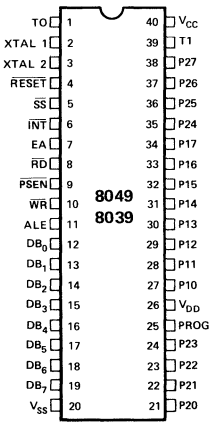
The Intel® 8049/8039/8039-6 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8049 contains a 2K x 8 program memory, a 128 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8049 can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8039 is the equivalent to an 8049 without program memory. The 8039-6 is a lower speed (6MHz) version of the 8039.

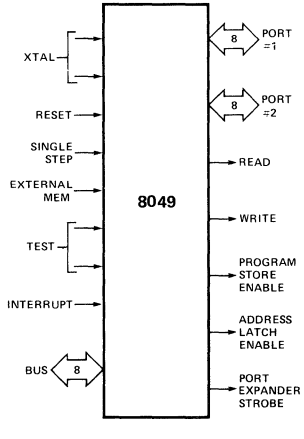
To reduce development problems to a minimum and provide maximum flexibility, two interchangeable pin-compatible versions of this single component microcomputer exist: the 8049 with factory-programmed mask ROM program memory for low-cost high volume production, and the 8039 without program memory for use with external program memories in prototype and preproduction systems.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8049 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

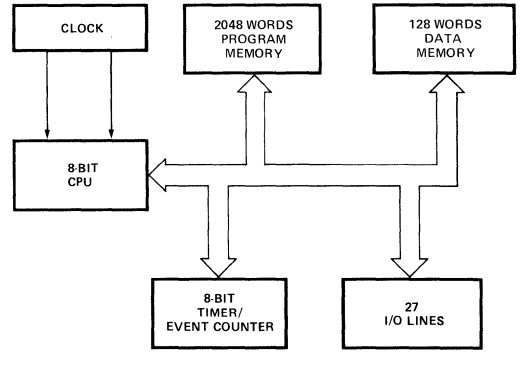
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	+5V during operation. Low power standby pin.
V_{CC}	40	Main power supply; +5V during operation.
PROG	25	Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243
D0-D7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device. Used as a Read Strobe to External Data Memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during verification, and power down. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a BUS write. (Active low) Used as write strobe to External Data Memory.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle
Accumulator	ADD A, R	Add register to A	1	1
	ADD A, @R	Add data memory to A	1	1
	ADD A, #data	Add immediate to A	2	2
	ADDC A, R	Add register with carry	1	1
	ADDC A, @R	Add data memory with carry	1	1
	ADDC A, #data	Add immediate with carry	2	2
	ANL A, R	And register to A	1	1
	ANL A, @R	And data memory to A	1	1
	ANL A, #data	And immediate to A	2	2
	ORL A, R	Or register to A	1	1
	ORL A, @R	Or data memory to A	1	1
	ORL A, #data	Or immediate to A	2	2
	XRL A, R	Exclusive Or register to A	1	1
	XRL A, @R	Exclusive or data memory to A	1	1
	XRL A, #data	Exclusive or immediate to A	2	2
	INC A	Increment A	1	1
	DEC A	Decrement A	1	1
	CLR A	Clear A	1	1
	CPL A	Complement A	1	1
	DA A	Decimal Adjust A	1	1
	SWAP A	Swap nibbles of A	1	1
	RL A	Rotate A left	1	1
	RLC A	Rotate A left through carry	1	1
	RR A	Rotate A right	1	1
	RRC A	Rotate A right through carry	1	1
Input/Output	IN A, P	Input port to A	1	2
	OUTL P, A	Output A to port	1	2
	ANL P, #data	And immediate to port	2	2
	ORL P, #data	Or immediate to port	2	2
	INS A, BUS	Input BUS to A	1	2
	OUTL BUS, A	Output A to BUS	1	2
	ANL BUS, #data	And immediate to BUS	2	2
	ORL BUS, #data	Or immediate to BUS	2	2
	MOVD A, P	Input Expander port to A	1	2
	MOVD P, A	Output A to Expander port	1	2
	ANLD P, A	And A to Expander port	1	2
	ORLD P, A	Or A to Expander port	1	2
Registers	INC R	Increment register	1	1
	INC @R	Increment data memory	1	1
	DEC R	Decrement register	1	1
Branch	JMP addr	Jump unconditional	2	2
	JMPP @A	Jump indirect	1	2
	DJNZ R, addr	Decrement register and skip	2	2
	JC addr	Jump on Carry = 1	2	2
	JNC addr	Jump on Carry = 0	2	2
	J Z addr	Jump on A Zero	2	2
	JNZ addr	Jump on A not Zero	2	2
	JT0 addr	Jump on T0 = 1	2	2
	JNT0 addr	Jump on T0 = 0	2	2
	JT1 addr	Jump on T1 = 1	2	2
	JNT1 addr	Jump on T1 = 0	2	2
	JF0 addr	Jump on F0 = 1	2	2
	JF1 addr	Jump on F1 = 1	2	2
	JTF addr	Jump on timer flag	2	2
	JNI addr	Jump on $\overline{INT}$ = 0	2	2
	JBb addr	Jump on Accumulator Bit	2	2

	Mnemonic	Description	Bytes	Cycles
Subroutine	CALL	Jump to subroutine	2	2
	RET	Return	1	2
	RETR	Return and restore status	1	2
Flags	CLR C	Clear Carry	1	1
	CPL C	Complement Carry	1	1
	CLR F0	Clear Flag 0	1	1
	CPL F0	Complement Flag 0	1	1
	CLR F1	Clear Flag 1	1	1
	CPL F1	Complement Flag 1	1	1
Data Moves	MOV A, R	Move register to A	1	1
	MOV A, @R	Move data memory to A	1	1
	MOV A, #data	Move immediate to A	2	2
	MOV R, A	Move A to register	1	1
	MOV @R, A	Move A to data memory	1	1
	MOV R, #data	Move immediate to register	2	2
	MOV @R, #data	Move immediate to data memory	2	2
	Move A, PSW	Move PSW to A	1	1
	MOV PSW, A	Move A to PSW	1	1
	XCH A, R	Exchange A and register	1	1
	XCH A,@R	Exchange A and data memory	1	1
	XCHD A, @R	Exchange nibble of A and register	1	1
	MOVX A, @R	Move external data memory to A	1	2
	MOVX @R, A	Move A to external data memory	1	2
	MOVP A, @A	Move to A from current page	1	2
	MOVP3 A, @A	Move to A from Page 3	1	2
Timer/Counter	MOV A, T	Read Timer/Counter	1	1
	MOV T, A	Load Timer/Counter	1	1
	STRT T	Start Timer	1	1
	STRT CNT	Start Counter	1	1
	STOP TCNT	Stop Timer/Counter	1	1
	EN TCNTI	Enable Timer/Counter Interrupt	1	1
	DIS TCNTI	Disable Timer/Counter Interrupt	1	1
Control	EN I	Enable external interrupt	1	1
	DIS I	Disable external interrupt	1	1
	SEL RB0	Select register bank 0	1	1
	SEL RB1	Select register bank 1	1	1
	SEL MB0	Select memory bank 0	1	1
	SEL MB1	Select memory bank 1	1	1
	ENT0 CLK	Enable Clock output on T0	1	1
	NOP	No Operation	1	1

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With
Respect to Ground .....-0.5V to +7V
Power Dissipation ..... 1.5 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	2.0		V_{CC}	V	
V_{IH1}	Input High Voltage ($\overline{RESET}$, X1, X2)	3.8		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			0.45	V	$I_{OL} = 2.0mA$
V_{OL1}	Output Low Voltage (All Other Outputs Except PROG)			0.45	V	$I_{OL} = 1.6mA$
V_{OL2}	Output Low Voltage (PROG)			0.45	V	$I_{OL} = 1.0mA$
V_{OH}	Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	$I_{OH} = -100\mu A$
V_{OH1}	Output High Voltage (All Other Outputs)	2.4			V	$I_{OH} = -50\mu A$
I_{IL}	Input Leakage Current (T1, $\overline{INT}$)			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{OL}	Output Leakage Current (Bus, T0) (High Impedance State)			±10	μA	$V_{SS} + 0.45 \leqslant V_{IN} \leqslant V_{CC}$
I_{DD}	Power Down Supply Current		25	50	mA	$T_A = 25°C$
$I_{DD}+I_{CC}$	Total Supply Current		100	170	mA	$T_A = 25°C$

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

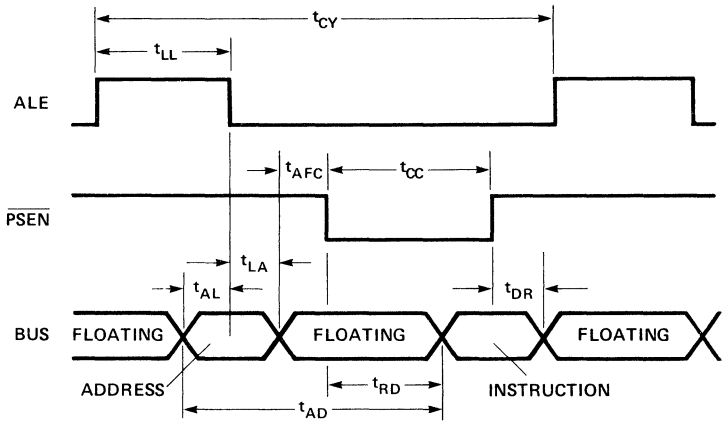
Symbol	Parameter	8049/8039 (Note 1) Min.	Max.	8039-6 Min.	Max.	Unit	Conditions (Note 2)
t_{LL}	ALE Pulse Width	150		400		ns	
t_{AL}	Address Setup to ALE	70		150		ns	
t_{LA}	Address Hold from ALE	50		80		ns	
t_{CC}	Control Pulse Width (PSEN, RD, WR)	300		700		ns	
t_{DW}	Data Set-Up Before WR	250		500		ns	
t_{WD}	Data Hold After WR	40		120		ns	$C_L = 20pF$
t_{CY}	Cycle Time	1.36	15.0	2.5	15.0	μs	11MHz XTAL (6MHz XTAL for -6)
t_{DR}	Data Hold	0	100	0	200	ns	
t_{RD}	PSEN, RD to Data In		200		500	ns	
t_{AW}	Address Setup to WR	200		230		ns	
t_{AD}	Address Setup to Data In		400		950	ns	
t_{AFC}	Address Float to RD, PSEN	-10		0		ns	

Notes: 1. 8039-6 specifications are also valid for 8049/8039 operating at 6MHz.

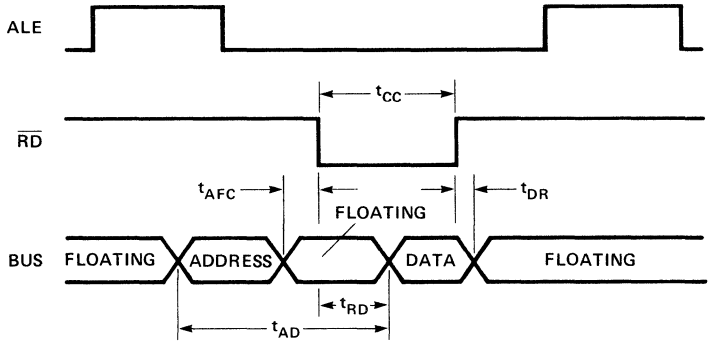
2. Control Outputs: $C_L = 80pF$
   BUS Outputs: $C_L = 150pF$

WAVEFORMS

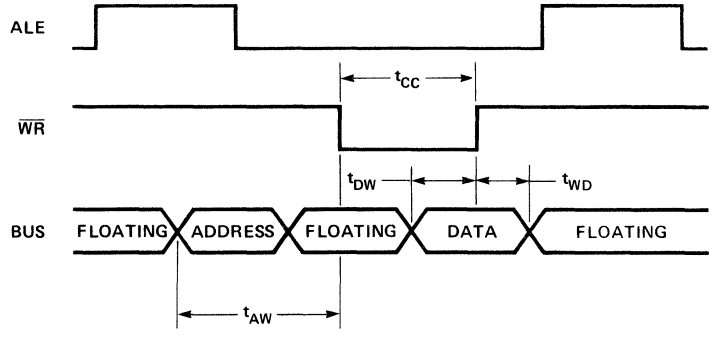
INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL DATA MEMORY



8243
MCS-48™ INPUT/OUTPUT EXPANDER

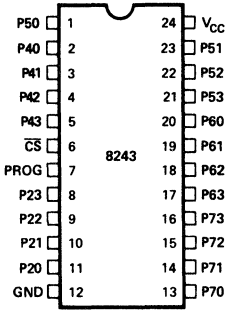
- **Low Cost**
- **Simple Interface to MCS-48™ Microcomputers**
- **Four 4-Bit I/O Ports**
- **AND and OR Directly to Ports**
- **24-Pin DIP**
- **Single 5V Supply**
- **High Output Drive**
- **Direct Extension of Resident 8048 I/O Ports**

The Intel® 8243 is an input/output expander designed specifically to provide a low cost means of I/O expansion for the MCS-48™ family of single chip microcomputers. Fabricated in 5 volts NMOS, the 8243 combines low cost, single supply voltage and high drive current capability.

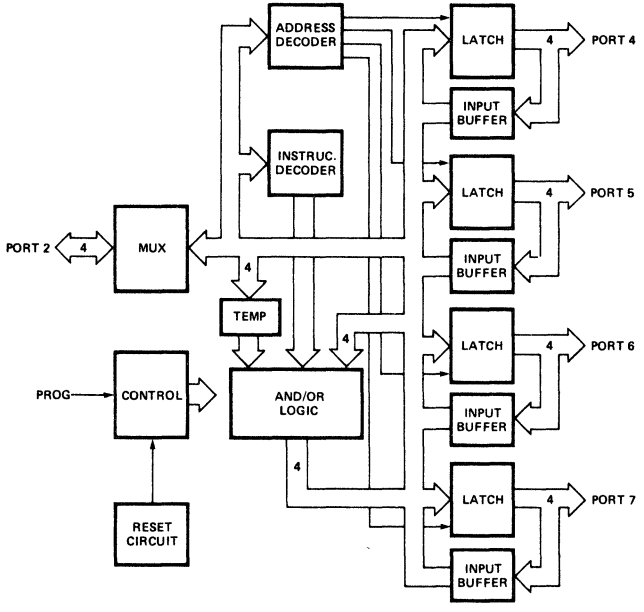
The 8243 consists of four 4-bit bidirectional static I/O ports and one 4-bit port which serves as an interface to the MCS-48 microcomputers. The 4-bit interface requires that only 4 I/O lines of the 8048 be used for I/O expansion, and also allows multiple 8243's to be added to the same bus.

The I/O ports of the 8243 serve as a direct extension of the resident I/O facilities of the MCS-48 microcomputers and are accessed by their own MOV, ANL, and ORL instructions.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Pin No.	Function
PROG	7	Clock Input. A high to low transistion on PROG signifies that address and control are available on P20-P23, and a low to high transition signifies that data is available on P20-23.
$\overline{CS}$	6	Chip Select Input. A high on CS inhibits any change of output or internal status.
P20-P23	11-8	Four (4) bit bi-directional port contains the address and control bits on a high to low transition of PROG. During a low to high transition contains the data for a selected output port if a write operation, or the data from a selected port before the low to high transition if a read operation.
GND	12	0 volt supply.
P40-P43 P50-P53 P60-P63 P70-P73	2-5 1,23-21 20-17 13-16	Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write) or a tri-state (after read). Data on pins P20-23 may be directly written, ANDed or ORed with previous data.
V_{CC}	24	+5 volt supply.

FUNCTIONAL DESCRIPTION

General Operation

The 8243 contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports:

- Transfer Accumulator to Port.
- Transfer Port to Accumulator.
- AND Accumulator to Port.
- OR Accumulator to Port.

All communication between the 8048 and the 8243 occurs over Port 2 (P20-P23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles:

The first containing the "op code" and port address and the second containing the actual 4-bits of data.

A high to low transition of the PROG line indicates that address is present while a low to high transition indicates the presence of data. Additional 8243's may be added to the 4-bit bus and chip selected using additional output lines from the 8048/8748/8035.

Power On Initialization

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

Write Modes

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi,A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi,A takes new data AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

Read Mode

The device has one read mode. The operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are tri-stated, and the input buffers switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the tri-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the 8243 output. A read of any port will leave that port in a high impedance state.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+0.5	V	
V_{OL1}	Output Low Voltage Ports 4-7			0.45	V	I_{OL} = 5 mA*
V_{OL2}	Output Low Voltage Port 7			1	V	I_{OL} = 20 mA
V_{OH1}	Output High Voltage Ports 4-7	2.4			V	I_{OH}= 240μA
I_{IL1}	Input Leakage Ports 4-7	-10		20	μA	V_{in} = V_{CC} to 0V
I_{IL2}	Input Leakage Port 2, CS, PROG	-10		10	μA	V_{in} = V_{CC} to 0V
V_{OL3}	Output Low Voltage Port 2			.45	V	I_{OL}= 0.6 mA
I_{CC}	V_{CC} Supply Current		10	20	mA	
V_{OH2}	Output Voltage Port 2	2.4				I_{OH}= 100μA
I_{OL}	Sum of all IO_L from 16 Outputs			80	mA	5 mA Each Pin

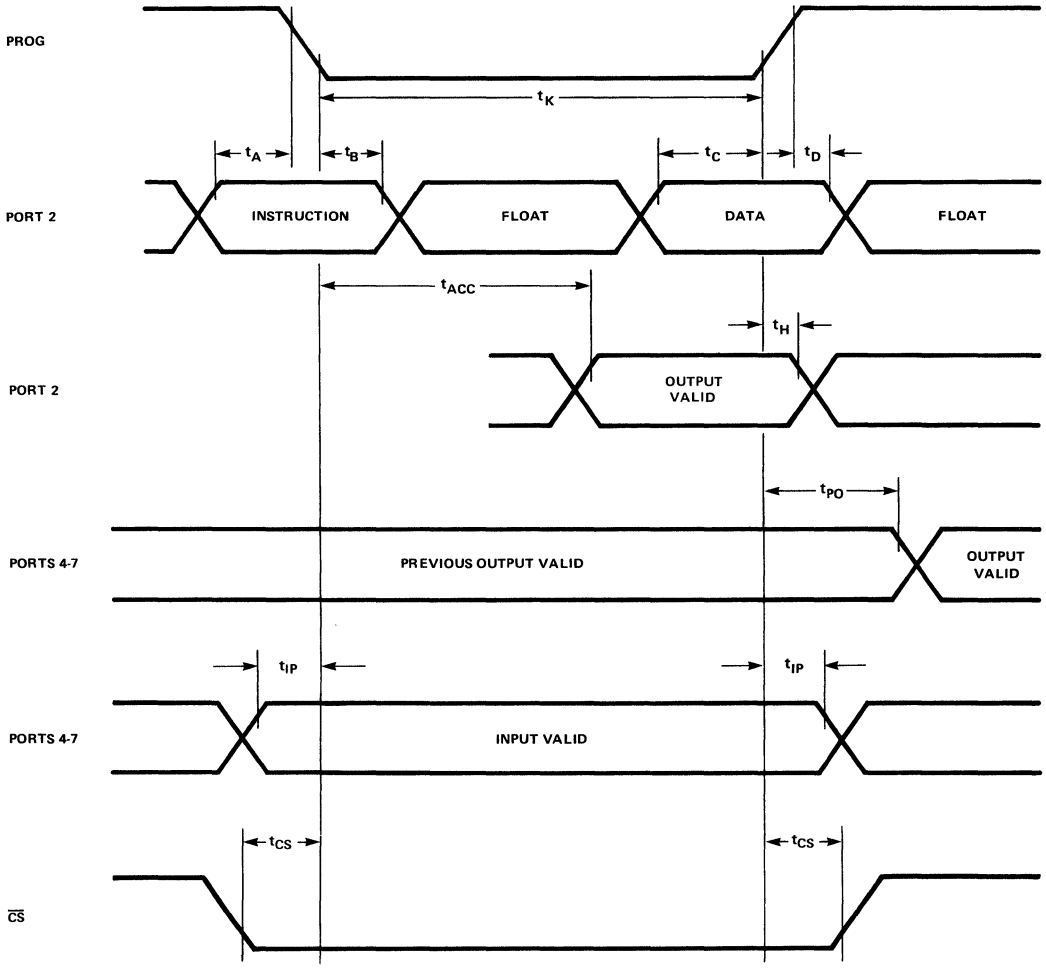
*See following graph for additional sink current capability

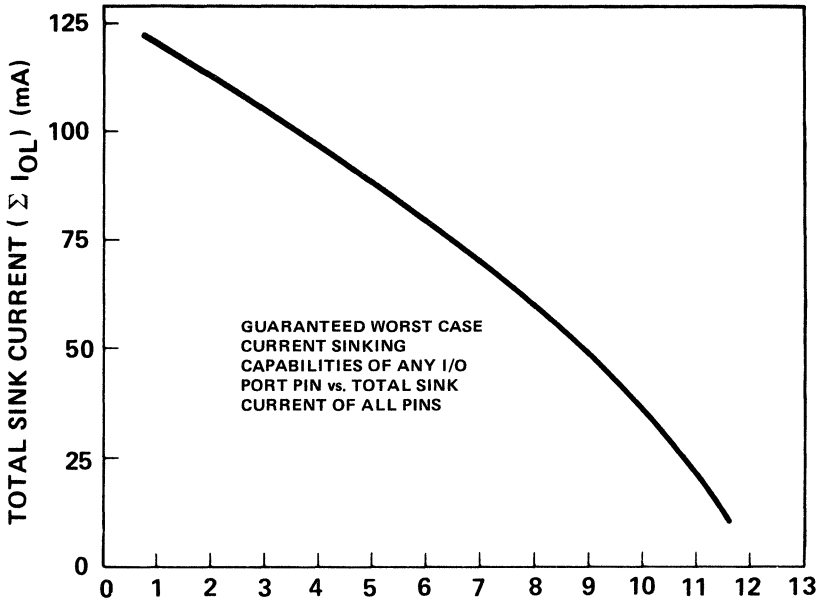
A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_A	Code Valid Before PROG	100		ns	80 pF Load
t_B	Code Valid After PROG	60		ns	20 pF Load
t_C	Data Valid Before PROG	200		ns	80 pF Load
t_D	Data Valid After PROG	20		ns	20 pF Load
t_H	Floating After PROG	0	150	ns	20 pF Load
t_K	PROG Negative Pulse Width	700		ns	
t_{CS}	CS Valid Before/After PROG	50		ns	
t_{PO}	Ports 4-7 Valid After PROG		700	ns	100 pF Load
t_{LP1}	Ports 4-7 Valid Before/After PROG	100		ns	
t_{ACC}	Port 2 Valid After PROG		650	ns	80 pF Load

WAVEFORMS


PROG
t_K
t_A
t_B
t_C
t_D
PORT 2
INSTRUCTION
FLOAT
DATA
FLOAT
t_{ACC}
t_H
PORT 2
OUTPUT VALID
t_{PO}
PORTS 4-7
PREVIOUS OUTPUT VALID
OUTPUT VALID
t_{IP}
t_{IP}
PORTS 4-7
INPUT VALID
t_{CS}
t_{CS}
$\overline{CS}$



Sink Capability

The 8243 can sink 5 mA@.45V on each of its 16 I/O lines simultaneously. If, however, all lines are not sinking simultaneously or all lines are not fully loaded, the drive capability of any individual line increases as is shown by the accompanying curve.

For example, if only 5 of the 16 lines are to sink current at one time, the curve shows that each of those 5 lines is capable of sinking 9 mA@.45V (if any lines are to sink 9 mA the total I_{OL} must not exceed 45 mA or five 9 mA loads).

Example: How many pins can drive 5 TTL loads (1.6 mA) assuming remaining pins are unloaded?

$I_{OL} = 5 \times 1.6\ mA = 8\ mA$
$\varepsilon I_{OL} = 60$ mA from curve
pins = 60 mA ÷ 8 mA/pin = 7.5 = 7

In this case, 7 lines can sink 8 mA for a total of 56 mA. This leaves 4 mA sink current capability which can be divided in any way among the remaining 8 I/O lines of the 8243.

Example: This example shows how the use of the 20 mA sink capability of Port 7 affects the sinking capability of the other I/O lines.

An 8243 will drive the following loads simultaneously.

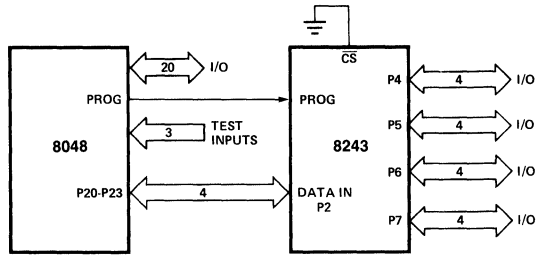
2 loads — 20 mA@1V (port 7 only)
8 loads — 4 mA@.45V
6 loads — 3.2 mA@.45V
Is this within the specified limits?

$\varepsilon I_{OL} = (2 \times 20) + (8 \times 4) + (6 \times 3.2) = 91.2$ mA.
From the curve: for $I_{OL} = 4$ mA, $\varepsilon I_{OL} \approx 93$ mA
since 91.2 mA < 93 mA the loads are within specified limits.

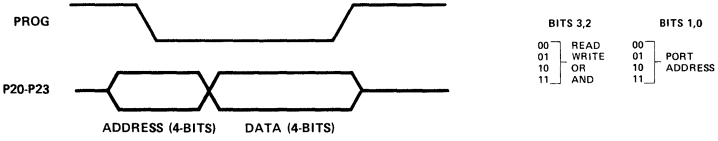
Although the 20 mA@1V loads are used in calculating εI_{OL}, it is the largest current required@.45V which determines the maximum allowable εI_{OL}.

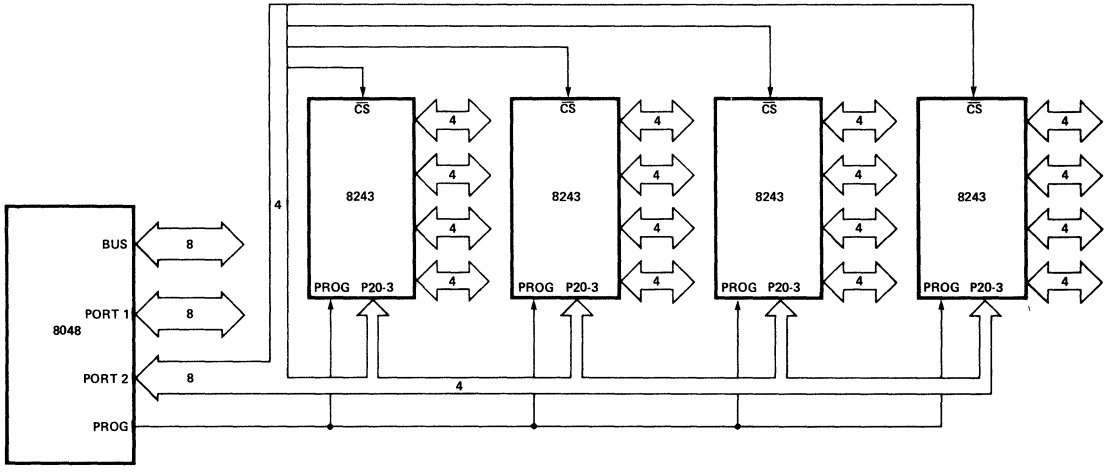
Note: A 10 to 50KΩ pullup resistor to +5V should be added to 8243 outputs when driving to 5V CMOS directly.

EXPANDER INTERFACE

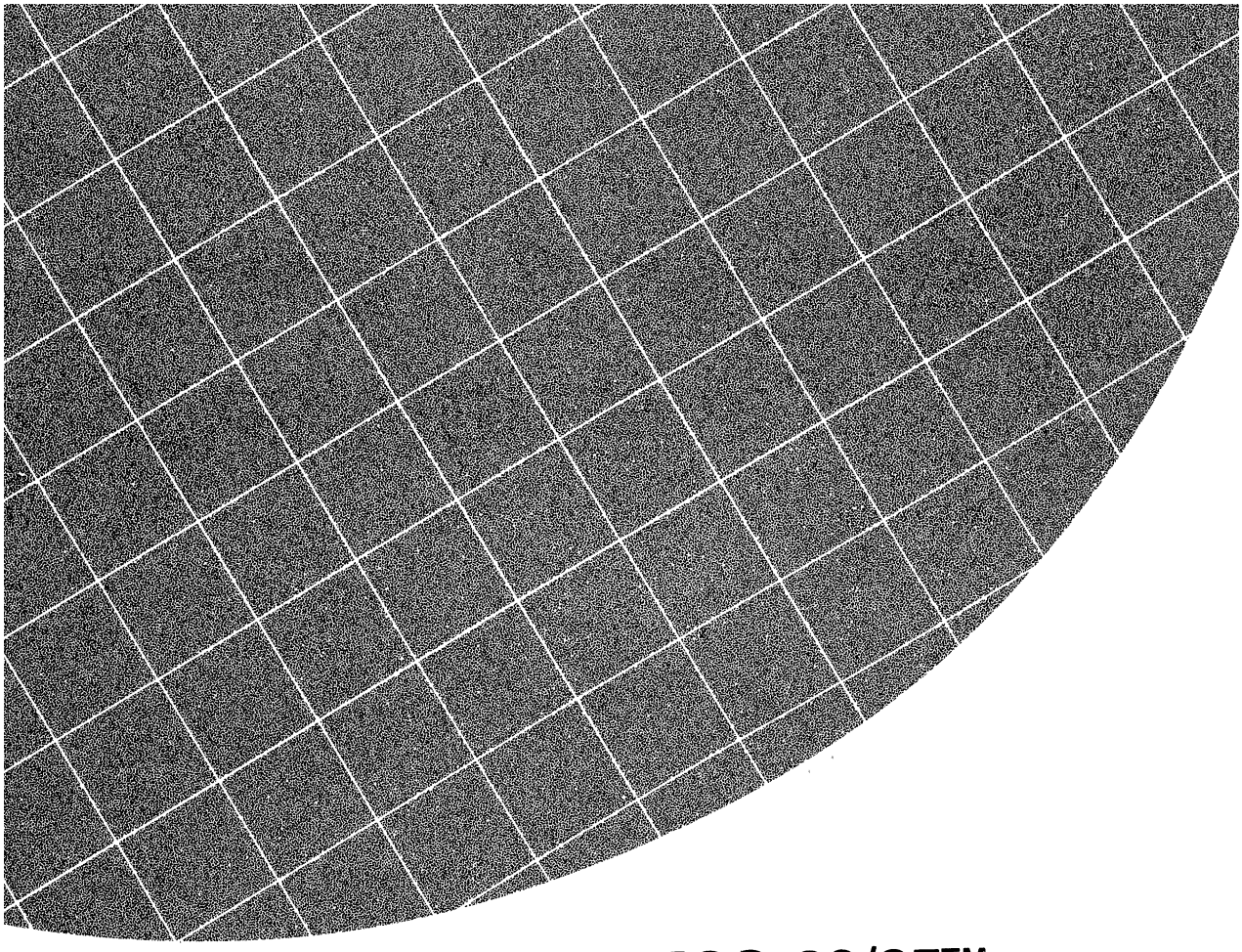


OUTPUT EXPANDER TIMING





USING MULTIPLE 8243's



MCS-80/85™ Microprocessors 9

INTRODUCTION

The MCS-80 and MCS-85 have become the industry standard 8-bit microcomputer systems. Their wide usage is due to many factors, among them total system support in terms of the largest family of state-of-the-art processors, memories, and peripheral components. Many of these are described in the pages that follow. In addition, system designers using the 8080A and 8085A have the benefit of the world's largest and most usable set of microcomputer development tools (see section 12).

The MCS-85 components are of particular interest for new microcomputer designs. Systems designed around the 8085A and the new 8085A-2 offer the highest performance-to-cost ratios in the industry. Higher speed, single power supply requirement, and low component count while maintaining total MCS-80 software compatibility are key features of the MCS-85 system.

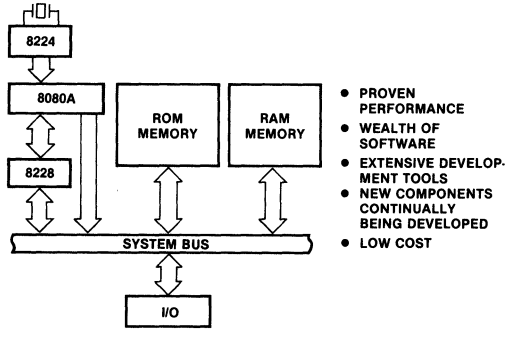


Figure 1. MCS-80™ — Foundation for MCS-85™

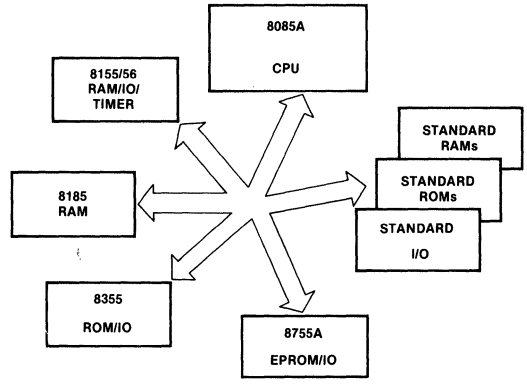


Figure 2. MCS-85™ — The New Industry Standard

Note: For more detailed information on the 8080A and 8085A microcomputer families, please consult the following:

MCS-80™ User's Manual (order number 98-153D) — Price $7.50
MCS-85™ User's Manual (order number 98-366E) — Price $5.00

Available from Intel, Literature Dept., 3065 Bowers Ave., Santa Clara, CA 95051

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8259A	Programmable Interrupt Controller	9-109
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8755A	16,384-Bit EPROM with I/O	9-132

Recommended Products For New 8085A Microcomputer Applications

Function	Part No.	Page No.	Description
Memory and I/O Expanders for MCS-85	8155/8156*	9-70	RAM-I/O-Timer
	8185*	9-77	1K x 8 Static Ram
	8355*	9-127	ROM-I/O
	8755A	9-132	EPROM-I/O
RAMs (Static)	2114	3-54	1K x 4
	2142	3-95	1K x 4
RAMs (Dynamic)	2117	3-64	16K x 1
	2118	3-88	16K x 1
RAM Support Circuits	8202	11-14	Dynamic RAM Controller
ROMs	2316E	4-12	2K x 8
EPROMs	2716	4-23	2K x 8
	2732	4-28	4K x 8
	2758	4-31	1K x 8
Microprocessor Support Circuits	8205	9-29	1-of-8 Decoder
	8257-5	9-92	DMA Controller
	8259A	9-109	Interrupt Controller
	8282	10-23	8-Bit Non-Inverting Latch
	8283	10-23	8-Bit Inverting Latch
	8286	10-33	8-Bit Non-Inverting Transceiver
	8287	10-33	8-Bit Inverting Transceiver
Peripherals	8251A	11-24	USART
	8253-5	11-32	Interval Timer
	8255A-5	11-43	PPI
	8271	11-64	Floppy Disk Controller
	8273	11-93	SDLC Controller
	8275	11-118	CRT Controller
	8278	11-142	Keyboard/Display Controller
	8279-5	11-152	Keyboard/Display Controller
	8291	11-164	GPIB Talker/Listener
	8292	11-188	GPIB Controller
	8294	11-190	Data Encrypter
	8295	11-201	Dot Matrix Printer Controller
	8041/8741	11-3	Universal Peripheral Interface

*For maximum performance use 8155-2/8156-2, 8185-2, and 8355-2 with the high performance 8085A-2 CPU.

8008/8008-1
8-BIT MICROPROCESSOR

- **Instruction Cycle Time — 1.25 μs with 8008-1 or 20 μs with 8008**
- **Directly Addresses 16K x 8 Bits of Memory (RAM, ROM, or S.R.)**
- **Interrupt Capability**
- **48 Instructions, Data Oriented**
- **Address Stack Contains 8 14-Bit Registers (Including Program Counter) Which Permit Nesting of Subroutines Up to 7 Levels**

The Intel® 8008 is a single chip MOS 8-bit parallel central processor unit (CPU) for the MCS-8 microcomputer system.

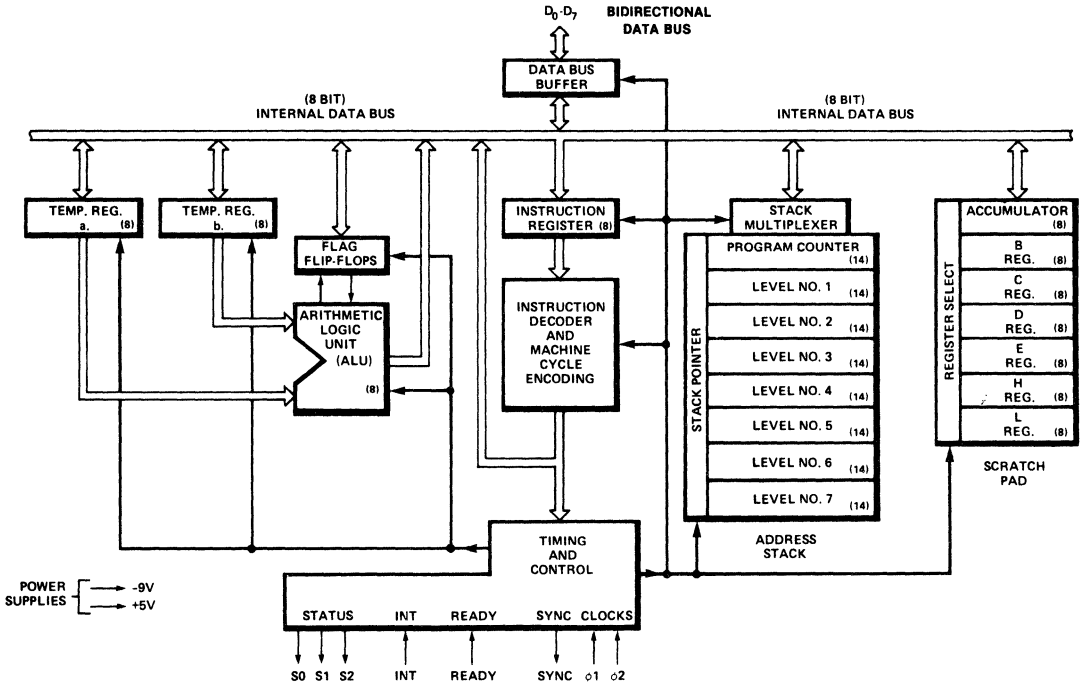
This CPU contains 6 8-bit data registers, an 8-bit accumulator, 2 8-bit temporary registers, 4 flag bits (carry, zero, sign, parity), and an 8-bit parallel binary arithmetic unit which implements addition, subtraction, and logical operations. A memory stack containing a 14-bit program counter and 7 14-bit words is used internally to store program and subroutine addresses. The 14-bit address permits the direct addressing of 16K words of memory (any mix of RAM, ROM, or S.R.).

The instruction set of the 8008 consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutine.

The normal program flow of the 8008 may be interrupted through the use of the interrupt control line. This allows the servicing of slow I/O peripheral devices while also executing the main program.

The ready command line synchronizes the 8008 to the memory cycle allowing any type or speed of semiconductor memory to be used.

BLOCK DIAGRAM



PIN DESCRIPTION

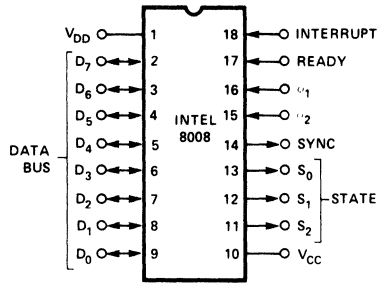


Figure 1. Pin Configuration

D_0-D_7

BI-DIRECTIONAL DATA BUS. All address and data communication between the processor and the program memory, data memory, and I/O devices occurs on these 8 lines. Cycle control information is also available.

INT

INTERRUPT input. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.

READY

READY input. This command line is used to synchronize the 8008 to the memory cycle allowing any speed memory to be used.

SYNC

SYNC output. Synchronization signal generated by the processor. It indicates the beginning of a machine cycle.

ϕ_1, ϕ_2

Two phase clock inputs.

S_0, S_1, S_2

MACHINE STATE OUTPUTS. The processor controls the use of the data bus and determines whether it will be sending or receiving data. State signals S_0, S_1, and S_2, along with SYNC inform the peripheral circuitry of the state of the processor.

V_{CC} +5V ±5%

V_{DD} -9V ±5%

INSTRUCTION SET

Data and Instruction Formats

Data in the 8008 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference, I/O arithmetic or logical, rotate or return instructions
Two Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	Immediate mode instructions
Three Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS	JUMP or CALL instructions
X X D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS*	*For the third byte of this instruction, D_6 and D_7 are "don't care" bits

For the MCS-8™ a logic "1" is defined as a high level and a logic "0" is defined as a low level.

Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE D_7 D_6	D_5 D_4 D_3	D_2 D_1 D_0	DESCRIPTION OF OPERATION
(1) MOV r_1, r_2	(5)	1 1	D D D	S S S	Load index register r_1 with the content of index register r_2.
(2) MOV r, M	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
MOV M, r	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) MVI r	(8)	0 0 B B	D D D B B B	1 1 0 B B B	Load index register r with data B . . . B.
MVI M	(9)	0 0 B B	1 1 1 B B B	1 1 0 B B B	Load memory register M with data B . . . B.
INR r	(5)	0 0	D D D	0 0 0	Increment the content of index register r (r ≠ A).
DCR r	(5)	0 0	D D D	0 0 1	Decrement the content of index register r (r ≠ A).

Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADD r	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADD M	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0 B B	0 0 0 B B B	1 0 0 B B B	
ADC r	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B from the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ADC M	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0 B B	0 0 1 B B B	1 0 0 B B B	
SUB r	(5)	1 0	0 1 0	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUB M	(8)	1 0	0 1 0	1 1 1	
SUI	(8)	0 0 B B	0 1 0 B B B	1 0 0 B B B	
SBB r	(5)	1 0	0 1 1	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBB M	(8)	1 0	0 1 1	1 1 1	
SBI	(8)	0 0 B B	0 1 1 B B B	1 0 0 B B B	

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7 D_6$	$D_5 D_4 D_3$	$D_2 D_1 D_0$	DESCRIPTION OF OPERATION
ANA r	(5)	1 0	1 0 0	S S S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
ANA M	(8)	1 0	1 0 0	1 1 1	
ANI	(8)	0 0	1 0 0	1 0 0	
		B B	B B B	B B B	
XRA r	(5)	1 0	1 0 1	S S S	Compute the EXCLUSIVE OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
XRA M	(8)	1 0	1 0 1	1 1 1	
XRI	(8)	0 0	1 0 1	1 0 0	
		B B	B B B	B B B	
ORA r	(5)	1 0	1 1 0	S S S	Compute the INCLUSIVE OR of the content of index register r, memory register m, or data B . . . B with the accumulator.
ORA M	(8)	1 0	1 1 0	1 1 1	
ORI	(8)	0 0	1 1 0	1 0 0	
		B B	B B B	B B B	
CMP r	(5)	1 0	1 1 1	S S S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CMP M	(8)	1 0	1 1 1	1 1 1	
CPI	(8)	0 0	1 1 1	1 0 0	
		B B	B B B	B B B	
RLC	(5)	0 0	0 0 0	0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0	0 0 1	0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0	0 1 0	0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0	0 1 1	0 1 0	Rotate the content of the accumulator right through the carry.

Program Counter and Stack Control Instructions

(4) JMP	(11)	0 1	X X X	1 0 0	Unconditionally jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$.
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	
		X X	B_3 B_3 B_3	B_3 B_3 B_3	
(5) JNC, JNZ, JP, JPO	(9 or 11)	0 1	0 C_4 C_3	0 0 0	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	
		X X	B_3 B_3 B_3	B_3 B_3 B_3	
JC, JZ JM, JPE	(9 or 11)	0 1	1 C_4 C_3	0 0 0	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	
		X X	B_3 B_3 B_3	B_3 B_3 B_3	
CALL	(11)	0 1	X X X	1 1 0	Unconditionally call the subroutine at memory address $B_3 \ldots$ $B_3B_2 \ldots B_2$. Save the current address (up one level in the stack).
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	
		X X	B_3 B_3 B_3	B_3 B_3 B_3	
CNC, CNZ, CP, CPO	(9 or 11)	0 1	0 C_4 C_3	0 1 0	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is false, and save the current address (up one level in the stack.) Otherwise, execute the next instruction in sequence.
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	
		X X	B_3 B_3 B_3	B_3 B_3 B_3	
CC, CZ, CM, CPE	(9 or 11)	0 1	1 C_4 C_3	0 1 0	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
		B_2 B_2	B_2 B_2 B_2	B_2 B_2 B_2	
		X X	B_3 B_3 B_3	B_3 B_3 B_3	
RET	(5)	0 0	X X X	1 1 1	Unconditionally return (down one level in the stack).
RNC, RNZ, RP, RPO	(3 or 5)	0 0	0 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is false. Otherwise, execute the next instruction in sequence.
RC, RZ RM, RPE	(3 or 5)	0 0	1 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0	A A A	1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).

Input/Output Instructions

IN	(8)	0 1	0 0 M	M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1	R R M	M M 1	Write the content of the accumulator into the selected output port (RRMMM, RR ≠ 00)

Machine Instruction

HLT	(4)	0 0	0 0 0	0 0 X	Enter the STOPPED state and remain there until interrupted.
	(4)	1 1	1 1 1	1 1 1	

NOTES

(1) SSS = Source Index Register, DDD = Destination Index Register — These registers, r_i, are designated A(accumulator–000), B(001), C(010), D(011), E(100), H(101), L(110).

(2) Memory registers are addressed by the contents of registers H & L.

(3) Additional bytes of instruction are designated by BBBBBBBB.

(4) X = "Don't Care".

(5) Flag flip-flops are defined by C_4C_3 carry (00-overflow or underflow), zero (01-result is zero), sign (10-MSB of result is "1"), parity (11-parity is even).

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−55°C to +150°C
Input Voltages and Supply Voltage With Respect to V_{CC}	+0.5 to −20V
Power Dissipation	1.0 W @ 25°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to 70°C, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$ unless otherwise specified. Logic "1" is defined as the more positive level (V_{IH}, V_{OH}). "0" is defined as the more negative level (V_{IL}, V_{OL}).

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
I_{DD}	AVERAGE SUPPLY CURRENT-OUTPUTS LOADED*		30	60	mA	$T_A = 25°C$
I_{LI}	INPUT LEAKAGE CURRENT			10	μA	$V_{IN} = 0V$
V_{IL}	INPUT LOW VOLTAGE (INCLUDING CLOCKS)	V_{DD}		$V_{CC}-4.2$	V	
V_{IH}	INPUT HIGH VOLTAGE (INCLUDING CLOCKS)	$V_{CC}-1.5$		$V_{CC}+0.3$	V	
V_{OL}	OUTPUT LOW VOLTAGE			0.4	V	$I_{OL} = 0.44mA$ $C_L = 200$ pF
V_{OH}	OUTPUT HIGH VOLTAGE	$V_{CC}-1.5$			V	$I_{OH} = 0.2mA$

*Measurements are made while the 8008 is executing a typical sequence of instructions. The test load is selected such that at $V_{OL} = 0.4V$, $I_{OL} = 0.44mA$ on each output.

A.C. CHARACTERISTICS

$T_A = 0°C$ to 70°C; $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$. All measurements are referenced to 1.5V levels.

SYMBOL	PARAMETER	8008 LIMITS MIN.	8008 LIMITS MAX.	8008-1 LIMITS MIN.	8008-1 LIMITS MAX.	UNIT	TEST CONDITIONS
t_{CY}	CLOCK PERIOD	2	3	1.25	3	μs	$t_R, t_F = 50$ns
t_R, t_F	CLOCK RISE AND FALL TIMES		50		50	ns	
$t_{\phi 1}$	PULSE WIDTH OF ϕ_1	.70		.35		μs	
$t_{\phi 2}$	PULSE WIDTH OF ϕ_2	.55		.35		μs	
t_{D1}	CLOCK DELAY FROM FALLING EDGE OF ϕ_1 TO FALLING EDGE OF ϕ_2	.90	1.1		1.1	μs	
t_{D2}	CLOCK DELAY FROM ϕ_2 TO ϕ_1	.40		.35		μs	
t_{D3}	CLOCK DELAY FROM ϕ_1 TO ϕ_2	.20		.20		μs	
t_{DD}	DATA OUT DELAY		1.0		1.0	μs	$C_L = 100$pF
t_{OH}	HOLD TIME FOR DATA BUS OUT	.10		.10		μs	
t_{IH}	HOLD TIME FOR DATA IN	[1]		[1]		μs	
t_{SD}	SYNC OUT DELAY		.70		.70	μs	$C_L = 100$pF
t_{S1}	STATE OUT DELAY (ALL STATES EXCEPT T1 AND T1I) [2]		1.1		1.1	μs	$C_L = 100$pF
t_{S2}	STATE OUT DELAY (STATES T1 AND T1I)		1.0		1.0	μs	$C_L = 100$pF
t_{RW}	PULSE WIDTH OF READY DURING ϕ_{22} TO ENTER T3 STATE	.35		.35		μs	
t_{RD}	READY DELAY TO ENTER WAIT STATE	.20		.20		μs	

[1] t_{IH} MIN ≥ t_{SD}

[2] If the INTERRUPT is not used, all states have the same output delay, t_{S1}.

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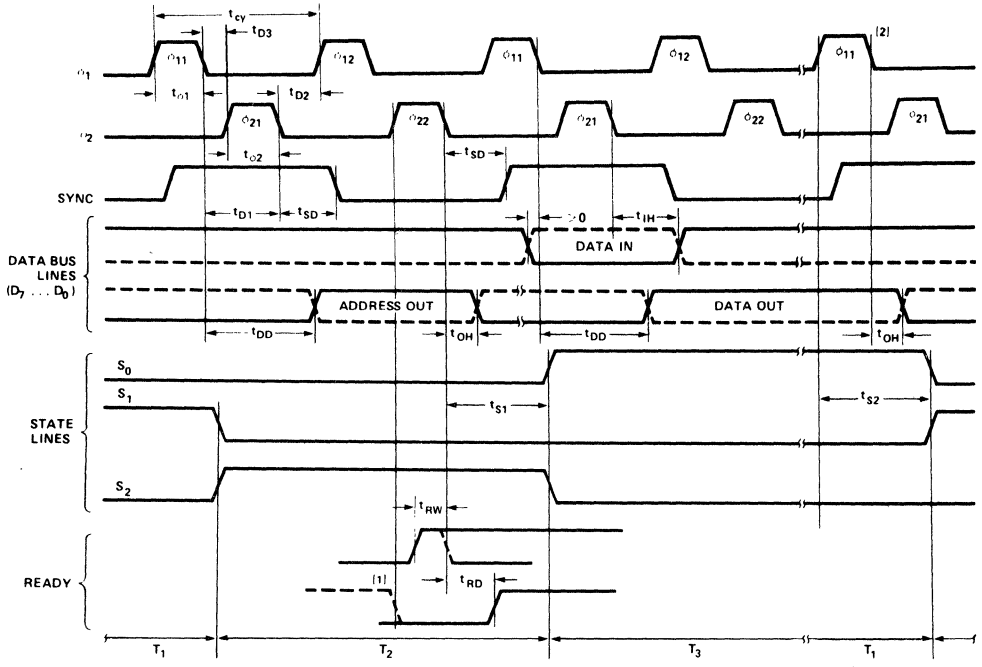
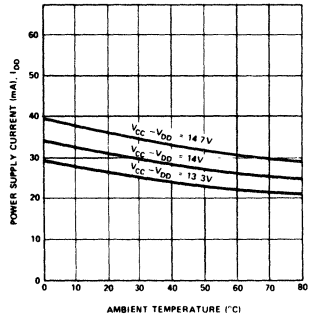
TIMING DIAGRAM



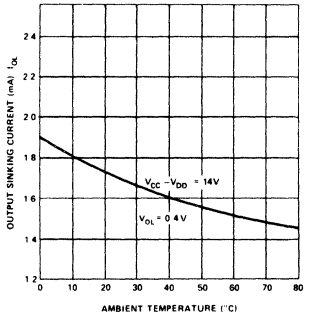
Notes: 1. READY line must be at "0" prior to ϕ_{22} of T_2 to guarantee entry into the WAIT state.
2. INTERRUPT line must not change levels within 200ns (max.) of falling edge of ϕ_1.

TYPICAL D.C. CHARACTERISTICS

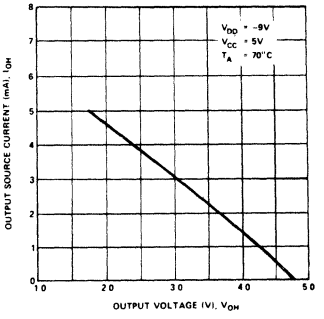
POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT SINKING CURRENT VS. TEMPERATURE

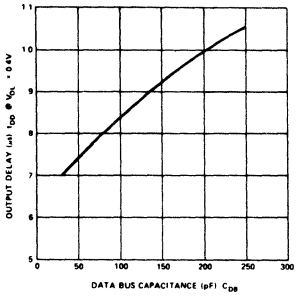


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



TYPICAL A.C. CHARACTERISTICS

DATA OUT DELAY VS. OUTPUT LOAD CAPACITANCE



CAPACITANCE f = 1MHz; T_A = 25°C; Unmeasured Pins Grounded

SYMBOL	TEST	LIMIT (pF)	
		TYP.	MAX.
C_{IN}	INPUT CAPACITANCE	5	10
C_{DB}	DATA BUS I/O CAPACITANCE	5	10
C_{OUT}	OUTPUT CAPACITANCE	5	10

8080A/8080A-1/8080A-2
8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

- **TTL Drive Capability**
- **2 μs (– 1:1.3 μs, – 2:1.5 μs) Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **6 General Purpose Registers and an Accumulator**
- **16-Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **16-Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary, and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

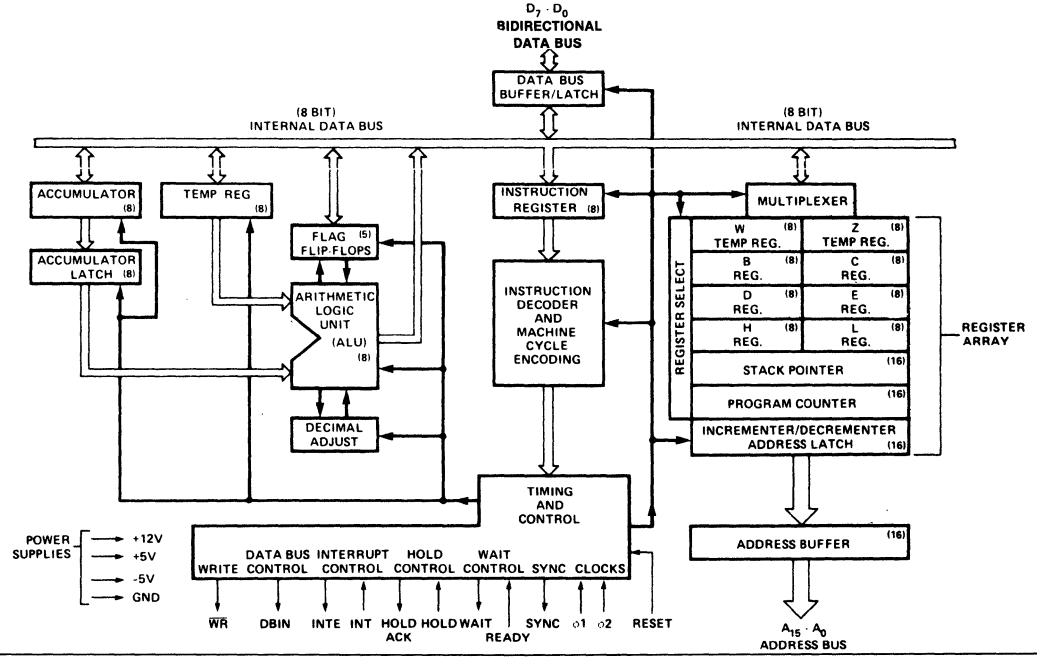
The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains 6 8-bit general purpose working registers and an accumulator. The 6 general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset 4 testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter, and all of the 6 general purpose registers. The 16-bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bidirectional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multiprocessor operation.

8080A CPU FUNCTIONAL BLOCK DIAGRAM



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PIN DESCRIPTION

The following describes the function of all of the 8080A I/O pins. Several of the descriptions refer to internal timing periods.

A_{15}-A_0 (output three-state)
ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.

D_7-D_0 (input/output three-state)
DATA BUS; the data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D_0 is the least significant bit.

SYNC (output)
SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)
DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.

READY (input)
READY; the READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)
WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

$\overline{WR}$ (output)
WRITE; the $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR}$ = 0).

HOLD (input)
HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

- the CPU is in the HALT state.
- the CPU is in the T2 or TW state and the READY signal is active.

As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)
HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:

- T3 for READ memory or input.
- The Clock Period following T3 for WRITE memory or OUTPUT operation.

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.

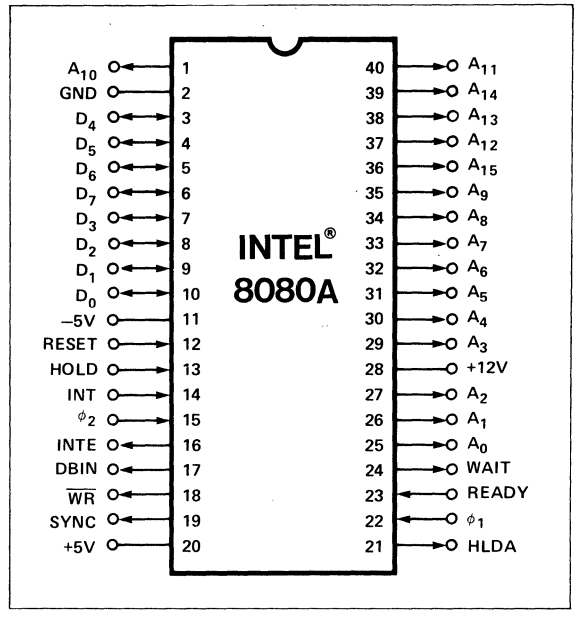


Figure 1. Pin Configuration

INTE (output)
INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)
INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input) [1]
RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS}	Ground Reference.
V_{DD}	+12 ± 5% Volts.
V_{CC}	+5 ± 5% Volts.
V_{BB}	-5 ±5% Volts (substrate bias).
ϕ_1, ϕ_2	2 externally supplied clock phases. (non TTL compatible)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70° C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}−1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}−1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = -150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	T_{CY} = .48 μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leq V_{IN} \leq V_{SS}+0.8V$ $V_{SS}+0.8V \leq V_{IN} \leq V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS} = 0V$, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

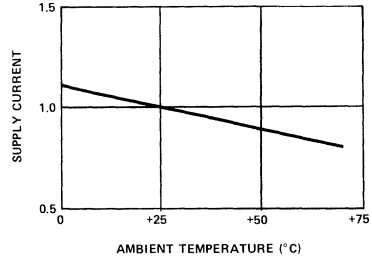


Figure 2. Typical Supply Current vs. Temperature, Normalized[3]

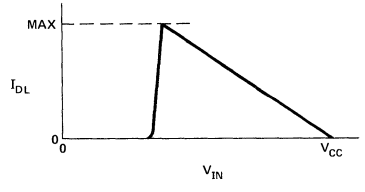


Figure 3. Data Bus Characteristic During DBIN

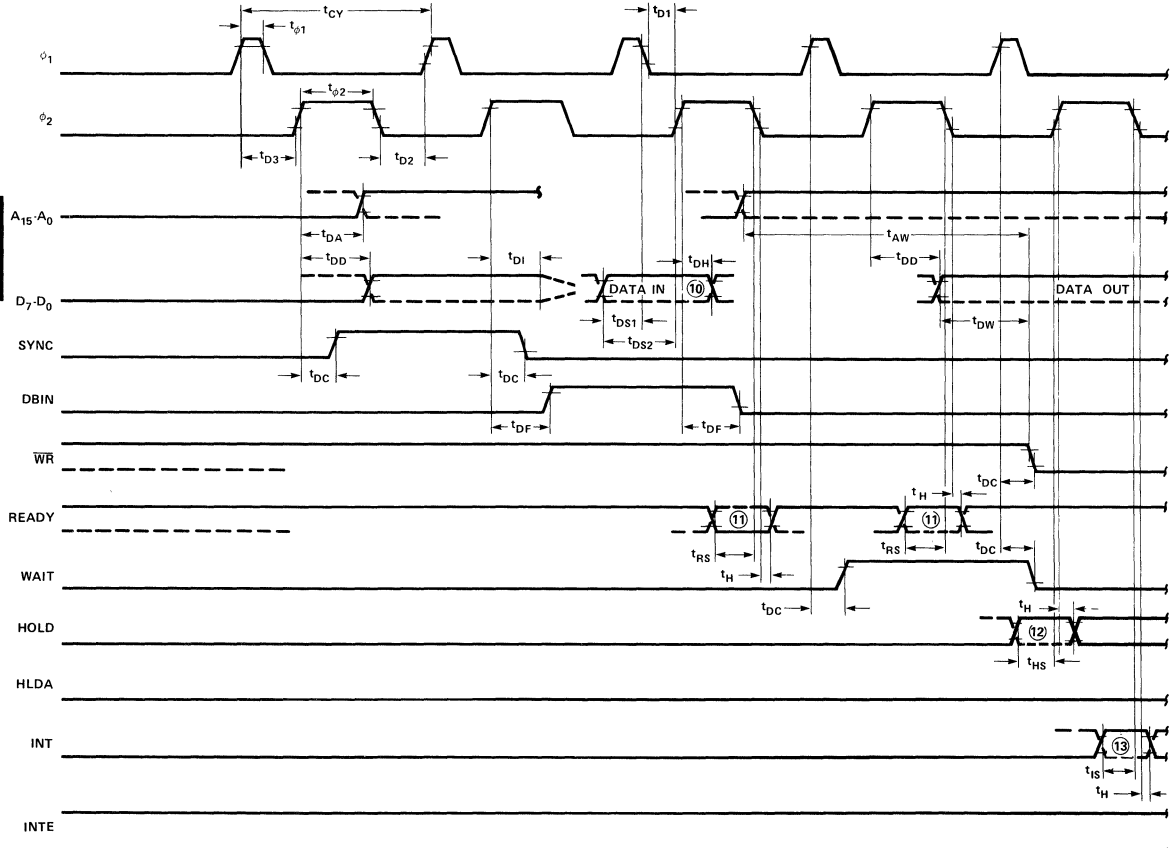
A.C. CHARACTERISTICS (8080A)

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	-1 Min.	-1 Max.	-2 Min.	-2 Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	0.48	2.0	0.32	2.0	0.38	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	0	25	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		50		60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		145		175		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		0		0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	70		60		70		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		60		70		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		200		150		175	nsec	C_L = 100 pF
t_{DD}[2]	Data Output Delay From ϕ_2		220		180		200	nsec	C_L = 100 pF
t_{DC}[2]	Signal Output Delay From ϕ_2 or ϕ_2 (SYNC, WR, WAIT, HLDA)		120		110		120	nsec	C_L = 50 pF
t_{DF}[2]	DBIN Delay From ϕ_2	25	140	25	130	25	140	nsec	C_L = 50 pF
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}		t_{DF}		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		10		20		nsec	

WAVEFORMS

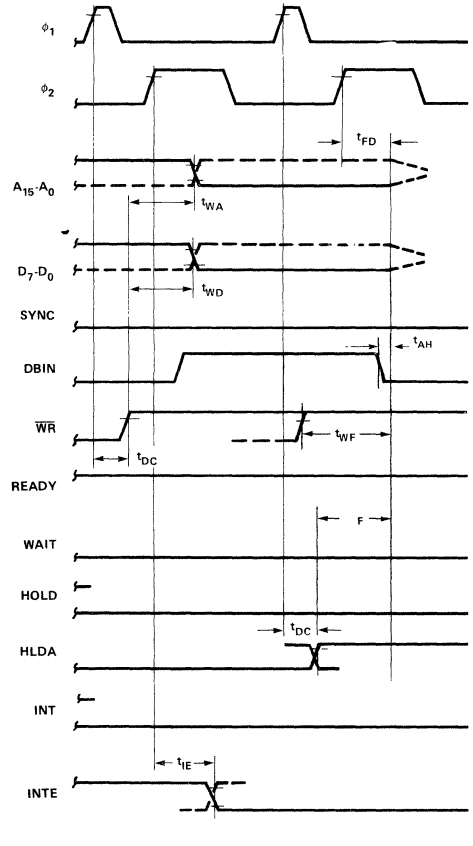
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



A.C. CHARACTERISTICS (8080A)

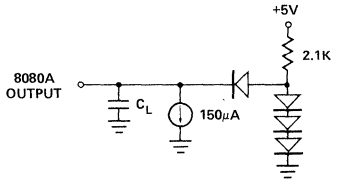
T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted

Symbol	Parameter	Min.	Max.	-1 Min.	-1 Max.	-2 Min.	-2 Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	150		120		130		nsec	
t_{DH}[1]	Data Holt time From ϕ_2 During DBIN	[1]		[1]		[1]		nsec	
t_{IE}[2]	INTE Output Delay From ϕ_2		200		200		200	nsec	C_L = 50 pF
t_{RS}	READY Setup Time During ϕ_2	120		90		90		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		120		120		nsec	
t_{IS}	INT Setup Time During ϕ_2	120		100		100		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		0		0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120		120		120	nsec	
t_{AW}[2]	Address Stable Prior to WR	[5]		[5]		[5]		nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$,HLDA,DBIN
t_{DW}[2]	Output Data Stable Prior to WR	[6]		[6]		[6]		nsec	
t_{WD}[2]	Output Data Stable From WR	[7]		[7]		[7]		nsec	
t_{WA}[2]	Address Stable From WR	[7]		[7]		[7]		nsec	
t_{HF}[2]	HLDA to Float Delay	[8]		[8]		[8]		nsec	
t_{WF}[2]	WR to Float Delay	[9]		[9]		[9]		nsec	
t_{AH}[2]	Address Hold Time After DBIN During HLDA	-20		-20		-20		nsec	



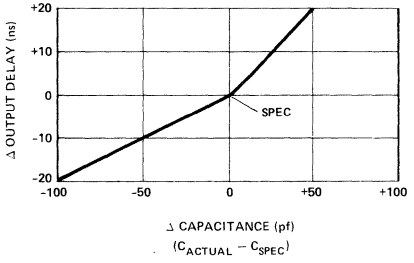
NOTES: (Parenthesis gives -1, -2 specifications, respectively)

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480$ ns (-1:320 ns, -2:380 ns).

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the 8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$ ns (-1:110 ns, -2:130 ns).
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$ ns (-1:150 ns, -2:170 ns).
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080A instruction set.

The following special instruction group completes the 8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the 8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

TYPICAL INSTRUCTIONS

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Immediate mode or I/O instructions

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

Jump, call or direct load and store instructions

For the 8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

8080 INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
MOVE, LOAD, AND STORE										
MOVr1,r2	Move register to register	0	1	D	D	D	S	S	S	5
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	11
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10

NOTES: 1. DDD or SSS: B: 000, C: 001, D: 010, E: 011, H: 100, L: 101, Memory: 110, A: 111
2. Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags

Summary of Processor Instructions (Cont.)

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	7

NOTES: 1. DDD or SSS: B=000. C=001. D=010. E=011. H=100. L=101. Memory=110. A=111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags

8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

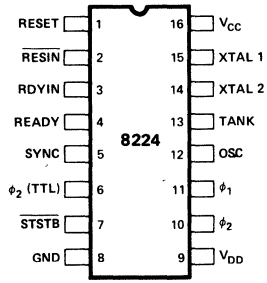
- **Single Chip Clock Generator/Driver for 8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**

The Intel® 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer to meet a variety of system speed requirements.

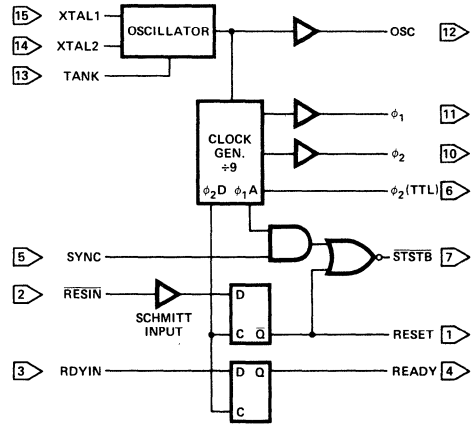
Also included are circuits to provide power-up reset, advance status strobe, and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
φ1	8080 CLOCKS
φ2	8080 CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
φ2 (TTL)	φ2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . . −0.5V to +7V
Supply Voltage, V_{DD} . . . . . −0.5V to +13.5V
Input Voltage . . . . . −1.5V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = +5.0V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
I_F	Input Current Loading			-.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.25V
V_C	Input Forward Clamp Voltage			1.0	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.6 2.0			V	Reset Input All Other Inputs
V_{IH}-V_{IL}	RESIN Input Hysteresis	.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage			.45 .45	V V	(ϕ_1,ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} =2.5mA All Other Outputs I_{OL} = 15mA
V_{OH}	Output "High" Voltage ϕ_1 , ϕ_2 READY, RESET All Other Outputs	 9.4 3.6 2.4			 V V V	 I_{OH} = -100μA I_{OH} = -100μA I_{OH} = -1mA
I_{SC}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

Crystal Requirements

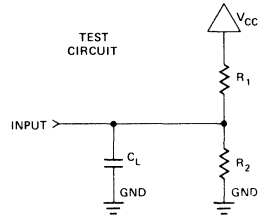
Tolerance: 0.005% at 0°C-70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35 pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4 mW

*With tank circuit use 3rd overtone mode.

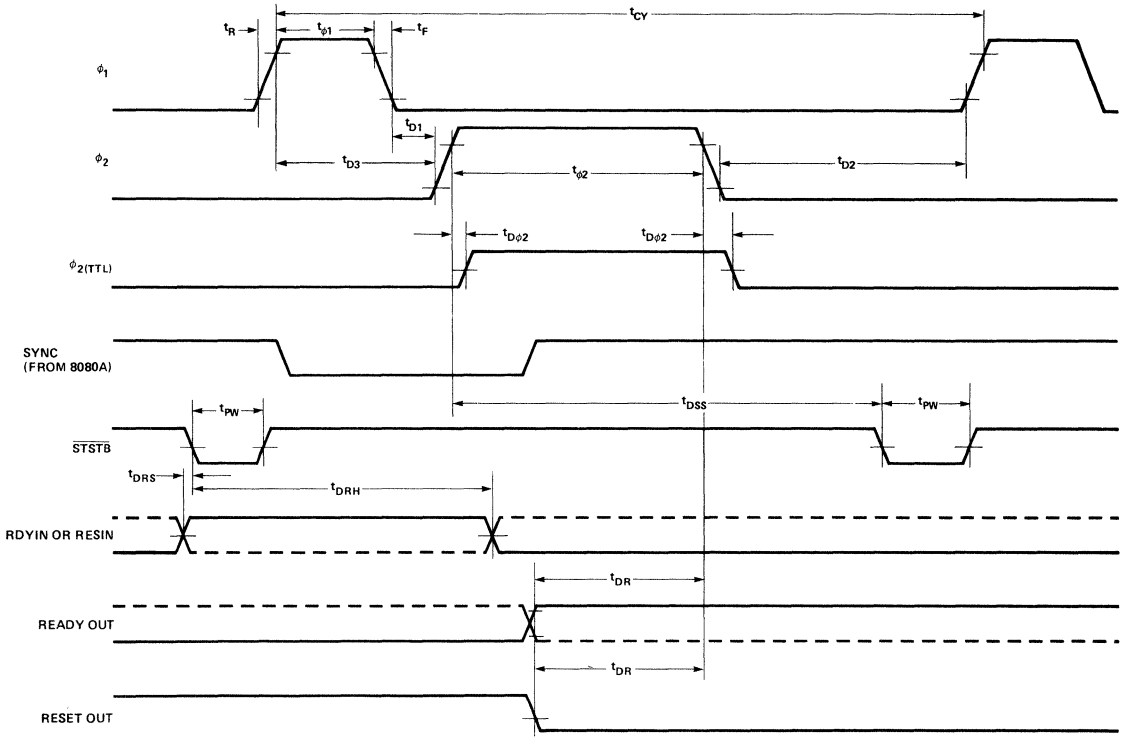
A.C. CHARACTERISTICS

V_{CC} = +5.0V ± 5%; V_{DD} = +12.0V ± 5%; T_A = 0°C to 70°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9}$ - 20ns			ns	C_L = 20pF to 50pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9}$ - 35ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9}$ - 14ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9}$ + 20ns		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2TTL,CL=30 R_1=300Ω R_2=600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9}$ - 30ns		$\frac{6tcy}{9}$		$\overline{STSTB}$,CL=15pF R_1 = 2K R_2 = 4K
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9}$ - 15ns				
t_{DRS}	RDYIN Setup Time to Status Strobe	50ns - $\frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	$\frac{4tcy}{9}$ - 25ns				Ready & Reset CL=10pF R_1=2K R_2=4K
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency			27	MHz	
C_{in}	Input Capacitance			8	pF	V_{CC}=+5.0V V_{DD}=+12V V_{BIAS}=2.5V f=1MHz



WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

EXAMPLE:

A.C. CHARACTERISTICS (For t_{CY} = 488.28 ns)

T_A = 0°C to 70°C; V_{DD} = +5V ±5%; V_{DD} = +12V ±5%.

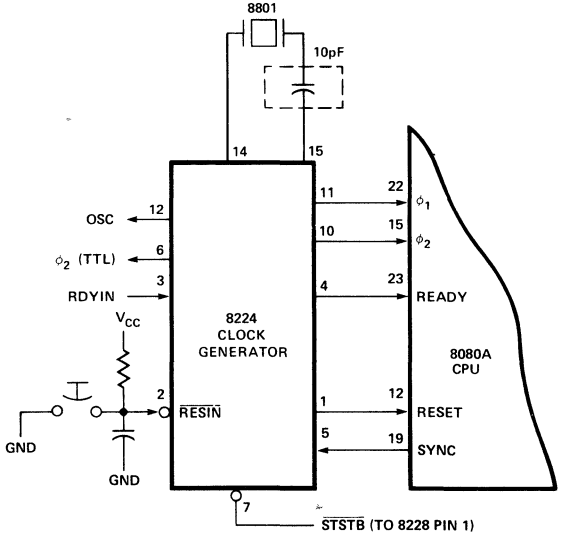
Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY}=488.28ns
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	Ready & Reset Loaded to 2mA/10pF
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5V unless specified otherwise.
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	

8801
CLOCK GENERATOR CRYSTAL FOR 8224/8080A

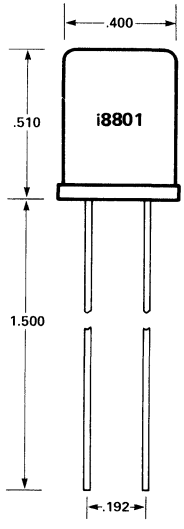
- **Specifically Selected for Intel® 8224**
- **18.432 MHz for 1.95 μs 8080A Cycle**
- **Simple Generation of all Standard Communication Baud Rates**
- **Frequency Deviation ±0.005%**
- **Fundamental Frequency Mode**
- **0°C to 70°C Operating Temperature**

The Intel® 8801 is a quartz crystal specifically selected to operate with the 8224 clock generator and the 8080A CPU. It resonates in the fundamental frequency mode at 18.432 MHz. This frequency allows the 8080A at full speed (T_{CY} = 488 ns) to have a cycle of 1.95 μs and also simplifies the generation of all standard communication baud rates. The 8801 crystal is exactly matched to the requirements of the 8080A/8224 and provides both high performance and system flexibility for the microcomputer designer.

8801 INTERFACE



PACKAGING INFORMATION



MCS-80/85

APPLICATIONS

The selection of 18.432 MHz provides the 8080A with clocks whose period is 488ns. This allows the 8080A to operate at very close to its maximum specified speed (480 ns). The 8224, when used with the 8801, outputs a signal on its OSC pin that is an approximately symetrical square wave at a frequency of 18.432 MHz. This frequency signal can be easily divided down to generate an accurate, stable baud rate clock that can be connected directly to the transmitter or receiver clocks of the 8251 USART. This feature allows the designer to support most standard communication interfaces with a minimum of extra hardware.

The chart below (Fig. 1) shows the equivalent baud rates that are generated with the corresponding dividers.

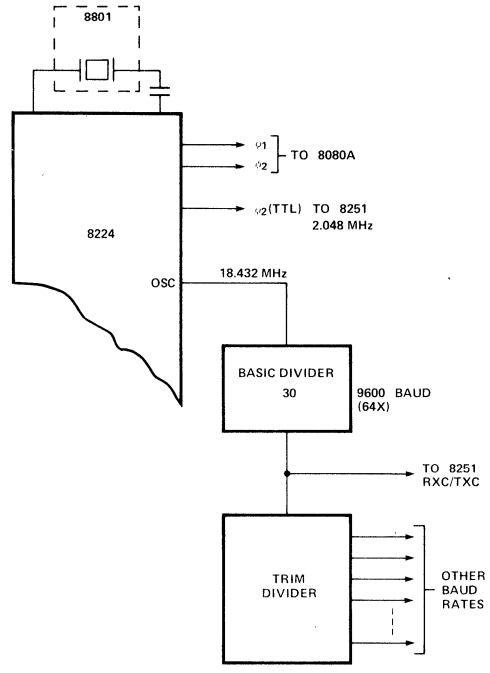


Figure 1. Block Diagram

BAUD RATE 64x	BAUD RATE 16x	FREQUENCY	BASIC DIVIDER	PLUS TRIM DIVIDER
9600		614.4 KH	÷30	–
4800	19.2K	307.2 KH	÷30	÷2
2400	9600	153.6 KH	÷30	÷4
1200	4800	76.8 KH	÷30	÷8
600	2400	38.4 KH	÷30	÷16
300	1200	19.2 KH	÷30	÷32
	600	9.6 KH	÷30	÷64
	300	4.8 KH	÷30	÷128
*109.1		6.982 KH	÷30	÷88

*For 109.1 (64x) Baud rate divide 1200 Baud Frequency (76.8 KH) by 11.

Figure 2. Baud Rate Chart

ELECTRICAL CHARACTERISTICS

Recommended Drive Level 5mW
Type of Resonance . . . . . Series
Equivalent Resistance . . . . . 20 ohms
Maximum Shunt Capacity 7pF
Maximum Frequency Deviation
0° – 70°C . . . . . ±.005%
-55°– 125°C . . . . . ±.002%

8228/8238
SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- **Single Chip System Control for MCS-80™ Systems**
- **Built-In Bidirectional Bus Driver for Data Bus Isolation**
- **Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28-Pin Dual In-Line Package**
- **Reduces System Package Count**
- ***8238 Has Advanced IOW/MEMW for Large System Timing Control**

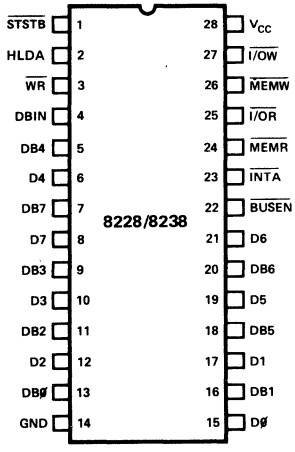
The Intel® 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bidirectional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

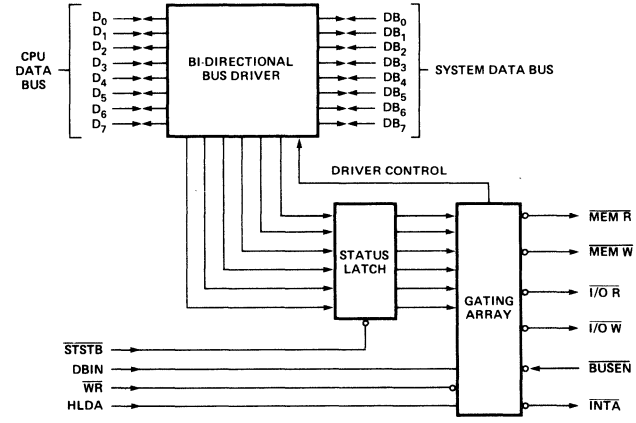
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an interrupt acknowledge by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable design of the MCS-80 systems.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
I/OR	I/O READ	WR	WR (FROM 8080)
I/OW	I/O WRITE	BUSEN	BUS ENABLE INPUT
MEMR	MEMORY READ	STSTB	STATUS STROBE (FROM 8224)
MEMW	MEMORY WRITE	VCC	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . . −0.5V to +7V
Input Voltage . . . . . −1.5V to +7V
Output Current 100mA

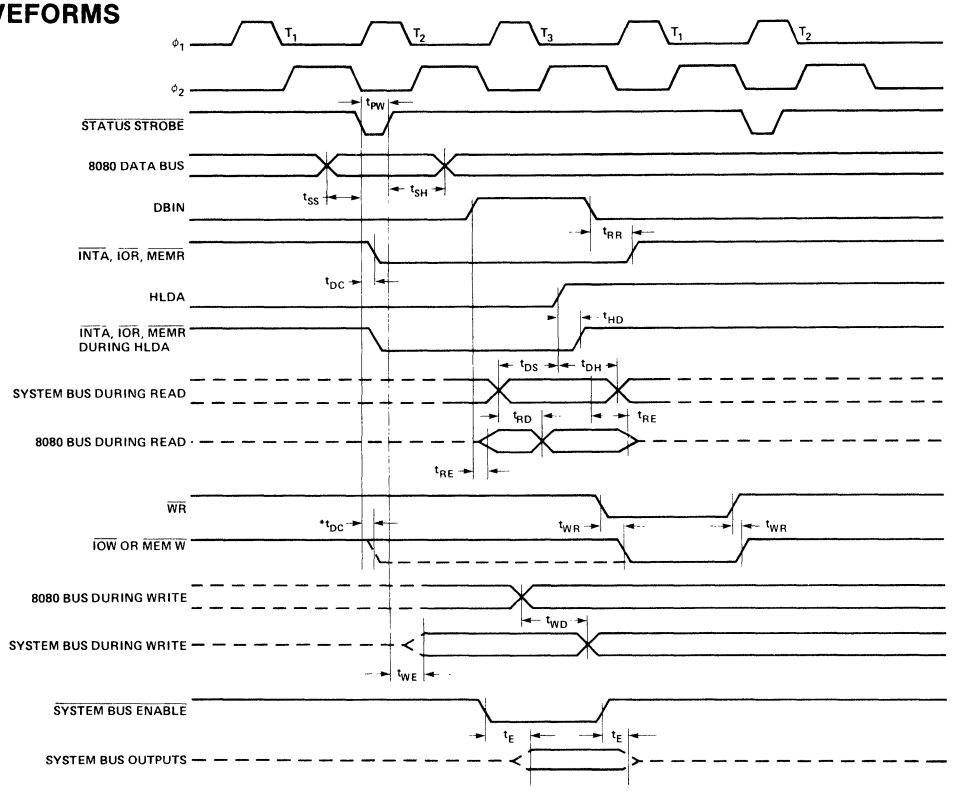
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		.75	-1.0	V	V_{CC}=4.75V; I_C=-5mA
I_F	Input Load Current, $\overline{STSTB}$			500	μA	V_{CC} = 5.25V
	D_2 & D_6			750	μA	V_F = 0.45V
	D_0, D_1, D_4, D_5, & D_7			250	μA	
	All Other Inputs			250	μA	
I_R	Input Leakage Current $\overline{STSTB}$			100	μA	V_{CC} = 5.25V
	DB_0-DB_7			20	μA	V_R = 5.25V
	All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		140	190	mA	V_{CC}=5.25V
V_{OL}	Output Low Voltage, D_0-D_7			.45	V	V_{CC}=4.75V; I_{OL}=2mA
	All Other Outputs			.45	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0-D_7	3.6	3.8		V	V_{CC}=4.75V; I_{OH}=-10μA
	All Other Outputs	2.4			V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15		90	mA	V_{CC}=5V
$I_{O(off)}$	Off State Output Current, All Control Outputs			100	μA	V_{CC}=5.25V; V_O=5.25
				-100	μA	V_O=.45V
I_{INT}	INTA Current			5	mA	(See Figure below)

Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*ADVANCED $\overline{IOW}$/$\overline{MEMW}$ FOR 8238 ONLY.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$.

Symbol	Parameter	Limits Min.	Limits Max.	Units	Condition
t_{PW}	Width of Status Strobe	22		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	60	ns	C_L = 100pF
t_{RR}	Delay from DBIN to Control Outputs		30	ns	C_L = 100pF
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	C_L = 25pF
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	C_L = 25pF
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	45	ns	C_L = 100pF
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	C_L = 100pF
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	C_L = 100pF
t_E	Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7		30	ns	C_L = 100pF
t_{HD}	HLDA to Read Status Outputs		25	ns	
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	C_L = 100pF

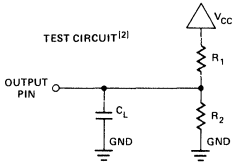
CAPACITANCE

This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

Test Conditions: NS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, f = 1MHz.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.



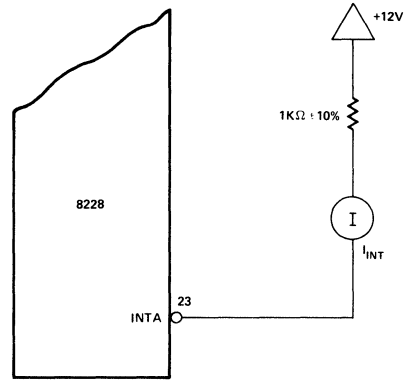


Figure 1. INTA Test Circuit (for RST 7)

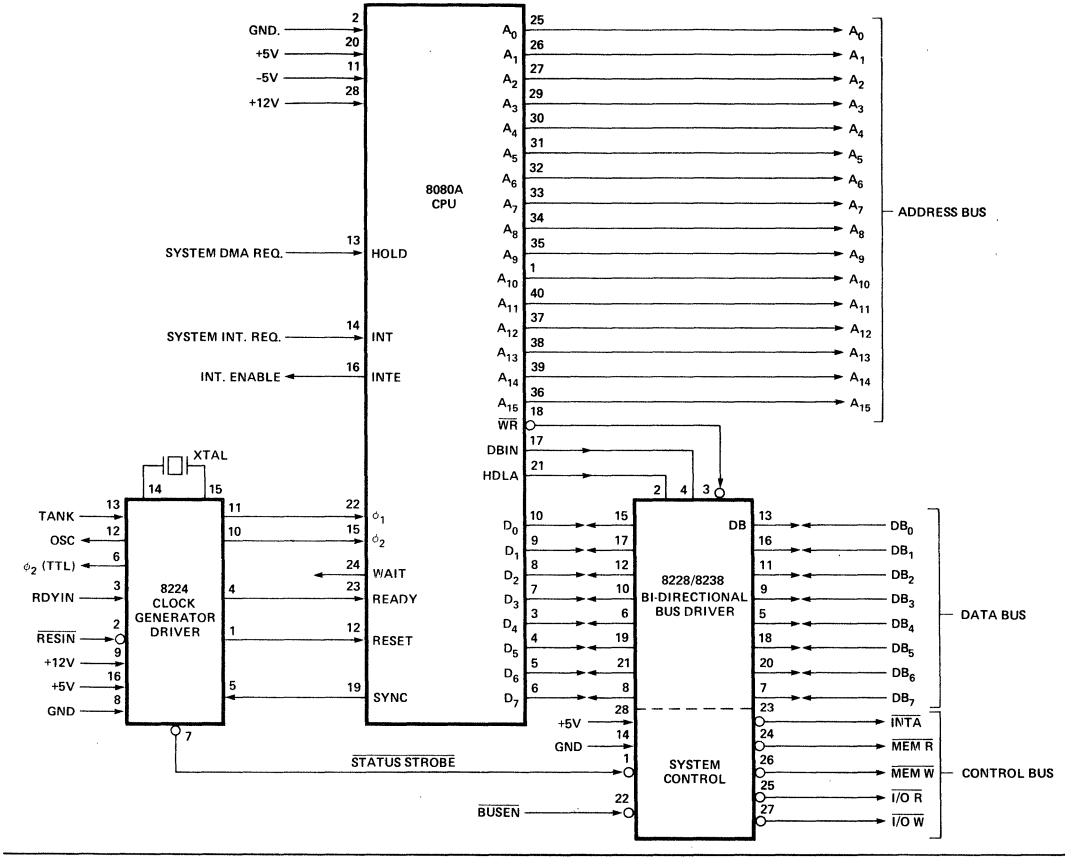


Figure 2. CPU Standard Interface

8205

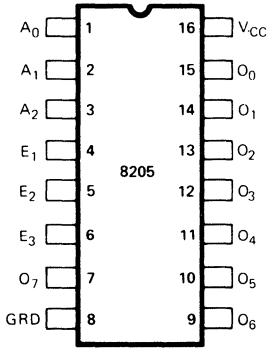
HIGH SPEED 1 OUT OF 8 BINARY DECODER

- **I/O Port or Memory Selector**
- **Simple Expansion — Enable Inputs**
- **High Speed Schottky Bipolar Technology — 18ns Max. Delay**
- **Directly Compatible with TTL Logic Circuits**
- **Low Input Load Current — .25 mA max., 1/6 Standard TTL Input Load**
- **Minimum Line Reflection — Low Voltage Diode Input Clamp**
- **Outputs Sink 10 mA min.**
- **16-Pin Dual-In-Line Ceramic or Plastic Package**

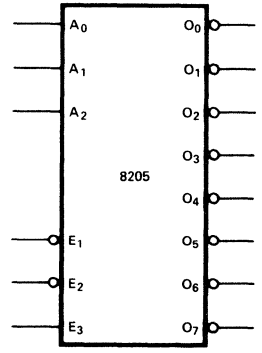
The 8205 decoder can be used for expansion of systems which utilize input ports, output ports, and memory components with active low chip select input. When the 8205 is enabled, one of its eight outputs goes "low", thus a single row of a memory system is selected. The 3 chip enable inputs on the 8205 allow easy system expansion. For very large systems, 8205 decoders can be cascaded such that each decoder can drive eight other decoders for arbitrary memory expansions.

The Intel® 8205 is packaged in a standard 16 pin dual-in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffusion process.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A_0-A_2	ADDRESS INPUTS
$\overline{E_1}$-$\overline{E_3}$	ENABLE INPUTS
$\overline{O_0}$-$\overline{O_7}$	DECODED OUTPUTS

ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

MCS-80/85

FUNCTIONAL DESCRIPTION

Decoder

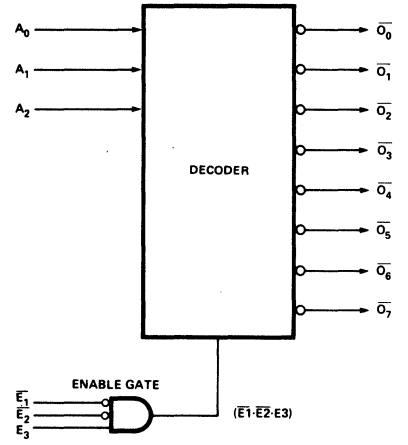
The 8205 contains a one out of eight binary decoder. It accepts a three bit binary code and by gating this input, creates an exclusive output that represents the value of the input code.

For example, if a binary code of 101 was present on the A0, A1 and A2 address input lines, and the device was enabled, an active low signal would appear on the $\overline{05}$ output line. Note that all of the other output pins are sitting at a logic high, thus the decoded output is said to be exclusive. The decoders outputs will follow the truth table shown below in the same manner for all other input variations.

Enable Gate

When using a decoder it is often necessary to gate the outputs with timing or enabling signals so that the exclusive output of the decoded value is synchronous with the overall system.

The 8205 has a built-in function for such gating. The three enable inputs ($\overline{E1}$, $\overline{E2}$, E3) are ANDed together and create a single enable signal for the decoder. The combination of both active "high" and active "low" device enable inputs provides the designer with a powerfully flexible gating function to help reduce package count in his system.



ADDRESS			ENABLE			OUTPUTS							
A_0	A_1	A_2	E_1	E_2	E_3	0	1	2	3	4	5	6	7
L	L	L	L	L	H	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	L
X	X	X	L	L	L	H	H	H	H	H	H	H	H
X	X	X	H	L	L	H	H	H	H	H	H	H	H
X	X	X	L	H	L	H	H	H	H	H	H	H	H
X	X	X	H	H	L	H	H	H	H	H	H	H	H
X	X	X	H	L	H	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H	H

APPLICATIONS OF THE 8205

The 8205 can be used in a wide variety of applications in microcomputer systems. I/O ports can be decoded from the address bus, chip select signals can be generated to select memory devices and the type of machine state such as in 8008 systems can be derived from a simple decoding of the state lines (S0, S1, S2) of the 8008 CPU.

I/O Port Decoder

Shown in the figure below is a typical application of the 8205. Address input lines are decoded by a group of 8205s (3). Each input has a binary weight. For example, A0 is assigned a value of 1 and is the LSB; A4 is assigned a value of 16 and is the MSB. By connecting them to the decoders as shown, an active low signal that is exclusive in nature and represents the value of the input address lines, is available at the outputs of the 8205s.

This circuit can be used to generate enable signals for I/O ports or any other decoder related application.

Note that no external gating is required to decode up to 24 exclusive devices and that a simple addition of an inverter or two will allow expansion to even larger decoder networks.

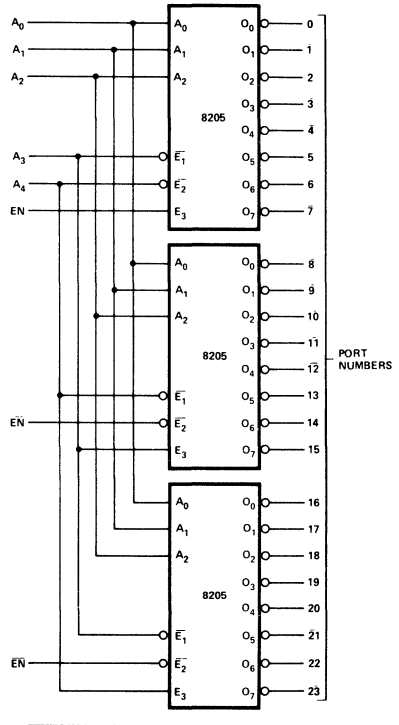
Chip Select Decoder

Using a very similar circuit to the I/O port decoder, an array of 8205s can be used to create a simple interface to a 24K memory system.

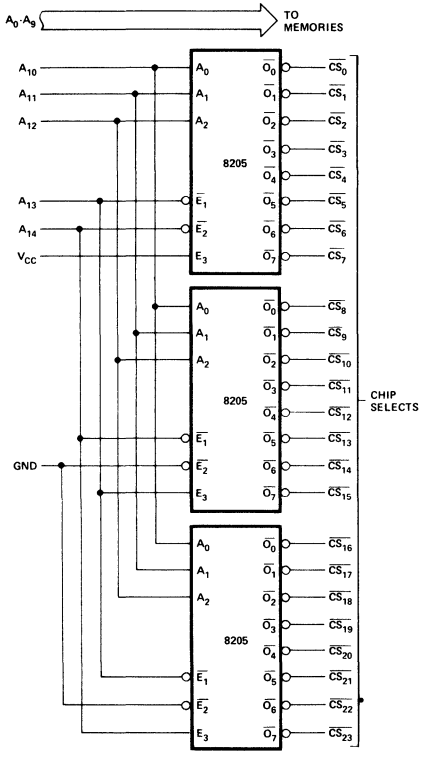
The memory devices used can be either ROM or RAM and are 1K in storage capacity. 8308s and 8102s are the devices typically used for this application. This type of memory device has ten (10) address inputs and an active "low" chip select ($\overline{CS}$). The lower order address bits A0-A9 which come from the microprocessor are "bussed" to all memory elements and the chip select to enable a specific device or group of devices comes from the array of 8205s. The output of the 8205 is active low so it is directly compatible with the memory components.

Basic operation is that the CPU issues an address to identify a specific memory location in which it wishes to "write" or "read" data. The most significant address bits A10-A14 are decoded by the array of 8205s and an exclusive, active low, chip select is generated that enables a specific memory device. The least significant address bits A0-A9 identify a specific location within the selected device. Thus, all addresses throughout the entire memory array are exclusive in nature and are non-redundant.

This technique can be expanded almost indefinitely to support even larger systems with the addition of a few inverters and an extra decoder (8205).



I/O Port Decoder



24K Memory Interface

Logic Element Example

Probably the most overlooked application of the 8205 is that of a general purpose logic element. Using the "on-chip" enabling gate, the 8205 can be configured to gate its decoded outputs with system timing signals and generate strobes that can be directly connected to latches, flip-flops and one-shots that are used throughout the system.

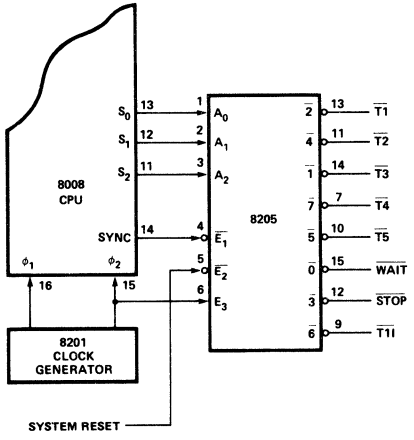
An excellent example of such an application is the "state decoder" in an 8008 CPU based system. The 8008 CPU issues three bits of information (S0, S1, S2) that indicate the nature of the data on the Data Bus during each machine state. Decoding of these signals is vital to generate strobes that can load the address latches, control bus discipline and general machine functions.

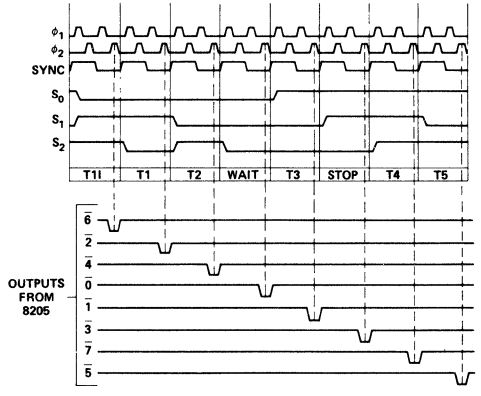
In the figure below a circuit is shown using the 8205 as the "state decoder" for an 8008 CPU that not only decodes the S0, S1, S2 outputs but gates these signals with the clock (phase 2) and the SYNC output of the 8008 CPU. The $\overline{T1}$ and $\overline{T2}$ decoded strobes can connect directly to devices like 8212s for latching the address information. The other decoded strobes can be used to generate signals to control the system data bus, memory timing functions and interrupt structure. RESET is connected to the enable gate so that strobes are not generated during system reset, eliminating accidental loading.

The power of such a circuit becomes evident when a single decoded strobe is logically broken down. Consider $\overline{T1}$ output, the boolean equation for it would be:

$$\overline{T1} = (\overline{S0} \cdot S1 \cdot \overline{S2}) \cdot (\overline{SYNC} \cdot \text{Phase } 2 \cdot \overline{\text{Reset}})$$

A six input NAND gate plus a few inverters would be needed to implement this function. The seven remaining outputs would need a similar circuit to duplicate their function, obviously a substantial savings in components can be achieved when using such a technique.





State Control Coding

S_0	S_1	S_2	STATE
0	1	0	T1
0	1	1	T1I
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOP
1	1	1	T4
1	0	1	T5

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias:	Ceramic	−65°C to +125°C
	Plastic	−65°C to +75°C
Storage Temperature		−65°C to +160°C
All Output or Supply Voltages		−0.5 to +7 Volts
All Input Voltages		−1.0 to +5.5 Volts
Output Currents		125 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

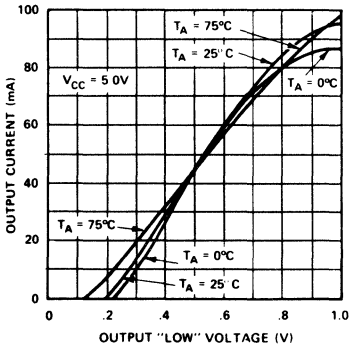
D.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = 5.0V ±5%

8205

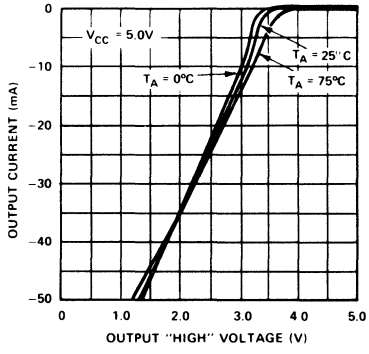
SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	TEST CONDITIONS
I_F	INPUT LOAD CURRENT		−0.25	mA	V_{CC} = 5.25V, V_F = 0.45V
I_R	INPUT LEAKAGE CURRENT		10	μA	V_{CC} = 5.25V, V_R = 5.25V
V_C	INPUT FORWARD CLAMP VOLTAGE		−1.0	V	V_{CC} = 4.75V, I_C = −5.0 mA
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	V_{CC} = 4.75V, I_{OL} = 10.0 mA
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	V_{CC} = 4.75V, I_{OH} = −1.5 mA
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	V_{CC} = 5.0V
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	V_{CC} = 5.0V
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	−40	−120	mA	V_{CC} = 5.0V, V_{OUT} = 0V
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	V_{CC} = 5.0V, I_{OX} = 40 mA
I_{CC}	POWER SUPPLY CURRENT		70	mA	V_{CC} = 5.25V

TYPICAL CHARACTERISTICS

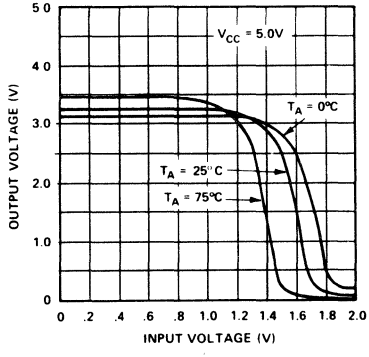
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



DATA TRANSFER FUNCTION



8205 SWITCHING CHARACTERISTICS

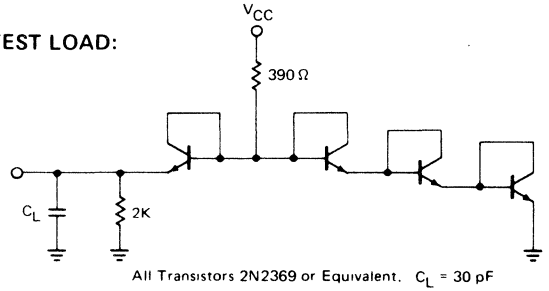
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec between 1V and 2V

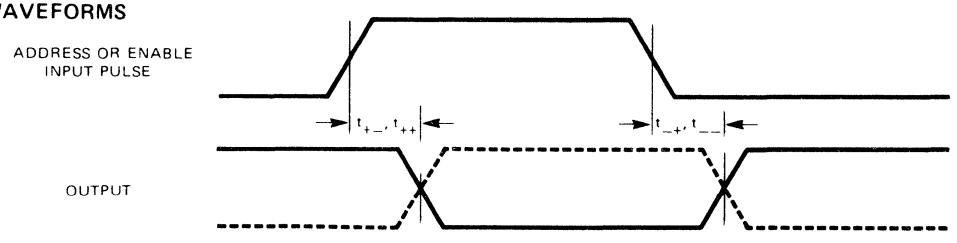
Measurements are made at 1.5V

TEST LOAD:



All Transistors 2N2369 or Equivalent. C_L = 30 pF

TEST WAVEFORMS



A.C. CHARACTERISTICS T_A = 0°C to +75°C, V_{CC} = 5.0V ±5% unless otherwise specified.

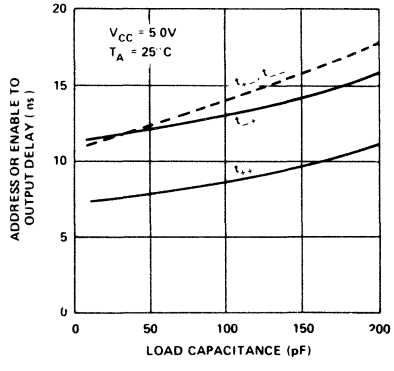
SYMBOL	PARAMETER		MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY		18	ns	
t_{-+}			18	ns	
t_{+-}			18	ns	
t_{--}			18	ns	
C_{IN} [1]	INPUT CAPACITANCE	P8205	4(typ.)	pF	f = 1 MHz, V_{CC} = 0V
		C8205	5(typ.)	pF	V_{BIAS} = 2.0V, T_A = 25°C

1. This parameter is periodically sampled and is not 100% tested.

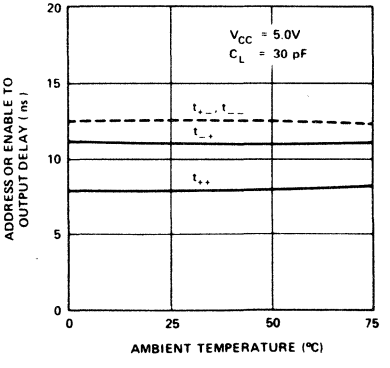
MCS-80/85

TYPICAL CHARACTERISTICS

ADDRESS OR ENABLE TO OUTPUT DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT DELAY VS. AMBIENT TEMPERATURE



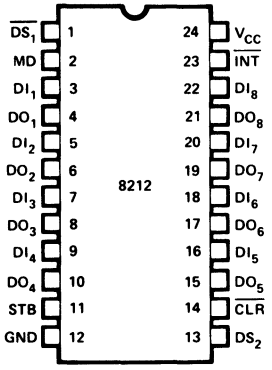
8212
8-BIT INPUT/OUTPUT PORT

- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current — .25mA Max.**
- **Three State Outputs**
- **Outputs Sink 15mA**
- **3.65V Output High Voltage for Direct Interface to 8008, 8080A, or 8085A CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches and Multiplexers in Microcomputer Systems**
- **Reduces System Package Count**

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

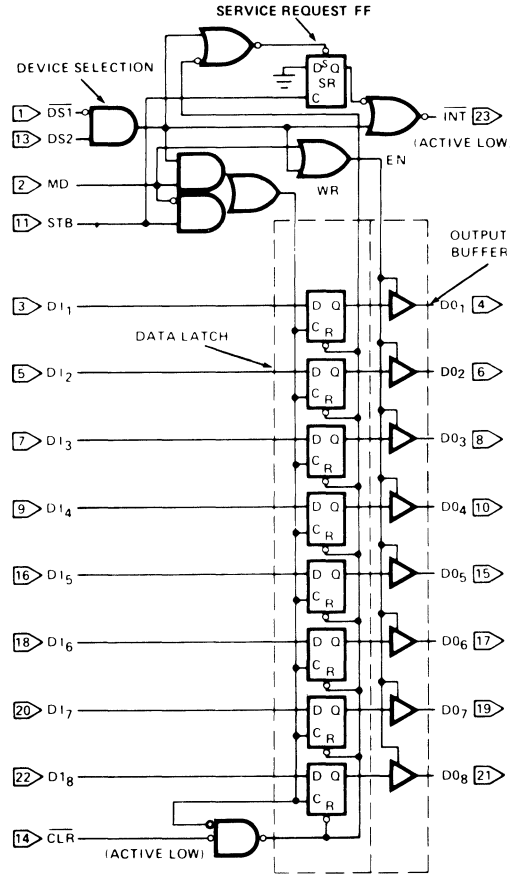
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



MCS-80/85

FUNCTIONAL DESCRIPTION

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The latched data is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

The high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS1}$, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

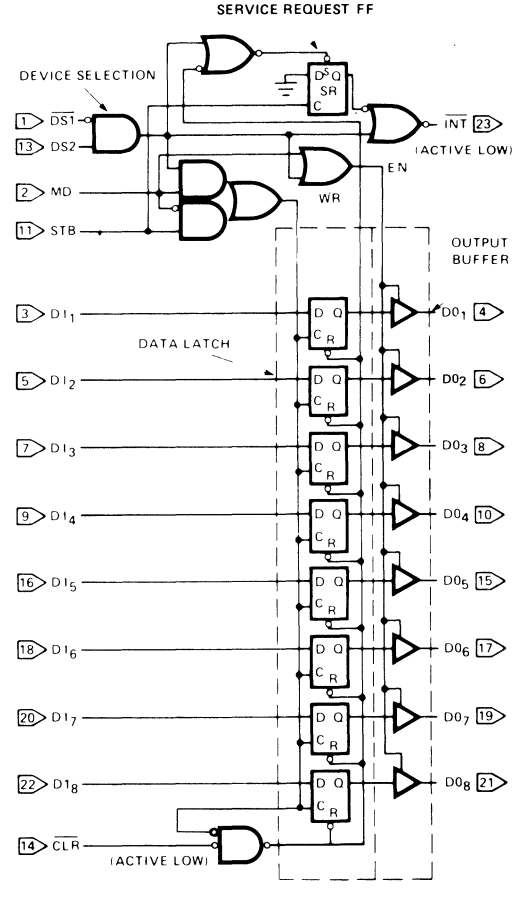
This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS1} \cdot DS2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.



STB	MD	($DS_1 \cdot DS_2$)	DATA OUT EQUALS
0	0	0	3 STATE
1	0	0	3 STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ – RESETS DATA LATCH
SETS SR FLIP-FLOP
(NO EFFECT ON OUTPUT BUFFER)

CLR	($\overline{DS_1} \cdot DS_2$)	STB	*SR	INT
0	0	0	1	1
0	1	0	1	0
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↓	1	0

*INTERNAL SR FLIP-FLOP

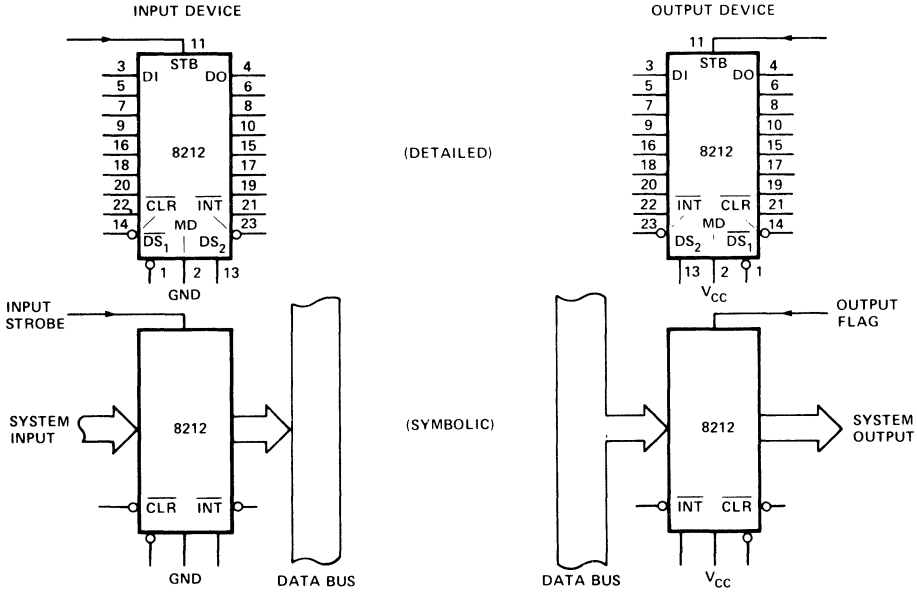
Applications of the 8212 — For Microcomputer Systems

I Basic Schematic Symbol
II Gated Buffer
III Bi-Directional Bus Driver
IV Interrupting Input Port
V Interrupt Instruction Port
VI Output Port
VII 8080A Status Latch
VIII 8085A Address Latch

1. Basic Schematic Symbols

Two examples of ways to draw the 8212 on system schematics — (1) the top being the detailed view showing pin numbers, and (2) the bottom being the symbolic view showing the system input or output as a system bus (bus containing 8 parallel lines). The output to the data bus is symbolic in referencing 8 parallel lines.

BASIC SCHEMATIC SYMBOLS



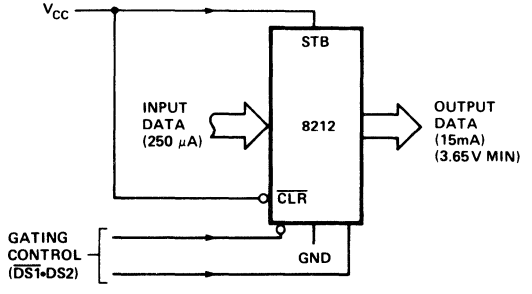
II. Gated Buffer (3-State)

The simplest use of the 8212 is that of a gated buffer. By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS1}$ and DS2.

When the device selection logic is false, the outputs are 3-state.

When the device selection logic is true, the input data from the system is directly transferred to the output. The input data load is 250 micro amps. The output data can sink 15 milli amps. The minimum high output is 3.65 volts.

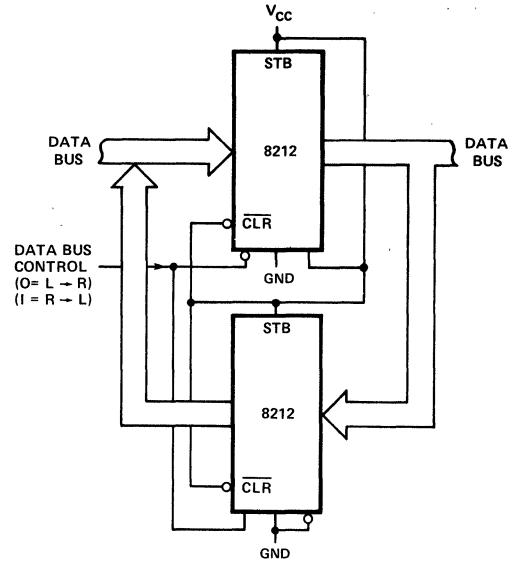
GATED BUFFER



III. Bi-Directional Bus Driver

A pair of 8212's wired (back-to-back) can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS1}$ on the first 8212 and to DS2 on the second. One device is active, and acting as a straight through buffer the other is in 3-state mode. This is a very useful circuit in small system design.

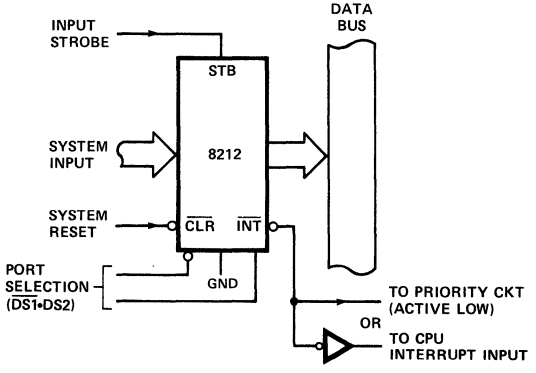
BI-DIRECTIONAL BUS DRIVER



IV. Interrupting Input Port

This use of an 8212 is that of a system input port that accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true — enabling the system input data onto the data bus.

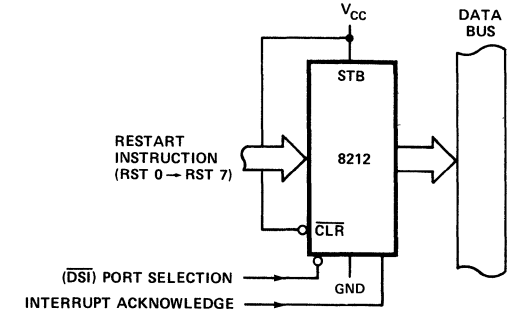
INTERRUPTING INPUT PORT



V. Interrupt Instruction Port

The 8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).

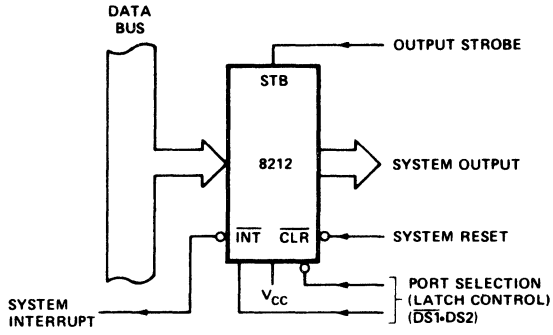
INTERRUPT INSTRUCTION PORT



VI. Output Port (With Hand-Shaking)

The 8212 can be used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of data. The selection of the port comes from the device selection logic.($\overline{DS1} \cdot DS2$)

OUTPUT PORT (WITH HAND-SHAKING)

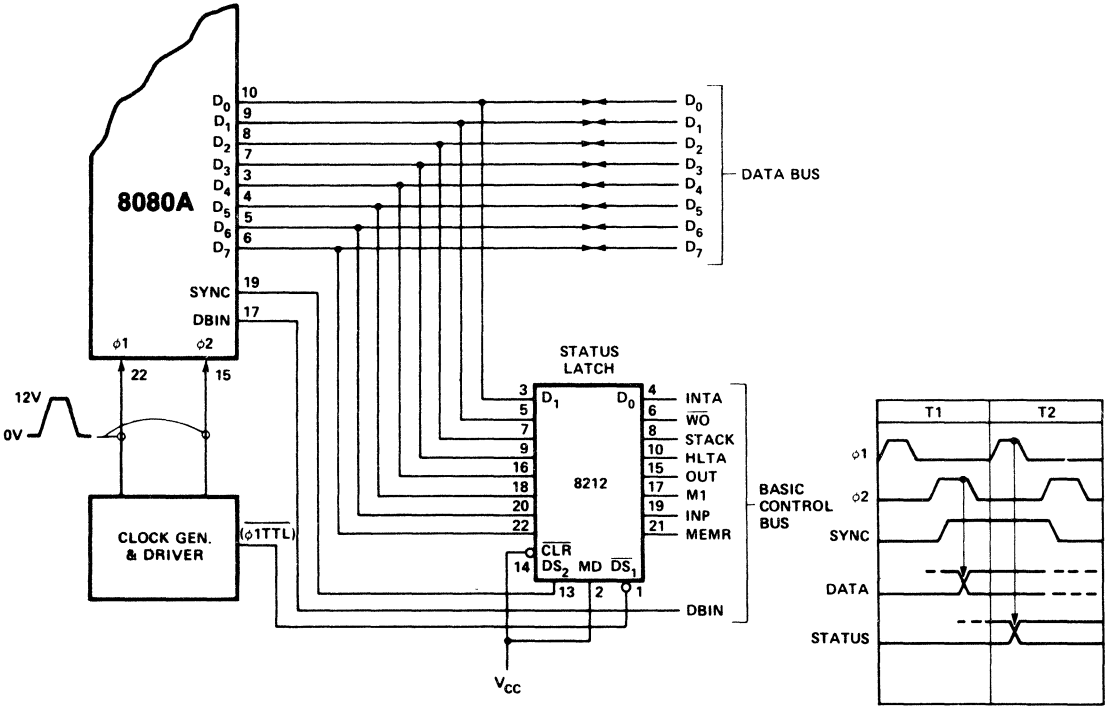


VII. 8080A Status Latch

Here the 8212 is used as the status latch for an 8080A microcomputer system. The input to the 8212 latch is directly from the 8080A data bus. Timing shows that when the SYNC signal is true, which is connected to the DS2 input and the phase 1 signal is true, which is a TTL level coming from the clock generator; then, the status data will be latched into the 8212.

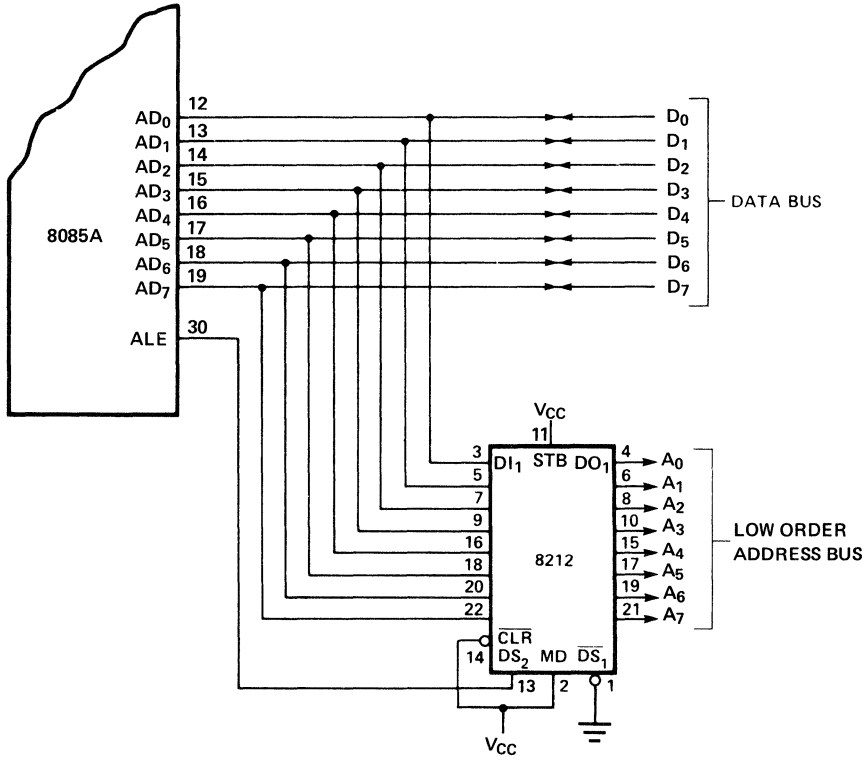
Note: The mode signal is tied high so that the output on the latch is active and enabled all the time.

It is shown that the two areas of concern are the bi-directional data bus of the microprocessor and the control bus.



VIII. 8085A Low-Order Address Latch

The 8085A microprocessor uses a multiplexed address/data bus that contains the low order 8-bits of address information during the first part of a machine cycle. The same bus contains data at a later time in the cycle. An address latch enable (ALE) signal is provided by the 8085A to be used by the 8212 to latch the address so that it may be available through the whole machine cycle. Note: In this configuration, the MODE input is tied high, keeping the 8212's output buffers turned on at all times.



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias Plastic ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
All Output or Supply Voltages ..... -0.5 to +7 Volts
All Input Voltages ..... -1.0 to 5.5 Volts
Output Currents 100mA

*COMMENT

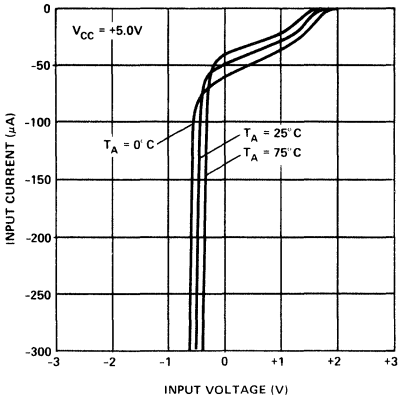
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $T_A = 0°C$ to $+75°C$, $V_{CC} = +5V \pm 5\%$

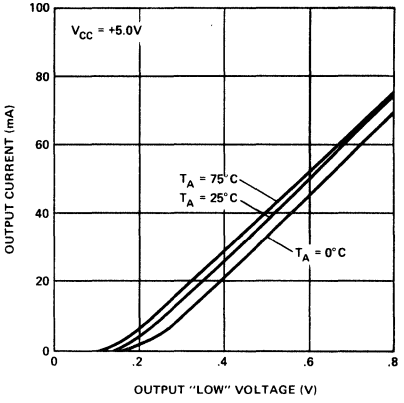
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current, ACK, DS_2, CR, DI_1-DI_8 Inputs			-.25	mA	$V_F = .45V$
I_F	Input Load Current MD Input			-.75	mA	$V_F = .45V$
I_F	Input Load Current DS_1 Input			-1.0	mA	$V_F = .45V$
I_R	Input Leakage Current, ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	$V_R \leq V_{CC}$
I_R	Input Leakage Current MO Input			30	μA	$V_R \leq V_{CC}$
I_R	Input Leakage Current DS_1 Input			40	μA	$V_R \leq V_{CC}$
V_C	Input Forward Voltage Clamp			-1	V	$I_C = -5mA$
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	$I_{OL} = 15mA$
V_{OH}	Output "High" Voltage	3.65	4.0		V	$I_{OH} = -1mA$
I_{SC}	Short Circuit Output Current	-15		-75	mA	$V_O = 0V$, $V_{CC} = 5V$
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	$V_O = .45V/5.25V$
I_{CC}	Power Supply Current		90	130	mA	

TYPICAL CHARACTERISTICS

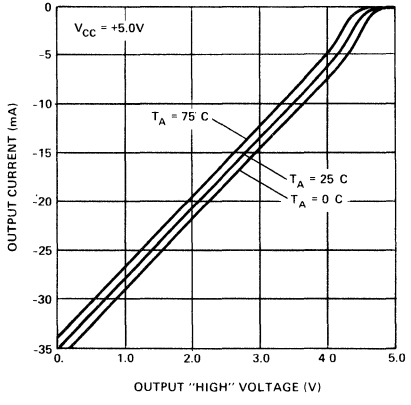
INPUT CURRENT VS. INPUT VOLTAGE



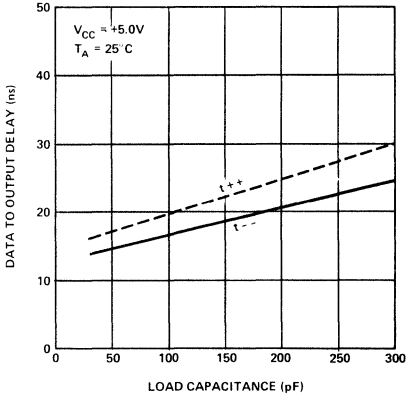
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



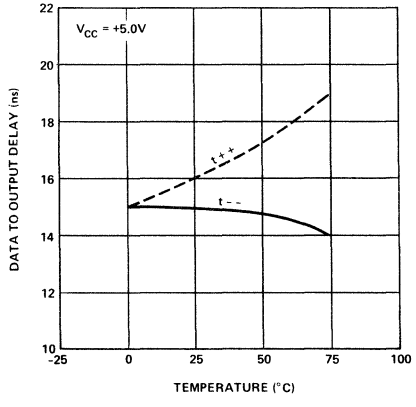
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



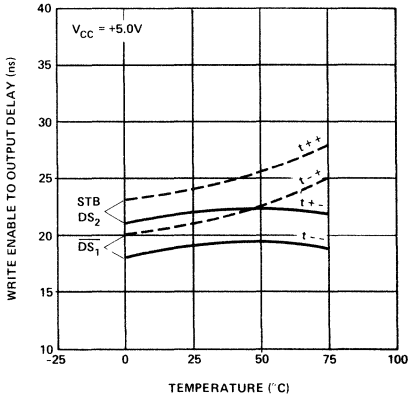
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA TO OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{PW}	Pulse Width	30			ns	
t_{PD}	Data to Output Delay			30	ns	Note 1
t_{WE}	Write Enable to Output Delay			40	ns	Note 1
t_{SET}	Data Set Up Time	15			ns	
t_H	Data Hold Time	20			ns	
t_R	Reset to Output Delay			40	ns	Note 1
t_S	Set to Output Delay			30	ns	Note 1
t_E	Output Enable/Disable Time			45	ns	Note 1
t_C	Clear to Output Delay			55	ns	Note 1

CAPACITANCE* $F = 1MHz$, $V_{BIAS} = 2.5V$, $V_{CC} = +5V$, $T_A = 25°C$

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	DS_1 MD Input Capacitance	9pF	12pF
C_{IN}	DS_2, CK, ACK, DI_1-DI_8 Input Capacitance	5pF	9pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8pF	12pF

*This parameter is sampled and not 100% tested.

SWITCHING CHARACTERISTICS

Conditions of Test

Input Pulse Amplitude = 2.5V
Input Rise and Fall Times 5ns
Between 1V and 2V Measurements made at 1.5V
with 15mA and 30pF Test Load

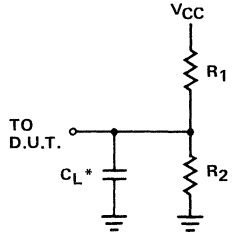
Note 1:

Test	C_L*	R_1	R_2
t_{PD}, t_{WE}, t_R, t_S, t_C	30pF	300Ω	600Ω
t_E, ENABLE↑	30pF	10KΩ	1KΩ
t_E, ENABLE↓	30pF	300Ω	600Ω
t_E, DISABLE↑	5pF	300Ω	600Ω
t_E, DISABLE↓	5pF	10KΩ	1KΩ

*Includes probe and jig capacitance.

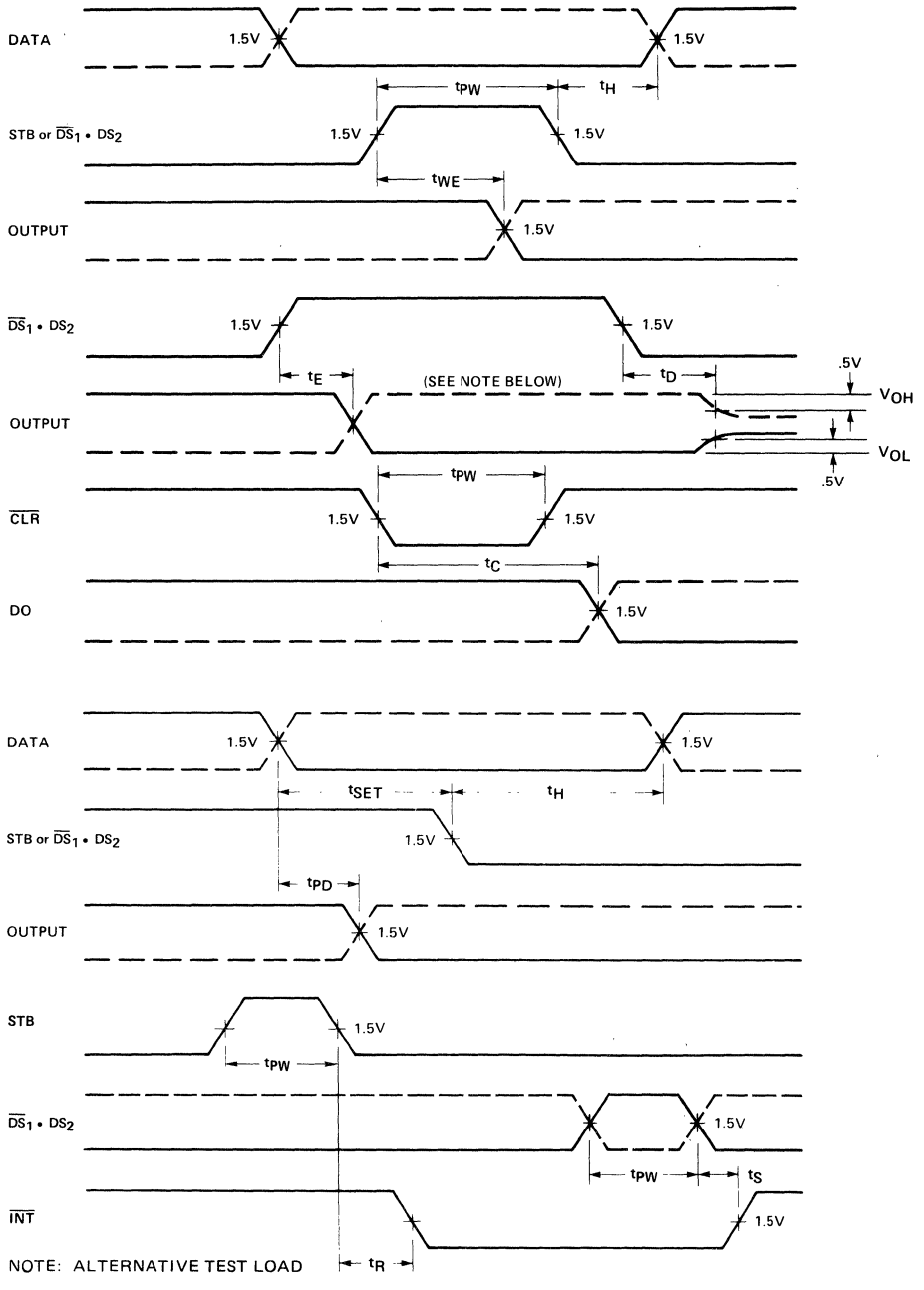
Test Load

15mA & 30pF



*INCLUDING JIG & PROBE CAPACITANCE

TIMING DIAGRAM



8214
PRIORITY INTERRUPT CONTROL UNIT

- **8 Priority Levels**
- **Current Status Register**
- **Priority Comparator**
- **Fully Expandable**
- **High Performance (50 ns)**
- **24-Pin Dual In-Line Package**

The Intel® 8214 is an 8-level priority interrupt control unit (PICU) designed to simplify interrupt-driven microcomputer systems.

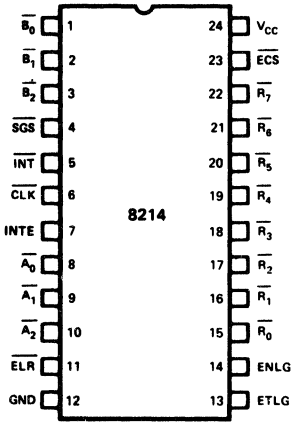
The PICU can accept 8 requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector information to identify the service routine.

The 8214 is fully expandable by the use of open collector interrupt output vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt-driven microcomputer systems.

*Note: The specifications for the 3214 are identical with those for the 8214.

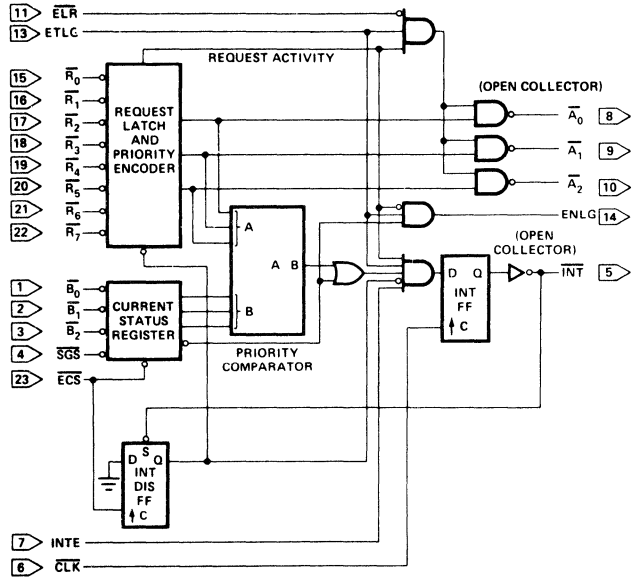
PIN CONFIGURATION



PIN NAMES

INPUTS		
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)	
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS	
$\overline{SGS}$	STATUS GROUP SELECT	
$\overline{ECS}$	ENABLE CURRENT STATUS	
INTE	INTERRUPT ENABLE	
$\overline{CLK}$	CLOCK (INT F-F)	
$\overline{ELR}$	ENABLE LEVEL READ	
ETLG	ENABLE THIS LEVEL GROUP	
OUTPUTS:		
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS	OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT. LOW)	OPEN COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP	

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 75°C
Storage Temperature . . . . . -65°C to +160°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5%.

Symbol	Parameter		Limits			Unit	Conditions
			Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage (all inputs)				-1.0	V	I_C=-5mA
I_F	Input Forward Current:	ETLG input		-.15	-0.5	mA	V_F=0.45V
		all other inputs		-.08	-0.25	mA	
I_R	Input Reverse Current:	ETLG input			80	μA	V_R=5.25V
		all other inputs			40	μA	
V_{IL}	Input LOW Voltage:	all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage:	all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current			90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I_{OL}=15mA
V_{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I_{OH}=-1mA
I_{OS}	Short Circuit Output Current:	ENLG output	-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
I_{CEX}	Output Leakage Current:	$\overline{INT}$ and $\overline{A_0}$-$\overline{A_2}$			100	μA	V_{CEX}=5.25V

NOTES:
1. Typical values are for T_A = 25° C, V_{CC} = 5.0V.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
t_{CY}	$\overline{CLK}$ Cycle Time	80	50		ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	80	25		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	75	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{CLK}$	70	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{CLK}$	90	55		ns
t_{RCH}[3]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	25	ns
t_{RIS}[4]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$-$\overline{R_7}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		100	120	ns
t_{ETA}	ETLG to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{ECS}$	15	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{ECS}$	15	10		ns
t_{REN}	$\overline{R_0}$-$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	25	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	90	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

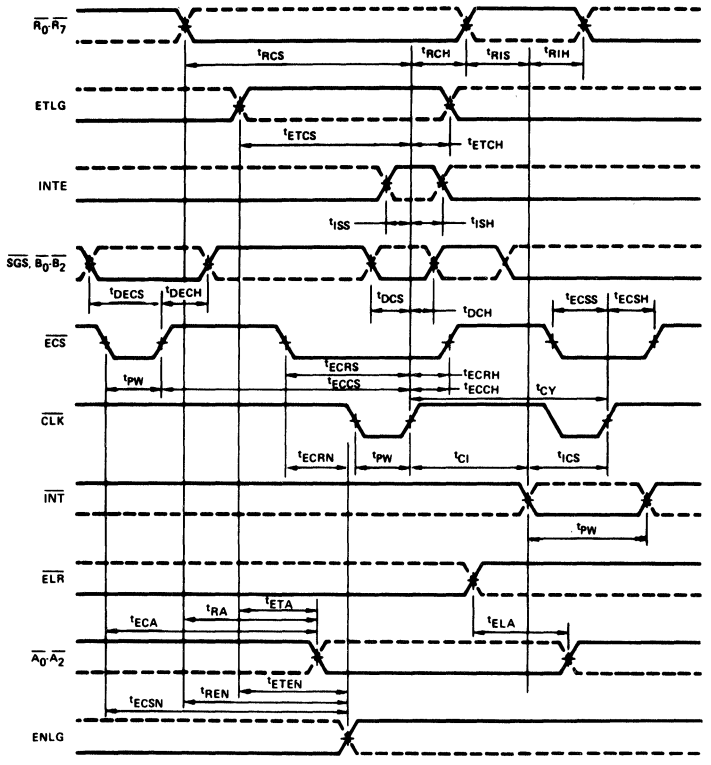
CAPACITANCE[5]

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max	
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		7	12	pF

Test Conditions: $V_{BIAS} = 2.5V$, $V_{CC} = 5V$, $T_A = 25°C$, f = 1 MHz

NOTE 5. This parameter is periodically sampled and not 100% tested.

WAVEFORMS



NOTES:

(1) Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.

(2) Required for proper operation if ISE is enabled during next clock pulse.

(3) These times are not required for proper operation but for desired change in interrupt flip-flop.

(4) Required for new request or status to be properly loaded.

Test Conditions

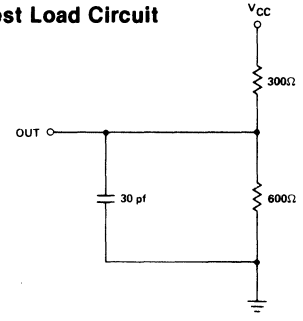
Input pulse amplitude: 2.5 volts.

Input rise and fall times: 5 ns between 1 and 2 volts.

Output loading of 15 mA and 30 pf.

Speed measurements taken at the 1.5V levels.

Test Load Circuit



MCS-80/85

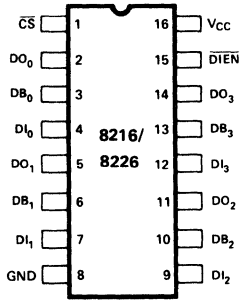
8216/8226
4-BIT PARALLEL BIDIRECTIONAL BUS DRIVER

- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current — 0.25 mA Maximum**
- **High Output Drive Capability for Driving System Bus**
- **3.65V Output High Voltage for Direct Interface to 8080 CPU**
- **3-State Outputs**
- **Reduces System Package Count**

The 8216/8226 is a 4-bit bidirectional bus driver/receiver. All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50 mA I_{OL} capability. A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

*Note: The specifications for the 3216/3226 are identical with those for the 8216/8226.

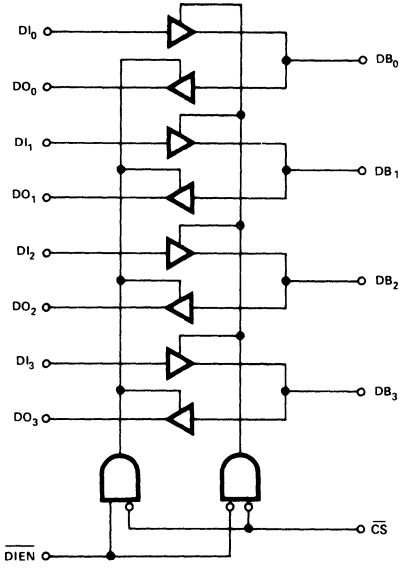
PIN CONFIGURATION



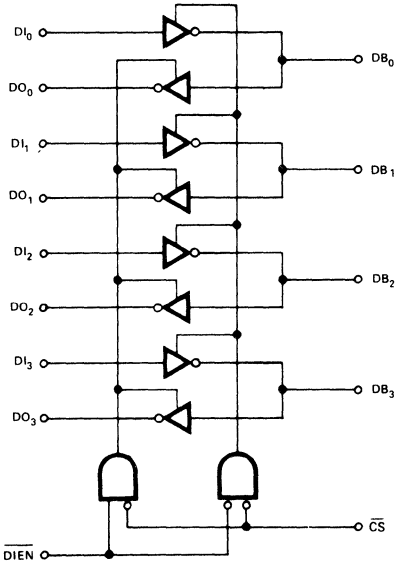
PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM
8216



LOGIC DIAGRAM
8226



MCS-80/85

FUNCTIONAL DESCRIPTION

Microprocessors like the 8080 are MOS devices and are generally capable of driving a single TTL load. The same is true for MOS memory devices. While this type of drive is sufficient in small systems with few components, quite often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The 8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bidirectional Driver

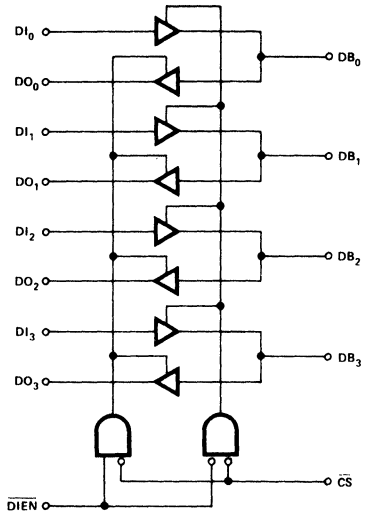
Each buffered line of the four bit driver consists of two separate buffers that are tri-state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is direct TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080 Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080 and 8008 CPUs is achieved with an adequate amount of noise immunity (350mV worst case).

Control Gating $\overline{DIEN}$, $\overline{CS}$

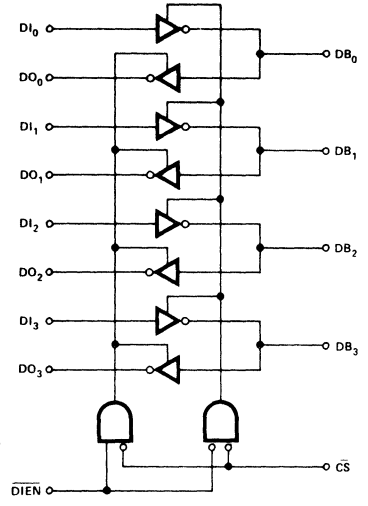
The $\overline{CS}$ input is actually a device select. When it is "high" the output drivers are all forced to their high-impedance state. When it is at "zero" the device is selected (enabled) and the direction of the data flow is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the direction of data flow (see Figure 1) for complete truth table. This direction control is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

The 8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.



(a) 8216

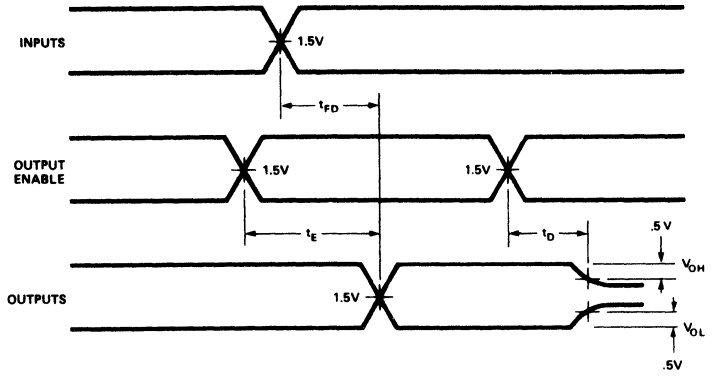


(b) 8226

$\overline{DIEN}$	$\overline{CS}$	
0	0	DI → DB
1	0	DB → DO
0	1	HIGH IMPEDANCE
1	1	

Figure 1. 8216/8226 Logic Diagrams

WAVEFORMS



A.C. CHARACTERISTICS

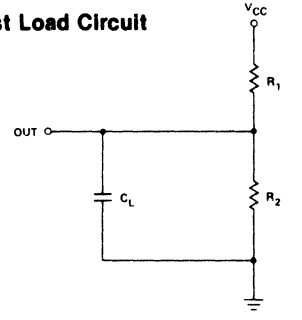
T_A = 0°C to +70°C, V_{CC} = +5V ±5%

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Conditions
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	C_L=30pF, R_1=300Ω R_2=600Ω
T_{PD2}	Input to Output Delay DB Outputs					
	8216		19	30	ns	C_L=300pF, R_1=90Ω
	8226		16	25	ns	R_2 = 180Ω
T_E	Output Enable Time					
	8216		42	65	ns	(Note 2)
	8226		36	54	ns	(Note 3)
T_D	Output Disable Time		16	35	ns	(Note 4)

Test Conditions:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

Test Load Circuit



CAPACITANCE[5]

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		4	8	pF
C_{OUT1}	Output Capacitance		6	10	pF
C_{OUT2}	Output Capacitance		13	18	pF

Test Conditions V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz.

NOTES:
1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. DO Outputs, C_L = 30pF, R_1 = 300/10 KΩ, R_2 = 180/1KΩ; DB Outputs, C_L = 300pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
3. DO Outputs, C_L = 30pF, R_1 = 300/10 KΩ, R_2 = 600/1K; DB Outputs, C_L = 300pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
4. DO Outputs, C_L = 5pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ; DB Outputs, C_L = 5pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.
5. This parameter is periodically sampled and not 100% tested.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 125 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC}=+5V ±5%

Symbol	Parameter		Limits Min.	Typ.	Max.	Unit	Conditions
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$			-0.15	-.5	mA	V_F = 0.45
I_{F2}	Input Load Current All Other Inputs			-0.08	-.25	mA	V_F = 0.45
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$				80	μA	V_R = 5.25V
I_{R2}	Input Leakage Current DI Inputs				40	μA	V_R = 5.25V
V_C	Input Forward Voltage Clamp				-1	V	I_C = -5mA
V_{IL}	Input "Low" Voltage				.95	V	
V_{IH}	Input "High" Voltage		2.0			V	
$\|I_O\|$	Output Leakage Current (3-State)	DO DB			20 100	μA	V_O = 0.45V/5.25V
I_{CC}	Power Supply Current	8216		95	130	mA	
		8226		85	120	mA	
V_{OL1}	Output "Low" Voltage			0.3	.45	V	DO Outputs I_{OL}=15mA DB Outputs I_{OL}=25mA
V_{OL2}	Output "Low" Voltage	8216		0.5	.6	V	DB Outputs I_{OL}=55mA
		8226		0.5	.6	V	DB Outputs I_{OL}=50mA
V_{OH1}	Output "High" Voltage		3.65	4.0		V	DO Outputs I_{OH} = -1mA
V_{OH2}	Output "High" Voltage		2.4	3.0		V	DB Outputs I_{OH} = -10mA
I_{OS}	Output Short Circuit Current		-15 -30	-35 -75	-65 -120	mA mA	DO Outputs $V_O \cong 0V$, DB Outputs V_{CC}=5.0V

NOTE: Typical values are for T_A = 25°C, V_{CC} = 5.0V.

APPLICATIONS OF THE 8216/8226

8080 Data Bus Buffer

The 8080 CPU Data Bus is capable of driving a single TTL load and is more than adequate for small, single board systems. When expanding such a system to more than one board to increase I/O or Memory size, it is necessary to provide a buffer. The 8216/8226 is a device that is exactly fitted to this application.

Shown in Figure 2 are a pair of 8216/8226 connected directly to the 8080 Data Bus and associated control signals. The buffer is bi-directional in nature and serves to isolate the CPU data bus.

On the system side, the DB lines interface with standard semiconductor I/O and Memory components and are completely TTL compatible. The DB lines also provide a high drive capability (50mA) so that an extremely large system can be dirven along with possible bus termination networks.

On the 8080 side the DI and DO lines are tied together and are directly connected to the 8080 Data Bus for bi-directional operation. The DO outputs of the 8216/8226 have a high voltage output capability of 3.65 volts which allows direct connection to the 8080 whose minimum input voltage is 3.3 volts. It also gives a very adequate noise margin of 350mV (worst case).

The $\overline{DIEN}$ inputs to 8216/8226 is connected directly to the 8080. $\overline{DIEN}$ is tied to DBIN so that proper bus flow is maintained, and $\overline{CS}$ is tied to $\overline{BUSEN}$ so that the system side Data Bus will be 3-stated when a Hold request has been acknowledged during a DMA activity.

Memory and I/O Interface to a Bidirectional Bus

In large microcomputer systems it is often necessary to provide Memory and I/O with their own buffers and at the same time maintain a direct, common interface to a bi-directional Data Bus. The 8216/8226 has separated data in and data out lines on one side and a common bi-directional set on the other to accomodate such a function.

Shown in Figure 3 is an example of how the 8216/8226 is used in this type of application.

The interface to Memory is simple and direct. The memories used are typically Intel® 8102, 8102A, 8101 or 8107B-4 and have separate data inputs and outputs. The DI and DO lines of the 8216/8226 tie to them directly and under control of the $\overline{MEMR}$ signal, which is connected to the $\overline{DIEN}$ input, an interface to the bi-directional Data Bus is maintained.

The interface to I/O is similar to Memory. The I/O devices used are typically Intel® 8255s, and can be used for both input and output ports. The $\overline{I/O\ R}$ signal is connected directly to the $\overline{DIEN}$ input so that proper data flow from the I/O device to the Data Bus is maintained.

The 8216/8226 can be used in a wide variety of other buffering functions in microcomputer systems such as Address Bus Drivers, Drivers to peripheral devices such as printers, and as Drivers for long length cables to other peripherals or systems.

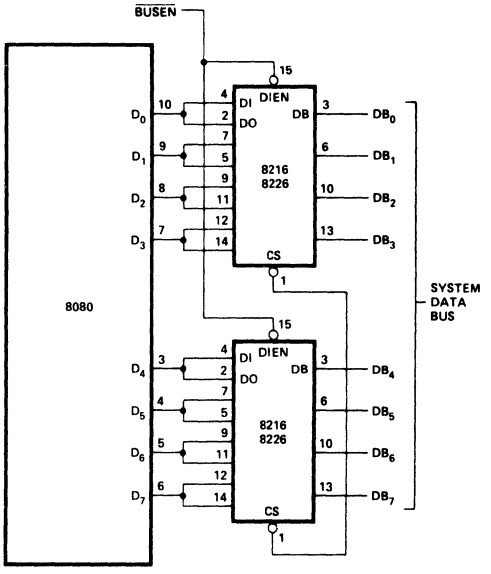


Figure 2. 8080 Data Bus Buffer

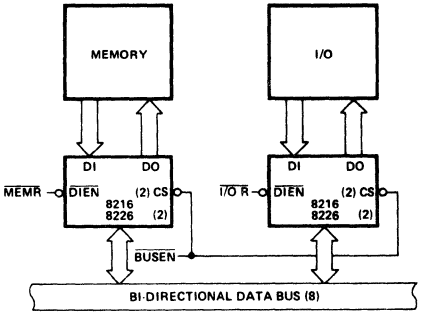


Figure 3. Memory and I/O Interface to a Bidirectional Bus

8085A/8085A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSORS

- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3 μs Instruction Cycle (8085A); 0.8 μs (8085A-2)**
- **On-Chip Clock Generator (with External Crystal, LC or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible interrupt**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64k Bytes of Memory**

The Intel® 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)] while maintaining total system expandability. The 8085A-2 is a faster version of the 8085A.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

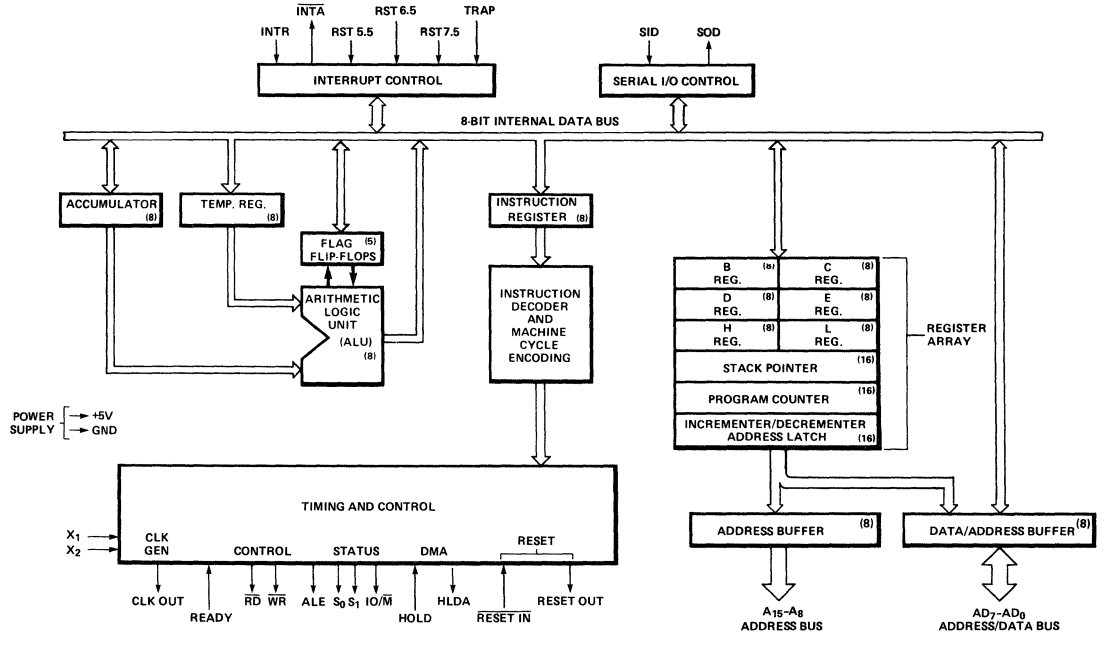


Figure 1. 8085A CPU Functional Block Diagram

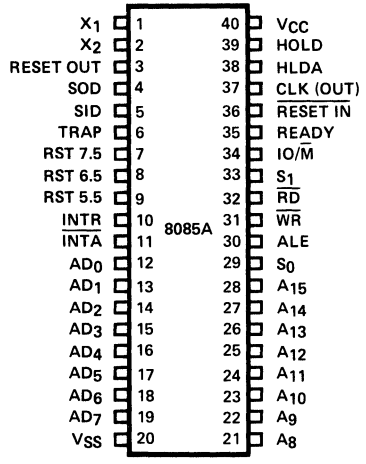


Figure 2. 8085A Pinout Diagram

8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

Symbol	Function
A_8–A_{15} (Output, 3-state)	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7} (Input/Output, 3-state)	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, and IO/$\overline{M}$ (Output)	Machine cycle status: IO/$\overline{M}$ S_1 S_0 Status 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Interrupt Acknowledge * 0 0 Halt * X X Hold * X X Reset * = 3-state (high impedance) X = unspecified
Symbol	**Function**
	S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$,S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$ (Output, 3-state)	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ (Output, 3-state)	WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

8085A FUNCTIONAL PIN DESCRIPTION (Continued)

Symbol	Function
$\overline{\text{INTA}}$ (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{\text{RD}}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5 (Inputs)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.)
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:

(1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

FUNCTIONAL DESCRIPTION

The 8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz (8085A) or 5 MHz (8085A-2), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The cpu (8085A), a RAM/IO (8156), and a ROM or EPROM/IO chip (8355 or 8755A).

The 8085A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC,DE,HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085A provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD, READY, and all Interrupts are synchronized with the processor's internal clock. The 8085A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

INTERRUPT AND SERIAL I/O

The 8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive.*

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. (See Section 2.2.7.) The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the 8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$. (See SIM, Chapter 4.)

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP — highest priority, RST 7.5, RST 6.5, RST 5.5, INTR — lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive.* The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the 8085A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

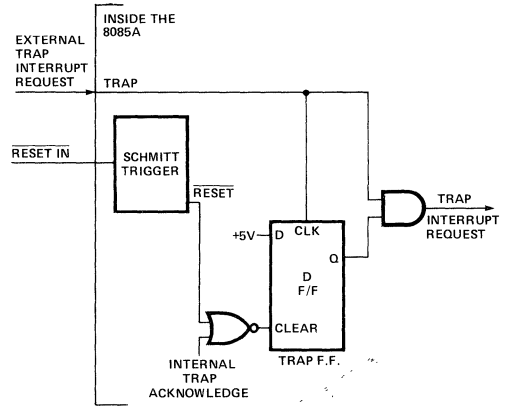


Figure 3. TRAP and $\overline{RESET\ IN}$ Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5–7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled. See the description of the RIM instruction in Chapter 4.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

DRIVING THE X_1 AND X_2 INPUTS

You may drive the clock inputs of the 8085A or 8085A-2 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the 8085A is operated with a 6 MHz crystal (for 3 MHz clock), and the 8085A-2 can be operated with a 10 MHz crystal (for 5 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired
C_L (load capacitance) $\leq$ 30 pf
C_S (shunt capacitance) $\leq$ 7 pf
R_S (equivalent shunt resistance) $\leq$ 75 Ohms
Drive level: 10 mW
Frequency tolerance: $\pm$.005% (suggested)

Note the use of the 20 pf capacitors between X_1, X_2 and ground. These capacitors are required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the 8085A, providing that its frequency tolerance of approximately $\pm$10% is acceptable. The components are chosen from the formula:

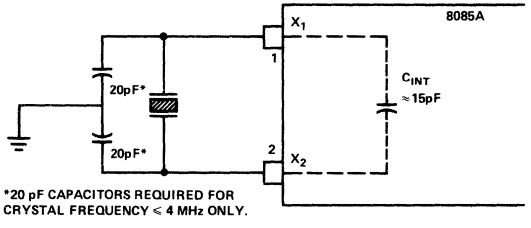
$$f = \frac{1}{2\pi\sqrt{L(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int}, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

An RC circuit may be used as the frequency-determining network for the 8085A if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

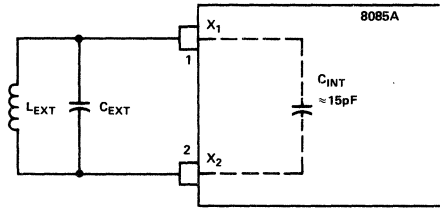
Figure 4 shows the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4 V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 open-circuited (Figue 4D). If the driving frequency is from 6 MHz to 10 MHz, stability of the clock generator will be improved by driving both X_1 and X_2 with a push-pull source (Figure 4E). To prevent self-oscillation of the 8085A, be sure that X_2 is not coupled back to X_1 through the driving circuit.

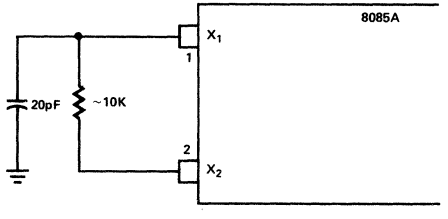


*20 pF CAPACITORS REQUIRED FOR CRYSTAL FREQUENCY ≤ 4 MHz ONLY.

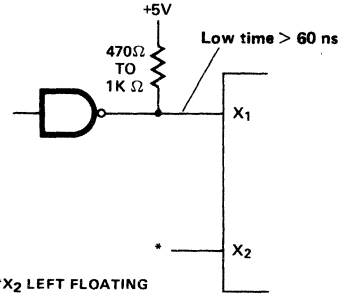
A. Quartz Crystal Clock Driver



B. LC Tuned Circuit Clock Driver

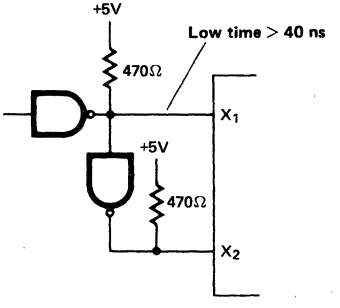


C. RC Circuit Clock Driver



*X_2 LEFT FLOATING

D. 1-6 MHz Input Frequency External Clock Driver Circuit



E. 1-10 MHz Input Frequency External Clock Driver Circuit

Figure 4. Clock Driver Circuits

GENERATING AN 8085A WAIT STATE

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 5 may be used to insert one WAIT state in each 8085A machine cycle

The D flip-flops should be chosen so that
- CLK is rising edge-triggered
- CLEAR is low-level active.

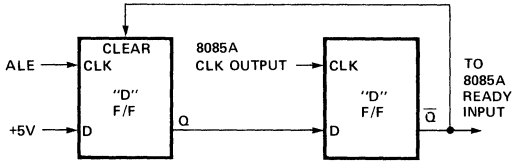


Figure 5. Generation of a Wait State for 8085A CPU

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085A can be used with slow memory. HOLD causes the cpu to relinquish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

The 8085A family includes memory components, which are directly compatible to the 8085A cpu. For example, a system consisting of the three chips, 8085A, 8156, and 8355 will have the following features: .

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 6.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 7 shows the system configuration of Memory Mapped I/O using 8085A.

The 8085A cpu can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 8.

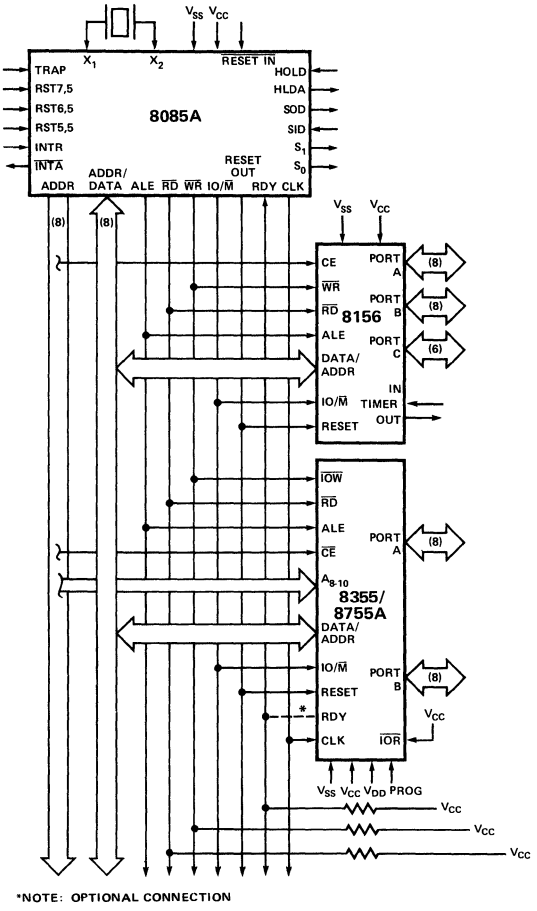


Figure 6. 8085A Minimum System (Standard I/O Technique)

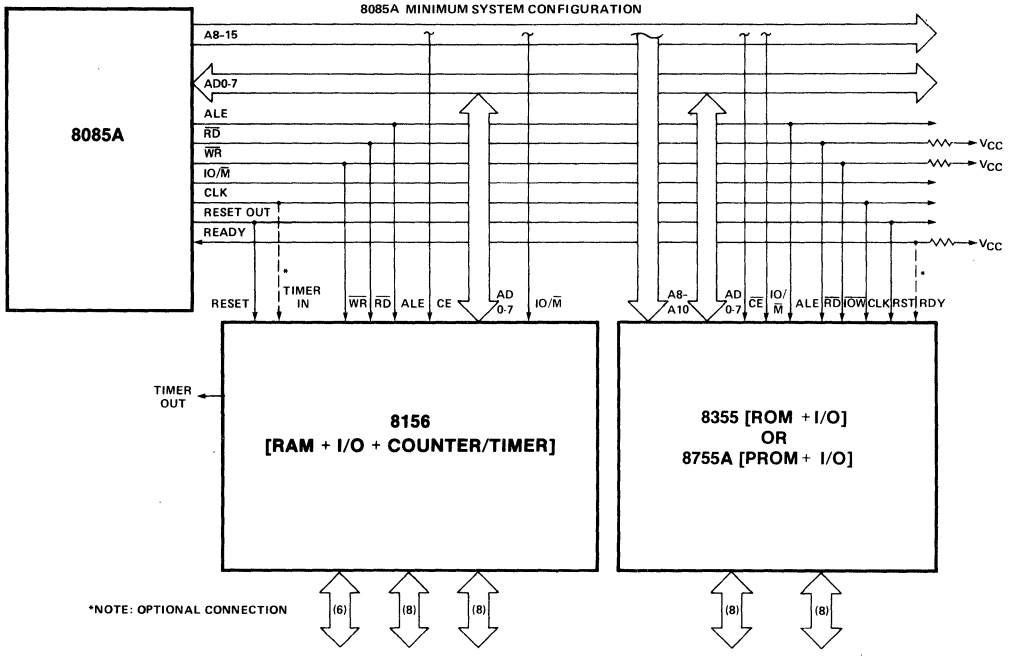


Figure 7. MCS-85™ Minimum System (Memory Mapped I/O)

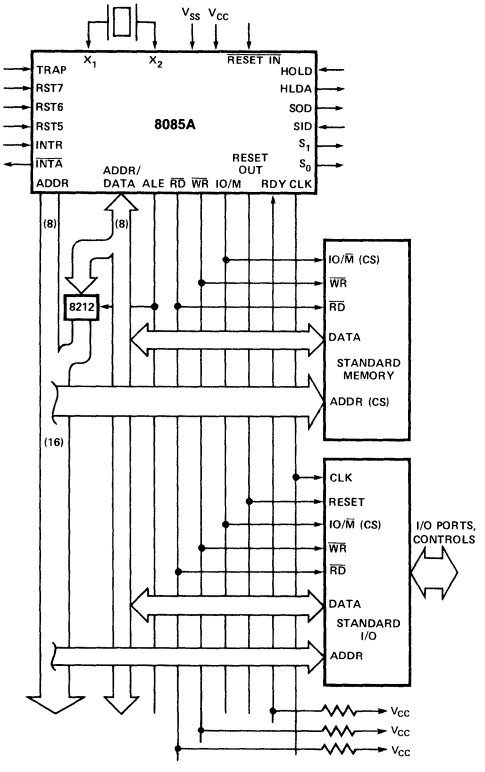


Figure 8. MCS-85™ System (Using Standard Memories)

BASIC SYSTEM TIMING

The 8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 9 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 2.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

TABLE 2. 8085A MACHINE CYCLE CHART

MACHINE CYCLE		STATUS			CONTROL		
		$IO/\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)	0	1	1	0	1	1
MEMORY READ	(MR)	0	1	0	0	1	1
MEMORY WRITE	(MW)	0	0	1	1	0	1
I/O READ	(IOR)	1	1	0	0	1	1
I/O WRITE	(IOW)	1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)	1	1	1	1	1	0
BUS IDLE	(BI): DAD	0	1	0	1	1	1
	ACK OF RST,TRAP	1	1	1	1	1	1
	HALT	TS	0	0	TS	TS	1

TABLE 3. 8085A MACHINE STATE CHART

Machine State	Status & Buses				Control		
	S1,S0	$IO/\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}$,$\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
† IO/M = 1 during T_4-T_6 of INA machine cycle.

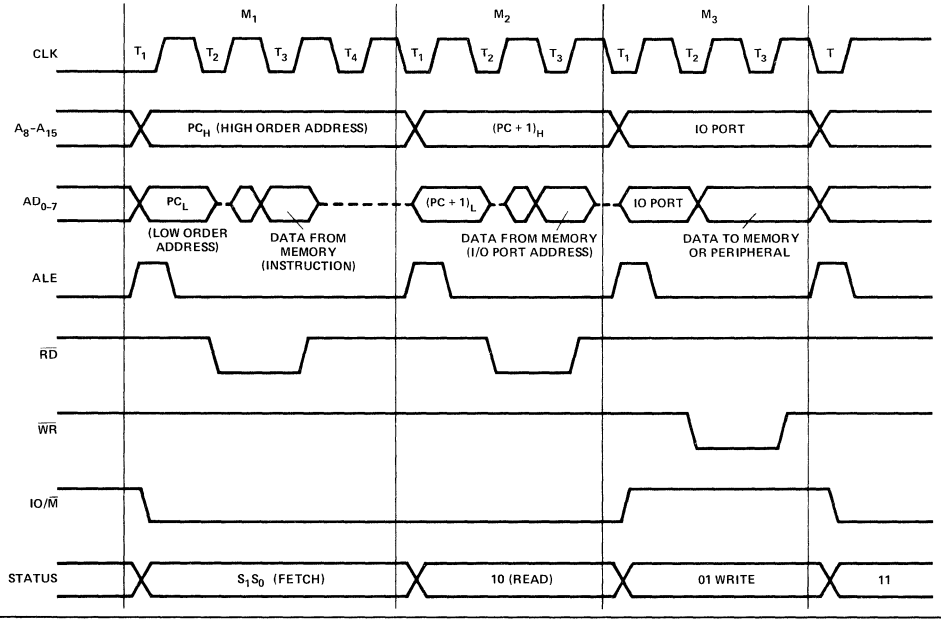


Figure 9. 8085A Basic System Timing

TABLE 4. ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1.5 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 5. D.C. CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{CC}	Power Supply Current		170	mA	
I_{IL}	Input Leakage		±10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \leqslant V_{out} \leqslant V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} +0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

TABLE 6. A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$; $V_{SS} = 0V$

Symbol	Parameter	8085A[2]		8085A-2[2] (Preliminary)		Units
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	ns
t_1	CLK Low Time — Standard 150 pF Loading	80		40		ns
	Lightly Loaded[8]	100				ns
t_2	CLK High Time — Standard 150 pF Loading	120		70		ns
	Lightly Loaded[8]	150				ns
t_r, t_f	CLK Rise and Fall Time		30		30	ns
t_{XKR}	X_1 Rising to CLK Rising	30	120	30	100	ns
t_{XKF}	X_1 Rising to CLK Falling	30	150	30	110	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control[1]	270		115		ns
t_{ACL}	A_{0-7} Valid to Leading of Control	240		115		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575		350	ns
t_{AFR}	Address Float after Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0		0	ns
t_{AL}	A_{8-15} Valid before Trailing Edge of ALE[1]	115		50		ns
t_{ALL}	A_{0-7} Valid before Trailing Edge of ALE	90		50		ns
t_{ARY}	READY Valid from Address Valid		220		100	ns
t_{CA}	Address (A_8–A_{15}) Valid after Control	120		60		ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) Edge of ALE	400		230		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		230		ns
t_{HABE}	HLDA to Bus Enable		210		150	ns
t_{HABF}	Bus Float after HLDA		210		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		ns
t_{HDH}	HOLD Hold Time	0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		ns
t_{INH}	INTR Hold Time	0		0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		ns
t_{LA}	Address Hold Time after ALE	100		50		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		ns
t_{LCK}	ALE Low during CLK High	100		50		ns
t_{LDR}	ALE to Valid Data during Read		460		270	ns
t_{LDW}	ALE to Valid Data during Write		200		120	ns
t_{LL}	ALE Width	140		80		ns
t_{LRY}	ALE to READY Stable		110		30	ns

TABLE 6. A.C. CHARACTERISTICS (Cont.)

Symbol	Parameter	8085A[2]		8085A-2[2] (Preliminary)		Units
		Min.	Max.	Min.	Max.	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		90		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300		150	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		ns
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$ [7]	0		0		ns
t_{RYH}	READY Hold Time	0		0		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		60		ns
t_{WDL}	LEADING Edge of WRITE to Data Valid		40		20	ns

Notes:
1. A_8-A_{15} address Specs apply to IO/$\overline{M}$, S_0, and S_1 except A_8-A_{15} are undefined during T_4-T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable.
2. Test conditions: t_{CYC} = 320ns (8085A)/200ns (8085A-2); C_L = 150pF.
3. For all output timing where C_L = 150pF use the following correction factors:
   25pF ≤ C_L < 150pF: -0.10 ns/pF
   150pF < C_L ≤ 300pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output voltage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20ns rise and fall time on inputs.
6. To calculate timing specifications at other values of t_{CYC} use Table 7.
7. Data hold time is guaranteed under all loading conditions.
8. Loading equivalent to 50 pF + 1 TTL input.

TABLE 7. BUS TIMING SPECIFICATION AS A T_{CYC} DEPENDENT

8085A

t_{AL}	–	(1/2) T - 45	MIN
t_{LA}	–	(1/2) T - 60	MIN
t_{LL}	–	(1/2) T - 20	MIN
t_{LCK}	–	(1/2) T - 60	MIN
t_{LC}	–	(1/2) T - 30	MIN
t_{AD}	–	(5/2 + N) T - 225	MAX
t_{RD}	–	(3/2 + N) T - 180	MAX
t_{RAE}	–	(1/2) T - 10	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T - 60	MIN
t_{WD}	–	(1/2) T - 60	MIN
t_{CC}	–	(3/2 + N) T - 80	MIN
t_{CL}	–	(1/2) T - 110	MIN
t_{ARY}	–	(3/2) T - 260	MAX
t_{HACK}	–	(1/2) T - 50	MIN
t_{HABF}	–	(1/2) T + 50	MAX
t_{HABE}	–	(1/2) T + 50	MAX
t_{AC}	–	(2/2) T - 50	MIN
t_1	–	(1/2) T - 80	MIN
t_2	–	(1/2) T - 40	MIN
t_{RV}	–	(3/2) T - 80	MIN
t_{LDR}	–	(4/2) T - 180	MAX

NOTE: N is equal to the total WAIT states.
T = t_{CYC}.

8085A-2 (Preliminary)

t_{AL}	–	(1/2) T - 50	MIN
t_{LA}	–	(1/2) T - 50	MIN
t_{LL}	–	(1/2) T - 20	MIN
t_{LCK}	–	(1/2) T - 50	MIN
t_{LC}	–	(1/2) T - 40	MIN
t_{AD}	–	(5/2 + N) T - 150	MAX
t_{RD}	–	(3/2 + N) T - 150	MAX
t_{RAE}	–	(1/2) T - 10	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T - 70	MIN
t_{WD}	–	(1/2) T - 40	MIN
t_{CC}	–	(3/2 + N) T - 70	MIN
t_{CL}	–	(1/2) T - 75	MIN
t_{ARY}	–	(3/2) T - 200	MAX
t_{HACK}	–	(1/2) T - 60	MIN
t_{HABF}	–	(1/2) T + 50	MAX
t_{HABE}	–	(1/2) T + 50	MAX
t_{AC}	–	(2/2) T - 85	MIN
t_1	–	(1/2) T - 60	MIN
t_2	–	(1/2) T - 30	MIN
t_{RV}	–	(3/2) T - 80	MIN
t_{LDR}	–	(4/2) T - 130	MAX

NOTE: N is equal to the total WAIT states.
T = t_{CYC}.

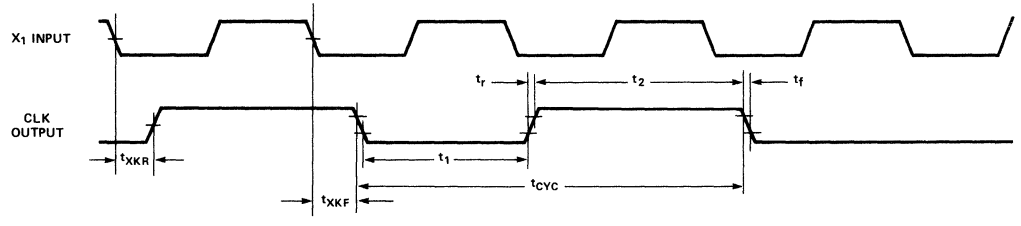
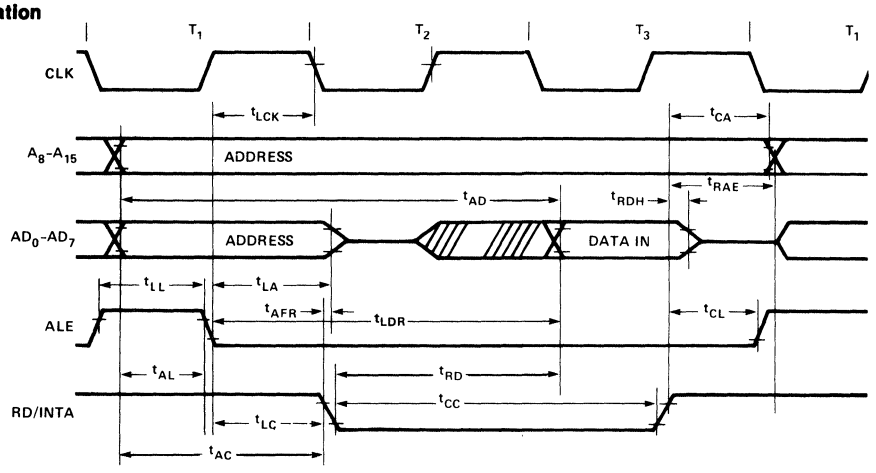
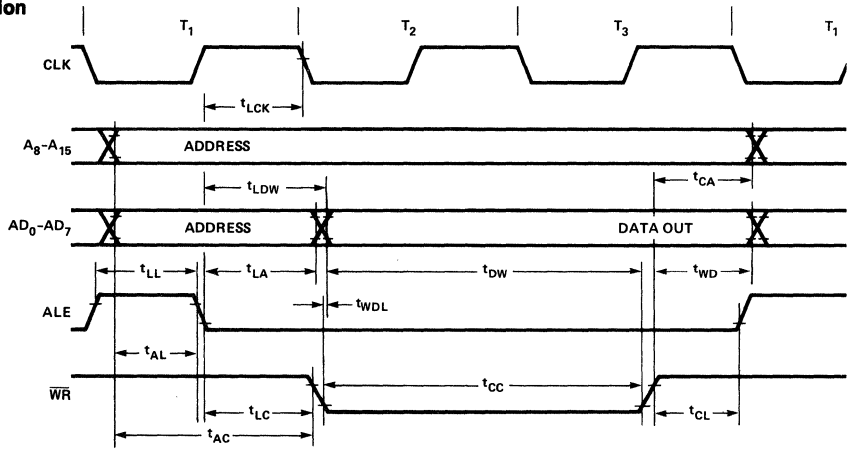


Figure 10. Clock Timing Waveform

Read Operation



Write Operation



Read operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation.

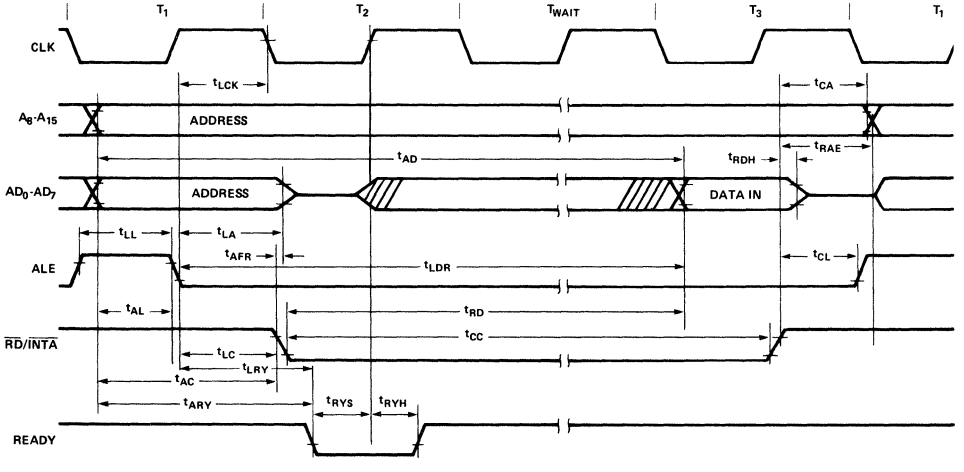


Figure 11. 8085A Bus Timing, With and Without Wait

Hold Operation

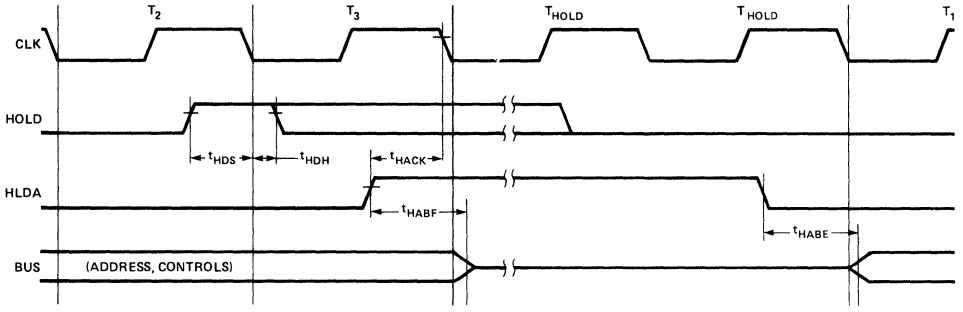


Figure 12. 8085A Hold Timing.

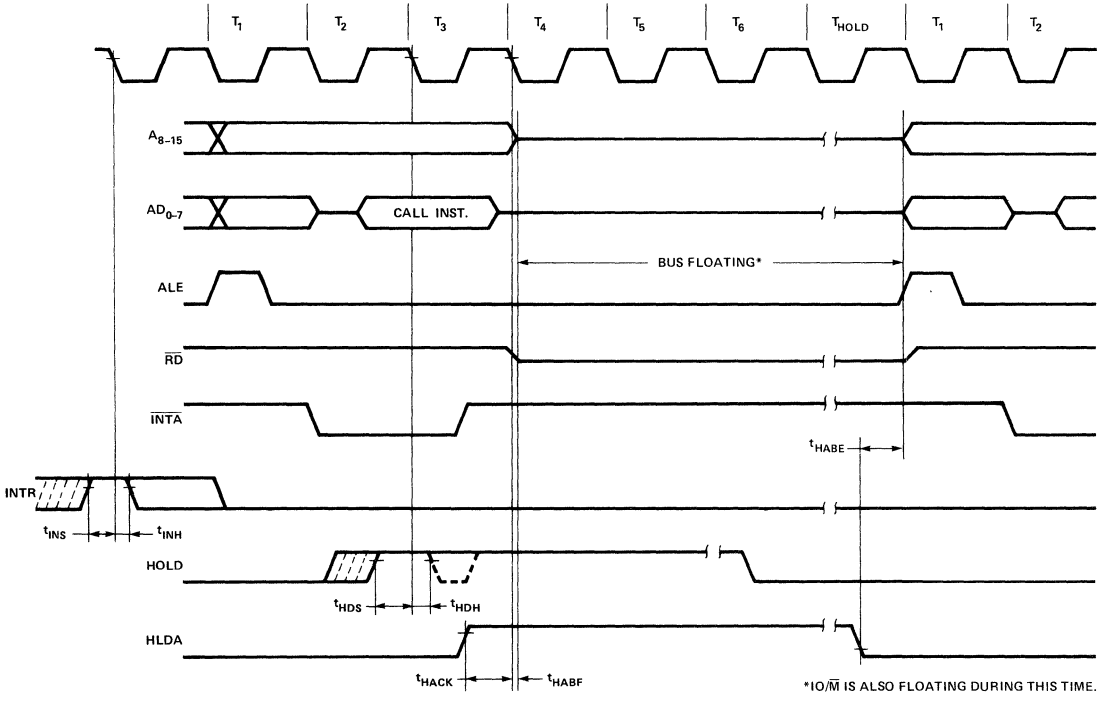


Figure 13. 8085A Interrupt and Hold Timing

TABLE 8. INSTRUCTION SET SUMMARY

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
MOVE, LOAD, AND STORE										
MOVr1 r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E H & L Registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4

TABLE 8. INSTRUCTION SET SUMMARY (Continued)

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
NEW 8085A INSTRUCTIONS										
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4

NOTES 1 DDD or SSS B 000, C 001, D 010, E 011, H 100 L 101 Memory 110 A 111
2 Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags

8155/8156/8155-2/8156-2
2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

8085A	8085A-2	Compatible CPU / Chip Enable
8155	8155-2	ACTIVE LOW
8156	8156-2	ACTIVE HIGH

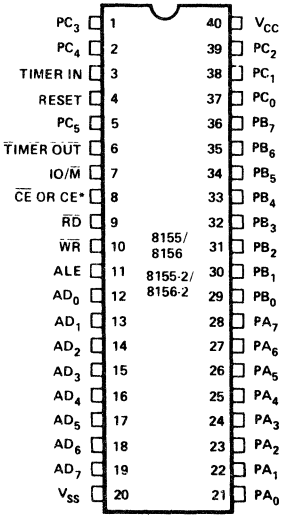
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/ Timer
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 8156 are RAM and I/O chips to be used in the MCS-85™ microcomputer system. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2.

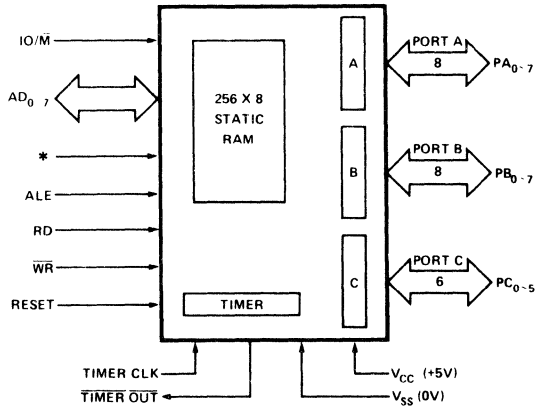
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



*: 8155/8155-2 = $\overline{CE}$, 8156/8156-2 = CE

8155/8156 PIN FUNCTIONS

Symbol	Function
RESET (input)	Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times.
AD_{0-7} (input)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155/56 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$ (input)	Chip Enable: On the 8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$ (input)	Read control: Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/$\overline{M}$.
ALE (input)	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$ (input)	Selects memory if low and I/O and command/status registers if high.
$PA_{0-7}(8)$ (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
$PB_{0-7}(8)$ (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
$PC_{0-5}(6)$ (input/output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — $\overline{ABF}$ (Port A Buffer Full) PC_2 — $\overline{A\ STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — $\overline{B\ BF}$ (Port B Buffer Full) PC_5 — B STB (Port B Strobe)
TIMER IN (input)	Input to the counter-timer.
$\overline{TIMER\ OUT}$ (output)	Timer output. This output can be either a square wave or a pulse depending on the timer mode.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

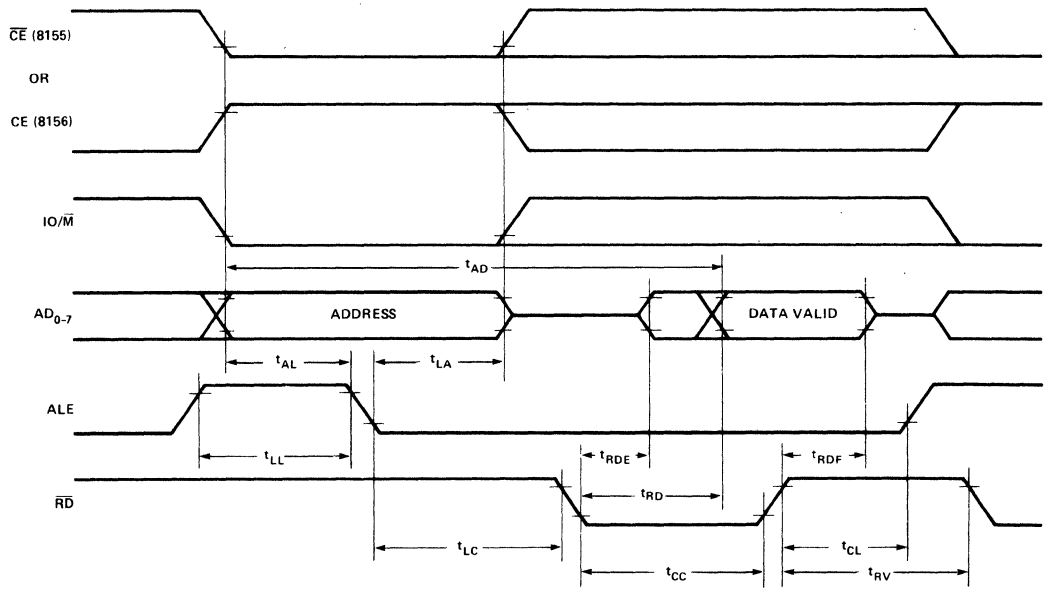
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	
I_{IL}(CE)	Chip Enable Leakage 8155 8156		 +100 -100	 μA μA	 V_{IN} = V_{CC} to 0V

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

		8155/8156		8155-2/8156-2 (Preliminary)		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNITS
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		30		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170		140	ns
t_{AD}	Address Stable to Data Out Valid		400		330	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float After READ	0	100	0	80	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to WRITE Set Up Time	150		100		ns
t_{WD}	Data In Hold Time After WRITE	0		0		ns
t_{RV}	Recovery Time Between Controls	300		200		ns
t_{WP}	WRITE to Port Output		400		300	ns
t_{PR}	Port Input Setup Time	70		50		ns
t_{RP}	Port Input Hold Time	50		10		ns
t_{SBF}	Strobe to Buffer Full		400		300	ns
t_{SS}	Strobe Width	200		150		ns
t_{RBE}	READ to Buffer Empty		400		300	ns
t_{SI}	Strobe to INTR On		400		300	ns
t_{RDI}	READ to INTR Off		400		300	ns
t_{PSS}	Port Setup Time to Strobe Strobe	50		0		ns
t_{PHS}	Port Hold Time After Strobe	120		100		ns
t_{SBE}	Strobe to Buffer Empty		400		300	ns
t_{WBF}	WRITE to Buffer Full		400		300	ns
t_{WI}	WRITE to INTR Off		400		300	ns
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low		400		300	ns
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High		400		300	ns
t_{RDE}	Data Bus Enable from READ Control	10		10		ns
t_1	TIMER-IN Low Time	80		40		ns
t_2	TIMER-IN High Time	120		70		ns

WAVEFORMS

a. Read Cycle



b. Write Cycle

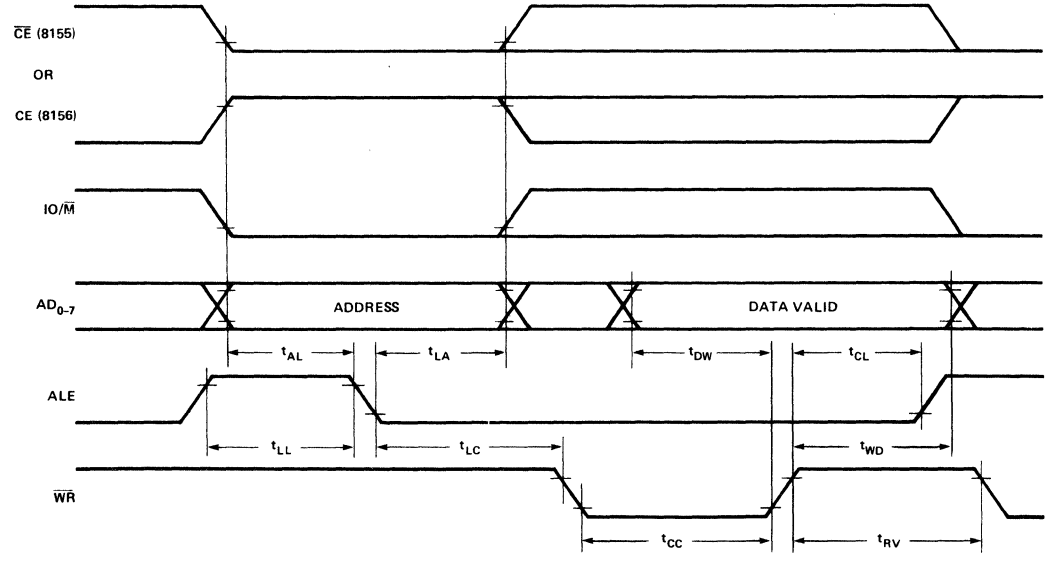
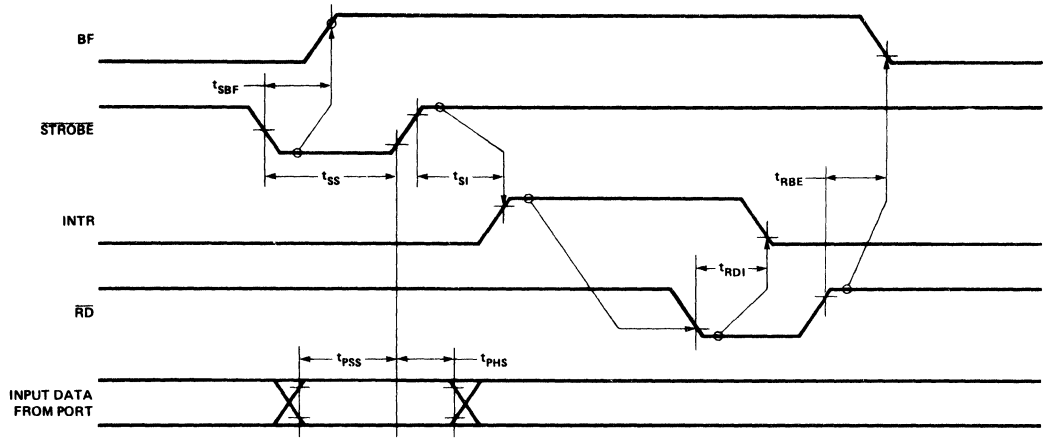


Figure 1. 8155/8156 Read/Write Timing Diagrams

a. Strobed Input Mode



b. Strobed Output Mode

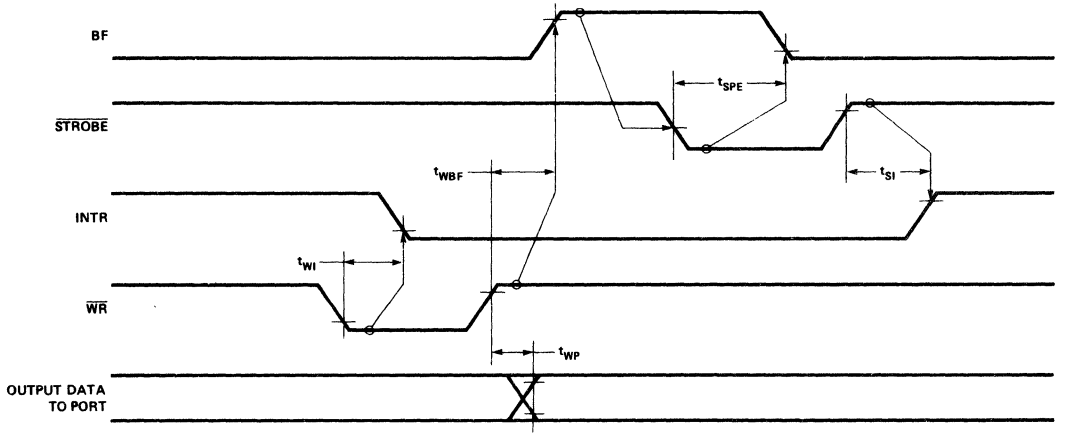
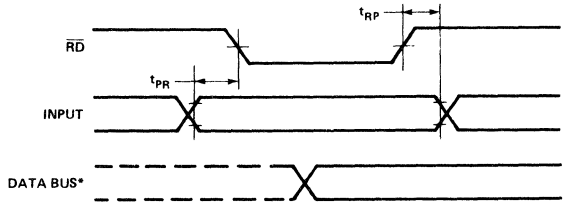
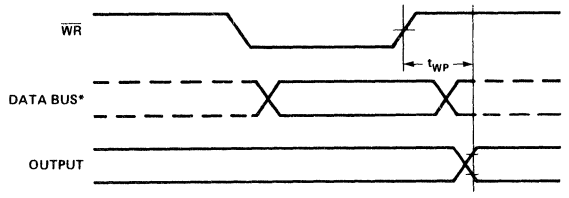


Figure 2. Strobed I/O Timing

a. Basic Input Mode

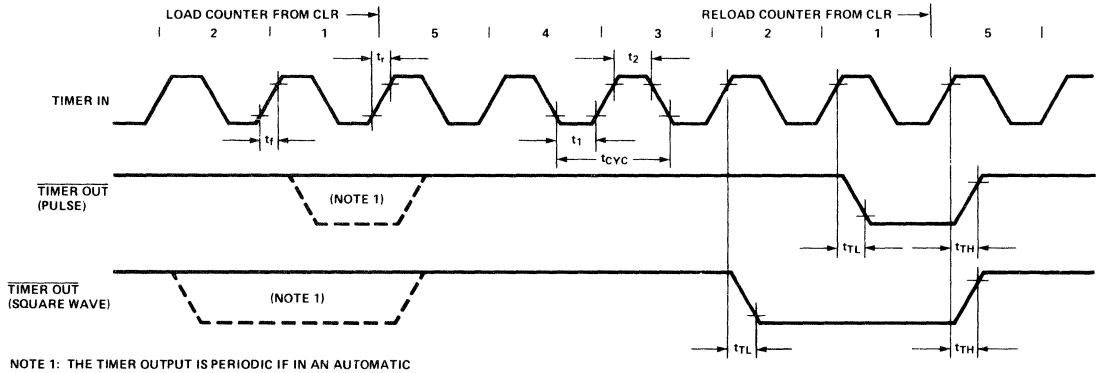


b. Basic Output Mode



*DATA BUS TIMING IS SHOWN IN FIGURE 7.

Figure 3. Basic I/O Timing Waveform



NOTE 1: THE TIMER OUTPUT IS PERIODIC IF IN AN AUTOMATIC RELOAD MODE (M_1 MODE BIT = 1)

Figure 4. Timer Output Waveform Countdown from 5 to 1

8185*/8185-2**
1024 x 8-BIT STATIC RAM FOR MCS-85™

***Compatible with 8085A**
****Compatible with 8085A-2**

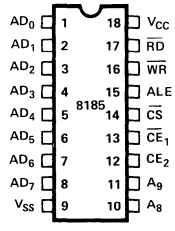
- **Multiplexed Address and Data Bus**
- **Directly Compatible with 8085A Microprocessor**
- **Low Operating Power Dissipation**
- **Low Standby Power Dissipation**
- **Single +5V Supply**
- **High Density 18-Pin Package**

The Intel® 8185 is an 8192-bit static random access memory (RAM) organized as 1024 words by 8-bits using N-channel Silicon-Gate MOS technology. The multiplexed address and data bus allows the 8185 to interface directly to the 8085A microprocessor to provide a maximum level of system integration

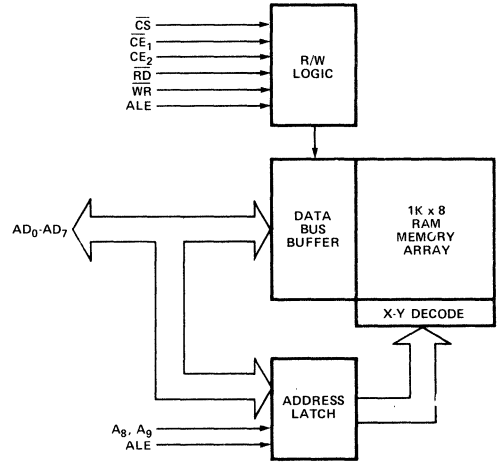
The low standby power dissipation minimizes system power requirements when the 8185 is disabled.

The 8185-2 is a high-speed selected version of the 8185.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

AD_0-AD_7	ADDRESS/DATA LINES
A_8, A_9	ADDRESS LINES
$\overline{CS}$	CHIP SELECT
$\overline{CE_1}$	CHIP ENABLE (IO/$\overline{M}$)
CE_2	CHIP ENABLE
ALE	ADDRESS LATCH ENABLE
$\overline{RD}$	READ ENABLE
$\overline{WR}$	WRITE ENABLE

OPERATIONAL DESCRIPTION

The 8185 has been designed to provide for direct interface to the multiplexed bus structure and bus timing of the 8085A microprocessor.

At the beginning of an 8185 memory access cycle, the 8-bit address on AD_{0-7}, A_8 and A_9, and the status of $\overline{CE}_1$ and CE_2 are all latched internally in the 8185 by the falling edge of ALE. If the latched status of both $\overline{CE}_1$ and CE_2 are active, the 8185 powers itself up, but no action occurs until the $\overline{CS}$ line goes low and the appropriate $\overline{RD}$ or $\overline{WR}$ control signal input is activated.

The $\overline{CS}$ input is not latched by the 8185 in order to allow the maximum amount of time for address decoding in selecting the 8185 chip. Maximum power consumption savings will occur, however, only when $\overline{CE}_1$ and CE_2 are activated selectively to power down the 8185 when it is not in use. A possible connection would be to wire the 8085A's IO/$\overline{M}$ line to the 8185's $\overline{CE}_1$ input, thereby keeping the 8185 powered down during I/O and interrupt cycles.

TABLE 1.
TRUTH TABLE FOR
POWER DOWN AND FUNCTION ENABLE

$\overline{CE}_1$	CE_2	$\overline{CS}$	(CS*)[2]	8185 Status
1	X	X	0	Power Down and Function Disable[1]
X	0	X	0	Power Down and Function Disable[1]
0	1	1	0	Powered Up and Function Disable[1]
0	1	0	1	Powered Up and Enabled

Notes:
X: Don't Care.
1: Function Disable implies Data Bus in high impedance state and not writing.
2: CS* = ($\overline{CE}_1$ = 0) • (CE_2 = 1) • ($\overline{CS}$ = 0)
CS* = 1 signifies all chip enables and chip select active

TABLE 2.
TRUTH TABLE FOR
CONTROL AND DATA BUS PIN STATUS

(CS*)	$\overline{RD}$	$\overline{WR}$	AD_{0-7} During Data Portion of Cycle	8185 Function
0	X	X	Hi-Impedance	No Function
1	0	1	Data from Memory	Read
1	1	0	Data to Memory	Write
1	1	1	Hi-Impedance	Reading, but not Driving Data Bus

Note:
X: Don't Care.

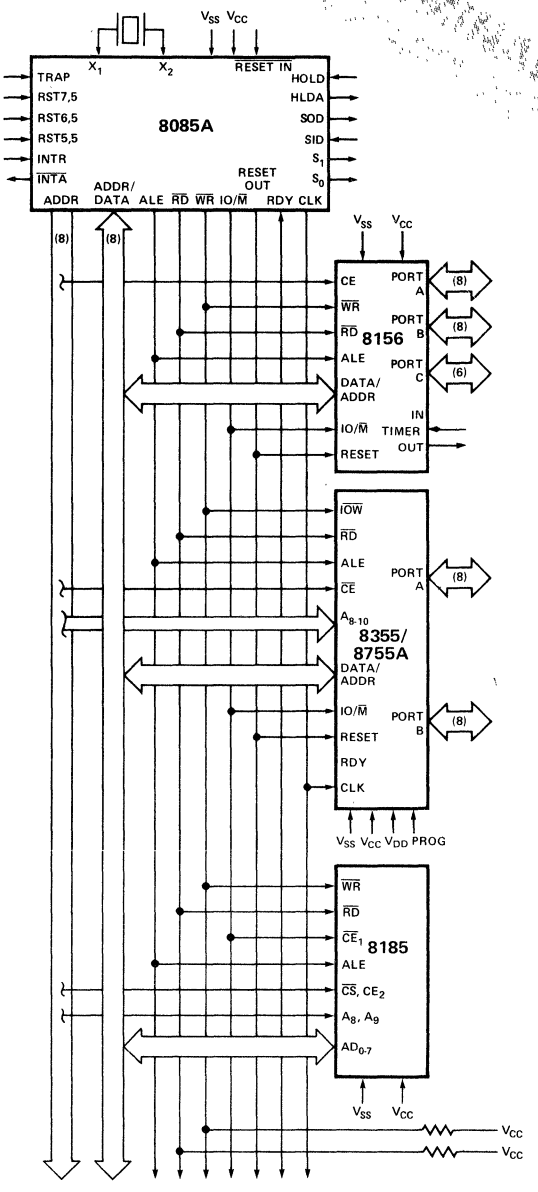


Figure 1. 8185 in an MCS-85 System.

4 Chips:
2K Bytes ROM
1.25K Bytes RAM
38 I/O Lines
1 Counter/Timer
2 Serial I/O Lines
5 Interrupt Inputs

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
with Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4			I_{OH} = 400μA
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current Powered Up		100	mA	
	Powered Down		25	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

Symbol	Parameter [1]	8185 Preliminary		8185-2 Preliminary		Units
		Min.	Max.	Min.	Max.	
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time After Latch	80		30		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control	170		140		ns
t_{LD}	ALE to Data Out Valid	300		200		ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float After READ	0	100	0	80	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to WRITE Set Up Time	150		150		ns
t_{WD}	Data In Hold Time After WRITE	20		20		ns
t_{SC}	Chip Select Set Up to Control Line	10		10		ns
t_{CS}	Chip Select Hold Time After Control	10		10		ns
t_{ALCE}	Chip Enable Set Up to ALE Falling	30		10		ns
t_{LACE}	Chip Enable Hold Time After ALE	50		30		ns

Notes:
1. All AC parameters are referenced at
   a) 2.4V and .45V for inputs
   b) 2.0V and .8V for outputs.

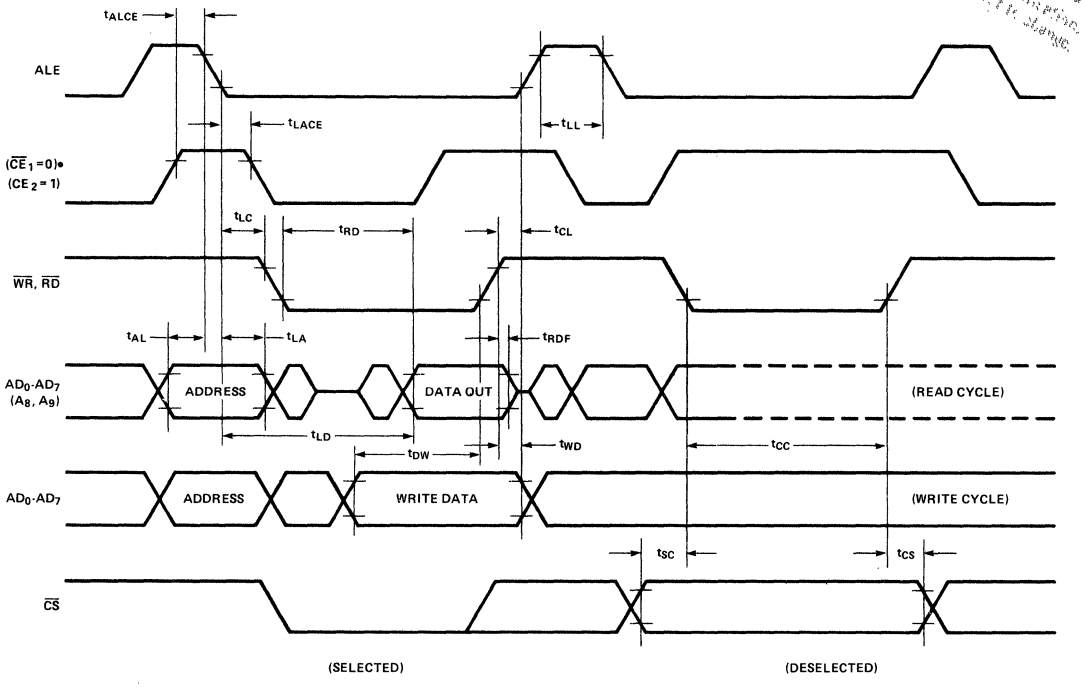


Figure 2. 8185 Timing.

8218/8219
BIPOLAR MICROCOMPUTER BUS CONTROLLERS FOR MCS-80™ AND MCS-85™ FAMILIES

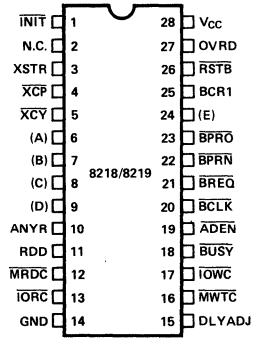
- **8218 for Use in MCS-80 Systems**
- **8219 for Use in MCS-85 Systems**
- **Coordinates the Sharing of a Common Bus Between Several CPU's**
- **Reduces Component Count in Multimaster Bus Arbitration Logic**
- **Single +5 Volt Power Supply**
- **28 Pin Package**

The 8218 and 8219 Microcomputer Bus Controllers consist of control logic which allows a bus master device such as a CPU or DMA channel to interface with other masters on a common bus, sharing memory and I/O devices. The 8218 and 8219 consist of:

1. Bus Arbitration Logic which operates from the Bus Clock ($\overline{BCLK}$) and resolves bus contention between devices sharing a common bus.
2. Timing Logic which when initiated by the bus arbitration logic generates timing signals for the memory and I/O command lines to guarantee set-up and hold times of the address/data lines onto the bus. The timing logic also signals to the bus arbitration logic when the current data transfer is completed and the bus is no longer needed.
3. Output Drive Logic which contains the logic and output drivers for the memory and I/O command lines.

An external RC time constant is used with the timing logic to generate the guaranteed address set-up and hold times on the bus. The 8219 can interface directly to the 8085A CPU and the 8218 interfaces to the 8080A CPU chip and the 8257 DMA controller.

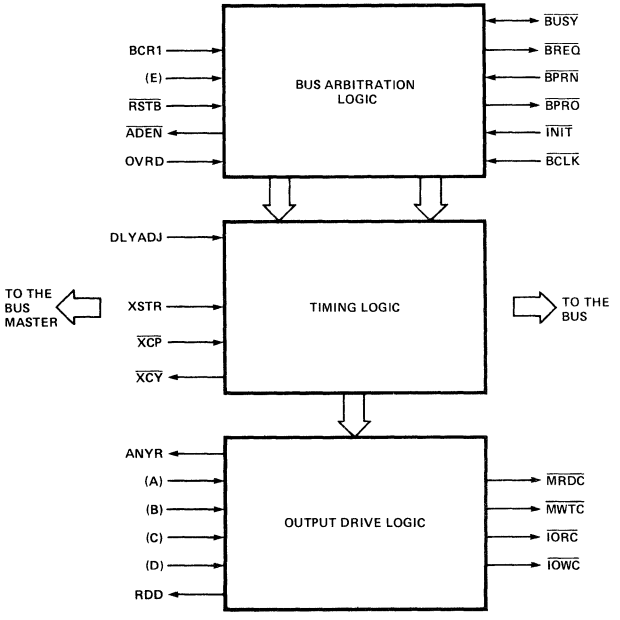
PIN CONFIGURATION



	8218	8219
(A)	$\overline{IOWR}$	IO/$\overline{M}$
(B)	$\overline{MWTR}$	$\overline{WR}$
(C)	$\overline{IORR}$	$\overline{RD}$
(D)	$\overline{MRDR}$	$\overline{ASRQ}$
(E)	$\overline{BCR2}$	BCR2

N.C. = NO CONNECT

BLOCK DIAGRAM



8218/8219 PIN DEFINITIONS

Signals Interfaced Directly to the System Bus

$\overline{\text{BREQ}}$ (TTL Output)

The Bus-Request is used with a central parallel priority resolution circuit. It indicates that the device needs to access the bus for one or more data transfers. It is synchronized with the Bus Clock.

$\overline{\text{BUSY}}$ (Input, O.C. Output)

Bus-Busy indicates to all master devices on the bus that the bus is in use. It inhibits any other device from getting the bus. It is synchronized with Bus Clock.

$\overline{\text{BCLK}}$ (Input)

The negative edge of Bus-Clock is used to synchronize the bus contention resolution circuit asynchronously to the CPU clock. It has 100ns min. period, 35%-65% duty cycle. It may be slowed, single stepped or stopped.

$\overline{\text{BPRN}}$ (Input)

The Bus-Priority-In indicates to a device that no device of a higher priority is requesting the bus. It is synchronous with the Bus Clock.

$\overline{\text{BPRO}}$ (TTL Output)

The Bus-Priority-Out is used with serial priority resolution circuits. Priority may be transferred to the next lower in priority as $\overline{\text{BPRN}}$.

$\overline{\text{INIT}}$ (Input)

The Initialize resets the 8218/8219 to a known internal state.

$\overline{\text{MRDC}}$ (3-State Output)

The Memory-Read-Control indicates that the Master is requesting a read operation from the addressed location. It is asynchronous to the Bus Clock.

$\overline{\text{MWTC}}$ (3-State Output)

The Memory-Write-Control indicates that data and an address have been placed on the bus by the Master and the data is to be deposited at that location. It is asynchronous to the Bus Clock.

$\overline{\text{IORC}}$ (3-State Output)

The I/O-Read-Control indicates that the Master is requesting a read operation from the I/O device addressed. It is asynchronous to the Bus Clock.

$\overline{\text{IOWC}}$ (3-State Output)

The I/O-Write-Control indicates that Data and an I/O device address has been placed on the bus by the Master and the data is to be deposited to the I/O device.

Signals Generated or Received by the Bus Master

BCR1/$\overline{\text{BCR2}}$ (Inputs)

Bus-Control-Request 1 or Bus-Control-Request 2 indicate to the 8218/8219 that the Master device is making a request to control the bus. BCR2 is active low in the 8218 ($\overline{\text{BCR2}}$). BCR2 is active high in the 8219.

RSTB (Input)

Request-Strobe latches the status of BCR1 and BCR2 into the 8218/8219. The strobe is active low in the 8218 and negative edge triggered in the 8219.

$\overline{\text{ADEN}}$ (TTL Output)

Address-and-Data-Enable indicates the Master has control of the bus. It is often used to enable Address and Data Buffers on the bus. It is synchronous with Bus Clock.

RDD (TTL Output)

Read-Data controls the direction of the bi-directional data bus drivers. It is asynchronous to the Bus Clock. A high on RDD indicates a read mode by the master.

OVRD (Input)

Override inhibits automatic deselect between transfers caused by a higher priority bus request. May be used for consecutive data transfers such as read-modify-write operations. It is asynchronous to the Bus Clock.

XSTR (Input, Rising-Edge-Triggered)

Transfer-Start-Request indicates to the 8218/8219 that a new data transfer cycle is requested to start. It is raised for each new word transfer in a multiple data word transfer. It is asynchronous to the Bus Clock.

$\overline{\text{XCP}}$ (Input, Falling-Edge-Triggered)

Transfer-Complete indicates to the 8218/8219 that the data has been received by the slave device in a write cycle or transmitted by the slave and received by master in a read cycle. It is asynchronous to the Bus Clock.

$\overline{\text{XCY}}$ (TTL Output)

Indicates that a data transfer is in progress. It is asynchronous to the Bus Clock.

$\overline{\text{WR}}$, $\overline{\text{RD}}$, IO/$\overline{\text{M}}$ (8219 Only) (Inputs from 8085 to the 8219)

WRITE, READ, IO/$\overline{\text{Memory}}$ are the control request inputs used by the 8085 and are internally decoded by the 8219 to produce the request signals $\overline{\text{MRDR}}$, $\overline{\text{MWTR}}$, $\overline{\text{IORR}}$, $\overline{\text{IOWR}}$. They are asynchronous to the Bus Clock.

$\overline{\text{ASRQ}}$ (8219 Only) (Input from 8085 System)

Can be used for interrupt status from the 8085. Acts like a level sensitive asynchronous bus request — no RSTB needed. It is asynchronous to the Bus Clock.

$\overline{\text{MRDR}}$, $\overline{\text{MWTR}}$, $\overline{\text{IORR}}$, $\overline{\text{IOWR}}$ (8218 Only) (Inputs from 8080 or 8257 to the 8218)

Memory-Read-Request, Memory-Write-Request, I/O-Read-Request, or I/O-Write-Request indicate that address and data have been placed on the bus and the appropriate request is being made to the addressed device. Only one of these inputs should be active at any one time. They are asynchronous to the Bus Clock.

ANYR (TTL Output)

Any-Request is the logical OR of the active state of $\overline{\text{MRDR}}$, $\overline{\text{MWTR}}$, $\overline{\text{IORR}}$, $\overline{\text{IOWR}}$. It may be tied to XSTR when the rising edge of ANYR is used to initiate a transfer.

DLYADJ (Input)

Delay-Adjust is used for connection of an external capacitor and resistor to ground to adjust the required set-up and hold time of address to control signal.

8218/8219 FUNCTIONAL DESCRIPTION

The 8218/8219 is a bipolar Bus Control Chip which reduces component count in the interface between a master device and the system Bus. (Master device: 8080, 8085, 8257 (DMA).)

The 8218 and 8219 serve three major functions:

1. Resolve bus contention.
2. Guarantee set-up and hold time of address/data lines to I/O and Memory read/write control signals (adjustable by external capacitor).
3. Provide sufficient drive on all bus command lines.

Bus Arbitration Logic

Bus Arbitration Logic activity begins when the Master makes a request for use of the bus on BCR1 or $\overline{BCR2}$. The request is strobed in by $\overline{RSTB}$. Following the next two falling edges of the bus clock (BCLK) the 8218/8219 outputs a bus request ($\overline{BREQ}$) and forces Bus Priority Out inactive (BPRO). See Figures 1a and 1b.

$\overline{BREQ}$ is used for requesting the bus when priority is decided by a parallel priority resolver circuit.

$\overline{BPRO}$ is used to allow lower priority devices to gain the bus when a serial priority resolving structure is used. $\overline{BPRO}$ would go to $\overline{BPRN}$ of the next lower priority Master.

When priority is granted to the Master (a low on $\overline{BPRN}$ and a high on $\overline{BUSY}$) the Master outputs a $\overline{BUSY}$ signal on the next falling edge of $\overline{BCLK}$. The $\overline{BUSY}$ signal locks the master onto the bus and prohibits the enable of any other masters onto the bus.

At the same time $\overline{BUSY}$ goes active, Address and Data Enable ($\overline{ADEN}$) goes active signifying that the Master has control of the bus. $\overline{ADEN}$ is often used to enable the bus drivers.

The Bus will be released only if the master loses priority; is not in the middle of a transfer, and Override is not active or, if the Master stops requesting the bus, is not in the middle of a data transfer, and Override is not active. $\overline{ADEN}$ then goes inactive.

Provision has been made in the 8218 to allow bus-synchronous requests. This mode is activated when BCR1, $\overline{BCR2}$ and $\overline{RSTB}$ are all low. This action asynchronously sets the synchronization flip flop (FF2) in Figure 1a.

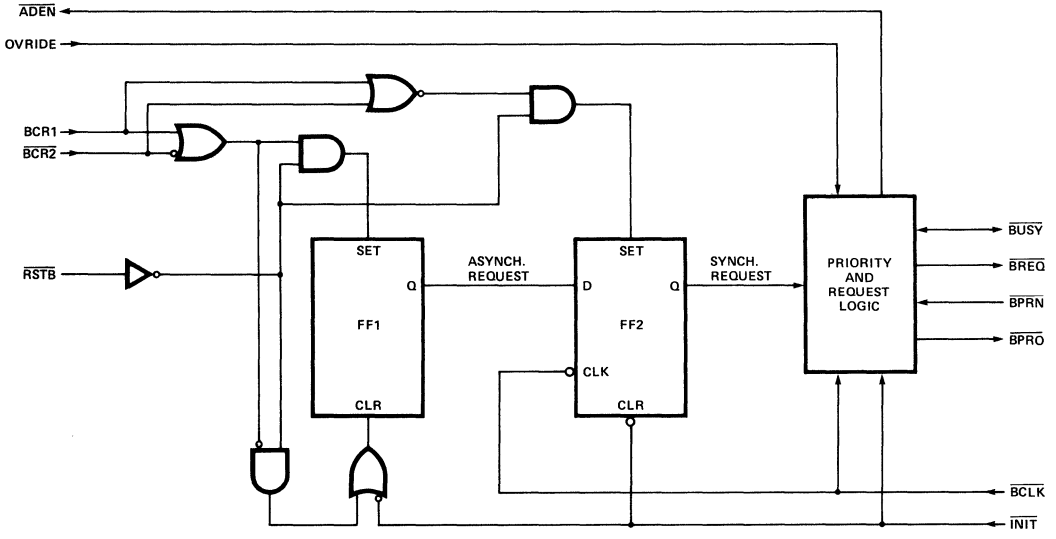


FIGURE 1a. 8218 BUS ARBITRATION LOGIC

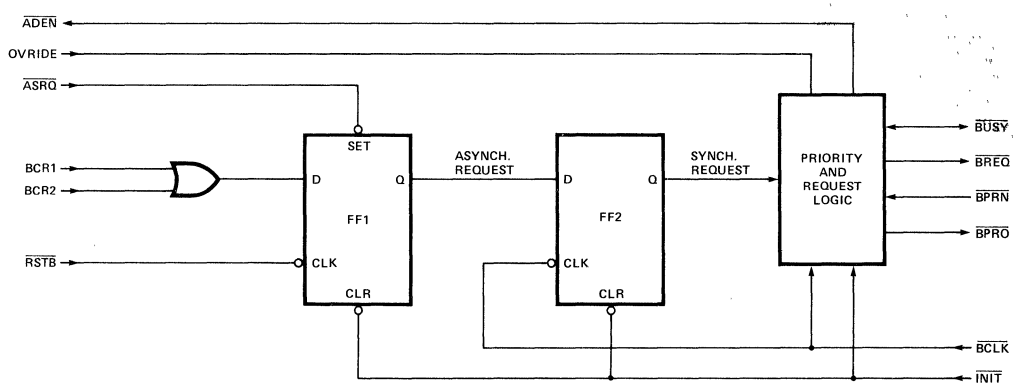


FIGURE 1b. 8219 BUS ARBITRATION LOGIC

Timing Logic

Timing Logic activity begins with the rising edge of XSTR (Transfer Start Request) or with $\overline{ADEN}$ going active, whichever occurs second. This action causes $\overline{XCY}$ (Transfer Cycle) to go active. 50-200ns later (depending on resistance and capacitance at DLYADJ) the appropriate Control Outputs will go active if the control input is active.

XSTR can be raised after the command goes active in the current transfer cycle so that a new transfer can be initiated immediately after the current transfer is complete.

A negative going edge on $\overline{XCP}$ (Transfer Complete) will cause the Control Outputs ($\overline{MRDC}$, etc.) to go inactive. 50-200ns later (depending on capacitance at DLYADJ) $\overline{XCY}$ will go inactive indicating the transfer cycle is completed.

Additional logic within the 8218/8219 guarantees that if a transfer cycle is started ($\overline{XCY}$ is active), but the bus is not requested ($\overline{BREQ}$ is inactive) and there is no command request input (ANYR is output low), then the transfer cycle will be cleared. This allows the bus to be released in applications where advanced bus requests are generated but the processor enters a HALT mode.

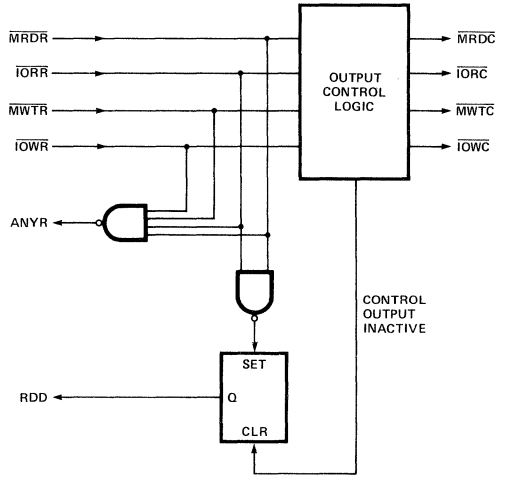


FIGURE 2a. 8218 CONTROL LOGIC

Control Logic

The control outputs are generated in the 8219 by decoding the 8085 system control outputs (i.e., RD, WR, IO/M) or in the 8218 by directly buffering the control inputs to the control outputs for use in an 8080 or DMA system (see Figures 2a and 2b). The control outputs may be held high (inactive) by the Timing Logic. Also the control outputs are enabled when the Master gains control of the bus and disabled when control is relinquished.

The Control Logic also has two other outputs, ANYR (Any Request) and RDD (Read Data). ANYR goes high (active) if any control requests (IOWR, etc.) are active. RDD controls the direction of the Masters Bi-directional Data Bus Drivers. The Bus Driver will always be in the Write mode (RDD = Low) except from the start of a Read Control Request to 25 to 70ns after $\overline{XCP}$ is activated.

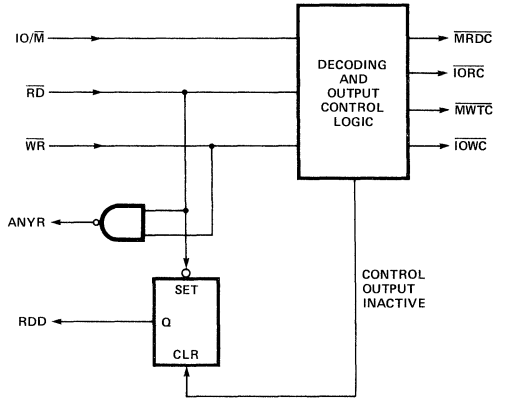


FIGURE 2b. 8219 CONTROL LOGIC

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage (V_{CC}) ..... -0.5V to +7V
Input Voltage ..... -1.0V to V_{CC} + 0.25V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

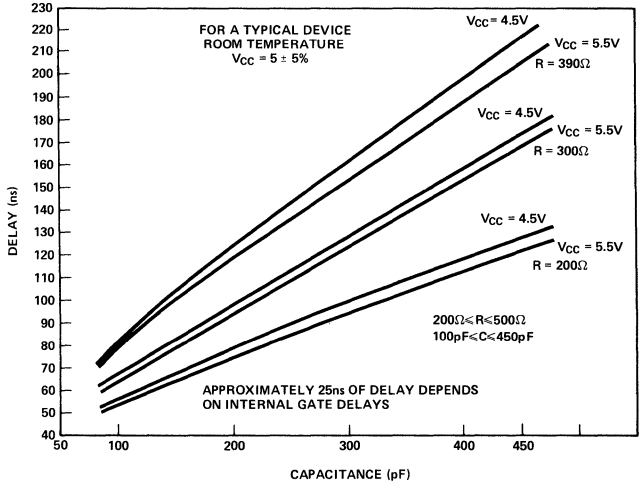
D.C. AND OPERATING CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = 5V ± 5%

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
V_C	Input Clamp Voltage			-1.0	V	V_{CC} = 4.75V, I_C = -5mA
I_F	Input Load Current					
	$\overline{MRDR}/\overline{INTA}/\overline{MWTR}/\overline{WR}$					V_{CC} = 5.25V
	$\overline{IORR}/\overline{RD}$, IOWR/IO/$\overline{M}$			-0.5	mA	V_F = 0.45V
	Other			-0.5	mA	
I_R	Input Leakage Current			100	μA	V_{CC} = 5.25 V_R = 5.25
V_{TH}	Input Threshold Voltage	0.8		2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		200	240	mA	V_{CC} = 5.25V
V_{OL}	Output Low Voltage					V_{CC} = 4.75
	$\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$			0.45	V	I_{OL} = 32mA
	$\overline{BREQ}$, $\overline{BUSY}$			0.45	V	I_{OL} = 20mA
	$\overline{XCY}$, $\overline{RDD}$, $\overline{ADEN}$			0.45	V	I_{OL} = 16mA
	$\overline{BPRO}$, ANYR			0.45	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage					V_{CC} = 4.75V
	$\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$ $\overline{BUSY}$ O.C.	2.4				I_{OH} = -2mA
	All Other Outputs	2.4				I_{OH} = -400μA
I_{OS}	Short Circuit Output Current	-10		-90	mA	V_{CC} = 5.25V, V_O = 0V
$I_{O(OFF)}$	Tri-State Output Current			-100	μA	V_{CC} = 5.25V, V_O = 0.45V
				+100	μA	V_{CC} = 5.25V, V_O = 5.25V

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{BCY}	Bus Clock Cycle Time	100			ns	35% to 65% Duty Cycle
t_{PW}	Bus Clock Pulse Width	35		0.65 t_{BCY}	ns	
t_{RQS}	$\overline{RSTB}$ to $\overline{BCLK}$ Set-Up Time	25			ns	
t_{CSS}	BCR_1 and $\overline{BCR_2}$ to $\overline{RSTB}$ Set-Up Time	15			ns	
t_{CSH}	BCR_1 and $\overline{BCR_2}$ to $\overline{RSTB}$ Hold Time	15			ns	
t_{RQD}	$\overline{BCLK}$ to $\overline{BREQ}$ Delay			35	ns	
t_{PRNS}	$\overline{BPRN}$ to $\overline{BCLK}$ Set-Up Time	23			ns	
t_{BNO}	$\overline{BRPN}$ to $\overline{BPRO}$ Delay			30	ns	
t_{BYD}	$\overline{BCLK}$ to $\overline{BUSY}$ Delay			55	ns	
t_{CAD}	$\overline{MRDR}$, $\overline{MWTR}$, $\overline{IORR}$, $\overline{IOWR}$ to ANYR Delay			30	ns	
t_{SXD}	XSTR to $\overline{XCY}$ Delay			40	ns	
t_{SCD}	XSTR to $\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$ Delay	50		200	ns	Adjustable by External R/C
t_{XSW}	XSTR Pulse Width	30			ns	
t_{XCD}	$\overline{XCP}$ to $\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$ Delay			50	ns	
t_{XCW}	$\overline{XCP}$ Pulse Width	35			ns	
t_{CCD}	$\overline{XCP}$ to $\overline{XCY}$ Delay	50		200	ns	Adjustable by External R/C
t_{CMD}	$\overline{MRDR}$, $\overline{MWTR}$, $\overline{IORR}$, $\overline{IOWR}$ to $\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$			35	ns	
t_{CRD}	$\overline{MRDR}$, $\overline{MWTR}$, $\overline{IORR}$, $\overline{IOWR}$ to RDD Delay			25	ns	
t_{RW}	$\overline{RSTB}$ Min. Neg. Pulse Width	30			ns	
t_{CPD}	$\overline{BCLK}$ to $\overline{BPRO}$ Delay			40	ns	
t_{XRD}	$\overline{XCP}$ to $\overline{RDD}$ Delay	25		70	ns	

8218/19 XSTR TO OUTPUT COMMAND DELAY
ONESHOT DELAY VS. DELAY ADJUST CAPACITANCE AND RESISTANCE



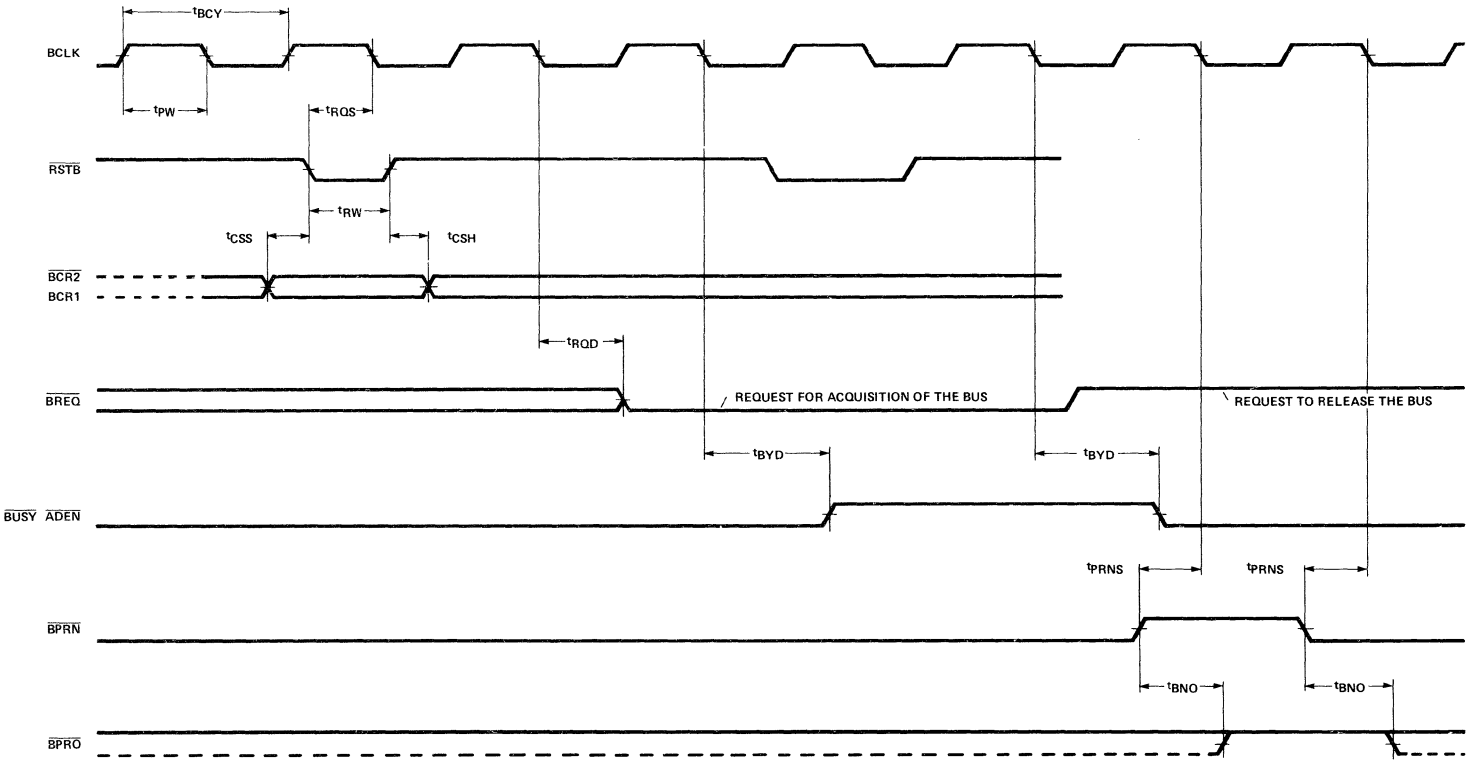


FIGURE 3a. 8218/8219 SYNCHRONOUS BUS TIMING (SYSTEM BUS PREVIOUSLY NOT IN USE).

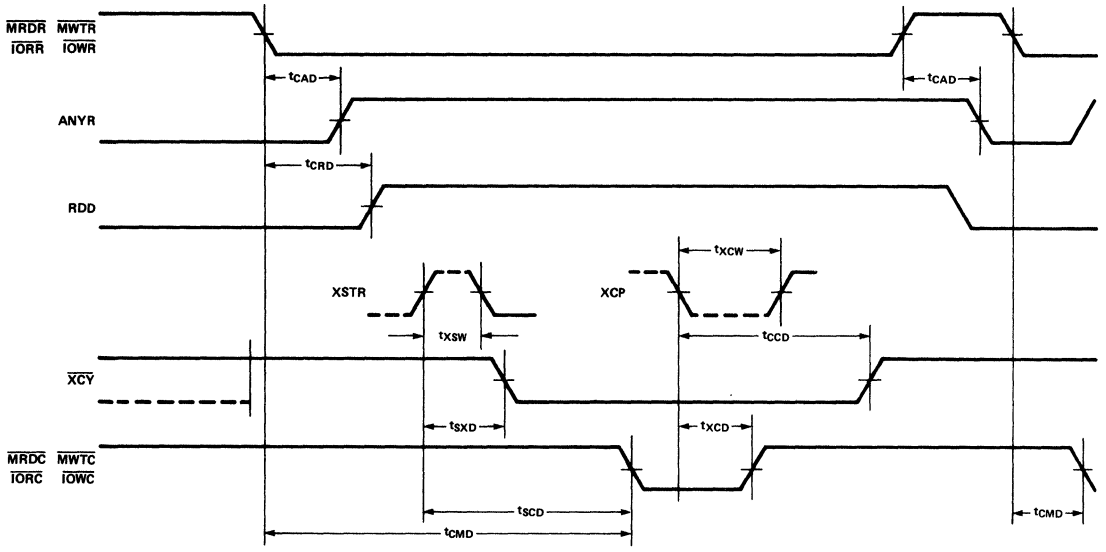


FIGURE 3b. 8218/8219 CONTROL CYCLE (SYSTEM BUS PREVIOUSLY NOT IN USE).

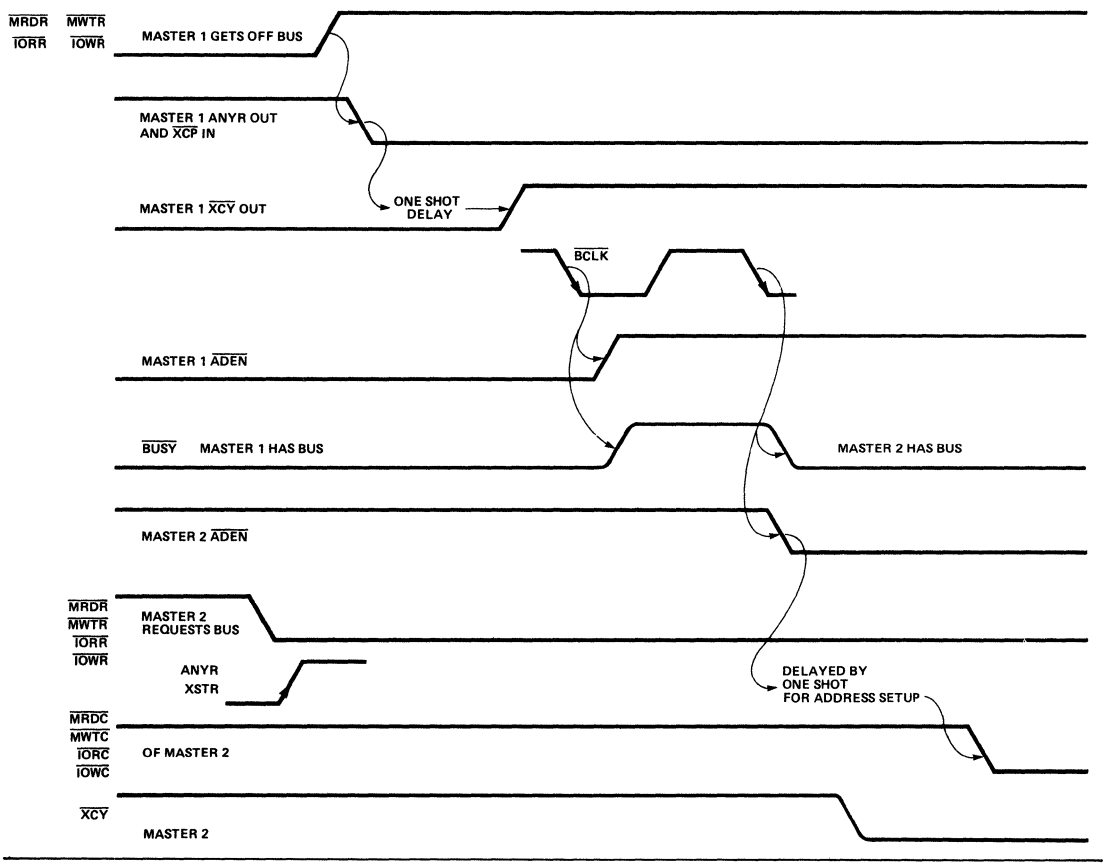


FIGURE 3c. 8218/8219 BUS CONTROL EXCHANGE (MASTER NO. 1 LEAVING BUS AND MASTER NO. 2 GETTING ON BUS).

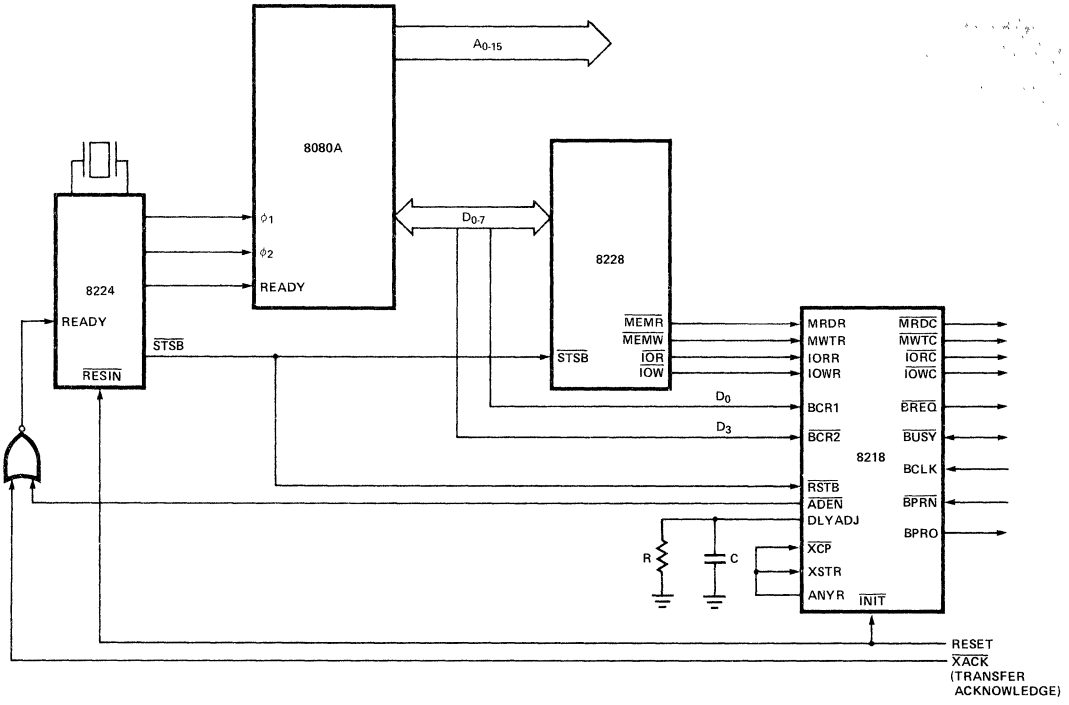


FIGURE 4a. MCS-80 CPU WITH 8218.

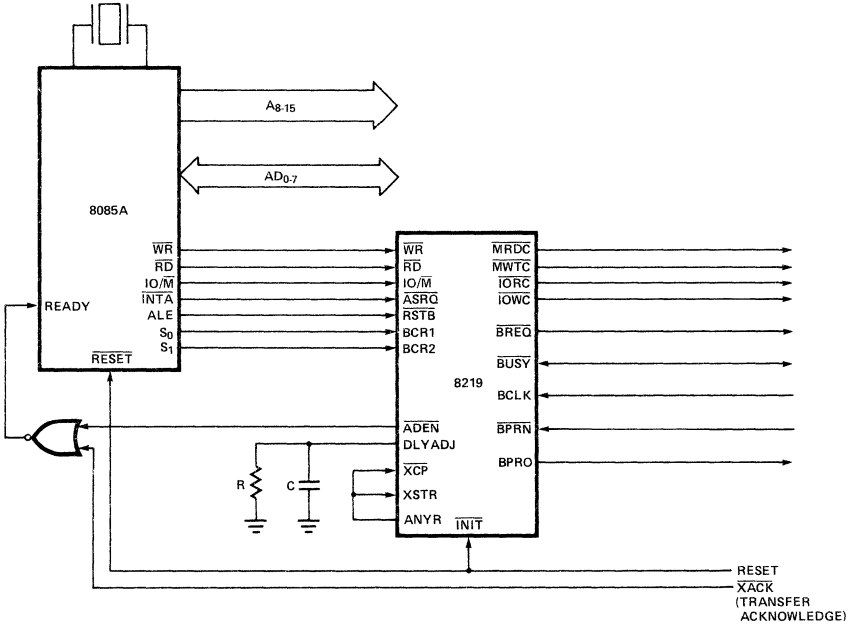


FIGURE 4b. MCS-85 CPU WITH 8219.

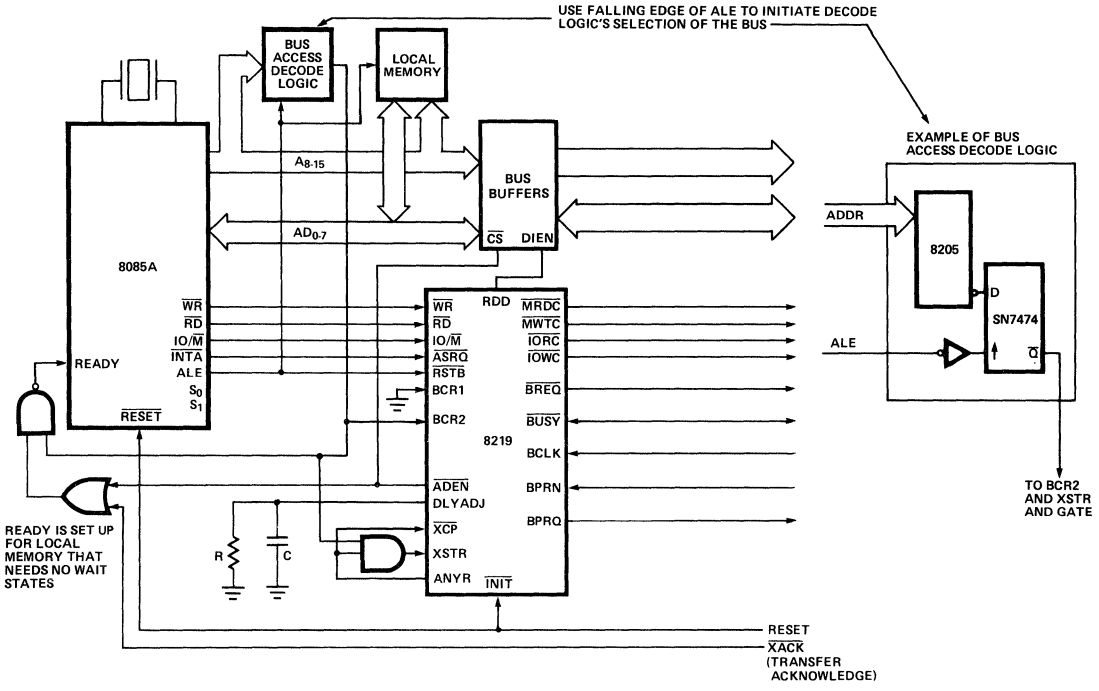
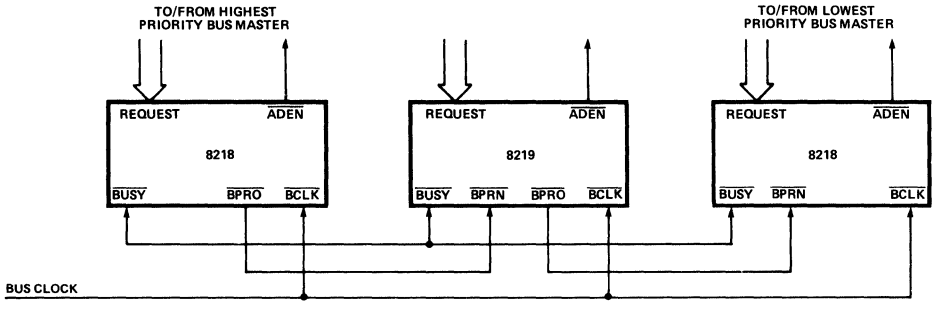
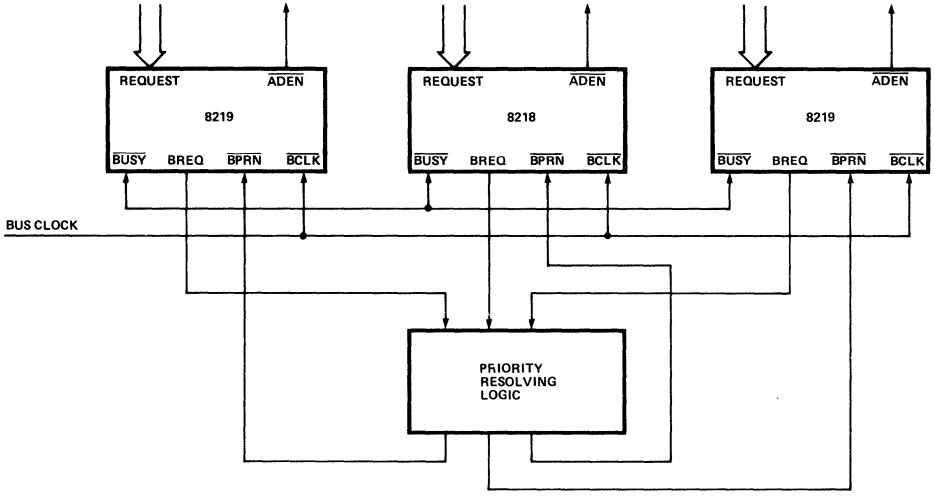


FIGURE 4c. MCS-85 CPU WITH 8219 USING LOCAL MEMORY.



"DAISY CHAIN" CONFIGURATION



PARALLEL REQUEST CONFIGURATION

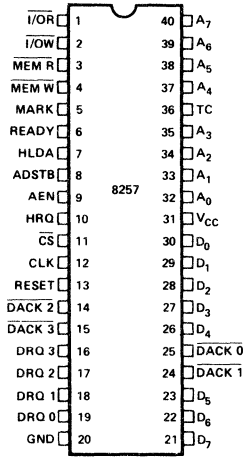
FIGURE 5. TWO METHODS OF CONNECTING MULTIPLE 8218/8219's TO RESOLVE BUS CONTENTION AMONG MULTIPLE MASTERS.

8257/8257-5
PROGRAMMABLE DMA CONTROLLER

- MCS-85™ Compatible 8257-5
- 4-Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Single TTL Clock
- Single +5V Supply
- Auto Load Mode

The Intel® 8257 is a 4-channel direct memory access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel® microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus in accomplished via the CPU's hold function. The 8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers. The 8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

PIN CONFIGURATION

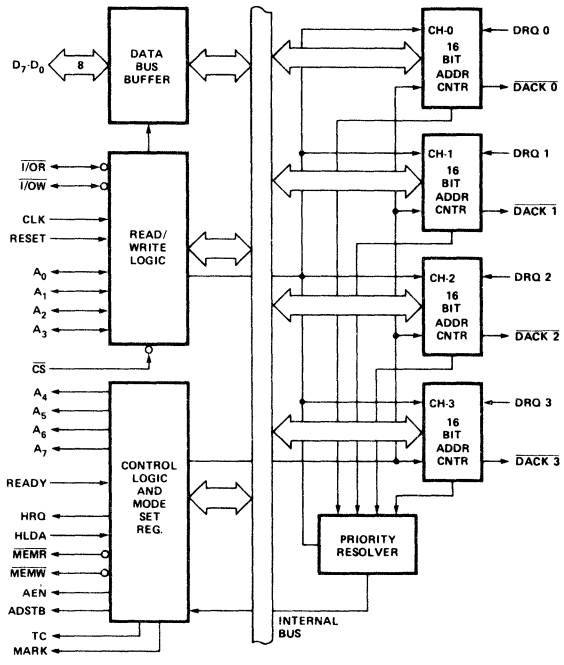


PIN NAMES

D_7-D_0	DATA BUS
A_7-A_0	ADDRESS BUS
$\overline{I/OR}$	I/O READ
$\overline{I/OW}$	I/O WRITE
$\overline{MEMR}$	MEMORY READ
$\overline{MEMW}$	MEMORY WRITE
CLK	CLOCK INPUT
RESET	RESET INPUT
READY	READY
HRQ	HOLD REQUEST (TO 8080A)
HLDA	HOLD ACKNOWLEDGE (FROM 8080A)

AEN	ADDRESS ENABLE
ADSTB	ADDRESS STROBE
TC	TERMINAL COUNT
MARK	MODULO 128 MARK
DRQ_3-DRQ_0	DMA REQUEST INPUT
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA ACKNOWLEDGE OUT
$\overline{CS}$	CHIP SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

General

The 8257 is a programmable, Direct Memory Access (DMA) device which, when coupled with a single Intel® 8212 I/O port device, provides a complete four-channel DMA controller for use in Intel® microcomputer systems. After being initialized by software, the 8257 can transfer a block of data, containing up to 16,384 bytes, between memory and a peripheral device directly, without further intervention required of the CPU. Upon receiving a DMA transfer request from an enabled peripheral, the 8257:

1. Acquires control of the system bus.
2. Acknowledges that requesting peripheral which is connected to the highest priority channel.
3. Outputs the least significant eight bits of the memory address onto system address lines A_0-A_7, outputs the most significant eight bits of the memory address to the 8212 I/O port via the data bus (the 8212 places these address bits on lines A_8-A_{15}), and
4. Generates the appropriate memory and I/O read/write control signals that cause the peripheral to receive or deposit a data byte directly from or to the addressed location in memory.

The 8257 will retain control of the system bus and repeat the transfer sequence, as long as a peripheral maintains its DMA request. Thus, the 8257 can transfer a block of data to/from a high speed peripheral (e.g., a sector of data on a floppy disk) in a single "burst". When the specified number of data bytes have been transferred, the 8257 activates its Terminal Count (TC) output, informing the CPU that the operation is complete.

The 8257 offers three different modes of operation: (1) DMA read, which causes data to be transferred from memory to a peripheral; (2) DMA write, which causes data to be transferred from a peripheral to memory; and (3) DMA verify, which does not actually involve the transfer of data. When an 8257 channel is in the DMA verify mode, it will respond the same as described for transfer operations, except that no memory or I/O read/write control signals will be generated, thus preventing the transfer of data. The 8257, however, will gain control of the system bus and will acknowledge the peripheral's DMA request for each DMA cycle. The peripheral can use these acknowledge signals to enable an internal access of each byte of a data block in order to execute some verification procedure, such as the accumulation of a CRC (Cyclic Redundancy Code) checkword. For example, a block of DMA verify cycles might follow a block of DMA read cycles (memory to peripheral) to allow the peripheral to verify its newly acquired data.

Block Diagram Description

1. DMA Channels

The 8257 provides four separate DMA channels (labeled CH-0 to CH-3). Each channel includes two sixteen-bit registers: (1) a DMA address register, and (2) a terminal count register. Both registers must be initialized before a channel is enabled. The DMA address register is loaded with the address of the first memory location to be accessed. The value loaded into the low-order 14-bits of the terminal count register specifies the number of DMA cycles minus one before the Terminal Count (TC) output is activated. For instance, a terminal count of 0 would cause the TC output to be active in the first DMA cycle for that channel. In general, if N = the number of desired DMA cycles, load the value N-1 into the low-order 14-bits of the terminal count register. The most significant two bits of the terminal count register specify the type of DMA operation for that channel.

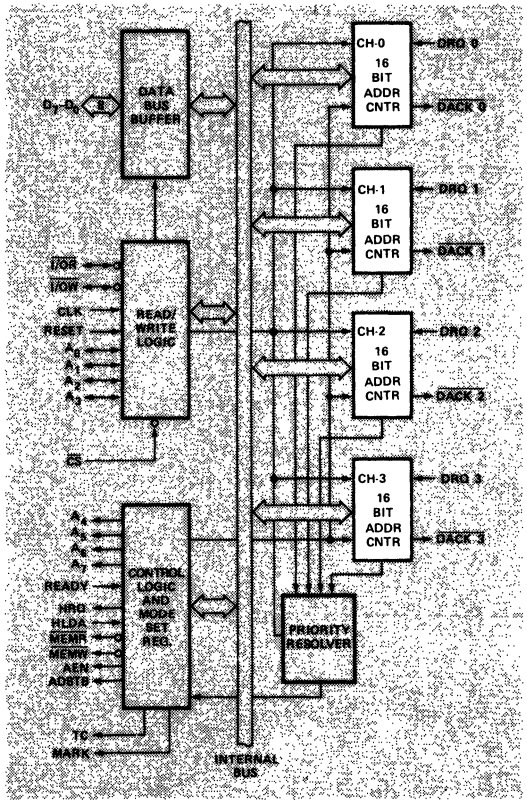


Figure 1. 8257 Block Diagram Showing DMA Channels

These two bits are not modified during a DMA cycle, but can be changed between DMA blocks.

Each channel accepts a DMA Request (DRQn) input and provides a DMA Acknowledge (DACKn) output.

(DRQ 0-DRQ 3)

DMA Request: These are individual asynchronous channel request inputs used by the peripherals to obtain a DMA cycle. If not in the rotating priority mode then DRQ 0 has the highest priority and DRQ 3 has the lowest. A request can be generated by raising the request line and holding it high until DMA acknowledge. For multiple DMA cycles (Burst Mode) the request line is held high until the DMA acknowledge of the last cycle arrives.

($\overline{\text{DACK 0}}$ - $\overline{\text{DACK 3}}$)

DMA Acknowledge: An active low level on the acknowledge output informs the peripheral connected to that channel that it has been selected for a DMA cycle. The $\overline{\text{DACK}}$ output acts as a "chip select" for the peripheral device requesting service. This line goes active (low) and inactive (high) once for each byte transferred even if a burst of data is being transferred.

2. Data Bus Buffer

This three-state, bi-directional, eight bit buffer interfaces the 8257 to the system data bus.

(D_0-D_7)

Data Bus Lines: These are bi-directional three-state lines. When the 8257 is being programmed by the CPU, eight-bits of data for a DMA address register, a terminal count register or the Mode Set register are received on the data bus. When the CPU reads a DMA address register, a terminal count register or the Status register, the data is sent to the CPU over the data bus. During DMA cycles (when the 8257 is the bus master), the 8257 will output the most significant eight-bits of the memory address (from one of the DMA address registers) to the 8212 latch via the data bus. These address bits will be transferred at the beginning of the DMA cycle; the bus will then be released to handle the memory data transfer during the balance of the DMA cycle.

BIT 15	BIT 14	TYPE OF DMA OPERATION
0	0	Verify DMA Cycle
0	1	Write DMA Cycle
1	0	Read DMA Cycle
1	1	(Illegal)

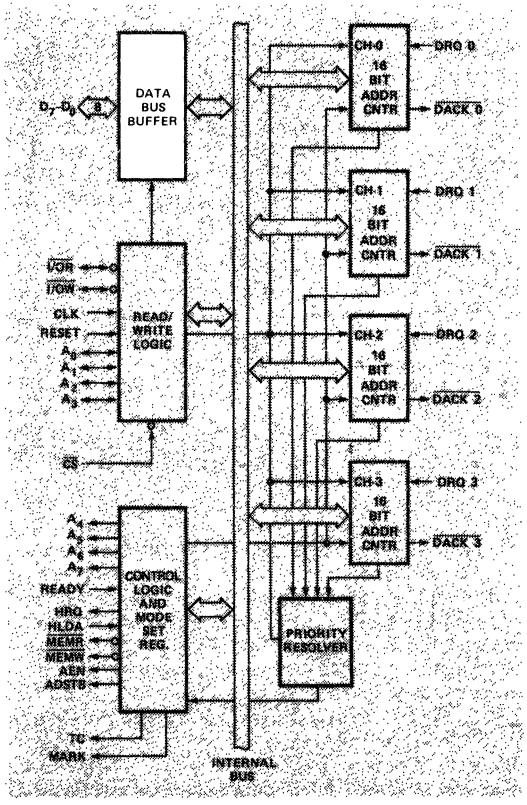


Figure 2. 8257 Block Diagram Showing Data Bus Buffer

3. Read/Write Logic

When the CPU is programming or reading one of the 8257's registers (i.e., when the 8257 is a "slave" device on the system bus), the Read/Write Logic accepts the I/O Read ($\overline{I/OR}$) or I/O Write ($\overline{I/OW}$) signal, decodes the least significant four address bits, (A_0-A_3), and either writes the contents of the data bus into the addressed register (if $\overline{I/OW}$ is true) or places the contents of the addressed register onto the data bus (if $\overline{I/OR}$ is true).

During DMA cycles (i.e., when the 8257 is the bus "master"), the Read/Write Logic generates the I/O read and memory write (DMA write cycle) or I/O Write and memory read (DMA read cycle) signals which control the data link with the peripheral that has been granted the DMA cycle.

Note that during DMA transfers Non-DMA I/O devices should be de-selected (disabled) using "AEN" signal to inhibit I/O device decoding of the memory address as an erroneous device address.

($\overline{I/OR}$)

I/O Read: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the 8-bit status register or the upper/lower byte of a 16-bit DMA address register or terminal count register to be read. In the "master" mode, $\overline{I/OR}$ is a control output which is used to access data from a peripheral during the DMA write cycle.

($\overline{I/OW}$)

I/O Write: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the contents of the data bus to be loaded into the 8-bit mode set register or the upper/lower byte of a 16-bit DMA address register or terminal count register. In the "master" mode, $\overline{I/OW}$ is a control output which allows data to be output to a peripheral during a DMA read cycle.

(CLK)

Clock Input: Generally from an Intel® 8224 Clock Generator device. (ϕ2 TTL) or Intel® 8085A CLK output.

(RESET)

Reset: An asynchronous input (generally from an 8224 or 8085 device) which disables all DMA channels by clearing the mode register and 3-states all control lines.

(A_0-A_3)

Address Lines: These least significant four address lines are bi-directional. In the "slave" mode they are inputs which select one of the registers to be read or programmed. In the "master" mode, they are outputs which constitute the least significant four bits of the 16-bit memory address generated by the 8257.

($\overline{CS}$)

Chip Select: An active-low input which enables the I/O Read or I/O Write input when the 8257 is being read or programmed in the "slave" mode. In the "master" mode, $\overline{CS}$ is automatically disabled to prevent the chip from selecting itself while performing the DMA function.

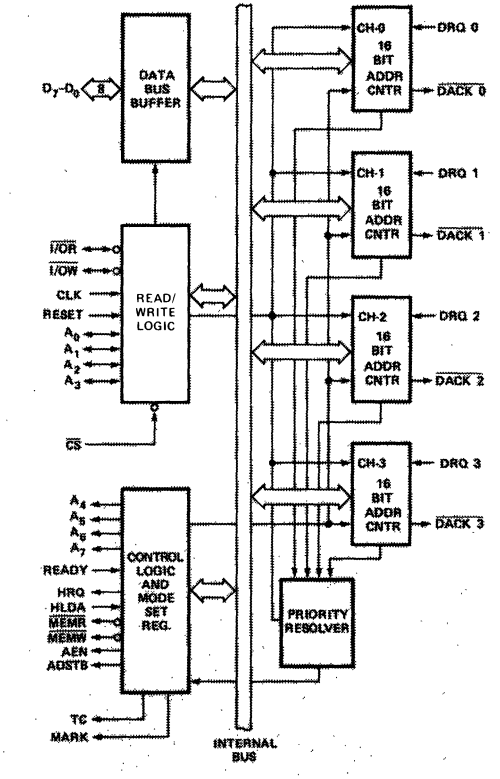


Figure 5. 8257 Block Diagram Showing Read/Write Logic Function

4. Control Logic

This block controls the sequence of operations during all DMA cycles by generating the appropriate control signals and the 16-bit address that specifies the memory location to be accessed.

(A_4-A_7)

Address Lines: These four address lines are three-state outputs which constitute bits 4 through 7 of the 16-bit memory address generated by the 8257 during all DMA cycles.

(READY)

Ready: This asynchronous input is used to elongate the memory read and write cycles in the 8257 with wait states if the selected memory requires longer cycles.

(HRQ)

Hold Request: This output requests control of the system bus. In systems with only one 8257, HRQ will normally be applied to the HOLD input on the CPU.

(HLDA)

Hold Acknowledge: This input from the CPU indicates that the 8257 has acquired control of the system bus.

($\overline{\text{MEMR}}$)

Memory Read: This active-low three-state output is used to read data from the addressed memory location during DMA Read cycles.

($\overline{\text{MEMW}}$)

Memory Write: This active-low three-state output is used to write data into the addressed memory location during DMA Write cycles.

(ADSTB)

Address Strobe: This output strobes the most significant byte of the memory address into the 8212 device from the data bus.

(AEN)

Address Enable: This output is used to disable (float) the System Data Bus and the System Control Bus. It may also be used to disable (float) the System Address Bus by use of an enable on the Address Bus drivers in systems to inhibit non-DMA devices from responding during DMA cycles. It may be further used to isolate the 8257 data bus from the System Data Bus to facilitate the transfer of the 8 most significant DMA address bits over the 8257 data I/O pins without subjecting the System Data Bus to any timing constraints for the transfer. When the 8257 is used in an I/O device structure (as opposed to memory mapped), this AEN output should be used to disable the selection of an I/O device when the DMA address is on the address bus. The I/O device selection should be determined by the DMA acknowledge outputs for the 4 channels.

(TC)

Terminal Count: This output notifies the currently selected peripheral that the present DMA cycle should be the last cycle for this data block. If the TC STOP bit in the Mode Set register is set, the selected channel will be automatically disabled at the end of that DMA cycle. TC is activated when the 14-bit value in the selected channel's terminal count register equals zero. Recall that the low-order 14-bits of the terminal count register should be loaded with the values (n-1), where n = the desired number of the DMA cycles.

(MARK)

Modulo 128 Mark: This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output. MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block. Only if the total number of DMA cycles (n) is evenly divisable by 128 (and the terminal count register was loaded with n-1), will MARK occur at 128 (and each succeeding multiple of 128) cycles from the beginning of the data block.

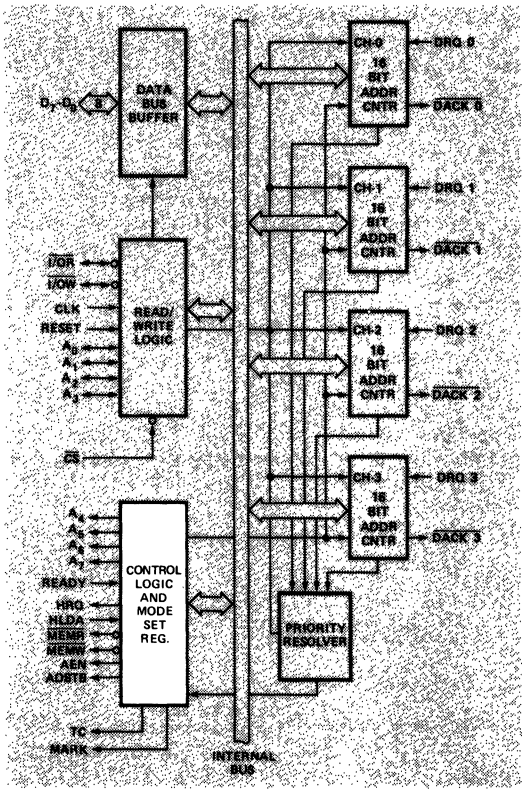
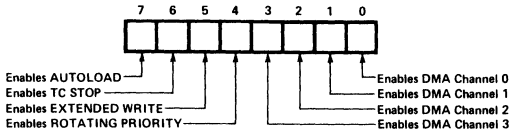


Figure 4. 8257 Block Diagram Showing Control Logic and Mode Set Register

5. Mode Set Register

When set, the various bits in the Mode Set register enable each of the four DMA channels, and allow four different options for the 8257:

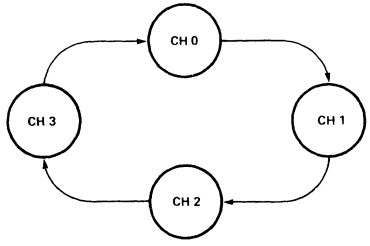


The Mode Set register is normally programmed by the CPU after the DMA address register(s) and terminal count register(s) are initialized. The Mode Set Register is cleared by the RESET input, thus disabling all options, inhibiting all channels, and preventing bus conflicts on power-up. A channel should not be left enabled unless its DMA address and terminal count registers contain valid values; otherwise, an inadvertent DMA request (DRQn) from a peripheral could initiate a DMA cycle that would destroy memory data.

The various options which can be enabled by bits in the Mode Set register are explained below:

Rotating Priority Bit 4

In the Rotating Priority Mode, the priority of the channels has a circular sequence. After each DMA cycle, the priority of each channel changes. The channel which had just been serviced will have the lowest priority.



If the ROTATING PRIORITY bit is not set (set to a zero), each DMA channel has a fixed priority. In the fixed priority mode, Channel 0 has the highest priority and Channel 3 has the lowest priority. If the ROTATING PRIORITY bit is set to a one, the priority of each channel changes after each DMA cycle (not each DMA request). Each channel moves up to the next highest priority assignment, while the channel which has just been serviced moves to the lowest priority assignment:

	CHANNEL→ JUST SERVICED	CH-0	CH-1	CH-2	CH-3
Priority → Assignments	Highest	CH-1	CH-2	CH-3	CH-0
	↑	CH-2	CH-3	CH-0	CH-1
	↓	CH-3	CH-0	CH-1	CH-2
	Lowest	CH-0	CH-1	CH-2	CH-3

Note that rotating priority will prevent any one channel from monopolizing the DMA mode; consecutive DMA cycles will service different channels if more than one channel is enabled and requesting service. There is no overhead penalty associated with this mode of operation. All DMA operations began with Channel 0 initially assigned to the highest priority for the first DMA cycle.

Extended Write Bit 5

If the EXTENDED WRITE bit is set, the duration of both the $\overline{\text{MEMW}}$ and $\overline{\text{I/OW}}$ signals is extended by activating them earlier in the DMA cycle. Data transfers within microcomputer systems proceed asynchronously to allow use of various types of memory and I/O devices with different access times. If a device cannot be accessed within a specific amount of time it returns a "not ready" indication to the 8257 that causes the 8257 to insert one or more wait states in its internal sequencing. Some devices are fast enough to be accessed without the use of wait states, but if they generate their READY response with the leading edge of the $\overline{\text{I/OW}}$ or $\overline{\text{MEMW}}$ signal (which generally occurs late in the transfer sequence), they would normally cause the 8257 to enter a wait state because it does not receive READY in time. For systems with these types of devices, the Extended Write option provides alternative timing for the I/O and memory write signals which allows the devices to return an early READY and prevents the unnecessary occurrence of wait states in the 8257, thus increasing system throughput.

TC Stop Bit 6

If the TC STOP bit is set, a channel is disabled (i.e., its enable bit is reset) after the Terminal Count (TC) output goes true, thus automatically preventing further DMA operation on that channel. The enable bit for that channel must be re-programmed to continue or begin another DMA operation. If the TC STOP bit is not set, the occurrence of the TC output has no effect on the channel enable bits. In this case, it is generally the responsibility of the peripheral to cease DMA requests in order to terminate a DMA operation.

Auto Load Bit 7

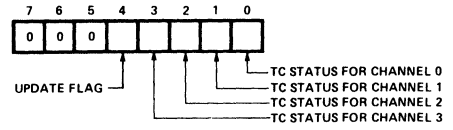
The Auto Load mode permits Channel 2 to be used for repeat block or block chaining operations, without immediate software intervention between blocks. Channel 2 registers are initialized as usual for the first data block; Channel 3 registers, however, are used to store the block re-initialization parameters (DMA starting address, terminal count and DMA transfer mode). After the first block of DMA cycles is executed by Channel 2 (i.e., after the TC output goes true), the parameters stored in the Channel 3 registers are transferred to Channel 2 during an "update" cycle. Note that the TC STOP feature, described above, has no effect on Channel 2 when the Auto Load bit is set.

If the Auto Load bit is set, the initial parameters for Channel 2 are automatically duplicated in the Channel 3 registers when Channel 2 is programmed. This permits repeat block operations to be set up with the programming of a single channel. Repeat block operations can be used in applications such as CRT refreshing. Channels 2 and 3 can still be loaded with separate values if Channel 2 is loaded before loading Channel 3. Note that in the Auto Load mode, Channel 3 is still available to the user if the Channel 3 enable bit is set, but use of this channel will change the values to be auto loaded into Channel 2 at update time. All that is necessary to use the Auto Load feature for chaining operations is to reload Channel 3 registers at the conclusion of each update cycle with the new parameters for the next data block transfer.

Each time that the 8257 enters an update cycle, the update flag in the status register is set and parameters in Channel 3 are transferred to Channel 2, non-destructively for Channel 3. The actual re-initialization of Channel 2 occurs at the beginning of the next channel 2 DMA cycle after the TC cycle. This will be the first DMA cycle of the new data block for Channel 2. The update flag is cleared at the conclusion of this DMA cycle. For chaining operations, the update flag in the status register can be monitored by the CPU to determine when the re-initialization process has been completed so that the next block parameters can be safely loaded into Channel 3.

6. Status Register

The eight-bit status register indicates which channels have reached a terminal count condition and includes the update flag described previously.



The TC status bits are set when the Terminal Count (TC) output is activated for that channel. These bits remain set until the status register is read or the 8257 is reset. The UPDATE FLAG, however, is not affected by a status register read operation. The UPDATE FLAG can be cleared by resetting the 8257, by changing to the non-auto load mode (i.e., by resetting the AUTO LOAD bit in the Mode Set register) or it can be left to clear itself at the completion of the update cycle. The purpose of the UPDATE FLAG is to prevent the CPU from inadvertently skipping a data block by overwriting a starting address or terminal count in the Channel 3 registers before those parameters are properly auto-loaded into Channel 2.

The user is cautioned against reading the TC status register and using this information to reenable channels that have not completed operation. Unless the DMA channels are inhibited a channel could reach terminal count (TC) between the status read and the mode write. DMA can be inhibited by a hardware gate on the HRQ line or by disabling channels with a mode word before reading the TC status.

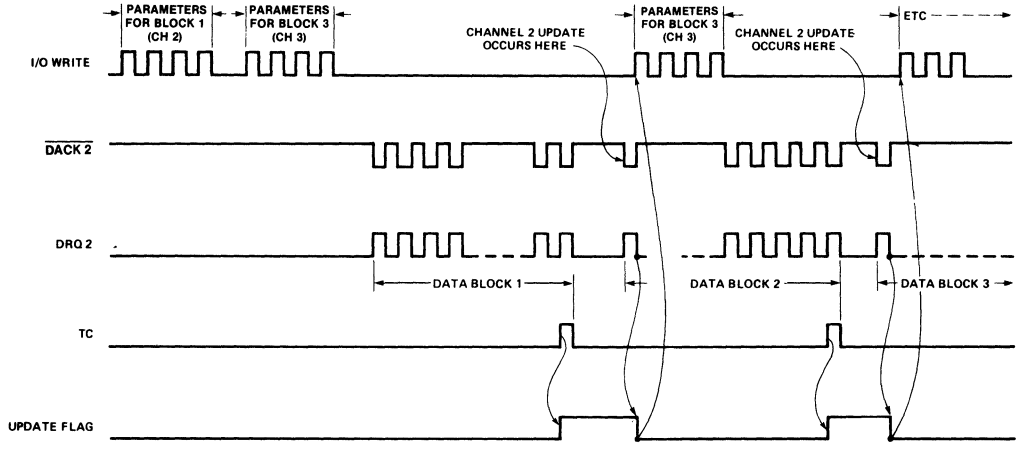


Figure 5. Autoload Timing

OPERATIONAL SUMMARY

Programming and Reading the 8257 Registers

There are four pairs of "channel registers": each pair consisting of a 16-bit DMA address register and a 16-bit terminal count register (one pair for each channel). The 8257 also includes two "general registers": one 8-bit Mode Set register and one 8-bit Status register. The registers are loaded or read when the CPU executes a write or read instruction that addresses the 8257 device and the appropriate register within the 8257. The 8228 generates the appropriate read or write control signal (generally I/OR or I/OW while the CPU places a 16-bit address on the system address bus, and either outputs the data to be written onto the system data bus or accepts the data being read from the data bus. All or some of the most significant 12 address bits A_4-A_{15} (depending on the systems memory, I/O configuration) are usually decoded to produce the chip select ($\overline{CS}$) input to the 8257. An I/O Write input (or Memory Write in memory mapped I/O configurations, described below) specifies that the addressed register is to be programmed, while an I/O Read input (or Memory Read) specifies that the addressed register is to be read. Address bit 3 specifies whether a "channel register" (A_3 = 0) or the Mode Set (program only)/Status (read only) register (A_3 = 1) is to be accessed.

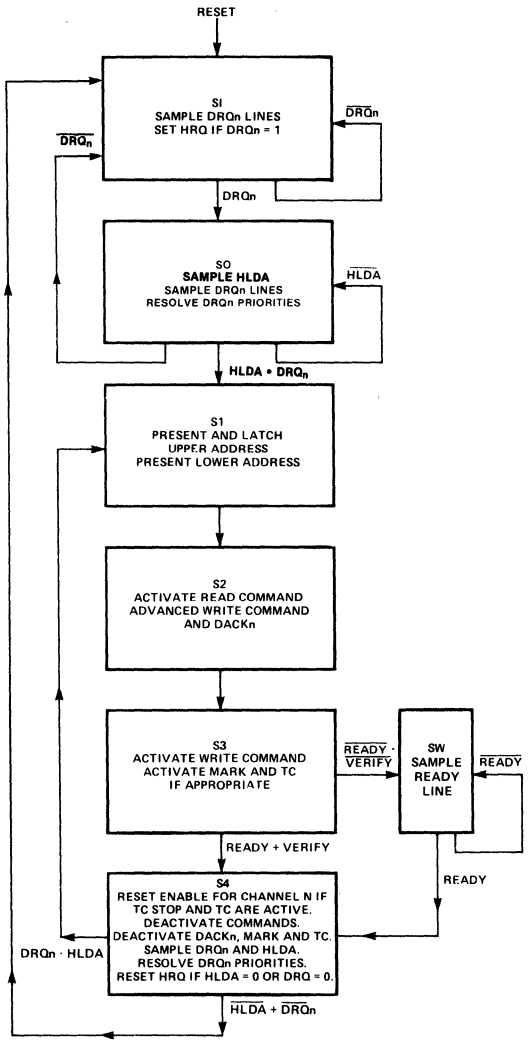
The least significant three address bits, A_0-A_2, indicate the specific register to be accessed. When accessing the Mode Set or Status register, A_0-A_2 are all zero. When accessing a channel register bit A_0 differentiates between the DMA address register (A_0 = 0) and the terminal count register (A_0 = 1), while bits A_1 and A_2 specify one of the four channels. Because the "channel registers" are 16-bits, two program instruction cycles are required to load or read an entire register. The 8257 contains a first/last (F/L) flip flop which toggles at the completion of each channel program or read operation. The F/L flip flop determines whether the upper or lower byte of the register is to be accessed. The F/L flip flop is reset by the RESET input and whenever the Mode Set register is loaded. To maintain proper synchronization when accessing the "channel registers" all channel command instruction operations should occur in pairs, with the lower byte of a register always being accessed first. Do not allow $\overline{CS}$ to clock while either $\overline{I/OR}$ or $\overline{I/OW}$ is active, as this will cause an erroneous F/L flip flop state. In systems utilizing an interrupt structure, interrupts should be disabled prior to any paired programming operations to prevent an interrupt from splitting them. The result of such a split would leave the F/L F/F in the wrong state. This problem is particularly obvious when other DMA channels are programmed by an interrupt structure.

CONTROL INPUT	$\overline{CS}$	$\overline{I/OW}$	$\overline{I/OR}$	A_3
Program Half of a Channel Register	0	0	1	0
Read Half of a Channel Register	0	1	0	0
Program Mode Set Register	0	0	1	1
Read Status Register	0	1	0	1

8257 Register Selection

REGISTER	BYTE	ADDRESS INPUTS				F/L	*BI-DIRECTIONAL DATA BUS							
		A_3	A_2	A_1	A_0		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CH-0 DMA Address	LSB	0	0	0	0	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
	MSB	0	0	0	0	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
CH-0 Terminal Count	LSB	0	0	0	1	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	MSB	0	0	0	1	1	Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8
CH-1 DMA Address	LSB	0	0	1	0	0	Same as Channel 0							
	MSB	0	0	1	0	1								
CH-1 Terminal Count	LSB	0	0	1	1	0								
	MSB	0	0	1	1	1								
CH-2 DMA Address	LSB	0	1	0	0	0	Same as Channel 0							
	MSB	0	1	0	0	1								
CH-2 Terminal Count	LSB	0	1	0	1	0								
	MSB	0	1	0	1	1								
CH-3 DMA Address	LSB	0	1	1	0	0	Same as Channel 0							
	MSB	0	1	1	0	1								
CH-3 Terminal Count	LSB	0	1	1	1	0								
	MSB	0	1	1	1	1								
MODE SET (Program only)	—	1	0	0	0	0	AL	TCS	EW	RP	EN3	EN2	EN1	EN0
STATUS (Read only)	—	1	0	0	0	0	0	0	0	UP	TC3	TC2	TC1	TC0

*A_0-A_{15}: DMA Starting Address, C_0-C_{13}: Terminal Count value (N-1), Rd and Wr: DMA Verify (00), Write (01) or Read (10) cycle selection, AL: Auto Load, TCS: TC STOP, EW: EXTENDED WRITE, RP: ROTATING PRIORITY, EN3-EN0: CHANNEL ENABLE MASK, UP: UPDATE FLAG, TC3-TC0: TERMINAL COUNT STATUS BITS.



1 DRQn refers to any DRQ line on an enabled DMA channel.

Figure 6. DMA Operation State Diagram

DMA OPERATION

Single Byte Transfers

A single byte transfer is initiated by the I/O device raising the DRQ line of one channel of the 8257. If the channel is enabled, the 8257 will output a HRQ to the CPU. The 8257 now waits until a HLDA is received insuring that the system bus is free for its use. Once HLDA is received the $\overline{DACK}$ line for the requesting channel is activated (LOW). The $\overline{DACK}$ line acts as a chip select for the requesting I/O device. The 8257 then generates the read and write commands and byte transfer occurs between the selected I/O device and memory. After the transfer is complete, the $\overline{DACK}$ line is set HIGH and the HRQ line is set LOW to indicate to the CPU that the bus is now free for use. DRQ must remain HIGH until $\overline{DACK}$ is issued to be recognized and must go LOW before S4 of the transfer sequence to prevent another transfer from occuring. (See timing diagram.)

Consecutive Transfers

If more than one channel requests service simultaneously, the transfer will occur in the same way a burst does. No overhead is incurred by switching from one channel to another. In each S4 the DRQ lines are sampled and the highest priority request is recognized during the next transfer. A burst mode transfer in a lower priority channel will be overridden by a higher priority request. Once the high priority transfer has completed control will return to the lower priority channel if its DRQ is still active. No extra cycles are needed to execute this sequence and the HRQ line remains active until all DRQ lines go LOW.

Control Override

The continuous DMA transfer mode described above can be interrupted by an external device by lowering the HLDA line. After each DMA transfer the 8257 samples the HLDA line to insure that it is still active. If it is not active, the 8257 completes the current transfer, releases the HRQ line (LOW) and returns to the idle state. If DRQ lines are still active the 8257 will raise the HRQ line in the third cycle and proceed normally. (See timing diagram.)

Not Ready

The 8257 has a Ready input similar to the 8080A and the 8085A. The Ready line is sampled in State 3. If Ready is LOW the 8257 enters a wait state. Ready is sampled during every wait state. When Ready returns HIGH the 8257 proceeds to State 4 to complete the transfer. Ready is used to interface memory or I/O devices that cannot meet the bus set up times required by the 8257.

Speed

The 8257 uses four clock cycles to transfer a byte of data. No cycles are lost in the master to master transfer maximizing bus efficiency. A 2MHz clock input will allow the 8257 to transfer at a rate of 500K bytes/second.

Memory Mapped I/O Configurations

The 8257 can be connected to the system bus as a memory device instead of as an I/O device for memory mapped I/O configurations by connecting the system memory control lines to the 8257's I/O control lines and the system I/O control lines to the 8257's memory control lines.

This configuration permits use of the 8080's considerably larger repertoire of memory instructions when reading or loading the 8257's registers. Note that with this connection, the programming of the Read (bit 15) and Write (bit 14) bits in the terminal count register will have a different meaning:

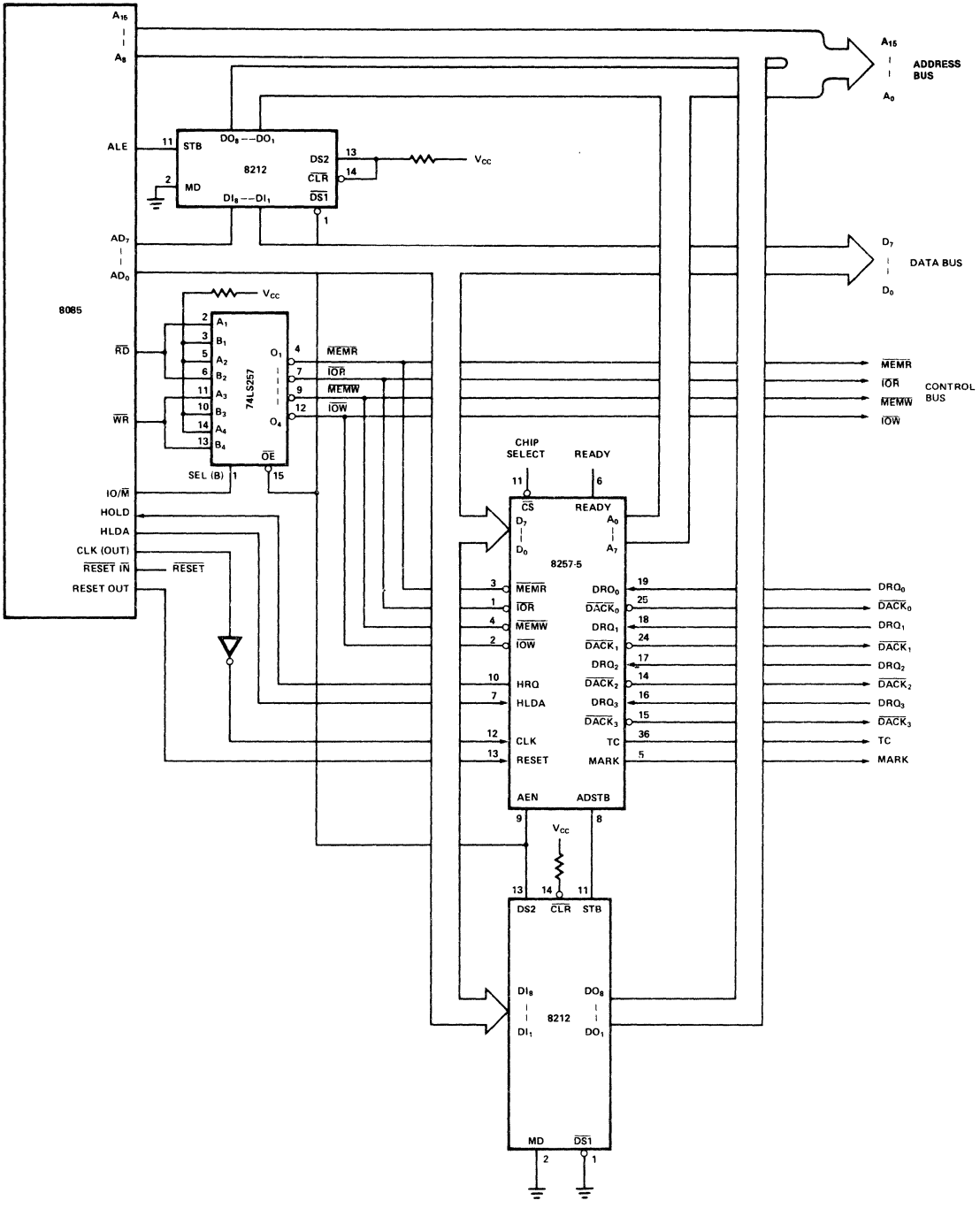


Figure 11. Detailed System Interface Schematic

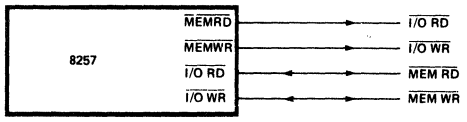


Figure 7. System Interface for Memory Mapped I/O

BIT 15 READ	BIT 14 WRITE	
0	0	DMA Verify Cycle
0	1	DMA Read Cycle
1	0	DMA Write Cycle
1	1	Illegal

Figure 8. TC Register for Memory Mapped I/O Only

SYSTEM APPLICATION EXAMPLES

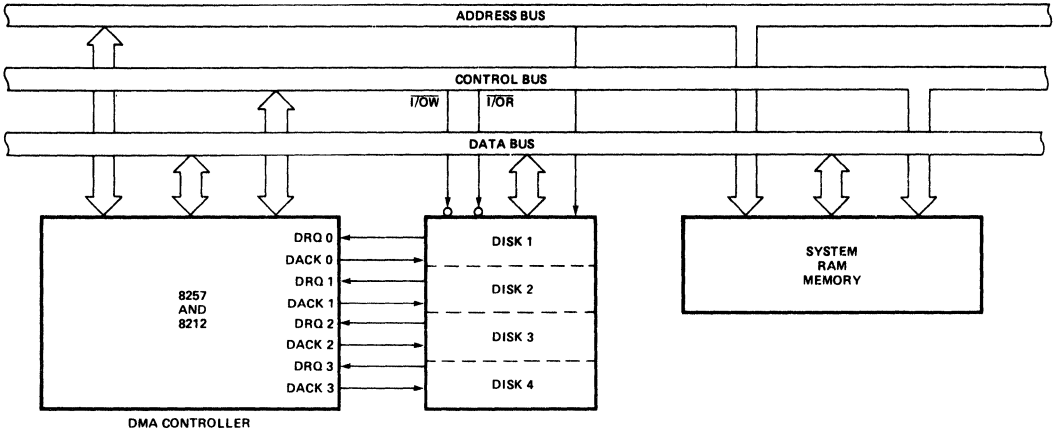


Figure 9. Floppy Disk Controller (4 Drives)

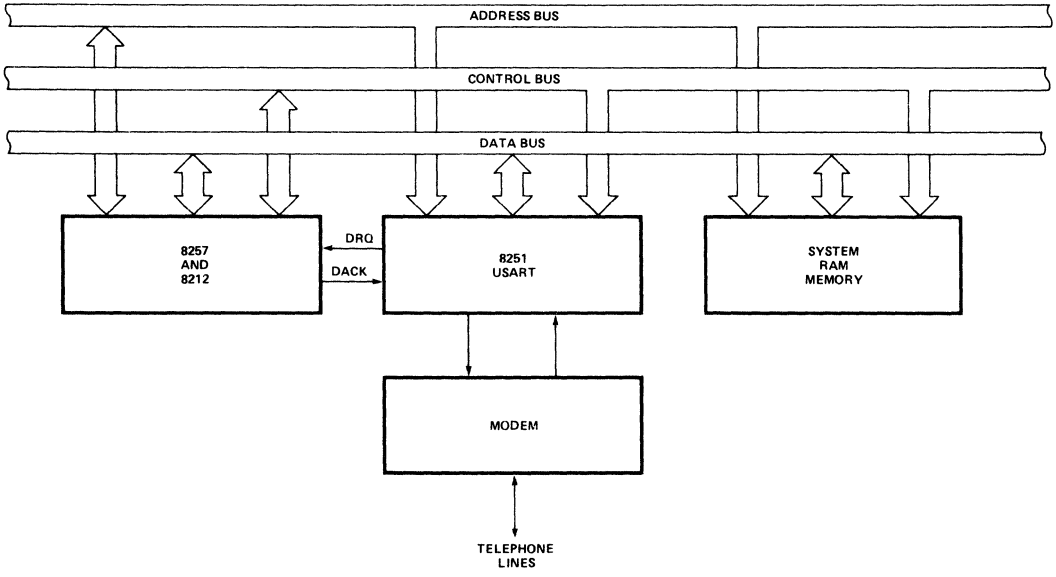


Figure 10. High-Speed Communication Controller

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	V_{CC}+.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	Volts	I_{OH}=-150μA for AB, DB and AEN I_{OH}=-80μA for others
V_{HH}	HRQ Output High Voltage	3.3	V_{CC}	Volts	I_{OH} = -80μA
I_{CC}	V_{CC} Current Drain		120	mA	
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Leakage During Float		±10	μA	V_{OUT} = V_{CC} to 0V

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS: PERIPHERAL (SLAVE) MODE

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%; GND = 0V (Note 1).

8080 Bus Parameters

Read Cycle:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{AR}	Adr or $\overline{CS}\downarrow$ Setup to $\overline{RD}\downarrow$	0		0		ns	
T_{RA}	Adr or $\overline{CS}\uparrow$ Hold from $\overline{RD}\uparrow$	0		0		ns	
T_{RD}	Data Access from $\overline{RD}\downarrow$	0	300	0	200	ns	(Note 2)
T_{DF}	DB→Float Delay from $\overline{RD}\uparrow$	20	150	20	100	ns	
T_{RR}	$\overline{RD}$ Width	250		250		ns	

Write Cycle:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{AW}	Adr Setup to $\overline{WR}\downarrow$	20		20		ns	
T_{WA}	Adr Hold from $\overline{WR}\uparrow$	0		0		ns	
T_{DW}	Data Setup to $\overline{WR}\uparrow$	200		200		ns	
T_{WD}	Data Hold from $\overline{WR}\uparrow$	0		0		ns	
T_{WW}	$\overline{WR}$ Width	200		200		ns	

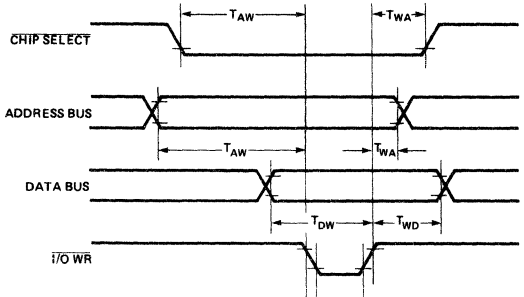
Other Timing:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{RSTW}	Reset Pulse Width	300		300		ns	
T_{RSTD}	Power Supply↑ (V_{CC}) Setup to Reset↓	500		500		μs	
T_r	Signal Rise Time		20		20	ns	
T_f	Signal Fall Time		20		20	ns	
T_{RSTS}	Reset to First $\overline{I/O}\overline{WR}$	2		2		t_{CY}	

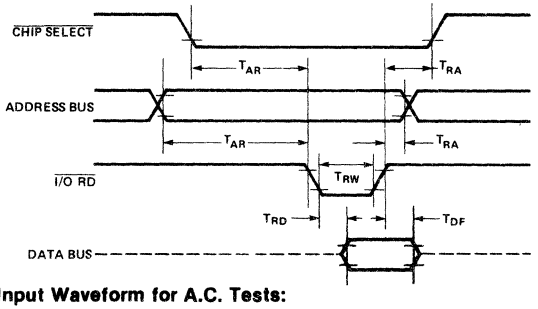
Notes: 1. All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V
Output "1" at 2.0V, "0" at 0.8V
2. 8257: C_L = 100pF, 8257-5: C_L = 150pF.

8257 PERIPHERAL MODE TIMING DIAGRAMS

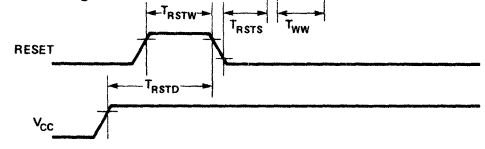
Write Timing:



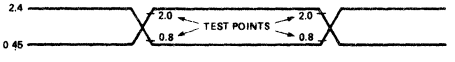
Read Timing:



Reset Timing:



Input Waveform for A.C. Tests:



A.C. CHARACTERISTICS: DMA (MASTER) MODE $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, GND = 0V.

Timing Requirements

SYMBOL	PARAMETER	8257		8257-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
T_{CY}	Cycle Time (Period)	0.320	4	0.320	4	μs
T_θ	Clock Active (High)	120	$.8T_{CY}$	80	$.8T_{CY}$	ns
T_{QS}	DRQ↑ Setup to θ↓ (SI, S4)	120		30		ns
T_{QH}	DRQ↓ Hold from HLDA↑[4]	0		0		ns
T_{HS}	HLDA↑ or ↓Setup to θ↓(SI, S4)	100		100		ns
T_{RS}	READY Setup Time to θ↑ (S3, Sw)	30		30		ns
T_{RH}	READY Hold Time from θ↑ (S3, Sw)	20		20		ns

Note: 4. Tracking Parameter.

Tracking Parameters

Signals labeled as Tracking Parameters (footnotes 4-7 under A.C. Specifications) are signals that follow similar paths through the silicon die. The propagation speed of these signals varies in the manufacturing process but the relationship between all these parameters is constant. The variation is less than or equal to 50 ns.

Suppose the following timing equation is being evaluated,

$$T_{A(MIN)} + T_{B(MAX)} \leq 150 \text{ ns}$$

and only minimum specifications exist for T_A and T_B. If $T_{A(MIN)}$ is used, and if T_A and T_B are tracking parameters, $T_{B(MAX)}$ can be taken as $T_{B(MIN)} + 50$ ns.

$$T_{A(MIN)} + (T_{B(MIN)}^* + 50 \text{ ns}) \leq 150 \text{ ns}$$

*if T_A and T_B are tracking parameters

A.C. CHARACTERISTICS: DMA (MASTER) MODE $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, GND = 0V

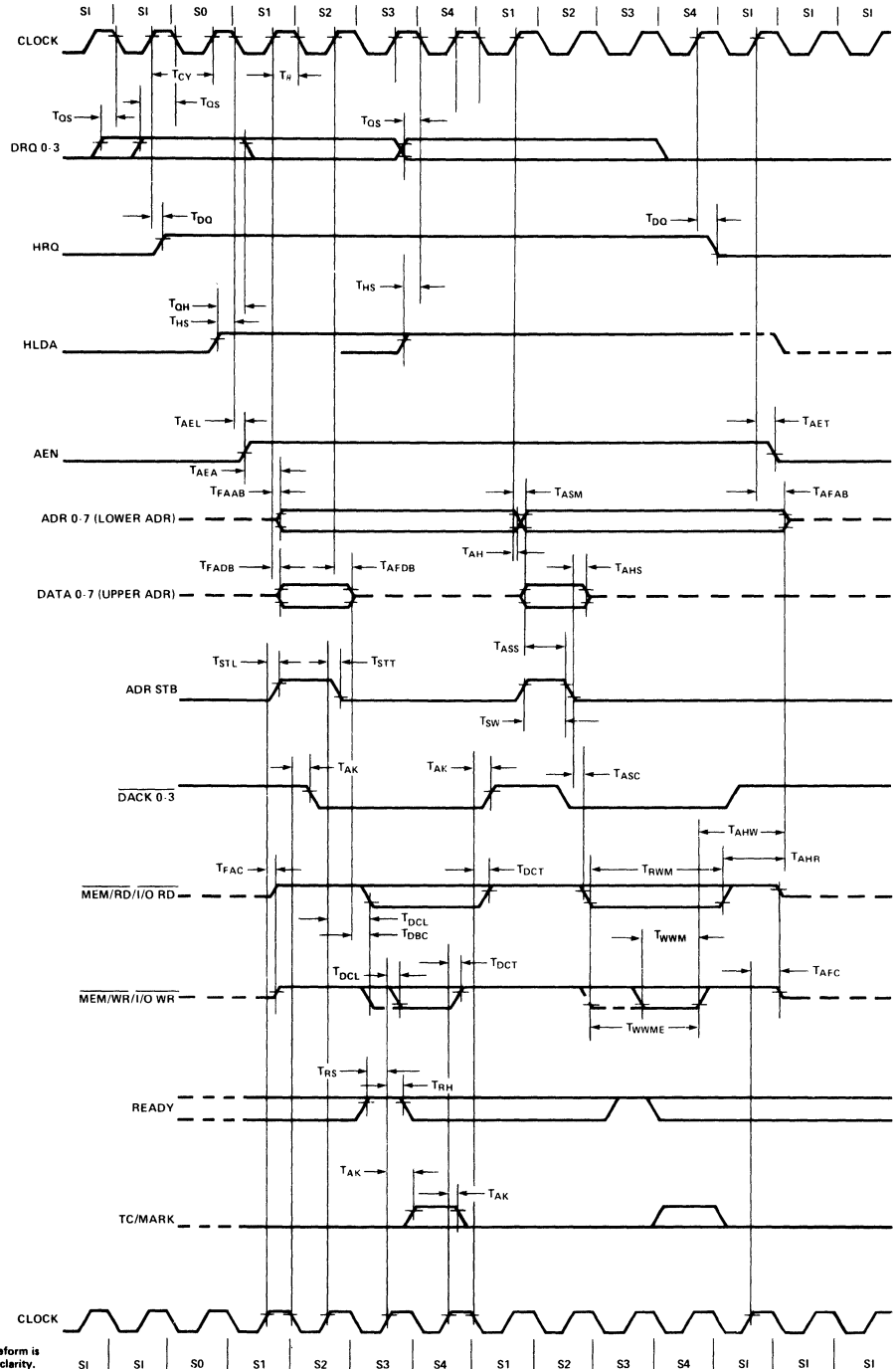
Timing Responses

SYMBOL	PARAMETER	8257		8257-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
T_{DQ}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 2.0V)[1]		160		160	ns
T_{DQ1}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 3.3V)[3]		250		250	ns
T_{AEL}	AEN↑ Delay from θ↓(S1)[1]		300		300	ns
T_{AET}	AEN↓ Delay from θ↑(SI)[1]		200		200	ns
T_{AEA}	Adr(AB)(Active) Delay from AEN↑(S1)[4]	20		20		ns
T_{FAAB}	Adr(AB)(Active) Delay from θ↑(S1)[2]		250		250	ns
T_{AFAB}	Adr(AB)(Float) Delay from θ↑(SI)[2]		150		150	ns
T_{ASM}	Adr(AB)(Stable) Delay from θ↑(S1)[2]		250		250	ns
T_{AH}	Adr(AB)(Stable) Hold from θ↑(S1)[2]	T_{ASM}-50		T_{ASM}-50		ns
T_{AHR}	Adr(AB)(Valid) Hold from $\overline{Rd}$↑(S1,SI)[4]	60		60		ns
T_{AHW}	Adr(AB)(Valid) Hold from $\overline{Wr}$↑(S1,SI)[4]	300		300		ns
T_{FADB}	Adr(DB)(Active) Delay from θ↑(S1)[2]		300		300	ns
T_{AFDB}	Adr(DB)(Float) Delay from θ↑(S2)[2]	T_{STT}+20	250	T_{STT}+20	170	ns
T_{ASS}	Adr(DB) Setup to AdrStb↓(S1-S2)[4]	100		100		ns
T_{AHS}	Adr(DB)(Valid) Hold from AdrStb↓(S2)[4]	50		50		ns
T_{STL}	AdrStb↑ Delay from θ↑(S1)[1]		200		200	ns
T_{STT}	AdrStb↓ Delay from θ↑(S2)[1]		140		140	ns
T_{SW}	AdrStb Width (S1-S2)[4]	T_{CY}-100		T_{CY}-100		ns
T_{ASC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from AdrStb↓(S2)[4]	70		70		ns
T_{DBC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from Adr(DB) (Float)(S2)[4]	20		20		ns
T_{AK}	DACK↑ or ↓Delay from θ↓(S2,S1) and TC/Mark↑ Delay from θ↑(S3) and TC/Mark↓ Delay from θ↑(S4)[1,5]		250		250	ns
T_{DCL}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from θ↑(S2) and $\overline{Wr}$↓ Delay from θ↑(S3)[2,6]		200		200	ns
T_{DCT}	$\overline{Rd}$↑ Delay from θ↓(S1,SI) and $\overline{Wr}$↑ Delay from θ↑(S4)[2,7]		200		200	ns
T_{FAC}	$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑(S1)[2]		300		300	ns
T_{AFC}	$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑(SI)[2]		150		150	ns
T_{RWM}	$\overline{Rd}$ Width (S2-S1 or SI)[4]	$2T_{CY} + T_\theta$-50		$2T_{CY} + T_\theta$-50		ns
T_{WWM}	$\overline{Wr}$ Width (S3-S4)[4]	T_{CY}-50		T_{CY}-50		ns
T_{WWME}	$\overline{Wr}$(Ext) Width (S2-S4)[4]	$2T_{CY}$-50		$2T_{CY}$-50		ns

Notes: 1. Load = 1 TTL. 2. Load = 1 TTL + 50pF. 3. Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V. 4. Tracking Parameter. 5. $\Delta T_{AK} < 50$ ns. 6. $\Delta T_{DCL} < 50$ ns. 7. $\Delta T_{DCT} < 50$ ns.

DMA MODE WAVEFORMS

CONSECUTIVE CYCLES AND BURST MODE SEQUENCE



NOTE: The clock waveform is duplicated for clarity. The 8257 requires only one clock input.

Figure 12. Consecutive Cycles and Burst Mode Sequence

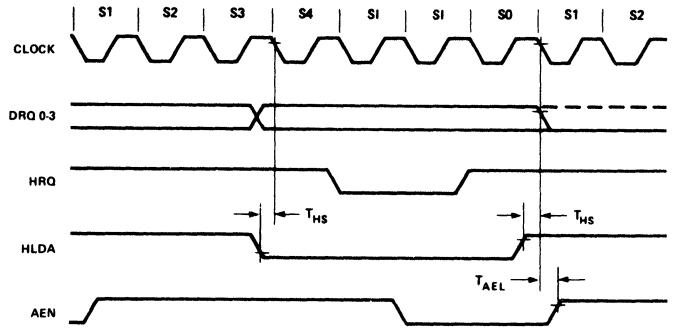


Figure 13. Control Override Sequence

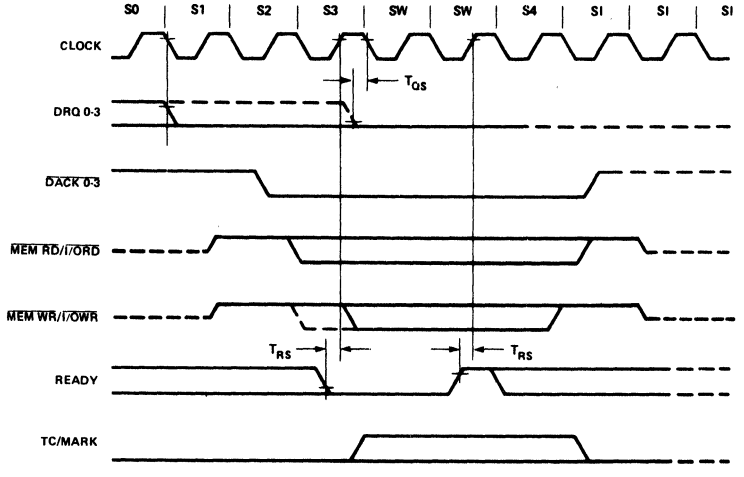


Figure 14. Not Ready Sequence

8259A
PROGRAMMABLE INTERRUPT CONTROLLER

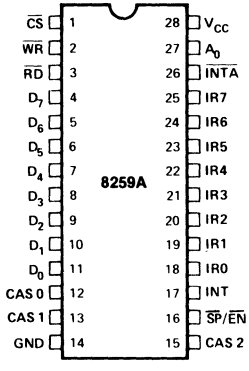
- **MCS-86™ Compatible**
- **MCS-80/85™ Compatible**
- **Eight-Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes**
- **Individual Request Mask Capability**
- **Single +5V Supply (No Clocks)**
- **28-Pin Dual-In-Line Package**

The Intel® 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel® 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).

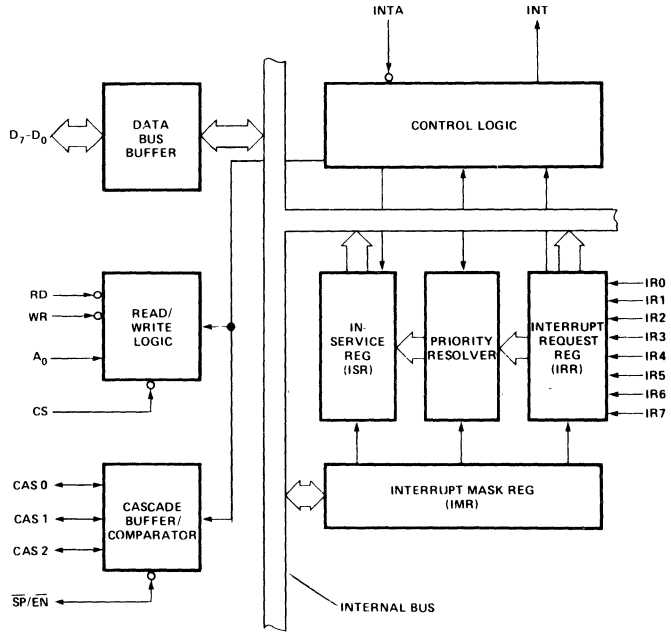
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS2-CAS0	CASCADE LINES
$\overline{SP}/\overline{EN}$	SLAVE PROGRAM INPUT/ENABLE
INT	INTERRUPT OUTPUT
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE INPUT
IR0-IR7	INTERRUPT REQUEST INPUTS

BLOCK DIAGRAM



MCS-80/85

INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

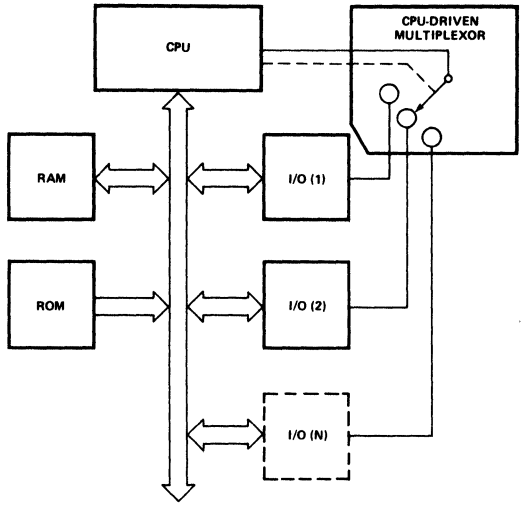
The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

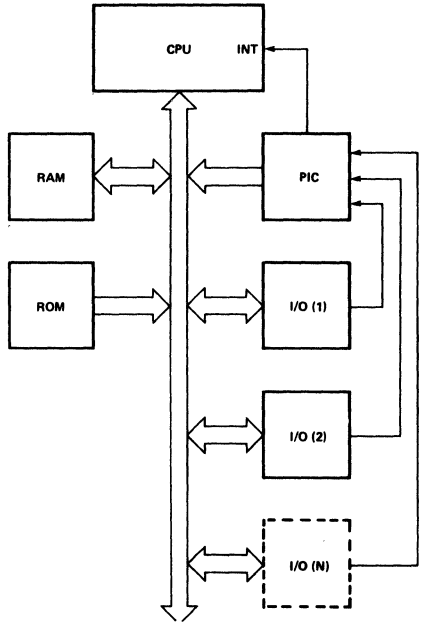
8259A BASIC FUNCTIONAL DESCRIPTION

GENERAL

The 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.



Polled Method



Interrupt Method

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

$\overline{INTA}$ (INTERRUPT ACKNOWLEDGE)

$\overline{INTA}$ pulses will cause the 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 8259A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

$\overline{CS}$ (CHIP SELECT)

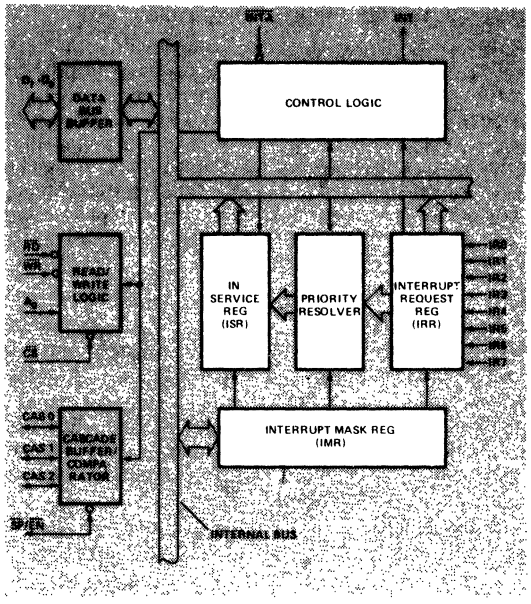
A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (WRITE)

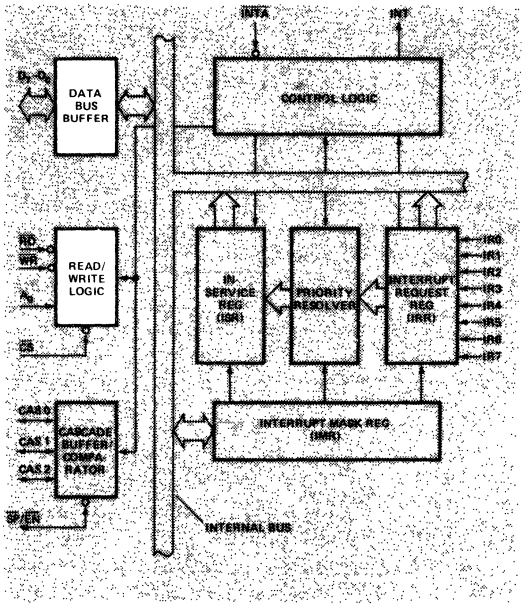
A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 8259A.

$\overline{RD}$ (READ)

A LOW on this input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.



8259A Block Diagram



8259A Block Diagram

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 8259A".)

INTERRUPT SEQUENCE

The powerful features of the 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

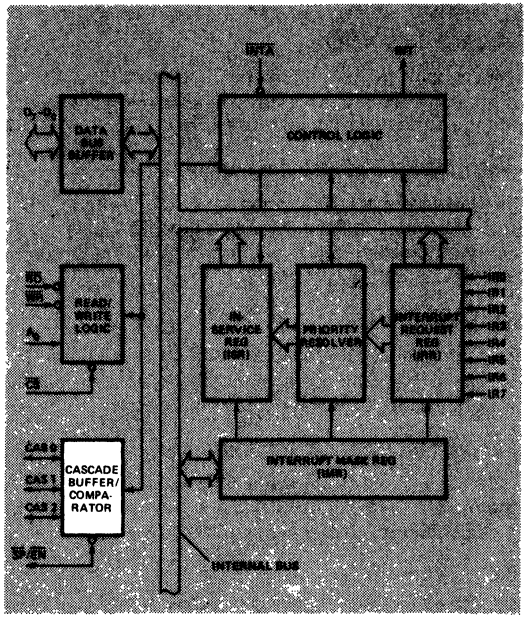
The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{INTA}$ pulses to be sent to the 8259A from the CPU group.
6. These two $\overline{INTA}$ pulses allow the 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

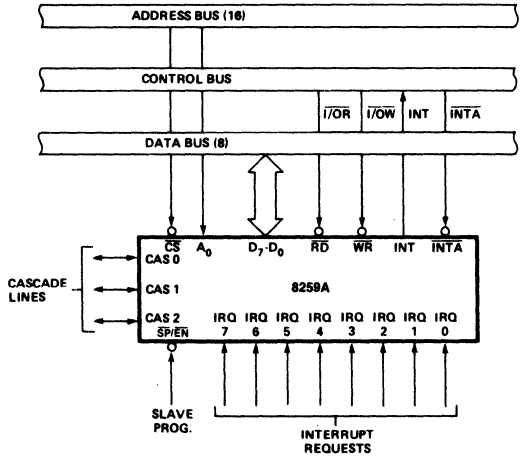
The events occurring in an MCS-86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive the Data Bus during this cycle.
5. The MCS-86 CPU will initiate a second $\overline{INTA}$ pulse. During this pulse, the 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration) the 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.



8259A Block Diagram



8259A Interface to Standard System Bus

INTERRUPT SEQUENCE OUTPUTS

MCS-80/85 SYSTEM

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the 8259A. When Interval = 8 only A_6 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8 – A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

MCS-86 SYSTEM

MCS-86 mode is similar to MCS-80 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80/85 systems in that the 8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the $\overline{INTA}$ pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in MCS-86 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in MCS-86 mode):

Content of Interrupt Vector Byte for MCS-86 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	A15	A14	A13	A12	A11	1	1	1
IR6	A15	A14	A13	A12	A11	1	1	0
IR5	A15	A14	A13	A12	A11	1	0	1
IR4	A15	A14	A13	A12	A11	1	0	0
IR3	A15	A14	A13	A12	A11	0	1	1
IR2	A15	A14	A13	A12	A11	0	1	0
IR1	A15	A14	A13	A12	A11	0	0	1
IR0	A15	A14	A13	A12	A11	0	0	0

PROGRAMMING THE 8259A

The 8259A accepts two types of command words generated by the CPU:

1. *Initialization Command Words (ICWs):* Before normal operation can begin, each 8259A in the system must be brought to a starting point — by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses. This sequence is described in Figure 1.

2. *Operation Command Words (OCWs):* These are the command words which command the 8259A to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 8259A anytime after initialization.

INITIALIZATION

GENERAL

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The Interrupt Mask Register is cleared.

b. IR 7 input is assigned priority 7.

c. The slave mode address is set to 7.

d. Special Mask Mode is cleared and Status Read is set to IRR.

e. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80/85 system, non SFNM).

***Note:** Master/Slave in ICW4 is only used in the buffered mode.

A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or Interrupting Level → DATA BUS (Note 1)
1			0	1	0	IMR → DATA BUS
						OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	DATA BUS → OCW2
0	0	1	1	0	0	DATA BUS → OCW3
0	1	X	1	0	0	DATA BUS → ICW1
1	X	X	1	0	0	DATA BUS → OCW1, ICW2, ICW3, ICW4 (Note 2)
						DISABLE FUNCTION
X	X	X	1	1	0	DATA BUS — 3-STATE (NO OPERATION)
X	X	X	X	X	1	DATA BUS — 3-STATE (NO OPERATION)

Notes: 1. Selection of IRR, ISR or Interrupting Level is based on the content of OCW3 written before the READ operation.
2. On-chip sequencer logic queues these commands into proper sequence.

8259A Basic Operation

INITIALIZATION COMMAND WORDS 1 AND 2 (ICW1, ICW2)

A_5-A_{15}: *Page starting address of service routines.* In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the 8259A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the 8259A, while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an MCS-86 system A_{15}-A_{11} are inserted in the five most significant bits of the vectoring byte and the 8259A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 8259A in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for MCS-86 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$ = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for MCS-86) are released by it on the Data Bus.

INITIALIZATION COMMAND WORD 4 (ICW4)

SFNM: If SFNM = 1 the special fully nested mode is programmed.

BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 8259A is programmed to be a master, M/S = 0 means the 8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 8259A for MCS-80/85 system operation, μPM = 1 sets the 8259A for MCS-86 system operation.

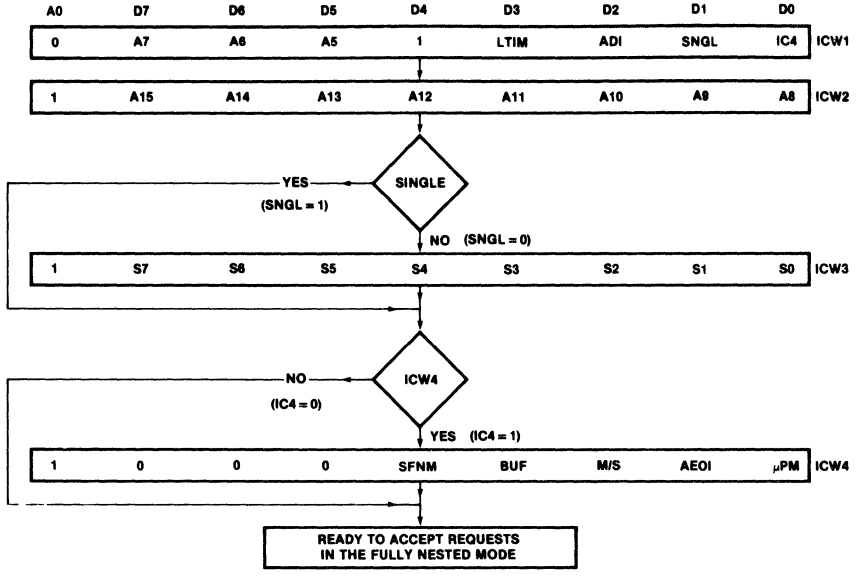
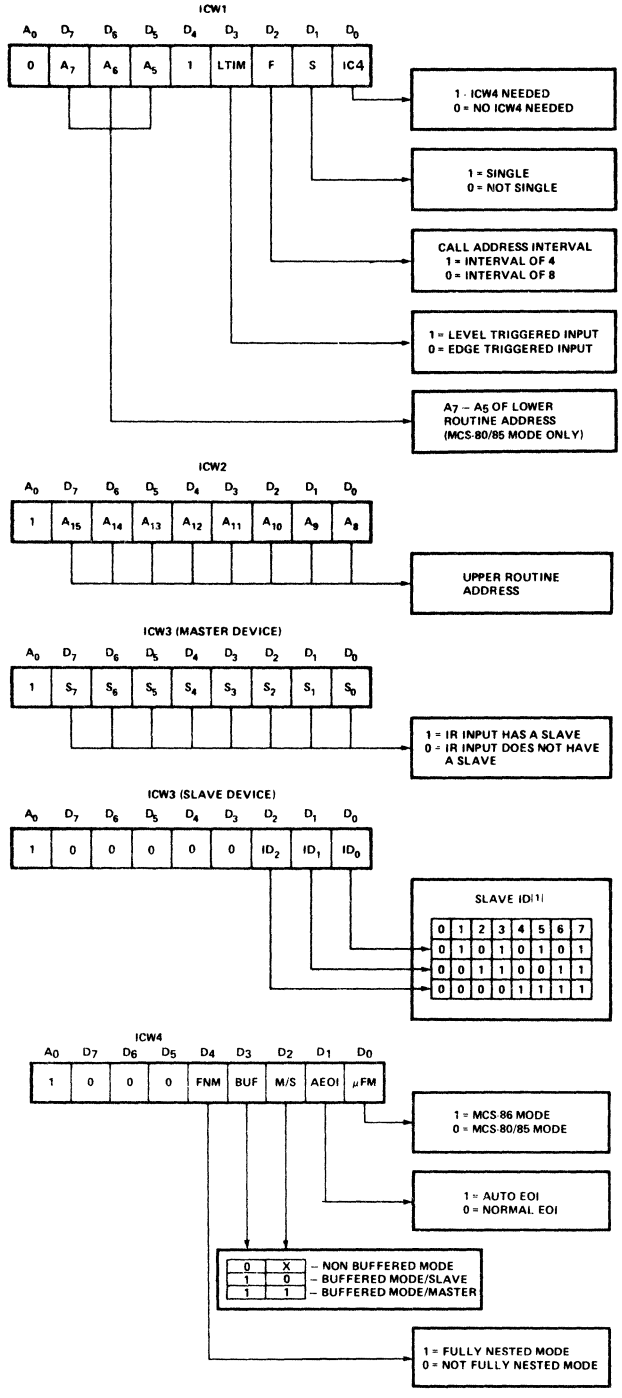


Figure 1. Initialization Sequence



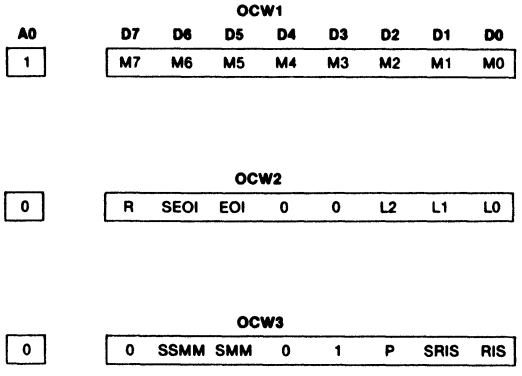
NOTE 1: SLAVED ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.
NOTE 2: X INDICATED "DON'T CARE".

Initialization Command Word Format

OPERATION COMMAND WORDS (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the 8259A operation, a selection of algorithms can command the 8259A to operate in various modes through the Operation Command Words (OCWs).

OPERATION CONTROL WORDS (OCWs)



OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). $M_7 - M_0$ represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

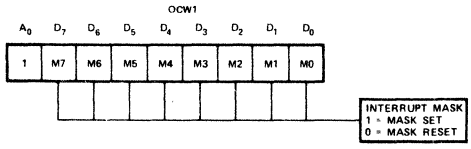
R, SEOI, EOI — These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

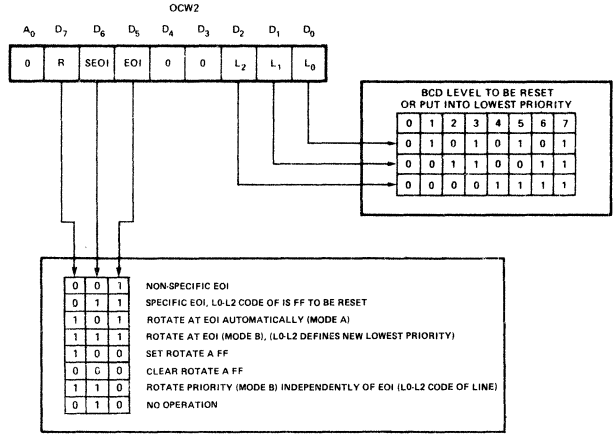
L_2, L_1, L_0 — These bits determine the interrupt level acted upon when the SEOI bit is active.

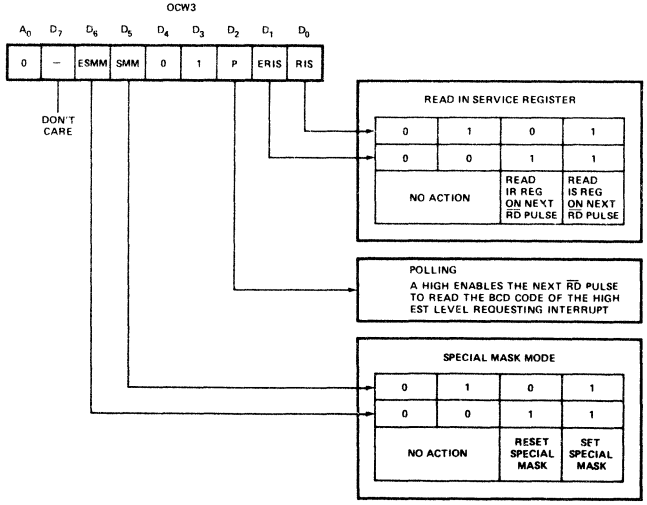
OPERATION CONTROL WORD 3 (OCW3)

ESMM — Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0 the SMM bit becomes a "don't care".

SMM — Special Mask Mode. If ESMM = 1 and SMM = 1 the 8259A will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the 8259A will revert to normal mask mode. When ESMM = 0, SMM has no effect.







Operation Command Word Format

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level *and enables* interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

BUFFERED MODE

When the 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the 8259A's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority form 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal Interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

POLL

In this mode the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by programmer initiative using a Poll command.

The Poll command is issued by setting P = "1" in OCW3. The 8259A treats the next $\overline{RD}$ pulse to the 8259A (i.e., $\overline{RD} = 0$, $\overline{CS} = 0$) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	–	–	–	–	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{INTA}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 8259A before returning from a service routine (EOI command). An EOI command must be issued twice, once for the master and once for the corresponding slave if slaves are in use.

There are two forms of EOI command: Specific and Non-Specific. When the 8259A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 8259A will automatically reset the highest IS bit of those that are set, since in the nested mode the highest IS level was necessarily the last level acknowledged and serviced.

However, when a mode is used which may disturb the fully nested structure, the 8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt (SEOI) must be issued which includes as part of the command the IS level to be reset. EOI is issued whenever EOI = 1, in OCW2, where L0-L2 is the binary level of the IS bit to be reset. Note that although the Rotate command can be issued together with an EOI where EOI = 1, it is not necessarily tied to it.

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 8259A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

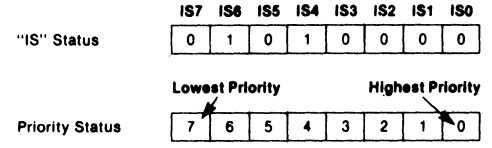
If AEOI = 1 in ICW4, then the 8259A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 8259A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in MCS-86). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 8259A.

To achieve automatic rotation (Rotate Mode A) within AEOI, there is a special rotate flip-flop. It is set by OCW2 with R = 1, SEOI = 0, EOI = 0, and cleared with R = 0, SEOI = 0, EOI = 0.

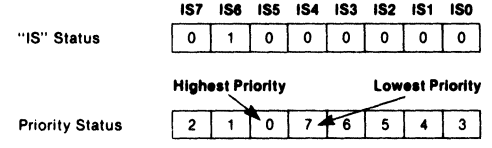
ROTATING PRIORITY MODE A (AUTOMATIC ROTATION) FOR EQUAL PRIORITY DEVICES

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most *once*. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)



After Rotate (IR4 was serviced, all other priorities rotated correspondingly)



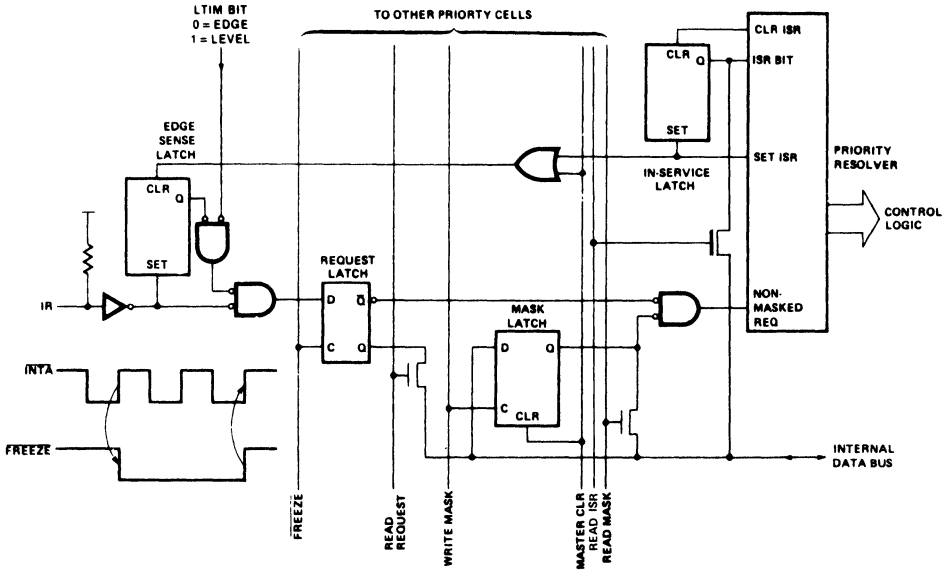
The Rotate command mode A is issued in OCW2 where: R = 1, EOI = 1, SEOI = 0. Internal status is updated by an End of Interrupt (EOI or AEOI) command. If R = 1, EOI = 0, SEOI = 0, a "Rotate-A" flip-flop is set. This is useful in AEOI, and described under Automatic End of Interrupt.

ROTATING PRIORITY MODE B (ROTATION BY SOFTWARE)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Rotate command is issued in OCW2 where: R = 1, SEOI = 1; L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command or independently.



NOTES

1. MASTER CLEAR ACTIVE ONLY DURING ICW1
2. FREEZE/ IS ACTIVE DURING $\overline{\text{INTA}}$/ AND POLL SEQUENCES ONLY
3. TRUTH TABLE FOR D-LATCH

C	D	Q	OPERATION
1	Di	Di	FOLLOW
0	X	Qn-1	HOLD

Priority Cell — Simplified Logic Diagram

LEVEL TRIGGERED MODE

This mode is programmed using bit 3 in ICW1.

If LTIM ='1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The above figure shows a conceptual circuit to give the reader an understanding of the level sensitive and edge sensitive input circuitry of the 8259A. Be sure to note that the request latch is a transparent D type latch.

READING THE 8259A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read by issuing a suitable OCW3 and reading with $\overline{\text{RD}}$.

Interrupt Mask Register: 8-bit register whose content specifies the interrupt request lines being masked. acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the $\overline{\text{RD}}$ pulse, a $\overline{\text{WR}}$ pulse is issued with OCW3 (ERIS = 1, RIS = 0.)

The ISR can be read in a similar mode when ERIS = 1, RIS = 1 in the OCW3.

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{\text{RD}}$ is active and A0 = 1.

Polling overrides status read when P = 1, ERIS = 1 in OCW3.

SUMMARY OF 8259A INSTRUCTION SET

Inst. #	Mnemonic	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description
1	ICW1 A	0	A7	A6	A5	1	0	1	1	0	Format = 4, single, edge triggered
2	ICW1 B	0	A7	A6	A5	1	1	1	1	0	Format = 4, single, level triggered
3	ICW1 C	0	A7	A6	A5	1	0	1	0	0	Byte 1 Initialization — Format = 4, not single, edge triggered
4	ICW1 D	0	A7	A6	A5	1	1	1	0	0	Format = 4, not single, level triggered
5	ICW1 E	0	A7	A6	0	1	0	0	1	0	No ICW4 Required — Format = 8, single, edge triggered
6	ICW1 F	0	A7	A6	0	1	1	0	1	0	Format = 8, single, level triggered
7	ICW1 G	0	A7	A6	0	1	0	0	0	0	Format = 8, not single, edge triggered
8	ICW1 H	0	A7	A6	0	1	1	0	0	0	Format = 8, not single, level triggered
9	ICW1 I	0	A7	A6	A5	1	0	1	1	1	Format = 4, single, edge triggered
10	ICW1 J	0	A7	A6	A5	1	1	1	1	1	Format = 4, single, level triggered
11	ICW1 K	0	A7	A6	A5	1	0	1	0	1	Byte 1 Initialization — Format = 4, not single, edge triggered
12	ICW1 L	0	A7	A6	A5	1	1	1	0	1	Format = 4, not single, level triggered
13	ICW1 M	0	A7	A6	0	1	0	0	1	1	ICW4 Required — Format = 8, single, edge triggered
14	ICW1 N	0	A7	A6	0	1	1	0	1	1	Format = 8, single, level triggered
15	ICW1 O	0	A7	A6	0	1	0	0	0	1	Format = 8, not single, edge triggered
16	ICW1 P	0	A7	A6	0	1	1	0	0	1	Format = 8, not single, level triggered
17	ICW2	1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization
18	ICW3 M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization — master
19	ICW3 S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization — slave
20	ICW4 A	1	0	0	0	0	0	0	0	0	No action, redundant
21	ICW4 B	1	0	0	0	0	0	0	0	1	Non-buffered mode, no AEOI, MCS-86
22	ICW4 C	1	0	0	0	0	0	0	1	0	Non-buffered mode, AEOI, MCS-80/85
23	ICW4 D	1	0	0	0	0	0	0	1	1	Non-buffered mode, AEOI, MCS-86
24	ICW4 E	1	0	0	0	0	0	1	0	0	No action, redundant
25	ICW4 F	1	0	0	0	0	0	1	0	1	Non-buffered mode, no AEOI, MCS-86
26	ICW4 G	1	0	0	0	0	0	1	1	0	Non-buffered mode, AEOI, MCS-80/85
27	ICW4 H	1	0	0	0	0	0	1	1	1	Non-buffered mode, AEOI, MCS-86
28	ICW4 I	1	0	0	0	0	1	0	0	0	Buffered mode, slave, no AEOI, MCS-80/85
29	ICW4 J	1	0	0	0	0	1	0	0	1	Buffered mode, slave, no AEOI, MCS-86
30	ICW4 K	1	0	0	0	0	1	0	1	0	Buffered mode, slave, AEOI, MCS-80/85
31	ICW4 L	1	0	0	0	0	1	0	1	1	Buffered mode, slave, AEOI, MCS-86
32	ICW4 M	1	0	0	0	0	1	1	0	0	Buffered mode, master, no AEOI, MCS-80/85
33	ICW4 N	1	0	0	0	0	1	1	0	1	Buffered mode, master, no AEOI, MCS-86
34	ICW4 O	1	0	0	0	0	1	1	1	0	Buffered mode, master, AEOI, MCS-80/85
35	ICW4 P	1	0	0	0	0	1	1	1	1	Buffered mode, master, AEOI, MCS-86
36	ICW4 NA	1	0	0	0	1	0	0	0	0	Fully nested mode, MCS-80, non-buffered, no AEOI
37	ICW4 NB	1	0	0	0	1	0	0	0	1	ICW4 NB through ICW4 ND are identical to ICW4 B through ICW4 D with the addition of Fully Nested Mode
38	ICW4 NC	1	0	0	0	1	0	0	1	0	
39	ICW4 ND	1	0	0	0	1	0	0	1	1	
40	ICW4 NE	1	0	0	0	1	0	1	0	0	Fully Nested Mode, MCS-80/85, non-buffered, no AEOI
41	ICW4 NF	1	0	0	0	1	0	1	0	1	ICW4 NF through ICW4 NP are identical to ICW4 F through ICW4 P with the addition of Fully Nested Mode
42	ICW4 NG	1	0	0	0	1	0	1	1	0	
43	ICW4 NH	1	0	0	0	1	0	1	1	1	
44	ICW4 NI	1	0	0	0	1	1	0	0	0	
45	ICW4 NJ	1	0	0	0	1	1	0	0	1	
46	ICW4 NK	1	0	0	0	1	1	0	1	0	
47	ICW4 NL	1	0	0	0	1	1	0	1	1	
48	ICW4 NM	1	0	0	0	1	1	1	0	0	
49	ICW4 NN	1	0	0	0	1	1	1	0	1	
50	ICW4 NO	1	0	0	0	1	1	1	1	0	
51	ICW4 NP	1	0	0	0	1	1	1	1	1	
52	OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask register, read mask register
53	OCW2 E	0	0	0	1	0	0	0	0	0	Non-specific EOI
54	OCW2 SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI. L0-L2 code of IS FF to be reset
55	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI Automatically (Mode A)
56	OCW2 RSE	0	1	1	1	0	0	L2	L1	L0	Rotate at EOI (mode B). L0-L2 code of line
57	OCW2 R	0	1	0	0	0	0	0	0	0	Set Rotate A FF
58	OCW2 CR	0	0	0	0	0	0	0	0	0	Clear Rotate A FF
59	OCW2 RS	0	1	1	0	0	0	L2	L1	L0	Rotate priority (mode B) independently of EOI
60	OCW3 P	0	0	0	0	0	1	1	0	0	Poll mode
61	OCW3 RIS	0	0	0	0	0	1	0	1	1	Read IS register

SUMMARY OF 8259A INSTRUCTION SET (Cont.)

Inst. #	Mnemonic	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description
62	OCW3 RR	0	0	0	0	0	1	0	1	0	Read request register
63	OCW3 SM	0	0	1	1	0	1	0	0	0	Set special mask mode
64	OCW3 RSM	0	0	1	0	0	1	0	0	0	Reset special mask mode

Note: 1. In the master mode $\overline{SP}$ pin = 1, in slave mode $\overline{SP}$ = 0

Cascading

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

A typical MCS-80/85 system is shown in Figure 2. The master controls, through the 3 line cascade bus, which one of the slaves will release the corresponding address.

As shown in Figure 2, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for MCS-86). The IRO input should not be connected to a slave 8259A unless IR1-IR7 also have slaves attached.

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first $\overline{INTA}$ pulse to the trailing edge of the third pulse. It is obvious that each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select ($\overline{CS}$) input of each 8259A.

The cascade lines of the Master 8259A are activated for any interrupt input, even if no slave is connected to that input.

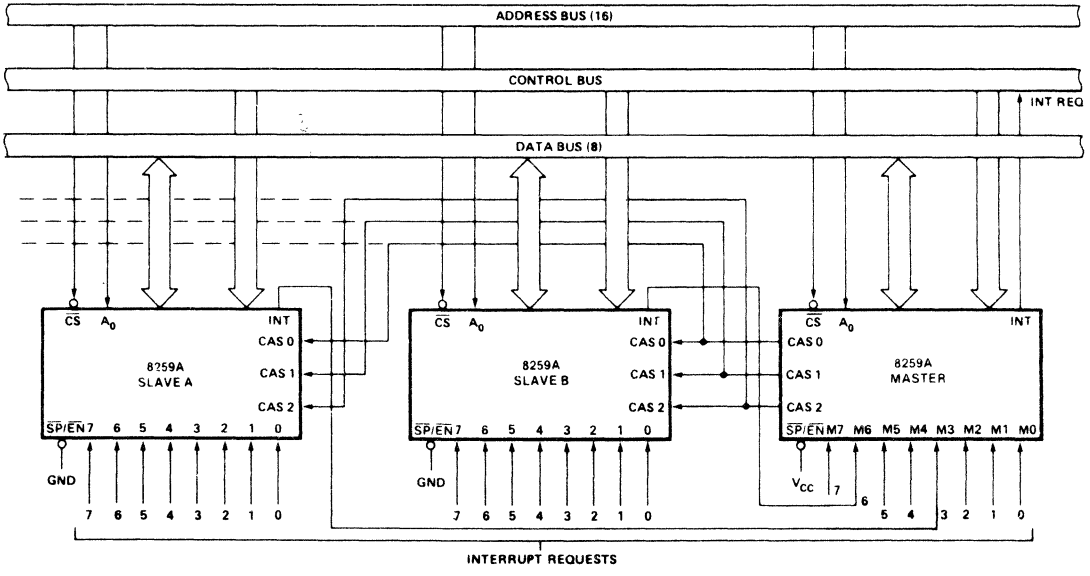


Figure 2. Cascading the 8259A

PIN FUNCTIONS

Name	I/O	Pin #	Function
V_{CC}		28	+5V supply.
GND		14	Ground.
D_{0-7}	I/O	11-4	Bidirectional data bus, used for: a) programming the mode of the 8259A (programming is done by software); b) the microprocessor can read the status of the 8259A; c) the 8259A will send vectoring data to the microprocessor when an interrupt is acknowledged.
IR_{0-7}	I	18-25	Interrupt Requests: These are asynchronous inputs. A positive-going edge will generate an interrupt request. Thus a request can be generated by raising the line and holding it high until acknowledged, or by a negative pulse. In level triggered mode, no edge is required. These lines are active HIGH.
$\overline{RD}$	I	3	Read (generally from 8228 in MCS-80 system or from 8086 in MCS-86 system).
$\overline{WR}$	I	2	Write (generally from 8228 in MCS-80 sytem or from 8086 in MCS-86 system).
$\overline{INTA}$	I	26	Interrupt Acknowledge (generally from 8228 in MCS-80 system, 8086 in MCS-86 system). The 8228 generates three distinct $\overline{INTA}$ pulses when a CALL is inserted, the 8086 produces two distinct $\overline{INTA}$ pulses during an interrupt cycle.
$\overline{CS}$	I	1	Chip Select: RD and WR are enabled by Chip Select, whereas Interrupt Acknowledge is Independent of Chip Select.
A0	I	27	Usually the least significant bit of the microprocessor address output (A1 in MCS-86 system). When A0 = 1 the Interrupt Mask Register can be loaded or read. When A0 = 0 the 8259A mode can be programmed or its status can be read. $\overline{CS}$ is active LOW.
INT	O	17	Goes directly to the microprocessor interrrupt input. This output will have high V_{OH} to match the 8080 3.3V V_{IH}. INT is active HIGH.
C0-C2	I/O	12 13 15	Three cascade lines, outputs in master mode and inputs in slave mode. The master issues the binary code of the acknowledged interrupt level on these lines. Each slave compares this code with its own.
$\overline{SP}/\overline{EN}$	I/O	16	$\overline{SP}/\overline{EN}$ is a dual function pin. In the buffered mode $\overline{SP}/\overline{EN}$ is used to enable bus transceivers ($\overline{EN}$). In the non-buffered mode $\overline{SP}/\overline{EN}$ determines if this 8259A is a master or a slave. If $\overline{SP}$ = 1 the 8259A is master; $\overline{SP}$ = 0 indicates a slave.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... −40°C to 85°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

*COMMENT
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 10% (8259-A), V_{CC} = 5V ± 10% (8259A)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-.5	V		
V_{IH}	Input High Voltage	2.0	V_{CC} + .5V	V	
V_{OL}	Output Low Voltage		.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
$V_{OH(INT)}$	Interrupt Output High Voltage	3.5 2.4		C V	I_{OH} = −100 μA I_{OH} = −400 μA
I_{LI}	Input Load Current		10	μA	V_{IN} = V_{CC} to 0V
I_{LOL}	Output Leakage Current		-10	μA	V_{OUT} = 0.45V
I_{CC}	V_{CC} Supply Current		85	mA	
I_{LIR}	IR Input Load Current		-300 10	μA μA	V_{IN} = 0 V_{IN} = V_{CC}

8259A A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$ $V_{CC} = 5V \pm 5\%$ (8259A-8) $V_{CC} = 5V \pm 10\%$ (8259A)

TIMING REQUIREMENTS

Symbol	Parameter	8259A-8 Min.	8259A-8 Max.	8259A Min.	8259A Max.	Units	Test Conditions
TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	50		0		ns	
TRHAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	5		0		ns	
TRLRH	$\overline{RD}$ Pulse Width	420		235		ns	
TAHWL	A0/$\overline{CS}$ Setup to$\overline{WR}$↓	50		0		ns	
TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}$↑	20		0		ns	
TWLWH	$\overline{WR}$ Pulse Width	400		290		ns	
TDVWH	Data Setup to $\overline{WR}$↑	300		240		ns	
TWHDX	Data Hold after $\overline{WR}$↑	40		0		ns	
TJLJH	Interrupt Request Width (Low)	100		100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave Only)	55		55		ns	
TRHRL	End of $\overline{RD}$ to Next Command	300		160		ns	
TWHRL	End of $\overline{WR}$ to Next Command	370		190		ns	

Note: 1. This is the low time required to clear the input latch in the edge triggered mode.

TIMING RESPONSES

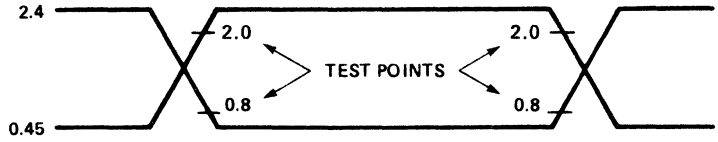
Symbol	Parameter	8259A-8 Min.	8259A-8 Max.	8259A Min.	8259A Max.	Units	Test Conditions
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$↓		300		200	ns	C of Data Bus Max. test C = 100 pF Min. test C = 15 pF C_{INT} = 100 pF C_{ENABLE} = 15pF
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$↑	10	200		100	ns	
TJHIH	Interrupt Output Delay		400		350	ns	
TIALCV	Cascade Valid from First $\overline{INTA}$↓ (Master Only)		565		565	ns	
TRLEL	Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↓		160		125	ns	
TRHEH	Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑		325		150	ns	
TAHDV	Data Valid from Stable Address		350		200	ns	
TCVDV	Cascade Valid to Valid Data		300		300	ns	

CAPACITANCE

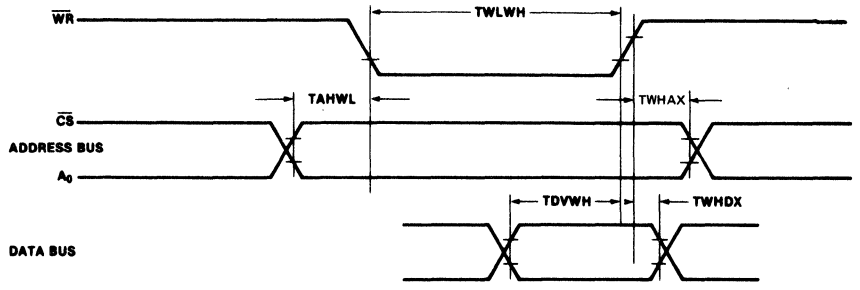
$T_A = 25°C$; $V_{CC} = GND = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

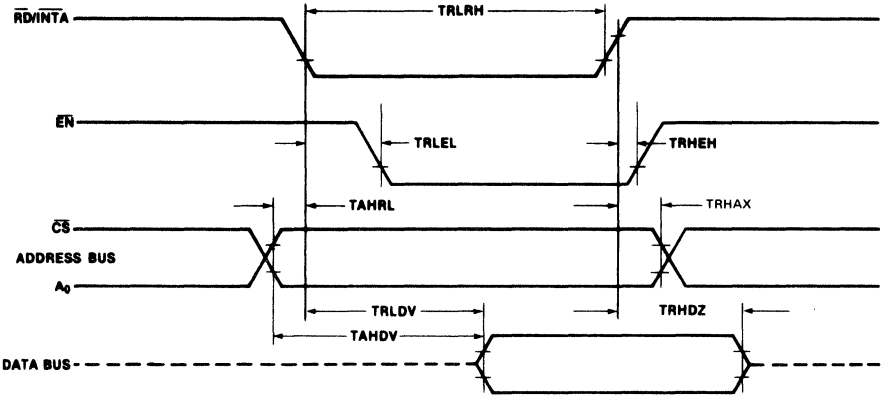
Input and Output Waveforms for A.C. Tests



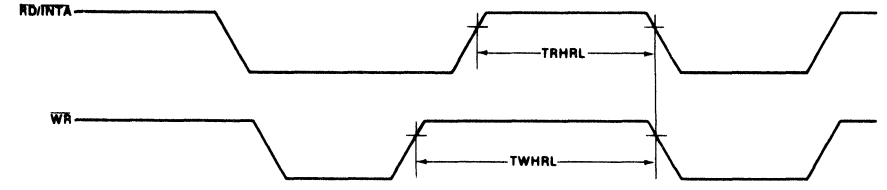
WRITE MODE



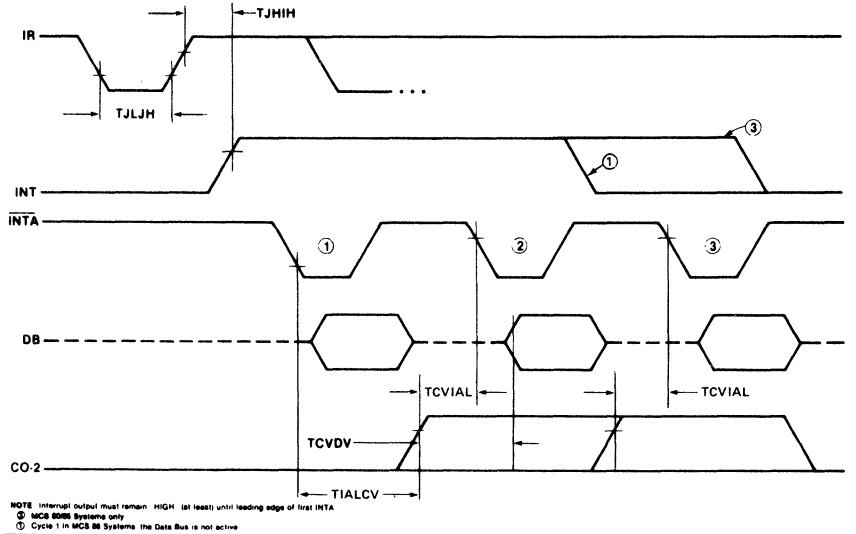
READ/INTA MODE



OTHER TIMING



INTA SEQUENCE



NOTE: Interrupt output must remain HIGH (at least) until leading edge of first INTA.
② MCS 80/85 Systems only.
① Cycle 1 in MCS 86 Systems: the Data Bus is not active.

8355*/8355-2**

16,384-BIT ROM WITH I/O

*Directly Compatible with 8085A CPU

**Directly Compatible with 8085A-2

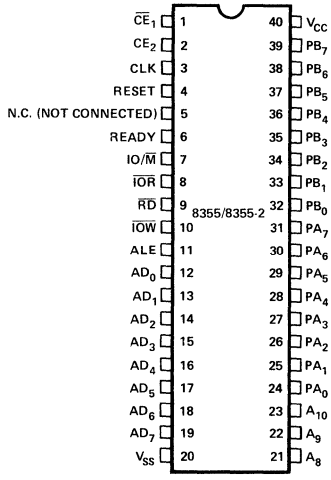
- 2048 Words x 8 Bits
- Single +5V Power Supply
- Internal Address Latch
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40-Pin DIP

The Intel® 8355 is a ROM and I/O chip to be used in the MCS-85™ microcomputer system. The ROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 400 ns to permit use with no wait states in the 8085A CPU.

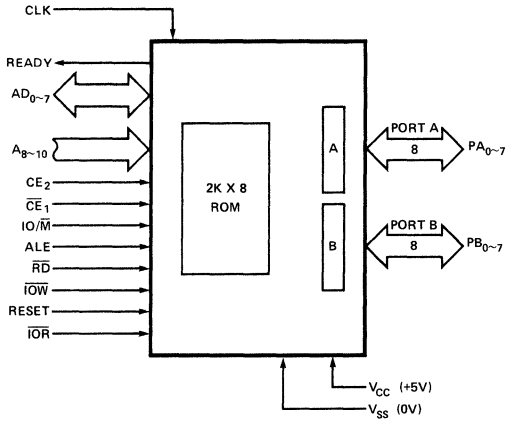
The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is indivdually programmable as input or output.

The 8355-2 has a 300ns access time for compatibility with the 8085A-2 microprocessor.

PIN CONFIGURATION



BLOCK DIAGRAM



Symbol	Function
ALE (Input)	When ALE (Address Latch Enable is high, AD_{0-7}, IO/$\overline{M}$, A_{8-10}, CE, and $\overline{CE}$ enter address latched. The signals (AD, IO/$\overline{M}$, A_{8-10}, CE, $\overline{CE}$) are latched in at the trailing edge of ALE.
AD_{0-7} (Input)	Bidirectional Address/Data bus. The lower 8-bits of the ROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched chip enables are active, the output buffers present data on the bus.
A_{8-10} (Input)	These are the high order bits of the ROM address. They do not affect I/O operations.
$\overline{CE_1}$ CE_2 (Input)	Chip Enable Inputs: $\overline{CE_1}$ is active low and CE_2 is active high. The 8355 can be accessed only when BOTH Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_{0-7} and READY outputs will be in a high impedance state.
IO/$\overline{M}$ (Input)	If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the ROM.
$\overline{RD}$ (Input)	If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected ROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are 3-state.
$\overline{IOW}$ (Input)	If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.

Symbol	Function
CLK (Input)	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE}$ low, CE high and ALE high.
READY (Output)	Ready is a 3-state output controlled by $\overline{CE_1}$, CE_2, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK (see Figure 6).
PA_{0-7} (Input/ Output)	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0. Read operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 low, or IO/$\overline{M}$ high, $\overline{RD}$ low, active chip enables, and AD_0 low.
PB_{0-7} (Input/ Output)	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0.
RESET (Input)	An input high on RESET causes all pins in Port A and B to assume input mode.
$\overline{IOR}$ (Input)	When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} ("1").
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	V_{CC} = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

		8355		8355-2 (Preliminary)		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
t_{CYC}	Clock Cycle Time	320		320		ns
T_1	CLK Pulse Width	80		80		ns
T_2	CLK Pulse Width	120		120		ns
t_f,t_r	CLK Rise and Fall Time		30		30	ns
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		30		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170		140	ns
t_{AD}	Address Stable to Data Out Valid		400		330	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float after READ	0	100	0	85	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to Write Set Up Time	150		150		ns
t_{WD}	Data In Hold Time After WRITE	10		10		ns
t_{WP}	WRITE to Port Output		400		400	ns
t_{PR}	Port Input Set Up Time	50		50		ns
t_{RP}	Port Input Hold Time	50		50		ns
t_{RYH}	READY HOLD Time	0	160	0	160	ns
t_{ARY}	ADDRESS (CE) to READY		160		160	ns
t_{RV}	Recovery Time Between Controls	300		200		ns
t_{RDE}	READ Control to Data Bus Enable	10		10		ns

Note: C_{LOAD} = 150pF

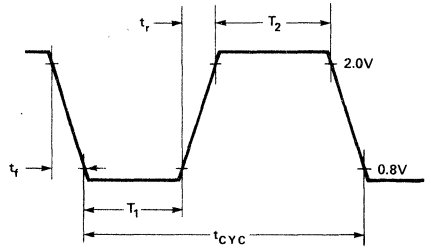


Figure 1. Clock Specification for 8355

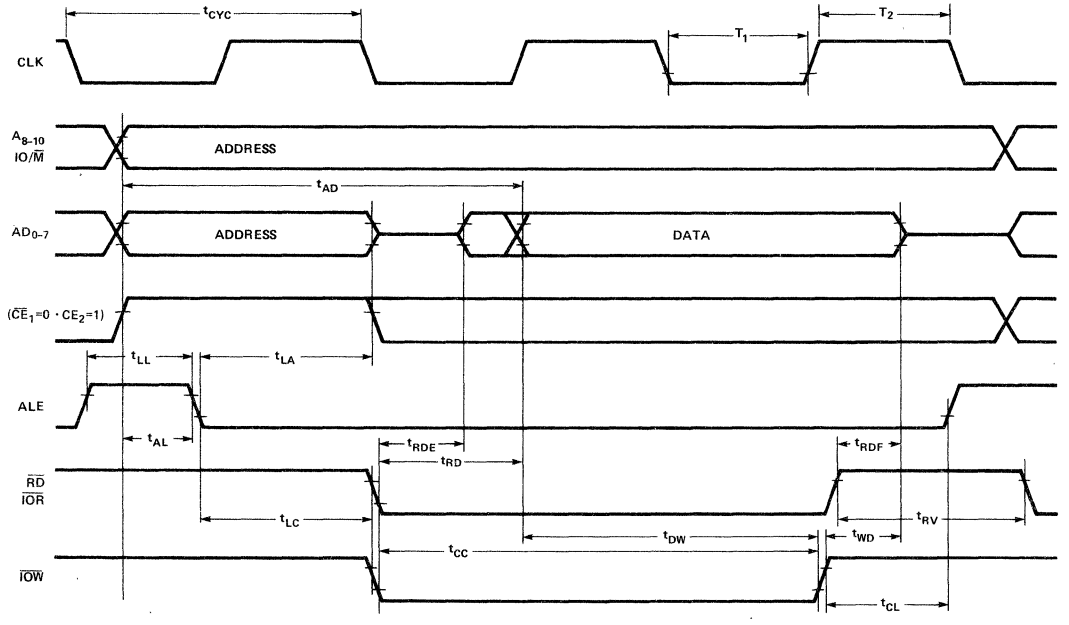
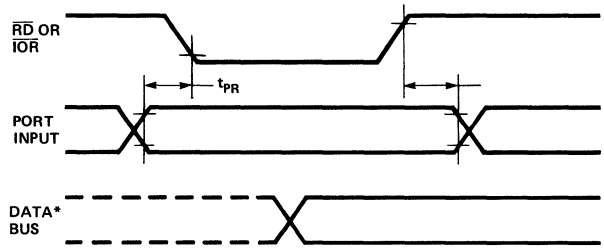
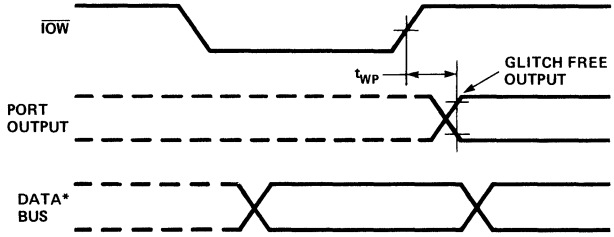


Figure 2. ROM Read and I/O Read and Write

a. Input Mode



b. Output Mode



*DATA BUS TIMING IS SHOWN IN FIGURE 4.

Figure 3. I/O Port Timing

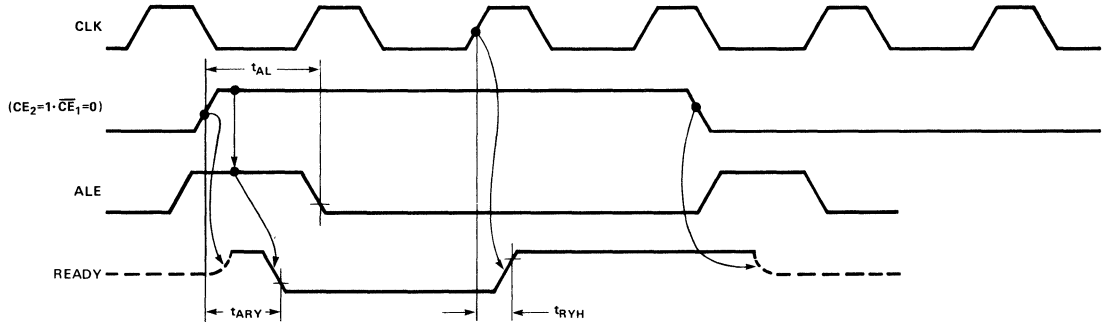


Figure 4. Wait State Timing (READY = 0)

8755A
16,384-BIT EPROM WITH I/O

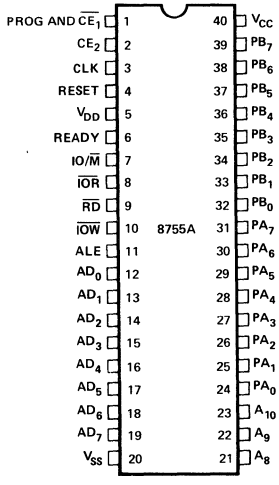
- **Directly Compatible with 8085A CPU**

- **2048 Words x 8 Bits**
- **Single +5V Power Supply (V_{CC})**
- **U.V. Erasable and Electrically Reprogrammable**
- **Internal Address Latch**
- **2 General Purpose 8-Bit I/O Ports**
- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **40-Pin DIP**

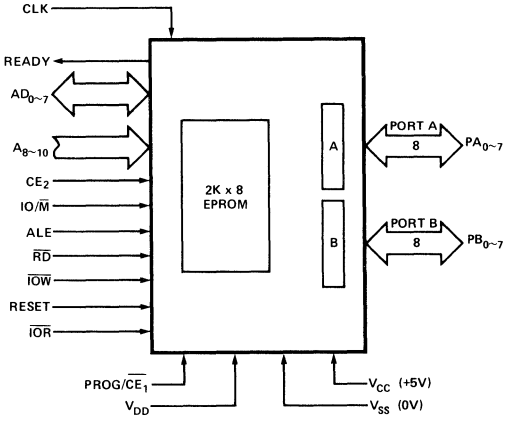
The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the MCS-85™ microcomputer system. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in an 8085A CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

PIN CONFIGURATION



BLOCK DIAGRAM



8755A FUNCTIONAL PIN DEFINITION

Symbol	Function
ALE (input)	When Address Latch Enable goes high, AD_{0-7}, IO/M, A_{8-10}, CE_2, and $\overline{CE_1}$ enter the address latches. The signals (AD, IO/M, A_{8-10}, CE) are latched in at the trailing edge of ALE.
AD_{0-7} (input/output)	Bidirectional Address/Data bus. The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10} (input)	These are the high order bits of the PROM address. They do not affect I/O operations.
PROG/$\overline{CE_1}$ CE_2 (input)	Chip Enable Inputs: $\overline{CE_1}$ is active low and CE_2 is active high. The 8755A can be accessed only when *BOTH* Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_{0-7} and READY outputs will be in a high impedance state. $\overline{CE_1}$ is also used as a programming pin. (See section on programming.)
IO/$\overline{M}$ (input)	If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the PROM.
$\overline{RD}$ (input)	If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected PROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are 3-stated.
$\overline{IOW}$ (input)	If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.
CLK (input)	The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE_1}$ low, CE_2 high, and ALE high.

Symbol	Function
READY (output)	READY is a 3-state output controlled by CE_2, $\overline{CE_1}$, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK. (See Figure 6.)
PA_{0-7} (input/output)	These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0, AD_1. Read operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 and AD_1 low, *or* IO/$\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 and AD_1 low.
PB_{0-7} (input/output)	This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0 and a 0 from AD_1.
RESET (input)	In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
$\overline{IOR}$ (input)	When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} ("1").
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.
V_{DD}	V_{DD} is a programming voltage, and must be tied to +5V when the 8755A is being read. For programming, a high voltage is supplied with V_{DD} = 25V, typical. (See section on programming.)

ERASURE CHARACTERISTICS

The erasure characteristics of the 8755A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8755A in approximately 3 years while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8755A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8755 window to prevent unintentional erasure.

The recommended erasure procedure for the 8755A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm^2 power rating. The 8755A should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

PROGRAMMING

Initially, and after each erasure, all bits of the EPROM portions of the 8755A are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 8755A can be programmed on the Intel® Universal PROM Programmer (UPP), and the PROMPT™ 80/85 and PROMPT-48™ design aids. The appropriate programming modules and adapters for use in programming both 8755A's and 8755's are shown in Table 1.

The program mode itself consists of programming a single address at a time, giving a single 50 msec pulse for every address. Generally, it is desirable to have a verify cycle after a program cycle for the same address as shown in the attached timing diagram. In the verify cycle (i.e., normal memory read cycle) 'V_{DD}' should be at +5V.

Preliminary timing diagrams and parameter values pertaining to the 8755A programming operation are contained in Figure 6.

TABLE 1. 8755A PROGRAMMING MODULE CROSS REFERENCE

MODULE NAME	USE WITH
UPP 955	UPP(4)
UPP UP2(2)	UPP 855
PROMPT 975	PROMPT 80/85(3)
PROMPT 475	PROMPT 48(1)

NOTES:
1. Described on p. 11-9 of 1978 System Data Catalog.
2. Special adaptor socket.
3. Described on p. 11-3 of 1978 System Data Catalog.
4. Described on p. 10-85 of 1978 System Data Catalog.

SYSTEM APPLICATIONS

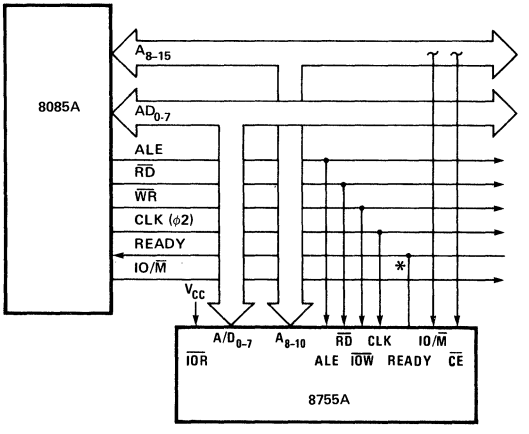
System Interface with 8085A

A system using the 8755A can use either one of the two I/O Interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE_2 and $\overline{CE}_1$. By using a combination of unused address lines A_{11-15} and the Chip Enable inputs, the 8085A system can use up to 5 each 8755A's without requiring a CE decoder.

If a memory mapped I/O approach is used the 8755A will be selected by the combination of both the Chip Enables and IO/$\overline{M}$ using the AD_{8-15} address lines. See Figure 1.



*NOTE: Optional connection.

Figure 1. 8755A in 8085A System (Memory-Mapped I/O)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5 to +7V*
Power Dissipation 1.5W

*Except for programming voltage.

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CYC}	Clock Cycle Time	320		ns	
T_1	CLK Pulse Width	80		ns	C_{LOAD} = 150 pF
T_2	CLK Pulse Width	120		ns	(See Figure 3)
t_f,t_r	CLK Rise and Fall Time		30	ns	
t_{AL}	Address to Latch Set Up Time	50		ns	
t_{LA}	Address Hold Time after Latch	80		ns	
t_{LC}	Latch to READ/WRITE Control	100		ns	
t_{RD}	Valid Data Out Delay from READ Control		170	ns	
t_{AD}	Address Stable to Data Out Valid		450	ns	150 pF Load
t_{LL}	Latch Enable Width	100		ns	
t_{RDF}	Data Bus Float after READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		ns	
t_{CC}	READ/WRITE Control Width	250		ns	
t_{DW}	Data In to WRITE Set Up Time	150		ns	
t_{WD}	Data In Hold Time After WRITE	30		ns	
t_{WP}	WRITE to Port Output		400	ns	
t_{PR}	Port Input Set Up Time	50		ns	
t_{RP}	Port Input Hold Time	50		ns	
t_{RYH}	READY HOLD TIME	0	160	ns	
t_{ARY}	ADDRESS (CE) to READY		160	ns	
t_{RV}	Recovery Time between Controls	300		ns	
t_{RDE}	Data Out Delay from READ Control	10		ns	
t_{LD}	ALE to Data Out Valid		350	ns	Preliminary

WAVEFORMS

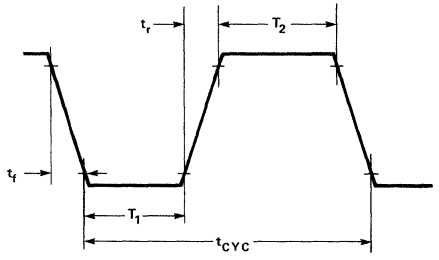


Figure 2. Clock Specification for 8755A

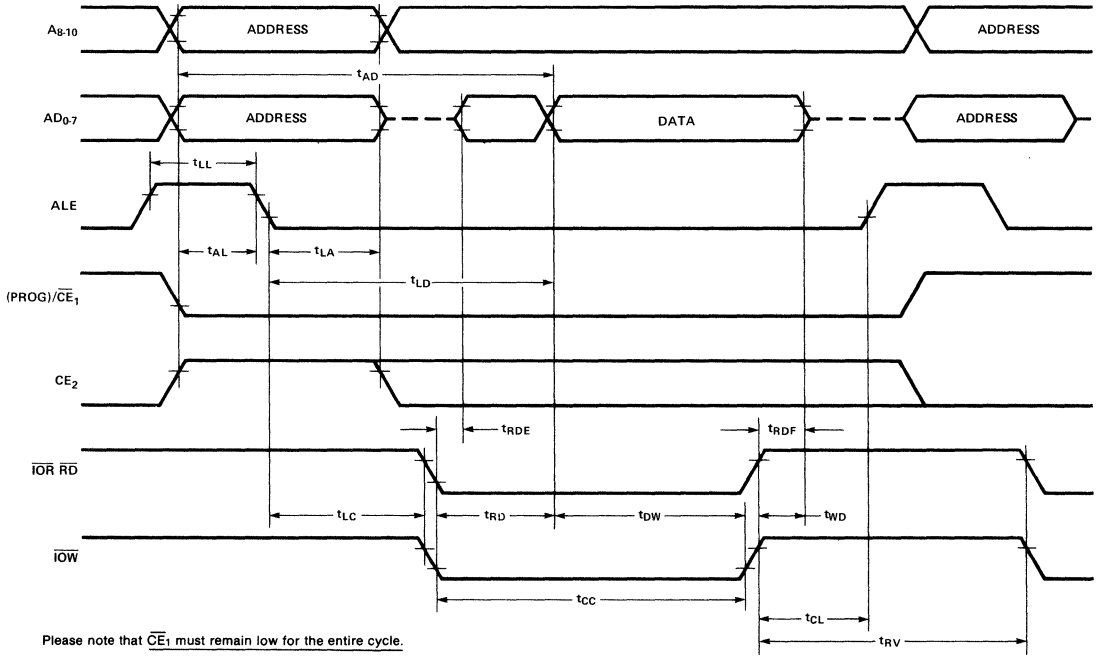


Figure 3. PROM Read, I/O Read and Write Timing

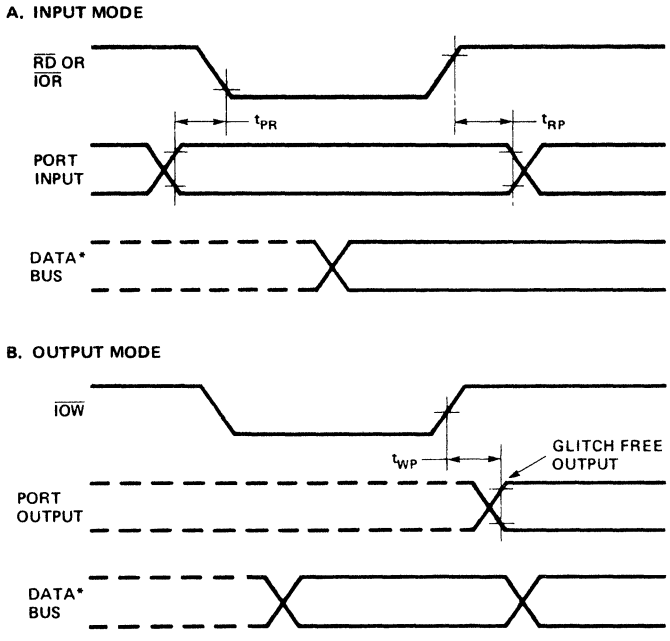


Figure 4. I/O Port Timing

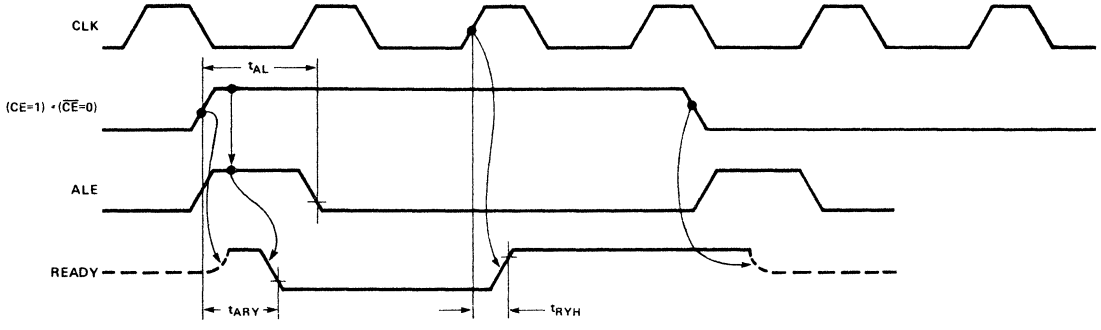


Figure 5. Wait State Timing (READY = 0)

D.C. SPECIFICATION PROGRAMMING

(T_A = 0°C to 70°C; V_{CC} = 5V ± 5%; V_{SS} = 0V)

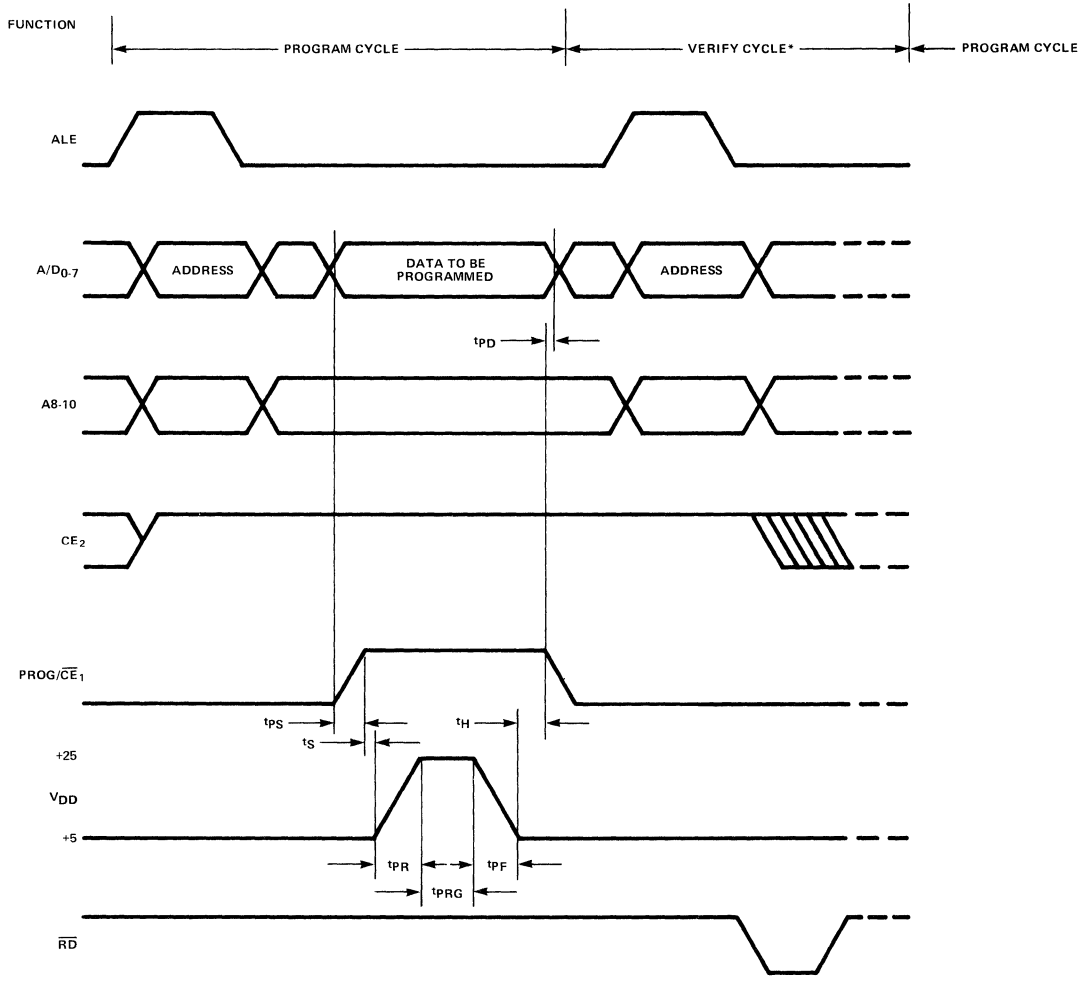
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Programming Voltage (during Write to EPROM)	24	25	26	V
I_{DD}	Prog Supply Current		15	30	mA

A.C. SPECIFICATION FOR PROGRAMMING

(T_A = 0°C to 70°C; V_{CC} = 5V ± 5%; V_{SS} = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PS}	Data Setup Time	10			ns
t_{PD}	Data Hold Time	0			ns
t_S	Prog Pulse Setup Time	2			μs
t_H	Prog Pulse Hold Time	2			μs
t_{PR}	Prog Pulse Rise Time	0.01	2		μs
t_{PF}	Prog Pulse Fall Time	0.01	2		μs
t_{PRG}	Prog Pulse Width	45	50		msec

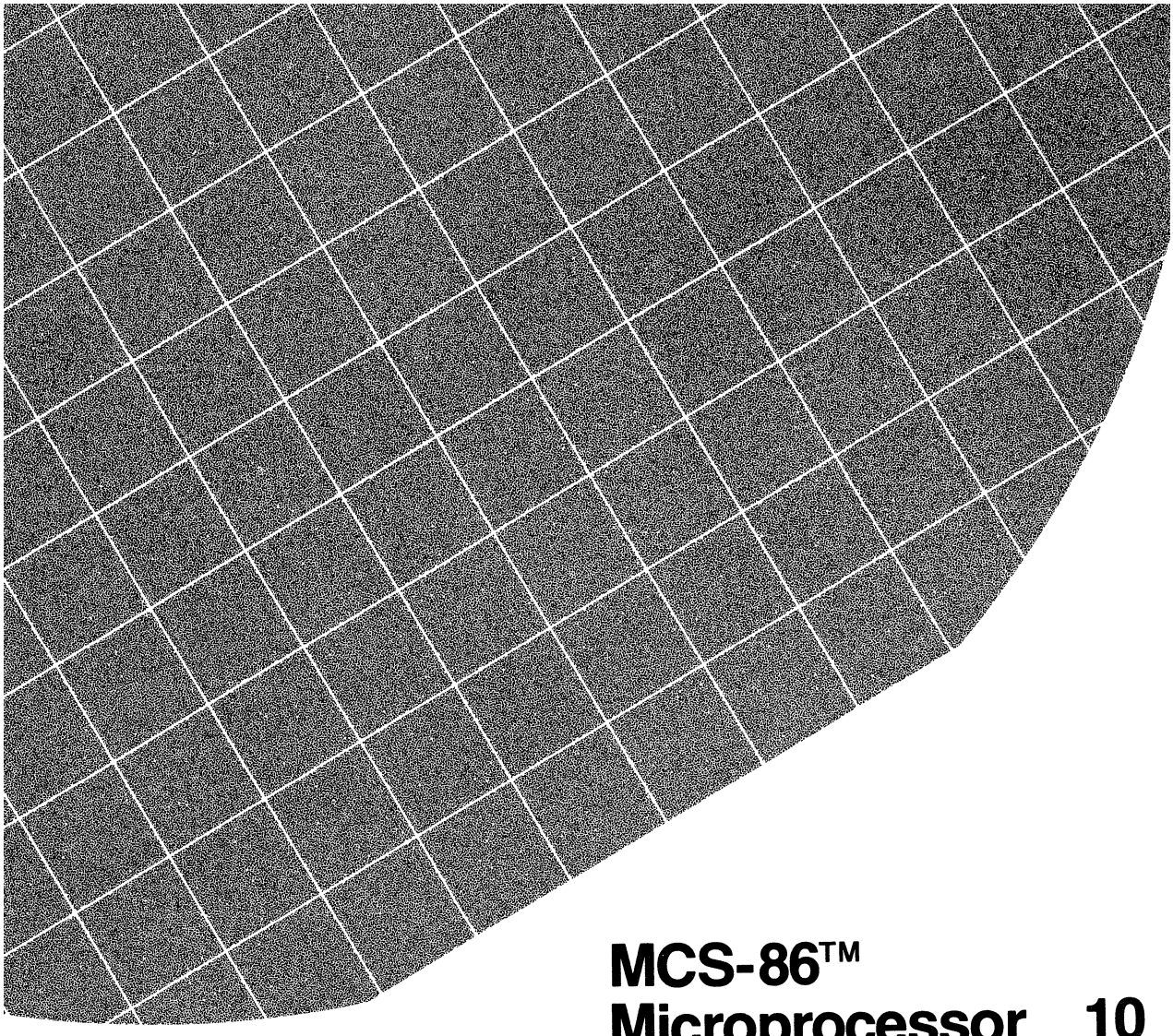
WAVEFORMS



*VERIFY CYCLE IS A REGULAR MEMORY READ CYCLE (WITH V_{DD} = +5V FOR 8755A)

Figure 6. 8755A Program Mode Timing Diagram

MCS-80/85



MCS-86™ Microprocessor 10

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THE MCS-86 MICROPROCESSOR FAMILY

INTRODUCTION

The Intel® 8086, a new microcomputer, extends the mid-range 8080 family into the 16-bit arena. The chip has attributes of both 8- and 16-bit processors. By executing the full set of 8080A/8085 8-bit instructions plus a powerful new set of 16-bit instructions, it enables a system designer familiar with existing 8080 devices to boost performance by a factor of as much as 10 while using essentially the same 8080 software package and development tools.

The goals of the 8086 architectural design were to extend existing 8080 features symmetrically, across the board, and to add processing capabilities not to be found in the 8080. The added features include 16-bit arithmetic, signed 8- and 16-bit arithmetic (including multiply and divide), efficient interruptible byte-string operations, and improved bit manipulation. Significantly, they also include mechanisms for such minicomputer-type operations as reentrant code, position-independent code, and dynamically relocatable programs. In addition, the processor may directly address up to 1 megabyte of memory and has been designed to support multiple-processor configurations.

Support for the 8086 is provided by offering a complete line of bipolar components: clock generator, octal latches, octal transceivers, and a bus controller. Existing 8-bit peripherals and memories can be used to build your complete system. A configuration option in the 8086 allows a complete 16-bit system to be built with as little as 11 components (including memory and I/O).

FURTHER INFORMATION

For more detailed information on the MCS-86 microcomputer family please consult the following Intel publication: MCS-86 User's Manual (order number 9800722A).

RECOMMENDED PRODUCTS FOR MCS-86 MICROCOMPUTER APPLICATIONS

Function	Part No.	Page No.	Description
RAMs (Static)	2114	3-54	1K x 4
	2141	3-89	4K x 1
	2142	3-95	1K x 4
	2148	3-106	1K x 4 High Speed
RAMs (Dynamic)	2117	3-64	16K x 1
	2118	3-88	16K x 1
RAM Support	8202	11-14	Dynamic RAM Controller
ROMs	2316E	4-12	2K x 8
EPROMs	2716	4-23	2K x 8
	2732	4-28	4K x 8
Microprocessor Support	8205	9-29	1-of-8 Decoder
	8257-5	9-92	DMA Controller
	8259A	9-109	Interrupt Controller
	8282	10-23	8-Bit Non-Inverting Latch
	8283	10-23	8-Bit Inverting Latch
	8284	10-27	Clock Generator
	8286	10-33	8-Bit Non-Inverting Transceiver
	8287	10-33	8-Bit Inverting Transceiver
	8288	10-37	Bus Controller
Peripherals	8251A	11-24	USART
	8253-5	11-32	Counter/Timer
	8255A-5	11-43	Programmable Peripheral Interface
	8271	11-64	Floppy Disk Controller
	8273	11-93	Communications Controller
	8275	11-118	CRT Controller
	8278	11-142	Keyboard/Display Controller
	8279-5	11-152	Keyboard/Display Controller
	8291	11-164	GPIB Talker/Listener
	8292	11-188	GPIB Controller
	8294	11-190	Data Encrypter
	8295	11-201	Dot Matrix Printer Controller
	8041/8741	11-3	Universal Peripheral Interface

8086/8086-4
16-BIT HMOS MICROPROCESSOR

- **Direct Addressing Capability to 1 MByte of Memory**
- **Assembly Language Compatible with 8080/8085**
- **14 Word, By 16-Bit Register Set with Symmetrical Operations**
- **24 Operand Addressing Modes**
- **Bit, Byte, Word, and Block Operations**
- **8-and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide**
- **5 MHz Clock Rate (4 MHz for 8086-4)**
- **MULTIBUS™ System Compatible Interface**

The Intel® 8086 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It addresses memory as a sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance.

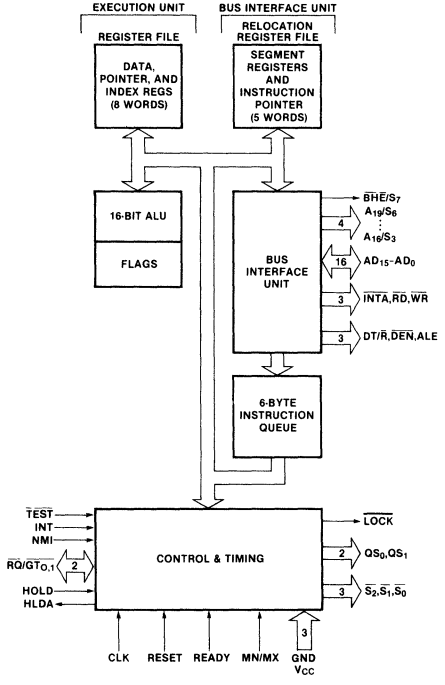
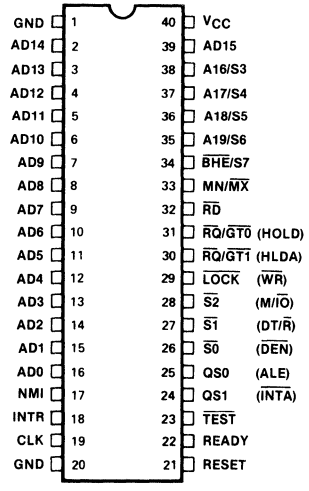


Figure 1. 8086 CPU Functional Block Diagram



40 LEAD

Figure 2. 8086 Pin Diagram

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The internal functions of the 8086 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of Figure 1.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage. See the Instruction Set description for further register set and architectural descriptions.

MEMORY ORGANIZATION

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is logically organized as a linear array of 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory can be further logically divided into code, data, alternate data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 3a.)

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. This performance penalty does not occur for instruction fetches, only word operands.

Physically, the memory is organized as a high bank (D_{15}-D_8) and a low bank (D_7-D_0) of 512K 8-bit bytes addressed in parallel by the processor's address lines A_{19}-A_1. Byte data with even addresses is transferred on the D_7-D_0 bus lines while odd addressed byte data (A_0 HIGH) is transferred on the D_{15}-D_8 bus lines. The processor provides two enable signals, $\overline{BHE}$ and A_0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor to the byte level as necessary.

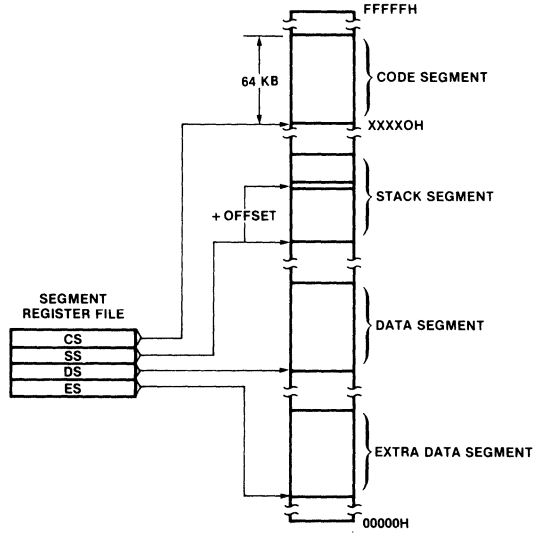


Figure 3a. Memory Organization

In referencing word data the BIU requires one or two memory cycles depending on whether or not the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (see Figure 3b.) Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt types has its service routine pointed to by a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

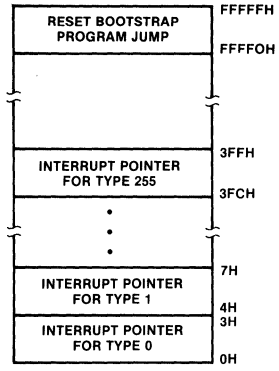


Figure 3b. Reserved Memory Locations

MINIMUM AND MAXIMUM MODES

The requirements for supporting minimum and maximum 8086 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 8086 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes dependent on the condition of the strap pin. When MN/$\overline{MX}$ pin is strapped to GND, the 8086 treats pins 24 through 31 in maximum mode. An 8288 bus controller interprets status information coded into $\overline{S}_0$,$\overline{S}_1$,$\overline{S}_2$ to generate bus timing and control signals compatible with the MULTIBUS™. When the MN/$\overline{MX}$ pin is strapped to V_{CC}, the 8086 generates bus control signals itself on pins 24 through 31, as shown in parentheses in Figure 2. Examples of minimum mode and maximum mode systems are shown in Figure 4.

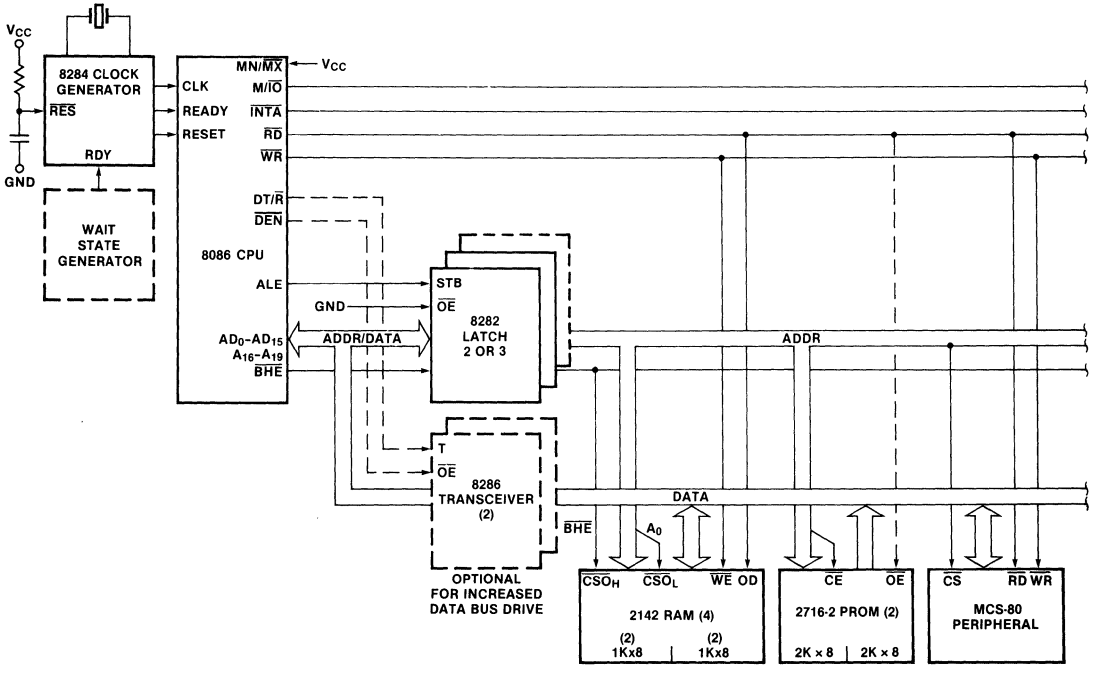


Figure 4a. Minimum Mode 8086 Typical System Configuration

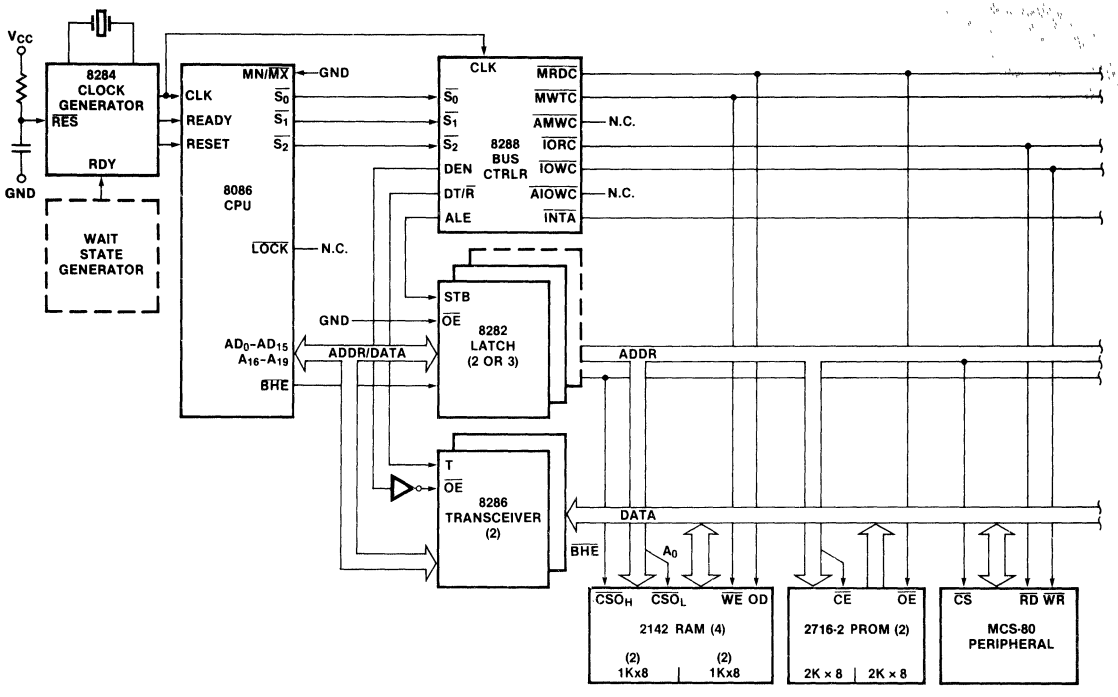


Figure 4b. Maximum Mode 8086 Typical System Configuration

BUS OPERATION

The 8086 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T_1, T_2, T_3 and T_4 (see Figure 5). The address is emitted from the processor during T_1 and data transfer occurs on the bus during T_3 and T_4. T_2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (T_W) are inserted between T_3 and T_4. Each inserted "Wait" state is of the same duration as a CLK cycle. Periods can occur between 8086 driven bus cycles. These are referred to as "Idle" states (T_I) or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T_1 of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the 8288 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S_3 through S_7 are multiplexed with high-order address bits and the $\overline{BHE}$ signal, and are therefore valid during T_2 through T_4. S_3 and S_4 indicate which segment register (see Instruction Set description) was used for this bus cycle in forming the address, according to the following table:

S_4	S_3	
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S_5 is a reflection of the PSW interrupt enable bit. $S_6 = 0$ and S_7 is a spare status bit.

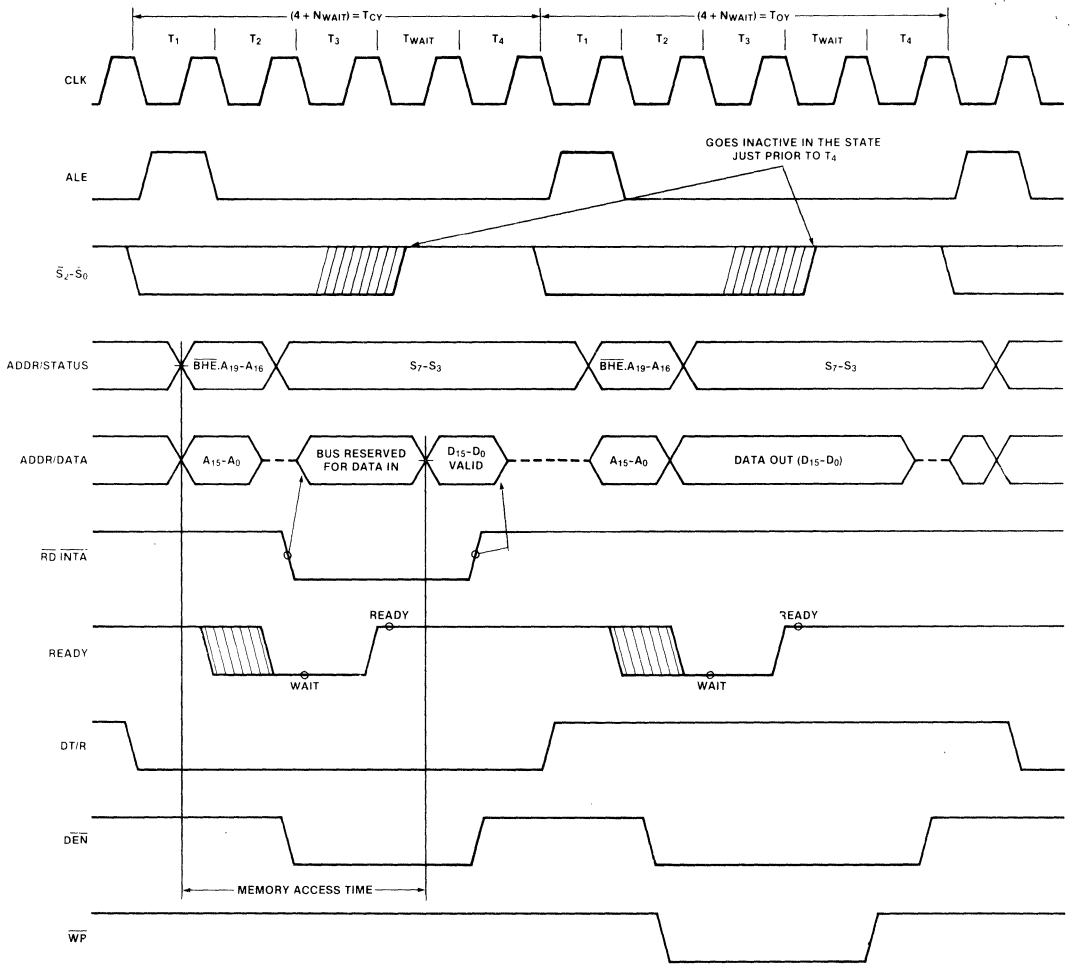


Figure 5. Basic System Timing

I/O ADDRESSING

In the 8086, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A_{15}–A_0. The address lines A_{19}–A_{16} are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D_7–D_0 bus lines and odd addressed bytes on D_{15}–D_8. Care must be taken to assure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

EXTERNAL INTERFACE

PROCESSOR RESET AND INITIALIZATION

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 8086 RESET is required to be HIGH for greater than 4 CLK cycles. The

8086 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 10 CLK cycles. After this interval the 8086 operates normally beginning with the instruction in absolute location FFFF0H (see Figure 3b). The details of this operation are specified in the Instruction Set description of the MCS-86 Users' Manual. The RESET input is internally synchronized to the processor clock. At initialization the HIGH-to-LOW transition of RESET must occur no sooner than 50 μs after power-up, to allow complete initialization of the 8086.

If INTR is asserted sooner than 9 CLK cycles after the end of RESET, the processor may execute one instruction before responding to the interrupt. NMI may not be asserted prior to the 2nd CLK cycle following the end of RESET.

INTERRUPT OPERATIONS

Interrupt operations fall into two classes; software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 3b), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location.

NON-MASKABLE INTERRUPT (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt. (See Instruction Set description.)

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any high-going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

MASKABLE INTERRUPT (INTR)

The 8086 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable FLAG status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block-type instruction. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the

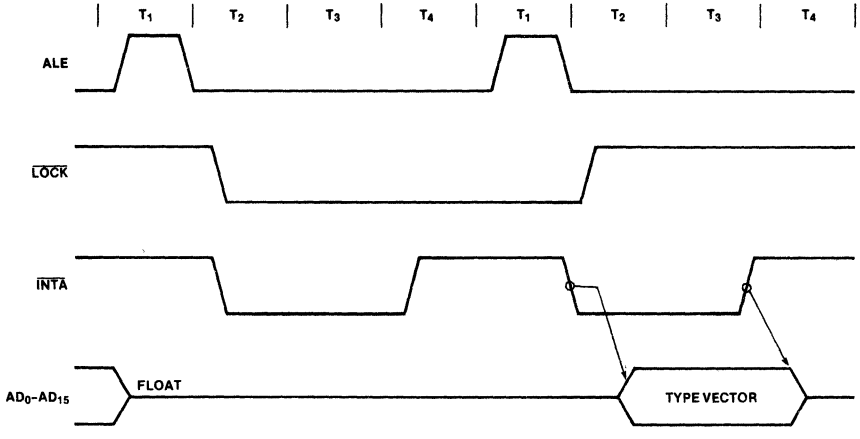


Figure 6. Interrupt Acknowledge Sequence

FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (figure 6) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 8086 emits the LOCK signal from T_2 of the first bus cycle until T_2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle a byte is fetched from the external interrupt system (e.g., 8259A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

HALT

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In Maximum Mode, the processor issues appropriate HALT status on $\overline{S}_2\overline{S}_1\overline{S}_0$ and the 8288 bus controller issues one ALE. The 8086 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator. An interrupt request or RESET will force the 8086 out of the "HALT" state.

READ/MODIFY/WRITE (SEMAPHORE) OPERATIONS VIA LOCK

The $\overline{LOCK}$ status information is provided by the processor when directly consecutive bus cycles are required during the execution of an instruction. This provides the processor with the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without the possibility of another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (forced LOW) in the clock cycle following the one in which the software "LOCK" prefix instruction is decoded by the EU. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While $\overline{LOCK}$ is active all interrupts are masked and a request on a $\overline{RQ}/\overline{GT}$ pin will be recorded and then honored at the end of the $\overline{LOCK}$.

EXTERNAL SYNCHRONIZATION VIA TEST

As an alternative to the interrupts and general I/O capabilities, the 8086 provides a single software-testable input known as the $\overline{TEST}$ signal. At any time the program may execute a WAIT instruction. If at that time the $\overline{TEST}$ signal is inactive (HIGH), program execution becomes suspended while the processor waits for $\overline{TEST}$ to become active. It must remain active for at least 5 CLK cycles. The WAIT instruction is re-executed repeatedly until that time. This activity does not consume bus cycles. The processor remains in an idle state while waiting. All 8086 drivers go to 3-state OFF if bus "Hold"is entered. If interrupts are enabled, they may occur while the processor is waiting. When this occurs the processor fetches the WAIT instruction one extra time, processes the interrupt, and then re-fetches and re-executes the WAIT instruction upon returning from the interrupt.

8086 COMPARED WITH 8080/8085

While the 8086 has new instruction coding patterns to allow for the greatly expanded capabilities, all functions of the 8080/8085 may be performed by the 8086 with identical program semantics to their 8080/8085 versions. For every 8080/8085 instruction there is a corresponding 8086 instruction (or, in rare cases, a short sequence of instructions). Virtually all 8086 data manipulation instructions may be specified to operate on either the full set of 16-bit registers or on an 8-bit subset of them which corresponds to the 8080 register set. This relationship is shown in Figure 7 where the shaded registers (names in parentheses) represent the 8080 register set.

BASIC SYSTEM TIMING

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 4a and 4b, respectively. In minimum mode, the MN/$\overline{MX}$ pin is strapped to V_{CC} and the processor emits bus control signals in a manner similar to the 8085. In maximum mode, the MN/$\overline{MX}$ pin is strapped to V_{SS} and the processor emits coded status information which the 8288 bus controller uses to generate MULTIBUS™ compatible bus control signals. Figure 5 illustrates the signal timing relationships.

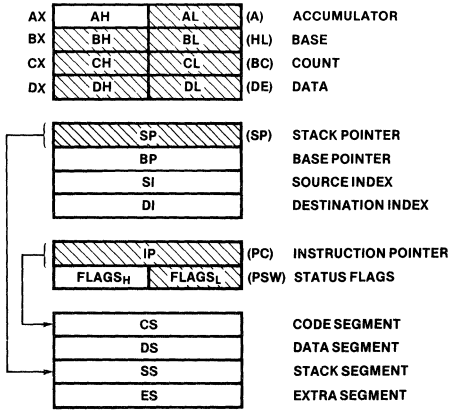


Figure 7. 8086 Register Model; (8080 Registers Shaded)

SYSTEM TIMING — MINIMUM SYSTEM

The read cycle begins in T_1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the local bus at this time, into the 8282/8283 latch. The $\overline{BHE}$ and A_0 signals address the low, high, or both bytes. From T_1 to T_4 the M/$\overline{IO}$ signal indicates a memory or I/O operation. At T_2 the address is removed from the local bus and the bus goes to a high impedance state. The read control signal is also asserted at T_2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver (8286/8287) is required to buffer the 8086 local bus, signals DT/$\overline{R}$ and $\overline{DEN}$ are provided by the 8086.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/$\overline{IO}$ signal is again asserted to indicate a memory or I/O write operation. In the T_2 immediately following the address emission the processor emits the data to be written into the addressed location. This data remains valid until the middle of T_4. During T_2, T_3, and T_W the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T_2 as opposed to the read which is delayed somewhat into T_2 to provide time for the bus to float.

The $\overline{BHE}$ and A_0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to the following table:

$\overline{BHE}$	A0	
0	0	Whole word
0	1	Upper byte from/ to odd address
1	0	Lower byte from/ to even address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D_7-D_0 bus lines and odd addressed bytes on D_{15}-D_8.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is floated. (See Figure 6.) In the second of two successive INTA cycles, a byte of information is read from bus lines D_7-D_0 as supplied by the interrupt system logic (i.e., 8259A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

BUS TIMING — MEDIUM COMPLEXITY SYSTEMS

For medium complexity systems the MN/$\overline{MX}$ pin is connected to V_{SS} and the 8288 Bus Controller is added to the system as well as an 8282/8283 latch for latching the system address, and a 8286/8287 transceiver to allow for bus loading greater than the 8086 is capable of handling. Signals ALE, DEN, and DT/$\overline{R}$ are generated by the 8288 instead of the processor in this configuration although their timing remains relatively the same. The 8086 status outputs ($\overline{S}_2$, $\overline{S}_1$, and $\overline{S}_0$) provide type-of-cycle information and become 8288 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 8288 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 8288 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence data isn't valid at the leading edge of write. The 8286/8287 transceiver receives the usual T and $\overline{OE}$ Inputs from the 8288's DT/$\overline{R}$ and DEN.

The pointer into the interrupt vector table, which is passed during the second INTA cycle, can derive from an 8259A located on either the local bus or the system bus. If the master 8259A Priority Interrupt Controller is positioned on the local bus, a TTL gate is required to disable the 8286/8287 transceiver when reading from the master 8259A during the interrupt acknowledge sequence and software "poll".

8086 FUNCTIONAL PIN DEFINITION

The following pin function descriptions are for 8086 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 8086 (without regard to additional bus buffers).

AD_{15}–AD_0 (INPUT/OUTPUT 3-STATE)

These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, T_W, T_4) bus. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7–D_0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions. (See table on page 8.) These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".

A_{19}/S_6, A_{18}/S_5, A_{17}/S_4, A_{16}/S_3 (OUTPUT 3-STATE)

During T_1 these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W, and T_4. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. A_{17}/S_4 and A_{16}/S_3 are encoded as follows:

A_{17}/S_4	A_{16}/S_3	
0 (LOW)	0	Alternate Data
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S_6 is 0 (LOW

This information indicates which relocation register is presently being used for data accessing.

These lines float to 3-state OFF during local bus "hold acknowledge".

$\overline{BHE}/S_7$ (OUTPUT 3-STATE)

During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D_{15}–D_8. Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. (See table on page 8.) The S_7 status information is available during T_2, T_3, and T_4. The signal is active LOW, and floats to 3-state OFF in "hold". It is LOW during T_1 for the first interrupt acknowledge cycle.

$\overline{RD}$ (OUTPUT 3-STATE)

Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the S_2 pin. This signal is used to read devices which reside on the 8086 local bus. $\overline{RD}$ is active LOW during T_2, T_3 and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the 8086 local bus has floated.

This signal floats to 3-state OFF in "hold acknowledge".

READY (INPUT)

READY is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory/IO is synchronized by the 8284 Clock Generator to form READY. This signal is active HIGH.

INTR (INPUT)

Interrupt request is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.

$\overline{TEST}$ (INPUT)

The $\overline{TEST}$ input is examined by the "Wait For Test" instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.

NMI (INPUT)

Non-maskable interrupt is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.

RESET (INPUT)

RESET causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.

CLK (INPUT)

The clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.

V_{CC}

V_{CC} is the $+5V \pm 10\%$ power supply pin.

GND

GND are the ground pins

The following pin function descriptions are for the 8086 minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

M/$\overline{IO}$ (OUTPUT 3-STATE)

This status line is logically equivalent to S_2 in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ floats to 3-state OFF in local bus "hold acknowledge".

$\overline{WR}$ (OUTPUT 3-STATE)

Write strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T_2, T_3 and T_W of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".

$\overline{INTA}$ (OUTPUT 3-STATE)

$\overline{INTA}$ is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3 and T_W of each interrupt acknowledge cycle. $\overline{INTA}$ floats to 3-state OFF in "hold acknowledge".

ALE (OUTPUT)

Address latch enable is provided by the processor to latch the address into the 8282/8283 address latch. It is a HIGH pulse active during T_1 of any bus cycle. Note that ALE is never floated.

DT/$\overline{R}$ (OUTPUT 3-STATE)

Data transmit/receive is needed in minimum system that desires to use an 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{R}$ is equivalent to $\overline{S_1}$ in the maximum mode, and its timing is the same as for M/$\overline{IO}$. (T = HIGH, R = LOW.) This signal floats to 3-state OFF in local bus "hold acknowledge".

$\overline{DEN}$ (OUTPUT 3-STATE)

Data enable is provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle it is active from the middle of T_2 until the middle of T_4, while for a write cycle it is active from the beginning of T_2 until the middle of T_4. $\overline{DEN}$ floats to 3-state OFF in local bus "hold acknowledge".

HOLD (INPUT), HLDA (OUTPUT)

HOLD indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of T_4 or T_I. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWer HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. (See Figure 13.)

The following pin function descriptions are for the 8086/8288 system in maximum mode (i.e., MN/$\overline{MX}$ = V_{SS}). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

$\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ (OUTPUT 3-STATE)

These status lines are encoded as follows:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1 (HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

Status is active during T_4, T_1, and T_2 and is returned to the passive state (1,1,1) during T_3 or during T_W when READY is HIGH. This status is used by the 8288 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$, or $\overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle.

These signals float to 3-state OFF in "hold acknowledge".

$\overline{RQ}/\overline{GT_0}$, $\overline{RQ}/\overline{GT_1}$ (INPUT/OUTPUT)

The request/grant pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor so may be left unconnected. The request/grant sequence is as follows (see Figure 12):

1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 8086 (pulse 1).
2. During the CPU's next T_4 or T_1 a pulse 1 CLK wide from the 8086 to the requesting master (pulse 2), indicates that the 8086 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK . The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge".
3. A pulse 1 CLK wide from the requesting master indicates to the 8086 (pulse 3) that the "hold" request is about to end and that the 8086 can reclaim the local bus at the next CLK. The CPU then enters T_4.

Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.

$\overline{LOCK}$ (OUTPUT 3-STATE)

The $\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in "hold acknowledge".

QS_1, QS_0 (OUTPUT)

QS_1 and QS_0 provide status to allow external tracking of the internal 8086 instruction queue.

QS_1	QS_0	
0 (LOW)	0	No Operation
0	1	First Byte of Op Code from Queue
1 (HIGH)	0	Empty the Queue
1	1	Subsequent Byte from Queue

The queue status is valid during the CLK cycle after which the queue operation is performed.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.3 to +7V
Power Dissipation . . . . . 2.5 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

8086/8086-4: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 400 μA
I_{CC}	Power Supply Current		275	mA	
I_{LI}	Input Leakage Current		±10	μA	$V_{IN} = V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	$V_{CC}+1.0$	V	
C_{IN}	Capacitance of Input Buffer (All input except AD_0-AD_{15}, RQ/GT)		10	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD_0-AD_{15}, RQ/GT)		20	pF	fc = 1 MHz

A.C. CHARACTERISTICS

8086/8086-4: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

8086 MINIMUM COMPLEXITY SYSTEM (Figure 8) TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TCLCL	CLK Cycle Period — 8086 — 8086-4	200 250	2000 2000	ns ns	
TCLCH	CLK Low Time	(⅔TCLCL)-15		ns	
TCHCL	CLK High Time	(⅓TCLCL)+2		ns	
TCH1CH2	CLK Rise Time		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10	ns	From 3.5V to 1.0V
TDVCL	Data In Setup Time	30		ns	
TCLDZ	Data In Hold Time	10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes 1, 2)	0		ns	
TRYHCH	READY Setup Time into 8086	(⅔TCLCL)-15		ns	
TCHRYX	READY Hold Time into 8086	30		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	-8		ns	
THVCH	Hold Setup Time	35		ns	
TINVCH	INTR, NMI, $\overline{TEST}$ Setup Time (See Note 2)	30		ns	

TIMING RESPONSES

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TCLAV	Address Valid Delay	15	110	ns	
TCLAX	Address Hold Time	10		ns	
TCLAZ	Address Float Delay	TCLAX	80	ns	
TLHLL	ALE Width	TCLCH-20		ns	
TCLLH	ALE Active Delay		80	ns	
TCHLL	ALE Inactive Delay		85	ns	
TLLAZ	ALE Inactive to Address Float	TCHCL-10		ns	
TCLDV	Data Valid Delay	15	110	ns	
TCHDZ	Data Float Delay	TCLAX	85	ns	C_L = 20-100 pF for all 8086 Outputs
TWHDZ	Data Hold Time After $\overline{WR}$	TCLCH-30		ns	
TCVCTV	Control Active Delay 1	10	110	ns	
TCHCTV	Control Active Delay 2	15	110	ns	
TCVCTX	Control Inactive Delay	10	110	ns	
TAZRL	Address Float to READ Active	0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-45		ns	
TCLHAV	HLDA Valid Delay	10	160	ns	

NOTES: 1. SIGNAL AT 8284 SHOWN FOR REFERENCE ONLY.
2. SETUP REQUIREMENT FOR ASYNCHRONOUS SIGNAL ONLY TO GUARANTEE RECOGNITION AT NEXT CLK.
3. APPLIES ONLY TO T2 STATE.

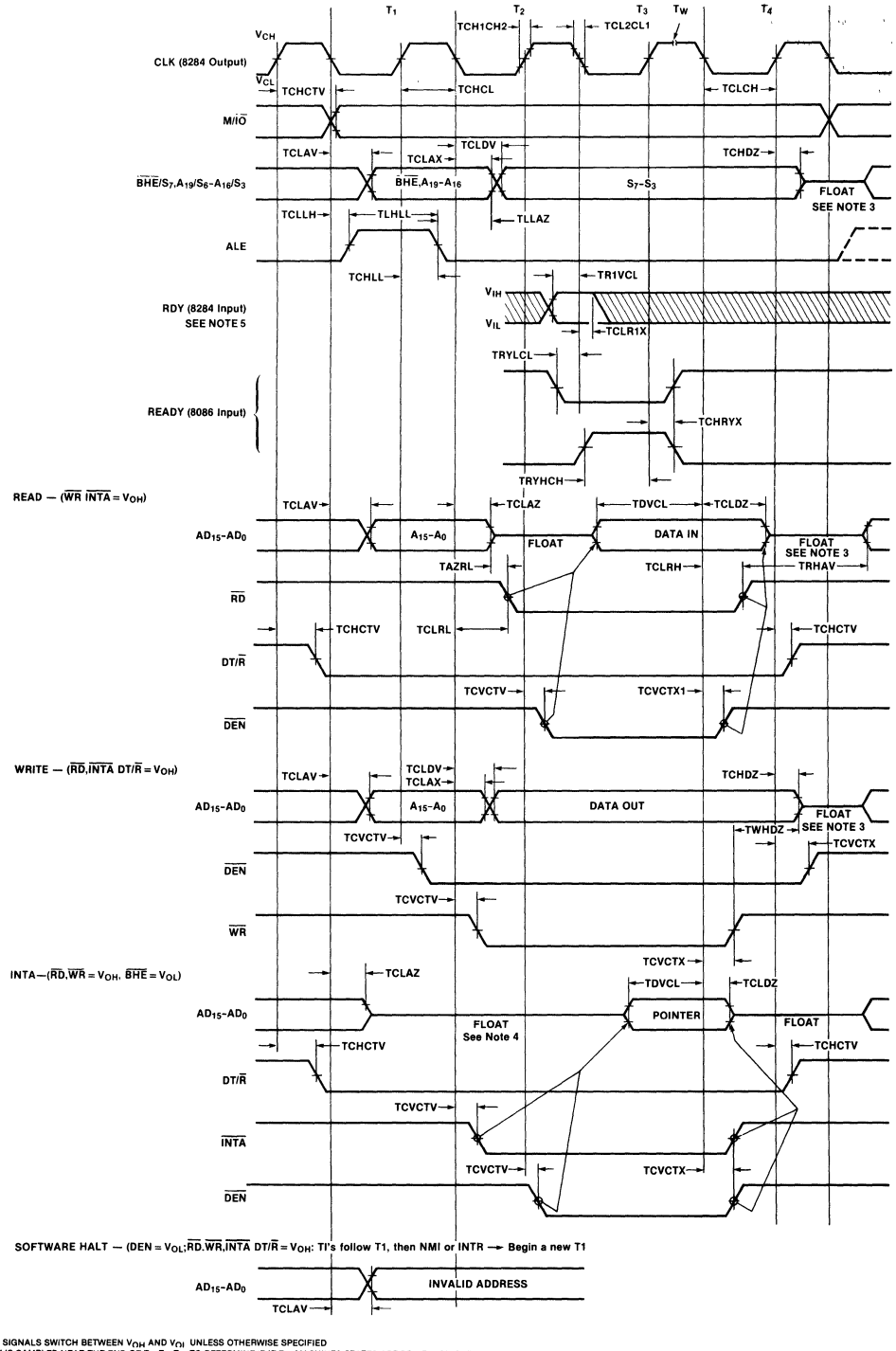
8086 MAX MODE SYSTEM (USING 8288 BUS CONTROLLER) (Figure 9) TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TCLCL	CLK Cycle Period — 8086 — 8086-4	200 250	2000 2000	ns ns	
TCLCH	CLK Low Time	(2/3TCLCL)-15		ns	
TCHCL	CLK High Time	(1/3TCLCL) + 2		ns	
TCH1CH2	CLK Rise Time		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10	ns	From 3.5V to 1.0V
TDVCL	Data In Setup Time	30		ns	
TCLDZ	Data In Hold Time	10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes 1, 2)	0		ns	
TRYHCH	READY Setup Time into 8086	(2/3TCLCL)-15		ns	
TCHRYX	READY Hold Time into 8086	30		ns	
TRYLCL	READY Inactive to CLK (See Note 4)	-8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) (See Note 2)	30		ns	
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time	35		ns	
TCHGX	$\overline{RQ}$ Hold Time into 8086	40		ns	

TIMING RESPONSES

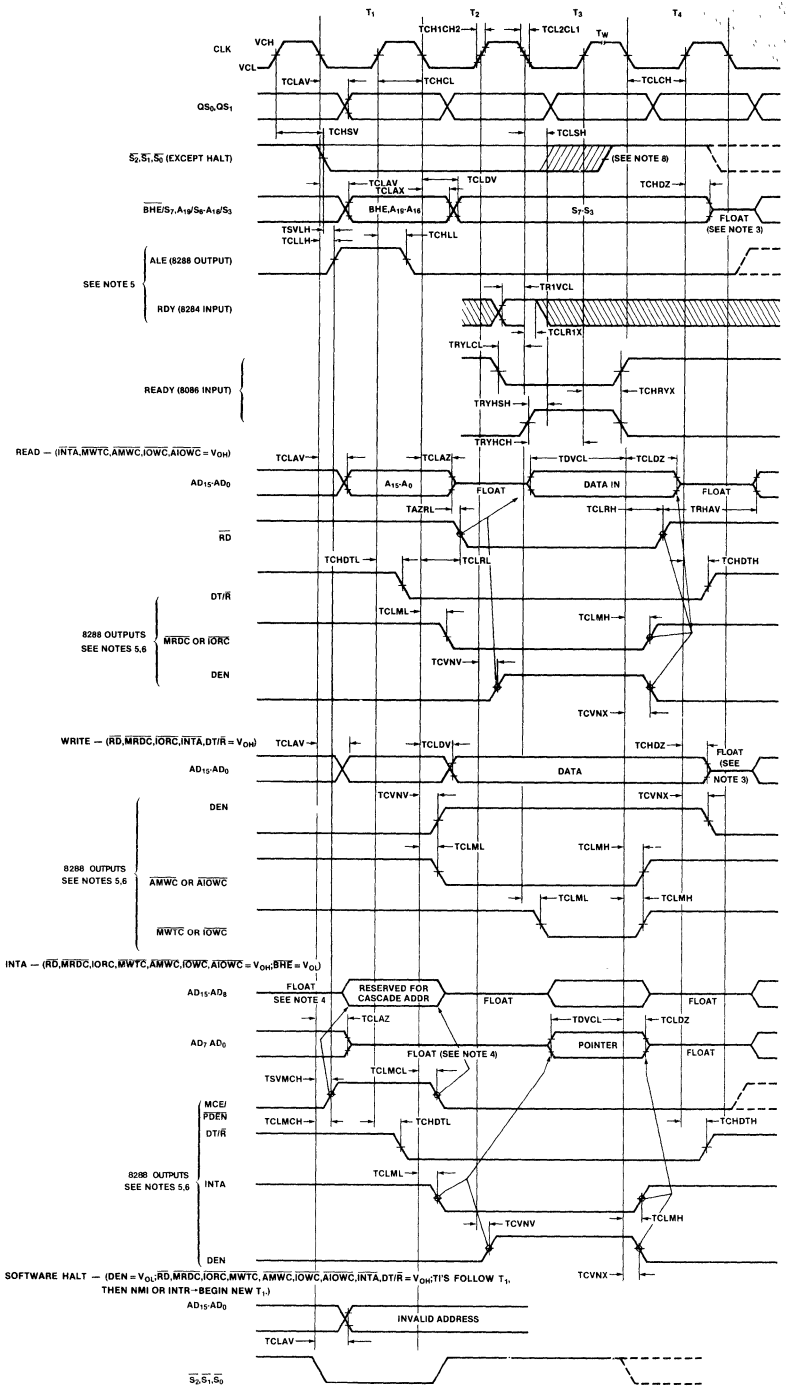
Symbol	Parameter	Min.	Max.	Units	Test Conditions
TCLML	Command Active Delay (See Note 1)	10	35	ns	
TCLMH	Command Inactive Delay (See Note 1)	10	35	ns	
TRYHSH	READY Active to Status Passive (See Note 3)		110	ns	
TCHSV	Status Active Delay	10	110	ns	
TCLSH	Status Inactive Delay	10	130	ns	
TCLAV	Address Valid Delay	15	110	ns	
TCLAX	Address Hold Time	10		ns	
TCLAZ	Address Float Delay	TCLAX	80	ns	
TSVLH	Status Valid to ALE High (See Note 1)		15	ns	
TSVMCH	Status Valid to MCE High (See Note 1)		15	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		15	ns	
TCLMCH	CLK Low to MCE High (See Note 1)		15	ns	
TCHLL	ALE Inactive Delay (See Note 1)		15	ns	C_L = 20-100 pF for all 8086 Outputs
TCLMCL	MCE Inactive Delay (See Note 1)		15	ns	
TCLDV	Data Valid Delay	15	110	ns	
TCHDZ	Data Float Delay	TCLAX	85	ns	
TCVNV	Control Active Delay (See Note 1)	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	ns	
TAZRL	Address Float to Read Active	0		ns	
TCLRL	RD Active Delay	10	165	ns	
TCLRH	RD Inactive Delay	10	150	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL-45		ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30	ns	
TCLGL	$\overline{GT}$ Active Delay		85	ns	
TCLGH	$\overline{GT}$ Inactive Delay		85	ns	

NOTES: 1. SIGNAL AT 8284 OR 8288 SHOWN FOR REFERENCE ONLY.
2. SETUP REQUIREMENT FOR ASYNCHRONOUS SIGNAL ONLY TO GUARANTEE RECOGNITION AT NEXT CLK.
3. APPLIES ONLY TO T3 AND WAIT STATES.
4. APPLIES ONLY TO T2 STATE.



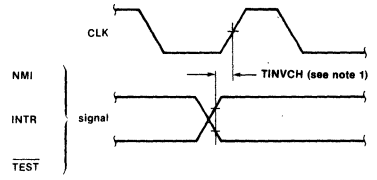
NOTES: 1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED
3. FOLLOWING A WRITE CYCLE THE LOCAL BUS IS FLOATED BY THE 8086 ONLY WHEN THE 8086 ENTERS A "HOLD ACKNOWLEDGE" STATE
4. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8086 LOCAL ADDR/DATA BUS IS FLOATING DURING THE SECOND INTA CYCLE
5. SIGNALS AT 8284 ARE SHOWN FOR REFERENCE ONLY.
6. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

Figure 8. 8086 Bus Timing — Minimum Mode System



NOTES: 1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED
3 FOLLOWING A WRITE CYCLE THE LOCAL BUS IS FLOATED BY THE 8086 ONLY WHEN THE 8086 ENTERS A "HOLD ACKNOWLEDGE" STATE
4 TWO INTA CYCLES RUN BACK-TO-BACK. THE 8086 LOCAL ADDR/DATA BUS IS FLOATING DURING THE SECOND INTA CYCLE
5 SIGNALS AT 8284 OR 8288 ARE SHOWN FOR REFERENCE ONLY
6 THE ISSUANCE OF THE 8288 COMMAND AND CONTROL SIGNALS (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA AND DEN) LAGS THE ACTIVE HIGH 8288 CEN
7 ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.
8 STATUS INACTIVE IN STATE JUST PRIOR TO T_4

Figure 9. 8086 Bus Timing — Maximum Mode System (Using 8288)



NOTE:

1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK

Figure 10. Asynchronous Signal Recognition

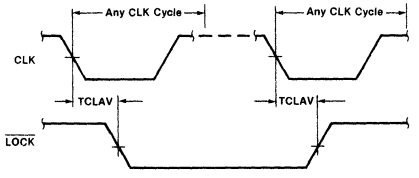
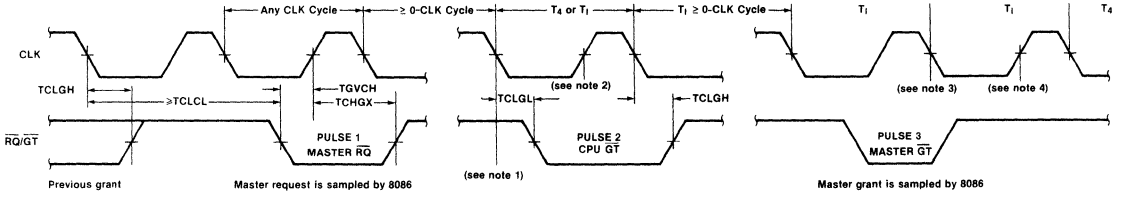


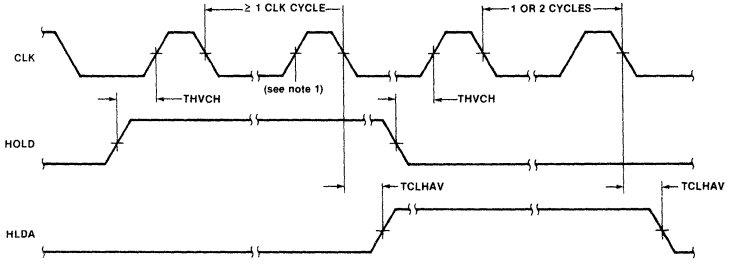
Figure 11. Bus Lock Signal Timing (Maximum Mode Only)



NOTES:

1. THE 8086 FLOATS $\overline{S_2}$,$\overline{S_1}$,$\overline{S_0}$ FROM 1.1.1 STATE ON THIS EDGE
2. THE 8086 FLOATS A_xD_x BUS $\overline{RD}$ AND $\overline{LOCK}$ ON THIS EDGE
3. THE OTHER MASTER FLOATS $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ FROM 1.1.1 STATE ON THIS EDGE
4. THE OTHER MASTER FLOATS A_xD_x $\overline{BUS}$, BHE, AND $\overline{LOCK}$ ON THIS EDGE

Figure 12. Request/Grant Sequence Timing (Maximum Mode Only)



NOTE:

1. BUS FLOATS ON THIS EDGE (SEE TCHDZ)

Figure 13. Hold/Hold Acknowledge Timing (Minimum Mode Only)

8086
INSTRUCTION SET SUMMARY

TRANSFER

Move:	3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
e to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
e to register	1 0 1 1 w reg	data	data if w=1	
to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
ator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
memory to segment registe	1 0 0 0 1 1 1 0	mod 0 reg r/m		
register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
Push:				
memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
	0 1 0 reg			
register	0 reg 1 1 0			
Pop:				
/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
	0 1 1 reg			
register	0 reg 1 1 1			
Exchange:				
/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		
with accumulator	1 0 0 1 0 reg			
In from:				
fixed port	1 1 1 0 0 1 0 w	port		
variable port	1 1 1 0 1 1 0 w			
Output to:				
fixed port	1 1 1 0 0 1 1 w	port		
variable port	1 1 1 0 1 1 1 w			
Translate byte to AL	1 1 0 1 0 1 1 1			
Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m		
Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
Load AH with flags	1 0 0 1 1 1 1 1			
Store AH into flags	1 0 0 1 1 1 1 0			
PUSH flags	1 0 0 1 1 1 0 0			
POP flags	1 0 0 1 1 1 0 1			

ARITHMETIC

Add:				
Memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w=01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w=1	
Add with carry:				
Memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w=01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w=1	
Increment:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
ASCII adjust for add	0 0 1 1 0 1 1 1			
Decimal adjust for add	0 0 1 0 0 1 1 1			
Subtract:				
Memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w=01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w=1	
Subtract with borrow				
Memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w=01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w=1	

DEC = Decrement:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG=Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP = Compare:				
Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w=01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w=1	
AAS=ASCII adjust for subtract	0 0 1 1 1 1 1 1			
DAS=Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL=Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL=Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM=ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV=Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV=Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD=ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW=Convert byte to word	1 0 0 1 1 0 0 0			
CWD=Convert word to double word	1 0 0 1 1 0 0 1			

LOGIC

NOT=Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL=Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR=Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR=Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL=Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR=Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL=Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR=Rotate through carry right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg /memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1	
TEST = And function to flags, no result:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1	
OR = Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1	
XOR = Exclusive or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w=1	

STRING MANIPULATION

REP=Repeat	1 1 1 1 0 0 1 z
MOVS=Move byte/word	1 0 1 0 0 1 0 w
CMPS=Compare byte/word	1 0 1 0 0 1 1 w
SCAS=Scan byte/word	1 0 1 0 1 1 1 w
LODS=Load byte/wd to AL/AX	1 0 1 0 1 1 0 w
STDS=Stor byte/wd from AL/A	1 0 1 0 1 0 1 w

MCS-86

CONTROL TRANSFER

CALL = Call:	76543210	76543210	76543210
Direct within segment	11101000	disp-low	disp-high
Indirect within segment	11111111	mod 010 r/m	
Direct intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 011 r/m	

JMP = Unconditional Jump:			
Direct within segment	11101001	disp-low	disp-high
Direct within segment-short	11101011	disp	
Indirect within segment	11111111	mod 100 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 101 r/m	

RET = Return from CALL:			
Within segment	11000011		
Within seg. adding immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment, adding immediate to SP	11001010	data-low	data-high

	76543210	
JE/JZ=Jump on equal/zero	01110100	disp
JL/JNGE=Jump on less/not greater or equal	01111100	disp
JLE/JNG=Jump on less or equal/not greater	01111110	disp
JB/JNAE=Jump on below/not above or equal	01110010	disp
JBE/JNA=Jump on below or equal/ not above	01110110	disp
JP/JPE=Jump on parity/parity even	01111010	disp
JO=Jump on overflow	01110000	disp
JS=Jump on sign	01111000	disp
JNE/JNZ=Jump on not equal/not zero	01110101	disp
JNL/JGE=Jump on not less/greater or equal	01111101	disp
JNLE/JG=Jump on not less or equal/ greater	01111111	disp
JNB/JAE=Jump on not below/above or equal	01110011	disp
JNBE/JA=Jump on not below or equal/above	01110111	disp
JNP/JPO=Jump on not par/par odd	01111011	disp
JNO=Jump on not overflow	01110001	disp
JNS=Jump on not sign	01111001	disp
LOOP=Loop CX times	11100010	disp
LOOPZ/LOOPE=Loop while zero/equal	11100001	disp
LOOPNZ/LOOPNE=Loop while not zero/equal	11100000	disp
JCXZ=Jump on CX zero	11100011	disp

INT = Interrupt		
Type specified	11001101	type
Type 3	11001100	
INTO=Interrupt on overflow	11001110	
IRET=Interrupt return	11001111	

PROCESSOR CONTROL

CLC=Clear carry	11111000	
CMC=Complement carry	11110101	
STC=Set carry	11111001	
CLD=Set direction	11111100	
STD=Set direction	11111101	
CLI=Clear interrupt	11111010	
STI=Set interrupt	11111011	
HLT=Halt	11110100	
WAIT=Wait	10011011	
ESC=Escape (to external device)	11011 x x x	mod x x x r/m
LOCK=Bus lock prefix	11110000	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

001 reg 110

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

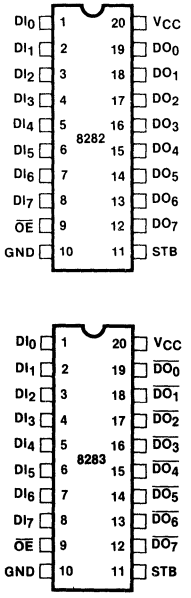
FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

8282/8283
OCTAL LATCH

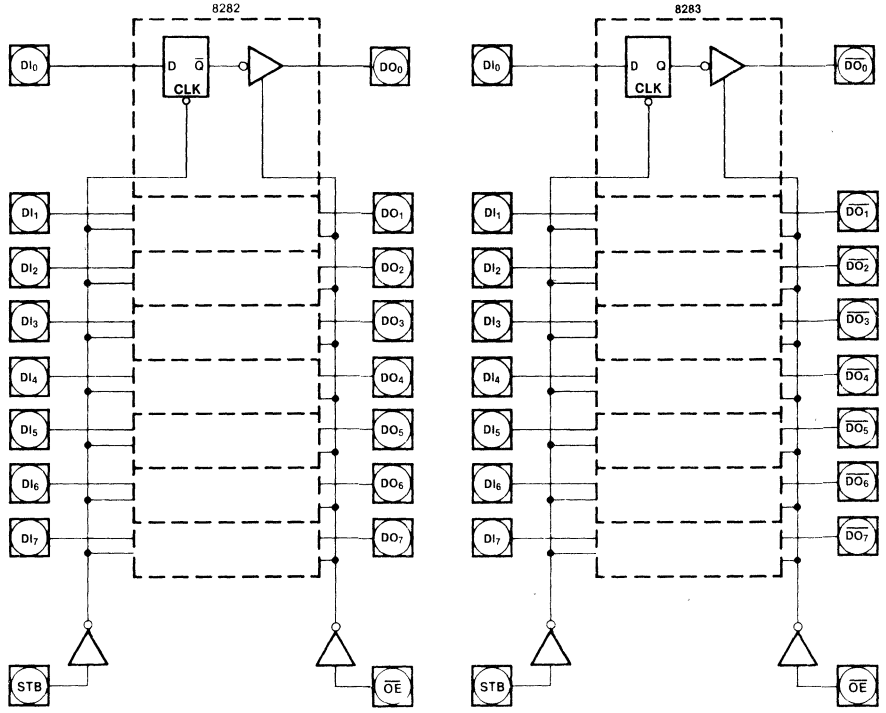
- **Fully Parallel 8-Bit Data Register and Buffer**
- **Transparent during Active Strobe**
- **Supports 8080, 8085, 8048, and 8086 Systems**
- **High Output Drive Capability for Driving System Data Bus**
- **3-State Outputs**
- **20-Pin Package with 0.3" Center**
- **No Output Low Noise when Entering or Leaving High Impedance State**

The 8282 and 8283 are 8-bit bipolar latches with 3-state output buffers. They can be used to implement latches, buffers, or multiplexers. The 8283 inverts the input data at its outputs while the 8282 does not. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with these devices.

PIN CONFIGURATIONS



LOGIC DIAGRAMS



PIN NAMES

DI_0-DI_7	DATA IN
DO_0-DO_7	DATA OUT
$\overline{OE}$	OUTPUT ENABLE
STB	STROBE

PIN DEFINITIONS

Pin	Description
STB	STROBE (Input). STB is an input control pulse used to strobe data at the data input pins (A_0-A_7) into the data latches. This signal is active HIGH to admit input data. The data is latched at the HIGH to LOW transition of STB.
$\overline{OE}$	OUTPUT ENABLE (Input). $\overline{OE}$ is an input control signal which when active LOW enables the contents of the data latches onto the data output pin (B_0-B_7). OE being inactive HIGH forces the output buffers to their high impedance state.
DI_0-DI_7	DATA INPUT PINS (Input). Data presented at these pins satisfying setup time requirements when STB is strobed and latched into the data input latches.
DO_0-DO_7 (8282) $\overline{DO_0}$-$\overline{DO_7}$ (8283)	DATA OUTPUT PINS (Output). When $\overline{OE}$ is true, the data in the data latches is presented as inverted (8283) or non-inverted (8282) data onto the data output pins.

OPERATIONAL DESCRIPTION

The 8282 and 8283 octal latches are 8-bit latches with 3-state output buffers. Data having satisfied the setup time requirements is latched into the data latches by strobing the STB line HIGH to LOW. Holding the STB line in its active HIGH state makes the latches appear transparent. Data is presented to the data output pins by activating the $\overline{OE}$ input line. When $\overline{OE}$ is inactive HIGH the output buffers are in their high impedance state. Enabling or disabling the output buffers will not cause negative-going transients to appear on the data output bus.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS FOR 8282/8283

Conditions: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_C	Input Clamp Voltage		−1	V	$I_C = -5$ mA
I_{CC}	Power Supply Current		160	mA	
I_F	Forward Input Current		−0.2	mA	$V_F = 0.45V$
I_R	Reverse Input Current		50	μA	$V_R = 5.25V$
V_{OL}	Output Low Voltage		0.50	V	$I_{OL} = 32$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -5$ mA
I_{OFF}	Output Off Current		±50	μA	$V_{OFF} = 0.45$ to $5.25V$
V_{IL}	Input Low Voltage		0.8	V	$V_{CC} = 5.0V$ See Note 1
V_{IH}	Input High Voltage	2.0		V	$V_{CC} = 5.0V$ See Note 1
C_{IN}	Input Capacitance		12	pF	F = 1 MHz $V_{BIAS} = 2.5V$, $V_{CC} = 5V$ $T_A = 25°C$

Notes: 1. Output Loading $I_{OL} = 32$ mA, $I_{OH} = -5$ mA, $C_L = 300$ pF

A.C. CHARACTERISTICS FOR 8282/8283

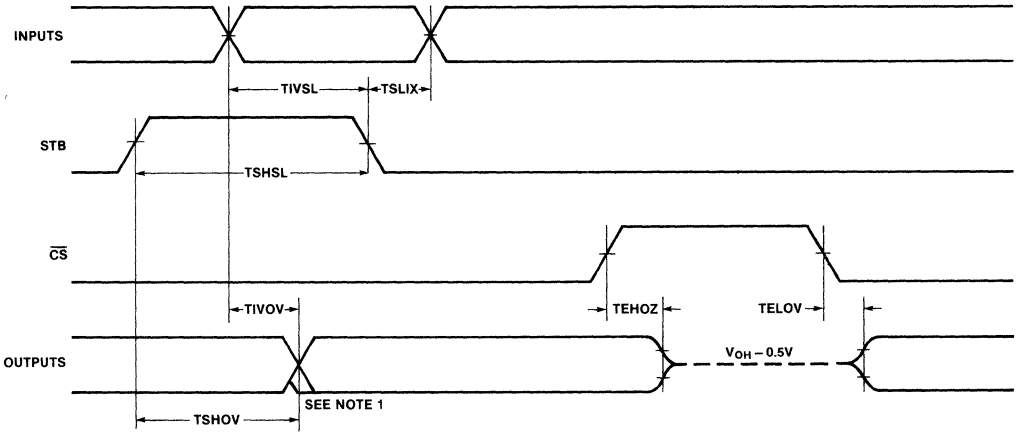
Conditions: $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Loading: Outputs — I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF

Symbol	Parameter	Min	Max	Units	Test Conditions
TIVOV	Input to Output Delay —Inverting —Non-Inverting		 25 35	 ns ns	(See Note 1)
TSHOV	STB to Output Delay —Inverting —Non-Inverting		 45 55	 ns ns	
TEHOZ	Output Disable Time		25	ns	
TELOV	Output Enable Time	10	50	ns	
TIVSL	Input to STB Setup Time	0		ns	
TSLIX	Input to STB Hold Time	25		ns	
TSHSL	STB High Time	15		ns	

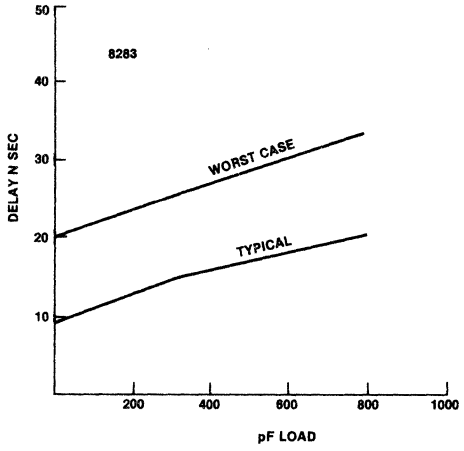
NOTE: 1. See waveforms and test load circuit on following page.

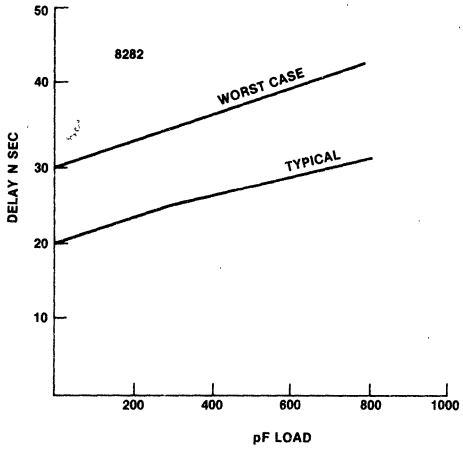
8282/8283 TIMING



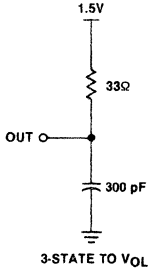
NOTE: 1. 8283 ONLY — OUTPUT MAY BE MOMENTARILY INVALID FOLLOWING THE HIGH GOING STB TRANSITION.
2. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED

OUTPUT DELAY VS. CAPACITANCE

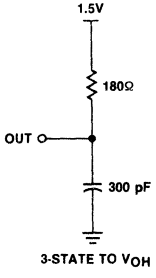




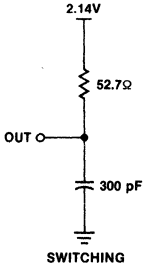
OUTPUT TEST LOAD CIRCUITS



3-STATE TO V_{OL}



3-STATE TO V_{OH}



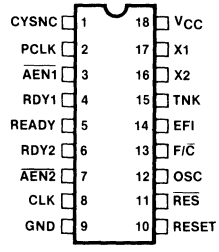
SWITCHING

8284
CLOCK GENERATOR AND DRIVER FOR 8086 CPU

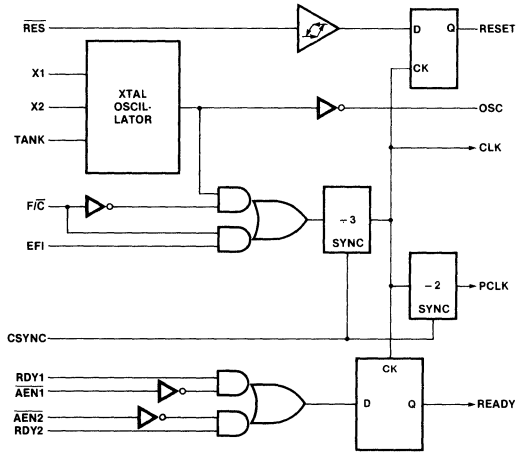
- **Generates the System Clock for the 8086**
- **Uses a Crystal or a TTL Signal for Frequency Source**
- **Single +5V Power Supply**
- **18-Pin Package**
- **Generates System Reset Output from Schmitt Trigger Input**
- **Provides Local Ready and MULTIBUS™ Ready Synchronization**
- **Capable of Clock Synchronization with other 8284's**

The 8284 is a bipolar clock generator/driver designed to provide clock signals for the 8086 CPU and peripherals. It also contains READY logic for operation with two MULTIBUS™ systems and provides the 8086's required READY synchronization and timing. Reset logic with hysteresis and synchronization is also provided.

8284 PIN CONFIGURATION



8284 BLOCK DIAGRAM



8284 PIN NAMES

X1, X2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE CRYSTAL
F/C	CLOCK SOURCE SELECT
EFI	EXTERNAL CLOCK INPUT
CSYNC	CLOCK SYNCHRONIZATION INPUT
RDY1, RDY2	READY SIGNAL FROM TWO MULTIBUS™ SYSTEMS
AEN1, AEN2	ADDRESS ENABLED QUALIFIERS FOR RDY1,2
RES	RESET INPUT
RESET	SYNCHRONIZED RESET OUTPUT
OSC	OSCILLATOR OUTPUT
CLK	MOS CLOCK FOR 8086
PCLK	TTL CLOCK FOR PERIPHERALS
READY	SYNCHRONIZED READY OUTPUT
V_{CC}	+5 VOLTS
GND	0 VOLTS

PIN DEFINITIONS

Pin	I/O	Definition
$\overline{AEN1}$, $\overline{AEN2}$	I	ADDRESS ENABLE. $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
READY	O	READY. READY is an active HIGH signal which is the synchronized RDY signal input. Since RDY occurs asynchronously with respect to the processor's clock (CLK) it is necessary for them to be synchronized before being presented to the processor. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2, TNK	I	CRYSTAL IN. X1 and X2 are the pins to which a crystal is attached with TNK (TANK) serving as the overtone input. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	I	FREQUENCY/CRYSTAL SELECT. F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	EXTERNAL FREQUENCY IN. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	O	PROCESSOR CLOCK. CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle. An output HIGH of 4.5 volts (V_{CC} = 5V) is provided on this pin to drive MOS devices.
PCLK	O	PERIPHERAL CLOCK. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	O	OSCILLATOR OUTPUT. OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	RESET IN. $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 8284 provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	RESET. Reset is an active HIGH signal which is used to reset the 8086 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	I	CLOCK SYNCHRONIZATION. CSYNC is an active HIGH signal which allows multiple 8284's to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		Ground
V_{CC}		+5V supply

FUNCTIONAL DESCRIPTION

GENERAL

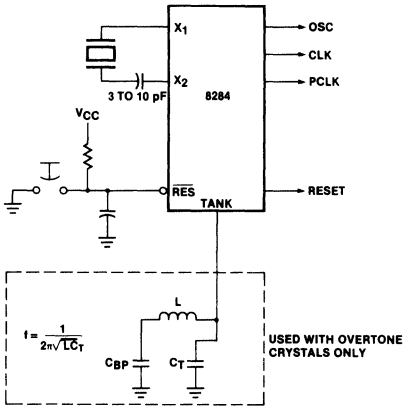
The 8284 is a single chip clock generator/driver for the 8086 CPU. The chip contains a crystal controlled oscillator, a "divide by three" counter, complete MULTIBUS™ "Ready" synchronization and reset logic.

OSCILLATOR

The oscillator circuit of the 8284 is designed primarily for use with an external series resonant, fundamental mode, crystal from which the basic operating frequency is derived. However, overtone mode crystals can be used with a tank circuit as shown in Figure 1.

The crystal frequency should be selected at three times the required CPU clock. X_1 and X_2 are the two crystal input crystal connections.

The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.



The tank input to the oscillator allows the use of overtone mode crystals. The tank circuit shunts the crystal's fundamental and high overtone frequencies and allows the third harmonic to oscillate. The external LC network is connected to the TANK input and is AC coupled to ground.

Figure 1

CLOCK GENERATOR

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 8284 clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 8284. This is accomplished with two Schottky flip-flops. (See Figure 2.) The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

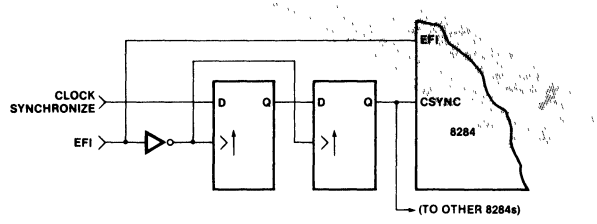


Figure 2. CSYNC Synchronization

CLOCK OUTPUTS

The CLK output is a 33% duty cycle MOS clock driver designed to drive the 8086 processor directly. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

RESET LOGIC

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power on reset by utilizing this function of the 8284.

READY SYNCHRONIZATION

Two READY inputs (RDY1, RDY2) are provided to accomomodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

The READY output is an active HIGH signal which is the synchronized RDY1 or RDY2 input. Since RDY1 and RDY2 occur asynchronously with respect to the processor's clock (CLK), it is necessary to synchronize them before presenting them to the processor to insure they meet the required set-up time. The READY logic does this job and also guarantees the required hold time before clearing the READY signal.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS FOR 8284

Conditions: $T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min	Max	Units	Test Conditions
I_F	Forward Input Current		−0.5	mA	$V_F = 0.45V$
I_R	Reverse Input Current		50	μA	$V_R = 5.25V$
V_C	Input Forward Clamp Voltage		−1.0	V	$I_C = -5$ mA
I_{CC}	Power Supply Current		140	mA	
V_{IL}	Input LOW Voltage		0.8	V	$V_{CC} = 5.0V$
V_{IH}	Input HIGH Voltage	2.0		V	$V_{CC} = 5.0V$
V_{IH_R}	Reset Input HIGH Voltage	2.6		V	$V_{CC} = 5.0V$
V_{OL}	Output LOW Voltage		0.45	V	5 mA
V_{OH}	Output HIGH Voltage CLK Other Outputs	4 2.4		V V	−1 mA −1 mA
V_{IH_R}-V_{IL_R}	$\overline{RES}$ Input Hysteresis	0.25		V	$V_{CC} = 5.0V$

A.C. CHARACTERISTICS FOR 8284

Conditions: $T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

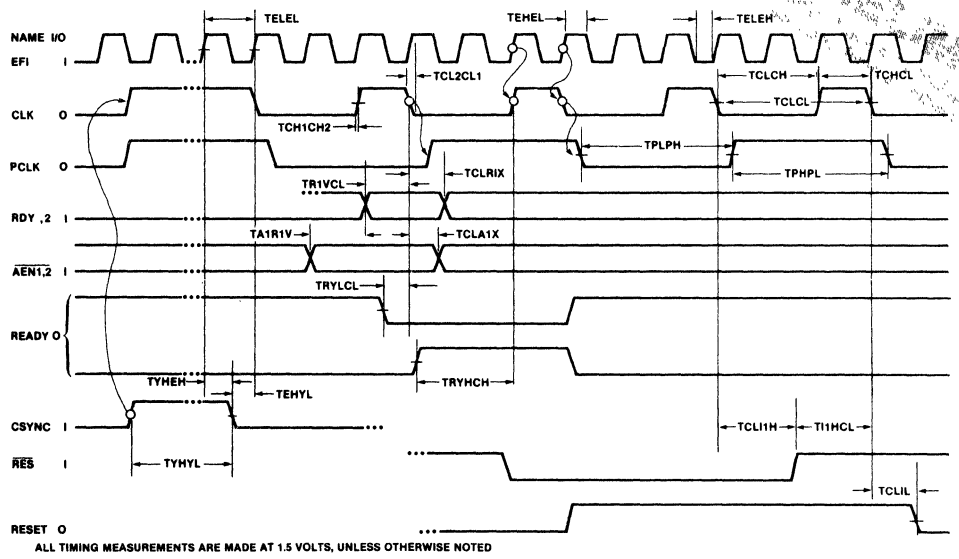
TIMING REQUIREMENTS

Symbol	Parameter	Min	Max	Units	Test Conditions
TEHEL	External Frequency High Time	20		ns	
TELEH	External Frequency Low Time	20		ns	
TELEL	EFI Period	TEHEL + TELEH + δ		ns	(Note 1)
	XTAL Frequency	12	25	MHz	
TR1VCL	RDY1, RDY2 Set-Up to CLK	35		ns	
TCLR1X	RDY1, RDY2 Hold to CLK	0		ns	
TA1VR1V	$\overline{AEN1}$, $\overline{AEN2}$ Set-Up to RDY1, RDY2	15		ns	
TCLA1X	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		ns	
TYHEH	CSYNC Set-Up to EFI	20		ns	
TEHYL	CSYNC Hold to EFI	20		ns	
TYHYL	CSYNC Width	2·TELEL		ns	
TI1HCL	$\overline{RES}$ Set-Up to CLK	65		ns	(Note 2)
TCLI1H	$\overline{RES}$ Hold to CLK	20		ns	(Note 2)

TIMING RESPONSES

Symbol	Parameter	Min	Max	Units	Test Conditions
TCLCL	CLK Cycle Period	125		ns	
TCHCL	CLK High Time	(⅓TCLCL) + 2.0		ns	Fig. 3 & Fig. 4
TCLCH	CLK Low Time	(⅔TCLCL) − 15.0		ns	Fig. 3 & Fig. 4
TCH1CH2 TCL2CL1	CLK Rise and Fall Time		10	ns	1.0V to 3.5V
TPHPL	PCLK High Time	TCLCL − 20		ns	
TPLPH	PCLK Low Time	TCLCL − 20		ns	
TRYLCL	Ready Inactive to CLK (See Note 4)	−8		ns	Fig. 5 & Fig. 6
TRYHCH	Ready Active to CLK (See Note 3)	(⅔TCLCL)−15.0		ns	Fig. 5 & Fig. 6
TCLIL	CLK to Reset Delay	40		ns	

Notes: 1. δ = EFI rise + EFI fall.
2. Set up and hold only necessary to guarantee recognition at next clock.
3. Applies only to T3 and TW states.
4. Applies only to T2 states.



ALL TIMING MEASUREMENTS ARE MADE AT 1.5 VOLTS, UNLESS OTHERWISE NOTED

A.C. TEST CIRCUITS

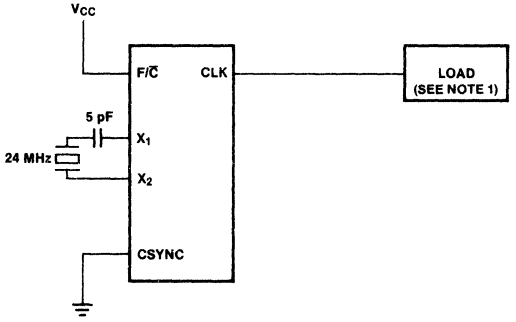


Figure 3. Clock High and Low Time

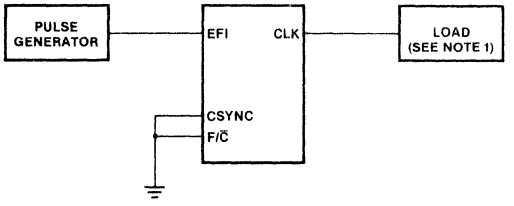


Figure 4. Clock High and Low Time

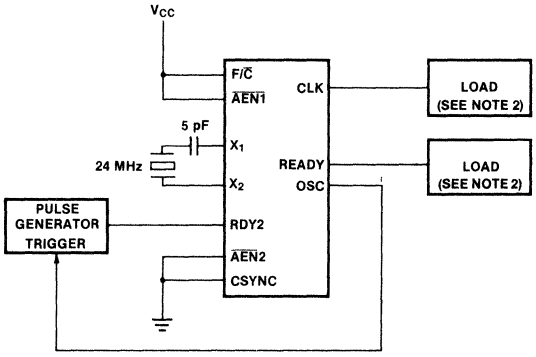


Figure 5. Ready to Clock

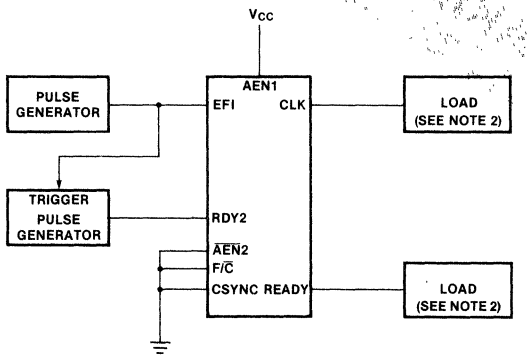
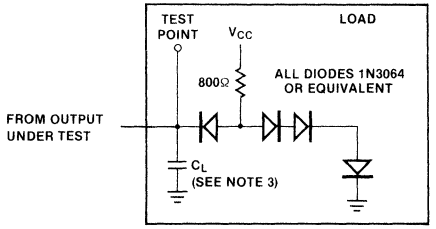


Figure 6. Ready to Clock



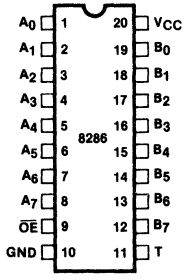
NOTES: 1. $C_L = 100$ pF
2. $C_L = 30$ pF
3. C_L INCLUDES PROBE AND JIG CAPACITANGE

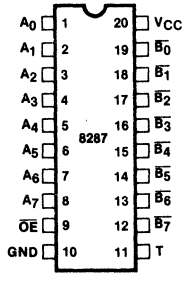
8286/8287
OCTAL BUS TRANSCEIVER

- **Data Bus Buffer Driver for MCS-86™, MCS-80™, MCS-85™, and MCS-48™ Families**
- **High Output Drive Capability for Driving System Data Bus**
- **Fully Parallel 8-Bit Transceivers**
- **3-State Outputs**
- **20-Pin Package with 0.3" Center**
- **No Output Low Noise when Entering or Leaving High Impedance State**

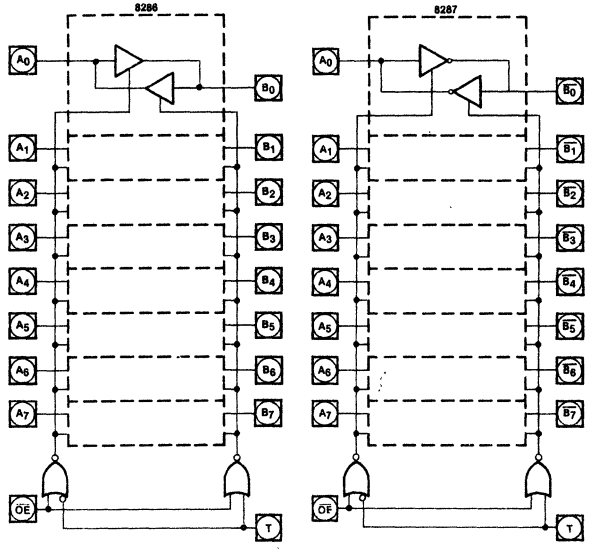
The 8286 and 8287 are 8-bit bipolar transceivers with 3-state outputs. The 8287 inverts the input data at its outputs while the 8286 does not. Thus, a wide variety of applications for buffering in microcomputer systems can be met.

PIN CONFIGURATIONS





LOGIC DIAGRAMS



PIN NAMES

A_0-A_7	LOCAL BUS DATA
B_0-B_7	SYSTEM BUS DATA
$\overline{OE}$	OUTPUT ENABLE
T	TRANSMIT

PIN DEFINITIONS

Pin	Description
T	TRANSMIT (Input). T is an input control signal used to control the direction of the transceivers. When HIGH, it configures the transceiver's B_0-B_7 as outputs with A_0-A_7 as inputs. T LOW configures A_0-A_7 as the outputs with B_0-B_7 serving as the inputs.
$\overline{OE}$	OUTPUT ENABLE (Input). $\overline{OE}$ is an input control signal used to enable the appropriate output driver (as selected by T) onto its respective bus. This signal is active LOW.
A_0-A_7	LOCAL BUS DATA PINS (Input/Output). These pins serve to either present data to or accept data from the processor's local bus depending upon the state of the T pin.
B_0-B_7 (8286) $\overline{B_0}$-$\overline{B_7}$ (8287)	SYSTEM BUS DATA PINS (Input/Output). These pins serve to either present data to or accept data from the system bus depending upon the state of the T pin.

OPERATIONAL DESCRIPTION

The 8286 and 8287 transceivers are 8-bit transceivers with high impedance outputs. With T active HIGH and $\overline{OE}$ active LOW, data at the A_0-A_7 pins is driven onto the B_0-B_7 pins. With T inactive LOW and $\overline{OE}$ active LOW, data at the B_0-B_7 pins is driven onto the A_0-A_7 pins. No output low glitching will occur whenever the transceivers are entering or leaving the high impedance state.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS FOR 8286/8287

Conditions: V_{CC} = 5V ±5%, T_A = 0°C to 70°C

Symbol	Parameter	Min	Max	Units	Test Conditions
V_C	Input Clamp Voltage		-1	V	I_C = -5 mA
I_{CC}	Power Supply Current—8287 —8286		130 160	mA mA	
I_F	Forward Input Current		-0.2	mA	V_F = 0.45V
I_R	Reverse Input Current		50	μA	V_R = 5.25V
V_{OL}	Output Low Voltage —B Outputs —A Outputs		0.5 0.5	V V	I_{OL} = 32 mA I_{OL} = 10 mA
V_{OH}	Output High Voltage —B Outputs —A Outputs	2.4 2.4		V V	I_{OH} = -5 mA I_{OH} = -1 mA
I_{OFF} I_{OFF}	Output Off Current Output Off Current		I_F I_R		V_{OFF} = 0.45V V_{OFF} = 5.25V
V_{IL}	Input Low Voltage —A Side —B Side		0.8 0.9	V V	V_{CC} = 5.0V, See Note 1 V_{CC} = 5.0V, See Note 1
V_{IH}	Input High Voltage	2.0		V	V_{CC} = 5.0V, See Note 1
C_{IN}	Input Capacitance		12	pF	F = 1 MHz V_{BIAS} = 2.5V, V_{CC} = 5V T_A = 25°C

Note: 1. B Outputs — I_{OL} = 32 mA, I_{OH} = -5 mA, C_L = 300 pF A Outputs — I_{OL} = 10 mA, I_{OH} = -1 mA, C_L = 100 pF

A.C. CHARACTERISTICS FOR 8286/8287

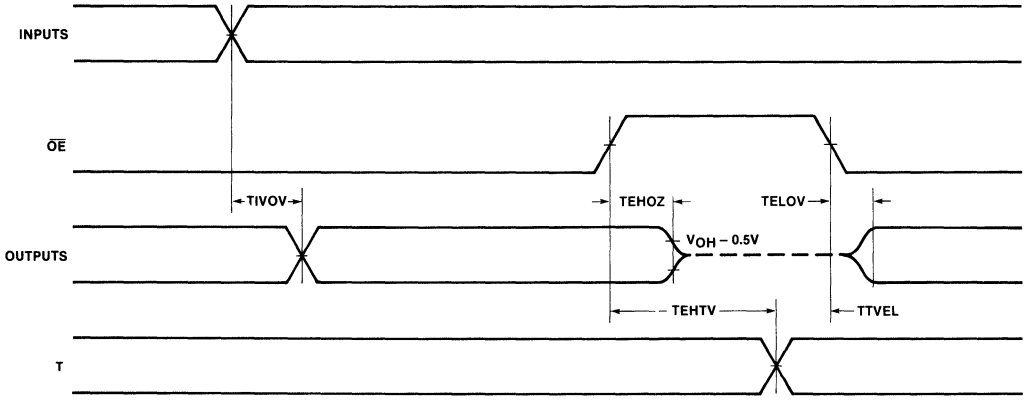
Conditions: V_{CC} = 5V ±5%, T_A = 0°C to 70°C

Loading: B Outputs — I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF
A Outputs — I_{OL} = 10 mA, I_{OH} = −1 mA, C_L = 100 pF

Symbol	Parameter	Min	Max	Units	Test Conditions
TIVOV	Input to Output Delay Inverting Non-Inverting		 25 35	 ns ns	(See Note 1)
TEHTV	Transmit/Receive Hold Time	TEHOZ		ns	
TTVEL	Transmit/Receive Setup	30		ns	
TEHOZ	Output Disable Time		25	ns	
TELOV	Output Enable Time	10	50	ns	

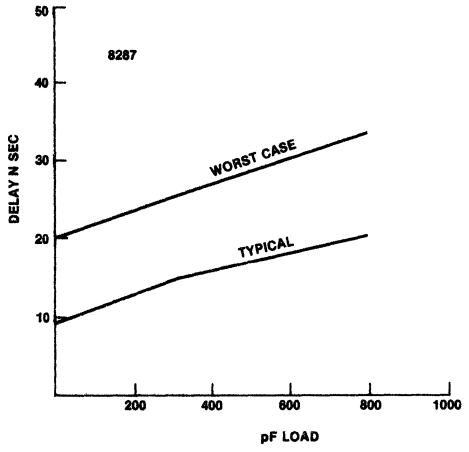
Note: 1. See waveforms and test load circuit on following page.

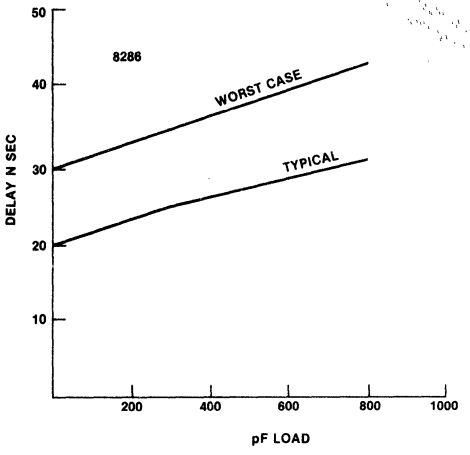
8286/8287 TIMING



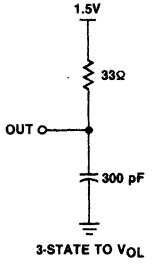
NOTE: 1. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

OUTPUT DELAY VS. CAPACITANCE

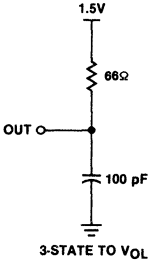




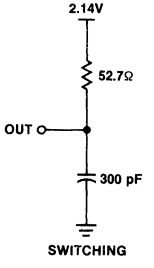
TEST LOAD CIRCUITS



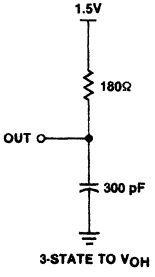
B OUTPUT



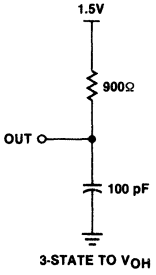
A OUTPUT



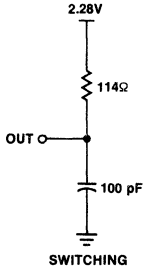
B OUTPUT



B OUTPUT



A OUTPUT



A OUTPUT

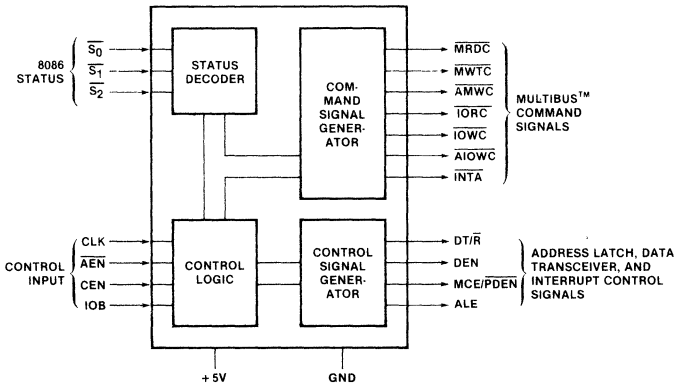
8288
BUS CONTROLLER FOR THE 8086 CPU

- **Bipolar Drive Capability**
- **Provides Advanced Commands**
- **Provides Wide Flexibility in System Configurations**
- **3-State Command Output Drivers**
- **Configurable for Use with an I/O Bus**
- **Facilitates Interface to One or Two Multi-Master Busses**

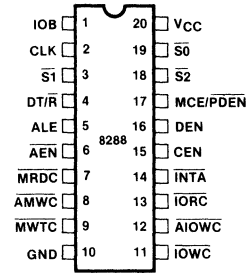
The Intel® 8288 Bus Controller is a 20-pin bipolar component for use with medium-to-large 8086 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.

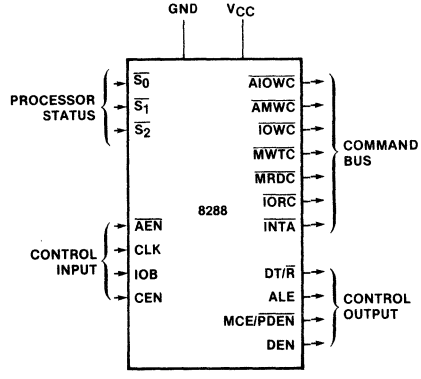
BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTIONAL PIN-OUT



MCS-86

PIN DEFINITIONS

Name	I/O	Function
V_{CC}		+5V supply.
GND		Ground.
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	I	Status Input Pins: These pins are the status input pins from the 8086 processor. The 8288 decodes these inputs to generate command and control signals at the appropriate time. When these pins are not in use (passive) they are all HIGH. (See chart under Command and Control Logic.)
CLK	I	Clock: This is a clock signal from the 8284 clock generator and serves to establish when command and control signals are generated.
ALE	O	Address Latch Enable: This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
DEN	O	Data Enable: This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/$\overline{R}$	O	Data Transmit/Receive: This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Receive (Read).
$\overline{AEN}$	I	Address Enable: $\overline{AEN}$ enables command outputs of the 8288 Bus Controller at least 85 ns after it becomes active (LOW). $\overline{AEN}$ going inactive immediately 3-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the 8288 is in the I/O Bus mode (IOB tied HIGH).
CEN	I	Command Enable: When this signal is LOW all 8288 command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	I	Input/Output Bus Mode: When the IOB is strapped HIGH the 8288 functions in the I/O Bus mode. When it is strapped LOW, the 8288 functions in the System Bus mode. (See sections on I/O Bus and System Bus modes).

Name	I/O	Function
$\overline{AIOWC}$	O	Advanced I/O Write Command: The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IOWC}$	O	I/O Write Command: This command line instructs an I/O device to read the data on the data bus. This signal is active LOW.
$\overline{IORC}$	O	I/O Read Command: This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	O	Advanced Memory Write Command: The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	O	Memory Write Command: This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{MRDC}$	O	Memory Read Command: This command line instructs the memory to drive its data onto the data bus. This signal is active LOW.
$\overline{INTA}$	O	Interrupt Acknowledge: This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/$\overline{PDEN}$	O	This is a dual function pin. MCE (IOB is tied LOW): Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ (IOB is tied HIGH): Peripheral Data Enable enables the data bus transceiver for the I/O bus during I/O instructions. It performs the same function for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.

COMMAND AND CONTROL LOGIC

The command logic decodes the three 8086 CPU status lines ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) to determine what command is to be issued.

This chart shows the meaning of each status "word".

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	8086 State	8288 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$,$\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$,$\overline{AMWC}$
1	1	1	Passive	None

The command is issued in one of two ways dependent on the mode of the 8288 Bus Controller.

I/O Bus Mode — The 8288 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode all I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the 8288 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one 8288 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode — The 8288 is in the System Bus mode if the IOB pin is strapped LOW. In this mode no command is issued until 85 ns after the $\overline{AEN}$ Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the 8086 CPU from entering an unnecessary wait state.

The command outputs are:

$\overline{MRDC}$ — Memory Read Command
$\overline{MWTC}$ — Memory Write Command
$\overline{IORC}$ — I/O Read Command
$\overline{IOWC}$ — I/O Write Command
$\overline{AMWC}$ — Advanced Memory Write Command
$\overline{AIOWC}$ — Advanced I/O Write Command
$\overline{INTA}$ — Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

Control Outputs

The control outputs of the 8288 are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). The DEN signal determines when the external bus should be enabled onto the local bus and the DT/$\overline{R}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the 8288. When the 8288 is in the IOB mode (IOB HIGH) the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the 8288 is in the System Bus mode (IOB LOW). During any interrupt sequence there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe data into the address latches. ALE also serves to strobe the status ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) into a latch within the 8288. For this reason an ALE occurs when entering a halt state.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the 8288. If the CEN pin is high the 8288 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
All Output and Supply Voltages ..... −0.5V to +7V
All Input Voltages ..... −1.0V to +5.5V
Power Dissipation ..... 1.5 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS FOR THE 8288

Conditions: $V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_C	Input Clamp Voltage		−1	V	$I_C = -5$ mA
I_{CC}	Power Supply Current		230	mA	
I_F	Forward Input Current		−0.7	mA	$V_F = 0.45V$
I_R	Reverse Input Current		50	μA	$V_R = V_{CC}$
V_{OL}	Output Low Voltage—Command Outputs Control Outputs		0.5 0.5	V V	$I_{OL} = 32$ mA $I_{OL} = 16$ mA
V_{OH}	Output High Voltage—Command Outputs Control Outputs	2.4 2.4		V V	$I_{OH} = -5$ mA $I_{OH} = -1$ mA
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
I_{OFF}	Output Off Current		100	μA	$V_{OFF} = 0.4$ to $5.25V$

A.C. CHARACTERISTICS FOR THE 8288

Conditions: $V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $70°C$

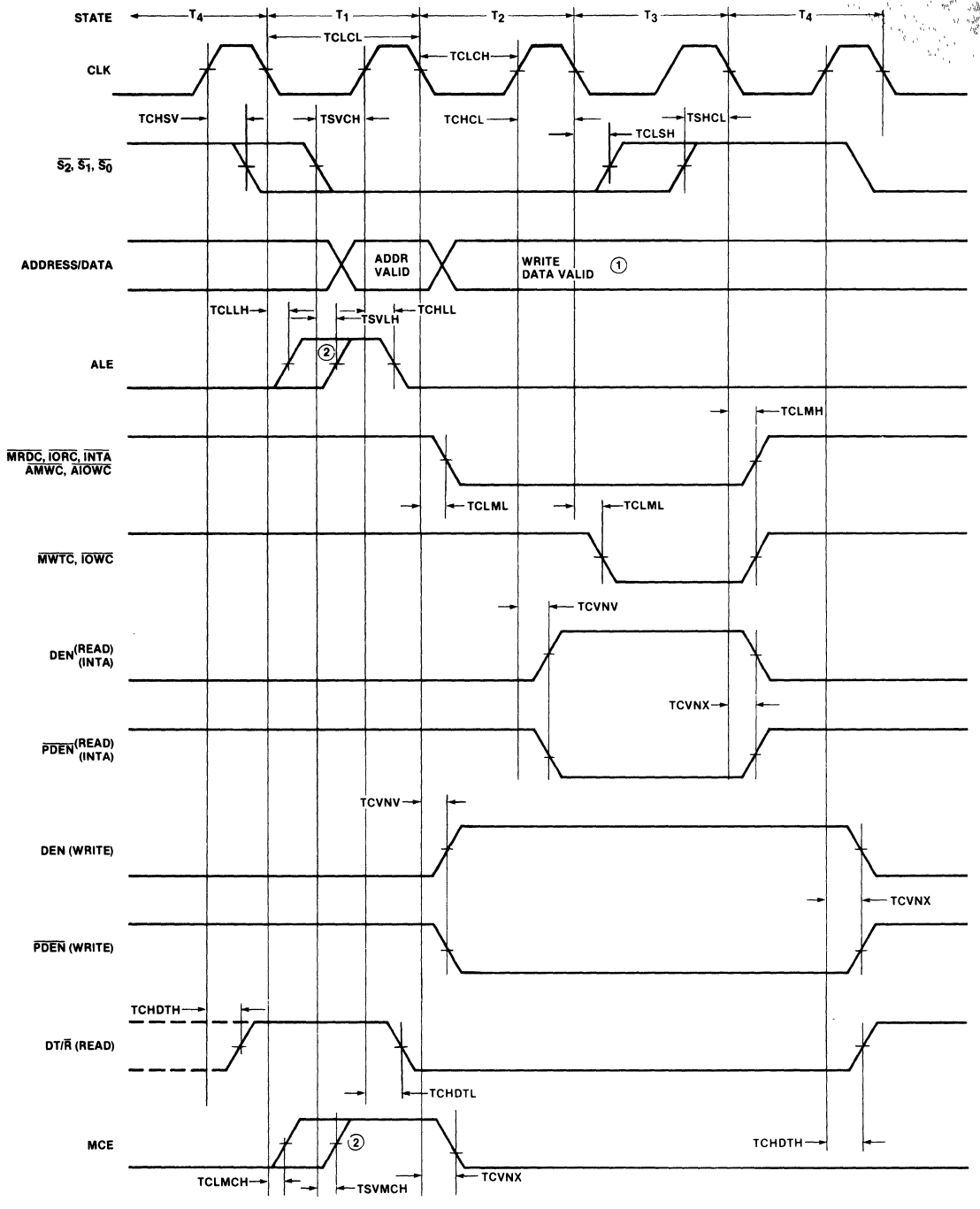
TIMING REQUIREMENTS

Symbol	Parameter	Min	Max	Unit	Loading
TCLCL	CLK Cycle Period	125		ns	
TCLCH	CLK Low Time	66		ns	
TCHCL	CLK High Time	40		ns	
TSVCH	Status Active Setup Time	65		ns	
TCHSV	Status Active Hold Time	10		ns	
TSHCL	Status Inactive Setup Time	55		ns	
TCLSH	Status Inactive Hold Time	10		ns	

TIMING RESPONSES

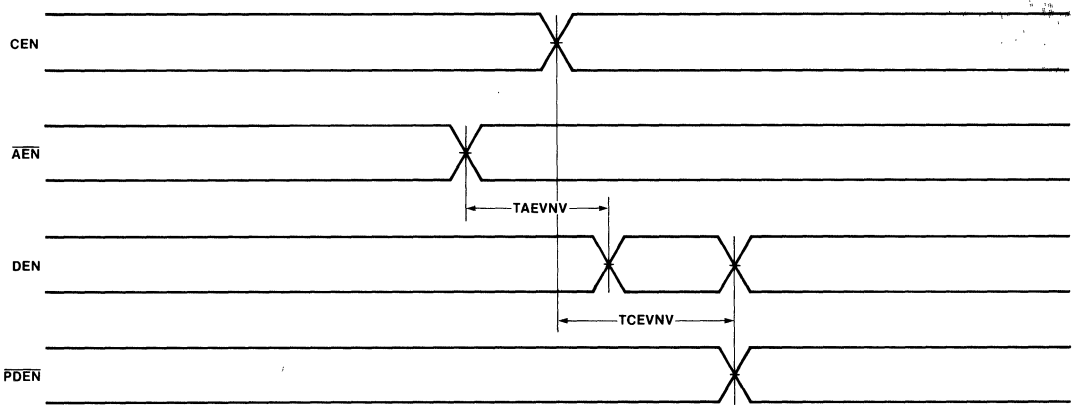
Symbol	Parameter	Min	Max	Unit	Loading
TCVNV	Control Active Delay	5	45	ns	
TCVNX	Control Inactive Delay	10	45	ns	
TCLLH, TCLMCH	ALE MCE Active Delay (from CLK)		15	ns	
TSVLH, TSVMCH	ALE MCE Active Delay (from Status)		15	ns	
TCHLL	ALE Inactive Delay		15	ns	$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: $I_{OL} = 32$ mA, $I_{OH} = -2$ mA, $C_L = 300$ pF
TCLML	Command Active Delay	10	35	ns	
TCLMH	Command Inactive Delay	10	35	ns	
TCHDTL	Direction Control Active Delay		50	ns	
TCHDTH	Direction Control Inactive Delay		30	ns	
TAELCH	Command Enable Time		40	ns	
TAEHCZ	Command Disable Time		40	ns	Other: $I_{OL} = 16$ mA, $I_{OH} = -1$ mA, $C_L = 80$ pF
TAELCV	Enable Delay Time	85	275	ns	
TAEVNV	$\overline{AEN}$ to DEN		20	ns	
TCEVNV	CEN to DEN, PDEN		20	ns	
TCELRH	CEN to Command		TCLML	ns	

8288 TIMING DIAGRAM

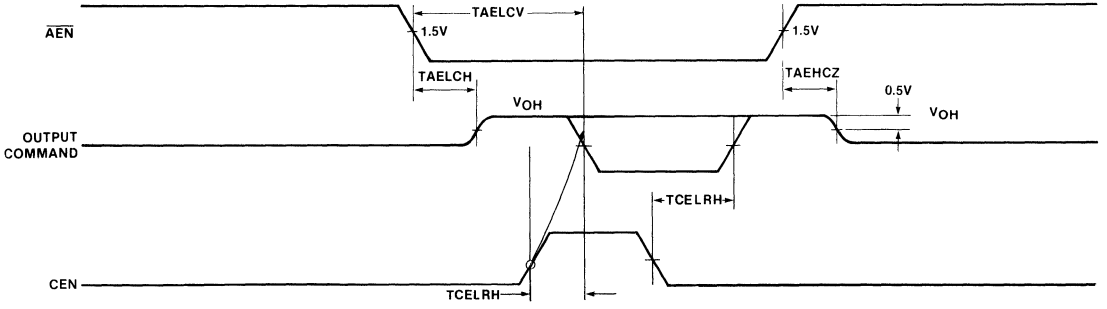


NOTES:
1. ADDRESS/DATA BUS IS SHOWN ONLY FOR REFERENCE PURPOSES.
2. LEADING EDGE OF ALE AND MCE IS DETERMINED BY THE FALLING EDGE OF CLK OR STATUS GOING ACTIVE, WHICHEVER OCCURS LAST
3. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS SPECIFIED OTHERWISE.

DEN, PDEN QUALIFICATION TIMING

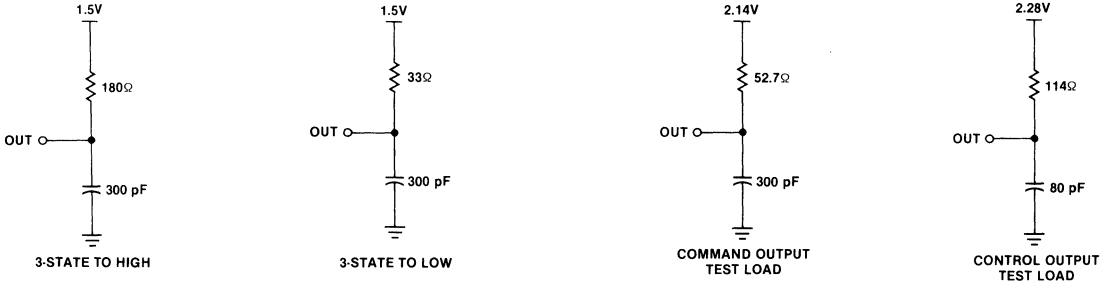


8288 ADDRESS ENABLE (AEN) TIMING (3-STATE ENABLE/DISABLE)

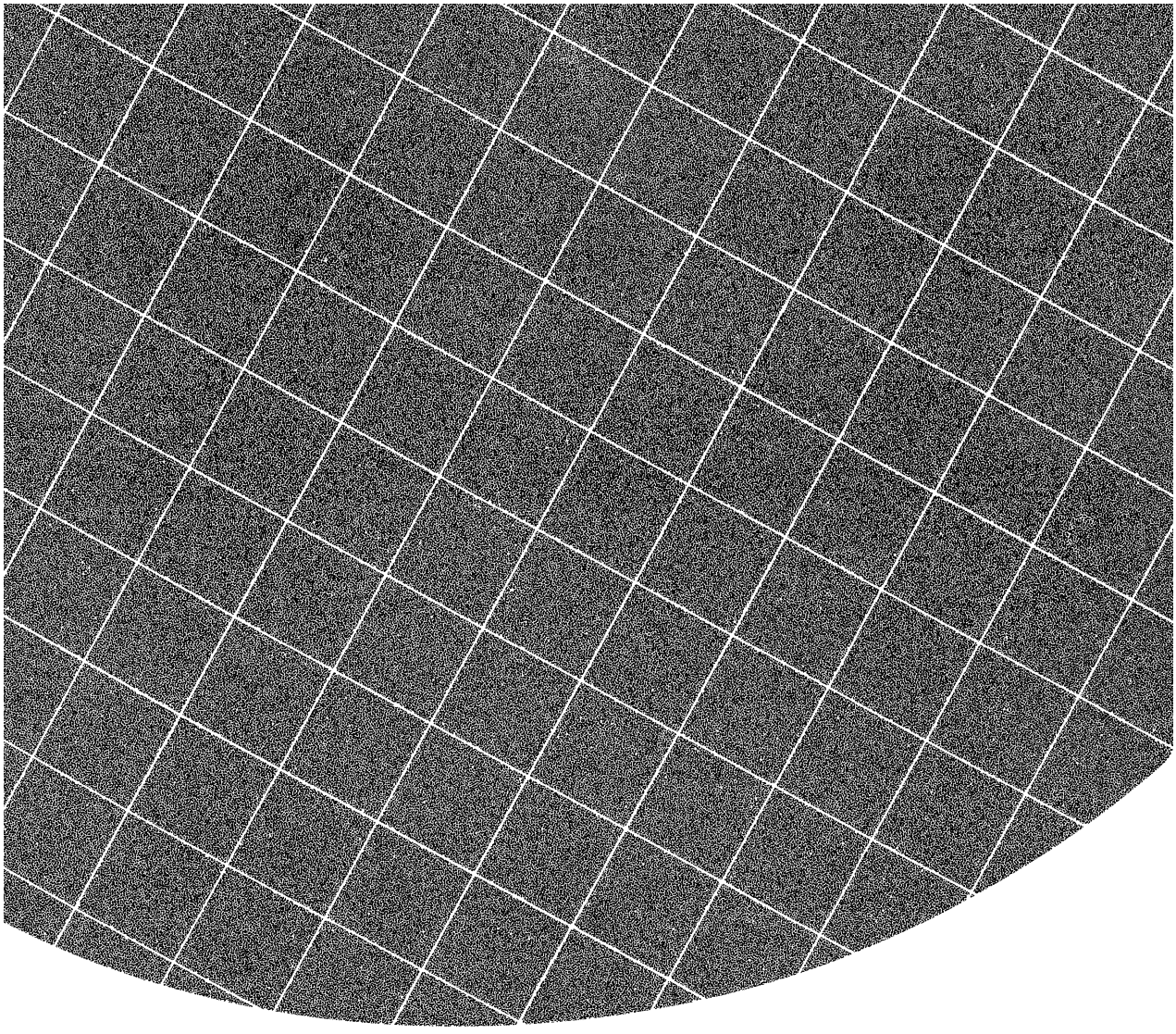


NOTE: CEN MUST BE LOW OR VALID PRIOR TO T2 TO PREVENT THE COMMAND FROM BEING GENERATED.

TEST LOAD CIRCUITS



3-STATE COMMAND OUTPUT TEST LOAD



Microprocessor Peripherals 11

MICROPROCESSOR PERIPHERALS

INTRODUCTION

Intel peripherals greatly enhance the 8080, the 8085, and many other microcomputers. These peripherals can significantly reduce development time, operating software, package count, board space, and parts costs while improving performance and increasing throughput in microcomputer systems. This section contains the most up-to-date data about Intel peripherals now available.

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8041A/8741A
UNIVERSAL PERIPHERAL INTERFACE
8-BIT MICROCOMPUTER

- **8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package**
- **One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface**
- **DMA, Interrupt, or Polled Operation Supported**
- **1024 x 8 ROM/EPROM, 64 x 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins**
- **Fully Compatible with MCS-48™, MCS-80™, MCS-85™, and MCS-86™ Microprocessor Families**
- **Expandable I/O**
- **ROM Power-Down Capability**
- **Single 5V Supply**

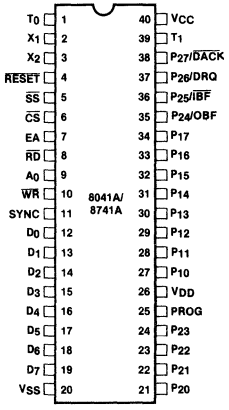
The Intel® 8041A/8741A is a general purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in MCS-48™, MCS-80™, MCS-85™, MCS-86™, and other 8-bit systems.

The UPI-41A™ has 1K words of program memory and 64 words of data memory on-chip. To allow full user flexibility the program memory is available as ROM in the 8041A version or as UV-erasable EPROM in the 8741A version. The 8741A and the 8041A are fully pin compatible for easy transition from prototype to production level designs.

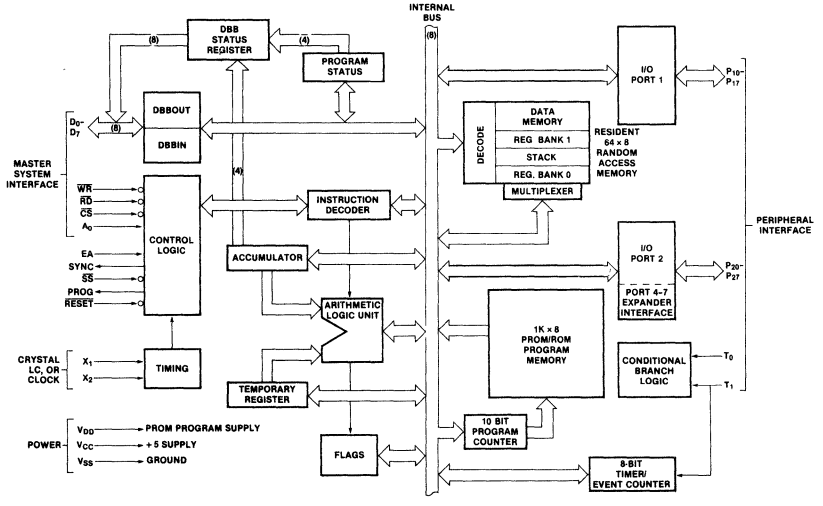
The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, low power standby mode (in the 8041A), single-step mode for debug (in the 8741A), and dual working register banks.

Because it's a complete microcomputer, the UPI provides more flexibility for the designer than conventional LSI interface devices. It is designed to be an efficient controller as well as an arithmetic processor. Applications include keyboard scanning, printer control, display multiplexing and similar functions which involve interfacing peripheral devices to microprocessor systems.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

Signal	Description
D_0-D_7	Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI-41A to an 8-bit master system data bus.
P_{10}-P_{17}	8-bit, PORT 1 quasi-bidirectional I/O lines.
P_{20}-P_{27}	8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P_{20}-P_{23}) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4-7 access. The upper 4 bits (P_{24}-P_{27}) can be programmed to provide Interrupt Request and DMA Handshake capability. Software control can configure P_{24} as OBF (Output Buffer Full), P_{25} as $\overline{IBF}$ (Input Buffer Full), P_{26} as DRQ (DMA Request), and P_{27} as $\overline{DACK}$ (DMA ACKnowledge).
$\overline{WR}$	I/O write input which enables the master CPU to write data and command words to the UPI-41A INPUT DATA BUS BUFFER.
$\overline{RD}$	I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
$\overline{CS}$	Chip select input used to select one UPI-41A out of several connected to a common data bus.
A_0	Address input used by the master processor to indicate whether byte transfer is data or command.
T_0, T_1	Input pins which can be directly tested using conditional branch instructions.
	T_1 also functions as the event timer input (under software control). T_0 is used during PROM programming and verification in the 8741A.
X_1, X_2	Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
SYNC	Output signal which occurs once per UPI-41A instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
EA	External access input which allows emulation, testing and PROM/ROM verification.
PROG	Multifunction pin used as the program pulse input during PROM programming.
	During I/O expander access the PROG pin acts as an address/data strobe to the 8243.
$\overline{RESET}$	Input used to reset status flip-flops and to set the program counter to zero.
	$\overline{RESET}$ is also used during PROM programming and verification.
$\overline{SS}$	Single step input used in the 8741A in conjunction with the SYNC output to step the program through each instruction.
V_{CC}	+5V power supply pin.
V_{DD}	+5V during normal operation. Programming supply pin during PROM programming. Low power standby pin in ROM version.
V_{SS}	Circuit ground potential.

MPU PERIPHERALS

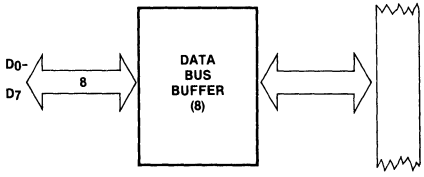
UPI INSTRUCTION SET

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR			
ADD A,Rr	Add register to A	1	1
ADD A,@Rr	Add data memory to A	1	1
ADD A,#data	Add immediate to A	2	2
ADDC A,Rr	Add immed. to A with carry	1	1
ADDC A,@Rr	Add immed. to A with carry	1	1
ADDC A,#data	Add immed. to A with carry	2	2
ANL A,Rr	AND register to A	1	1
ANL A,@Rr	AND data memory to A	1	1
ANL A,#data	AND immediate to A	2	2
ORL A,Rr	OR register to A	1	1
ORL A,@Rr	OR data memory to A	1	1
ORL A,#data	OR immediate to A	2	2
XRL A,Rr	Exclusive OR register to A	1	1
XRL A,@Rr	Exclusive OR data memory to A	1	1
XRL A,#data	Exclusive OR immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal Adjust A	1	1
SWAP A	Swap digits of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
INPUT/OUTPUT			
IN A,Pp	Input port to A	1	2
OUTL Pp,A	Output A to port	1	2
ANL Pp,#data	AND immediate to port	2	2
ORL Pp,#data	OR immediate to port	2	2
IN A,DBB	Input DBB to A, clear IBF	1	1
OUT DBB,A	Output A to DBB, set OBF	1	1
MOVD A,Pp	Input Expander port to A	1	2
MOVD Pp,A	Output A to Expander port	1	2
ANLD Pp,A	AND A to Expander port	1	2
ORLD Pp,A	OR A to Expander port	1	2
DATA MOVES			
MOV A,Rr	Move register to A	1	1
MOV A,@Rr	Move data memory to A	1	1
MOV A,#data	Move immediate to A	2	2
MOV Rr,A	Move A to register	1	1
MOV @Rr,A	Move A to data memory	1	1
MOV Rr,#data	Move immediate to register	2	2
MOV @Rr,#data	Move immediate to data memory	2	2
MOV A,PSW	Move PSW to A	1	1
MOV PSW,A	Move A to PSW	1	1
XCH A,Rr	Exchange A and register	1	1
XCH A,@Rr	Exchange A and data memory	1	1
XCHD A,@Rr	Exchange digit of A and register	1	1
MOVP A,@A	Move to A from current page	1	2
MOVP3, A,@A	Move to A from page 3	1	2
TIMER/COUNTER			
MOV A,T	Read Timer/Counter	1	1
MOV T,A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	Start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/Counter Interrupt	1	1
DIS TCNTI	Disable Timer/Counter Interrupt	1	1

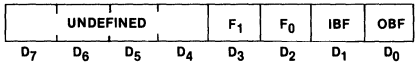
FEATURES AND ENHANCEMENTS

UPI-41

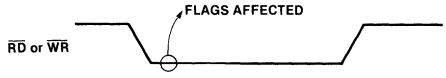
1. Single Data Bus Buffer



2. 4 Bits of Status



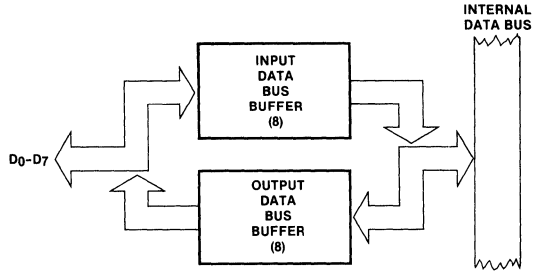
3. $\overline{RD}$ and $\overline{WR}$ are level triggered. IBF, OBF, F_1 and INT change internally when $\overline{RD}$ or $\overline{WR}$ are low.



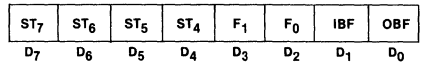
4. P_{24} and P_{25} are port pins only.

UPI-41A

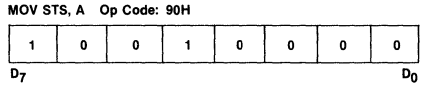
1. Two Data Bus Buffers, one for input and one for output. This allows a much cleaner Master/Slave protocol.



2. 8 Bits of Status



ST_4-ST_7 are user definable status bits. These bits are defined by the "MOV STS, A" single byte, single cycle instruction. Bits 4-7 of the accumulator are moved to bits 4-7 of the status register. Bits 0-3 of the status register are not affected.



3. $\overline{RD}$ and $\overline{WR}$ are edge triggered. IBF, OBF, F_1 and INT change internally after the trailing edge of $\overline{RD}$ or $\overline{WR}$.

4. P_{24} and P_{25} are port pins or Buffer Flag pins which can be used to interrupt a master processor. These pins default to port pins on Reset.

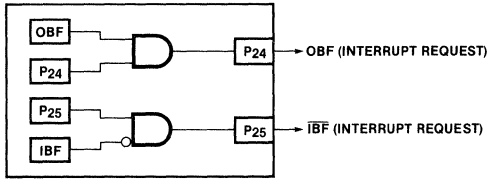
   If the "EN FLAGS" instruction has been executed, P_{24} becomes the OBF (Output Buffer Full) pin. A "1" written to P_{24} enables the OBF pin (the pin outputs the OBF Status Bit). A "0" written to P_{24} disables the OBF pin (the pin remains low). This pin can be used to indicate that valid data is available from the UPI-41A (in Output Data Bus Buffer).

UPI-41

5. P_{26} and P_{27} are port pins only.

UPI-41A

If "EN FLAGS" has been executed, P_{25} becomes the $\overline{IBF}$ (Input Buffer Full) pin. A "1" written to P_{25} enables the $\overline{IBF}$ pin (the pin outputs the inverse of the $\overline{IBF}$ Status Bit). A "0" written to P_{25} disables the $\overline{IBF}$ pin (the pin remains low). This pin can be used to indicate that the UPI-41 is ready for data.



DATA BUS BUFFER INTERRUPT CAPABILITY

EN FLAGS Op Code: 0F5H

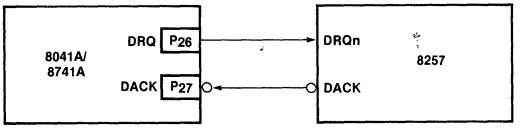
1	1	1	1	0	1	0	1

D_7 D_0

5. P_{26} and P_{27} are port pins or DMA handshake pins for use with a DMA controller. These pins default to port pins on Reset.

   If the "EN DMA" instruction has been executed, P_{26} becomes the DRQ (DMA ReQuest) pin. A "1" written to P_{26} causes a DMA request (DRQ is activated). DRQ is deactivated by DACK·RD, DACK·WR, or execution of the "EN DMA" instruction.

   If "EN DMA" has been executed, P_{27} becomes the $\overline{DACK}$ (DMA ACKnowledge) pin. This pin acts as a chip select input for the Data Bus Buffer registers during DMA transfers.



DMA HANDSHAKE CAPABILITY

EN DMA Op Code: 0E5H

1	1	1	0	0	1	0	1

D_1 D_0

MPU PERIPHERALS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . – 65°C to + 150°C
Voltage on Any Pin With Respect to Ground . . . . . 0.5V to + 7V
Power Dissipation . . . . . 1.5 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to 70°C, $V_{SS} = 0V$, 8041A: $V_{CC} = +5V \pm 10\%$, 8741A: $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage (All Except X_1, X_2)	-0.5	0.8	V	
V_{IH1}	Input High Voltage (All Except X_1, X_2, $\overline{RESET}$)	2.2	V_{CC}		
V_{IH2}	Input High Voltage (X_1, X_2, $\overline{RESET}$)	3.0	V_{CC}	V	
V_{OL1}	Output Low Voltage (D_2-D_7, Sync)		0.45	V	$I_{OL} = 2.0$ mA
V_{OL2}	Output Low Voltage (All Other Outputs Except Prog)		0.45	V	$I_{OL} = 1.6$ mA
V_{OL3}	Output Low Voltage (Prog)		0.45	V	$I_{OL} = 1.0$ mA
V_{OH1}	Output High Voltage (D_0-D_7)	2.4		V	$I_{OH} = -400\ \mu A$
V_{OH2}	Output High Voltage (All Other Outputs)	2.4		V	$I_{OH} = -50\ \mu A$
I_{IL}	Input Leakage Current (T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A_0, EA)		± 10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{OZ}	Output Leakage Current (D_0-D_7, High Z State)		± 10	μA	$V_{SS} + 0.45 \leqslant V_{IN} \leqslant V_{CC}$
I_{LI1}	Low Input Load Current ($P_{10}P_{17}$, $P_{20}P_{27}$		0.5	mA	$V_{IL} = 0.8V$
I_{LI2}	Low Input Load Current ($\overline{RESET}$, SS)		0.2	mA	$V_{IL} = 0.8V$
I_{DD}	V_{DD} Supply Current		1.5	mA	
$I_{CC} + I_{DD}$	Total Supply Current		125	mA	

A.C. CHARACTERISTICS

$T_A = 0°C$ to 70°C, $V_{SS} = 0V$, 8041A: $V_{CC} = V_{DD} = +5V \pm 10\%$, 8741A: $V_{CC} = V_{DD} = +5V \pm 5\%$

DBB READ

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AR}	$\overline{CS}$, A_0 Setup to $\overline{RD}\downarrow$	0		ns	
t_{RA}	$\overline{CS}$, A_0 Hold After $\overline{RD}\uparrow$	0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	250		ns	$t_{CY} = 2.5\ \mu s$
t_{AD}	$\overline{CS}$, A_0 to Data Out Delay		225	ns	$C_L = 150$ pF
t_{RD}	$\overline{RD}\downarrow$ to Data Out Delay		225	ns	$C_L = 150$ pF
t_{RDF}	$\overline{RD}\uparrow$ to Data Float Delay		100	ns	
t_{RV}	Recovery Time Between Reads And/Or Write	300		ns	
t_{CY}	Cycle Time	2.5	15	μs	

DBB WRITE

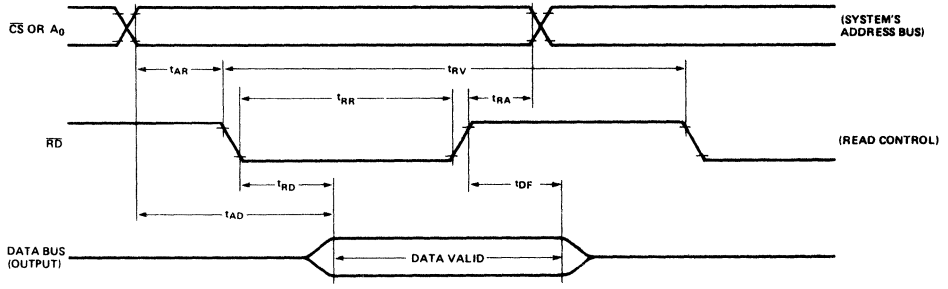
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	CS, A_0 Setup to WR↓	0		ns	
t_{WA}	CS, A_0 Hold After WR↑	0		ns	
t_{WW}	WR Pulse Width	250		ns	
t_{DW}	Data Setup to WR↑	150		ns	
t_{WD}	Data Hold Aftert WR↑	0		ns	

A.C. TEST CONDITIONS

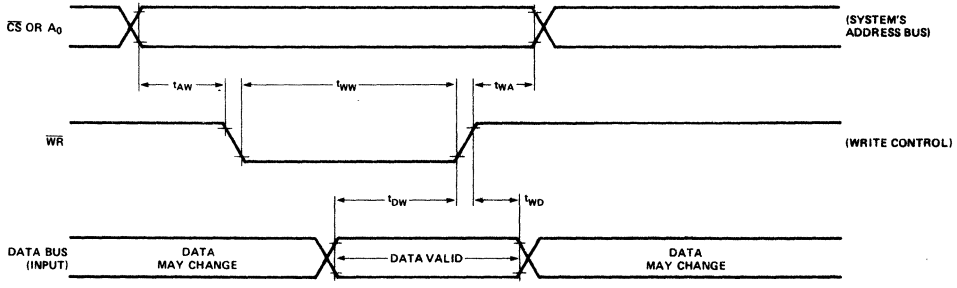
D_7-D_0 Outputs R_L = 2.2k to V_{SS}
4.3k to V_{CC}
$C_L \leq$ 100 pF

WAVEFORMS

1. READ OPERATION—DATA BUS BUFFER REGISTER.



2. WRITE OPERATION—DATA BUS BUFFER REGISTER.



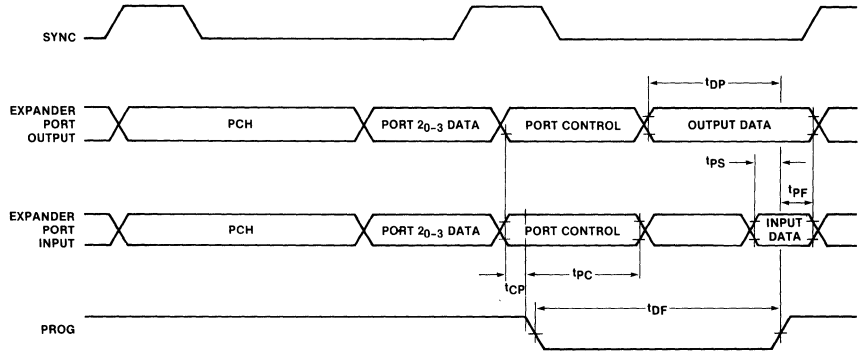
MPU PERIPHERALS

A.C. CHARACTERISTICS—PORT 2

$T_A = 0°C$ to $70°C$, 8041A: $V_{CC} = +5V \pm 10\%$, 8741A: $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CP}	Port Control Setup Before Falling Edge of $\overline{PROG}$	110		ns	
t_{PC}	Port Control Hold After Falling Edge of $\overline{PROG}$	140		ns	
t_{DP}	Output Data Setup Time	220		ns	
t_{PF}	Input Data Hold Time	110		ns	
t_{PP}	$\overline{PROG}$ Pulse Width	1400		ns	
t_{PS}	Input Data Setup Time	700		ns	

WAVEFORMS—PORT 2

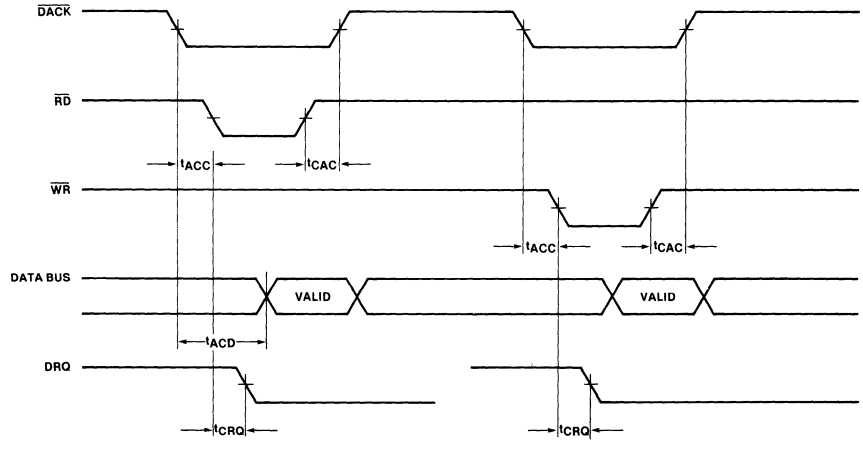


A.C. CHARACTERISTICS—DMA

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{ACC}	DAC to $\overline{WR}$ or $\overline{RD}$	0		ns	
t_{CAC}	$\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$	0		ns	
t_{ACD}	$\overline{DACK}$ to Data Valid		225	ns	$C_L = 150$ pF
t_{CRQ}	$\overline{RD}$ or $\overline{WR}$ to DRQ Cleared		200	ns	

WAVEFORMS—DMA



Mnemonic	Description	Bytes	Cycles
CONTROL			
EN DMA	Enable DMA Handshake Lines	1	1
EN I	Enable IBF Interrupt	1	1
DIS I	Disable IBF Interrupt	1	1
EN FLAGS	Enable Master Interrupts	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
NOP	No Operation	1	1
REGISTERS			
INC Rr	Increment register	1	1
INC @Rr	Increment data memory	1	1
DEC Rr	Decrement register	1	1
SUBROUTINE			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2
FLAGS			
CLR C	Clear Carry	1	1
CPL C	Complement Carry	1	1
CLR F0	Clear Flag 0	1	1
CPL F0	Complement Flag 0	1	1
CLR F1	Clear F1 Flag	1	1
CPL F1	Complement F1 Flag	1	1
MOV STS, A	A_4-A_7 to Bits 4-7 of Status	1	1
BRANCH			
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R,addr	Decrement register and skip	2	2
JC addr	Jump on Carry = 1	2	2
JNC addr	Jump on Carry = 0	2	2
JZ addr	Jump on A Zero	2	2
JNZ addr	Jump on A not Zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 Flag = 1	2	2
JF1 addr	Jump on F1 Flag = 1	2	2
JTF addr	Jump on Timer Flag = 1, Clear Flag	2	2
JNIBF addr	Jump on IBF Flag = 0	2	2
JOBF addr	Jump on OBF Flag = 1	2	2
JBb addr	Jump on Accumulator Bit	2	2

APPLICATIONS

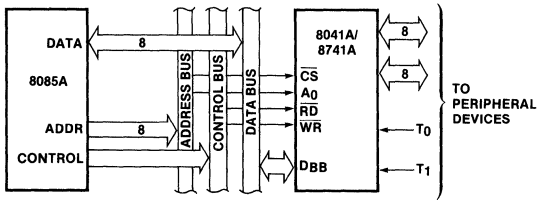


Figure 1. 8085A-8041A Interface

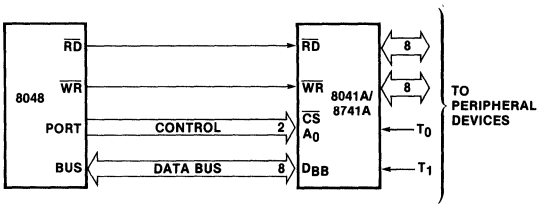


Figure 2. 8048-8041A Interface

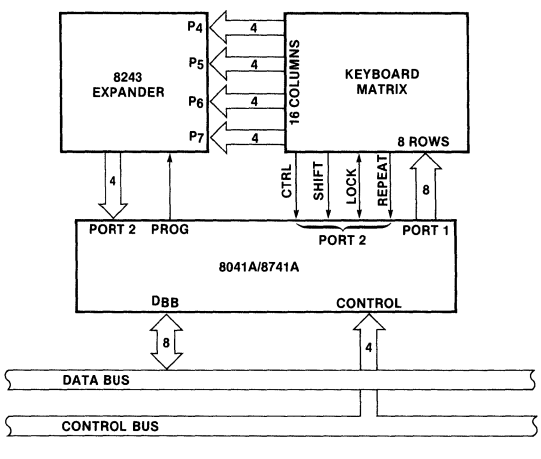


Figure 3. 8041A-8243 Keyboad Scanner

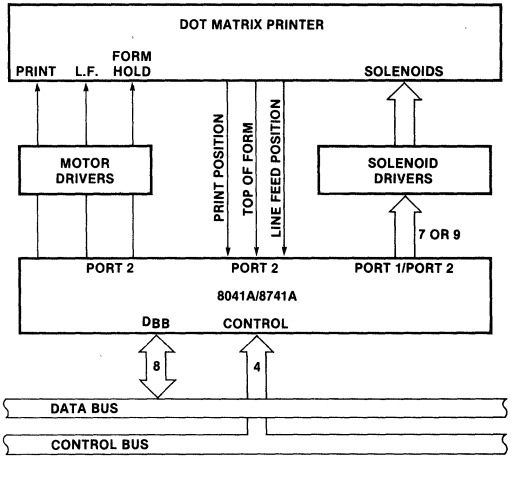


Figure 4. 8041A Matrix Printer Interface

PROGRAMMING, VERIFYING, AND ERASING THE 8741A EPROM

Programming/Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock input (1 to 6 MHz)
RESET	Initialization and address latching
TEST 0	Selection of program or verify mode
EA	Activation of program/verify modes
BUS	Address and data input data output during verify
P20-1	Address input
V_{DD}	Programming power supply
PROG	Program pulse input

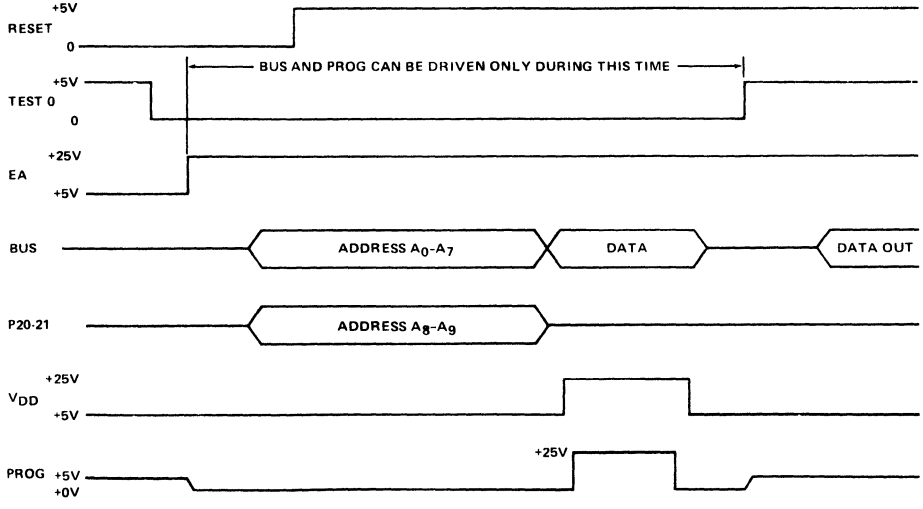
The program/verify sequence is:

1. V_{DD} = 5V, clock applied or internal oscillator operating, RESET = 0V, TEST 0 = 5V, EA = 5V, BUS and PROG floating.
2. Insert 8741A in programming socket.
3. TEST 0 = 0V (select program mode).
4. EA = 25V (activate program mode).
5. Address applied to BUS and P20-1.
6. RESET = 5V (latch address).
7. Data applied to BUS.
8. V_D = 25V (programming power).
9. PROG = 0V followed by one 50 ms pulse to 25V.
10. V_{DD} = 5V.
11. TEST 0 = 5V (verify mode).
12. Read and verify data on BUS.
13. TEST 0 = 0V.
14. RESET = 0V and repeat from step 5.
15. Programmer should be at conditions of step 1 when 8741A is removed from socket.

Programming Options

The 8741A EPROM can be programmed by either of two Intel products:

1. PROMPT-48 Microcomputer Design Aid.
2. Universal PROM Programmer (UPP-101 or UPP-102) Peripheral of the Intellec® Development System with a UPP-848 Personality Card.



WARNING: An attempt to program a missocketed 8741A will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC output. The lack of this clock may be used to disable the programmer.

Figure 5. Programming/Verification Sequence

8741A Erasure Characteristics

The erasure characteristics of the 8741A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8741A in approximately 3 years while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 8741A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8741A window to prevent unintentional erasure.

The recommended erasure procedure for the 8741 is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 w-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The 8741A should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

A.C. TIMING SPECIFICATION FOR PROGRAMMING

T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{DD} = 25V ±1V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Setup Time to $\overline{\text{RESET}}$ ↑	4tcy			
t_{WA}	Address Hold Time After $\overline{\text{RESET}}$ ↑	4tcy			
t_{DW}	Data in Setup Time to PROG ↑	4tcy			
t_{WD}	Data in Hold Time After PROG ↓	4tcy			
t_{PH}	$\overline{\text{RESET}}$ Hold Time to Verify	4tcy			
t_{VDDW}	V_{DD}	4tcy			
t_{VDDH}	V_{DD} Hold Time After PROG ↓	0			
t_{PW}	Program Pulse Width	50	60	MS	
t_{TW}	Test 0 Setup Time for Program Mode	4tcy			
t_{WT}	Test 0 Hold Time After Program Mode	4tcy			
t_{DO}	Test 0 to Data Out Delay		4tcy		
t_{WW}	$\overline{\text{RESET}}$ Pulse Width to Latch Address	4tcy			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	5.0		μs	
t_{RE}	$\overline{\text{RESET}}$ Setup Time Before EA ↑	4tcy			

Note: If TEST 0 is high, t_{DO} can be triggered by $\overline{\text{RESET}}$ 1.

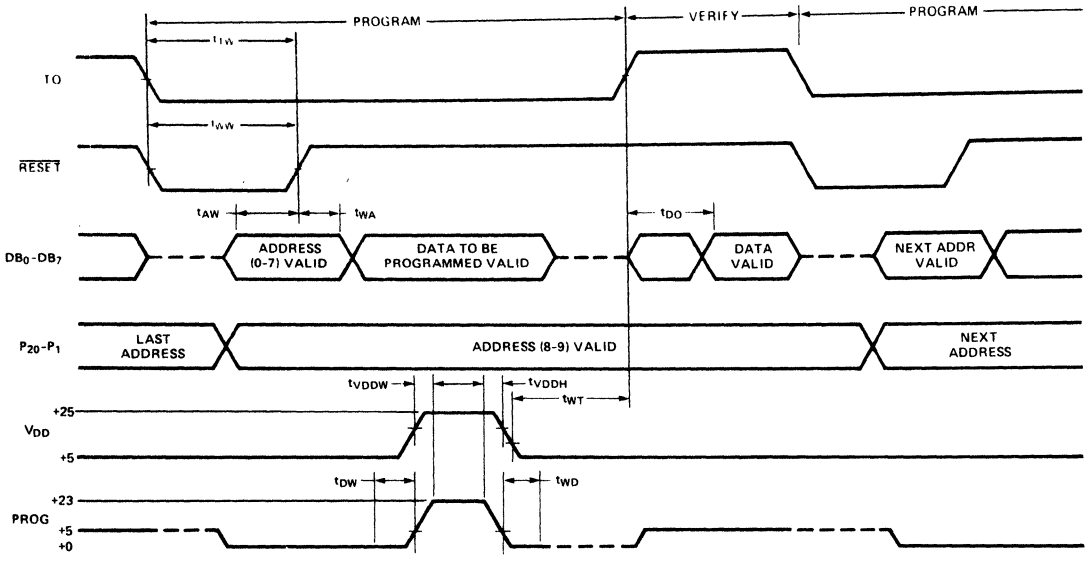
D.C. SPECIFICATION FOR PROGRAMMING

T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{DD} = 25V ±1V

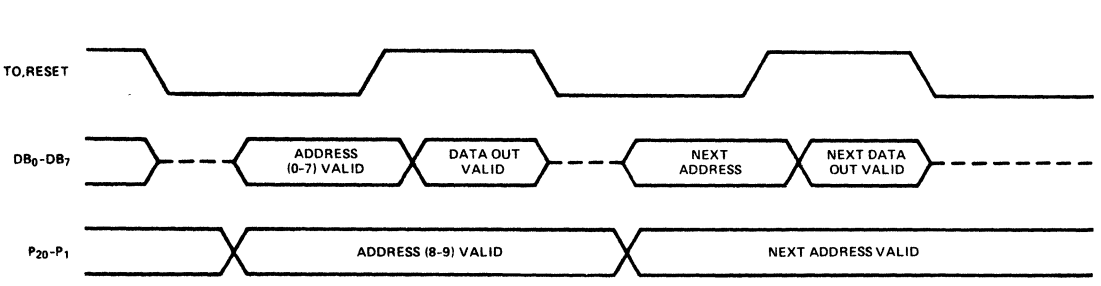
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DOH}	V_{DD} Program Voltage High Level	24.0	26.0	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	21.5	24.5	V	
V_{PL}	PROG Voltage Low Level		0.2	V	
V_{EAH}	EA Program or Verify Voltage High Level	21.5	24.5	V	
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		16.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

WAVEFORMS

Combination Program/Verify Mode (EPROMs Only)



Verify Mode (ROM/EPROM)

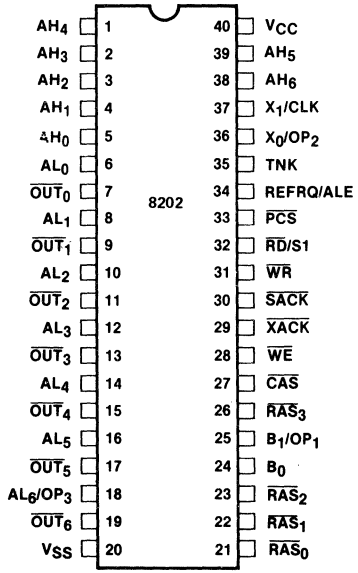


8202
DYNAMIC RAM CONTROLLER

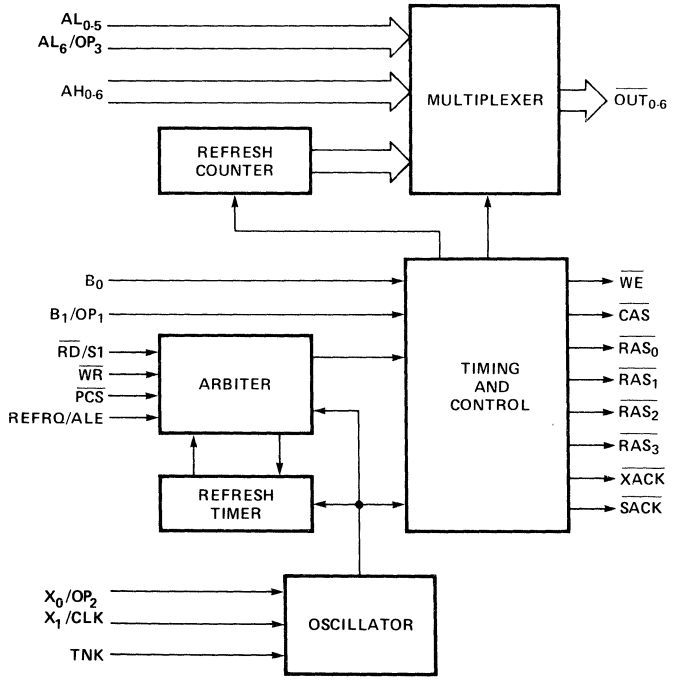
- **Provides All Signals Necessary to Control 2104A, 2117, or 2118 Dynamic Memories**
- **Directly Addresses and Drives Up to 128K Bytes Without External Drivers**
- **Provides Address Multiplexing and Strobes**
- **Provides a Refresh Timer and a Refresh Counter**
- **Refresh Cycles May be Internally or Externally Requested**
- **Provides Transparent Refresh Capability**
- **Fully Compatible with Intel® 8080A, 8085A and 8086 Microprocessors**
- **Decodes 8085A Status for Advanced Read Capability**
- **Provides System Acknowledge and Transfer Acknowledge Signals**
- **Internal or External Clock Capability**

The 8202 is a Dynamic RAM System Controller designed to provide all signals necessary to use 2104A, 2117, or 2118 Dynamic RAMs in microcomputer systems. The 8202 provides multiplexed addresses and address strobes, as well as refresh/access arbitration. Refresh cycles can be started internally or externally.

PIN CONFIGURATION



8202 BLOCK DIAGRAM



MPU PERIPHERALS

PIN DESCRIPTIONS

Pin Name	#	I/O	Pin Description
AL_0	6	I	Low-Order Address. These Address
AL_1	8	I	inputs are used to generate the Row
AL_2	10	I	Address for the Multiplexer. If the
AL_3	12	I	AL_6/OP_3 input is pulled to +12V
AL_4	14	I	through a 5KΩ resistor, the 8202
AL_5	16	I	configures itself for 4K RAMs. If
AL_6/OP_3	18	I	AL_6/OP_3 is driven with TTL levels, the 8202 configures itself for 16K RAMs.
AH_0	5	I	High-Order Address. These Ad-
AH_1	4	I	dress inputs are used to generate
AH_2	3	I	the Column Address for the Multi-
AH_3	2	I	plexer. If the 8202 is configured for
AH_4	1	I	4K RAMs, AH_6 can be used as an
AH_5	39	I	active high Chip select for the mem-
AH_6	38	I	ory controlled by 8202. For 16K RAM operation, AH_6 becomes the most significant column address bit.
$\overline{OUT_0}$	7	O	Output of the Multiplexer. These
$\overline{OUT_1}$	9	O	outputs are designed to drive the ad-
$\overline{OUT_2}$	11	O	dresses of the Dynamic RAM array.
$\overline{OUT_3}$	13	O	For 4K RAM operation, $\overline{OUT_6}$ is de-
$\overline{OUT_4}$	15	O	signed to drive the 2104A $\overline{CS}$ input.
$\overline{OUT_5}$	17	O	(Note that the $\overline{OUT_{0-6}}$ pins do not
$\overline{OUT_6}$	19	O	require inverters or drivers for proper operation.
$\overline{WE}$	28	O	Write Enable. This output is designed to drive the Write Enable inputs of the Dynamic RAM array.
$\overline{CAS}$	27	O	Column Address Strobe. This output is used to latch the Column Address into the Dynamic RAM array.
$\overline{RAS_0}$	21	O	Row Address Strobe. These outputs
$\overline{RAS_1}$	22	O	are used to latch the Row Address
$\overline{RAS_2}$	23	O	into the bank of dynamic RAMs,
$\overline{RAS_3}$	26	O	selected by the 8202 Bank Address pins (B_0, B_1/OP_1)
B_0	24	I	Bank Address. These inputs are
B_1/OP_1	25	I	used to select one of four banks of dynamic RAM via the $\overline{RAS_{0-3}}$ outputs. If the B_1/OP_1 input is pulled to +12V through a 5KΩ resistor, the 8202 configures itself to the Advanced Read mode. This mode changes the function of the 8202 $\overline{RD}/S_1$ and REFRQ/ALE inputs and disables the $\overline{RAS_0}$ and $\overline{RAS_1}$ outputs.

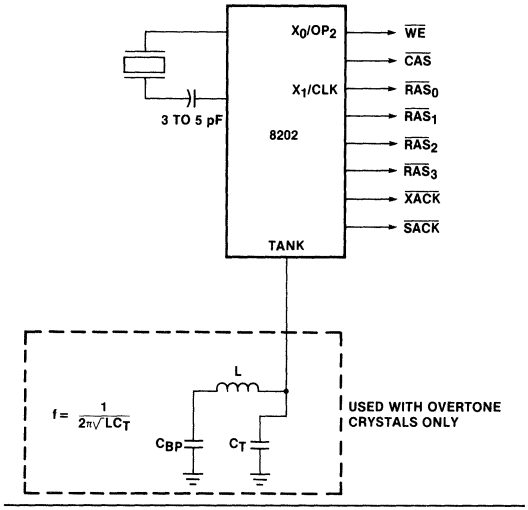
Pin Name	#	I/O	Pin Description
$\overline{RD}/S_1$	32	I	Read/S_1 input. This input is used to request a read cycle. In normal operation, a low on this input informs the arbiter that a read cycle is requested. In the Advanced Read Mode, this input is designed to accept the S1 status signal from the 8085A (fully decoded for a read). The trailing edge of ALE informs the arbiter that a read cycle is requested by latching S_1.
$\overline{WR}$	31	I	Write Input. This input is used to request a write cycle. A low on this input informs the arbiter that a write cycle is desired.
$\overline{PCS}$	33	I	Protected Chip Select. A low on this input enables the $\overline{WR}$ and $\overline{RD}/S_1$ inputs. $\overline{PCS}$ is protected against terminating a cycle in progress.
REFRQ/ ALE	34	I	Refresh Request/Address Latch Enable. During normal operation, a high on this input indicates to the arbiter that a refresh cycle is being requested. In the Advanced Read Mode, this input is used to latch the state of the 8085 S1 signal into the $\overline{RD}/S_1$ input. If S_1 is high at this time, a Read Cycle is requested. In this mode, transparent refresh is not possible.
$\overline{XACK}$	29	O	Transfer acknowledge. This output is a strobe indicating valid data during a read cycle or data written during a write cycle. $\overline{XACK}$ can be used to latch valid data from the RAM array.
$\overline{SACK}$	30	O	System Acknowledge. This output indicates the beginning of a memory access cycle. It can be used as an advanced transfer acknowledge to eliminate wait states. (Note: If a memory access request is made during a refresh cycle, $\overline{SACK}$ is delayed until $\overline{XACK}$ in the memory access cycle).
X_0/OP_2	36	I	Crystal Inputs. These inputs are de-
X_1/CLK	37	I	signed for a quartz crystal to control the frequency of the oscillator. If X_0/OP_2 is pulled to +12V through a 1KΩ resistor, X_1/CLK becomes a TTL input for an external clock.
TNK	35		Tank. This pin is used for a tank circuit connection.
V_{CC}	40		+5V ± 10%
V_{SS}	20		Ground.

BASIC FUNCTIONAL DESCRIPTION

The 8202 consists of six basic blocks; the oscillator, the arbiter, the refresh timer, the refresh counter, the multiplexer, and the timing and control block.

Oscillator

The oscillator provides the basic timing for all 8202 operations. The oscillator circuit is designed primarily for use with an external series resonant fundamental mode crystal. Overtone crystals may be used with the tank circuit shown in Figure 1. A small capacitor (3-5) pF should be placed in series with any crystal to block D.C. stress and assure oscillation at the proper frequency.



The tank input to the oscillator allows the use of overtone mode crystals. The tank circuit shunts the crystal's fundamental and high overtone frequencies and allows the third harmonic to oscillate. The external LC network is connected to the TANK input and is AC coupled to ground.

If the X_0/OP_2 pin is pulled to +12V, through a 1KΩ resistor, the 8202 can be driven by a TTL clock on the X_1/CLK input. No tank circuit is required in this mode.

Arbiter

The 8202 provides 3 different operational cycles:

1. Read Cycle
2. Write Cycle
3. Refresh Cycle

The read and write cycles are initiated by external requests ($\overline{RD}/S_1$ and $\overline{PCS}$ or $\overline{WR}$ and $\overline{PCS}$). A refresh cycle may be initiated by the internal refresh timer, or by an external request (REFRQ/ALE). The arbiter resolves conflicts between cycle requests and cycles in execution.

If the B_1/OP_1 input is pulled to +12V through a 5KΩ resistor (Advanced Read mode), $\overline{RD}/S_1$ becomes an input for the S_1 status signal of the 8085A (fully decoded for read). REFRQ/ALE becomes an input for the ALE signal of the 8085 (used to latch S_1. If S_1 is "high" at the falling edge of ALE, a read cycle will be requested. Transparent refresh is not possible in this mode.

Refresh Timer

The refresh timer is a simple timer that indicates to the arbiter that it is time for a refresh cycle. The refresh timer is reset when a refresh cycle is requested.

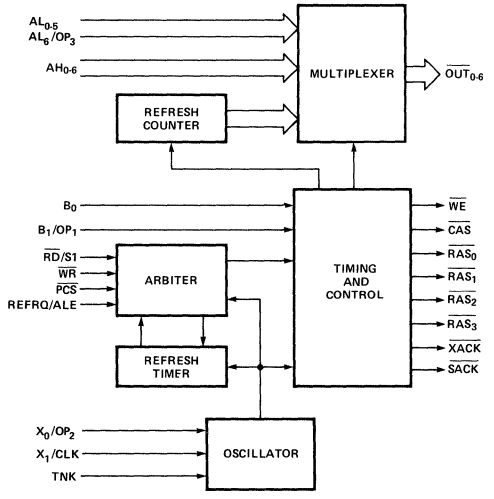
Refresh Counter

The refresh counter contains the address of the row to be refreshed. This counter is incremented after every refresh cycle.

Multiplexer

The multiplexer is designed to provide the dynamic RAM array with row addresses, column addresses and refresh addresses at the proper times. Its inputs consist of AL_{0-5}, AL_6/OP_3, AH_{0-6}, and the refresh counter.

If AL_6/OP_3 is pulled to +12V through a 5KΩ resistor, the 8202 configures itself for 4K RAMs. In this mode, AL_{0-5} provides the multiplexer with the six bit row address. AH_{0-5} provides the multiplexer with the six bit column address.



$\overline{OUT}_{0-5}$ provide the RAM array with twelve bits of multiplexed address. AH_6 can be used as an active high chip select for the RAM array if $\overline{OUT}_6$ drives $\overline{CS}$. Note that the $\overline{OUT}_{0-6}$ signals do not require inverters or drivers.

If the 8202 is configured for 16K RAMs, AL_{0-5} and AL_6/OP_3 provide the multiplexer with seven bits of row

address. $\overline{AH}_{0-6}$ provides it with seven bits of column address. $\overline{OUT}_{0-6}$ provides the RAM array with fourteen bits of multiplexed address.

Timing and Control Block

The timing and control block executes one of three operational cycles at the request of the arbiter (Read, Write, and Refresh cycles). It provides the RAM array with $\overline{WE}$, $\overline{CAS}$, and $\overline{RAS}$ signals. It provides the CPU with transfer and system acknowledge ($\overline{XACK}$ and $\overline{SACK}$) signals. It controls the multiplexer during all cycles. It resets the refresh timer and increments the refresh counter during refresh cycles.

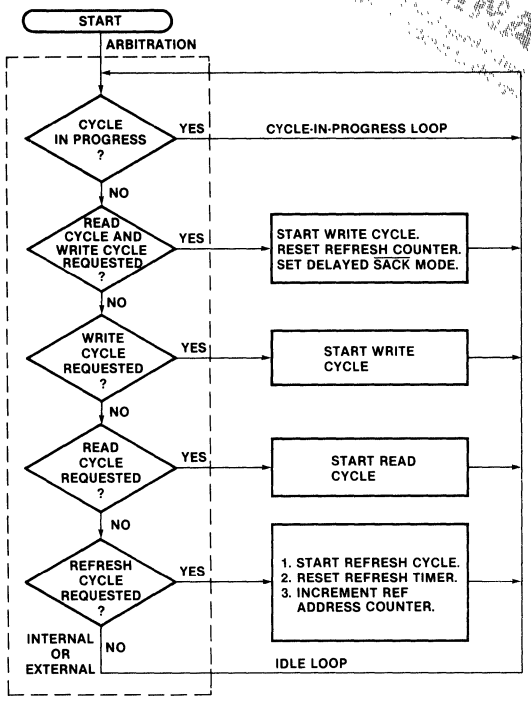
Inputs B_0 and B_1/OP_1 are used to select one of four banks of dynamic RAM via the $\overline{RAS}_{0-3}$ outputs.

If B_1/OP_1 is pulled to +12V through a 5KΩ resistor, the 8202 configures itself to the Advanced Read Mode. This mode changes the function of the $\overline{RD}/S_1$ and REFRQ/ALE inputs and disables the $\overline{RAS}_0$ and $\overline{RAS}_1$ outputs.

SYSTEM OPERATION

The 8202 is always in one of the following states:

1. Idle.
2. Performing a Test Cycle.
3. Performing a Write Cycle.
4. Performing a Read Cycle.
5. Performing a Refresh Cycle.



Idle

When the 8202 is idle, no cycle is in progress, the arbiter monitors internal and external cycle requests, and the refresh timer counts towards an internal refresh cycle request. (Fig. X.1)

While the 8202 is idle, the arbiter samples access cycle requests and refresh cycle requests, internal or external, on the rising edge of clock. If both Read and Write cycle requests are active when sampled, a test cycle is started. If a write-cycle request is active when sampled, a write cycle is started. If a read cycle request is active when sampled, a read cycle is started. If a refresh cycle request was previously pulsed or is active when sampled, a refresh cycle is started. Due to internal delays, if an access cycle request and a refresh cycle request occur simultaneously, the access cycle will be executed before the refresh cycle is executed.

Test Cycle

When a test cycle is started, (Read and Write Cycle Requests both active when sampled) the refresh counter is set to zero and the delayed $\overline{SACK}$ mode is reset, while the 8202 executes a write cycle. This cycle is used for testing only and is not recommended for normal system operation.

Write Cycle (Fig. X.2)

When a write cycle is started, (Write-Cycle Request active when sampled) the Multiplexer drives the $\overline{OUT}$ 0-6 pins with the low order address. Then, if the delayed $\overline{SACK}$ Mode is not set, $\overline{SACK}$ is activated. The row address is strobed into the selected bank of RAMs. The multiplexer then drives the $\overline{OUT}$ 0-6 pins with the high order address and the write enable ($\overline{WE}$) pin is activated. The column address is then strobed into the RAM array.

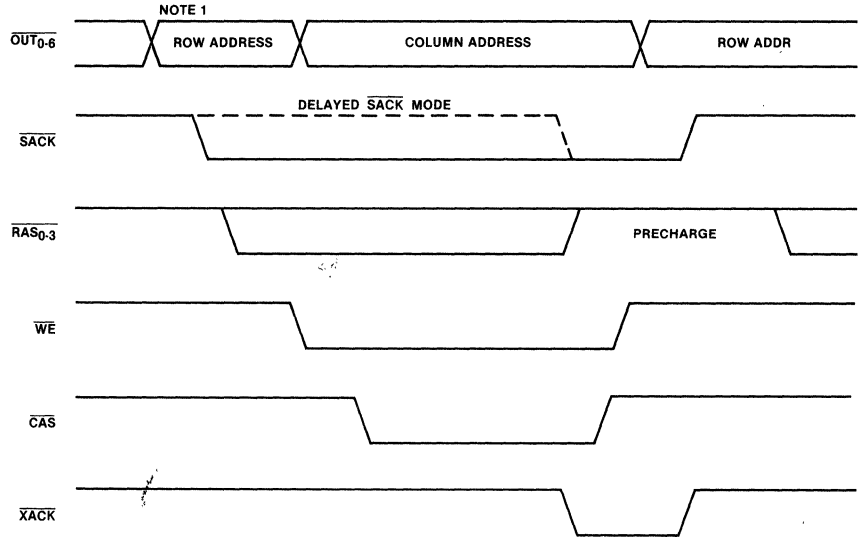
Near the end of the cycle, the $\overline{XACK}$ output is activated. If the Delayed $\overline{SACK}$ Mode is set, $\overline{SACK}$ had the same timing as $\overline{XACK}$. At the end of the cycle, all signals are deactivated, the Delayed $\overline{SACK}$ Mode is exited, and the precharge time begins. After the precharge time, the 8202 re-enters the idle state. The refresh timer continues to count during access cycles.

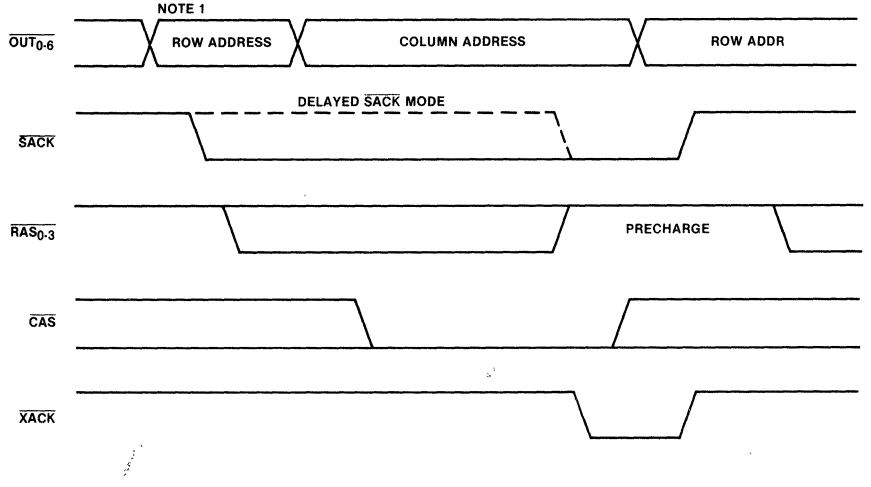
If the REFRQ pin is pulsed or held active while a write cycle is in progress, a refresh cycle will occur immediately following the write cycle, if the Advanced Read Mode is not selected.

Read Cycle (Fig. X.3)

Read cycle operation is the same as write cycle operation, except the write enable ($\overline{WE}$) signal is not activated.

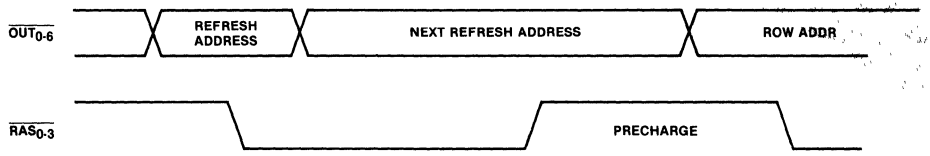
If the REFRQ pin is pulsed or held active while a read cycle is in progress, a refresh cycle will occur immediately following the read cycle, if the Advanced Read Mode is not selected.





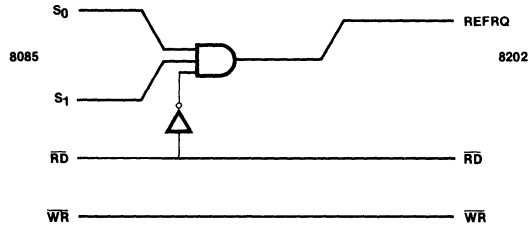
Refresh Cycle (Fig. X.4)

When a refresh cycle is started, (refresh-cycle request previously pulsed or active when sampled) the 8202 resets the Refresh Timer. The Multiplexer drives the OUT 0-6 pins with the refresh address contained in the Refresh Counter. The 8202 then activates the Row Address Strobe (RAS 0-3) signals. At the end of the refresh cycle, all signals are deactivated, the refresh counter is incremented, and the precharge time begins. After the precharge time, the 8202 re-enters the Idle State.



Hidden Refresh Cycle

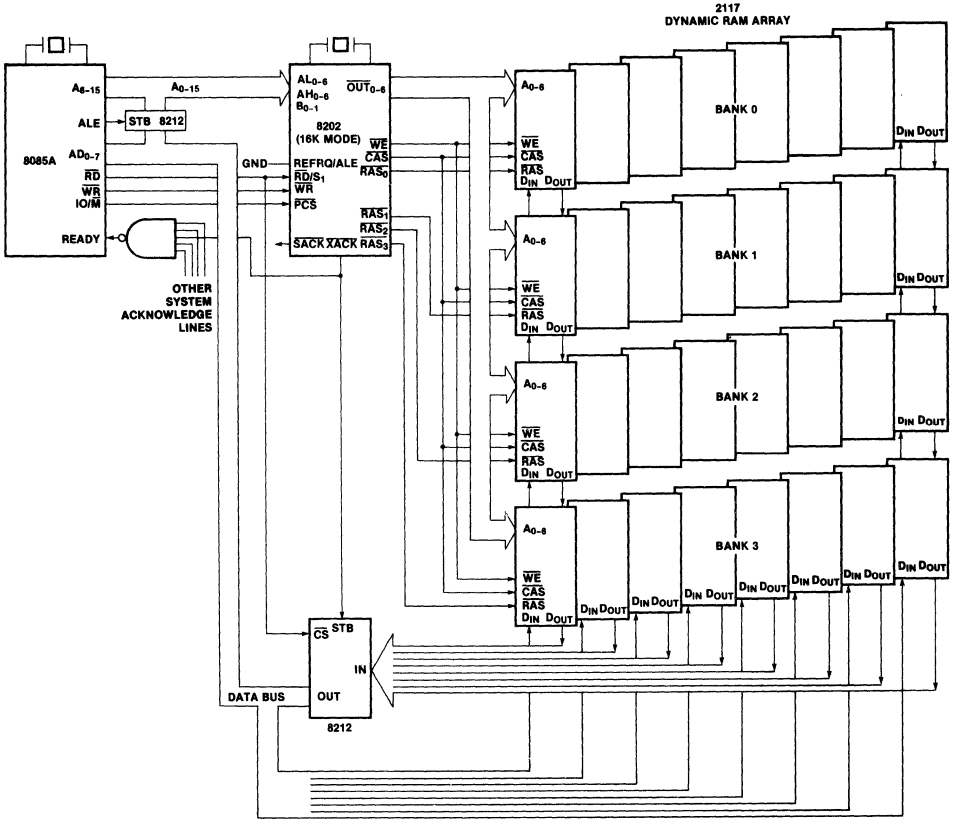
Distributed hidden refresh operation is most efficient if REFRQ is strobed during a command cycle such as fetch, where it is intended for the refresh cycle to follow. This is illustrated for 8085 in the following diagram.



System Configurations

Currently, there exists a wide range of processor bus structures, processor speeds, and memory speeds. As a result, the 8202 offers many possible system configurations with equally many cost-performance tradeoffs.

The following system block diagram illustrates just one of the possible system configurations supported by the 8202:



Other system configurations are described in the Intel, Application Note AP45, "Using the 8202 Dynamic RAM Controller." Other related documents are:

- "Intel Memory Design Handbook" (Dynamic Ram sections).
- AR-1, "Simplify Your Dynamic RAM/Microprocessor Interface."
- AP-38, "Application Techniques for the Intel 8085A Bus."

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias.....0°C to 70°C
Storage Temperature.....-65°C to +150°C
Voltage On Any Pin
With Respect to Ground.....-0.5V to +7V
Power Dissipation.....1.4 Watts

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 10\%$; $GND = 0V$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_C	Input Clamp Voltage		−1.0	V	$I_C = -5$ mA
I_{CC}	Power Supply Current		250	mA	
I_F	Forward Input Current X_1/CLK All Other Inputs		 −2.0 −320	 mA μA	 $V_F = 0.45V$ $V_F = 0.45V$
I_R	Reverse Input Current		40	μA	$V_R = V_{CC}$
V_{OL}	Output Low Voltage $\overline{SACK}$, $\overline{XACK}$ All Other Outputs		 0.45 0.45	 V V	 $I_{OL} = 5$ mA $I_{OL} = 3$ mA
V_{OH}	Output High Voltage $\overline{SACK}$, $\overline{XACK}$ All Other Outputs	 2.4 2.6		 V V	 $I_{OH} = -1$ mA $I_{OH} = -1$ mA
V_{IL}	Input Low Voltage		0.8	V	$V_{CC} = 5.0V$
V_{IH}	Input High Voltage	2.0		V	$V_{CC} = 5.0V$

MPU PERIPHERALS

CAPACITANCE

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		30	pF	$F = 1$ MHz $V_{BIAS} = 2.5V$, $V_{CC} = 5V$ $T_A = 25°C$

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Loading:

$\overline{SACK}$, $\overline{XACK}$	CL = 30 pF
$\overline{OUT_0} - \overline{OUT_6}$	CL = 160 pF
$\overline{RAS_1} - \overline{RAS_4}$	CL = 115 pF
$\overline{WE}$	CL = 224 pF
$\overline{CAS}$	CL = 320 pF

Measurements made with respect to $\overline{RAS_1} - \overline{RAS_4}$, CAS, WE, $\overline{OUT_0} - \overline{OUT_6}$ are at 2.4V and 0.8V. All other pins are measured at 1.5V.

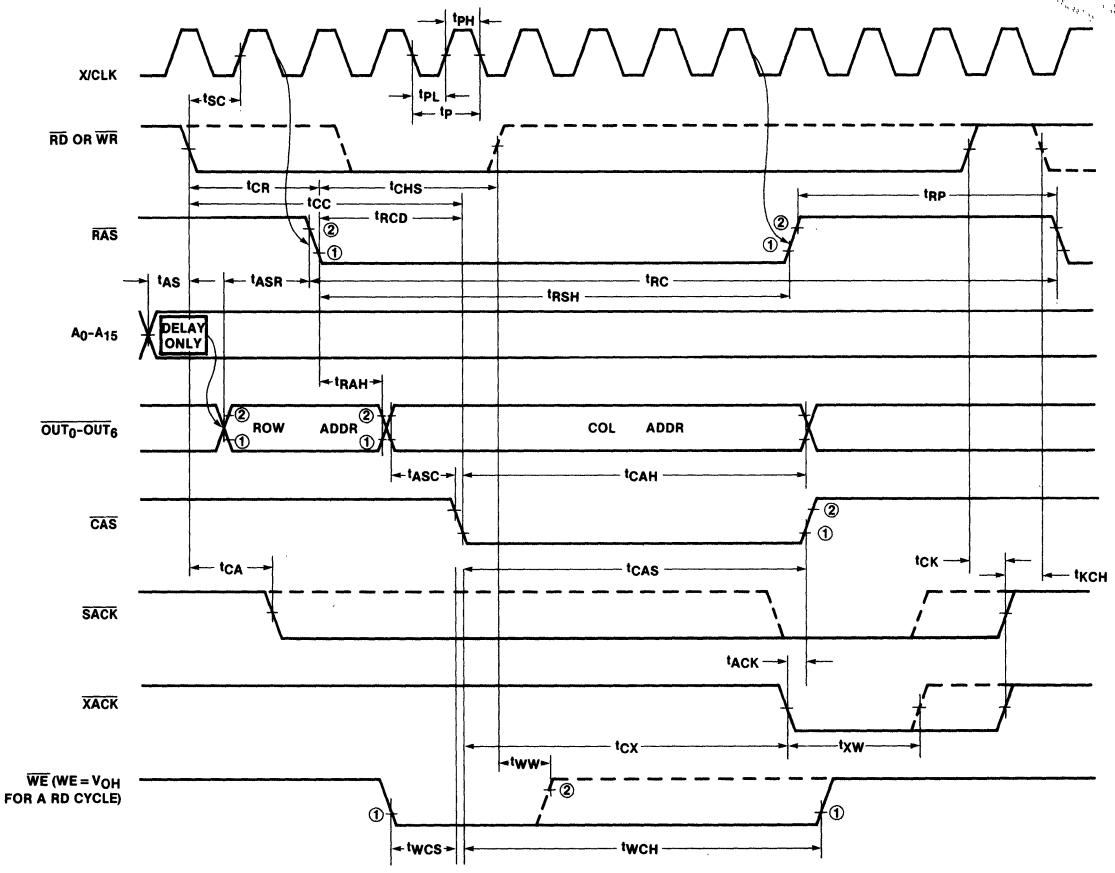
Symbol	Parameter	Min	Max	Units
t_P	Clock (Internal/External) Period (See Note 1)	40	54	ns
t_{RC}	Memory Cycle Time	10 t_P – 30	12 t_P	ns
t_{RAH}	Row Address Hold Time	t_P – 10		ns
t_{ASR}	Row Address Setup Time	t_{PH}		ns
t_{CAH}	Column Address Hold Time	5 t_P		ns
t_{ASC}	Column Address Setup Time	t_P – 35		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	2 t_P – 10	2 t_P + 30	ns
t_{WCS}	$\overline{WE}$ Setup to $\overline{CAS}$	t_P – 40		ns
t_{RSH}	$\overline{RAS}$ Hold Time	5 t_P – 30		ns
t_{CAS}	$\overline{CAS}$ Pulse Width	5 t_P		ns
t_{RP}	$\overline{RAS}$ Precharge Time (See Note 2)	4 t_P – 30		ns
t_{WCH}	$\overline{WE}$ Hold Time to $\overline{CAS}$	5 t_P – 20		ns
t_{REF}	Internally Generated Refresh to Refresh Time 64 Cycle 128 Cycle	 548 t_P 264 t_P	 576 t_P 288 t_P	 ns ns
t_{CR}	$\overline{RD}$, $\overline{WR}$ to $\overline{RAS}$ Delay	t_{PH} + 30	t_{PH} + t_P + 75	ns
t_{CC}	$\overline{RD}$, $\overline{WR}$ to $\overline{CAS}$ Delay	t_{PH} + 2 t_P + 25	t_{PH} + 3 t_P + 85	ns
t_{RFR}	REFRQ to $\overline{RAS}$ Delay	1.5 t_P + 30	2.5 t_P + 100	ns
t_{AS}	$A_0 - A_{15}$ to $\overline{RD}$, $\overline{WR}$ Setup Time (See Note 4)	0		ns
t_{CA}	$\overline{RD}$, $\overline{WR}$ to $\overline{SACK}$ Leading Edge		t_P + 40	ns
t_{CK}	$\overline{RD}$, $\overline{WR}$ to $\overline{XACK}$, $\overline{SACK}$ Trailing Edge Delay		30	ns
t_{KCH}	$\overline{RD}$, $\overline{WR}$ Inactive Hold to $\overline{SACK}$ Trailing Edge	10		ns
t_{SC}	$\overline{RD}$, $\overline{WR}$, $\overline{PCS}$ to X/CLK Setup Time (See Note 3)	15		ns
t_{CX}	$\overline{CAS}$ to $\overline{XACK}$ Time	5 t_P – 25	5 t_P + 20	ns
t_{ACK}	$\overline{XACK}$ Leading Edge to $\overline{CAS}$ Trailing Edge Time	10		ns
t_{XW}	$\overline{XACK}$ Pulse Width	2 t_P – 25		ns
t_{LL}	REFRQ Pulse Width	20		ns
t_{CHS}	$\overline{RD}$, $\overline{WR}$, $\overline{PCS}$ Active Hold to $\overline{RAS}$	0		ns
t_{WW}	$\overline{WR}$ to $\overline{WE}$ Propagation Delay	8	50	ns
t_{AL}	S_1 to ALE Setup Time	40		ns
t_{LA}	S_1 to ALE Hold Time	2 t_P + 40		ns
t_{PL}	External Clock Low Time	15		ns
t_{PH}	External Clock High Time	20		ns
t_{PH}	External Clock High Time for $V_{CC} = 5V \pm 5\%$	17		ns

Notes:

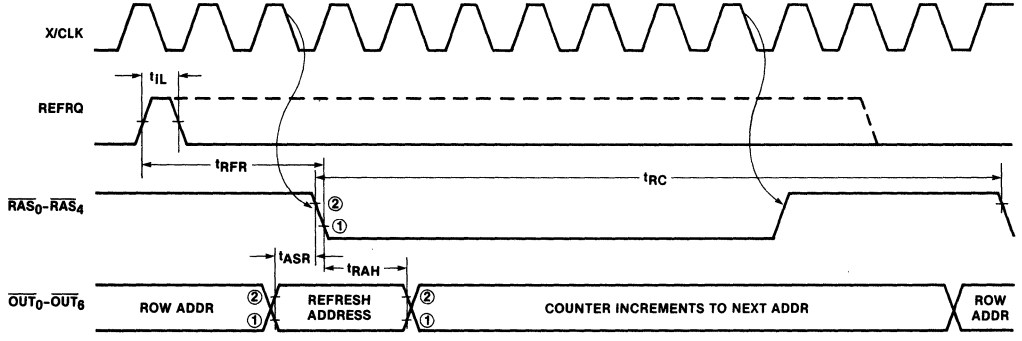
1. t_P minimum determines maximum oscillator frequency.
   t_P maximum determines minimum frequency to maintain 2 ms refresh rate and t_{RP} minimum.
2. To achieve the minimum time between the $\overline{RAS}$ of a memory cycle and the $\overline{RAS}$ of a refresh cycle, such as a transparent refresh, REFRQ should be pulsed in the previous memory cycle.
3. t_{SC} is not required for proper operation which is in agreement with the other specs, but can be used to synchronize external signals with X/CLK if it is desired.
4. If t_{AS} is less than 0 then the only impact is that t_{ASR} decreases by a corresponding amount.

8202 TIMING

NORMAL READ OR WRITE CYCLE

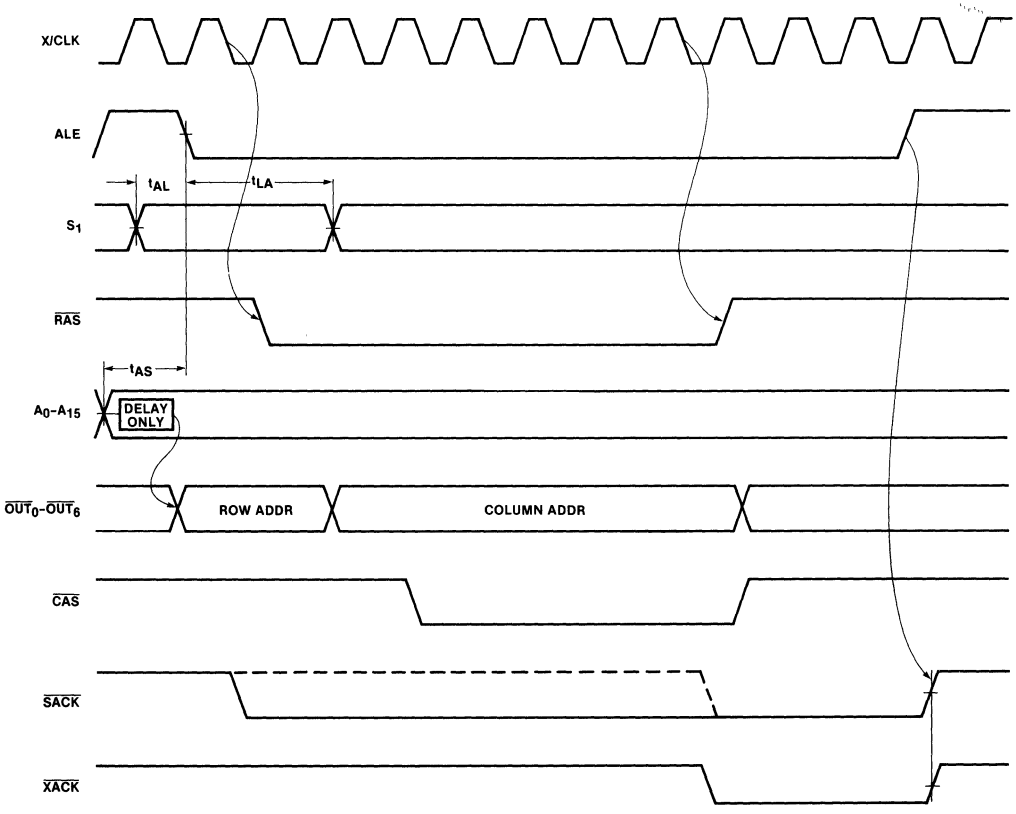


REFRESH CYCLE



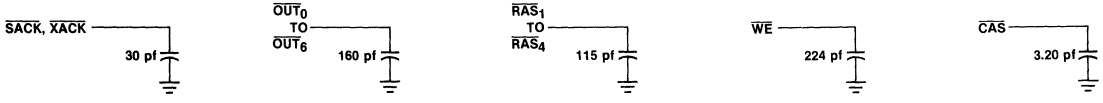
(CAS = VOH) IF THE REFRESH CYCLE IS INTERNALLY TRIGGERED THEN IGNORE REFRQ.

ADVANCED READ MODE USING THE SIMPLIFIED 8085 INTERFACE OPTION



OTHER TIMING PARAMETERS ARE THE SAME AS NORMAL MODE
WRITE CYCLE IS THE SAME AS NORMAL MODE EXCEPT THAT $\overline{XACK}$ AND $\overline{SACK}$ GO INACTIVE ON THE RISING EDGE OF ALE

OUTPUT TEST LOAD CIRCUIT



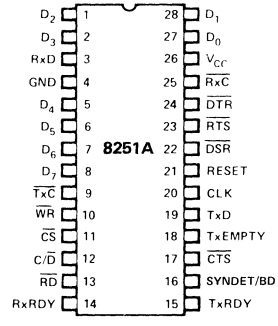
8251A
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
- **Synchronous 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion**
- **Asynchronous 5-8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling.**
- **Synchronous Baud Rate — DC to 64K Baud**
- **Asynchronous Baud Rate — DC to 19.2K Baud**
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun and Framing**
- **Fully Compatible with 8080/8085 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs are TTL Compatible**
- **Single +5V Supply**
- **Single TTL Clock**

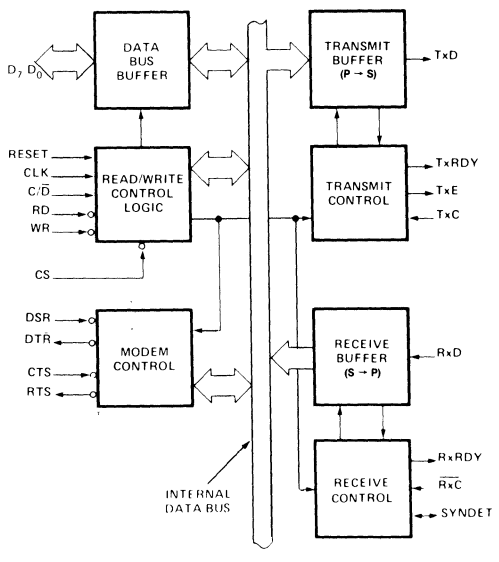
The Intel® 8251A is the enhanced version of the industry standard, Intel® 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's new high performance family of microprocessors such as the 8085. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is constructed using N-channel silicon gate technology.

MPU PERIPHERALS

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D_7 D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char from 8080)

$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

FEATURES AND ENHANCEMENTS

8251A is an advanced design of the industry standard USART, the Intel® 8251. The 8251A operates with an extended range of Intel microprocessors that includes the new 8085 CPU and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements, and reviewing the AC and DC specifications of the 8251A.

The 8251A incorporates all the key features of the 8251 and has the following additional features and enhancements:

- 8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.
- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the 8251A is not selected, the $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device.
- The 8251A Status can be read at any time but the status update will be inhibited during status read.
- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Synchronous Baud rate from DC to 64K.
- Fully compatible with Intel's new industry standard, the MCS-85.

FOR COMPLETE INFORMATION ON THIS DATA SHEET

When used as an input (external SYNC detect mode), a positive going signal will cause the 8251A to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. When External SYNC Detect is programmed, the Internal SYNC Detect is disabled.

BREAK DETECT (Async Mode Only)

This output will go high whenever the receiver remains low through two consecutive stop bit sequences (including the start bits, data bits, and parity bits). Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

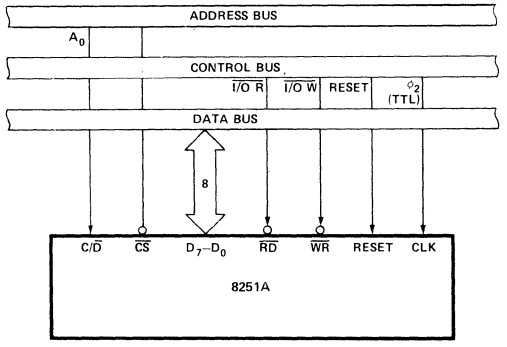


Figure 4. 8251A Interface to 8080 Standard System Bus

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251A is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the 8251A to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD/OFF PARITY, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251A is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251A. On the other hand, the 8251A receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251A has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The 8251A cannot begin transmission until the Tx Enable (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251A

Prior to starting data transmission or reception, the 8251A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251A and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

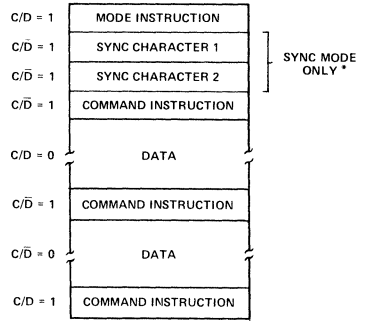
This format defines the general operational characteristics of the 8251A. It must follow a Reset operation (internal or external). Once the Mode Instruction has been written into the 8251A by the CPU, SYNC characters or Command Instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251A.

Both the Mode and Command Instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251A for data communication.

All control words written into the 8251A after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251A at any time in the data block during the operation of the 8251A. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251A back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.



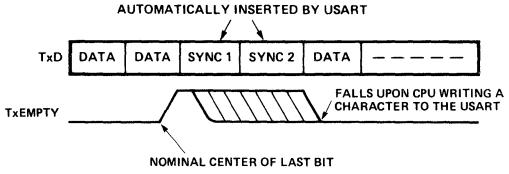
* The second SYNC character is skipped if MODE instruction has programmed the 8251A to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251A to ASYNC mode.

Figure 5. Typical Data Block

Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251A which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251A with a data character before the 8251A Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251A is empty and SYNC characters are being sent out. TxEMPTY does not go low when the SYNC is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the 8251A.



Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the SYNC mode has been programmed, ENTER HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared at every bit boundary with the first SYNC character until a match occurs. If the 8251A has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the 8251A out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode. Parity is checked when not in Hunt, regardless of whether the Receiver is enabled or not.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost. This will also set all the used character bits in the buffer to a "one", thus preventing a possible false SYNDET caused by data that happens to be in the Rx Buffer at ENTER HUNT time. Note that the SYNDET F/F is reset at each Status Read, regardless of whether internal or external SYNC has been programmed. This does not cause the 8251A to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the "known" word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been programmed, then both sync characters have been contiguously received to gate a SYNDET indication.) When external SYNDET mode is selected, internal Sync Detect is disabled, and the SYNDET F/F may be set at any bit boundary.

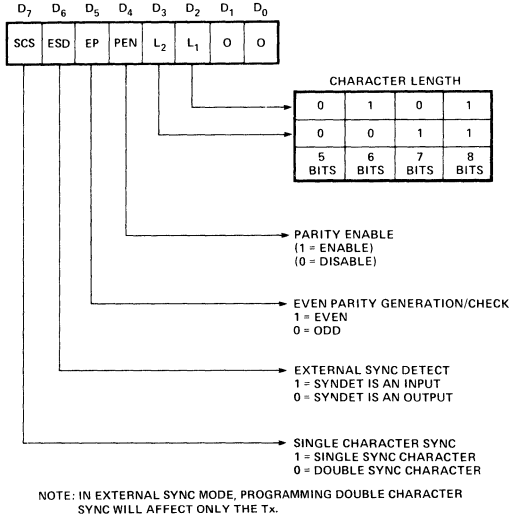


Figure 8. Mode Instruction Format, Synchronous Mode

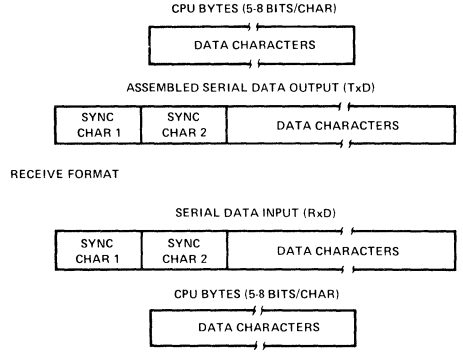


Figure 9. Data Format, Synchronous Mode

MPU PERIPHERALS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –400 μA
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} TO 0.45V
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} TO 0.45V
I_{CC}	Power Supply Current		100	mA	All Outputs = High

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND

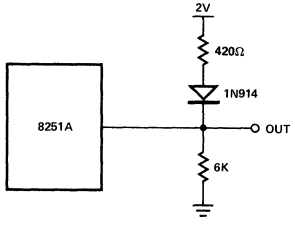


Figure 16. Test Load Circuit

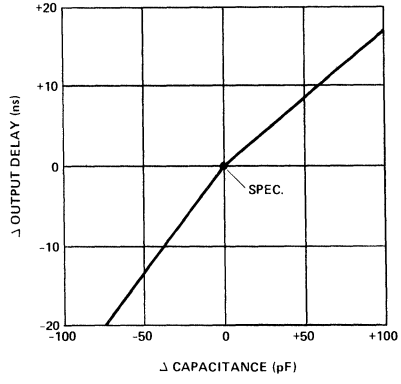


Figure 17. Typical Δ Output Delay vs. Δ Capacitance (pF)

A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

Bus Parameters (Note 1)

Read Cycle:

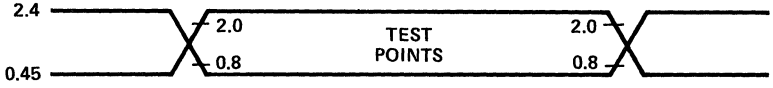
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	50		ns	Note 2
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	50		ns	Note 2
t_{RR}	$\overline{READ}$ Pulse Width	250		ns	
t_{RD}	Data Delay from $\overline{READ}$		250	ns	3, C_L = 150 pF
t_{DF}	$\overline{READ}$ to Data Floating	10	100	ns	

Write Cycle:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AW}	Address Stable Before $\overline{WRITE}$	50		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	50		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	250		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	150		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	30		ns	
t_{RV}	Recovery Time Between WRITES	6		t_{CY}	Note 4

NOTES: 1. AC timings measured V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.
2. Chip Select ($\overline{CS}$) and Command/Data (C/$\overline{D}$) are considered as Addresses.
3. Assumes that Address is valid before $\overline{RD}\downarrow$.
4. This recovery time is for Mode Initialization only. Write Data is allowed only when TxRDY = 1.
Recovery Time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.

Input Waveforms for AC Tests



Other Timings:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{CY}	Clock Period	320	1350	ns	Notes 5, 6
t_{ϕ}	Clock High Pulse Width	140	t_{CY-90}	ns	
$t_{\overline{\phi}}$	Clock Low Pulse Width	90		ns	
t_R, t_F	Clock Rise and Fall Time	5	20	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	
f_{Tx}	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	64	kHz	
	16x Baud Rate	DC	310	kHz	
	64x Baud Rate	DC	615	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1x Baud Rate	DC	64	kHz	
	16x Baud Rate	DC	310	kHz	
	64x Baud Rate	DC	615	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
t_{TxRDY}	TxRDY Pin Delay from Center of last Bit		8	t_{CY}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$		180	ns	Note 7
t_{RxRDY}	RxRDY Pin Delay from Center of last Bit		24	t_{CY}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$		150	ns	Note 7
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$		24	t_{CY}	Note 7
t_{ES}	External SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$		16	t_{CY}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Last Bit		20	t_{CY}	Note 7
t_{WC}	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)		8	t_{CY}	Note 7
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		20	t_{CY}	Note 7

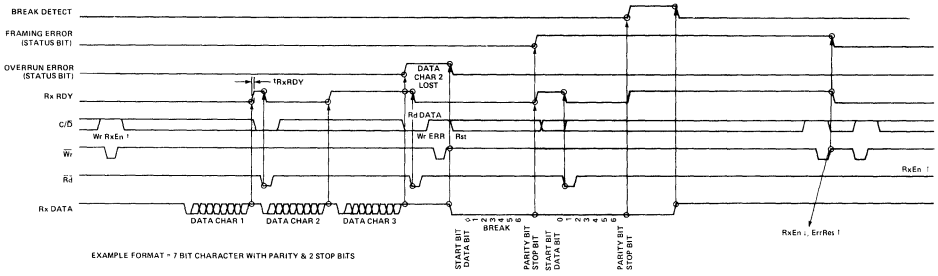
MPU PERIPHERALS

5. The TxC and RxC frequencies have the following limitations with respect to CLK.
   For 1x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
   For 16x and 64x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$

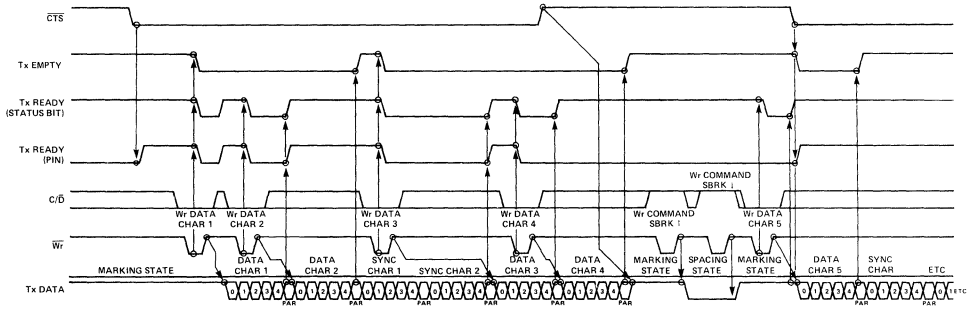
6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during Reset.

7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

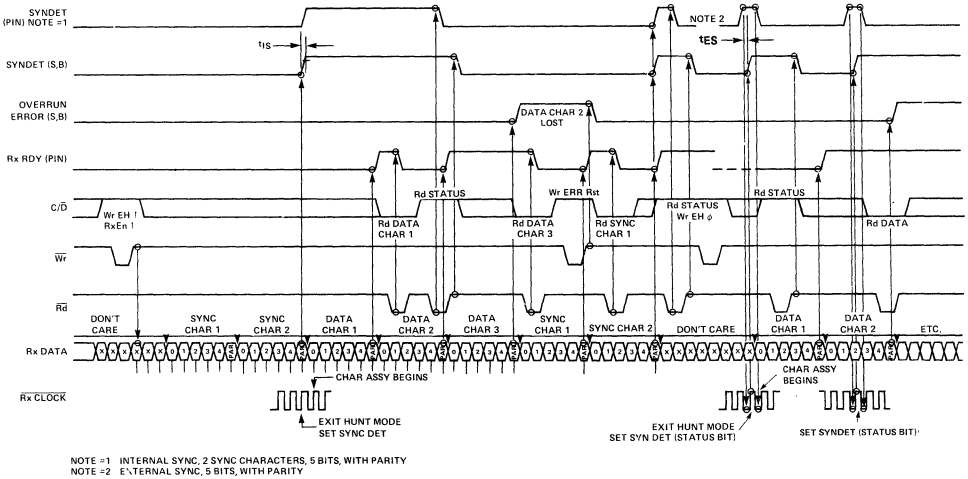
Receiver Control & Flag Timing (ASYNC Mode)



Transmitter Control & Flag Timing (SYNC Mode)



Receiver Control & Flag Timing (SYNC Mode)



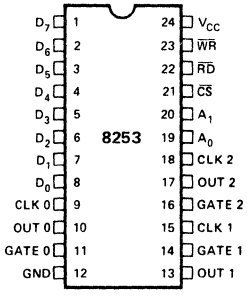
8253/8253-5
PROGRAMMABLE INTERVAL TIMER

- **MCS—85™ Compatible 8253-5**
- **3 Independent 16-Bit Counters**
- **DC to 2 MHz**
- **Programmable Counter Modes**
- **Count Binary or BCD**
- **Single +5V Supply**
- **24-Pin Dual In-Line Package**

The Intel® 8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

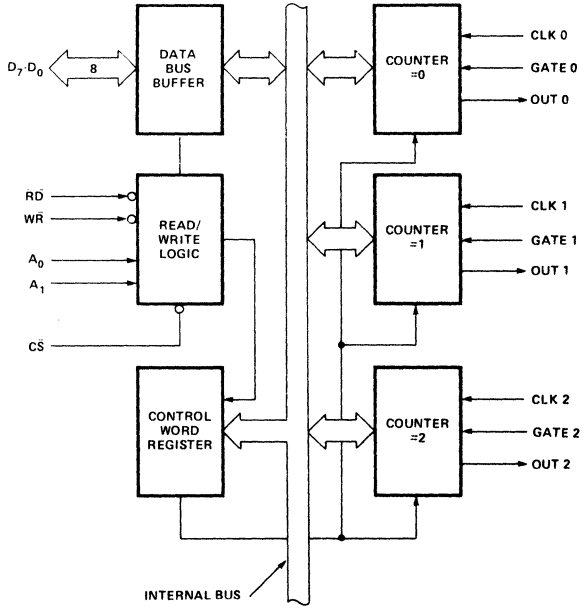
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (8-BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
$\overline{RD}$	READ COUNTER
WR	WRITE COMMAND OR DATA
$\overline{CS}$	CHIP SELECT
A_0-A_1	COUNTER SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM



MPU PERIPHERALS

FUNCTIONAL DESCRIPTION

General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

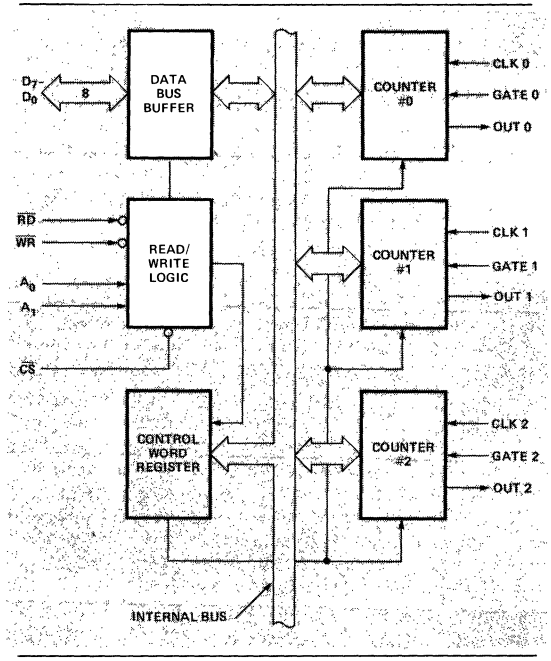


Figure 1. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

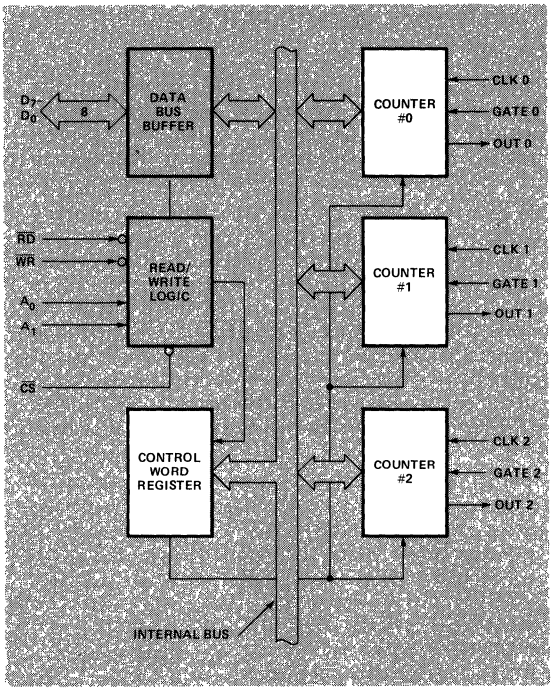


Figure 2. Block Diagram Showing Control Word Register and Counter Functions

8253 SYSTEM INTERFACE

The 8253 is a component of the Intel™ Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.

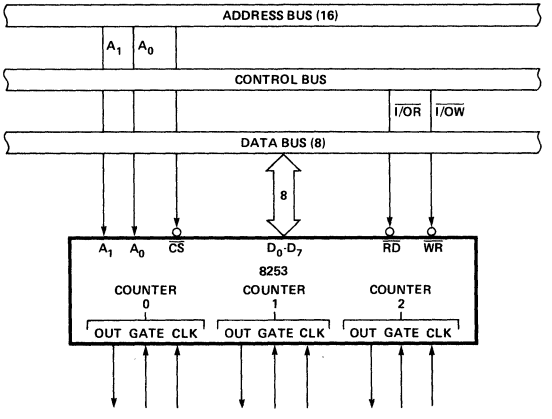


Figure 3. 8253 System Interface

OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL — Read/Load:

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE Definition

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.
(2) Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N – 1)/2 counts.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

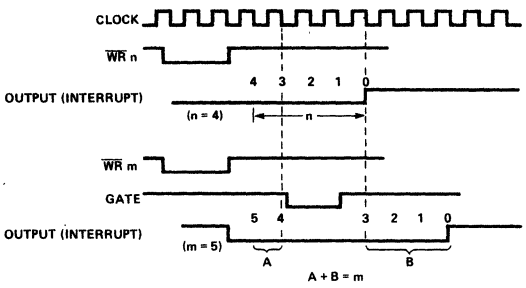
If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

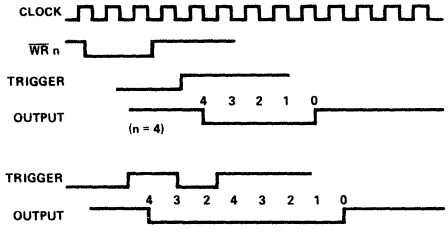
Modes \ Signal Status	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

Figure 4. Gate Pin Operations Summary

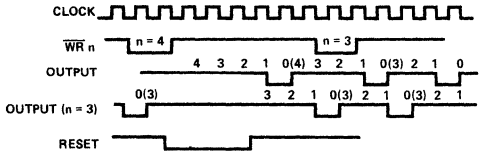
MODE 0: Interrupt on Terminal Count



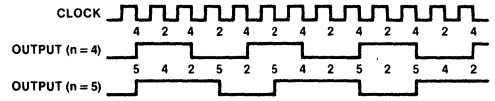
MODE 1: Programmable One-Shot



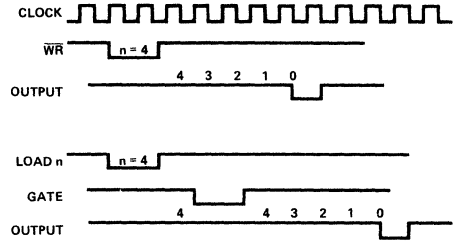
MODE 2: Rate Generator



MODE 3: Square Wave Generator



MODE 4: Software Triggered Strobe



MODE 5: Hardware Triggered Strobe

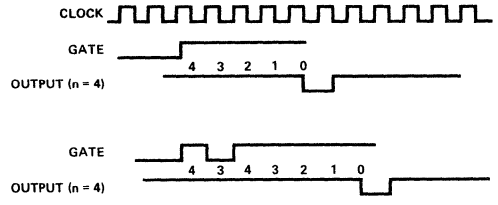


Figure 5. 8253 Timing Diagrams

8253 READ/WRITE PROCEDURE

Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Figure 6. Programming Format

			A1	A0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Figure 7. Alternate Programming Formats

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1-11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB).

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

MODE Register for Latching Count

A0, A1 = 11

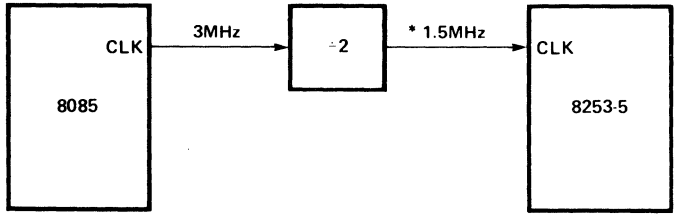
D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1,SC0 — specify counter to be latched.

D5,D4 — 00 designates counter latching operation.

X — don't care.

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.



*If an 8085 clock output is to drive an 8253-5 clock input, it must be reduced to 2 MHz or less.

Figure 8. MCS-85™ Clock Interface*

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5 V to +7 V
Power Dissipation ..... 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}+.5V	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 2
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		140	mA	

Note 1: 8253, I_{OL} = 1.6 mA; 8253-5, I_{OL} = 2.2 mA.
Note 2: 8253, I_{OH} = −150 μA; 8253-5, I_{OH} = −400 μA.

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V

Bus Parameters (Note 1)

Read Cycle:

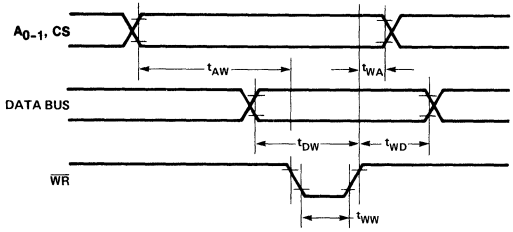
SYMBOL	PARAMETER	8253 MIN.	8253 MAX.	8253-5 MIN.	8253-5 MAX.	UNIT
t_{AR}	Address Stable Before $\overline{READ}$	50		30		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
t_{RD}	Data Delay From $\overline{READ}$[2]		300		200	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	ns
t_{RV}	Recovery Time Between READ and Any Other Control Signal	1		1		μs

Write Cycle:

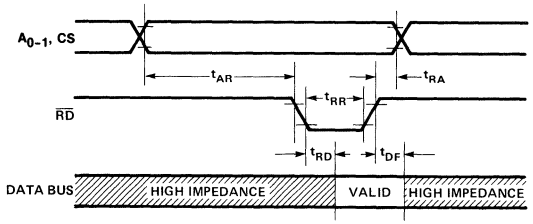
SYMBOL	PARAMETER	8253 MIN.	8253 MAX.	8253-5 MIN.	8253-5 MAX.	UNIT
t_{AW}	Address Stable Before $\overline{WRITE}$	50		30		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		250		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
t_{RV}	Recovery Time Between $\overline{WRITE}$ and Any Other Control Signal	1		1		μs

Notes: 1. AC timings measured at $V_{OH} = 2.2$, $V_{OL} = 0.8$
2. Test Conditions: 8253, $C_L = 100pF$; 8253-5: $C_L = 150pF$.

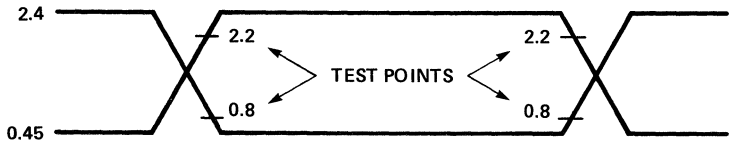
Write Timing:



Read Timing:



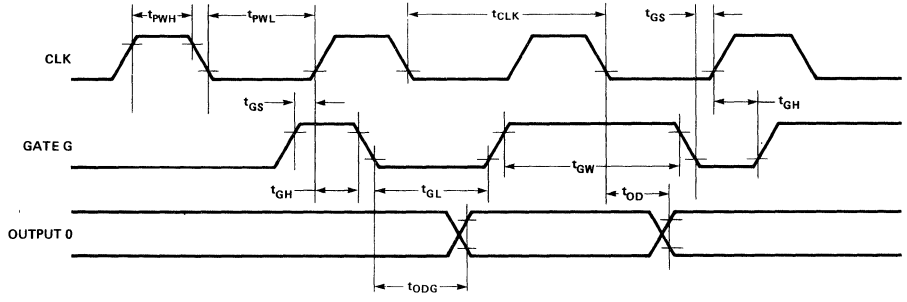
Input Waveforms for A.C. Tests:



Clock and Gate Timing:

SYMBOL	PARAMETER	8253		8253-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{CLK}	Clock Period	380	dc	380	dc	ns
t_{PWH}	High Pulse Width	230		230		ns
t_{PWL}	Low Pulse Width	150		150		ns
t_{GW}	Gate Width High	150		150		ns
t_{GL}	Gate Width Low	100		100		ns
t_{GS}	Gate Set Up Time to CLK↑	100		100		ns
t_{GH}	Gate Hold Time After CLK↑	50		50		ns
t_{OD}	Output Delay From CLK↓[1]		400		400	ns
t_{ODG}	Output Delay From Gate↓[1]		300		300	ns

Note 1: Test Conditions: 8253: C_L = 100pF; 8253-5: C_L = 150pF.

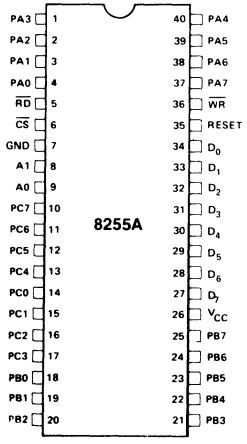


8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

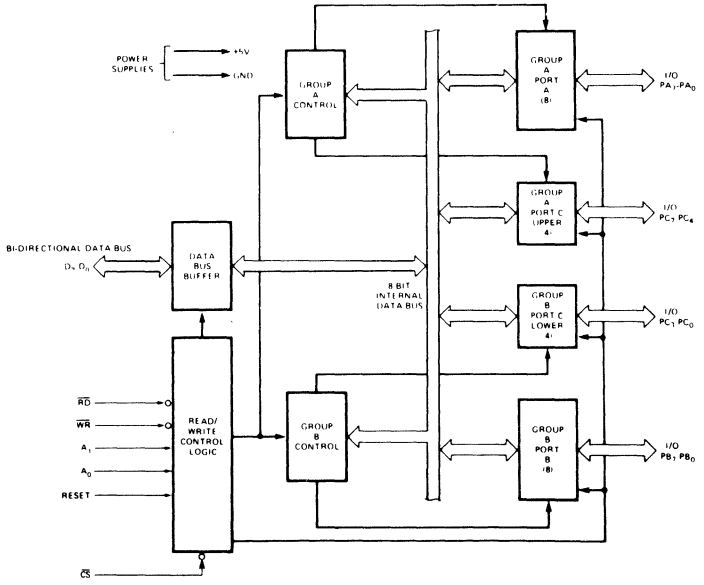
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A BLOCK DIAGRAM



MPU PERIPHERALS

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel® microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communiction between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A ⇒ DATA BUS
0	1	0	1	0	PORT B ⇒ DATA BUS
1	0	0	1	0	PORT C ⇒ DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS ⇒ PORT A
0	1	1	0	0	DATA BUS ⇒ PORT B
1	0	1	0	0	DATA BUS ⇒ PORT C
1	1	1	0	0	DATA BUS ⇒ CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS ⇒ 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS ⇒ 3-STATE

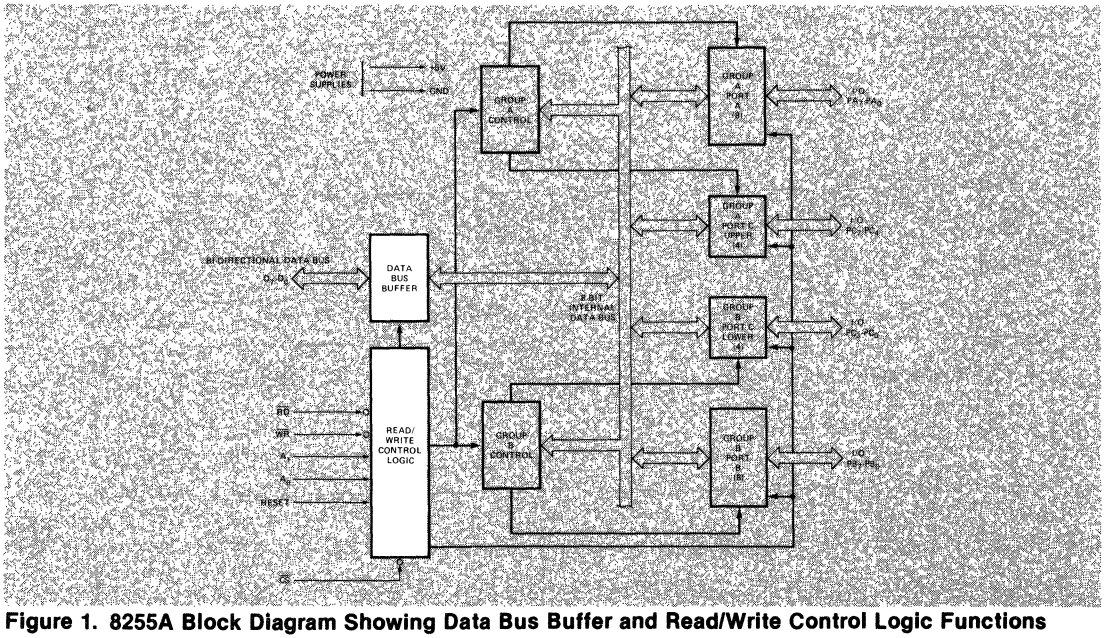


Figure 1. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

(RESET)

Reset. A "high on this input clears the control register and all ports (A, C, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

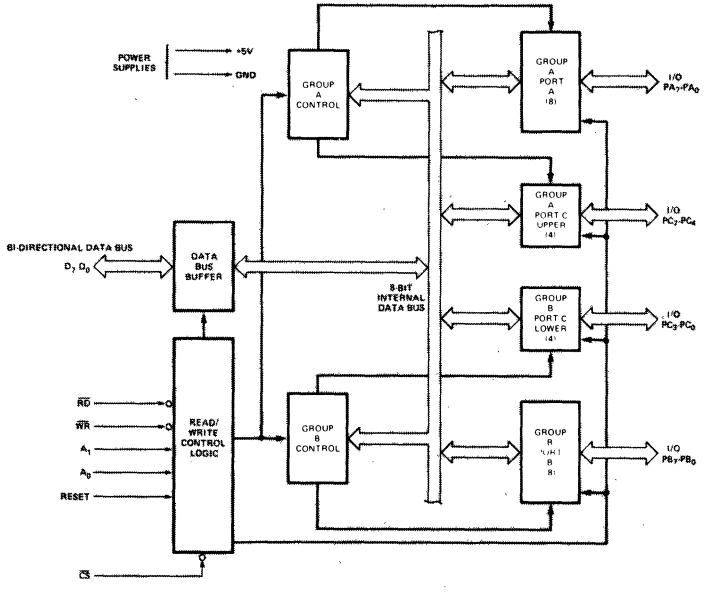
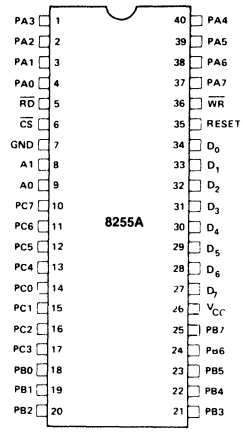


Figure 2. 8225A Block Diagram Showing Group A and Group B Control Functions

PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

MPU PERIPHERALS

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic Input/Output
Mode 1 — Strobed Input/Output
Mode 2 — Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

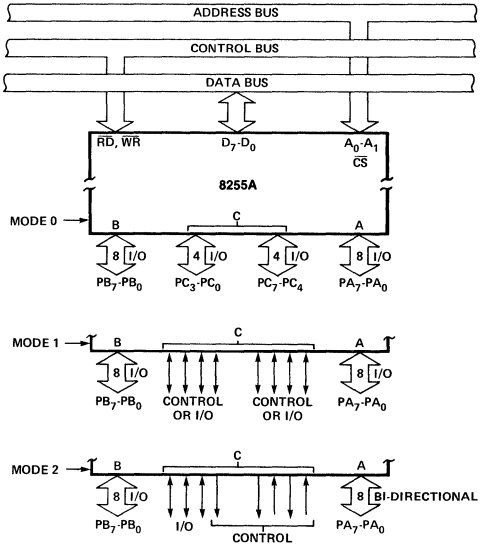


Figure 3. Basic Mode Definitions and Bus Interface

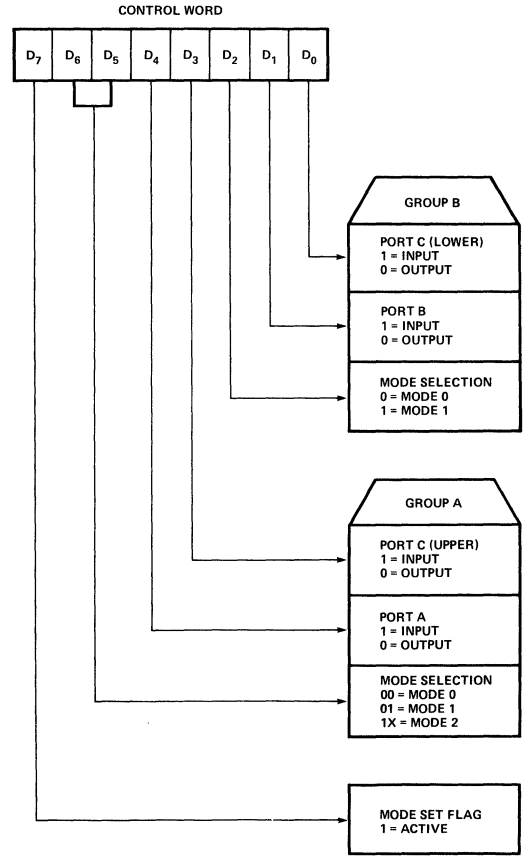


Figure 4. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

MPU PERIPHERALS

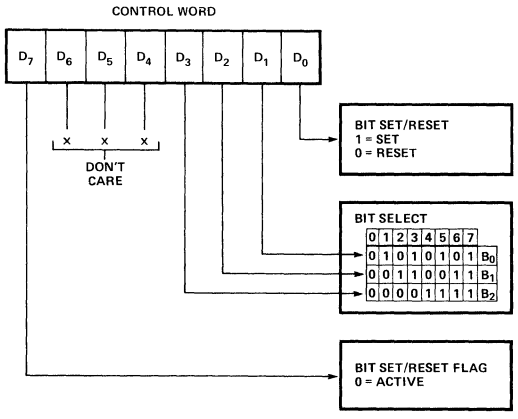


Figure 5. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

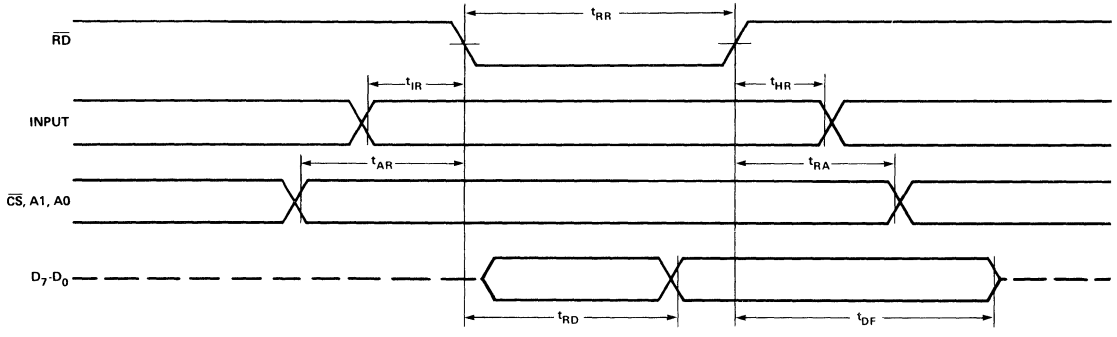
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

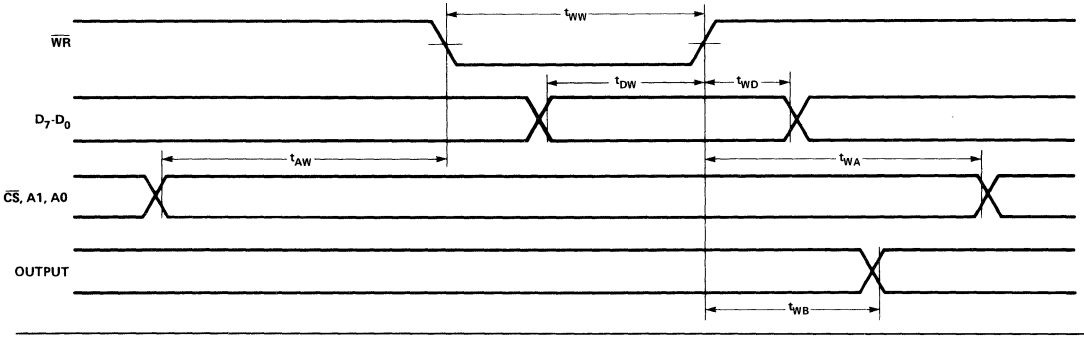
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)



MODE 0 (Basic Output)

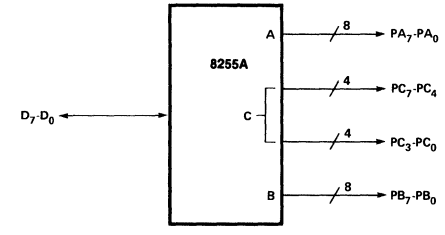
MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations

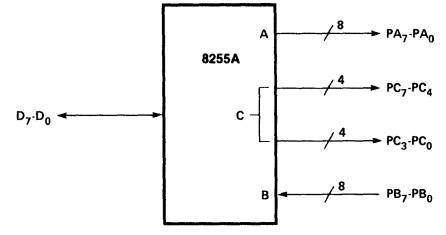
CONTROL WORD #0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0



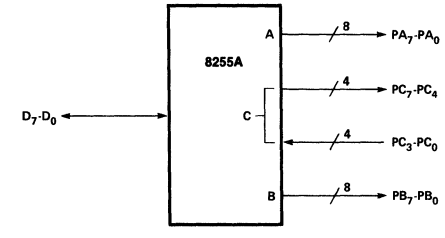
CONTROL WORD #2

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	0



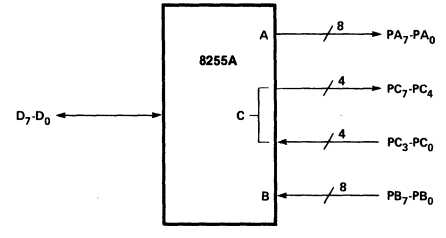
CONTROL WORD #1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	1



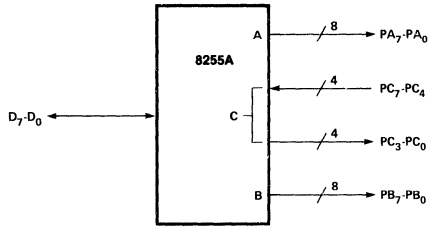
CONTROL WORD #3

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	1



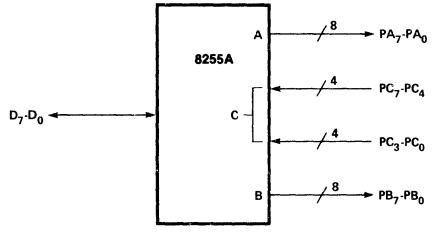
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



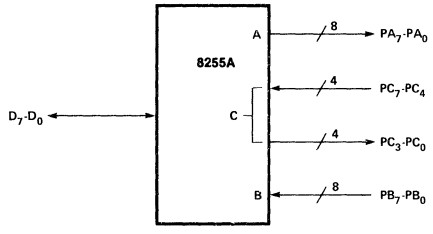
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



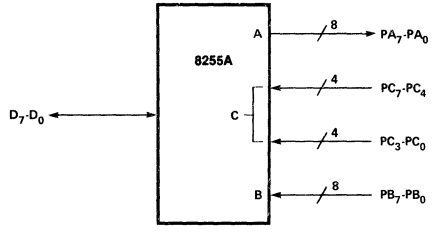
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



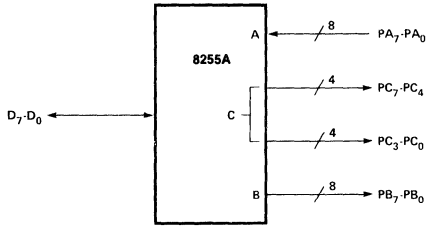
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



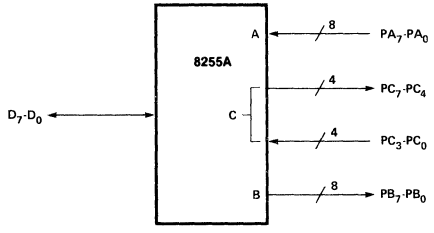
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



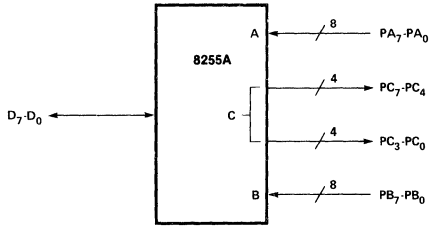
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



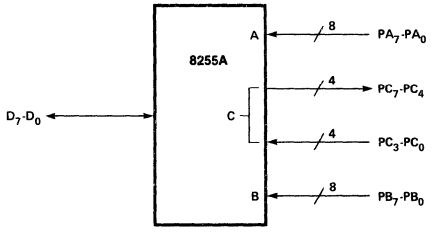
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



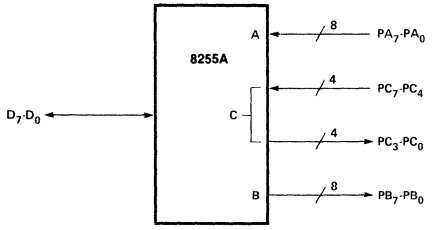
CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1



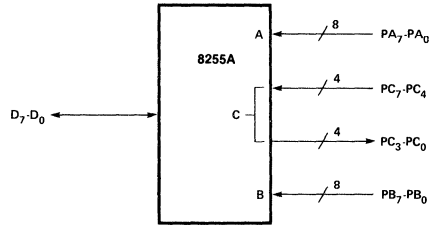
CONTROL WORD #12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	0



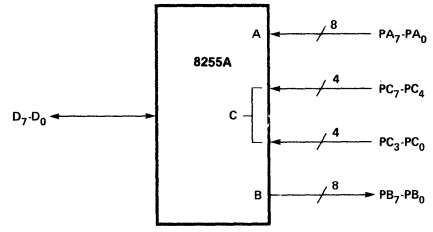
CONTROL WORD #14

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	0



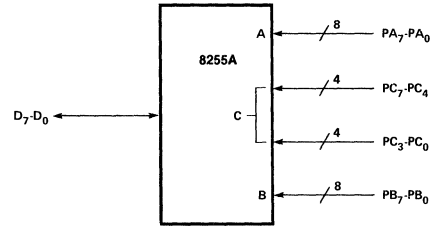
CONTROL WORD #13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	1



CONTROL WORD #15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	1



Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and Port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

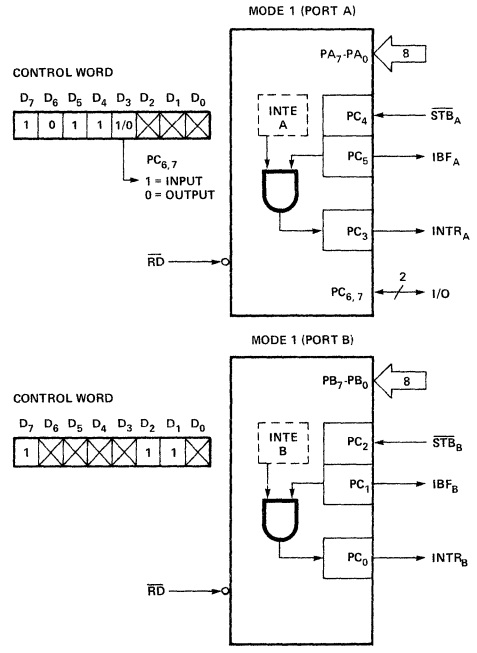


Figure 6. MODE 1 Input

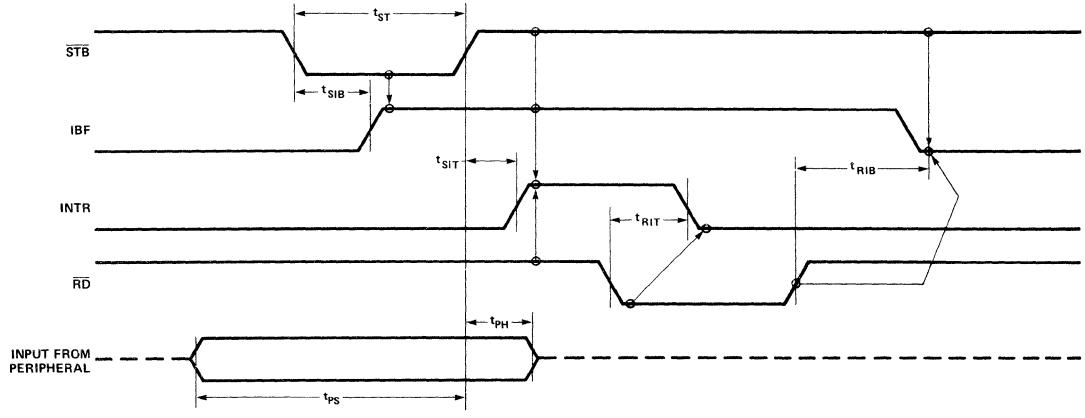


Figure 7. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK Input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

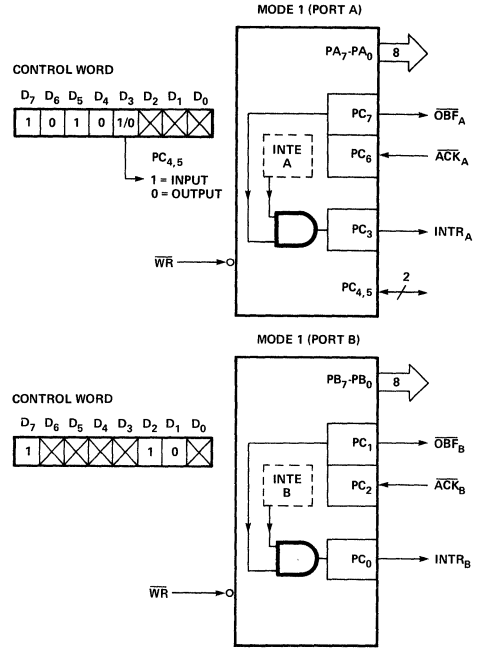


Figure 8. MODE 1 Output

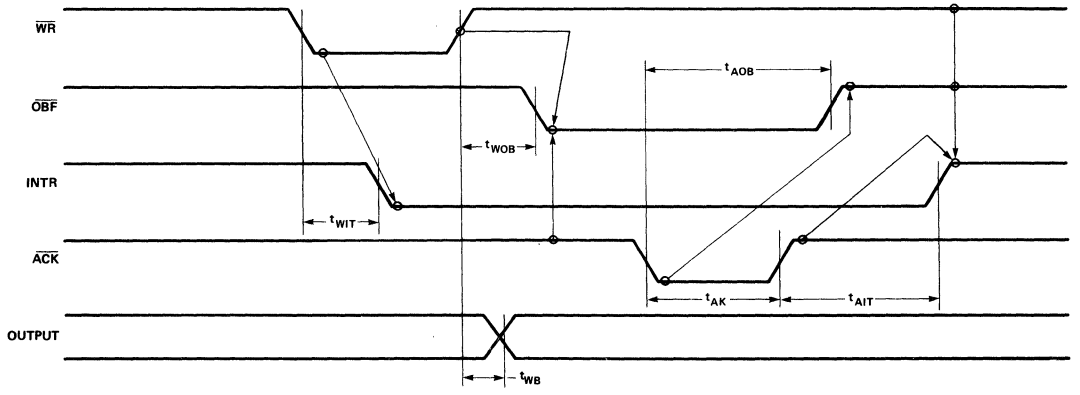


Figure 9. Mode 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

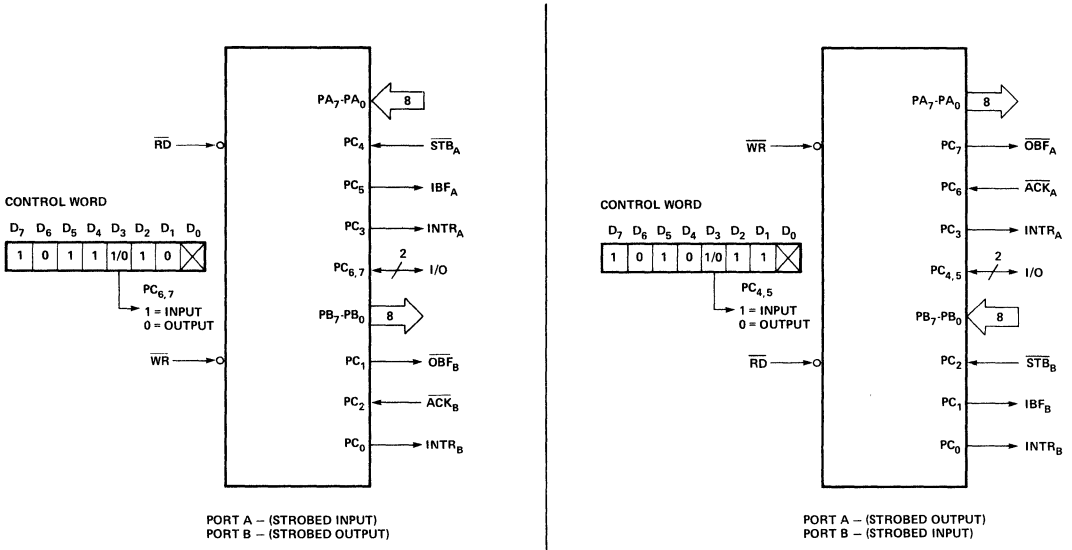


Figure 10. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{\text{OBF}}$ (Output Buffer Ful). The OBF output will go "low" to indicate that the CPU has written data out to port A.

$\overline{\text{ACK}}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{\text{STB}}$ (Strobe Input)

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

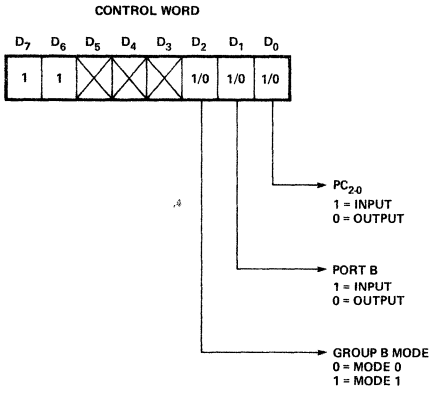


Figure 11. MODE Control Word

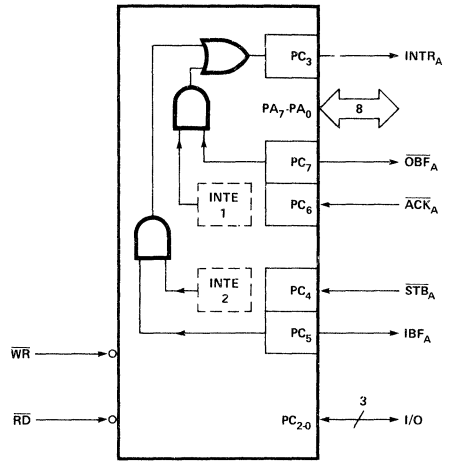


Figure 12. MODE 2

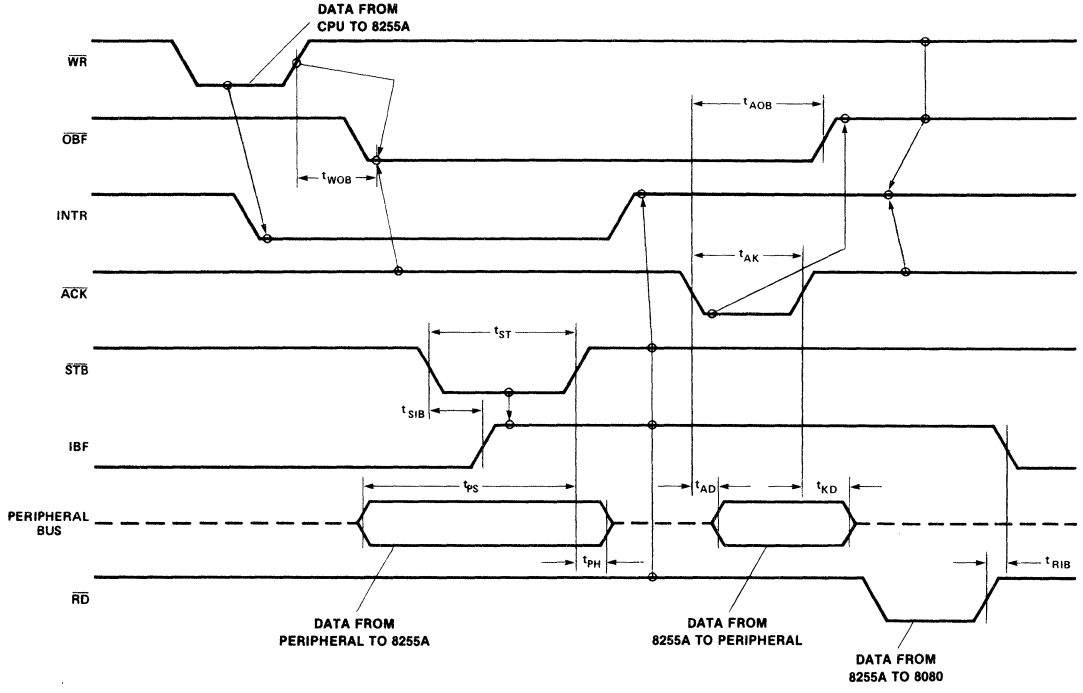


Figure 13. MODE 2 (Bidirectional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

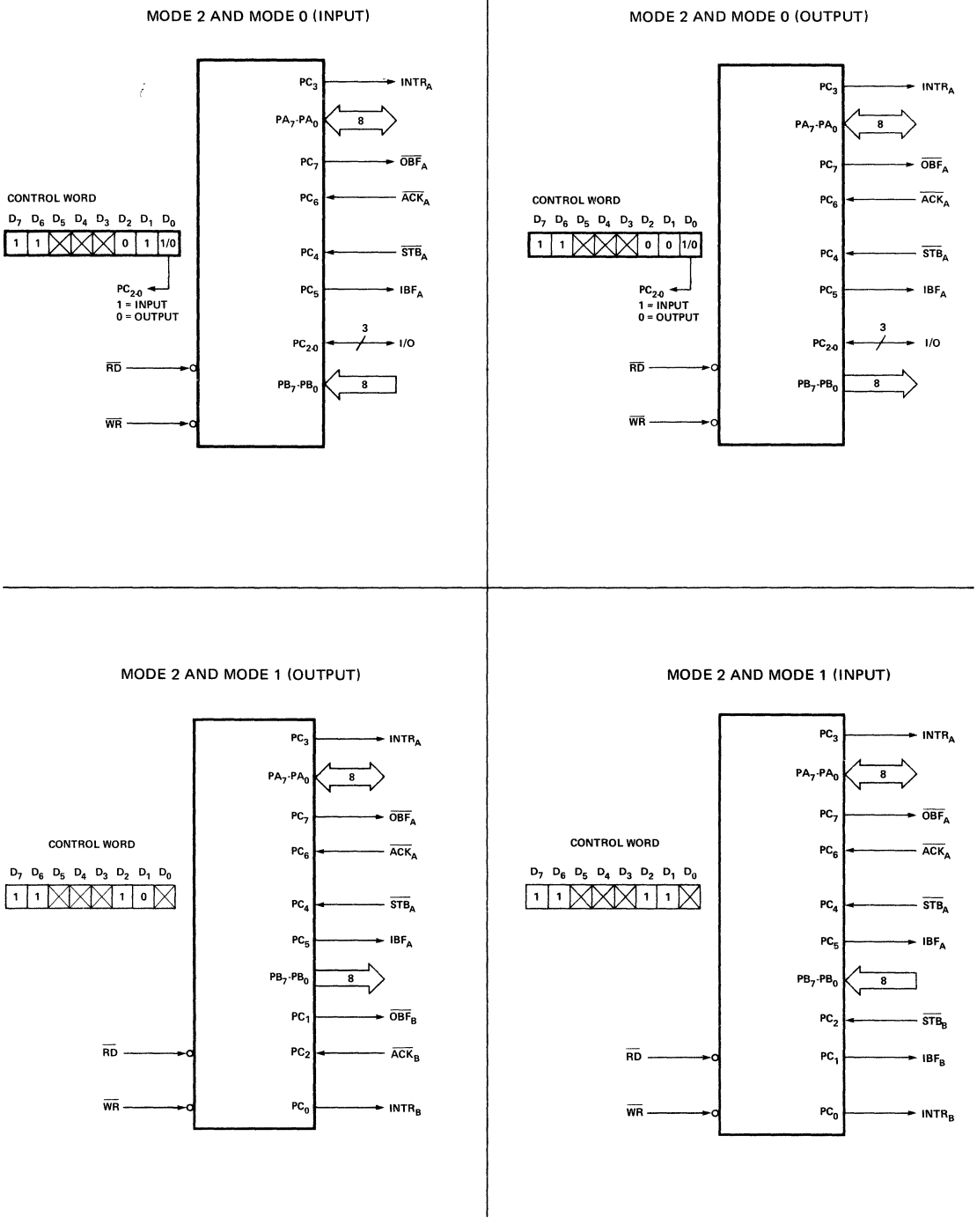


Figure 14. MODE 2 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	◄►	
PA_1	IN	OUT	IN	OUT	◄►	
PA_2	IN	OUT	IN	OUT	◄►	
PA_3	IN	OUT	IN	OUT	◄►	
PA_4	IN	OUT	IN	OUT	◄►	
PA_5	IN	OUT	IN	OUT	◄►	
PA_6	IN	OUT	IN	OUT	◄►	
PA_7	IN	OUT	IN	OUT	◄►	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs –
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs –
Bits in C upper (PC_7-PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

Source Current Capability on Port B and Port C

Any set of **eight** output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

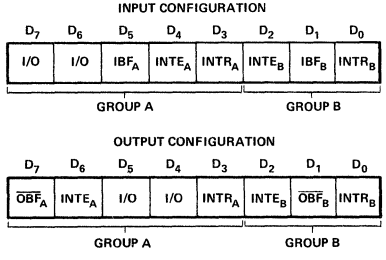


Figure 15. MODE 1 Status Word Format

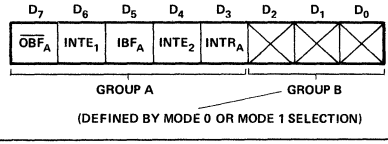


Figure 16. MODE 2 Status Word Format

APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 17 through 23 present a few examples of typical applications of the 8255A.

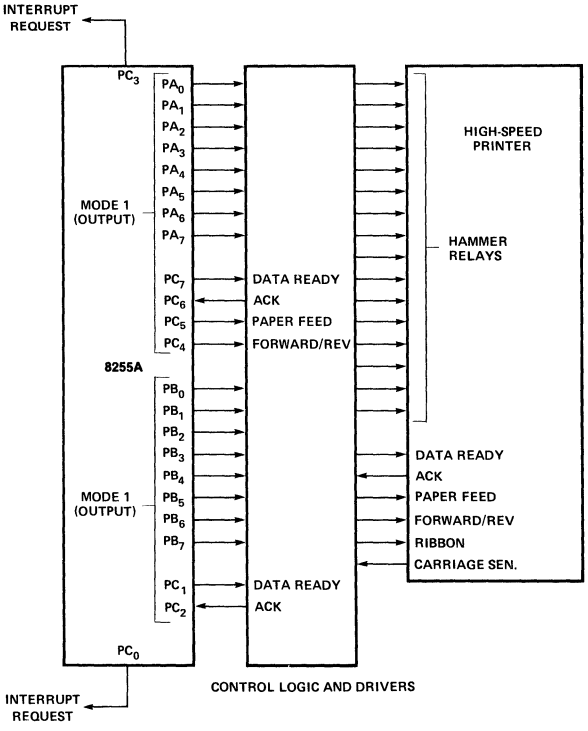


Figure 17. Printer Interface

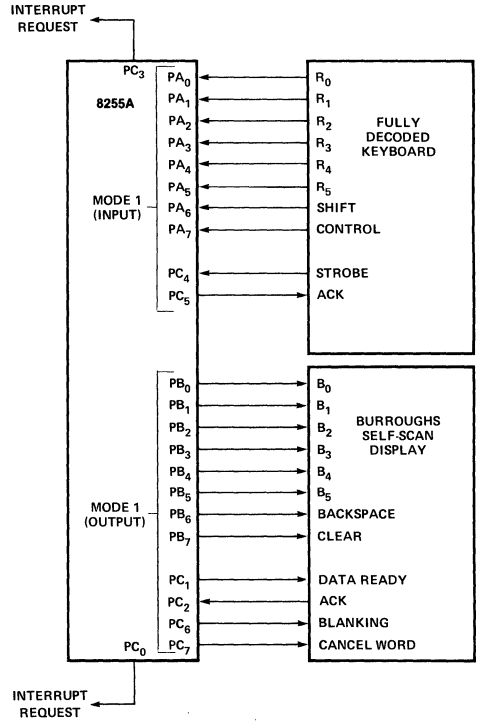


Figure 18. Keyboard and Display Interface

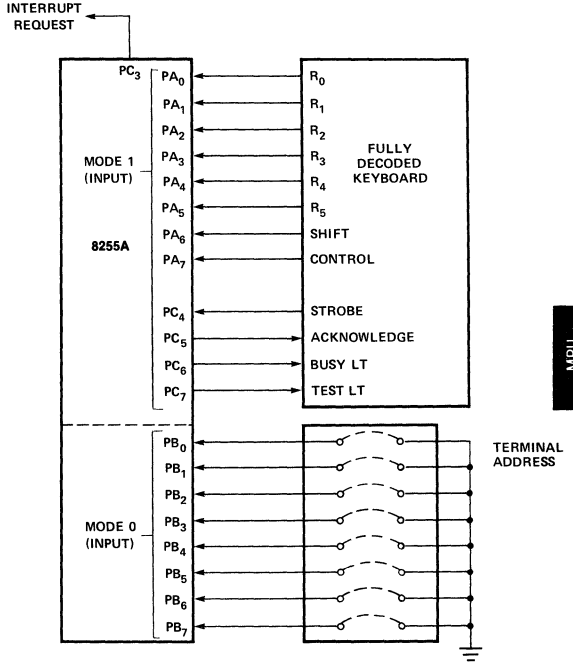


Figure 19. Keyboard and Terminal Address Interface

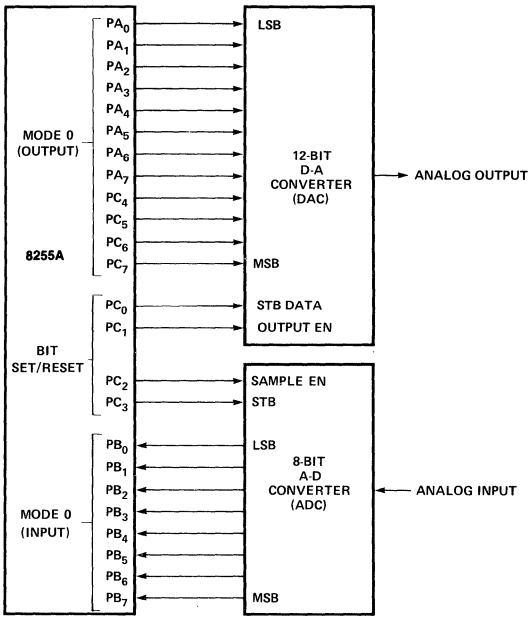


Figure 20. Digital to Analog, Analog to Digital

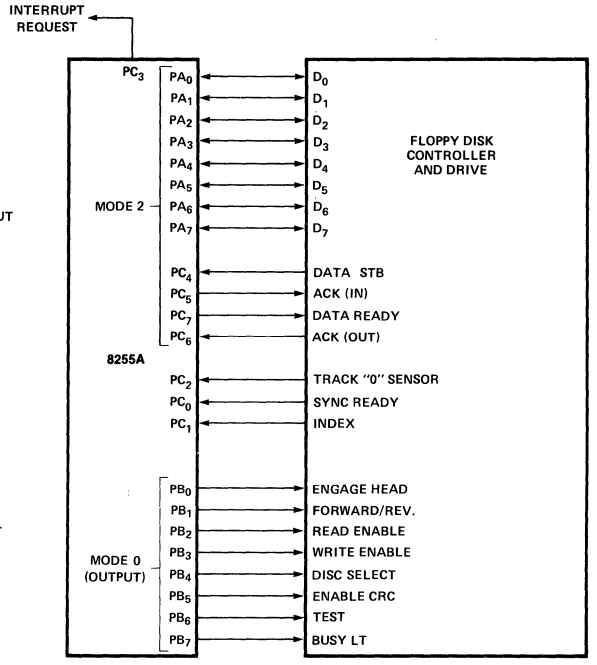


Figure 22. Basic Floppy Disc Interface

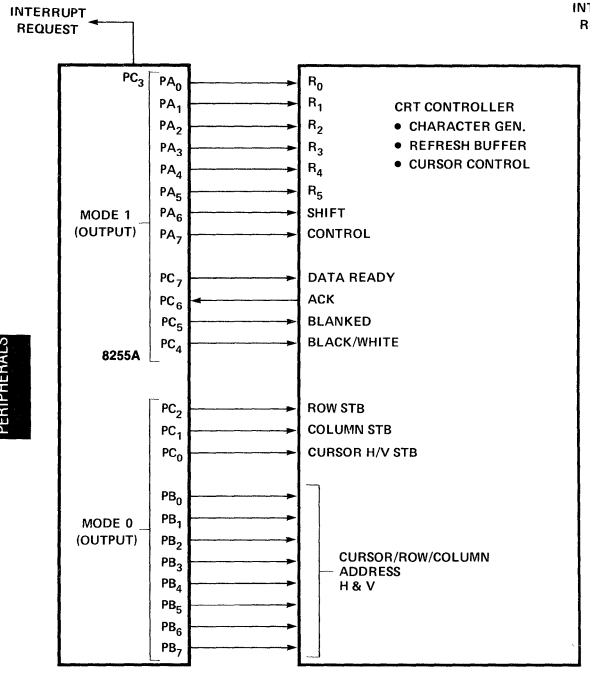


Figure 21. Basic CRT Controller Interface

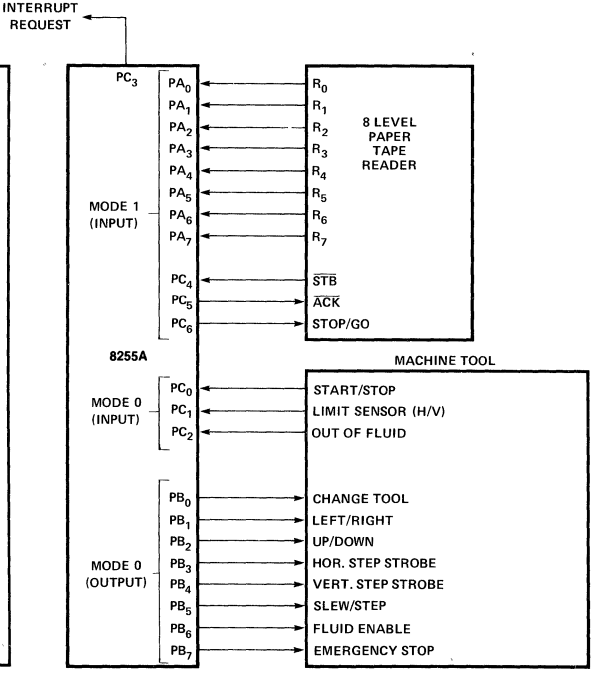


Figure 23. Machine Tool Controller Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%; GND = 0V

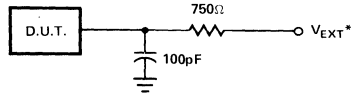
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45	V	I_{OL} = 2.5mA
V_{OL}(PER)	Output Low Voltage (Peripheral Port)		0.45	V	I_{OL} = 1.7mA
V_{OH}(DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH}(PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = -200μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	R_{EXT} = 750Ω; V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V

Note 1: Available on any 8 pins from Port B and C.

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND



*V_{EXT} is set at various voltages during testing to guarantee the specification.

Figure 24. Test Load Circuit (for dB)

A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = +5V ±5%; GND = 0V

NOTE: The 8255A-5 specifications are not final. Some parametric limits are subject to change.

Bus Parameters

Read:

SYMBOL	PARAMETER	8255A MIN.	8255A MAX.	8255A-5 MIN.	8255A-5 MAX.	UNIT
t_{AR}	Address Stable Before READ	0		0		ns
t_{RA}	Address Stable After READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid From READ[1]		250		200	ns
t_{DF}	Data Float After READ	10	150	10	100	ns
t_{RV}	Time Between READs and/or WRITEs	850		850		ns

Write:

SYMBOL	PARAMETER	8255A MIN.	8255A MAX.	8255A-5 MIN.	8255A-5 MAX.	UNIT
t_{AW}	Address Stable Before WRITE	0		0		ns
t_{WA}	Address Stable After WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid After WRITE	30		30		ns

Other Timings:

SYMBOL	PARAMETER	8255A MIN.	8255A MAX.	8255A-5 MIN.	8255A-5 MAX.	UNIT
t_{WB}	WR = 1 to Output[1]		350		350	ns
t_{IR}	Peripheral Data Before RD	0		0		ns
t_{HR}	Peripheral Data After RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data Before T.E. of STB	0		0		ns
t_{PH}	Per. Data After T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output[1]		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		300		300	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350		350	ns
t_{WIT}	WR = 0 to INTR = 0[1]		850		850	ns

Notes: 1. Test Conditions: 8255A: C_L = 100pF; 8255A-5: C_L = 150pF.
2. Period of Reset pulse must be at least 50μs during or after power on. Subsequent Reset pulse can be 500 ns min.

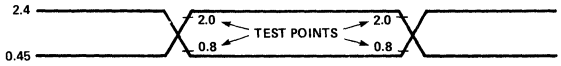


Figure 25. Input Waveforms for A.C. Tests

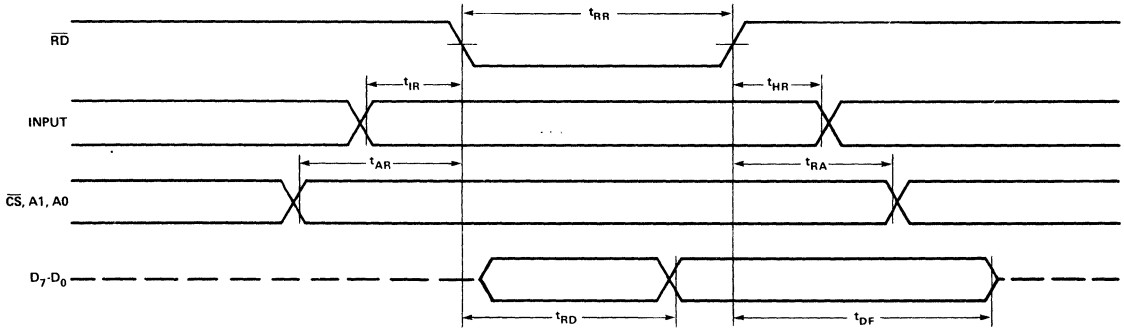


Figure 26. MODE 0 (Basic Input)

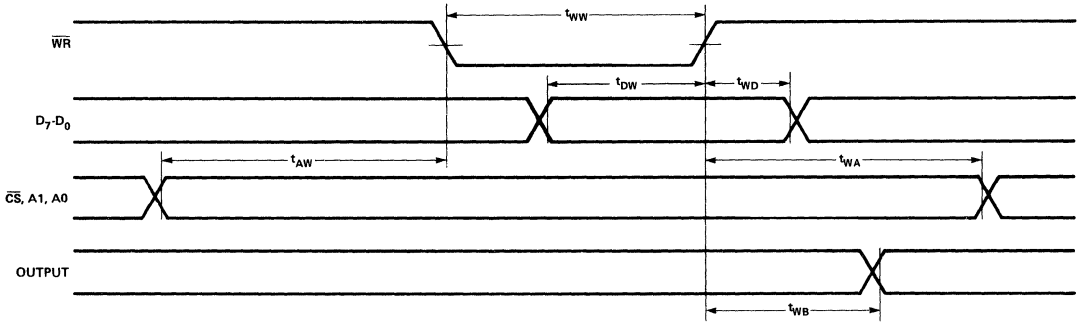


Figure 27. MODE 0 (Basic Output)

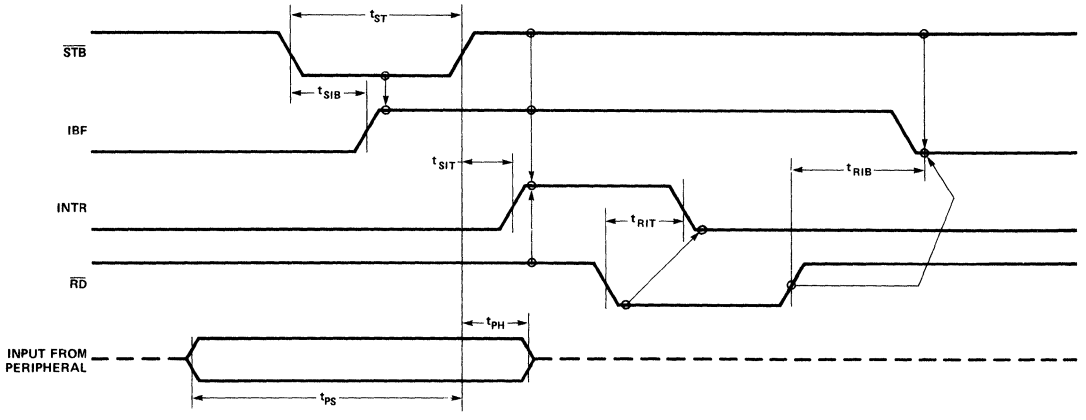


Figure 28. MODE 1 (Strobed Inut)

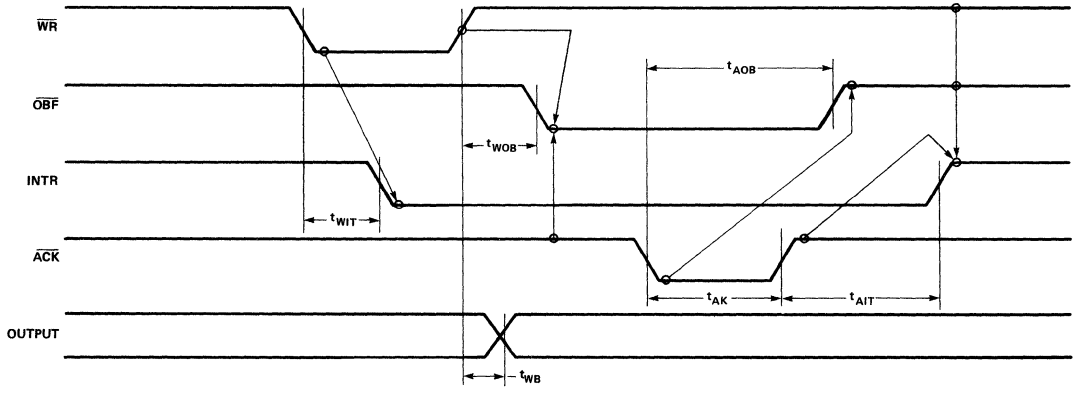


Figure 29. MODE 1 (Strobed Output)

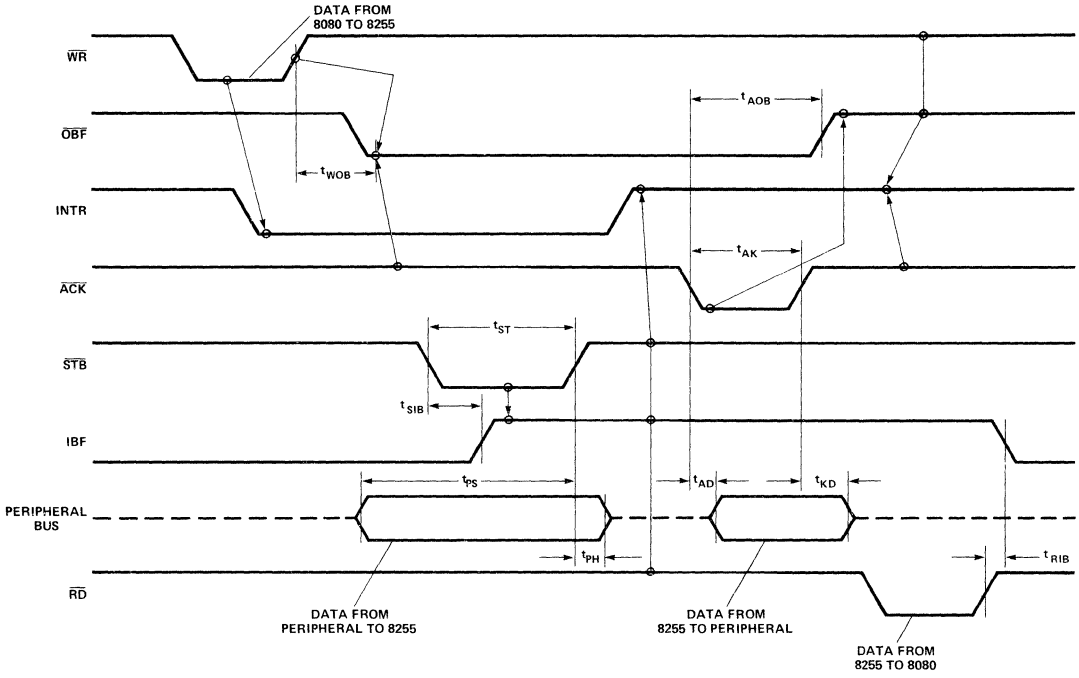


Figure 30. MODE 2 (Bidirectional)

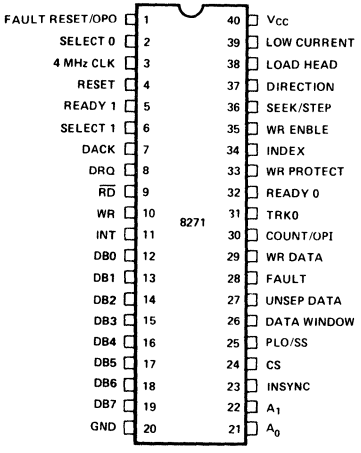
NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

8271
PROGRAMMABLE FLOPPY DISK CONTROLLER

- **IBM 3740 Soft Sectored Format Compatible**
- **Programmable Record Lengths**
- **Multi-Sector Capability**
- **Maintain Dual Drives with Minimum Software Overhead Expandable to 4 Drives**
- **Automatic Read/Write Head Positioning and Verification**
- **Internal CRC Generation and Checking**
- **Programmable Step Rate, Settle-Time, Head Load Time, Head Unload Index Count**
- **Fully MCS-80 and MCS-85 Compatible**
- **Single +5V Supply**
- **40-Pin Package**

The Intel® 8271 Programmable Floppy Disk Controller (FDC) is an LSI component designed to interface one to 4 floppy disk drives to an 8-bit microcomputer system. Its powerful control functions minimize both hardware and software overhead normally associated with floppy disk controllers.

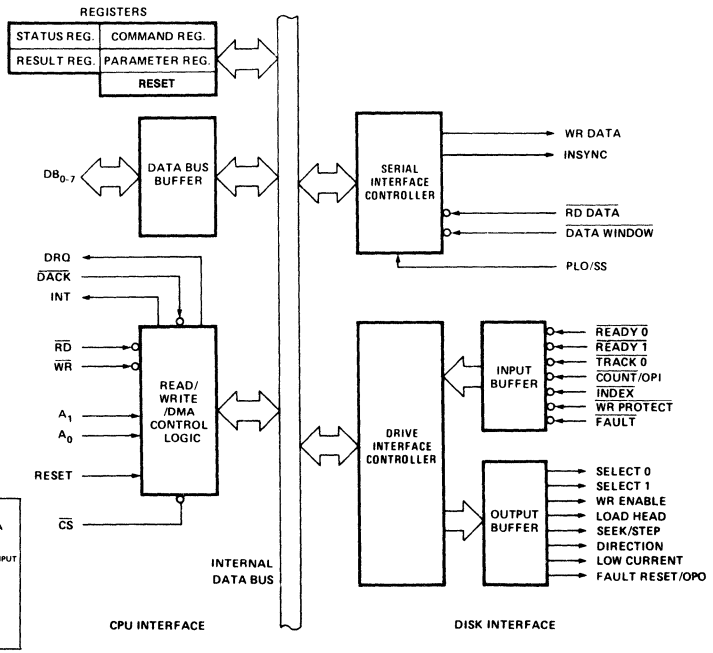
PIN CONFIGURATION



PIN NAMES

$DB_7 - DB_0$	DATA BUS (BI DIRECTIONAL)	PLO/SS	PLO/SINGLE SHOT
CLK	CLOCK INPUT (TTL)	DATA WINDOW	DATA WINDOW
SELECT 1, 0	SELECT 1, 0	UNSEP DATA	UNSEPARATED DATA
FAULT RESET/OPO	FAULT RESET/OPTIONAL OUTPUT	FAULT	FAULT
RESET	CHIP RESET	WR DATA	WRITE DATA
READY 1, 0	READY 1, 0	COUNT/OPI	COUNT/OPTIONAL INPUT
DACK	DMA ACKNOWLEDGE	TRK 0	TRACK 0
DRQ	DMA REQUEST	WR PROTECT	WRITE PROTECT
RD	CPU READ INPUT	INDEX	INDEX
WR	CPU WRITE INPUT	WR ENABLE	WRITE ENABLE
INT	INTERRUPT	SEEK/STEP	SEEK/STEP
$A_{1,0}$	REGISTER SELECT	DIRECTION	DIRECTION
INSYNC	READ DATA INSYNC	LOAD HEAD	LOAD HEAD
CS	CHIP SELECT	LOW CURRENT	LOW CURRENT

BLOCK DIAGRAM



MPU PERIPHERALS

8271 BASIC FUNCTIONAL DESCRIPTION

General

The 8271 Floppy Disk Controller (FDC) interfaces either two single or one dual floppy drive to an eight bit microprocessor and is fully compatible with Intel's new high performance MCS-85 microcomputer system. With minimum external circuitry, this innovative controller supports most standard, commonly-available flexible disk drives including the mini-floppy.

The 8271 FDC supports a comprehensive soft sectored format which is IBM 3740 compatible and includes provision for the designating and handling of bad tracks. It is a high level controller that relieves the CPU (and user) of many of the control tasks associated with implementing a floppy disk interface. The FDC supports a variety of high level instructions which allow the user to store and retrieve data on a floppy disk without dealing with the low level details of disk operation.

In addition to the standard read/write commands, a scan command is supported. The scan command allows the user program to specify a data pattern and instructs the FDC to search for that pattern on a track. Any application that is required to search the disk for information (such as point of sale price lookup, disk directory search, etc.), may use the scan command to reduce the CPU overhead. Once the scan operation is initiated, no CPU intervention is required.

Hardware Description

The 8271 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name	Pin No.	I/O	Description
V_{CC}	(40)		+5V supply
GND	(20)		Ground
Clock	(3)	I	A square wave clock
Reset	(4)	I	A high signal on the reset input forces the 8271 to an idle state. The 8271 remains idle until a command is issued by the CPU. The output signals of the drive interface are forced inactive (LOW). Reset must be active for 10 or more clock cycles.
$\overline{CS}$	(24)	I	The I/O Read and I/O Write inputs are enabled by the chip select signal.
DB_7-DB_0	(19-12)	I/O	The Data Bus lines are bidirectional, three-state lines (8080 data bus compatible).
$\overline{WR}$	(10)	I	The Write signal is used to signal the control logic that a transfer of data from the data bus to the 8271 is required.
$\overline{RD}$	(9)	I	The Read signal is used to signal the control logic that a transfer of data from the 8271 to the data bus is required.
INT	(11)	O	The interrupt signal indicates that the 8271 requires service.
A_1-A_0	(22-21)	I	These two lines are CPU interface Register select lines.
DRQ	(8)	O	The DMA request signal is used to request a transfer of data between the 8271 and memory.
$\overline{DACK}$	(7)	I	The DMA acknowledge signal notifies the 8271 that a DMA cycle has been granted. For non-DMA transfers, this signal should be driven in the manner of a "Chip Select".
Select 1- Select 0	(6) (2)	O	These lines are used to specify the selected drive. These lines are set by the command byte.
Fault Reset/ OPO	(1)	O	The optional fault reset output line is used to reset an error condition which is latched by the drive. If this line is not used for a fault reset it can be used as an optional output line. This line is set with the write special register command.
Write Enable	(35)	O	This signal enables the drive write logic.
Seek/Step	(36)	O	This multi-function line is used during drive seeks.
Direction	(37)	O	The direction line specifies the seek direction. A high level on this pin steps the R/W head toward the spindle (step-in), a low level steps the head away from the spindle (step-out).
Load Head	(38)	O	The load head line causes the drive to load the Read/Write head against the diskette.
Low Current	(39)	O	This line notifies the drive that track 43 or greater is selected.
$\overline{Ready\ 1}$, $\overline{Ready\ 0}$	(5) (32)	I	These two lines indicate that the specified drive is ready.
$\overline{Fault}$	(28)	I	This line is used by the drive to specify a file unsafe condition.
$\overline{Count/OPI}$	(30)	I	If the optional seek/direction/count seek mode is selected, the count pin receives pulses to step the R/W head to the desired track. Otherwise, this line can be used as an optional input.
$\overline{Write\ Protect}$	(33)	I	This signal specifies that the diskette inserted is write protected.
$\overline{TRK0}$	(31)	I	This signal indicates when the R/W head is positioned over track zero.
$\overline{Index}$	(34)	I	The index signal gives an indication of the relative position of the diskette.
PLO/SS	(25)	I	This pin is used to specify the type of data separator used. Phase-Locked Oscillator/Single Shot.
Write Data	(29)	O	Composite write data.

Pin Name	Pin No.	I/O	Description
$\overline{\text{Unseparated}}$ $\overline{\text{Data}}$	(27)	I	This input is the unseparated data and clocks.
$\overline{\text{Data Window}}$	(26)	I	This is a data window established by a single-shot or phase-locked oscillator data separator.
INSYNC	(23)	O	This line is high when 8271 has attained input data synchronization, by detecting 2 bytes of zeros followed by an expected Address Mark. It will stay high until the end of the ID or data field.

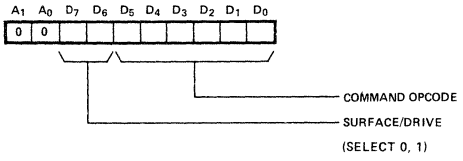
CPU Interface Description

This interface minimizes CPU involvement by supporting a set of high level commands and both DMA and non-DMA type data transfers and by providing hierarchical status information regarding the result of command execution.

The CPU utilizes the control interface (see the Block diagram) to specify the FDC commands and to determine the result of an executed command. This interface is supported by five Registers which are addressed by the CPU via the A_1, A_0, $\overline{RD}$ and $\overline{WR}$ signals. If an 8080 based system is used, the $\overline{RD}$ and $\overline{WR}$ signals can be driven by the 8228's $\overline{I/OR}$ and $\overline{I/OW}$ signals. The registers are defined as follows:

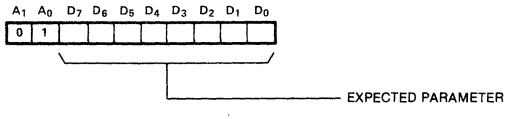
Command Register

The CPU loads an appropriate command into the Command Register which has the following format:



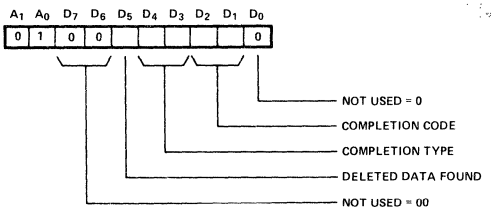
Parameter Register

Accepts parameters of commands that require further description; up to five parameters may be required, example:



Result Register

The Result Register is used to supply the outcome of FDC command execution (such as a good/bad completion) to the CPU. The standard Result byte format is:



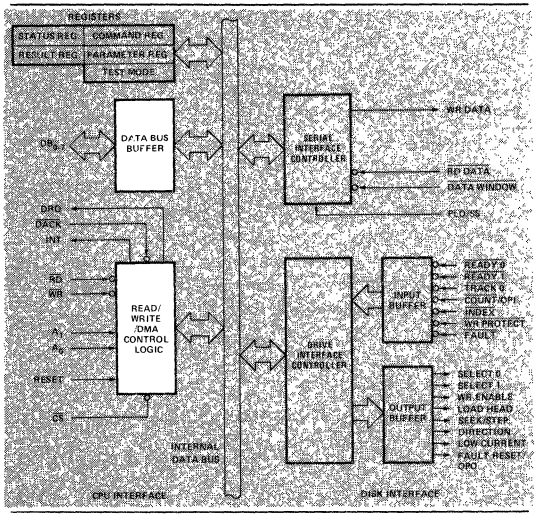
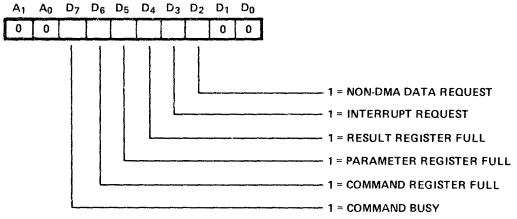


Figure 1. 8271 Block Diagram Showing CPU Interface Functions

Status Register

Reflects the state of the FDC.



Reset Register

Allows the 8271 to be reset by the program. Reset must be active for 11 or more chip clocks.

INT (Interrupt Line)

Another element of the control interface is the Interrupt line (INT). This line is used to signal the CPU that an FDC operation has been completed. It remains active until the result register is read.

DMA Operation

The 8271 can transfer data in either DMA or non DMA mode. The data transfer rate of a floppy disk drive is high enough (one byte every 32 μsec) to justify DMA transfer. In DMA mode the elements of the DMA interface are:

DRQ: DMA Request:
The DMA request signal is used to request a transfer of data between the 8271 and memory.

$\overline{\text{DACK}}$: DMA Acknowledge:
The DMA acknowledge signal notifies the 8271 that a DMA cycle has been granted.

$\overline{\text{RD}}$, $\overline{\text{WR}}$: Read, Write
The read and write signals are used to specify the direction of the data transfer.

DMA transfers require the use of a DMA controller such as the Intel®8257. The function of the DMA controller is to provide sequential addresses and timing for the transfer at a starting address determined by the CPU. Counting of data block lengths is performed by the FDC.

To request a DMA transfer, the FDC raises DRQ. DACK and RD enable DMA data onto the bus (independently of CHIP SELECT). DACK and WR transfer DMA data to the FDC. If a data transfer request (read or write) is not serviced within 31 μsec, the command is cancelled, a late DMA status is set, and an interrupt is generated. In DMA mode, an interrupt is generated at the completion of the data block transfer.

When configured to transfer data in non-DMA mode, the CPU must pass data to the FDC in response to the non-DMA data requests indicated by the status word. The data is passed to and from the chip by asserting the DACK and the RD or WR signals. Chip select should be inactive (HIGH).

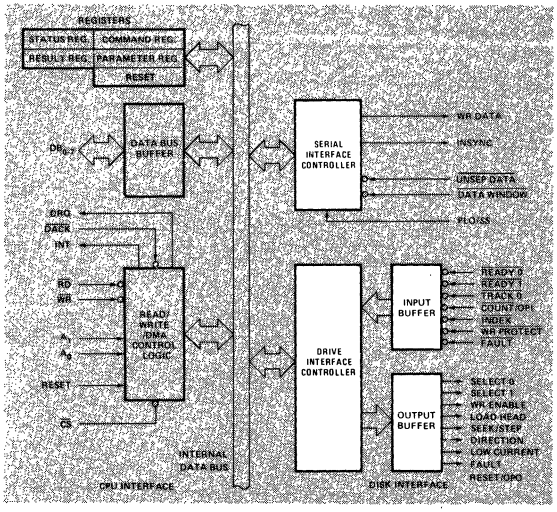


Figure 2. 8271 Block Diagram Showing Disk Interface Functions

Disk Drive Interface

The 8271 disk drive interface supports the high level command structure described in the Command Description section. The 8271 maintains the location of bad tracks and the current track location for two drives. However, with minor software support, this interface can support four drives by expanding the two drive select lines (select 0, select 1) with the addition of minimal support hardware.

The FDC Disk Drive Interface has the following major functions.

READ FUNCTIONS

Utilize the user supplied data window to obtain the clock and data patterns from the unseparated read data.

Establish byte synchronization.

Compute and verify the ID and data field CRCs.

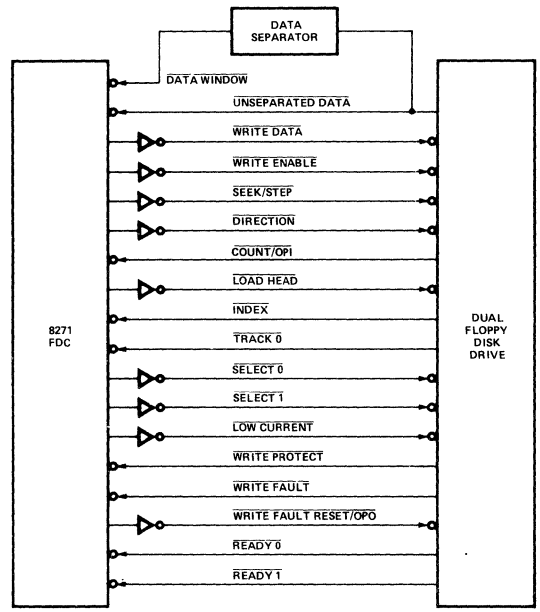
WRITE FUNCTIONS

Encode composite write data.

Compute the ID and data field CRCs and append them to their respective fields.

CONTROL FUNCTIONS

Generate the programmed step rate, head load time, head settling time, head unload delay, and monitor drive functions.



NOTE: INPUTS TO CHIP MAY REQUIRE RECEIVERS (AT LEAST PULL UP/DOWN PAIRS).

Figure 3. 8271 Disk Drive Interface

Data Separation

The 8271 needs only a data window to separate the data from the composite read data as well as to detect missing clocks in the Address Marks.

The window generation logic may be implemented using either a single-shot separator or a phase-locked oscillator.

Single-Shot Separator

The single-shot separator approach is the lowest cost solution.

The FDC samples the value of Data Window on the leading edge of Unseparated Data and determines whether the delay from the previous pulse was a half or full bit-cell (high input = full bit-cell, low input = half bit-cell).
PLO/SS should be tied to Ground.

Insync Pin

This pin gives an indication of whether the 8271 is synchronized with the serial data stream during read operations. This pin can be used with a phase-locked oscillator for soft and hard locking.

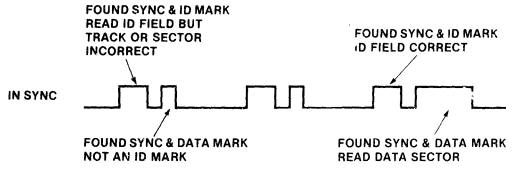
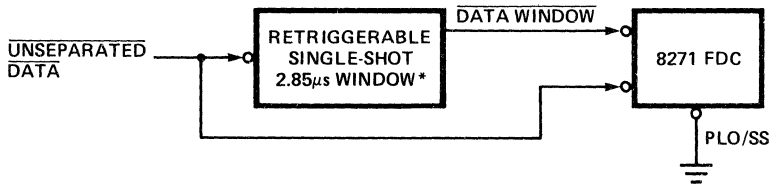


Figure 4. Insync Waveform



*FOR MINI-FLOPPY DATA WINDOW = 5.7μsec

Figure 5. Single-Shot Data Separator Block Diagram

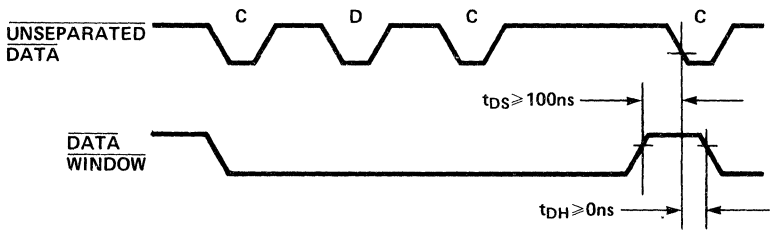


Figure 6. Single-Shot Data Window Timing

Phase-Locked Oscillator Separator

The FDC samples the value of Data Window on the leading edge of Unseparated Data and determines whether the pulse represents a Clock or Data Pulse.

PLO/SS should be tied to V_{CC} (+5V).

Insync may be used to provide soft and hard locking control for the phase-locked oscillator.

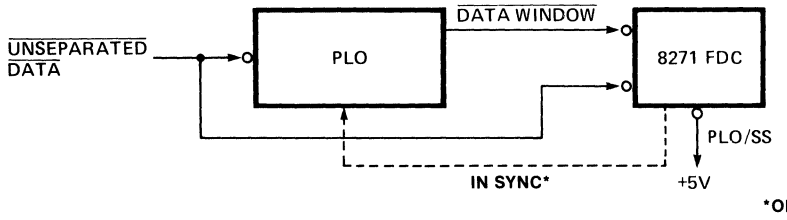
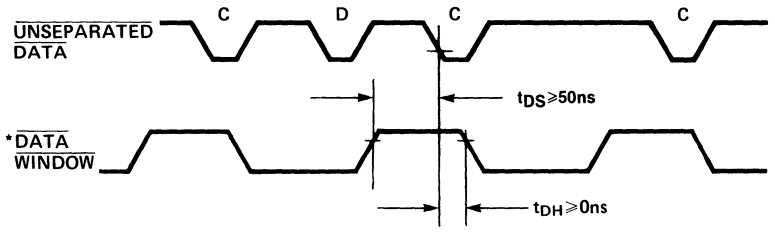


Figure 7. PLO Data Separator Block Diagram



*DATA WINDOW MAY BE 180° OUT OF PHASE IN PLO DATA SEPARATION MODE.

Figure 8. PLO Data Window Timing

Disk Drive Control Interface

The disk drive control interface performs the high level and programmable flexible disk drive operations. It custom tailors many varied drive performance parameters such as the step rate, settling time, head load time, and head unload index count. The following is the description of the control interface.

Write Enable

The Write Enable controls the read and write functions of a flexible disk drive. When Write Enable is a logical one, it enables the drive write electronics to pass current through the Read/Write head. When Write Enable is a logical zero, the drive Write circuitry is disabled and the Read/Write head detects the magnetic flux transitions recorded on a diskette. The write current turn-on is as follows.

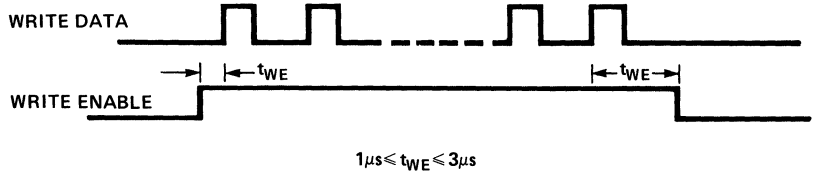


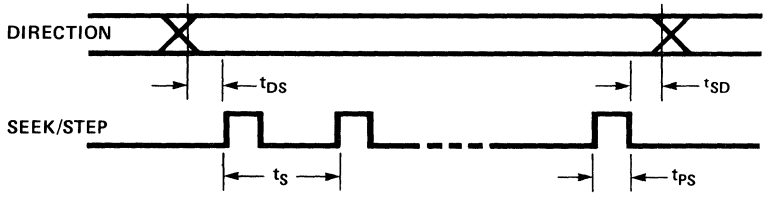
Figure 9. Write Enable Timing

Seek Control

Seek Control is accomplished by Seek/Step, Direction, and Count pins and can be implemented two ways to provide maximum flexibility in the subsystem design. One instance is when the programmed step rate is not equal to zero. In this case, the 8271 uses the Seek/Step and Direction pins (the Seek/Step pin becomes a Step pin). Programmable Step timing parameters are shown.

Another instance is when the programmable step rate is equal to zero, in which case the 8271 holds the seek line high until the appropriate number of user-supplied step pulses have been counted on the count input pin.

The Direction pin is a control level indicating the direction in which the R/W head is stepped. A logic high level on this line moves the head toward the spindle (step-in). A logic low level moves the head away from the spindle (step-out).

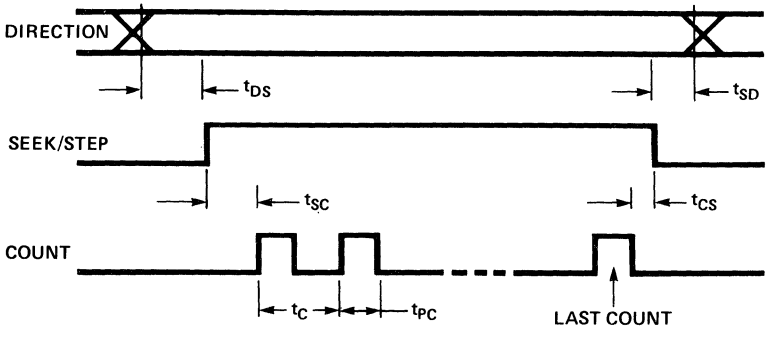


$t_{PS}=t_{DS}=t_{SD}=10\mu s$

STANDARD: $1ms \leq t_S \leq 255ms$

MINI-FLOPPY: $2ms \leq t_s \leq 510ms$

Figure 10. Seek Timing



$t_{DS}=t_{SD}=t_{CS}=10\mu s$

$t_{SC} \geq 1\mu s$

$t_{PC} \geq 20\mu s$

$t_C \geq 1ms$

Figure 11. Seek/Step/Count Timing

Head Seek Settling Time

The 8271 allows the head settling time to be programmed from 0 to 255ms, in increments of 1ms.

The head settling time is defined as the interval of time from completion of the last step to the time when reading or writing on the diskette is possible (R/W Enable). The R/W head is assumed loaded.

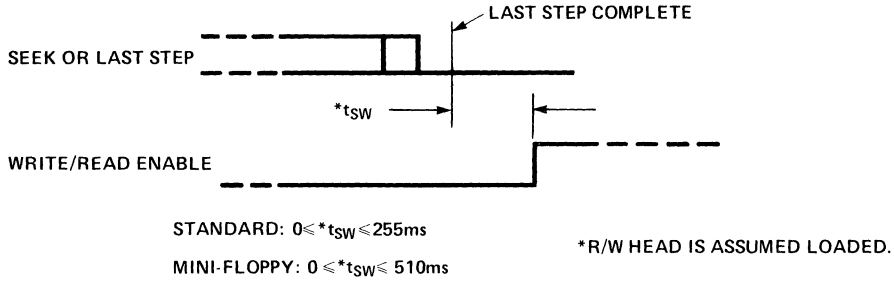


Figure 12. Head Load Settling Timing

Load Head

When active, load head output pin causes the drive's read/write head to be loaded on the diskette. When the head is initially loaded, there is a programmed delay (0 to 60ms in 4ms increments) prior to any read or write operation. Provision is also made to unload the head following an operation within a programmed number of diskette revolutions.

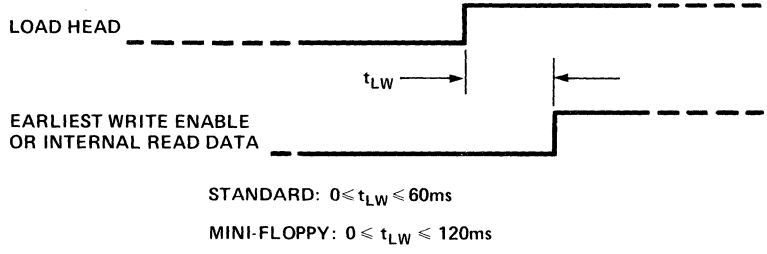


Figure 13. Head Load to Read/Write Timing

Index

The Index input is used to determine "Sector not found" status and to initiate format track/read ID commands and head unload Index and Count operations.

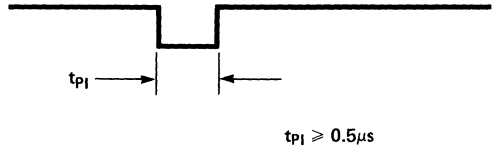


Figure 14. Index Timing

Track 0

This input pin indicates that the diskette is at track 0. During any seek operation, the stepping out of the actuator ceases when the track 0 pin becomes active.

Select 1, 0

Only one drive may be selected at a time. The Input/Output pins that must be externally qualified with Select 0 and Select 1 are:

Unseparated Data
Data Window
Write Enable
Seek/Step
Count/Optional Input
Load Head
Track 0
Low Current
Write Protect
Write Fault
Fault Reset/Optional Output
Index

When a new set of select bits is specified by a new command or the FDC finishes the index count before head unload, the following pins will be set to the 0 state:

Write Enable (35)
Seek/Step (36)
Direction (37)
Load Head (38)
Low Head Current (39)

The select pins will be set to the state specified by the command or both are set to zero following the index count before head unload.

Low Current

This output pin is active whenever the physical track location of the selected drive is greater than 43. Generally this signal is used to enable compensation for the lower velocities encountered while recording on the inner tracks.

Write Protect

The 8271 will not write to a disk when this input pin is active and will interrupt the CPU if a Write attempt is made. Operations which check Write Protect are aborted if the Write Protect line is active.

This signal normally originates from a sensor which detects the presence or absence of the Write Protect hole in the diskette jacket.

Write Fault and Write Fault Reset

The Write Fault input is normally latched by the drive and indicates any condition which could endanger data integrity. The 8271 interrupts the CPU anytime Write Fault is detected during an operation and immediately resets the Write Enable, Seek/Step, Direction, and Low Current signals. The write fault condition can be cleared by using the write fault reset pin. If the drive being used does not support write fault, then this pin should be connected to V_{CC} through a pull-up resistor.

Ready 1, 0

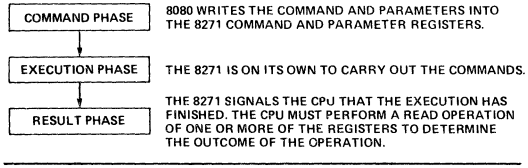
These two pins indicate the functional status of the disk drives. Whenever an operation is attempted on a drive which is not ready, an interrupt is generated. The interface continually monitors this input during an operation and if a Not Ready condition occurs, immediately terminates the operation. Note that the 8271 latches the Not Ready condition and it can only be reset by the execution of a Read Drive Status command. For drives that do not support a ready signal, either one can be derived with a one shot and the index pulse, or the ready inputs can be grounded and Ready determined through some software means.

PRINCIPLES OF OPERATION

As an 8080 peripheral device, the 8271 accepts commands from the CPU, executes them and provides a RESULT back to the 8080 CPU at the end of command execution. The communication with the CPU is established by the activation of $\overline{CS}$ and $\overline{RD}$ or $\overline{WR}$. The A_1, A_0 inputs select the appropriate registers on the chip:

$\overline{DACK}$	$\overline{CS}$	A_1	A_0	$\overline{RD}$	$\overline{WR}$	Operation
1	0	0	0	0	1	Read Status
1	0	0	0	1	0	Write Command
1	0	0	1	0	1	Read Result
1	0	0	1	1	0	Write Parameter
1	0	1	0	1	0	Write Reset Reg.
0	1	X	X	1	0	Write Data
0	1	X	X	0	1	Read Data
0	0	X	X	X	X	Not Allowed

The FDC operation is composed of the following sequence of events.



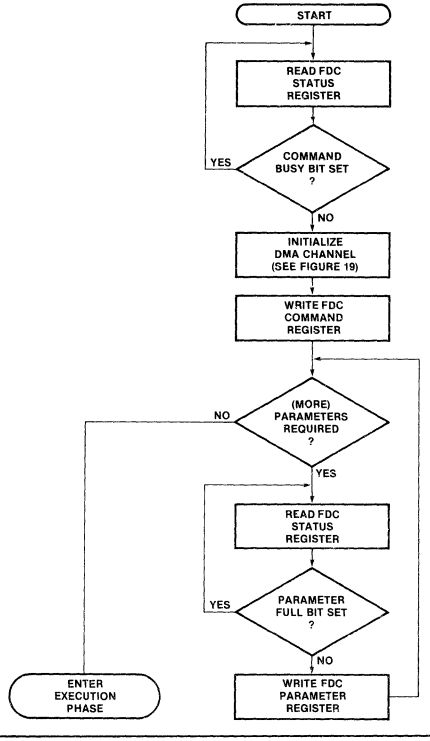
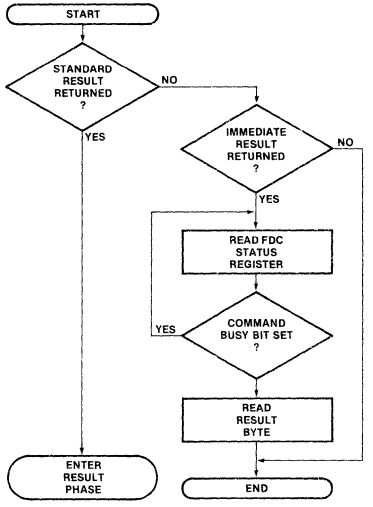


Figure 15. Passing the Command and Parameters to the 8271

The Command Phase

The software writes a command to the command register. As a function of the command issued, from zero to five parameters are written to the parameter register. Refer to diagram showing a flow chart of the command phase. Note that the flow chart shows that a command may not be issued if the FDC status register indicates that the device is busy. Issuing a command while another command is in progress is illegal. The flow chart also shows a parameter buffer full check. The FDC status indicates the state of the parameter buffer. If a parameter is issued while the parameter buffer is full, the previous parameter is over written and lost.



NOTE:

STANDARD RESULT RETURNED CAN BE DETERMINED BY MASKING OUT THE DRIVE SELECT BITS OF THE COMMAND BYTE (BITS 7 AND 6) AND CHECKING FOR A VALUE OF LESS THAN $2C_{16}$ (IF LESS THAN $2C_{16}$, STANDARD RESULT IS RETURNED).

IMMEDIATE RESULT RETURNED CAN BE DETERMINED BY ADDITIONALLY MASKING OUT BITS 5 AND 4 OF THE COMMAND BYTE AND CHECKING FOR A VALUE OF C_{16} OR GREATER (IF C_{16} OR GREATER, IMMEDIATE RESULT RETURNED).

Figure 16. Checking for Result Type Following 8271 Command and Parameters

The Execution Phase

During the execution phase the operation specified during the command phase is performed. During this phase, there is no CPU involvement if the system utilizes DMA for the data transfers. The execution phase of each command is discussed within the detailed command descriptions. The following table summarizes many of the basic execution phase characteristics.

EXECUTION PHASE BASIC CHARACTERISTICS

The following table summarizes the various commands with corresponding execution phase characteristics.

COMMANDS	1 Deleted Data	2 Head	3 Ready	4 Write/ Protect	5 Seek	6 Seek Check	7 Result	8 Completion Interrupt
SCAN DATA	SKIP	LOAD	√	x	YES	YES	YES	YES
SCAN DATA AND DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
WRITE DATA	x	LOAD	√	√	YES	YES	YES	YES
WRITE DEL DATA	x	LOAD	√	√	YES	YES	YES	YES
READ DATA	SKIP	LOAD	√	x	YES	YES	YES	YES
READ DATA AND DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
READ ID	x	LOAD	√	x	YES	NO	YES	YES
VERIFY DATA AND DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
FORMAT TRACK	x	LOAD	√	√	YES	NO	YES	YES
SEEK	x	LOAD	y	x	YES	NO	YES	YES
READ DRIVE STATUS	x	–	x	x	NO	NO	NOTE 5	NO
SPECIFY	x	–	x	x	NO	NO	NO	NO
RESET	x	UNLOAD	x	x	NO	NO	NO	NO
R SP REGISTERS	x	–	x	x	NO	NO	NOTE 6	NO
W SP REGISTERS	x	–	x	x	NO	NO	NO	NO

Note: 1. "x" → DON'T CARE 2. "√" → check 3. "–" → No change 4. "y" → Check at end of operation 5. See "READ DRIVE STATUS" command. 6. See "READ SPECIAL REGISTER" command.

Table 1. Execution Phase Basic Characteristics

Explanation of the execution phase characteristics table.

1. Deleted Data Processing

   If deleted data is encountered during an operation that is marked skip in the table, the deleted data record is not transferred into memory, but the record is counted. For example, if the command and parameters specify a read of five records and one of the records was written with a deleted data mark, four records are transferred to memory. The deleted data flag is set in the result byte. However, if the operation is marked transfer, all data is transferred to memory regardless of the type of data mark.

2. Head

   The Head column in the table specifies whether the Read/Write head will be loaded or not. If the table specifies load, the head is loaded after it is positioned over the track. The head loaded by a command remains loaded until the user specified number of index pulses have occurred.

3. Ready

   The Ready column indicates if the ready line (Ready 1, Ready 0) associated with the selected drive is checked. A not ready state is latched by the 8271 until the user executes a read status command.

4. Write Protect

   The operations that are marked check Write Protect are immediately aborted if Write Protect line is active at the beginning of an operation.

5. Seek

   Many of the 8271 commands cause a seek to the desired track. A current track register is maintained for each drive or surface.

6. Seek Check

   Operations that perform Seek Check verify that selected data in the ID field is correct before the 8271 accesses the data field.

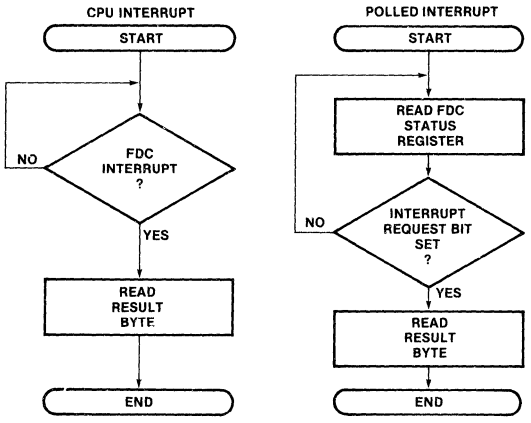


Figure 17. Getting the Result

The Result Phase

During the Result Phase, the FDC notifies the CPU of the outcome of the command execution. This phase may be initiated by:

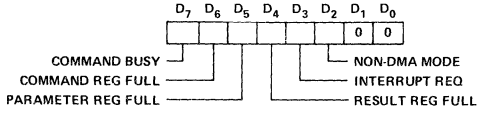
1. The successful completion of an operation.
2. An error detected during an operation.

PROGRAMMING

A_1	A_0	CS RD	CS WR
0	0	Status Reg	Command Reg
0	1	Result Reg	Parameter Reg
1	0	—	Reset Reg
1	1	—	—

STATUS REGISTER

FDC Status



Bit 7: Command Busy

The command busy bit is set on writing to the command register. Whenever the FDC is busy processing a command, the command busy bit is set to a one. This bit is set to zero after the command is completed.

Bit 6: Command Full

The command full bit is set on writing to the command buffer and cleared when the FDC begins processing the command.

Bit 5: Parameter Full

This bit indicates the state of the parameter buffer. This bit is set when a parameter is written to the FDC and reset after the FDC has accepted the parameter.

Bit 4: Result Full

This bit indicates the state of the result buffer. It is valid only after Command Busy bit is low. This bit is set when the FDC finishes a command and is reset after the result byte is read by the CPU. The data in the result buffer is valid only after the FDC has completed a command. Reading the result buffer while a command is in progress yields no useful information.

Bit 3: Interrupt Request

This bit reflects the state of the FDC INT pin. It is set when FDC requests attention as a result of the completion of an operation or failure to complete an intended operation. This bit is cleared by reading the result register.

Bit 2: Non-DMA Data Request

When the FDC is utilized without a DMA controller, this bit is used to indicate FDC data requests. Note that in the non-DMA mode, an interrupt is generated (interrupt request bit is set) with each data byte written to or read from the diskette.

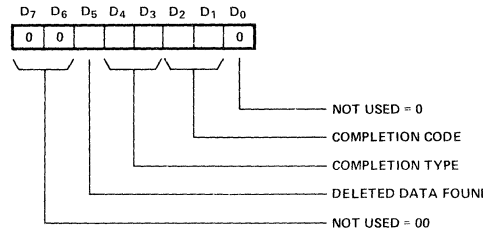
Bits 1 and 0:

Not used (zero returned).

After reading the Status Register, the CPU then reads the Result Register for more information.

THE RESULT REGISTER

This byte format facilitates the use of an address table to look up error routines and messages. The standard result byte format is:



Bits 7 and 6:

Not used (zero returned).

Bit 5:

Deleted Data Found: This bit is set when deleted data is encountered during a transaction.

Bits 4 and 3: Completion Type

The completion type field provides general information regarding the outcome of an operation.

The completion type field provides general information regarding the outcome of an operation.

Completion Type	Event
00	Good Completion — No Error
01	System Error — recoverable errors;
10	operator intervention probably required for recovery.
11	Command/Drive Error — either a program error or drive hardware failure.

Bits 2 and 1: Completion Code

The completion code field provides more detailed information about the completion type (See Table).

Completion Type	Completion Code	Event
00	00	Good Completion/ Scan Not Met
00	01	Scan Met Equal
00	10	Scan Met Not Equal
00	11	—
01	00	Clock Error
01	01	Late DMA
01	10	ID CRC Error
01	11	Data CRC Error
10	00	Drive Not Ready
10	01	Write Protect
10	10	Track 0 Not Found
10	11	Write Fault
11	00	Sector Not Found
11	01	—
11	10	—
11	11	—

It is important to note the hierarchical structure of the result byte. In very simple systems where only a GO-NO GO result is required, the user may simply branch on a zero result (a zero result is a good completion). The next level of complexity is at the completion type interface. The completion type supplies enough information so that the software may distinguish between fatal and non-fatal errors. If a completion type 01 occurs, ten retries should be performed before the error is considered unrecoverable.

The Completion Type/Completion Code interface supplies the greatest detail about each type of completion. This interface is used when detailed information about the transaction completion is required.

Bit 0:

Not used (zero returned).

Definition	Interpretation
Successful Completion/ Scan Not Met	The diskette operation specified was completed without error. If scan operation was specified, the pattern scanned was not found on the track addressed.
Scan Met Equal	The data pattern specified with the scan command was found on the track addressed with the specified comparison, and the equality was met.
Scan Met Not Equal	The data pattern specified with the scan command was found with the specified comparison on the track addressed, but the equality was not met.
Clock Error	During a diskette read operation, a clock bit was missing (dropped). Note that this function is disabled when reading any of the ID address marks (which contain missing clock pulses). If this error occurs, the operation is terminated immediately and an interrupt is generated.
Late DMA	During either a diskette read or write operation, the data channel did not respond within the allotted time interval to prevent data from being overwritten or lost. This error immediately terminates the operation and generates an interrupt.
ID Field CRC Error	The CRC word (two bytes) derived from the data read in an ID field did not match the CRC word written in the ID field when the track was formatted. If this error occurs, the associated diskette operation is prevented and no data is transferred.
Data Field CRC Error	During a diskette read operation, the CRC word derived from the data field read did not match the data field CRC word previously written. If this error occurs, the data read from the sector should be considered invalid.
Drive Not Ready	The drive addressed was not ready. This indication is caused by any of the following conditions: 1. Drive not powered up 2. Diskette not loaded 3. Non-existent drive addressed 4. Drive went not ready during an operation Note that this completion code is cleared only through an FDC read drive status command.
Write Protect	A diskette write operation was specified on a write protected diskette. The intended write operation is prevented and no data is written on the diskette.
Track 00 Not Found	During a seek to track 00 operation, the drive failed to provide a track 00 indication after being stepped 255 times.
Write Fault	This error is dependent on the drive supported and indicates that the fault input to the FDC has been activated by the drive.
Sector Not Found	Either the sector addressed could not be found within one complete revolution of the diskette (two index marks encountered) or the track address specified did not match the track address contained in the ID field. Note that when the track address specified and the track address read do not match, the FDC automatically increments its track address register (stepping the drive to the next track) and again compares the track addresses. If the track addresses still do not match, the track address register is incremented a second time and another comparison is made before the sector not found completion code is set.

Table 2. Completion Code Interpretation

INITIALIZATION

Reset Command

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
PAR:	1	0	0	0	0	0	0	0	0	1
PAR:	1	0	0	0	0	0	0	0	0	0

Function: The Reset command emulates the action of the reset pin. It is issued by outputting a one followed by a zero to the Reset register.

1. The drive control signals are forced low.
2. An in-progress command is aborted.
3. The FDC status register flags are cleared.
4. The FDC enters an idle state until the next command is issued.

Reset must be active for 10 or more clock cycles.

SPECIFY COMMAND

Many of the interface characteristics of the FDC are specified by the systems software. Prior to initiating any drive operation command, the software must execute the three specify commands. There are two types of specify commands selectable by the first parameter issued.

First Parameter	Specify Type
$0D_H$	Initialization
10_H	Load bad Tracks Surface '0'
18_H	Load bad Tracks Surface '1'

The Specify command is used prior to performing any diskette operation (including formatting of a diskette) to define the drive's inherent operating characteristics and also is used following a formatting operation or installation of another diskette to define the locations of bad tracks. Since the Specify command only loads internal registers within the 8271 and does not involve an actual diskette operation, command processing is limited to only Command Phase. Note that once the operating characteristics and bad tracks have been specified for a given drive and diskette, redefining these values need only be done if a diskette with unique bad tracks is to be used or if the system is powered down.

Initialization:

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	0	1	1	0	1	0	1
PAR:	0	1	0	0	0	0	1	1	0	1
PAR:	0	1	STEP RATE*							
PAR:	0	1	HEAD SETTLING TIME*							
PAR:	0	1	INDEX CNT BEFORE HEAD UNLOAD*				HEAD LOAD TIME*			

*Note: Mini-floppy parameters are doubled.

Parameter 0 — $0D_H$ = Select Specify Initialization.
Parameter 1 — D_7-D_0 = Step Rate (0-255ms in 1ms steps).
Parameter 2 — D_7-D_0 = Head Settling Time (0-255ms in 1 ms steps). {0 – 510ms in 2ms steps} () = standard, {} = mini

Parameter 3 — D_7-D_4 = Index Count — Specifies the number of Revolutions (0-14) which are to occur before the FDC automatically unloads the R/W head. If 15 is specified, the head remains loaded.

D_3-D_0 = Head Load Time (0-60ms in steps of 4ms). {0 – 120ms in 8ms steps} () = standard, {} = mini

Load Bad Tracks

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	0	1	1	0	1	0	1
PAR:	0	1	0	0	0	1	1/0	0	0	0
PAR:	0	1	BAD TRACK NO. 1							
PAR:	0	1	BAD TRACK NO. 2							
PAR:	0	1	CURRENT TRACK							

Parameter 0: 10_H = Load Surface zero bad tracks
18_H = Load Surface one bad track

Parameter 1:
Bad track address number 1 (Physical Address).

It is recommended to program both bad tracks and current track to FF_H during initialization.

SEEK COMMAND

The seek command moves the head to the specified track without loading the head or verifying the track.

The seek operation uses the specified bad tracks to compute the physical track address. This feature insures that the seek operation positions the head over the correct track.

When a seek to track zero is specified, the FDC steps the head until the track 00 signal is detected.

If the track 00 signal is not detected within $(FF)_H$ steps, a track 0 not found error status is returned.

A seek to track zero is used to position the read/write head when the current head position is unknown (such as after a power up).

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	SEL 1	SEL 0	1	0	1	0	0	1
PAR:	0	1	TRACK ADDRESS 0-255							

Seek operations are not verified. A subsequent read or write operation must be performed to determine if the correct track is located.

READ DRIVE STATUS COMMAND

This command is used to interrogate the drive status. Upon completion the result register will hold the final drive status.

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	SEL 1	SEL 0	1	0	1	1	0	0

RESULT: EACH BIT INDICATES CURRENT STATE OF INPUT PINS.

A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	—	RDY 1*	WR FAULT	INDEX	WR PROT	RDY 0*	TRACK 0	CNT. / OPI

IF A DRIVE NOT READY RESULT IS RETURNED, THE READ STATUS MUST BE ISSUED TO CLEAR THE CONDITION.

*Note the two ready bits are zero latching. Therefore, to clear the drive not ready condition, assuming the drive is ready, and to detect it via software, one must issue this command twice.

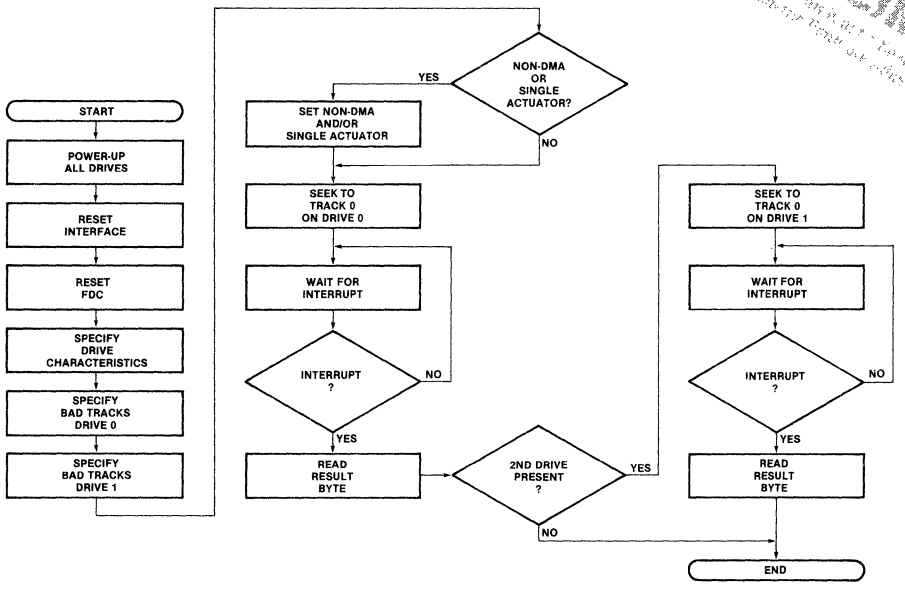


Figure 18. Initialization of the 8271 by the User

Read/Write Special Registers

This command is used to access special registers within the 8271.

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	SEL 1	SEL 0	COMMAND OPCODE					
PAR:	0	1	REGISTER ADDRESS							

Command code:

$3D_H$ Read Special Register
$3A_H$ Write Special Register

For both commands, the first parameter is the register address; for Write commands a second parameter specifies data to be written. Only the Read Special Register command supplies a result.

Description	Register Address in Hex	Comment
Scan Sector Number	06	See Scan Description
Scan MSB of Count	14	See Scan Description
Scan LSB of Count	13	See Scan Description
Surface 0 Current Track	12	
Surface 1 Current Track	1A	
Mode Register	17	See Mode Register Description
Drive Control Output Port	23	See Drive Output Port Description
Drive Control Input Port	22	See Drive Input Port Description
Surface 0 Bad Track 1	10	
Surface 0 Bad Track 2	11	
Surface 1 Bad Track 1	18	
Surface 1 Bad Track 2	19	

Table 3. Special Registers

Mode Register Write Parameter Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	0	0		

= 0 DMA MODE, = 1 NON DMA

= 0 DOUBLE, = 1 SINGLE ACTUATOR

Bits 6 & 7

Must be one.

Bits 5-2

(Not used). Must be set to zero.

***Bit 1**

Double/Single Actuator: Selects single or double actuator mode. If the single actuator mode is selected, the FDC assumes that the physical track location of both disks is always the same. This mode facilitates control of a drive which has a single actuator mechanism to move two heads.

***Bit 0**

Data Transfer Mode: This bit selects the data transfer mode. If this bit is a zero, the FDC operates in the DMA mode (DMA Request/ACK). If this bit is a one, the FDC operates in non-DMA mode. When the FDC is operating in DMA mode, interrupts are generated at the completion of commands. If the non-DMA mode is selected, the FDC generates an interrupt for every data byte transferred.

*Bits 0 and 1 are initialized to zero.

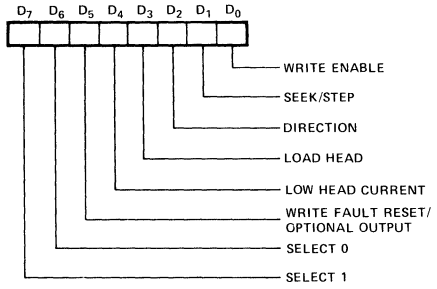
Non-DMA Transfers in DMA Mode

If the user desires, he may retain the use of interrupts generated upon command completions. This mode is accomplished by selecting the DMA capability, but using the DMA REQ/ACK pins as effective INT and CS signals, respectively.

Drive Control Input Port

Reading this port will give the CPU exactly the data that the FDC sees at the corresponding pins. Reading this port will update the drive not ready status, but will not clear the status. (See Read Drive Status Command for Bit locations.)

Drive Control Output Port Format



Each of these signals correspond to the chip pin of the same name. On standard-sized drives with write fault detection logic, bit 5 is set to generate the write fault reset signal. This signal is used to clear a write fault indication within the drive. On mini-sized drives, this bit can be used to turn on or off the drive motor prior to initiating a drive operation. A time delay after turn on may be necessary for the drive to come up to speed. The register must be read prior to writing the register in order to save the states of the remaining bits. When the register is subsequently written to modify bit 5, the remaining bits must be restored to their previous states.

IBM DISKETTE GENERAL FORMAT INFORMATION

The IBM Flexible Diskette used for data storage and retrieval is organized into concentric circular paths or TRACKS. There are 77 tracks on either one or both sides (surfaces) of the diskette. On double-sided diskettes, the corresponding top and bottom tracks are referred to as a CYLINDER. Each track is further divided into fixed length sections or SECTORS. The number of sectors per track — 26, 15 or 8 — is determined when a track is formatted and is dependent on the sector length — 128, 256 or 512 bytes respectively — specified.

All tracks on the diskette are referenced to a physical index mark (a small hole in the diskette). Each time the hole passes a photodetector cell (one revolution of the diskette), an Index pulse is generated to indicate the logical beginning of a track. This index pulse is used to initiate a track formatting operation.

Track Format

Each Diskette Surface is divided into 77 tracks with each track divided into fixed length sectors. A sector can hold a whole record or a part of a record. If the record is shorter than the sector length, the unused bytes are filled with binary zeros. If a record is longer than the sector length, the record is written over as many sectors as its length requires. The sector size that provides the most efficient use of diskette space can be chosen depending upon the record length required.

Tracks are numbered from 00 (outer-most) to 76 (inner-most) and are used as follows:

TRACK 00 reserved as System Label Track
TRACKS 01 through 74 used for data
TRACKS 75 and 76 used as alternates.

Each sector consists of an ID field (which holds a unique address for the sector) and a data field.

The ID field is seven bytes long and is written for each sector when the track is formatted. Each ID field consists of an ID field Address Mark, a Cylinder Number byte which identifies the track number, a Head Number byte which specifies the head used (top or bottom) to access the sector, a Record Number byte identifying the sector number (1 through 26 for 128 byte sectors), an N-byte specifying the byte length of the sector and two CRC (Cyclic Redundancy Check) bytes.

The Gaps separating the index mark and the ID and data fields are written on a track when it is formatted. These gaps provide both an interval for switching the drive electronics from reading or writing and compensation for rotational speed and other diskette-to-diskette and drive-to-drive manufacturing tolerances to ensure that data written on a diskette by one system can be read by another (diskette interchangeability).

IBM Format Implementation Summary

Track Format

The disk has 77 tracks, numbered physically from 00 to 76, with track 00 being the outermost track. There are logically 75 data tracks and two alternate tracks. Any two tracks may be initialized as bad tracks. The data tracks are numbered logically in sequence from 00 to 74, skipping over bad tracks (alternate tracks replace bad tracks). Note: In IBM format track 00 cannot be a bad track.

Sector Format

Each track is divided into 26, 15, or 8 sectors of 128, 256, or 512 bytes length respectively. The first sector is numbered 01, and is physically the first sector after the physical index mark. The logical sequence of the remaining sectors may be nonsequential physically. The location of these is determined at initialization by CPU software.

Each sector consists of an ID field and a data field. All fields are separated by gaps. The beginning of each field is indicated by 6 bytes of $(00)_H$ followed by a one byte address mark.

Address Marks

Address Marks are unique bit patterns one byte in length which are used to identify the beginning of ID and Data fields. Address Mark bytes are unique from all other data

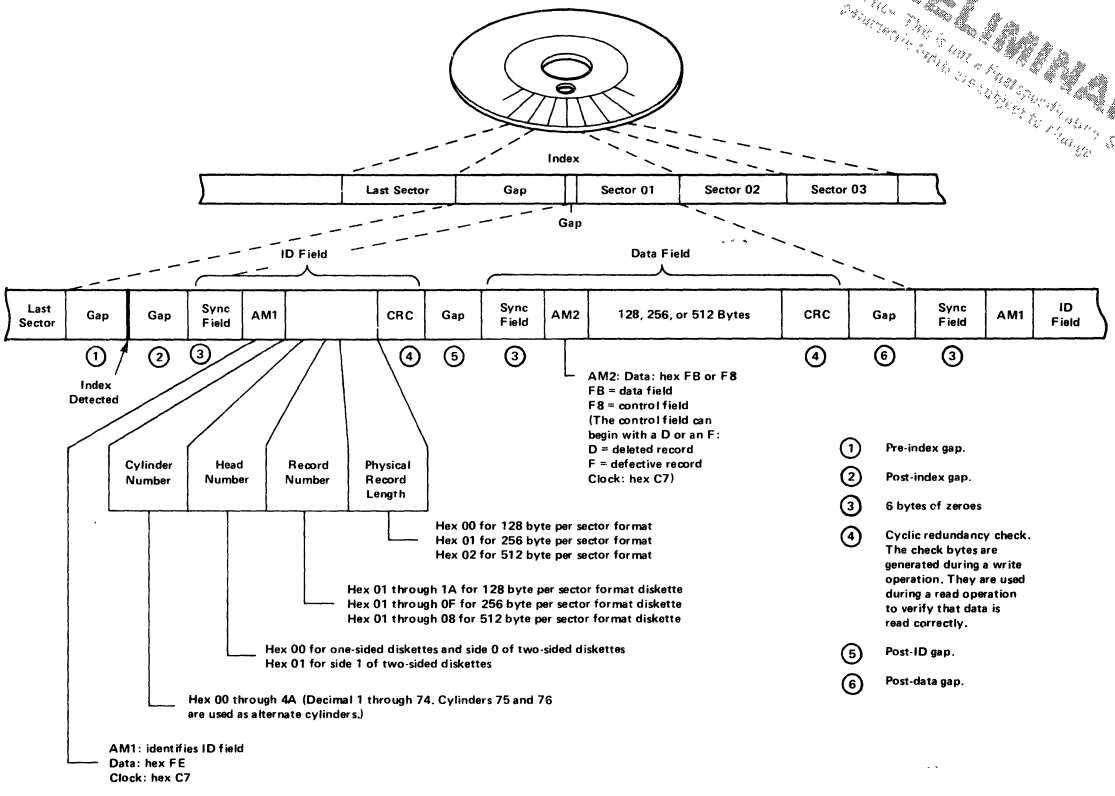


Figure 19. Track Format

bytes in that certain bit cells do not contain a clock bit (all other data bytes have clock bits in every bit cell.) There are four different types of Address Marks used. Each of these is used to identify different types of fields.

Index Address Mark

The Index Address Mark is located at the beginning of each track and is a fixed number of bytes in front of the first record.

ID Address Mark

The ID Address Mark byte is located at the beginning of each ID field on the diskette.

Data Address Mark

The Data Address Mark byte is located at the beginning of each non-deleted Data Field on the diskette.

Deleted Data Address Mark

The Deleted Data Address Mark byte is located at the beginning of each deleted Data Field on the diskette.

Address Mark Summary	Clock Pattern	Data Pattern
Index Address Mark	D7	FC
ID Address Mark	C7	FE
Data Address Mark	C7	FB
Deleted Data Address Mark	C7	F8
Bad Track ID Address Mark	C7	FE

ID Field

MARK	C	H	R	N	CRC	CRC

C = Cylinder (Track) Address, 00-74
H = Head Address
R = Record (Sector) Address, 01-26
N = Record (Sector) Length, 00-02
Note: Sector Length = 128 x 2^N bytes
CRC = 16 Bit CRC Character (See Below)

Data Field

MARK	DATA	CRC	CRC

Data is 128, 256, or 512 bytes long.

Note: All marks, data, ID characters and CRC characters are recorded and read most significant bit first.

CRC Character

The 16-bit CRC character is generated using the generator polynominal $X^{16} + X^{12} + X^5 + 1$, normally initialized to $(FF)_H$. It is generated from all characters (except the CRC in the ID or data field), including the data (not the clocks) in the address mark. It is recorded and read most significant bit first.

Data Format

Data is written (general case) in the following manner:

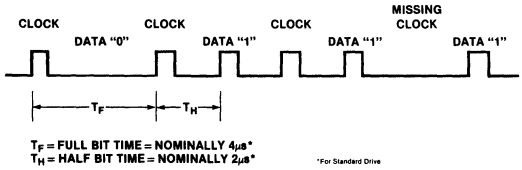


Figure 20. Data Format

References

"The IBM Diskette for Standard Data Interchange," IBM Document GA21-9182-0. "System 32," Chapter 8, IBM Document GA21-9176-0.

Bad Track Format

The Bad Track Format is the same as the good track format except that the bad track ID field is initialized as follows:

$$C = H = R = N = (FF)_H$$

When formatting, bad track registers should be set to FF_H for the drive during the formatting, thus specifying no bad tracks. Thus, all tracks are left available for formatting.

The track following the bad track(s) should be one higher in number than track before the bad track(s).

Upon completion of the format the bad tracks should be set up using the write special register command. The 8271 will then generate an extra step pulse to cross the bad track, locating a new track that now happens to be an extra track out.

Format Track

Format Command

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	SEL 1	SEL 0	1	0	0	0	1	1
PAR:	0	1	TRACK ADDRESS							
PAR:	0	1	GAP 3 SIZE MINUS 6							
PAR:	0	1	RECORD LENGTH			NO. OF SECTORS/TRACK				
PAR:	0	1	GAP 5 SIZE MINUS 6							
PAR:	0	1	GAP 1 SIZE MINUS 6							

The format command can be used to initialize a disk track compatible with the IBM 3740 format. A Shugart "IBM Type" mini-floppy format may also be generated.

The Format command can be used to initialize a diskette, one track at a time. When format command is used, the program must supply ID fields for each sector on the track. During command execution, the supplied ID fields (track head sector addresses and the sector length) are written sequentially on the diskette. The ID address marks originate from the 8271 and are written automatically as the first byte of each ID field. The CRC character is written in the last two bytes of the ID field and is derived from the data written in the first five bytes. During the formatting operation, the data field of each sector is filled with data pattern $(E5)_H$. The CRC, derived from the data pattern is also appended to the last byte.

1. The parameter 2 ($D_7 - D_5$) of the Format command specify record length, the bits are coded the same way as in the Read Data commands.
2. The programmable gap sizes (gap 3, gap 5, and gap 1) must be programmed such that the 6 bytes of zero (sync) are subtracted from the intended gap size i.e., if gap 1 is intended to be 16 bytes long, programmed length must be 16 – 6 = 10 bytes (of FF_H's).

Mini-Floppy Disk Format

The mini-floppy disk format differs from the standard disk format in the following ways:

1. Gap 5 and the Index Address mark have been eliminated.
2. There are fewer sectors/tracks.

GAPS

The following is the gap size and description summary:

Gap 1 Programmable
Gap 2 17 Bytes
Gap 3 Programmable
Gap 4 Variable
Gap 5 Programmable

The last six bytes of gaps 1,2,3 and 5 are $(00)_H$, all other bytes in the gaps are $(FF)_H$. The Gap 1,3 and 5 count specified by the user are the number of bytes of $(FF)_H$. Gap 4 is written until the leading edge of the index pulse. If a Gap 5 size of zero is specified, the Index Mark is not written.

Gap 1:
N bytes FF's
6 bytes 0's for sync
This gap separates the index address mark of the index pulse from the first ID mark. It is used to protect the first ID field from a write on the last physical sector of the current track.

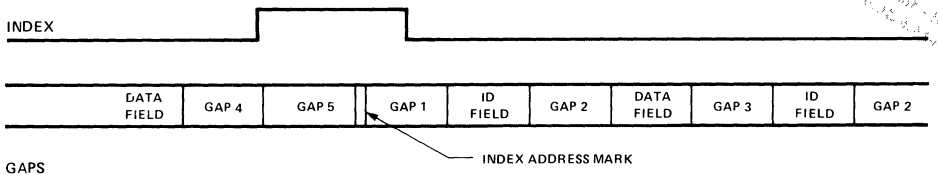
Gap 2:
11 bytes FF's
6 bytes 0's for sync
This gap separates the ID field from the data mark and field such that during a write only the data field will be changed even if the write gate turns on early, due to drive speed changes.

Gap 3:
N bytes FF's
6 bytes 0's for sync
This gap separates a data area from the next ID field. It is used so that during drive speed changes the next ID mark will not be overwritten, thus causing loss of data.

Gap 4:
FF's only
This gap fills out the rest of the disk and is used for slack during formatting. During drive speed variations this gap will shrink or grow if the disk is re-formatted.

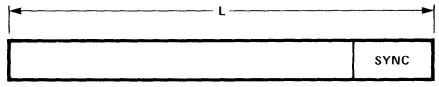
Gap 5:
N bytes FF's
6 bytes 0's for sync
This gap separates the last sector from the Index Address mark and is used to assure that the index address mark is not destroyed by writing on the last physical data sector on the track.

The number of FF bytes is programmable for gaps 1, 3 and 5.

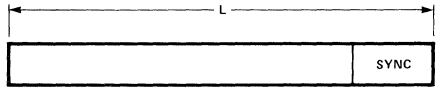


GAPS

GAP 1: POST INDEX GAP



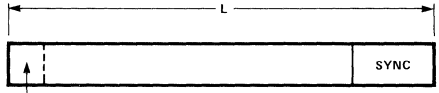
GAP 2: POST ID FIELD GAP



WRITE GATE TURN-ON FOR UPDATE OF NEXT DATA FIELD.

NOTE: THE WRITE GATE TURN-ON SHOULD BE TIMED TO WITHIN ± ≈ 1 BIT BY COUNTING THE BYTES IN THE GAP UNTIL 1 BYTE BEFORE THE TURN-ON.

GAP 3: POST DATA FIELD GAP

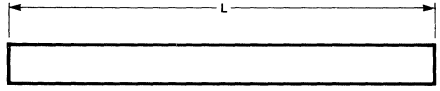


WRITE GATE TURN-OFF FROM UPDATE OF PREVIOUS DATA FIELD.

NOTE: IBM FORMAT REQUIRES AT LEAST 2 BINARY "1" BITS AS A DATA FIELD POSTAMBLE.

2-BITS

GAP 4: FINAL GAP



GAP 5: INITIAL GAP

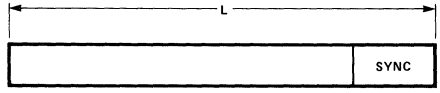
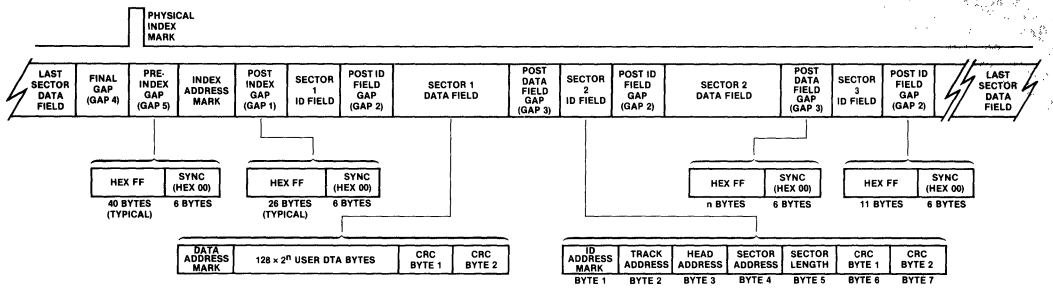


Figure 21. Track Format

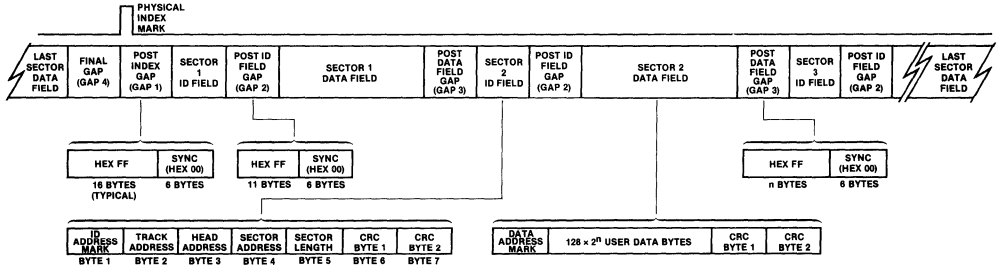


NUMBER OF SECTORS	NUMBER OF BYTES										
	GAP 1		ID FIELD	GAP 2		DATA FIELD	GAP 3		GAP 4	GAP 5	
	*ONES	SYNC		ONES	SYNC		*ONES	SYNC		*ONES	SYNC
26	26	6	7	11	6	131	27	6	275	40	6
15	26	6	7	11	6	259	48	6	129	40	6
8	26	6	7	11	6	515	90	6	146	40	6
4	26	6	7	11	6	1027	224	6	236	40	6
2	26	6	7	11	6	2051	255	6	719	40	6
1	26	6	7	11	6	4099	0	0	1007	40	6

*Program Specified

5208 Bytes Per Track

Figure 22. Standard Diskette Track Format



NUMBER OF SECTORS	NUMBER OF BYTES								
	GAP 1		ID FIELD	GAP 2		DATA FIELD	GAP 3		GAP 4
	*ONES	SYNC		ONES	SYNC		*ONES	SYNC	
18	16	6	7	11	6	131	11	6	24
10	16	6	7	11	6	259	21	6	30
5	16	6	7	11	6	515	74	6	88
2	16	6	7	11	6	1027	255	6	740
1	16	6	7	11	6	2051	0	0	1028

*Program Specified

3125 Bytes Per Track

Figure 23. Mini-Diskette Track Format

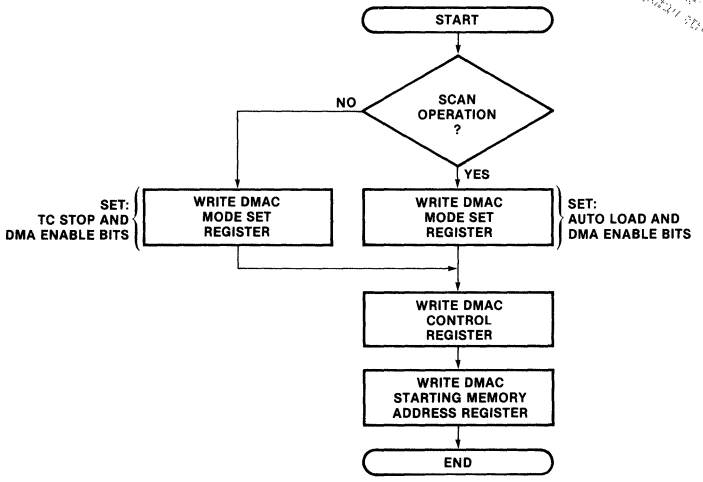


Figure 23. User DMA Channel Initialization Flowchart

Read ID Command

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	SEL 1	SEL 0	0	1	1	0	1	1
PAR:	0	1	TRACK ADDRESS							
PAR:	0	1	0	0	0	0	0	0	0	0
PAR:	0	1	NUMBER OF ID FIELDS							

The Read ID command transfers the specified number of ID fields into memory (beginning with the first ID field after Index). The CRC character is checked but not transferred.

These fields are entered into memory in the order in which they are physically located on the disk, with the first field being the one starting at the index pulse.

Data Processing Commands

All the routine Read/Write commands examine specific drive status lines before beginning execution, perform an implicit seek to the track address and load the drive's read/write head. Regardless of the type of command (i.e., read, write or verify), the 8271 first reads the ID field(s) to verify that the correct track has been located (see sector not found completion code) and also to locate the addressed sector. When a transfer is complete (or cannot be completed), the 8271 sets the interrupt request bit in the status register and provides an indication of the outcome of the operation in the result register.

If a CRC error is detected during a multisector transfer, processing is terminated with the sector in error. The address of the failing sector number can be determined by examining the Scan Sector Number register using the Read Special Register command.

Full power of the multisector read/write commands can be realized by doing DMA transfer using Intel® 8257 DMA Controller, For example, in a 128 byte per sector multisector write command, the entire data block (containing 128 bytes times the number of sectors) can be located in a disk memory buffer. Upon completion of the command phase, the 8271 begins execution by accessing the desired track, verifying the ID field, and locating the data field of the first record to be written. The 8271 then DMA-accesses the first sector and starts counting and writing one byte at a time until all 128 bytes are written. It then locates the data field of the next sector and repeats the procedure until all the specified sectors have been written. Upon completion of the execution phase the 8271 enters into the result phase and interrupts the CPU for availability of status and completion results. Note that all read/write commands, single or multisector are executed without CPU intervention.

Note, execution of multi-sector operations are faster if the sectors are *not* interleaved.

128 Byte Single Record Format

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	SEL 1	SEL 0	COMMAND OPCODE					
PAR:	0	1	TRACK ADDR 0-255							
PAR:	0	1	SECTOR 0-255							

Commands	Opcode
READ DATA	12
READ DATA AND DELETED DATA	16
WRITE DATA	0A
WRITE DELETED DATA	0E
VERIFY DATA AND DELETED DATA	1E

Variable Length/Multi-Record Format

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	SEL 1	SEL 0	COMMAND OPCODE					
PAR:	0	1	TRACK ADDR 0-255							
PAR:	0	1	SECTOR 0-255							
PAR:	0	1	LENGTH				NO. OF SECTORS			

D_7-D_5 of Parameter 2 determine the length of the disk record.

0 0 0	128 Bytes
0 0 1	256 Bytes
0 1 0	512 Bytes
0 1 1	1024 Bytes
1 0 0	2048 Bytes
1 0 1	4096 Bytes
1 1 0	8192 Bytes
1 1 1	16,384 Bytes

Commands	Opcode
READ DATA	13
READ DATA AND DELETED DATA	17
WRITE DATA	0B
WRITE DELETED DATA	0F
VERIFY DATA AND DELETED DATA	1F
SCAN DATA	00
SCAN DATA AND DELETED DATA	04

Read Commands

Read Data, Read Data and Deleted Data.

Function

The read command transfers data from a specified disk record or group of records to memory. The operation of this command is outlined in execution phase table.

Write Commands

Write Data, Write Deleted Data.

Function

The write command transfers data from memory to a specified disk record or group of records.

Verify Command

Verify Data and Deleted Data.

Function

The verify command is identical to the read data and deleted data command except that the data is not transferred to memory. This command is used to check that a record or a group of records has been written correctly by verifying the CRC character.

Scan Commands

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	SEL 1	SEL 0	0	0	0	S.DATA S.DELD	0	0
PAR:	0	1	TRACK ADDR 0 255							
PAR:	0	1	SECTOR 0 255							
PAR	0	1	LENGTH				NO. OF SECTORS			
PAR	0	1	SCAN TYPE		STEP SIZE					
PAR:	0	1	FIELD LENGTH (KEY)							

Command $D_2 = 0$ Scan Data
$D_2 = 1$ Scan Data and Deleted Data

Scan Commands, Scan Data and Scan Data and Deleted Data, are used to search a specific data pattern or "key" from memory. The 8271 FDC operation during a scan is unique in that data is read from memory and from the diskette simultaneously.

During the scan operation, the key is compared repetitively (using the 8257 DMA Controller in auto load mode) with the data read from the diskette (e.g., an eight byte key would be compared with the first eight bytes (1-8) read from the diskette, the second eight bytes (9-16), the third eight bytes (17-24), etc.). The scan operation is concluded when the key is located or when the specified number of sectors have been searched without locating the key. When concluded, the 8271 FDC requests an interrupt. The program must then read the result register to determine if the scan was successful (if the key was located). If successful, several of the FDC's special registers can be examined (read special registers command) to determine more specific information relating to the scan (i.e., the sector number in which the key was located, and the number of bytes within the sector that were not compared when the key was located).

The 8271 does not do a sliding scan, it does a fixed block linear search. This means the key in memory is compared to an equal length block in a sector; when these blocks meet the scan conditions the scan will stop. Otherwise, the scan continues until all the sectors specified have been searched.

The following factors regarding key length must be considered when establishing a key in memory.

1. When searching multiple sectors, the length of the key must be evenly divisible into the sector length to prevent the key from being split at subsequent sector boundaries. Since the character FF_H is not compared, the key in memory can be padded to the required length using this character. For example, if the actual pattern compared on the diskette is twelve characters in length, the field length should be sixteen and four bytes of FF_H

would be appended to the key. Consequently, the last block of sixteen bytes compared within the first sector would end at the sector boundary and the first byte of the next sector would be compared with the first byte of the key. Splitting data over sector boundarys will not work properly since the FDC expects the start of key at each sector boundary.

2. Since the first byte of the key is compared with the first byte of the sector, when the pattern does not begin with the first byte of the sector, the key must be offset using the character FF_{16}. For example, if the first byte of a nine byte pattern begins on the fifth byte of the sector, four bytes of FF_{16} are prefixed to the key (and three bytes of FF_{16} are appended to the key to meet the length requirement) so that the first actual comparison begins on the fifth byte.

The Scan Commands require five parameters:

Parameter 0, Track Address

Specifies the track number containing the sectors to be scanned. Legal values range from 00_H to $4C_H$ (0 to 76) for a standard diskette and from 00_H to 22_H (0 to 34) for a mini-sized diskette.

Parameter 1, Sector Address

Specifies the first sector to be scanned. The number of sectors scanned is specified in parameter 2, and the order in which sectors are scanned is specified in parameter 3.

Parameter 2, Sector Length/Number of Sectors

The sector length field (bits 7-5) specifies the number of data bytes allocated to each sector (see parameter 2, routine read and write commands for field interpretation). The number of sectors field (bits 4-0) specifies the number of sectors to be scanned. The number specified ranges from one sector to the physical number of sectors on the track.

Parameter 3

D_7-D_6: Indicate scan type

00-EQ Scan for each character within the field length (key) equal to the corresponding character within the disk sector. The scan stops after the first equal condition is met.

01-GEQ Scan for each character within the disk sector greater than or equal to the corresponding character within the field length (key). The scan stops after the first greater than or equal condition is met.

10-LEQ Scan for each character within the disk sector less than or equal to the corresponding character within the field length (key). The scan stops after the first less than or equal condition is met.

D_5-D_0: Step Size: The Step Size field specifies the offset to the next sector in a multisector scan. In this case, the next sector address is generated by adding the Step Size to the current sector address.

Parameter 4, Field Length

Specifies the number of bytes to be compared (length of key). While the range of legal values is from 1 to 255, the field length specified should be evenly divisible into the sector length to prevent the key from being split at sector boundaries, if the multisector scan commands are used.

Scan Command Results

More detailed information about the completion of Scan Commands may be obtained by executing Read Special Register commands.

Read Special Register

Parameter (Hex)	Results
06	The sector number of the sector in which the specified scan data pattern was located.
14	MSB Count — The number of 128 byte blocks remaining to be compared in the current sector when the scan data pattern was located. This register is decremented with each 128 byte block read.
13	LSB Count — The number of bytes remaining to be compared in the current sector when the scan data pattern is located. This register is initialized to 128 and is decremented with each byte compared.

Upon a scan met condition, the equation below can be used to determine the last byte in the located pattern.

Pointer = sector length − ((Register 14H) * 128 + (Register 13H))

8271 Scan Command Example

Assume there are only 2 records on track 0 with the following data:

Record 01: 01 02 03 04 05 06 07 08 000....00
Record 02: 01 02 AA 55 00 00 00 00 00

Command	Field Length [1]	Starting Sector #	# of Sectors	Key [2]	Completion Code [3]	Special Registers [4] R06	R14	R13	Comment
* SCAN EQ	2	1	1	01,02	SME	01	0	127D	Met in first field
SCAN EQ	2	1	1	02,03	SNM	X	X	X	Not met
SCAN EQ	2	1	1	FF[5],05	SNM	X	X	X	Not met with don't care
* SCAN EQ	2	1	1	FF[5],06	SME	01	0	123D	Met with don't care
* SCAN EQ	2	1	2	AA,55	SME	02	0	125D	Met in Record 02
* SCAN EQ	2	2	1	01,02	SME	02	0	127D	Starting sector ≠ 1
* SCAN EQ	4	1	1	05,06,07,08	SME	01	0	121D	Field, Key length = 4
* SCAN GEQ	4	1	1	05,06,07,08	SME	01	0	121D	GEQ-SME
* SCAN GEQ	4	1	1	05,04,07,08	SMNE	01	0	121D	GEQ-SMNE
* SCAN GEQ	4	1	2	00,03,AA,44 [6]	SNM	X	X	X	GEQ-SNM
* SCAN LEQ	4	1	1	01,03,FF,04	SMNE	01	0	125D	LEQ-SMNE
* SCAN LEQ	4	1	1	01,02,FF,04	SME	01	0	125D	LEQ-SME

NOTES:

1. Field Length — Each record is partitioned into a number of fields equal to the record size divided by the field length. Note that the record size should be evenly divisable by the field length to insure proper operation of multi record scan. Also, maximum field length = 256 bytes.

2. Key — The key is a string of bytes located in the user system memory. The key length should equal the field length. By programming the 8257 DMA Controller into the auto load mode, the key will be recursively read in by the chip (once per field).

3. Completion Code — Shows how Scan command was met or not met.
   SNM — SCAN Not Met — 0 0 (also Good Complete)
   SME — SCAN Met Equal — 0 1
   SMNE — SCAN Met Not Equal — 1 0

4. Special Registers
   R06 — This register contains the record number where the scan was met.
   R14 — This register contains the MSB count and is decremented every 128 characters.

Length (ℓ) (D7-D5 of PAR 2)	Record Size	R14 = $2^{\ell} - 1$ (Initialize at Beginning of Record)
000	128 Bytes	0
001	256 Bytes	1
010	512 Bytes	3
011	1024 Bytes	7
•	•	•
•	•	•
•	•	•

   R13 — This register contains a modulo 128 LSB count which is initialized to 128 at beginning of each record. This count is decremented after each character is compared except for the last character in a pattern match situation.

5. The OFF_H character in the key is treated as a don't care character position.

6. The Scan comparison is done on a byte by byte basis. That is, byte 1 of each field is compared to byte 1 of the key, byte 2 of each field is compared to byte 2 of the key, etc.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . – 65°C to + 150°C
Voltage on Any Pin with
Respect to Ground . . . . . – 0.5V to + 7V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0°C$ to 70°C, $V_{CC} = +5.0V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	(V_{CC} + 0.5)	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA for Data Bus Pins I_{OL} = 1.7 mA for All Other Pins
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -220\ \mu A$
I_{IL}	Input Load Current		± 10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OZ}	Off-State Output Current		± 10	μA	$V_{OUT} = V_{CC}$ to 0V
I_{CC}	V_{CC} Supply Current		180	mA	

CAPACITANCE

$T_A = 25°C$, $V_{CC} = GND = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	t_c = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured Pins Returned to GND

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = +5.0V \pm 5\%$

Read Cycle

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AC}	Select Setup to $\overline{RD}$	0		ns	Note 2
t_{CA}	Select Hold from $\overline{RD}$	0		ns	Note 2
t_{RR}	$\overline{RD}$ Pulse Width	250		ns	
t_{AD}	Data Delay from Address		250	ns	Note 2
t_{RD}	Data Delay from $\overline{RD}$		150	ns	$C_L = 150$ pF, Note 2
t_{DF}	Output Float Delay	20	100	ns	$C_L = 20$ pF for Minimum; 150 pF for Maximum
t_{DC}	DACK Setup to $\overline{RD}$	25		ns	
t_{CD}	DACK Hold from $\overline{RD}$	25		ns	
t_{KD}	Data Delay from DACK		250	ns	

Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AC}	Select Setup to $\overline{WR}$	0		ns	
t_{CA}	Select Hold from $\overline{WR}$	0		ns	
t_{WW}	$\overline{WR}$ Pulse Width	250		ns	
t_{DW}	Data Setup to $\overline{WR}$	150		ns	
t_{WD}	Data Hold from $\overline{WR}$	0		ns	
t_{DC}	DACK Setup to $\overline{WR}$	25		ns	
t_{CD}	DACK Hold from $\overline{WR}$	25		ns	

DMA

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CQ}	Request Hold from $\overline{WR}$ or $\overline{RD}$ (for Non-Burst Mode)		150	ns	

Other Timing

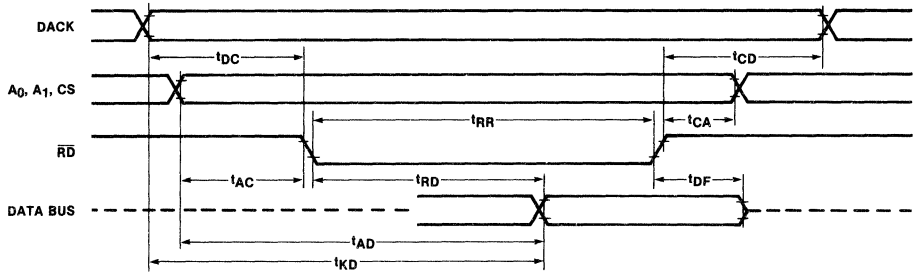
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{RSTW}	Reset Pulse Width	10		t_{CY}	
t_r	Input Signal Rise Time		20	ns	
t_f	Input Signal Fall Time		20	ns	
t_{RSTS}	Reset to First $\overline{IOWR}$	2		t_{CY}	
t_{CY}	Clock Period	250			Note 3
t_{CL}	Clock Low Period	110		ns	
t_{CH}	Clock High Period	122		ns	
t_{DS}	Data Window Setup to Unseparated Clock and Data	50		ns	
t_{DH}	Data Window Hold from Unseparated Clock and Data	0		ns	

NOTES:

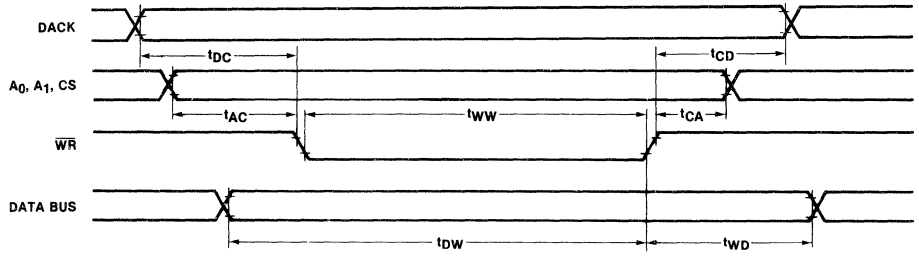
1. All timing measurements are made at the reference voltages unless otherwise specified: Input "1" at 2.0V, "0" at 0.8V
   Output "1" at 2.0V, "0" at 0.8V
2. t_{AD}, t_{RD}, t_{AC}, and t_{CA} are not concurrent specs.
3. Standard Floppy: $t_{CY} = 250$ ns $\pm 0.4\%$ Mini-Floppy: $t_{CY} = 500$ ns $\pm 0.4\%$

WAVEFORMS

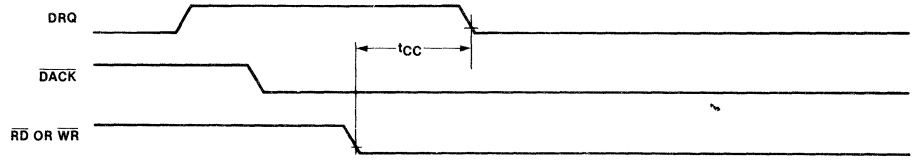
Read Waveforms

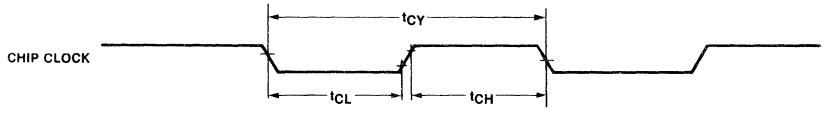


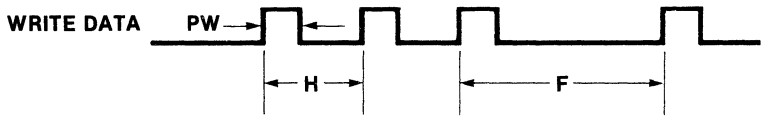
Write Waveforms



DMA Waveforms



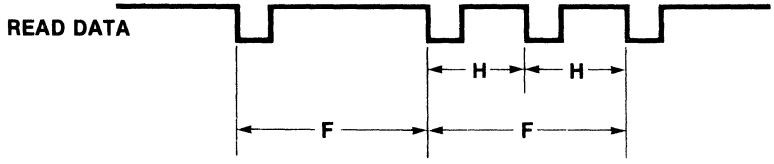




PULSE WIDTH PW = t_{CY} ±30 ns
H (HALF BIT CELL) = 8 t_{CY}
F (FULL BIT CELL) = 16 t_{CY}

*t_{CY} =		**t_{CY} =	
250 ns	±0.4%	500 ns	±0.4%
250 ns	±30 ns	500 ns	±30 ns
2.0 μs	± 8 ns	4.0 μs	±16 ns
4.0 μs	±16 ns	8.0 μs	±32 ns

Figure 24. Write Data



*t_{CY} = 250 ns **t_{CY} = 500 ns

F = 16 t_{CY} ±8 t_{CY}
H = 8 t_{CY} ±4 t_{CY}

Figure 25. Read Data

*STANDARD FLEXIBLE DISK DRIVE TIMING
**MINI-FLOPPY TIMING

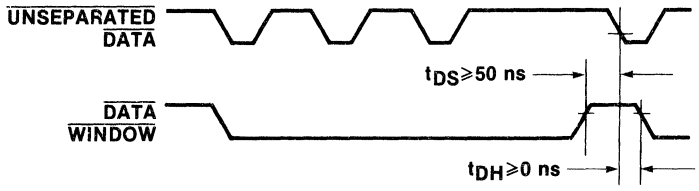
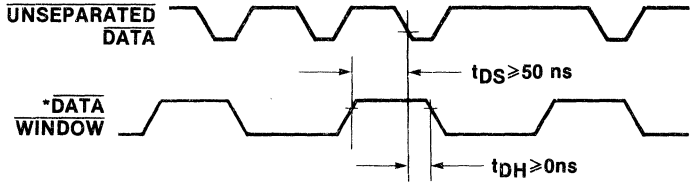


Figure 26. Single-Shot Data Separator



*DATA WINDOW MAY BE 180° OUT OF PHASE IN PLO DATA SEPARATION MODE.

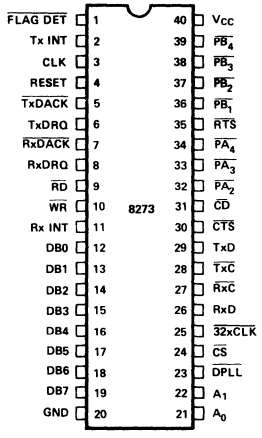
Figure 27. PLO Data Separator

8273
PROGRAMMABLE HDLC/SDLC PROTOCOL CONTROLLER

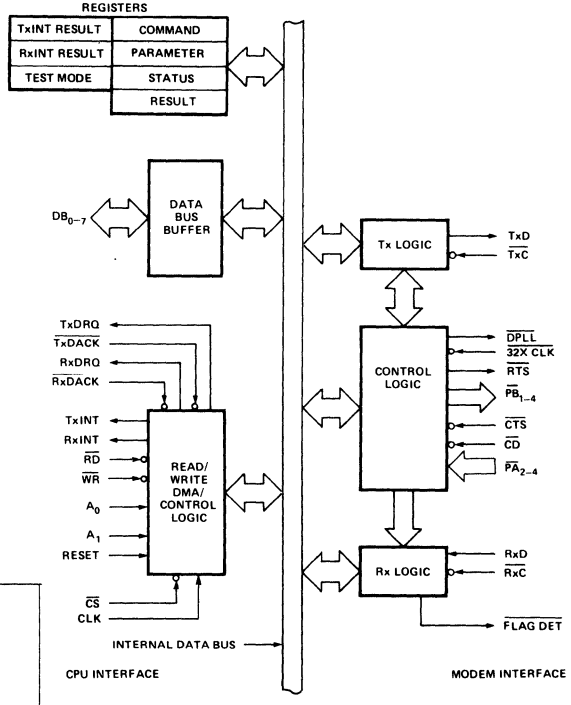
- **HDLC/SDLC Compatible**
- **Frame Level Commands**
- **Full Duplex, Half Duplex, or Loop SDLC Operation**
- **Up to 64K Baud Transfers**
- **Two User Programmable Modem Control Ports**
- **Automatic FCS (CRC) Generation and Checking**
- **Programmable NRZI Encode/Decode**
- **N-Bit Reception Capability**
- **Digital Phase Locked Loop Clock Recovery**
- **Minimum CPU Overhead**
- **Fully Compatible with 8080/8085 CPUs**
- **Single +5V Supply**
- **40-Pin Package**

The Intel® 8273 Programmable HDLC/SDLC Protocol Controller is a dedicated device designed to support the ISO/C-CITT's HDLC and IBM's SDLC communication line protocols. It is fully compatible with Intel's new high performance microcomputer systems such as the MCS-85™. A frame level command set is achieved by a unique microprogrammed dual processor chip architecture. The processing capability supported by the 8273 relieves the system CPU of the low level real-time tasks normally associated with controllers.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

DB0–DB7	DATA BUS (8 BITS)	$\overline{CS}$	CHIP SELECT
$\overline{FLAG\ DET}$	FLAG DETECT	$\overline{32xCLK}$	32 TIMES CLOCK
TxINT	TRANSMITTER INTERRUPT	Rx D	RECEIVER DATA
CLK	CLOCK INPUT	$\overline{Rx\ C}$	RECEIVER CLOCK
$\overline{RESET}$	RESET	$\overline{Tx\ C}$	TRANSMITTER CLOCK
$\overline{Tx\ DACK}$	TRANSMITTER DMA ACKNOWLEDGE	Tx D	TRANSMITTER DATA
TxDRQ	TRANSMITTER DMA REQUEST	$\overline{CTS}$	CLEAR TO SEND
$\overline{RD}$	READ INPUT	$\overline{CD}$	CARRIER DETECT
$\overline{WR}$	WRITE INPUT	$\overline{PA_2}$–$\overline{PA_4}$	GP INPUT PORTS
$\overline{Rx\ DACK}$	RECEIVER DMA ACKNOWLEDGE	$\overline{PB_1}$–$\overline{PB_4}$	GP OUTPUT PORTS
Rx DRQ	RECEIVER DMA REQUEST	$\overline{RTS}$	REQUEST TO SEND
Rx INT	RECEIVER INTERRUPT	V_{CC}	+5 VOLT SUPPLY
A0–A1	COMMAND REGISTER SELECT ADDRESS	GND	GROUND
$\overline{DPLL}$	DIGITAL PHASE LOCKED LOOP		

MPU PERIPHERALS

A BRIEF DESCRIPTION OF HDLC/SDLC PROTOCOLS

General

The High Level Data Link Control (HDLC) is a standard communication link protocol established by International Standards Organization (ISO). HDLC is the discipline used to implement ISO X.25 packet switching systems.

The Synchronous Data Link Control (SDLC) is an IBM communication link protocol used to implement the System Network Architecture (SNA). Both the protocols are bit oriented, code independent, and ideal for full duplex communication. Some common applications include terminal to terminal, terminal to CPU, CPU to CPU, satellite communication, packet switching and other high speed data links. In systems which require expensive cabling and interconnect hardware, any of the two protocols could be used to simplify interfacing (by going serial), thereby reducing interconnect hardware costs. Since both the protocols are speed independent, reducing interconnect hardware could become an important application.

Network

In both the HDLC and SDLC line protocols, according to a pre-assigned hierarchy, a PRIMARY (Control) STATION controls the overall network (data link) and issues commands to the SECONDARY (Slave) STATIONS. The latter comply with instructions and respond by sending appropriate RESPONSES. Whenever a transmitting station must end transmission prematurely it sends an ABORT character. Upon detecting an abort character, a receiving station ignores the transmission block called a FRAME. Time fill between frames can be accomplished by transmitting either continuous frame preambles called FLAGS or an abort character. A time fill within a frame is not permitted. Whenever a station receives a string of more that fifteen consecutive ones, the station goes into an IDLE state.

Frames

A single communication element is called a FRAME which can be used for both Link Control and data transfer purposes. The elements of a frame are the beginning eight bit FLAG (F) consisting of one zero, six ones, and a zero, an eight bit ADDRESS FIELD (A), an eight bit CONTROL FIELD (C), a variable (N-bit) INFORMATION FIELD (I), a sixteen bit FRAME CHECK SEQUENCE (FCS), and an eight bit end FLAG (F), having the same bit pattern as the beginning flag. In HDLC the Address (A) and Control (C) bytes are extendable. The HDLC and the SDLC use three types of frames; an Information Frame is used to transfer data, a Supervisory Frame is used for control purposes, and a Non-sequenced Frame is used for initialization and control of the secondary stations.

Frame Characteristics

An important characteristic of a frame is that its contents are made code transparent by use of a zero bit insertion and deletion technique. Thus, the user can adopt any format or code suitable for his system — it may even be a computer word length or a "memory dump". The frame is bit oriented that is, bits, not characters in each field, have specific meanings. The Frame Check Sequence (FCS) is an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices. The Command and Response information frames contain sequence numbers in the control fields identifying the sent and received frames. The sequence numbers are used in Error Recovery Procedures (ERP) and as implicit acknowledgement of frame communication, enhancing the true full-duplex nature of the HDLC/SDLC protocols.

In contrast, BISYNC is basically half-duplex (two way alternate) because of necessity to transmit immediate acknowledgement frames. HDLC/SDLC therefore saves propagation delay times and have a potential of twice the throughput rate of BISYNC.

It is possible to use HDLC or SDLC over half duplex lines but there is a corresponding loss in throughput because both are primarily designed for full-duplex communication. As in any synchronous system, the bit rate is determined by the clock bits supplied by the modem, protocols themselves are speed independent.

A byproduct of the use of zero-bit insertion-deletion technique is the non-return-to-zero invert (NRZI) data transmission/reception compatibility. The latter allows HDLC/SDLC protocols to be used with asynchronous data communication hardware in which the clocks are derived from the NRZI encoded data.

References

IBM Synchronous Data Link Control General Information, IBM, GA27-3093-1.

Standard Network Access Protocol Specification, DATAPAC, Trans-Canada Telephone System CCG111

Recommendation X.25, ISO/CCITT March 2, 1976.

IBM 3650 Retail Store System Loop Interface OEM Information, IBM, GA 27-3098-0

Guidebook to Data Communications, Training Manual, Hewlett-Packard 5955-1715

IBM Introduction to Teleprocessing, IBM, GC 20-8095-02

System Network Architecture, Technical Overview, IBM, GA 27-3102

System Network Architecture Format and Protocol, IBM GA 27-3112

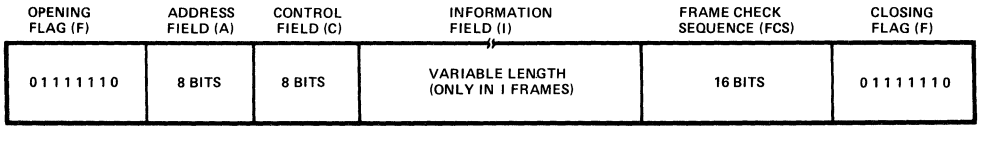


Figure 1. Frame Format

FUNCTIONAL DESCRIPTION

General

The Intel® 8273 HDLC/SDLC controller is a microcomputer peripheral device which supports the International Standards Organization (ISO) High Level Data Link Control (HDLC), and IBM Synchronous Data Link Control (SDLC) communications protocols. This controller minimizes CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. The 8273 can be used in either synchronous or asynchronous applications. In asynchronous applications the data can be programmed to be encoded/decoded in NRZI code. The clock is derived from the NRZI data using a digital phase locked loop. The data transparency is achieved by using a zero-bit insertion/deletion technique. The frames are automatically checked for errors during reception by verifying the Frame Check Sequence (FCS); the FCS is automatically generated and appended before the final flag in transmit.

The 8273 recognizes and can generate flags (01111110), Abort, Idle, and GA (EOP) characters.

The 8273 can assume either a primary (control) or a secondary (slave) role. It can therefore be readily implemented in an SDLC loop configuration as typified by the IBM 3650 Retail Store System by programming the 8273 into a one-bit delay mode. In such a configuration, a two wire pair can be effectively used for data transfer between controllers and loop stations. The digital phase locked loop output pin can be used by the loop station without the presence of an accurate Tx clock.

Hardware Description

The 8273 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name (No.)	I/O	Description
V_{CC} (40)		+5V Supply
GND (20)		Ground
RESET (4)	I	A high signal on this pin will force the 8273 to an idle state. The 8273 will remain idle until a command is issued by the CPU. The modem interface output signals are forced high. Reset must be true for a minimum of 10 TCY.
$\overline{CS}$ (24)	I	The $\overline{RD}$ and $\overline{WR}$ inputs are enabled by the chip select input.
DB_7-DB_0 (19-12)	I/O	The Data Bus lines are bidirectional three-state lines which interface with the system Data Bus.
$\overline{WR}$ (10)	I	The Write signal is used to control the transfer of either a command or data from CPU to the 8273.
$\overline{RD}$ (9)	I	The Read signal is used to control the transfer of either a data byte or a status word from the 8273 to the CPU.
TxINT (2)	O	The Transmitter interrupt signal indicates that the transmitter logic requires service.
RxINT (11)	O	The Receiver interrupt signal indicates that the Receiver logic requires service.
TxDRQ (6)	O	Requests a transfer of data between memory and the 8273 for a transmit operation.
RxRDQ (8)	O	Requests a transfer of data between the 8273 and memory for a receive operation.
$\overline{TxDACK}$ (5)	I	The Transmitter DMA acknowledge signal notifies the 8273 that the TxDMA cycle has been granted.
$\overline{RxDACK}$ (7)	I	The Receiver DMA acknowledge signal notifies the 8273 that the RxDMA cycle has been granted.
A_1-A_0 (22-21)	I	These two lines are CPU Interface Register Select lines.
TxD (29)	O	This line transmits the serial data to the communication channel.
$\overline{TxC}$ (28)	I	The transmitter clock is used to synchronize the transmit data.
RxD (26)	I	This line receives serial data from the communication channel.
$\overline{RxC}$ (27)	I	The Receiver Clock is used to synchronize the receive data.
$\overline{32X\ CLK}$ (25)	I	The 32X clock is used to provide clock recovery when an asynchronous modem is used. In loop configuration the loop station can run without an accurate 1X clock by using the 32X CLK in conjunction with the DPLL output. (This pin must be grounded when not used).
$\overline{DPLL}$ (23)	O	Digital Phase Locked Loop output can be tied to RxC and/or TxC when 1X clock is not available. DPLL is used with 32X CLK.
$\overline{FLAG\ DET}$ (1)	O	Flag Detect signals that a flag (01111110) has been received by an active receiver.
$\overline{RTS}$ (35)	O	Request to Send signals that the 8273 is ready to transmit data.
$\overline{CTS}$ (30)	I	Clear to Send signals that the modem is ready to accept data from the 8273.
$\overline{CD}$ (31)	I	Carrier Detect signals that the line transmission has started and the 8273 may begin to sample data on RxD line.
$\overline{PA_{2-4}}$ (32-34)	I	General purpose input ports. The logic levels on these lines can be Read by the CPU through the Data Bus Buffer.
$\overline{PB_{1-4}}$ (36-39)	O	General purpose output ports. The CPU can write these output lines through Data Bus Buffer.
CLK (3)	I	A square wave TTL clock.

CPU Interface

The CPU interface is optimized for the MCS-80/85™ bus with an 8257 DMA controller. However, the interface is flexible, and allows either DMA or non-DMA data transfers, interrupt or non-interrupt driven. It further allows maximum line utilization by providing early interrupt mechanism for buffered (only the information field can be transferred to memory) Tx command overlapping. It also provides separate Rx and Tx interrupt output channels for efficient operation. The 8273 keeps the interrupt request active until all the associated interrupt results have been read.

The CPU utilizes the CPU interface to specify commands and transfer data. It consists of seven registers addressed via $\overline{CS}$, A_1, A_0, $\overline{RD}$ and $\overline{WR}$ signals and two independent data registers for receive data and transmit data. A_1, A_0 are generally derived from two low order bits of the address bus. If an 8080 based CPU is utilized, the $\overline{RD}$ and $\overline{WR}$ signals may be driven by the 8228 $\overline{I/OR}$ and $\overline{I/OW}$. The table shows the seven register select decoding:

A_1	A_0	$\overline{TxDACK}$	$\overline{RxDACK}$	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Register
0	0	1	1	0	1	0	Command
0	0	1	1	0	0	1	Status
0	1	1	1	0	1	0	Parameter
0	1	1	1	0	0	1	Result
1	0	1	1	0	1	0	Reset
1	0	1	1	0	0	1	TxINT Result
1	1	1	1	0	1	0	—
1	1	1	1	0	0	1	RxINT Result
X	X	0	1	1	1	0	Transmit Data
X	X	1	0	1	0	1	Receive Data

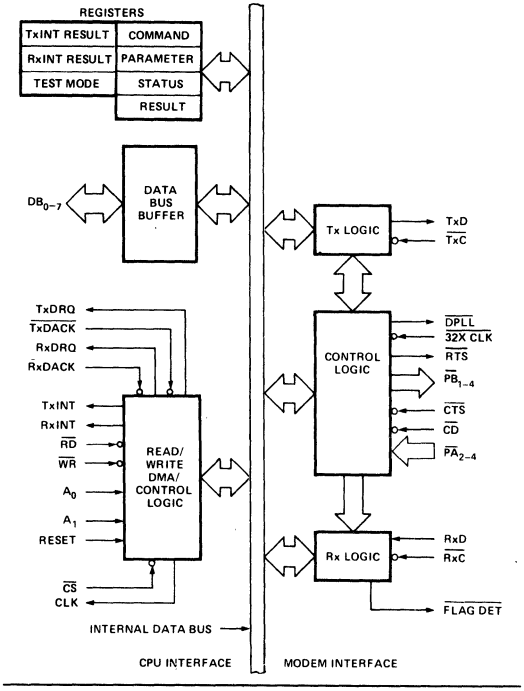


Figure 2. 8273 Block Diagram Showing CPU Interface Functions

Register Description

Command

Operations are initiated by writing an appropriate command in the Command Register.

Parameter

Parameters of commands that require additional information are written to this register.

Result

Contains an immediate result describing an outcome of an executed command.

Transmit Interrupt Result

Contains the outcome of 8273 transmit operation (good/bad completion).

Receive Interrupt Result

Contains the outcome of 8273 receive operation (good/bad completion), followed by additional results which detail the reason for interrupt.

Status

The status register reflects the state of the 8273 CPU Interface.

DMA Data Transfers

The 8273 CPU interface supports two independent data interfaces: receive data and transmit data. At high data transmission speeds the data transfer rate of the 8273 is great enough to justify the use of direct memory access (DMA) for the data transfers. When the 8273 is configured in DMA mode, the elements of the DMA interfaces are:

TxDRQ: Transmit DMA Request

Requests a transfer of data between memory and the 8273 for a transmit operation.

$\overline{TxDACK}$: Transmit DMA Acknowledge

The $\overline{TxDACK}$ signal notifies the 8273 that a transmit DMA cycle has been granted. It is also used with $\overline{WR}$ to transfer data to the 8273 in non-DMA mode.

RxDRQ: Receive DMA Request

Requests a transfer of data between the 8273 and memory for a receive operation.

$\overline{\text{RxDACK}}$: Receive DMA Acknowledge

The $\overline{\text{RxDACK}}$ signal notifies the 8273 that a receive DMA cycle has been granted. It is also used with $\overline{\text{RD}}$ to read data from the 8273 in non-DMA mode.

$\overline{\text{RD}}$, $\overline{\text{WR}}$: Read, Write

The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals are used to specify the direction of the data transfer.

DMA transfers require the use of a DMA controller such as the Intel 8257. The function of the DMA controller is to provide sequential addresses and timing for the transfer, at a starting address determined by the CPU. Counting of data block lengths is performed by the 8273.

To request a DMA transfer the 8273 raises the appropriate DMA REQUEST. DMA ACKNOWLEDGE and READ enables DMA data onto the bus (independently of CHIP SELECT). DMA ACKNOWLEDGE and WRITE transfers DMA data to the 8273 (independent of CHIP SELECT).

It is also possible to configure the 8273 in the non-DMA data transfer mode. In this mode the CPU module must pass data to the 8273 in response to non-DMA data requests indicated by the status word.

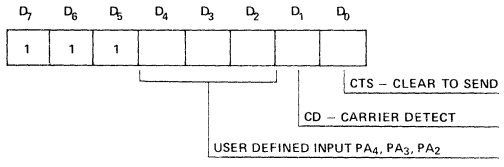
Modem Interface

The 8273 Modem interface provides both dedicated and user defined modem control functions. All the control signals are active low so that EIA RS-232C inverting drivers (MC 1488) and inverting receivers (MC 1489) may be used to interface to standard modems. For asynchronous operation, this interface supports programmable NRZI data encode/decode, a digital phase locked loop for efficient clock extraction from NRZI data, and modem control ports with automatic $\overline{\text{CTS}}$, $\overline{\text{CD}}$ monitoring and $\overline{\text{RTS}}$ generation. This interface also allows the 8273 to operate in PRE-FRAME SYNC mode in which the 8273 prefixes 16 transitions to a frame to synchronize idle lines before transmission of the first flag.

It should be noted that all the 8273 port operations deal with logical values, for instance, bit D0 of Port A will be a one when $\overline{\text{CTS}}$ (Pin 30) is a physical zero (logical one).

Port A — Input Port

During operation, the 8273 interrogates input pins $\overline{\text{CTS}}$ (Clear to Send) and $\overline{\text{CD}}$ (Carrier Detect). $\overline{\text{CTS}}$ is used to condition the start of a transmission. If during transmission $\overline{\text{CTS}}$ is lost the 8273 generates an interrupt. During reception, if $\overline{\text{CD}}$ is lost, the 8273 generates an interrupt.



The user defined input bits correspond to the 8273 PA_4, PA_3 and PA_2 pins. The 8273 does not interrogate or manipulate these bits.

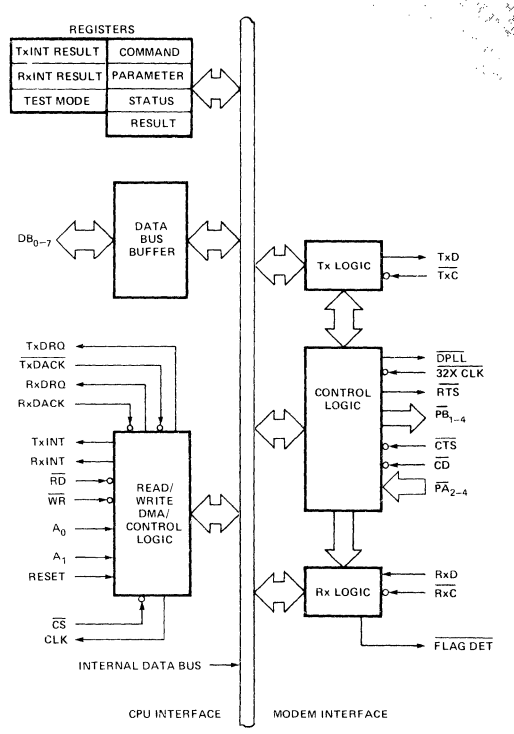
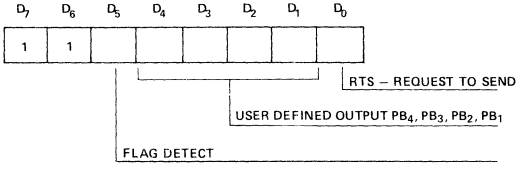


Figure 3. 8273 Block Diagram Showing Control Logic Functions

Port B - Output Port

During normal operation, if the CPU sets $\overline{\text{RTS}}$ active, the 8273 will not change this pin; however, if the CPU sets $\overline{\text{RTS}}$ inactive, the 8273 will activate it before each transmission and deactivate it one byte time after transmission. While the receiver is active the flag detect pin is pulsed each time a flag sequence is detected in the receive data stream. Following an 8273 reset, all pins of Port B are set to a high, inactive level.



The user defined output bits correspond to the state of PB_4-PB_1 pins. The 8273 does not interrogate or manipulate these bits.

Serial Data Logic

The Serial data is synchronized by the user transmit ($\overline{TxC}$) and receive ($\overline{RxC}$) clocks. The leading edge of $\overline{TxC}$ generates new transmit data and the trailing edge of $\overline{RxC}$ is used to capture receive data. The NRZI encoding/decoding of the receive and transmit data is programmable.

The diagnostic features included in the Serial Data logic are programmable loop back of data and selectable clock for the receiver. In the loop-back mode, the data presented to the TxD pin is internally routed to the receive data input circuitry in place of the RxD pin, thus allowing a CPU to send a message to itself to verify operation of the 8273.

In the selectable clock diagnostic feature, when the data is looped back, the receiver may be presented incorrect sample timing by the external circuitry. The user may select to substitute the $\overline{TxC}$ pin for the $\overline{RxC}$ input on-chip so that the clock used to generate the loop back data is used to sample it. Since TxD is generated off the leading edge of $\overline{TxC}$ and RxD is sampled on the trailing edge, the selected clock allows bit synchronism.

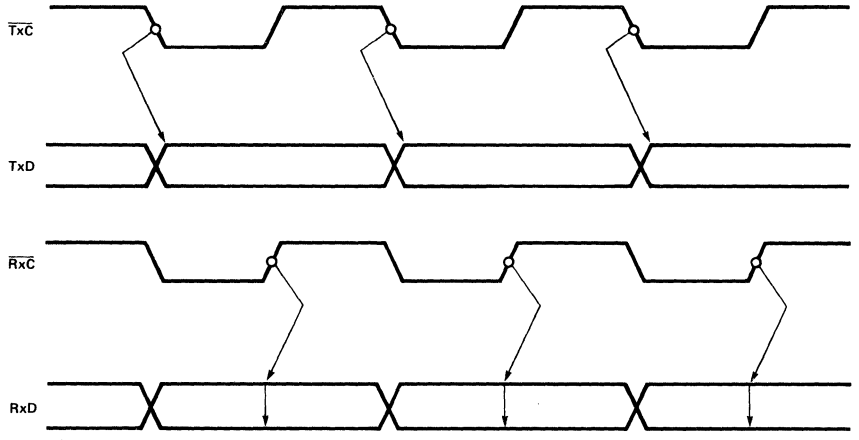


Figure 4. Transmit/Receive Timing

Asynchronous Mode Interface

Although the 8273 is fully compatible with the HDLC/SDLC communication line protocols, which are primarily designed for synchronous communication, the 8273 can also be used in asynchronous applications by using this interface. The interface employs a digital phase locked loop (DPLL) for clock recovery from a receive data stream and programmable NRZI encoding and decoding of data. The use of NRZI coding with SDLC transmission guarantees that within a frame, data transitions will occur at least every five bit times — the longest sequence of ones which may be transmitted without zero-bit insertion. The DPLL should be used only when NRZI coding is used since the NRZI coding will transmit zero sequence as line transitions. The digital phase locked loop also facilitates full-duplex and half-duplex asynchronous implementation with, or without modems.

Digital Phase Locked Loop

In asynchronous applications, the clock is derived from the receiver data stream by the use of the digital phase locked loop (DPLL). The DPLL requires a clock input at 32 times the required baud rate. The receive data (RxD) is sampled with this $\overline{32X\ CLK}$ and the 8273 DPLL supplies a sample pulse nominally centered on the RxD bit cells. The DPLL has a built-in "stiffness" which reduces sensitivity to line noise and bit distortion. This is accomplished by making phase error adjustments in discrete increments. Since the nominal pulse is made to occur at 32 counts of the $\overline{32X\ CLK}$, these counts are subtracted or added to the nominal, depending upon which quadrant of the four error quadrants the data edge occurs in. For example if an RxD edge is detected in quadrant A1, it is apparent that the $\overline{DPLL}$ sample "A" was placed too close to the trailing edge of the data cell; sample "B" will then be placed at T = ($T_{nominal}$ - 2 counts)$_l$ = 30 counts of the $\overline{32X\ CLK}$ to move the sample pulse "B" toward the nominal center of the next bit cell. A data edge occuring in quadrant B1 would cause a smaller adjustment of phase with T = 31 counts of the $\overline{32X\ CLK}$. Using this technique the $\overline{DPLL}$ pulse will converge to nominal bit center within 12 data bit times, worst case, with constant incoming RxD edges.

A method of attaining bit synchronism following a line idle is to use PRE-FRAME SYNC mode of transmission.

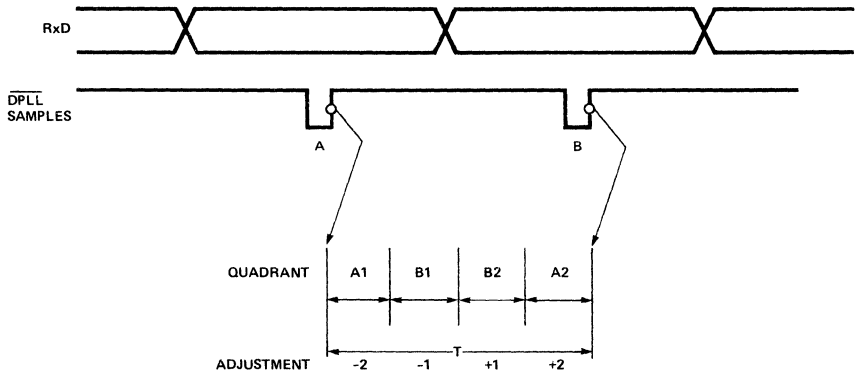
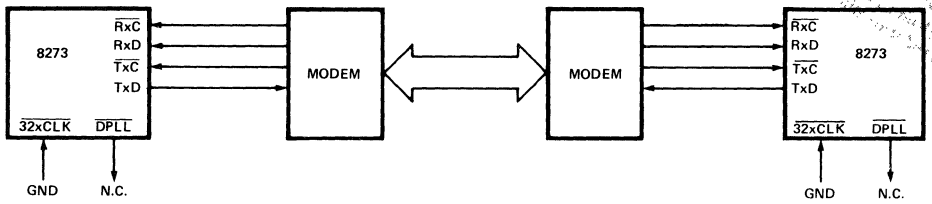
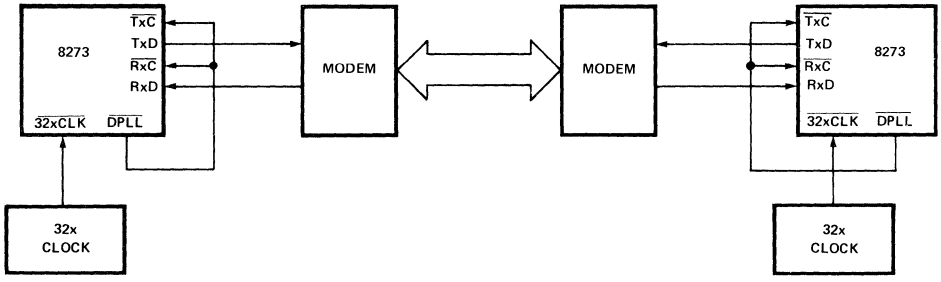


Figure 5. DPLL Sample Timing

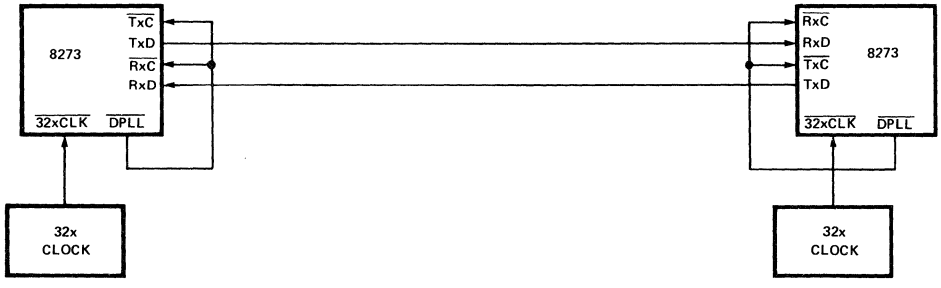
Synchronous Modem — Duplex or Half Duplex Operation



Asynchronous Modems — Duplex or Half Duplex Operation



Asynchronous — No Modems — Duplex or Half Duplex



SDLC Loop

The DPLL simplifies the SDLC loop station implementation. In this application, each secondary station on a loop data link is a repeater set in one-bit delay mode. The signals sent out on the loop by the loop controller (primary station) are relayed from station to station then, back to the controller. Any secondary station finding its address in the A field captures the frame for action at that station. All received frames are relayed to the next station on the loop.

Loop stations are required to derive bit timing from the incoming NRZI data stream. The DPLL generates sample Rx clock timing for reception and uses the same clock to implement Tx clock timing.

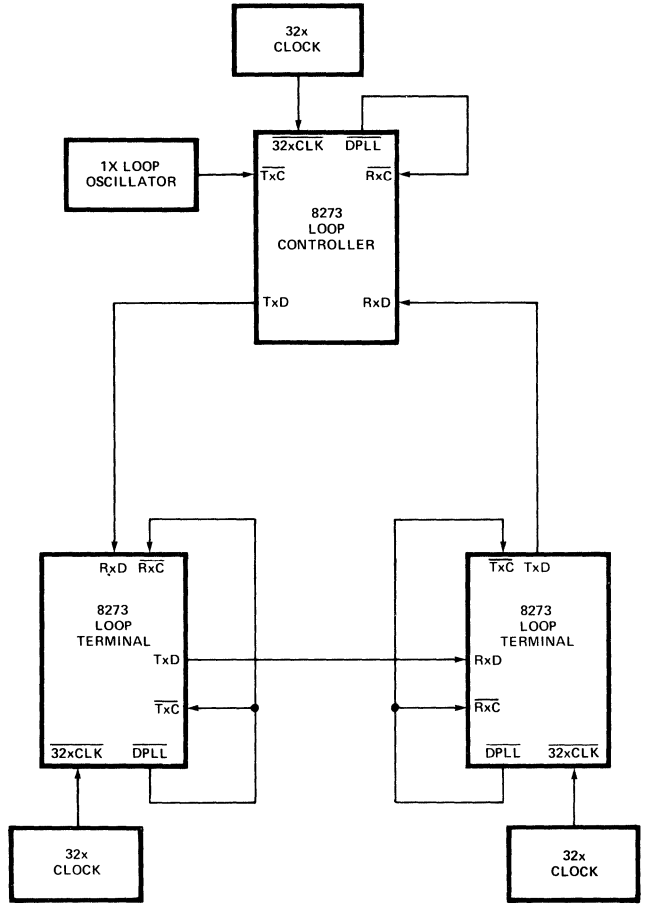
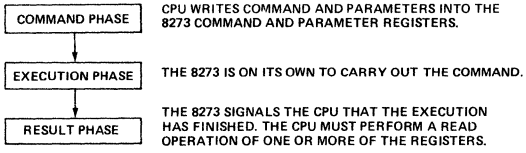


Figure 6. SDLC Loop Application

PRINCIPLES OF OPERATION

The 8273 is an intelligent peripheral controller which relieves the CPU of many of the rote tasks associated with constructing and receiving frames. It is fully compatible with the MCS-80/85™ system bus. As a peripheral device, it accepts commands from a CPU, executes these commands and provides an Interrupt and Result back to the CPU at the end of the execution. The communication with the CPU is done by activation of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ pins, while the A_1, A_0 select the appropriate registers on the chip as described in the Hardware Description Section.

The 8273 operation is composed of the following sequence of events:



The Command Phase

During the command phase, the software writes a command to the command register. The command bytes provide a general description of the type of operation requested. Many commands require more detailed information about the command. In such a case up to four parameters are written into the parameter register. The flowchart of the command phase indicates that a command may not be issued if the Status Register indicates that the device is busy. Similarly if a parameter is issued when the Parameter Buffer shows full, incorrect operation will occur.

The 8273 is a duplex device and both transmitter and receiver may each be executing a command or passing results at any given time. For this reason separate interrupt pins are provided. However, the command register must be used for one command sequence at a time.

Status Register

The status register contains the status of the 8273 activity. The description is as follows.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CBSY	CBF	CPBF	CRBF	RxINT	TxINT	RxIRA	TxIRA

Bit 7 CBSY (Command Busy)

Indicates in-progress command, set for CPU poll when Command Register is full, reset upon command phase completion. It is improper to write a command when CBSY is set; it results in incorrect operation.

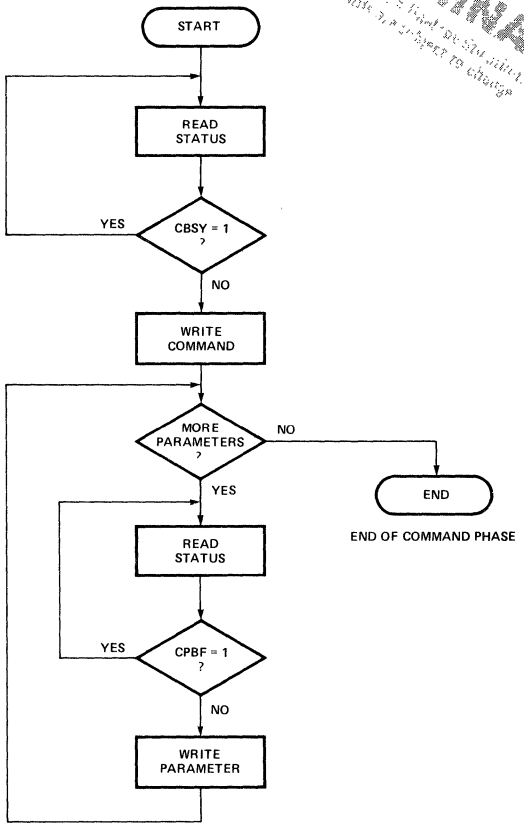


Figure 7. Command Phase Flowchart

Bit 6 CBF (Command Buffer Full)

Indicates that the command register is full, it is reset when the 8273 accepts the command byte but does not imply that execution has begun.

Bit 5 CPBF (Command Parameter Buffer Full)

CPBF is set when the parameter buffer is full, and is reset by the 8273 when it accepts the parameter. The CPU may poll CPBF to determine when additional parameters may be written.

Bit 4 CRBF (Command Result Buffer Full)

Indicates that an executed command immediate result is present in the Result Register. It is set by 8273 and reset when CPU reads the result.

Bit 3 RxINT (Receiver Interrupt)

RxINT indicates that the receiver requires CPU attention. It is identical to RxINT (pin 11) and is set by the 8273 either upon good/bad completion of a specified command or by Non-DMA data transfer. It is reset only after the CPU has read the result byte or has received a data byte from the 8273 in a Non-DMA data transfer.

Bit 2 TxINT (Transmitter Interrupt)

The TxINT indicates that the transmitter requires CPU attention. It is identical to TxINT (pin 2). It is set by 8273 either upon good/bad completion of a specified command or by Non-DMA data transfer. It is reset only after the CPU has read the result byte or has transferred transmit data byte to the 8273 in a Non-DMA transfer.

Bit 1 RxIRA (Receiver Interrupt Result Available)

The RxIRA is set by the 8273 when an interrupt result byte is placed in the RxINT register. It is reset after the CPU has read the RxINT register.

Bit 0 TxIRA (Transmitter Interrupt Result Available)

The TxIRA is set by the 8273 when an interrupt result byte is placed in the TxINT register. It is reset when the CPU has read the TxINT register.

The Execution Phase

Upon accepting the last parameter, the 8273 enters into the Execution Phase. The execution phase may consist of a DMA or other activity, and may or may not require CPU intervention. The CPU intervention is eliminated in this phase if the system utilizes DMA for the data transfers, otherwise, for non-DMA data transfers, the CPU is interrupted by the 8273 via TxINT and RxINT pins, for each data byte request.

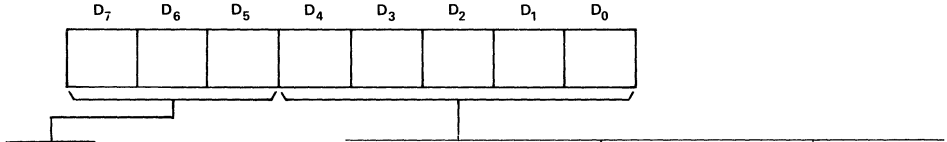
The Result Phase

During the result phase, the 8273 notifies the CPU of the execution outcome of a command. This phase is initiated by:

1. The successful completion of an operation
2. An error detected during an operation.

To facilitate quick network software decisions, two types of execution results are provided:

1. An Immediate Result
2. A Non-Immediate Result

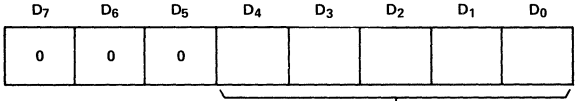


D_7	D_6	D_5	
1	1	1	All 8 bits received
0	0	0	D_0 received
1	0	0	D_1-D_0 received
0	1	0	D_2-D_0 received
1	1	0	D_3-D_0 received
0	0	1	D_4-D_0 received
1	0	1	D_5-D_0 received
0	1	1	D_6-D_0 received

*Partial Byte Received

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Receiver Interrupt Result Code	Rx Status After INT
*	*	*	0	0	0	0	0	A_1 match or general receive	Active
*	*	*	0	0	0	0	1	A_2 match	Active
0	0	0	0	0	0	1	1	CRC error	Active
0	0	0	0	0	0	1	0	Abort detected	Active
0	0	0	0	0	1	0	1	Idle detect	Disabled
0	0	0	0	0	1	1	0	EOP detected	Disabled
0	0	0	0	0	1	1	1	Frame less than 32 bits	Active
0	0	0	0	1	0	0	0	DMA overrun detected	Disabled
0	0	0	0	1	0	0	1	Memory buffer overflow	Disabled
0	0	0	0	1	0	1	0	Carrier detect failure	Disabled
0	0	0	0	1	0	1	1	Receive interrupt overrun	Disabled

Figure 8. Rx Interrupt Result Byte Format



D_4	D_3	D_2	D_1	D_0	
0	1	1	0	0	Early transmit interrupt
0	1	1	0	1	Frame transmit complete
0	1	1	1	0	DMA underrun
0	1	1	1	1	Clear to Send (CTS) error
1	0	0	0	0	Abort complete

Figure 10. Tx Interrupt Result Byte Format

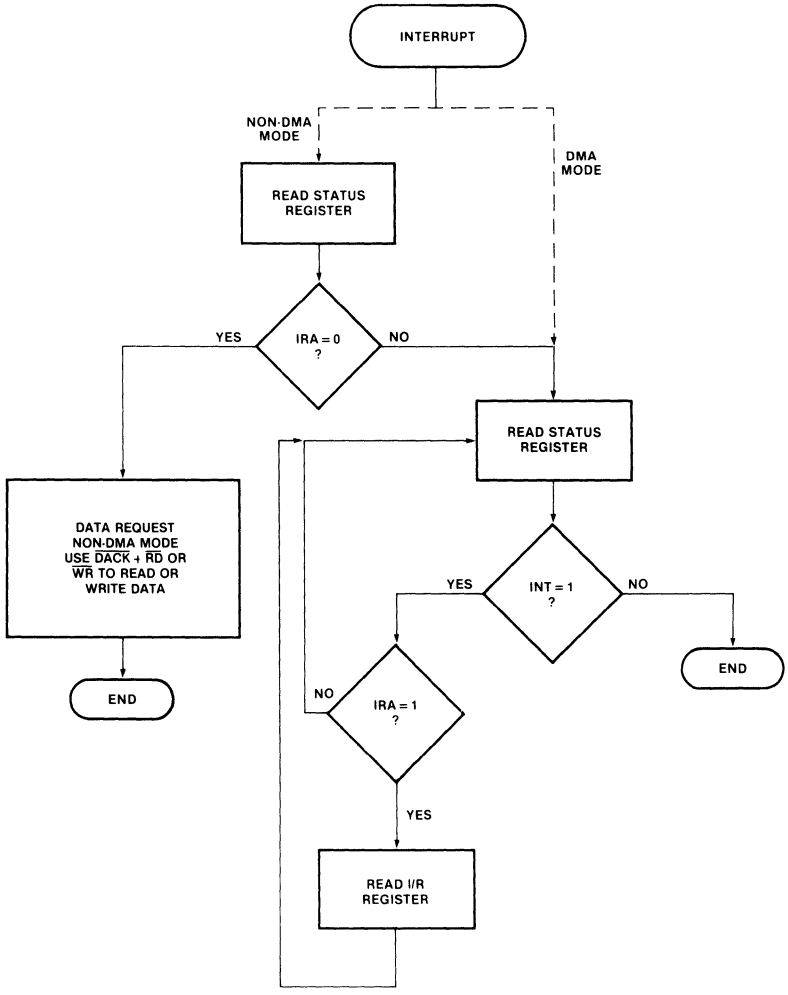
Immediate result is provided by the 8273 for commands such as Read Port A and Read Port B which have information ($\overline{CTS}$, $\overline{CD}$, $\overline{RTS}$, etc.) that the network software needs to make quick operational decisions.

A command which cannot provide an immediate result will generate an interrupt to signal the beginning of the Result phase. The immediate results are provided in the Result Register; all non-immediate results are available upon device interrupt, through Tx Interrupt Result Register TxI/R or Rx Interrupt Result Register RxI/R. The result may consist of a one-byte interrupt code indicating the condition for the interrupt and, if required, one or more bytes which detail the condition.

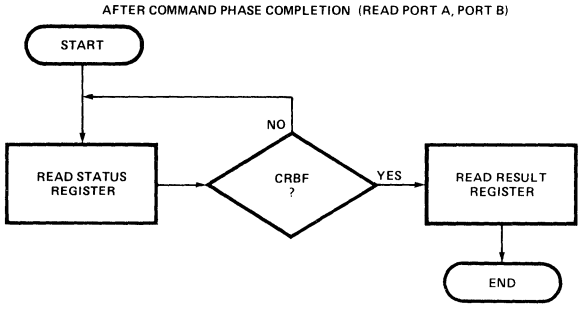
Tx and Rx Interrupt Result Registers

The Result Registers have a result code, the three high order bits D_7-D_5 of which are set to zero for all but the receive command. This command result contains a count that indicates the number of bits received in the last byte. If a partial byte is received, the high order bits of the last data byte are indeterminate.

All results indicated in the command summary must be read during the result phase.



RESULT PHASE FLOWCHART — INTERRUPT RESULTS



RESULT PHASE FLOWCHART — IMMEDIATE RESULTS

Figure 9. Rx Interrupt Service

DETAILED COMMAND DESCRIPTION

General

The 8273 HDLC/SDLC controller supports a comprehensive set of high level commands which allows the 8273 to be readily used in full-duplex, half-duplex, synchronous, asynchronous and SDLC loop configuration, with or without modems. These frame-level commands minimize CPU and software overhead. The 8273 has address and control byte buffers which allow the receive and transmit commands to be used in buffered or non-buffered modes.

In buffered transmit mode, the 8273 transmits a flag automatically, reads the Address and Control buffer registers and transmits the fields, then via DMA, it fetches the information field. The 8273, having transmitted the information field, automatically appends the Frame Check Sequence (FCS) and the end flag. Correspondingly, in buffered read mode, the Address and Control fields are stored in their respective buffer registers and only Information Field is transferred to memory.

In non-buffered transmit mode, the 8273 transmits the beginning flag automatically, then fetches and transmits the Address, Control and Information fields from the memory, appends the FCS character and an end flag. In the non-buffered receive mode the entire contents of a frame are sent to memory with the exception of the flags and FCS.

HDLC Implementation

HDLC Address and Control field are extendable. The extension is selected by setting the low order bit of the field to be extended to a one, a zero in the low order bit indicates the last byte of the respective field.

Since Address/Control field extension is normally done with software to maximize extension flexibility, the 8273 does not create or operate upon contents of the extended HDLC Address/Control fields. Extended fields are transparently passed by the 8273 to user as either interrupt results or data transfer requests. Software must assemble the fields for transmission and interrogate them upon reception.

However, the user can take advantage of the powerful 8273 commands to minimize CPU/Software overhead and simplify buffer management in handling extended fields. For instance buffered mode can be used to separate the first two bytes, then interrogate the others from buffer. Buffered mode is perfect for a two byte address field.

The 8273 when programmed, recognizes protocol characters unique to HDLC such as Abort, which is a string of seven or more ones (01111111). Since Abort character is the same as the GA (EOP) character used in SDLC Loop applications, Loop Transmit and Receive commands are not recommended to be used in HDLC. HDLC does not support Loop mode.

Initialization Set/Reset Commands

These commands are used to manipulate data within the 8273 registers. The Set commands have a single parameter which is a mask that corresponds to the bits to be set. (They perform a logical-OR of the specified register with the mask provided as a parameter). The Register commands have a single parameter which is a mask that has a zero in the bit positions that are to be reset. (They perform a logical-AND of the specified register with the mask).

Set One-Bit Delay (CMD Code A4)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	0	1	0	0	1	0	0
PAR:	0	1	1	0	0	0	0	0	0	0

When one bit delay is set, 8273 retransmits the received data stream one bit delayed. This mode is entered at a receiver character boundary, and should only be used by Loop Stations.

Reset One-Bit Delay (CMD Code 64)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	1	1	0	0	1	0	0
PAR:	0	1	0	1	1	1	1	1	1	1

The 8273 stops the one bit delayed retransmission mode.

Set Data Transfer Mode (CMD Code 97)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	0	0	1	0	1	1	1
PAR:	0	1	0	0	0	0	0	0	0	1

When the data transfer mode is set, the 8273 will interrupt when data bytes are required for transmission or are available from a receive. If a transmit interrupt occurs and the status indicates that there is no Transmit Result (TxIRA = 0), the interrupt is a transmit data request. If a receive interrupt occurs and the status indicates that there is no receive result (RxIRA = 0), the interrupt is a receive data request.

Reset Data Transfer Mode (CMD Code 57)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	1	0	1	0	1	1	1
PAR:	0	1	1	1	1	1	1	1	1	0

If the Data Transfer Mode is reset, the 8273 data transfers are performed through the DMA requests without interrupting the CPU.

Set Operating Mode (CMD Code 91)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	0	0	1	0	0	0	1
PAR:	0	1	0	0						

1 = FLAG STREAM MODE
1 = PREFRAME SYNC MODE
1 = BUFFERED MODE
1 = EARLY INTERRUPT MODE
1 = EOP INTERRUPT MODE
1 = HDLC MODE

Reset Operating Mode (CMD Code 51)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	1	0	1	0	0	0	1
PAR:	0	1	1	1						

Any mode switches set in CMD code 91 can be reset using this command by placing zeros in the appropriate positions.

(D5) HDLC Mode

In HDLC mode, a bit sequence of seven ones (01111111) is interpreted as an abort character. Otherwise, eight ones (011111111) signal an abort.

(D4) EOP Interrupt Mode

In EOP interrupt mode, an interrupt is generated whenever an EOP character (01111111) is detected by an active receiver. This mode is useful for the implementation of an SDLC loop controller in detecting the end of a message stream after a loop poll.

(D3) Transmitter Early Interrupt Mode (Tx)

The early interrupt mode is specified to indicate when the 8273 should generate an end of frame interrupt. When set, an early interrupt is generated when the last data character has been passed to the 8273. If the user software responds with another transmit command before the final flag is sent, the final flag interrupt will not be generated and a new frame will immediately begin when the current frame is complete. This permits frames to be separated by a single flag. If no additional Tx commands are provided, a final interrupt will follow.

If this bit is zero, the interrupt will be generated only after the final flag has been transmitted.

(D2) Buffered Mode

If the buffered mode bit is set to a one, the first two bytes (normally the address (A) and control (C) fields) of a frame are buffered by the 8273. If this bit is a zero the address and control fields are passed to and from memory.

(D1) Preframe Sync Mode

If this bit is set to a one the 8273 will transmit two characters before the first flag of a frame.
To guarantee sixteen line transitions, the 8273 sends two bytes of data $(00)_H$ if NRZI is set or data $(55)_H$ if NRZI is not set.

(D0) Flag Stream Mode

If this bit is set to a one, the following table outlines the operation of the transmitter.

TRANSMITTER STATE	ACTION
Idle	Send Flags immediately.
Transmit or Transmit-Transparent Active	Send Flags after the transmission complete
Loop Transmit Active	Ignore command.
1 Bit Delay Active	Ignore command.

If this bit is reset to zero the following table outlines the operation of the transmitter.

TRANSMITTER STATE	ACTION
IDLE	Send Idles on next character boundary.
Transmit or Transmit-Transparent Active	Send Idles after the transmission is complete.
Loop Transmit Active	Ignore command.
1 Bit Delay Active	Ignore command.

Set Serial I/O Mode (CMD Code A0)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	0	1	0	0	0	0	0
PAR:	0	1	0	0	0	0	0			

1 = NRZ1 MODE
1 = TxC → RxC
1 = LOOP BACK TxD → RxD

Reset Serial I/O Mode (CMD Code 60)

This command allows bits set in CMD code A0 to be reset by placing zeros in the appropriate positions.

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	1	1	0	0	0	0	0
PAR:	0	1	1	1	1	1	1			

(D2) Loop Back

If this bit is set to a one, the transmit data is internally routed to the receive data circuitry.

(D1) TxC → RxC

If this bit is set to a one, the transmit clock is internally routed to the receive clock circuitry. It is normally used with the loop back bit (D2).

(D0) NRZI Mode

If this bit is set to a one, NRZI encoding and decoding of transmit and receive data is provided. If this bit is a zero, the transmit and receive data is treated as a normal positive logic bit stream.

NRZI encoding specifies that a zero causes a change in the polarity of the transmitted signal and a one causes no polarity change. NRZI is used in all asynchronous operations. Refer to IBM document GA27-3093 for details.

Reset Device Command

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
TMR:	1	0	0	0	0	0	0	0	0	1
TMR:	1	0	0	0	0	0	0	0	0	0

An 8273 reset command is executed by outputing a $(01)_H$ followed by $(00)_H$ to the reset register (TMR). See 8273 AC timing characteristics for Reset pulse specifications.

The reset command emulates the action of the reset pin.

1. The modem control signals are forced high (inactive level).
2. The 8273 status register flags are cleared.
3. Any commands in progress are terminated immediately.
4. The 8273 enters an idle state until the next command is issued.
5. The Serial I/O and Operating Mode registers are set to zero and DMA data register transfer mode is selected.
6. The device assumes a non-loop SDLC terminal role.

Receive Commands

The 8273 supports three receive commands: General Receive, Selective Receive, and Selective Loop Receive.

General Receive (CMD Code C0)

General receive is a receive mode in which frames are received regardless of the contents of the address field.

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
CMD:	0	0	1	1	0	0	0	0	0	0	
PAR:	0	1	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)								
PAR:	0	1	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH (B1)								

NOTES:

1. If buffered mode is specified, the R0, R1 receive frame length (result) is the number of data bytes received.
2. If non-buffered mode is specified, the R0, R1 receive frame length (result) is the number of data bytes received plus two (the count includes the address and control bytes).
3. The frame check sequence (FCS) is not transferred to memory.
4. Frames with less than 32 bits between flags are ignored (no interrupt generated) if the buffered mode is specified.
5. In the non-buffered mode an interrupt is generated when a less than 32 bit frame is received, since data transfer requests have occurred.
6. The 8273 receiver is always disabled when an Idle is received after a valid frame. The CPU module must issue a receive command to re-enable the receiver.
7. The intervening ABORT character between a final flag and an IDLE does not generate an interrupt.
8. If an ABORT Character is not preceded by a flag and is followed by an IDLE, an interrupt will be generated for the ABORT followed by an IDLE interrupt one character time later. The reception of an ABORT will disable the receiver.

Selective Receive (CMD Code C1)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
CMD:	0	0	1	1	0	0	0	0	0	1	
PAR:	0	1	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)								
PAR:	0	1	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH (B1)								
PAR:	0	1	RECEIVE FRAME ADDRESS MATCH FIELD ONE (A1)								
PAR:	0	1	RECEIVE FRAME ADDRESS MATCH FIELD TWO (A2)								

Selective receive is a receive mode in which frames are ignored unless the address field matches any one of two address fields given to the 8273 as parameters.

When selective receive is used in HDLC the 8273 looks at the first character, if extended, software must then decide if the message is for this unit.

Selective Loop Receive (CMD Code C2)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
CMD:	0	0	1	1	0	0	0	0	1	0	
PAR:	0	0	LEAST SIGNIFICANT BYTE OF THE RECEIVE BUFFER LENGTH (B0)								
PAR:	0	1	MOST SIGNIFICANT BYTE OF RECEIVE BUFFER LENGTH (B1)								
PAR:	0	1	RECEIVE FRAME ADDRESS MATCH FIELD ONE (A1)								
PAR:	0	1	RECEIVE FRAME ADDRESS MATCH FIELD TWO (A2)								

Selective loop receive operates like selective receive except that the transmitter is placed in flag stream mode automatically after detecting an EOP (01111111) following a valid received frame. The one bit delay mode is also reset at the end of a selective loop receive.

Receive Disable (CMD Code C5)

Terminates an active receive command immediately.

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	0	1	0	1
PAR: NONE										

Transmit Commands

The 8273 supports three transmit commands: Transmit Frame, Loop Transmit, Transmit Transparent.

Transmit Frame (CMD Code C8)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	0	0	0
PAR:	0	1	LEAST SIGNIFICANT BYTE OF FRAME LENGTH (L0)							
PAR:	0	1	MOST SIGNIFICANT BYTE OF FRAME LENGTH (L1)							
PAR:	0	1	ADDRESS FIELD OF TRANSMIT FRAME (A)							
PAR:	0	1	CONTROL FIELD OF TRANSMIT FRAME (C)							

Transmits one frame including: initial flag, frame check sequence, and the final flag.

If the buffered mode is specified, the L0, L1, frame length provided as a parameter is the length of the information field and the address and control fields must be input.

In unbuffered mode the frame length provided must be the length of the information field plus two and the address and control fields must be the first two bytes of data. Thus only the frame length bytes are required as parameters.

Loop Transmit (CMD Code CA)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	0	1	0
PAR:	0	1	LEAST SIGNIFICANT BYTE OF FRAME LENGTH (L0)							
PAR:	0	1	MOST SIGNIFICANT BYTE OF FRAME LENGTH (L1)							
PAR:	0	1	ADDRESS FIELD OF TRANSMIT FRAME (A)							
PAR:	0	1	CONTROL FIELD OF TRANSMIT FRAME (C)							

Transmits one frame in the same manner as the transmit frame command except:

1. This command should be given only in one-bit delay mode.
2. If the flag stream mode is not active transmission will begin after a received EOP has been converted to a flag.
3. If the flag stream mode is active transmission will begin at the next flag boundary for buffered mode or at the third flag boundary for non-buffered mode.
4. At the end of a loop transmit the one-bit delay mode is entered and the flag stream mode is reset.

Transmit Transparent (CMD Coded C9)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	0	0	1
PAR:	0	1	LEAST SIGNIFICANT BYTE OF FRAME LENGTH (L0)							
PAR:	0	1	MOST SIGNIFICANT BYTE OF FRAME LENGTH (L1)							

The 8273 will transmit a block of raw data without protocol, i.e., no zero bit insertion, flags, or frame check sequences.

Abort Transmit Commands

An abort command is supported for each type of transmit command. The abort commands are ignored if a transmit command is not in progress.

Abort Transmit Frame (CMD Code CC)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	1	0	0

PAR: NONE

After an abort character (eight contiguous ones) is transmitted, the transmitter reverts to sending flags or idles as a function of the flag stream mode specified.

Abort Loop Transmit (CMD Code CE)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	1	1	0

PAR: NONE

After a flag is transmitted the transmitter reverts to one bit delay mode.

Abort Transmit Transparent (CMD Code CD)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	1	0	0	1	1	0	1

PAR: NONE

The transmitter reverts to sending flags or idles as a function of the flag stream mode specified.

Modem Control Commands

The modem control commands are used to manipulate the modem control ports.

When read Port A or Port B commands are executed the result of the command is returned in the result register. The Bit Set Port B command requires a parameter that is a mask that corresponds to the bits to be set. The Bit Reset Port B command requires a mask that has a zero in the bit positions that are to be reset.

Read Port A (CMD Code 22)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	0	1	0	0	0	1	0

PAR: NONE

Read Port B (CMD Code 23)

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	0	1	0	0	0	1	1

PAR: NONE

Set Port B Bits (CMD Code A3)

This command allows user defined Port B pins to be set.

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	1	0	1	0	0	0	1	1
PAR:	0	1	0	0						

RTS – REQUEST TO SEND
USER DEFINED
FLAG DETECT

(D_5) Flag Detect

This bit can be used to set the flag detect pin. However, it will be reset when the next flag is detected.

(D_4-D_1) User Defined Outputs

These bits correspond to the state of the PB_4-PB_1 output pins.

(D_0) Request to Send

This is a dedicated 8273 modem control signal, and reflects the same logical state of RTS pin.

Reset Port B Bits (CMD Code 63)

This command allows Port B user defined bits to be reset.

	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CMD:	0	0	0	1	1	0	0	0	1	1
PAR:	0	1	1	1						

RTS – REQUEST TO SEND
USER DEFINED
FLAG DETECT

This command allows Port B (D_4-D_1) user defined bits to be reset. These bits correspond to Output Port pins (PB_4-PB_1).

8273 Command Summary

Command Description	Command (HEX)	Parameter	Results	Result Port	Completion Interrupt
Set One Bit Delay	A4	Set Mask	None	—	No
Reset One Bit Delay	64	Reset Mask	None	—	No
Set Data Transfer Mode	97	Set Mask	None	—	No
Reset Data Transfer Mode	57	Reset Mask	None	—	No
Set Operating Mode	91	Set Mask	None	—	No
Reset Operating Mode	51	Reset Mask	None	—	No
Set Serial I/O Mode	A0	Set Mask	None	—	No
Reset Serial I/O Mode	60	Reset Mask	None	—	No
General Receive	C0	B0,B1	RIC,R0,R1,(A,C)[2]	RXI/R	Yes
Selective Receive	C1	B0,B1,A1,A2	RIC,R0,R1,(A,C)[2]	RXI/R	Yes
Selective Loop Receive	C2	B0,B1,A1,A2	RIC,R0,R1,(A,C)[2]	RXI/R	Yes
Receive Disable	C5	None	None	—	No
Transmit Frame	C8	L0,L1,(A,C)[1]	TIC	TXI/R	Yes
Loop Transmit	CA	L0,L1,(A,C)[1]	TIC	TXI/R	Yes
Transmit Transparent	C9	L0,L1	TIC	TXI/R	Yes
Abort Transmit Frame	CC	None	TIC	TXI/R	Yes
Abort Loop Transmit	CE	None	TIC	TXI/R	Yes
Abort Transmit Transparent	CD	None	TIC	TXI/R	Yes
Read Port A	22	None	Port Value	Result	No
Read Port B	23	None	Port Value	Result	No
Set Port B Bit	A3	Set Mask	None	—	No
Reset Port B Bit	63	Reset Mask	None	—	No

Notes: 1. Issued only when in buffered mode. 2. Read as results only in buffered mode.

8273 Command Summary Key

B0 — Least significant byte of the receive buffer length.
B1 — Most significant byte of the receive buffer length.
L0 — Least significant byte of the Tx frame length.
L1 — Most significant byte of the Tx frame length.
A1 — Receive frame address match field one.
A2 — Receive frame address match field two.
A — Address field of received frame. If non-buffered mode is specified, this result is not provided.
C — Control field of received frame. If non-buffered mode is specified this result is not provided.
RXI/R — Receive interrupt result register.
TXI/R — Transmit interrupt result register.
R0 — Least significant byte of the length of the frame received.
R1 — Most significant byte of the length of the frame received.
RIC — Receiver interrupt result code.
TIC — Transmitter interrupt result code.

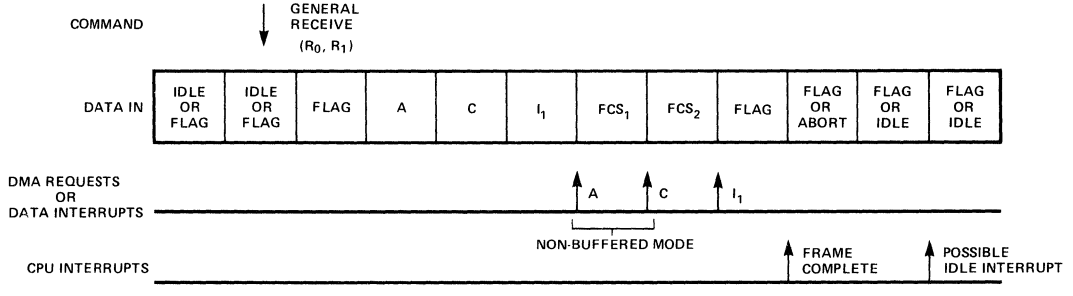


Figure 12. Typical Frame Reception

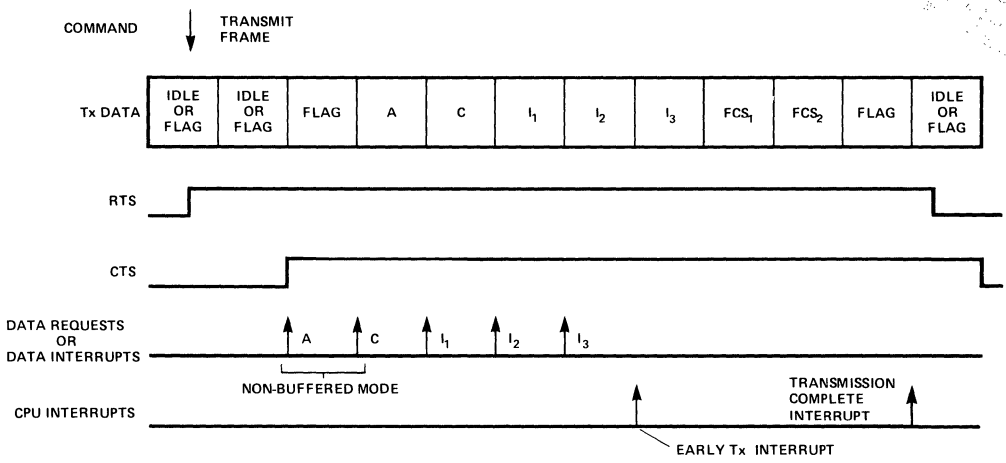


Figure 13. Typical Frame Transmission

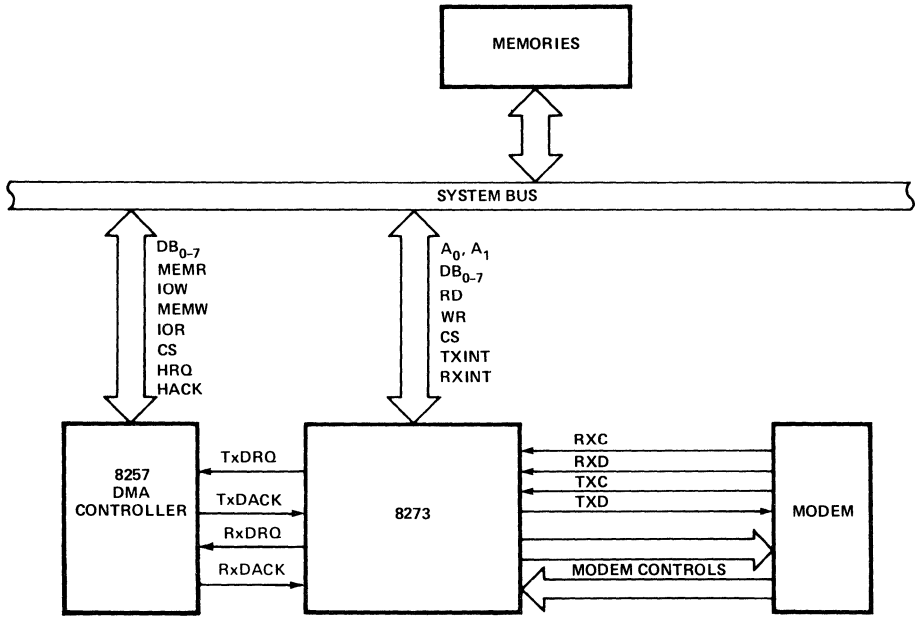


Figure 14. 8273 System Diagram

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With Respect to Ground ..... -0.5V to +7V
Power Dissipation ..... 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5.0V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA for Data Bus pins I_{OL} = 1.7 mA for all other pins
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −200 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OZ}	Off-State Output Current		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		180	mA	

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	t_c = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured Pins Returned to GND

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = +5.0V \pm 5\%$

Read Cycle

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AC}	Select Setup to $\overline{RD}$	0		ns	Note 3
t_{CA}	Select Hold from $\overline{RD}$	0		ns	Note 3
t_{RR}	RD Pulse Width	0		ns	
t_{AD}	Data Delay from Address		250	ns	Note 3
t_{RD}	Data Delay from $\overline{RD}$		150	ns	$C_L = 150$ pF, Note 3
t_{DF}	Output Float Delay	20	100	ns	$C_L = 20$ pF for Minimum; 150 pF for Maximum
t_{DC}	DACK Setup to $\overline{RD}$	25		ns	
t_{CD}	DACK Hold from $\overline{RD}$	25		ns	
t_{KD}	Data Delay from DACK		250	ns	

Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AC}	Select Setup to $\overline{WR}$	0		ns	
t_{CA}	Select Hold from $\overline{WR}$	0		ns	
t_{WW}	$\overline{WR}$ Pulse Width	250		ns	
t_{DW}	Data Setup to $\overline{WR}$	150		ns	
t_{WD}	Data Hold from $\overline{WR}$	0		ns	
t_{DC}	DACK Setup to $\overline{WR}$	25		ns	
t_{CD}	DACK Hold from $\overline{WR}$	25		ns	

DMA

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CQ}	Request Hold from $\overline{WR}$ or $\overline{RD}$ (for Non-Burst Mode)		150	ns	

Other Timing

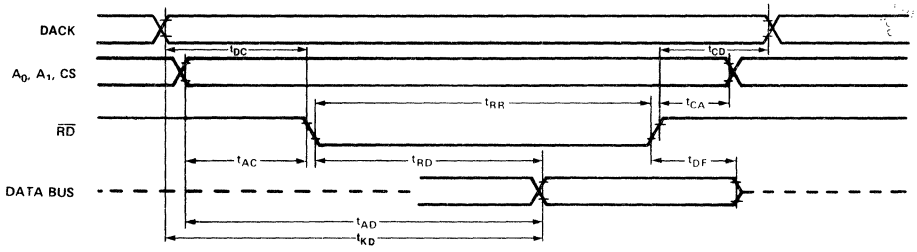
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{RSTW}	Reset Pulse Width	10		t_{CY}	
t_r	Input Signal Rise Time		20	ns	
t_f	Input Signal Fall Time		20	ns	
t_{RSTS}	Reset to First $\overline{IOWR}$	2		t_{CY}	
t_{CY}	Clock	250		ns	Note 2
t_{CL}	Clock Low	110		ns	
t_{CH}	Clock High	122		ns	
t_{DCL}	Data Clock Low	200		ns	
t_{DCH}	Data Clock High	200		ns	
t_{DCY}	Data Clock	15625		ns	Note 2
t_{TD}	Transmit Data Delay		100	ns	
t_{DS}	Data Setup Time	100		ns	
t_{DH}	Data Hold Time	0		ns	
t_{DPLL}	$\overline{DPLL}$ Output Low	200		ns	
t_{FLD}	$\overline{FLAG\ DET}$ Output Low	$8 \cdot t_{CY} \pm 50$		ns	

NOTES:

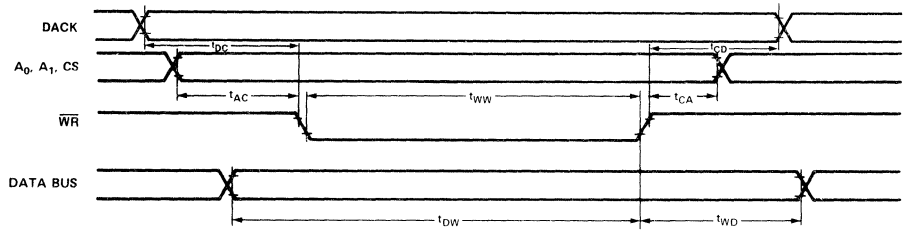
1. All timing measurements are made at the reference voltages unless otherwise specified: Input "1" at 2.0V, "0" at 0.8V
   Output "1" at 2.0V, "0" at 0.8V
2. 64K baud maximum operating rate.
3. t_{AD}, t_{RD}, t_{AC}, and t_{CA} are not concurrent specs.

WAVEFORMS

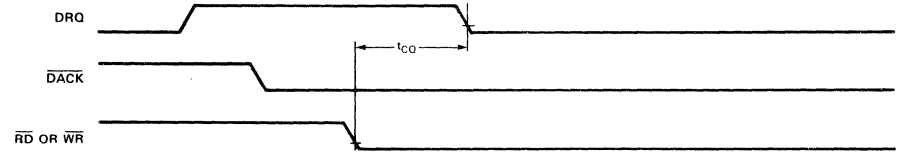
Read Waveforms

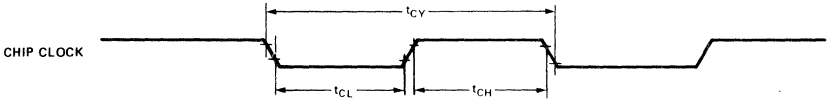


Write Waveforms

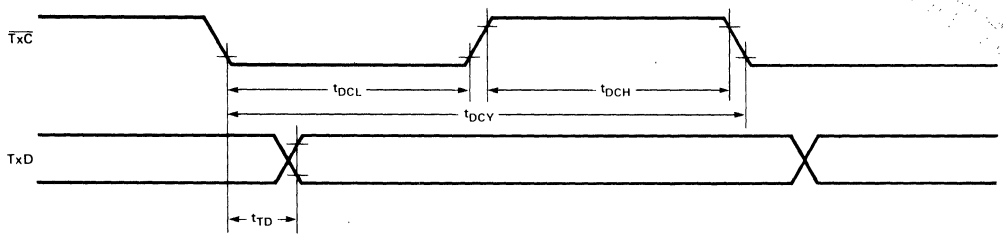


DMA Waveforms

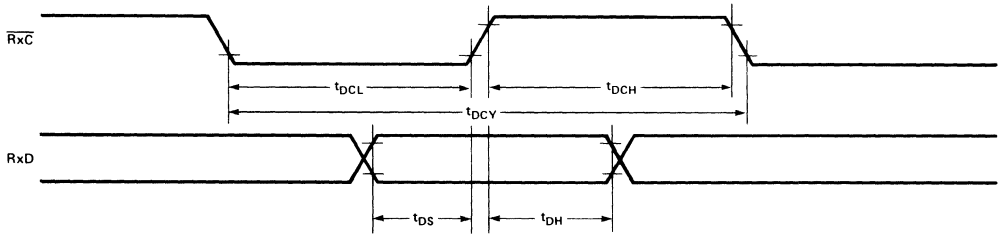




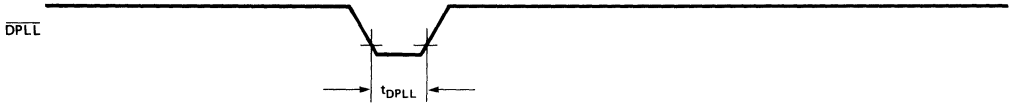
Transmit Data Waveforms



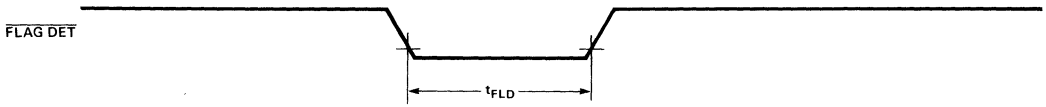
Receive Data Waveforms



DPLL Output Waveform



Flag Detect Output Waveform

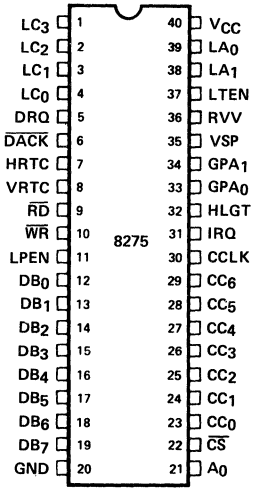


8275
PROGRAMMABLE CRT CONTROLLER

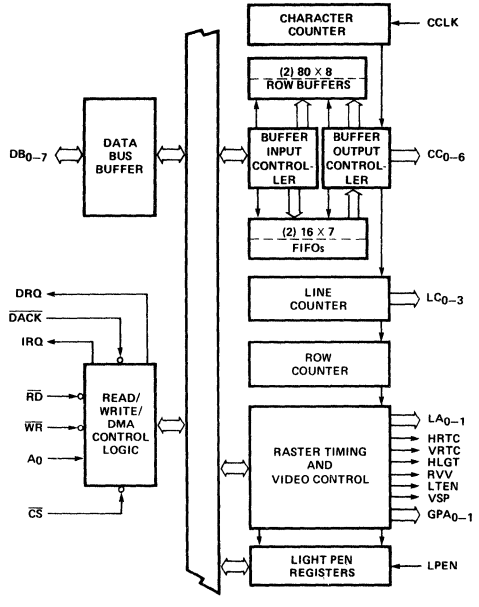
- **Programmable Screen and Character Format**
- **6 Independent Visual Field Attributes**
- **11 Visual Character Attributes (Graphic Capability)**
- **Cursor Control (4 Types)**
- **Light Pen Detection and Registers**
- **Fully MCS-80™ and MCS-85™ Compatible**
- **Dual Row Buffers**
- **Programmable DMA Burst Mode**
- **Single +5V Supply**
- **40-Pin Package**

The Intel® 8275 Programmable CRT Controller is a single chip device to interface CRT raster scan displays with Intel® microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the 8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

DB_{0-1}	BI-DIRECTIONAL DATA BUS	LC_{0-3}	LINE COUNTER OUTPUTS
DRQ	DMA REQUEST OUTPUT	LA_{0-1}	LINE ATTRIBUTE OUTPUTS
$\overline{DACK}$	DMA ACKNOWLEDGE INPUT	HRTC	HORIZONTAL RETRACE OUTPUT
IRQ	INTERRUPT REQUEST OUTPUT	VRTC	VERTICAL RETRACE OUTPUT
$\overline{RD}$	READ STROBE INPUT	HLGT	HIGHLIGHT OUTPUT
$\overline{WR}$	WRITE STROBE INPUT	RVV	REVERSE VIDEO OUTPUT
A_0	REGISTER ADDRESS INPUT	LTEN	LIGHT ENABLE OUTPUT
CS	CHIP SELECT INPUT	VSP	VIDEO SUPPRESS OUTPUT
CCLK	CHARACTER CLOCK INPUT	GPA_{0-1}	GENERAL PURPOSE ATTRIBUTE OUTPUTS
CC_{0-6}	CHARACTER CODE OUTPUTS	LPEN	LIGHT PEN INPUT

MPU PERIPHERALS

PIN DESCRIPTIONS

Pin #	Pin Name	I/O	Pin Description
1	LC_3	O	Line count. Output from the line counter which is used to address the character generator for the line positions on the screen.
2	LC_2		
3	LC_1		
4	LC_0		
5	DRQ	O	DMA request. Output signal to the 8257 DMA controller requesting a DMA cycle.
6	$\overline{DACK}$	I	DMA acknowledge. Input signal from the 8257 DMA controller acknowledging that the requested DMA cycle has been granted.
7	HRTC	O	Horizontal retrace. Output signal which is active during the programmed horizonta' retrace interval. During this period the VSP output is high and the LTEN output is low.
8	VRTC	O	Vertical retrace. Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
9	$\overline{RD}$	I	Read input. A control signal to read registers.
10	$\overline{WR}$	I	Write input. A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
11	LPEN	I	Light pen. Input signal from the CRT system signifying that a light pen signal has been detected.
12	DB_0	I/O	Bi-directional three-state data bus lines. The outputs are enabled during a read of the C or P ports.
13	DB_1		
14	DB_2		
15	DB_3		
16	DB_4		
17	DB_5		
18	DB_6		
19	DB_7		
20	Ground		Ground
40	V_{CC}		+5V power supply
39	LA_0	O	Line attribute codes. These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.
38	LA_1		
37	LTEN	O	Light enable. Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
36	RVV	O	Reverse video. Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
35	VSP	O	Video suppression. Output signal used to blank the video signal to the CRT. This output is active: — during the horizontal and vertical retrace intervals. — at the top and bottom lines of rows if underline is programmed to be number 8 or greater. — when an end of row or end of screen code is detected. — When a DMA underrun occurs. — at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for character and field attributes) — to create blinking displays as specified by cursor, character attribute, or field attribute programming.
34	GPA_1	O	General purpose attribute codes. Outputs which are enabled by the general purpose field attribute codes.
33	GPA_0		
32	HLGT	O	Highlight. Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.
31	IRQ	O	Interrupt request.
30	CCLK	I	Character clock (from dot/timing logic).
29	CC_6	O	Character codes. Output from the row buffers used for character selection in the character generator.
28	CC_5		
27	CC_4		
26	CC_3		
25	CC_2		
24	CC_1		
23	CC_0		
22	$\overline{CS}$	I	Chip select. The read and write are enabled by $\overline{CS}$.
21	A_0	I	Port address. A high input on A_0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.

FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8275 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

$\overline{RD}$ (Read)

A "low" on this input informs the 8275 that the CPU is reading data or status information from the 8275.

$\overline{WR}$ (Write)

A "low" on this input informs the 8275 that the CPU is writing data or control words to the 8275.

$\overline{CS}$ (Chip Select)

A "low" on this input selects the 8275. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.

DRQ (DMA Request)

A "high" on this output informs the DMA Controller that the 8275 desires a DMA transfer.

$\overline{DACK}$ (DMA Acknowledge)

A "low" on this input informs the 8275 that a DMA cycle is in progress.

IRQ (Interrupt Request)

A "high" on this output informs the CPU that the 8275 desires interrupt service.

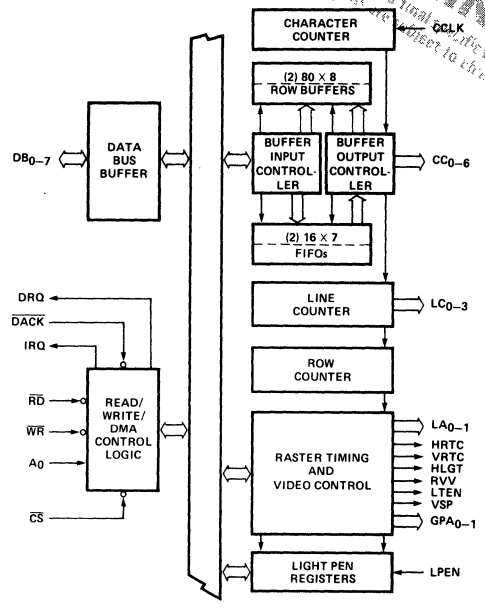


Figure 1. 8275 Block Diagram Showing Data Bus Buffer and Read/Write Functions

A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	Write 8275 Parameter
0	1	0	0	Read 8275 Parameter
1	0	1	0	Write 8275 Command
1	1	0	0	Read 8275 Status
X	1	1	0	Three-State
X	X	X	1	Three-state

MPU PERIPHERALS

Character Counter

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be a derivative of the external dot clock.

Line Counter

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row Counter

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Light Pen Registers

The Light Pen Registers are two registers that store the contents of the character counter and the row counter whenever there is a rising edge on the LPEN (Light Pen) input.

Note: Software correction is required.

Raster Timing and Video Controls

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of LA_{0-1} (Line Attribute), HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and GPA_{0-1} (General Purpose Attribute) outputs.

Row Buffers

The Row Buffers are two 80 character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

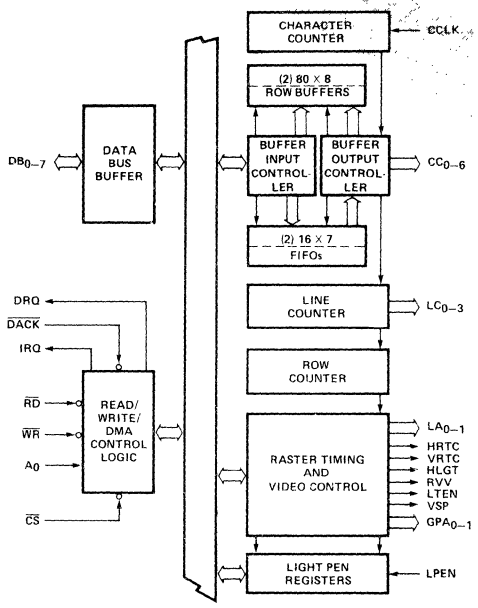


Figure 2. 8275 Block Diagram Showing Counter and Register Functions

FIFOs

There are two 16 character FIFOs in the 8275. They are used to provide extra row buffer length in the Transparent Attribute Mode (see Detailed Operation section).

Buffer Input/Output Controllers

The Buffer Input/Output Controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action. (Examples: An "End of Screen–Stop DMA" special code will cause the Buffer Input Controller to stop further DMA requests. A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)

SYSTEM OPERATION

The 8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with the 8257 DMA Controller and standard character generator ROMs for dot matrix decoding. Dot level timing must be provided by external circuitry.

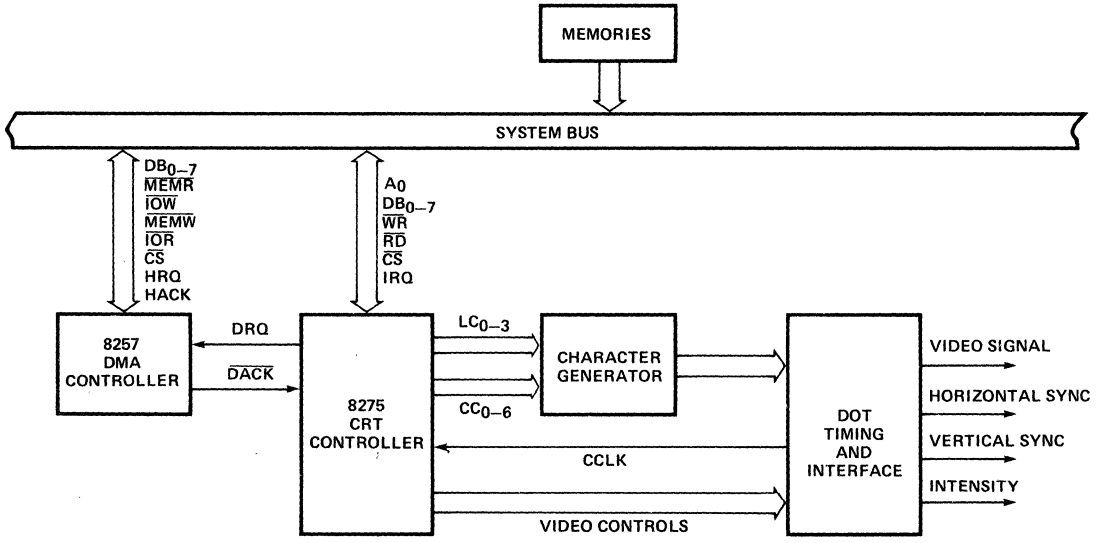


Figure 3. 8275 Systems Block Diagram Showing Systems Operation

General Systems Operational Description

The 8275 provides a "window" into the microcomputer system memory.

Display characters are retrieved from memory and displayed on a row by row basis. The 8275 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

The 8275 requests DMA to fill the row buffer that is not being used for display. DMA burst length and spacing is programmable. (See Programming Section.)

The 8275 displays character rows one line at a time.

The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See Programming Section.)

The 8275 provides special Control Codes which can be used to minimize DMA or software overhead. It also provides Visual Attribute Codes to cause special action or symbols on the screen without the use of the character generator (see Visual Attributes Section).

The 8275 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is programmable.

The 8275 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)

The 8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read on command. (See Programming Section.)

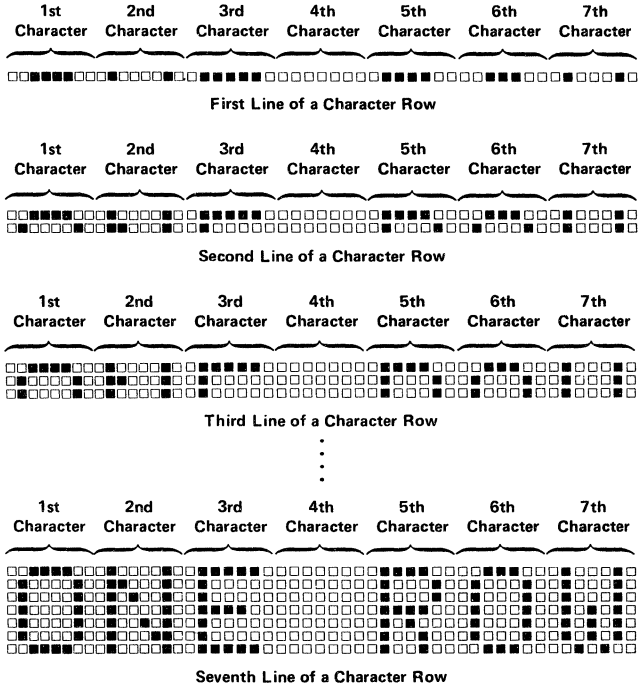


Figure 4. Display of a Character Row

Display Row Buffering

Before the start of a frame, the 8275 requests DMA and one row buffer is filled with characters.

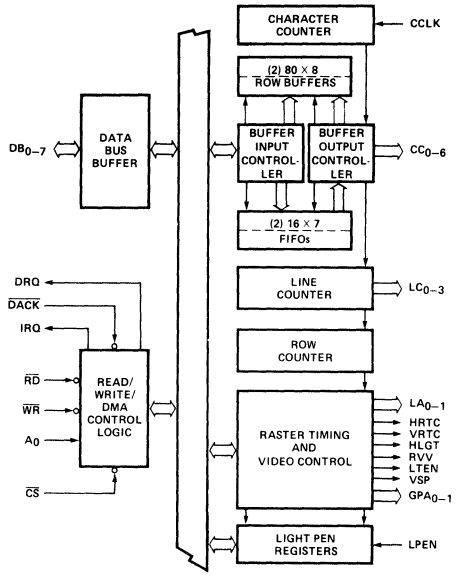


Figure 5. First Row Buffer Filled

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, DMA begins filling the other row buffer with the next row of characters.

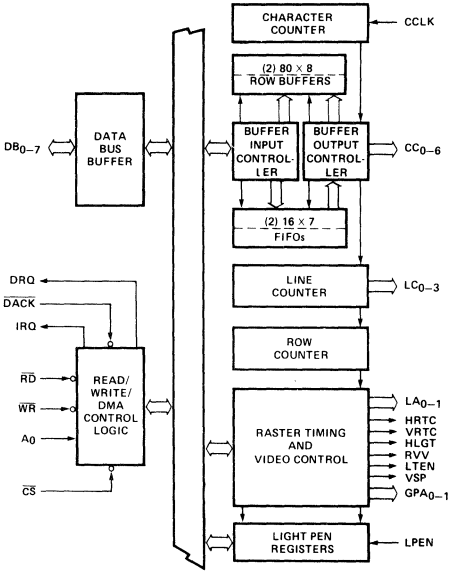


Figure 6. Second Buffer Filled, First Row Displayed

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

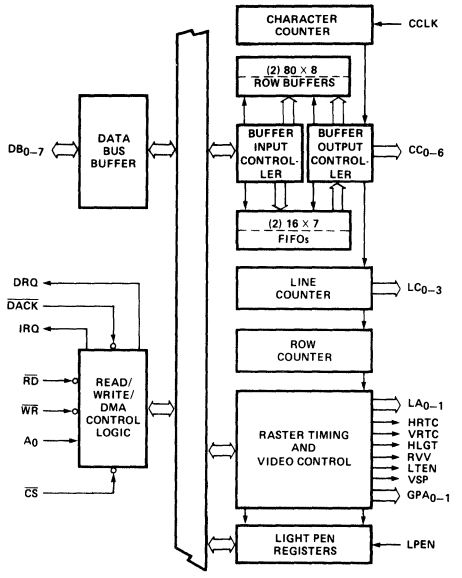


Figure 7. First Buffer Filled with Third Row, Second Row Displayed

This is repeated until all of the character rows are displayed.

Display Format

Screen Format

The 8275 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

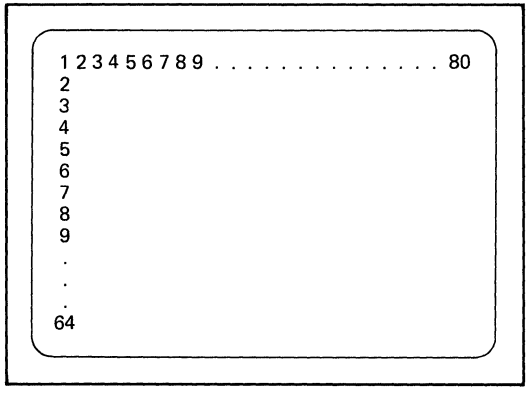


Figure 8. Screen Format

The 8275 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. DMA is not requested for the blanked rows.

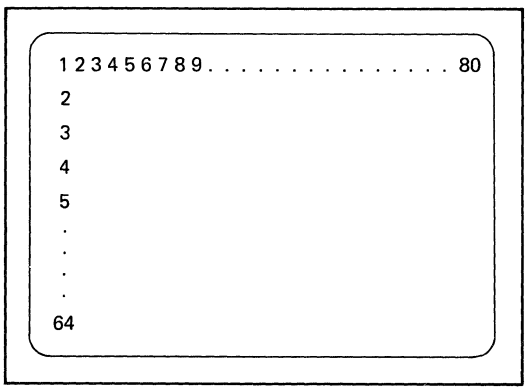


Figure 9. Blank Alternate Rows Mode

Row Format

The 8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

Note: In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by the line counter (see examples).

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □ □	0 0 0 0	1 1 1 1
1	□ □ □ □ ■ □ □ □ □	0 0 0 1	0 0 0 0
2	□ □ □ ■ □ ■ □ □ □	0 0 1 0	0 0 0 1
3	□ □ ■ □ □ □ ■ □ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ □ □ □ □ □ ■ □	0 1 0 1	0 1 0 0
6	□ ■ ■ ■ ■ ■ ■ ■ □	0 1 1 0	0 1 0 1
7	□ ■ □ □ □ □ □ ■ □	0 1 1 1	0 1 1 0
8	□ ■ □ □ □ □ □ ■ □	1 0 0 0	0 1 1 1
9	□ ■ □ □ □ □ □ ■ □	1 0 0 1	1 0 0 0
10	□ □ □ □ □ □ □ □ □	1 0 1 0	1 0 0 1
11	□ □ □ □ □ □ □ □ □	1 0 1 1	1 0 1 0
12	□ □ □ □ □ □ □ □ □	1 1 0 0	1 0 1 1
13	□ □ □ □ □ □ □ □ □	1 1 0 1	1 1 0 0
14	□ □ □ □ □ □ □ □ □	1 1 1 0	1 1 0 1
15	□ □ □ □ □ □ □ □ □	1 1 1 1	1 1 1 0

Figure 10. Example of a 16-Line Format

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □	0 0 0 0	1 0 0 1
1	□ □ □ ■ □ □ □	0 0 0 1	0 0 0 0
2	□ □ ■ □ ■ □ □	0 0 1 0	0 0 0 1
3	□ ■ □ □ □ ■ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ ■ ■ ■ ■ □	0 1 0 1	0 1 0 0
6	□ ■ □ □ □ ■ □	0 1 1 0	0 1 0 1
7	□ ■ □ □ □ ■ □	0 1 1 1	0 1 1 0
8	□ □ □ □ □ □ □	1 0 0 0	0 1 1 1
9	□ □ □ □ □ □ □	1 0 0 1	1 0 0 0

Figure 11. Example of a 10-Line Format

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □ □	0000	1011
1	□ □ □ □ ■ □ □ □ □	0001	0000
2	□ □ □ ■ □ ■ □ □ □	0010	0001
3	□ □ ■ □ □ □ ■ □ □	0011	0010
4	□ ■ □ □ □ □ □ ■ □	0100	0011
5	□ ■ □ □ □ □ □ ■ □	0101	0100
6	□ ■ ■ ■ ■ ■ ■ ■ □	0110	0101
7	□ ■ □ □ □ □ □ ■ □	0111	0110
8	□ ■ □ □ □ □ □ ■ □	1000	0111
9	□ ■ □ □ □ □ □ ■ □	1001	1000
10	■ ■ ■ ■ ■ ■ ■ ■ ■	1010	1001
11	□ □ □ □ □ □ □ □ □	1011	1010

Top and Bottom Lines are Blanked

Figure 12. Underline in Line Number 10

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ ■ □ □ □	0000	0111
1	□ □ ■ □ ■ □ □	0001	0000
2	□ ■ □ □ □ ■ □	0010	0001
3	□ ■ □ □ □ ■ □	0011	0010
4	□ ■ ■ ■ ■ ■ □	0100	0011
5	□ ■ □ □ □ ■ □	0101	0100
6	□ ■ □ □ □ ■ □	0110	0101
7	■ ■ ■ ■ ■ ■ ■	0111	0110

Top and Bottom Lines are not Blanked

Figure 13. Underline in Line Number 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.

Dot Format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

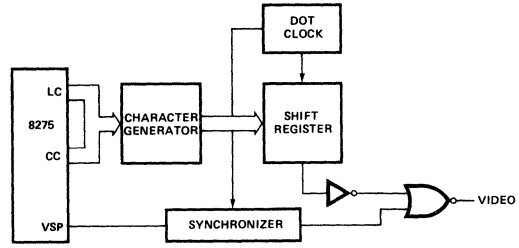


Figure 14. Typical Dot Level Block Diagram

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

Raster Timing

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This is constantly repeated.

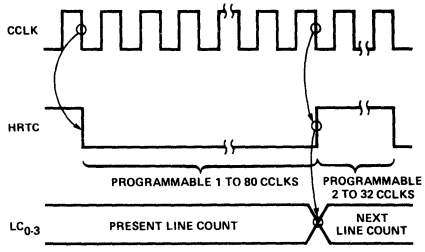


Figure 15. Line Timing

The line counter is driven by the character counter. It is used to generate the line address outputs (LC_{0-3}) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

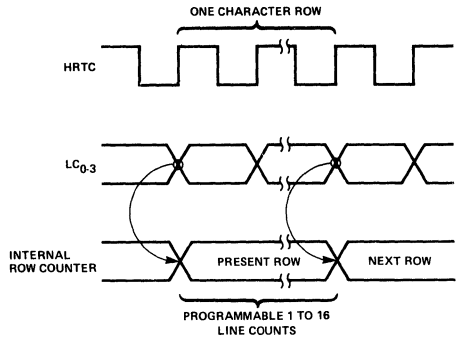


Figure 16. Row Timing

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

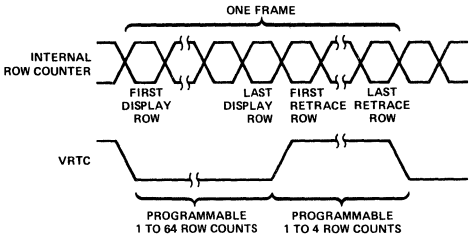


Figure 17. Frame Timing

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.

DMA Timing

The 8275 can be programmed to request burst DMA transfers of 1 to 8 characters. The interval between bursts is also programmable (from 0 to 55 character clock periods ±1). This allows the user to tailor his DMA overhead to fit his system needs.

The first DMA request of the frame occurs one *row time* before the end of vertical retrace. DMA requests continue as programmed, until the row buffer is filled. If the row buffer is filled in the middle of a burst, the 8275 terminates the burst and resets the burst counter. No more DMA requests will occur until the *beginning* of the *next* row. At that time, DMA requests are activated as programmed until the other buffer is filled.

If, for any reason, there is a DMA underrun, a flag in the status word will be set.

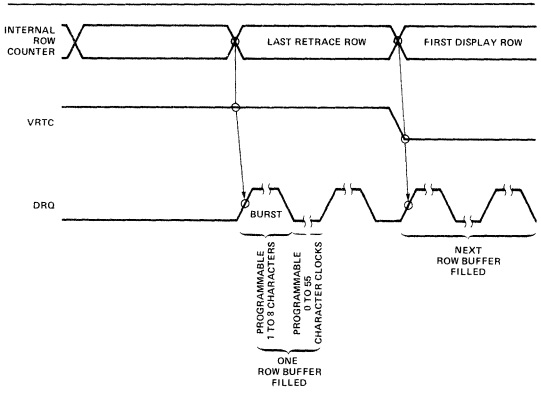


Figure 18. DMA Timing

The DMA controller is typically initialized for the next frame at the end of the current frame.

Interrupt Timing

The 8275 can be programmed to generate an interrupt request at the end of each frame. This can be used to reinitialize the DMA controller. If the 8275 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row*.

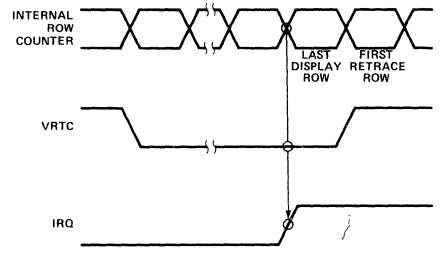


Figure 19. Beginning of Interrupt Request

IRQ will go inactive after the status register is read.

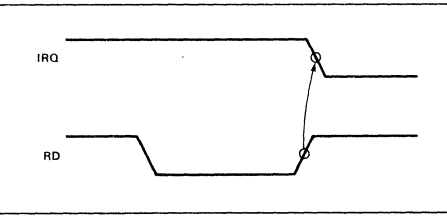


Figure 20. End of Interrupt Request

A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Another method of reinitializing the DMA controller is to have the DMA controller itself interrupt on terminal count. With this method, the 8275 interrupt enable flag should not be set.

Note: Upon power-up, the 8275 Interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the 8275 before system interrupts are enabled.

VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the 8275 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

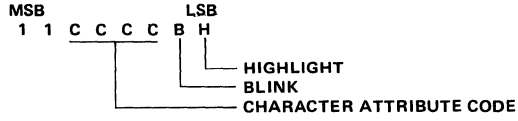
There are two types of Visual Attribute Codes. They are Character Attributes and Field Attributes.

Character Attribute Codes

Character attribute codes are codes that can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the Line Attribute outputs (LA_{0-1}), the Video Suppression output (VSP), and the Light Enable output. The dot level timing circuitry can use these signals to generate the proper symbols.

Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the Video Suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the Highlight output (HGLT).

Character Attributes



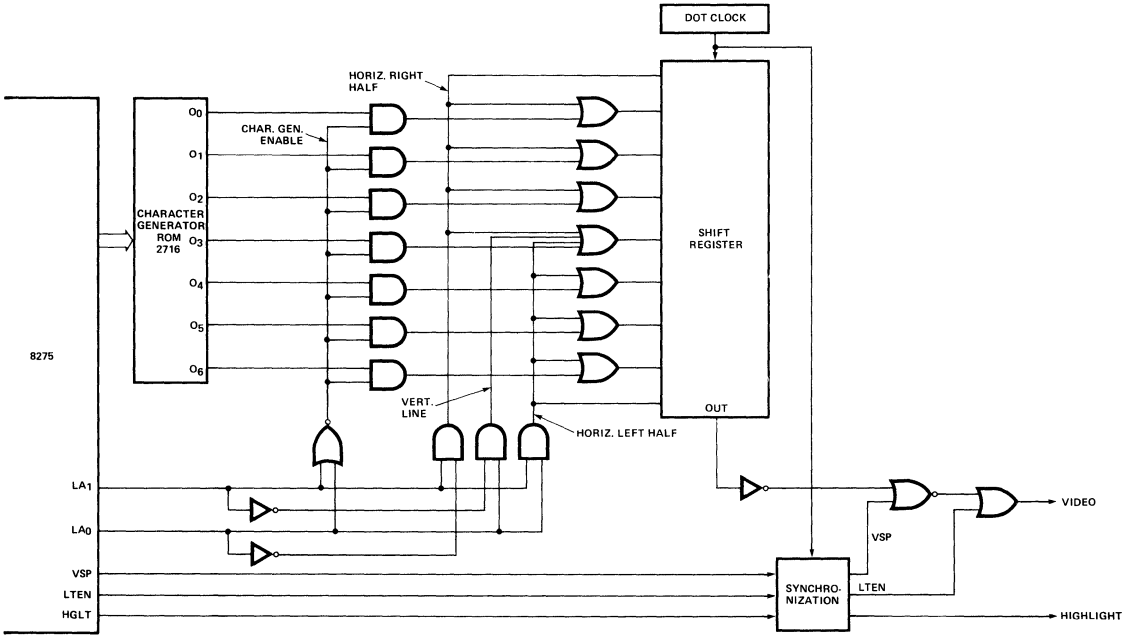


Figure 21. Typical Character Attribute Logic

Character attributes were designed to produce the following graphics:

CHARACTER ATTRIBUTE CODE "CCCC"		OUTPUTS LA_1	OUTPUTS LA_0	OUTPUTS VSP	OUTPUTS LTEN	SYMBOL	DESCRIPTION
0000	Above Underline	0	0	1	0		Top Left Corner
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0001	Above Underline	0	0	1	0		Top Right Corner
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0010	Above Underline	0	1	0	0		Bottom Left Corner
	Underline	1	0	0	0		
	Below Underline	0	0	1	0		
0011	Above Underline	0	1	0	0		Bottom Right Corner
	Underline	1	1	0	0		
	Below Underline	0	0	1	0		
0100	Above Underline	0	0	1	0		Top Intersect
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
0101	Above Underline	0	1	0	0		Right Intersect
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0110	Above Underline	0	1	0	0		Left Intersect
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0111	Above Underline	0	1	0	0		Bottom Intersect
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1000	Above Underline	0	0	1	0		Horizontal Line
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1001	Above Underline	0	1	0	0		Vertical Line
	Underline	0	1	0	0		
	Below Underline	0	1	0	0		
1010	Above Underline	0	1	0	0		Crossed Lines
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
1011	Above Underline	0	0	0	0		Not Recommended *
	Underline	0	0	0	0		
	Below Underline	0	0	0	0		
1100	Above Underline	0	0	1	0		Special Codes
	Underline	0	0	1	0		
	Below Underline	0	0	1	0		
1101	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						
1110	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						
1111	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						

*Character Attribute Code 1011 is not recommended for normal operation. Since none of the attribute outputs are active, the character Generator will not be disabled, and an indeterminate character will be generated.

Character Attribute Codes 1101, 1110, and 1111 are illegal.

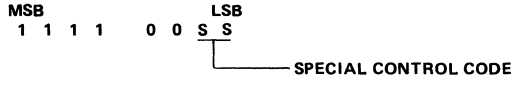
Blinking is active when B = 1.

Highlight is active when H = 1.

Special Codes

Four special codes are available to help reduce memory, software, or DMA overhead.

Special Control Character



S S	FUNCTION
0 0	End of Row
0 1	End of Row-Stop DMA
1 0	End of Screen
1 1	End of Screen-Stop DMA

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop DMA Code (01) causes the DMA Control Logic to stop DMA for the rest of the row when it is written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.

The End of Screen-Stop DMA Code (11) causes the DMA Control Logic to stop DMA for the rest of the frame when it is written into the Row Buffer. It affects the display in the same way as the End of Screen Code (10).

If the Stop DMA feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

Note: If a Stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop DMA character.

Field Attributes

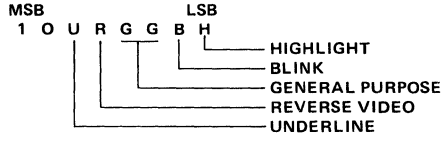
The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

1. *Blink* — Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* — Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
3. *Reverse Video* — Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
4. *Underline* — Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).

5,6. *General Purpose* — There are two additional 8275 outputs which act as general purpose, independently programmable field attributes. GPA_{0-1} are active high outputs.

Field Attribute Code



H = 1 FOR HIGHLIGHTING
B = 1 FOR BLINKING
R = 1 FOR REVERSE VIDEO
U = 1 FOR UNDERLINE
GG = GPA_1, GPA_0

The 8275 can be programmed to provide visible or invisible field attribute characters.

If the 8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.

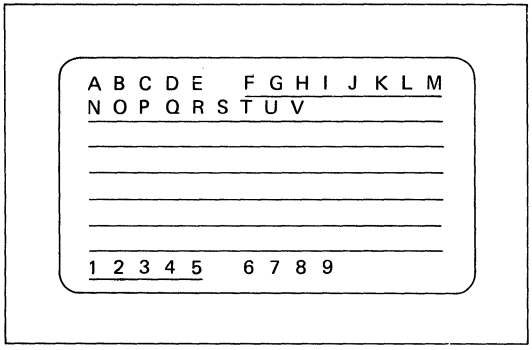


Figure 22. Example of the Visible Field Attribute Mode (Underline Attribute)

If the 8275 is programmed in the invisible field attribute mode, the 8275 FIFO is activated.

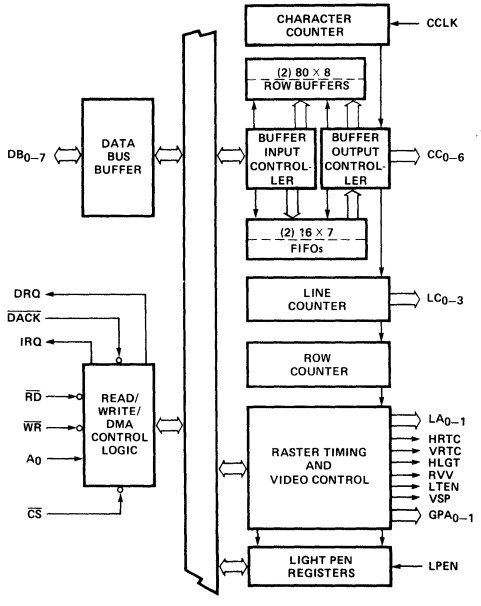


Figure 23. Block Diagram Showing FIFO Activation

Each row buffer has a corresponding FIFO. These FIFOs are 16 characters by 7 bits in size.

When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the *next* character in the proper FIFO.

When a field attribute is placed in the Buffer Output Controller during display, it causes the controller to immediately put a character from the FIFO on the Character Code outputs (CC_{0-6}). The chosen Visual Attributes are also activated.

Since the FIFO is 16 characters long, no more than 16 field attribute characters may be used per line in this mode. If more are used, a bit in the status word is set and the first characters in the FIFO are written over and lost.

Note: Since the FIFO is 7 bits wide, the MSB of any characters put in it are stripped off. Therefore, a Visual Attribute or Special Code must *not* immediately follow a field attribute code. If this situation does occur, the Visual Attribute or Special Code will be treated as a normal display character.

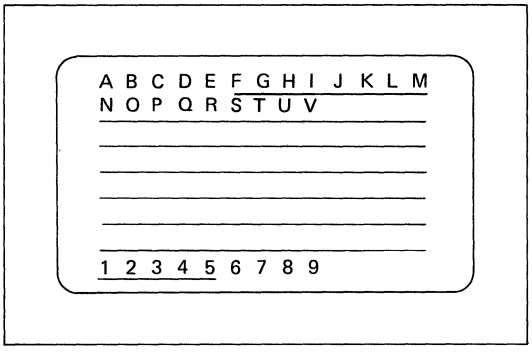


Figure 24. Example of the Invisible Field Attribute Mode (Underline Attribute)

Field and Character Attribute Interaction

Character Attribute Symbols are affected by the Reverse Video (RRV) and General Purpose (GPA_{0-1}) field attributes. They are not affected by Underline, Blink or Highlight field attributes; however, these characteristics can be programmed *individually* for Character Attribute Symbols.

Cursor Timing

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Light Pen Detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enables the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the 8275 LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

Note: Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

Device Programming

The 8275 has two programming registers, the Command Register (CREG) and the Parameter Register (PREG). It also has a Status Register (SREG). The Command Register can only be written into and the Status Registers can only be read from. They are addressed as follows:

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

The 8275 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

Instruction Set

The 8275 instruction set consists of 8 commands.

COMMAND	NO. OF PARAMETER BYTES
Reset	4
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the 8275 (SREG) can be read by the CPU at any time.

1. Reset Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Reset Command	0	0	0	0	0	0	0	0
Parameters	Write	0	Screen Comp Byte 1	S	H	H	H	H	H	H	H
	Write	0	Screen Comp Byte 2	V	V	R	R	R	R	R	R
	Write	0	Screen Comp Byte 3	U	U	U	U	L	L	L	L
	Write	0	Screen Comp Byte 4	M	F	C	C	Z	Z	Z	Z

Action – After the reset command is written, DMA requests stop, 8275 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter – S Spaced Rows

S	FUNCTIONS
0	Normal Rows
1	Spaced Rows

Parameter – HHHHHHH Horizontal Characters/Row

H	H	H	H	H	H	H	NO. OF CHARACTERS PER ROW
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
			.				.
			.				.
			.				.
1	0	0	1	1	1	1	80
1	0	1	0	0	0	0	Undefined
			.				.
			.				.
			.				.
1	1	1	1	1	1	1	Undefined

Parameter – VV Vertical Retrace Row Count

V	V	NO. OF ROW COUNTS PER VRTC
0	0	1
0	1	2
1	0	3
1	1	4

Parameter – RRRRRR Vertical Rows/Frame

R	R	R	R	R	R	NO. OF ROWS/FRAME
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
			.			.
			.			.
			.			.
1	1	1	1	1	1	64

Parameter – UUUU Underline Placement

U	U	U	U	LINE NUMBER OF UNDERLINE
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter – LLLL Number of Lines per Character Row

L	L	L	L	NO. OF LINES/ROW
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter – M Line Counter Mode

M	LINE COUNTER MODE
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

Parameter – F Field Attribute Mode

F	FIELD ATTRIBUTE MODE
0	Transparent
1	Non-Transparent

Parameter – CC Cursor Format

C	C	CURSOR FORMAT
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Nonblinking reverse video block
1	1	Nonblinking underling

Parameter – ZZZZ Horizontal Retrace Count

Z	Z	Z	Z	NO. OF CHARACTER COUNTS PER HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

Note: uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

2. Start Display Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Start Display	0	0	1	S	S	S	B	B
No parameters											

S S S BURST SPACE CODE

S	S	S	NO. OF CHARACTER CLOCKS BETWEEN DMA REQUESTS
0	0	0	0
0	0	1	7
0	1	0	15
0	1	1	23
1	0	0	31
1	0	1	39
1	1	0	47
1	1	1	55

B B BURST COUNT CODE

B	B	NO. OF DMA CYCLES PER BURST
0	0	1
0	1	2
1	0	4
1	1	8

Action – 8275 interrupts are enabled, DMA requests begin, video is enabled, Interrupt Enable and Video Enable status flags are set.

3. Stop Display Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Stop Display	0	1	0	0	0	0	0	0
No parameters											

Action – Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to re-enable the display.

4. Read Light Pen Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Read Light Pen	0	1	1	0	0	0	0	0
Parameters	Read	0	Char. Number	(Char. Position in Row)							
	Read	0	Row Number	(Row Number)							

Action – The 8275 is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

Note: Software correction of light pen position is required.

5. Load Cursor Position:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Load Cursor	1	0	0	0	0	0	0	0
Parameters	Write	0	Char. Number	(Char. Position in Row)							
	Write	0	Row Number	(Row Number)							

Action – The 8275 is conditioned to place the next two parameter bytes into the cursor position registers. Status flags not affected.

6. Enable Interrupt Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Enable Interrupt	1	0	1	0	0	0	0	0
No parameters											

Action – The interrupt enable status flag is set and interrupts are enabled.

7. Disable Interrupt Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Disable Interrupt	1	1	0	0	0	0	0	0
No parameters											

Action – Interrupts are disabled and the interrupt enable status flag is reset.

8. Preset Counters Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Preset Counters	1	1	1	0	0	0	0	0
No parameters											

Action – The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.

Status Flags

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Read	1	Status Word	0 IE IR LP IC VE OU F0

IE – (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.

IR – (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

LP – This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.

IC – (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE – (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

DU – (DMA Underrun) This flag is set whenever a data underrun occurs during DMA transfers. Upon detection of DU, the DMA operation is stopped and the screen is blanked until after the vertical retrace interval. This flag is reset after a status read.

FO – (FIFO Overrun) This flag is set whenever the FIFO is overrun. It is reset on a status read.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5V ±5%

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		160	mA	

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

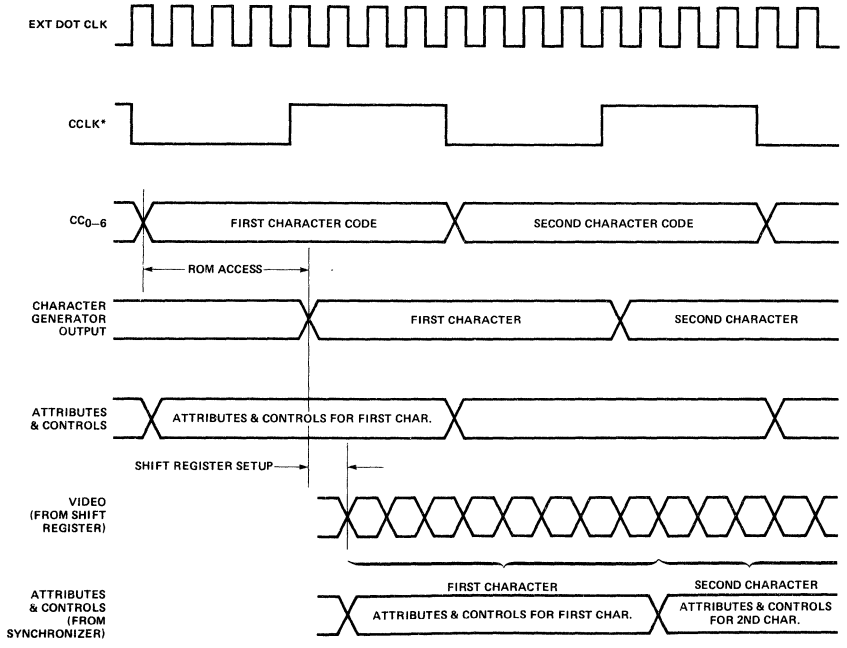
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance		10	pF	f_c = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}.

Other Timing:

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CC}	Character Code Output Delay		150	ns	C_L = 50 pF
t_{HR}	Horizontal Retrace Output Delay		150	ns	C_L = 50 pF
t_{LC}	Line Count Output Delay		250	ns	C_L = 50 pF
t_{AT}	Control/Attribute Output Delay		250	ns	C_L = 50 pF
t_{VR}	Vertical Retrace Output Delay		250	ns	C_L = 50 pF
t_{IR}	IRQ↑ from CCLK↓		250	ns	C_L = 50 pF
t_{RI}	IRQ↓ from Rd↑		250	ns	C_L = 50 pF
t_{KQ}	DRQ↑ from CCLK↓		250	ns	C_L = 50 pF
t_{WQ}	DRQ↑ from WR↑		250	ns	C_L = 50 pF
t_{RQ}	DRQ↓ from WR↓		200	ns	C_L = 50 pF
t_{LR}	DACK↓ to WR↓	0		ns	
t_{RL}	WR↑ to DACK↑	0		ns	
t_{PR}	LPEN Rise		50	ns	
t_{PH}	LPEN Hold	100		ns	

Note: Timing measurements are made at the following reference voltages: Output "1" = 2.0V, "0" = 0.8V.

WAVEFORMS



*CCLK IS A MULTIPLE OF THE DOT CLOCK AND AN INPUT TO THE 8275.

Figure 25. Typical Dot Level Timing

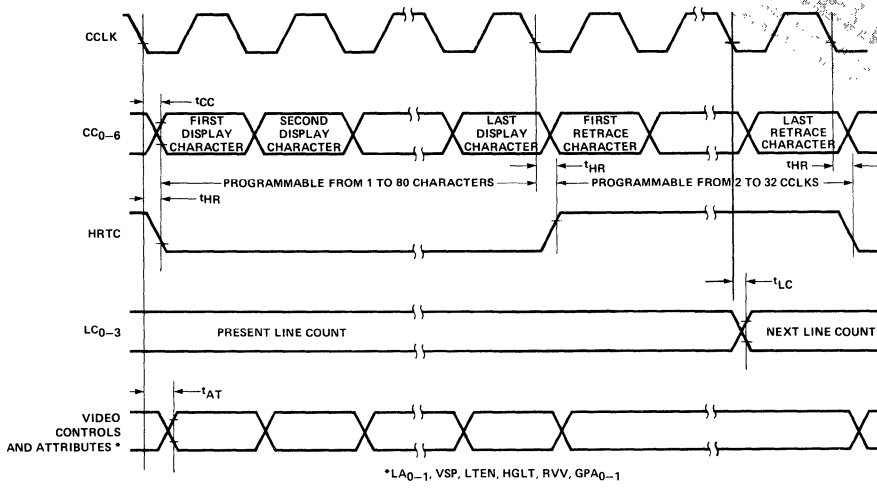


Figure 26. Line Timing

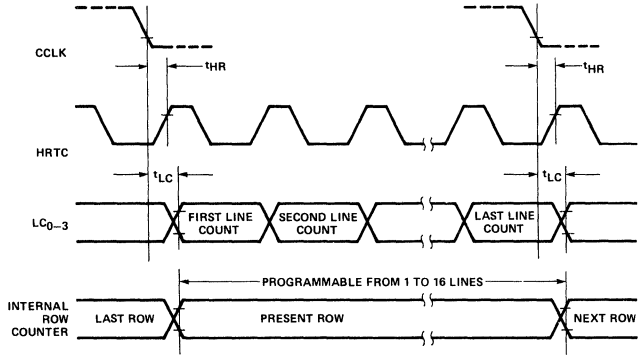


Figure 27. Row Timing

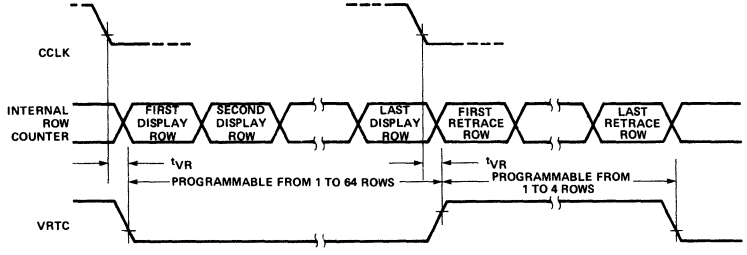


Figure 28. Frame Timing

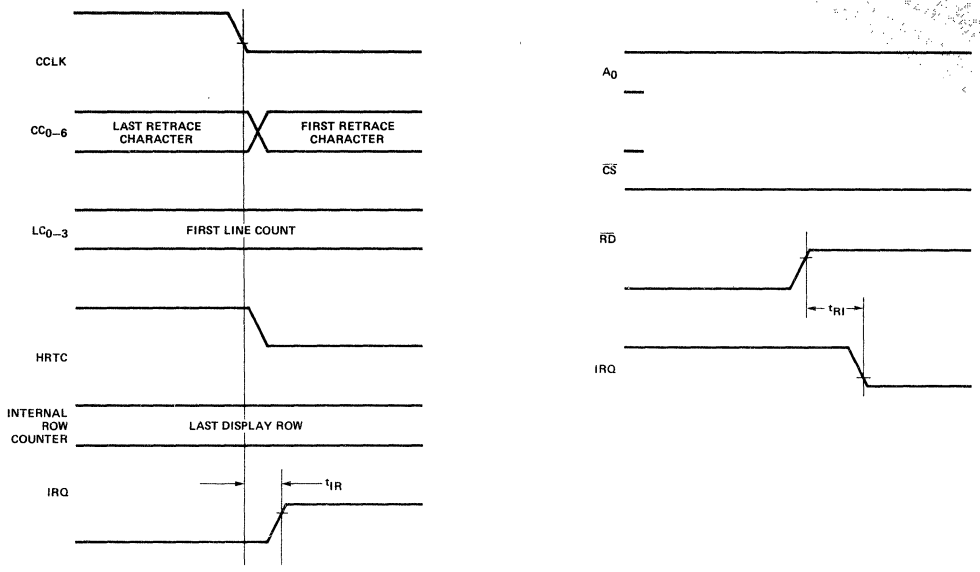


Figure 29. Interrupt Timing

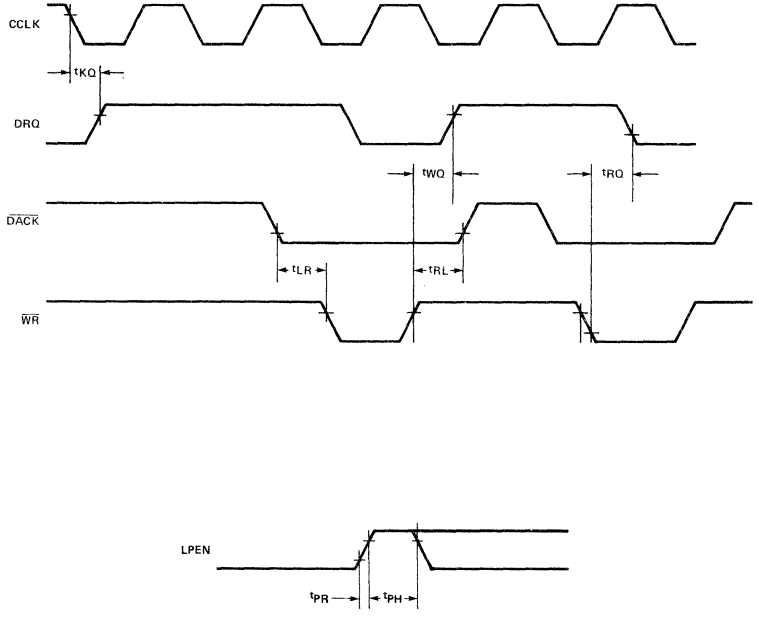


Figure 30. DMA Timing

A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

Bus Parameters (Note 1)

Read Cycle:

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Hold Time for READ	0		ns	
t_{RR}	READ Pulse Width	250		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 150 pF
t_{DF}	READ to Data Floating	20	100	ns	

Write Cycle:

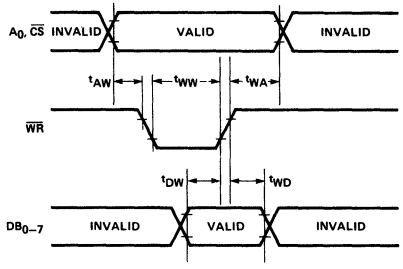
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Hold Time for WRITE	0		ns	
t_{WW}	WRITE Pulse Width	250		ns	
t_{DW}	Data Setup Time for WRITE	150		ns	
t_{WD}	Data Hold Time for WRITE	0		ns	

Clock Timing:

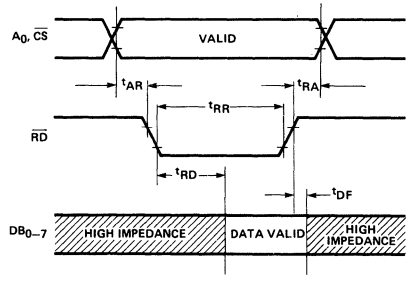
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CLK}	Clock Period	320		ns	
t_{KH}	Clock High	120		ns	
t_{KL}	Clock Low	120		ns	
t_{KR}	Clock Rise	5	30	ns	
t_{KF}	Clock Fall	5	30	ns	

Note 1: AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8

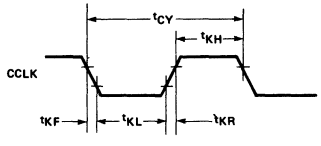
Write Timing



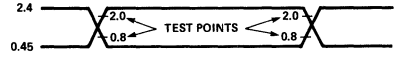
Read Timing



Clock Timing



Input Waveforms (For A.C. Tests)



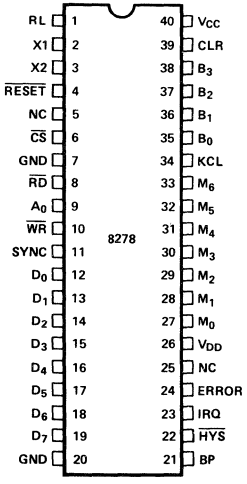
8278
PROGRAMMABLE KEYBOARD INTERFACE

- **Simultaneous Keyboard and Display Operations**
- **Interface Signals for Contact and Capacitive Coupled Keyboards**
- **128-Key Scanning Logic**
- **10.7 msec Matrix Scan Time for 128 Keys and 6 MHz Clock**
- **8-Character Keyboard FIFO**
- **N-Key Rollover with Programmable Error Mode on Multiple New Closures**
- **16-Character 7-Segment Display Interface**
- **Right or Left Entry Display RAM**
- **Depress/Release Mode Programmable**
- **Interrupt Output on Key Entry**

The Intel® 8278 is a general purpose programmable keyboard and display interface device designed for use with 8-bit microprocessors such the MDS-80™ and MCS-85™. The keyboard portion can provide a scanned interface to 128-key contact or capacitive-coupled keyboards. The keys are fully debounced with N-key rollover and programmable error generation on multiple new key closures. Keyboard entries are stored in an 8-character FIFO with overrun status indication when more than 8 characters are entered. Key entries set an interrupt request output to the master CPU.

The display portion of the 8278 provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric displays and simple indicators may be used. The 8278 has a 16X4 display RAM which can be loaded or interrogated by the CPU. Both right entry calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

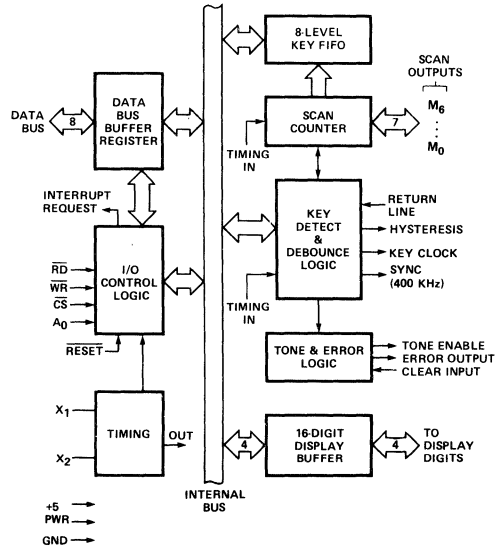
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS
$\overline{RD}$, $\overline{WR}$	READ, WRITE STROBES
$\overline{CS}$	CHIP SELECT
A_0	CONTROL/DATA SELECT
$\overline{RESET}$	RESET INPUT
X_1, X_2	FREQ. REFERENCE INPUT
SYNC	HIGH FREQUENCY OUTPUT CLOCK
RL	KEYBOARD RETURN LINE
CLR	CLEAR ERROR
KCL	KEY CLOCK
M_6-M_0	MATRIX SCAN LINES
B_3-B_0	DISPLAY OUTPUTS
ERROR	ERROR SIGNAL
$\overline{IRQ}$	INTERRUPT REQUEST
$\overline{HYS}$	HYSTERESIS
BP	TONE ENABLE

BLOCK DIAGRAM



PIN DESCRIPTION

The 8278 is packaged in a 40-pin DIP. The following is a brief functional description of each pin.

Signal	Pin No.	Description
D_0-D_7	12-19	Three-state, bi-directional data bus lines used to transfer data and commands between the CPU and the 8278.
$\overline{WR}$	10	Write strobe which enables the master CPU to write data and commands between the CPU and the 8278.
$\overline{RD}$	8	Read strobe which enables the master CPU to read data and status from the 8278 internal registers.
$\overline{CS}$	6	Chip select input used to enable reading and writing to the 8278.
A_0	9	Address input used by the CPU to indicate control or data.
$\overline{RESET}$	4	A low signal on this pin resets the 8278.
X_1, X_2	2,3	Inputs for crystal, L-C or external timing signal to determine internal oscillator frequency.
IRQ	23	Interrupt Request Output to the master CPU. In the keyboard mode the IRQ line goes low with each FIFO read and returns high if there is still information in the FIFO or an ERROR has occurred.
M_0-M_6	27-33	Matrix scan outputs. These outputs control a decoder which scans the key matrix columns and the 16 display digits. Also, the Matrix scan outputs are used to multiplex the return lines from the key matrix.
RL	1	Input from the multiplexer which indicates whether the key currently being scanned is closed.
$\overline{HYS}$	22	Hysteresis output to the analog detector. (Capacitive keyboard configuration). A "0" means the key currently being scanned has already been recorded.
KCL	34	Key clock output to the analog detector (capacitive keyboard configuration) used to reset the detector before scanning a key.
SYNC	11	High frequency (400 KHz) output signal used in the key scan to detect a closed key (capacitive keyboard configuration).
B_0-B_3	35-38	These four lines contain binary coded decimal display information synchronized to the keyboard column scan. The outputs are for multiplexed digital displays.
ERROR	24	Error signal. This line is high whenever two new key closures are detected during a single scan or when too many characters are entered into the keyboard FIFO. It is reset by a system RESET pulse or by a "1" input on the CLR pin or by the CLEAR ERROR command.
CLR	39	Input used to clear an ERROR condition in the 8278.
BP	21	Tone enable output. This line is high for 10ms following a valid key closure; it is set high and remains high during an ERROR condition.
V_{CC}, V_{DD}	40,26	+5 volt power input: +5V ± 10%.
GND	20,7	Signal ground.

PRINCIPLES OF OPERATION

The following is a description of the major elements of the Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 1.

I/O Control and Data Buffers

The I/O control section uses the $\overline{CS}$, A_0, $\overline{RD}$, and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers (see Table 1). All data flow to and from the 8278 is enabled by $\overline{CS}$. The 8-bits of information being transferred by the CPU is identified by A_0. A logic one means information is command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Bus Buffer (DBB). The DBB register is a bi-directional 8-bit buffer register which connects the internal 8278 bus buffer register to the external bus. When the chip is not selected ($\overline{CS}$ = 1) the DBB is in the high impedance state. The DBB acts as an input when ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$) = (1, 0, 0) and an output when ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$) = (0, 1, 0).

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	Condition
0	0	1	0	Read DBB Data
0	1	1	0	Read STATUS
0	0	0	1	Write Data to DBB
0	1	0	1	Write Command to DBB
1	X	X	X	Disable 8278 Bus is High Impedance

Scan Counter

The scan counter provides the timing to scan the keyboard and display. The four MSB's (M_3-M_6) scan the display digits and provide column scan to the keyboard via a 4 to 16 decoder. The three LSB's (M_0-M_2) are used to multiplex the row return lines into the 8278.

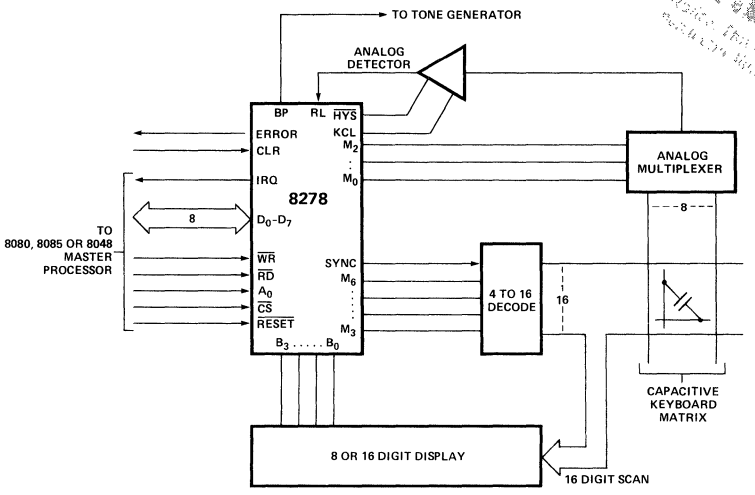


Figure 1. System Configuration for Capacitive-Coupled Keyboard

Keyboard Debounce and Control

The 8278 system configuration is shown in Figure 2. The rows of the matrix are scanned and the outputs are multiplexed by the 8278. When a key closure is detected, the debounce logic waits about 12 msec to check if the key remains closed. If it does, the address of the key in the matrix is transferred into a FIFO buffer.

FIFO and FIFO Status

The 8278 contains an 8X8 FIFO character buffer. Each new entry is written into a successive FIFO location and each is then read out in the order of entry. A FIFO status register keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or key entries will be recognized as an error. The status can be read by a $\overline{RD}$ with $\overline{CS}$ low and A_0 high. The status logic also provides a IRQ signal to the master processor whenever the FIFO is not empty.

Display Address Registers and Display RAM

The display Address registers hold the address of the word currently being written or read by the CPU and the 4-bit nibble being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The display RAM can be directly read by the CPU after the correct mode and address is set. Data entry to the display can be set to either left or right entry.

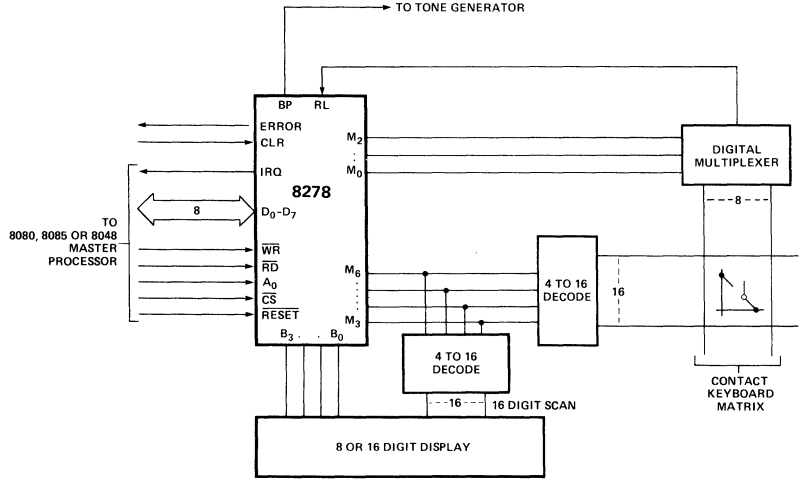
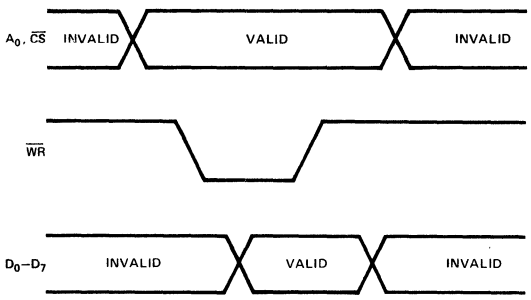


Figure 2. System Configuration for Contact Keyboard

8278 COMMANDS

The 8278 operating mode is programmed by the master CPU using the A_0, WR, and D_0-D_7 inputs as shown below:



The master CPU presents the proper command on the D_0-D_7 data lines with A_0=1 and then sends a $\overline{WR}$ pulse. The command is latched by the 8278 on the rising edge of the $\overline{WR}$ and is decoded internally to set the proper operating mode.

COMMAND SUMMARY

Keyboard/Display Mode Set

CODE	0	0	0	N	E	I	D	K

where the mode set bits are defined as follows:

K — the keyboard mode select bit
0 — normal key entry mode
1 — special function mode: Entry on key closure and on key release

D — the display entry mode select bit
0 — left display entry
1 — right display entry

I — the interrupt request (IRQ) output enable bit.
0 — enable IRQ output
1 — disable IRQ output

E — the error mode select bit
0 — error on multiple key depression
1 — no error on multiple key depression

N — the number of display digits select
0 — 16 display digits
1 — 8 display digits

NOTE: The default mode following a RESET input is all bits zero:

0	0	0	0	0	0	0	0

Read FIFO Command

CODE	0	1	0	0	0	0	0	0

Read Display Command

CODE	0	1	1	AI	A_3	A_2	A_1	A_0

Where AI indicates Auto Increment and A_3-A_0 is the address of the next display character to be read out.

AI=1 AUTO increment
AI=0 no AUTO increment

Write Display Command

CODE	1	0	0	AI	A_3	A_2	A_1	A_0

Where AI indicates Auto Increment and A_3-A_0 is the address of the next display character to be written.

Clear/Blank Command

CODE	1	0	1	UD	BD	CD	CF	CE

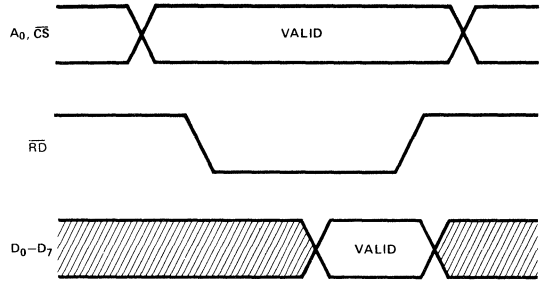
Where the command bits are defined as follows:

CE = Clear ERROR
CF = Clear FIFO
CD = Clear Display RAM to all High
BD = Blank Display to all High (Display RAM unaffected)
UD = Unblank Display

The display is cleared and blanked following a Reset.

8278 Status Read

The status register in the 8278 can be read by the master CPU using the A_0, $\overline{RD}$, and D_0-D_7 inputs as shown below:



The 8278 places 8-bits of status information on the D_0-D_7 lines following (A_0, $\overline{CS}$, $\overline{RD}$) = 1, 0 , 0 inputs from the master.

Status Format

S_3	S_2	S_1	S_0	B	KE	IBF	OBF
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Where the status bits are defined as follows:

OBF = Output Buffer Full Flag
IBF = Input Buffer Full Flag
KE = Keyboard Error Flag (multiple depression)
B = BUSY Flag
S_3-S_0 = FIFO Status

Status Description

The S_3-S_0 status bits indicate the number of entries (0 to 8) in the 8-level FIFO. A FIFO overrun will lock status at 1111. The overrun condition will prevent further key entries until cleared.

A multiple key closure error will set the KE flag and prevent further key entries until cleared.

The IBF and OBF flags signify the status of the 8278 data buffer registers used to transfer information (data, status or commands) to and from the master CPU.

The IBF flag is set when the master CPU writes Data or Commands to the 8278. The IBF flag is cleared by the 8278 during its response to the Data or Command.

The OBF flag is set when the 8278 has output data ready for the master CPU. This flag is cleared by a master CPU Data READ.

The Busy flag in the status register is used as a LOCK-OUT signal to the master processor during response to any command or data write from the master.

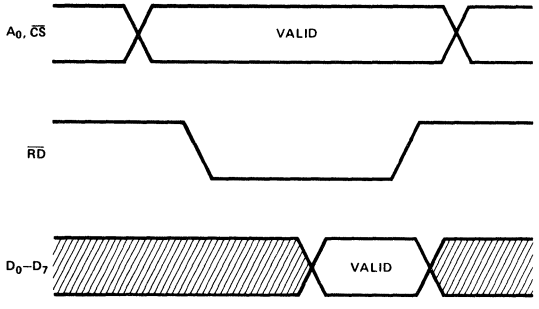
The master must test the Busy flag before each read (during a sequence) to be sure that the 8278 is ready with valid DATA.

The ERROR and TONE outputs from the 8278 are set high for either type of error. Both types of error are cleared by the CLR input, by the CLEAR ERROR command, or by a reset. The FIFO and Display buffers are cleared independently of the Errors.

FIFO status is used to indicate the number of characters in the FIFO and to indicate whether an error has occurred. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO. The character read will be the last one entered. FIFO status will remain at 0000 and the error condition will not be set.

8278 Data Read

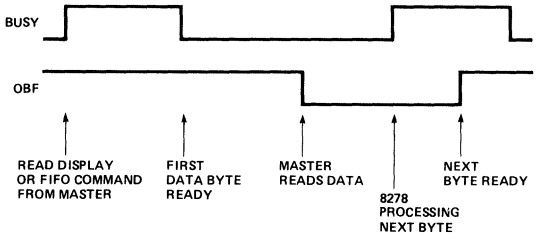
The master CPU can read DATA from the 8278 FIFO or Display buffers by using the A_0, $\overline{RD}$, and D_0-D_7 inputs as follows:



The master sends a $\overline{RD}$ pulse with A_0=0 and CS=0 and the 8278 responds by outputing data on lines D_0-D_7. The data is strobed by the trailing edge of $\overline{RD}$.

Data Read Sequence

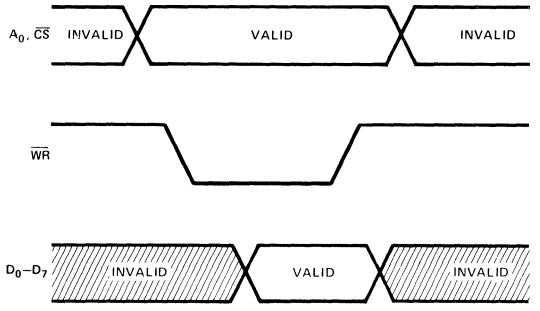
Before reading data, the master CPU must send a command to select FIFO or Display data. Following the command, the master must read STATUS and test the BUSY flag and the OBF flag to verify that the 8278 has responded to the previous command. A typical DATA READ sequence is as follows:



After the first read following a Read Display or Read FIFO command, successive reads may occur as soon as OBF rises.

8278 Data Write

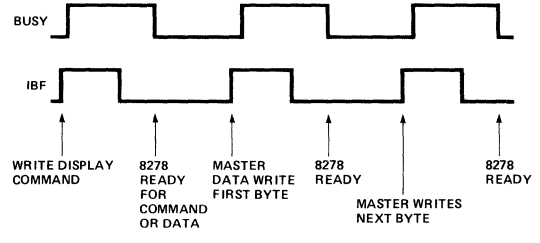
The master CPU can write DATA to the 8278 Display buffers by using the A_0, $\overline{WR}$ and D_0-D_7 inputs as follows:



The master CPU presents the Data on the D_0-D_7 lines with A_0=0 and then sends a $\overline{WR}$ pulse. The data is latched by the 8278 on the rising edge of $\overline{WR}$.

Data Write Sequence

Before writing data to the 8278, the master CPU must first send a command to select the desired display entry mode and to specify the address of the next data byte. Following the commands, the master must read STATUS and test the BUSY flag (B) and IBF flag to verify that the 8278 has responded. A typical sequence is shown below:



INTERFACE CONSIDERATIONS

Scanned Keyboard Mode

With N-key rollover each key depression is treated independently from all others. When a key is depressed the debounce logic waits for a full scan of 128 keys and then checks to see if the key is still down. If it is, the key is entered into the FIFO.

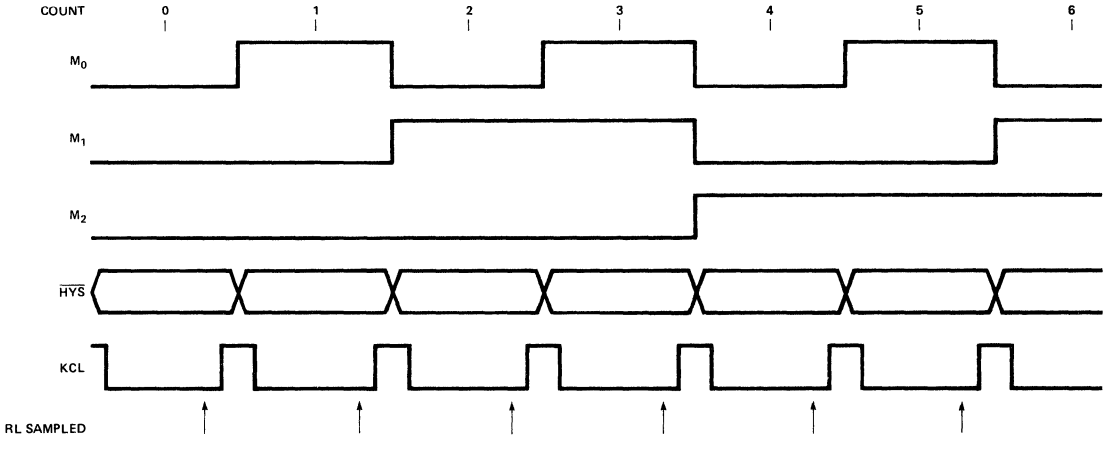


Figure 3. Keyboard Timing

If two key closures occur during the same scan the ERROR output is set, the KE flag is set in the Status word, the TONE output is activated and IRQ is set, and no further inputs are accepted. This condition is cleared by a high signal on the CLEAR input or by a system $\overline{RESET}$ input or by the CLEAR ERROR command.

In the special function mode both the key closure and the key release cause an entry to the FIFO. The release is entered with the MSB=1.

Any key entry triggers the TONE output for 10ms.

The $\overline{HYS}$ and KCL outputs enable the analog multiplexer and detector to be synchronized for interface to capacitive coupled keyboards.

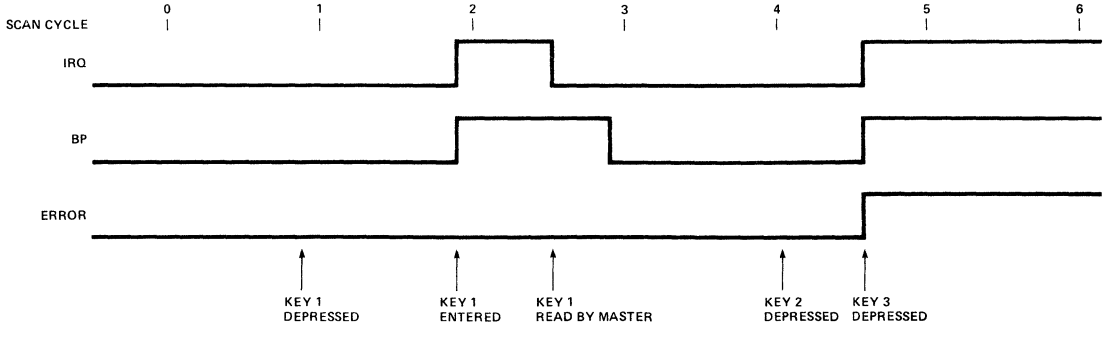
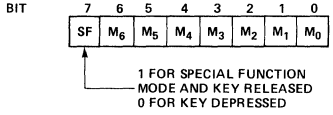


Figure 4. Key Entry and Error Timing

Data Format

In the scanned keyboard mode, the code entered into the FIFO corresponds to the position or address of the switch in the keyboard. The MSB is relevant only for special function keys in which code "0" signifies closure and "1" signifies release. The next four bits are the column count which indicates which column the key was found in. The last three bits are from the row counter.

KEY CODING



Display

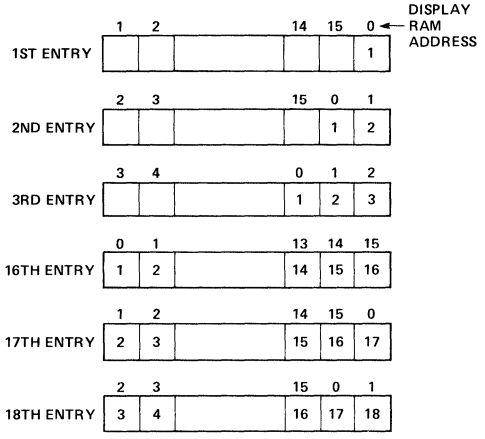
Display data is entered into a 16x4 display register and may be entered from the left, from the right or into specific locations in the display register. A new data character is put out on B_0-B_3 each time the M_6-M_3 lines change (i.e., once every 0.75ms with a 6 MHz crystal). Data is blanked during the time the column select lines change by raising the display outputs. Output data is positive true.

Left Entry

The left entry mode is the simplest display format in that each display position in the display corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 is the right-most display character. Entering characters from position zero causes the display to fill from the left. The 17th character is entered back in the left-most position and filling again proceeds from there.

Right Entry

Right entry is the method used by most electronic calculators. The first entry is placed in the right-most display character. The next entry is also placed in the right-most character after the display is shifted left one character. The left-most character is shifted off the end and is lost.



Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended. A Clear Display command should be given before display data is entered if the number of data characters is not equal to 16 (or 8) in this mode.

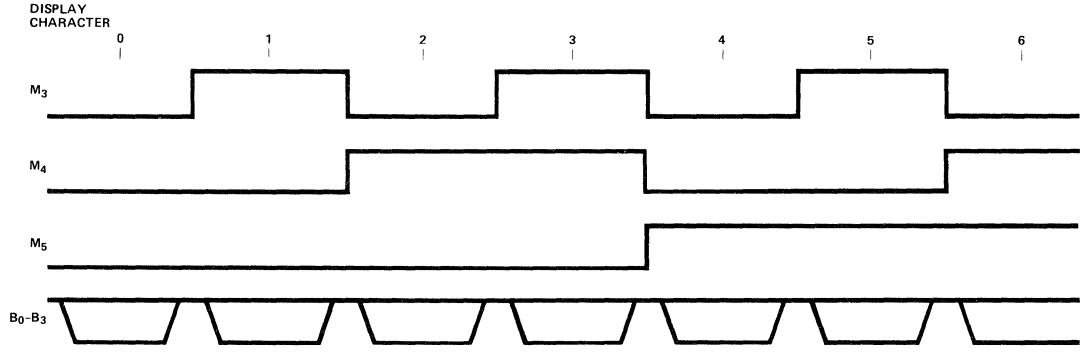
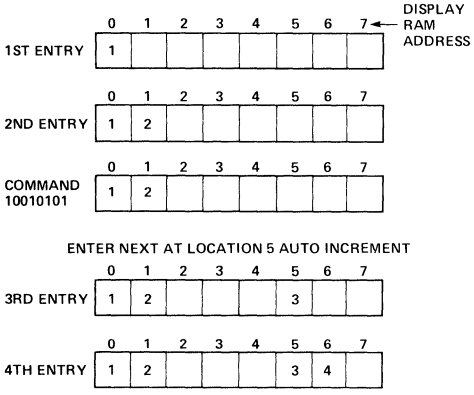


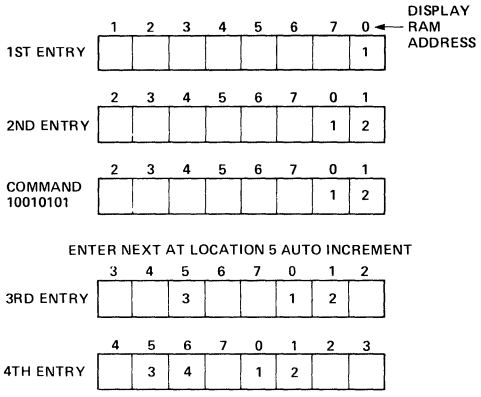
Figure 5. Display Timing

Auto Increment

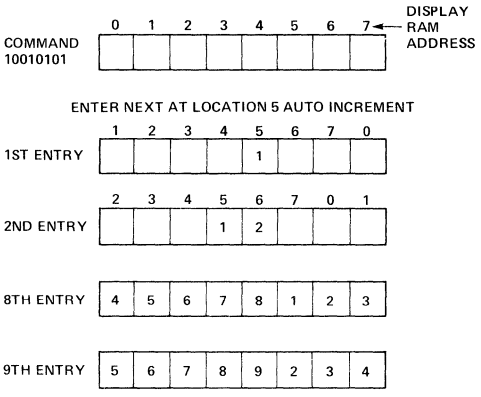
In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Left Entry — Auto Increment mode has no undesirable side effects and the result is predictable:



In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except that the address sequence is interrupted:



Starting at an arbitrary location operates as shown below:



Entry appears to be from the initial entry point.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1.5 Watt

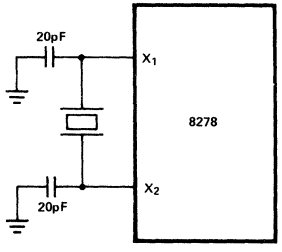
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

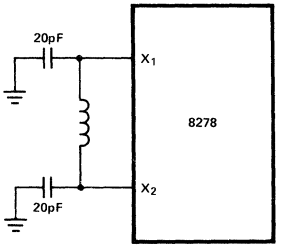
Commercial: T_A = 0°C to 70°C; V_{CC} = +5V ±5%; V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Units	Condition
V_{IL}	Input Low Voltage (All Inputs Except X_1, X_2	-0.5	0.8	V	
V_{IH1}	Input High Voltage (All Inputs Except X_1, X_2, $\overline{RESET}$	2.0	V_{CC}	V	
V_{IH2}	$\overline{RESET}$ High Voltage	3.0	V_{CC}	V	
V_{OL1}	Output Low Voltage (D_0-D_7)		0.45	V	I_{OL} = 2.0mA
V_{OL2}	Output Low Voltage (All Other Outputs)		0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage (D_0-D_7)	2.4		V	I_{OH} = -400μA
V_{OH2}	Output High Voltage (All Other Outputs)	2.4		V	I_{OH} = -50μA
I_{IL}	Input Leakage Current (All Inputs Except $\overline{RESET}$)		±10	μA	V_{IN} = V_{CC}
I_{OL}	Output Leakage Current (D_0-D_7)		±10	μA	V_{IN} = V_{SS} + 0.45V or V_{IN} = V_{CC}
I_{DD} + I_{CC}	Total Supply Current		135	mA	V_{CC} = 5.5V
I_{DD}	V_{DD} Supply Current		25	mA	V_{CC} = 5.5V
I_{LI}	Low Input Source Current ($\overline{RESET}$)		0.2	mA	V_{IL} = 0.8V

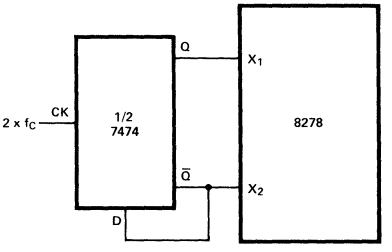
8278 CLOCK OPTIONS



1-6 MHz CRYSTAL



40 μh-130 μh INDUCTOR



EXTERNAL CLOCK

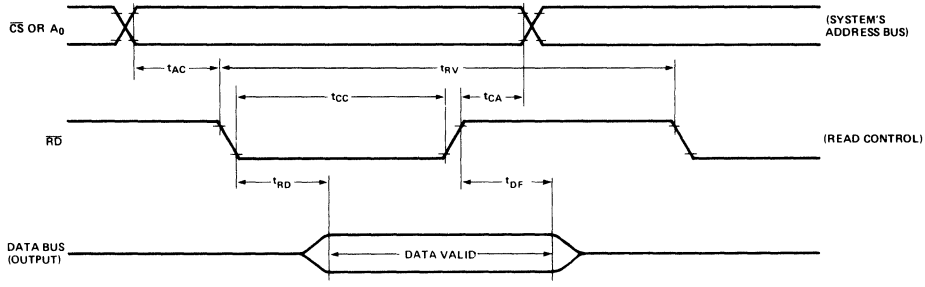
A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$

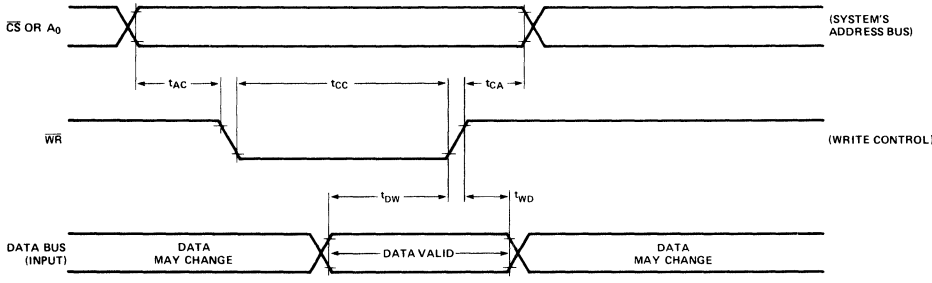
Symbol	Parameter	Min.	Max.	Units	Condition
t_{AC}	Address ($\overline{CS}$, A_0) Setup to Control ($\overline{RD}$, $\overline{WR}$)	0		ns	D_0-D_7, C_L = 150pF
t_{CA}	Address Hold from Control	0		ns	
t_{CC}	Control Pulse Width	250		ns	
t_{DW}	Data in Setup to $\overline{WR}$ T.E.	150		ns	
t_{WD}	Data in Hold After $\overline{WR}$ T.E.	0		ns	
t_{RD}	$\overline{RD}$ L.E. to Data Out Valid		150	ns	
t_{DF}	$\overline{RD}$ T.E. to Data Out Float	10	100	ns	
t_{MCY}	Matrix Cycle Time		10.7	ms	With 6MHz Crystal
t_{RV}	Recovery Time Between Reads and/or Writes	1		μs	

WAVEFORMS

Read Operation — Data Bus Buffer Register



Write Operation — Data Bus Buffer Register



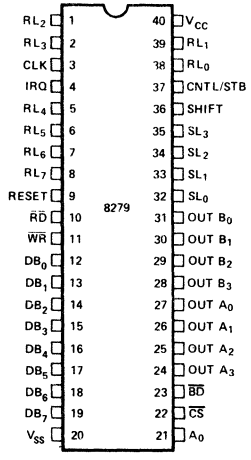
8279/8279-5
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- **MCS-85™ Compatible 8279-5**
- **Simultaneous Keyboard Display Operations**
- **Scanned Keyboard Mode**
- **Scanned Sensor Mode**
- **Strobed Input Entry Mode**
- **8-Character Keyboard FIFO**
- **2-Key Lockout or N-Key Rollover with Contact Debounce**
- **Dual 8- or 16-Numerical Display**
- **Single 16-Character Display**
- **Right or Left Entry 16-Byte Display RAM**
- **Mode Programmable from CPU**
- **Programmable Scan Timing**
- **Interrupt Output on Key Entry**

The Intel® 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16X8 display RAM which can be organized into dual 16X4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

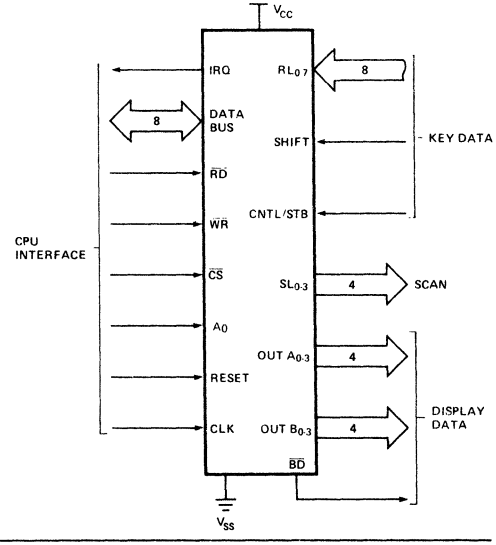
PIN CONFIGURATION



PIN NAMES

DB_{0-7}	I/O	DATA BUS (BI DIRECTIONAL)
CLK	I	CLOCK INPUT
RESET	I	RESET INPUT
$\overline{CS}$	I	CHIP SELECT
$\overline{RD}$	I	READ INPUT
$\overline{WR}$	I	WRITE INPUT
A_0	I	BUFFER ADDRESS
IRQ	O	INTERRUPT REQUEST OUTPUT
SL_{0-3}	O	SCAN LINES
RL_{0-7}	I	RETURN LINES
SHIFT	I	SHIFT INPUT
CNTL/STB	I	CONTROL/STROBE INPUT
$OUT\ A_{0-3}$	O	DISPLAY (A) OUTPUTS
$OUT\ B_{0-3}$	O	DISPLAY (B) OUTPUTS
$\overline{BD}$	O	BLANK DISPLAY OUTPUT

LOGIC SYMBOL



HARDWARE DESCRIPTION

The 8279 is packaged in a 40 pin DIP. The following is a functional description of each pin.

No. Of Pins	Designation	Function
8	DB_0-DB_7	Bi-directional data bus. All data and commands between the CPU and the 8279 are transmitted on these lines.
1	CLK	Clock from system used to generate internal timing.
1	RESET	A high signal on this pin resets the 8279. After being reset the 8279 is placed in the following mode: 1) 16 8-bit character display —left entry. 2) Encoded scan keyboard—2 key lockout. Along with this the program clock prescaler is set to 31.
1	$\overline{CS}$	Chip Select. A low on this pin enables the interface functions to receive or transmit.
1	A_0	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
2	$\overline{RD}$, $\overline{WR}$	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
1	IRQ	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
2	V_{SS}, V_{CC}	Ground and power supply pins.
4	SL_0-SL_3	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
8	RL_0-RL_7	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
1	SHIFT	The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
1	CNTL/STB	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in the Strobed Input mode. (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
4 4	OUT A_0-OUT A_3 OUT B_0-OUT B_3	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8 bit port.
1	$\overline{BD}$	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.

PRINCIPLES OF OPERATION

The following is a description of the major elements of the 8279 Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 1.

I/O Control and Data Buffers

The I/O control section uses the $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers. All data flow to and from the 8279 is enabled by $\overline{CS}$. The character of the information, given or desired by the CPU, is identified by A_0. A logic one means the information is a command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Buffers. The Data Buffers are bi-directional buffers that connect the internal bus to the external bus. When the chip is not selected ($\overline{CS}$ = 1), the devices are in a high impedance state. The drivers input during $\overline{WR} \bullet \overline{CS}$ and output during $\overline{RD} \bullet \overline{CS}$.

Control and Timing Registers and Timing Control

These registers store the keyboard and display modes and other operating conditions programmed by the CPU. The modes are programmed by presenting the proper command on the data lines with A_0 = 1 and then sending a $\overline{WR}$. The command is latched on the rising edge of $\overline{WR}$.

FUNCTIONAL DESCRIPTION

Since data input and display are an integral part of many microprocessor designs, the system designer needs an interface that can control these functions without placing a large load on the CPU. The 8279 provides this function for 8-bit microprocessors.

The 8279 has two sections: keyboard and display. The keyboard section can interface to regular typewriter style keyboards or random toggle or thumb switches. The display section drives alphanumeric displays or a bank of indicator lights. Thus the CPU is relieved from scanning the keyboard or refreshing the display.

The 8279 is designed to directly connect to the microprocessor bus. The CPU can program all operating modes for the 8279. These modes include:

Input Modes

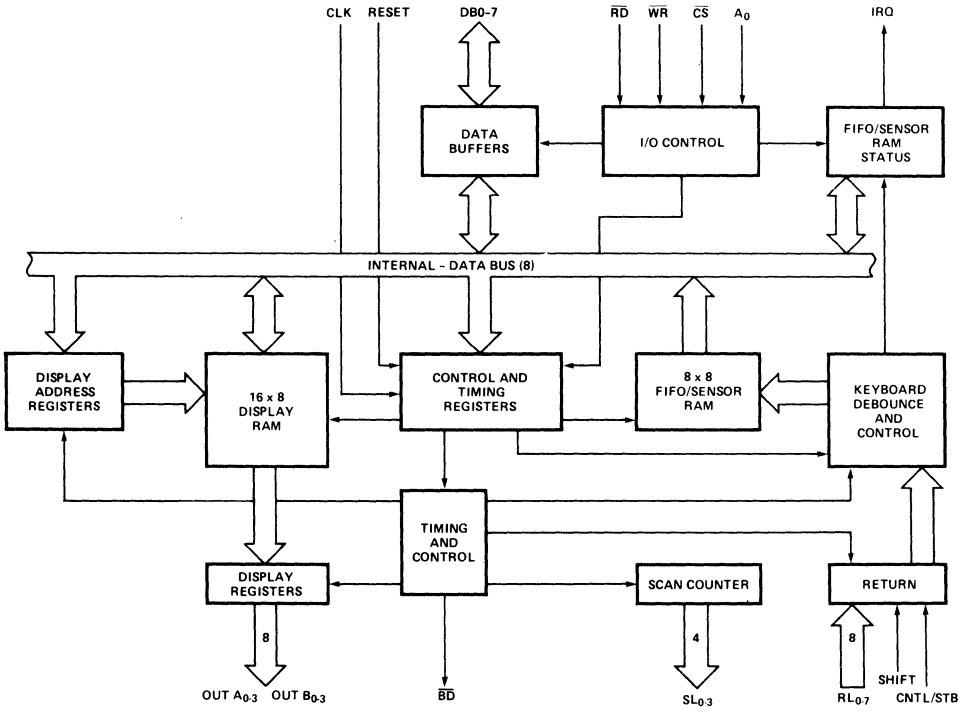
- Scanned Keyboard — with encoded (8 x 8 key keyboard) or decoded (4 x 8 key keyboard) scan lines. A key depression generates a 6-bit encoding of key position. Position and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key lockout or N-key rollover.
- Scanned Sensor Matrix — with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines. Key status (open or closed) stored in RAM addressable by CPU.
- Strobed Input — Data on return lines during control line strobe is transferred to FIFO.

Output Modes

- 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit.
- Right entry or left entry display formats.

Other features of the 8279 include:

- Mode programming from the CPU.
- Clock Prescaler
- Interrupt output to signal CPU when there is keyboard or sensor data available.
- An 8 byte FIFO to store keyboard information.
- 16 byte internal Display RAM for display refresh. This RAM can also be read by the CPU.



The command is then decoded and the appropriate function is set. The timing control contains the basic timing counter chain. The first counter is a ÷ N prescaler that can be programmed to yield an internal frequency of 100 kHz which gives a 5.1 ms keyboard scan time and a 10.3 ms debounce time. The other counters divide down the basic internal frequency to provide the proper key scan, row scan, keyboard matrix scan, and display scan times.

Scan Counter

The scan counter has two modes. In the encoded mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the keyboard and display. In the decoded mode, the scan counter decodes the least significant 2 bits and provides a decoded 1 of 4 scan. Note than when the keyboard is in decoded scan, so is the display. This means that only the first 4 characters in the Display RAM are displayed.

In the encoded mode, the scan lines are active high outputs. In the decoded mode, the scan lines are active low outputs.

Return Buffers and Keyboard Debounce and Control

The 8 return lines are buffered and latched by the Return Buffers. In the keyboard mode, these lines are scanned, looking for key closures in that row. If the debounce circuit detects a closed switch, it waits about 10 msec to check if the switch remains closed. If it does, the address of the switch in the matrix plus the status of SHIFT and CONTROL are transferred to the FIFO. In the scanned Sensor Matrix modes, the contents of the return lines is directly transferred to the corresponding row of the Sensor RAM (FIFO) each key scan time. In Strobed Input mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

FIFO/Sensor RAM and Status

This block is a dual function 8 x 8 RAM. In Keyboard or Strobed Input modes, it is a FIFO. Each new entry is written into successive RAM positions and each is then read in order of entry. FIFO status keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or writes will be recognized as an error. The status can be read by an $\overline{RD}$ with $\overline{CS}$ low and A_0 high. The status logic also provides an IRQ signal when the FIFO is not empty. In Scanned Sensor Matrix mode, the memory is a Sensor RAM. Each row of the Sensor RAM is loaded with the status of the corresponding row of sensor in the sensor matrix. In this mode, IRQ is high if a change in a sensor is detected.

Display Address Registers and Display RAM

The Display Address Registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The Display RAM can be directly read by the CPU after the correct mode and address is set. The addresses for the A and B nibbles are automatically updated by the 8279 to match data entry by the CPU. The A and B nibbles can be entered independently or as one word, according to the mode that is set by the CPU. Data entry to the display can be set to either left or right entry. See Interface Considerations for details.

SOFTWARE OPERATION

8279 commands

The following commands program the 8279 operating modes. The commands are sent on the Data Bus with $\overline{CS}$ low and A_0 high and are loaded to the 8279 on the rising edge of $\overline{WR}$.

Keyboard/Display Mode Set

	MSB							LSB
Code:	0	0	0	D	D	K	K	K

Where DD is the Display Mode and KKK is the Keyboard Mode.

DD

0	0	8 8-bit character display — Left entry
0	1	16 8-bit character display — Left entry*
1	0	8 8-bit character display — Right entry
1	1	16 8-bit character display — Right entry

For description of right and left entry, see Interface Considerations. Note that when decoded scan is set in keyboard mode, the display is reduced to 4 characters independent of display mode set.

KKK

0	0	0	Encoded Scan Keyboard — 2 Key Lockout*
0	0	1	Decoded Scan Keyboard — 2-Key Lockout
0	1	0	Encoded Scan Keyboard — N-Key Rollover
0	1	1	Decoded Scan Keyboard — N-Key Rollover
1	0	0	Encoded Scan Sensor Matrix
1	0	1	Decoded Scan Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

Code:	0	0	1	P	P	P	P	P

All timing and multiplexing signals for the 8279 are generated by an internal prescaler. This prescaler divides the external clock (pin 3) by a programmable integer. Bits PPPPP determine the value of this integer which ranges from 2 to 31. Choosing a divisor that yields 100 kHz will give the specified scan and debounce times. For instance, if Pin 3 of the 8279 is being clocked by a 2 MHz signal, PPPPP should be set to 10100 to divide the clock by 20 to yield the proper 100 kHz operating frequency.

Read FIFO/Sensor RAM

Code:	0	1	0	AI	X	A	A	A	X = Don't Care

The CPU sets up the 8279 for a read of the FIFO/Sensor RAM by first writing this command. In the Scan Key-

*Default after reset.

board Mode, the Auto-Increment flag (AI) and the RAM address bits (AAA) are irrelevant. The 8279 will automatically drive the data bus for each subsequent read ($A_0 = 0$) in the same sequence in which the data first entered the FIFO. All subsequent reads will be from the FIFO until another command is issued.

In the Sensor Matrix Mode, the RAM address bits AAA select one of the 8 rows of the Sensor RAM. If the AI flag is set (AI = 1), each successive read will be from the subsequent row of the sensor RAM.

Read Display RAM

Code:

0	1	1	AI	A	A	A	A

The CPU sets up the 8279 for a read of the Display RAM by first writing this command. The address bits AAAA select one of the 16 rows of the Display RAM. If the AI flag is set (AI = 1), this row address will be incremented after each following read *or write* to the Display RAM. Since the same counter is used for both reading and writing, this command sets the next read *or write* address and the sense of the Auto-Increment mode for both operations.

Write Display RAM

Code:

1	0	0	AI	A	A	A	A

The CPU sets up the 8279 for a write to the Display RAM by first writing this command. After writing the command with $A_0 = 1$, all subsequent writes with $A_0 = 0$ will be to the Display RAM. The addressing and Auto-Increment functions are identical to those for the Read Display RAM. However, this command does not affect the source of subsequent Data Reads; the CPU will read from whichever RAM (Display or FIFO/Sensor) which was last specified. If, indeed, the Display RAM was last specified, the Write Display RAM will, nevertheless, change the next Read location.

Display Write Inhibit/Blanking

The IW Bits can be used to mask nibble A and nibble B in applications requiring separate 4-bit display ports. By setting the IW flag (IW = 1) for one of the ports, the port becomes marked so that entries to the Display RAM from the CPU do not affect that port. Thus, if each nibble is input to a BCD decoder, the CPU may write a digit to the Display RAM without affecting the other digit being displayed. It is important to note that bit B_0 corresponds to bit D_0 on the CPU bus, and that bit A_3 corresponds to bit D_7.

If the user wishes to blank the display, the BL flags are available for each nibble. The last Clear command issued determines the code to be used as a "blank." This code defaults to all zeros after a reset. Note that both BL flags must be set to blank a display formatted with a single 8-bit port.

Clear

The C_D bits are available in this command to clear all rows of the Display RAM to a selectable blanking code as follows:

C_D	C_D	C_D	
0	X		All Zeros (X = Don't Care)
1	0		AB = Hex 20 (0010 0000)
1	1		All Ones
			Enable clear display when = 1 (or by C_A = 1)

During the time the Display RAM is being cleared (~160 μs), it may not be written to. The most significant bit of the FIFO status word is set during this time. When the Display RAM becomes available again, it automatically resets.

If the C_F bit is asserted ($C_F = 1$), the FIFO status is cleared and the interrupt output line is reset. Also, the Sensor RAM pointer is set to row 0.

C_A, the Clear All bit, has the combined effect of C_D and C_F; it uses the C_D clearing code on the Display RAM and also clears FIFO status. Furthermore, it resynchronizes the internal timing chain.

End Interrupt/Error Mode Set

Code:

1	1	1	E	X	X	X	X

X = Don't care.

For the sensor matrix modes this command lowers the IRQ line and enables further writing into RAM. (The IRQ line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset).

For the N-key rollover mode — if the E bit is programmed to "1" the chip will operate in the special Error mode. (For further details, see Interface Considerations Section.)

Status Word

The status word contains the FIFO status, error, and display unavailable signals. This word is read by the CPU when A_0 is high and $\overline{CS}$ and $\overline{RD}$ are low. See Interface Considerations for more detail on status word.

Data Read

Data is read when A_0, $\overline{CS}$ and $\overline{RD}$ are all low. The source of the data is specified by the Read FIFO or Read Display commands. The trailing edge of $\overline{RD}$ will cause the address of the RAM being read to be incremented if the Auto-Increment flag is set. FIFO reads always increment (if no error occurs) independent of AI.

Data Write

Data that is written with A_0, $\overline{CS}$ and $\overline{WR}$ low is always written to the Display RAM. The address is specified by the latest Read Display or Write Display command. Auto-Incrementing on the rising edge of $\overline{WR}$ occurs if AI set by the latest display command.

INTERFACE CONSIDERATIONS

Scanned Keyboard Mode, 2-Key Lockout

There are three possible combinations of conditions that can occur during debounce scanning. When a key is depressed, the debounce logic is set. Other depressed keys are looked for during the next two scans. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If the FIFO was empty, IRQ will be set to signal the CPU that there is an entry in the FIFO. If the FIFO was full, the key will not be entered and the error flag will be set. If another closed switch is encountered, no entry to the FIFO can occur. If all other keys are released before this one, then it will be entered to the FIFO. If this key is released before any other, it will be entirely ignored. A key is entered to the FIFO only once per depression, no matter how many keys were pressed along with it or in what order they were released. If two keys are depressed within the debounce cycle, it is a simultaneous depression. Neither key will be recognized until one key remains depressed alone. The last key will be treated as a single key depression.

Scanned Keyboard Mode, N-Key Rollover

With N-key Rollover each key depression is treated independently from all others. When a key is depressed, the debounce circuit waits 2 keyboard scans and then checks to see if the key is still down. If it is, the key is entered into the FIFO. Any number of keys can be depressed and another can be recognized and entered into the FIFO. If a simultaneous depression occurs, the keys are recognized and entered according to the order the keyboard scan found them.

Scanned Keyboard — Special Error Modes

For N-key rollover mode the user can program a special error mode. This is done by the "End Interrupt/Error Mode Set" command. The debounce cycle and key-validity check are as in normal N-key mode. If during a single debounce cycle, two keys are found depressed, this is considered a simultaneous multiple depression, and sets an error flag. This flag will prevent any further writing into the FIFO and will set interrupt (if not yet set). The error flag could be read in this mode by reading the FIFO STATUS word. (See "FIFO STATUS" for further details.) The error flag is reset by sending the normal CLEAR command with $C_F = 1$.

Sensor Matrix Mode

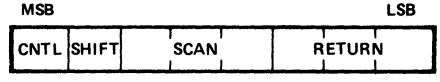
In Sensor Matrix mode, the debounce logic is inhibited. The status of the sensor switch is inputted directly to the Sensor RAM. In this way the Sensor RAM keeps an image of the state of the switches in the sensor matrix. Although debouncing is not provided, this mode has the advantage that the CPU knows how long the sensor was closed and when it was released. A keyboard mode can only indicate a validated closure. To make the software easier, the designer should functionally group the sensors by row since this is the format in which the CPU will read them.

The IRQ line goes high if any sensor value change is detected at the end of a sensor matrix scan. The IRQ line is cleared by the first data read operation if the Auto-Increment flag is set to zero, or by the End Interrupt command if the Auto-Increment flag is set to one.

Note: Multiple changes in the matrix Addressed by ($SL_{0-3} = 0$) may cause multiple interrupts. ($SL_0 = 0$ in the Decoded Mode). Reset may cause the 8279 to see multiple changes.

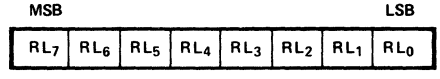
Data Format

In the Scanned Keyboard mode, the character entered into the FIFO corresponds to the position of the switch in the keyboard plus the status of the CNTL and SHIFT lines (non-inverted). CNTL is the MSB of the character and SHIFT is the next most significant bit. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.

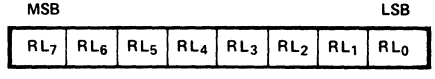


SCANNED KEYBOARD DATA FORMAT

In Sensor Matrix mode, the data on the return lines is entered directly in the row of the Sensor RAM that corresponds to the row in the matrix being scanned. Therefore, each switch postion maps directly to a Sensor RAM position. The SHIFT and CNTL inputs are ignored in this mode. Note that switches are not necessarily the only thing that can be connected to the return lines in this mode. Any logic that can be triggered by the scan lines can enter data to the return line inputs. Eight multiplexed input ports could be tied to the return lines and scanned by the 8279.



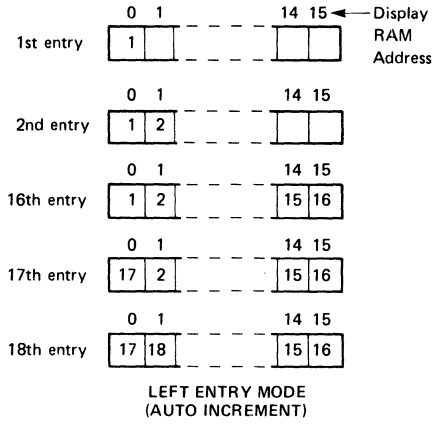
In Strobed Input mode, the data is also entered to the FIFO from the return lines. The data is entered by the rising edge of a CNTL/STB line pulse. Data can come from another encoded keyboard or simple switch matrix. The return lines can also be used as a general purpose strobed input.



Display

Left Entry

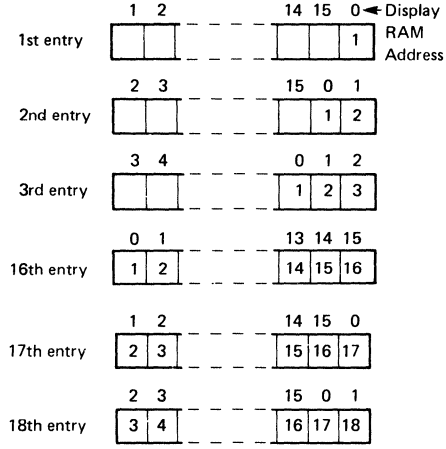
Left Entry mode is the simplest display format in that each display position directly corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 (or address 7 in 8 character display) is the right most display character. Entering characters from position zero causes the display to fill from the left. The 17th (9th) character is entered back in the left most position and filling again proceeds from there.



LEFT ENTRY MODE
(AUTO INCREMENT)

Right Entry

Right entry is the method used by most electronic calculators. The first entry is placed in the right most display character. The next entry is also placed in the right most character after the display is shifted left one character. The left most character is shifted off the end and is lost.

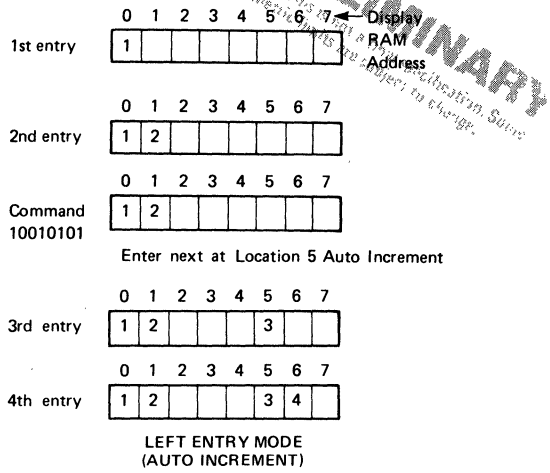


RIGHT ENTRY MODE
(AUTO INCREMENT)

Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended.

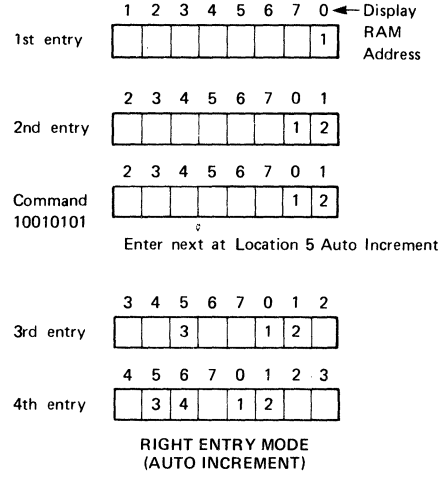
Auto Increment

In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Auto Increment mode has no undesirable side effects and the result is predictable:



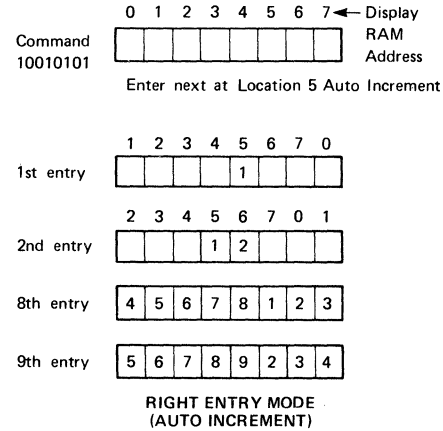
LEFT ENTRY MODE
(AUTO INCREMENT)

In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except if the address sequence is interrupted:



RIGHT ENTRY MODE
(AUTO INCREMENT)

Starting at an arbitrary location operates as shown below:



RIGHT ENTRY MODE
(AUTO INCREMENT)

Entry appears to be from the initial entry point.

8/16 Character Display Formats

If the display mode is set to an 8 character display, the on duty-cycle is double what it would be for a 16 character display (e.g., 5.1 ms scan time for 8 characters vs. 10.3 ms for 16 characters with 100 kHz internal frequency).

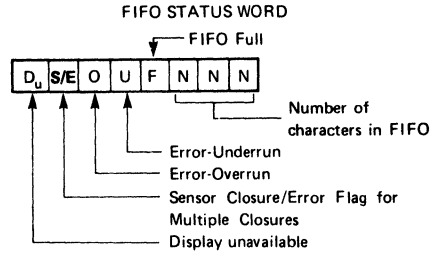
G. FIFO Status

FIFO status is used in the Keyboard and Strobed Input modes to indicate the number of characters in the FIFO and to indicate whether an error has occurred. There are two types of errors possible: overrun and underrun. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO.

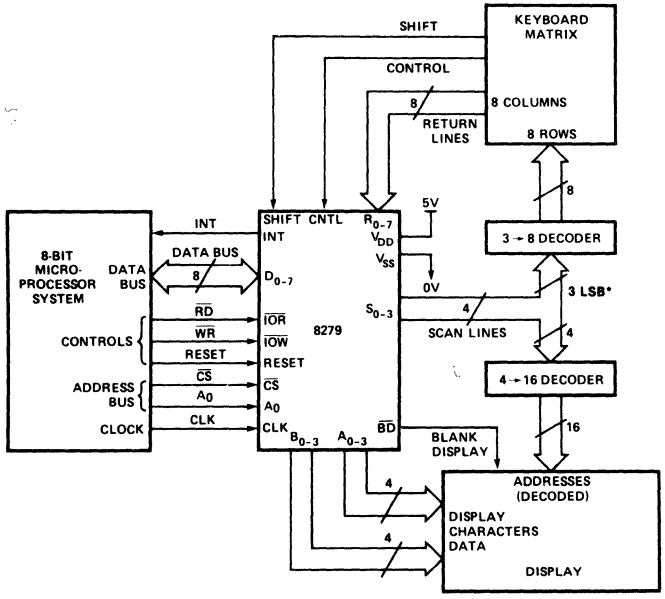
The FIFO status word also has a bit to indicate that the Display RAM was unavailable because a Clear Display or Clear All command had not completed its clearing operation.

In a Sensor Matrix mode, a bit is set in the FIFO status word to indicate that at least one sensor closure location is contained in the Sensor RAM.

In Special Error Mode the S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.



APPLICATIONS



*Do not drive the keyboard decoder with the MSB of the scan lines.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to 125°C
Voltage on any Pin with
Respect to Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . .1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS} = 0V, Note 1

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL1}	Input Low Voltage for Return Lines	-0.5	1.4	V	
V_{IL2}	Input Low Voltage for All Others	-0.5	0.8	V	
V_{IH1}	Input High Voltage for Return Lines	2.2		V	
V_{IH2}	Input High Voltage for All Others	2.0		V	
V_{OL}	Output Low Voltage		0.45	V	Note 2
V_{OH}	Output High Voltage on Interrupt Line	3.5		V	Note 3
I_{IL1}	Input Current on Shift, Control and Return Lines		+10 -100	μA μA	$V_{IN} = V_{CC}$ V_{IN} = 0V
I_{IL2}	Input Leakage Current on All Others		±10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ to 0V
I_{CC}	Power Supply Current		120	mA	

Notes:
1. 8279, V_{CC} = +5V ±5%; 8279-5, V_{CC} = +5V ±10%.
2. 8279, I_{OL} = 1.6mA; 8279-5, I_{OL} = 2.2mA.
3. 8279, I_{OH} = -100μA; 8279-5, I_{OH} = -400μA.

CAPACITANCE

SYMBOL	TEST	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{in}	Input Capacitance	5	10	pF	$V_{in}=V_{CC}$
C_{out}	Output Capacitance	10	20	pF	$V_{out}=V_{CC}$

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS} = 0V, (Note 1)

Bus Parameters

Read Cycle:

Symbol	Parameter	8279 Min.	8279 Max.	8279-5 Min.	8279-5 Max.	Unit
t_{AR}	Address Stable Before $\overline{READ}$	50		0		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		0		ns
t_{RR}	$\overline{READ}$ Pulse Width	420		250		ns
t_{RD}[2]	Data Delay from $\overline{READ}$		300		150	ns
t_{AD}[2]	Address to Data Valid		450		250	ns
t_{DF}	$\overline{READ}$ to Data Floating	10	100	10	100	ns
t_{RCY}	Read Cycle Time	1		1		μs

Write Cycle:

Symbol	Parameter	8279 Min.	8279 Max.	8279-5 Min.	8279-5 Max.	Unit
t_{AW}	Address Stable Before $\overline{WRITE}$	50		0		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		0		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		250		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		150		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		0		ns

Notes:
1. 8279, V_{CC} = +5V ±5%; 8279-5, V_{CC} = +5V ±10%.
2. 8279, C_L = 100pF; 8279-5, C_L = 150pF.

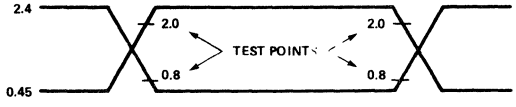
Other Timings:

Symbol	Parameter	8279 Min.	8279 Max.	8279-5 Min.	8279-5 Max.	Unit
$t_{\phi W}$	Clock Pulse Width	230		120		nsec
t_{CY}	Clock Period	500		320		nsec

Keyboard Scan Time:	5.1 msec	Digit-on Time:	480 μsec
Keyboard Debounce Time:	10.3 msec	Blanking Time:	160 μsec
Key Scan Time:	80 μsec	Internal Clock Cycle:	10 μsec
Display Scan Time:	10.3 msec		

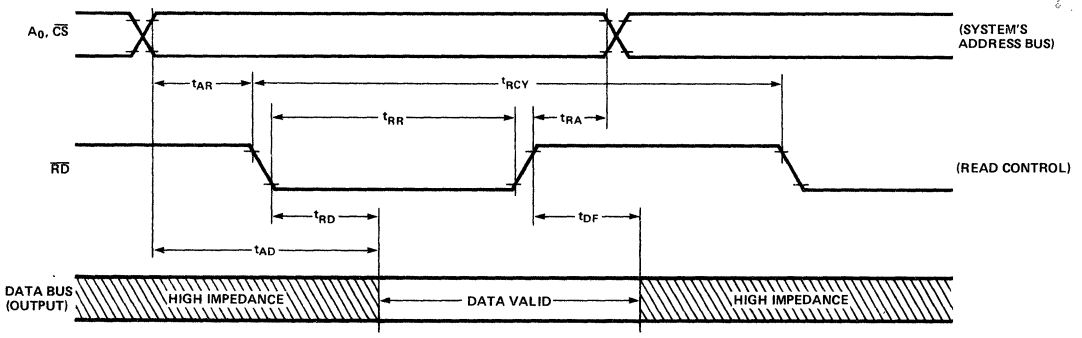
MPU PERIPHERALS

Input Waveforms For A.C. Tests

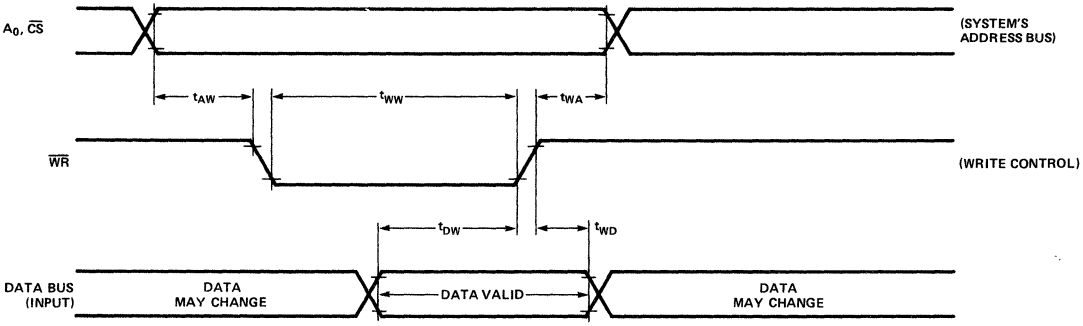


WAVEFORMS

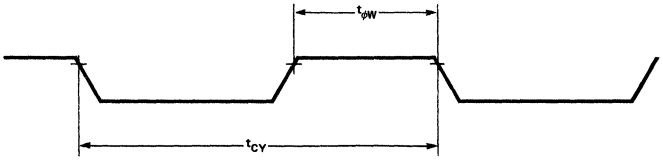
Read Operation



Write Operation

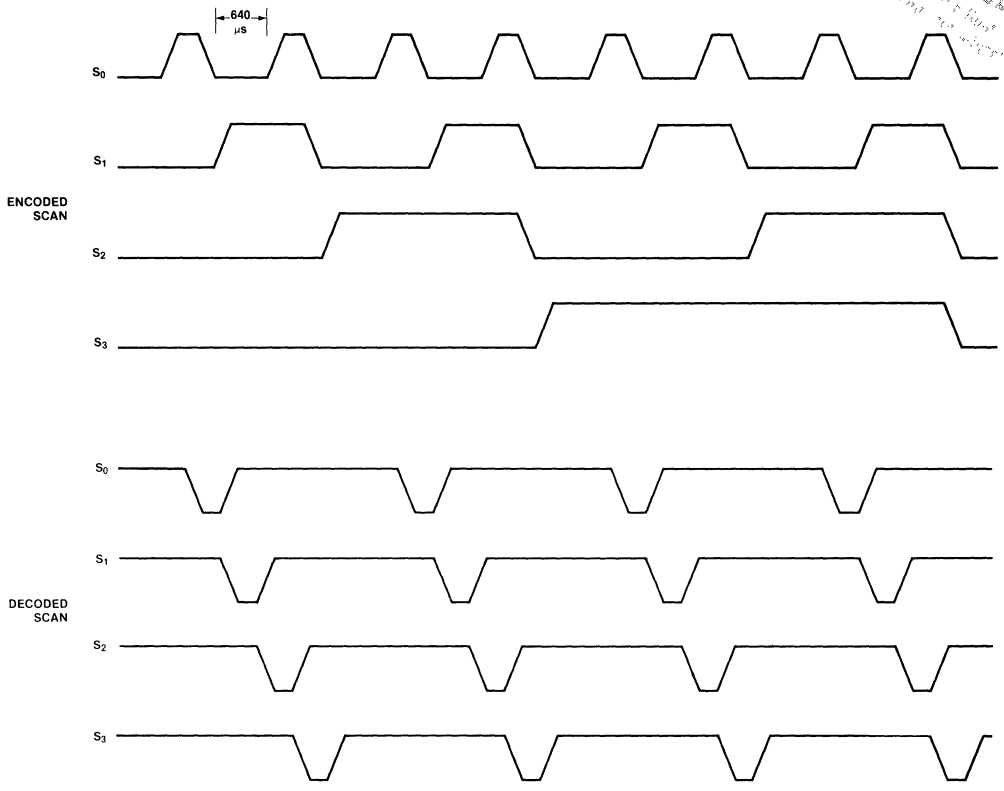


Clock Input

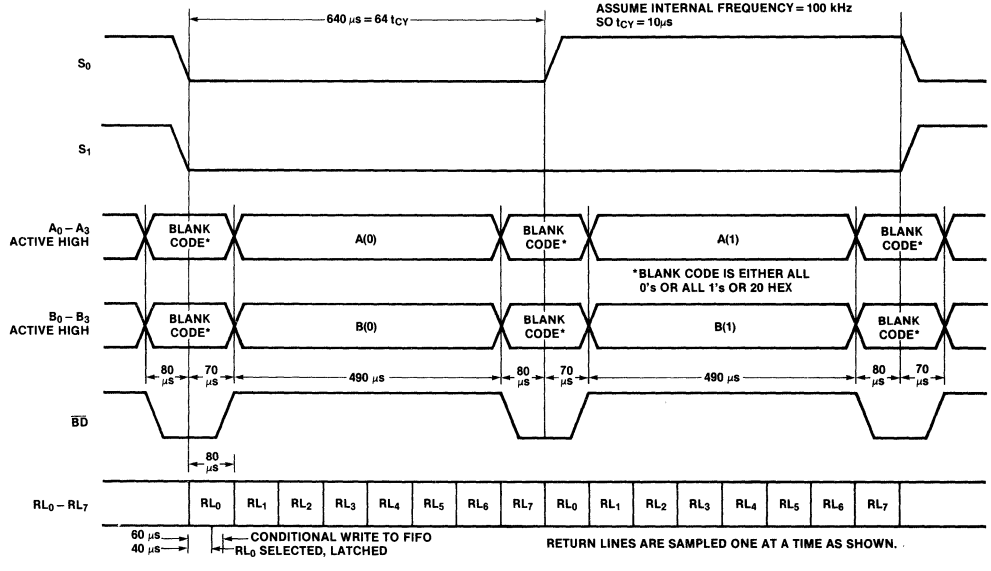


MPU PERIPHERALS

SCAN WAVEFORMS



DISPLAY WAVEFORMS



NOTE: SHOWN IS ENCODED SCAN LEFT ENTRY
S_2-S_3 ARE NOT SHOWN BUT THEY ARE SIMPLY S_1 DIVIDED BY 2 AND 4

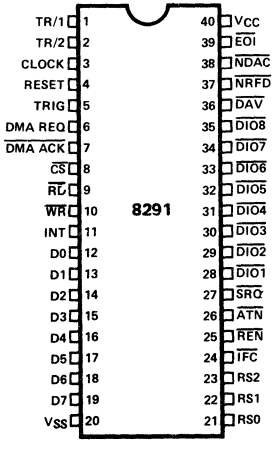
8291
GPIB TALKER/LISTENER

- Designed to Interface Microprocessors (e.g., 8080, 8085, 8086, 8048) to an IEEE Standard 488 Digital Interface Bus
- Programmable Data Transfer Rate
- Complete Source and Acceptor Handshake
- Complete Talker and Listener Functions with Extended Addressing
- Service Request, Parallel Poll, Device Clear, Device Trigger, Remote/Local Functions
- Selectable Interrupts
- On-Chip Primary and Secondary Address Recognition
- Automatic Handling of Addressing and Handshake Protocol
- Provision for Software Implementation of Additional Features
- 1 – 8 MHz Clock Range
- 16 Registers (8 Read, 8 Write), 2 for Data Transfer, the Rest for Interface Function Control, Status, etc.
- Directly Interfaces to External Non-Inverting Transceivers for Connection to the GPIB
- Provides Three Addressing Modes, Allowing the Chip to be Addressed Either as a Major or a Minor Talker/Listener with Primary or Secondary Addressing
- DMA Handshake Provision Allows for Bus Transfers without CPU Intervention
- Trigger Output Pin
- On-Chip EOS (End of Sequence) Message Recognition Facilitates Handling of Multi-Byte Transfers

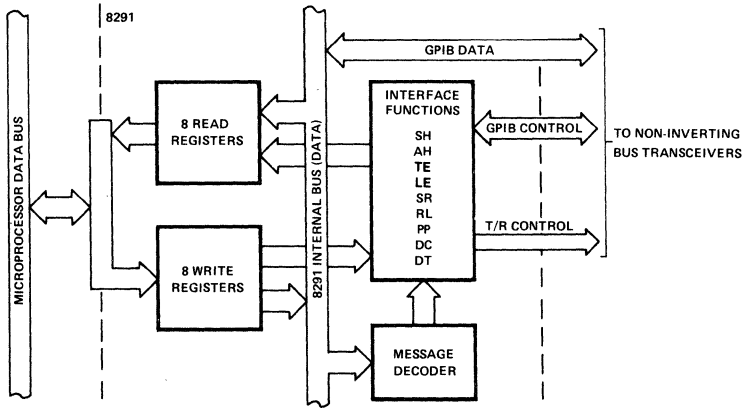
The 8291 GPIB Talker/Listener is a microprocessor-controlled chip designed to interface microprocessors (e.g., 8048, 8080, 8085, 8086) to an IEEE Standard 488 Instrumentation Interface Bus. It implements all of the Standard's interface functions except for the controller.

MPU PERIPHERALS

PIN CONFIGURATION



BLOCK DIAGRAM

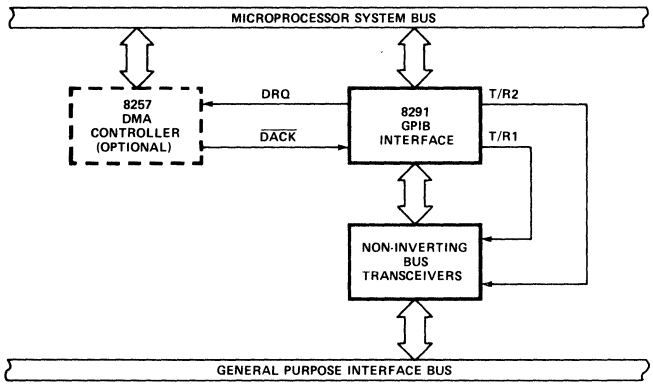


PIN DESCRIPTION

Symbol	I/O	Pin No.	Function
D_0-D_7	I/O	12-19	Data bus port, to be connected to microprocessor data bus.
RS_0-RS_2	I	21-23	Register select inputs, to be connected to three non-multiplexed microprocessor address bus lines. Select which of the 8 internal read (write) registers will be read from (written into) with the execution of $\overline{RD}$ ($\overline{WR}$).
$\overline{CS}$	I	8	Chip select. When low, enables reading from or writing into the register selected by RS_0-RS_2.
$\overline{RD}$	I	9	Read strobe. When low, selected register contents are read by the CPU.
$\overline{WR}$	I	10	Write strobe. When low, data is written into the selected register.
INT ($\overline{INT}$)	O	11	Interrupt request to the microprocessor, set high for request and cleared when the appropriate register is accessed by the CPU. May be software configured to be active low.
DMA REQ	O	6	DMA request, normally low, set high to indicate byte output or byte input, in DMA mode; reset by DMA ACK.
$\overline{DMA\ ACK}$	I	&	DMA acknowledge. When low, resets DMA REQ and selects data in/data out register for DMA data transfer (actual transfer done by $\overline{RD}$/$\overline{WR}$ pulse).
TRIG	O	5	Trigger output, normally low; generates a triggering pulse corresponding to the GET command.
CLOCK	I	3	External clock input, used for internal time delays generator. May be any speed in 1-8 MHz range.
RESET	I	4	Reset input. When high, forces the device into an "Idle" (initialization) mode. The device will remain at "Idle" until released by the microprocessor.
$\overline{DIO_1}$-$\overline{DIO_8}$	I/O	28-35	8-bit GPIB data port, used for bidirectional data byte transfer between 8291 and GPIB via non-inverting external line transceivers.
$\overline{DAV}$	I/O	36	Data valid; GPIB handshake control line. Indicates the availability and validity of information on the DIO lines.
$\overline{NRFD}$	I/O	37	Not ready for data; GPIB handshake control line. Indicates the condition of readiness of device(s) connected to the bus to accept data.
$\overline{NDAC}$	I/O	38	Not data accepted; GPIB handshake control line. Indicates the condition of acceptance of data by the device(s) connected to the bus.
$\overline{ATN}$	I	26	Attention; GPIB command line. Specifies how data on DIO lines are to be interpreted.
$\overline{IFC}$	I	24	Interface clear; GPIB command line. Places the interface functions in a known quiescent state.
$\overline{SRQ}$	O	27	Service request; GPIB command line. Indicates the need for attention and requests an interruption of the current sequence of events on the GPIB.
$\overline{REN}$	I	25	Remote enable; GPIB command line. Selects (in conjunction with other messages) remote or local control of the device.
$\overline{EOI}$	I/O	39	End or identify; GPIB command line. Indicates the end of a multiple byte transfer sequence or, in conjunction with ATN, addresses the device during a polling sequence.
T/R1	O	1	External transceivers control line. Set high to indicate output data/signals on the DIO_1-DIO_8 and DAV lines and input signals on the NRFD and NDAC lines (active source handshake). Set low to indicate input data/signals on the DIO_1-DIO_8 and DAV lines and output signals on the NRFD and NDAC lines (active acceptor handshake).
T/R2	O	2	External transceivers control line. Set high to indicate output signals on the EOI line. Set low to indicate expected input signal on the EOI line during parallel poll.
V_{CC}	P.S.	40	Positive power supply (5V ± 10%).
GND	P.S.	20	Potential ground circuit.

Note: all signals on the 8291 pins are specified with positive logic. However, IEEE 488 specifies negative logic on its 16 signal lines.

8291 SYSTEM DIAGRAM



THE GENERAL PURPOSE INTERFACE BUS (GPIB)

The General Purpose Interface Bus (GPIB) is defined in the IEEE Standard 488-1975 "Digital Interface for Programmable Instrumentation." Although a knowledge of this standard is assumed, Figure 1 provides the bus structure for quick reference. Also, Tables 1 and 2 reference the interface state mnemonics and the interface messages respectively. Modified state diagrams for the 8291 are presented in Appendix A.

GENERAL DESCRIPTION

The 8291 is a microprocessor controlled device designed to interface microprocessors e.g., 8048, 8080, 8085, 8086 to the GPIB. It implements all of the interface functions defined in the IEEE 488 Standard. If an implementation of the Standard's Controller function is desired, it can be connected with an Intel® 8292 to form a complete interface.

The 8291 handles communication between a microprocessor controlled device and the GPIB. Its capabilities include data transfer, handshake protocol, talker/listener addressing procedures, device clearing and triggering, service request, and both serial and parallel polling schemes. In most procedures, it does not disturb the microprocessor unless a byte is waiting on input or a byte sent on output (output buffer empty).

The 8291 architecture includes 16 registers. Eight of these registers may be written into by the microprocessor. The other eight registers may be read by the microprocessor. One each of these read and write registers is for direct data transfers. The rest of the write registers control the various features of the chip, while the rest of the read registers provide the microprocessor with a monitor of GPIB states, various bus conditions, and device conditions.

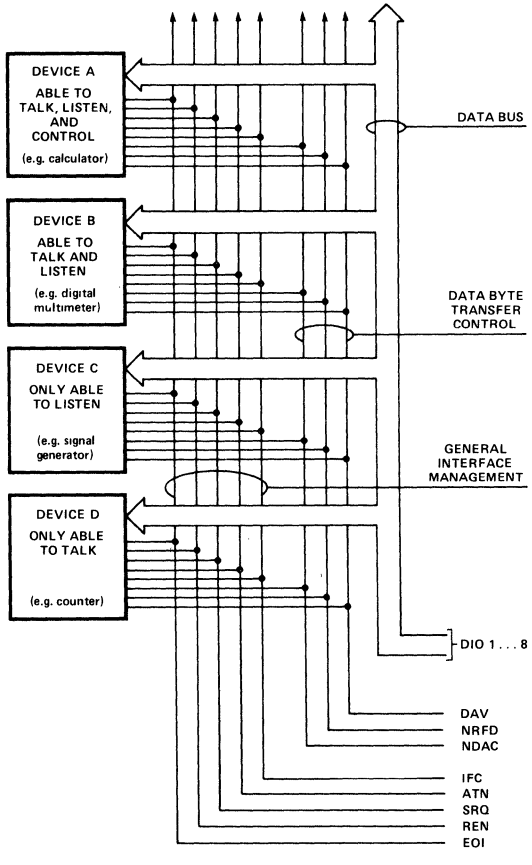


Figure 1. Interface Capabilities and Bus Structure.

GPIB Addressing

Each device connected to the GPIB must have at least one address whereby the controller device in charge of the bus can configure it to talk, listen, or send status. An 8291 implementation of the GPIB offers the user three addressing modes from which the device can be initialized for each application. The first of these modes allows for the device to have two separate primary addresses. The second mode allows the user to implement a single talker/listener with a two byte address (primary address + secondary address). The third mode again allows for two distinct addresses but in this instance, they can each have a two-byte address. However, this mode requires that the secondary addresses be passed to the microprocessor for verification. These three addressing schemes are described in more detail in the discussion of the Address registers.

TABLE 1.
IEEE 488 INTERFACE STATE MNEMONICS

Mnemonic	State Represented
ACDS	Accept Data State
ACRS	Acceptor Ready State
AIDS	Acceptor Idle State
ANRS	Acceptor Not Ready State
APRS	Affirmative Poll Response State
AWNS	Acceptor Wait for New Cycle State
CACS	Controller Active State
CADS	Controller Addressed State
CAWS	Controller Active Wait State
CIDS	Controller Idle State
CPPS	Controller Parallel Poll State
CPWS	Controller Parallel Poll Wait State
CSBS	Controller Standby State
CSNS	Controller Service Not Requested State
CSRS	Controller Service Requested State
CSWS	Controller Synchronous Wait State
CTRS	Controller Transfer State
DCAS	Device Clear Active State
DCIS	Device Clear Idle State
DTAS	Device Trigger Active State
DTIS	Device Trigger Idle State
LACS	Listener Active State
LADS	Listener Addressed State
LIDS	Listener Idle State
LOCS	Local State
LPAS	Listener Primary Addressed State
LPIS	Listener Primary Idle State
LWLS	Local With Lockout State
NPRS	Negative Poll Response State

Mnemonic	State Represented
PACS	Parallel Poll Addressed to Configure State
PPAS	Parallel Poll Active State
PPIS	Parallel Poll Idle State
PPSS	Parallel Poll Standby State
PUCS	Parallel Poll Unaddressed to Configure State
REMS	Remote State
RWLS	Remote With Lockout State
SACS	System Control Active State
SDYS	Source Delay State
SGNS	Source Generate State
SIAS	System Control Interface Clear Active State
SIDS	Source Idle State
SIIS	System Control Interface Clear Idle State
SINS	System Control Interface Clear Not Active State
SIWS	Source Idle Wait State
SNAS	System Control Not Active State
SPAS	Serial Poll Active State
SPIS	Serial Poll Idle State
SPMS	Serial Poll Mode State
SRAS	System Control Remote Enable Active State
SRIS	System Control Remote Enable Idle State
SRNS	System Control Remote Enable Not Active State
SRQS	Service Request State
STRS	Source Transfer State
SWNS	Source Wait for New Cycle State
TACS	Talker Active State
TADS	Talker Addressed State
TIDS	Talker Idle State
TPIS	Talker Primary Idle State

– – – – – – The Controller function is implemented on the Intel® 8292.

TABLE 2.
IEEE 488 INTERFACE MESSAGE REFERENCE LIST

Mnemonic	Message	Interface Function(s)
LOCAL MESSAGES RECEIVED (By Interface Functions)		
*gts	go to standby	C
ist	individual status	PP
lon	listen only	L, LE
lpe	local poll enable	PP
nba	new byte available	SH
pon	power on	SH,AH,T,TE,L,LE,SR,RL,PP,C
rdy	ready	AH
*rpp	request parallel poll	C
*rsc	request system control	C
rsv	request service	SR
rtl	return to local	RL
*sic	send interface clear	C
*sre	send remote enable	C
*tca	take control asynchronously	C
*tcs	take control synchronously	AH, C
ton	talk only	T, TE
REMOTE MESSAGES RECEIVED		
ATN	Attention	SH,AH,T,TE,L,LE,PP,C
DAB	Data Byte	(Via L, LE)
DAC	Data Accepted	SH
DAV	Data Valid	AH
DCL	Device Clear	DC
END	End	(via L, LE)
GET	Group Execute Trigger	DT
GTL	Go to Local	RL
IDY	Identify	L,LE,PP
IFC	Interface Clear	T,TE,L,LE,C
LLO	Local Lockout	RL
MLA	My Listen Address	L,LE,RL,T,TE
MSA	My Secondary Address	TE,LE,RL
MTA	My Talk Address	T,TE,L,LE
OSA	Other Secondary Address	TE
OTA	Other Talk Address	T, TE
PCG	Primary Command Group	TE,LE,PP
†PPC	Parallel Poll Configure	PP
†[PPD)	Parallel Poll Disable	PP
†[PPE]	Parallel Poll Enable	PP
*PPR_N	Parallel Poll Response N	(via C)
†PPU	Parallel Poll Unconfigure	PP
REN	Remote Enable	RL
RFD	Ready for Data	SH
RQS	Request Service	(via L, LE)
[SDC]	Select Device Clear	DC
SPD	Serial Poll Disable	T, TE
SPE	Serial Poll Enable	T, TE
*SQR	Service Request	(via C)
STB	Status Byte	(via L, LE)
*TCT or [TCT]	Take Control	C
UNL	Unlisten	L, LE

*These messages are handled only by Intel's 8292.
†Undefined commands which may be passed to the microprocessor.

TABLE 2. (Cont'd)
IEEE 488 INTERFACE MESSAGE REFERENCE LIST

Mnemonic	Message	** Interface Function(s)
REMOTE MESSAGES SENT		
ATN	Attention	C
DAB	Data Byte	(via T, TE)
DAC	Data Accepted	AH
DAV	Data Valid	SH
DCL	Device Clear	(via C)
END	End	(via T)
GET	Group Execute Trigger	(via C)
GTL	Go to Local	(via C)
IDY	Identify	C
IFC	Interface Clear	C
LLO	Local Lockout	(via C)
MLA or [MLA]	My Listen Address	(via C)
MSA or [MSA]	My Secondary Address	(via C)
MTA or [MTA]	My Talk Address	(via C)
OSA	Other Secondary Address	(via C)
OTA	Other Talk Address	(via C)
PCG	Primary Command Group	(via C)
PPC	Parallel Poll Configure	(via C)
[PPD]	Parallel Poll Disable	(via C)
[PPE]	Parallel Poll Enable	(via C)
PPR_N	Parallel Poll Response N	PP
PPU	Parallel Poll Unconfigure	(via C)
REN	Remote Enable	C
RFD	Ready for Data	AH
RQS	Request Service	T, TE
[SDC]	Selected Device Clear	(via C)
SPD	Serial Poll Disable	(via C)
SPE	Serial Poll Enable	(via C)
SRQ	Service Request	SR
STB	Status Byte	(via T, TE)
TCT	Take Control	(via C)
UNL	Unlisten	(via C)

**All Controller messages must be sent via Intel's 8292.

8291 Registers

A bit-by-bit map of the 16 registers on the 8291 is presented in Table 3. A more detailed explanation of each of these registers and their functions follows. The access of these registers by the microprocessor is accomplished by using the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and RS_0-RS_2 pins.

Register	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	RS_0-RS_2
All Read Registers	0	0	1	CCC
All Write Registers	0	1	0	CCC
Don't Care	1	X	X	XXX

TABLE 3. 8291 REGISTERS

READ REGISTERS								RS2	RS1	RS0	WRITE REGISTERS							
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	0	0	0	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
DATA IN											DATA OUT							
CPT	APT	GET	END	DEC	ERR	BO	BI	0	0	1	CPT	APT	GET	END	DEC	ERR	BO	BI
INTERRUPT STATUS 1											INTERRUPT MASK 1							
INT	SPAS	LLO	REM	SPASC	LLOC	REMC	ADSC	0	1	0	0	0	DMAO	DMAI	SPASC	LLOC	REMC	ADSC
INTERRUPT STATUS 2											INTERRUPT MASK 2							
S8	SRQS	S6	S5	S4	S3	S2	S1	0	1	1	S8	rsv	S6	S5	S4	S3	S2	S1
SERIAL POLL STATUS											SERIAL POLL MODE							
ton	lon	EOI	LPAS	TPAS	LA	TA	MJMN	1	0	0	TO	LO	0	0	0	0	ADM1	ADM0
ADDRESS STATUS											ADDRESS MODE							
CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0	1	0	1	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0
COMMAND PASS THROUGH											AUX MODE							
X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0	1	1	0	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
ADDRESS 0											ADDRESS 0/1							
X	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1	1	1	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
ADDRESS 1											EOS							

Data Registers

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

DATA-IN REGISTER (0R)

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

DATA-OUT REGISTER (0W)

The data-in register is used to move data from the GPIB to the microprocessor or to memory when the 8291 is addressed to listen. Incoming information is separately latched by this register, and its contents are not destroyed by a write to the data-out register. The RFD (Ready for Data) message is held false until the byte is removed from the data in register, either by the microprocessor or by DMA. The 8291 then completes the handshake automatically. In RFD/DAV holdoff mode (see Auxiliary Register A), the handshake is not finished until a command is sent telling the 8291 to release the holdoff. In this way, the same byte may be read several times, or an over anxious talker may be held off until all available data has been processed.

When the 8291 is addressed to talk, it uses the data-out register to move data onto the GPIB. Upon a write to this register, the 8291 initiates and completes the handshake while sending the byte out over the bus. When the RFD/DAV holdoff mode is in effect, data is held until the release command is issued. Also, a read of the data-in register does not destroy the information in the data-out register.

Interrupt Registers

CPT	APT	GET	END	DEC	ERR	BO	BI

INTERRUPT STATUS 1 (1R)

CPT	APT	GET	END	DEC	ERR	BO	BI

INTERRUPT MASK 1 (1W)

INT	SPAS	LLO	REM	SPASC	LLOC	REMC	ADSC

INTERRUPT STATUS 2 (2R)

0	0	DMAO	DMAI	SPASC	LLOC	REMC	ADSC

INTERRUPT MASK 2 (2W)

The 8291 can be configured to generate an interrupt to the microprocessor upon the occurrence of any of 12 conditions or events on the GPIB. Upon receipt of an interrupt, the microprocessor must read the Interrupt Status registers to determine which event has occurred, and then execute the appropriate service routine (if necessary). Each of the 12 interrupt status bits has a matching mask bit in the interrupt mask registers. These mask bits are used to select the events that will cause the INT pin to be asserted. Writing a logic "1" into any of these bits enables the corresponding interrupt status bits to generate an interrupt. Bits in the Interrupt Status registers are set regardless of the states of the mask bits. The Interrupt Status registers are then cleared upon being read or when a local pon (power-on) message is executed. If an event occurs while one of the Interrupt Status registers is being read, the event is typically held until after its register is cleared and then placed in the register.

The mnemonics for each of the bits in these registers and a brief description of their respective functions appears in Table 4. This table also indicates how each of the interrupt bits is set.

TABLE 4. Interrupt Bits

Indicates Undefined Commands	CPT	An undefined command has been received.
Set by (TPAS + LPAS)•SCG•ACDS•MODE 3	APT	A secondary address must be passed through to the microprocessor for recognition.
Set by DTAS	GET	A group execute trigger has occurred.
Set by (EOS + EOI)•LACS	END	An EOS or EOI message has been received.
Set by DCAS	DEC	Device Clear Active State has occurred.
Set by TACS•nba•DAC•RFD	ERR	Interface error has occurred; no listeners are active.
TACS•(SWNS + SGNS)	BO	A byte has been output.
Set by LACS•ACDS	BI	A byte has been input.
Shows status of the INT pin	INT	These are status only. They will not generate interrupts, nor do they have corresponding mask bits.
The device has been enabled for a serial poll	SPAS	
The device is in local lock out state. (LWLS+RWLS)	LLO	
The device is in a remote state. (REMS+RWLS)	REM	
SPAS ⇄ $\overline{\text{SPAS}}$	SPASC	Serial Poll Active State change interrupt
LLO ⇄ NO LLO	LLOC	Local lock out change interrupt.
Remote ⇄ Local	RLC	Remote/Local change interrupt.
Addressed ⇄ Unaddressed	ADSC	Address status change interrupt.*

*In ton (talk-only) and lon (listen-only) modes, no ADSC interrupt is generated.

The BO and BI interrupts enable the user to perform data transfer cycles. BO indicates that a byte has been sent to the GPIB and a new data byte may be written into the Data Out register. It is set by the occurrence of TACS • (SWNS + SGNS). Hence, it is reset when a data byte is written into the Data Out register, when ATN is asserted on the GPIB, or when the device stops being addressed to talk. Similarly, BI is set when an input byte is accepted into the 8291 and reset when the microprocessor reads the Data In register. BO and BI are also reset by pon (power-on local message) and by a read of the Interrupt Status 1 register. However, if it is so desired, data transfer cycles may be performed without reading the Interrupt Status 1 register if all interrupts except for BO or BI are masked; BO and BI will automatically reset after each byte is transferred.

If the 8291 is used without DMA, the BO and BI interrupts may be enabled through the DMA REQ pin. The DMAO and DMAI bits in the Interrupt Mask 2 register would be the corresponding mask bits for this feature. Thus, implementing this feature, with BO and BI masked from the INT pin, allows for servicing of these interrupts without reading the Interrupt Status registers.

The ERR bit is set to indicate the bus error condition where the 8291 is an active talker, tries sending a byte to the GPIB, but there are no active listeners (e.g., all devices on the GPIB are in AIDS). The logical equivalent of (nba • TACS • DAC • RFD) will set this bit.

The DEC bit is set whenever DCAS has occurred. The user must define a known state to which all device functions will return in DCAS. Typically this state will be a power-on state. However, the state of the device functions at DCAS is at the designer's discretion. It should be noted that DCAS has no effect on the interface functions which are returned to a known state by the IFC (interface clear) message or the pon local message.

The End Interrupt bit may be used by the microprocessor to detect that a multi-byte transfer has been completed. The bit will be set when the 8291 is an active listener (LACS) and either EOS or EOI is received. EOS will generate an interrupt when the byte in the Data In register matches the byte in the EOS register. Otherwise the interrupt will be generated when a true input is detected at the EOI pin of the 8291.

The GET interrupt bit is used by the microprocessor to detect that DTAS has occurred. It is set by the 8291 when the GET message is received while it is addressed to listen. The TRIG output pin of the 8291 is also asserted when the GET message is received. Thus, the basic operation of the device may be started without involving the microprocessor.

The APT interrupt bit indicates to the processor that a secondary address is available in the CPT register for validation. This interrupt will only occur if Mode 3 addressing is in effect. (Refer to the section on addressing.) In Mode 2, secondary addresses will be recognized on the 8291. They will be ignored in Mode 1.

The CPT interrupt bit flags the occurrence of an undefined command and of all secondary commands following an undefined command. The Command pass through feature is enabled by the BO bit of Auxiliary register B.

$$UDC = [\overline{UCG} + ACG(TADS \bullet \overline{PPC} + LADS \bullet \overline{TCT})] \bullet undefined \bullet BO$$

where:

ACG — Addressed Command Group
UCG — Universal Command Group
SCG — Secondary Command Group

Any message not decoded by the 8291 (not included in the state diagrams in Appendix B) becomes an undefined command. Note from the logic equation that any addressed command is automatically ignored when the 8291 is not addressed.

Undefined commands are read by the CPU from the Command Pass Through Register of the 8291. Until this register is read, the 8291 will hold off the handshake (only if the CPT feature is enabled).

An especially useful feature of the 8291 is its ability to generate interrupts from state transitions in the interface functions. In particular, the lower 4 bits of the Interrupt Status 2 register, if enabled by the corresponding mask bits, will cause an interrupt upon changes in the following states as defined in IEEE 488:

Bit 0	ADSC	change in LIDS or TIDS or MJMN
Bit 1	RLC	change in LOCS or REMS
Bit 2	LLOC	change in LWLS or RWLS
Bit 3	SPASC	change in SPAS

The upper 4 bits of the Interrupt Status 2 register are available to the processor as status bits. Thus, if one of the bits 1-3 generates an interrupt indicating a state change has taken place, the corresponding status bit (bits 5-7) may be read to determine what the new state is. To determine the nature of a change in addressed status (bit 0) the Address Status Register is available to be read. And finally, bit 7 monitors the state of the 8291 INT pin. Logically, it is an OR of all unmasked interrupt status bits. One should note that bits 4-7 of the Interrupt Status 2 Register do not generate interrupts, but are available only to be read as status bits by the processor.

Bits 4 and 5 (DMAI, DMAO) of the Interrupt Mask 2 Register are available to enable direct data transfers between memory and the GPIB, DMAI (DMA in) enables the DMA REQ (DMA request) pin of the 8291 to be asserted upon the occurrence of BI. Similarly, DMAO (DMA out) enables the DMA REQ pin to be asserted upon the occurrence of BO. One might note that the DMA REQ pin may be used as a second interrupt output pin, monitoring BI and/or BO and masked by DMAI and DMAO. One should note that the DMA REQ pin is not affected by a read of the Interrupt Status 1 Register. It is reset whenever a byte is written to the Data Out Register or read from the Data in Register.

To ensure that an interrupt status bit will not be cleared without being read, and will not remain uncleared after being read, the 8291 implements a special interrupt

handling procedures. When an unmasked interrupt bit is set in either of the Interrupt Status Registers, the input of the registers are blocked until the set bit is read and reset by the microprocessor. Thus, potential problems arise when interrupt status changes while the register is being blocked. However, the 8291 stores all new interrupts in a temporary register and transfers them to the appropriate interrupt Status Register after the interrupt has been reset. In the Interrupt Status 1 Register and in ADSC bit, this transfer takes place only if the corresponding bits were read as zeroes. For the other status change bits in the Interrupt Status 2 Register, the transfer will always take place. However, even number of changes in these status bits during blocking time will cause no interrupt.

Serial Poll Registers

S8	SRQS	S6	S5	S4	S3	S2	S1

SERIAL POLL STATUS (3R)

S8	rsv	S6	S5	S4	S3	S2	S1

SERIAL POLL MODE (3W)

The Serial Poll Mode Register is used to establish the status byte that the 8291 sends out on the GPIB data lines when it receives the SPE (Serial Poll Enable) message. Bit 6 of this register is reserved for the rsv (request service) local message. Setting this bit to 1 causes the 8291 to assert its SRQ line, indicating its need for attention from the controller-in-charge of the GPIB. When service has been granted, the bit should be cleared by the microprocessor. The other bits of this register are available for sending status information over the GPIB. Sometime after the microprocessor initiates a request for service by setting bit 6, the controller of the GPIB sends the SPE message and then addresses the 8291 to talk. At this point, one byte of status is returned by the 8291 via the Serial Poll Mode Register.

The Serial Poll Status Register is available for reading the status byte in the Serial Poll Mode Register. The processor may check the status of a request for service by polling bit 6 of this register, which corresponds to SRQS (Service Request State). When a Serial Poll is conducted and the controller-in-charge reads the status byte, the SRQS bit is cleared. The SRQ line is tied to this bit, so that a request for service is terminated when the 8291's status byte is read. The rsv bit of the Serial Poll Mode Register must then be cleared by the microprocessor.

Address Registers

ton	lon	EOI	LPAS	TPAS	LA	TA	MJMN

ADDRESS STATUS (4R)

X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0

ADDRESS 0 (6R)

X	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1

ADDRESS 1 (7R)

TO	LO	0	0	0	0	ADM1	ADM0

ADDRESS MODE (4W)

ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

ADDRESS 0/1 (6W)

The Address Mode Register is used to select one of the five modes of addressing available on the 8291. It determines the way in which the 8291 uses the information in the Address 0 and Address 1 registers:

—In Mode 1, the contents of the Address 0 Register constitute the "Major" talker/listener address while the Address 1 Register represents the "Minor" talker/listener address. In applications where only one address is needed, the major talker/listener is used, and the minor talker/listener should be disabled. Loading an addres via the Address 0/1 Register into Address Registers 0 and 1 enables the major and minor talker/listener functions respectively.

—In Mode 2 the 8291 recognizes two sequential address bytes: a primary followed by a secondary. Both address bytes must be received in order to enable the device to talk or listen. In this manner, Mode 2 addressing implements the extended talker and listener functions as defined in IEEE 488.

To use Mode 2 addressing the primary address must be loaded into the Address 0 Register, and the Secondary address is placed in the Address 1 Register. With both primary and secondary addresses residing on chip, the 8291 can handle all addressing sequences without processor intervention.

—In Mode 3, the 8291 handles addressing just as it does in Mode 1, except that each Major or Minor primary address must be followed by a secondary address. All secondary addresses must be verified by the microprocessor when Mode 3 is used. When the 8291 is in TPAS or LPAS (talker/listener primary addresses state), and it does not recognize the byte on the DIO lines, an APT interrupt is generated (see section on Interrupt Registers) and the byte is available in the CPT (Command Pass-Through) Register. As part of its interrupt service routine, the microprocessor must read the CPT Register and write one of the following responses to the Auxiliary Mode Register:

1. 07H implies a non-valid secondary address
2. 0FH implies a valid secondary address

Setting the "ton" bit generates the local ton (talk-only) message and sets the 8291 to a talk-only mode. This mode allows the device to operate as a talker in an interface system without a controller.

Setting the "lon" bit generates the local lon (listen-only) message and sets the 8291 to a listen-only mode. This mode allows the device to operate as a listener in an interface system without a controller.

The mode of addressing implemented by the 8291 may be selected by writing one of the following bytes to the Address Mode Register:

Register Contents	Mode
10000000	Enable talk only mode (ton)
01000000	Enable listen only mode (lon)
11000000	The 8291 may talk to itself
00000001	Mode 1, (Primary-Primary)
00000010	Mode 2 (Primary-Secondary)
00000011	Mode 3 (Primary/APT-Primary/APT)

The Address Status Register contains information used by the microprocessor to handle its own addressing. This information includes status bits that monitor the address state of each talker/listener, "ton" and "lon" flags which indicate the talk only and listen only states, and an EOI bit which, when set, signifies that the END message came with the last data byte. LPAS and TPAS indicate that the listener or talker primary address has been received. The microprocessor can then use these bits when the secondary address is passed through to determine whether the 8291 is addressed to talk or listen. The LA (listener addressed) bit will be set when the 8291 is in LACS (Listener Active State) or in LADS (Listener Addressed State). Similarly, the TA (Talker Addressed bit will be set to indicate TACS or TADS, but also to indicate SPAS (Serial Poll Active State). The MJMN bit is used to determine whether the information in the other bits applies to the Major or Minor talker/listener. It is set to "1" when the Minor talker/listener is addressed. It should be noted that only one talker/listener may be active at any one time. Thus, the MJMN bit will indicate which, if either, of the talker/listeners is addressed or active.

The Address 0/1 Register is used for specifying the device's addresses according to the format selected in the Address Mode Register. Five bit addresses may be loaded into the Address 0 and Address 1 registers by writing into the Address 0/1 Register. The ARS bit is used to select which of these registers the other seven bits will be loaded into. The DT and DL bits may be used to disable the talker or listener function at the address signified by the other five bits. When Mode 1 addressing is used and only one primary address is desired, both the talker and the listener should be disabled at the Minor address.

As an example of how the Address 0/1 Register might be used, consider an example where two primary addresses are needed in the device. The Major primary address will be selectable only as a talker and the Minor primary address will be selectable only as a listener. This configuration of the 8291 is formed by the following sequence of writes by the microprocessor:

Operation	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	Data	RS2-RS0
1. Select addressing Mode 1	0	1	0	00000001	100
2. Load major address into Address 0 Register with listener function disabled.	0	1	0	001AAAAA	110
3. Load minor address into Address 1 Register with talker function disabled.	0	1	0	110BBBBB	110

At this point, the addresses AAAAA and BBBBB are stored in the Address 0 and Address 1 registers respectively, and are available to be read by the microprocessor. Thus, it is not necessary to store any address information elsewhere. Also, with the information stored in the Address 0 and Address 1 registers, processor intervention is not required to recognize addressing by the controller. Only in Mode 3, where secondary addresses are passed through, must the processor intervene in the addressing sequence.

Command Pass Through Register

CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

COMMAND PASS THROUGH (5R)

The Command Pass Through Register is used to transfer undefined 8-bit remote message codes from the GPIB to the microprocessor. When the CPT feature is enabled (bit B0 in Auxiliary Register B), any message not decoded by the 8291 becomes an undefined command. When Mode 3 addressing is used secondary addresses are also passed through the CPT Register. In either case, the 8291 will holdoff the handshake until the microprocessor reads this register and issues the VSCMD auxiliary command.

The CPT and APT interrupts flag the availability of undefined commands and secondary addresses in the CPT Register. The details of these interrupts are explained in the section on Interrupt Registers.

An added feature of the 8291 is its ability to handle undefined secondary commands following undefined primaries. Thus, the number of available commands for user definition or future IEEE 488 definition is significantly increased; one undefined primary command followed by a sequence of as many as 32 secondary commands can be processed. However, it is recommended that users do not define their own commands since such definition would violate IEEE 488.

The recommended use of the 8291's undefined command capabilities is for a controller-configured Parallel Poll. The PPC message is an undefined primary command typically followed by PPE, an undefined secondary command. For details on this procedure, refer to the section on Parallel Poll Protocol.

Auxiliary Mode Register

CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0

AUX MODE (5W)

CNT0—2:CONTROL BITS
COM0—:COMMAND BITS

The Auxiliary Mode Register contains a three-bit control field and a five-bit command field. It is used for several purposes on the 8291:

1. To load "hidden" auxiliary registers on the 8291.
2. To issue commands from the microprocessor to the 8291.
3. To preset an internal counter used to generate T1, delay in the Source Handshake function, as defined in IEEE 488.

Table 4 summarizes how these tasks are performed with the Auxiliary Mode Register. Note that the three control bits determine how the five command bits are interpreted.

TABLE 4

CODE		COMMAND
CONTROL BITS	COMMAND BITS	
000	0CCCC	Execute auxiliary command CCCC
001	0FFFF	Preset internal counter to match external clock frequency of FFFF MHZ (FFFF - binary representation of 1 to 8 MHz)
100	DDDDD	Write DDDDD into auxiliary register A
101	0DDDD	Write DDDD into auxiliary register B
011	USP$_3$P$_2$P$_1$	Configure/unconfigure parallel poll SP$_3$P$_2$P$_1$ as defined in Std. 488. (Configure if U = 0, Unconfigure if U = 1). This command is the local poll enable (lpe) message when U = 0.

AUXILIARY COMMANDS

Auxiliary commands are executed by the 8291 whenever 0000CCCC is written into the Auxiliary Mode Register, where CCCC is the 4-bit command code.

4-Bit Code	Description
0000	Immediate Execute pon — This command resets the 8291 to a power up state (local pon message as defined in IEEE 488). The following conditions constitute the power up state: 1. All talkers and listeners are disabled. 2. No interrupt status bits are set. The 8291 is designed to power up in certain states as specified in the IEEE 488 state diagrams. Thus, the following states are in effect in the power up state: SIDS, AIDS, TIDS, LIDS, NPRS, LOCS, and PPIS. The "0000" pon is an immediate execute command (a pon pulse). It is also used to release the "initialize" state generated by either an external reset pulse or the "0010" Chip Reset command.
0010	Chip Reset (Initialize) — This command has the same effect as a pulse applied to the Reset pin. (Refer to the section on Reset Procedure.)
0011	Finish Handshake — This command finishes a handshake that was stopped because of a holdoff on RFD or DAV. (Refer to Auxiliary Register A.)
0100	Trigger — A "Group Execute Trigger" is forced by this command. It has the same effect as a GET command issued by the controller-in-charge of the GPIB, but does not cause a GET interrupt.
0101	rtl[1] — This command corresponds to the local rtl message as defined in IEEE 488. The 8291 will go to a local state if local lockout is not in effect.
0110	Send EOI — The EOI line of the 8291 may be asserted with this command. The command causes EOI to go true with the next byte transmitted. The EOI line is then cleared upon completion of the handshake for that byte.
0111, 1111	Non-Valid/Valid Secondary Address or Command (VSCMD) — This command informs the 8291 that the secondary address received by the microprocessor was valid or invalid (0111 → invalid, 1111 → valid). If Mode 3 addressing is used, the processor must field each extended address and respond to it, or the GPIB will hang up. Note that the COM3 bit is the invalid/valid flag. The valid (1111) command is also used to tell the 8291 to continue from the command-pass-through state (immediate execute command).
0001, 1001	Parallel Poll Flag (local "ist" message) — This command sets (1001) or clears (0001) the parallel poll flag. A "1" is sent over the assigned data line (PPR-Parallel Poll Response true) only if the parallel poll flag matches the sense bit from the lpe local message (or indirectly from the PPE message). For a more complete description of the Parallel Poll features and procedures refer to the section on Parallel Poll Protocol.

1. Subsequently the 8291 will include "set rtl" and "clear rtl" commands.

INTERNAL COUNTER

The internal counter determines the delay time allowed for the settling of data on the DIO lines. This delay time is defined as T_1 in IEEE 488 and appears in the Source Handshake state diagram between SDYS and STRS. As such, DAV is asserted T_1 *after* the DIO lines are driven. Consequently, T_1 is a major factor in determining the data transfer rate of the 8291 over the GPIB (T_1 = TWROV2-TWROI5).

When open-collector transceivers are used for connection to the GPIB, T_1 is defined by IEEE 488 to be 2μsec. By writing 0010FFFF into the Auxiliary Mode Register, the counter is preset to match a f_C MHz clock input, where FFFF is the binary representation of N_F ($1 \leq N_F \leq 8$, $N_F = (FFFF)_2$). When $N_F = f_C$, a 2μsec T_1 delay will be generated before each DAV asserted.

$$T_{1(\mu sec)} = \frac{2N_F}{f_C} + t_{SYNC}\ ,\ 1 \leqslant N_F \leqslant 8$$

t_{SYNC} is a synchronization error, greater than zero and smaller than the larger of T clock high and T clock low. (For a 50% duty cycle clock, t_{SYNC} is less than half the clock cycle).

If it is necessary that T_1 be different from 2μsec, N_F may be set to a value other than f_C. In this manner, data transfer rates may be programmed for a given system. In small systems, for example, where transfer rates exceeding GPIB specifications are required, one may set $N_F < f_C$ and decrease T_1.

When tri-state transceivers are used, IEEE 488 allows a higher transfer rate (lower T_1). Use of the 8291 with such transceivers is enabled by setting B2 in Auxiliary Register B.In this case, setting $N_F = f_C$ causes a T_1 delay of 2μsec to be generated for the first byte transmitted — all subsequent bytes will have a delay of 500 nsec.

$$T_1(\text{High Speed})\ \mu sec = \frac{N_F}{2f_C} + t_{SYNC}$$

Thus, setting $N_F = 1$ using a 4 MHz clock will generate for a 50% duty cycle clock (t_{SYNC}<125 nsec.):

$$T_1 = \frac{1}{2.4} + 0.125 = 0.250\ \mu sec = 250\ nsec$$

AUXILIARY REGISTER A

Auxiliary Register A is a "hidden" 5-bit register which is used to enable some of the 8291 features. Whenever a 100 $A_4A_3A_2A_1A_0$ byte is written into the Auxiliary Register, it is loaded with the data $A_4A_3A_2A_1A_0$. Setting the respective bits to "1" enables the following features:

A_0 — RFD/DAV Holdoff on all Data: If the 8291 is listening, RFD will not be sent true until the "finish handshake" auxiliary command is issued by the microprocessor. If the 8291 is talking, DAV is not sent true until the "finish handshake" command is given. In both cases, the holdoff will be in effect for each data byte.

A_1 — RFD/DAV Holdoff on End: This feature enables the holdoff on EOI or EOS (if enabled). However, no holdoff will be in effect on any other data bytes.

A_2 — End on EOS Received: Whenever the byte in the Data In Register matches the byte in the EOS Register, the End interrupt bit will be set in the Interrupt Status 1 Register.

A_3 — Output EOI on EOS Sent: Any occurrence of data in the Data Out Register matching the EOS Register causes the EOI line to be sent true along with the data.

A_4 — EOS Binary Compare: Setting this bit causes the EOS Register to function as a full 8-bit word. When it is not set, the EOS Register is a 7-bit word (for ASCII characters).

If $A_0 = A_1 = 1$, a special "continuous Acceptor Handshake cycling" mode is enabled. This mode should be used only in a controller system configuration, where both the 8291 and the 8292 are used. It provides a continuous cycling through the Acceptor Handshake state diagram, requiring no local messages from the microprocessor; the rdy local message is automatically generated when in ANRS. As such, the 8291 Acceptor Handshake serves as the controller Acceptor Handshake. Thus, the controller cycles through the Acceptor Handshake without delaying the data transfer in progress. When the t_{CS} local message is executed, the 8291 is taken out of the "continuous AH cycling" mode, the GPIB hangs up in ANRS, and a BI interrupt is generated to indicate that control may be taken. A simpler procedure may be used when a "t_{CS} on end of block" is executed; the 8291 may stay in "continuous AH cycling". Upon the end of a block (EOI or EOS received), a holdoff is generated, the GPIB hangs up in ANRS, and control may be taken.

AUXILIARY REGISTER B

Auxiliary Register B is a "hidden" 4-bit register which is used to enable some of the features of the 8291. Whenever a 1010$B_3B_2B_1B_0$ is written into the Auxiliary Mode Register, it is loaded with the data $B_3B_2B_1B_0$. Setting the respective bits to "1" enables the following features:

B_0 — Enable Undefined Command Pass Through: This feature allows any commands not recognized by the 8291 to be handled in software. If enabled, this feature will cause the 8291 to holdoff the handshake when an undefined command is received. The microprocessor must then read the command from the Command Pass Through Register and send the VSCMD auxiliary command. Until the VSCMD command is sent, the handshake holdoff will be in effect.

B_1 — Send EOI in SPAS: This bit enables EOI to be sent with the status byte; EOI is sent true in Serial Poll Active State. Otherwise, EOI is sent false in SPAS.

B_2 — Enable High Speed Data Transfer: This feature may be enabled when tri-state external transceivers are used. The data transfer rate is limited by T_1 (delay time generated in the Source Handshake function), which is defined according to the type of transceivers used. When the "High Speed" feature is enabled, T_1 = 2 microseconds is generated for the first byte transmitted after each true to false transition of ATN. For all subsequent bytes, T_1 = 500 nanoseconds. Refer to the Internal Counter section for an explanation of T_1 duration as a function of B_2 and of clock frequency.

B_3 — Enable Active Low Interrupt: Setting this bit causes the polarity of the INT pin to be reversed, providing an output signal compatible with Intel's MCS-48™. Interrupt registers are not affected by this bit.

PARALLEL POLL PROTOCOL

Writing a 011USP$_3$P$_2$P$_1$ into the Auxiliary Mode Register will configure (U=0) or unconfigure (U=1) the 8291 for a parallel poll. When U=0, this command is the "lpe" (local poll enable) local message as defined in IEEE 488. The "S" bit is the sense in which the 8291 is configured; only if the Parallel Poll Flag ("ist" local message) matches this bit will the Parallel Poll Response, PPR$_N$, be sent true. The bits P$_3$P$_2$P$_1$ specify which of the eight data lines PPR$_N$ will be sent over. Thus, once the 8291 has been configured for Parallel Poll, whenever it senses both EOI and ATN true, it will automatically compare its PP flag with the sense bit and send PPR$_N$ true or false according to the comparison.

If a PP$_2$* implementation is desired, the "lpe" and "ist" local messages are all that are needed. Typically, the user will configure the 8291 for Parallel Poll immediately after initialization. During normal operation the microprocessor will set or clear the Parallel Poll Flag (ist) according to the device's need for service. Consequently the 8291 will be set up to give the proper response to IDY (EOI • ATN) without directly involving the microprocessor.

If a PP1* implementation is desired, the undefined command features of the 8291 must be used. In PP1, the 8291 is indirectly configured for Parallel Poll by the active controller on the GPIB. The sequence at the 8291 being configured is as follows:

1. The PPC message is received true. Being an undefined command, it is loaded into the Command Pass Through Register, and a CPT interrupt is sent to the microprocessor. The handshake is automatically held off.

2. The microprocessor reads the CPT Register and sends VSCMD to the 8291, releasing the handshake.

3. Having received an undefined primary command, the 8291 is set up to receive an undefined secondary command, the PPE message. This message is also received into the CPT Register, the handshake is held off, and the CPT interrupt is generated.

4. The microprocessor reads the PPE message and decodes the SP$_3$P$_2$P$_1$ information. It then sends the appropriate "lpe" local message to the 8291. Finally, the microprocessor sends VSCMD and the handshake is released.

*As defined in IEEE Standard 488.

End of Sequence (EOS) Register

EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

EOS REGISTER

The EOS Register and its features offer an alternative to the "Send EOI" auxiliary command. A seven or eight bit byte (ASCII or binary) may be placed in the register to flag the end of a block or read. The type of EOS byte to be used is selected in Auxiliary Register bit A$_4$.

If the 8291 is a listener, and the "End on EOS Received" is enabled at bit A$_2$, then an End interrupt is generated in the Interrupt Status 1 Register whenever the byte in the Data-In Register matches the byte in the EOS Register.

If the 8291 is a talker, and the "Output EOI on EOS Sent" is enabled at bit A$_3$, then the EOI line is sent true with the next data byte whenever the contents of the Data Out Register match the EOS register.

Reset Procedure

The 8291 is reset to an initialization state either by a pulse applied to its Reset pin, or by a reset auxiliary command (02H written into the Auxiliary Command Register). The following conditions are caused by a reset pulse (or local reset command):

1. A "pon" local message as defined by IEEE 488 is held true until the initialization state is released.
2. The Interrupt Status Registers are cleared.
3. Auxiliary Registers A and B are cleared.
4. The Serial Poll Mode Register is cleared.
5. The Parallel Poll Flag is cleared.
6. The EOI bit in the Address Status Register is cleared.
7. N_F in the Internal Counter is set to 8 MHz. This setting causes the longest possible t_1 delay to be generated in the Source Handshake (16 μsec for 1 MHz clock).

The initiallization state is released by an "immediate execute pon" command (00H written into the Auxiliary Command Register).

The suggested initialization sequence is:

1. Apply a reset pulse or send the reset auxiliary command.
2. Set the desired initial conditions by writing into the Interrupt Mask, Serial Poll Mode, Address Mode, Address 0/1, and EOS Registers. Auxiliary Registers A and B, and the internal counter should also be initialized.
3. Send the "immediate execute pon" auxiliary command to release the initialization state.
4. If a PP$_2$ Parallel Poll implementation is to be used the "lpe" local message may be sent, configuring the 8291 for a Parallel Poll Response on an assigned line. (Refer to the section on Parallel Poll Protocol.)

Using DMA

The 8291 may be connected to the Intel 8257 DMA Controller for DMA operation. The DMA REQ pin of the 8291 requests a DMA byte transfer from the 8257. It is set by BO or BI flip flops, masked by the DMAO and DMAI bits in the Interrupt Mask 2 Register. (After reading, the INT1 register BO and BI interrupts will be cleared but not BO and BI in DREQ equation.)

The $\overline{\text{DMA ACK}}$ pin is driven by the 8257 in response to the DMA request. When $\overline{\text{DMA ACK}}$ is true (active low) it sets CS = RS0 = RS1 = RS2 = 0 such that the RD and WR signals sent by the 8257 refer to the Data In and Data Out Registers. Also, the DMA request line is reset by $\overline{\text{DMA ACK}}$.

DMA input sequence:

1. A data byte is accepted from the GPIB by the 8291.
2. A BI interrupt is generated and DMA REQ is set.
3. $\overline{\text{DMA ACK}}$ is asserted by the 8257 and DMA REQ is reset.
4. $\overline{\text{RD}}$ is driven by the 8257 and the contents of the Data In Register are transferred to MCS bus.
5. The 8291 sends RFD true on the GPIB and proceeds with the Acceptor Handshake protocol.

DMA output sequence:

1. A BO interrupt is generated (indicating that the Data Out Register is empty) and DMA REQ is asserted.
2. $\overline{\text{DMA ACK}}$ is asserted by the 8257 and DMA REQ is reset.
3. $\overline{\text{WR}}$ is driven by the 8257 and a byte is transferred from the MCS bus into the Data Out Register.
4. The 8291 sends DAV true on the GPIB and proceeds with the Source Handshake protocol.

It should be noted that each time the device is addressed, the Address Status Register should be read, and the 8257 should be initialized accordingly. (Refer to the 8257 data sheet available in Intel's Peripheral Design Handbook.)

System Configuration

Microprocessor Bus Connection

The 8291 is 8080, 8048, 8085 and 8086 compatible. The three address pins (RS_0, RS_1, RS_2) should be connected to the non-multiplexed address bus (for example: A_8, A_9, A_{10}). In case of 8080, any address lines may be used.

External Transceivers Connection

8291 IEEE bus pins are TTL compatible. For IEEE Std. bus connection, external transceivers are required. 8291 supplies Transmit/Receive control pins: T/R1 controls DIO_{1-8}, NRFD, NADC and DAV transceivers, T/R2 controls EOI transceiver. IFC, ATN, REN are always inputs and SRQ is always an output.

Logically, TR1 = TACS + SPAS + PPAS;
TR2 = TACS + SPAS.

Refer to 8292 Data Sheet for 8291/8292 system configuration.

DEVICE ELECTRICAL CHARACTERISTICS

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5V ± 10%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL}=2mA (4mA for TR1 pin)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA (-150μA for SRQ pin)
V_{OH-INT}	Interrupt Output High Voltage	2.4		V	I_{OH}=-400μA
		3.5		V	I_{OH}=-50μA
I_{IL}	Input Leakage		10	μA	V_{IN}=0V to V_{CC}
I_{LOL}	Output Leakage Current		-10	μA	V_{OUT}=0.45V
I_{LOH}	Output Leakage Current		10	μA	V_{OUT}=V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	T_A=0°C

A.C. CHARACTERISTICS

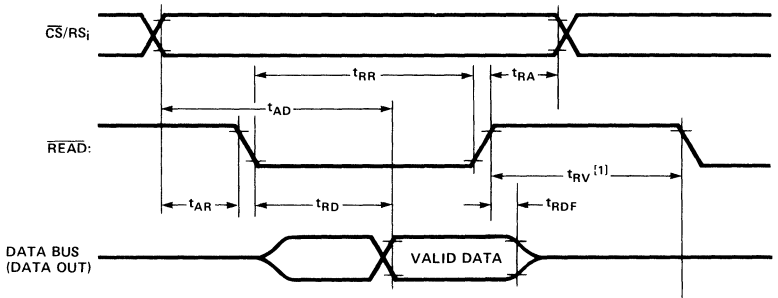
V_{CC} = 5V ± 10%, Commercial: T_A = 0°C to 70°C

Symbol	Parameter	Min.	Max.	Unit
t_{AR}	Address Stable Before $\overline{READ}$	0		nsec[1]
t_{RA}	Address Hold After $\overline{READ}$	0		nsec[1]
t_{RR}	$\overline{READ}$ width	250		nsec[2]
t_{AD}	Address Stable to Data Valid		250	nsec[1]
t_{RD}	$\overline{READ}$ to Data Valid		100	nsec[2]
t_{RDF}	Data Float After $\overline{READ}$	0	60[2]	nsec
t_{AW}	Address Stable Before $\overline{WRITE}$	0		nsec[1]
t_{WA}	Address Hold After $\overline{WRITE}$	0		
t_{WW}	$\overline{WRITE}$ Width	250		nsec[1]
t_{DW}	Data Set Up Time to the Trailing Edge of $\overline{WRITE}$	150		nsec[1]
t_{WD}	Data Hold Time After $\overline{WRITE}$	0		nsec[1]
t_{AKRQ}	$\overline{DACK}$↓ to DREQ↓		130	nsec
t_{DKDA6}	$\overline{DACK}$↓ to Up Data Valid		200	nsec

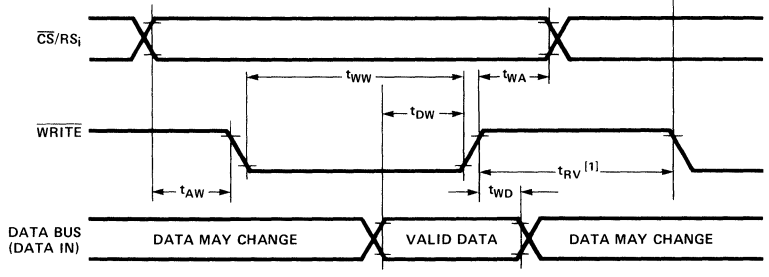
Notes:
1. 8080 System C_{Lmax} = 100pF; C_{Lmin} = 15pF; 3 MHz clock.
2. 8085 System C_L = 150pF; 4 MHz clock.

TIMING WAVEFORMS

READ

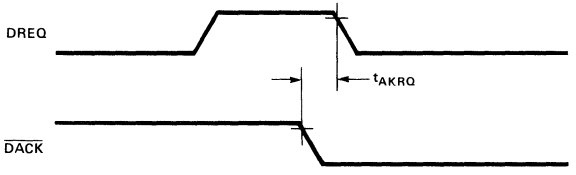


WRITE



NOTES: 1. t_{RV} IS THE TIME BETWEEN READ OR WRITE OPERATIONS WITH THE CHIP SELECTED (CHIP RECOVERY TIME).

DMA



GPIB TIMINGS[1]

Symbol	Parameter	Max.	Unit	Test Conditions
TEOT13	$\overline{EOI}\downarrow$ to TR1$\uparrow$	90	nsec	PPSS, $\overline{ATN}$=0.45V
TEODI6	$\overline{EOI}\downarrow$ to $\overline{DIO}$ Valid	130	nsec	PPSS, $\overline{ATN}$=0.45V
TEOT12	$\overline{EOI}\downarrow$ to TR1$\downarrow$	130	nsec	PPSS, $\overline{ATN}$=0.45V
TATND4	$\overline{ATN}\downarrow$ to $\overline{NDAC}\downarrow$	130	nsec	TACS, AIDS
TATT14	$\overline{ATN}\downarrow$ to TR1$\downarrow$	130	nsec	TACS, AIDS
TATT24	$\overline{ATN}\downarrow$ to TR2$\downarrow$	130	nsec	TACS, AIDS
TDNVD3-C	$\overline{DAV}\downarrow$ to $\overline{NDAC}\uparrow$	350	nsec	AH, CACS
TNDDV1	$\overline{NDAC}\uparrow$ to $\overline{DAV}\uparrow$	300	nsec	SH, STRS
TNRDV2	$\overline{NRFD}\uparrow$ to $\overline{DAV}\downarrow$	300	nsec	SH, T1 True
TNDDR1	$\overline{NDAC}\uparrow$ to DREQ$\uparrow$	350	nsec	SH
TDVDR3	$\overline{DAV}\downarrow$ to DREQ$\uparrow$	350	nsec	AH, LACS, $\overline{ATN}$=2.4V
TDVND2-C	$\overline{DAV}\uparrow$ to $\overline{NDAC}\downarrow$	350	nsec	AH,LACS
TDVNR1-C	$\overline{DAV}\uparrow$ to $\overline{NRFD}\uparrow$	350	nsec	AH, LACS, rdy=True
TRDNR3	$\overline{RD}\downarrow$ to $\overline{NRFD}\uparrow$	500	nsec	AH, LACS
TWRDI5	$\overline{WR}$ to $\overline{DIO}$ Valid	200	nsec	SH, TACS, RS = 0.4V
TWRDV2	$\overline{WR}\uparrow$ to $\overline{DAV}\downarrow$	760	nsec	$\overline{NRFD}$ = 2.4V, RS = 0.4V, SH, TACS, High Speed Transfers Enabled, $N_F = f_C = 8$ MHz

Notes:
1. All GPIB timings are at the pins of the 8291.

Appendix A

MODIFIED STATE DIAGRAMS

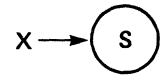
Figure A.1 presents the interface function state diagrams. It is derived from IEEE Std. state diagrams, with the following changes:

A. Controller function omitted.
B. Addressing modes included in T,L state diagrams.

Note that in Mode 3, MSA, OSA are generated only after secondary address validity check by the microprocessor (APT interrupt).

C. All remote messages sent true in each state are indicated.
D. All remote multiline messages decoded are conditioned by ACDS. The multiplication by ACDS is not drawn to simplify the diagrams.

E. The symbol



indicates:

1. When event X occurs, the function will return to state S.
2. X overrides any other transition condition in the function.

Statement 2 simplifies the diagram, avoiding the explicit use of $\overline{X}$ to condition all transitions from S to other states.

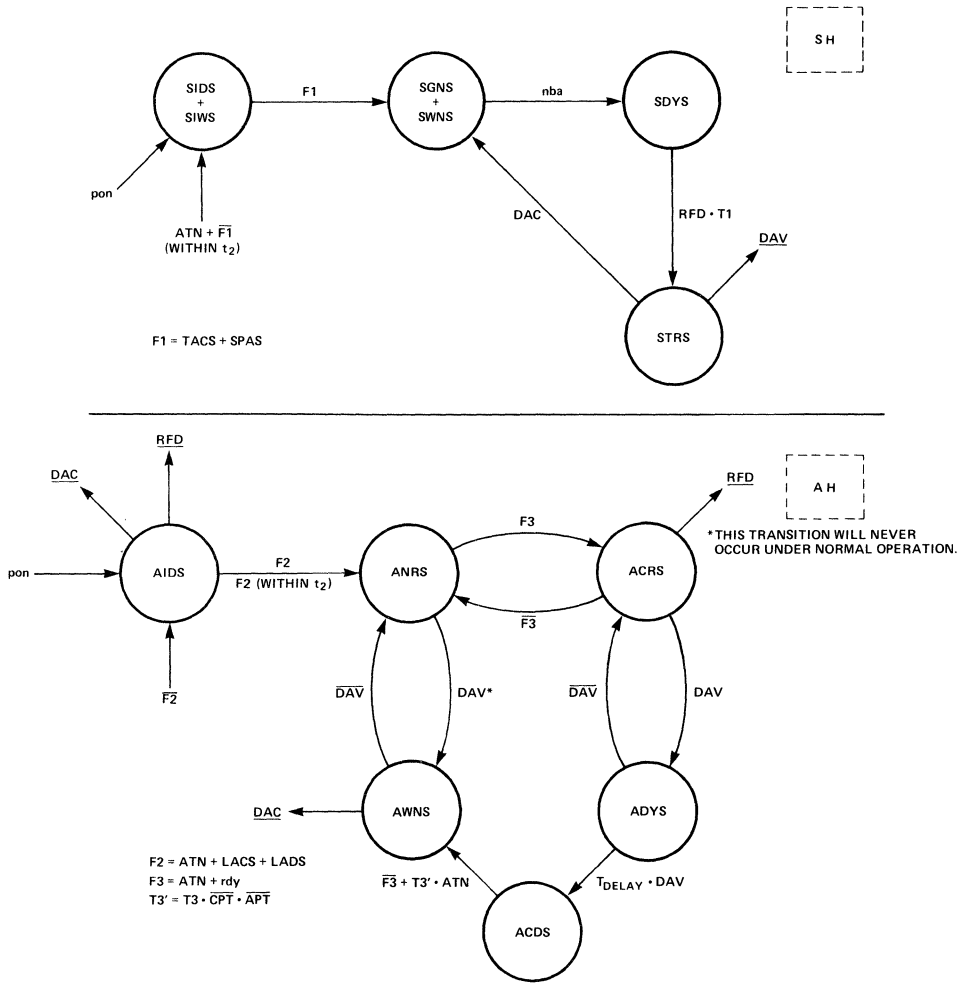


Figure A.1. 8291 State Diagrams (Continued next page)

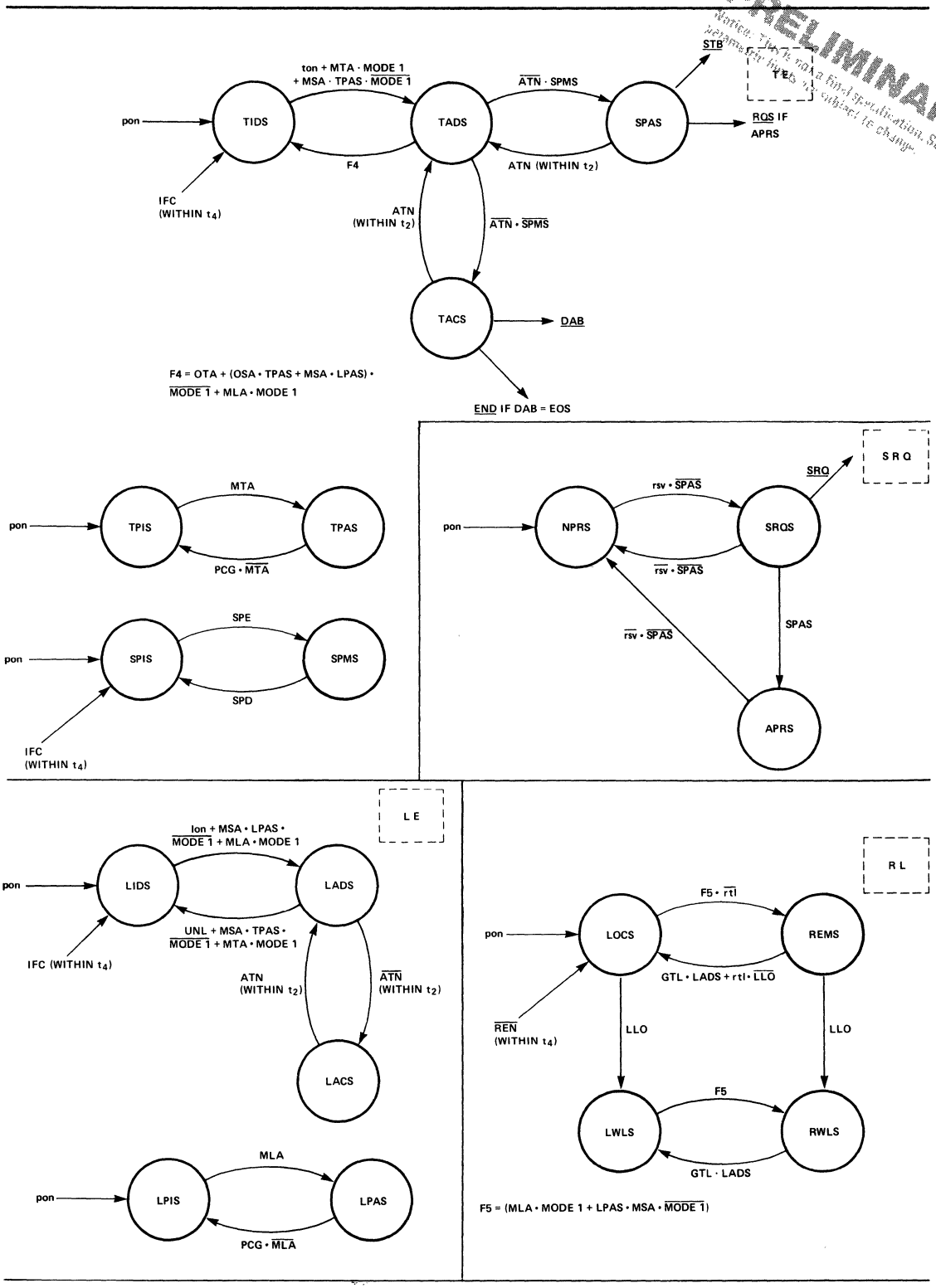


Figure A.1. 8291 State Diagrams (Continued next page)

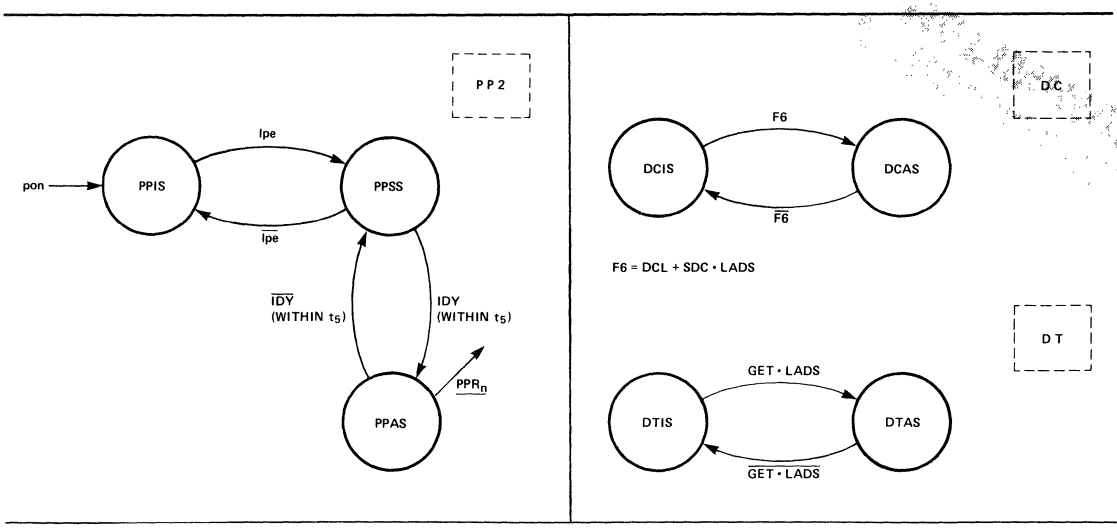


Figure A.1. 8291 State Diagrams

Appendix B

IEEE 488 TIME VALUES

Time Value Identifier*	Function (Applies to)	Description	Value
T_1	SH	Settling Time for Multiline Messages	$\geq 2\mu s$†
t_2	LC,$\overline{IC}$,SH,AH,T,L	Response to ATN	$\leq$ 200ns
T_3	AH	Interface Message Accept Time ‡	$> 0\ \delta$
t_4	T,TE,L,LE,C,CE	Response to IFC or REN False	$< 100\mu s$
t_5	PP	Response to ATN+EOI	$\leq$ 200ns
T_6	C	Parallel Poll Execution Time	$\geq 2\mu s$
T_7	C	Controller Delay to Allow Current Talker to see ATN Message	$\geq$ 500ns
T_8	C	Length of IFC or REN False	$> 100\mu s$
T_9	C	Delay for EOI**	$\geq 1.5\mu s$††

* Time values specified by a lower case t indicate the maximum time allowed to make a state transition. Time values specified by an upper case T indicate the minimum time that a function must remain in a state before exiting.

† If three-state drivers are used on the DIO, DAV, and EOI lines, T_1 may be:
1. $\geq$ 1100ns
2. Or $\geq$ 700ns if it is known that within the controller ATN is driven by a three-state driver.
3. Or $\geq$ 500ns for all subsequent bytes following the first sent after each false transition of ATN (the first byte must be sent in accordance with (1) or (2).
4. Or $\geq$ 350ns for all subsequent bytes following the first sent after each false transition of ATN under conditions specified in Section 5.2.3 and warning note. See IEEE Standard 488.

‡ Time required for interface functions to accept, not necessarily respond to interface messages.

δ Implementation independent.

** Delay required for EOI, NDAC, and NRFD signal lines to indicate valid states.

†† $\geq$ 600ns for three-state drivers.

Appendix C
THE THREE WIRE HANDSHAKE

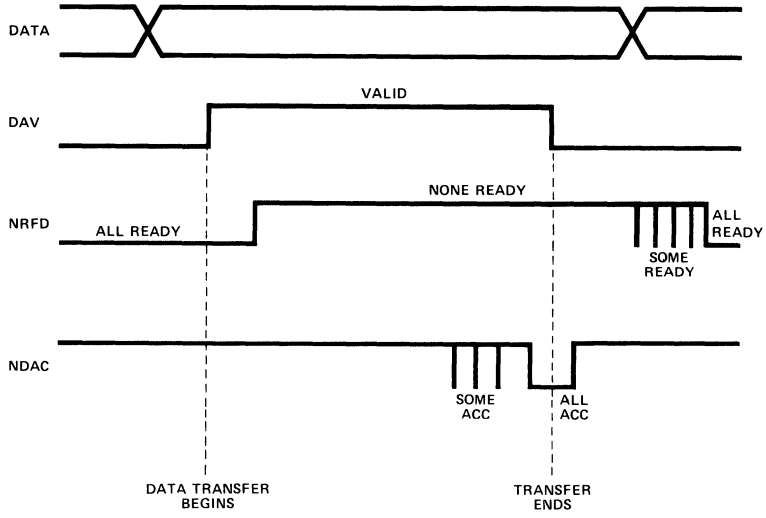
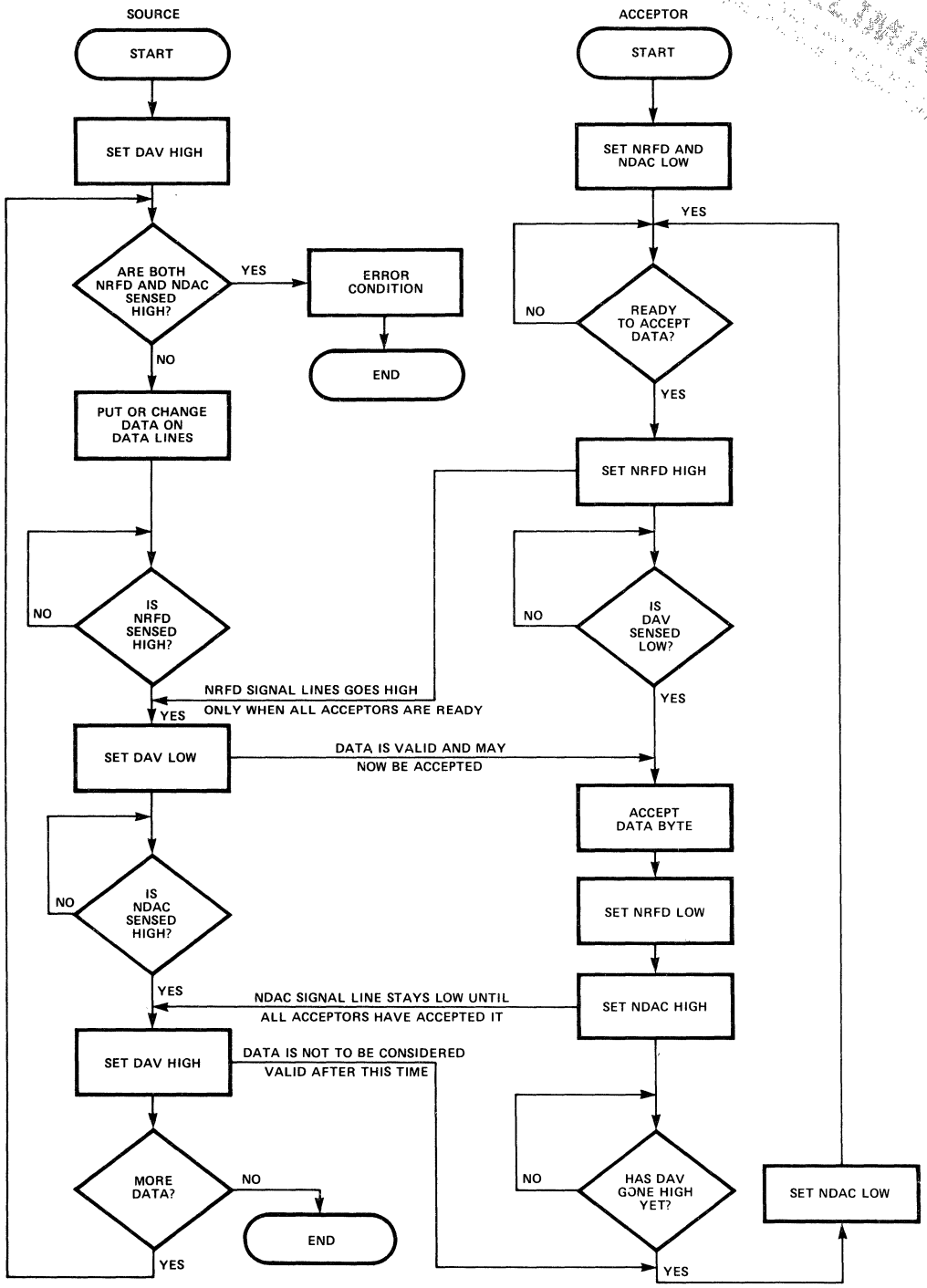


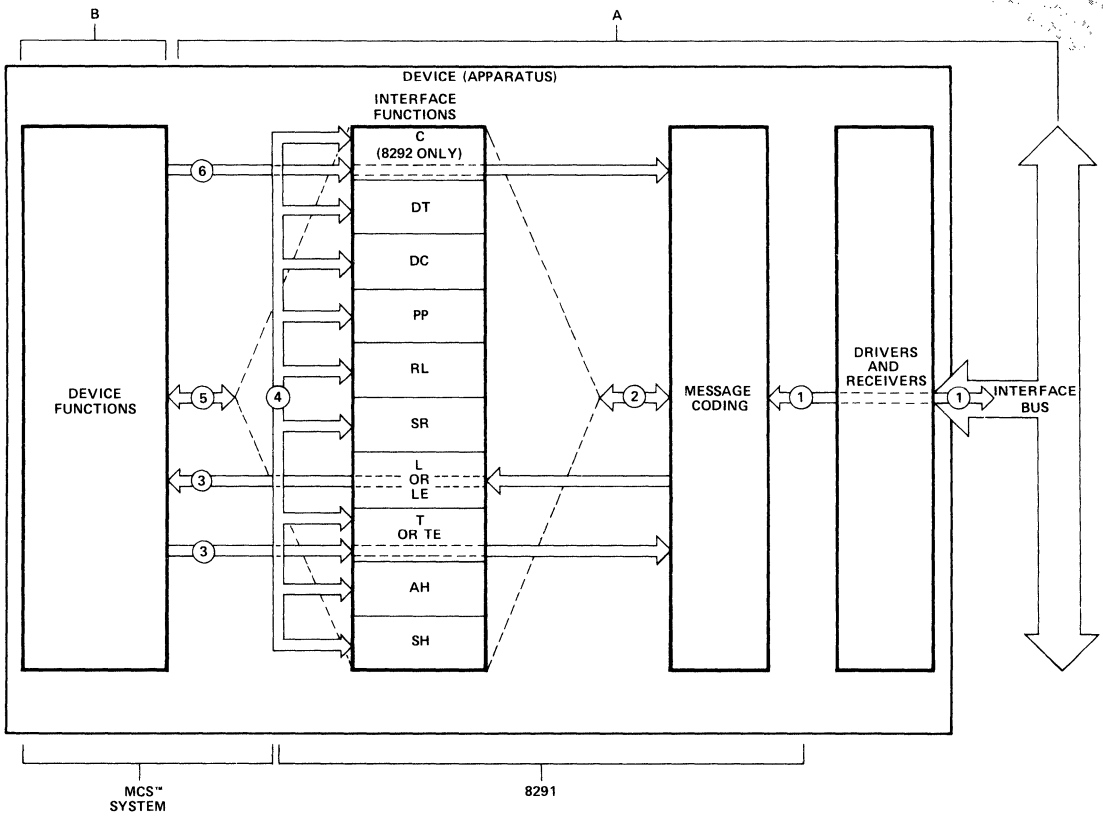
Figure C.1. 3-Wire Handshake Timing.



FLOW DIAGRAM OUTLINES SEQUENCE OF EVENTS DURING TRANSFER OF DATA BYTE. MORE THAN ONE LISTENER AT A TIME CAN ACCEPT DATA BECAUSE OF LOGICAL AND CONNECTION OF NRFD AND NDAC LINES.

Figure C.2. Handshake Flowchart.

Appendix D
FUNCTIONAL PARTITIONS



A – CAPABILITY DEFINED BY THE 488-1975 STANDARD.
B – CAPABILITY DEFINED BY THE DESIGNER.
1 – INTERFACE BUS SIGNAL LINES.
2 – REMOTE INTERFACE MESSAGES TO AND FROM INTERFACE FUNCTIONS.
3 – DEVICE DEPENDENT MESSAGES TO AND FROM DEVICE FUNCTIONS.
4 – STATE LINKAGES BETWEEN INTERFACE FUNCTIONS.
5 – LOCAL MESSAGES BETWEEN DEVICE FUNCTIONS AND INTERFACE FUNCTIONS (MESSAGES TO INTERFACE FUNCTIONS ARE DEFINED, MESSAGES FROM INTERFACE FUNCTIONS EXIST ACCORDING TO THE DESIGNER'S CHOICE).
6 – CONTROL MESSAGES (8292 ONLY).

Figure D.1. Functional Partition Within a Device.

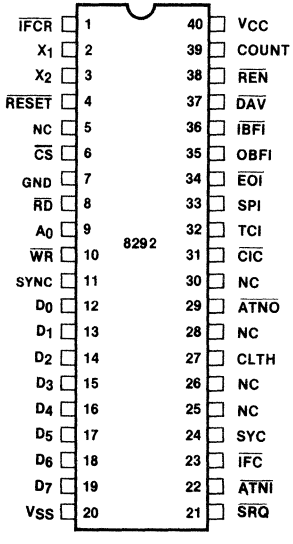
8292
GPIB CONTROLLER

FEATURES:

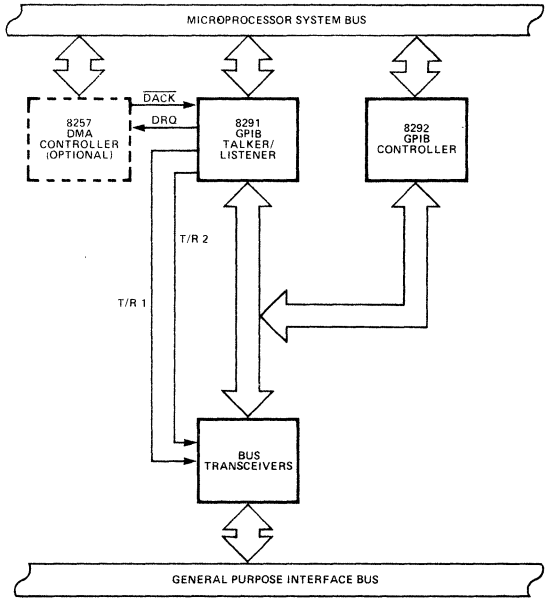
- **Complete IEEE Standard 488 Controller Function.**
- **Interface Clear (IFC) Sending Capability Allows for Seizure of Control and/or Initialization of the Bus.**
- **Responds to Service Requests (SRQ).**
- **Sends (REN), Allowing Instruments to Switch to Remote Control.**
- **Complete Implementation of Transfer Control Protocol.**
- **Synchronous Control Seizure Prevents the Destruction of any Data Transmission in Progress.**
- **Connects with the 8291 to Form a Complete IEEE Standard 488 Interface Talker/Listener/Controller.**

The 8292 GPIB CONTROLLER is a microprocessor-controlled chip designed to connect with the 8291 GPIB TALKER/LISTENER to implement the full IEEE Standard 488 controller function, including transfer control protocol. The 8292 is a pre-programmed UPI-41A.™

PIN CONFIGURATION



8291, 8292 SYSTEM DIAGRAM



MPU PERIPHERALS

PIN DESCRIPTION

Symbol	I/O	Pin No.	Function
D_0-D_7	I/O	12-19	8 bidirectional lines used for communication between the central processor and the 8292's data bus buffers and status register.
A_0	I	9	Address Line—Used to select between the data bus and the status register during read operations and to distinguish between data and commands written into the 8292 during write operations.
$\overline{CS}$	I	6	Chip Select Input—Used to select the 8292 from other devices on the common data bus.
$\overline{RD}$	I	8	I/O write input which allows the master CPU to write to the 8292.
$\overline{WR}$	I	10	I/O read input which allows the master CPU to read from the 8292.
$\overline{RESET}$	I	4	Used to initialize the chip to a known state during power on.
$\overline{DAV}$	I/O	37	DAV Handshake Line—Used only during parallel poll, configures to force the 8291 to accept the parallel poll status bits.
$\overline{ATNI}$	I	22	Attention In—Used by the 8292 to monitor the GPIB ATN control line. It is used during "take control synchronously" execution and during the transfer control procedure.
$\overline{CIC}$	O	31	Controller In Charge—Controls the S/R input of the SRQ bus transceiver. It can also be used to indicate that the 8292 is in charge of the bus.
$\overline{EOI}$	I/O	34	End Or Identify—One of the GPIB management lines, as defined by IEEE Std. 488-1975. Used with ATN as Identify Message during parallel poll.
$\overline{IFC}$	I/O	23	Interface Clear—One of the GPIB management lines, as defined by IEEE Std. 488-1975, places all devices in a known quiescent state.
SYC	I	24	System Controller—Monitors the system controller switch.
OBFI	O	35	Output Buffer Full—Used as an interrupt to the central processor while the output buffer of the 8292 is full. The feature can be enabled and disabled by the interrupt mask register.
$\overline{IBFI}$	O	36	Input Buffer Not Full—Used to interrupt the central processor while the input buffer of the 8292 is empty. This feature is enabled and disabled by the interrupt mask register.
$\overline{ATNO}$	O	29	Attention Out—Controls the ATN control line of the bus through external logic for tcs (take control synchronously) purpose. (ATN is a GPIB control line, as defined by IEEE Std. 488-1975.)
$\overline{SRQ}$	I	21	Service Request—One of the IEEE control lines. Sampled by the 8292 when it is controller in charge, if true—SPI interrupt to the monitor will be generated.
$\overline{REN}$	O	38	The Remote Enable bus signal selects remote or local control of the device on the bus. A GPIB bus management line, as defined by IEEE Std. 488-1975.
TCI	O	32	Task Complete Interrupt—Interrupt to the control processor used to indicate that the task requested was completed by the 8292 and the information requested is ready in the data bus.
SPI	O	33	Special Interrupt—Used as an interrupt on events not initiated by the central processor.
CLTH	O	27	CLEAR LATCH Output—Used to clear the $\overline{IFCR}$ after recognized by the 8292. Usually low (except after hardware Reset), will be pulsed low when $\overline{IFCR}$ is recognized by the 8292.
$\overline{IFCR}$	I	1	IFC Received (latched)—The 8292 monitors the IFC Line (when not system controller) through this pin.
COUNT	I	39	Count Input—When enabled by the proper command the internal counter will count external events through this pin. High to low transition will increment the internal counter by one. The pin is sampled once per three internal instruction cycles (7.5 μsec when using 6 MHz XTAL). It can be used for byte counting when connected to NDAC line, or for block counting when connected to the EOI line.
X_1,X_2	I	2,3	Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
SYNC	O	11	8041A instruction cycle synchronization signal; it is an output clock with a frequency of XTAL ÷ 15.
V_{CC}	P.S.	40	+5V supply input.
V_{SS}	P.S.	7,20	Circuit ground potential.

8294
DATA ENCRYPTION UNIT

- **Certified by National Bureau of Standards**
- **80 Byte/Sec Data Conversion Rate**
- **64-Bit Data Encryption Using 56-Bit Key**
- **DMA Interface**
- **3 Interrupt Outputs to Aid in Loading and Unloading Data**
- **7-Bit User Output Port**
- **Single 5V ± 10% Power Supply**
- **Peripheral to MCS-86™, MCS-85™, MCS-80™ and MCS-48™ Processors**
- **Implements Federal Information Processing Data Encryption Standard**
- **Encrypt and Decrypt Modes Available**

DESCRIPTION

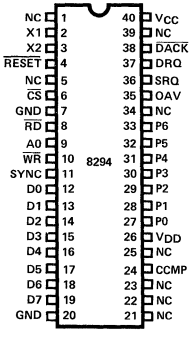
The Intel® 8294 Data Encryption Unit (DEU) is a microprocessor peripheral device designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard. The DEU operates on 64-bit text words using a 56-bit user-specified key to produce 64-bit cipher words. The operation is reversible: if the cipher word is operated upon, the original text word is produced. The algorithm itself is permanently contained in the 8294; however, the 56-bit key is user-defined and may be changed at any time.

The 56-bit key and 64-bit message data are transferred to and from the 8294 in 8-bit bytes by way of the system data bus. A DMA interface and three interrupt outputs are available to minimize software overhead associated with data transfer. Also, by using the DMA interface two or more DEUs may be operated in parallel to achieve effective system conversion rates which are virtually any multiple of 80 bytes/second. The 8294 also has a 7-bit TTL compatible output port for user-specified functions.

Because the 8294 implements the NBS encryption algorithm it can be used in a variety of Electronic Funds Transfer applications as well as other electronic banking and data handling applications where data must be encrypted.

MPU PERIPHERALS

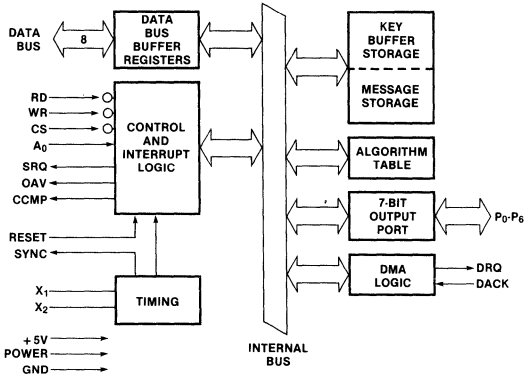
PIN CONFIGURATION



PIN NAMES

PIN NAME	FUNCTION
D_7-D_0	DATA BUS
$\overline{RD}$,$\overline{WR}$	READ,WRITE STROBES
$\overline{CS}$	CHIP SELECT
A_0	CONTROL/DATA SELECT
$\overline{RESET}$	RESET INPUT
X_1X_2	FREQUENCY REFERENCE INPUT
SYNC	HIGH FREQUENCY OUTPUT
DRQ,$\overline{DACK}$	DMA REQUEST,DMA ACKNOWLEDGE
SRQ,OAV,CCMP	INTERRUPT REQUEST OUTPUTS
P_6-P_0	OUTPUT PORT LINES
V_{CC},V_{DD},GND	+5V POWER,GND
NC	NO CONNECTION

BLOCK DIAGRAM



Pin #	Pin Name	I/O	Pin Description
1	NC	—	No connection.
2	X1	I	Inputs for crystal, L-C or external timing signal to determine internal oscillator frequency.
3	X2		
4	$\overline{RESET}$	I	A low signal to this pin resets the 8294.
5	NC	—	No connection.
6	$\overline{CS}$	I	A low signal to this pin enables reading and writing to the 8294.
7	GND	—	This pin must be tied to ground.
8	$\overline{RD}$	I	An active low read strobe at this pin enables the CPU to read data and status from the internal DEU registers.
9	A_0	I	Address input used by the CPU to select DEU registers during read and write operations.
10	$\overline{WR}$	I	An active low write strobe at this pin enables the CPU to send data and commands to the DEU.
11	SYNC	O	High frequency (Clock ÷ 15) output. Can be used as a strobe for external circuitry.
12	D_0	I/O	Three-state, bi-directional data bus lines used to transfer data between the CPU and the 8294.
13	D_1		
14	D_2		
15	D_3		
16	D_4		
17	D_5		
18	D_6		
19	D_7		
20	GND	—	This pin must be tied to ground.
21	NC	—	No connection.
22	NC	—	No connection.
23	NC	—	No connection.
24	CCMP	O	Conversion Complete. Interrupt to the CPU indicating that the encryption/decryption of an 8-byte block is complete.
25	NC	—	No connection.
26	V_{DD}	—	+5V power input. (+5V ± 10%) Low power standby pin.
27	P0	O	User output port lines. Output lines available to the user via a CPU command which can assert selected port lines. These lines have nothing to do with the encryption function. At power-on, each line is in a 1 state.
28	P1		
29	P2		
30	P3		
31	P4		
32	P5		
33	P6		
34	NC	—	No connection.
35	OAV	O	Output Available. Interrupt to the CPU indicating that the 8294 has data or status available in its output buffer. OAV = 1 implies OBF = 1.
37	DRQ	O	DMA request. Output signal to the 8257 DMA Controller requesting a DMA cycle.
38	SRQ	O	Service Request. Interrupt to the CPU indicating that the 8294 is awaiting data or commands at the input buffer. SRQ = 1 implies IBF = 0.
38	$\overline{DACK}$	I	DMA acknowledge. Input signal from the 8257 DMA Controller acknowledging that the requested DMA cycle has been granted.
39	NC	—	No connection.
40	V_{CC}	—	+5 volt power input: +5V ± 10%.

BASIC FUNCTIONAL DESCRIPTION

OPERATION

The data conversion sequence is as follows:

1. A Set Mode command is given, enabling the desired interrupt outputs.
2. An Enter New Key command is issued, followed by 8 data inputs which are retained by the DEU for encryption/decryption. Each byte must have odd parity.
3. An Encrypt Data or Decrypt Data command sets the DEU in the desired mode.

After this, data conversions are made by writing 8 data bytes and then reading back 8 converted data bytes. Any of the above commands may be issued between data conversions to change the basic operation of the DEU; e.g., a Decrypt Data command could be issued to change the DEU from encrypt mode to decrypt mode without changing either the key or the interrupt outputs enabled.

INTERNAL DEU REGISTERS

Four internal registers are addressable by the master processor: 2 for input, and 2 for output. The following table describes how these registers are accessed.

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_0	Register
1	0	0	0	Data input buffer
0	1	0	0	Data output buffer
1	0	0	1	Command input buffer
0	1	0	1	Status output buffer
X	X	1	X	Don't care

The functions of each of these registers are described below.

Data Input Buffer — Data written to this register is interpreted in one of three ways, depending on the preceding command sequence.

1. Part of a key.
2. Data to be encrypted or decrypted.
3. A DMA block count.

Data Output Buffer — Data read from this register is the output of the encryption/decryption operation.

Command Input Buffer — Commands to the DEU are written into this register. (See command summary below.)

Status Output Buffer — DEU status is available in this register at all times. It is used by the processor for poll-driven command and data transfer operations.

STATUS BIT:	7	6	5	4	3	2	1	0
FUNCTION:	X	X	X	KPE	CF	DEC	IBF	OBF

OBF Output Buffer Full; OBF = 1 indicates that output from the encryption/decryption function is available in the Data Output Buffer. It is reset when the data is read.

IBF Input Buffer Full; A write to the Data Input Buffer or to the Command Input Buffer sets IBF = 1. The DEU resets this flag when it has accepted the input byte. Nothing should be written when IBF = 1.

DEC Decrypt; indicates whether the DEU is in an encrypt or a decrypt mode. DEC = 1 implies the decrypt mode. DEC = 0 implies the encrypt mode.

CF Completion Flag; This flag may be used to indicate any or all of three events in the data transfer protocol.

1. It may be used in lieu of a counter in the processor routine to flag the end of an 8-byte transfer.
2. It must be used to indicate the validity of the KPE flag.
3. It may be used in lieu of the CCMP interrupt to indicate the completion of a DMA operation.

KPE Key Parity Error; After a new key has been entered, the DEU uses this flag in conjunction with the CF flag to indicate correct or incorrect parity.

COMMAND SUMMARY

1 — Enter New Key

OP CODE:

0	1	0	0	0	0	0	0
MSB							LSB

This command is followed by 8 data byte inputs which are retained in the key buffer (RAM) to be used in encrypting and decrypting data. These data bytes must have odd parity represented by the LSB.

2 — Encrypt Data

OP CODE:

0	0	1	1	0	0	0	0
MSB							LSB

This command puts the 8294 into the encrypt mode.

3 — Decrypt Data

OP CODE:

0	0	1	0	0	0	0	0
MSB							LSB

This command puts the 8294 into the decrypt mode.

4 — Set Mode

OP CODE:

0	0	0	0	A	B	C	D
MSB							LSB

where:

A is the OAV (Output Available) interrupt enable
B is the SRQ (Service Request) interrupt enable
C is the DMA (Direct Memory Access) transfer enable
D is the CCMP (Conversion Complete) interrupt enable

MPU PERIPHERALS

This command determines which interrupt outputs will be enabled. A "1" in bits A, B, or D will enable the OAV, SRQ, or CCMP interrupts respectively. A "1" in bit C will allow DMA transfers. When bit C is set the OAV and SRQ interrupts should also be enabled (bits A,B = 1). Following the command in which bit C, the DMA bit, is set, the 8294 will expect one data byte to specify the number of 8-byte blocks to be converted using DMA.

5 — Write to Output Port

OP CODE:

1	P_6	P_5	P_4	P_3	P_2	P_1	P_0
MSB							LSB

This command causes the 7 least significant bits of the command byte to be latched as output data on the 8294 output port. The initial output data is 1111111. Use of this port is independent of the encryption/decryption function.

PROCESSOR/DEU INTERFACE PROTOCOL

ENTERING A NEW KEY

The timing sequence for entering a new key is shown in Figure 1. A flowchart showing the CPU software to accommodate this sequence is given in Figure 2.

After the Enter New Key command is issued, 8 data bytes representing the new key are written to the data input buffer (most significant byte first). After the eighth byte is accepted by the DEU, CF goes true (CF = 1). The CF bit goes false again when KPE is valid. The CPU can then check the KPE flag. If KPE = 1, a parity error has been detected and the DEU has not accepted the key. Each byte is checked for odd parity, where the parity bit is the LSB of each byte.

Since the CF bit is used in this protocol to indicate the validity of the KPE flag, it may not be used to flag the end of the 8 byte key entry. CF = 1 only as long as KPE is invalid. Therefore, the CPU might not detect that CF = 1 and the key entry is complete before KPE becomes valid. Thus, a counter should be used, as in Figure 2, to flag the end of the new key entry. Then, CF is used to indicate a valid KPE flag.

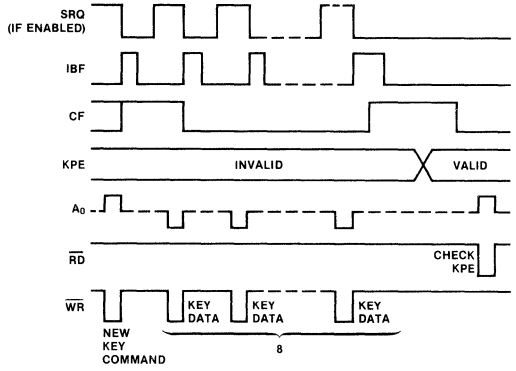


Figure 1. Entering a New Key

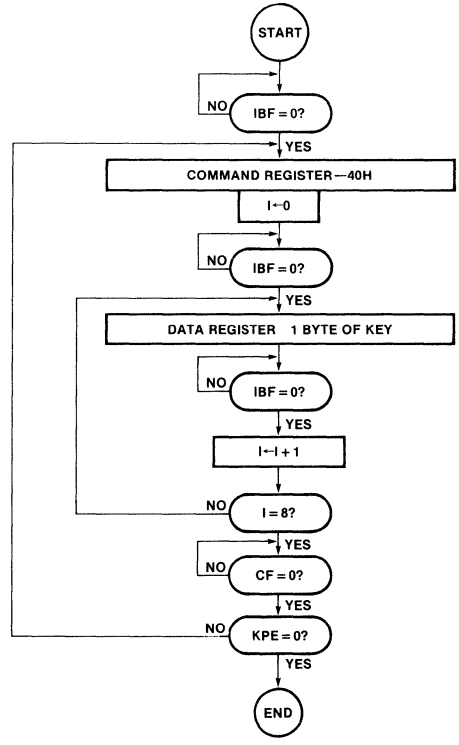


Figure 2. Flowchart for Entering a New Key

ENCRYPTING OR DECRYPTING DATA

Figure 3 shows the timing sequence for encrypting or decrypting data. The CPU writes 8 data bytes to the DEU's data input buffer for encryption/decryption. CF then goes true (CF = 1) to indicate that the DEU has accepted the 8-byte block. Thus, the CPU may test for IBF = 0 and CF = 1 to terminate the input mode, or it may use a software counter. When the encryption/-decryption is complete, the CCMP and OAV interrupts are asserted and the OBF flag is set true (OBF = 1). OAV and OBF are set false again after each of the converted data bytes is read back by the CPU. The CCMP interrupt is set false, and remains false, after the first read. After 8 bytes have been read back by the CPU, CF goes false (CF = 0). Thus, the CPU may test for CF = 0 to terminate the read mode. Also, the CCMP interrupt may be used to initiate a service routine which performs the next series of 8 data reads and 8 data writes.

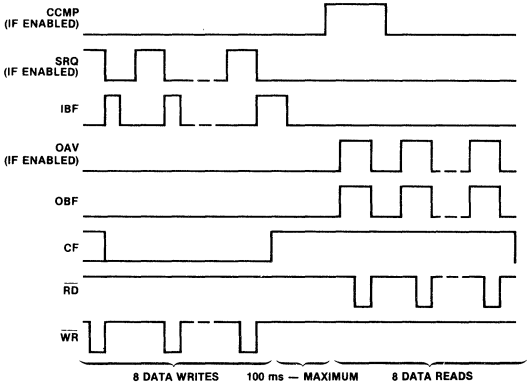


Figure 3. Encrypting/Decrypting Data

Figure 4 offers two flowcharts outlining the alternative means of implementing the data conversion protocol. Either the CF flag or a software counter may be used to end the read and write modes.

SRQ = 1 implies IBF = 0, OAV = 1 implies OBF = 1. This allows interrupt routines to do data transfers without checking status first. However, the OAV service routine must detect and flag the end of a data conversion.

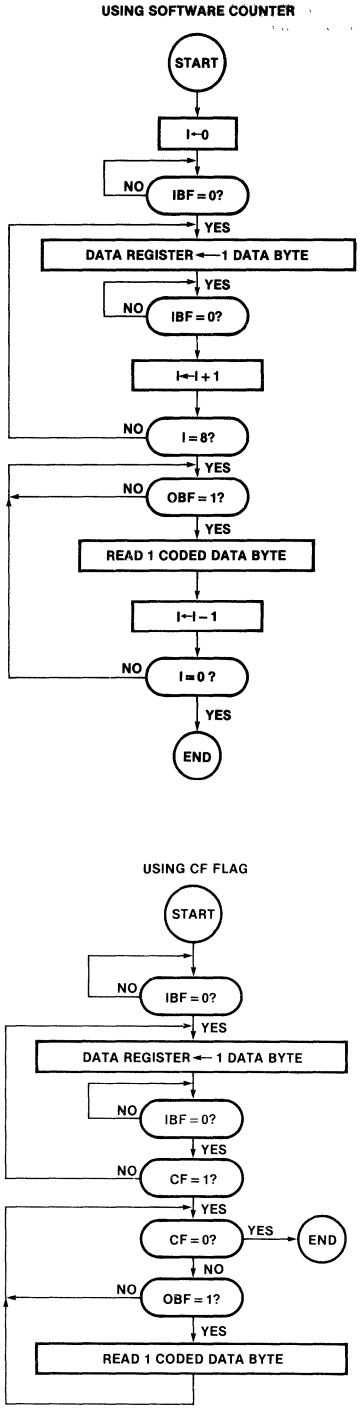


Figure 4. Data Conversion Flowcharts

USING DMA

The timing sequence for data conversions using DMA is shown in Figure 5. This sequence can be better understood when considered in conjunction with the hardware DMA interface in Figure 6. Note that the use of the DMA feature requires 3 external AND gates and 2 DMA channels (one for input, one for output). Since the DEU has only one DMA request pin, the SRQ and OAV outputs are used in conjunction with two of the AND gates to create separate DMA request outputs for the 2 DMA channels. The third AND gate combines the two active-low $\overline{DACK}$ inputs.

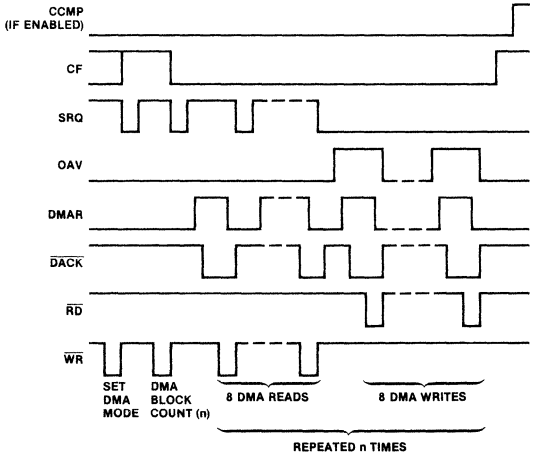
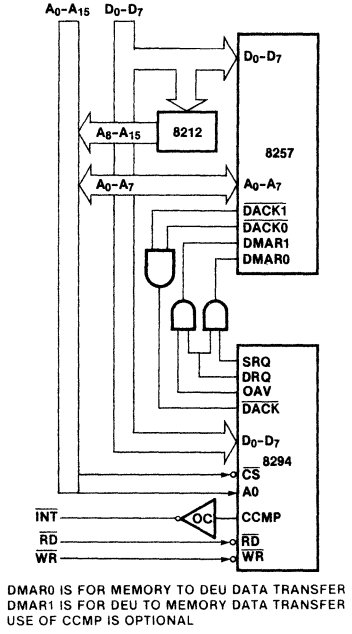


Figure 5. DMA Sequence



DMAR0 IS FOR MEMORY TO DEU DATA TRANSFER
DMAR1 IS FOR DEU TO MEMORY DATA TRANSFER
USE OF CCMP IS OPTIONAL

Figure 6. DMA Interface

To initiate a DMA transfer, the CPU must first initialize the two DMA channels as shown in the flowchart in Figure 7. It must then issue a Set Mode command to the DEU enabling the OAV, SRQ, and DMA outputs. The CCMP interrupt may be enabled or disabled, depending on whether that output is desired. Following the Set Mode command, there must be a data byte giving the number of 8-byte blocks of data (n<256) to be converted. The DEU then generates the required number of DMA requests to the 2 DMA channels with no further CPU intervention. When the requested number of blocks has been converted, the DEU will set CF and assert the CCMP interrupt (if enabled). CCMP then goes false again with the next write to the DEU (command or data). Upon completion of the conversion, the DMA mode is disabled and the DEU returns to the encrypt/decrypt mode. The enabled interrupt outputs, however, will remain enabled until another Set Mode command is issued.

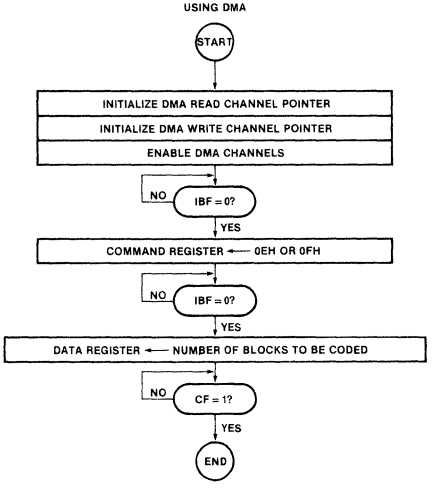


Figure 7. DMA Flowchart

SINGLE BYTE COMMANDS

Figure 8 shows the timing and protocol for single byte commands. Note that any of the commands is effective as a pacify command in that they may be entered at any time, except during a DMA conversion. The DEU is thus set to a known state. However, if a command is issued out of sequence, an additional protocol is required (Figure 9). The CPU must wait until the command is accepted (IBF = 0). A data read must then be issued to clear anything the preceding command sequence may have left in the Data Output Buffer.

CPU/DEU INTERFACES

Figures 10 through 13 illustrate four interface configurations used in the CPU/DEU data transfers. In all cases SRQ will be true (if enabled) and IBF will be false when the DEU is ready to accept data or commands.

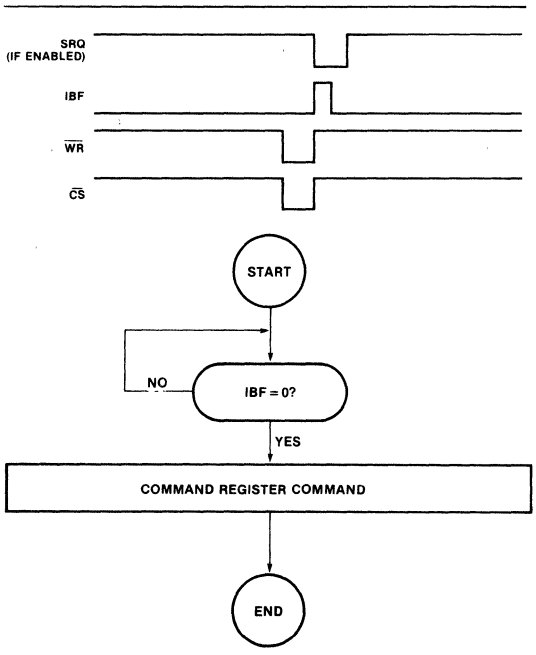


Figure 8. Single Byte Commands

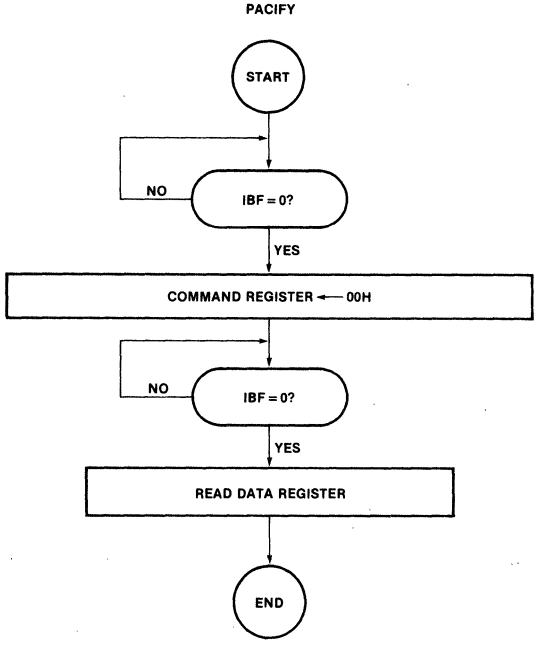


Figure 9. Pacify Protocol

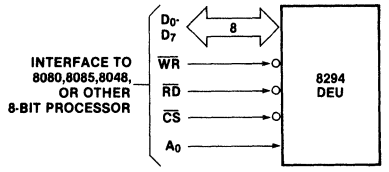


Figure 10. Polling Interface

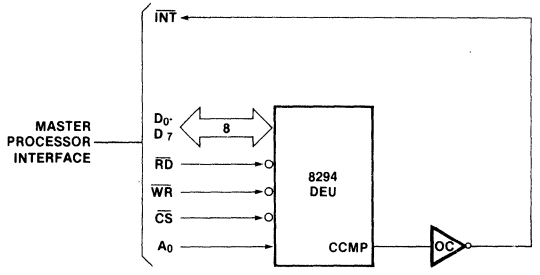


Figure 11. Single Interrupt Interface

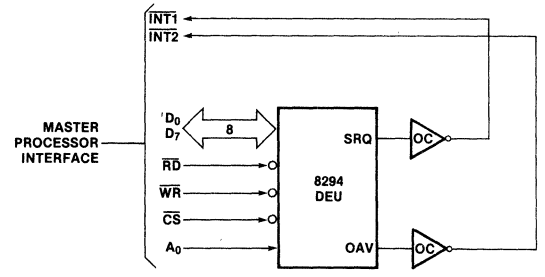
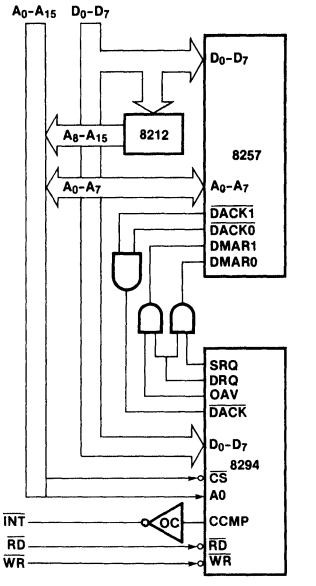


Figure 12. Dual Interrupt Interface



DMAR0 IS FOR MEMORY TO DEU DATA TRANSFER
DMAR1 IS FOR DEU TO MEMORY DATA TRANSFER
USE OF CCMP IS OPTIONAL

Figure 13. DMA Interface

OSCILLATOR AND TIMING CIRCUITS

The 8294's internal timing generation is controlled by a self-contained oscillator and timing circuit. A choice of crystal, L-C or external clock can be used to derive the basic oscillator frequency.

The resident timing circuit consists of an oscillator, a state counter and a cycle counter as illustrated in Figure 14.

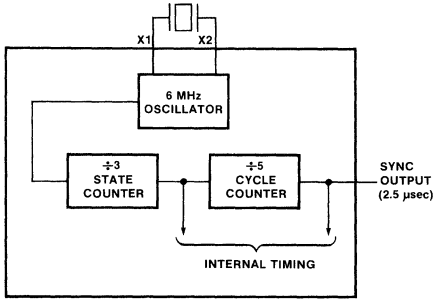
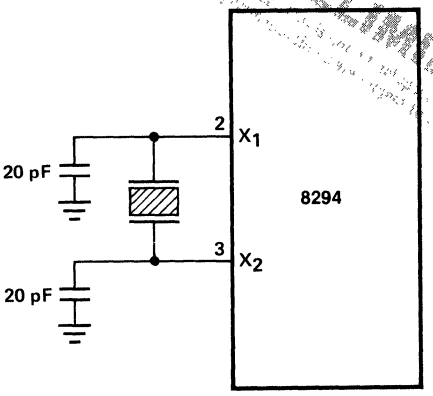


Figure 14. Oscillator Configuration

OSCILLATOR

The on-board oscillator is a series resonant circuit with a frequency range of 1 to 6 MHz. Pins X1 and X2 are input and output (respectively) of a high gain amplifier stage. A crystal or inductor and capacitator connected between X1 and X2 provide the feedback and proper phase shift for oscillation. Recommended connections for crystal or L-C are shown in Figure 15.



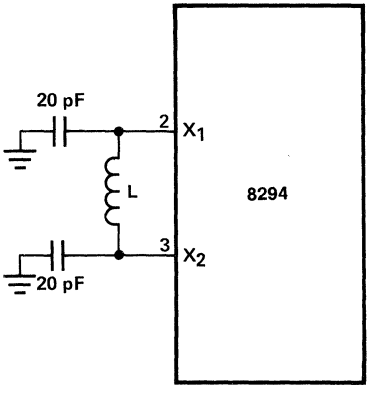


Figure 15. Recommended Crystal and L-C Connections

A recommended range of inductance and capacitance combinations is given below:

L = 130 μH corresponds to 3 MHz
L = 40 μH corresponds to 5 MHz

An external clock signal can also be used as a frequency reference to the 8294; however, the levels are *not* compatible. The signal must be in the 1 MHz-6 MHz frequency range and must be connected to pins X1 and X2 by buffers with a suitable pull-up resistor to guarantee that a logic "1" is above 3.0 volts. Two recommended connections are shown in Figure 16.

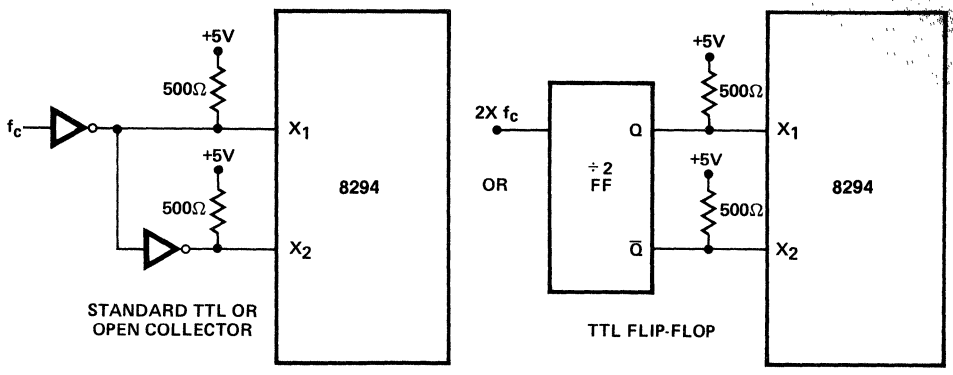


Figure 16. Recommended Connections for External Clock Signal

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin With
Respect to Ground ..... 0.5V to +7V
Power Dissipation ..... 1.5 Watt

COMMENT
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C TO 70°C, V_{CC} = V_{DD} = +5V ± 10% V_{SS} = 0V

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except X_1, X_2, $\overline{RESET}$)	−0.5		0.8	V	
V_{IH_1}	Input High Voltage (All Except X_1, X_2 $\overline{RESET}$)	2.0		V_{CC}	V	
V_{IH2}	Input High Voltage (X_1,X_2 $\overline{RESET}$)	3.0		V_{CC}	V	
V_{OL_1}	Output Low Voltage (D_0-D_7, Sync)			0.45	V	I_{OL} = 2.0 mA
V_{OL2}	Output Low Voltage All Other Outputs			0.45	V	I_{OL} = 1.6 mA
V_{OH1}	Output High Voltage (D_0-D_7)	2.4			V	I_{OH} = −400 μA
V_{OH2}	Output High Voltage (All Other Outputs)	2.4			V	I_{OH} = −50 μA
I_{IL}	Input Leakage Current $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A_0,			± 10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{OZ}	Output Leakage Current (D_0-D_7, High Z State)			± 10	μA	$V_{SS}+0.45 \leq V_{IN} \leq V_{CC}$
I_{DD}	V_{DD} Supply Current		10	25	mA	
$I_{DD}+I_{CC}$	Total Supply Current		65	135	mA	
I_{LI1}	Low Input Load Current Pins 24, 27-38			0.4	mA	V_{IL} = 0.8V
I_{LI2}	Low Input Load Current $\overline{RESET}$			0.2	mA	V_{IL} = 0.8V

A.C. CHARACTERISTICS $T_A = 0°C$ TO $70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

DBB READ

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AR}	$\overline{CS}$,A_0 Setup to $\overline{RD}$ ↓	0		ns	
t_{RA}	$\overline{CS}$, A_0 Hold After $\overline{RD}$ ↑	0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	250		ns	
t_{AD}	$\overline{CS}$, A_0 to Data Out Delay		150	ns	
t_{RD}	$\overline{RD}$ ↓ to Data Out Delay		150	ns	
t_{RDF}	$\overline{RD}$ ↑ to Data Float Delay	10		ns	
			100	ns	
t_{RV}	Recovery Time Between Reads and/or Write	1		μs	
t_{CY}	Cycle Time	2.5		μs	6 MHz Crystal

DBB WRITE

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	$\overline{CS}$, A_0 Setup to $\overline{WR}$ ↓	0		ns	
t_{WA}	$\overline{CS}$, A_0 Hold After $\overline{WR}$ ↑	0		ns	
t_{WW}	$\overline{WR}$ Pulse Width	250		ns	
t_{DW}	Data Setup to $\overline{WR}$ ↑	150		ns	
t_{WD}	Data Hold to $\overline{WR}$ ↑	0		ns	

DMA AND INTERRUPT TIMING

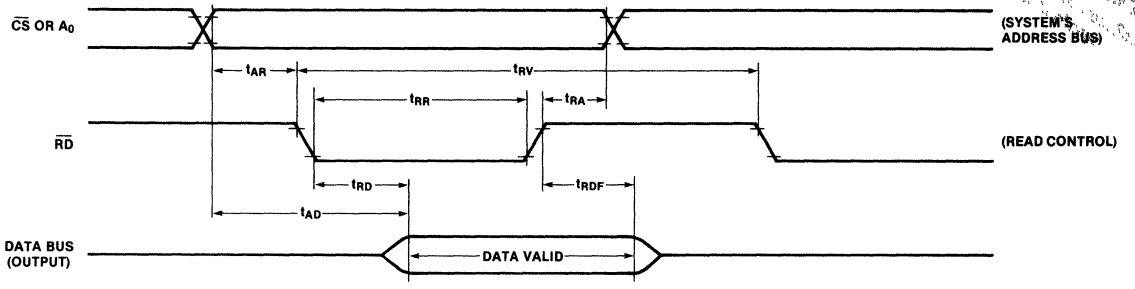
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{KC}	$\overline{DACK}$ Setup to Control	50		ns	
t_{CK}	$\overline{DACK}$ Hold After Control	0		ns	
t_{CR}	Control L.E. to DRQ T.E.		150	ns	
t_{CI}	Control T.E. to Interrupt T.E.		$t_{CY} + 500$	ns	

A.C. TEST CONDITIONS

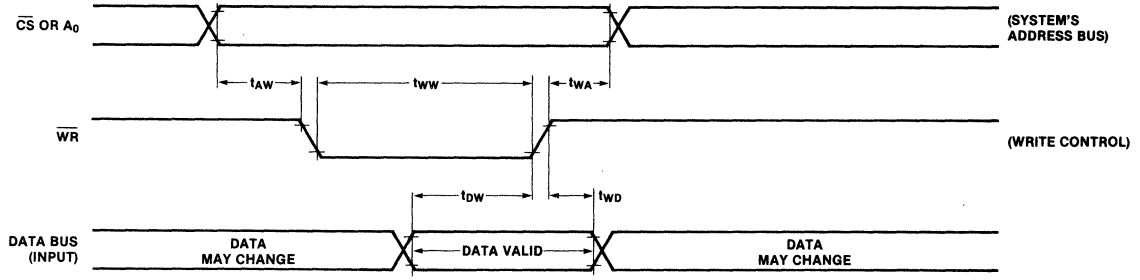
D_7–D_0 Outputs $C_L = 150$ pF

WAVEFORMS

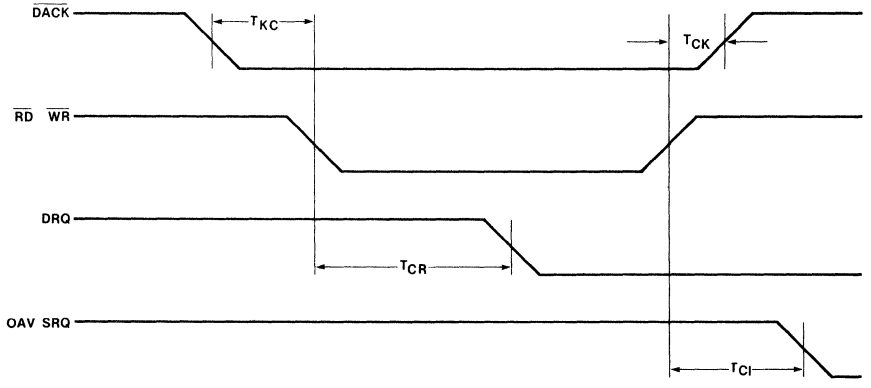
1. READ OPERATION — OUTPUT BUFFER REGISTER.



2. WRITE OPERATION — INPUT BUFFER REGISTER.



DMA AND INTERRUPT TIMING



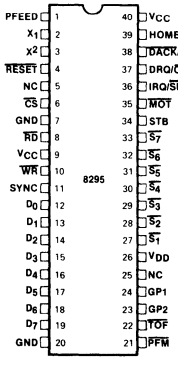
8295
DOT MATRIX PRINTER CONTROLLER

- **Interfaces Dot Matrix Printers to MCS-48™, MCS-80™, MCS-85™ Systems**
- **40 Character Buffer On Chip**
- **Serial or Parallel Communication with Host**
- **DMA Transfer Capability**
- **Programmable Character Density (10 or 12 Chararcters/Inch)**
- **Programmable Print Intensity**
- **Single or Double Width Printing**
- **Programmable Multiple Line Feeds**
- **3 Tabulations**
- **2 General Purpose Outputs**

The Intel® 8295 Dot Matrix Printer Controller provides an interface for microprocessors to the LRC 7040 Series dot matrix impact printers. It may also be used as an interface to other similar printers.

The chip may be used in a serial or parallel communication mode with the host processor. Furthermore, it provides internal buffering of up to 40 characters and contains a 7 × 7 matrix character generator accommodating 64 ASCII characters.

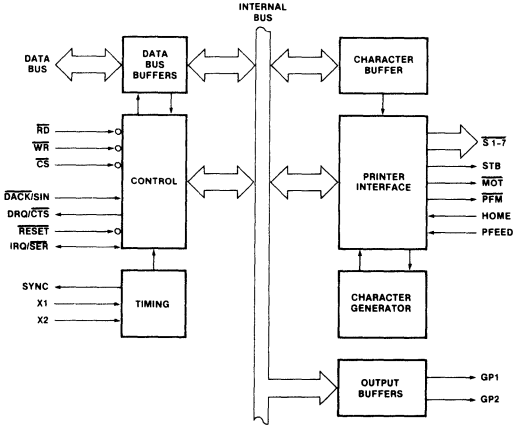
PIN CONFIGURATION



PIN NAMES

PIN NAME	FUNCTION
D_0-D_7	DATA BUS
$\overline{RD}$, $\overline{WR}$	READ, WRITE STROBES
$\overline{CS}$	CHIP SELECT
$\overline{RESET}$	RESET INPUT
X_1, X_2	FREQUENCY REFERENCE INPUTS
SYNC	HIGH FREQUENCY OUTPUT
MOT, $\overline{PFM}$	MAIN, PAPER FEED MOTOR DRIVES
DRQ, $\overline{DACK}$	DMA REQUEST, ACKNOWLEDGE
SIN, $\overline{CTS}$	SERIAL INPUT, CLEAR-TO-SEND
IRQ/$\overline{SER}$	INTERRUPT REQUEST, SERIAL GROUND
$\overline{S_1}$-$\overline{S_7}$	SOLENOID DRIVE OUTPUTS
PFEED	PAPER FEED INPUT
HOME, $\overline{TOF}$	HOME, TOP-OF-FORM INPUTS
STB	SOLENOID STROBE OUTPUT
GP1, GP2	GENERAL PURPOSE OUTPUTS
V_{CC}, V_{DD}, GND	+5V POWER, GND

BLOCK DIAGRAM



MPU PERIPHERALS

FUNCTIONAL DESCRIPTION

The 8295 interfaces microcomputers to the LRC 7040 Series dot matrix impact printers, and to other similar printers. It provides internal buffering of up to 40 characters. Printing begins automatically when the buffer is full or when a carriage return character is received.

Communication between the 8295 and the host processor can be implemented in either a serial or parallel mode. The parallel mode allows for character transfers into the buffer via DMA cycles. The serial mode features selectable data rates from 110 to 4800 baud.

The 8295 also offers two general purpose output pins which can be set or cleared by the host processor. They can be used with various printers to implement such functions as ribbon color selection, enabling form release solenoid, and reverse document feed.

COMMAND SUMMARY

Hex Code	Description
00	Clear GP1. This command brings the GP1 pin to a logic low state. After power on it is automatically set high.
01	Clear GP2. Same as the above but for GP2.
02	Set GP1. Sets GP1 pin to a logic high state, inverse of command 00.
03	Set GP2. Same as above but for GP2. Inverse command 01.
04	Software Reset. This is a pacify command. This command is not effective immediately after commands requiring a parameter, as the Reset command will be interpreted as a parameter.
05	Print 10 characters/in. density.
06	Print 12 characters/in. density.
07	Print double width characters. This command prints characters at twice the normal width, that is, at either 17 or 20 characters per line.
08	Enable DMA mode; must be followed by two bytes specifying the number of data characters to be fetched. Least significant byte accepted first.
09	Tab character.
0A	Line feed.
0B	Multiple Line Feed; must be followed by a byte specifying the number of line feeds.
0C	Top of Form. Enables the line feed output until the Top of Form input is activated.
0D	Carriage Return. Signifies end of a line and enables the printer to start printing.
0E	Set Tab #1, followed by tab position byte.
0F	Set Tab #2, followed by tab position byte. Should be greater than Tab #1.
10	Set Tab #3, followed by tab position byte. Should be greater than Tab #2.
11	Print Head Home on Right. On some printers the print head home position is on the right. This command would enable normal left to right printing with such printers.
12	Set Strobe Width; must be followed by strobe width selection byte. This command adjusts the duration of the strobe activation.

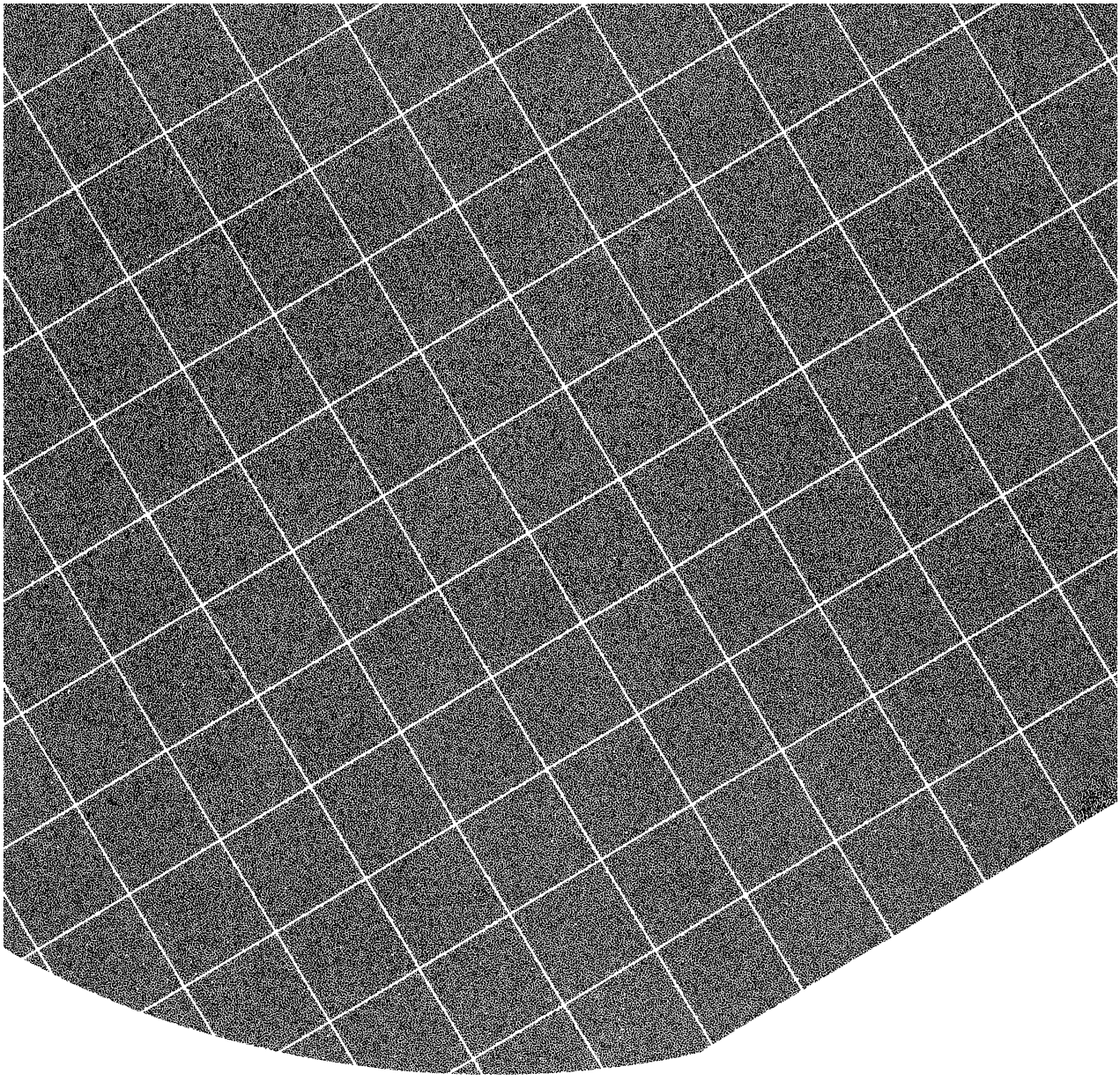
CHARACTER SET

Hex Code	Print Char.	Hex Code	Print Char.	Hex Code	Print Char.	Hex Code	Print Char.
20	space	30	0	40	@	50	P
21	!	31	1	41	A	51	Q
22	"	32	2	42	B	52	R
23	#	33	3	43	C	53	S
24	$	34	4	44	D	54	T
25	%	35	5	45	E	55	U
26	&	36	6	46	F	56	V
27	,	37	7	47	G	57	W
28	(	38	8	48	H	58	X
29	)	39	9	49	I	59	Y
2A	*	3A	:	5A	J	5A	Z
2B	+	3B	;	4B	K	5B	[
2C	'	3C	<	4C	L	5C	\
2D	–	3D	=	4D	M	5D	]
2E	.	3E	>	4E	N	5E	↑
2F	/	4F	?	4F	O	5F	—

PIN DESCRIPTION

Name	I/O	Pin #	Description
D_0-D_7	I/O	12-19	Three-state bidirectional data bus buffer lines used to interface the 8295 to the host processor in the parallel mode. In the serial mode D_0-D_2 sets up the baud rate.
$\overline{WR}$	I	10	Write input which enables the master CPU to write data and commands to the 8295. In the serial mode this pin must be tied to ground.
$\overline{RD}$	I	8	Read input which enables the master CPU to read data and status. In the serial mode this pin must be tied to V_{CC}.
$\overline{CS}$	I	6	Chip select input used to enable the $\overline{RD}$ and $\overline{WR}$ inputs except during DMA, active low.
$\overline{RESET}$	I	4	Reset input, active low. After reset the 8295 will be set for 12 characters/inch single width printing, solenoid strobe at 320 msec.
PFEED	I	1	Paper feed input switch.
HOME	I	39	Home input switch, used by the 8295 to detect that the print head is in the home position.
X_1, X_2	I	2,3	Inputs for a crystal to set internal oscillator frequency. For proper operation use 6 MHz crystal.
$\overline{PFM}$	O	21	Paper feed motor drive, active low.
$\overline{MOT}$	O	35	Main motor drive, active low.
GP1, GP2	O	23,24	General purpose output pins.
$\overline{S_1}$-$\overline{S_7}$	O	27-33	Solenoid drive outputs; active low.
STB	O	34	Solenoid strobe output. Used to determine duration of solenoids activation.
$\overline{TOF}$	I	22	Top of form input, used to sense top of form signal for type T printer, active low.
IRQ/$\overline{SER}$	I/O	36	In parallel mode it is an interrupt request input to the master CPU; in serial mode it should be strapped to ground.
DRQ/$\overline{CTS}$	O	37	In the parallel mode used as DMA request output pin to indicate to the 8257 that a DMA transfer is requested; in the serial mode used as clear-to-send signal.
$\overline{DACK}$/ SIN	I/O	38	In the parallel mode used as DMA acknowledgement; in the serial mode, used as input for data.
SYNC	O	11	Output signal which occurs once per instruction cycle (2.5 μsec with 6 MHz crystal); can be used as a reference clock.
V_{CC}	—	9,40	+5V power supply.
V_{DD}	—	26	+5V low power standby supply.
GND	—	20	Circuit and supply ground.

MPU
PERIPHERALS



Microcomputer Development Systems 12

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MODEL 210
INTELLEC SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Low cost development system for MCS-80, MCS-85, and MCS-48 microprocessor families

Compact four-slot chassis

Single LSI electronics board with CPU, 32K bytes RAM memory, and 4K bytes ROM memory

Self-test diagnostic capability

Eight-level nested, maskable priority interrupt system

Built-in interfaces for TTY, CRT, printer, high speed paper tape reader/punch and universal PROM programmer

Standard MULTIBUS with multiprocessor and DMA capabilities

ROM-based monitor, assembler, and editor

Compatible with standard Intellec/iSBC expansion modules

Software compatible with previous Intellec systems

The Model 210 Intellec Series II Microcomputer Development System is a low cost, fully supported development system providing basic hardware and software support for development of products based around Intel's MCS-80 or MCS-85 microprocessor families. Through optional software, this development capability can be extended to products based on the MCS-48 family of microprocessors. Using the user supplied system console (TTY or equivalent), the product designer may enter and correct a program source code, assemble, and begin execution, all using the Model 210 ROM-resident editor/assembler. MCS-80 and MCS-85 debugging is accomplished by means of system monitor debug commands. Completed programs may be punched to paper tape for loading into the user's system or programmed into PROM using the optional Intellec UPP-103 Universal PROM Programmer.

FUNCTIONAL DESCRIPTION

Hardware Components

The Intellec Series II Model 210 is a compact, 4-inch table-top chassis with a 4-slot cardcage, power supply, and two printed circuit cards. The CPU, interrupt, I/O, and bus interface circuitry are all fashioned from Intel's high technology LSI components and located on one PC board. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second PC board (the parallel I/O board — PIO) containing additional I/O interface logic is mounted on the rear panel. The remaining 3 slots in the cardcage are available for system expansion. A simplified block diagram of the IPB is shown in Figure 1.

System Components

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap "self-test" diagnostics, and the Intellec Series II System Monitor. The eight-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259 interrupt controller, the interrupt system may be user programmed to respond to individual needs.

Input/Output

IPB Serial Channels — The I/O subsystem in the Model 210 consists of two parts. Two serial channels are provided directly on the IPB itself. Each channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. One channel contains current loop adapters for teletype compatibility. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished programmatically through an Intel 8253 interval timer. The 8253 also serves as the real-time clock for the entire system. I/O activity is signaled to the system through a second 8259 interrupt controller, operating in a polled mode, nested to the primary 8259.

PIO Interface Logic — The second part of the I/O subsystem consists of the interface logic provided on the PIO board itself. Utilizing Intel's UPI-41 programmable peripheral controller, the PIO board provides device interfaces for standard Intellec peripherals, including a printer, high speed paper tape reader, high speed paper tape punch, and Universal PROM programmer. Communication between the IPB and PIO is maintained over a separate 8-bit bidirectional data bus. Connectors for the four devices specified above, as well as the two serial channels, are mounted directly on the PIO.

Control

User control is maintained through a front panel consisting of a power switch and indicator, reset/boot switch, run/halt light, and eight interrupt switches and indicators. The front-panel circuit board is attached directly to the IPB, allowing the eight interrupt switches to connect to the primary 8259, as well as to the Intellec Series II bus.

MULTIBUS Capability

All Intellec Series II models implement the industry-standard MULTIBUS. MULTIBUS enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microprocessor family.

Software

All standard Model 210 software is ROM-based to eliminate costly delays of loading paper tape. The capabilities of the system monitor with its "self-test" diagnostics, text editor, and MCS-80/MCS-85 or MCS-48 ROM assemblers are described on pages 10-22 to 10-25 of this catalog.

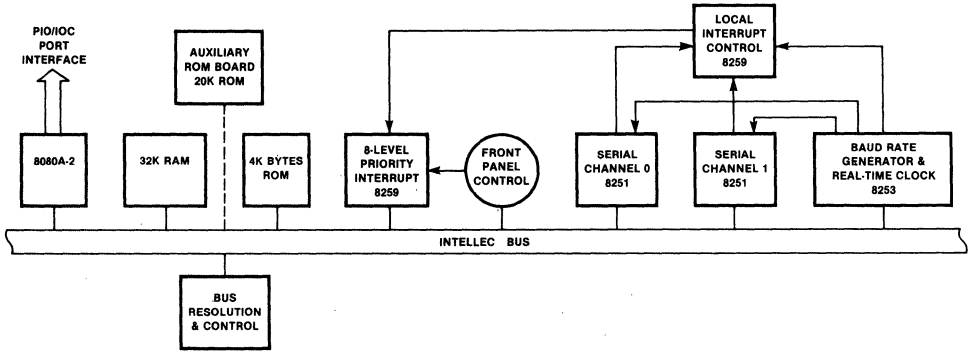


Figure 1. Simplified Integrated Processor Board (IPB) Block Diagram for the Model 210 Intellec Series II Microcomputer Development System

SPECIFICATIONS

Host Processor (IPB)

8080A-2 based, operating at 2.600 MHz.

RAM — 32K, expandable to 64K with iSBC 032 RAM board (system monitor occupies 62K through 64K)

ROM — 4K (2K in monitor, 2K in boot/diagnostic), expandable with addition of 20K auxiliary ROM board containing text editor and assembler

Bus — MULTIBUS, maximum transfer rate of 5 MHz

Clocks — Host processor, crystal controlled at 2.6 MHz, bus clock, crystal controlled at 9.8304 MHz

Memory Access Time

RAM — 585 ns max

PROM — 450 ns max

I/O Interfaces

2 serial I/O channels, RS232C, at 110-9600 baud (asynchronous) or 150-56K baud (synchronous). Baud rates and serial format fully programmable using Intel 8251 USARTs. Serial channel 1 additionally provided with 20 mA current loop. Parallel I/O interfaces provided for paper tape punch, paper tape reader, printer, and UPP-103 Universal PROM Programmer.

Interrupts

8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

Direct Memory Access (DMA)

Standard capability on MULTIBUS; implemented for user selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

Physical Characteristics

Width — 17.37 in. (44.12 cm)

Height — 4.81 in. (12.22 cm)

Depth — 19.13 in. (48.59 cm)

Weight — 45 lb (20.5 kg)

Electrical Characteristics

DC Power Supply

Volts Supplied	Amps Supplied	Typical System Requirements
+ 5±5%	24	3.5
+12±5%	2.0	0.1
−12±5%	0.3	0.05
−10±5%	1.0	0.1

AC Requirements

50-60 Hz, 115/230V AC

Environmental Characteristics

Operating Temperature — 0°C to 35°C (95°F)

Equipment Supplied

Model 210 chassis

Integrated processor board (IPB)

Parallel I/O board (PIO)

ROM-resident system monitor

Auxiliary ROM board with MCS-80/MCS-85 assembler and text editor

PROM programming software (paper tape)

Assembler cross reference program (paper tape)

Reference Manuals

9800558 — A Guide to Microcomputer Development Systems (SUPPLIED)

9800557 — Intellec Series II Model 210 User's Guide (SUPPLIED)

9800555 — Intellec Series II Hardware Interface Manual (SUPPLIED)

9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)

9800605 — Intellec Series II System Monitor Source Listing (SUPPLIED)

9800554 — Intellec Series II Schematic Drawings (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-210	Intellec Series II Model 210 microcomputer development system

MODEL 220
INTELLEC SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Complete microcomputer development system in one package for MCS-80, MCS-85, and MCS-48 microprocessor families

Single LSI electronics board with CPU, 32K bytes RAM memory, and 4K bytes ROM memory

Self-test diagnostic capability

Eight-level nested, maskable priority interrupt system

Built-in interfaces for high speed paper tape reader/punch, printer, and universal PROM programmer

Integral CRT with detachable upper/lower case typewriter-style full ASCII keyboard

Integral 250K-byte floppy disk with total storage capacity expandable to over 2M bytes

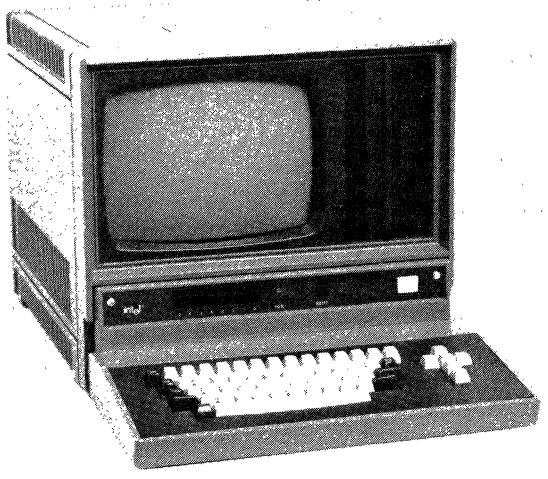
Powerful ISIS-II Diskette Operating System with relocating macroassembler, linker, and locater

Standard MULTIBUS with multi-processor and DMA capability

Compatible with standard Intellec/iSBC expansion modules

Software compatible with previous Intellec systems

The Model 220 Intellec Series II Microcomputer Development System is a complete microcomputer development system integrated into one compact package. It includes a CPU with 32K bytes of RAM memory, 4K bytes of ROM memory, a 2000-character CRT, detachable full ASCII keyboard with cursor controls and upper/lower case capability, and a 250K-byte floppy diskette drive. Powerful ISIS-II Diskette Operating System software allows the Model 220 to be used quickly and efficiently for assembling and debugging programs for Intel's MCS-80, MCS-85, or MCS-48 microprocessor families without the need for paper tape handling. ISIS-II performs all file handling operations for the user, leaving him free to concentrate on the details of his own application. When used in conjunction with an optional in-circuit emulator (ICE) module, the Model 220 provides all the hardware and software development tools necessary for the rapid development of a microcomputer-based product.



FUNCTIONAL DESCRIPTION

Hardware Components

The Intellec Series II Model 220 is a packaged, highly integrated microcomputer development system consisting of a CRT chassis with a 6-slot cardcage, power supply, fans, cables, single floppy diskette drive, and two printed circuit cards. A separate, full ASCII keyboard is connected with a cable.

CPU Cards — The master CPU card contains its own microprocessor, memory, I/O, interrupt, and bus interface circuitry, fashioned from Intel's high-technology LSI components. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second, slave CPU card, is responsible for all remaining I/O control, including the CRT and keyboard interface and floppy disk control. This card, mounted on the rear panel, also contains its own microprocessor, RAM and ROM memory, and I/O interface, thus in effect creating a dual processor environment. Known as the I/O controller (IOC), the slave CPU card communicates with the IPB over an 8-bit bidirectional data bus, thus leaving the remaining 5 slots in the cardcage available for system expansion. A block diagram of the IOC is shown in Figure 1.

System Components

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap "self-test" diagnostics and the Intellec Series II System Monitor. The eight-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259 interrupt controller, the interrupt system may be user programmed to respond to individual needs.

Input/Output

IBP Serial Channels — The I/O subsystem in the Model 220 consists of two parts: the IOC card and two serial channels on the IPB itself. Each serial channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. Both may be connected to a user defined data set or data terminal. One channel contains current loop adapters. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished programmatically through an Intel 8253 interval timer. The 8253 also serves as a real-time clock for the entire system. I/O activity through both serial channels is signaled to the system through a second 8259 interrupt controller, operating in a polled mode, nested to the primary 8259.

IOC Interface — The remainder of system I/O activity takes place in the IOC. The IOC provides interfaces for the CRT, keyboard, integral floppy disk and standard Intellec peripherals, including a printer, high speed paper tape reader/punch, and universal PROM programmer. The IOC contains its own independent microprocessor, also an 8080A-2. This CPU controls all I/O operations, as well as supervising communications with the IPB. 8K bytes of ROM contain all I/O control firmware. 8K bytes of ROM are used for CRT screen refresh storage and the floppy disk buffer. These do not occupy any space in Intellec Series II main memory since the IOC is a totally independent microcomputer subsystem.

Integral CRT Display — The CRT is a 12-inch raster scan-type monitor with a 50/60 Hz vertical scan rate and 15.5 kHz horizontal scan rate. Controls are provided for brightness and contrast adjustments. The interface to the CRT is provided through an Intel 8275 single chip, programmable CRT controller. The master processor on

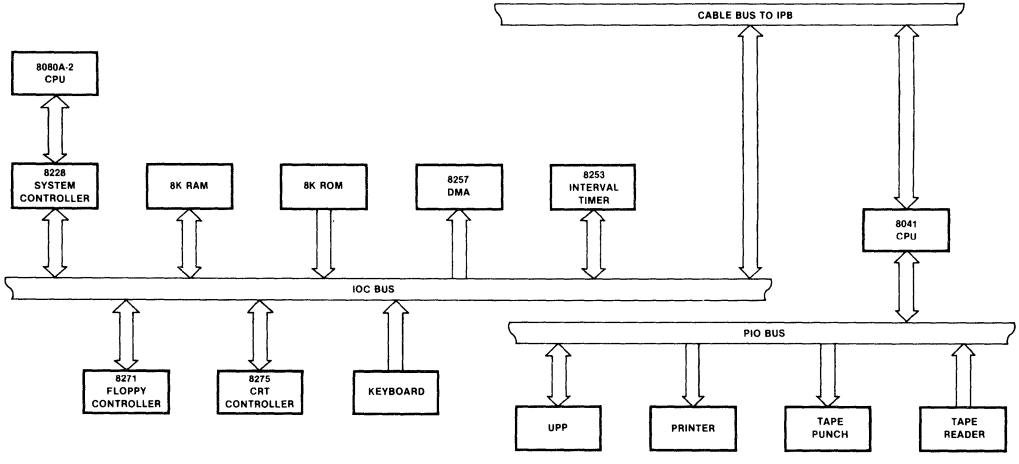


Figure 1. I/O Controller (IOC) Block Diagram for the Model 220 Intellec Series II Microcomputer Development System

the IPB transfers a character for display to the IOC, where it is stored in RAM. The CRT controller reads a line at a time into its line buffer through an Intel 8257 DMA controller and then feeds one character at a time to the character generator to produce the video signal. Timing for the CRT control is provided by an Intel 8253 interval timer. The screen display is formatted as 25 rows of 80 characters. The full set of ASCII characters are displayed, including lower-case alphas.

Keyboard — The keyboard interfaces directly to the IOC processor via an 8-bit data bus. The keyboard contains an Intel UPI-41 Universal Peripheral Interface, which scans the keyboard, encodes the characters, and buffers the characters to provide N-key rollover. The keyboard itself is a high quality typewriter-style keyboard containing the full ASCII character set. An upper/lower case switch allows the system to be used for document preparation. Cursor control keys are also provided.

Floppy Disk Drive

The floppy disk drive is controlled by an Intel 8271 single chip, programmable floppy disk controller. It transfers data via an Intel 8257 DMA controller between an IOC RAM buffer and the diskette. The 8271 handles reading and writing of data, formatting diskettes, and reading status, all upon appropriate commands from the IOC microprocessor.

Peripheral Interface

A UPI-41 Universal Peripheral Interface on the IOC board performs similar functions to the UPI-41 on the PIO board in the Model 210. It provides interface for other standard Intellec peripherals, including a printer, high speed paper tape reader, high speed paper tape punch, and universal PROM programmer. Communication between the IPB and IOC is maintained over a separate, 8-bit bidirectional data bus. Connectors for the devices named above, as well as the two serial channels, are mounted directly on the IOC itself.

Control

User control is maintained through a front panel consisting of a power switch and indicator, reset/boot switch, run/halt light, and eight interrupt switches and indicators. the front-panel circuit board is attached directly to the IPB, allowing the eight interrupt switches to connect to the primary 8259, as well as to the Intellec Series II bus.

MULTIBUS Capability

All Intellec Series II models implement the industry-standard MULTIBUS. MULTIBUS enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microcomputer family.

Expansion

The Model 220 may be expanded to 64K of RAM and up to 2.25M bytes of on-line diskette storage.

SPECIFICATIONS

Host Processor (IPB)

8080A-2 based, operating at 2.600 MHz.

RAM — 32K, expandable to 64K with iSBC 032 RAM boards (system monitor occupies 62K through 64K)

ROM — 4K (2K in monitor, 2K in boot/diagnostic)

Bus — MULTIBUS, maximum transfer rate of 5 MHz

Clocks — Host processor, crystal controlled at 2.6 MHz, bus clock, crystal controlled at 9.8304 MHz

I/O Interfaces

2 Serial I/O Channels, RS232C, at 110-9600 baud (asynchronous) or 150-56K baud (synchronous). Baud rates and serial format fully programmable using Intel 8251 USARTs. Serial Channel 1 additionally provided with 20 mA current loop. Parallel I/O interfaces provided for paper tape punch, paper tape reader, printer, and UPP-103 Universal PROM Programmer.

Interrupts

8-level, maskable, nested priority interrupt network initiated from front panel or user selected devices.

Direct Memory Access (DMA)

Standard capability on MULTIBUS; implemented for user selected DMA devices through optional DMA module — maximum transfer rate of 2 MHz.

Memory Access Time

RAM — 585 ns max

PROM — 450 ns max

Diskette

Diskette System Capacity — 250K bytes (formatted)

Diskette System Transfer Rate — 160K bits/sec

Diskette System Access Time

Track-to-Track: 10 ms max
Average Random Positioning: 260 ms max
Rotational Speed: 360 rpm
Average Rotational Latency: 83 ms max
Recording Mode: FM

Physical Characteristics

Width — 17.37 in. (44.12 cm)

Height — 15.81 in. (40.16 cm)

Depth — 19.13 in. (48.59 cm)

Weight — 86 lb (39 kg)

Keyboard
Width — 17.37 in. (44.12 cm)
Height — 3.0 in. (7.62 cm)
Depth — 9.0 in. (22.0 cm)
Weight — 6 lb (3 kg)

Electrical Characteristics

DC Power Supply

Volts Supplied	Amps Supplied	Typical System Requirements
+ 5 ± 5%	30.0	7.5
+ 12 ± 5%	2.5	0.2
− 12 ± 5%	0.3	0.05
− 10 ± 5%	1.5	0.15
+ 15 ± 5%	1.5	1.3*
+ 24 ± 5%	1.7	1.2*

*Not available on bus.

AC Requirements
50-60 Hz. 115/230V AC

Equipment Supplied

Model 220 chassis
Integrated processor board (IPB)
I/O controller board (IOC)
CRT and keyboard
250K-byte floppy disk drive
ROM resident system monitor
ISIS-II system diskette with MCS-80/MCS-85 macroassembler

Reference Manuals

9800558 — A Guide to Microcomputer Development Systems (SUPPLIED)

9800559 — Intellec Series II Installation and Service Manual (SUPPLIED)

9800306 — ISIS-II System User's Guide (SUPPLIED)

9800556 — Intellec Series II Hardware Reference Manual (SUPPLIED)

9800555 — Intellec Series II Hardware Interface Manual (SUPPLIED)

9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)

9800605 — Intellec Series II System Monitor Source Listing (SUPPLIED)

9800554 — Intellec Series II Schematic Drawing (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-220	Intellec Series II Model 220 microcomputer development system (110V/60 Hz)
MDS-221	Intellec Series II Model 220 microcomputer development system (220V/50 Hz)

MODEL 230
INTELLEC SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Complete microcomputer development center for Intel MCS-80, MCS-85, and MCS-48 microprocessor families

LSI electronics board with CPU, RAM, ROM, I/O, and interrupt circuitry

64K bytes RAM memory

Self-test diagnostic capability

Eight-level nested, maskable priority interrupt system

Built-in interfaces for high speed paper tape reader/punch, printer, and universal PROM programmer

Integral CRT with detachable upper/lower case typewriter-style full ASCII keyboard

Powerful ISIS-II Diskette Operating System software with relocating macroassembler, linker, and locater

1 million bytes (expandable to 2.5M bytes) of diskette storage

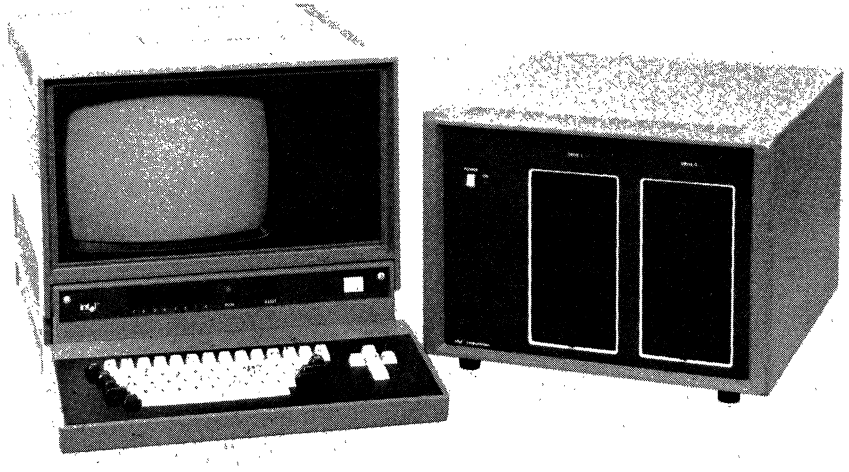
Supports PL/M and FORTRAN high level languages

Standard MULTIBUS with multiprocessor and DMA capability

Compatible with standard Intellec/iSBC expansion modules

Software compatible with previous Intellec systems

The Model 230 Intellec Series II Microcomputer Development System is a complete center for the development of microcomputer-based products. It includes a CPU, 64K bytes of RAM, 4K bytes of ROM memory, a 2000-character CRT, a detachable full ASCII keyboard, and dual double density diskette drives providing over 1 million bytes of on-line data storage. Powerful ISIS-II Diskette Operating System software allows the Model 230 to be used quickly and efficiently for assembling and/or compiling and debugging programs for Intel's MCS-80, MCS-85, or MCS-48 microprocessor families without the need for handling paper tape. ISIS-II performs all file handling operations, leaving the user free to concentrate on the details of his own application. When used in conjunction with an optional in-circuit emulator (ICE) module, the Model 230 provides all the hardware and software development tools necessary for the rapid development of a microcomputer-based product.



FUNCTIONAL DESCRIPTION

Hardware Components

The Intellec Series II Model 230 is a packaged, highly integrated microcomputer development system consisting of a CRT chassis with a 6-slot cardcage, power supply, fans, cables, and five printed circuit cards. A separate, full ASCII keyboard is connected with a cable. A second chassis contains two floppy disk drives capable of double-density operation along with a separate power supply, fans, and cables for connection to the main chassis. A block diagram of the Model 230 is shown in Figure 1.

CPU Cards — The master CPU card contains its own microprocessor, memory, I/O, interrupt and bus interface circuitry fashioned from Intel's high technology LSI components. Known as the integrated processor board (IPB), it occupies the first slot in the cardcage. A second slave CPU card is responsible for all remaining I/O control including the CRT and keyboard interface. This card, mounted on the rear panel, also contains its own microprocessor, RAM and ROM memory, and I/O interface logic, thus, in effect, creating a dual processor environment. Known as the I/O controller (IOC), the slave CPU card communicates with the IPB over an 8-bit bidirectional data bus.

Memory and Control Cards — In addition, 32K bytes of RAM (bringing the total to 64K bytes) is located on a separate card in the main cardcage. Fabricated from Intel's 16K RAMs, the board also contains all necessary address decoding and refresh logic. Two additional boards in the cardcage are used to control the two double-density floppy disk drives.

Expansion — Two remaining slots in the cardcage are available for system expansion. Additional expansion of 4 slots can be achieved through the addition of an Intellec Series II expansion chassis.

System Components

The heart of the IPB is an Intel NMOS 8-bit microprocessor, the 8080A-2, running at 2.6 MHz. 32K bytes of RAM memory are provided on the board using Intel 16K RAMs. 4K of ROM is provided, preprogrammed with system bootstrap "self-test" diagnostics and the Intellec Series II System Monitor. The eight-level vectored priority interrupt system allows interrupts to be individually masked. Using Intel's versatile 8259 interrupt controller, the interrupt system may be user programmed to respond to individual needs.

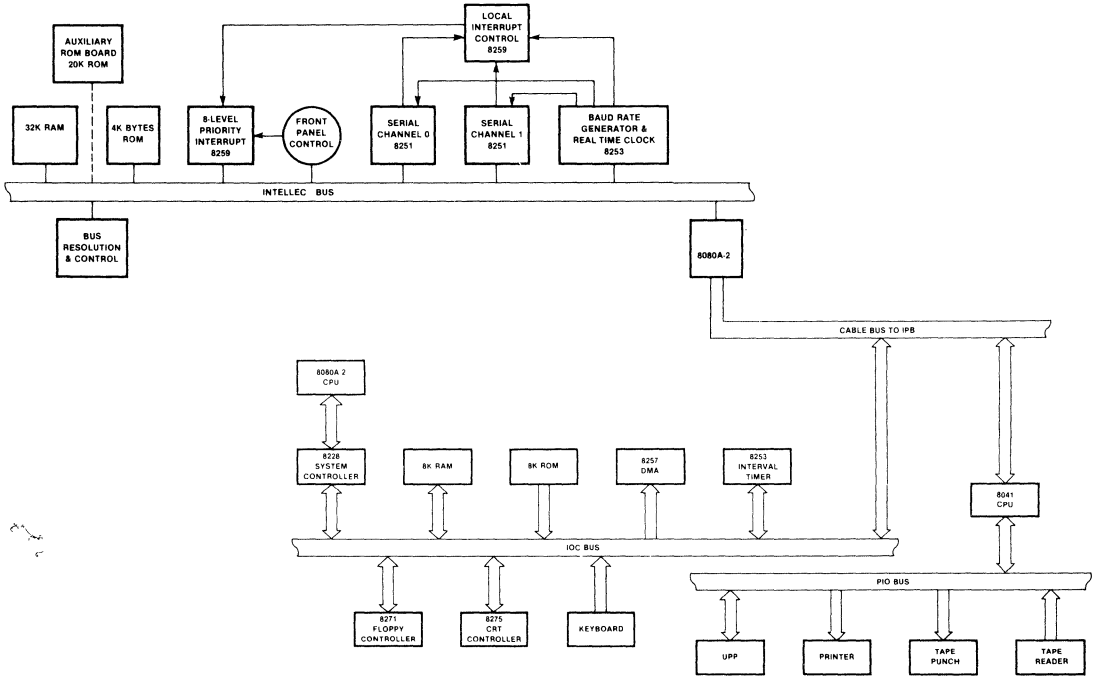


Figure 1. Intellec Series II Model 230 Microcomputer Development System Block Diagram

Input/Output

IPB Serial Channels — The I/O subsystem in the Model 230 consists of two parts: the IOC card and two serial channels on the IPB itself. Each serial channel is RS232 compatible and is capable of running asynchronously from 110 to 9600 baud or synchronously from 150 to 56K baud. Both may be connected to a user defined data set or terminal. One channel contains current loop adapters. Both channels are implemented using Intel's 8251 USART. They can be programmatically selected to perform a variety of I/O functions. Baud rate selection is accomplished progammatically through an Intel 8253 interval timer. The 8253 also serves as a real-time clock for the entire system. I/O activity through both serial channels is signaled to the system through a second 8259 interrupt controller, operating in a polled mode nested to the primary 8259.

IOC Interface — The remainder of system I/O activity takes place in the IOC. The IOC provides interface for the CRT, keyboard, and standard Intellec peripherals including printer, high speed paper tape reader/punch, and universal PROM programmer. The IOC contains its own independent microprocessor, also an 8080A-2. The CPU controls all I/O operations as well as supervising communications with the IPB. 8K bytes of ROM contain all I/O control firmware. 8K bytes of RAM are used for CRT screen refresh storage. These do not occupy space in Intellec Series II main memory since the IOC is a totally independent microcomputer subsystem.

Integral CRT

Display — The CRT is a 12-inch raster scan type monitor with a 50/60 Hz vertical scan rate and 15.5 kHz horizontal scan rate. Controls are provided for brightness and contrast adjustments. The interface to the CRT is provided through an Intel 8275 single chip programmable CRT controller. The master processor on the IPB transfers a character for display to the IOC, where it is stored in RAM. The CRT controller reads a line at a time into its line buffer through an Intel 8257 DMA controller and then feeds one character at a time to the character generator to produce the video signal. Timing for the CRT control is provided by an Intel 8253 interval timer. The screen display is formatted as 25 rows of 80 characters. The full set of ASCII characters are displayed, including lower case alphas.

Keyboard — The keyboard interfaces directly to the IOC processor via an 8-bit data bus. The keyboard contains an Intel UPI-41 Universal Peripheral Interface, which scans the keyboard, encodes the characters, and buffers the characters to provide N-key rollover. The keyboard itself is a high quality typewriter style keyboard containing the full ASCII character set. An upper/lower case switch allows the system to be used for document preparation. Cursor control keys are also provided.

Peripheral Interface

A UPI-41 Universal Peripheral Interface on the IOC board performs similar functions to the UPI-41 on the PIO board in the Model 210. It provides interface for other standard Intellec peripherals including a printer, high speed paper tape reader, high speed paper tape punch, and universal PROM programmer. Communication between the IPB and IOC is maintained over a separate 8-bit bidirectional data bus. Connectors for the four devices named above, as well as the two serial channels, are mounted directly on the IOC itself.

Control

User control is maintained through a front panel, consisting of a power switch and indicator, reset/boot switch, run/halt light, and eight interrupt switches and indicators. The front panel circuit board is attached directly to the IPB, allowing the eight interrupt switches to connect to the primary 8259, as well as to the Intellec Series II bus.

Diskette System

The Intellec Series II double density diskette system provides direct access bulk storage, intelligent controller, and two diskette drives. Each drive provides ½ million bytes of storage with a data transfer rate of 500,000 bits/second. The controller is implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controller provides an interface to the Intellec Series II system bus, as well as supporting up to four diskette drives. The diskette system records all data in soft sector format. The diskette system is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

Diskette Controller Boards — The diskette controller consists of two boards, the channel board and the interface board. These two PC boards reside in the Intellec Series II system chassis and constitute the diskette controller. The channel board receives, decodes and responds to channel commands from the 8080A-2 CPU in the Model 230. The interface board provides the diskette controller with a means of communication with the diskette drives and with the Intellec system bus. The interface board validates data during reads using a cyclic redundancy check (CRC) polynomial and generates CRC data during write operations. When the diskette controller requires access to Intellec system memory, the interface board requests and maintains DMA master control of the system bus, and generates the appropriate memory command. The interface board also acknowledges I/O commands as required by the Intellec bus. In addition to supporting a second set of double density drives, the diskette controller may co-reside with the Intel single density controller to allow up to 2.5 million bytes of on-line storage.

MULTIBUS Capability

All Intellec Series II models implement the industry standard MULTIBUS. MULTIBUS enables several bus masters, such as CPU and DMA devices, to share the bus and memory by operating at different priority levels. Resolution of bus exchanges is synchronized by a bus clock signal derived independently from processor clocks. Read/write transfers may take place at rates up to 5 MHz. The bus structure is suitable for use with any Intel microcomputer family.

SPECIFICATIONS

Host Processor (IPB)

RAM — 64K (system monitor occupies 62K through 64K)
ROM — 4K (2K in monitor, 2K in boot/diagnostic)

Diskette System Capacity (Basic Two Drives)

Unformatted
Per Disk: 6.2 megabits
Per Track: 82.0 kilobits

Formatted
Per Disk: 4.1 megabits
Per Track: 53.2 kilobits

Diskette Performance

Diskette System Transfer Rate — 500 kilobits/sec

Diskette System Access Time
Track-to-Track: 10 ms
Head Settling Time: 10 ms

Average Random Positioning Time — 260 ms

Rotational Speed — 360 rpm
Average Rotational Latency — 83 ms
Recording Mode — M^2FM

Physical Characteristics

Width — 17.37 in. (44.12 cm)
Height — 15.81 in. (40.16 cm)
Depth — 19.13 in. (48.59 cm)
Weight — 73 lb (33 kg)

Keyboard
Width — 17.37 in. (44.12 cm)
Height — 3.0 in. (7.62 cm)
Depth — 9.0 in. (22.86 cm)
Weight — 6 lb (3 kg)

Dual Drive Chassis
Width — 16.88 in. (42.88 cm)
Height — 12.08 in. (30.68 cm)
Depth — 19.0 in. (48.26 cm)
Weight — 64 lb (29 kg)

Electrical Characteristics

DC Power Supply

	Volts Supplied	Amps Supplied	Typical System Requirements
	+ 5 ± 5%	30	14.25
	+ 12 ± 5%	2.5	0.2
	− 12 ± 5%	0.3	0.05
	− 10 ± 5%	1.5	15
*	+ 15 ± 5%	1.5	1.3
*	+ 24 ± 5%	1.7	

*Not available on bus.

AC Requirements — 50/60 Hz, 115/230V AC

Environmental Characteristics

Operating Temperature — 0° to 35°C (95°F)

Equipment Supplied

Model 230 chassis
Integrated processor board (IPB)
I/O controller board (IOC)
32K RAM board
CRT and keyboard
Double density floppy disk controller (2 boards)
Dual drive floppy disk chassis and cables
2 floppy disk drives (512K byte capacity each)
ROM-resident system monitor
ISIS-II system diskette with MCS-80/MCS-85 macroassembler

Reference Manuals

9800558 — A Guide to Microcomputer Development Systems (SUPPLIED)
9800550 — Intellec Series II Installation and Service Guide (SUPPLIED)
9800306 — ISIS-II System User's Guide (SUPPLIED)
9800556 — Intellec Series II Hardware Reference Manual (SUPPLIED)
9800555 — Intellec Series II Hardware Reference Manual (SUPPLIED)
9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)
9800292 — ISIS-II 8080/8085 Assembler Operator's Manual (SUPPLIED)
9800605 — Intellec Series II Systems Monitor Source Listing (SUPPLIED)
9800554 — Intellec Series II Schematic Drawings (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-230	Intellec Series II Model 230 microcomputer development system (110V/60 Hz)
MDS-231	Intellec Series II Model 230 microcomputer development system (220V/50 Hz)

EXPANSION CHASSIS
INTELLEC SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Four expansion slots for Intellec Series II systems

Internal power supply

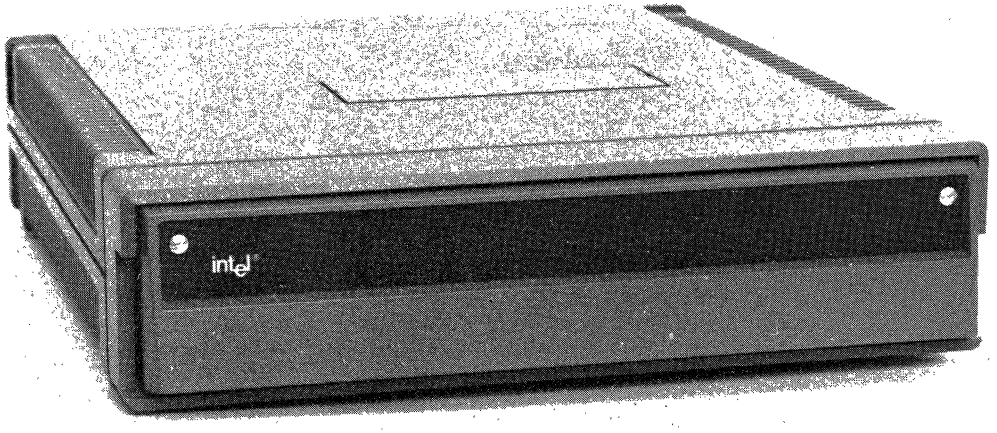
Snug fit beneath all Intellec Series II units

Cable connectable to main Intellec bus

Standard Intellec MULTIBUS with multi-processor and DMA capability

Compatible with standard Intellec/iSBC expansion modules

The Intellec Series II Expansion Chassis provides four expansion slots for use with Intellec Series II microcomputer development systems. With its own separate power supply, the expansion chassis may be fully loaded with any boards needed to expand a user's Intellec Series II system. With the addition of the expansion chassis, Intellec Series II Models 220 and 230 contain a total of ten slots, sufficient for any configuration Intellec Series II system. The Intellec Series II Expansion Chassis is a compact chassis with a four slot cardcage, power supply, fans, and cable assemblies. It is designed to fit under any Intellec Series II system, connect directly to the system bus through an opening in the top of the chassis, and provide additional slots for the system users. The power supply is linked directly to the main chassis power supply, allowing power to flow to both chassis when the main power is turned on.



SPECIFICATIONS

Physical Characteristics

Width — 17.37 in. (44.12 cm)
Height — 4.81 in. (17.22 cm)
Depth — 19.13 in. (48.59 cm)
Weight — 42 lb. (19 kg)

Electrical Characteristics

DC Power Supply

Volts Supplied	Amps Supplied	System Requirements
+ 5±5%	24	None
+12±5%	2.0	None
−12±5%	0.3	None
−10±5%	1.0	None

AC Requirements — 50-60 Hz, 115/230V AC

Environmental Characteristics

Operating Temperature — 0° to 35°C (95°F)

Equipment Supplied

Expansion chassis
Cables

Reference Manuals

9800550 — Intellec Series II Installation and Service Guide (SUPPLIED)

9800554 — Intellec Series II Schematic Drawings (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-201	Intellec Series II expansion chassis

MODEL 770 PRINTER
INTELLEC SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Provides low cost, hard copy printer for CRT-based systems

Prints original plus four copies

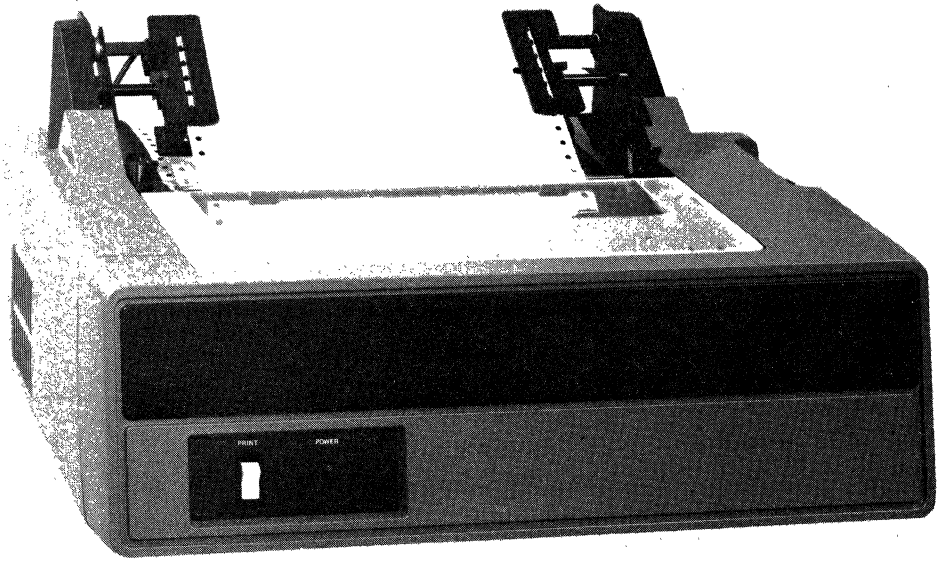
Prints 60 characters per seconds (21-90 lines per minute)

Offers 5 x 7 dot matrix character format

Provides for rear or bottom tractor feed

Provides adjustable line width from 80 to 132 columns on 8½ inch line

The Intellec Series II Microcomputer Development System Model 770 Printer is a low cost, hard copy printer designed for use with CRT-based Intellec Series II and Intellec microcomputer development systems. Unidirectional printing at 60 characters per second makes the Model 770 an ideal printer for microcomputer-based system designers with small to medium printing requirements. The 8½-inch line width may be filled with 80 to 132 characters by varying the character size. The printer uses standard fanfold paper through a tractor-feed mechanism to produce an original and up to four copies. Paper can be fed from either the bottom or the rear of the printer for versatility in any lab environment.



SPECIFICATIONS

Printing Method
Impact, character-by-character printing, one line character buffer.

Printing Rate
Characters — 60 cps
Full Lines — 21 @ 80 characters/line, 90 @ 20 characters/line

Transmission Rate
Parallel — Up to 75,000 cps

Character Structure
5 x 7 dot matrix, 10 point type equivalent

Code
USASCII — 64 characters printed

Switch Controls
On-Off

Indicators
Paper Out

Format
80 to 132 characters per line, variable.
10 to 165 characters per inch, operator adjustable.
6 lines per inch.

Paper Feed
Tractor Feed — 5.5 ips slew

Paper
Standard sprocketed paper, 8½ in. to 9½ in. paper width

Number of Copies
Original plus up to four carbon copies

Physical Characteristics
Width — 24.5 in. (62.2 cm)
Height — 7.0 in. (17.8 cm)
Depth — 18.0 in. (45.7 cm)
Weight — 60 lb (27 kg)

Electrical Characteristics
50-60 Hz, 110/230V AC ± 10%

Environmental Characteristics
Temperature — Operating: – 40° to 100°F (5° to 40°C), Storage: – 40° to 160°F (– 40° to 50°C)
Humidity — Operating: 5% to 90% (no condensation), Storage: 0% to 95% (no condensation)

ORDERING INFORMATION

Part Number	Description
MDS-770	60 CPS printer (110V/60 Hz)
MDS-771	60 CPS printer (220V/50 Hz)

INTELLEC PRINTER

Provides listing of hard copy output at 55 lines per minute

Switch selectable to 80 or 132 characters per 8½-inch line

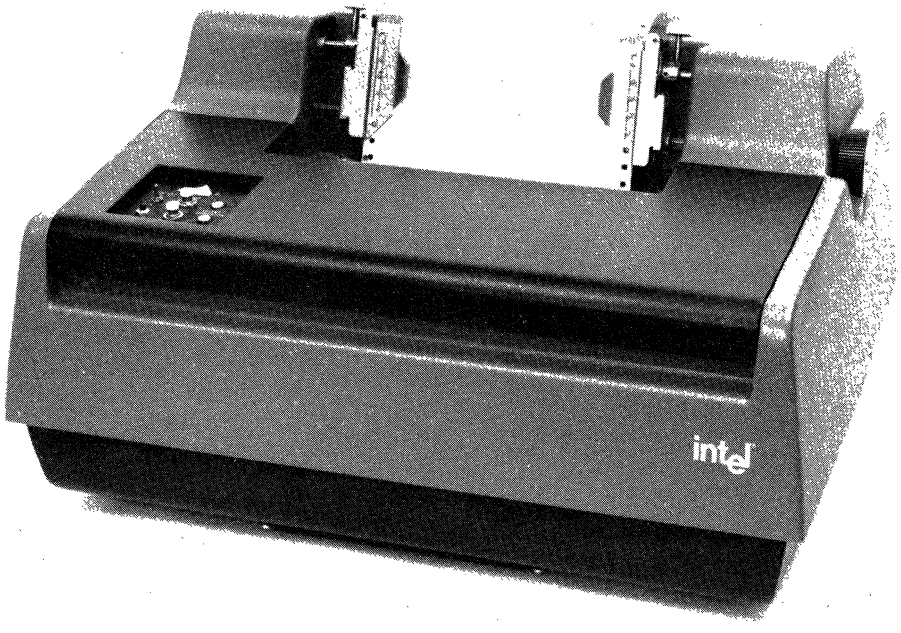
Employs 5 x 7 dot matrix with standard 2-channel, vertical control format

Prints up to four copies on standard 8½-inch fanfold paper

Provides automatic on-off motor switch for quiet operation

Provides optional finished metal stand and paper takeup tray

The Intellec Printer provides hard copy listings at 10 to 16 times the speed of a teleprinter. The automatic on-off motor control allows the user to maintain a low noise environment and yet send information to the printer from the Intellec system console without additional manipulation of line printer switches. The user may select a column width of 80 characters per line (10 characters per inch) or 132 characters per line (16.5 characters per inch) either manually or under program control. Top of page spacing capability is available under user programmable format control. The printer uses standard 8½-inch fanfold paper and can produce up to four carbon copies along with the original. Paper may be fed either from the bottom or from the rear of the printer for versatility in any lab environment.



SPECIFICATIONS

Printing Method
Impact, character-by-character printing, one line character buffer

Printing Rate
Characters — 100 or 165 cps
Full Lines — 55 lines per minute (80- or 132-character line)

Transmission Rate
Parallel — Up to 75,000 characters per second

Data Input
Parallel

Character Structure
5 x 7 dot matrix, 10-point type equivalent

Code
USASCII — 64 characters printed

Switch Controls
On/off
Select
Forms override
Normal/condensed top of form

Indicators
Paper out
Select

Manual Controls
Form thickness
Paper advance knob

Buffer
One line character buffer

Format
80 or 132 characters maximum per line, 6 lines per inch

Paper Feed
Sprocket fed, 4 I.P.S. slew, adjustable to 9½-in. width

Paper
Standard sprocketed paper

Number of Copies
Original and up to four carbon copies

Warranty
The MDS-PRN is warranted against defects in materials and workmanship for a period of one (1) year on mechanical parts, 90 days on electrical parts, and 45 days on labor.

Physical Characteristics
Width — 23.25 in. (59.1 cm)
Height — 12.75 in. (32.4 cm)
Depth — 18.75 in. (47.6 cm)
Weight — 66 lb (30.2 kg)

Electrical Characteristics
115V AC ± 10%, 60 Hz (or 230V AC ± 10%, 50 Hz as option)

Environmental Characteristics
Temperature — 40° to 100°F, operating; – 40° to 160°F, storage
Humidity —5% to 90% (no condensation) operating; 0% to 95% (no condensation) storage

Optional Equipment
MDS-STD finished metal stand and paper tray

Reference Manuals
None

ORDERING INFORMATION

Part No.	Description
MDS-PRN	Printer unit
MDS-STD	Stand and paper tray

MCS-48 DISKETTE-BASED SOFTWARE SUPPORT PACKAGE

Extends Intellec microcomputer development system to support MCS-48 development

Takes advantage of powerful ISIS-II file handling and storage capabilities

MCS-48 assembler provides conditional assembly and macro capability

Provides assembler output in standard Intel hex format

The MCS-48 Diskette-Based Software Support Package is provided with the Intel ISIS-II system diskette and contains both the MCS-48 assembler and the diskette version of the universal PROM mapper. The assembler translates symbolic 8048 assembly language instructions into the appropriate machine operation codes, and provides both conditional and macroassembler programming. Output may be loaded either to an ICE-48 module for debugging or into an Intellec microcomputer development system for 8748 PROM programming using the universal PROM programmer.

FUNCTIONAL DESCRIPTION

The MCS-48, a software support assembler package, is provided with the ISIS-II system diskette and contains both the MCS-48 assembler and the diskette version of the universal PROM mapper. The MCS-48 assembler translates symbolic 8048 assembly language instructions into the appropriate machine operation codes. The ability to refer to program addresses with symbolic names eliminates the errors of hand translation and makes it easier to modify programs when adding or deleting instructions. Conditional assembly permits the programmer to specify which portions of the master source document should be included or deleted in variations on a basic system design, such as the code required to handle optional external devices. Macro capability allows the programmer use of a single label to define a routine. The MCS-48 assembler will assemble the code required by the reserved routine whenever the macro label is inserted in the text. Output from the assembler is in standard Intel hex format. It may be either loaded directly to an in-circuit emulator (ICE-48) module for integrated hardware/software debugging, or loaded into an Intellec development system for 8748 PROM programming using the universal PROM programmer. A sample assembly listing is shown in Table 1.

```
ISIS-II 8048 MACROASSEMBLER, V1.0                                    PAGE 1

LOC  OBJ                    SEQ          SOURCE STATEMENT

                             1   ;DECIMAL ADDITION ROUTINE  ADD BCD NUMBER
                             2   ;AT LOCATION 'BETA' TO BCD NUMBER AT 'ALPHA' WITH
                             3   ;RESULT IN 'ALPHA'  LENGTH OF NUMBER IS 'COUNT' DIGIT
                             4   ;PAIRS  (ASSUME BOTH BETA AND ALPHA ARE SAME LENGTH
                             5   ;AND HAVE EVEN NUMBER OF DIGITS OR MSD IS 0 IF
                             6   ;ODD)
                             7   INIT     MACRO    AUGND,ADDND,CNT
                             8            MOV      R0, #AUGND
                             9   L1       MOV      R1, #ADDND
                            10            MOV      R2, #CNT
                            11            ENDM
                            12   .
0001E                       13   ALPHA    EQU      30
0028                        14   BETA     EQU      40
0032                        15   COUNT    EQU      5
0100                        16            ORG      100H
                            17            INIT     ALPHA, BETA, COUNT
0100  B81E                  18+           MOV      R0, #ALPHA
0102  B928                  19+L1         MOV      R1, #BETA
0104  BA32                  20+           MOV      R2, #COUNT
0106  97                    21            CLR      C
0107  F0                    22   LP       MOV      A, @R0
0108  71                    23            ADDC     A, @R1
0109  57                    24            DA       A
010A  A1                    25            MOV      @R0, A
010B  18                    26            INC      R0
010C  19                    27            INC      R1
010D  EA07                  28            DJNZ     R2, LP
                                          END

USER SYMBOLS
ALPHA  0001E    BETA 0028    COUNT 0005    LP 0107
L1     0102

ASSEMBLY COMPLETE, NO ERRORS


ISIS-II ASSEMBLER SYMBOL CROSS REFERENCE, V1.0                       PAGE 1

SYMBOL CROSS REFERENCE

ALPHA  13#  17
BETA   14#  17
COUNT  15#  17
INIT    7#  17
L1     19#
LP     22#  28
```

Table 1. Sample MCS-48 Diskette-Based Assembly Listing

SPECIFICATIONS

Operating Environment

Required Hardware

Intellec microcomputer development system
System console
Intellec diskette operating system
32K RAM (absoluteassembler)
48K RAM (macroassembler)

Optional Hardware

Universal PROM programmer

Shipping Media

Diskette

Reference Manuals

9800255 — MCS-48/UPI-41 Assembly Language Programming Manual (SUPPLIED)

9800236 — Universal PROM Mapper Operator's Manual (SUPPLIED)

9800306 — ISIS-II User's Guide (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Product Code	Description
MDS-D48	Diskette-based assembler for MCS-48 family of microprocessors

PL/M-80
HIGH LEVEL PROGRAMMING LANGUAGE
INTELLEC RESIDENT COMPILER

Provides resident operation on Intellec Microcomputer Development System and Intellec Series II microcomputer development systems

Produces relocatable and linkable object code

Sophisticated code optimization reduces application memory requirements

Speeds project completion with increased programmer productivity

Cuts software development and maintenance costs

Improves product reliability with simplified language and consequent error reduction

Eases enhancement as system capabilities expand

The PL/M-80 High Level Programming Language Intellec Resident Compiler is an advanced, high level programming language for Intel 8080 and 8085 microprocessors, iSBC-80 OEM computer systems, and Intellec microcomputer development systems. PL/M has been substantially enhanced since its introduction in 1973 and has become one of the most effective and powerful microprocessor systems implementation tools available. It is easy to learn, facilitates rapid program development and debugging, and significantly reduces maintenance costs. PL/M is an algorithmic language in which program statements naturally express the algorithm to be programmed, thus freeing programmers to concentrate on system development rather than assembly language details (such as register allocation, meanings of assembler mnemonics, etc.). The PL/M compiler efficiently converts free-form PL/M programs into equivalent 8080/8085 instructions. Substantially fewer PL/M statements are necessary for a given application than would be using assembly language or machine code. Since PL/M programs are problem oriented and thus more compact, programming in PL/M results in a high degree of productivity during development efforts, resulting in significant cost reduction in software development and maintenance for the user.

MPU SYSTEM

FUNCTIONAL DESCRIPTION

The PL/M compiler is an efficient multiphase compiler that accepts source programs, translates them into object code, and produces requested listings. After compilation, the object program may be first linked to other modules, then located to a specific area of memory, and finally executed. The diagram shown in Figure 1 illustrates a program development cycle where the program consists of three modules: PL/M, FORTRAN, and assembly language. A typical PL/M compiler procedure is shown in Table 1.

Features

Major features of the Intel PL/M-80 compiler and programming language include:

Resident Operation — on Intellec microcomputer development systems eliminates the need for a large in-house computer or costly timesharing system.

Object Code Generation — of relocatable and linkable object codes permits PL/M program development and debugging in small modules, which may be easily linked with other modules and/or library routines to form a complete application.

Extensive Code Optimization — including compile time arithmetic, constant subscript resolution, and common subexpression elimination, results in generation of short, efficient CPU instruction sequences.

Symbolic Debugging — fully supported in the PL/M compiler and ICE-85 in-circuit emulators.

Compile Time Options — includes general listing format commands, symbol table listing, cross reference listing, and "innerlist" of generated assembly language instructions.

Block Structure — aids in utilization of structured programming techniques.

Access — provided by high level PL/M statements to hardware resources (interrupt systems, absolute addresses, CPU input/output ports).

Data Definition — enables complex data structures to be defined at a high level.

Re-entrant Procedures — may be specified as a user option.

Benefits

PL/M is designed to be an efficient, cost-effective solution to the special requirements of microcomputer software development as illustrated by the following benefits of PL/M use:

Low Learning Effort — even for the novice programmer, because PL/M is easy to learn.

Earlier Project Completion — on critical projects, because PL/M substantially increases programmmer productivity while reducing program development time.

Lower Development Cost — because increased programmer productivity requiring less programming resources for a given function translates into lower software development costs.

Increased Reliability — because of PL/M's use of simple statements in the program algorithm, which are easier to correct and thus substantially reduce the risk of costly errors in systems that have already reached full production status.

Easier Enhancement and Maintenance — because programs written in PL/M are easier to read and easier to understand than assembly language, and thus are easier to enhance and maintain as system capabilities expand and future products are developed.

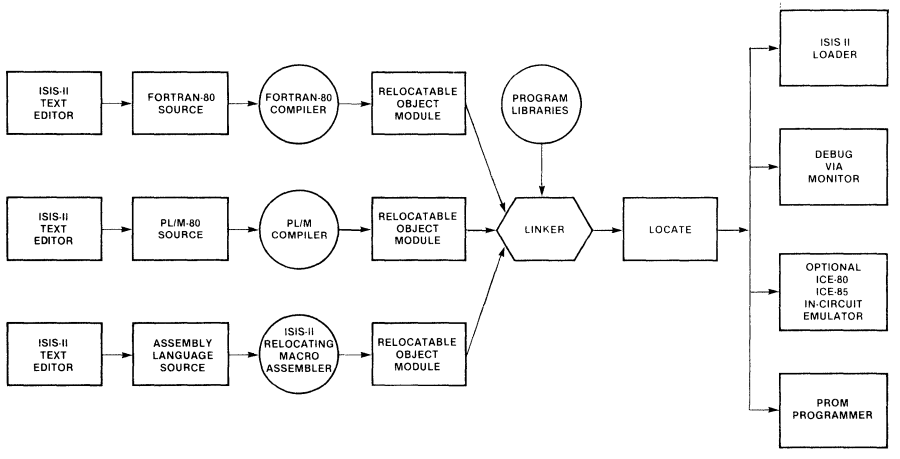


Figure 1. Program Development Cycle Block Diagram

Simpler Project Development — because the Intellec microcomputer development system with resident PL/M-80 is all that is needed for developing and debugging software for 8080 and 8085 microcomputers, and the use of expensive (and remote) timesharing or large computers is consequently not required.

```
                                    $OBJECT(:F1:FACT.OB2)
                                    $DEBUG
                                    $XREF
                                    $TITLE('FACTORIAL GENERATOR — PROCEDURE')
                                    $PAGEWIDTH(80)

 1                                  FACT:
                                    DO;

 2     1                            DECLARE NUMCH BYTE PUBLIC;

 3     1                            FACTORIAL: PROCEDURE (NUM,PTR) PUBLIC;
 4     2                                DECLARE NUM BYTE, PTR ADDRESS;
 5     2                                DECLARE DIGITS BASED PTR (161) BYTE;
 6     2                                DECLARE (I,C,M) BYTE;

 7     2                                NUMCH = 1; DIGITS(1) = 1;
 9     2                                DO M = 1 TO NUM;
10     3                                    C = 0;
11     3                                    DO I = 1 TO NUMCH;
12     4                                        DIGITS(I) = DIGITS(I)*M + C;
13     4                                        C = DIGITS(I)/10;
14     4                                        DIGITS(I) = DIGITS(I) — 10*C;
15     4                                    END;

16     3                                    IF C<>0 THEN
17     3                                    DO;
18     4                                        NUMCH = NUMCH + 1; DIGITS(NUMCH) = C;
20     4                                        C = DIGITS(NUMCH)/10;
21     4                                        DIGITS(NUMCH) = DIGITS(NUMCH) — 10*C;
22     4                                    END
                                        END;

24     2                            END FACTORIAL;

25     1                            END;
```

Table 1. PL/M-80 Compiler Sample Factorial Generator Procedure

SPECIFICATIONS

Operating Environment

Required Hardware

Intellec microcomputer development system
65K bytes of memory
Dual diskette drives
System console — teletype

Optional Hardware

CRT as system console
Line printer

Required Software — ISIS-II diskette operating system

Shipping Media

Diskette

Reference Manuals

980026 — PL/M-80 Programming Manual (SUPPLIED)

9800300 — ISIS-II PL/M-80 Compiler Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Product Code	Description
MDS-PLM	High level language compiler

MDS-311
8086 SOFTWARE DEVELOPMENT PACKAGE

PL/M-86 high level programming language

ASM86 assembler for 8086 assembly language programming

CONV86 converter for conversion of 8080/8085 assembly language source code to 8086 assembly language source code

LINK86, LOC86 and QRL86 link and relocation utilities

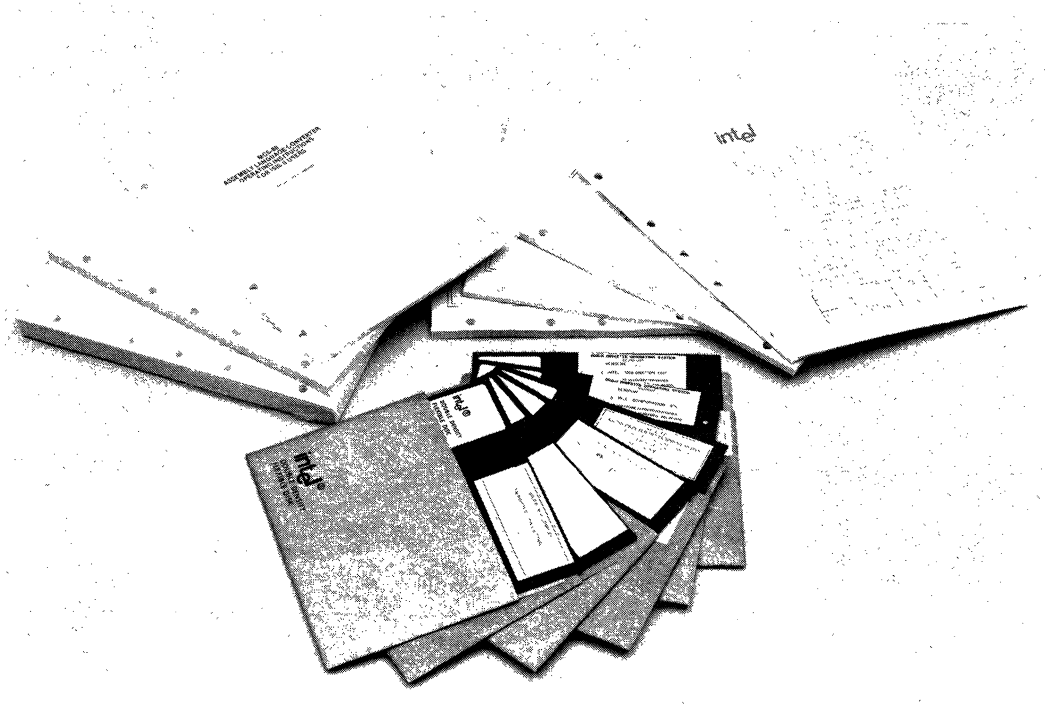
OH86 object-to-hexadecimal converter

LIB86 library manager

The 8086 software development package provides a set of software development tools for the 8086 microprocessor and iSBC 86/12 single board computer. The package operates under the ISIS-II operating system on Intellec® Microcomputer Development Systems—Model 800 or Series II—thus minimizing requirements for additional hardware or training for Intel Microcomputer Development System users.

The package permits 8080/8085 users to efficiently convert existing programs into 8086 object code from either 8080/8085 assembly language source code or PL/M-80 source code.

For the new Intel Microcomputer Development System user, the package operating on an Intellec Model 230 Microcomputer Development System provides total 8086 software development capability.



MPU SYSTEM

PL/M-86 HIGH LEVEL PROGRAMMING LANGUAGE

Sophisticated new compiler design allows user to achieve maximum benefits of 8086 capabilities

Language is upward compatible from PL/M-80, assuring MCS™-80/85 design portability

Supports 16-bit signed integer and 32-bit floating point arithmetic

Produces relocatable and linkable object code

Supports full extended addressing features of the 8086 microprocessor

Sophisticated code optimization assures efficient code generation and minimum application memory utilization

Like its counterpart for MCS™-80/85 program development, PL/M-86 is an advanced structured high level programming language. PL/M-86 is a new compiler created specifically for performing software development for the Intel® 8086 Microprocessor.

PL/M-86 has significant new capabilities over PL/M-80 that take advantage of the new facilities provided by the 8086 microprocessor, yet the PL/M-86 language remains downward compatible with PL/M-80.

With the exception of interrupts, hardware flags, and time-critical code sequences, PL/M-80 programs may be recompiled under PL/M-86 with little or no conversion required. PL/M-86, like PL/M-80, is easy to learn, facilitates rapid program development, and reduces program maintenance costs.

PL/M is a powerful, structured high level algorithmic language in which program statements can naturally express the program algorithm. This frees the programmer to concentrate on the system implementation without concern for burdensome details of assembly language programming (such as register allocation, meanings of assembler mnemonics, etc.).

The PL/M-86 compiler efficiently converts free-form PL/M language statements into equivalent 8086 machine instructions. Substantially fewer PL/M statements are necessary for a given application that if it were programmed at the assembly language or machine code level.

Since PL/M programs are implementation problem oriented and more compact, use of PL/M results in a high degree of engineering productivity during project development. This translates into significant reductions in initial software development and follow-on maintenance costs for the user.

FEATURES

Major features of the Intel PL/M-86 compiler and programming language include:

- **Supports Five Data Types**
  - — Byte: 8-bit unsigned number
  - — Word: 16-bit unsigned number
  - — Integer: 16-bit signed number
  - — Real: 32-bit floating point number
  - — Pointer: 16-bit or 32-bit memory address indicator
- **Two Data Structuring Facilities**
  - — Array: Indexed list of same type data elements
  - — Structure: Named collection of same or different type data elements
  - — Combinations of Each: Arrays of structures or structures of arrays
- **Block Structure**
  - — Permits use of structured programming techniques
- **Relocatable and Linkable Object Code**
  - — Permits PL/M-86 programs to be developed and debugged in small modules. These modules can be easily linked with other modules and/or library routines to form a complete application system.

- **Built-In String Handling Facilities**
  - — Operates on byte strings or word strings
  - — Six Functions: MOVE, COMPARE, TRANSLATE, SEARCH, SKIP, and SET
- **Automatic Support for 8086 Extended Addressing**
  - — Three compiler options offer a separate model of computation for programs from 128K bytes to 1-Megabyte in size
  - — Language transparency for extended addressing
- **Support for ICE-86™ and Symbolic Debugging**
  - — Debug option for inclusion of symbol table in object modules for In-Circuit Emulation with symbolic debugging
- **Numerous Compiler Options**
  - — A host of 26 compiler options including:
    - Conditional compilation
    - Included file or copy facility
    - Two levels of optimization
    - Intra-module and inter-module cross reference
    - Arbitrary placement of compiler and user files on any available combination of disk drives
- **Reentrant and Interrupt Procedures**
  - — May be specified as user options

BENEFITS

PL/M-86 is designed to be an efficient, cost-effective solution to the special requirements of 8086 Microcomputer Software Development, as illustrated by the following benefits of PL/M-86 use:

- **Low Learning Effort** — PL/M-86 is easy to learn and to use, even for the novice programmer.
- **Earlier Project Completion** — Critical projects are completed much earlier than otherwise possible because PL/M-86, a structured high-level language, increases programmer productivity.
- **Lower Development Cost** — Increases in programmer productivity translate immediately into lower software development costs because less programming resources are required for a given programmed function.
- **Increased Reliability** — PL/M-86 is designed to aid in the development of reliable software (PL/M-86 programs are simple statements of the program algorithm). This substantially reduces the risk of costly correction of errors in systems that have already reached full production status, as the more simply stated the program is, the more likely it is to perform its intended function.
- **Easier Enhancements and Maintenance** — Programs written in PL/M tend to be self-documenting, thus easier to read and understand. This means it is easier to enhance and maintain PL/M programs as the system capabilities expand and future products are developed.
- **Simpler Project Development** — The Intellec® Development Systems offer a cost-effective hardware base for the development of 8086 designs. PL/M-86 and other elements of ISIS-II and the 8086 Software Development Package are all that is needed for development of software for the 8086 microcomputer and iSBC 86/12 single board computer. This further reduces development time and costs because expensive (and remote) time sharing of large computers is not required. Present users of Intel Intellec® Development Systems can begin to develop 8086 designs without expensive hardware reinvestment or costly retraining.

SAMPLE PROGRAM

```
STATISTICS: DO;

/*The procedure in this module computes the mean and variance of an array of data, X, of length N + 1, according to
the method of Kahan and  Parlett  (University of California, Berkeley, Memo no. UCB/ERL M77/21.*/

STAT: PROCEDURE(X$PTR,N,MEAN$PTR,VARIANCE$PTR) PUBLIC;

DECLARE (X$PTR,MEAN$PTR,VARIANCE$PTR) POINTER,
          X BASED X$PTR (1) REAL,
          N INTEGER,
          MEAN BASED MEAN$PTR REAL,
          VARIANCE BASED VARIANCE$PTR REAL,
          (M,Q,DIFF) REAL,
          I INTEGER;

M = X(0);
Q = 0.0;

DO  I = 1 TO N;
    DIFF = X(I) - M;
    M = M + DIFF/FLOAT(I + 1);
    Q = Q + DIFF*DIFF*FLOAT(I)/FLOAT(I + 1);
END;

MEAN = M;
VARIANCE = Q/FLOAT(N);

END STAT;

END STATISTICS;
```

ASM86 ASSEMBLER

A new assembler that encourages well-designed and well-structured programs

ASM86 is highly mnemonic and compact, with most mnemonics representing several distinct machine instructions

ASM86 will generate optimal code

Powerful "EQU" (equate) facility allows complex expressions to be represented as a single symbol

Enhanced data handling capabilities

Fully detailed set of error messages

The 8086 assembly language is "strongly typed". This means it performs extensive checks on the usage of variables and labels. The assembler uses the attributes which are derived explicitly when a variable or label is first declared, then makes sure that each use of a symbol in later instructions conforms to the usage defined for that symbol when it was declared.

Compared to earlier assemblers, ASM86 supports substantially improved flexibility in data definition and manipulation:

-RECORDS
-PROCEDURES
-ARRAYS

Its capabilities allow very sophisticated goals and significantly simplified coding to be achieved with a straightforward use of the language.

For example a data RECORD smaller than a word may be defined as a collection of named bit-fields and operators for manipulating these subfields are automatically defined when the record is declared. Bit-fields within a record may be referenced directly by name.

Powerful string manipulation instructions permit direct transfers to or from memory or the accumulator. They can be prefixed with a repeat operator for repetitive execution with a count-down and a condition test. These operations automatically decrement or increment the relevant indexes to memory, depending on the direction flag.

The assembler fully supports the 8086 addressing modes by providing for complex address expressions involving base and index registers and field offsets. A powerful EQU facility allows the use of simplified synonyms for complicated expressions which may occur throughout a module.

The 8086 assembly language includes approximately 100 instruction mnemonics. From these few mnemonics, the assembler can generate over 3,800 distinct machine instructions. These instructions are differentiated by the assembler's ability to evaluate the "TYPE" of the operands to the instruction and then generate the proper machine instruction. ASM86 will generate the shortest machine instruction possible given no forward referencing or given explicit information as to the characteristics of the forward referenced symbol.

ASM86 provides a detailed set of error messages which may appear both in the regular list file and the error print file. As a debugging feature, the list file may include a detailed listing of the user symbol table.

ASM86 allows the user power and flexibility, and is fully compatible with LINK86, LOC86, QRL86 and LIB86.The ASM86 operator's manual includes details on linking ASM86 programs with programs written in PL/M-86.

ASM86 implements directives which reflect the high level orientation of the 8086 architecture.

ASM86 assembles code significantly faster than ASM80 V2.0.

CONV 86

MCS-80/85 to MCS-86 ASSEMBLY LANGUAGE CONVERTER UTILITY PROGRAM

Translates 8080/8085 Assembly Language Source Code to 8086 Assembly Language Source Code

Provides a fast and accurate means to convert 8080/8085 programs to the 8086, facilitating program portability.

Automatically generates proper ASM-86 directives to set up a "virtual 8080" environment that is compatible with PL/M-86.

In support of Intel's commitment to software portability, CONV86 is offered as a tool to move 8080/8085 programs to the 8086. A comprehensive manual, "MCS-86 Assembly Language Converter Operating Instructions for ISIS-II Users" (9800642), covers the entire conversion process. Detailed methodology of the conversion process is fully described therein.

CONV86 will accept as input an error-free 8080/8085 assembly-language source file and optional controls, and produce as output, optional PRINT and OUTPUT files.

The PRINT file is a formatted copy of the 8080/8085 source and 8086 source file with embedded caution messages.

The OUTPUT file is an 8086 source file.

CONV86 issues a caution message when it detects a potential problem in the converted 8086 code.

A transliteration of the 8080/8085 programs occurs, with each 8080/8085 construct mapped to its exact 8086 counterpart:

—Registers
—Condition flags
—Instructions
—Operands
—Assembler directives
—Assembler control lines

Because CONV86 is a transliteration process, there is the possibility of as much as a 15%-20% code expansion over the 8080/8085 code. For compactness and efficiency it is recommended that critical portions of programs be re-coded in 8086 assembly language.

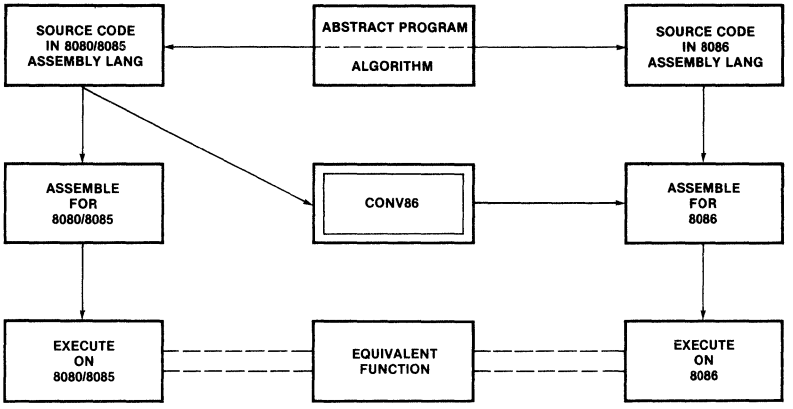
Also, as a consequence of the transliteration, some manual editing may be required for converting instruction sequences dependent on:

-instruction length, timing, or encoding
-interrupt processing
-PL/M parameter passing conventions

} mechanical editing procedures for these are suggested in the converter manual.

The set directive, macro definitions, macro calls, and conditional assembly directives are not supported by Version V1.0 of the 8086 Assembler. Appendix F of the MCS-86 Assembly Language Converter Operating Instructions for ISIS-II Users contains instructions for converting 8080/8085 programs containing these features, by using the macro expansion printed in the 8080/8085 assembler listing.

The accompanying diagram illustrates the flow of the conversion process. Initially, the abstract program may be represented in 8080/8085 or 8086 assembly language to execute on that respective target machine. The conversion process is porting a source destined for the 8080/8085 to the 8086 via CONV86.



PORTING 8080/8085 SOURCE CODE TO THE 8086

LINK86

Automatic combination of separately compiled or assembled 8086 programs into a relocatable module

Automatic selection of required modules from specified libraries to satisfy symbolic references

Extensive debug symbol manipulation; the user is allowed the choices of line number and local symbol deletion and may selectively purge definitions of public symbols

Automatic generation of a summary map giving results of the LINK86 process

Abbreviated control syntax

Relocatable modules may be merged into a single module suitable for inclusion in a library

Supports "incremental" linking

LINK86 combines object modules specified in the LINK86 input list into a single output module. LINK86 combines segments from the input modules according to the order in which the modules are listed.

Support for incremental linking is provided since an output module produced by LINK86 can be an input to another link. At each stage in the incremental linking process, unneeded public symbols may be purged.

LINK86 will link any valid set of input modules without any controls. However, controls are available to control the output of diagnostic information in the LINK86 process and to control the content of the output module.

LINK86 allows the user to create a large program as the combination of several smaller, separately compiled modules. After development and debugging of these component modules the user can link them together, locate them using LOC86, and enter final testing with much of the work accomplished.

LOC86

Automatic and independent relocation of segments. Segments may be relocated to best match users memory configuration

Extensive debug symbol manipulation, allowing line numbers, local symbols, and public symbols to be purged and listed selectively

Automatic generation of a summary map giving starting address, segment addresses and lengths, and debug symbols and their addresses

Extensive capability to manipulate the order and placement of segments in 8086 memory

Abbreviated control syntax

Relocatability allows the programmer to code programs or sections of programs without having to know the final arrangement of the object code in memory.

LOC86 converts relative addresses in an input module to absolute addresses. LOC86 orders the segments in the input module and assigns absolute addresses to the segments. The sequence in which the segments in the input module are assigned absolute addresses is determined by their order in the input module and the controls supplied with the command.

LOC86 will relocate any valid input module without any controls. However, controls are available to control the output of diagnostic information in the LOC86 process, to control the content of the output module, or both.

The program you are developing will almost certainly use some mix of random access memory (RAM), read-only memory (ROM), and/or programmable read-only memory (PROM). Therefore, the location of your program affects both cost and performance in your application. The relocation feature allows you to develop your program on the Intellec development system and then simply relocate the object code to suit your application.

QRL86

Combination linkage and relocation tool

Combines object modules and converts relative addresses to absolute addresses in a single step

QRL86 can be used for quick turnaround during development, whereas the extra capabilities of LINK86 and LOC86 may be needed to finalize the product at the end of development

QRL86 purges unsatisfied externals while LINK86 and LOC86 allow them to be kept for future processing

QRL86 provides 25% faster turnaround than LINK86 and LOC86, but does not have as wide a range of controls:

- **Incremental linking**
- **Selective purge of publics**

QRL86 controls give the capability of changing the order and placement of segments in memory

QRL86 combines object modules and converts relative addresses to absolute addresses in a single step. The segment is the fundamental unit with which linkage and relocation functions work. First, segments are combined, then absolute addresses are assigned to segments. Addresses that are referenced relative to the beginning of a segment are translated to absolute memory address references.

The modules to be combined are specified in a list in the QRL86 command. In general, QRL86 will link and locate any set of valid input modules without any controls. However, controls are available for you to modify the manner in which QRL86 links and locates and to control the output of information in the process.

OH86

OH86 command converts an 8086 absolute object module to symbolic hexadecimal format

Facilitates preparing a file for later loading by a symbolic hexadecimal loader, such as the iSBC Monitor or Universal PROM Mapper

Converts an absolute module to a more readable format that can be displayed on a CRT or printed for debugging

The OH86 command converts an 8086 absolute object module to the hexadecimal format. This conversion may be necessary to format a module for later loading by a hexadecimal loader such as the iSBC 86/12 monitor or Univeral Prom Mapper. The conversion may also be made to put the module in a more readable format that can be displayed or printed.

The module to be converted must be in absolute format; the output from the QRL86 and LOC86 is in absolute format.

LIB86

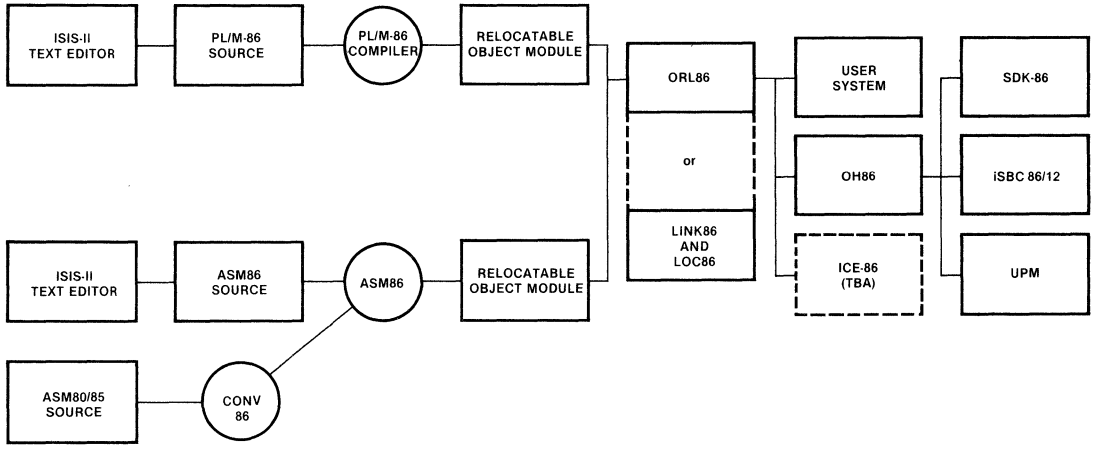
LIB86 is a library manager program which allows you to:

- **Create specially formatted files to contain libraries of object modules**
- **Maintain these libraries by adding or deleting modules**
- **Print a listing of the modules and public symbols in a library file**

Libraries can be used as input to QRL86 or LINK86 which will automatically link modules from the library that satisfy external references in the modules being linked

Libraries aid in the job of building programs. The library manager program, LIB86, creates and maintains files containing object modules. The operation of LIB86 is controlled by commands to indicate which operation LIB86 is to perform. The commands are:

CREATE — creates an empty library file
ADD — adds object modules to a library file
DELETE — deletes modules from a library file
LIST — lists the module directory of library files
EXIT — terminates the LIB86 program and returns control to ISIS-II



MPU SYSTEM

SPECIFICATIONS

Operating Environment

Required Hardware

Intellec® Microcomputer Development System

— MDS-800, MDS-888
— Series II

64K Bytes of RAM Memory

Dual Diskette Drives

— Single or Double* Density

System Console

— CRT or Hardcopy Interactive Device

Optional Hardware

Universal PROM Programmer
Line Printer*
ICE-86™*

Required Software

ISIS-II Diskette Operating System

— Single or Double* Density

*Recommended

Documentation Package

PL/M-86 Programming Manual (9800466)
ISIS-II PL/M-86 Compiler Operator's Manual (9800478)
MCS™-86 User's Manual (9800694)
MCS-86 Software Development Utilities Operating Instructions for ISIS-II Users (9800639)
MCS-86 Assembly Language Reference Manual (9800640)
MCS-86 Assembler Operating Instructions for ISIS-II Users (9800641)
MCS-86 Assembly Language Converter Operating Instructions for ISIS-II Users (9800642)
MCS-86 Absolute Object File Formats (9800821)
Universal PROM Programmer User's Manual (9800819A)

Flexible Diskettes

— Single and Double* Density

FORTRAN-80
8080/8085 ANS FORTRAN 77
INTELLEC® RESIDENT COMPILER

Meets and exceeds ANS FORTRAN 77 Subset Language Specification

Supports Intel Floating Point Standard with either the floating point support library or the iSBC-310 High Speed Mathematics Board

Resident operation on Intellec® Microcomputer Development System and Intellec® Series II Microcomputer Development System

Supports full symbolic debugging with ICE-80™ and ICE-85™

Produces relocatable and linkable object code compatible with resident PL/M-80 and 8080/8085 Macro Assembler

Full FORTRAN 77 language I/O support or optional RMX-80 run-time library

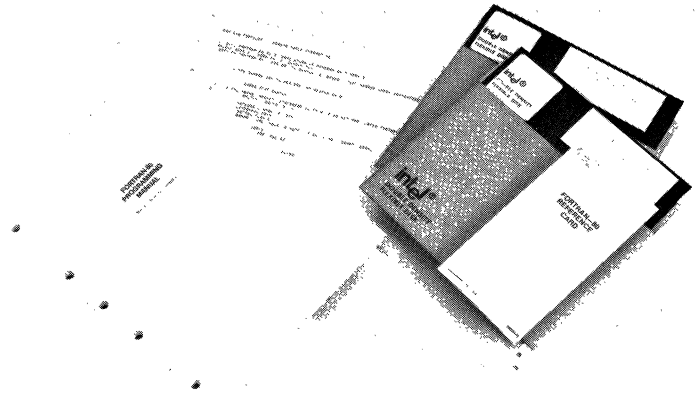
Well defined I/O interface for configuration with user-supplied drivers

Sophisticated code optimization insures efficient program implementation

FORTRAN-80 is a computer industry-standard, high-level programming language and compiler that translates FORTRAN statements into relocatable object modules. When the object modules are linked together and located into absolute program modules, they are suitable for execution on Intel® 8080/8085 Microprocessors, iSBC-80 OEM Computer Systems, and Intellec® Microcomputer Development Systems. FORTRAN-80 meets and exceeds the ANS FORTRAN 77 Language Subset Specification[1]. The compiler operates on the Intellec Microcomputer Development System under the ISIS-II Disk Operating Systems and produces efficient relocatable object modules that are compatible for linkage with PL/M-80 and 8080/8085 Macro Assembler modules.

The ANS FORTRAN 77 language specification offers many powerful extensions to the FORTRAN language that are especially well suited to Intel® 8080/8085 Microprocessor software development. Because FORTRAN-80 conforms to the ANS FORTRAN 77 standard, the user is assured of compatibility with existing FORTRAN software that meets the standard as well as a guarantee of upward compatibility to other computer systems supporting an ANS FORTRAN 77 Compiler.

[1] ANSI X3J3/90



MPU SYSTEM

FORTRAN-80 LANGUAGE FEATURES

Major ANS FORTRAN 77 features supported by the Intel® FORTRAN-80 Programming Language include:

- Structured Programming is supported with the IF ... THEN ... ELSE IF ... ELSE ... END IF constructs.
- CHARACTER data type permits alphanumeric data to be handled as strings rather than characters stored in array elements.
- Full I/O capabilities include:
  - — Sequential and Direct Access files
  - — Error handling facilities
  - — Formatted, Free-formatted, and Unformatted data representation
  - — Internal (in-memory) file units provide capability to format and reformat data in internal memory buffers
  - — List Directed Formatting
- Supports arrays of up to seven dimensions.
- Supports logical operators
  .EQV. — Logical equivalence
  .NEQV. — Logical nonequivalence

Major extensions to FORTRAN 77 in Intel FORTRAN-80 include:

- Direct 8080/8085 port I/O supported by intrinsic subroutines.
- Binary and Hexadecimal integer constants.
- Well defined interface to FORTRAN-80 I/O statements (READ, OPEN, etc.), allowing easy use of user-supplied I/O drivers.
- User-defined INTEGER storage lengths of 1, 2 or 4 bytes.
- User-defined LOGICAL storage lengths of 1, 2 or 4 bytes.
- REAL STORAGE lengths of 4 bytes.
- Bitwise Boolean operations using logical operators on integer values.
- Hollerith data constants.
- Implicit extension of the length of an integer or logical expression to the length of the left-hand side in an assignment statement.
- A format descriptor to suppress carriage return on a terminal output device at the end of the record.

FORTRAN-80 COMPILER FEATURES

- Supports multiple compilation units in single source file.
- Optional Assembly Language code listing.
- Comprehensive cross-reference, symbol attribute and error listing.
- Compiler controls and directives are compatible with other Intel language translators.
- Optional Reentrancy.
- User-defined default storage lengths.
- Optional FORTRAN 66 Do Loop semantics.
- Source files may be prepared in free format.
- The INCLUDE control permits specified source files to be combined into a compilation unit at compile time.
- Transparent interface for software and hardware floating point support, allowing either to be chosen at time of linking.

FORTRAN-80 BENEFITS

FORTRAN-80 provides a means of developing application software for Intel® MCS-80/85 products in a familiar, widely accepted, and computer industry-standardized programming language. FORTRAN-80 will greatly enhance the user's ability to provide cost-effective solutions to software development for Intel microprocessors as illustrated by the following:

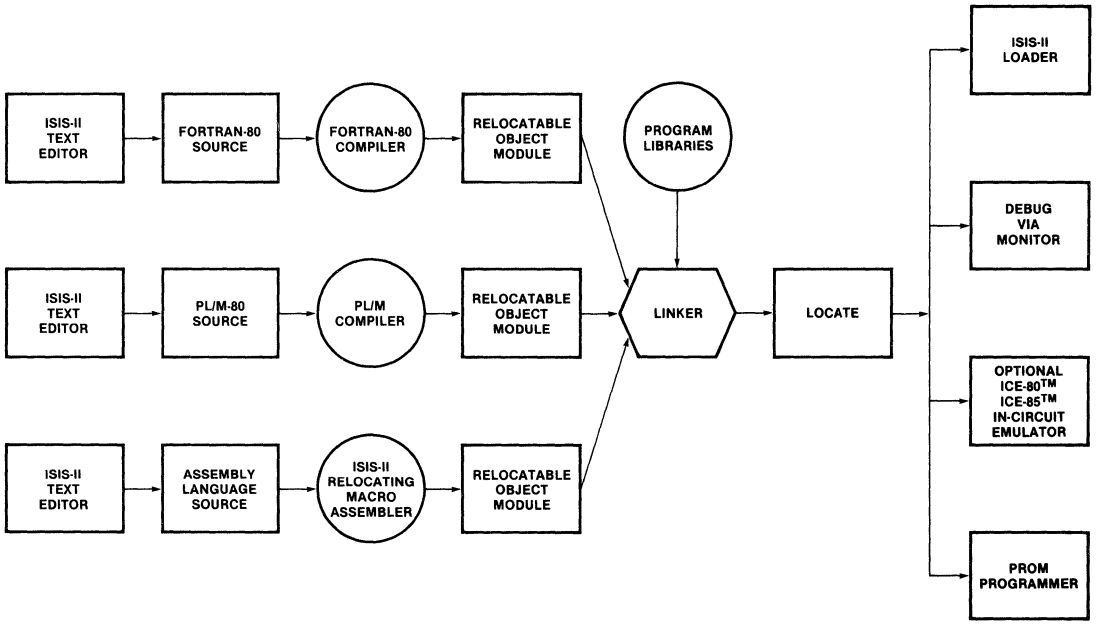
- *Completely Complementary to Existing Intel Software Design Tools* — Object modules are linkable with new or existing Assembly Language and PL/M Modules.
- *Incremental Runtime Library Support* — Runtime overhead is limited only to facilities required by the program.
- *Low Learning Effort* — FORTRAN-80, like PL/M, is easy to learn and use. Existing FORTRAN software can be ported to FORTRAN-80, and programs developed in FORTRAN-80 can be run on any other computer with ANS FORTRAN 77.
- *Earlier Project Completion* — Critical projects are completed earlier than otherwise possible because FORTRAN-80 will substantially increase programmer productivity, and is complementary to PL/M Modules by providing comprehensive arithmetic, I/O formatting, and data management support in the language.
- *Lower Development Cost* — Increases in programmer productivity translates into lower software development costs because less programming resources are required for a given function.
- *Increased Reliability* — The nature of high-level languages, including FORTAN-80, is that they lend themselves to simple statements of the program algorithm. This substantially reduces the risk of costly errors in systems that have already reached production status.
- *Easier Enhancements and Maintenance* — Like PL/M, program modules written in FORTRAN-80 are easier to read and understand than assembly language. This means it is easier to enhance and maintain FORTRAN-80 programs as system capabilities expand and future products are developed.
- *Comprehensive, Yet Simple Project Development* — The Intellec Microcomputer Development System, with the 8080/8085 Macro Assembler, PL/M-80 and FORTRAN-80 is the most comprehensive software design facility available for the Intel MCS-80/85 Microprocessor family. This reduces development time and cost because expensive (and remote) timesharing or large computers are not required.

SAMPLE FORTRAN-80 SOURCE PROGRAM LISTING

```
*    **  THIS PROGRAM IS AN EXAMPLE OF ISIS-II FORTRAN-80 THAT
*    **  CONVERTS TEMPERATURE BETWEEN CELSIUS AND FARENHEIT

      PROGRAM CONVRT

      CHARACTER*1 CHOICE, SCALE

      PRINT 100
*     **  ENTER CONVERSION SCALE (C OR F)
10    PRINT 200
      READ (5,300) SCALE

        IF (SCALE .EQ. 'C')
     +     THEN
              PRINT 400
*             **  ENTER THE NUMBER OF DEGREES FARENHEIT
              READ (5,*) DEGF
              DEGC = 5./9.*(DEGF-32)
*             **  PRINT THE ANSWER
              WRITE (6,500) DEGF,DEGC
*             **  RUN AGAIN?
20            PRINT 600
              READ (5,300) CHOICE
                 IF (CHOICE .EQ. 'Y')
     +              THEN
                       GOTO 10
                 ELSE IF (CHOICE .EQ. 'N')
     +              THEN
                       CALL EXIT
                 ELSE
                    GOTO 20
                 END IF
        ELSE IF (SCALE .EQ. 'F')
     +     THEN
*             **  CONVERT FROM FARENHEIT TO CELSIUS
              PRINT 700
              READ (5,*) DEGC
              DEGF = 9./5.*DEGC+32.
*             **  PRINT THE ANSWER
              WRITE (6,800) DEGC,DEGF
              GOTO 20
        ELSE
*          **  NOT A VALID ENTRY FOR THE SCALE
           WRITE (6,900) SCALE
           GOTO 10
        END IF
100   FORMAT(' TEMPERATURE CONVERSION PROGRAM',//,
     +' TYPE C FOR FARENHEIT TO CELSIUS OR',/,
     +' TYPE F FOR CELSIUS TO FARENHEIT',//)
200   FORMAT(/,' CONVERSION? ',$)
300   FORMAT(A1)
400   FORMAT(/,'ENTER DEGREES FARENHEIT: ',$)
500   FORMAT(/,F7.2,' DEGREES FARENHEIT = ',F7.2,' DEGREES CELSIUS')
600   FORMAT(/,' AGAIN (Y OR N)? ',$)
700   FORMAT(/,' ENTER DEGREES CELSIUS: ',$)
800   FORMAT(/,F7.2,' DEGREES CELSIUS = ',F7.2,' DEGREES FARENHEIT',/)
900   FORMAT(/,1H ,A1,' NOT A VALID CHOICE - TRY AGAIN!',/)
      END
```

FORTRAN-80

The FORTRAN-80 Compiler is an efficient, multiphase compiler that accepts source programs, translates them into relocatable object code, and produces requested listings. After compilation, the object program may be linked to other modules, located to a specific area of memory, then executed. The diagram shown below illustrates a program development cycle where the program consists of modules created by FORTRAN-80, PL/M-80 and the 8080/8085 Macro Assembler.



SPECIFICATIONS

OPERATING ENVIRONMENT

Required Hardware:

Intellec® Microcomputer Development System
- MDS-800, MDS-888
- Series II Model 220, Model 230

64K bytes of RAM memory

Dual diskette drives
- Single or Double Density

System console
- CRT or hardcopy interactive device

Optional Hardware:

Line Printer
ICE-80™, ICE-85™

Required Software:

ISIS-II Diskette Operating System
- Single or Double Density

Optional Software:

iSBC-801 FORTRAN-80 Run-Time Software Package for RMX-80

DOCUMENTATION PACKAGE

FORTRAN-80 Programming Manual (9800481)

ISIS-II FORTRAN-80 Compiler Operator's Manual (9800480)

FORTRAN-80 Programming Reference Card (9800547)

SHIPPING MEDIA

Flexible Diskettes
- Single and Double Density

ORDERING INFORMATION

PRODUCT CODE	DESCRIPTION
MDS-301	FORTRAN-80 Compiler for Intellec Microcomputer Development Systems

BASIC-80
EXTENDED ANS 1978 BASIC
INTELLEC® RESIDENT INTERPRETER

Meets ANS 1978 standard for minimal BASIC and adds many powerful extensions

Operates under the ISIS-II operating system on Intellec and Intellec Series-II Microcomputer Development Systems

Full sequential and random disk file I/O with ISIS-II

Applications range from prototyping microcomputer software to inexpensive engineering and management problem solving on the Intellec systems

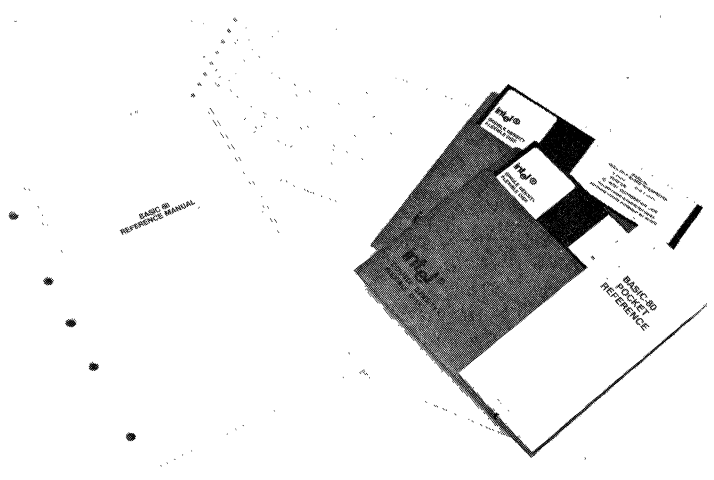
Supports the Intel floating point standard and provides integer and string data types

Can call user subroutines written in FORTRAN-80, PL/M-80, and 8080/85 macro assembler that are resident in the Intellec memory

Easily learned language and interactive environment combine to provide a flexible and powerful facility for developing programs to run on the Intellec Microcomputer Development Systems

BASIC is an industry standard, high-level programming language which is designed to be easily learned and used by novices and experienced programmers alike. The interpreter provides an interactive environment which allows fast and easy program development, testing, and debugging. BASIC is widely used for problem solving in engineering and management; extensive software exists for business applications such as order entry, accounts receivable, accounts payable, and inventory control, and engineering applications such as numeric and statistical analysis.

Intel's BASIC-80 meets the standards of ANS 1978 BASIC and extends them to take advantage of the software development capabilities of the Intellec Microcomputer Development Systems. The matching of these resources with the ease of programming in BASIC-80 provides a very effective tool for both microprocessor systems development and inexpensive applications programming and problem solving on the Intellec systems.



MPU SYSTEM

BASIC-80 LANGUAGE FEATURES

Standard ANS 78 BASIC features, all supported by BASIC-80, include:

- String and numeric constants, variables, and arrays.
- FOR . . . TO . . . STEP . . . NEXT statements for loop execution.
- IF . . . THEN statements for conditional execution.
- ON . . . GOTO statements for computed branching.
- GOSUB/RETURN subroutine calls and returns.
- Built in scientific functions:

ABS	RND	TAN
EXP	SGN	COS
INT	SQR	SIN
LOG	ATN	

- User defined single statement functions.

Major extensions to ANS 78 BASIC which BASIC-80 provides include:

- Support for the Intel single and double precision floating point standard.
- Disk file I/O, supporting both random access and sequential access files.
- Direct read and write to CPU I/O ports through the INP and OUT functions.
- Direct memory read and write through the PEEK and POKE functions.
- Calls to user-supplied external subroutines, which may have been written in FORTRAN-80, PL/M-80, or 8080/8085 Assembly Language and have been located at absolute memory locations using the ISIS-II facilities.
- User directed error trapping and handling functions.
- Program execution trace command.
- Formatted print statement with the PRINT USING function.
- ELSE clause for IF . . . THEN statements.
- Matrices with up to 110 dimensions.
- Extensive string manipulation functions.
- Boolean operators.
- Type conversion functions—integer, floating point, and character.

BENEFITS OF BASIC-80

- Added Value to the Intellec Systems—with BASIC-80 the Intellec Microcomputer Development Systems can be effectively used in many engineering and management applications.
- Inexpensive and Accessible Computational Facility—the ease of use and flexibility inherent in BASIC-80 and its interpretive environment fit well with the "at hand" computational resources of the Intellec systems. The combination is a particularly useful tool for obtaining fast and accurate results.
- Easy to Learn—the language is designed to be easily understood and learned. Results are obtained faster and people who may benefit from using the system can do so easily.
- Aid in Microcomputer Software Design—microcomputer software can be prototyped in BASIC-80 to inexpensively develop and test program logic.
- Complemented by Existing Software—subroutines written in PL/M-80, FORTRAN-80, and ASM 8080/85 can be called from BASIC-80 programs.
- Easy to Enhance and Maintain—BASIC-80, being straightforward and easily understood, provides for programs that are easy to maintain and modify in the future.

SPECIFICATIONS

Operating Environment

Required Hardware:

Intellec Microcomputer Development System
— MDS-800, MDS-888
— Series-II Model 220, Model 230

48K bytes of RAM memory

Diskette drive
— Single or double density

System console
— CRT or hard copy interactive device

Optional Hardware:

Line printer
Additional diskette drive

Required Software:

ISIS-II Diskette Operating System
— Single or double density

Documentation Package:

Basic-80 Reference Manual (9800758A)
Basic-80 Programming Reference Card (9800774)

Shipping Media:

Flexible diskettes
— Single and double density

EXAMPLE BASIC-80 PROGRAM

```
list
10 PRINT "THIS PROGRAM CALCULATES THE MEAN AND STANDARD"
20 PRINT " DEVIATION OF INPUT DATA"
30 S=0:V=0
40 INPUT "NUMBER OF VALUES";N
50 FOR I=1 TO N
60 INPUT A(I)
70 S=S+A(I)
80 NEXT
90 S=S/N
100 REM CALCULATION OF VARIANCE
110 FOR I=1 TO N
120 V=V+(A(I)-S)^2/N
130 NEXT
140 SD=SQR(V)
150 PRINT "MEAN=";S
160 PRINT "STANDARD DEVIATION IS=";SD
Ok

run
THIS PROGRAM CALCULATES THE MEAN AND STANDARD
 DEVIATION OF INPUT DATA
NUMBER OF VALUES? 6
? 34.7
? 32.9
? 38.2
? 35
? 37.6
? 40.9
MEAN= 36.55
STANDARD DEVIATION IS= 2.642442
Ok
```

ORDERING INFORMATION

Product Code	Description
MDS-320	ISIS-II BASIC-80 Disk-Based Interpreter

INTELLEC® SINGLE/DOUBLE DENSITY FLEXIBLE DISK SYSTEM

Flexible Disk system providing high speed Input/Output and data storage for Intellec Microcomputer Development Systems

Available in both single density and double density systems

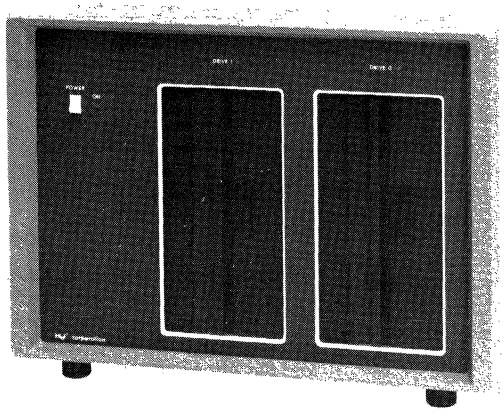
Data recorded on single density flexible disk is in IBM soft-sectored format which allows ¼ million byte data capacity with up to 200 files per flexible disk

Data recorded on double density flexible disk is in soft-sectored format which allows ½ million byte data capacity with up to 200 files per flexible disk

Associated software supports up to four double density drives and two single density drives, providing up to 2.5 Megabytes of storage in one system

Dynamic allocation and deallocation of flexible disk sectors for variable length files

The Intellec® Flexible Disk System is a sophisticated, general purpose, bulk storage peripheral for use with the Intellec Microcomputer Development System. The use of a flexible disk operating system significantly reduces program development time. The software system known as ISIS-II (Intel System Implementation Supervisor), provides the ability to edit, assemble, compile, link, relocate, execute and debug programs, and performs all file management tasks for the user.



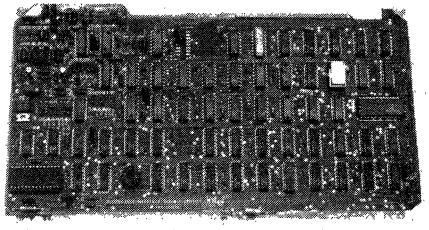
FLEXIBLE DISK SYSTEM

HARDWARE

The Intellec® flexible disk system provides direct access bulk storage, intelligent controller, and two flexible disk drives. Each single density drive provides ¼ million bytes of storage with a data transfer rate of 250,000 bits/second. The double density drive provides ½ million bytes of storage with a data transfer rate of 500,000 bits/second. The controllers are implemented with Intel's powerful Series 3000 Bipolar Microcomputer Set. The controllers provide interface to the Intellec System bus. Each single density controller will support two drives. Each double density controller will support up to four drives. The flexible disk system records all data in soft sector format.

The single/double density flexible disk controllers each consists of two boards, the Channel Board and the Interface Board. These two printed circuit boards reside in the Intellec System chassis. The boards are shown in the photograph, and are described in more detail in the following paragraphs.

SINGLE/DOUBLE DENSITY CHANNEL BOARD



DOUBLE DENSITY INTERFACE BOARD
(SINGLE DENSITY INTERFACE BOARD
IS SIMILAR TO THE ONE SHOWN ABOVE)

CHANNEL BOARD

The *Channel Board* is the primary control module within the flexible disk system. The Channel Board receives, decodes, and responds to channel commands from the Central Processor Unit (CPU) in the Intellec system. The Channel Board can access a block of Intellec system memory to determine the particular flexible disk operations to be performed and fetch the parameters required for the successful completion of the specified operation.

The control functions of the Channel Board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 Central Processing Elements (2-bit slice per CPE), a 3001 Microprogram Control Unit, and 512 x 32 bits of 3604 programmable-read-only-memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the Channel Board.

This board is the same for either single or double density drives, except that the Series 3000 microcode is different.

INTERFACE BOARD

The *Interface Board* provides the flexible disk controller with a means of communication with the flexible disk drives, as well as with the Intellec system bus. Under control of the microprogram being executed on the Channel Board, the Interface Board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the flexible disk platter), cause the head to move to the proper track and verify successful operation. The Interface Board accepts the data being read off the flexible disk, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the Channel Board.

During write operations, the Interface Board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

When the flexible disk controller requires access to Intellec system memory, the Interface Board requests the DMA master control of the system bus, and generates the appropriate memory command. The Interface Board also acknowledges I/O commands as required by the Intellec bus.

The Flexible Disk System is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

The channel board is different for single and double density drives, due to the different recording techniques used. The single density controller boards support one set of dual single density drives. The double density controller boards support up to two sets of dual double density drives (four drives total).

The double density controller may co-reside with the Intel single density controller to allow conversion of single density flexible disk to double density format, and provide up to 2.5M bytes of storage.

FLEXIBLE DISK DRIVE MODULES

Each flexible disk drive consists of read/write and control electronics, drive mechanisms, read/write head, track positioning mechanism, and the removable flexible disk platter. These components interact to perform the following functions:

- Interpret and generate control signals
- Move read/write head to selected track
- Read and write data

ASSOCIATED SOFTWARE — INTEL SYSTEMS IMPLEMENTATION SUPERVISOR (ISIS-II)

The Flexible Disk Drive System is to be used in conjunction with the ISIS-II Operating System. ISIS-II provides total file management capabilities, file editing, library management, run-time supports, and utility management.

ISIS-II provides automatic implementation of random access disk files. Up to 200 files may be stored on each ¼ million byte flexible disk for single density system or on each ½ million byte flexible disk for double density system. For more information, see the ISIS-II data specification sheet.

ISIS-II OPERATIONAL ENVIRONMENTAL

ISIS-II

32K bytes RAM memory
48K bytes when using Assembler Macro feature
64K bytes when using PL/M or Fortran
System Console
Single or Double density Flexible Disk Drive

HARDWARE SPECIFICATIONS

MEDIA

Single Density	Double Density
Flexible Disk	Double Density Specified Flexible Disk
One Recording Surface	One Recording Surface
IBM Soft Sector Format	Soft Sector Format
77 Tracks/Diskette	77 Tracks/Diskette
26 Sectors/Track	52 Sectors/Track
128 Bytes/Sector	128 Bytes/Sector

PHYSICAL CHARACTERISTICS

CHASSIS AND DRIVES

Mounting:	Table-Top or Standard 19" Retma Cabinet
Height:	12.08 in. (30.68 cm)
Width:	16.88 in. (42.88 cm)
Depth:	19.00 in. (48.26 cm)
Weight:	64.0 lb (29.0 kg)

ELECTRICAL CHARACTERISTICS

CHASSIS

DC Power Supplies
Supplied Internal to the Cabinet

AC Power Requirements
3-wire input with center conductor (earth ground) tied to chassis

Single-phase, 115 VAC; 60 Hz; 1.2 Amp Maximum (For a Typical Unit)
230 VAC; 50 Hz; 0.7 Amp Maximum (For a Typical Unit)

FLEXIBLE DISK OPERATING SYSTEM CONTROLLER

DC Power Requirements (All power supplied by Intellec Development System)

CHANNEL BOARD

Single Density	Double Density
5V @ 3.75A (typ), 5A (max)	5V @ 3.75A (typ), 5A (max)

INTERFACE BOARD

Single Density	Double Density
5V @ 1.5A (typ), 2.5A (max)	5V @ 1.5A (typ), 2.5A (max) – 10V @ 0.1A (typ), 0.2A (max)

FLEXIBLE DISK DRIVE PERFORMANCE SPECIFICATION

	Single Density	Double Density
Capacity (Unformatted):		
Per Disk	3.1 megabits	6.2 megabits
Per Track	41 kilobits	82 kilobits
Capacity (Formatted):		
Per Disk	2.05M bits	4.10 megabits
Per Track	26.6K bits	53.2 kilobits
Data Transfer Rate	250 kilobits/sec	500 kilobits/sec
Access Time:		
Track-to-Track	10 ms	10 ms
Head Settling Time	10 ms	10 ms
Average Random Positioning Time	260 ms	260 ms
Rotational Speed	360 rpm	360 rpm
Average Latency	83 ms	83 ms
Recording Mode	Frequency Modulation	M^2FM

ENVIRONMENTAL CHARACTERISTICS

MEDIA

Temperature:
Operating: 15.6°C to 51.7°C
Non-Operating: 5°C to 55°C
Humidity:
Operating: 8 to 80% (Wet bulb 29.4°C)
Non-Operating: 8 to 90%

DRIVES AND CHASSIS

Temperature:
Operating: 10°C to 38°C
Non-Operating: – 35°C to 65°C
Humidity:
Operating: 20% to 80% (Wet bulb 26.7°C)
Non-Operating: 5% to 95%

CONTROLLER BOARDS

Temperature:
Operating: 0 to 55°C
Non-Operating: – 55°C to 85°C
Humidity:
Operating: Up to 95% relative humidity without condensation
Non-Operating: All conditions without condensation of water or frost

EQUIPMENT SUPPLIED

SINGLE DENSITY

Cabinet, Power Supplies, Line Cord, Two Drives
Single Density FDC Channel Board
Single Density FDC Interface Board
Dual Auxiliary Board Connector
Flexible Disk Controller Cable
Flexible Disk Peripheral Cable
Hardware Reference Manual
Reference Schematics
ISIS-II Single Density System Disk
ISIS-II System User's Guide

DOUBLE DENSITY

Cabinet, Power Supplies, Line Cord, Two Drives
Double Density FDC Channel Board
Double Density FDC Interface Board
Dual Auxiliary Board Connector
Flexible Disk Controller Cable
Flexible Disk Peripheral Cable
Hardware Reference Manual
Reference Schematics
ISIS-II Double Density System Disk
ISIS-II System User's Guide

OPTIONAL EQUIPMENT

MDS-640	Rack Mount Kit
MDS-BLD	10 Blank Flexible Disks
MDS-DDR	Second Drive Cabinet with two additional drives

ORDERING INFORMATION

Part Number	Description
MDS-2DS/110V 2DS/220V	Flexible Disk drive unit with two drives, single density drive controller, software, and cables.
MDS-DDS/110V DDS/220V	Flexible Disk drive unit with two drives, double density drive controller, software, and cables.
MDS-DDR/110V DDR/220V	Add-on drive unit with two drives and double density cable, without controller and software. Can be used with double density controller.

ISIS-II
DISKETTE OPERATING SYSTEM
MICROCOMPUTER DEVELOPMENT SYSTEM

Supports up to four double density drives and two single density drives, providing up to 2.5 megabytes of storage in one system with up to 200 files per diskette

Relocating MCS-80/MCS-85 macro-assembler contains extended macro and conditional assembly capability

Command file facility allows console commands to be submitted from diskette file

Diskette operating system functions callable from user programs

Diskette system text editor provides string search, substitution, insertions, and deletion commands

Supports resident, high level programming languages, PL/M and FORTRAN

Provides dynamic allocation and de-allocation of diskette sectors for variable length files

Linker automatically combines separately assembled or compiled programs into single relocatable module

Library manager creates and updates program libraries

Supports all standard Intellec peripherals

Provides access to all Intellec monitor facilities

The ISIS-II Microcomputer Development System Diskette Operating System is a sophisticated, general purpose, high speed data handler and file manipulation system. It provides the ability to edit, assemble, compile, link, relocate, execute, and debug programs, and performs all user file management tasks. The ISIS-II operating system resides on the system diskette and supports a broad range of user oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS-II relocating macroassembler, linker, object locator, and library manager may be loaded from the diskette in seconds. All passes of the assembler may be executed without the need for user intervention. Object code and listings may be directed to any output device, or stored as diskette files. Powerful system console commands are provided in an easy to use context. Monitor mode may be entered by a special prefix to any sytem command or program call.

FUNCTIONAL DESCRIPTION

The ISIS-II operating system resides on the system diskette and supports a broad range of user oriented design aid software. Total file management and input editing features greatly reduce software development time. The ISIS-II relocating macroassembler, linker, object locator, and library manager may be loaded from the diskette in seconds. All passes of the assembler may be executed without the need for user intervention. Object code and listings may be directed to any output device, or stored as diskette files. A diagram of the ISIS-II system program development flow is shown in Figure 1.

ISIS-II Files

A file is a user defined collection of information of variable length. ISIS-II also treats each of the standard Intellec system peripherals as files through preassignment of unique file names to each device. In this manner data may be copied from one device to another (i.e., tape reader to tape punch) using the same command required to copy one diskette data file to another. ISIS-II provides automatic implementation of random access disk files. Each file is identified by a user chosen name unique on its diskette. Up to 200 files may be stored on each diskette.

ISIS-II System Commands

ISIS-II system commands are designed to provide the user with a powerful, easy to use program and file manipulation capability. Several commands have the capability of operating on several files at once via the wildcard file naming convention. As an example, the command DELETE ★.OBJ deletes all files in the diskette directory with the suffix .OBJ. A summary of ISIS-II system commands is presented in Table 1.

Call Capability — The delete, rename, and attribute assignment commands, along with a set of file I/O routines, are callable from user written programs. This allows the user to open, close, read, and write diskette files, access standard peripheral devices, write error messages, and load other programs via simple program call statements.

Command	Operation
Initialize disk	Initializes a diskette for use by the system. Requires only one disk drive.
Attribute assignment	Assigns specified attributes to a file, such as write-protect.
Copy	Creates copies of existing diskette files or transfers files from one device to another.
Delete	Removes a file from the diskette, thereby freeing space for allocation of other files.
Directory	Lists name, size, and attributes of files from a specified diskette directory.
Rename	Allows diskette files to be renamed.
Format	Initializes a diskette for use by the system. (Use with two or more drives.)
Debug	Loads a specified program from a diskette into memory and then transfers control to the Intellec monitor for execution and or debugging.
Submit	Provides capability for executing a series of ISIS-II commands previously written to a diskette file.

Table 1. ISIS-II System Commands

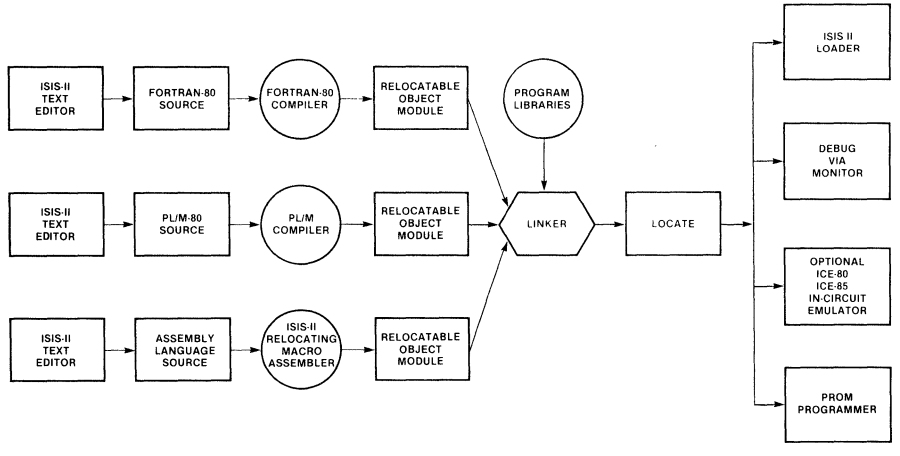


Figure 1. Program Development Flow Using ISIS-II Disk Operating System

ISIS-II Text Editor

The ISIS-II text editor is a comprehensive tool for assembly language, PL/M, and FORTRAN program entry and correction for Intel microcomputers. Its command set allows either entire lines of text or individual characters to be manipulated within a line.

Program Entry — Programs may be entered from the console keyboard or may be loaded directly. Text is stored internally in the editor's workspace, and may be edited with the following commands:

- string insertion or deletion
- string search
- string substitution

Utility Commands — To facilitate the use of these editing commands, utility commands are used to change positions in the workspace. These include:

- move pointer by line or by character
- move pointer to start of workspace
- move pointer to end of workspace

Storage — The contents of the workspace are stored on diskette and can be immediately accessed by ISIS-II commands or other programs, such as the ISIS-II MCS-80/MCS-85 macroassembler.

ISIS-II MCS-80/MCS-85 Relocating Macroassembler

Address Translation — The ISIS-II MCS-80/MCS-85 macroassembler translates assembly language mnemonics into relocatable and/or absolute object code modules. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easy to modify programs by adding or deleting instructions. Extended macro capability eliminates the need to rewrite similar sections of code repeatedly, and thus simplifies program documentation. Conditional assembly permits the assembler to include or delete sections of code that may vary from system to system, such as the code required to handle optional external devices. Additionally, the user is allowed complete freedom in assigning the location of code, data, and stack segments.

List File — The ISIS-II Assembler accepts diskette file input and produces a relocatable object file with corresponding symbol table and assembly listing file, including any error messages. A cross reference listing is also optionally produced. The list file may then be examined from the system console or copied to a specified list device.

Object File — The relocatable object file generated by the assembler may be combined with other object programs residing on the diskette to form a single relocatable object module or it can be converted to an absolute form for subsequent loading and execution.

ISIS-II Linker

The ISIS-II linker provides the capability to combine the outputs of several independently compiled or assembled object modules (files) into a single relocatable object module. The linker automatically resolves all external program and data references during the linking process. Object modules produced from previous link operations may be easily linked to a new module. ISIS-II also provides facilities to ease the generation of overlays. An optional link map showing the contents and lengths of each segment in the output module can be requested. All unsatisfied external references are also listed. If requested by the user, the ISIS-II linker can search a specified set of program libraries for routines to be included in the output module.

ISIS-II Object Locator

The ISIS-II locate program takes output from either the resident FORTRAN or PL/M compilers, the macroassembler, or the linker and transforms that output from relocatable format to an absolute format which may then be loaded via the standard ISIS-II loader, or loaded into an appropriate in-circuit emulator (ICE) module. During the locate process, code, data, and stack segments may be separately relocated, allowing code to be put in areas to be subsequently specified as ROM, while data and the stack are directed to RAM addresses. A locate map showing absolute addresses for each code and data segment and a symbol table dump listing symbols, attributes, and absolute address may also be requested.

ISIS-II Library Manager

The ISIS-II Library Manager program provides for the creation and maintenance of a program library containing Intel-provided and user-written programs and subroutines. These library routines may be linked to a program using the ISIS-II linker. Several libraries, each containing its own set of routines, may be created.

ORDERING INFORMATION

Part Number	Description
MDS-2DS or MDS-DDS 220	Diskette operating system

INTELLEC PROMPT 48
MCS-48 MICROCOMPUTER DESIGN AID

Complete low cost design aid and EPROM programmer for revolutionary MCS-48 single component computers

Simplifies microcomputing, allowing user to enter, run, debug, and save machine language programs with calculator-like ease

Utilizes two removable 8-bit MCS-48 CPUs
- **— 8748 CPU with erasable, reprogrammable on-chip program memory**
- **— 8035 CPU with off-chip program memory**

1K-byte erasable, reprogrammable on-chip (8748), expandable program memory, 1K-byte RAM in PROMPT system

64 bytes RAM on-chip, expandable register memory

256 bytes expandable RAM data memory in PROMPT system

27 on-chip TTL compatible expandable I/O lines

On-chip clock, internal timer/event counter, two vectored interrupts, eight level stack control

Single +5V DC system power requirement

Integral keyboard and displays (no teletypewriter or CRT terminal required)

Extensive PROMPT 48 monitor, allowing system I/O, bus, and memory expansion

Includes comprehensive design library

The Intellec Prompt 48 MCS-48 Microcomputer Design Aid is a low cost, fully-assembled design aid for the revolutionary 8748 single component microcomputer. PROMPT 48 simplifies the programming of MCS-48 systems — programs may be entered and debugged with calculator-like ease on the large, informative display and keyboard panel. The comprehensive design library with tutorial manual is ideal for newcomers to microcomputing. PROMPT 48's panel connector allows easy access to I/O ports and system bus. Thus users can expand program memory beyond the 1K bytes provided internally.

MPU SYSTEM

FUNCTIONAL DESCRIPTION

"PROMPT" stands for PROgraMming Tool. It is a programmer for 8748 EPROMs, and a versatile aid for debugging MCS-48 programs. Programs can be entered via its integral panel keyboard, programming socket, or serial channel. Almost any terminal can be interfaced to the serial channel, including a teletypewriter, CRT, or an Intellec microcomputer development system. Intellec PROMPT 48 simplifies the programming of MCS-48 systems. Like the 8748 it is radically new, highly integrated, and expandable. Like the MCS-48 family, it is low cost, and ideal for small applications and programs. It is a design aid, not a development system with sophisticated software and peripherals.

MCS-48 Processors

PROMPT 48 comes complete with two of Intel's revolutionary MCS-48 processors: an 8748-4 Single Component 8-Bit Microcomputer and and 8035-4 Single Component 8-Bit Microcomputer. Advances in n-channel MOS technology allow Intel, for the first time to integrate into one 40-pin component all computer functions:

8-bit CPU
1K x 8-bit EPROM/ROM program memory
64 x 8-bit RAM data memory
27 input/output lines
8-bit timer/event counter

Performance — More than 90 instructions — each one or two cycles — make the single chip MCS-48 equal in performance to most multi-chip microprocessors. The MCS-48 is an efficient controller and arithmetic processor, with extensive bit handling, binary, and BCD arithmetic instructions. These are encoded for minimum program length; 70% are single byte operation codes, and none is more than two bytes.

Flexibility — Three interchangeable, pin-compatible devices offer flexibility and low cost in development and production, as follows:

8748 — with user-programmable and erasable EPROM program memory for prototype and pre-productions systems.

8048 — with factory-programmed mask ROM memory for low-cost, high volume production.

8035 — without program memory, for use with external program memories.

Circuitry — Each MCS-48 processor operates on a single +5V supply, with internal oscillator and clock driver, and circuitry for interrupts and resets. Extra circuitry is in the 8048 ROM processor to allow low power standby operation. The 64 x 8 RAM data memory can be independently powered.

Compatibility — For systems requiring additional compatibility, the MCS-48 can be expanded with the new 8243 I/O expander, 8155 I/O and 256-byte RAM, 8755 I/O and 2K-byte EPROM, or 8355 I/O and 2K ROM devices. MCS-48 processors readily interface to MCS-80/85 peripherals and standard memories.

Memory Capacity

PROMPT 48 is a complete, fully assembled and powered microcomputer system including program memory, data memory, I/O, and system monitor beyond that available on MCS-48 single component computers. 1K bytes of PROMPT system RAM serve as "writable program memory" — a ROM simulator for the program memory on each MCS-48 computer. 256 bytes of PROMPT system RAM serve as "external data memory," beyond the 64 register bytes on each MCS-48 computer. Users may further expand program or data memory via the panel I/O ports and bus connector.

Programming

Programs written first in assembly language, are entered in machine language and debugged with calculator-like ease on the large, informative display and keyboard panel. Most MCS-48 operations can be specified with only two keystrokes. Once entered, routines can be exercised one instruction (single step) or many instructions at a time. The principal MCS-48 register — the accumulator — is displayed while single stepping. Programs can be executed in real time (GO NO BREAK) or with as many as eight different breakpoints (GO WITH BREAK).

Control

PROMPT 48 can be fully controlled either by the panel keyboard and displays, or remotely by a serial channel. Thus a teletypewriter or CRT can be used but neither is required.

Access

The PROMPT panel I/O ports and bus connector allow easy access to all MCS-48 pins except those reserved for control by the PROMPT system, namely EA external access, SS single step, and X1, X2 clock inputs.

Optional Expansion

PROMPT 48 may be expanded beyond the resources on both the MCS-48 single component computer and the PROMPT system. External program and data memory may be interfaced and input/out ports added with the 8243 I/O expander.

FEATURES

Single Component Computer

The 8748 is the first microcomputer fully integrated on one component. All elements of a computing system are provided, including CPU, RAM, I/O, timer, interrupts, and erasable, reprogrammable nonvolatile program memory.

Programming Socket

PROMPT's programming socket programs this revolutionary "smart PROM"—the 8748—in a highly reliable, convenient manner. A fail-safe interlock ensures the device is properly inserted before applying programming pulses. Each location may be individually programmed, one byte at a time. A read-before-write programming algorithm prevents device damage by inadvertently programming unerased memory.

MCS-48 Processors

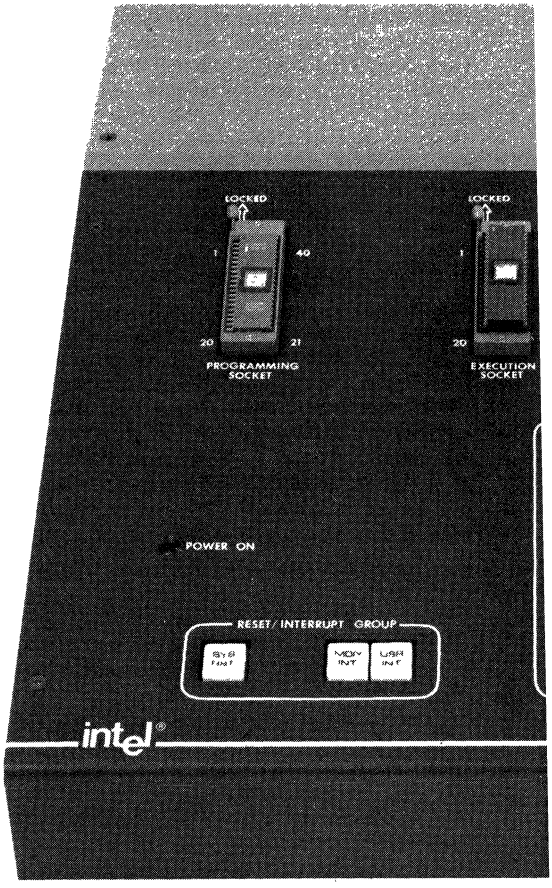
The execution socket accepts either an 8035 or an 8748 MCS-48 processor. Both are supplied with each PROMPT 48, and either can serve as heart of the PROMPT system. There are no processors within the PROMPT 48 mainframe, which instead contains monitor ROM and RAM, user RAM, peripherals, drivers, and sophisticated control circuitry. Once a processor is seated in the execution socket and power is applied, the PROMPT system comes to life. Various access modes may be selected such as program execution from PROMPT system RAM, or from on-chip PROM. Thus programs may first be executed from PROMPT RAM with the 8035 processor. When debugging is complete, the 8035 (execution socket) processor can program the 8748 (programming socket) processor. Finally, a programmed 8748 processor may be exercised by itself from the execution socket. The execution socket processor runs either monitor or user programs.

System Monitor

The system reset command initializes the PROMPT system and enters the monitor. The monitor interrupt command exits a user program gracefully, preserving system status and entering the monitor. The user interrupt command causes an interrupt only if the PROMPT system is running a user program. A comprehensive system monitor resides in four 1K-byte read only memories. It drives the PROMPT keyboard and displays and responds to commands and functions. The top 16 bytes of on-chip program memory must be used by the PROMPT system to switch between monitor and user programs. It requires one level of the MCS-48 eight-level stack.

Commands

PROMPT 48's commands are grouped and color-coded to simplify access to the 8748's separate program and data memory. Registers, data memory, or program memory, may be examined and modified with the examine and modify commands. Then either the next or previous register and memory locations may be accessed with one keystroke. Programs may be exercised in three modes. The go no break (GO NO BREAK) runs in real time. The go with break (GO WITH BREAK) mode is not real time — after each instruction the MCS-48 program counter is compared against pending breakpoints. If no break is encountered, execution resumes. The go single step (GO SINGLE STEP) mode exercises one instruction at a time. Commands are like sentences, with parameters separated by ⊡ NEXT. Each command ends with ⊡ EXECUTE/END. In addition to the PROMPT basic commands, thirteen functions simplify programming. Each is started merely by pressing a hex data/function key and entering parameters as required, as shown in Table 1.



MPU SYSTEM

Cable Interface

An optional cable, PROMPT-SER, directly connects the PROMPT system to virtually any terminal via a rear access slot.

Key	Function	Operation
2	Port 2 map	Allows specification of direction of each pin on port 2. Port 2 is multiplexed to address external program memory and expand I/O. Thus it must be buffered; the P2 map command establishes the direction of buffering.
3	Program EPROM	Programs 8748 EPROMs.
4	Byte search (with optional mask)	Sweeps through register, data, or program memory searching for byte matches. Starting and ending memory addresses are specified.
5	Word search (with optional mask)	Sweeps through register, data, or program memory searching for word matches. Starting and ending memory addresses are specified.
6	Hex calculator	Computes hexadecimal sums and differences.
7	8748 program for debug	Similar to program EPROM, but ensures that the top of program memory contains monitor re-entry code for debugging.
8	Compare	Verifies any portions of EPROM program memory against PROMPT memory.
9	Move memory	Allows blocks of register, data, or program memory to be moved.
A	Access	Specifies one of six access modes for PROMPT 48. For example EPROM, PROMPT RAM, or external program memory, and a variety of input/output options may be selected.
B	Breakpoint	Allows any or all of the eight breakpoints to be set and cleared.
C	Clear	Clears portions of register, data, or program memory.
D	Dump	Dumps register, data, or program memory to PROMPT's serial channel: for example, a teletypewriter paper tape punch.
E	Enter	Enters (reads) register, data, or program memory from PROMPT's serial channel.
F	Fetch	Fetches programs from EPROM to PROMPT RAM.

Table 1. PROMPT 48 Commands and Functions

Access

Easy access to the pins of the executing processor is provided via the I/O ports and bus connector. Only the EA external access, SS single step, and X1, X2 clock inputs are reserved for the PROMPT system.

Expansion

Program or data memory may be expanded beyond that provided on-chip or in the PROMPT system. I/O ports may be expanded, as with the 8243, or peripheral controllers may be memory-mapped. The I/O ports and Bus connector allows the execution socket processor to be directly interfaced to prototype systems, yet be controlled from the PROMPT panel.

Control

The command/function group panel keyboard and displays completely control PROMPT 48—a teletypewriter or CRT terminal is not needed. A hyphen prompting character appears whenever a command or function can be entered. Addresses and data are shown whenever examining registers and memory. Parameters for commands and functions are also shown.

Documentation

The PROMPT 48 manual includes chapters for the reader with little or no programming experience. Topics treated range from number systems to microcomputer hardware design. A novel, unifying set of tutorial diagrams — MICROMAPS — simplify microcomputer concepts. PROMPT's handy, pocket-sized reference cardlet can be affixed to the mainframe. Programming pads aid in the organization and documentation of programs. These features, plus a comprehensive design library of manuals, articles, and application notes, make the Intellec PROMPT 48 ideal for the newcomer to microcomputing.

SPECIFICATIONS

Timing

Basic Instruction — 2.5 μs
Cycle Time — t_{CY} = 2.5 μs
Clock — 6 MHz ± 0.1%

Memory Bytes

The 8748 contains 64 bytes of register memory, no external data memory, and 1024 bytes of RAM program memory. The PROMPT system provides 256 bytes of external data memory, and 1024 bytes of RAM program memory. PROMPT RAM program memory can be used in place of the on-chip EPROM program memory; thus programs less than 1024 bytes may be designed. For larger programs additional memory can be directly interfaced to the MCS-48 bus via the PROMPT panel I/O ports and bus connector.

Memory Configuration

Memory	Maximum	On Chip	In PROMPT 48
Register	64	64	0
Data	3328	0	256
Program	4096	1024 EPROM	1024 RAM

I/O Ports

All MCS-48 I/O ports are accessible on the PROMPT panel connector.

Bus — A true bidirectional 8-bit port with associated strobes. If the bidirectional feature is not needed, bus can serve as either a statically latched output port or a non-latching input port. Input and output lines cannot be mixed.

Ports 1 and 2 — Data written to these 8-bit ports is latched and remains unchanged until written. As inputs these lines are not latching. The lines of ports 1 and 2 are called quasibidirectional. A special output structure allows each line of port 1 and half of port 2 to serve as an input, an output, or both. Any mix of input, output, and both lines is allowed.

T0, T1, and INT — Three pins that can serve as inputs. T0 can be designated as a clock output. Input/output can be expanded via the PROMPT panel connector with a special I/O expander (8243) or standard peripherals.

Reset and Interrupts

Reset — initializes the PROMPT system and enters the monitor.

Monitor Interrupt — exits a user program gracefully, preserving system status and entering the monitor.

User Interrupt — causes an interrupt only if the PROMPT system is running a user program.

The processor traps to location 3_{16}. The MCS-48 timer/event counter is not used by the PROMPT system and is available to the user. Either timer flag or interrupt will signal when overflow has occurred. The timer interrupt can be used only in the go-no-break (real time) mode.

EPROM Programming

PROMPT 48 provides a programming socket to directly program 8748s. Programs are loaded into the PROMPT RAM program memory via keyboard. EPROM, teletypewriter, or other serial interface. A fail-safe interlock ensures programming pulses are applied only if the device is properly inserted. Inadvertant reprogramming is prevented by a read-before-write programming algorithm. Each location may be individually programmed, one byte at a time.

Panel I/O Ports and Bus Connectors

All MCS-48 pins, except five, are accessible on the I/O ports and bus connector. The five reserved for PROMPT system control are EA external access, SS single step, X1, X2 crystal inputs, and 5V. Due to internal buffering of the MCS-48 bus, access times will be negligibly degraded by the PROMPT system. Since MCS-48 processors do not communicate internal address gate status, bus data must be driven out if neither PSEN nor RD is asserted.

System Devices

Both user programs and the PROMPT monitor enjoy access to system devices: serial I/O, panel displays, and keyboard. These are memory-mapped to program memory addresses beyond 2K.

Serial I/O — The serial I/O port (data 820_{16}, control 821_{16}) is defined by software and jumpers for 110 baud, 20 mA current loop, but can easily be jumpered for other baud rates and RS232C levels. Asynchronous or synchronous transmission, data format, control characters, and parity can be programmed.

Panel Displays — Eight display ports (data 810-817_{16}) allow each of the panel displays to be written from user programs. Data written on a display device will time out after a fixed interval. Displays must be refreshed on a polled or interrupt-driven basis. User programs can call software drivers which provide this capability.

Keyboard — Software is used to debounce the panel keyboard (data 810_{16}). The monitor's input routines (see Software Drivers) provide this debouncing and can be called from user programs.

Commands

Single step
With break } Go
No break

Examine/modify { Register / Data / Program } Memory

Open previous/clear/entry ⊡ Next ☐ Execute/End

Functions

2 Port 2 map
3 Program EPROM (8748)
4 Search (R, D or P)* memory for 1 byte, optional mask
5 Search (R, D or P) memory for 2 bytes, optional mask
6 Hexadecimal calculator +, −
7 8748 program EPROM for debug
8 Compare EPROM with memory
9 Move memory (R, D or P)
A Access
B Breakpoint
C Clear memory (R, D or P)
D Dump memory (R, D or P)
E Enter (read) memory (R, D or P)
F Fetch EPROM program memory

Note
*R, D, or P is register, data, or program.

Software Drivers

Panel Keyboard In — KBIN, KDBIN
Panel Display Out — DGS6, DGOUT, HXOUT, BLK, REFS, ENREF
Serial Channel — CI, CO, RI, PO, CSTS

Connectors

Serial I/O — 3M 3462-0001 Flat Crimp/AMP 88106-1 Flat Crimp/ TI H312113 Solder/AMP 1-583485-5 Solder.

Panel I/O Ports and Bus Connector — 3M 3425 Flat Crimp. A complete cable set including wirewrap header for prototyping is included with each PROMPT.

Equipment Supplied

PROMPT 48 mainframe with two MCS-48 processors (8748, 8035), display/keyboard, EPROM programmer, power supply, cabinet, and ROM-based monitor.
110 V AC power cable
110 or 220 V AC
Fuse
Panel I/O ports
Bus connector cable set

Physical Characteristics

Height — 5.3 in. (13.5 cm) max
Width — 17 in. (43.2 cm)
Depth — 17 in. (43.2 cm) max
Weight — 21 lb. (9.6 kg)

Electrical Characteristics

Power Requirements — either 115 or 230V AC (± 10%) may be switch selected on the mainframe. 1.8 amps max current (at 125 V AC).
Frequency — 47-63 Hz

Environmental Characteristics

Operating Temperature — 0°C to +40°C
Non-Operating Temperature — 20°C to +65°C

Reference Manuals

9800402 — Intellec PROMPT 48 User's Manual (SUPPLIED)
9800270 — MCS-48 User's Manual (SUPPLIED)
9800255 — MCS-48 and UPI-41 Assembly Language Programming Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
PROMPT-48 or PROMPT-48-220V	Intellec PROMPT 48 MCS-48 microcomputer design aid. Complete with two MCS-48 processors (8748 and 8305), EPROM programmer, integral keyboard, displays, and system monitor in ROM.
PROMPT-SER	Serial cable for connecting PROMPT to TTY, CRT

ICE-49
MCS-48 IN-CIRCUIT EMULATOR

Emulates 8049, 8048, 8748, 8039, 8035, and 8021* Microcomputers

Extends Intellec microcomputer development system debug power to user configured system via external cable and 40-pin plug, replacing system MCS-48 device

Emulates user system MCS-48 device in real time

Shares static RAM memory with user system for program debug

Provides hardware comparators for user designated break conditions

Eliminates need for extraneous debugging tools residing in user system

Collects bus, register, and MCS-48 status information on instructions emulated

Provides capability to examine and alter MCS-48 registers, memory, and flag values, and to examine pin and port values

Integrates hardware and software efforts early to save development time

The ICE-49 MCS-48 In-Circuit Emulator module is an Intellec-resident module that interfaces with any MCS-48 system. The MCS-48 family consists of the 8049, 8048, 8748, 8039, 8035, and 8021 microcomputers. The ICE-49 module interfaces with an MCS-48 system through a cable terminating in an MCS-48 pin-compatible plug which replaces the MCS-48 device in the sytem. With the ICE-49 plug in place, the designer has the capability to execute the system in real time while collecting up to 255 instruction cycles of real-time trace data. In addition, he can single step the system program to monitor more closely the program logic during execution. Static RAM memory is available through the ICE-49 module to emulate MCS-48 program and data memory. The designer can display and alter the contents of data and replacement RAM control memory, internal MCS-48 registers and flags and I/O ports. Powerful debug capability is extended into the MCS-48 system while ICE-49 debug hardware and software remain inside the Intellec system. Symbolic reference capability allows the designer to use meaningful symbols rather than absolute values when examining and modifying memory, registers, flags, and I/O ports in this system.

*EM1 emulator board is also required.

FUNCTIONAL DESCRIPTION

Debug Capability Inside User System

The ICE-49 module provides the user with the ability to debug a full prototype or production system without introducing extraneous hardware or software test tools. The module connects to the user system through the socket provided for the MCS-48 device in the user system. Intellec memory is used for the execution of the ICE-49 software. The Intellec console and file handling capabilities provide the designer with the ability to communicate with the ICE-49 module and display information on the operation of the prototype system. The ICE-49 module block diagram is shown in Figure 1.

Batch Testing

In conjunction with the ISIS-II diskette operating system, the ICE-49 module can run extensive system diagnostics without operator intervention. The designer or test engineer can define a complete diagnostic exercise, which is stored in a file on the diskette. When activated with an ISIS-II submit command, this file can instruct the ICE-49 module to execute the diagnostic routine and store the results in another file on the diskette. Results are available to the designer at his convenience. In this way, routine diagnostics and long term testing may be done without tying up valuable manpower.

Integrated Hardware/Software Development

The user prototype need consist of no more than an MCS-48 socket and timing logic to begin integration of software and hardware development efforts. Through the ICE-49 module mapping capabilities, Intellec system resources can be accessed to replace prototype memory. Hardware designs can be tested using the system software to drive the final product. Thus, the system integration phase, which can be costly when attempting to mesh completed hardware and software products, becomes a convenient two-way debug tool when begun early in the design cycle.

Real-Time Trace

The ICE-49 module captures trace information while the designer is executing programs in real time. The instructions executed, program counter, port values for bus 0, port 1 and port 2, and the values of selected MCS-48 status lines are stored for the last 255 instruction cycles executed. When retrieved for display, code is disassembled for user convenience. This provides data for determining how the user system was reacting prior to emulation break, and is available whether the break was user initiated or the result of an error condition. For more detailed information on the actions of internal registers, flags, or other system operations, the user may operate in single or multiple step sequences tailored to system debug needs.

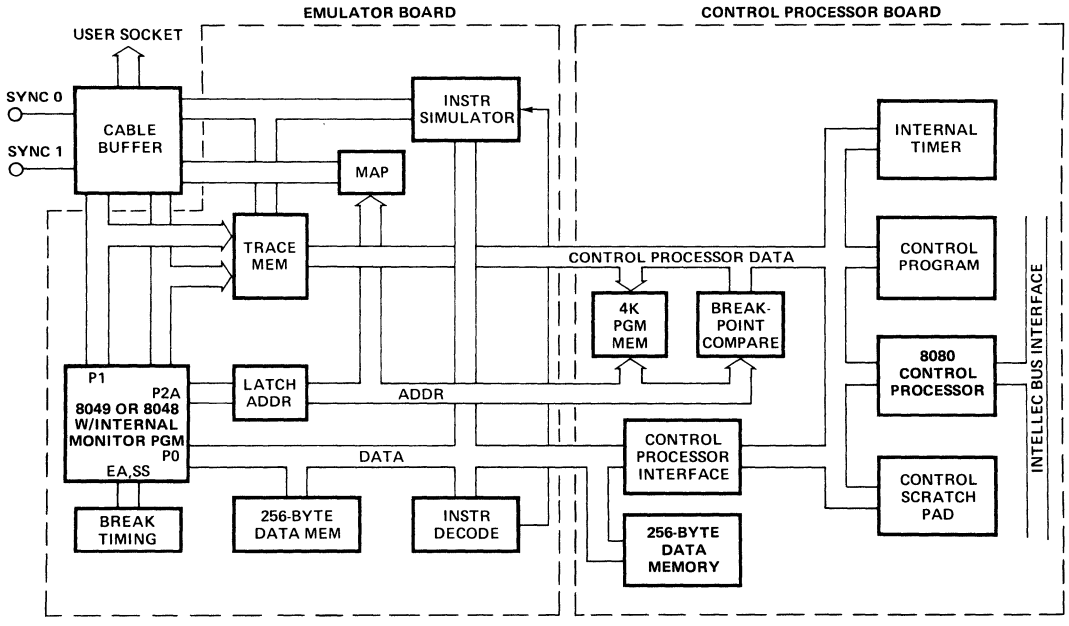


Figure 1. ICE-49 Module Block Diagram

Memory Mapping

The 8049, 8748 and 8048 contain internal program and data memory. Both program and data memory can be expanded using external memory devices.

Internal Memory — When the MCS-48 microcomputer is replaced by the ICE-49 socket in a system, the ICE-49 module supplies static RAM memory as a replacement for the internal microcomputer memory. The ICE-49 module has enough RAM memory available to emulate up to the total 4K control memory capability of the system. The ICE-49 module also provides for up to 320 bytes of data memory.

External Memory — The ICE-49 module separates replacement control memory into sixteen 256-byte blocks. Replacement external data memory consists of one 256-byte block. Each block of memory can be defined separately as supplied by the user system or supplied by the ICE-49 module. The user may assign ICE-49 equivalent memory to take the place of external memory not yet supplied in his system.

Symbolic Debugging

ICE-49 software provides symbolic definition of all MCS-48 registers, flags, and selected MCS-48 pins. Symbolically defined pseudo registers provide access to the sense of MCS-48 flip flops which enable time, counter, interrupt, and flag-0/flag-1 options. In addition, the user may reference locations in program and data memory, or their contents, symbolically. The user symbol table generated along with the object file during a program assembly may be loaded to Intellec memory for access during emulation. The user is encouraged to add to this symbol table any additional symbolic values for memory addresses, constants, or variables he may find useful during system debugging. Symbols may be substituted for numeric values in any of the ICE-49 commands. Symbolic reference is a great advantage to the system designer. He is no longer burdened with the need to recall or look up those addresses of key locations in his program that can change with each assembly. Meaningful symbols from his source program may be used instead. For example, the command:

```
GO FROM .START TILL XDATA. RSLT WRITTEN
```

begins execution of the program at the address referenced by the label START in the designers assembly program. A breakpoint is set to occur the first time the microprocessor writes to the external data memory location referenced by RSLT. The designer does not have to be concerned with the physical locations of START and RSLT. The ICE-49 software driver supplies them automatically from information stored in the symbol table.

Hardware

The ICE-49 module is a microcomputer system utilizing Intel's 8049 or 8048/8748 microcomputer as its nucleus. The 8049 provides the 8049, 8039 emulation characteristics. The 8048/8748 provides the 8748/8648/8035/8021 emulation characteristics. The ICE-49 module uses an Intel 8080 to communicate with the Intellec host processor via a common memory space. The 8080 also controls an internal ICE-49 bus for intramodule communication. ICE-49 hardware consists of two PC boards, the controller board, and the emulator board, all of which reside in the Intellec chassis. A cable interfaces the ICE-49 boards to the MCS-48 system. The cable terminates in a MCS-48 pin compatible plug which replaces any MCS-48 device in the user system. The ICE-49 module block diagram is shown in Figure 1.

Real-Time Trace

Trace Buffer — While the ICE-49 module is executing the user program, it is monitoring port, program counter, data, and status lines. Values for each instruction cycle executed are stored in a 255 x 44 real-time RAM trace buffer. A resetable timer resident on the controller board counts instruction cycles.

Controller Board

The ICE-49 module talks to the Intellec system as a peripheral device. The controller board receives commands from the Intellec system and responds through the parameter block. Three 15-bit hardware breakpoint registers are available for loading by the user. While in emulation mode, a hardware comparator is constantly monitoring address and status lines for a match to terminate an emulation. The breakpoint registers provide a signal when a match is detected. The user may disable the emulation break capability and use the signal to synchronize other debug tools. The controller board returns real-time trace data, MCS-48 register, flag, and pin values, and ICE-49 status information, to a control block in the Intellec system when emulation is terminated. This information is available to the user through the ICE-49 interrogation commands. Error conditions, when present, are automatically displayed on the Intellec system console. The controller board also contains static RAM memory, which can be used to emulate MCS-48 program and data memory in real time. 4K of memory is available in sixteen 256-byte pages to emulate MCS-48 PROM or PROM program memory. A 256-byte page of data memory is available to access in place of MCS-48 external data memory. The controller board address map directs the ICE-49 module to access either replacement ICE-49 memory or actual user system external memory in 256-byte segments based on information provided by the user.

Emulator Board

The emulator board contains the 8049* and peripheral logic required to emulate the MCS-48 device in the user system. A software selectable 6 MHz or 3 MHz clock drives the emulated MCS-48 device. This clock can be disabled and replaced with a user supplied TTL clock in the user system.

*Use 8048 with internal monitor program when emulating 8748/8048/8035/8021.

Cable Card

The cable card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector which plugs into the user system in the socket designed for the MCS-48 device.

Software

The ICE-49 software driver is a RAM-based program which provides the user with an easy to use command language (see Table 1, Table 2, and Table 3) for defining breakpoints, initiating real-time emulation or single step operation, and interrogating and altering user system status recorded during emulation. The ICE-49 command language contains a broad range of modifiers to provide the user with maximum flexibility in defining the operation to be performed. The ICE-49 software driver is available on diskette and operates in 32K of Intellec RAM memory.

Command	Operation
Enable	Activates breakpoint and display registers for use with go and step commands.
Go	Initiates real-time emulation and allows user to specify breakpoints and data retrieval.
Step	Initiates emulation in single instruction increments. Each step is followed by register dump. User may optionally tailor other diagnostic activity to his needs.
Interrupt	Emulates user system interrupt.

Table 1. ICE-49 Emulation Commands

Command	Operation
Display	Prints contents of memory, MCS-48 device registers, I/O ports, flags, pins, real-time trace data, symbol table, or other diagnostic data on list device.
Change	Alters contents of memory, register, output port, or flag. Sets or alters breakpoints and display registers.
Map	Defines memory status.
Base	Establishes mode of display for output data.
Suffix	Establishes mode of display input data.

Table 2. ICE-49 Interrogation Commands

Command	Operation
Load	Fetches user symbol table and object code from input device.
Save	Sends user symbol table and object code to output device.
Define	Enters symbol name and value to user symbol table.
Move	Moves block of memory data to another area of memory.
List	Defines list device.
Exit	Returns program control to ISIS-II.
Evaluate	Converts expression to equivalent values in binary, octal, decimal, and hex.
Remove	Deletes symbols from symbol table.
Reset	Reinitializes ICE-49 hardware.

Table 3. ICE-49 Utility Commands

SPECIFICATIONS

ICE-49 Operating Environment

Required Hardware

Intellec microcomputer development system
System console
Intellec diskette operating system
ICE-49 Module

Required Software

System monitor
ISIS-II

Equipment Supplied

Printed circuit boards (control board, emulator board)
Interface cables and buffer module
ICE-49 software, diskette-based version (single density or double density)
8048 with internal monitor program

System Clock

Crystal controlled 6.0 MHz internal, 3.0 MHz internal or user supplied TTL external: software selectable.

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 8.00 lb. (3.64 kg)

Electrical Characteristics

DC Power Requirements

V_{CC} = +5V ±5%
I_{CC} = 10A max; 7.0A typ
V_{DD} = +12V ±5%
I_{DD} = 79 mA max; 45 mA typ
V_{BB} = −10V ±5%
I_{BB} = 20 mA max

Input Impedance — @ICE-49 user socket pins:

V_{IL} = 0.8V (max), I_{IL} = -1.6 mA,
V_{IH} = 2.0V (min), I_{IH} = 40 μA

For Bus:
V_{IL} = 0.8V (max), I_{IL} = -250 μA
V_{IH} = 2.0V (min), I_{IH} = 20 μA

Output Impedance — @ICE-49 user socket pins:

P1, P2:
V_{OL} = 0.5V (max), I_{OL} = 16 mA
V_{OH} = V_{CC} (10K pullup)

For Bus:
V_{OL} = 0.5V (max), I_{OL} = 25 mA
V_{OH} = 3.65V (min), I_{OH} = -1 mA

Others:
V_{OL} = 0.5V (max), I_{OL} = 16 mA
V_{OH} = 2.4V (max), I_{OH} = -400 μA

Environmental Characteristics

Operating Temperature — 0°C to 40°C (Room Temperature)

Operating Humidity — Up to 95% relative humidity without condensation

Reference Manuals

9800632 — ICE-49 Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-49-ICE	8049, 8048, 8039, 8748, 8035, 8021 CPU in-circuit emulator. Cable assembly and interactive diskette software included
MDS-498	Assembled kit to upgrade ICE-48 to ICE-49 capability. ICE-49 emulator board, 8049/8048 CPU components with internal monitor program, ICE-49 firmware and diskette software included.

ICE-80
8080 IN-CIRCUIT EMULATOR

Connects Intellec system to user configured system via an external cable and 40-pin plug, replacing the user system 8080

Allows real-time (2 MHz) emulation of user system 8080

Shares Intellec RAM, ROM, and PROM memory and Intellec I/O facilities with user system

Checks for up to three hardware and four software break conditions

Offers full symbolic debugging capabilities

Eliminates need for extraneous debugging tools residing in user system

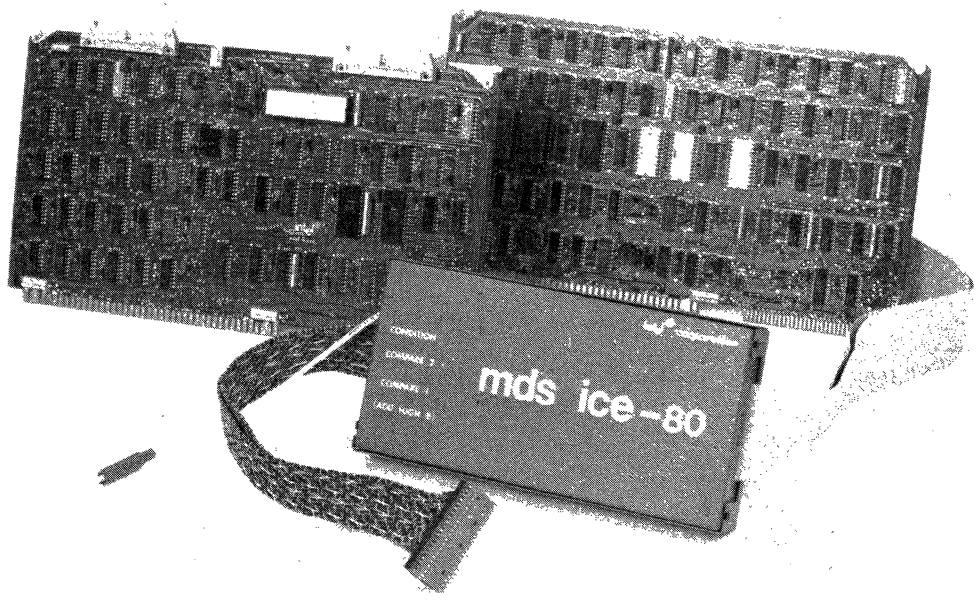
Provides address, data, and 8080 status information on last 44 machine cycles emulated

Provides capability to examine and alter CPU registers, main memory, pin, and flag values

Integrates hardware and software development efforts

Available in diskette or paper tape versions

The Intellec ICE-80 8080 In-Circuit Emulator is an Intellec resident module designed to interface with any user configured 8080 system. With ICE-80 as a replacement for a prototype system 8080, the designer may emulate the system's 8080 in real time, single step the system's program, and substitute Intellec memory and I/O for user system equivalents. Powerful Intellec debug functions are extended into the user system. For the first time the designer may examine and modify his system with symbolic references instead of absolute values.



FUNCTIONAL DESCRIPTION

Integrated Hardware/Software Development

Use of the ICE-80 module enables the system integration phase, which can be so costly and frustrating when attempting to mesh completed hardware and software products, to become a convenient two-way debug tool when begun early in the design cycle. The user prototype need consist of no more than an 8080 CPU socket and a user bus to begin integration of software and hardware development efforts. With the ICE-80 mapping capabilities, system resources may be accessed for missing prototype hardware. Hardware designs may be tested using system software to drive the final product. A functional block diagram of the ICE-80 module is shown in Figure 1.

Symbolic Debugging Capability

ICE-80 provides for user-defined symbolic references to program memory addresses and data. Symbols may be substituted for numeric values in any of the ICE-80 commands. The user is thus relieved from looking up addresses of variables or program subroutines.

Symbol Table — The user symbol table generated along with the object file during a PL/M compilation or a MAC80 or resident assembly, is loaded to memory along with the user program to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables found useful during system debugging. By referring to symbolic memory addresses, the user may be assured of examining, changing, or breaking at the intended location.

Symbolic Reference — ICE-80 provides symbolic definition of all 8080 registers, flags, and selected pins. The following symbolic references are also provided for user convenience: TIMER, a 16-bit register containing the number of ϕ_2 clock pulses elapsed during emulation; ADDRESS, the address of the last instruction emulated; INTERRUPTENABLED, the user 8080 interrupt mechanism status; and UPPERLIMIT, the highest RAM address occupied by user memory.

Debug Capability Inside User System

ICE-80 provides for user debugging of full prototype or production systems without introducing extraneous hardware or software test tools. ICE-80 connects to the user system through the socket provided for the user 8080 in the user system (See Figure 2). Intellec memory is used for the execution of the ICE-80 software, while I/O provides the user with the ability to communicate with ICE-80 and receive information on the generation of the user system. A sample ICE-80 debug session is shown in Figure 3.

I/O Mapping and Memory

Memory and I/O for the user system may be resident in the user system or "borrowed" from the Intellec system through ICE-80's mapping capability.

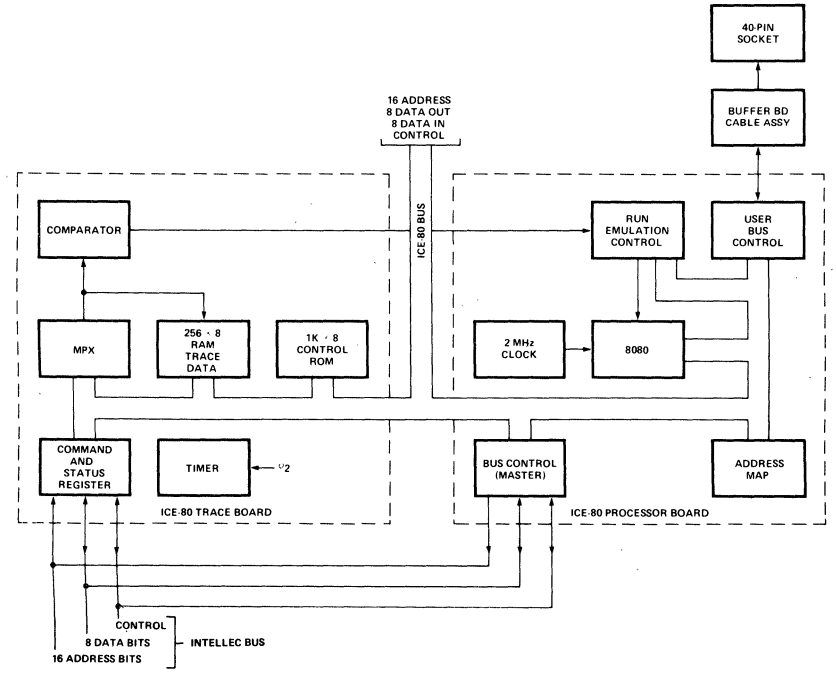


Figure 1. Functional Block Diagram of ICE-80 Module

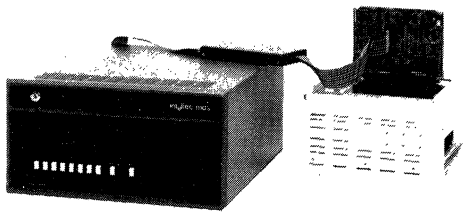


Figure 2. ICE-80 Module Installed in User System

Memory Blocking — ICE-80 separates user memory into 16 4K blocks. User I/O is divided into 16 16-port blocks. Each block of memory or I/O may be defined independently. The user may assign system equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, memory or I/O may be accessed in place of user system devices during prototype or production checkout.

Error Messages — The user may also designate a block of memory or I/O as nonexistent. ICE-80 issues error messages when memory or I/O designated as nonexisting is accessed by the user program.

Real-Time Trace

ICE-80 captures valuable trace information while the user is executing programs in real time. The 8080 status, the user memory or port addressed, and the data read or written (snap data), is stored for the last 44 machine cycles executed. This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was user initiated or the result of an error condition. For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multiple step sequences tailored to system debug needs.

Hardware

The heart of the ICE-80 is a microcomputer system utilizing Intel's 8080 microprocessor as its nucleus. This system communicates with the Intellec host processor via I/O commands. Host processor commands and ICE-80 status are interchanged through registers on the ICE-80 trace board. ICE-80 and the system also communicate through a control block resident in the Intellec main memory, which contains detailed configuration and status information transmitted at an emulation break. ICE-80 hardware consists of two PC boards — the processor and trace boards residing in the Intellec chassis — and a 6-foot cable interfacing to the user system. The trace and processor boards communicate with the system on the bus, and also with each other on a separate ICE-80 bus. ICE-80 connects to the user system through a cable that plugs directly into the socket provided for the user's 8080.

Trace Board

The trace board talks to the system as a peripheral device. It receives commands to ICE-80 and returns ICE-80 responses. While ICE-80 is executing the user program, the trace board collects data for each machine cycle emulated (snap data). The information is continuously stored in high-speed bipolar memory.

Breakpoint — The trace board also contains two 24-bit hardware breakpoint registers which can be loaded by the user. While in emulation mode, a hardware comparitor is constantly monitoring address and status lines for a match to terminate an emulation. A user probe is also available for attachment to any user signal. When this signal goes true a break condition is recognized.

Interrogation — The trace board signals the processor board when a command to ICE-80 or break condition has been detected. The ICE-80 CPU then sends data stored on the trace board to the control block in memory. Snap data, along with information on 8080 registers and pin status and the reason for the emulation break, are then available for access during interrogation mode. Error conditions, if present, are transmitted and automatically displayed for the user.

Processor Board

An 8080 CPU resides on the processor board. During emulation it executes instructions from the user's program. At all other times it executes instructions from the control program in the trace module's ROM.

Timing — The processor board contains an internal clock generator to provide clocks to the user emulation CPU at 2 MHz. The CPU can alternately be driven by a clock derived from user system signal lines. The clock source is selected by a jumper option on the board. A timer on the trace board counts the ϕ_2 clock pulses during emulation and can provide the user with the exact timing of the emulation.

On/Off Control — The processor board turns on an emulation when ICE-80 has received a run command from the system. It terminates emulation when a break condition is detected on the trace board, or the user's program attempts to access memory or I/O ports designated as nonexistent in the user system, or the user 8080 is inactive for a quarter of a second.

Status Storage — The address map located on the processor board stores the assigned location of each user memory or I/O block. During emulation the processor board determines whether to send/receive information

```
ISIS 8080 MACROASSEMBLER, V1.0          PAGE 1

                ;USER PROGRAM TO OUTPUT A SERIES OF
                ;CHARACTERS TO SDK-80 CONSOLE DEVICE
                ;
1320                    ORG     1320H
01E3            C0      EQU     1E3H    ;SDK-80 CONSOLE OUT DRIVER
                ;
1320 0601       START:  MVI     B,1     ;SET UP B VALUE
1322 3A3613             LDA     DAT1    ;LOAD A WITH DAT1 VALUE
135 4F          LOOP:   MDV     C,A
1326 CDE301             CALL    C0      ;SEND C VALUE TO CONSOLE
1329 79                 MOV     A,C     ;RESTORE A
132A 93                 SBB     B       ;SUBTRACT B FROM A
132B 323713             STA     RSLT    ;STORE RESULT IN RSLT
132E FE40               CPI     40H     ;LAST VALUE TO PRINT
1330 C22513             JNZ     LOOP    ;LOOP AGAIN IF A>40H
1333 C32013             JMP     START   ;ELSE RESTART WHOLE PROCEDURE
                ;
1336 5A         DAT1:   DB      5AH
1337            RSLT:   DS      1
0000                    END

ISIS, V1.0      INITIAL ICE-80 SESSION
-ICE80          (Note: The SDK-80 Monitor has already been used to initialize the SDK-80 Board)
ISIS ICE-80, V1.0
(1) **XFORM MEMORY 0 TO 1 U
    *XFORM IO 0FH U
(2) *LOAD PROG. HEX
    ERR = 067
    STAT = 11H TYPE = 06H CMND = 07H ADDR = 1320H GOOD = 06H BAD = 04H
    *CHANGE MEMORY 1321H = FFH
    ERR = 067
    STAT = 11H TYPE = 06H CMND = 07H ADDR = 1321H GOOD = FFH BAD = FDH
    *LOAD PROG. HEX
(3) *GO FROM START UNTIL RSLT WRITTEN
    EMULATION BEGUN
(4) ERR = 067
    STAT = 11H TYPE = 07H CMND = 02H
(5) *DISPLAY CYCLES 5

    STAT = A2H ADDR = 1326H DATA = CDH
    STAT = 82H ADDR = 1327H DATA = E3H
    STAT = 82H ADDR = 1328H DATA = 01H
    STAT = 04H ADDR = FFFFH DATA = 13H
    STAT = 04H ADDR = FFFEH DATA = 29H
(6) *CHANGE DOUBLE REGISTER SP = 13FFH
    *BASE HEX
    *EQUATE STOP = 1333H
(7) *GO FROM START UNTIL STOP EXECUTED THEN DUMP
    EMULATION BEGUN
    B = 01H C = 41H D = 00H E = 00H H = 00H L = 00H F = 56H A = 40H P = 1320H * = 1333H S = 13FFH
    EMULATION TERMINATED AT 1333H
(8) *EXIT
    *FFFF
```

Notes

1. Set up user memory and I/O. The program is set up to execute in block 1 (1000H–1FFFH) of user memory, and requires access to the SDK-80 monitor (block 0) and I/O ports in block 0FH. Both ports and memory are defined as available to the user system. All other memory and I/O is initialized by ICE-80 as nonexistent (guarded).

2. A load command generates an error. The type and command numbers indicate that a data mismatch occurred on a write to memory command. The data to be written to address 1320H should have been 06H. When ICE-80 read the data after writing it, a 04H was detected. A change command to a different memory address hints that bit 1 does not go to 1 anywhere in this memory block. Examination indicates that a pin was shorted on the RAM located at 1300H–13FFH in the prototype system. The problem is fixed and a subsequent load succeeds.

3. A real-time emulation is begun. The program is executed from 'START' (1320H) and continues until 'RSLT' is written [in location 1328H, the contents of the accumulator is stored in (written into) 'RSLT'].

4. An error condition results: TYPE 07, CMND 02 indicate the program accessed is a guarded area.

5. The last 5 machine cycles executed are displayed. The last instruction executed was a call (CDH). The fourth and fifth cycles are a push operation (designated by status 04H) to store the program counter before executing the call. The stack pointer was not initialized in the program and is accessing memory location FFFFH.

6. After making a note to initialize the stack pointer in the next assembly, a temporary fix is effected by setting the stack pointer to the top of user available memory.

7. After setting the base for displays to hex and adding the symbol 'STOP' to the symbol table, emulation is started which will terminate when the instruction at 1333H ('STOP') is executed. When emulation terminates, a dump of the contents of user 8080 registers is requested. One can see that the value of the accumulator is set at 40H, the stack pointer is set at 13FFH, the last address executed (*) is 1333H, and the program counter has been set to 1320H.

8. Exit returns control to the MDS monitor.

Figure 3. Sample ICE-80 Debug Session

on the Intellec or user bus by consulting the address map. The processor board allows the ICE-80 CPU to gain access to the bus as a master to "borrow" Intellec facilities. At an emulation break, the processor board stores the status of specified 8080 input and output signals, disables all interaction with the user bus, and commands the trace board to send stored information to a control block in Intellec memory for access during interrogation mode.

Cable Card

The cable card is included for cable driving. It transmits address and data bus information to the user system through a 40-pin connector that plugs into the user system in the socket designed for the 8080 when enabled by the processor module's user bus control logic.

Software

The ICE-80 software driver (ICE80SD) is a RAM-based program providing easy to use English language commands for defining breakpoints, initiating emulation, and interrogating and altering the user system status recorded during emulation. ICE-80 commands are configured with a broad range of modifiers to provide the user with maximum flexibility in describing the operation to be performed. Listings of emulation commands, interrogation commands, and utility commands are provided in Table 1, Table 2, and Table 3, respectively.

Command	Operation
Go	Initiates real-time emulation and allows user to specify breakpoints, data retrieval, and conditions under which emulation should be reinitiated.
Step	Initiates emulation in single or multiple instruction increments. User may specify register dump or tailor diagnostic activity to his needs following each step, and define conditions under which stepping should continue.
Range	Delimits blocks of instructions for which register dump or tailored diagnostics are to occur.
Continue	Resumes real-time emulation.
Call	Emulates user system interrupt.

Table 1. ICE-80 Emulation Commands

Command	Operation
Base	Establishes mode of display for output data.
Display	Prints contents of memory, 8080 registers, input ports, 8080 flags, 8080 pins, snap data, symbol table, or other diagnostic data on list device. May also be used for base-to-base conversion, or for addition or subtraction in any base.
Change	Alters contents of memory, register, output port, or 8080 flag.
XFORM	Defines memory and I/O status.
Search	Looks through memory range for specified value.

Table 2. ICE-80 Interrogation Commands

Command	Operation
Load	Fetches user symbol table and object code from input device.
Save	Sends user symbol table and object code to output device.
Equate	Enters symbol name and value to user symbol table.
Fill	Fills memory range with specified value.
Move	Moves block of memory data to another area of memory.
Timeout	Enables/disables user CPU ¼ second wait state timeout.
List	Defines list device (diskette-based version only).
Exit	Returns program control to monitor.

Table 3. ICE-80 Utility Commands

SPECIFICATIONS

Paper Tape-Based ICE80SD Operating Environment

Required Hardware
Intellec system
System console
Reader device
Punch device
ICE-80

Required Software
System monitor

Diskette-Based ICE80SD Operating Environment

Required Hardware
Intellec system
32K bytes RAM memory
System console
ISIS MOS floppy disk drive
ICE-80

Required Software
System monitor
ISIS-II Diskette Operating System

System Clock
Crystal controlled 2.185 MHz ± 0.01%. May be replaced by user clock through jumper selection.

Connectors
Edge Connector — CDC VPB01E32A00A1

Physical Characteristics
Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 8.00 lb (3.64 kg)

Electrical Characteristics
DC Power Requirements
V_{CC} = + 5V, ± 5%
I_{CC} = 9.81A max; 6.90A typ
V_{DD} = + 12V, ± 5%
I_{DD} = 79 mA max; 45 mA typ
V_{BB} = − 9V, ± 5%
I_{BB} = 1 mA max; 1μA typ

Environmental Characteristics
Operating Temperature — 0°C to 40°C
Operating Humidity — Up to 95% relative humidity without condensation

Equipment Supplied
Printed circuit modules (2)
Interface cables and buffer board
ICE-80 software driver, paper tape version
(ICE-80 software driver, diskette-based version is supplied with diskette operating systems)

Reference Manuals
9800185 — ICE-80 Operator's Manual (SUPPLIED)
9800556 — Intellec Series II Hardware Reference Manual (SUPPLIED)
9800554 — Intellec Series II Schematic Drawings (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
MDS-80-ICE	8080 CPU in-circuit emulator, cable assembly and interactive software included

ICE-85
MCS-85 IN-CIRCUIT EMULATOR

Connects the Intellec system resources to the user configured system via a 40-pin adaptor plug

Executes user system software in real time

Shares Intellec memory and I/O facilities with user system

Provides 1023 states of 8085 trace data plus 18 additional logic signals via external trace module

Offers full symbolic debugging capability for both assembly language and Intel's high level compiler language, PL/M-80

Displays trace data from user's 8085 in assembler mnemonics and allows personality groupings of data sampled by external 18-channel trace module

Extends ICE capabilities to prototype system peripheral circuitry by allowing user to execute peripheral chip analysis routines

Provides ability to examine and alter MCS-85 registers, memory, flag values, interrupt bits, and I/O ports

The ICE-85 MCS-85 In-Circuit Emulator is an Intellec resident module designed to interface with any user configured 8085 system. In addition, an external trace module provides access to user system peripheral circuitry via a user configured DIP clip for peripheral ICs or may be attached to as many as 18 separate prototype signal nodes via individual probe clips. Using the ICE-85 module, the designer may execute prototype software in real time or single step mode and may substitute Intellec system memory and I/O for their user system equivalents. ICE capability may be extended to the remaining user system peripheral circuitry by allowing the user to create and execute a library of user defined peripheral chip analyzer routines. All user access to the prototype system software may be done symbolically by assigning names to program locations and data, I/O ports, and groups of external trace signals. For the first time, in-ciruit emulation extends beyond a user prototype CPU to the entire user system, allowing in-system emulation.

SYMBOLIC DEBUGGING CAPABILITY

ICE-85 allows the user to make symbolic references to I/O ports, memory addresses and data in his program. Symbols and PL/M statement number may be substituted for numeric values in any of the ICE-85 commands. The user is relieved from looking up addresses of variables or program subroutines.

The user symbol table generated along with the object file during a PL/M-80 compilation or by the ISIS-II 8080/8085 Macro Assembler is loaded into the Intellec® System memory along with the user program which is to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that are found useful during system debugging. By referring to symbol memory addresses, the user can examine, change or break at the intended location.

ICE-85 provides symbolic definition of all 8085 registers, interrupt bits and flags. The following symbolic references are also provided for user convenience: TIMER, the low-order 16 bits of a register containing the number of 2 MHz clock pulses elapsed during emulation; HTIMER, the high-order 16 bits of the timer counter; PPC, the address of the last instruction emulated; BUFFERSIZE, the number of frames of valid trace data (between 0 and 1022).

PERSONALITY GROUPED DISPLAYS

Trace data in the 1023 by 42-channel real-time trace memory buffer is displayed in easy to read format. The user has the option to specify trace data displays in actual 8085 assembler instruction mnemonics. The data collected from the External Trace Module can be grouped and symbolically named according to user specifications and displayed in the appropriate number base designation. Simple ICE-85 commands allow the user to select any portion of the 42K-bit trace buffer for immediate display.

MEMORY AND I/O MAPPING

Memory and I/O for the user system can be resident in the user system or "borrowed" from the Intellec® System through ICE-85's mapping capability.

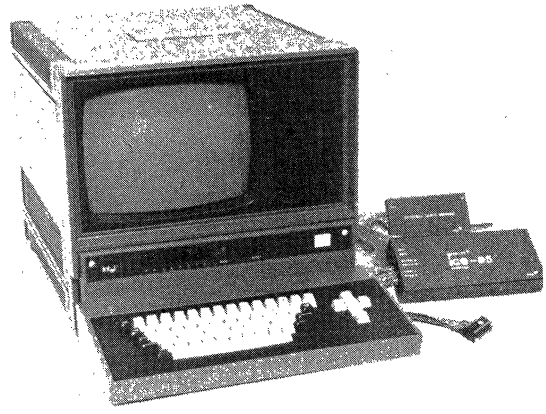
ICE-85 separates user memory into 32 2K blocks. Each block of memory can be defined independently. The user may assign Intellec® System equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, Intellec® System memory or I/O can be accessed in place of suspect user system devices during prototyping or production checkout.

The user can also designate a block of memory or I/O as nonexistent. ICE-85 issues error messages when memory or I/O designated as nonexistent is accessed by the user program.

INTEGRATED HARDWARE/SOFTWARE DEVELOPMENT

The user prototype need consist of no more than an 8085 CPU socket and a user bus to begin integration of software and hardware development efforts. Through ICE-85 mapping capabilities, Intellec® System equivalents can be accessed for missing prototype hardware. Hardware designs can be tested using the system software which will drive the final product.

The system integration phase, which can be so costly when attempting to mesh completed hardware and software products, becomes a convenient two-way debug tool when begun early in the design cycle.



TYPICAL ICE INTERROGATION AND UTILITY COMMANDS

DISPLAY/ CHANGE	Display/Changes the values of symbols and the contents of 8085 registers, pseudo-registers, status flags, interrupt bits, I/O ports and memory.
EVALU-ATE	Displays the value of an expression in the binary, octal, decimal or hexadecimal.
SEARCH	Searches user memory between locations in a user program for specified contents.
CALL	*Emulates* a procedure starting at a specified memory address in user memory.
ICALL	*Executes* a user-supplied procedure starting at a specified memory address in the Intellec® System memory.
EXECUTE	Saves emulated program registers and emulates a user-supplied subroutine to access peripheral chips in the user's system.

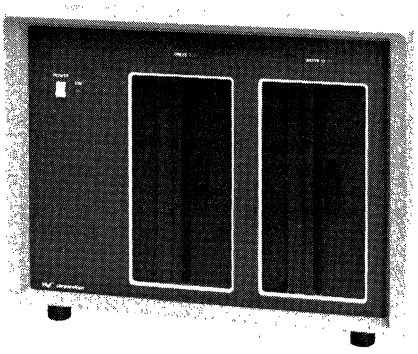
REAL TIME TRACE

ICE-85 captures valuable trace information from the emulating CPU and the External Trace Module while the user is executing programs in real time. The 8085 status, the user memory or port addressed, the data read or written, the serial data lines and data from 18 external signals, is stored for the last 1023 machine states executed (511 machine cycles). This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was user-initiated or the result of an error condition.

For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multi-step sequences tailored to system debug needs.

EXTERNAL TRACE MODULE

TTL level signals from 18 points in the user system may be synchronously sampled by the External Trace Module and collected in ICE-85's trace buffer. The signals can be collected from a single peripheral chip via the supplied 40-pin DIP clip or may be placed by the user on up to 18 separate signal nodes using the supplied 18 individual probe clips. These signals are included in the 42-channel breakpoint comparisons and clock qualifiers. Also, data from these 18 channels may be displayed in each to read, user-defined groupings.



SYNCHRONOUS OPERATION WITH OTHER DESIGN AIDS

ICE-85 can be synchronized with other Intellec® design aids by means of two external synchronization lines. These lines are used to enable and disable ICE-85 trace data collection and to cause break conditions based on an external signal which may not be included in the ICE-85 breakpoint registers. In addition, ICE-85 can generate signals on these lines which may be used to control other design aids.

EMULATION CONTROLS AND COMMANDS

GROUP	Defines into a symbolically named group, a channel or combination of channels from the 8085 Microcprocessor and/or the External Trace Module.
GO	Initiates real-time emulation and controls emulation break conditions.
STEP	Initiates emulation in single instruction steps. User may specify the type and amount of information displayed following each step, and define conditions under which stepping should continue.
PRINT	Prints the user-specified portion of the trace memory to the selected list device.

BREAK REGISTERS/TRACE MEMORY

ICE-85 has two breakpoint registers which are used to break emulation, and two trace qualifier registers which are used to control the collection of trace data during emulation. Each register is 42 entries wide, one entry for each channel and each entry can take any one of the three values 0, 1 or "don't care".

The trace buffer, also 42 entries wide, collects data sampled from 24 8085 processor channels and 18 external channels sampled by the External Trace Module. The signals collected from the 8085 include address lines, data lines, status lines and serial input and output lines. The 18 channels extending from the External Trace Module synchronously sample and collect into the trace buffer any user-specified TTL compatible signal from the rest of the prototype system. "Break" and "trace qualification" may therefore occur as a result of a match of any combination of up to 42 channels of CPU and external circuitry signals.

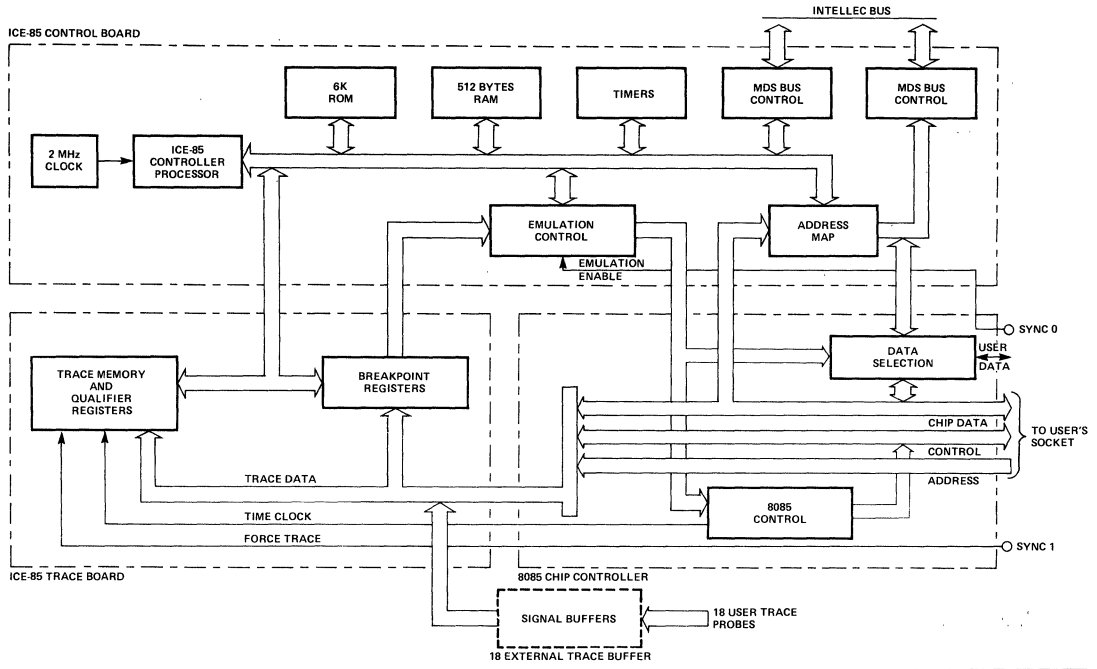


Figure 1. Functional Block Diagram of ICE-85 Module

SPECIFICATIONS

ICE-85 Operating Environment

Required Hardware
Intellec microcomputer development system
System console
Intellec diskette operating system
ICE-85 module

Required Software
System monitor
ISIS-II

Emulation Clock

User's system clock or ICE-85 adaptor socket (6.144 MHz crystal)

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Packaged Weight — 6.00 lb (2.73 kg)

Electrical Characteristics

DC Power Requirements

$V_{CC} = +5V \pm 5\%$
$I_{CC} = 12A$ max; 10A typ
$V_{DD} = +12V \pm 5\%$
$I_{DD} = 80$ mA max; 60 mA typ
$V_{BB} = -10V \pm 5\%$
$I_{BB} = 30$ mA max; 10 μA typ

Environmental Characteristics

Operating Temperature — 0° to 40°C

Operating Humidity — Up to 95% relative humidity without condensation.

Equipment Supplied

18-channel external trace module
Printed circuit boards (2)
Interface cable and emulation buffer module
ICE-85 software, diskette-based version

Reference Manuals

9800463 — ICE-85 Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

MPU SYSTEM

ORDERING INFORMATION

Part Number	Description
MDS-85-ICE	8085 CPU in-circuit emulator and 18-channel external trace module

ICE-86™
8086 IN-CIRCUIT EMULATOR

Hardware in-circuit emulation

Full symbolic debugging

Breakpoints to halt emulation on a wide variety of conditions

Comprehensive trace of program execution, both conditional and unconditional

Disassembly of trace or memory from object code into assembler mnemonics

2K bytes of high speed ICE-86 mapped memory

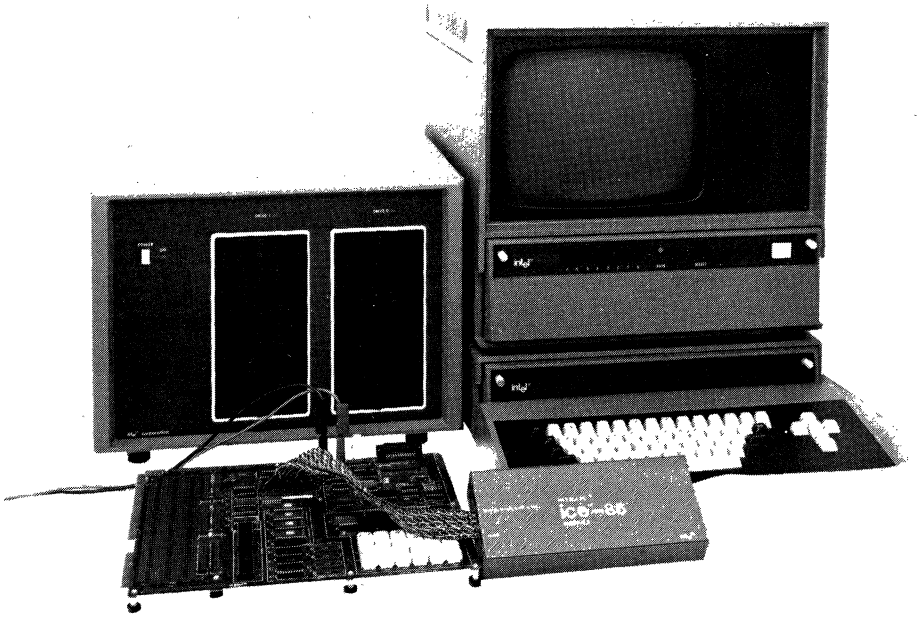
Software debugging with or without user system

Handles full 1 megabyte addressability of 8086

Compound commands

Command macros

The ICE-86 module provides In-Circuit Emulation for the 8086 microprocessor and the iSBC 86/12 Single Board Computer. It includes three circuit boards which reside in Intellec Microcomputer Development Systems. A cable and buffer box connect the Intellec system to the user system by replacing the user's 8086. Powerful Intellec debug functions are thus extended into the user system. Using the ICE-86 module, the designer can execute prototype software in continuous or single-step mode and can substitute blocks of Intellec system memory for user equivalents. Breakpoints allow the user to stop emulation on user-specified conditions, and the trace capability gives a detailed history of the program execution prior to the break. All user access to the prototype system software may be done symbolically by referring to the source program variables and labels.



INTEGRATED HARDWARE/SOFTWARE DEVELOPMENT

The ICE-86 emulator allows hardware and software development to proceed interactively. This is more effective than the traditional method of independent hardware and software development followed by system integration. With the ICE-86 module, prototype hardware can be added to the system as it is designed. Software and hardware testing occurs while the product is being developed.

Conceptually, the ICE-86 emulator assists three stages of development:

1. It can be operated without being connected to the user's system, so ICE-86 debugging capabilities can be used to facilitate program development before any of the user's hardware is available.
2. Integration of software and hardware can begin when any functional element of the user system hardware is connected to the 8086 socket. Through ICE-86 mapping capabilities, Intellec memory, ICE memory, or diskette memory can be substituted for missing prototype memory. Time-critical program modules are debugged before hardware implementation by using the 2K-bytes of high-speed ICE-resident memory. As each section of the user's hardware is completed, it is added to the prototype. Thus each section of the hardware and software is "system" tested as it becomes available.
3. When the user's prototype is complete, it is tested with the final version of the user system software. The ICE-86 module is then used for real time emulation of the 8086 to debug the system as a completed unit.

Thus the ICE-86 module provides the user with the ability to debug a prototype or production system at any stage in its development without introducing extraneous hardware or software test tools.

SYMBOLIC DEBUGGING

Symbols and PL/M statement numbers may be substituted for numeric values in any of the ICE-86 commands. This allows the user to make symbolic references to I/O ports, memory addresses, and data in the user program. Thus the user need not remember the addresses of variables or program subroutines.

Symbols can be used to reference variables, procedures, program labels, and source statements. A variable can be displayed or changed by referring to it by name rather than by its absolute location in memory. Using symbols for statement labels, program labels, and procedure names simplifies both tracing and breakpoint setting. Disassembly of a section of code from either trace or program memory into its assembly mnemonics is readily accomplished.

Furthermore, each symbol may have associated with it one of the data types BYTE, WORD, INTEGER, SINTEGER (for short, 8-bit integer) or POINTER. Thus the user need not remember the type of a source program variable when examining or modifying it. For example, the command "!VAR" displays the value in memory of variable VAR in a format appropriate to its type, while the command "!VAR = !VAR + 1" increments the value of the variable.

The user symbol table generated along with the object file during a PL/M-86 compilation or an ASM-86 assembly is loaded into memory along with the user program which is to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that are found useful during system debugging.

The ICE-86 module provides access through symbolic definition to all of the 8086 registers and flags. The READY, NMI, $\overline{\text{TEST}}$, HOLD, RESET, INTR, and MN/$\overline{\text{MX}}$ pins of the 8086 can also be read. Symbolic references to key ICE-86 emulation information are also provided.

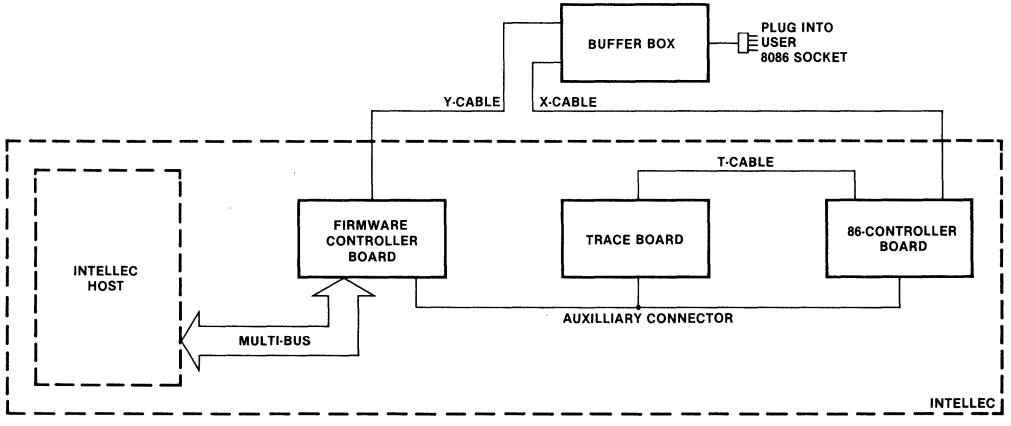
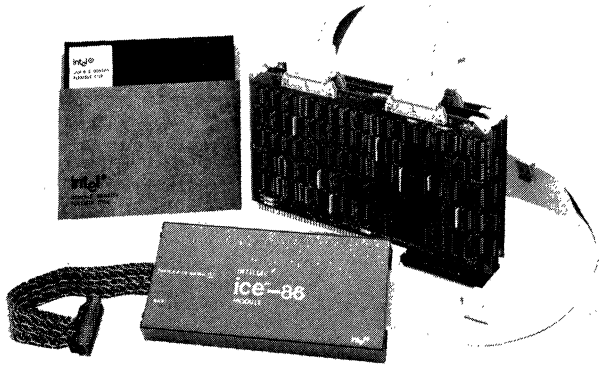


Figure 1. ICE-86 Block Diagram



A typical ICE-86 development configuration. It is based on an MDS-230 Development System, which also includes an MDS-DDS Double Density Diskette Operating System and an MDS-201 Expansion Chassis (which holds the ICE-86 emulator). The ICE-86 module is shown connected to a user prototype system, in this case, an SDK-86.

MACROS AND COMPOUND COMMANDS

The ICE-86 module provides a programmable diagnostic facility which allows the user to tailor its operation using macro commands and compound commands.

A macro is a set of ICE-86 commands which is given a single name. Thus, a sequence of commands which is executed frequently may be invoked simply by typing in a single command. The user first defines the macro by entering the entire sequence of commands which he wants to execute. He then names the macro and stores it for future use. He executes the macro by typing its name and passing up to ten parameters to the commands in the macro. Macros may be saved on a disk file for use in subsequent debugging sessions.

Compound commands provide conditional execution of commands(IF), and execution of commands until a condition is met or until they have been executed a specified number of times (COUNT, REPEAT).

Compound commands and macros may be nested any number of times.

MEMORY MAPPING

Memory for the user system can be resident in the user system or "borrowed" from the Intellec System through ICE-86's mapping capability.

The ICE-86 emulator allows the memory which is addressed by the 8086 to be mapped in 1K-byte blocks to:

1. Physical memory in the user's system,
2. Either of two 1K-byte blocks of ICE-86 high speed memory,
3. Intellec memory,
4. A random-access diskette file.

The user can also designate a block of memory as nonexistent. The ICE-86 module issues an error message when any such "guarded" memory is addressed by the user program.

Command	Description
GO	Initializes emulation and allows the user to specify the starting point and breakpoints. Example: GO FROM .START TILL .DELAY EXECUTED where START and DELAY are statement labels.
STEP	Allows the user to single-step through the program.

Table 1. Summary of ICE-86 Emulation Commands

OPERATION MODES

The ICE-86 software is a RAM-based program that provides the user with easy-to-use commands for initiating emulation, defining breakpoints, controlling trace data collection, and displaying and controlling system parameters. ICE-86 commands are configured with a broad range of modifiers which provide the user with maximum flexibility in describing the operation to be performed.

Emulation

Emulation commands to the ICE-86 emulator control the process of setting up, running and halting an emulation of the user's 8086. Breakpoints and tracepoints enable ICE-86 to halt emulation and provide a detailed trace of execution in any part of the user's program. A summary of the emulation commands is shown in Table 1.

Breakpoints — The ICE-86 module has two breakpoint registers that allow the user to halt emulation when a specified condition is met. The breakpoint registers may be set up for execution or non-execution breaking. An execution breakpoint consists of a single address which causes a break whenever the 8086 executes from its queue an instruction byte which was obtained from

the address. A non-execution breakpoint causes an emulation break when a specified condition other than an instruction execution occurs. A non-execution breakpoint condition, using one or both breakpoint registers, may be specified by any one of or a combination of:

1. *A set of address values.* Break on a set of address values has three valuable features:
   a. Break on a single address.
   b. The ability to set any number of breakpoints within a limited range (1024 bytes maximum) of memory.
   c. The ability to break in an unlimited range. Execution is halted on any memory access to an address greater than (or less than) any 20-bit breakpoint address.
2. *A particular status of the 8086 bus* (one or more of: memory or I/O read or write, instruction fetch, halt, or interrupt acknowledge).
3. *A set of data values* (features comparable to break on a set of address values, explained in point one).
4. *A segment register* (break occurs when the register is used in an effective address calculation).

An external breakpoint match output for user access is provided on the buffer box. This allows synchronization of other test equipment when a break occurs.

Tracepoints — The ICE-86 module has two tracepoint registers which establish match conditions to conditionally start and stop trace collection. The trace information is gathered at least twice per bus cycle, first when the address signals are valid and second when the data signals are valid. If the 8086 execution queue is otherwise active, additional frames of trace are collected.

Each trace frame contains the 20 address/data lines and detailed information on the status of the 8086. The trace memory can store 1,023 frames, or an average of about 300 bus cycles, providing ample data for determining how the 8086 was reacting prior to emulation break. The trace memory contains the last 1,023 frames of trace data collected, even if this spans several separate emulations. The user has the option of displaying each frame of the trace data or displaying by instruction in actual ASM-86 Assembler mnemonics. Unless the user chooses to disable trace, the trace information is always available after an emulation.

Interrogation and Utility

Interrogation and utility commands give the user convenient access to detailed information about the user program and the state of the 8086 that is useful in debugging hardware and software. Changes can be made in both memory and the 8086 registers, flags, input pins, and I/O ports. Commands are also provided for various utility operations such as loading and saving program files, defining symbols and macros, displaying trace data, setting up the memory map, and returning control to ISIS-II. A summary of the basic interrogation and utility commands is shown in Table 2.

Memory/Register Commands

Display or change the contents of:
- Memory
- 8086 Registers
- 8086 Status flags
- 8086 Input pins
- 8086 I/O ports
- ICE-86 Pseudo-Registers (e.g. emulation timer)

Memory Mapping Commands

Display, declare, set, or reset the ICE-86 memory mapping.

Symbol Manipulation Commands

Display any or all symbols, program modules, and program line numbers and their associated values (locations in memory).

Set the domain (choose the particular program module) for the line numbers.

Define new symbols as they are needed in debugging.

Remove any or all symbols, modules, and program statements.

Change the value of any symbol.

TYPE

Assign or change the type of any symbol in the symbol table.

ASM

Disassemble user program memory into ASM-86 Assembler mnemonics.

PRINT

Display the specified portion of the trace memory.

LOAD

Fetch user symbol table and object code from the input file.

SAVE

Send user symbol table and object code to the output file.

LIST

Send a copy of all output (including prompts, input line echos, and error messages) to the chosen output device (e.g. disk, printer) as well as the console.

EVALUATE

Display the value of an expression in binary, octal, decimal, hexadecimal, and ASCII.

SUFFIX/BASE

Establish the default base for numeric values in input text/output display (binary, octal, decimal, or hexadecimal).

CLOCK

Select the internal (ICE-86 provided, for stand-alone mode only) or an external (user-provided) system clock.

RWTIMEOUT

Allows the user to time out READ/WRITE command signals based on the time taken by the 8086 to access Intellec memory or diskette memory.

ENABLE/DISABLE RDY

Enable or disable logical AND of ICE-86 Ready with the user Ready signal for accessing Intellec memory, ICE memory, or diskette memory.

Table 2. Summary of Basic ICE-86 Interrogation and Utility Commands

DIFFERENCES BETWEEN ICE-86 EMULATION AND THE 8086 MICROPROCESSOR

The ICE-86 module emulates the actual operation of the 8086 microprocessor with the following exceptions:

- The ICE-86 module will not respond to a user system NMI or RESET signal when it is out of emulation.
- Trap is ignored in single step mode and on the first instruction step of an emulation.
- The MIN/MAX line, which chooses the "minimum" or "maximum" configuration of the 8086, must not change dynamically in the user system.
- In the "minimum" mode, the user HOLD signal must remain active until HLDA is output by the ICE-86 emulator.
- The $\overline{RQ}/\overline{GT}$ lines in the "maximum" configuration are not supported.

The speed of run emulation by the ICE-86 module depends on where the user has mapped his memory. As the user prototype progresses to include memory, emulation becomes real time.

Memory Mapped To	Estimated Speed
User System	100% of real time*, up to 4 MHz clock
ICE	2 wait states per 8086-controlled bus cycle
Intellec	Approximately 0.02% of real time at 4 MHz clock
Diskette	**

*100% of real time is emulation at the user system clock rate with no wait states.

**The emulation speed from diskette is comparable to Intellec memory, but emulation must wait when a new page is accessed on the diskette.

DC CHARACTERISTICS OF ICE-86 USER CABLE

1. Output Low Voltages [V_{OL}(Max) = 0.4V]

	I_{OL} (Min)
AD0-AD15	12 mA (24 mA @ 0.5V)
A16/S3-A19/S7, $\overline{BHE}$/S7, $\overline{RD}$, $\overline{LOCK}$, QS0, QS1, $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{WR}$, M/$\overline{IO}$, DT/$\overline{R}$, $\overline{DEN}$, ALE, $\overline{INTA}$	8 mA (16 mA @ 0.5V)
HLDA	7 mA
$\overline{MATCH0\ OR\ MATCH1}$ (on buffer box)	16 mA

2. Output High Voltages [V_{OH} (Min) = 2.4V]

	I_{OH}(Min)
AD0-AD15	– 3 mA
A16/S3-A19/S7, $\overline{BHE}$/S7, $\overline{RD}$, $\overline{LOCK}$, QS0, QS1, $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{WR}$, M/$\overline{IO}$, DT/$\overline{R}$, $\overline{DEN}$, ALE, $\overline{INTA}$	– 2.6 mA
HLDA	– 3.0 mA
$\overline{MATCH0\ OR\ MATCH1}$ (on buffer box)	– 0.8 mA

3. Input Low Voltages [V_{IL}(Max) = 0.8V]

	I_{IL} (Max)
AD0-AD15	– 0.2 mA
NMI, CLK	– 0.4 mA
READY	– 0.8 mA
INTR, HOLD, $\overline{TEST}$, RESET	– 1.4 mA
MN/$\overline{MX}$ (0.1 μf to GND)	– 3.3 mA

4. Input High Voltages [V_{IH}(Min) = 2.0V]

	I_{IH}(Max)
AD0-AD15	80 μA
NMI, CLK	20 μA
READY	40 μA
INTR, HOLD, $\overline{TEST}$, RESET	– 0.4 mA
MN/$\overline{MX}$ (0.1 μF to GND)	– 1.1 mA

5. $\overline{RQ}/\overline{GT0}$, $\overline{RQ}/\overline{GT1}$ are pulled up to + 5V through a 5.6K ohm resistor. No current is taken from user circuit at V_{CC} pin.

SPECIFICATIONS

ICE-86 Operating Environment

Required Hardware

Intellec microcomputer development system with:

1. Three adjacent slots for the ICE-86 module. (Series II requires MDS-201 Expansion Chassis).
2. 64K bytes of Intellec memory. If user prototype program memory is desired, additional memory above the basic 64K is required.

System console
Intellec diskette operating system
ICE-86 module

Required Software

System monitor
ISIS-II, version 3.4 or subsequent
ICE-86 software

Equipment Supplied

Printed circuit boards (3)
Interface cable and emulation buffer module
Operator's manual
ICE-86 software, diskette-based

Emulation Clock

User system clock up to 4 MHz or 2 MHz ICE-86 internal clock in stand-alone mode

Physical Characteristics

Printed Circuit Boards

Width: 12.00 in (30.48 cm)
Height: 6.75 in (17.15 cm)
Depth: 0.50 in (1.27 cm)
Packaged Weight: 9.00 lb (4.10 kg)

Electrical Characteristics

DC Power

$V_{CC} = +5V +5\% -4\%$
$I_{CC} = 15A$ maximum; 11A typical
$V_{DD} = +12V \pm 5\%$
$I_{DD} = 120$ mA maximum; 80 mA typical
$V_{BB} = -10V \pm 5\%$ or $-12V \pm 5\%$ (optional)
$I_{BB} = 15$ mA maximum; 12 mA typical

Environmental Characteristics

Operating Temperature: 0° to 40°C

Operating Humidity: Up to 95% relative humidity without condensation.

ORDERING INFORMATION

Part Number	Description
MDS-86-ICE	8086 CPU in-circuit emulator

EM1
8021 EMULATION BOARD

EPROM functional equivalent of 8021 — single component 8-bit microcomputer

Based on 8748 — user programmable/ erasable EPROM 8-bit computer

Operates with ICE-49™ to provide full in-circuit debugging of 8021 prototype system

Connects to prototype system through 8021 pin compatible plug

On-card 3.0 MHz or external TTL driven clock

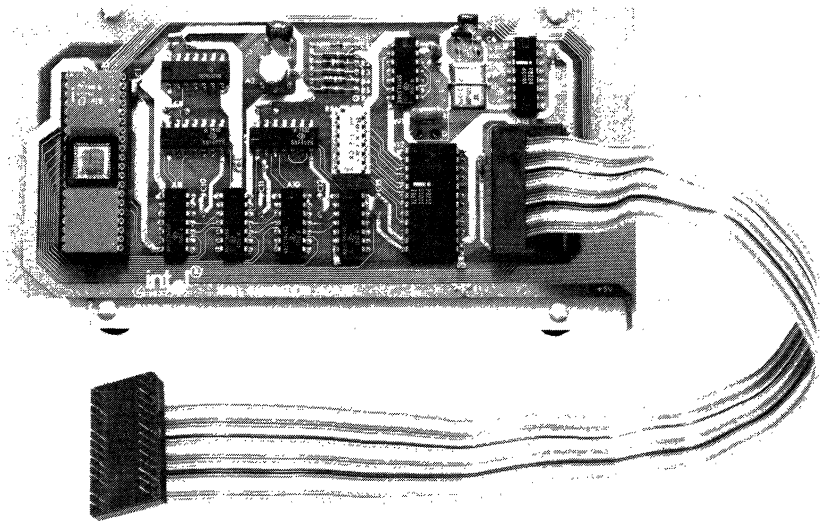
Portable 4″ x 7″ microcomputer circuit assembly

The MDS-EM1 emulator board is a ready-to-use 4″ × 7″ microcomputer circuit assembly that emulates the Intel 8021 microcomputer. A 12-inch flat-cable assembly connects the board to the 8021 socket in a prototype system. The board is designed so that it can be mounted either as a stand-alone unit or within the prototype assembly.

The 8021 microcomputer has 1K × 8 mask programmable ROM program memory and 64 × 8 RAM data memory. The EM1 is controlled by an Intel 8748, with 1K of EPROM program memory and a 64-byte data memory. The EPROM can be programmed and erased repeatedly during hardware and software development. The EM1 has several ancillary circuits that perform the following functions which are specific to the 8021:

Zero crossing detector
Crystal controlled clock/buffer
Port 0 simulator

For prototype debugging, the 8748 can be removed from its socket and replaced with a cable to an Intel ICE-49. When used with the EM1, ICE-49 emulates the 8021 in real time, or single steps the 8021 program at the user's command. A full range of capabilities for examining and modifying 8021 memory and status are supplied through ICE-49.



HARDWARE

The EM1 emulation board uses the 8748 to perform the emulation.

P0 Simulator

Port 0 of the 8021 is a quasi-bidirectional* port. The P0 simulator converts the data bus of the 8748 into a quasi-bidirectional port.

Crystal Control Clock Buffer

The EM1 allows the user to select an on-board oscillator or a TTL clock driven from the 8021 user's prototype system via a Cambion Suitcase jumper.

Jumper	Position	State
W1	A-B	On-Board
	C-D	External TTL Clock

*A bidirectional port which serves as an input port, output port, or both, even though outputs are statically latched.

Zero Cross Detection Simulator

The zero cross detection simulator enables the 8748's T1 input to detect zero-crossings. The circuitry provides a high level signal on a positive crossing and a low level signal on a negative crossing of zero to the T1 input of the 8748.

Reset Buffer

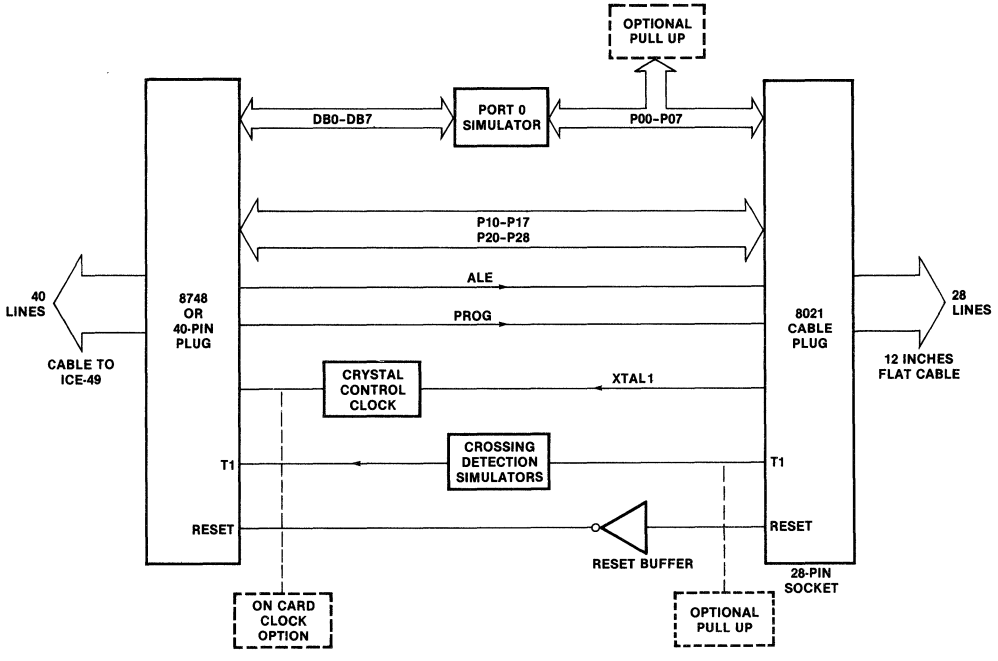
The 8021 resets on a logic HIGH level signal. However, the 8748 resets on a logic LOW level, thus an inverter is provided on the MDS-EM1 to make the two chips compatible.

Optional Pull Ups

Resistors are provided to simulate the optional pull-up resistors on T1 input and port 0 of the 8021. A removable resistor pack is used on port 0. The T1 input pull up can be installed by soldering in a 50K resistor.

SOFTWARE

When emulating the 8021 with EM1 the user must observe the 8021 instruction set.



EM1 FUNCTION DIAGRAM

SPECIFICATIONS

Operating Environment

Stand-Alone Required Hardware

EM1 emulation board

In-Circuit Emulation Required Hardware

EM1 emulation board

Intellec Microcomputer Development System configured to support ICE-49

Equipment Supplied

EM1 printed circuit board

12″ long flat cable terminating in 28-pin plug, pin compatible with 8021

EM1 Operator's Manual

System Clock

Crystal controlled 3.0 MHz on board or user supplied TTL external clock: hardware jumper selectable

Physical Characteristics

Width: 7.0 in. (17.78 cm)
Height: 4.0 in. (10.16 cm)
Depth: 0.75 in. (1.91 cm)
Weight: <1.0 lb (0.45 kg)

Electrical Characteristics

DC Power

$V_{CC} = 5V \pm 5\%$

$I_{CC} = 300$ mA (max)

Environmental Characteristics

Operating Temperature—0°C to 55°C

Operating Humidity—Up to 95% relative humidity without condensation

ORDERING INFORMATION

Part Number	Description
MDS-EM1	8021 Emulation Board

EM2
8022 EMULATION BOARD

Portable 4.25″ x 2.75″ microcomputer circuit assembly

Connects directly into prototype system through Intel® 8022* pin compatible socket

Provides Intel® 8755A — 2K x 8 EPROM

EPROM functional and electrical equivalent of Intel® 8022 — single component 8-bit computer

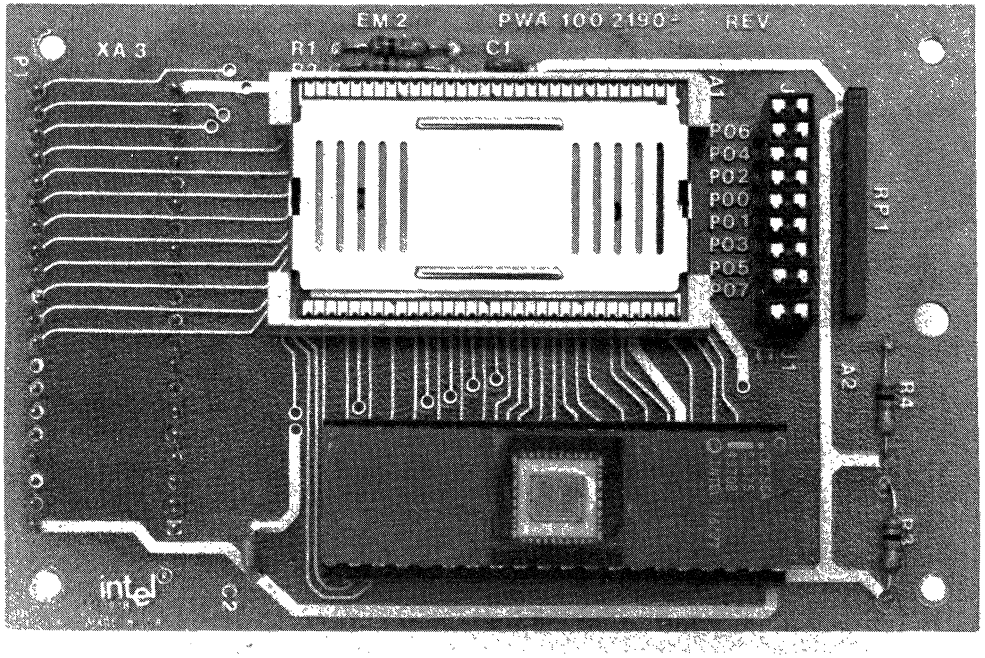
The EM2 emulator board is a ready-to-use 4.25″ x 2.75″ microcomputer circuit assembly that emulates the Intel® 8022 single chip microcomputer. The emulator board is designed to plug directly into the 8022 socket. No interfacing and interconnection cables are necessary. Power is obtained from the user's system.

The EM2 emulator board provides the user a full EPROM functional and electrical equivalent of the 8022 single component 8-bit microcomputer.

The EM2 emulator board consists of an Intel® 8022 emulator chip and an Intel® 8755A, providing the EM2 emulator board with a 2K x 8 EPROM program memory which can be programmed and erased repeatedly during hardware and software development.

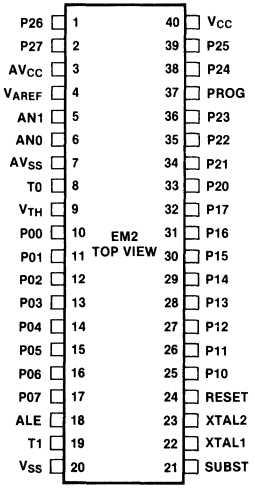
The 8022E emulator chip is a modified version of the 8022 intended for use in design support systems. Instead of using resident ROM memory as the 8022, the 8022E uses an external 2K EPROM 8755A memory for program storage, allowing easy program modification.

*See Intel® 8022 Data Sheet.

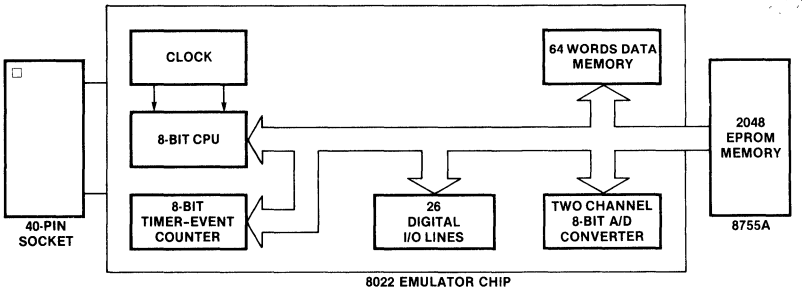


MPU SYSTEM

40-PIN SOCKET CONFIGURATION



EM2 BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential.
V_{CC}	40	+5V circuit power supply.
PROG	37	Output strobe for Intel® 8243 I/O expander.
P00–P07 Port 0	10–17	8-bit open-drain port with comparator inputs. The switching threshold is set externally by V_{TH}. Optional pull-up resistors may be added via ROM mask selection. (The emulator board has switch selection of this option.)
V_{TH}	9	Port 0 threshold reference pin.
P10–P17 Port 1	25–32	8-bit quasi-bidirectional port.
P20–P27	33–36	8-bit quasi-bidirectional port.
Port 2	38–39 1–2	P20–P23 also serve as a 4-bit I/O expander for Intel® 8243.
T0	8	Interrupt input and input pin testable using the conditional transfer instructions JT0 and JNT0. Initiates an interrupt following a low level input if interrupt is enabled. Interrupt is disabled after a reset.
T1	19	Input pin testable using the JT1 and JNT1 conditional transfer instructions. Can be designated the timer/event counter input using the STRT CNT instruction. Also serves as the zero-cross detection input to allow zero-crossover sensing of slowly moving AC inputs. Optional pull-up resistor may be added via ROM mask selection.
RESET	24	Input used to initialize the processor by clearing status flip-flops and setting the program counter to zero.
AV_{SS}	7	A/D converter GND potential. Also establishes the lower limit of the conversion range.
AV_{CC}	3	A/D +5V power supply.
SUBST	21	Substrate pin used with a bypass capacitor to stabilize the substrate voltage and improve A/D accuracy.
V_{AREF}	4	A/D converter reference voltage. Establishes the upper limit of the conversion range.
AN0, AN1	6,5	Analog inputs to A/D converter. Software selectable on-chip via SEL AN0 and SEL AN1 instructions.
ALE	18	Address Latch Enable. Signal occurring once every 30 input input clocks (once every single cycle instruction), used as an output clock.
XTAL1	22	One side of crystal, inductor, or resistor input for internal oscillator. Also input for external frequency source. (Not TTL compatible.)
XTAL2	23	Other side of timing control element. This pin is not connected when an external frequency source is used.

On the EM2 Board:

The Intel® 8755A EPROM can be programmed using any of the modules listed in Table 1.

Module	Description
UPP-103	Universal PROM Programmer. Requires UPP-955, which includes 8755A Personality Card with 40-pin adapter socket.
PROMPT-48	Intellec® MCS-48 Microcomputer Design Aid. Requires PROMPT-475 Programming Adapter.
PROMPT-80/85	Intellec® 8080/8085 Microcomputer Design Aid. Requires PROMPT-975 Programming Adapter.

Table 1. 8755A Proramming Module

The 8755A EPROM is erased when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). Sunlight and certain fluorescent lamps have wavelengths in the 3000Å to 4000Å range. If the 8755A is to be exposed to sunlight or room fluorescent lighting for extended periods, then opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light which has a wavelength of 2537Å. The integrated dose (UV intensity multiplied by exposure time) for erasure should be a minimum of 15W-sec/cm. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000μ W/em^2 power rating. Place the 8755A within one inch of the lamp during erasure. Some lamps include a filter which should be removed before erasure.

SPECIFICATIONS

Operating Environment

Intel® 8755A EPROM Programming

UPP-103
PROMPT-48
PROMPT-80/85

Intellec Microcomputer Development System

Software

8048 Assembler
ISIS-II Diskette Operating System

Equipment Supplied

EM2 Printed Circuit Board
EM2 Reference Manual

Physical Characteristics

Width: 2.75 in. (6.98 cm)
Height: 4.25 in. (10.79 cm)
Depth: 1.5 in. (3.81 cm)
Weight: 0.5 lb (0.23 kg)

Electrical Characteristics

DC Power

$V_{CC} = 5V \pm 5\%$
$I_{CC} = 300$ mA (maximum)

Environmental Characteristics

Operating Temperature — 0 to 55°C

Operating Humidity — Up to 95% relative humidity without condensation

ORDERING INFORMATION

Part Number	Description
MDS-EM2	8022 Emulation Board

UPP-103*
UNIVERSAL PROM PROGRAMMER

Replaces UPP-101, UPP-102 Universal PROM Programmers

Intellec development system peripheral for PROM programming and verification

Provides personality cards for programming all Intel PROM families

Provides zero insertion force sockets for both 16-pin and 24-pin PROMs

Universal PROM mapper software provides powerful data manipulation and programming commands

Provides flexible power source for system logic and programming pulse generation

Holds two personality cards to facilitate programming operations using several PROM types

The UPP-103 Universal PROM Programmer is an Intellec system peripheral capable of programming and verifying the following Intel programmable ROMs (PROMs): 1702A, 2704, 2708, 2716, 3601, 8702A, 8704, and 8708. In addition, the UPP-103 programs the PROM memory portions of the 8748 microcomputer and the 8755 PROM and I/O chip. Programming and verification operations are initiated from the Intellec development system console and are controlled by the universal PROM mapper (UPM) program.

FUNCTIONAL DESCRIPTION

Universal PROM Programmer

The basic Universal PROM Programmer (UPP) consists of a controller module, two personality card sockets, a front panel, power supplies, a chassis, and an Intellec development system interconnection cable. An Intel 4040-based intelligent controller monitors the commands from the Intellec System and controls the data transfer interface between the selected PROM personality card and the Intellec memory. A unique personality card contains the appropriate pulse generation functions for each Intel PROM family. Programming and verifying any Intel PROM may be accomplished by selecting and plugging in the appropriate personality card. The front panel contains a power-on switch and indicator, a reset switch, and two zero-force insertion sockets (one 16-pin and one 24-pin or two 24-pin). A central power supply provides power for system logic and for PROM programming pulse generation. The Universal PROM Programmer may be used as a table top unit or mounted in a standard 19-inch RETMA cabinet.

Universal PROM Mapper

The Universal PROM Mapper (UPM) is the software program used to control data transfer between paper tape or diskette files and a PROM plugged into the Universal PROM Programmer. It uses Intellec system memory for intermediate storage. The UPM transfers data in 8-bit HEX, BNPF, or binary object format between paper tape or diskette files and the Intellec system memory. While the data is in Intellec system memory, it can be displayed and changed. In addition, word length, bit position, and data sense can be adjusted as required for the PROM to be programmed. PROMs may also be duplicated or altered by copying the PROM contents into the Intellec system memory. Easy to use program and compare commands give the user complete control over programming and verification operations. The UPM eliminates the need for a variety of personalized PROM programming routines because it contains the programming algorithms for all Intel PROM families.

Optional Versions

There are two versions of the UPM: one that runs under the Intellec system monitor (paper tape system), and one that runs under ISIS-II, the Intellec diskette operating system (diskette-based system). The paper tape version is included with the Universal PROM Programmer. The diskette-based version of the UPM is available on all ISIS-II system diskettes.

SPECIFICATIONS

Hardware Interface

Data — Two 8-bit unidirectional buses

Commands — 3 write commands, 2 read commands, one initiate command

Physical Characteristics

Width — 6 in. (14.7 cm)

Height — 7 in. (17.2 cm)

Depth — 17 in. (41.7 cm)

Weight — 18 lb (8.2 kg)

Electrical Characteristics

AC Power Requirements — 50–60 Hz; 115/230V AC: 80W

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Optional Equipment

Personality Cards

UPP-361: 3601 personality card

UPP-816: 2716 personality card

UPP-832: 2732 personality card

UPP-848: 8748 personality card with 40-pin adaptor socket

UPP-855: 8755 personality card with 40-pin adaptor socket

UPP-865: 3602, 3622, 3602A, 3622A, 3621, 3604, 3624, 3604A, 3624A, 3604AL, 36046-6, 3605, 3625, 3608, 3628

UPP-872: 8702A/1702A personality card

UPP-878: 8708/8704/2708/2704 personality card

PROM Programming Sockets

UPP-501: 16-pin/24-pin socket pair

UPP-502: 24-pin/24-pin socket pair

UPP-562: Socket adaptor for 3621, 3602, 3622, 3602A, 3622A

UPP-555: Socket adaptor for 3604AL, 36046-6, 3608, 3628

UPP-566: Socket adaptor for 3605, 3625

Equipment Supplied

Cabinet

Power supplies

4040 intelligent controller module

Specified zero insertion force socket pair

Intellec development system interface cable

Universal PROM Mapper program (paper tape version — disk-based version available on ISIS-II diskettes)

Reference Manuals

9800133 — Universal PROM Programmer Hardware Reference Manual (SUPPLIED)

9800554 — Intellec Series II Schematics Drawings (SUPPLIED)

9800819 — Universal PROM Programmer User's Manual (SUPPLIED)

ORDERING INFORMATION

Part Number	Description
UPP-103	Universal PROM programmer with 16-pin/24-pin socket pair and 24-pin/24-pin socket pair

SDK-85
MCS-85 SYSTEM DESIGN KIT

Complete single board microcomputer system including CPU, memory, and I/O

Easy to assemble, low cost, kit form

Extensive system monitor software in ROM

Interactive LED display and keyboard

Large wire-wrap area for custom interfaces

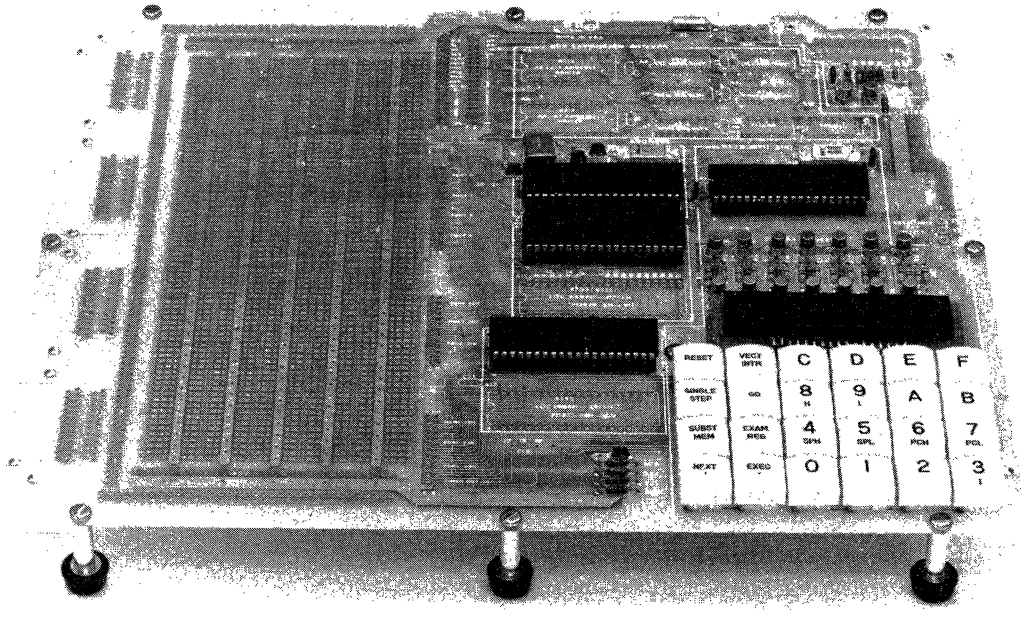
Popular 8080A instruction set

Interfaces directly with TTY

High performance 3 MHz 8085A CPU (1.3 μs instruction cycle)

Comprehensive design library included

The SDK-85 MCS-85 System Design Kit is a complete single board microcomputer system in kit form. It contains all components required to complete construction of the kit, including LED display, keyboard, resistors, caps, crystal, and miscellaneous hardware. Included is a preprogrammed ROM containing a system monitor for general software utilities and system diagnostics. The complete kit includes a 6-digit LED display and a 24-key keyboard for a direct insertion, examination, and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal. The SDK-85 is an inexpensive, high performance prototype system that has designed-in flexibility for simple interface to the user's application.



MPU SYSTEM

FUNCTIONAL DESCRIPTION

The SDK-85 is a complete 8085A microcomputer system on a single board, in kit form. It contains all necessary components to build a useful, functional system. Such items as resistors, capacitors, and sockets are included. Assembly time varies from three to five hours, depending on the skill of the user. The SDK-85 functional block diagram is shown in Figure 1.

8085A Processor

The SDK-85 is designed around Intel's 8085A microprocessor. The Intel 8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software upward compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's: 8085A (CPU), 8156 (RAM), and 8355/8755 (ROM/PROM). A block diagram of the 8085A microprocessor is shown in Figure 2.

System Integration — The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

Addressing — The 8085A uses a multiplexed data bus. The 16-bit address is split between the 8-bit address bus and the 8-bit address/data bus. The on-chip address latches of 8155/8156/8355/8755 memory products allows a direct interface with the 8085A.

System Monitor

A compact but powerful system monitor is supplied with the SDK-85 to provide general software utilities and system diagnostics. It comes in a pre-programmed ROM.

Communications Interface

The SDK-85 communicates with the outside world through either the on-board LED display/keyboard combination, or the user's TTY terminal (jumper selectable).

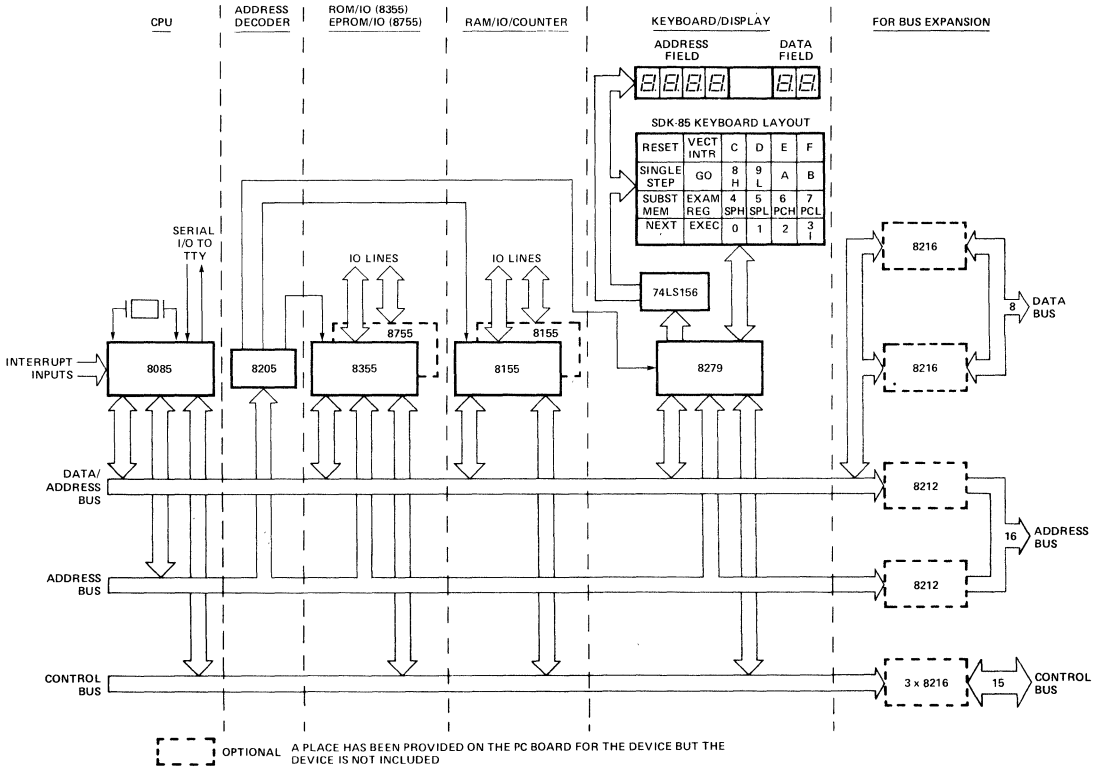
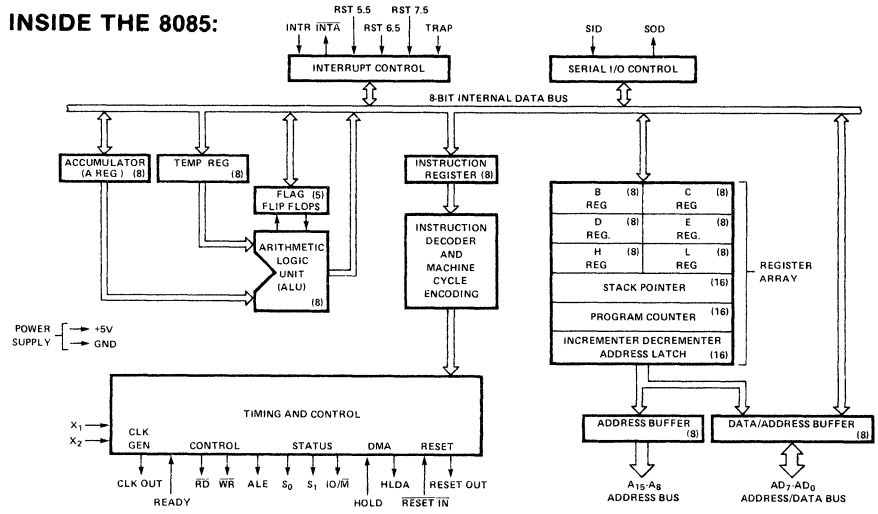


Figure 1. SDK-85 System Design Kit Functional Block Diagram



- SEVEN 8-BIT REGISTERS. SIX OF THEM CAN BE LINKED IN REGISTER PAIRS FOR CERTAIN OPERATIONS.
- 8-BIT ALU.
- 16-BIT STACK POINTER (STACK IS MAINTAINED OFFBOARD IN SYSTEM RAM MEMORY).
- 16-BIT PROGRAM COUNTER.

Figure 2. 8085A Microprocessor Block Diagram

Both memory and I/O can be easily expanded by simply soldering in additional devices in locations provided for this purpose. A large area of the board (45 sq. in.) is laid out as general purpose wire-wrap for the user's custom interfaces.

Assembly

Only a few simple tools are required for assembly; soldering iron, cutters, screwdriver, etc. The SDK-85 user's manual contains step-by-step instructions for easy assembly without mistakes. Once construction is complete, the user connects his kit to a power supply and the SDK-85 is ready to go. The monitor starts immediately upon power-on or reset.

Command	Operation
Reset	Starts monitor.
Go	Allows user to execute user program.
Single step	Allows user to execute user program one instruction at a time—useful for debugging.
Substitute memory	Allows user to examine and modify memory locations.
Examine register	Allows user to examine and modify 8085A's register contents.
Vector interrupt	Serves as user interrupt button.

Table 1. Keyboard Monitor Commands

Commands — Keyboard monitor commands and teletype monitor commands are provided in Table 1 and Table 2, respectively.

Command	Operation
Display memory	Displays multiple memory locations.
Substitute memory	Allows user to examine and modify memory locations one at a time.
Insert instructions	Allows user to store multiple bytes in memory.
Move memory	Allows user to move blocks of data in memory.
Examine register	Allows user to examine and modify the 8085A's register contents.
Go	Allows user to execute user programs.

Table 2. Teletype Monitor Commands

Documentation

In addition to detailed information on using the monitors, the SDK-85 user's manual provides circuit diagrams, a monitor listing, and a description of how the system works. The complete design library for the SDK-85 is shown in Figure 3 and listed in the Specifications section under Reference Manuals.

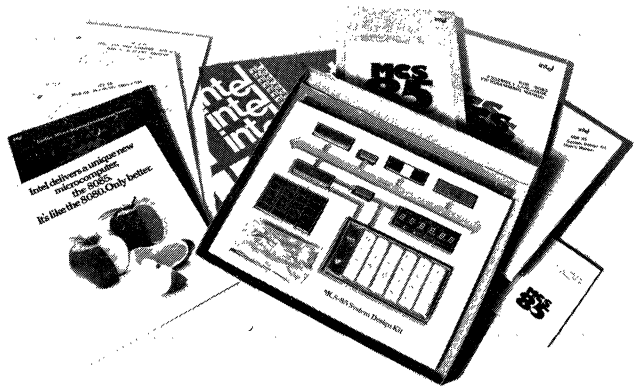


Figure 3. SDK-85 Design Library

8085A INSTRUCTION SET

Table 3 contains a summary of processor instructions used for the 8085A microprocessor.

Mnemonic	Description	Instruction Code[2] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[3] Cycles
MOVE, LOAD, AND STORE										
MOVr1r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
STAX B	**Store A indirect**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**7**
STAX D	**Store A indirect**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**7**
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E, H & L registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6

Mnemonic[1]	Description	Instruction Code[2] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[3] Cycles
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12

continued

Mnemonic[1]	Description	Instruction Code[2] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[3] Cycles
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7

Mnemonic[1]	Description	Instruction Code[2] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[3] Cycles
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupts	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
NEW 8085 INSTRUCTIONS										
RIM	Read interrupt mask	0	0	1	0	0	0	0	0	4
SIM	Set interrupt mask	0	0	1	1	0	0	0	0	4

Notes

1. All mnemonics copyright © Intel Corporation 1977.
2. DDD or SSS: B = 000, C = 001, D = 010, E = 011, H = 100, L = 101, Memory = 110, A = 111.
3. Two possible cycle times. (6/12) indicates instruction cycles dependent on condition flags.

Table 3. Summary of 8085A Processor Instructions

SPECIFICATIONS

Central Processor

CPU — 8085A

Instruction Cycle — 1.3 μs

Tcy — 330 ns

Memory

ROM — 2K bytes (expandable to 4K bytes) 8355/8755A

RAM — 256 bytes (expandable to 512 bytes) 8155

Addressing

ROM — 0000-07FF (expendable to 0FFF with an additional 8355/8755A)

RAM — 2000-20FF (2800-28FF available with an additional 8155)

Note

The wire-wrap area of the SDK-85 PC board may be used for additional custom memory expansion up to the 64K-byte addressing limit of the 8085A.

Input/Output

Parallel — 38 lines (expandable to 76 lines)

Serial — Through SID/SOD ports of 8085A. Software generated baud rate.

Baud Rate — 110

Interfaces

Bus — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Serial I/O — 20 mA current loop TTY

Note
By populating the buffer area of the board, the user has access to all bus signals that enable him to design custom system expansions into the kit's wire-wrap area.

Interrupts

Three Levels
(RST 7.5) — Keyboard interrupt
(RST 6.5) — TTL input
(INTR) — TTL input

DMA

Hold Request — Jumper selectable. TTL compatible input.

Software

System Monitor — Pre-programmed 8755A or 8355 ROM
Addresses — 0000-07FF
Monitor I/O — Keyboard/display or TTY (serial I/O)

Physical Characteristics

Width — 12.0 in. (30.5 cm)
Height — 10 in. (25.4 cm)
Depth — 0.50 in. (1.27 cm)
Weight — approx. 12 oz

Electrical Characteristics

DC Power Requirement (power supply not included in kit)

Voltage	Current
V_{CC} 5V ±5%	1.3A
V_{TTY} – 10V ± 10%	0.3A (V_{TTY} required only if teletype is connected)

Environmental Characteristics

Operating Temperature — 0-55°C

Reference Manuals

9800451 — SDK-85 User's Manual (SUPPLIED)

9800366 — MCS-85 User's Manual (SUPPLIED)

9800301 — 8080/8085 Assembly Language Programming Manual (SUPPLIED)

8085/8080 Assembly Language Reference Card (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SDK-85	MCS-85 system design kit

SDK-86
MCS-86 SYSTEM DESIGN KIT

Complete single board microcomputer system including CPU, memory, and I/O

Easy to assemble kit form

High performance 8086 16-bit CPU

Interfaces directly with TTY or CRT

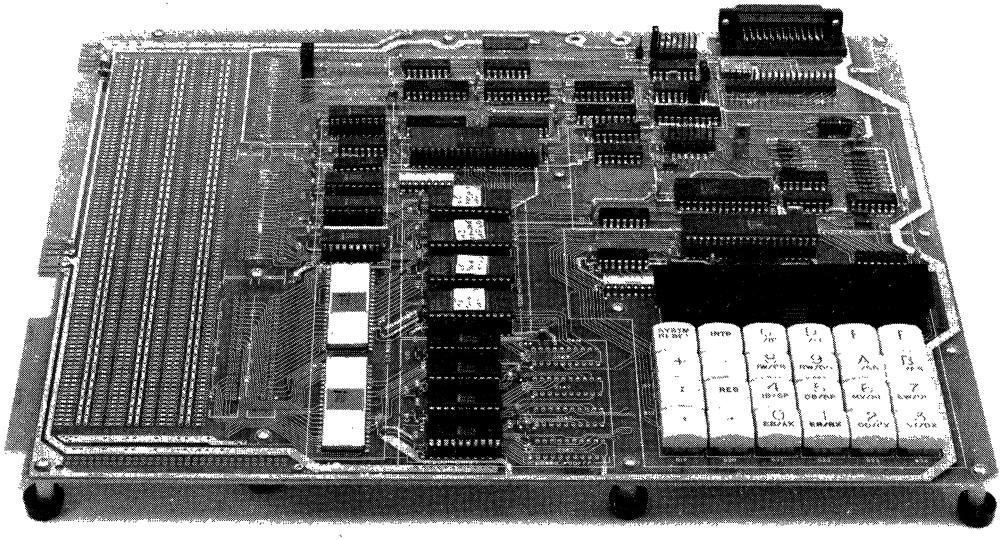
Interactive LED display and keyboard

Wire wrap area for custom interfaces

Extensive system monitor software in ROM

Comprehensive design library included

The SDK-86 MCS-86 System Design Kit is a complete single board 8086 microcomputer system in kit form. It contains all necessary components to complete construction of the kit, including LED display, keyboard, resistors, caps, crystal, and miscellaneous hardware. Included are preprogrammed ROMs containing a system monitor for general software utilities and system diagnostics. The complete kit includes an 8-digit LED display and a mnemonic 24-key keyboard for direct insertion, examination, and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal, CRT terminal, or the serial port of an Intellec system. The SDK-86 is a high performance prototype system with designed-in flexibility for simple interface to the user's application.



FUNCTIONAL DESCRIPTION

The SDK-86 is a complete MCS-86 microcomputer system on a single board, in kit form. It contains all necessary components to build a useful, functional system. Such items as resistors, caps, and sockets are included. Assembly time varies from 4 to 10 hours, depending on the skill of the user. The SDK-86 functional block diagram is shown in Figure 1.

8086 Processor

The SDK-86 is designed around Intel's 8086 microprocessor. The Intel 8086 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor features attributes of both 8-bit and 16-bit microprocessors in that it addresses memory as a sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance. Additional features of the 8086 include the following:

- Direct addressing capability to one megabyte of memory
- Assembly language compatibility with 8080/8085
- 14 word x 16-bit register set with symmetrical operations
- 24 operand addressing modes
- Bit, byte, word, and block operations
- 8 and 16-byte signed and unsigned arithmetic in binary or decimal mode, including multiply and divide
- 5 MHz clock rate
- MULTIBUS compatible system interface

A block diagram of the 8086 microprocessor is shown in Figure 2.

System Monitor

A compact but powerful system monitor is supplied with the SDK-86 to provide general software utilities and system diagnostics. It comes in preprogrammed read only memories (ROMs).

Communications Interface

The SDK-86 communicates with the outside world through either the on-board light emitting diode (LED) display/keyboard combination or the user's TTY or CRT terminal (jumper selectable), or by means of a special mode in which an Intellec development system transports finished programs to and from the SDK-86. Memory may be easily expanded by simply soldering in additional devices in locations provided for this purpose. A large area of the board (22 square inches) is laid out as general purpose wire-wrap for the user's custom interfaces.

Assembly

Only a few simple tools are required for assembly: soldering iron, cutters, screwdriver, etc. The SDK-86 assembly manual contains step-by-step instructions for easy assembly with a minimum of mistakes. Once construction is complete, the user connects his kit to a power supply and the SDK-86 is ready to go. The monitor starts immediately upon power-on or reset.

Commands — Keyboard mode commands, serial port commands, and Intellec slave mode commands are summarized in Table 1, Table 2, and Table 3, respectively. The SDK-86 keyboard is shown in Figure 3.

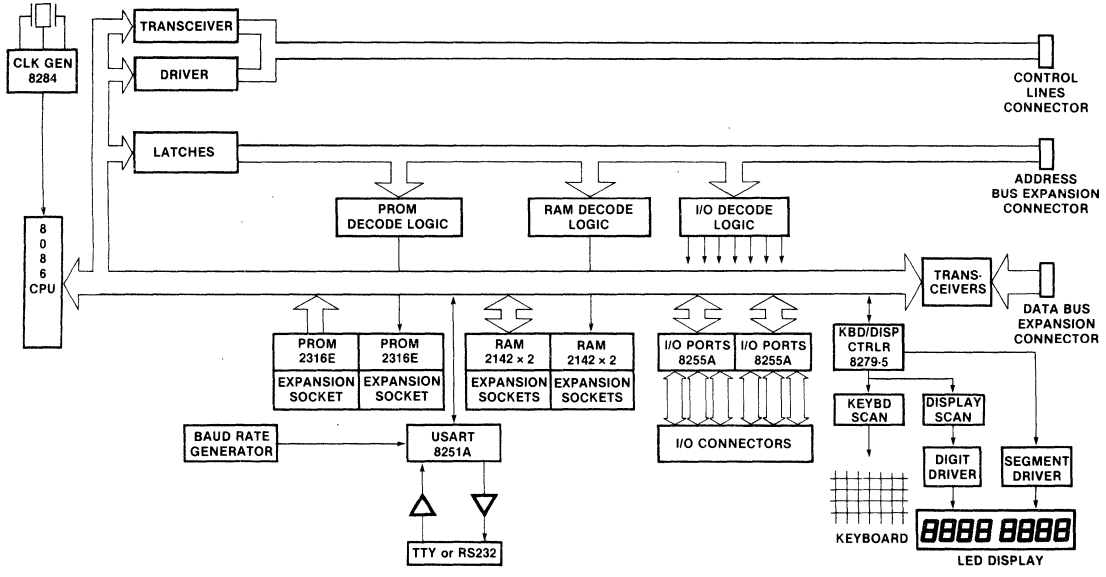


Figure 1. SDK-86 System Design Kit Functional Block Diagram

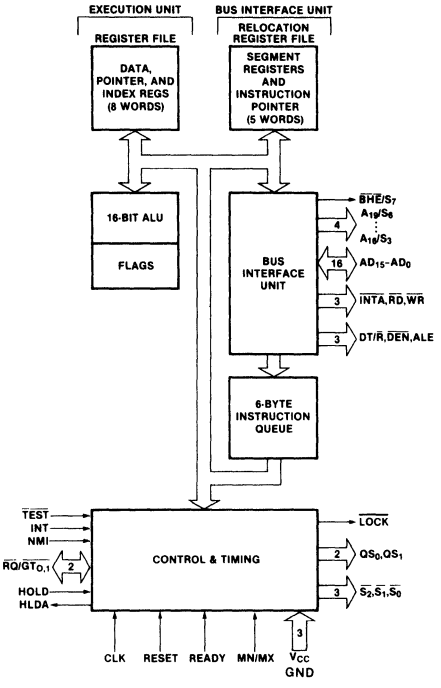


Figure 2. 8086 Microprocessor Block Diagram

SYSTM RESET	INTR	C /IP	D /FL	E	F
+	–	8 IW/CS	9 OW/DS	A /ISS	B /ES
:	REG	4 IB/SP	5 OB/BP	6 MV/SI	7 EW/DI
,	.	0 EB/AX	1 ER/BX	2 GO/CX	3 ST/DX

Figure 3. SDK-86 Keyboard

Documentation

In addition to detailed information on using the monitors, the SDK-86 user's manual provides circuit diagrams, a monitor listing, and a description of how the system works. The complete design library for the SDK-86 is shown in Figure 4 and listed in the Specifications section under Reference Manuals.

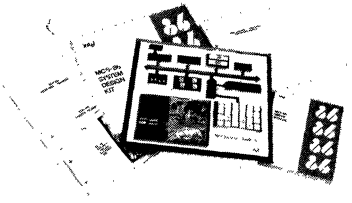


Figure 4. SDK-86 Design Library

Command	Operation
Reset	Starts monitor.
Go	Allows user to execute user program, and causes it to halt at predetermined program stop. Useful for debugging.
Single step	Allows user to execute user program one instruction at a time. Useful for debugging.
Substitute memory	Allows user to examine and modify memory locations in byte or word mode.
Examine register	Allows user to examine and modify 8086 register contents.
Block move	Allows user to relocate program and data portions in memory.
Input or output	Allows direct control of SDK-86 I/O facilities in byte or mode.

Table 1. Keyboard Mode Commands

Command	Operation
Dump memory	Allows user to print or display large blocks of memory information in hex format than amount visible on terminal's CRT display.
Start/continue display	Allows user to display blocks of memory information larger than amount visible on terminal's CRT display.
Punch/read paper tape	Allows user to transmit finished programs into and out of SDK-86 via TTY paper tape punch.

Table 2. Serial Mode Commands

Command	Operation
Up/download	Allows user to transport finished programs between Intellec and SDK-86, using special Intellec utility program.

Note
The Intellec slave mode utilizes all the keyboard mode commands and serial mode commands (listed in Tables 1 and 2, respectively), as well as the up/download slave mode command, via the console of the Intellect development system, using the SDK-C86 product.

Table 3. Intellec Slave Mode Commands

8086 INSTRUCTION SET

Table 4 contains a summary of processor instructions used for the 8086 microprocessor.

Mnemonic and Description	Instruction Code			
DATA TRANSFER				
MOV = Move:	76543210	76543210	76543210	76543210
Register/memory to/from register	100010dw	mod reg r/m		
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1
Immediate to register	1011w reg	data	data if w=1	
Memory to accumulator	1010000w	addr-low	addr-high	
Accumulator to memory	1010001w	addr-low	addr-high	
Register/memory to segment register	10001110	mod 0 reg r/m		
Segment register to register/memory	10001100	mod 0 reg r/m		
PUSH = Push:				
Register/memory	11111111	mod 110 r/m		
Register	01010 reg			
Segment register	000 reg 110			
POP = Pop:				
Register/memory	10001111	mod 000 r/m		
Register	01011 reg			
Segment register	000 reg 111			
XCHG = Exchange:				
Register/memory with register	1000011w	mod reg r/m		
Register with accumulator	10010 reg			
IN = Input				
Fixed port	1110010w	port		
Variable port	1110110w			
OUT = Output				
Fixed port	1110011w	port		
Variable port	1110111w			
XLAT=Translate byte to AL	11010111			
LEA=Load EA to register	10001101	mod reg r/m		
LDS=Load pointer to DS	11000101	mod reg r/m		
LES=Load pointer to ES	11000100	mod reg r/m		
LAHF=Load AH with flags	10011111			
SAHF=Store AH into flags	10011110			
PUSHF=Push flags	10011100			
POPF=Pop flags	10011101			
ARITHMETIC				
ADD = Add:				
Reg /memory with register to either	000000dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01
Immediate to accumulator	0000010w	data	data if w=1	
ADC = Add with carry:				
Reg /memory with register to either	000100dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01
Immediate to accumulator	0001010w	data	data if w=1	
INC = Increment:				
Register/memory	1111111w	mod 000 r/m		
Register	01000 reg			
AAA=ASCII adjust for add	00110111			
DAA=Decimal adjust for add	00100111			
SUB = Subtract:				
Reg./memory and register to either	001010dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01
Immediate from accumulator	0010110w	data	data if w=1	
SBB = Subtract with borrow				
Reg./memory and register to either	000110dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01
Immediate from accumulator	0001110w	data	data if w=1	
DEC = Decrement:				
Register/memory	1111111w	mod 001 r/m		
Register	01001 reg			
NEG=Change sign	1111011w	mod 011 r/m		

Mnemonic and Description	Instruction Code			
CMP = Compare:	76543210	76543210	76543210	76543210
Register/memory and register	001110dw	mod reg r/m		
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01
Immediate with accumulator	0011110w	data	data if w=1	
AAS=ASCII adjust for subtract	00111111			
DAS=Decimal adjust for subtract	00101111			
MUL=Multiply (unsigned)	1111011w	mod 100 r/m		
IMUL=Integer multiply (signed)	1111011w	mod 101 r/m		
AAM=ASCII adjust for multiply	11010100	00001010		
DIV=Divide (unsigned)	1111011w	mod 110 r/m		
IDIV=Integer divide (signed)	1111011w	mod 111 r/m		
AAD=ASCII adjust for divide	11010101	00001010		
CBW=Convert byte to word	10011000			
CWD=Convert word to double word	10011001			
LOGIC				
NOT=Invert	1111011w	mod 010 r/m		
SHL/SAL=Shift logical/arithmetic left	110100vw	mod 100 r/m		
SHR=Shift logical right	110100vw	mod 101 r/m		
SAR=Shift arithmetic right	110100vw	mod 111 r/m		
ROL=Rotate left	110100vw	mod 000 r/m		
ROR=Rotate right	110100vw	mod 001 r/m		
RCL=Rotate through carry flag left	110100vw	mod 010 r/m		
RCR=Rotate through carry right	110100vw	mod 011 r/m		
AND = And.				
Reg /memory and register to either	001000dw	mod reg r/m		
Immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1
Immediate to accumulator	0010010w	data	data if w=1	
TEST = And function to flags, no result:				
Register/memory and register	1000010w	mod reg r/m		
Immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1
Immediate data and accumulator	1010100w	data	data if w=1	
OR = Or:				
Reg /memory and register to either	000010dw	mod reg r/m		
Immediate to register/memory	1000000w	mod001 r/m	data	data if w=1
Immediate to accumulator	0000110w	data	data if w=1	
XOR = Exclusive or:				
Reg /memory and register to either	001100dw	mod reg r/m		
Immediate to register/memory	1000000w	mod110 r/m	data	data if w=1
Immediate to accumulator	0011010w	data	data if w=1	
STRING MANIPULATION				
REP=Repeat	1111001z			
MOVS = Move byte/word	1010010w			
CMPS = Compare byte/word	1010011w			
SCAS = Scan byte/word	1010111w			
LODS = Load byte/wd to AL/AX	1010110w			
STOS = Stor byte/wd frm AL/A	1010101w			
CONTROL TRANSFER				
CALL = Call:				
Direct within segment	11101000	disp-low	disp-high	
Indirect within segment	11111111	mod 010 r/m		
Direct intersegment	10011010	offset-low	offset-high	
		seg-low	seg-high	
Indirect intersegment	11111111	mod 011 r/m		

MPU SYSTEM

continued

Mnemonic and Description	76543210	76543210	76543210
JMP = Unconditional Jump:			
Direct within segment	11101001	disp-low	disp-high
Direct within segment-short	11101011	disp	
Indirect within segment	11111111	mod 100 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 101 r/m	
RET = Return from CALL:			
Within segment	11000011		
Within seg adding immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment adding immediate to SP	11001010	data-low	data-high
JE/JZ=Jump on equal/zero	01110100	disp	
JL/JNGE=Jump on less/not greater or equal	01111100	disp	
JLE/JNG=Jump on less or equal/not greater	01111110	disp	
JB/JNAE=Jump on below/not above or equal	01110010	disp	
JBE/JNA=Jump on below or equal/ not above	01110110	disp	
JP/JPE=Jump on parity/parity even	01111010	disp	
JO=Jump on overflow	01110000	disp	
JS=Jump on sign	01111000	disp	
JNE/JNZ=Jump on not equal/not zero	01110101	disp	
JNL/JGE=Jump on not less/greater or equal	01111101	disp	
JNLE/JG=Jump on not less or equal/ greater	01111111	disp	
JNB/JAE=Jump on not below/above or equal	01110011	disp	
JNBE/JA=Jump on not below or equal/above	01110111	disp	
JNP/JPO=Jump on not par/par odd	01111011	disp	
JNO=Jump on not overflow	01110001	disp	

Mnemonic and Description	76543210	76543210
JNS=Jump on not sign	01111001	disp
LOOP Loop CX times	11100010	disp
LOOPZ/LOOPE=Loop while zero/equal	11100001	disp
LOOPNZ/LOOPNE=Loop while not zero/equal	11100000	disp
JCXZ=Jump on CX zero	11100011	disp
INT Interrupt		
Type specified	11001101	type
Type 3	11001100	
INTO=Interrupt on overflow	11001110	
IRET=Interrupt return	11001111	
PROCESSOR CONTROL		
CLC=Clear carry	11111000	
CMC=Complement carry	11110101	
STC=Set carry	11111001	
CLD=Clear direction	11111100	
STD=Set direction	11111101	
CLI=Clear interrupt	11111010	
STI=Set interrupt	11111011	
HLT=Halt	11110100	
WAIT=Wait	10011011	
ESC=Escape (to external device)	11011xxx	mod x x x r/m
LOCK=Bus lock prefix	11110000	

Notes

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value
Greater = more positive,
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction, if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high· disp-low

if s w = 01 then 16 bits of immediate data form the operand
if s w = 11 then an immediate data byte is sign extended to form the 16-bit operand
if v = 0 then "count" = 1, if v = 0 then "count" in (CL)
x = don't care
if v = 0 then "count" = 1, if v = 1 then "count" in (CL) register
z is used for string primitives for comparison with ZF FLAG

SEGMENT OVERRIDE PREFIX

001	reg	110

REG is assigned according to the following table

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file

FLAGS = X X X X (0F) (DF) (IF) (TF) (SF) (ZF) X (AF)·X (PF) X (CF)

Table 4. 8086 Instruction Set Summary

SPECIFICATIONS

Central Processor

CPU — 8086-4

Note

May be operated at 2.5 MHz or 5 MHz, jumper selectable, for use with 8086.

Memory

ROM — 8K bytes 2316/2716

RAM — 2K bytes (expandable to 4K bytes) 2142

Addressing

ROM — FE000-FFFFF

RAM — 0-7FF (800-FFF available with additional 2142's)

Note

The wire-wrap area of the SDK-86 PC board may be used for additional custom memory expansion.

Input/Output

Parallel — 48 lines (two 8255A's)

Serial — RS232 or current loop (8251A)

Baud Rate — selectable from 110 to 4800 baud

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — 20 mA current loop TTY or RS232

Note
The user has access to all bus signals which enable him to design custom system expansions into the kit's wire-wrap area.

Interrupts (256 vectored)

Maskable
Non-maskable
TRAP

DMA

Hold Request — Jumper selectable. TTL compatible input.

Software

System Monitor — Preprogrammed 2716 or 2316 ROMs

Addresses — FE000-FFFFF

Monitor I/O — Keyboard/display or TTY or CRT (serial I/O)

Physical Characteristics

Width — 13.5 in. (34.3 cm)

Height — 12 in. (30.5 cm)

Depth — 1.75 in. (4.45 cm)

Weight — approx. 24 oz. (3.3 kg)

Electrical Characteristics

DC Power Requirement

(Power supply not included in kit)

Voltage	Current
V_{CC} 5V ± 5%	3.5A
V_{TTY} – 12V ± 10%	0.3A
	(V_{TTY} required only if teletype is connected)

Environmental Characteristics

Operating Temperature — 0-50°C

Reference Manuals

9800697A — SDK-86 MCS-86 System Design Kit Assembly Manual

9800722 — MCS-86 User's Manual

9800640A — 8086 Assembly Language Programming Manual

8086 Assembly Language Reference Card

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

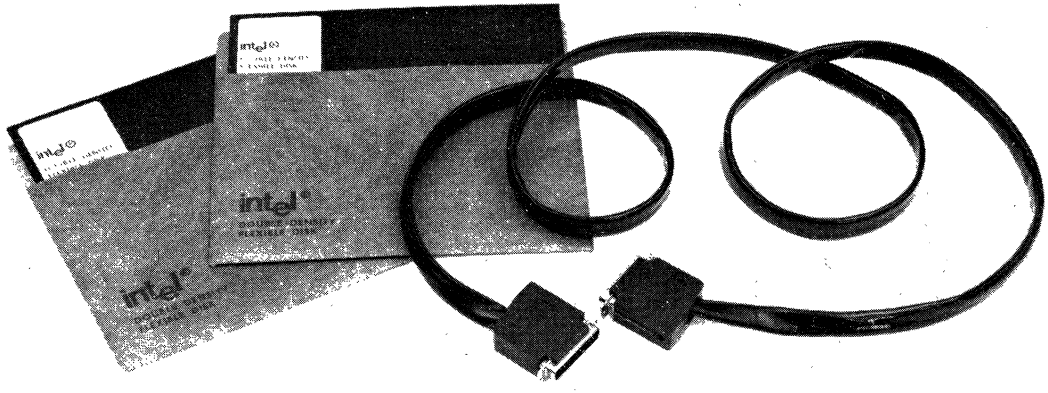
Part Number	Description
SDK-86	MCS-86 system design kit

SDK-C86

MCS-86™ SYSTEM DESIGN KIT SOFTWARE AND CABLE INTERFACE TO INTELLEC® DEVELOPMENT SYSTEM

- **Provides the Software and Hardware Communications Link Between an Intellec® Development System and the SDK-86**
- **Intellec® System Files can be Accessed and Down loaded to the SDK-86 Resident Memory**
- **Data in SDK-86 Memory can be Uploaded and Saved in Intellec® System Files**
- **Enhances and Extends the Power and Usefulness of the SDK-86**
- **Allows the SDK-86 to Become an Execution Vehicle for ISIS-II Developed 8086 Object Code Using the MDS-311 Software Cross Development Package**
- **All SDK-86 Serial Port Mode Commands Become Available at Console of the Intellec® System**

The SDK-C86 product provides the software and hardware link for using the SDK-86 monitor in conjunction with an Intellec® Development System while adding features of data transfer between SDK-86 memory and Intellec® System files. The user may enter programs and data into the SDK-86 and then save them on a diskette. Also, programs and data may be created on the Intellec® System using the MDS-311 cross development software package, then loaded into the SDK-86 for testing and checkout. This provides a real time execution environment of the SDK-86 as a peripheral to the Intellec® System.



HARDWARE

There are two serial ports on the Intellec® System back panel, TTY and CRT. Assuming that one of the ports is used for the Intellec® console, the SDK-C86 cable can plug into the unused port. The SDK-86 is jumper selectable to accept either the CRT (RS232) or TTY (20mA current loop) signals.

The edge connector on the SDK-86 has the MULTIBUS™ form factor. No signals are connected to the fingers except the power supply traces. Therefore, the SDK-86 can plug directly into the Intellec® motherboard to obtain power while using the SDK-C86 cable as the communication link.

SOFTWARE

Two programs must be invoked to operate in the SDK-86 slave mode. One program runs on the SDK-86, and another runs in any ISIS-II environment that includes a diskette drive.

The serial I/O monitor is installed on the SDK-86 and operates as though it was talking to a terminal. The software in the Intellec® allows the Intellec®, with a console device, to behave as if it were a terminal to the SDK-86.

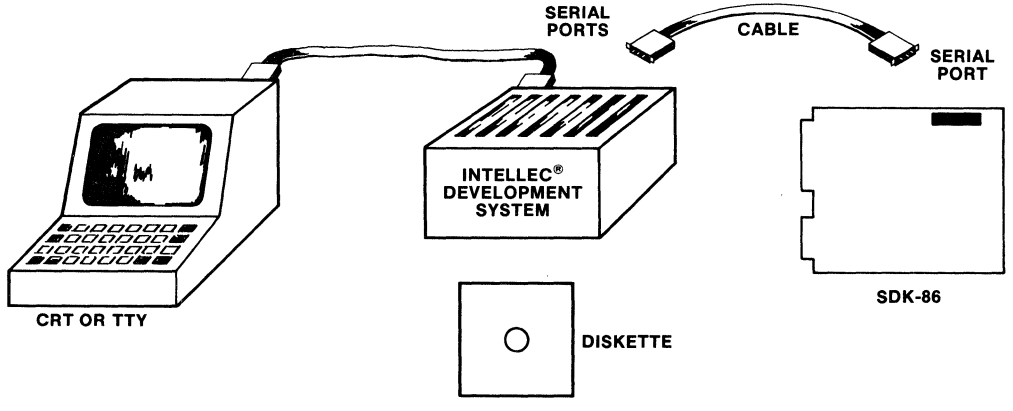
The SDK-C86 software program in the Intellec reads the console input device, then passes the character to the SDK-86 through the serial port. It also receives the characters from the SDK-86 and displays them at the console output device. Besides the basic transfer function, this program also recognizes and performs the Upload and Download functions.

COMMAND MODES

- Transparent: In this mode, the SDK-C86 software passes all characters through without any processing. All the commands of the SDK-86 monitor (except paper tape commands) are available and will function in exactly the same manner as if the terminal were attached directly to the serial port of the SDK-86.
- Upload/Download: In this mode the SDK-C86 software, in the Intellec®, recognizes the mnemonic for Upload or Download from the terminal. It "translates" the Download command to an R (Read hexadecimal tape) command and the Upload command to a W (Write hexadecimal tape). The R and W commands are then passed on to the SDK-86 monitor. Using these paper tape commands allows for a checksummed transfer of data between the Intellec® and the SDK-86 memory.

COMMAND SUMMARY

- Reset — starts the SDK-86 monitor.
- Execute with Breakpoint (G) — Allows you to execute a user program and cause it to halt at a predetermined program step — useful for debugging.
- Single Step (N) — allows you to execute a user program one instruction at a time — useful for debugging.
- Substitute Memory (S, SW) — allows you to examine and modify memory locations in byte or word mode.
- Examine Register (X) — allows you to examine and modify the 8086's register contents.
- Block Move (M) — allows you to relocate program and data portions in memory.
- Input or Output (I, IW, O, OW) — allows direct control of the SDK-86's I/O facilities in byte or word mode.
- Display Memory (D) — allows you to print or display large blocks of memory information in HEX format.
- Load (L) — allows you to load hex format object files into SDK-86 memory from an Intellec.
- Transfer (T) — allows you to save contents of SDK-86 memory in a hex format object file in the Intellec.



SDK-86/Intellec® Slave Mode Configuration

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Insite™, Intel's Software Index and Technology Exchange, is a collection of programs, subroutines, procedures, and macros written by users of Intel's 8008, 8048, 8080, 8085 and 8086 microcomputers, iSBC-80 OEM computer systems, and Intellec® development systems. Thanks to customer contributions to Insite™, Intel is able to make these programs available to all users of Intel microcomputers. By taking advantage of the availability of these general-purpose routines, the microcomputer design engineer and programmer can save many hours of programming and debugging time. The library of programs also serves as a good learning tool for those unfamiliar with Intel assembly language or PL/M-80 and FORTRAN-80, Intel's high-level languages for the 8008, 8080 and 8085 microcomputers.

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MPU SYSTEM

INSITE PROGRAM LIBRARY MANUAL

Each member will be sent the Program Library Manual consisting of an abstract for each program indicating the function of the routine, required hardware and software, and memory requirements, plus the source listings that are five pages and under.

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PROGRAM SUBMITTAL

Programs submitted for our review must follow the guidelines listed below:

1. Programs must be written in a standard Intel Assembly Language or PL/M-80. These languages are documented in the following manuals:
   a. 8008/MCS-8 Assembly Programming Manual #98-019B
   b. 8080/8085 Assembly Language Programming Manual #98-301C
   c. 8080/8085 Floating-Point Arithmetic Library User's Manual #98-452B
   d. PL/M-80 Programming Manual #98-268B
   e. MCS-48 and UPI-41 Assembly Language Manual #98-255C
   f. FORTRAN-80 Programming Manual #98-481A
   g. 8086 Assembly Language Reference Manual #98-640A
   h. PL/M-86 Programming Manual #98-466A
2. A source listing of the program must be included. This must be the output listing of a compile or assembly. All accepted programs must be capable of compilation or assembly by Intel standard compilers or assemblers. No consideration will be given to partial programs or duplication of existing programs.
3. A test program which assures the validity of the contributed program must be included. This must show the correct operation of the program.
4. A source paper tape or diskette of the contributed program is required. This will be used for the reproduction of tapes for other members.

Complete the Submittal Form as follows: (please type or print)

1. **Processor** (check appropriate box).
2. **Program Title:** Name and brief description of program function.
3. **Function:** Detailed description of operations performed by the program. Attach additional pages if necessary.
4. **Required Hardware:**
   For example: TTY or Ports 0 and 1
   Interrupt Circuitry
   I/O Interface
   Machine line and configuration for cross products
5. **Required Software:**
   For example: TTY Driver
   Floating Point Package
   Support software required for cross products
6. **Input Parameters:** Description of register values, memory areas or values accepted from input ports.
7. **Output Results:** Values to be expected in registers, memory areas or on output ports.
8. *Program Details:* (for resident products only)
   a. Register modified
   b. RAM required (bytes)
   c. ROM required (bytes)
   d. Maximum subroutine nesting level
9. **Assembler/Compiler Used:**
   For example: PL/M-80
   Intellec® MDS Macro Assembler
   FORTRAN-80
10. **Programmer, Company and Address.**

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3-Byte Positive Fractional Multiply
5 Level (BARDOT) to 8 Level (ASCII) Paper Tape Conversion
8-Bit Multiply and Divide
8-Bit Random Number Generator
12 x 12 Multiply
16-Bit CRC for Polynomial X16 + X12 + X5 + 1
16-Bit Division — 16-Bit Result
16-Bit Division — 16-Bit Result
16-Bit Multiply — 16-Bit Result
16-Bit Multiply — 16-Bit Result
16-Bit Multiply — 32-Bit Result
16-Bit Random Number Generator
16-Bit Square Root Routine
32-Bit Binary to BCD Conversion, Leading Zero Blanking
32-Bit Divide Subroutine
2708 PROM Programmer for Intellec 8/MOD 80
4040 Cross Assembler for Intellec 8/MOD 80 and MDS-800
8008 Cross Assembler for 8085-MACRO Definition — M8008.SRC
8008 Cross Inverse Assembler for HP 2100
8008 Disassembler
8008 MACRO Assembler Version 2.0
8008 MACRO Definition Set for Assembly on PDP-11
8048 BCD Multiply
8048-DIV — Division Routine
8048 — Seven Segment Display Interface Subroutines — SCAN
8048 TUNE GENERATOR
8080 CPU Exercise Routine
8080 Cross Assembler for Tektronix 4051
8080 Disassembler
8080 Disassembler
8080 Double Precision ARC Tangent
8080 Floating Point A^b
8080 Floating Point Extended Math Package
8080 Floating Point with BCD Conversion Routine
8080 Idle Analyzer for Approximating CPU Utilization
8080 I/O System Status Display
8080 Least Squares Quadratic Fitting Routine
8080 MACRO Assembler 4.1
8080 RAM Memory Test
8080 Symbol Table Dump
8085 Cross Assembler for the DEC PDP8 and PDP11
9600 Initialize CRT and UART for Baud
Absorbance Calculation
A/D Converter Routine
ADCCP Remainder Routine
Adaptive Game Program
Algebraic Compare Subroutine
Align Program — Intermediate Pass Between PLM/Pass 1 & 2
Analog/Digital Polling Routine
AP29 "USING THE 8085 SERIAL I/O LINES"
APL Graphic Display on a 5 x 7 Dot Matrix
Approximating Routine
Arctan 2 Subroutine
ARRAY ADDRESSING SUBROUTINE AND CALLING MACRO
ASCII Display
ASCII to EBCDIC and EBCDIC to ASCII Converters
ASCII String to Intel Floating Point
Assembler Oriented Centronics 306 Line Printer Handler and Error Only Assembler
Bandit Static Display
Banner Print and Punch
BASIC CPU State Vector Maintenance
Basic Digital Panel Meter Call
BASIC Interpreter
BASIC/M Translator and Interpreter
BCD to BIN Conversion Routine
BCD to/from Binary Conversion
BCD Input and Direct Conversion to Binary Routine
BCD Multiplication
BCD Sum for 8008
BCD Up/Down Counter
BIN to BCD Conversion Routine
Binary to BCD Subroutine
Binary to HEX Routine
Binary Loader for MDS
Binary Multiplication — 24-Bit
Binary Search
Binary Search Routine
Binary Tape Program
BINDECBIN — Binary to/from BCD
BINLB — 8080 System Loader
BIORIM
Blackjack
$BLPT
BOOT — Bootstrap Loading and Program Patching
Calculate a Calendar
Calendar Subroutine
Card Reader Driver, Hollerith to ASCII Conversion
Character Interpreted Memory Dump
CLI
Clock Subroutine
Compare
COMPARE Files
Compare Object Code Tape with Memory
Control Data Output
Controller for Hewlett-Packard 9871A Printer
Conversion of Scientific to Easily Readable Notation
Crap's
CRECH — Cyclic Redundancy Check
Cross Assembler ASM08
Cross Assembler for NOVA 1200
Cross Assembler for NOVA 1220, IBM 360/40 and CDC 3000
Cross Assembler for PDP-11
Cross Assembler for PDP-11
Cross Assembler for Varian Data Machine
Cross Reference for PAS80 PASCAL Programs — XREF80
CRTBZ — GET
Cut and Paste Editor (PL/M)
Cyclic Redundancy Character Generator
Cyclic Redundancy Check
Cyclic Redundancy Check for Data String of 2^{16} Bytes
Data Array Move
Data General to Intellec MDS Diskette Transport Package
Data I/O PROM Processor
"DATCON B1" Analog to Digital Conversion Program
Decrement H and L Regsiters
Delete Comments
Diagnostic 1003 — Memory Validity Check
Digital to Analog Conversion for Eight Outputs
Disable Hold — Screen Mode
Disassembler
Disk Dump Routine for ICOM F DOS-11/MOD 80 Floppy DOS
Diskette Recovery Program, Recovery 1
Display
Double Precision Integer Arithmetic Package
Double Precision Multiply
Driver for Tektronix 4010 Grafic Screen
DTMHEX
Elementary Function Package
Enable Hold — Screen Mode
ERLIST
Examin
EXEC
Factorial of a Decimal Number
Fast Floating Point Square Root Routine
FAST & SLOW
FDUMP
Field
Fixed and Floating Point Arithmetic Routines
Fixed Point CHEBYSHEV Sine and Cosine for PL/M Users
Flag Processing Routine
Floating Point Conversion Routine
Floating Point Decimal and HEX Format Conversion
Floating Point Format Conversion Package
Floating Point Interpreter
Floating Point Math Package
Floating Point Package for Intel 8008 and 8080 Microprocessors
Floating Point Procedures
Floating Point Square Root
Floating Point Utility Programs for Use with FPAL.LIB
Fly Reader Driver
Format
Format Intel Data
Gambol
Game of Life
Gamma Function Subroutine
Generalized Stepper Motor Drive Program
GLANCE
GRAPH
Gray to Binary Conversion
Handler for Tally PTP
Hang
Hazeltine 2000 CRT Function Driver
Hewlett-Packard Calculator to MDS800 I/O Control Program — HPIO
HEX Convert — Convert Intel HEX to Prolog HEX File Converter
Hex to ASCII Conversion
HEX to Decimal Conversion
HEX Format Paper Tape Dump for SDK
HEX Tape Loader for SDK
High Speed Paper Tape Reader with Stepper Motor Control
Histogram
I8080 Cross Assembler for Intel 8080/8085 Microprocessors
IBM Selectric Input Program
IBM Selectric Output Program
ICE-80 Disassembler
I-Command — Insert Data in HEX Form from TTY into RAM
Input/Output Commands for MDS
Insert Tab Characters for Spaces
Intel Format HEX Data File Load/Read
Intellec 8 MOD 80 Monitor
Intellec 8/MOD 80 — Silent 700 Interface
Intellec MDS Diagnostic Confidence Test Version 1.1
Intellec MDS Monitor Version 2.0
Intellec 8 Text Editor
Interfacing the MDS and HP 2644
Interrupt Driven Clock Routine
Interrupt Handler (Re-Entrant)
Interrupt Service Routine
INVERT Data in RAM
I/O Routine for TI Silent 700 Terminal
I/O Simulation MACROS
I/O Test Program for SBC 80/20 — IOTEST
Join
Julian Data Routine
K, Program Trap and Dump Routine
Kalah
Keyboard Scanner
Kill the Rotating Bit
Lander
Lerr
Legible Paper Tape
Lewthwaite's Game
Linear System (Gauss Elimination) — LISY
LISP INTERPRETER
List
List Device Program
List SCR
List 1 — High Speed List Program for Intellec 8
List/Print/Type "List SRC" on Diskette
LLL/Chernack Basic Interpreter
LOAD
Log Base 2
LSORT
MACRO Assembler for DG NOVA
Main Routine DDUMP(Diskette DUMP Routines)
Mastermind
Mastermind 8080
"Mastermind 8080" for SBC 80/10
Match
Match Game
Maze
Maze
MBCD N1 x N2 Bytes Decimal Multiply Subroutine
MDS Back to Back Data Transfer
Memory Compare
Memory Diagnostic Program
Memory Dump
Memory Test for the 8080
Memory Test Program
μScope 820 Test Instrument, iSBC 80/10 Diagnostic Program
MINITH-RMX Minimal Terminal Handler
Model 101 Centronics Printer Handler
Mon256 — 256-Byte PROM Monitor

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Monitor for iSBC 80/05 or 80/04 — MON805
Monitor for iSBC 80/10 or 80/10A — MON810
Monitor for iSBC 80/20 or 80/20-4 — MON820
Morse Code Generator
MSAVE/MLOAD Utilities for MDS-800 with DOS
MUL/DIV Multi-Precision Pack for 8080
Natural Logarithm
N-Byte Binary Multiplicaiton and Leading Zero Blanking
Nim
Nim
Non-Encoded Keyboard Subroutine
Nova Cross Assembler — Intel 8080
Numbers
Octal Code Conversion for PDP-11
Octal Debugging Program (ODT) for the MCS-80 Computer
Octal PROM Programming
OCTHEX
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Optimized Ultra Fast Floating Point Package
Output Message Generator
P2708 PROM Programming Routine
Page Break for Tektronix 4010 I/O Graphics Terminal
Page Listing Program
Paper Tape Leader I.D
Paper Tape Reformatter for SDK
Pass — Parameter Passing Routine
PDP-11 Binary File to Intel HEX File Converter
PDP-11 Program Load to HEX, Dump, & Verify
PILOT-80 ISIS-II Version 2.0
PL/M 80 Pass 3
PL/M Floating Point Interface
PL/M Histogram Procedure and Random Number Generator
Print
Print Program for G.E. Terminet-1200 Printer
Print Out Source File on Floppy Disk
Print Text for SBC 80/10
Program Test Load
PROM Programmer for Intellec 8
Prompt Pong
Proportional Power Control Image Builder
Punch Binary Tape
Punch Test or TTY Reader/Punch Test
Quicksort Procedures
RAM Check
RAM Test Program
Random Number Generator — RINGEN
RANDOM$BITS
React
Read and Interrupt Modifications for Intellec 8/MOD 80
Read/Write Routines for Interchange Tapes
Reader Test
Real Time Clock Service Routine
Real Time Executive
Real Time Monitor
RECOVR
Relative Jump Routine
Relocatable FMath and XMath, 8085 Floating Point Package
RIA80
RMSTF — Integration Routine
RMX/80-based Keyboard Input Handler Subroutine
Run 0
Sample Automatic Test Equipment
Save/Restore CPU State on an Interrupt
SBC Communicator
SBC 80P Real Time Clock
SBC 80/10 8255 Test
SBC 80/10 Interactive Monitor
SBC 80/10 Port I/O Exerciser
SBC 310 Floating Point System for Use with SBC 80/20
SCAN
SCAN — 8048 — Seven Segment Display interface Subroutines
SDK-80 Keyboard Monitor
SDK-80 Paper Tape Punch Routine
SDK80 TRAP
SDK PROM Programmer
Sequential Pascal Compiler
Serial PROM Programmer
Sets Horizontal Tabs on Terminet
Shellsorting Routine
SinX, CosX Subroutine
Slot Machine
SMAL:Symbolic Microcontroller Assembly Language
SMPY16: 16-Bit 2's Complement Signed Multiplication
Snap Dump 8080
Software Stack Routines for 8008
Source Paper Tape to Magnetic Cassette
SQRTF — Calculates 8-Bit Root of 16-Bit Number
Stage2
Statement Counter
STEP
String Manipulation Package
Structured Assembler for 8080
Subroutine DMULT (Decimal Multiplication)
Subroutine Log — Common Logarithms
Subroutine SORT
Symbol Cross-Reference
Symbol Table
Symbol Table Dump for Intellec 8/MOD *0
Symbol Table List Routine
Tabs
Tally — Use Tally 2200 Line Printer in Assembly Stage of Programming
Tally R2050 HSPTR Driver
Tape Duplicator
Tape Labeler for MDS
Teleprocessing Buffer Routine
Terminal Editor
Terminet 300
Terminet 1200
Text Editor, Enhanced
Text Storage Program
Thermocouple Linearization (Type J)
Thumbwheel SBC 80/10 Test Program
Tic-Tac-Toe
Tic-Tac-Toe — 3 Dimensional
Time Sharing Communications
TIMIT — Interrupt Driven Real Time Clock Routine
T.I. Silent 700 Interface — Intellec MDS
T.I. Silent 700 SBC 80 Monitor Interface
TRACE — Program Trace and Debugger
Trace & Register Print Out
Trace Routine
TRACE Version 7.0
TTY Binary Dump Routine
TTY Binary Load Routine
TTY Diagnostic
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WRMIN-RMX Minimal Terminal Output

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*Please refer to Intel OEM Price List for membership fee.

μSCOPE 820
MICROPROCESSOR SYSTEM CONSOLE

Gives complete control over microprocessor, including single step, run-with-display, or run-real-time capability

Provides a 32-bit hardware breakpoint with bit masking and a 256-word trace memory

Executes diagnostic routines from μScope 820 console overlay memory

Provides an interface to microcomputer systems for troubleshooting system problems

Monitors, displays, and alters register, memory, and I/O values for system under test

Executes instrument resident software patch routines even when microcomputer system is ROM-based

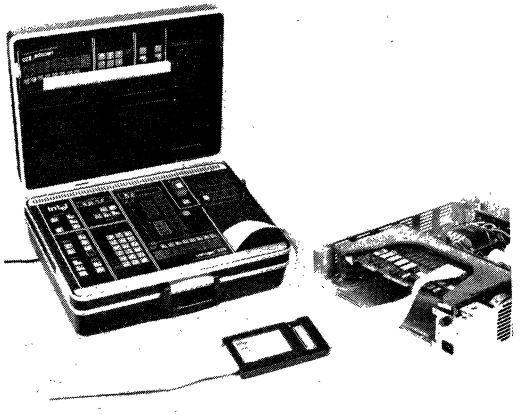
Is a stand-alone, self-contained, rugged portable unit

Human engineered with easy to read 9-segment hexadecimal displays and extensive operator prompting

Designed to support many different microprocessors

Has built-in, self-test operation

Intel's new μSCOPE 820 Microprocessor System Console provides equipment manufacturers with a portable microcomputer system designed to expedite troubleshooting and maintenance of other microcomputer systems. The unit can control and examine system operations. Diagnostics can be automated by EPROM (erasable, programmable read only memories) or ROMs into the socket at the upper left of the keyboard display panel. The μScope 820 is a portable, self-contained instrument designed to provide the control, monitoring, and interaction necessary to effectively and quickly evaluate and debug 8-bit microcomputer-based systems in the lab, on the production line, or in the field. Connection to the user's system is through a personality probe plugged into the microprocessor socket. Each personality probe is unique to each microprocessor type. The instrument features many different operating and control modes, allowing the operator to carry out a number of functional checks on the microcomputer system under test (SUT). Although the unit has been specifically designed to ease the task of microcomputer system checkout for the lab, production line, and field technician, it also provides the more powerful analytical capabilities necessary to troubleshoot difficult problems by the more experienced, sophisticated user. Preprogrammed test routines resident in front panel PROMs, dedicated high level commands keys, visual prompting, and simplified data entry sequences all ease the checkout of microcomputer hardware. For more rigorous diagnostic tasks, the unit provides a 32-bit maskable hardware breakpoint with optional course of action after a breakpoint match, a 256 × 32-bit trace memory, and a 128 × 8 overlay RAM that allows real-time entry of test routines via the μScope 820 keyboard.



FEATURES

CPU Control

The instrument provides complete control over the operation of the microprocessor in the system under test (SUT). The user CPU can be forced to halt, single step, reset, run real time, or run with display. All of the above CPU commands may be issued without impacting other operational parameters or diagnostic sequences previously established.

Reset/Self-Test

The reset and self-test features of the unit allow the operator to either initialize the instrument to a known state or quickly verify that the instrument is operating correctly. When the console is reset, the breakpoint and overlay memory are disabled, the display registers are cleared and the specific examine modes are aborted.

When the operator initiates the self-test of the unit, a sequence of operations take place which serve to confirm proper operation of a majority of the instrument.

Breakpoint Control

The hardware breakpoint of the instrument allows the operator to alter the normal program flow of the SUT. Breakpoint logic is implemented in hardware, thereby eliminating any throughput degradation of the SUT. All 32 bits of the breakpoint condition word are maskable in order to allow the breakpoint condition to be as specific or as general as may be desired. The occurrence of a breakpoint match can cause an unconditional halt, incrementing of the pass counter, calling of a subroutine, or the recording of a single cycle of trace data. All of these options are selectable via the exam action key prior to enabling the breakpoint.

Trace Memory

The console has a full 32-bit word trace memory that records 256 cycles of SUT operation without causing any delays. The trace memory provides information about CPU operation just prior to a CPU halt or just prior to the initiation of a panel freeze via the trace display key. The operator can alternatively elect to have data recorded on all SUT microprocessor cycles or only when program execution of the SUT microprocessor generates a breakpoint match. Once the data is recorded, sequential examination of the data may be accomplished simply by depressing the exam next or exam last keys.

Overlay Memory

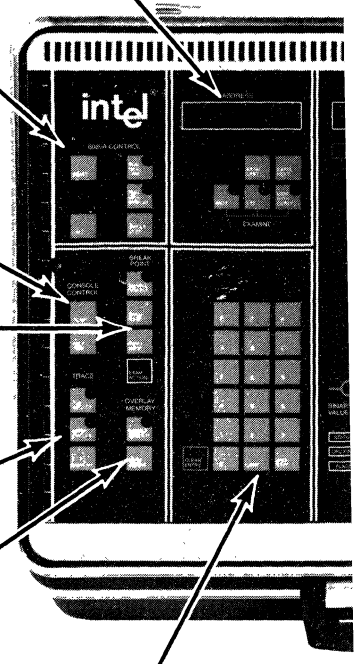
A unique feature of the unit is the ability to map its memory onto the SUT memory space. Using the overlay memory allows the operator to insert patch, exercise, or diagnostic subroutines at any location or point of execution in the SUT program. The subroutine may either be entered via the front panel hexadecimal keypad or via the front panel's ROM/PROM socket. By using the unit's overlay memory, the operator may quickly set up the SUT to execute special maintenance or troubleshooting programs to permit rapid evaluation of system operation.

Address Display/Select

A dedicated, 4-digit hexadecimal address display allows the following address information to be displayed:

- The address of any memory location.
- The I/O port number of any I/O port.
- The address of any overlay memory location.
- The address of the overlay memory origin assignment.
- The address at which the breakpoint is to occur.
- The address portion of the breakpoint mask.
- The address of the given trace record element.

An additional feature of the address display/select logic is that once the operator has initiated a given memory, trace, or I/O examination, it is possible to continue the examination in a sequential fashion either in an ascending or descending address value.

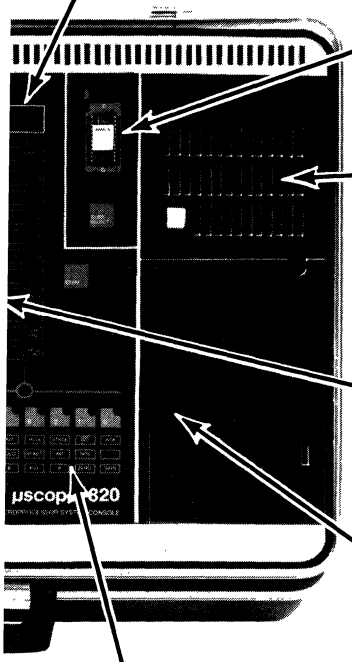


Address, Data, and Control Entry

The address, data, and control variable entry into the instrument is accomplished via the conveniently located hexadecimal keypad. For selection of the information to be displayed or modified the operator enters the hexadecimal value of the desired address, I/O port number, or label assigned to each of the registers. Once this entry is made, the operator can then elect to either continue data entry if modification is desired or press the end execute key if examination only is desired. For all data entry sequences potentially requiring multiple value entry, the μScope 820 Microprocessor System Console provides operator prompting to indicate the specific information expected.

Value Display/Select

The value displays provide clear and easy to use information. Together with the address display, they provide simultaneous readout of trace vectors, breakpoint conditions and breakpoint mask values, memory contents, and I/O port contents. In addition, the display allows readout of all single and double byte register values, the state of CPU pins and flags, and information regarding the course of action following the occurrence of a breakpoint, as well as information regarding the breakpoint pass count. The information displayed by the 4-digit hexadecimal value readouts is selected via the hexadecimal keypad in conjunction with any of the instrument's eleven dedicated examine keys. Further, the information is either displayed statically or is continually updated 10 times/sec if the unit is in the run-with-display mode.



Binary Data Display/Modification

All 8-bit values can be displayed in binary format on the instrument. The binary display operates in parallel with the hexadecimal display and is provided for those instances where operator recognition is enhanced by binary presentation. The selection procedure for the binary data display is identical to that for the hexadecimal value display. Once the selection has been made, the operator may alter the value by means of further hex keypad entries or by changing the binary state of any of the data bits via the eight binary data switches.

Front Panel

The front panel of the μScope 820 Microprocessor System Console has been designed to be rugged and durable as well as easy to use and understand. A plastic overlay employing membrane switch contacts provides long lasting durability as well as protection from accidental spills. Audio and tactile feedback for the membrane switches is provided for operator convenience. Ease of use of the front panel has been further enhanced by human engineering with functional grouping of switches as well as LEDs that prompt the operator during data entry sequences. Graphics have also been added to reinforce the functional switch groupings as well as data entry procedures.

PROM/ROM Socket

A front panel socket is provided for mounting 2K PROMs or ROMs that serve as storage for preprogrammed test subroutines. The actual useable program space of the PROM/ROM is 1920 bytes. The remaining 128 bytes of storage, shadowed by RAM, are used by the unit to identify up to 16 separate subroutines in the PROM/ROM and to define the specific instrument states and conditions under which the subroutine will be called. Each of the separate subroutines is uniquely enabled by the subroutine select (SUBR SELECT) key and the hex keypad.

Power Supply

The system console is complete with its own fully regulated DC power supply that provides all the DC power required by the unit itself, as well as that which is required by the associated microprocessor probe. The supply is completely self-contained, including its own AC on/off switch, line fuse, line filter, and power cord. An additional feature of the power supply is that it has been designed to permit line voltage selection in the field to facilitate operation with a wide range of AC line voltages and frequencies.

Breakpoint Action

Following the occurrence of a breakpoint match, the operator has the flexibility to execute a number of different diagnostic operations. The selection of these alternate courses of action is accomplished by pushing the exam action key and then entering the assigned value of the specific action desired via the hex keypad. Further keypad entries specify the parametric value of the action selected such as the number of breakpoint pass counts or the start address of a subroutine call following a breakpoint.

Probe Connection

The instrument is intended to work with many of the microprocessors available today. This is accomplished by standardized interface logic which transmits and receives various address, data, and control signals between the system console and the circuitry of the particular probe. The interconnect circuitry between the instrument and probe has been designed to drive a 4-foot cable that permits convenient positioning of the panel and the SUT. In addition, a board edge connector has been provided for a personality ROM that provides front panel definition and interpretation of specific control signals for different types of microprocessors. This personality ROM is supplied with each probe kit.

FUNCTIONAL DESCRIPTION

CPU Control

User selectable commands permit one of four possible CPU operating modes:

Run Real Time — User's CPU runs at full speed set by user clock. No wait states or cycle stealing are required.

Run with Display — User's CPU runs at full speed, except that 10 times/sec the instrument halts user's CPU temporarily to acquire display data. Worse case throughput is 95% of real time operation.

Halt — User CPU halted at next opcode fetch. DMA activity is permitted during halt.

Single Step — User CPU executes one instruction then halts.

Breakpoint Control

The breakpoint condition is set by a 32-bit word (16-bit address, 8-bit data, 8-bit status). The breakpoint mask is also set by a 32-bit word which is bit selectable. There are three courses of action following a breakpoint match:

1. Halt on first opcode fetch following breakpoint match.

2. Halt on first opcode fetch following Nth breakpoint match $1 \leqslant N \leqslant 256$.

3. Execute subroutine beginning at first opcode fetch following breakpoint match.

All breakpoint actions following a match are controlled by the breakpoint enable/disable switch except for trace recording and the sync trigger output. The sync output is a negative true TTL output occurring whenever a breakpoint match occurs.

Trace Memory

The trace memory is a 256-word memory with each word consisting of 16 address bits, 8 data bits, and 8 status bits. The memory is a circular buffer which records the last 256 cycles (words) prior to a user CPU halt or display trace command. Trace data can be recorded on all CPU cycles or only when breakpoint matches occur (independent of breakpoint enable/disable status). In addition, the operator may initiate a panel freeze to temporarily stop all trace data recording, and allow display of previously recorded data without halting the user CPU.

Overlay Memory

The μScope 820 Microprocessor System Console allows memory read/writes of the user CPU in any assigned 1K or 2K block to be made to the instrument's overlay memory. For 1K block assignments, the first 128 bytes reside in the instrument's RAM memory while the remaining 896 bytes reside in the interchangeable front panel ROM/EPROM (either Intel's 2716 EPROM or Intel's 2316E ROM). For 2K block assignments, again the first 128 bytes are from RAM and the remaining 1920 bytes are from the front panel 2716/2316E.

Data Entry

All single and double byte items may be entered via the front panel hexadecimal keypad. In addition, all single byte items may be optionally entered via eight binary input keys.

Data Display

Eight hexadecimal 0.5 in. LEDs are provided for the simultaneous display of 4 bytes of information. The displays are physically separated into two groups. The first group displays 2 bytes of address, while the second group displays CPU data, status, single and double byte register values, or single and double byte breakpoint values. In addition, eight binary displays are used to provide quick recognition of single byte binary data patterns.

Self Test

The necessary hardware and software have been incorporated into the instrument to facilitate the self-checking of the majority of its operations. Included in these self tests are:

- Bit tests of all breakpoint condition and mask latches.
- Bit tests of all RAM.
- Verifies checksum on all operating system ROMs.
- Clears trace memory and performs bit test on trace RAM.
- Checks miscellaneous I/O ports and peripheral components
- Lights all front panel displays for user verification.

SPECIFICATIONS

Commands

Reset
Self test
CPU reset
Run real time
Run with display
Halt
Single step
Enable/disable breakpoint
Enable/disable overlay
Enable trace all cycles
Enable trace at breakpoint
Examine/modify value
  — Single registers
  — Double registers
  — CPU states
  — Breakpoint pass count
Examine/modify memory
Examine/modify I/O
Examine/modify overlay memory
Examine/modify next location
Examine/modify last location

Examine/modify breakpoint condition
Examine/modify breakpoint mask
Examine/modify breakpoint action
Examine/modify overlay origin
Display trace data
Clear entry
Continue
End/execute
Subroutine select

Connection

Four external connections to the μScope 820 Microprocessor System Console are provided:

1.2m (4 ft), 50 conductor flat cable — for connection to the microprocessor probe

20-pin board edge connector — for the probe personality PROM

24-pin zero force insertion sockets — for overlay EPROM/ROM

Recessed pin — for breakpoint sync output

Breakpoint

Pulse Width — 180 ns typ
Output High — 2.5V min, − 1.2 mA
Output Low — 0.5V max, 24.0 mA

Physical Characteristics

Width — 18-7/8 in. (479 mm)
Length — 15-1/2 in. (394 mm)
Height (top closed) — 6-5/8 in. (168 mm)
Height (top removed) — 4-5/8 in. (117 mm)
Weight — 20 lb (9.1 kg)

Electrical Characteristics

Voltage — 100, 120, 220, 240 — 10% + 5%, 110V AC max
Frequency — 48–63 Hz

Environmental Characteristics

Operating Temperature — 0°C to 55°C (32°F to 130°F)
Storage Temperature — −40°C to 75°C (−40°F to 167°F)
Humidity — 95% RH, 15°C to 40°C (59°F to 104°F) non-condensing

Accessories Supplied

Two keys
One fuse for 220/240V operation
One 2.3m (7.5 ft) power cord

Reference Manuals

9800526A — μScope 820 Operator's Handbook (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
USC-820	Microprocessor system console

μSCOPE PROBE 8080A

Provides interconnection for 8080A microprocessor-based systems to μScope 820 Microprocessor System Console

Provides complete control over system under test (SUT), yet causes minimal interference with SUT operation

Comes complete with cable, buffer box, personality ROM, and μScope 820 system console overlay

Fits securely in console carrying case during transit

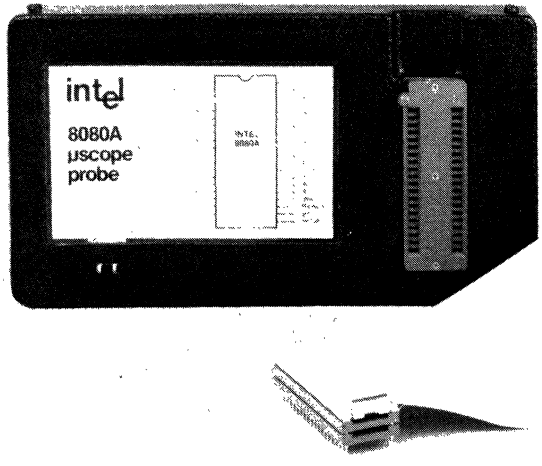
Provides complete protection for plug pins during transit

Connects via 4-foot cable to μScope 820 console

Has user system interconnect cable with integral ground plane for low noise operation

Operates over broad range of environmental conditions

The μScope Probe 8080A provides the μScope Microprocessor System Console with the ability to interact with 8080A microcomputer-based systems. The purpose of the probe is to interface the μScope 820 console to the CPU of the system under test (SUT). All of the interface signals and the associated circuitry have been designed to be effectively transparent to the SUT. CPU data, address, and clock lines are sensed by the probe 8080A, with only the CPU ground lines being switched. In addition, all SUT loading and timing degradations have been minimized by specially designed buffer circuitry. The mechanical design of the probe is compact, rugged, and allows proper operation of the probe and the console over the full ambient range specified. The buffer circuitry and the ground plane design of the interconnect cable provide low noise electrical signals while allowing the SUT to be four feet from the system console.



SPECIFICATIONS

μScope 820 Console Configuration

Several features of the console are directly determined by the probe being used with it. The instrument features that are determined by the 8080A interface probe are:

Single Registers — A, B, C, D, E, H, L

Double Registers — BC, DE, HL, PC, SP

CPU States — Flags, CPU pins (SYNC, RESET, HLDA, HOLD, READY, INT, INTE)

Trace/Breakpoint Word Size — 32 bits with 16 bits of address, 8 bits of data, and 8 bits of CPU status.

μScope 820 Console Interconnect

The probe interconnection to the μScope 820 console is accomplished via a 4-foot (1.2m) flat cable. 50-pin mating connectors plug into a board edge conector in the power cord compartment of the instrument and into a flat cable connector on the buffer box.

System Under Test (SUT) Interconnect

Interconnection from the buffer box to the SUT is accomplished with a 16-inch (406 mm) flat cable, complete with an integral ground plane, which is terminated with a low profile 40-pin DIP connector. The DIP connector is inserted into the SUT 8080A socket and the 8080A itself is plugged into the 40-pin socket provided on the probe buffer box.

Connections

Three external connections to the probe are provided:

50-pin flat cable connector on buffer box

40-pin zero insertion socket for the 8080A

40-pin low profile replaceable IC DIP connector for connection to SUT

Accessories Supplied

One μScope 820 system console overlay
One personality ROM
One hardware reference manual

Physical Characteristics

Probe Buffer Box

Height: 0.75 in. (19 mm)
Length: 7.25 in. (184 mm)
Width: 3.75 in. (95 mm)

User System Interconnect Cable

Width: 2¼ in. (57 mm)
Length: 16 in. (406 mm) flat cable

μScope 820 Console Personality ROM PC Card

Height: ¾ in. (19 mm)
Width: 2¼ in. (57 mm)
Length: 3¼ in. (83 mm)

Electrical Characteristics

All DC specifications are in addition to user system parameters. All capacitance values include cables and connectors.

Non-Intercepted Signals

ø1, ø2	± 10 μA max; 55 pF typ
A_{15}-A_0, D_7-D_0	−0.25 mA max @ 0.45V; 30 μA max @ 5.25V; 49 pF typ
+ 12V Supply	15 μA max
WAIT	35 pF typ (capacitance loading only)

Intercepted Signals

Outputs to User System	
SYNC	20 mA min @ 0.5V; −1 mA min @ 2.7V; 40 pF typ
HOLDA, INTE, DBIN, and $\overline{WR}$	4 mA min @ 0.4V; −0.2 mA min @ 2.7V; 40 pF typ
Inputs from User System	
INT, READY, RESET	40 μA max @ 2.7V; −0.72 mA max @ 0.4V; 50 pF typ
HOLD	60 μA max @ 2.7V; −1.08 mA max @ 0.4V; 50 pF typ

Power Requirements — Power supplied by μScope 820 Microprocessor System Console.

Environmental Characteristics

Operating Temperature — 0°C to 55°C (32°F to 130°F)

Storage Temperature — −40°C to 75°C (−40°F to 167°F)

Humidity — 95% RH, 15°C to 40°C (59°F to 104°F) noncondensing

Reference Manuals

9800526 — μScope 820 Operator's Manual (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

MPU SYSTEM

ORDERING INFORMATION

Part Number	Description
PRB-80	8080A interface probe

μSCOPE™ PROBE 8085

Provides interconnection for both 8085 and 8085A Microprocessor-based Systems to the μScope™ Microprocessor System Console

Comes complete with cable, buffer box, personality ROM, and μScope system console overlay

Has user system interconnect cable with integral ground plane for low noise operation

Increases diagnostic capability via four user positioned external inputs

Operates over a broad range of environmental conditions

Provides complete control over the system under test, yet causes minimal interference with system under test operation

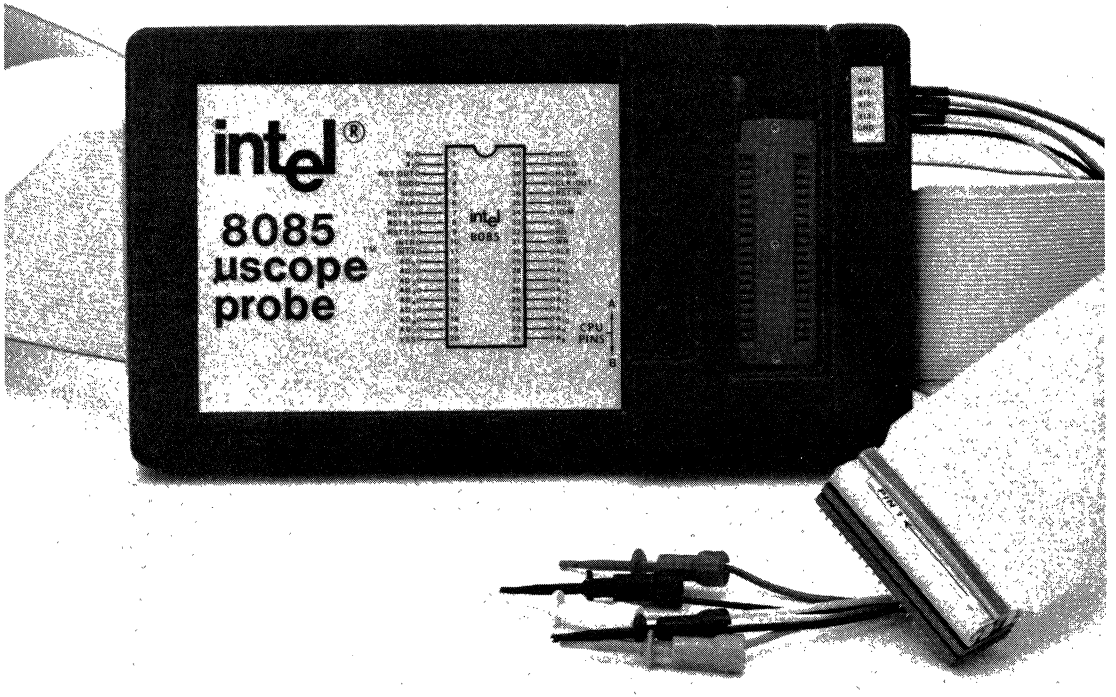
Fits securely in the console carrying case during transit

Provides complete protection for plug pins during transit

The probe 8085 provides the μScope Console with the ability to interact with 8085 and 8085A Microcomputer-based systems. The purpose of the probe is to interface the μScope Console to the CPU of the system under test (SUT). All of the interface signals and the associated circuitry have been designed to be effectively transparent to the SUT. CPU data, address, and clock lines are sensed by the probe 8085, with only the CPU control lines being switched. In addition, all SUT loading and timing degradations have been minimized by specially designed buffer circuitry.

The mechanical design of the probe is compact, rugged, and allows proper operation of the probe and the console over the full ambient range specified. The buffer circuitry and the ground plane design of the interconnect cable provide low noise electrical signals while allowing the SUT to be 4 feet from the system console.

The probe can be reconfigured to test either 8085 or 8085A microprocessor-based systems. The user can operate the microprocessor from either the system under test crystal or one adjacent to the probe 8085 CPU socket. User control of the probe interaction with CPU control signals insures maximum compatibility with the system under test. Test and diagnostic capability is increased by integrating four external inputs into the probe 8085.



MPU SYSTEM

GENERAL

μSCOPE CONSOLE INTERCONNECT

The probe interconnection to the μScope Console is accomplished via a 1.2m (4 ft.) flat cable. 50-pin mating connectors plug into a board edge connector in the power cord compartment of the instrument and into a flat cable connector on the buffer box.

SYSTEM UNDER TEST (SUT) INTERCONNECT

Interconnection from the buffer box to the SUT is accomplished with a 200mm (8 in.) flat cable, complete with an integral ground plane, which is terminated with a low profile 40-pin DIP connector. The DIP connector is inserted into the SUT 8085 socket and the 8085 itself is plugged into the 40-pin socket provided on the probe buffer box.

μSCOPE CONSOLE CONFIGURATION

Several features of the μScope Console are directly determined by the probe being used with it. The features that are determined by the 8085 interface probe are:

- Single Registers: A, B, C, D, E, H, L
- Double Registers: BC, DE, HL, PC, SP
- CPU States: Flags, CPU pins, Interrupt Masks, and Interrupt States
- Trace/Breakpoint Word Size: 32 bits with 16 bits of address, 8 bits of data and 8 bits of CPU status
- 4 external inputs included in the 8 bits of CPU status for examining, recording in trace memory, and transferring control

ELECTRICAL SPECIFICATIONS

All DC specifications are in addition to user system parameters. All capacitance values include cables and connectors.

Non-Intercepted Signals

x1, x2, reset out	16pF typical
AD_0-AD_7, A_8-A_{15}	-0.25 mA max @ 0.45V; 10 μA max @ 5.25V; 26 pF typical
SID	40 μA max @ 2.7V; -0.6 mA max @ 0.4V; 20 pF typical
SOD	20 μA max @ 2.7V; -0.4 mA max @ 0.4V; 20 pF typical

Intercepted Signals

Output to user system:

ALE	19 mA max @ 0.5 volt; -900 μA max @ 2.7 volt
CLK	2 mA max @ 0.64 volt; -400 μA max @ 2.6 volt
SS0, SSI	8 mA max @ 0.5 volt; -400 μA max @ 2.7 volt
RD, WR, IO/$\overline{M}$	24 mA max @ 0.5 volt; -2.6 mA max @ 2.4 volt
INTA	21 mA max @ 0.5 volt; -3.6 mA max @ 2.4 volt
HLDA	6 mA max @ 0.5 volt; -350 μA max @ 2.7 volt

All Output Signals have capacitance of 20pF typical.

Inputs from user system:

RESET IN, READY, HOLD, RST 6.5, RST 5.5, INTR, TRAP	-0.8 mA @ 0.4V; 40 μA max @ 2.7V; 20 pF typical
RST 7.5	-0.88 mA @ 0.4V; -0.25 mA max @ 2.7V; 20 pF typical

External Inputs:

XI0, XI1, XI2, XI3	-0.25 mA max @ 0.45V; 10 μA max @ 5.25V; 2.4V min Input High Voltage; 0.85V max Input Low Voltage

CONNECTIONS

Three external connections to the probe are provided:

- 50-pin flat cable connector on buffer box
- 40-pin zero insertion force socket for the 8085 SUT CPU
- 40-pin low profile replaceable IC DIP connector for connection to SUT

CHARACTERISTICS

PHYSICAL CHARACTERISTICS

Probe Buffer Box:

Height:	22mm (7/8 in.)
Length:	208mm (8-1/4 in.)
Width:	116mm (4-5/8 in.)

User System Interconnect Cable:

Width:	57mm (2-1/4 in.)
Length:	200mm (8 in.) flat cable

μScope Console Personality ROM PC Card:

Height:	19mm (3/4 in.)
Width:	57mm (2-1/4 in.)
Length:	86mm (3-1/4 in.)

POWER REQUIREMENTS

Power supplied by μScope Microprocessor System Console.

ENVIRONMENTAL CONDITIONS

Operating Temperature:	0° to 50°C (32° to 122°F)
Storage Temperature:	-40° to 75°C (-40° to 167°F)
Humidity:	95% RH, 15° to 40°C (59° to 104°F) noncondensing

ACCESSORIES SUPPLIED

One Probe 8085 overlay for the μScope System Console

One Personality ROM

One Operator's Manual

Four Test Probes for the External Inputs

MPU SYSTEM

ORDERING INFORMATION

Part Number	Description
PRB-85	8085 Interface Probe

MICROCOMPUTER TRAINING PROGRAMS

INTRODUCTION

Intel provides complete training for all its system related products. Courses are given regularly at Intel's training centers located in Santa Clara, California; Boston, Massachusetts; and Chicago, Illinois. These training centers are staffed by highly trained and experienced instructors. This section describes the overall program for microcomputer training and provides outlines for the following courses offered by Intel.

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PL/M-80 Language/Software Design 14-7
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PL/M-86 Language/Software Design 14-9
MCS-48 System 14-10

ADVANCED LEVEL

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MICROCOMPUTER TRAINING PROGRAMS

Courses presented at training centers and customer facilities

Training center locations
- **Boston**
- **Chicago**
- **Santa Clara**

Scheduled on a continuing basis throughout the year

Evening workshops

On-site courses tuned to customer requirements

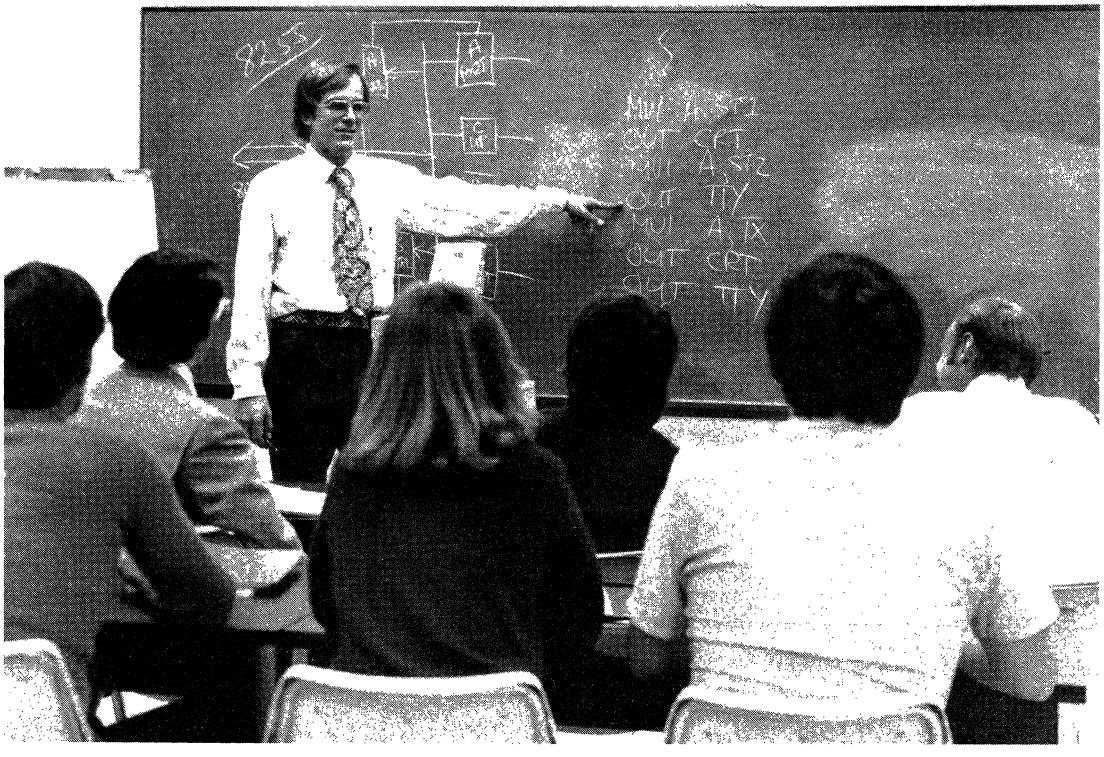
System demonstration

Hands-on laboratory sessions reinforce lecture

Training center classes limited to 15 attendees

Intellec microcomputer development systems with in-circuit emulators used in laboratory

Microcomputers are being used in hundreds of applications from simple controllers to complex data processing systems. To enable users to bring microcomputers into their applications, Intel offers a selection of workshops designed to provide users with the tools for making optimum use of Intel microcomputers in system development.



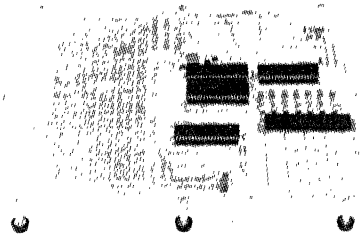
INTRODUCTION TO MICROCOMPUTERS

This workshop offers five days of lectures, questions and answers, practical learning, and hands-on training with your own microcomputer. You'll learn the fundamentals and general uses of microprocessors, and the basics of microcomputer-based design. The best learning will come from using and programming an operating SDK-85 System Design Kit (described below). When the training session is completed, an SDK-85 kit is yours to keep.

Attendees: One who has limited programming and design experience, and does not need to learn about development systems. A background in electronics is helpful but not necessary. (Maximum attendance is 20.)

Day 1
Introduction to Microcomputers
Computer Ogranization
Instruction Execution
Lab—Using Microcomputers
Day 2
Elementary Programming
Microcomputer Interfacing
Lab—Audio Oscillator Using Digital Techniques
Day 3
Computer Arithmetic
Conditional Jumps
Stacks and Subroutines
Push/Pop
Lab—Using Monitor Routine
Day 4
Interrupts
Computer Kit Hardware
Memory Systems
Decimal Arithmetic
Lab—A Digital Clock
Day 5
Introduction to Single Chip Microcomputers
Introduction to High Level Langnuages
Introduction to 16-Bit Microcomputers
Survey of Programming Aids

SPECIAL OFFER!



Included in the price of the course is an SDK-85 kit which includes:

3 MHz CPU (enhanced 8080)
Keyboard—24 keys
Display—6 digits
Monitor ROM 2048 bytes
RAM Memory 256 bytes
38 I/O lines
Teletype interface
Complete documentation

Table 1. Introduction to Microcomputers Course Outline

Microcomputer Concepts Workshop

The student will learn microcomputer terminology, run a microcomputer program, and gain insight in the development process and selecting the most appropriate microcomputer for an application.

Attendees: Project leaders, managers, administrative staff, or non-technical personnel who need a better understanding of microcomputer fundamental concepts.

Day 1	Day 2
Introduction Terminology SDK-85—Microcomputer Experiment iSBC Demonstration Development System Laboratory	Review Single Chip Design Example iSBC Design Example Hardware/Software Tradeoffs

Table 2. Microcomputer Concepts Workshop Course Outline

Development System Operations Workshop

This lab-intensive workshop teaches the student how to operate the Intellec Microcomputer Development System and the ISIS (Intel Systems Implementation Supervisor) disk operating system. Laboratory operations include editing data files, assembling and compiling programs, using relocation and linkage facilities, and identifying the correct documentation. This is not a programming course.

Attendees: A programmer who will be using the Intellec MDS. In addition, the technician, programmer-aid, or clerk who needs to operate the Intellec MDS can benefit from this course.

Day 1	Day 3
Introduction System Installation, Interconnections, Power-Up Utility Commands—COPY, DELETE, RENAME, DIR, ATTRIB Day 2 Review Edit—Build and Modify a File Compile Assemble	Review Link/Locate Diagnostic Programs BASIC-80 Identify Manuals

Table 3. Development System Operations Workshop Course Outline

COURSE DESCRIPTIONS

MCS-80/85 System Workshop

This workshop will prepare the student to design and develop a system using Intel 8080/8085 microprocessors by means of lectures, demonstrations, and laboratory "hands-on" experience with the Intellec Microcomputer Development System and an in-circuit emulator. The course outline for this workshop is presented in Table 4.

Prerequisites: A knowledge of binary and hexadecimal number systems and basic logic functions is recommended.

Day 1
Introduction
a. Microprocessor System
   1. Function
   2. Organization
   3. Programming
b. Central Processor Overview
   1. Functional Sections
   2. Programming Model
   3. Execution Sequence

Assembly Language Instructions
a. Input/Output
b. Register/Memory Reference
c. Arithmetic, Logical, Rotates

Input/Output Techniques
a. Programmed I/O
b. Interrupt I/O
c. Direct Memory Access

Programmed Input/Output
a. Status Request
b. Command
c. Data Transfer

Development System
a. Function
b. System Monitor
c. Disk Operating System

Debugging With the System Monitor
a. Break Points
b. Examine Registers

Laboratory
a. Using the System Monitor
b. Program Instruction Sequences
c. Debugging and Break Points

Day 2
Basic CPU Timing
a. Instruction Fetch
b. Bus Structure
c. Read/Write Timing

Subroutines
a. Invocation
b. Stack Memory
c. Parameters

Interrupt System
a. Description
b. RST Instruction
c. Service Subroutines

Disk Operating System Modules
a. Macro Assembler
b. Text Editor
c. File Utility Commands

Laboratory
a. Using the Disk Operating System
b. Program Assembly and Execution

Day 3
Programming Techniques
a. Branch Tables
b. Direct Load/Store Instructions
c. Special Purpose Instructions

8085 Timing
a. Ready/Wait
b. DMA/Hold

8085 Interrupts
a. RST 5.5, 6.5, 7.5
b. Trap
c. RIM, SIM

8080 vs. 8085
a. 8080 Chip Set
   1. 8228/8238 System Controller
   2. 8224 Clock Generator
b. 8080 Bus Structure
c. 8080 Instruction Timing

Memory Interfacing
a. RAM/ROM/PROM Address Decoding
b. 8708 PROM/8185 RAM

Laboratory
a. Program Design Using Development System
b. Program DEBUG Under Disk Operating System

Day 4
8085 CPU Set
a. 8085 Bus Structure
b. 8355/8755 ROM/EPROM and I/O
c. 8155 RAM/Timer and I/O

I/O Design
a. Memory-mapped
b. 8255 Parallel Interface
c. 8251 Serial Interface

In-Circuit Emulator
a. Prototype Development
b. Resource Sharing
c. Mapping Commands
d. Utility Commands
e. Debug Commands
f. Emulation Syntax

Laboratory
a. Use of the In-Circuit Emulator for System Debugging

Day 5
Relocation and Linkage
a. ISIS-II LINK and LOCATE Commands
b. Relocatable Libraries
c. Parameter Passing
d. System Design

Macros
Single Board Computers
a. Use as a System Component
b. Parallel I/O Options
c. Serial I/O Options
d. Interrupt System
e. Family Boards

Table 4. MCS-80/85 System Workshop Course Outline

PL/M-80 Language/Software Design Workshop

This workshop will prepare the student for designing, developing, and debugging modular PL/M-80 programs, by means of lectures, demonstrations, and laboratory "hands-on" experience with the Intellec Microcomputer Development System and an in-circuit emulator. The course outline for this workshop is presented in Table 5.

Prerequisites: A knowledge of binary and hexadecimal number systems and basic logic functions is required. To attain maximum benefit from course presentation, some background in logic design and computer programming is recommended.

Day 1
Introduction
a. Preview of Course
b. Overview of PL/M, Linking and Relocation
c. Why use a High Level Language
Definitions
Symbols, Identifiers, Reserved Words, Comments, Data Elements, Expressions, Statements, Declarations
Data Elements
Variables, Subscripted Variables, Data Type, Constants
Operators, Operations and Priorities
Arithmetic and Boolean
Evaluating Expressions
Statements
Redefine, Basic, Conditional
Assignment
a. Implement a Given Algorithm in PL/M

Day 2
ISIS-II Disc Operating System
a. Components of System
ISIS-II File Structure
a. System Files
b. User Files
c. Device Files
d. Directory and File Attributes
ISIS-II Commands
a. CUSPS—Commonly Used System Programs
b. Directory and Attribute Commands
c. Rename and Delete Commands
d. Creating System and User Discs
ISIS-II Editor
a. Definition of Terminology
b. Invoking the Editor
c. Editor Commands
d. Editing Existing Files
ISIS-II PL/M 80 Compiler
a. Invoking PL/M
b. Compiler Options
ISIS-II Locate
a. Invoking Locate
Laboratory
a. Introduction to ISIS-II Disc Operating System
b. Creating a PL/M Source File
c. Compiling a PL/M Program
d. Locating and Executing a PL/M Program

Day 3
Review
Procedures
a. Declaration
b. Invocation
c. Program Construction
Data References
a. Based Variables
b. Variable Equivalencing
Blocks
a. Concept and Use
b. Scope of Declarations
Predeclared Procedures
a. TIME, MOVE, LENGTH, LAST and SIZE Procedures
b. Type Transfers
c. Shifts and Rotates
The Memory Array and STACKPTR Variables
Laboratory
a. Compile and Locate Program
b. Execute Program

Day 4
Review
Modular Implementation
a. Compilation Modules
b. Modular Programming
ISIS-II Link
a. Invoking Link
b. Link Options
c. Assembly Object Modules
In-Circuit Emulator
a. Definition
b. System Overview
1. Memory and I/O Mapping
2. Breakpoint Capability
3. Dynamic Tracing
4. Control Block
In-Circuit Emulator Software Driver
a. Modes
b. Commands
System Debugging Examples
System Demonstration
Laboratory
a. Locate
b. Load and Emulate Using In-Circuit Emulator

Day 5
Review
Interrupt Procedures
Reentrant Procedures
ISIS-II Librarian
a. Creating a Library
b. Managing a Library
1. Adding Modules
2. Deleting Modules
ISIS-II System Interfaces
a. System Library
Discussion of Selected Programs
Laboratory
a. Create a Library
b. Link Object to a Library

Table 5. PL/M-80 Language/Software Design Workshop Course Outline

MCS-86 System Workshop

This workshop will prepare the student to develop assembly language programs and design systems based on the Intel 8086 microprocessor through the use of lecture, demonstration, and laboratory "hands-on" experience with the SDK-86 and the Intellec Microcomputer Development System. The course outline for this workshop is presented in Table 6.

Prerequisites: The student has programmed a computer in assembly language and, preferably, is familiar with the 8080/8085 microprocessor.

Day 1

Introduction
a. Microcomputer system
   1. Function
   2. Memory organization
   3. Interfacing
b. Central processor overview
   1. Programming
   2. Instruction format

Assembly Language Instruction
a. Register and data operations
   1. 8-bit
   2. 16-bit
b. I/O operations

System Design Kit (SDK-86)
a. Demonstration
b. Debugging

Laboratory
a. Using the SDK-86

Day 2

Review
CPU Architecture
a. Addressing modes

Procedures
a. Invocation
b. Stack management
c. Parameters

Day 3

Review
8086 CPU
a. Block diagram
b. Signal description

Interrupt System
a. Description
b. Signal pins

8259A — Priority Interrupt Control Unit
Development System
a. ISIS
b. Editor
c. Demonstration

Laboratory
a. Using the development system

Day 4

Review
Programming for Large Systems
a. Segmentation registers
b. Assembler
c. Linkage
d. Locate

Laboratory
a. Assembler programming techniques

Programming
a. Arithmetic
b. String operators

Day 5

CPU Timing
a. Read cycle
b. Memory access time
c. Write cycle

8284 — Clock Generator

8288 — Bus Controller

8282/3 — Octal Latch

8286/7 — Octal Transceiver

Single Board Computer
a. Design example

Other 8086 Configurations

Introduction to PL/M-86

Application Techniques

Table 6. MCS-86 System Workshop Course Outline

PL/M-86 Language/Software Design Workshop

This workshop will prepare the student for designing, developing, and debugging modular PL/M-86 programs using lecture, demonstration, and laboratory "hands-on" experience with the Intellec Microcomputer Development System. The course outline for this workshop is presented in Table 7.

Prerequisites: A knowledge of binary and hexadecimal number systems and basic logic functions is required. To attain maximum benefit from course presentation, some background in logic design and computer programming is recommended.

Day 1

Introduction
a. Preview of course
b. Overview of PL/M, linking and relocation
c. Why use a high level language

Definitions
a. Symbols, identifiers, reserved words, comments, data elements, expressions, statements, declarations

Data Elements
a. Variables, subscripted variables, constants

Data Types
a. Logical, integer, real

Operators, Operations and Priorities
a. Arithmetic and boolean

Evaluating Expressions

Statements
a. Redefine, basic, conditional

Assignment
a. Implement a given algorithm in PL/M

Day 2

ISIS-II Disk Operating System
a. Components of system

ISIS-II File Structure
a. System files
b. User files
c. Device files
d. Directory and file attributes

ISIS-II Commands
a. CUSPS — Commonly Used System Programs
b. Directory and attribute commands
c. Rename and delete commands
d. Creating system and user disks

ISIS-II Editor
a. Definition of terminology
b. Invoking the editor
c. Editor commands
d. Editing existing files

ISIS-II PL/M-86 Compiler
a. Invoking PL/M
b. Compiler options

ISIS-II LOC-86
a. Invoking LOC-86

Laboratory
a. Introduction to ISIS-II disk operating system
b. Creating a PL/M source file
c. Compiling a PL/M program
d. Locating and executing a PL/M program

Day 3

Review

Procedures
a. Declaration
b. Invocation
c. Program construction

Data References
a. Based variables
b. Variable equivalencing
c. Pointer type

Statement Labels

Unconditional Transfers

Blocks
a. Concept and use
b. Scope of declarations
c. Modular compilation
d. Modular program

ISIS-II LINK-86
a. Invoking LINK-86
b. Link options
c. Assembly object modules

Laboratory
a. Compile program modules
b. Link and locate modules
c. Execute program

Day 4

Review
ISIS-II LIB-86
a. Creating a library
b. Managing a library
   1. Adding modules
   2. Deleting modules

String Operations
a. Move bytes or words
b. Compare bytes or words
c. Find bytes or words
d. Skip bytes or words

The LOCKSET Procedure
a. Excluding mutual access

Laboratory
a. Create a library
b. Link object to a library
c. Locate

Day 5

Review
Interrupt Procedures

Reentrant Procedures

Predeclared Procedues
a. TIME, MOVE, LENGTH, LAST and SIZE procedures
b. Type transfers
c. Shifts and rotates

The Memory Array and STACKPTR Variables

Discussion of Selected Programs

Laboratory
a. Execution and debugging of selected programs

Table 7. PL/M-86 Language/Software Design Workshop Course Outline

MCS-48 System Workshop

This workshop will prepare the student to design and develop a system using the Intel 8049 microprocessor, by means of lectures, demonstrations, and laboratory "hands-on" experience with the Intellec Microcomputer Development System, the PROMPT-48, and an in-circuit emulator. The course outline for this workshop is presented in Table 8.

Prerequisites: A knowledge of binary and hexadecimal number systems and basic logic functions is required. To attain maximum benefit from course presentation, some background in logic design or computer programming is recommended.

Day 1
Orientation
Introduction
a. Microprocessor System
  1. Function
  2. Organization
  3. Programming
b. 8048 Overview
  1. Functional Sections
  2. Programming Model
  3. Execution Sequence
Assembly Language Instructions
a. I/O Instructions
b. Data Move Instructions
c. Increment/Decrement Instructions
d. Branch Instructions
e. Worksession No. 1
f. Accumulator Group Instructions
  1. ADD/ADDC
  2. Logicals
PROMPT-48
a. Function
b. Operation
Laboratory Exercise
a. Program Entry and Execution Using PROMPT-48

Day 2
Assembly Language Instructions
a. Accumulator Group Instructions
  1. Flags
  2. Rotates
b. Specials (XCH, DA, SWAP)
c. Worksession No. 2
d. Subroutines
  1. Invocation
  2. Stack Operation
e. Interrupt System
  1. Description
  2. Service Subroutines
  3. Multiple Source Systems
Development System
a. Function
b. Disk Operating System
Text Editor and Macro Assembler
a. Function
b. Operation
Laboratory Exercise
a. Bootstrap Procedures
b. Create, Edit, and Assemble Source Program
c. Execute Program

Day 3
System Timing
a. Basic Timing and Timer
b. Bus Timing for Peripheral Devices
Peripherals and Design
a. Expanding Memory
  1. Program Memory (1, 2K ROMs)
  2. Data Memory (RAMs)
b. Expanding Ports (8243)
  1. Device Characteristics
  2. Software Control of Ports
c. Combination Chips
  1. 8155 RAM and I/O Chip
  2. 8355, 8755 ROM and I/O Chip
d. Peripheral Interfacing (Parallel)
  1. 8255 Parallel I/O
  2. 8279 Keyboard and Display Interface
    —Keyboard Scanning Techniques
    —Display Refresh
Laboratory Exercise
a. Edit and Assemble Using DOS
b. Execute Using PROMPT-48

Day 4
Peripherals and Design
a. Peripheral Interfacing (Serial)
  1. Transmission Formats
  2. Asynchronous Operation
  3. RS232C Interface
In-Circuit Emulator
a. Prototype Development
b. Resource Sharing
c. Commands
  1. Mapping
  2. Utility
  3. Interrogation
  4. Emulation
Laboratory Exercise
a. Use of the In-Circuit Emulator for System Debugging

Day 5
8048 Family
a. 8049
b. 8041
  1. 8041/8048 Difference
  2. 8041 Slave/Master Protocol
c. 8021
d. 8022
Analog Interfacing
a. Successive Approximation A/D
b. A/D, D/A Chips
c. A/D Design
Laboratory

Table 8. MCS-48 System Workshop Course Outline

RMX/80 Real-Time Multi-Tasking Executive System Workshop

This workshop will cover the concepts of multi-tasking, i.e., what a task is, concurrency of tasks, asynchronous events, priorities and scheduling, resource sharing, interrupts, and inter-task communication. Also included will be discussions on sytem design, writing tasks, system generation, and debugging. The course outline for this workshop is presented in Table 9.

Prerequisites: Prior attendance at the PL/M-80 language/software design workshop. This may be satisfied with an equivalent knowledge of PL/M-80 language and compiler, ISIS-II utility facilities, ISIS-II relocation facilities, and modular systems programming.

Day 1
Introduction
What is RMX/80
a. Constituent Parts of the RMX/80 Product
b. Overview of the RMX/80 Development Process
Review of the Development Process
a. Intel 8080/8085 Translators
   1. Assembler
   2. PL/M-80 Compiler
b. ISIS-II Commands
c. LINKing Task Modules with the RMX/80 Nucleus and Intel Provided Tasks
d. LOCATEing the Final Module in an End Product Environment (Single Board Computer Modules)
e. Debugging the Task Environment
Real Time Asynchronous Event Processing
a. Definition of Terminology
b. Recognition of Asynchronous Events
   1. Polling (Status Loop)
   2. Preemption (Interrupt)
c. The Single Unit Program
   1. Status Environment
   2. Interrupt Environment
d. Program Execution
   1. Sequential Processing
   2. Concurrent Processing

Day 2
RMX/80 Model
a. Task
   1. Single Unit Program
b. Exchanges and Messages
   1. SEND Function
   2. WAIT Function
c. Context Switching and Dispatching of Tasks
d. A Sequential Model
e. A Concurrent Model
f. The Interrupt Exchange/Message
RMX/80 Terminal Handler
a. Message Formats
b. Service Request Exchanges
   1. Terminal Input (Line Edited)
   2. Terminal Output
c. Service Response Exchanges
Implementing an RMX Task(s) Module
a. Translator INCLUDE option
b. Creating a Task(s) Module
c. RMX/80 System Creation
d. Configuration Module
e. System Generation
Laboratory
a. Implementation of Two Modules
Day 3
Laboratory
a. Implement Configuration Module and System Generation
Use of In-Circuit Emulator to Emulate Task System
Terminal Handler
a. Line Edit Input
b. Control Character Table
c. Alarm Exchange—Alarm Message Type
d. DEBUGGER and Wakeup Exchange
DEBUGGER Task
a. Configuration
b. Invoking the DEBUGGER
c. DEBUGGER Commands
Day 4
RMX/80 Interrupt Processing
a. Interrupt Exchanges
b. Enabling and Disabling Interrupt Levels
c. Software Priorities and Interrupt Masking
d. User Defined Interrupt Handling
Line Printer Driver Task Example
a. Interrupt Handling
   1. Using RMX/80 Model
   2. User Defined Handler
Laboratory
a. Interrupt Handling
Day 5
Disk File System
a. Disk File System Services
b. Add-on ISIS-II Services
c. Configuration
   1. Free Space Manager
   2. Concurrent Operation
d. File System Structure
   1. Directory Format
   2. File Data Format
Laboratory
a. Disk File System

Table 9. RMX/80 Real-Time Multi-Tasking Executive System Workshop Course Outline

Advanced MCS-86 Assembly Language Workshop

This workshop will prepare the student to program the 8086 components in assembly language. The design and programming of large systems, use of Link, Locate, and Library, Input/Output controllers, and ICE-86 are included. This advanced course reviews material presented in the intermediate level MCS-86 System Workshop, and then proceeds to investigate these more advanced topics.

Prerequisite: MCS-86 System Workshop.

Length: 5 days

TOPICS INCLUDE:

- **Review of Instruction Set**
- **Assembler Directives**
- **Segmentation**
- **Programming of Input/Output Controllers**
- **ICE-86**
- **Reentrant Coding**
- **Interrupt Structures**
- **PL/M-86 Linkage**
- **iSBC 86/12**

Table 10. Advanced MCS-86 Assembly Language Workshop Course Outline

iSBC Design Project

The class is divided into teams and implements a project from given specifications. The system is built using several iSBC boards and is tested under ICE-85 (In-Circuit Emulator). The use of multiple processors is explored, and modular software development is emphasized.

Attendee: System designer or programmer and a graduate of an Intel workshop who wants more laboratory experience with the ICE-85 development tool, or who wants to design with iSBC boards. (Maximum attendance is 12.)

Prerequisite: MCS-80/85 System or PL/M-80 Language/Software Design Workshops.

Length: 5 days

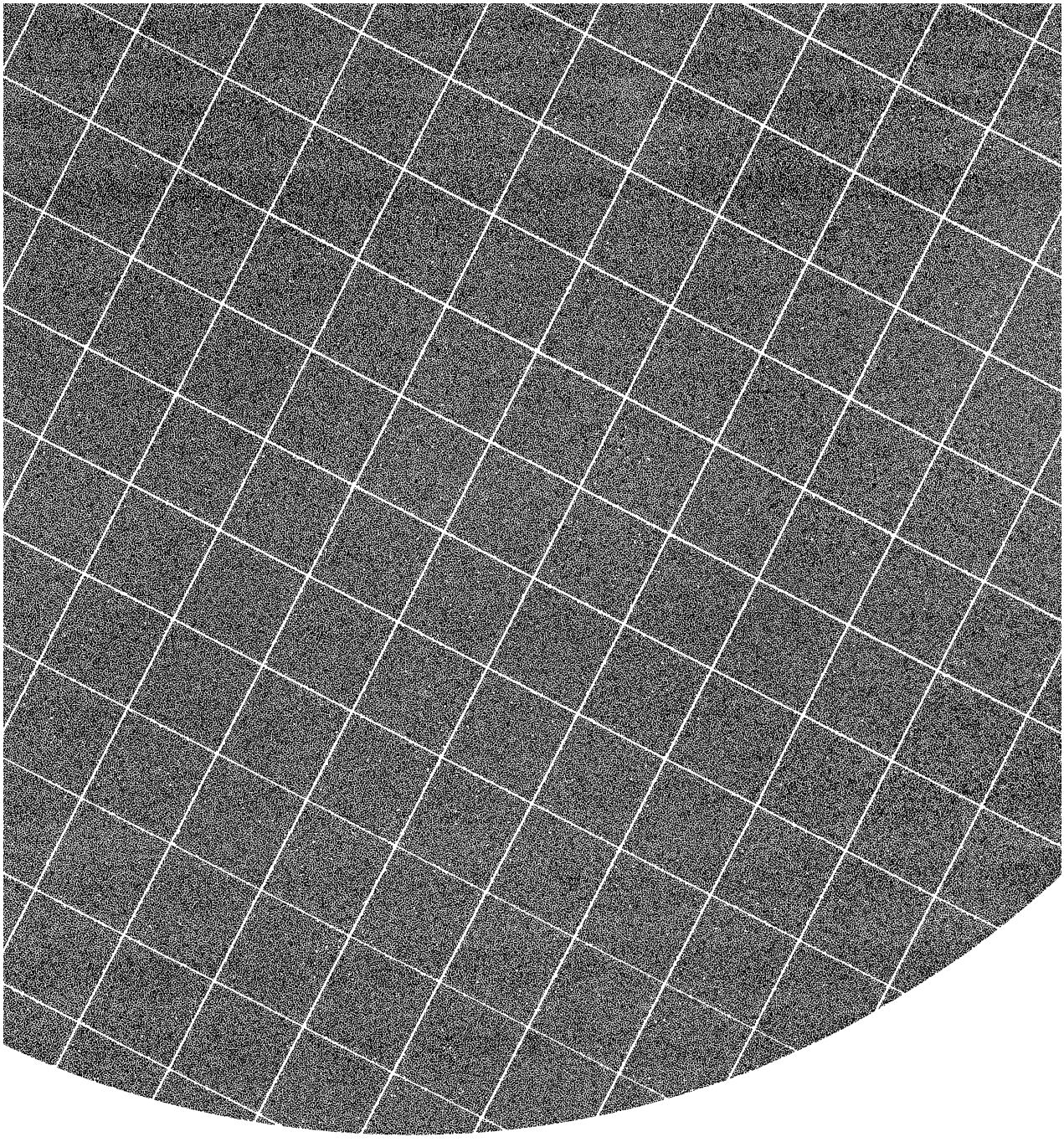
TOPICS INCLUDE:

- **iSBC Board Line Review**
- **Multibus Operation and Interfacing**
- **Design Specifications**
- **Project Team Organizations**
- **Module Development**
- **Module Documentation**
- **Software Integration**
- **ICE-85 Operation**
- **Semaphores and Multiprocessor Communication**
- **System Integration, Link/Locate**
- **System Testing and Evaluation**

Table 11. iSBC Design Project Course Outline

REGISTRATION AND ADDITIONAL INFORMATION

Contact MCSD Training at Intel Corporation, Santa Clara, California 95051, (408) 987-8003 or your local Intel sales office.



Industrial Grade Products

13

INTEL INDUSTRIAL GRADE PRODUCTS

Intel's industrial grade components are designed for extended operating temperature ranges (– 40°C to + 85°C). They have been designed for reliable operation in severe industrial environments, and are fully tested and burned-in before delivery.

This section offers preliminary data sheets which include functional description, pin-out description and block diagram.

For copies of complete data sheets when available, contact Intel literature department, M/S 4-903, 3065 Bowers Avenue, Santa Clara, CA 95051

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I2114
INDUSTRIAL GRADE
1024 x 4 BIT STATIC RAM

	2114-3	2114	2114L3	2114L
Max. Access Time (ns)	300	450	300	450
Max. Power Dissipation (mw)	575	575	410	410

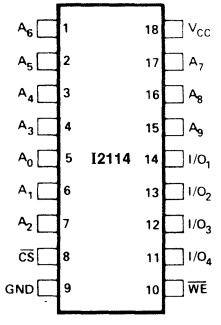
- **High Density 18 Pin Package**
- **Identical Cycle and Access Times**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **Industrial Temperature Range −40°C to +85°C**

The Intel® I2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

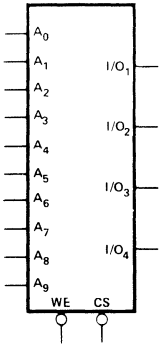
The I2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The I2114 is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

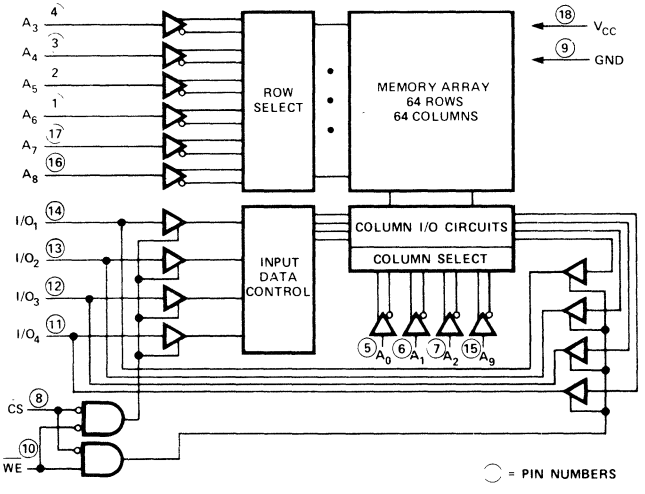
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

INDUSTRIAL GRADE

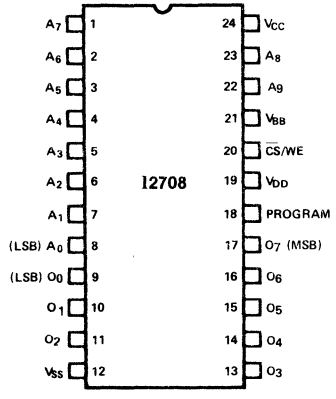
I2708/I8708*
INDUSTRIAL GRADE
8K UV ERASABLE PROM

	Max. Power	Max. Access	Organization
I2708	800 mW	450 ns	1K x 8

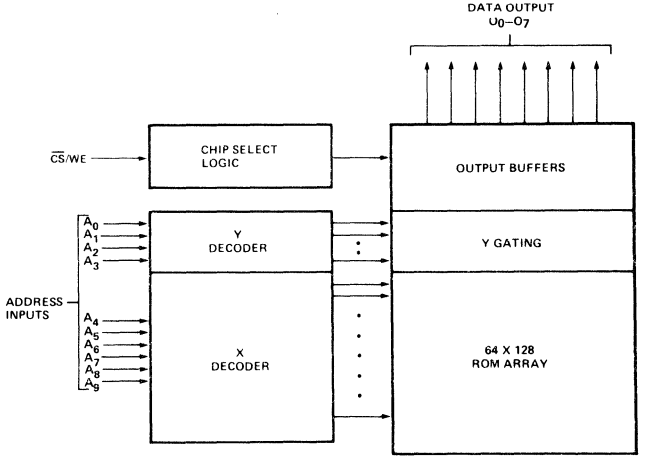
- **Industrial Grade Temperature Range: −40°C to +85°C**
- **Fast Access Time — 450 ns Max**
- **Static — No Clocks Required**
- **Data Inputs and Outputs TTL Compatible during both Read and Program Modes**
- **Three-State Outputs — OR-Tie Capability**

The Intel® Industrial Grade I2708 is a 8192-bit ultraviolet light erasable and electrically reprogrammable EPROM, ideally suited where fast turnaround and pattern experimentation are important requirements. All data inputs and outputs are TTL compatible during both the read and program modes. The outputs are three-state, allowing direct interface with common system bus structures. The I2708 is fabricated with the N-channel silicon gate FAMOS technology and is available in a 24-pin dual in-line package.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS/INPUTS
$\overline{CS}/WE$	CHIP SELECT/WRITE ENABLE INPUT

PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1-8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}/WE$ 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED 26V	+12	V_{IHW}	-5	+5

INDUSTRIAL GRADE

I2716
INDUSTRIAL GRADE
16K (2K x 8) UV ERASABLE PROM

- **Fast Access Time: 450 ns Max**
- **Industrial Grade Temperature Range: −40°C to +85°C**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— 603 mW Max. Active Power**
  - **— 165 mW Max. Standby Power**
- **Simple Programming Requirements**
  Single Location Programming
  Programs with One 50 ms Pulse
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

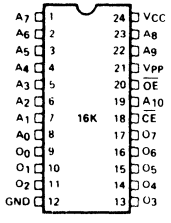
The Intel® Industrial Grade I2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The I2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The I2716, with its single 5-volt supply and with an access time of 450 ns max, is ideal for use with the newer high performance industrial grade +5V microprocessors such as Intel's I8085 and I8086. The I2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 603 mW while the maximum standby power dissipation is only 165 mW, a 75% savings.

The I2716 has the simplest and fastest method yet devised for programming EPROMs—single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the I2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION

I2716



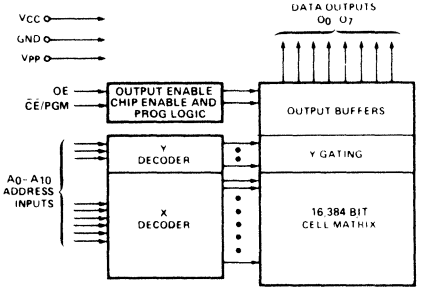
PIN NAMES

A_0–A_{10}	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



INDUSTRIAL GRADE

I8048/I8648/I8748/I8035
INDUSTRIAL TEMPERATURE RANGE
SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8048 Mask Programmable ROM**
- **8648 One-Time Factory Programmable EPROM**
- **8748 User Programmable/Erasable EPROM**
- **8035/8035L External ROM or EPROM**
- **−40°C to +85°C Operation**

- **8-Bit CPU, ROM, RAM, I/O in Single Package**
- **Interchangeable ROM and EPROM Versions**
- **Single 5V Supply**
- **2.5 μsec and 5.0 μsec Cycle Versions: All instructions 1 or 2 Cycles**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 ROM/EPROM 64 x 8 RAM 27 I/O LINES**
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Single Level Interrupt**

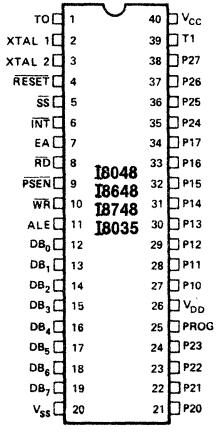
The Intel® 8048/8648/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8035 is the equivalent of an 8048 without program memory. The 8035L has the RAM power-down mode of the 8048 while the 8035 does not. The 8648 is a one-time programmable (at the factory) 8748 which can be ordered as the first 25 pieces of a new 8048 ROM order. The substitution of 8648's for 8048's allows for very fast turnaround for initial code verification and evaluation units.

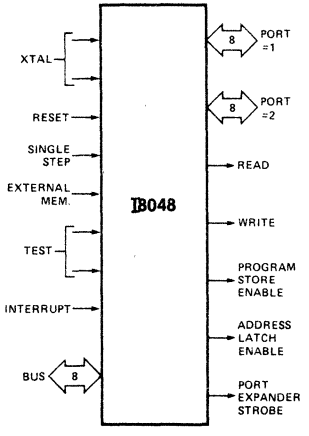
To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the 8048 with factory-programmed mask ROM program memory for low cost, high volume production, and the 8035 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

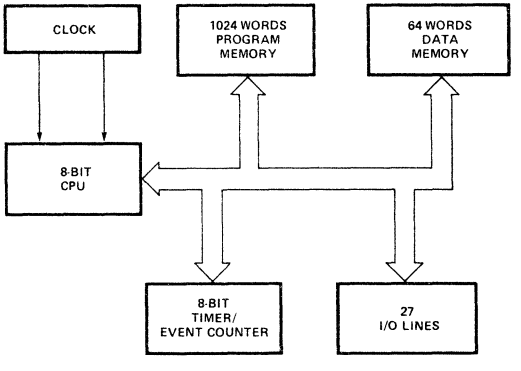
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



INDUSTRIAL GRADE

I8155/I8156
2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

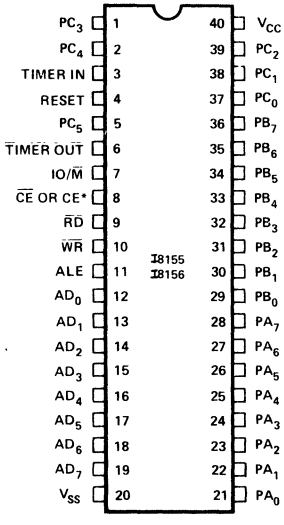
- **Industrial Temperature Range (−40°C to +85°C)**
- **256 Word x 8 Bits**
- **Single +5V Power Supply**
- **Completely Static Operation**
- **Internal Address Latch**
- **2 Programmable 8 Bit I/O Ports**
- **1 Programmable 6-Bit I/O Port**
- **Programmable 14-Bit Binary Counter/ Timer**
- **Multiplexed Address and Data Bus**
- **40 Pin DIP**

The I8155 and I8156 are RAM and I/O chips to be used in the MCS-85™ microcomputer system. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in I8085A CPU.

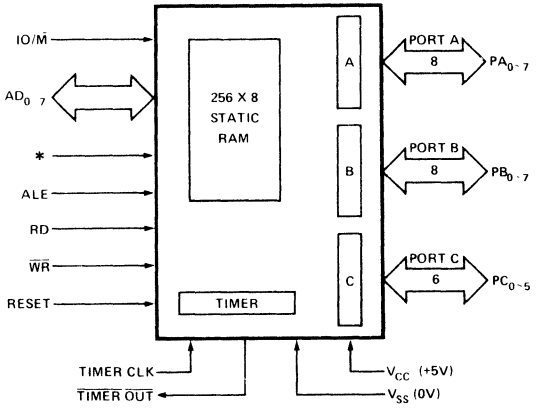
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



*: I8155 = $\overline{CE}$, I8156 = CE

INDUSTRIAL GRADE

I8212
8-BIT INPUT/OUTPUT PORT

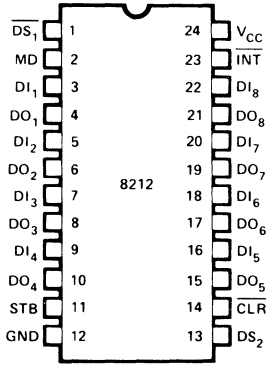
- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current — .25mA Max.**
- **Three State Outputs**
- **Outputs Sink 15mA**
- **3.65V Output High Voltage for Direct Interface to 8008, 8080A, or 8085A CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches and Multiplexers in Microcomputer Systems**
- **−40°C to +85°C Temp Range**

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

Note: The specifications for the 3212 are identical with those for the 8212.

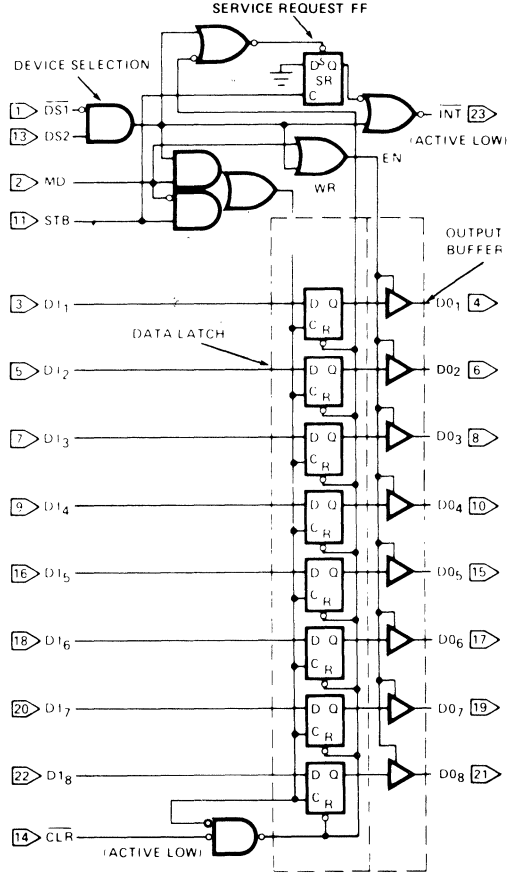
PIN CONFIGURATION



PIN NAMES

DI_1 DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



INDUSTRIAL GRADE

I8216/8226
4 BIT PARALLEL BIDIRECTIONAL BUS DRIVER

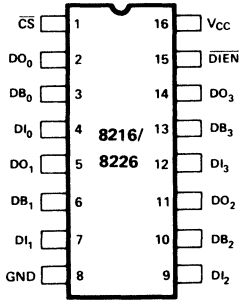
- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current — .25 mA Maximum**
- **High Output Drive Capability for Driving System Data Bus**
- **3.65V Output High Voltage for Direct Interface to 8080 CPU**
- **Three State Outputs**
- **Reduces System Package Count**
- **−40°C to +85°C Temp Range**

The 8216/8226 is a 4-bit bi-directional bus driver/receiver.

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50mA I_{OL} capability.

A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

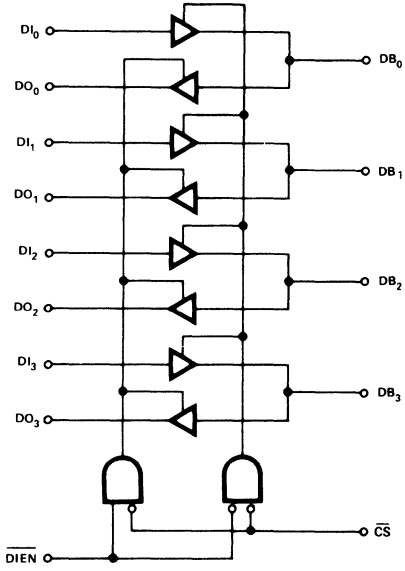
PIN CONFIGURATION



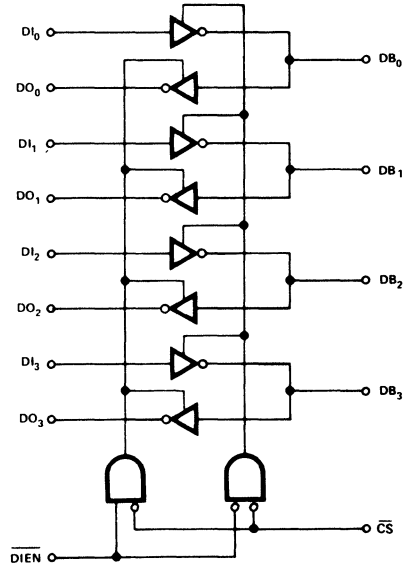
PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM 8216



LOGIC DIAGRAM 8226



INDUSTRIAL GRADE

I8243
MCS-48™ INPUT/OUTPUT EXPANDER

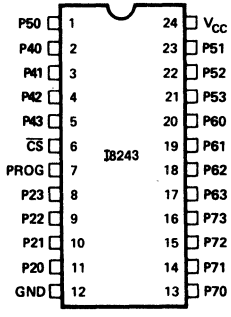
- −40°C to +85°C Operation
- Low Cost
- Simple Interface to MCS-48™ Microcomputers
- Four 4-Bit I/O Ports
- AND and OR Directly to Ports
- 24-Pin DIP
- Single 5V Supply
- High Output Drive
- Direct Extension of Resident 8048 I/O Ports

The Intel® 8243 is an input/output expander designed specifically to provide a low cost means of I/O expansion for the MCS-48™ family of single chip microcomputers. Fabricated in 5 volts NMOS, the 8243 combines low cost, single supply voltage and high drive current capability.

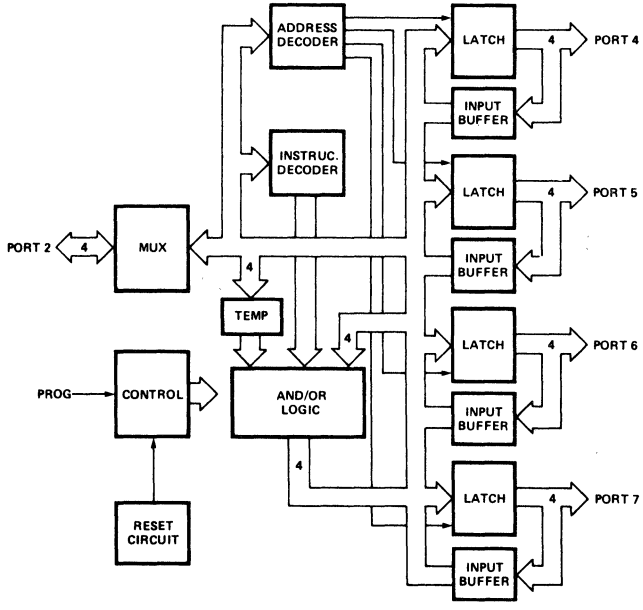
The 8243 consists of four 4-bit bidirectional static I/O ports and one 4-bit port which serves as an interface to the MCS-48 microcomputers. The 4-bit interface requires that only 4 I/O lines of the 8048 be used for I/O expansion, and also allows multiple 8243's to be added to the same bus.

The I/O ports of the 8243 serve as a direct extension of the resident I/O facilities of the MCS-48 microcomputers and are accessed by their own MOV, ANL, and ORL instructions.

PIN CONFIGURATION



BLOCK DIAGRAM



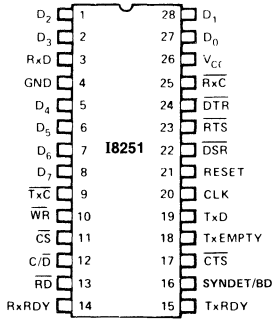
INDUSTRIAL GRADE

I8251
PROGRAMMABLE COMMUNICATION INTERFACE

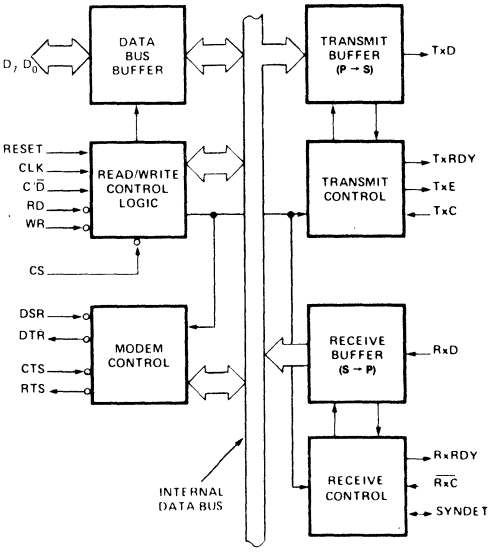
- **Synchronous and Asynchronous Operation**
- **Synchronous 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion**
- **Asynchronous 5-8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling.**
- **Industrial Grade Temperature Range −40°C to +85°C**
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun and Framing**
- **28-Pin DIP Package**
- **All Inputs and Outputs are TTL Compatible**
- **Single +5V Supply**
- **Single TTL Clock**

The Intel® I8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's new high performance family of microprocessors such as the 8085. The I8251 is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is constructed using N-channel silicon gate technology.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D_7 D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char from 8080)

$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

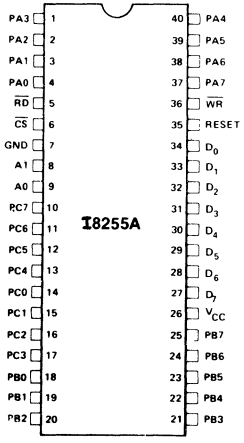
INDUSTRIAL GRADE

I8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- **Extended Temperature Range (−40°C to +85°C)**
- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Improved Timing Characteristics**
- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40-Pin Dual In-Line Package**
- **Reduces System Package Count**
- **Improved DC Driving Capability**

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

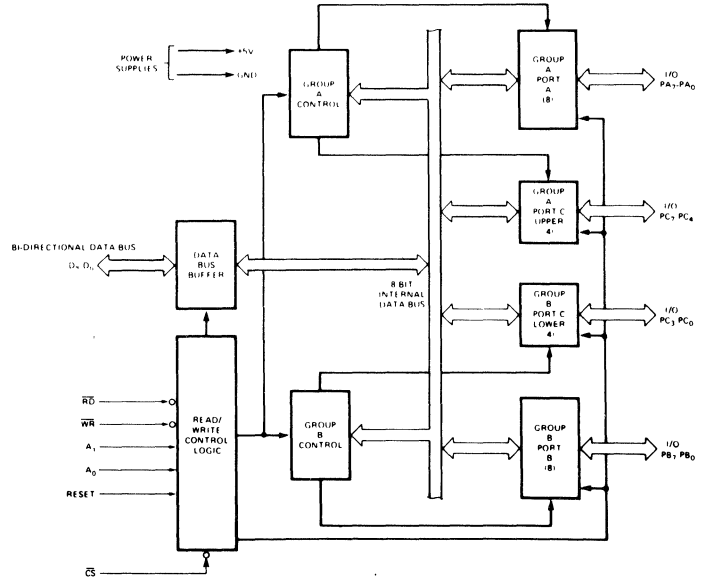
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	Ø VOLTS

8255A BLOCK DIAGRAM



INDUSTRIAL GRADE

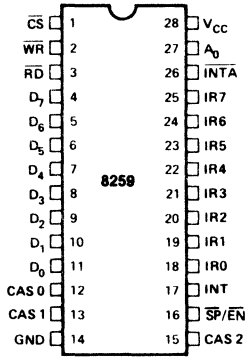
I8259
PROGRAMMABLE INTERRUPT CONTROLLER

- **MCS-86™ Compatible**
- **MCS-80/85™ Compatible**
- **Eight-Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes**
- **Individual Request Mask Capability**
- **Single +5V Supply (No Clocks)**
- **−40°C to +85°C Temp. Range**

The Intel® 8259 Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259 is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

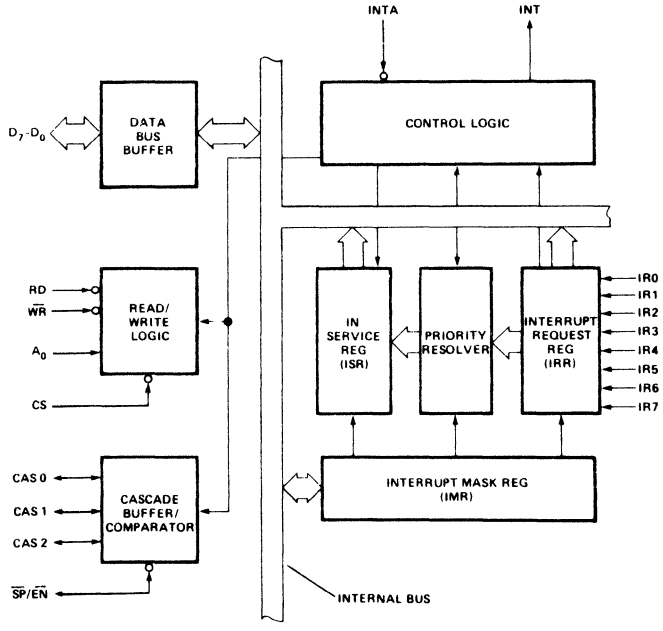
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS2-CAS0	CASCADE LINES
$\overline{SP}/\overline{EN}$	SLAVE PROGRAM INPUT/ENABLE
INT	INTERRUPT OUTPUT
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE INPUT
IR0-IR7	INTERRUPT REQUEST INPUTS

BLOCK DIAGRAM



INDUSTRIAL GRADE

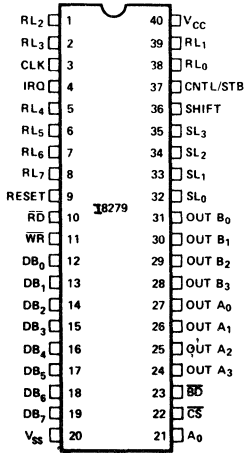
I8279
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- **Extended Temperature Range (−40°C to +85°C)**
- **Simultaneous Keyboard Display Operations**
- **Scanned Keyboard Mode**
- **Scanned Sensor Mode**
- **Strobed Input Entry Mode**
- **8-Character Keyboard FIFO**
- **2-Key Lockout or N-Key Rollover with Contact Debounce**
- **Dual 8- or 16-Numerical Display**
- **Single 16-Character Display**
- **Right or Left Entry 16-Byte Display RAM**
- **Mode Programmable from CPU**
- **Programmable Scan Timing**
- **Interrupt Output on Key Entry**

The Intel® 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel® microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16X8 display RAM which can be organized into dual 16X4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

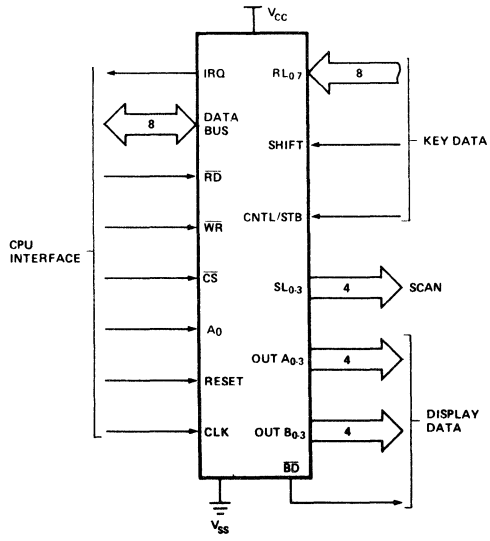
PIN CONFIGURATION



PIN NAMES

DB_{0-7}	I/O	DATA BUS (BI DIRECTIONAL)
CLK	I	CLOCK INPUT
RESET	I	RESET INPUT
$\overline{CS}$	I	CHIP SELECT
$\overline{RD}$	I	READ INPUT
$\overline{WR}$	I	WRITE INPUT
A_0	I	BUFFER ADDRESS
IRQ	O	INTERRUPT REQUEST OUTPUT
SL_{0-3}	O	SCAN LINES
RL_{0-7}	I	RETURN LINES
SHIFT	I	SHIFT INPUT
CNTL/STB	I	CONTROL/STROBE INPUT
OUT A_{0-3}	O	DISPLAY (A) OUTPUTS
OUT B_{0-3}	O	DISPLAY (B) OUTPUTS
$\overline{BD}$	O	BLANK DISPLAY OUTPUT

LOGIC SYMBOL



INDUSTRIAL GRADE

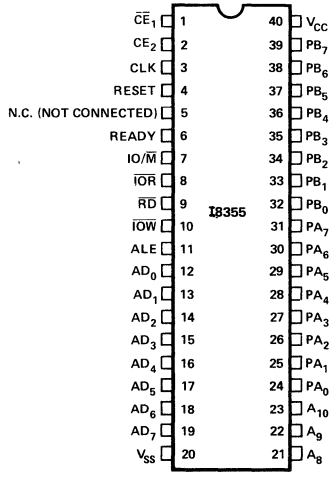
I8355*
16,384-BIT ROM WITH I/O
*Directly Compatible with I8085A CPU

- Industrial Temperature Range (−40°C to +85°C)
- 2048 Words x 8 Bits
- Single +5V Power Supply
- Internal Address Latch
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40-Pin DIP

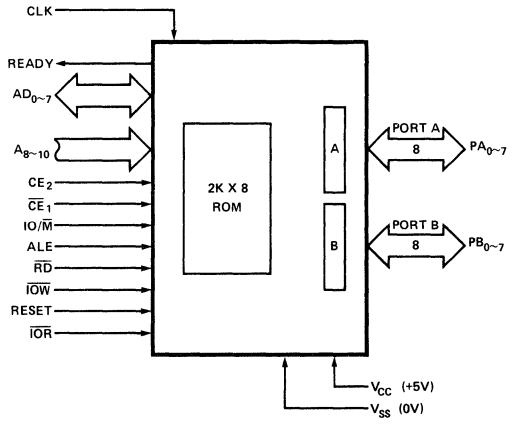
The Intel® 8355 is a ROM and I/O chip to be used in the MCS-85™ microcomputer system. The ROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 400 ns to permit use with no wait states in the I8085A CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is indivdually programmable as input or output.

PIN CONFIGURATION



BLOCK DIAGRAM



INDUSTRIAL GRADE

I8755A-8
16,384-BIT EPROM WITH I/O

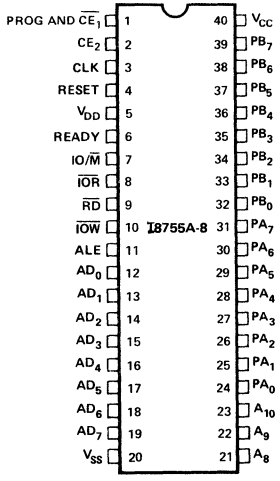
• Directly Compatible with I8085A CPU

- **Industrial Temperature Range (−40°C to +85°C)**
- **2048 Words × 8 Bits**
- **Single +5V Power Supply (V_{CC})**
- **U.V. Erasable and Electrically Reprogrammable**
- **Internal Address Latch**
- **2 General Purpose 8-Bit I/O Ports**
- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **40-Pin DIP**

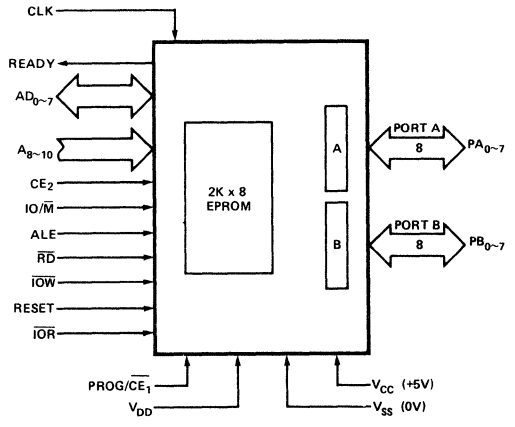
The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the MCS-85™ microcomputer system. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 750 ns to permit use with one wait state in a 3 MHz 8085A system.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

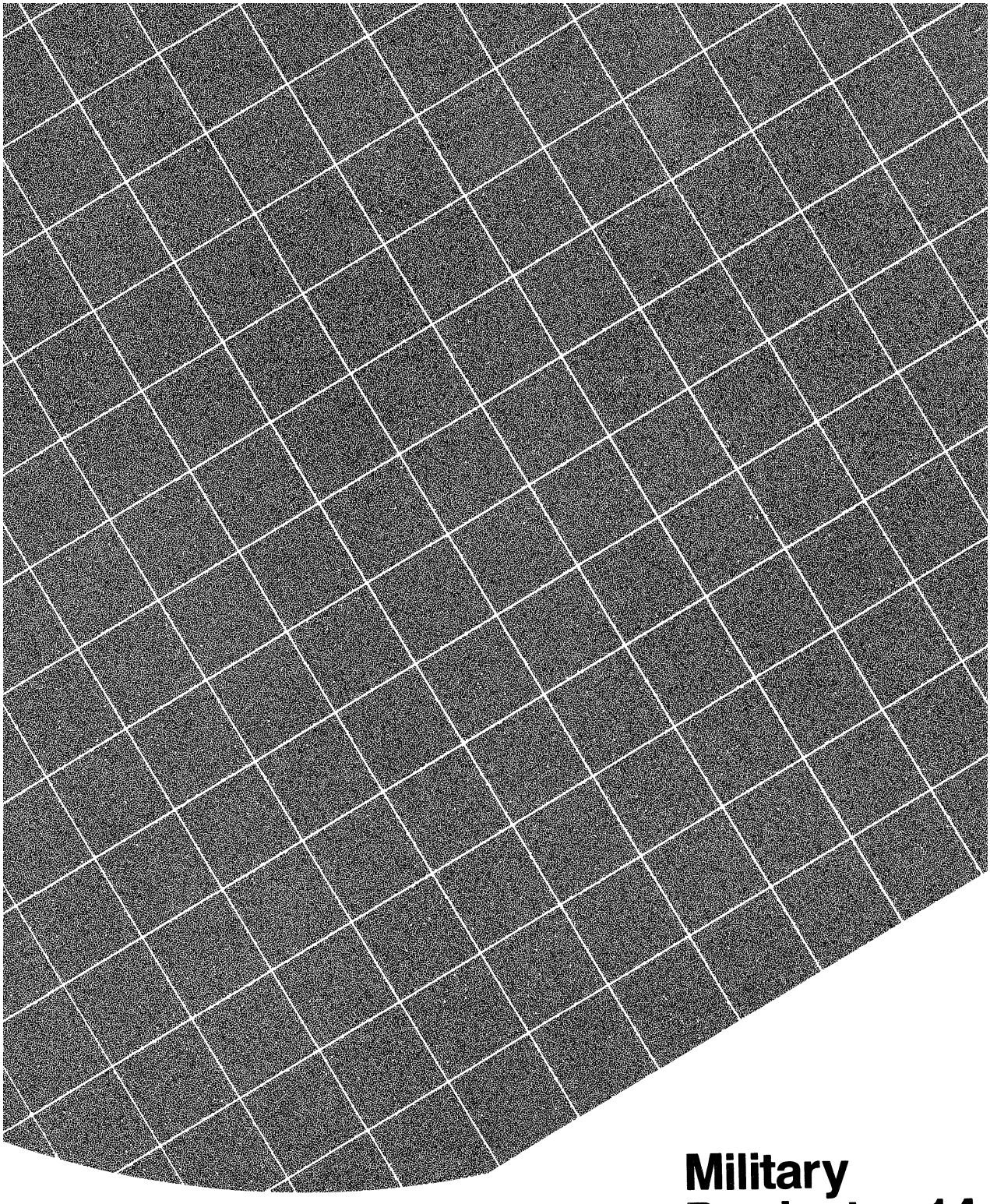
PIN CONFIGURATION



BLOCK DIAGRAM



INDUSTRIAL GRADE



Military Products 14

INTEL MILITARY PRODUCTS

In 1977, Intel qualified the first military microprocessor to MIL-M-38510. The JAN version of the industry standard 8080A is listed in QPL, Part I as M38510/42001BQB.

Intel also offers an extensive family of selected microprocessor and memory components for military/hi-rel applications. All standard military products are screened to full Level B requirements of MIL-STD-883B, Method 5004. Additionally, complete lot conformance testing is performed in accordance with MIL-STD-883B, Method 5005.

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MILITARY PRODUCT REQUIREMENTS

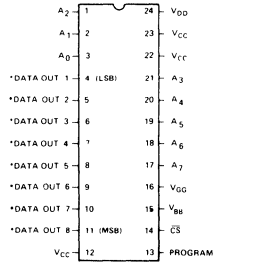
General Requirements	MIL-M-38510 Requirements	JAN (Level B)	883 (Level B)
CERTIFICATION			
A. Product Assurance Program Plan	Para. 3.4.1.2	X	N/A
B. Manufacturer's Certification	Para. 3.4.1.2.1	X	N/A
DEVICE QUALIFICATION	Para. 4.4	X	N/A
TRACEABILITY	Para. 3.4.6	X	N/A
COUNTRY OF MANUFACTURE	Para. 3.2.1	X	N/A
Screening Test Requirements	**Screening Per Method 5004 of MIL-STD-883**		
INTERNAL VISUAL	2010, Cond. B	100%	100%
STABILIZATION BAKE	1008, Cond. C (24 Hrs. @ 150°C)	100%	100%
TEMPERATURE CYCLING	1010, Cond. C (10 cycles −65°C to +150°C)	100%	100%
CONSTANT ACCELERATION	2001, Cond. D or E As Applicable	100%	100%
SEAL (HERMETICITY)	1014		
A. Fine	Cond. B (5 x 10 atm-cc/sec)	100%	100%
B. Gross	Cond. C		
PRE BURN-IN ELECTRICAL	Per Applicable Device Specification	100%	100%
BURN-IN	1015, Cond. C or F (160 Hrs. @ 125°C)	100%	100%
FINAL ELECTRICAL TESTS			
A. Static (@ 25°C, Min and Max Rated Temp)	Per Applicable Device Specification	100%	100%
B. Dynamic and Functional (@ 25°C)	Per Applicable Device Specification	100%	100%
EXTERNAL VISUAL	2009	100%	100%
Quality Conformance Inspection Tests	**Per MIL-STD-883, Method 5005**	**JAN (Level B)**	**883 (Level B)**
GROUP A Electrical Tests	Per Applicable Device Specification. Table I, Subgroups as Required	Every Inspection Lot	Every Inspection Lot
GROUP B Package Function and Mechanical Tests	Per Table IIb, Subgroups 1-3	Every 6 Weeks	Every 6 Weeks
GROUP C Die Related Tests	Per Table III, Subgroups 1 and 2	Every 12 Weeks	Every 12 Weeks
GROUP D Package Related Tests	Per Table IV, Subgroups 1-5	Every 6 Months	Every 6 Months

M1702A
2K (256 x 8) UV ERASABLE PROM
–55°C to +100°C OPERATION

- **Fast Access Time: Max. 850ns**
- **Completely Static**
- **Inputs and Outputs DTL and TTL Compatible**
- **All 2048 Bits Factory Tested Prior to Shipment**
- **Three-State Output**
- **24 Pin Dip**

The Intel® M1702A is a 256-word by 8-bit ultraviolet light erasable and electrically reprogrammable EPROM which is specified over the –55°C to +100°C temperature range. The M1702A has a transparent lid which allows the user to expose the M1702A to UV light to erase the bit pattern. A new pattern can then be written into the device.

PIN CONFIGURATION



*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

*REFER TO THE 1702A DATA SHEET FOR PIN CONNECTIONS DURING READ AND PROGRAM

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . –65°C to 110°C
Storage Temperature . . . . . –65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to –20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . –48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS
READ OPERATION

T_A = -55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = -9V ±10%, V_{GG} = -9V ±10% unless otherwise noted.

Symbol	Test	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			10	μA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{IH2}
I_{DD1}[1]	Power Supply Current		35	50	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$ = 0.0V, I_{OL} = 0.0mA, T_A = 25°C, Continuous
I_{DD3}	Power Supply Current		38	65	mA	$\overline{CS}$ = V_{IH2}, I_{OL} = 0.0mA, T_A = -55°C, Continuous
I_{CF}	Output Clamp Current		8	11	mA	V_{OUT} = -1.0V, T_A = -55°C, Continuous
I_{GG}	Gate Supply Current			10	μA	
V_{IL1}	Input Low Voltage for TTL Interface	-1		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}-6	V	
V_{IH1}	Address Input High Voltage	V_{CC}-2		V_{CC}+0.3	V	
V_{IH2}	Chip Select Input High Voltage	V_{CC}-1.5		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	-2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		-3	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = -200μA

Note 1. Typical values are at nominal voltages and T_A = 25°C.

MILITARY

A.C. CHARACTERISTICS

T_A = -55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = -9V ±10%, V_{GG} = -9V ±10% unless otherwise noted.

Symbol	Test	Limits Min.	Limits Max.	Unit
Freq.	Repetition Rate		1.2	MHz
t_{OH}	Previous Read Data Valid		0.1	μs
t_{ACC}	Address to Output Delay		0.85	μs
t_{CS}	Chip Select Delay		0.5	μs
t_{CO}	Output Delay From $\overline{CS}$		0.35	μs
t_{OD}	Output Deselect		0.3	μs

CAPACITANCE * T_A = 25°C

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$, $\overline{CS} = V_{CC}$ — All unused pins
C_{OUT}	Output Capacitance	10	15	pF	$V_{OUT} = V_{CC}$, $V_{GG} = V_{CC}$ — are at A.C. ground

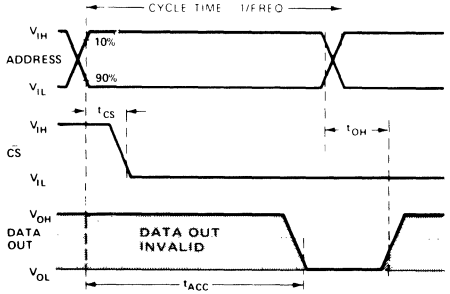
*This parameter is sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

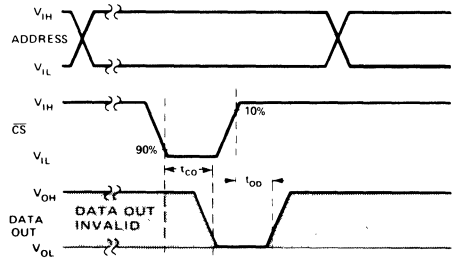
Conditions of Test:

Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns
Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns), C_L=15pF

A) READ OPERATION



B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION



ERASING AND PROGRAMMING PROCEDURE

The erasing and programming procedure of the M1702A is the same as the 0°C to 70°C 1702A. The procedure is described in the Data Catalog PROM/ROM Programming Instructions section.

M2114
1024 x 4 BIT STATIC RAM

	2114-3	2114	2114L3	2114L
Max. Access Time (ns)	300	450	300	450
Max. Power Dissipation (mw)	575	575	410	410

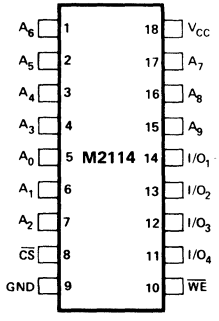
- **High Density 18 Pin Package**
- **Identical Cycle and Access Times**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **Military Temperature Range -55°C to +125°C**

The Intel® M2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

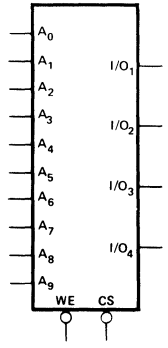
The M2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The M2114 is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

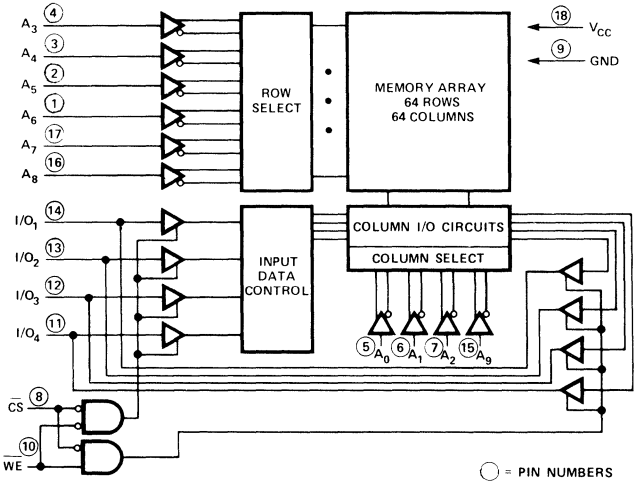
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

MILITARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-65°C to +150°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1.0W
D.C. Output Current	5mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = -55°C to +125°C, V_{CC} = 5V ± 10%, unless otherwise noted.

SYMBOL	PARAMETER	M2114, M2114-3			M2114L3, M2114L3			UNIT	CONDITIONS
		Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (All Input Pins)			10			10	µA	V_{IN} = 0 to 5.5V
$\|I_{LO}\|$	I/O Leakage Current			10			10	µA	$\overline{CS}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		80	95			65	mA	V_{IN} = 5.5V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current			105			75	mA	V_{IN} = 5.5V $I_{I/O}$ = 0 mA, T_A = -55°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	6.0		2.1	6.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	-1.0	-1.4		-1.0	-1.4		mA	V_{OH} = 2.4V
I_{OS}[2]	Output Short Circuit Current			40			40	mA	

NOTE: 1. Typical values are for T_A = 25° C and V_{CC} = 5.0V.
2. Duration not to exceed 30 seconds.

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = OV
C_{IN}	Input Capacitance	5	pF	V_{IN} = OV

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0.8 Volt to 2.0 Volt
Input Rise and Fall Times	10 nsec
Input and Output Timing Levels	1.5 Volts
Output Load	1 TTL Gate and C_L = 100 pF

TEST NOTE: This circuit employs a self starting oscillator and a charge pump which require a certain amount of time after POWER ON to start functioning properly. This M2114 circuit is conservatively specified as requiring 500 µsec after V_{CC} reaches its specified limits (4.50V).

A.C. CHARACTERISTICS $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	M2114, M2114L		M2114-3, M2114L3		UNIT
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	450		300		ns
t_A	Access Time		450		300	ns
t_{CO}	Chip Selection to Output Valid		120		100	ns
t_{CX}	Chip Selection to Output Active	20		20		ns
t_{OTD}	Output 3-state from Deselection		100		80	ns
t_{OHA}	Output Hold from Address Change	50		50		ns

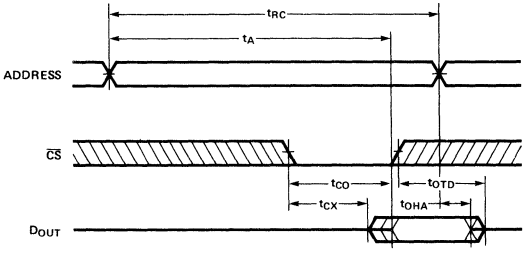
WRITE CYCLE [2]

SYMBOL	PARAMETER	M2114, M2114L		M2114-3, M2114L3		UNIT
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	450		300		ns
t_W	Write Time	200		150		ns
t_{WR}	Write Release Time	0		0		ns
t_{OTW}	Output 3-state from Write		100		80	ns
t_{DW}	Data to Write Time Overlap	200		150		ns
t_{DH}	Data Hold From Write Time	0		0		ns

NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

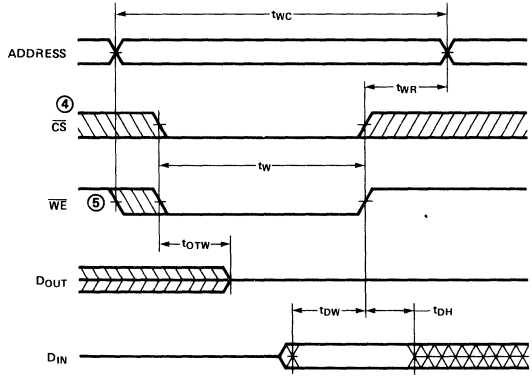
WAVEFORMS

READ CYCLE ③



NOTES:
③ $\overline{WE}$ is high for a Read Cycle.
④ If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
⑤ $\overline{WE}$ must be high during all address transitions.

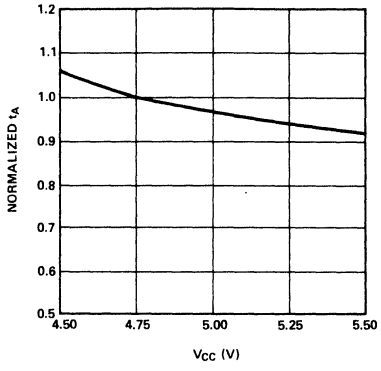
WRITE CYCLE



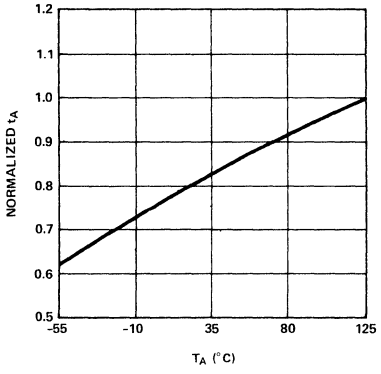
MILITARY

TYPICAL D.C. AND A.C. CHARACTERISTICS

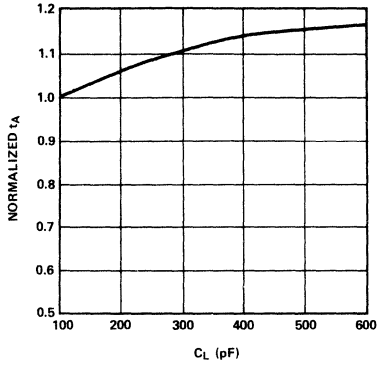
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



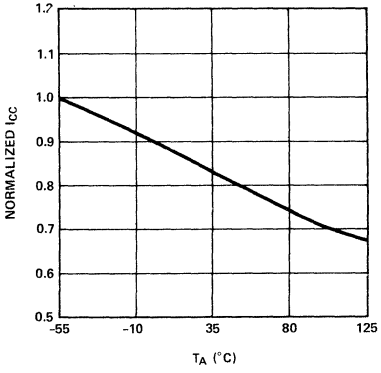
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



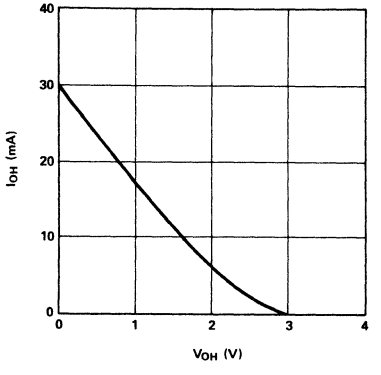
NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



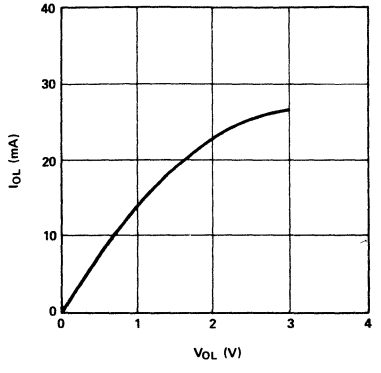
NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



M2115A, M2125A FAMILY
HIGH SPEED 1K X 1 BIT STATIC RAM

	M2115AL, M2125AL	M2115A, M2125A
Max. T_{AA} (ns)	75	55
Max. I_{CC} (mA)	75	125

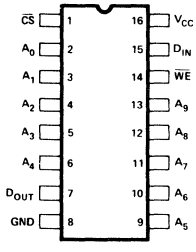
- **HMOS Technology**
- **Low Operating Power Dissipation 413mW (M2115AL, M2125AL)**
- **Fast Access Time Over -55°C to 125°C — 55ns Maximum (M2115A, M2125A)**
- **Single 5V Supply with ±10% Tolerance**
- **TTL Inputs and Output**
- **Uncommitted Collector (M2115A, M2115AL) and Three State (M2125A, M2125AL) Output**
- **Non-Inverting Data Output**
- **Hermetic 16 Pin Dual In-Line Package**

The Intel® M2115A and M2125A families are fully static, random access memories (RAMs) organized as 1024 words by 1 bit, which operate over a -55°C to +125°C ambient temperature range. Both open collector (M2115A) and three-state (M2125A) outputs are available. The M2115A and M2125A use fully DC stable (static) circuitry throughout in both the array and the decoding, and, therefore, require no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

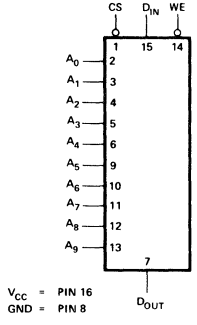
The M2115AL and M2125AL are ideal for high-performance systems where speed and power dissipation are significant design considerations. They have a maximum access time of 75 ns, while power dissipation is only 413 mW maximum. The M2115A and M2125A at 55 ns maximum should be considered for applications in which speed is a primary design objective.

The devices are directly TTL compatible in all respects: inputs, outputs and a single +5V supply. A separate chip select lead allows easy selection of an individual package when outputs are OR-tied.

PIN CONFIGURATION



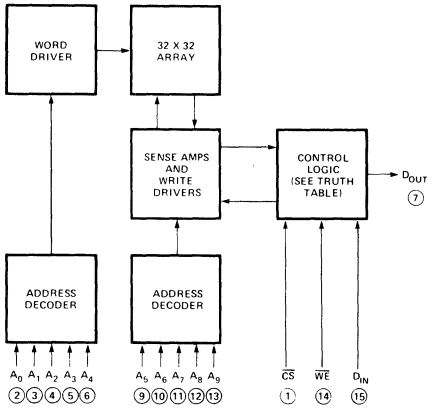
LOGIC SYMBOL



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT 2115A FAMILY	OUTPUT 2125A FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	HIGH Z	HIGH Z	NOT SELECTED
L	L	L	HIGH Z	HIGH Z	WRITE "0"
L	L	H	HIGH Z	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

MILITARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −65°C to +135°C
Storage Temperature . . . . . −65°C to +150°C
All Output or Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −0.5V to +6V
D.C. Output Current . . . . . 20 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1,2]

V_{CC} = 5V ±10%, T_A = −55°C to +125°C

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
V_{OL1}	M2115A, M2115AL Output Low Voltage			0.45	V	I_{OL} = 10 mA
V_{OL2}	M2125A, M2125AL Output Low Voltage			0.45	V	I_{OL} = 5 mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		−0.1	−40	μA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max., V_{IN} = 4.5V
I_{CEX}	M2115A, M2115AL Output Leakage Current		0.1	100	μA	V_{CC} = Max., V_{OUT} = 4.5V
$\|I_{OFF}\|$	M2125A, M2125AL Output Leakage Current (High Z)		0.1	50	μA	V_{CC} = Max., V_{OUT} = 0.5V/2.4V
I_{OS}[3]	M2125A, M2125AL Current Short Circuit to Ground			−100	mA	V_{CC} = Max.
V_{OH}	M2115A, M2115AL Output High Voltage	2.4			V	I_{OH} = −3.2 mA
I_{CC1}	M2115AL, M2125AL Power Supply Current		60	75	mA	All Inputs Grounded, Output Open
I_{CC2}	M2115A, M2125A Power Supply Current		100	125	mA	All Inputs Grounded, Output Open

NOTES:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute.
   Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (@ 400 f_{PM} air flow) = 45°C/W
   θ_{JA} (still air) = 60°C/W
   θ_{JC} = 25°C/W
2. Typical limits are at V_{CC} = 5V, T_A = +25°C and maximum loading.
3. Duration of short circuit current should not exceed 1 second.

MILITARY

M2115AL, M2115A A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±10%, T_A = −55°C to +125°C

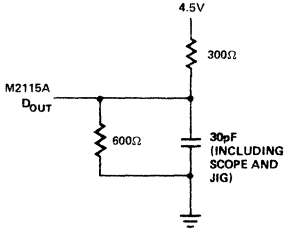
READ CYCLE

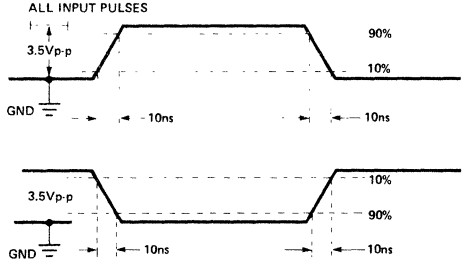
Symbol	Test	M2115AL Limits			M2115A Limits			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{ACS}	Chip Select Time	5		45	5		45	ns
t_{RCS}	Chip Select Recovery Time			50			35	ns
t_{AA}	**Address Access Time**		**40**	**75**		**35**	**55**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			ns

WRITE CYCLE

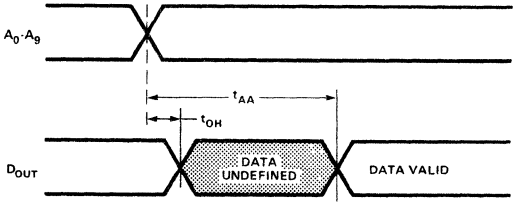
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{WS}	Write Enable Time			45			35	ns
t_{WR}	Write Recovery Time	0		50	0		35	ns
t_W	Write Pulse Width	55	10		40	10		ns
t_{WSD}	Data Setup Time Prior to Write	5	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		ns
t_{WSA}	Address Setup Time	15	0		5	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		ns
t_{WSCS}	Chip Select Setup Time	5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		ns

A.C. TEST CONDITIONS

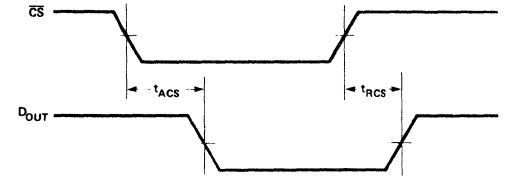




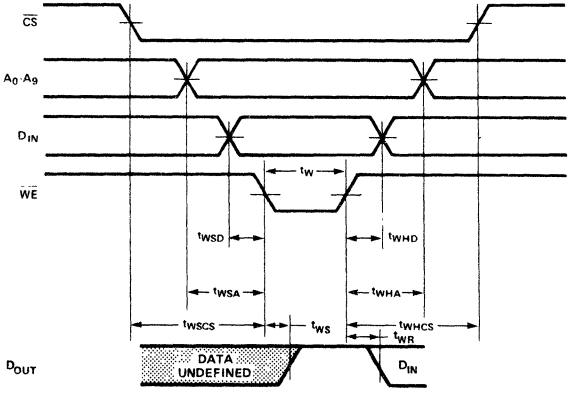
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

MILITARY

M2125AL, M2125A A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±10%, T_A = −55°C to +125°C

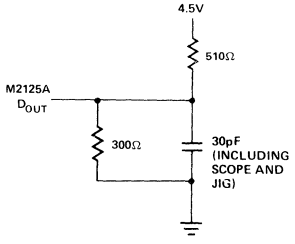
READ CYCLE

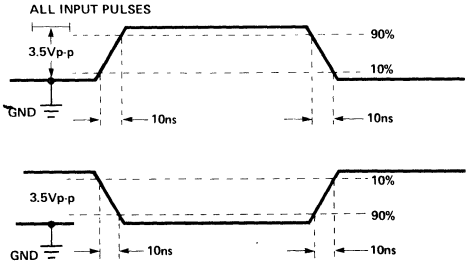
Symbol	Test	M2125AL Limits Min.	Typ.	Max.	M2125A Limits Min.	Typ.	Max.	Units
t_{ACS}	Chip Select Time	5		45	5		45	ns
t_{ZRCS}	Chip Select to HIGH Z			50			35	ns
t_{AA}	**Address Access Time**		**40**	**75**		**25**	**55**	**ns**
t_{OH}	Previous Read Data Valid After Change of Address	10			10			ns

WRITE CYCLE

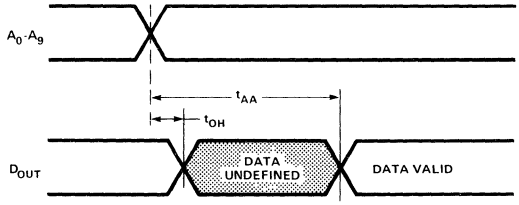
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{ZWS}	Write Enable to HIGH Z			45			35	ns
t_{WR}	Write Recovery Time	0		50	0		35	ns
t_W	Write Pulse Width	55	10		40	10		ns
t_{WSD}	Data Setup Time Prior to Write	5	−5		5	−5		ns
t_{WHD}	Data Hold Time After Write	5	0		5	0		ns
t_{WSA}	Address Setup Time	15	0		5	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		ns
t_{WSCS}	Chip Select Setup Time	5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		ns

A.C. TEST CONDITIONS

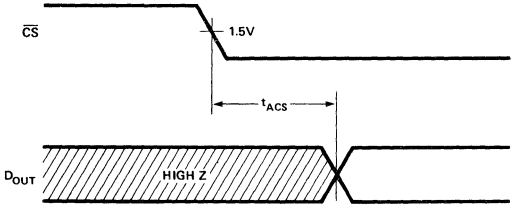




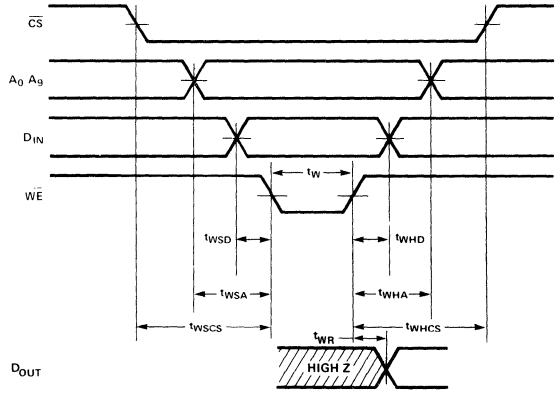
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



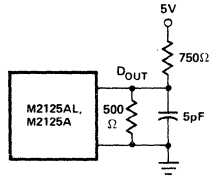
WRITE CYCLE



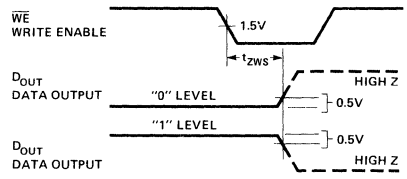
(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

MILITARY

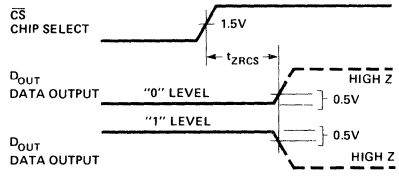
M2125AL, M2125A WRITE ENABLE TO HIGH Z DELAY



LOAD 1



M2125AL, M2125A PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(All t_{ZXX} parameters are measured at a delta of 0.5V from the logic level and using Load 1.)

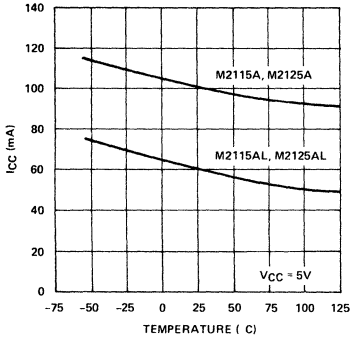
CAPACITANCE* V_{CC} = 5V, f = 1 MHz, T_A = 25°C

Symbol	Test	M2115AL, M2115A Limits		M2125AL, M2125A Limits		Units	Test Conditions
		Typ.	Max.	Typ.	Max.		
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	CS = 5V, All other inputs = 0V, Output Open

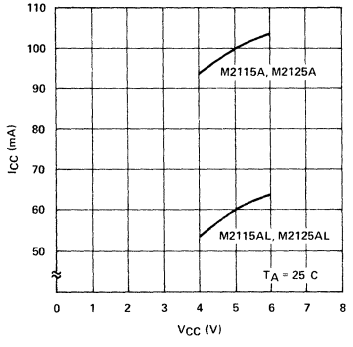
*This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

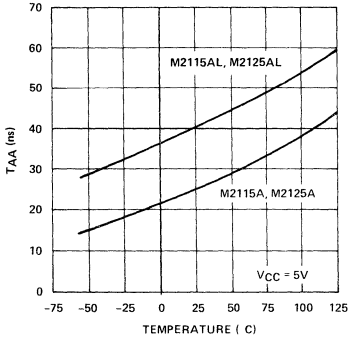
I_{CC} vs. TEMPERATURE



I_{CC} vs. V_{CC}



ACCESS TIME vs. TEMPERATURE



MILITARY

M2147
4096 X 1 BIT STATIC RAM

	M2147
Max. Access Time (ns)	85
Max. Active Current (mA)	180
Max. Standby Current (mA)	30

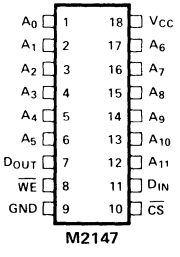
- **HMOS Technology**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **±10% Power Supply Tolerance**
- **Automatic Power-Down**
- **High Density 18-Pin Package**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Separate Data Input and Output**
- **Three-State Output**
- **Full Military Temperature Range**

The Intel® M2147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the military user this means low standby power dissipation without the need for clocks,address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the M2147— the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are de-selected.

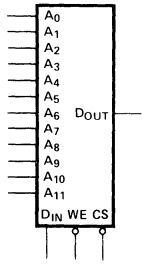
The M2147 is placed in an 18-pin package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

PIN CONFIGURATION

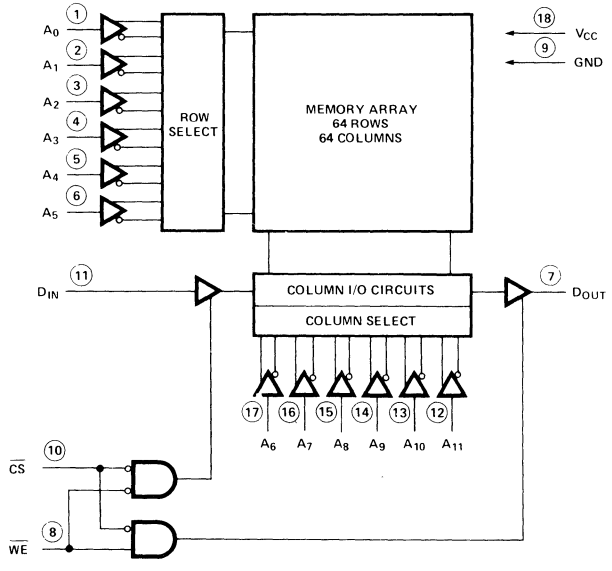


M2147

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

MILITARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -65°C to +135°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin With
Respect to Ground ..... -1.5V to +7V
Power Dissipation 1.2W
D.C. Output Current ..... 20 mA

COMMENT. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS [1]

T_A = -55°C to +125°C, V_{CC} = +5V±10%, unless otherwise specified

Symbol	Parameter	M2147 Min.	M2147 Typ.[2]	M2147 Max.	Unit	Test Conditionsp
I_{LI}	Input Load Current (All Input Pins)		0.01	10	µA	V_{CC} = MAX., V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	50	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max., V_{OUT} = GND to 4.5V
I_{CC}	Operating Current		120	160	mA	T_A=25°C; V_{CC}=Max., $\overline{CS}$=V_{IL} Outputs Open
				180	mA	T_A=-55°C; V_{CC}=Max., $\overline{CS}$=V_{IL} Outputs Open
I_{SB}	Standby Current		18	30	mA	V_{CC}=Min. to Max., $\overline{CS}$=V_{IH}
I_{PO}[3]	Peak Power On Current		35	70	mA	V_{CC}=GND to V_{CC} Min., $\overline{CS}$=Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	-1.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 5mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -1.0mA
I_{OS}[4]	Output Short Circuit Current	-150		150	mA	V_{OUT} = GND to V_{CC}

Notes:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and specified loading.
3. I_{CC} exceeds I_{SB} maximum during power on, as shown in Graph 7. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.
4. Duration not to exceed 30 seconds.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.5 Volts
Input Rise and Fall Times	10 nsec
Input and Output Timing Reference Levels	1.5 Volts
Output Load	See Figure 1

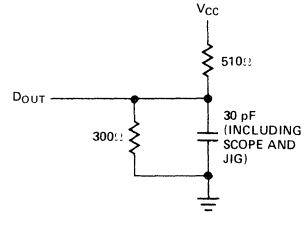


Figure 1. Output Load

CAPACITANCE

T_A = 25°C, f = 1.0MHz [5]

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0V

Note 5. This parameter is sampled and not 100% tested.

A.C. CHARACTERISTICS

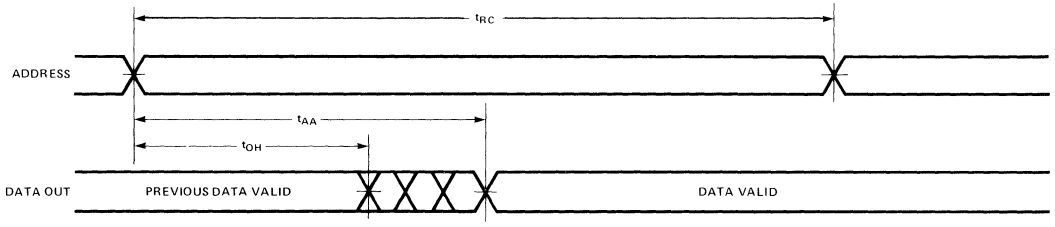
T_A = -55°C to +125°C, V_{CC} = +5V±10%, unless otherwise specified

READ CYCLE

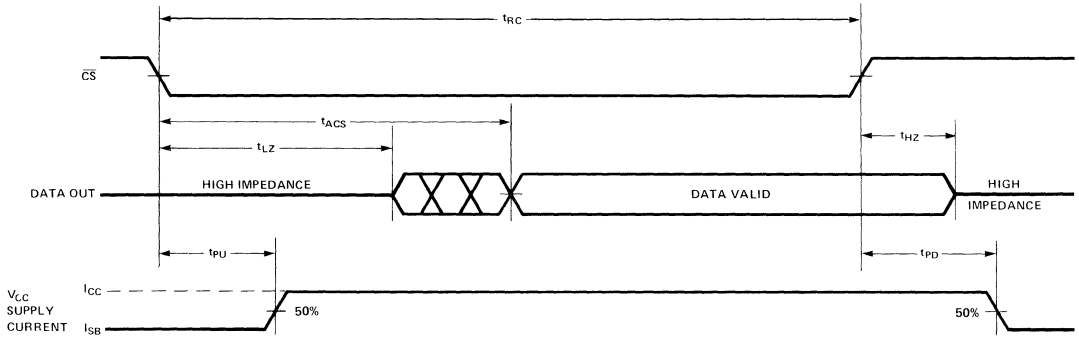
Symbol	Parameter	M2147 Min.	M2147 Max.	Unit	Test Conditions
t_{RC}	Read Cycle Time	85		ns	
t_{AA}	Address Access Time		85	ns	
t_{ACS1}	Chip Select Access Time		85	ns	Note 1
t_{ACS2}	Chip Select Access Time		100	ns	Note 2
t_{OH}	Output Hold from Address Change	5		ns	
t_{LZ}	Chip Selection to Output in Low Z	10		ns	
t_{HZ}	Chip Deselection to Output in High Z	0	40	ns	
t_{PU}	Chip Selection to Power Up Time	0		ns	
t_{PD}	Chip Deselection to Power Down Time		30	ns	

WAVEFORMS

READ CYCLE NO. 1 [3,4]



READ CYCLE NO. 2 [3,5]



Notes 1. Chip deselected for greater than 55ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
3. $\overline{WE}$ is high for Read Cycles.
4. Device is continuously selected, $\overline{CS}$ = V_{IL}.
5. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

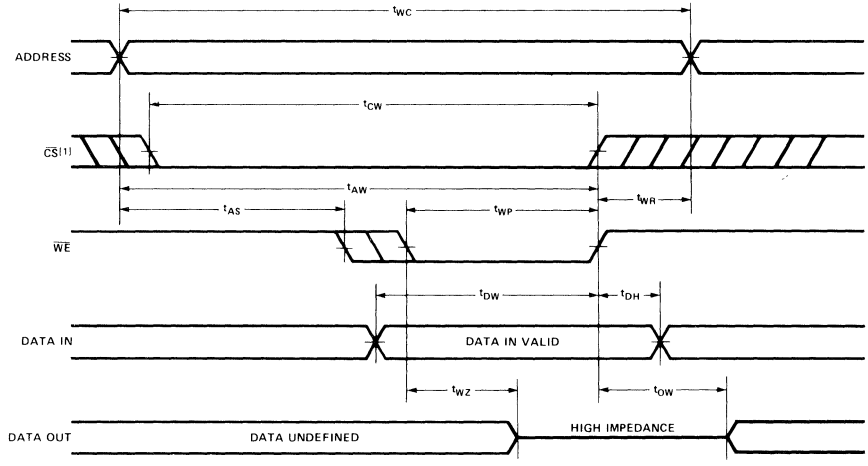
A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

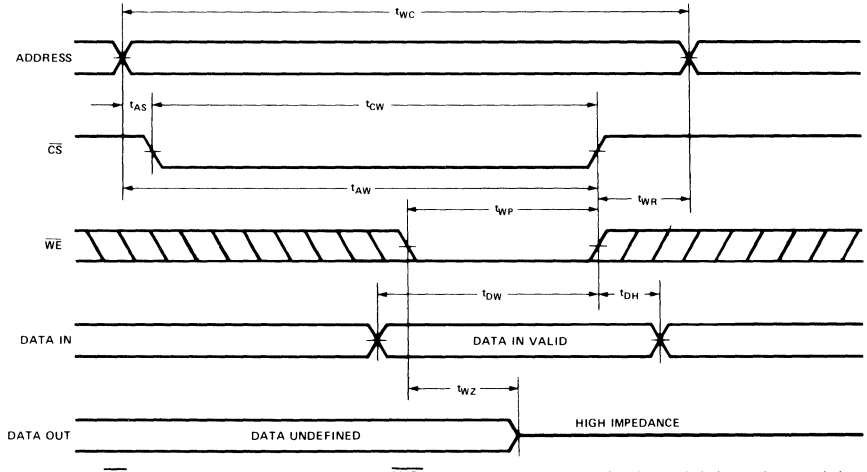
Symbol	Parameter	M2147 Min.	M2147 Max.	Unit	Test Conditions
t_{WC}	Write Cycle Time	85		ns	
t_{CW}	Chip Selection to End of Write	70		ns	
t_{AW}	Address Valid to End of Write	70		ns	
t_{AS}	Address Setup Time	0		ns	
t_{WP}	Write Pulse Width	55		ns	
t_{WR}	Write Recovery Time	15		ns	
t_{DW}	Data Valid to End of Write	35		ns	
t_{DH}	Data Hold Time	10		ns	
t_{WZ}	Write Enabled to Output in High Z	0	50	ns	
t_{OW}	Output Active from End of Write	0		ns	

WAVEFORMS

WRITE CYCLE #1 ($\overline{WE}$ CONTROLLED)



WRITE CYCLE #2 ($\overline{CS}$ CONTROLLED)

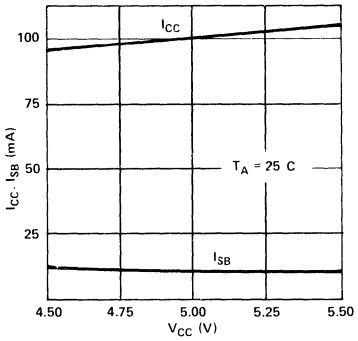


Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

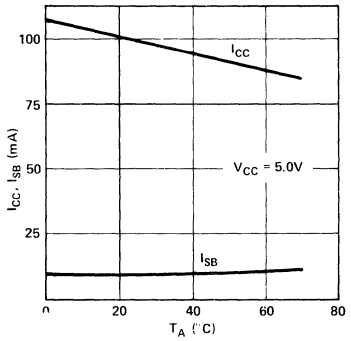
MILITARY

TYPICAL D.C. AND A.C. CHARACTERISTICS

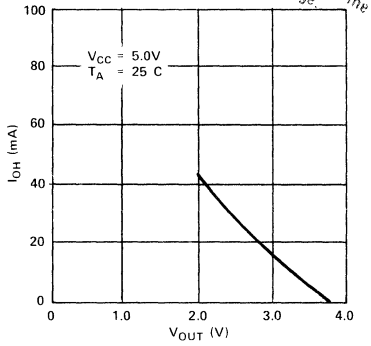
GRAPH 1
SUPPLY CURRENT VS.
SUPPLY VOLTAGE



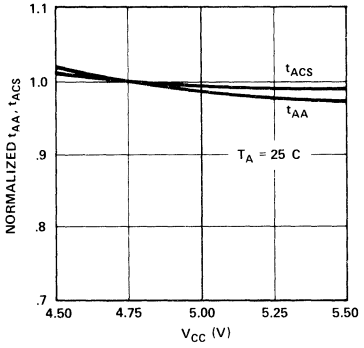
GRAPH 2
SUPPLY CURRENT VS.
AMBIENT TEMPERATURE



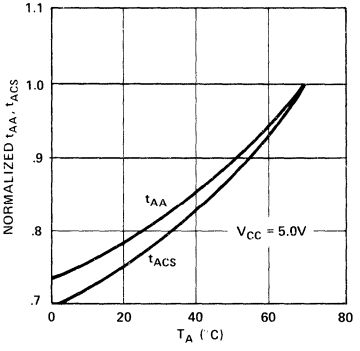
GRAPH 3
OUTPUT SOURCE CURRENT VS.
OUTPUT VOLTAGE



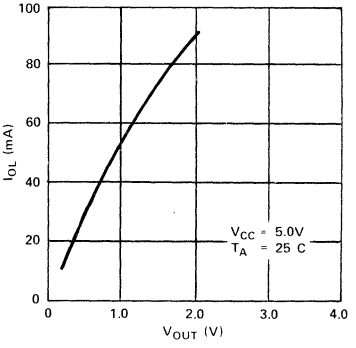
GRAPH 4
NORMALIZED ACCESS TIME
VS. SUPPLY VOLTAGE



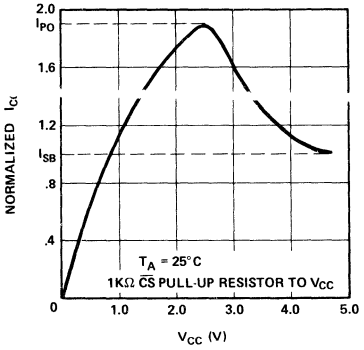
GRAPH 5
NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE



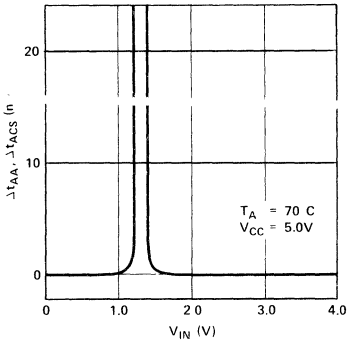
GRAPH 6
OUTPUT SINK CURRENT VS.
OUTPUT VOLTAGE



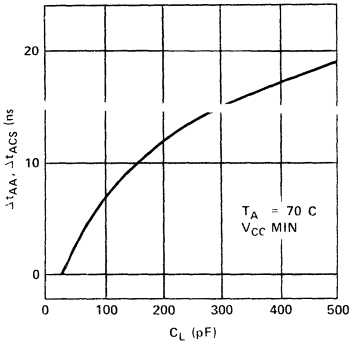
GRAPH 7
TYPICAL POWER-ON CURRENT
VS. POWER SUPPLY VOLTAGE



GRAPH 8
ACCESS TIME CHANGE VS.
INPUT VOLTAGE



GRAPH 9
ACCESS TIME CHANGE VS.
OUTPUT LOADING



MILITARY

DEVICE DESCRIPTION

The M2147 is produced with HMOS, a new high-performance MOS technology which incorporates on-chip substrate bias generation combined with device scaling to achieve high-performance. The speed-power product of this process has been measured at 1pj, approximately four times better than previous MOS processes.

This process, combined with new design ideas, gives the M2147 its unique features. High speed, low power and ease-of-use have been obtained in a single part. The low-power feature is controlled with the Chip Select input, which is not a clock and does not have to be cycled. Multiple read or write operations are possible during a single select period. Access times are equal to cycle times, resulting in a data rate of 11.8 MHz. This is considerably higher performance than for clocked static designs.

Whenever the M2147 is deselected, it automatically reduces its power requirements to a fraction of the active power, as shown in Figure 1. This is achieved by switching off the power to unnecessary portions of the internal peripheral circuitry. This feature adds up to significant system power savings. The average power per device declines as system size grows because a continually higher portion of the memory is deselected. Device power dissipation asymptotically approaches the standby power level, as shown in Figure 2.

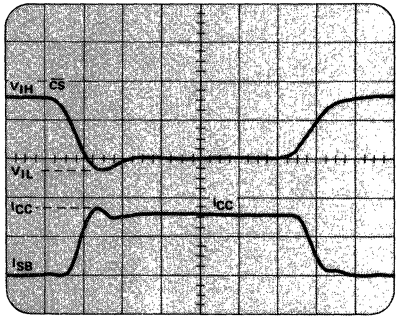


FIGURE 1. i_{CC} WAVEFORM.

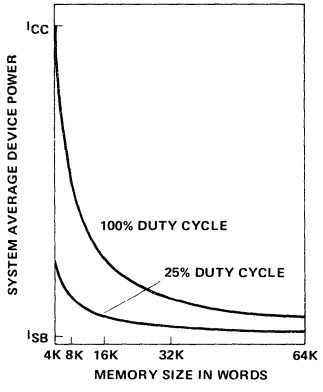


FIGURE 2. AVERAGE DEVICE DISSIPATION VS. MEMORY SIZE.

There is no functional constraint on the amount of time the M2147 is deselected. However, there is a relationship between deselect time and Chip Select access time. With no compensation, the automatic power switch would cause an increase in Chip Select access time, since some time is lost in repowering the device upon selection. A feature of the M2147 design is its ability to compensate for this loss. The amount of compensation is a function of deselect time, as shown in Figure 3. For short deselect times, Chip Select access time becomes slower than address access time, since full compensation typically requires 40ns. For longer deselect times, Chip Select access time actually becomes faster than address access time because the compensation more than offsets the time lost in powering up. The spec accounts for this characteristic by specifying two Chip Select access times, t_{ACS1} and t_{ACS2}.

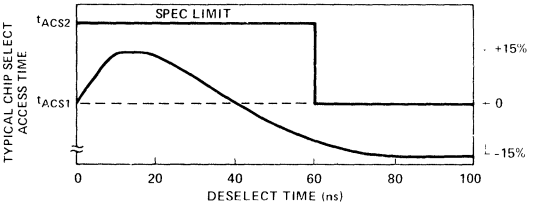


FIGURE 3. t_{ACS} VS. DESELECT TIME.

The power switching characteristic of the M2147 requires more careful decoupling than would be required of a constant power device. It is recommended that a 0.1μF to 0.3μF ceramic capacitor be used on every other device, with a 22μF to 47μF bulk electrolytic decoupler every 16 devices. The actual values to be used will depend on board layout, trace widths and duty cycle. Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two-layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 4.

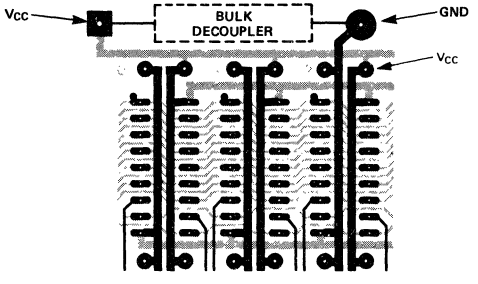


FIGURE 4. PC LAYOUT.

Terminations are recommended on input signal lines to the M2147 devices. In high speed systems, fast drivers can cause significant reflections when driving the high impedance inputs of the M2147. Terminations may be required to match the impedance of the line to the driver. The type of termination used depends on designer preference and may be parallel resistive or resistive-capacitive. The latter reduces terminator power dissipation.

MILITARY

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EXTENDED TEMP. RANGE

M2708
8K (1K x 8) UV ERASABLE PROM

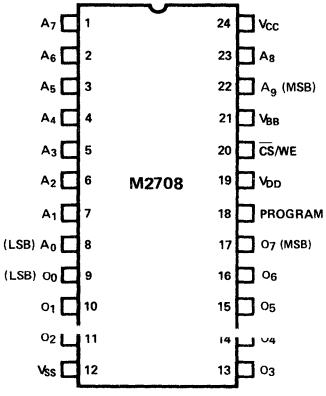
- **Extended Temperature Range: −55°C to 100°C**
- **Fast Programming: Typ. 100 sec. For All 8K Bits**
- **Low Power During Programming**
- **Access Time: 450 ns Max.**
- **Standard Power Supplies: +12V, +5V, −5V**
- **Static: No Clocks Required**
- **Inputs and Outputs TTL Compatible During Both Read and Program Modes**
- **Three-State Output: OR-Tie Capability**
- **Hermetic Package: 24 Pin DIP**

The Intel M2708 is a high speed 8192 bit erasable and electrically reprogrammable ROM (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

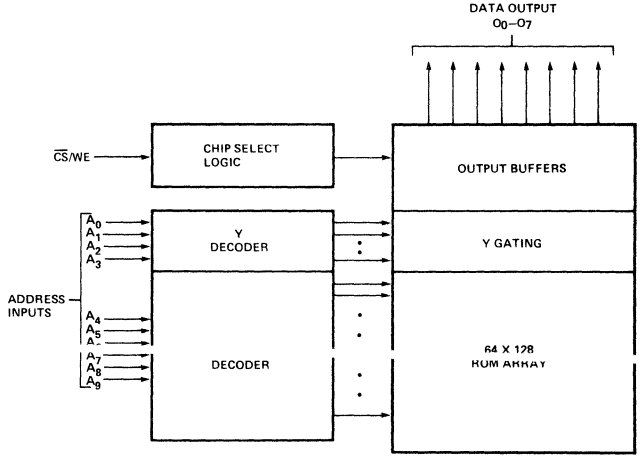
The M2708 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices.

The M2708 is fabricated with the time proven N-channel silicon gate technology.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1-8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED V_{IHP}	+12	V_{IHW}	-5	+5

MILITARY

Absolute Maximum Ratings*

Temperature Under Bias	-65°C to 110°C
Storage Temperature	-65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to -0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to -0.3V
All Input or Output Voltages With Respect to V_{BB} During Read	+15V to -0.3V
$\overline{CS}$/WE Input With Respect to V_{BB} During Programming	+20V to -0.3V
Program Input With Respect to V_{BB}	+35V to -0 3V
Power Dissipation	1.8W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

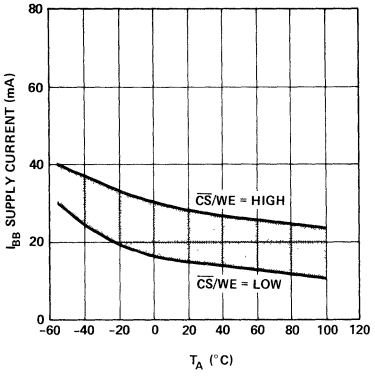
T_A = -55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = +12V ±10%, V_{BB}[1] = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	V_{IN} = 5.5 V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10	μA	V_{OUT} = 5.5 V, $\overline{CS}$/WE = 5V
I_{DD}[3]	V_{DD} Supply Current		50	80	mA	Worst Case Supply Currents:
I_{CC}[3]	V_{CC} Supply Current		6	15	mA	All Inputs High
I_{BB}[3]	V_{BB} Supply Current		30	60	mA	$\overline{CS}$/WE = 5V; T_A = -55°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			750	mW	T_A = 100°C

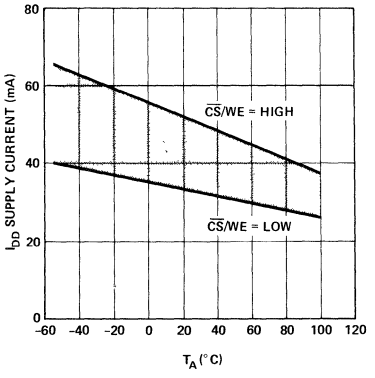
NOTES:
1. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. The total power dissipation of the 2704/2708 is specified at 750 mW. It is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

Typical D.C. Characteristics

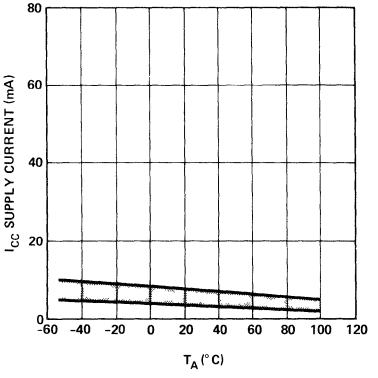
I_{BB} CURRENT VS. TEMPERATURE



I_{DD} CURRENT VS. TEMPERATURE



I_{CC} CURRENT VS. TEMPERATURE



MILITARY

A.C. Characteristics

T_A = -55°C to 100°C, V_{CC} = +5V ±10%, V_{DD} = +12V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
t_{CO}	Chip Select to Output Delay		60	120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance[1] T_A = 25°C, f = 1MHz

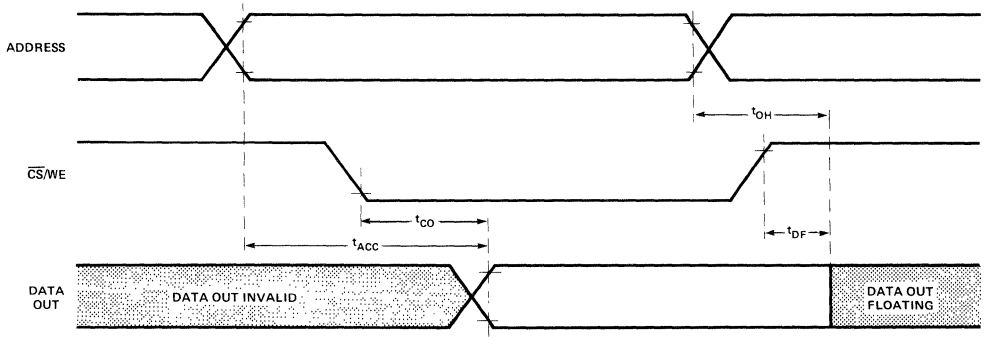
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN}=0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT}=0V

Note 1. This parameter is sampled and not 100% tested.

A.C. TEST CONDITIONS:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs
Input Pulse Levels: 0.65V to 3.0V

Waveforms



ERASURE CHARACTERISTICS

The erasure characteristics of the M2708 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical M2708 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the M2708 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the M2708 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog PROM/ROM Programming Instructions section) for the M2708 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 1200 μW/cm^2 power rating. The M2708 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

MILITARY

I. ERASING PROCEDURE

The M2708 is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 10W-sec/cm^2. An example of an ultraviolet source which can erase the M2708 in 30 minutes is the Model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the PROM should be placed about one inch away from the lamp tubes.

Two manufacturers of the S52 are Ultra-Violet Products, Inc. (San Gabriel, Calif.) and Product Specialities, Inc. (Issaquah, Washington).

To prevent damage to the device, it is recommended that no more ultraviolet light exposure be used than that necessary to erase the M2708.

II. PROGRAMMING INSTRUCTIONS

Initially, and after each erasure, all bits of the M2708 are in the "1" state (Output High). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the $\overline{CS}$/WE input (Pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8-bits in parallel, to the data output lines (O_1-O_8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up one program pulse per address is applied to the program input (Pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to N x $t_{PW} \geqslant$100 ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops through all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Examples (Using N x $t_{PW} \geqslant$ 100 ms)

Example 1: All 8096 bits are to be programmed with a 0.5 ms program pulse width.

The minimum number of program loops is 200. One program loop consists of words 0 to 1023.

Example 2: Words 0 to 100 and 500 to 600 are to be programmed. All other bits are "don't care". The program pulse width is 0.75 ms.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's.

Example 3: Same requirements as example 2 but the PROM is now to be *updated* to include data for words 750 to 770.

The minimum number of program loops is 133. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1's. Addresses 0 to 100 and 500 to 600 must be re-programmed with their original data pattern.

MILITARY

PROGRAM CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

D.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Address and $\overline{CS}$/WE Input Sink Current			10	μA	V_{IN} = 5.25V
I_{IPL}	Program Pulse Source Current			3	mA	
I_{IPH}	Program Pulse Sink Current			20	mA	
I_{DD}	V_{DD} Supply Current		45	55	mA	Worst Case Supply Currents:
I_{CC}	V_{CC} Supply Current		5	8	mA	All Inputs High
I_{BB}	V_{BB} Supply Current		30	35	mA	$\overline{CS}$/WE = 5V; T_A = 25°C
V_{IL}	Input Low Level (except Program)	V_{SS}		0.65	V	
V_{IH}	Input High Level for all Addresses and Data	3.0		V_{CC}+1	V	
V_{IHW}	$\overline{CS}$/WE Input High Level	11.4		12.6	V	Referenced to V_{SS}
V_{IHP}	Program Pulse High Level	25		27	V	Referenced to V_{SS}
V_{ILP}	Program Pulse Low Level	V_{SS}		1	V	V_{IHP} - V_{ILP} = 25V min.

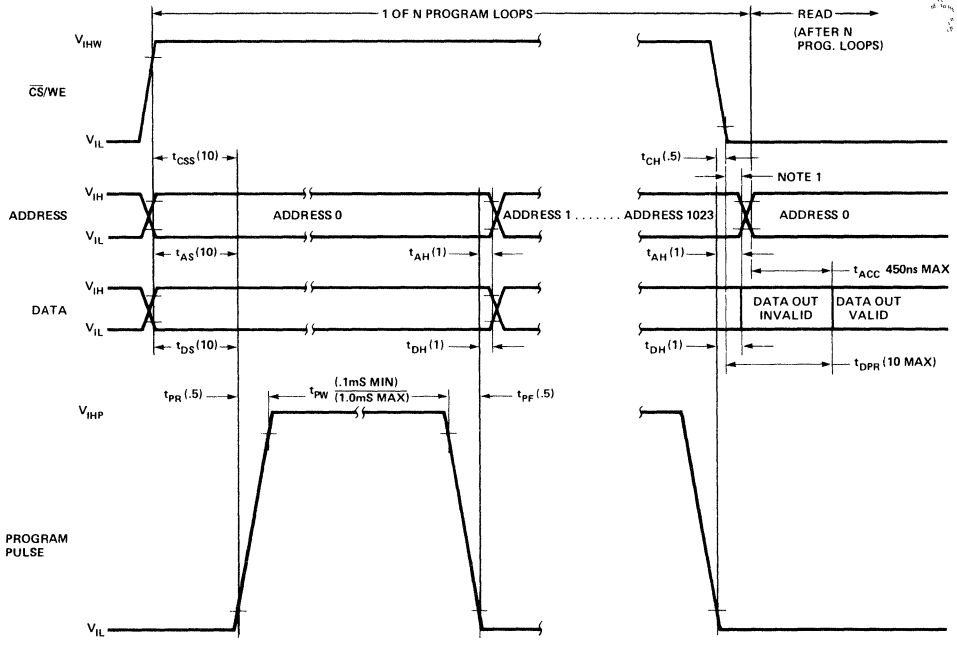
A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	$\overline{CS}$/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	$\overline{CS}$/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	.5		2.0	μs

NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

MILITARY

Programming Waveforms

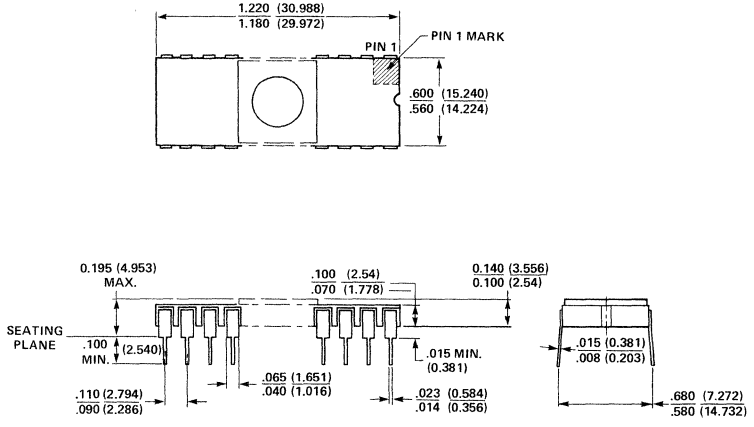


NOTE 1. THE $\overline{CS}/WE$ TRANSITION MUST OCCUR AFTER THE PROGRAM PULSE TRANSITION AND BEFORE THE ADDRESS TRANSITION.

NOTE 2. NUMBERS IN ( ) INDICATE MINIMUM TIMING IN μS UNLESS OTHERWISE SPECIFIED.

Packaging Information

24 LEAD HERMETIC DUAL IN-LINE PACKAGE



MILITARY

M2716
16K (2K x 8) UV ERASABLE PROM

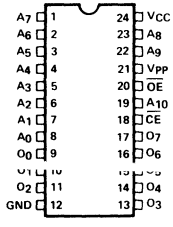
- **Extended Temperature Range**
  – 55°C to + 100°C Operation
- **Single + 5V Power Supply**
- **Single Programming Requirements**
  — Single Location Programming
  — Programs with One 50 ms Pulse
- **Static Standby Mode**
- **Low Power Dissipation of 165 mW max. standby power**
- **Fast Access Time; 450 ns max.**
- **Inputs and Outputs TTL Compatible during Read and Program**

The Intel® M2716 is a 16,384-bit ultraviolet erasable and electrically programmable read only memory (EPROM) specified over the – 55°C to + 100°C temperature range. The M2716 operates from a single + 5V power supply, has a static power-down mode, and features fast, single-address location programming. It makes designing with EPROMs faster, easier and more economical.

The M2716 has a static standby mode which reduces the power dissipation without increasing access time. The active power dissipation is reduced by over 60% in the standby power mode.

The M2716 has the simplest and fastest method devised yet for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time — either individually, sequentially or at random, with the M2716's single-address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



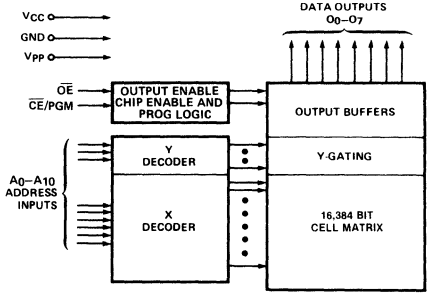
MODE SELECTION

MODE \ PINS	CE/PGM (18)	OE (20)	VPP (21)	VCC (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
[illegible]	[illegible]	[illegible]	[illegible]	+5	High Z

PIN NAMES

A_0–A_{10}	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

BLOCK DIAGRAM



MILITARY

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section

Absolute Maximum Ratings*

Temperature Under Bias ..... −65°C to +110°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with Respect to Ground ..... +6V to −0.3V
V_{PP} Supply Voltage with Respect to Ground During Program ..... +26.5V to −0.3V

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

$T_A = -55°C$ to $+100°C$, V_{CC}[1,2] $= +5V \pm 10\%$, V_{PP}[2] $= V_{CC}$

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ[3]	Max.		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.50V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.50V$
I_{PP1}[2]	V_{PP} Current			5	mA	$V_{PP} = 5.50V$
I_{CC1}[2]	V_{CC} Current (Standby)		10	30	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC2}[2]	V_{CC} Current (Active)		57	115	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

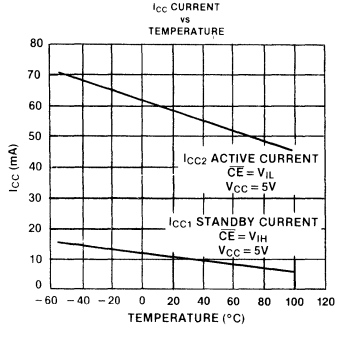
NOTES: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

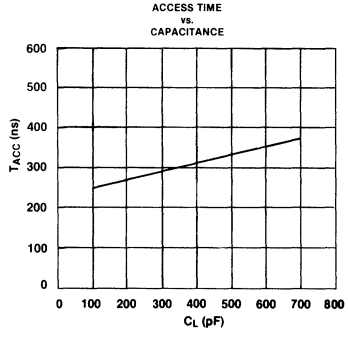
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.

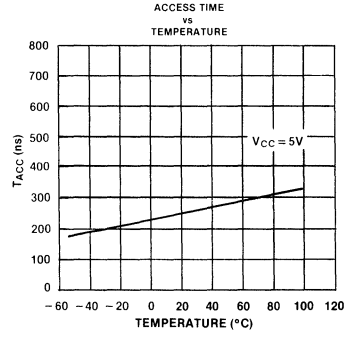
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.

4. This parameter is only sampled and is not 100% tested.

Typical Characteristics







MILITARY

A.C. Characteristics

$T_A = -55°C$ to $+100°C$, V_{CC}[1,2] $= +5V \pm 10\%$, V_{PP}[2] $= V_{CC}$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{ACC}	Address to Output Delay			450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay			450	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			150	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		130	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

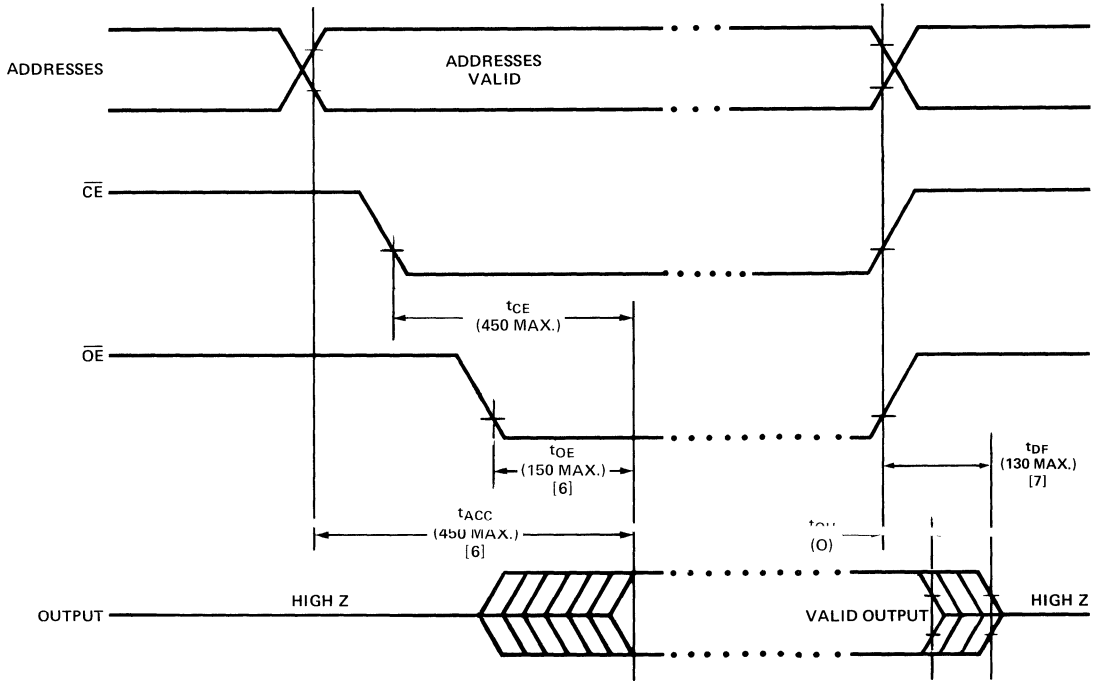
Capacitance[4] $T_A = 25°C$, $f = 1$ MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

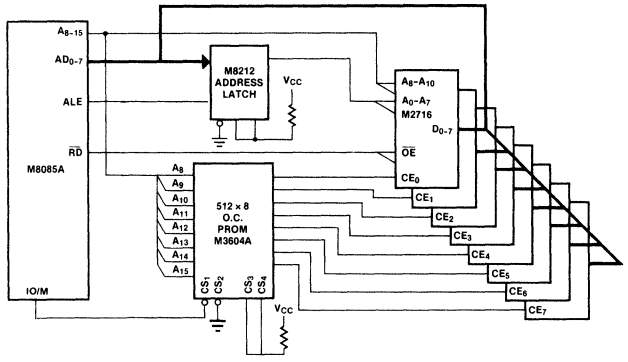
Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms[5]



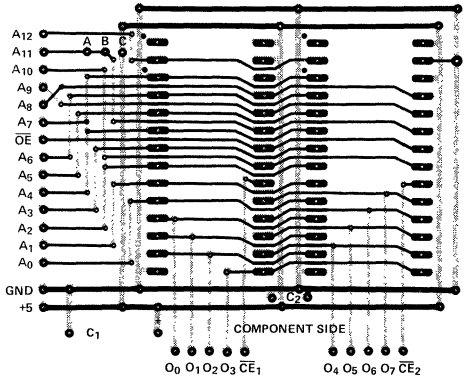
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. All times shown in parentheses are minimum and are nsec unless otherwise specified.
6. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
7. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

TYPICAL 16K EPROM SYSTEM



- **This scheme accomplished by using $\overline{CE}$ as the primary decode. $\overline{OE}$ is now controlled by previously unused signal. RD now controls data on and off the bus by way of $\overline{OE}$.**
- **The use of a PROM as a decoder allows for:**
  a) Compatibility with upward (and downward) memory expansion.
  b) Easy assignment of ROM memory modules, compatible with PL/M modular software concepts.

8K, 16K, 32K, 64K 5V EPROM/ROM FAMILY PRINTED CIRCUIT BOARD LAYOUT



ERASURE CHARACTERISTICS

The erasure characteristics of the M2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical device in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the M2716 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog PROM/ROM Programming Instruction Section) for the M2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/CM^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μ W/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the M2716 are listed in Table 1. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a + 5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

MODE SELECTION

PINS / MODE	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The M2716 has two control functions, both of which must be logically satisfied in order to obtain dat at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 150 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M2716 has a standby mode which reduces the active power dissipation by 75%, from 633 mW to 165 mW. The M2716 is placed in the standby mode by applying a TTL high special to the CE input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

OUTPUT OR-TIEING

Because M2716's are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connections. The two line control function allows for

a) the lowest possible memory power dissipation, and,
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING

Initially, and after each erasure, all bits of the M2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" wil be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can progam any location at any time — either individually, sequentially, or at random. The program pulse has a maximum wit)dth of 55 msec. The M2716 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple M2716's in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2716's may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$ input programs the paralleled M2716's.

PROGRAM INHIBIT

Programming of multiple M2716's in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like units (including $\overline{OE}$) of the parallel M2716's may be common. A TTL level program pulse applied to a M2716's $\overline{CE}$ input with V_{PP} at 25V will program that M2716. A low level $\overline{CE}$ input inhibits the other M2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

DEVICE RELIABILITY

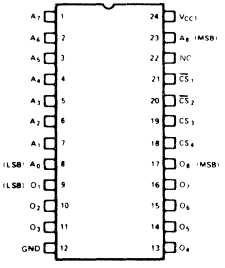
The M2716 is built on a proven 2 layer polysilicon NMOS technology. Extensive testing and monitoring has allowed us to achieve failure rates equal to other memory devices. For detailed failure rate predictions and reliability data, request Intel 2716 Reliability Report.

M3604A, M3624A
4K (512 x 8) HIGH-SPEED PROM

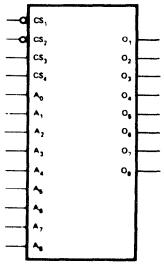
- **Military Temperature Range: -55° C to +125° C**
- **Fast Access Time — 90nsec Maximum**
- **Open Collector (M3604A) or Three-State (M3624A) Outputs**
- **Four Chip Select Inputs for Easy Memory Expansion**
- **Polycrystalline Silicon Fuse for Higher Reliability**
- **Standard Packaging — 24 Pin Hermetic Dual In-Line Lead Configuration**

The M3604A and M3624A are military temperature range PROMs organized as 512 words by 8 bits. They are manufactured with all outputs high and logic output low levels can be electrically programmed in selected bit locations. The M3604A and M3624A, except for programming, have the same electrical specifications and are direct replacements to their predecessors, the M3604 and M3624.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-65°C to +135 C
Storage Temperature	-65°C to +160°C
Output or Supply Voltages	-0.5V to 7 Volts
All Input Voltages	-1.6V to 5.6V
Output Currents	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS V_{CC} = +5.0V ±10%, T_A = −55°C to +125°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}= Max, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}= Max, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC}= Max, V_A= Max
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC}= Max, V_S= Max
V_{CA}	Address Input Clamp Voltage		-0.9	−1.5	V	V_{CC}= Min, I_A= −10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	−1.5	V	V_{CC}= Min, I_S= −10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}= Min, I_{OL}= 10mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC}= Max, V_{CE}= Max
I_{CC1}	Power Supply Current (M3604A)			190	mA	V_{CC1}= Max, V_{A0}→V_{A8}=0V, $\overline{CS}_1$=$\overline{CS}_2$=0V, CS_3=CS_4= 5.5V
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC}= 5.0V, T_A=25°C
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}= 5.0V, T_A=25°C

M3624A ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	μA	V_O= Max or 0.45V, V_{CC}= Max, $\overline{CS}_1$=$\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	−20	-25	−80	mA	V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 5V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

MILITARY

A.C. CHARACTERISTICS V_{CC} = +5.0V ±10%, T_A = −55°C to +125°C

SYMBOL	PARAMETER	LIMITS TYP.[1]	LIMITS MAX.	UNIT	CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	90	ns	$\overline{CS}_1 = \overline{CS}_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to Select the PROM
t_{S++}	Chip Select to Output Delay	20	45	ns	
t_{S--}	Chip Select to Output Delay	20	45	ns	

CAPACITANCE [2] T_A = 25°C, f = 1 MHz

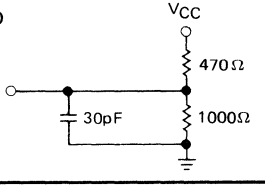
SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTES: 1. Typical values are at 25°C and nominal voltage.
2. This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

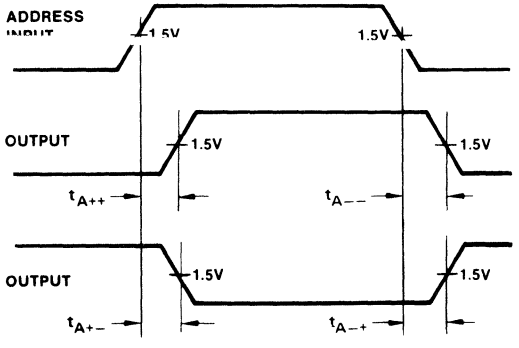
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test - 2.5 MHz

10 mA TEST LOAD

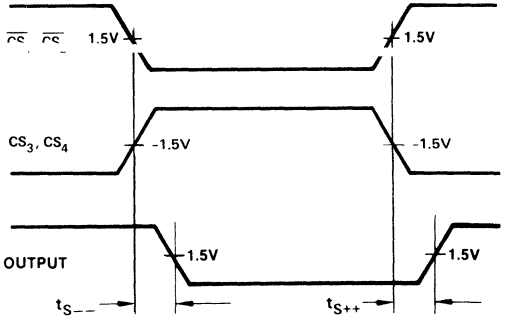


WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



MILITARY

M3625A
4K (1K x 4) PROM

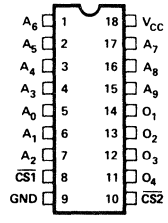
- ± 10% Power Supply Tolerance
- Fast Access Time: 60 ns Maximum
- Lower Power Dissipation: 0.14 mW/Bit Typically
- Simple Memory Expansion Two Chip Select Inputs
- Three-State Outputs
- Polycrystalline Silicon Fuse for Higher Reliability
- Hermetic 18-Pin DIP

The Intel® M3625A is a high density, 4096-bit bipolar PROM organized as 1024 words by 4 bits. The 1024 by 4 organization gives ideal word or bit modularity for memory array expansion. The M3625A is fully specified over the −55 °C to 125 °C temperature range with ± 10% power supply variation.

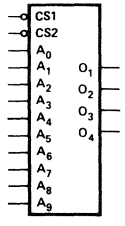
The M3625A is packaged in an 18-pin dual-in-line hermetic package with 300 milli-inch centers. Thus, twice the bit density can be achieved in the same memory board areas as 512 by 8-bit PROMs in 24-pin packages.

The highly reliable polycrystalline silicon fuse technology is used in the manufacturing of the M3625A. All outputs are initially a logical high and logic low levels can be electrically programmed in selected bit locations.

PIN CONFIGURATION



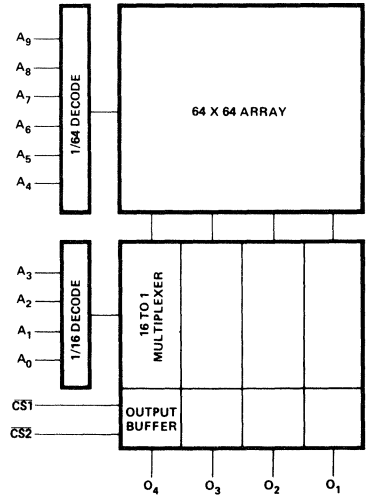
LOGIC SYMBOL



PIN NAMES

A_0-A_9	ADDRESS INPUTS
$\overline{CS}$	CHIP SELECT INPUT
O_1-O_4	OUTPUTS

BLOCK DIAGRAM



MILITARY

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions.

Absolute Maximum Ratings*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +160°C
Output or Supply Voltages ..... −0.5V to 7V
All Input Voltages ..... −1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics: All limits apply for $V_{CC} = +5.0V \pm 10\%$, $T_A = -55°C$ to $+125°C$, unless otherwise specified.

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.5V$, $V_A = 0.45V$
I_{FS}	Chip Select Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.5V$, $V_S = 0.45V$
I_{RA}	Address Input Leakage Current			40	μA	$V_{CC} = 5.5V$, $V_A = 5.5V$
I_{RS}	Chip Select Input Leakage Current			40	μA	$V_{CC} = 5.5V$, $V_S = 5.5V$
$\|I_O\|$	Output Leakage for High Impedance Stage			40	μA	$V_O = 5.5V$ or $0.45V$, $V_{CC} = 5.5V$, $\overline{CS_1} = \overline{CS_2} = 2.4V$
I_{SC}[2]	Output Short Circuit Current	−20	−35	−80	mA	$V_O = 0V$
V_{CA}	Address Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.5V$, $I_A = -10mA$
V_{CS}	Chip Select Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.5V$, $I_S = -10mA$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -2.4mA$, $V_{CC} = 4.5V$
V_{OL}	Output Low Voltage		0.3	0.45	V	$V_{CC} = 4.5V$, $I_{OL} = 10mA$
I_{CC}	Power Supply Current		110	140	mA	$V_{CC} = 5.5V$, $V_{A0} \rightarrow V_{A9} = 0V$, $\overline{CS_1} = \overline{CS_2} = V_{IH}$
V_{IL}	Input "Low" Voltage			0.85	V	$T_A = 25°C$
V_{IH}	Input "High" Voltage	2.0			V	$T_A = 25°C$

NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. Unmeasured outputs are open during this test.

MILITARY

A.C. Characteristics: $V_{CC} = +5.0V \pm 10\%$, $T_A = -55°C$ to $+125°C$.

Symbol	Parameter	Max. Limits	Unit	Conditions
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	ns	$\overline{CS_1} = \overline{CS_2} = V_{IL}$ to select the PROM.
t_{S++}	Chip Select to Output Delay	35	ns	
t_{S--}	Chip Select to Output Delay	35	ns	

Capacitance[1] $T_A = 25°C$, f = 1 MHz.

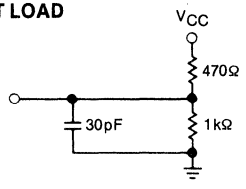
Symbol	Parameter	Limits Typ.	Limits Max.	Unit	Test Conditions	
C_{INA}	Address Input Capacitance	3	8	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{INS}	Chip Select Input Capacitance	4	8	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	5	10	pF	$V_{CC} = 5V$	$V_{OUT} = 2.5V$

NOTES:
1. This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

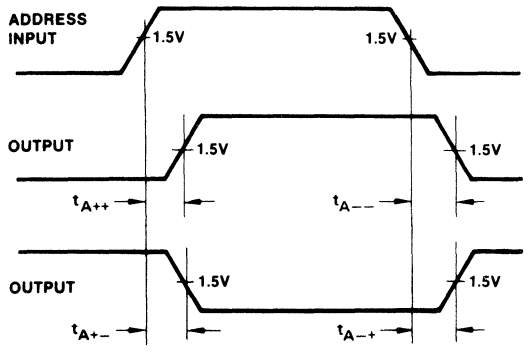
Conditions of Test:
Input pulse amplitudes — 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1V and 2V
Speed measurements are made at 1.5V levels
Output loading — 10mA and 30pF
Frequency of test — 2.5MHz

10mA TEST LOAD

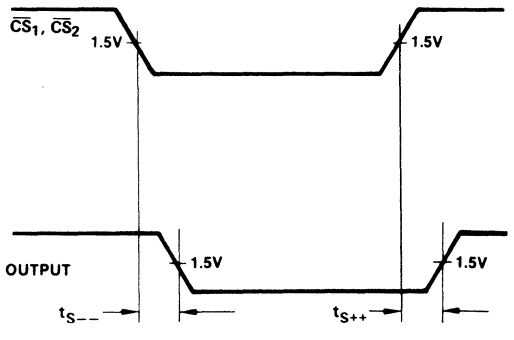


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



MILITARY

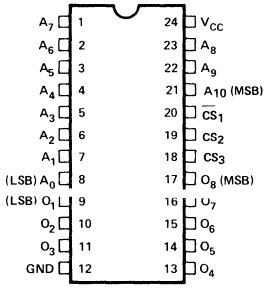
M3636
16K (2K x 8) BIPOLAR PROM

- **−55°C to +125°C Operation**
- **Fast Access Time: 80 ns Maximum**
- **Low Power Dissipation: 0.05 mW/Bit Typically**
- **Three Chips Select Input for Easy Memory Expansion**
- **Pin Compatible to 8K PROMs**
- **Three-State Outputs**
- **Hermetic 24-Pin DIP**
- **Polycrystalline Silicon Fuses for Higher Fuse Reliability**

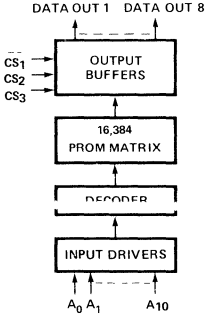
The Intel® M3636 is a fully decoded 16,384 bit PROM organized as 2048 words by 8 bits. The worst case access time of 80 ns is specified over the −55°C to +125°C temperature range and 5% V_{CC} power supply tolerances. There are three chip selects provided to facilitate expansion into larger PROM arrays. The PROMs use the Schottky clamped TTL technology with polycrystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

Prior to the 16,384 bit M3636, the highest density bipolar PROM available was 8196 bits. The high density of the M3636 now easily doubles the capacity without an increase in area on existing designs currently using 1024 by 8-bit PROMs. There is also little, if any, penalty in power since the power/bit is approximately one-half that of 8K PROMs. The M3636 is packaged in a hermetic 24-pin dual in-line package.

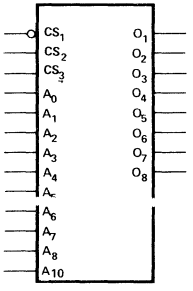
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

$A_0 - A_{10}$	ADDRESS INPUTS
$\overline{CS_1}$, CS_2, CS_3	CHIP SELECT INPUTS[1]
$O_1 - O_8$	DATA OUTPUTS

[1] To select the PROM $\overline{CS_1} = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$

MILITARY

PROGRAMMING

The programming specifications are described in the PROM/ROM Programming section of the Data Catalogue.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −65°C to +125°C
Storage Temperature ..... −65°C to +160°C
Output or Supply Voltages ..... −0.5V to 7 Volts
All Input Voltages ..... −1V to 5.5V
Output Currents ..... 100 mA

**Comment:* Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

All Limits Apply for $V_{CC} = +5.0V \pm 5\%$, $T_A = -55°C$ to $125°C$ unless otherwise specified

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.25V$, $V_A = 0.45V$
I_{FS}	Chip Select Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.25V$, $V_S = 0.45V$
I_{RA}	Address Input Leakage Current			40	μA	$V_{CC} = 5.25V$, $V_A = 5.25V$
I_{RS}	Chip Select Input Leakage Current			40	μA	$V_{CC} = 5.25V$, $V_S = 5.25V$
$\|I_O\|$	Output Leakage for High Impedance State			100	μA	$V_O = 5.25V$ or 0.45V, $V_{CC} = 5.25V$, $CS_1 = 2.4V$
I_{SC}[1]	Output Short Circuit Current	−20	−35	−80	mA	$V_O = 0V$
V_{CA}	Address Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.75V$, $I_A = -10$ mA
V_{CS}	Chip Select Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.75V$, $I_S = -10$ mA
V_{OH}	Output High Voltage	2.4	3.0		V	$I_{OH} = -2.4$ mA, $V_{CC} = 4.75V$
V_{OL}	Output Low Voltage		0.3	0.45	V	$V_{CC} = 4.75V$, $I_{OL} = 10$ mA
I_{CC}	Power Supply Current		150	185	mA	$V_{CC} = 5.25V$
V_{IL}	Input "Low" Voltage			0.85	V	$V_{CC} = 5.0V \pm 5\%$, $T_A = 25°C$
V_{IH}	Input "High" Voltage	2.0			V	$V_{CC} = 5.0V \pm 5\%$, $T_A = 25°C$

Notes:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. Unmeasured outputs are open during this test.

MILITARY

A.C. CHARACTERISTICS $V_{CC} = \pm 5 \pm 5\%$, $T_A = -55°C$ to $125°C$

SYMBOL	PARAMETER	MAX. LIMITS	UNIT	CONDITIONS
T_A	Address to Output Delay	80	ns	$\overline{CS}_1 = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$ to select the PROM.
t_{EN}	Output Enable Time	50	ns	
t_{DIS}	Output Disable Time	50	ns	

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

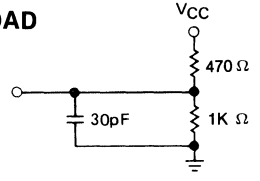
SYMBOL	PARAMETER	TYP. LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$	$V_{OUT} = 2.5V$

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

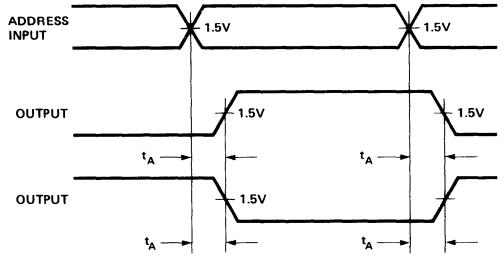
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test – 2.5 MHz

10 mA TEST LOAD

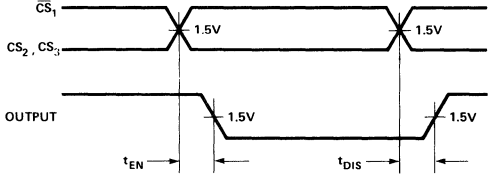


WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



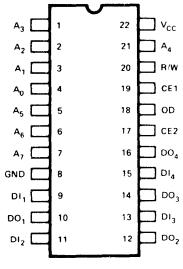
M5101-4, M5101L-4
256 x 4 BIT STATIC CMOS RAM

- **Military Temperature Range: -55°C to +125°C**
- **Ultra Low Standby Current: 200nA/Bit**
- **Fast Access Time — 800ns**
- **Single +5V Power Supply**
- **CE2 Controls Unconditional Standby Mode**
- **Three-State Output**

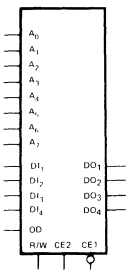
The Intel® M5101 is an ultra-low power 256 X 4 CMOS RAM specified over the -55°C to +125°C temperature range. The RAM uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. When deselected with CE2 low, the M5101 draws from the single 5-volt supply only 200 microamps at 125°C.

The Intel® M5101 is fabricated with an ion-implanted, silicon gate, Complementary MOS (CMOS) process. This technology allows the design and production of ultra-low power, high performance memories.

PIN CONFIGURATION
5101



LOGIC SYMBOL
5101



PIN NAMES

DI_1 - DI_4	DATA INPUT	OD	OUTPUT DISABLE
A_0 - A_7	ADDRESS INPUTS	DO_1 - DO_4	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$ CE2	CHIP ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . -65°C to 135°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . -0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

*COMMENT.

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS FOR M5101-4, M5101L-4

T_A = -55°C to 125°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}[2]	Input Current		8		nA	V_{IN} = 0 to 5.25V
I_{LOH}[2]	Output High Leakage			2	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = V_{CC}
I_{LOL}[2]	Output Low Leakage			2	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = 0.0V
I_{CC1}	Operating Current		11	25	mA	V_{IN} = V_{CC} Except $\overline{CE1}$ ≤0.01V Outputs Open
I_{CC2}	Operating Current		20	32	mA	V_{IN} = 2.2V Except $\overline{CE1}$ ≤0.5V Outputs Open
I_{CCL}[2]	Standby Current		2	200	μA	V_{IN} = 0 to V_{CC}, Except CE2 ≤ 0.2V
V_{IL}	Input "Low" Voltage	-0.3		0.5	V	
V_{IH}	Input "High" Voltage	V_{CC}-2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	V_{CC}-2.0			V	I_{OH} = 1.0mA

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in I_{CCL}.

MILITARY

Low V_{CC} Data Retention Characteristics (For M5101L-4) T_A = -55°C to 125°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	CE2 ≤ 0.2V	V_{DR} = 2.0V.
I_{CCDR}	Data Retention Current		2	200	μA		
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[2]			ns		

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.
2. t_{RC} = Read Cycle Time.

A.C. CHARACTERISTICS FOR M5101-4, M5101L-4

READ CYCLE T_A = -55°C to 125°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	800			ns	(See below)
t_A	Access Time			800	ns	
t_{CO1}	Chip Enable ($\overline{CE1}$) to Output			700	ns	
t_{CO2}	Chip Enable (CE2) to Output			850	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}	Data Output to High Z State	0		150	ns	
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0			ns	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	800			ns	(See below)
t_{AW}	Write Delay	150			ns	
t_{CW1}	Chip Enable ($\overline{CE1}$) To Write	550			ns	
t_{CW2}	Chip Enable (CE2) To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

A. C. CONDITIONS OF TEST

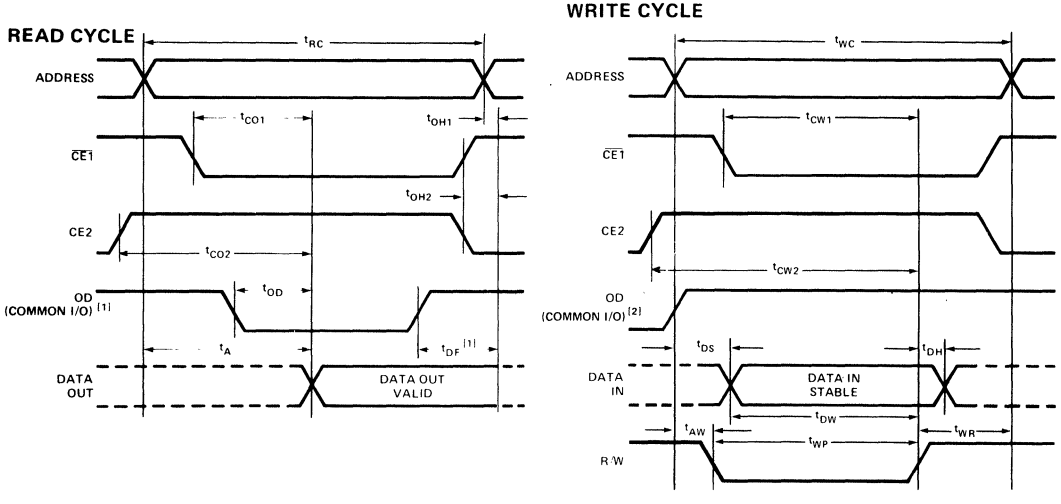
Input Pulse Levels: 0.5 Volt to V_{CC}-2.0 Volt
Input Pulse Rise and Fall Times: 20nsec
Timing Measurement Reference Level: 1.5 Volt
Output Load: 1 TTL Gate and C_L = 100pF

CAPACITANCE[3] T_A = 25°C, f = 1MHz

Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

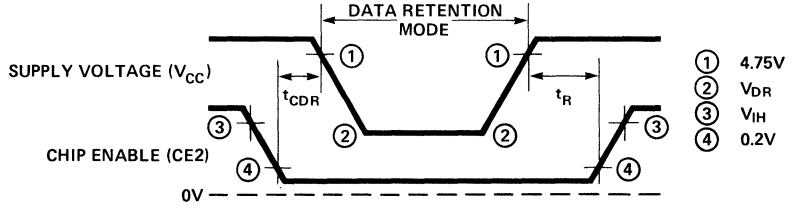
NOTE: 3. This parameter is periodically sampled and is not 100% tested.

WAVEFORMS



NOTES: 1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

Low V_{CC} Data Retention



M8080A

8-BIT N-CHANNEL MIRCOPROCESSOR

The M8080A is functionally compatible with the Intel® 8080.

- **Fully Military Temperature Range −55°C to +125°C**
- **±10% Power Supply Tolerance**
- **2 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **6 General Purpose Registers and an Accumulator**
- **16-Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **16-Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary, and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**
- **TTL Drive Capability**

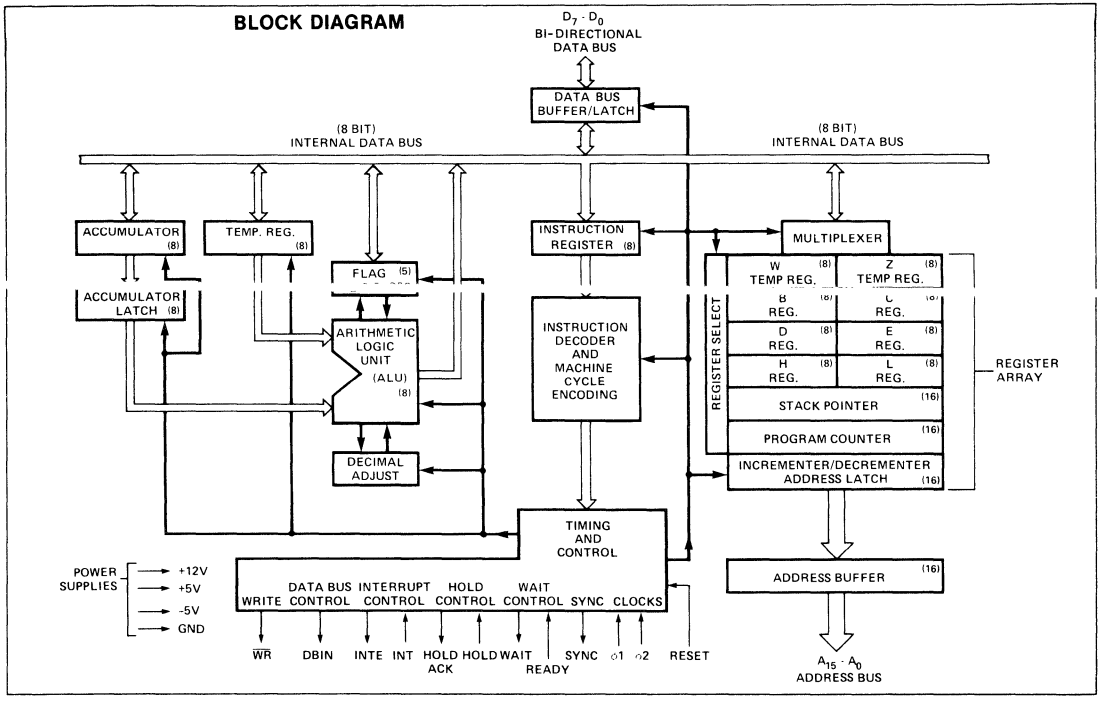
The Intel® M8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The M8080A contains 6 8-bit general purpose working registers and an accumulator. The 6 general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset 4 testable flags. A fifth flag provides decimal arithmetic operation.

The M8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store /retrieve the contents of the accumulator, flags, program counter and all of the 6 general purpose registers. The 16-bit stack pointer controls the addressing of this external stack. This stack gives the M8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bidirectional data busses are used to facilitate easy interface to memory and I/O. SIgnals to control the interface to memory and I/O are provided directly by the M8080A. Ultimate control of the address and data busses resides with the hold signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling device for (DMA) direct memory access or multi-processor operation.

BLOCK DIAGRAM



MILITARY

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the M8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the M8080A instruction set.

The following special instruction group completes the M8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the M8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Immediate mode or I/O instructions

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

Jump, call or direct load and store instructions

For the M8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

MILITARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.7W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IHC}	Clock Input High Voltage	8.5		$V_{DD}+1$	V	
V_{IL}	Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IH}	Input High Voltage	3.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		50	80	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	100	mA	T_{CY} = .48 μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}+0.8V$ $V_{SS}+0.8V \leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS} + 0.45V$

CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:

1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

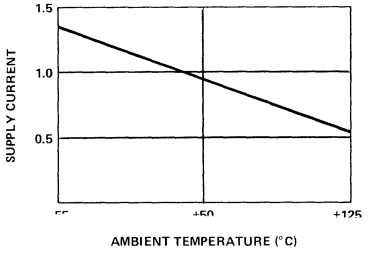


Figure 1. Typical Supply Current vs. Temperature, Normalized[3]

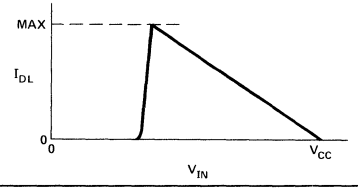


Figure 2. Data Bus Characteristic During DBIN

MILITARY

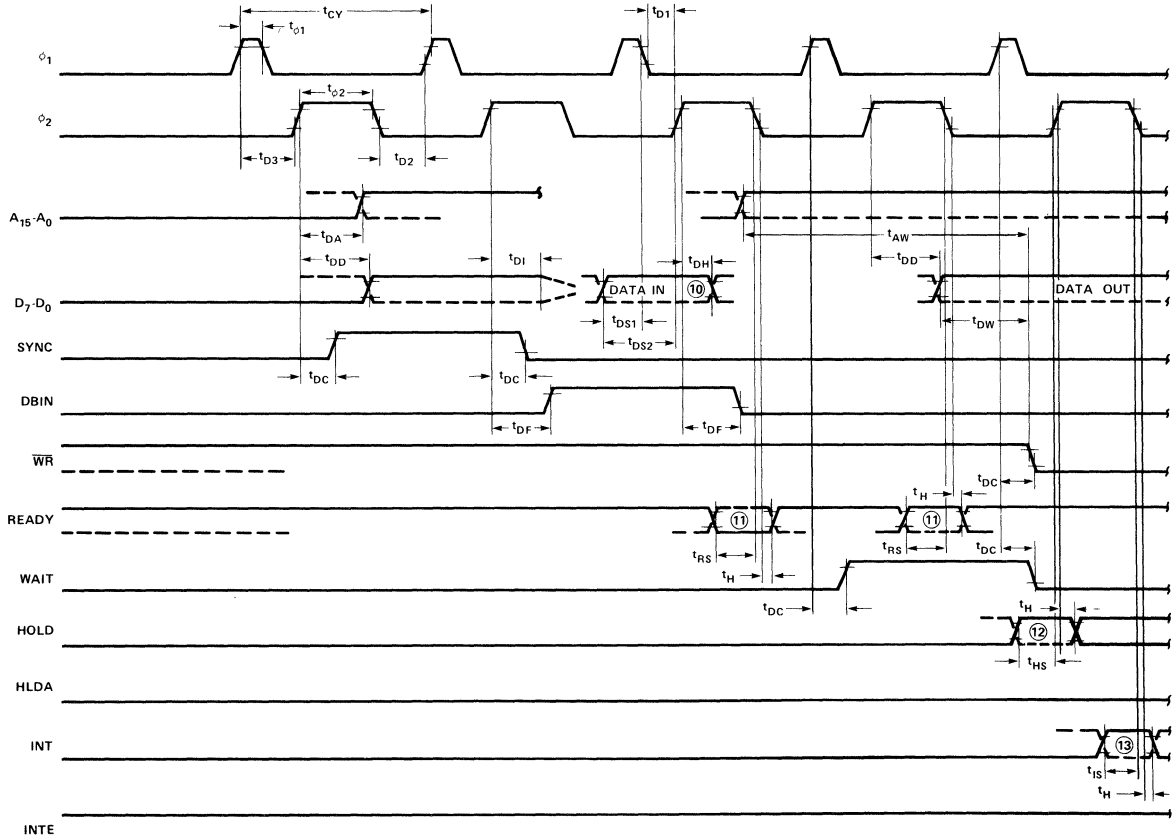
A.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	0.48	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	80		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{DD}[2]	Data Output Delay From ϕ_2		220	nsec	
t_{DC}[2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$,WAIT,HLDA)		140	nsec	
t_{DF}[2]	DBIN Delay From ϕ_2	25	150	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		nsec	

WAVEFORMS[14]

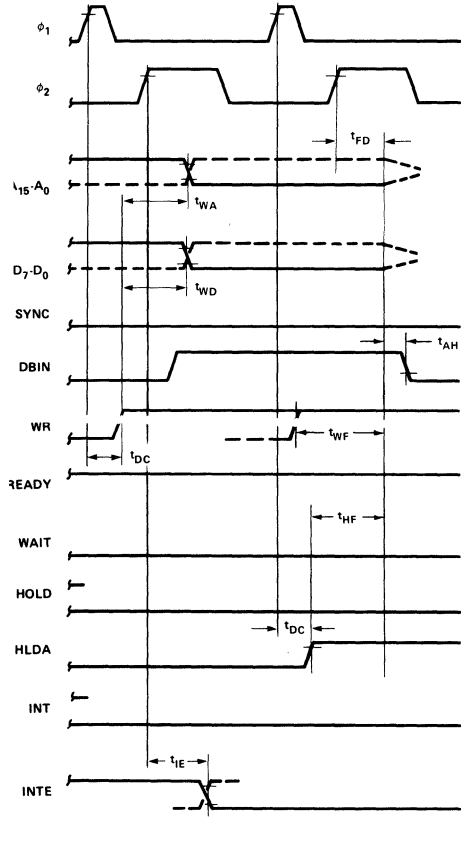
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 7.0V, "0" = 1.0V; INPUTS "1" = 3.0V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



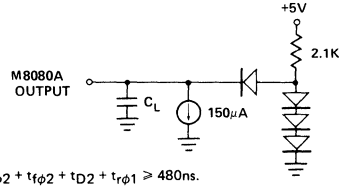
A.C. CHARACTERISTICS (Continued)

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	130		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	120		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		nsec	
t_{IS}	INT Setup Time During ϕ_2	120		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		130	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L=50pf
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	

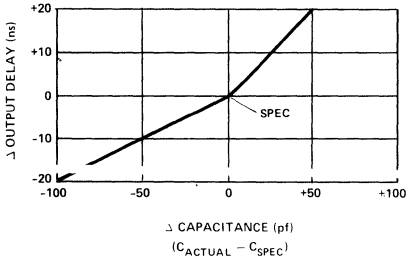


NOTES:
1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi 2} + t_{\phi 2} + t_{f\phi 2} + t_{D2} + t_{r\phi 1} \geq 480$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the M8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi 2} - 140$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi 2} - 170$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi 2} + 10$ns If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi 2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi 2} - 10$ns
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

MILITARY

M8212
8-BIT INPUT/OUTPUT PORT

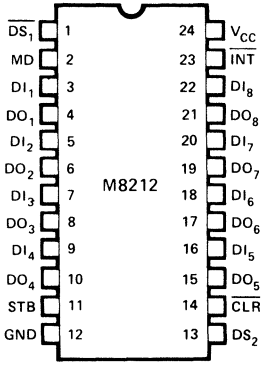
- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current 0.25mA Max**
- **3-State Outputs**
- **Full Military Temperature Range -55° C to +125° C**
- **3.4V Output High Voltage for Direct Interface to M8080A CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches, and Multiplexers in Microcomputer Systems**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**
- **24-Pin Dual In-Line Package**

The Intel® M8212/M3212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

*Note: The specifications for the M3212 are identical with those for the M8212.

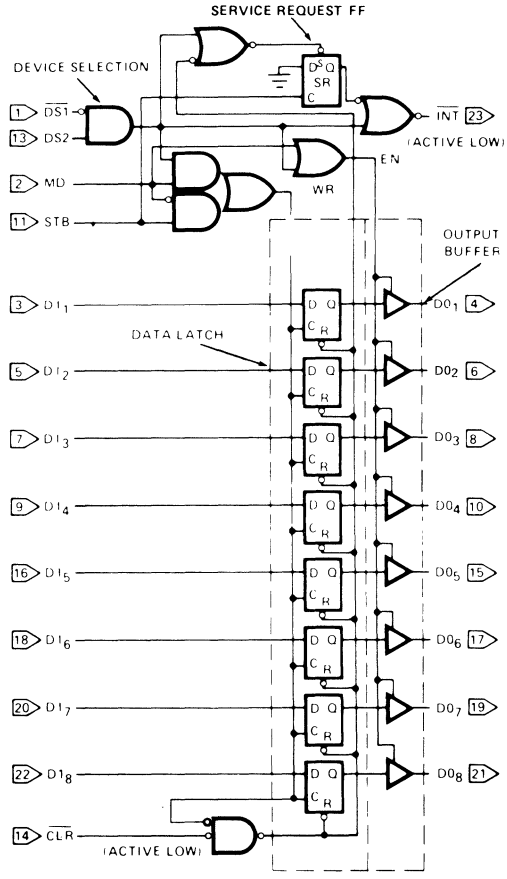
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



MILITARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +160°C
All Output or Supply Voltages .... −0.5 to +7 Volts
All Input Voltages ..... −1.0 to 5.5 Volts
Output Currents ..... 100 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current STB, DS_2, CR, DI_1-DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current STB, DS, CR, DI_1-DI_8 Inputs			10	μA	$V_R = V_{CC}$
I_R	Input Leakage Current MD Input			30	μA	$V_R = V_{CC}$
I_R	Input Leakage Current DS_1 Input			40	μA	$V_R = V_{CC}$
V_C	Input Forward Voltage Clamp			−1.2	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.80	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 10mA
V_{OH}	Output "High" Voltage	3.5	4.0		V	I_{OH} = -.5mA
I_{OS}	Short Circuit Output Current	-15		-75	mA	V_{CC} = 5.0V
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current		90	145	mA	

A.C. CHARACTERISTICS

T_A = -55°C to +125°C V_{CC} = +5V ±10%

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
t_{PW}	Pulse Width	40		ns	
t_{PD}	Data To Output Delay		30	ns	NOTE 1
t_{WE}	Write Enable To Output Delay		50	ns	NOTE 1
t_{SET}	Data Setup Time	20		ns	
t_H	Data Hold Time	30		ns	
t_R	Reset To Output Delay		55	ns	NOTE 1
t_S	Set To Output Delay		35	ns	NOTE 1
t_E	Output Enable/Disable Time		50	ns	NOTE 1 C_L = 30 pF
t_C	Clear To Output Delay		55	ns	NOTE 1

CAPACITANCE F = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = +5V, T_A = 25°C

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	$\overline{DS}_1$ MD Input Capacitance	9 pF	15 pF
C_{IN}	DS_2, $\overline{CLR}$, STB, DI_1-DI_8 Input Capacitance	5 pF	10 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8 pF	15 pF

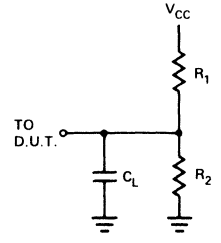
SWITCHING CHARACTERISTICS

Conditions of Test

Input Pulse Amplitude = 2.5V

Input Rise and Fall Times: 5 ns between 1V and 2V

Test Load

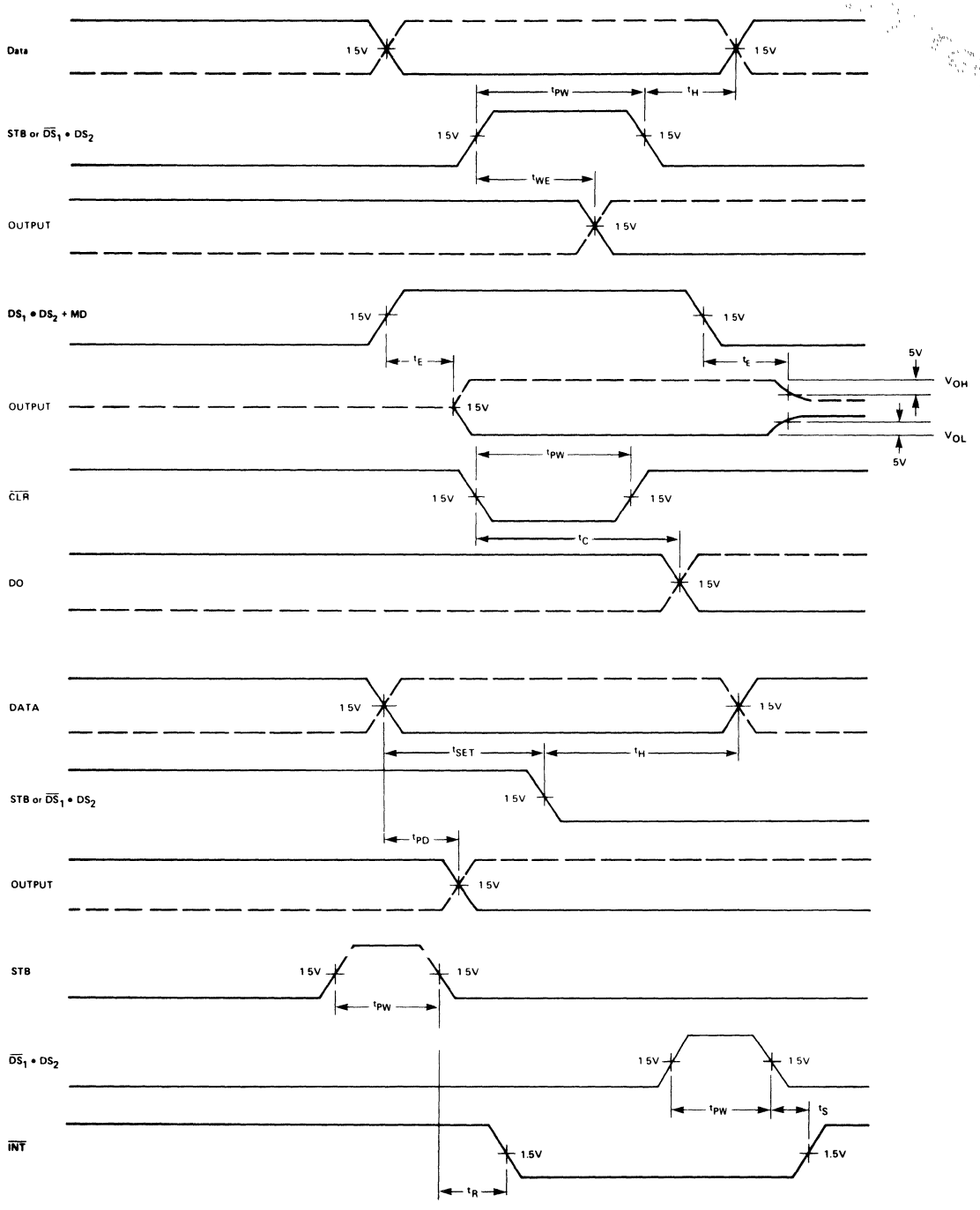


NOTE 1:

TEST	C_L	R_1	R_2
t_{PD}, t_{WE}, t_R, t_S, t_C	30pF	300Ω	600Ω
t_E, ENABLE↑	30pF	10KΩ	1KΩ
t_E, ENABLE↓	30pF	300Ω	600Ω
t_E, DISABLE↑	5pF	300Ω	600Ω
t_E, DISABLE↓	5pF	10KΩ	1KΩ

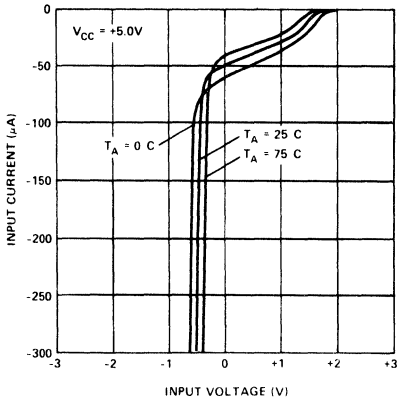
MILITARY

TIMING DIAGRAM

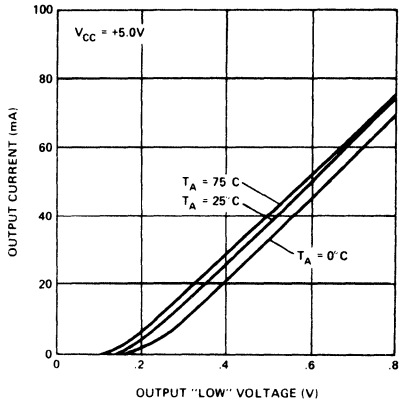


TYPICAL CHARACTERISTICS

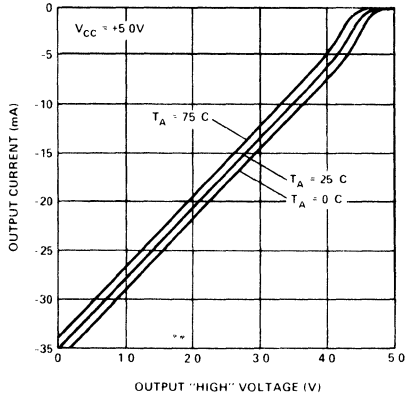
INPUT CURRENT VS. INPUT VOLTAGE



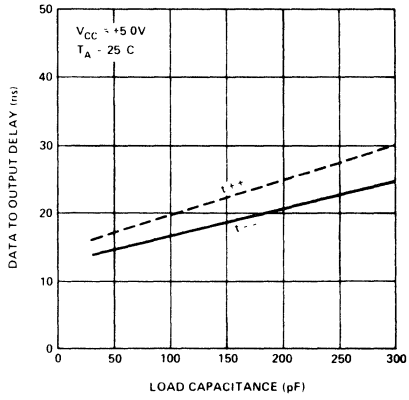
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



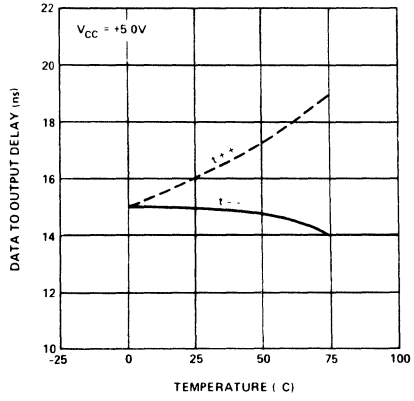
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



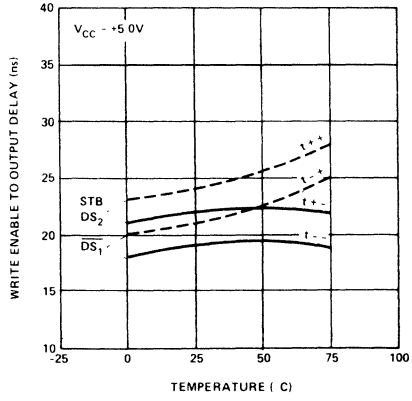
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA TO OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



MILITARY

M8214
PRIORITY INTERRUPT CONTROL UNIT

- **8 Priority Levels**
- **Fully Expandable**
- **Current Status Register**
- **Priority Comparator**
- **24-Pin Dual In-Line Package**
- **Full Military Temperature Range −55°C to +125°C**
- **+10% Power Supply Tolerance**

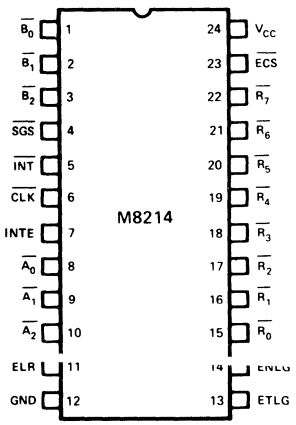
The Intel® M8214 is an 8-level priority interrupt control unit (PICU) designed to simplify interrupt-driven microcomputer systems.

The PICU can accept 8 requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue and interrupt to the system along with vector information to identify the service routine.

The M8214 is fully expandable by the use of open collector interrupt output vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt-driven microcomputer systems.

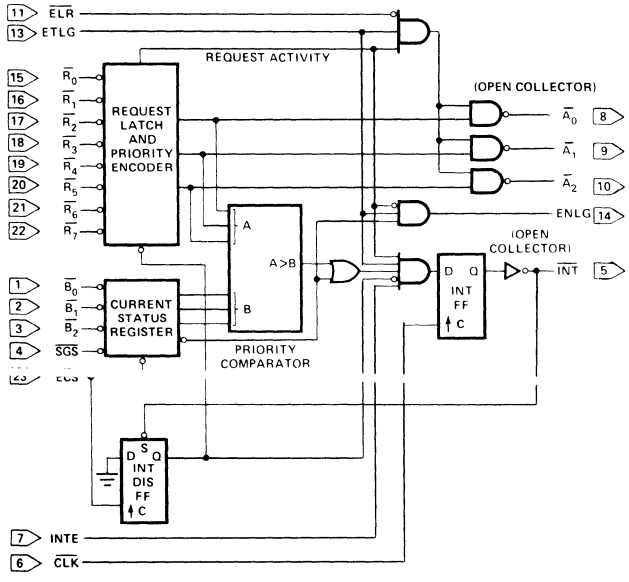
PIN CONFIGURATION



PIN NAMES

INPUTS		
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)	
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS	
$\overline{SGS}$	STATUS GROUP SELECT	
$\overline{ECS}$	ENABLE CURRENT STATUS	
INTE	INTERRUPT ENABLE	
$\overline{CLK}$	CLOCK (INT F-F)	
$\overline{ELR}$	ENABLE LEVEL READ	
ETLG	ENABLE THIS LEVEL GROUP	
OUTPUTS		
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS	OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT LOW)	OPEN COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP	

LOGIC DIAGRAM



MILITARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +160°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Output Currents . . . . . 100 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 55°C to 125°C V_{CC} = 5V ±10%

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage (all inputs)			-1.2	V	I_C=-5mA
I_F	Input Forward Current: ETLG input		-.15	-0.5	mA	V_F=0.45V
	all other inputs		-.08	-0.25	mA	
I_R	Input Reverse Current: ETLG input			80	μA	V_R=5.5V
	all other inputs			40	μA	
V_{IL}	Input LOW Voltage: all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage: all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current		90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage: all outputs		.3	.45	V	I_{OL}=10mA
V_{OH}	Output HIGH Voltage: ENLG output	2.4	3.0		V	I_{OH}=-1mA
I_{OS}	Short Circuit Output Current: ENLG output	-15	-35	-55	mA	V_{CC}=5.0V
I_{CEX}	Output Leakage Current: $\overline{INT}$, $\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$			100	μA	V_{CEX}=5.5V

NOTES:
1. Typical values are for T_A = 25° C, V_{CC} = 5.0V.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

MILITARY

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
t_{CY}	$\overline{CLK}$ Cycle Time	85			ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	25		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{CLK}$	90	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{CLK}$	100	55		ns
t_{RCH}[3]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	30	ns
t_{RIS}[4]	$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$-$\overline{R_7}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		100	130	ns
t_{ETA}	ETLG to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{ECS}$	20	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{ECS}$	20	10		ns
t_{REN}	$\overline{R_0}$-$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	30	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	110	ns
t_{ECSN}	ECS to ENLG Propagation Delay		55	55	ns

CAPACITANCE

Symbol	Parameter	Limits Min.	Typ.[1]	Max	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance Except ENLG (Pin 14)		7	12	pF

Test Conditions: V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C, f = 1 MHz

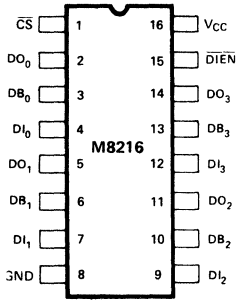
MILITARY

M8216/M8226
4-BIT PARALLEL BIDIRECTIONAL BUS DRIVER

- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current: 0.25mA Maximum**
- **High Output Drive Capability for Driving System Data Bus**
- **16-Pin Dual In-Line Package**
- **3.40V Output High Voltage for Direct Interface to 8080 CPU**
- **3-State Outputs**
- **Full Military Temperature Range -55°C to +125°C**
- **±10% Power Supply Tolerance**

The M8216/M8226 is a 4-bit bidirectional bus driver/receiver. All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.40V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50 mA I_{OL} capability. A non-inverting (M8216) and an inverting (M8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

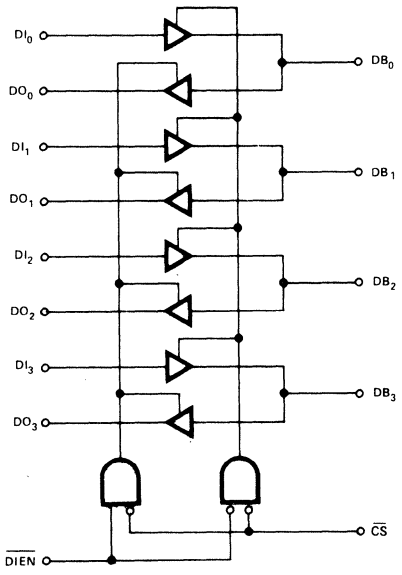
PIN CONFIGURATION



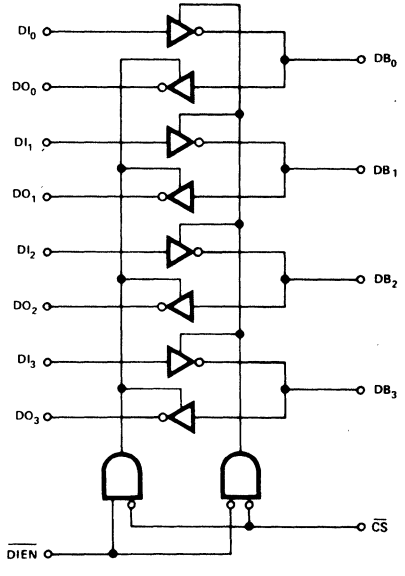
PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM M8216



LOGIC DIAGRAM M8226



MILITARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +160°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Output Currents . . . . . 125 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

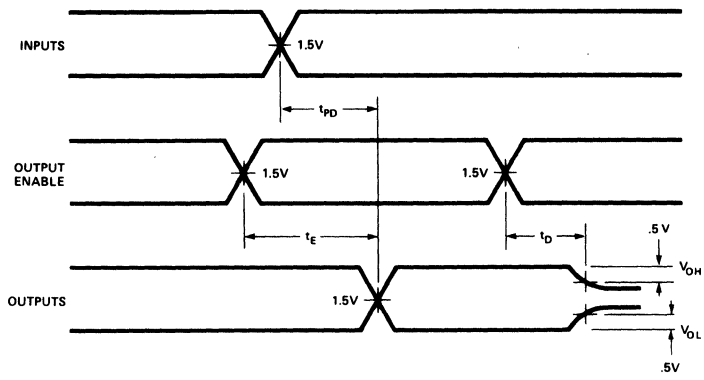
T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Conditions
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		-0.15	-.5	mA	V_F = 0.45
I_{F2}	Input Load Current All Other Inputs		-0.08	-.25	mA	V_F = 0.45
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$			20	μA	V_R = 5.5V
I_{R2}	Input Leakage Current DI Inputs			10	μA	V_R = 5.5V
V_C	Input Forward Voltage Clamp			-1.2	V	I_C = -5mA
V_{IL}	Input "Low" Voltage M8216			.95	V	V_{CC} = 5V
V_{IL}	Input "Low" Voltage M8226			.90	V	V_{CC} = 5V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5V
$\|I_O\|$	Output Leakage Current (3-State) DO DB			20 100	μA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current M8216		95	130	mA	
I_{CC}	Power Supply Current M8226		85	120	mA	
V_{OL1}	Output "Low" Voltage		0.3	.45	V	DO Outputs I_{OL} = 15mA DB Outputs I_{OL} = 25mA
V_{OL2}	Output "Low" Voltage		0.5	.6	V	DB Outputs I_{OL} = 45mA
V_{OH}	Output "High" Voltage	3.4	3.8		V	DO Outputs I_{OH} = -.5mA
V_{OH2}	Output "High" Voltage	2.4	3.0		V	DO Outputs I_{OH} = -2mA DB Outputs I_{OH} = -5.0mA
I_{OS}	Output Short Circuit Current	-15	-35	-65	mA	DO Outputs V_{CC} = 5.0V
		-30	-75	-120	mA	DB Outputs V_{CC} = 5.0V

NOTE: Typical values are for T_A = 25°C, V_{CC} = 5.0V.

MILITARY

WAVEFORMS



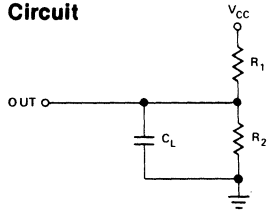
A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Conditions
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	(NOTE 2)
T_{PD2}	Input to Output Delay DB Outputs M8216		19	33	ns	(NOTE 2)
T_{PD2}	Input to Output Delay DB Outputs M8226		16	25	ns	(NOTE 2)
T_E	Output Enable Time M8216		42	75	ns	(NOTE 2)
T_E	Output Enable Time M8226		36	62	ns	(NOTE 2)
T_D	Output Disable Time M8216		16	40	ns	(NOTE 2)
T_D	Output Disable Time M8226		16	38	ns	(NOTE 2)

Test Conditions

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.

Test Load Circuit



CAPACITANCE

Symbol	Parameter		Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance			4	6	pF
C_{OUT1}	Output Capacitance	DO Outputs		6	10	pF
C_{OUT2}	Output Capacitance	DB Outputs		13	18	pF

Test Conditions: V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz.

NOTES: 1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.

2.

TEST	C_L	R_1	R_2
T_{PD1}	30pF	300Ω	600Ω
T_{PD2}	300pF	90Ω	180Ω
T_E, (DO, ENABLE↑)	30pF	10KΩ	1KΩ
T_E, (DO, ENABLE↓)	30pF	300Ω	600Ω
T_E, (DB, ENABLE↑)	300pF	10KΩ	1KΩ
T_E, (DB, ENABLE↓)	300pF	90Ω	180Ω
T_D, (DO, DISABLE↑)	5pF	300Ω	600Ω
T_D, (DO, DISABLE↓)	5pF	10KΩ	1KΩ
T_D, (DB, DISABLE↑)	5pF	90Ω	180Ω
T_D, (DB, DISABLE↓)	5pF	10KΩ	1KΩ

M8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

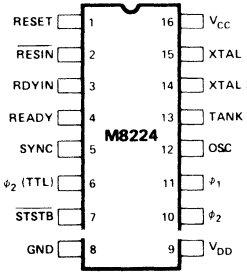
- **Single Chip Clock Generator/Driver for M8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Fully Military Temperature Range −55°C to +125°C**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**

The Intel® M8224 is a single chip clock generator/driver for the M8080A CPU. It is controlled by a crystal, selected by the designer to meet a variety of system speed requirements.

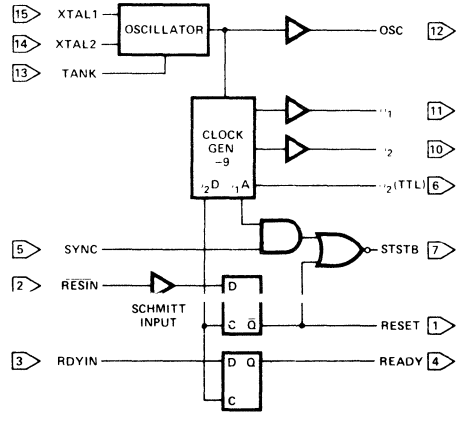
Also included are circuits to provide power-up reset, advance status trobe, and synchronization of ready.

The M8224 provides the designer with a significant reduction of packages used to generate clocks and timing for M8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

$\overline{RESIN}$	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
$\overline{STSTB}$	STATUS STB (ACTIVE LOW)
ϕ_1	8080 CLOCKS
ϕ_2	8080 CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
ϕ_2 (TTL)	ϕ_2 CLK (TTL LEVEL)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

MILITARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -55°C to 125°C
Storage Temperature . . . . . -65°C to 150°C
Supply Voltage, V_{CC} . . . . . -0.5V to +7V
Supply Voltage, V_{DD} . . . . . -0.5V to +13.5V
Input Voltage . . . . . -1.0V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to 125°C; V_{CC} = +5.0V ±10%; V_{DD} = +12V ±10%.

Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
I_F	Input Current Loading			-.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.5V
V_C	Input Forward Clamp Voltage			-1.2	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage $\overline{RESIN}$ All Other Inputs	2.6 2.0			V	
V_{IH}-V_{IL}	$\overline{RESIN}$ Input Hysteresis	.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage OSC, ϕ2 (TTL)			.45	V	I_{OL} = 10mA
	All Other Outputs			.45	V	I_{OL} = 2.5mA
V_{OH}	Output "High" Voltage					
	ϕ_1 , ϕ_2	9.0			V	I_{OH} = -100μA
	READY, RESET	3.3			V	I_{OH} = -100μA
	OSC, ϕ2 (TTL), $\overline{STSTB}$	2.4			V	I_{OH} = -1mA
I_{OS}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

Crystal Requirements

Tolerance: .005% at -55°C to 125°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

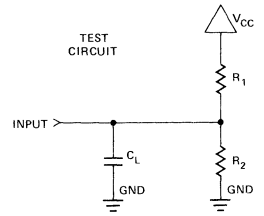
*With tank circuit use 3rd overtone mode.

MILITARY

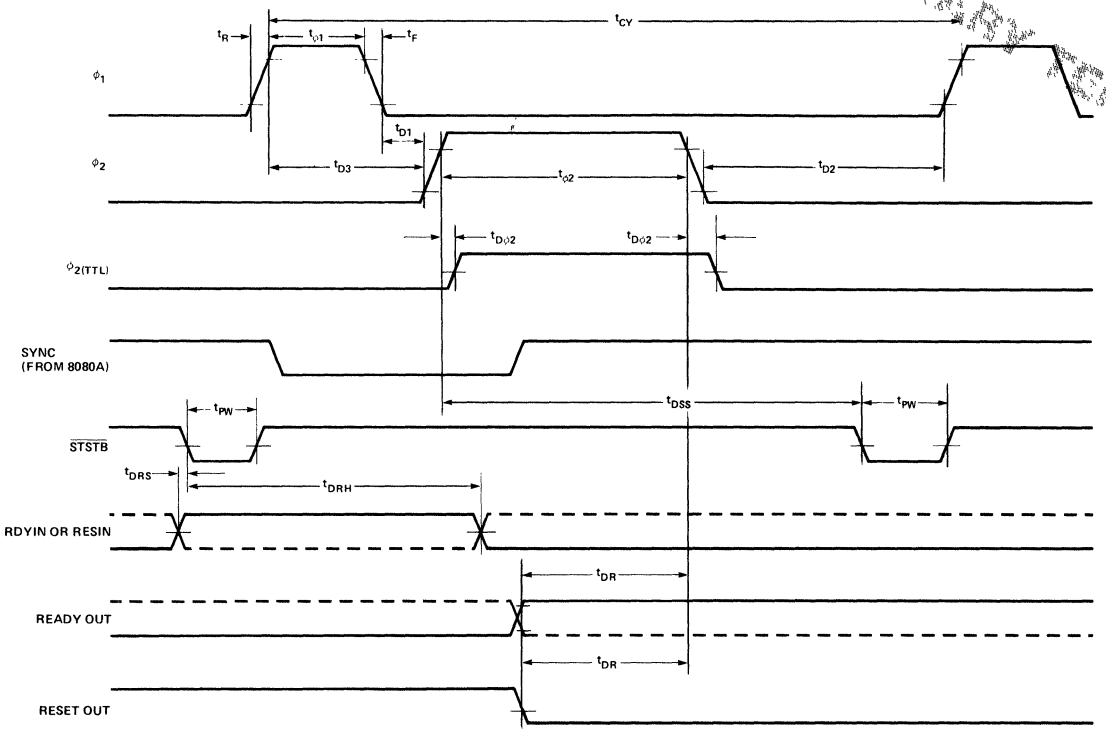
A.C. CHARACTERISTICS

V_{CC} = +5.0 ±10%; V_{DD} = +12.0V ±10%; T_A = -55°C to +125°C

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9}$ - 20ns			ns	C_L = 20pF to 50pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9}$ - 45ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9}$ - 25ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9}$ + 40ns		
t_R	ϕ_1 and ϕ_2 Rise Time			25		
t_F	ϕ_1 and ϕ_2 Fall Time			25		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2TTL,CL=30pF R_1=300Ω R_2=600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9}$ - 30ns		$\frac{6tcy}{9}$		
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9}$ - 23ns				$\overline{STSTB}$, CL=15pF R_1 = 2K R_2 = 4K
t_{DRS}	RDYIN Setup Time to Status Strobe	50ns - $\frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	READY or RESET to ϕ_2 Delay	$\frac{4tcy}{9}$ - 25ns				CL=10pF R_1=2K R_2=4K
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency	27			MHz	
C_{in}	Input Capacitance			8	pF	V_{CC}=+5.0V V_{DD}=+12V V_{BIAS}=2.5V f=1MHz



WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 7.0V. READY, RESET Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

Example:

A.C. CHARACTERISTICS (For t_{CY} = 488.28 ns.)

T_A = -55°C to 125°C; V_{DD} = +5V ±10%; V_{DD} = +12V ±10%.

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY}=488.28ns
$t_{\phi 2}$	ϕ_2 Pulse Width	226			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	84			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		149	ns	
t_r	Output Rise Time			25	ns	
t_f	Output Fall Time			25	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	31			ns	Ready & Reset Loaded to 2mA/10pF
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5V unless specified otherwise.
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	

MILITARY

M8228
SYSTEM CONTROLLER AND BUS DRIVER FOR M8080A CPU

- **Single Chip System Control for MCS-80™ Systems**
- **Built-In Bidirectional Bus Driver for Data Bus Isolation**
- **Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28-Pin Dual In-Line Package**
- **Reduces System Package Count**
- **Full Military Temperature Range −55°C to +125°C**
- **±10% Power Supply Tolerance**

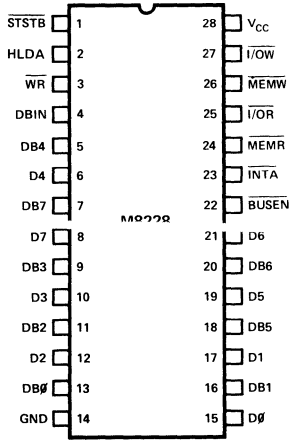
The Intel® M8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bidirectional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

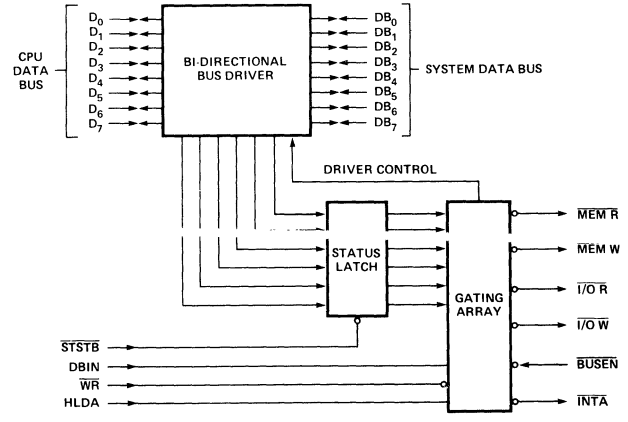
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The M8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an interrupt acknowledge by the M8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The M8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	$\overline{INTA}$	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
$\overline{I/OR}$	I/O READ	$\overline{WR}$	WR (FROM 8080)
$\overline{I/OW}$	I/O WRITE	$\overline{BUSEN}$	BUS ENABLE INPUT
$\overline{MEMR}$	MEMORY READ	$\overline{STSTB}$	STATUS STROBE (FROM 8224)
$\overline{MEMW}$	MEMORY WRITE	V_{CC}	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

MILITARY

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -55°C to 125°C
Storage Temperature . . . . . -65°C to 150°C
Supply Voltage, V_{CC} . . . . . -0.5V to +7V
Input Voltage . . . . . -1.0V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = -55°C to 125°C; V_{CC} = 5V ±10%.

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		-1.2	V	I_C = -5mA
I_F	Input Load Current, $\overline{STSTB}$		500	μA	
	D_2, D_6		750	μA	V_F = 0.4V
	D_0, D_1, D_4, D_5, D_7		250	μA	
	All Other Inputs		250	μA	
I_R	Input Leakage Current DB_0 - D_7		20	μA	V_R = 5.5V
	All Other Inputs		100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8	2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		210	mA	
V_{OL}	Output Low Voltage, D_0 - D_7		.5	V	I_{OL} = 2mA
	All Other Outputs		.5	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0 - D_7	3.3		V	I_{OH} = -10μA
	All Other Outputs	2.4		V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15	90	mA	V_{CC} = 5V
$I_{O\ (Off)}$	Off State Output Current, All Controls Outputs		100	μA	V_O = 5.5V
			-100	μA	V_O = .45V
I_{INT}	$\overline{INTA}$ Current		5	mA	(See Figure 1)

Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

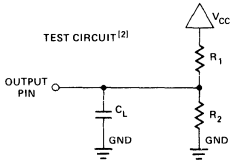
MILITARY

CAPACITANCE This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, f = 1MHz.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.



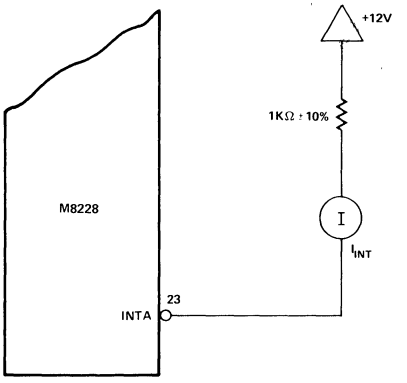


Figure 1. INTA Test Circuit (for RST 7)

A.C. CHARACTERISTICS $T_A = -55°C$ to $125°C$; $V_{CC} = 5V \pm 10\%$.

Symbol	Parameter	Limits Min.	Max.	Units	Condition
t_{PW}	Width of Status Strobe	25		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	75	ns	$C_L = 100pF$
t_{RR}	Delay from DBIN to Control Outputs		30	ns	$C_L = 100pF$
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	$C_L = 25pF$
t_{RD}	Delay from System Bus to 8080 Bus during Read		45	ns	$C_L = 25pF$
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	60	ns	$C_L = 100pF$
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	$C_L = 100pF$
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	$C_L = 100pF$
t_E	Delay from System Bus Enable to System Bus DB_0-DB_7		30	ns	$C_L = 100pF$
t_{HD}	HLDA to Read Status Outputs		25	ns	$C_L = 100pF$
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	

MILITARY

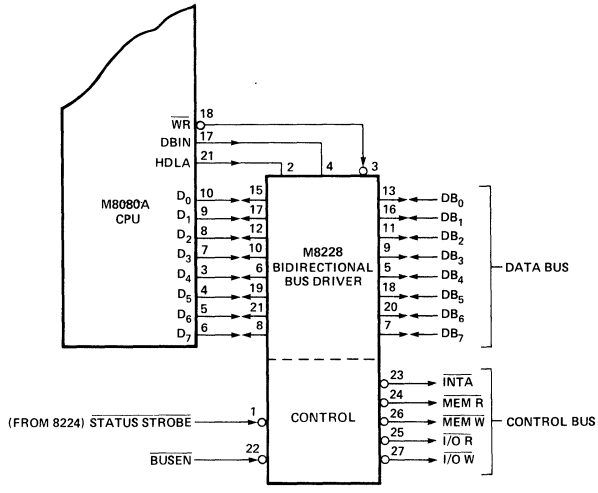


Figure 2. M8080A CPU Interface

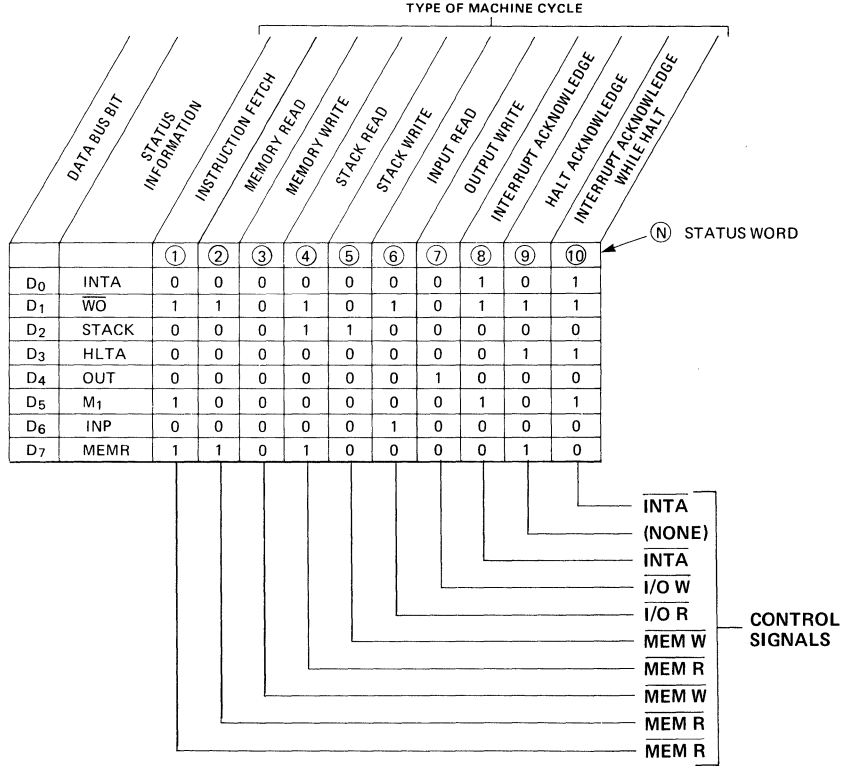
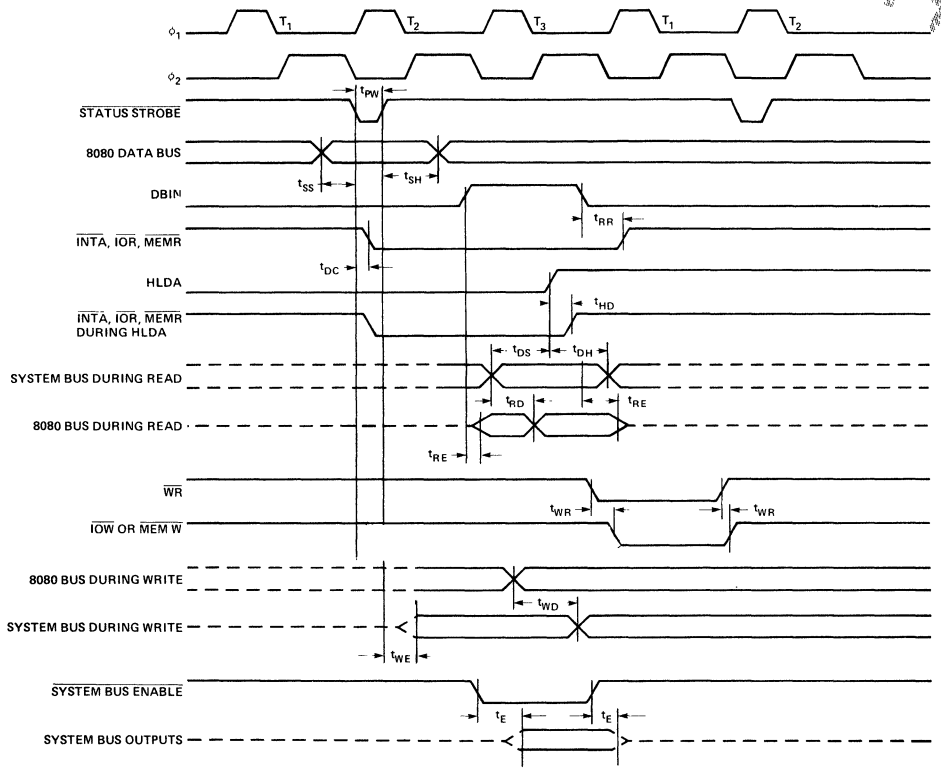


Figure 3. Status Word Chart

WAVEFORMS



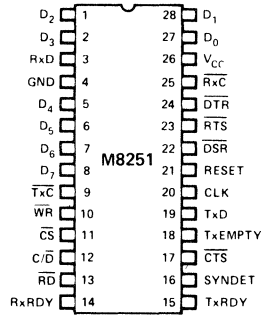
VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

M8251
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    5-8 Bit Characters
    Internal or External Character Synchronization
    Automatic Sync Insertion
  - **Asynchronous:**
    5-8 Bit Characters
    Clock Rate — 1,16 or 64 Times Baud Rate
    Break Character Generation
    1, 1½, or 2 Stop Bits
    False Start Bit Detection
- **Baud Rate — DC to 56k Baud (Sync Mode)**
  DC to 8.1k Baud (Async Mode)
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **All Inputs and Outputs Are TTL Compatible**
- **Full Military Temperature Range -55°C to +125°C**
- **±10% Power Supply Tolerance**

The M8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.

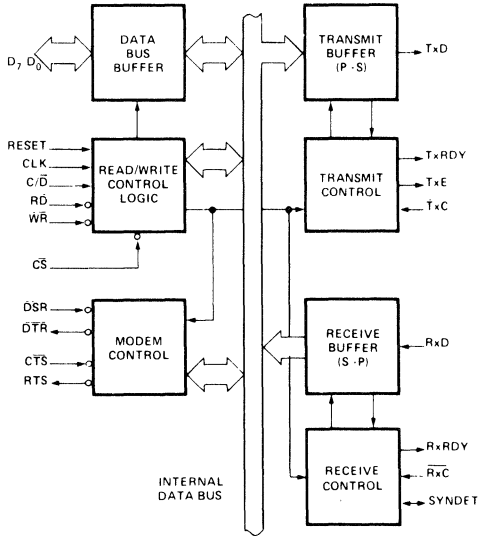
PIN CONFIGURATION



Pin Name	Pin Function
D_7 D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char from 8080)

Pin Name	Pin Function
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET	Sync Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

M8251 BLOCK DIAGRAM



MILITARY

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to GND . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100μA
I_{DL}	Data Bus Leakage			50 10	μA μA	V_{OUT} = .45V V_{OUT} = V_{CC}
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.5V
I_{CC}	Power Supply Current		45	80		

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

TEST LOAD CIRCUIT:

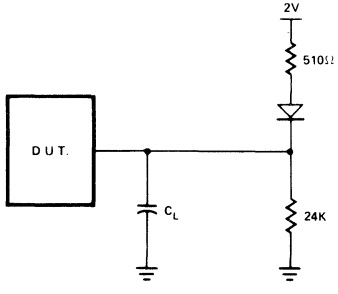
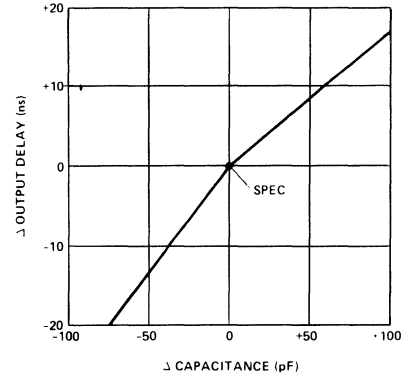


Figure 1.



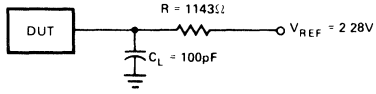
A.C. CHARACTERISTICS [2]

T_A = -55°C to +125°C; V_{CC} = 5.0V ±10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{CY}	Clock Period	.420		1.35	μs	
$t_{\phi W}$	Clock Pulse Width	220			ns	
t_R,t_F	Clock Rise and Fall Time	0		50	ns	
t_{WR}	$\overline{WRITE}$ Pulse Width	400			ns	
t_{DS}	Data Set-Up Time for $\overline{WRITE}$	200			ns	
t_{DH}	Data Hold Time for $\overline{WRITE}$	40			ns	
t_{AW}	Address Stable before $\overline{WRITE}$	20			ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	20			ns	
t_{RD}	READ Pulse Width	430			ns	
t_{DD}	Data Delay from $\overline{READ}$			350	ns	
t_{DF}	$\overline{READ}$ to Data Floating [3]	25		200	ns	C_L=15pF to 100pF
t_{AR}	Address (CE, C/$\overline{D}$) Stable before $\overline{READ}$	50			ns	
t_{RA}	Address (CE, C/$\overline{D}$) Hold Time for $\overline{READ}$	5			ns	
t_{DTx}	TxD Delay from Falling Edge of TxC			1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2			μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2			μs	
f_{Tx} [1]	Transmitter Clock Frequency					
	1X Baud Rate	DC		56	KHz	
	16X and 64X Baud Rate	DC		529	KHz	
f_{Rx} [1]	Receiver Clock Frequency					
	1X Baud Rate	DC		56	KHz	
	16X and 64X Baud Rate	DC		529	KHz	
t_{Tx}	TxRDY Delay from Center of Data Bit			16	CLK Period	
t_{Rx}	RxRDY Delay from Center of Data Bit	15		20	CLK Period	
t_{IS}	Internal Syndet Delay from Center of Data Bit	20		25	CLK Period	
t_{ES}	External Syndet Set-Up Time before Falling Edge of RxC			16	CLK Period	

Note 1: The TxC and RxC frequencies have the following limitation with respect to CLK.
For ASYNC Mode, t_{Tx} or $t_{Rx} \geq 4.5\ t_{CY}$
For SYNC Mode, t_{Tx} or $t_{Rx} \geq 30\ t_{CY}$
2. AC timings are measured at V_{OH} = 2.0V, V_{OL} = 0.8V, and load circuit of Figure 1.
3. Float timings are measured at V_{OH} = 2.48V, V_{OL} = 2.08V

Figure 1. Test Load Circuit.



WAVEFORMS (See 8251 Waveforms, page 10-155)

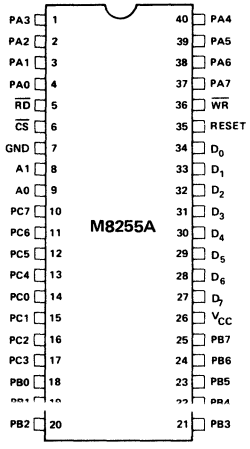
M8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with MCS-80™ Microprocessor Family**
- **Full Military Temperature Range −55°C to +125°C**
- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40-Pin Dual In-Line Package**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**

The Intel® M8255A is a general purpose programmable I/O device designed for use with microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

Other features of the M8255A include bit set and reset capability and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

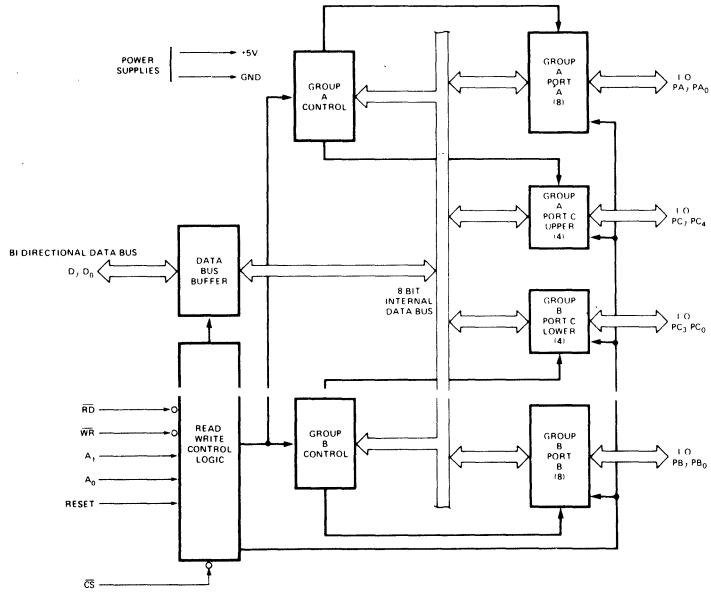
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	Ø VOLTS

M8255A BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

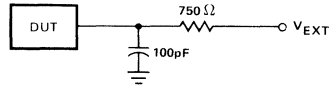
Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to GND . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = -55°C to +125°C; V_{CC} = +5V ±10%; GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45	V	I_{OL} = 2.5mA
V_{OL}(PER)	Output Low Voltage (Peripheral Port)		0.45	V	I_{OL} = 1.7mA
V_{OH}(DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH}(PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = -200μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V

Note 1: Available on any 8 pins from Port B and C.



A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%; GND = 0V

SYMBOL	PARAMETER	8255A MIN.	8255A MAX.	UNIT
t_{AR}	Address Stable Before READ	0		ns
t_{RA}	Address Stable After READ	0		ns
t_{RR}	READ Pulse Width	300		ns
t_{RD}	Data Valid From READ[1]		250	ns
t_{DF}	Data Float After READ	10	150	ns
t_{RV}	Time Between READs and/or WRITEs	850		ns
t_{AW}	Address Stable Before WRITE	0		ns
t_{WA}	Address Stable After WRITE	20		ns
t_{WW}	WRITE Pulse Width	400		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		ns
t_{WD}	Data Valid After WRITE	30		ns
t_{WB}	WR = 1 to Output[1]		350	ns
t_{IR}	Peripheral Data Before RD	0		ns
t_{HR}	Peripheral Data After RD	0		ns
t_{AK}	ACK Pulse Width	300		ns
t_{ST}	STB Pulse Width	500		ns
t_{PS}	Per. Data Before T.E. of STB	0		ns

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t_{PH}	Per. Data After T.E. of STB	180		ns
t_{AD}	ACK = 0 to Output[1]		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		650	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		300	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350	ns
t_{WIT}	WR = 0 to INTR = 0[1]		850	ns

Notes:
1. Test condition: 8255A: C_L = 100pF
2. Period of Reset pulse must be at least 50μF during or after power on. Subsequent Reset pulse can be 500ns min.

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

Figure 31. Test Load Circuit

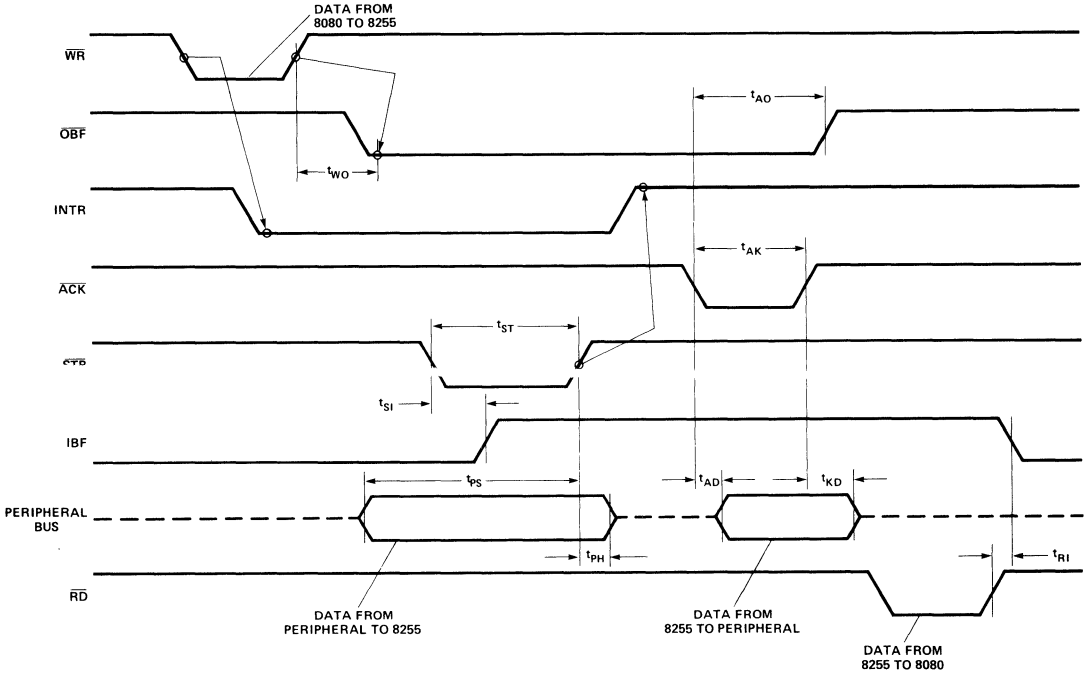

Figure 32. MODE 2 (Bidirectional)

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M8085A
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3 μs Instruction Cycle**
- **On-Chip Clock Generator (with External Crystal, LC or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible interrupt**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64k Bytes of Memory**

The Intel® M8085A is a complete 8-bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed.

The M8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The M8085A uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus.

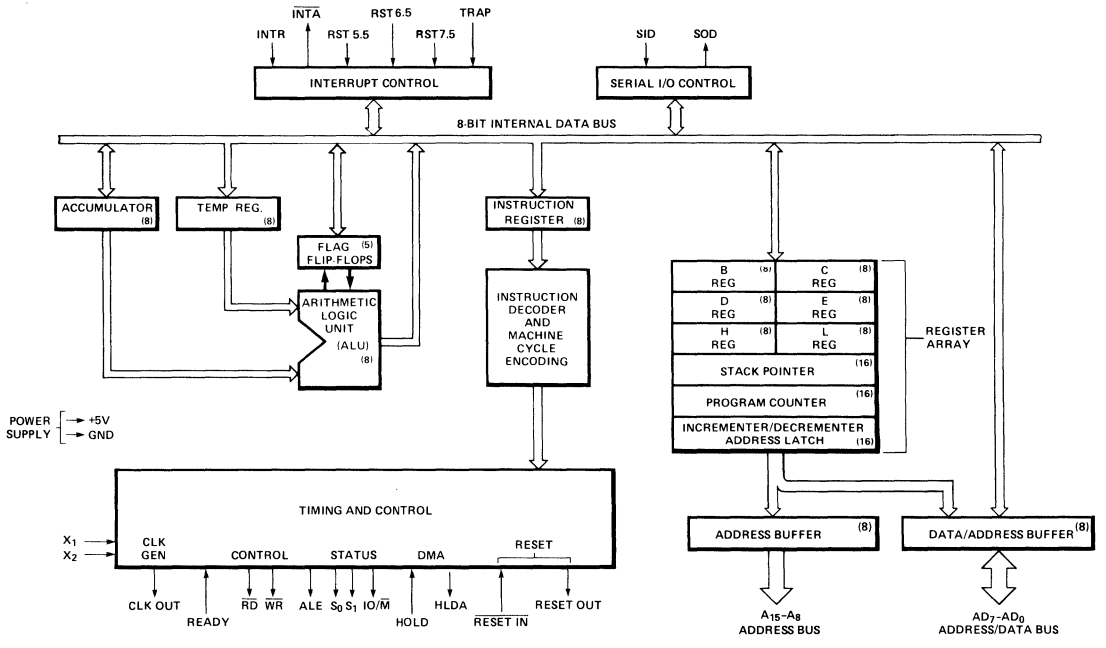

Figure 1. M8085A CPU Functional Block Diagram.

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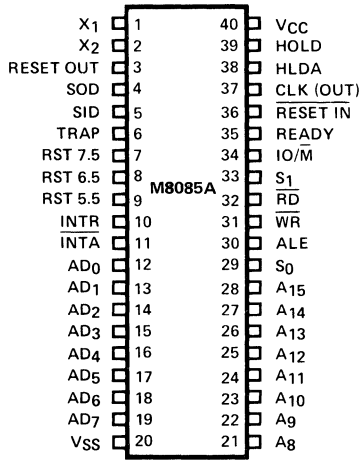

Figure 2. M8085A Pinout Diagram

M8085A FUNCTIONAL PIN DESCRIPTION

The following describes the function of each pin:

Symbol	Function
A_8–A_{15} (Output, 3-state)	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7} (Input/Output, 3-state)	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, and IO/$\overline{M}$ (Output)	Machine cycle status: IO/$\overline{M}$ S_1 S_0 Status 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Interrupt Acknowledge * 0 0 Halt * X X Hold * X X Reset * = 3-state (high impedance) X = unspecified
S_1	S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$,S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$ (Output, 3-state)	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ (Output, 3-state)	WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

M8085A FUNCTIONAL PIN DESCRIPTION (Continued)

Symbol	Function
$\overline{\text{INTA}}$ (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{\text{RD}}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5 (Inputs)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.)
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:

(1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

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FUNCTIONAL DESCRIPTION

The M8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz, thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU (8085A), a RAM/IO (8156), and a ROM or EPROM/IO chip (8355 or 8755A).

The M8085A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The M8085A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC,DE,HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The M8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The M8085A provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD, READY, and all Interrupts are synchronized with the processor's internal clock. The M8085A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the M8085A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

INTERRUPT AND SERIAL I/O

The M8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive.*

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. (See Section 2.2.7.) The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the M8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$. (See SIM, Chapter 4.)

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP — highest priority, RST 7.5, RST 6.5, RST 5.5, INTR — lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive.* The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the M8085A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

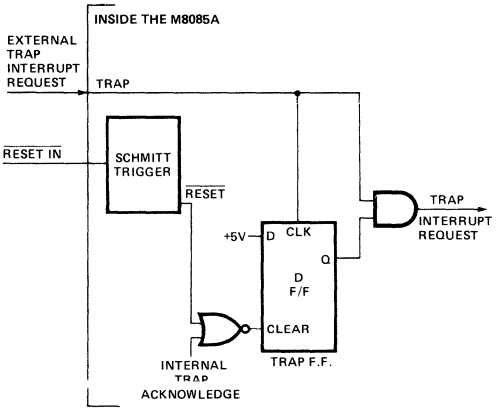

Figure 3. TRAP and $\overline{RESET\ IN}$ Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5–7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled. See the description of the RIM instruction in Chapter 4.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

BASIC SYSTEM TIMING

The M8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 4 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/$\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 2.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

TABLE 2. M8085A MACHINE CYCLE CHART

MACHINE CYCLE		STATUS			CONTROL		
		IO/$\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)	0	1	1	0	1	1
MEMORY READ	(MR)	0	1	0	0	1	1
MEMORY WRITE	(MW)	0	0	1	1	0	1
I/O READ	(IOR)	1	1	0	0	1	1
I/O WRITE	(IOW)	1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)	1	1	1	1	1	0
BUS IDLE	(BI): DAD	0	1	0	1	1	1
	ACK. OF RST,TRAP	1	1	1	1	1	1
	HALT	TS	0	0	TS	TS	1

TABLE 3. M8085A MACHINE STATE CHART

Machine State	Status & Buses				Control		
	S1,S0	IO/$\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}$,$\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0" TS = High Impedance
1 = Logic "1" X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction
† IO/M = 1 during T_4-T_6 of INA machine cycle.

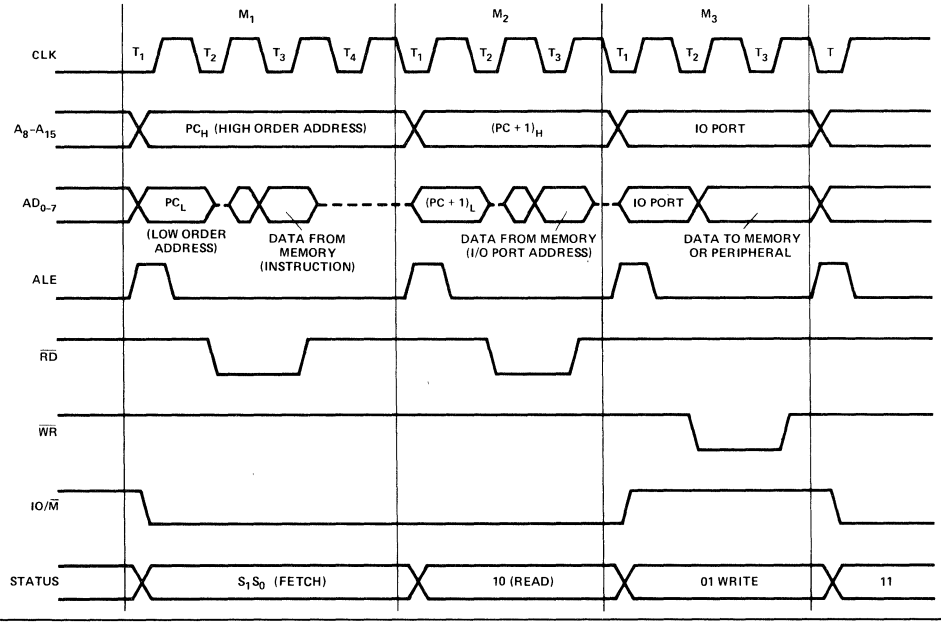

Figure 4. M8085A Basic System Timing

TABLE 4. ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . .–55°C to +125°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . .–0.5V to +7V
Power Dissipation . . . . . 1.5 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 4. D.C. CHARACTERISTICS

(T_A = -55°C to +125°C; V_{CC} = 5V ±10%; V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{CC}	Power Supply Current		200	mA	
I_{IL}	Input Leakage		±10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \leqslant V_{out} \leqslant V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} +0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

TABLE 5. A.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{CC} = 5V ±10%; V_{SS} = 0V

Symbol	Parameter	M8085A[2]		Units
		Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	ns
t_1	CLK Low Time	80		ns
t_2	CLK High Time	120		ns
t_r, t_f	CLK Rise and Fall Time		30	ns
t_{XKR}	X_1 Rising to CLK Rising	30	120	ns
t_{XKF}	X_1 Rising to CLK Falling	30	150	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control[1]	270		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575	ns
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0	ns
t_{AL}	A_{8-15} Valid Before Trailing Edge of ALE[1]	115		ns
t_{ALL}	A_{0-7} Valid Before Trailing Edge of ALE	90		ns
t_{ARY}	READY Valid from Address Valid		220	ns
t_{CA}	Address (A_8-A_{15}) Valid After Control	120		ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) Edge of ALE	400		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		ns
t_{HABE}	HLDA to Bus Enable		210	ns
t_{HABF}	Bus Float After HLDA		210	ns
t_{HACK}	HLDA Valid to TRailing Edge of CLK	110		ns
t_{HDH}	HOLD Hold Time	0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		ns
t_{INH}	INTR Hold Time	0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		ns
t_{LA}	Address Hold Time After ALE	100		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		ns
t_{LCK}	ALE Low During CLK High	100		ns
t_{LDR}	ALE to Valid Data During Read		460	ns
t_{LDW}	ALE to Valid Data During Write		200	ns
t_{LL}	ALE Width	140		ns
t_{LRY}	ALE to READY Stable		110	ns

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TABLE 5. A.C. CHARACTERISTICS (Cont.)

Symbol	Parameter	M8085A[2]		Units
		Min.	Max.	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		ns
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$ [7]	0		ns
t_{RYH}	READY Hold Time	0		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		ns
t_{WDL}	LEADING Edge of WRITE to Data Valid		40	ns

Notes:
1. A_8-A_{15} address Specs apply to IO/$\overline{M}$, S_0, and S_1 except A_8-A_{15} are undefined during T_4-T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable.
2. Test conditions: t_{CYC} = 320ns; C_L = 150pF.
3. For all output timing where C_L = 150pF use the following correction factors:
   25pF ≤ C_L < 150pF: -0.10 ns/pF
   150pF < C_L ≤ 300pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output voltage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20ns rise and fall time on inputs.
6. To calculate timing specifications at other values of t_{CYC} use Table 6.
7. Data hold time is guaranteed under all loading conditions.

TABLE 6. BUS TIMING SPECIFICATION AS A T_{CYC} DEPENDENT

M8085A

t_{AL}	–	(1/2) T - 45	MIN
t_{LA}	–	(1/2) T - 60	MIN
t_{LL}	–	(1/2) T - 20	MIN
t_{LCK}	–	(1/2) T - 60	MIN
t_{LC}	–	(1/2) T - 30	MIN
t_{AD}	–	(5/2 + N) T - 225	MAX
t_{RD}	–	(3/2 + N) T - 180	MAX
t_{RAE}	–	(1/2) T - 10	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T – 60	MIN
t_{WD}	–	(1/2) T - 60	MIN
t_{CC}	–	(3/2 + N) T - 80	MIN
t_{CL}	–	(1/2) T - 110	MIN
t_{ARY}	–	(3/2) T - 260	MAX
t_{HACK}	–	(1/2) T - 50	MIN
t_{HABF}	–	(1/2) T + 50	MAX
t_{HABE}	–	(1/2) T + 50	MAX
t_{AC}	–	(2/2) T - 50	MIN
t_1	–	(1/2) T - 80	MIN
t_2	–	(1/2) T - 40	MIN
t_{RV}	–	(3/2) T - 80	MIN
t_{LDR}	–	(4/2) T - 180	MAX

NOTE: N is equal to the total WAIT states.

$T = t_{CYC}$.

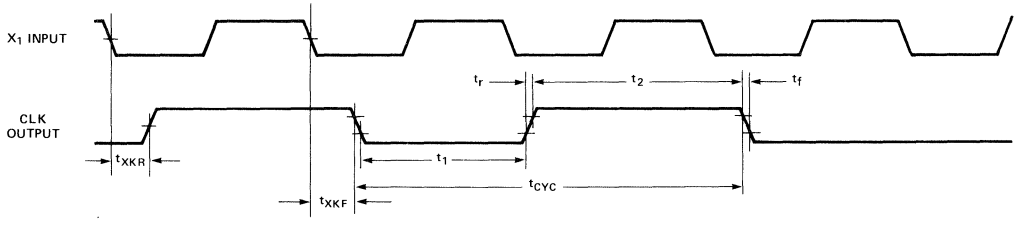
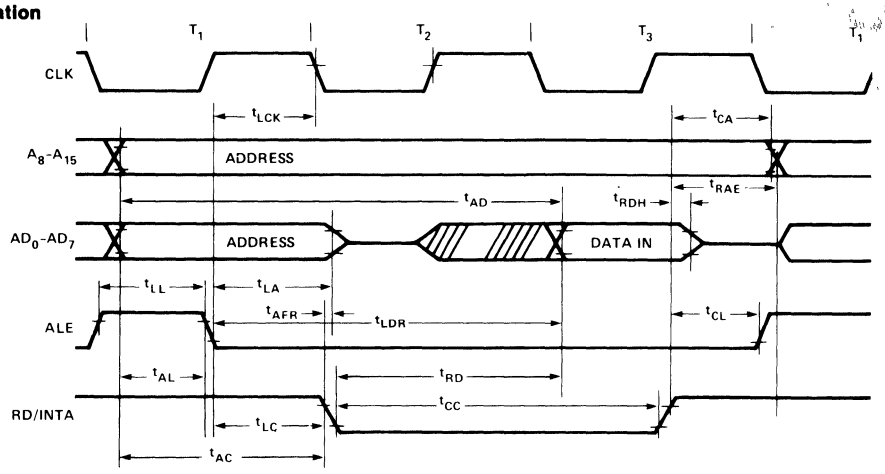
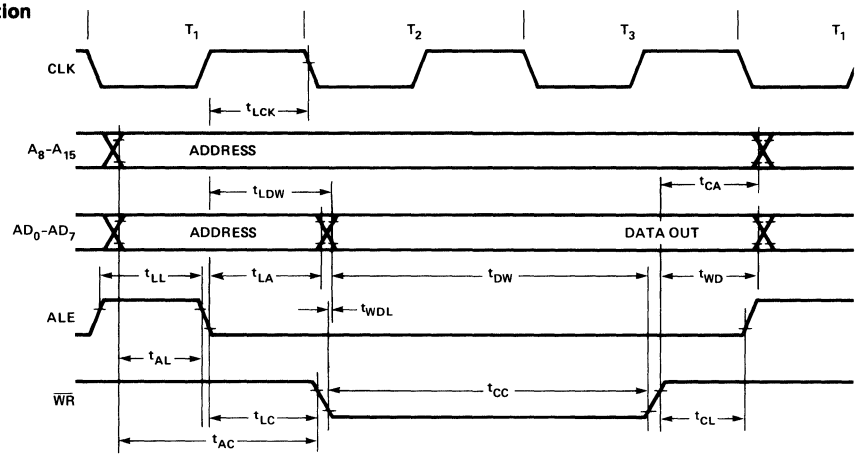


Figure 5. Clock Timing Waveform

Read Operation



Write Operation



Read operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation.

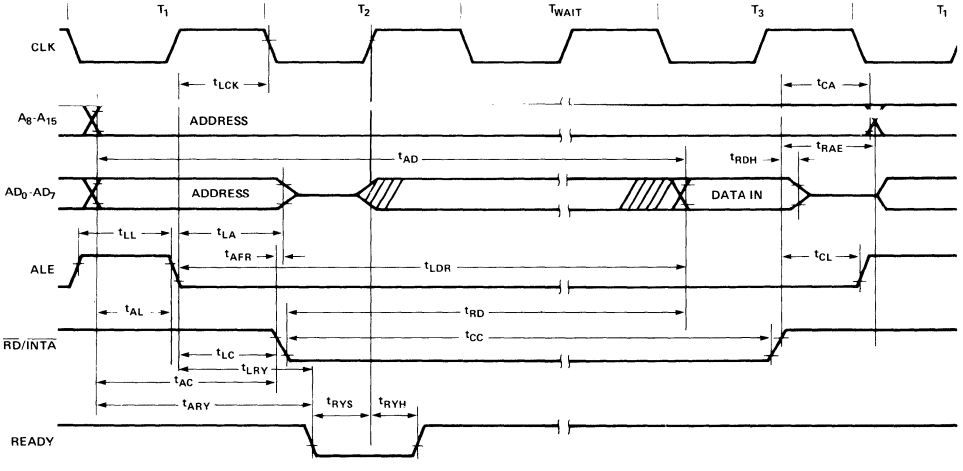


Figure 6. M8085A Bus Timing, With and Without Wait

Hold Operation

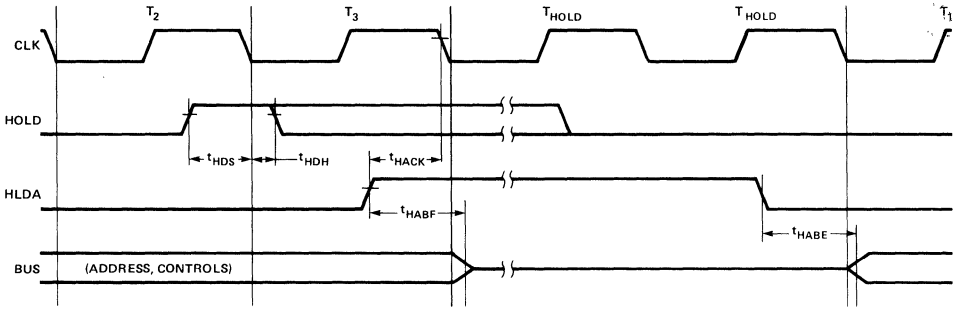


Figure 7. M8085A Hold Timing

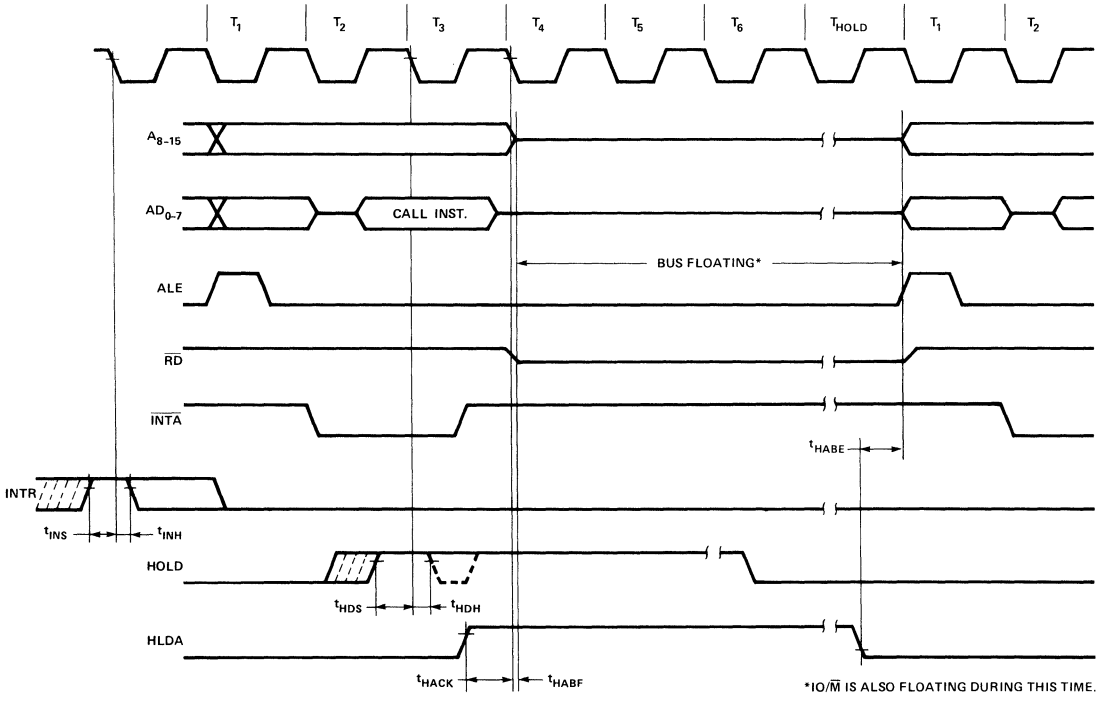


Figure 8. M8085A Interrupt and Hold Timing

TABLE 7. INSTRUCTION SET SUMMARY

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
MOVE, LOAD, AND STORE										
MOVr1 r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E H & L Registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
[illegible]	[illegible]	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
[illegible]	[illegible]	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4

TABLE 7. INSTRUCTION SUMMARY (Cont.)

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
NEW M8085A INSTRUCTIONS										
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4

NOTES 1 DDD or SSS B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111
2 Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags

M8155
2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

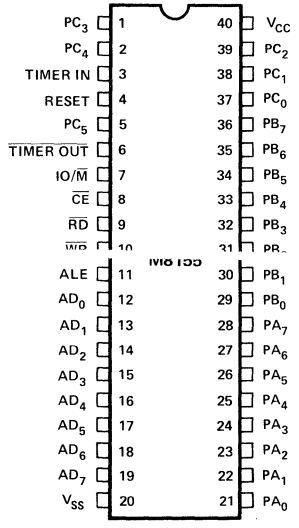
- **Military Temperature Range Operation (-55°C TO +125°C)**
- **256 Word x 8 Bits**
- **Single +5V Power Supply**
- **Completely Static Operation**
- **Internal Address Latch**
- **2 Programmable 8 Bit I/O Ports**
- **1 Programmable 6-Bit I/O Port**
- **Programmable 14-Bit Binary Counter/ Timer**
- **Multiplexed Address and Data Bus**
- **40 Pin DIP**

The M8155 is a RAM and I/O chip to be used in the MCS-85™ microcomputer system. The RAM portion is designed with 2048 static cells organized as 256 x 8. It has a maximum access time of 400 ns to permit use with no wait states in the 8085A CPU.

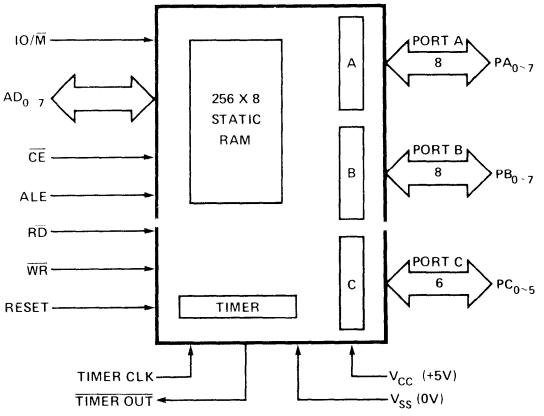
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



MILITARY

M8155 PIN FUNCTIONS

Symbol	Function
RESET (input)	Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times.
AD_{0-7} (input)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the M8155 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
$\overline{CE}$ (input)	Chip Enable: On the M8155, this pin is $\overline{CE}$ and is ACTIVE LOW.
$\overline{RD}$ (input)	Read control: Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/$\overline{M}$.
ALE (input)	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$ (input)	Selects memory if low and I/O and command/status registers if high.
PA_{0-7}(8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7}(8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5}(6) (input/output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — ABF (Port A Buffer Full) PC_2 — $\overline{A\ STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — $\overline{B\ BF}$ (Port B Buffer Full) PC_5 — B STB (Port B Strobe)
TIMER IN (input)	Input to the counter-timer.
$\overline{TIMER\ OUT}$ (output)	Timer output. This output can be either a square wave or a pulse depending on the timer mode.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

DESCRIPTION

The M8155 contains the following:

- 2k Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA_{0-7}, PB_{0-7}, PC_{0-5}) or the memory (RAM) portion. (See Figure 1.)

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

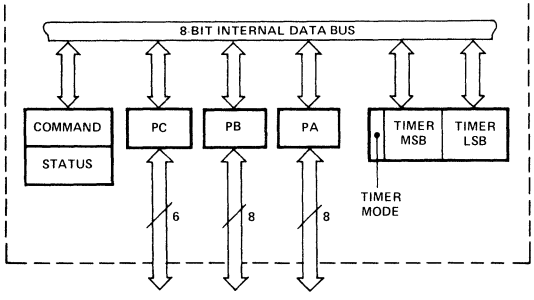


Figure 1. M8155 Internal Registers

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 2. The contents of the command register may never be read.

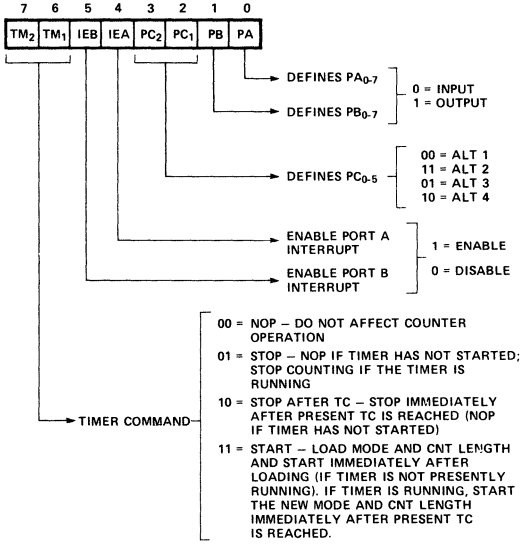


Figure 2. Command Register Bit Assignment

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 3. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

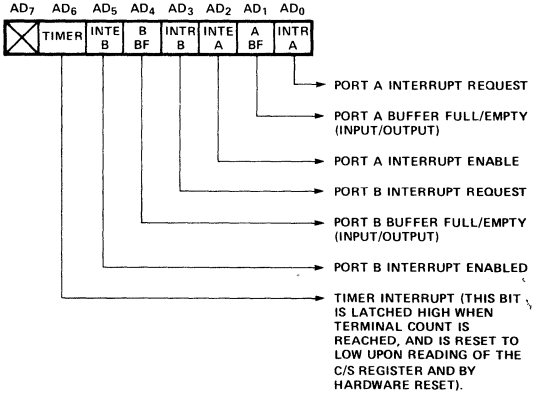


Figure 3. Status Register Bit Assignment

INPUT/OUTPUT SECTION

The I/O section of the M8155 consists of five registers: (See Figure 4.)

- **Command/Status Register (C/S)** — Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD_{0-7} lines.

- **PA Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

- **PB Register** — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.

- **PC Register** — This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

  When PC_{0-5} is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the M8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 1.)

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS†								SELECTION
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Interval Command/Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	Port C — General Purpose I/O or Control
X	X	X	X	X	1	0	0	Low-Order 8 bits of Timer Count
X	X	X	X	X	1	0	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X: Don't Care.
†: I/O Address must be qualified by $\overline{CE}$ = 0 (M8155) and IO/$\overline{M}$ = 1 in order to select the appropriate register.

Figure 4. I/O Port and Timer Addressing Scheme

Figure 5 shows how I/O PORTS A and B are structured within the M8155:

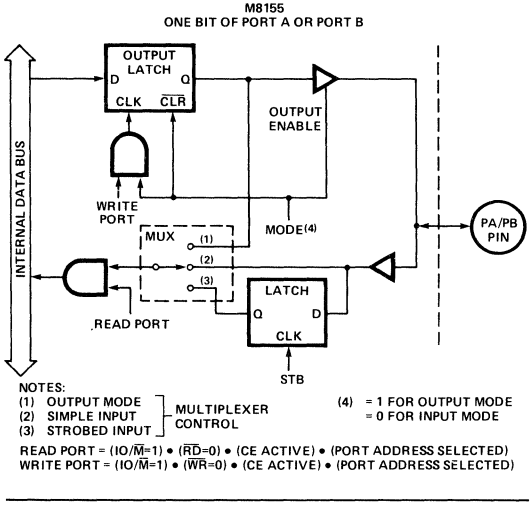


Figure 5. M8155 Port Functions

MILITARY

TABLE 1. TABLE OF PORT CONTROL ASSIGNMENT.

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A Strobe)	A $\overline{STB}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B Strobe)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the M8155 are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the M8155 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 6 shows how the M8155 I/O ports might be configured in a typical MCS-85 system.

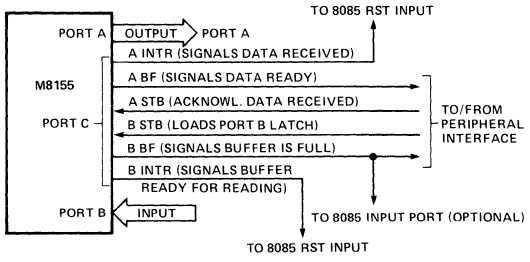


Figure 6. Example: Command Register = 00111001

TIMER SECTION

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 4).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 7). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0-13.

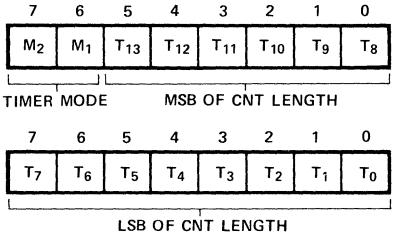


Figure 7. Timer Format

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 9.

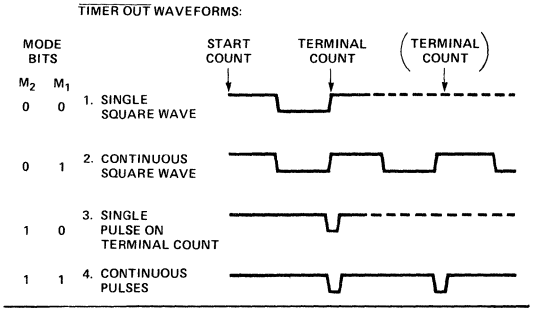


Figure 8. Timer Modes

Bits 6-7 (TM_2 and TM_1) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM_2	TM_1	
0	0	NOP — Do not affect counter operation.
0	1	STOP — NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 9.

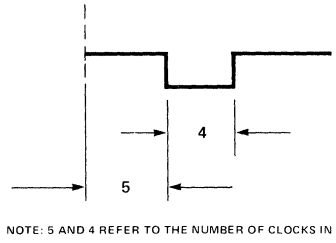


Figure 9. Asymmetrical Square-Wave Output Resulting from Count of 9

The counter in the M8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does *stop* the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the M8155 chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085A be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count — 1 if full count is odd).

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the M8155 always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = -55°C to +125°C; V_{CC} = 5V ±10%)

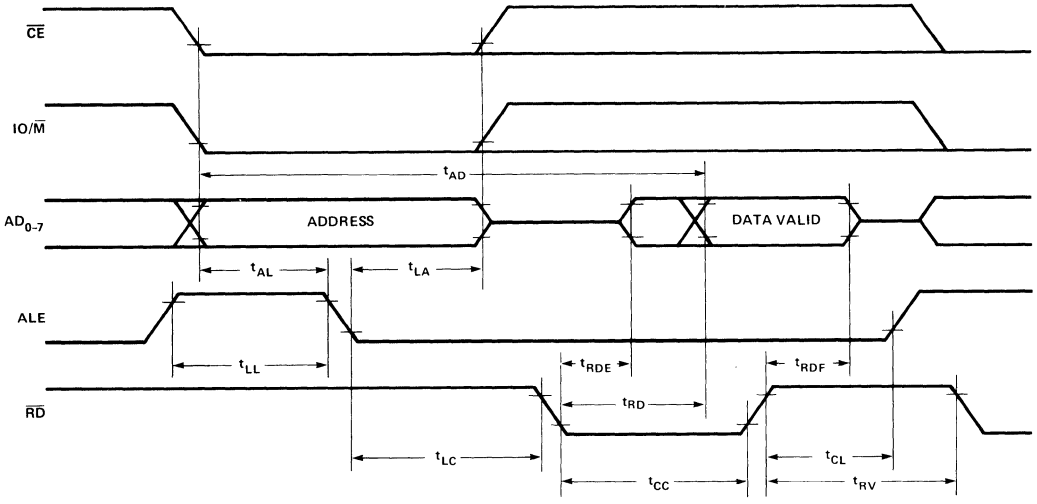
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	
I_{IL}(CE)	Chip Enable Leakage M8155		+100	μA	V_{IN} = V_{CC} to 0V

A.C. CHARACTERISTICS (T_A = -55°C to +125°C; V_{CC} = 5V ±10%)

		M8155		
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
t_{AL}	Address to Latch Set Up Time	50		ns
t_{LA}	Address Hold Time after Latch	80		ns
t_{LC}	Latch to READ/WRITE Control	100		ns
t_{RD}	Valid Data Out Delay from READ Control		170	ns
t_{AD}	Address Stable to Data Out Valid		400	ns
t_{LL}	Latch Enable Width	100		ns
t_{RDF}	Data Bus Float After READ	0	100	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		ns
t_{CC}	READ/WRITE Control Width	250		ns
t_{DW}	Data In to WRITE Set Up Time	150		ns
t_{WD}	Data In Hold Time After WRITE	0		ns
t_{RV}	Recovery Time Between Controls	300		ns
t_{WP}	WRITE to Port Output		400	ns
t_{PR}	Port Input Setup Time	70		ns
t_{RP}	Port Input Hold Time	50		ns
t_{SBF}	Strobe to Buffer Full		400	ns
t_{SS}	Strobe Width	200		ns
t_{RBE}	READ to Buffer Empty		400	ns
t_{SI}	Strobe to INTR On		400	ns
t_{RDI}	READ to INTR Off		400	ns
t_{PSS}	Port Setup Time to Strobe Strobe	50		ns
t_{PHS}	Port Hold Time After Strobe	120		ns
t_{SBE}	Strobe to Buffer Empty		400	ns
t_{WBF}	WRITE to Buffer Full		400	ns
t_{WI}	WRITE to INTR Off		400	ns
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low		400	ns
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High		400	ns
t_{RDE}	Data Bus Enable from READ Control	10		ns
t_1	TIMER-IN Low Time	80		ns
t_2	TIMER-IN High Time	120		ns

WAVEFORMS

a. Read Cycle



b. Write Cycle

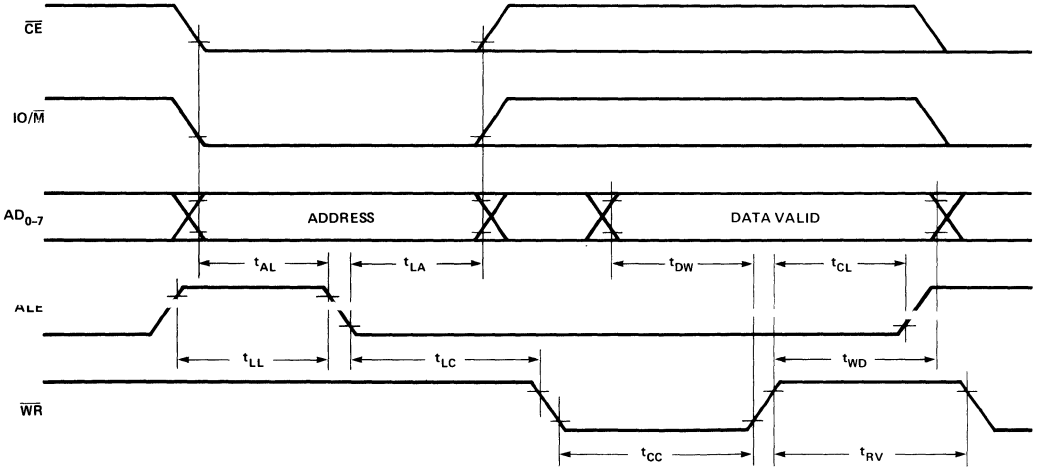
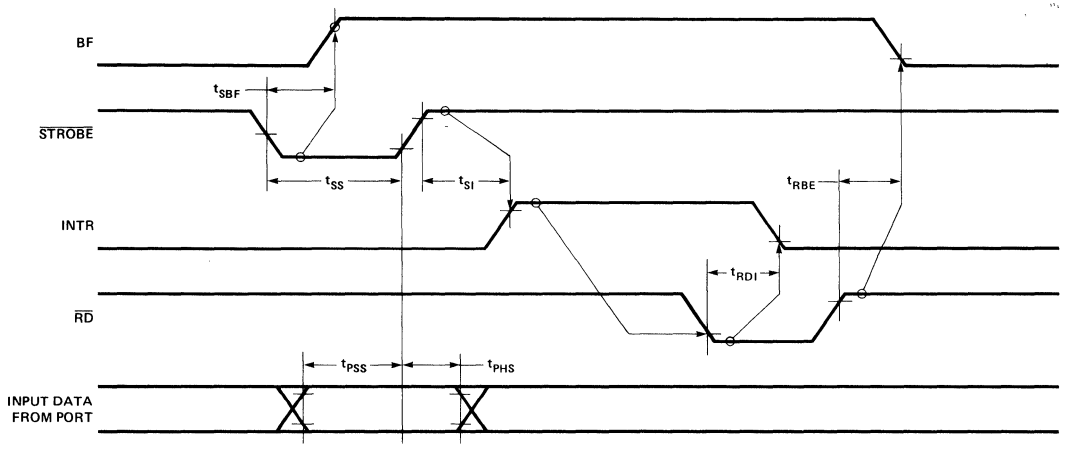


Figure 10. M8155 Read/Write Timing Diagrams

a. Strobed Input Mode



b. Strobed Output Mode

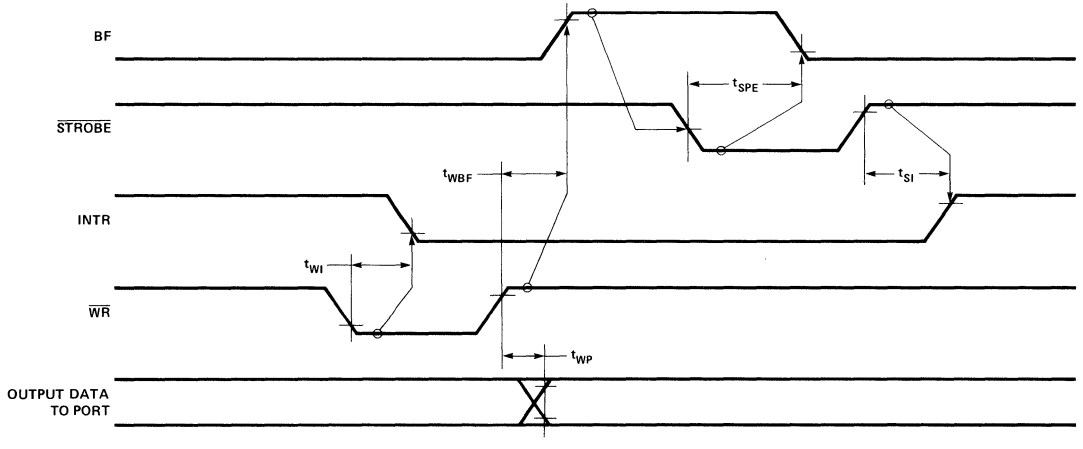
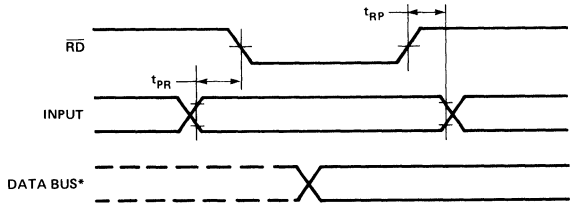
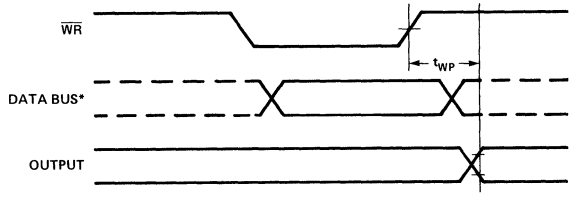


Figure 11. Strobed I/O Timing

a. Basic Input Mode

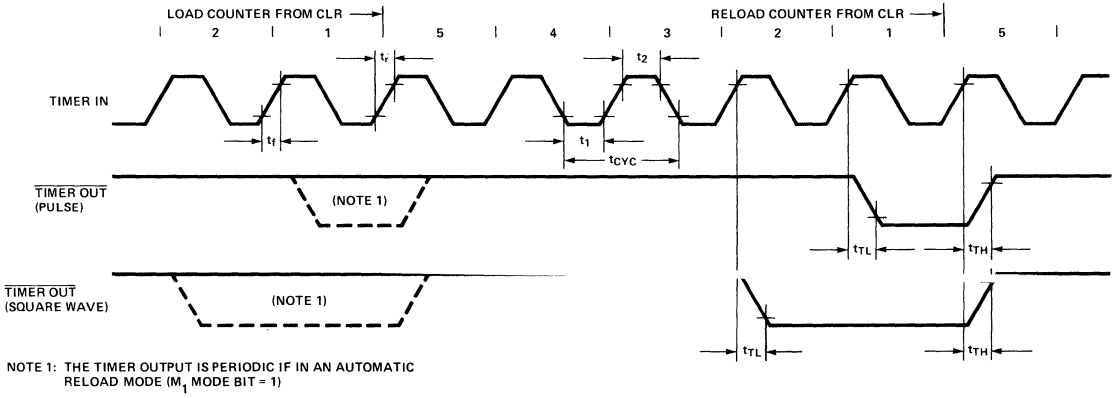


b. Basic Output Mode



*DATA BUS TIMING IS SHOWN IN FIGURE 7.

Figure 12. Basic I/O Timing Wavefore



NOTE 1: THE TIMER OUTPUT IS PERIODIC IF IN AN AUTOMATIC RELOAD MODE (M_1 MODE BIT = 1)

Figure 13. Timer Output Waveform Countdown from 5 to 1

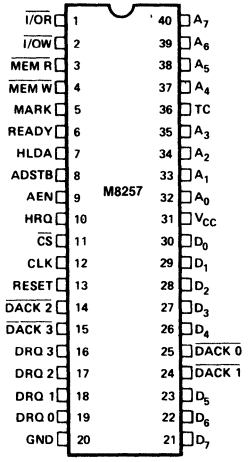
MILITARY

M8257
PROGRAMMABLE DMA CONTROLLER

- **Full Military Temp. Range −55°C to 125°C**
- **4-Channel DMA Controller**
- **Priority DMA Request Logic**
- **Channel Inhibit Logic**
- **Terminal Count and Modulo 128 Outputs**
- **Single TTL Clock**
- **Single +5V Supply**
- **Auto Load Mode**

The Intel® M8257 is a 4-channel direct memory access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel® microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus in accomplished via the CPU's hold function. The M8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers. The M8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

PIN CONFIGURATION

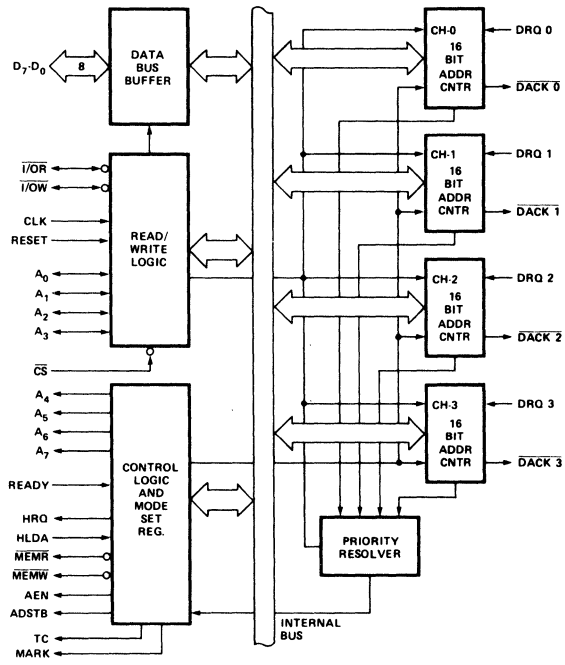


PIN NAMES

D_7-D_0	DATA BUS
A_7-A_0	ADDRESS BUS
$\overline{I/OR}$	I/O READ
$\overline{I/OW}$	I/O WRITE
$\overline{MEMR}$	MEMORY READ
$\overline{MEMW}$	MEMORY WRITE
CLK	CLOCK INPUT
RESET	RESET INPUT
READY	READY
HRQ	HOLD REQUEST (TO 8080A)
HLDA	HOLD ACKNOWLEDGE (FROM 8080A)

AEN	ADDRESS ENABLE
ADSTB	ADDRESS STROBE
TC	TERMINAL COUNT
MARK	MODULO 128 MARK
DRQ_3-DRQ_0	DMA REQUEST INPUT
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA ACKNOWLEDGE OUT
$\overline{CS}$	CHIP SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM



MILITARY

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . – 55°C to 125°C
Storage Temperature . . . . . – 65°C to + 150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = -55°C$ to $125°C$, $V_{CC} = +5V \pm 10\%$, GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.2	V_{CC}+.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	Volts	I_{OH}=-150μA for AB, DB and AEN I_{OH}=-80μA for others
V_{HH}	HRQ Output High Voltage	3.3	V_{CC}	Volts	I_{OH} = -80μA
I_{CC}	V_{CC} Current Drain		120	mA	
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Leakage During Float		±10	μA	V_{OUT} = V_{CC} to 0V

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS: PERIPHERAL (SLAVE) MODE

$T_A = -55°C$ to $125°C$, $V_{CC} = 5.0V \pm 10\%$; GND = 0V (Note 1).

8080 Bus Parameters

Read Cycle:

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
T_{AR}	Adr or $\overline{CS}\downarrow$ Setup to $\overline{RD}\downarrow$	0		ns	
T_{RA}	Adr or $\overline{CS}\uparrow$ Hold from $\overline{RD}\uparrow$	0		ns	
T_{RD}	Data Access from $\overline{RD}\downarrow$	0	300	ns	(Note 2)
T_{DF}	DB→Float Delay from $\overline{RD}\uparrow$	20	150	ns	
T_{RR}	$\overline{RD}$ Width	250		ns	

Write Cycle:

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
T_{AW}	Adr Setup to $\overline{WR}\downarrow$	20		ns	
T_{WA}	Adr Hold from $\overline{WR}\uparrow$	35		ns	
T_{DW}	Data Setup to $\overline{WR}\uparrow$	200		ns	
T_{WD}	Data Hold from $\overline{WR}\uparrow$	0		ns	
T_{WW}	$\overline{WR}$ Width	175		ns	

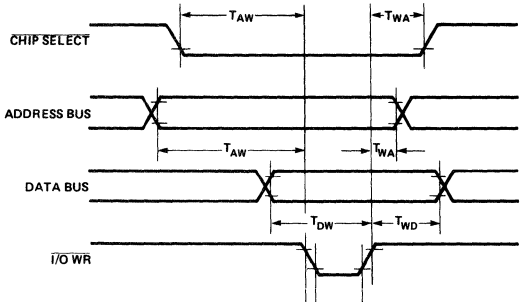
Other Timing:

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
T_{RSTW}	Reset Pulse Width	300		ns	
T_{RSTD}	Power Supply↑ (V_{CC}) Setup to Reset↓	500		μs	
T_r	Signal Rise Time		20	ns	
T_f	Signal Fall Time		20	ns	
T_{RSTS}	Reset to First $\overline{I/O}\overline{WR}$	2		t_{CY}	

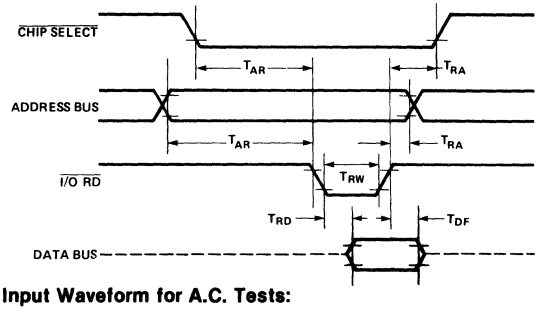
Notes: 1. All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V
Output "1" at 2.0V, "0" at 0.8V
2. M8257: $C_L = 100$ pF, 8257-5: $C_L = 150$ pF.

M8257 PERIPHERAL MODE TIMING DIAGRAMS

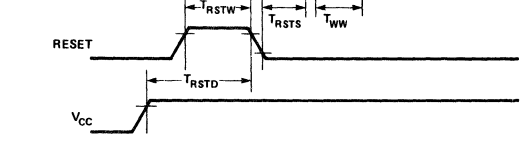
Write Timing:



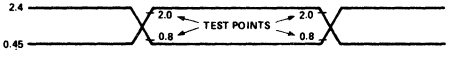
Read Timing:



Reset Timing:



Input Waveform for A.C. Tests:



MILITARY

A.C. CHARACTERISTICS: DMA (MASTER) MODE

$T_A = -55°C$ to $125°C$, $V_{CC} = +5V \pm 10\%$, GND = 0V

Timing Requirements

Symbol	Parameter	Min.	Max.	Unit
T_{CY}	Cycle Time (Period)	0.320	4	μs
T_θ	Clock Active (High)	120	$.8T_{CY}$	ns
T_{QS}	DRQ↑ Setup to θ↓ (SI, S4)	120		ns
T_{QH}	DRQ↓ Hold from HLDA↑[4]	0		ns
T_{HS}	HLDA↑ or ↓Setup to θ↓ (SI, S4)	100		ns
T_{RS}	READY Setup Time to θ↑ (S3, Sw)	30		ns
T_{RH}	READY Hold Time from θ↑ (S3, Sw)	20		ns

Note: 4. Tracking Parameter.

Tracking Parameters

Signals labeled as Tracking Parameters (footnotes 4-7 under A.C. Specifications) are signals that follow similar paths through the silicon die. The propagation speed of these signals varies in the manufacturing process but the relationship between all these parameters is constant. The variation is less than or equal to 50 ns.

Suppose the following timing equation is being evaluated,

$$T_{A(MIN)} + T_{B(MAX)} \leq 150 \text{ ns}$$

and only minimum specifications exist for T_A and T_B. If $T_{A(MIN)}$ is used, and if T_A and T_B are tracking parameters, $T_{B(MAX)}$ can be taken as $T_{B(MIN)} + 50$ ns.

$$T_{A(MIN)} + (T_{B(MIN)}^* + 50 \text{ ns}) \leq 150 \text{ ns}$$

*if T_A and T_B are tracking parameters

A.C. CHARACTERISTICS: DMA (MASTER) MODE

$T_A = -55°C$ to $125°C$, $V_{CC} = +5V \pm 10\%$, GND = 0V

Timing Responses

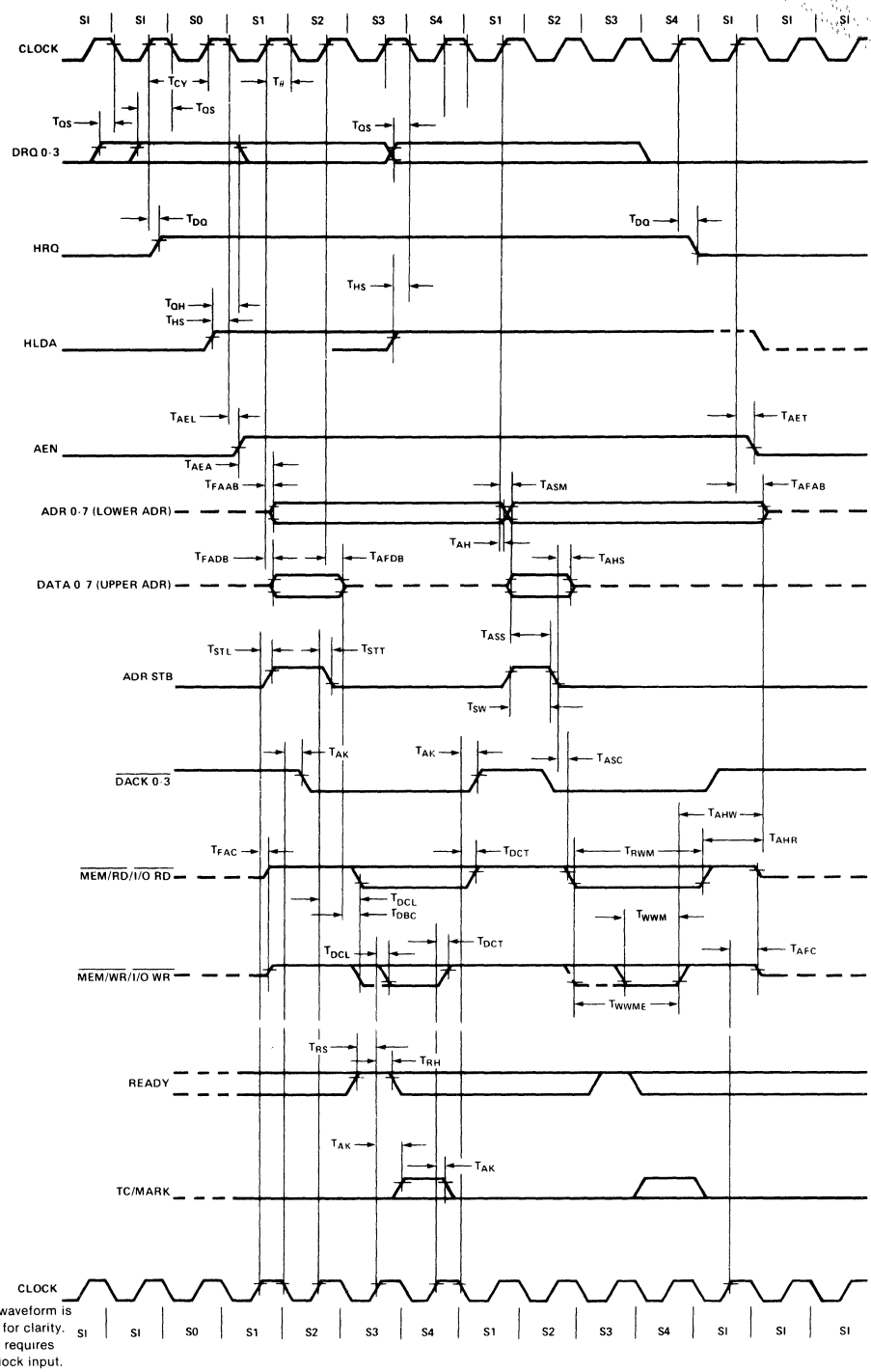
Symbol	Parameter	Min.	Max.	Unit
T_{DQ}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 2.0V)[1]		180	ns
T_{DQ1}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 3.3V)[3]		270	ns
T_{AEL}	AEN↑ Delay from θ↓(S1)[1]		300	ns
T_{AET}	AEN↓ Delay from θ↑(SI)[1]		200	ns
T_{AEA}	Adr(AB)(Active) Delay from AEN↑(S1)[4]	20		ns
T_{FAAB}	Adr(AB)(Active) Delay from θ↑(S1)[2]		270	ns
T_{AFAB}	Adr(AB)(Float) Delay from θ↑(SI)[2]		200	ns
T_{ASM}	Adr(AB)(Stable) Delay from θ↑(S1)[2]		250	ns
T_{AH}	Adr(AB)(Stable) Hold from θ↑(S1)[2]	$T_{ASM} - 50$		ns
T_{AHR}	Adr(AB)(Valid) Hold from $\overline{Rd}$↑(S1, SI)[4]	60		ns
T_{AHW}	Adr(AB)(Valid) Hold from $\overline{Wr}$↑(S1, SI)[4]	300		ns
T_{FADB}	Adr(DB)(Active) Delay from θ↑(S1)[2]		300	ns
T_{AFDB}	Adr(DB)(Float) Delay from θ↑(S2)[2]	$T_{STT} + 20$	250	ns
T_{ASS}	Adr(DB) Setup to AdrStb↓(S1-S2)[4]	100		ns
T_{AHS}	Adr(DB)(Valid) Hold from AdrStb↓(S2)[4]	50		ns
T_{STL}	AdrStb↑ Delay from θ↑(S1)[1]		200	ns
T_{STT}	AdrStb↓Delay from θ↑(S2)[1]		160	ns
T_{SW}	AdrStb Width (S1-S2)[4]	$T_{CY} - 100$		ns
T_{ASC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from AdrStb↓(S2)[4]	70		ns
T_{DBC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from Adr(DB) (Float)(S2)[4]	20		ns
T_{AK}	DACK↑ or ↓Delay from θ↓(S2, S1) and TC/Mark↑ Delay from θ↑(S3) and TC/Mark↓ Delay from θ↑(S4)[1,5]		270	ns
T_{DCL}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from θ↑(S2) and $\overline{Wr}$↓ Delay from θ↑(S3)[2,6]		250	ns
T_{DCT}	$\overline{Rd}$↑ Delay from θ↓(S1, SI) and $\overline{Wr}$↑ Delay from θ↑(S4)[2,7]		200	ns
T_{FAC}	$\overline{Rd}$ or $\overline{Wr}$(Active) from θ↑(S1)[2]		300	ns
T_{AFC}	$\overline{Rd}$ or $\overline{Wr}$(Float) from θ↑(SI)[2]		170	ns
T_{RWM}	$\overline{Rd}$ Width (S2-S1 or SI)[4]	$2T_{CY} + T_\theta - 50$		ns
T_{WWM}	$\overline{Wr}$ Width (S3-S4)[4]	$T_{CY} - 50$		ns
T_{WWME}	$\overline{Wr}$(Ext) Width (S2-S4)[4]	$2T_{CY} - 50$		ns

Notes: 1. Load = 1 TTL. 2. Load = 1 TTL + 50 pF. 3. Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V. 4. Tracking Parameter. 5. $\Delta T_{AK} < 50$ ns. 6. $\Delta T_{DCL} < 50$ ns. 7. $\Delta T_{DCT} < 50$ ns.

MILITARY

DMA MODE WAVEFORMS

CONSECUTIVE CYCLES AND BURST MODE SEQUENCE



NOTE: The clock waveform is duplicated for clarity. The M8257 requires only one clock input.

Figure 12. Consecutive Cycles and Burst Mode Sequence

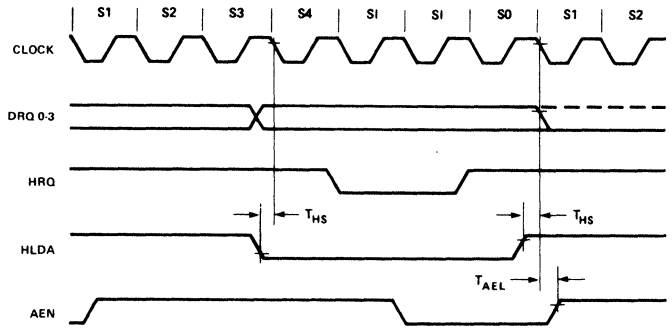


Figure 13. Control Override Sequence

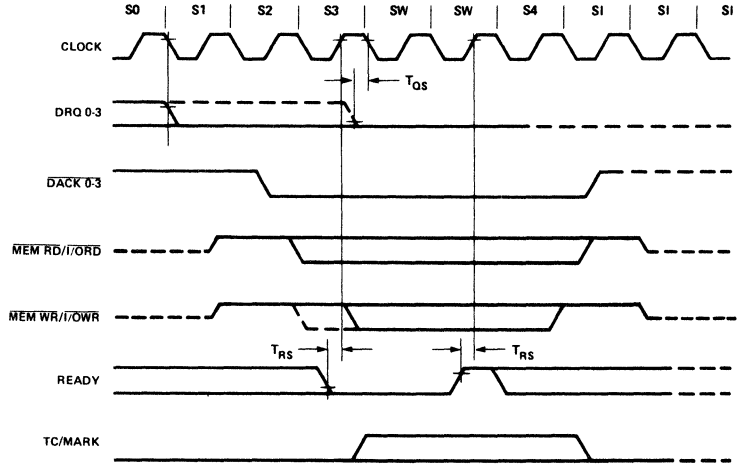


Figure 14. Not Ready Sequence

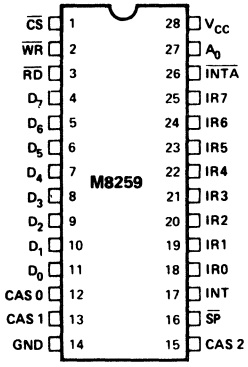
M8259
PROGRAMMABLE INTERRUPT CONTROLLER

- **Full Military Temperature Range −55°C to +125°C**
- **Eight Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes**
- **Individual Request Mask Capability**
- **Single +5V Supply (No Clocks)**
- **28-Pin Dual-In-Line Package**
- **Fully Compatible with Intel CPUs**

The M8259 handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts, without additional circuitry. It will be packaged in a 28-pin plastic DIP, uses nMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The M8259 is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

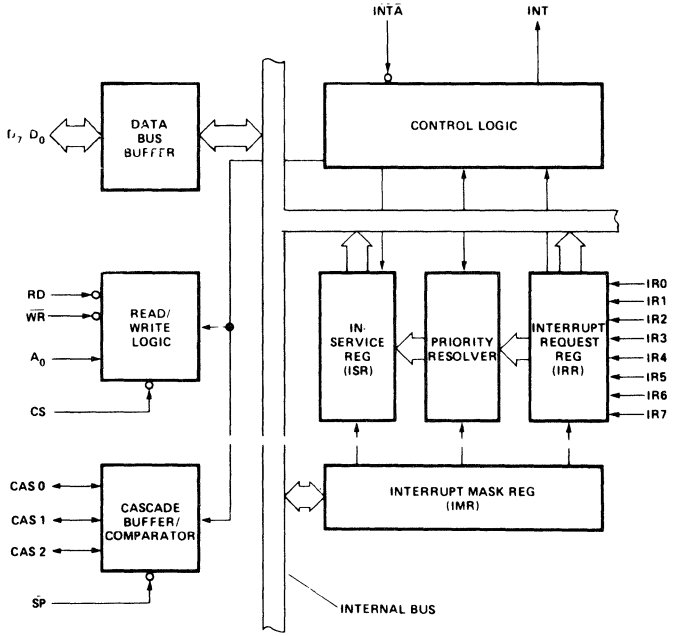
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS1-CAS0	CASCADE LINES
$\overline{SP}$	SLAVE PROGRAM INPUT
INT	INTERRUPT OUTPUT
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE INPUT
IR0-IR7	INTERRUPT REQUEST INPUTS

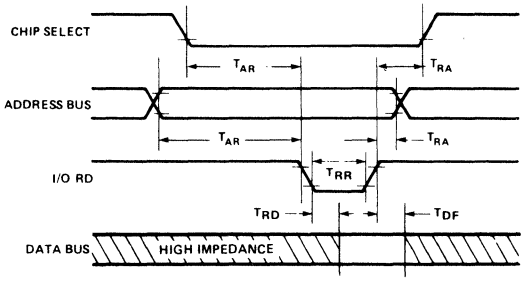
BLOCK DIAGRAM



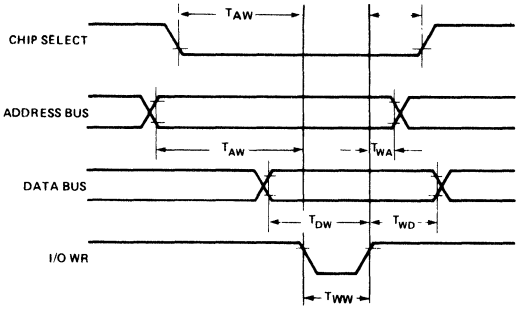
MILITARY

WAVEFORMS

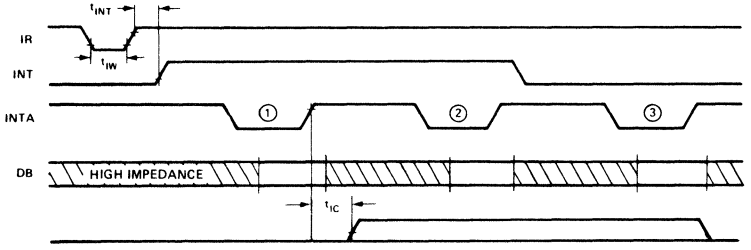
READ TIMING



WRITE TIMING



OTHER TIMING



NOTE: INTERRUPT REQUEST MUST REMAIN "HIGH" (AT LEAST) UNTIL LEADING EDGE OF FIRST INTA.

MILITARY

A.C. CHARACTERISTICS $T_A = -55°C$ to $+125°C$; $V_{CC} = +5V \pm 10\%$ GND = 0V

BUS PARAMETERS

Read

Symbol	Parameter	Min.	Max.	Unit
t_{AR}	$\overline{CS}/A_0$ Stable Before $\overline{RD}$ or $\overline{INTA}$	50		ns
t_{RA}	$\overline{CS}/A_0$ Stable After $\overline{RD}$ or $\overline{INTA}$	5		ns
t_{RR}	$\overline{RD}$ Pulse Width	420		ns
t_{RD}	Data Valid From $\overline{RD}/\overline{INTA}$[1]		360	ns
t_{DF}	Data Float After $\overline{RD}/\overline{INTA}$	20	200	ns

Write

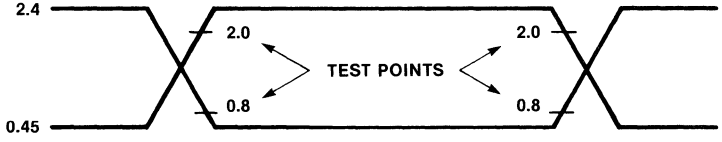
Symbol	Parameter	Min.	Max.	Unit
t_{AW}	A_0 Stable Before $\overline{WR}$	50		ns
t_{WA}	A_0 Stable After $\overline{WR}$	20		ns
t_{WW}	$\overline{WR}$ Pulse Width	420		ns
t_{DW}	Data Valid to $\overline{WR}$ (T.E.)	300		ns
t_{WD}	Data Valid After $\overline{WR}$	40		ns

Other Timings

Symbol	Parameter	Min.	Max.	Unit
t_{IW}	Width of Interrupt Request Pulse	100		ns
t_{INT}	INT↑ After IR↑	400		ns
t_{IC}	Cascade Line Stable After $\overline{INTA}$↑	400		ns

Note 1: $C_L = 100$ pF.

INPUT WAVEFORMS FOR A.C. TESTS



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . – 55°C to + 125°C
Storage Temperature . . . . . – 65°C to + 150°C
Voltage On Any Pin With Respect to Ground . . . . . – 0.5V to + 7V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS $T_A = -55°C$ to $+125°C$; $V_{CC} = 5V \pm 10\%$

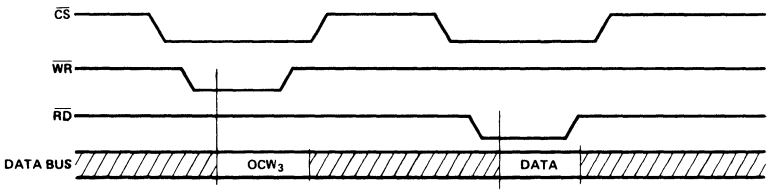
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	– 0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu A$
V_{OH-INT}	Interrupt Output High Voltage	2.4 3.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -50\ \mu A$
$I_{IL(IR_{0-7})}$	Input Leakage Current for IR_{0-7}		– 300 10	μA μA	$V_{IN} = 0V$ $V_{IN} = V_{CC}$
I_{IL}	Input Leakage Current for Other Inputs		10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		± 10	μA	$V_{OUT} = 0.45V$ to V_{CC}
I_{CC}	V_{CC} Supply Current		100	mA	

CAPACITANCE $T_A = 25°C$; $V_{CC} = GND = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

MILITARY

Read Status/Poll Mode



M8048/M8748/M8035

SINGLE COMPONENT 8-BIT MICROCOMPUTER

***8048 Mask Programmable ROM**
***8748 User Programmable/Erasable EPROM**
***8035 External ROM or EPROM**

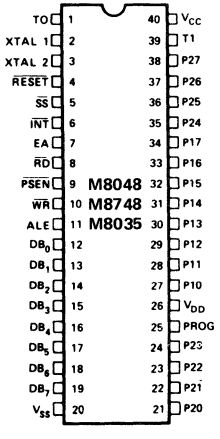
- **-55°C to +125°C Operation (M8048/M8035L)**
- **-55°C to +100°C Operation (M8748/M8035)**
- **8-Bit CPU, ROM, RAM, I/O in Single Package**
- **Interchangeable ROM and EPROM Versions**
- **Single 5V Supply**
- **2.5 µsec and 5.0 µsec Cycle Versions All Instructions 1 or 2 Cycles.**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 ROM/EPROM 64 x 8 RAM 27 I/O Lines**
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Single Level Interrupt**

The Intel® M8048/M8748/M8035/M8035L is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

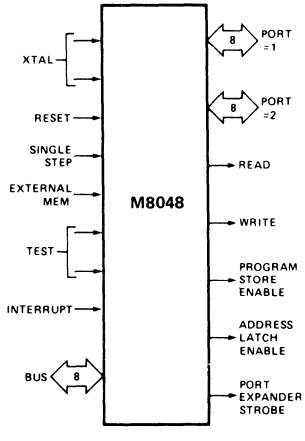
The M8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability, the M8048 can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The M8035 is the equivalent of an M8048 without program memory. The M8035L has the RAM power down mode of the M8048 while the M8035 does not. To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible* versions of this single component microcomputer exist: the M8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the M8048 with factory-programmed mask ROM program memory for low cost, high volume production, and the M8035 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The M8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

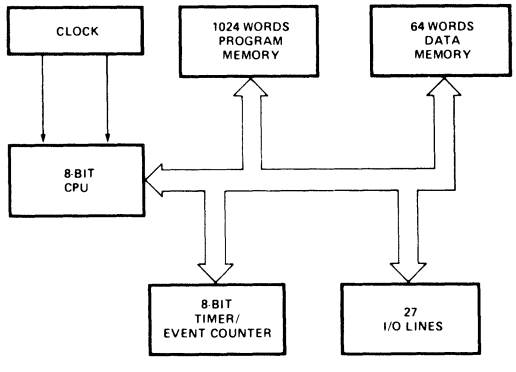
PIN CONFIGURATION



LOGIC SYMBOL

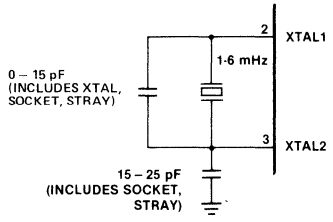


BLOCK DIAGRAM



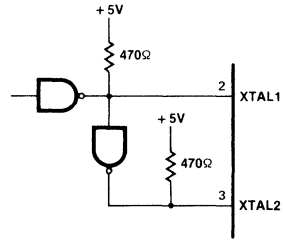
MILITARY

CRYSTAL OSCILLATOR MODE



CRYSTAL SERIES RESISTANCE SHOULD BE <75Ω AT 6 MHz, <180Ω AT 3.6 MHz.

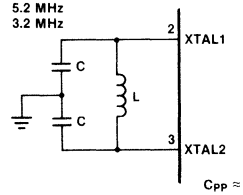
DRIVING FROM EXTERNAL SOURCE



BOTH X1 AND X2 SHOULD BE DRIVEN.
RESISTORS TO V_{CC} ARE NEEDED TO ENSURE V_{IH} = 3.8V IF TTL CIRCUITRY IS USED. THE MINIMUM HIGH AND THE MINIMUM LOW TIMES ARE 45%.

LC OSCILLATOR MODE

L	C	NOMINAL f
45 μH	20 pF	5.2 MHz
120 μH	20 pF	3.2 MHz



$$f \approx \frac{1}{2\pi\sqrt{LC'}}$$

$$C' = \frac{C + 3C_{PP}}{2}$$

$C_{PP} \approx 5 – 10$ pF PIN-TO-PIN CAPACITANCE

EACH C SHOULD BE APPROXIMATELY 20 pF, INCLUDING STRAY CAPACITANCE.

PROGRAMMING, VERIFYING, AND ERASING THE 8748 EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock Input (1 to 6MHz)
$\overline{\text{Reset}}$	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input Data Output During Verify
P20-1	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING:

An attempt to program a missocketed 8748 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. V_{DD} = 5v, Clock applied or internal oscillator operating, $\overline{\text{RESET}}$ = 0v, TEST 0 = 5v, EA = 5v, BUS and PROG floating.
2. Insert 8748 in programming socket
3. TEST 0 = 0v (select program mode)
4. EA = 23V (activate program mode)
5. Address applied to BUS and P20-1
6. $\overline{\text{RESET}}$ = 5v (latch address)
7. Data applied to BUS
8. V_{DD} = 25v (programming power)
9. PROG = 0v followed by one 50ms pulse to 23V
10. V_{DD} = 5v
11. TEST 0 = 5v (verify mode)
12. Read and verify data on BUS
13. TEST 0 = 0v
14. $\overline{\text{RESET}}$ = 0v and repeat from step 5
15. Programmer should be at conditions of step 1 when 8748 is removed from socket.

MILITARY

AC TIMING SPECIFICATION FOR PROGRAMMING

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 25V \pm 1V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Setup Time to $\overline{RESET}$ ↑	4tcy			
t_{WA}	Address Hold Time After $\overline{RESET}$ ↑	4tcy			
t_{DW}	Data in Setup Time to PROG ↑	4tcy			
t_{WD}	Data in Hold Time After PROG ↓	4tcy			
t_{PH}	$\overline{RESET}$ Hold Time to Verify	4tcy			
t_{VDDW}	V_{DD}	4tcy			
t_{VDDH}	V_{DD} Hold Time After PROG ↓	0			
t_{PW}	Program Pulse Width	50	60	mS	
t_{TW}	Test 0 Setup Time for Program Mode	4tcy			
t_{WT}	Test 0 Hold Time After Program Mode	4tcy			
t_{DO}	Test 0 to Data Out Delay		4tcy		
t_{WW}	$\overline{RESET}$ Pulse Width to Latch Address	4tcy			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	5.0		μs	
t_{RE}	$\overline{RESET}$ Setup Time Before EA ↑	4tcy			

Note: If Test 0 is high t_{DO} can be triggered by $\overline{RESET}$ ↑.

DC SPECIFICATION FOR PROGRAMMING

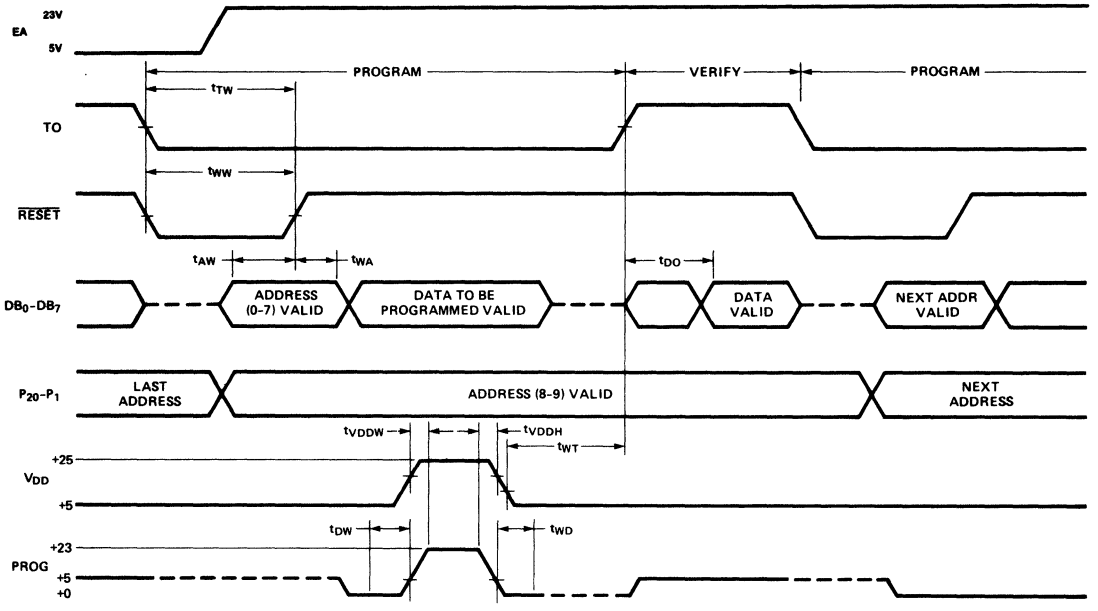
$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 25V \pm 1V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DOH}	V_{DD} Program Voltage High Level	24.0	26.0	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	21.5	24.5	V	
V_{PL}	PROG Voltage Low Level		0.2	V	
V_{EAH}	EA Program or Verify Voltage High Level	21.5	24.5	V	8748
V_{EAH1}	EA1 Verify Voltage High Level	11.4	12.6	V	8048
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		16.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

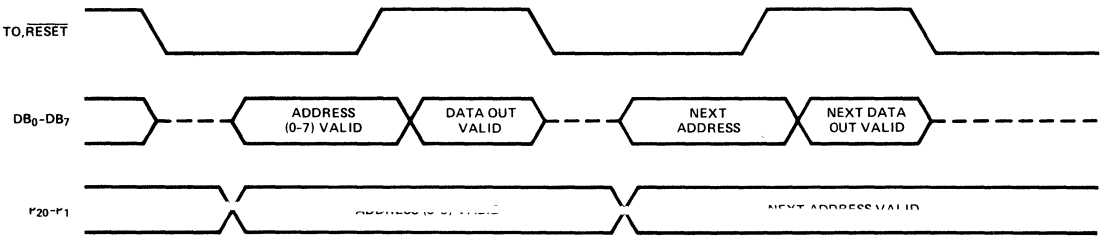
MILITARY

WAVEFORMS FOR PROGRAMMING

COMBINATION PROGRAM/VERIFY MODE (EPROM'S ONLY)



VERIFY MODE (ROM/EPROM)



NOTES:
1. PROG MUST FLOAT IF EA IS LOW (i.e., ≠23V), OR IF T0 = 5V FOR THE 8748. FOR THE 8048 PROG MUST ALWAYS FLOAT.
2. X_1 AND X_2 DRIVEN BY 3 MHz CLOCK WILL GIVE 5μsec t_{CY}. THIS IS ACCEPTABLE FOR ALL PARTS.

The 8748 EPROM can be programmed by either of two Intel products:

1. PROMPT-48 Microcomputer Design Aid, or
2. Universal PROM Programmer (UPP Series) peripheral of the Intellec® Development System with a UPP-848 Personality Card.

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle
Accumulator	ADD A, R	Add register to A	1	1
	ADD A, @R	Add data memory to A	1	1
	ADD A, #data	Add immediate to A	2	2
	ADDC A, R	Add register with carry	1	1
	ADDC A, @R	Add data memory with carry	1	1
	ADDC A, #data	Add immediate with carry	2	2
	ANL A, R	And register to A	1	1
	ANL A, @R	And data memory to A	1	1
	ANL A, #data	And immediate to A	2	2
	ORL A, R	Or register to A	1	1
	ORL A, @R	Or data memory to A	1	1
	ORL A, #data	Or immediate to A	2	2
	XRL A, R	Exclusive or register to A	1	1
	XRL A, @R	Exclusive or data memory to A	1	1
	XRL A, #data	Exclusive or immediate to A	2	2
	INC A	Increment A	1	1
	DEC A	Decrement A	1	1
	CLR A	Clear A	1	1
	CPL A	Complement A	1	1
	DA A	Decimal adjust A	1	1
	SWAP A	Swap nibbles of A	1	1
	RL A	Rotate A left	1	1
	RLC A	Rotate A left through carry	1	1
	RR A	Rotate A right	1	1
	RRC A	Rotate A right through carry	1	1
Input/Output	IN A, P	Input port to A	1	2
	OUTL P, A	Output A to port	1	2
	ANL P, #data	And immediate to port	2	2
	ORL P, #data	Or immediate to port	2	2
	INS A, BUS	Input BUS to A	1	2
	OUTL BUS, A	Output A to BUS	1	2
	ANL BUS, #data	And immediate to BUS	2	2
	ORL BUS, #data	Or immediate to BUS	2	2
	MOVD A, P	Input expander port to A	1	2
	MOVD P, A	Output A to expander port	1	2
	ANLD P, A	And A to expander port	1	2
	ORLD P, A	Or A to expander port	1	2
Registers	INC R	Increment register	1	1
	INC @R	Increment data memory	1	1
	DEC R	Decrement register	1	1
Branch	JMP addr	Jump unconditional	2	2
	JMPP @A	Jump indirect	1	2
	DJNZ R, addr	Decrement register and skip	2	2
	JC addr	Jump on carry = 1	2	2
	JNC addr	Jump on carry = 0	2	2
	JZ addr	Jump on A zero	2	2
	JNZ addr	Jump on A not zero	2	2
	JT0 addr	Jump on T0 = 1	2	2
	JNT0 addr	Jump on T0 = 0	2	2
	JT1 addr	Jump on T1 = 1	2	2
	JNT1 addr	Jump on T1 = 0	2	2
	JF0 addr	Jump on F0 = 1	2	2
	JF1 addr	Jump on F1 = 1	2	2
	JTF addr	Jump on timer flag	2	2
	JNI addr	Jump on $\overline{INT}$ = 0	2	2
	JBb addr	Jump on accumulator bit	2	2

	Mnemonic	Description	Bytes	Cycles
Subroutine	CALL	Jump to subroutine	2	2
	RET	Return	1	2
	RETR	Return and restore status	1	2
Flags	CLR C	Clear carry	1	1
	CPL C	Complement carry	1	1
	CLR F0	Clear flag 0	1	1
	CPL F0	Complement flag 0	1	1
	CLR F1	Clear flag 1	1	1
	CPL F1	Complement flag 1	1	1
Data Moves	MOV A, R	Move register to A	1	1
	MOV A, @R	Move data memory to a	1	1
	MOV A, #data	Move immediate to A	2	2
	MOV R, A	Move A to register	1	1
	MOV @R, A	Move A to data memory	1	1
	MOV R, #data	Move immediate to register	2	2
	MOV @R, #data	Move immediate to data memory	2	2
	MOV A, PSW	Move PSW to A	1	1
	MOV PSW, A	Move A to PSW	1	1
	XCH A, R	Exchange A and register	1	1
	XCHA, @R	Exchange A and data memory	1	1
	XCHD A, @R	Exchange nibble of A and register	1	1
	MOVX A, @R	Move external data memory to A	1	2
	MOVX @R, A	Move A to external data memory	1	2
	MOVP A, @A	Move to A from current page	1	2
	MOVP3 A, @A	Move to A from page 3	1	2
Timer/Counter	MOV A, T	Read timer/counter	1	1
	MOV T, A	Load timer/counter	1	1
	STRT T	Start timer	1	1
	STRT CNT	Start counter	1	1
	STOP TCNT	Stop timer/counter	1	1
	EN TCNTI	Enable timer/counter interrupt	1	1
	DIS TCNTI	Disable timer/counter interrupt	1	1
Control	EN I	Enable external interrupt	1	1
	DIS I	Disable external interrupt	1	1
	SEL RB0	Select register bank 0	1	1
	SEL RB1	Select register bank 1	1	1
	SEL MB0	Select memory bank 0	1	1
	SEL MB1	Select memory bank 1	1	1
	ENT0 CLK	Enable clock output on T0	1	1
	NOP	No operation	1	1

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 and 8035L.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+23V) input pin during 8748 programming.
		Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB_0-DB_7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENTO CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.

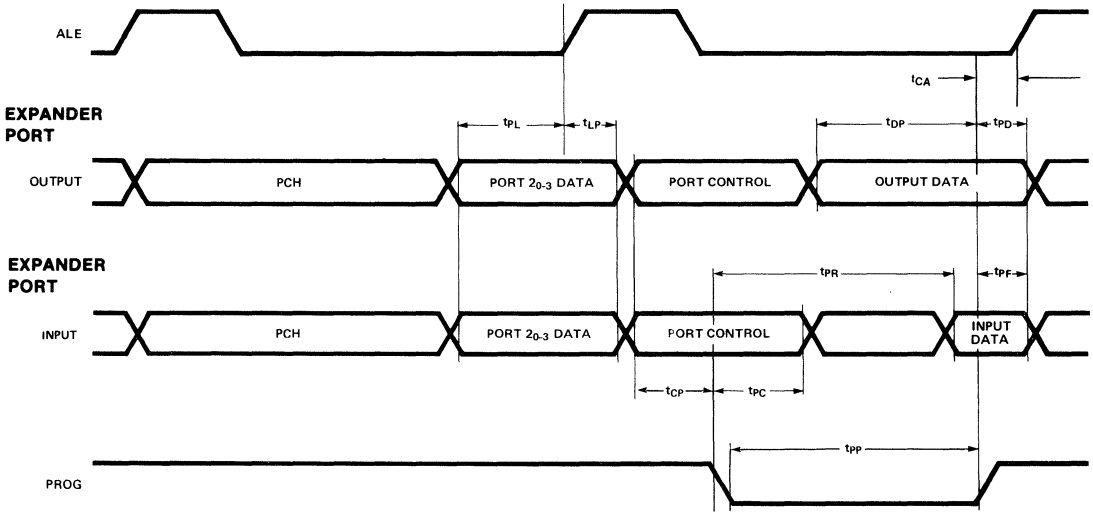
Designation	Pin#	Function
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device.
		Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a bus write. (Active low)
		Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in junction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

A.C. CHARACTERISTICS (PORT 2 TIMING)

T_A = -55°C to (100°C 8748/8035/125°C 8048/8035L), V_{CC} = +5V ± 10%, V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CP}	Port Control Setup Before Falling Edge of $\overline{PROG}$	115		ns	
t_{PC}	Port Control Hold After Falling Edge of $\overline{PROG}$	65		ns	
t_{PR}	PROG to Time P2 Input Must Be Valid		860	ns	
t_{PF}	Input Data Hold Time	0	160	ns	
t_{DP}	Output Data Setup Time	230		ns	
t_{PD}	Output Data Hold Time	25		ns	
t_{PP}	$\overline{PROG}$ Pulse Width	920		ns	
t_{PL}	Port 2 I/O Data Setup	300		ns	
t_{LP}	Port 2 I/O Data Hold	120		ns	

PORT 2 TIMING



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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias
- 8748/8035 ..... -55°C to +100°C
- 8048/8035L ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

Voltage On Any Pin With Respect to Ground ..... -0.5 to +7V

Power Dissipation ..... 1.5 Watt

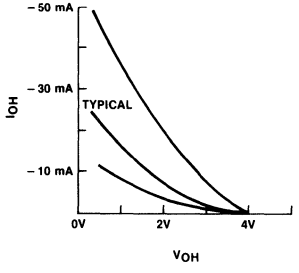
COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

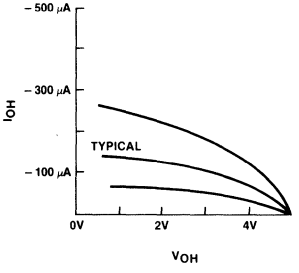
T_A = -55°C to (100°C 8748/8035/125°C 8048/8035L), $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except $\overline{RESET}$, X1, X2)	-.5		.7	V	
V_{IL1}	Input Low Voltage ($\overline{RESET}$, X1, X2)	-.5		.5	V	
V_{IH}	Input High Voltage (All Except XTAL1, XTAL 2, $\overline{RESET}$)	2.3		V_{CC}	V	
V_{IH1}	Input High Voltage ($\overline{RESET}$, X1, X2)	3.8		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			.45	V	I_{OL} = 1.2mA
V_{OL1}	Output Low Voltage (All Other Outputs)			.45	V	I_{OL} = 0.8mA
V_{OH}	Output High Voltage (BUS)	2.4			V	I_{OH} = -240μA
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	I_{OH} = -50μA
V_{OH2}	Output High Voltage (All Other Outputs)	2.4			V	I_{OH} = -30μA
I_{LI}	Input Leakage Current (T1, $\overline{INT}$)			± 10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LI1}	Input Leakage Current (P10-P17, P20-P27, EA, $\overline{SS}$)			-700	μA	V_{SS}+.45 $\leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current (BUS, TO) (High Impedance State)			± 10	μA	V_{SS} + .45$\leq V_{IN} \leq V_{CC}$
I_{DD}	V_{DD} Supply Current		10	25	mA	
$I_{DD} + I_{CC}$	Total Supply Current		80	155	mA	

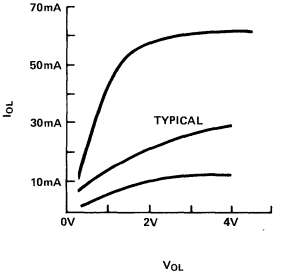
BUS



P1, P2



BUS, P1, P2



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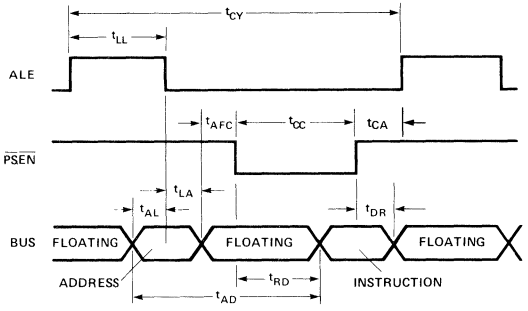
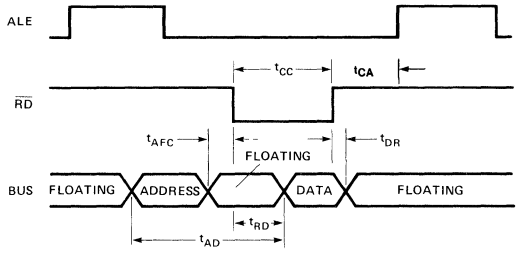
WAVEFORMS

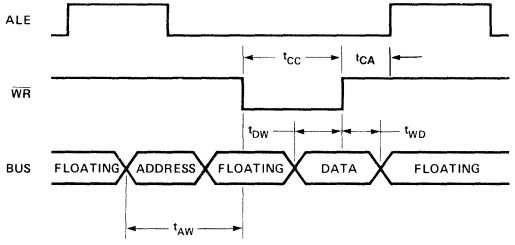
Instruction Fetch From External Program Memory



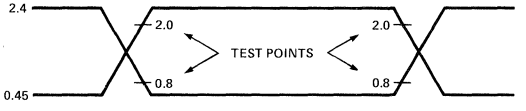
Read From External Data Memory



Write to External Data Memory



Input and Output Waveforms for A.C. Tests



A.C. CHARACTERISTICS

T_A = -55°C to (100°C 8748/8035/125°C 8048/8035L), V_{CC} = V_{DD} = +5V ± 10%, V_{SS} = 0V

Symbol	Parameter	8048 8648 (Note 2) 8748/8035/8035L		8748 8035		Unit	Conditions (Note 1)
		Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	200		300		ns	
t_{AL}	Address Setup to ALE	120		120		ns	
t_{LA}	Address Hold from ALE	80		80		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	400		600		ns	
t_{DW}	Data Setup before $\overline{WR}$	420		600		ns	
t_{WD}	Data Hold After $\overline{WR}$	80		120		ns	C_L = 20pF
t_{CY}	Cycle Time	2.5	15.0	4.17	15.0	μs	(3.6 MHz XTAL 8748/8035)
t_{DR}	Data Hold	0	200	0	200	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		400		600	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		260		ns	
t_{AD}	Address Setup to Data In		600		900	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	-40		-60		ns	
t_{CA}	Control Pulse to ALE	10		10		ns	

Note 1: Control outputs: C_L = 80 pF t_{CY} = 2.5μs for 8048/8035L
BUS Outputs: C_L = 150 pF 4.17μs for 8748/8035

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