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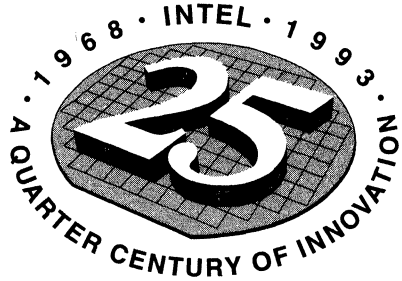

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80186
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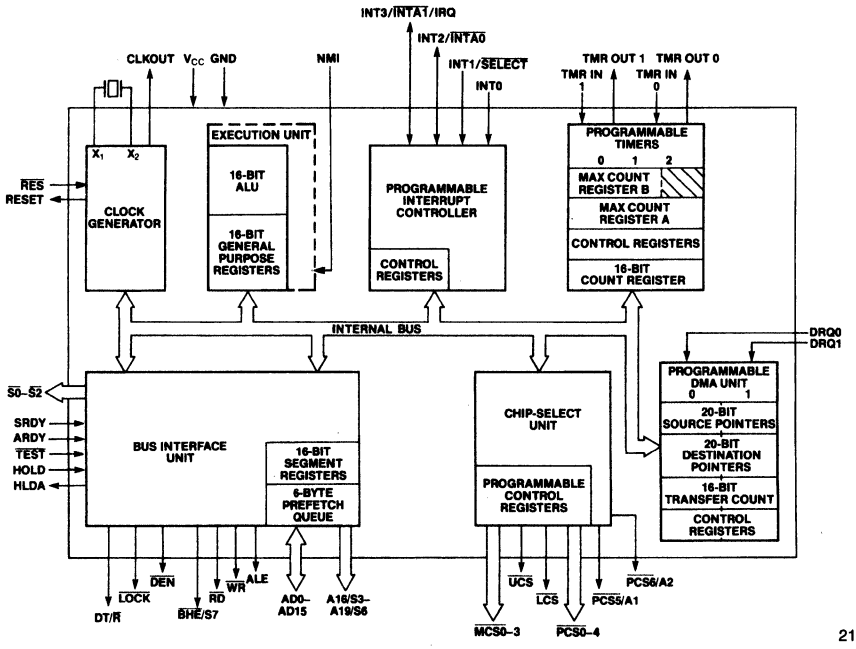

210451-1

Figure 1. 80186 Block Diagram

May 1991
Order Number: 210451-011

The Intel 80186 is a highly integrated 16-bit microprocessor. The 80186 effectively combines 15–20 of the most common 8086 system components onto one. The 80186 provides two times greater throughput than the standard 5 MHz 8086. The 80186 is upward compatible with 8086 and 8088 software and adds 10 new instruction types to the existing set.

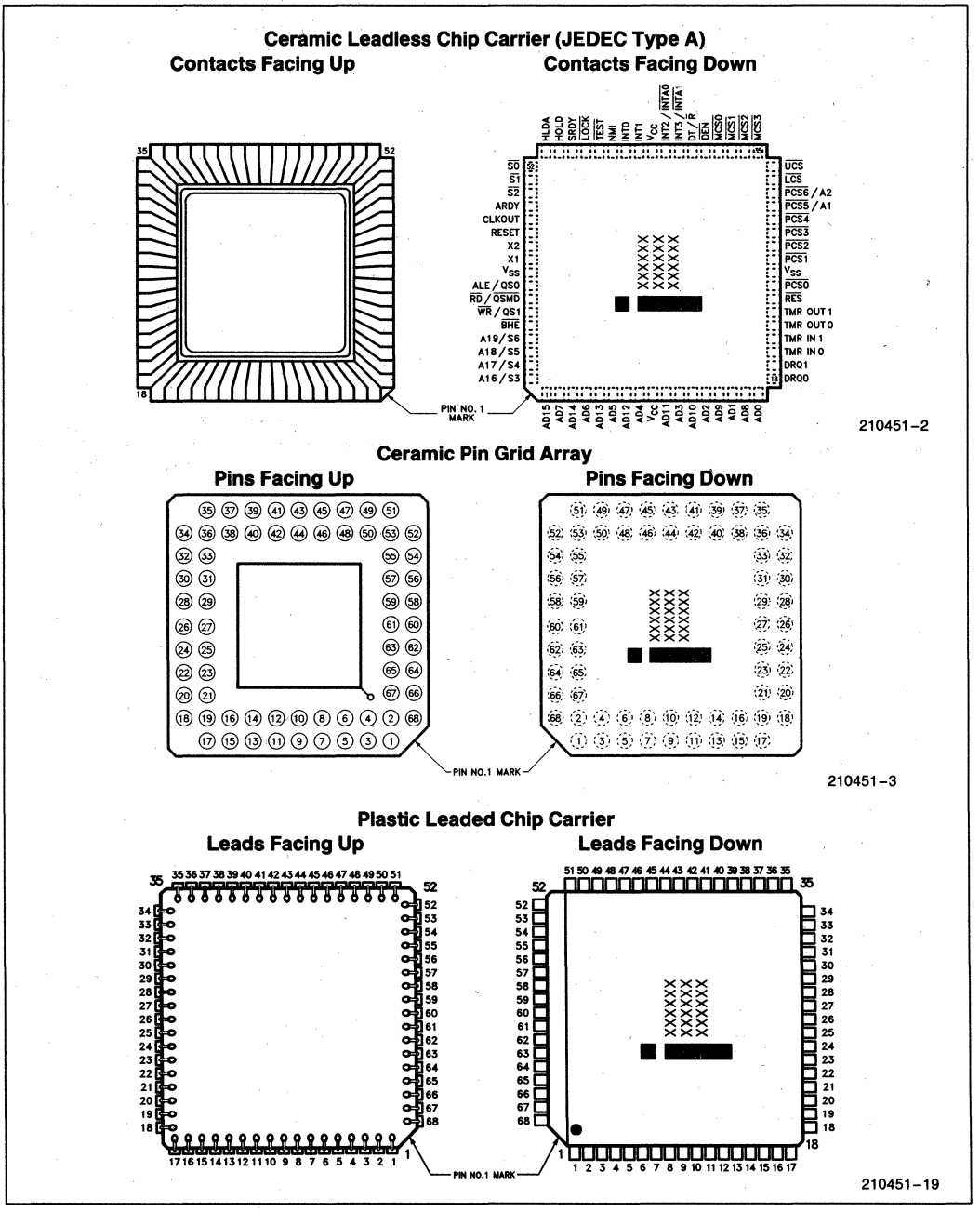

Figure 2. 80186 Pinout Diagrams

Table 1. 80186 Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	9 43	I	**System Power:** +5 volt power supply.
V_{SS}	26 60	I	System Ground.
RESET	57	O	Reset Output indicates that the 80186 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal.
X1 X2	59 58	I O	Crystal Inputs X1 and X2 provide external connections for a fundamental mode parallel resonant crystal for the internal oscillator. Instead of using a crystal, an external clock may be applied to X1 while minimizing stray capacitance on X2. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT.
$\overline{RES}$	24	I	An active $\overline{RES}$ causes the 80186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80186 clock. The 80186 begins fetching instructions approximately 6½ clock cycles after $\overline{RES}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{RES}$ held LOW. $\overline{RES}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network.
$\overline{TEST}$	47	I/O	$\overline{TEST}$ is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when "WAIT" execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80186 is waiting for $\overline{TEST}$, interrupts will be serviced. During power-up, active $\overline{RES}$ is required to configure $\overline{TEST}$ as an input. This pin is synchronized internally.
TMR IN 0 TMR IN 1	20 21	I I	Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized.
TMR OUT 0 TMR OUT 1	22 23	O O	Timer outputs are used to provide single pulse or continous waveform generation, depending upon the timer mode selected.
DRQ0 DRQ1	18 19	I I	DMA Request is asserted HIGH by an external device when it is ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
NMI	46	I	The Non-Maskable Interrupt input causes a Type 2 interrupt. An NMI transition from LOW to HIGH is latched and synchronized internally, and initiates the interrupt at the next instruction boundary. NMI must be asserted for at least one clock. The Non-Maskable Interrupt cannot be avoided by programming.
INT0 INT1/$\overline{SELECT}$ INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$/IRQ	45 44 42 41	I I I/O I/O	Maskable Interrupt Requests can be requested by activating one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When Slave Mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
A19/S6 A18/S5 A17/S4 A16/S3	65 66 67 68	O O O O	Address Bus Outputs (16–19) and Bus Cycle Status (3–6) indicate the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W, and T_4, the S6 pin is LOW to indicate a CPU-initiated bus cycle or HIGH to indicate a DMA-initiated bus cycle. During the same T-states, S3, S4, and S5 are always LOW. The status pins float during bus HOLD or RESET.
AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	1 3 5 7 10 12 14 16 2 4 6 8 11 13 15 17	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	Address/Data Bus (0–15) signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W, and T_4) bus. The bus is active HIGH. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7 through D_0. It is LOW during T_1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations.
$\overline{BHE}$/S7	64	O	During T_1 the Bus High Enable signal should be used to determine if data is to be enabled onto the most significant half of the data bus; pins D_{15}–D_8. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the higher half of the bus. The S_7 status information is available during T_2, T_3, and T_4. S_7 is logically equivalent to $\overline{BHE}$. $\overline{BHE}$/S7 floats during HOLD.
			$\overline{BHE}$ and A0 Encodings
			$\overline{BHE}$ Value / **A0 Value** / **Function** 0 / 0 / Word Transfer 0 / 1 / Byte Transfer on upper half of data bus (D15–D8) 1 / 0 / Byte Transfer on lower half of data bus (D_7–D_0) 1 / 1 / Reserved
ALE/QS0	61	O	Address Latch Enable/Queue Status 0 is provided by the 80186 to latch the address. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T_1 of the associated bus cycle, effectively one-half clock cycle earlier than in the 8086. The trailing edge is generated off the CLKOUT rising edge in T_1 as in the 8086. Note that ALE is never floated.
$\overline{WR}$/QS1	63	O	Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active LOW, and floats during HOLD. When the 80186 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.
			QS1 / **QS0** / **Queue Operation** 0 / 0 / No queue operation 0 / 1 / First opcode byte fetched from the queue 1 / 1 / Subsequent byte fetched from the queue 1 / 0 / Empty the queue

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RD}/\overline{QSMD}$	62	I/O	Read Strobe is an active LOW signal which indicates that the 80186 is performing a memory or I/O read cycle. It is guaranteed not to go LOW before the A/D bus is floated. An internal pull-up ensures that $\overline{RD}$ is HIGH during RESET. Following RESET the pin is sampled to determine whether the 80186 is to provide ALE, $\overline{RD}$, and $\overline{WR}$, or queue status information. To enable Queue Status Mode, $\overline{RD}$ must be connected to GND. $\overline{RD}$ will float during bus HOLD.
ARDY	55	I	Asynchronous Ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUT, and is active HIGH. The falling edge of ARDY must be synchronized to the 80186 clock. Connecting ARDY HIGH will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the SRDY pin.
SRDY	49	I	Synchronous Ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active-HIGH input synchronized to CLKOUT. The use of SRDY allows a relaxed system timing over ARDY. This is accomplished by elimination of the one-half clock cycle required to internally synchronize the ARDY input signal. Connecting SRDY high will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the ARDY pin.
$\overline{LOCK}$	48	O	$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of that instruction. No instruction prefetching will occur while $\overline{LOCK}$ is asserted. When executing more than one LOCK instruction, always make sure there are 6 bytes of code between the end of the first LOCK instruction and the start of the second LOCK instruction. $\overline{LOCK}$ is driven HIGH for one clock during RESET and then floated.
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	52 53 54	O O O	Bus cycle status $\overline{S0}$–$\overline{S2}$ are encoded to provide bus-transaction information:

80186 Bus Cycle Status Information

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

The status pins float during HOLD.
$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.

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Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
HOLD HLDA	50 51	I O	HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the 80186 clock. The 80186 will issue a HLDA (HIGH) in response to a HOLD request at the end of T_4 or T_i. Simultaneous with the issuance of HLDA, the 80186 will float the local bus and control lines. After HOLD is detected as being LOW, the 80186 will lower HLDA. When the 80186 needs to run another bus cycle, it will again drive the local bus and control lines.
$\overline{UCS}$	34	O	Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{UCS}$ is software programmable.
$\overline{LCS}$	33	O	Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{LCS}$ is software programmable.
$\overline{MCS0}$ $\overline{MCS1}$ $\overline{MCS2}$ $\overline{MCS3}$	38 37 36 35	O O O O	Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{MCS0}$–3 are software programmable.
$\overline{PCS0}$ $\overline{PCS1}$ $\overline{PCS2}$ $\overline{PCS3}$ $\overline{PCS4}$	25 27 28 29 30	O O O O O	Peripheral Chip Select signals 0–4 are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{PCS0}$–4 are software programmable.
$\overline{PCS5}$/A1	31	O	Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software-programmable. $\overline{PCS5}$/A1 does not float during bus HOLD. When programmed to provide latched A1, this pin will retain the previously latched value during HOLD.
$\overline{PCS6}$/A2	32	O	Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software programmable. $\overline{PCS6}$/A2 does not float during bus HOLD. When programmed to provide latched A2, this pin will retain the previously latched value during HOLD.
DT/$\overline{R}$	40	O	Data Transmit/Receive controls the direction of data flow through an external data bus transceiver. When LOW, data is transferred to the 80186. When HIGH the 80186 places write data on the data bus.
$\overline{DEN}$	39	O	Data Enable is provided as a data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access. $\overline{DEN}$ is HIGH whenever DT/$\overline{R}$ changes state. During RESET, $\overline{DEN}$ is driven HIGH for one clock, then floated. $\overline{DEN}$ also floats during HOLD.

FUNCTIONAL DESCRIPTION

Introduction

The following Functional Description describes the base architecture of the 80186. The 80186 is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip while providing twice the performance of the standard 8086. The 80186 is object code compatible with the 8086/8088 microprocessors and adds 10 new instruction types to the 8086/8088 instruction set.

80186 BASE ARCHITECTURE

The 8086, 8088, 80186, and 80286 family all contain the same basic set of registers, instructions, and addressing modes.

Register Set

The 80186 base architecture has fourteen registers as shown in Figures 3a and 3b. These registers are grouped into the following categories.

General Registers

Eight 16-bit general purpose registers may be used for arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

Segment Registers

Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

Base and Index Registers

Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

Status and Control Registers

Two 16-bit special purpose registers record or alter certain aspects of the 80186 processor state. These are the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed, and the Status Word Register, which contains status and control flag bits (see Figures 3a and 3b).

Status Word Description

The Status Word records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the 80186 within a given operating mode (bits 8, 9, and 10). The Status Word Register is 16-bits wide. The function of the Status Word bits is shown in Table 2.

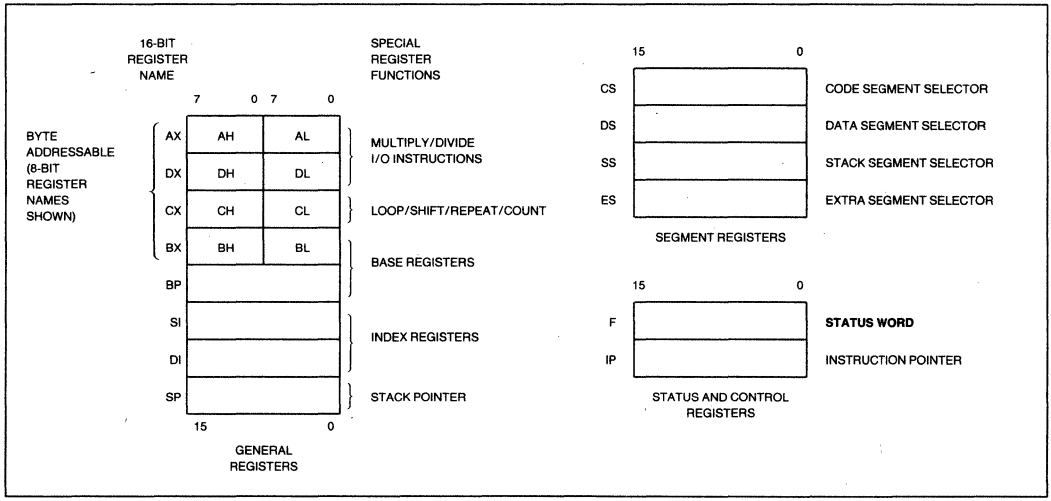

Figure 3a. 80186 Register Set

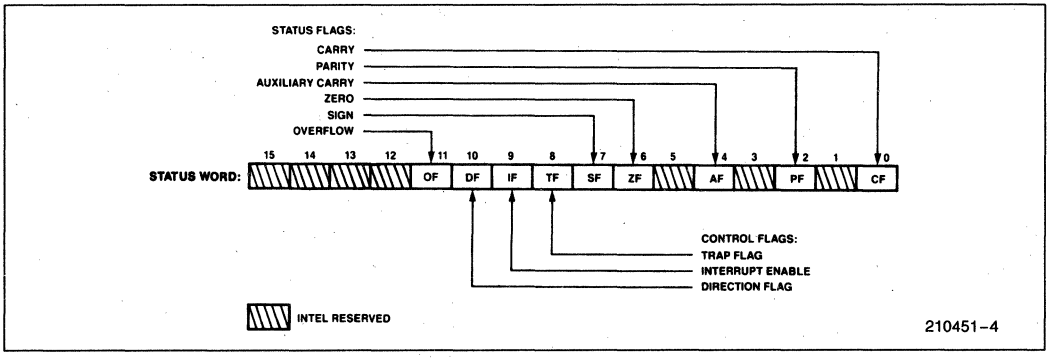

Figure 3b. Status Word Format

Table 2. Status Word Bit Functions

Bit Position	Name	Function
0	CF	Carry Flag—Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag—Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag—Set if result is zero; cleared otherwise
7	SF	Sign Flag—Set equal to high-order bit of result (0 if positive, 1 if negative)
8	TF	Single Step Flag—Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-enable Flag—When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag—Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag—Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high-level instructions, and processor control. These categories are summarized in Figure 4.

An 80186 instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory. Specific operand addressing modes are discussed later in this data sheet.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment register (code, data, stack, extra). The physical address is calculated by shifting the base value LEFT by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 5). This allows for a 1 MByte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 3). These rules follow the way programs are written (see Figure 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack
ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero
LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word
FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{\text{TEST}}$ pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Figure 4. 80186 Instruction Set

CONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal
JAE/JNB	Jump if above or equal/not below
JB/JNAE	Jump if below/not above nor equal
JBE/JNA	Jump if below or equal/not above
JC	Jump if carry
JE/JZ	Jump if equal/zero
JG/JNLE	Jump if greater/not less nor equal
JGE/JNL	Jump if greater or equal/not less
JL/JNGE	Jump if less/not greater nor equal
JLE/JNG	Jump if less or equal/not greater
JNC	Jump if not carry
JNE/JNZ	Jump if not equal/not zero
JNO	Jump if not overflow
JNP/JPO	Jump if not parity/parity odd
JNS	Jump if not sign

JO	Jump if overflow
JP/JPE	Jump if parity/parity even
JS	Jump if sign
UNCONDITIONAL TRANSFERS	
CALL	Call procedure
RET	Return from procedure
JMP	Jump
ITERATION CONTROLS	
LOOP	Loop
LOOPE/LOOPZ	Loop if equal/zero
LOOPNE/LOOPNZ	Loop if not equal/not zero
JCXZ	Jump if register CX = 0
INTERRUPTS	
INT	Interrupt
INTO	Interrupt if overflow
IRET	Interrupt return

Figure 4. 80186 Instruction Set (Continued)

To access operands that do not reside in one of the four immediately available segments, a full 32-bit pointer can be used to reload both the base (segment) and offset values.

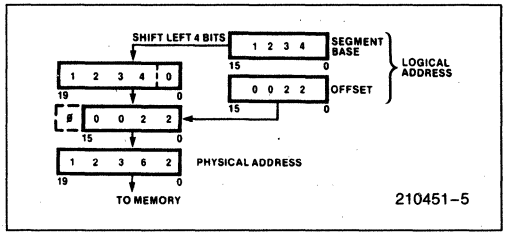

Figure 5. Two Component Address

Table 3. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data.
Stack	Stack (SS)	All stack pushes and pops; any memory references which use BP Register as a base register.
External Data (Global)	Extra (ES)	All string instruction references which use the DI register as an index.
Local Data	Data (DS)	All other data references.

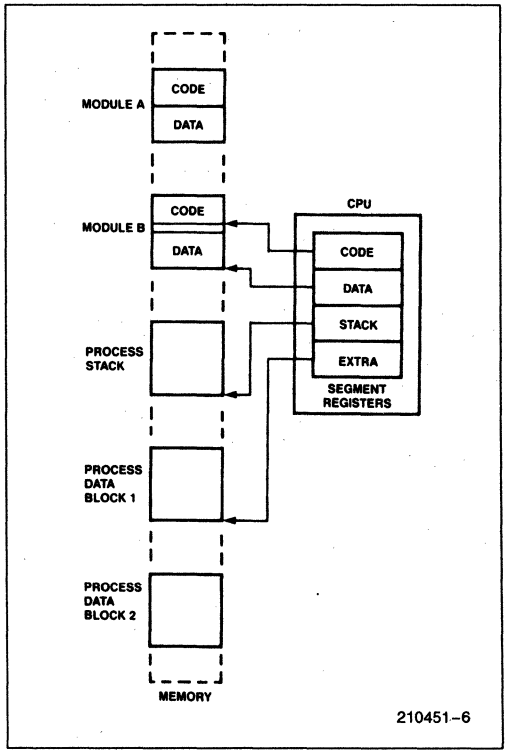

Figure 6. Segmented Memory Helps Structure Software

Addressing Modes

The 80186 provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an Index register.
- *Based indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

Data Types

The 80186 directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32- and 64-bit integers are supported using an 8087 Numeric Data Coprocessor with the 80186.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component or a 16-bit segment base component in addition to a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 to 64K bytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4-bits) of the byte.
- *Floating Point:* A signed 32-, 64-, or 80-bit real number representation. (Floating point operands are supported using an 8087 Numeric Data Coprocessor with the 80186.)

In general, individual data elements must fit within defined segment limits. Figure 7 graphically represents the data types supported by the 80186.

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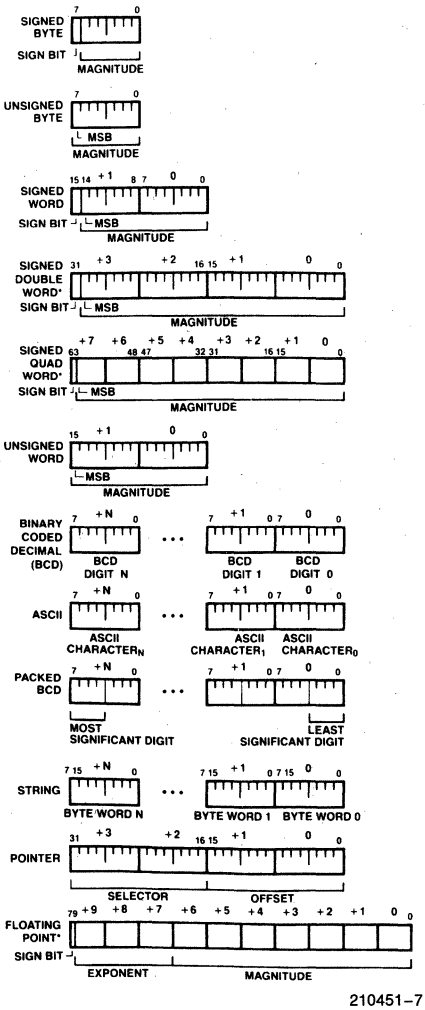
I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A_{15}–A_8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Status Word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.



NOTE:
*Supported by using an 8087 Numeric Data Coprocessor with the 80186.

Figure 7. 80186 Supported Data Types

Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. If the exception was caused by executing an ESC instruction with the ESC trap bit set in the relocation register, the return instruction will point to the ESC instruction, or to the segment override prefix immediately preceding the ESC instruction if the prefix was present. In all other cases, the return address from an exception will point at the instruction immediately following the instruction causing the exception.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0–31, some of which are used for instruction exceptions, are reserved. Table 4 shows the 80186 predefined types and default priority levels. For each interrupt, an 8-bit vector must be supplied to the 80186 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. In addition, internal peripherals and noncascaded external interrupts will generate their own vectors through the internal interrupt controller. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Interrupt Sources

The 80186 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INT0, DIV, IDIV, etc.). All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type (Table 4), multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

Those pre-defined 80186 interrupts which cannot be masked by programming are described below.

DIVIDE ERROR EXCEPTION (TYPE 0)

Generated when a DIV or IDIV instruction quotient cannot be expressed in the number of bits in the destination.

SINGLE-STEP INTERRUPT (TYPE 1)

Generated after most instructions if the TF flag is set. Interrupts will not be generated after prefix instructions (e.g., REP), instructions which modify segment registers (e.g., POP DS), or the WAIT instruction.

NON-MASKABLE INTERRUPT—NMI (TYPE 2)

An external interrupt source which cannot be masked.

Table 4. 80186 Interrupt Vectors

Interrupt Name	Vector Type	Vector Address	Default Priority	Related Instructions	Applicable Notes
Divide Error Exception	0	00H	1	DIV, IDIV	1
Single Step Interrupt	1	04H	1A	All	2
Non-Maskable Interrupt (NMI)	2	08H	1	All	
Breakpoint Interrupt	3	0CH	1	INT	1
INTO Detected Overflow Exception	4	10H	1	INTO	1
Array Bounds Exception	5	14H	1	BOUND	1
Unused Opcode Exception	6	18H	1	Undefined Opcodes	1
ESC Opcode Exception	7	1CH	1	ESC Opcodes (Coprocessor)	1, 3
Timer 0 Interrupt	8	20H	2A		4, 5
Timer 1 Interrupt	18	48H	2B		4, 5
Timer 2 Interrupt	19	4CH	2C		4, 5
Reserved	9	24H	3		
DMA 0 Interrupt	10	28H	4		5
DMA 1 Interrupt	11	2CH	5		
INT0 Interrupt	12	30H	6		
INT1 Interrupt	13	34H	7		
INT2 Interrupt	14	38H	8		
INT3 Interrupt	15	3CH	9		
Reserved	16, 17	40H, 44H			
Reserved	20–31	50H–7CH			

NOTES:
Default priorities for the interrupt sources are used only if the user does not program each source to a unique priority level.
1. Generated as a result of an instruction execution.
2. Performed in same manner as 8086.
3. An ESC (coprocessor) opcode will cause a trap only if the proper bit is set in the peripheral control block relocation register.
4. All three timers constitute one source of request to the interrupt controller. As such, they share the same priority level with respect to other interrupt sources. However, the timers have a defined priority order among themselves (2A > 2B > 2C).
5. The vector type numbers for these sources are programmable in Slave Mode.

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BREAKPOINT INTERRUPT (TYPE 3)

A one-byte version of the INT instruction. It uses 12 as an index into the service routine address table (because it is a type 3 interrupt).

INTO DETECTED OVERFLOW EXCEPTION (TYPE4)

Generated during an INTO instruction if the OF bit is set.

ARRAY BOUNDS EXCEPTION (TYPE 5)

Generated during a BOUND instruction if the array index is outside the array bounds. The array bounds are located in memory at a location indicated by one of the instruction operands. The other operand indicates the value of the index to be checked.

UNUSED OPCODE EXCEPTION (TYPE 6)

Generated if execution is attempted on undefined opcodes.

ESCAPE OPCODE EXCEPTION (TYPE 7)

Generated if execution is attempted of ESC opcodes (D8H–DFH). This exception will only be generated if a bit in the relocation register is set. The return address of this exception will point to the ESC instruction causing the exception. If a segment override prefix preceded the ESC instruction, the return address will point to the segment override prefix.

Hardware-generated interrupts are divided into two groups: maskable interrupts and non-maskable interrupts. The 80186 provides maskable hardware interrupt request pins INT0–INT3. In addition, maskable interrupts may be generated by the 80186

integrated DMA controller and the integrated timer unit. The vector types for these interrupts is shown in Table 4. Software enables these inputs by setting the interrupt flag bit (IF) in the Status Word. The interrupt controller is discussed in the peripheral section of this data sheet.

Further maskable interrupts are disabled while servicing an interrupt because the IF bit is reset as part of the response to an interrupt or exception. The saved Status Word will reflect the enable status of the processor prior to the interrupt. The interrupt flag will remain zero unless specifically set. The interrupt return instruction restores the Status Word, thereby restoring the original status of IF bit. If the interrupt return re-enables interrupts, and another interrupt is pending, the 80186 will immediately service the highest-priority interrupt pending, i.e., no instructions of the main line program will be executed.

Non-Maskable Interrupt Request (NMI)

A non-maskable interrupt (NMI) is also provided. This interrupt is serviced regardless of the state of the IF bit. A typical use of NMI would be to activate a power failure routine. The activation of this input causes an interrupt with an internally supplied vector value of 2. No external interrupt acknowledge sequence is performed. The IF bit is cleared at the beginning of an NMI interrupt to prevent maskable interrupts from being serviced.

Single-Step Interrupt

The 80186 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single-step interrupt and is controlled by the single-step flag bit (TF) in the Status Word. Once this bit is set, an internal single-step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single-stepped.

Initialization and Processor Reset

Processor initialization is accomplished by driving the $\overline{RES}$ input pin LOW. $\overline{RES}$ must be LOW during power-up to ensure proper device initialization. $\overline{RES}$ forces the 80186 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{RES}$ is active. After $\overline{RES}$ becomes inactive and an internal processing interval elapses, the 80186 begins execution with the instruction at physical location FFFF0(H). $\overline{RES}$ also sets some registers to predefined values as shown in Table 5.

Table 5. 80186 Initial Register State after RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

80186 CLOCK GENERATOR

The 80186 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

Oscillator

The oscillator circuit of the 80186 is designed to be used with a parallel resonant fundamental mode crystal. This is used as the time base for the 80186. The crystal frequency selected will be double the CPU clock frequency. Use of an LC or RC circuit is not recommended with this oscillator. If an external oscillator is used, it can be connected directly to the input pin X1 in lieu of a crystal. The output of the oscillator is not directly available outside the 80186. The recommended crystal configuration is shown in Figure 8.

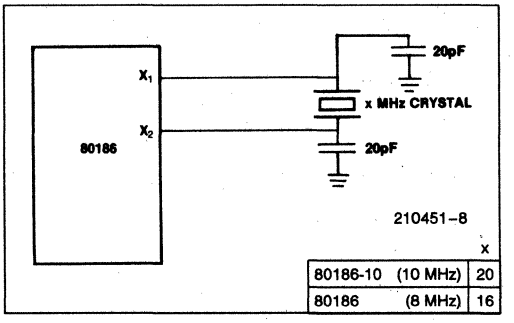

Figure 8. Recommended 80186 Crystal Configuration

Intel recommends the following values for crystal selection parameters:

Temperature Range:	0 to 70°C
ESR (Equivalent Series Resistance):	30Ω max
C_0 (Shunt Capacitance of Crystal):	7.0 pf max
C_1 (Load Capacitance):	20 pf ± 2 pf
Drive Level:	1 mW max

Clock Generator

The 80186 clock generator provides the 50% duty cycle processor clock for the 80186. It does this by dividing the oscillator output by 2 forming the symmetrical clock. If an external oscillator is used, the state of the clock generator will change on the falling edge of the oscillator signal. The CLKOUT pin provides the processor clock signal for use outside the 80186. This may be used to drive other system components. All timings are referenced to the output clock.

READY Synchronization

The 80186 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T_2, T_3, and again in the middle of each T_W until ARDY is sampled HIGH. One-half CLKOUT cycle of resolution time is used for full synchronization of a rising ARDY signal. A high-to-low transition on ARDY may be used as an indication of the not ready condition but it must be performed synchronously to CLKOUT **either** in the middle of T_2, T_3, or T_W, **or** at the falling edge of T_3 or T_W.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T_2, T_3 and again at the end of each T_W until it is sampled HIGH. By using this input rather than the asynchronous ready input, the half-clock cycle resolution time penalty is eliminated. This input must satisfy set-up and hold times to guarantee proper operation of the circuit.

In addition, the 80186, as part of the integrated chip-select logic, has the capability to program WAIT states for memory and peripheral blocks. This is discussed in the Chip Select/Ready Logic description.

RESET Logic

The 80186 provides both a $\overline{RES}$ input pin and a synchronized RESET output pin for use with other system components. The $\overline{RES}$ input pin on the 80186 is provided with hysteresis in order to facilitate power-on Reset generation via an RC network. RESET output is guaranteed to remain active for at least five clocks given a $\overline{RES}$ input of at least six clocks. RESET may be delayed up to approximately two and one-half clocks behind $\overline{RES}$.

Multiple 80186 processors may be synchronized through the $\overline{RES}$ input pin, since this input resets both the processor and divide-by-two internal counter in the clock generator. In order to ensure that the divide-by-two counters all begin counting at the same time, the active going edge of $\overline{RES}$ must satisfy a 25 ns setup time before the falling edge of the 80186 clock input. In addition, in order to ensure that all CPUs begin executing in the same clock cycle, the reset must satisfy a 25 ns setup time before the rising edge of the CLKOUT signal of all the processors.

LOCAL BUS CONTROLLER

The 80186 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides outputs that can be used to enable external buffers and to direct the flow of data on and off the local bus.

Memory/Peripheral Control

The 80186 provides ALE, $\overline{RD}$, and $\overline{WR}$ bus control signals. The $\overline{RD}$ and $\overline{WR}$ signals are used to strobe data from memory or I/O to the 80186 or to strobe data from the 80186 to memory or I/O. The ALE line provides a strobe to latch the address when it is valid. The 80186 local bus controller does not provide a memory/$\overline{I/O}$ signal. If this is required, use the $\overline{S2}$ signal (which will require external latching), make the memory and I/O spaces nonoverlapping, or use only the integrated chip-select circuitry.

Transceiver Control

The 80186 generates two control signals to be connected to transceiver chips. This capability allows the addition of transceivers for extra buffering without adding external logic. These control lines, DT/$\overline{R}$ and $\overline{DEN}$, are generated to control the flow of data through the transceivers. The operation of these signals is shown in Table 6.

Table 6. Transceiver Control Signals Description

Pin Name	Function
$\overline{DEN}$ (Data Enable)	Enables the output drivers of the transceivers. It is active LOW during memory, I/O, or INTA cycles.
DT/$\overline{R}$ (Data Transmit/ Receive)	Determines the direction of travel through the transceivers. A HIGH level directs data away from the processor during write operations, while a LOW level directs data toward the processor during a read operation.

Local Bus Arbitration

The 80186 uses a HOLD/HLDA system of local bus exchange. This provides an asynchronous bus exchange mechanism. This means multiple masters utilizing the same bus can operate at separate clock frequencies. The 80186 provides a single HOLD/HLDA pair through which all other bus masters may gain control of the local bus. External circuitry must arbitrate which external device will gain control of the bus when there is more than one alternate local bus master. When the 80186 relinquishes control of the local bus, it floats $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S0}$–$\overline{S2}$, $\overline{LOCK}$, AD0–AD15, A16–A19, $\overline{BHE}$, and DT/$\overline{R}$ to allow another master to drive these lines directly.

The 80186 HOLD latency time, i.e., the time between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is the highest-priority activity request which the processor may receive: higher than instruction fetching or internal DMA cycles. However, if a DMA cycle is in progress, the 80186 will complete the transfer before relinquishing the bus. This implies that if a HOLD request is received just as a DMA transfer begins, the HOLD latency time can be as great as 4 bus cycles. This will occur if a DMA word transfer operation is taking place from an odd address to an odd address. This is a total of 16 clocks or more, if WAIT states are required. In addition, if locked transfers are performed, the HOLD latency time will be increased by the length of the locked transfer.

Local Bus Controller and Reset

During RESET the local bus controller will perform the following action:

- Drive $\overline{DEN}$, $\overline{RD}$, and $\overline{WR}$ HIGH for one clock cycle, then float.

NOTE:
$\overline{RD}$ is also provided with an internal pull-up device to prevent the processor from inadvertently entering Queue Status Mode during RESET.

- Drive $\overline{S0}$–$\overline{S2}$ to the inactive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Float AD0–15, A16–19, $\overline{BHE}$, DT/$\overline{R}$.
- Drive ALE LOW (ALE is never floated).
- Drive HLDA LOW.

INTERNAL PERIPHERAL INTERFACE

All the 80186 integrated peripherals are controlled by 16-bit registers contained within an internal 256-byte control block. The control block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D_{15-0}, SRDY, and ARDY will be ignored. The base address of the control block must be on an even 256-byte boundary (i.e., the lower 8 bits of the base address are all zeros). All of the defined registers within this control block may be read or written by the 80186 CPU at any time.

The control block base address is programmed by a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block (see Figure 9). It provides the upper 12 bits of the base address of the control block. The control block is effectively an internal chip select range and must abide by all the rules concerning chip selects (the chip select circuitry is discussed later in this data sheet). Any access to the 256 bytes of the control block activates an internal chip select. Other chip selects may overlap the control block only if they are programmed to zero wait states and ignore external ready. In addition, bit 12 of this register determines whether the control block will be mapped into I/O or memory space. If this bit is 1, the control block will be located in memory space. If the bit is 0, the control block will be located in I/O space. If the control register block is mapped into I/O space, the upper 4 bits of the base address must be programmed as 0 (since I/O addresses are only 16 bits wide).

In addition to providing relocation information for the control block, the relocation register contains bits which place the interrupt controller into Slave Mode, and cause the CPU to interrupt upon encountering ESC instructions. At RESET, the relocation register

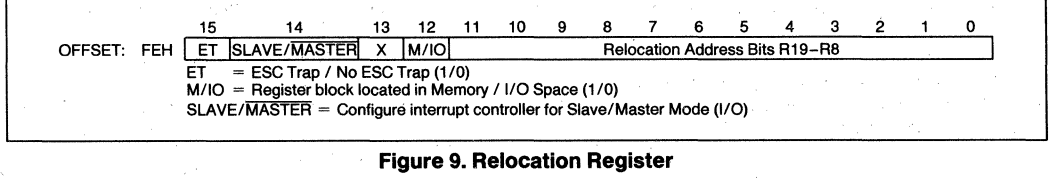

Figure 9. Relocation Register

is set to 20FFH, which maps the control block to start at FF00H in I/O space. An offset map of the 256-byte control register block is shown in Figure 10.

CHIP-SELECT/READY GENERATION LOGIC

The 80186 contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

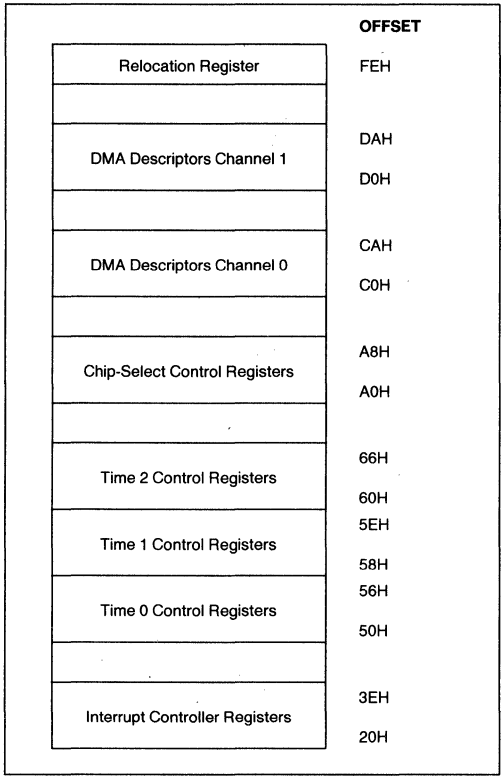

Figure 10. Internal Register Map

Memory Chip Selects

The 80186 provides 6 memory chip select outputs for 3 address areas; upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

The range for each chip select is user-programmable and can be set to 2K, 4K, 8K, 16K, 32K, 64K, 128K (plus 1K and 256K for upper and lower chip selects). In addition, the beginning or base address of the midrange memory chip select may also be selected. Only one chip select may be programmed to be active for any memory location at a time. All chip select sizes are in bytes, whereas 80186 memory is arranged in words. This means that if, for example, 16 64K x 1 memories are used, the memory block size will be 128K, not 64K.

Upper Memory $\overline{CS}$

The 80186 provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the 80186 begins executing at memory location FFFF0H.

The upper limit of memory defined by this chip select is always FFFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is also defined. Table 7 shows the relationship between the base address selected and the size of the memory block obtained.

Table 7. UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000	256K	C038H

The lower limit of this memory block is defined in the UMCS register (see Figure 11). This register is at offset A0H in the internal control block. The legal values for bits 6–13 and the resulting starting address and memory block sizes are given in Table 7. Any combination of bits 6–13 not shown in Table 7 will result in undefined operation. After reset, the UMCS register is programmed for a 1K area. It must be reprogrammed if a larger upper memory area is desired.

The internal generation of any 20-bit address whose upper 16 bits are equal to or greater than the UMCS

value (with bits 0–5 as "0") asserts $\overline{UCS}$. UMCS bits R2–R0 specify the ready mode for the area of memory defined by this chip select register, as explained later.

Lower Memory $\overline{CS}$

The 80186 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The lower limit of memory defined by this chip select is always 0H, while the upper limit is programmable. By programming the upper limit, the size of the memory block is defined. Table 8 shows the relationship between the upper address selected and the size of the memory block obtained.

Table 8. LMCS Programming Values

Upper Address	Memory Block Size	LMCS Value (Assuming R0=R1=R2=0)
003FFH	1K	0038H
007FFH	2K	0078H
00FFFH	4K	00F8H
01FFFH	8K	01F8H
03FFFH	16K	03F8H
07FFFH	32K	07F8H
0FFFFH	64K	0FF8H
1FFFFH	128K	1FF8H
3FFFFH	256K	3FF8H

The upper limit of this memory block is defined in the LMCS register (see Figure 12) at offset A2H in the internal control block. The legal values for bits 6–15 and the resulting upper address and memory block sizes are given in Table 8. Any combination of bits 6–15 not shown in Table 8 will result in undefined operation. After RESET, the LMCS register value is undefined. However, the $\overline{LCS}$ chip-select line will not become active until the LMCS register is accessed.

Any internally generated 20-bit address whose upper 16 bits are less than or equal to LMCS (with bits 0–5 "1") will assert $\overline{LCS}$. LMCS register bits R2–R0 specify the READY mode for the area of memory defined by this chip-select register.

Mid-Range Memory $\overline{CS}$

The 80186 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located within the 80186 1M byte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the mid-range select lines, as shown in Table 9, is determined by bits 8–14 of the MPCS register (see Figure 13). This register is at location A8H in the internal control block. One and only one of bits 8–14 must be set at a time. Unpredictable operation of the $\overline{MCS}$ lines will otherwise occur. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the mid-range block. If the total block size is 32K, each chip select is active for 8K of memory with $\overline{MCS0}$ being active for the first range and $\overline{MCS3}$ being active for the last range.

The EX and MS in MPCS relate to peripheral functionality as described in a later section.

Table 9. MPCS Programming Values

Total Block Size	Individual Select Size	MPCS Bits 14–8
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

The base address of the mid-range memory block is defined by bits 15–9 of the MMCS register (see Figure 14). This register is at offset A6H in the internal

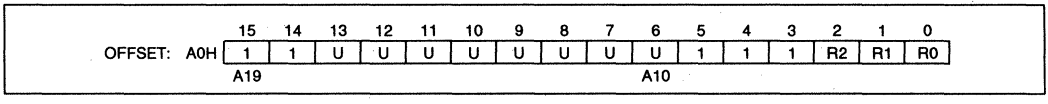

Figure 11. UMCS Register

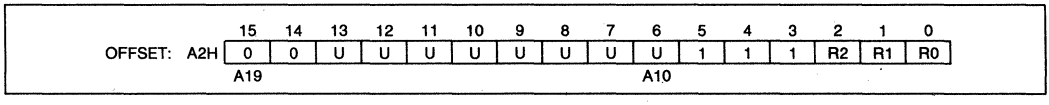

Figure 12. LMCS Register

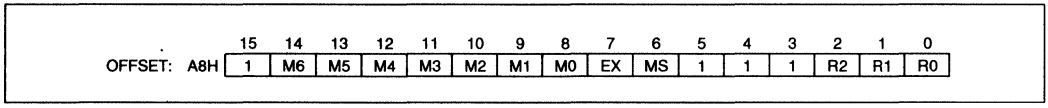

Figure 13. MPCS Register

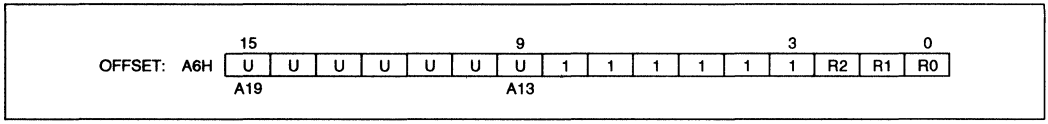

Figure 14. MMCS Register

control block. These bits correspond to bits A19–A13 of the 20-bit memory address. Bits A12–A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the mid-range block size is 32K (or the size of the block for which each $\overline{MCS}$ line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, since the first few integer multiples of a 32K memory block are 0H, 8000H, 10000H, 18000H, etc. After RESET, the contents of both of these registers are undefined. However, none of the $\overline{MCS}$ lines will be active until both the MMCS and MPCS registers are accessed.

MMCS bits R2–R0 specify READY mode of operation for all four mid-range chip selects.

The 512K block size for the mid-range memory chip selects is a special case. When using 512K, the base address would have to be at either locations 00000H or 80000H. If it were to be programmed at 00000H when the $\overline{LCS}$ line was programmed, there would be an internal conflict between the $\overline{LCS}$ ready generation logic and the $\overline{MCS}$ ready generation logic. Likewise, if the base address were programmed at 80000H, there would be a conflict with the $\overline{UCS}$ ready generation logic. Since the $\overline{LCS}$ chip-select line does not become active until programmed, while the $\overline{UCS}$ line is active at reset, the memory base can be set only at 00000H. If this base address is selected, however, the $\overline{LCS}$ range must not be programmed.

Peripheral Chip Selects

The 80186 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address may be located in either memory or I/O space.

Seven $\overline{CS}$ lines called $\overline{PCS0}$–6 are generated by the 80186. The base address is user-programmable; however it can only be a multiple of 1K bytes, i.e., the least significant 10 bits of the starting address are always 0.

$\overline{PCS5}$ and $\overline{PCS6}$ can also be programmed to provide latched address bits A1 and A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0 and A1 pins used for selecting internal registers of 8-bit peripheral chips. This simplifies the external hardware because the peripheral registers can be located on even boundaries in I/O or memory space.

The starting address of the peripheral chip-select block is defined by the PACS register (see Figure 15). The register is located at offset A4H in the internal control block. Bits 15–6 of this register correspond to bits 19–10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block. Bits 9–0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12–15 must be programmed zero, since the I/O address is only 16 bits wide. Table 10 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

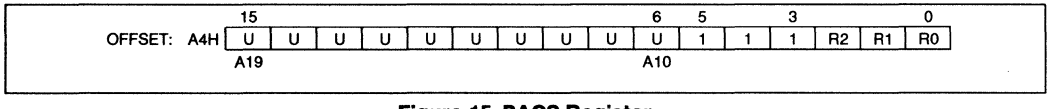

Figure 15. PACS Register

The user should program bits 15–6 to correspond to the desired peripheral base location. PACS bits 0–2 are used to specify READY mode for $\overline{PCS0}$–$\overline{PCS3}$.

Table 10. PCS Address Ranges

$\overline{PCS}$ Line	Active between Locations
$\overline{PCS0}$	PBA —PBA+127
$\overline{PCS1}$	PBA+128—PBA+255
$\overline{PCS2}$	PBA+256—PBA+383
$\overline{PCS3}$	PBA+384—PBA+511
$\overline{PCS4}$	PBA+512—PBA+639
$\overline{PCS5}$	PBA+640—PBA+767
$\overline{PCS6}$	PBA+768—PBA+895

The mode of operation of the peripheral chip selects is defined by the MPCS register (which is also used to set the size of the mid-range memory chip-select block, see Figure 13). The register is located at offset A8H in the internal control block. Bit 7 is used to select the function of $\overline{PCS5}$ and $\overline{PCS6}$, while bit 6 is used to select whether the peripheral chip selects are mapped into memory or I/O space. Table 11 describes the programming of these bits. After RESET, the contents of both the MPCS and the PACS registers are undefined, however none of the PCS lines will be active until both of the MPCS and PACS registers are accessed.

Table 11. MS, EX Programming Values

Bit	Description
MS	1 = Peripherals mapped into memory space.
	0 = Peripherals mapped into I/O space.
EX	0 = 5 $\overline{PCS}$ lines. A1, A2 provided.
	1 = 7 $\overline{PCS}$ lines. A1, A2 are not provided.

MPCS bits 0–2 specify the READY mode for $\overline{PCS4}$–$\overline{PCS6}$ as outlined below.

READY Generation Logic

The 80186 can generate a READY signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the 80186 may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

READY control consists of 3 bits for each $\overline{CS}$ line or group of lines generated by the 80186. The interpretation of the READY bits is shown in Table 12.

Table 12. READY Bits Programming

R2	R1	R0	Number of WAIT States Generated
0	0	0	0 wait states, external RDY also used.
0	0	1	1 wait state inserted, external RDY also used.
0	1	0	2 wait states inserted, external RDY also used.
0	1	1	3 wait states inserted, external RDY also used.
1	0	0	0 wait states, external RDY ignored.
1	0	1	1 wait state inserted, external RDY ignored.
1	1	0	2 wait states inserted, external RDY ignored.
1	1	1	3 wait states inserted, external RDY ignored.

The internal ready generator operates in parallel with external READY, not in series if the external READY is used (R2 = 0). For example, if the internal generator is set to insert two wait states, but activity on the external READY lines will insert four wait states, the processor will only insert four wait states, not six. This is because the two wait states generated by the internal generator overlapped the first two wait states generated by the external ready signal. Note that the external ARDY and SRDY lines are always ignored during cycles accessing internal peripherals.

R2–R0 of each control word specifies the READY mode for the corresponding block, with the exception of the peripheral chip selects: R2–R0 of PACS set the $\overline{PCS0}$–3 READY mode, R2–R0 of MPCS set the $\overline{PCS4}$–6 READY mode.

Chip Select/Ready Logic and Reset

Upon RESET, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to insert 3 wait states in conjunction with external READY (i.e., UMCS resets to FFFBH).

- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

DMA CHANNELS

The 80186 DMA controller provides two independent DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a maximum data transfer rate of 1.25 Mword/sec or 2.5 MBytes/sec at 10 MHz.

DMA Operation

Each channel has six registers in the control block which define each channel's operation. The control registers consist of a 20-bit Source pointer (2 words), a 20-bit destination pointer (2 words), a 16-bit Transfer Count Register, and a 16-bit Control Word. The format of the DMA Control Blocks is shown in Table 13. The Transfer Count Register (TC) specifies the number of DMA transfers to be performed. Up to 64K byte or word transfers can be performed with automatic termination. The Control Word defines the channel's operation (see Figure 17). All registers may be modified or altered during any DMA activity. Any changes made to these registers will be reflected immediately in DMA operation.

Table 13. DMA Control Block Format

Register Name	Register Address	
	Ch. 0	Ch. 1
Control Word	CAH	DAH
Transfer Count	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

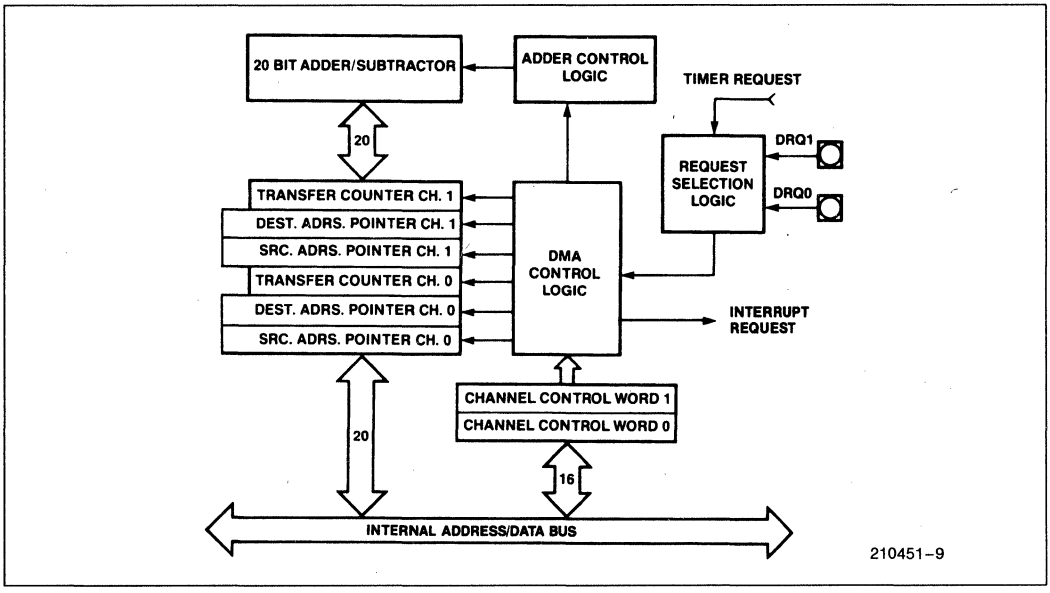

Figure 16. DMA Unit Block Diagram

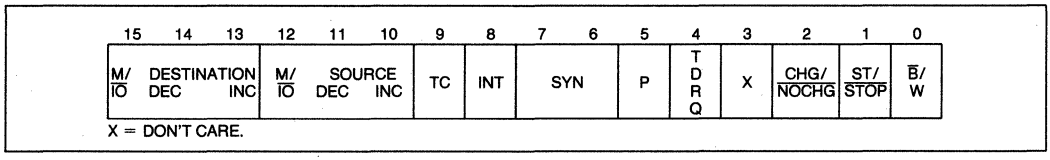

Figure 17. DMA Control Register

DMA Channel Control Word Register

Each DMA Channel Control Word determines the mode of operation for the particular 81086 DMA channel. This register specifies:

- the mode of synchronization;
- whether bytes or words will be transferred;
- whether interrupts will be generated after the last transfer;
- whether DMA activity will cease after a programmed number of DMA cycles;
- the relative priority of the DMA channel with respect to the other DMA channel;
- whether the source pointer will be incremented, decremented, or maintained constant after each transfer;
- whether the source pointer addresses memory or I/O space;
- whether the destination pointer will be incremented, decremented, or maintained constant after each transfer; and
- whether the destination pointer will address memory or I/O space.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

DMA Control Word Bit Descriptions

DEST: M/$\overline{IO}$ Destination pointer is in memory (1) or I/O (0) space.

DEC Decrement destination pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

INC Increment destination pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

If both INC and DEC are specified, the pointer will not change after each cycle.

SOURCE: M/$\overline{IO}$ Source pointer is in memory (1) or I/O (0) space.

DEC Decrement source pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

INC Increment source pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

If both INC and DEC are specified, the pointer will not change after each cycle.

TC: If set, DMA will terminate when the contents of the transfer count register reach zero. The ST/$\overline{STOP}$ bit will also be reset at this point. If cleared, the DMA controller will decrement the transfer count register for each DMA cycle, but DMA transfers will not stop when the transfer count register reaches zero.

INT: Enable interrupts to CPU upon transfer count termination.

SYN: 00 No synchronization.

NOTE:

When unsynchronized transfers are specified, the TC bit will be ignored and the ST bit will be cleared upon the transfer count reaching zero, stopping the channel.

01 Source synchronization.

10 Destination synchronization.

11 Unused.

P: Channel priority relative to other channel during simultaneous requests.

0 Low priority.

1 High priority.

Channels will alternate cycles if both are set at same priority level.

TDRQ: Enable/Disable (1/0) DMA requests from timer 2.

CHG/$\overline{\text{NOCHG}}$: Change/Do not change (1/0) ST/$\overline{\text{STOP}}$ bit. If this bit is set when writing the control word, the ST/$\overline{\text{STOP}}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{\text{STOP}}$ bit will not be altered. This bit is not stored; it will always be read as 0.

ST/$\overline{\text{STOP}}$: Start/Stop (1/0) channel.

$\overline{\text{B}}$/W: Byte/Word (0/1) transfers.

DMA Destination and Source Pointer Registers

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address (see Figure 18). These pointers may be individually incremented or decremented after each transfer. If word transfers are performed the pointer is incremented or decremented by two. Each pointer may point into either memory or I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on values for the pointer registers. Higher transfer rates can be obtained if all word transfers are performed to even addresses, since this will allow data to be accessed in a single bus cycle.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). The register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA Control Register. If the TC bit in the DMA control word is set or if unsynchronized transfers are programmed, however, DMA activity will terminate when the transfer count register reaches zero.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred. When source or unsynchronized transfers are performed, the DMA channel may begin another transfer immediately after the end of a previous DMA transfer. This allows a complete transfer to take place every 2 bus cycles or eight clock cycles (assuming no wait states). When destination synchronized transfers are performed, data will not be fetched from the source address until the destination device signals that it is ready to receive it. Also, the DMA controller will relinquish control of the bus after every transfer. If no other bus activity is initiated, another destination synchronized DMA cycle will begin after two processor clocks. This allows the destination device time to remove its request if another transfer is not desired. Since the DMA controller will relinquish the bus, the CPU can initiate a bus cycle. As a result, a complete bus cycle will often be inserted between destination synchronized transfers. Table 14 shows the maximum DMA transfer rates.

Table 14. Maximum DMA Transfer Rates @ CLKOUT = 10 MHz

Type of Synchronization Selected	CPU Running	CPU Halted
Unsynchronized	2.5MBytes/sec	2.5MBytes/sec
Source Synch.	2.5MBytes/sec	2.5MBytes/sec
Destination Synch.	1.7MBytes/sec	2.0MBytes/sec

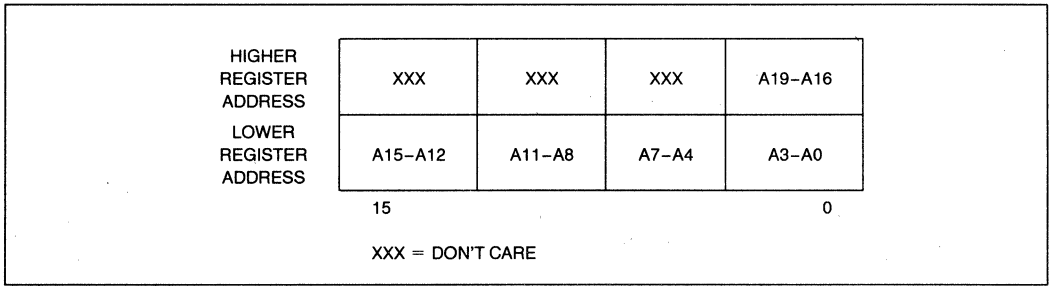

Figure 18. DMA Pointer Register Format

DMA Acknowledge

No explicit DMA acknowledge pulse is provided. Since both source and destination pointers are maintained, a read from a requesting source, or a write to a requesting destination, should be used as the DMA acknowledge signal. Since the chip-select lines can be programmed to be active for a given block of memory or I/O space, and the DMA pointers can be programmed to point to the same given block, a chip-select line could be used to indicate a DMA acknowledge.

DMA Priority

The DMA channels may be programmed to give one channel priority over the other, or they may be programmed to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses to odd memory locations; also, an external bus hold takes priority over an internal DMA cycle. Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time will suffer during sequences of continuous DMA cycles. An NMI request, however, will cause all internal DMA activity to halt. This allows the CPU to quickly respond to the NMI request.

DMA Programming

DMA cycles will occur whenever the ST/STOP bit of the Control Register is set. If synchronized transfers are programmed, a DRQ must also be generated. Therefore the source and destination transfer pointers, and the transfer count register (if used) must be programmed before the ST/$\overline{\text{STOP}}$ bit is set.

Each DMA register may be modified while the channel is operating. If the CHG/NOCHG bit is cleared when the control register is written, the ST/$\overline{\text{STOP}}$ bit of the control register will not be modified by the write. If multiple channel registers are modified, it is recommended that a LOCKED string transfer be used to prevent a DMA transfer from occurring between updates to the channel registers.

DMA Channels and Reset

Upon RESET, the DMA channels will perform the following actions:

- The Start/Stop bit for each channel will be reset to STOP.
- Any transfer in progress is aborted.

TIMERS

The 80186 provides three internal 16-bit programmable timers (see Figure 19). Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

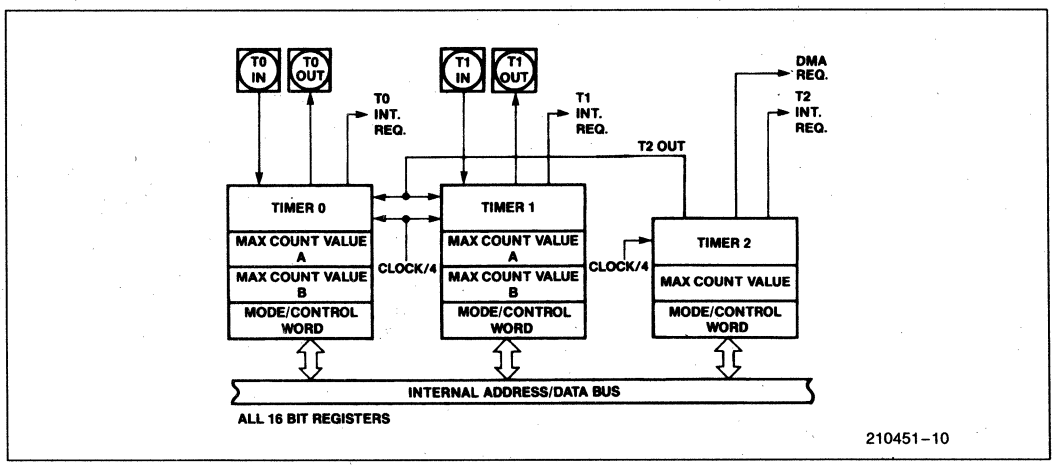

Figure 19. Timer Block Diagram

Timer Operation

The timers are controlled by 11 16-bit registers in the peripheral control block. The configuration of these registers is shown in Table 15. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a MAX COUNT register, which defines the maximum count the timer will reach. After reaching the MAX COUNT register value, the timer count value will reset to zero during that same clock, i.e., the maximum count value is never stored in the count register itself. Timers 0 and 1 are, in addition, equipped with a second MAX COUNT register, which enables the timers to alternate their count between two different MAX COUNT values. If a single MAX COUNT register is used, the timer output pin will switch LOW for a single clock, 1 clock after the maximum count value has been reached. In the dual MAX COUNT register mode, the output pin will indicate which MAX COUNT register is currently in use, thus allowing nearly complete freedom in selecting waveform duty cycles. For the timers with two MAX COUNT registers, the RIU bit in the control register determines which is used for the comparison.

Each timer gets serviced every fourth CPU-clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU-clock rate (2 MHz for an 8 MHz CPU clock). Due to internal synchronization and pipelining of the timer circuitry, a timer output may take up to 6 clocks to respond to any individual clock or gate input.

Since the count registers and the maximum count registers are all 16 bits wide, 16 bits of resolution are provided. Any Read or Write access to the timers will add one wait state to the minimum four-clock bus cycle, however. This is needed to synchronize and coordinate the internal data flows between the internal timers and the internal bus.

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between MAX COUNT registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

These options are selectable via the timer mode/control word.

Timer Mode/Control Register

The mode/control register (see Figure 20) allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

Table 15. Timer Control Block Format

Register Name	Register Offset		
	Tmr. 0	Tmr. 1	Tmr. 2
Mode/Control Word	56H	5EH	66H
Max Count B	54H	5CH	not present
Max Count A	52H	5AH	62H
Count Register	50H	58H	60H

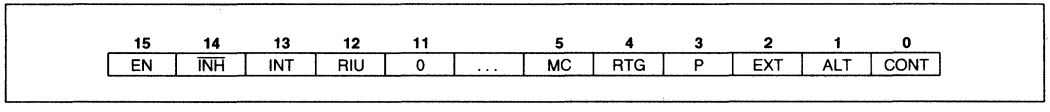

Figure 20. Timer Mode/Control Register

EN:

The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transistions during the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

$\overline{\text{INH}}$:

The inhibit bit allows for selective updating of the enable (EN) bit. If INH is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If INH is a zero during the write, the EN bit will be unaffected by the operation.This bit is not stored; it will always be a 0 on a read.

INT:

When set, the INT bit enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual MAX COUNT register mode, an interrupt will be generated each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the Interrupt Controller).

RIU:

The Register In Use bit indicates which MAX COUNT register is currently being used for comparison to the timer count value. A zero value indicates register A. The RIU bit cannot be written, i.e., its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.

MC:

The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. This bit is set regardless of the timer's interrupt-enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts.

Programmer intervention is required to clear this bit.

RTG:

Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is HIGH, the timer will count; if the input pin is LOW, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the 80186 clock.

When RTG = 1, the input pin detects LOW-to-HIGH transitions. The first such transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

P:

The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

EXT:

The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the 80186 clock. If this bit is set, the timer will count LOW-to-HIGH transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input to output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

ALT:

The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method of generating non-repetitive waveforms. Square waves and pulse

outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will go LOW for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT:

Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset, and halt.

Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Count Registers

Each of the three timers has a 16-bit count register. The contents of this register may be read or written by the processor at any time. If the register is written while the timer is counting,the new value will take effect in the current count cycle.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two max count values whenever the current maximum count is reached. A timer resets when the timer count register equals the max count value being used. If the timer count register or the max count register is changed so that the max count is less than the timer count, the timer does not immediately reset. Instead, the timer counts up to 0FFFFH, "wraps around" to zero, counts up to the max count value, and then resets.

Timers and Reset

Upon RESET, the Timers will perform the following actions:

- All EN (Enable) bits are reset preventing timer counting.
- For Timers 0 and 1, the RIU bits are reset to zero and the ALT bits are set to one. This results in the Timer Out pins going high.

INTERRUPT CONTROLLER

The 80186 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The 80186 interrupt controller has its own control register that sets the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service rountines for lower priority interrupts may be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Figure 21.

The 80186 has a special Slave Mode in which the internal interrupt controller acts as a slave to an external master. The controller is programmed into this mode by setting bit 14 in the peripheral control block relocation register. (See Slave Mode section.)

MASTER MODE OPERATION

Interrupt Controller External Interface

Five pins are provided for external interrupt sources. One of these pins is NMI, the non-maskable interrupt. NMI is generally used for unusual events such as power-fail interrupts. The other four pins may be configured in any of the following ways:

- As four interrupt input lines with internally generated interrupt vectors.
- As an interrupt line and interrupt acknowledge line pair (Cascade Mode) with externally generated interrupt vectors plus two interrupt input lines with internally generated vectors.
- As two pairs of interrupt/interrupt acknowledge lines (Cascade Mode) with externally generated interrupt vectors.

External sources in the Cascade Mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the 80186 on the second cycle. The capability to interface to external 8259A programmable interrupt controllers is provided when the inputs are configured in Cascade Mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in Master Mode are similar to the 8259A. The interrupt controller responds identically to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

Fully Nested Mode

When in the fully nested mode four pins are used as direct interrupt requests as in Figure 22. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate with interrupts enabled, yet be suspended only by interrupts of higher priority than the in-service interrupt.

When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register. This is required to allow subsequent interrupts from this interrupt source and to allow servicing of lower-priority interrupts. An EOI command is executed at the end of the service routine just before the return from interrupt instruction. If the fully nested structure has been upheld, the next highest-priority source with its IS bit set is then serviced.

Cascade Mode

The 80186 has four interrupt pins and two of them have dual functions. In the fully nested mode the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In the Cascade Mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. The interconnection is shown in Figure 23. INT0 is an interrupt input interfaced to an 8259A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to that peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the Cascade Mode by programming the proper value into INT0 and INT1 control registers. The use of the dedicated acknowledge signals eliminates the need for the use of external logic to generate $\overline{\text{INTA}}$ and device select signals.

The primary Cascade Mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave 8259As. Three levels of priority are created, requiring priority resolution in the 80186 interrupt controller, the master 8259As, and the slave 8259As. If an external interrupt is serviced, one IS bit is set at each of these levels. When the interrupt service routine is completed, up to three end-of-interrupt commands must be issued by the programmer.

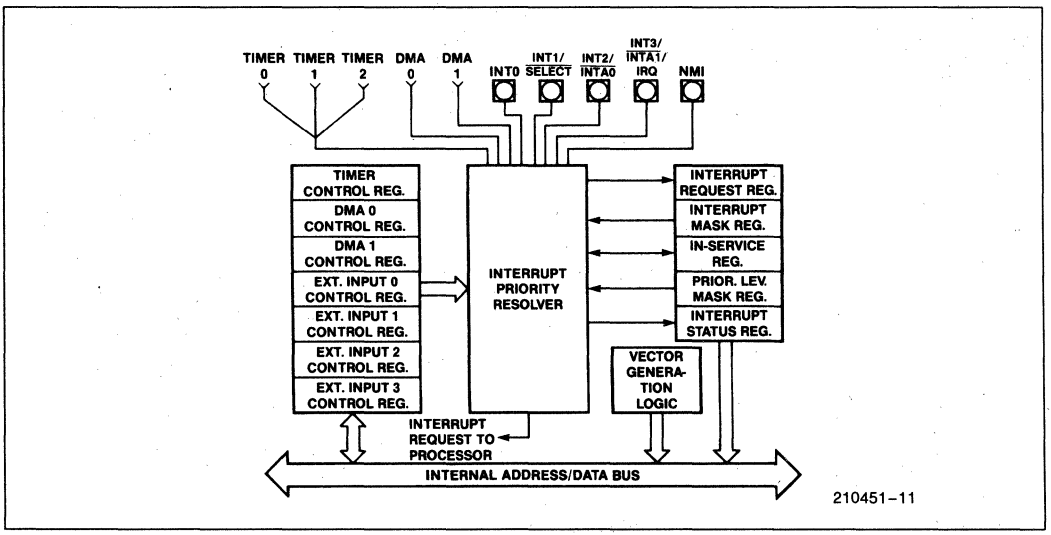

Figure 21. Interrupt Controller Block Diagram

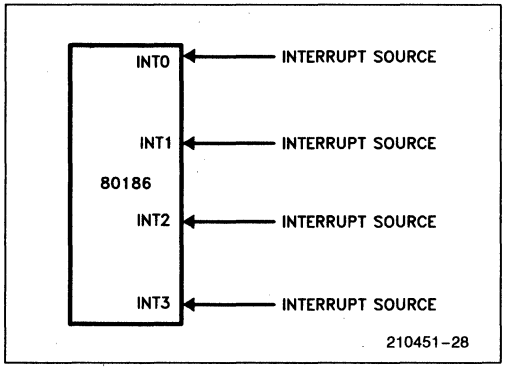

Figure 22. Fully Nested (Direct) Mode Interrupt Controller Connections

Special Fully Nested Mode

This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external 8259A masters. Normally, an interrupt request from an interrupt source will not be recognized unless the in-service bit for that source is reset. If more than one interrupt source is connected to an external interrupt controller, all of the interrupts will be funneled through the same 80186 interrupt request pin. As a result, if the external interrupt controller receives a higher-priority interrupt, its interrupt will not be recognized by the 80186 controller until the 80186 in-service bit is reset. In Special Fully Nested Mode, the 80186 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interrupts from a single pin. An in-service bit will continue to be set, however, to inhibit interrupts from other lower-priority 80186 interrupt sources.

Special procedures should be followed when resetting IS bits at the end of interrupt service routines. Software polling of the IS register in the external master 8259A is required to determine if there is more than one bit set. If so, the IS bit in the 80186 remains active and the next interrupt service routine is entered.

Operation in a Polled Environment

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the Poll Word (Figure 32). Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service. Bits 0–4 indicate to the processor the type vector of the highest-priority source requesting service. Reading the Poll Word causes the In-Service bit of the highest priority source to be set.

It is desirable to be able to read the Poll Word information without guaranteeing service of any pending interrupt, i.e., not set the indicated in-service bit. The 80186 provides a Poll Status Word in addition to the conventional Poll Word to allow this to be done. Poll Word information is duplicated in the Poll Status Word, but reading the Poll Status Word does not set the associated in-service bit. These words are located in two adjacent memory locations in the register file.

Master Mode Features

Programmable Priority

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority). All interrupt sources have preprogrammed default priority levels (see Table 4).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 4 is used. If the serviced interrupt routine reenables interrupts, other interrupt requests can be serviced.

End-of-Interrupt Command

The end-of-interrupt (EOI) command is used by the programmer to reset the In-Service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The nonspecific command does not specify which IS bit is reset. When issued, the interrupt controller automatically resets the IS bit of the highest priority source with an active service routine. A specific EOI command requires that the programmer send the interrupt vector type to the interrupt controller indicating which source's IS bit is to be reset. This command is used when the fully nested structure has been disturbed or the highest priority IS bit that was set does not belong to the service routine in progress.

Trigger Mode

The four external interrupt pins can be programmed in either edge- or level-trigger mode. The control register for each external source has a level-trigger

mode (LTM) bit. All interrupt inputs are active HIGH. In the edge sense mode or the level-trigger mode, the interrupt request must remain active (HIGH) until the interrupt request is acknowledged by the 80186 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go LOW for at least one clock cycle to re-enable the input. In the level-trigger mode, no such provision is made: holding the interrupt input HIGH will cause continuous interrupt requests.

Interrupt Vectoring

The 80186 Interrupt Controller will generate interrupt vectors for the integrated DMA channels and the integrated Timers. In addition, the Interrupt Controller will generate interrupt vectors for the external interrupt lines if they are not configured in Cascade or Special Fully Nested Mode. The interrupt vectors generated are fixed and cannot be changed (see Table 4).

Interrupt Controller Registers

The Interrupt Controller register model is shown in Figure 24. It contains 15 registers. All registers can both be read or written unless specified otherwise.

In-Service Register

This register can be read from or written into. The format is shown in Figure 25. It contains the In-Service bit for each of the interrupt sources. The In-Service bit is set to indicate that a source's service routine is in progress. When an In-Service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the In-Service bit for all three timers; the D0 and D1 bits are the In-Service bits for the two DMA channels; the I0–I3 are the In-Service bits for the external interrupt pins. The IS bit is set when the processor acknowledges an interrupt request either by an interrupt acknowledge or by reading the poll register. The IS bit is reset at the end of the interrupt service routine by an end-of-interrupt command.

Interrupt Request Register

The internal interrupt sources have interrupt request bits inside the interrupt controller. The format of this register is shown in Figure 25. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

The state of the external interrupt input pins is also indicated. The state of the external interrupt pins is not a stored condition inside the interrupt controller, therefore the external interrupt bits cannot be written. The external interrupt request bits are set when an interrupt request is given to the interrupt controller, so if edge-triggered mode is selected, the bit in the register will be HIGH only after an inactive-to-active transition. For internal interrupt sources, the register bits are set when a request arrives and are reset when the processor acknowledges the requests.

Writes to the interrupt request register will affect the D0 and D1 interrupt request bits. Setting either bit will cause the corresponding interrupt request while clearing either bit will remove the corresponding interrupt request. All other bits in the register are read-only.

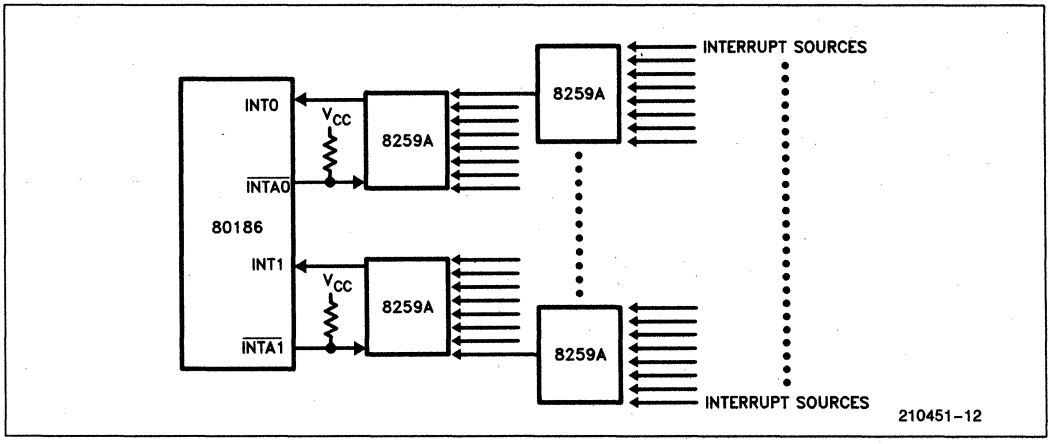

Figure 23. Cascade and Special Fully Nested Mode Interrupt Controller Connections

Mask Register

This is a 16-bit register that contains a mask bit for each interrupt source. The format for this register is shown in Figure 25. A one in a bit position corresponding to a particular source masks the source from generating interrupts. These mask bits are the exact same bits which are used in the individual control registers; programming a mask bit using the mask register will also change this bit in the individual control registers, and vice versa.

	OFFSET
INT3 CONTROL REGISTER	3EH
INT2 CONTROL REGISTER	3CH
INT1 CONTROL REGISTER	3AH
INT0 CONTROL REGISTER	38H
DMA 1 CONTROL REGISTER	36H
DMA 0 CONTROL REGISTER	34H
TIMER CONTROL REGISTER	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY MASK REGISTER	2AH
MASK REGISTER	28H
POLL STATUS REGISTER	26H
POLL REGISTER	24H
EOI REGISTER	22H

Figure 24. Interrupt Controller Registers (Master Mode)

Priority Mask Register

This register masks all interrupts below a particular interrupt priority level. The format of this register is shown in Figure 26. The code in the lower three bits of this register inhibits interrupts of priority lower (a higher priority number) than the code specified. For example, 100 written into this register masks interrupts of level five (101), six (110), and seven (111). The register is reset to seven (111) upon RESET so no interrupts are masked due to priority number.

Interrupt Status Register

This register contains general interrupt controller status information. The format of this register is shown in Figure 27. The bits in the status register have the following functions:

DHLT: DMA Halt Transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed. This bit allows prompt service of all non-maskable interrupts. This bit may also be set by the programmer.

IRTx: These three bits represent the individual timer interrupt request bits. These bits differentiate between timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt request. Note that setting any one of these three bits initiates an interrupt request to the interrupt controller.

15	14	•	•	•	10	9	8	7	6	5	4	3	2	1	0
0	0	•	•	•	0	0	0	I3	I2	I1	I0	D1	D0	0	TMR

Figure 25. In-Service, Interrupt Request, and Mask Register Formats

15	14	•	•	•	•	•	•	•	•	•	3	2	1	0
0	0	•	•	•	•	•	•	•	•	•	0	PRM2	PRM1	PRM0

Figure 26. Priority Mask Register Format

15	14	•	•	•	•	•	7	6	5	4	3	2	1	0
DHLT	0	•	•	•	•	•	0	0	0	0	0	IRT2	IRT1	IRT0

Figure 27. Interrupt Status Register Format (Master Mode)

Timer, DMA 0, 1; Control Register

These registers are the control words for all the internal interrupt sources. The format for these registers is shown in Figure 28. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits interrupt requests from the interrupt source. The MSK bits in the individual control registers are the exact same bits as are in the Mask Register; modifying them in the individual control registers will also modify them in the Mask Register, and vice versa.

INT0-INT3 Control Registers

These registers are the control words for the four external input pins. Figure 29 shows the format of the INT0 and INT1 Control registers; Figure 30 shows the format of the INT2 and INT3 Control registers. In Cascade Mode or Special Fully Nested Mode, the control words for INT2 and INT3 are not used.

The bits in the various control registers are encoded as follows:

PRO-2: Priority programming information. Highest Priority = 000, Lowest Priority = 111

LTM: Level-trigger mode bit. 1 = level-triggered; 0 = edge-triggered. Interrupt Input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = non-mask.

C: Cascade mode bit, 1 = cascade; 0 = direct

SFNM: Special Fully Nested Mode bit, 1 = SFNM

EOI Register

The end of the interrupt register is a command register which can only be written into. The format of this register is shown in Figure 31. It initiates an EOI command when written to by the 80186 CPU.

The bits in the EOI register are encoded as follows:

S_x: Encoded information that specifies an interrupt source vector type as shown in Table 4. For example, to reset the In-Service bit for DMA channel 0, these bits should be set to 01010, since the vector type for DMA channel 0 is 10.

NOTE:

To reset the single In-Service bit for any of the three timers, the vector type for timer 0 (8) should be written in this register.

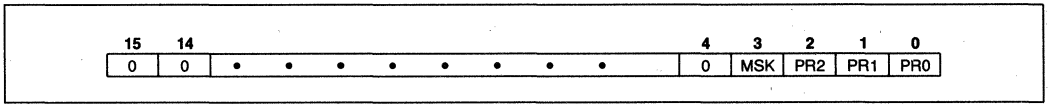

Figure 28. Timer/DMA Control Registers Formats

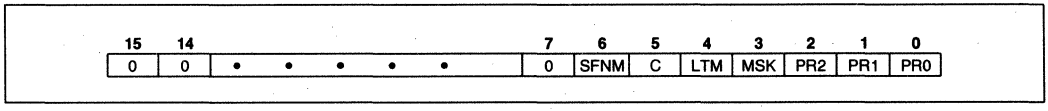

Figure 29. INT0/INT1 Control Register Formats

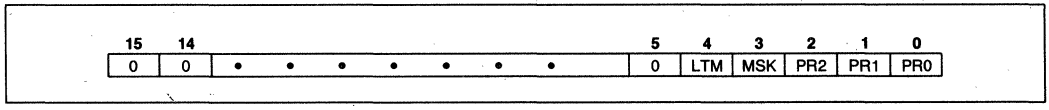

Figure 30. INT2/INT3 Control Register Formats

NSPEC/SPEC: A bit that determines the type of EOI command. Nonspecific = 1, Specific = 0.

Poll and Poll Status Registers

These registers contain polling information. The format of these registers is shown in Figure 32. They can only be read. Reading the Poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt. Reading the poll status register will not set the IS bit of the highest priority pending interrupt; only the status of pending interrupts will be provided.

Encoding of the Poll and Poll Status register bits are as follows:

S_X: Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt Request = 1; no Interrupt Request = 0.

SLAVE MODE OPERATION

When Slave Mode is used, the internal 80186 interrupt controller will be used as a slave controller to an external master interrupt controller. The internal 80186 resources will be monitored by the internal interrupt controller, while the external controller functions as the system master interrupt controller. Upon reset, the 80186 will be in Master Mode. To provide for slave mode operation bit 14 of the relocation register should be set.

Because of pin limitations caused by the need to interface to an external 8259A master, the internal interrupt controller will no longer accept external inputs. There are however, enough 80186 interrupt controller inputs (internally) to dedicate one to each timer. In this mode, each timer interrupt source has its own mask bit, IS bit, and control word.

In Slave Mode each peripheral must be assigned a unique priority to ensure proper interrupt controller operation. Therefore, it is the programmer's responsibility to assign correct priorities and initialize interrupt control registers before enabling interrupts.

These level assignments must remain fixed in the Slave Mode of operation.

Slave Mode External Interface

The configuration of the 80186 with respect to an external 8259A master is shown in Figure 33. The INT0 (pin 45) input is used as the 80186 CPU interrupt input. IRQ (pin 41) functions as an output to send the 80186 slave-interrupt-request to one of the 8 master-PIC-inputs.

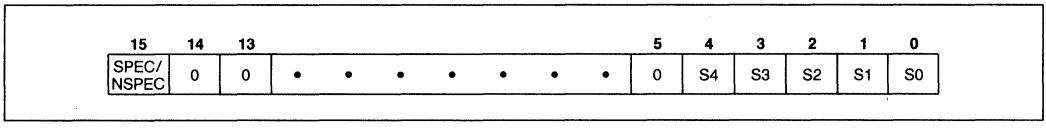

Figure 31. EOI Register Format

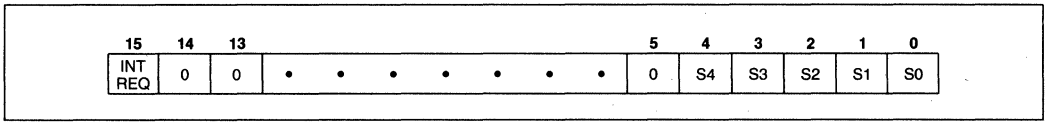

Figure 32. Poll and Poll Status Register Format

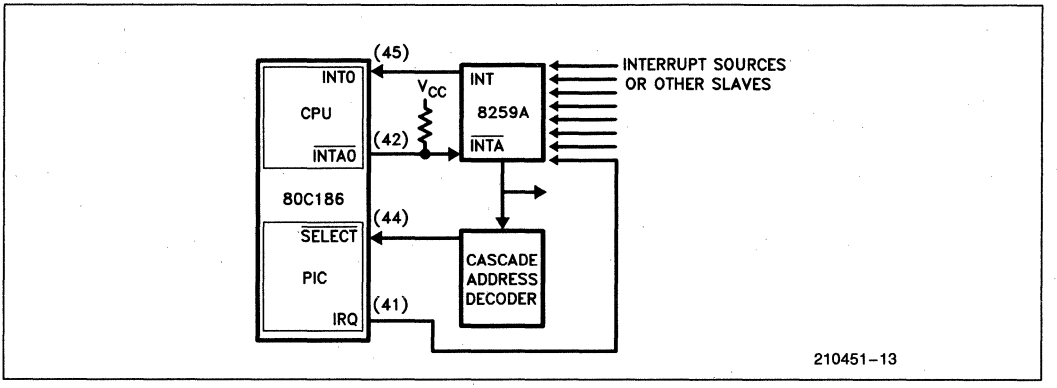

Figure 33. Slave Mode Interrupt Controller Connections

Correct master-slave interface requires decoding of the slave addresses (CAS0-2). Slave 8259As do this internally. Because of pin limitations, the 80186 slave address will have to be decoded externally. $\overline{\text{SELECT}}$ (pin 44) is used as a slave-select input. Note that the slave vector address is transferred internally, but the READY input must be supplied externally.

$\overline{\text{INTA0}}$ (pin 42) is used as an acknowledge output, suitable to drive the $\overline{\text{INTA}}$ input of an 8259A.

Interrupt Nesting

Slave Mode operation allows nesting of interrupt requests. When an interrupt is acknowledged, the priority logic masks off all priority levels except those with equal or higher priority.

Vector Generation in the Slave Mode

Vector generation in Slave Mode is exactly like that of an 8259A or 82C59A slave. The interrupt controller generates an 8-bit vector type number which the CPU multiplies by four to use as an address into the vector table. The five most significant bits of this type number are user-programmable while the three least significant bits are defined according to Figure 34. The significant five bits of the vector are programmed by writing to the Interrupt Vector register at offset 20H.

Specific End-of-Interrupt

In Slave Mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset. The command is executed by writing the correct value in the Specific EOI register at offset 22H.

Interrupt Controller Registers in the Slave Mode

All control and command registers are located inside the internal peripheral control block. Figure 34 shows the offsets of these registers.

End-of-Interrupt Register

The end-of-interrupt register is a command register which can only be written. The format of this register is shown in Figure 35. It initiates an EOI command when written by the 80186 CPU.

The bits in the EOI register are encoded as follows:

VT_X: Three least-significant vector type bits corresponding to the source for which the IS bit is to be reset. Figure 34 indicates these bits.

In-Service Register

This register can be read from or written into. It contains the in-service bit for each of the internal interrupt sources. The format for this register is shown in Figure 36. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers. The source's IS bit is set when the processor acknowledges its interrupt request.

Interrupt Request Register

This register indicates which internal peripherals have interrupt requests pending. The format of this register is shown in Figure 36. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request. As in Master Mode, D0 and D1 are read/write; all other bits are read only.

Mask Register

This register contains a mask bit for each interrupt source. The format for this register is shown in Figure 36. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked. These mask bits are exactly the same bits which are used in the individual control registers, i.e., changing the state of a mask bit in this register will also change the state of the mask bit in the individual interrupt control register corresponding to the bit.

Control Registers

These registers are the control words for all the internal interrupt sources. The format of these registers is shown in Figure 37. Each of the timers and both of the DMA channels have their own Control Register.

The bits of the Control Registers are encoded as follows:

pr_x: 3-bit encoded field indicating a priority level for the source.

msk: mask bit for the priority level indicated by pr_x bits.

	OFFSET
TIMER2 CONTROL REGISTER (VECTOR TYPE xxxxx101)	3AH
TIMER1 CONTROL REGISTER (VECTOR TYPE xxxxx100)	38H
DMA1 CONTROL REGISTER (VECTOR TYPE xxxxx011)	36H
DMA0 CONTROL REGISTER (VECTOR TYPE xxxxx010)	34H
TIMER0 CONTROL REGISTER (VECTOR TYPE xxxxx000)	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT-REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY-LEVEL MASK REGISTER	2AH
MASK REGISTER	28H
SPECIFIC EOI REGISTER	22H
INTERRUPT VECTOR REGISTER	20H

Figure 34. Interrupt Controller Registers (Slave Mode)

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15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	0	0	0	VT2	VT1	VT0

Figure 35. Specific EOI Register Format

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	TMR2	TMR1	D1	D0	0	TMR0

Figure 36. In-Service, Interrupt Request, and Mask Register Format

Interrupt Vector Register

This register provides the upper five bits of the interrupt vector address. The format of this register is shown in Figure 38. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.

The format of the bits in this register is:

t_x: 5-bit field indicating the upper five bits of the vector address.

Priority-Level Mask Register

This register indicates the lowest priority-level interrupt which will be serviced.

The encoding of the bits in this register is:

m_x: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

Interrupt Status Register

This register is defined as in Master Mode except that DHLT is not implemented. (See Figure 27).

Interrupt Controller and Reset

Upon RESET, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying Fully Nested Mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All Interrupt Service bits reset to 0.
- All Interrupt Request bits reset to 0.
- All MSK (Interrupt Mask) bits set to 1 (mask).
- All C (Cascade) bits reset to 0 (non-Cascade).
- All PRM (Priority Mask) bits set to 1, implying no levels masked.
- Initialized to Master Mode.

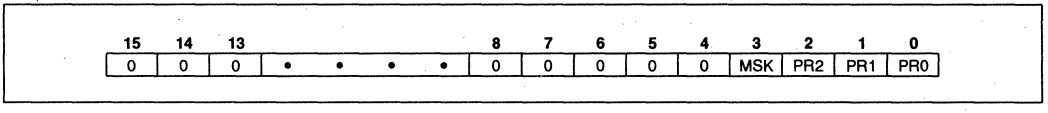

Figure 37. Control Word Format

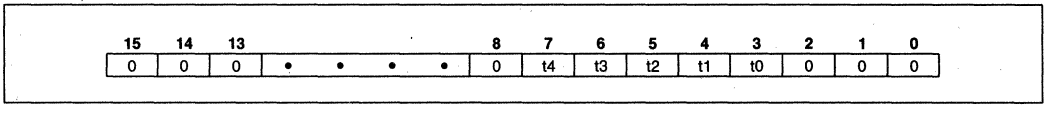

Figure 38. Interrupt Vector Register Format

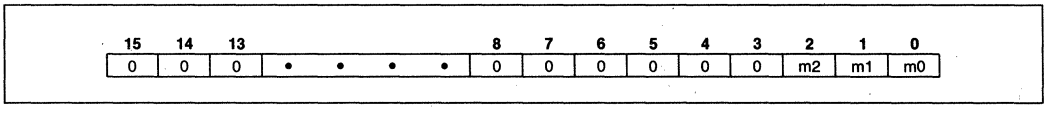

Figure 39. Priority Level Mask Register

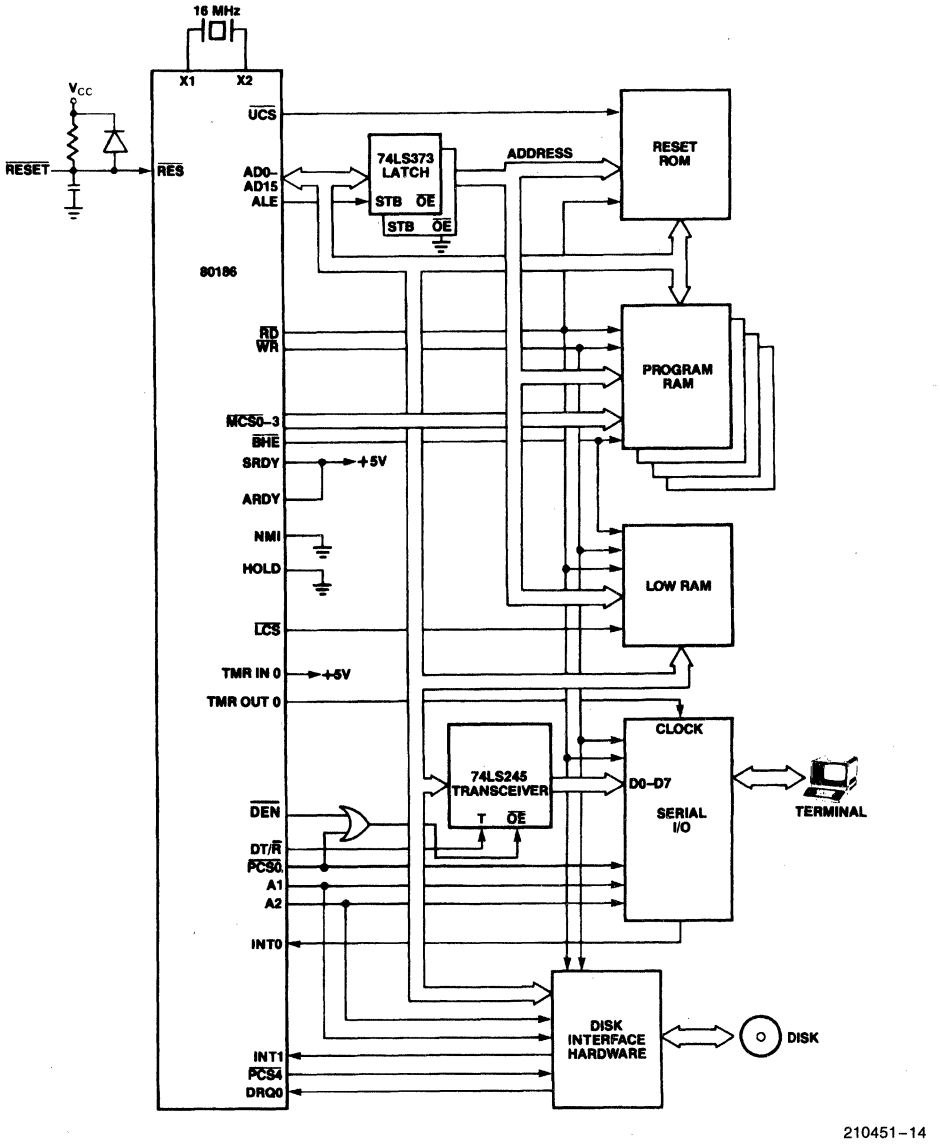

Figure 40. Typical 80186 Computer

24

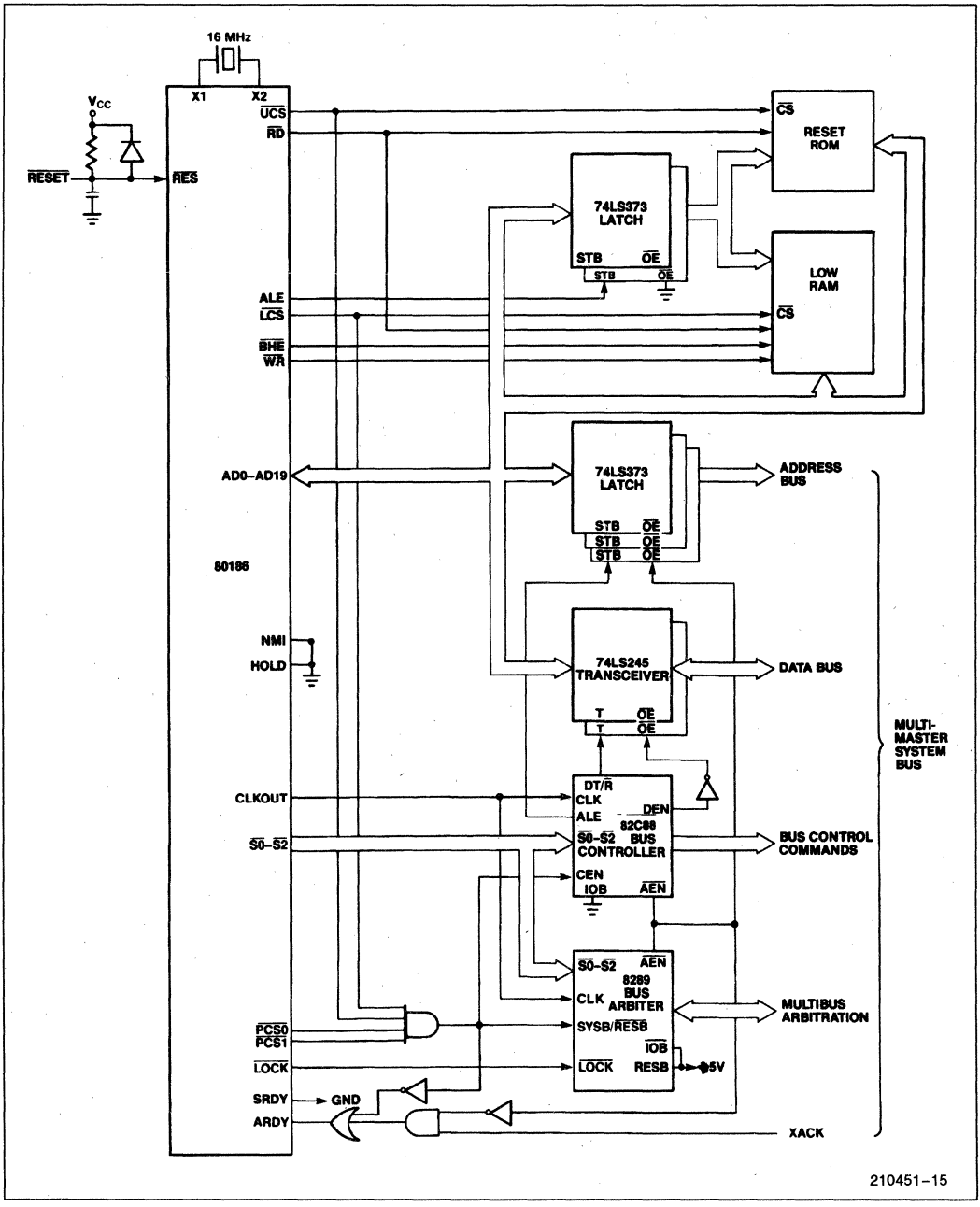

Figure 41. Typical 80186 Multi-Master Bus Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on any Pin with
Respect to Ground.....−1.0V to +7V
Power Dissipation 3W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

Applicable to 80186 (8 MHz), 80186-10 (10 MHz).

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage (All except X1 and $\overline{RES}$)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_a = 2.5 mA for $\overline{S0}$–$\overline{S2}$ I_a = 2.0 mA for all other Outputs
V_{OH}	Output High Voltage	2.4		V	I_{oa} = −400 μA
I_{CC}	Power Supply Current		600*	mA	T_A = −40°C
			550	mA	T_A = 0°C
			415	mA	T_A = +70°C
I_{LI}	Input Leakage Current		±10	μA	0V < V_{IN} < V_{CC}
I_{LO}	Output Leakage Current		±10	μA	0.45V < V_{OUT} < V_{CC}
V_{CLO}	Clock Output Low		0.6	V	I_a = 4.0 mA
V_{CHO}	Clock Output High	4.0		V	I_{oa} = −200 μA
V_{CLI}	Clock Input Low Voltage	−0.5	0.6	V	
V_{CHI}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		20	pF	

*For extended temperature parts only.

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PIN TIMINGS

A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

80186 Timing Requirements All Timings Measured At 1.5V Unless Otherwise Noted.

Symbol	Parameter	80186 (8 MHz)		80186-10 (10 MHz)		Units	Test Conditions
		Min	Max	Min	Max		
T_{DVCL}	Data in Setup (A/D)	20		15		ns	
T_{CLDX}	Data in Hold (A/D)	10		8		ns	
T_{ARYHCH}	Asynchronous Ready (ARDY) Active Setup Time (1)	20		15		ns	
T_{ARYLCL}	ARDY Inactive Setup Time	35		25		ns	
T_{CLARX}	ARDY Hold Time	15		15		ns	
T_{ARYCHL}	Asynchronous Ready Inactive Hold Time	15		15		ns	
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time (2)	20		20		ns	
T_{CLSRY}	SRDY Transition Hold Time (2)	15		15		ns	
T_{HVCL}	HOLD Setup (1)	25		20		ns	
T_{INVCH}	INTR, NMI, $\overline{TEST}$, TIM IN, Setup (1)	25		25		ns	
T_{INVCL}	DRQ0, DRQ1, Setup (1)	25		20		ns	
80186 Master Interface Timing Responses							
T_{CLAV}	Address Valid Delay	5	55	5	44	ns	C_L = 20–200 pF all Outputs (Except T_{CLTMV}) @ 8 & 10 MHz
T_{CLAX}	Address Hold	10		10		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	35	T_{CLAX}	30	ns	
T_{CHCZ}	Command Lines Float Delay		45		40	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		55		45	ns	
T_{LHLL}	ALE Width	$T_{CLCL}-35$		$T_{CLCL}-30$		ns	
T_{CHLH}	ALE Active Delay		35		30	ns	
T_{CHLL}	ALE Inactive Delay		35		30	ns	
T_{LLAX}	Address Hold from ALE Inactive	$T_{CHCL}-25$		$T_{CHCL}-20$		ns	
T_{CLDV}	Data Valid Delay	10	44	10	40	ns	
T_{CLDOX}	Data Hold Time	10		10		ns	
T_{WHDX}	Data Hold after WR	$T_{CLCL}-40$		$T_{CLCL}-34$		ns	
T_{CVCTV}	Control Active Delay 1	5	50	5	40	ns	
T_{CHCTV}	Control Active Delay 2	10	55	10	44	ns	
T_{CVCTX}	Control Inactive Delay	5	55	5	44	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycle)	10	70	10	56	ns	

1. To guarantee recognition at next clock.
2. To guarantee proper operation.

PIN TIMINGS (Continued)

A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ±10%) (Continued)

80186 Master Interface Timing Responses (Continued)

Symbol	Parameter	80186 (8 MHz)		80186-10 (10 MHz)		Units	Test Conditions
		Min	Max	Min	Max		
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	10	70	10	56	ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	10	55	10	44	ns	
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	$T_{CLCL}-40$		$T_{CLCL}-40$		ns	
T_{CLHAV}	HLDA Valid Delay	5	50	5	40	ns	
T_{RLRH}	$\overline{RD}$ Width	$2T_{CLCL}-50$		$2T_{CLCL}-46$		ns	
T_{WLWH}	$\overline{WR}$ Width	$2T_{CLCL}-40$		$2T_{CLCL}-34$		ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH}-25$		$T_{CLCH}-19$		ns	
T_{CHSV}	Status Active Delay	10	55	10	45	ns	
T_{CLSH}	Status Inactive Delay	10	65	10	50	ns	
T_{CLTMV}	Timer Output Delay		60		48	ns	100 pF max @ 8 & 10 MHz
T_{CLRO}	Reset Delay		60		48	ns	
T_{CHQSV}	Queue Status Delay		35		28	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{AVCH}	Address Valid to Clock High	10		10		ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	5	65	5	60	ns	
80186 Chip-Select Timing Responses							
T_{CLCSV}	Chip-Select Active Delay		66		45	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	35		35		ns	
T_{CHCSX}	Chip-Select Inactive Delay	5	35	5	32	ns	
80186 CLKIN Requirements							
T_{CKIN}	CLKIN Period	62.5	250	50	250	ns	
T_{CKHL}	CLKIN Fall Time		10		10	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		10		10	ns	1.0 to 3.5V
T_{CLCK}	CLKIN Low Time	25		20		ns	1.5V
T_{CHCK}	CLKIN High Time	25		20		ns	1.5V
80186 CLKOUT Timing (200 pF load)							
T_{CICO}	CLKIN to CLKOUT Skew		50		25	ns	
T_{CLCL}	CLKOUT Period	125	500	100	500	ns	
T_{CLCH}	CLKOUT Low Time	$\frac{1}{2}T_{CLCL}-7.5$		$\frac{1}{2}T_{CLCL}-6.0$		ns	1.5V
T_{CHCL}	CLKOUT High Time	$\frac{1}{2}T_{CLCL}-7.5$		$\frac{1}{2}T_{CLCL}-6.0$		ns	1.5V
T_{CH1CH2}	CLKOUT Rise Time		15		12	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		15		12	ns	3.5 to 1.0V

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has from 5 to 7 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

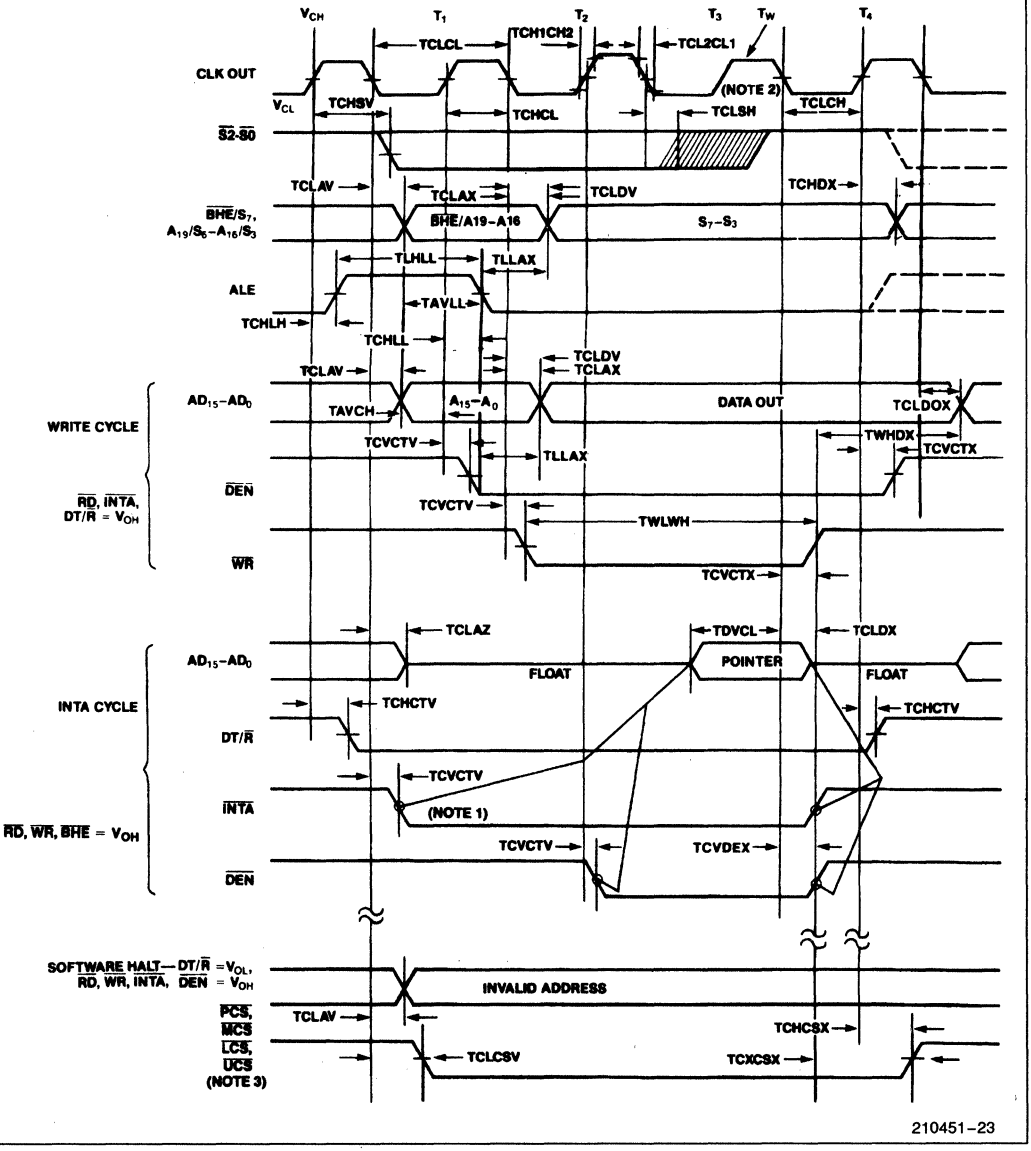
A: Address
ARY: Asynchronous Ready Input
C: Clock Output
CK: Clock Input
CS: Chip Select
CT: Control (DT/$\overline{R}$, $\overline{DEN}$, . . .)
D: Data Input
DE: $\overline{DEN}$
H: Logic Level High
IN: Input (DRQ0, TIM0, . . .)
L: Logic Level Low or ALE
O: Output
QS: Queue Status (QS1, QS2)
R: $\overline{RD}$ signal, $\overline{RESET}$ signal
S: Status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$)
SRY: Synchronous Ready Input
V: Valid
W: WR Signal
X: No Longer a Valid Logic Level
Z: Float

Examples:

T_{CLAV} — Time from Clock low to Address valid
T_{CHLH} — Time from Clock high to ALE high
T_{CLCSV} — Time from Clock low to Chip Select valid

WAVEFORMS

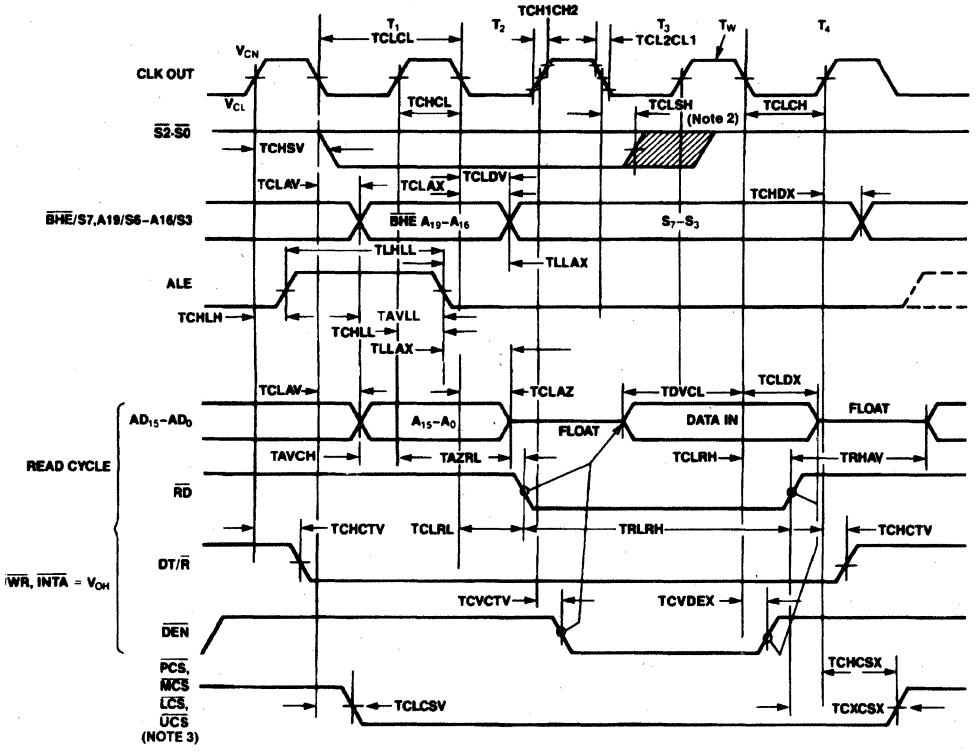
MAJOR CYCLE TIMING



210451-23

WAVEFORMS (Continued)

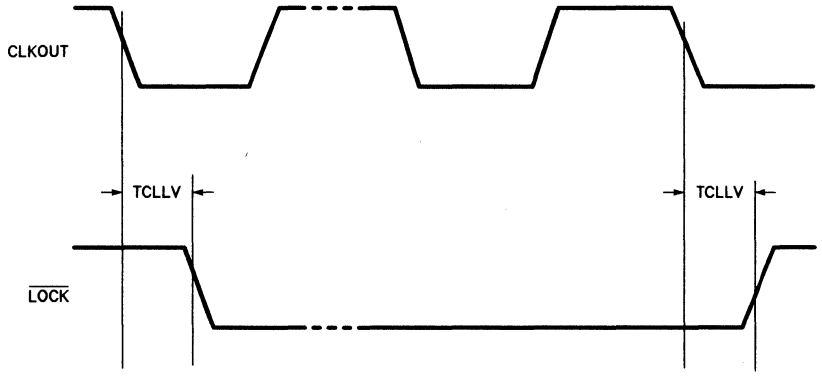
MAJOR CYCLE TIMING (Continued)



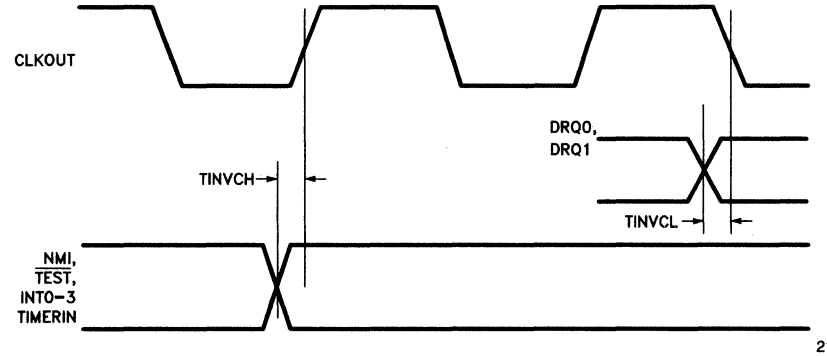
210451-24

NOTES:
1. INTA occurs one clock later in slave mode.
2. Status inactive just prior to T_4.
3. If latched A1 and A2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.

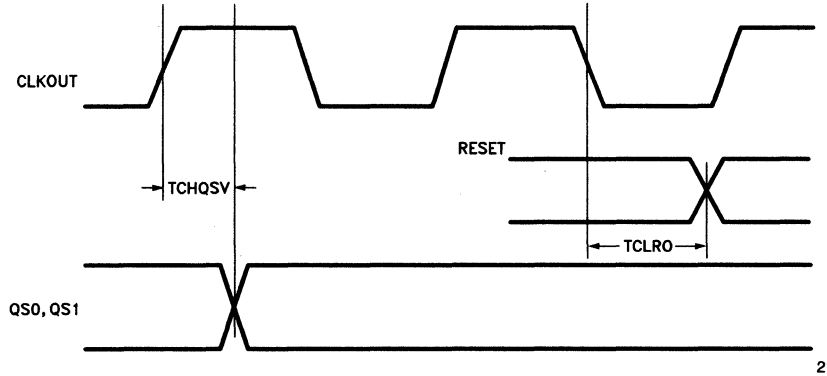
WAVEFORMS (Continued)



210451-30

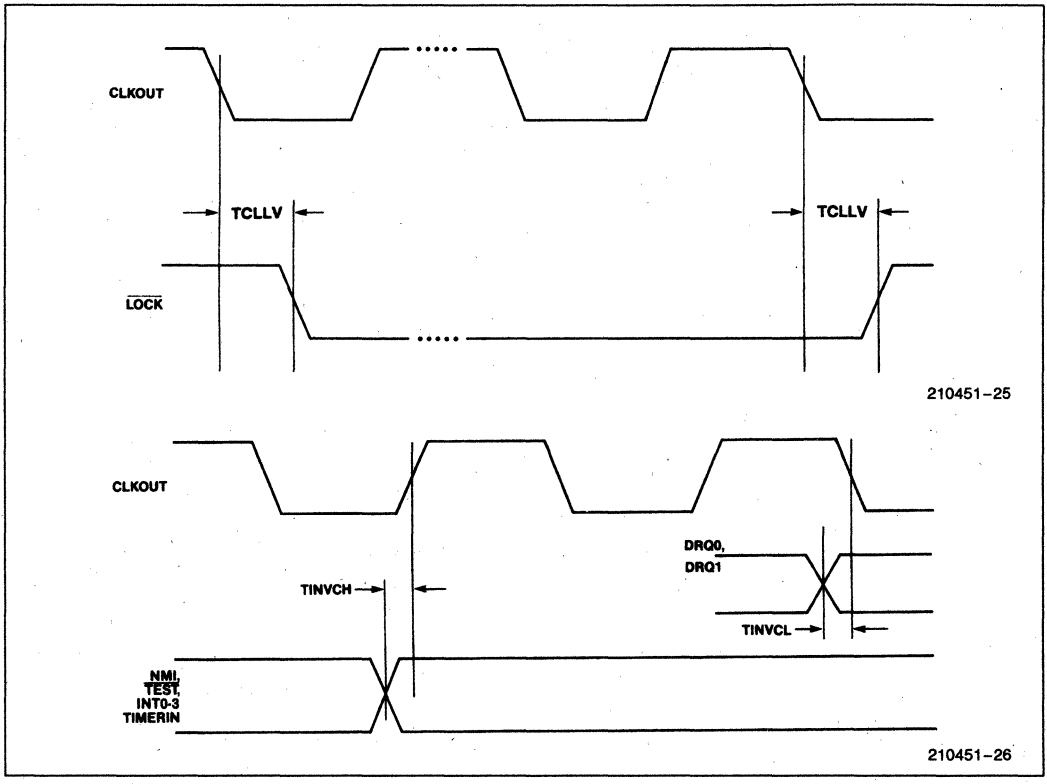


210451-31



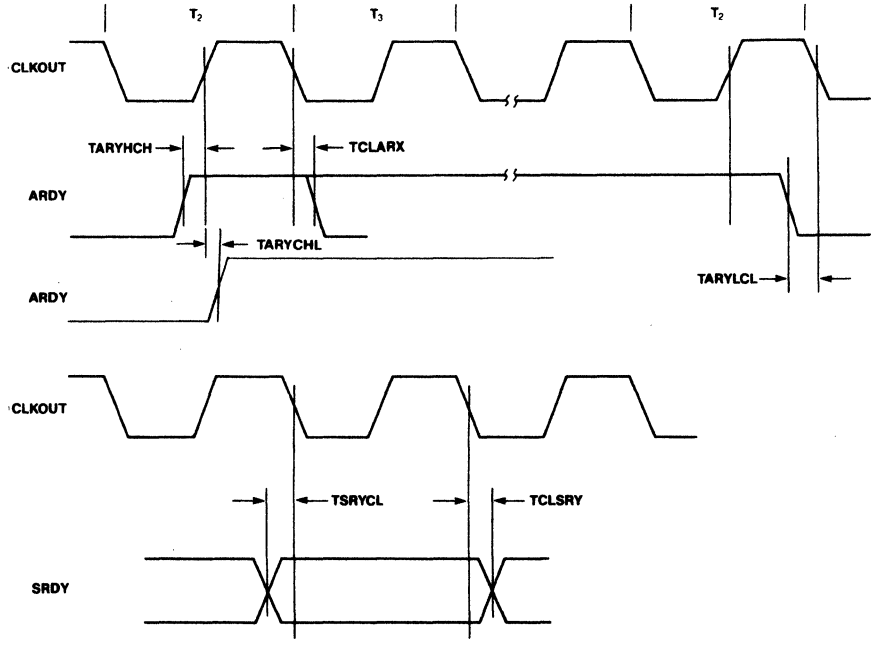
210451-32

WAVEFORMS (Continued)



WAVEFORMS (Continued)

READY TIMING



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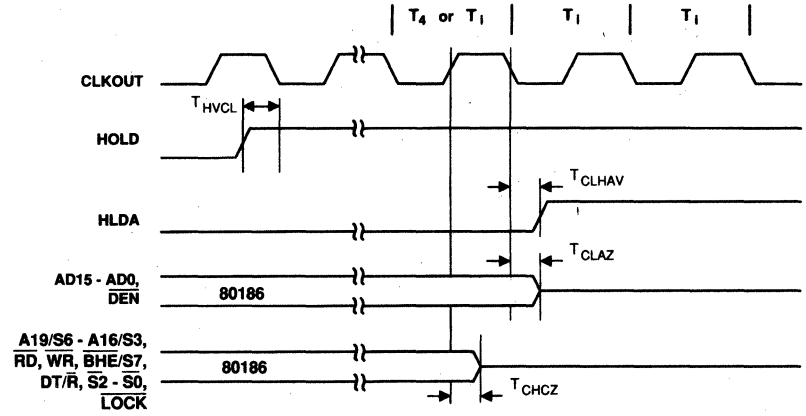
WAVEFORMS (Continued)

HOLD/HLDA TIMING (Entering Hold)



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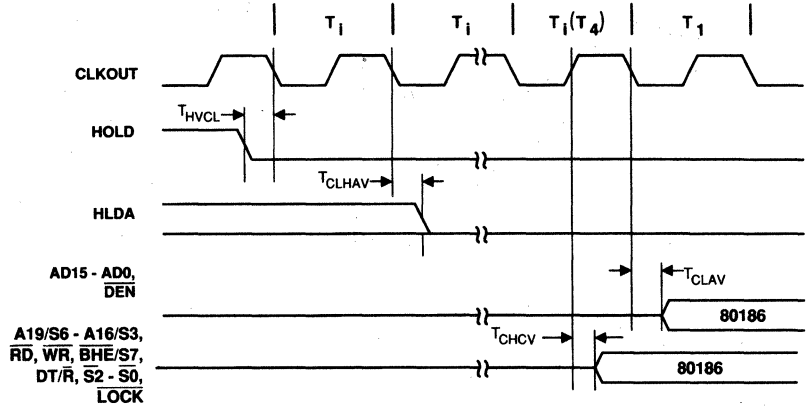
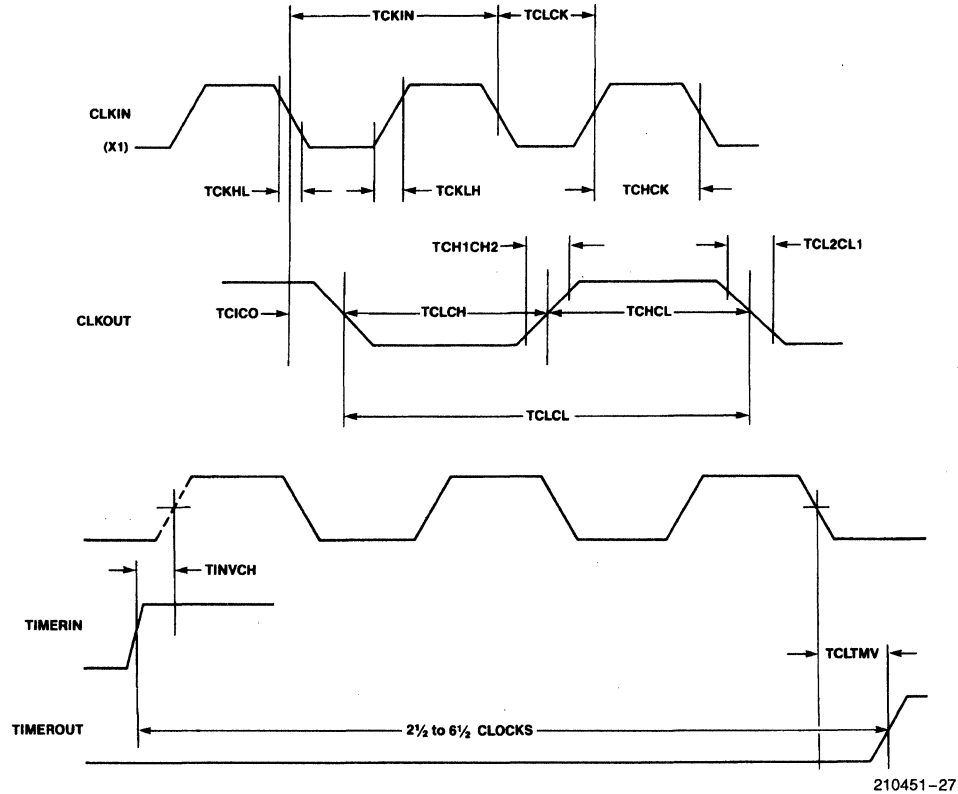
HOLD/HLDA TIMING (Leaving Hold)



210451-34

WAVEFORMS (Continued)

TIMER ON 80186



210451-27

80186 EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the 80186 microprocessor. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range without burn-in.

With the commercial standard temperature range operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic, for a minimum time of 160 hours at +125°C with V_{CC} = 5.5V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 16. All A.C. and D.C. specifications not mentioned in this section are the same for both commercial and EXPRESS parts.

Table 16. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
A	PGA	Commercial	No
N	PLCC	Commercial	No
R	LCC	Commercial	No
TA	PGA	Extended	No
QA	PGA	Commercial	Yes
QR	LCC	Commercial	Yes

NOTE:
Not all package/temperature range/speed combinations are available.

80186 EXECUTION TIMINGS

A determination of 80186 program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDS occur.
- All word-data is located on even-address boundaries.

All instructions which involve memory accesses can also require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

With a 16-bit BIU, the 80186 has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format	Clock Cycles	Comments
DATA TRANSFER			
MOV = Move:			
Register to Register/Memory	1000100w mod reg r/m	2/12	
Register/memory to register	1000101w mod reg r/m	2/9	
Immediate to register/memory	1100011w mod 000 r/m data data if w=1	12–13	8/16-bit
Immediate to register	1011w reg data data if w=1	3–4	8/16-bit
Memory to accumulator	1010000w addr-low addr-high	8	
Accumulator to memory	1010001w addr-low addr-high	9	
Register/memory to segment register	10001110 mod 0 reg r/m	2/9	
Segment register to register/memory	10001100 mod 0 reg r/m	2/11	
PUSH = Push:			
Memory	11111111 mod 110 r/m	16	
Register	01010 reg	10	
Segment register	000reg110	9	
Immediate	011010s0 data data if s=0	10	
PUSHA = Push All	01100000	36	
POP = Pop:			
Memory	10001111 mod 000 r/m	20	
Register	01011 reg	10	
Segment register	000reg111 (reg≠01)	8	
POPA = Pop All	01100001	51	
XCHG = Exchange:			
Register/memory with register	1000011w mod reg r/m	4/17	
Register with accumulator	10010 reg	3	
IN = Input from:			
Fixed port	1110010w port	10	
Variable port	1110110w	8	
OUT = Output to:			
Fixed port	1110011w port	9	
Variable port	1110111w	7	
XLAT = Translate byte to AL	11010111	11	
LEA = Load EA to register	10001101 mod reg r/m	6	
LDS = Load pointer to DS	11000101 mod reg r/m (mod≠11)	18	
LES = Load pointer to ES	11000100 mod reg r/m (mod≠11)	18	
LAHF = Load AH with flags	10011111	2	
SAHF = Store AH into flags	10011110	3	
PUSHF = Push flags	10011100	9	
POPF = Pop flags	10011101	8	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10	
Register with register/memory	0011100w	mod reg r/m			3/10	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26–28	
Register-Word					35–37	
Memory-Byte					32–34	
Memory-Word					41–43	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
ARITHMETIC (Continued)						
IMUL = Integer multiply (signed):	1111011w	mod101 r/m				
Register-Byte					25–28	
Register-Word					34–37	
Memory-Byte					31–34	
Memory-Word					40–43	
IMUL = Integer Immediate multiply (signed)	011010s1	mod reg r/m	data	data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w	mod110 r/m				
Register-Byte					29	
Register-Word					38	
Memory-Byte					35	
Memory-Word					44	
IDIV = Integer divide (signed):	1111011w	mod111 r/m				
Register-Byte					44–52	
Register-Word					53–61	
Memory-Byte					50–58	
Memory-Word					59–67	
AAM = ASCII adjust for multiply	11010100	00001010			19	
AAD = ASCII adjust for divide	11010101	00001010			15	
CBW = Convert byte to word	10011000				2	
CWD = Convert word to double word	10011001				4	
LOGIC						
Shift/Rotate Instructions:						
Register/Memory by 1	1101000w	mod TTT r/m			2/15	
Register/Memory by CL	1101001w	mod TTT r/m			5+n/17+n	
Register/Memory by Count	1100000w	mod TTT r/m	count		5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR					
AND = **And:**						
Reg/memory and register to either	001000dw	mod reg r/m			3/10	
Immediate to register/memory	1000000w	mod100 r/m	data	data if w=1	4/16	
Immediate to accumulator	0010010w	data	data if w=1		3/4	8/16-bit
TEST = **And function to flags, no result:**						
Register/memory and register	1000010w	mod reg r/m			3/10	
Immediate data and register/memory	1111011w	mod000 r/m	data	data if w=1	4/10	
Immediate data and accumulator	1010100w	data	data if w=1		3/4	8/16-bit
OR = **Or:**						
Reg/memory and register to either	000010dw	mod reg r/m			3/10	
Immediate to register/memory	1000000w	mod001 r/m	data	data if w=1	4/16	
Immediate to accumulator	0000110w	data	data if w=1		3/4	8/16-bit

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
XOR = Exclusive or:						
Reg/memory and register to either	001100dw	mod reg r/m			3/10	
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	4/16	
Immediate to accumulator	0011010w	data	data if w=1		3/4	8/16-bit
NOT = Invert register/memory	1111011w	mod 010 r/m			3/10	
STRING MANIPULATION						
MOVS = Move byte/word	1010010w				14	
CMPS = Compare byte/word	1010011w				22	
SCAS = Scan byte/word	1010111w				15	
LODS = Load byte/wd to AL/AX	1010110w				12	
STOS = Store byte/wd from AL/AX	1010101w				10	
INS = Input byte/wd from DX port	0110110w				14	
OUTS = Output byte/wd to DX port	0110111w				14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	11110010	1010010w			8+8n	
CMPS = Compare string	1111001z	1010011w			5+22n	
SCAS = Scan string	1111001z	1010111w			5+15n	
LODS = Load string	11110010	1010110w			6+11n	
STOS = Store string	11110010	1010101w			6+9n	
INS = Input string	11110010	0110110w			8+8n	
OUTS = Output string	11110010	0110111w			8+8n	
CONTROL TRANSFER						
CALL = Call:						
Direct within segment	11101000	disp-low	disp-high		15	
Register/memory indirect within segment	11111111	mod 010 r/m			13/19	
Direct intersegment	10011010	segment offset			23	
		segment selector				
Indirect intersegment	11111111	mod 011 r/m	(mod ≠ 11)		38	
JMP = Unconditional jump:						
Short/long	11101011	disp-low			14	
Direct within segment	11101001	disp-low	disp-high		14	
Register/memory indirect within segment	11111111	mod 100 r/m			11/17	
Direct intersegment	11101010	segment offset			14	
		segment selector				
Indirect intersegment	11111111	mod 101 r/m	(mod ≠ 11)		26	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
RET = **Return from CALL:**						
Within segment	11000011				16	
Within seg adding immed to SP	11000010	data-low	data-high		18	
Intersegment	11001011				22	
Intersegment adding immediate to SP	11001010	data-low	data-high		25	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22 + 16(n − 1)	
LEAVE = Leave Procedure	11001001				8	
INT = **Interrupt:**						
Type specified	11001101	type			47	
Type 3	11001100				45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110				48/4	
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33–35	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
ESC = Processor Extension Escape	11011TTT mod LLL r/m (TTT LLL are opcode to processor extension)	6	
NOP = No Operation	10010000	3	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

REVISION HISTORY

The sections significantly revised since version -010 are:

Pin Description Table	Added note to $\overline{TEST}$ pin requiring proper RESET at power-up to configure pin as input.
	Renamed pin 44 to INT1/$\overline{SELECT}$ and pin 41 to INT3/$\overline{INTA}$1/IRQ to better describe their functions in Slave Mode.
Initialization and Processor Reset	Added reminder to drive$\overline{RES}$ pin LOW during power-up.
Major Cycle Timing Waveform	Clarified applicability of T_{CLCSV} to latched A1 and A2 in footnote.
HOLD/HLDA Timing Waveforms	Redrawn to indicate correct relationship of HOLD inactive to HLDA inactive.
Slave Mode Operation	The three low order bits associated with vector generation and performing EOI are not alterable; however, the priority levels are programmable. This information is a clarification only.

The sections significantly revised since version -009 are:

Pin Description Table	Various descriptions rewritten for clarity.
Interrupt Vector Table	Redrawn for clarity.
A.C. Characteristics	Added reminder that T_{SRYCL} and T_{CLSRY} must be met.
Explanation of the A.C. Symbols	New section.
Major Cycle Timing Waveforms	T_{CLRO} indicated.

The sections significantly revised since version -008 are:

Pin Description Table	Noted $\overline{RES}$ to be low more than 4 clocks. Connections to X1 and X2 clarified.
DMA Control Bit Descriptions	Moved and clarified note concerning TC condition for ST/$\overline{STOP}$ clearing during unsynchronized transfers.
Interrupt Controller, etc.	Renamed iRMX Mode to Slave Mode.
Interrupt Request Register	Noted that D0 and D1 are read/write, others read-only.
Execution Timings	Effect of bus width clarified.

The sections significantly revised since the October, 1986 version -007 are:

A.C. Characteristics	Deleted column for 12.5 MHz devices. Intel never marketed a 12.5 MHz 80186.

The sections significantly revised since the February, 1986 version -007 are:

A.C. Characteristics	Several timings changed in anticipation of test change (all listed in ns): T_{CLAV} (min.) at 10 MHz from 50 to 44; T_{CVCTV} (min.) at 8 MHz from 10 to 5; T_{CVCTV} (max.) from 70 to 50 at 8 MHz and 56 to 40 at 10 MHz.

80C186
CHMOS HIGH INTEGRATION 16-BIT MICROPROCESSOR

- **Operation Modes Include:**
  - **Enhanced Mode Which Has**
    - **DRAM Refresh Control Unit**
    - **Power-Save Mode**
    - **Direct Interface to New Numerics Coprocessor**
  - **Compatible Mode**
    - **NMOS 80186 Pin-for-Pin Replacement for Non-Numerics Applications**
- **Integrated Feature Set**
  - **Enhanced 80C86/C88 CPU**
  - **Clock Generator**
  - **2 Independent DMA Channels**
  - **Programmable Interrupt Controller**
  - **3 Programmable 16-Bit Timers**
  - **Dynamic RAM Refresh Control Unit**
  - **Programmable Memory and Peripheral Chip Select Logic**
  - **Programmable Wait State Generator**
  - **Local Bus Controller**
  - **Power Save Mode**
  - **System-Level Testing Support (High Impedance Test Mode)**
- **Available in 16 MHz (80C186-16), 12.5 MHz (80C186-12) and 10 MHz (80C186) Versions**
- **Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O**
- **Completely Object Code Compatible with All Existing 8086/8088 Software and Also Has 10 Additional Instructions Over 8086/8088**
- **Complete System Development Support**
  - **All 8086 and NMOS 80186 Software Development Tools Can Be Used for 80C186 System Development**
    - **ASM 86 Assembler, PL/M-86, Pascal-86, FORTRAN-86, C-86 and System Utilities**
    - **In-Circuit-Emulator (ICE™-186)**
- **High Performance Numeric Coprocessing Capability through 80C187 Interface**
- **Available in 68-Pin:**
  - **Plastic Leaded Chip Carrier (PLCC)**
  - **Ceramic Pin Grid Array (PGA)**
  - **Ceramic Leadless Chip Carrier (JEDEC A Package)**

  (See Packaging Outlines and Dimensions, Order Number 231369)
- **Available in EXPRESS Extended Temperature Range (−40°C to +85°C)**
- **Available in Military:**
  - **Different Specifications**
  - **10 MHz (M80C186-10) and 12.5 MHz (M80C186-12) Versions**

  (See M80C186 data sheet, Order Number 270500 for specifications)

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The Intel 80C186 is a CHMOS high integration microprocessor. In has features which are new to the 80186 family which include a DRAM refresh control unit, power-save mode and a direct numerics interface. When used in "compatible" mode, the 80C186 is 100% pin-for-pin compatible with the NMOS 80186 (except for 8087 applications). The "enhanced" mode of operation allows the full feature set of the 80C186 to be used. The 80C186 is upward compatible with 8086 and 8088 software and fully compatible with 80186 and 80188 software.

October 1991
Order Number: 270354-005

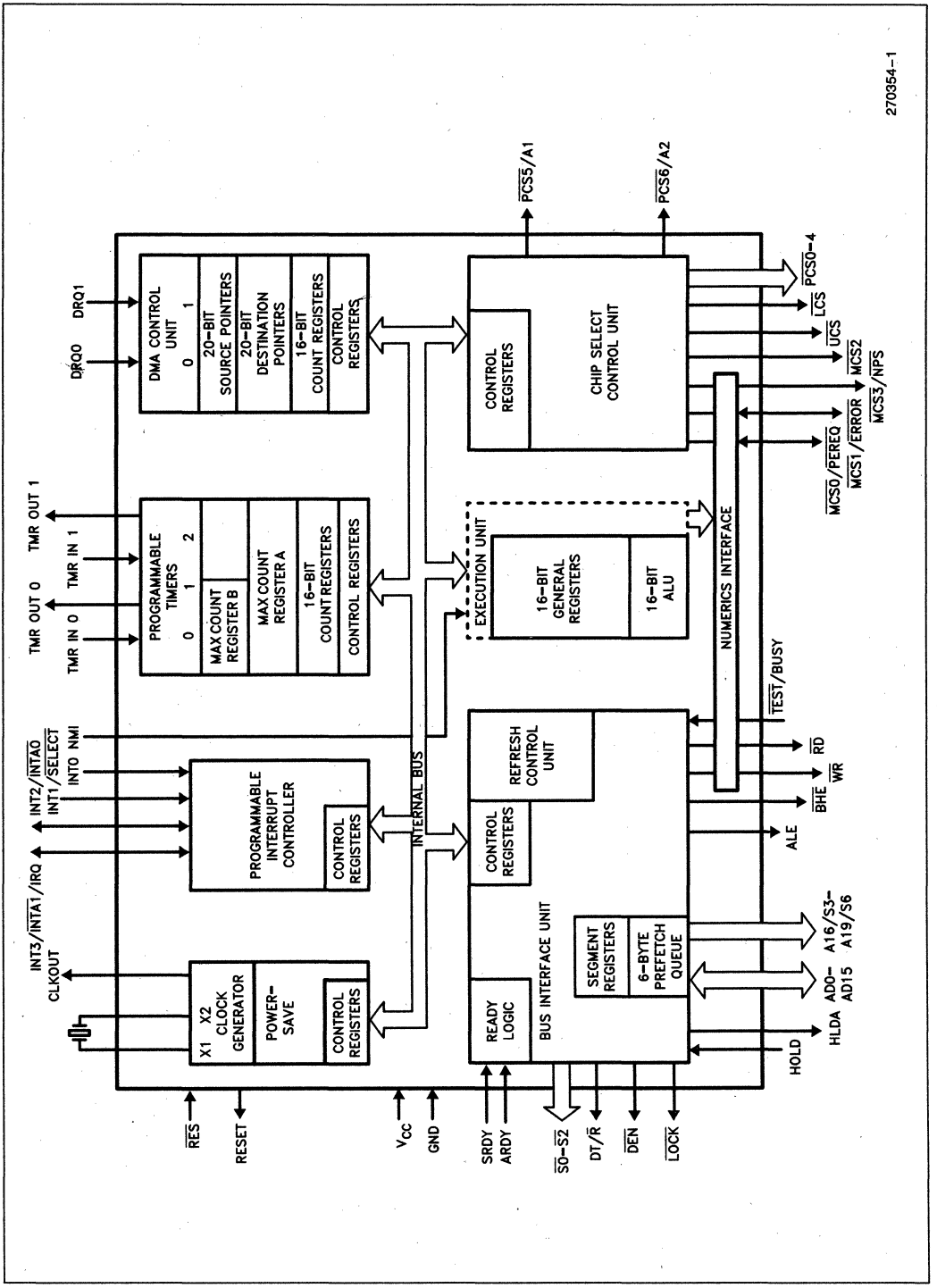
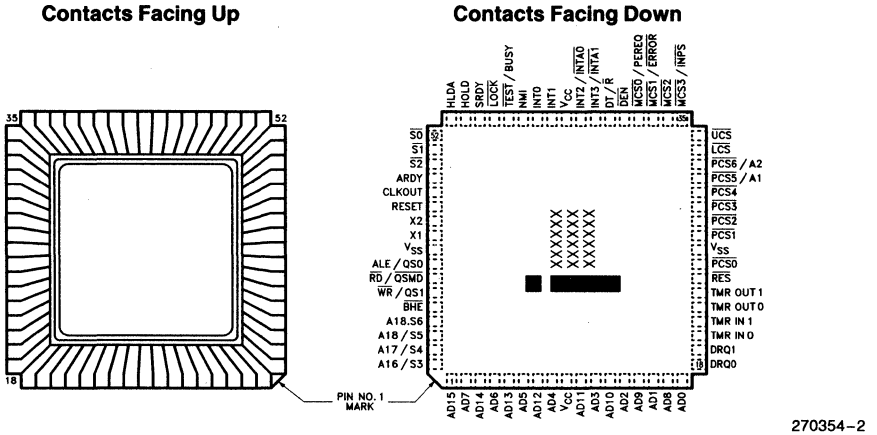


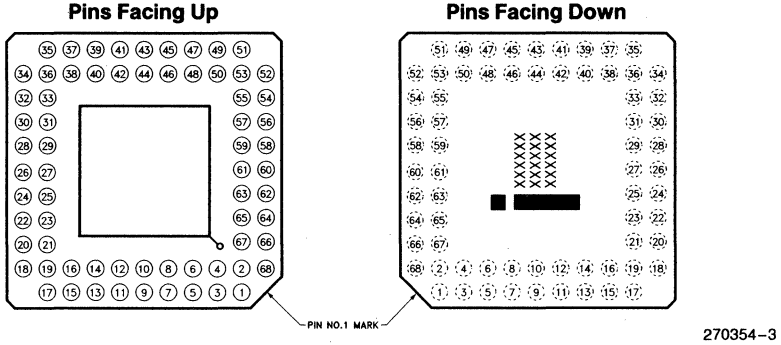
Figure 1. 80C186 Block Diagram

Ceramic Leadless Chip Carrier (JEDEC Type A)



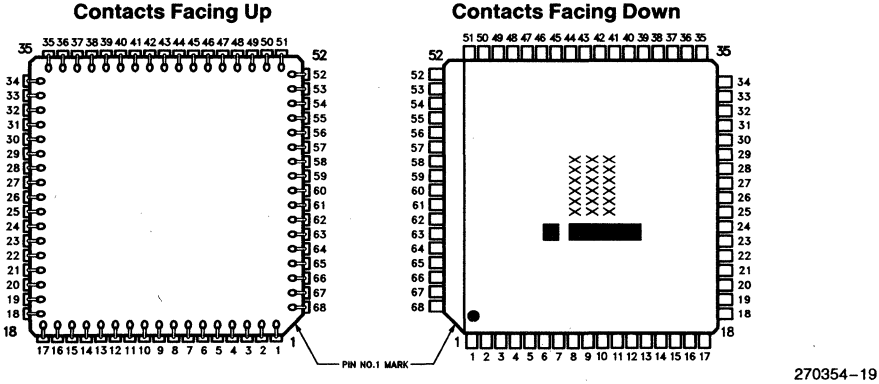
270354-2

Ceramic Pin Grid Array



270354-3

Plastic Leaded Chip Carrier



270354-19

Figure 2. 80C186 Pinout Diagrams

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Table 1. 80C186 Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	9 43	I I	System Power: +5 volt power supply.
V_{SS}	26 60	I I	System Ground.
RESET	57	O	RESET Output indicates that the 80C186 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal. Reset goes inactive 2 clockout periods after $\overline{RES}$ goes inactive. When tied to the $\overline{TEST}$/BUSY pin, RESET forces the 80C186 into enhanced mode. RESET is not floated during bus hold.
X1 X2	59 58	I O	Crystal Inputs X1 and X2 provide external connections for a fundamental mode or third overtone parallel resonant crystal for the internal oscillator. X1 can connect to an external clock instead of a crystal. In this case, minimize the capacitance on X2. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT is active during reset and bus hold.
$\overline{RES}$	24	I	An active $\overline{RES}$ causes the 80C186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80C186 clock. The 80C186 begins fetching instructions approximately 6½ clock cycles after $\overline{RES}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{RES}$ held LOW. $\overline{RES}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network.
$\overline{TEST}$/BUSY	47	I/O	The $\overline{TEST}$ pin is sampled during and after reset to determine whether the 80C186 is to enter Compatible or Enhanced Mode. Enhanced Mode requires $\overline{TEST}$ to be HIGH on the rising edge of $\overline{RES}$ and LOW four CLKOUT cycles later. Any other combination will place the 80C186 in Compatible Mode. During power-up, active $\overline{RES}$ is required to configure $\overline{TEST}$/BUSY as an input. A weak internal pullup ensures a HIGH state when the input is not externally driven. $\overline{TEST}$—In Compatible Mode this pin is configured to operate as $\overline{TEST}$. This pin is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when WAIT execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled every five clocks until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80C186 is waiting for $\overline{TEST}$, interrupts will be serviced. BUSY—In Enhanced Mode, this pin is configured to operate as BUSY. The BUSY input is used to notify the 80C186 of Numerics Processor Extension activity. Floating point instructions executing in the 80C186 sample the BUSY pin to determine when the Numerics Processor is ready to accept a new command. BUSY is active HIGH.
TMR IN 0 TMR IN 1	20 21	I I	Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized. Timer Inputs must be tied HIGH when not being used as clock or retrigger inputs.
TMR OUT 0 TMR OUT 1	22 23	O O	Timer outputs are used to provide single pulse or continous waveform generation, depending upon the timer mode selected. These outputs are not floated during a bus hold.

Table 1. 80C186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
DRQ0 DRQ1	18 19	I I	DMA Request is asserted HIGH by an external device when it is ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
NMI	46	I	The Non-Maskable Interrupt input causes a Type 2 interrupt. An NMI transition from LOW to HIGH is latched and synchronized internally, and initiates the interrupt at the next instruction boundary. NMI must be asserted for at least one CLKOUT period. The Non-Maskable Interrupt cannot be avoided by programming.
INT0 INT1/$\overline{\text{SELECT}}$ INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$/IRQ	45 44 42 41	I I I/O I/O	Maskable Interrupt Requests can be requested by activating one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When Slave Mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).
A19/S6 A18/S5 A17/S4 A16/S3	65 66 67 68	O O O O	Address Bus Outputs (16–19) and Bus Cycle Status (3–6) indicate the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W, and T_4, the S6 pin is LOW to indicate a CPU-initiated bus cycle or HIGH to indicate a DMA-initiated bus cycle. During the same T-states, S3, S4, and S5 are always LOW. These outputs are floated during bus hold or reset.
AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	1 3 5 7 10 12 14 16 2 4 6 8 11 13 15 17	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	Address/Data Bus (0–15) signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W, and T_4) bus. The bus is active HIGH. A_0 is analogous to $\overline{\text{BHE}}$ for the lower byte of the data bus, pins D_7 through D_0. It is LOW during T_1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations. These pins are floated during a bus hold or reset.

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Table 1. 80C186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{BHE}$	64	O	The $\overline{BHE}$ (Bus High Enable) signal is analogous to A0 in that it is used to enable data on to the most significant half of the data bus, pins D15–D8. $\overline{BHE}$ will be LOW during T_1 when the upper byte is transferred and will remain LOW through T_3 AND T_W. $\overline{BHE}$ does not need to be latched. $\overline{BHE}$ will float during HOLD or RESET. In Enhanced Mode, $\overline{BHE}$ will also be used to signify DRAM refresh cycles. A refresh cycle is indicated by both $\overline{BHE}$ and A0 being HIGH.
			$\overline{BHE}$ and A0 Encodings
			$\overline{BHE}$ Value / **A0 Value** / **Function** 0 / 0 / Word Transfer 0 / 1 / Byte Transfer on upper half of data bus (D15–D8) 1 / 0 / Byte Transfer on lower half of data bus (D_7–D_0) 1 / 1 / Refresh
ALE/QS0	61	O	Address Latch Enable/Queue Status 0 is provided by the 80C186 to latch the address. ALE is active HIGH, with addresses guaranteed valid on the trailing edge.
$\overline{WR}$/QS1	63	O	Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. It is active LOW, and floats during bus hold or reset. When the 80C186 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.
			QS1 / **QS0** / **Queue Operation** 0 / 0 / No queue operation 0 / 1 / First opcode byte fetched from the queue 1 / 1 / Subsequent byte fetched from the queue 1 / 0 / Empty the queue
$\overline{RD}$/$\overline{QSMD}$	62	O/I	Read Strobe is an active LOW signal which indicates that the 80C186 is performing a memory or I/O read cycle. It is guaranteed not to go LOW before the A/D bus is floated. An internal pull-up ensures that $\overline{RD}$/$\overline{QSMD}$ is HIGH during RESET. Following RESET the pin is sampled to determine whether the 80C186 is to provide ALE, $\overline{RD}$, and $\overline{WR}$, or queue status information. To enable Queue Status Mode, $\overline{RD}$ must be connected to GND. $\overline{RD}$ will float during bus HOLD.
ARDY	55	I	Asynchronous Ready informs the 80C186 that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUT and is active HIGH. The falling edge of ARDY must be synchronized to the 80C186 clock. Connecting ARDY HIGH will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the SRDY pin.
SRDY	49	I	Synchronous Ready informs the 80C186 that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active-HIGH input synchronized to CLKOUT. The use of SRDY allows a relaxed system timing over ARDY. This is accomplished by elimination of the one-half clock cycle required to internally synchonize the ARDY input signal. Connecting SRDY high will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the ARDY pin.

Table 1. 80C186 Pin Description (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{LOCK}$</td><td>48</td><td>O</td><td>$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus. $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction immediately following the LOCK prefix. It remains active until the completion of that instruction. No instruction prefetching will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ floats during bus hold or reset.</td></tr>
<tr><td>$\overline{S0}$
$\overline{S1}$
$\overline{S2}$</td><td>52
53
54</td><td>O
O
O</td><td>Bus cycle status $\overline{S0}$–$\overline{S2}$ are encoded to provide bus-transaction information:
80C186 Bus Cycle Status Information
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus Cycle Initiated</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction Fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Data from Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Data to Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive (no bus cycle)</td></tr>
</table>
The status pins float during HOLD.
$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.</td></tr>
<tr><td>HOLD
HLDA</td><td>50
51</td><td>I
O</td><td>HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. The 80C186 generates HLDA (HIGH) in response to a HOLD request. Simultaneous with the issuance of HLDA, the 80C186 will float the local bus and control lines. After HOLD is detected as being LOW, the 80C186 will lower HLDA. When the 80C186 needs to run another bus cycle, it will again drive the local bus and control lines.
In Enhanced Mode, HLDA will go low when a DRAM refresh cycle is pending in the 80C186 and an external bus master has control of the bus. It will be up to the external master to relinquish the bus by lowering HOLD so that the 80C186 may execute the refresh cycle.</td></tr>
<tr><td>$\overline{UCS}$</td><td>34</td><td>O/I</td><td>Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. $\overline{UCS}$ does not float during bus hold. The address range activating $\overline{UCS}$ is software programmable.
$\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the 80C186 will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{UCS}$ has a weak internal pullup that is active during RESET to ensure that the 80C186 does not enter ONCE mode inadvertently.</td></tr>
</table>

Table 1. 80C186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{LCS}$	33	O/I	Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. $\overline{LCS}$ does not float during bus HOLD. The address range activating $\overline{LCS}$ is software programmable. $\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the 80C186 will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{LCS}$ has a weak internal pullup that is active only during RESET to ensure that the 80C186 does not enter ONCE mode inadvertently.
$\overline{MCS0}$/PEREQ $\overline{MCS1}$/$\overline{ERROR}$ $\overline{MCS2}$ $\overline{MCS3}$/$\overline{NPS}$	38 37 36 35	O/I O/I O O	Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines do not float during bus HOLD. The address ranges activating $\overline{MCS0}$–3 are software programmable. In Enhanced Mode, $\overline{MCS0}$ becomes a PEREQ input (Processor Extension Request). When connected to the Numerics Processor Extension, this input is used to signal the 80C186 when to make numeric data transfers to and from the NPX. $\overline{MCS3}$ becomes $\overline{NPS}$ (Numeric Processor Select) which may only be activated by communication to the Numerics Processor Extension. $\overline{MCS1}$ becomes $\overline{ERROR}$ in enhanced mode and is used to signal numerics coprocessor errors. $\overline{MCS0}$/PEREQ and $\overline{MCS1}$/$\overline{ERROR}$ have weak internal pullups which are active during reset.
$\overline{PCS0}$ $\overline{PCS1}$ $\overline{PCS2}$ $\overline{PCS3}$ $\overline{PCS4}$	25 27 28 29 30	O O O O O	Peripheral Chip Select signals 0–4 are active LOW when a reference is made to the defined peripheral area (64K byte I/O or 1 MByte memory space). These lines do not float during bus HOLD. The address ranges activating $\overline{PCS0}$–4 are software programmable.
$\overline{PCS5}$/A1	31	O	Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software-programmable. $\overline{PCS5}$/A1 does not float during bus HOLD. When programmed to provide latched A1, this pin will retain the previously latched value during HOLD.
$\overline{PCS6}$/A2	32	O	Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software-programmable. $\overline{PCS6}$/A2 does not float during bus HOLD. When programmed to provide latched A2, this pin will retain the previously latched value during HOLD.
DT/$\overline{R}$	40	O	Data Transmit/Receive controls the direction of data flow through an external data bus transceiver. When LOW, data is transferred to the 80C186. When HIGH the 80C186 places write data on the data bus. DT/$\overline{R}$ floats during a bus hold or reset.
$\overline{DEN}$	39	O	Data Enable is provided as a data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access (including 80C187 access). $\overline{DEN}$ is HIGH whenever DT/$\overline{R}$ changes state. During RESET, $\overline{DEN}$ is driven HIGH for one clock, then floated. $\overline{DEN}$ also floats during HOLD.

FUNCTIONAL DESCRIPTION

Introduction

The following Functional Description describes the base architecture of the 80C186. The 80C186 is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip. The 80C186 is object code compatible with the 8086/8088 microprocessors and adds 10 new instruction types to the 8086/8088 instruction set.

The 80C186 has two major modes of operation, Compatible and Enhanced. In Compatible Mode the 80C186 is completely compatible with NMOS 80186, with the exception of 8087 support. The Enhanced mode adds three new features to the system design. These are Power-Save control, Dynamic RAM refresh, and an asynchronous Numerics Coprocessor interface.

80C186 BASE ARCHITECTURE

The 8086, 8088, 80186, and 80188 family all contain the same basic set of registers, instructions, and addressing modes. The 80C186 processor is upward compatible with the 8086 and 8088 CPUs.

Register Set

The 80C186 base architecture has fourteen registers as shown in Figures 3a and 3b. These registers are grouped into the following categories.

General Registers

Eight 16-bit general purpose registers may be used for arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

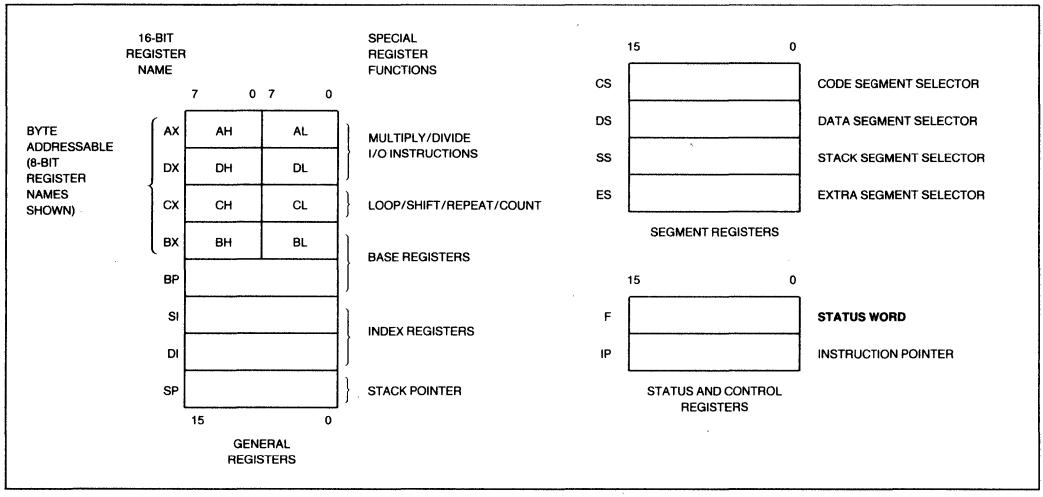

Figure 3a. 80C186 Register Set

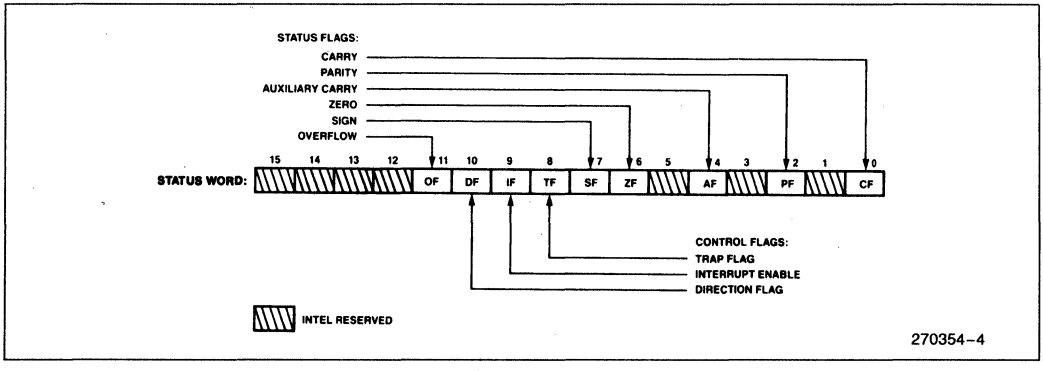

Figure 3b. Status Word Format

Segment Registers

Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

Base and Index Registers

Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

Status and Control Registers

Two 16-bit special purpose registers record or alter certain aspects of the 80C186 processor state. These are the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed, and the Status Word Register, which contains status and control flag bits (see Figures 3a and 3b).

Status Word Description

The Status Word records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the 80C186 within a given operating mode (bits 8, 9, and 10). The Status Word Register is 16-bits wide. The function of the Status Word bits is shown in Table 2.

Table 2. Status Word Bit Functions

Bit Position	Name	Function
0	CF	Carry Flag—Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag—Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag—Set if result is zero; cleared otherwise
7	SF	Sign Flag—Set equal to high-order bit of result (0 if positive, 1 if negative)
8	TF	Single Step Flag—Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-enable Flag—When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag—Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag—Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high-level instructions, and processor control. These categories are summarized in Figure 4.

An 80C186 instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory. Specific operand addressing modes are discussed later in this data sheet.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment register (code, data, stack, extra). The physical address is calculated by shifting the base value LEFT by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 5). This allows for a 1 MByte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 3). These rules follow the way programs are written (see Figure 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack
ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero
LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word
FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{\text{TEST}}$ pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Figure 4. 80C186 Instruction Set

CONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal
JAE/JNB	Jump if above or equal/not below
JB/JNAE	Jump if below/not above nor equal
JBE/JNA	Jump if below or equal/not above
JC	Jump if carry
JE/JZ	Jump if equal/zero
JG/JNLE	Jump if greater/not less nor equal
JGE/JNL	Jump if greater or equal/not less
JL/JNGE	Jump if less/not greater nor equal
JLE/JNG	Jump if less or equal/not greater
JNC	Jump if not carry
JNE/JNZ	Jump if not equal/not zero
JNO	Jump if not overflow
JNP/JPO	Jump if not parity/parity odd
JNS	Jump if not sign

JO	Jump if overflow
JP/JPE	Jump if parity/parity even
JS	Jump if sign
UNCONDITIONAL TRANSFERS	
CALL	Call procedure
RET	Return from procedure
JMP	Jump
ITERATION CONTROLS	
LOOP	Loop
LOOPE/LOOPZ	Loop if equal/zero
LOOPNE/LOOPNZ	Loop if not equal/not zero
JCXZ	Jump if register CX = 0
INTERRUPTS	
INT	Interrupt
INTO	Interrupt if overflow
IRET	Interrupt return

Figure 4. 80C186 Instruction Set (Continued)

To access operands that do not reside in one of the four immediately available segments, a full 32-bit pointer can be used to reload both the base (segment) and offset values.

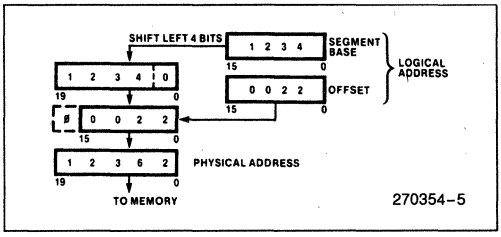

Figure 5. Two Component Address

Table 3. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data.
Stack	Stack (SS)	All stack pushes and pops; any memory references which use BP Register as a base register.
External Data (Global)	Extra (ES)	All string instruction references which use the DI register as an index.
Local Data	Data (DS)	All other data references.

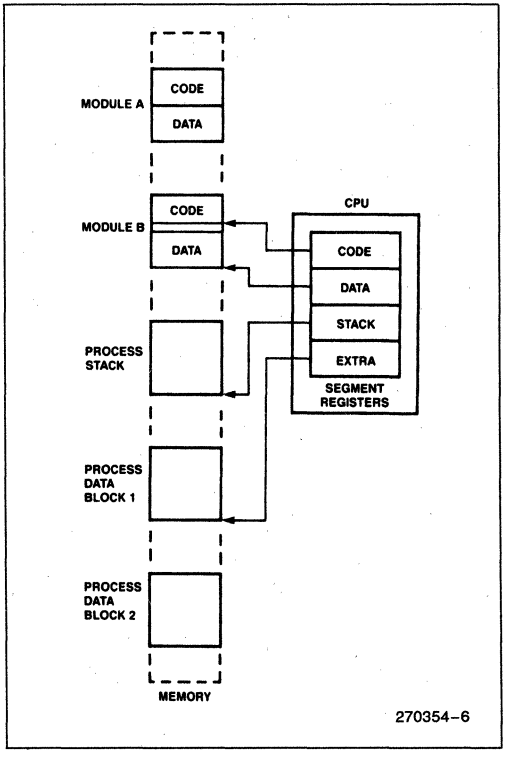

Figure 6. Segmented Memory Helps Structure Software

Addressing Modes

The 80C186 provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an Index register.
- *Based indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

Data Types

The 80C186 directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32- and 64-bit integers are supported using a Numeric Data Coprocessor with the 80C186.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component or a 16-bit segment base component in addition to a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 to 64K bytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4-bits) of the byte.
- *Floating Point:* A signed 32-, 64-, or 80-bit real number representation. (Floating point operands are supported using a Numeric Data Coprocessor with the 80C186.)

In general, individual data elements must fit within defined segment limits. Figure 7 graphically represents the data types supported by the 80C186.

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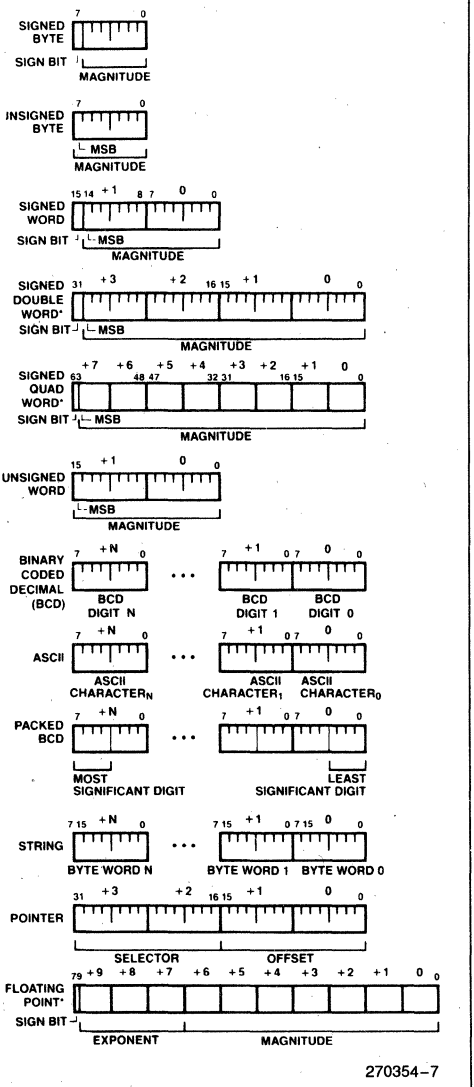
I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A_{15}–A_8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Status Word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.



NOTE:
*Supported by using a Numeric Data Coprocessor with the 80C186.

Figure 7. 80C186 Supported Data Types

Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. If the exception was caused by executing an ESC instruction with the ESC trap bit set in the relocation register, the return instruction will point to the ESC instruction, or to the segment override prefix immediately preceding the ESC instruction if the prefix was present. In all other cases, the return address from an exception will point at the instruction immediately following the instruction causing the exception.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0–31, some of which are used for instruction exceptions, are reserved. Table 4 shows the 80C186 predefined types and default priority levels. For each interrupt, an 8-bit vector must be supplied to the 80C186 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. In addition, internal peripherals and noncascaded external interrupts will generate their own vectors through the internal interrupt controller. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Interrupt Sources

The 80C186 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INT0, DIV, IDIV, etc.). All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type (Table 4), multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

Those pre-defined 80C186 interrupts which cannot be masked by programming are described below.

DIVIDE ERROR EXCEPTION (TYPE 0)

Generated when a DIV or IDIV instruction quotient cannot be expressed in the number of bits in the destination.

SINGLE-STEP INTERRUPT (TYPE 1)

Generated after most instructions if the TF flag in the status word is set. This interrupt allows programs to execute one instruction at a time. Interrupts will not be generated after prefix instructions (e.g., REP), instructions which modify segment registers (e.g., POP DS), or the WAIT instruction. Vectoring to the single-step interrupt service routine clears the TF bit. An IRET instruction in the interrupt service routine

Table 4. 80C186 Interrupt Vectors

Interrupt Name	Vector Type	Vector Address	Default Priority	Related Instructions	Applicable Notes
Divide Error Exception	0	00H	1	DIV, IDIV	1
Single Step Interrupt	1	04H	1A	All	2
Non-Maskable Interrupt (NMI)	2	08H	1	All	
Breakpoint Interrupt	3	0CH	1	INT	1
INTO Detected Overflow Exception	4	10H	1	INTO	1
Array Bounds Exception	5	14H	1	BOUND	1
Unused Opcode Exception	6	18H	1	Undefined Opcodes	1
ESC Opcode Exception	7	1CH	1	ESC Opcodes (Coprocessor)	1, 3
Timer 0 Interrupt	8	20H	2A		4
Timer 1 Interrupt	18	48H	2B		4, 6
Timer 2 Interrupt	19	4CH	2C		4, 6
Reserved	9	24H	3		
DMA 0 Interrupt	10	28H	4		6
DMA 1 Interrupt	11	2CH	5		6
INT0 Interrupt	12	30H	6		
INT1 Interrupt	13	34H	7		
INT2 Interrupt	14	38H	8		
INT3 Interrupt	15	3CH	9		
Numerics Coprocessor Exception	16	40H	1	ESC Opcodes (Numerics Coprocessor)	1, 5
Reserved	17	44H			
Reserved	20–31	50H . . . 7CH			

NOTES:
Default priorities for the interrupt sources are used only if the user does not program each source to a unique priority level.
1. Generated as a result of an instruction execution.
2. Performed in the same manner as 8086.
3. An ESC (coprocessor) opcode will cause a trap if the 80C186 is in compatible mode or if the processor is in Enhanced Mode with the proper bit set in the peripheral control block relocation register. **The 80C186 is not directly compatible with the 80186 in this respect.**
4. All three timers constitute one source of request to the interrupt controller. As such, they share the same priority level with respect to other interrupt sources. However, the timers have a defined priority order among themselves (2A > 2B > 2C).
5. Numerics coprocessor exceptions are detected by the 80C186 upon execution of a subsequent numerics instruction.
6. The vector type numbers for these sources are programmable in Slave Mode.

restores the TF bit to logic "1" and transfers control to the next instruction to be single-stepped.

NON-MASKABLE INTERRUPT—NMI (TYPE 2)

An external interrupt source which is serviced regardless of the state of the IF bit. No external interrupt acknowledge sequence is performed. The IF bit is cleared at the beginning of an NMI interrupt to prevent maskable interrupts from being serviced. A typical use of NMI would be to activate a power failure routine.

BREAKPOINT INTERRUPT (TYPE 3)

A one-byte version of the INT instruction. It uses 12 as an index into the service routine address table (because it is a type 3 interrupt).

INTO DETECTED OVERFLOW EXCEPTION (TYPE4)

Generated during an INTO instruction if the 0F bit is set.

ARRAY BOUNDS EXCEPTION (TYPE 5)

Generated during a BOUND instruction if the array index is outside the array bounds. The array bounds are located in memory at a location indicated by one of the instruction operands. The other operand indicates the value of the index to be checked.

UNUSED OPCODE EXCEPTION (TYPE 6)

Generated if execution is attempted on undefined opcodes.

ESCAPE OPCODE EXCEPTION (TYPE 7)

Generated if execution is attempted of ESC opcodes (D8H–DFH). In compatible mode operation, ESC opcodes will always generate this exception. In enhanced mode operation, the exception will be generated only if a bit in the relocation register is set. The return address of this exception will point to the ESC instruction causing the exception. If a segment override prefix preceded the ESC instruction, the return address will point to the segment override prefix.

NOTE:
80C186 processing of ESC (numerics coprocessor) opcodes differs substantially from the 80186.

NUMERICS COPROCESSOR EXCEPTION (TYPE 16)

An interrupt generated in response to an unmasked error in the 80C187 Numerics Coprocessor Extension. In general, the 80C187 does not detect an error until the instruction after the error occurred. A numerics coprocessor error is signalled to the 80C187 on its $\overline{\text{ERROR}}$ input pin.

Hardware-generated interrupts are divided into two groups: maskable interrupts and non-maskable interrupts. The 80C186 provides maskable hardware interrupt request pins INT0–INT3. In addition, maskable interrupts may be generated by the 80C186 integrated DMA controller and the integrated timer unit. The vector types for these interrupts is shown in Table 4. Software enables these inputs by setting the interrupt flag bit (IF) in the Status Word. The interrupt controller is discussed in the peripheral section of this data sheet.

Further maskable interrupts are disabled while servicing an interrupt because the IF bit is reset as part of the response to an interrupt or exception. The saved Status Word will reflect the enable status of the processor prior to the interrupt. The interrupt flag will remain zero unless specifically set. The interrupt return instruction restores the Status Word, thereby restoring the original status of IF bit. If the interrupt return re-enables interrupts, and another interrupt is pending, the 80C186 will immediately service the highest-priority interrupt pending, i.e., no instructions of the main line program will be executed.

Initialization and Processor Reset

Processor initialization is accomplished by driving the $\overline{\text{RES}}$ input pin LOW. $\overline{\text{RES}}$ must be LOW during power-up to ensure proper device initialization. $\overline{\text{RES}}$ forces the 80C186 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{\text{RES}}$ is active. After $\overline{\text{RES}}$ becomes inactive and an internal processing interval elapses, the 80C186 begins execution with the instruction at physical location FFFF0(H). $\overline{\text{RES}}$ also sets some registers to predefined values as shown in Table 5.

Table 5. 80C186 Initial Register State after RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

80C186 CLOCK GENERATOR

The 80C186 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

Oscillator

The 80C186 oscillator circuit is designed to be used either with a parallel resonant fundamental or third-overtone mode crystal, depending upon the frequency range of the application as shown in Figure 8c. This is used as the time base for the 80C186. The crystal frequency chosen should be twice the required processor frequency. Use of an LC or RC circuit is not recommended.

The output of the oscillator is not directly available outside the 80C186. The two recommended crystal configurations are shown in Figures 8a and 8b. When used in third-overtone mode the tank circuit shown in Figure 8b is recommended for stable operation. The sum of the stray capacitances and load-

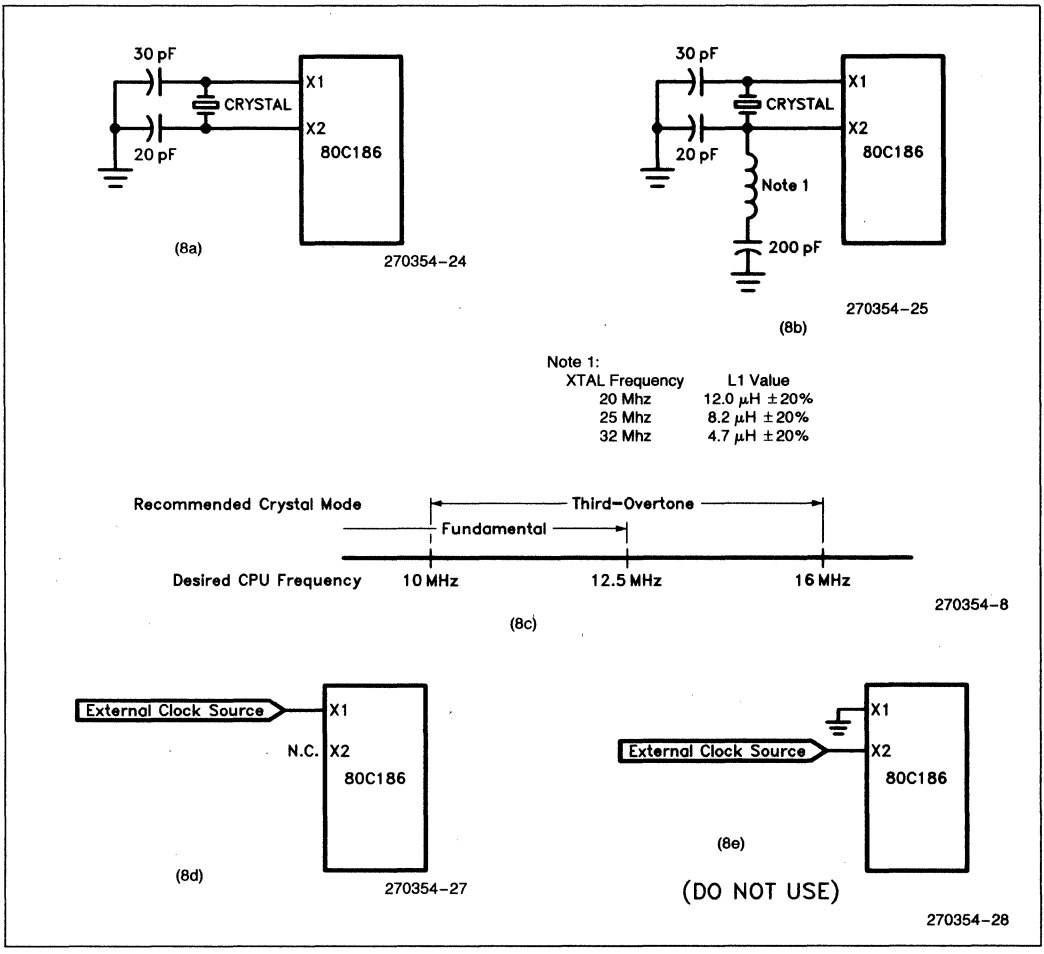


Figure 8. 80C186 Oscillator Configurations (see text)

ing capacitors should equal the values shown. It is advisable to limit stray capacitance between the X1 and X2 pins to less than 10 pF. While a fundamental-mode circuit will require approximately 1 ms for start-up, the third-overtone arrangement may require 1 ms to 3 ms to stabilize.

Alternately, the oscillator may be driven from an external source as shown in Figure 8d. The configuration shown in Figure 8e is not recommended.

Intel recommends the following values for crystal selection parameters.

Temperature Range:	0 to 70°C
ESR (Equivalent Series Resistance):	40Ω max
C_0 (Shunt Capacitance of Crystal):	7.0 pF max
C_1 (Load Capacitance):	20 pF ± 2 pF
Drive Level:	1 mW max

Clock Generator

The 80C186 clock generator provides the 50% duty cycle processor clock for the 80C186. It does this by dividing the oscillator output by 2 forming the symmetrical clock. If an external oscillator is used, the state of the clock generator will change on the falling edge of the oscillator signal. The CLKOUT pin provides the processor clock signal for use outside the 80C186. This may be used to drive other system components. All timings are referenced to the output clock.

READY Synchronization

The 80C186 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T_2, T_3, and again in the middle of each T_W until ARDY is sampled HIGH. One-half CLKOUT cycle of resolution time is used for full synchronization of a rising ARDY signal. A high-to-low transition on ARDY may be used as an indication of the not ready condition but it must be performed synchronously to CLKOUT **either** in the middle of T_2, T_3, **or** T_W, or at the falling edge of T_3 or T_W.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T_2, T_3 and again at the end of each T_W until it is sampled HIGH. By using this input rather than the asynchronous ready input, the half-clock cycle resolution time penalty is eliminated. This input must satisfy set-up and hold times to guarantee proper operation of the circuit.

In addition, the 80C186, as part of the integrated chip-select logic, has the capability to program WAIT states for memory and peripheral blocks. This is discussed in the Chip Select/Ready Logic description.

RESET Logic

The 80C186 provides both a $\overline{RES}$ input pin and a synchronized RESET output pin for use with other system components. The $\overline{RES}$ input pin on the 80C186 is provided with hysteresis in order to facilitate power-on Reset generation via an RC network. RESET output is guaranteed to remain active for at least five clocks given a $\overline{RES}$ input of at least six clocks. RESET may be delayed up to approximately two and one-half clocks behind $\overline{RES}$.

LOCAL BUS CONTROLLER

The 80C186 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides outputs that can be used to enable external buffers and to direct the flow of data on and off the local bus.

Memory/Peripheral Control

The 80C186 provides ALE, $\overline{RD}$, and $\overline{WR}$ bus control signals. The $\overline{RD}$ and $\overline{WR}$ signals are used to strobe data from memory or I/O to the 80C186 or to strobe data from the 80C186 to memory or I/O. The ALE line provides a strobe to latch the address when it is valid. The 80C186 local bus controller does not provide a memory/$\overline{I/O}$ signal. If this is required, use the $\overline{S2}$ signal (which will require external latching), make the memory and I/O spaces nonoverlapping, or use only the integrated chip-select circuitry.

Transceiver Control

The 80C186 generates two control signals for external transceiver chips. This capability allows the addition of transceivers for extra buffering without adding external logic. These control lines, DT/$\overline{R}$ and $\overline{DEN}$, are generated to control the flow of data through the transceivers. The operation of these signals is shown in Table 6.

Table 6. Transceiver Control Signals Description

Pin Name	Function
$\overline{DEN}$ (Data Enable)	Enables the output drivers of the transceivers. It is active LOW during memory, I/O, numeric processor extension, or INTA cycles.
DT/$\overline{R}$ (Data Transmit/ Receive)	Determines the direction of travel through the transceivers. A HIGH level directs data away from the processor during write operations, while a LOW level directs data toward the processor during a read operation.

Local Bus Arbitration

The 80C186 uses a HOLD/HLDA system of local bus exchange. This provides an asynchronous bus exchange mechanism. This means multiple masters utilizing the same bus can operate at separate clock frequencies. The 80C186 provides a single HOLD/HLDA pair through which all other bus masters may gain control of the local bus. External circuitry must arbitrate which external device will gain control of the bus when there is more than one alternate local bus master. When the 80C186 relinquishes control of the local bus, it floats $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S0}$–$\overline{S2}$, $\overline{LOCK}$, AD0–AD15, A16–A19, $\overline{BHE}$, and DT/$\overline{R}$ to allow another master to drive these lines directly.

The 80C186 HOLD latency time, i.e., the time between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is second only to DRAM refresh requests in priority of activity requests the processor may receive. Any bus cycle in progress will be completed before the 80C186 relinquishes the bus. This implies that if a HOLD request is received just as a DMA transfer begins, the HOLD latency can be as great as 4 bus cycles. This will occur if a DMA word trans-

fer operation is taking place from an odd address to an odd address. This is a total of 16 clock cycles or more if WAIT states are required. In addition, if locked transfers are performed, the HOLD latency time will be increased by the length of the locked transfer.

If the 80C186 has relinquished the bus and a refresh request is pending, HLDA is removed (driven low) to signal the remote processor that the 80C186 wishes to regain control of the bus. The 80C186 will wait until HOLD is removed before taking control of the bus to run the refresh cycle.

Local Bus Controller and Reset

During RESET the local bus controller will perform the following action:

- Drive $\overline{DEN}$, $\overline{RD}$, and $\overline{WR}$ HIGH for one clock cycle, then float them.
- Drive $\overline{S0}$–$\overline{S2}$ to the inactive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Float AD0–15, A16–19, $\overline{BHE}$, DT/$\overline{R}$.
- Drive ALE LOW
- Drive HLDA LOW.

$\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$, and $\overline{TEST}$/BUSY pins have internal pullup devices which are active while $\overline{RES}$ is applied. Excessive loading or grounding certain of these pins causes the 80C186 to enter an alternative mode of operation:

- $\overline{RD}$/QSMD low results in Queue Status Mode.
- $\overline{UCS}$ and $\overline{LCS}$ low results in ONCE™ Mode.
- $\overline{TEST}$/BUSY low (and high later) results in Enhanced Mode.

INTERNAL PERIPHERAL INTERFACE

All the 80C186 integrated peripherals are controlled by 16-bit registers contained within an internal 256-byte control block. The control block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D_{15-0}, SRDY, and ARDY will be ignored. The base address of the control block must be on an even 256-byte boundary (i.e., the lower 8 bits of the base address are all zeros). All of the defined registers within this control block may be read or written by the 80C186 CPU at any time.

The control block base address is programmed by a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block (see Figure 9). It provides the upper 12 bits of the base address of the control block. The control block is effectively an internal chip select range and must abide by all the rules concerning chip selects (the chip select circuitry is discussed later in this data sheet). Any access to the 256 bytes of the control block activates an internal chip select.

Other chip selects may overlap the control block only if they are programmed to zero wait states and ignore external ready. In addition, bit 12 of this register determines whether the control block will be mapped into I/O or memory space. If this bit is 1, the control block will be located in memory space. If the bit is 0, the control block will be located in I/O space. If the control register block is mapped into I/O space, the upper 4 bits of the base address must be programmed as 0 (since I/O addresses are only 16 bits wide).

In addition to providing relocation information for the control block, the relocation register contains bits which place the interrupt controller into Slave Mode, and cause the CPU to interrupt upon encountering ESC instructions. At RESET, the relocation register is set to 20FFH, which maps the control block to start at FF00H in I/O space. An offset map of the 256-byte control register block is shown in Figure 10.

CHIP-SELECT/READY GENERATION LOGIC

The 80C186 contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

Memory Chip Selects

The 80C186 provides 6 memory chip select outputs for 3 address areas; upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

The range for each chip select is user-programmable and can be set to 2K, 4K, 8K, 16K, 32K, 64K, 128K (plus 1K and 256K for upper and lower chip selects). In addition, the beginning or base address

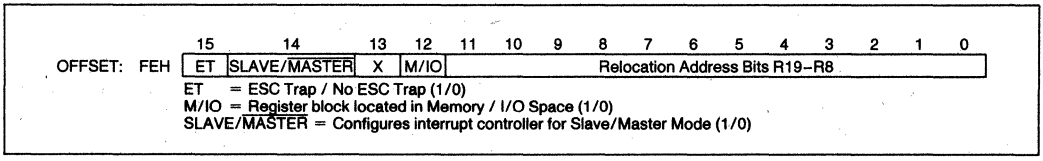


Figure 9. Relocation Register

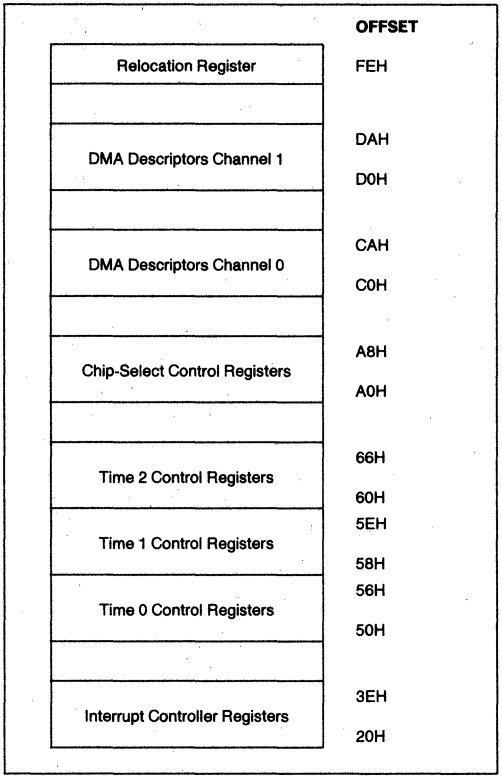


Figure 10. Internal Register Map

of the midrange memory chip select may also be selected. Only one chip select may be programmed to be active for any memory location at a time. All chip select sizes are in bytes, whereas 80C186 memory is arranged in words. This means that if, for example, 16 64K x 1 memories are used, the memory block size will be 128K, not 64K.

Upper Memory $\overline{CS}$

The 80C186 provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the 80C186 begins executing at memory location FFFF0H.

The upper limit of memory defined by this chip select is always FFFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is also defined. Table 7 shows the relationship between the base address selected and the size of the memory block obtained.

Table 7. UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000	256K	C038H

The lower limit of this memory block is defined in the UMCS register (see Figure 11). This register is at offset A0H in the internal control block. The legal values for bits 6–13 and the resulting starting address and memory block sizes are given in Table 7. Any combination of bits 6–13 not shown in Table 7 will result in undefined operation. After reset, the UMCS register is programmed for a 1K area. It must be reprogrammed if a larger upper memory area is desired.

The internal generation of any 20-bit address whose upper 16 bits are equal to or greater than the UMCS value (with bits 0–5 as "0") asserts $\overline{UCS}$. UMCS bits R2–R0 specify the ready mode for the area of memory defined by the chip select register, as explained later.

Lower Memory $\overline{CS}$

The 80C186 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The lower limit of memory defined by this chip select is always 0H, while the upper limit is programmable. By programming the upper limit, the size of the memory block is defined. Table 8 shows the relationship between the upper address selected and the size of the memory block obtained.

Table 8. LMCS Programming Values

Upper Address	Memory Block Size	LMCS Value (Assuming R0=R1=R2=0)
003FFH	1K	0038H
007FFH	2K	0078H
00FFFH	4K	00F8H
01FFFH	8K	01F8H
03FFFH	16K	03F8H
07FFFH	32K	07F8H
0FFFFH	64K	0FF8H
1FFFFH	128K	1FF8H
3FFFFH	256K	3FF8H

The upper limit of this memory block is defined in the LMCS register (see Figure 12) at offset A2H in the internal control block. The legal values for bits 6–15 and the resulting upper address and memory block sizes are given in Table 8. Any combination of bits 6–15 not shown in Table 8 will result in undefined operation. After RESET, the LMCS register value is undefined. However, the $\overline{LCS}$ chip-select line will not become active until the LMCS register is accessed.

Any internally generated 20-bit address whose upper 16 bits are less than or equal to LMCS (with bits 0–5 "1") will assert $\overline{LCS}$. LMCS register bits R2–R0 specify the READY mode for the area of memory defined by this chip-select register.

Mid-Range Memory $\overline{CS}$

The 80C186 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located within the 80C186 1M byte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the mid-range select lines, as shown in Table 9, is determined by bits 8–14 of the MPCS register (see Figure 13). This register is at location A8H in the internal control block. One and only one of bits 8–14 must be set at a time. Unpredictable operation of the $\overline{MCS}$ lines will otherwise occur. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the mid-range block. If the total block size is 32K, each chip select is active for 8K of memory with $\overline{MCS0}$ being active for the first range and $\overline{MCS3}$ being active for the last range.

The EX and MS in MPCS relate to peripheral functionality as described in a later section.

Table 9. MPCS Programming Values

Total Block Size	Individual Select Size	MPCS Bits 14–8
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

The base address of the mid-range memory block is defined by bits 15–9 of the MMCS register (see Figure 14). This register is at offset A6H in the internal control block. These bits correspond to bits A19–A13 of the 20-bit memory address. Bits A12–A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the mid-range block size is 32K (or the size of the block for which each $\overline{MCS}$ line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, since the first few integer multiples of a 32K memory block are 0H, 8000H, 10000H, 18000H, etc. After RESET, the contents of both registers are undefined. However, none of the $\overline{MCS}$ lines will be active until both the MMCS and MPCS registers are accessed.

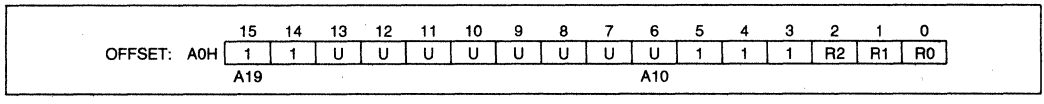


Figure 11. UMCS Register

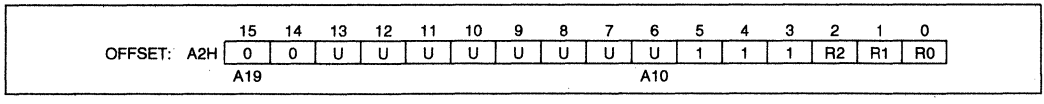


Figure 12. LMCS Register

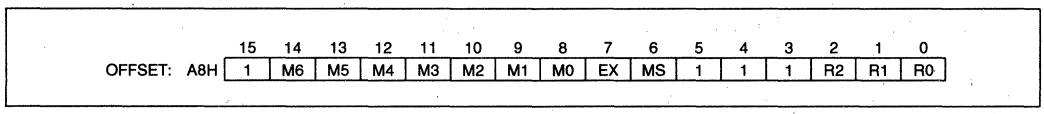


Figure 13. MPCS Register

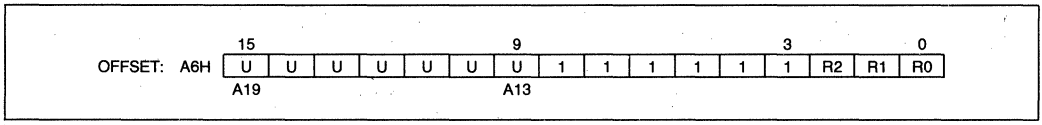


Figure 14. MMCS Register

MMCS bits R2–R0 specify READY mode of operation for all four mid-range chip selects.

The 512K block size for the mid-range memory chip selects is a special case. When using 512K, the base address would have to be at either locations 00000H or 80000H. If it were to be programmed at 00000H when the $\overline{LCS}$ line was programmed, there would be an internal conflict between the $\overline{LCS}$ ready generation logic and the $\overline{MCS}$ ready generation logic. Likewise, if the base address were programmed at 80000H, there would be a conflict with the $\overline{UCS}$ ready generation logic. Since the $\overline{LCS}$ chip-select line does not become active until programmed, while the $\overline{UCS}$ line is active at reset, the memory base can be set only at 00000H. If this base address is selected, however, the $\overline{LCS}$ range must not be programmed.

In Enhanced Mode, three of the four $\overline{MCS}$ pins become handshaking pins for the 80C187 Numerics Processor Extension. $\overline{MCS2}$ is still available as a chip select covering one-fourth the mid-range address block, subject to the usual programming of the MPCS and MMCS registers.

Peripheral Chip Selects

The 80C186 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address may be located in either memory or I/O space.

Seven $\overline{CS}$ lines called $\overline{PCS0}$–6 are generated by the 80C186. The base address is user-programmable; however it can only be a multiple of 1K bytes, i.e., the least significant 10 bits of the starting address are always 0.

$\overline{PCS5}$ and $\overline{PCS6}$ can also be programmed to provide latched address bits A1 and A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0 and A1 pins used for selecting internal registers of external 8-bit peripheral chips. This scheme simplifies the external hardware because the peripheral registers can be located on even boundaries in I/O or memory space.

The starting address of the peripheral chip-select block is defined by the PACS register (see Figure 15). The register is located at offset A4H in the internal control block. Bits 15–6 of this register correspond to bits 19–10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block. Bits 9–0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12–15 must be programmed zero, since the I/O address is only 16 bits wide. Table 10 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

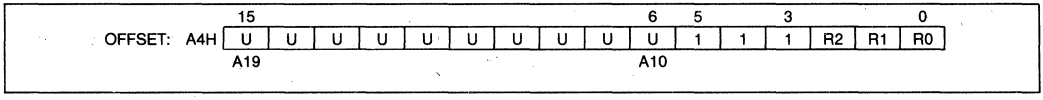


Figure 15. PACS Register

The user should program bits 15–6 to correspond to the desired peripheral base location. PACS bits 0–2 are used to specify READY mode for $\overline{PCS0}$–$\overline{PCS3}$.

Table 10. PCS Address Ranges

$\overline{PCS}$ Line	Active between Locations
$\overline{PCS0}$	PBA —PBA + 127
$\overline{PCS1}$	PBA + 128—PBA + 255
$\overline{PCS2}$	PBA + 256—PBA + 383
$\overline{PCS3}$	PBA + 384—PBA + 511
$\overline{PCS4}$	PBA + 512—PBA + 639
$\overline{PCS5}$	PBA + 640—PBA + 767
$\overline{PCS6}$	PBA + 768—PBA + 895

The mode of operation of the peripheral chip selects is defined by the MPCS register (which is also used to set the size of the mid-range memory chip-select block, see Figure 13). The register is located at offset A8H in the internal control block. Bit 7 is used to select the function of $\overline{PCS5}$ and $\overline{PCS6}$, while bit 6 is used to select whether the peripheral chip selects are mapped into memory or I/O space. Table 11 describes the programming of these bits. After RESET, the contents of both the MPCS and the PACS registers are undefined, however none of the PCS lines will be active until both of the MPCS and PACS registers are accessed.

Table 11. MS, EX Programming Values

Bit	Description
MS	1 = Peripherals mapped into memory space.
	0 = Peripherals mapped into I/O space.
EX	0 = 5 $\overline{PCS}$ lines. A1, A2 provided.
	1 = 7 $\overline{PCS}$ lines. A1, A2 are not provided.

MPCS bits 0–2 specify the READY mode for $\overline{PCS4}$–$\overline{PCS6}$ as outlined below.

READY Generation Logic

The 80C186 can generate a READY signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the 80C186 may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

READY control consists of 3 bits for each $\overline{CS}$ line or group of lines generated by the 80C186. The interpretation of the READY bits is shown in Table 12.

Table 12. READY Bits Programming

R2	R1	R0	Number of WAIT States Generated
0	0	0	0 wait states, external RDY also used.
0	0	1	1 wait state inserted, external RDY also used.
0	1	0	2 wait states inserted, external RDY also used.
0	1	1	3 wait states inserted, external RDY also used.
1	0	0	0 wait states, external RDY ignored.
1	0	1	1 wait state inserted, external RDY ignored.
1	1	0	2 wait states inserted, external RDY ignored.
1	1	1	3 wait states inserted, external RDY ignored.

The internal ready generator operates in parallel with external READY, not in series if the external READY is used (R2 = 0). For example, if the internal generator is set to insert two wait states, but activity on the external READY lines will insert four wait states, the processor will only insert four wait states, not six. This is because the two wait states generated by the internal generator overlapped the first two wait states generated by the external ready signal. Note that the external ARDY and SRDY lines are always ignored during cycles accessing internal peripherals.

R2–R0 of each control word specifies the READY mode for the corresponding block, with the exception of the peripheral chip selects: R2–R0 of PACS set the $\overline{PCS0}$–3 READY mode, R2–R0 of MPCS set the $\overline{PCS4}$–6 READY mode.

Chip Select/Ready Logic and Reset

Upon RESET, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to insert 3 wait states in conjunction with external READY (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

DMA CHANNELS

The 80C186 DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data.

DMA Operation

Each channel has six registers in the control block which define each channel's operation. The control registers consist of a 20-bit Source pointer (2 words), a 20-bit destination pointer (2 words), a 16-bit Transfer Count Register, and a 16-bit Control Word. The format of the DMA Control Blocks is shown in Table 13. The Transfer Count Register (TC) specifies the number of DMA transfers to be performed. Up to 64K byte or word transfers can be performed with automatic termination. The Control Word defines the channel's operation (see Figure 17). All registers may be modified or altered during any DMA activity. Any changes made to these registers will be reflected immediately in DMA operation.

Table 13. DMA Control Block Format

Register Name	Register Address	
	Ch. 0	Ch. 1
Control Word	CAH	DAH
Transfer Count	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

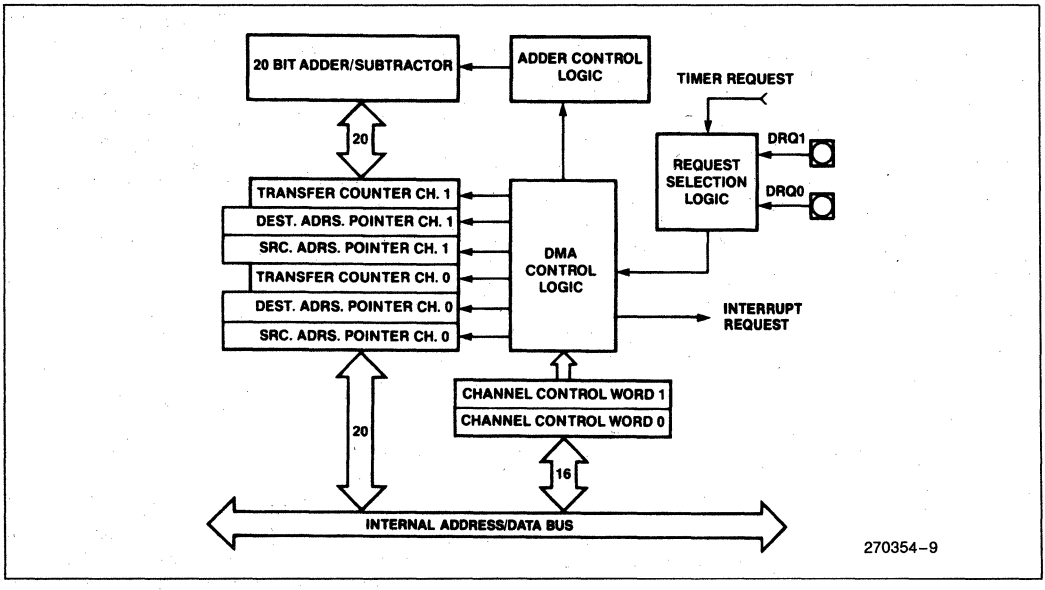


Figure 16. DMA Unit Block Diagram

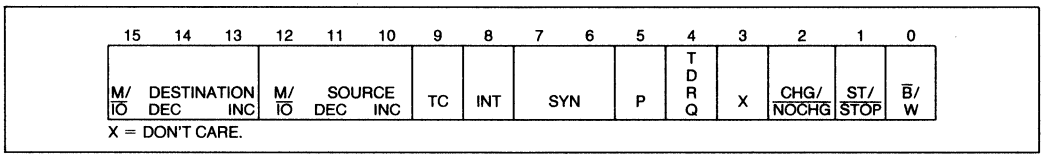


Figure 17. DMA Control Register

DMA Channel Control Word Register

Each DMA Channel Control Word determines the mode of operation for the particular 80C186 DMA channel. This register specifies:

- the mode of synchronization;
- whether bytes or words will be transferred;
- whether interrupts will be generated after the last transfer;
- whether DMA activity will cease after a programmed number of DMA cycles;
- the relative priority of the DMA channel with respect to the other DMA channel;
- whether the source pointer will be incremented, decremented, or maintained constant after each transfer;
- whether the source pointer addresses memory or I/O space;
- whether the destination pointer will be incremented, decremented, or maintained constant after each transfer; and
- whether the destination pointer will address memory or I/O space.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

DMA Control Word Bit Descriptions

DEST: M/$\overline{IO}$ Destination pointer is in memory (1) or I/O (0) space.

DEC Decrement destination pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

INC Increment destination pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

If both INC and DEC are specified, the pointer will remain constant after each cycle.

SOURCE: M/$\overline{IO}$ Source pointer is in memory (1) or I/O (0) space.

DEC Decrement source pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

INC Increment source pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

If both INC and DEC are specified, the pointer will remain constant after each cycle.

TC: If set, DMA will terminate when the contents of the transfer count register reach zero. The ST/$\overline{STOP}$ bit will also be reset at this point. If cleared, the DMA controller will decrement the transfer count register for each DMA cycle, but DMA transfers will not stop when the transfer count register reaches zero.

INT: Enable interrupts to CPU upon transfer count termination.

SYN: 00 No synchronization.

NOTE:

When unsynchronized transfers are specified, the TC bit will be ignored and the ST/$\overline{STOP}$ bit will be cleared upon the transfer count reaching zero, stopping the channel.

01 Source synchronization.

10 Destination synchronization.

11 Unused.

P: Channel priority relative to other channel during simultaneous requests.

0 Low priority.

1 High priority.

Channels will alternate cycles if both are set at same priority level.

TDRQ: Enable/Disable (1/0) DMA requests from timer 2.

CHG/$\overline{NOCHG}$: Change/Do not change (1/0) ST/$\overline{STOP}$ bit. If this bit is set when writing to the control word, the ST/$\overline{STOP}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{STOP}$ bit will not be altered. This bit is not stored; it will always be read as 0.

ST/$\overline{STOP}$: Start/Stop (1/0) channel.

$\overline{B}$/W: Byte/Word (0/1) transfers.

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DMA Destination and Source Pointer Registers

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. For each DMA channel to be used, all four pointer registers must be initialized. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address (see Figure 18). These pointers may be individually incremented or decremented after each transfer. If word transfers are performed the pointer is incremented or decremented by two.

Each pointer may point into either memory or I/O space. Since the upper four bits of the address are not automatically programmed to zero, the user must program them in order to address the normal 64K I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on values for the pointer registers. Higher transfer rates can be achieved if all word transfers are performed to or from even addresses so that accesses will occur in single bus cycles.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). The register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA Control Register. If the TC bit in the DMA control word is set or if unsynchronized transfers are programmed, however, DMA activity will terminate when the transfer count register reaches zero.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred. When source or unsynchronized transfers are performed, the DMA channel may begin another transfer immediately after the end of a previous DMA transfer. This allows a complete transfer to take place every 2 bus cycles or eight clock cycles (assuming no wait states). When destination synchronization is performed, data will not be fetched from the source address until the destination device signals that it is ready to receive it. When destination synchronized transfers are requested, the DMA controller will relinquish control of the bus after every transfer. If no other bus activity is initiated, another DMA cycle will begin after two processor clocks. This allows the destination device time to remove its request if another transfer is not desired. Since the DMA controller will relinquish the bus, the CPU can initiate a bus cycle. As a result, a complete bus cycle will often be inserted between destination synchronized transfers. Table 14 shows the maximum DMA transfer rates.

Table 14. Maximum DMA Transfer Rates at CLKOUT = 16 MHz

Type of Synchronization Selected	CPU Running	CPU Halted
Unsynchronized	4.0MBytes/sec	4.0MBytes/sec
Source Synch	4.0MBytes/sec	4.0MBytes/sec
Destination Synch	2.7MBytes/sec	3.2MBytes/sec

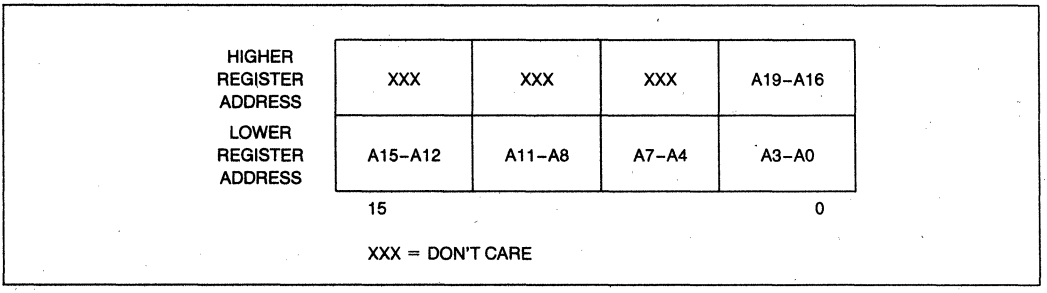

Figure 18. DMA Pointer Register Format

DMA Acknowledge

No explicit DMA acknowledge pulse is provided. Since both source and destination pointers are maintained, a read from a requesting source, or a write to a requesting destination, should be used as the DMA acknowledge signal. Since the chip-select lines can be programmed to be active for a given block of memory or I/O space, and the DMA pointers can be programmed to point to the same given block, a chip-select line could be used to indicate a DMA acknowledge.

DMA Priority

The DMA channels may be programmed to give one channel priority over the other, or they may be programmed to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses to odd memory locations; also an external bus hold takes priority over an internal DMA cycle. Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time will suffer during sequences of continuous DMA cycles. An NMI request, however, will cause all internal DMA activity to halt. This allows the CPU to quickly respond to the NMI request.

DMA Programming

DMA cycles will occur whenever the ST/$\overline{\text{STOP}}$ bit of the Control Register is set. If synchronized transfers are programmed, a DRQ must also be generated. Therefore the source and destination transfer pointers, and the transfer count register (if used) must be programmed before the ST/$\overline{\text{STOP}}$ bit is set.

Each DMA register may be modified while the channel is operating. If the CHG/NOCHG bit is cleared when the control register is written, the ST/$\overline{\text{STOP}}$ bit of the control register will not be modified by the write. If multiple channel registers are modified, it is recommended that a LOCKED string transfer be used to prevent a DMA transfer from occurring between updates to the channel registers.

DMA Channels and Reset

Upon RESET, the state of the DMA channels will be as follows:

- The ST/$\overline{\text{STOP}}$ bit for each channel will be reset to $\overline{\text{STOP}}$.
- Any transfer in progress is aborted.
- The values of the transfer count registers, source pointers, and destination pointers are indeterminate.

TIMERS

The 80C186 provides three internal 16-bit programmable timers (see Figure 19). Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

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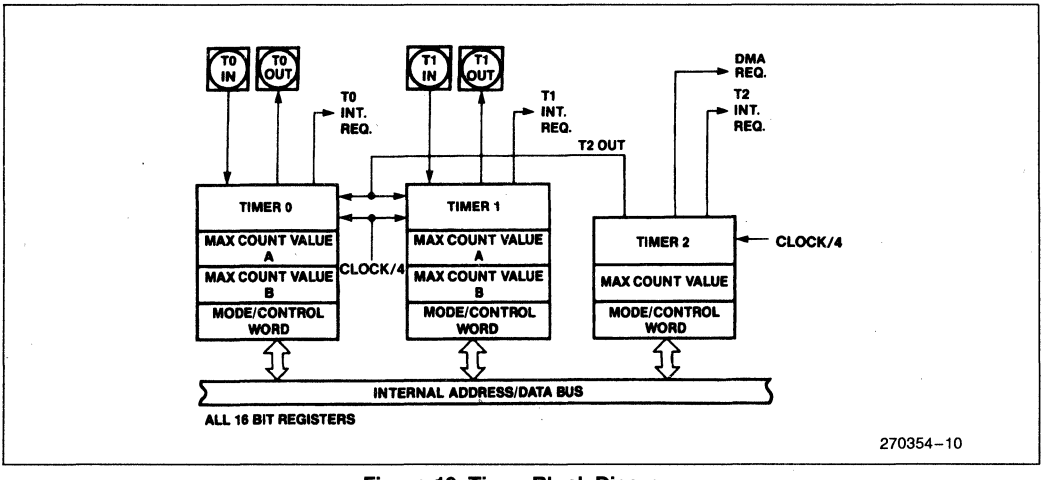


Figure 19. Timer Block Diagram

Timer Operation

The timers are controlled by 11 16-bit registers in the peripheral control block. The configuration of these registers is shown in Table 15. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a MAX COUNT register, which defines the maximum count the timer will reach. After reaching the MAX COUNT register value, the timer count value will reset to zero during that same clock, i.e., the maximum count value is never stored in the count register itself. Timers 0 and 1 are, in addition, equipped with a second MAX COUNT register, which enables the timers to alternate their count between two different MAX COUNT values. If a single MAX COUNT register is used, the timer output pin will switch LOW for a single clock, 1 clock after the maximum count value has been reached. In the dual MAX COUNT register mode, the output pin will indicate which MAX COUNT register is currently in use, thus allowing nearly complete freedom in selecting waveform duty cycles. For the timers with two MAX COUNT registers, the RIU bit in the control register determines which is used for the comparison.

Each timer gets serviced every fourth CPU-clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU-clock rate. Due to internal synchronization and pipelining of the timer circuitry, a timer output may take up to 6 clocks to respond to any individual clock or gate input.

Since the count registers and the maximum count registers are all 16 bits wide, 16 bits of resolution are provided. Any Read or Write access to the timers will add one wait state to the minimum four-clock bus cycle, however. This is needed to synchronize and coordinate the internal data flows between the internal timers and the internal bus.

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between MAX COUNT registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

These options are selectable via the timer mode/control word.

Timer Mode/Control Register

The mode/control register (see Figure 20) allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

Table 15. Timer Control Block Format

Register Name	Register Offset		
	Tmr. 0	Tmr. 1	Tmr. 2
Mode/Control Word	56H	5EH	66H
Max Count B	54H	5CH	not present
Max Count A	52H	5AH	62H
Count Register	50H	58H	60H

EN:

The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transistions during the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

$\overline{\text{INH}}$:

The inhibit bit allows for selective updating of the enable (EN) bit. If $\overline{\text{INH}}$ is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If $\overline{\text{INH}}$ is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT:

When set, the INT bit enables interrupts from the timer, which will be generated on every terminal

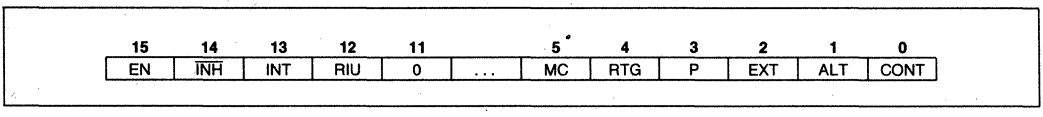


Figure 20. Timer Mode/Control Register

count. If the timer is configured in dual MAX COUNT register mode, an interrupt will be generated each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the Interrupt Controller).

RIU:

The Register In Use bit indicates which MAX COUNT register is currently being used for comparison to the timer count value. A zero value indicates register A. The RIU bit cannot be written, i.e., its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.

MC:

The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. This bit is set regardless of the timer's interrupt-enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts.

Programmer intervention is required to clear this bit.

RTG:

Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is HIGH, the timer will count; if the input pin is LOW, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the 80C186 clock.

When RTG = 1, the input pin detects LOW-to-HIGH transitions. The first such transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

P:

The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

EXT:

The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the 80C186 clock.

If this bit is set, the timer will count LOW-to-HIGH transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input to output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

ALT:

The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method of generating non-repetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will go LOW for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT:

Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset, and halt.

Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Count Registers

Each of the three timers has a 16-bit count register. The contents of this register may be read or written by the processor at any time. If the register is written while the timer is counting, the new value will take effect in the current count cycle.

The count registers should be programmed before attempting to use the timers since they are not automatically initialized to zero.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two max count values whenever the current maximum count is reached. A timer resets when the timer count register equals the max count value being used. If the timer count register or the max count register is changed so that the max count is less than the timer count, the timer does not immediately reset. Instead, the timer counts up to 0FFFFH, "wraps around" to zero, counts up to the max count value, and then resets.

Timers and Reset

Upon RESET, the state of the timers will be as follows:

- All EN (Enable) bits are reset preventing timer counting.
- For Timers 0 and 1, the RIU bits are reset to zero and the ALT bits are set to one. This results in the Timer Out pins going HIGH.
- The contents of the count registers are indeterminate.

INTERRUPT CONTROLLER

The 80C186 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The 80C186 interrupt controller has its own control register that sets the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Figure 21.

The 80C186 has a special Slave Mode in which the internal interrupt controller acts as a slave to an external master. The controller is programmed into this mode by setting bit 14 in the peripheral control block relocation register. (See Slave Mode section.)

MASTER MODE OPERATION

Interrupt Controller External Interface

Five pins are provided for external interrupt sources. One of these pins is NMI, the non-maskable interrupt. NMI is generally used for unusual events such as power-fail interrupts. The other four pins may be configured in any of the following ways:

- As four interrupt lines with internally generated interrupt vectors.
- As an interrupt line and interrupt acknowledge line pair (Cascade Mode) with externally generated interrupt vectors plus two interrupt input lines with internally generated vectors.
- As two pairs of interrupt/interrupt acknowledge lines (Cascade Mode) with externally generated interrupt vectors.

External sources in the Cascade Mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the 80C186 on the second cycle. The capability to interface to external 82C59A programmable interrupt controllers is provided when the inputs are configured in Cascade Mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in Master Mde are similar to the 82C59A. The interrupt controller responds identically to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

Fully Nested Mode

When in the fully nested mode four pins are used as direct interrupt requests as in Figure 22. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate with interrupts enabled, yet be suspended only by interrupts of higher priority than the in-service interrupt.

When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register. This is required to allow subsequent interrupts from this interrupt source and to allow servicing of lower-priority interrupts. An EOI command is executed at the end of the service routine just before the return from interrupt instruction. If the fully nested structure has been upheld, the next highest-priority source with its IS bit set is then serviced.

Cascade Mode

The 80C186 has four interrupt pins and two of them have dual functions. In the fully nested mode the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In the Cascade Mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. The interconnection is shown in Figure 23. INT0 is an interrupt input interfaced to an 82C59A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to that peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the Cascade Mode by programming the proper value into INT0 and INT1 control registers. The use of the dedicated acknowledge signals eliminates the need for the use of external logic to generate $\overline{\text{INTA}}$ and device select signals.

The primary Cascade Mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave 82C59As. Three levels of priority are created, requiring priority resolution in the 80C186 interrupt controller, the master 82C59As, and the slave 82C59As. If an external interrupt is serviced, one IS bit is set at each of these levels. When the interrupt service routine is completed, up to three end-of-interrupt commands must be issued by the programmer.

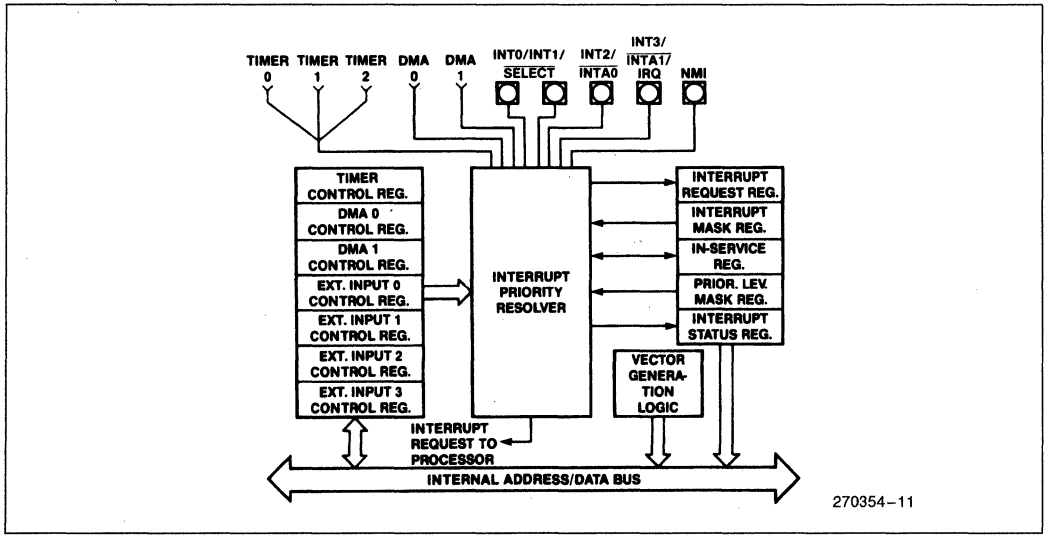


Figure 21. Interrupt Controller Block Diagram

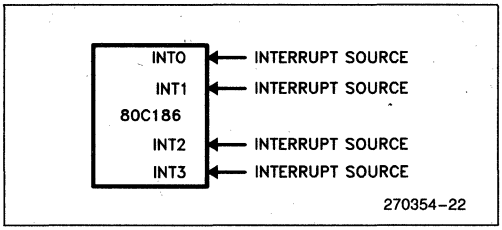


Figure 22. Fully Nested (Direct) Mode Interrupt Controller Connections

Special Fully Nested Mode

This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external 82C59A masters. Normally, an interrupt request from an interrupt source will not be recognized unless the in-service bit for that source is reset. If more than one interrupt source is connected to an external interrupt controller, all of the interrupts will be funneled through the same 80C186 interrupt request pin. As a result, if the external interrupt controller receives a higher-priority interrupt, its interrupt will not be recognized by the 80C186 controller until the 80C186 in-service bit is reset. In Special Fully Nested Mode, the 80C186 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interrupts from a single pin. An in-service bit will continue to be set, however, to inhibit interrupts from other lower-priority 80C186 interrupt sources.

Special procedures should be followed when resetting IS bits at the end of interrupt service routines. Software polling of the IS register in the external master 82C59A is required to determine if there is more than one bit set. If so, the IS bit in the 80C186 remains active and the next interrupt service routine is entered.

Operation in a Polled Environment

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the Poll Word (Figure 32). Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service. Bits 0–4 indicate to the processor the type vector of the highest-priority source requesting service. Reading the Poll Word causes the In-Service bit of the highest priority source to be set.

It is desirable to be able to read the Poll Word information without guaranteeing service of any pending interrupt, i.e., not set the indicated in-service bit. The 80C186 provides a Poll Status Word in addition to the conventional Poll Word to allow this to be done. Poll Word information is duplicated in the Poll Status Word, but reading the Poll Status Word does not set the associated in-service bit. These words are located in two adjacent memory locations in the register file.

Master Mode Features

Programmable Priority

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority). All interrupt sources have preprogrammed default priority levels (see Table 4).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 4 is used. If the serviced interrupt routine reenables interrupts, other interrupt requests can be serviced.

End-of-Interrupt Command

The end-of-interrupt (EOI) command is used by the programmer to reset the In-Service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The nonspecific command does not specify which IS bit is reset. When issued, the interrupt controller automatically resets the IS bit of the highest priority source with an active service routine. A specific EOI command requires that the programmer send the interrupt vector type to the interrupt controller indicating which source's IS bit is to be reset. This command is used when the fully nested structure has been disturbed or the highest priority IS bit that was set does not belong to the service routine in progress.

Trigger Mode

The four external interrupt pins can be programmed in either edge- or level-trigger mode. The control register for each external source has a level-trigger mode (LTM) bit. All interrupt inputs are active HIGH. In the edge sense mode or the level-trigger mode, the interrupt request must remain active (HIGH) until the interrupt request is acknowledged by the

80C186 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go LOW for at least one clock cycle to re-enable the input. In the level-trigger mode, no such provision is made: holding the interrupt input HIGH will cause continuous interrupt requests.

Interrupt Vectoring

The 80C186 Interrupt Controller will generate interrupt vectors for the integrated DMA channels and the integrated Timers. In addition, the Interrupt Controller will generate interrupt vectors for the external interrupt lines if they are not configured in Cascade or Special Fully Nested Modes. The interrupt vectors generated are fixed and cannot be changed (see Table 4).

Interrupt Controller Registers

The Interrupt Controller register model is shown in Figure 24. It contains 15 registers. All registers can both be read or written unless specified otherwise.

In-Service Register

This register can be read from or written into. The format is shown in Figure 25. It contains the In-Service bit for each of the interrupt sources. The In-Service bit is set to indicate that a source's service routine is in progress. When an In-Service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the In-Service bit for all three timers; the D0 and D1 bits are the In-Service bits for the two DMA channels; the I0–I3 are the In-Service bits for the external interrupt pins. The IS bit is set when the processor acknowledges an interrupt request either by an interrupt acknowledge or by reading the poll register. The IS bit is reset at the end of the interrupt service routine by an end-of-interrupt command.

Interrupt Request Register

The internal interrupt sources have interrupt request bits inside the interrupt controller. The format of this register is shown in Figure 25. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

The state of the external interrupt input pins is also indicated. The state of the external interrupt pins is not a stored condition inside the interrupt controller, therefore the external interrupt bits cannot be written. The external interrupt request bits are set when an interrupt request is given to the interrupt controller, so if edge-triggered mode is selected, the bit in the register will be HIGH only after an inactive-to-active transition. For internal interrupt sources, the register bits are set when a request arrives and are reset when the processor acknowledges the requests.

Writes to the interrupt request register will affect the D0 and D1 interrupt request bits. Setting either bit will cause the corresponding interrupt request while clearing either bit will remove the corresponding interrupt request. All other bits in the register are read-only.

Mask Register

This is a 16-bit register that contains a mask bit for each interrupt source. The format for this register is shown in Figure 25. A one in a bit position corre-

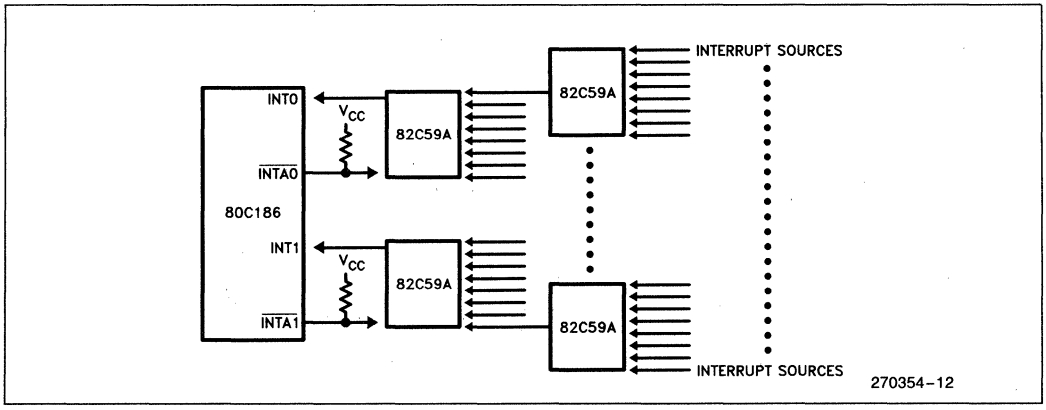


Figure 23. Cascade and Special Fully Nested Mode Interrupt Controller Connections

sponding to a particular source masks the source from generating interrupts. These mask bits are the exact same bits which are used in the individual control registers; programming a mask bit using the mask register will also change this bit in the individual control registers, and vice versa.

	OFFSET
INT3 CONTROL REGISTER	3EH
INT2 CONTROL REGISTER	3CH
INT1 CONTROL REGISTER	3AH
INT0 CONTROL REGISTER	38H
DMA 1 CONTROL REGISTER	36H
DMA 0 CONTROL REGISTER	34H
TIMER CONTROL REGISTER	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY MASK REGISTER	2AH
MASK REGISTER	28H
POLL STATUS REGISTER	26H
POLL REGISTER	24H
EOI REGISTER	22H

Figure 24. Interrupt Controller Registers (Master Mode)

Priority Mask Register

This register masks all interrupts below a particular interrupt priority level. The format of this register is shown in Figure 26. The code in the lower three bits of this register inhibits interrupts of priority lower (a higher priority number) than the code specified. For example, 100 written into this register masks interrupts of level five (101), six (110), and seven (111). The register is reset to seven (111) upon RESET so no interrupts are masked due to priority number.

Interrupt Status Register

This register contains general interrupt controller status information. The format of this register is shown in Figure 27. The bits in the status register have the following functions:

DHLT: DMA Halt Transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed. This bit allows prompt service of all non-maskable interrupts. This bit may also be set by the programmer.

IRTx: These three bits represent the individual timer interrupt request bits. These bits differentiate between timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt request. Note that setting any one of these three bits initiates an interrupt request to the interrupt controller.

15	14	•	•	•	10	9	8	7	6	5	4	3	2	1	0
0	0				0	0	0	I3	I2	I1	I0	D1	D0	0	TMR

Figure 25. In-Service, Interrupt Request, and Mask Register Formats

15	14	•	•	•	•	•	•	•	•	•	3	2	1	0
0	0										0	PRM2	PRM1	PRM0

Figure 26. Priority Mask Register Format

15	14	•	•	•	•	•	7	6	5	4	3	2	1	0
DHLT	0						0	0	0	0	0	IRT2	IRT1	IRT0

Figure 27. Interrupt Status Register Format (Master Mode)

Timer, DMA 0, 1; Control Register

These registers are the control words for all the internal interrupt sources. The format for these registers is shown in Figure 28. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits its interrupt requests from the interrupt source. The MSK bits in the individual control registers are the exact same bits as are in the Mask Register; modifying them in the individual control registers will also modify them in the Mask Register, and vice versa.

INT0-INT3 Control Registers

These registers are the control words for the four external input pins. Figure 29 shows the format of the INT0 and INT1 Control registers; Figure 30 shows the format of the INT2 and INT3 Control registers. In Cascade Mode or Special Fully Nested Mode, the control words for INT2 and INT3 are not used.

The bits in the various control registers are encoded as follows:

PRO-2: Priority programming information. Highest Priority = 000, Lowest Priority = 111

LTM: Level-trigger mode bit. 1 = level-triggered; 0 = edge-triggered. Interrupt Input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = non-mask.

C: Cascade mode bit, 1 = cascade; 0 = direct

SFNM: Special Fully Nested Mode bit, 1 = SFNM

EOI Register

The end of the interrupt register is a command register which can only be written into. The format of this register is shown in Figure 31. It initiates an EOI command when written to by the 80C186 CPU.

The bits in the EOI register are encoded as follows:

S_X: Encoded information that specifies an interrupt source vector type as shown in Table 4. For example, to reset the In-Service bit for DMA channel 0, these bits should be set to 01010, since the vector type for DMA channel 0 is 10.

NOTE:

To reset the single In-Service bit for any of the three timers, the vector type for timer 0 (8) should be written in this register.

NSPEC/SPEC: A bit that determines the type of EOI command. Nonspecific = 1, Specific = 0.

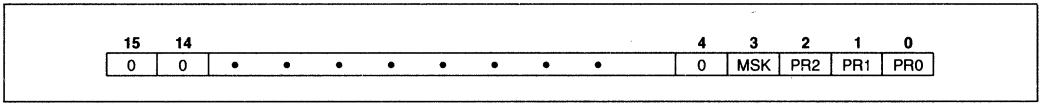


Figure 28. Timer/DMA Control Registers Formats

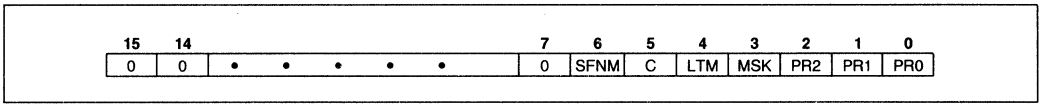


Figure 29. INT0/INT1 Control Register Formats

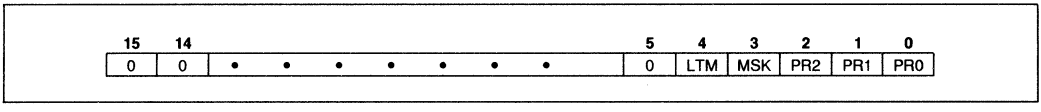


Figure 30. INT2/INT3 Control Register Formats

Poll and Poll Status Registers

These registers contain polling information. The format of these registers is shown in Figure 32. They can only be read. Reading the Poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt. Reading the poll status register will not set the IS bit of the highest priority pending interrupt; only the status of pending interrupts will be provided.

Encoding of the Poll and Poll Status register bits are as follows:

S_x: Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt Request = 1; no Interrupt Request = 0.

SLAVE MODE OPERATION

When Slave Mode is used, the internal 80C186 interrupt controller will be used as a slave controller to an external master interrupt controller. The internal 80C186 resources will be monitored by the internal interrupt controller, while the external controller functions as the system master interrupt controller.

Upon reset, the 80C186 will be in master mode. To provide for slave mode operation bit 14 of the relocation register should be set.

Because of pin limitations caused by the need to interface to an external 82C59A master, the internal interrupt controller will no longer accept external inputs. There are however, enough 80C186 interrupt controller inputs (internally) to dedicate one to each timer. In this mode, each timer interrupt source has its own mask bit, IS bit, and control word.

In Slave Mode each peripheral must be assigned a unique priority to ensure proper interrupt controller operation. Therefore, it is the programmer's responsibility to assign correct priorities and initialize interrupt control registers before enabling interrupts.

Slave Mode External Interface

The configuration of the 80C186 with respect to an external 82C59A master is shown in Figure 33. The INT0 (Pin 45) input is used as the 80C186 CPU interrupt input. IRQ (Pin 41) functions as an output to send the 80C186 slave-interrupt-request to one of the 8 master-PIC-inputs.

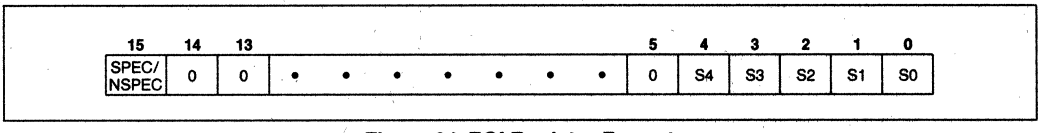


Figure 31. EOI Register Format

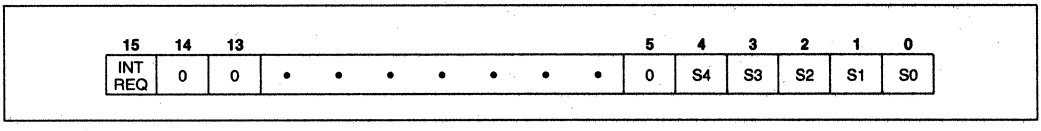


Figure 32. Poll and Poll Status Register Format

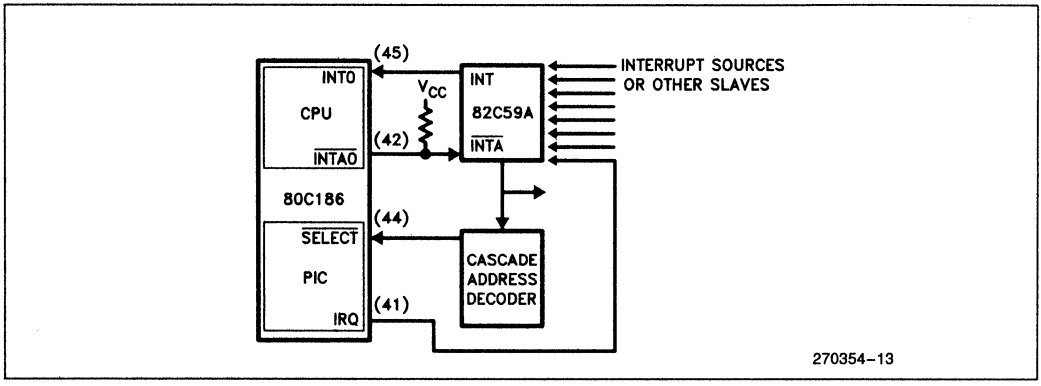


Figure 33. Slave Mode Interrupt Controller Connections

Correct master-slave interface requires decoding of the slave addresses (CAS0-2). Slave 82C59As do this internally. Because of pin limitations, the 80C186 slave address will have to be decoded externally. SELECT (Pin 44) is used as a slave-select input. Note that the slave vector address is transferred internally, but the READY input must be supplied externally.

INTA0 (Pin 42) is used as an acknowledge output, suitable to drive the INTA input of an 82C59A.

Interrupt Nesting

Slave Mode operation allows nesting of interrupt requests. When an interrupt is acknowledged, the priority logic masks off all priority levels except those with equal or higher priority.

Vector Generation in the Slave Mode

Vector generation in Slave Mode is exactly like that of an 8259A or 82C59A slave. The interrupt controller generates an 8-bit vector type number which the CPU multiplies by four to use as an address into the vector table. The five most significant bits of this type number are user-programmable while the three least significant bits are defined according to Figure 34. The significant five bits of the vector are programmed by writing to the Interrupt Vector register at offset 20H.

Specific End-of-Interrupt

In Slave Mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset. The command is executed by writing the correct value in the Specific EOI register at offset 22H.

Interrupt Controller Registers in the Slave Mode

All control and command registers are located inside the internal peripheral control block. Figure 34 shows the offsets of these registers.

End-of-Interrupt Register

The end-of-interrupt register is a command register which can only be written. The format of this register is shown in Figure 35. It initiates an EOI command when written by the 80C186 CPU.

The bits in the EOI register are encoded as follows:

VT_X: Three least-significant vector type bits corresponding to the source for which the IS bit is to be reset. Figure 34 indicates these bits.

24

In-Service Register

This register can be read from or written into. It contains the in-service bit for each of the internal interrupt sources. The format for this register is shown in Figure 36. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers. The source's IS bit is set when the processor acknowledges its interrupt request.

Interrupt Request Register

This register indicates which internal peripherals have interrupt requests pending. The format of this register is shown in Figure 36. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request. As in Master Mode, D0 and D1 are read/write; all other bits are read only.

Mask Register

This register contains a mask bit for each interrupt source. The format for this register is shown in Figure 36. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked. These mask bits are exactly the same bits which are used in the individual control registers, i.e., changing the state of a mask bit in this register will also change the state of the mask bit in the individual interrupt control register corresponding to the bit.

Control Registers

These registers are the control words for all the internal interrupt sources. The format of these registers is shown in Figure 37. Each of the timers and both of the DMA channels have their own Control Register.

The bits of the Control Registers are encoded as follows:

pr_x: 3-bit encoded field indicating a priority level for the source.

msk: mask bit for the priority level indicated by pr_x bits.

	OFFSET
TIMER 2 CONTROL REGISTER (VECTOR TYPE XXXXX101)	3AH
TIMER 1 CONTROL REGISTER (VECTOR TYPE XXXXX100)	38H
DMA1 CONTROL REGISTER (VECTOR TYPE XXXXX011)	36H
DMA0 CONTROL REGISTER (VECTOR TYPE XXXXX010)	34H
TIMER0 CONTROL REGISTER (VECTOR TYPE XXXXX000)	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT-REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY-LEVEL MASK REGISTER	2AH
MASK REGISTER	28H
SPECIFIC EOI REGISTER	22H
INTERRUPT VECTOR REGISTER	20H

Figure 34. Interrupt Controller Registers (Slave Mode)

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	0	0	0	VT2	VT1	VT0

Figure 35. Specific EOI Register Format

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	TMR2	TMR1	D1	D0	0	TMR0

Figure 36. In-Service, Interrupt Request, and Mask Register Format

Interrupt Vector Register

This register provides the upper five bits of the interrupt vector address. The format of this register is shown in Figure 38. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.

The format of the bits in this register is:

t_x: 5-bit field indicating the upper five bits of the vector address.

Priority-Level Mask Register

This register indicates the lowest priority-level interrupt which will be serviced.

The encoding of the bits in this register is:

m_x: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

Interrupt Status Register

This register is defined as in Master Mode except that DHLT is not implemented (see Figure 27).

Interrupt Controller and Reset

Upon RESET, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying Fully Nested Mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All Interrupt Service bits reset to 0.
- All Interrupt Request bits reset to 0.
- All MSK (Interrupt Mask) bits set to 1 (mask).
- All C (Cascade) bits reset to 0 (non-Cascade).
- All PRM (Priority Mask) bits set to 1, implying no levels masked.
- Initialized to Master Mode.

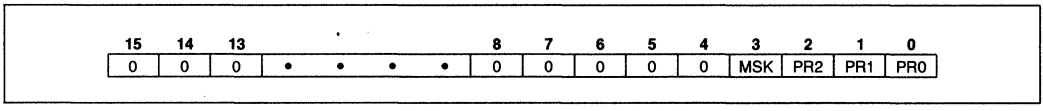


Figure 37. Control Word Format

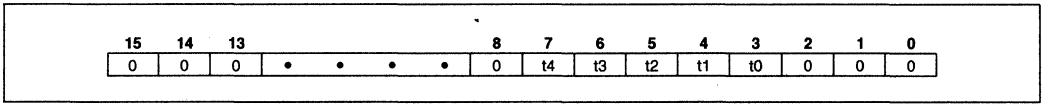


Figure 38. Interrupt Vector Register Format

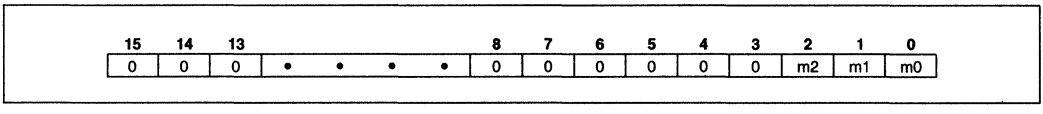


Figure 39. Priority Level Mask Register

Enhanced Mode Operation

In Compatible Mode the 80C186 operates with all the features of the NMOS 80186, with the exception of 8087 support (i.e. no numeric coprocessing is possible in Compatible Mode). Queue-Status information is still available for design purposes other than 8087 support.

All the Enhanced Mode features are completely masked when in Compatible Mode. A write to any of the Enhanced Mode registers will have no effect, while a read will not return any valid data.

In Enhanced Mode, the 80C186 will operate with Power-Save, DRAM refresh, and numerics coprocessor support in addition to all the Compatible Mode features.

Entering Enhanced Mode

If connected to a numerics coprocessor, this mode will be invoked automatically. Without an NPX, this mode can be entered by tying the RESET output signal from the 80C186 to the TEST/BUSY input.

Queue-Status Mode

The queue-status mode is entered by strapping the $\overline{RD}$ pin low. $\overline{RD}$ is sampled at RESET and if LOW, the 80C186 will reconfigure the ALE and $\overline{WR}$ pins to be QS0 and QS1 respectively. This mode is available on the 80C186 in both Compatible and Enhanced Modes.

DRAM Refresh Control Unit Description

The Refresh Control Unit (RCU) automatically generates DRAM refresh bus cycles. The RCU operates only in Enhanced Mode. After a programmable period of time, the RCU generates a memory read request to the BIU. If the address generated during a refresh bus cycle is within the range of a properly programmed chip select, that chip select will be activated when the BIU executes the refresh bus cycle. The ready logic and wait states programmed for that region will also be in force. If no chip select is activated, then external ready is automatically required to terminate the refresh bus cycle.

If the HLDA pin is active when a DRAM refresh request is generated (indicating a bus hold condition), then the 80C186 will deactivate the HLDA pin in order to perform a refresh cycle. The circuit external to the 80C186 must remove the HOLD signal for at least one clock in order to execute the refresh cycle. The sequence of HLDA going inactive while HOLD is being held active can be used to signal a pending refresh request.

All registers controlling DRAM refresh may be read and written in Enhanced Mode. When the processor is operating in Compatible Mode, they are deselected and are therefore inaccessible. Some fields of these registers cannot be written and are always read as zeros.

DRAM Refresh Addresses

The address generated during a refresh cycle is determined by the contents of the MDRAM register (see Figure 40) and the contents of a 9-bit counter. Figure 41 illustrates the origin of each bit.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDRAM: Offset E0H	M6	M5	M4	M3	M2	M1	M0	0	0	0	0	0	0	0	0	0

Bits 0–8: Reserved, read back as 0.

Bits 9–15: M0–M6, are address bits A13–A19 of the 20-bit memory refresh address. These bits should correspond to any chip select address to be activated for the DRAM partition. These bits are cleared to 0 on RESET.

Figure 40. Memory Partition Register

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
M6	M5	M4	M3	M2	M1	M0	0	0	0	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	1

M6–M0: Bits defined by MDRAM Register

CA8–CA0: Bits defined by refresh address counter. These bits change according to a linear/feedback shift register; they do not directly follow a binary count.

Figure 41. Addresses Generated by RCU

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDRAM: Offset E2H	0	0	0	0	0	0	0	C8	C7	C6	C5	C4	C3	C2	C1	C0

Bits 0–8: C0–C8, clock divisor register, holds the number of CLKOUT cycles between each refresh request.

Bits 9–15: Reserved, read back as 0.

Figure 42. Clock Pre-Scaler Register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EDRAM: Offset E4H	E	0	0	0	0	0	0	T8	T7	T6	T5	T4	T3	T2	T1	T0

Bits 0–8: T0–T8, refresh clock counter outputs. Read only.

Bits 9–14: Reserved, read back as 0.

Bit 15: Enable RCU, set to 0 on RESET.

Figure 43. Enable RCU Register

Refresh Control Unit Programming and Operation

After programming the MDRAM and the CDRAM registers (Figures 40 and 42), the RCU is enabled by setting the "E" bit in the EDRAM register (Figure 43). The clock counter (T0–T8 of EDRAM) will be loaded from C0–C8 of CDRAM during T_3 of instruction cycle that sets the "E" bit. The clock counter is then decremented at each subsequent CLKOUT.

A refresh is requested when the value of the counter has reached 1 and the counter is reloaded from CDRAM. In order to avoid missing refresh requests, the value in the CDRAM register should always be at least 18 (12H). Clearing the "E" bit at anytime will clear the counter and stop refresh requests, but will not reset the refresh address counter.

POWER-SAVE CONTROL

Power Save Operation

The 80C186, when in Enhanced Mode, can enter a power saving state by internally dividing the processor clock frequency by a programmable factor. This divided frequency is also available at the CLKOUT pin. The PDCON register contains the two-bit fields for selecting the clock division factor and the enable bit.

All internal logic, including the Refresh Control Unit and the timers, will have their clocks slowed down by the division factor. To maintain a real time count or a fixed DRAM refresh rate, these peripherals must be re-programmed when entering and leaving the power-save mode.

The power-save mode is exited whenever an interrupt is processed by automatically resetting the enable bit. If the power-save mode is to be re-entered after serving the interrupt, the enable bit will need to be set in software before returning from the interrupt routine.

The internal clocks of the 80C186 will begin to be divided during the T_3 state of the instruction cycle that sets the enable bit. Clearing the enable bit will restore full speed in the T_3 state of that instruction.

At no time should the internal clock frequency be allowed to fall below 0.5 MHz. This is the minimum operational frequency of the 80C186. For example, an 80C186 running with a 12 MHz crystal (6 MHz CLOCKOUT) should never have a clock divisor greater than eight.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDCON: Offset F0H	E	0	0	0	0	0	0	0	0	0	0	0	0	0	F1	F0

Bits 0–1: Clock Divisor Select

F1	F0	Division Factor
0	0	divide by 1
0	1	divide by 4
1	0	divide by 8
1	1	divide by 16

Bits 2–14: Reserved, read back as zero.

Bit 15: Enable Power Save Mode. Set to zero on RESET.

Figure 44. Power-Save Control Register

Interface for 80C187 Numeric Processor Extension

In Enhanced Mode, three of the mid-range memory chip selects are redefined according to Table 16 for use with the 80C187. The fourth chip select, $\overline{MCS2}$ functions as in compatible mode, and may be programmed for activity with ready logic and wait states accordingly. As in compatible mode, $\overline{MCS2}$ will function for one-fourth a programmed block size.

Table 16. $\overline{MCS}$ Assignments

Compatible Mode	Enhanced Mode	
$\overline{MCS0}$	PEREQ	Processor Extension Request
$\overline{MCS1}$	$\overline{ERROR}$	NPX Error
$\overline{MCS2}$	$\overline{MCS2}$	Mid-Range Chip Select
$\overline{MCS3}$	$\overline{NPS}$	Numeric Processor Select

Four port addresses are assigned to the 80C186/80C187 interface for 16-bit reads and writes. Table 17 shows the port definitions. These ports are not accessible by using the 80C186 I/O instructions. However, numerics operations will cause a $\overline{PCS}$ line to be activated if it is properly programmed for this I/O range.

Table 17. Numerics Coprocessor I/O Port Assignments

I/O Address	Read Definition	Write Definition
00F8H	Status/Control	Opcode
00FAH	Data	Data
00FCH	reserved	CS:IP, DS:EA
00FEH	Opcode Status	reserved

ONCE™ Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C186 has a test mode available which allows all pins to be placed in a high-impedance state. ONCE stands for "ON Circuit Emulation". When placed in this mode, the 80C186 will put all pins in the high-impedance state until RESET.

The ONCE mode is selected by tying the $\overline{UCS}$ and the $\overline{LCS}$ LOW during RESET. These pins are sampled on the low-to-high transition of the $\overline{RES}$ pin. The $\overline{UCS}$ and the $\overline{LCS}$ pins have weak internal pull-up resistors similar to the $\overline{RD}$ and $\overline{TEST}$/BUSY pins to guarantee normal operation.

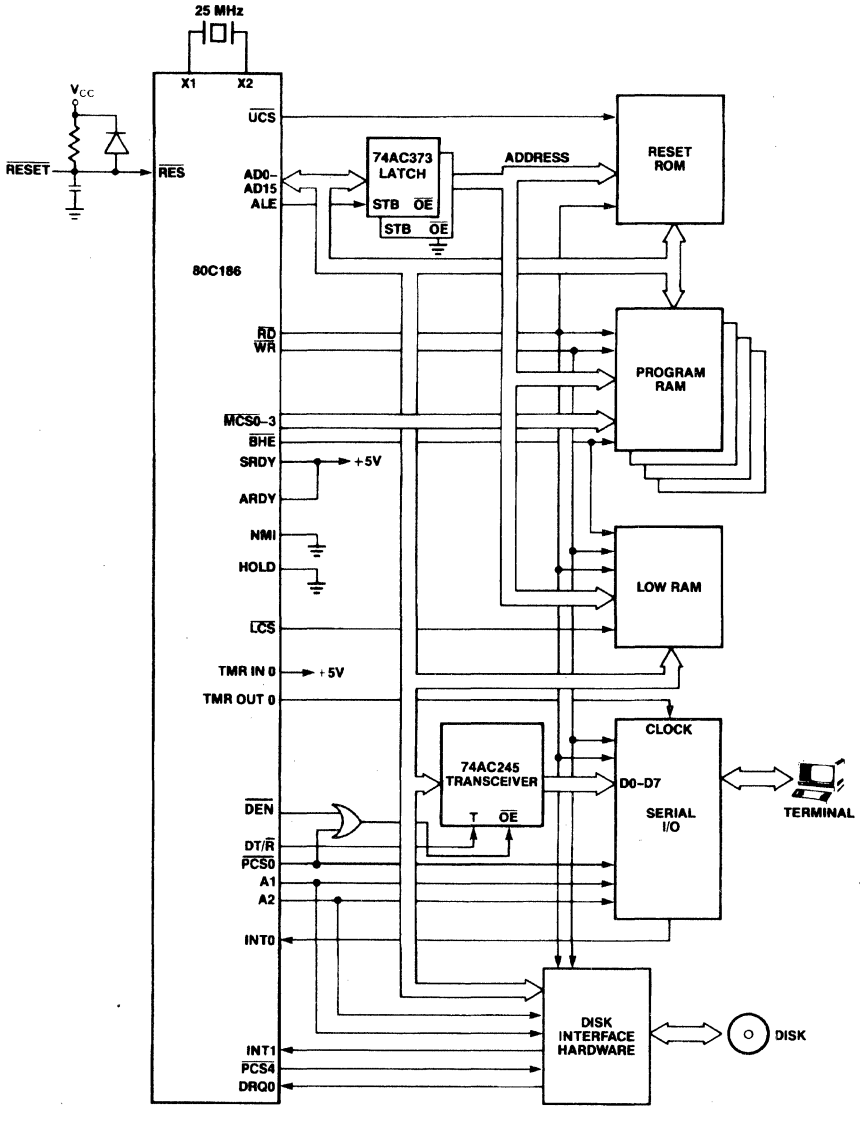


Figure 45. Typical 80C186 Computer

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias .... 0°C to +70°C

Storage Temperature ..... −65°C to +150°C

Voltage on Any Pin with Respect to Ground ..... −1.0V to +7.0V

Package Power Dissipation 1W

Not to exceed the maximum allowable die temperature based on thermal resistance of the package.

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: This data sheet is only valid for devices indicated in the Specification Level Markings section. Specifications contained in the following tables are subject to change.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±10% except V_{CC} = 5V ± 5% at f > 12.5 MHz

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except X1)	−0.5	0.2 V_{CC} − 0.3	V	
V_{IL1}	Clock Input Low Voltage (X1)	−0.5	0.6	V	
V_{IH}	Input High Voltage (All except X1, $\overline{RES}$, ARDY, and SRDY)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage (SRDY, ARDY)	0.2 V_{CC} + 1.1	V_{CC} + 0.5	V	
V_{IH3}	Clock Input High Voltage (X1)	3.9	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA (S0, 1, 2) I_{OL} = 2.0 mA (others)
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −2.4 mA @ 2.4V (4)
		V_{CC} − 0.5	V_{CC}	V	I_{OH} = −200 μA @ V_{CC} −0.5(4)
I_{CC}	Power Supply Current		150	mA	@ 16 MHz, 0°C V_{CC} = 5.25V (3)
			120	mA	@ 12.5 MHz, 0°C V_{CC} = 5.5V (3)
			100	mA	@ 10 MHz, 0°C V_{CC} = 5.5V (3)
I_{LI}	Input Leakage Current		±10	μA	@ 0.5 MHz, 0.45V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	μA	@ 0.5 MHz, 0.45V ≤ V_{OUT} ≤ V_{CC}(1)
V_{CLO}	Clock Output Low		0.45	V	I_{CLO} = 4.0 mA
V_{CHO}	Clock Output High	V_{CC} − 0.5		V	I_{CHO} = −500 μA
C_{IN}	Input Capacitance		10	pF	@ 1 MHz(2)
C_{IO}	Output or I/O Capacitance		20	pF	@ 1 MHz(2)

NOTES:

1. Pins being floated during HOLD or by invoking the ONCE Mode.
2. Characterization conditions are a) Frequency = 1 MHz; b) Unmeasured pins at GND; c) V_{IN} at + 5.0V or 0.45V. This parameter is not tested.
3. Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.
4. $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$, and $\overline{TEST}$/BUSY pins have internal pullup devices. Loading some of these pins above I_{OH} = −200 μA can cause the 80C186 to go into alternative modes of operation. See the section on Local Bus Controller and Reset for details.

POWER SUPPLY CURRENT

Current is linearly proportional to clock frequency and is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.

Maximum current is given by I_{CC} = 8.4 mA × freq. (MHz) + 15 mA.

Typical current is given by I_{CC} (typical) = 6.4 mA × freq. (MHz) + 4.0 mA. "Typicals" are based on a limited number of samples taken from early manufacturing lots measured at V_{CC} = 5V and room temperature. "Typicals" are not guaranteed.

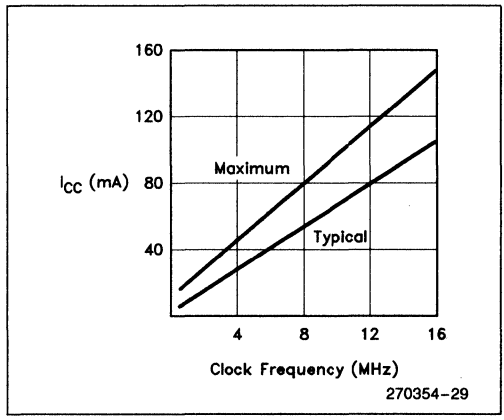


Figure 46. I_{CC} vs Frequency

A. C. CHARACTERISTICS

MAJOR CYCLE TIMINGS (READ CYCLE)

$T_A = 0^\circ C$ to $+70^\circ C$, V_{CC} = 5V ± 10% except V_{CC} = 5V± 5% at f > 12.5 MHz

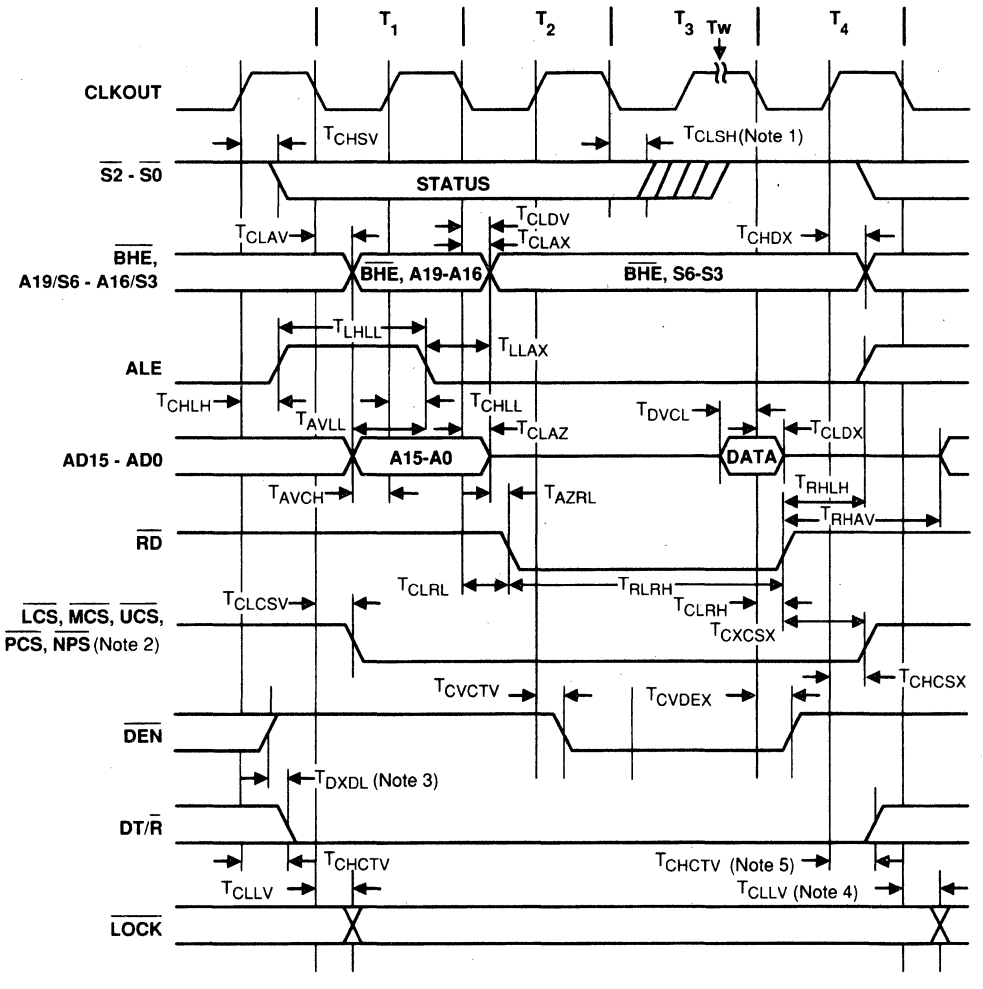
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	80C186		80C186-12		80C186-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C186 GENERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{DVCL}	Data in Setup (A/D)	15		15		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		3		ns	
80C186 GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	5	45	5	35	5	31	ns	
T_{CLSH}	Status Inactive Delay	5	46	5	35	5	30	ns	
T_{CLAV}	Address Valid Delay	5	44	5	36	5	33	ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	5	40	5	36	5	33	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		30		25		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		T_{CLCL} - 15		T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 18		T_{CLCH} - 15		T_{CLCH} - 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} - 15		T_{CHCL} - 15		T_{CHCL} - 15		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	T_{CLAX}	20	ns	
T_{CLCSV}	Chip-Select Active Delay	3	42	3	33	3	30	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} - 10		T_{CLCH} - 10		T_{CLCH} - 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	5	35	5	30	5	25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	44	3	37	3	31	ns	
T_{CVDEX}	$\overline{DEN}$ Inctive Delay	5	44	5	37	5	31	ns	
T_{CHCTV}	Control Active Delay 2	5	44	5	37	5	31	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	3	35	ns	
80C186 TIMING RESPONSES (Read Cycle)									
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	5	44	5	37	5	31	ns	
T_{RLRH}	$\overline{RD}$ Pulse Width	$2T_{CLCL}$ - 30		$2T_{CLCL}$ - 25		$2T_{CLCL}$ - 25		ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	5	44	5	37	5	31	ns	
T_{RHLH}	$\overline{RD}$ Inactive to ALE High	T_{CLCH} - 14		T_{CLCH} - 14		T_{CLCH} - 14		ns	Equal Loading
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	T_{CLCL} - 15		T_{CLCL} - 15		T_{CLCL} - 15		ns	Equal Loading

270354-34

A. C. CHARACTERISTICS

READ CYCLE WAVEFORMS



NOTES:

1. Status inactive in state preceding T_4 .
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by write.

270354-35

24

A. C. CHARACTERISTICS

MAJOR CYCLE TIMINGS (WRITE CYCLE)

$T_A = 0^\circ C$ to $+70^\circ C$, V_{CC} = 5V ± 10% except V_{CC} = 5V± 5% at f > 12.5 MHz

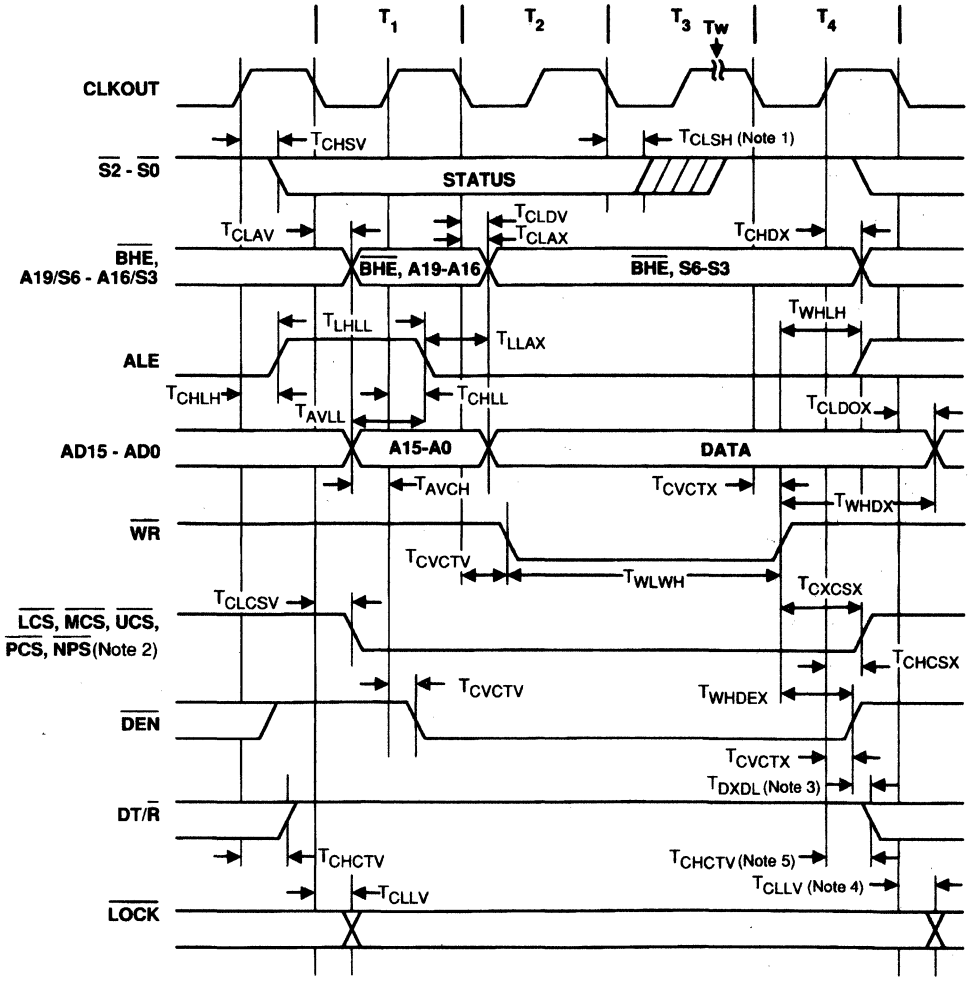
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC}$ - 0.5V.

Symbol	Parameter	80C186		80C186-12		80C186-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C186 GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	5	45	5	35	5	31	ns	
T_{CLSH}	Status Inactive Delay	5	46	5	35	5	30	ns	
T_{CLAV}	Address Valid Delay	5	44	5	36	5	33	ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	5	40	5	36	5	33	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		30		25		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		T_{CLCL} - 15		T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 18		T_{CLCH} - 15		T_{CLCH} - 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} - 15		T_{CHCL} - 15		T_{CHCL} - 15		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLDOX}	Data Hold Time	3		3		3		ns	
T_{CVCTV}	Control Active Delay 1	3	44	3	37	3	31	ns	
T_{CVCTX}	Control Inactive Delay	3	44	3	37	3	31	ns	
T_{CLCSV}	Chip-Select Active Delay	3	42	3	33	3	30	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} - 10		T_{CLCH} - 10		T_{CLCH} - 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	5	35	5	30	5	25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	3	35	ns	
80C186 TIMING RESPONSES (Write Cycle)									
T_{WLWH}	$\overline{WR}$ Pulse Width	$2T_{CLCL}$ - 30		$2T_{CLCL}$ - 25		$2T_{CLCL}$ - 25		ns	
T_{WHLH}	$\overline{WR}$ Inactive to ALE High	T_{CLCH} - 14		T_{CLCH} - 14		T_{CLCH} - 14		ns	Equal Loading
T_{WHDX}	Data Hold After $\overline{WR}$	T_{CLCL} - 34		T_{CLCL} - 20		T_{CLCL} - 20		ns	Equal Loading
T_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	T_{CLCH} - 10		T_{CLCH} - 10		T_{CLCH} - 10		ns	Equal Loading

270354-36

A. C. CHARACTERISTICS

WRITE CYCLE WAVEFORMS



NOTES:

1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by read, INTA, or halt.

270354-37

24

A. C. CHARACTERISTICS

MAJOR CYCLE TIMINGS (INTERRUPT ACKNOWLEDGE CYCLE)

$T_A = 0^\circ C$ to $+70^\circ C$, V_{CC} = 5V ± 10% except V_{CC} = 5V± 5% at f > 12.5 MHz

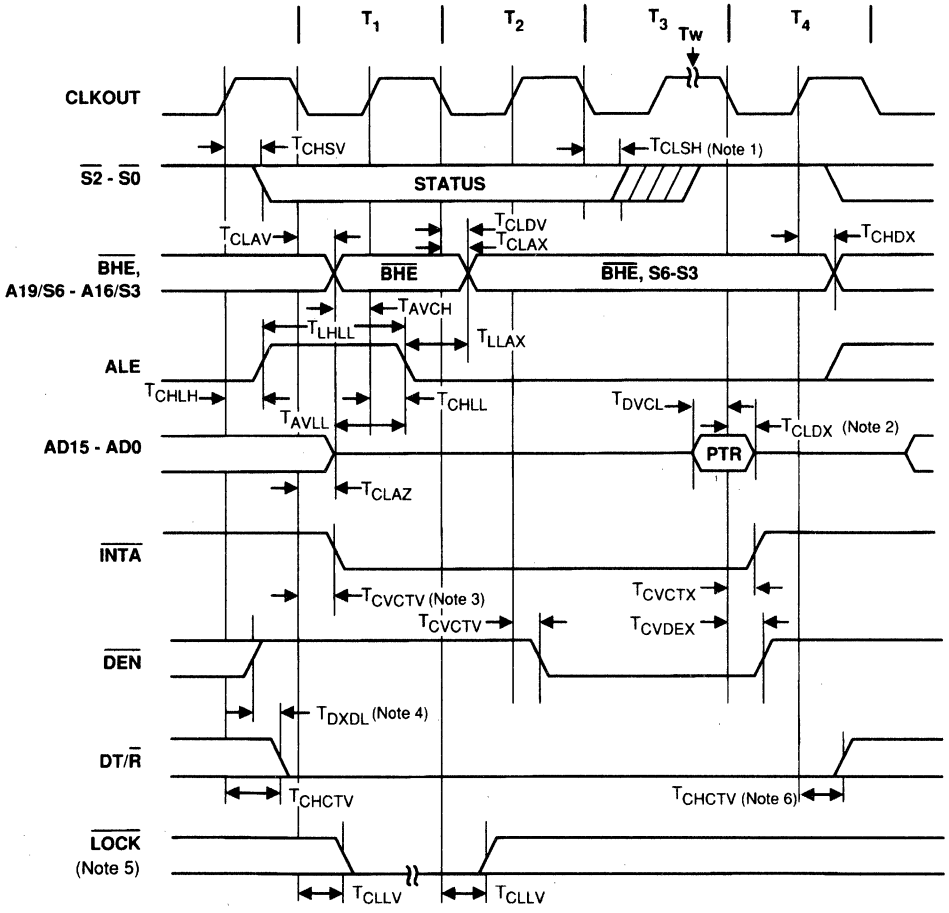
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC}$ - 0.5V.

Symbol	Parameter	80C186		80C186-12		80C186-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C186 GENERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{DVCL}	Data in Setup (A/D)	15		15		15		ns	
TCLDX	Data in Hold (A/D)	3		3		3		ns	
80C186 GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	5	45	5	35	5	31	ns	
T_{CLSH}	Status Inactive Delay	5	46	5	35	5	30	ns	
T_{CLAV}	Address Valid Delay	5	44	5	36	5	33	ns	
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	5	40	5	36	5	33	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		30		25		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		T_{CLCL} - 15		T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 18		T_{CLCH} - 15		T_{CLCH} - 15		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	T_{CHCL} - 15		T_{CHCL} - 15		T_{CHCL} - 15		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	T_{CLAX}	20	ns	
T_{CVCTV}	Control Active Delay 1	3	44	3	37	3	31	ns	
T_{CVCTX}	Control Inactive Delay	3	44	3	37	3	31	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	5	44	5	37	5	31	ns	
T_{CVDEX}	$\overline{DEN}$ Inctive Delay (Non-Write Cycles)	5	44	5	37	5	31	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	3	35	ns	

270354-38

A. C. CHARACTERISTICS

INTERRUPT ACKNOWLEDGE CYCLE WAVEFORMS



NOTES:

1. Status inactive in state preceding T_4.
2. The data hold time lasts only until $\overline{INTA}$ goes inactive, even if the $\overline{INTA}$ transition occurs prior to T_{CLDX} (min).
3. $\overline{INTA}$ occurs one clock later in Slave Mode.
4. For write cycle followed by interrupt acknowledge cycle.
5. $\overline{LOCK}$ is active upon T_1 of the first interrupt acknowledge cycle and inactive upon T_2 of the second interrupt acknowledge cycle.

270354-39

24

A. C. CHARACTERISTICS

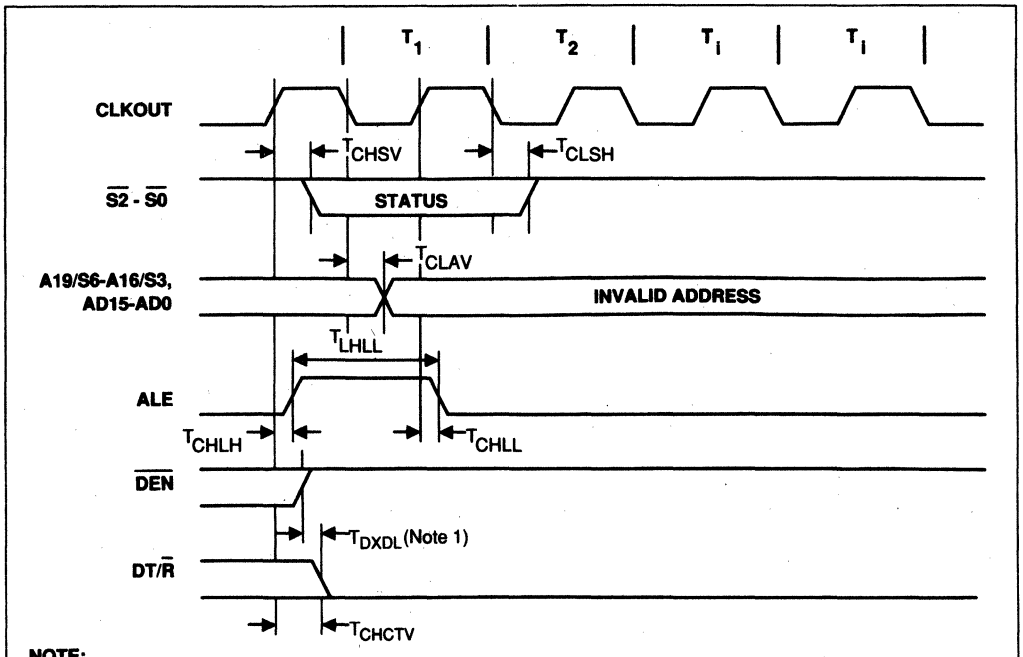
SOFTWARE HALT CYCLE TIMINGS

$T_A = 0^\circ C$ to $+70^\circ C$, V_{CC} = 5V ± 10% except V_{CC} = 5V ± 5% at f > 12.5 MHz

All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	80C186		80C186-12		80C186-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C186 GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	5	45	5	35	5	31	ns	
T_{CLSH}	Status Inactive Delay	5	46	5	35	5	30	ns	
T_{CLAV}	Address Valid Delay	5	44	5	36	5	33	ns	
T_{CHLH}	ALE Active Delay		30		25		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		T_{CLCL} - 15		T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25		20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low		0		0		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	5	44	5	37	5	31	ns	

SOFTWARE HALT CYCLE WAVEFORMS



NOTE:
1. For write cycle followed by halt cycle.

270354-40

A. C. CHARACTERISTICS

CLOCK TIMINGS

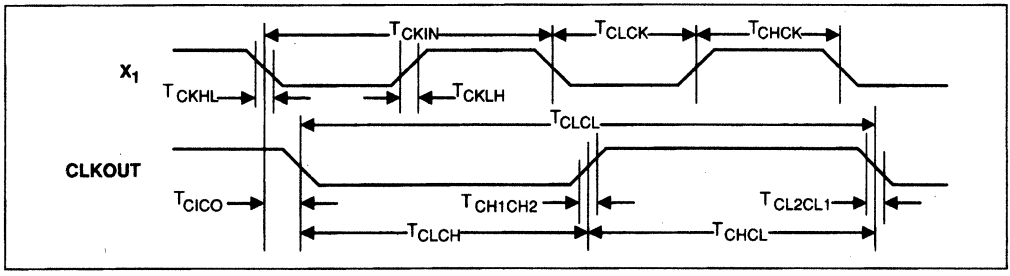
$T_A = 0^\circ C$ to $+70^\circ C$, V_{CC} = 5V ± 10% except V_{CC} = 5V± 5% at f > 12.5 MHz

All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC}$ - 0.5V.

Symbol	Parameter	80C186		80C186-12		80C186-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C186 CLKIN REQUIREMENTS Measurements taken with following conditions: External clock input to X1 and X2 not connected (float)									
T_{CKIN}	CLKIN Period	50	1000	40	1000	31.25	1000	ns	
T_{CLCK}	CLKIN Low Time	20		16		13		ns	1.5 V(2)
T_{CHCK}	CLKIN High Time	20		16		13		ns	1.5 V(2)
T_{CKHL}	CLKIN Fall Time		5		5		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5		5		5	ns	1.0 to 3.5V
80C186 CLKOUT TIMING									
T_{CICO}	CLKIN to CLKOUT Skew		25		21		17	ns	
T_{CLCL}	CLKOUT Period	100	2000	80	2000	62.5	2000	ns	
T_{CLCH}	CLKOUT Low Time	0.5 T_{CLCL} -8		0.5 T_{CLCL} -7		0.5 T_{CLCL} -7		ns	C_L=100pF(2)
		0.5 T_{CLCL} -6		0.5 T_{CLCL} -5		0.5 T_{CLCL} -5		ns	C_L=50pF(3)
T_{CHCL}	CLKOUT High Time	0.5 T_{CLCL} -8		0.5 T_{CLCL} -7		0.5 T_{CLCL} -7		ns	C_L=100pF(4)
		0.5 T_{CLCL} -6		0.5 T_{CLCL} -5		0.5 T_{CLCL} -5		ns	C_L=50pF(3)
T_{CH1CH2}	CLKOUT Rise Time		10		10		10	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		10		10		10	ns	3.5 to 1.0V

NOTES:
1. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}
2. Tested under worst case conditions: V_{CC} = 5.5V (5.25V @ 16 MHz). $T_A = 70^\circ C$.
3. Not Tested.
4. Tested under worst case conditions: V_{CC} = 4.5V (4.75V @ 16 MHz). $T_A = 0^\circ C$.

CLOCK WAVEFORMS



270354-41

A. C. CHARACTERISTICS

READY, PERIPHERAL, AND QUEUE STATUS TIMINGS

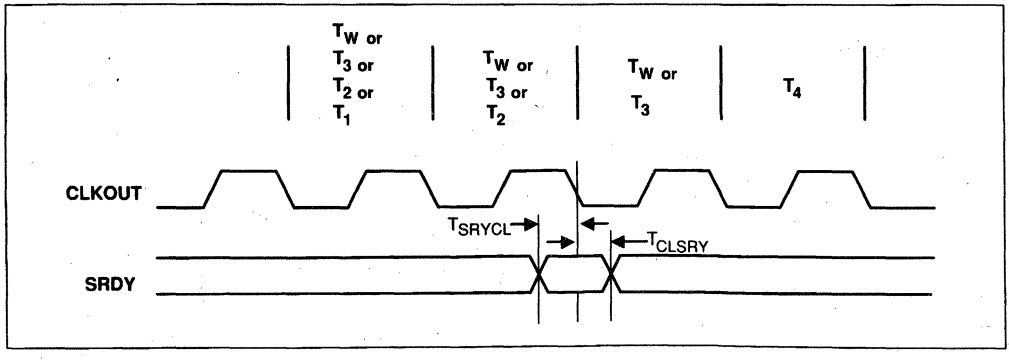
$T_A = 0^\circ C$ to $+70^\circ C$, V_{CC} = 5V ± 10% except V_{CC} = 5V± 5% at f > 12.5 MHz

All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH}= 2.4V except at X1 where $V_{IH} = V_{CC}$- 0.5V.

Symbol	Parameter	80C186		80C186-12		80C186-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C186 READY AND PERIPHERAL TIMING REQUIREMENTS									
T_{SRYCL}	Synchronous Ready(SRDY) Transition Setup Time (1)	15		15		15		ns	
T_{CLSRY}	SRDY Transition Hold Time (1)	15		15		15		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time (2)	15		15		15		ns	
T_{CLARX}	ARDY Active Hold Time (1)	15		15		15		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	15		15		15		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time (1)	25		25		25		ns	
T_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time (2)	15		15		15		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time (2)	15		15		15		ns	
80C186 PERIPHERAL AND QUEUE STATUS TIMING RESPONSES									
T_{CLTMV}	Timer Output Delay		40		33		27	ns	
T_{CHQSV}	Queue Status Delay		37		32		30	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

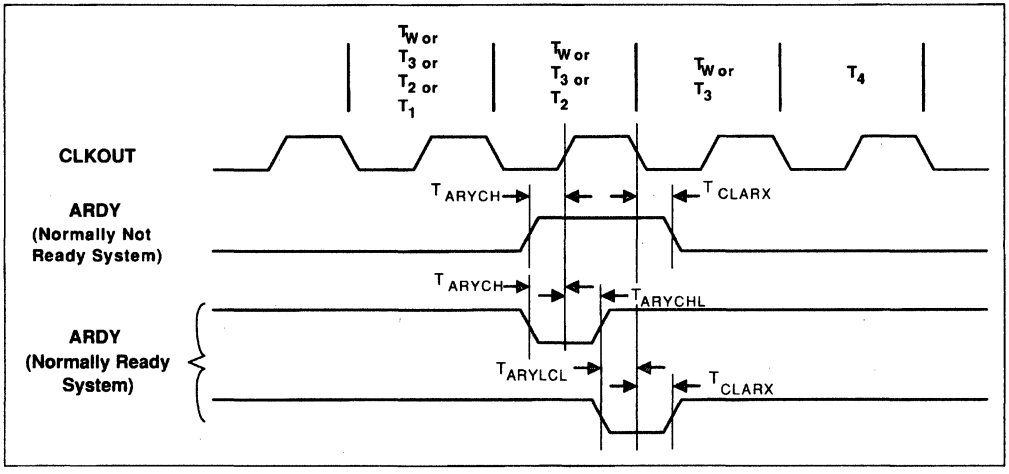
SYNCHRONOUS READY (SRDY) WAVEFORMS



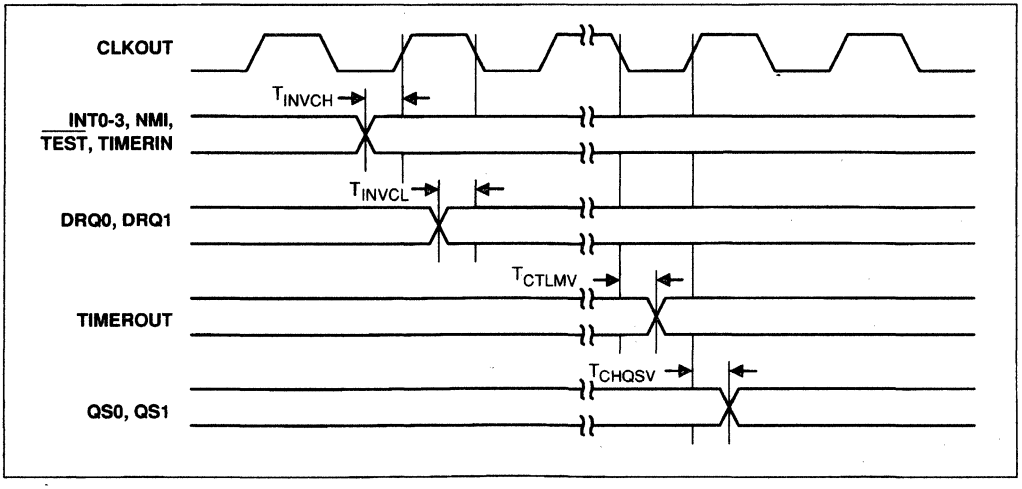
270354-42

A. C. CHARACTERISTICS

ASYNCHRONOUS READY (ARDY) WAVEFORMS



PERIPHERAL AND QUEUE STATUS WAVEFORMS



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A. C. CHARACTERISTICS

RESET AND HOLD/HLDA TIMINGS

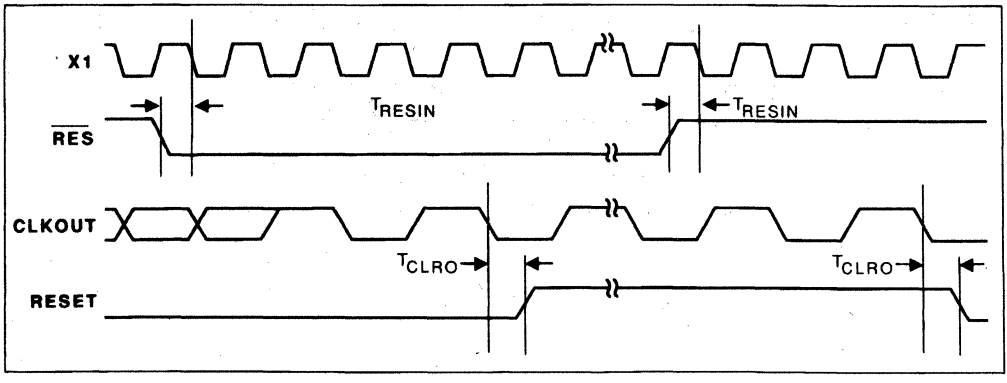
$T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5V \pm 10\%$ except $V_{CC} = 5V \pm 5\%$ at $f > 12.5$ MHz

All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	80C186		80C186-12		80C186-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C186 RESET AND HOLD/HLDA TIMING REQUIREMENTS									
T_{RESIN}	$\overline{RES}$ Setup	15		15		15		ns	
T_{HVCL}	HOLD Setup (1)	15		15		15		ns	
80C186 GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	T_{CLAX}	20	ns	
T_{CLAV}	Address Valid Delay	5	44	5	36	5	33	ns	
80C186 RESET AND HOLD/HLDA TIMING RESPONSES									
T_{CLRO}	Reset Delay		40		33		27	ns	
T_{CLHAV}	HLDA Valid Delay	3	40	3	33	3	25	ns	
T_{CHCZ}	Command Lines Float Delay		40		33		28	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		44		36		32	ns	

NOTE:
1. To guarantee recognition at next clock.

RESET WAVEFORMS



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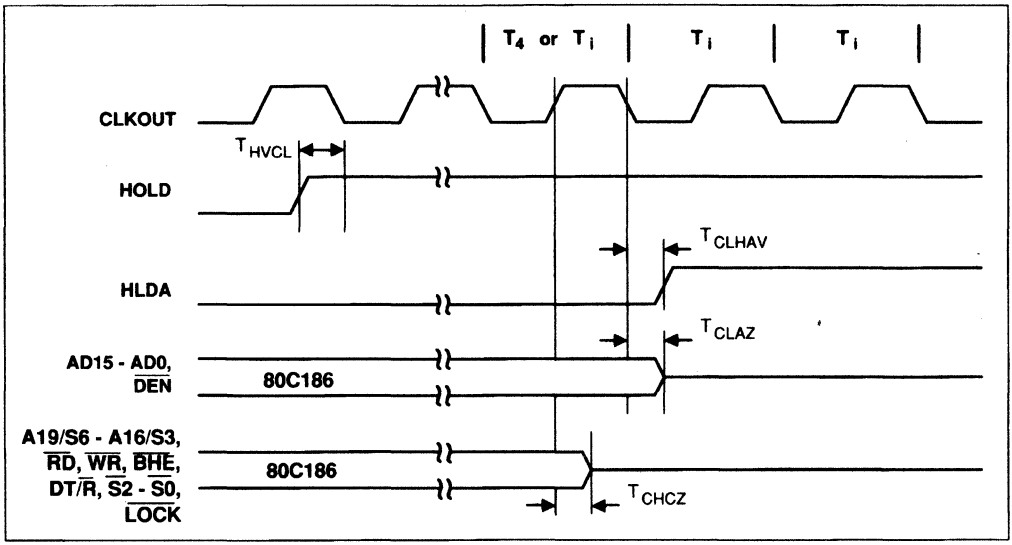
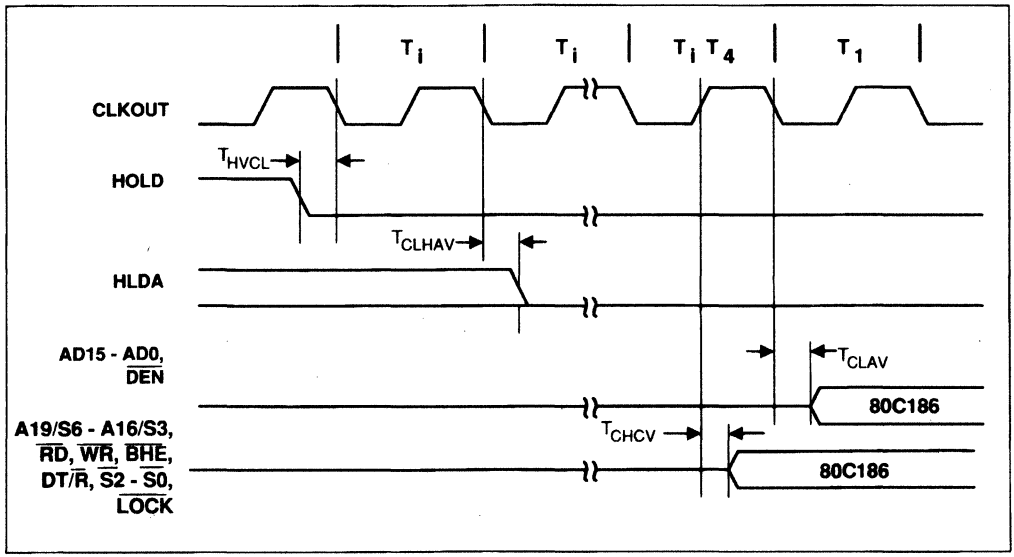
A. C. CHARACTERISTICS

HOLD/HLDA WAVEFORMS (Entering Hold)



HOLD/HLDA WAVEFORMS (Leaving Hold)



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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has from 5 to 7 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
ARY: Asynchronous Ready Input
C: Clock Output
CK: Clock Input
CS: Chip Select
CT: Control (DT/$\overline{R}$, $\overline{DEN}$, . . .)
D: Data Input
DE: $\overline{DEN}$
H: Logic Level High
IN: Input (DRQ0, TIM0, . . .)
L: Logic Level Low or ALE
O: Output
QS: Queue Status (QS1, QS2)
R: $\overline{RD}$ Signal, RESET Signal
S: Status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$)
SRY: Synchronous Ready Input
V: Valid
W: WR Signal
X: No Longer a Valid Logic Level
Z: Float

Examples:

T_{CLAV} — Time from Clock low to Address valid
T_{CHLH} — Time from Clock high to ALE high
T_{CLCSV} — Time from Clock low to Chip Select valid

WAVEFORMS

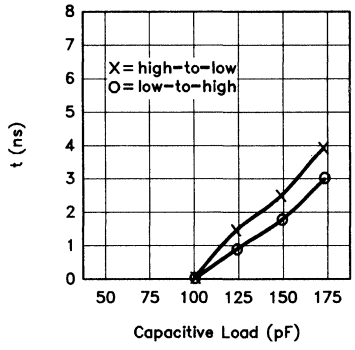

Figure 47. Capacitive Derating Curve

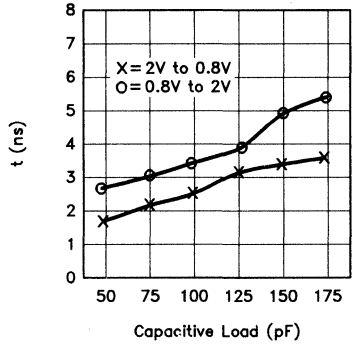

Figure 48. TTL Level Rise and Fall Times for Output Buffers

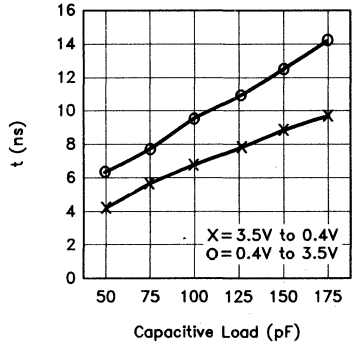

Figure 49. CMOS Level Rise and Fall Times for Output Buffers

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80C186 EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the 80C186 microprocessor. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The 80C186 EXPRESS program includes an extended temperature range. With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

Package types and EXPRESS versions are identified by a one or two-letter prefix to the part number. The prefixes are listed in Table 18. All AC and DC specifications not mentioned in this section are the same for both commercial and EXPRESS parts.

Table 18. Prefix Identification

Prefix	Package Type	Temperature Range
A	PGA	Commercial
N	PLCC	Commercial
R	LCC	Commercial
TA	PGA	Extended
TN	PLCC	Extended
TR	LCC	Extended

NOTE:
Extended temperature versions of the 80C186 are not available at 16 MHz.

80C186 EXECUTION TIMINGS

A determination of 80C186 program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the 80C186 has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1000100w	mod reg r/m			2/12	
Register/memory to register	1000101w	mod reg r/m			2/9	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12–13	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3–4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8	
Accumulator to memory	1010001w	addr-low	addr-high		9	
Register/memory to segment register	10001110	mod 0 reg r/m			2/9	
Segment register to register/memory	10001100	mod 0 reg r/m			2/11	
PUSH = Push:						
Memory	11111111	mod 1 1 0 r/m			16	
Register	01010 reg				10	
Segment register	000reg110				9	
Immediate	011010s0	data	data if s=0		10	
PUSHA = Push All	01100000				36	
POP = Pop:						
Memory	10001111	mod 0 0 0 r/m			20	
Register	01011 reg				10	
Segment register	000reg111	(reg≠01)			8	
POPA = Pop All	01100001				51	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10	
Variable port	1110110w				8	
OUT = Output to:						
Fixed port	1110011w	port			9	
Variable port	1110111w				7	
XLAT = Translate byte to AL	11010111				11	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		18	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		18	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				9	
POPF = Pop flags	10011101				8	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if sw=01	4/16	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	4/16	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	4/16	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if sw=01	4/16	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10	
Register with register/memory	0011100w	mod reg r/m			3/10	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	3/10	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26–28	
Register-Word					35–37	
Memory-Byte					32–34	
Memory-Word					41–43	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
ARITHMETIC (Continued)						
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w	mod 1 0 1 r/m				
Register-Byte					25–28	
Register-Word					34–37	
Memory-Byte					31–34	
Memory-Word					40–43	
IMUL = Integer immediate multiply (signed)	0 1 1 0 1 0 s 1	mod reg r/m	data	data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w	mod 1 1 0 r/m				
Register-Byte					29	
Register-Word					38	
Memory-Byte					35	
Memory-Word					44	
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w	mod 1 1 1 r/m				
Register-Byte					44–52	
Register-Word					53–61	
Memory-Byte					50–58	
Memory-Word					59–67	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0			19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0			15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0				2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1				4	
LOGIC						
Shift/Rotate Instructions:						
Register/Memory by 1	1 1 0 1 0 0 0 w	mod TTT r/m			2/15	
Register/Memory by CL	1 1 0 1 0 0 1 w	mod TTT r/m			5+n/17+n	
Register/Memory by Count	1 1 0 0 0 0 0 w	mod TTT r/m	count		5+n/17+n	
	TTT Instruction 0 0 0 ROL 0 0 1 ROR 0 1 0 RCL 0 1 1 RCR 1 0 0 SHL/SAL 1 0 1 SHR 1 1 1 SAR					
AND = **And:**						
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1	4/16	
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1		3/4	8/16-bit
TEST = **And function to flags, no result:**						
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m			3/10	
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1	4/10	
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1		3/4	8/16-bit
OR = **Or:**						
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1	4/16	
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1		3/4	8/16-bit

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
XOR = **Exclusive or:**						
Reg/memory and register to either	0 0 1 1 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1	4/16	
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1		3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w	mod 0 1 0 r/m			3/10	
STRING MANIPULATION						
MOVS = Move byte/word	1 0 1 0 0 1 0 w				14	
CMPS = Compare byte/word	1 0 1 0 0 1 1 w				22	
SCAS = Scan byte/word	1 0 1 0 1 1 1 w				15	
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w				12	
STOS = Store byte/wd from AL/AX	1 0 1 0 1 0 1 w				10	
INS = Input byte/wd from DX port	0 1 1 0 1 1 0 w				14	
OUTS = Output byte/wd to DX port	0 1 1 0 1 1 1 w				14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	1 1 1 1 0 0 1 0	1 0 1 0 0 1 0 w			8+8n	
CMPS = Compare string	1 1 1 1 0 0 1 z	1 0 1 0 0 1 1 w			5+22n	
SCAS = Scan string	1 1 1 1 0 0 1 z	1 0 1 0 1 1 1 w			5+15n	
LODS = Load string	1 1 1 1 0 0 1 0	1 0 1 0 1 1 0 w			6+11n	
STOS = Store string	1 1 1 1 0 0 1 0	1 0 1 0 1 0 1 w			6+9n	
INS = Input string	1 1 1 1 0 0 1 0	0 1 1 0 1 1 0 w			8+8n	
OUTS = Output string	1 1 1 1 0 0 1 0	0 1 1 0 1 1 1 w			8+8n	
CONTROL TRANSFER						
CALL = **Call:**						
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high		15	
Register/memory indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m			13/19	
Direct intersegment	1 0 0 1 1 0 1 0	segment offset			23	
		segment selector				
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m	(mod ≠ 11)		38	
JMP = **Unconditional jump:**						
Short/long	1 1 1 0 1 0 1 1	disp-low			14	
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high		14	
Register/memory indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m			11/17	
Direct intersegment	1 1 1 0 1 0 1 0	segment offset			14	
		segment selector				
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	(mod ≠ 11)		26	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
RET = **Return from CALL:**						
Within segment	11000011				16	
Within seg adding immed to SP	11000010	data-low	data-high		18	
Intersegment	11001011				22	
Intersegment adding immediate to SP	11001010	data-low	data-high		25	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110 000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22+16(n−1)	
LEAVE = Leave Procedure	11001001				8	
INT = **Interrupt:**						
Type specified	11001101	type			47	
Type 3	11001100				45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110				48/4	
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33–35	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	
	(TTT LLL are opcode to processor extension)		

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

REVISION HISTORY

The sections significantly revised since version -004 are:

Pin Description Table	Added note to $\overline{TEST}$/BUSY pin requiring proper RESET at power-up to configure pin as input. Renamed pin 44 to INT1/$\overline{SELECT}$ and pin 41 to INT3/$\overline{INTA1}$/IRQ to better describe their functions in Slave Mode.
Initialization and Processor Reset	Added reminder to drive $\overline{RES}$ pin LOW during power-up.
Read and Write Cycle Waveforms	Clarified applicability of T_{CLCSV} to latched A1 and A2 in footnotes.
Slave Mode Operation	The three low order bits associated with vector generation and performing EOI are not alterable; however, the priority levels are programmable. This information is a clarification only.

The sections significantly revised since version -003 are:

Front Page	Deleted references to burn-in devices.
Local Bus Controller and Reset	Clarified effects of excessive loading on pins with internal pullup devices. Equivalent resistance no longer shown.
D.C. Characteristics	Renamed V_{CLI} to V_{IL1}. Renamed V_{CHI} to V_{IH3}. Changed V_{OH} (min.) from 0.8 V_{CC} to V_{CC} − 0.5V. Changed I_{CC} (max.) from 180 mA to 150 mA at 16 MHz, 150 mA to 120 mA at 12.5 mA, and 100 mA to 120 mA at 10 MHz. Changed V_{CLO} (max.) from 0.5V to 0.45V. Changed V_{CHO} (min.) from 0.8 V_{CC} to V_{CC} − 0.5V. Clarified effect of excessive loading on pins with internal pullup devices.
Power Supply Current	Added equation and graph for maximum current.
A.C. Characteristics	Many timings changed (all listed in ns): T_{DVCL} (min.) at 16 MHz from 10 to 15; T_{CLDX} (min.) from 5 to 3; T_{CLAV} (max.) at 10 MHz from 50 to 44; T_{CHCV} (max.) from 45 to 44 at 10 MHz, and from 37 to 36 at 12.5 MHz; T_{LHLL} (min.) from T_{CLCL} − 30 to T_{CLCL} − 15; T_{LLAX} (min.) at 10 MHz from T_{CHCL} − 20 to T_{CHCL} − 15; T_{CVCTV} (max.) from 56 to 44 at 10 MHz and from 47 to 37 at 12.5 MHz; T_{CVDEX} (max.) from 56 to 44 at 10 MHz, 47 to 37 at 12.5 MHz, and from 35 to 31 at 16 MHz; T_{RHAV} (min.) from T_{CLCL} − 40 at 10 MHz and T_{CLCL} − 20 at 12.5 MHz and 16 MHz to T_{CLCL} − 15 at all frequencies; T_{RLRH} (min.) from 2 T_{CLCL} − 46 to 2 T_{CLCL} − 30 at 10 MHz, from 2 T_{CLCL} − 40 to 2 T_{CLCL} − 25 at 12.5 MHz, and 2 T_{CLCL} − 30 to 2 T_{CLCL} − 25 at 16 MHz; T_{WLWH} (min.) from 2 T_{CLCL} − 34 to 2 T_{CLCL} − 30 at 10 MHz, and 2 T_{CLCL} − 30 to 2 T_{CLCL} − 25 at 12.5 MHz; T_{AVLL} (min.) from T_{CLCH} − 19 to T_{CLCH} − 18 at 10 MHz; T_{CLSH} (max.) at 10 MHz from 50 to 46; T_{CLTMV} (max.) from 48 to 40 at 10 MHz, 40 to 33 at 12.5 MHz, and 30 to 27 at 16 MHz; T_{CLRO} (max.) from 48 to 40 at 10 MHz, 40 to 33 at 12.5 MHz, and 30 to 27 at 16 MHz; T_{CHQSV} (max.) from 28 to 37 at 10 MHz, 28 to 32 at 12.5 MHz, and 25 to 30 at 16 MHz; T_{CHDX} (min.) from 5 to 10; T_{CLLV} (max.) at 10 MHz from 45 to 40 and at 12.5 MHz from 40 to 37; T_{CLCSV} (max.) from 45 to 42 at 10 MHz; T_{CHCSX} (max.) from 32 to 35 at 10 MHz, 28 to 30 at 12.5 MHz, and 23 to 25 at 16 MHz; and T_{CH1CH2} and T_{CL2CL1} (max.) at 16 MHz from 8 to 10. Added new timings for T_{WHDEX}, T_{RHLH}, and T_{WHLH}. Established min. timing for T_{CLCSV}.
Timing Waveforms	Section rearranged to show waveforms on same or facing page relative to corresponding tabular data. T_{CLSRY} drawn to same clock edge as T_{SRYCL}. Drawing changed to indicate one less clock between HOLD inactive and HLDA inactive.
Specification Level Markings	New Section.

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The sections significantly revised since version -002 are:

Block Diagram	Redrawn to illustrate numerics coprocessor interface.
Pin Description Table	Various descriptions rewritten for clarity.
Interrupt Vector Table	Redrawn for clarity. Interrupt Type 16 listed.
ESC Opcode Exception Description	Note added concerning ESC trap.
Oscillator Configurations	Deleted drive of X2 with inverted X1.
RESET Logic	Deleted paragraph concerning setup times for synchronization of multiple processors.
Local Bus Arbitration	Added description of HLDA when a refresh cycle is pending.
Local Bus Controller and Reset	Added description of pullup devices for appropriate pins.
DMA Controller	Added reminder to initialize transfer count registers and pointer registers.
Timers	Added reminder to intialize count registers.
DRAM Refresh Addresses	Refresh address counter described in figure.
D.C. Characteristics	V_{IH2} indicated for SRDY, ARDY. I_{CC} (max.) now indicated for all devices.
Power Supply Current	Typical I_{CC} indicated.
A.C. Characteristics	Input V_{IH} test condition at X1 added. T_{CLDOX}, T_{CVCTV}, T_{CVCTX}, T_{CLHAV}, and T_{CLLV} minimums reduced from 5 ns to 3 ns. T_{CLCH} (min.) and T_{CHCL} (min.) relaxed by 2 ns. Added reminder that T_{SRYCL} and T_{CLSRY} must be met.
Explanation of the A.C. Symbols	New Section.
Major Cycle Timing Waveforms	T_{DXDL} indicated in Read Cycle. T_{CLRO} indicated.
Rise/Fall and Capacitive Derating Curves	New Figures added.
Instruction Set Summary	ESC instruction clock count deleted.

The sections significantly revised since version -001 are:

Pin Description Table	Noted $\overline{RES}$ to be low more than 4 clocks.
Oscillator Configurations	Added reminder not to drive X2.
DMA Transfer Rate Table	Corrected to reflect 16 MHz capability.
DMA Control Bit Descriptions	Moved and clarified note concerning TC condition for ST/$\overline{STOP}$ clearing during unsynchronized transfers.
Interrupt Controller, etc.	Renamed iRMX Mode to Slave Mode.
Interrupt Request Register	Noted that D0 and D1 are read/write, others read-only.
DRAM Refresh Addresses	Added figure to explain refresh address bits.
A.C. Characteristics	Many timings changed (all listed in ns): T_{CLDX} (min.) from 8 to 5; T_{SRYCL} (min.) from 20 to 15; T_{HVCL} (min.) from 20 to 15; T_{INVCH} (min.) from 25 to 15; T_{INVCL} (min.) from 20 to 15; T_{CLAV} at 12.5 MHz from 4–33 to 5–36; T_{CLAV} at 16 MHz from 4–30 to 5–33; T_{CLAX} (min.) to 0; T_{CLDV} (min.) at 10 MHz from 10 to 5; T_{CLDV} (min.) at 12.5 MHz from 10–33 to 5–36; T_{CLDV} (min.) at 16 MHz from 10–30 to 5–33; T_{CLDOX} (min.) from 10 at 10 MHz and 8 at 12.5 MHz to 5 at both frequencies; T_{CVCTV} (max.) and T_{CHCTV} (max.) at 16 MHz from 25 to 31; T_{CHCTV} (min.) and T_{CVDEX} (min.) both from 10 at 10 MHz and 8 at 12.5 MHz to 5 at both frequencies; T_{CVCTX} (max.) at 16 MHz from 25 to 33; T_{CLRL} at 10 MHz from 10–56 to 5–44; T_{CLRL} at 12.5 MHz from 8–47 to 5–35; T_{CLRL} (max.) at 16 MHz from 25 to 31; T_{CLRH} (min.) at 10 MHz from 10 to 5 and at 12.5 MHz from 8 to 5; T_{CHSV} (min.) at 10 MHz from 10 to 5 and at 12.5 MHz from 8 to 5; T_{CHSV} (max.) at 16 MHz from 25 to 31; T_{CLSH} (min.) at 10 MHz from 10 to 5 and at 12.5 MHz from 8 to 5; T_{CHQSV} (max.) at 12.5 MHz from 23 to 28 and at 16 MHz from 23 to 25; T_{CHDX} (min.) at 10 MHz from 10 to 5 and at 12.5 MHz from 8 to 5; T_{AVCH} (min.) to 0; T_{CLLV} (max.) at 10 MHz from 60 to 45 and at 12.5 MHz from 55 to 40 and at 16 MHz from 40 to 35; T_{DXDL} (min.) to 0; T_{CXCSX} (min.) from 35 at 10 MHz and 29 at 12.5 MHz and 25 at 16 MHz to $T_{CLCH} - 10$ at all frequencies; T_{CHCSX} (min.) at 12.5 MHz and 16 MHz from 4–23 to 5–28 and 5–23 respectively.
Execution Timings	Clarified effect of bus width.

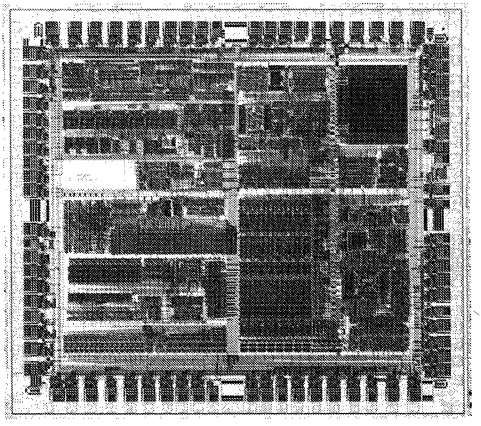
SPECIFICATION LEVEL MARKINGS

Current 80C186 devices bear backside lot code information consisting of seven digits followed by letters. The second, third, and fourth digits comprise a manufacturing date code. This preliminary data sheet applies only to 80C186 devices with a date code corresponding to week 25 of 1989 (backside markings x925xxx XXX) or later.

80C186XL20, 16, 12, 10
16-BIT HIGH INTEGRATION EMBEDDED PROCESSOR

- Low Power, Full Static Version of 80C186
- Operation Modes:
  - Enhanced Mode
    - DRAM Refresh Control Unit
    - Power-Save Mode
    - Direct Interface to 80C187
  - Compatible Mode
    - NMOS 80186 Pin-for-Pin Replacement for Non-Numerics Applications
- Integrated Feature Set
  - Static, Modular CPU
  - Clock Generator
  - 2 Independent DMA Channels
  - Programmable Interrupt Controller
  - 3 Programmable 16-Bit Timers
  - Dynamic RAM Refresh Control Unit
  - Programmable Memory and Peripheral Chip Select Logic
  - Programmable Wait State Generator
  - Local Bus Controller
  - Power-Save Mode
  - System-Level Testing Support (High Impedance Test Mode)
- Completely Object Code Compatible with Existing 8086/8088 Software and Has 10 Additional Instructions over 8086/8088
- Speed Versions Available
  - 20 MHz (80C186XL20)
  - 16 MHz (80C186XL16)
  - 12.5 MHz (80C186XL12)
  - 10 MHz (80C186XL)
- Direct Addressing Capability to 1 MByte Memory and 64 Kbyte I/O
- Complete System Development Support
  - All 8086 and 80C186 Software Development Tools Can Be Used for 80C186XL System Development
    - ASM 86 Assembler, PL/M-86, Pascal-86, Fortran-86, iC-86 and System Utilities
    - In-Circuit-Emulator (ICE™-186)
- Available in 68-Pin:
  - Plastic Leaded Chip Carrier (PLCC)
  - Ceramic Pin Grid Array (PGA)
  - Ceramic Leadless Chip Carrier (JEDEC A Package)
- Available in 80-Pin Quad Flat Pack (EIAJ)
- Available in EXPRESS Extended Temperature Range (−40°C to +85°C)

The Intel 80C186XL is a Modular Core re-implementation of the 80C186 Microprocessor. It offers higher speed and lower power consumption than the standard 80C186 but maintains 100% clock-for-clock functional compatibility. Packaging and pinout are also identical.



272032-42

May 1992
Order Number: 272032-002

80C186XL20, 16, 12, 10
16-BIT HIGH INTEGRATION EMBEDDED PROCESSOR

CONTENTS

CONTENTS

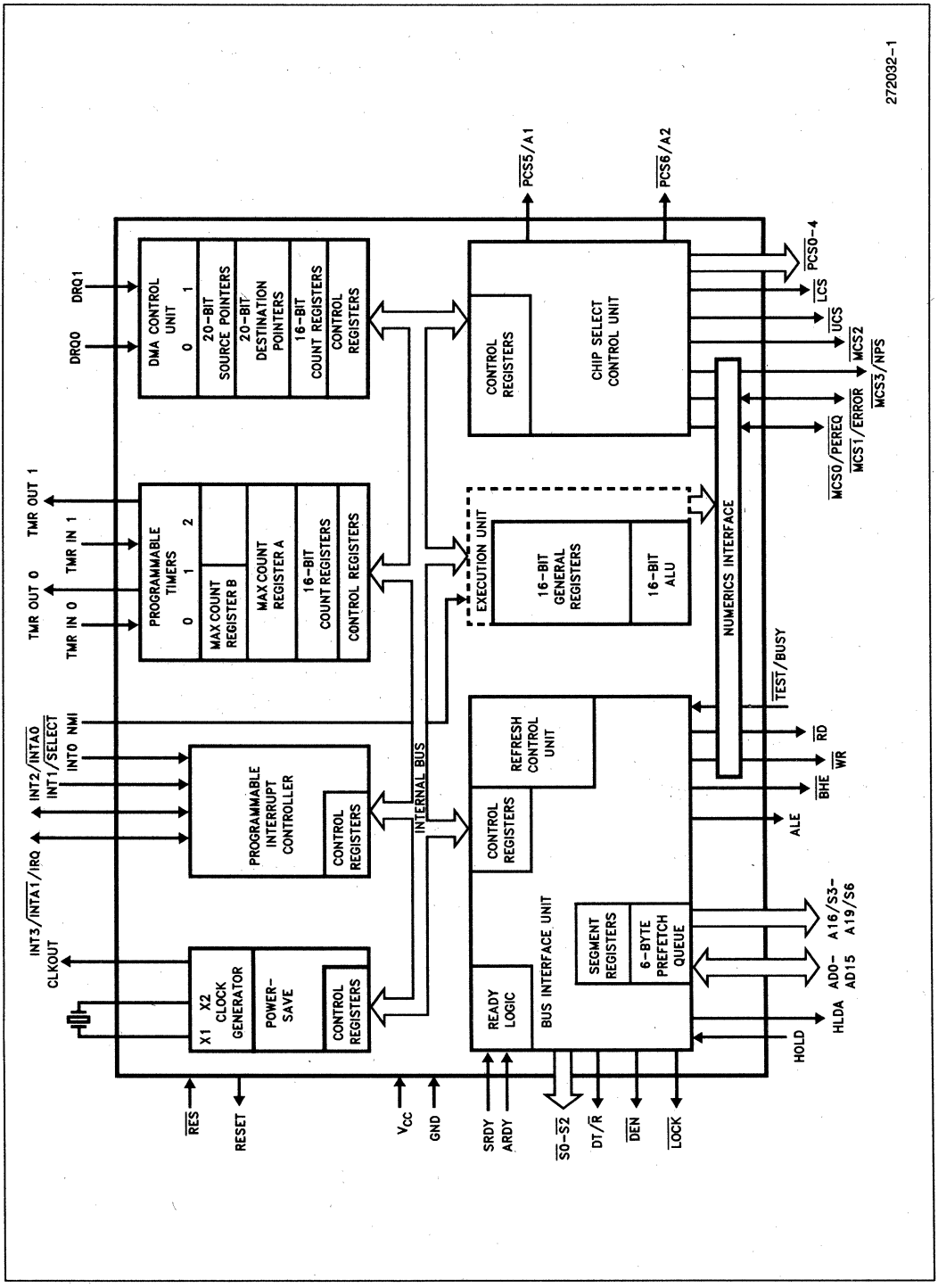
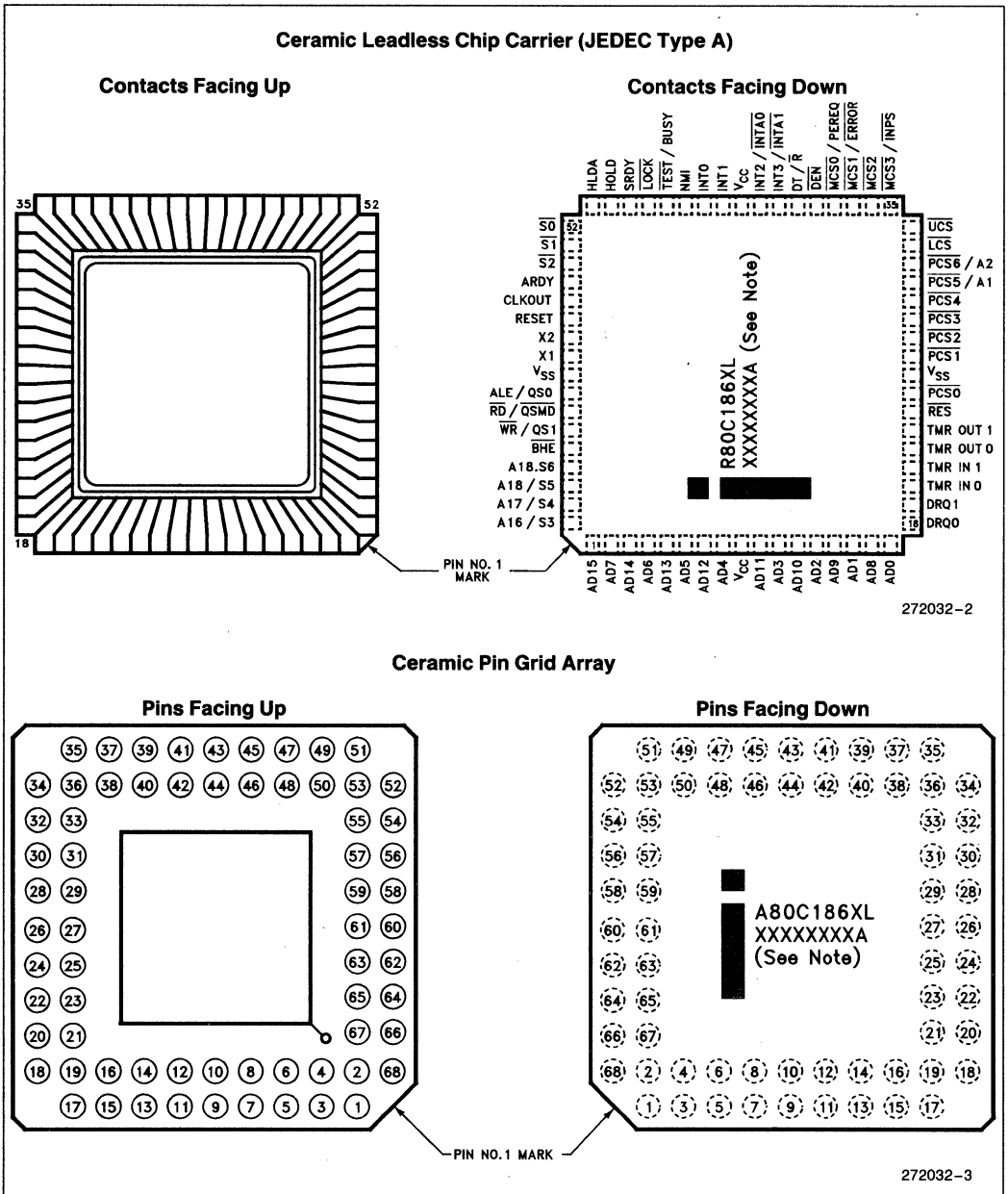


Figure 1. 80C186XL Block Diagram



NOTE:
XXXXXXXXA indicates the Intel FPO number.

Figure 2. 80C186XL Pinout Diagrams

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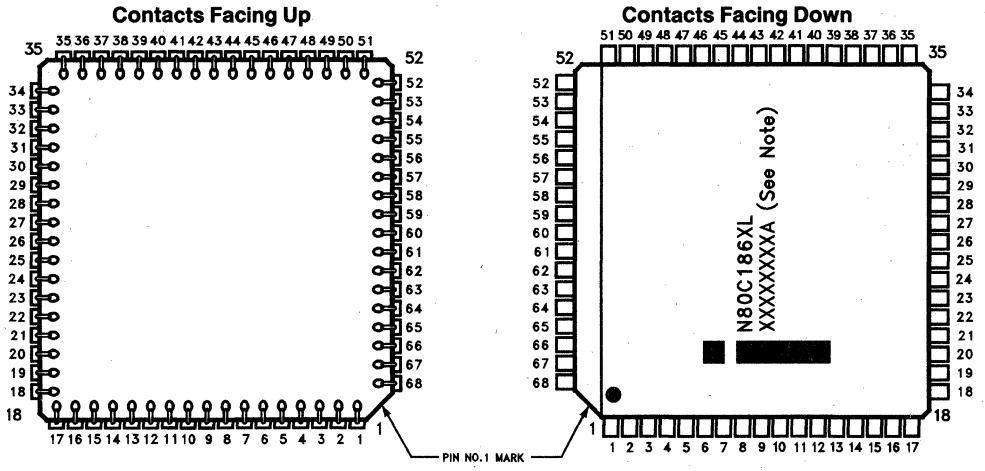
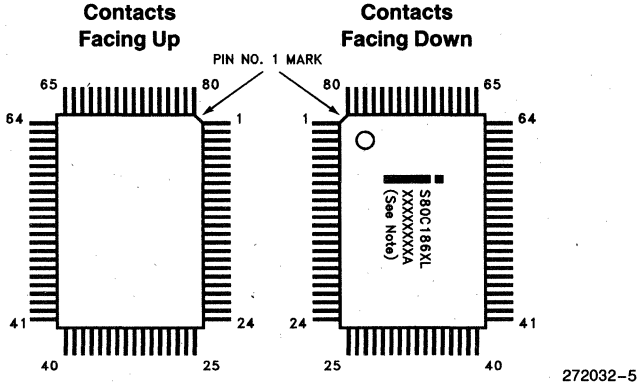
Plastic Leaded Chip Carrier



272032-4

80-Pin Quad Flat Pack (EIAJ)



272032-5

NOTE:
XXXXXXXXA indicates the Intel FPO number.

Figure 2. 80C186XL Pinout Diagrams (Continued)

Table 1. 80C186XL Pin Description

Symbol	LCC PGA PLCC Pin No.	QFP Pin No.	Type	Name and Function
V_{CC}	9 43	33, 34, 72, 73	I I	System Power: +5 volt power supply.
V_{SS}	26 60	12, 13, 53	I I	System Ground.
RESET	57	18	O	RESET Output indicates that the 80C186XL CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal. Reset goes inactive 2 clockout periods after $\overline{RES}$ goes inactive. When tied to the $\overline{TEST}$/BUSY pin, RESET forces the 80C186XL into enhanced mode. RESET is not floated during bus hold.
X1 X2	59 58	16 17	I O	Crystal Inputs X1 and X2 provide external connections for a fundamental mode or third overtone parallel resonant crystal for the internal oscillator. X1 can connect to an external clock instead of a crystal. In this case, minimize the capacitance on X2. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	19	O	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT is active during reset and bus hold.
$\overline{RES}$	24	55	I	An active $\overline{RES}$ causes the 80C186XL to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80C186XL clock. The 80C186XL begins fetching instructions approximately 6½ clock cycles after $\overline{RES}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{RES}$ held LOW. $\overline{RES}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network.
$\overline{TEST}$/BUSY	47	29	I/O	The $\overline{TEST}$ pin is sampled during and after reset to determine whether the 80C186XL is to enter Compatible or Enhanced Mode. Enhanced Mode requires $\overline{TEST}$ to be HIGH on the rising edge of $\overline{RES}$ and LOW four CLKOUT cycles later. Any other combination will place the 80C186XL in Compatible Mode. During power-up, active $\overline{RES}$ is required to configure $\overline{TEST}$/BUSY as an input. A weak internal pullup ensures a HIGH state when the input is not externally driven. $\overline{TEST}$—In Compatible Mode this pin is configured to operate as $\overline{TEST}$. This pin is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when WAIT execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled every five clocks until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80C186XL is waiting for $\overline{TEST}$, interrupts will be serviced. BUSY—In Enhanced Mode, this pin is configured to operate as BUSY. The BUSY input is used to notify the 80C186XL of Math Coprocessor activity. Floating point instructions executing in the 80C186XL sample the BUSY pin to determine when the Math Coprocessor is ready to accept a new command. BUSY is active HIGH.

Table 1. 80C186XL Pin Description (Continued)

Symbol	LCC PGA PLCC Pin No.	QFP Pin No.	Type	Name and Function
TMR IN 0 TMR IN 1	20 21	59 58	I I	Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized. Timer Inputs must be tied HIGH when not being used as clock or retrigger inputs.
TMR OUT 0 TMR OUT 1	22 23	57 56	O O	Timer outputs are used to provide single pulse or continous waveform generation, depending upon the timer mode selected. These outputs are not floated during a bus hold.
DRQ0 DRQ1	18 19	61 60	I I	DMA Request is asserted HIGH by an external device when it is ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
NMI	46	30	I	The Non-Maskable Interrupt input causes a Type 2 interrupt. An NMI transition from LOW to HIGH is latched and synchronized internally, and initiates the interrupt at the next instruction boundary. NMI must be asserted for at least one CLKOUT period. The Non-Maskable Interrupt cannot be avoided by programming.
INT0 INT1/$\overline{\text{SELECT}}$ INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$/IRQ	45 44 42 41	31 32 35 36	I I I/O I/O	Maskable Interrupt Requests can be requested by activating one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When Slave Mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).
A19/S6 A18/S5 A17/S4 A16/S3	65 66 67 68	6 5 4 3	O O O O	Address Bus Outputs (16–19) and Bus Cycle Status (3–6) indicate the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W and T_4, the S6 pin is LOW to indicate a CPU-initiated bus cycle or HIGH to indicate a DMA-initiated or refresh bus cycle. During the same T-states, S3, S4 and S5 are always LOW. These outputs are floated during bus hold or reset.
AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	1 3 5 7 10 12 14 16 2 4 6 8 11 13 15 17	1 79 77 75 71 69 67 65 80 78 76 74 70 68 66 64	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	Address/Data Bus (0–15) signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W and T_4) bus. The bus is active HIGH. A_0 is analogous to $\overline{\text{BHE}}$ for the lower byte of the data bus, pins D_7 through D_0. It is LOW during T_1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations. These pins are floated during a bus hold or reset.

Table 1. 80C186XL Pin Description (Continued)

<table>
<tr><th>Symbol</th><th>LCC PGA PLCC Pin No.</th><th>QFP Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{BHE}$</td><td>64</td><td>7</td><td>O</td><td>The $\overline{BHE}$ (Bus High Enable) signal is analogous to A0 in that it is used to enable data on to the most significant half of the data bus, pins D15–D8. $\overline{BHE}$ will be LOW during T_1 when the upper byte is transferred and will remain LOW through T_3 AND T_W. $\overline{BHE}$ does not need to be latched. $\overline{BHE}$ will float during HOLD or RESET.
In Enhanced Mode, $\overline{BHE}$ will also be used to signify DRAM refresh cycles. A refresh cycle is indicated by both $\overline{BHE}$ and A0 being HIGH.
$\overline{BHE}$ and A0 Encodings
<table><tr><th>$\overline{BHE}$ Value</th><th>A0 Value</th><th>Function</th></tr><tr><td>0</td><td>0</td><td>Word Transfer</td></tr><tr><td>0</td><td>1</td><td>Byte Transfer on upper half of data bus (D15–D8)</td></tr><tr><td>1</td><td>0</td><td>Byte Transfer on lower half of data bus (D_7–D_0)</td></tr><tr><td>1</td><td>1</td><td>Refresh</td></tr></table></td></tr>
<tr><td>ALE/QS0</td><td>61</td><td>10</td><td>O</td><td>Address Latch Enable/Queue Status 0 is provided by the 80C186XL to latch the address. ALE is active HIGH, with addresses guaranteed valid on the trailing edge.</td></tr>
<tr><td>$\overline{WR}$/QS1</td><td>63</td><td>8</td><td>O</td><td>Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. It is active LOW, and floats during bus hold or reset. When the 80C186XL is in Queue Status Mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.<table><tr><th>QS1</th><th>QS0</th><th>Queue Operation</th></tr><tr><td>0</td><td>0</td><td>No queue operation</td></tr><tr><td>0</td><td>1</td><td>First opcode byte fetched from the queue</td></tr><tr><td>1</td><td>1</td><td>Subsequent byte fetched from the queue</td></tr><tr><td>1</td><td>0</td><td>Empty the queue</td></tr></table></td></tr>
<tr><td>$\overline{RD}$/$\overline{QSMD}$</td><td>62</td><td>9</td><td>O/I</td><td>Read Strobe is an active LOW signal which indicates that the 80C186XL is performing a memory or I/O read cycle. It is guaranteed not to go LOW before the A/D bus is floated. An internal pull-up ensures that $\overline{RD}$/$\overline{QSMD}$ is HIGH during RESET. Following RESET the pin is sampled to determine whether the 80C186XL is to provide ALE, $\overline{RD}$, and $\overline{WR}$, or queue status information. To enable Queue Status Mode, $\overline{RD}$ must be connected to GND. $\overline{RD}$ will float during bus HOLD.</td></tr>
<tr><td>ARDY</td><td>55</td><td>20</td><td>I</td><td>Asynchronous Ready informs the 80C186XL that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUT and is active HIGH. The falling edge of ARDY must be synchronized to the 80C186XL clock. Connecting ARDY HIGH will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the SRDY pin.</td></tr>
<tr><td>SRDY</td><td>49</td><td>27</td><td>I</td><td>Synchronous Ready informs the 80C186XL that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active-HIGH input synchronized to CLKOUT. The use of SRDY allows a relaxed system timing over ARDY. This is accomplished by elimination of the one-half clock cycle required to internally synchonize the ARDY input signal. Connecting SRDY high will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the ARDY pin.</td></tr>
</table>

Table 1. 80C186XL Pin Description (Continued)

Symbol	LCC PGA PLCC Pin No.	QFP Pin No.	Type	Name and Function
$\overline{LOCK}$	48	28	O	$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus. $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction immediately following the LOCK prefix. It remains active until the completion of that instruction. No instruction prefetching will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ floats during bus hold or reset.
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	52 53 54	23 22 21	O O O	Bus cycle status $\overline{S0}$–$\overline{S2}$ are encoded to provide bus-transaction information: **80C186XL Bus Cycle Status Information** $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ — **Bus Cycle Initiated** 0 0 0 — Interrupt Acknowledge 0 0 1 — Read I/O 0 1 0 — Write I/O 0 1 1 — Halt 1 0 0 — Instruction Fetch 1 0 1 — Read Data from Memory 1 1 0 — Write Data to Memory 1 1 1 — Passive (no bus cycle) The status pins float during HOLD. $\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.
HOLD HLDA	50 51	26 25	I O	HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. The 80C186XL generates HLDA (HIGH) in response to a HOLD request. Simultaneous with the issuance of HLDA, the 80C186XL will float the local bus and control lines. After HOLD is detected as being LOW, the 80C186XL will lower HLDA. When the 80C186XL needs to run another bus cycle, it will again drive the local bus and control lines. In Enhanced Mode, HLDA will go low when a DRAM refresh cycle is pending in the 80C186XL and an external bus master has control of the bus. It will be up to the external master to relinquish the bus by lowering HOLD so that the 80C186XL may execute the refresh cycle.
$\overline{UCS}$	34	45	O/I	Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. $\overline{UCS}$ does not float during bus hold. The address range activating $\overline{UCS}$ is software programmable. $\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the 80C186XL will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{UCS}$ has a weak internal pullup that is active during RESET to ensure that the 80C186XL does not enter ONCE Mode inadvertently.
$\overline{LCS}$	33	46	O/I	Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. $\overline{LCS}$ does not float during bus HOLD. The address range activating $\overline{LCS}$ is software programmable.

Table 1. 80C186XL Pin Description (Continued)

Symbol	CLCC PGA PLCC Pin No.	QFP Pin No.	Type	Name and Function
$\overline{LCS}$ (Continued)				$\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the 80C186XL will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{LCS}$ has a weak internal pullup that is active only during RESET to ensure that the 80C186XL does not enter ONCE mode inadvertently.
$\overline{MCS0}$/PEREQ $\overline{MCS1}$/$\overline{ERROR}$ $\overline{MCS2}$ $\overline{MCS3}$/$\overline{NPS}$	38 37 36 35	39 40 41 42	O/I O/I O O	Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines do not float during bus HOLD. The address ranges activating $\overline{MCS0–3}$ are software programmable. In Enhanced Mode, $\overline{MCS0}$ becomes a PEREQ input (Processor Extension Request). When connected to the Math Coprocessor, this input is used to signal the 80C186XL when to make numeric data transfers to and from the coprocessor. $\overline{MCS3}$ becomes $\overline{NPS}$ (Numeric Processor Select) which may only be activated by communication to the 80C187. $\overline{MCS1}$ becomes $\overline{ERROR}$ in Enhanced Mode and is used to signal numerics coprocessor errors. $\overline{MCS0}$/PEREQ and $\overline{MCS1}$/$\overline{ERROR}$ have weak internal pullups which are active during reset.
$\overline{PCS0}$ $\overline{PCS1}$ $\overline{PCS2}$ $\overline{PCS3}$ $\overline{PCS4}$	25 27 28 29 30	54 52 51 50 49	O O O O O	Peripheral Chip Select signals 0–4 are active LOW when a reference is made to the defined peripheral area (64K byte I/O or 1 MByte memory space). These lines do not float during bus HOLD. The address ranges activating $\overline{PCS0–4}$ are software programmable.
$\overline{PCS5}$/A1	31	48	O	Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software-programmable. $\overline{PCS5}$/A1 does not float during bus HOLD. When programmed to provide latched A1, this pin will retain the previously latched value during HOLD.
$\overline{PCS6}$/A2	32	47	O	Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software-programmable. $\overline{PCS6}$/A2 does not float during bus HOLD. When programmed to provide latched A2, this pin will retain the previously latched value during HOLD.
DT/$\overline{R}$	40	37	O	Data Transmit/Receive controls the direction of data flow through an external data bus transceiver. When LOW, data is transferred to the 80C186XL. When HIGH the 80C186XL places write data on the data bus. DT/$\overline{R}$ floats during a bus hold or reset.
$\overline{DEN}$	39	38	O	Data Enable is provided as a data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access (including 80C187 access). $\overline{DEN}$ is HIGH whenever DT/$\overline{R}$ changes state. During RESET, $\overline{DEN}$ is driven HIGH for one clock, then floated. $\overline{DEN}$ also floats during HOLD.
N.C.	—	2, 11, 14 15, 24, 43, 44, 62, 63	—	Not connected. To maintain compatibility with future products, do not connect to these pins.

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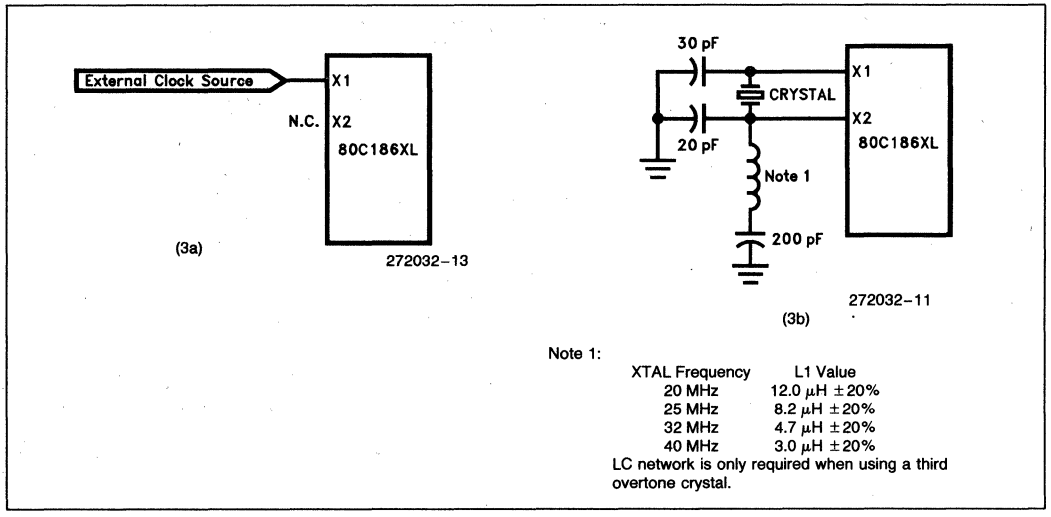

Figure 3. 80C186XL Oscillator Configurations (see text)

INTRODUCTION

The following Functional Description describes the base architecture of the 80C186XL. The 80C186XL is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip. The 80C186XL is object code compatible with the 8086/8088 microprocessors and adds 10 new instruction types to the 8086/8088 instruction set.

The 80C186XL has two major modes of operation, Compatible and Enhanced. In Compatible Mode the 80C186XL is completely compatible with NMOS 80186, with the exception of 8087 support. The Enhanced mode adds three new features to the system design. These are Power-Save control, Dynamic RAM refresh, and an asynchronous Numerics Coprocessor interface.

80C186XL BASE ARCHITECTURE

80C186XL Clock Generator

The 80C186XL provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

The 80C186XL oscillator circuit is designed to be used either with a parallel resonant fundamental or third-overtone mode crystal, depending upon the frequency range of the application. This is used as the time base for the 80C186XL.

The output of the oscillator is not directly available outside the 80C186XL. The recommended crystal configuration is shown in Figure 3b. When used in third-overtone mode, the tank circuit is recommended for stable operation. Alternately, the oscillator may be driven from an external source as shown in Figure 3a.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide by two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC Timings are referenced to CLKOUT.

Intel recommends the following values for crystal selection parameters.

Temperature Range:	Application Specific
ESR (Equivalent Series Resistance):	60Ω max
C_0 (Shunt Capacitance of Crystal):	7.0 pF max
C_1 (Load Capacitance):	20 pF ±5 pF
Drive Level:	2 mW max

Bus Interface Unit

The 80C186XL provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides outputs that can be used to enable external buffers and to direct the flow of data on and off the local bus.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information and data (for write operations) information. It is also responsible for reading data from the local bus during a read operation. Synchronous and asynchronous ready input pins are provided to extend a bus cycle beyond the minimum four states (clocks).

The 80C186XL bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus.

During RESET the local bus controller will perform the following action:

- Drive $\overline{DEN}$, $\overline{RD}$ and $\overline{WR}$ HIGH for one clock cycle, then float them.
- Drive $\overline{S0}$–$\overline{S2}$ to the inactive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Float AD0–15, A16–19, $\overline{BHE}$, DT/$\overline{R}$.
- Drive ALE LOW
- Drive HLDA LOW.

$\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$ and $\overline{TEST}$/BUSY pins have internal pullup devices which are active while $\overline{RES}$ is applied. Excessive loading or grounding certain of these pins causes the 80C186XL to enter an alternative mode of operation:

- $\overline{RD}$/$\overline{QSMD}$ low results in Queue Status Mode.
- $\overline{UCS}$ and $\overline{LCS}$ low results in ONCE™ Mode.
- $\overline{TEST}$/BUSY low (and high later) results in Enhanced Mode.

80C186XL PERIPHERAL ARCHITECTURE

All the 80C186XL integrated peripherals are controlled by 16-bit registers contained within an internal 256-byte control block. The control block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles. An offset map of the 256-byte control register block is shown in Figure 4.

Chip-Select/Ready Generation Logic

The 80C186XL contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

The 80C186XL provides 6 memory chip select outputs for 3 address areas; upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

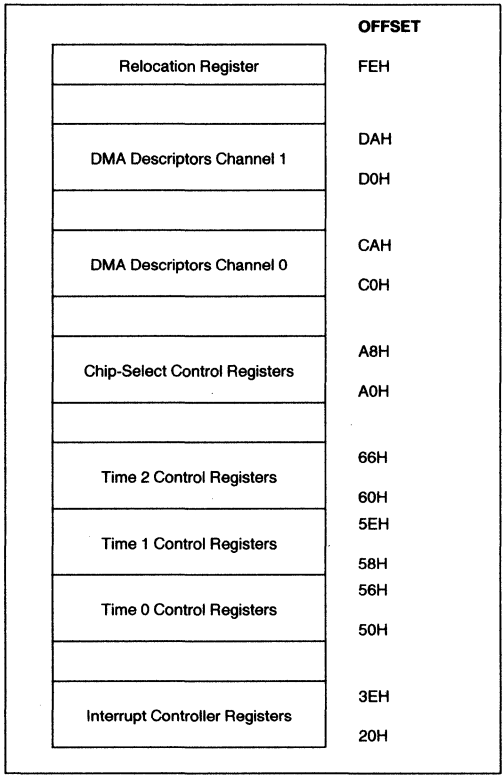

Figure 4. Internal Register Map

The 80C186XL provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the 80C186XL begins executing at memory location FFFF0H.

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The 80C186XL provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The 80C186XL provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located within the 80C186XL 1 Mbyte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The 80C186XL can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address may be located in either memory or I/O space.

The 80C186XL can generate a READY signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the 80C186XL may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

Upon RESET, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to insert 3 wait states in conjunction with external READY (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers.

DMA Unit

The 80C186XL DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data.

Timer/Counter Unit

The 80C186XL provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

Interrupt Control Unit

The 80C186XL can receive interrupts from a number of sources, both internal and external. The 80C186XL has 5 external and 2 internal interrupt sources (Timer/Couners and DMA). The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Enhanced Mode Operation

In Compatible Mode the 80C186XL operates with all the features of the NMOS 80186, with the exception of 8087 support (i.e. no math coprocessing is possible in Compatible Mode). Queue-Status information is still available for design purposes other than 8087 support.

All the Enhanced Mode features are completely masked when in Compatible Mode. A write to any of the Enhanced Mode registers will have no effect, while a read will not return any valid data.

In Enhanced Mode, the 80C186XL will operate with Power-Save, DRAM refresh, and numerics coprocessor support in addition to all the Compatible Mode features.

If connected to a math coprocessor, this mode will be invoked automatically. Without an NPX, this mode can be entered by tying the RESET output signal from the 80C186XL to the $\overline{TEST}$/BUSY input.

Queue-Status Mode

The queue-status mode is entered by strapping the $\overline{RD}$ pin low. $\overline{RD}$ is sampled at RESET and if LOW, the 80C186XL will reconfigure the ALE and $\overline{WR}$ pins to be QS0 and QS1 respectively. This mode is available on the 80C186XL in both Compatible and Enhanced Modes.

DRAM Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates DRAM refresh bus cycles. The RCU operates only in Enhanced Mode. After a programmable period of time, the RCU generates a memory read request to the BIU. If the address generated during a refresh bus cycle is within the range of a properly programmed chip select, that chip select will be activated when the BIU executes the refresh bus cycle.

Power-Save Control

The 80C186XL, when in Enhanced Mode, can enter a power saving state by internally dividing the processor clock frequency by a programmable factor. This divided frequency is also available at the CLKOUT pin.

All internal logic, including the Refresh Control Unit and the timers, have their clocks slowed down by the division factor. To maintain a real time count or a fixed DRAM refresh rate, these peripherals must be re-programmed when entering and leaving the power-save mode.

Interface for 80C187 Math Coprocessor

In Enhanced Mode, three of the mid-range memory chip selects are redefined according to Table 2 for use with the 80C187. The fourth chip select, $\overline{MCS2}$ functions as in compatible mode, and may be programmed for activity with ready logic and wait states accordingly. As in Compatible Mode, $\overline{MCS2}$ will function for one-fourth a programmed block size.

Table 2. $\overline{MCS}$ Assignments

Compatible Mode	Enhanced Mode	
$\overline{MCS0}$	PEREQ	Processor Extension Request
$\overline{MCS1}$	$\overline{ERROR}$	NPX Error
$\overline{MCS2}$	$\overline{MCS2}$	Mid-Range Chip Select
$\overline{MCS3}$	$\overline{NPS}$	Numeric Processor Select

ONCE™ Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C186XL has a test mode available which allows all pins to be placed in a high-impedance state. ONCE stands for "ON Circuit Emulation". When placed in this mode, the 80C186XL will put all pins in the high-impedance state until RESET.

The ONCE mode is selected by tying the $\overline{UCS}$ and the $\overline{LCS}$ LOW during RESET. These pins are sampled on the low-to-high transition of the $\overline{RES}$ pin. The $\overline{UCS}$ and the $\overline{LCS}$ pins have weak internal pull-up resistors similar to the $\overline{RD}$ and $\overline{TEST}$/BUSY pins to guarantee ONCE Mode is not entered inadvertently during normal operation. $\overline{LCS}$ and $\overline{UCS}$ must be held low at least one clock after $\overline{RES}$ goes high to guarantee entrance into ONCE Mode.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias .... 0°C to +70°C

Storage Temperature ..... −65°C to +150°C

Voltage on Any Pin with Respect to Ground ..... −1.0V to +7.0V

/Package Power Dissipation 1W

Not to exceed the maximum allowable die temperature based on thermal resistance of the package.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTICE: The specifications are subject to change without notice.

DC CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except X1)	−0.5	0.2 V_{CC} − 0.3	V	
V_{IL1}	Clock Input Low Voltage (X1)	−0.5	0.6	V	
V_{IH}	Input High Voltage (All except X1 and $\overline{RES}$)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC} + 0.5	V	
V_{IH2}	Clock Input High Voltage (X1)	3.9	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA (S0, 1, 2) I_{OL} = 2.0 mA (others)
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −2.4 mA @ 2.4V (4)
		V_{CC} − 0.5	V_{CC}	V	I_{OH} = −200 µA @ V_{CC} −0.5(4)
I_{CC}	Power Supply Current		100	mA	@ 20 MHz, 0°C V_{CC} = 5.5V(3)
			80	mA	@16 MHz, 0°C V_{CC} = 5.5V(3)
			65	mA	@ 12.5 MHz, 0°C V_{CC} = 5.5V (3)
			50	mA	@ 10 MHz, 0°C V_{CC} = 5.5V (3)
			100	µA	@ DC 0°C V_{CC} = 5.5V
I_{LI}	Input Leakage Current		±10	µA	@ 0.5 MHz, 0.45V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	µA	@ 0.5 MHz, 0.45V ≤ V_{OUT} ≤ V_{CC}(1)
V_{CLO}	Clock Output Low		0.45	V	I_{CLO} = 4.0 mA

DC CHARACTERISTICS (Continued) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{CHO}	Clock Output High	$V_{CC} - 0.5$		V	$I_{CHO} = -500\ \mu A$
C_{IN}	Input Capacitance		10	pF	@ 1 MHz(2)
C_{IO}	Output or I/O Capacitance		20	pF	@ 1 MHz(2)

NOTES:
1. Pins being floated during HOLD or by invoking the ONCE Mode.
2. Characterization conditions are a) Frequency = 1 MHz; b) Unmeasured pins at GND; c) V_{IN} at + 5.0V or 0.45V. This parameter is not tested.
3. Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.
4. $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$ and $\overline{TEST}$/BUSY pins have internal pullup devices. Loading some of these pins above $I_{OH} = -200\ \mu A$ can cause the 80C186XL to go into alternative modes of operation. See the section on Local Bus Controller and Reset for details.

POWER SUPPLY CURRENT

Current is linearly proportional to clock frequency and is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.

Maximum current is given by $I_{CC} = 5\ mA \times$ freq. (MHz) + I_{QL}.

I_{QL} is the quiescent leakage current when the clock is static. I_{QL} is typically less than 100 μA.

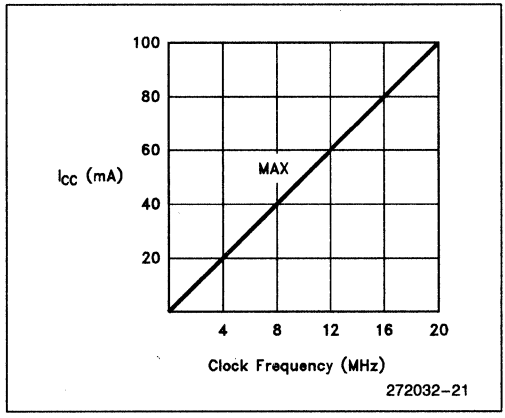

Figure 5. I_{CC} vs Frequency

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AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (READ CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL		80C186XL12			
		Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	40	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 18		T_{CLCH} − 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 15		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	ns	
T_{CLCSV}	Chip-Select Active Delay	3	42	3	33	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	35	3	30	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	44	3	37	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay	3	44	3	37	ns	
T_{CHCTV}	Control Active Delay 2	3	44	3	37	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	ns	
80C186XL TIMING RESPONSES (Read Cycle)							
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	3	44	3	37	ns	
T_{RLRH}	$\overline{RD}$ Pulse Width	$2T_{CLCL}$ − 30		$2T_{CLCL}$ − 25		ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	3	44	3	37	ns	
T_{RHLH}	$\overline{RD}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	T_{CLCL} − 15		T_{CLCL} − 15		ns	Equal Loading

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (READ CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL16		80C186XL20			
		Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		10		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	31	3	25	ns	
T_{CLSH}	Status Inactive Delay	3	30	3	25	ns	
T_{CLAV}	Address Valid Delay	3	33	3	27	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	33	3	27	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 15		T_{CLCH} − 10		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 10		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	ns	
T_{CLCSV}	Chip-Select Active Delay	3	30	3	25	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	t_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	25	3	20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	31	3	22	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay	3	31	3	22	ns	
T_{CHCTV}	Control Active Delay 2	3	31	3	22	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	35	3	22	ns	
80C186XL TIMING RESPONSES (Read Cycle)							
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	3	31	3	27	ns	
T_{RLRH}	$\overline{RD}$ Pulse Width	2T_{CLCL} − 25		2T_{CLCL} − 20		ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	3	31	3	27	ns	
T_{RHLH}	$\overline{RD}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	T_{CLCL} − 15		T_{CLCL} − 15		ns	Equal Loading

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AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (WRITE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL		80C186XL12			
		Min	Max	Min	Max		
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	40	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 18		T_{CLCH} − 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 15		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLDOX}	Data Hold Time	3		3		ns	
T_{CVCTV}	Control Active Delay 1	3	44	3	37	ns	
T_{CVCTX}	Control Inactive Delay	3	44	3	37	ns	
T_{CLCSV}	Chip-Select Active Delay	3	42	3	33	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	35	3	30	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	ns	
80C186XL TIMING RESPONSES (Write Cycle)							
T_{WLWH}	$\overline{WR}$ Pulse Width	$2T_{CLCL}$ − 30		$2T_{CLCL}$ − 25		ns	
T_{WHLH}	$\overline{WR}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{WHDX}	Data Hold after $\overline{WR}$	T_{CLCL} − 34		T_{CLCL} − 20		ns	Equal Loading
T_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (WRITE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL16		80C186XL20			
		Min	Max	Min	Max		
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	31	3	25	ns	
T_{CLSH}	Status Inactive Delay	3	30	3	25	ns	
T_{CLAV}	Address Valid Delay	3	33	3	27	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	33	3	27	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 15		T_{CLCH} − 10		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 10		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLDOX}	Data Hold Time	3		3		ns	
T_{CVCTV}	Control Active Delay 1	3	31	3	25	ns	
T_{CVCTX}	Control Inactive Delay	3	31	3	25	ns	
T_{CLCSV}	Chip-Select Active Delay	3	30	3	25	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	25	3	20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	35	3	22	ns	
80C186XL TIMING RESPONSES (Write Cycle)							
T_{WLWH}	$\overline{WR}$ Pulse Width	$2T_{CLCL}$ − 25		$2T_{CLCL}$ − 20		ns	
T_{WHLH}	$\overline{WR}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{WHDX}	Data Hold after $\overline{WR}$	T_{CLCL} − 20		T_{CLCL} − 15		ns	Equal Loading
T_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading

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AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (INTERRUPT ACKNOWLEDGE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL		80C186XL12			
		Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	40	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 18		T_{CLCH} − 15		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 15		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	ns	
T_{CVCTV}	Control Active Delay 1	3	44	3	37	ns	
T_{CVCTX}	Control Inactive Delay	3	44	3	37	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	44	3	37	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycles)	3	44	3	37	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	ns	

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (INTERRUPT ACKNOWLEDGE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL16		80C186XL20			
		Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		10		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	31	3	25	ns	
T_{CLSH}	Status Inactive Delay	3	30	3	25	ns	
T_{CLAV}	Address Valid Delay	3	33	3	27	ns	
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	33	3	27	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 15		T_{CLCH} − 10		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 10		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	ns	
T_{CVCTV}	Control Active Delay 1	3	31	3	25	ns	
T_{CVCTX}	Control Inactive Delay	3	31	3	25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	31	3	22	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycles)	3	31	3	22	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	35	3	22	ns	

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AC CHARACTERISTICS

SOFTWARE HALT CYCLE TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL		80C186XL12			
		Min	Max	Min	Max		
80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low		0		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	44	3	37	ns	

Symbol	ParameterTarget	Values				Unit	Test Conditions
		80C186XL16		80C186XL20			
		Min	Max	Min	Max		
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	31	3	25	ns	
T_{CLSH}	Status Inactive Delay	3	30	3	25	ns	
T_{CLAV}	Address Valid Delay	3	33	3	27	ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low		0		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	31	3	22	ns	

AC CHARACTERISTICS

CLOCK TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL		80C186XL12			
		Min	Max	Min	Max		
80C186XL CLKIN REQUIREMENTS(1)							
T_{CKIN}	CLKIN Period	50	∞	40	∞	ns	
T_{CLCK}	CLKIN Low Time	20	∞	16	∞	ns	1.5V(2)
T_{CHCK}	CLKIN High Time	20	∞	16	∞	ns	1.5V(2)
T_{CKHL}	CLKIN Fall Time		5		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5		5	ns	1.0 to 3.5V
80C186XL CLKOUT TIMING							
T_{CICO}	CLKIN to CLKOUT Skew		25		21	ns	
T_{CLCL}	CLKOUT Period	100	∞	80	∞	ns	
T_{CLCH}	CLKOUT Low Time	0.5 T_{CLCL} − 6		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(3)
T_{CHCL}	CLKOUT High Time	0.5 T_{CLCL} − 6		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(4)
T_{CH1CH2}	CLKOUT Rise Time		10		10	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		10		10	ns	3.5 to 1.0V

NOTES:
1. External clock applied to X1 and X2 not connected.
2. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}.
3. Tested under worst case conditions: V_{CC} = 5.5V T_A = 70°C.
4. Tested under worst case conditions: V_{CC} = 4.5V T_A = 0°C.

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AC CHARACTERISTICS

CLOCK TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL16		80C186XL20			
		Min	Max	Min	Max		
80C186XL CLKIN REQUIREMENTS(1)							
T_{CKIN}	CLKIN Period	31.25	∞	25	∞	ns	
T_{CLCK}	CLKIN Low Time	13	∞	10	∞	ns	1.5V(2)
T_{CHCK}	CLKIN High Time	13	∞	10	∞	ns	1.5V(2)
T_{CKHL}	CLKIN Fall Time		5		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5		5	ns	1.0 to 3.5V
80C186XL CLKOUT TIMING							
T_{CICO}	CLKIN to CLKOUT Skew		17		17	ns	
T_{CLCL}	CLKOUT Period	62.5		50		ns	
T_{CLCH}	CLKOUT Low Time	0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(3)
T_{CHCL}	CLKOUT High Time	0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(4)
T_{CH1CH2}	CLKOUT Rise Time		10		8	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		10		8	ns	3.5 to 1.0V

NOTES:
1. External clock applied to X1 and X2 not connected.
2. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}.
3. Tested under worst case conditions: V_{CC} = 5.5V. T_A = 70°C.
4. Tested under worst case conditions: V_{CC} = 4.5V. T_A = 0°C.

AC CHARACTERISTICS

READY, PERIPHERAL AND QUEUE STATUS TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL		80C186XL12			
		Min	Max	Min	Max		
80C186XL READY AND PERIPHERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	15		15		ns	
T_{CLSRY}	SRDY Transition Hold Time(1)	15		15		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time(2)	15		15		ns	
T_{CLARX}	ARDY Active Hold Time(1)	15		15		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	15		15		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	25		25		ns	
T_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time(2)	15		15		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time(2)	15		15		ns	
80C186XL PERIPHERAL AND QUEUE STATUS TIMING RESPONSES							
T_{CLTMV}	Timer Output Delay		40		33	ns	
T_{CHQSV}	Queue Status Delay		37		32	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

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AC CHARACTERISTICS

READY, PERIPHERAL, AND QUEUE STATUS TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL16		80C186XL20			
		Min	Max	Min	Max		
80C186XL READY AND PERIPHERAL TIMING REQUIREMENTS							
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	15		10		ns	
T_{CLSRY}	SRDY Transition Hold Time(1)	15		10		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time(2)	15		10		ns	
T_{CLARX}	ARDY Active Hold Time(1)	15		10		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	15		10		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	25		15		ns	
T_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time(2)	15		10		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time(2)	15		10		ns	
80C186XL PERIPHERAL AND QUEUE STATUS TIMING RESPONSES							
T_{CLTMV}	Timer Output Delay		27		22	ns	
T_{CHQSV}	Queue Status Delay		30		27	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

AC CHARACTERISTICS

RESET AND HOLD/HLDA TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL		80C186XL12			
		Min	Max	Min	Max		
80C186XL RESET AND HOLD/HLDA TIMING REQUIREMENTS							
T_{RESIN}	$\overline{RES}$ Setup	15		15		ns	
T_{HVCL}	HOLD Setup(1)	15		15		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
80C186XL RESET AND HOLD/HLDA TIMING RESPONSES							
T_{CLRO}	Reset Delay		40		33	ns	
T_{CLHAV}	HLDA Valid Delay	3	40	3	33	ns	
T_{CHCZ}	Command Lines Float Delay		40		33	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		44		36	ns	

NOTE:
1. To guarantee recognition at next clock.

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AC CHARACTERISTICS

RESET AND HOLD/HLDA TIMINGS

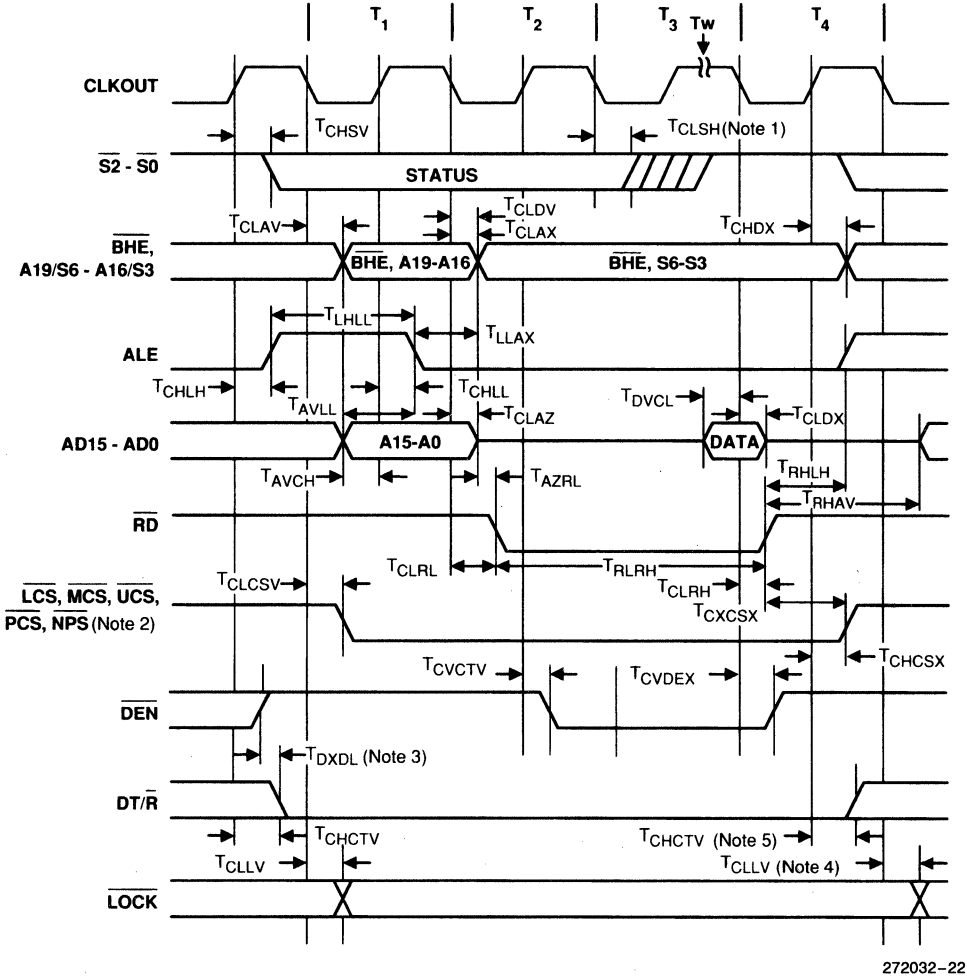
T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C186XL16		80C186XL20			
		Min	Max	Min	Max		
80C186XL RESET AND HOLD/HLDA TIMING REQUIREMENTS							
T_{RESIN}	$\overline{RES}$ Setup	15		15		ns	
T_{HVCL}	HOLD Setup(1)	15		10		ns	
80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	ns	
T_{CLAV}	Address Valid Delay	3	33	3	22	ns	
80C186XL RESET AND HOLD/HLDA TIMING RESPONSES							
T_{CLRO}	Reset Delay		27		22	ns	
T_{CLHAV}	HLDA Valid Delay	3	25	3	22	ns	
T_{CHCZ}	Command Lines Float Delay		28		25	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		32		26	ns	

NOTE:
1. To guarantee recognition at next clock.

AC CHARACTERISTICS

READ CYCLE WAVEFORMS

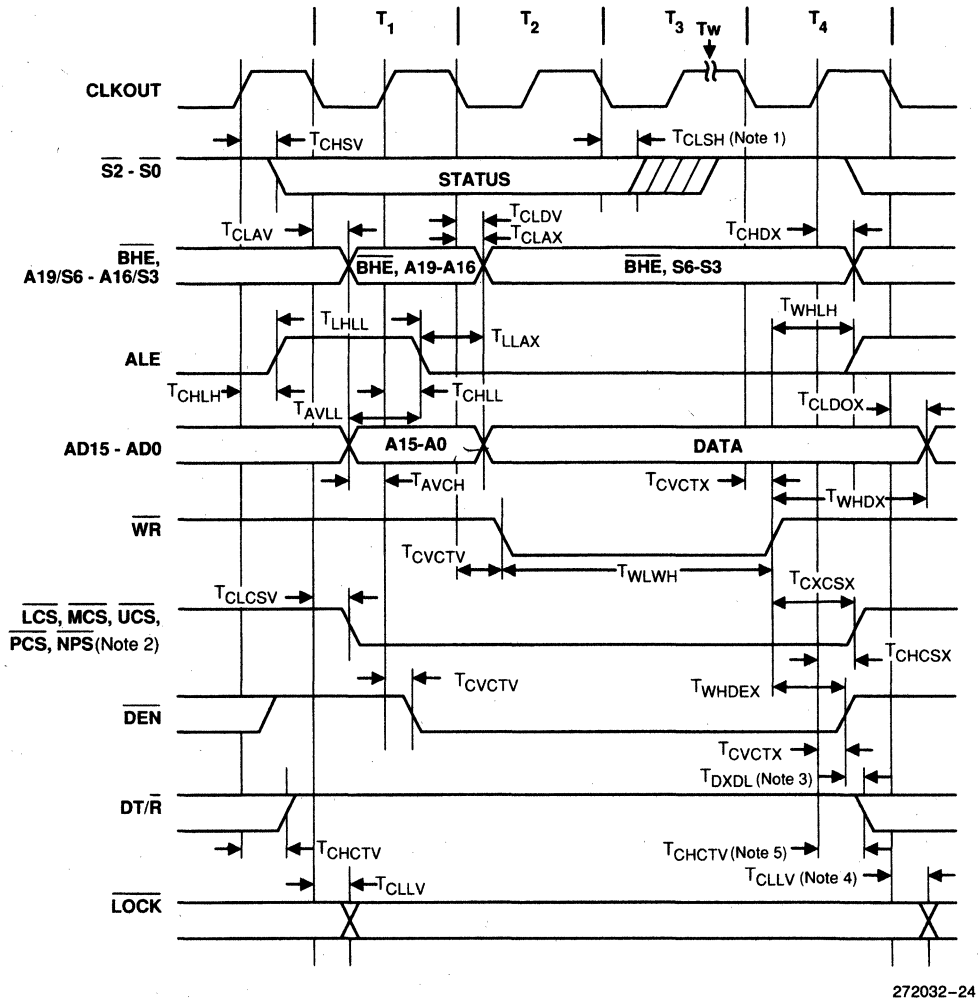


NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by write.

Figure 6

AC CHARACTERISTICS

WRITE CYCLE WAVEFORMS

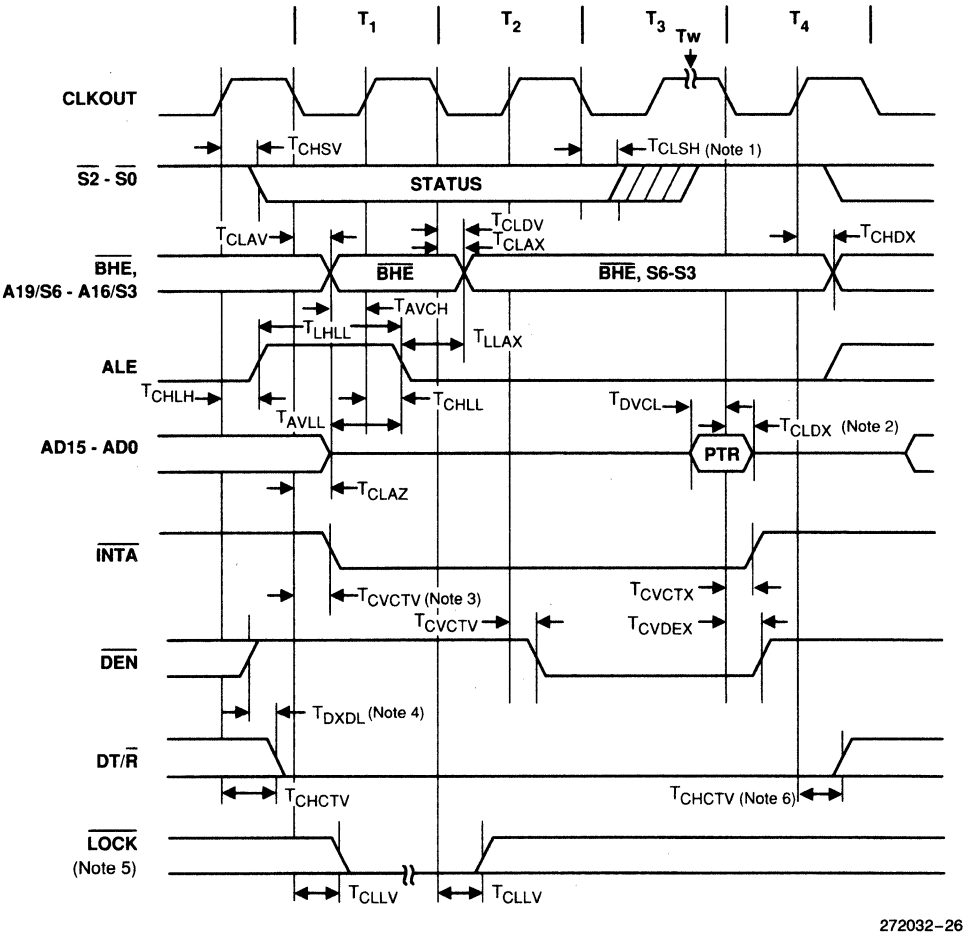


NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by read, INTA, or halt.

Figure 7

AC CHARACTERISTICS

INTERRUPT ACKNOWLEDGE CYCLE WAVEFORMS



NOTES:
1. Status inactive in state preceding T_4.
2. The data hold time lasts only until $\overline{INTA}$ goes inactive, even if the $\overline{INTA}$ transition occurs prior to T_{CLDX} (min).
3. $\overline{INTA}$ occurs one clock later in Slave Mode.
4. For write cycle followed by interrupt acknowledge cycle.
5. $\overline{LOCK}$ is active upon T_1 of the first interrupt acknowledge cycle and inactive upon T_2 of the second interrupt acknowledge cycle.
6. Changes in T-state preceding next bus cycle if followed by write.

Figure 8

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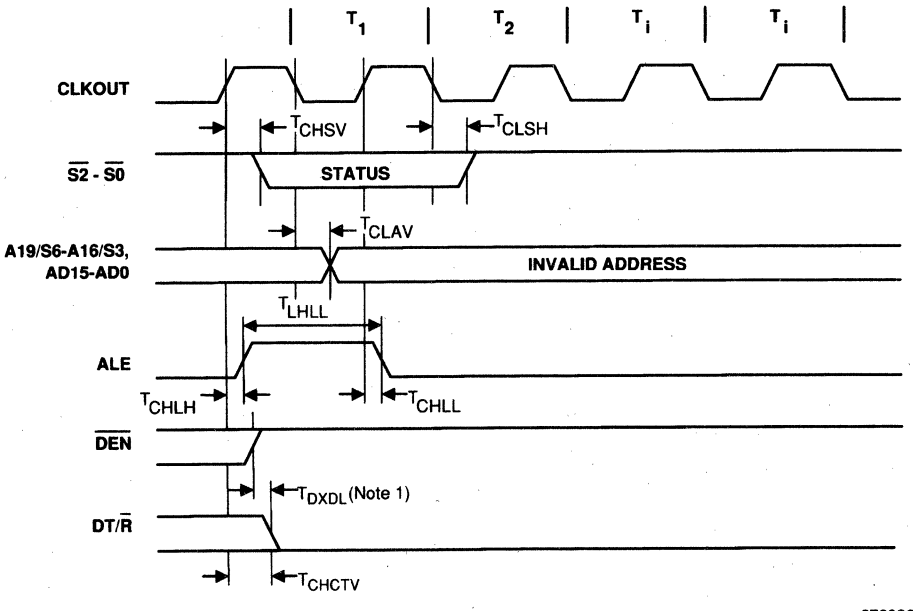
AC CHARACTERISTICS

SOFTWARE HALT CYCLE WAVEFORMS



NOTE:
1. For write cycle followed by halt cycle.

Figure 9

WAVEFORMS

CLOCK WAVEFORMS

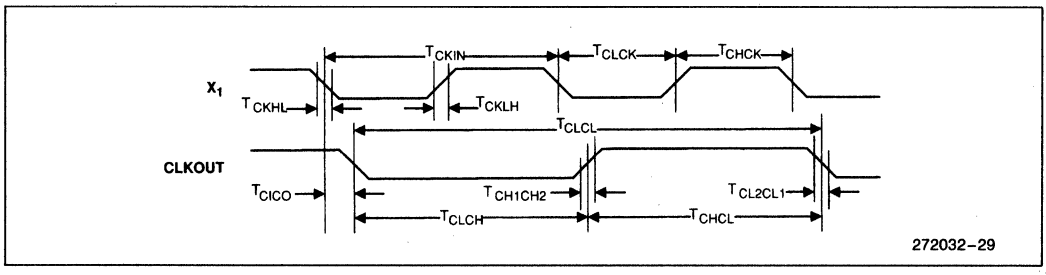


Figure 10

RESET WAVEFORMS

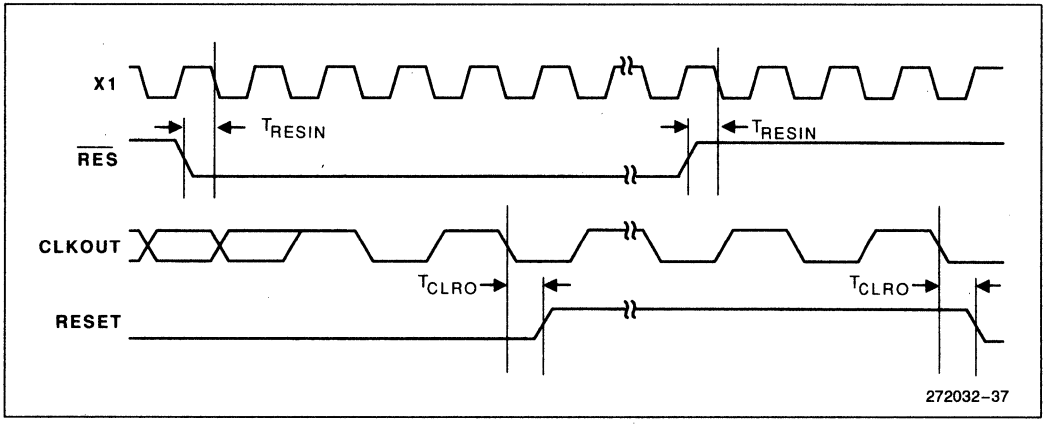


Figure 11

SYNCHRONOUS READY (SRDY) WAVEFORMS

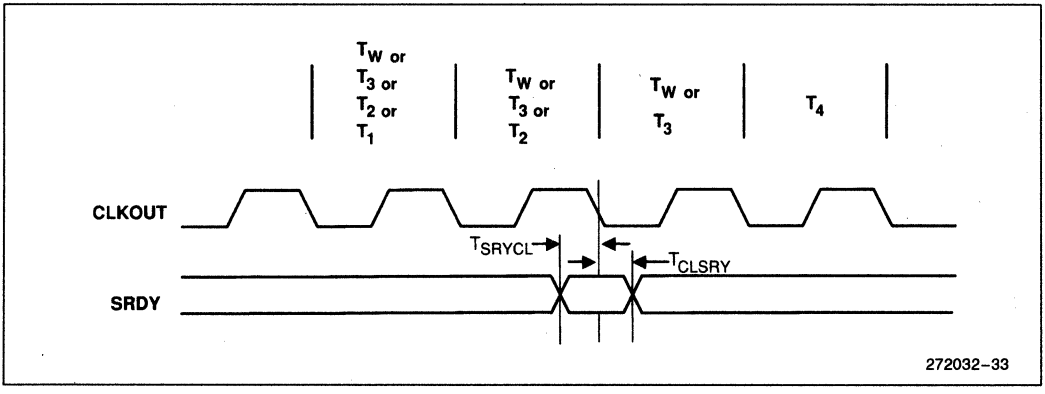


Figure 12

AC CHARACTERISTICS

ASYNCHRONOUS READY (ARDY) WAVEFORMS

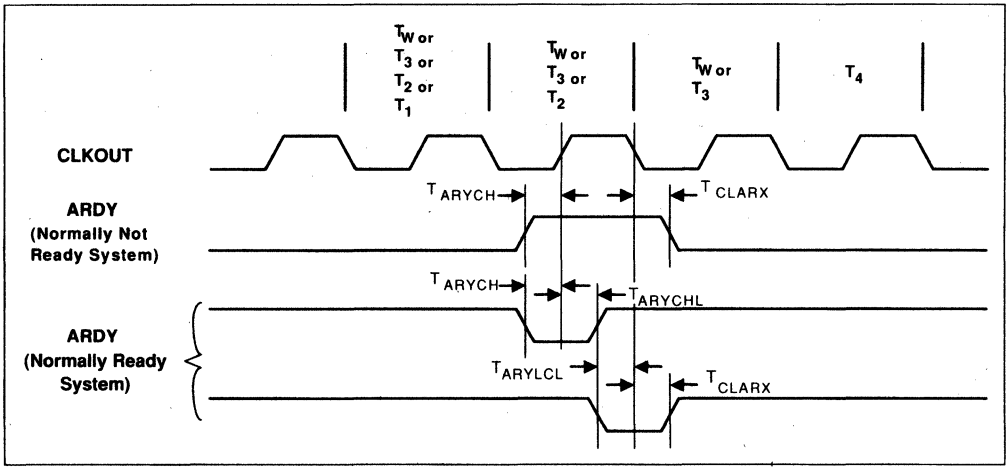


Figure 13

PERIPHERAL AND QUEUE STATUS WAVEFORMS

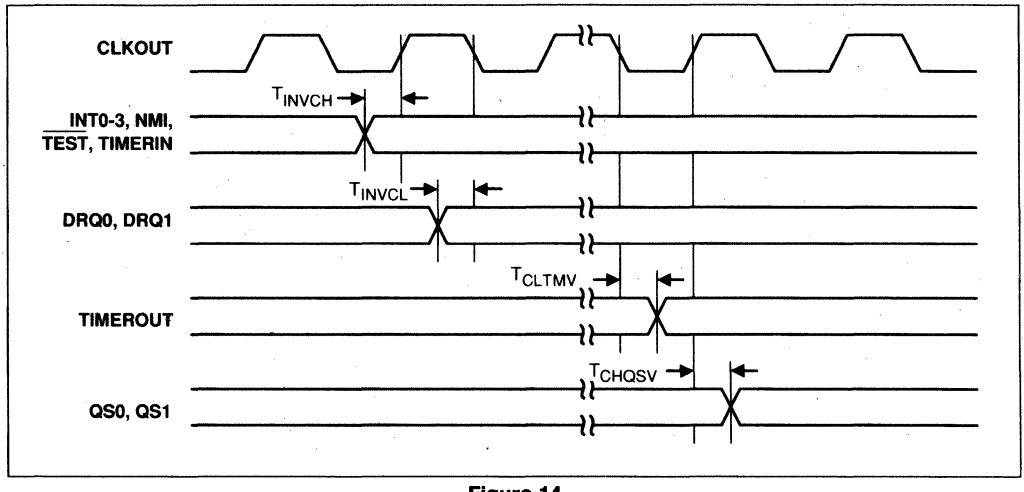


Figure 14

272032-34

AC CHARACTERISTICS

HOLD/HLDA WAVEFORMS (Entering Hold)

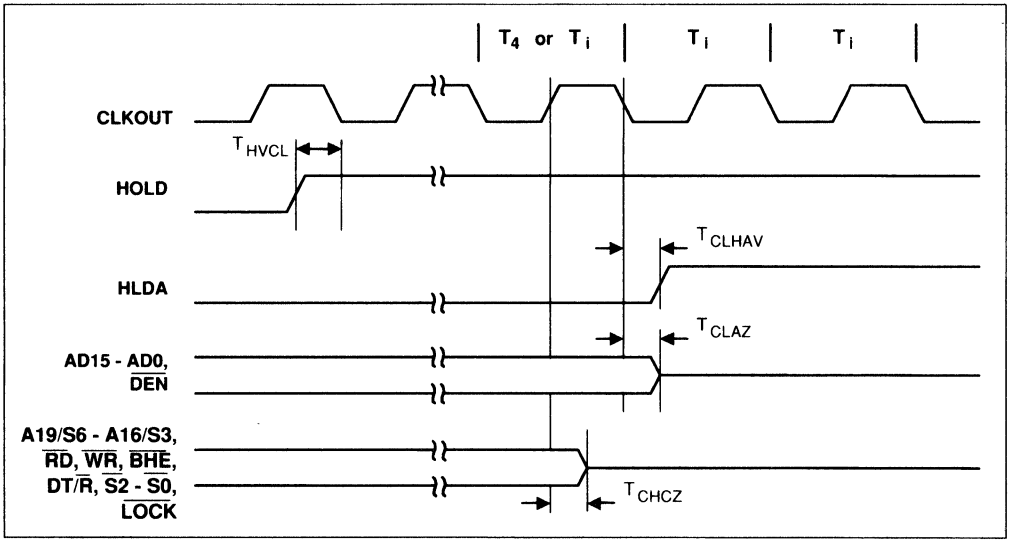


Figure 15

HOLD/HLDA WAVEFORMS (Leaving Hold)

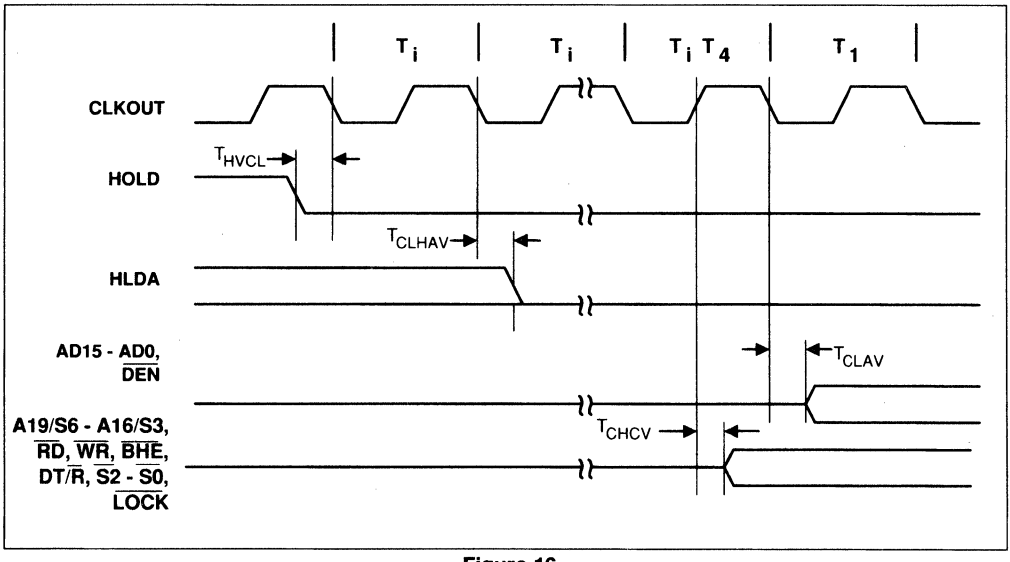


Figure 16

272032-36

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has from 5 to 7 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
ARY: Asynchronous Ready Input
C: Clock Output
CK: Clock Input
CS: Chip Select
CT: Control (DT/$\overline{R}$, $\overline{DEN}$, . . .)
D: Data Input
DE: $\overline{DEN}$
H: Logic Level High
OUT: Input (DRQ0, TIM0, . . .)
L: Logic Level Low or ALE
O: Output
QS: Queue Status (QS1, QS2)
R: $\overline{RD}$ Signal, RESET Signal
S: Status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$)
SRY: Synchronous Ready Input
V: Valid
W: WR Signal
X: No Longer a Valid Logic Level
Z: Float

Examples:

T_{CLAV} — Time from Clock low to Address valid
T_{CHLH} — Time from Clock high to ALE high
T_{CLCSV} — Time from Clock low to Chip Select valid

DERATING CURVES

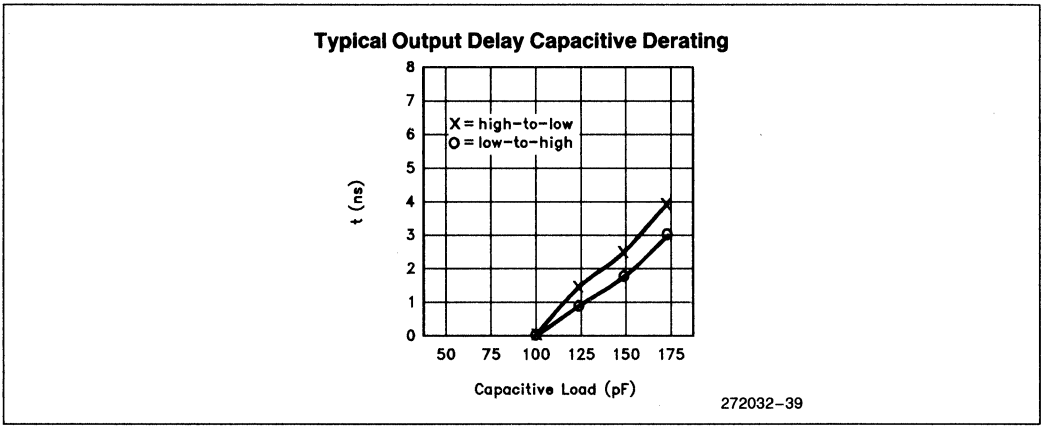


Figure 17. Capacitive Derating Curve

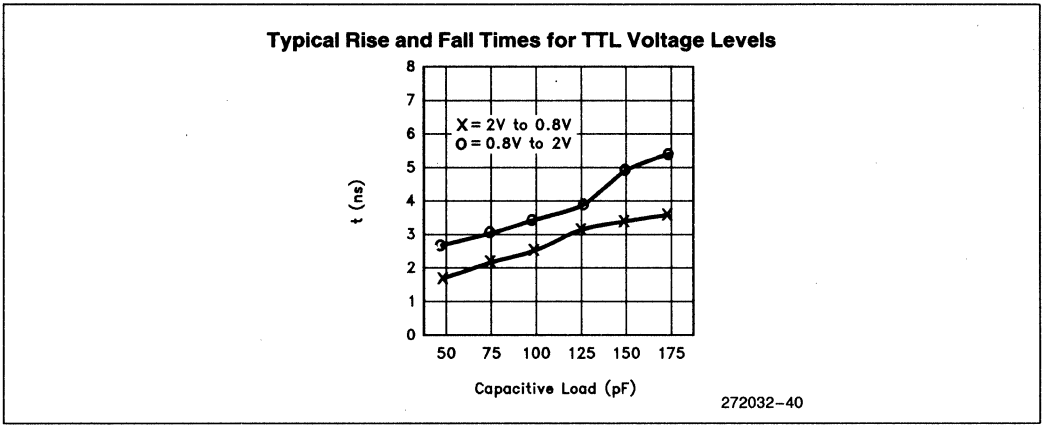


Figure 18. TTL Level Rise and Fall Times for Output Buffers

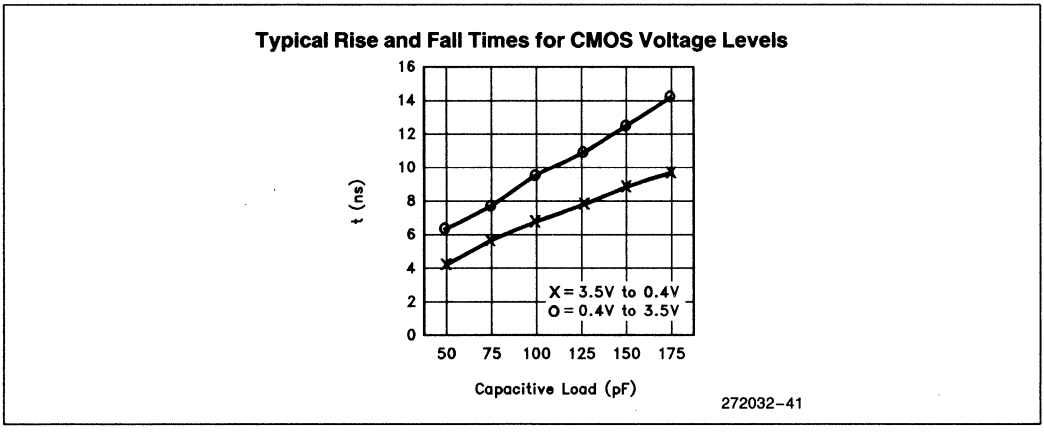


Figure 19. CMOS Level Rise and Fall Times for Output Buffers

80C186XL EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the 80C186XL microprocessor. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The 80C186XL EXPRESS program includes an extended temperature range. With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

Package types and EXPRESS versions are identified by a one or two-letter prefix to the part number. The prefixes are listed in Table 3. All AC and DC specifications not mentioned in this section are the same for both commercial and EXPRESS parts.

Table 3. Prefix Identification

Prefix	Package Type	Temperature Range
A	PGA	Commercial
N	PLCC	Commercial
R	LCC	Commercial
S	QFP	Commercial
TA	PGA	Extended
TN	PLCC	Extended
TR	LCC	Extended
TS	QFP	Extended

80C186XL EXECUTION TIMINGS

A determination of 80C186XL program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the 80C186XL has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1000100w	mod reg r/m			2/12	
Register/memory to register	1000101w	mod reg r/m			2/9	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12–13	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3–4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8	
Accumulator to memory	1010001w	addr-low	addr-high		9	
Register/memory to segment register	10001110	mod 0 reg r/m			2/9	
Segment register to register/memory	10001100	mod 0 reg r/m			2/11	
PUSH = Push:						
Memory	11111111	mod 1 1 0 r/m			16	
Register	01010 reg				10	
Segment register	000reg110				9	
Immediate	011010s0	data	data if s=0		10	
PUSHA = Push All	01100000				36	
POP = Pop:						
Memory	10001111	mod 0 0 0 r/m			20	
Register	01011 reg				10	
Segment register	000reg111	(reg≠01)			8	
POPA = Pop All	01100001				51	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10	
Variable port	1110110w				8	
OUT = Output to:						
Fixed port	1110011w	port			9	
Variable port	1110111w				7	
XLAT = Translate byte to AL	11010111				11	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		18	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		18	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				9	
POPF = Pop flags	10011101				8	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10	
Register with register/memory	0011100w	mod reg r/m			3/10	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26–28	
Register-Word					35–37	
Memory-Byte					32–34	
Memory-Word					41–43	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
ARITHMETIC (Continued)			
IMUL = Integer multiply (signed):	1111011w | mod101 r/m		
Register-Byte		25–28	
Register-Word		34–37	
Memory-Byte		31–34	
Memory-Word		40–43	
IMUL = Integer Immediate multiply (signed)	011010s1 | mod reg r/m | data | data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w | mod110 r/m		
Register-Byte		29	
Register-Word		38	
Memory-Byte		35	
Memory-Word		44	
IDIV = Integer divide (signed):	1111011w | mod111 r/m		
Register-Byte		44–52	
Register-Word		53–61	
Memory-Byte		50–58	
Memory-Word		59–67	
AAM = ASCII adjust for multiply	11010100 | 00001010	19	
AAD = ASCII adjust for divide	11010101 | 00001010	15	
CBW = Convert byte to word	10011000	2	
CWD = Convert word to double word	10011001	4	
LOGIC			
Shift/Rotate Instructions:			
Register/Memory by 1	1101000w | mod TTT r/m	2/15	
Register/Memory by CL	1101001w | mod TTT r/m	5+n/17+n	
Register/Memory by Count	1100000w | mod TTT r/m | count	5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR		
AND = **And:**			
Reg/memory and register to either	001000dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod100 r/m | data | data if w=1	4/16	
Immediate to accumulator	0010010w | data | data if w=1	3/4	8/16-bit
TEST = **And function to flags, no result:**			
Register/memory and register	1000010w | mod reg r/m	3/10	
Immediate data and register/memory	1111011w | mod000 r/m | data | data if w=1	4/10	
Immediate data and accumulator	1010100w | data | data if w=1	3/4	8/16-bit
OR = **Or:**			
Reg/memory and register to either	000010dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod001 r/m | data | data if w=1	4/16	
Immediate to accumulator	0000110w | data | data if w=1	3/4	8/16-bit

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
XOR = Exclusive or:						
Reg/memory and register to either	001100dw	mod reg r/m			3/10	
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	4/16	
Immediate to accumulator	0011010w	data	data if w=1		3/4	8/16-bit
NOT = Invert register/memory	1111011w	mod 010 r/m			3/10	
STRING MANIPULATION						
MOVS = Move byte/word	1010010w				14	
CMPS = Compare byte/word	1010011w				22	
SCAS = Scan byte/word	1010111w				15	
LODS = Load byte/wd to AL/AX	1010110w				12	
STOS = Store byte/wd from AL/AX	1010101w				10	
INS = Input byte/wd from DX port	0110110w				14	
OUTS = Output byte/wd to DX port	0110111w				14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	11110010	1010010w			8+8n	
CMPS = Compare string	1111001z	1010011w			5+22n	
SCAS = Scan string	1111001z	1010111w			5+15n	
LODS = Load string	11110010	1010110w			6+11n	
STOS = Store string	11110010	1010101w			6+9n	
INS = Input string	11110010	0110110w			8+8n	
OUTS = Output string	11110010	0110111w			8+8n	
CONTROL TRANSFER						
CALL = Call:						
Direct within segment	11101000	disp-low	disp-high		15	
Register/memory indirect within segment	11111111	mod 010 r/m			13/19	
Direct intersegment	10011010	segment offset			23	
		segment selector				
Indirect intersegment	11111111	mod 011 r/m	(mod ≠ 11)		38	
JMP = Unconditional jump:						
Short/long	11101011	disp-low			14	
Direct within segment	11101001	disp-low	disp-high		14	
Register/memory indirect within segment	11111111	mod 100 r/m			11/17	
Direct intersegment	11101010	segment offset			14	
		segment selector				
Indirect intersegment	11111111	mod 101 r/m	(mod ≠ 11)		26	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
RET = **Return from CALL:**						
Within segment	11000011				16	
Within seg adding immed to SP	11000010	data-low	data-high		18	
Intersegment	11001011				22	
Intersegment adding immediate to SP	11001010	data-low	data-high		25	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22+16(n−1)	
LEAVE = Leave Procedure	11001001				8	
INT = **Interrupt:**						
Type specified	11001101	type			47	
Type 3	11001100				45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110				48/4	
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33-35	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	
	(TTT LLL are opcode to processor extension)		

Shaded areas indicate instructions not available in 8086/8088 microsystems.

FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

REVISION HISTORY

The following changes were made between the -001 and -002 versions of the 80C186XL data sheets. The -002 data sheet applies to any 80C188XL with a "B" alpha character after the FPO number. The FPO number location is show in Figure 2.

1. Much of the information provided in the -001 version of the data sheet has been removed. Detail descriptions of part functionality may be found in the 80C186XL User's Manual.
2. All AC Timing waveforms were combined at the end of the AC Characteristics section.
3. T_{WHLH} for the 80C186XL12 was changed from $T_{CLCH} - 10$ to $T_{CLCH} - 14$ due to a previous typographical error.
4. T_{RESIN} for the 80C186XL20 was change from 10 ns to 15 ns.
5. Output test conditions were changed from C_L = 50–200 pF to C_L = 50 pF to reflect newer test equipment. Note: this has no effect on AC Timing specifications.

ERRATA

An A or B step 80C186XL has the following errata. The A or B step 80C186XL can be identified by the presence of an "A" or "B" alpha character, respectively, next to the FPO number. The FPO number location is shown in Figure 2.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the INTA1 line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistently, it is dependent on interrupt timing.

PRODUCT IDENTIFICATION

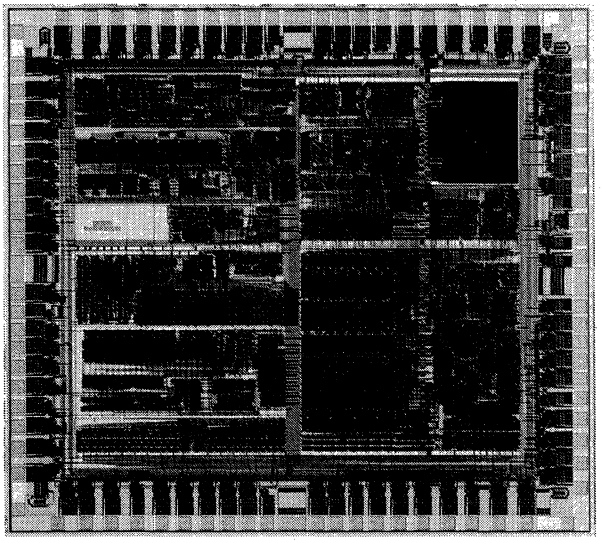
Intel 80C186XL devices are marked with a 9-character alphanumeric Intel FPO number underneath the product number. This data sheet (272032-002) is valid for 80C186XL devices with an "A" or "B" as the ninth character in the FPO number, as illustrated in Figure 2.

80C186EA20, 16, 12
16-BIT HIGH INTEGRATION EMBEDDED PROCESSOR

- **80C186 Upgrade for Power Critical Applications**
- **Full Static Operation**
- **True CMOS Inputs and Outputs**

- **Integrated Feature Set**
  - **Static 186 CPU Core**
  - **Power Save, Idle and Powerdown Modes**
  - **Clock Generator**
  - **2 Independent DMA Channels**
  - **3 Programmable 16-Bit Timers**
  - **Dynamic RAM Refresh Control Unit**
  - **Programmable Memory and Peripheral Chip Select Logic**
  - **Programmable Wait State Generator**
  - **Local Bus Controller**
  - **System-Level Testing Support (High Impedance Test Mode)**
- **Speed Versions Available:**
  - **20 MHz (80C186EA20)**
  - **16 MHz (80C186EA16)**
  - **12.5 MHz (80C186EA12)**
- **Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O**
- **Complete System Development Support**
  - **All 8086/8088 and 80C186 Family Software Development Tools Can Be Used for 80C186EA System Development**
    - **ASM86 Assembler, iC-86, Pascal-86, Fortran-86, PL/M-86 and System Utilities**
    - **In-Circuit-Emulator (ICE™-186)**
- **Operation Includes Numerics Mode for Direct Interface to 80C187 Numerics Coprocessor**
- **Available in the Following Packages:**
  - **68-Pin Plastic Leaded Chip Carrier (PLCC)**
  - **80-Pin EIAJ Quad Flat Pack (QFP)**

The 80C186EA is a CHMOS high integration embedded microprocessor. The 80C186EA includes all of the features of an "Enhanced Mode" 80C186 while adding the additional capabilities of Idle and Powerdown Modes. In Numerics Mode, the 80C186EA interfaces directly with an 80C187 Numerics Coprocessor.



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May 1992
Order Number: 272019-002

80C186EA20, 16, 12
16-Bit High Integration Embedded Processor

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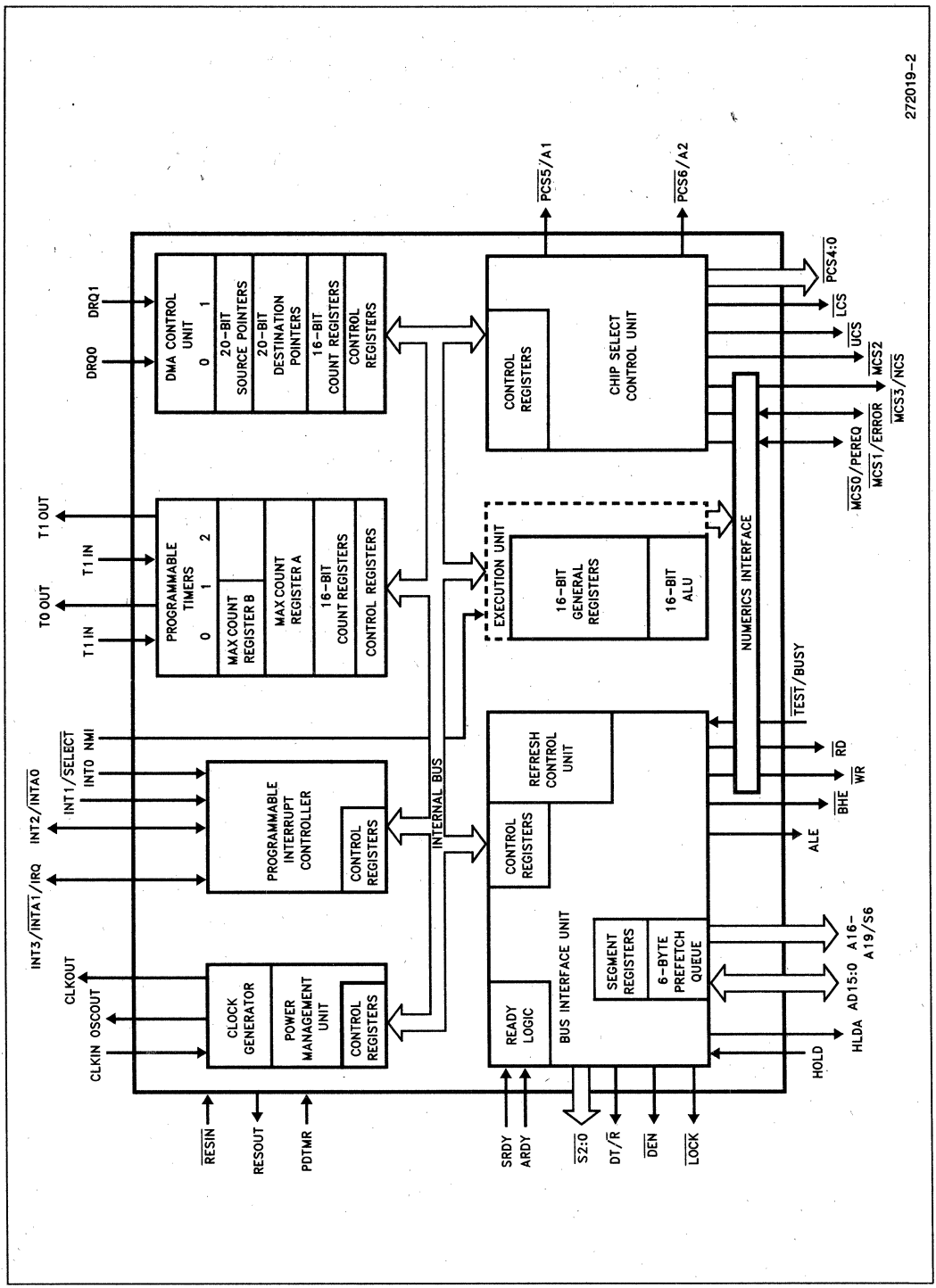


Figure 1. 80C186EA Block Diagram

INTRODUCTION

The 80C186EA is the second product in a new generation of low-power, high-integration microprocessors. It enhances the existing 80C186 family by offering new features and new operating modes. The 80C186EA is object code compatible with the 80C186/80C188 embedded processor.

The feature set of the 80C186EA meets the needs of low-power, space-critical applications. Low-power applications benefit from the static design of the CPU core and the integrated peripherals. Minimum current consumption is achieved by providing a Powerdown Mode that halts operation of the device, and freezes the clock circuits. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space-critical applications benefit from the integration of commonly used system peripherals. Two flexible DMA channels perform CPU-independent data transfers. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 128 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters round out the feature set of the 80C186EA.

OVERVIEW

Figure 1 shows a block diagram of the 80C186EA. The Execution Unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instructions, and static operation. The Bus Interface Unit (BIU) is the same as that found on the original 80C186 family products. An independent internal bus is used to allow communication between the BIU and internal peripherals.

80C186EA CORE ARCHITECTURE

Bus Interface Unit

The 80C186EA core incorporates a bus controller that generates local bus control signals. In addition, it employs a HOLD/HLDA protocol to share the local bus with other bus masters.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information and data (for write operations) information. It is also responsible for reading data off the local bus during a read operation. SRDY and ARDY input pins are provided to extend a bus cycle beyond the minimum four states (clocks).

The 80C186EA local bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the mulitplexed address/data bus.

Clock Generator

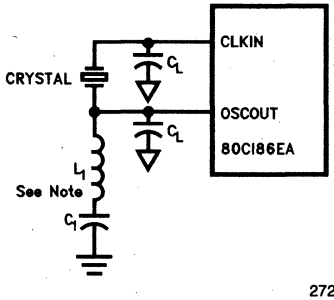
The 80C186EA provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, and two low-power operating modes.

The oscillator circuit is designed to be used with either a **parallel resonant** fundamental or third-overtone mode crystal network. Alternatively, the oscillator circuit may be driven from an external clock source. Figure 2 shows the various operating modes of the 80C186EA oscillator circuit.

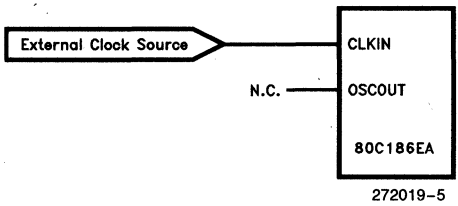
The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide-by-two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.

The following parameters are recommended when choosing a crystal:

Temperature Range:	Application Specific
ESR (Equivalent Series Resistance):	60Ω max
C0 (Shunt Capacitance of Crystal):	7.0 pF max
C_L (Load Capacitance):	20 pF ± 5 pF
Drive Level:	2 mW max



(A) Crystal Connection



(B) Clock Connection

NOTE:
The L_1C_1 network is **only** required when using a third-overtone crystal.

Figure 2. 80C186EA Clock Configurations

80C186EA PERIPHERAL ARCHITECTURE

The 80C186EA has integrated several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexible and provide logical interconnections between supporting units (e.g., the interrupt control unit supports interrupt requests from the timer/counters or DMA channels).

The list of integrated peripherals include:

- 4-Input Interrupt Control Unit
- 3-Channel Timer/Counter Unit
- 2-Channel DMA Unit
- 13-Output Chip-Select Unit
- Refresh Control Unit
- Power Management logic

The registers associated with each integrated peripheral are contained within a 128 x 16 register file called the Peripheral Control Block (PCB). The PCB can be located in either memory or I/O space on any 256 byte address boundary.

Figure 3 provides a list of the registers associated with the PCB when the processor's Interrupt Control Unit is in Master Mode. In Slave Mode, the definitions of some registers change. Figure 4 provides register definitions specific to Slave Mode.

Interrupt Control Unit

The 80C186EA can receive interrupts from a number of sources, both internal and external. The Interrupt Control Unit (ICU) serves to merge these requests on a priority basis, for individual service by the CPU. Each interrupt source can be independently masked by the Interrupt Control Unit or all interrupts can be globally masked by the CPU.

Internal interrupt sources include the Timers and DMA channels. External interrupt sources come from the four input pins INT3:0. The NMI interrupt pin is not controlled by the ICU and is passed directly to the CPU. Although the timers only have one request input to the ICU, separate vector types are generated to service individual interrupts within the Timer Unit.

Timer/Counter Unit

The 80C186EA Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms, generate timed interrupts, etc.

PCB Offset	Function
00H	Reserved
02H	Reserved
04H	Reserved
06H	Reserved
08H	Reserved
0AH	Reserved
0CH	Reserved
0EH	Reserved
10H	Reserved
12H	Reserved
14H	Reserved
16H	Reserved
18H	Reserved
1AH	Reserved
1CH	Reserved
1EH	Reserved
20H	Reserved
22H	End of Interrupt
24H	Poll
26H	Poll Status
28H	Interrupt Mask
2AH	Priority Mask
2CH	In-Service
2EH	Interrupt Request
30H	Interrupt Status
32H	Timer Control
34H	DMA0 Int. Control
36H	DMA1 Int. Control
38H	INT0 Control
3AH	INT1 Control
3CH	INT2 Control
3EH	INT3 Control

PCB Offset	Function
40H	Reserved
42H	Reserved
44H	Reserved
46H	Reserved
48H	Reserved
4AH	Reserved
4CH	Reserved
4EH	Reserved
50H	Timer 0 Count
52H	Timer 0 Compare A
54H	Timer 0 Compare B
56H	Timer 0 Control
58H	Timer 1 Count
5AH	Timer 1 Compare A
5CH	Timer 1 Compare B
5EH	Timer 1 Control
60H	Timer 2 Count
62H	Timer 2 Compare
64H	Reserved
66H	Timer 2 Control
68H	Reserved
6AH	Reserved
6CH	Reserved
6EH	Reserved
70H	Reserved
72H	Reserved
74H	Reserved
76H	Reserved
78H	Reserved
7AH	Reserved
7CH	Reserved
7EH	Reserved

PCB Offset	Function
80H	Reserved
82H	Reserved
84H	Reserved
86H	Reserved
88H	Reserved
8AH	Reserved
8CH	Reserved
8EH	Reserved
90H	Reserved
92H	Reserved
94H	Reserved
96H	Reserved
98H	Reserved
9AH	Reserved
9CH	Reserved
9EH	Reserved
A0H	UMCS
A2H	LMCS
A4H	PACS
A6H	MMCS
A8H	MPCS
AAH	Reserved
ACH	Reserved
AEH	Reserved
B0H	Reserved
B2H	Reserved
B4H	Reserved
B6H	Reserved
B8H	Reserved
BAH	Reserved
BCH	Reserved
BEH	Reserved

PCB Offset	Function
C0H	DMA0 Src. Lo
C2H	DMA0 Src. Hi
C4H	DMA0 Dest. Lo
C6H	DMA0 Dest. Hi
C8H	DMA0 Count
CAH	DMA0 Control
CCH	Reserved
CEH	Reserved
D0H	DMA1 Src. Lo
D2H	DMA1 Src. Hi
D4H	DMA1 Dest. Lo
D6H	DMA1 Dest. Hi
D8H	DMA1 Count
DAH	DMA1 Control
DCH	Reserved
DEH	Reserved
E0H	Refresh Base
E2H	Refresh Time
E4H	Refresh Control
E6H	Reserved
E8H	Reserved
EAH	Reserved
ECH	Reserved
EEH	Reserved
F0H	Power-Save
F2H	Power Control
F4H	Reserved
F6H	Step ID
F8H	Reserved
FAH	Reserved
FCH	Reserved
FEH	Relocation

Figure 3. 80C186EA Peripheral Control Block Registers

PCB Offset	Function
20H	Interrupt Vector
22H	Specific EOI
24H	Reserved
26H	Reserved
28H	Interrupt Mask
2AH	Priority Mask
2C	In-Service
2E	Interrupt Request
30	Interrupt Status
32	TMR0 Interrupt Control
34	DMA0 Interrupt Control
36	DMA1 Interrupt Control
38	TMR1 Interrupt Control
3A	TMR2 Interrupt Control
3C	Reserved
3E	Reserved

Figure 4. 80C186EA Slave Mode Peripheral Control Block Registers

DMA Control Unit

The 80C186EA DMA Contol Unit provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O space in any combination: memory to memory, memory to I/O, I/O to I/O or I/O to memory. Data can be transferred either in bytes or words. Transfers may proceed to or from either even or odd addresses, but even-aligned word transfers proceed at a faster rate. Each data transfer consumes two bus cycles (a minimum of eight clocks), one cycle to fetch data and the other to store data. The chip-select/ready logic may be programmed to point to the memory or I/O space subject to DMA transfers in order to provide hardware chip select lines. DMA cycles run at higher priority than general processor execution cycles.

Chip-Select Unit

The 80C186EA Chip-Select Unit integrates logic which provides up to 13 programmable chip-selects to access both memories and peripherals. In addition, each chip-select can be programmed to automatically terminate a bus cycle independent of the condition of the SRDY and ARDY input pins. The chip-select lines are available for all memory and I/O bus cycles, whether they are generated by the CPU, the DMA unit, or the Refresh Control Unit.

Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 9-bit address generator is maintained by the RCU with the address presented on the A9:1 address lines during the refresh bus cycle. Address bits A19:13 are programmable to allow the refresh address block to be located on any 8 Kbyte boundary.

Power Management

The 80C186EA has three operational modes to control the power consumption of the device. They are Power Save Mode, Idle Mode, and Powerdown Mode.

Power Save Mode divides the processor clock by a programmable value to take advantage of the fact that current is linearly proportional to frequency. An unmasked interrupt, NMI, or reset will cause the 80C186EA to exit Power Save Mode.

Idle Mode freezes the clocks of the Execution Unit and the Bus Interface Unit at a logic zero state while all peripherals operate normally.

Powerdown Mode freezes all internal clocks at a logic zero level and disables the crystal oscillator. All internal registers hold their values provided V_{CC} is maintained. Current consumption is reduced to transistor leakage only.

80C187 Interface

The 80C187 Numerics Coprocessor may be used to extend the 80C186EA instruction set to include floating point and advanced integer instructions. Connecting the 80C186EA RESOUT and $\overline{TEST}$/BUSY pins to the 80C187 enables Numerics Mode operation. In Numerics Mode, three of the four Mid-Range Chip Select ($\overline{MCS}$) pins become handshaking pins for the interface. The exchange of data and control information proceeds through four dedicated I/O ports.

If an 80C187 is not present, the 80C186EA configures itself for regular operation at reset.

ONCE™ Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C186EA has a test mode available which forces all output and input/output pins to be placed in the high-impedance state. ONCE stands for "ON Circuit Emulation". The ONCE mode is selected by forcing the $\overline{UCS}$ and $\overline{LCS}$ pins LOW (0) during a processor reset (these pins are weakly held to a HIGH (1) level) while $\overline{RESIN}$ is active.

DIFFERENCES BETWEEN THE 80C186 AND THE 80C186EA

The 80C186EA is intended as a direct functional upgrade for 80C186 designs. In many cases, it will be possible to replace an existing 80C186 with little or no hardware redesign. The following sections describe differences in pinout, operating modes, and AC and DC specifications to keep in mind.

Pinout Compatibility

The 80C186EA requires a PDTMR pin to time the processor's exit from Powerdown Mode. The original pin arrangement for the 80C186 in the PLCC package did not have any spare leads to use for PDTMR, so the DT/$\overline{R}$ pin was sacrificed. The arrangement of all the other leads in the 68-lead PLCC is identical between the 80C186 and the 80C186EA. DT/$\overline{R}$ may be readily synthesized by latching the $\overline{S1}$ status output. Therefore, upgrading a PLCC 80C186 to PLCC 80C186EA is particularly straightforward. You must connect a capacitor to the 80C186EA PDTMR pin in order to use Powerdown Mode.

The 80-lead QFP (EIAJ) pinouts are distinctly different between the 80C186 and the 80C186EA. In addition to the PDTMR pin, the 80C186EA has more power and ground pins and the overall arrangement of pins was shifted. A new circuit board layout for the 80C186EA is required.

Operating Modes

The 80C186 has two operating modes, Compatible and Enhanced. Compatible Mode is a pin-to-pin replacement for the NMOS 80186, except for numerics coprocessing. In Enhanced Mode, the processor has a Refresh Control Unit, the Power-Save feature and an interface to the 80C187 Numerics Coprocessor. The $\overline{MCS0}$, $\overline{MCS1}$, and $\overline{MCS3}$ pins change their functions to constitute handshaking pins for the 80C187.

The 80C186EA allows all non-80C187 users to use all the $\overline{MCS}$ pins for chip-selects. In regular operation, all 80C186EA features (including those of the Enhanced Mode 80C186) are present except for the interface to the 80C187. Numerics Mode disables the three chip-select pins and reconfigures them for connection to the 80C187.

TTL vs CMOS Inputs

The inputs of the 80C186EA are rated for CMOS switching levels for improved noise immunity, but the 80C186 inputs are rated for TTL switching levels. In particular, the 80C186EA requires a minimum V_{IH} of 3.5V to recognize a logic one while the 80C186 requires a minimum V_{IH} of only 1.9V (assuming 5.0V operation). The solution is to drive the 80C186EA with true CMOS devices, such as those from the HC and AC logic families, or to use pullup resistors where the added current draw is not a problem.

Timing Specifications

80C186EA timing relationships are expressed in a simplified format over the 80C186. The AC performance of an 80C186EA at a specified frequency will be very close to that of an 80C186 at the same frequency. Check the timings applicable to your design prior to replacing the 80C186.

PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the 80C186EA in the Plastic Leaded Chip Carrier (PLCC) package and Quad Flat Pack (QFP) package. For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

Pin Descriptions

Each pin or logical set of pins is described in Table 2. There are three columns for each entry in the Pin Description Table.

The **Pin Name** column contains a mnemonic that describes the pin function. Negation of the signal name (for example, $\overline{\text{RESIN}}$) denotes a signal that is active low.

The **Pin Type** column contains two kinds of information. The first symbol indicates whether a pin is power (P), ground (G), input only (I), output only (O) or input/output (I/O). Some pins have multiplexed functions (for example, A19/S6). Additional symbols indicate additional characteristics for each pin. Table 1 lists all the possible symbols for this column.

Input pins may be either synchronous or asynchronous. Asynchronous pins require that setup and hold times be met only in order to guarantee *recognition* at a particular clock edge. Synchronous pins require that setup and hold times be met to guarantee proper *operation.* For example, missing the setup or hold time for the SRDY pin (a synchronous input) will result in a system failure or lockup. Input pins may also be edge- or level-sensitive. The possible characteristics for input pins are S(E), S(L), A(E) and A(L).

Output states are dependent upon the current activity of the processor. There are four operational states that are different from regular operation: bus hold, reset, Idle Mode and Powerdown Mode. Appropriate characteristics for these states are also indicated in this column, with the legend for all possible characteristics in Table 1.

Finally, the **Pin Description** column contains a text description of each pin.

As an example, consider AD15:0. I/O signifies the pins are bidirectional. S(L) signifies that the input function is synchronous and level-sensitive. H(Z) signifies that, as outputs, the pins are high-impedance upon acknowledgement of bus hold. R(Z) signifies that the pins float during reset. P(X) signifies that the pins retain their states during Powerdown Mode.

Table 1. Pin Description Nomenclature

Symbol	Description
P	Power Pin (Apply + V_{CC} Voltage)
G	Ground (Connect to V_{SS})
I	Input Only Pin
O	Output Only Pin
I/O	Input/Output Pin
S(E)	Synchronous, Edge Sensitive
S(L)	Synchronous, Level Sensitive
A(E)	Asynchronous, Edge Sensitive
A(L)	Asynchronous, Level Sensitive
H(1)	Output Driven to V_{CC} during Bus Hold
H(0)	Output Driven to V_{SS} during Bus Hold
H(Z)	Output Floats during Bus Hold
H(Q)	Output Remains Active during Bus Hold
H(X)	Output Retains Current State during Bus Hold
R(WH)	Output Weakly Held at V_{CC} during Reset
R(1)	Output Driven to V_{CC} during Reset
R(0)	Output Driven to V_{SS} during Reset
R(Z)	Output Floats during Reset
R(Q)	Output Remains Active during Reset
R(X)	Output Retains Current State during Reset
I(1)	Output Driven to V_{CC} during Idle Mode
I(0)	Output Driven to V_{SS} during Idle Mode
I(Z)	Output Floats during Idle Mode
I(Q)	Output Remains Active during Idle Mode
I(X)	Output Retains Current State during Idle Mode
P(1)	Output Driven to V_{CC} during Powerdown Mode
P(0)	Output Driven to V_{SS} during Powerdown Mode
P(Z)	Output Floats during Powerdown Mode
P(Q)	Output Remains Active during Powerdown Mode
P(X)	Output Retains Current State during Powerdown Mode

Table 2. 80C186EA Pin Descriptions

Name	Type	Description
V_{CC}	P	**POWER** connections consist of six pins which must be shorted externally to a V_{CC} board plane.
V_{SS}	G	**GROUND** connections consist of five pins which must be shorted externally to a V_{SS} board plane.
CLKIN	I A(E)	**CLocK INput** is an input for an external clock. An external oscillator operating at two times the required 80C186EA operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O H(Q) R(Q) P(Q)	**OSCillator OUTput** is only used when using a crystal to generate the external clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin is not to be used as 2X clock output for non-crystal applications (i.e., this pin is N.C. for non-crystal applications). OSCOUT does not float in ONCE mode.
CLKOUT	O H(Q) R(Q) P(Q)	**CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transistions every falling edge of CLKIN.
$\overline{\text{RESIN}}$	I A(L)	**RESet IN** causes the 80C186EA to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the 80C186EA begins fetching opcodes at memory location 0FFFF0H.
RESOUT	O H(0) R(1) P(0)	**RESet OUTput** that indicates the 80C186EA is currently in the reset state. RESOUT will remain active as long as $\overline{\text{RESIN}}$ remains active. When tied to the $\overline{\text{TEST}}$/BUSY pin, RESOUT forces the 80C186EA into Numerics Mode.
PDTMR	I/O A(L) H(WH) R(Z) P(1)	**Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the 80C186EA waits after an exit from power down before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I A(E)	**Non-Maskable Interrupt** input causes a Type 2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{\text{TEST}}$/BUSY	I A(E)	**$\overline{\text{TEST}}$/BUSY** is sampled upon reset to determine whether the 80C186EA is to enter Numerics Mode. In regular operation, the pin is **$\overline{\text{TEST}}$.** $\overline{\text{TEST}}$ is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (low). In Numerics Mode, the pin is **BUSY**. BUSY notifies the 80C186EA of 80C187 Numerics Coprocessor activity.
AD15:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed **Address** and **Data** bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle.
A18:16 A19/S6	H(Z) R(Z) P(X)	These pins provide multiplexed **Address** during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. A18:16 are driven to a logic 0 during the data phase of the bus cycle. Also during the data phase, S6 is driven to a logic 0 to indicate a CPU-initiated bus cycle or logic 1 to indicate a DMA-initiated bus cycle or a refresh cycle.

Table 2. 80C186EA Pin Descriptions (Continued)

Name	Type	Description
$\overline{S2:0}$	O H(Z) R(Z) P(1)	Bus cycle **Status** are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ Bus Cycle Initiated 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive (no bus activity)
ALE/QS0	O H(0) R(0) P(0)	**Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle. In Queue Status Mode, QS0 provides queue status information along with QS1.
$\overline{BHE}$	O H(Z) R(Z) P(X)	**Byte High Enable** output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. $\overline{BHE}$ and A0 have the following logical encoding: A0 $\overline{BHE}$ Encoding 0 0 Word Transfer 0 1 Even Byte Transfer 1 0 Odd Byte Transfer 1 1 Refresh Operation
$\overline{RD}/\overline{QSMD}$	I/O H(Z) R(WH) P(1)	**ReaD** output signals that the accessed memory or I/O device must drive data information onto the data bus. Upon reset, this pin has an alternate function. As $\overline{QSMD}$, it enables **Queue Status Mode** when grounded. In Queue Status Mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide the following information about processor/instruction queue interaction: QS1 QS0 Queue Operation 0 0 No Queue Operation 0 1 First Opcode Byte Fetched from the Queue 1 1 Subsequent Byte Fetched from the Queue 1 0 Empty the Queue
$\overline{WR}$/QS1	O H(Z) R(Z) P(1)	**WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device. In Queue Status Mode, QS1 provides queue status information along with QS0.
ARDY	I A(L) S(L)	**Asychronous ReaDY** is an input to signal for the end of a bus cycle. ARDY is asynchronous on rising CLKOUT and synchronous on falling CLKOUT. ARDY or SRDY must be active to terminate any 80C186EA bus cycle, unless they are ignored due to correct programming of the Chip Select Unit.
SRDY	I S(L)	**Synchronous ReaDY** is an input to signal for the end of a bus cycle. ARDY or SRDY must be active to terminate any 80C186EA bus cycle, unless they are ignored due to correct programming of the Chip Select Unit.
$\overline{DEN}$	O H(Z) R(Z) P(1)	**Data ENable** output to control the enable of bidirectional transceivers when buffering an 80C186EA system. $\overline{DEN}$ is active only when data is to be transferred on the bus.

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Table 2. 80C186EA Pin Descriptions (Continued)

Name	Type	Description
DT/$\overline{R}$	O H(Z) R(Z) P(X)	**Data Transmit/Receive** output controls the direction of a bi-directional buffer when buffering an 80C186EA system. DT/$\overline{R}$ is only available for the QFP (EIAJ) package (S80C186EA).
$\overline{LOCK}$	I/O H(Z) R(WH) P(1)	**LOCK** output indicates that the bus cycle in progress is not to be interrupted. The 80C186EA will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low.
HOLD	I A(L)	**HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The 80C186EA will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
HLDA	O H(1) R(0) P(0)	**HoLD Acknowledge** output to indicate that the 80C186EA has relinquish control of the local bus. When HLDA is asserted, the 80C186EA will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly.
$\overline{UCS}$	O H(1) R(1) P(1)	**Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH. During a processor reset, $\overline{UCS}$ and $\overline{LCS}$ are used to enable ONCE Mode.
$\overline{LCS}$	O H(1) R(1) P(1)	**Lower Chip Select** will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. $\overline{LCS}$ is inactive after a reset. During a processor reset, $\overline{UCS}$ and $\overline{LCS}$ are used to enable ONCE Mode.
$\overline{MCS0}$/PEREQ $\overline{MCS1}$/$\overline{ERROR}$ $\overline{MCS2}$ $\overline{MCS3}$/$\overline{NCS}$	I/O H(1) R(1) P(1) A(L)	These pins provide a multiplexed function. If enabled, these pins normally comprise a block of **Mid-Range Chip Select** outputs which will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. In Numerics Mode, three of the pins become handshaking pins for the 80C187. The **CoProcessor REQuest** input signals that a data transfer is pending. **$\overline{ERROR}$** is an input which indicates that the previous numerics coprocessor operation resulted in an exception condition. An interrupt Type 16 is generated when $\overline{ERROR}$ is sampled active at the beginning of a numerics operation. **Numerics Coprocessor Select** is an output signal generated when the processor accesses the 80C187.
$\overline{PCS4:0}$	O H(1) R(1) P(1)	**Peripheral Chip Selects** go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user.
$\overline{PCS5}$/A1 $\overline{PCS6}$/A2	0 H(1)/H(X) R(1) P(1)	These pins provide a multiplexed function. As additional **Peripheral Chip Selects,** they go active whenever the address of a memory or I/O bus cycle is within the address limitations by the user. They may also be programmed to provide latched **Address** A2:1 signals.
T0OUT T1OUT	O H(Q) R(1) P(Q)	**Timer OUTput** pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.
T0IN T1IN	I A(L) A(E)	**Timer INput** is used either as clock or control signals, depending on the timer mode selected.

Table 2. 80C186EA Pin Descriptions (Continued)

Name	Type	Description
DRQ0 DRQ1	I A(L)	**DMA ReQuest** is asserted by an external request when it is prepared for a DMA transfer.
INT0 INT1/$\overline{\text{SELECT}}$	I A(E,L)	Maskable **INTerrupt** input will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with $\overline{\text{INTA0}}$ and $\overline{\text{INTA1}}$ to interface with an external slave controller. INT1 becomes $\overline{\text{SELECT}}$ when the ICU is configured for Slave Mode.
INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$/IRQ	I/O A(E,L) /H(1) R(Z) /P(1)	These pins provide multiplexed functions. As inputs, they provide a maskable **INTerrupt** that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an **INTerrupt Acknowledge** handshake signal to allow interrupt expansion. INT3/$\overline{\text{INTA1}}$ becomes **IRQ** when the ICU is configured for Slave Mode.
N.C.	—	**No Connect.** For compatibility with future products, do not connect to these pins.

80C186EA PINOUT

Tables 3 and 4 list the 80C186EA pin names with package location for the 68-pin Plastic Leaded Chip Carrier (PLCC) component. Figure 9 depicts the complete 80C186EA pinout (PLCC package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 5 and 6 list the 80C186EA pin names with package location for the 80-pin Quad Flat Pack (EIAJ) component. Figure 6 depicts the complete 80C186EA (EIAJ QFP package) as viewed from the top side of the component (i.e., contacts facing down).

Table 3. PLCC Pin Names with Package Location

Address/Data Bus	
Name	**Location**
AD0	17
AD1	15
AD2	13
AD3	11
AD4	8
AD5	6
AD6	4
AD7	2
AD8	16
AD9	14
AD10	12
AD11	10
AD12	7
AD13	5
AD14	3
AD15	1
A16	68
A17	67
A18	66
A19/S6	65

Bus Control	
Name	**Location**
ALE/QS0	61
$\overline{\text{BHE}}$	64
$\overline{\text{S0}}$	52
$\overline{\text{S1}}$	53
$\overline{\text{S2}}$	54
$\overline{\text{RD}}$/$\overline{\text{QSMD}}$	62
$\overline{\text{WR}}$/QS1	63
ARDY	55
SRDY	49
$\overline{\text{DEN}}$	39
$\overline{\text{LOCK}}$	48
HOLD	50
HLDA	51

Power	
Name	**Location**
V_{SS}	26, 60
V_{CC}	9, 43

Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	24
RESOUT	57
CLKIN	59
OSCOUT	58
CLKOUT	56
$\overline{\text{TEST}}$/BUSY	47
PDTMR	40
NMI	46
INT0	45
INT1/SELECT	44
INT2/$\overline{\text{INTA0}}$	42
INT3/$\overline{\text{INTA1}}$/IRQ	41

I/O	
Name	**Location**
$\overline{\text{UCS}}$	34
$\overline{\text{LCS}}$	33
$\overline{\text{MCS0}}$/PEREQ	38
$\overline{\text{MCS1}}$/$\overline{\text{ERROR}}$	37
$\overline{\text{MCS2}}$	36
$\overline{\text{MCS3}}$/$\overline{\text{NCS}}$	35
$\overline{\text{PCS0}}$	25
$\overline{\text{PCS1}}$	27
$\overline{\text{PCS2}}$	28
$\overline{\text{PCS3}}$	29
$\overline{\text{PCS4}}$	30
$\overline{\text{PCS5}}$/A1	31
$\overline{\text{PCS6}}$/A2	32
T0OUT	22
T0IN	20
T1OUT	23
T1IN	21
DRQ0	18
DRQ1	19

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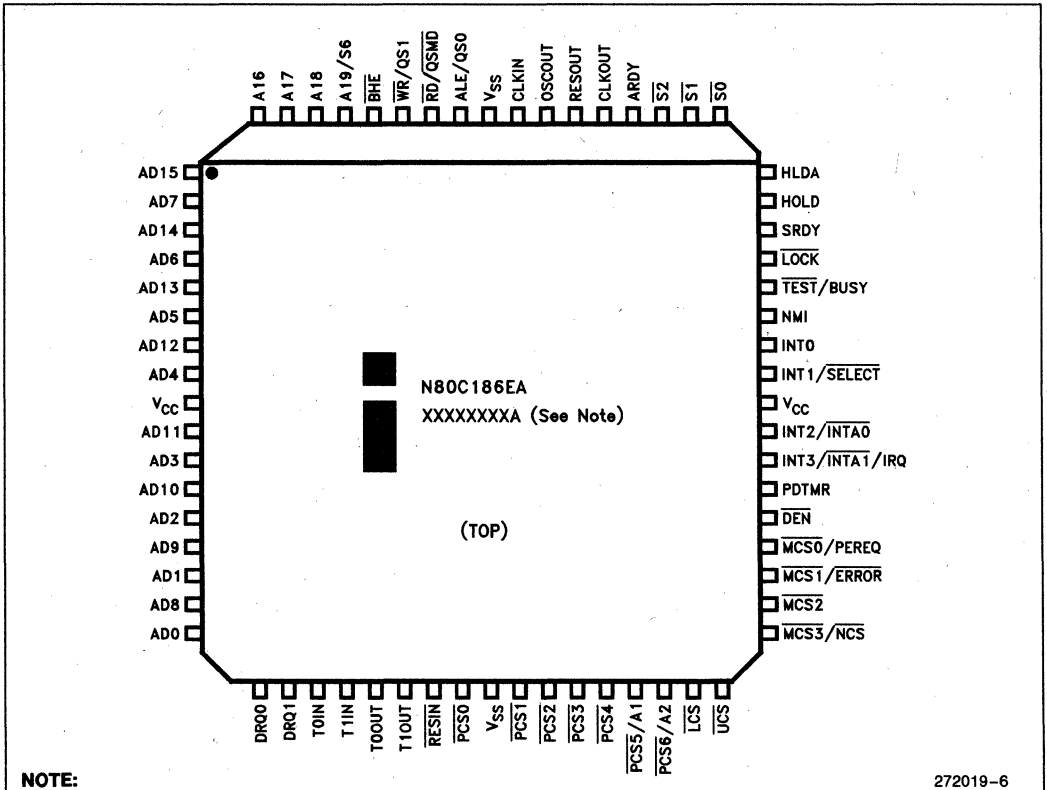
Table 4. PLCC Package Locations with Pin Name

Location	Name
1	AD15
2	AD7
3	AD14
4	AD6
5	AD13
6	AD5
7	AD12
8	AD4
9	V_{CC}
10	AD11
11	AD3
12	AD10
13	AD2
14	AD9
15	AD1
16	AD8
17	AD0

Location	Name
18	DRQ0
19	DRQ1
20	T0IN
21	T1IN
22	T0OUT
23	T1OUT
24	$\overline{RESIN}$
25	$\overline{PCS0}$
26	V_{SS}
27	$\overline{PCS1}$
28	$\overline{PCS2}$
29	$\overline{PCS3}$
30	$\overline{PCS4}$
31	$\overline{PCS5}$/A1
32	$\overline{PCS6}$/A2
33	$\overline{LCS}$
34	$\overline{UCS}$

Location	Name
35	$\overline{MCS3}/\overline{NCS}$
36	$\overline{MCS2}$
37	$\overline{MCS1}/\overline{ERROR}$
38	$\overline{MCS0}$/PEREQ
39	$\overline{DEN}$
40	PDTMR
41	INT3/$\overline{INTA1}$/ IRQ
42	INT2/$\overline{INTA0}$
43	V_{CC}
44	INT1/SELECT
45	INT0
46	NMI
47	$\overline{TEST}$/BUSY
48	LOCK
49	SRDY
50	HOLD
51	HLDA

Location	Name
52	$\overline{S0}$
53	$\overline{S1}$
54	$\overline{S2}$
55	ARDY
56	CLKOUT
57	RESOUT
58	OSCOUT
59	CLKIN
60	V_{SS}
61	ALE/QS0
62	$\overline{RD}/\overline{QSMD}$
63	$\overline{WR}$/QS1
64	$\overline{BHE}$
65	A19/S6
66	A18
67	A17
68	A16



NOTE:
The nine-character alphanumeric code (XXXXXXXXA) underneath the product number is the Intel FPO number.

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Figure 5. 68-Lead PLCC Pinout Diagram

Table 5. QFP (EIAJ) Pin Name with Package Location

Address/Data Bus	
Name	**Location**
AD0	64
AD1	66
AD2	68
AD3	70
AD4	74
AD5	76
AD6	78
AD7	80
AD8	65
AD9	67
AD10	69
AD11	71
AD12	75
AD13	77
AD14	79
AD15	1
A16	3
A17	4
A18	5
A19/S6	6

Bus Control	
Name	**Location**
ALE/QS0	10
$\overline{BHE}$	7
$\overline{S0}$	23
$\overline{S1}$	22
$\overline{S2}$	21
$\overline{RD}/\overline{QSMD}$	9
$\overline{WR}$/QS1	8
ARDY	20
SRDY	27
DT/$\overline{R}$	37
$\overline{DEN}$	39
$\overline{LOCK}$	28
HOLD	26
HLDA	25

Power	
Name	**Location**
V_{SS}	12, 13, 24, 53, 62
V_{CC}	2, 33, 34, 44, 72, 73

Processor Control	
Name	**Location**
$\overline{RESIN}$	55
RESOUT	18
CLKIN	16
OSCOUT	17
CLKOUT	19
$\overline{TEST}$/BUSY	29
PDTMR	38
NMI	30
INT0	31
INT1/$\overline{SELECT}$	32
INT2/$\overline{INTA0}$	35
INT3/$\overline{INTA1}$/ IRQ	36
N.C.	11, 14, 15, 63

I/O	
Name	**Location**
$\overline{UCS}$	45
$\overline{LCS}$	46
$\overline{MCS0}$/PEREQ	40
$\overline{MCS1}$/$\overline{ERROR}$	41
$\overline{MCS2}$	42
$\overline{MCS3}$/$\overline{NCS}$	43
$\overline{PCS0}$	54
$\overline{PCS1}$	52
$\overline{PCS2}$	51
$\overline{PCS3}$	50
$\overline{PCS4}$	49
$\overline{PCS5}$/A1	48
$\overline{PCS6}$/A2	47
T0OUT	57
T0IN	59
T1OUT	56
T1IN	58
DRQ0	61
DRQ1	60

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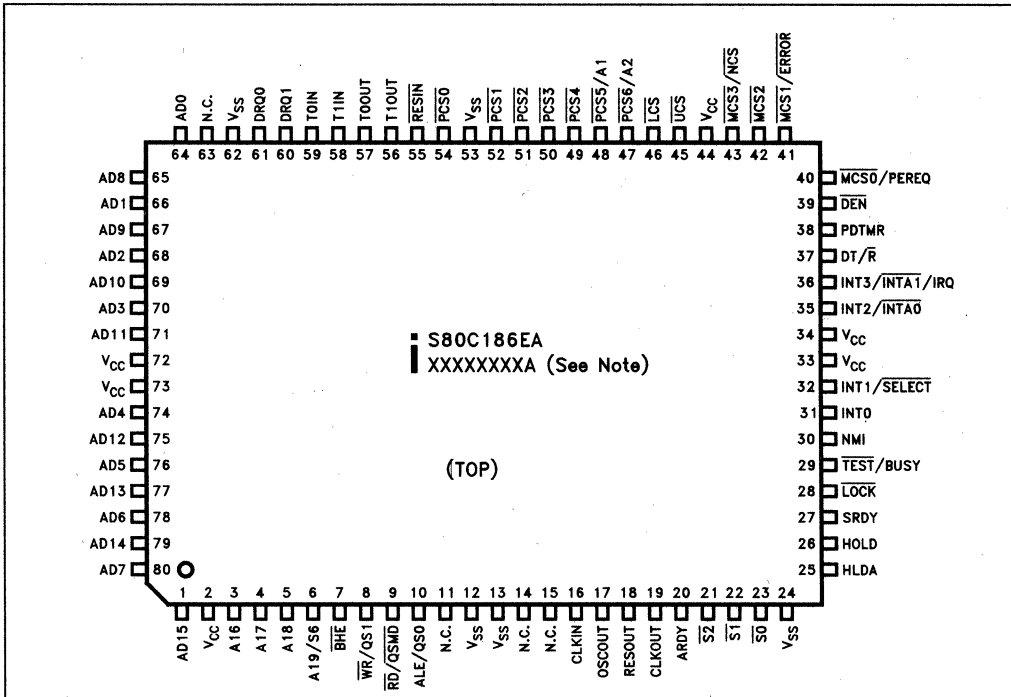
Table 6. QFP (EIAJ) Package Location with Pin Names

Location	Name	Location	Name	Location	Name	Location	Name
1	AD15	21	$\overline{S2}$	41	$\overline{MCS1}$/$\overline{ERROR}$	61	DRQ0
2	V_{CC}	22	$\overline{S1}$	42	$\overline{MCS2}$	62	V_{SS}
3	A16	23	$\overline{S0}$	43	$\overline{MCS3}$/$\overline{NCS}$	63	N.C.
4	A17	24	V_{SS}	44	V_{CC}	64	AD0
5	A18	25	HLDA	45	$\overline{UCS}$	65	AD8
6	A19/S6	26	HOLD	46	$\overline{LCS}$	66	AD1
7	$\overline{BHE}$	27	SRDY	47	$\overline{PCS6}$/A2	67	AD9
8	$\overline{WR}$/QS1	28	$\overline{LOCK}$	48	$\overline{PCS5}$/A1	68	AD2
9	$\overline{RD}$/$\overline{QSMD}$	29	$\overline{TEST}$/BUSY	49	$\overline{PCS4}$	69	AD10
10	ALE/QS0	30	NMI	50	$\overline{PCS3}$	70	AD3
11	N.C.	31	INT0	51	$\overline{PCS2}$	71	AD11
12	V_{SS}	32	INT1/$\overline{SELECT}$	52	$\overline{PCS1}$	72	V_{CC}
13	V_{SS}	33	V_{CC}	53	V_{SS}	73	V_{CC}
14	N.C.	34	V_{CC}	54	$\overline{PCS0}$	74	AD4
15	N.C.	35	INT2/$\overline{INTA0}$	55	$\overline{RESIN}$	75	AD12
16	CLKIN	36	INT3/$\overline{INTA1}$/	56	T1OUT	76	AD5
17	OSCOUT		IRQ	57	T0OUT	77	AD13
18	RESOUT	37	DT/$\overline{R}$	58	T1IN	78	AD6
19	CLKOUT	38	PDTMR	59	T0IN	79	AD14
20	ARDY	39	$\overline{DEN}$	60	DRQ1	80	AD7
		40	$\overline{MCS0}$/PEREQ				



NOTE:
The nine-character alphanumeric code (XXXXXXXXA) underneath the product number is the Intel FPO number.

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Figure 6. Quad Flat Pack (EIAJ) Pinout Diagram

PACKAGE THERMAL SPECIFICATIONS

The 80C186EA is specified for operation when T_C (the case temperature) is within the range of 0°C to 85°C (PLCC package) or 0°C to 106°C (QFP-EIAJ) package. T_C may be measured in any environment to determine whether the 80C186EA is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P \times \theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 7 for the 68-pin Plastic Leaded Chip Carrier (PLCC) package.

Table 8 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies. P (the maximum power consumption, specified in watts) is calculated by using the maximum ICC as tabulated in the DC specifications and V_{CC} of 5.5V.

Table 7. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow Linear ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PLCC)	29	25	21	19	17	16.5
θ_{CA} (QFP)	66	63	60.5	59	58	57

Table 8. Maximum T_A at Various Airflows (in °C)

		Airflow Linear ft/min (m/sec)					
	T_F (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A (PLCC)	25	78	80	81	82	82.5	83
	32	74	76	78	79	79.5	80
	40	70	72	74	75	76	76.5
T_A (QFP)	25	84	85.5	86	87	87	87.5
	32	77.5	79	80	80.5	81	81.5
	40	70	71.5	73	74	74	75

ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

Absolute Maximum Ratings*

Storage Temperature ..... −65°C to +150°C

Case Temperature under Bias ... −65°C to +150°C

Supply Voltage with Respect to V_{SS} ..... −0.5V to +6.5V

Voltage on Other Pins with Respect to V_{SS} ..... −0.5V to V_{CC} + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.5	5.5	V
T_F	Input Clock Frequency			
	80C186EA20	0	40	MHz
	80C186EA16	0	32	MHz
	80C186EA12	0	25	MHz
T_C	Case Temperature under Bias			
	N80C186EA (PLCC)	0	+100	°C
	S80C186EA (QFP)	0	+114	°C

Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80C186EA based circuit board should contain separate power (V_{CC}) and ground (V_{SS}) planes. All V_{CC} and V_{SS} pins **must** be connected to the appropriate plane. Pins identified as "N.C." must not be connected in the system. Decoupling capacitors should be placed near the 80C186EA. The value and type of decoupling capacitors is application and board layout dependent. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Always connect any unused input pins to an appropriate signal level. In particular, unused interrupt pins (NMI, INT3:0) should be connected to V_{SS} to avoid unwanted interrupts. **Leave any unused output pin or any "N.C." pin unconnected.**

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage for All Pins	−0.5	0.3 V_{CC}	V	
V_{IH}	Input High Voltage for All Pins	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 3 mA (min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −2 mA (min)
V_{HYR}	Input Hysterisis on $\overline{RESIN}$	0.30		V	
I_{IL1}	Input Leakage Current (except $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$, $\overline{LOCK}$ and $\overline{TEST}$/BUSY)		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{IL2}	Input Leakage Current ($\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$, $\overline{ERROR}$, $\overline{LOCK}$ and $\overline{TEST}$/BUSY	−275		μA	V_{IN} = 0.7 V_{CC} (Note 1)
I_{OL}	Output Leakage Current		±10	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 2)
I_{CC}	Supply Current Cold (RESET) 80C186EA20 80C186EA16 80C186EA12		 100 80 62.5	 mA mA mA	(Note 3)
I_{ID}	Supply Current In Idle Mode 80C186EA20 80C186EA16 80C186EA12		 70 56 44	 mA mA mA	
I_{PD}	Supply Current In Powerdown Mode 80C186EA20 80C186EA16 80C186EA12		 100 100 100	 μA μA μA	
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 4)
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz

NOTES:
1. $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$, $\overline{LOCK}$ and $\overline{TEST}$/BUSY have internal pullups that are only activated during RESET. Loading these pins above I_{OL} = −275 μA will cause the 80C186EA to enter alternate modes of operation.
2. Output pins are floated using HOLD or ONCE Mode.
3. Measured at worst case temperature and V_{CC} with all outputs loaded as specified in the AC Test Conditions, and with the device in RESET ($\overline{RESIN}$ held low). RESET is worst case for I_{CC}.
4. Output capacitance is the capacitive load of a floating output pin.

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I_{CC} VERSUS FREQUENCY AND VOLTAGE

The current (I_{CC}) consumption of the 80C186EA is essentially composed of two components; I_{PD} and I_{CCS}.

I_{PD} is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or V_{CC} (no clock applied to the device). I_{PD} is equal to the Powerdown current and is typically less than 50 μA.

I_{CCS} is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since I_{CCS} is typically much greater than I_{PD}, I_{PD} can often be ignored when calculating I_{CC}.

I_{CCS} is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: V = Device operating voltage (V_{CC})

C_{DEV} = Device capacitance

f = Device operating frequency

I_{CCS} = I_{CC} = Device current

Measuring C_{DEV} on a device like the 80C186EA would be difficult. Instead, C_{DEV} is calculated using the above formula by measuring I_{CC} at a known V_{CC} and frequency (see Table 9). Using this C_{DEV} value, I_{CC} can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical I_{CC} when operating at 20 MHz, 4.8V.

$$I_{CC} = I_{CCS} = 4.8 \times 0.515 \times 20 \approx 49 \text{ mA}$$

PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: t = desired delay in **seconds**

C_{PD} = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132$ μF is required. Round up to standard (available) capacitive values.

NOTE:
The above equation applies to delay times greater than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperature will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

Table 9. C_{DEV} Values

Parameter	Typ	Max	Units	Notes
C_{DEV} (Device in Reset)	0.515	0.905	mA/V*MHz	1, 2
C_{DEV} (Device in Idle)	0.391	0.635	mA/V*MHz	1, 2

1. Max C_{DEV} is calculated at −40°C, all floating outputs driven to V_{CC} or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical C_{DEV} is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

AC SPECIFICATIONS

AC Characteristics—80C186EA20

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	40	MHz	1
T_C	CLKIN Period	25	∞	ns	1
T_{CH}	CLKIN High Time	10	∞	ns	1, 2
T_{CL}	CLKIN Low Time	10	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	17	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	22	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	3	27	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	22	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, AD15:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	3	27	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		ns	1, 9
T_{CLIS}	AD15:0, ARDY, SRDY, DRQ1:0	10		ns	1, 10
T_{CLIH}	AD15:0, ARDY, SRDY, DRQ1:0	3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, $\overline{ERROR}$	10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, $\overline{ERROR}$	3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	10		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (from CLKIN)	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 12 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 13 for rise and fall times outside 50 pF.
6. See Figure 13 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C186EA operation (SRDY, AD15:0).

AC SPECIFICATIONS (Continued)

AC Characteristics—80C186EA16

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	32	MHz	1
T_C	CLKIN Period	31.25	∞	ns	1
T_{CH}	CLKIN High Time	10	∞	ns	1, 2
T_{CL}	CLKIN Low Time	10	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	20	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	23	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	3	28	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	23	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, AD15:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	3	28	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		ns	1, 9
T_{CLIS}	AD15:0, ARDY, SRDY, DRQ1:0	10		ns	1, 10
T_{CLIH}	AD15:0, ARDY, SRDY, DRQ1:0	3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, $\overline{ERROR}$	10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, $\overline{ERROR}$	3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	10		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (from CLKIN)	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 12 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 13 for rise and fall times outside 50 pF.
6. See Figure 13 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C186EA operation (SRDY, AD15:0).

AC SPECIFICATIONS (Continued)

AC Characteristics—80C186EA12

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	25	MHz	1
T_C	CLKIN Period	40	∞	ns	1
T_{CH}	CLKIN High Time	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	23	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, S2:0, DEN, DT/R, BHE, LOCK, A19:16	3	25	ns	1, 4, 6, 7
T_{CHOV2}	MCS3:0, LCS, UCS, PCS6:0, NCS, RD, WR	3	30	ns	1, 4, 6, 8
T_{CLOV1}	BHE, DEN, LOCK, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	25	ns	1, 4, 6
T_{CLOV2}	RD, WR, MCS3:0, LCS, UCS, PCS6:0, AD15:0, NCS, INTA1:0, S2:0	3	30	ns	1, 4, 6
T_{CHOF}	RD, WR, BHE, DT/R, LOCK, S2:0, A19:16	0	25	ns	1
T_{CLOF}	DEN, AD15:0	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	TEST, NMI, INT3:0, T1:0IN, ARDY	10		ns	1, 9
T_{CHIH}	TEST, NMI, INT3:0, T1:0IN, ARDY	3		ns	1, 9
T_{CLIS}	AD15:0, ARDY, SRDY, DRQ1:0	10		ns	1, 10
T_{CLIH}	AD15:0, ARDY, SRDY, DRQ1:0	3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, ERROR	10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, ERROR	3		ns	1, 9
T_{CLIS}	RESIN (to CLKIN)	10		ns	1, 9
T_{CLIH}	RESIN (from CLKIN)	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 12 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 13 for rise and fall times outside 50 pF.
6. See Figure 13 for rise and fall times.
7. T_{CHOV1} applies to BHE, LOCK and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to RD and WR only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C186EA operation (SRDY, AD15:0).

AC SPECIFICATIONS (Continued)

Relative Timings (80C186EA20, 16, 12)

Symbol	Parameter	Min	Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Rising to ALE Falling	T − 15		ns	
T_{AVLL}	Address Valid to ALE Falling	½T − 10		ns	
T_{PLLL}	Chip Selects Valid to ALE Falling	½T − 10		ns	1
T_{LLAX}	Address Hold from ALE Falling	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{RHLH}	$\overline{RD}$ Rising to ALE Rising	½T − 10		ns	1
T_{WHLH}	$\overline{WR}$ Rising to ALE Rising	½T − 10		ns	1
T_{AFRL}	Address Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Falling to $\overline{RD}$ Rising	(2*T) − 5		ns	2
T_{WLWH}	$\overline{WR}$ Falling to $\overline{WR}$ Rising	(2*T) − 5		ns	2
T_{RHAV}	$\overline{RD}$ Rising to Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHDEX}	$\overline{WR}$ Rising to $\overline{DEN}$ Rising	½T − 10		ns	1
T_{WHPH}	$\overline{WR}$ Rising to Chip Select Rising	½T − 10		ns	1, 4
T_{RHPH}	$\overline{RD}$ Rising to Chip Select Rising	½T − 10		ns	1, 4
T_{PHPL}	$\overline{CS}$ Inactive to $\overline{CS}$ Active	½T − 10		ns	1
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		ns	5
T_{OVRH}	ONCE ($\overline{UCS}$, $\overline{LCS}$) Active to $\overline{RESIN}$ Rising	T		ns	3
T_{RHOX}	ONCE ($\overline{UCS}$, $\overline{LCS}$) to $\overline{RESIN}$ Rising	T		ns	3

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Not tested.
4. Not applicable to latched A2:1. These signals change only on falling T_1.
5. For write cycle followed by read cycle.

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 7. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

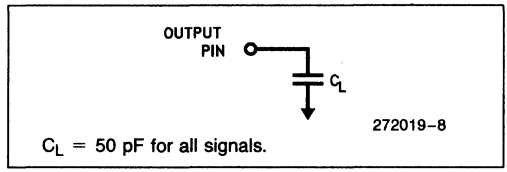

Figure 7. AC Test Load

AC TIMING WAVEFORMS

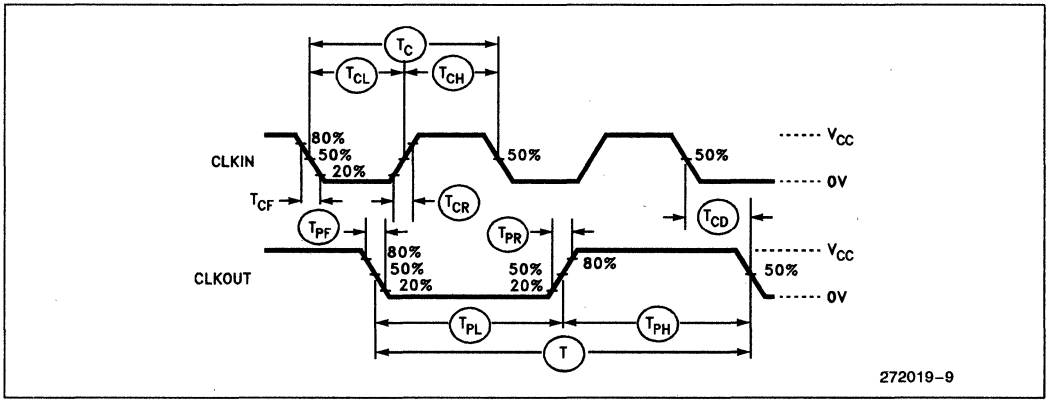

Figure 8. Input and Output Clock Waveform

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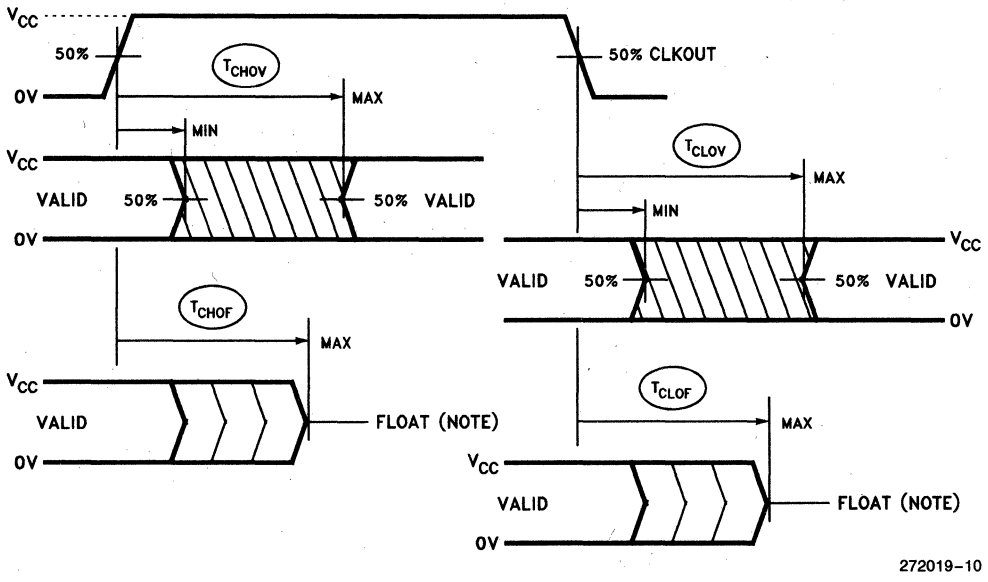
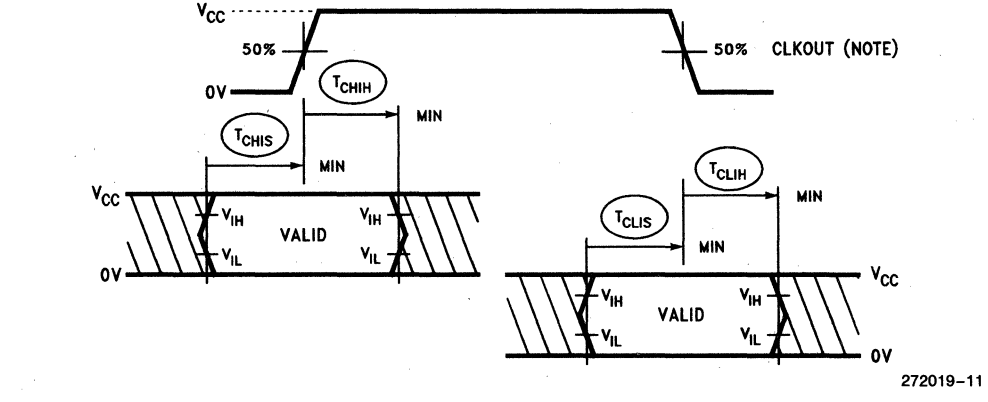


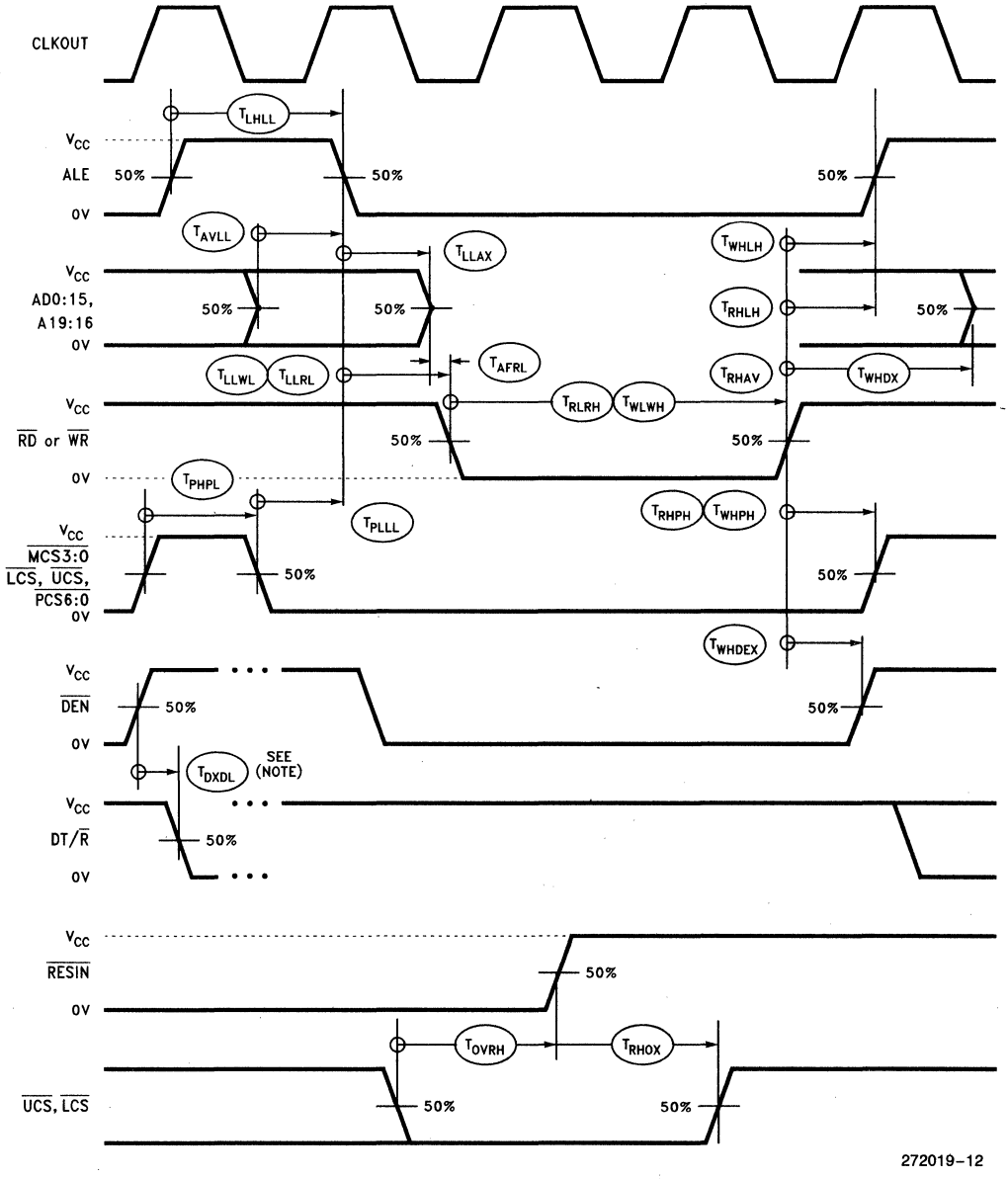
NOTE:
20% V_{CC} < Float < 80% V_{CC}

Figure 9. Output Delay and Float Waveform



NOTE:
$\overline{RESIN}$ measured to CLKIN, not CLKOUT

Figure 10. Input Setup and Hold



NOTE:
T_{DXDL} for write cycle followed by read cycle.

Figure 11. Relative Signal Waveform

DERATING CURVES

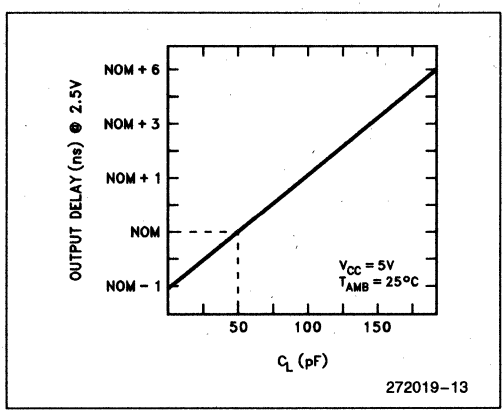


Figure 12. Typical Output Delay Variations Versus Load Capacitance

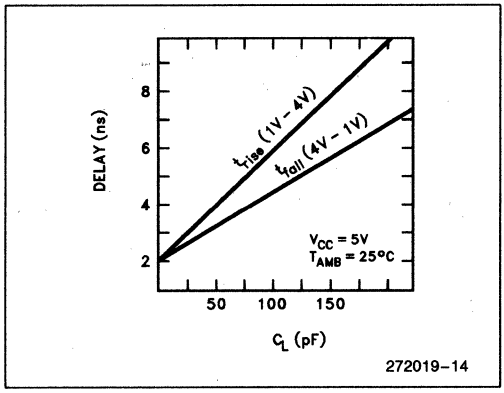


Figure 13. Typical Rise and Fall Variations Versus Load Capacitance

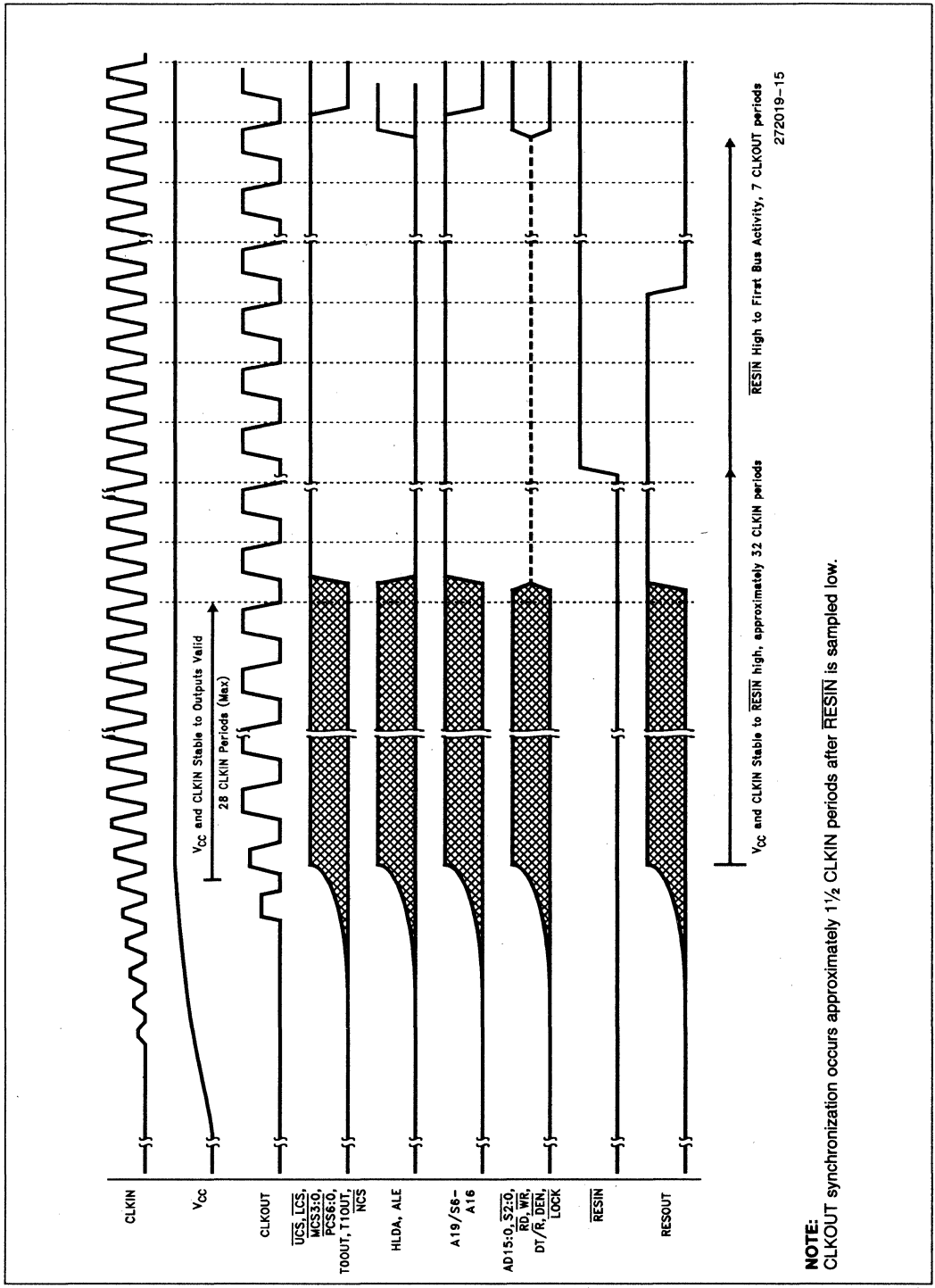
RESET

The 80C186EA will perform a reset operation any time the $\overline{RESIN}$ pin is active. The $\overline{RESIN}$ pin is actually synchronized before it is presented internally, which means that the clock must be operating before a reset can take effect. From a power-on state, $\overline{RESIN}$ must be held active (low) in order to guarantee correct initialization of the 80C186EA. **Failure to provide $\overline{RESIN}$ while the device is powering up will result in unspecified operation of the device.**

Figure 14 shows the correct reset sequence when first applying power to the 80C186EA. An external clock connected to CLKIN must not exceed the V_{CC} threshold being applied to the 80C186EA. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the 80C186EA. When attaching a crystal to the device, $\overline{RESIN}$ must remain active until both V_{CC} and CLKOUT are stable (the length of time is application specific and depends on the startup characteristics of the crystal circuit). The $\overline{RESIN}$ pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that $\overline{RESIN}$ is never really sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Figure 15 shows the timing sequence when $\overline{RESIN}$ is applied after V_{CC} is stable and the device has been operating. Note that a reset will terminate all activity and return the 80C186EA to a known operating state. Any bus operation that is in progress at the time $\overline{RESIN}$ is asserted will terminate immediately (note that most control signals will be driven to their inactive state first before floating).

While $\overline{RESIN}$ is active, signals $\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$, $\overline{LOCK}$, and $\overline{TEST}$/BUSY are configured as inputs and weakly held high by internal pullup transistors. Forcing $\overline{UCS}$ and $\overline{LCS}$ low selects ONCE Mode. Forcing $\overline{QSMD}$ low selects Queue Status Mode. Forcing $\overline{TEST}$/BUSY high at reset and low four clocks later enables Numerics Mode. Forcing $\overline{LOCK}$ low is prohibited and results in unspecified operation.



NOTE:
CLKOUT synchronization occurs approximately 1½ CLKIN periods after RESIN is sampled low.

Figure 14. 80C186EA Powerup Reset

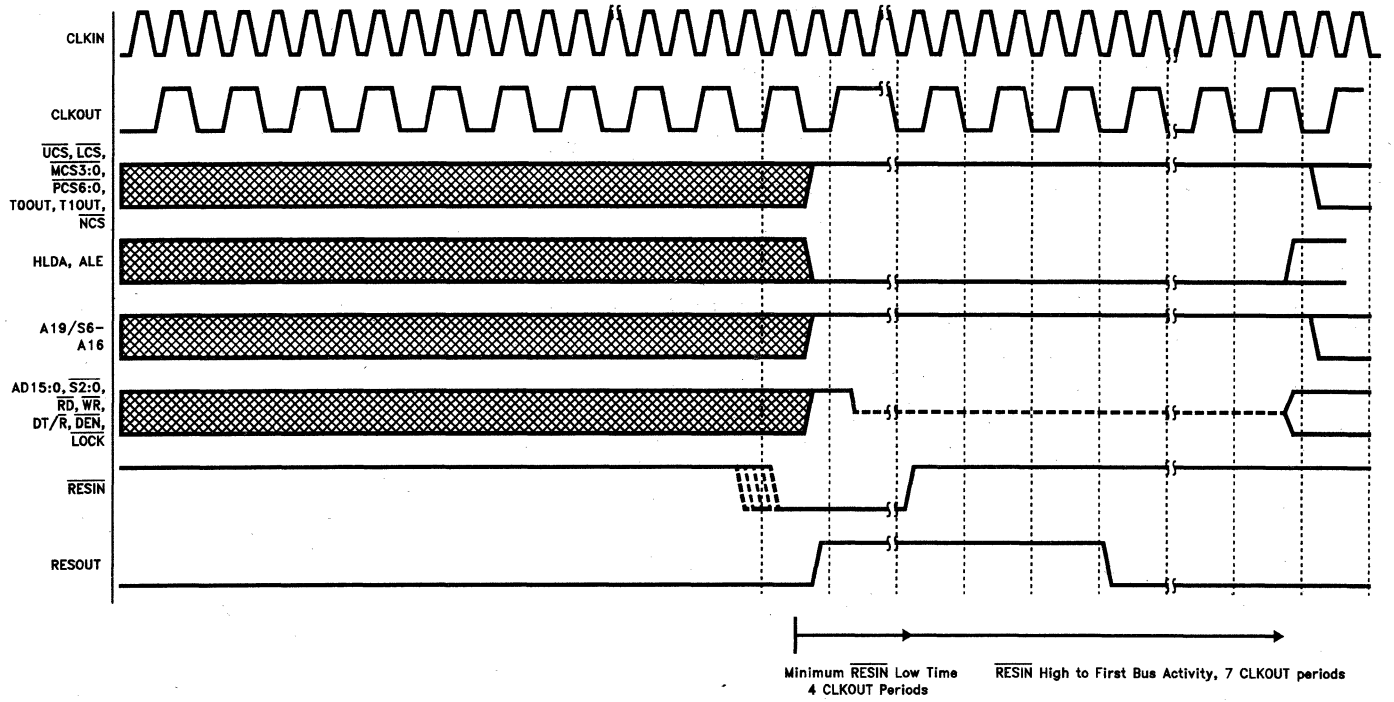
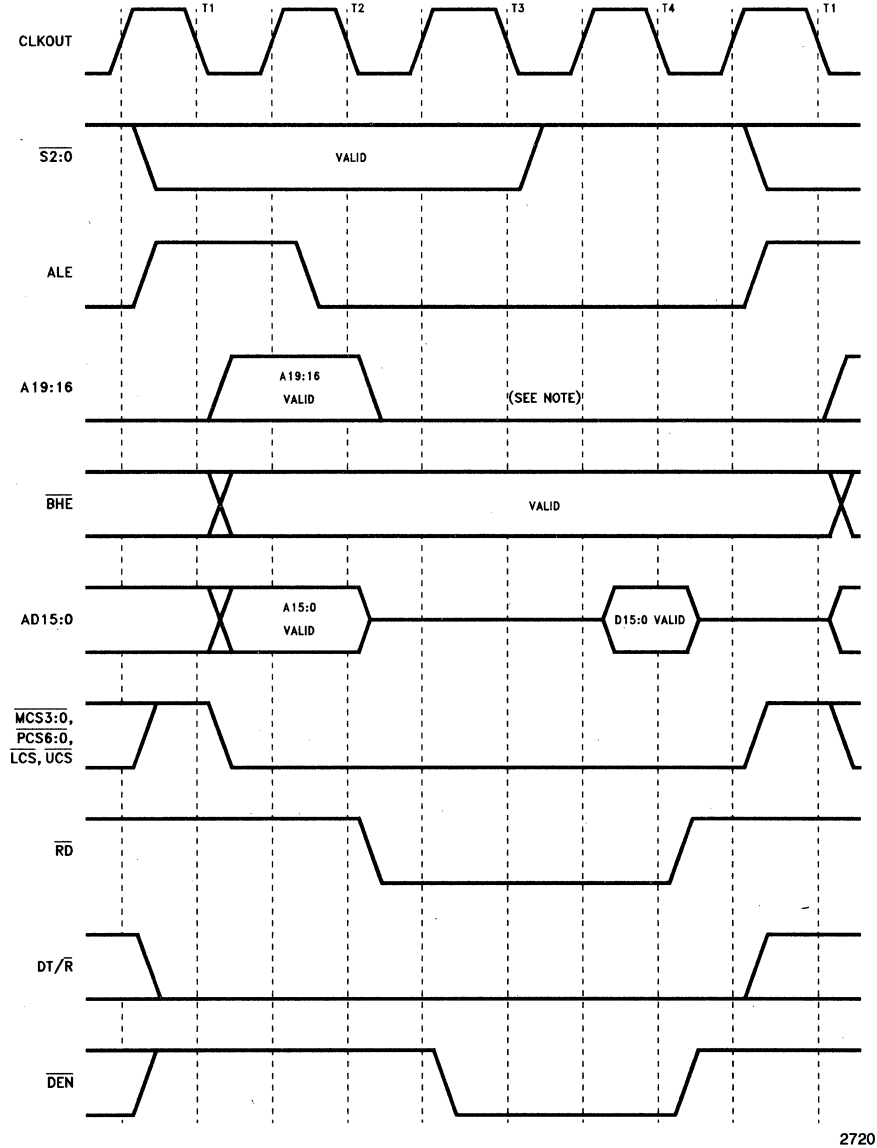


Figure 15. 80C186EA Warm Reset

NOTE:
CLKOUT resynchronization occurs approximately 1½ CLKIN periods after RESIN is sampled low. If RESIN is sampled low while CLKOUT is transitioning high, then CLKOUT will remain high for two CLKIN periods. If RESIN is sampled low while CLKOUT is transitioning high, then CLKOUT will not be affected.

BUS CYCLE WAVEFORMS

Figures 16 through 22 present the various bus cycles that are generated by the 80C186EA. What is shown in the figure is the relationship of the various bus signals to CLKOUT. These figures along with the information present in **AC Specifications** allow the user to determine all the critical timing analysis needed for a given application.



NOTE:
During the data phase of the bus cycle, A19/S6 is driven high for a DMA or refresh cycle.

Figure 16. Read, Fetch and Refresh Cycle Waveform

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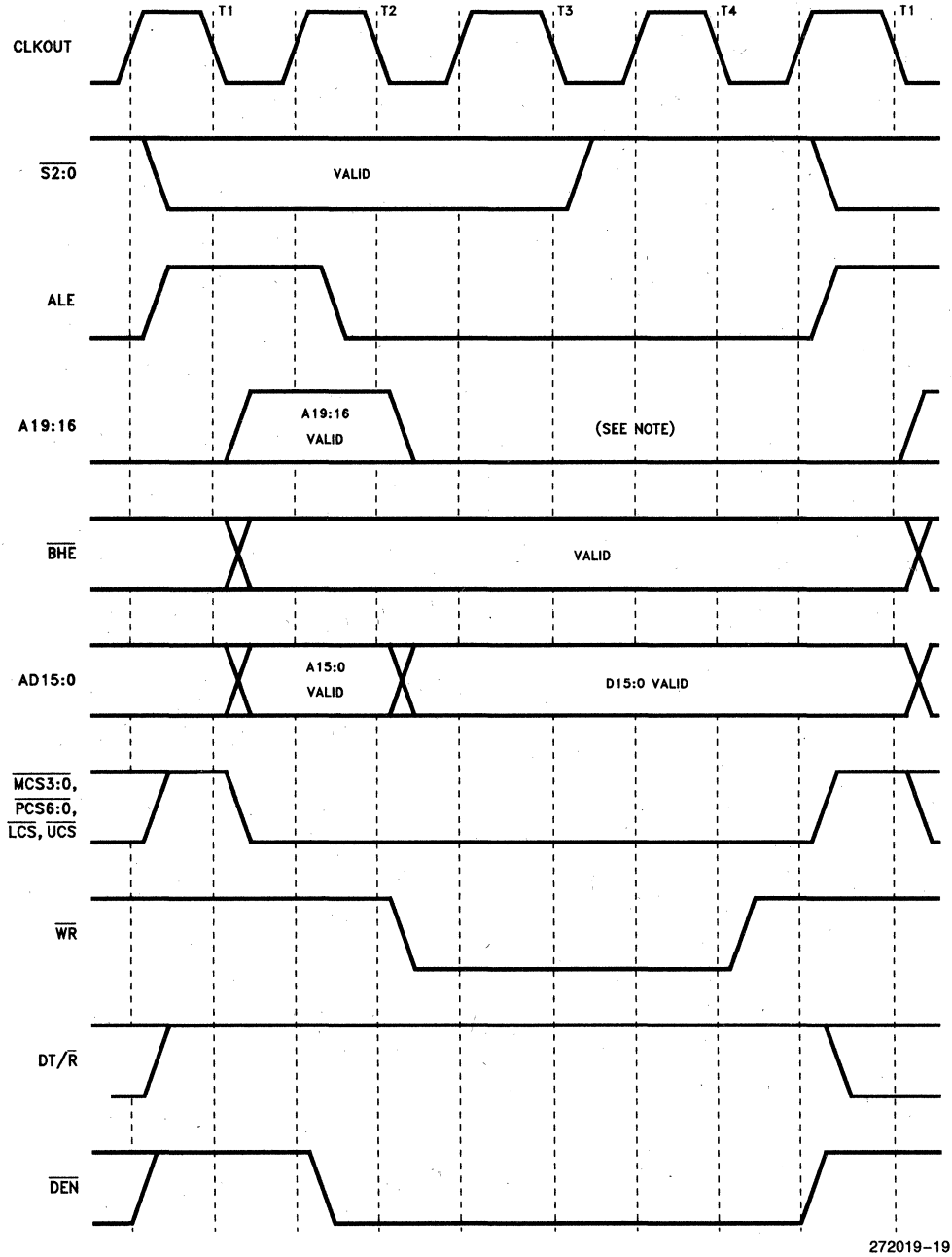
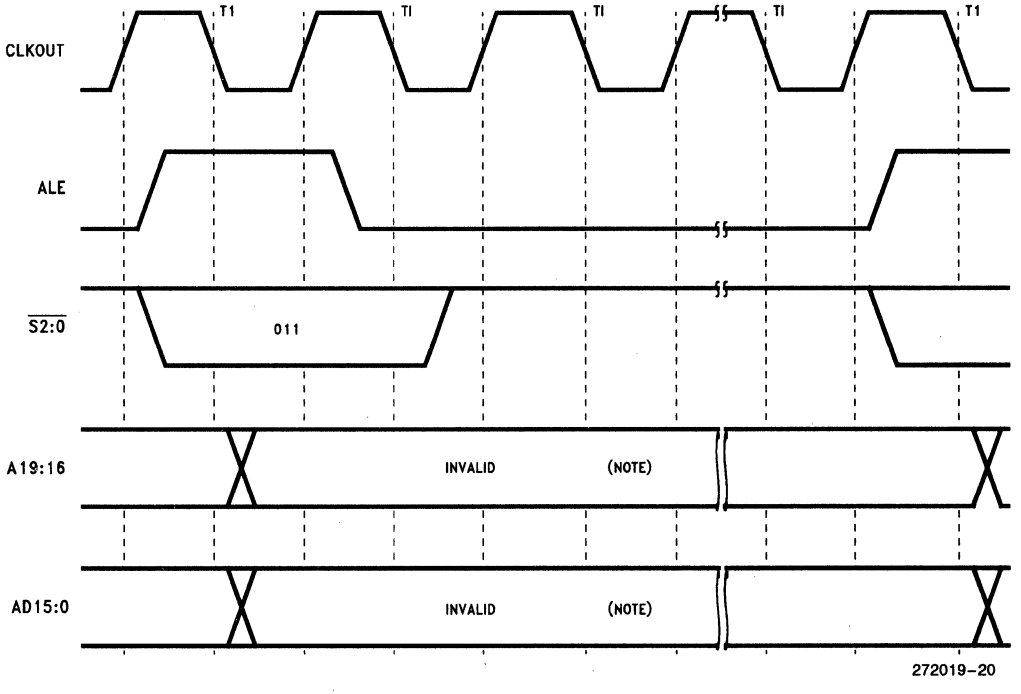


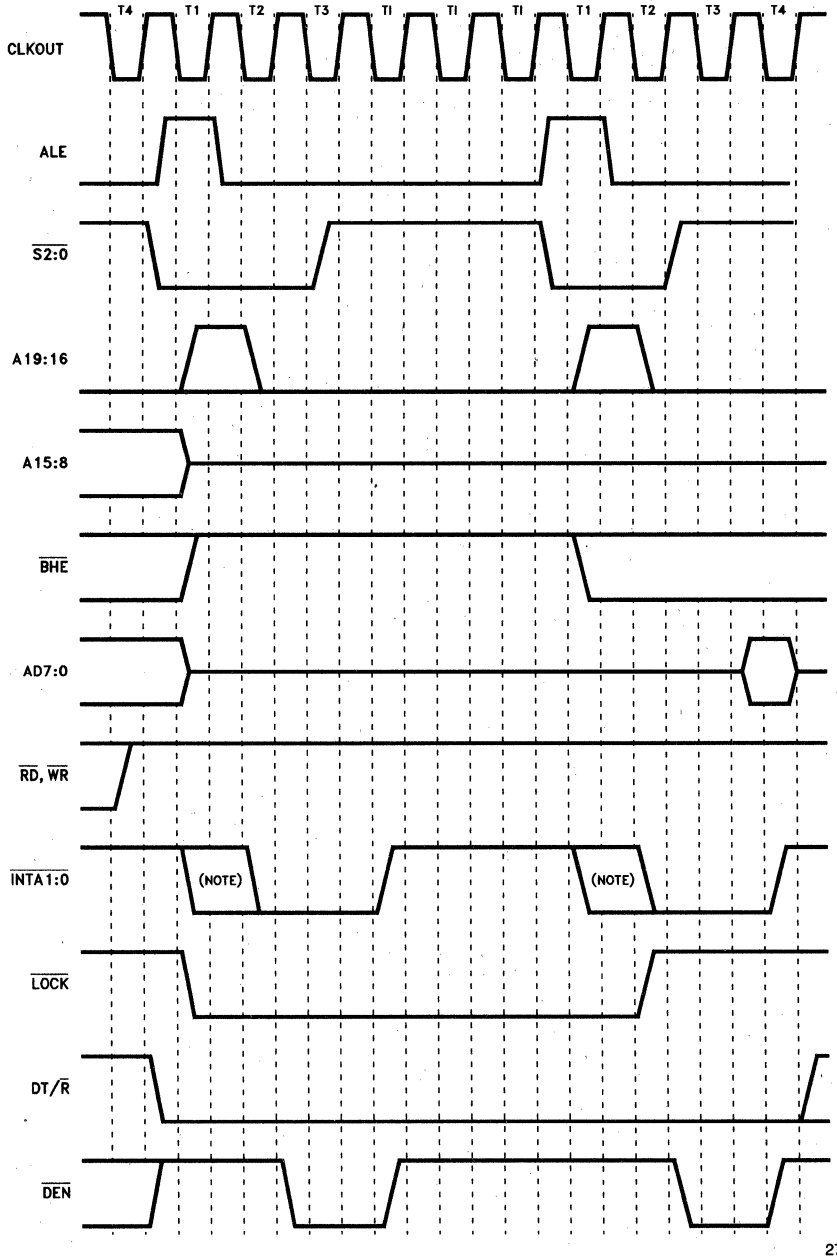
NOTE:
During the data phase of the bus cycle, A19/S6 is driven high for a DMA cycle.

Figure 17. Write Cycle Waveform



NOTE:
The 80C186EA drives these pins to 0 during Idle and Powerdown Modes.

Figure 18. Halt Cycle Waveform



NOTE:
INTA occurs one clock later in Slave Mode.

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Figure 19. INTA Cycle Waveform

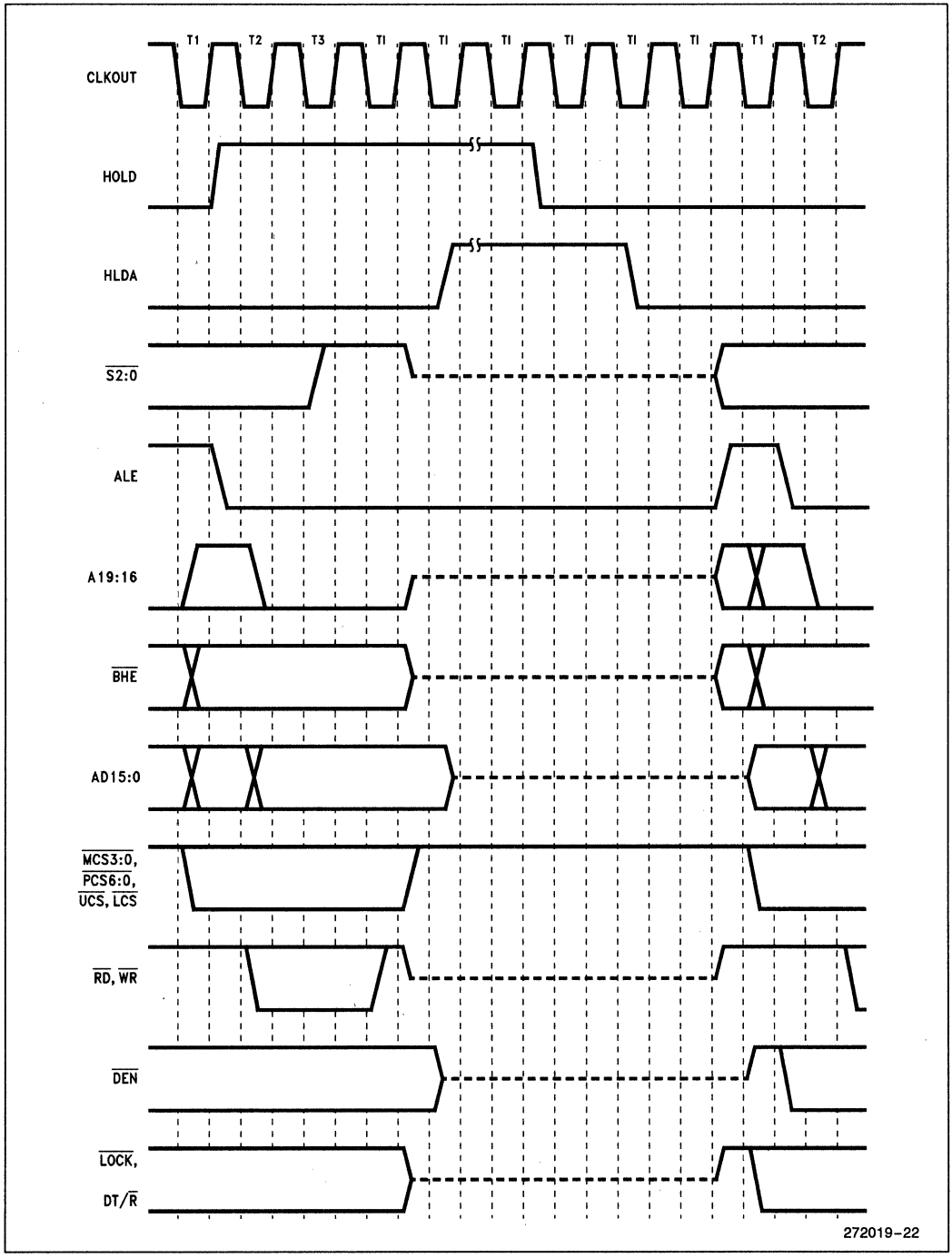


Figure 20. HOLD/HLDA Waveform

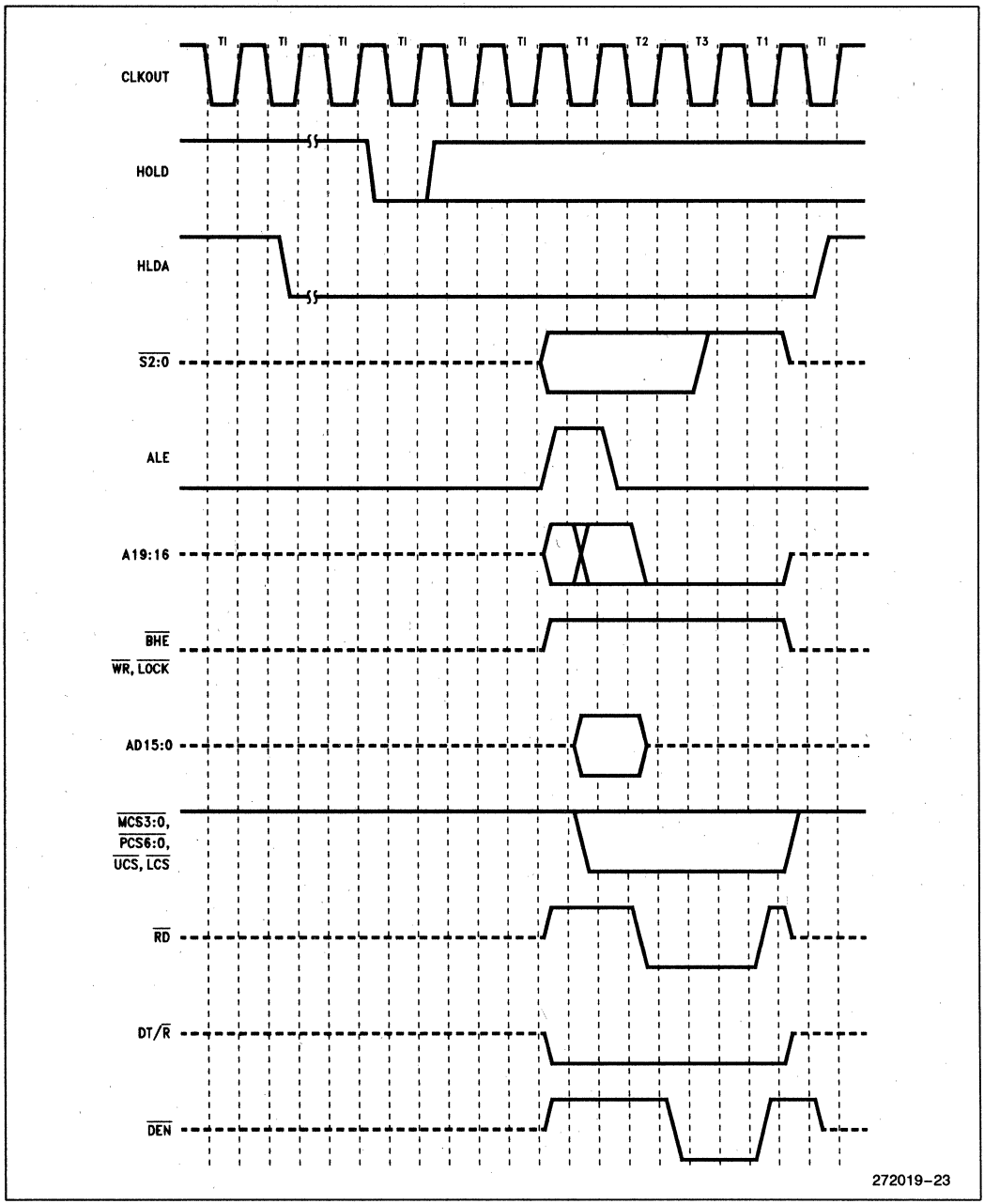
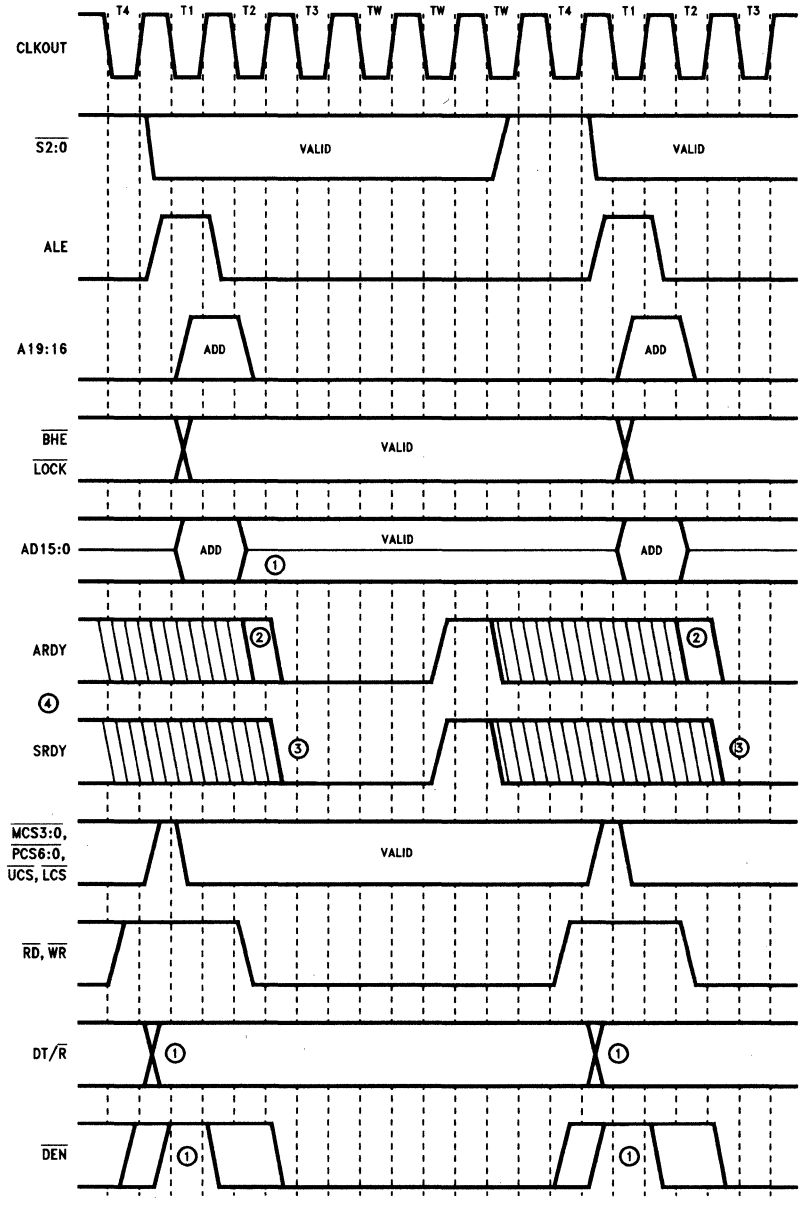


Figure 21. DRAM Refresh Cycle During Hold Acknowledge



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NOTES:
1. Generalized diagram for READ or WRITE.
2. ARDY low by either edge causes a wait state. Only rising ARDY is fully synchronized.
3. SRDY low causes a wait state. SRDY must meet setup and hold times to ensure correct device operation.
4. Either ARDY or SRDY active high will terminate a bus cycle.

Figure 22. Ready Waveform

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REGISTER BIT SUMMARY

Figures 23 through 30 present the bit definition of each register that is active (not reserved) in the Peripheral Control Block (PCB). Each register can be thought to occupy one word (16-bits) of either memory or I/O space, although not all bits in the register necessarily have a function. A register bit is **not** guaranteed to return a specific logic value if an "X" appears for the bit definition (i.e., if a zero was written to the register bit it may not be returned as a zero when read). Furthermore, a 0 must be written to any bit that is indicated by an "X" to ensure compatibility with future products or potential product changes.

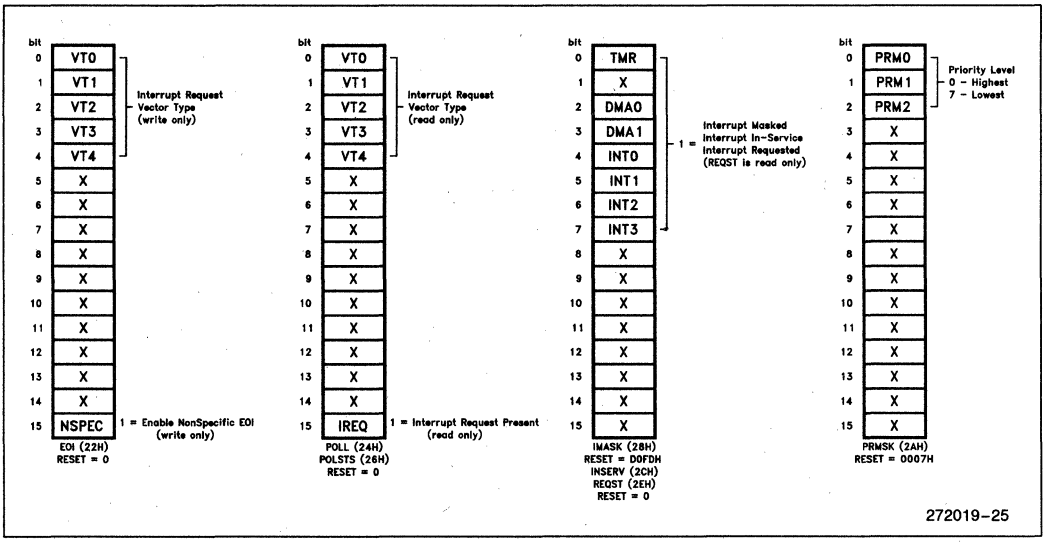

Figure 23. Interrupt Control Unit Registers (Master Mode)

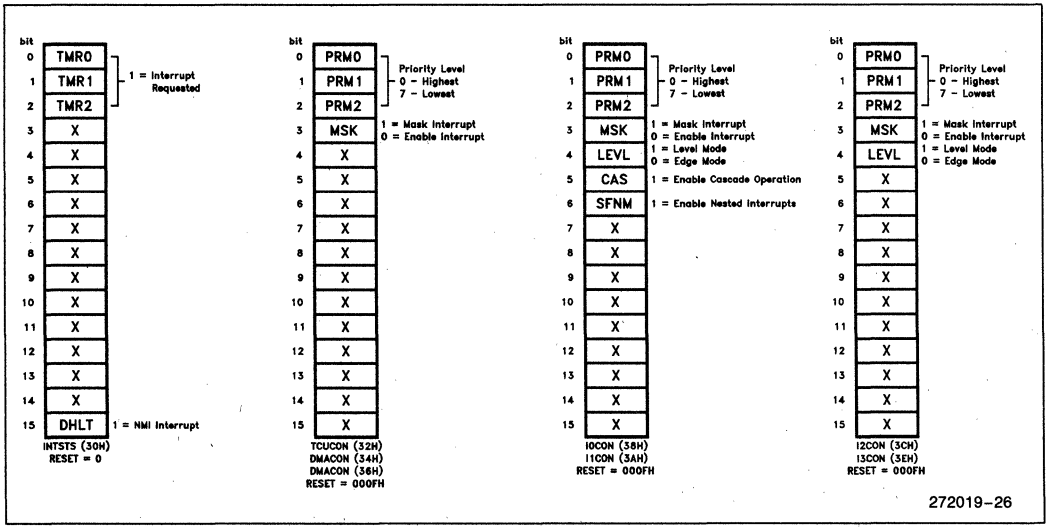

Figure 24. Interrupt Control Unit Registers (Master Mode)

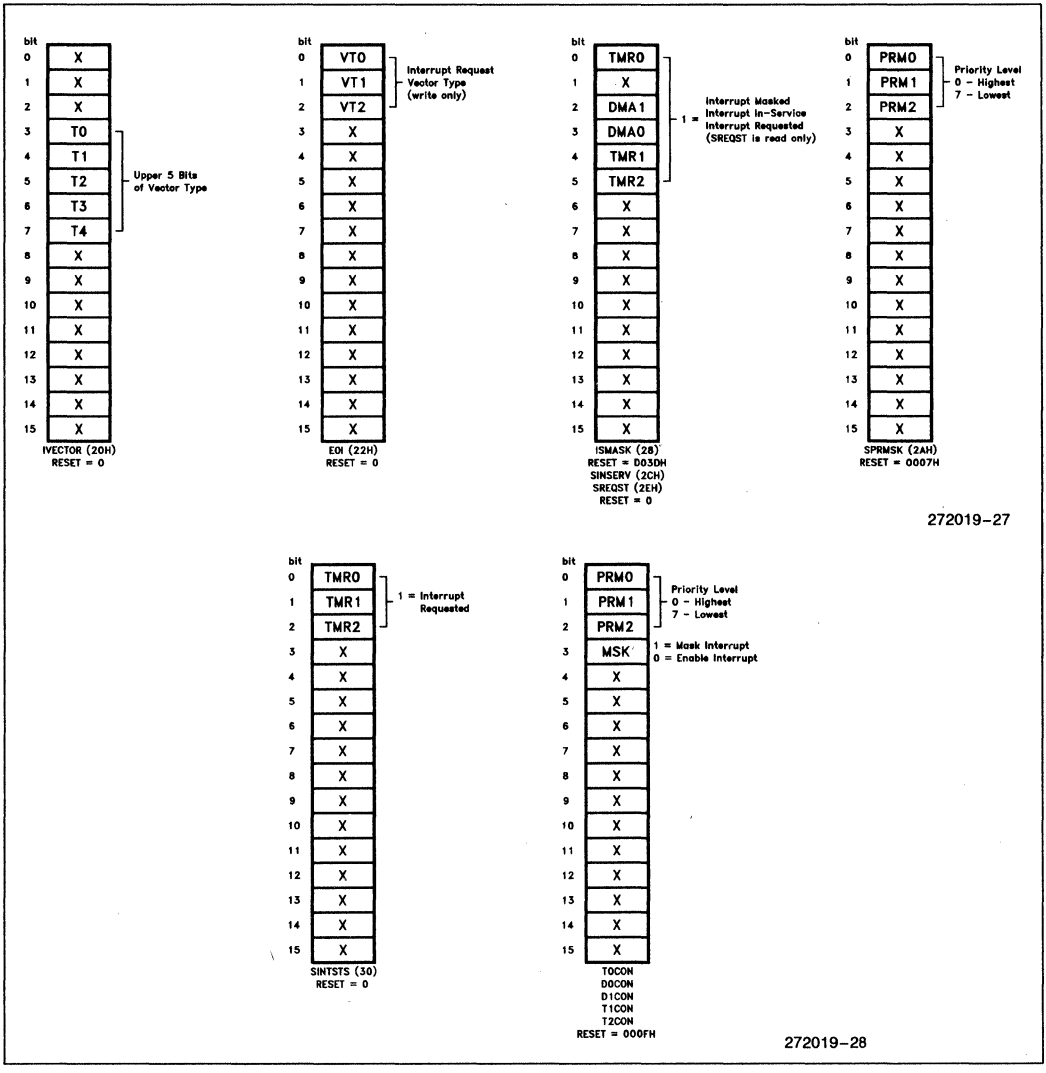

Figure 25. Interrupt Control Unit Registers (Slave Mode)

24

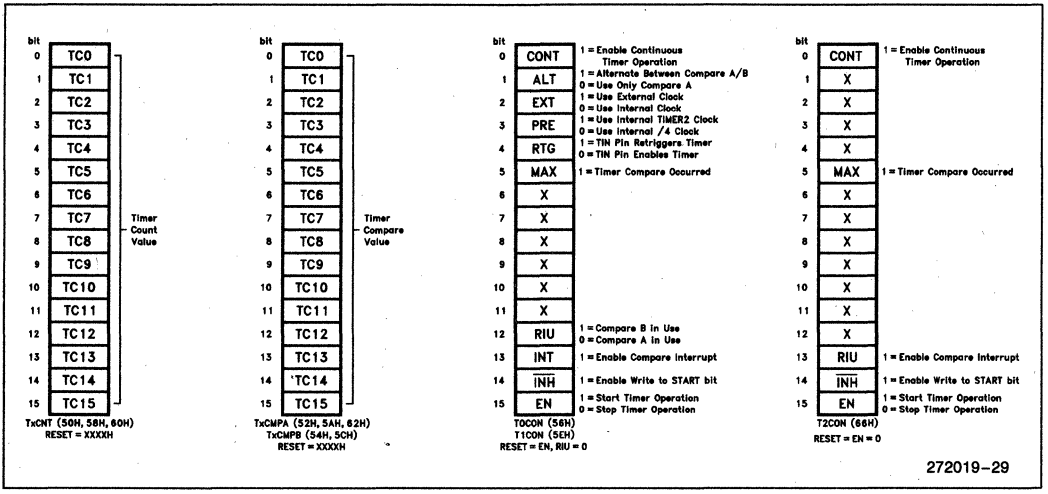

Figure 26. Timer Control Unit Registers

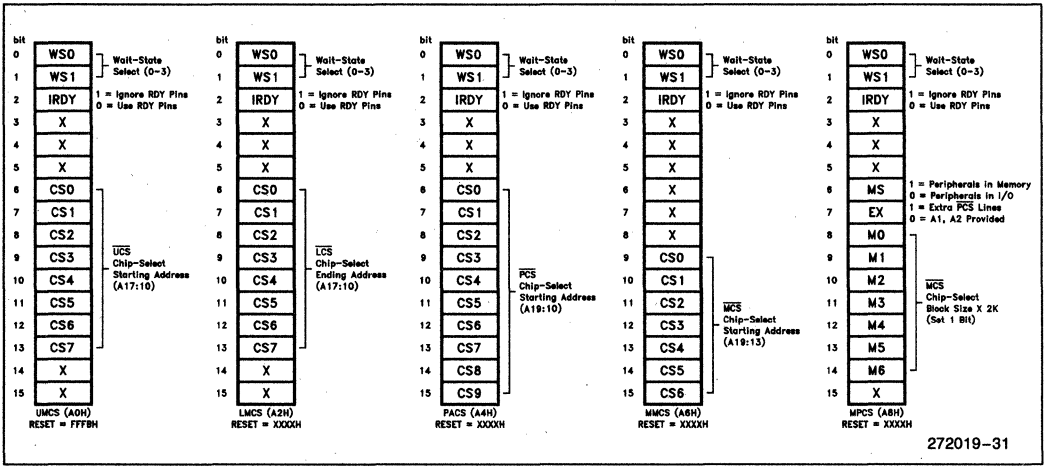

Figure 27. Chip-Select Unit Registers

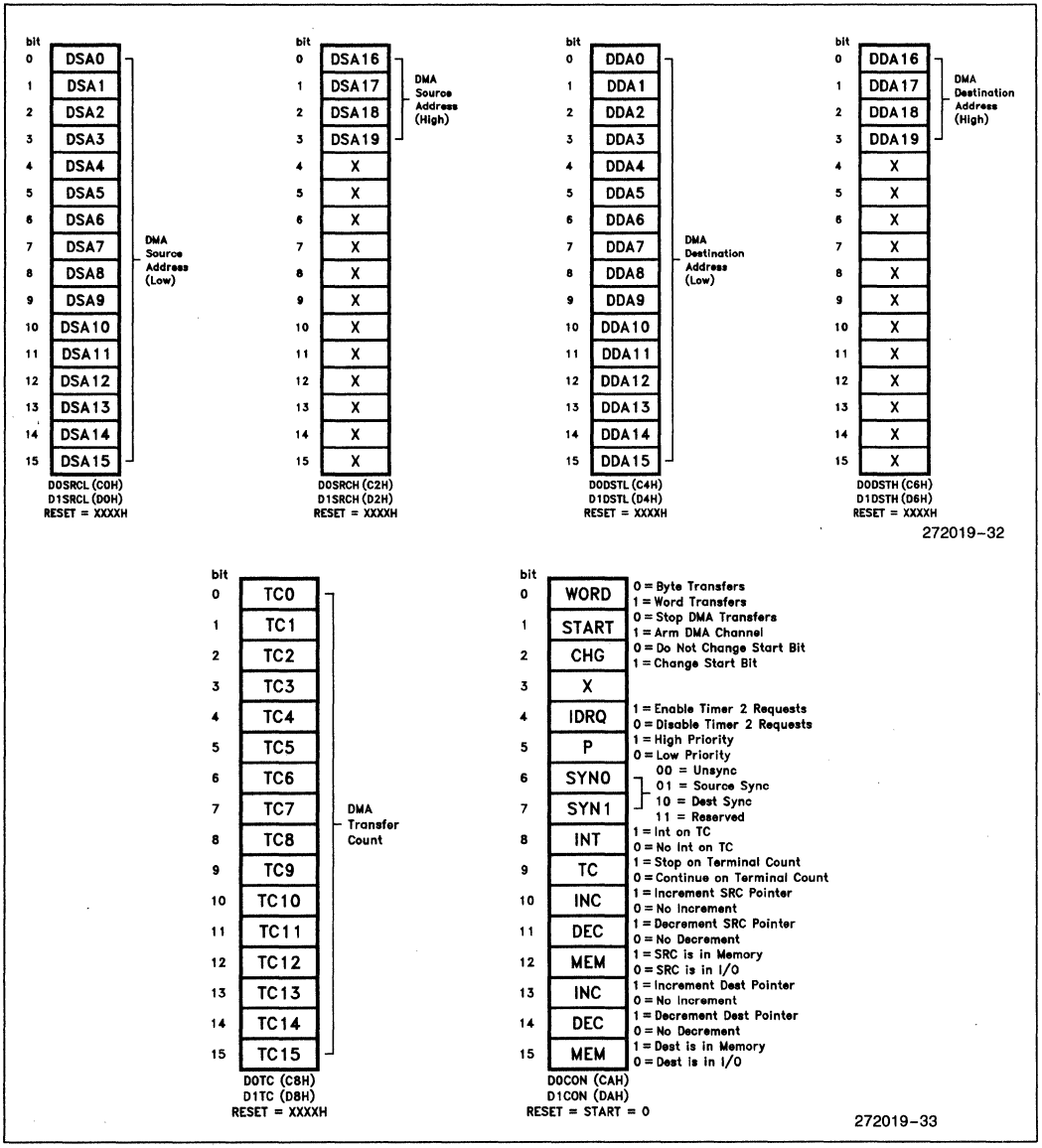

Figure 28. DMA Unit Registers

24

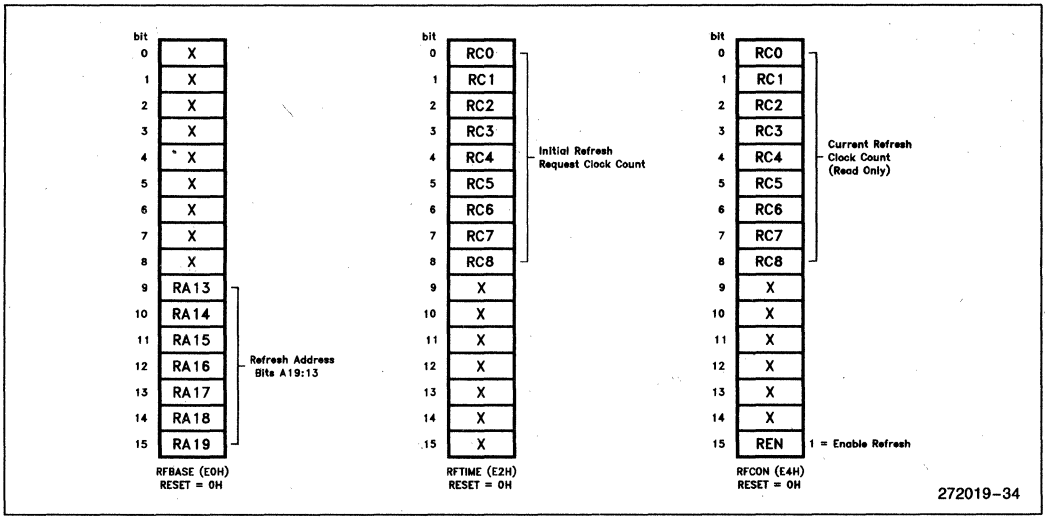

Figure 29. Refresh Control Unit Registers

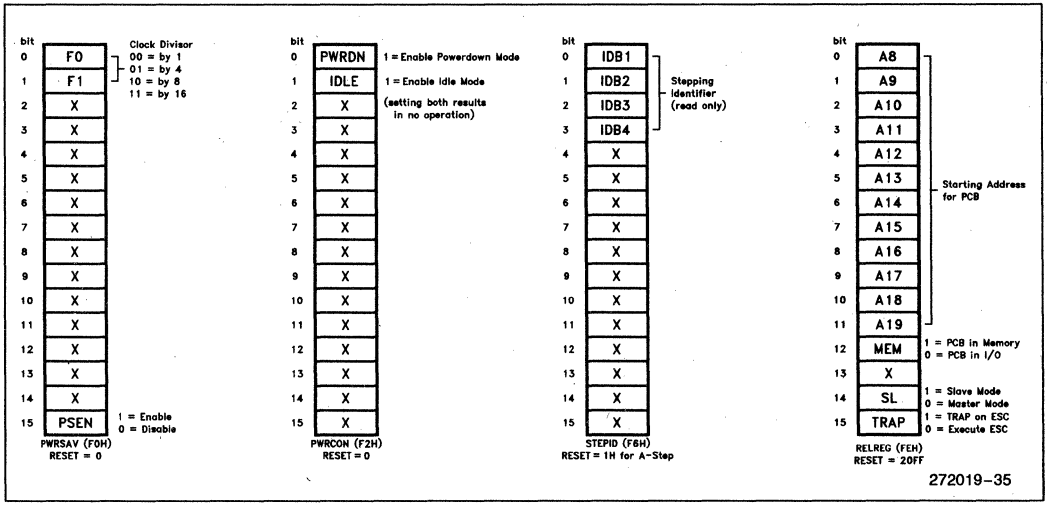

Figure 30. Power Management, Relocation and Stepping Registers

80C186EA EXPRESS

The Intel EXPRESS program offers an extended temperature range as an enhancement to the 80C186EA operational specifications. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the standard commercial temperature range, operational characteristics are guaranteed over a temperature range corresponding to 0°C to +70°C ambient. With the extended temperature range option, operational characteristics are guaranteed over a temperature range corresponding to −40°C to +85°C ambient.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 9. All AC and DC specifications are the same for both commercial and EXPRESS parts.

Table 9. Prefix Identification

Prefix	Package Type	Temperature Range
N	PLCC	Commercial
S	QFP (EIAJ)	Commercial
TN	PLCC	Extended
TS	QFP (EIAJ)	Extended

80C186EA EXECUTION TIMINGS

A determination of 80C186EA program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the **minimum** execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the 80C186EA has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1000100w	mod reg r/m			2/12	
Register/memory to register	1000101w	mod reg r/m			2/9	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12–13	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3–4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8	
Accumulator to memory	1010001w	addr-low	addr-high		9	
Register/memory to segment register	10001110	mod 0 reg r/m			2/9	
Segment register to register/memory	10001100	mod 0 reg r/m			2/11	
PUSH = Push:						
Memory	11111111	mod 1 1 0 r/m			16	
Register	01010 reg				10	
Segment register	000reg110				9	
Immediate	011010s0	data	data if s=0		10	
PUSHA = Push All	01100000				36	
POP = Pop:						
Memory	10001111	mod 0 0 0 r/m			20	
Register	01011 reg				10	
Segment register	000reg111	(reg≠01)			8	
POPA = Pop All	01100001				51	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10	
Variable port	1110110w				8	
OUT = Output to:						
Fixed port	1110011w	port			9	
Variable port	1110111w				7	
XLAT = Translate byte to AL	11010111				11	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		18	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		18	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				9	
POPF = Pop flags	10011101				8	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10	
Register with register/memory	0011100w	mod reg r/m			3/10	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26-28	
Register-Word					35-37	
Memory-Byte					32-34	
Memory-Word					41-43	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
ARITHMETIC (Continued)						
IMUL = Integer multiply (signed):	1111011w	mod101 r/m				
Register-Byte					25–28	
Register-Word					34–37	
Memory-Byte					31–34	
Memory-Word					40–43	
IMUL = Integer immediate multiply (signed)	011010s1	mod reg r/m	data	data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w	mod110 r/m				
Register-Byte					29	
Register-Word					38	
Memory-Byte					35	
Memory-Word					44	
IDIV = Integer divide (signed):	1111011w	mod111 r/m				
Register-Byte					44–52	
Register-Word					53–61	
Memory-Byte					50–58	
Memory-Word					59–67	
AAM = ASCII adjust for multiply	11010100	00001010			19	
AAD = ASCII adjust for divide	11010101	00001010			15	
CBW = Convert byte to word	10011000				2	
CWD = Convert word to double word	10011001				4	
LOGIC						
Shift/Rotate Instructions:						
Register/Memory by 1	1101000w	mod TTT r/m			2/15	
Register/Memory by CL	1101001w	mod TTT r/m			5+n/17+n	
Register/Memory by Count	1100000w	mod TTT r/m	count		5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR					
AND = **And:**						
Reg/memory and register to either	001000dw	mod reg r/m			3/10	
Immediate to register/memory	1000000w	mod100 r/m	data	data if w=1	4/16	
Immediate to accumulator	0010010w	data	data if w=1		3/4	8/16-bit
TEST = **And function to flags, no result:**						
Register/memory and register	1000010w	mod reg r/m			3/10	
Immediate data and register/memory	1111011w	mod000 r/m	data	data if w=1	4/10	
Immediate data and accumulator	1010100w	data	data if w=1		3/4	8/16-bit
OR = **Or:**						
Reg/memory and register to either	000010dw	mod reg r/m			3/10	
Immediate to register/memory	1000000w	mod001 r/m	data	data if w=1	4/16	
Immediate to accumulator	0000110w	data	data if w=1		3/4	8/16-bit

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
LOGIC (Continued)			
XOR = Exclusive or:			
Reg/memory and register to either	001100dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod 110 r/m | data | * data if w=1	4/16	
Immediate to accumulator	0011010w | data | data if w=1	3/4	8/16-bit
NOT = Invert register/memory	1111011w | mod 010 r/m	3/10	
STRING MANIPULATION			
MOVS = Move byte/word	1010010w	14	
CMPS = Compare byte/word	1010011w	22	
SCAS = Scan byte/word	1010111w	15	
LODS = Load byte/wd to AL/AX	1010110w	12	
STOS = Store byte/wd from AL/AX	1010101w	10	
INS = Input byte/wd from DX port	0110110w	14	
OUTS = Output byte/wd to DX port	0110111w	14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)			
MOVS = Move string	11110010 | 1010010w	8+8n	
CMPS = Compare string	1111001z | 1010011w	5+22n	
SCAS = Scan string	1111001z | 1010111w	5+15n	
LODS = Load string	11110010 | 1010110w	6+11n	
STOS = Store string	11110010 | 1010101w	6+9n	
INS = Input string	11110010 | 0110110w	8+8n	
OUTS = Output string	11110010 | 0110111w	8+8n	
CONTROL TRANSFER			
CALL = Call:			
Direct within segment	11101000 | disp-low | disp-high	15	
Register/memory indirect within segment	11111111 | mod 010 r/m	13/19	
Direct intersegment	10011010 | segment offset segment selector	23	
Indirect intersegment	11111111 | mod 011 r/m | (mod ≠ 11)	38	
JMP = Unconditional jump:			
Short/long	11101011 | disp-low	14	
Direct within segment	11101001 | disp-low | disp-high	14	
Register/memory indirect within segment	11111111 | mod 100 r/m	11/17	
Direct intersegment	11101010 | segment offset segment selector	14	
Indirect intersegment	11111111 | mod 101 r/m | (mod ≠ 11)	26	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
RET = **Return from CALL:**						
Within segment	11000011				16	
Within seg adding immed to SP	11000010	data-low	data-high		18	
Intersegment	11001011				22	
Intersegment adding immediate to SP	11001010	data-low	data-high		25	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22+16(n−1)	
LEAVE = Leave Procedure	11001001				8	
INT = **Interrupt:**						
Type specified	11001101	type			47	
Type 3	11001100				45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110				48/4	
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33–35	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	
	(TTT LLL are opcode to processor extension)		

Shaded areas indicate instructions not available in 8086/8088 microsystems.

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

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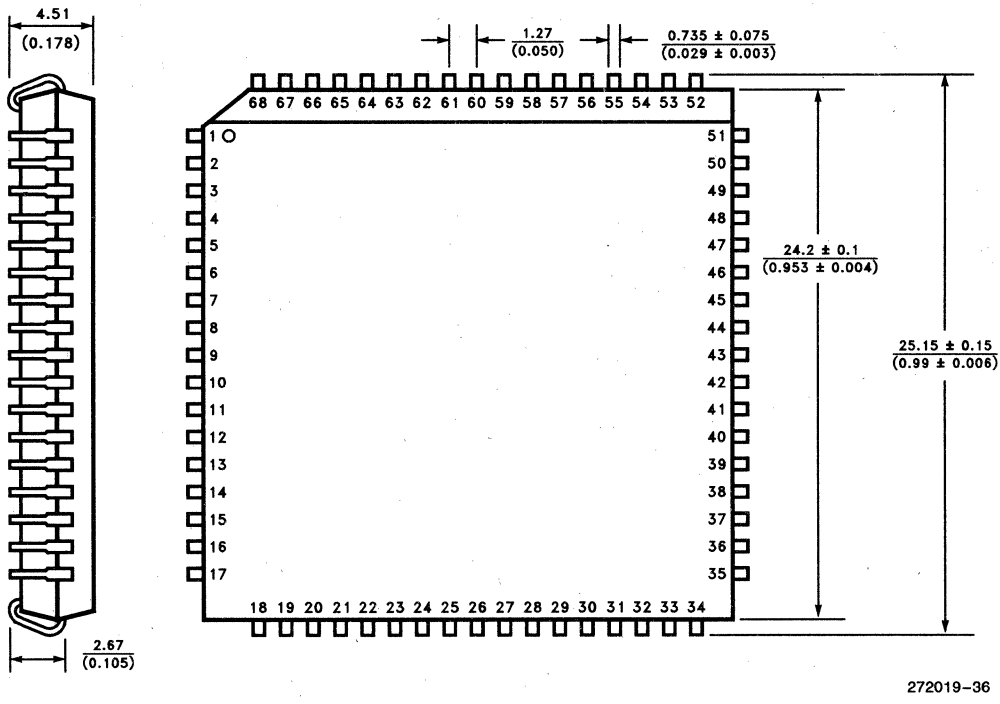
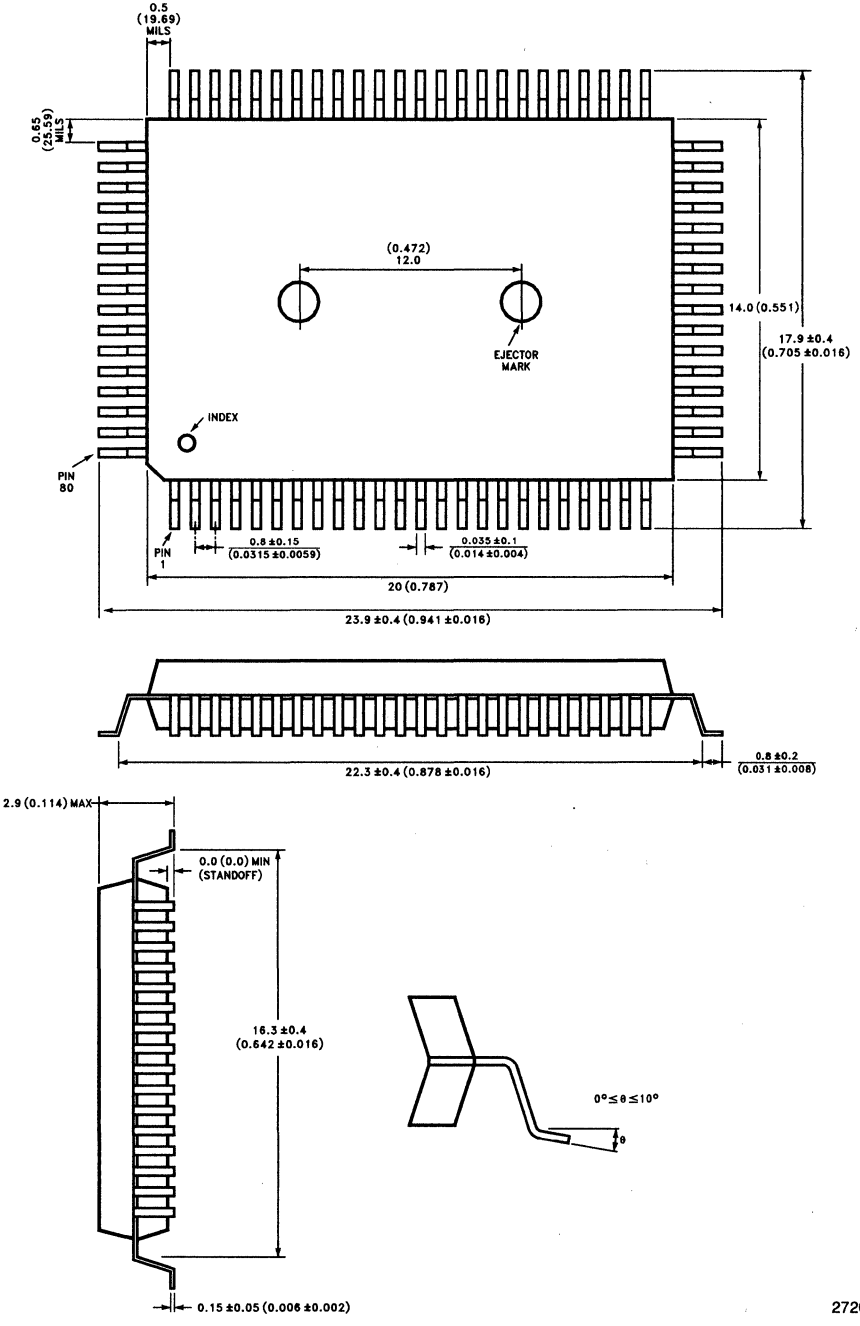


NOTE:
Units are mm/(inches).

Figure 31. PLCC Principal Dimensions



NOTE:
Units are mm (inches) unless specified.

Figure 32. QFP (EIAJ) Principal Dimensions

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REVISION HISTORY

Intel 80C186EA devices are marked with a 9-character alphanumeric Intel FPO number underneath the product number. This data sheet (272019-001) is valid for 80C186EA devices with an "A" or "B" as the ninth character in the FPO number, as illustrated in Figure 5 for the 68-lead PLCC package and Figure 6 for the 84-lead QFP (EIAJ) package. Such devices may also be identified by reading a value of 01H or 02H from the STEPID register.

The following changes were made between the -001 and -002 versions of the 80C188EA data sheets. The -002 data sheet applies to any 80C188EA with a "B" alpha character after the FPO number. The FPO number location is shown in Figures 5 and 6.

1. Much of the information provided in the -001 version of the data sheet has been removed. Detail descriptions of part functionality may be found in the 80C188EA User's Manual.

ERRATA

An 80C186EA with a STEPID value of 01H or 02H has the following known errata. A device with a STEPID of 01H or 02H can be visually identified by noting the presence of an "A" or "B" alpha character, repectively, next to the FPO number. The FPO number location is shown in Figures 5 and 6.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the INTA1 line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistantly, it is dependent on interrupt timing.

80C186EB-20, -16, -13, -8
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSOR

- **Full Static Operation**
- **True CMOS Inputs and Outputs**
- **−40°C to +85°C Operating Temperature Range**

- **Integrated Feature Set**
  - **Low-Power Static CPU Core**
  - **Two Independent UARTs each with an Integral Baud Rate Generator**
  - **Two 8-Bit Multiplexed I/O Ports**
  - **Programmable Interrupt Controller**
  - **Three Programmable 16-Bit Timer/Counters**
  - **Clock Generator**
  - **Ten Programmable Chip Selects with Integral Wait-State Generator**
  - **Memory Refresh Control Unit**
  - **System Level Testing Support (ONCE™ Mode)**
- **Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O**
- **Speed Versions Available:**
  - **20 MHz (80C186EB-20)**
  - **16 MHz (80C186EB-16)**
  - **13 MHz (80C186EB-13)**
  - **8 MHz (80C186EB-8)**
- **Low-Power Operating Modes:**
  - **Idle Mode Freezes CPU Clocks but keeps Peripherals Active**
  - **Powerdown Mode Freezes All Internal Clocks**
- **Complete System Development Support**
  - **ASM86 Assembler, PL/M 86, Pascal 86, Fortran 86, C-86, and System Utilities**
  - **In-Circuit Emulator (ICE™-186EB)**
- **Supports 80C187 Numeric Coprocessor Interface (TN80C186EB Only)**
- **Available In:**
  - **80-Pin Quad Flat Pack (TS80C186EB)**
  - **84-Pin Plastic Leaded Chip Carrier (TN80C186EB)**

The 80C186EB is a second generation CHMOS High-Integration microprocessor. It has features that are new to the 80C186 family and include a STATIC CPU core, an enhanced Chip Select decode unit, two independent Serial Channels, I/O ports, and the capability of Idle or Powerdown low power modes.

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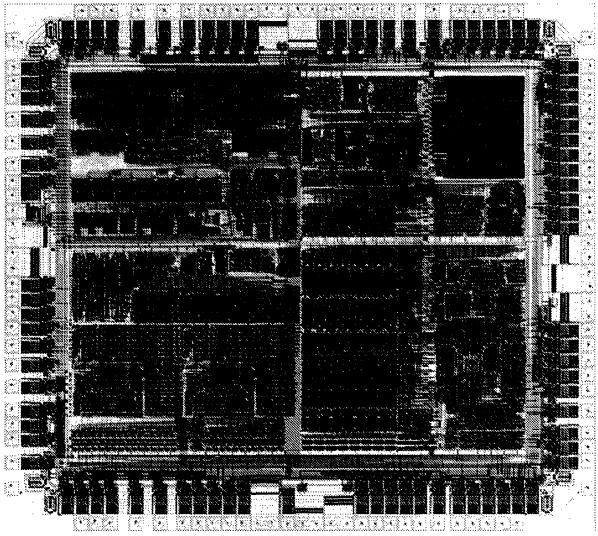


270803-37

May 1992
Order Number: 270803-004

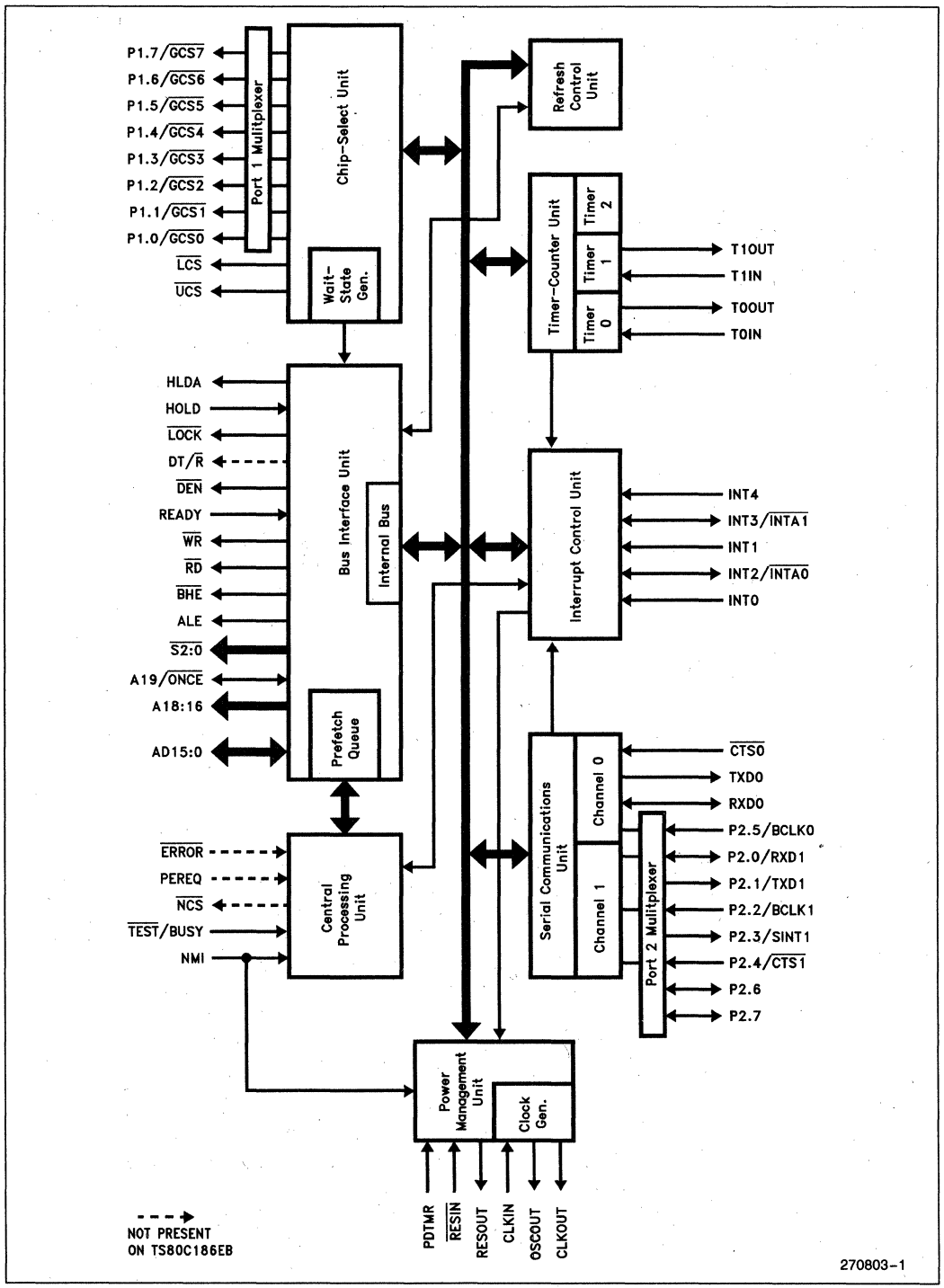


Figure 1. 80C186EB Block Diagram

INTRODUCTION

The 80C186EB is the first product in a new generation of low-power, high-integration microprocessors. It enhances the existing 186 family by offering new features and new operating modes. The 80C186EB is object code compatible with the 80C186/80C188 microprocessors.

The feature set of the 80C186EB meets the needs of low power, space critical applications. Low-Power applications benefit from the static design of the CPU core and the integrated peripherals. Minimum current consumption is achieved by providing a Powerdown mode that halts operation of the device, and freezes the clock circuits. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space critical applications benefit from the integration of commonly used system peripherals. Two serial channels are provided for services such as diagnostics, inter-processor communication, modem interface, terminal display interface, and many others. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 129 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters and sixteen multiplexed I/O port pins round out the feature set of the 80C186EB.

OVERVIEW

Figure 1 shows a block diagram of the 80C186EB. The Execution Unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instruction, and full static operation. The Bus Interface Unit (BIU) is the same as that found on the original 186 family products, except the queue-status mode has been deleted and buffer interface control has been changed to ease system design timings. An independent internal bus is used to allow communication between the BIU and internal peripherals.

BUS INTERFACE UNIT

The 80C186EB core incorporates a bus controller that generates local bus control signals. In addition, it employs a HOLD/HLDA protocol to share the local bus with other bus masters.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information, and data (for write operations) information. It is also responsible for reading data off the local bus during a read operation. A READY input pin is provided to extend a bus cycle beyond the minimum four states (clocks).

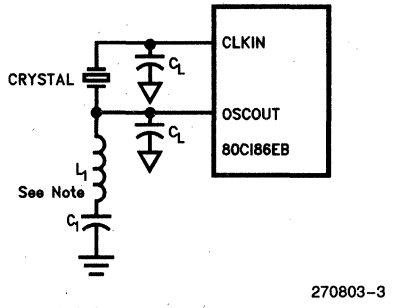
The 80C186EB local bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. (Both $\overline{DEN}$ and DT/$\overline{R}$ are available on the TN80C186EB device, only $\overline{DEN}$ is available on the TS80C186EB device.) This capability allows the addition of transceivers for simple buffering of the mulitplexed address/data bus.

CLOCK GENERATOR

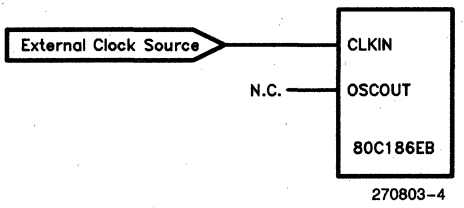
The 80C186EB provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, and two low-power operating modes.

The oscillator circuit is designed to be used with either a **parallel resonant** fundamental or third-overtone mode crystal network. Alternatively, the oscillator circuit may be driven from an external clock source. Figure 2 shows the various operating modes of the 80C186EB oscillator circuit.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide-by-two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.



(A) Crystal Connection



(B) Clock Connection

NOTE:
The L_1C_1 network is **only** required when using a third-overtone crystal.

Figure 2. 80C186EB Clock Configurations

The following parameters are recommended when choosing a crystal:

Temperature Range:	Application Specific
ESR (Equivalent Series Resistance):	40Ω max
C0 (Shunt Capacitance of Crystal):	7.0 pF max
C_L (Load Capacitance):	20 pF ± 2 pF
Drive Level:	1 mW max

80C186EB Peripheral Architecture

The 80C186EB has integrated several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexible and provide logical interconnections between supporting units (e.g., the interrupt control unit supports interrupt requests from the timer/counters or serial channels).

The list of integrated peripherals includes:

- 7-Input Interrupt Control Unit
- 3-Channel Timer/Counter Unit
- 2-Channel Serial Communications Unit
- 10-Output Chip-Select Unit
- I/O Port Unit
- Refresh Control Unit
- Power Management Unit

The registers associated with each integrated peripheral are contained within a 128 x 16 register file called the Peripheral Control Block (PCB). The PCB can be located in either memory or I/O space on any 256 Byte address boundary.

Figure 3 provides a list of the registers associated with the PCB. The Register Bit Summary at the end of this specification individually lists all of the registers and identifies each of their programming attributes.

INTERRUPT CONTROL UNIT

The 80C186EB can receive interrupts from a number of sources, both internal and external. The interrupt control unit serves to merge these requests on a priority basis, for individual service by the CPU. Each interrupt source can be independently masked by the Interrupt Control Unit (ICU) or all interrupts can be globally masked by the CPU.

Internal interrupt sources include the Timers and Serial channel 0. External interrupt sources come from the five input pins INT4:0. The NMI interrupt pin is not controlled by the ICU and is passed directly to the CPU. Although the Timer and Serial channel each have only one request input to the ICU, separate vector types are generated to service individual interrupts within the Timer and Serial channel units.

TIMER/COUNTER UNIT

The 80C186EB Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms, generate timed interrupts. etc.

PCB Offset	Function
00H	Reserved
02H	End Of Interrupt
04H	Poll
06H	Poll Status
08H	Interrupt Mask
0AH	Priority Mask
0CH	In-Service
0EH	Interrupt Request
10H	Interrupt Status
12H	Timer Control
14H	Serial Control
16H	INT4 Control
18H	INT0 Control
1AH	INT1 Control
1CH	INT2 Control
1EH	INT3 Control
20H	Reserved
22H	Reserved
24H	Reserved
26H	Reserved
28H	Reserved
2AH	Reserved
2CH	Reserved
2EH	Reserved
30H	Timer0 Count
32H	Timer0 Compare A
34H	Timer0 Compare B
36H	Timer0 Control
38H	Timer1 Count
3AH	Timer1 Compare A
3CH	Timer1 Compare B
3EH	Timer1 Control

PCB Offset	Function
40H	Timer2 Count
42H	Timer2 Compare
44H	Reserved
46H	Timer2 Control
48H	Reserved
4AH	Reserved
4CH	Reserved
4EH	Reserved
50H	Reserved
52H	Port0 Pin
54H	Port0 Control
56H	Port0 Latch
58H	Port1 Direction
5AH	Port1 Pin
5CH	Port1 Control
5EH	Port1 Latch
60H	Serial0 Baud
62H	Serial0 Count
64H	Serial0 Control
66H	Serial0 Status
68H	Serial0 RBUF
6AH	Serial0 TBUF
6CH	Reserved
6EH	Reserved
70H	Serial1 Baud
72H	Serial1 Count
74H	Serial1 Control
76H	Serial1 Status
78H	Serial1 RBUF
7AH	Serial1 TBUF
7CH	Reserved
7EH	Reserved

PCB Offset	Function
80H	GCS0 Start
82H	GCS0 Stop
84H	GCS1 Start
86H	GCS1 Stop
88H	GCS2 Start
8AH	GCS2 Stop
8CH	GCS3 Start
8EH	GCS3 Stop
90H	GCS4 Start
92H	GCS4 Stop
94H	GCS5 Start
96H	GCS5 Stop
98H	GCS6 Start
9AH	GCS6 Stop
9CH	GCS7 Start
9EH	GCS7 Stop
A0H	LCS Start
A2H	LCS Stop
A4H	UCS Start
A6H	UCS Stop
A8H	Relocation
AAH	Reserved
ACH	Reserved
AEH	Reserved
B0H	Refresh Base
B2H	Refresh Time
B4H	Refresh Control
B6H	Refresh Address
B8H	Power Control
BAH	Reserved
BCH	Step ID
BEH	Reserved

PCB Offset	Function
C0H	Reserved
C2H	Reserved
C4H	Reserved
C6H	Reserved
C8H	Reserved
CAH	Reserved
CCH	Reserved
CEH	Reserved
D0H	Reserved
D2H	Reserved
D4H	Reserved
D6H	Reserved
D8H	Reserved
DAH	Reserved
DCH	Reserved
DEH	Reserved
E0H	Reserved
E2H	Reserved
E4H	Reserved
E6H	Reserved
E8H	Reserved
EAH	Reserved
ECH	Reserved
EEH	Reserved
F0H	Reserved
F2H	Reserved
F4H	Reserved
F6H	Reserved
F8H	Reserved
FAH	Reserved
FCH	Reserved
FEH	Reserved

Figure 3. 80C186EB Peripheral Control Block Registers

SERIAL COMMUNICATIONS UNIT

The Serial Control Unit (SCU) of the 80C186EB contains two independent channels. Each channel is identical in operation except that only channel 0 is supported by the integrated interrupt controller (channel 1 has an external interrupt pin). Each channel has its own baud rate generator that is independent of the Timer/Counter Unit, and can be internally or externally clocked at up to one half the 80C186EB operating frequency.

Independent baud rate generators are provided for each of the serial channels. For the asynchronous modes, the generator supplies an 8x baud clock to both the receive and transmit register logic. A 1x baud clock is provided in the synchronous mode.

CHIP-SELECT UNIT

The 80C186EB Chip-Select Unit (CSU) integrates logic which provides up to ten programmable chip-selects to access both memories and peripherals. In addition, each chip-select can be programmed to automatically insert additional clocks (wait-states) into the current bus cycle and automatically terminate a bus cycle independent of the condition of the READY input pin.

I/O PORT UNIT

The I/O Port Unit (IPU) on the 80C186EB supports two 8-bit channels of input, output, or input/output operation. Port 1 is multiplexed with the chip select pins and is output only. Most of Port 2 is multiplexed with the serial channel pins. Port 2 pins are limited to either an output or input function depending on the operation of the serial pin it is multiplexed with.

REFRESH CONTROL UNIT

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 12-bit address generator is maintained by the RCU and is presented on the A12:1 address lines during the refresh bus cycle. Address bits A19:13 are programmable to allow the refresh address block to be located on any 8 Kbyte boundary.

POWER MANAGEMENT UNIT

The 80C186EB Power Management Unit (PMU) is provided to control the power consumption of the device. The PMU provides three power modes: Active, Idle, and Powerdown.

Active Mode indicates that all units on the 80C186EB are functional and the device consumes maximum power (depending on the level of peripheral operation). Idle Mode freezes the clocks of the Execution and Bus units at a logic zero state (all peripherals continue to operate normally).

The Powerdown mode freezes all internal clocks at a logic zero level and disables the crystal oscillator. All internal registers hold their values provided V_{CC} is maintained. Current consumption is reduced to just transistor junction leakage.

80C187 Interface

The 80C186EB (PLCC package only) supports the direct connection of the 80C187 Numerics Coprocessor.

ONCE™ Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C186EB has a test mode available which forces all output and input/output pins to be placed in the high-impedance state. ONCE stands for "ON Circuit Emulation". The ONCE mode is selected by forcing the A19/$\overline{\text{ONCE}}$ pin LOW (0) during a processor reset (this pin is weakly held to a HIGH (1) level) while $\overline{\text{RESIN}}$ is active.

PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the 80C186EB in the Plastic Leaded Chip Carrier (PLCC) package and Quad Flat Pack (QFP) package. For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

Pin Descriptions

The 80C186EB pins are described in this section. Table 1 presents the legend for interpreting the pin descriptions in Table 2. Figure 4 provides an example pin description entry. The "I/O" signifies that the pins are bidirectional (i.e., have both an input and output function). The "S" indicates that, as an input, the signal is synchronized to CLKOUT for proper operation. The "H(Z)" indicates that these pins will float while the processor is in the Hold Acknowledge state. R(Z) indicates that these pins will float while $\overline{\text{RESIN}}$ is low. P(X) Indicates that these pins will retain its current value when Idle or Powerdown Modes are entered.

All pins float while the processor is in the ONCE™ Mode, except OSCOUT (OSCOUT is required for crystal operation).

Name	Type	Description
AD15:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed ADDRESS and DATA bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information are transferred during the data phase of the bus cycle.

Figure 4. Example Pin Description Entry

Table 1. Pin Description Nomenclature

Symbol	Description
I	Input Only Pin
O	Output Only Pin
I/O	Pin can be either input or output
—	Pin "must be" connected as described
S(..)	Synchronous. Input must meet setup and hold times for proper operation of the processor. The pin is: S(E) edge sensitive S(L) level sensitive
A(..)	Asynchronous. Input must meet setup and hold only to guarantee recognition. The pin is: A(E) edge sensitive A(L) level sensitive
H(..)	While the processor's bus is in the Hold Acknowledge state, the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Z) floats H(Q) remains active H(X) retains current state
R(..)	While the processor's $\overline{\text{RES}}$ line is low, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Z) floats R(WH) weak pullup R(WL) weak pulldown
P(..)	While Idle or Powerdown modes are active, the pin: P(1) is driven to V_{CC} P(0) is driven to V_{SS} P(Z) floats P(Q) remains active(1) P(X) retains current state

NOTE:
1. Any pin that specifies P(Q) are valid for Idle Mode. All pins are P(X) for Powerdown Mode.

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Table 2. 80C186EB Pin Descriptions

Name	Type	Description
V_{CC}		**POWER** connections consist of four pins which must be shorted externally to a V_{CC} board plane.
V_{SS}		**GROUND** connections consist of six pins which must be shorted externally to a V_{SS} board plane.
CLKIN	I A(E)	**CLocK INput** is an input for an external clock. An external oscillator operating at two times the required 80C186EB operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O H(Q) R(Q) P(Q)	**OSCillator OUTput** is only used when using a crystal to generate the external clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin is not to be used as 2X clock output for non-crystal applications (i.e., this pin is N.C. for non-crystal applications). OSCOUT does not float in ONCE mode.
CLKOUT	O H(Q) R(Q) P(Q)	**CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transistions every falling edge of CLKIN.
$\overline{\text{RESIN}}$	I A(L)	**RESet IN** causes the 80C186EB to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the 80C186EB begins fetching opcodes at memory location 0FFFF0H.
RESOUT	O H(0) R(1) P(0)	**RESet OUTput** that indicates the 80C186EB is currently in the reset state. RESOUT will remain active as long as $\overline{\text{RESIN}}$ remains active.
PDTMR	I/O A(L) H(WH) R(Z) P(1)	**Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the 80C186EB waits after an exit from power down before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I A(E)	**Non-Maskable Interrupt** input causes a TYPE-2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{\text{TEST}}$/BUSY	I A(E)	**TEST** is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (LOW). $\overline{\text{TEST}}$ is alternately known as BUSY when interfacing with an 80C187 numerics coprocessor.
AD15:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed **Address** and **Data** bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle.
A18:16 A19/$\overline{\text{ONCE}}$	H(Z) R(WH) P(X)	These pins provide multiplexed **Address** during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. These pins are driven to a logic 0 during the data phase of the bus cycle. During a processor reset ($\overline{\text{RESIN}}$ active), A19/$\overline{\text{ONCE}}$ is used to enable ONCE mode. A18:16 must not be driven low during reset or improper 80C186EB operation may result.

Table 2. 80C186EB Pin Descriptions (Continued)

Name	Type	Description
$\overline{S2:0}$	O H(Z) R(Z) P(1)	Bus cycle **Status** are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ Bus Cycle Initiated 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive (no bus activity)
ALE	O H(0) R(0) P(0)	**Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle.
$\overline{BHE}$	O H(Z) R(Z) P(X)	**Byte High Enable** output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. $\overline{BHE}$ and A0 have the following logical encoding: A0 $\overline{BHE}$ Encoding 0 0 Word Transfer 0 1 Even Byte Transfer 1 0 Odd Byte Transfer 1 1 Refresh Operation
$\overline{RD}$	O H(Z) R(Z) P(1)	**ReaD** output signals that the accessed memory or I/O device must drive data information onto the data bus.
$\overline{WR}$	O H(Z) R(Z) P(1)	**WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device.
READY	I A(L) S(L)	**READY** input to signal the completion of a bus cycle. READY must be active to terminate any 80C186EB bus cycle, unless it is ignored by correctly programming the Chip-Select Unit.
$\overline{DEN}$	O H(Z) R(Z) P(1)	**Data ENable** output to control the enable of bi-directional transceivers when buffering a 80C186EB system. $\overline{DEN}$ is active only when data is to be transferred on the bus.
DT/$\overline{R}$	O H(Z) R(Z) P(X)	**Data Transmit/Receive** output controls the direction of a bi-directional buffer when buffering an 80C186EB system. DT/$\overline{R}$ is only available for the PLCC package (TN80C186EB).
$\overline{LOCK}$	I/O H(Z) R(WH) P(1)	**LOCK** output indicates that the bus cycle in progress is not to be interrupted. The 80C186EB will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low.

Table 2. 80C186EB Pin Descriptions (Continued)

Name	Type	Description
HOLD	I A(L)	**HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The 80C186EB will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
HLDA	O H(1) R(0) P(0)	**HoLD Acknowledge** output to indicate that the 80C186EB has relinquish control of the local bus. When HLDA is asserted, the 80C186EB will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly.
$\overline{NCS}$	O H(1) R(1) P(1)	**Numerics Coprocessor Select** output is generated when accessing a numerics coprocessor. $\overline{NCS}$ is not provided on the TS80C186EB.
$\overline{ERROR}$	I A(L)	**ERROR** input that indicates the last numerics coprocessor operation resulted in an exception condition. An interrupt TYPE 16 is generated if $\overline{ERROR}$ is sampled active at the beginning of a numerics operation. $\overline{ERROR}$ is not provided on the TS80C186EB.
PEREQ	I A(L)	**CoProcessor REQuest** signals that a data transfer between an External Numerics Coprocessor and Memory is pending. PEREQ is not provided on the TS80C186EB.
$\overline{UCS}$	O H(1) R(1) P(1)	**Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH.
$\overline{LCS}$	O H(1) R(1) P(1)	**Lower Chip Select** will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. $\overline{LCS}$ is inactive after a reset.
P1.0/$\overline{GCS0}$ P1.1/$\overline{GCS1}$ P1.2/$\overline{GCS2}$ P1.3/$\overline{GCS3}$ P1.4/$\overline{GCS4}$ P1.5/$\overline{GCS5}$ P1.6/$\overline{GCS6}$ P1.7/$\overline{GCS7}$	O H(X)/H(1) R(1) P(X)/P(1)	These pins provide a multiplexed function. If enabled, each pin can provide a **Generic Chip Select** output which will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. When not programmed as a Chip-Select, each pin may be used as a general purpose output **Port.** As an output port pin, the value of the pin can be read internally.
T0OUT T1OUT	O H(Q) R(1) P(Q)	**Timer OUTput** pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.
T0IN T1IN	I A(L) A(E)	**Timer INput** is used either as clock or control signals, depending on the timer mode selected.

Table 2. 80C186EB Pin Descriptions (Continued)

Name	Type	Description
INT0 INT1 INT4	I A(E,L)	Maskable **INTerrupt** input will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with $\overline{\text{INTA0}}$ and $\overline{\text{INTA1}}$ to interface with an external slave controller.
INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$	I/O A(E,L) /H(1) R(Z) /P(1)	These pins provide a multiplexed function. As inputs, they provide a maskable **INTerrupt** that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an INTERRUPT ACKNOWLEDGE handshake signal to allow interrupt expansion.
P2.7 P2.6	I/O A(L) H(X) R(Z) P(X)	BI-DIRECTIONAL, open-drain **Port** pins.
$\overline{\text{CTS0}}$ P2.4/$\overline{\text{CTS1}}$	I A(L)	**Clear-To-Send** input is used to prevent the transmission of serial data on their respective TXD signal pin. $\overline{\text{CTS1}}$ is multiplexed with an input only port function.
TXD0 P2.1/TXD1	O H(X)/H(Q) R(1) P(X)/P(Q)	**Transmit Data** output provides serial data information. TXD1 is multiplexed with an output only **Port** function. During synchronous serial communications, TXD will function as a clock output.
RXD0 P2.0/RXD1	I/O A(L) R(Z) H(Q) P(X)	**Receive Data** input accepts serial data information. RXD1 is multiplexed with an input only **Port** function. During synchronous serial communications, RXD is bi-directional and will become an output for transmission or data (TXD becomes the clock).
P2.5/BCLK0 P2.2/BCLK1	I A(L)/A(E)	**Baud CLocK** input can be used as an alternate clock source for each of the integrated serial channels. BCLKx is multiplexed with an input only **Port** function, and cannot exceed a clock rate greater than one-half the operating frequency of the 80C186EB.
P2.3/SINT1	O H(X)/H(Q) R(0) P(X)/P(Q)	**Serial INTerrupt** output will go active to indicate serial channel 1 requires service. SINT1 is multiplexed with an output only **Port** function.

80C186EB PINOUT

Tables 3 and 4 list the 80C186EB pin names with package location for the 84-pin Plastic Leaded Chip Carrier (PLCC) component. Figure 5 depicts the complete 80C186EB pinout (PLCC package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 5 and 6 list the 80C186EB pin names with package location for the 80-pin Quad Flat Pack (QFP) component. Figure 6 depicts the complete 80C186EB (QFP package) as viewed from the top side of the component (i.e., contacts facing down).

Table 3. PLCC Pin Names with Package Location

Address/Data Bus	
Name	**Location**
AD0	61
AD1	66
AD2	68
AD3	70
AD4	72
AD5	74
AD6	76
AD7	78
AD8	62
AD9	67
AD10	69
AD11	71
AD12	73
AD13	75
AD14	77
AD15	79
A16	80
A17	81
A18	82
A19/$\overline{\text{ONCE}}$	83

Bus Control	
Name	**Location**
ALE	6
$\overline{\text{BHE}}$	7
$\overline{\text{S0}}$	10
$\overline{\text{S1}}$	9
$\overline{\text{S2}}$	8
$\overline{\text{RD}}$	4
$\overline{\text{WR}}$	5
READY	18
$\overline{\text{DEN}}$	11
DT/$\overline{\text{R}}$	16
$\overline{\text{LOCK}}$	15
HOLD	13
HLDA	12

Power	
Name	**Location**
V_{SS}	2, 22, 43 63, 65, 84
V_{CC}	1, 23 42, 64

Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	37
RESOUT	38
CLKIN	41
OSCOUT	40
CLKOUT	44
$\overline{\text{TEST}}$/BUSY	14
$\overline{\text{NCS}}$	60
PEREQ	39
$\overline{\text{ERROR}}$	3
PDTMR	36
NMI	17
INT0	31
INT1	32
INT2/$\overline{\text{INTA0}}$	33
INT3/$\overline{\text{INTA1}}$	34
INT4	35

I/O	
Name	**Location**
$\overline{\text{UCS}}$	30
$\overline{\text{LCS}}$	29
P1.0/$\overline{\text{GCS0}}$	28
P1.1/$\overline{\text{GCS1}}$	27
P1.2/$\overline{\text{GCS2}}$	26
P1.3/$\overline{\text{GCS3}}$	25
P1.4/$\overline{\text{GCS4}}$	24
P1.5/$\overline{\text{GCS5}}$	21
P1.6/$\overline{\text{GCS6}}$	20
P1.7/$\overline{\text{GCS7}}$	19
T0OUT	45
T0IN	46
T1OUT	47
T1IN	48
RXD0	53
TXD0	52
P2.5/BCLK0	54
$\overline{\text{CTS0}}$	51
P2.0/RXD1	57
P2.1/TXD1	58
P2.2/BCLK1	59
P2.3/SINT1	55
P2.4/$\overline{\text{CTS1}}$	56
P2.6	50
P2.7	49

Table 4. PLCC Package Locations with Pin Name

Location	Name	Location	Name	Location	Name	Location	Name
1	V_{CC}	22	V_{SS}	43	V_{SS}	64	V_{CC}
2	V_{SS}	23	V_{CC}	44	CLKOUT	65	V_{SS}
3	$\overline{ERROR}$	24	P1.4/$\overline{GCS4}$	45	T0OUT	66	AD1
4	$\overline{RD}$	25	P1.3/$\overline{GCS3}$	46	T0IN	67	AD9
5	$\overline{WR}$	26	P1.2/$\overline{GCS2}$	47	T1OUT	68	AD2
6	ALE	27	P1.1/$\overline{GCS1}$	48	T1IN	69	AD10
7	$\overline{BHE}$	28	P1.0/$\overline{GCS0}$	49	P2.7	70	AD3
8	$\overline{S2}$	29	$\overline{LCS}$	50	P2.6	71	AD11
9	$\overline{S1}$	30	$\overline{UCS}$	51	$\overline{CTS0}$	72	AD4
10	$\overline{S0}$	31	INT0	52	TXD0	73	AD12
11	$\overline{DEN}$	32	INT1	53	RXD0	74	AD5
12	HLDA	33	INT2/$\overline{INTA0}$	54	P2.5/BCLK0	75	AD13
13	HOLD	34	INT3/$\overline{INTA1}$	55	P2.3/SINT1	76	AD6
14	$\overline{TEST}$/BUSY	35	INT4	56	P2.4/$\overline{CTS1}$	77	AD14
15	$\overline{LOCK}$	36	PDTMR	57	P2.0/RXD1	78	AD7
16	DT/$\overline{R}$	37	$\overline{RESIN}$	58	P2.1/TXD1	79	AD15
17	NMI	38	RESOUT	59	P2.2/BCLK1	80	A16
18	READY	39	PEREQ	60	$\overline{NCS}$	81	A17
19	P1.7/$\overline{GCS7}$	40	OSCOUT	61	AD0	82	A18
20	P1.6/$\overline{GCS6}$	41	CLKIN	62	AD8	83	A19/$\overline{ONCE}$
21	P1.5/$\overline{GCS5}$	42	V_{CC}	63	V_{SS}	84	V_{SS}

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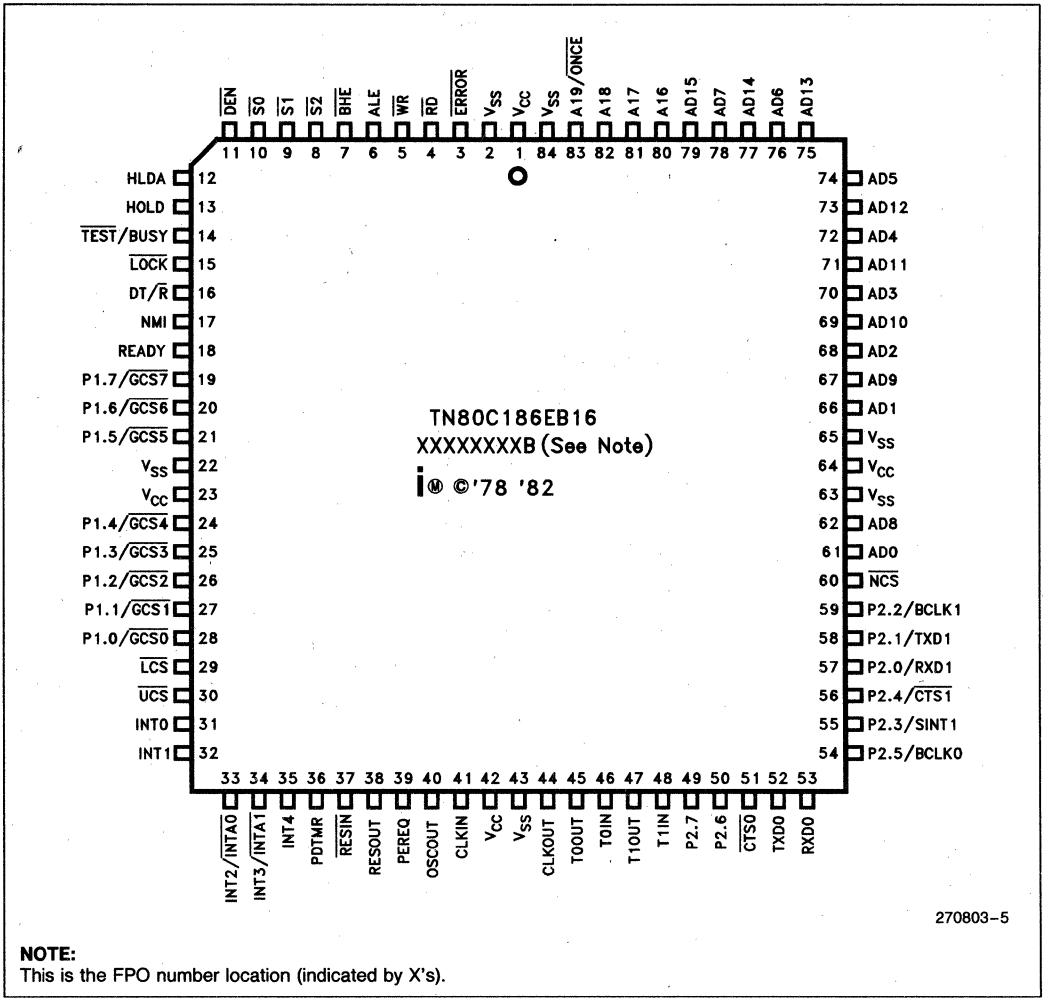


NOTE:
This is the FPO number location (indicated by X's).

Figure 5. 84-Pin Plastic Leaded Chip Carrier Pinout Diagram

Table 5. QFP Pin Name with Package Location

Address/Data Bus	
Name	**Location**
AD0	10
AD1	15
AD2	17
AD3	19
AD4	21
AD5	23
AD6	25
AD7	27
AD8	11
AD9	16
AD10	18
AD11	20
AD12	22
AD13	24
AD14	26
AD15	28
A16	29
A17	30
A18	31
A19/$\overline{ONCE}$	32

Bus Control	
Name	**Location**
ALE	38
$\overline{BHE}$	39
$\overline{S0}$	42
$\overline{S1}$	41
$\overline{S2}$	40
$\overline{RD}$	36
$\overline{WR}$	37
READY	49
$\overline{DEN}$	43
$\overline{LOCK}$	47
HOLD	45
HLDA	44

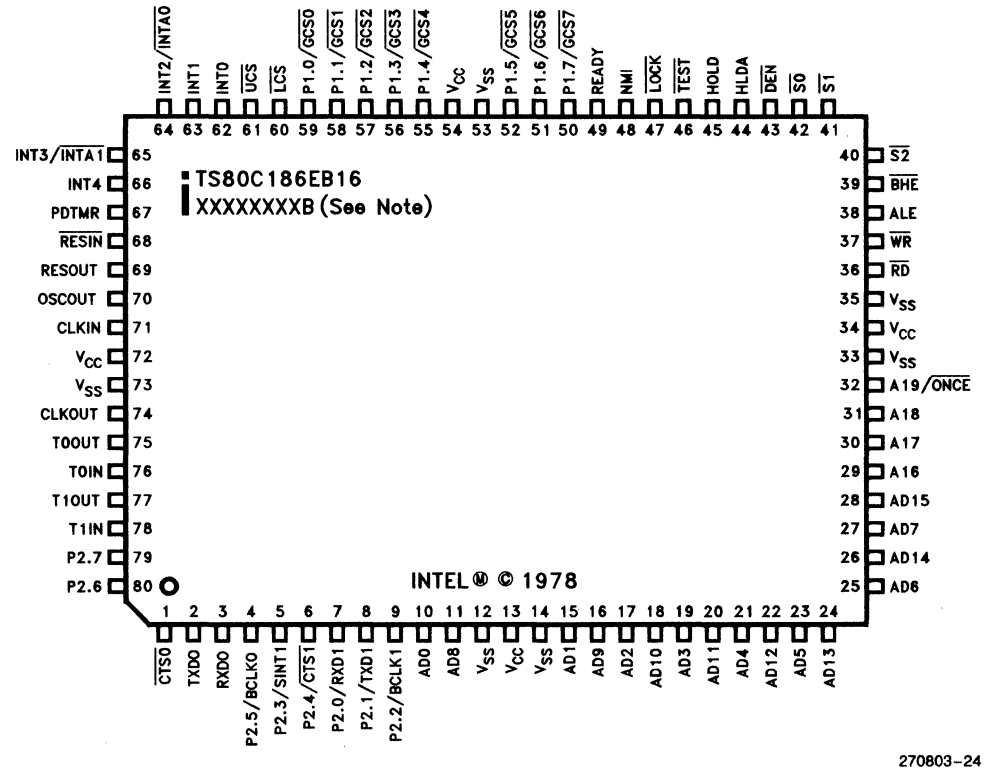
Power	
Name	**Location**
V_{SS}	12, 14, 33
	35, 53, 73
V_{CC}	13, 34
	54, 72

Processor Control	
Name	**Location**
$\overline{RESIN}$	68
RESOUT	69
CLKIN	71
OSCOUT	70
CLKOUT	74
$\overline{TEST}$	46
PDTMR	67
NMI	48
INT0	62
INT1	63
INT2/$\overline{INTA0}$	64
INT3/$\overline{INTA1}$	65
INT4	66

I/O	
Name	**Location**
$\overline{UCS}$	61
$\overline{LCS}$	60
P1.0/$\overline{GCS0}$	59
P1.1/$\overline{GCS1}$	58
P1.2/$\overline{GCS2}$	57
P1.3/$\overline{GCS3}$	56
P1.4/$\overline{GCS4}$	55
P1.5/$\overline{GCS5}$	52
P1.6/$\overline{GCS6}$	51
P1.7/$\overline{GCS7}$	50
T0OUT	75
T0IN	76
T1OUT	77
T1IN	78
RXD0	3
TXD0	2
P2.5/BCLK0	4
$\overline{CTS0}$	1
P2.0/RXD1	7
P2.1/TXD1	8
P2.2/BCLK1	9
P2.3/SINT1	5
P2.4/$\overline{CTS1}$	6
P2.6	80
P2.7	79

Table 6. QFP Package Location with Pin Names

Location	Name	Location	Name	Location	Name	Location	Name
1	$\overline{CTS0}$	21	AD4	41	$\overline{S1}$	61	$\overline{UCS}$
2	TXD0	22	AD12	42	$\overline{S0}$	62	INT0
3	RXD0	23	AD5	43	$\overline{DEN}$	63	INT1
4	P2.5/BCLK0	24	AD13	44	HLDA	64	INT2/$\overline{INTA0}$
5	P2.3/SINT1	25	AD6	45	HOLD	65	INT3/$\overline{INTA1}$
6	P2.4/$\overline{CTS1}$	26	AD14	46	$\overline{TEST}$	66	INT4
7	P2.0/RXD1	27	AD7	47	$\overline{LOCK}$	67	PDTMR
8	P2.1/TXD1	28	AD15	48	NMI	68	$\overline{RESIN}$
9	P2.2/BCLK1	29	A16	49	READY	69	RESOUT
10	AD0	30	A17	50	P1.7/$\overline{GCS7}$	70	OSCOUT
11	AD8	31	A18	51	P1.6/$\overline{GCS6}$	71	CLKIN
12	V_{SS}	32	A19/$\overline{ONCE}$	52	P1.5/$\overline{GCS5}$	72	V_{CC}
13	V_{CC}	33	V_{SS}	53	V_{SS}	73	V_{SS}
14	V_{SS}	34	V_{CC}	54	V_{CC}	74	CLKOUT
15	AD1	35	V_{SS}	55	P1.4/$\overline{GCS4}$	75	T0OUT
16	AD9	36	$\overline{RD}$	56	P1.3/$\overline{GCS3}$	76	T0IN
17	AD2	37	$\overline{WR}$	57	P1.2/$\overline{GCS2}$	77	T1OUT
18	AD10	38	ALE	58	P1.1/$\overline{GCS1}$	78	T1IN
19	AD3	39	$\overline{BHE}$	59	P1.0/$\overline{GCS0}$	79	P2.7
20	AD11	40	$\overline{S2}$	60	$\overline{LCS}$	80	P2.6



NOTE:
This is the FPO number location (indicated by X's).

Figure 6. Quad Flat Pack Pinout Diagram

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PACKAGE THERMAL SPECIFICATIONS

The 80C186EB is specified for operation when T_C (the case temperature) is within the range of −40°C to +100°C (PLCC package) or −40°C to +114°C (QFP package). T_C may be measured in any environment to determine whether the 80C186EB is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P*\theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 7 for the 84-pin Plastic Leaded Chip Carrier (PLCC) package.

Table 8 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies. P (the maximum power consumption, specified in watts) is calculated by using the maximum ICC as tabulated in the DC specifications and V_{CC} of 5.5V.

Table 7. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow Linear ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PLCC)	30	24	21	19	17	16.5
θ_{CA} (QFP)	58	47	43	40	38	36

Table 8. Maximum T_A at Various Airflows (in °C)

		Airflow Linear ft/min (m/sec)					
	T_F (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A (PLCC)	16	91.5	93.5	94	94.5	95.5	95.5
	26	88.5	91	92	92.5	93.5	93.5
	32	85	87.5	89.5	90.5	91.5	92
T_A (QFP)	16	98	101	102	103	103.5	104
	26	92	96	97.5	99	99.5	100
	32	85	90.5	92.5	94	95	96

ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	−65°C to +150°C
Case Temp Under Bias	−65°C to +120°C
Supply Voltage with respect to V_{SS}	−0.5V to +6.5V
Voltage on other Pins with respect to V_{SS}	−0.5V to V_{CC} +0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.5	5.5	V
T_F	Input Clock Frequency			
	80C186EB-20	0	40	MHz
	80C186EB-16	0	32	MHz
	80C186EB-13	0	26.08	MHz
	80C186EB	0	16	MHz
T_C	Case Temperature Under Bias			
	TN80C186EB-XX (PLCC)	−40	+100	°C
	TS80C186EB-XX (QFP)	−40	+114	°C

RECOMMENDED CONNECTIONS

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80C186EB-based circuit board should include separate power (V_{CC}) and ground (V_{SS}) planes. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "NC" must not be connected in the system. Liberal decoupling capacitance should be placed near the 80C186EB. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by placing the decoupling capacitors as close as possible to the 80C186EB V_{CC} and V_{SS} package pins.

Always connect any unused input to an appropriate signal level. In particular, unused interrupt inputs (INT0:4) should be connected to V_{CC} through a pull-up resistor (in the range of 50 KΩ). **Leave any unused output pin or any NC pin unconnected.**

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	−0.5	0.3*V_{CC}	V	
V_{IH}	Input High Voltage	0.7*V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 3 mA (Min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −2 mA (Min)
V_{HYR}	Input Hysterisis on $\overline{RESIN}$	0.50		V	
I_{LI1}	Input Leakage Current for pins: AD15:0, READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$, NMI, INT4:0, T0IN, T1IN, RXD0, $\overline{BCLK0}$, $\overline{CTS0}$, RXD1, $\overline{BCLK1}$, $\overline{CTS1}$, P2.6, P2.7		±15	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LI2}	Input Leakage Current for pins: $\overline{ERROR}$, PEREQ	±0.275	±7	mA	0V ≤ V_{IN} < V_{CC}
I_{LI3}	Input Leakage Current for pins: A19/$\overline{ONCE}$, A18:16, $\overline{LOCK}$	−0.275	−5.0	mA	V_{IN} = 0.7 V_{CC} (Note 1)
I_{LO}	Output Leakage Current		±15	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 2)
I_{CC}	Supply Current Cold (RESET) 80C186EB-20		108	mA	(Note 3)
	80C186EB-16		90	mA	(Note 3)
	80C186EB-13		73	mA	(Note 3)
	80C186EB-8		45	mA	(Note 3)
I_{ID}	Supply Current Idle 80C186EB-20		76	mA	(Note 4)
	80C186EB-16		63	mA	(Note 4)
	80C186EB-13		48	mA	(Note 4)
	80C186EB-8		31	mA	(Note 4)
I_{PD}	Supply Current Powerdown 80C186EB-20		100	μA	(Note 5)
	80C186EB-16		100	μA	(Note 5)
	80C186EB-13		100	μA	(Note 5)
	80C186EB-8		100	μA	(Note 5)
CIN	Input Pin Capacitance	0	15	pF	T_F = 1 MHz
COUT	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 6)

NOTES:
1. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
2. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
3. Measured with the device in RESET and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
4. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
5. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
6. Output Capacitance is the capacitive load of a floating output pin.

I_{CC} VERSUS FREQUENCY AND VOLTAGE

The current (I_{CC}) consumption of the 80C186EB is essentially composed of two components; I_{PD} and I_{CCS}.

I_{PD} is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or V_{CC} (no clock applied to the device). I_{PD} is equal to the Powerdown current and is typically less than 50 μA.

I_{CCS} is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since I_{CCS} is typically much greater than I_{PD}, I_{PD} can often be ignored when calculating I_{CC}.

I_{CCS} is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: V = Device operating voltage (V_{CC})

C_{DEV} = Device capacitance

f = Device operating frequency

$I_{CCS} = I_{CC}$ = Device current

Measuring C_{DEV} on a device like the 80C186EB would be difficult. Instead, C_{DEV} is calculated using the above formula by measuring I_{CC} at a known V_{CC} and frequency (see Table 9). Using this C_{DEV} value, I_{CC} can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical I_{CC} when operating at 10 MHz, 4.8V.

$$I_{CC} = I_{CCS} = 4.8 \times 0.583 \times 10 \approx 28 \text{ mA}$$

PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: t = desired delay in **seconds**

C_{PD} = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132$ μF is required. Round up to standard (available) capacitive values.

NOTE:
The above equation applies to delay times greater than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperature will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

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Table 9. Device Capacitance (C_{DEV}) Values

Parameter	Typ	Max	Units	Notes
C_{DEV} (Device in Reset)	0.583	1.02	mA/V*MHz	1, 2
C_{DEV} (Device in Idle)	0.408	0.682	mA/V*MHz	1, 2

1. Max C_{DEV} is calculated at −40°C, all floating outputs driven to V_{CC} or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical C_{DEV} is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

AC SPECIFICATIONS

AC Characteristics—80C186EB-20

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	40	MHz	1
T_C	CLKIN Period	25	∞	ns	1
T_{CH}	CLKIN High Time	10	∞	ns	1, 2
T_{CL}	CLKIN Low Time	10	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	17	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	20	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	3	25	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	20	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	3	25	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD15:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD15:0	3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, $\overline{ERROR}$	10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, $\overline{ERROR}$	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C186EB operation.

AC SPECIFICATIONS (Continued)

AC Characteristics—80C186EB-16

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	32	MHz	1
T_C	CLKIN Period	31.25	∞	ns	1
T_{CH}	CLKIN High Time	10	∞	ns	1, 2
T_{CL}	CLKIN Low Time	10	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	20	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	22	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	3	27	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	22	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	3	27	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD15:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD15:0	3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, $\overline{ERROR}$	10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, $\overline{ERROR}$	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C186EB operation.

AC SPECIFICATIONS (Continued)

AC Characteristics—80C186EB-13

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	26.08	MHz	1
T_C	CLKIN Period	38.34	∞	ns	1
T_{CH}	CLKIN High Time	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	23	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	25	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	3	30	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	25	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	3	30	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD15:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD15:0	3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, $\overline{ERROR}$	10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, $\overline{ERROR}$	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C186EB operation.

AC SPECIFICATIONS (Continued)

AC Characteristics—80C186EB-8

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	16	MHz	1
T_C	CLKIN Period	62.5	∞	ns	1
T_{CH}	CLKIN High Time	15	∞	ns	1, 2
T_{CL}	CLKIN Low Time	15	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	27	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	30	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	3	35	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	30	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	3	35	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	35	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD15:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD15:0	3		ns	1, 10
T_{CLIS}	HOLD, PEREQ, $\overline{ERROR}$	10		ns	1, 9
T_{CLIH}	HOLD, PEREQ, $\overline{ERROR}$	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C186EB operation.

AC SPECIFICATIONS (Continued)

Relative Timings (80C186EB-20, -16, -13, -8)

Symbol	Parameter	Min	Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Rising to ALE Falling	T − 15		ns	
T_{AVLL}	Address Valid to ALE Falling	½T − 10		ns	
T_{PLLL}	Chip Selects Valid to ALE Falling	½T − 10		ns	1
T_{LLAX}	Address Hold from ALE Falling	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{WHLH}	$\overline{WR}$ Rising to ALE Rising	½T − 10		ns	1
T_{AFRL}	Address Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Falling to $\overline{RD}$ Rising	(2*T) − 5		ns	2
T_{WLWH}	$\overline{WR}$ Falling to $\overline{WR}$ Rising	(2*T) − 5		ns	2
T_{RHAV}	$\overline{RD}$ Rising to Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHPH}	$\overline{WR}$ Rising to Chip Select Rising	½T − 10		ns	1
T_{RHPH}	$\overline{RD}$ Rising to Chip Select Rising	½T − 10		ns	1
T_{PHPL}	$\overline{CS}$ Inactive to $\overline{CS}$ Active	½T − 10		ns	1
T_{OVRH}	$\overline{ONCE}$ Active to $\overline{RESIN}$ Rising	T		ns	3
T_{RHOX}	$\overline{ONCE}$ Hold from $\overline{RESIN}$ Rising	T		ns	3

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Not tested.

AC SPECIFICATIONS (Continued)

Serial Port Mode 0 Timings (80C186EB-20, 16, -13, -8)

Symbol	Parameter	Min	Max	Unit	Notes
T_{XLXL}	TXD Clock Period	T (n + 1)		ns	1, 2
T_{XLXH}	TXD Clock Low to Clock High (n > 1)	2T − 35	2T + 35	ns	1
T_{XLXH}	TXD Clock Low to Clock High (n = 1)	T − 35	T + 35	ns	1
T_{XHXL}	TXD Clock High to Clock Low (n > 1)	(n − 1) T − 35	(n − 1) T + 35	ns	1, 2
T_{XHXL}	TXD Clock High to Clock Low (n = 1)	T − 35	T + 35	ns	1
T_{QVXH}	RXD Output Data Setup to TXD Clock High (n > 1)	(n − 1) T − 35		ns	1, 2
T_{QVXH}	RXD Output Data Setup to TXD Clock High (n = 1)	T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (n > 1)	2T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (n = 1)	T − 35		ns	1
T_{XHQZ}	RXD Output Data Float after Last TXD Clock High		T + 20	ns	1
T_{DVXH}	RXD Input Data Setup to TXD Clock High	T + 20		ns	1
T_{XHDX}	RXD Input Data Hold after TXD Clock High	0		ns	1

NOTES:
1. See Figure 12 for waveforms.
2. n is the value of the BxCMP register ignoring the ICLK Bit (i.e., ICLK = 0).

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 7. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

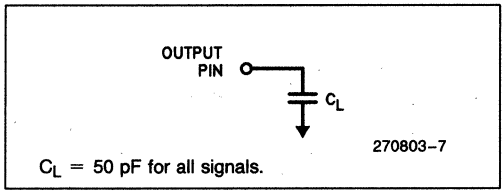


Figure 7. AC Test Load

AC TIMING WAVEFORMS

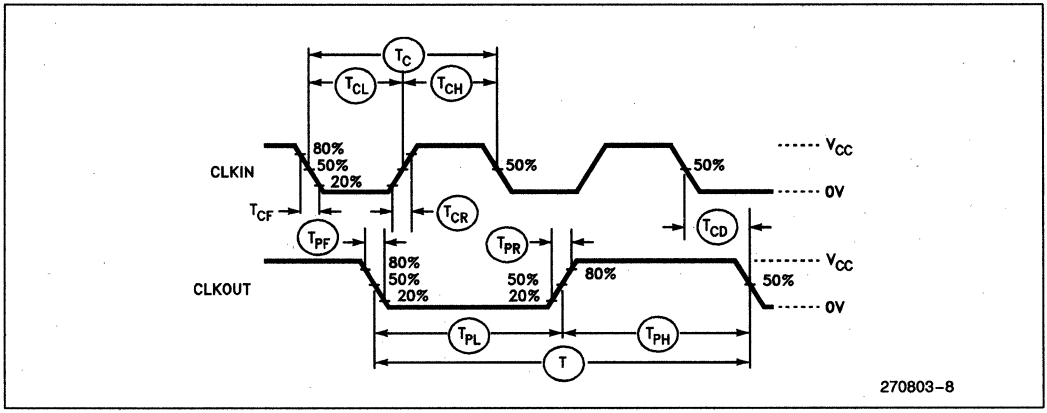
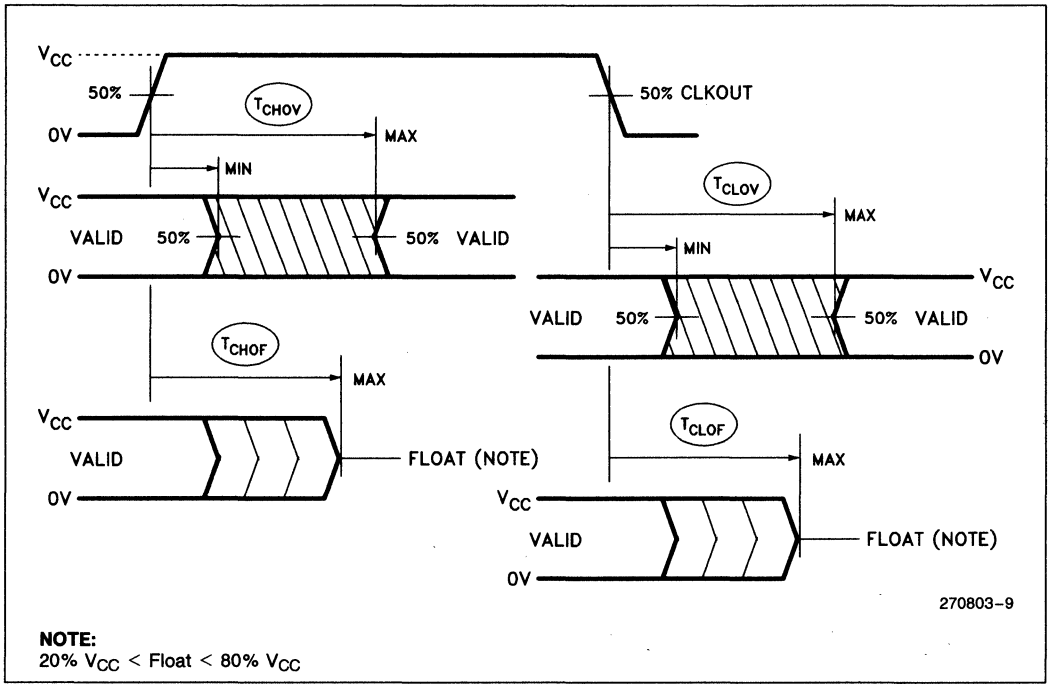


Figure 8. Input and Output Clock Waveform



NOTE:
20% V_{CC} < Float < 80% V_{CC}

Figure 9. Output Delay and Float Waveform

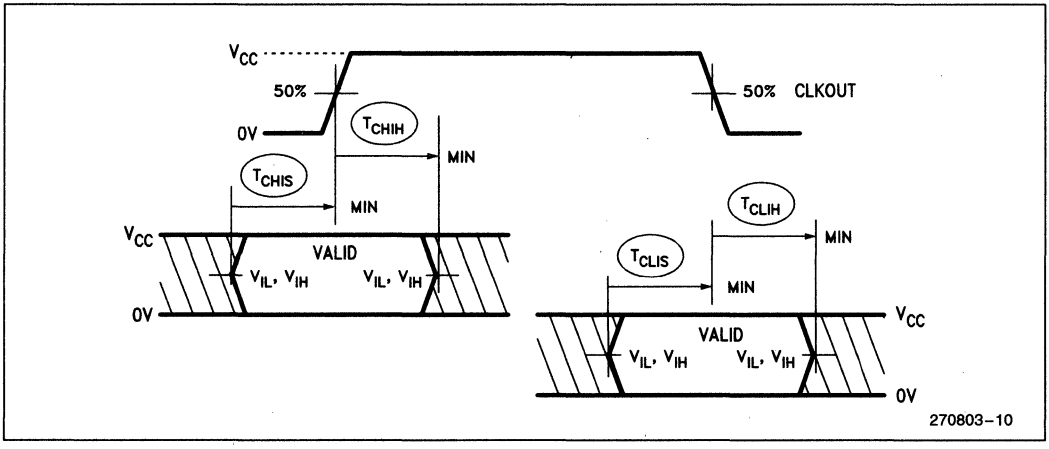


Figure 10. Input Setup and Hold

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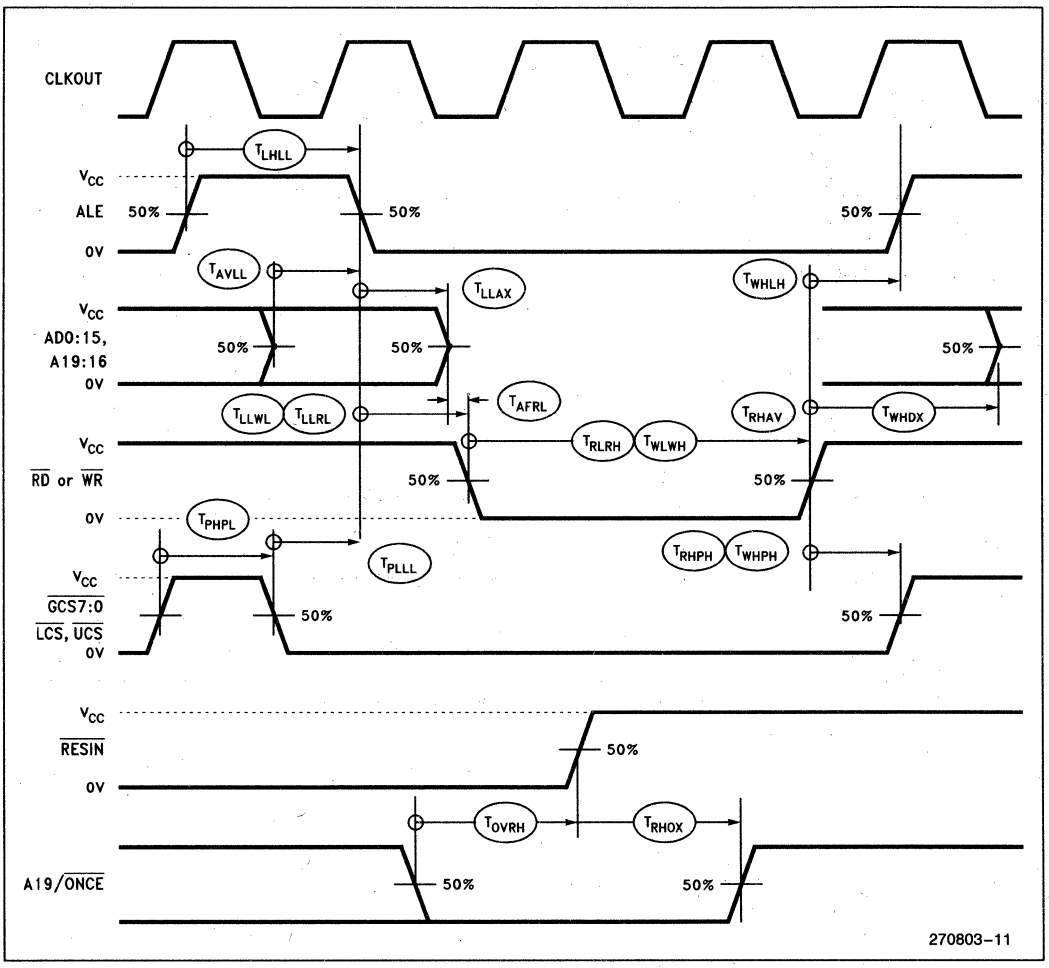

Figure 11. Relative Signal Waveform

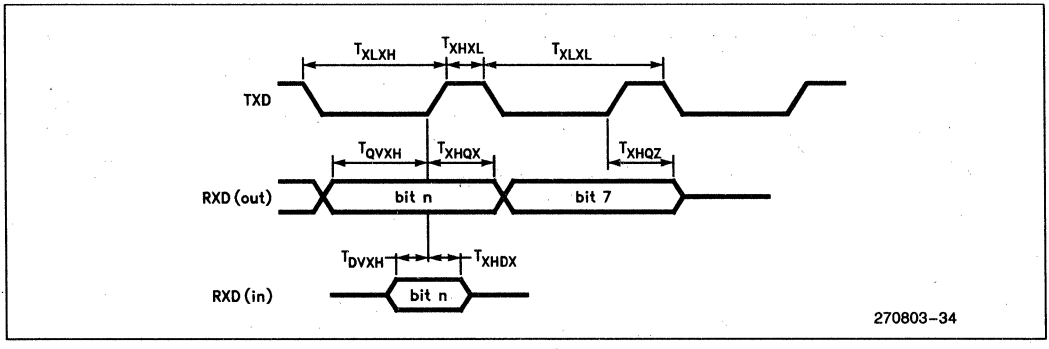

Figure 12. Serial Port Mode 0 Waveform

DERATING CURVES

TYPICAL OUTPUT DELAY VARIATIONS VERSUS LOAD CAPACITANCE

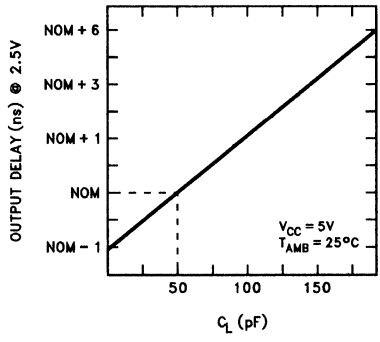

Figure 13

TYPICAL RISE AND FALL VARIATIONS VERSUS LOAD CAPACITANCE

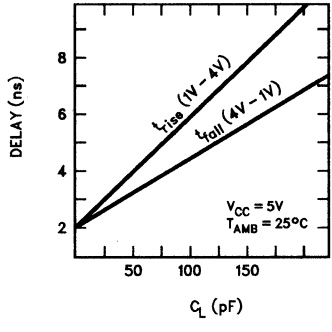

Figure 14

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RESET

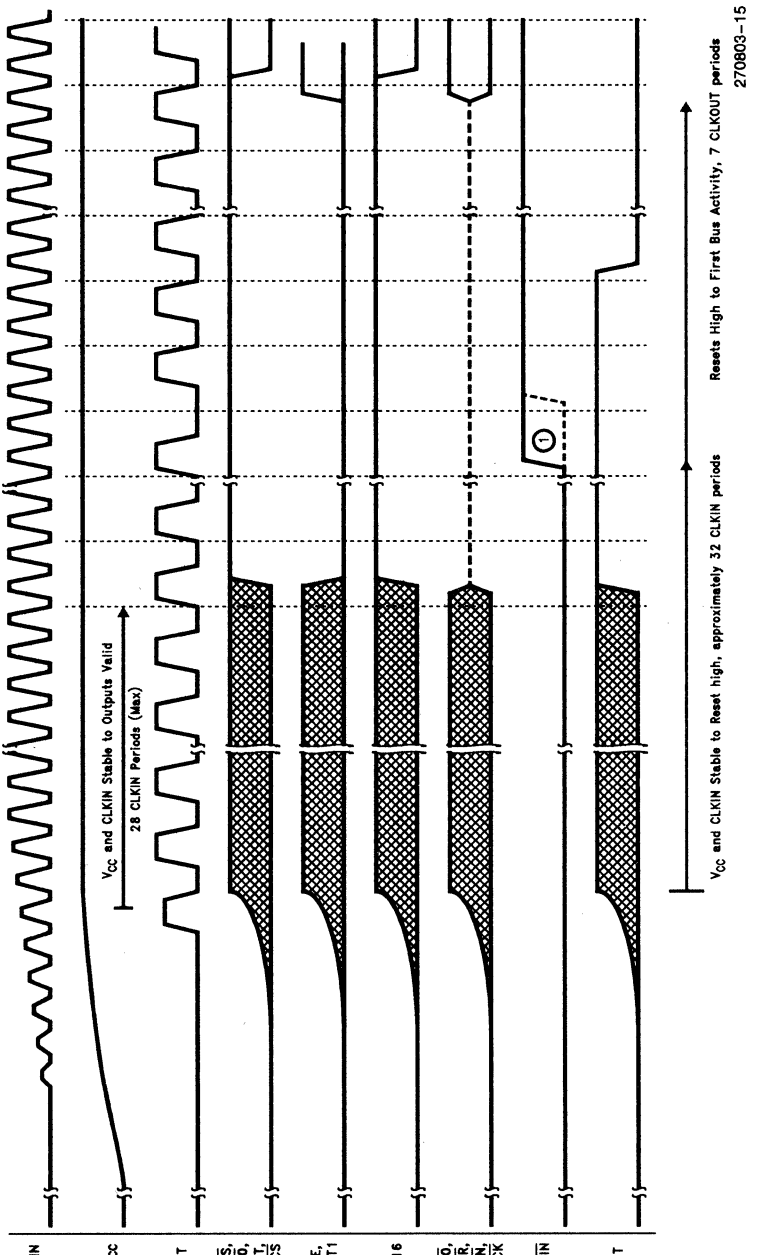
The 80C186EB will perform a reset operation any time the $\overline{RESIN}$ pin active. The $\overline{RESIN}$ pin is actually synchronized before it is presented internally, which means that the clock must be operating before a reset can take effect. From a power-on state, $\overline{RESIN}$ must be held active (low) in order to guarantee correct initialization of the 80C186EB. **Failure to provide $\overline{RESIN}$ while the device is powering up will result in unspecified operation of the device.**

Figure 15 shows the correct reset sequence when first applying power to the 80C186EB. An external clock connected to CLKIN must not exceed the V_{CC} threshold being applied to the 80C186EB. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the 80C186EB. When attaching a crystal to the device, $\overline{RESIN}$ must remain active until both V_{CC} and CLKOUT are stable (the length of time is application specific and depends on the startup characteristics of the crystal circuit). The $\overline{RESIN}$ pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that $\overline{RESIN}$ is never really sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Figure 16 shows the timing sequence when $\overline{RESIN}$ is applied after V_{CC} is stable and the device has been operating. Note that a reset will terminate all activity and return the 80C186EB to a known operating state. Any bus operation that is in progress at the time $\overline{RESIN}$ is asserted will terminate immediately (note that most control signals will be driven to their inactive state first before floating).

While $\overline{RESIN}$ is active, bus signals $\overline{LOCK}$, A19/$\overline{ONCE}$, and A18:16 are configured as inputs and weakly held high by internal pullup transistors. Only 19/$\overline{ONCE}$ can be overdriven to a low and is used to enable $\overline{ONCE}$ Mode. Forcing $\overline{LOCK}$ or A18:16 low at any time while $\overline{RESIN}$ is low is prohibited and will cause unspecified device operation.

COLD RESET WAVEFORMS



NOTE:
CLKOUT synchronization occurs on the rising edge of RESIN. If RESIN is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If RESIN is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.

Figure 15

WARM RESET WAVEFORMS

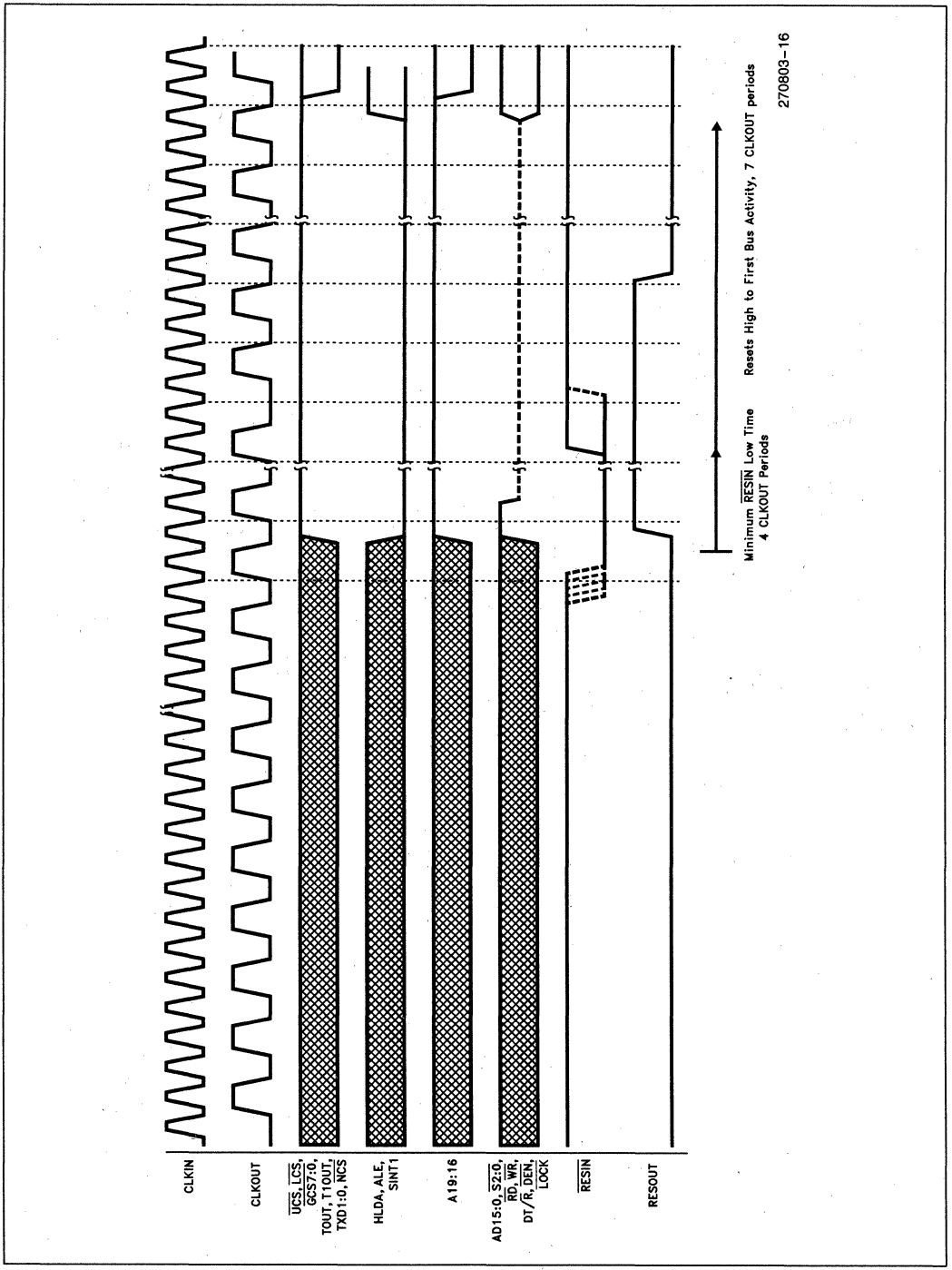


Figure 16

BUS CYCLE WAVEFORMS

Figures 17 through 23 present the various bus cycles that are generated by the 80C186EB. What is shown in the figure is the relationship of the various bus signals to CLKOUT. These figures along with the information present in **AC Specifications** allow the user to determine all the critical timing analysis needed for a given application.

MEMORY READ, I/O READ, INSTRUCTION FETCH, AND REFRESH WAVEFORM

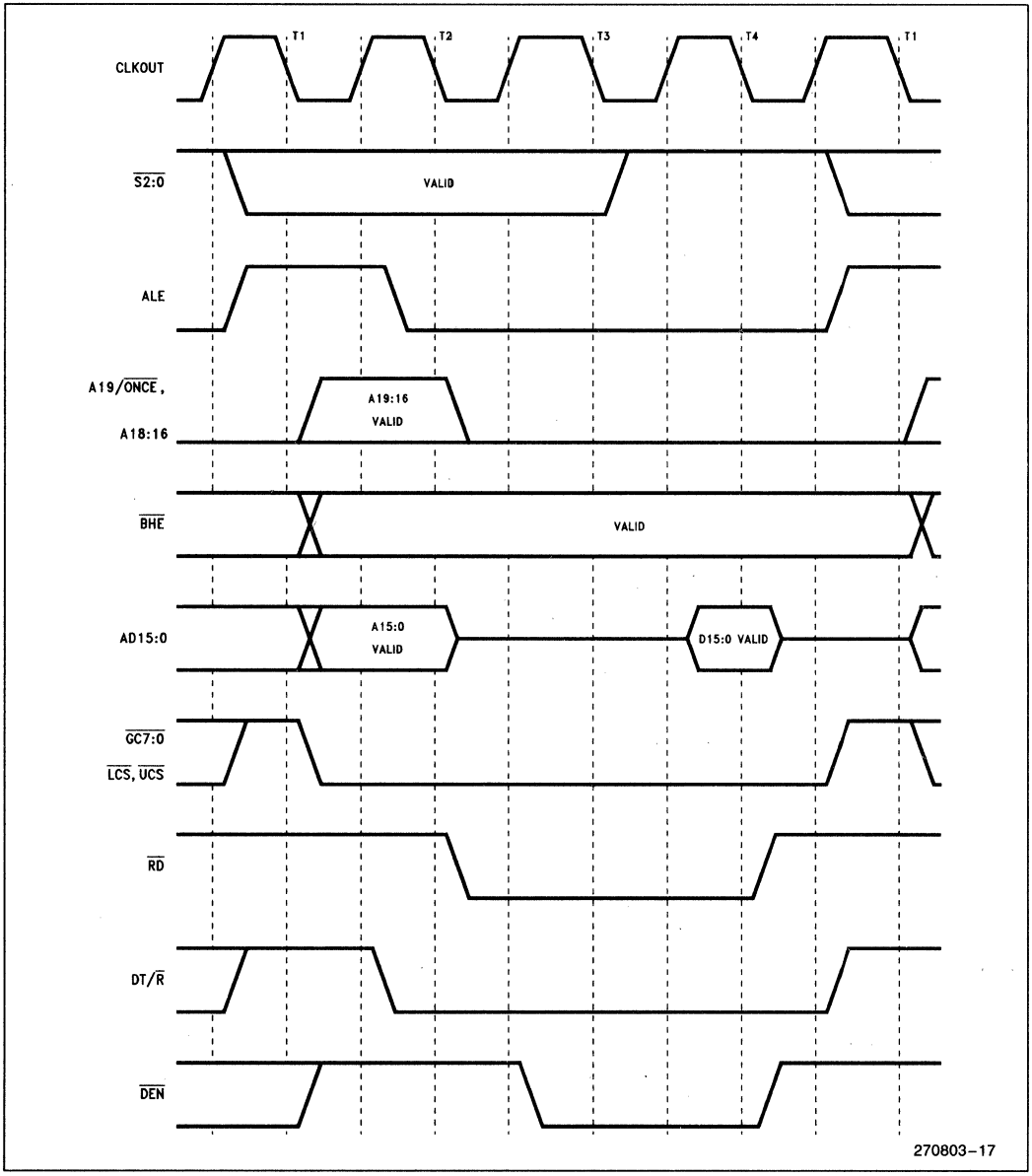


Figure 17

MEMORY WRITE AND I/O WRITE CYCLE WAVEFORM

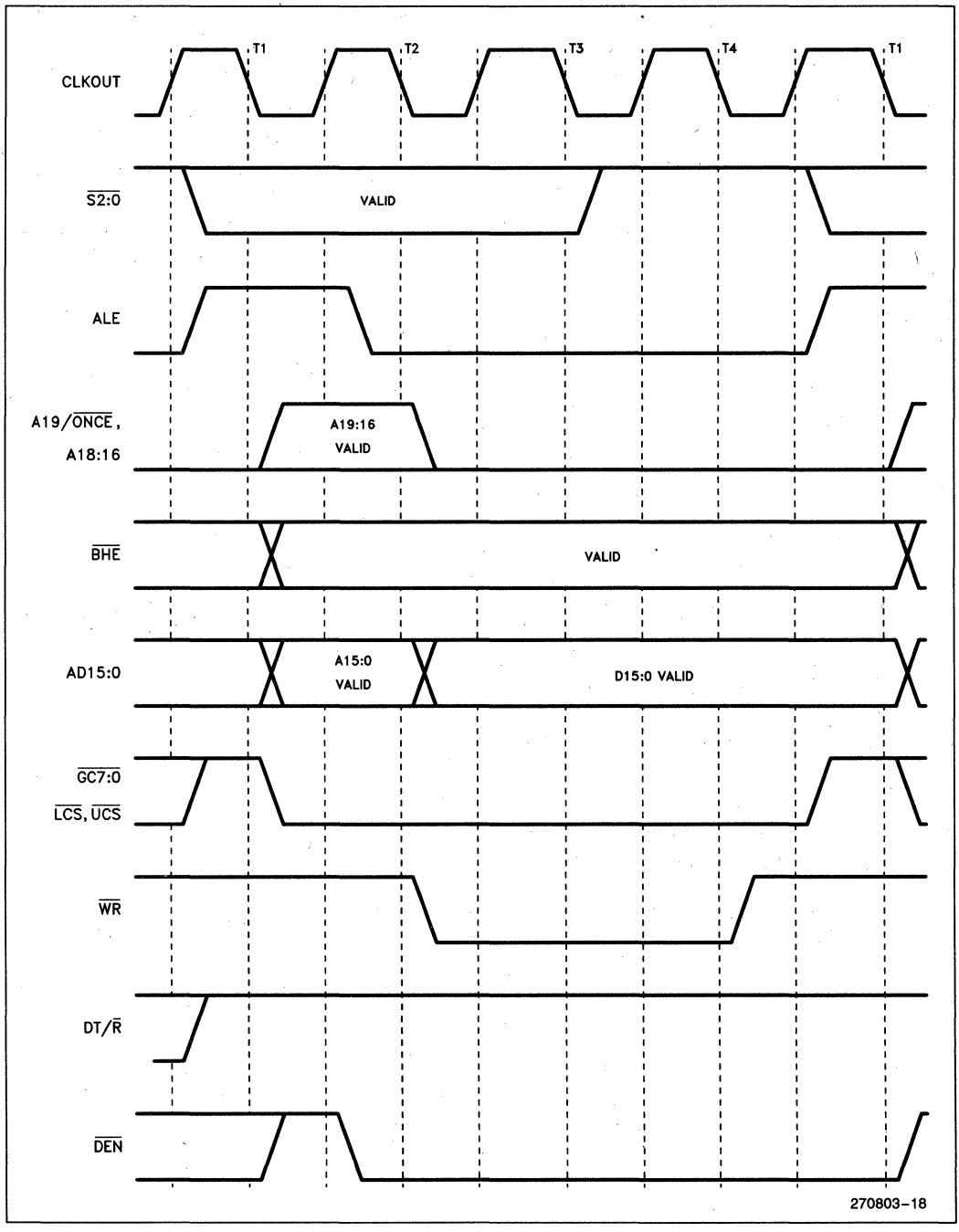
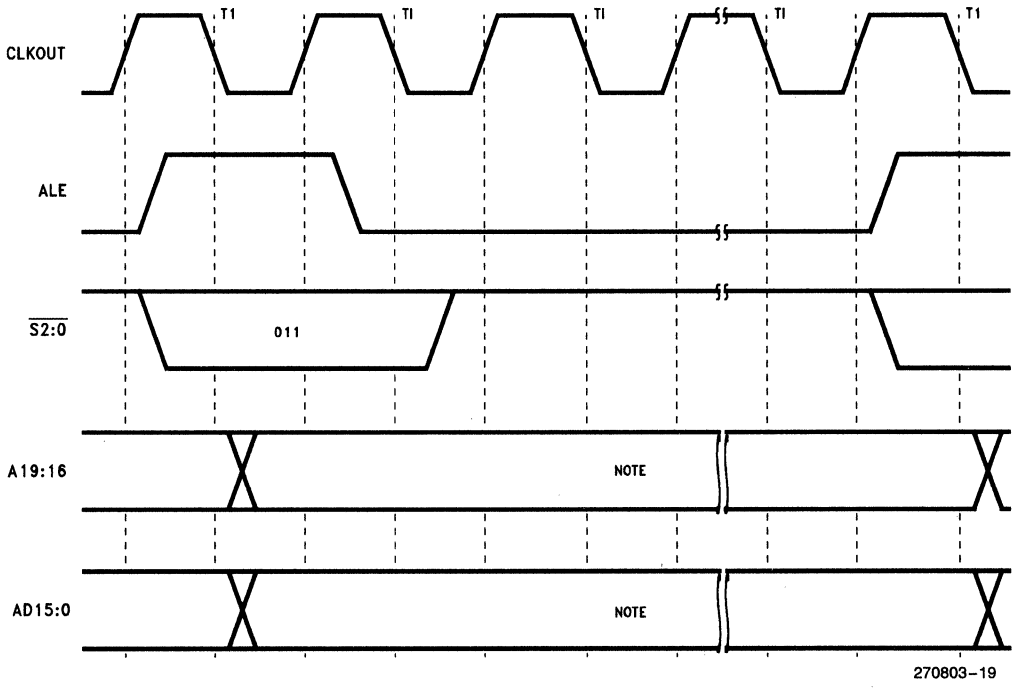


Figure 18

HALT CYCLE WAVEFORM



NOTE:
The address driven is typically the location of the next instruction prefetch. Under a majority of instruction sequences the AD15:0 bus will float, while the A19:16 bus remains driven and all bus control signals are driven to their inactive state.

Figure 19

CASCADE MODE INTERRUPT ACKNOWLEDGE CYCLE WAVEFORM

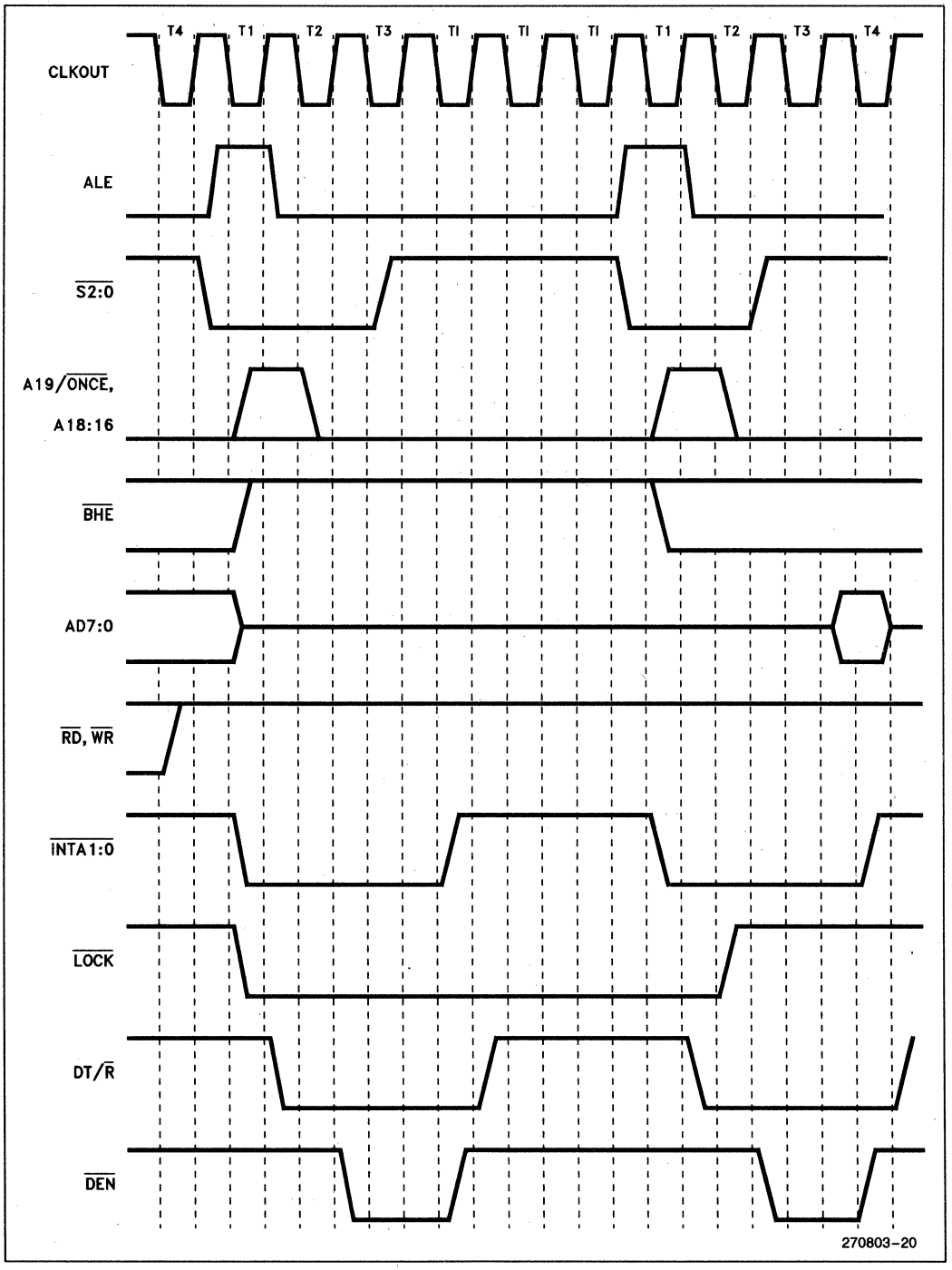


Figure 20

HOLD/HLDA CYCLE WAVEFORMS

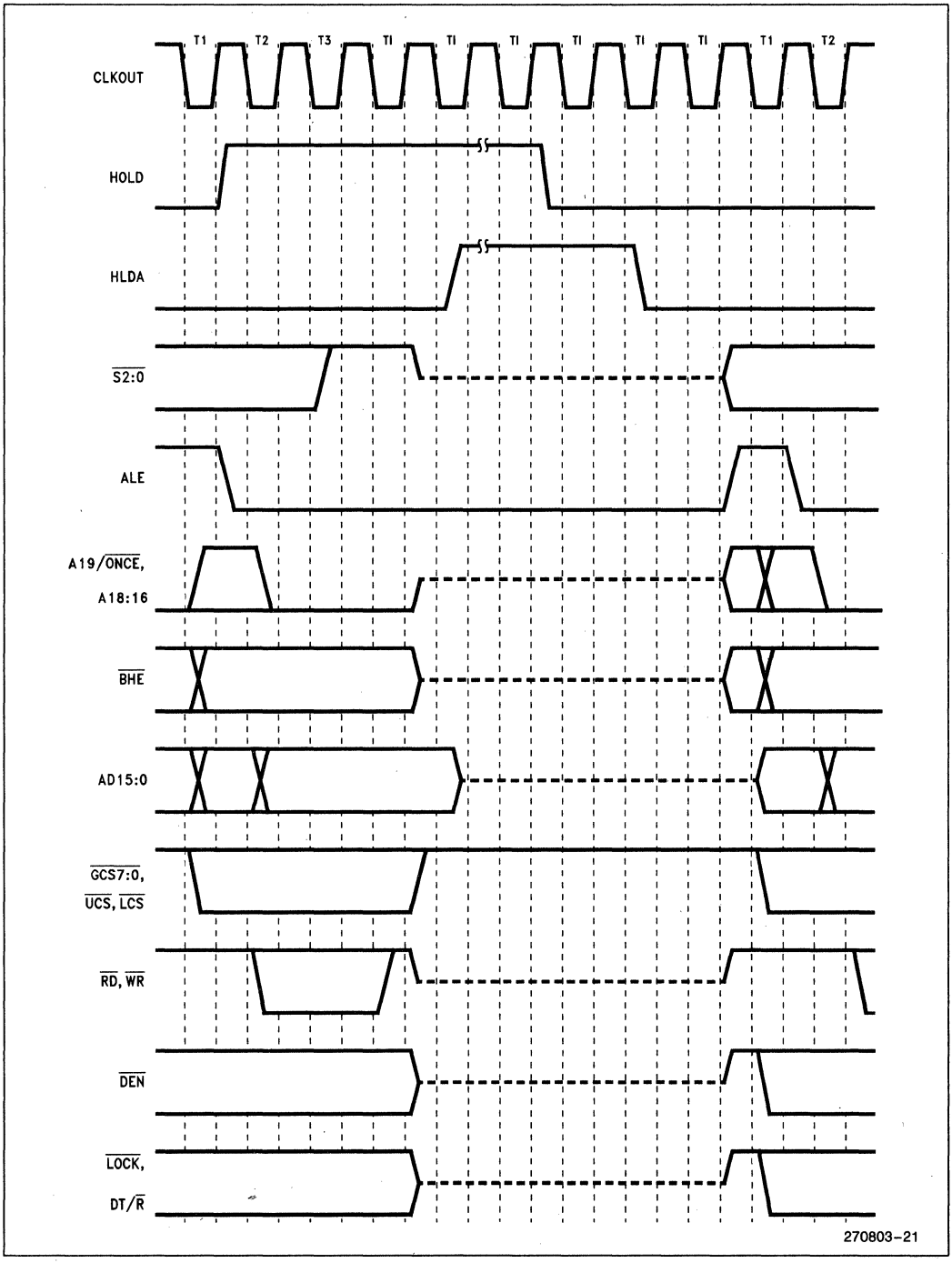
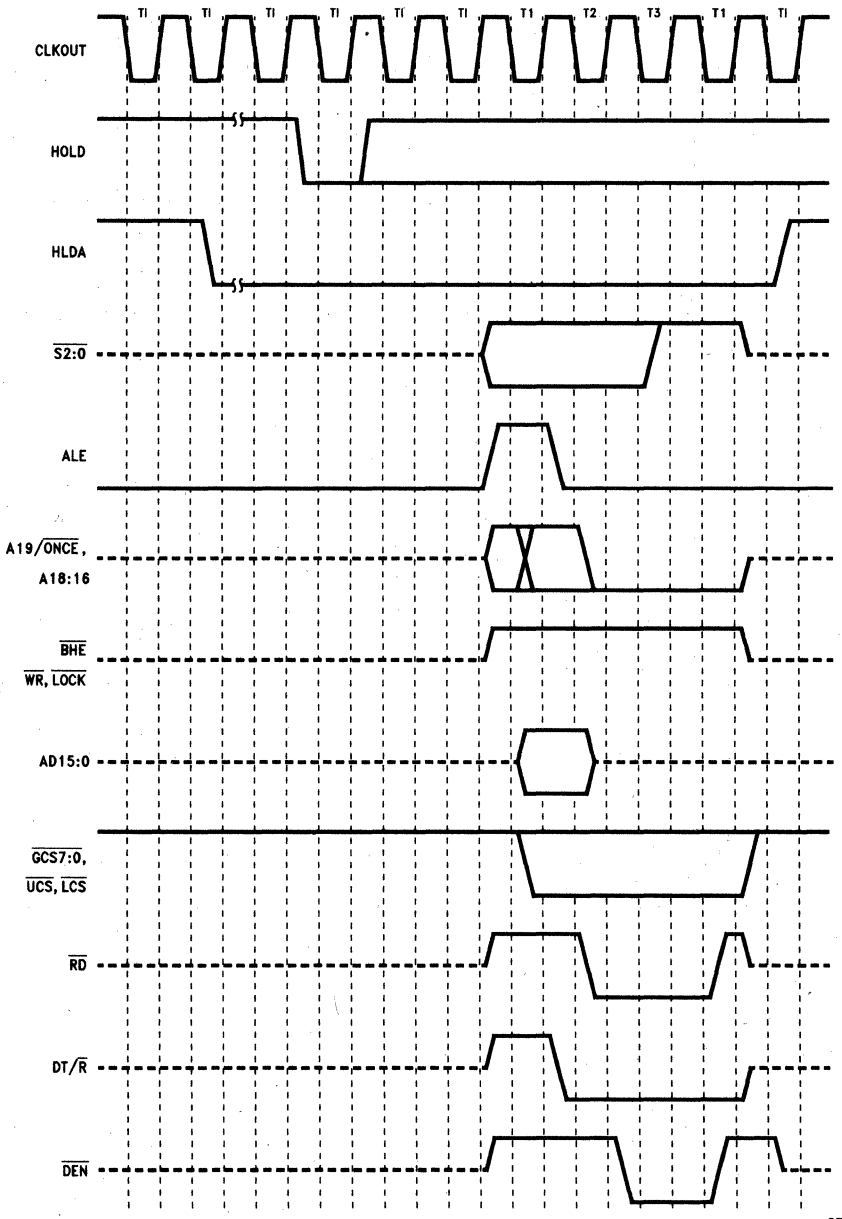


Figure 21

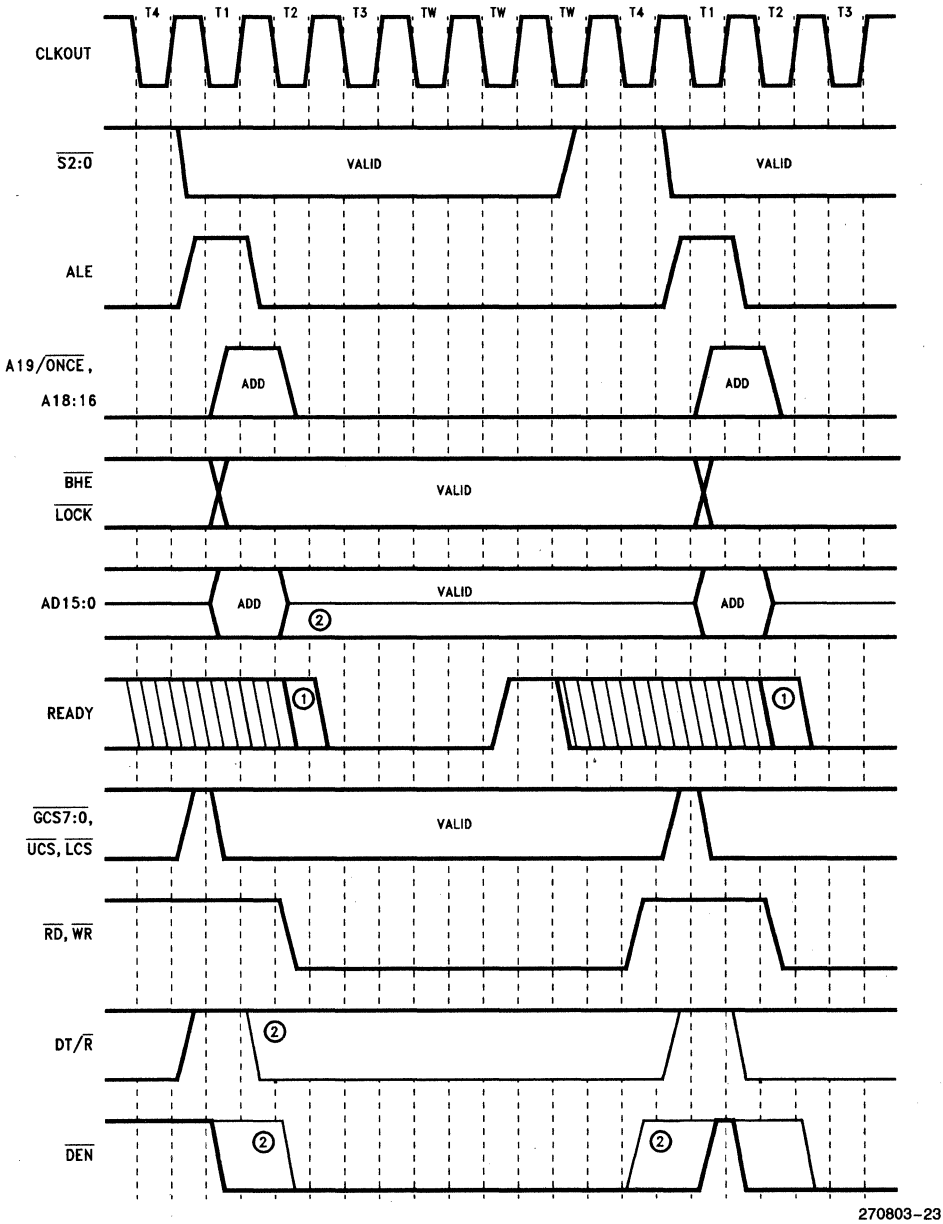
REFRESH DURING HLDA CYCLE WAVEFORM



NOTES:
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.

Figure 22

READY CYCLE WAVEFORM



NOTES:
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.

Figure 23

REGISTER BIT SUMMARY

Figures 24 through 31 present the bit definition of each register that is active (not reserved) in the Peripheral Control Block (PCB). Each register can be thought to occupy one word (16-bits) of either memory or I/O space, although not all bits in the register necessarily have a function. A register bit is **not** guaranteed to return a specific logic value if an "X" appears for the bit definition (i.e., if a zero was written to the register bit it may not be returned as a zero when read). Furthermore, a 0 must be written to any bit that is indicated by an "X" to ensure compatibility with future products or potential product changes.

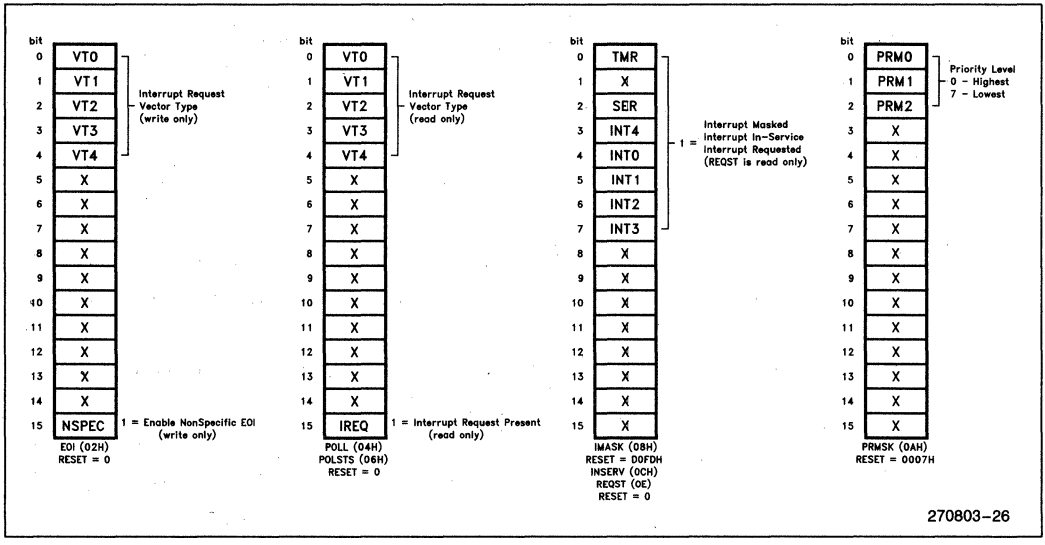


Figure 24. Interrupt Control Unit Registers

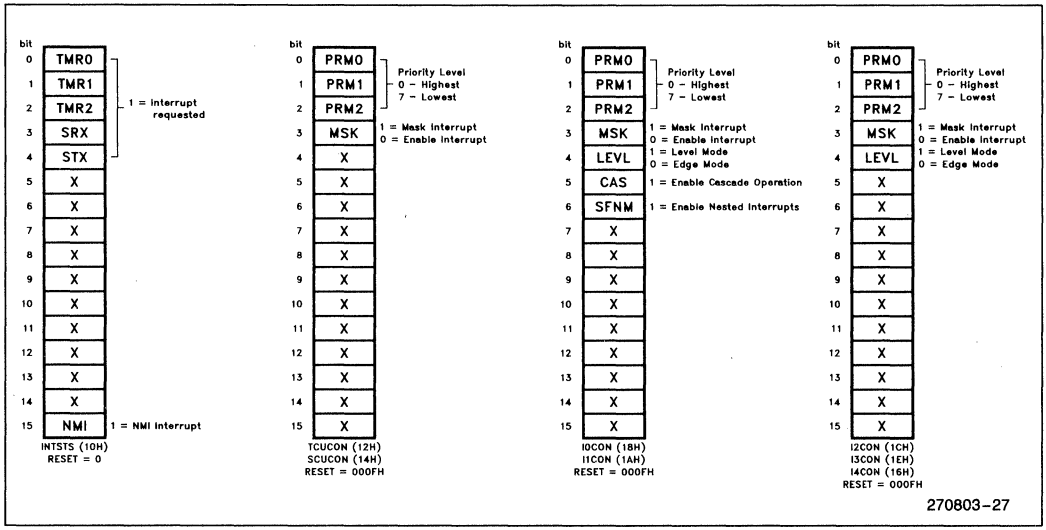


Figure 25. Interrupt Control Unit Registers

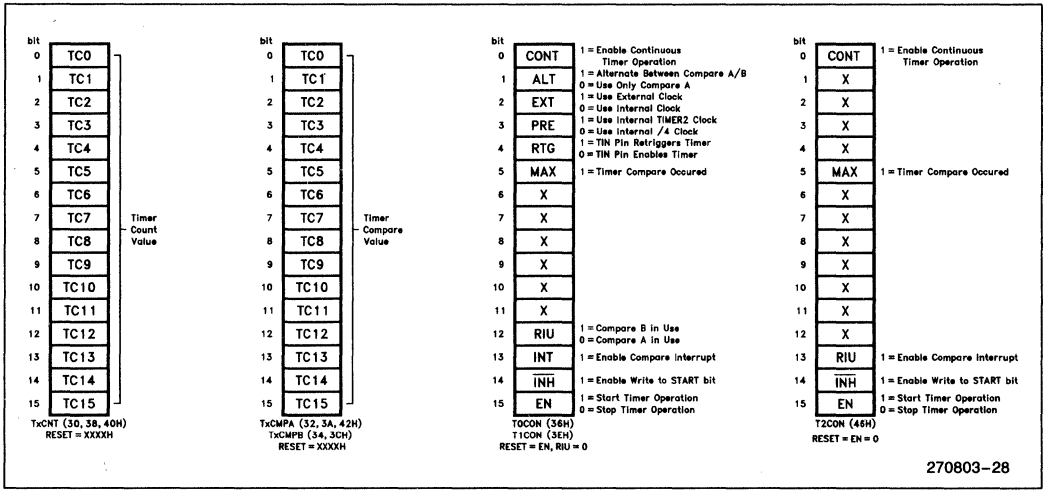


Figure 26. Timer Control Unit Registers

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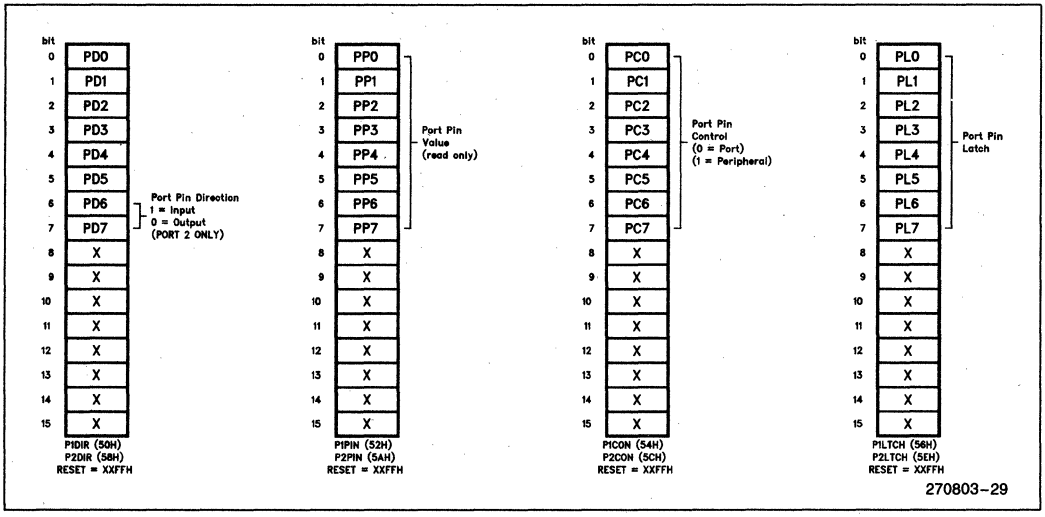

Figure 27. I/O Port Unit Registers

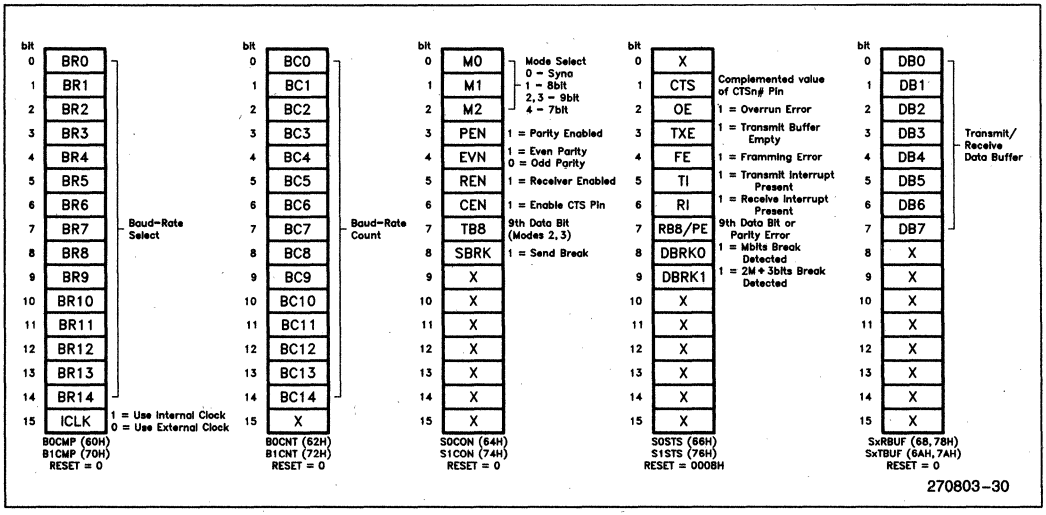

Figure 28. Serial Communications Unit Registers

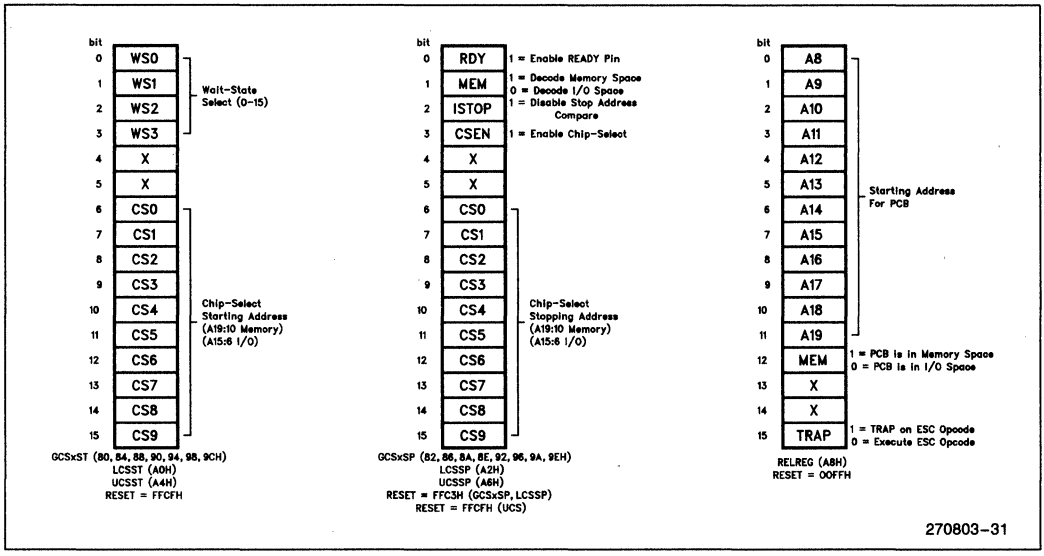

Figure 29. Chip-Select Unit Registers

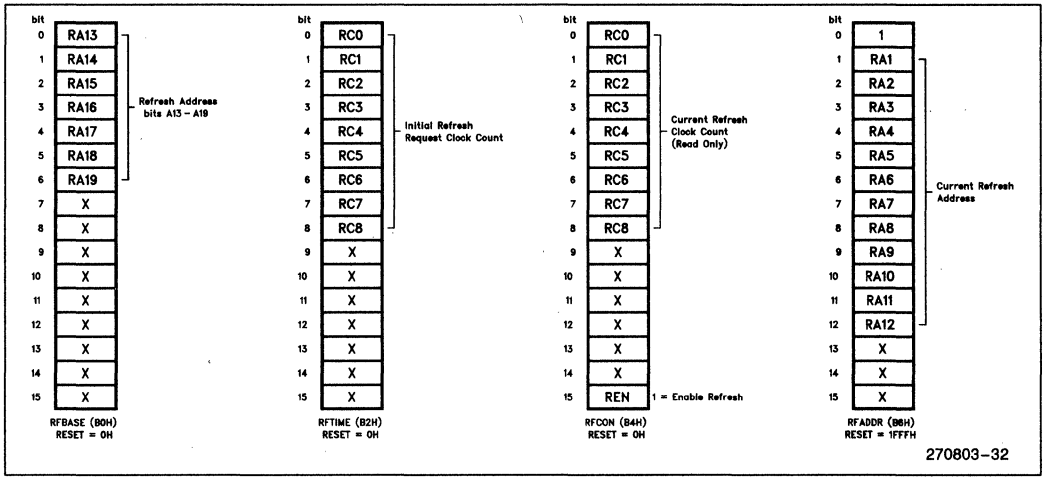

Figure 30. Refresh Control Unit Registers

24

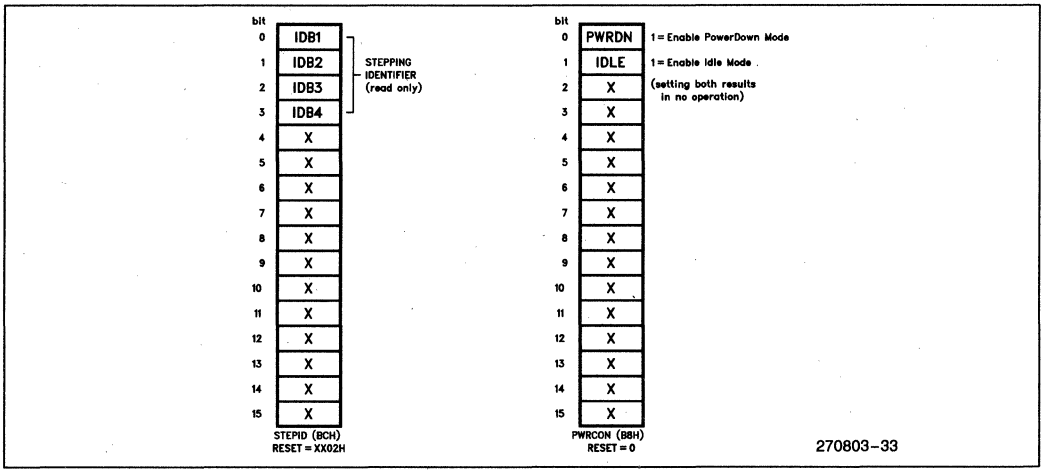

Figure 31. Power Management Unit Registers

80C186EB EXECUTION TIMINGS

A determination of 80C186EB program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the **minimum** execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the 80C186EB has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1000100w	mod reg r/m			2/12	
Register/memory to register	1000101w	mod reg r/m			2/9	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12-13	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3-4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8	
Accumulator to memory	1010001w	addr-low	addr-high		9	
Register/memory to segment register	10001110	mod 0 reg r/m			2/9	
Segment register to register/memory	10001100	mod 0 reg r/m			2/11	
PUSH = Push:						
Memory	11111111	mod 1 1 0 r/m			16	
Register	01010 reg				10	
Segment register	000reg110				9	
Immediate	011010s0	data	data if s=0		10	
PUSHA = Push All	01100000				36	
POP = Pop:						
Memory	10001111	mod 0 0 0 r/m			20	
Register	01011 reg				10	
Segment register	000reg111	(reg≠01)			8	
POPA = Pop All	01100001				51	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10	
Variable port	1110110w				8	
OUT = Output to:						
Fixed port	1110011w	port			9	
Variable port	1110111w				7	
XLAT = Translate byte to AL	11010111				11	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		18	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		18	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				9	
POPF = Pop flags	10011101				8	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

24

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if sw=01	4/16	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	4/16	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	4/16	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if sw=01	4/16	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10	
Register with register/memory	0011100w	mod reg r/m			3/10	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	3/10	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26-28	
Register-Word					35-37	
Memory-Byte					32-34	
Memory-Word					41-43	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
ARITHMETIC (Continued)			
IMUL = Integer multiply (signed):	1111011w | mod101 r/m		
Register-Byte		25–28	
Register-Word		34–37	
Memory-Byte		31–34	
Memory-Word		40–43	
IMUL = Integer Immediate multiply (signed)	011010s1 | mod reg r/m | data | data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w | mod110 r/m		
Register-Byte		29	
Register-Word		38	
Memory-Byte		35	
Memory-Word		44	
IDIV = Integer divide (signed):	1111011w | mod111 r/m		
Register-Byte		44–52	
Register-Word		53–61	
Memory-Byte		50–58	
Memory-Word		59–67	
AAM = ASCII adjust for multiply	11010100 | 00001010	19	
AAD = ASCII adjust for divide	11010101 | 00001010	15	
CBW = Convert byte to word	10011000	2	
CWD = Convert word to double word	10011001	4	
LOGIC			
Shift/Rotate Instructions:			
Register/Memory by 1	1101000w | mod TTT r/m	2/15	
Register/Memory by CL	1101001w | mod TTT r/m	5+n/17+n	
Register/Memory by Count	1100000w | mod TTT r/m | count	5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR		
AND = **And:**			
Reg/memory and register to either	001000dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod100 r/m | data | data if w=1	4/16	
Immediate to accumulator	0010010w | data | data if w=1	3/4	8/16-bit
TEST = **And function to flags, no result:**			
Register/memory and register	1000010w | mod reg r/m	3/10	
Immediate data and register/memory	1111011w | mod000 r/m | data | data if w=1	4/10	
Immediate data and accumulator	1010100w | data | data if w=1	3/4	8/16-bit
OR = **Or:**			
Reg/memory and register to either	000010dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod001 r/m | data | data if w=1	4/16	
Immediate to accumulator	0000110w | data | data if w=1	3/4	8/16-bit

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
XOR = Exclusive or:						
Reg/memory and register to either	001100dw	mod reg r/m			3/10	
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	4/16	
Immediate to accumulator	0011010w	data	data if w=1		3/4	8/16-bit
NOT = Invert register/memory	1111011w	mod 010 r/m			3/10	
STRING MANIPULATION						
MOVS = Move byte/word	1010010w				14	
CMPS = Compare byte/word	1010011w				22	
SCAS = Scan byte/word	1010111w				15	
LODS = Load byte/wd to AL/AX	1010110w				12	
STOS = Store byte/wd from AL/AX	1010101w				10	
INS = Input byte/wd from DX port	0110110w				14	
OUTS = Output byte/wd to DX port	0110111w				14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	11110010	1010010w			8+8n	
CMPS = Compare string	1111001z	1010011w			5+22n	
SCAS = Scan string	1111001z	1010111w			5+15n	
LODS = Load string	11110010	1010110w			6+11n	
STOS = Store string	11110010	1010101w			6+9n	
INS = Input string	11110010	0110110w			8+8n	
OUTS = Output string	11110010	0110111w			8+8n	
CONTROL TRANSFER						
CALL = Call:						
Direct within segment	11101000	disp-low	disp-high		15	
Register/memory indirect within segment	11111111	mod 010 r/m			13/19	
Direct intersegment	10011010	segment offset			23	
		segment selector				
Indirect intersegment	11111111	mod 011 r/m	(mod ≠ 11)		38	
JMP = Unconditional jump:						
Short/long	11101011	disp-low			14	
Direct within segment	11101001	disp-low	disp-high		14	
Register/memory indirect within segment	11111111	mod 100 r/m			11/17	
Direct intersegment	11101010	segment offset			14	
		segment selector				
Indirect intersegment	11111111	mod 101 r/m	(mod ≠ 11)		26	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
RET = **Return from CALL:**						
Within segment	11000011				16	
Within seg adding immed to SP	11000010	data-low	data-high		18	
Intersegment	11001011				22	
Intersegment adding immediate to SP	11001010	data-low	data-high		25	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110 000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22 + 16(n − 1)	
LEAVE = Leave Procedure	11001001				8	
INT = **Interrupt:**						
Type specified	11001101	type			47	
Type 3	11001100				45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110				48/4	
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33–35	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	
	(TTT LLL are opcode to processor extension)		

Shaded areas indicate instructions not available in 8086/8088 microsystems.

FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

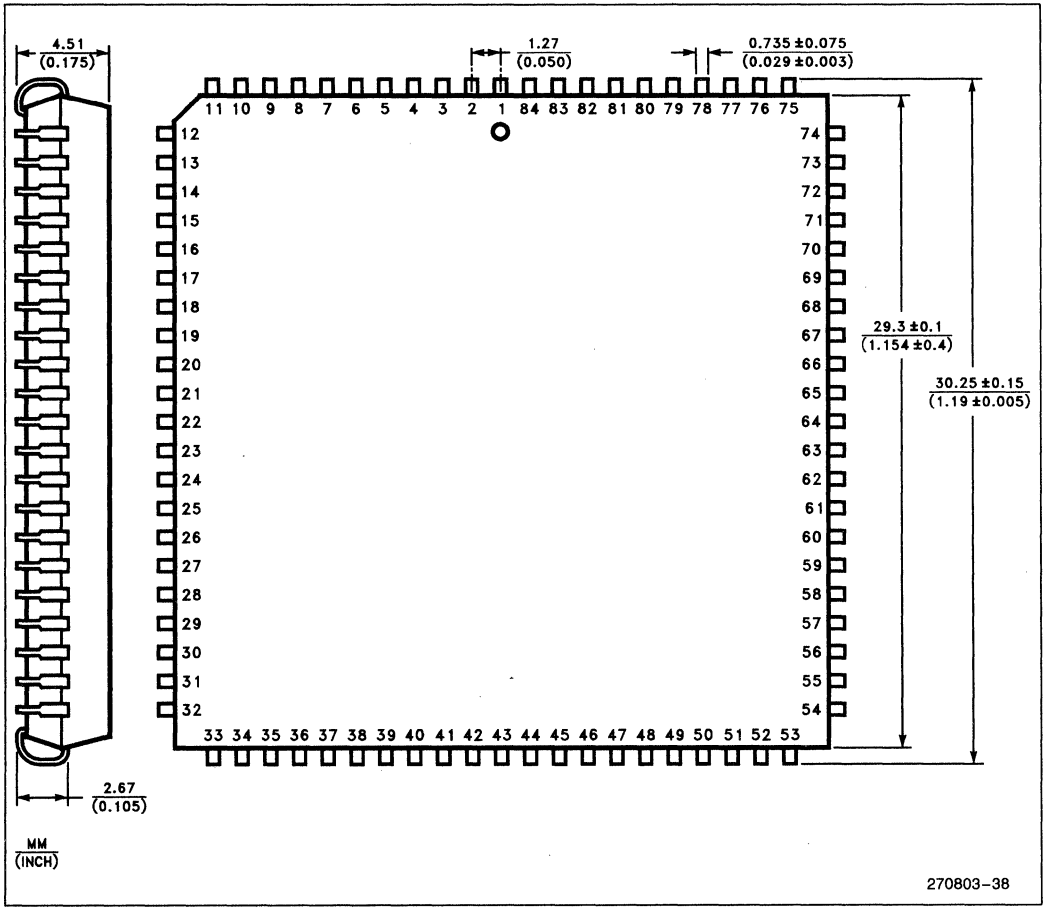

Figure 32. PLCC Principal Dimensions

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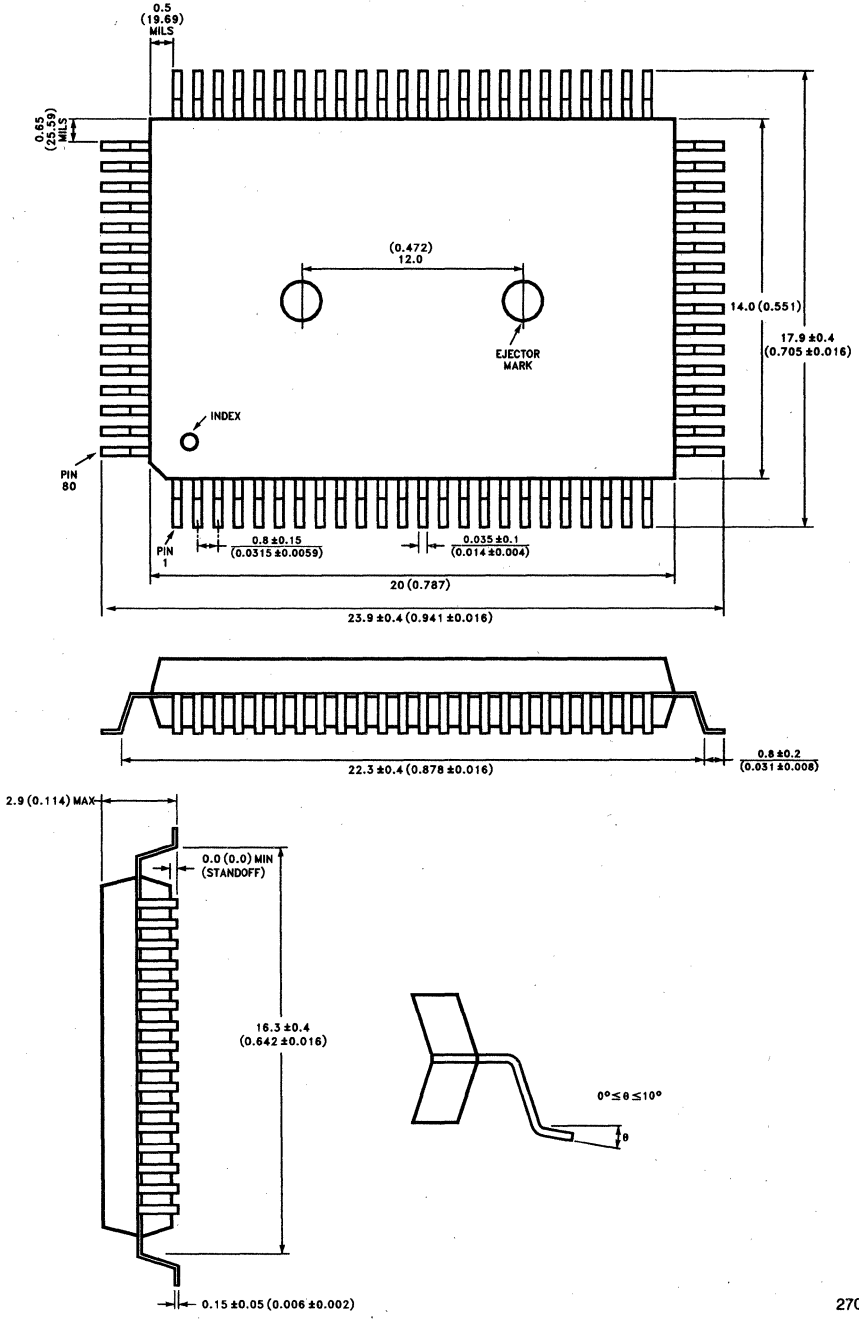

NOTE:
Units are mm (inches) unless specified.

Figure 33. QFP Principal Dimensions

ERRATA

An 80C186EB with a STEPID value of 0001H has the following known errata. A device with a STEPID of 0001H can be visually identified by noting the **absence** of an alpha character next to the FPO number or by the **presence** of an **"A"** alpha character next to the FPO number. The FPO number location is shown in Figures 5 and 6.

1. A19/$\overline{\text{ONCE}}$ is not latched by the rising edge of $\overline{\text{RESIN}}$. A19/$\overline{\text{ONCE}}$ must remain active (LOW) at all times to remain in the ONCE™ Mode. Removing A19/$\overline{\text{ONCE}}$ after $\overline{\text{RESIN}}$ is high will return all output pins to a driving state, however, the 80C186EB will remain in a reset state.
2. During interrupt acknowledge (INTA) bus cycles, the bus controller will ignore the state of the READY pin if the previous bus cycle ignored the state of the READY pin. This errata can only occur if the Chip-Select Unit is being used. All active chip-selects must be programmed to use READY (RDY bit must be programmed to a 1) if wait-states are required for INTA bus cycles.
3. CLKOUT will transition off the **rising** edge of CLKIN rather than the falling edge of CLKIN. This does not affect any bus timings other than T_{CD}.
4. $\overline{\text{RESIN}}$ has a hysterisis of only 130 mV. It is recommended that $\overline{\text{RESIN}}$ be driven by a Schmitt triggered device to avoid processor lockup during reset using an RC circuit.
5. SINT1 will only go active for one clock period when a receive or transmit interrupt is pending (i.e., it does not remain active until the S1STS register is read). If SINT1 is to be connected to any of the 80C186EB interrupt lines (INT0–INT4), then it must be latched by user logic.

An 80C186EB with a STEPID value of 0001H or 0002H has the following known errata. Otherwise, an 80C186EB with a STEPID value of 0002H has no known errata (as of this publication). A device with a STEPID of 0002H can be visually identified by noting the presence of a "B" or "C" alpha character next to the FPO number. The FPO number location is shown in Figures 5 and 6.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the $\overline{\text{INTA1}}$ line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistantly, it is dependent on interrupt timing.

REVISION HISTORY

The following changes have been made between the -001 version and the -002 version of the 80C186EB data sheet. The -002 data sheet applies to all devices with no alpha character or an "A" alpha character after the FPO number (or by reading a STEPID of 0001H). The FPO number location is shown in Figures 5 and 6.

1. Figure 1 was updated to correct for incorrect pin names (TXD1 and $\overline{\text{TEST}}$/BUSY), and to rename the Powerdown Control Unit to the Power Management Unit.
2. Figure 3 was corrected to indicate that the STEP ID register is located at 0BCH (not 0BAH), and to rename the INTx control registers.
3. Page 6, Power Control Unit was changed to Power Management Unit.
4. Figure 4 was corrected to indicate that the AD15:0 are P(X) rather than P(Z).
5. Table 1 was updated. The following list of pins either had changes to their TYPE field or their DESCRIPTION field.
   OSCOUT, PDTMR, AD15:0, A19:16, $\overline{\text{S2:0}}$, $\overline{\text{DEN}}$, $\overline{\text{LOCK}}$, HLDA, P1.0–P1.7, TxOUT, INT4, SINT1.
6. Figures 4 and 5 were updated to change pin name P2.3/SINT to P2.3/SINT1.
7. PDTMR pin capacitance chart was added to page 21.
8. TCD specification was changed to 20, 23, 27 ns for the -16, -13, and -8 devices respectively.
9. Serial port timings on page 27 were updated.
10. Figures 14 and 15 were updated to correctly identify the names of signals affected by $\overline{\text{RESIN}}$.
11. Correction of the text describing Figures 26 and 27.
12. Changes I4CON register location described in Figure 24.
13. The description of P1CON and P2CON in Figure 26 was changed to indicate that a 0 selects the Port function, while a 1 selects the Peripheral function.
14. Changed Figure 30 description to Power Management Unit.
15. Added $\overline{\text{RESIN}}$ hysterisis anamoly to errata descriptions.

The following changes have been made between the -002 version and the -003 version of the 80C186EB data sheet. This -003 data sheet applies to any 80C186EB with a "B" alpha character after the FPO number. The FPO number location is shown in Figures 5 and 6.

1. The data sheet was changed from a Product Preview version to an Advanced Information version.
2. Figures 1, 5, 6, 8, 11, 12, 17, 22, 23, 24, 26, 29 and 31 and Tables 3 and 4 were updated to correct for errors.
3. The DC specifications table has changed. Also, notes 3, 4 and 5 have been changed/added.
4. Graphs for I_{CC} versus Frequency have been changed to equations with supporting text.
5. Graphs for PDTMR pin capacitance have been changed to equations with supporting text.
6. AC Hold timings have been changed from 0 ns to 3 ns.
7. READY input setup time has been changed from 13 ns to 10 ns.
8. Serial port MODE 0 timings have been changed.
9. Various typing errors have been corrected throughout the document.

The following changes were made between the -003 and -004 versions of the 80C186EB data sheets. The -004 data sheets applies to any 80C186EB with a "B" alpha character after the FPO number. The FPO number location is shown in Figures 5 and 6.

1. 20 MHz Electrical, DC and AC Specifications were added to the appropriate sections.
2. The following 80C186EB Core Architecture sections were deleted:
   Register Set
   Instruction Set
   Memory Organization
   Addressing Modes
   Data Types
   Interrupts
3. Most of the 80C186EB Peripheral Architecture sections were condensed along with the Register Bit Summary section.
4. Most of the Tables and Figures have been renumbered due to edits.

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80C186EC-16, -13
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSOR

- **Full Static Operation**
- **True CMOS Inputs and Outputs**
- **−40°C to +85°C Operating Temperature Range**

- **Integrated Feature Set:**
  - **Low-Power, Static, Enhanced 8086 CPU Core**
  - **Two Independent DMA Supported UARTs, each with an Integral Baud Rate Generator**
  - **Four Independent DMA Channels**
  - **24 Multiplexed I/O Port Pins**
  - **Two 8259A Compatible Programmable Interrupt Controllers**
  - **Three Programmable 16-Bit Timer/ Counters**
  - **32-Bit Watchdog Timer**
  - **Ten Programmable Chip Selects with Integral Wait-State Generator**
  - **Memory Refresh Control Unit**
  - **Power Management Unit**
  - **On-Chip Oscillator**
  - **System Level Testing Support (ONCE™ Mode)**
- **Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O**
- **Low-Power Operating Modes:**
  - **Idle Mode Freezes CPU Clocks but Keeps Peripherals Active**
  - **Powerdown Mode Freezes All Internal Clocks**
  - **Powersave Mode Divides All Clocks by Programmable Prescalar**
- **Complete System Development Support**
  - **ASM86 Assembler, PL/M 86, Pascal86, Fortran 86, iC-86 and System Utilities**
  - **In-Circuit Emulator (ICE™-186EC)**
- **Supports 80C187 Numerics Processor Extension**
- **Package Types:**
  - **100-Pin EIAJ Quad Flat Pack (QFP) (S80C186EC)**
  - **100-Pin Plastic Quad Flat Pack (PQFP) (KU80C186EC)**
- **Speed Versions Available:**
  - **16 MHz (80C186EC-16)**
  - **13 MHz (80C186EC-13)**

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The 80C186EC is a member of the 186 Integrated Processor Family. The 186 Integrated Processor Family incorporates several different VLSI devices all of which share a common CPU architecture: the 8086/8088. The 80C186EC uses the latest high density CHMOS technology to integrate several of the most common system peripherals with an enhanced 8086 CPU core to create a powerful system on a single monolithic silicon die.

April 1992
Order Number: 272027-002

80C186EC-16, -13
16-Bit High-Integration Embedded Processor

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CONTENTS

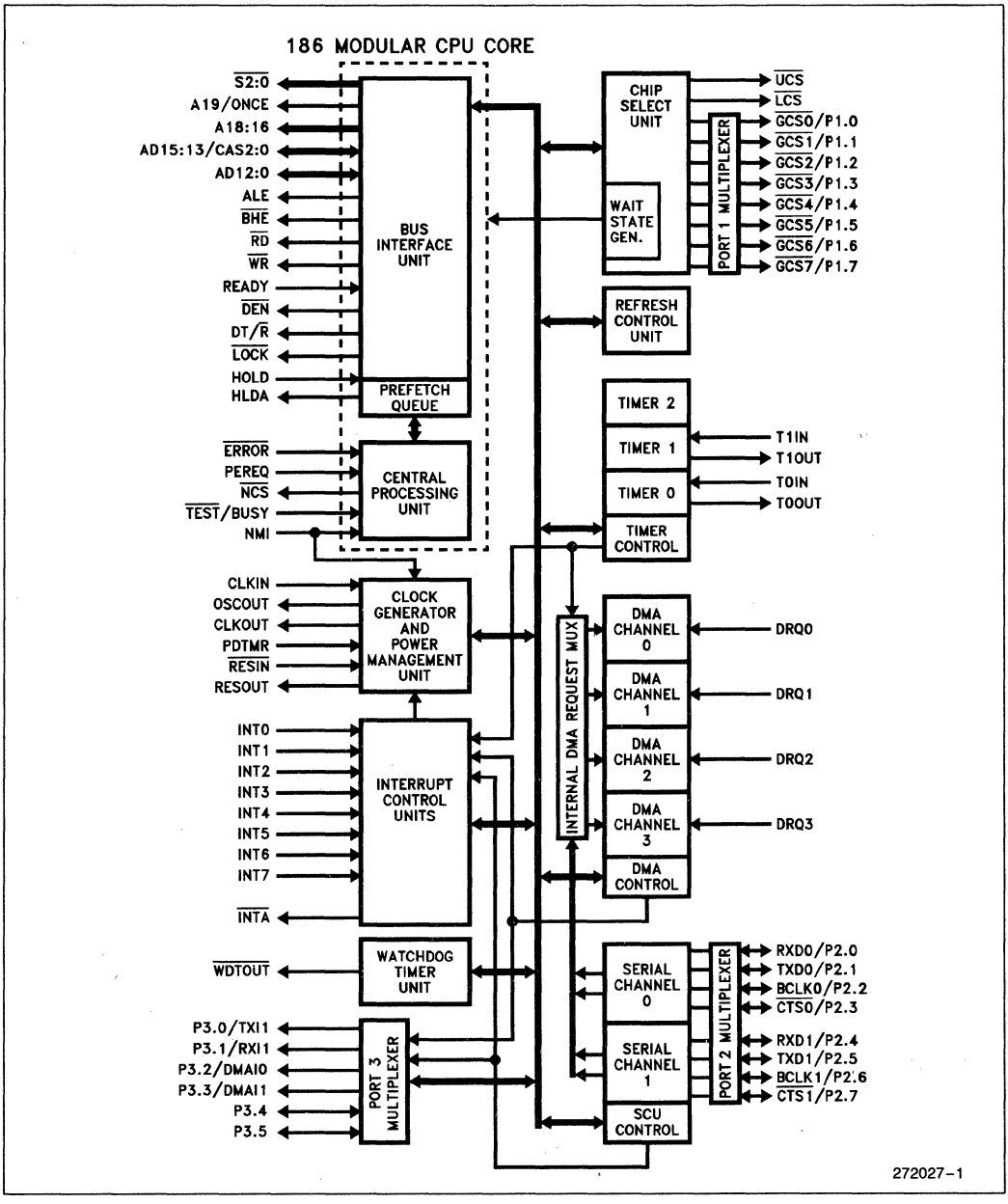

Figure 1. 80C186EC Block Diagram

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INTRODUCTION

The 186 Integrated Processor Family incorporates a wide range of VLSI devices tailored to suit the needs of embedded system designers. All 186 Family devices share a common CPU architecture: the industry standard 8086/8088. Code developed on other "X86" platforms can be ported with little or no modification to any of the 186 Integrated Processor Family devices.

Each of the 186 Integrated Processor Family devices adds a full complement of peripherals to the 8086/8088 CPU core. The type of peripherals and level of integration vary between family members. A complete 186 Family system can often be designed with just the addition of RAM, ROM and simple glue logic. The space savings afforded by high-integration are critical as designers continue to strive for smaller size and portability.

The 80C186EC is one of the highest integration members of the 186 Integrated Processor Family. Two serial ports are provided for services such as interprocessor communication, diagnostics and modem interfacing. Four DMA channels allow for high speed data movement as well as support of the on-board serial ports. A flexible chip select unit simplifies memory and peripheral interfacing. The three general purpose timer/counters can be used for a variety of time measurement and waveform generation tasks. A watchdog timer is provided to insure system integrity even in the most hostile of environments. Two 8259A compatible interrupt controllers handle internal interrupts, and, up to 57 external interrupt requests. A DRAM refresh unit and 24 multiplexed I/O ports round out the feature set of the 80C186EC.

OVERVIEW

Figure 1 shows a block diagram of the 80C186EC. The execution unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhanced execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instructions and full static operation. The bus interface unit (BIU) is the same as that found on the original 186 family products, except the queue-status mode has been deleted and buffer interface control has been changed to ease system design timings. An independent internal bus is used for communication between the BIU and on-chip peripherals.

80C186EC CORE ARCHITECTURE

Bus Interface Unit

The 80C186EC core incorporates a bus controller that generates local bus control signals. In addition, it employs a HOLD/HLDA protocol to share the local bus with other bus masters.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information and data (for write operations) information. It is also responsible for reading data from the local bus during a read operation. A ready input pin is provided to extend a bus cycle beyond the minimum four states (clocks).

The 80C186EC bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus.

Clock Generator

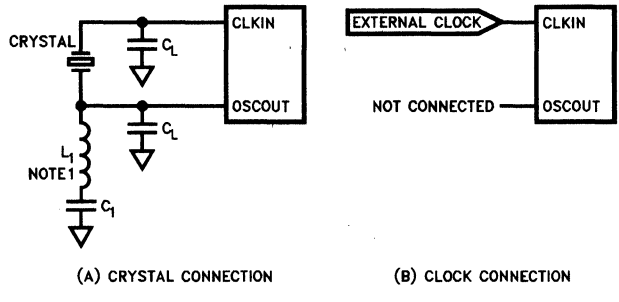
The 80C186EC provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter and three low-power operating modes.

The oscillator circuit is designed to be used with either a parallel resonant fundamental or third-overtone mode crystal network. Alternatively, the oscillator circuit may be driven from an external clock source. Figure 2 shows the various operating modes of the 80C186EC oscillator circuit.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide-by-two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.

The following parameters are recommended when choosing a crystal:

Temperature Range:	Application Specific
ESR (Equivalent Series Res.):	40Ω max
C0 (Shunt Capacitance of Crystal):	7.0 pF max
C_L (Load Capacitance):	20 pF ±2 pF
Drive Level:	1 mW (max)



NOTE:
1. The LC network is only required when using a third overtone crystal.

Figure 2. 80C186EC Clock Connections

80C186EC Peripheral Architecture

The 80C186EC integrates several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexbile and provide logical interconnections between supporting units (e.g., the DMA unit can accept requests from the Serial Communications Unit).

The list of integrated peripherals includes:

— Two cascaded, 8259A compatible, Programmable Interrupt Controllers
— 3-Channel Timer/Counter Unit
— 2-Channel Serial Communications Unit
— 4-Channel DMA Unit
— 10-Output Chip-Select Unit
— 32-bit Watchdog Timer Unit
— I/O Port Unit
— Refresh Control Unit
— Power Management Unit

The registers associated with each integrated peripheral are contained within a 128 x 16-bit register file called the Peripheral Control Block (PCB). The base address of the PCB is programmable and can be located on any 256 byte address boundary in either memory or I/O space.

Figure 3 provides a list of the registers associated with the PCB. The Register Bit Summary individually lists all of the registers and identifies each of their programming attributes.

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PCB Offset	Function
00H	Master PIC Port 0
02H	Master PIC Port 1
04H	Slave PIC Port 0
06H	Slave PIC Port 1
08H	Reserved
0AH	SCU Int. Req. Ltch.
0CH	DMA Int. Req. Ltch.
0EH	TCU Int. Req. Ltch.
10H	Reserved
12H	Reserved
14H	Reserved
16H	Reserved
18H	Reserved
1AH	Reserved
1CH	Reserved
1EH	Reserved
20H	WDT Reload High
22H	WDT Reload Low
24H	WDT Count High
26H	WDT Count Low
28H	WDT Clear
2AH	WDT Disable
2CH	Reserved
2EH	Reserved
30H	T0 Count
32H	T0 Compare A
34H	T0 Compare B
46H	T0 Control
38H	T1 Count
3AH	T1 Compare A
3CH	T1 Compare B
3EH	T1 Control

PCB Offset	Function
40H	T2 Count
42H	T2 Compare
44H	Reserved
46H	T2 Control
48H	Port 3 Direction
4AH	Port 3 Pin State
4CH	Port 3 Mux Control
4EH	Port 3 Data Latch
50H	Port 1 Direction
52H	Port 1 Pin State
54H	Port 1 Mux Control
56H	Port 1 Data Latch
58H	Port 2 Direction
5AH	Port 2 Pin State
5CH	Port 2 Mux Control
5EH	Port 2 Data Latch
60H	SCU 0 Baud
62H	SCU 0 Count
64H	SCU 0 Control
66H	SCU 0 Status
68H	SCU 0 RBUF
6AH	SCU 0 TBUF
6CH	Reserved
6EH	Reserved
70H	SCU 1 Baud
72H	SCU 1 Count
74H	SCU 1 Control
76H	SCU 1 Status
78H	SCU 1 RBUF
7AH	SCU 1 TBUF
7CH	Reserved
7EH	Reserved

PCB Offset	Function
80H	GCS0 Start
82H	GCS0 Stop
84H	GCS1 Start
86H	GCS1 Stop
88H	GCS2 Start
8AH	GCS2 Stop
8CH	GCS3 Start
8EH	GCS3 Stop
90H	GCS4 Start
92H	GCS4 Stop
94H	GCS5 Start
96H	GCS5 Stop
98H	GCS6 Start
9AH	GCS6 Stop
9CH	GCS7 Start
9EH	GCS7 Stop
A0H	LCS Start
A2H	LCS Stop
A4H	UCS Start
A6H	UCS Stop
A8H	Relocation Register
AAH	Reserved
ACH	Reserved
AEH	Reserved
B0H	Refresh Base Addr.
B2H	Refresh Time
B4H	Refresh Control
B6H	Refresh Address
B8H	Power Control
BAH	Reserved
BCH	Step ID
BEH	Powersave

PCB Offset	Function
C0H	DMA 0 Source Low
C2H	DMA 0 Source High
C4H	DMA 0 Dest. Low
C6H	DMA 0 Dest. High
C8H	DMA 0 Count
CAH	DMA 0 Control
CCH	DMA Module Pri.
CEH	DMA Halt
D0H	DMA 1 Source Low
D2H	DMA 1 Source High
D4H	DMA 1 Dest. Low
D6H	DMA 1 Dest. High
D8H	DMA 1 Count
DAH	DMA 1 Control
DCH	Reserved
DEH	Reserved
E0H	DMA 2 Source Low
E2H	DMA 2 Source High
E4H	DMA 2 Dest. Low
E6H	DMA 2 Dest. High
E8H	DMA 2 Count
EAH	DMA 2 Control
ECH	Reserved
EEH	Reserved
F0H	DMA 3 Source Low
F2H	DMA 3 Source High
F4H	DMA 3 Dest. Low
F6H	DMA 3 Dest. High
F8H	DMA 3 Count
FAH	DMA 3 Control
FCH	Reserved
FEH	Reserved

Figure 3. 80C186EC Peripheral Control Block Registers

Programmable Interrupt Controllers

The 80C186EC utilizes two 8259A compatible Programmable Interrupt Controllers (PIC) to manage both internal and external interrupts. The 8259A modules are configured in a master/slave arrangement.

Seven of the external interrupt pins, INT0 through INT6, are connected to the master 8259A module. The eighth external interrupt pin, INT7, is connected to the slave 8259A module.

There are a total of 11 internal interrupt sources from the integrated peripherals: 4 Serial, 4 DMA and 3 Timer/Counter.

Timer/Counter Unit

The 80C186EC Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for external control or clocking. The third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms or generate timed interrupts.

Serial Communications Unit

The Serial Communications Unit (SCU) of the 80C186EC contains two independent channels. Each channel is identical in operation except that only channel 0 is directly supported by the integrated interrupt controller (the channel 1 interrupts are routed to external interrupt pins). Each channel has its own baud rate generator and can be internally or externally clocked up to one half the 80C186EC operating frequency. Both serial channels can request service from the DMA unit thus providing block reception and transmission without CPU intervention.

Independent baud rate generators are provided for each of the serial channels. For the asynchronous modes, the generator supplies an 8x baud clock to both the receive and transmit shifting register logic. A 1x baud clock is provided in the synchronous mode.

DMA Unit

The four channel Direct Memory Access (DMA) Unit is comprised of two modules with two channels each. All four channels are identical in operation. DMA transfers can take place from memory to memory, I/O to memory, memory to I/O or I/O to I/O. DMA requests can be external (on the DRQ pins), internal (from Timer 2 or a serial channel) or software initiated.

The DMA Unit transfers data as bytes only. Each data transfer requires at least two bus cycles, one to fetch data and one to deposit. The minimum clock count for each transfer is 8, but this will vary depending on synchronization and wait states.

Chip-Select Unit

The 80C186EC Chip-Select Unit (CSU) integrates logic which provides up to ten programmable chip-selects to access both memories and peripherals. In addition, each chip-select can be programmed to automatically insert additional clocks (wait states) into the current bus cycle, and/or automatically terminate a bus cycle independent of the condition of the READY input pin.

I/O Port Unit

The I/O Port Unit on the 80C186EC supports two 8-bit channels and one 6-bit channel of input, output or input/output operation. Port 1 is multiplexed with the chip select pins and is output only. Port 2 is multiplexed with the pins for serial channels 1 and 2. All Port 2 pins are input/output. Port 3 has a total of 6 pins: four that are multiplexed with DMA and serial port interrupts and two that are non-multiplexed, open drain I/O.

Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 12-bit address generator is maintained by the RCU and is presented on the A12:1 address lines during the refresh bus cycle. Address bits A19:13 are programmable to allow the refresh address block to be located on any 8 Kbyte boundary.

Watchdog Timer Unit

The Watchdog Timer Unit (WDT) allows for graceful recovery from unexpected hardware and software upsets. The WDT consists of a 32-bit counter that decrements every clock cycle. If the counter reaches zero before being reset, the $\overline{\text{WDTOUT}}$ pin is

pulled low for four clock cycles. Logically ANDing the $\overline{\text{WDTOUT}}$ pin with the power-on reset signal allows the WDT to reset the device in the event of a WDT timeout. If a less drastic method of recovery is desired, $\overline{\text{WDTOUT}}$ can be connected directly to NMI or one of the INT input pins. The WDT may also be used as a general purpose timer.

Power Management Unit

The 80C186EC Power Management Unit (PMU) is provided to control the power consumption of the device. The PMU provides four power management modes: Active, Powersave, Idle and Powerdown.

Active Mode indicates that all units on the 80C186EC are operating at ½ the CLKIN frequency.

Idle Mode freezes the clocks of the Execution and Bus units at a logic zero state (all peripherals continue to operate normally).

The Powerdown Mode freezes all internal clocks at a logic zero level and disables the crystal oscillator.

In Powersave Mode, all internal clock signals are divided by a programmable prescalar (up to 1/64 the normal frequency). Powersave Mode can be used with Idle Mode as well as during normal (Active Mode) operation.

80C187 Interface

The 80C186EC supports the direct connection of the 80C187 Numerics Processor Extension. The 80C187 can dramatically improve the performance of calculation intensive applications.

ONCE™ Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C186EC has a test mode available which forces all output and input/output pins to be placed in the high-impedance state. ONCE stands for "ON Circuit Emulation". The ONCE mode is selected by forcing the A19/S6/$\overline{\text{ONCE}}$ pin low during a processor reset (this pin is weakly held high during reset to prevent inadvertant entrance into ONCE Mode).

PACKAGE INFORMATION

This section describes the pin functions, pinout and thermal characteristics for the 80C186EC in both the Plastic Quad Flat Pack (JEDEC PQFP) and the EIAJ Quad Flat Pack (QFP). For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

Pin Descriptions

Each pin or logical set of pins is described in Table 2. There are four columns for each entry in the Pin Description Table. The following sections describe each column.

Column 1: Pin Name

In this column is a mnemonic that describes the pin function. Negation of the signal name (i.e. $\overline{\text{RESIN}}$) implies that the signal is active low.

Column 2: Pin Type

A pin may be either power (P), ground (G), input only (I), output only (O) or input/output (I/O). Please note that some pins have more than 1 function. A19/S6/$\overline{\text{ONCE}}$, for example, is normally an output but functions as an input during reset. For this reason A19/S6/$\overline{\text{ONCE}}$ is classified as an input/output pin.

Column 3: Input Type (for I and I/O types only)

There are two different types of input pins on the 80C186EC: asynchronous and synchronous. **Asynchronous** pins require that setup and hold times be met only to *guarantee recognition*. **Synchronous** input pins require that the setup and hold times be met to *guarantee proper operation*. Stated simply, missing a setup or hold on an asynchronous pin will result in something minor (i.e. a timer count will be missed) whereas missing a setup or hold on a synchronous pin will result in system failure (the system will "lock up").

An input pin may also be edge or level sensitive.

Column 4: Output States (for O and I/O types only)

The state of an output or I/O pin is dependent on the operating mode of the device. There are four modes of operation that are different from normal active mode: Bus Hold, Reset, Idle Mode, Powerdown Mode. This column describes the output pin state in each of these modes.

The legend for interpreting the information in the Pin Descriptions is shown in Table 1.

As an example, please refer to the table entry for AD12:0. The "I/O" signifies that the pins are bidirectional (i.e. have both an input and output function). The "S" indicates that, as an input the signal must be synchronized to CLKOUT for proper operation. The "H(Z)" indicates that these pins will float while the processor is in the Hold Acknowledge state. R(Z) indicates that these pins will float while $\overline{\text{RESIN}}$ is low. P(0) and I(0) indicate that these pins will drive 0 when the device is in either Powerdown or Idle Mode.

Some pins, the I/O Ports for example, can be programmed to perform more than one function. Multifunction pins have a "/" in their signal name between the different functions (i.e. P3.0/RXI1). If the input pin type or output pin state differ between functions, then that will be indicated by separating the state (or type) with a "/" (i.e. H(X)/H(Q)). In this example when the pin is configured as P3.0 then its hold output state is H(X); when configured as RXI1 its output state is H(Q).

All pins float while the processor is in the ONCE Mode (with the exception of OSCOUT).

Table 1. Pin Description Nomenclature

Symbol	Description
P	Power Pin (apply + V_{CC} voltage)
G	Ground (connect to V_{SS})
I	Input only pin
O	Output only pin
I/O	Input/Output pin
S(E)	Synchronous, edge sensitive
S(L)	Synchronous, level sensitive
A(E)	Asynchronous, edge sensitive
A(L)	Asynchronous, level sensitive
H(1)	Output driven to V_{CC} during bus hold
H(0)	Output driven to V_{SS} during bus hold
H(Z)	Output floats during bus hold
H(Q)	Output remains active during bus hold
H(X)	Output retains current state during bus hold
R(WH)	Output weakly held at V_{CC} during reset
R(1)	Output driven to V_{CC} during reset
R(0)	Output driven to V_{SS} during reset
R(Z)	Output floats during reset
R(Q)	Output remains active during reset
R(X)	Output retains current state during reset
I(1)	Output driven to V_{CC} during Idle Mode
I(0)	Output driven to V_{SS} during Idle Mode
I(Z)	Output floats during Idle Mode
I(Q)	Output remains active during Idle Mode
I(X)	Output retains current state during Idle Mode
P(1)	Output driven to V_{CC} during Powerdown Mode
P(0)	Output driven to V_{SS} during Powerdown Mode
P(Z)	Output floats during Powerdown Mode
P(Q)	Output remains active during Powerdown Mode
P(X)	Output retains current state during Powerdown Mode

Table 2. 80C186EC Pin Descriptions

Pin Name	Pin Type	Input Type	Output States	Pin Description
V_{CC}	P	—	—	**POWER** +5V ±10% power supply connection
V_{SS}	G	—	—	**GROUND**
CLKIN	I	A(E)	—	**CLocK INput** is the external clock input. An external oscillator operating at two times the required 80C186EC operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O	—	H(Q) R(Q) I(Q) P(X)	**OSCillator OUTput** is only used when using a crystal to generate the internal clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin can not be used as 2X clock output for non-crytsal applications (i.e. this pin is not connected for non-crystal applications).
CLKOUT	O	—	H(Q) R(Q) I(Q) P(X)	**CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transitions every falling edge of CLKIN.
$\overline{\text{RESIN}}$	I	A(L)	—	**RESet IN** causes the 80C186EC to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the 80C186EC begins fetching opcodes at memory location 0FFFF0H.
RESOUT	O	—	H(0) R(1) I(0) P(0)	**RESet OUTput** that indicates the 80C186EC is currently in the reset state. RESOUT will remain active as long as $\overline{\text{RESIN}}$ remains active.
PDTMR	I/O	A(L)	H(WH) R(Z) P(WH) I(WH)	**Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the 80C186EC waits after an exit from Powerdown before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I	A(E)	—	**Non-Maskable Interrupt** input causes a TYPE-2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{\text{TEST}}$/BUSY	I	A(E)	—	**TEST** is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (LOW). $\overline{\text{TEST}}$ is alternately known as **BUSY** when interfacing with an 80C187 numerics coprocessor.
A19/S6/$\overline{\text{ONCE}}$	I/O	A(L)	H(Z) R(WH) I(0) P(0)	This pin drives address bit 19 during the address phase of the bus cycle. During T2 and T3 this pin functions as status bit 6. S6 is low to indicate CPU bus cycles and high to indicate DMA or refresh bus cycles. During a processor reset ($\overline{\text{RESIN}}$ active) this pin becomes the ONCE input pin. Holding this pin low during reset will force the part into ONCE Mode.

Table 2. 80C186EC Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
A18/S5 A17/S4 A16/S3	I/O	A(L)	H(Z) R(WH) I(0) P(0)	These pins drive address information during the address phase of the bus cycle. During T2 and T3 these pins drive status information (which is always 0 on the 80C186EC). These pins are used as inputs during factory test; driving these pins low during reset will cause unspecified operation.
AD15/CAS2 AD14/CAS1 AD13/CAS0	I/O	S(L)	H(Z) R(Z) I(0) P(0)	These pins are part of the multiplexed ADDRESS and DATA bus. During the address phase of the bus cycle, address bits 15 through 13 are presented on these pins and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle. Pins AD15:13/ CAS2:0 drive the 82C59 slave address information during interrupt acknowledge cycles.
AD12:0	I/O	S(L)	H(Z) R(Z) I(0) P(0)	These pins provide a multiplexed ADDRESS and DATA bus. During the address phase of the bus cycle, address bits 0 through 12 are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle.
$\overline{S2:0}$	O	—	H(Z) R(1) I(1) P(1)	Bus cycle Status are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ **Bus Cycle Initiated** 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Instruction Queue Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive (No bus activity)
ALE	O	—	H(0) R(0) I(0) P(0)	**Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle.
$\overline{BHE}$	O	—	H(Z) R(Z) I(1) P(1)	**Byte High Enable** output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. $\overline{BHE}$ and A0 have the following logical encoding: **A0** $\overline{BHE}$ **Encoding** 0 0 Word transfer 0 1 Even Byte transfer 1 0 Odd Byte transfer 1 1 Refresh operation
$\overline{RD}$	O	—	H(Z) R(Z) I(1) P(1)	**ReaD** output signals that the accessed memory or I/O device should drive data information onto the data bus.

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Table 2. 80C186EC Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
$\overline{WR}$	O	—	H(Z) R(Z) I(1) P(1)	**WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device.
READY	I	A(L) S(L) (Note 1)	—	**READY** input to signal the completion of a bus cycle. READY must be active to terminate any 80C186EC bus cycle, unless it is ignored by correctly programming the Chip-Select unit.
$\overline{DEN}$	O	—	H(Z) R(Z) I(1) P(1)	**Data ENable** output to control the enable of bi-directional transceivers when buffering a 80C186EC system. $\overline{DEN}$ is active only when data is to be transferred on the bus.
DT/$\overline{R}$	O	—	H(Z) R(Z) I(X) P(X)	**Data Transmit/Receive** output controls the direction of a bi-directional buffer when buffering an 80C186EC system.
$\overline{LOCK}$	I/O	A(L)	H(Z) R(Z) I(X) P(X)	**LOCK** output indicates that the bus cycle in progress is not interruptable. The 80C186EC will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low.
HOLD	I	A(L)	—	**HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The 80C186EC will relinquish control of the local bus between instruction boundaries that are not LOCKed.
HLDA	O	—	H(1) R(0) I(0) P(0)	**HoLD Acknowledge** output to indicate that the 80C186EC has relinquished control of the local bus. When HLDA is asserted, the 80C186EC will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly.
$\overline{NCS}$	O	—	H(1) R(1) I(1) P(1)	**Numerics Coprocessor Select** output is generated when acessing a numerics coprocessor.
$\overline{ERROR}$	I	A(L)	—	**ERROR** input that indicates the last numerics processor extension operation resulted in an exception condition. An interrupt TYPE 16 is generated if $\overline{ERROR}$ is sampled active at the beginning of a numerics operation. Systems not using an 80C187 must tie $\overline{ERROR}$ to V_{CC}.
PEREQ	I	A(L)	—	**Processor Extension REQuest** signals that a data transfer between an 80C187 Numerics Processor Extension and Memory is pending. Systems not using an 80C187 must tie this pin to V_{SS}.

Table 2. 80C186EC Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
$\overline{UCS}$	O	—	H(1) R(1) I(1) P(1)	**Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address range programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH.
$\overline{LCS}$	O	—	H(1) R(1) I(1) P(1)	**Lower Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address range programmed by the user. $\overline{LCS}$ is inactive after a reset.
P1.0/$\overline{GCS0}$ P1.1/$\overline{GCS1}$ P1.2/$\overline{GCS2}$ P1.3/$\overline{GCS3}$ P1.4/$\overline{GCS4}$ P1.5/$\overline{GCS5}$ P1.6/$\overline{GCS6}$ P1.7/$\overline{GCS7}$	O	—	H(X)/H(1) R(1) I(X)/I(1) P(X)/P(1)	These pins provide a multiplexed function. If enabled, each pin can provide a **General purpose Chip Select** output which will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. When not programmed as a Chip-Select, each pin may be used as a general purpose output port.
T0OUT T1OUT	O	—	H(Q) R(1) I(Q) P(X)	**Timer OUTput** pins can be programmed to provide single clock or continuous waveform generation, depending on the timer mode selected.
T0IN T1IN	I	A(L) A(E)	—	**Timer INput** is used either as clock or control signals, depending on the timer mode selected. This pin may be either level or edge sensitive depending on the programming mode.
INT7:0	I	A(L) A(E)	—	**Maskable INTerrupt** input will cause a vector to a specific Type interrupt routine. The INT6:0 pins can be used as cascade inputs from slave 8259A devices. The INT pins can be configured as level or edge sensitive.
$\overline{INTA}$	O	—	H(1) R(1) I(1) P(1)	**INTerrupt Acknowledge** output is a handshaking signal used by external 82C59A-2 Programmable Interrupt Controllers.
P3.5 P3.4	I/O	A(L)	H(X) R(Z) I(X) H(X)	Bidirectional, open-drain port pins.
P3.3/DMAI1 P3.2/DMAI0	O	—	H(X) R(0) I(Q) P(X)	**DMA Interrupt** output goes active to indicate that the channel has completed a transfer. DMAI1 and DMAI0 are multiplexed with output only port functions.
P3.1/TXI1	O	—	H(X)/H(Q) R(0) I(Q) P(X)	**Transmit Interrupt** output goes active to indicate that serial channel 1 has completed a transfer. TXI1 is multiplexed with an output only Port function.

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Table 2. 80C186EC Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
P3.0/RXI1	O	—	H(X)/H(Q) R(0) I(Q) P(X)	**Receive Interrupt** output goes active to indicate that serial channel 1 has completed a reception. RXI1 is multiplexed with an output only port function.
$\overline{\text{WDTOUT}}$	O	—	H(Q) R(1) I(Q) P(X)	**WatchDog Timer OUTput** is driven low for four clock cycles when the watchdog timer reaches zero. $\overline{\text{WDTOUT}}$ may be ANDed with the power-on reset signal to reset the 80C186EC when the watchdog timer is not properly reset.
P2.7/$\overline{\text{CTS1}}$ P2.3/$\overline{\text{CTS0}}$	I/O	A(L)	H(X) R(Z) I(X) P(X)	**Clear-To-Send** input is used to prevent the transmission of serial data on the TXD signal pin. $\overline{\text{CTS1}}$ and $\overline{\text{CTS0}}$ are multiplexed with an I/O Port function.
P2.6/BCLK1 P2.2/BCLK0	I/O	A(L)/ A(E)	H(X) R(Z) I(X) P(X)	**Baud CLocK** input can be used as an alternate clock source for each of the integrated serial channels. The BCLK inputs are multiplexed with I/O Port functions. The BCLK input frequency cannot exceed ½ the operating frequency of the 80C186EC.
P2.5/TXD1 P2.1/TXD0	I/O	A(L)	H(Q) R(Z) I(X)/I(Q) P(X)	**Transmit Data** output provides serial data information. The TXD outputs are multiplexed with I/O Port functions. During synchronous serial communications, TXD will function as a clock output.
P2.4/RXD1 P2.0/RXD0	I/O	A(L)	H(X)/H(Q) R(Z) I(X)/I(Q) P(X)	**Receive Data** input accepts serial data information. The RXD pins are multiplexed with I/O Port functions. During synchronous serial communications, RXD is bi-directional and will become an output for transmission of data (TXD becomes the clock).
DRQ3:0	I	A(L)	—	**DMA ReQuest** input pins are used to request a DMA transfer. The timing of the request is dependent on the programmed synchronization mode.

NOTE:
1. READY is A(E) for the rising edge of CLKOUT, S(E) for the falling edge of CLKOUT.

80C186EC Pinout

Tables 3 and 4 list the 80C186EC pin names with package location for the 100-pin Plastic Quad Flat Pack (PQFP) component. Figure 4 depicts the complete 80C186EC pinout (PQFP) package as viewed from the top side of the component (i.e. contacts facing down).

Tables 5 and 6 list the 80C186EC pin names with package location for the 100-pin EIAJ Quad Flat Pack (QFP) component. Figure 5 depicts the complete 80C186EC (QFP package) as viewed from the top side of the component (i.e. contacts facing down).

Table 3. 80C186EC PQFP Pin Functions with Location

AD Bus	
Name	**Pin**
AD0	73
AD1	72
AD2	71
AD3	70
AD4	66
AD5	65
AD6	64
AD7	63
AD8	60
AD9	59
AD10	58
AD11	57
AD12	56
AD13/CAS0	55
AD14/CAS1	54
AD15/CAS2	53
A16/S3	77
A17/S4	76
A18/S5	75
A19/S6/$\overline{\text{ONCE}}$	74

Bus Control	
Name	**Pin**
ALE	52
$\overline{\text{BHE}}$	51
$\overline{\text{S0}}$	78
$\overline{\text{S1}}$	79
$\overline{\text{S2}}$	80
$\overline{\text{RD}}$	50
$\overline{\text{WR}}$	49
READY	85
$\overline{\text{DEN}}$	47
DT/$\overline{\text{R}}$	46
$\overline{\text{LOCK}}$	48
HOLD	44
HLDA	45
$\overline{\text{INTA}}$	34

Power and Ground	
Name	**Pin**
V_{CC}	13
V_{CC}	14
V_{CC}	38
V_{CC}	62
V_{CC}	67
V_{CC}	69
V_{CC}	86
V_{SS}	12
V_{SS}	15
V_{SS}	37
V_{SS}	39
V_{SS}	61
V_{SS}	68
V_{SS}	87

Processor Control	
Name	**Pin**
$\overline{\text{RESIN}}$	8
RESOUT	7
CLKIN	10
OSCOUT	11
CLKOUT	6
$\overline{\text{TEST}}$/BUSY	83
PEREQ	81
$\overline{\text{NCS}}$	35
$\overline{\text{ERROR}}$	84
PDTMR	9
NMI	82
INT0	30
INT1	31
INT2	32
INT3	33
INT4	40
INT5	41
INT6	42
INT7	43

I/O	
Name	**Pin**
$\overline{\text{UCS}}$	88
$\overline{\text{LCS}}$	89
P1.7/$\overline{\text{GCS7}}$	90
P1.6/$\overline{\text{GCS6}}$	91
P1.5/$\overline{\text{GCS5}}$	92
P1.4/$\overline{\text{GCS4}}$	93
P1.3/$\overline{\text{GCS3}}$	94
P1.2/$\overline{\text{GCS2}}$	95
P1.1/$\overline{\text{GCS1}}$	96
P1.0/$\overline{\text{GCS0}}$	97
P2.7/$\overline{\text{CTS1}}$	23
P2.6/BCLK1	22
P2.5/TXD1	21
P2.4/RXD1	20
P2.3/$\overline{\text{CTS0}}$	19
P2.2/BCLK0	18
P2.1/TXD0	17
P2.0/RXD0	16
P3.5	29
P3.4	28
P3.3/DMAI1	27
P3.2/DMAI0	26
P3.1/TXI1	25
P3.0/RXI1	24
T0IN	3
T0OUT	2
T1IN	5
T1OUT	4
DRQ0	98
DRQ1	99
DRQ2	100
DRQ3	1
$\overline{\text{WDTOUT}}$	36

Table 4. PQFP Pin Locations with Pin Name

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DRQ3	26	DMAI0/P3.2	51	$\overline{BHE}$	76	A17/S4
2	T0OUT	27	DMAI1/P3.3	52	ALE	77	A16/S3
3	T0IN	28	P3.4	53	AD15	78	$\overline{S0}$
4	T1OUT	29	P3.5	54	AD14	79	$\overline{S1}$
5	T1IN	30	INT0	55	AD13	80	$\overline{S2}$
6	CLKOUT	31	INT1	56	AD12	81	PEREQ
7	RESOUT	32	INT2	57	AD11	82	NMI
8	$\overline{RESIN}$	33	INT3	58	AD10	83	$\overline{TEST}$
9	PDTMR	34	$\overline{INTA}$	59	AD9	84	$\overline{ERROR}$
10	CLKIN	35	$\overline{NCS}$	60	AD8	85	READY
11	OSCOUT	36	$\overline{WDTOUT}$	61	V_{SS}	86	V_{CC}
12	V_{SS}	37	V_{SS}	62	V_{CC}	87	V_{SS}
13	V_{CC}	38	V_{CC}	63	AD7	88	$\overline{UCS}$
14	V_{CC}	39	V_{SS}	64	AD6	89	$\overline{LCS}$
15	V_{SS}	40	INT4	65	AD5	90	P1.7/$\overline{GCS7}$
16	P2.0/RXD0	41	INT5	66	AD4	91	P1.6/$\overline{GCS6}$
17	P2.1/TXD0	42	INT6	67	V_{CC}	92	P1.5/$\overline{GCS5}$
18	P2.2/BCLK0	43	INT7	68	V_{SS}	93	P1.4/$\overline{GCS4}$
19	P2.3/$\overline{CTS0}$	44	HOLD	69	V_{CC}	94	P1.3/$\overline{GCS3}$
20	P2.4/RXD1	45	HLDA	70	AD3	95	P1.2/$\overline{GCS2}$
21	P2.5/TXD1	46	DT/$\overline{R}$	71	AD2	96	P1.1/$\overline{GCS1}$
22	P2.6/BCLK1	47	$\overline{DEN}$	72	AD1	97	P1.0/$\overline{GCS0}$
23	P2.7/$\overline{CTS1}$	48	$\overline{LOCK}$	73	AD0	98	DRQ0
24	P3.0/RXI1	49	$\overline{WR}$	74	A19/S6/$\overline{ONCE}$	99	DRQ1
25	P3.1/TXI1	50	$\overline{RD}$	75	A18/S5	100	DRQ2

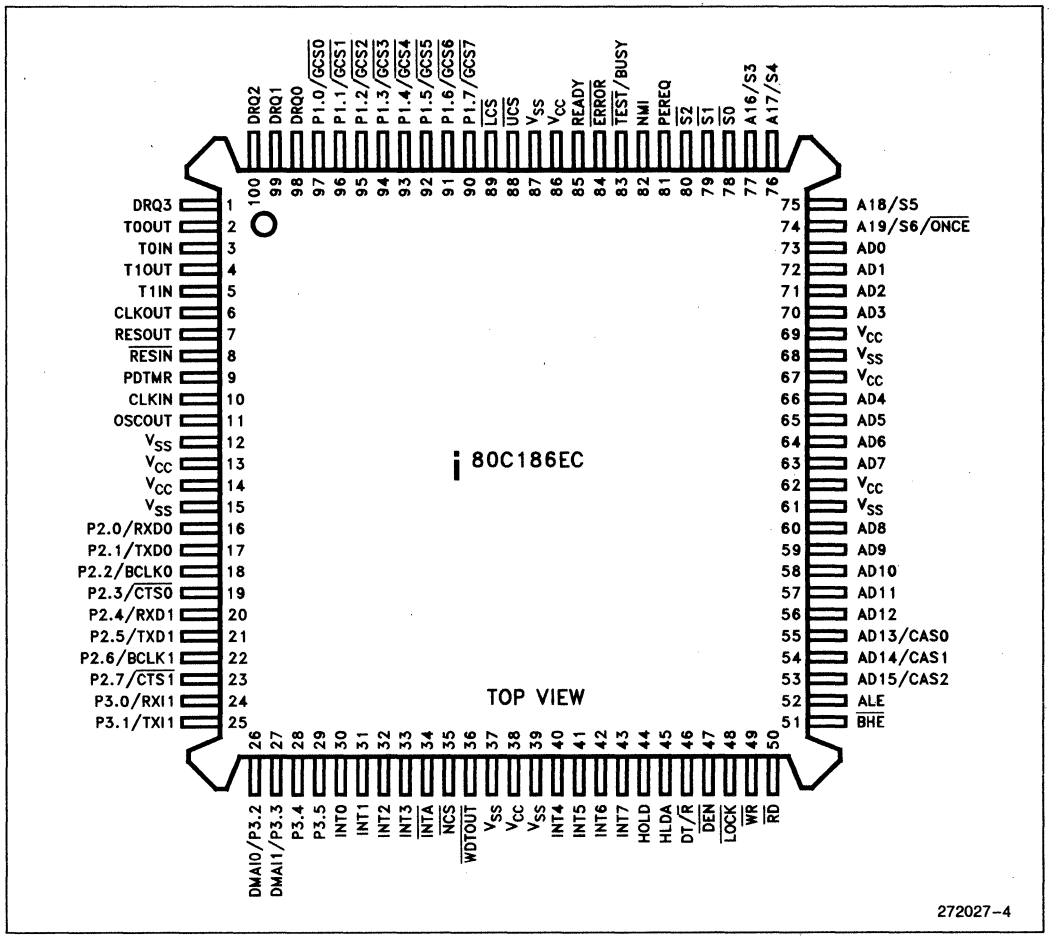

Figure 4. 100-Pin Plastic Quad Flat Pack Package (PQFP)

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Table 5. QFP Pin Names with Package Location

AD Bus	
Name	**Pin**
AD0	76
AD1	75
AD2	74
AD3	73
AD4	69
AD5	68
AD6	67
AD7	66
AD8	63
AD9	62
AD10	61
AD11	60
AD12	59
AD13/CAS0	58
AD14/CAS1	57
AD15/CAS2	56
A16/S3	80
A17/S4	79
A18/S5	78
A19/S6/$\overline{\text{ONCE}}$	77

Bus Control	
Name	**Pin**
ALE	55
$\overline{\text{BHE}}$	54
$\overline{\text{S0}}$	81
$\overline{\text{S1}}$	82
$\overline{\text{S2}}$	83
$\overline{\text{RD}}$	53
$\overline{\text{WR}}$	52
READY	88
$\overline{\text{DEN}}$	50
DT/$\overline{\text{R}}$	49
$\overline{\text{LOCK}}$	51
HOLD	47
HLDA	48
$\overline{\text{INTA}}$	37

Power and Ground	
Name	**Pin**
V_{CC}	16
V_{CC}	17
V_{CC}	41
V_{CC}	65
V_{CC}	70
V_{CC}	72
V_{CC}	89
V_{SS}	15
V_{SS}	18
V_{SS}	40
V_{SS}	42
V_{SS}	64
V_{SS}	71
V_{SS}	90

Processor Control	
Name	**Pin**
$\overline{\text{RESIN}}$	11
RESOUT	10
CLKIN	13
OSCOUT	14
CLKOUT	9
$\overline{\text{TEST}}$/BUSY	86
PEREQ	84
$\overline{\text{NCS}}$	38
$\overline{\text{ERROR}}$	87
PDTMR	12
NMI	85
INT0	33
INT1	34
INT2	35
INT3	36
INT4	43
INT5	44
INT6	45
INT7	46

I/O	
Name	**Pin**
$\overline{\text{UCS}}$	91
$\overline{\text{LCS}}$	92
P1.7/$\overline{\text{GCS7}}$	93
P1.6/$\overline{\text{GCS6}}$	94
P1.5/$\overline{\text{GCS5}}$	95
P1.4/$\overline{\text{GCS4}}$	96
P1.3/$\overline{\text{GCS3}}$	97
P1.2/$\overline{\text{GCS2}}$	98
P1.1/$\overline{\text{GCS1}}$	99
P1.0/$\overline{\text{GCS0}}$	100
P2.7/$\overline{\text{CTS1}}$	26
P2.6/BCLK1	25
P2.5/TXD1	24
P2.4/RXD1	23
P2.3/$\overline{\text{CTS0}}$	22
P2.2/BCLK0	21
P2.1/TXD0	20
P2.0/RXD0	19
P3.5	32
P3.4	31
P3.3/DMAI1	30
P3.2/DMAI0	29
P3.1/TXI1	28
P3.0/RXI1	27
T0IN	6
T0OUT	5
T1IN	8
T1OUT	7
DRQ0	1
DRQ1	2
DRQ2	3
DRQ3	4
$\overline{\text{WDTOUT}}$	39

Table 6. QFP Package Location with Pin Names

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DRQ0	26	P2.7/$\overline{CTS1}$	51	$\overline{LOCK}$	76	AD0
2	DRQ1	27	P3.0/RXI1	52	$\overline{WR}$	77	A19/S6/$\overline{ONCE}$
3	DRQ2	28	P3.1/TXI1	53	$\overline{RD}$	78	A18/S5
4	DRQ3	29	DMAI0/P3.2	54	$\overline{BHE}$	79	A17/S4
5	T0OUT	30	DMAI1/P3.3	55	ALE	80	A16/S3
6	T0IN	31	P3.4	56	AD15	81	$\overline{S0}$
7	T1OUT	32	P3.5	57	AD14	82	$\overline{S1}$
8	T1IN	33	INT0	58	AD13	83	$\overline{S2}$
9	CLKOUT	34	INT1	59	AD12	84	PEREQ
10	RESOUT	35	INT2	60	AD11	85	NMI
11	$\overline{RESIN}$	36	INT3	61	AD10	86	$\overline{TEST}$
12	PDTMR	37	$\overline{INTA}$	62	AD9	87	$\overline{ERROR}$
13	CLKIN	38	$\overline{NCS}$	63	AD8	88	READY
14	OSCOUT	39	$\overline{WDTOUT}$	64	V_{SS}	89	V_{CC}
15	V_{SS}	40	V_{SS}	65	V_{CC}	90	V_{SS}
16	V_{CC}	41	V_{CC}	66	AD7	91	$\overline{UCS}$
17	V_{CC}	42	V_{SS}	67	AD6	92	$\overline{LCS}$
18	V_{SS}	43	INT4	68	AD5	93	P1.7/$\overline{GCS7}$
19	P2.0/RXD0	44	INT5	69	AD4	94	P1.6/$\overline{GCS6}$
20	P2.1/TXD0	45	INT6	70	V_{CC}	95	P1.5/$\overline{GCS5}$
21	P2.2/BCLK0	46	INT7	71	V_{SS}	96	P1.4/$\overline{GCS4}$
22	P2.3/$\overline{CTS0}$	47	HOLD	72	V_{CC}	97	P1.3/$\overline{GCS3}$
23	P2.4/RXD1	48	HLDA	73	AD3	98	P1.2/$\overline{GCS2}$
24	P2.5/TXD1	49	DT/$\overline{R}$	74	AD2	99	P1.1/$\overline{GCS1}$
25	P2.6/BCLK1	50	$\overline{DEN}$	75	AD1	100	P1.0/$\overline{GCS0}$

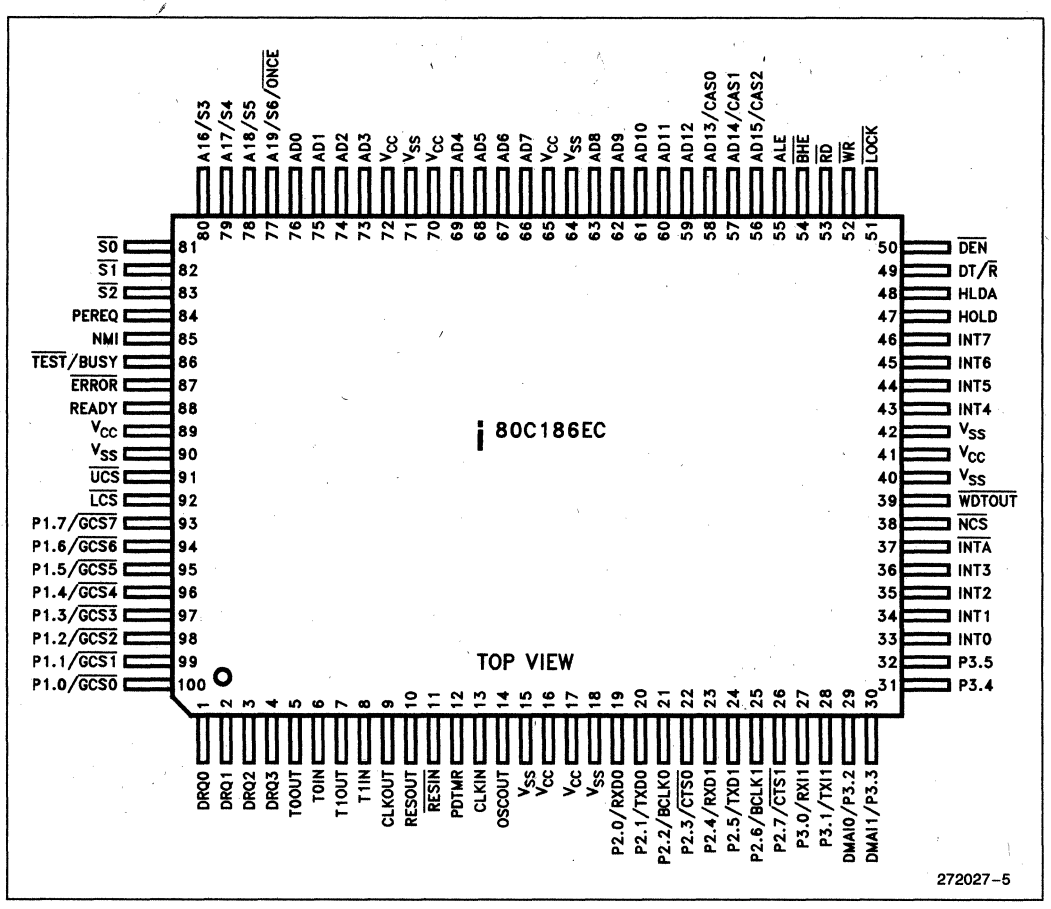

Figure 5. Quad Flat Pack (EIAJ) Pinout Diagram

PACKAGE THERMAL SPECIFICATIONS

The 80C186EC is specified for operation when T_C (the case temperature) is within the range of −40°C to +100°C. T_C may be measured in any environment to determine whether the 80C186EC is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P * \theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 7 for the 100-pin Quad Flat Pack (QFP) package.

Table 8 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies. P (the maximum power consumption—specified in Watts) is calculated by using the maximum I_{CC} and V_{CC} of 5.5V.

Table 7. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow in ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PQFP)	27.0	22.0	18.0	15.0	14.0	13.5
θ_{CA} (QFP)	64.5	55.5	51.0	TBD	TBD	TBD

Table 8. Maximum T_A at Various Airflows (in °C)

		Airflow in ft/min (m/sec)					
	T_F (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PQFP)	TBD	TBD	TBD	TBD	TBD	TBD	TBD
θ_{CA} (QFP)	TBD	TBD	TBD	TBD	TBD	TBD	TBD

ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Storage Temperature ..... −65°C to +150°C

Case Temperature Under Bias... −65°C to +100°C

Supply Voltage
with Respect to V_{SS} ..... −0.5V to +6.5V

Voltage on Other Pins
with Respect to V_{SS} ..... −0.5V to V_{CC} + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.5	5.5	V
T_F	Input Clock Frequency			
	80C186EC-16	0	32	MHz
	80C186EC-13	0	26.08	MHz
T_C	Case Temperature Under Bias			
	KU80C186EC-XX (PQFP)	−40°C	+100	°C
	S80C186EC-XX (QFP)	−40°C	+100	°C

Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80C186EC-based circuit board should include separate power (V_{CC}) and ground (V_{SS}) planes. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Liberal decoupling capacitance should be placed near the 80C186EC. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by placing the decoupling capacitors as close as possible to the 80C186EC V_{CC} and V_{SS} package pins.

Always connect any unused input to an appropriate signal level. In particular, unused interrupt inputs (NMI, INT0:7) should be connected to V_{SS} through a pull-down resistor. Leave any unused output pin unconnected.

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	−0.5	0.3*V_{CC}	V	
V_{IH}	Input High Voltage	0.7*V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 3 mA (Min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −2 mA (Min)
V_{HYR}	Input Hysteresis on $\overline{RESIN}$	0.5		V	
I_{LI}	Input Leakage Current for Pins: AD15:0, READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$/BUSY, NMI, INT7:0, T0IN, T1IN, P2.7–P2.0, P3.5–P3.0, DRQ3:0, PEREQ, $\overline{ERROR}$		±15	μA	0 ≤ V_{IN} ≤ V_{CC}
I_{LIU}	Input Leakage for Pins with Pullups Active During Reset: A19:16, $\overline{LOCK}$	−0.2	−5	mA	V_{IN} = 0.7 V_{CC} (Note 1)
I_{LO}	Output Leakage for Floated Output Pins		±15	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 2)
I_{CC}	Supply Current Cold (in RESET) 80C186EC-16 80C186EC-13		 85 70	 mA mA	(Note 3)
I_{ID}	Supply Current in Idle Mode 80C186EC-16 80C186EC-13		 60 50	 mA mA	(Note 4)
I_{PD}	Supply Current in Powerdown Mode 80C186EC-16 80C186EC-13		 100 100	 μA μA	(Note 5)
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 6)

NOTES:
1. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
2. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
3. Measured with the device in RESET and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
4. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
5. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
6. Output Capacitance is the capacitive load of a floating output pin.

I_{CC} versus Frequency and Voltage

The I_{CC} consumed by the 80C186EC is composed of two components:

1. I_{PD}—The quiescent current that represents internal device leakage. Measured with all inputs at either V_{CC} or ground and no clock applied.
2. I_{CCS}—The switching current used to charge and discharge internal parasitic capacitance when changing logic levels. I_{CCS} is related to both the frequency of operation and the device supply voltage (V_{CC}). I_{CCS} is given by the formula:

$$\text{Power} = V * I = V^2 * C_{DEV} * f$$
$$\therefore I_{CCS} = V * C_{DEV} * f$$

Where:

V = Supply Voltage (V_{CC})

C_{DEV} = Device Capacitance

f = Operating Frequency

Measuring C_{PD} on a device like the 80C186EC would be difficult. Instead, C_{PD} is calculated using the above formula with I_{CC} values measured at known V_{CC} and frequency. Using the C_{PD} value, the user can calculate I_{CC} at any voltage and frequency within the specified operating range.

Example. Calculate typical I_{CC} at 14 MHz, 5.2V V_{CC}.

$I_{CC} = I_{PD} + I_{CCS}$
$= 0.1\text{ mA} + 5.2V * 0.77 * 14\text{ MHz}$
$= 56.2\text{ mA}$

PDTMR Pin Delay Calculation

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown Mode. A delay is required only when using the on chip oscillator to allow the crystal or resonator circuit to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e. a device reset while in Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized.

To calculate the value of capacitor to use to provide a desired delay, use the equation:

$$440 \times t = C_{PD}\ (5V, 25°C)$$

Where:

t = desired delay in **seconds**
C_{PD} = capacitive load on PDTMR in **microfarads**

Example. For a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6} = 0.132\ \mu F$ is required. Round up to a standard (available) capacitor value.

NOTE:
The above equation applies to delay time longer than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% to −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperatures will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

Parameter	Target Typical	Target Max	Units	Notes
CPD	0.77	1.37	mA/V*MHz	1, 2
CPD (Idle Mode)	0.55	0.96	mA/V*MHz	1, 2

NOTES:
1. Maximum C_{PD} is measured at −40°C with all outputs loaded as specified in the AC test conditions and the device in reset (or Idle Mode). Due to tester limitations, CLKOUT and OSCOUT also have 50 pF loads that increase I_{CC} by V*C*F.
2. Typical C_{PD} is calculated at 25°C assuming no loads on CLKOUT or OSCOUT and the device in reset (or Idle Mode).

AC SPECIFICATIONS

AC Characteristics—80C186EC-16

Symbol	Parameter	TARGET Min	TARGET Max	Unit	Notes
INPUT CLOCK					
TF	CLKIN Frequency	0	32	MHz	1
TC	CLKIN Period	31.25	∞	ns	1
TCH	CLKIN High Time	10	∞	ns	1, 2
TCL	CLKIN Low Time	10	∞	ns	1, 2
TCR	CLKIN Rise Time	1	10	ns	1, 3
TCF	CLKIN Fall Time	1	10	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	20	ns	1, 4
T	CLKOUT Period		2 * TC	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	22	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$, $\overline{NCS}$, $\overline{WDTOUT}$	3	27	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	22	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GSC7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0, $\overline{NCS}$, $\overline{INTA}$, $\overline{S2:0}$	3	27	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	25	ns	1
INPUT REQUIREMENTS					
T_{CHIS}	$\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, BCLK1:0, P3.4, P3.5	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, DRQ1:0, BCLK1:0, P3.4, P3.5	3		ns	1, 9
T_{CLIS}	AD15:0, READY	10		ns	1, 10
T_{CLIH}	AD15:0, READY	3		ns	1, 10
T_{CLIS}	HOLD, $\overline{RESIN}$, PEREQ, $\overline{ERROR}$, DRQ3:0	10		ns	1, 9
T_{CLIH}	HOLD, $\overline{RESIN}$, REREQ, $\overline{ERROR}$, DRQ3:0	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 16 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 17 for rise and fall times outside 50 pF.
6. See Figure 17 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C186EC operation.

AC Characteristics—80C186EC-13

Symbol	Parameter	TARGET Min	TARGET Max	Unit	Notes
INPUT CLOCK					
TF	CLKIN Frequency	0	26.08	MHz	1
TC	CLKIN Period	38.34	∞	ns	1
TCH	CLKIN High Time	12	∞	ns	1, 2
TCL	CLKIN Low Time	12	∞	ns	1, 2
TCR	CLKIN Rise Time	1	10	ns	1, 3
TCF	CLKIN Fall Time	1	10	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	23	ns	1, 4
T	CLKOUT Period		2 * TC	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	25	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$, $\overline{NCS}$, $\overline{WDTOUT}$	3	30	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	25	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0, $\overline{NCS}$, $\overline{INTA}$, $\overline{S2:0}$	3	30	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	30	ns	1
INPUT REQUIREMENTS					
T_{CHIS}	$\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, BCLK1:0, P3.4, P3.5	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, DRQ3:0, BCLK1:0, P3.4, P3.5	3		ns	1, 9
T_{CLIS}	AD15:0, READY	10		ns	1, 10
T_{CLIH}	AD15:0, READY	3		ns	1, 10
T_{CLIS}	HOLD, $\overline{RESIN}$, PEREQ, $\overline{ERROR}$, DRQ3:0	10		ns	1, 9
T_{CLIH}	HOLD, $\overline{RESIN}$, REREQ, $\overline{ERROR}$, DRQ3:0	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 16 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 17 for rise and fall times outside 50 pF.
6. See Figure 17 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C186EC operation.

Relative Timings—80C186EC-16, 13

Symbol	Parameter	TARGET Min	TARGET Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Active Pulse Width	T − 15		ns	
T_{AVLL}	AD Valid Setup before ALE Falls	½T − 10		ns	
T_{PLLL}	Chip Select Valid before ALE Falls	½T − 10		ns	1
T_{LLAX}	AD Hold after ALE Falls	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{WHLH}	$\overline{WR}$ Rising to Next ALE Rising	½T − 10		ns	1
T_{AFRL}	AD Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Active Pulse Width	2T − 5		ns	2
T_{WLWH}	$\overline{WR}$ Active Pulse Width	2T − 5		ns	2
T_{RHAX}	$\overline{RD}$ Rising to Next Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHPH}	$\overline{WR}$ Rise to Chip Select Rise	½T − 10		ns	1
T_{RHPH}	$\overline{RD}$ Rise to Chip Select Rise	½T − 10		ns	1
T_{PHPL}	Chip Select Inactive to Next Chip Select Active	½T − 10		ns	1
T_{OVRH}	$\overline{ONCE}$ Active Setup to $\overline{RESIN}$ Rising	T		ns	
T_{RHOX}	$\overline{ONCE}$ Hold after $\overline{RESIN}$ Rise	T		ns	
T_{IHIL}	$\overline{INTA}$ High to Next $\overline{INTA}$ Low during INTA Cycle	4T − 5		ns	4
T_{ILIH}	$\overline{INTA}$ Active Pulse Width	2T − 5		ns	2, 4
T_{CVIL}	CAS2:0 Setup before 2nd $\overline{INTA}$ Pulse Low	8T		ns	2, 4
T_{ILCX}	CAS2:0 Hold after 2nd $\overline{INTA}$ Pulse Low	4T		ns	2, 4
T_{IRES}	Interrupt Resolution Time		150	ns	3
T_{IRLH}	IR Low Time to Reset Edge Detector	50		ns	
T_{IRHIF}	IR Hold Time after 1st $\overline{INTA}$ Falling	25		ns	4, 5

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Interrupt resolution time is the delay between an unmasked interrupt request going active and the interrupt output of the 8259A module going active. This is not directly measureable by the user. For interrupt pin INT7 the delay from an active signal to an active input to the CPU would actually be twice the T_{IRES} value since the signal must pass through two 8259A modules.
4. See INTA Cycle Waveforms for definition.
5. To guarantee interrupt is not spurious.

Serial Port Mode 0 Timings—80C186EC-16, 13

Symbol	Parameter	TARGET Min	TARGET Max	Unit	Notes
RELATIVE TIMINGS					
T_{XLXL}	TXD Clock Period	T (n + 1)		ns	1, 2
T_{XLXH}	TXD Clock Low to Clock High (N > 1)	2T − 35	2T + 35	ns	1
T_{XLXH}	TXD Clock Low to Clock High (N = 1)	T − 35	T + 35	ns	1
T_{XHXL}	TXD Clock High to Clock Low (N > 1)	(n − 1) T − 35	(n − 1) T + 35	ns	1, 2
T_{XHXL}	TXD Clock High to Clock Low (N = 1)	T − 35	T + 35	ns	1
T_{QVXH}	RXD Output Data Setup to TXD Clock High (N > 1)	(n − 1)T − 35		ns	1, 2
T_{QVXH}	RXD Output Data Setup to TXD Clock High (N = 1)	T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (N > 1)	2T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (N = 1)	T − 35		ns	1
T_{XHQZ}	RXD Output Data Float after Last TXD Clock High		T + 20	ns	1
T_{DVXH}	RXD Input Data Setup to TXD Clock High	T + 20		ns	1
T_{XHDX}	RXD Input Data Setup after TXD Clock High	0		ns	1

NOTES:
1. See Figure 15 for Waveforms.
2. n is the value in the BxCMP register ignoring the ICLK bit.

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 6. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms for AC specification definitions, test pins and illustrations.

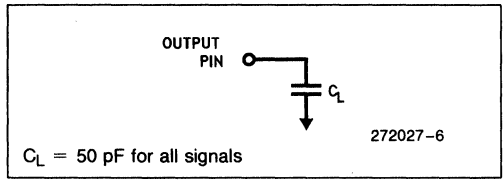

Figure 6. AC Test Load

AC TIMING WAVEFORMS

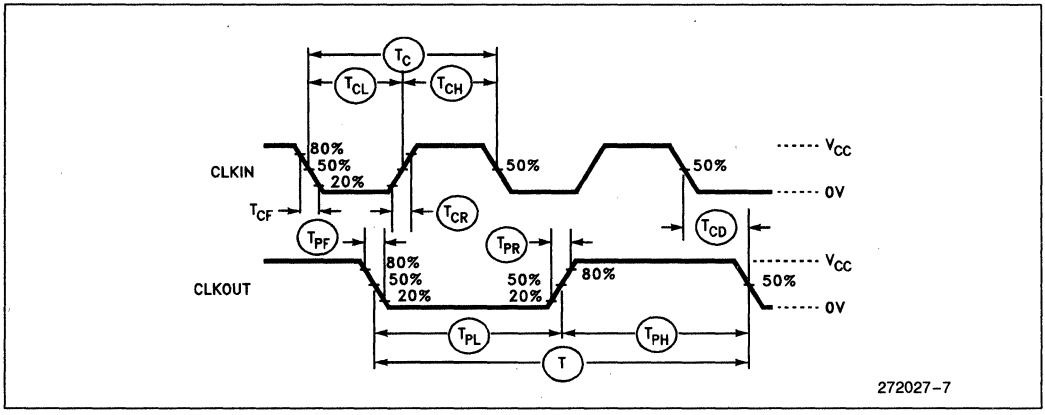

Figure 7. Input and Output Clock Waveforms

24

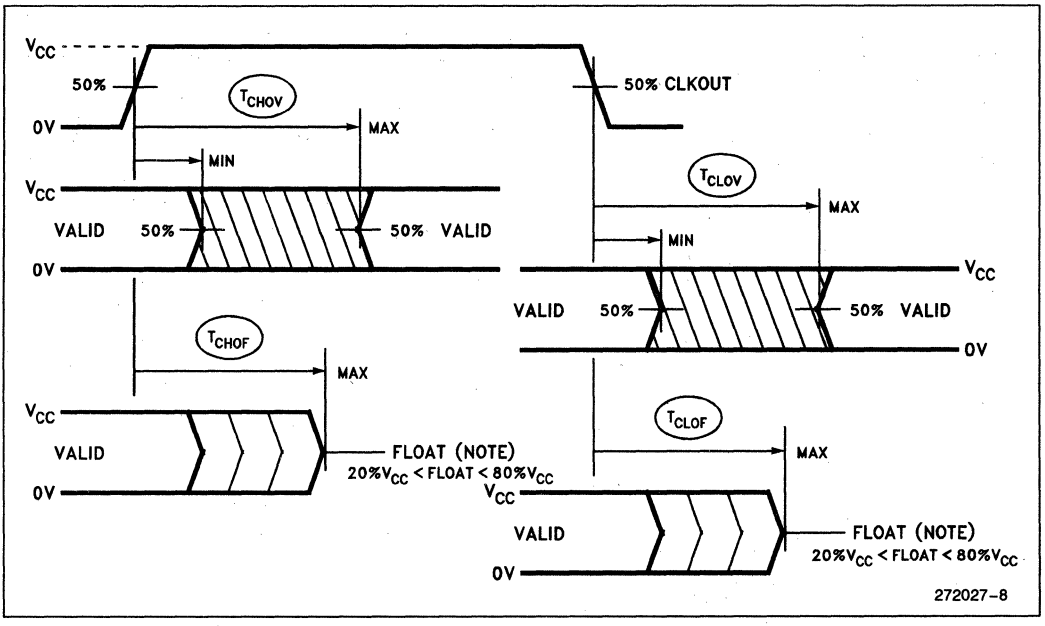

Figure 8. Output Delay and Float Waveforms

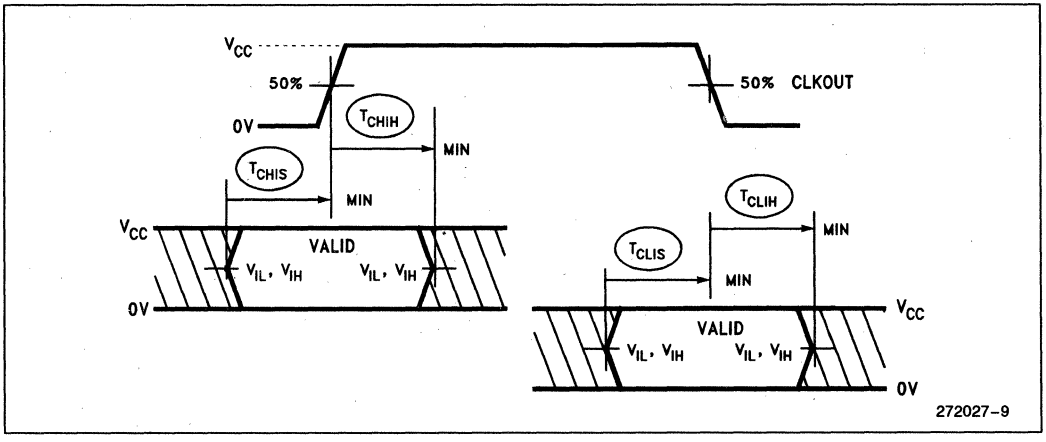

Figure 9. Input Setup and Hold

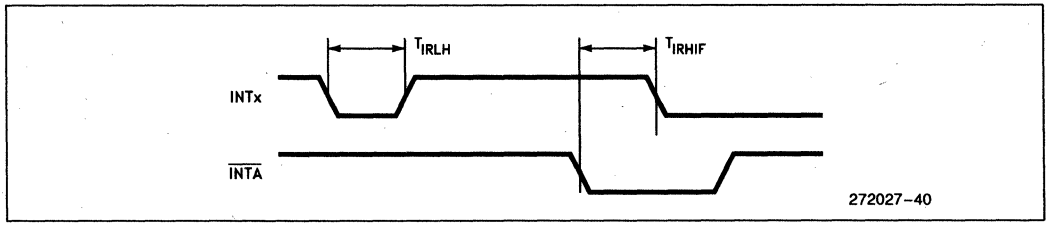

Figure 10. Relative Interrupt Signal Timings

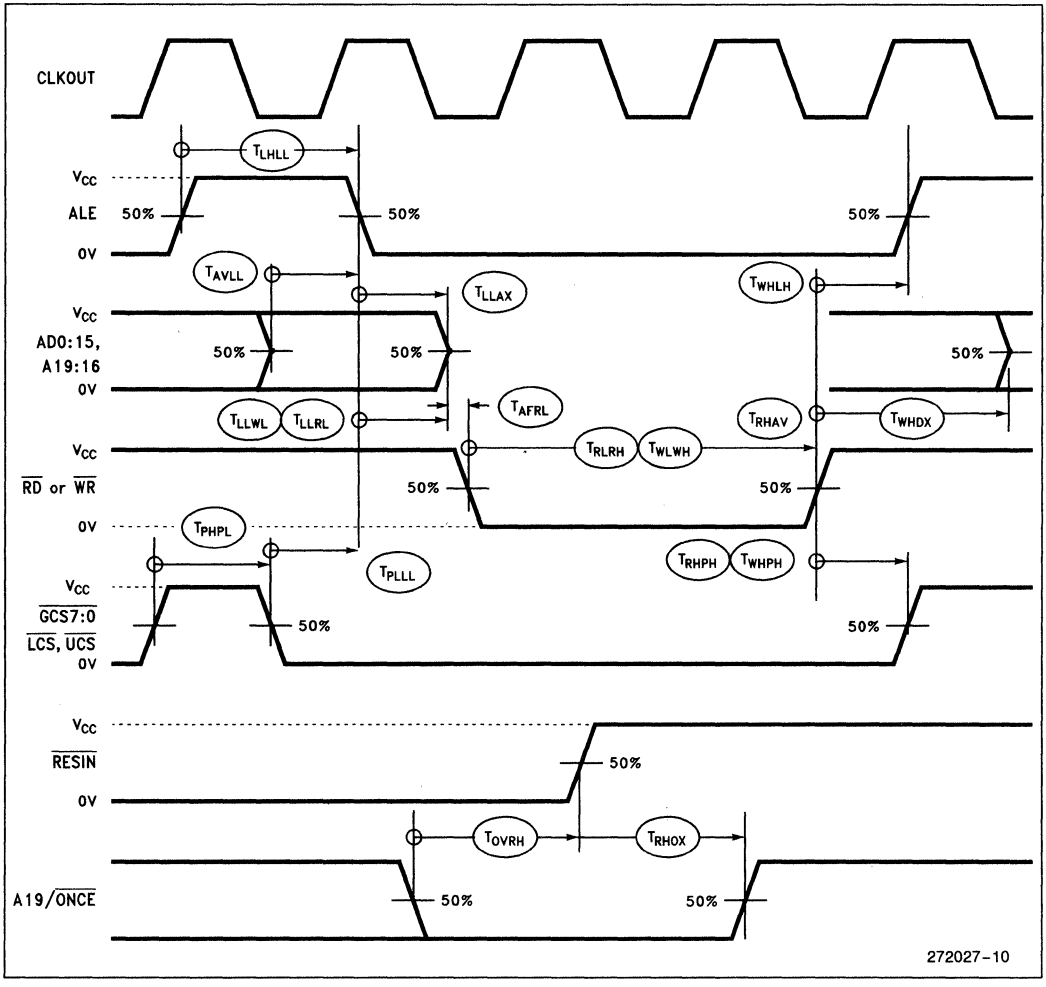

Figure 11. Relative Signal Waveform

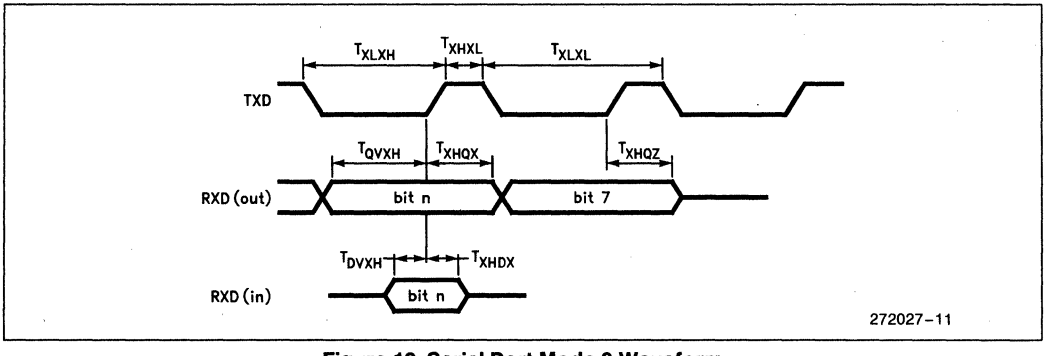

Figure 12. Serial Port Mode 0 Waveform

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DERATING CURVES

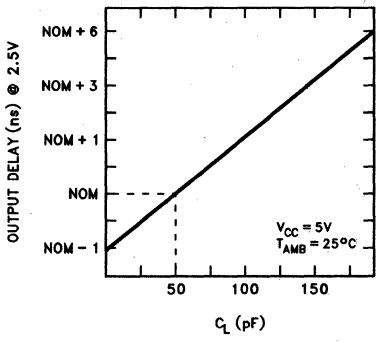


Figure 13. Typical Output Delay Variations versus Load Capacitance

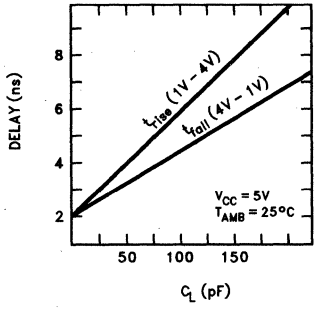


Figure 14. Typical Rise and Fall Variations versus Load Capacitance

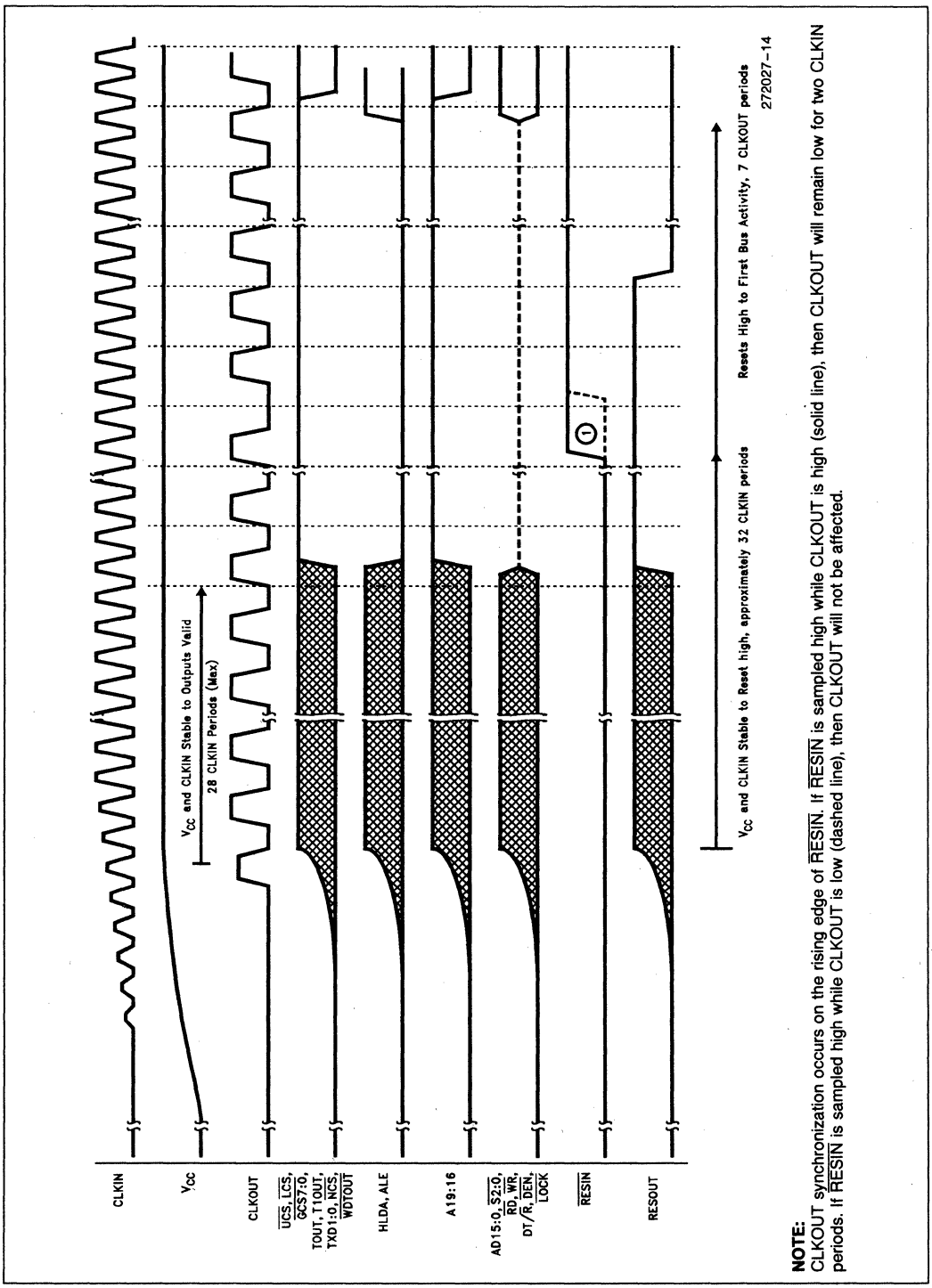
RESET

The 80C186EC will perform a reset operation any time the $\overline{\text{RESIN}}$ pin is active. The $\overline{\text{RESIN}}$ pin is synchronized before it is presented internally, which means that the clock must be operating before a reset can take effect. From a power-on state, $\overline{\text{RESIN}}$ must be held active (low) in order to guarantee correct initialization of the 80C186EC. **Failure to provide $\overline{\text{RESIN}}$ while the device is powering up will result in unspecified operation of the device.**

Figure 15 shows the correct reset sequence when first applying power to the 80C186EC. An external clock connected to CLKIN must not exceed the V_{CC} threshold being applied to the 80C186EC. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the 80C186EC. When attaching a crystal to the device, $\overline{\text{RESIN}}$ must remain active until both V_{CC} and CLKOUT are stable (the length of time is application specific and depends on the startup characteristics of the crystal circuit). The $\overline{\text{RESIN}}$ pin is designed to operate correctly using a RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that $\overline{\text{RESIN}}$ is never sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Figure 16 shows the timing sequence when $\overline{\text{RESIN}}$ is applied after V_{CC} is stable and the device has been operating. Note that a reset will terminate all activity and return the 80C186EC to a known operating state. Any bus operation that is in progress at the time $\overline{\text{RESIN}}$ is asserted will terminate immediately (note that most control signals will be driven to their inactive state first before floating).

While $\overline{\text{RESIN}}$ is active, bus signals $\overline{\text{LOCK}}$, A19/S16/$\overline{\text{ONCE}}$ and A18:16 are configured as inputs and weakly held high by internal pullup transistors. Only A19/$\overline{\text{ONCE}}$ can be overdriven to a low and is used to enable the ONCE™ Mode. Forcing $\overline{\text{LOCK}}$ or A18:16 low at any time while $\overline{\text{RESIN}}$ is low is prohibited and will cause unspecified device operation.



NOTE:
CLKOUT synchronization occurs on the rising edge of $\overline{RESIN}$. If $\overline{RESIN}$ is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If $\overline{RESIN}$ is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.

Figure 15. Cold RESET Waveforms

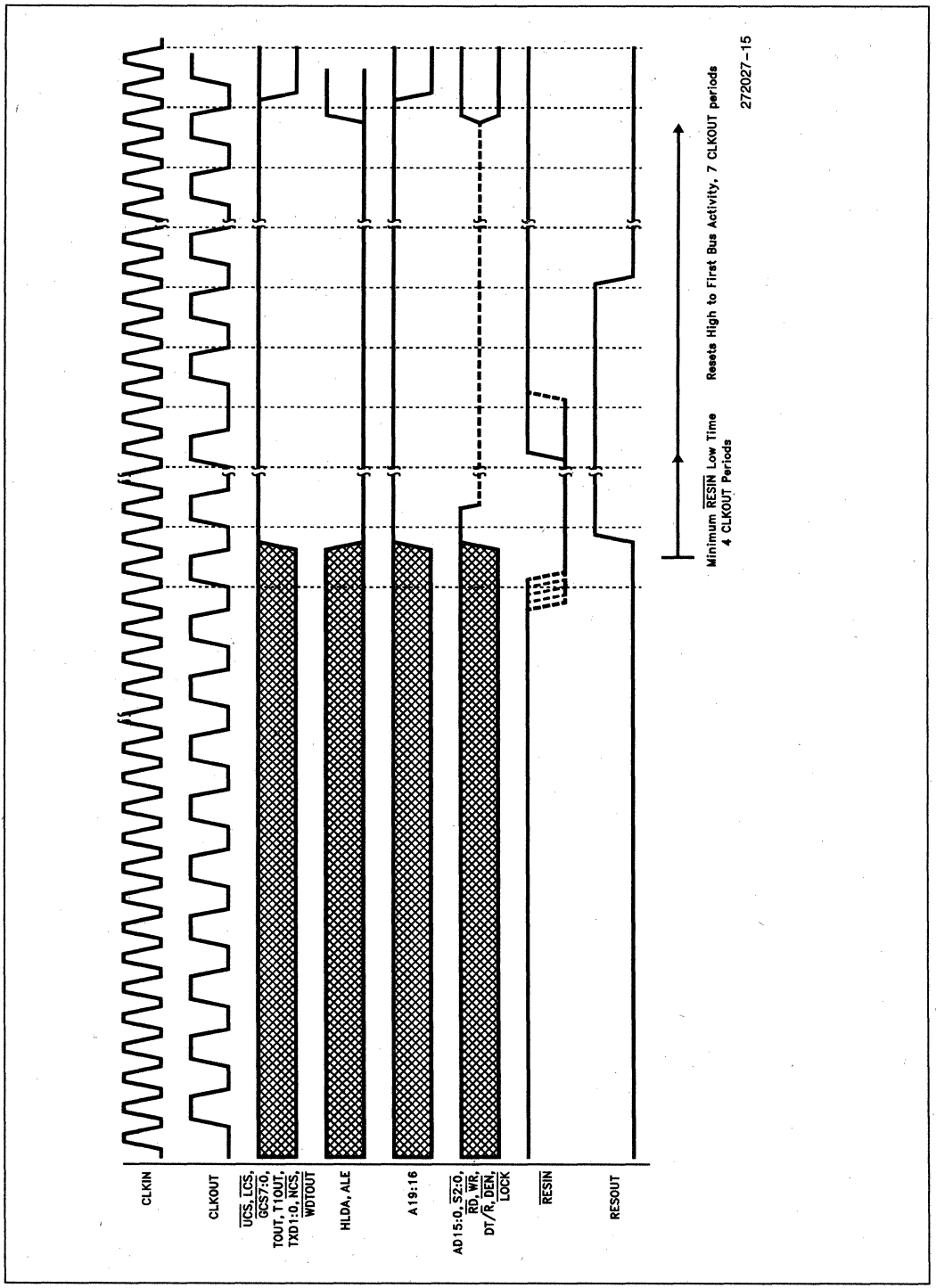


Figure 16. Warm RESET Waveforms

BUS CYCLE WAVEFORMS

Figures 17 through 23 present the various bus cycles that are generated by the 80C186EC. What is shown in the figure is the relationship of the various bus signals to CLKOUT. These figures along with the information present in Section 4.5, AC Specifications, allow the user to determine all the critical timing analysis needed for a given application.

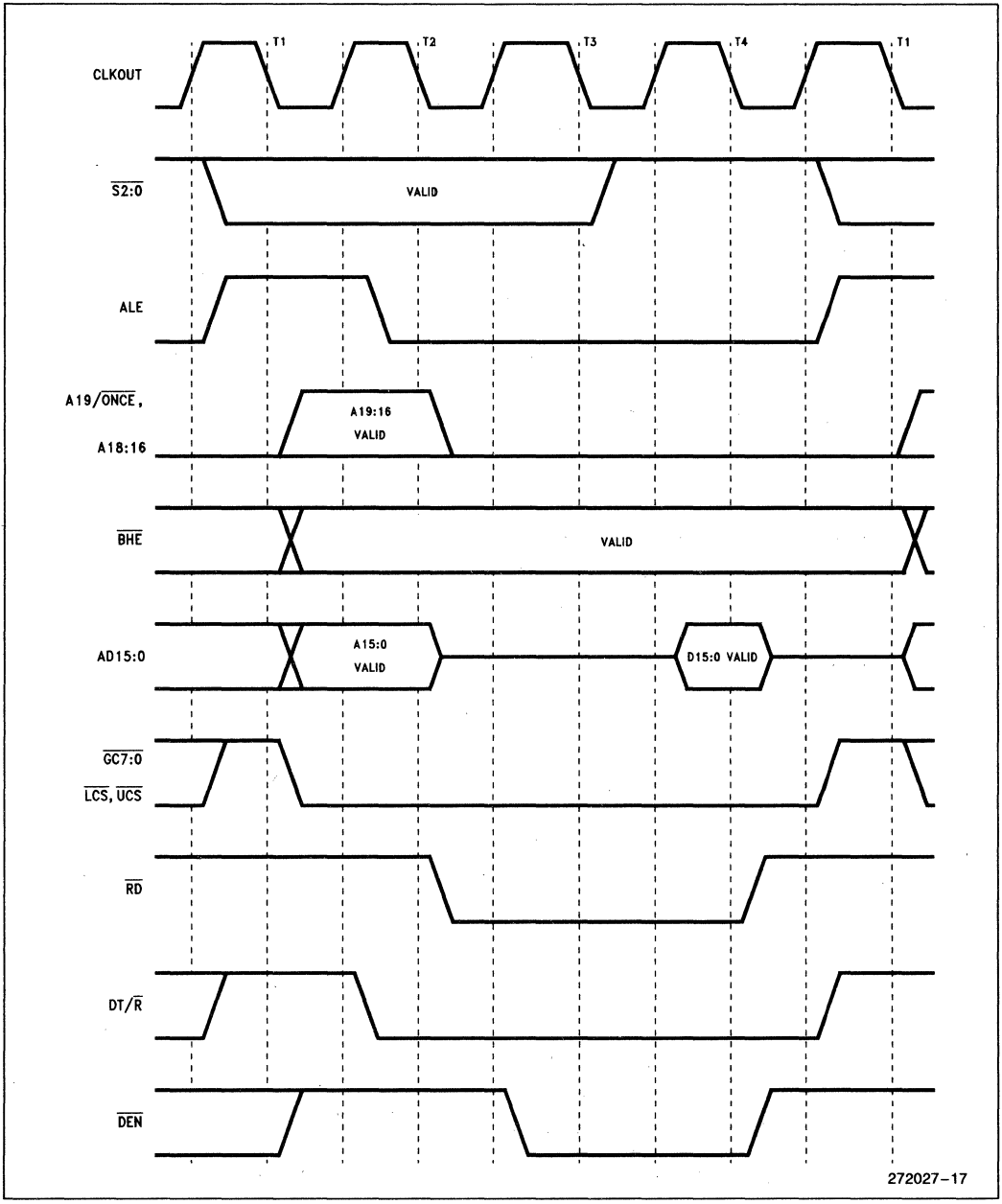


Figure 17. Memory Read, I/O Read, Instruction Fetch and Refresh Waveform

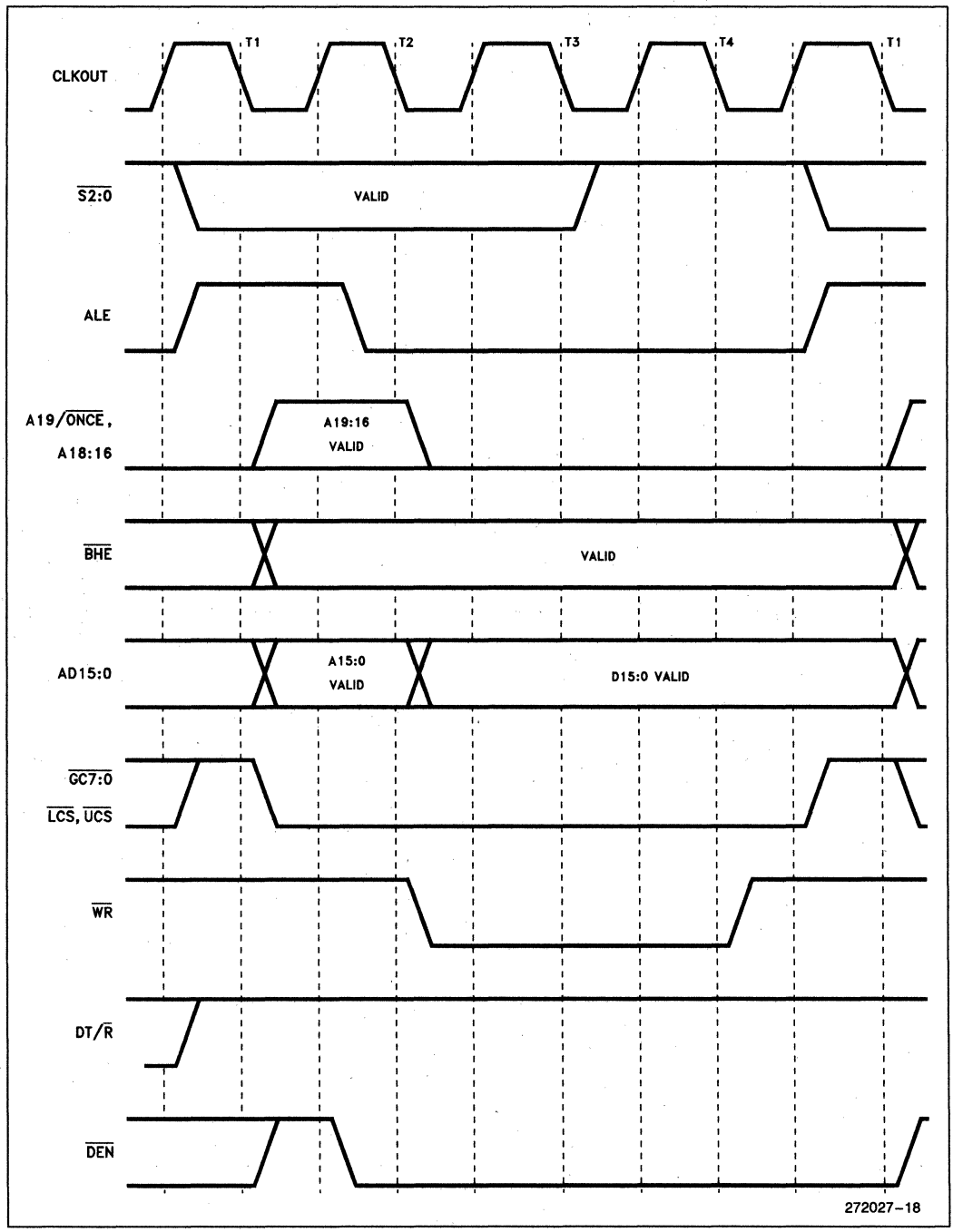
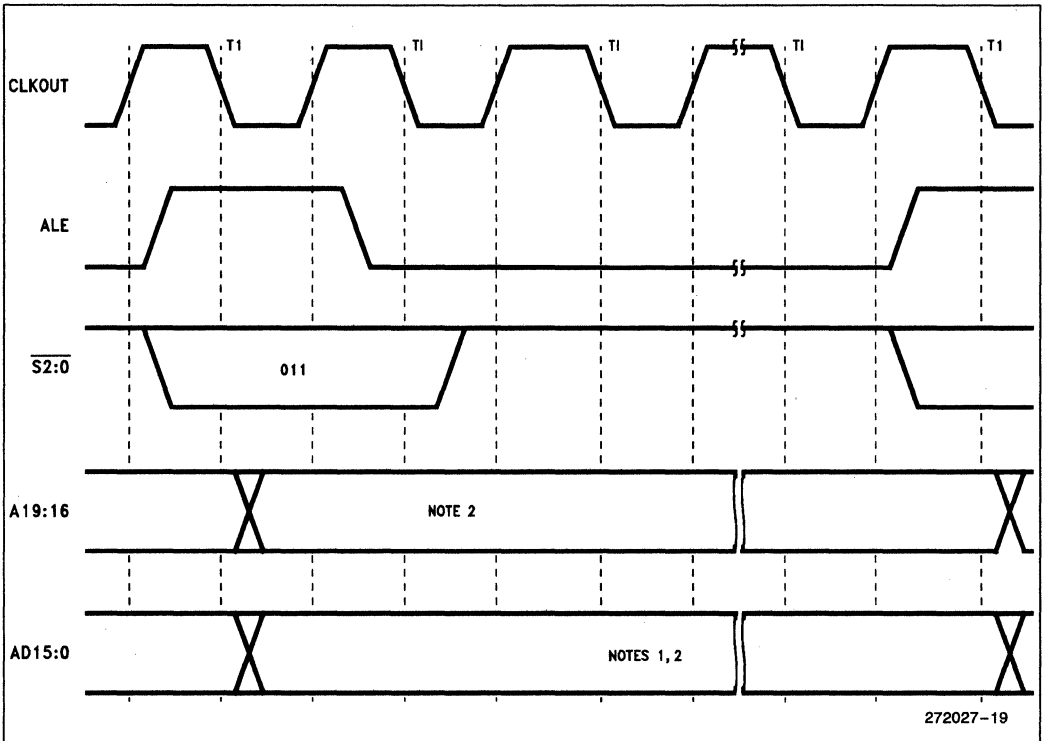


Figure 18. Memory Write and I/O Write Cycle Waveform



NOTES:
1. Address information is invalid. If previous bus cycle was a read, then the AD15:0 lines will float during T1. Otherwise, the AD15:0 lines will continue to drive during T1 (data is invalid). All other control lines are in their inactive state.
2. All address lines drive zeros while in Powerdown or Idle Mode.

Figure 19. Halt Cycle Waveform

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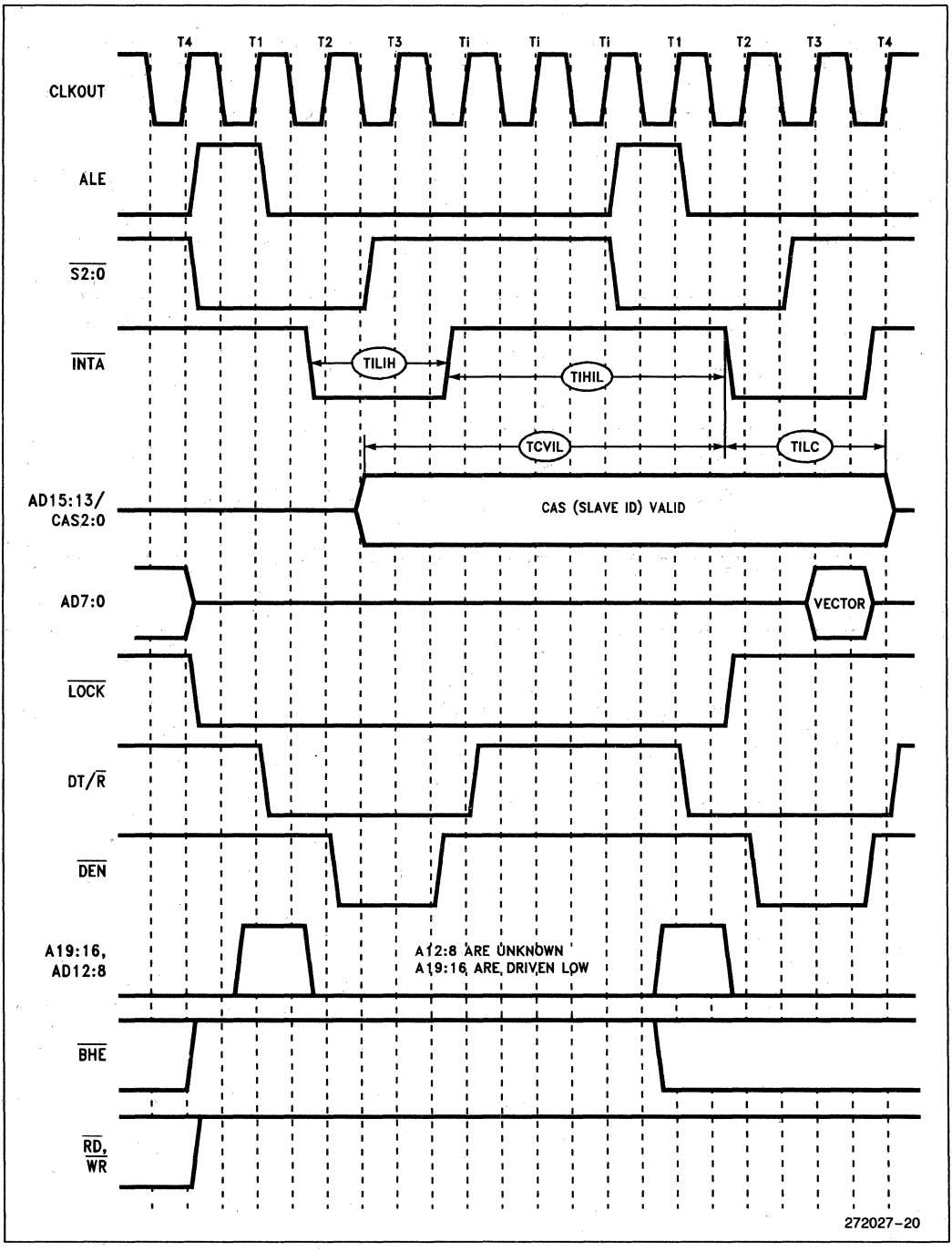


Figure 20. Interrupt Acknowledge Cycle Waveform

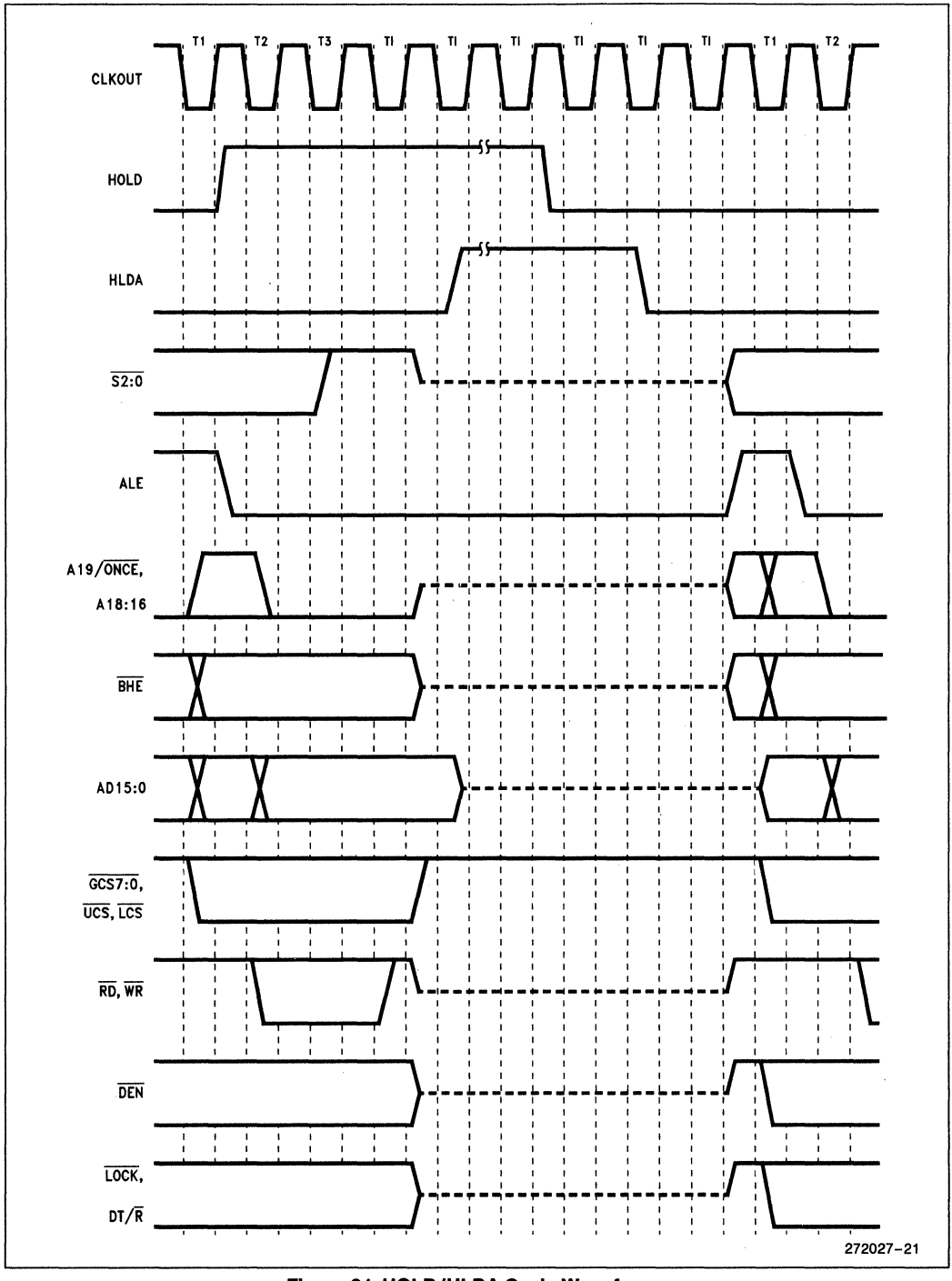


Figure 21. HOLD/HLDA Cycle Waveforms

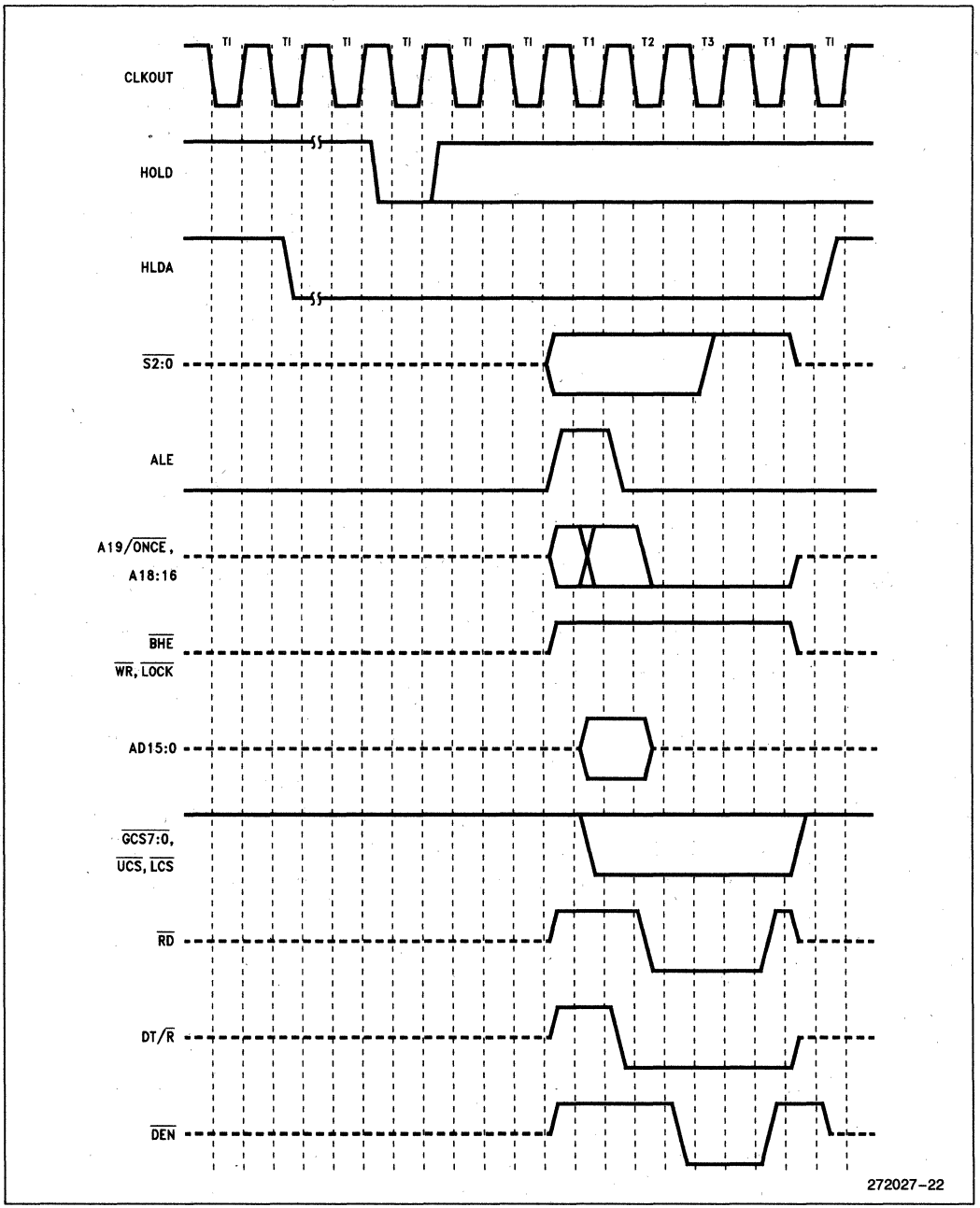
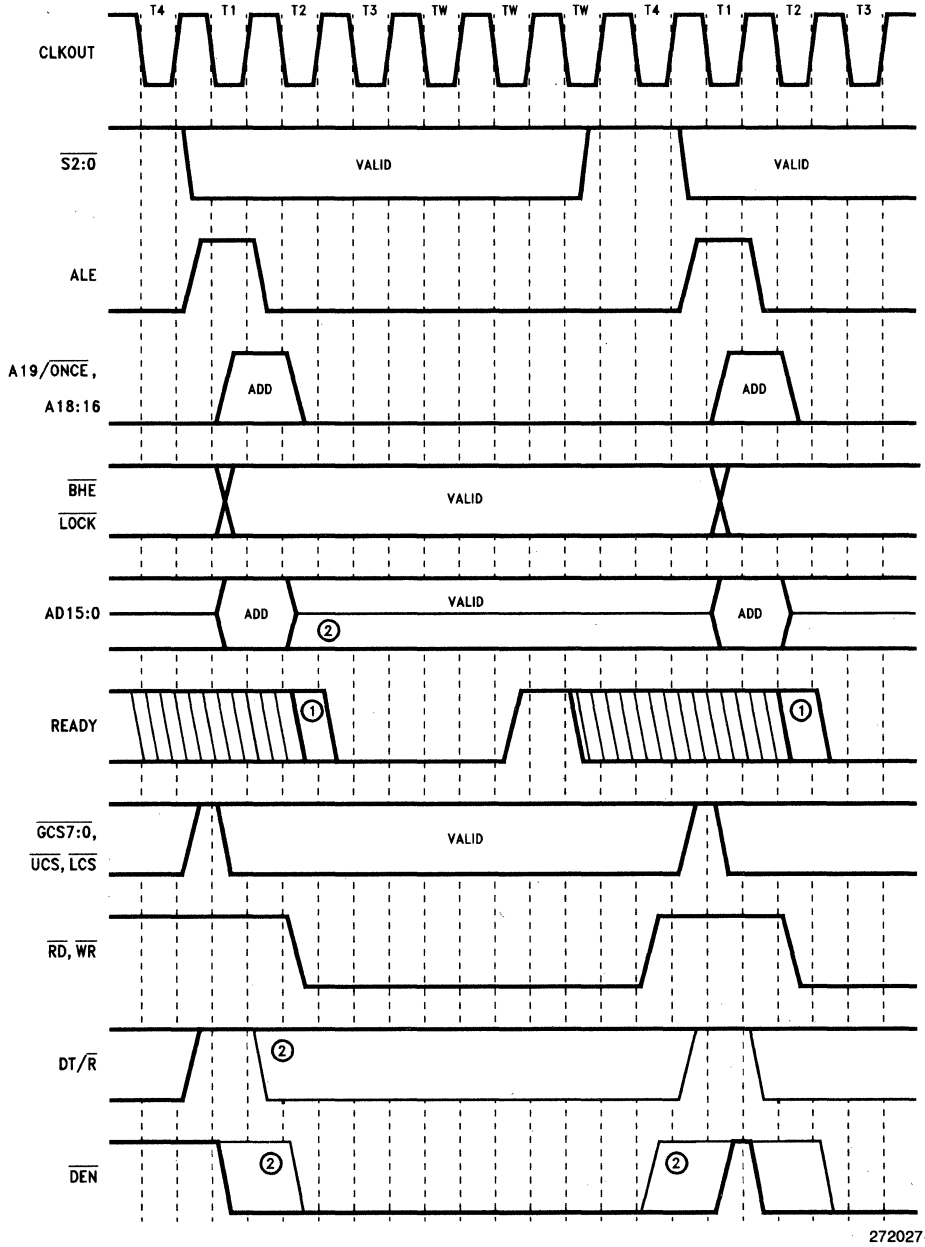


Figure 22. Refresh during HLDA Waveforms



NOTES:
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.

Figure 23. READY Cycle Waveforms

REGISTER BIT SUMMARY

Figures 24 through 37 present the bit definition of each register that is active (not reserved) in the Peripheral Control Block (PCB). Each register can be thought to occupy one word (16-bits) of either memory or I/O space, although not all bits in the register necessarily have a function. A register bit is not guaranteed to return a specific logic value if an "X" appears for the bit definition (i.e., if a zero was written to the register bit it may not be returned as a zero when read). Furthermore, a 0 must be written to any bit that is indicated by an "X" to ensure compatibility with future products or potential product changes. Any register bit that has a specific value in it (a "0" or a "1"), must be written to that value in order to guarantee proper operation of the 80C186EC.

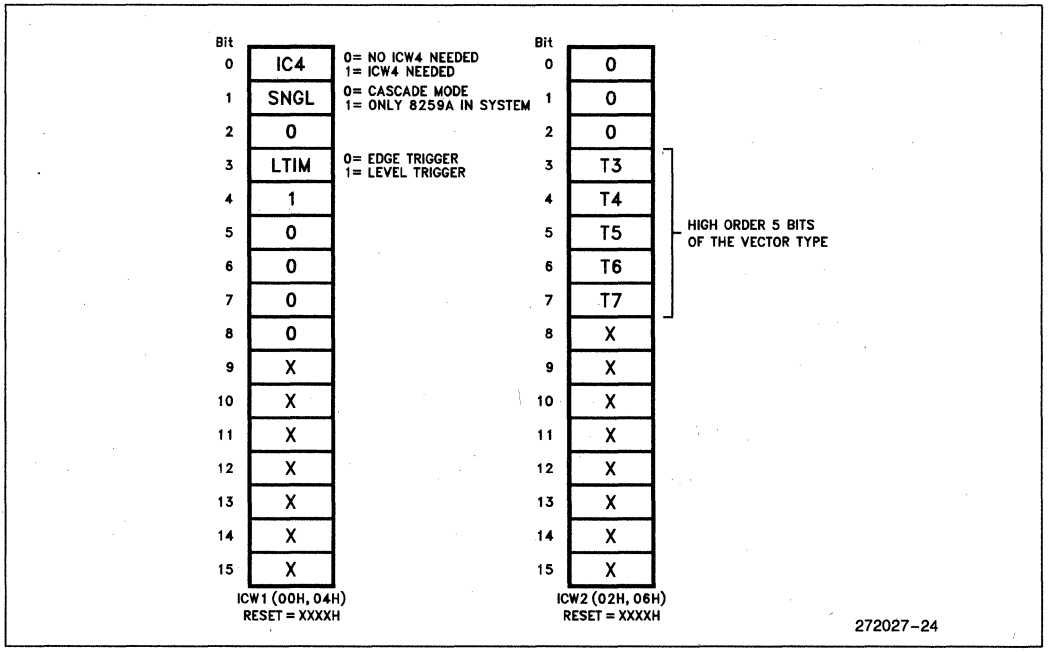


Figure 24. 8259A Module Initialization Command Words (ICWs)

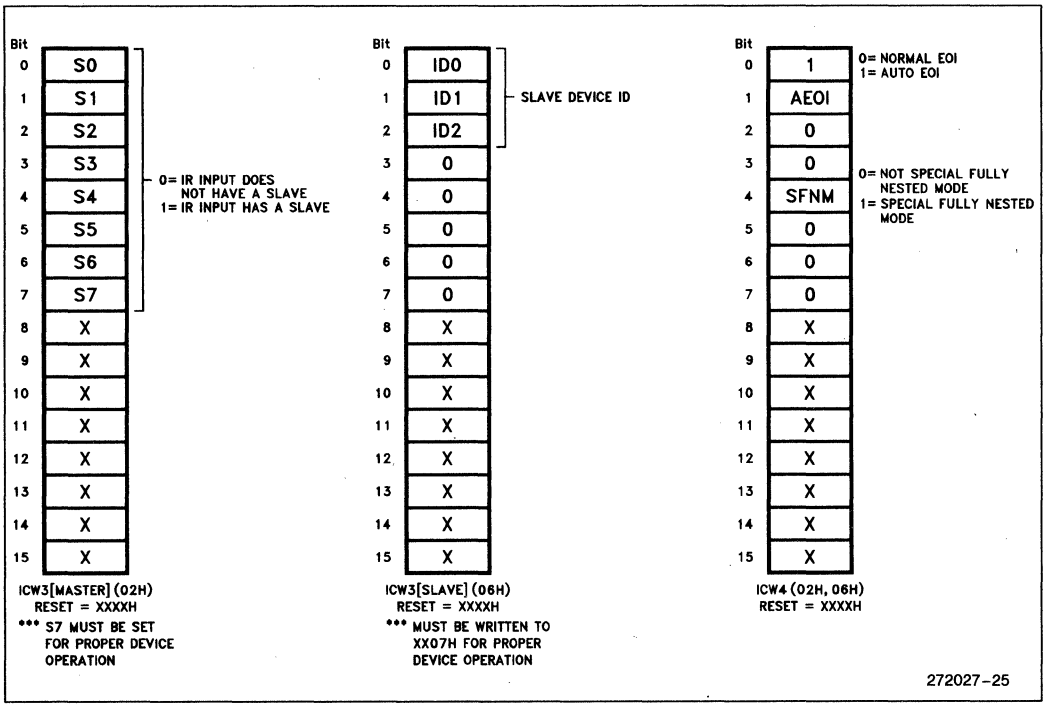


Figure 25. 8259A Module Initialization Command Words (ICWs) (Continued)

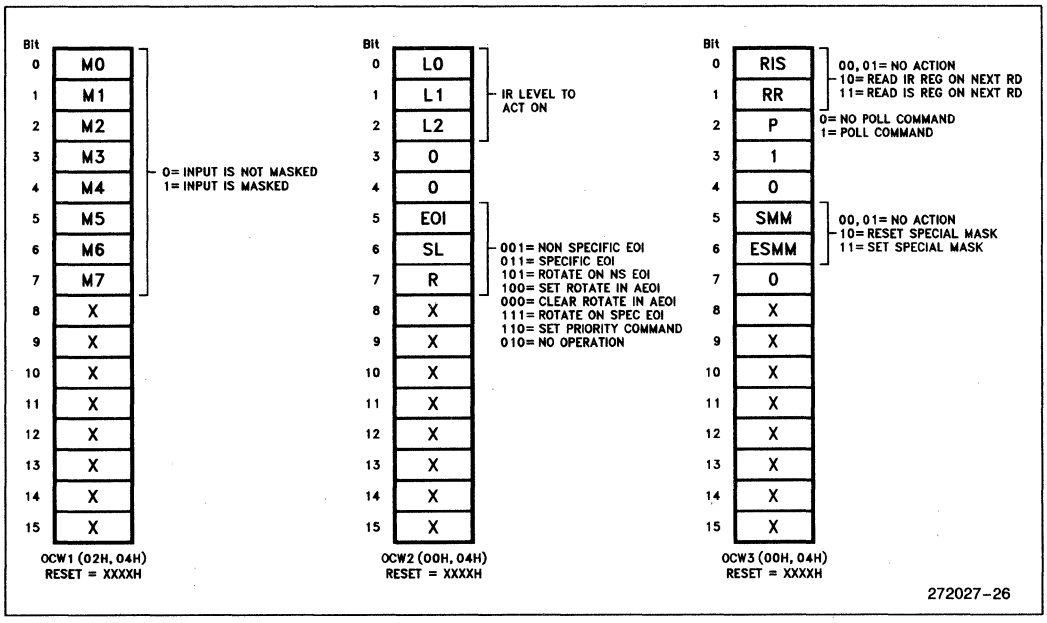


Figure 26. 8259A Module Operation Command Words

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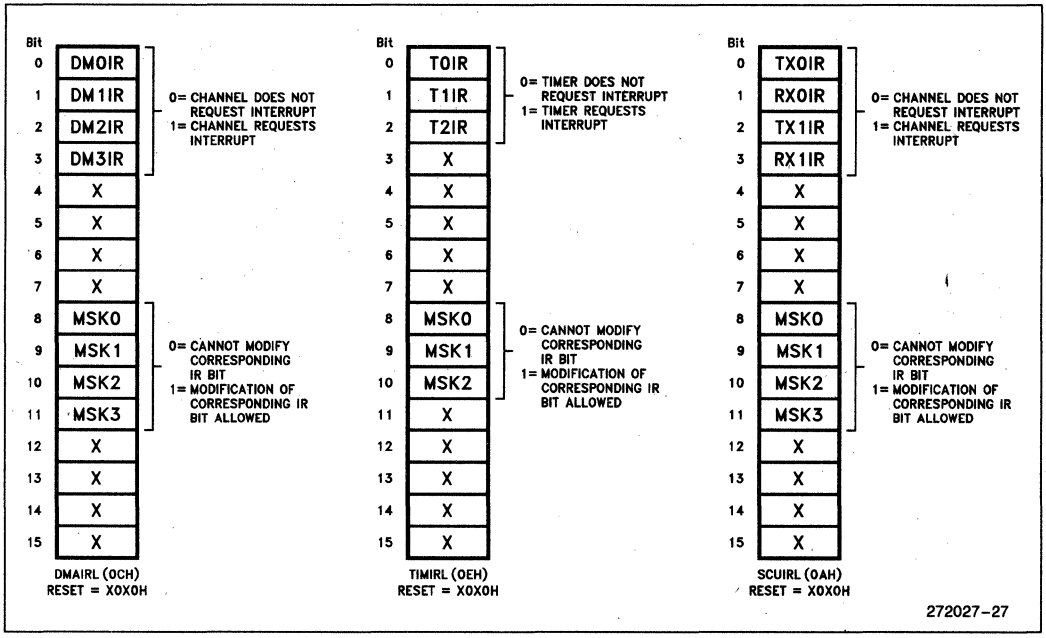

Figure 27. Interrupt Request Latch Registers

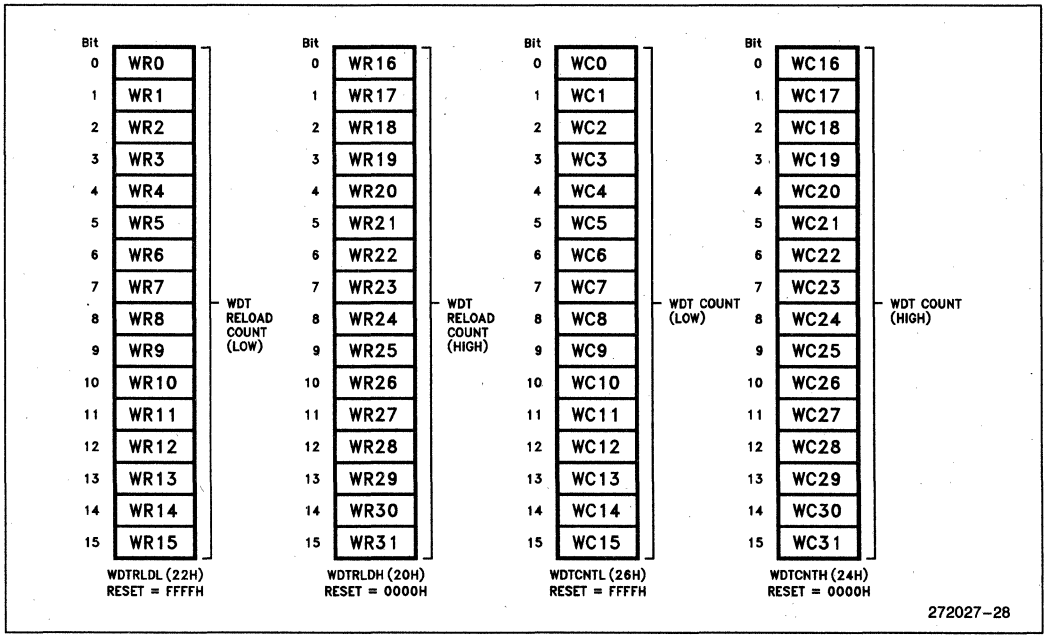

Figure 28. Watchdog Timer Registers

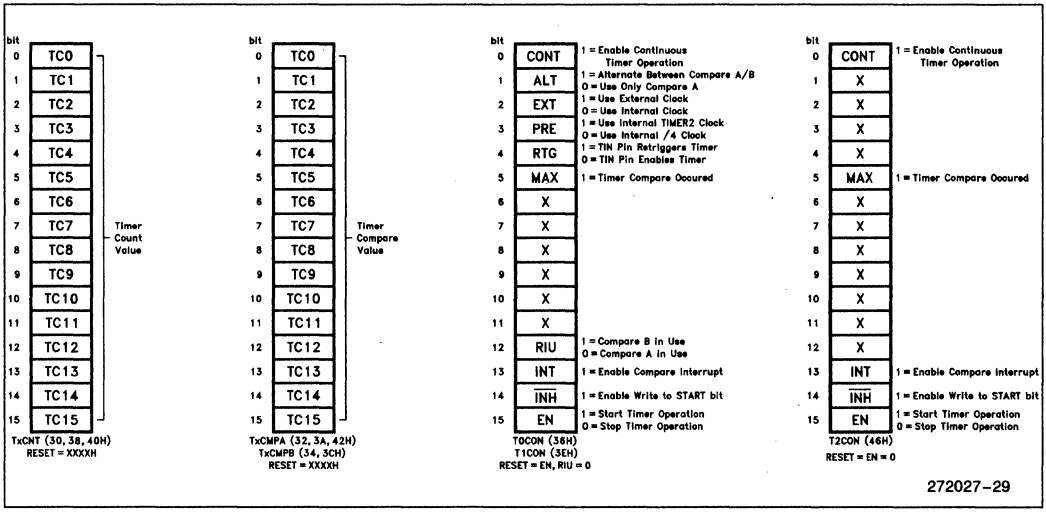

Figure 29. Timer Control Unit Registers

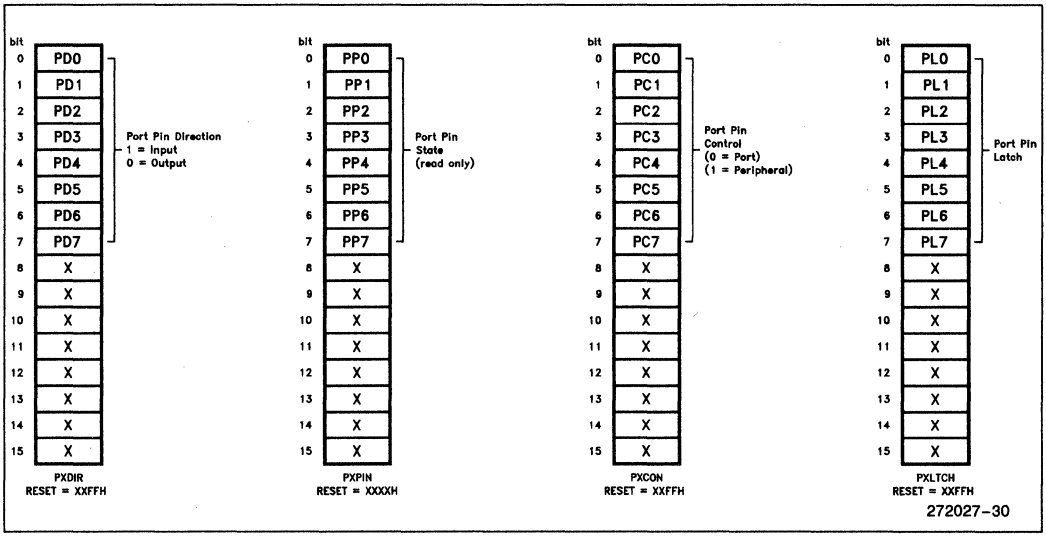

Figure 30. I/O Port Unit Registers

24

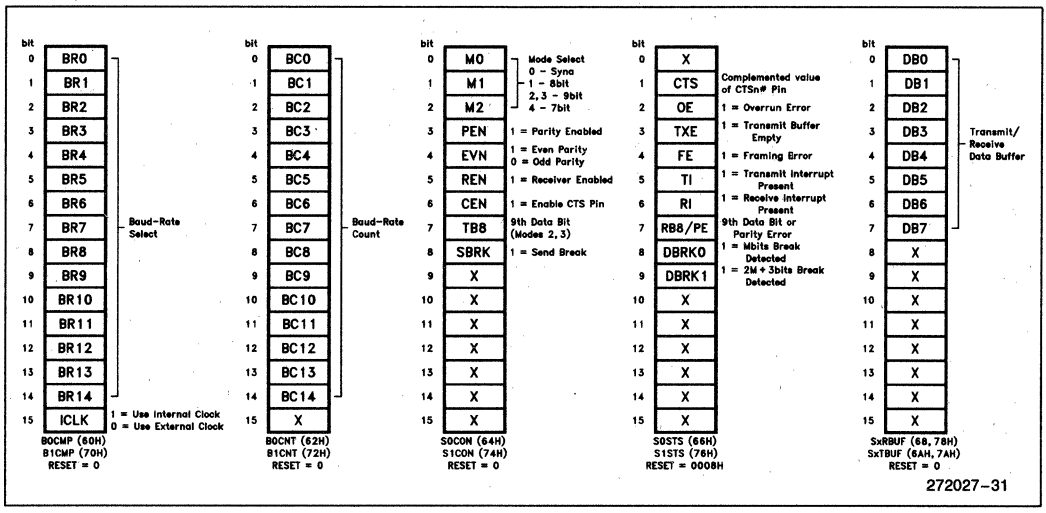

Figure 31. Serial Communications Unit Registers

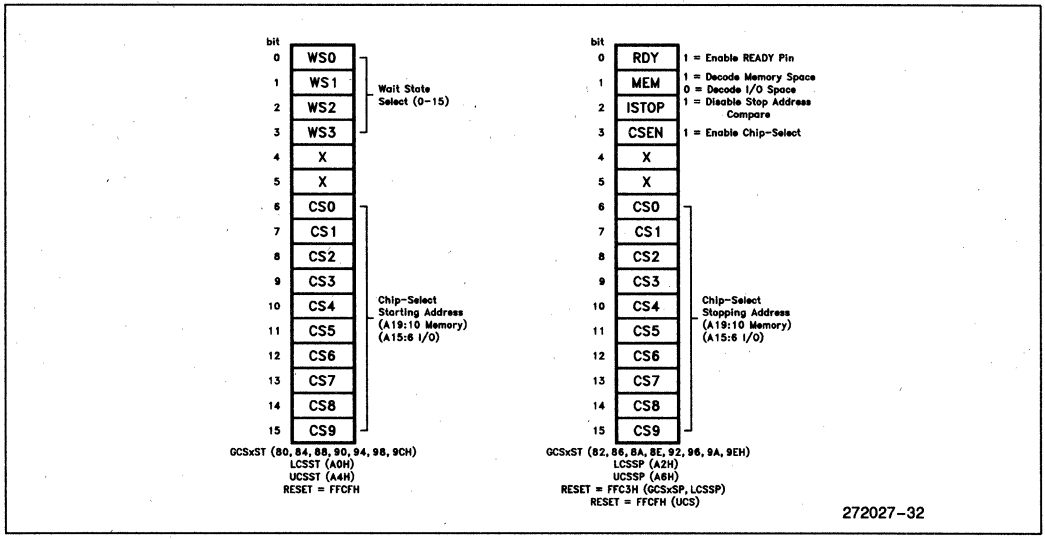

Figure 32. Chip-Select Unit Registers

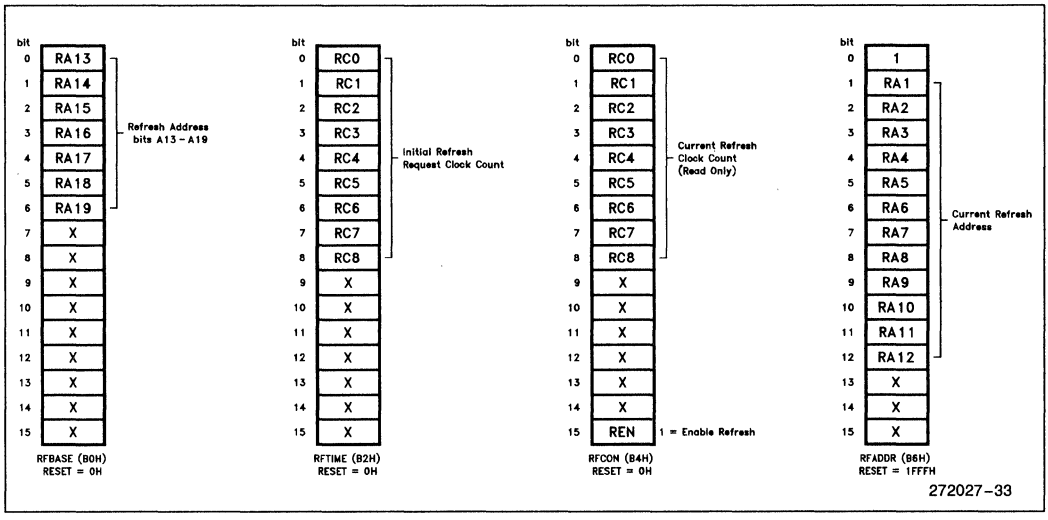

Figure 33. Refresh Control Unit Registers

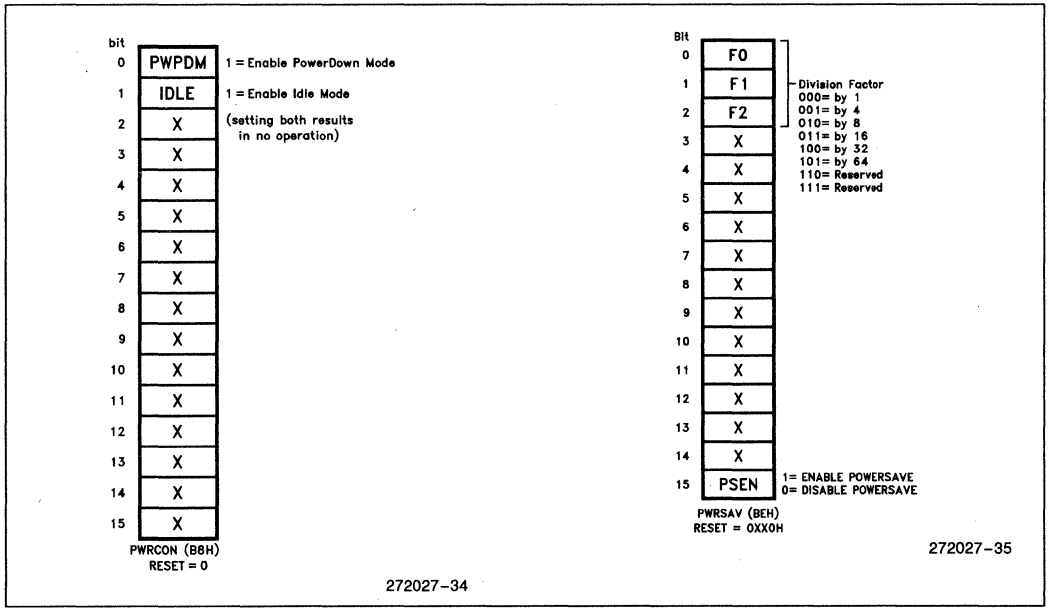

Figure 34. Power Management Unit Registers

24

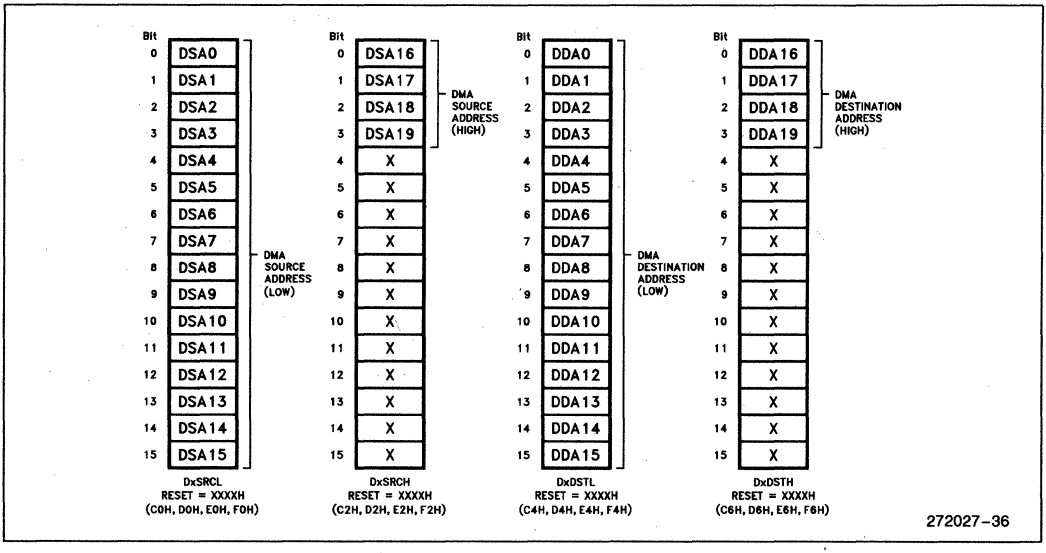

Figure 35. DMA Unit Registers

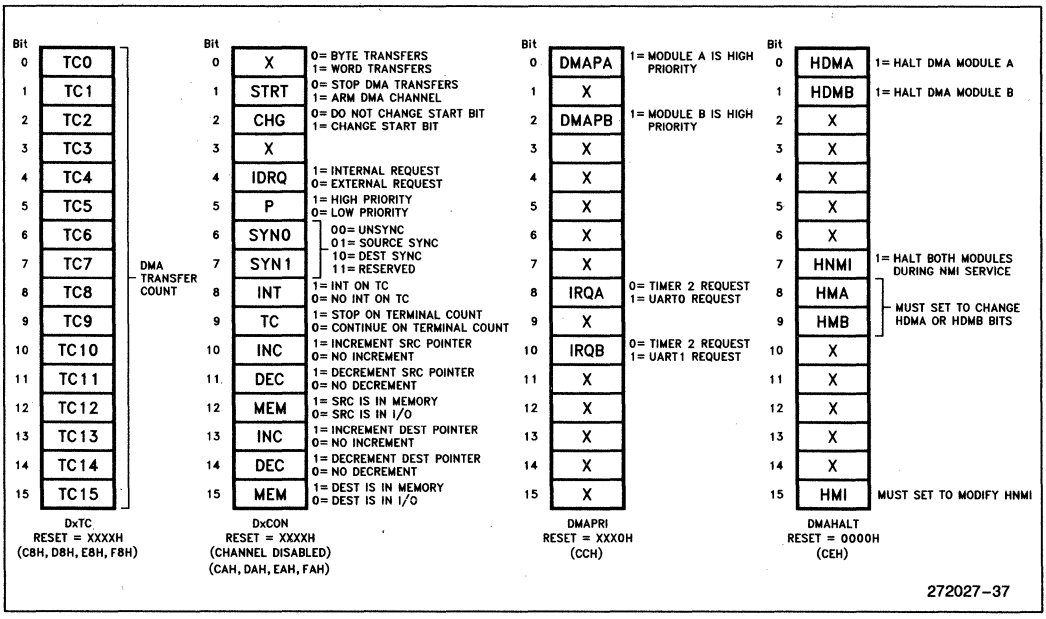

Figure 36. DMA Unit Registers (Continued)

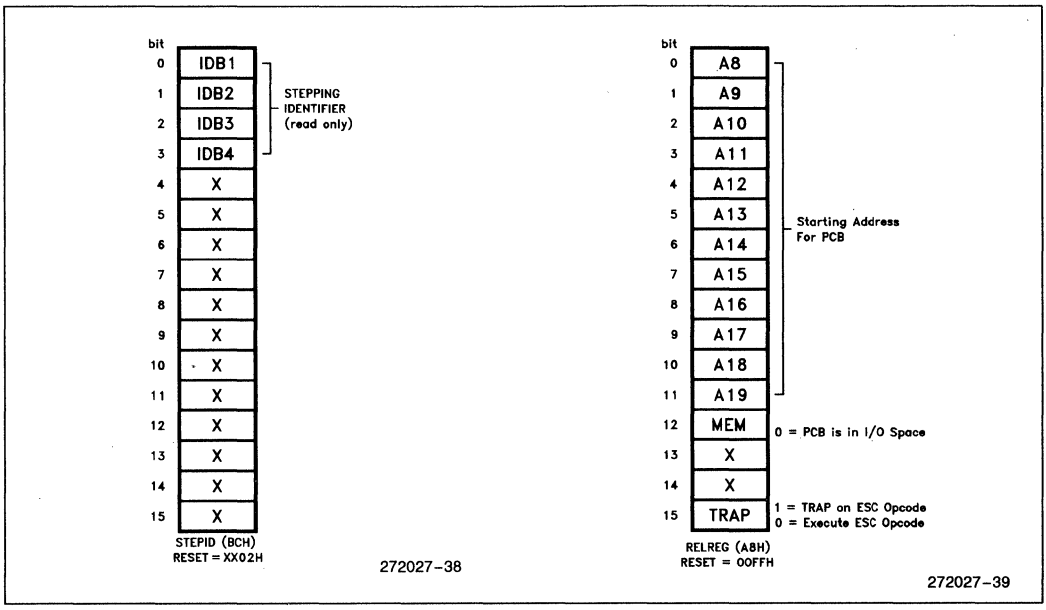

Figure 37. Relocation and Stepping Identifier Registers

80C186EC EXECUTION TIMINGS

A determination of 80C186EC program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the **minimum** execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the 80C186EC has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

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INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1000100w	mod reg r/m			2/12	
Register/memory to register	1000101w	mod reg r/m			2/9	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12–13	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3–4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8	
Accumulator to memory	1010001w	addr-low	addr-high		9	
Register/memory to segment register	10001110	mod 0 reg r/m			2/9	
Segment register to register/memory	10001100	mod 0 reg r/m			2/11	
PUSH = Push:						
Memory	11111111	mod 1 1 0 r/m			16	
Register	01010 reg				10	
Segment register	000reg110				9	
Immediate	011010s0	data	data if s=0		10	
PUSHA = Push All	01100000				36	
POP = Pop:						
Memory	10001111	mod 0 0 0 r/m			20	
Register	01011 reg				10	
Segment register	000reg111	(reg≠01)			8	
POPA = Pop All	01100001				51	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10	
Variable port	1110110w				8	
OUT = Output to:						
Fixed port	1110011w	port			9	
Variable port	1110111w				7	
XLAT = Translate byte to AL	11010111				11	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		18	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		18	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				9	
POPF = Pop flags	10011101				8	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10	
Register with register/memory	0011100w	mod reg r/m			3/10	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26–28	
Register-Word					35–37	
Memory-Byte					32–34	
Memory-Word					41–43	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
ARITHMETIC (Continued)						
IMUL = Integer multiply (signed):	1111011w	mod101 r/m				
Register-Byte					25–28	
Register-Word					34–37	
Memory-Byte					31–34	
Memory-Word					40–43	
IMUL = Integer Immediate multiply (signed)	011010s1	mod reg r/m	data	data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w	mod110 r/m				
Register-Byte					29	
Register-Word					38	
Memory-Byte					35	
Memory-Word					44	
IDIV = Integer divide (signed):	1111011w	mod111 r/m				
Register-Byte					44–52	
Register-Word					53–61	
Memory-Byte					50–58	
Memory-Word					59–67	
AAM = ASCII adjust for multiply	11010100	00001010			19	
AAD = ASCII adjust for divide	11010101	00001010			15	
CBW = Convert byte to word	10011000				2	
CWD = Convert word to double word	10011001				4	
LOGIC						
Shift/Rotate Instructions:						
Register/Memory by 1	1101000w	mod TTT r/m			2/15	
Register/Memory by CL	1101001w	mod TTT r/m			5+n/17+n	
Register/Memory by Count	1100000w	mod TTT r/m	count		5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR					
AND = **And:**						
Reg/memory and register to either	001000dw	mod reg r/m			3/10	
Immediate to register/memory	1000000w	mod100 r/m	data	data if w=1	4/16	
Immediate to accumulator	0010010w	data	data if w=1		3/4	8/16-bit
TEST = **And function to flags, no result:**						
Register/memory and register	1000010w	mod reg r/m			3/10	
Immediate data and register/memory	1111011w	mod000 r/m	data	data if w=1	4/10	
Immediate data and accumulator	1010100w	data	data if w=1		3/4	8/16-bit
OR = **Or:**						
Reg/memory and register to either	000010dw	mod reg r/m			3/10	
Immediate to register/memory	1000000w	mod001 r/m	data	data if w=1	4/16	
Immediate to accumulator	0000110w	data	data if w=1		3/4	8/16-bit

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
LOGIC (Continued)			
XOR = **Exclusive or:**			
Reg/memory and register to either	001100dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod 110 r/m | data | data if w=1	4/16	
Immediate to accumulator	0011010w | data | data if w=1	3/4	8/16-bit
NOT = Invert register/memory	1111011w | mod 010 r/m	3/10	
STRING MANIPULATION			
MOVS = Move byte/word	1010010w	14	
CMPS = Compare byte/word	1010011w	22	
SCAS = Scan byte/word	1010111w	15	
LODS = Load byte/wd to AL/AX	1010110w	12	
STOS = Store byte/wd from AL/AX	1010101w	10	
INS = Input byte/wd from DX port	0110110w	14	
OUTS = Output byte/wd to DX port	0110111w	14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)			
MOVS = Move string	11110010 | 1010010w	8+8n	
CMPS = Compare string	1111001z | 1010011w	5+22n	
SCAS = Scan string	1111001z | 1010111w	5+15n	
LODS = Load string	11110010 | 1010110w	6+11n	
STOS = Store string	11110010 | 1010101w	6+9n	
INS = Input string	11110010 | 0110110w	8+8n	
OUTS = Output string	11110010 | 0110111w	8+8n	
CONTROL TRANSFER			
CALL = **Call:**			
Direct within segment	11101000 | disp-low | disp-high	15	
Register/memory indirect within segment	11111111 | mod 010 r/m	13/19	
Direct intersegment	10011010 | segment offset | segment selector	23	
Indirect intersegment	11111111 | mod 011 r/m (mod ≠ 11)	38	
JMP = **Unconditional jump:**			
Short/long	11101011 | disp-low	14	
Direct within segment	11101001 | disp-low | disp-high	14	
Register/memory indirect within segment	11111111 | mod 100 r/m	11/17	
Direct intersegment	11101010 | segment offset | segment selector	14	
Indirect intersegment	11111111 | mod 101 r/m (mod ≠ 11)	26	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
RET = **Return from CALL:**						
Within segment	11000011				16	
Within seg adding immed to SP	11000010	data-low	data-high		18	
Intersegment	11001011				22	
Intersegment adding immediate to SP	11001010	data-low	data-high		25	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22+16(n−1)	
LEAVE = Leave Procedure	11001001				8	
INT = **Interrupt:**						
Type specified	11001101	type			47	
Type 3	11001100				45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110				48/4	
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33–35	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	
	(TTT LLL are opcode to processor extension)		

Shaded areas indicate instructions not available in 8086/8088 microsystems.

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

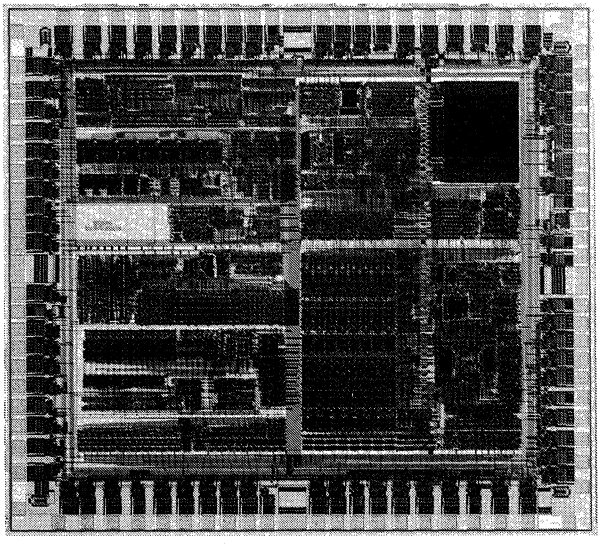
intel

80L186EA-13, -8
16-BIT HIGH INTEGRATION EMBEDDED PROCESSOR

- 3V Operation, V_{CC} = 2.7V–5.5V
- Full Static Operation
- True CMOS Inputs and Outputs

- Integrated Feature Set
  - Static 186 CPU Core
  - Power Save, Idle and Powerdown Modes
  - Clock Generator
  - 2 Independent DMA Channels
  - 3 Programmable 16-Bit Timers
  - Dynamic RAM Refresh Control Unit
  - Programmable Memory and Peripheral Chip Select Logic
  - Programmable Wait State Generator
  - Local Bus Controller
  - System-Level Testing Support (High Impedance Test Mode)
- Speed Versions Available:
  - 13 MHz (80L186EA-13)
  - 8 MHz (80L186EA-8)
- Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O
- Complete System Development Support
  - All 8086/8088 and 80C186 Family Software Development Tools Can Be Used for 80L186EA System Development
    - ASM86 Assembler, iC-86, Pascal-86, FORTRAN-86, PL/M-86 and System Utilities
    - In-Circuit-Emulator (ICE™-186)
- Available in the Following Packages:
  - 68-Pin Plastic Leaded Chip Carrier (PLCC)
  - 80-Pin EIAJ Quad Flat Pack (QFP)
- Available in EXPRESS Extended Temperature Range (−40°C to +85°C)

The 80L186EA is the 3V version of the 80C186EA Embedded Processor. By reducing V_{CC}, further power savings can be realized over the standard 80C186EA, making the 80L186EA ideal for battery-powered portable applications.



272021-1

June 1992
Order Number: 272021-002

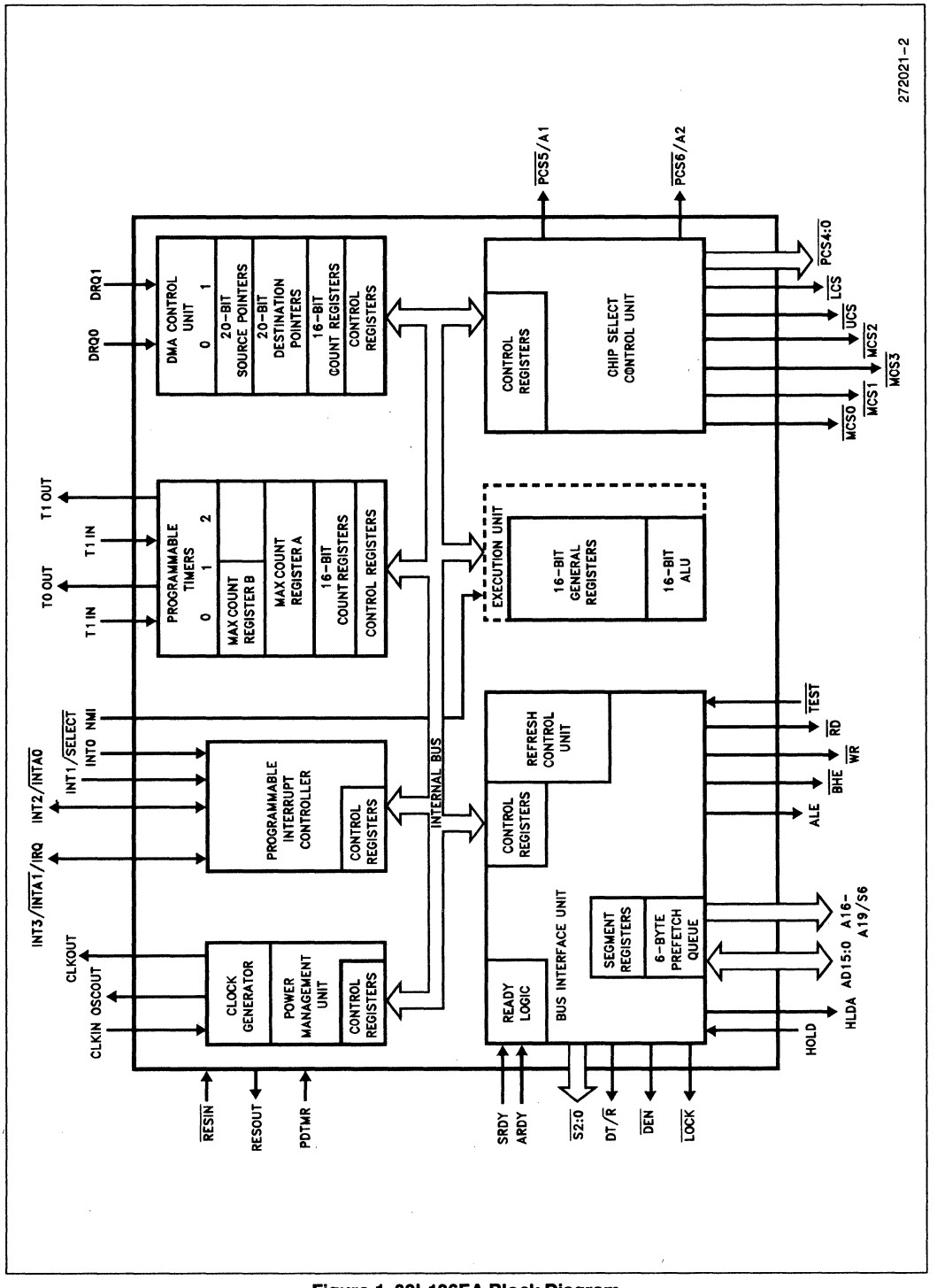


Figure 1. 80L186EA Block Diagram

INTRODUCTION

The 80L186EA is the second member of the 186 Integrated Processor Family to go to 3V operation, following the 80L186EB. The 80L186EA is the 3V version of the 80C186EA. The 80L186EA is functionally compatible with the industry standard 80C186 embedded processor. Current 80C186 users can easily upgrade their designs to use the 80L186EA and benefit from the reduced power consumption of 3V operation.

The feature set of the 80L186EA meets the needs of battery-powered applications. Battery-powered applications benefit from the static CPU core and peripherals. Minimum current consumption is achieved by combining low voltage operation along with the features of the power management unit, thus maximizing battery life. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space-critical applications benefit from the integration of commonly used system peripherals. Two flexible DMA channels perform CPU-independent data transfers. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 128 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters round out the feature set of the 80L186EA.

OVERVIEW

Figure 1 shows a block diagram of the 80L186EA. The Execution Unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instructions, and static operation. The Bus Interface Unit (BIU) is the same as that found on the original 80C186 family products. An independent internal bus is used to allow communication between the BIU and internal peripherals.

Differences between the 80C186 and the 80L186EA

The 80L186EA is intended as a direct functional upgrade for 80C186 designs. In many cases, it will be possible to replace an existing 80C186 with little or no hardware redesign. The following sections describe differences in pinout, operating modes, and AC and DC specifications to keep in mind.

Pinout Compatibility

The 80L186EA requires a PDTMR pin to time the processor's exit from Powerdown Mode. The original pin arrangement for the 80C186 in the PLCC package did not have any spare leads to use for PDTMR, so the DT/$\overline{R}$ pin was sacrificed. The arrangement of all the other leads in the 68-lead PLCC is identical between the 80C186 and the 80L186EA. DT/$\overline{R}$ may be readily synthesized by latching the $\overline{S1}$ status output. Therefore, upgrading a PLCC 80C186 to PLCC 80L186EA is particularly straightforward. You must connect a capacitor to the 80L186EA PDTMR pin in order to use Powerdown Mode.

The 80-lead QFP (EIAJ) pinouts are distinctly different between the 80C186 and the 80L186EA. In addition to the PDTMR pin, the 80L186EA has more power and ground pins and the overall arrangement of pins was shifted. A new circuit board layout for the 80L186EA is required.

Operating Modes

The 80C186 has two operating modes, Compatible and Enhanced. Compatible Mode is a pin-to-pin replacement for the NMOS 80186, except for numerics coprocessing. In Enhanced Mode, the processor has a Refresh Control Unit and the Power-Save feature.

In regular operation, all 80L186EA features (including those of the Enhanced Mode 80C186) are present.

PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the 80L186EA in the Plastic Leaded Chip Carrier (PLCC) package and Quad Flat Pack (QFP) package. For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

Pin Descriptions

Each pin or logical set of pins is described in Table 2. There are three columns for each entry in the Pin Description Table.

The **Pin Name** column contains a mnemonic that describes the pin function. Negation of the signal name (for example, $\overline{\text{RESIN}}$) denotes a signal that is active low.

The **Pin Type** column contains two kinds of information. The first symbol indicates whether a pin is power (P), ground (G), input only (I), output only (O) or input/output (I/O). Some pins have multiplexed functions (for example, A19/S6). Additional symbols indicate additional characteristics for each pin. Table 4 lists all the possible symbols for this column.

Input pins may be either synchronous or asynchronous. Asynchronous pins require that setup and hold times be met only in order to guarantee *recognition* at a particular clock edge. Synchronous pins require that setup and hold times be met to guarantee proper *operation.* For example, missing the setup or hold time for the SRDY pin (a synchronous input) will result in a system failure or lockup. Input pins may also be edge- or level-sensitive. The possible characteristics for input pins are S(E), S(L), A(E) and A(L).

Output states are dependent upon the current activity of the processor. There are four operational states that are different from regular operation: bus hold, reset, Idle Mode and Powerdown Mode. Appropriate characteristics for these states are also indicated in this column, with the legend for all possible characteristics in Table 1.

Finally, the **Pin Description** column contains a text description of each pin.

As an example, consider AD15:0. I/O signifies the pins are bidirectional. S(L) signifies that the input function is synchronous and level-sensitive. H(Z) signifies that, as outputs, the pins are high-impedance upon acknowledgement of bus hold. R(Z) signifies that the pins float during reset. P(X) signifies that the pins retain their states during Powerdown Mode.

Table 1. Pin Description Nomenclature

Symbol	Description
P	Power Pin (Apply + V_{CC} Voltage)
G	Ground (Connect to V_{SS})
I	Input Only Pin
O	Output Only Pin
I/O	Input/Output Pin
S(E)	Synchronous, Edge Sensitive
S(L)	Synchronous, Level Sensitive
A(E)	Asynchronous, Edge Sensitive
A(L)	Asynchronous, Level Sensitive
H(1)	Output Driven to V_{CC} during Bus Hold
H(0)	Output Driven to V_{SS} during Bus Hold
H(Z)	Output Floats during Bus Hold
H(Q)	Output Remains Active during Bus Hold
H(X)	Output Retains Current State during Bus Hold
R(WH)	Output Weakly Held at V_{CC} during Reset
R(1)	Output Driven to V_{CC} during Reset
R(0)	Output Driven to V_{SS} during Reset
R(Z)	Output Floats during Reset
R(Q)	Output Remains Active during Reset
R(X)	Output Retains Current State during Reset
I(1)	Output Driven to V_{CC} during Idle Mode
I(0)	Output Driven to V_{SS} during Idle Mode
I(Z)	Output Floats during Idle Mode
I(Q)	Output Remains Active during Idle Mode
I(X)	Output Retains Current State during Idle Mode
P(1)	Output Driven to V_{CC} during Powerdown Mode
P(0)	Output Driven to V_{SS} during Powerdown Mode
P(Z)	Output Floats during Powerdown Mode
P(Q)	Output Remains Active during Powerdown Mode
P(X)	Output Retains Current State during Powerdown Mode

Table 2. 80L186EA Pin Descriptions

Name	Type	Description
V_{CC}	P	**POWER** connections consist of six pins which must be shorted externally to a V_{CC} board plane.
V_{SS}	G	**GROUND** connections consist of five pins which must be shorted externally to a V_{SS} board plane.
CLKIN	I A(E)	**CLocK INput** is an input for an external clock. An external oscillator operating at two times the required 80L186EA operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O H(Q) R(Q) P(Q)	**OSCillator OUTput** is only used when using a crystal to generate the external clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin is not to be used as 2X clock output for non-crystal applications (i.e., this pin is N.C. for non-crystal applications). OSCOUT does not float in ONCE mode.
CLKOUT	O H(Q) R(Q) P(Q)	**CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transistions every falling edge of CLKIN.
$\overline{\text{RESIN}}$	I A(L)	**RESet IN** causes the 80L186EA to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the 80L186EA begins fetching opcodes at memory location 0FFFF0H.
RESOUT	O H(0) R(1) P(0)	**RESet OUTput** that indicates the 80L186EA is currently in the reset state. RESOUT will remain active as long as $\overline{\text{RESIN}}$ remains active.
PDTMR	I/O A(L) H(WH) R(Z) P(1)	**Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the 80L186EA waits after an exit from power down before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I A(E)	**Non-Maskable Interrupt** input causes a Type 2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{\text{TEST}}$	I A(E)	$\overline{\text{TEST}}$ is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (low).
AD15:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed **Address** and **Data** bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle.
A18:16 A19/S6	H(Z) R(Z) P(X)	These pins provide multiplexed **Address** during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. A18:16 are driven to a logic 0 during the data phase of the bus cycle. Also during the data phase, S6 is driven to a logic 0 to indicate a CPU-initiated bus cycle or logic 1 to indicate a DMA-initiated bus cycle or a refresh cycle.

Table 2. 80L186EA Pin Descriptions (Continued)

Name	Type	Description
$\overline{S2:0}$	O H(Z) R(Z) P(1)	Bus cycle **Status** are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ Bus Cycle Initiated 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive (no bus activity)
ALE/QS0	O H(0) R(0) P(0)	**Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle. In Queue Status Mode, QS0 provides queue status information along with QS1.
$\overline{BHE}$	O H(Z) R(Z) P(X)	**Byte High Enable** output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. $\overline{BHE}$ and A0 have the following logical encoding: A0 $\overline{BHE}$ Encoding 0 0 Word Transfer 0 1 Even Byte Transfer 1 0 Odd Byte Transfer 1 1 Refresh Operation
$\overline{RD}$/$\overline{QSMD}$	I/O H(Z) R(WH) P(1)	**ReaD** output signals that the accessed memory or I/O device must drive data information onto the data bus. Upon reset, this pin has an alternate function. As $\overline{QSMD}$, it enables **Queue Status Mode** when grounded. In Queue Status Mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide the following information about processor/instruction queue interaction: QS1 QS0 Queue Operation 0 0 No Queue Operation 0 1 First Opcode Byte Fetched from the Queue 1 1 Subsequent Byte Fetched from the Queue 1 0 Empty the Queue
$\overline{WR}$/QS1	O H(Z) R(Z) P(1)	**WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device. In Queue Status Mode, QS1 provides queue status information along with QS0.
ARDY	I A(L) S(L)	**Asychronous ReaDY** is an input to signal for the end of a bus cycle. ARDY is asynchronous on rising CLKOUT and synchronous on falling CLKOUT. ARDY or SRDY must be active to terminate any 80L186EA bus cycle, unless they are ignored due to correct programming of the Chip Select Unit.
SRDY	I S(L)	**Synchronous ReaDY** is an input to signal for the end of a bus cycle. ARDY or SRDY must be active to terminate any 80L186EA bus cycle, unless they are ignored due to correct programming of the Chip Select Unit.
$\overline{DEN}$	O H(Z) R(Z) P(1)	**Data ENable** output to control the enable of bidirectional transceivers when buffering an 80L186EA system. $\overline{DEN}$ is active only when data is to be transferred on the bus.

Table 2. 80L186EA Pin Descriptions (Continued)

Name	Type	Description
DT/$\overline{R}$	O H(Z) R(Z) P(X)	**Data Transmit/Receive** output controls the direction of a bi-directional buffer when buffering an 80L186EA system. DT/$\overline{R}$ is only available for the QFP (EIAJ) package (S80L186EA).
$\overline{LOCK}$	I/O H(Z) R(WH) P(1)	**LOCK** output indicates that the bus cycle in progress is not to be interrupted. The 80L186EA will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low.
HOLD	I A(L)	**HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The 80L186EA will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
HLDA	O H(1) R(0) P(0)	**HoLD Acknowledge** output to indicate that the 80L186EA has relinquish control of the local bus. When HLDA is asserted, the 80L186EA will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly.
$\overline{UCS}$	O H(1) R(1) P(1)	**Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH. During a processor reset, $\overline{UCS}$ and $\overline{LCS}$ are used to enable ONCE Mode.
$\overline{LCS}$	O H(1) R(1) P(1)	**Lower Chip Select** will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. $\overline{LCS}$ is inactive after a reset. During a processor reset, $\overline{UCS}$ and $\overline{LCS}$ are used to enable ONCE Mode.
$\overline{MCS0}$ $\overline{MCS1}$ $\overline{MCS2}$ $\overline{MCS3}$	O H(1) R(1) P(1) A(L)	If enabled, these pins comprise a block of **Mid-Range Chip Select** outputs which will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user.
$\overline{PCS4:0}$	O H(1) R(1) P(1)	**Peripheral Chip Selects** go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user.
$\overline{PCS5}$/A1 $\overline{PCS6}$/A2	0 H(1)/H(X) R(1) P(1)	These pins provide a multiplexed function. As additional **Peripheral Chip Selects,** they go active whenever the address of a memory or I/O bus cycle is within the address limitations by the user. They may also be programmed to provide latched **Address** A2:1 signals.
T0OUT T1OUT	O H(Q) R(1) P(Q)	**Timer OUTput** pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.
T0IN T1IN	I A(L) A(E)	**Timer INput** is used either as clock or control signals, depending on the timer mode selected.

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Table 2. 80L186EA Pin Descriptions (Continued)

Name	Type	Description
DRQ0 DRQ1	I A(L)	**DMA ReQuest** is asserted by an external request when it is prepared for a DMA transfer.
INT0 INT1/$\overline{\text{SELECT}}$	I A(E,L)	Maskable **INTerrupt** input will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with $\overline{\text{INTA0}}$ and $\overline{\text{INTA1}}$ to interface with an external slave controller. INT1 becomes $\overline{\text{SELECT}}$ when the ICU is configured for Slave Mode.
INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$/IRQ	I/O A(E,L) /H(1) R(Z) /P(1)	These pins provide multiplexed functions. As inputs, they provide a maskable **INTerrupt** that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an **INTerrupt Acknowledge** handshake signal to allow interrupt expansion. INT3/$\overline{\text{INTA1}}$ becomes **IRQ** when the ICU is configured for Slave Mode.
N.C.	—	**No Connect.** For compatibility with future products, do not connect to these pins.

80L186EA PINOUT

Tables 3 and 4 list the 80L186EA pin names with package location for the 68-pin Plastic Leaded Chip Carrier (PLCC) component. Figure 2 depicts the complete 80L186EA pinout (PLCC package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 5 and 6 list the 80L186EA pin names with package location for the 80-pin Quad Flat Pack (EIAJ) component. Figure 2 depicts the complete 80L186EA (EIAJ QFP package) as viewed from the top side of the component (i.e., contacts facing down).

Table 3. PLCC Pin Names with Package Location

Address/Data Bus	
Name	**Location**
AD0	17
AD1	15
AD2	13
AD3	11
AD4	8
AD5	6
AD6	4
AD7	2
AD8	16
AD9	14
AD10	12
AD11	10
AD12	7
AD13	5
AD14	3
AD15	1
A16	68
A17	67
A18	66
A19/S6	65

Bus Control	
Name	**Location**
ALE/QS0	61
$\overline{\text{BHE}}$	64
$\overline{\text{S0}}$	52
$\overline{\text{S1}}$	53
$\overline{\text{S2}}$	54
$\overline{\text{RD}}$/QSMD	62
$\overline{\text{WR}}$/QS1	63
ARDY	55
SRDY	49
$\overline{\text{DEN}}$	39
$\overline{\text{LOCK}}$	48
HOLD	50
HLDA	51

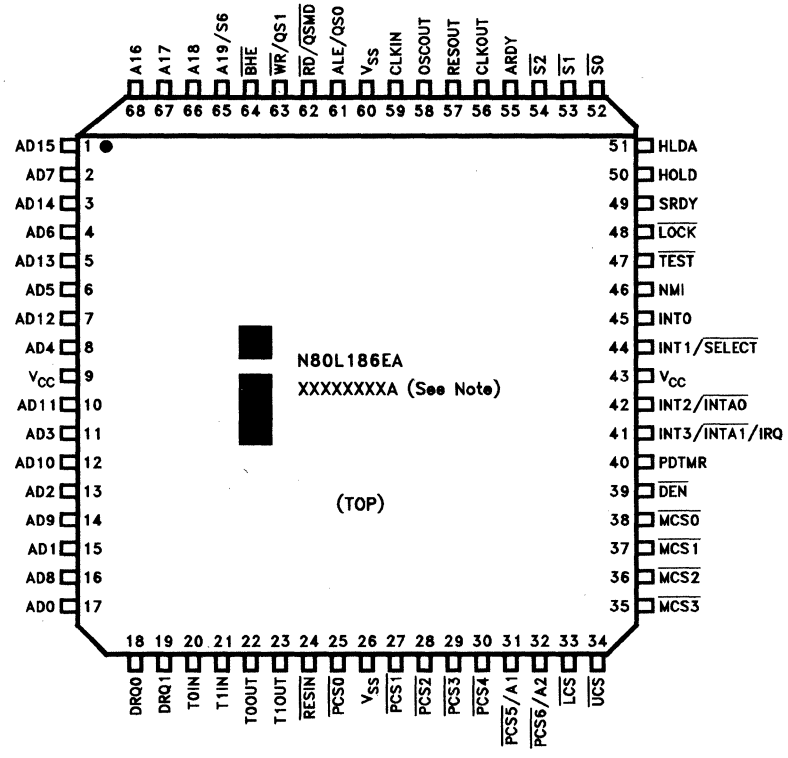
Power	
Name	**Location**
V_{SS}	26, 60
V_{CC}	9, 43

Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	24
RESOUT	57
CLKIN	59
OSCOUT	58
CLKOUT	56
$\overline{\text{TEST}}$	47
PDTMR	40
NMI	46
INT0	45
INT1/SELECT	44
INT2/$\overline{\text{INTA0}}$	42
INT3/$\overline{\text{INTA1}}$/IRQ	41

I/O	
Name	**Location**
$\overline{\text{UCS}}$	34
$\overline{\text{LCS}}$	33
$\overline{\text{MCS0}}$	38
$\overline{\text{MCS1}}$	37
$\overline{\text{MCS2}}$	36
$\overline{\text{MCS3}}$	35
$\overline{\text{PCS0}}$	25
$\overline{\text{PCS1}}$	27
$\overline{\text{PCS2}}$	28
$\overline{\text{PCS3}}$	29
$\overline{\text{PCS4}}$	30
$\overline{\text{PCS5}}$/A1	31
$\overline{\text{PCS6}}$/A2	32
T0OUT	22
T0IN	20
T1OUT	23
T1IN	21
DRQ0	18
DRQ1	19

Table 4. PLCC Package Locations with Pin Name

Location	Name	Location	Name	Location	Name	Location	Name
1	AD15	18	DRQ0	35	$\overline{MCS3}$	52	$\overline{S0}$
2	AD7	19	DRQ1	36	$\overline{MCS2}$	53	$\overline{S1}$
3	AD14	20	T0IN	37	$\overline{MCS1}$	54	$\overline{S2}$
4	AD6	21	T1IN	38	$\overline{MCS0}$	55	ARDY
5	AD13	22	T0OUT	39	$\overline{DEN}$	56	CLKOUT
6	AD5	23	T1OUT	40	PDTMR	57	RESOUT
7	AD12	24	$\overline{RESIN}$	41	INT3/$\overline{INTA1}$/	58	OSCOUT
8	AD4	25	$\overline{PCS0}$		IRQ	59	CLKIN
9	V_{CC}	26	V_{SS}	42	INT2/$\overline{INTA0}$	60	V_{SS}
10	AD11	27	$\overline{PCS1}$	43	V_{CC}	61	ALE/QS0
11	AD3	28	$\overline{PCS2}$	44	INT1/SELECT	62	$\overline{RD}$/$\overline{QSMD}$
12	AD10	29	$\overline{PCS3}$	45	INT0	63	$\overline{WR}$/QS1
13	AD2	30	$\overline{PCS4}$	46	NMI	64	$\overline{BHE}$
14	AD9	31	$\overline{PCS5}$/A1	47	$\overline{TEST}$	65	A19/S6
15	AD1	32	$\overline{PCS6}$/A2	48	LOCK	66	A18
16	AD8	33	$\overline{LCS}$	49	SRDY	67	A17
17	AD0	34	$\overline{UCS}$	50	HOLD	68	A16
				51	HLDA		



NOTE:
The nine-character alphanumeric code (XXXXXXXXA) underneath the product number is the Intel FPO number.

Figure 2. 68-Lead PLCC Pinout Diagram

Table 5. QFP (EIAJ) Pin Name with Package Location

Address/Data Bus	
Name	**Location**
AD0	64
AD1	66
AD2	68
AD3	70
AD4	74
AD5	76
AD6	78
AD7	80
AD8	65
AD9	67
AD10	69
AD11	71
AD12	75
AD13	77
AD14	79
AD15	1
A16	3
A17	4
A18	5
A19/S6	6

Bus Control	
Name	**Location**
ALE/QS0	10
$\overline{BHE}$	7
$\overline{S0}$	23
$\overline{S1}$	22
$\overline{S2}$	21
$\overline{RD}/\overline{QSMD}$	9
$\overline{WR}$/QS1	8
ARDY	20
SRDY	27
DT/$\overline{R}$	37
$\overline{DEN}$	39
$\overline{LOCK}$	28
HOLD	26
HLDA	25

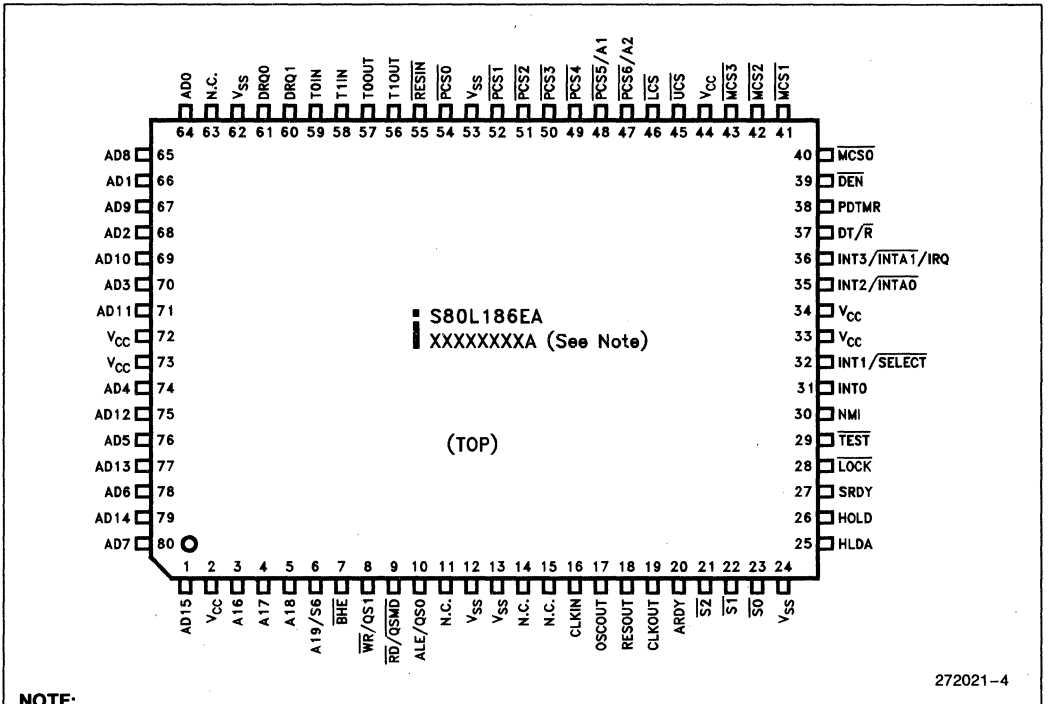
Power	
Name	**Location**
V_{SS}	12, 13, 24, 53, 62
V_{CC}	2, 33, 34, 44, 72, 73

Processor Control	
Name	**Location**
$\overline{RESIN}$	55
RESOUT	18
CLKIN	16
OSCOUT	17
CLKOUT	19
$\overline{TEST}$	29
PDTMR	38
NMI	30
INT0	31
INT1/$\overline{SELECT}$	32
INT2/$\overline{INTA0}$	35
INT3/$\overline{INTA1}$/ IRQ	36
N.C.	11, 14, 15, 63

I/O	
Name	**Location**
$\overline{UCS}$	45
$\overline{LCS}$	46
$\overline{MCS0}$	40
$\overline{MCS1}$	41
$\overline{MCS2}$	42
$\overline{MCS3}$	43
$\overline{PCS0}$	54
$\overline{PCS1}$	52
$\overline{PCS2}$	51
$\overline{PCS3}$	50
$\overline{PCS4}$	49
$\overline{PCS5}$/A1	48
$\overline{PCS6}$/A2	47
T0OUT	57
T0IN	59
T1OUT	56
T1IN	58
DRQ0	61
DRQ1	60

Table 6. QFP (EIAJ) Package Location with Pin Names

Location	Name	Location	Name	Location	Name	Location	Name
1	AD15	21	$\overline{S2}$	41	$\overline{MCS1}$	61	DRQ0
2	V_{CC}	22	$\overline{S1}$	42	$\overline{MCS2}$	62	V_{SS}
3	A16	23	$\overline{S0}$	43	$\overline{MCS3}$	63	N.C.
4	A17	24	V_{SS}	44	V_{CC}	64	AD0
5	A18	25	HLDA	45	$\overline{UCS}$	65	AD8
6	A19/S6	26	HOLD	46	$\overline{LCS}$	66	AD1
7	$\overline{BHE}$	27	SRDY	47	$\overline{PCS6}$/A2	67	AD9
8	$\overline{WR}$/QS1	28	$\overline{LOCK}$	48	$\overline{PCS5}$/A1	68	AD2
9	$\overline{RD}/\overline{QSMD}$	29	$\overline{TEST}$	49	$\overline{PCS4}$	69	AD10
10	ALE/QS0	30	NMI	50	$\overline{PCS3}$	70	AD3
11	N.C.	31	INT0	51	$\overline{PCS2}$	71	AD11
12	V_{SS}	32	INT1/$\overline{SELECT}$	52	$\overline{PCS1}$	72	V_{CC}
13	V_{SS}	33	V_{CC}	53	V_{SS}	73	V_{CC}
14	N.C.	34	V_{CC}	54	$\overline{PCS0}$	74	AD4
15	N.C.	35	INT2/$\overline{INTA0}$	55	$\overline{RESIN}$	75	AD12
16	CLKIN	36	INT3/$\overline{INTA1}$/	56	T1OUT	76	AD5
17	OSCOUT		IRQ	57	T0OUT	77	AD13
18	RESOUT	37	DT/$\overline{R}$	58	T1IN	78	AD6
19	CLKOUT	38	PDTMR	59	T0IN	79	AD14
20	ARDY	39	$\overline{DEN}$	60	DRQ1	80	AD7
		40	$\overline{MCS0}$				



NOTE:
The nine-character alphanumeric code (XXXXXXXXA) underneath the product number is the Intel FPO number.

Figure 3. Quad Flat Pack (EIAJ) Pinout Diagram

PACKAGE THERMAL SPECIFICATIONS

The 80L186EA is specified for operation when T_C (the case temperature) is within the range of 0°C to 85°C (PLCC package) or 0°C to 106°C (QFP-EIAJ) package. T_C may be measured in any environment to determine whether the 80L186EA is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P \times \theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 7 for the 68-pin Plastic Leaded Chip Carrier (PLCC) package.

Table 8 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies. P (the maximum power consumption, specified in watts) is calculated by using the maximum ICC as tabulated in the DC specifications and V_{CC} of 5V.

Table 7. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow Linear ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PLCC)	29	25	21	19	17	16.5
θ_{CA} (QFP)	66	63	60.5	59	58	57

Table 8. Maximum T_A at Various Airflows (in °C)

		Airflow Linear ft/min (m/sec)					
	T_F (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A (PLCC)	25	78	80	81	82	82.5	83
	32	74	76	78	79	79.5	80
	40	70	72	74	75	76	76.5
T_A (QFP)	25	84	85.5	86	87	87	87.5
	32	77.5	79	80	80.5	81	81.5
	40	70	71.5	73	74	74	75

ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +150°C

Case Temperature under Bias ... −65°C to +150°C

Supply Voltage with Respect to V_{SS} ..... −0.5V to +6.5V

Voltage on Other Pins with Respect to V_{SS} ..... −0.5V to V_{CC} + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	5.5	V
T_F	Input Clock Frequency			
	80L186EA13	0	26	MHz
	80L186EA8	0	16	MHz
T_C	Case Temperature under Bias			
	N80L186EA (PLCC)	0	+100	°C
	S80L186EA (QFP)	0	+114	°C

RECOMMENDED CONNECTIONS

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80L186EA based circuit board should contain separate power (V_{CC}) and ground (V_{SS}) planes. All V_{CC} and V_{SS} pins **must** be connected to the appropriate plane. Pins identified as "N.C." must not be connected in the system. Decoupling capacitors should be placed near the 80L186EA. The value and type of decoupling capacitors is application and board layout dependent. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Always connect any unused input pins to an appropriate signal level. In particular, unused interrupt pins (NMI, INT3:0) should be connected to V_{SS} to avoid unwanted interrupts. **Leave any unused output pin or any "N.C." pin unconnected.**

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage	−0.5	0.3*V_{CC}	V	
V_{IH}	Input High Voltage	0.7*V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6 mA (Min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −1 mA (Min)
V_{HYR}	Input Hysterisis on RESIN	0.30		V	
I_{LI1}	Input Leakage Current (except $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{LOCK}$ and $\overline{TEST}$)		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{IL2}	Input Leakage Current ($\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{LOCK}$ and $\overline{TEST}$)	−275		μA	V_{IN} = 0.7 V_{CC} (Note 1)
I_{OL}	Output Leakage Current		±10	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 2)
I_{CC5}	Supply Current (RESET, 5.5V) 80L186EA-13 80L186EA-8		 40	 mA mA	 (Note 3) (Note 3)
I_{CC3}	Supply Current (RESET, 2.7V) 80L186EA-13 80L186EA-8		 20	 mA mA	 (Note 3) (Note 3)
I_{ID5}	Supply Current Idle (5.5V) 80L186EA-13 80L186EA-8		 28	 mA mA	
I_{ID3}	Supply Current Idle (2.7V) 80L186EA-13 80L186EA-8		 14	 mA mA	
I_{PD5}	Supply Current Powerdown (5.5V) 80L186EA-13 80L186EA-8		 100 100	 μA μA	
I_{PD3}	Supply Current Powerdown (2.7V) 80L186EA-13 80L186EA-8		 50 50	 μA μA	
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 4)
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz

NOTES:
1. $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{LOCK}$ and $\overline{TEST}$ have internal pullups that are only activated during RESET. Loading these pins above I_{OL} = −275 μA will cause the 80L186EA to enter alternate modes of operation.
2. Output pins are floated using HOLD or ONCE Mode.
3. Measured at worst case temperature and V_{CC} with all outputs loaded as specified in the AC Test Conditions, and with the device in RESET ($\overline{RESIN}$ held low).
4. Output capacitance is the capacitive load of a floating output pin.

I_{CC} VERSUS FREQUENCY AND VOLTAGE

The current (I_{CC}) consumption of the 80L186EA is essentially composed of two components; I_{PD} and I_{CCS}.

I_{PD} is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or V_{CC} (no clock applied to the device). I_{PD} is equal to the Powerdown current and is typically less than 50 μA.

I_{CCS} is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since I_{CCS} is typically much greater than I_{PD}, I_{PD} can often be ignored when calculating I_{CC}.

I_{CCS} is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: V = Device operating voltage (V_{CC})

C_{DEV} = Device capacitance

f = Device operating frequency

I_{CCS} = I_{CC} = Device current

Measuring C_{DEV} on a device like the 80L186EA would be difficult. Instead, C_{DEV} is calculated using the above formula by measuring I_{CC} at a known V_{CC} and frequency (see Table 9). Using this C_{DEV} value, I_{CC} can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical I_{CC} when operating at 20 MHz, 4.8V.

$$I_{CC} = I_{CCS} = 4.8 \times 0.515 \times 20 \approx 49 \text{ mA}$$

PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: t = desired delay in **seconds**

C_{PD} = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132$ μF is required. Round up to standard (available) capacitive values.

NOTE:
The above equation applies to delay times greater than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperature will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

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Table 9. C_{DEV} Values

Parameter	Typ	Max	Units	Notes
C_{DEV} (Device in Reset)	0.515	0.905	mA/V*MHz	1, 2
C_{DEV} (Device in Idle)	0.391	0.635	mA/V*MHz	1, 2

1. Max C_{DEV} is calculated at −40°C, all floating outputs driven to V_{CC} or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical C_{DEV} is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

AC SPECIFICATIONS

AC Characteristics—80L186EA13

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	2C	MHz	1
T_C	CLKIN Period	38.5	∞	ns	1
T_{CH}	CLKIN High Time	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	45	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	15	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	15	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{LOCK}$	3	27	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{RD}$, $\overline{WR}$	3	32	ns	1, 4, 6, 8
T_{CHOV3}	$\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, A19:16	3	30	ns	1, 4, 6, 11
T_{CLOV1}	$\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT	3	27	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{INTA1:0}$	3	32	ns	1, 4, 6
T_{CLOV3}	$\overline{BHE}$, $\overline{DEN}$, A19:16	3	30	ns	1, 4, 6
T_{CLOV4}	AD15:0	3	34	ns	1, 4, 6
T_{CLOV5}	$\overline{S2:0}$	3	38	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	35	ns	1

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 9 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 10 for rise and fall times outside 50 pF.
6. See Figure 10 for rise and fall times.
7. T_{CHOV1} applies to $\overline{LOCK}$ and only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L186EA operation (SRDY, AD15:0).
11. T_{CHOV3} applies to $\overline{BHE}$ and A19:16 only after a HOLD release.

AC SPECIFICATIONS (Continued)

AC Characteristics—80L186EA13 (Continued)

Symbol	Parameter	Min	Max	Units	Notes
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	25		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		ns	1, 9
T_{CLIS}	AD15:0, ARDY, SRDY, DRQ1:0	25		ns	1, 10
T_{CLIH}	AD15:0, ARDY, SRDY, DRQ1:0	3		ns	1, 10
T_{CLIS}	HOLD	25		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	25		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (from CLKIN)	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 9 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 10 for rise and fall times outside 50 pF.
6. See Figure 10 for rise and fall times.
7. T_{CHOV1} applies to $\overline{LOCK}$ and only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L186EA operation (SRDY, AD15:0).
11. T_{CHOV3} applies to $\overline{BHE}$ and A19:16 only after a HOLD release.

AC SPECIFICATIONS (Continued)

AC Characteristics—80L186EA8

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	2C	MHz	1
T_C	CLKIN Period	38.5	∞	ns	1
T_{CH}	CLKIN High Time	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	95	ns	1, 4
T	CLKOUT Period		2*T_C	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	15	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	15	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{LOCK}$	3	27	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{RD}$, $\overline{WR}$	3	32	ns	1, 4, 6, 8
T_{CHOV3}	$\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, A19:16	3	30	ns	1, 4, 6, 11
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	27	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{INTA1:0}$	3	35	ns	1, 4, 6
T_{CLOV3}	$\overline{BHE}$, $\overline{DEN}$, A19:16	3	30	ns	1, 4, 6
T_{CLOV4}	AD15:0	3	35	ns	1, 4, 6
T_{CLOV5}	$\overline{S2:0}$	3	40	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	35	ns	1

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 9 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 10 for rise and fall times outside 50 pF.
6. See Figure 10 for rise and fall times.
7. T_{CHOV1} applies to $\overline{LOCK}$ and only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L186EA operation (SRDY, AD15:0).
11. T_{CHOV3} applies to $\overline{BHE}$ and A19:16 only after a HOLD release.

AC SPECIFICATIONS (Continued)

AC Characteristics—80L186EA8 (Continued)

Symbol	Parameter	Min	Max	Units	Notes
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	25		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		ns	1, 9
T_{CLIS}	AD15:0, ARDY, SRDY, DRQ1:0	25		ns	1, 10
T_{CLIH}	AD15:0, ARDY, SRDY, DRQ1:0	3		ns	1, 10
T_{CLIS}	HOLD	25		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	25		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (from CLKIN)	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 9 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 10 for rise and fall times outside 50 pF.
6. See Figure 10 for rise and fall times.
7. T_{CHOV1} applies to $\overline{LOCK}$ and only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L186EA operation (SRDY, AD15:0).
11. T_{CHOV3} applies to $\overline{BHE}$ and A19:16 only after a HOLD release.

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AC SPECIFICATIONS (Continued)

Relative Timings—80L188EA-13,-8

Symbol	Parameter	Min	Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Rising to ALE Falling	T − 15		ns	
T_{AVLL}	Address Valid to ALE Falling	½T − 10		ns	
T_{PLLL}	Chip Selects Valid to ALE Falling	½T − 10		ns	1
T_{LLAX}	Address Hold from ALE Falling	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{RHLH}	$\overline{RD}$ Rising to ALE Rising	½T − 10		ns	1
T_{WHLH}	$\overline{WR}$ Rising to ALE Rising	½T − 10		ns	1
T_{AFRL}	Address Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Falling to $\overline{RD}$ Rising	(2*T) − 5		ns	2
T_{WLWH}	$\overline{WR}$ Falling to $\overline{WR}$ Rising	(2*T) − 5		ns	2
T_{RHAV}	$\overline{RD}$ Rising to Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHDEX}	$\overline{WR}$ Rising to $\overline{DEN}$ Rising	½T − 10		ns	1
T_{WHPH}	$\overline{WR}$ Rising to Chip Select Rising	½T − 10		ns	1, 4
T_{RHPH}	$\overline{RD}$ Rising to Chip Select Rising	½T − 10		ns	1, 4
T_{PHPL}	$\overline{CS}$ Inactive to $\overline{CS}$ Active	½T − 10		ns	1
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		ns	5
T_{OVRH}	ONCE ($\overline{UCS}$, $\overline{LCS}$) Active to $\overline{RESIN}$ Rising	T		ns	3
T_{RHOX}	ONCE ($\overline{UCS}$, $\overline{LCS}$) to $\overline{RESIN}$ Rising	T		ns	3

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Not tested.
4. Not applicable to latched A2:1. These signals change only on falling T_1.
5. For write cycle followed by read cycle.

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 4. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

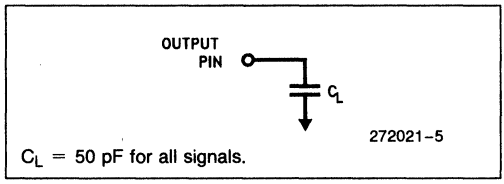

Figure 4. AC Test Load

AC TIMING WAVEFORMS

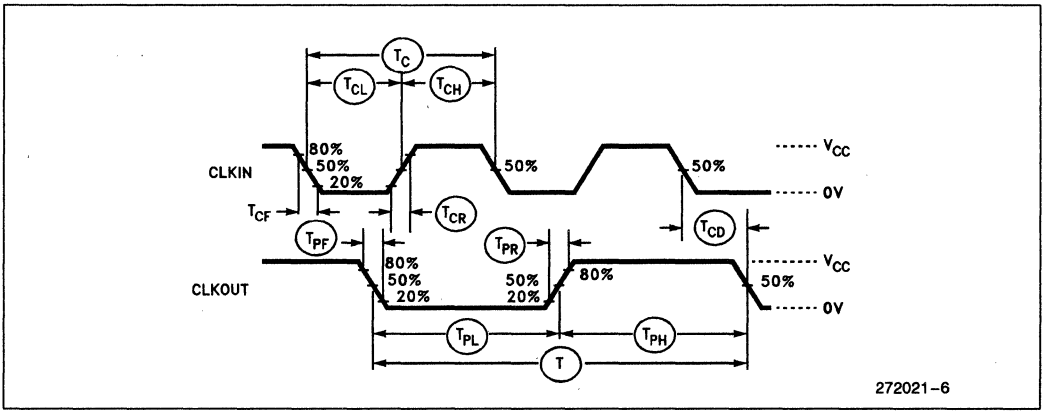

Figure 5. Input and Output Clock Waveform

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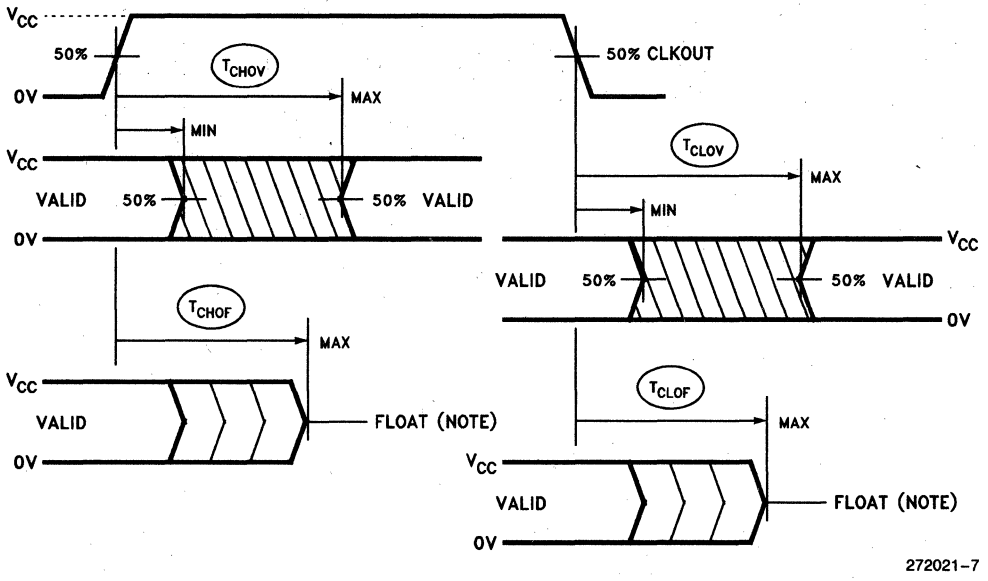
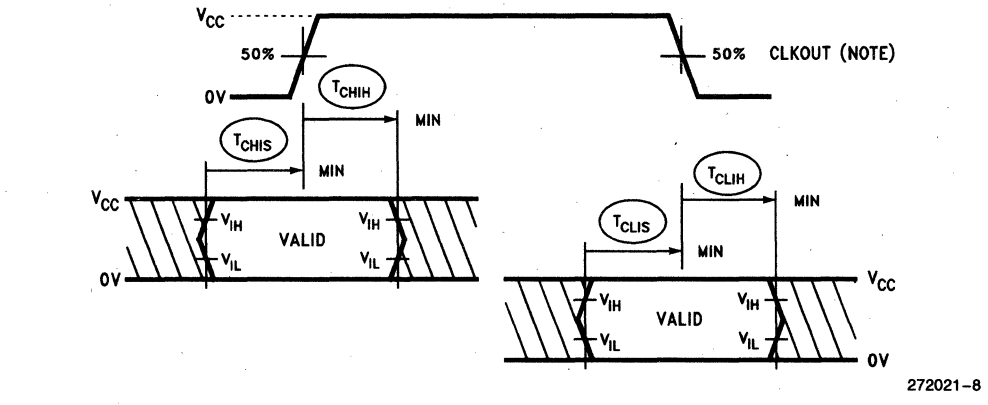


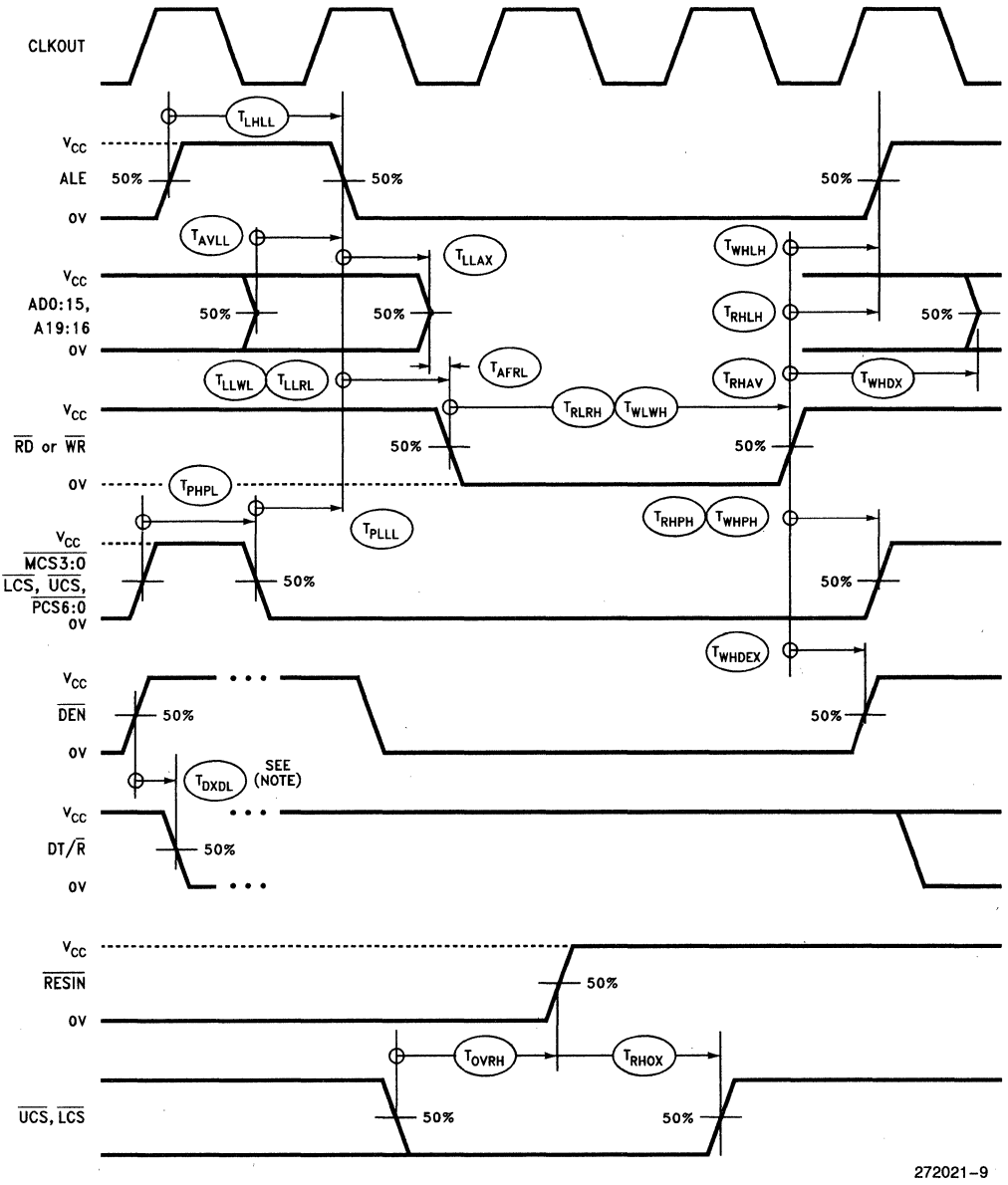
NOTE:
20% V_{CC} < Float < 80% V_{CC}

Figure 6. Output Delay and Float Waveform



NOTE:
$\overline{RESIN}$ measured to CLKIN, not CLKOUT

Figure 7. Input Setup and Hold



NOTE:
T_{DXDL} for write cycle followed by read cycle.

Figure 8. Relative Signal Waveform

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DERATING CURVES

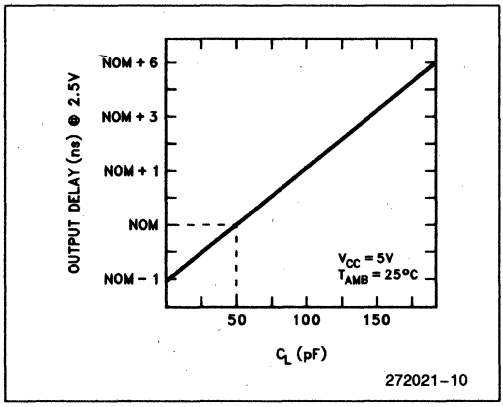


Figure 9. Typical Output Delay Variations Versus Load Capacitance

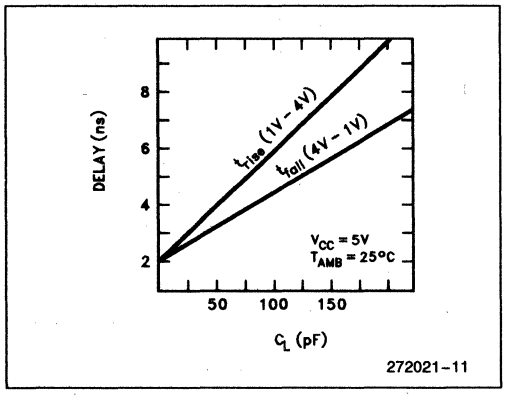


Figure 10. Typical Rise and Fall Variations Versus Load Capacitance

80L186EA EXPRESS

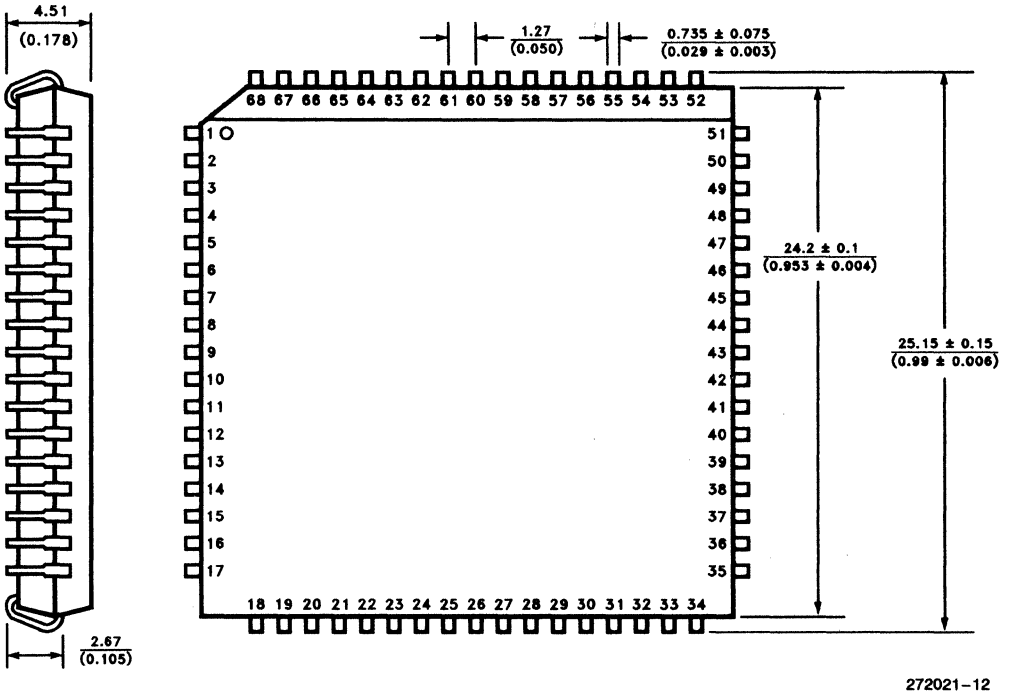
The Intel EXPRESS program offers an extended temperature range as an enhancement to the 80L186EA operational specifications. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the standard commercial temperature range, operational characteristics are guaranteed over a temperature range corresponding to 0°C to +70°C ambient. With the extended temperature range option, operational characteristics are guaranteed over a temperature range corresponding to −40°C to +85°C ambient.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 10. All AC and DC specifications are the same for both commercial and EXPRESS parts.

Table 10. Prefix Identification

Prefix	Package Type	Temperature Range
N	PLCC	Commercial
S	QFP (EIAJ)	Commercial
TN	PLCC	Extended
TS	QFP (EIAJ)	Extended



NOTE:
Units are mm/(inches).

Figure 11. PLCC Principal Dimensions

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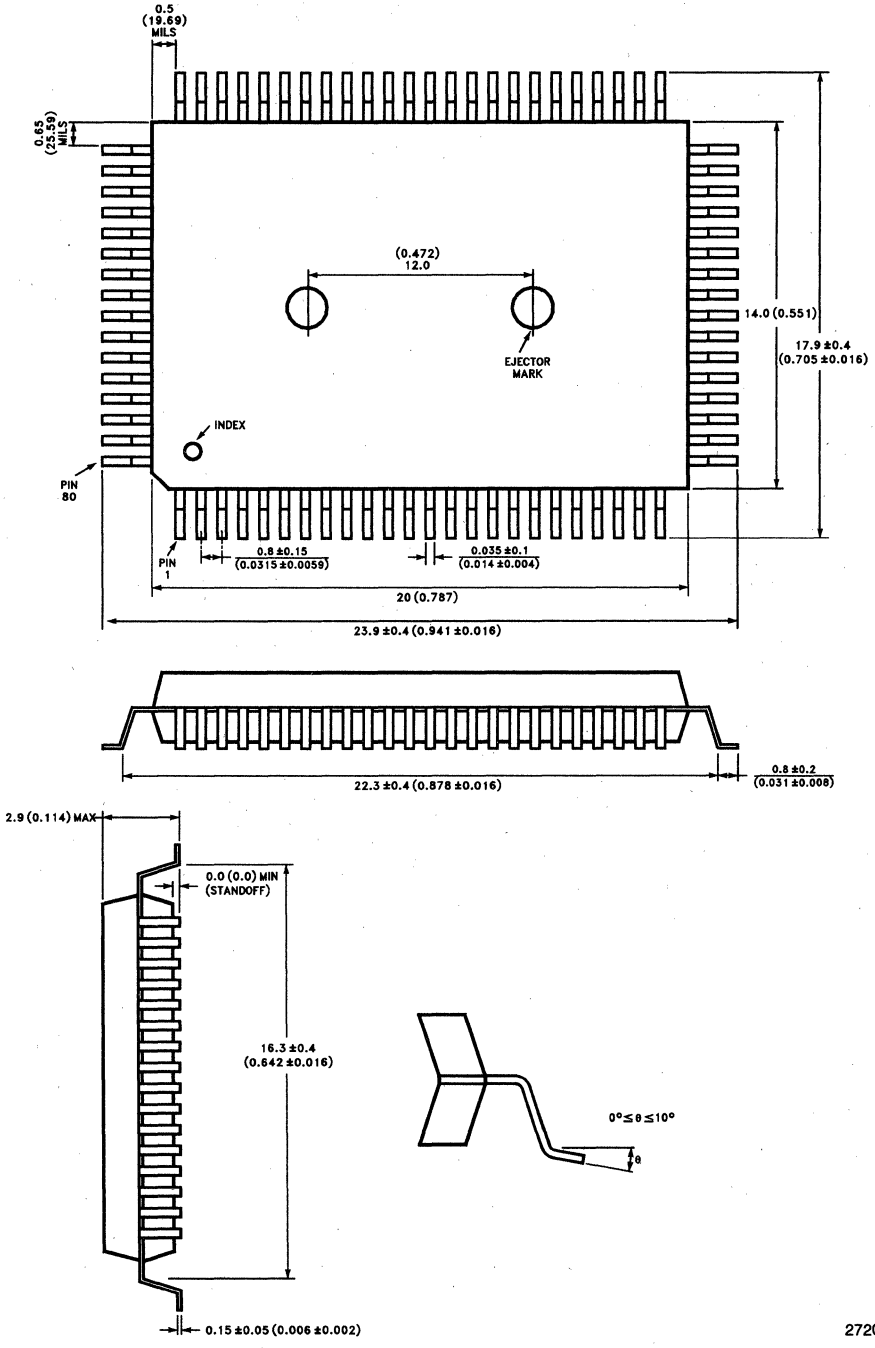


NOTE:
Units are mm (inches) unless specified.

Figure 12. QFP (EIAJ) Principal Dimensions

REVISION HISTORY

Intel 80L186EA devices are marked with a 9-character alphanumeric Intel FPO number underneath the product number. This data sheet (272021-001) is valid for 80L186EA devices with an "A" as the ninth character in the FPO number, as illustrated in Figure 2 for the 68-lead PLCC package and Figure 3 for the 80-lead QFP (EIAJ) package. Such devices may also be identified by reading a value of 01H from the STEPID register.

The following changes were made from revision −001 to −002 of this data sheet:

1. AC and DC specifications for 13 MHz parts were added.

80L186EA

An 80L186EA with a STEPID value of 01H or 02H has the following known errata. A device with a STEPID of 01H or 02H can be visually identified by noting the presence of a "A" or "B" alpha character, respectively, next to the FPO number. The FPO number location is shown in Figures 2 and 3.

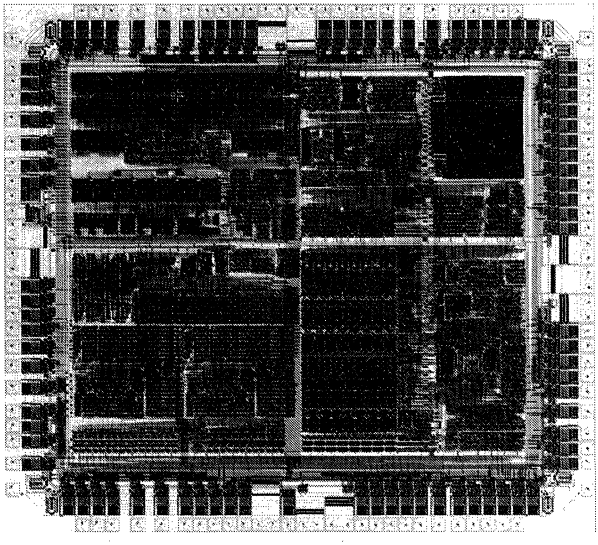
1. An internal condition with the interrupt controller can cause no acknowledge cycle on the INTA1 line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority input exists. This errata will not occur consistantly, it is dependent on interrupt timing.

80L186EB-13, -8
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSOR

• 3V Operation, V_{CC} = 2.7V–5.5V
• Full Static Operation
• True CMOS Inputs and Outputs
• −40°C to +85°C Operating Temperature Range

- **Integrated Feature Set**
  - **Low-Power Static CPU Core**
  - **Two Independent UARTs each with an Integral Baud Rate Generator**
  - **Two 8-Bit Multiplexed I/O Ports**
  - **Programmable Interrupt Controller**
  - **Three Programmable 16-Bit Timer/Counters**
  - **Clock Generator**
  - **Ten Programmable Chip Selects with Integral Wait-State Generator**
  - **Memory Refresh Control Unit**
  - **System Level Testing Support (ONCE™ Mode)**
- **Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O**
- **Speed Version Available:**
  - **−13 MHz (80L186EB-13)**
  - **8 MHz (80L186EB-8)**
- **Low-Power Operating Modes:**
  - **Idle Mode Freezes CPU Clocks but keeps Peripherals Active**
  - **Powerdown Mode Freezes All Internal Clocks**
- **Complete System Development Support**
  - **ASM86 Assembler, PL/M 86, Pascal 86, Fortran 86, C-86, and System Utilities**
  - **In-Circuit Emulator (ICE™-186EB)**
- **Available In:**
  - **80-Pin Quad Flat Pack (TS80L186EB)**
  - **84-Pin Plastic Leaded Chip Carrier (TN80L186EB)**

The 80L186EB is the 3V version of the 80C186EB embedded processor. By reducing V_{CC}, further power savings can be realized over the standard 80C186EB, making the 80L186EB ideal for battery-powered portable applications.



270921-1

May 1992
Order Number: 270921-003

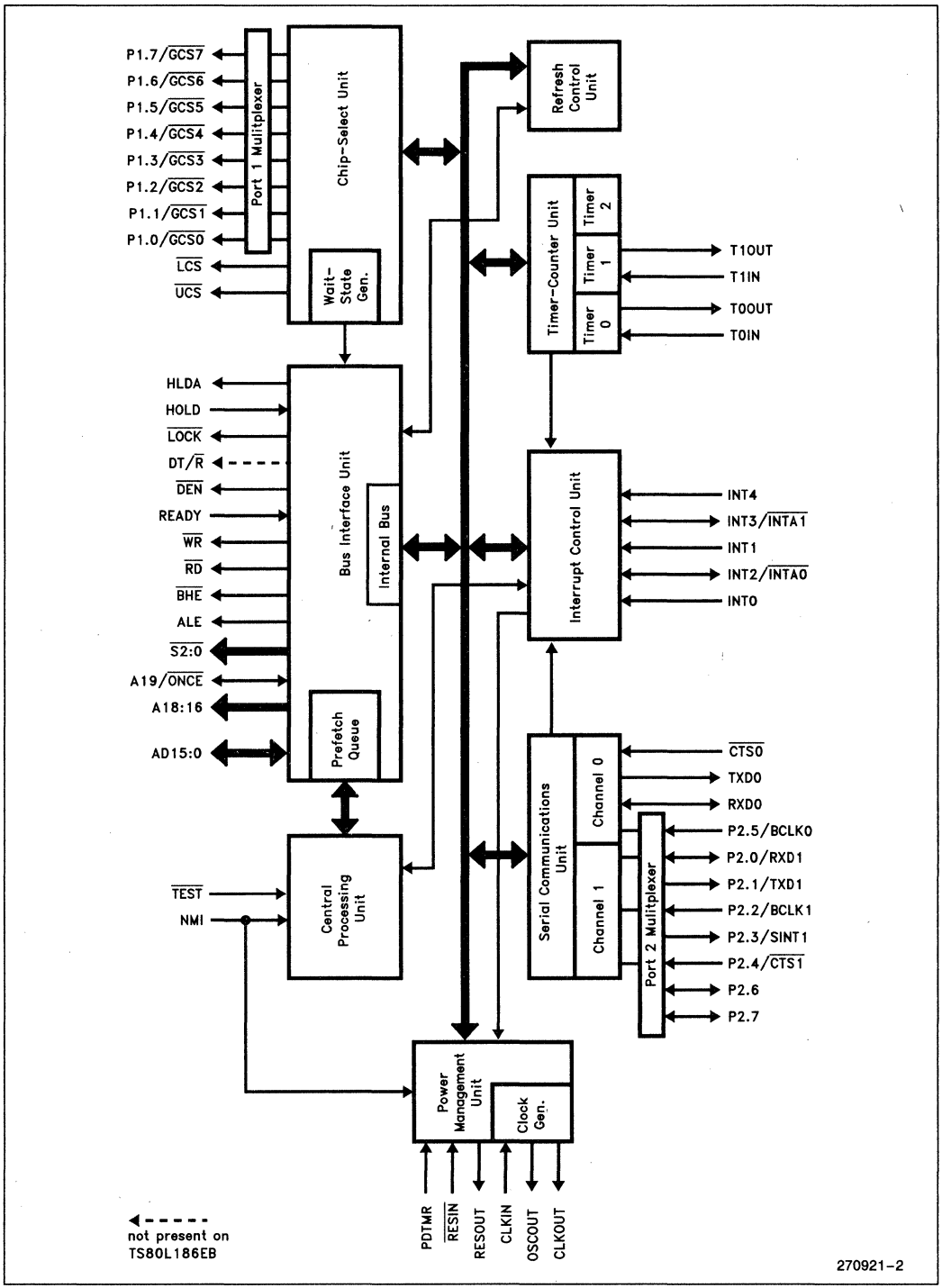


Figure 1. 80L186EB Block Diagram

INTRODUCTION

The 80L186EB is the first product in a new generation of low-power, high-integration microprocessors. It enhances the existing 186 family by offering new features and new operating modes. The 80L186EB is object code compatible with the 80C186/80C188 microprocessors.

The feature set of the 80L186EB meets the needs of battery-powered applications. Battery-powered applications benefit from the static CPU core and peripherals. Minimum current consumption is achieved by combining low voltage operation along with the features of the power management unit, thus maximizing battery life. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space critical applications benefit from the integration of commonly used system peripherals. Two serial channels are provided for services such as diagnostics, inter-processor communication, modem interface, terminal display interface and many others. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 129 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters and sixteen multiplexed I/O port pins round out the feature set of the 80L186EB.

OVERVIEW

Figure 1 shows a block diagram of the 80L186EB. The Execution Unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instructions and full static operation. The Bus Interface Unit (BIU) is the same as that found on the original 186 family products, except the queue-status mode has been deleted and buffer interface control has been changed to ease system design timings. An independent internal bus is used to allow communication between the BIU and internal peripherals.

PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the 80L186EB in the Plastic Leaded Chip Carrier (PLCC) package and Quad Flat Pack (QFP) package. For complete package specifications and information, see the Intel Packaging Handbook (Order Number: 240800).

80L186EB PINOUT

Tables 1 and 2 list the 80L186EB pin names with package location for the 84-pin Plastic Leaded Chip Carrier (PLCC) component. Figure 2 depicts the complete 80L186EB pinout (PLCC package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 3 and 4 list the 80L186EB pin names with package location for the 80-pin Quad Flat Pack (QFP) component. Figure 3 depicts the complete 80L186EB (QFP package) as viewed from the top side of the component (i.e., contacts facing down).

Table 1. PLCC Pin Names with Package Location

Address/Data Bus	
Name	**Location**
AD0	61
AD1	66
AD2	68
AD3	70
AD4	72
AD5	74
AD6	76
AD7	78
AD8	62
AD9	67
AD10	69
AD11	71
AD12	73
AD13	75
AD14	77
AD15	79
A16	80
A17	81
A18	82
A19/$\overline{\text{ONCE}}$	83

Bus Control	
Name	**Location**
ALE	6
$\overline{\text{BHE}}$	7
$\overline{\text{S0}}$	10
$\overline{\text{S1}}$	9
$\overline{\text{S2}}$	8
$\overline{\text{RD}}$	4
$\overline{\text{WR}}$	5
READY	18
$\overline{\text{DEN}}$	11
DT/$\overline{\text{R}}$	16
$\overline{\text{LOCK}}$	15
HOLD	13
HLDA	12

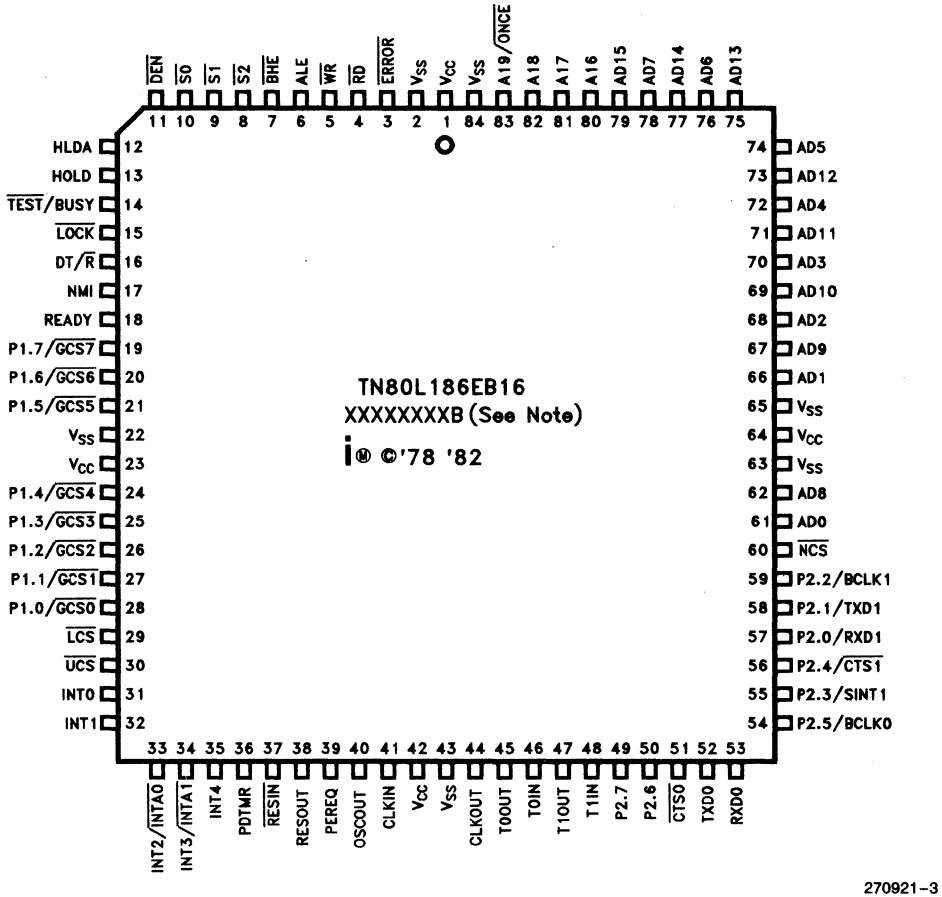
Power	
Name	**Location**
V_{CC}	1, 23, 42, 64
V_{SS}	2, 22, 43, 63, 65, 84

Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	37
RESOUT	38
CLKIN	41
OSCOUT	40
CLKOUT	44
$\overline{\text{TEST}}$	14
NC	60
NC	39
NC	3
PDTMR	36
NMI	17
INT0	31
INT1	32
INT2/$\overline{\text{INTA0}}$	33
INT3/$\overline{\text{INTA1}}$	34
INT4	35

I/O	
Name	**Location**
$\overline{\text{UCS}}$	30
$\overline{\text{LCS}}$	29
P1.0/$\overline{\text{GCS0}}$	28
P1.1/$\overline{\text{GCS1}}$	27
P1.2/$\overline{\text{GCS2}}$	26
P1.3/$\overline{\text{GCS3}}$	25
P1.4/$\overline{\text{GCS4}}$	24
P1.5/$\overline{\text{GCS5}}$	21
P1.6/$\overline{\text{GCS6}}$	20
P1.7/$\overline{\text{GCS7}}$	19
T0OUT	45
T0IN	46
T1OUT	47
T1IN	48
RXD0	53
TXD0	52
P2.5/BCLK0	54
$\overline{\text{CTS0}}$	51
P2.0/RXD1	57
P2.1/TXD1	58
P2.2/BCLK1	59
P2.3/SINT1	55
P2.4/$\overline{\text{CTS1}}$	56
P2.6	50
P2.7	49

Table 2. PLCC Package Locations with Pin Name

Location	Name	Location	Name	Location	Name	Location	Name
1	V_{CC}	22	V_{SS}	43	V_{SS}	64	V_{CC}
2	V_{SS}	23	V_{CC}	44	CLKOUT	65	V_{SS}
3	NC	24	P1.4/$\overline{GCS4}$	45	T0OUT	66	AD1
4	$\overline{RD}$	25	P1.3/$\overline{GCS3}$	46	T0IN	67	AD9
5	$\overline{WR}$	26	P1.2/$\overline{GCS2}$	47	T1OUT	68	AD2
6	ALE	27	P1.1/$\overline{GCS1}$	48	T1IN	69	AD10
7	$\overline{BHE}$	28	P1.0/$\overline{GCS0}$	49	P2.7	70	AD3
8	$\overline{S2}$	29	$\overline{LCS}$	50	P2.6	71	AD11
9	$\overline{S1}$	30	$\overline{UCS}$	51	$\overline{CTS0}$	72	AD4
10	$\overline{S0}$	31	INT0	52	TXD0	73	AD12
11	$\overline{DEN}$	32	INT1	53	RXD0	74	AD5
12	HLDA	33	INT2/$\overline{INTA0}$	54	P2.5/BCLK0	75	AD13
13	HOLD	34	INT3/$\overline{INTA1}$	55	P2.3/SINT1	76	AD6
14	$\overline{TEST}$	35	INT4	56	P2.4/$\overline{CTS1}$	77	AD14
15	$\overline{LOCK}$	36	PDTMR	57	P2.0/RXD1	78	AD7
16	DT/$\overline{R}$	37	$\overline{RESIN}$	58	P2.1/TXD1	79	AD15
17	NMI	38	RESOUT	59	P2.2/BCLK1	80	A16
18	READY	39	NC	60	NC	81	A17
19	P1.7/$\overline{GCS7}$	40	OSCOUT	61	AD0	82	A18
20	P1.6/$\overline{GCS6}$	41	CLKIN	62	AD8	83	A19/$\overline{ONCE}$
21	P1.5/$\overline{GCS5}$	42	V_{CC}	63	V_{SS}	84	V_{SS}



NOTE:
This is the FPO number location (indicated by X's).

Figure 2. 84-Pin Plastic Leaded Chip Carrier Pinout Diagram

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Table 3. QFP Pin Name with Package Location

Address/Data Bus	
Name	**Location**
AD0	10
AD1	15
AD2	17
AD3	19
AD4	21
AD5	23
AD6	25
AD7	27
AD8	11
AD9	16
AD10	18
AD11	20
AD12	22
AD13	24
AD14	26
AD15	28
A16	29
A17	30
A18	31
A19/$\overline{\text{ONCE}}$	32

Bus Control	
Name	**Location**
ALE	38
$\overline{\text{BHE}}$	39
$\overline{\text{S0}}$	42
$\overline{\text{S1}}$	41
$\overline{\text{S2}}$	40
$\overline{\text{RD}}$	36
$\overline{\text{WR}}$	37
READY	49
$\overline{\text{DEN}}$	43
$\overline{\text{LOCK}}$	47
HOLD	45
HLDA	44

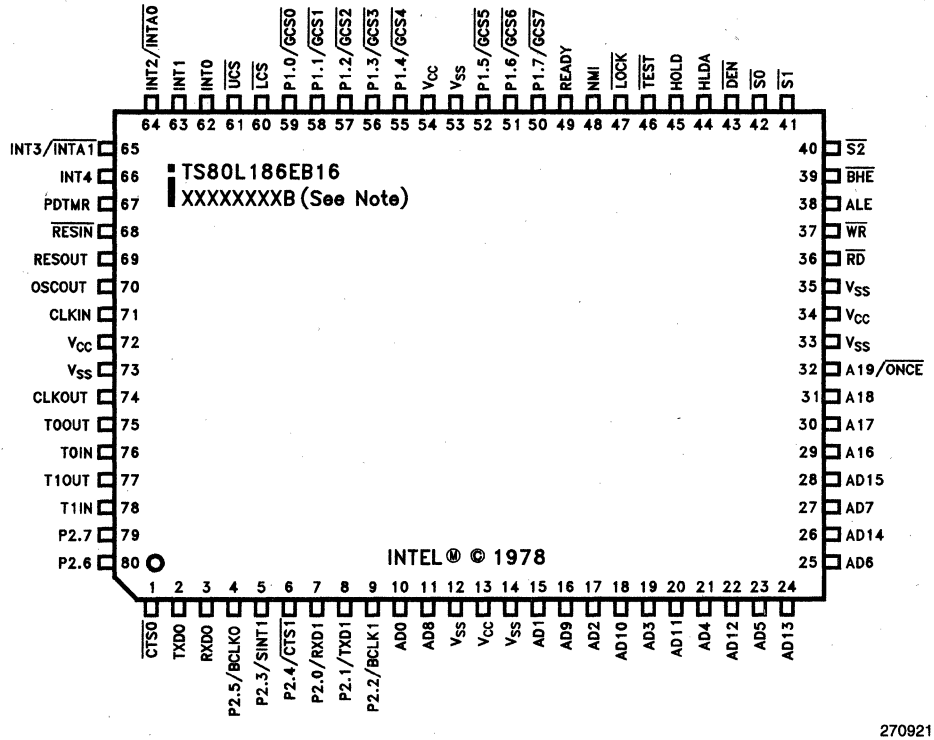
Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	68
RESOUT	69
CLKIN	71
OSCOUT	70
CLKOUT	74
$\overline{\text{TEST}}$	46
PDTMR	67
NMI	48
INT0	62
INT1	63
INT2/$\overline{\text{INTA0}}$	64
INT3/$\overline{\text{INTA1}}$	65
INT4	66

Power	
Name	**Location**
V_{CC}	13, 34, 54, 72
V_{SS}	12, 14, 33, 35, 53, 73

I/O	
Name	**Location**
$\overline{\text{UCS}}$	61
$\overline{\text{LCS}}$	60
P1.0/$\overline{\text{GCS0}}$	59
P1.1/$\overline{\text{GCS1}}$	58
P1.2/$\overline{\text{GCS2}}$	57
P1.3/$\overline{\text{GCS3}}$	56
P1.4/$\overline{\text{GCS4}}$	55
P1.5/$\overline{\text{GCS5}}$	52
P1.6/$\overline{\text{GCS6}}$	51
P1.7/$\overline{\text{GCS7}}$	50
T0OUT	75
T0IN	76
T1OUT	77
T1IN	78
RXD0	3
TXD0	2
P2.5/BCLK0	4
$\overline{\text{CTS0}}$	1
P2.0/RXD1	7
P2.1/TXD1	8
P2.2/BCLK1	9
P2.3/SINT1	5
P2.4/$\overline{\text{CTS1}}$	6
P2.6	80
P2.7	79

Table 4. QFP Package Location with Pin Names

Location	Name	Location	Name	Location	Name	Location	Name
1	$\overline{CTS0}$	21	AD4	41	$\overline{S1}$	61	$\overline{UCS}$
2	TXD0	22	AD12	42	$\overline{S0}$	62	INT0
3	RXD0	23	AD5	43	$\overline{DEN}$	63	INT1
4	P2.5/BCLK0	24	AD13	44	HLDA	64	INT2/$\overline{INTA0}$
5	P2.3/SINT1	25	AD6	45	HOLD	65	INT3/$\overline{INTA1}$
6	P2.4/$\overline{CTS1}$	26	AD14	46	$\overline{TEST}$	66	INT4
7	P2.0/RXD1	27	AD7	47	$\overline{LOCK}$	67	PDTMR
8	P2.1/TXD1	28	AD15	48	NMI	68	$\overline{RESIN}$
9	P2.2/BCLK1	29	A16	49	READY	69	RESOUT
10	AD0	30	A17	50	P1.7/$\overline{GCS7}$	70	OSCOUT
11	AD8	31	A18	51	P1.6/$\overline{GCS6}$	71	CLKIN
12	V_{SS}	32	A19/$\overline{ONCE}$	52	P1.5/$\overline{GCS5}$	72	V_{CC}
13	V_{CC}	33	V_{SS}	53	V_{SS}	73	V_{SS}
14	V_{SS}	34	V_{CC}	54	V_{CC}	74	CLKOUT
15	AD1	35	V_{SS}	55	P1.4/$\overline{GCS4}$	75	T0OUT
16	AD9	36	$\overline{RD}$	56	P1.3/$\overline{GCS3}$	76	T0IN
17	AD2	37	$\overline{WR}$	57	P1.2/$\overline{GCS2}$	77	T1OUT
18	AD10	38	ALE	58	P1.1/$\overline{GCS1}$	78	T1IN
19	AD3	39	$\overline{BHE}$	59	P1.0/$\overline{GCS0}$	79	P2.7
20	AD11	40	$\overline{S2}$	60	$\overline{LCS}$	80	P2.6



NOTE:
This is the FPO number location (indicated by X's).

Figure 3. Quad Flat Pack Pinout Diagram

PACKAGE THERMAL SPECIFICATIONS

The 80L186EB is specified for operation when T_C (the case temperature) is within the range of −40°C to +100°C (PLCC package) or −40°C to +114°C (QFP package). T_C may be measured in any environment to determine whether the 80L186EB is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P^*\theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 5 for the 84-pin Plastic Leaded Chip Carrier (PLCC) package.

Table 6 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies. P (the maximum power consumption, specified in watts) is calculated by using the maximum ICC as tabulated in the DC specifications and V_{CC} of 5V.

Table 5. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow Linear ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PLCC)	30	24	21	19	17	16.5
θ_{CA} (QFP)	58	47	43	40	38	36

Table 6. Maximum T_A at Various Airflows (in °C)

		Airflow Linear ft/min (m/sec)					
	T_F (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A (PLCC)	16	91.5	93.5	94	94.5	95.5	95.5
T_A (QFP)	16	98	101	102	103	103.5	104

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ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	−65°C to +150°C
Case Temp Under Bias	−65°C to +120°C
Supply Voltage wrt V_{SS}	−0.5V to +6.5V
Voltage on other Pins with Respect to V_{SS}	−0.5V to V_{CC} +0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	5.5	V
T_F	Input Clock Frequency			
	80L186EB13	0	26	MHz
	80L186EB8	0	16	MHz
T_C	Case Temperature Under Bias			
	N80L186EB (PLCC)	−40	+100	°C
	S80L186EB (QFP)	−40	+114	°C

RECOMMENDED CONNECTIONS

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80L186EB-based circuit board should include separate power (V_{CC}) and ground (V_{SS}) planes. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "NC" must not be connected in the system. Liberal decoupling capacitance should be placed near the 80L186EB. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by placing the decoupling capacitors as close as possible to the 80L186EB V_{CC} and V_{SS} package pins.

Always connect any unused input to an appropriate signal level. In particular, unused interrupt inputs (INT0:4) should be connected to V_{CC} through a pull-up resistor (in the range of 100 KΩ). **Leave any unused output pin or any NC pin unconnected.**

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	−0.5	0.3*V_{CC}	V	
V_{IH}	Input High Voltage	0.7*V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6 mA (Min) (Note 1)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −1 mA (Min) (Note 1)
V_{HYR}	Input Hysterisis on $\overline{RESIN}$	0.50		V	
I_{LI1}	Input Leakage Current for pins: AD15:0, READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$, NMI, INT4:0, T0IN, T1IN, RXD0, $\overline{BCLK0}$, $\overline{CTS0}$, RXD1, $\overline{BCLK1}$, $\overline{CTS1}$, SINT1, P2.6, P2.7		±15	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LI2}	Input Leakage Current for pins: A19/$\overline{ONCE}$, A18:16, $\overline{LOCK}$	−0.275	−5	μA	V_{IN} = 0.7 V_{CC} (Note 2)
I_{LO}	Output Leakage Current		±15	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 3)
I_{CC5}	Supply Current (RESET, 5.5V) 80L186EB-13 80L186EB-8		 70 45	 mA mA	 (Note 4) (Note 4)
I_{CC3}	Supply Current (RESET, 2.7V) 80L186EB-13 80L186EB-8		 26 22	 mA mA	 (Note 4) (Note 4)
I_{ID5}	Supply Current Idle (5.5V) 80L186EB-13 80L186EB-8		 48 31	 mA mA	 (Note 5) (Note 5)
I_{ID3}	Supply Current Idle (2.7V) 80L186EB-13 80L186EB-8		 24 15	 mA mA	 (Note 5) (Note 5)
I_{PD5}	Supply Current Powerdown (5.5V) 80L186EB-13 80L186EB-8		 100 100	 μA μA	 (Note 6) (Note 6)
I_{PD3}	Supply Current Powerdown (2.7V) 80L186EB-13 80L186EB-8		 30 30	 μA μA	 (Note 6) (Note 6)
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 7)

NOTES:
1. I_{OL} and I_{OH} measured at V_{CC} = 2.7V.
2. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
3. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
4. Measured with the device in RESET and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
5. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
6. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
7. Output Capacitance is the capacitive load of a floating output pin.

I_{CC} VERSUS FREQUENCY AND VOLTAGE

The current (I_{CC}) consumption of the 80L186EB is essentially composed of two components; I_{PD} and I_{CCS}.

I_{PD} is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or V_{CC} (no clock applied to the device). I_{PD} is equal to the Powerdown current and is typically less than 50 μA.

I_{CCS} is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since I_{CCS} is typically much greater than I_{PD}, I_{PD} can often be ignored when calculating I_{CC}.

I_{CCS} is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: V = Device operating voltage (V_{CC})

C_{DEV} = Device capacitance

f = Device operating frequency

I_{CCS} = I_{CC} = Device current

Measuring C_{DEV} on a device like the 80C186EB would be difficult. Instead, C_{DEV} is calculated using the above formula by measuring I_{CC} at a known V_{CC} and frequency (see Table 7). Using this C_{DEV} value, I_{CC} can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical I_{CC} when operating at 8 MHz, 3V.

$$I_{CC} = I_{CCS} = 3 \times 0.583 \times 8 \approx 14 \text{ mA}$$

PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: t = desired delay in **seconds**

C_{PD} = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132$ μF is required. Round up to standard (available) capacitive values.

NOTE:
The above equation applies to delay times greater than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperature will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

Table 7. Device Capacitance (C_{DEV}) Values

Parameter	Typ	Max	Units	Notes
C_{DEV} (Device in Reset)	0.583	1.02	mA/V*MHz	1, 2
C_{DEV} (Device in Idle)	0.408	0.682	mA/V*MHz	1, 2

NOTES:
1. Max C_{DEV} is calculated at −40°C, all floating outputs driven to V_{CC} or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical C_{DEV} is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

AC SPECIFICATIONS

AC Characteristics—(80L186EB-8)

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	16	MHz	1
T_C	CLKIN Period	62.5	∞	ns	1
T_{CH}	CLKIN High Time	15	∞	ns	1, 2
T_{CL}	CLKIN Low Time	15	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	50	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	15	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	15	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	30	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	3	35	ns	1, 4, 6, 7
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	30	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD15:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$	3	35	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	35	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, T1:OIN, P2.6, P2.7 READY, $\overline{CTS1:0}$, BCLK1:0	25		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, T1:OIN, BCLK1:0 READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD15:0, READY	25		ns	1, 10
T_{CLIH}	READY, AD15:0	3		ns	1, 10
T_{CLIS}	HOLD	25		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 10 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 11 for rise and fall times outside 50 pF.
6. See Figure 11 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L186EB operation.

AC SPECIFICATIONS

AC Characteristics—(80L186EB-13)

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	26	MHz	1
T_C	CLKIN Period	38.5	∞	ns	1
T_{CH}	CLKIN High Time	15	∞	ns	1, 2
T_{CL}	CLKIN Low Time	15	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	40	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	10	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	10	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	25	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{RD}$, $\overline{WR}$	3	30	ns	1, 4, 6, 7
T_{CLOV1}	$\overline{BHE}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	25	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, A15:8, AD7:0, $\overline{NCS}$, $\overline{INTA1:0}$	3	30	ns	1, 4, 6
T_{CLOV3}	$\overline{S2:0}$	3	35	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$	0	35	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, T1:OIN, P2.6, P2.7 READY, $\overline{CTS1:0}$, BCLK1:0	20		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, T1:OIN, BCLK1:0 READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD15:0, READY	20		ns	1, 10
T_{CLIH}	READY, AD15:0	3		ns	1, 10
T_{CLIS}	HOLD	20		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 10 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 11 for rise and fall times outside 50 pF.
6. See Figure 11 for rise and fall times.
7. T_{CHOV1} applies to $\overline{BHE}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L186EB operation.

AC SPECIFICATIONS (Continued)

Relative Timings (80L186EB-8, -13)

Symbol	Parameter	Min	Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Rising to ALE Falling	T − 15		ns	
T_{AVLL}	Address Valid to ALE Falling	½T − 10		ns	
T_{PLLL}	Chip Selects Valid to ALE Falling	½T − 10		ns	1
T_{LLAX}	Address Hold from ALE Falling	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{WHLH}	$\overline{WR}$ Rising to ALE Rising	½T − 10		ns	1
T_{AFRL}	Address Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Falling to $\overline{RD}$ Rising	(2*T) − 5		ns	2
T_{WLWH}	$\overline{WR}$ Falling to $\overline{WR}$ Rising	(2*T) − 5		ns	2
T_{RHAX}	$\overline{RD}$ Rising to Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHPH}	$\overline{WR}$ Rising to Chip Select Rising	½T − 10		ns	1
T_{RHPH}	$\overline{RD}$ Rising to Chip Select Rising	½T − 10		ns	1
T_{PHPL}	$\overline{CS}$ Active to $\overline{CS}$ Inactive	½T − 10		ns	1
T_{OVRH}	$\overline{ONCE}$ Active to $\overline{RESIN}$ Rising	1T		ns	
T_{RHOX}	$\overline{ONCE}$ Hold from $\overline{RESIN}$ Rising	1T		ns	

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.

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AC SPECIFICATIONS (Continued)

Serial Port Mode 0 Timings (80L186EB-8, -13)

Symbol	Parameter	Min	Max	Unit	Notes
T_{XLXL}	TXD Clock Period	T(N + 1)		ns	1, 2
T_{XLXH}	TXD Clock Low to Clock High (N > 1)	2T − 35	2T + 35	ns	1, 2
T_{XLXH}	TXD Clock Low to Clock High (N = 1)	T − 35	T + 35	ns	1, 2
T_{XHXL}	TXD Clock High to Clock Low (N > 1)	T(N − 1) − 35	T(N − 1) + 35	ns	2
T_{XHXL}	TXD Clock High to Clock Low (N = 1)	T − 35	T + 35	ns	2
T_{QVXH}	RXD Output Data Setup to TXD Clock High (n > 1)	T (n − 1) − 35		ns	1, 2
T_{QVXH}	RXD Output Data Setup to TXD Clock High (n = 1)	T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (n > 1)	2T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (n = 1)	T − 35		ns	1
T_{XHQZ}	RXD Output Data Float after Last TXD Clock High		T + 20	ns	1
T_{DVXH}	RXD Input Data Setup to TXD Clock High	T + 20		ns	1
T_{XHDX}	RXD Input Data Hold after TXD Clock High	0		ns	1

NOTES:
1. See Figure 9 for waveforms.
2. n is the value of the BxCMP register ignoring the ICLK Bit (i.e., ICLK = 0).

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 4. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

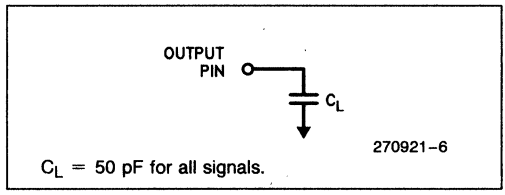

Figure 4. AC Test Load

AC TIMING WAVEFORMS

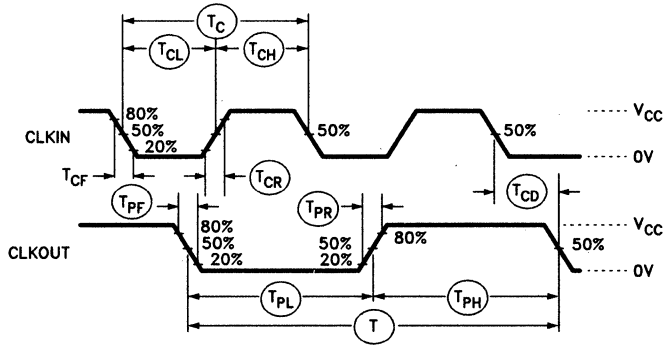

Figure 5. Input and Output Clock Waveform

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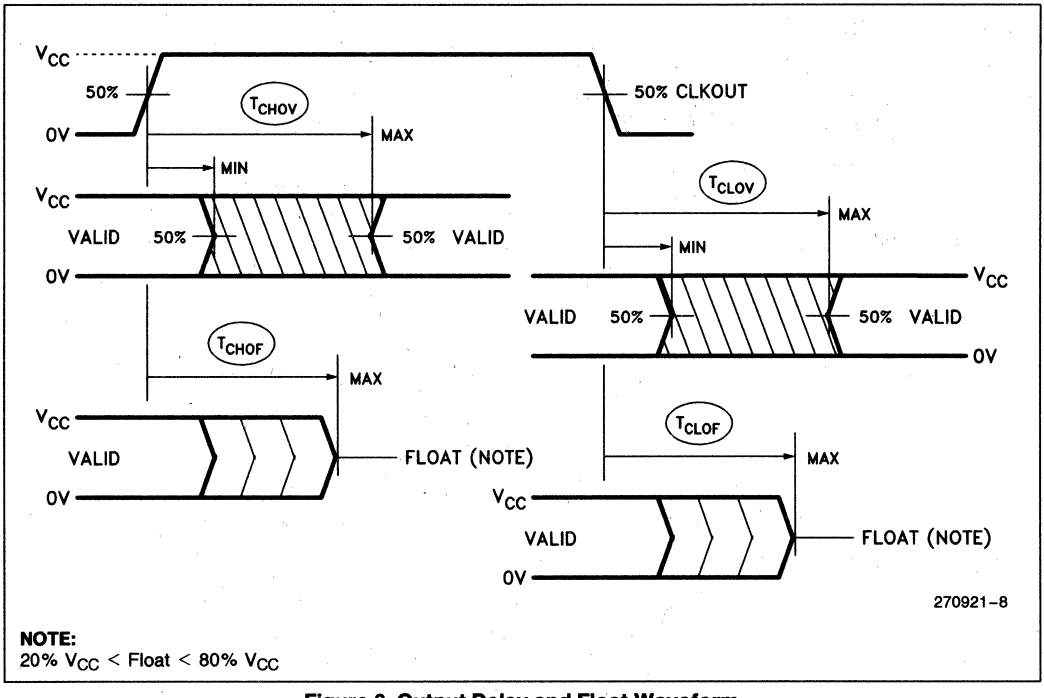

NOTE:
20% V_{CC} < Float < 80% V_{CC}

Figure 6. Output Delay and Float Waveform

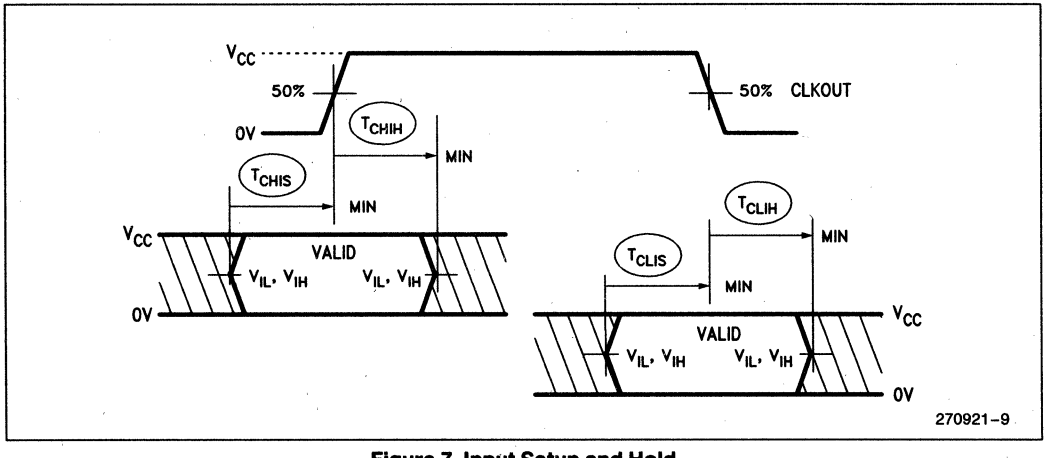

Figure 7. Input Setup and Hold

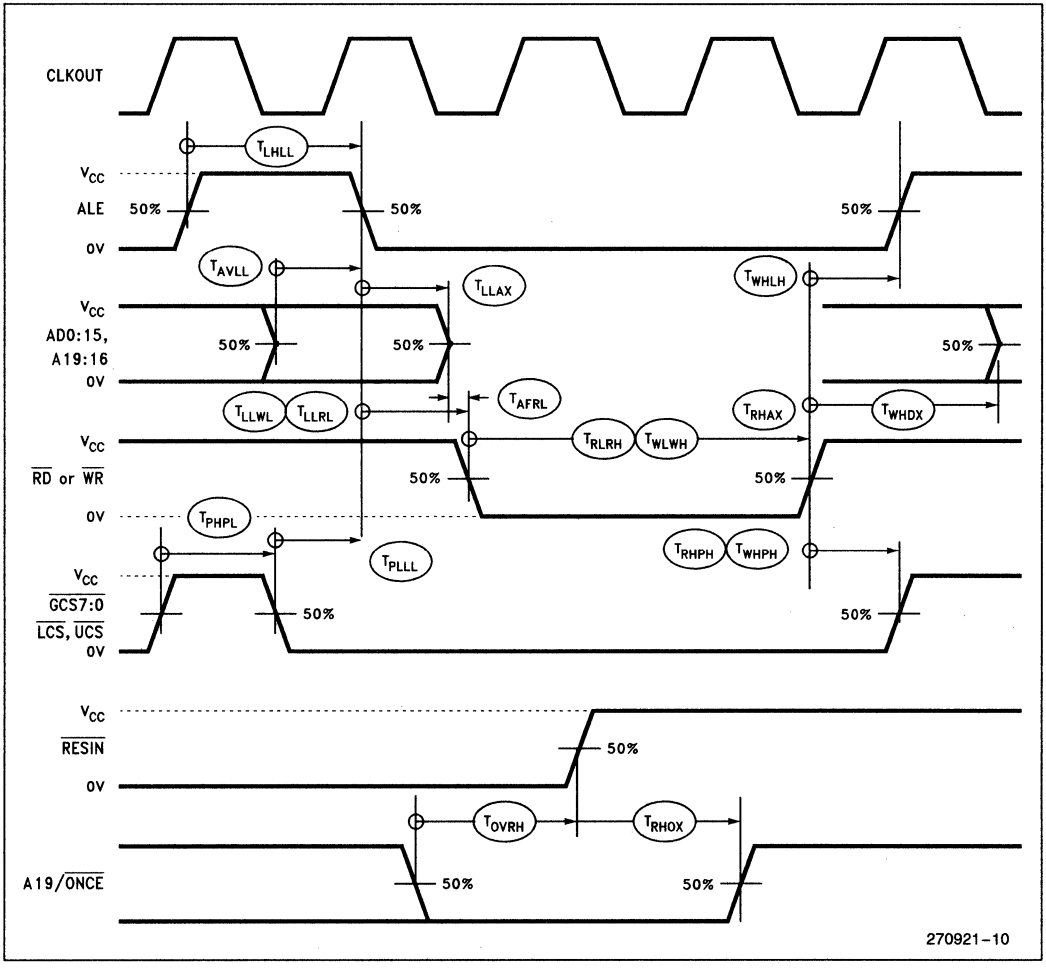

Figure 8. Relative Signal Waveform

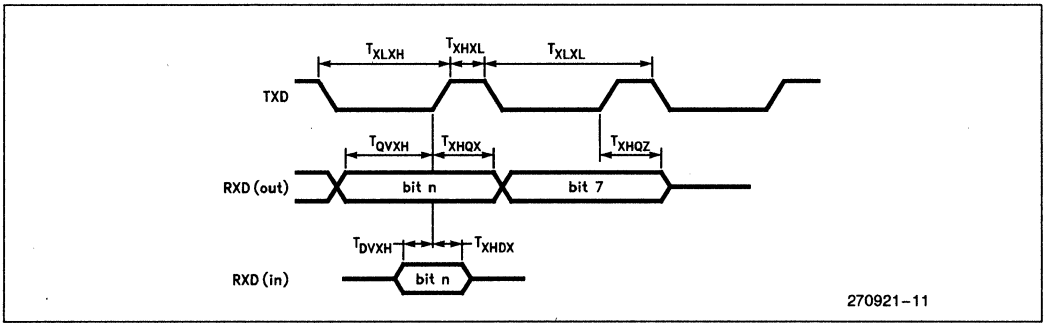

Figure 9. Serial Port Mode 0 Waveform

DERATING CURVES

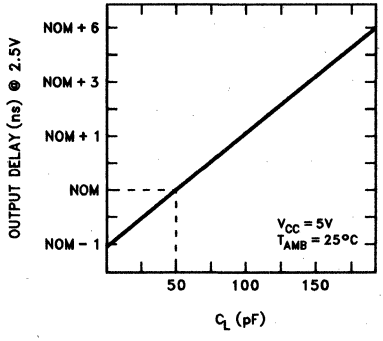

Figure 10. Typical Output Delay Variations vs Load Capacitance

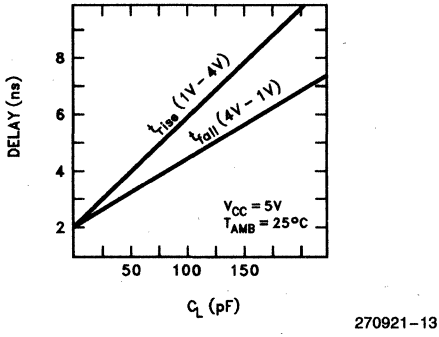

Figure 11. Typical Rise and Fall Variations vs Load Capacitance

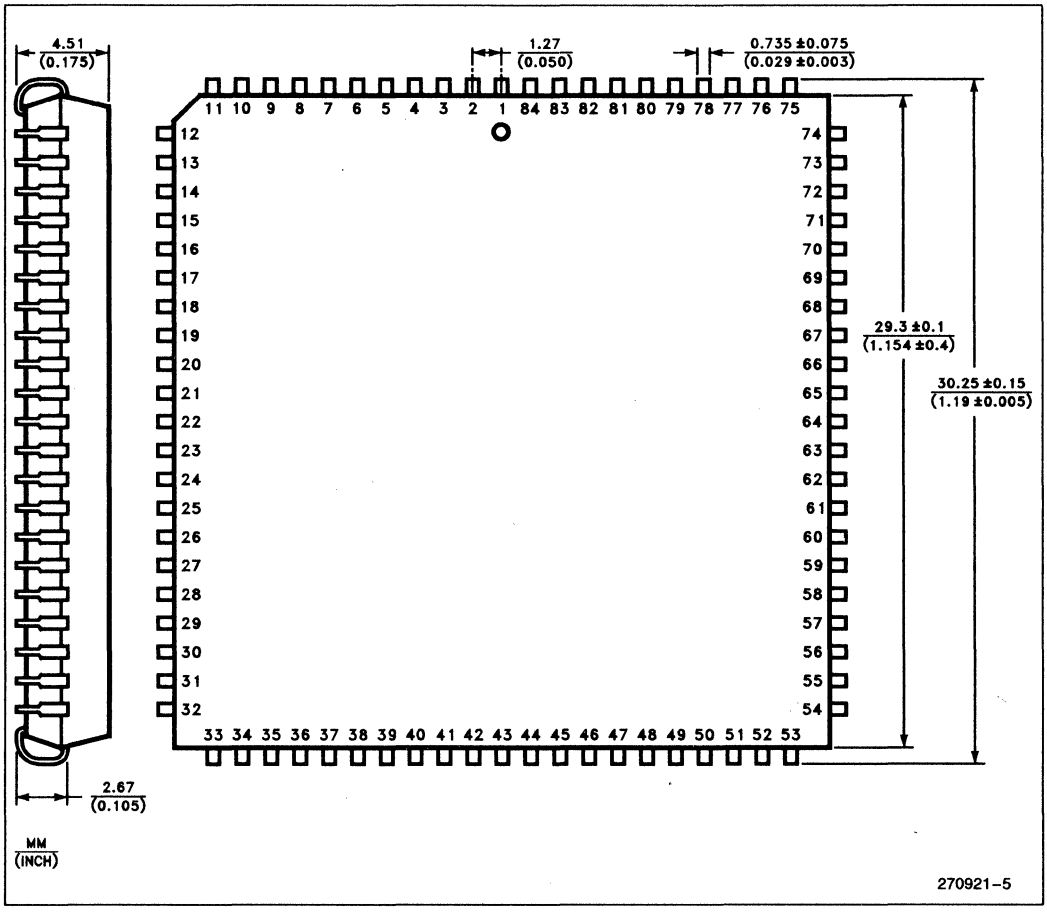

Figure 12. PLCC Principal Dimensions

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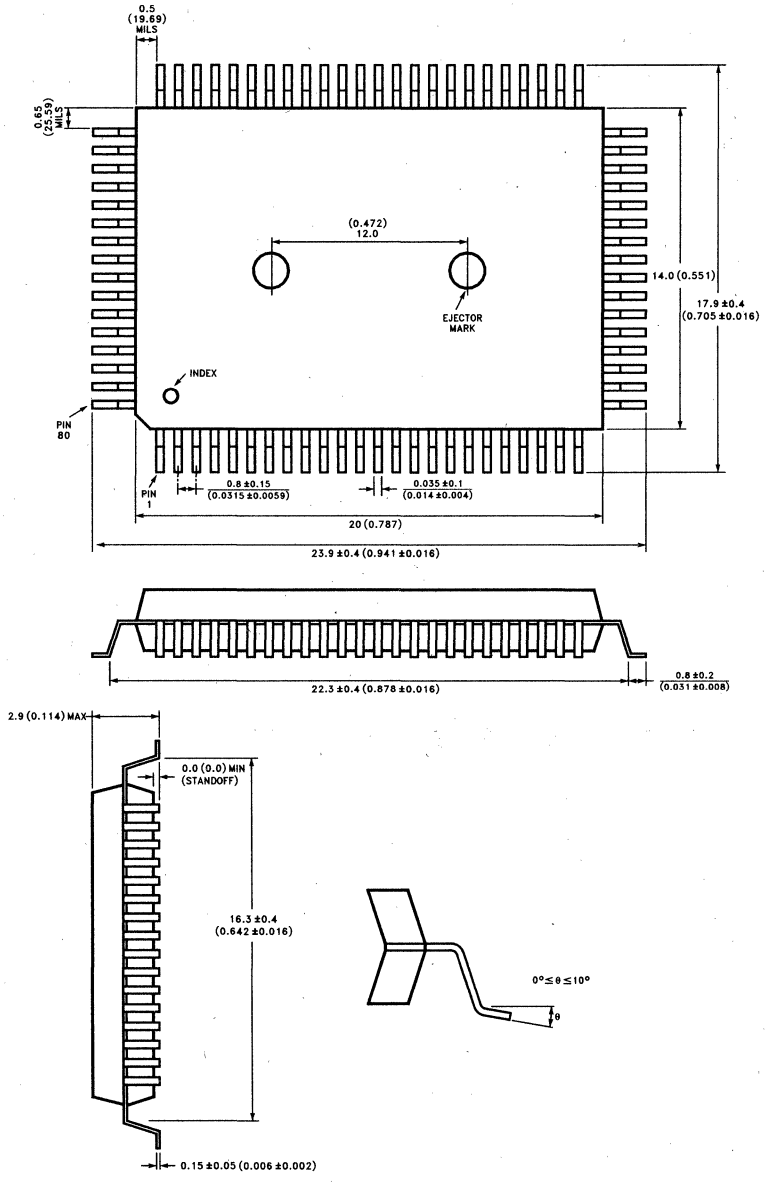

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NOTE:
Units are mm (inches) unless specified.

Figure 13. QFP Principal Dimensions

ERRATA

An 80L186EB with a STEPID value of 0001H has the following known errata. A device with a STEPID of 0001H can be visually identified by noting the **absence** of an alpha character next to the FPO number or by the **presence** of an **"A"** alpha character next to the FPO number. The FPO number location is shown in Figures 2 and 3.

1. A19/$\overline{\text{ONCE}}$ is not latched by the rising edge of $\overline{\text{RESIN}}$. A19/$\overline{\text{ONCE}}$ must remain active (LOW) at all times to remain in the ONCE™ Mode. Removing A19/$\overline{\text{ONCE}}$ after $\overline{\text{RESIN}}$ is high will return all output pins to a driving state, however, the 80L186EB will remain in a reset state.
2. During interrupt acknowledge (INTA) bus cycles, the bus controller will ignore the state of the READY pin if the previous bus cycle ignored the state of the READY pin. This errata can only occur if the Chip-Select Unit is being used. All active chip-selects must be programmed to use READY (RDY bit must be programmed to a 1) if wait-states are required for INTA bus cycles.
3. CLKOUT will transition off the **rising** edge of CLKIN rather than the falling edge of CLKIN. This does not affect any bus timings other than T_{CICO}.
4. $\overline{\text{RESIN}}$ has a hysterisis of only 130 mV. It is recommended that $\overline{\text{RESIN}}$ be driven with a Schmitt triggered device to avoid processor lockup during reset when using an RC circuit.
5. SINT1 will only go active for one clock period when a receive or transmit interrupt is pending (i.e., it does not remain active until the S1STS register is read). If SINT1 is to be connected to any of the 80L186EB interrupt lines (INT0–INT4), then it must be latched by user logic.

An 80L188EB with a STEPID value of 0001H or 0002H has the following known errata. Otherwise, an 80L188EB with a STEPID value of 0002H has no known errata (as of this publication). A device with a STEPID of 0002H can be visually identified by noting the presence of a "B" or "C" alpha character next to the FPO number. The FPO number location is shown in Figures 2 and *3*.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the $\overline{\text{INTA1}}$ line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistantly, it is dependent on interrupt timing.

REVISION HISTORY

The following changes have been made between the -001 version and this (-002) version of the 80L186EB data sheet. This -002 data sheet applies to any 80L186EB with a "B" alpha character after the FPO number. The FPO number location is shown in Figures 2 and 3.

1. The data sheet was changed from a Product Preview version to an Advance Information version.
2. The DC specifications table has changed. Also, notes have been changed/added.
3. Graphs for I_{CC} versus Frequency have been changed to equations with supporting text.
4. Graphs for PDTMR pin capacitance have been changed to equations with supporting text.
5. Serial port MODE 0 timings have been changed.
6. Various typing errors have been corrected throughout the document.

The following changes were made between the -002 and -003 versions of the 80L188EB data sheets. The -003 data sheet applies to any 80L188EB with a "B" alpha character after the FPO number. The FPO number location is shown in Figures 2 and 3.

1. 13 MHz Electrical, DC and AC Specifications were added to the appropriate sections.
2. The timing T_{CLOV3} was added to the AC Specifications for $\overline{\text{S2:0}}$.
3. An errata appearing on both A and B steppings (INTA1) was added.

80C187
80-BIT MATH COPROCESSOR

- **High Performance 80-Bit Internal Architecture**
- **Implements ANSI/IEEE Standard 754-1985 for Binary Floating-Point Arithmetic**
- **Upward Object-Code Compatible from 8087**
- **Fully Compatible with 387™DX and 387™SX Math Coprocessors. Implements all 387 Architectural Enhancements over 8087**
- **Directly Interfaces with 80C186 CPU**
- **80C186/80C187 Provide a Software/ Binary Compatible Upgrade from 80186/82188/8087 Systems**
- **Expands 80C186's Data Types to Include 32-, 64-, 80-Bit Floating-Point, 32-, 64-Bit Integers and 18-Digit BCD Operands**
- **Directly Extends 80C186's Instruction Set to Trigonometric, Logarithmic, Exponential, and Arithmetic Instructions for All Data Types**
- **Full-Range Transcendental Operations for SINE, COSINE, TANGENT, ARCTANGENT, and LOGARITHM**
- **Built-In Exception Handling**
- **Eight 80-Bit Numeric Registers, Usable as Individually Addressable General Registers or as a Register Stack**
- **Available in 40-Pin CERDIP and 44-Pin PLCC Package**

  (See Packaging Outlines and Dimensions, Order #231369)

The Intel 80C187 is a high-performance math coprocessor that extends the architecture of the 80C186 with floating-point, extended integer, and BCD data types. A computing system that includes the 80C187 fully conforms to the IEEE Floating-Point Standard. The 80C187 adds over seventy mnemonics to the instruction set of the 80C186, including support for arithmetic, logarithmic, exponential, and trigonometric mathematical operations. The 80C187 is implemented with 1.5 micron, high-speed CHMOS III technology and packaged in both a 40-pin CERDIP and a 44-pin PLCC package. The 80C187 is upward object-code compatible from the 8087 math coprocessor and will execute code written for the 80387DX and 80387SX math coprocessors.

August 1990
Order Number: 270640-004

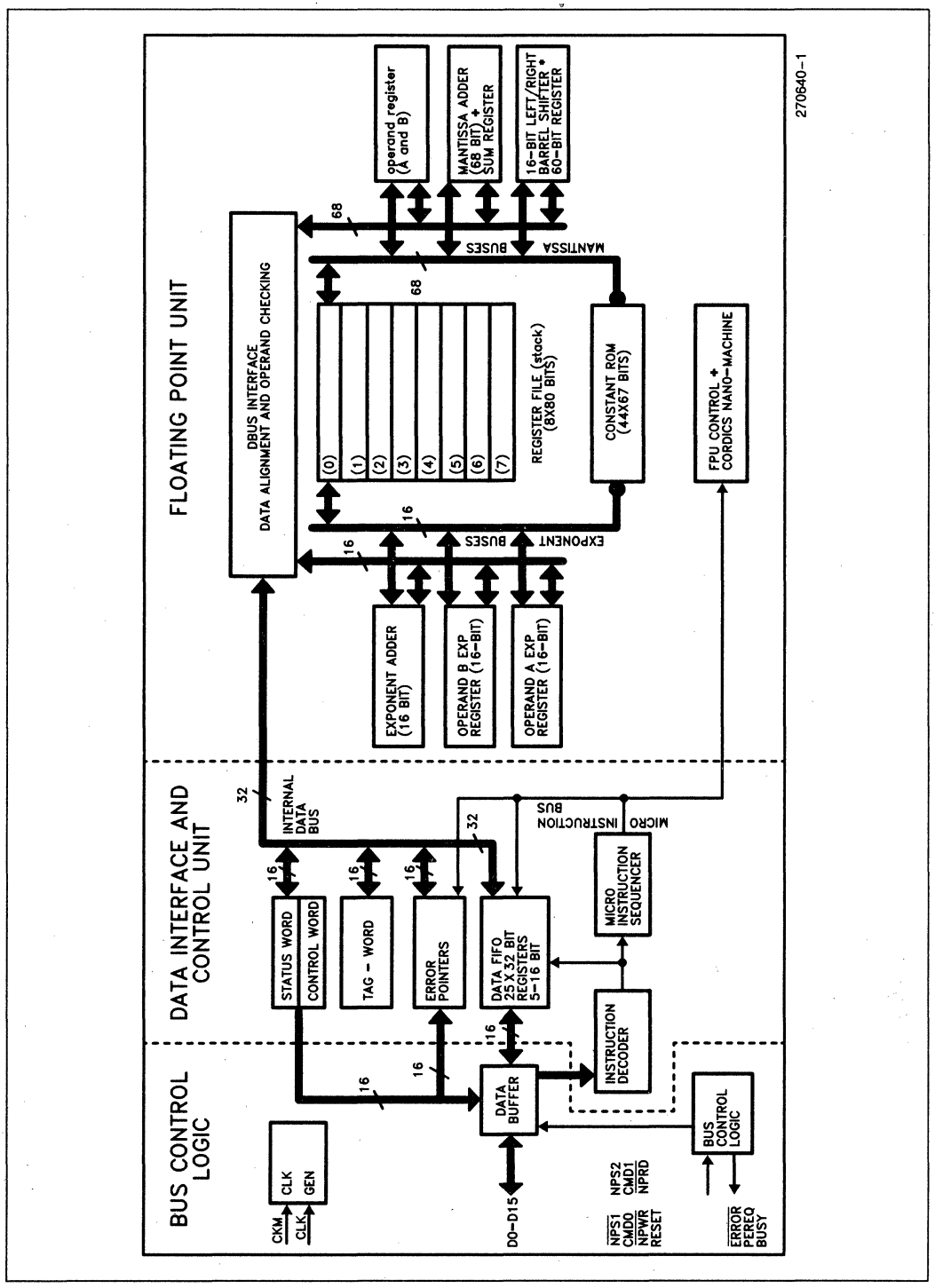


Figure 1. 80C187 Block Diagram

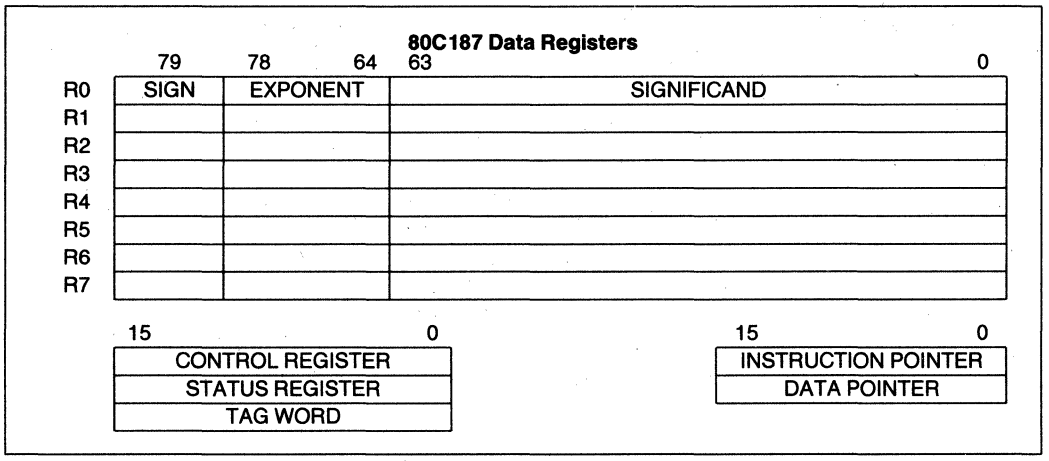


Figure 2. Register Set

FUNCTIONAL DESCRIPTION

The 80C187 Math Coprocessor provides arithmetic instructions for a variety of numeric data types. It also executes numerous built-in transcendental functions (e.g. tangent, sine, cosine, and log functions). The 80C187 effectively extends the register and instruction set of the 80C186 CPU for existing data types and adds several new data types as well. Figure 2 shows the additional registers visible to programs in a system that includes the 80C187. Essentially, the 80C187 can be treated as an additional resource or an extension to the CPU. The 80C186 CPU together with an 80C187 can be used as a single unified system.

A 80C186 system that includes the 80C187 is completely upward compatible with software for the 8086/8087.

The 80C187 interfaces only with the 80C186 CPU. The interface hardware for the 80C187 is not implemented on the 80C188.

PROGRAMMING INTERFACE

The 80C187 adds to the CPU additional data types, registers, instructions, and interrupts specifically designed to facilitate high-speed numerics processing. All new instructions and data types are directly supported by the assembler and compilers for high-level languages. The 80C187 also supports the full 80387DX instruction set.

All communication between the CPU and the 80C187 is transparent to applications software. The CPU automatically controls the 80C187 whenever a numerics instruction is executed. All physical memory and virtual memory of the CPU are available for storage of the instructions and operands of programs that use the 80C187. All memory addressing modes are available for addressing numerics operands.

The end of this data sheet lists by class the instructions that the 80C187 adds to the instruction set.

NOTE:
The 80C187 Math Coprocessor is also referred to as a Numeric Processor Extension (NPX) in this document.

Data Types

Table 1 lists the seven data types that the 80C187 supports and presents the format for each type. Operands are stored in memory with the least significant digit at the lowest memory address. Programs retrieve these values by generating the lowest address. For maximum system performance, all operands should start at even physical-memory addresses; operands may begin at odd addresses, but will require extra memory cycles to access the entire operand.

Internally, the 80C187 holds all numbers in the extended-precision real format. Instructions that load operands from memory automatically convert operands represented in memory as 16-, 32-, or 64-bit integers, 32- or 64-bit floating-point numbers, or 18-digit packed BCD numbers into extended-precision real format. Instructions that store operands in memory perform the inverse type conversion.

Numeric Operands

A typical NPX instruction accepts one or two operands and produces one (or sometimes two) results. In two-operand instructions, one operand is the contents of an NPX register, while the other may be a memory location. The operands of some instructions are predefined; for example, FSQRT always takes the square root of the number in the top stack element (refer to the section on Data Registers).

Register Set

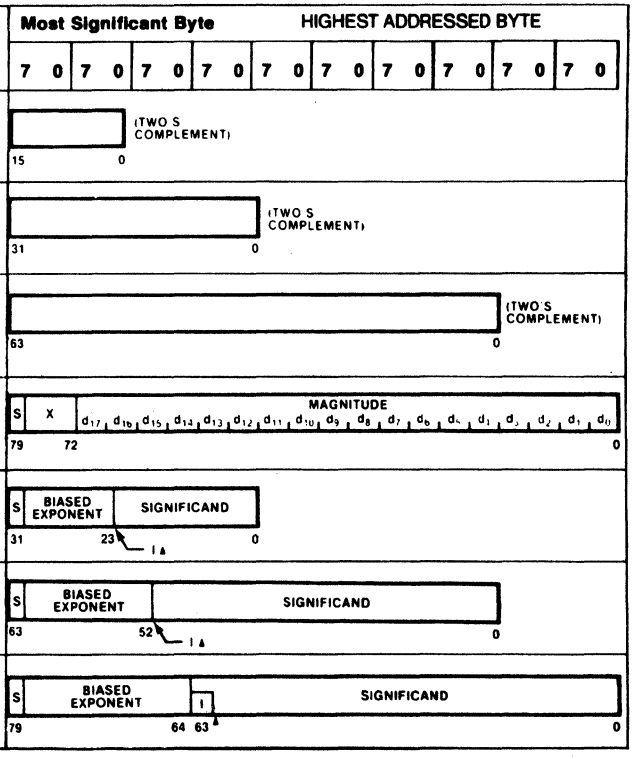
Figure 2 shows the 80C187 register set. When an 80C187 is present in a system, programmers may use these registers in addition to the registers normally available on the CPU.

DATA REGISTERS

80C187 computations use the extended-precision real data type.

Table 1. Data Type Representation in Memory

Data Formats	Range	Precision
Word Integer	$\pm 10^4$	16 Bits
Short Integer	$\pm 10^9$	32 Bits
Long Integer	$\pm 10^{18}$	64 Bits
Packed BCD	$\pm 10^{18}$	18 Digits
Single Precision	$\pm 10^{\pm 38}$	24 Bits
Double Precision	$\pm 10^{\pm 308}$	53 Bits
Extended Precision	$\pm 10^{\pm 4932}$	64 Bits



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NOTES:
1. S = Sign bit (0 = Positive, 1 = Negative)
2. d_n = Decimal digit (two per byte)
3. X = Bits have no significance; 80C187 ignores when loading, zeros when storing
4. ▲ = Position of implicit binary point
5. I = Integer bit of significand; stored in temporary real, implicit in single and double precision
6. Exponent Bias (normalized values):
   Single: 127 (7FH)
   Double: 1023 (3FFH)
   Extended Real: 16383 (3FFFH)
7. Packed BCD: $(-1)^S (D_{17} \ldots D_0)$
8. Real: $(-1)^S (2^{E\text{-BIAS}}) (F_0, F_1 \ldots)$

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The 80C187 register set can be accessed either as a stack, with instructions operating on the top one or two stack elements, or as individually addressable registers. The TOP field in the status word identifies the current top-of-stack register. A "push" operation decrements TOP by one and loads a value into the new top register. A "pop" operation stores the value from the current top register and then increments TOP by one. The 80C187 register stack grows "down" toward lower-addressed registers.

Instructions may address the data registers either implicitly or explicitly. Many instructions operate on the register at the TOP of the stack. These instructions implicitly address the register at which TOP points. Other instructions allow the programmer to explicitly specify which register to use. This explicit addressing is also relative to TOP.

TAG WORD

The tag word marks the content of each numeric data register, as Figure 3 shows. Each two-bit tag represents one of the eight data registers. The principal function of the tag word is to optimize the NPX's performance and stack handling by making it possible to distinguish between empty and nonempty register locations. It also enables exception handlers to identify special values (e.g. NaNs or denormals) in the contents of a stack location without the need to perform complex decoding of the actual data.

STATUS WORD

The 16-bit status word (in the status register) shown in Figure 4 reflects the overall state of the 80C187. It may be read and inspected by programs.

Bit 15, the B-bit (busy bit) is included for 8087 compatibility only. It always has the same value as the ES bit (bit 7 of the status word); it does **not** indicate the status of the BUSY output of 80C187.

Bits 13–11 (TOP) point to the 80C187 register that is the current top-of-stack.

The four numeric condition code bits (C_3–C_0) are similar to the flags in a CPU; instructions that perform arithmetic operations update these bits to reflect the outcome. The effects of these instructions on the condition code are summarized in Tables 2 through 5.

Bit 7 is the error summary (ES) status bit. This bit is set if any unmasked exception bit is set; it is clear otherwise. If this bit is set, the $\overline{\text{ERROR}}$ signal is asserted.

Bit 6 is the stack flag (SF). This bit is used to distinguish invalid operations due to stack overflow or underflow from other kinds of invalid operations. When SF is set, bit 9 (C_1) distinguishes between stack overflow (C_1 = 1) and underflow (C_1 = 0).

Figure 4 shows the six exception flags in bits 5–0 of the status word. Bits 5–0 are set to indicate that the 80C187 has detected an exception while executing an instruction. A later section entitled "Exception Handling" explains how they are set and used.

Note that when a new value is loaded into the status word by the FLDENV or FRSTOR instruction, the value of ES (bit 7) and its reflection in the B-bit (bit 15) are not derived from the values loaded from memory but rather are dependent upon the values of the exception flags (bits 5–0) in the status word and their corresponding masks in the control word. If ES is set in such a case, the $\overline{\text{ERROR}}$ output of the 80C187 is activated immediately.

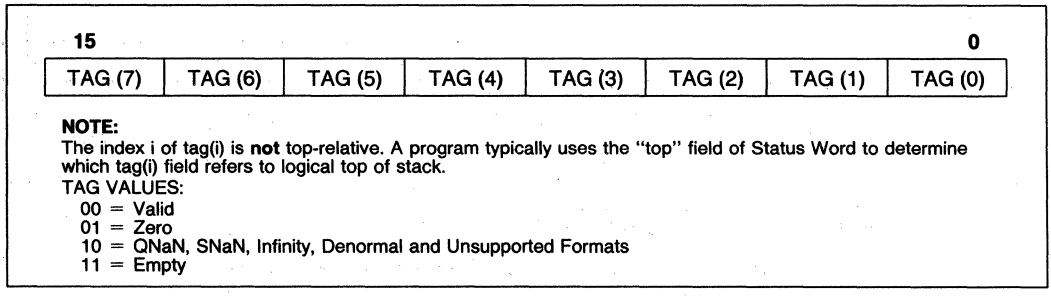
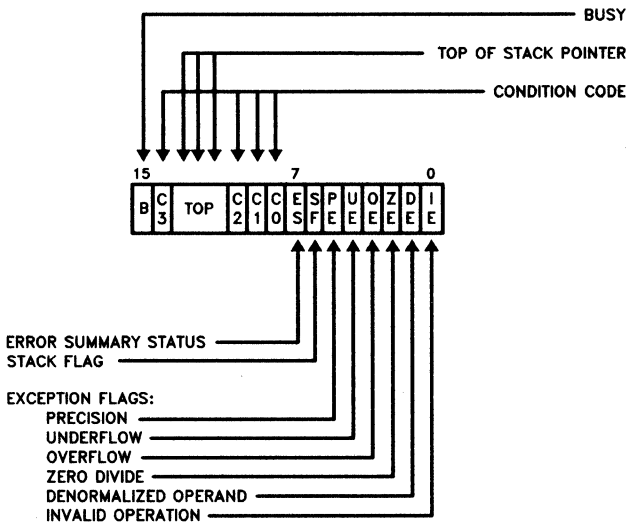


Figure 3. Tag Word



ES is set if any unmasked exception bit is set; cleared otherwise.
See Table 2 for interpretation of condition code.
TOP values:
000 = Register 0 is Top of Stack
001 = Register 1 is Top of Stack
•
•
•
111 = Register 7 is Top of Stack
For definitions of exceptions, refer to the section entitled, "Exception Handling"

Figure 4. Status Word

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CONTROL WORD

The NPX provides several processing options that are selected by loading a control word from memory into the control register. Figure 5 shows the format and encoding of fields in the control word.

Table 2. Condition Code Interpretation

Instruction	C0(S)	C3(Z)	C1(A)	C2(C)
FPREM, FPREM1 (See Table 3)	Three Least Significant Bits of Quotient Q2 Q0		Q1 or O/$\overline{U}$	Reduction 0 = Complete 1 = Incomplete
FCOM, FCOMP, FCOMPP, FTST FUCOM, FUCOMP, FUCOMPP, FICOM, FICOMP	Result of Comparison (See Table 4)		Zero or O/$\overline{U}$	Operand is not Comparable (Table 4)
FXAM	Operand Class (See Table 5)		Sign or O/$\overline{U}$	Operand Class (Table 5)
FCHS, FABS, FXCH, FINCSTP, FDECSTP, Constant Loads, FXTRACT, FLD, FILD, FBLD, FSTP (Ext Real)	UNDEFINED		Zero or O/$\overline{U}$	UNDEFINED
FIST, FBSTP, FRNDINT, FST, FSTP, FADD, FMUL, FDIV, FDIVR, FSUB, FSUBR, FSCALE, FSQRT, FPATAN, F2XM1, FYL2X, FYL2XP1	UNDEFINED		Roundup or O/$\overline{U}$	UNDEFINED
FPTAN, FSIN, FCOS, FSINCOS	UNDEFINED		Roundup or O/$\overline{U}$, Undefined if C2 = 1	Reduction 0 = Complete 1 = Incomplete
FLDENV, FRSTOR	Each Bit Loaded from Memory			
FLDCW, FSTENV, FSTCW, FSTSW, FCLEX, FINIT, FSAVE	UNDEFINED			

O/$\overline{U}$ When both IE and SF bits of status word are set, indicating a stack exception, this bit distinguishes between stack overflow (C1 = 1) and underflow (C1 = 0).

Reduction If FPREM or FPREM1 produces a remainder that is less than the modulus, reduction is complete. When reduction is incomplete the value at the top of the stack is a partial remainder, which can be used as input to further reduction. For FPTAN, FSIN, FCOS, and FSINCOS, the reduction bit is set if the operand at the top of the stack is too large. In this case the original operand remains at the top of the stack.

Roundup When the PE bit of the status word is set, this bit indicates whether one was added to the least significant bit of the result during the last rounding.

UNDEFINED Do not rely on finding any specific value in these bits.

The low-order byte of this control word configures exception masking. Bits 5–0 of the control word contain individual masks for each of the six exceptions that the 80C187 recognizes.

The high-order byte of the control word configures the 80C187 operating mode, including precision, rounding, and infinity control.

- The "infinity control bit" (bit 12) is not meaningful to the 80C187, and programs must ignore its value. To maintain compatibility with the 8087, this bit can be programmed; however, regardless of its value, the 80C187 always treats infinity in the affine sense ($-\infty < +\infty$). This bit is initialized to zero both after a hardware reset and after the FINIT instruction.
- The rounding control (RC) bits (bits 11–10) provide for directed rounding and true chop, as well as the unbiased round to nearest even mode specified in the IEEE standard. Rounding control affects only those instructions that perform rounding at the end of the operation (and thus can generate a precision exception); namely, FST, FSTP, FIST, all arithmetic instructions (except FPREM, FPREM1, FXTRACT, FABS, and FCHS), and all transcendental instructions.
- The precision control (PC) bits (bits 9–8) can be used to set the 80C187 internal operating precision of the significand at less than the default of 64 bits (extended precision). This can be useful in providing compatibility with early generation arithmetic processors of smaller precision. PC affects only the instructions ADD, SUB, DIV, MUL, and SQRT. For all other instructions, either the precision is determined by the opcode or extended precision is used.

Table 3. Condition Code Interpretation after FPREM and FPREM1 Instructions

Condition Code				Interpretation after FPREM and FPREM1	
C2	C3	C1	C0		
1	X	X	X	Incomplete Reduction: Further Iteration Required for Complete Reduction	
0	Q1	Q0	Q2	Q MOD 8	Complete Reduction: C0, C3, C1 Contain Three Least Significant Bits of Quotient
	0	0	0	0	
	0	1	0	1	
	1	0	0	2	
	1	1	0	3	
	0	0	1	4	
	0	1	1	5	
	1	0	1	6	
	1	1	1	7	

Table 4. Condition Code Resulting from Comparison

Order	C3	C2	C0
TOP > Operand	0	0	0
TOP < Operand	0	0	1
TOP = Operand	1	0	0
Unordered	1	1	1

Table 5. Condition Code Defining Operand Class

C3	C2	C1	C0	Value at TOP
0	0	0	0	+ Unsupported
0	0	0	1	+ NaN
0	0	1	0	− Unsupported
0	0	1	1	− NaN
0	1	0	0	+ Normal
0	1	0	1	+ Infinity
0	1	1	0	− Normal
0	1	1	1	− Infinity
1	0	0	0	+ 0
1	0	0	1	+ Empty
1	0	1	0	− 0
1	0	1	1	− Empty
1	1	0	0	+ Denormal
1	1	1	1	− Denormal

INSTRUCTION AND DATA POINTERS

Because the NPX operates in parallel with the CPU, any exceptions detected by the NPX may be reported after the CPU has executed the ESC instruction which caused it. To allow identification of the failing numerics instruction, the 80C187 contains registers that aid in diagnosis. These registers supply the opcode of the failing numerics instruction, the address of the instruction, and the address of its numerics memory operand (if appropriate).

The instruction and data pointers are provided for user-written exception handlers. Whenever the 80C187 executes a new ESC instruction, it saves the address of the instruction (including any prefixes that may be present), the address of the operand (if present), and the opcode.

The instruction and data pointers appear in the format shown by Figure 6. The ESC instruction FLDENV, FSTENV, FSAVE and FRSTOR are used to transfer these values between the registers and memory. Note that the value of the data pointer is *undefined* if the prior ESC instruction did not have a memory operand.

Interrupt Description

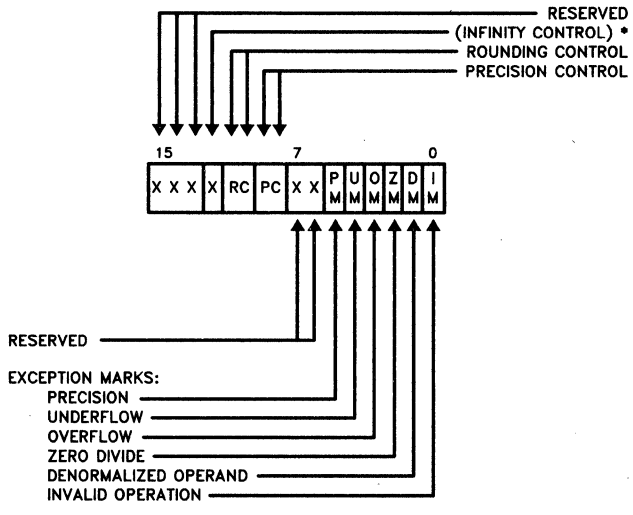
CPU interrupt 16 is used to report exceptional conditions while executing numeric programs. Interrupt 16 indicates that the previous numerics instruction caused an unmasked exception. The address of the faulty instruction and the address of its operand are stored in the instruction pointer and data pointer registers. Only ESC instructions can cause this interrupt. The CPU return address pushed onto the stack of the exception handler points to an ESC instruction (including prefixes). This instruction can be restarted after clearing the exception condition in the NPX. FNINIT, FNCLEX, FNSTSW, FNSTENV, and FNSAVE cannot cause this interrupt.

Exception Handling

The 80C187 detects six different exception conditions that can occur during instruction execution. Table 6 lists the exception conditions in order of precedence, showing for each the cause and the default action taken by the 80C187 if the exception is masked by its corresponding mask bit in the control word.

Any exception that is not masked by the control word sets the corresponding exception flag of the status word, sets the ES bit of the status word, and asserts the $\overline{\text{ERROR}}$ signal. When the CPU attempts to execute another ESC instruction, interrupt 16 occurs. The exception condition must be resolved via an interrupt service routine. The return address pushed onto the CPU stack upon entry to the service routine does not necessarily point to the failing instruction nor to the following instruction. The 80C187 saves the address of the floating-point instruction that caused the exception and the address of any memory operand required by that instruction.

If error trapping is required at the end of a series of numerics instructions (specifically, when the last ESC instruction modifies memory data and that data is used in subsequent nonnumerics instructions), it is necessary to insert the FNOP instruction to force the 80C187 to check its $\overline{\text{ERROR}}$ input.



Precision Control
00— 24 Bits (Single Precision)
01— (Reserved)
10— 53 Bits (Double Precision)
11— 64 Bits (Extended Precision)

Rounding Control
00— Round to Nearest or Even
01— Round Down (toward $-\infty$)
10— Round Up (toward $+\infty$)
11— Chop (Truncate toward Zero)

*The "infinity control" bit is not meaningful to the 80C187. To maintain compatibility with the 8087, this bit can be programmed; however, regardless of its value, the 80C187 treats infinity in the affine sense ($-\infty < +\infty$).

Figure 5. Control Word

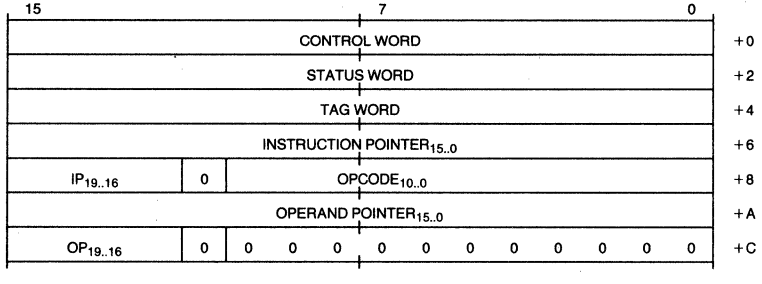


Figure 6. Instruction and Data Pointer Image in Memory

Table 6. Exceptions

Exception	Cause	Default Action (If Exception is Masked)
Invalid Operation	Operation on a signalling NaN, unsupported format, indeterminate form (0*∞, 0/0), (+∞) + (−∞), etc.), or stack overflow/underflow (SF is also set)	Result is a quiet NaN, integer indefinite, or BCD indefinite
Denormalized Operand	At least one of the operands is denormalized, i.e. it has the smallest exponent but a nonzero significand	The operand is normalized, and normal processing continues
Zero Divisor	The divisor is zero while the dividend is a noninfinite, nonzero number	Result is ∞
Overflow	The result is too large in magnitude to fit in the specified format	Result is largest finite value or ∞
Underflow	The true result is nonzero but too small to be represented in the specified format, and, if underflow exception is masked, denormalization causes loss of accuracy	Result is denormalized or zero
Inexact Result (Precision)	The true result is not exactly representable in the specified format (e.g. 1/3); the result is rounded according to the rounding mode	Normal processing continues

Initialization

After FNINIT or RESET, the control word contains the value 037FH (all exceptions masked, precision control 64 bits, rounding to nearest) the same values as in an 8087 after RESET. For compatibility with the 8087, the bit that used to indicate infinity control (bit 12) is set to zero; however, regardless of its setting, infinity is treated in the affine sense. After FNINIT or RESET, the status word is initialized as follows:

- All exceptions are set to zero.
- Stack TOP is zero, so that after the first push the stack top will be register seven (111B).
- The condition code C_3–C_0 is **undefined**.
- The B-bit is zero.

The tag word contains FFFFH (all stack locations are empty).

80C186/80C187 initialization software should execute an FNINIT instruction (i.e. an FINIT without a preceding WAIT) after RESET. The FNINIT is not strictly required for 80C187 software, but Intel recommends its use to help ensure upward compatibility with other processors.

8087 Compatibility

This section summarizes the differences between the 80C187 and the 8087. Many changes have been designed into the 80C187 to directly support the IEEE standard in hardware. These changes result in increased performance by elminating the need for software that supports the standard.

GENERAL DIFFERENCES

The 8087 instructions FENI/FNENI and FDISI/FNDISI perform no useful function in the 80C187 Numeric Processor Extension. They do not alter the state of the 80C187 Numeric Processor Extension. (They are treated similarly to FNOP, except that ERROR is not checked.) While 8086/8087 code containing these instructions can be executed on the 80C186/80C187, it is unlikely that the exception-handling routines containing these instructions will be completely portable to the 80C187 Numeric Processor Extension.

The 80C187 differs from the 8087 with respect to instruction, data, and exception synchronization. Except for the processor control instructions, all of the 80C187 numeric instructions are automatically synchronized by the 80C186 CPU. When necessary, the

80C186 automatically tests the BUSY line from the 80C187 Numeric Processor Extension to ensure that the 80C187 Numeric Processor Extension has completed its previous instruction before executing the next ESC instruction. No explicit WAIT instructions are required to assure this synchronization. For the 8087 used with 8086 and 8088 CPUs, explicit WAITs are required before each numeric instruction to ensure synchronization. Although 8086/8087 programs having explicit WAIT instructions will execute on the 80C186/80C187, these WAIT instructions are unnecessary.

The 80C187 supports only affine closure for infinity arithmetic, not projective closure.

Operands for FSCALE and FPATAN are no longer restricted in range (except for $\pm\infty$); F2XM1 and FPTAN accept a wider range of operands.

Rounding control is in effect for FLD *constant*.

Software cannot change entries of the tag word to values (other than empty) that differ from actual register contents.

After reset, FINIT, and incomplete FPREM, the 80C187 resets to zero the condition code bits C_3–C_0 of the status word.

In conformance with the IEEE standard, the 80C187 does not support the special data formats pseudozero, pseudo-NaN, pseudoinfinity, and unnormal.

The denormal exception has a different purpose on the 80C187. A system that uses the denormal-exception handler solely to normalize the denormal operands, would better mask the denormal exception on the 80C187. The 80C187 automatically normalizes denormal operands when the denormal exception is masked.

EXCEPTIONS

A number of differences exist due to changes in the IEEE standard and to functional improvements to the architecture of the 80C186/80C187:

1. The 80C186/80C187 traps exceptions only on the next ESC instruction; i.e. the 80C186 does not notice unmasked 80C187 exceptions on the 80C186 $\overline{\text{ERROR}}$ input line until a later numerics instruction is executed. Because the 80C186 does not sample $\overline{\text{ERROR}}$ on WAIT and FWAIT instructions, programmers should place an FNOP instruction at the end of a sequence of numerics instructions to force the 80C186 to sample its $\overline{\text{ERROR}}$ input.
2. The 80C187 Numeric Processor Extension signals exceptions through a dedicated $\overline{\text{ERROR}}$ line to the CPU. The 80C187 error signal does not pass through an interrupt controller (the 8087 INT signal does). Therefore, any interrupt-controller-oriented instructions in numerics exception handlers for the 8086/8087 should be deleted.
3. Interrupt vector 16 must point to the numerics exception handling routine.
4. The ESC instruction address saved in the 80C187 Numeric Processor Extension includes any leading prefixes before the ESC opcode. The corresponding address saved in the 8087 does not include leading prefixes.
5. When the overflow or underflow exception is masked, the 80C187 differs from the 8087 in rounding when overflow or underflow occurs. The 80C187 produces results that are consistent with the rounding mode.
6. When the underflow exception is masked, the 80C187 sets its underflow flag only if there is also a loss of accuracy during denormalization.
7. Fewer invalid-operation exceptions due to denormal operands, because the instructions FSQRT, FDIV, FPREM, and conversions to BCD or to integer normalize denormal operands before proceeding.
8. The FSQRT, FBSTP, and FPREM instructions may cause underflow, because they support denormal operands.
9. The denormal exception can occur during the transcendental instructions and the FXTRACT instruction.
10. The denormal exception no longer takes precedence over all other exceptions.
11. When the denormal exception is masked, the 80C187 automatically normalizes denormal operands. The 8087 performs unnormal arithmetic, which might produce an unnormal result.
12. When the operand is zero, the FXTRACT instruction reports a zero-divide exception and leaves $-\infty$ in ST(1).
13. The status word has a new bit (SF) that signals when invalid-operation exceptions are due to stack underflow or overflow.
14. FLD *extended precision* no longer reports denormal exceptions, because the instruction is not numeric.
15. FLD *single/double precision* when the operand is denormal converts the number to extended precision and signals the denormalized oper-

and exception. When loading a signalling NaN, FLD *single/double precision* signals an invalid-operand exception.

16. The 80C187 only generates quiet NaNs (as on the 8087); however, the 80C187 distinguishes between quiet NaNs and signalling NaNs. Signalling NaNs trigger exceptions when they are used as operands; quiet NaNs do not (except for FCOM, FIST, and FBSTP which also raise IE for quiet NaNs).
17. When stack overflow occurs during FPTAN and overflow is masked, both ST(0) and ST(1) contain quiet NaNs. The 8087 leaves the original operand in ST(1) intact.
18. When the scaling factor is $\pm\infty$, the FSCALE (ST(0), ST(1) instruction behaves as follows (ST(0) and ST(1) contain the scaled and scaling operands respectively):
    - FSCALE (0, ∞) generates the invalid operation exception.
    - FSCALE (finite, $-\infty$) generates zero with the same sign as the scaled operand.
    - FSCALE (finite, $+\infty$) generates ∞ with the same sign as the scaled operand.

    The 8087 returns zero in the first case and raises the invalid-operation exception in the other cases.
19. The 80C187 returns signed infinity/zero as the unmasked response to massive overflow/underflow. The 8087 supports a limited range for the scaling factor; within this range either massive overflow/underflow do not occur or undefined results are produced.

Table 7. Pin Summary

Pin Name	Function	Active State	Input/ Output
CLK	CLocK		I
CKM	ClocKing Mode		I
RESET	System reset	High	I
PEREQ	Processor Extension REQuest	High	O
BUSY	Busy status	High	O
$\overline{\text{ERROR}}$	Error status	Low	O
D_{15}–D_0	Data pins	High	I/O
$\overline{\text{NPRD}}$	Numeric Processor ReaD	Low	I
$\overline{\text{NPWR}}$	Numeric Processor WRite	Low	I
$\overline{\text{NPS1}}$	NPX select #1	Low	I
NPS2	NPX select #2	High	I
CMD0	CoMmanD 0	High	I
CMD1	CoMmanD 1	High	I
V_{CC}	System power		I
V_{SS}	System ground		I

HARDWARE INTERFACE

In the following description of hardware interface, an overbar above a signal name indicates that the active or asserted state occurs when the signal is at a low voltage. When no overbar is present above the signal name, the signal is asserted when at the high voltage level.

Signal Description

In the following signal descriptions, the 80C187 pins are grouped by function as follows:

1. Execution Control— CLK, CKM, RESET
2. NPX Handshake— PEREQ, BUSY, $\overline{\text{ERROR}}$
3. Bus Interface Pins— D_{15}–D_0, $\overline{\text{NPWR}}$, $\overline{\text{NPRD}}$
4. Chip/Port Select— $\overline{\text{NPS1}}$, NPS2, CMD0, CMD1
5. Power Supplies— V_{CC}, V_{SS}

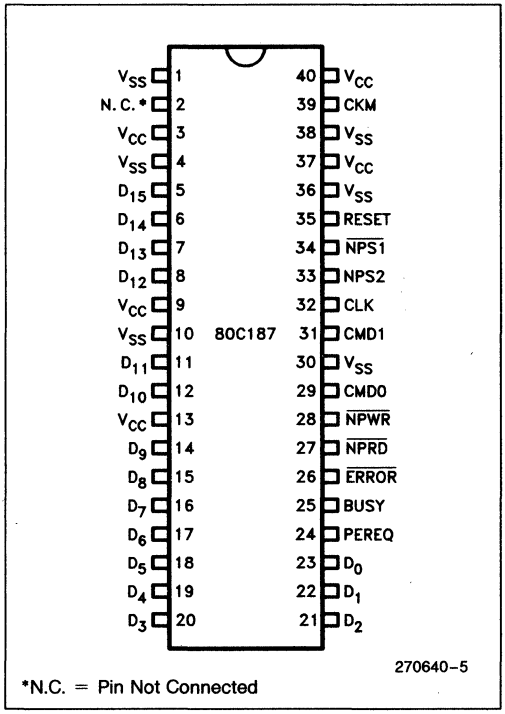
Table 7 lists every pin by its identifier, gives a brief description of its function, and lists some of its characteristics. Figure 7 shows the locations of pins on the CERDIP package, while Figure 8 shows the locations of pins on the PLCC package. Table 8 helps to locate pin identifiers in Figures 7 and 8.

Clock (CLK)

This input provides the basic timing for internal operation. This pin does not require MOS-level input; it will operate at either TTL or MOS levels up to the maximum allowed frequency. A minimum frequency must be provided to keep the internal logic properly functioning. Depending on the signal on CKM, the signal on CLK can be divided by two to produce the internal clock signal (in which case CLK may be up to 32 MHz in frequency), or can be used directly (in which case CLK may be up to 12.5 MHz).

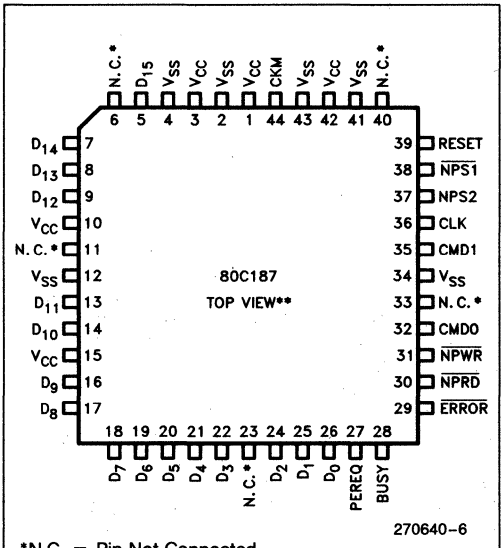
Clocking Mode (CKM)

This pin is a strapping option. When it is strapped to V_{CC} (HIGH), the CLK input is used directly; when strapped to V_{SS} (LOW), the CLK input is divided by two to produce the internal clock signal. During the RESET sequence, this input must be stable at least four internal clock cycles (i.e. CLK clocks when CKM is HIGH; 2 × CLK clocks when CKM is LOW) before RESET goes LOW.



*N.C. = Pin Not Connected

Figure 7. CERDIP Pin Configuration



*N.C. = Pin Not Connected

**"Top View" means as the package is seen from the component side of the board.

Figure 8. PLCC Pin Configuration

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Table 8. PLCC Pin Cross-Reference

Pin Name	CERDIP Package	PLCC Package
BUSY	25	28
CKM	39	44
CLK	32	36
CMD0	29	32
CMD1	31	35
D_0	23	26
D_1	22	25
D_2	21	24
D_3	20	22
D_4	19	21
D_5	18	20
D_6	17	19
D_7	16	18
D_8	15	17
D_9	14	16
D_{10}	12	14
D_{11}	11	13
D_{12}	8	9
D_{13}	7	8
D_{14}	6	7
D_{15}	5	5
$\overline{\text{ERROR}}$	26	29
No Connect	2	6, 11, 23, 33, 40
$\overline{\text{NPRD}}$	27	30
$\overline{\text{NPS1}}$	34	38
NPS2	33	37
$\overline{\text{NPWR}}$	28	31
PEREQ	24	27
RESET	35	39
V_{CC}	3, 9, 13, 37, 40	1, 3, 10, 15, 42
V_{SS}	1, 4, 10, 30, 36, 38	2, 4, 12, 34, 41, 43

System Reset (RESET)

A LOW to HIGH transition on this pin causes the 80C187 to terminate its present activity and to enter a dormant state. RESET must remain active (HIGH) for at least four internal clock periods. (The relation of the internal clock period to CLK depends on CLKM; the internal clock may be different from that of the CPU.) Note that the 80C187 is active internally for 25 clock periods after the termination of the RESET signal (the HIGH to LOW transition of RESET); therefore, the first instruction should not be written to the 80C187 until 25 internal clocks after the falling edge of RESET. Table 9 shows the status of the output pins during the reset sequence. After a reset, all output pins return to their inactive states.

Table 9. Output Pin Status during Reset

Output Pin Name	Value during Reset
BUSY	HIGH
$\overline{\text{ERROR}}$	HIGH
PEREQ	LOW
D_{15}–D_0	TRI-STATE OFF

Processor Extension Request (PEREQ)

When active, this pin signals to the CPU that the 80C187 is ready for data transfer to/from its data FIFO. When there are more than five data transfers,

PEREQ is deactivated after the first three transfers and subsequently after every four transfers. This signal always goes inactive before BUSY goes inactive.

Busy Status (BUSY)

When active, this pin signals to the CPU that the 80C187 is currently executing an instruction. This pin is active HIGH. It should be connected to the 80C186's $\overline{TEST}$/BUSY pin. During the RESET sequence this pin is HIGH. The 80C186 uses this HIGH state to detect the presence of an 80C187.

Error Status ($\overline{ERROR}$)

This pin reflects the ES bit of the status register. When active, it indicates that an unmasked exception has occurred. This signal can be changed to inactive state only by the following instructions (without a preceding WAIT): FNINIT, FNCLEX, FNSTENV, FNSAVE, FLDCW, FLDENV, and FRSTOR. This pin should be connected to the $\overline{ERROR}$ pin of the CPU. $\overline{ERROR}$ can change state only when BUSY is active.

Data Pins (D_{15}-D_0)

These bidirectional pins are used to transfer data and opcodes between the CPU and 80C187. They are normally connected directly to the corresponding CPU data pins. Other buffers/drivers driving the local data bus must be disabled when the CPU reads from the NPX. High state indicates a value of one. D_0 is the least significant data bit.

Numeric Processor Write ($\overline{NPWR}$)

A signal on this pin enables transfers of data from the CPU to the NPX. This input is valid only when $\overline{NPS1}$ and NPS2 are both active.

Numeric Processor Read ($\overline{NPRD}$)

A signal on this pin enables transfers of data from the NPX to the CPU. This input is valid only when $\overline{NPS1}$ and NPS2 are both active.

Numeric Processor Selects ($\overline{NPS1}$ and NPS2)

Concurrent assertion of these signals indicates that the CPU is performing an escape instruction and enables the 80C187 to execute that instruction. No data transfer involving the 80C187 occurs unless the device is selected by these lines.

Command Selects (CMD0 and CMD1)

These pins along with the select pins allow the CPU to direct the operation of the 80C187.

System Power (V_{CC})

System power provides the +5V ±10% DC supply input. All V_{CC} pins should be tied together on the circuit board and local decoupling capacitors should be used between V_{CC} and V_{SS}.

System Ground (V_{SS})

All V_{SS} pins should be tied together on the circuit board and local decoupling capacitors should be used between V_{CC} and V_{SS}.

Processor Architecture

As shown by the block diagram (Figure 1), the 80C187 NPX is internally divided into three sections: the bus control logic (BCL), the data interface and control unit, and the floating-point unit (FPU). The FPU (with the support of the control unit which contains the sequencer and other support units) executes all numerics instructions. The data interface and control unit is responsible for the data flow to and from the FPU and the control registers, for receiving the instructions, decoding them, and sequencing the microinstructions, and for handling some of the administrative instructions. The BCL is responsible for CPU bus tracking and interface.

BUS CONTROL LOGIC

The BCL communicates solely with the CPU using I/O bus cycles. The BCL appears to the CPU as a special peripheral device. It is special in two respects: the CPU initiates I/O automatically when it encounters ESC instructions, and the CPU uses reserved I/O addresses to communicate with the BCL. The BCL does not communicate directly with memory. The CPU performs all memory access, transferring input operands from memory to the 80C187 and transferring outputs from the 80C187 to memory. A dedicated communication protocol makes possible high-speed transfer of opcodes and operands between the CPU and 80C187.

Table 10. Bus Cycles Definition

$\overline{NPS1}$	NPS2	CMD0	CMD1	$\overline{NPRD}$	$\overline{NPWR}$	Bus Cycle Type
x	0	x	x	x	x	80C187 Not Selected
1	x	x	x	x	x	80C187 Not Selected
0	1	0	0	1	0	Opcode Write to 80C187
0	1	0	0	0	1	CW or SW Read from 80C187
0	1	1	0	0	1	Read Data from 80C187
0	1	1	0	1	0	Write Data to 80C187
0	1	0	1	1	0	Write Exception Pointers
0	1	0	1	0	1	Reserved
0	1	1	1	0	1	Read Opcode Status
0	1	1	1	1	0	Reserved

DATA INTERFACE AND CONTROL UNIT

The data interface and control unit latches the data and, subject to BCL control, directs the data to the FIFO or the instruction decoder. The instruction decoder decodes the ESC instructions sent to it by the CPU and generates controls that direct the data flow in the FIFO. It also triggers the microinstruction sequencer that controls execution of each instruction. If the ESC instruction is FINIT, FCLEX, FSTSW, FSTSW AX, FSTCW, FSETPM, or FRSTPM, the control executes it independently of the FPU and the sequencer. The data interface and control unit is the one that generates the BUSY, PEREQ, and $\overline{ERROR}$ signals that synchronize 80C187 activities with the CPU.

FLOATING-POINT UNIT

The FPU executes all instructions that involve the register stack, including arithmetic, logical, transcendental, constant, and data transfer instructions. The data path in the FPU is 84 bits wide (68 significant bits, 15 exponent bits, and a sign bit) which allows internal operand transfers to be performed at very high speeds.

Bus Cycles

The pins $\overline{NPS1}$, NPS2, CMD0, CMD1, $\overline{NPRD}$ and $\overline{NPWR}$ identify bus cycles for the NPX. Table 10 defines the types of 80C187 bus cycles.

80C187 ADDRESSING

The $\overline{NPS1}$, NPS2, CMD0, and CMD1 signals allow the NPX to identify which bus cycles are intended for the NPX. The NPX responds to I/O cycles when the I/O address is 00F8H, 00FAH, 00FCH, or 00FEH. The correspondence betwen I/O addresses and control signals is defined by Table 11. To guarantee correct operation of the NPX, programs must not perform any I/O operations to these reserved port addresses.

Table 11. I/O Address Decoding

I/O Address (Hexadecimal)	80C187 Select and Command Inputs			
	NPS2	$\overline{NPS1}$	CMD1	CMD0
00F8	1	0	0	0
00FA	1	0	0	1
00FC	1	0	1	0
00FE	1	0	1	1

CPU/NPX SYNCHRONIZATION

The pins BUSY, PEREQ, and $\overline{\text{ERROR}}$ are used for various aspects of synchronization between the CPU and the NPX.

BUSY is used to synchronize instruction transfer from the CPU to the 80C187. When the 80C187 recognizes an ESC instruction, it asserts BUSY. For most ESC instructions, the CPU waits for the 80C187 to deassert BUSY before sending the new opcode.

The NPX uses the PEREQ pin of the CPU to signal that the NPX is ready for data transfer to or from its data FIFO. The NPX does not directly access memory; rather, the CPU provides memory access services for the NPX.

Once the CPU initiates an 80C187 instruction that has operands, the CPU waits for PEREQ signals that indicate when the 80C187 is ready for operand transfer. Once all operands have been transferred (or if the instruction has no operands) the CPU continues program execution while the 80C187 executes the ESC instruction.

In 8086/8087 systems, WAIT instructions are required to achieve synchronization of both commands and operands. The 80C187, however, does not require WAIT instructions. The WAIT or FWAIT instruction commonly inserted by high-level compilers and assembly-language programmers for exception synchronization is not treated as an instruction by the 80C186 and does not provide exception trapping. (Refer to the section "System Configuration for 8087-Compatible Exception Trapping".)

Once it has started to execute a numerics instruction and has transferred the operands from the CPU, the 80C187 can process the instruction in parallel with and independent of the host CPU. When the NPX detects an exception, it asserts the $\overline{\text{ERROR}}$ signal, which causes a CPU interrupt.

OPCODE INTERPRETATION

The CPU and the NPX use a bus protocol that adapts to the numerics opcode being executed. Only the NPX directly interprets the opcode. Some of the results of this interpretation are relevant to the CPU. The NPX records these results (opcode status information) in an internal 16-bit register. The 80C186 accesses this register only via reads from NPX port 00FEH. Tables 10 and 11 define the signal combinations that correspond to each of the following steps.

1. The CPU writes the opcode to NPX port 00F8H. This write can occur even when the NPX is busy or is signalling an exception. The NPX does not necessarily begin executing the opcode immediately.
2. The CPU reads the opcode status information from NPX port 00FEH.
3. The CPU initiates subsequent bus cycles according to the opcode status information. The opcode status information specifies whether to wait until the NPX is not busy, when to transfer exception pointers to port 00FCH, when to read or write operands and results at port 00FAH, etc.

For most instructions, the NPX does not start executing the previously transferred opcode until the CPU (guided by the opcode status information) first writes exception pointer information to port 00FCH of the NPX. This protocol is completely transparent to programmers.

Bus Operation

With respect to bus interface, the 80C187 is fully asynchronous with the CPU, even when it operates from the same clock source as the CPU. The CPU initiates a bus cycle for the NPX by activating both $\overline{\text{NPS1}}$ and NPS2, the NPX select signals. During the CLK period in which $\overline{\text{NPS1}}$ and NPS2 are activated, the 80C187 also examines the $\overline{\text{NPRD}}$ and $\overline{\text{NPRW}}$

input signals to determine whether the cycle is a read or a write cycle and examines the CMD0 and CMD1 inputs to determine whether an opcode, operand, or control/status register transfer is to occur. The 80C187 activates its BUSY output some time after the leading edge of the $\overline{NPRD}$ or $\overline{NPRW}$ signal. Input and ouput data are referenced to the trailing edges of the $\overline{NPRD}$ and $\overline{NPRW}$ signals.

The 80C187 activates the PEREQ signal when it is ready for data transfer. The 80C187 deactivates PEREQ automatically.

System Configuration

The 80C187 can be connected to the 80C186 CPU as shown by Figure 9. (Refer to the 80C186 Data Sheet for an explanation of the 80C186's signals.) This interface has the following characteristics:

- The 80C187's $\overline{NPS1}$, $\overline{ERROR}$, PEREQ, and BUSY pins are connected directly to the corresponding pins of the 80C186.
- The 80C186 pin $\overline{MCS3}/\overline{NPS}$ is connected to $\overline{NPS1}$; NPS2 is connected to V_{CC}. Note that if the 80C186 CPU's $\overline{DEN}$ signal is used to gate external data buffers, it must be combined with the $\overline{NPS}$ signal to insure numeric accesses will not activate these buffers.
- The $\overline{NPRD}$ and $\overline{NPRW}$ pins are connected to the $\overline{RD}$ and $\overline{WR}$ pins of the 80C186.
- CMD1 and CMD0 come from the latched A_2 and A_1 of the 80C186, respectively.
- The 80C187 BUSY output connects to the 80C186 $\overline{TEST}$/BUSY input. During RESET, the signal at the 80C187 BUSY output automatically programs the 80C186 to use the 80C187.
- The 80C187 can use the CLKOUT signal of the 80C186 to conserve board space when operating at 12.5 MHz or less. In this case, the 80C187 CKM input must be pulled HIGH. For operation in excess of 12.5 MHz, a double-frequency external oscillator for CLK input is needed. In this case, CKM must be pulled LOW.

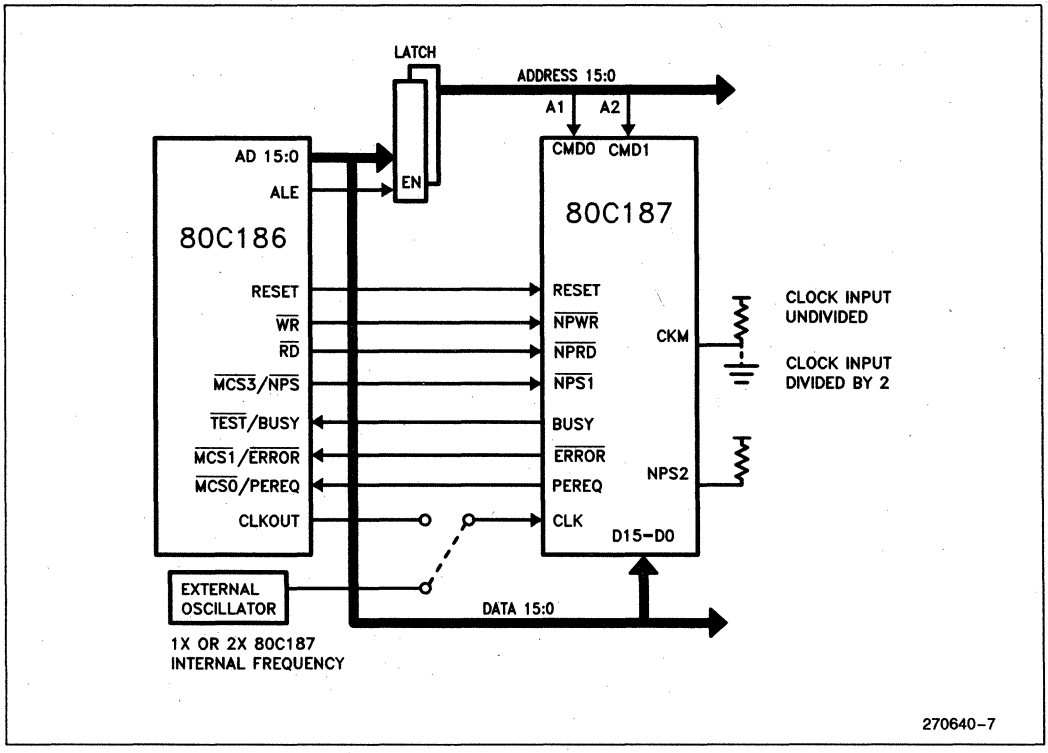
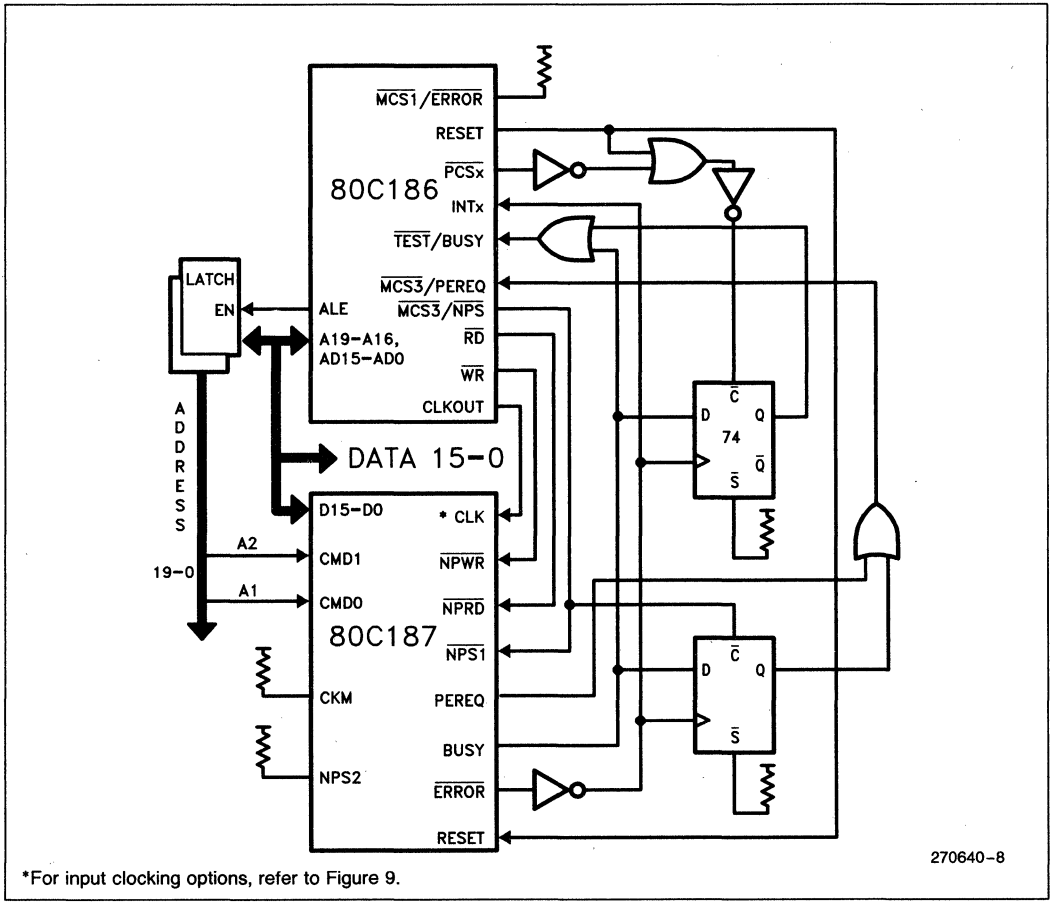


Figure 9. 80C186/80C187 System Configuration

System Configuration for 80186/ 80187-Compatible Exception Trapping

When the 80C187 $\overline{\text{ERROR}}$ output signal is connected directly to the 80C186 $\overline{\text{ERROR}}$ input, floating-point exceptions cause interrupt #16. However, existing software may be programmed to expect floating-point exceptions to be signalled over an external interrupt pin via an interrupt controller.

For exception handling compatible with the 80186/ 82188/8087, the 80C186 can be wired to recognize exceptions through an external interrupt pin, as Figure 10 shows. (Refer to the 80C186 Data Sheet for an explanation of the 80C186's signals.) With this arrangement, a flip-flop is needed to latch BUSY upon assertion of $\overline{\text{ERROR}}$. The latch can then be cleared during the exception-handler routine by forcing a $\overline{\text{PCS}}$ pin active. The latch must also be cleared at RESET in order for the 80C186 to work with the 80C187.



*For input clocking options, refer to Figure 9.

Figure 10. System Configuration for 8087-Compatible Exception Trapping

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ELECTRICAL DATA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

Absolute Maximum Ratings*

Case Temperature Under Bias (T_C) . . . 0°C to +85°C

Storage Temperature . . . . . −65°C to +150°C

Voltage on Any Pin with Respect to Ground . . . . −0.5V to V_{CC} +0.5V

Power Dissipation 1.5W

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Power and Frequency Requirements

The typical relationship between I_{CC} and the frequency of operation F is as follows:

$I_{CC_{typ}} = 55 + 5 \cdot F$ mA where F is in MHz.

When the frequency is reduced below the minimum operating frequency specified in the AC Characteristics table, the internal states of the 80C187 may become indeterminate. The 80C187 clock cannot be stopped; otherwise, I_{CC} would increase significantly beyond what the equation above indicates.

DC Characteristics T_C = 0°C to +85°C, V_{CC} = +5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input LOW Voltage	−0.5	+0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CC} +0.5	V	
V_{ICL}	Clock Input LOW Voltage	−0.5	+0.8	V	
V_{ICH}	Clock Input HIGH Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output LOW Voltage		0.45	V	I_{OL} = 3.0 mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −0.4 mA
I_{CC}	Power Supply Current		156 135	mA mA	16 MHz 12.5 MHz
I_{LI}	Input Leakage Current		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	I/O Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC} − 0.45V
C_{IN}	Input Capacitance		10	pF	F_C = 1 MHz
C_O	I/O or Output Capacitance		12	pF	F_C = 1 MHz
C_{CLK}	Clock Capacitance		20	pF	F_C = 1 MHz

AC Characteristics

T_C = 0°C to +85°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V unless otherwise specified

Symbol	Parameter	12.5 MHz		16 MHz		Test Conditions
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	
T_{dvwh} (t6)	Data Setup to $\overline{NPWR}$	43		33		
T_{whdx} (t7)	Data Hold from $\overline{NPWR}$	14		14		
T_{rlrh} (t8)	$\overline{NPRD}$ Active Time	59		54		
T_{wlwh} (t9)	$\overline{NPWR}$ Active Time	59		54		
T_{avwl} (t10)	Command Valid to $\overline{NPWR}$	0		0		
T_{avrl} (t11)	Command Valid to $\overline{NPRD}$	0		0		
T_{mhrl} (t12)	Min Delay from PEREQ Active to $\overline{NPRD}$ Active	40		30		
T_{whax} (t18)	Command Hold from $\overline{NPWR}$	12		8		
T_{rhax} (t19)	Command Hold from $\overline{NPRD}$	12		8		
T_{ivcl} (t20)	$\overline{NPRD}$, $\overline{NPWR}$, RESET to CLK Setup Time	46		38		Note 1
T_{clih} (t21)	$\overline{NPRD}$, $\overline{NPWR}$, RESET from CLK Hold Time	26		18		Note 1
T_{rscl} (t24)	RESET to CLK Setup	21		19		Note 1
T_{clrs} (t25)	RESET from CLK Hold	14		9		Note 1
T_{cmdi} (t26)	Command Inactive Time					
	Write to Write	69		59		
	Read to Read	69		59		
	Read to Write	69		59		
	Write to Read	69		59		

NOTE:
1. This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific CLK edge.

Timing Responses

All timings are measured at 1.5V unless otherwise specified

Symbol	Parameter	12.5 MHz		16 MHz		Test Conditions
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	
T_{rhqz} (t27)	$\overline{NPRD}$ Inactive to Data Float*		18		18	Note 2
T_{rlqv} (t28)	$\overline{NPRD}$ Active to Data Valid		50		45	Note 3
T_{ilbh} (t29)	$\overline{ERROR}$ Active to Busy Inactive	104		104		Note 4
T_{wlbv} (t30)	$\overline{NPWR}$ Active to Busy Active		80		60	Note 4
T_{klml} (t31)	$\overline{NPRD}$ or $\overline{NPWR}$ Active to PEREQ Inactive		80		60	Note 5
T_{rhqh} (t32)	Data Hold from $\overline{NPRD}$ Inactive	2		2		Note 3
T_{rlbh} (t33)	RESET Inactive to BUSY Inactive		80		60	

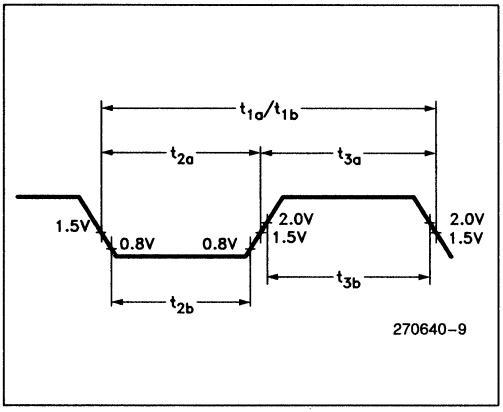
NOTES:
*The data float delay is not tested.
2. The float condition occurs when the measured output current is less than I_{OL} on D_{15}–D_0.
3. D_{15}–D_0 loading: C_L = 100 pF.
4. BUSY loading: C_L = 100 pF.
5. On last data transfer of numeric instruction.

Clock Timings

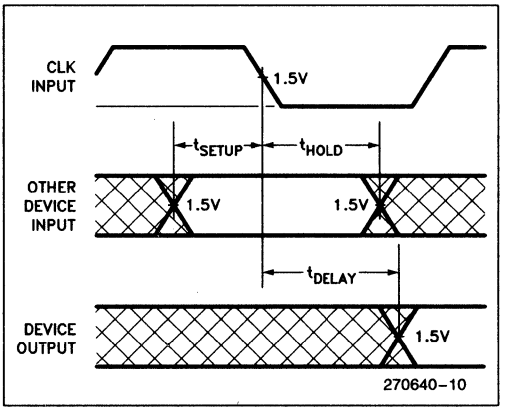
Symbol		Parameter		12.5 MHz		16 MHz*		Test Conditions
				Min (ns)	Max (ns)	Min (ns)	Max (ns)	
T_{clcl}	(t1a)	CLK Period	CKM = 1	80	250	N/A	N/A	Note 6
	(t1B)		CKM = 0	40	125	31.25	125	Note 6
T_{clch}	(t2a)	CLK Low Time	CKM = 1	35		N/A		Note 6
	(t2b)		CKM = 0	9		7		Note 7
T_{chcl}	(t3a)	CLK High Time	CKM = 1	35		N/A		Note 6
	(t3b)		CKM = 0	13		9		Note 8
T_{ch2ch1}	(t4)				10		8	Note 9
T_{ch1ch2}	(t5)				10		8	Note 10

NOTES:
*16 MHz operation is available only in divide-by-2 mode (CKM strapped LOW).
6. At 1.5V
7. At 0.8V
8. At 2.0V
9. CKM = 1: 3.7V to 0.8V at 16 MHz, 3.5V to 1.0V at 12.5 MHz
10. CKM = 1: 0.8V to 3.7V at 16 MHz, 1.0V to 3.5V at 12.5 MHz

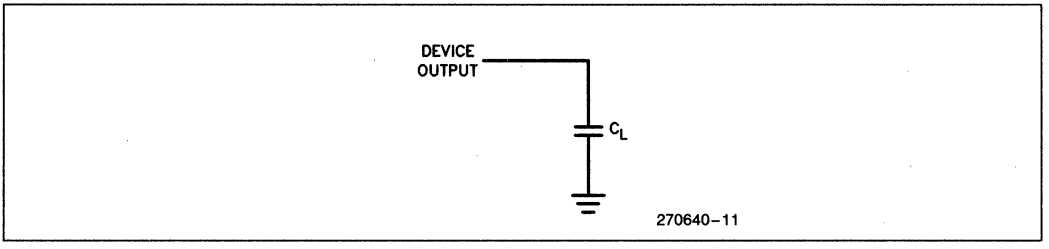
AC DRIVE AND MEASUREMENT POINTS—CLK INPUT



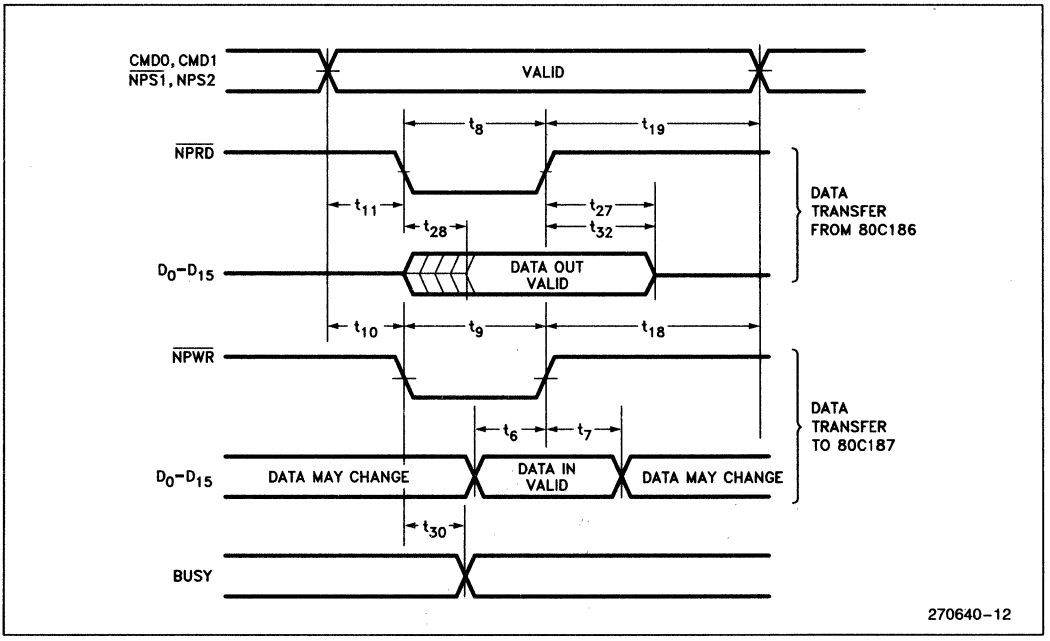
AC SETUP, HOLD, AND DELAY TIME MEASUREMENTS—GENERAL



AC TEST LOADING ON OUTPUTS



DATA TRANSFER TIMING (INITIATED BY CPU)



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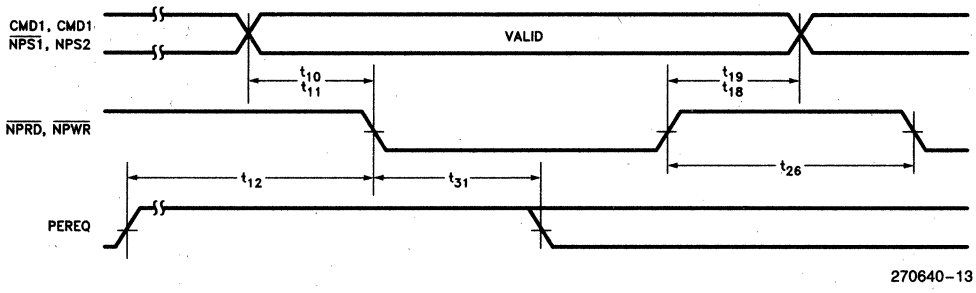
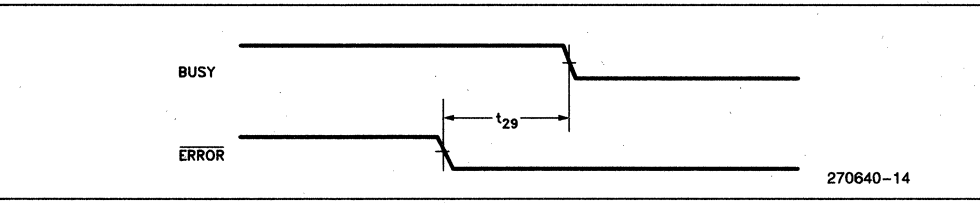
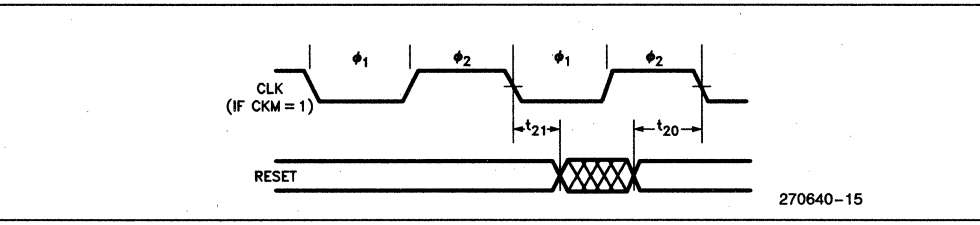
DATA CHANNEL TIMING (INITIATED BY 80C187)



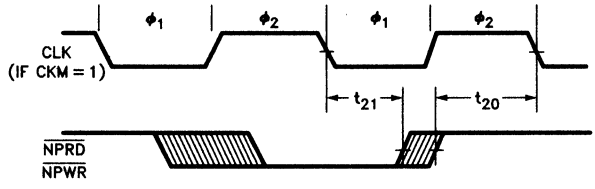
ERROR OUTPUT TIMING



CLK, RESET TIMING (CKM = 1)

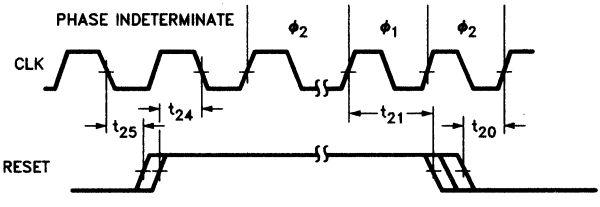


CLK, $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ TIMING (CKM = 1)



270640-16

CLK, RESET TIMING (CKM = 0)

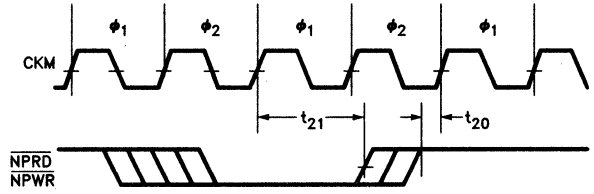


270640-17

RESET must meet timing shown to guarantee known phase of internal divide by 2 circuits.

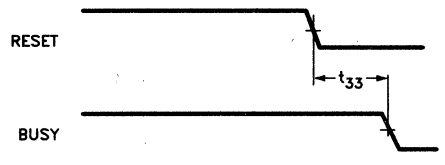
NOTE:
RESET, $\overline{\text{NPWR}}$, $\overline{\text{NPRD}}$ inputs are asynchronous to CLK. Timing requirements are given for testing purposes only, to assure recognition at a specific CLK edge.

CLK, $\overline{\text{NPRD}}$, $\overline{\text{NPWR}}$ TIMING (CKM = 0)



270640-18

RESET, BUSY TIMING



270640-19

80C187 EXTENSIONS TO THE CPU's INSTRUCTION SET

Instructions for the 80C187 assume one of the five forms shown in Table 12. In all cases, instructions are at least two bytes long and begin with the bit pattern 11011B, which identifies the ESCAPE class of instruction. Instructions that refer to memory operands specify addresses using the CPU's addressing modes.

MOD (Mode field) and R/M (Register/Memory specifier) have the same interpretation as the corresponding fields of CPU instructions (refer to Programmer's Reference Manual for the CPU). The DISP (displacement) is optionally present in instructions that have MOD and R/M fields. Its presence depends on the values of MOD and R/M, as for instructions of the CPU.

The instruction summaries that follow assume that the instruction has been prefetched, decoded, and is ready for execution; that bus cycles do not require wait states; that there are no local bus HOLD requests delaying processor access to the bus; and that no exceptions are detected during instruction execution. Timings are given in internal 80C187 clocks and include the time for opcode and data transfer between the CPU and the NPX. If the instruction has MOD and R/M fields that call for both base and index registers, add one clock.

Table 12. Instruction Formats

	Instruction									Optional Field
	First Byte				Second Byte					
1	11011	OPA		1	MOD		1	OPB	R/M	DISP
2	11011	MF		OPA	MOD		OPB *		R/M	DISP
3	11011	d	P	OPA	1	1	OPB *		ST (i)	
4	11011	0	0	1	1	1	1	OP		
5	11011	0	1	1	1	1	1	OP		
	15–11	10	9	8	7	6	5	4 3	2 1 0	

NOTES:
OP = Instruction opcode, possibly split into two fields OPA and OPB

MF = Memory Format
- 00— 32-Bit Real
- 01— 32-Bit Integer
- 10— 64-Bit Real
- 11— 16-Bit Integer

d = Destination
- 0— Destination is ST(0)
- 0— Destination is ST(i)

R XOR d = 0— Destination (op) Source
R XOR d = 1— Source (op) Destination

*In FSUB and FDIV, the low-order bit of OPB is the R (reversed) bit

P = Pop
- 0— Do not pop stack
- 1— Pop stack after operation

ESC = 11011

ST(i) = Register Stack Element i
- 000 = Stack Top
- 001 = Second Stack Element
- •
- •
- •
- 111 = Eighth Stack Element

80C187 Extensions to the 80C186 Instruction Set

Instruction	Encoding			Clock Count Range			
	Byte 0	Byte 1	Optional Bytes 2-3	32-Bit Real	32-Bit Integer	64-Bit Real	16-Bit Integer
DATA TRANSFER							
FLD = Load[a]							
Integer/real memory to ST(0)	ESC MF 1	MOD 000 R/M	DISP	40	65-72	59	67-71
Long integer memory to ST(0)	ESC 111	MOD 101 R/M	DISP		90-101		
Extended real memory to ST(0)	ESC 011	MOD 101 R/M	DISP		74		
BCD memory to ST(0)	ESC 111	MOD 100 R/M	DISP		296-305		
ST(i) to ST(0)	ESC 001	11000 ST(i)			16		
FST = Store							
ST(0) to integer/real memory	ESC MF 1	MOD 010 R/M	DISP	58	93-107	73	80-93
ST(0) to ST(i)	ESC 101	11010 ST(i)			13		
FSTP = Store and Pop							
ST(0) to integer/real memory	ESC MF 1	MOD 011 R/M	DISP	58	93-107	73	80-93
ST(0) to long integer memory	ESC 111	MOD 111 R/M	DISP		116-133		
ST(0) to extended real	ESC 011	MOD 111 R/M	DISP		83		
ST(0) to BCD memory	ESC 111	MOD 110 R/M	DISP		542-564		
ST(0) to ST(i)	ESC 101	11001 ST (i)			14		
FXCH = Exchange							
ST(i) and ST(0)	ESC 001	11001 ST(i)			20		
COMPARISON							
FCOM = Compare							
Integer/real memory to ST(0)	ESC MF 0	MOD 010 R/M	DISP	48	78-85	67	77-81
ST(i) to ST(0)	ESC 000	11010 ST(i)			26		
FCOMP = Compare and pop							
Integer/real memory to ST	ESC MF 0	MOD 011 R/M	DISP	48	78-85	67	77-81
ST(i) to ST(0)	ESC 000	11011 ST(i)			28		
FCOMPP = Compare and pop twice							
ST(1) to ST(0)	ESC 110	1101 1001			28		
FTST = Test ST(0)	ESC 001	1110 0100			30		
FUCOM = Unordered compare	ESC 101	11100 ST(i)			26		
FUCOMP = Unordered compare and pop	ESC 101	11101 ST(i)			28		
FUCOMPP = Unordered compare and pop twice	ESC 010	1110 1001			28		
FXAM = Examine ST(0)	ESC 001	11100101			32-40		
CONSTANTS							
FLDZ = Load +0.0 into ST(0)	ESC 001	1110 1110			22		
FLD1 = Load +1.0 into ST(0)	ESC 001	1110 1000			26		
FLDPI = Load pi into ST(0)	ESC 001	1110 1011			42		
FLDL2T = Load $\log_2(10)$ into ST(0)	ESC 001	1110 1001			42		

Shaded areas indicate instructions not available in 8087.

NOTE:
a. When loading single- or double-precision zero from memory, add 5 clocks.

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80C187 Extensions to the 80C186 Instruction Set (Continued)

Instruction	Encoding			Clock Count Range			
	Byte 0	Byte 1	Optional Bytes 2–3	32-Bit Real	32-Bit Integer	64-Bit Real	16-Bit Integer
CONSTANTS (Continued)							
FLDL2E = Load $\log_2(e)$ into ST(0)	ESC 001	1110 1010			42		
FLDLG2 = Load $\log_{10}(2)$ into ST(0)	ESC 001	1110 1100			43		
FLDLN2 = Load $\log_e(2)$ into ST(0)	ESC 001	1110 1101			43		
ARITHMETIC							
FADD = Add							
Integer/real memory with ST(0)	ESC MF 0	MOD 000 R/M	DISP	44–52	77–92	65–73	77–91
ST(i) and ST(0)	ESC d P 0	11000 ST(i)			25–33[b]		
FSUB = Subtract							
Integer/real memory with ST(0)	ESC MF 0	MOD 10 R R/M	DISP	44–52	77–92	65–73	77–91[c]
ST(i) and ST(0)	ESC d P 0	1110 R R/M			28–36[d]		
FMUL = Multiply							
Integer/real memory with ST(0)	ESC MF 0	MOD 001 R/M	DISP	47–57	81–102	68–93	82–93
ST(i) and ST(0)	ESC d P 0	1100 1 R/M			31–59[e]		
FDIV = Divide							
Integer/real memory with ST(0)	ESC MF 0	MOD 11 R R/M	DISP	108	140–147[f]	128	142–146[g]
ST(i) and ST(0)	ESC d P 0	1111 R R/M			90[h]		
FSQRT[i] = Square root	ESC 001	1111 1010			124–131		
FSCALE = Scale ST(0) by ST(1)	ESC 001	1111 1101			69–88		
FPREM = Partial remainder of ST(0) ÷ ST(1)	ESC 001	1111 1000			76–157		
FPREM1 = Partial remainder (IEEE)	ESC 001	1111 0101			97–187		
FRNDINT = Round ST(0) to integer	ESC 001	1111 1100			66–82		
FXTRACT = Extract components of ST(0)	ESC 001	1111 0100			72–78		
FABS = Absolute value of ST(0)	ESC 001	1110 0001			24		
FCHS = Change sign of ST(0)	ESC 001	1110 0000			26–27		

Shaded areas indicate instructions not available in 8087.

NOTES:
b. Add 3 clocks to the range when d = 1.
c. Add 1 clock to **each** range when R = 1.
d. Add 3 clocks to the range when d = 0.
e. typical = 54 (When d = 0, 48–56, typical = 51).
f. Add 1 clock to the range when R = 1.
g. 153–159 when R = 1.
h. Add 3 clocks to the range when d = 1.
i. $-0 \leq ST(0) \leq +\infty$.

80C187 Extensions to the 80C186 Instruction Set (Continued)

Instruction	Encoding			Clock Count Range
	Byte 0	Byte 1	Optional Bytes 2–3	
TRANSCENDENTAL				
FCOS = Cosine of ST(0)	ESC 001	1111 1111		125–774j
FPTAN[k] = Partial tangent of ST(0)	ESC 001	1111 0010		193–499j
FPATAN = Partial arctangent	ESC 001	1111 0011		316–489
FSIN = Sine of ST(0)	ESC 001	1111 1110		124–773j
FSINCOS = Sine and cosine of ST(0)	ESC 001	1111 1011		196–811j
F2XM1[l] = $2^{ST(0)} - 1$	ESC 001	1111 0000		213–478
FYL2X[m] = ST(1) * $\log_2(ST(0))$	ESC 001	1111 0001		122–540
FYL2XP1[n] = ST(1) * $\log_2(ST(0) + 1.0)$	ESC 001	1111 1001		259–549
PROCESSOR CONTROL				
FINIT = Initialize NPX	ESC 011	1110 0011		35
FSTSW AX = Store status word	ESC 111	1110 0000		17
FLDCW = Load control word	ESC 001	MOD 101 R/M	DISP	23
FSTCW = Store control word	ESC 001	MOD 111 R/M	DISP	21
FSTSW = Store status word	ESC 101	MOD 111 R/M	DISP	21
FCLEX = Clear exceptions	ESC 011	1110 0010		13
FSTENV = Store environment	ESC 001	MOD 110 R/M	DISP	146
FLDENV = Load environment	ESC 001	MOD 100 R/M	DISP	113
FSAVE = Save state	ESC 101	MOD 110 R/M	DISP	550
FRSTOR = Restore state	ESC 101	MOD 100 R/M	DISP	482
FINCSTP = Increment stack pointer	ESC 001	1111 0111		23
FDECSTP = Decrement stack pointer	ESC 001	1111 0110		24
FFREE = Free ST(i)	ESC 101	1100 0 ST(i)		20
FNOP = No operations	ESC 001	1101 0000		14

Shaded areas indicate instructions not available in 8087.

NOTES:
j. These timings hold for operands in the range $|x| < \pi/4$. For operands not in this range, up to 78 clocks may be needed to reduce the operand.
k. $0 \leq |ST(0)| < 2^{63}$.
l. $-1.0 \leq ST(0) \leq 1.0$.
m. $0 \leq ST(0) < \infty$, $-\infty < ST(1) < +\infty$.
n. $0 \leq |ST(0)| < (2 - \sqrt{(2)})/2$, $-\infty < ST(1) < +\infty$.

DATA SHEET REVISION REVIEW

The following list represents the key differences between the -002 and the -001 version of the 80C187 data sheet. Please review this summary carefully.

1. Figure 10, titled "System Configuration for 8087—Compatible Exception Trapping", was replaced with a revised schematic. The previous configuration was faulty. Updated timing diagrams on Data Transfer Timing, Error Output, and RESET/BUSY.

80188
HIGH INTEGRATION 8-BIT MICROPROCESSOR

- **Integrated Feature Set**
  - — Enhanced 8086-2 CPU
  - — Clock Generator
  - — 2 Independent DMA Channels
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  - — 3 Programmable 16-Bit Timers
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- **16-Bit Internal Architecture with 8-Bit Data Bus Interface**
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  - — In-Circuit-Emulator (I²ICE™-186/188)
- **Numeric Coprocessing Capability Through 8087 Interface**
- **Available in 68 Pin:**
  - — Ceramic Leadless Chip Carrier (LCC)
  - — Ceramic Pin Grid Array (PGA)
  - — Plastic Leaded Chip Carrier (PLCC)

  (See Packaging Outlines and Dimensions, Order #231369)
- **Available in EXPRESS**
  - — Standard Temperature with Burn-In
  - — Extended Temperature Range (−40°C to +85°C)

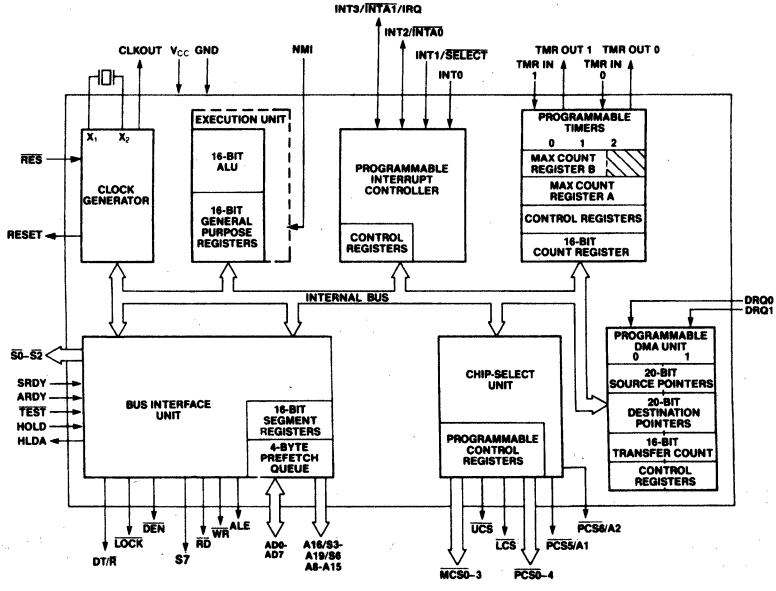

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Figure 1. 80188 Block Diagram

May 1991
Order Number: 210706-011

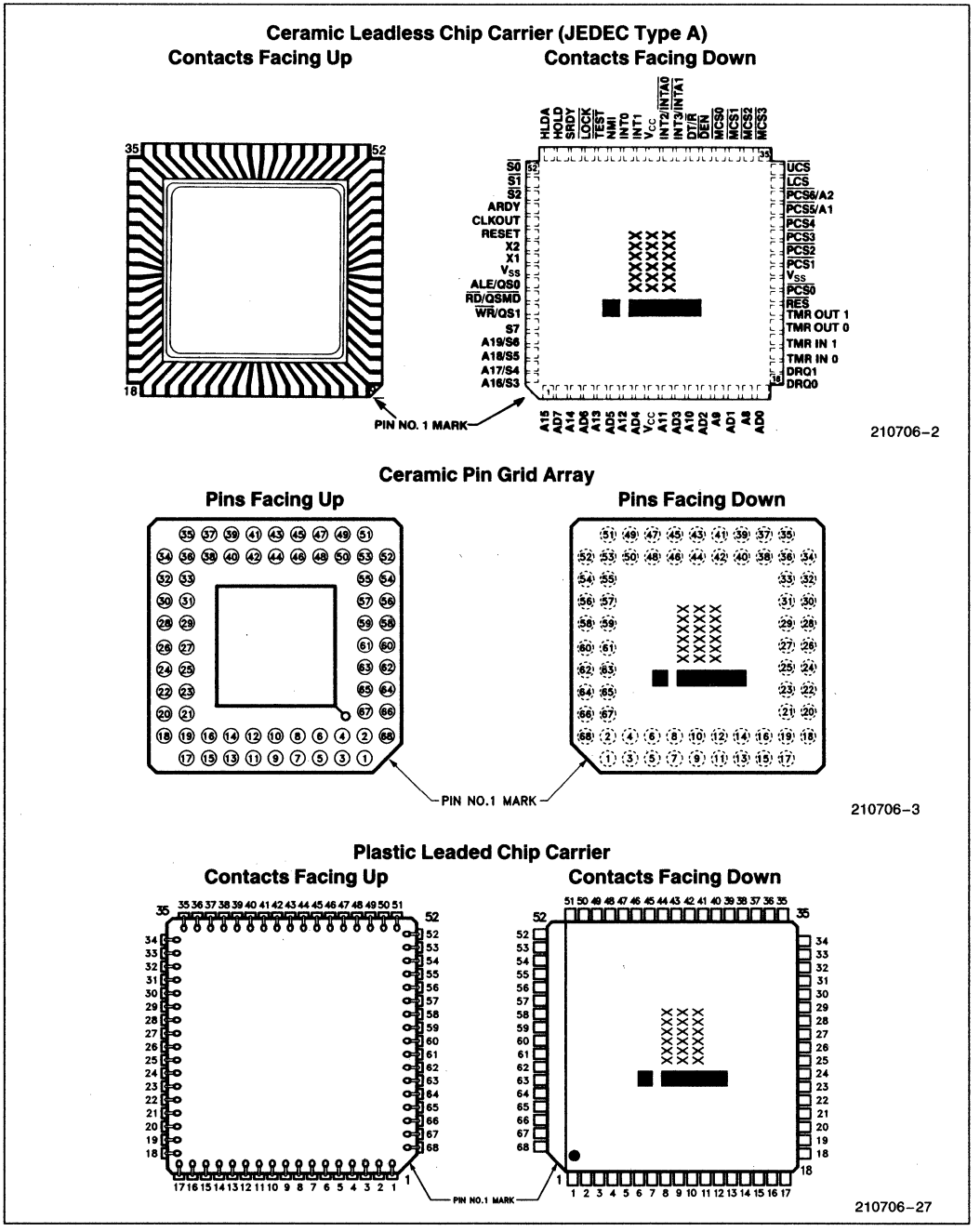

Figure 2. 80188 Pinout Diagram

Table 1. 80188 Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	9 43	I I	**SYSTEM POWER:** +5 volt power supply.
V_{SS}	26 60	I I	**SYSTEM GROUND**
RESET	57	O	**RESET OUTPUT:** Indicates that the 80188 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal.
X1 X2	59 58	I O	**CRYSTAL INPUTS:** X1 and X2 provide external connections for a fundamental mode parallel resonant crystal for the internal oscillator. Instead of using a crystal, an external clock may be applied to X1 while minimizing stray capacitance on X2. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	**CLOCK OUTPUT:** Provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT.
$\overline{RES}$	24	I	**PROCESSOR RESET:** Causes the 80188 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80188 clock. The 80188 begins fetching instructions approximately 6½ clock cycles after $\overline{RES}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{RES}$ held low. $\overline{RES}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network. When $\overline{RES}$ occurs, the 80188 will drive the status lines to an inactive level for one clock, and then float them.
$\overline{TEST}$	47	I/O	**$\overline{TEST}$:** Is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when "WAIT" execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80188 is waiting for $\overline{TEST}$, interrupts will be serviced. During power-up, active $\overline{RES}$ is required to configure $\overline{TEST}$ as an input. This pin is synchronized internally.
TMR IN 0 TMR IN 1	20 21	I I	**TIMER INPUTS:** Are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized.
TMR OUT 0 TMR OUT 1	22 23	O O	**TIMER OUTPUTS:** Are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.
DRQ0 DRQ1	18 19	I I	**DMA REQUEST:** Is asserted HIGH by an external device when it is ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
NMI	46	I	**NON-MASKABLE INTERRUPT:** Causes a Type 2 interrupt. An NMI transition from LOW to HIGH is latched and synchronized internally, and initiates the interrupt at the next instruction boundary. NMI must be asserted for at least one clock. The Non-Maskable Interrupt cannot be avoided by programming.
INT0 INT1/SELECT INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$/ IRQ	45 44 42 41	I I I/O I/O	**MASKABLE INTERRUPT REQUESTS:** Can be requested by activating one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When Slave Mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).

Table 1. 80188 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
A19/S6 A18/S5 A17/S4 A16/S3	65 66 67 68	O O O O	**ADDRESS BUS OUTPUTS (16–19) and BUS CYCLE STATUS (3–6):** Indicate the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W, and T_4, the S6 pin is LOW to indicate a CPU-initiated bus cycle or HIGH to indicate a DMA-initiated bus cycle. During the same T-states, S3, S4, and S5 are always LOW. The status pins float during bus HOLD or RESET.
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	2 4 6 8 11 13 15 17	I/O I/O I/O I/O I/O I/O I/O I/O	**ADDRESS/DATA BUS (0-7):** Signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W, and T_4) bus. The bus is active HIGH.
A15 A14 A13 A12 A11 A10 A9 A8	1 3 5 7 10 12 14 16	O O O O O O O O	**ADDRESS-ONLY BUS (8-15):** Containing valid address from T_1-T_4. The bus is active HIGH.
S7	64	O	This signal is HIGH to indicate that the 80188 has an 8-bit data bus. S7 floats during HOLD.
ALE/QS0	61	O	**ADDRESS LATCH ENABLE/QUEUE STATUS 0:** Is provided by the 80188 to latch the address. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T_1 of the associated bus cycle, effectively one-half clock cycle earlier than in the 8088. The trailing edge is generated off the CLKOUT rising edge in T_1 as in the 8088. Note that ALE is never floated.
$\overline{WR}$/QS1	63	O	**WRITE STROBE/QUEUE STATUS 1:** Indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active LOW, and floats during HOLD. When the 80188 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.

QS1	QS0	Queue Operation
0	0	No Queue Operation
0	1	First Opcode Byte Fetched from the Queue
1	1	Subsequent Byte Fetched from the Queue
1	0	Empty the Queue

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Table 1. 80188 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RD}$/QSMD	62	I/O	**READ STROBE:** Is an active LOW signal which indicates that the 80188 is performing a memory or I/O read cycle. It is guaranteed not to go LOW before the A/D bus is floated. An internal pull-up ensures that $\overline{RD}$ is HIGH during RESET. Following RESET the pin is sampled to determine whether the 80188 is to provide ALE, $\overline{RD}$, and $\overline{WR}$, or queue status information. To enable Queue Status Mode, $\overline{RD}$ must be connected to GND. $\overline{RD}$ will float during bus HOLD.
ARDY	55	I	**ASYNCHRONOUS READY:** Informs the 80188 that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUT and is active HIGH. The falling edge of ARDY must be synchronized to the 80188 clock. Connecting ARDY HIGH will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the SRDY pin.
SRDY	49	I	**SYNCHRONOUS READY:** Informs the 80188 that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active-HIGH input synchronized to CLKOUT. The use of SRDY allows a relaxed system timing over ARDY. This is accomplished by elimination of the one-half clock cycle required to internally synchronize the ARDY input signal. Connecting SRDY high will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the ARDY pin.
$\overline{LOCK}$	48	O	**$\overline{LOCK}$:** Output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of that instruction. No instruction prefetching will occur while $\overline{LOCK}$ is asserted. When executing more than one LOCK instruction, always make sure there are 4 bytes of code between the end of the first LOCK instruction and the start of the second LOCK instruction. $\overline{LOCK}$ is active LOW, is driven HIGH for one clock during RESET, and then floated.
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	52 53 54	O O O	**BUS CYCLE STATUS $\overline{S0}$–$\overline{S2}$:** Are encoded to provide bus-transaction information:

80188 Bus Cycle Status Information

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

The status pins float during HOLD.
$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.

Table 1. 80188 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
HOLD (input) HLDA (output)	50 51	I O	**HOLD:** Indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the 80188 clock. The 80188 will issue a HLDA in response to a HOLD request at the end of T_4 or T_i. Simultaneous with the issuance of HLDA, the 80188 will float the local bus and control lines. After HOLD is detected as being LOW, the 80188 will lower HLDA. When the 80188 needs to run another bus cycle, it will again drive the local bus and control lines.
$\overline{UCS}$	34	O	**UPPER MEMORY CHIP SELECT:** Is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{UCS}$ is software programmable.
$\overline{LCS}$	33	O	**LOWER MEMORY CHIP SELECT:** Is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{LCS}$ is software programmable.
$\overline{MCS0}$ $\overline{MCS1}$ $\overline{MCS2}$ $\overline{MCS3}$	38 37 36 35	O O O O	**MID-RANGE MEMORY CHIP SELECT SIGNALS:** Are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{MCS0}$–3 are software programmable.
$\overline{PCS0}$ $\overline{PCS1}$ $\overline{PCS2}$ $\overline{PCS3}$ $\overline{PCS4}$	25 27 28 29 30	O O O O O	**PERIPHERAL CHIP SELECT SIGNALS 0–4:** Are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{PCS0}$–4 are software programmable.
$\overline{PCS5}$/A1	31	O	**PERIPHERAL CHIP SELECT 5 or LATCHED A1:** May be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software programmable. $\overline{PCS5}$/A1 does not float during bus HOLD. When programmed to provide latched A1, this pin will retain the previously latched value during HOLD.
$\overline{PCS6}$/A2	32	O	**PERIPHERAL CHIP SELECT 6 or LATCHED A2:** May be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software-programmable. $\overline{PCS6}$/A2 does not float during bus HOLD. When programmed to provide latched A2, this pin will retain the previously latched value during HOLD.
DT/$\overline{R}$	40	O	**DATA TRANSMIT/RECEIVE:** Controls the direction of data flow through an external data bus transceiver. When LOW, data is transferred to the 80188. When HIGH the 80188 places write data on the data bus.
$\overline{DEN}$	39	O	**DATA ENABLE:** Is provided as a data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access. $\overline{DEN}$ is HIGH whenever DT/$\overline{R}$ changes state. During RESET, $\overline{DEN}$ is driven HIGH for one clock, then floated. $\overline{DEN}$ also floats during bus HOLD.

FUNCTIONAL DESCRIPTION

Introduction

The following Functional Description describes the base architecture of the 80188. The 80188 is a very high integration 8-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip while providing twice the performance of the standard 8088. The 80188 is object code compatible with the 8086, 8088 microprocessors and adds 10 new instruction types to the 8086, 8088 instruction set.

80188 BASE ARCHITECTURE

The 8086, 8088, 80186, 80188 and 80286 family all contain the same basic set of registers, instructions, and addressing modes. The 80188 processor is upward compatible with the 8086, 8088, 80186, and 80286 CPUs.

Register Set

The 80188 base architecture has fourteen registers as shown in Figures 3a and 3b. These registers are grouped into the following categories.

GENERAL REGISTERS

Eight 16-bit general purpose registers may be used for arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

SEGMENT REGISTERS

Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

BASE AND INDEX REGISTERS

Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

STATUS AND CONTROL REGISTERS

Two 16-bit special purpose registers record or alter certain aspects of the 80188 processor state. These are the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed, and the Status Word Register, which contains status and control flag bits (see Figures 3a and 3b).

STATUS WORD DESCRIPTION

The Status Word records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the 80188 within a given operating mode (bits 8, 9, and 10). The Status Word Register is 16-bits wide. The function of the Status Word bits is shown in Table 2.

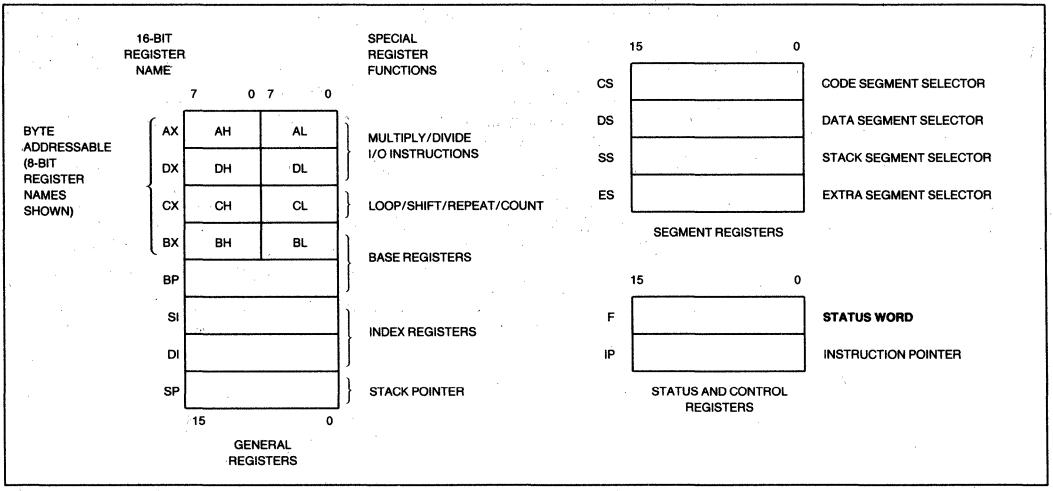

Figure 3a. 80188 Register Set

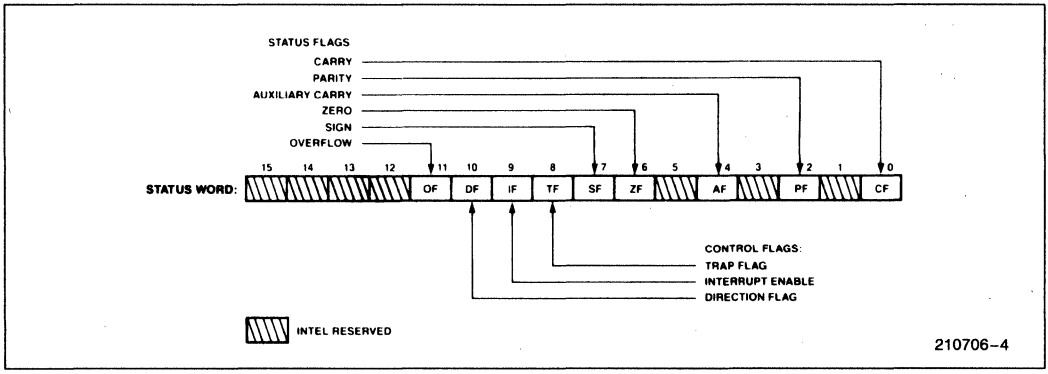

Figure 3b. Status Word Format

Table 2. Status Word Bit Functions

Bit Position	Name	Function
0	CF	Carry Flag—Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag—Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag—Set if result is zero; cleared otherwise
7	SF	Sign Flag—Set equal to high-order bit of result (0 if positive, 1 if negative)
8	TF	Single Step Flag—Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-Enable Flag—When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag—Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag—Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high-level instructions, and processor control. These categories are summarized in Figure 4.

An 80188 instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory. Specific operand addressing modes are discussed later in this data sheet.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment registers (code, data, stack, extra). The physical address is calculated by shifting the base value LEFT by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 5). This allows for a 1 MByte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 3). These rules follow the way programs are written (see Figure 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.

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GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack
ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero
LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word
FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{TEST}$ pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Figure 4. 80188 Instruction Set

CONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal
JAE/JNB	Jump if above or equal/not below
JB/JNAE	Jump if below/not above nor equal
JBE/JNA	Jump if below or equal/not above
JC	Jump if carry
JE/JZ	Jump if equal/zero
JG/JNLE	Jump if greater/not less nor equal
JGE/JNL	Jump if greater or equal/not less
JL/JNGE	Jump if less/not greater nor equal
JLE/JNG	Jump if less or equal/not greater
JNC	Jump if not carry
JNE/JNZ	Jump if not equal/not zero
JNO	Jump if not overflow
JNP/JPO	Jump if not parity/parity odd
JNS	Jump if not sign

JO	Jump if overflow
JP/JPE	Jump if parity/parity even
JS	Jump if sign
UNCONDITIONAL TRANSFERS	
CALL	Call procedure
RET	Return from procedure
JMP	Jump
ITERATION CONTROLS	
LOOP	Loop
LOOPE/LOOPZ	Loop if equal/zero
LOOPNE/LOOPNZ	Loop if not equal/not zero
JCXZ	Jump if register CX = 0
INTERRUPTS	
INT	Interrupt
INTO	Interrupt if overflow
IRET	Interrupt return

Figure 4. 80188 Instruction Set (Continued)

To access operands that do not reside in one of the four immediately available segments, a full 32-bit pointer can be used to reload both the base (segment) and offset values.

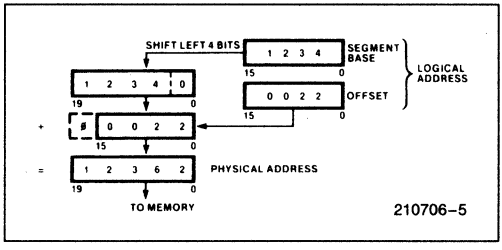

Figure 5. Two Component Address

Table 3. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data.
Stack	Stack (SS)	All stack pushes and pops; any memory references which use BP Register as a base register.
External Data (Global)	Extra (ES)	All string instruction references which use the DI register as an index.
Local Data	Data (DS)	All other data references.

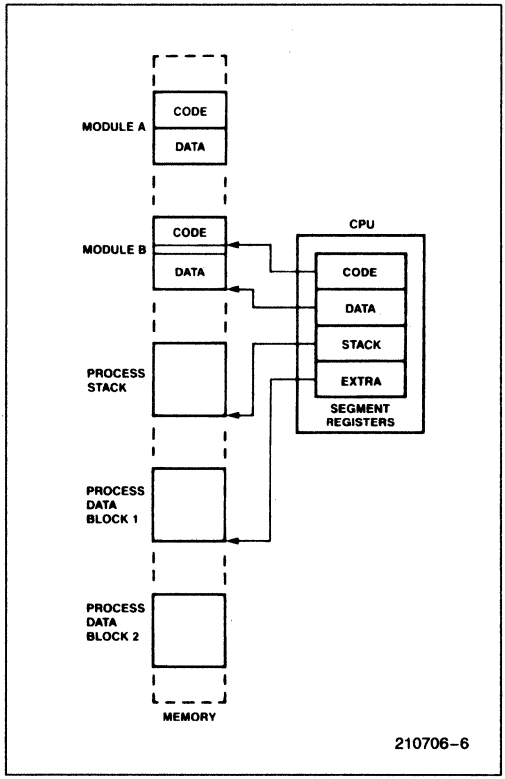

Figure 6. Segmented Memory Helps Structure Software

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Addressing Modes

The 80188 provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an index register.
- *Based Indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

Data Types

The 80188 directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32- and 64-bit integers are supported using an 8087 Numeric Data Coprocessor with the 80188.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component or a 16-bit segment base component in addition to a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 to 64K bytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4-bits) of the byte.
- *Floating Point:* A signed 32-, 64-, or 80-bit real number representation. (Floating point operands are supported using an 8087 Numeric Data Coprocessor with the 80188.)

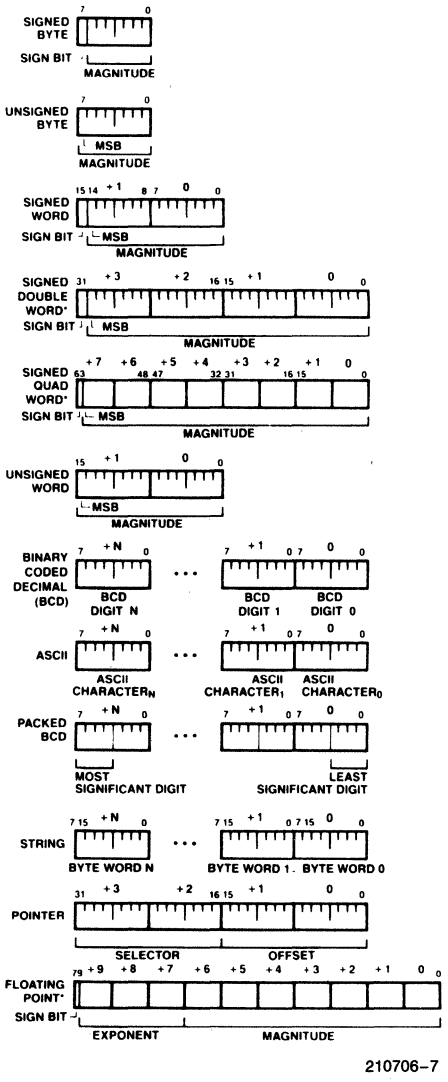
In general, individual data elements must fit within defined segment limits. Figure 7 graphically represents the data types supported by the 80188.

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A_{15}–A_8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Status Word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.



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NOTE:
*Supported using an 8087 Numeric Data Coprocessor with the 80188.

Figure 7. 80188 Supported Data Types

Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. If the exception was caused by executing an ESC instruction with the ESC trap bit set in the relocation register, the return instruction will point to the ESC instruction, or to the segment override prefix immediately preceding the ESC instruction if the prefix was present. In all other cases, the return address from an exception will point at the instruction immediately following the instruction causing the exception.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0–31, some of which are used for instruction exceptions, are reserved. Table 4 shows the 80188 predefined types and default priority levels. For each interrupt, an 8-bit vector must be supplied to the 80188 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. In addition, internal peripherals and noncascaded external interrupts will generate their own vectors through the internal interrupt controller. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Interrupt Sources

The 80188 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INT0, DIV, IDIV, etc.). All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type (Table 4), multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

Those pre-defined 80188 interrupts which cannot be masked by programming are described below.

DIVIDE ERROR EXCEPTION (TYPE 0)

Generated when a DIV or IDIV instruction quotient cannot be expressed in the number of bits in the destination.

SINGLE-STEP INTERRUPT (TYPE 1)

Generated after most instructions if the TF flag is set. Interrupts will not be generated after prefix instructions (e.g., REP), instructions which modify segment registers (e.g., POP DS), or the WAIT instruction.

NON-MASKABLE INTERRUPT—NMI (TYPE 2)

An external interrupt source which cannot be masked.

Table 4. 80188 Interrupt Vectors

Interrupt Name	Vector Type	Vector Address	Default Priority	Related Instructions	Applicable Notes
Divide Error Exception	0	00H	1	DIV, IDIV	1
Single Step Interrupt	1	04H	1A	All	2
Non-Maskable Interrupt (NMI)	2	08H	1	All	
Breakpoint Interrupt	3	0CH	1	INT	1
INTO Detected Overflow Exception	4	10H	1	INTO	1
Array Bounds Exception	5	14H	1	BOUND	1
Unused Opcode Exception	6	18H	1	Undefined Opcodes	1
ESC Opcode Exception	7	1CH	1	ESC Opcodes	1, 3
Timer 0 Interrupt	8	20H	2A		4, 5
Timer 1 Interrupt	18	48H	2B		4, 5
Timer 2 Interrupt	19	4CH	2C		4, 5
Reserved	9	24H	3		
DMA 0 Interrupt	10	28H	4		5
DMA 1 Interrupt	11	2CH	5		5
INT0 Interrupt	12	30H	6		
INT1 Interrupt	13	34H	7		
INT2 Interrupt	14	38H	8		
INT3 Interrupt	15	3CH	9		
Reserved	16, 17	40H, 44H			
Reserved	20–31	50H . . . 7CH			

NOTES:
Default priorities for the interrupt sources are used only if the user does not program each source into a unique priority level.
1. Generated as a result of an instruction execution.
2. Performed in same manner as 8088.
3. An ESC opcode will cause a trap if the power bit is set in the peripheral control block relocation register.
4. All three timers constitute one source of request to the interrupt controller. As such, they share the same priority level with respect to other interrupt sources. However, the timers have a defined priority order among themselves (2A > 2B > 2C).
5. The vector type numbers for these sources are programmable in Slave Mode.

BREAKPOINT INTERRUPT (TYPE 3)

A one-byte version of the INT instruction. It uses 12 as an index into the service routine address table (because it is a type 3 interrupt).

INTO DETECTED OVERFLOW EXCEPTION (TYPE 4)

Generated during an INTO instruction if the OF bit is set.

ARRAY BOUNDS EXCEPTION (TYPE 5)

Generated during a BOUND instruction if the array index is outside the array bounds. The array bounds are located in memory at a location indicated by one of the instruction operands. The other operand indicates the value of the index to be checked.

UNUSED OPCODE EXCEPTION (TYPE 6)

Generated if execution is attempted on undefined opcodes.

ESCAPE OPCODE EXCEPTION (TYPE 7)

Generated if execution is attempted of ESC opcodes (D8H–DFH). This exception will only be generated if a bit in the relocation register is set. The return address of this exception will point to the ESC instruction causing the exception. If a segment override prefix preceded the ESC instruction, the return address will point to the segment override prefix.

Hardware-generated interrupts are divided into two groups: maskable interrupts and non-maskable interrupts. The 80188 provides maskable hardware interrupt request pins INT0–INT3. In addition, maskable interrupts may be generated by the 80188 integrated DMA controller and the integrated timer unit. The vector types for these interrupts are shown in Table 4. Software enables these inputs by setting the Interrupt Flag bit (IF) in the Status Word. The interrupt controller is discussed in the peripheral section of this data sheet.

Further maskable interrupts are disabled while servicing an interrupt because the IF bit is reset as part of the response to an interrupt or exception. The saved Status Word will reflect the enable status of the processor prior to the interrupt. The interrupt flag will remain zero unless specifically set. The interrupt return instruction restores the Status Word, thereby restoring the original status of IF bit. If the interrupt return re-enables interrupts, and another interrupt is pending, the 80188 will immediately service the highest-priority interrupt pending, i.e., no instructions of the main line program will be executed.

Non-Maskable Interrupt Request (NMI)

A non-maskable interrupt (NMI) is also provided. This interrupt is serviced regardless of the state of the IF bit. A typical use of NMI would be to activate a power failure routine. The activation of this input causes an interrupt with an internally supplied vector value of 2. No external interrupt acknowledge sequence is performed. The IF bit is cleared at the beginning of an NMI interrupt to prevent maskable interrupts from being serviced.

Single-Step Interrupt

The 80188 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single-step interrupt and is controlled by the single-step flag bit (TF) in the Status Word. Once this bit is set, an internal single-step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single-stepped.

Initialization and Processor Reset

Processor initialization is accomplished by driving the $\overline{RES}$ input pin LOW. $\overline{RES}$ must be LOW during power-up to ensure proper device initialization, $\overline{RES}$ forces the 80188 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{RES}$ is active. After $\overline{RES}$ becomes inactive and an internal processing interval elapses, the 80188 begins execution with the instruction at physical location FFFF0(H). $\overline{RES}$ also sets some registers to predefined values as shown in Table 5.

Table 5. 80188 Initial Register State after RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

THE 80188 COMPARED TO THE 80186

The 80188 CPU is an 8-bit processor designed around the 80186 internal structure. Most internal functions of the 80188 are identical to the equivalent 80186 functions. The 80188 handles the external bus the same way the 80186 does with the distinction of handling only 8 bits at a time. Sixteen bit operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. The differences between the 80188 and the 80186 are outlined below. Internally, there are three differences between the 80188 and the 80186. All changes are related to the 8-bit bus interface.

- The queue length is 4 bytes in the 80188, whereas the 80186 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8 bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The 80188 BIU will fetch a new instruction to load into the queue each time there is a 1-byte hole (space available) in the queue. The 80186 waits until a 2-byte space is available.

- The internal execution time of the instruction is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU may also be limited by the speed of instruction fetches when a series of simple operations occur. When the more sophisticated instructions of the 80188 are being used, the queue has time to fill and the execution proceeds as fast as the execution unit will allow.

The 80188 and 80186 are completely software compatible by virtue of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally well on an 80188 or an 80186.

The hardware interface of the 80188 contains the major differences between the two CPUs. The pin assignments are nearly identical, however, with the following functional changes.

- A8–A15—These pins are only address outputs on the 80188. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.
- $\overline{BHE}$ has no meaning on the 80188 and has been eliminated.

80188 Clock Generator

The 80188 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

Oscillator

The oscillator circuit of the 80188 is designed to be used with a parallel resonant fundamental mode crystal. This is used as the time base for the 80188. The crystal frequency selected will be double the CPU clock frequency. Use of an LC or RC circuit is not recommended with this oscillator. If an external oscillator is used, it can be connected directly to input pin X1 in lieu of a crystal. The output of the oscillator is not directly available outside the 80188. The recommended crystal configuration is shown in Figure 8.

Intel recommends the following values for crystal selection parameters.

Temperature Range:	0 to 70°C
ESR (Equivalent Series Resistance):	30Ω max
C_0 (Shunt Capacitance of Crystal):	7.0 pf max
C_L (Load Capacitance):	20 pf ±2 pf
Drive Level:	1 mW max

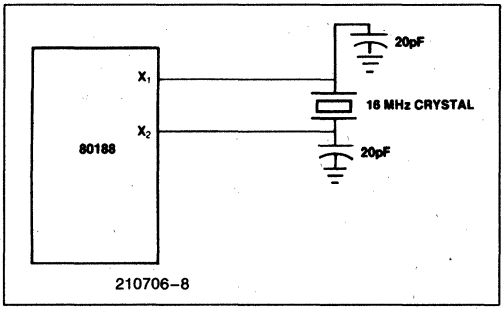

Figure 8. Recommended 8 MHz 80188 Crystal Configuration

Clock Generator

The 80188 clock generator provides the 50% duty cycle processor clock for the 80188. It does this by dividing the oscillator output by 2 forming the symmetrical clock. If an external oscillator is used, the state of the clock generator will change on the falling edge of the oscillator signal. The CLKOUT pin provides the processor clock signal for use outside the 80188. This may be used to drive other system components. All timings are referenced to the output clock.

READY Synchronization

The 80188 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T_2, T_3, and again in the middle of each T_W until ARDY is sampled HIGH. One-half CLKOUT cycle of resolution time is used for full synchronization of a rising ARDY signal. A high-to-low transition on ARDY may be used as an indication of the not ready condition but it must be performed synchronously to CLKOUT **either** in the middle of T_2, T_3, **or** T_W, or at the falling edge of T_3 or T_W.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T_2, T_3, and again at the end of each T_W until it is sampled HIGH. By using this input rather than the asynchronous ready input, the half-clock cycle resolution time penalty is eliminated.

This input must satisfy set-up and hold times to guarantee proper operation of the circuit.

In addition, the 80188, as part of the integrated chip-select logic, has the capability to program WAIT states for memory and peripheral blocks. This is discussed in the Chip Select/Ready Logic description.

RESET Logic

The 80188 provides both a $\overline{RES}$ input pin and a synchronized RESET output pin for use with other system components. The $\overline{RES}$ input pin on the 80188 is provided with hysteresis in order to facilitate power-on Reset generation via an RC network. RESET output is guaranteed to remain active for at least five clocks given a $\overline{RES}$ input of at least six clocks. RESET may be delayed up to approximately two and one-half clocks behind $\overline{RES}$.

Multiple 80188 processors may be synchronized through the $\overline{RES}$ input pin, since this input resets both the processor and divide-by-two internal counter in the clock generator. In order to ensure that the divide-by-two counters all begin counting at the same time, the active going edge of $\overline{RES}$ must satisfy a 25 ns setup time before the falling edge of the 80188 clock input. In addition, in order to ensure that all CPUs begin executing in the same clock cycle, the reset must satisfy a 25 ns setup time before the rising edge of the CLKOUT signal of all the processors.

LOCAL BUS CONTROLLER

The 80188 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides outputs that can be used to enable external buffers and to direct the flow of data on and off the local bus.

Memory/Peripheral Control

The 80188 provides ALE, $\overline{RD}$, and $\overline{WR}$ bus control signals. The $\overline{RD}$ and $\overline{WR}$ signals are used to strobe data from memory or I/O to the 80188 or to strobe data from the 80188 to memory or I/O. The ALE line provides a strobe to latch the address when it is valid. The 80188 local bus controller does not provide a memory/$\overline{I/O}$ signal. If this is required, use the $\overline{S2}$ signal (which will require external latching), make the memory and I/O spaces nonoverlapping, or use only the integrated chip-select circuitry.

Transceiver Control

The 80188 generates two control signals for external transceiver chips. This capability allows the addition of transceivers for extra buffering without adding external logic. These control lines, DT/$\overline{R}$ and $\overline{DEN}$, are generated to control the flow of data through the transceivers. The operation of these signals is shown in Table 6.

Table 6. Transceiver Control Signals Description

Pin Name	Function
$\overline{DEN}$ (Data Enable)	Enables the output drivers of the transceivers. It is active LOW during memory, I/O, or INTA cycles.
DT/$\overline{R}$ (Data Transmit/ Receive)	Determines the direction of travel through the transceivers. A HIGH level directs data away from the processor during write operations, while a LOW level directs data toward the processor during a read operation.

Local Bus Arbitration

The 80188 uses a HOLD/HLDA system of local bus exchange. This provides an asynchronous bus exchange mechanism. This means multiple masters utilizing the same bus can operate at separate clock frequencies. The 80188 provides a single HOLD/HLDA pair through which all other bus masters may gain control of the local bus. External circuitry must arbitrate which external device will gain control of the bus when there is more than one alternate local bus master. When the 80188 relinquishes control of the local bus, it floats $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S0}$–$\overline{S2}$, $\overline{LOCK}$, AD0–AD7, A8–A19, $\overline{S7}$, and DT/$\overline{R}$ to allow another master to drive these lines directly.

The 80188 HOLD latency time, i.e., the time between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is the highest-priority activity request which the processor may receive: higher than instruction fetching or internal DMA cycles. However, if a DMA cycle is in progress, the 80188 will complete the transfer before relinquishing the bus. This implies that if a HOLD request is received just as a DMA transfer begins, the HOLD latency time can be as great as 4 bus cycles. This will occur if a DMA word transfer operation is taking place from an odd address to an odd address. This is a total of 16 clocks or more, if WAIT states are required. In addition, if locked transfers are performed, the HOLD latency time will be increased by the length of the locked transfer.

Local Bus Controller and Reset

During RESET the local bus controller will perform the following actions:

- Drive $\overline{DEN}$, $\overline{RD}$, and $\overline{WR}$ HIGH for one clock cycle, then float.

NOTE:
$\overline{RD}$ is also provided with an internal pull-up device to prevent the processor from inadvertently entering Queue Status Mode during RESET.

- Drive $\overline{S0}$–$\overline{S2}$ to the inactive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Three-state AD0–7, A8–19, S7, DT/$\overline{R}$.
- Drive ALE LOW (ALE is never floated).
- Drive HLDA LOW.

INTERNAL PERIPHERAL INTERFACE

All the 80188 integrated peripherals are controlled by 16-bit registers contained within an internal 256-byte control block. The control block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D_{7-0}, SRDY, and ARDY will be ignored. The base address of the control block must be on an even 256-byte boundary (i.e., the lower 8 bits of the base address are all zeros). All of the defined registers within this control block may be read or written by the 80188 CPU at any time

The control block base address is programmed by a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block (see Figure 9). It provides the upper 12 bits of the base address of the control block. Note that mapping the control register block into an address range corresponding to a chip-select range is not recommended (the chip select circuitry is discussed later in this data sheet. In addition, bit 12 of this register determines whether the control block will be mapped into I/O or memory space. If this bit is 1, the control block will be located in memory space. If the bit is 0, the control block will be located in I/O space. If the control register block is mapped into I/O space, the upper 4 bits of the base address must be programmed as 0 (since I/O addresses are only 16 bits wide).

Whenever mapping the 188 peripheral control block to another location, the programming of the relocation register should be done with a byte write (i.e. OUT DX,AL). Any access to the control block is done 16 bits at a time. Thus, internally, the relocation register will get written with 16 bits of the AX register while externally, the BIU will run only one 8-bit bus cycle. If a word instruction is used (i.e. OUT DX,AX), the relocation register will be written on the first bus cycle. The Bus Interface Unit (BIU) will then run a second bus cycle which is unnecessary. The address of the second bus cycle will no longer be within the control block (i.e. the control block was moved on the first cycle), and therefore, will require the generation of an external ready signal to complete the cycle. For this reason we recommend byte operations to the relocation register. Byte instructions may also be used for the other registers in the control block and will eliminate half of the bus cycles required if a word operation had been specified. Byte operations are only valid on even addresses though, and are undefined on odd addresses.

In addition to providing relocation information for the control block, the relocation register contains bits which place the interrupt controller into Slave Mode, and cause the CPU to interrupt upon encountering ESC instructions. At RESET, the relocation register is set to 20FFH which maps the control block to start at FF00H in I/O space. An offset map of the 256-byte control register block is shown in Figure 10.

CHIP-SELECT/READY GENERATION LOGIC

The 80188 contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

Memory Chip Selects

The 80188 provides 6 memory chip select outputs for 3 address areas: upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

The range for each chip select is user-programmable and can be set to 2K, 4K, 8K, 16K, 32K, 64K, 128K (plus 1K and 256K for upper and lower chip selects). In addition, the beginning or base address

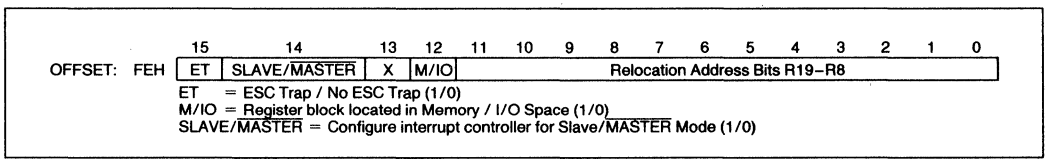

Figure 9. Relocation Register

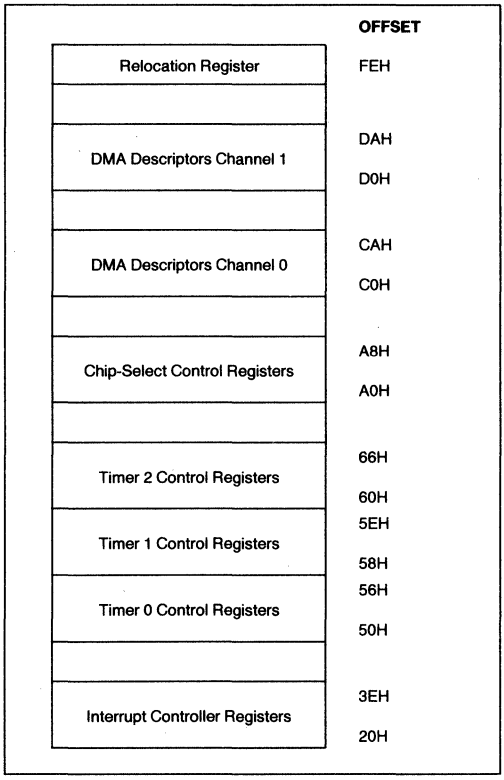

Figure 10. Internal Register Map

of the midrange memory chip select may also be selected. Only one chip select may be programmed to be active for any memory location at a time. All chip select sizes are in bytes.

Upper Memory $\overline{CS}$

The 80188 provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the 80188 begins executing at memory location FFFF0H.

The upper limit of memory defined by this chip select is always FFFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is also defined. Table 7 shows the relationship between the base address selected and the size of the memory block obtained.

Table 7. UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000	256K	C038H

The lower limit of this memory block is defined in the UMCS register (see Figure 11). This register is at offset A0H in the internal control block. The legal values for bits 6–13 and the resulting starting address and memory block sizes are given in Table 7. Any combination of bits 6–13 not shown in Table 7 will result in undefined operation. After reset, the UMCS register is programmed for a 1K area. It must be reprogrammed if a larger upper memory area is desired.

The internal generation of any 20-bit address whose upper 16 bits are equal to or greater than the UMCS value (with bits 0–5 as "0") asserts $\overline{UCS}$. UMCS bits R2–R0 specify the ready mode for the area of memory defined by the chip select register, as explained later.

Lower Memory $\overline{CS}$

The 80188 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The lower limit of memory defined by this chip select is always 0H, while the upper limit is programmable. By programming the upper limit, the size of the memory block is defined. Table 8 shows the relationship between the upper address selected and the size of the memory block obtained.

Table 8. LMCS Programming Values

Upper Address	Memory Block Size	LMCS Value (Assuming R0=R1=R2=0)
003FFH	1K	0038H
007FFH	2K	0078H
00FFFH	4K	00F8H
01FFFH	8K	01F8H
03FFFH	16K	03F8H
07FFFH	32K	07F8H
0FFFFH	64K	0FF8H
1FFFFH	128K	1FF8H
3FFFFH	256K	3FF8H

The upper limit of this memory block is defined in the LMCS register (see Figure 12) at offset A2H in the internal control block. The legal values for bits 6–15 and the resulting upper address and memory block sizes are given in Table 8. Any combination of bits 6–15 not shown in Table 8 will result in undefined operation. After RESET, the LMCS register value is undefined. However, the $\overline{LCS}$ chip-select line will not become active until the LMCS register is accessed.

Any internally generated 20-bit address whose upper 16 bits are less than or equal to LMCS (with bits 0–5 "1") will assert $\overline{LCS}$. LMCS register bits R2–R0 specify the READY mode for the area of memory defined by this chip-select register.

Mid-Range Memory $\overline{CS}$

The 80188 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located within the 80188 1M byte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the mid-range select lines, as shown in Table 9, is determined by bits 8–14 of the MPCS register (see Figure 13). This register is at location A8H in the internal control block. One and only one of bits 8–14 must be set at a time. Unpredictable operation of the $\overline{MCS}$ lines will otherwise occur. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the mid-range block. If the total block size is 32K, each chip select is active for 8K of memory with $\overline{MCS0}$ being active for the first range and $\overline{MCS3}$ being active for the last range.

The EX and MS in MPCS relate to peripheral functionality as described in a later section.

Table 9. MPCS Programming Values

Total Block Size	Individual Select Size	MPCS Bits 14–8
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

The base address of the mid-range memory block is defined by bits 15–9 of the MMCS register (see Figure 14). This register is at offset A6H in the internal control block. These bits correspond to bits A19–A13 of the 20-bit memory address. Bits A12–A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the mid-range block size is 32K (or the size of the block for which each $\overline{MCS}$ line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, since the first few integer multiples of a 32K memory block are 0H, 8000H, 10000H, 18000H, etc. After RESET, the contents of both of these registers are undefined. However, none of the $\overline{MCS}$ lines will be active until both the MMCS and MPCS registers are accessed.

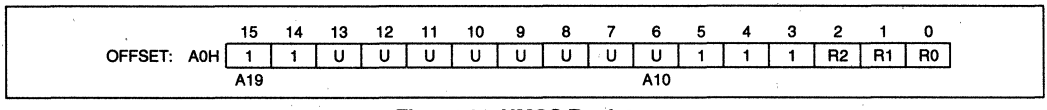

Figure 11. UMCS Register

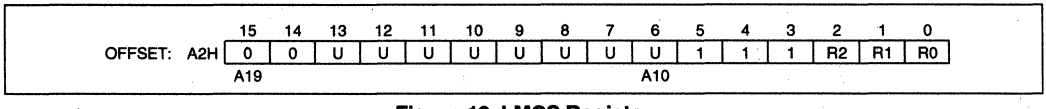

Figure 12. LMCS Register

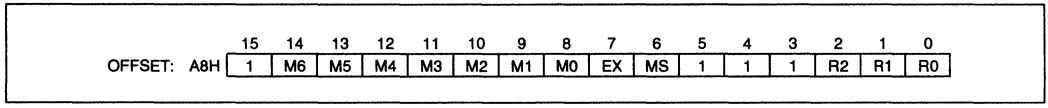

Figure 13. MPCS Register

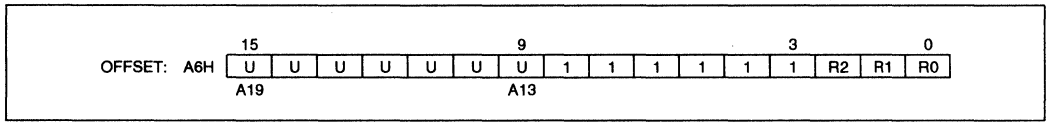

Figure 14. MMCS Register

MMCS bits R2–R0 specify READY mode of operation for all four mid-range chip selects.

The 512K block size for the mid-range memory chip selects is a special case. When using 512K, the base address would have to be at either locations 00000H or 80000H. If it were to be programmed at 00000H when the $\overline{LCS}$ line was programmed, there would be an internal conflict between the $\overline{LCS}$ ready generation logic and the $\overline{MCS}$ ready generation logic. Likewise, if the base address were programmed at 80000H, there would be a conflict with the $\overline{UCS}$ ready generation logic. Since the $\overline{LCS}$ chip-select line does not become active until programmed, while the $\overline{UCS}$ line is active at reset, the memory base can be set only at 00000H. If this base address is selected, however, the $\overline{LCS}$ range must not be programmed.

Peripheral Chip Selects

The 80188 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address may be located in either memory or I/O space.

Seven $\overline{CS}$ lines called $\overline{PCS0}$–6 are generated by the 80188. The base address is user-programmable; however it can only be a multiple of 1K bytes, i.e., the least significant 10 bits of the starting address are always 0.

$\overline{PCS5}$ and $\overline{PCS6}$ can also be programmed to provide latched address bits A1 and A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0 and A1 pins used for selecting internal registers of 8-bit peripheral chips.

The starting address of the peripheral chip-select block is defined by the PACS register (see Figure 15). The register is located at offset A4H in the internal control block. Bits 15–6 of this register correspond to bits 19–10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block. Bits 9–0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12–15 must be programmed zero, since the I/O address is only 16 bits wide. Table 10 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

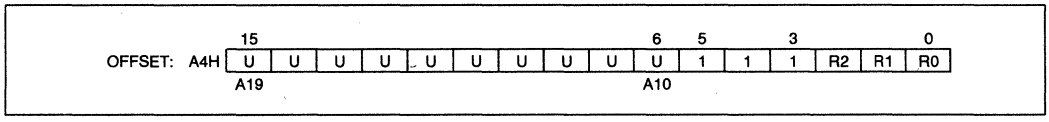

Figure 15. PACS Register

The user should program bits 15–6 to correspond to the desired peripheral base location. PACS bits 0–2 are used to specify READY mode for $\overline{PCS0}$–$\overline{PCS3}$.

Table 10. PCS Address Ranges

$\overline{PCS}$ Line	Active between Locations
$\overline{PCS0}$	PBA —PBA+127
$\overline{PCS1}$	PBA+128—PBA+255
$\overline{PCS2}$	PBA+256—PBA+383
$\overline{PCS3}$	PBA+384—PBA+511
$\overline{PCS4}$	PBA+512—PBA+639
$\overline{PCS5}$	PBA+640—PBA+767
$\overline{PCS6}$	PBA+768—PBA+895

The mode of operation of the peripheral chip selects is defined by the MPCS register (which is also used to set the size of the mid-range memory chip-select block, see Figure 13). The register is located at offset A8H in the internal control block. Bit 7 is used to select the function of $\overline{PCS5}$ and $\overline{PCS6}$, while bit 6 is used to select whether the peripheral chip selects are mapped into memory or I/O space. Table 11 describes the programming of these bits. After RESET, the contents of both the MPCS and the PACS registers are undefined, however none of the PCS lines will be active until both of the MPCS and PACS registers are accessed.

Table 11. MS, EX Programming Values

Bit	Description
MS	1 = Peripherals mapped into memory space.
	0 = Peripherals mapped into I/O space.
EX	0 = 5 $\overline{PCS}$ lines. A1, A2 provided.
	1 = 7 $\overline{PCS}$ lines. A1, A2 are not provided.

MPCS bits 0–2 specify the READY mode for $\overline{PCS4}$–$\overline{PCS6}$ as outlined below.

READY Generation Logic

The 80188 can generate a READY signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the 80188 may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

READY control consists of 3 bits for each $\overline{CS}$ line or group of lines generated by the 80188. The interpretation of the READY bits is shown in Table 12.

Table 12. READY Bits Programming

R2	R1	R0	Number of WAIT States Generated
0	0	0	0 wait states, external RDY also used.
0	0	1	1 wait state inserted, external RDY also used.
0	1	0	2 wait states inserted, external RDY also used.
0	1	1	3 wait states inserted, external RDY also used.
1	0	0	0 wait states, external RDY ignored.
1	0	1	1 wait state inserted, external RDY ignored.
1	1	0	2 wait states inserted, external RDY ignored.
1	1	1	3 wait states inserted, external RDY ignored.

The internal READY generator operates in parallel with external READY, not in series if the external READY is used (R2 = 0). For example, if the internal generator is set to insert two wait states, but activity on the external READY lines will insert four wait states, the processor will only insert four wait states, not six. This is because the two wait states generated by the internal generator overlapped the first two wait states generated by the external ready signal. Note that the external ARDY and SRDY lines are always ignored during cycles accessing internal peripherals.

R2–R0 of each control word specifies the READY mode for the corresponding block, with the exception of the peripheral chip selects: R2–R0 of PACS set the $\overline{PCS0}$–3 READY mode, R2–R0 of MPCS set the $\overline{PCS4}$–6 READY mode.

Chip Select/Ready Logic and Reset

Upon RESET, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to insert 3 wait states in conjunction with external READY (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

DMA Channels

The 80188 DMA controller provides two independent DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer. Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a data transfer rate of one MByte/sec at 8 MHz.

DMA Operation

Each channel has six registers in the control block which define each channel's operation. The control registers consist of a 20-bit Source pointer (2 words), a 20-bit Destination pointer (2 words), a 16-bit Transfer Count Register, and a 16-bit Control Word.

The format of the DMA Control Blocks is shown in Table 13. The Transfer Count Register (TC) specifies the number of DMA transfers to be performed. Up to 64K byte transfers can be performed with automatic termination. The Control Word defines the channel's operation (see Figure 17). All registers may be modified or altered during any DMA activity. Any changes made to these registers will be reflected immediately in DMA operation.

Table 13. DMA Control Block Format

Register Name	Register Address	
	Ch. 0	Ch. 1
Control Word	CAH	DAH
Transfer Count	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

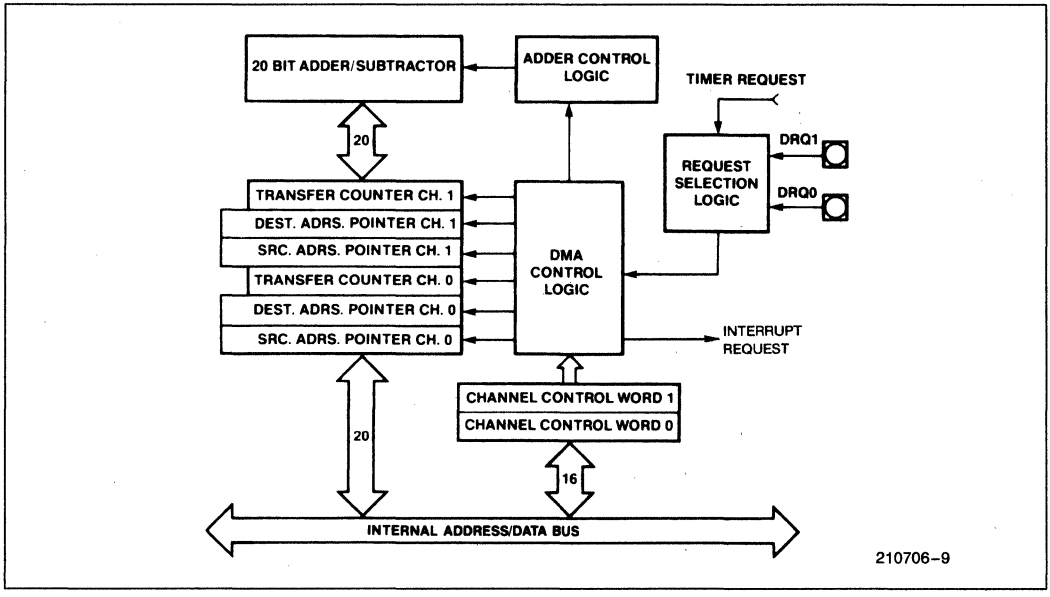

Figure 16. DMA Unit Block Diagram

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M/$\overline{IO}$	DEST DEC	DEST INC	M/$\overline{IO}$	SRC DEC	SRC INC	TC	INT	SYN		P	TDRQ	X	CHG/$\overline{NOCHG}$	ST/$\overline{STOP}$	X

X = Don't Care

Figure 17. DMA Control Register

DMA Channel Control Word Register

Each DMA Channel Control Word determines the mode of operation for the particular 80188 DMA channel. This register specifies:

- the mode of synchronization;
- whether interrupts will be generated after the last transfer;
- whether DMA activity will cease after a programmed number of DMA cycles;
- the relative priority of the DMA channel with respect to the other DMA channel;
- whether the source pointer will be incremented, decremented, or maintained constant after each transfer;
- whether the source pointer addresses memory or I/O space;
- whether the destination pointer will be incremented, decremented, or maintained constant after each transfer; and
- whether the destination pointer will address memory or I/O space.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

DMA Control Word Bit Descriptions

DEST: M/$\overline{IO}$ Destination pointer is in memory (1) or I/O (0) space.

DEC Decrement destination pointer by 1 after each transfer.

INC Increment destination pointer by 1 after each transfer.

If both INC and DEC are specified, the pointer will not be changed after each cycle.

SOURCE: M/$\overline{IO}$ Source pointer is in memory (1) or I/O (0) space.

DEC Decrement source pointer by 1 after each transfer.

INC Increment source pointer by 1 after each transfer.

If both INC and DEC are specified, the pointer will not be changed after each cycle.

TC: If set, DMA will terminate when the contents of the transfer count register reach zero. The ST/$\overline{STOP}$ bit will also be reset at this point. If cleared, the DMA controller will decrement the transfer count register for each DMA cycle, but DMA transfers will not stop when the transfer count register reaches zero.

INT: Enable interrupts to CPU upon transfer count termination.

SYN: 00 No synchronization.

NOTE:

When unsynchronized transfers are specified, the TC bit will be ignored and the ST bit will be cleared upon the transfer count reaching zero, stopping the channel.

01 Source Synchronization.

10 Destination Synchronization.

11 Unused.

P: Channel priority relative to other channel during simultaneous requests.

0 Low priority.

1 High priority.

Channels will alternate cycles if both are set at the same priority level.

TDRQ: Enable/Disable (1/0) DMA requests from Timer 2.

CHG/$\overline{NOCHG}$: Change/Do Not Change (1/0) the ST/$\overline{STOP}$ bit. If this bit is set when writing the control word, the ST/$\overline{STOP}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{STOP}$ bit will not be altered. This bit is not stored; it will always be read as 0.

ST/$\overline{STOP}$: Start/Stop (1/0) Channel.

DMA Destination and Source Pointer Registers

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address (see Figure 18). These pointers may be individually incremented or decremented after each transfer. Each pointer may point into either memory or I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on values for the pointer registers.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). The register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA Control Register. If the TC bit in the DMA control word is set or if unsynchronized transfers are programmed, DMA activity will terminate when the transfer count register reaches zero.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred. When source or unsynchronized transfers are performed, the DMA channel may begin another transfer immediately after the end of a previous DMA transfer. This allows a complete transfer to take place every 2 bus cycles or eight clock cycles (assuming no wait states). When destination synchronized transfers are performed, data will not be fetched from the source address until the destination device signals that it is ready to receive it. Also, the DMA controller will relinquish control of the bus after every transfer. If no other bus activity is initiated, another destination synchronized DMA cycle will begin after two processor clocks. This allows the destination device time to remove its request if another transfer is not desired. Since the DMA controller will relinquish the bus, the CPU can initiate a bus cycle. As a result, a complete bus cycle will often be inserted between destination synchronized transfers. Table 14 shows the maximum DMA transfer rates.

Table 14. Maximum DMA Transfer Rates @ CLKOUT = 8 MHz

Type of Synchronization Selected	CPU Running	CPU Halted
Unsynchronized	1.0 MBytes/sec	1.0 MBytes/sec
Source Synch	1.0 MBytes/sec	1.0 MBytes/sec
Destination Synch	0.67 MBytes/sec	0.80 MBytes/sec

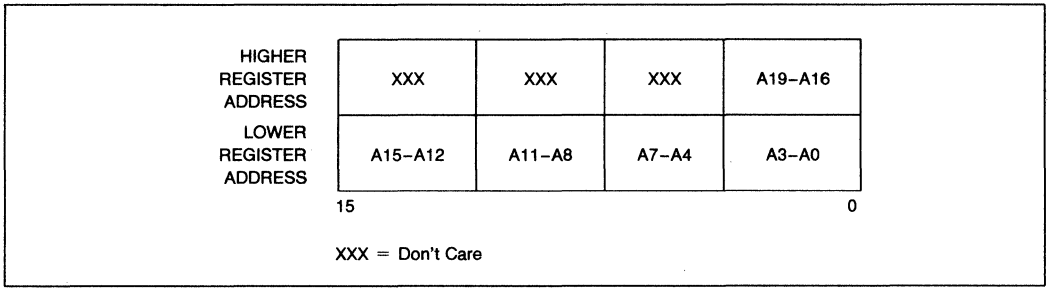

Figure 18. DMA Pointer Register Format

DMA Acknowledge

No explicit DMA acknowledge pulse is provided. Since both source and destination pointers are maintained, a read from a requesting source, or a write to a requesting destination, should be used as the DMA acknowledge signal. Since the chip-select lines can be programmed to be active for a given block of memory or I/O space, and the DMA pointers can be programmed to point to the same given block, a chip-select line could be used to indicate a DMA acknowledge.

DMA Priority

The DMA channels may be programmed to give one channel priority over the other, or they may be programmed to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses to odd memory locations; also, an external bus hold takes priority over an internal DMA cycle. Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time will suffer during sequences of continuous DMA cycles. An NMI request, however, will cause all internal DMA activity to halt. This allows the CPU to quickly respond to the NMI request.

DMA Programming

DMA cycles will occur whenever the ST/$\overline{\text{STOP}}$ bit of the Control Register is set. If synchronized transfers are programmed, a DRQ must also be generated. Therefore, the source and destination transfer pointers, and the transfer count register (if used) must be programmed before the ST/$\overline{\text{STOP}}$ bit is set.

Each DMA register may be modified while the channel is operating. If the CHG/$\overline{\text{NOCHG}}$ bit is cleared when the control register is written, the ST/$\overline{\text{STOP}}$ bit of the control register will not be modified by the write. If multiple channel registers are modified, it is recommended that a LOCKED string transfer be used to prevent a DMA transfer from occurring between updates to the channel registers.

DMA Channels and Reset

Upon RESET, the DMA channels will perform the following actions:

- The ST/$\overline{\text{STOP}}$ bit for each channel will be reset to STOP.
- Any transfer in progress is aborted.

TIMERS

The 80188 provides three internal 16-bit programmable timers (see Figure 19). Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

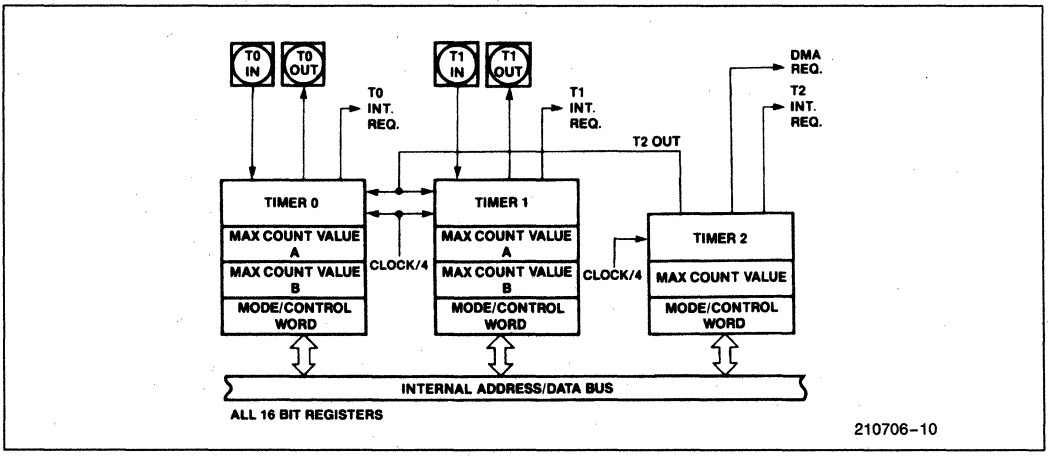

Figure 19. Timer Block Diagram

Timer Operation

The timers are controlled by 11 16-bit registers in the peripheral control block. The configuration of these registers is shown in Table 15. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a MAX COUNT register, which defines the maximum count the timer will reach. After reaching the MAX COUNT register value, the timer count value will reset to zero during that same clock, i.e., the maximum count value is never stored in the count register itself. Timers 0 and 1 are, in addition, equipped with a second MAX COUNT register, which enables the timers to alternate their count between two different MAX COUNT values. If a single MAX COUNT register is used, the timer output pin will switch LOW for a single clock, 2 clocks after the maximum count value has been reached. In the dual MAX COUNT register mode, the output pin will indicate which MAX COUNT register is currently in use, thus allowing nearly complete freedom in selecting waveform duty cycles. For the timers with two MAX COUNT registers, the RIU bit in the control register determines which is used for the comparison.

Each timer gets serviced every fourth CPU-clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU-clock rate (2 MHz for an 8 MHz CPU clock). Due to internal synchronization and pipelining of the timer circuitry, a timer output may take up to 6 clocks to respond to any individual clock or gate input.

Since the count registers and the maximum count registers are all 16 bits wide, 16 bits of resolution are provided. Any Read or Write access to the timers will add one wait state to the minimum four-clock bus cycle, however. This is needed to synchronize and coordinate the internal data flows between the internal timers and the internal bus.

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between MAX COUNT registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

These options are selectable via the timer mode/control word.

Timer Mode/Control Register

The mode/control register (see Figure 20) allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

Table 15. Timer Control Block Format

Register Name	Register Offset		
	Tmr. 0	Tmr. 1	Tmr. 2
Mode/Control Word	56H	5EH	66H
Max Count B	54H	5CH	not present
Max Count A	52H	5AH	62H
Count Register	50H	58H	60H

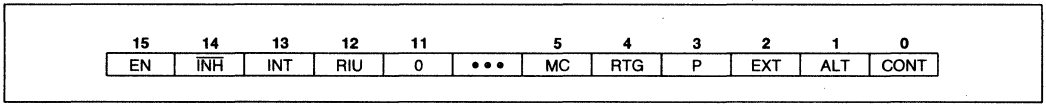

Figure 20. Timer Mode/Control Register

EN

The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transitions during the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

$\overline{\text{INH}}$

The inhibit bit allows for selective updating of the enable (EN) bit. If $\overline{\text{INH}}$ is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If $\overline{\text{INH}}$ is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT

When set, the INT bit enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual MAX COUNT register mode, an interrupt will be generated each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the Interrupt Controller.)

RIU

The Register In Use bit indicates which MAX COUNT register is currently being used for comparison to the timer count value. A zero value indicates register A. The RIU bit cannot be written, i.e., its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.

MC

The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. This bit is set regardless of the timer's interrupt-enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts. Programmer intervention is required to clear this bit.

RTG

Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is HIGH, the timer will count; if the input pin is LOW, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the 80188 clock.

When RTG = 1, the input pin detects LOW-to-HIGH transitions. The first such transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

P

The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

EXT

The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the 80188 clock. If this bit is set, the timer will count LOW-to-HIGH transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input to output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

ALT

The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method of generating non-repetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of

the timer output pin. If ALT is zero, the output pin will go LOW for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT

Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset, and halt.

Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Count Registers

Each of the three timers has a 16-bit count register. The contents of this register may be read or written by the processor at any time. If the register is written while the timer is counting, the new value will take effect in the current count cycle.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two max count values whenever the current maximum count is reached. A timer resets when the timer count register equals the max count value being used. If the timer count register or the max count register is changed so that the max count is less than the timer count, the timer does not immediately reset. Instead, the timer counts up to 0FFFFH, "wraps around" to zero, counts up to the max count value, and then resets.

Timers and Reset

Upon RESET, the Timers will perform the following actions:

- All EN (Enable) bits are reset preventing timer counting.
- For Timers 0 and 1, the RIU bits are reset to zero and the ALT bits are set to one. This results in the Timer Out pins going HIGH.

INTERRUPT CONTROLLER

The 80188 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The 80188 interrupt controller has its own control register that sets the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Figure 21.

The 80188 has a special Slave Mode in which the internal interrupt controller acts as a slave to an external master. The controller is programmed into this mode by setting bit 14 in the peripheral control block relocation register. (See Slave Mode section.)

MASTER MODE OPERATION

Interrupt Controller External Interface

Five pins are provided for external interrupt sources. One of these pins is NMI, the non-maskable interrupt. NMI is generally used for unusual events such as power-fail interrupts. The other four pins may be configured in any of the following ways:

- As four interrupt input lines with internally generated interrupt vectors.
- As an interrupt line and interrupt acknowledge line pair (Cascade Mode) with externally generated interrupt vectors plus two interrupt input lines with internally generated vectors.
- As two pairs of interrupt/interrupt acknowledge lines (Cascade Mode) with externally generated interrupt vectors.

External sources in the Cascade Mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the 80188 on the second cycle. The capability to interface to external 8259A programmable interrupt controllers is provided when the inputs are configured in Cascade Mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in Master Mode are similar to the 8259A. The interrupt controller responds identically to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

FULLY NESTED MODE

When in the fully nested mode four pins are used as direct interrupt requests as in Figure 22. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in-service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate with interrupts enabled, yet be suspended only by interrupts of higher priority than the in-service interrupt.

When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register. This is required to allow subsequent interrupts from this interrupt source and to allow servicing of lower-priority interrupts. An EOI command is executed at the end of the service routine just before the return from interrupt instruction. If the fully nested structure has been upheld, the next highest-priority source with its IS bit set is then serviced.

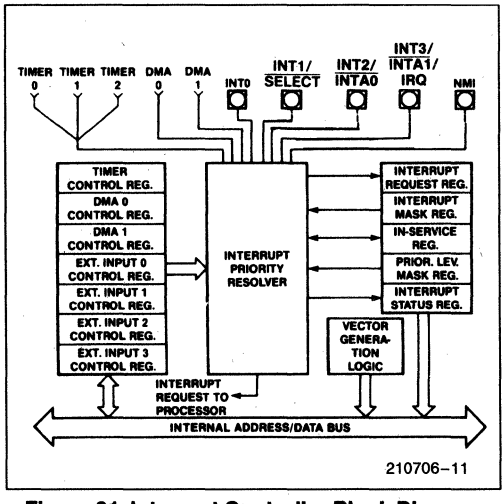

Figure 21. Interrupt Controller Block Diagram

CASCADE MODE

The 80188 has four interrupt pins and two of them have dual functions. In the fully nested mode the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In the Cascade Mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. The interconnection is shown in Figure 23. INT0 is an interrupt input interfaced to an 8259A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to that peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the Cascade Mode by programming the proper value into INT0 and INT1 control registers. The use of the dedicated acknowledge signals eliminates the need for the use of external logic to generate $\overline{\text{INTA}}$ and device select signals.

The primary Cascade Mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave 8259As. Three levels of priority are created, requiring priority resolution in the 80188 interrupt controller, the master 8259As, and the slave 8259As. If an external interrupt is serviced, one IS bit is set at each of these levels. When the interrupt service routine is completed, up to three end-of-interrupt commands must be issued by the programmer.

SPECIAL FULLY NESTED MODE

This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external 8259A masters. Normally, an interrupt request from an interrupt source will not be recognized unless the in-service bit for that source is reset. If more than one interrupt source is connected to an external interrupt controller, all of the interrupts will be funneled through the same 80188 interrupt request pin. As a result, if the external interrupt controller receives a higher-priority interrupt, its interrupt will not be recognized by the 80188 controller until the 80188 in-service bit is reset. In Special Fully Nested Mode, the 80188 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interrupts from a single pin. An in-service bit will continue to be set, however, to inhibit interrupts from other lower-priority 80188 interrupt sources.

Special procedures should be followed when resetting IS bits at the end of interrupt service routines. Software polling of the IS register in the external master 8259A is required to determine if there is more than one bit set. If so, the IS bit in the 80188 remains active and the next interrupt service routine is entered.

Operation in a Polled Environment

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the Poll Word (Figure 32). Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service. Bits 0–4 indicate to the processor the type vector of the highest-priority source requesting service. Reading the Poll Word causes the In-Service bit of the highest priority source to be set.

It is desirable to be able to read the Poll Word information without guaranteeing service of any pending interrupt, i.e., not set the indicated in-service bit. The 80188 provides a Poll Status Word in addition to the conventional Poll Word to allow this to be done. Poll Word information is duplicated in the Poll Status Word, but reading the Poll Status Word does not set the associated in-service bit. These words are located in two adjacent memory locations in the register file.

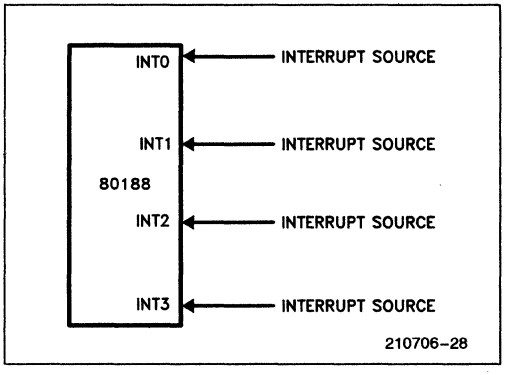

Figure 22. Fully Nested (Direct) Mode Interrupt Controller Connections

Master Mode Features

PROGRAMMABLE PRIORITY

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority). All interrupt sources have preprogrammed default priority levels (see Table 4).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 4 is used. If the serviced interrupt routine reenables interrupts, other interrupt requests can be serviced.

END-OF-INTERRUPT COMMAND

The end-of-interrupt (EOI) command is used by the programmer to reset the In-Service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The nonspecific command does not specify which IS bit is reset. When issued, the interrupt controller automatically resets the IS bit of the highest priority source with an active service routine. A specific EOI command requires that the programmer send the interrupt vector type to the interrupt controller indicating which source's IS bit is to be reset. This command is used when the fully nested structure has been disturbed or the highest priority IS bit that was set does not belong to the service routine in progress.

TRIGGER MODE

The four external interrupt pins can be programmed in either edge- or level-trigger mode. The control register for each external source has a level-trigger mode (LTM) bit. All interrupt inputs are active HIGH. In the edge sense mode or the level-trigger mode, the interrupt request must remain active (HIGH) until the interrupt request is acknowledged by the 80188 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go LOW for at least one clock cycle to re-enable the input. In the level-trigger mode, no such provision is made: holding the interrupt input HIGH will cause continuous interrupt requests.

INTERRUPT VECTORING

The 80188 Interrupt Controller will generate interrupt vectors for the integrated DMA channels and the integrated Timers. In addition, the Interrupt Controller will generate interrupt vectors for the external interrupt lines if they are not configured in Cascade or Special Fully Nested Modes. The interrupt vectors generated are fixed and cannot be changed (see Table 4).

Interrupt Controller Registers

The Interrupt Controller register model is shown in Figure 24. It contains 15 registers. All registers can both be read or written unless specified otherwise.

IN-SERVICE REGISTER

This register can be read from or written into. The format is shown in Figure 25. It contains the In-Service bit for each of the interrupt sources. The In-Service bit is set to indicate that a source's service routine is in progress. When an In-Service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the In-Service bit for all three timers; the D0 and D1 bits are the In-Service bits for the two DMA channels; the I0–I3 are the In-Service bits for the external interrupt pins. The IS bit is set when the processor acknowledges an interrupt request either by an interrupt acknowledge or by reading the poll register. The IS bit is reset at the end of the interrupt service routine by an end-of-interrupt command.

INTERRUPT REQUEST REGISTER

The internal interrupt sources have interrupt request bits inside the interrupt controller. The format of this register is shown in Figure 25. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

The state of the external interrupt input pins is also indicated. The state of the external interrupt pins is not a stored condition inside the interrupt controller, therefore the external interrupt bits cannot be written. The external interrupt request bits are set when an interrupt request is given to the interrupt controller, so if edge-triggered mode is selected, the bit in the register will be HIGH only after an inactive-to-active transition. For internal interrupt sources, the register bits are set when a request arrives and are reset when the processor acknowledges the requests.

Writes to to the interrupt request register will affect the D0 and D1 interrupt request bits. Setting either bit will cause the corresponding interrupt request while clearing either bit will remove the corresponding interrupt request. All other bits in the register are read-only.

MASK REGISTER

This is a 16-bit register that contains a mask bit for each interrupt source. The format for this register is shown in Figure 25. A one in a bit position corresponding to a particular source masks the source from generating interrupts. These mask bits are the exact same bits which are used in the individual control registers; programming a mask bit using the mask register will also change this bit in the individual control registers, and vice versa.

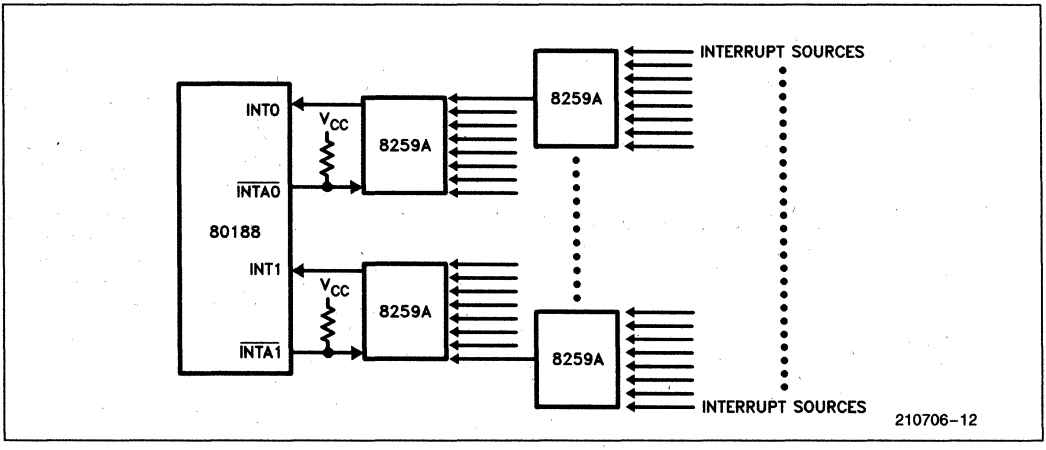

Figure 23. Cascade and Special Fully Nested Mode Interrupt Controller Connections

	OFFSET
INT3 CONTROL REGISTER	3EH
INT2 CONTROL REGISTER	3CH
INT1 CONTROL REGISTER	3AH
INT0 CONTROL REGISTER	38H
DMA 1 CONTROL REGISTER	36H
DMA 0 CONTROL REGISTER	34H
TIMER CONTROL REGISTER	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY MASK REGISTER	2AH
MASK REGISTER	28H
POLL STATUS REGISTER	26H
POLL REGISTER	24H
EOI REGISTER	22H

Figure 24. Interrupt Controller Registers (Master Mode)

PRIORITY MASK REGISTER

This register masks all interrupts below a particular interrupt priority level. The format of this register is shown in Figure 26. The code in the lower three bits of this register inhibits interrupts of priority lower (a higher priority number) than the code specified. For example, 100 written into this register masks interrupts of level five (101), six (110), and seven (111). The register is reset to seven (111) upon RESET so no interrupts are masked due to priority number.

INTERRUPT STATUS REGISTER

This register contains general interrupt controller status information. The format of this register is shown in Figure 27. The bits in the status register have the following functions:

DHLT: DMA Halt Transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed. This bit allows prompt service of all non-maskable interrupts. This bit may also be set by the programmer.

IRTx: These three bits represent the individual timer interrupt request bits. These bits differentiate between timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt requests. Note that setting any one of these three bits initiates an interrupt request to the interrupt controller.

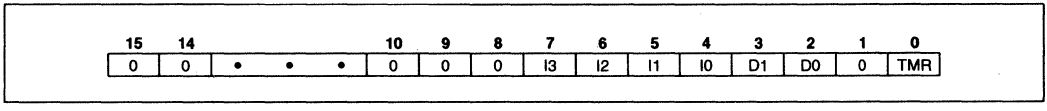

Figure 25. In-Service, Interrupt Request, and Mask Register Formats

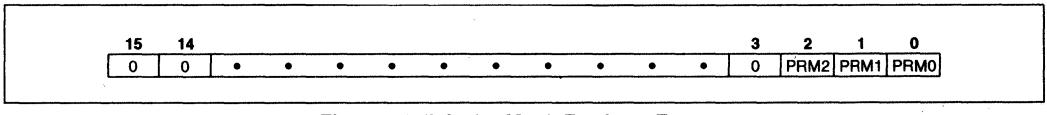

Figure 26. Priority Mask Register Format

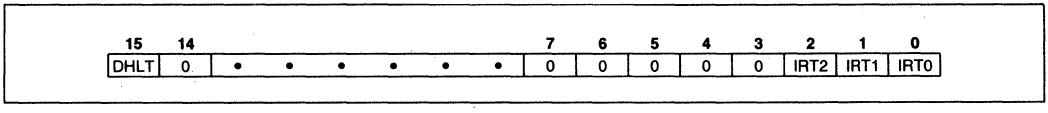

Figure 27. Interrupt Status Register Format (non-RMX Mode)

TIMER, DMA 0, 1; CONTROL REGISTERS

These registers are the control words for all the internal interrupt sources. The format for these registers is shown in Figure 28. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits interrupt requests from the interrupt source. The MSK bits in the individual control registers are the exact same bits as are in the Mask Register; modifying them in the individual control registers will also modify them in the Mask Register, and vice versa.

INT0-INT3 CONTROL REGISTERS

These registers are the control words for the four external input pins. Figure 29 shows the format of the INT0 and INT1 Control registers; Figure 30 shows the format of the INT2 and INT3 Control registers. In Cascade Mode or Special Fully Nested Mode, the control words for INT2 and INT3 are not used.

The bits in the various control registers are encoded as follows:

PRO-2: Priority programming information. Highest priority = 000, lowest priority = 111.

LTM: Level-trigger mode bit. 1 = level-triggered; 0 = edge-triggered. Interrupt Input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = non-mask.

C: Cascade mode bit, 1 = cascade; 0 = direct.

SFNM: Special Fully Nested Mode bit, 1 = SFNM.

EOI REGISTER

The end of the interrupt register is a command register which can only be written into. The format of this register is shown in Figure 31. It initiates an EOI command when written to by the 80188 CPU.

The bits in the EOI register are encoded as follows:

S_x: Encoded information that specifies an interrupt source vector type as shown in Table 4. For example, to reset the In-Service bit for DMA channel 0, these bits should be set to 01010, since the vector type for DMA channel 0 is 10.

NOTE:
To reset the single In-Service bit for any of the three timers, the vector type for timer 0 (8) should be written in this register.

NSPEC/SPEC: A bit that determines the type of EOI command. Nonspecific = 1, Specific = 0.

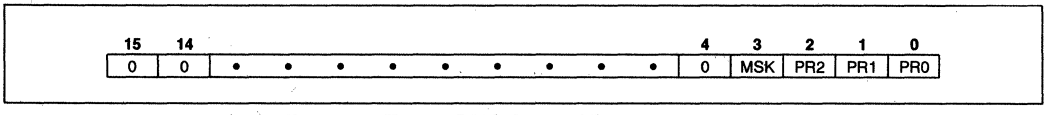

Figure 28. Timer/DMA Control Register Formats

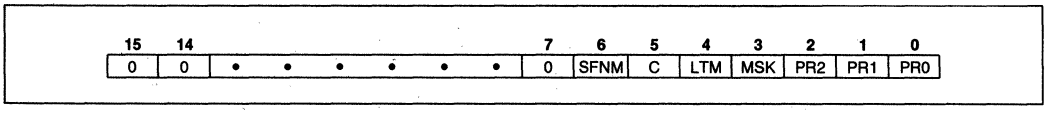

Figure 29. INT0/INT1 Control Register Formats

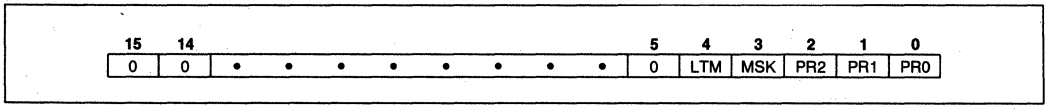

Figure 30. INT2/INT3 Control Register Formats

POLL AND POLL STATUS REGISTERS

These registers contain polling information. The format of these registers is shown in Figure 32. They can only be read. Reading the Poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt. Reading the poll status register will not set the IS bit of the highest priority pending interrupt; only the status of pending interrupts will be provided.

Encoding of the Poll and Poll Status register bits are as follows:

S_X: Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt Request = 1; no Interrupt Request = 0.

SLAVE MODE OPERATION

When Slave Mode is used, the internal 80188 interrupt controller will be used as a slave controller to an external master interrupt controller. The internal 80188 resources will be monitored by the internal interrupt controller, while the external controller functions as the system master interrupt controller. Upon reset, the 80188 will be in Master Mode. To provide for slave mode operation bit 14 of the relocation register should be set.

Because of pin limitations caused by the need to interface to an external 8259A master, the internal interrupt controller will no longer accept external inputs. There are however, enough 80188 interrupt controller inputs (internally) to dedicate one to each timer. In this mode, each timer interrupt source has its own mask bit, IS bit, and control word.

In Slave Mode each peripheral must be assigned a unique priority to ensure proper interrupt controller operation. Therefore, it is the programmer's responsibility to assign correct priorities and initialize interrupt control regisers before enable interrupts.

Slave Mode External Interface

The configuration of the 80188 with respect to an external 8259A master is shown in Figure 33. The INT0 (pin 45) input is used as the 80188 CPU interrupt input. IRQ (pin 41) functions as an output to send the 80188 slave-interrupt-request to one of the 8 master-PIC-inputs.

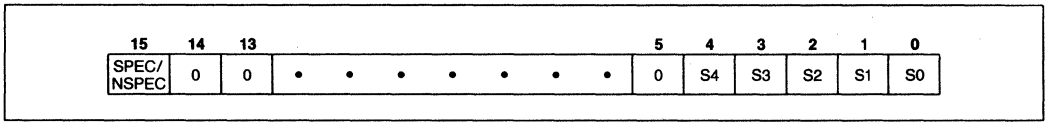

Figure 31. EOI Register Format

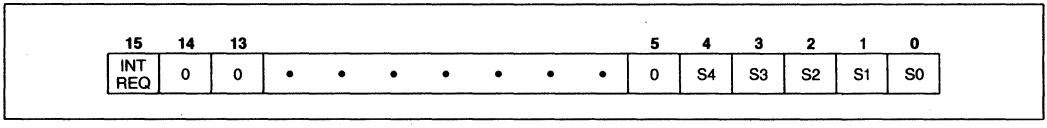

Figure 32. Poll and Poll Status Register Format

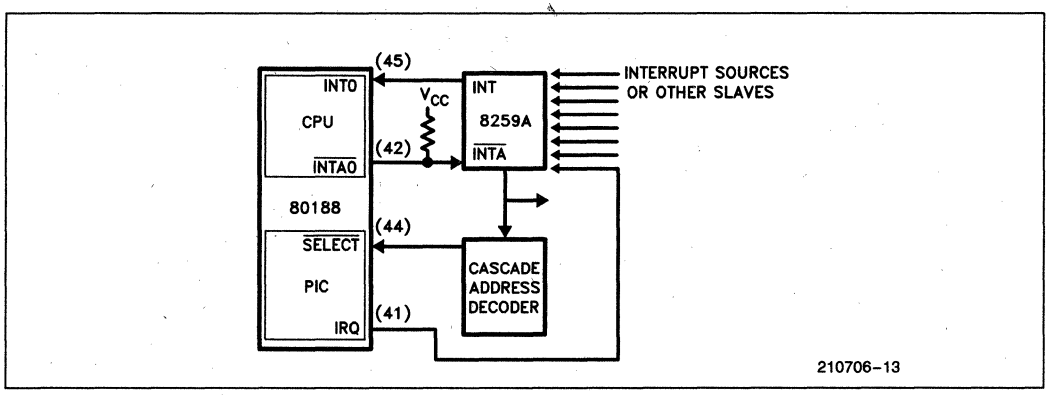

Figure 33. Slave Mode Interrupt Controller Connections

Correct master-slave interface requires decoding of the slave addresses (CAS0–2). Slave 8259As do this internally. Because of pin limitations, the 80188 slave address will have to be decoded externally. $\overline{\text{SELECT}}$ (pin 44) is used as a slave-select input. Note that the slave vector address is transferred internally, but the READY input must be supplied externally.

$\overline{\text{INTA0}}$ (pin 42) is used as an acknowledge output, suitable to drive the $\overline{\text{INTA}}$ input of an 8259A.

Interrupt Nesting

Slave Mode operation allows nesting of interrupt requests. When an interrupt is acknowledged, the priority logic masks off all priority levels except those with equal or higher priority.

Vector Generation in the Slave Mode

Vector generation in Slave Mode is exactly like that of an 8259A or 82C59A slave. The interrupt controller generates an 8-bit vector type number which the CPU multiplies by four to use as an address into the vector table. The five most significant bits of this type number are user-programmable while the three least significant bits are defined according to Figure 34. The significant five bits of the vector are programmed by writing to the Interrupt Vector register at offset 20H.

Specific End-of-Interrupt

In Slave Mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset. The command is executed by writing the correct value in the Specific EOI register at offset 22H.

Interrupt Controller Registers in the Slave Mode

All control and command registers are located inside the internal peripheral control block. Figure 34 shows the offsets of these registers.

END-OF-INTERRUPT REGISTER

The end-of-interrupt register is a command register which can only be written. The format of this register is shown in Figure 35. It initiates an EOI command when written by the 80188 CPU.

The bits in the EOI register are encoded as follows:

VT_X: Three least-significant vector type bits corresponding to the source for which the IS bit is to be reset. Figure 34 indicates these bits.

IN-SERVICE REGISTER

This register can be read from or written into. It contains the in-service bit for each of the internal interrupt sources. The format for this register is shown in Figure 36. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers. The source's IS bit is set when the processor acknowledges its interrupt request.

INTERRUPT REQUEST REGISTER

This register indicates which internal peripherals have interrupt requests pending. The format of this register is shown in Figure 36. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request. As in Master Mode, D0 and D1 are read/write, all other bits are read only.

MASK REGISTER

This register contains a mask bit for each interrupt source. The format for this register is shown in Figure 36. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked. These mask bits are exactly the same bits which are used in the individual control registers, i.e., changing the state of a mask bit in this register will also change the state of a mask bit in the individual interrupt control register corresponding to the bit.

CONTROL REGISTERS

These registers are the control words for all the internal interrupt sources. The format of these registers is shown in Figure 37. Each of the timers and both of the DMA channels have their own Control Register.

The bits of the Control Registers are encoded as follows:

pr_x: 3-bit encoded field indicating a priority level for the source.

msk: mask bit for the priority level indicated by pr_x bits.

	OFFSET
TIMER 2 CONTROL REGISTER (VECTOR TYPE xxxxx 101)	3AH
TIMER 1 CONTROL REGISTER (VECTOR TYPE xxxxx 100)	38H
DMA 1 CONTROL REGISTER (VECTOR TYPE xxxxx 011)	36H
DMA 0 CONTROL REGISTER (VECTOR TYPE xxxxx 010)	34H
TIMER 0 CONTROL REGISTER (VECTOR TYPE xxxxx 000)	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY-LEVEL MASK REGISTER	2AH
MASK REGISTER	28H
SPECIFIC EOI REGISTER	22H
INTERRUPT VECTOR REGISTER	20H

Figure 34. Interrupt Controller Registers (Slave Mode)

24

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	0	0	0	VT2	VT1	VT0

Figure 35. Specific EOI Register Format

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	TMR2	TMR1	D1	D0	0	TMR0

Figure 36. In-Service, Interrupt Request, and Mask Register Format

INTERRUPT VECTOR REGISTER

This register provides the upper five bits of the interrupt vector address. The format of this register is shown in Figure 38. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.

The format of the bits in this register is:

t_x: 5-bit field indicating the upper five bits of the vector address.

PRIORITY-LEVEL MASK REGISTER

This register indicates the lowest priority-level interrupt which will be serviced.

The encoding of the bits in this register is:

m_x: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

INTERRUPT STATUS REGISTER

This register is defined as in Master Mode except that DHLT is not implemented. (See Figure 27).

Interrupt Controller and Reset

Upon RESET, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying Fully Nested Mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All Interrupt Service bits reset to 0.
- All Interrupt Request bits reset to 0.
- All MSK (Interrupt Mask) bits set to 1 (mask).
- All C (Cascade) bits reset to 0 (non-Cascade).
- All PRM (Priority Mask) bits set to 1, implying no levels masked.
- Initialized to Master Mode.

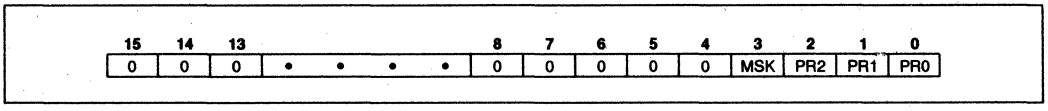

Figure 37. Control Word Format

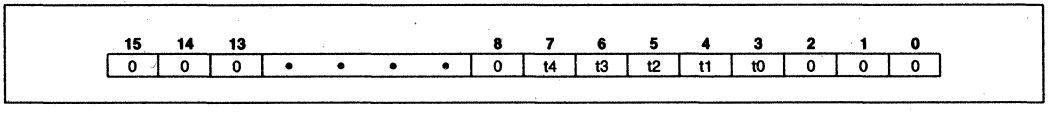

Figure 38. Interrupt Vector Register Format

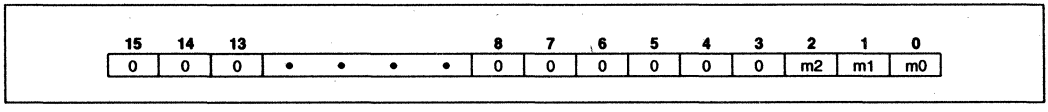

Figure 39. Priority Level Mask Register

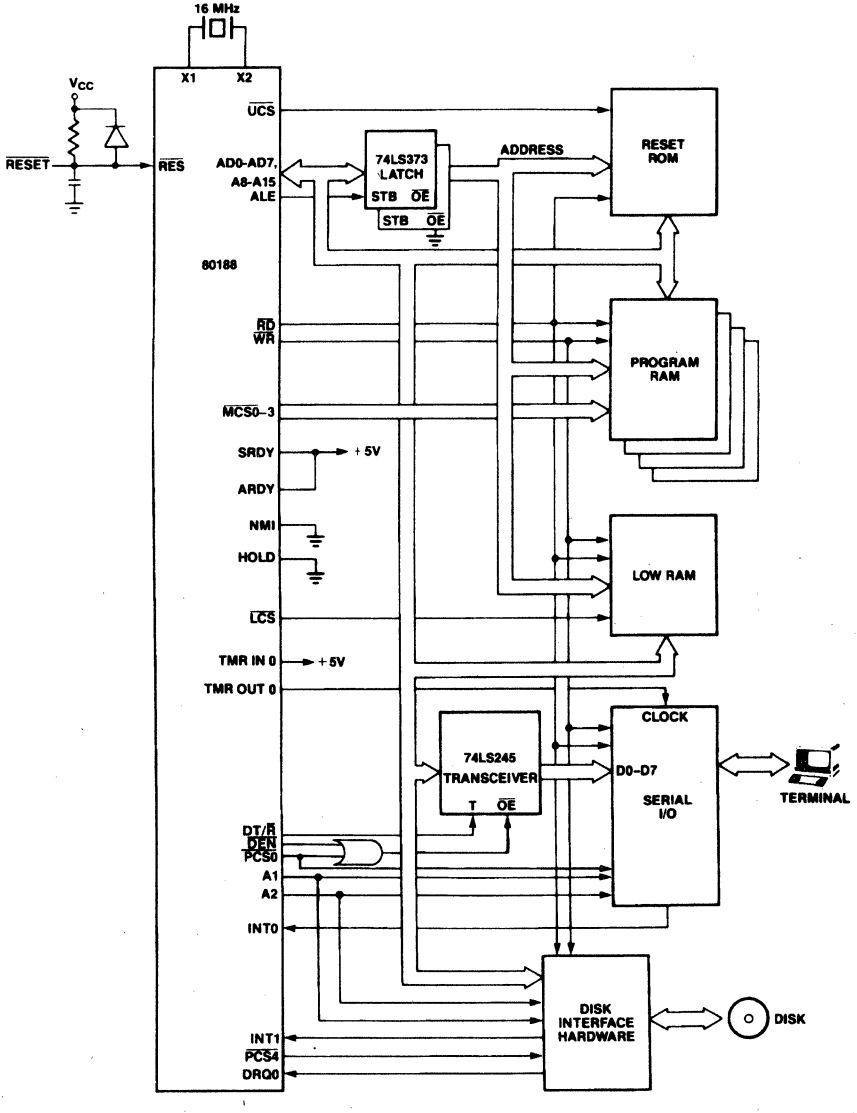

Figure 40. Typical 80188 Computer

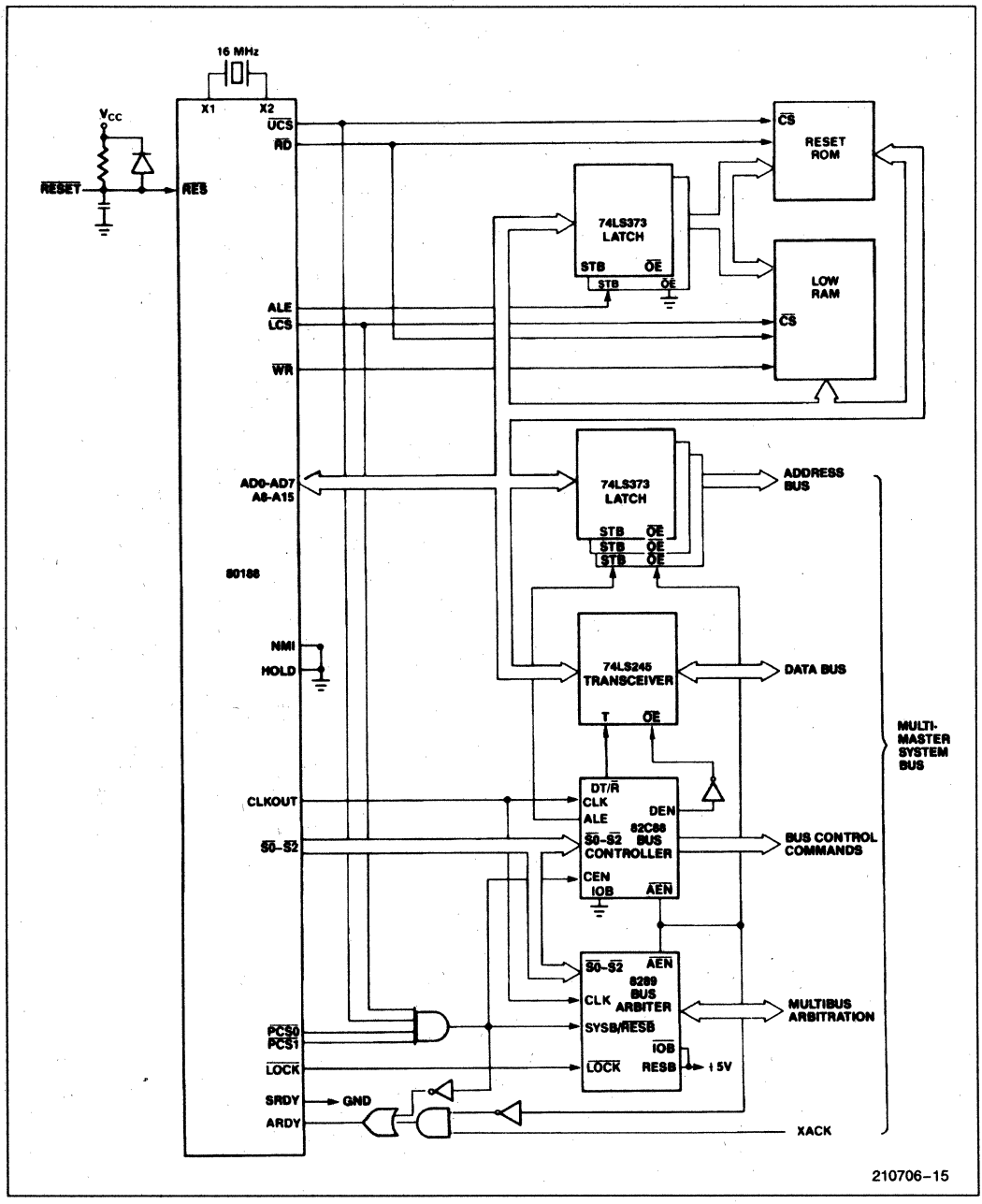

Figure 41. Typical 80188 Multi-Master Bus Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on any Pin with
Respect to Ground.....−1.0V to +7V
Power Dissipation .....3 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

Applicable to 80188 (8 MHz)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage (All except X1 and $\overline{RES}$)	2.0	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC} + 0.5	V	
V_{CLI}	X1 Input Low Voltage	−0.5	0.6	V	
V_{CHI}	X1 Input High Voltage	3.9	V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage		0.45	V	I_a = 2.5 mA for $\overline{S0}$–$\overline{S2}$ I_a = 2.0 mA for all other outputs
V_{OH}	Output High Voltage	2.4		V	I_{oa} = −400 μA
I_{CC}	Power Supply Current		600*	mA	T_A = −40°C
			550	mA	T_A = 0°C
			415	mA	T_A = +70°C
I_{LI}	Input Leakage Current		±10	μA	0V < V_{IN} < V_{CC}
I_{LO}	Output Leakage Current		±10	μA	0.45V < V_{OUT} < V_{CC}
V_{CLO}	Clock Output Low		0.6	V	I_a = 4.0 mA
V_{CHO}	Clock Output High	4.0		V	I_{oa} = −200 μA
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		20	pF	

*For extended temperature parts only.

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PIN TIMINGS

A.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

80188 Timing Requirements All Timings Measured At 1.5 Volts Unless Otherwise Noted

Symbol	Parameter	80188 (8 MHz)		Units	Test Conditions
		Min	Max		
T_{DVCL}	Data in Setup (A/D)	20		ns	
T_{CLDX}	Data in Hold (A/D)	10		ns	
T_{ARYHCH}	Asynchronous Ready (ARDY) active setup time(1)	20		ns	
T_{ARYLCL}	ARDY inactive setup time	35		ns	
T_{CLARX}	ARDY hold time	15		ns	
T_{ARYCHL}	Asynchronous Ready inactive hold time	15		ns	
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(2)	20		ns	
T_{CLSRY}	SRDY Transition Hold Time(2)	15		ns	
T_{HVCL}	HOLD Setup(1)	25		ns	
T_{INVCH}	INTR, NMI, $\overline{TEST}$, TMR IN, Setup(1)	25		ns	
T_{INVCL}	DRQ0, DRQ1, Setup(1)	25		ns	
80188 Master Interface Timing Responses					
T_{CLAV}	Address Valid Delay	5	55	ns	C_L = 20–200 pF all outputs (except T_{CLTMV}) @ 8 MHz
T_{CLAX}	Address Hold	10		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	35	ns	
T_{CHCZ}	Command Lines Float Delay		45	ns	
T_{CHCV}	Command Lines Valid Delay (after float)		55	ns	
T_{LHLL}	ALE Width	$T_{CLCL}-35$		ns	
T_{CHLH}	ALE Active Delay		35	ns	
T_{CHLL}	ALE Inactive Delay		35	ns	
T_{LLAX}	Address Hold to ALE Inactive	$T_{CHCL}-25$		ns	
T_{CLDV}	Data Valid Delay	10	44	ns	
T_{CLDOX}	Data Hold Time	10		ns	
T_{WHDX}	Data Hold after WR	$T_{CLCL}-40$		ns	
T_{CVCTV}	Control Active Delay 1	5	50	ns	
T_{CHCTV}	Control Active Delay 2	10	55	ns	
T_{CVCTX}	Control Inactive Delay	5	55	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycle)	10	70	ns	

1. To guarantee recognition at next clock.
2. To guarantee proper operation.

PIN TIMINGS (Continued)

A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5V ±10%) (Continued)

80188 Master Interface Timing Responses (Continued)

Symbol	Parameter	80188 (8 MHz)		Units	Test Conditions
		Min	Max		
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	10	70	ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	10	55	ns	
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	$T_{CLCL}-40$		ns	
T_{CLHAV}	HLDA Valid Delay	5	50	ns	
T_{RLRH}	$\overline{RD}$ Width	$2T_{CLCL}-50$		ns	
T_{WLWH}	$\overline{WR}$ Width	$2T_{CLCL}-40$		ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH}-25$		ns	
T_{CHSV}	Status Active Delay	10	55	ns	
T_{CLSH}	Status Inactive Delay	10	65	ns	
T_{CLTMV}	Timer Output Delay		60	ns	100 pF max
T_{CLRO}	Reset Delay		60	ns	
T_{CHQSV}	Queue Status Delay		35	ns	
T_{CHDX}	Status Hold Time	10		ns	
T_{AVCH}	Address Valid to Clock High	10		ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	5	65	ns	
80188 Chip-Select Timing Responses					
T_{CLCSV}	Chip-Select Active Delay		66	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	35		ns	
T_{CHCSX}	Chip-Select Inactive Delay	5	35	ns	
80188 CLKIN Requirements					
T_{CKIN}	CLKIN Period	62.5	250	ns	
T_{CKHL}	CLKIN Fall Time		10	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		10	ns	1.0 to 3.5V
T_{CLCK}	CLKIN Low Time	25		ns	1.5V
T_{CHCK}	CLKIN High Time	25		ns	1.5V

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PIN TIMINGS (Continued)

A.C. CHARACTERISTICS (Continued)

(T_A = 0°C to +70°C, V_{CC} = 5V ±10%) (Continued)

80188 CLKOUT Timing (200 pF load)

Symbol	Parameter	80188 (8 MHz)		Units	Test Conditions
		Min	Max		
T_{CICO}	CLKIN to CLKOUT Skew		50	ns	
T_{CLCL}	CLKOUT Period	125	500	ns	
T_{CLCH}	CLKOUT Low Time	$\frac{1}{2}T_{CLCL}-7.5$		ns	1.5V
T_{CHCL}	CLKOUT High Time	$\frac{1}{2}T_{CLCL}-7.5$		ns	1.5V
T_{CH1CH2}	CLKOUT Rise Time		15	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		15	ns	3.5 to 1.0V

Explanation of the AC Symbols

Each timing symbol has from 5 to 7 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

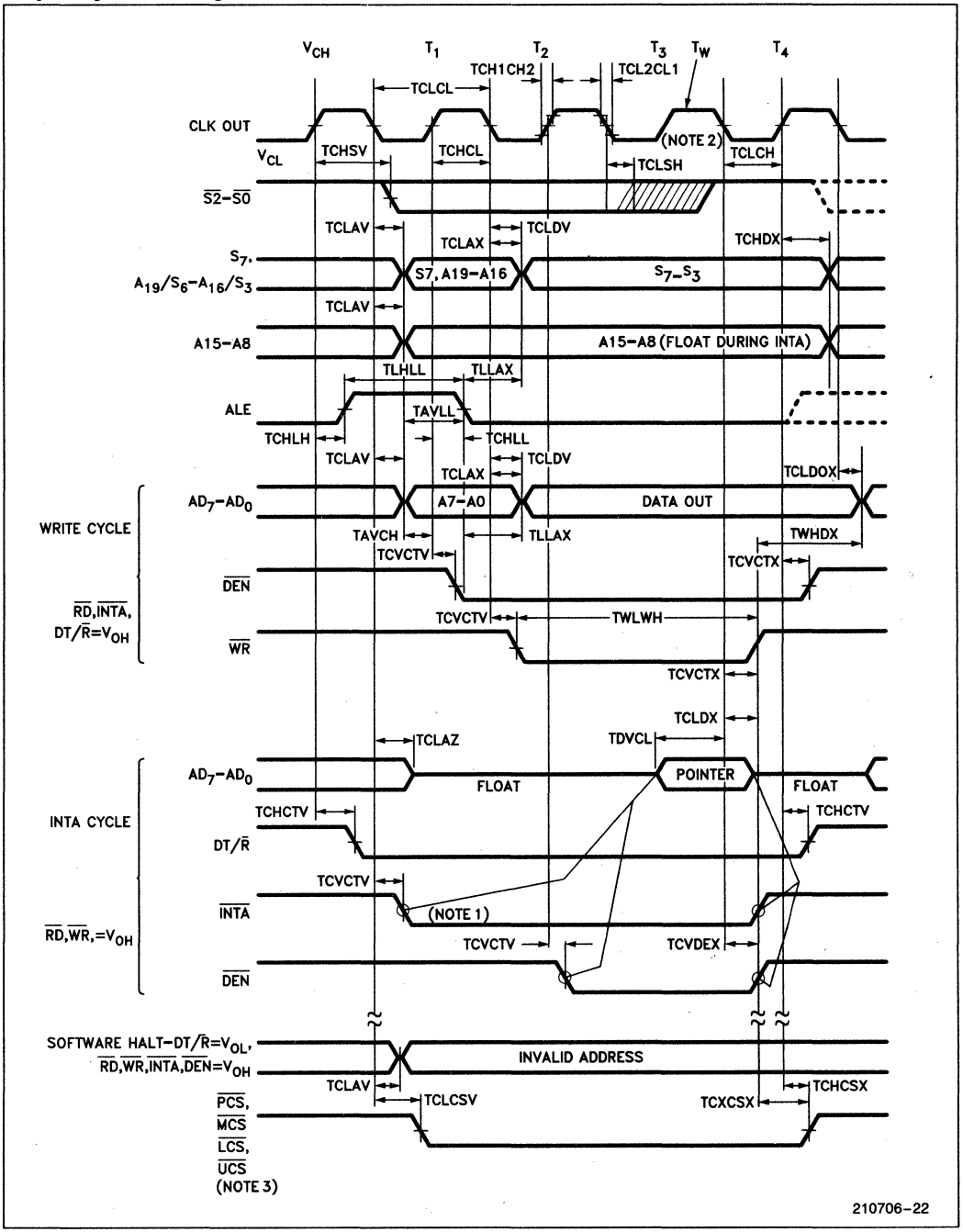
A: Address
ARY: Asynchronous Ready Input
C: Clock Output
CK: Clock Input
CS: Chip Select
CT: Control (DT/$\overline{R}$, $\overline{DEN}$, . . .)
D: Data Input
DE: $\overline{DEN}$
H: Logic Level High
IN: Input (DRQ0, TIM0, . . .)
L: Logic Level Low or ALE
O: Output
QS: Queue Status (QS1, QS2)
R: $\overline{RD}$ Signal, RESET Signal
S: Status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$)
SRY: Synchronous Ready Input
V: Valid
W: WR Signal
X: No Longer a Valid Logic Level
Z: Float

Examples:

T_{CLAV}— Time from Clock Low to Address Valid
T_{CHLH}— Time from Clock High to ALE High
T_{CLCSV}— Time from Clock LOW to Chp Select Valid

WAVEFORMS

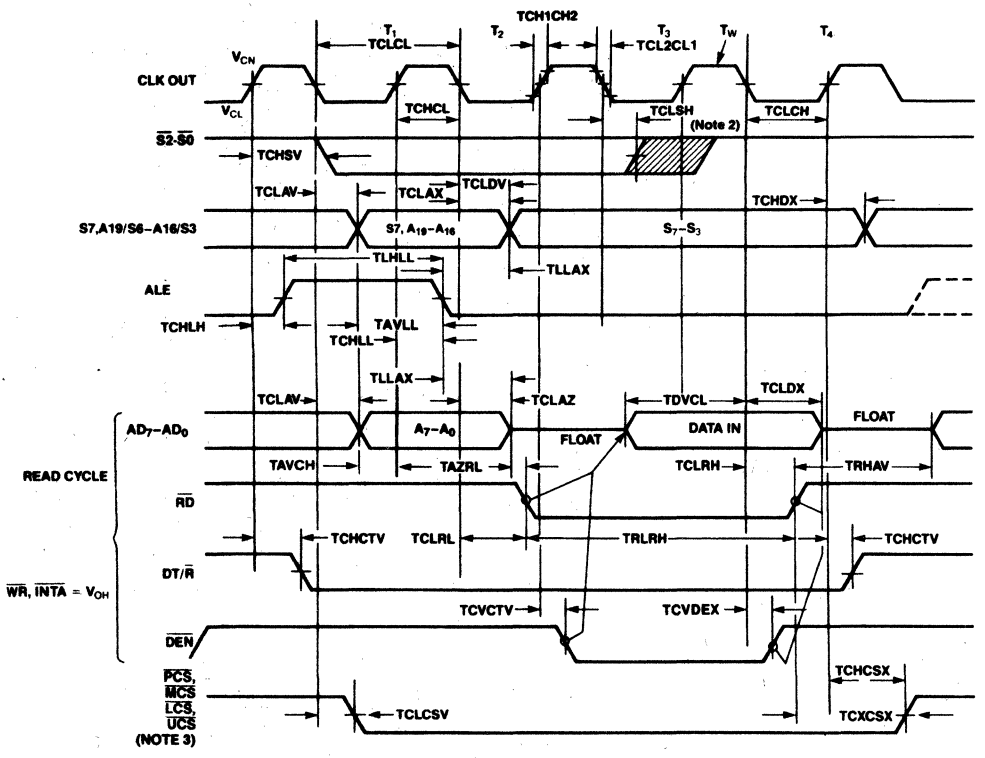
Major Cycle Timing



210706-22

WAVEFORMS (Continued)

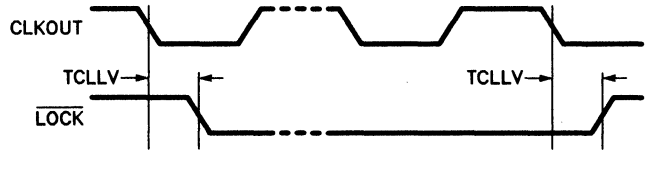
Major Cycle Timing (Continued)



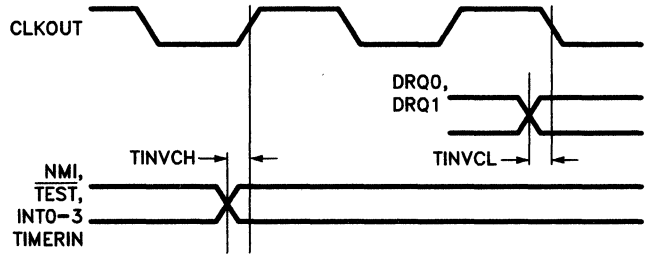
210706-23

NOTES:
1. INTA occurs one clock later in Slave Mode.
2. Status inactive just prior to T_4.
3. If latched A1 and A2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.

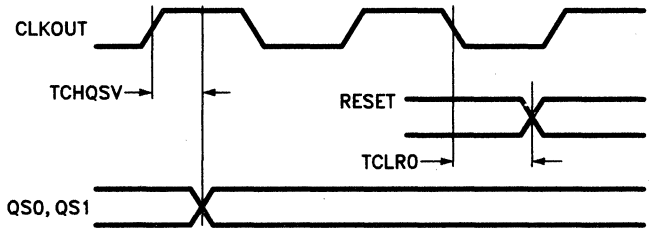
WAVEFORMS (Continued)



210706-30



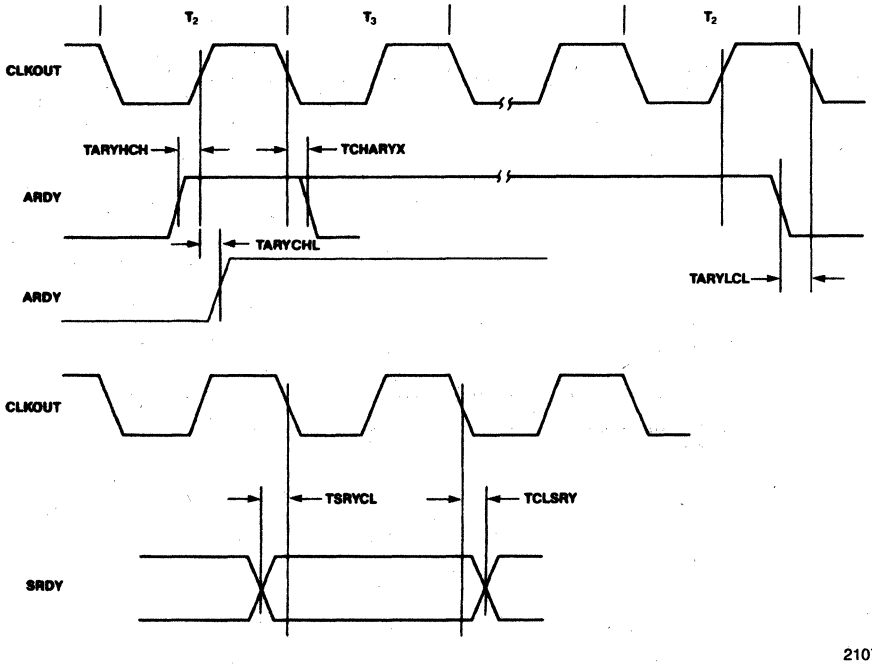
210706-31



210706-32

WAVEFORMS (Continued)

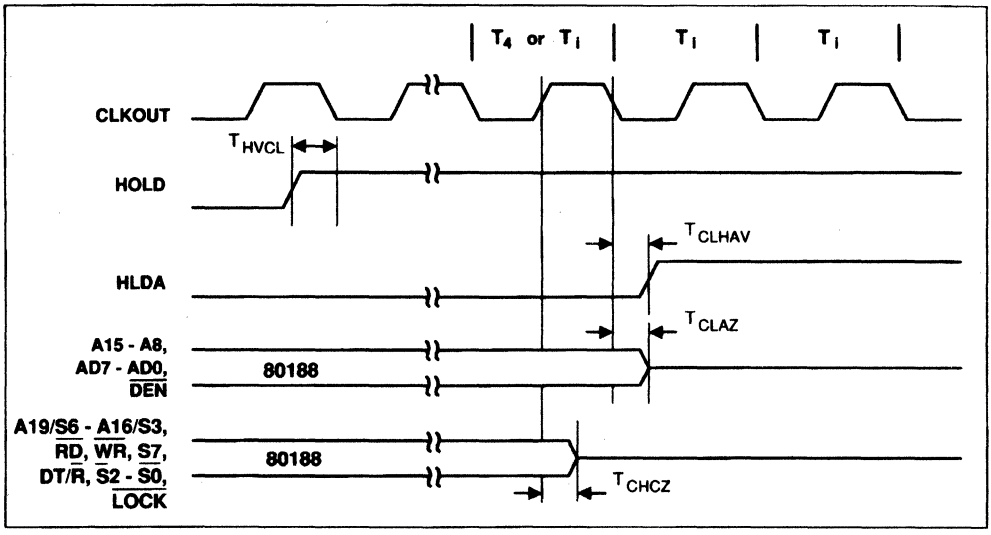
READY TIMING



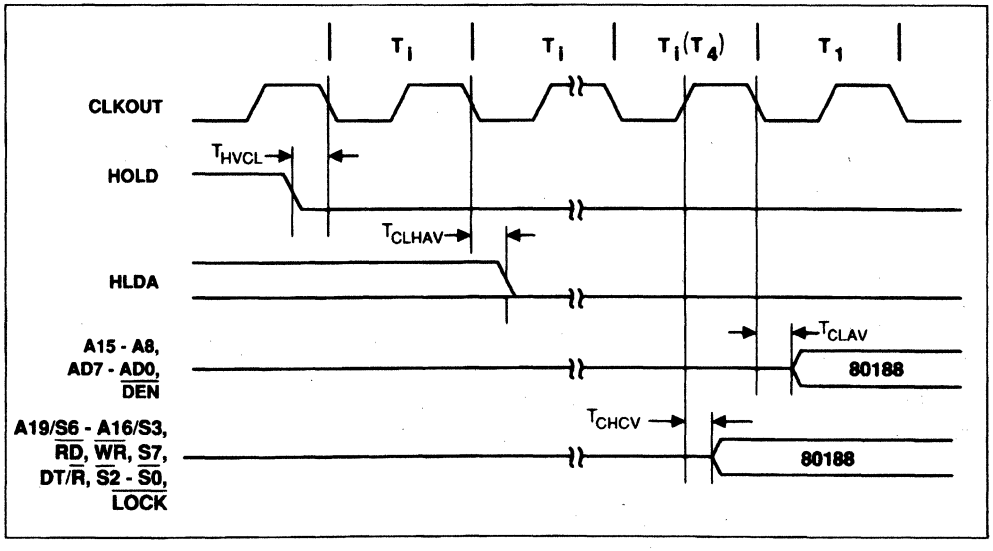
210706-29

WAVEFORMS (Continued)

HOLD/HLDA TIMING (Entering Hold)



HOLD/HLDA TIMING (Leaving Hold)



210706-33

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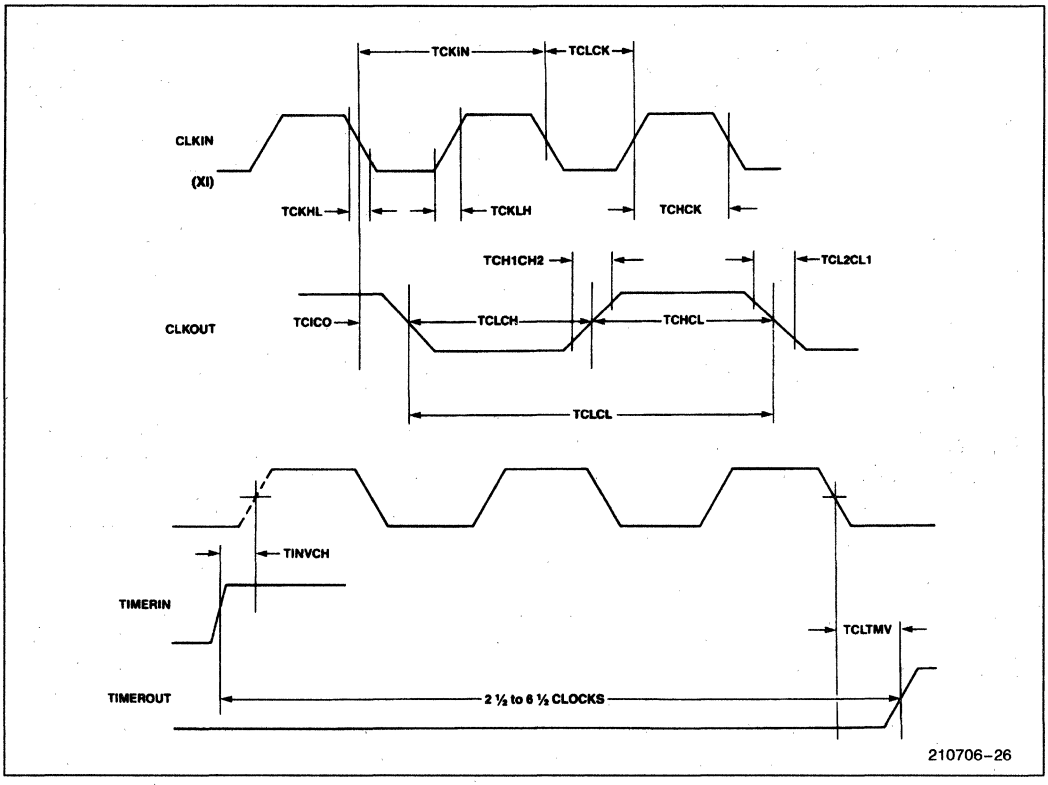
WAVEFORMS (Continued)

Timer On 80188



80188 EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the 80188 microprocessor. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The EXPRESS program includes the commercial standard temperature range with burn-in and an extended temperature range without burn-in.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

The optional burn-in is dynamic, for a minimum time of 160 hours at 125°C with V_{CC} = 5.5V ±0.25V, following guidelines in MIL-STD-883, Method 1015.

Package types and EXPRESS versions are identified by a one or two-letter prefix to the part number. The prefixes are listed in Table 16. All AC and DC specifications not mentioned in this section are the same for both commercial and EXPRESS parts.

Table 16. Prefix Identification

Prefix	Package Type	Temperature Range	Burn-In
A	PGA	Commercial	No
N	PLCC	Commercial	No
R	LCC	Commercial	No
TA	PGA	Extended	No
QR	LCC	Commercial	Yes

NOTE:
Not all package/temperature range combinations are available.

80188 EXECUTION TIMINGS

A determination of 80188 program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.

All instructions which involve memory accesses can also require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the Bus Interface Unit (BIU) and execution unit.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

The 80188 8-bit BIU is noticeably limited in its performance relative to the execution unit. A sufficient number of prefetched bytes may not reside in the prefetch queue much of the time. Therefore, actual program execution time may be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to register/memory	1000100w	mod reg r/m			2/12*	
Register/memory to register	1000101w	mod reg r/m			2/9*	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12/13*	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3/4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8*	
Accumulator to memory	1010001w	addr-low	addr-high		9*	
Register/memory to segment register	10001110	mod 0 reg r/m			2/13	
Segment register to register/memory	10001100	mod 0 reg r/m			2/15	
PUSH = Push:						
Memory	11111111	mod 1 1 0 r/m			20	
Register	01010 reg				14	
Segment register	000reg110				13	
Immediate	011010s0	data	data if s=0		14	
PUSHA = Push All	01100000				68	
POP = Pop:						
Memory	10001111	mod 0 0 0 r/m			24	
Register	01011 reg				14	
Segment register	000reg111	(reg≠01)			12	
POPA = Pop All	01100001				83	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17*	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10*	
Variable port	1110110w				8*	
OUT = Output to:						
Fixed port	1110011w	port			9*	
Variable port	1110111w				7*	
XLAT = Translate byte to AL	11010111				15	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		26	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		26	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				13	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.
*Note: Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
POPF = Pop flags	10011101				12	
SEGMENT = **Segment Override:**						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = **Add:**						
Reg/memory with register to either	000000dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16*	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = **Add with carry:**						
Reg/memory with register to either	000100dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16*	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = **Increment:**						
Register/memory	1111111w	mod 000 r/m			3/15*	
Register	01000 reg				3	
SUB = **Subtract:**						
Reg/memory and register to either	001010dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16*	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = **Subtract with borrow:**						
Reg/memory and register to either	000110dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16*	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = **Decrement:**						
Register/memory	1111111w	mod 001 r/m			3/15*	
Register	01001 reg				3	
CMP = **Compare:**						
Register/memory with register	0011101w	mod reg r/m			3/10*	
Register with register/memory	0011100w	mod reg r/m			3/10*	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10*	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10*	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.
*Note: Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
ARITHMETIC (Continued)			
MUL = Multiply (unsigned):	1111011w | mod 100 r/m		
Register-Byte		26–28	
Register-Word		35–37	
Memory-Byte		32–34	
Memory-Word		41–43*	
IMUL = Integer multiply (signed):	1111011w | mod 101 r/m		
Register-Byte		25–28	
Register-Word		34–37	
Memory-Byte		31–34	
Memory-Word		40–43*	
IMUL = Integer immediate multiply (signed)	011010s1 | mod reg r/m | data | data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w | mod 110 r/m		
Register-Byte		29	
Register-Word		38	
Memory-Byte		35	
Memory-Word		44*	
IDIV = Integer divide (signed):	1111011w | mod 111 r/m		
Register-Byte		44–52	
Register-Word		53–61	
Memory-Byte		50–58	
Memory-Word		59–67*	
AAM = ASCII adjust for multiply	11010100 | 00001010	19	
AAD = ASCII adjust for divide	11010101 | 00001010	15	
CBW = Convert byte to word	10011000	2	
CWD = Convert word to double word	10011001	4	
LOGIC **Shift/Rotate Instructions:**			
Register/Memory by 1	1101000w | mod TTT r/m	2/15	
Register/Memory by CL	1101001w | mod TTT r/m	5+n/17+n	
Register/Memory by Count	1100000w | mod TTT r/m | count	5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR		
AND = And:			
Reg/memory and register to either	001000dw | mod reg r/m	3/10*	
Immediate to register/memory	1000000w | mod 100 r/m | data | data if w=1	4/16*	
Immediate to accumulator	0010010w | data | data if w=1	3/4	8/16-bit

Shaded areas indicate instructions not available in 8086, 8088 microsystems.
*Note: Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
TEST = And function to flags, no result:						
Register/memory and register	1000010w	mod reg r/m			3/10*	
Immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	4/10*	
Immediate data and accumulator	1010100w	data	data if w=1		3/4	8/16-bit
OR = Or:						
Reg/memory and register to either	000010dw	mod reg r/m			3/10*	
Immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0000110w	data	data if w=1		3/4	8/16-bit
XOR = Exclusive or:						
Reg/memory and register to either	001100dw	mod reg r/m			3/10*	
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0011010w	data	data if w=1		3/4	8/16-bit
NOT = Invert register/memory	1111011w	mod 010 r/m			3/10*	
STRING MANIPULATION:						
MOVS = Move byte/word	1010010w				14*	
CMPS = Compare byte/word	1010011w				22*	
SCAS = Scan byte/word	1010111w				15*	
LODS = Load byte/wd to AL/AX	1010110w				12*	
STOS = Store byte/wd from AL/AX	1010101w				10*	
INS = Input byte/wd from DX port	0110110w				14	
OUTS = Output byte/wd to DX port	0110111w				14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	11110010	1010010w			8+8n*	
CMPS = Compare string	1111001z	1010011w			5+22n*	
SCAS = Scan string	1111001z	1010111w			5+15n*	
LODS = Load string	11110010	1010110w			6+11n*	
STOS = Store string	11110010	1010101w			6+9n*	
INS = Input string	11110010	0110110w			8+8n*	
OUTS = Output string	11110010	0110111w			8+8n*	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.
*Note: Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
CONTROL TRANSFER			
CALL = Call:			
Direct within segment	11101000 | disp-low | disp-high	19	
Register/memory indirect within segment	11111111 | mod 0 1 0 r/m	17/27	
Direct intersegment	10011010 | segment offset segment selector	31	
Indirect intersegment	11111111 | mod 0 1 1 r/m (mod ≠ 11)	54	
JMP = Unconditional jump:			
Short/long	11101011 | disp-low	14	
Direct within segment	11101001 | disp-low | disp-high	14	
Register/memory indirect within segment	11111111 | mod 1 0 0 r/m	11/21	
Direct intersegment	11101010 | segment offset segment selector	14	
Indirect intersegment	11111111 | mod 1 0 1 r/m (mod ≠ 11)	34	
RET = Return from CALL:			
Within segment	11000011	20	
Within seg adding immed to SP	11000010 | data-low | data-high	22	
Intersegment	11001011	30	
Intersegment adding immediate to SP	11001010 | data-low | data-high	33	
JE/JZ = Jump on equal/zero	01110100 | disp	4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100 | disp	4/13	
JLE/JNG = Jump on less or equal/not greater	01111110 | disp	4/13	
JB/JNAE = Jump on below/not above or equal	01110010 | disp	4/13	
JBE/JNA = Jump on below or equal/not above	01110110 | disp	4/13	
JP/JPE = Jump on parity/parity even	01111010 | disp	4/13	
JO = Jump on overflow	01110000 | disp	4/13	
JS = Jump on sign	01111000 | disp	4/13	
JNE/JNZ = Jump on not equal/not zero	01110101 | disp	4/13	
JNL/JGE = Jump on not less/greater or equal	01111101 | disp	4/13	
JNLE/JG = Jump on not less or equal/greater	01111111 | disp	4/13	
JNB/JAE = Jump on not below/above or equal	01110011 | disp	4/13	
JNBE/JA = Jump on not below or equal/above	01110111 | disp	4/13	
JNP/JPO = Jump on not par/par odd	01111011 | disp	4/13	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.
*Note: Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
CONTROL TRANSFER (Continued)			
JNO = Jump on not overflow	01110001 | disp	4/13	
JNS = Jump on not sign	01111001 | disp	4/13	
JCXZ = Jump on CX zero	11100011 | disp	5/15	
LOOP = Loop CX times	11100010 | disp	6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001 | disp	6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000 | disp	6/16	
ENTER = Enter Procedure	11001000 | data-low | data-high | L		
L = 0		19	
L = 1		29	
L > 1		26+20(n−1)	
LEAVE = Leave Procedure	11001001	8	
INT = Interrupt:			
Type specified	11001101 | type	47	
Type 3	11001100	45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110	48/4	
IRET = Interrupt return	11001111	28	
BOUND = Detect value out of range	01100010 | mod reg r/m	33–35	
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
ESC = Processor Extension Escape	11011TTT | mod LLL r/m (TTT LLL are opcode to processor extension)	6	
NOP = No Operation	10010000	3	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.
*Note: Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

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FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field

if mod = 00 then DISP = 0*, disp-low and disp-high are absent

if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent

if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP

if r/m = 001 then EA = (BX) + (DI) + DISP

if r/m = 010 then EA = (BP) + (SI) + DISP

if r/m = 011 then EA = (BP) + (DI) + DISP

if r/m = 100 then EA = (SI) + DISP

if r/m = 101 then EA = (DI) + DISP

if r/m = 110 then EA = (BP) + DISP*

if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

REVISION HISTORY

The sections significantly revised since version -010 are:

Pin Description Table	Added note to $\overline{TEST}$ pin requiring proper RESET at power-up to configure pin as input.
	Renamed pin 44 to INT1/$\overline{SELECT}$ and pin 41 to INT3/$\overline{INTA1}$/IRQ to better describe their functions in Slave Mode.
Initialization and Processor Reset	Added reminder to drive $\overline{RES}$ pin LOW during power-up.
Major Cycle Timing Waveform	Clarified applicability of T_{CLCSV} to latched A1 and A2 in footnote.
HOLD/HLDA Timing Waveforms	Redrawn to indicate correct relationship of HOLD inactive to HLDA inactive.
Instruction Set Summary	Corrected clock count for ENTER instruction.
Slave Mode Operation	The three low order bits associated with vector generation and performing EOI are not alterable; however, the priority levels are programmable. This information is a clarification only.

The sections significantly revised since version -009 are:

Pin Description Table	Various descriptions rewritten for clarity.
Interrupt Vector Table	Redrawn for clarity.
A.C. Characteristics	Added reminder that T_{SRYCL} and T_{CLSRY} must be met.
Explanation of the A.C. Symbols	New section.
Major Cycle Timing Waveforms	T_{CLRO} indicated.

The sections significantly revised since version -008 are:

Pin Description Table	Noted $\overline{RES}$ to be low more than 4 clocks. Connections to X1 and X2 clarified.
DMA Control Bit Descriptions	Moved and clarified note concerning TC condition for ST/$\overline{STOP}$ clearing during unsynchronized transfers.
Interrupt Controller, etc.	Renamed iRMX Mode to Slave Mode.
Interrupt Request Register	Noted that D0 and D1 are read/write, others read-only.
Execution Timings	Clarified effect of bus width.
A.C. Characteristics	10 MHz 80188 no longer offered.

The sections significantly revised since version -007 are:

A.C. Characteristics	Several timings changed in anticipation of test change (all listed in ns): T_{CLAV} (min.) at 10 MHz from 50 to 44; T_{CVCTV} (min.) at 8 MHz from 10 to 5; T_{CVCTV} (max.) from 70 to 50 at 8 MHz and 56 to 40 at 10 MHz.

80C188
CHMOS HIGH INTEGRATION 16-BIT MICROPROCESSOR

- **Operation Modes Include:**
  - **Enhanced Mode Which Has**
    - **DRAM Refresh Control Unit**
    - **Power-Save Mode**
  - **Compatible Mode**
    - **NMOS 80188 Pin for Pin Replacement for Non-Numerics Applications**
- **Integrated Feature Set**
  - **Enhanced 80C86/C88 CPU**
  - **Clock Generator**
  - **2 Independent DMA Channels**
  - **Programmable Interrupt Controller**
  - **3 Programmable 16-Bit Timers**
  - **Dynamic RAM Refresh Control Unit**
  - **Programmable Memory and Peripheral Chip Select Logic**
  - **Programmable Wait State Generator**
  - **Local Bus Controller**
  - **Power Save Mode**
  - **System-Level Testing Support (High Impedance Test Mode)**
- **Available in 16 MHz (80C188-16), 12.5 MHz (80C188-12) and 10 MHz (80C188) Versions**
- **Direct Addressing Capability to 1 MByte Memory and 64 KByte I/O**
- **Completely Object Code Compatible with All Existing 8086/8088 Software and Also Has 10 Additional Instructions over 8086/8088**
- **Complete System Development Support**
  - **All 8088 and NMOS 80188 Software Development Tools Can Be Used for 80C186 System Development**
    - **ASM86 Assembler, PL/M-86, Pascal-86, Fortran-86, C-86 and System Utilities**
    - **In-Circuit-Emulator (ICE™-188)**
- **Available in 68 Pin:**
  - **Plastic Leaded Chip Carrier (PLCC)**
  - **Ceramic Pin Grid Array (PGA)**
  - **Ceramic Leadless Chip Carrier (JEDEC A Package)**

  (See Packaging Outlines and Dimensions, Order Number 231369)
- **Available in EXPRESS Extended Temperature Range (−40°C to +85°C)**

The Intel 80C188 is a CHMOS high integration microprocessor. It has features which are new to the 80186 family which include a DRAM refresh control unit and power-save mode. When used in "compatible" mode, the 80C188 is 100% pin-for-pin compatible with the NMOS 80188 (except for 8087 applications). The "enhanced" mode of operation allows the full feature set of the 80C188 to be used. The 80C188 is upward compatible with 8086 and 8088 software and fully compatible with 80186 and 80188 software, except for numerics applications.

October 1991
Order Number: 270432-004

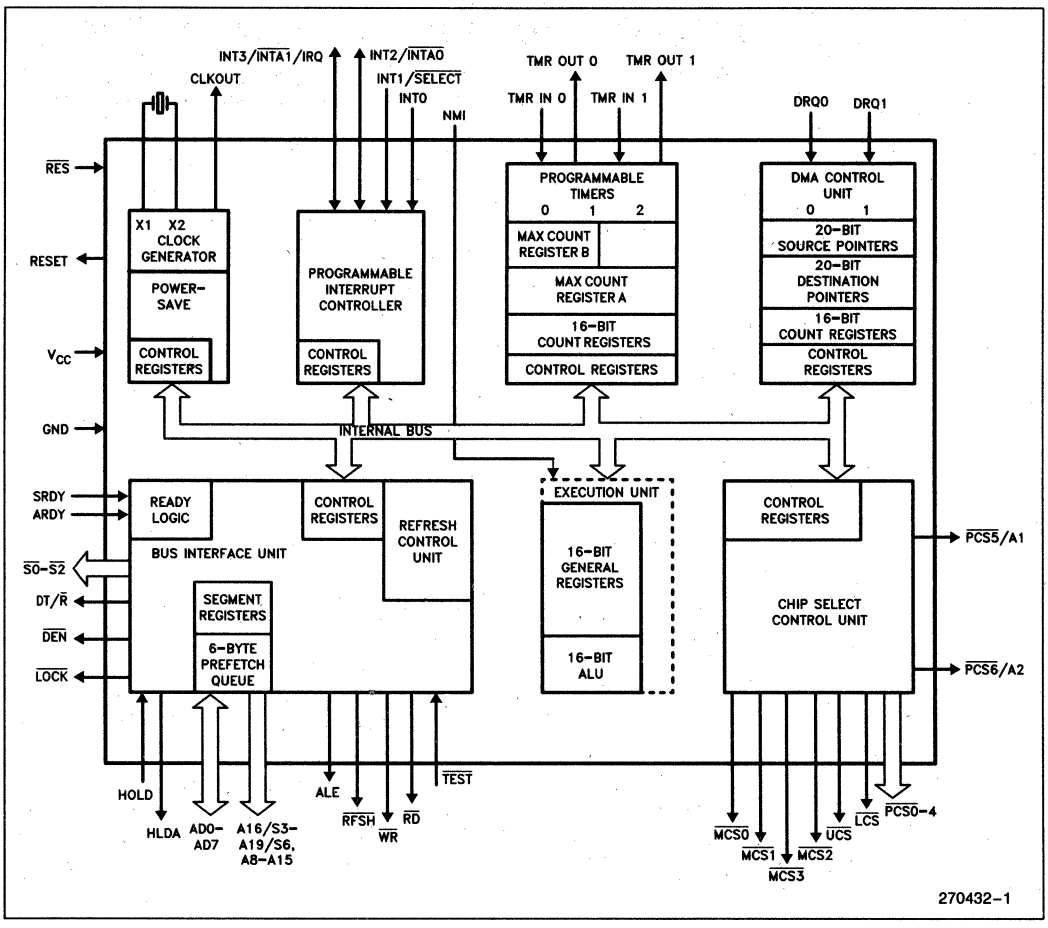
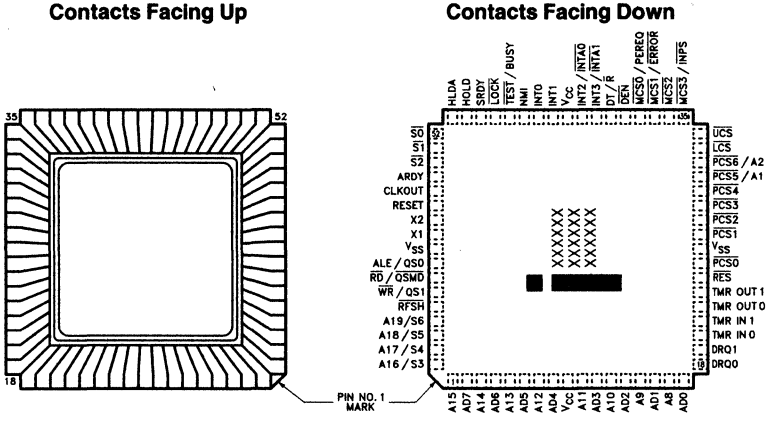


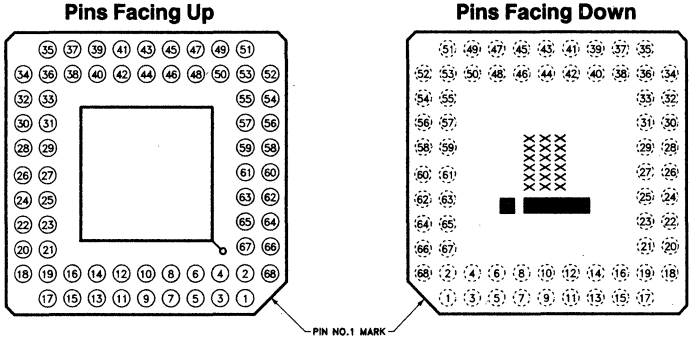
Figure 1. 80C188 Block Diagram

Ceramic Leadless Chip Carrier (JEDEC Type A)



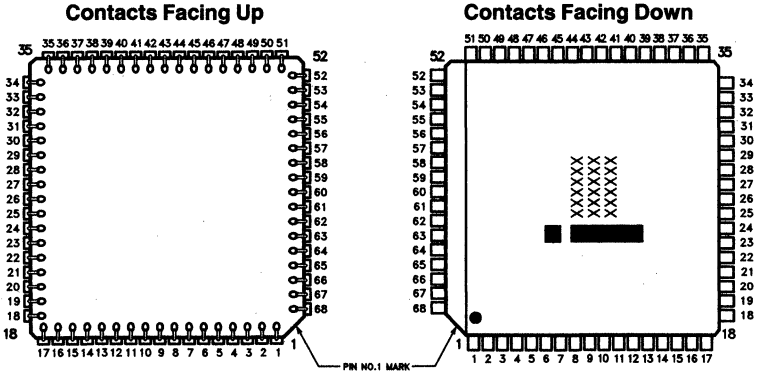
270432-2

Ceramic Pin Grid Array



270432-3

Plastic Leaded Chip Carrier



270432-4

Figure 2. 80C188 Pinout Diagrams

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Table 1. 80C188 Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	9 43	I I	System Power: +5 volt power supply.
V_{SS}	26 60	I I	System Ground.
RESET	57	O	RESET Output indicates that the 80C188 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal. Reset goes inactive 2 clockout periods after $\overline{RES}$ goes inactive. When tied to the $\overline{TEST}$ pin, RESET forces the 80C188 into enhanced mode. RESET is not floated during bus hold.
X1 X2	59 58	I O	Crystal Inputs X1 and X2 provide external connections for a fundamental mode or third overtone parallel resonant crystal for the internal oscillator. X1 can connect to an external clock instead of a crystal. In this case, minimize the capacitance on X2. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT is active during reset and bus hold.
$\overline{RES}$	24	I	An active $\overline{RES}$ causes the 80C188 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80C188 clock. The 80C188 begins fetching instructions approximately 6½ clock cycles after $\overline{RES}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{RES}$ held LOW. $\overline{RES}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network.
$\overline{TEST}$	47	I/O	The $\overline{TEST}$ pin is sampled during and after reset to determine whether the 80C188 is to enter Compatible or Enhanced Mode. Enhanced Mode requires $\overline{TEST}$ to be HIGH on the rising edge of $\overline{RES}$ and LOW four CLKOUT cycles later. Any other combination will place the 80C188 in Compatible Mode. A weak internal pullup ensures a HIGH state when the pin is not driven. This pin is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when WAIT execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled every five clocks until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80C188 is waiting for $\overline{TEST}$, interrupts will be serviced. During power-up, active $\overline{RES}$ is required to configure $\overline{TEST}$ as an input.
TMR IN 0 TMR IN 1	20 21	I I	Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized. Timer Inputs must be tied HIGH when not being used as clock or retrigger inputs.
TMR OUT 0 TMR OUT 1	22 23	O O	Timer outputs are used to provide single pulse or continous waveform generation, depending upon the timer mode selected. These outputs are not floated during a bus hold.

Table 1. 80C188 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
DRQ0 DRQ1	18 19	I I	DMA Request is asserted HIGH by an external device when it is ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
NMI	46	I	The Non-Maskable Interrupt input causes a Type 2 interrupt. An NMI transition from LOW to HIGH is latched and synchronized internally, and initiates the interrupt at the next instruction boundary. NMI must be asserted for at least one CLKOUT period. The Non-Maskable Interrupt cannot be avoided by programming.
INT0 INT1/$\overline{\text{SELECT}}$ INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$/IRQ	45 44 42 41	I I I/O I/O	Maskable Interrupt Requests can be requested by activating one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When slave mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).
A19/S6 A18/S5 A17/S4 A16/S3	65 66 67 68	O O O O	Address Bus Outputs (16–19) and Bus Cycle Status (3–6) indicate the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W, and T_4, status information is available on these lines as encoded below: During T_2, T_3, T_W, and T_4, the S6 pin is LOW to indicate a CPU-initiated bus cycle or HIGH to indicate a DMA-initiated bus cycle. During the same T-states, S3, S4, and S5 are always LOW. These outputs are floated during a bus hold or reset.
A15 A14 A13 A12 A11 A10 A9 A8	1 3 5 7 10 12 14 16	O O O O O O O O	Address-Only Bus (15–8) contains valid addresses from T_1–T_4. The bus is active high. These outputs are floated during a bus hold or reset.
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	2 4 6 8 11 13 15 17	I/O I/O I/O I/O I/O I/O I/O I/O	Address/Data Bus (7–0) signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W, and T_4) bus. The bus is active high. These pins are floated during a bus hold or reset.
$\overline{\text{RFSH}}$	64	O	In compatible mode, $\overline{\text{RFSH}}$ is HIGH. In enhanced mode, $\overline{\text{RFSH}}$ is asserted LOW to signify a refresh bus cycle. The $\overline{\text{RFSH}}$ output pin floats during bus hold or reset, regardless of operating mode.

Table 1. 80C186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
ALE/QS0	61	O	Address Latch Enable/Queue Status 0 is provided by the 80C188 to latch the address. ALE is active HIGH, with addresses guaranteed valid on the trailing edge.
$\overline{WR}$/QS1	63	O	Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. It is active LOW, and floats during bus hold or reset. When the 80C188 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.

QS1	QS0	Queue Operation
0	0	No queue operation
0	1	First opcode byte fetched from the queue
1	1	Subsequent byte fetched from the queue
1	0	Empty the queue

$\overline{RD}$/$\overline{QSMD}$	62	O/I	Read Strobe is an active LOW signal which indicates that the 80C188 is performing a memory or I/O read cycle. It is guaranteed not to go LOW before the A/D bus is floated. An internal pull-up ensures that $\overline{RD}$/$\overline{QSMD}$ is HIGH during RESET. Following RESET the pin is sampled to determine whether the 80C188 is to provide ALE, $\overline{RD}$ and $\overline{WR}$, or queue status information. To enable Queue Status Mode, $\overline{RD}$ must be connected to GND. $\overline{RD}$ will float during bus HOLD.
ARDY	55	I	Asynchronous Ready informs the 80C188 that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUT and is active HIGH. The falling edge of ARDY must be synchronized to the 80C188 clock. Connecting ARDY HIGH will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the SRDY pin.
SRDY	49	I	Synchronous Ready informs the 80C188 that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active-HIGH input synchronized to CLKOUT. The use of SRDY allows a relaxed system timing over ARDY. This is accomplished by elimination of the one-half clock cycle required to internally synchronize the ARDY input signal. Connecting SRDY high will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the ARDY pin.

Table 1. 80C188 Pin Description (Continued)

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>$\overline{LOCK}$</td><td>48</td><td>O</td><td>$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus. $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction immediately following the LOCK prefix. It remains active until the completion of that instruction. No instruction prefetching will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ floats during bus hold or reset.</td></tr>
<tr><td>$\overline{S0}$
$\overline{S1}$
$\overline{S2}$</td><td>52
53
54</td><td>O
O
O</td><td>Bus cycle status $\overline{S0}$–$\overline{S2}$ are encoded to provide bus-transaction information:
80C188 Bus Cycle Status Information
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus Cycle Initiated</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction Fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Data from Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Data to Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive (no bus cycle)</td></tr>
</table>
The status pins float during HOLD.
$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.</td></tr>
<tr><td>HOLD
HLDA</td><td>50
51</td><td>I
O</td><td>HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. The 80C188 generates HLDA (HIGH) in response to a HOLD request. Simultaneous with the issuance of HLDA, the 80C188 will float the local bus and control lines. After HOLD is detected as being LOW, the 80C188 will lower HLDA. When the 80C188 needs to run another bus cycle, it will again drive the local bus and control lines.
In Enhanced Mode, HLDA will go low when a DRAM refresh cycle is pending in the 80C188 and an external bus master has control of the bus. It will be up to the external master to relinquish the bus by lowering HOLD so that the 80C188 may execute the refresh cycle.</td></tr>
<tr><td>$\overline{UCS}$</td><td>34</td><td>O/I</td><td>Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. $\overline{UCS}$ does not float during bus hold. The address range activating $\overline{UCS}$ is software programmable.
$\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the 80C188 will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{UCS}$ has a weak internal pullup that is active during RESET to ensure that the 80C188 does not enter the ONCE mode inadvertently.</td></tr>
</table>

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Table 1. 80C188 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{LCS}$	33	O/I	Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. $\overline{LCS}$ does not float during bus HOLD. The address range activating $\overline{LCS}$ is software programmable. $\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the 80C186 will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{LCS}$ has a weak internal pullup that is active only during RESET to ensure that the 80C188 does not enter ONCE Mode inadvertently.
$\overline{MCS0}$ $\overline{MCS1}$ $\overline{MCS2}$ $\overline{MCS3}$	38 37 36 35	O O O O	Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines do not float during bus HOLD. The address ranges activating $\overline{MCS0}$–3 are software programmable.
$\overline{PCS0}$ $\overline{PCS1}$ $\overline{PCS2}$ $\overline{PCS3}$ $\overline{PCS4}$	25 27 28 29 30	O O O O O	Peripheral Chip Select signals 0–4 are active LOW when a reference is made to the defined peripheral area (64K I/O space or 1 Mbyte memory space). These lines do not float during bus HOLD. The address ranges activating $\overline{PCS0}$–4 are software programmable.
$\overline{PCS5}$/A1	31	O	Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software-programmable. $\overline{PCS5}$/A1 does not float during bus HOLD. When programmed to provide latched A1, this pin will retain the previously latched value during HOLD.
$\overline{PCS6}$/A2	32	O	Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software-programmable. $\overline{PCS6}$/A2 does not float during bus HOLD. When programmed to provide latched A2, this pin will retain the previously latched value during HOLD.
DT/$\overline{R}$	40	O	Data Transmit/Receive controls the direction of data flow through an external data bus transceiver. When LOW, data is transferred to the 80C188. When HIGH the 80C188 places write data on the data bus. DT/$\overline{R}$ floats during a bus hold or RESET.
$\overline{DEN}$	39	O	Data Enable is provided as a data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access. $\overline{DEN}$ is HIGH whenever DT/$\overline{R}$ changes state. During RESET, $\overline{DEN}$ is driven HIGH for one clock, then floated. $\overline{DEN}$ also floats during HOLD.

FUNCTIONAL DESCRIPTION

Introduction

The following Functional Description describes the base architecture of the 80C188. The 80C188 is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip. The 80C188 is object code compatible with the 8086/8088 microprocessors and adds 10 new instruction types to the 8086/8088 instruction set.

The 80C188 has two major modes of operation, Compatible and Enhanced. In Compatible Mode the 80C188 is completely compatible with NMOS 80188, with the exception of 8087 support. The Enhanced mode adds two new features to the system design. These are Power-Save control and Dynamic RAM refresh.

80C188 BASE ARCHITECTURE

The 8086, 8088, 80186, and 80188 families all contain the same basic set of registers, instructions, and addressing modes. The 80C188 processor is upward compatible with the 8086 and 8088 CPUs.

Register Set

The 80C188 base architecture has fourteen registers as shown in Figures 3a and 3b. These registers are grouped into the following categories.

General Registers

Eight 16-bit general purpose registers may be used for arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

Segment Registers

Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

Base and Index Registers

Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

Status and Control Registers

Two 16-bit special purpose registers record or alter certain aspects of the 80C188 processor state. These are the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed, and the Status Word Register, which contains status and control flag bits (see Figures 3a and 3b).

Status Word Description

The Status Word records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the 80C186 within a given operating mode (bits 8, 9, and 10). The Status Word Register is 16-bits wide. The function of the Status Word bits is shown in Table 2.

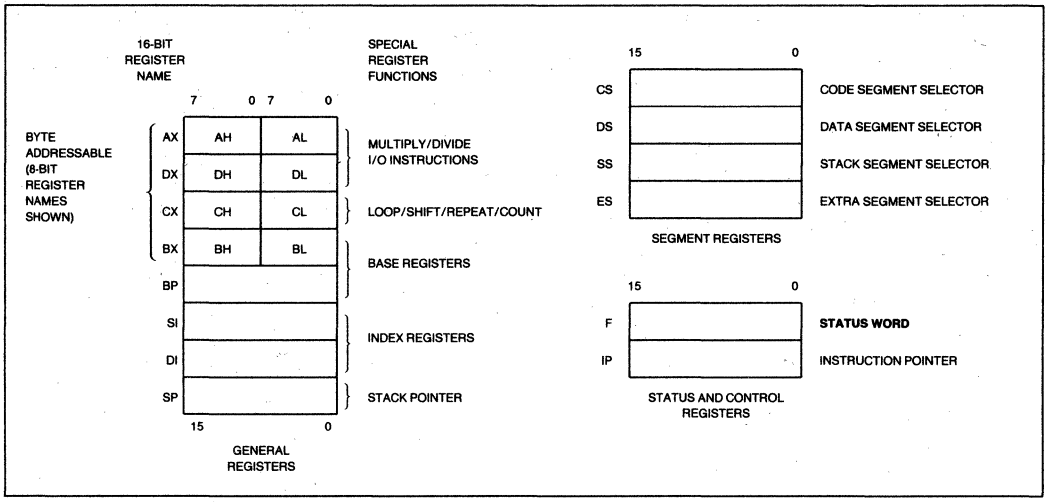

Figure 3a. 80C188 Register Set

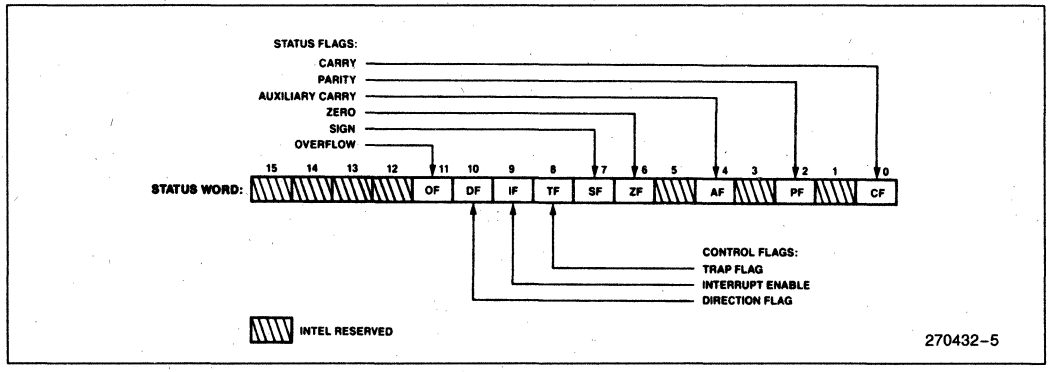

Figure 3b. Status Word Format

Table 2. Status Word Bit Functions

Bit Position	Name	Function
0	CF	Carry Flag—Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag—Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag—Set if result is zero; cleared otherwise
7	SF	Sign Flag—Set equal to high-order bit of result (0 if positive, 1 if negative)
8	TF	Single Step Flag—Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-enable Flag—When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag—Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag—Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high-level instructions, and processor control. These categories are summarized in Figure 4.

An 80C188 instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory. Specific operand addressing modes are discussed later in this data sheet.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment register (code, data, stack, extra). The physical address is calculated by shifting the base value LEFT by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 5). This allows for a 1 MByte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 3). These rules follow the way programs are written (see Figure 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack
ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero
LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word
FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{\text{TEST}}$ pin active
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Figure 4. 80C188 Instruction Set

CONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal
JAE/JNB	Jump if above or equal/not below
JB/JNAE	Jump if below/not above nor equal
JBE/JNA	Jump if below or equal/not above
JC	Jump if carry
JE/JZ	Jump if equal/zero
JG/JNLE	Jump if greater/not less nor equal
JGE/JNL	Jump if greater or equal/not less
JL/JNGE	Jump if less/not greater nor equal
JLE/JNG	Jump if less or equal/not greater
JNC	Jump if not carry
JNE/JNZ	Jump if not equal/not zero
JNO	Jump if not overflow
JNP/JPO	Jump if not parity/parity odd
JNS	Jump if not sign

JO	Jump if overflow
JP/JPE	Jump if parity/parity even
JS	Jump if sign
UNCONDITIONAL TRANSFERS	
CALL	Call procedure
RET	Return from procedure
JMP	Jump
ITERATION CONTROLS	
LOOP	Loop
LOOPE/LOOPZ	Loop if equal/zero
LOOPNE/LOOPNZ	Loop if not equal/not zero
JCXZ	Jump if register CX = 0
INTERRUPTS	
INT	Interrupt
INTO	Interrupt if overflow
IRET	Interrupt return

Figure 4. 80C188 Instruction Set (Continued)

To access operands that do not reside in one of the four immediately available segments, a full 32-bit pointer can be used to reload both the base (segment) and offset values.

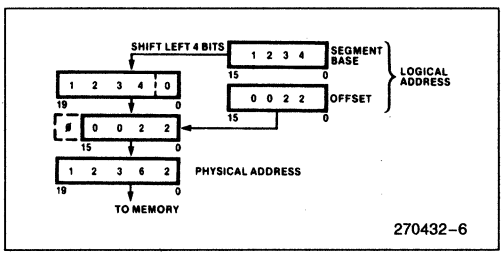

Figure 5. Two Component Address

Table 3. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data.
Stack	Stack (SS)	All stack pushes and pops; any memory references which use BP Register as a base register.
External Data (Global)	Extra (ES)	All string instruction references which use the DI register as an index.
Local Data	Data (DS)	All other data references.

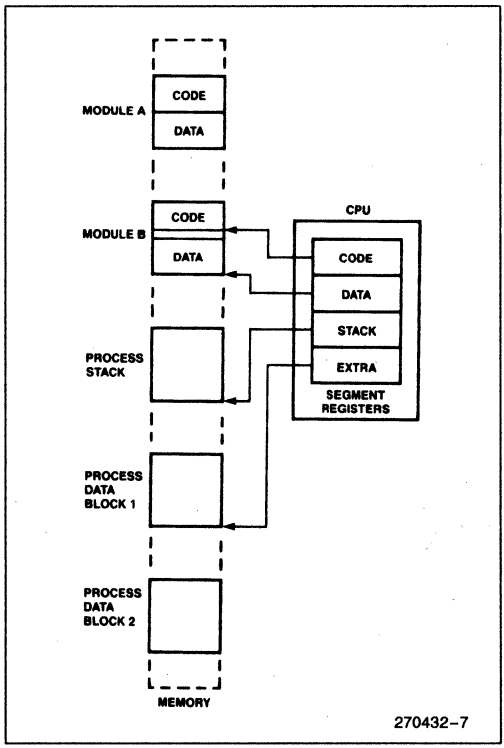

Figure 6. Segmented Memory Helps Structure Software

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Addressing Modes

The 80C188 provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an Index register.
- *Based indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

Data Types

The 80C188 directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component or a 16-bit segment base component in addition to a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 to 64K bytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4-bits) of the byte.

In general, individual data elements must fit within defined segment limits. Figure 7 graphically represents the data types supported by the 80C188.

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A_{15}–A_8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Status Word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.

Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. If the exception was caused by attempted execution of an ESC instruction, the return instruction will point to the ESC instruction, or to the segment override prefix immediately preceding

the ESC instruction if the prefix was present. In all other cases, the return address from an exception will point at the instruction immediately following the instruction causing the exception.

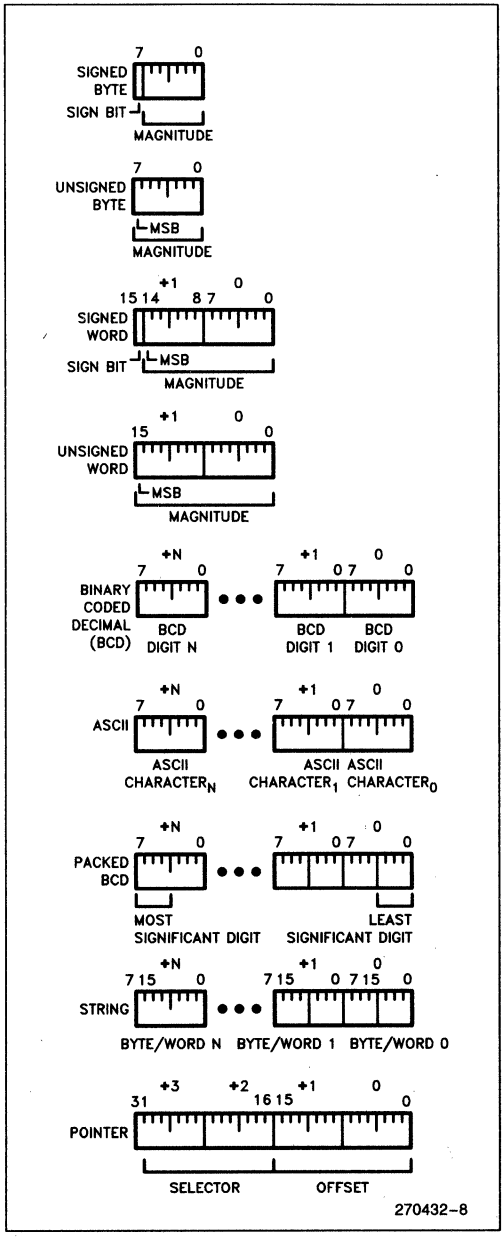

Figure 7. 80C188 Supported Data Types

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0–31, some of which are used for instruction exceptions, are reserved. Table 4 shows the 80C188 predefined types and default priority levels. For each interrupt, an 8-bit vector must be supplied to the 80C186 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. In addition, internal peripherals and noncascaded external interrupts will generate their own vectors through the internal interrupt controller. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Interrupt Sources

The 80C188 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INT0, DIV, IDIV, etc.). All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type (Table 4), multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

Those pre-defined 80C188 interrupts which cannot be masked by programming are described below.

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DIVIDE ERROR EXCEPTION (TYPE 0)

Generated when a DIV or IDIV instruction quotient cannot be expressed in the number of bits in the destination.

SINGLE-STEP INTERRUPT (TYPE 1)

Generated after most instructions if the TF flag in the status word is set. This interrupt allows programs to execute one instruction at a time. Interrupts will not be generated after prefix instructions (e.g., REP), instructions which modify segment registers (e.g., POP DS), or the WAIT instruction. Vectoring to the single-step interrupt service routine clears the TF bit. An IRET instruction in the interrupt service routine restores the TF bit to logic "1" and transfers control to the next instruction to be single-stepped.

NON-MASKABLE INTERRUPT—NMI (TYPE 2)

An external interrupt source which is serviced regardless of the state of the IF bit. No external acknowledge sequence is performed. The IF bit is cleared at the beginning of an NMI interrupt to prevent maskable interrupts from being serviced. A typical use of NMI would be to activate a power failure routine.

Table 4. 80C188 Interrupt Vectors

Interrupt Name	Vector Type	Vector Address	Default Priority	Related Instructions	Applicable Notes
Divide Error Exception	0	00H	1	DIV, IDIV	1
Single Step Interrupt	1	04H	1A	All	2
Non-Maskable Interrupt (NMI)	2	08H	1	All	
Breakpoint Interrupt	3	0CH	1	INT	1
INTO Detected Overflow Exception	4	10H	1	INTO	1
Array Bounds Exception	5	14H	1	BOUND	1
Unused-Opcode Exception	6	18H	1	Undefined Opcodes	1
ESC Opcode Exception	7	1CH	1	ESC Opcodes	1, 3
Timer 0 Interrupt	8	20H	2A		4, 5
Timer 1 Interrupt	18	48H	2B		4, 5
Timer 2 Interrupt	19	4CH	2C		4, 5
Reserved	9	24H	3		
DMA 0 Interrupt	10	28H	5		5
DMA 1 Interrupt	11	2CH	5		5
INT0 Interrupt	12	30H	6		
INT1 Interrupt	13	34H	7		
INT2 Interrupt	14	38H	8		
INT3 Interrupt	15	3CH	9		
Reserved	16, 17	40H, 44H			
Reserved	20–31	50H . . . 7CH			

NOTES:
Default priorities for the interrupt sources are used only if the user does not program each source to a unique priority level.
1. Generated as a result of an instruction execution.
2. Performed in same manner as 8088.
3. An ESC opcode will cause a trap regardless of the 80C188 operating mode. The 80C188 is not directly compatible with the 80188 in this respect. The instruction set of a numerics coprocessor cannot be executed.
4. All three timers constitute one source of request to the interrupt controller. As such, they share the same priority level with respect to other interrupt sources. However, the timers have a defined priority order among themselves (2A > 2B > 2C).
5. The vector type numbers for these sources are programmable in Slave Mode.

BREAKPOINT INTERRUPT (TYPE 3)

A one-byte version of the INT instruction. It uses 12 as an index into the service routine address table (because it is a type 3 interrupt).

INTO DETECTED OVERFLOW EXCEPTION (TYPE 4)

Generated during an INTO instruction if the 0F bit is set.

ARRAY BOUNDS EXCEPTION (TYPE 5)

Generated during a BOUND instruction if the array index is outside the array bounds. The array bounds are located in memory at a location indicated by one of the instruction operands. The other operand indicates the value of the index to be checked.

UNUSED OPCODE EXCEPTION (TYPE 6)

Generated if execution is attempted on undefined opcodes.

ESCAPE OPCODE EXCEPTION (TYPE 7)

Generated if execution is attempted of ESC opcodes (D8H–DFH). The 80C188 does not check an escape opcode trap bit as does the 80C186. On the 80C188, ESC traps occcur in both compatible and enhanced operating modes. The return address of this exception will point to the ESC instruction causing the exception. If a segment override prefix preceded the ESC instruction, the return address will point to the segment override prefix.

NOTE:
Unlike the 80188, all numerics coprocessor opcodes cause a trap. The 80C188 does not support the numerics interface.

Hardware-generated interrupts are divided into two groups: maskable interrupts and non-maskable interrupts. The 80C188 provides maskable hardware interrupt request pins INT0–INT3. In addition, maskable interrupts may be generated by the 80C188 integrated DMA controller and the integrated timer unit. The vector types for these interrupts is shown in Table 4. Software enables these inputs by setting the interrupt flag bit (IF) in the Status Word. The interrupt controller is discussed in the peripheral section of this data sheet.

Further maskable interrupts are disabled while servicing an interrupt because the IF bit is reset as part of the response to an interrupt or exception. The saved Status Word will reflect the enable status of the processor prior to the interrupt. The interrupt flag will remain zero unless specifically set. The interrupt return instruction restores the Status Word, thereby restoring the original status of IF bit. If the interrupt return re-enables interrupts, and another interrupt is pending, the 80C188 will immediately service the highest-priority interrupt pending, i.e., no instructions of the main line program will be executed.

Initialization and Processor Reset

Processor initialization is accomplished by driving the $\overline{RES}$ input pin LOW. $\overline{RES}$ must be LOW during power-up to ensure proper device initialization. $\overline{RES}$ forces the 80C188 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{RES}$ is active. After $\overline{RES}$ becomes inactive and an internal processing interval elapses, the 80C188 begins execution with the instruction at physical location FFFF0(H). $\overline{RES}$ also sets some registers to predefined values as shown in Table 5.

Table 5. 80C188 Initial Register State after RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

THE 80C188 COMPARED TO THE 80C186

The 80C188 is an 8-bit processor designed based on the 80C186 internal structure. Most internal functions of the 80C188 are identical to the equivalent 80C186 functions. The 80C188 handles the external bus the same way the 80C186 does with the distinction of handling only 8 bits at a time. Sixteen-bit operands are fetched or written in two consecutive bus cycles. The processors will look the same to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions except numerics instructions have the same end result. Internally, there are four differences between the 80C188 and the 80C186. All changes are related to the 8-bit bus interface.

- The queue length is 4 bytes in the 80C188, whereas the 80C186 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8 bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The 80C188 BIU will fetch a new instruction to load into the queue each time there is a 1-byte hole (space available) in the queue. The 80C186 waits until a 2-byte space is available.
- The internal execution time of an instruction is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU may also be limited by the rate of instruction fetches when a series of simple operations occur. When the more sophisticated instructions of the 80C188 are being used, the queue has more time to fill and the execution proceeds more closely to the speed at which the execution unit will allow.
- The 80C188 does not have a numerics interface, since the 80C186 numerics interface inherently requires 16-bit communication with the numerics coprocessor.

The 80C188 and 80C186 are completely software compatible (except for numerics instructions) by virtue of their identical execution units. However, software that is system dependent may not be completely transferable.

The bus interface and associated control signals vary somewhat between the two processors. The pin assignments are nearly identical, with the following functional changes:

- A8–A15—These pins are only address outputs on the 80C188. These address lines are latched internally and remain valid throughout the bus cycle.
- $\overline{BHE}$ has no meaning on the 80C188. However, it was necessary to designate this pin the $\overline{RFSH}$ pin in order to provide an indication of DRAM refresh bus cycles.

80C188 CLOCK GENERATOR

The 80C188 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

Oscillator

The 80C188 oscillator circuit is designed to be used either with a parallel resonant fundamental or third-overtone mode crystal, depending upon the frequency range of the application as shown in Figure 8c. This is used as the time base for the 80C188. The crystal frequency chosen should be twice the required processor frequency. Use of an LC or RC circuit is not recommended.

The output of the oscillator is not directly available outside the 80C188. The two recommended crystal configurations are shown in Figures 8a and 8b. When used in third-overtone mode the tank circuit shown in Figure 8b is recommended for stable operation. The sum of the stray capacitances and loading capacitors should equal the values shown. It is advisable to limit stray capacitance between the X1 and X2 pins to less than 10 pF. While a fundamental-mode circuit will require approximately 1 ms for start-up, the third-overtone arrangement may require 1 ms to 3 ms to stabilize.

Alternately, the oscillator may be driven from an external source as shown in Figure 8d. The configuration shown in Figure 8e is not recommended.

Intel recommends the following values for crystal selection parameters:

Temperature Range:	0 to 70°C
ESR (Equivalent Series Resistance):	40Ω max
C_0 (Shunt Capacitance of Crystal):	7.0 pF max
C_1 (Load Capacitance):	20 pF ± 2 pF
Drive Level:	1 mW max

Clock Generator

The 80C188 clock generator provides the 50% duty cycle processor clock for the 80C188. It does this by dividing the oscillator output by 2 forming the symmetrical clock. If an external oscillator is used, the state of the clock generator will change on the falling edge of the oscillator signal. The CLKOUT pin provides the processor clock signal for use outside the 80C188. This may be used to drive other system components. All timings are referenced to the output clock.

READY Synchronization

The 80C188 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T_2, T_3 and again in the middle of each T_W until ARDY is sampled HIGH. One-half CLKOUT cycle of resolution time is used for full synchronization of a rising ARDY signal. A high-to-low transition on ARDY may be used as an indication of the not ready condition but it must be performed synchronously to CLKOUT **either** in the middle of T_2, T_3 or T_W, **or** at the falling edge of T_3 or T_W.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T_2, T_3 and again at the end of each T_W until it is sampled HIGH. By using this input rather than the asynchronous ready input, the half-clock cycle resolution time penalty is eliminated. This input must satisfy set-up and hold times to guarantee proper operation of the circuit.

In addition, the 80C188, as part of the integrated chip-select logic, has the capability to program WAIT states for memory and peripheral blocks. This is discussed in the Chip Select/Ready Logic description.

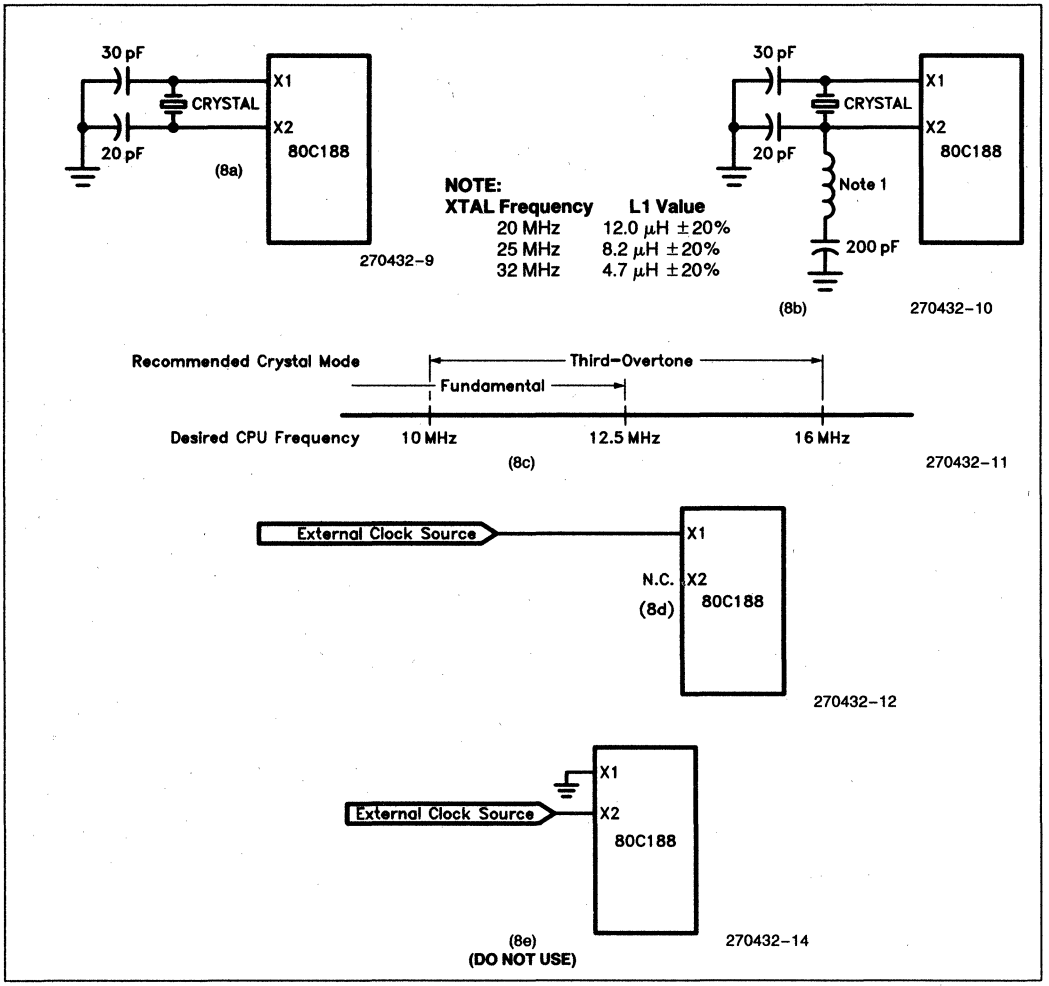

Figure 8. 80C188 Oscillator Configurations (see text)

RESET Logic

The 80C188 provides both a $\overline{RES}$ input pin and a synchronized RESET output pin for use with other system components. The $\overline{RES}$ input pin on the 80C188 is provided with hysteresis in order to facilitate power-on Reset generation via an RC network. RESET output is guaranteed to remain active for at least five clocks given a $\overline{RES}$ input of at least six clocks. RESET may be delayed up to approximately two and one-half clocks behind $\overline{RES}$.

LOCAL BUS CONTROLLER

The 80C188 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides outputs that can be used to enable external buffers and to direct the flow of data on and off the local bus.

Memory/Peripheral Control

The 80C188 provides ALE, $\overline{RD}$, and $\overline{WR}$ bus control signals. The $\overline{RD}$ and $\overline{WR}$ signals are used to strobe data from memory or I/O to the 80C188 or to strobe data from the 80C188 to memory or I/O. The ALE line provides a strobe to latch the address when it is valid. The 80C188 local bus controller does not provide a memory/$\overline{I/O}$ signal. If this is required, use the $\overline{S2}$ signal (which will require external latching), make the memory and I/O spaces nonoverlapping, or use only the integrated chip-select circuitry.

Transceiver Control

The 80C188 generates two control signals for external transceiver chips. This capability allows the addition of transceivers for extra buffering without adding external logic. These control lines, DT/$\overline{R}$ and $\overline{DEN}$, are generated to control the flow of data through the transceivers. The operation of these signals is shown in Table 6.

Table 6. Transceiver Control Signals Description

Pin Name	Function
$\overline{DEN}$ (Data Enable)	Enables the output drivers of the transceivers. It is active LOW during memory, I/O, or INTA cycles.
DT/$\overline{R}$ (Data Transmit/ Receive)	Determines the direction of travel through the transceivers. A HIGH level directs data away from the processor during write operations, while a LOW level directs data toward the processor during a read operation.

Local Bus Arbitration

The 80C188 uses a HOLD/HLDA system of local bus exchange. This provides an asynchronous bus exchange mechanism. This means multiple masters utilizing the same bus can operate at separate clock frequencies. The 80C188 provides a single HOLD/HLDA pair through which all other bus masters may gain control of the local bus. External circuitry must arbitrate which external device will gain control of the bus when there is more than one alternate local bus master. When the 80C188 relinquishes control of the local bus, it floats $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S0}$–$\overline{S2}$, $\overline{LOCK}$, AD0–AD7, A8–A19, S7/$\overline{RFSH}$, and DT/$\overline{R}$ to allow another master to drive these lines directly.

The 80C188 HOLD latency time, i.e., the time between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is second only to DRAM refresh requests in priority of activity requests the processor may receive. Any bus cycle in progress will be completed before the 80C188 relinquishes the bus. This implies that if a HOLD request is received just as a DMA transfer begins, the HOLD latency can be as great as 4 bus cycles. This will occur if a DMA word transfer operation is taking place from an odd address to an odd address. This is a total of 16 clock cycles or more if WAIT states are required. In addition, if locked transfers are performed, the HOLD latency time will be increased by the length of the locked transfer.

If the 80C188 has relinquished the bus and a refresh request is pending, HLDA is removed (driven LOW) to signal the remote processor that the 80C188 wishes to regain control of the bus. The 80C188 will wait until HOLD is removed before taking control of the bus to run the refresh cycle.

Local Bus Controller and Reset

During RESET, the local bus controller will perform the following action:

- Drive $\overline{DEN}$, $\overline{RD}$, and $\overline{WR}$ HIGH for one clock cycle, then float them.
- Drive $\overline{S0}$–$\overline{S2}$ to the inactive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Float AD0–AD7, A8–A19, S7/$\overline{RFSH}$, DT/$\overline{R}$.
- Drive ALE LOW.
- Drive HLDA LOW.

$\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$, and $\overline{TEST}$ pins have internal pullup devices which are active while $\overline{RES}$ is applied. Excessive loading or grounding certain of these pins causes the 80C188 to enter an alternative mode of operation:

- $\overline{RD}$/$\overline{QSMD}$ LOW results in Queue Status Mode.
- $\overline{UCS}$ and $\overline{LCS}$ LOW results in ONCE Mode.
- $\overline{TEST}$ LOW (and HIGH later) results in Enhanced Mode.

INTERNAL PERIPHERAL INTERFACE

All the 80C188 integrated peripherals are controlled by 16-bit registers contained within an internal 256-byte control block. The control block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D_{15-0}, SRDY, and ARDY will be ignored. The base address of the control block must be on an even 256-byte boundary (i.e., the lower 8 bits of the base address are all zeros). All of the defined registers within this control block may be read or written by the 80C188 CPU at any time.

The control block base address is programmed by a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block (see Figure 9). It provides the upper 12 bits of the base address of the control block. The control block is effectively an internal chip select range and must abide by all the rules concerning chip selects (the chip select circuitry is discussed later in this data sheet). Any access to the 256 bytes of the control block activates an internal chip select. Other chip selects may overlap the control block only if they are programmed to zero wait states and ignore external ready. In addition, bit 12 of this register determines whether the control block will be mapped into I/O or memory space. If this bit is 1, the control block will be located in memory space. If the bit is 0, the control block will be located in I/O space. If the control register block is mapped into I/O space, the upper 4 bits of the base address must be programmed as 0 (since I/O addresses are only 16 bits wide).

In addition to providing relocation information for the control block, the relocation register contains bits which place the interrupt controller into Slave Mode. At RESET, the relocation register is set to 20FFH, which maps the control block to start at FF00H in I/O space. An offset map of the 256-byte control register block is shown in Figure 10.

CHIP-SELECT/READY GENERATION LOGIC

The 80C188 contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

Memory Chip Selects

The 80C188 provides 6 memory chip select outputs for 3 address areas; upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

The range for each chip select is user-programmable and can be set to 2K, 4K, 8K, 16K, 32K, 64K, 128K (plus 1K and 256K for upper and lower chip selects). In addition, the beginning or base address of the midrange memory chip select may also be selected. Only one chip select may be programmed to be active for any memory location at a time. All chip select sizes are in bytes.

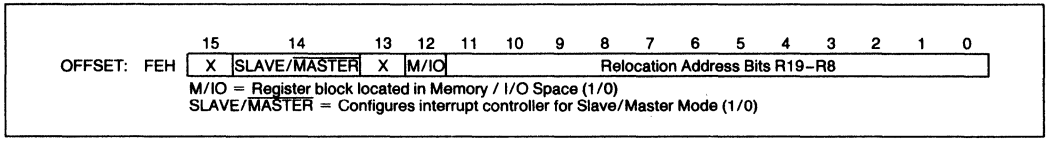

Figure 9. Relocation Register

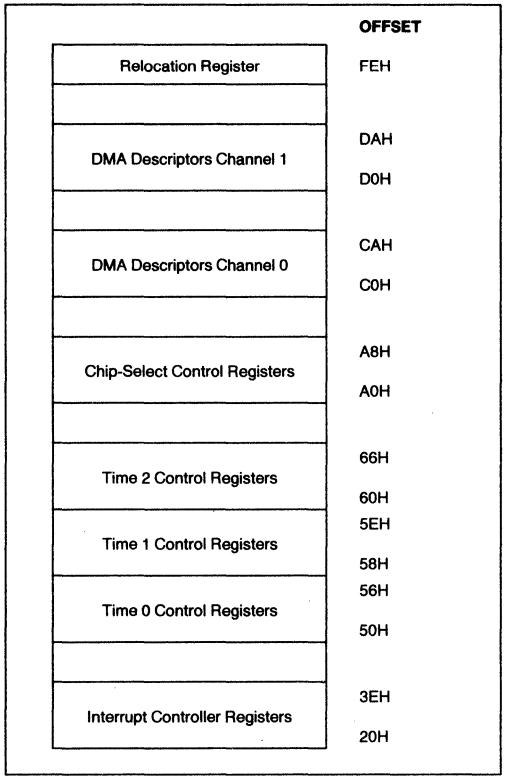

Figure 10. Internal Register Map

Upper Memory $\overline{CS}$

The 80C188 provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the 80C188 begins executing at memory location FFFF0H.

The upper limit of memory defined by this chip select is always FFFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is also defined. Table 7 shows the relationship between the base address selected and the size of the memory block obtained.

Table 7. UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000	256K	C038H

The lower limit of this memory block is defined in the UMCS register (see Figure 11). This register is at offset A0H in the internal control block. The legal values for bits 6–13 and the resulting starting address and memory block sizes are given in Table 7. Any combination of bits 6–13 not shown in Table 7 will result in undefined operation. After reset, the UMCS register is programmed for a 1K area. It must be reprogrammed if a larger upper memory area is desired.

The internal generation of any 20-bit address whose upper 16 bits are equal to or greater than the UMCS value (with bits 0–5 as "0") asserts $\overline{UCS}$. UMCS bits R2–R0 specify the ready mode for the area of memory defined by the chip select register, as explained later.

Lower Memory $\overline{CS}$

The 80C188 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The lower limit of memory defined by this chip select is always 0H, while the upper limit is programmable. By programming the upper limit, the size of the memory block is defined. Table 8 shows the relationship between the upper address selected and the size of the memory block obtained.

Table 8. LMCS Programming Values

Upper Address	Memory Block Size	LMCS Value (Assuming R0 = R1 = R2 = 0)
003FFH	1K	0038H
007FFH	2K	0078H
00FFFH	4K	00F8H
01FFFH	8K	01F8H
03FFFH	16K	03F8H
07FFFH	32K	07F8H
0FFFFH	64K	0FF8H
1FFFFH	128K	1FF8H
3FFFFH	256K	3FF8H

The upper limit of this memory block is defined in the LMCS register (see Figure 12) at offset A2H in the internal control block. The legal values for bits 6–15 and the resulting upper address and memory block sizes are given in Table 8. Any combination of bits 6–15 not shown in Table 8 will result in undefined operation. After RESET, the LMCS register value is undefined. However, the $\overline{LCS}$ chip-select line will not become active until the LMCS register is accessed.

Any internally generated 20-bit address whose upper 16 bits are less than or equal to LMCS (with bits 0–5 "1") will assert $\overline{LCS}$. LMCS register bits R2–R0 specify the READY mode for the area of memory defined by this chip-select register.

Mid-Range Memory $\overline{CS}$

The 80C188 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located within the 80C188 1M byte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the mid-range select lines, as shown in Table 9, is determined by bits 8–14 of the MPCS register (see Figure 13). This register is at location A8H in the internal control block. One and only one of bits 8–14 must be set at a time. Unpredictable operation of the $\overline{MCS}$ lines will otherwise occur. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the mid-range block. If the total block size is 32K, each chip select is active for 8K of memory with $\overline{MCS0}$ being active for the first range and $\overline{MCS3}$ being active for the last range.

The EX and MS in MPCS relate to peripheral functionality as described in a later section.

Table 9. MPCS Programming Values

Total Block Size	Individual Select Size	MPCS Bits 14–8
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

The base address of the mid-range memory block is defined by bits 15–9 of the MMCS register (see Figure 14). This register is at offset A6H in the internal control block. These bits correspond to bits A19–A13 of the 20-bit memory address. Bits A12–A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the mid-range block size is 32K (or the size of the block for which each $\overline{MCS}$ line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, since the first few integer multiples of a 32K memory block are 0H, 8000H, 10000H, 18000H, etc. After RESET, the contents of both registers are undefined. However, none of the $\overline{MCS}$ lines will be active until both the MMCS and MPCS registers are accessed.

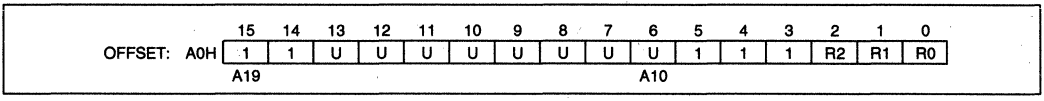

Figure 11. UMCS Register

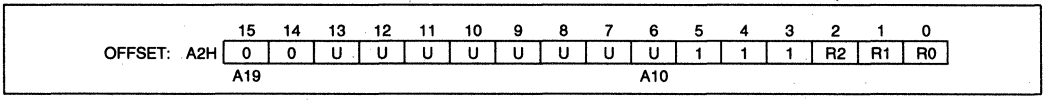

Figure 12. LMCS Register

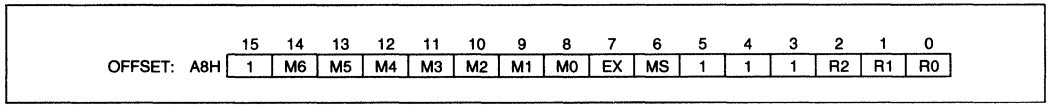

Figure 13. MPCS Register

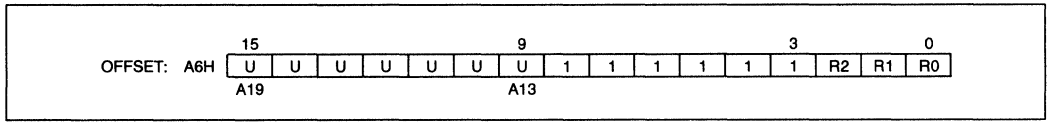

Figure 14. MMCS Register

MMCS bits R2–R0 specify READY mode of operation for all four mid-range chip selects.

The 512K block size for the mid-range memory chip selects is a special case. When using 512K, the base address would have to be at either locations 00000H or 80000H. If it were to be programmed at 00000H when the $\overline{LCS}$ line was programmed, there would be an internal conflict between the $\overline{LCS}$ ready generation logic and the $\overline{MCS}$ ready generation logic. Likewise, if the base address were programmed at 80000H, there would be a conflict with the $\overline{UCS}$ ready generation logic. Since the $\overline{LCS}$ chip-select line does not become active until programmed, while the $\overline{UCS}$ line is active at reset, the memory base can be set only at 00000H. If this base address is selected, however, the $\overline{LCS}$ range must not be programmed.

Peripheral Chip Selects

The 80C188 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address may be located in either memory or I/O space.

Seven $\overline{CS}$ lines called $\overline{PCS0}$–6 are generated by the 80C188. The base address is user-programmable; however it can only be a multiple of 1K bytes, i.e., the least significant 10 bits of the starting address are always 0.

$\overline{PCS5}$ and $\overline{PCS6}$ can also be programmed to provide latched address bits A1 and A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0 and A1 pins used for selecting internal registers of 8-bit peripheral chips.

The starting address of the peripheral chip-select block is defined by the PACS register (see Figure 15). The register is located at offset A4H in the internal control block. Bits 15–6 of this register correspond to bits 19–10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block. Bits 9–0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12–15 must be programmed zero, since the I/O address is only 16 bits wide. Table 10 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

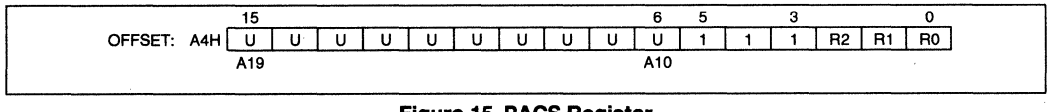

Figure 15. PACS Register

The user should program bits 15–6 to correspond to the desired peripheral base location. PACS bits 0–2 are used to specify READY mode for $\overline{PCS0}$–$\overline{PCS3}$.

Table 10. PCS Address Ranges

$\overline{PCS}$ Line	Active between Locations
$\overline{PCS0}$	PBA —PBA+127
$\overline{PCS1}$	PBA+128—PBA+255
$\overline{PCS2}$	PBA+256—PBA+383
$\overline{PCS3}$	PBA+384—PBA+511
$\overline{PCS4}$	PBA+512—PBA+639
$\overline{PCS5}$	PBA+640—PBA+767
$\overline{PCS6}$	PBA+768—PBA+895

The mode of operation of the peripheral chip selects is defined by the MPCS register (which is also used to set the size of the mid-range memory chip-select block, see Figure 13). The register is located at offset A8H in the internal control block. Bit 7 is used to select the function of $\overline{PCS5}$ and $\overline{PCS6}$, while bit 6 is used to select whether the peripheral chip selects are mapped into memory or I/O space. Table 11 describes the programming of these bits. After RESET, the contents of both the MPCS and the PACS registers are undefined, however none of the PCS lines will be active until both of the MPCS and PACS registers are accessed.

Table 11. MS, EX Programming Values

Bit	Description
MS	1 = Peripherals mapped into memory space.
	0 = Peripherals mapped into I/O space.
EX	0 = 5 $\overline{PCS}$ lines. A1, A2 provided.
	1 = 7 $\overline{PCS}$ lines. A1, A2 are not provided.

MPCS bits 0–2 specify the READY mode for $\overline{PCS4}$–$\overline{PCS6}$ as outlined below.

READY Generation Logic

The 80C188 can generate a READY signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the 80C188 may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

READY control consists of 3 bits for each $\overline{CS}$ line or group of lines generated by the 80C188. The interpretation of the READY bits is shown in Table 12.

Table 12. READY Bits Programming

R2	R1	R0	Number of WAIT States Generated
0	0	0	0 wait states, external RDY also used.
0	0	1	1 wait state inserted, external RDY also used.
0	1	0	2 wait states inserted, external RDY also used.
0	1	1	3 wait states inserted, external RDY also used.
1	0	0	0 wait states, external RDY ignored.
1	0	1	1 wait state inserted, external RDY ignored.
1	1	0	2 wait states inserted, external RDY ignored.
1	1	1	3 wait states inserted, external RDY ignored.

The internal READY generator operates in parallel with external READY, not in series, if the external READY is used (R2 = 0). For example, if the internal generator is set to insert two wait states, but activity on the external READY lines will insert four wait states, the processor will only insert four wait states, not six. This is because the two wait states generated by the internal generator overlapped the first two wait states generated by the external ready signal. Note that the external ARDY and SRDY lines are always ignored during cycles accessing internal peripherals.

R2–R0 of each control word specifies the READY mode for the corresponding block, with the exception of the peripheral chip selects: R2–R0 of PACS set the $\overline{PCS0}$–3 READY mode, R2–R0 of MPCS set the $\overline{PCS4}$–6 READY mode.

Chip Select/Ready Logic and Reset

Upon RESET, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to insert 3 wait states in conjunction with external READY (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

DMA CHANNELS

The 80C188 DMA controller provides two independent DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer. Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data.

DMA Operation

Each channel has six registers in the control block which define each channel's operation. The control registers consist of a 20-bit Source pointer (2 words), a 20-bit destination pointer (2 words), a 16-bit Transfer Count Register, and a 16-bit Control Word. The format of the DMA Control Blocks is shown in Table 13. The Transfer Count Register (TC) specifies the number of DMA transfers to be performed. Up to 64K byte transfers can be performed with automatic termination. The Control Word defines the channel's operation (see Figure 17). All registers may be modified or altered during any DMA activity. Any changes made to these registers will be reflected immediately in DMA operation.

Table 13. DMA Control Block Format

Register Name	Register Address	
	Ch. 0	Ch. 1
Control Word	CAH	DAH
Transfer Count	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

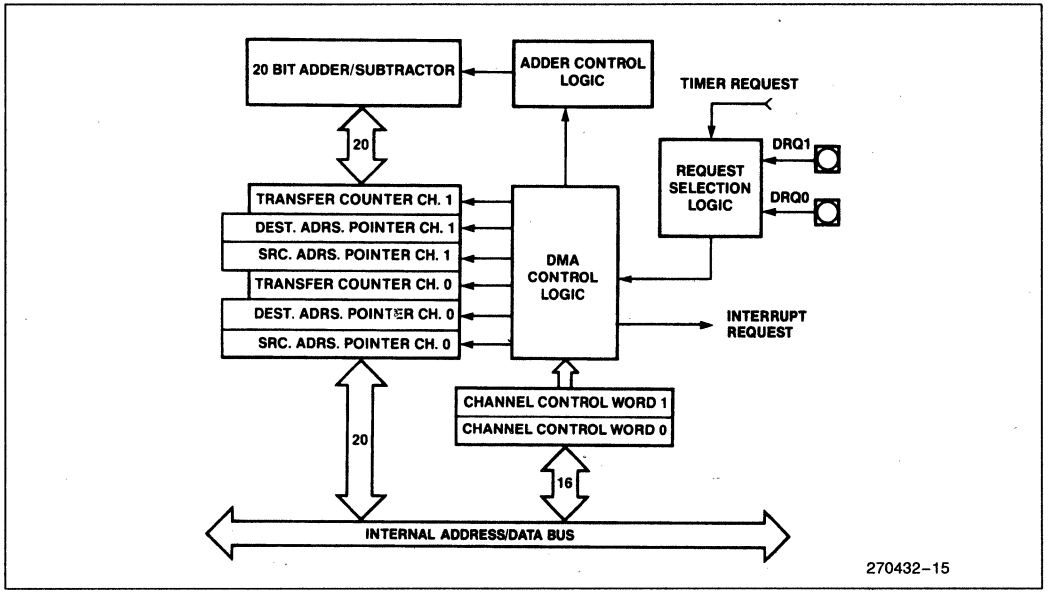

Figure 16. DMA Unit Block Diagram

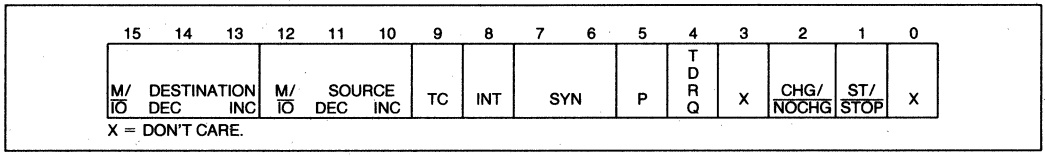

Figure 17. DMA Control Register

DMA Channel Control Word Register

Each DMA Channel Control Word determines the mode of operation for the particular 80C188 DMA channel. This register specifies:

- the mode of synchronization;
- whether interrupts will be generated after the last transfer;
- whether DMA activity will cease after a programmed number of DMA cycles;
- the relative priority of the DMA channel with respect to the other DMA channel;
- whether the source pointer will be incremented, decremented, or maintained constant after each transfer;
- whether the source pointer addresses memory or I/O space;
- whether the destination pointer will be incremented, decremented, or maintained constant after each transfer; and
- whether the destination pointer will address memory or I/O space.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

DMA Control Word Bit Descriptions

DEST: M/$\overline{IO}$ Destination pointer is in memory (1) or I/O (0) space.

DEC Decrement destination pointer by 1 after each transfer.

INC Increment destination pointer by 1 after each transfer.

If both INC and DEC are specified, the pointer will remain constant after each cycle.

SOURCE: M/$\overline{IO}$ Source pointer is in memory (1) or I/O (0) space.

DEC Decrement source pointer by 1 after each transfer.

INC Increment source pointer by 1 after each transfer.

If both INC and DEC are specified, the pointer will remain constant after each cycle.

TC: If set, DMA will terminate when the contents of the transfer count register reach zero. The ST/$\overline{STOP}$ bit will also be reset at this point. If cleared, the DMA controller will decrement the transfer count register for each DMA cycle, but the DMA transfers will not stop when the transfer count register reaches zero.

INT: Enable interrupts to CPU upon transfer count termination.

SYN: 00 No synchronization.

NOTE:

When unsynchronized transfers are specified, the TC bit will be ignored and the ST/$\overline{STOP}$ bit will be cleared upon the transfer count reaching zero, stopping the channel.

01 Source synchronization.

10 Destination synchronization.

11 Unused.

P: Channel priority relative to other channel during simultaneous requests.

0 Low priority.

1 High priority.

Channels will alternate cycles if both are set at the same priority level.

TDRQ: Enable/Disable (1/0) DMA requests from timer 2.

CHG/$\overline{NOCHG}$: Change/Do not change (1/0) the ST/$\overline{STOP}$ bit. If this bit is set when writing the control word, the ST/$\overline{STOP}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{STOP}$ bit will not be altered. This bit is not stored; it will always be read as 0.

ST/$\overline{STOP}$: Start/Stop (1/0) channel.

DMA Destination and Source Pointer Registers

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. For each DMA Channel to be used, all four pointer registers must be initialized. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address (see Figure 18). These pointers may be individually incremented or decremented after each transfer.

Each pointer may point into either memory or I/O space. Since the upper four bits of the address are not automatically programmed to zero, the user must program them in order to address the normal 64K I/O space. There is no restriction on values for the pointer registers.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). The register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA Control Register. If the TC bit in the DMA control word is set or if unsynchronized transfers are programmed, however, DMA activity will terminate when the transfer count register reaches zero.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred. When source or unsynchronized transfers are performed, the DMA channel may begin another transfer immediately after the end of a previous DMA transfer. This allows a complete transfer to take place every 2 bus cycles or eight clock cycles (assuming no wait states). When destination synchronization is performed, data will not be fetched from the source address until the destination device signals that it is ready to receive it. Also, the DMA controller will relinquish control of the bus after every transfer. If no other bus activity is initiated, another destination synchronized DMA cycle will begin after two processor clocks. This allows the destination device time to remove its request if another transfer is not desired. Since the DMA controller will relinquish the bus, the CPU can initiate a bus cycle. As a result, a complete bus cycle will often be inserted between destination synchronized transfers. Table 14 shows the maximum DMA transfer rates.

Table 14. Maximum DMA Transfer Rates at CLKOUT = 16 MHz

Type of Synchronization Selected	CPU Running	CPU Halted
Unsynchronized	2.0 MBytes/sec	2.0 MBytes/sec
Source Synch	2.0 MBytes/sec	2.0 MBytes/sec
Destination Synch	1.3 MBytes/sec	1.6 MBytes/sec

24

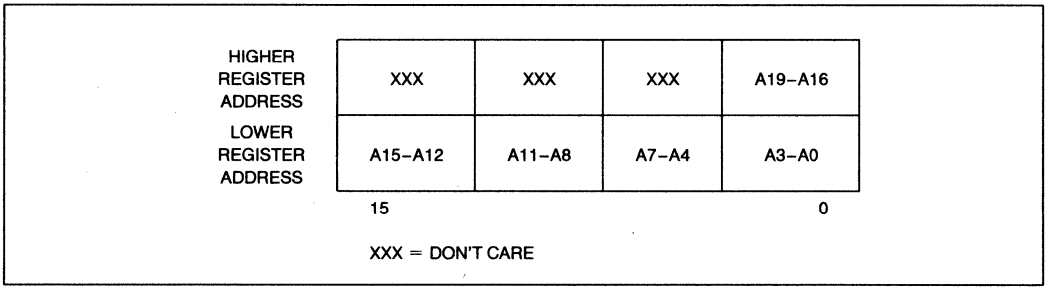

Figure 18. DMA Pointer Register Format

DMA Acknowledge

No explicit DMA acknowledge pulse is provided. Since both source and destination pointers are maintained, a read from a requesting source, or a write to a requesting destination, should be used as the DMA acknowledge signal. Since the chip-select lines can be programmed to be active for a given block of memory or I/O space, and the DMA pointers can be programmed to point to the same given block, a chip-select line could be used to indicate a DMA acknowledge.

DMA Priority

The DMA channels may be programmed to give one channel priority over the other, or they may be programmed to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses; also, an external bus hold takes priority over an internal DMA cycle. Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time will suffer during sequences of continuous DMA cycles. An NMI request, however, will cause all internal DMA activity to halt. This allows the CPU to quickly respond to the NMI request.

DMA Programming

DMA cycles will occur whenever the ST/$\overline{\text{STOP}}$ bit of the Control Register is set. If synchronized transfers are programmed, a DRQ must also be generated. Therefore the source and destination transfer pointers, and the transfer count register (if used) must be programmed before the ST/STOP bit is set.

Each DMA register may be modified while the channel is operating. If the CHG/NOCHG bit is cleared when the control register is written, the ST/STOP bit of the control register will not be modified by the write. If multiple channel registers are modified, it is recommended that a LOCKED string transfer be used to prevent a DMA transfer from occurring between updates to the channel registers.

DMA Channels and Reset

Upon RESET, the state of the DMA channels will be as follows:

- The ST/$\overline{\text{STOP}}$ bit for each channel will be reset to $\overline{\text{STOP}}$.
- Any transfer in progress is aborted.
- The values of the transfer count registers, source pointers and destination pointers are indeterminate.

TIMERS

The 80C188 provides three internal 16-bit programmable timers (see Figure 19). Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

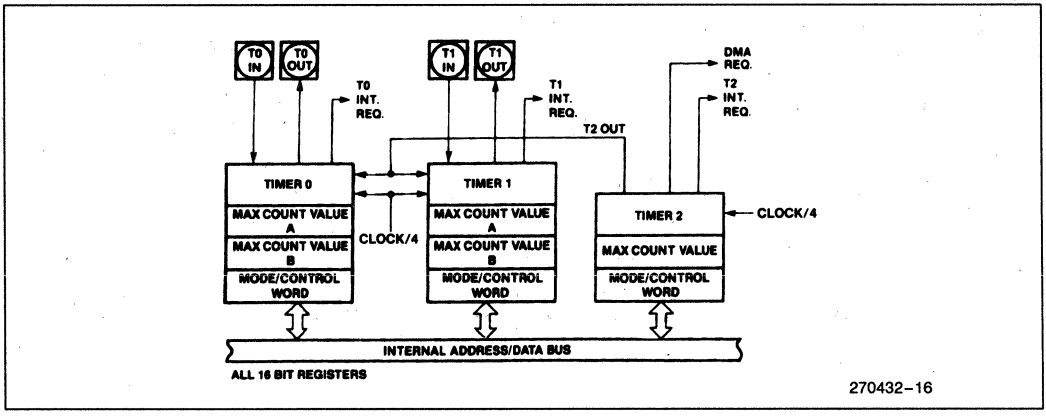

Figure 19. Timer Block Diagram

Timer Operation

The timers are controlled by 11 16-bit registers in the peripheral control block. The configuration of these registers is shown in Table 15. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a MAX COUNT register, which defines the maximum count the timer will reach. After reaching the MAX COUNT register value, the timer count value will reset to zero during that same clock, i.e., the maximum count value is never stored in the count register itself. Timers 0 and 1 are, in addition, equipped with a second MAX COUNT register, which enables the timers to alternate their count between two different MAX COUNT values. If a single MAX COUNT register is used, the timer output pin will switch LOW for a single clock, 1 clock after the maximum count value has been reached. In the dual MAX COUNT register mode, the output pin will indicate which MAX COUNT register is currently in use, thus allowing nearly complete freedom in selecting waveform duty cycles. For the timers with two MAX COUNT registers, the RIU bit in the control register determines which is used for the comparison.

Each timer gets serviced every fourth CPU-clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU-clock rate. Due to internal synchronization and pipelining of the timer circuitry, a timer output may take up to 6 clocks to respond to any individual clock or gate input.

Since the count registers and the maximum count registers are all 16 bits wide, 16 bits of resolution are provided. Any Read or Write access to the timers will add one wait state to the minimum four-clock bus cycle, however. This is needed to synchronize and coordinate the internal data flows between the internal timers and the internal bus.

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between MAX COUNT registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

These options are selectable via the timer mode/control word.

Timer Mode/Control Register

The mode/control register (see Figure 20) allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

Table 15. Timer Control Block Format

Register Name	Register Offset		
	Tmr. 0	Tmr. 1	Tmr. 2
Mode/Control Word	56H	5EH	66H
Max Count B	54H	5CH	not present
Max Count A	52H	5AH	62H
Count Register	50H	58H	60H

24

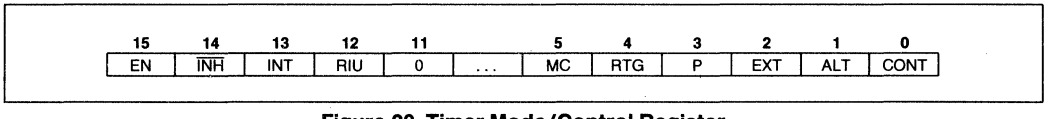

Figure 20. Timer Mode/Control Register

EN:

The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transistions during the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

$\overline{\text{INH}}$:

The inhibit bit allows for selective updating of the enable (EN) bit. If $\overline{\text{INH}}$ is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If $\overline{\text{INH}}$ is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT:

When set, the INT bit enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual MAX CONT register mode, an interrupt will be generated each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the Interrupt Controller).

RIU:

The Register In Use bit indicates which MAX COUNT register is currently being used for comparison to the timer count value. A zero value indicates register A. The RIU bit cannot be written, i.e., its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.

MC:

The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. This bit is set regardless of the timer's interrupt-enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts.

Programmer intervention is required to clear this bit.

RTG:

Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is HIGH, the timer will count; if the input pin is LOW, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the 80C188 clock.

When RTG = 1, the input pin detects LOW-to-HIGH transitions. The first such transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

P:

The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

EXT:

The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the 80C188 clock. If this bit is set, the timer will count LOW-to-HIGH transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input to output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

ALT:

The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method of generating non-repetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will go LOW for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT:

Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset, and halt.

Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Count Registers

Each of the three timers has a 16-bit count register. The contents of this register may be read or written by the processor at any time. If the register is written while the timer is counting,the new value will take effect in the current count cycle.

The count registers should be programmed before attempting to use the timers since they are not automatically initialized to zero.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two max count values whenever the current maximum count is reached.

A timer resets when the timer count register equals the max count value being used. If the timer count register or the max count register is changed so that the max count is less than the timer count, the timer does not immediately reset. Instead, the timer counts up to 0FFFFH, "wraps around" to zero, counts up to the max count value, and then resets.

Timers and Reset

Upon RESET, the state of the timers will be as follows:

- All EN (Enable) bits are reset preventing timer counting.
- For Timers 0 and 1, the RIU bits are reset to zero and the ALT bits are set to one. This results in the Timer Out pins going HIGH.
- The contents of the count registers are indeterminate.

INTERRUPT CONTROLLER

The 80C188 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The 80C188 interrupt controller has its own control register that sets the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Figure 21.

The 80C188 has a special Slave Mode in which the internal interrupt controller acts as a slave to an external master. The controller is programmed into this mode by setting bit 14 in the peripheral control block relocation register. (See Slave Mode section.)

MASTER MODE OPERATION

Interrupt Controller External Interface

Five pins are provided for external interrupt sources. One of these pins is NMI, the non-maskable interrupt. NMI is generally used for unusual events such as power-fail interrupts. The other four pins may be configured in any of the following ways:

- As four interrupt input lines with internally generated interrupt vectors.
- As an interrupt line and interrupt acknowledge line pair (cascade mode) with externally generated interrupt vectors plus two interrupt input lines with internally generated vectors.
- As two pairs of interrupt/interrupt acknowledge lines (Cascade Mode) with externally generated interrupt vectors.

External sources in the Cascade Mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the 80C188 on the second cycle. The capability to interface to external 82C59A programmable interrupt controllers is provided when the inputs are configured in Cascade Mode.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the 82C59A. The interrupt controller responds identically to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

Fully Nested Mode

When in the fully nested mode four pins are used as direct interrupt requests as in Figure 22. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate with interrupts enabled, yet be suspended only by interrupts of higher priority than the in-service interrupt.

When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register. This is required to allow subsequent interrupts from this interrupt source and to allow servicing of lower-priority interrupts. An EOI command is executed at the end of the service routine just before the return from interrupt instruction. If the fully nested structure has been upheld, the next highest-priority source with its IS bit set is then serviced.

Cascade Mode

The 80C188 has four interrupt pins and two of them have dual functions. In the fully nested mode the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In the Cascade Mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. The interconnection is shown in Figure 23. INT0 is an interrupt input interfaced to an 82C59A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to that peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the Cascade or non-Cascade Mode by programming the proper value into INT0 and INT1 control registers. The use of the dedicated acknowledge signals eliminates the need for the use of external logic to generate $\overline{\text{INTA}}$ and device select signals.

The primary Cascade Mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave 82C59As. Three levels of priority are created, requiring priority resolution in the 80C188 interrupt controller, the master 82C59As, and the slave 82C59As. If an external interrupt is serviced, one IS bit is set at each of these levels. When the interrupt service routine is completed, up to three end-of-interrupt commands must be issued by the programmer.

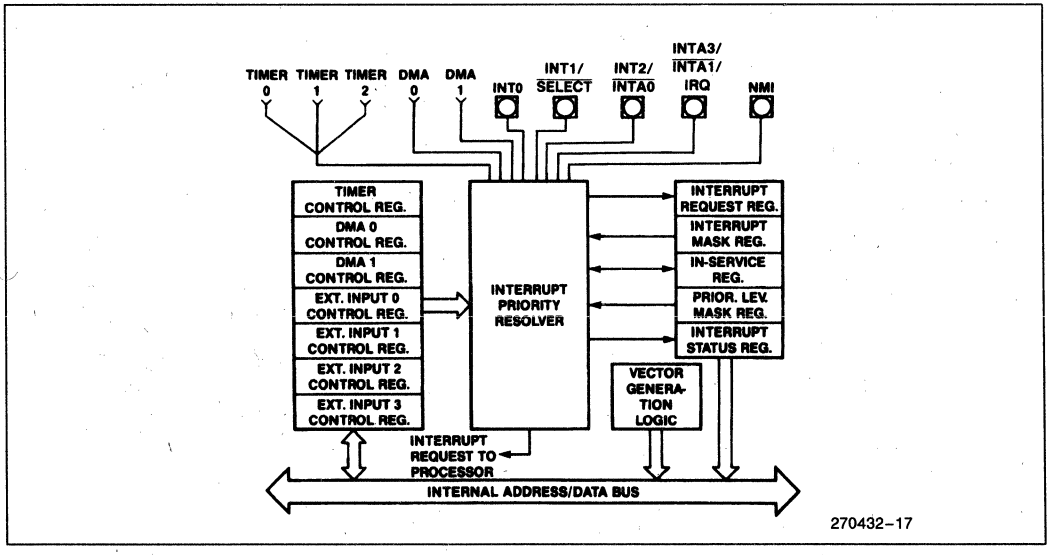

Figure 21. Interrupt Controller Block Diagram

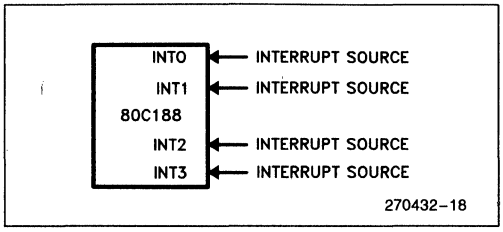

Figure 22. Fully Nested (Direct) Mode Interrupt Controller Connections

Special Fully Nested Mode

This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external 82C59A masters. Normally, an interrupt request from an interrupt source will not be recognized unless the in-service bit for that source is reset. If more than one interrupt source is connected to an external interrupt controller, all of the interrupts will be funneled through the same 80C188 interrupt request pin. As a result, if the external interrupt controller receives a higher-priority interrupt, its interrupt will not be recognized by the 80C188 controller until the 80C188 in-service bit is reset. In Special Fully Nested Mode, the 80C188 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interrupts from a single pin. An in-service bit will continue to be set, however, to inhibit interrupts from other lower-priority 80C188 interrupt sources.

Special procedures should be followed when resetting IS bits at the end of interrupt service routines. Software polling of the IS register in the external master 82C59A is required to determine if there is more than one bit set. If so, the IS bit in the 80C188 remains active and the next interrupt service routine is entered.

Operation in a Polled Environment

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the Poll Word (Figure 32). Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service. Bits 0–4 indicate to the processor the type vector of the highest-priority source requesting service. Reading the Poll Word causes the In-Service bit of the highest priority source to be set.

It is desirable to be able to read the Poll Word information without guaranteeing service of any pending interrupt, i.e., not set the indicated in-service bit. The 80C188 provides a Poll Status Word in addition to the conventional Poll Word to allow this to be done. Poll Word information is duplicated in the Poll Status Word, but reading the Poll Status Word does not set the associated in-service bit. These words are located in two adjacent memory locations in the register file.

Master Mode Features

Programmable Priority

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority). All interrupt sources have preprogrammed default priority levels (see Table 4).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 4 is used. If the serviced interrupt routine reenables interrupts, other interrupt requests can be serviced.

End-of-Interrupt Command

The end-of-interrupt (EOI) command is used by the programmer to reset the In-Service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The nonspecific command does not specify which IS bit is reset. When issued, the interrupt controller automatically resets the IS bit of the highest priority source with an active service routine. A specific EOI command requires that the programmer send the interrupt vector type to the interrupt controller indicating which source's IS bit is to be reset. This command is used when the fully nested structure has been disturbed or the highest priority IS bit that was set does not belong to the service routine in progress.

Trigger Mode

The four external interrupt pins can be programmed in either edge- or level-trigger mode. The control register for each external source has a level-trigger mode (LTM) bit. All interrupt inputs are active HIGH. In the edge sense mode or the level-trigger mode, the interrupt request must remain active (HIGH) until the interrupt request is acknowledged by the

80C188 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go LOW for at least one clock cycle to re-enable the input. In the level-trigger mode, no such provision is made: holding the interrupt input HIGH will cause continuous interrupt requests.

Interrupt Vectoring

The 80C186 Interrupt Controller will generate interrupt vectors for the integrated DMA channels and the integrated Timers. In addition, the Interrupt Controller will generate interrupt vectors for the external interrupt lines if they are not configured in Cascade or Special Fully Nested Mode. The interrupt vectors generated are fixed and cannot be changed (see Table 4).

Interrupt Controller Registers

The Interrupt Controller register model is shown in Figure 24. It contains 15 registers. All registers can both be read or written unless specified otherwise.

In-Service Register

This register can be read from or written into. The format is shown in Figure 25. It contains the In-Service bit for each of the interrupt sources. The In-Service bit is set to indicate that a source's service routine is in progress. When an In-Service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the In-Service bit for all three timers; the D0 and D1 bits are the In-Service bits for the two DMA channels; the I0–I3 are the In-Service bits for the external interrupt pins. The IS bit is set when the processor acknowledges an interrupt request either by an interrupt acknowledge or by reading the poll register. The IS bit is reset at the end of the interrupt service routine by an end-of-interrupt command.

Interrupt Request Register

The internal interrupt sources have interrupt request bits inside the interrupt controller. The format of this register is shown in Figure 25. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

The state of the external interrupt input pins is also indicated. The state of the external interrupt pins is not a stored condition inside the interrupt controller, therefore the external interrupt bits cannot be written. The external interrupt request bits are set when an interrupt request is given to the interrupt controller, so if edge-triggered mode is selected, the bit in the register will be HIGH only after an inactive-to-active transition. For internal interrupt sources, the register bits are set when a request arrives and are reset when the processor acknowledges the requests.

Writes to the interrupt request register will affect the D0 and D1 interrupt request bits. Setting either bit will cause the corresponding interrupt request while clearing either bit will remove the corresponding interrupt request. All other bits in the register are read-only.

Mask Register

This is a 16-bit register that contains a mask bit for each interrupt source. The format for this register is shown in Figure 25. A one in a bit position corre-

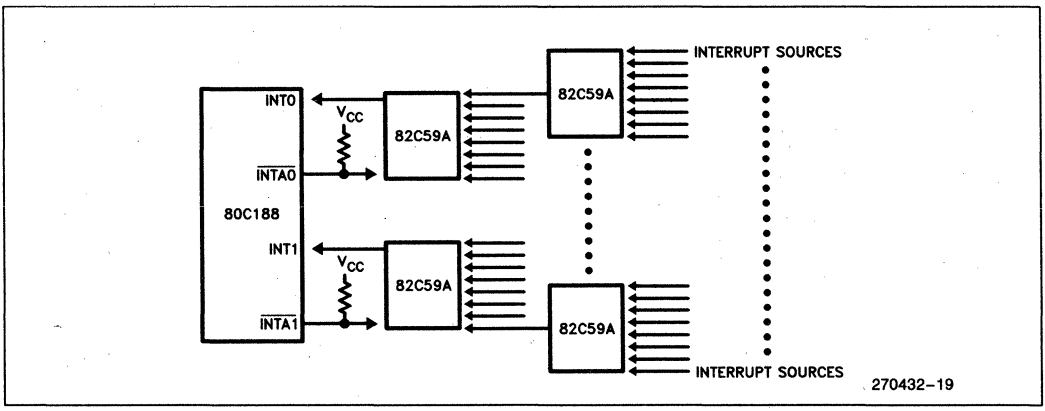

Figure 23. Cascade and Special Fully Nested Mode Interrupt Controller Connections

sponding to a particular source masks the source from generating interrupts. These mask bits are the exact same bits which are used in the individual control registers; programming a mask bit using the mask register will also change this bit in the individual control registers, and vice versa.

	OFFSET
INT3 CONTROL REGISTER	3EH
INT2 CONTROL REGISTER	3CH
INT1 CONTROL REGISTER	3AH
INT0 CONTROL REGISTER	38H
DMA 1 CONTROL REGISTER	36H
DMA 0 CONTROL REGISTER	34H
TIMER CONTROL REGISTER	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY MASK REGISTER	2AH
MASK REGISTER	28H
POLL STATUS REGISTER	26H
POLL REGISTER	24H
EOI REGISTER	22H

Figure 24. Interrupt Controller Registers (Master Mode)

Priority Mask Register

This register masks all interrupts below a particular interrupt priority level. The format of this register is shown in Figure 26. The code in the lower three bits of this register inhibits interrupts of priority lower (a higher priority number) than the code specified. For example, 100 written into this register masks interrupts of level five (101), six (110), and seven (111). The register is reset to seven (111) upon RESET so no interrupts are masked due to priority number.

Interrupt Status Register

This register contains general interrupt controller status information. The format of this register is shown in Figure 27. The bits in the status register have the following functions:

DHLT: DMA Halt Transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed. This bit allows prompt service of all non-maskable interrupts. This bit may also be set by the programmer.

IRTx: These three bits represent the individual timer interrupt request bits. These bits differentiate between timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt request. Note that setting any one of these three bits initiates an interrupt request to the interrupt controller.

24

15	14	•	•	•	10	9	8	7	6	5	4	3	2	1	0
0	0	•	•	•	0	0	0	I3	I2	I1	I0	D1	D0	0	TMR

Figure 25. In-Service, Interrupt Request, and Mask Register Formats

15	14	•	•	•	•	•	•	•	•	•	3	2	1	0
0	0	•	•	•	•	•	•	•	•	•	0	PRM2	PRM1	PRM0

Figure 26. Priority Mask Register Format

15	14	•	•	•	•	•	7	6	5	4	3	2	1	0
DHLT	0	•	•	•	•	•	0	0	0	0	0	IRT2	IRT1	IRT0

Figure 27. Interrupt Status Register Format (Master Mode)

Timer, DMA 0, 1; Control Register

These registers are the control words for all the internal interrupt sources. The format for these registers is shown in Figure 28. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits interrupt requests from the interrupt source. The MSK bits in the individual control registers are the exact same bits as are in the Mask Register; modifying them in the individual control registers will also modify them in the Mask Register, and vice versa.

INT0-INT3 Control Registers

These registers are the control words for the four external input pins. Figure 29 shows the format of the INT0 and INT1 Control registers; Figure 30 shows the format of the INT2 and INT3 Control registers. In Cascade Mode or Special Fully Nested Mode, the control words for INT2 and INT3 are not used.

The bits in the various control registers are encoded as follows:

PRO-2: Priority programming information. Highest Priority = 000, Lowest Priority = 111

LTM: Level-trigger mode bit. 1 = level-triggered; 0 = edge-triggered. Interrupt Input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = non-mask.

C: Cascade mode bit, 1 = cascade; 0 = direct

SFNM: Special Fully Nested Mode bit, 1 = SFNM

EOI Register

The end of the interrupt register is a command register which can only be written into. The format of this register is shown in Figure 31. It initiates an EOI command when written to by the 80C188 CPU.

The bits in the EOI register are encoded as follows:

S_x: Encoded information that specifies an interrupt source vector type as shown in Table 4. For example, to reset the In-Service bit for DMA channel 0, these bits should be set to 01010, since the vector type for DMA channel 0 is 10.

NOTE:

To reset the single In-Service bit for any of the three timers, the vector type for timer 0 (8) should be written in this register.

NSPEC/SPEC: A bit that determines the type of EOI command. Nonspecific = 1, Specific = 0.

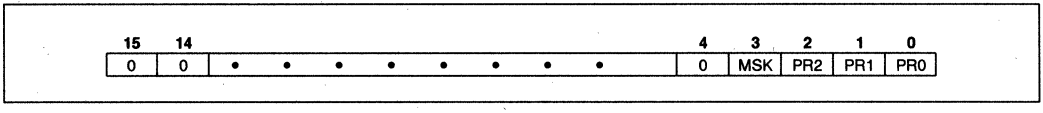

Figure 28. Timer/DMA Control Registers Formats

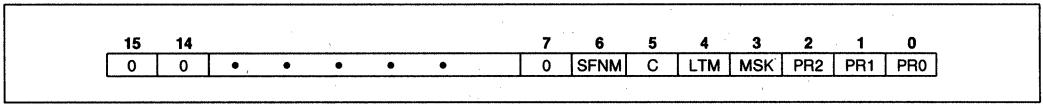

Figure 29. INT0/INT1 Control Register Formats

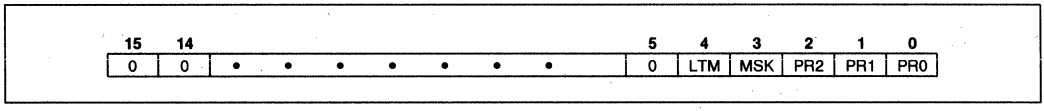

Figure 30. INT2/INT3 Control Register Formats

Poll and Poll Status Registers

These registers contain polling information. The format of these registers is shown in Figure 32. They can only be read. Reading the Poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt. Reading the poll status register will not set the IS bit of the highest priority pending interrupt; only the status of pending interrupts will be provided.

Encoding of the Poll and Poll Status register bits are as follows:

S_x: Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt Request = 1; no Interrupt Request = 0.

SLAVE MODE OPERATION

When Slave Mode is used, the internal 80C188 interrupt controller will be used as a slave controller to an external master interrupt controller. The internal 80C188 resources will be monitored by the internal interrupt controller, while the external controller functions as the system master interrupt controller.

Upon reset, the 80C188 will be in master mode. To provide for slave mode operation bit 14 of the relocation register should be set.

Because of pin limitations caused by the need to interface to an external 82C59A master, the internal interrupt controller will no longer accept external inputs. There are however, enough 80C188 interrupt controller inputs (internally) to dedicate one to each timer. In this mode, each timer interrupt source has its own mask bit, IS bit, and control word.

In Slave Mode each peripheral must be assigned a unique priority to ensure proper interrupt controller operation. Therefore, it is the programmer's responsibility to assign correct priorities and initialize interrupt control registers before enabling interrupts.

Slave Mode External Interface

The configuration of the 80C188 with respect to an external 82C59A master is shown in Figure 33. The INT0 (Pin 45) input is used as the 80C188 CPU interrupt input. IRQ (Pin 41) functions as an output to send the 80C188 slave-interrupt-request to one of the 8 master-PIC-inputs.

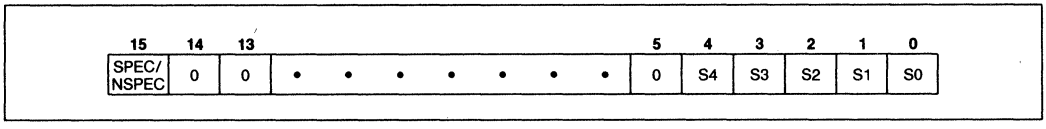

Figure 31. EOI Register Format

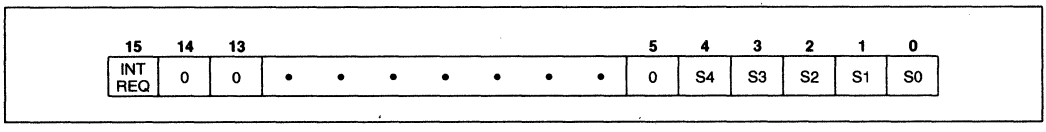

Figure 32. Poll and Poll Status Register Format

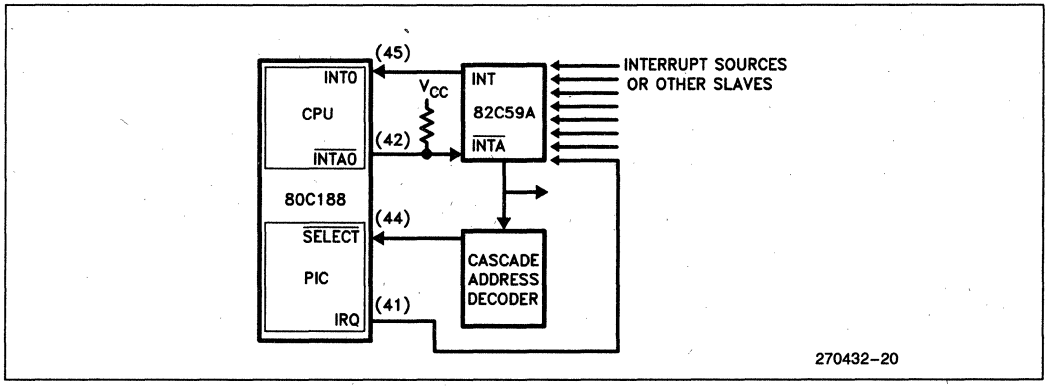

Figure 33. Slave Mode Interrupt Controller Connections

Correct master-slave interface requires decoding of the slave addresses (CAS0-2). Slave 82C59As do this internally. Because of pin limitations, the 80C188 slave address will have to be decoded externally. $\overline{\text{SELECT}}$ (Pin 44) is used as a slave-select input. Note that the slave vector address is transferred internally, but the READY input must be supplied externally.

$\overline{\text{INTA0}}$ (Pin 42) is used as an acknowledge output, suitable to drive the $\overline{\text{INTA}}$ input of an 82C59A.

Interrupt Nesting

Slave Mode operation allows nesting of interrupt requests. When an interrupt is acknowledged, the priority logic masks off all priority levels except those with equal or higher priority.

Vector Generation in the Slave Mode

Vector generation in Slave Mode is exactly like that of an 8259A or 82C59A slave. The interrupt controller generates an 8-bit vector type number which the CPU multiplies by four to use as an address into the vector table. The five most significant bits of this type number are user-programmable while the three least significant bits are defined according to Figure 34. The significant five bits of the vector are programmed by writing to the Interrupt Vector register at offset 20H.

Specific End-of-Interrupt

In Slave Mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset. The command is executed by writing the correct value in the Specific EOI register at offset 22H.

Interrupt Controller Registers in the Slave Mode

All control and command registers are located inside the internal peripheral control block. Figure 34 shows the offsets of these registers.

End-of-Interrupt Register

The end-of-interrupt register is a command register which can only be written. The format of this register is shown in Figure 35. It initiates an EOI command when written by the 80C188 CPU.

The bits in the EOI register are encoded as follows:

VT_X: Three least-significant vector type bits corresponding to the source for which the IS bit is to be reset. Figure 34 indicates these bits.

In-Service Register

This register can be read from or written into. It contains the in-service bit for each of the internal interrupt sources. The format for this register is shown in Figure 36. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers. The source's IS bit is set when the processor acknowledges its interrupt request.

Interrupt Request Register

This register indicates which internal peripherals have interrupt requests pending. The format of this register is shown in Figure 36. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request. As in Master Mode, D0 and D1 are read/write; all other bits are read only.

Mask Register

This register contains a mask bit for each interrupt source. The format for this register is shown in Figure 36. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked. These mask bits are exactly the same bits which are used in the individual control registers, i.e., changing the state of a mask bit in this register will also change the state of the mask bit in the individual interrupt control register corresponding to the bit.

Control Registers

These registers are the control words for all the internal interrupt sources. The format of these registers is shown in Figure 37. Each of the timers and both of the DMA channels have their own Control Register.

The bits of the Control Registers are encoded as follows:

pr_x: 3-bit encoded field indicating a priority level for the source.

msk: mask bit for the priority level indicated by pr_x bits.

	OFFSET
TIMER 2 CONTROL REGISTER (VECTOR TYPE xxxxx101)	3AH
TIMER 1 CONTROL REGISTER (VECTOR TYPE xxxxx100)	38H
DMA 1 CONTROL REGISTER (VECTOR TYPE xxxxx011)	36H
DMA 0 CONTROL REGISTER (VECTOR TYPE xxxxx010)	34H
TIMER 0 CONTROL REGISTER (VECTOR TYPE xxxxx000)	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT-REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY-LEVEL MASK REGISTER	2AH
MASK REGISTER	28H
SPECIFIC EOI REGISTER	22H
INTERRUPT VECTOR REGISTER	20H

Figure 34. Interrupt Controller Registers (Slave Mode)

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15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	0	0	0	VT2	VT1	VT0

Figure 35. Specific EOI Register Format

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	TMR2	TMR1	D1	D0	0	TMR0

Figure 36. In-Service, Interrupt Request, and Mask Register Format

Interrupt Vector Register

This register provides the upper five bits of the interrupt vector address. The format of this register is shown in Figure 38. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.

The format of the bits in this register is:

t_X: 5-bit field indicating the upper five bits of the vector address.

Priority-Level Mask Register

This register indicates the lowest priority-level interrupt which will be serviced.

The encoding of the bits in this register is:

m_X: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

Interrupt Status Register

This register is defined as in Master Mode except that DHLT is not implemented (see Figure 27).

Interrupt Controller and Reset

Upon RESET, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying Fully Nested Mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All Interrupt Service bits reset to 0.
- All Interrupt Request bits reset to 0.
- All MSK (Interrupt Mask) bits set to 1 (mask).
- All C (Cascade) bits reset to 0 (non-Cascade).
- All PRM (Priority Mask) bits set to 1, implying no levels masked.
- Initialized to Master Mode.

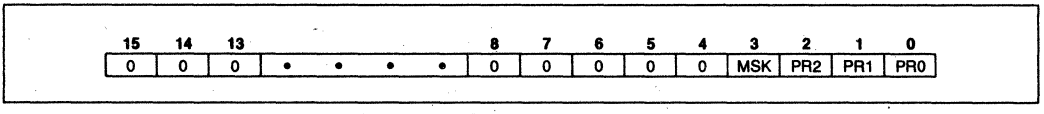


Figure 37. Control Word Format

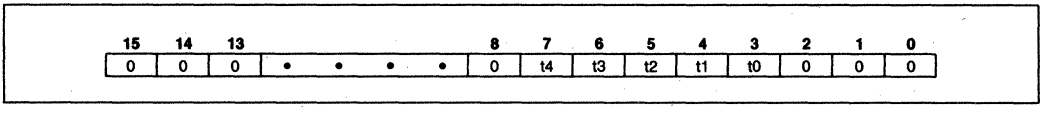


Figure 38. Interrupt Vector Register Format

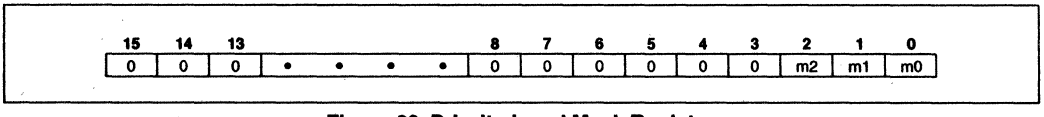


Figure 39. Priority Level Mask Register

Enhanced Mode Operation

In Compatible Mode the 80C188 operates with all the features of the NMOS 80188, with the exception of 8087 support (i.e. no numeric coprocessing is possible). Queue-Status information is still available for design purposes other than 8087 support.

All the Enhanced Mode features are completely masked when in Compatible Mode. A write to any of the Enhanced Mode registers will have no effect, while a read will not return any valid data.

In Enhanced Mode, the 80C188 will operate with Power-Save and DRAM refresh, in addition to all the Compatible Mode features.

Entering Enhanced Mode

Enhanced mode can be entered by tying the RESET output signal from the 80C188 to the TEST/BUSY input.

Queue-Status Mode

The queue-status mode is entered by strapping the $\overline{RD}$ pin low. $\overline{RD}$ is sampled at RESET and if LOW, the 80C188 will reconfigure the ALE and $\overline{WR}$ pins to be QS0 and QS1 respectively. This mode is available on the 80C188 in both Compatible and Enhanced Modes.

DRAM Refresh Control Unit Description

The Refresh Control Unit (RCU) automatically generates DRAM refresh bus cycles. The RCU operates only in Enhanced Mode. After a programmable period of time, the RCU generates a memory read request to the BIU. If the address generated during a refresh bus cycle is within the range of a properly programmed chip select, that chip select will be activated when the BIU executes the refresh bus cycle. The ready logic and wait states programmed for that region will also be in force. If no chip select is activated, then external ready is automatically required to terminate the refresh bus cycle.

If the HLDA pin is active when a DRAM refresh request is generated (indicating a bus hold condition), then the 80C188 will deactivate the HLDA pin in order to perform a refresh cycle. The circuit external to the 80C188 must remove the HOLD signal for at least one clock in order to execute the refresh cycle. The sequence of HLDA going inactive while HOLD is being held active can be used to signal a pending refresh request.

All registers controlling DRAM refresh may be read and written in Enhanced Mode. When the processor is operating in Compatible Mode, they are deselected and are therefore inaccessible. Some fields of these registers cannot be written and are always read as zeros.

DRAM Refresh Addresses

The address generated during a refresh cycle is determined by the contents of the MDRAM register (see Figure 40) and the contents of a 9-bit counter. Figure 41 illustrates the origin of each bit.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDRAM: Offset E0H	M6	M5	M4	M3	M2	M1	M0	0	0	0	0	0	0	0	0	0

Bits 0–8: Reserved, read back as 0.

Bits 9–15: M0–M6, are address bits A13–A19 of the 20-bit memory refresh address. These bits should correspond to any chip select address to be activated for the DRAM partition. These bits are cleared to 0 on RESET.

Figure 40. Memory Partition Register

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
M6	M5	M4	M3	M2	M1	M0	0	0	0	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	1

M6–M0: Bits defined by MDRAM Register

CA8–CA0: Bits defined by refresh address counter. These bits change according to a linear/feedback shift register; they do not directly follow a binary count.

Figure 41. Addresses Generated by RCU

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDRAM: Offset E2H	0	0	0	0	0	0	0	C8	C7	C6	C5	C4	C3	C2	C1	C0

Bits 0–8: C0–C8, clock divisor register, holds the number of CLKOUT cycles between each refresh request.

Bits 9–15: Reserved, read back as 0.

Figure 42. Clock Pre-Scaler Register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EDRAM: Offset E4H	E	0	0	0	0	0	0	T8	T7	T6	T5	T4	T3	T2	T1	T0

Bits 0–8: T0–T8, refresh clock counter outputs. Read only.

Bits 9–14: Reserved, read back as 0.

Bit 15: Enable RCU, set to 0 on RESET.

Figure 43. Enable RCU Register

Refresh Control Unit Programming and Operation

After programming the MDRAM and the CDRAM registers (Figures 40 and 42), the RCU is enabled by setting the "E" bit in the EDRAM register (Figure 43). The clock counter (T0–T8 of EDRAM) will be loaded from C0–C8 of CDRAM during T_3 of instruction cycle that sets the "E" bit. The clock counter is then decremented at each subsequent CLKOUT.

A refresh is requested when the value of the counter has reached 1 and the counter is reloaded from CDRAM. In order to avoid missing refresh requests, the value in the CDRAM register should always be at least 18 (12H). Clearing the "E" bit at anytime will clear the counter and stop refresh requests, but will not reset the refresh address counter.

POWER-SAVE CONTROL

Power Save Operation

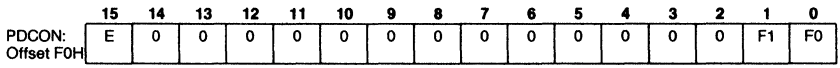
The 80C188, when in Enhanced Mode, can enter a power saving state by internally dividing the processor clock frequency by a programmable factor. This divided frequency is also available at the CLKOUT pin. The PDCON register contains the two-bit fields for selecting the clock division factor and the enable bit.

All internal logic, including the Refresh Control Unit and the timers, will have their clocks slowed down by the division factor. To maintain a real time count or a fixed DRAM refresh rate, these peripherals must be re-programmed when entering and leaving the power-save mode.

The power-save mode is exited whenever an interrupt is processed by automatically resetting the enable bit. If the power-save mode is to be re-entered after serving the interrupt, the enable bit will need to be set in software before returning from the interrupt routine.

The internal clocks of the 80C188 will begin to be divided during the T_3 state of the instruction cycle that sets the enable bit. Clearing the enable bit will restore full speed in the T_3 state of that instruction.

At no time should the internal clock frequency be allowed to fall below 0.5 MHz. This is the minimum operational frequency of the 80C188. For example, an 80C188 running with a 12 MHz crystal (6 MHz CLOCKOUT) should never have a clock divisor greater than eight.



Bits 0–1: Clock Divisor Select

F1	F0	Division Factor
0	0	divide by 1
0	1	divide by 4
1	0	divide by 8
1	1	divide by 16

Bits 2–14: Reserved, read back as zero.

Bit 15: Enable Power Save Mode. Set to zero on RESET.

Figure 44. Power-Save Control Register

ONCE™ Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C188 has a test mode available which allows all pins to be placed in a high-impedance state. ONCE stands for "ON Circuit Emulation". When placed in this mode, the 80C188 will put all pins in the high-impedance state until RESET.

The ONCE mode is selected by tying the $\overline{UCS}$ and the $\overline{LCS}$ LOW during RESET. These pins are sampled on the low-to-high transition of the $\overline{RES}$ pin. The $\overline{UCS}$ and the $\overline{LCS}$ pins have weak internal pull-up resistors similar to the $\overline{RD}$ and $\overline{TEST}$ pins to guarantee normal operation.

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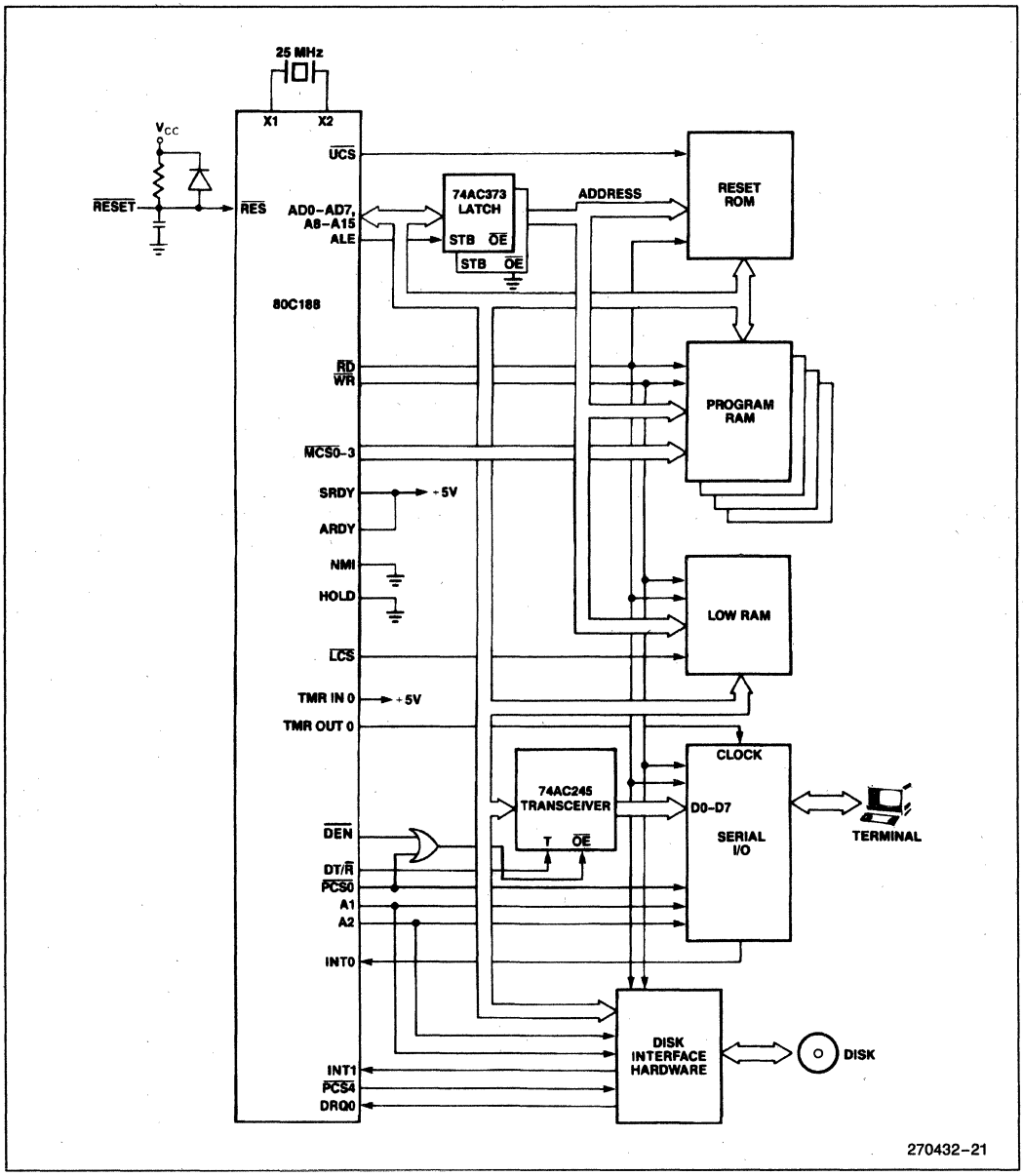

Figure 45. Typical 80C188 Computer

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with Respect to Ground .....−1.0V to +7.0V
Package Power Dissipation 1W

Not to exceed the maximum allowable die temperature based on thermal resistance of the package.

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±10% except V_{CC} = 5V ± 5% at f > 12.5 MHz

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except X1)	−0.5	0.2 V_{CC} − 0.3	V	
V_{IL2}	Clock Input Low Voltage (X1)	−0.5	0.6	V	
V_{IH}	Input High Voltage (All except X1, $\overline{RES}$, ARDY and SRDY)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage (SRDY, ARDY)	0.2 V_{CC} + 1.1	V_{CC} +0.5	V	
V_{IH3}	Clock Input High Voltage (X1)	3.9	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA (S0, 1, 2) I_{OL} = 2.0 mA (others)
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −2.4 mA @ 2.4V(4)
		V_{CC} − 0.5	V_{CC}	V	I_{OH} = −200 μA @ V_{CC} −0.5
I_{CC}	Power Supply Current		150	mA	@16 MHz, 0°C V_{CC} = 5.25V(3)
			120	mA	@12.5 MHz, 0°C V_{CC} = 5.5V(3)
			100	mA	@10 MHz, 0°C V_{CC} = 5.5V(3)
I_{LI}	Input Leakage Current		±10	μA	@0.5 MHz 0.45V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	μA	@0.5 MHz 0.45V ≤ V_{OUT} ≤ V_{CC}(1)
V_{CLO}	Clock Output Low		0.45	V	I_{CLO} = 4.0 mA
V_{CHO}	Clock Output High	V_{CC} − 0.5		V	I_{CHO} = −500 μA
C_{IN}	Input Capacitance		10	pF	@ 1 MHz(2)
C_{IO}	Output or I/O Capacitance		20	pF	@ 1 MHz(2)

NOTES:
1. Pins being floated during HOLD or by invoking the ONCE Mode.
2. Characterization conditions are a) Frequency = 1 MHz; b) Unmeasured pins at GND; c) V_{IN} at +5.0V or 0.45V. This parameter is not tested.
3. Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.
4. $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{TEST}$ pins have internal pullup devices. Loading some of these pins above I_{OH} = −200 μA can cause the 80C188 to go into alternative modes of operation. See the section on Local Bus Controller and Reset for details.

POWER SUPPLY CURRENT

Current is linearly proportional to clock frequency and is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.

Maximum current is given by I_{CC} = 8.4 mA × freq. (MHz) + 15 mA.

Typical current is given by I_{CC} (typ.) = 6.4 mA X freq. (MHz) +4.0 mA. "Typicals" are based on a limited number of samples taken from early manufacturing lots measured at V_{CC} = 5V and room temperature. "Typicals" are not guaranteed.

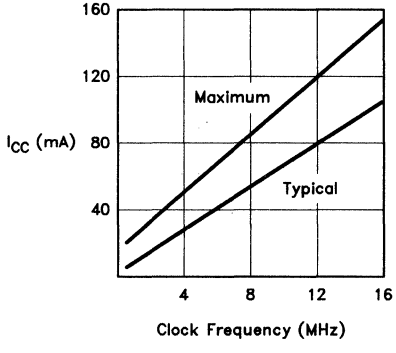

Figure 46. I_{CC} vs Frequency

A. C. CHARACTERISTICS

MAJOR CYCLE TIMINGS (READ CYCLE)

$T_A = 0^\circ C$ to $+70^\circ C$, V_{CC} = 5V ± 10% except V_{CC} = 5V± 5% at f > 12.5 MHz

All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	80C188		80C188-12		80C188-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C188 GENERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{DVCL}	Data in Setup (A/D)	15		15		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		3		ns	
80C188 GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	5	45	5	35	5	31	ns	
T_{CLSH}	Status Inactive Delay	5	46	5	35	5	30	ns	
T_{CLAV}	Address Valid Delay	5	44	5	36	5	33	ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	5	40	5	36	5	33	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		30		25		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		T_{CLCL} - 15		T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 18		T_{CLCH} - 15		T_{CLCH} - 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} - 15		T_{CHCL} - 15		T_{CHCL} - 15		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	T_{CLAX}	20	ns	
T_{CLCSV}	Chip-Select Active Delay	3	42	3	33	3	30	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} - 10		T_{CLCH} - 10		T_{CLCH} - 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	5	35	5	30	5	25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	44	3	37	3	31	ns	
T_{CVDEX}	$\overline{DEN}$ Inctive Delay	5	44	5	37	5	31	ns	
T_{CHCTV}	Control Active Delay 2	5	44	5	37	5	31	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	3	35	ns	
80C188 TIMING RESPONSES (Read Cycle)									
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	5	44	5	37	5	31	ns	
T_{RLRH}	$\overline{RD}$ Pulse Width	$2T_{CLCL}$ - 30		$2T_{CLCL}$ - 25		$2T_{CLCL}$ - 25		ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	5	44	5	37	5	31	ns	
T_{RHLH}	$\overline{RD}$ Inactive to ALE High	T_{CLCH} - 14		T_{CLCH} - 14		T_{CLCH} - 14		ns	Equal Loading
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	T_{CLCL} - 15		T_{CLCL} - 15		T_{CLCL} - 15		ns	Equal Loading

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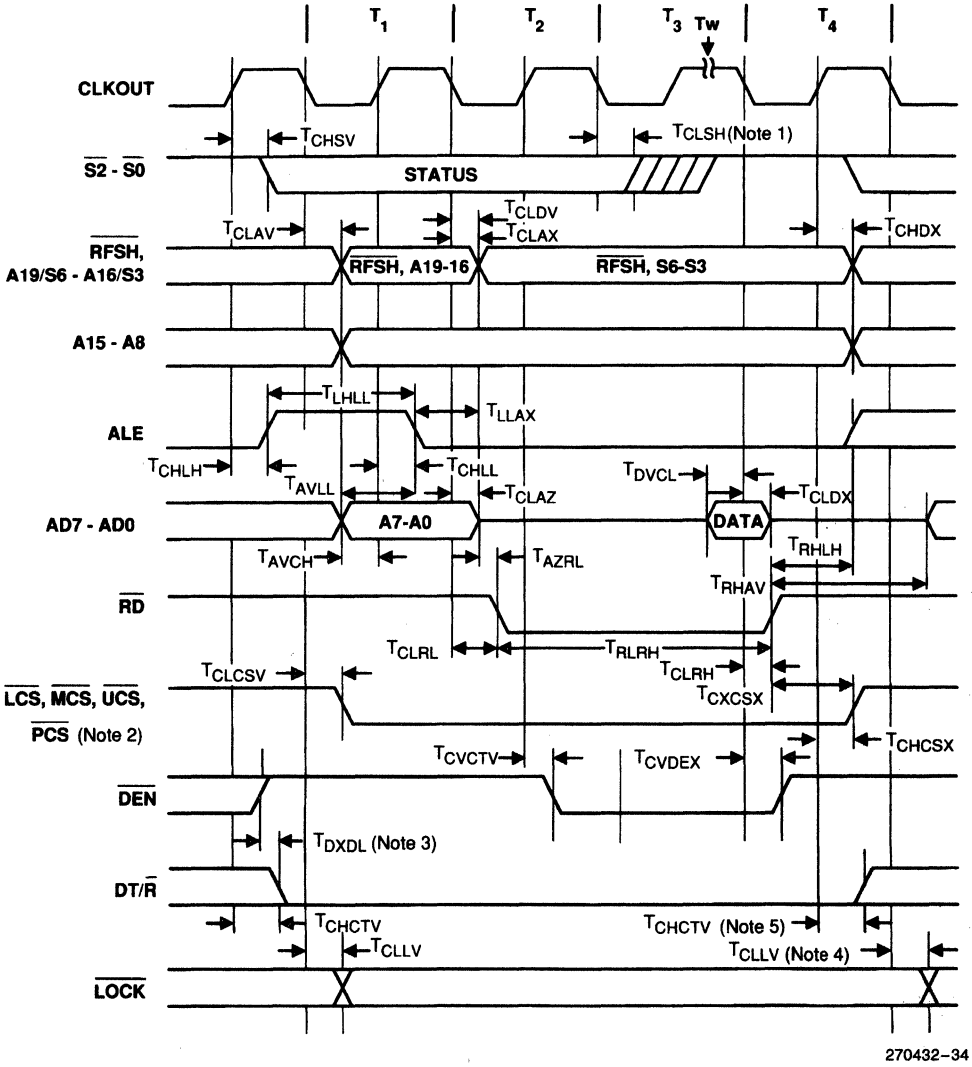
A.C. CHARACTERISTICS

READ CYCLE WAVEFORMS



NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by write.

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A. C. CHARACTERISTICS

MAJOR CYCLE TIMINGS (WRITE CYCLE)

$T_A = 0\ ^{\circ}C$ to $+70\ ^{\circ}C$, $V_{CC} = 5V \pm 10\%$ except $V_{CC} = 5V \pm 5\%$ at $f > 12.5$ MHz

All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50\text{-}200$ pF (10 MHz) and $C_L = 50\text{-}100$ pF (12.5-16 MHz).
For A.C. tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	80C188		80C188-12		80C188-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C188 GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	5	45	5	35	5	31	ns	
T_{CLSH}	Status Inactive Delay	5	46	5	35	5	30	ns	
T_{CLAV}	Address Valid Delay	5	44	5	36	5	33	ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	5	40	5	36	5	33	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		30		25		20	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		30		25		20	ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH} - 18$		$T_{CLCH} - 15$		$T_{CLCH} - 15$		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	$T_{CHCL} - 15$		$T_{CHCL} - 15$		$T_{CHCL} - 15$		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLDOX}	Data Hold Time	3		3		3		ns	
T_{CVCTV}	Control Active Delay 1	3	44	3	37	3	31	ns	
T_{CVCTX}	Control Inactive Delay	3	44	3	37	3	31	ns	
T_{CLCSV}	Chip-Select Active Delay	3	42	3	33	3	30	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	$T_{CLCH} - 10$		$T_{CLCH} - 10$		$T_{CLCH} - 10$		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	5	35	5	30	5	25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	3	35	ns	
80C188 TIMING RESPONSES (Write Cycle)									
T_{WLWH}	$\overline{WR}$ Pulse Width	$2T_{CLCL} - 30$		$2T_{CLCL} - 25$		$2T_{CLCL} - 25$		ns	
T_{WHLH}	$\overline{WR}$ Inactive to ALE High	$T_{CLCH} - 14$		$T_{CLCH} - 14$		$T_{CLCH} - 14$		ns	Equal Loading
T_{WHDX}	Data Hold After $\overline{WR}$	$T_{CLCL} - 34$		$T_{CLCL} - 20$		$T_{CLCL} - 20$		ns	Equal Loading
T_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	$T_{CLCH} - 10$		$T_{CLCH} - 10$		$T_{CLCH} - 10$		ns	Equal Loading

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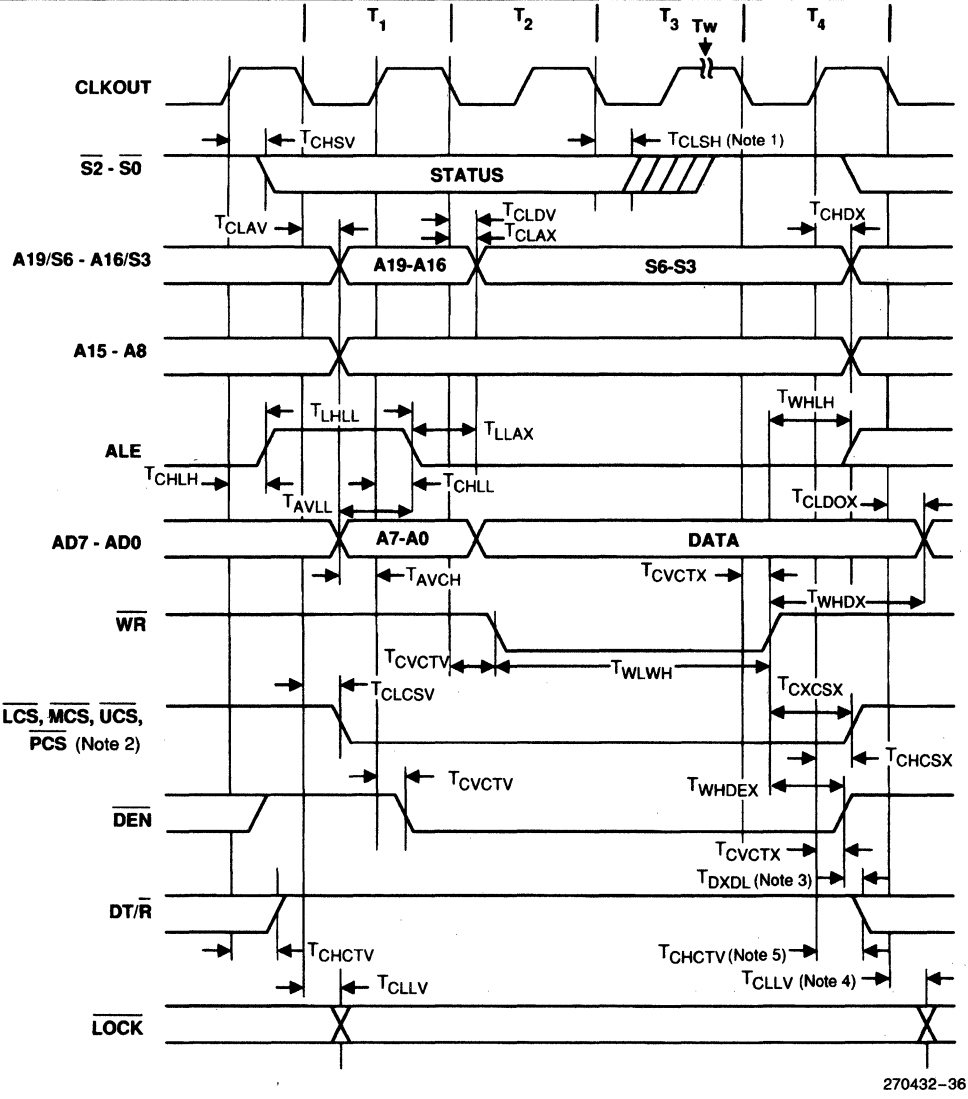
A.C. CHARACTERISTICS

WRITE CYCLE WAVEFORMS



NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by read, INTA, or halt.

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A. C. CHARACTERISTICS

MAJOR CYCLE TIMINGS (INTERRUPT ACKNOWLEDGE CYCLE)

$T_A = 0^\circ$ C to $+70^\circ$ C, $V_{CC} = 5V \pm 10\%$ except $V_{CC} = 5V \pm 5\%$ at f > 12.5 MHz

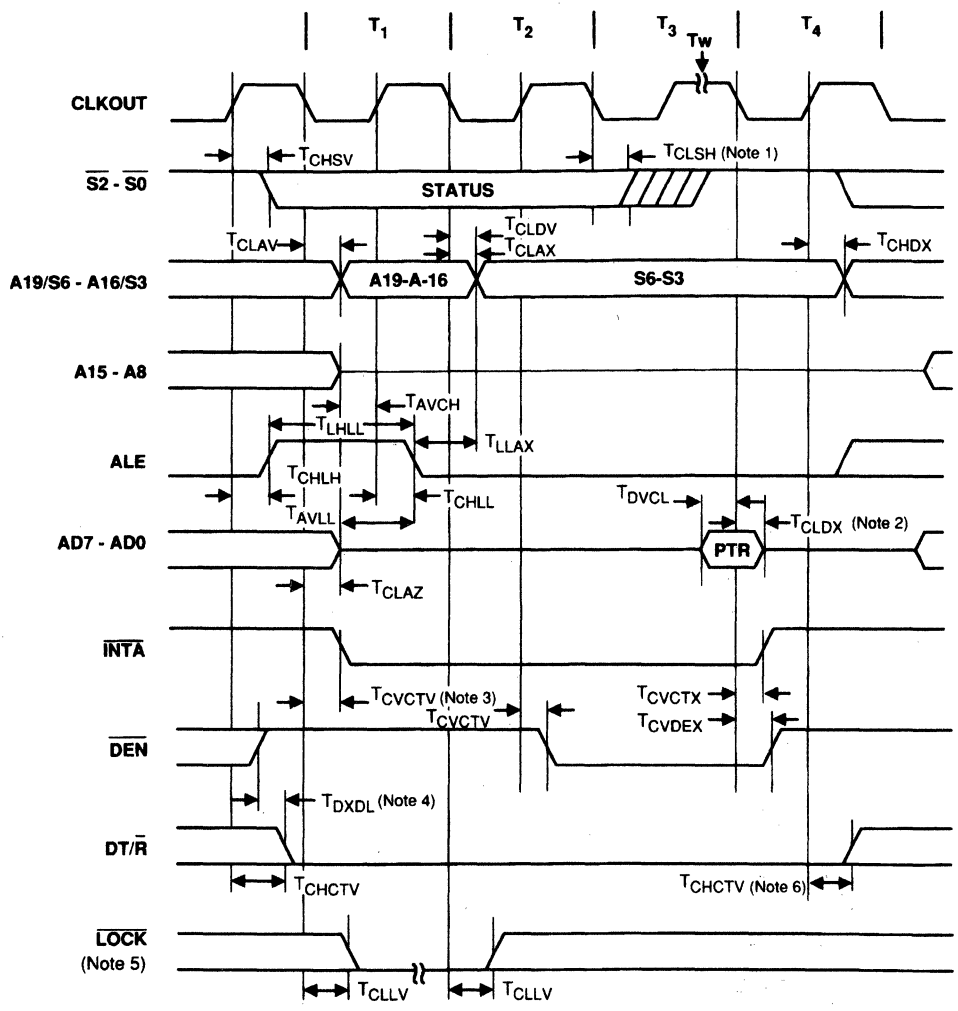
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	80C188		80C188-12		80C188-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C188 GENERAL TIMING REQUIREMENTS (Listed More Than Once)									
T_{DVCL}	Data in Setup (A/D)	15		15		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		3		ns	
80C188 GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	5	45	5	35	5	31	ns	
T_{CLSH}	Status Inactive Delay	5	46	5	35	5	30	ns	
T_{CLAV}	Address Valid Delay	5	44	5	36	5	33	ns	
T_{AVCH}	Address Valid to Clock High	0		0		0		ns	
T_{CLAX}	Address Hold	0		0		0		ns	
T_{CLDV}	Data Valid Delay	5	40	5	36	5	33	ns	
T_{CHDX}	Status Hold Time	10		10		10		ns	
T_{CHLH}	ALE Active Delay		30		25		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		T_{CLCL} - 15		T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 18		T_{CLCH} - 15		T_{CLCH} - 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} - 15		T_{CHCL} - 15		T_{CHCL} - 15		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	T_{CLAX}	20	ns	
T_{CVCTV}	Control Active Delay 1	3	44	3	37	3	31	ns	
T_{CVCTX}	Control Inactive Delay	3	44	3	37	3	31	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	5	44	5	37	5	31	ns	
T_{CVDEX}	$\overline{DEN}$ Inctive Delay (Non-Write Cycles)	5	44	5	37	5	31	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	3	35	ns	

270432-37

A. C. CHARACTERISTICS

INTERRUPT ACKNOWLEDGE CYCLE WAVEFORMS



NOTES:

1. Status inactive in state preceding T_4.
2. The data hold time lasts only until $\overline{INTA}$ goes inactive, even if the $\overline{INTA}$ transition occurs prior to T_{CLDX}(min).
3. $\overline{INTA}$ occurs one clock later in Slave Mode.
4. For write cycle followed by interrupt acknowledge cycle.
5. $\overline{LOCK}$ is active upon T_1 of the first interrupt acknowledge cycle and inactive upon T_2 of the second interrupt acknowledge cycle.
6. Changes in T-state preceding next bus cycle if followed by write.

270432-38

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A. C. CHARACTERISTICS

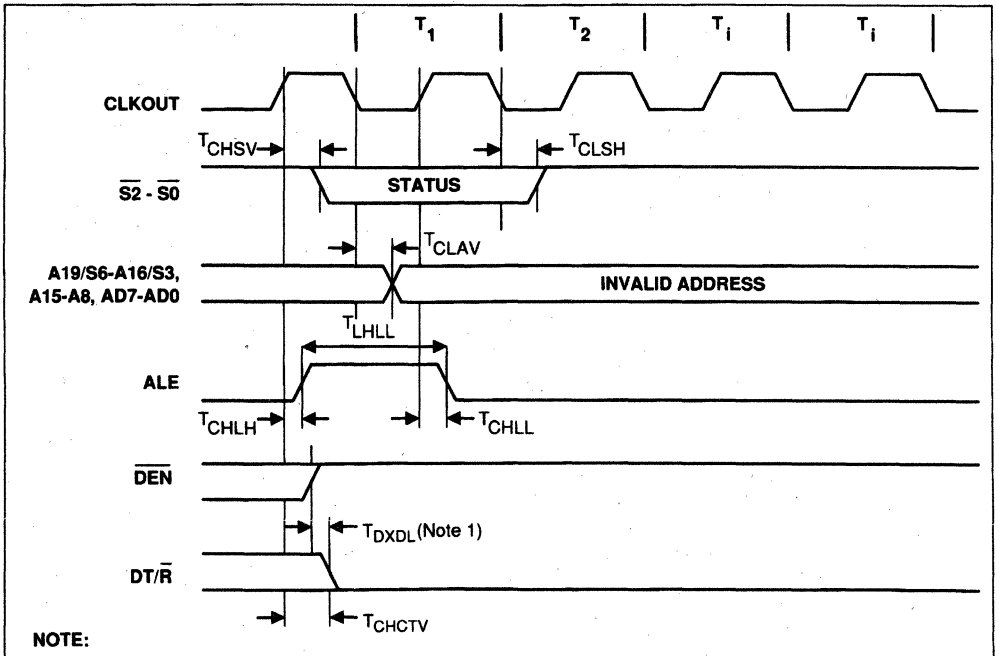
SOFTWARE HALT CYCLE TIMINGS

$T_A = 0^\circ C$ to $+70^\circ C$, V_{CC} = 5V ± 10% except V_{CC} = 5V ± 5% at f > 12.5 MHz

All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	80C188		80C188-12		80C188-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C188 GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CHSV}	Status Active Delay	5	45	5	35	5	31	ns	
T_{CLSH}	Status Inactive Delay	5	46	5	35	5	30	ns	
T_{CLAV}	Address Valid Delay	5	44	5	36	5	33	ns	
T_{CHLH}	ALE Active Delay		30		25		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		T_{CLCL} - 15		T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25		20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low		0		0		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	5	44	5	37	5	31	ns	

SOFTWARE HALT CYCLE WAVEFORMS



NOTE:
1. For write cycle followed by halt cycle.

270432-39

A. C. CHARACTERISTICS

CLOCK TIMINGS

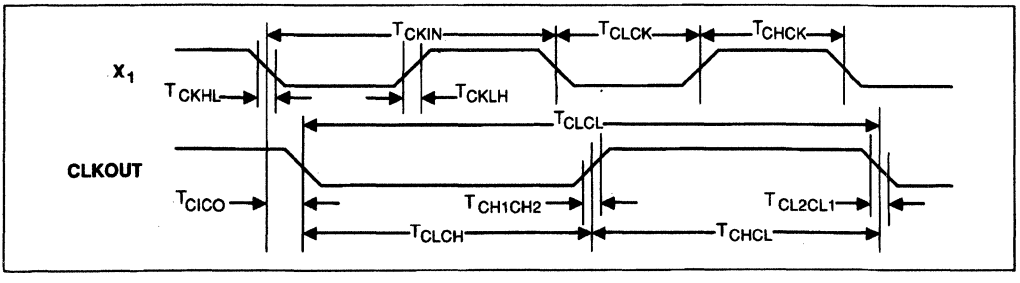
$T_A = 0^\circ C$ to $+70^\circ C$, V_{CC}= 5V ±10% except V_{CC}= 5V ±5% at f > 12.5 MHz

All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH}= 2.4V except at X1 where V_{IH}= V_{CC}- 0.5V.

Symbol	Parameter	80C188		80C188-12		80C188-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C188 CLKIN REQUIREMENTS Measurements taken with following conditions: External clock input to X1 and X2 not connected (float)									
T_{CKIN}	CLKIN Period	50	1000	40	1000	31.25	1000	ns	
T_{CLCK}	CLKIN Low Time	20		16		13		ns	1.5 V(2)
T_{CHCK}	CLKIN High Time	20		16		13		ns	1.5 V(2)
T_{CKHL}	CLKIN Fall Time		5		5		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5		5		5	ns	1.0 to 3.5V
80C188 CLKOUT TIMING									
T_{CICO}	CLKIN to CLKOUT Skew		25		21		17	ns	
T_{CLCL}	CLKOUT Period	100	2000	80	2000	62.5	2000	ns	
T_{CLCH}	CLKOUT Low Time	0.5 T_{CLCL} -8		0.5 T_{CLCL} -7		0.5 T_{CLCL} -7		ns	C_L=100pF(2)
		0.5 T_{CLCL} -6		0.5 T_{CLCL} -5		0.5 T_{CLCL} -5		ns	C_L=50pF(3)
T_{CHCL}	CLKOUT High Time	0.5 T_{CLCL} -8		0.5 T_{CLCL} -7		0.5 T_{CLCL} -7		ns	C_L=100pF(4)
		0.5 T_{CLCL} -6		0.5 T_{CLCL} -5		0.5 T_{CLCL} -5		ns	C_L=50pF(3)
T_{CH1CH2}	CLKOUT Rise Time		10		10		10	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		10		10		10	ns	3.5 to 1.0V

NOTES:
1. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}
2. Tested under worst case conditions: V_{CC} = 5.5V (5.25V @ 16 MHz). T_A = 70°C.
3. Not Tested.
4. Tested under worst case conditions: V_{CC} = 4.5V (4.75V @ 16 MHz). T_A = 0°C.

CLOCK WAVEFORMS



270432-40

A. C. CHARACTERISTICS

READY, PERIPHERAL, AND QUEUE STATUS TIMINGS

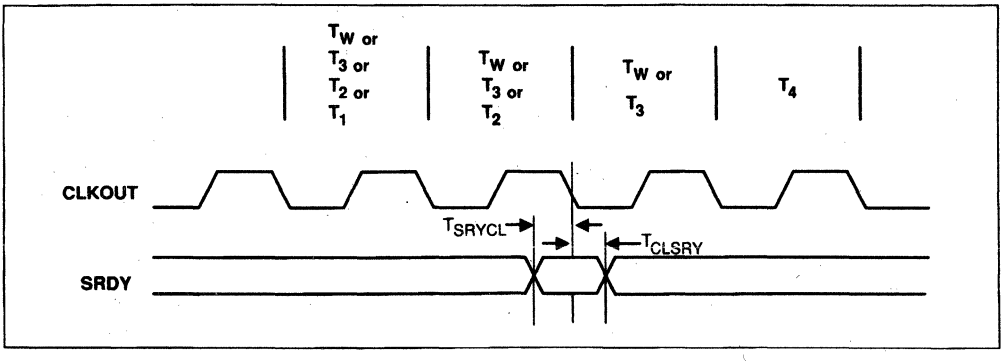
$T_A = 0^o$ C to $+70^o$ C, V_{CC} = 5V± 10% except V_{CC} = 5V± 5% at f > 12.5 MHz

All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50-200 pF (10 MHz) and C_L = 50-100 pF (12.5-16 MHz).
For A.C. tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	80C188		80C188-12		80C188-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C188 READY AND PERIPHERAL TIMING REQUIREMENTS									
T_{SRYCL}	Synchronous Ready(SRDY) Transition Setup Time (1)	15		15		15		ns	
T_{CLSRY}	SRDY Transition Hold Time (1)	15		15		15		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time (2)	15		15		15		ns	
T_{CLARX}	ARDY Active Hold Time (1)	15		15		15		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	15		15		15		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time (1)	25		25		25		ns	
T_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time (2)	15		15		15		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time(2)	15		15		15		ns	
80C188 PERIPHERAL AND QUEUE STATUS TIMING RESPONSES									
T_{CLTMV}	Timer Output Delay		40		33		27	ns	
T_{CHQSV}	Queue Status Delay		37		32		30	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

SYNCHRONOUS READY (SRDY) WAVEFORMS



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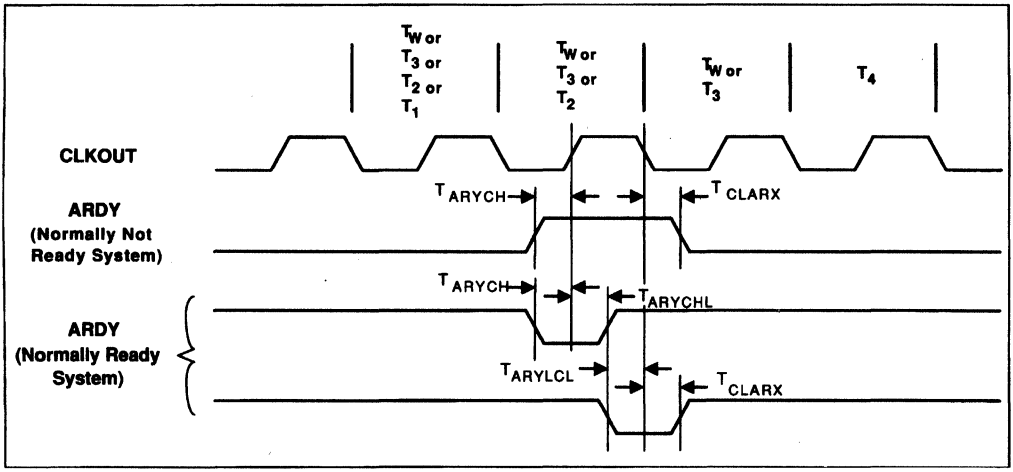
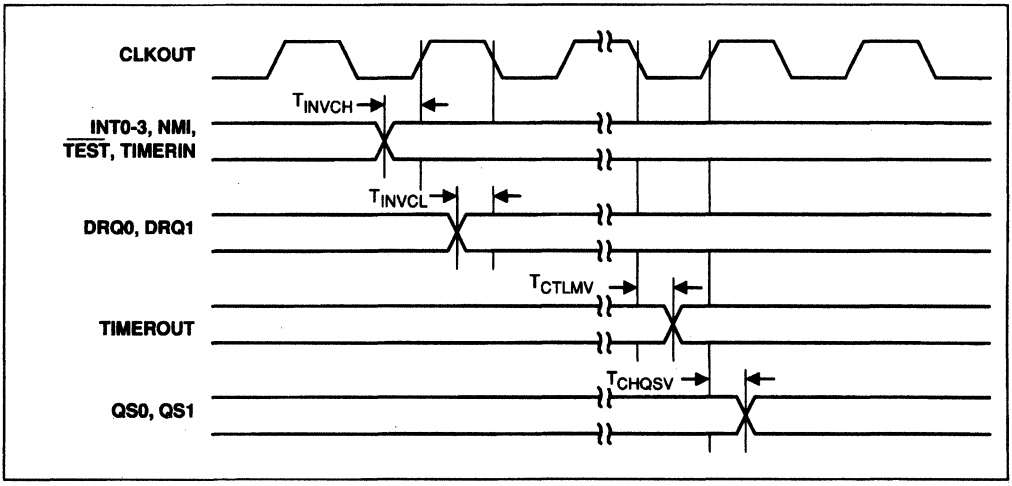
A. C. CHARACTERISTICS

ASYNCHRONOUS READY (ARDY) WAVEFORMS



PERIPHERAL AND QUEUE STATUS WAVEFORMS



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A. C. CHARACTERISTICS

RESET AND HOLD/HLDA TIMINGS

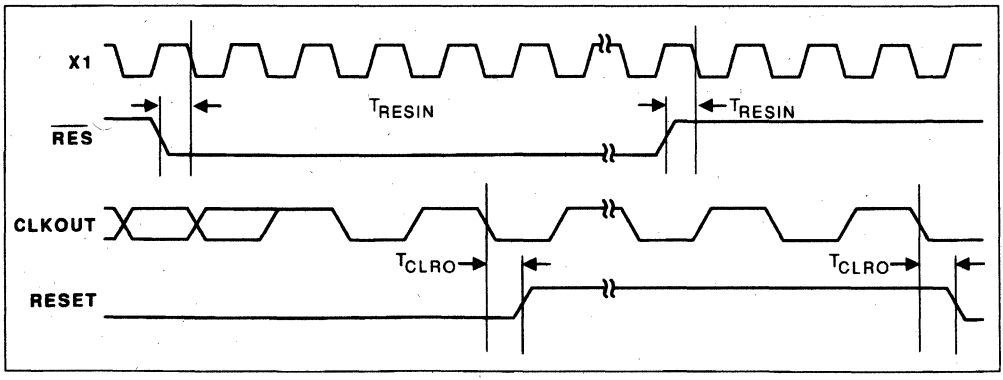
$T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5V \pm 10\%$ except $V_{CC} = 5V \pm 5\%$ at $f > 12.5$ MHz

All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50\text{-}200$ pF (10 MHz) and $C_L = 50\text{-}100$ pF (12.5-16 MHz).
For A.C. tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	80C188		80C188-12		80C188-16		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
80C188 RESET AND HOLD/HLDA TIMING REQUIREMENTS									
T_{RESIN}	$\overline{RES}$ Setup	15		15		15		ns	
T_{HVCL}	HOLD Setup (1)	15		15		15		ns	
80C188 GENERAL TIMING RESPONSES (Listed More Than Once)									
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	T_{CLAX}	20	ns	
T_{CLAV}	Address Valid Delay	5	44	5	36	5	33	ns	
80C188 RESET AND HOLD/HLDA TIMING RESPONSES									
T_{CLRO}	Reset Delay		40		33		27	ns	
T_{CLHAV}	HLDA Valid Delay	3	40	3	33	3	25	ns	
T_{CHCZ}	Command Lines Float Delay		40		33		28	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		44		36		32	ns	

NOTE:
1. To guarantee recognition at next clock.

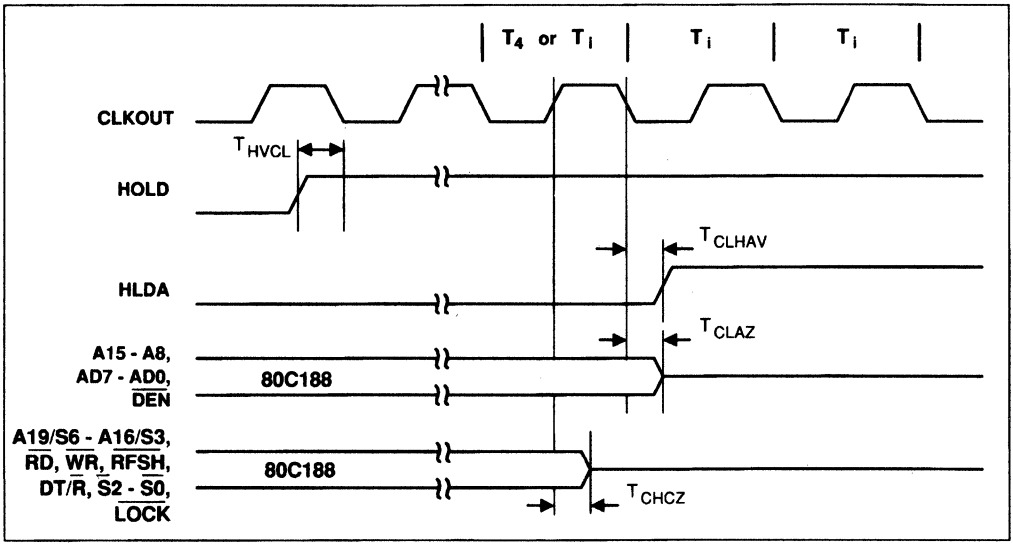
RESET WAVEFORMS



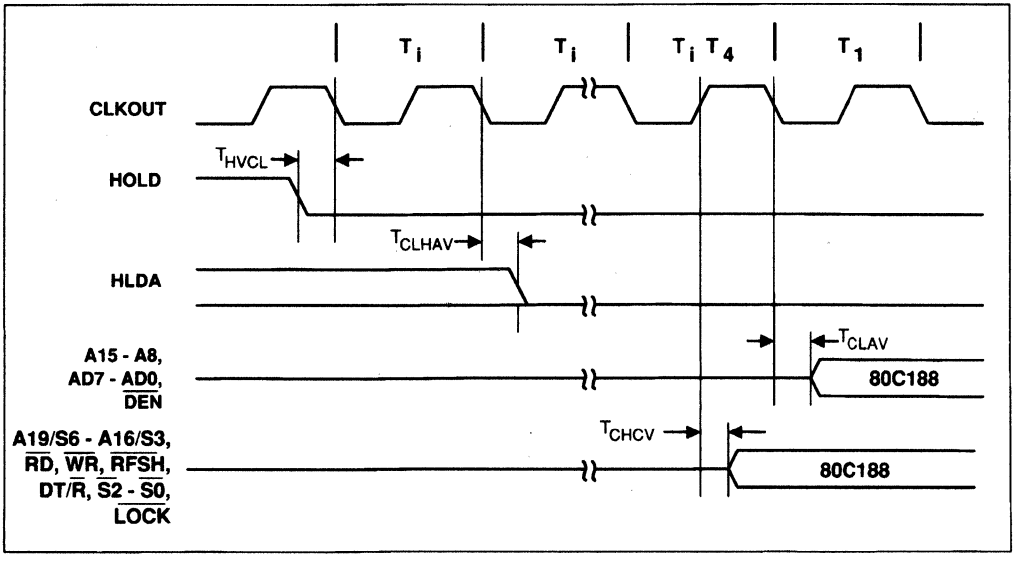
270432-43

A. C. CHARACTERISTICS

HOLD/HLDA WAVEFORMS (Entering Hold)



HOLD/HLDA WAVEFORMS (Leaving Hold)



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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has from 5 to 7 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address

ARY: Asynchronous Ready Input

C: Clock Output

CK: Clock Input

CS: Chip Select

CT: Control (DT/$\overline{R}$, $\overline{DEN}$, . . .)

D: Data Input

DE: $\overline{DEN}$

H: Logic Level High

IN: Input (DRQ0, TIM0, . . .)

L: Logic Level Low or ALE

O: Output

QS: Queue Status (QS1, QS2)

R: $\overline{RD}$ Signal, RESET Signal

S: Status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$)

SRY: Synchronous Ready Input

V: Valid

W: WR Signal

X: No Longer a Valid Logic Level

Z: Float

Examples:

T_{CLAV}— Time from Clock Low to Address Valid

T_{CHLH}— Time from Clock High to ALE High

T_{CLCSV}— Time from Clock Low to Chip Select Valid

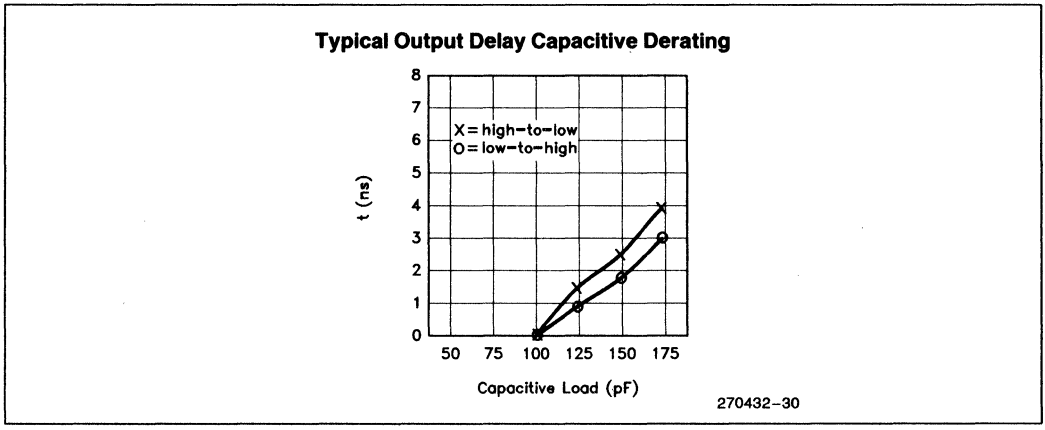

Figure 47. Capacitive Derating Curve

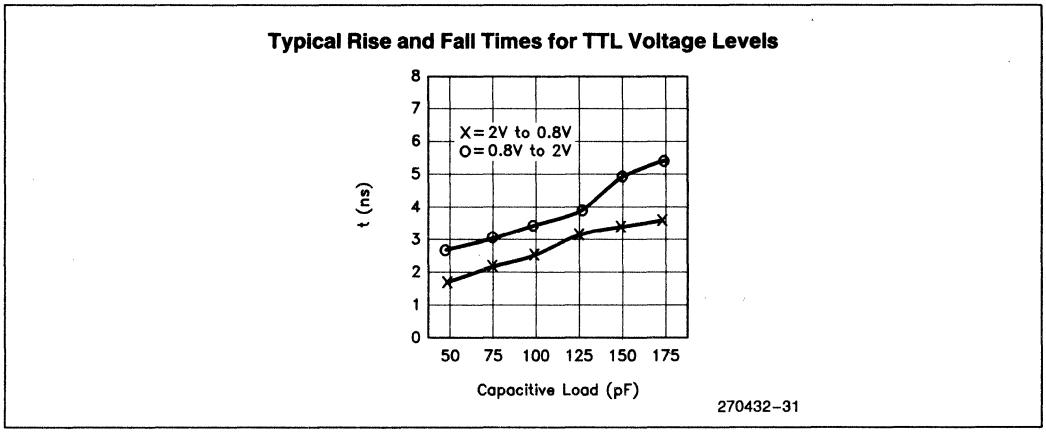

Figure 48. TTL Level Slew Rates for Output Buffers

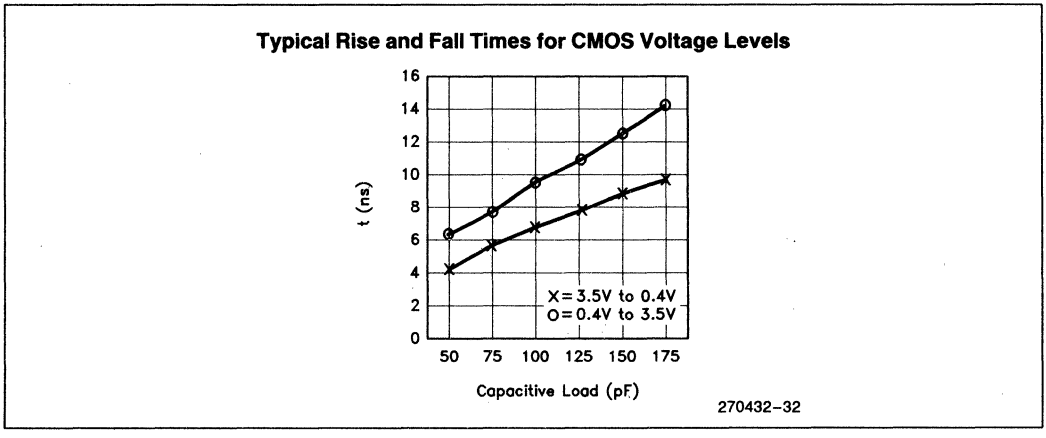

Figure 49. CMOS Level Slew Rates for Output Buffers

80C188 EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the 80C188 microprocessor. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The 80C188 EXPRESS program includes an extended temperature range. With the commercial standard temperature range operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

Package types and EXPRESS versions are identified by a one or two-letter prefix to the part number. The prefixes are listed in Table 16. All AC and DC specifications not mentioned in this section are the same for both commercial and EXPRESS parts.

Table 16. Prefix Identification

Prefix	Package Type	Temperature Range
A	PGA	commercial
N	PLCC	commercial
R	LCC	commercial
TA	PGA	extended
TN	PLCC	extended
TR	LCC	extended

NOTE:
Extended temperature versions of the 80C188 are not available at 16 MHz.

80C188 EXECUTION TIMINGS

A determination of 80C188 program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

The 80C188 8-bit BIU is noticeably limited in its performance relative to the execution unit. A sufficient number of prefetched bytes may not reside in the prefetch queue much of the time. Therefore, actual program execution time will be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1000100w	mod reg r/m			2/12*	
Register/memory to register	1000101w	mod reg r/m			2/9*	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12/13	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3/4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8*	
Accumulator to memory	1010001w	addr-low	addr-high		9*	
Register/memory to segment register	10001110	mod 0 reg r/m			2/13	
Segment register to register/memory	10001100	mod 0 reg r/m			2/15	
PUSH = Push:						
Memory	11111111	mod 1 1 0 r/m			20	
Register	01010 reg				14	
Segment register	000reg110				13	
Immediate	011010s0	data	data if s=0		14	
PUSHA = Push All	01100000				68	
POP = Pop:						
Memory	10001111	mod 0 0 0 r/m			24	
Register	01011 reg				14	
Segment register	000reg111	(reg≠01)			12	
POPA = Pop All	01100001				83	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17*	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10*	
Variable port	1110110w				8*	
OUT = Output to:						
Fixed port	1110011w	port			9*	
Variable port	1110111w				7*	
XLAT = Translate byte to AL	11010111				15	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		26	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		26	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				13	
POPF = Pop flags	10011101				12	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

***NOTE:**
Clock cycles show[illegible]or byte transfer. For word operations, add 4 clock cycles for all memory transfers.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16*	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16*	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15*	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16*	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16*	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15*	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10*	
Register with register/memory	0011100w	mod reg r/m			3/10*	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10*	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10*	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
ARITHMETIC (Continued)			
MUL = Multiply (unsigned):	1111011w | mod 100 r/m		
Register-Byte		26–28	
Register-Word		35–37	
Memory-Byte		32–34	
Memory-Word		41–43*	
IMUL = Integer multiply (signed):	1111011w | mod101 r/m		
Register-Byte		25–28	
Register-Word		34–37	
Memory-Byte		31–34	
Memory-Word		40–43*	
IMUL = Integer Immediate multiply (signed)	011010s1 | mod reg r/m | data | data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w | mod110 r/m		
Register-Byte		29	
Register-Word		38	
Memory-Byte		35	
Memory-Word		44*	
IDIV = Integer divide (signed):	1111011w | mod111 r/m		
Register-Byte		44–52	
Register-Word		53–61	
Memory-Byte		50–58	
Memory-Word		59–67*	
AAM = ASCII adjust for multiply	11010100 | 00001010	19	
AAD = ASCII adjust for divide	11010101 | 00001010	15	
CBW = Convert byte to word	10011000	2	
CWD = Convert word to double word	10011001	4	
LOGIC			
Shift/Rotate Instructions:			
Register/Memory by 1	1101000w | mod TTT r/m	2/15	
Register/Memory by CL	1101001w | mod TTT r/m	5+n/17+n	
Register/Memory by Count	1100000w | mod TTT r/m | count	5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR		
AND = **And:**			
Reg/memory and register to either	001000dw | mod reg r/m	3/10*	
Immediate to register/memory	1000000w | mod100 r/m | data | data if w=1	4/16*	
Immediate to accumulator	0010010w | data | data if w=1	3/4	8/16-bit

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
TEST = And function to flags, no result:						
Register/memory and register	1000010w	mod reg r/m			3/10*	
Immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	4/10*	
Immediate data and accumulator	1010100w	data	data if w=1		3/4	8/16-bit
OR = Or:						
Reg/memory and register to either	000010dw	mod reg r/m			3/10*	
Immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0000110w	data	data if w=1		3/4	8/16-bit
XOR = Exclusive or:						
Reg/memory and register to either	001100dw	mod reg r/m			3/10*	
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0011010w	data	data if w=1		3/4	8/16-bit
NOT = Invert register/memory	1111011w	mod 010 r/m			3/10*	
STRING MANIPULATION						
MOVS = Move byte/word	1010010w				14*	
CMPS = Compare byte/word	1010011w				22*	
SCAS = Scan byte/word	1010111w				15*	
LODS = Load byte/wd to AL/AX	1010110w				12*	
STOS = Store byte/wd from AL/AX	1010101w				10*	
INS = Input byte/wd from DX port	0110110w				14	
OUTS = Output byte/wd to DX port	0110111w				14	
Repeated by count in CX (REP/ REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	11110010	1010010w			8+8n*	
CMPS = Compare string	1111001z	1010011w			5+22n*	
SCAS = Scan string	1111001z	1010111w			5+15n*	
LODS = Load string	11110010	1010110w			6+11n*	
STOS = Store string	11110010	1010101w			6+9n*	
INS = Input string	11110010	0110110w			8+8n*	
OUTS = Output string	11110010	0110111w			8+8n*	
CONTROL TRANSFER						
CALL = Call:						
Direct within segment	11101000	disp-low	disp-high		19	
Register/memory indirect within segment	11111111	mod 010 r/m			17/27	
Direct intersegment	10011010	segment offset			31	
		segment selector				
Indirect intersegment	11111111	mod 011 r/m	(mod ≠ 11)		54	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
JMP = Unconditional jump:						
Short/long	11101011	disp-low			14	
Direct within segment	11101001	disp-low	disp-high		14	
Register/memory indirect within segment	11111111	mod 100 r/m			11/21	
Direct intersegment	11101010	segment offset			14	
		segment selector				
Indirect intersegment	11111111	mod 101 r/m	(mod ≠ 11)		34	
RET = Return from CALL:						
Within segment	11000011				20	
Within seg adding immed to SP	11000010	data-low	data-high		22	
Intersegment	11001011				30	
Intersegment adding immediate to SP	11001010	data-low	data-high		33	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					19	
L = 1					29	
L > 1					26 + 20(n − 1)	
LEAVE = Leave Procedure	11001001				8	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
CONTROL TRANSFER (Continued)			
INT = **Interrupt:**			
Type specified	11001101 | type	47	
Type 3	11001100	45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110	48/4	
IRET = Interrupt return	11001111	28	
BOUND = Detect value out of range	01100010 | mod reg r/m	33–35	
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

REVISION HISTORY

The sections significantly revised since version -003 are:

Pin Description Table	Added note to $\overline{TEST}$ pin requiring proper RESET at power-up to configure pin as input. Renamed pin 44 to INT1/$\overline{SELECT}$ and pin 41 to INT3/$\overline{INTA1}$/IRQ to better describe their functions in Slave Mode.
Initialization and Processor Reset	Added reminder to drive $\overline{RES}$ pin LOW during power-up.
Read and Write Cycle Waveforms	Clarified applicability of T_{CLCSV} to latched A1 and A2 in footnotes.
Instruction Set Summary	Corrected clock count for ENTER instruction.
Slave Mode Operation	The three low order bits associated with vector generation and performing EOI are not alterable; however, the priority levels are programmable. This information is a clarification only.

The sections significantly revised since version -002 are:

Front Page	Deleted references to burn-in devices.
Local Bus Controller and Reset	Clarified effects of excessive loading on pins with internal pullup devices. Equivalent resistance no longer shown.
D.C. Characteristics	Renamed V_{CLI} to V_{IL1}. Renamed V_{CHI} to V_{IH3}. Changed V_{OH} (min) from 0.8 V_{CC} to V_{CC} − 0.5V. Changed I_{CC} (max) from 180 mA to 150 mA at 16 MHz, 150 mA to 120 mA at 12.5 MHz, and 120 mA to 100 mA at 10 MHz. Changed V_{CLO} (max) from 0.5V to 0.45V. Changed V_{CHO} (min) from 0.8 V_{CC} to V_{CC} − 0.5V. Clarified effect of excessive loading on pins with internal pullup devices.
Power Supply Current	Added equation and graph for maximum current.
A.C. Characteristics	Many timings changed (all listed in ns): T_{DVCL} (min) at 16 MHz from 10 to 15; T_{CLDX} (min) from 5 to 3; T_{CLAV} (max) at 10 MHz from 50 to 44; T_{CHCV} (max) from 45 to 44 at 10 MHz and from 37 to 36 at 12.5 MHz; T_{LHLL} (min) from T_{CLCL} − 30 to T_{CLCL} − 15; T_{LLAX} (min) at 10 MHz from T_{CHCL} − 20 to T_{CHCL} − 15; T_{CVCTV} (max) from 56 to 44 at 10 MHz, and from 47 to 37 at 12.5 MHz; T_{CVDEX} (max) from 56 to 44 at 10 MHz, 47 to 37 at 12.5 MHz, and from 35 to 31 at 16 MHz; T_{RHAV} (min) from T_{CLCL} − 40 at 10 MHz and T_{CLCL} − 20 at 12.5 MHz and 16 MHz to T_{CLCL} − 15 at all frequencies; T_{RLRH} (min) from 2 T_{CLCL} − 46 to 2 T_{CLCL} − 30 at 10 MHz, from 2 T_{CLCL} − 40 to 2 T_{CLCL} − 25 at 12.5 MHz, and T_{CLCL} − 30 to 2 T_{CLCL} − 25 at 16 MHz; T_{WLWH} (min) from 2 T_{CLCL} − 34 to 2 T_{CLCL} − 30 at 10 MHz, and 2 T_{CLCL} − 30 to 2 T_{CLCL} − 25 at 12.5 MHz, T_{AVLL} (min) from T_{CLCH} − 19 to T_{CLCH} − 18 at 10 MHz; T_{CLSH} (max) at 10 MHz from 50 to 46; T_{CLTMV} (max) from 48 to 40 at 10 MHz; 40 to 33 at 12.5 MHz, and 30 to 27 at 16 MHz; T_{CLRO} (max) from 48 to 40 at 10 MHz, 40 to 33 at 12.5 MHz, and 37 to 27 at 16 MHz; T_{CHQSV} (max) from 28 to 37 at 10 MHz, 28 to 32 at 12.5 MHz, and 25 to 30 at 16 MHz; T_{CHDX} (min) from 5 to 10; T_{CLLV} (max) at 10 MHz from 45 to 40 and at 12.5 MHz from 40 to 37; T_{CLCSV} (max) from 45 to 42 at 10 MHz; T_{CHCSX} (max) from 32 to 35 at 10 MHz, 28 to 30 at 12.5 MHz, and 23 to 25 at 16 MHz; and T_{CH1CH2} and T_{CL2CL1} (max) at 16 MHz from 8 to 10. Added new timings for T_{WHDEX}, T_{RHLH}, and T_{WHLH}. Established minimum timing for T_{CLCSV}.

Timing Waveforms	Section rearranged to show waveforms on same or facing page relative to corresponding tabular data. T_{CLSRY} drawn to same clock edge as T_{SRYCL}. Drawing changed to indicate one less clock between HOLD inactive and HLDA inactive.
Specification Level Markings	New section.

The sections significantly revised since version -001 are:

LCC Contact Diagram	Corrections made to upper address pins.
Pin Description Table	Various descriptions rewritten for clarity.
Interrupt Vector Table	Redrawn for clarity.
ESC Opcode Exception Description	Note added concerning ESC trap.
Oscillator Configurations	Deleted drive of X2 with inverted X1.
RESET Logic	Deleted paragraph concerning setup times for synchronization of multiple processors.
Local Bus Arbitration	Added description of HLDA when a refresh cycle is pending.
Local Bus Controller and Reset	Added description of pullup devices for appropriate pins.
DMA Controller	Added reminder to initialize transfer count registers and pointer registers.
Timers	Added reminder to initialize count registers.
DRAM Refresh Addresses	Refresh address counter described in figure.
D.C. Characteristics	V_{IH2} indicated for SRDY, ARDY. I_{CC} (max.) now indicated for all devices.
Power Supply Current	Typical I_{CC} indicated.
A.C. Characteristics	Input V_{IH} test condition at X1 added. T_{CLDOX}, T_{CVCTV}, T_{CVCTX}, T_{CLHAV} and T_{CLLV} minimums reduced from 5 ns to 3 ns. T_{CLCH} min. and T_{CHCL} min. relaxed by 2 ns. Added reminder that T_{SRYCL} and T_{CLSRY} must be met.
Explanation of the A.C. Symbols	New section.
Major Cycle Timing Waveforms	T_{DXDL} indicated in Read Cycle. T_{CLRO} indicated.
Rise/Fall Times and Capacitive Derating Curves	New Figures added.
Instruction Set Summary	ESC deleted.

SPECIFICATION LEVEL MARKINGS

Current 80C188 devices bear backside lot code information consisting of seven digits followed by letters. The second, third, and fourth digits comprise a manufacturing data code. This preliminary data sheet applies only to 80C188 devices with a date code corresponding to week 25 of 1989 (backside markings x925xxx XXX) or later.

80C188XL20, 16, 12, 10
16-BIT HIGH INTEGRATION EMBEDDED PROCESSOR

- Low Power, Full Static Version of the 80C188
- Operation Modes Include:
  - Enhanced Mode
    - DRAM Refresh Control Unit
    - Power-Save Mode
  - Compatible Mode
    - NMOS 80C188 Pin-for-Pin Replacement for Non-Numerics Applications
- Integrated Feature Set
  - Static, Modular CPU
  - Clock Generator
  - 2 Independent DMA Channels
  - Programmable Interrupt Controller
  - 3 Programmable 16-Bit Timers
  - Dynamic RAM Refresh Control Unit
  - Programmable Memory and Peripheral Chip Select Logic
  - Programmable Wait State Generator
  - Local Bus Controller
  - Power-Save Mode
  - System-Level Testing Support (High Impedance Test Mode)
- Speed Versions Available
  - 20 MHz (80C188XL20)
  - 16 MHz (80C188XL16)
  - 12.5 MHz (80C188XL12)
  - 10 MHz (80C188XL)
- Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O
- Completely Object Code Compatible with Existing 8086/8088 Software and Has 10 Additional Instructions over 8086/8088
- Complete System Development Support
  - All 8086 and 80C186 Software Development Tools Can Be Used for 80C188XL System Development
    - ASM 86 Assembler, PL/M-86, Pascal-86, Fortran-86 iC-86 and System Utilities
  - In-Circuit-Emulator (ICE™-186)
- Available in 68-Pin:
  - Plastic Leaded Chip Carrier (PLCC)
  - Ceramic Pin Grid Array (PGA)
  - Ceramic Leadless Chip Carrier (JEDEC A Package)
- Available in 80-Pin Quad Flat Pack (EIAJ)
- Available in EXPRESS Extended Temperature Range (−40°C to +85°C)

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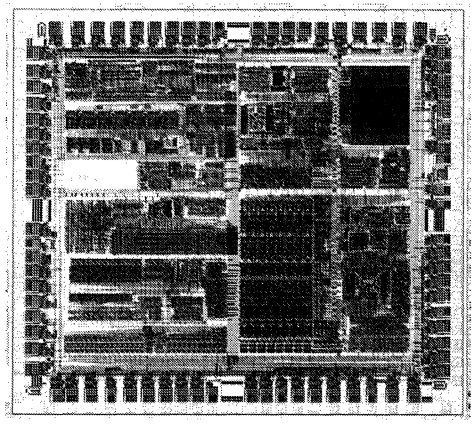
The Intel 80C188XL is a Modular Core re-implementation of the 80C188 Microprocessor. It offers higher speed and lower power consumption than the standard 80C188 but maintains 100% clock-for-clock functional compatibility. Packaging and pinout are also identical.



270975-48

June 1992
Order Number: 270975-002

80C188XL20, 16, 12, 10
16-BIT HIGH INTEGRATION EMBEDDED PROCESSOR

CONTENTS

CONTENTS

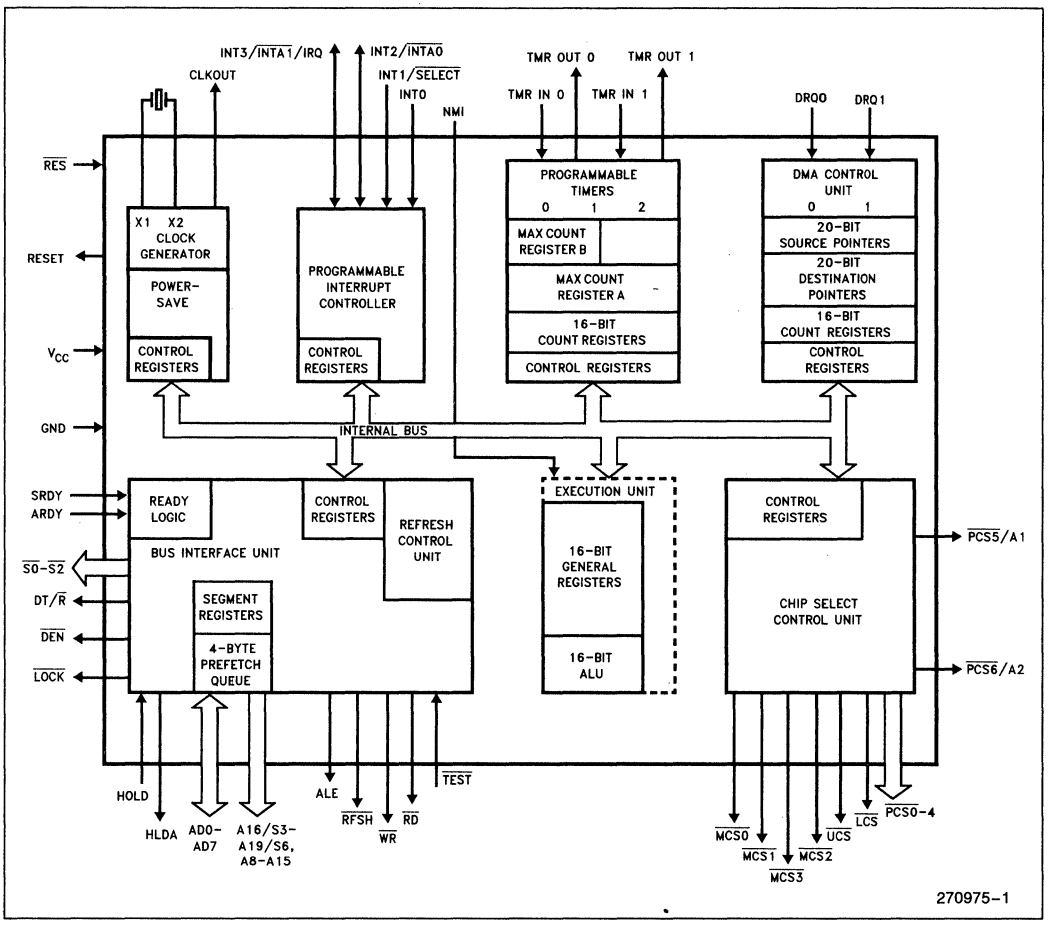
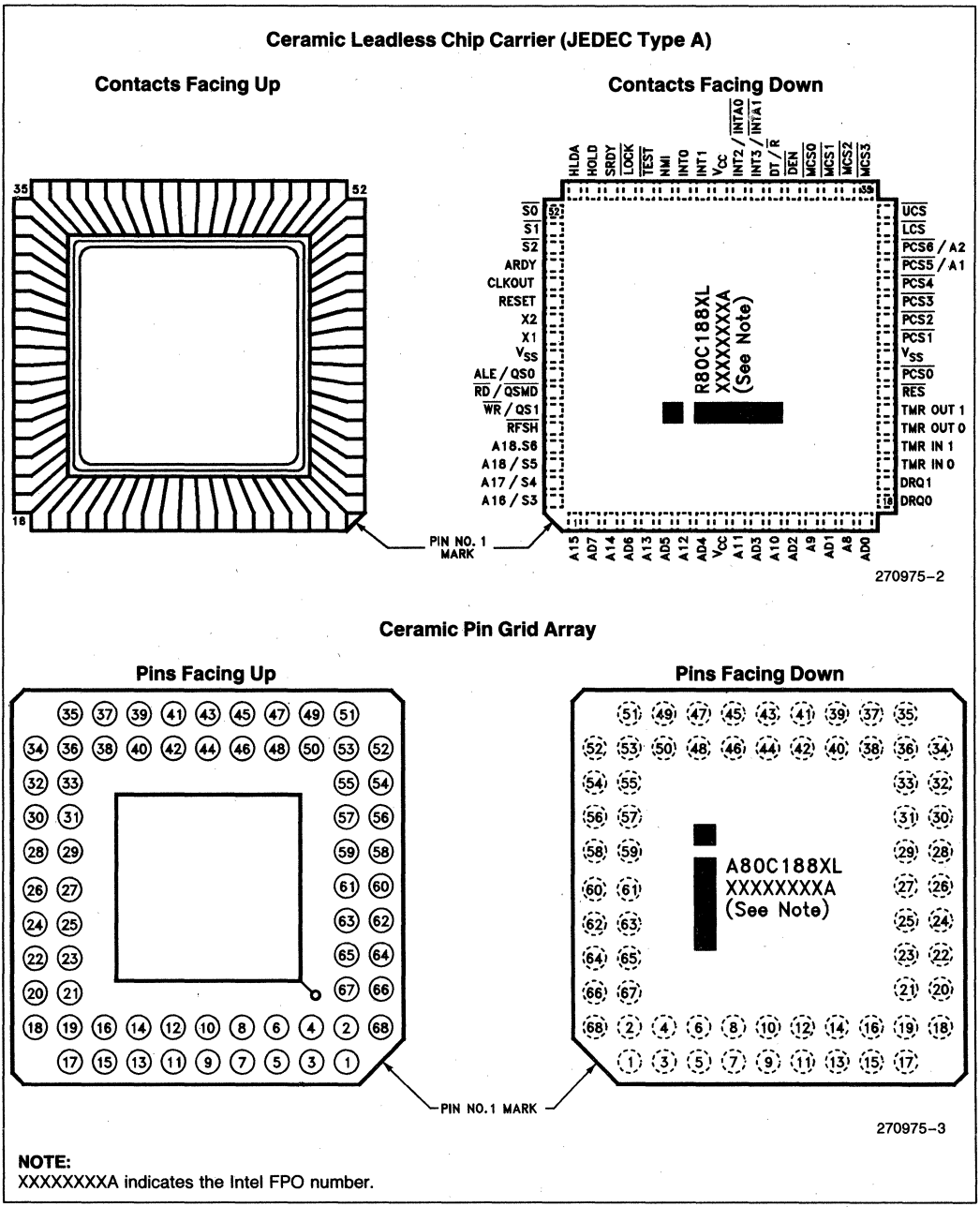


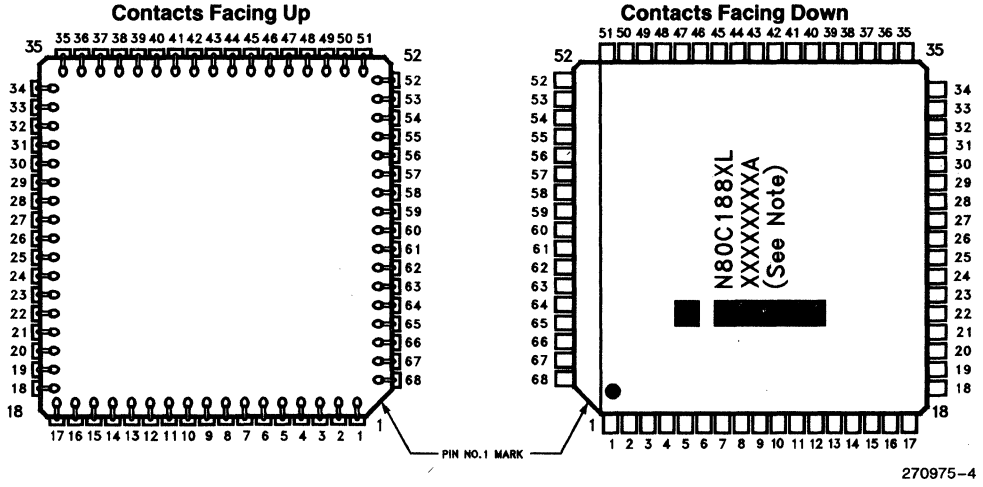
Figure 1. 80C188XL Block Diagram



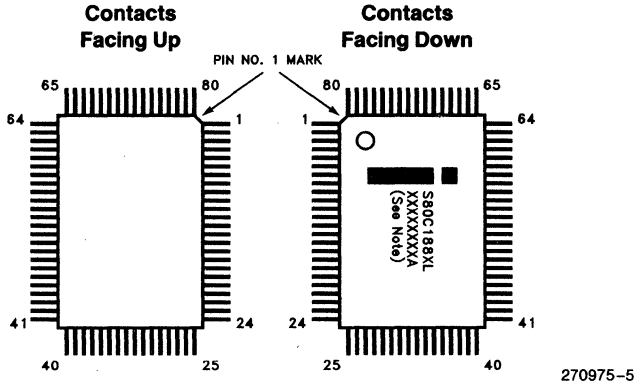
NOTE:
XXXXXXXXA indicates the Intel FPO number.

Figure 2. 80C188XL Pinout Diagrams

Plastic Leaded Chip Carrier



80-Pin Quad Flat Pack (EIAJ)



NOTE:
XXXXXXXXA indicates the Intel FPO number.

Figure 2. 80C188XL Pinout Diagrams (Continued)

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Table 1. 80C188XL Pin Description

Symbol	LCC PGA PLCC Pin No.	QFP Pin No.	Type	Name and Function
V_{CC}	9 43	33, 34 72, 73	I I	System Power: +5 volt power supply.
V_{SS}	26 60	12, 13 53	I I	System Ground.
RESET	57	18	O	RESET Output indicates that the 80C188XL CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal. Reset goes inactive 2 clockout periods after $\overline{RES}$ goes inactive. When tied to the $\overline{TEST}$ pin, RESET forces the 80C188XL into enhanced mode. RESET is not floated during bus hold.
X1 X2	59 58	16 17	I O	Crystal Inputs X1 and X2 provide external connections for a fundamental mode or third overtone parallel resonant crystal for the internal oscillator. X1 can connect to an external clock instead of a crystal. In this case, minimize the capacitance on X2. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	19	O	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT is active during reset and bus hold.
$\overline{RES}$	24	55	I	An active $\overline{RES}$ causes the 80C188XL to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80C188XL clock. The 80C188XL begins fetching instructions approximately 6½ clock cycles after $\overline{RES}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{RES}$ held LOW. $\overline{RES}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network.
$\overline{TEST}$	47	29	I/O	The $\overline{TEST}$ pin is sampled during and after reset to determine whether the 80C188XL is to enter Compatible or Enhanced Mode. Enhanced Mode requires $\overline{TEST}$ to be HIGH on the rising edge of $\overline{RES}$ and LOW four CLKOUT cycles later. Any other combination will place the 80C188XL in Compatible Mode. A weak internal pullup ensures a HIGH state when the pin is not driven. This pin is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when WAIT execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled every five clocks until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80C188XL is waiting for $\overline{TEST}$, interrupts will be serviced. During power-up, active $\overline{RES}$ is required to configure $\overline{TEST}$ as an input.
TMR IN 0 TMR IN 1	20 21	59 58	I I	Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized. Timer Inputs must be tied HIGH when not being used as clock or retrigger inputs.

Table 1. 80C188XL Pin Description (Continued)

Symbol	LCC PGA PLCC Pin No.	QFP Pin No.	Type	Name and Function
TMR OUT 0 TMR OUT 1	22 23	57 56	O O	Timer outputs are used to provide single pulse or continous waveform generation, depending upon the timer mode selected. These outputs are not floated during a bus hold.
DRQ0 DRQ1	18 19	61 60	I I	DMA Request is asserted HIGH by an external device when it is ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
NMI	46	30	I	The Non-Maskable Interrupt input causes a Type 2 interrupt. An NMI transition from LOW to HIGH is latched and synchronized internally, and initiates the interrupt at the next instruction boundary. NMI must be asserted for at least one CLKOUT period. The Non-Maskable Interrupt cannot be avoided by programming.
INT0 INT1/$\overline{\text{SELECT}}$ INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$/IRQ	45 44 42 41	31 32 35 36	I I I/O I/O	Maskable Interrupt Requests can be requested by activating one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When Slave Mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).
A19/S6 A18/S5 A17/S4 A16/S3	65 66 67 68	6 5 4 3	O O O O	Address Bus Outputs (16–19) and Bus Cycle Status (3–6) indicate the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W and T_4 status information is available on these lines as encoded below: During T_2, T_3, T_W and T_4, the S6 pin is LOW to indicate a CPU-initiated bus cycle or HIGH to indicate a DMA-initiated or refresh bus cycle. During the same T-states, S3, S4 and S5 are always LOW. These outputs are floated during a bus hold or reset.
A15 A14 A13 A12 A11 A10 A9 A8	1 3 5 7 10 12 14 16	1 79 77 75 71 69 67 65	O O O O O O O O	Address-Only Bus (15–8) contains valid addresses from T_1–T_4. The bus is active high. These outputs are floated during a bus hold or reset.
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	2 4 6 8 11 13 15 17	80 78 76 74 70 68 66 64	I/O I/O I/O I/O I/O I/O I/O I/O	Address/Data Bus (7–0) signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W and T_4) bus. The bus is active high. These pins are floated during a bus hold or reset.

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Table 1. 80C188XL Pin Description (Continued)

Symbol	LCC PGA PLCC Pin No.	QFP Pin No.	Type	Name and Function
$\overline{RFSH}$	64	7	O	In compatible mode, $\overline{RFSH}$ is HIGH. In enhanced mode, $\overline{RFSH}$ is asserted LOW to signify a refresh bus cycle. The $\overline{RFSH}$ output pin floats during bus hold or reset, regardless of operating mode.
ALE/QS0	61	10	O	Address Latch Enable/Queue Status 0 is provided by the 80C188XL to latch the address. ALE is active HIGH, with addresses guaranteed valid on the trailing edge.
$\overline{WR}$/QS1	63	8	O	Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. It is active LOW, and floats during bus hold or reset. When the 80C188XL is in Queue Status Mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.

QS1	QS0	Queue Operation
0	0	No queue operation
0	1	First opcode byte fetched from the queue
1	1	Subsequent byte fetched from the queue
1	0	Empty the queue

$\overline{RD}$/$\overline{QSMD}$	62	9	O/I	Read Strobe is an active LOW signal which indicates that the 80C188XL is performing a memory or I/O read cycle. It is guaranteed not to go LOW before the A/D bus is floated. An internal pull-up ensures that $\overline{RD}$/$\overline{QSMD}$ is HIGH during RESET. Following RESET the pin is sampled to determine whether the 80C188XL is to provide ALE, $\overline{RD}$ and $\overline{WR}$, or queue status information. To enable Queue Status Mode, $\overline{RD}$ must be connected to GND. $\overline{RD}$ will float during bus HOLD.
ARDY	55	20	I	Asynchronous Ready informs the 80C188XL that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUT and is active HIGH. The falling edge of ARDY must be synchronized to the 80C188XL clock. Connecting ARDY HIGH will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the SRDY pin.
SRDY	49	27	I	Synchronous Ready informs the 80C188XL that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active-HIGH input synchronized to CLKOUT. The use of SRDY allows a relaxed system timing over ARDY. This is accomplished by elimination of the one-half clock cycle required to internally synchronize the ARDY input signal. Connecting SRDY high will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the ARDY pin.

Table 1. 80C188XL Pin Description (Continued)

Symbol	LCC PGA PLCC Pin No.	QFP Pin No.	Type	Name and Function
$\overline{LOCK}$	48	28	O	$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus. $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction immediately following the LOCK prefix. It remains active until the completion of that instruction. No instruction prefetching will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ floats during bus hold or reset.
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	52 53 54	23 22 21	O O O	Bus cycle status $\overline{S0}$–$\overline{S2}$ are encoded to provide bus-transaction information: **80C188XL Bus Cycle Status Information** $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ — Bus Cycle Initiated 0 0 0 — Interrupt Acknowledge 0 0 1 — Read I/O 0 1 0 — Write I/O 0 1 1 — Halt 1 0 0 — Instruction Fetch 1 0 1 — Read Data from Memory 1 1 0 — Write Data to Memory 1 1 1 — Passive (no bus cycle) The status pins float during HOLD. $\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.
HOLD HLDA	50 51	26 25	I O	HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. The 80C188XL generates HLDA (HIGH) in response to a HOLD request. Simultaneous with the issuance of HLDA, the 80C188XL will float the local bus and control lines. After HOLD is detected as being LOW, the 80C188XL will lower HLDA. When the 80C188XL needs to run another bus cycle, it will again drive the local bus and control lines. In Enhanced Mode, HLDA will go low when a DRAM refresh cycle is pending in the 80C188XL and an external bus master has control of the bus. It will be up to the external master to relinquish the bus by lowering HOLD so that the 80C188XL may execute the refresh cycle.
$\overline{UCS}$	34	45	O/I	Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. $\overline{UCS}$ does not float during bus hold. The address range activating $\overline{UCS}$ is software programmable. $\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the 80C188XL will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{UCS}$ has a weak internal pullup that is active during RESET to ensure that the 80C188XL does not enter the ONCE Mode inadvertently.

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Table 1. 80C188XL Pin Description (Continued)

Symbol	LCC PGA PLCC Pin No.	QFP Pin No.	Type	Name and Function
$\overline{LCS}$	33	46	O/I	Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. $\overline{LCS}$ does not float during bus HOLD. The address range activating $\overline{LCS}$ is software programmable. $\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the 80C188XL will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{LCS}$ has a weak internal pullup that is active only during RESET to ensure that the 80C188XL does not enter ONCE Mode inadvertently.
$\overline{MCS0}$ $\overline{MCS1}$ $\overline{MCS2}$ $\overline{MCS3}$	38 37 36 35	39 40 41 42	O O O O	Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines do not float during bus HOLD. The address ranges activating $\overline{MCS0–3}$ are software programmable.
$\overline{PCS0}$ $\overline{PCS1}$ $\overline{PCS2}$ $\overline{PCS3}$ $\overline{PCS4}$	25 27 28 29 30	54 52 51 50 49	O O O O O	Peripheral Chip Select signals 0–4 are active LOW when a reference is made to the defined peripheral area (64K I/O space or 1 Mbyte memory space). These lines do not float during bus HOLD. The address ranges activating $\overline{PCS0–4}$ are software programmable.
$\overline{PCS5}$/A1	31	48	O	Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software-programmable. $\overline{PCS5}$/A1 does not float during bus HOLD. When programmed to provide latched A1, this pin will retain the previously latched value during HOLD.
$\overline{PCS6}$/A2	32	47	O	Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software-programmable. $\overline{PCS6}$/A2 does not float during bus HOLD. When programmed to provide latched A2, this pin will retain the previously latched value during HOLD.
DT/$\overline{R}$	40	37	O	Data Transmit/Receive controls the direction of data flow through an external data bus transceiver. When LOW, data is transferred to the 80C188XL. When HIGH the 80C188XL places write data on the data bus. DT/$\overline{R}$ floats during a bus hold or RESET.
$\overline{DEN}$	39	38	O	Data Enable is provided as a data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access. $\overline{DEN}$ is HIGH whenever DT/$\overline{R}$ changes state. During RESET, $\overline{DEN}$ is driven HIGH for one clock, then floated. $\overline{DEN}$ also floats during HOLD.
N.C.	—	2, 11,14, 15, 24, 43, 44, 62, 63	—	Not Connected. To maintain compatibility with future products, do not connect these pins.

INTRODUCTION

The following Functional Description describes the base architecture of the 80C188XL. The 80C188XL is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip. The 80C188XL is object code compatible with the 8086/8088 microprocessors and adds 10 new instruction types to the 8086/8088 instruction set.

The 80C188XL has two major modes of operation, Compatible and Enhanced. In Compatible Mode the 80C188XL is completely compatible with NMOS 80188, with the exception of 8087 support. The Enhanced mode adds two new features to the system design. These are Power-Save control and Dynamic RAM refresh.

80C188XL BASE ARCHITECTURE

80C188XL Clock Generator

The 80C188XL provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs and reset circuitry.

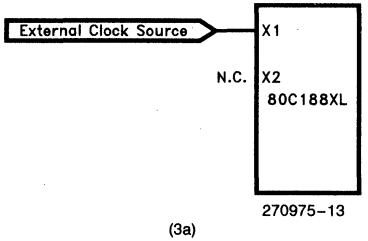
The 80C188XL oscillator circuit is designed to be used either with a parallel resonant fundamental or third-overtone mode crystal, depending upon the frequency range of the application. This is used as the time base for the 80C188XL.

The output of the oscillator is not directly available outside the 80C188XL. The recommended crystal configuration is shown in Figure 3b. When used in third-overtone mode, the tank circuit is recommended for stable operation. Alternately, the oscillator may be driven from an external source as shown in Figure 3a.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide by two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.

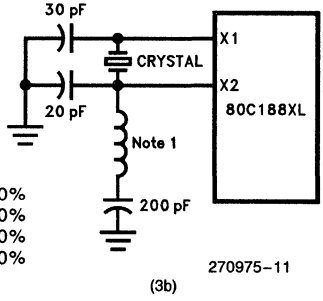
Intel recommends the following values for crystal selection parameters:

Temperature Range:	Application Specific
ESR (Equivalent Series Resistance):	60Ω max
C_0 (Shunt Capacitance of Crystal):	7.0 pF max
C_1 (Load Capacitance):	20 pF ±5 pF
Drive Level:	2 mW max



NOTE:

XTAL Frequency	L1 Value
20 MHz	12.0 μH ±20%
25 MHz	8.2 μH ±20%
32 MHz	4.7 μH ±20%
40 MHz	3.0 μH ±20%



LC Network is only required when using a third overtone crystal.

Figure 3. 80C188XL Oscillator Configurations (see text)

Bus Interface Unit

The 80C188XL provides a bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides outputs that can be used to enable external buffers and to direct the flow of data on and off the local bus.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information add data (for write operations) information. It is also responsible for reading data from the lcoal bus during a read operation. Synchronous and asynchronous ready input pins are provided to extend a bus cycle beyond the minimum four states (clocks).

The 80C188XL bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus.

During RESET, the local bus controller will perform the following action:

- Drive $\overline{DEN}$, $\overline{RD}$ and $\overline{WR}$ HIGH for one clock cycle, then float them.
- Drive $\overline{S0}$–$\overline{S2}$ to the inactive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Float AD0–AD7, A8–A19, S7/$\overline{RFSH}$, DT/$\overline{R}$.
- Drive ALE LOW.
- Drive HLDA LOW.

$\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$ and $\overline{TEST}$ pins have internal pullup devices which are active while $\overline{RES}$ is applied. Excessive loading or grounding certain of these pins causes the 80C188XL to enter an alternative mode of operation:

- $\overline{RD}$/$\overline{QSMD}$ LOW results in Queue Status Mode.
- $\overline{UCS}$ and $\overline{LCS}$ LOW results in ONCE Mode.
- $\overline{TEST}$ LOW (and HIGH later) results in Enhanced Mode.

80C188XL PERIPHERAL ARCHITECTURE

All the 80C188XL integrated peripherals are controlled by 16-bit registers contained within an internal 256-byte control block. The control block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles. An offset map of the 256-byte control register block is shown in Figure 3.

Chip-Select/Ready Generation Logic

The 80C188XL contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

The 80C188XL provides 6 memory chip select outputs for 3 address areas; upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

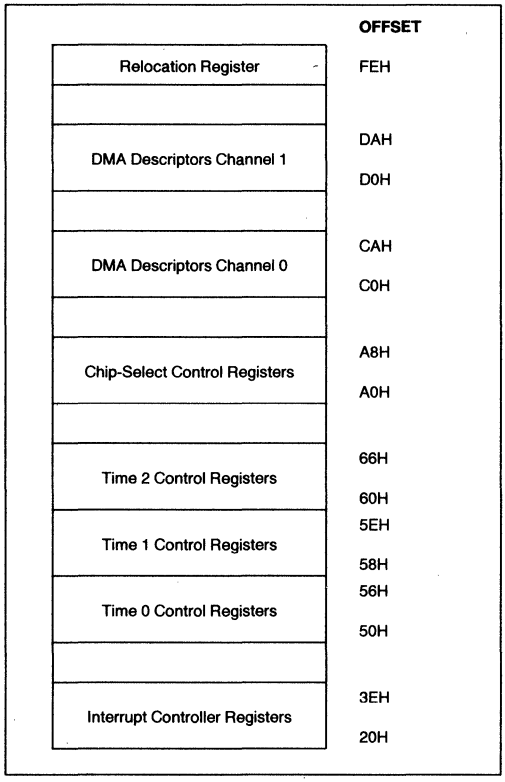


Figure 4. Internal Register Map

The 80C188XL provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the 80C188XL begins executing at memory location FFFF0H.

The 80C188XL provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The 80C188XL provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located within the 80C188XL 1 Mbyte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The 80C188XL can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address may be located in either memory or I/O space.

The 80C188XL can generate a READY signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the 80C188XL may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

Upon RESET, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to insert 3 wait states in conjunction with external READY (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers.

DMA Unit

The 80C188XL DMA controller provides two independent DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer. Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data.

Timer/Counter Unit

The 80C188XL provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

Interrupt Control Unit

The 80C188XL can receive interrupts from a number of sources, both internal and external. The 80C188XL has 5 external and 2 internal interrupt sources (Timer/Counters and DMA). The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Enhanced Mode Operation

In Compatible Mode the 80C188XL operates with all the features of the NMOS 80188, with the exception of 8087 support (i.e. no numeric coprocessing is possible). Queue-Status information is still available for design purposes other than 8087 support.

All the Enhanced Mode features are completely masked when in Compatible Mode. A write to any of the Enhanced Mode registers will have no effect, while a read will not return any valid data.

In Enhanced Mode, the 80C188XL will operate with Power-Save and DRAM refresh, in addition to all the Compatible Mode features.

Enhanced mode can be entered by tying the RESET output signal from the 80C188XL to the $\overline{\text{TEST}}$ input.

Queue-Status Mode

The queue-status mode is entered by strapping the $\overline{\text{RD}}$ pin low. $\overline{\text{RD}}$ is sampled at RESET and if LOW, the 80C188XL will reconfigure the ALE and $\overline{\text{WR}}$ pins to be QS0 and QS1 respectively. This mode is available on the 80C188XL in both Compatible and Enhanced Modes.

DRAM Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates DRAM refresh bus cycles. The RCU operates only in Enhanced Mode. After a programmable period of time, the RCU generates a memory read request to the BIU. If the address generated during a refresh bus cycle is within the range of a properly programmed chip select, that chip select will be activated when the BIU executes the refresh bus cycle.

Power-Save Control

The 80C188XL, when in Enhanced Mode, can enter a power saving state by internally dividing the processor clock frequency by a programmable factor. This divided frequency is also available at the CLKOUT pin.

All internal logic, including the Refresh Control Unit and the timers, have their clocks slowed down by the division factor. To maintain a real time count or a fixed DRAM refresh rate, these peripherals must be re-programmed when entering and leaving the power-save mode.

ONCE™ Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C188XL has a test mode available which allows all pins to be placed in a high-impedance state. ONCE stands for "ON Circuit Emulation". When placed in this mode, the 80C188XL will put all pins in the high-impedance state until RESET.

The ONCE Mode is selected by tying the $\overline{\text{UCS}}$ and the $\overline{\text{LCS}}$ LOW during RESET. These pins are sampled on the low-to-high transition of the $\overline{\text{RES}}$ pin. The $\overline{\text{UCS}}$ and the $\overline{\text{LCS}}$ pins have weak internal pull-up resistors similar to the $\overline{\text{RD}}$ and $\overline{\text{TEST}}$ pins to guarantee ONCE Mode is not entered inadvertently during normal operation. $\overline{\text{LCS}}$ and $\overline{\text{UCS}}$ must be held low at least one clock after $\overline{\text{RES}}$ goes high to guarantee entrance into ONCE Mode.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias .....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with
Respect to Ground .....−1.0V to +7.0V
Package Power Dissipation 1W
Not to exceed the maximum allowable die temperature based on thermal resistance of the package.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTICE: The specifications are subject to change without notice.

DC CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except X1)	−0.5	0.2 V_{CC} − 0.3	V	
V_{IL1}	Clock Input Low Voltage (X1)	−0.5	0.6	V	
V_{IH}	Input High Voltage (All except X1 and $\overline{RES}$)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC} + 0.5	V	
V_{IH2}	Clock Input High Voltage (X1)	3.9	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA (S0, 1, 2) I_{OL} = 2.0 mA (others)
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −2.4 mA @ 2.4V (4)
		V_{CC} − 0.5	V_{CC}	V	I_{OH} = −200 µA @ V_{CC} −0.5(4)
I_{CC}	Power Supply Current		100	mA	@ 20 MHz, 0°C V_{CC} = 5.5V(3)
			80	mA	@16 MHz, 0°C V_{CC} = 5.5V(3)
			65	mA	@ 12.5 MHz, 0°C V_{CC} = 5.5V (3)
			50	mA	@ 10 MHz, 0°C V_{CC} = 5.5V (3)
			100	µA	@ DC 0°C V_{CC} = 5.5V
I_{LI}	Input Leakage Current		±10	µA	@ 0.5 MHz, 0.45V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	µA	@ 0.5 MHz, 0.45V ≤ V_{OUT} ≤ V_{CC}(1)
V_{CLO}	Clock Output Low		0.45	V	I_{CLO} = 4.0 mA

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DC CHARACTERISTICS (Continued) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{CHO}	Clock Output High	$V_{CC} - 0.5$		V	$I_{CHO} = -500\ \mu A$
C_{IN}	Input Capacitance		10	pF	@ 1 MHz(2)
C_{IO}	Output or I/O Capacitance		20	pF	@ 1 MHz(2)

NOTES:
1. Pins being floated during HOLD or by invoking the ONCE Mode.
2. Characterization conditions are a) Frequency = 1 MHz; b) Unmeasured pins at GND; c) V_{IN} at + 5.0V or 0.45V. This parameter is not tested.
3. Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.
4. $\overline{RD}/QSMD$, $\overline{UCS}$, $\overline{LCS}$ and $\overline{TEST}$ pins have internal pullup devices. Loading some of these pins above $I_{OH} = -200\ \mu A$ can cause the 80C186 to go into alternative modes of operation. See the section on Local Bus Controller and Reset for details.

POWER SUPPLY CURRENT

Current is linearly proportional to clock frequency and is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.

Maximum current is given by $I_{CC} = 5\ mA \times$ freq. (MHz) + I_{QL}.

I_{QL} is the quiescent leakage current when the clock is static. I_{QL} is typically less than 100 μA.

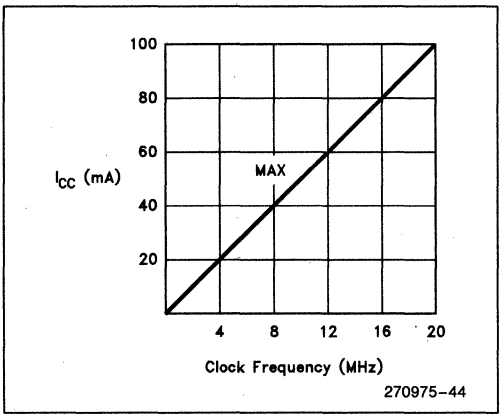

Figure 4. I_{CC} vs Frequency

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (READ CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL		80C188XL12			
		Min	Max	Min	Max		
80C188XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
80C188XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	40	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 18		T_{CLCH} − 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 15		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	ns	
T_{CLCSV}	Chip-Select Active Delay	3	42	3	33	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	35	3	30	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	44	3	37	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay	3	44	3	37	ns	
T_{CHCTV}	Control Active Delay 2	3	44	3	37	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	ns	
80C188XL TIMING RESPONSES (Read Cycle)							
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	3	44	3	37	ns	
T_{RLRH}	$\overline{RD}$ Pulse Width	$2T_{CLCL}$ − 30		$2T_{CLCL}$ − 25		ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	3	44	3	37	ns	
T_{RHLH}	$\overline{RD}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	T_{CLCL} − 15		T_{CLCL} − 15		ns	Equal Loading

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AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (READ CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50–200 PF (10 MHz) and C_L = 50–100 pF (12.5–20 MHz).
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL16		80C188XL20			
		Min	Max	Min	Max		
80C188XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		10		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
80C188XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	31	3	25	ns	
T_{CLSH}	Status Inactive Delay	3	30	3	25	ns	
T_{CLAV}	Address Valid Delay	3	33	3	27	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	33	3	27	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 15		T_{CLCH} − 10		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 10		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	ns	
T_{CLCSV}	Chip-Select Active Delay	3	30	3	25	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	t_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	25	3	20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	31	3	25	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay	3	31	3	22	ns	
T_{CHCTV}	Control Active Delay 2	3	31	3	22	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	35	3	22	ns	
80C188XL TIMING RESPONSES (Read Cycle)							
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	3	31	3	27	ns	
T_{RLRH}	$\overline{RD}$ Pulse Width	$2T_{CLCL}$ − 25		$2T_{CLCL}$ − 20		ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	3	31	3	27	ns	
T_{RHLH}	$\overline{RD}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	T_{CLCL} − 15		T_{CLCL} − 15		ns	Equal Loading

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (WRITE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL		80C188XL12			
		Min	Max	Min	Max		
80C188XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	40	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 18		T_{CLCH} − 15		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 15		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLDOX}	Data Hold Time	3		3		ns	
T_{CVCTV}	Control Active Delay 1	3	44	3	37	ns	
T_{CVCTX}	Control Inactive Delay	3	44	3	37	ns	
T_{CLCSV}	Chip-Select Active Delay	3	42	3	33	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	35	3	30	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	ns	
80C188XL TIMING RESPONSES (Write Cycle)							
T_{WLWH}	$\overline{WR}$ Pulse Width	$2T_{CLCL}$ − 30		$2T_{CLCL}$ − 25		ns	
T_{WHLH}	$\overline{WR}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{WHDX}	Data Hold after $\overline{WR}$	T_{CLCL} − 34		T_{CLCL} − 20		ns	Equal Loading
T_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading

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AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (WRITE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL16		80C188XL20			
		Min	Max	Min	Max		
80C188XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	31	3	25	ns	
T_{CLSH}	Status Inactive Delay	3	30	3	25	ns	
T_{CLAV}	Address Valid Delay	3	33	3	27	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	33	3	27	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 15		T_{CLCH} − 10		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 10		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLDOX}	Data Hold Time	3		3		ns	
T_{CVCTV}	Control Active Delay 1	3	31	3	25	ns	
T_{CVCTX}	Control Inactive Delay	3	31	3	25	ns	
T_{CLCSV}	Chip-Select Active Delay	3	30	3	25	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	25	3	20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	35	3	22	ns	
80C188XL TIMING RESPONSES (Write Cycle)							
T_{WLWH}	$\overline{WR}$ Pulse Width	$2T_{CLCL}$ − 25		$2T_{CLCL}$ − 20		ns	
T_{WHLH}	$\overline{WR}$ Inactive to ALE High	T_{CLCH} − 14		T_{CLCH} − 14		ns	Equal Loading
T_{WHDX}	Data Hold after $\overline{WR}$	T_{CLCL} − 20		T_{CLCL} − 15		ns	Equal Loading
T_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	T_{CLCH} − 10		T_{CLCH} − 10		ns	Equal Loading

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (INTERRUPT ACKNOWLEDGE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL		80C188XL12			
		Min	Max	Min	Max		
80C188XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
80C188XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	40	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 18		T_{CLCH} − 15		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 15		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	ns	
T_{CVCTV}	Control Active Delay 1	3	44	3	37	ns	
T_{CVCTX}	Control Inactive Delay	3	44	3	37	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	44	3	37	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycles)	3	44	3	37	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	ns	

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AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (INTERRUPT ACKNOWLEDGE CYCLE)

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL16		80C188XL20			
		Min	Max	Min	Max		
80C188XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		10		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
80C188XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	31	3	25	ns	
T_{CLSH}	Status Inactive Delay	3	30	3	25	ns	
T_{CLAV}	Address Valid Delay	3	33	3	27	ns	
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	33	3	27	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} − 15		T_{CLCH} − 10		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	T_{CHCL} − 15		T_{CHCL} − 10		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	ns	
T_{CVCTV}	Control Active Delay 1	3	31	3	25	ns	
T_{CVCTX}	Control Inactive Delay	3	31	3	25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	31	3	22	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycles)	3	31	3	22	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	35	3	22	ns	

AC CHARACTERISTICS

SOFTWARE HALT CYCLE TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL		80C188XL12			
		Min	Max	Min	Max		
80C188XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low		0		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	44	3	37	ns	

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL16		80C188XL20			
		Min	Max	Min	Max		
80C188XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	31	3	25	ns	
T_{CLSH}	Status Inactive Delay	3	30	3	25	ns	
T_{CLAV}	Address Valid Delay	3	33	3	27	ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} − 15		T_{CLCL} − 15		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low		0		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	31	3	22	ns	

AC CHARACTERISTICS

CLOCK TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL		80C188XL12			
		Min	Max	Min	Max		
80C188XL CLKIN REQUIREMENTS(1)							
T_{CKIN}	CLKIN Period	50	∞	40	∞	ns	
T_{CLCK}	CLKIN Low Time	20	∞	16	∞	ns	1.5V(2)
T_{CHCK}	CLKIN High Time	20	∞	16	∞	ns	1.5V(2)
T_{CKHL}	CLKIN Fall Time		5		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5		5	ns	1.0 to 3.5V
80C188XL CLKOUT TIMING							
T_{CICO}	CLKIN to CLKOUT Skew		25		21	ns	
T_{CLCL}	CLKOUT Period	100	∞	80	∞	ns	
T_{CLCH}	CLKOUT Low Time	0.5 T_{CLCL} − 6		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(3)
T_{CHCL}	CLKOUT High Time	0.5 T_{CLCL} − 6		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(4)
T_{CH1CH2}	CLKOUT Rise Time		10		10	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		10		10	ns	3.5 to 1.0V

NOTES:
1. External clock applied to X1 and X2 not connected.
2. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}.
3. Tested under worst case conditions: V_{CC} = 5.5V T_A = 70°C.
4. Tested under worst case conditions: V_{CC} = 4.5V T_A = 0°C.

AC CHARACTERISTICS

CLOCK TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL16		80C188XL20			
		Min	Max	Min	Max		
80C188XL CLKIN REQUIREMENTS(1)							
T_{CKIN}	CLKIN Period	31.25	∞	25	∞	ns	
T_{CLCK}	CLKIN Low Time	13	∞	10	∞	ns	1.5V(2)
T_{CHCK}	CLKIN High Time	13	∞	10	∞	ns	1.5V(2)
T_{CKHL}	CLKIN Fall Time		5		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5		5	ns	1.0 to 3.5V
80C188XL CLKOUT TIMING							
T_{CICO}	CLKIN to CLKOUT Skew		17		17	ns	
T_{CLCL}	CLKOUT Period	62.5		50		ns	
T_{CLCH}	CLKOUT Low Time	0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(3)
T_{CHCL}	CLKOUT High Time	0.5 T_{CLCL} − 5		0.5 T_{CLCL} − 5		ns	C_L = 100 pF(4)
T_{CH1CH2}	CLKOUT Rise Time		10		8	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		10		8	ns	3.5 to 1.0V

NOTES:
1. External clock applied to X1 and X2 not connected.
2. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}.
3. Tested under worst case conditions: V_{CC} = 5.5V T_A = 70°C.
4. Tested under worst case conditions: V_{CC} = 4.5V T_A = 0°C.

AC CHARACTERISTICS

READY, PERIPHERAL AND QUEUE STATUS TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL		80C188XL12			
		Min	Max	Min	Max		
80C188XL READY AND PERIPHERAL TIMING REQUIREMENTS							
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	15		15		ns	
T_{CLSRY}	SRDY Transition Hold Time(1)	15		15		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time(2)	15		15		ns	
T_{CLARX}	ARDY Active Hold Time(1)	15		15		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	15		15		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	25		25		ns	
T_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time(2)	15		15		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time(2)	15		15		ns	
80C188XL PERIPHERAL AND QUEUE STATUS TIMING RESPONSES							
T_{CLTMV}	Timer Output Delay		40		33	ns	
T_{CHQSV}	Queue Status Delay		37		32	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

AC CHARACTERISTICS

READY, PERIPHERAL AND QUEUE STATUS TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL16		80C188XL20			
		Min	Max	Min	Max		
80C188XL READY AND PERIPHERAL TIMING REQUIREMENTS							
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	15		10		ns	
T_{CLSRY}	SRDY Transition Hold Time(1)	15		10		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time(2)	15		10		ns	
T_{CLARX}	ARDY Active Hold Time(1)	15		10		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	15		10		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	25		15		ns	
T_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time(2)	15		10		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time(2)	15		10		ns	
80C188XL PERIPHERAL AND QUEUE STATUS TIMING RESPONSES							
T_{CLTMV}	Timer Output Delay		27		22	ns	
T_{CHQSV}	Queue Status Delay		30		27	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

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AC CHARACTERISTICS

RESET AND HOLD/HLDA TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL		80C188XL12			
		Min	Max	Min	Max		
80C188XL RESET AND HOLD/HLDA TIMING REQUIREMENTS							
T_{RESIN}	$\overline{RES}$ Setup	15		15		ns	
T_{HVCL}	HOLD Setup(1)	15		15		ns	
80C188XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
80C188XL RESET AND HOLD/HLDA TIMING RESPONSES							
T_{CLRO}	Reset Delay		40		33	ns	
T_{CLHAV}	HLDA Valid Delay	3	40	3	33	ns	
T_{CHCZ}	Command Lines Float Delay		40		33	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		44		36	ns	

NOTE:
1. To guarantee recognition at next clock.

AC CHARACTERISTICS

RESET AND HOLD/HLDA TIMINGS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50 pF.
For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where V_{IH} = V_{CC} − 0.5V.

Symbol	Parameter	Values				Unit	Test Conditions
		80C188XL16		80C188XL20			
		Min	Max	Min	Max		
80C188XL RESET AND HOLD/HLDA TIMING REQUIREMENTS							
T_{RESIN}	$\overline{RES}$ Setup	15		15		ns	
T_{HVCL}	HOLD Setup(1)	15		10		ns	
80C188XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	ns	
T_{CLAV}	Address Valid Delay	3	33	3	22	ns	
80C188XL RESET AND HOLD/HLDA TIMING RESPONSES							
T_{CLRO}	Reset Delay		27		22	ns	
T_{CLHAV}	HLDA Valid Delay	3	25	3	22	ns	
T_{CHCZ}	Command Lines Float Delay		28		25	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		32		26	ns	

NOTE:
1. To guarantee recognition at next clock.

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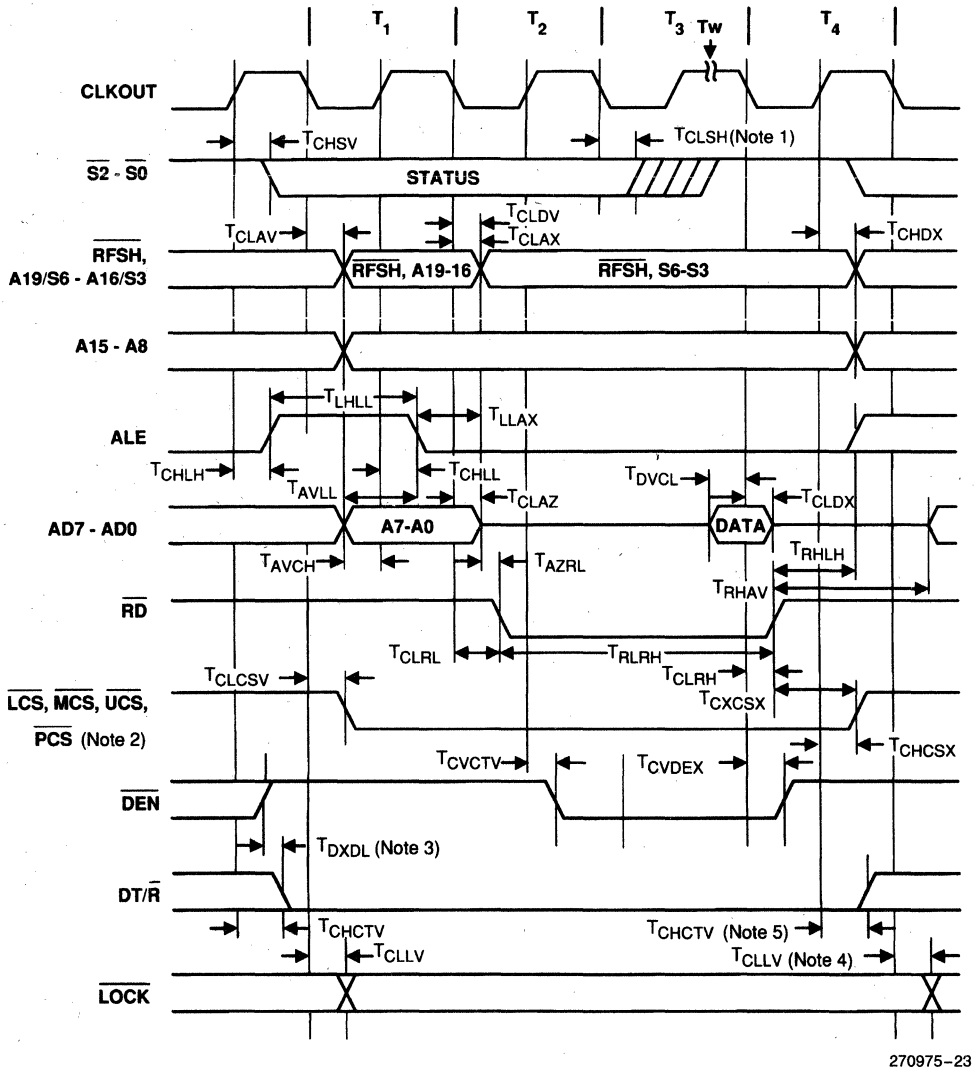
AC CHARACTERISTICS

READ CYCLE WAVEFORMS

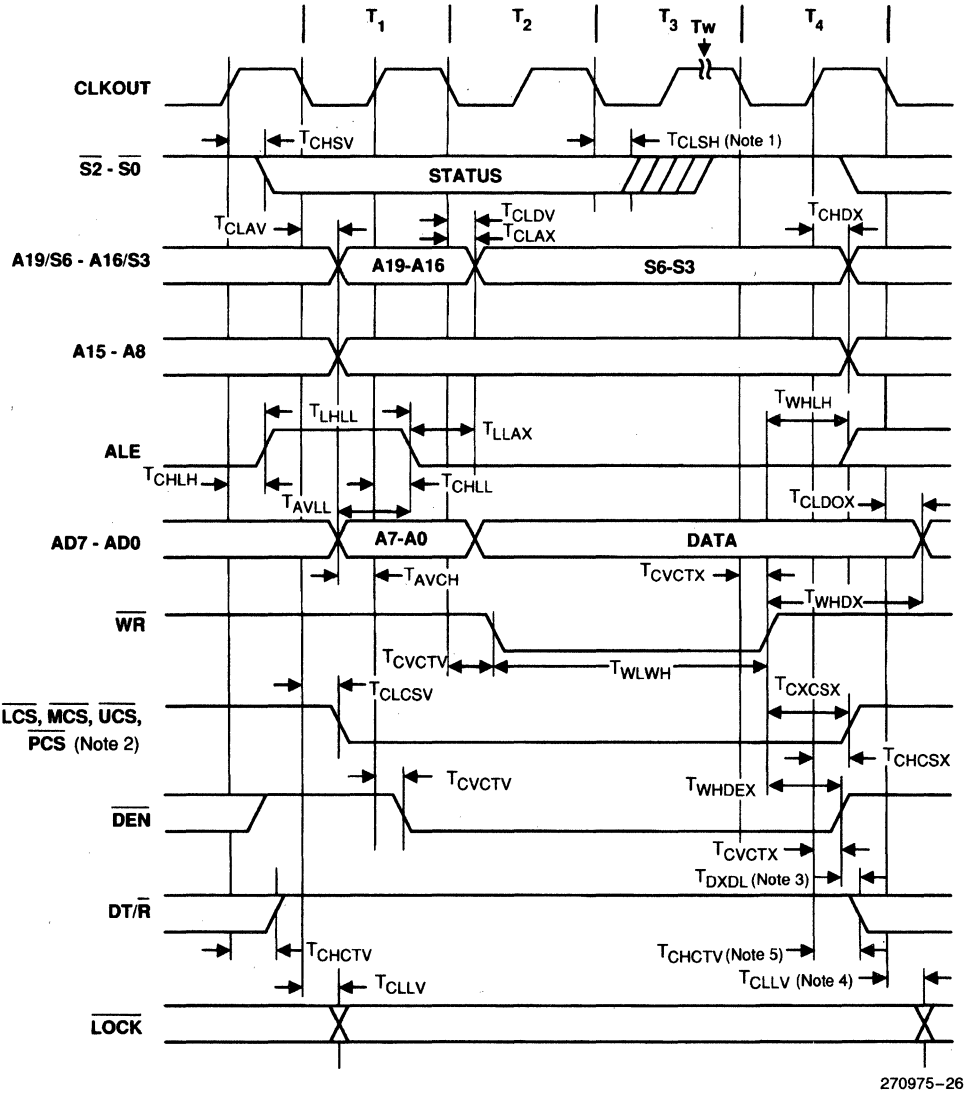


NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by write.

Figure 5

AC CHARACTERISTICS

WRITE CYCLE WAVEFORMS

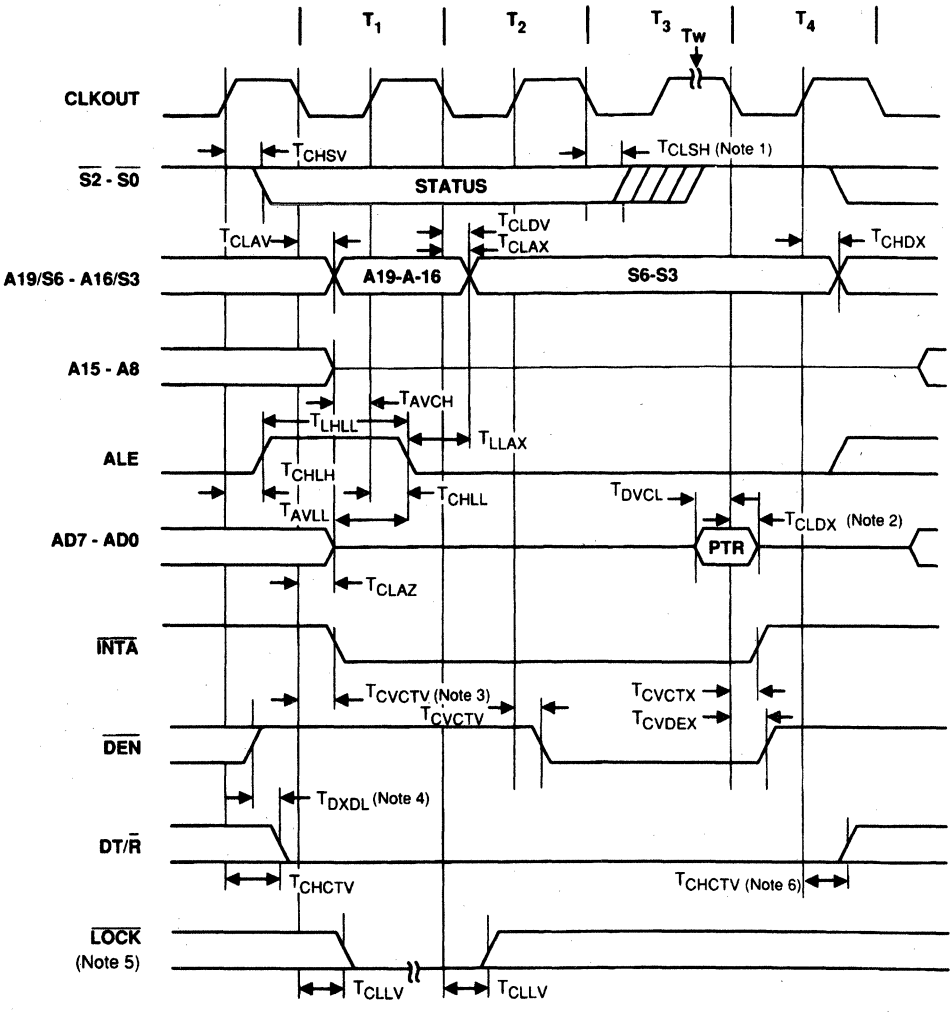


NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by read, INTA, or halt.

Figure 6

AC CHARACTERISTICS

INTERRUPT ACKNOWLEDGE CYCLE WAVEFORMS



NOTES:

1. Status inactive in state preceding T_4.
2. The data hold time lasts only until $\overline{INTA}$ goes inactive, even if the $\overline{INTA}$ transition occurs prior to T_{CLDX}(min).
3. $\overline{INTA}$ occurs one clock later in Slave Mode.
4. For write cycle followed by interrupt acknowledge cycle.
5. $\overline{LOCK}$ is active upon T_1 of the first interrupt acknowledge cycle and inactive upon T_2 of the second interrupt acknowledge cycle.
6. Changes in T-state preceding next bus cycle if followed by write.

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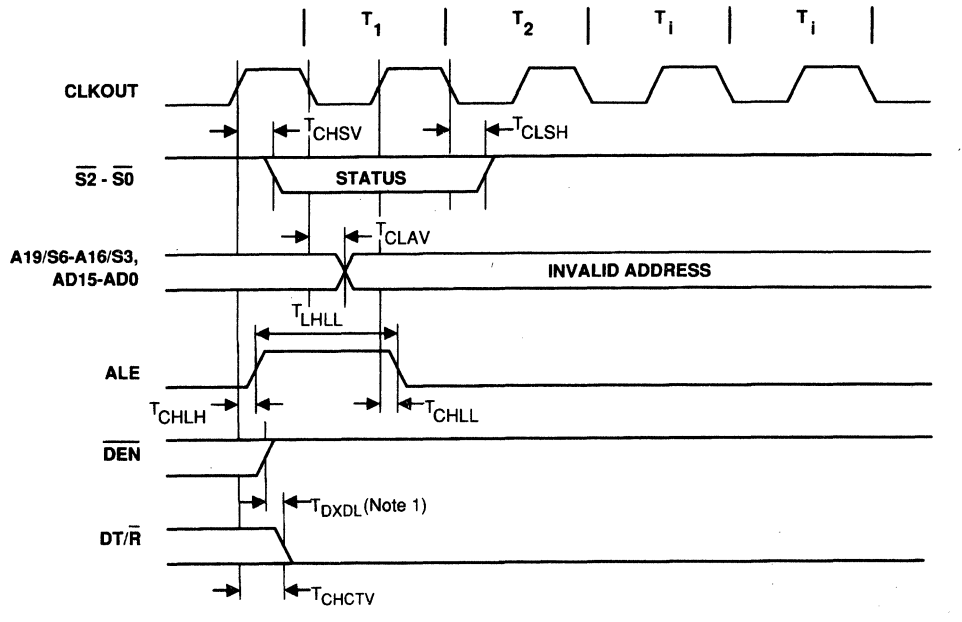
Figure 7

AC CHARACTERISTICS

SOFTWARE HALT CYCLE WAVEFORMS



NOTE:
1. For write cycle followed by halt cycle.

Figure 8

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CLOCK WAVEFORMS

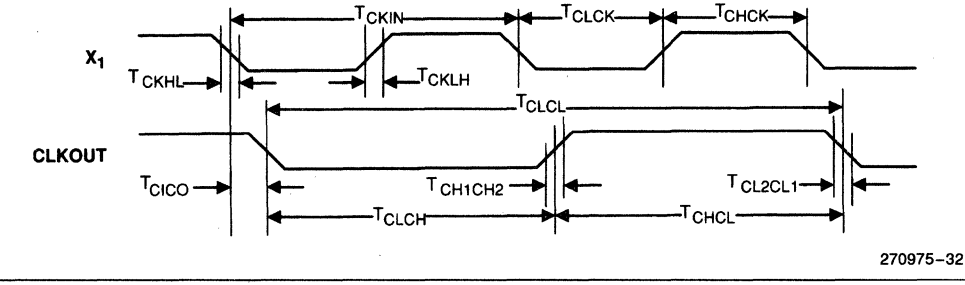

Figure 9

AC CHARACTERSITICS

RESET WAVEFORMS

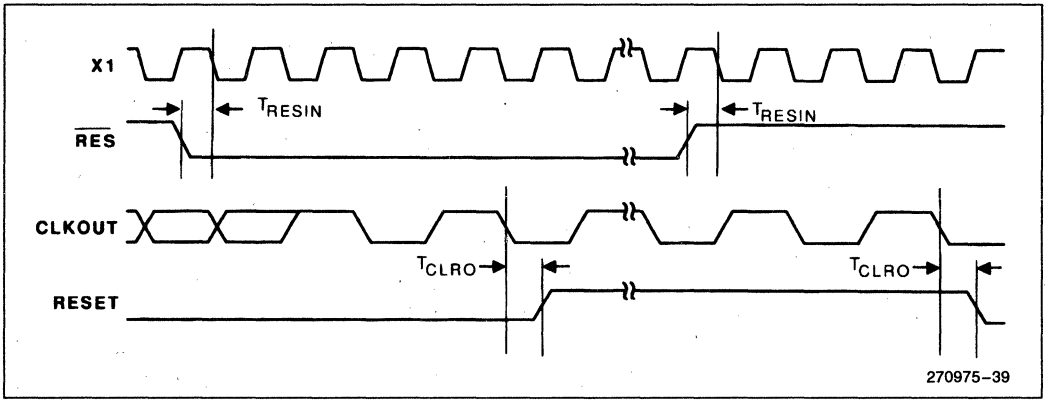

Figure 10

SYNCHRONOUS READY (SRDY) WAVEFORMS

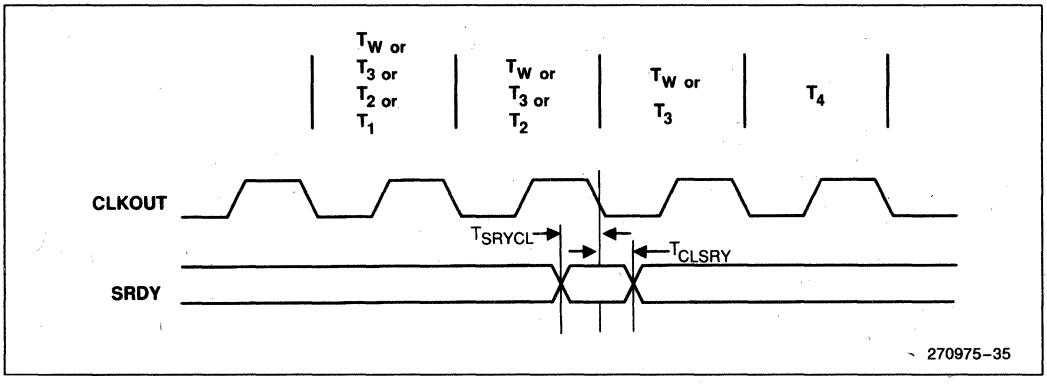

Figure 11

AC CHARACTERISTICS

ASYNCHRONOUS READY (ARDY) WAVEFORMS

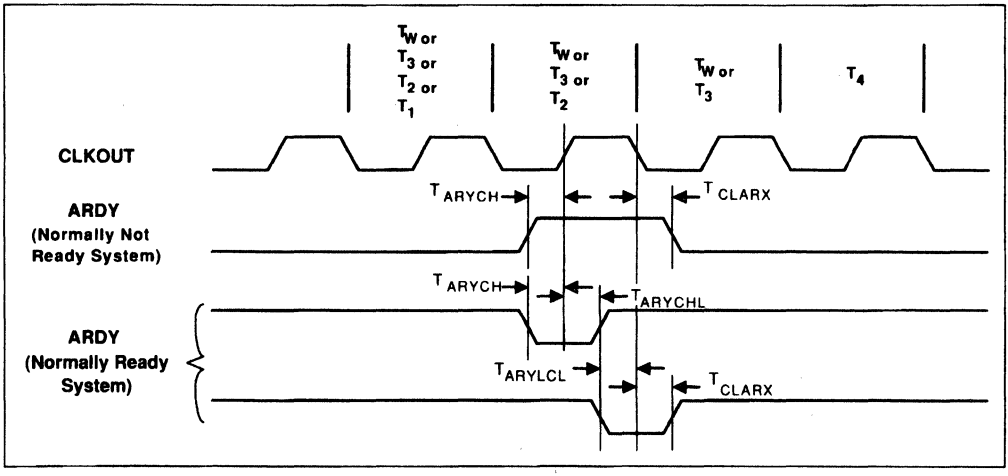

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Figure 12

PERIPHERAL AND QUEUE STATUS WAVEFORMS

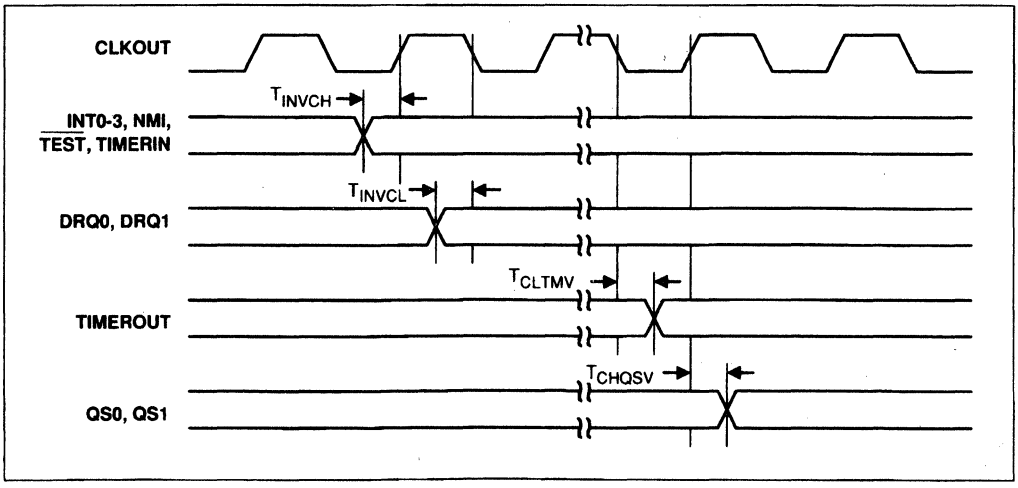

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Figure 13

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AC CHARACTERISTICS

HOLD/HLDA WAVEFORMS (Entering Hold)

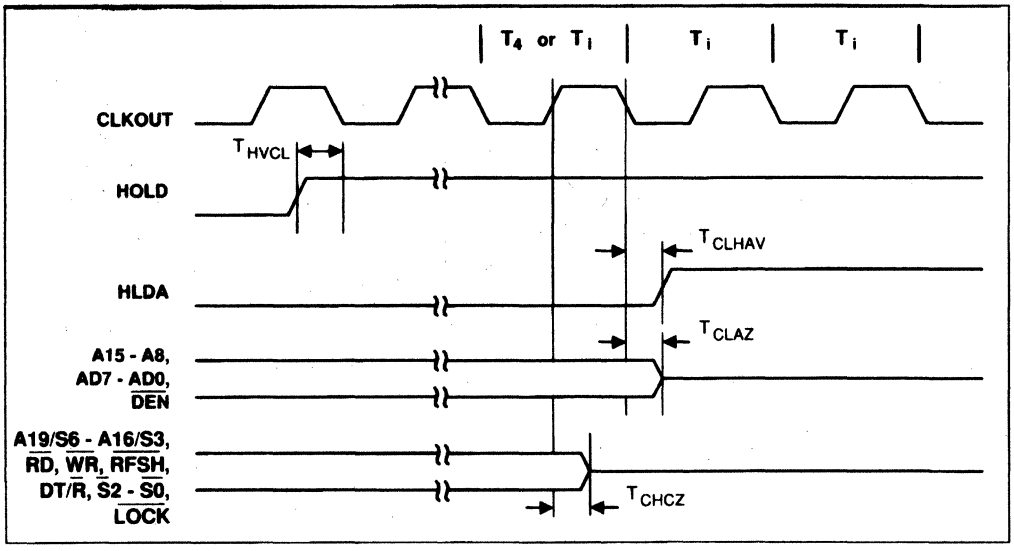
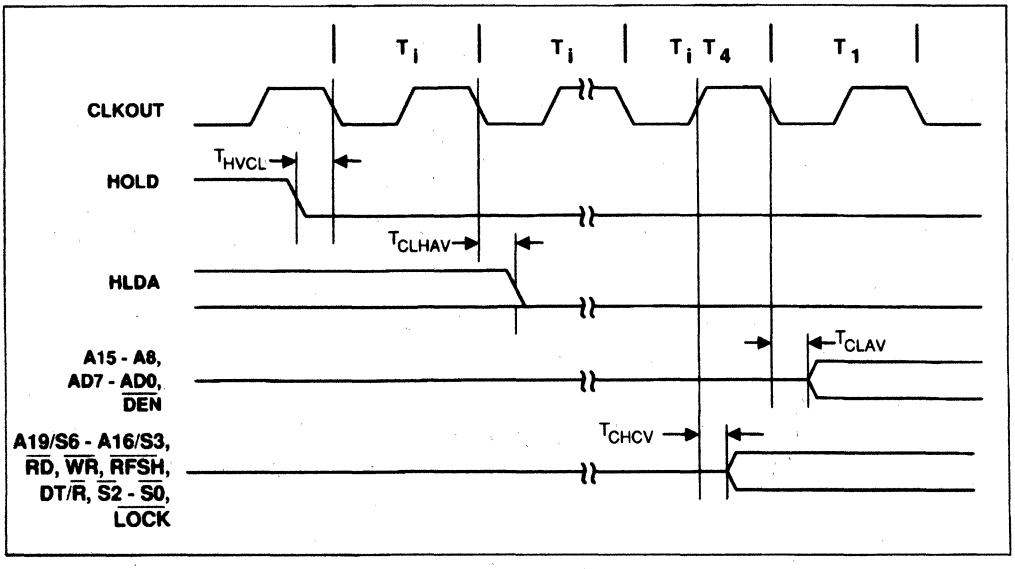


Figure 14

HOLD/HLDA WAVEFORMS (Leaving Hold)



270975-40

Figure 15

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has from 5 to 7 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address

ARY: Asynchronous Ready Input

C: Clock Output

CK: Clock Input

CS: Chip Select

CT: Control (DT/$\overline{R}$, $\overline{DEN}$, . . .)

D: Data Input

DE: $\overline{DEN}$

H: Logic Level High

IN: Input (DRQ0, TIM0, . . .)

L: Logic Level Low or ALE

O: Output

QS: Queue Status (QS1, QS2)

R: $\overline{RD}$ Signal, RESET Signal

S: Status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$)

SRY: Synchronous Ready Input

V: Valid

W: WR Signal

X: No Longer a Valid Logic Level

Z: Float

Examples:

T_{CLAV}— Time from Clock Low to Address Valid

T_{CHLH}— Time from Clock High to ALE High

T_{CLCSV}— Time from Clock Low to Chip Select Valid

DERATING CURVES

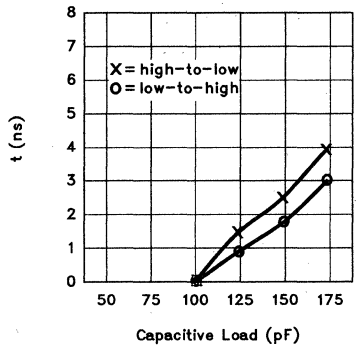


Figure 16. Capacitive Derating Curve

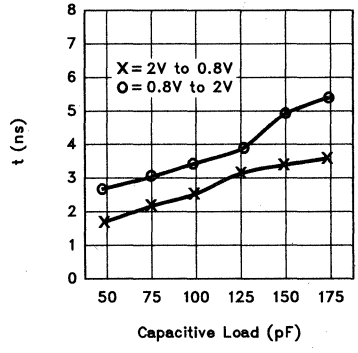


Figure 17. TTL Level Slew Rates for Output Buffers

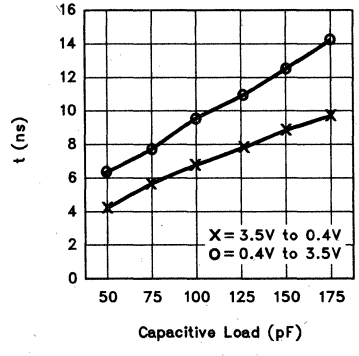


Figure 18. CMOS Level Slew Rates for Output Buffers

80C188XL EXPRESS

The Intel EXPRESS system offers enhancements to the operational specifications of the 80C188XL microprocessor. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

The 80C188XL EXPRESS program includes an extended temperature range. With the commercial standard temperature range operational characteristics are guaranteed over the temperature range of 0°C to +70°C. With the extended temperature range option, operational characteristics are guaranteed over the range of −40°C to +85°C.

Package types and EXPRESS versions are identified by a one or two-letter prefix to the part number. The prefixes are listed in Table 2. All AC and DC specifications not mentioned in this section are the same for both commercial and EXPRESS parts.

Table 2. Prefix Identification

Prefix	Package Type	Temperature Range
A	PGA	Commercial
N	PLCC	Commercial
R	LCC	Commercial
S	QFP	Commercial
TA	PGA	Extended
TN	PLCC	Extended
TR	LCC	Extended
TS	QFP	Extended

80C188XL EXECUTION TIMINGS

A determination of 80C188XL program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

The 80C188XL 8-bit BIU is noticeably limited in its performance relative to the execution unit. A sufficient number of prefetched bytes may not reside in the prefetch queue much of the time. Therefore, actual program execution time will be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1000100w	mod reg r/m			2/12*	
Register/memory to register	1000101w	mod reg r/m			2/9*	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12/13	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3/4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8*	
Accumulator to memory	1010001w	addr-low	addr-high		9*	
Register/memory to segment register	10001110	mod 0 reg r/m			2/13	
Segment register to register/memory	10001100	mod 0 reg r/m			2/15	
PUSH = Push:						
Memory	11111111	mod 1 1 0 r/m			20	
Register	01010 reg				14	
Segment register	000reg110				13	
Immediate	011010s0	data	data if s=0		14	
PUSHA = Push All	01100000				68	
POP = Pop:						
Memory	10001111	mod 0 0 0 r/m			24	
Register	01011 reg				14	
Segment register	000reg111	(reg≠01)			12	
POPA = Pop All	01100001				83	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17*	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10*	
Variable port	1110110w				8*	
OUT = Output to:						
Fixed port	1110011w	port			9*	
Variable port	1110111w				7*	
XLAT = Translate byte to AL	11010111				15	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		26	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		26	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				13	
POPF = Pop flags	10011101				12	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16*	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16*	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15*	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16*	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16*	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15*	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10*	
Register with register/memory	0011100w	mod reg r/m			3/10*	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10*	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10*	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
ARITHMETIC (Continued)			
MUL = Multiply (unsigned):	1111011w | mod 100 r/m		
Register-Byte		26–28	
Register-Word		35–37	
Memory-Byte		32–34	
Memory-Word		41–43*	
IMUL = Integer multiply (signed):	1111011w | mod 101 r/m		
Register-Byte		25–28	
Register-Word		34–37	
Memory-Byte		31–34	
Memory-Word		40–43*	
IMUL = Integer immediate multiply (signed)	011010s1 | mod reg r/m | data | data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w | mod 110 r/m		
Register-Byte		29	
Register-Word		38	
Memory-Byte		35	
Memory-Word		44*	
IDIV = Integer divide (signed):	1111011w | mod 111 r/m		
Register-Byte		44–52	
Register-Word		53–61	
Memory-Byte		50–58	
Memory-Word		59–67*	
AAM = ASCII adjust for multiply	11010100 | 00001010	19	
AAD = ASCII adjust for divide	11010101 | 00001010	15	
CBW = Convert byte to word	10011000	2	
CWD = Convert word to double word	10011001	4	
LOGIC			
Shift/Rotate Instructions:			
Register/Memory by 1	1101000w | mod TTT r/m	2/15	
Register/Memory by CL	1101001w | mod TTT r/m	5+n/17+n	
Register/Memory by Count	1100000w | mod TTT r/m | count	5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR		
AND = **And:**			
Reg/memory and register to either	001000dw | mod reg r/m	3/10*	
Immediate to register/memory	1000000w | mod 100 r/m | data | data if w=1	4/16*	
Immediate to accumulator	0010010w | data | data if w=1	3/4	8/16-bit

Shaded areas indicate instructions not available in 8086/8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
TEST = And function to flags, no result:						
Register/memory and register	1000010w	mod reg r/m			3/10*	
Immediate data and register/memory	1111011w	mod000 r/m	data	data if w=1	4/10*	
Immediate data and accumulator	1010100w	data	data if w=1		3/4	8/16-bit
OR = Or:						
Reg/memory and register to either	000010dw	mod reg r/m			3/10*	
Immediate to register/memory	1000000w	mod001 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0000110w	data	data if w=1		3/4	8/16-bit
XOR = Exclusive or:						
Reg/memory and register to either	001100dw	mod reg r/m			3/10*	
Immediate to register/memory	1000000w	mod110 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0011010w	data	data if w=1		3/4	8/16-bit
NOT = Invert register/memory	1111011w	mod010 r/m			3/10*	
STRING MANIPULATION						
MOVS = Move byte/word	1010010w				14*	
CMPS = Compare byte/word	1010011w				22*	
SCAS = Scan byte/word	1010111w				15*	
LODS = Load byte/wd to AL/AX	1010110w				12*	
STOS = Store byte/wd from AL/AX	1010101w				10*	
INS = Input byte/wd from DX port	0110110w				14	
OUTS = Output byte/wd to DX port	0110111w				14	
Repeated by count in CX (REP/ REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	11110010	1010010w			8+8n*	
CMPS = Compare string	1111001z	1010011w			5+22n*	
SCAS = Scan string	1111001z	1010111w			5+15n*	
LODS = Load string	11110010	1010110w			6+11n*	
STOS = Store string	11110010	1010101w			6+9n*	
INS = Input string	11110010	0110110w			8+8n*	
OUTS = Output string	11110010	0110111w			8+8n*	
CONTROL TRANSFER						
CALL = Call:						
Direct within segment	11101000	disp-low	disp-high		19	
Register/memory indirect within segment	11111111	mod010 r/m			17/27	
Direct intersegment	10011010	segment offset			31	
		segment selector				
Indirect intersegment	11111111	mod011 r/m	(mod ≠ 11)		54	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
JMP = Unconditional jump:						
Short/long	11101011	disp-low			14	
Direct within segment	11101001	disp-low	disp-high		14	
Register/memory indirect within segment	11111111	mod 100 r/m			11/21	
Direct intersegment	11101010	segment offset			14	
		segment selector				
Indirect intersegment	11111111	mod 101 r/m	(mod ≠ 11)		34	
RET = Return from CALL:						
Within segment	11000011				20	
Within seg adding immed to SP	11000010	data-low	data-high		22	
Intersegment	11001011				30	
Intersegment adding immediate to SP	11001010	data-low	data-high		33	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					19	
L = 1					29	
L > 1					26 + 20(n − 1)	
LEAVE = Leave Procedure	11001001				8	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
CONTROL TRANSFER (Continued)			
INT = Interrupt:			
Type specified	11001101 | type	47	
Type 3	11001100	45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110	48/4	
IRET = Interrupt return	11001111	28	
BOUND = Detect value out of range	01100010 | mod reg r/m	33–35	
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

24

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

REVISION HISTORY

The following changes were made between the -001 and -002 versions of the 80C188XL data sheets. The -002 data sheet applies to any 80C188XL with a "B" alpha character after the FPO number. The FPO number location is shown in Figure 2.

1. Much of the information provided in the -001 version of the data sheet has been removed. Detail descriptions of part functionality may be found in the 80C188XL User's Manual.
2. All AC Timing waveforms were combined at the end of the AC Characteristics section.
3. t_{WHLH} for the 80C188XL12 was changed from $t_{CLCH} - 10$ to $t_{CLCH} - 14$ due to a previous typographical error.
4. t_{RESIN} for the 80C188XL20 was changed from 10 ns to 15 ns.
5. Output test conditions were changed from C_L = 50 − 200 pF to C_L = 50 pF to reflect newer test equipment. Note: This has no effect on AC Timing specifications.

ERRATA

An A or B step 80C188XL has the following errata. The A or B step 80C188XL can be identified by the presence of an "A" or "B" alpha character, respectively, next to the FPO number. The FPO number location is shown in Figure 2.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the INTA1 line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistantly, it is dependent on interrupt timing.

PRODUCT IDENTIFICATION

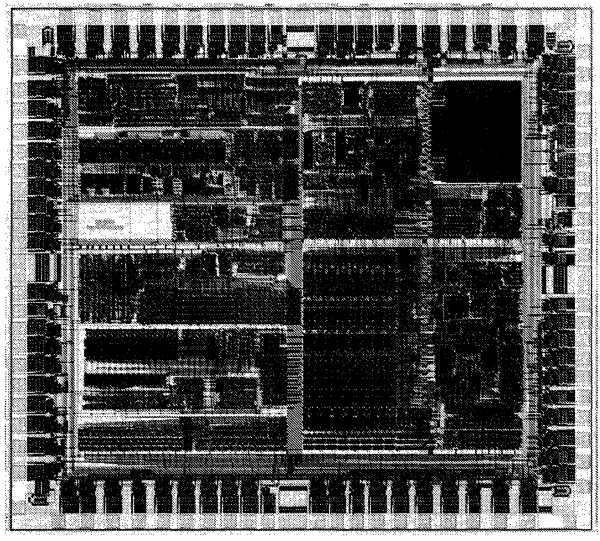
Intel 80C188XL devices are marked with a 9-character alphanumeric Intel FPO number underneath the product number. This data sheet (270975-002) is valid for 80C188XL devices with an "A" or "B" as the ninth character in the FPO number, as illustrated in Figure 2.

80C188EA20, 16, 12
16-BIT HIGH INTEGRATION EMBEDDED PROCESSOR

- 80C188 Upgrade for Power Critical Applications
- Full Static Operation
- True CMOS Inputs and Outputs

- Integrated Feature Set
  - Static 186 CPU Core
  - Power Save, Idle and Powerdown Modes
  - Clock Generator
  - 2 Independent DMA Channels
  - 3 Programmable 16-Bit Timers
  - Dynamic RAM Refresh Control Unit
  - Programmable Memory and Peripheral Chip Select Logic
  - Programmable Wait State Generator
  - Local Bus Controller
  - System-Level Testing Support (High Impedance Test Mode)
- Speed Versions Available:
  - 20 MHz (80C188EA20)
  - 16 MHz (80C188EA16)
  - 12.5 MHz (80C188EA12)
- Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O
- Complete System Development Support
  - All 8086/8088 and 80C186 Family Software Development Tools Can Be Used for 80C188EA System Development
    - ASM86 Assembler, iC-86, Pascal-86, Fortran-86, PL/M-86, and System Utilities
    - In-Circuit-Emulator (ICE™-186)
- Available in the Following Packages:
  - 68-Pin Plastic Leaded Chip Carrier (PLCC)
  - 80-Pin EIAJ Quad Flat Pack (QFP)

The 80C188EA is a CHMOS high integration embedded microprocessor. The 80C188EA includes all of the features of an "Enhanced Mode" 80C188 while adding the additional capabilities of Idle and Powerdown Modes.



272020-1

April 1992
Order Number: 272020-002

80C188EA20, 16, 12
16-Bit High Integration Embedded Processor

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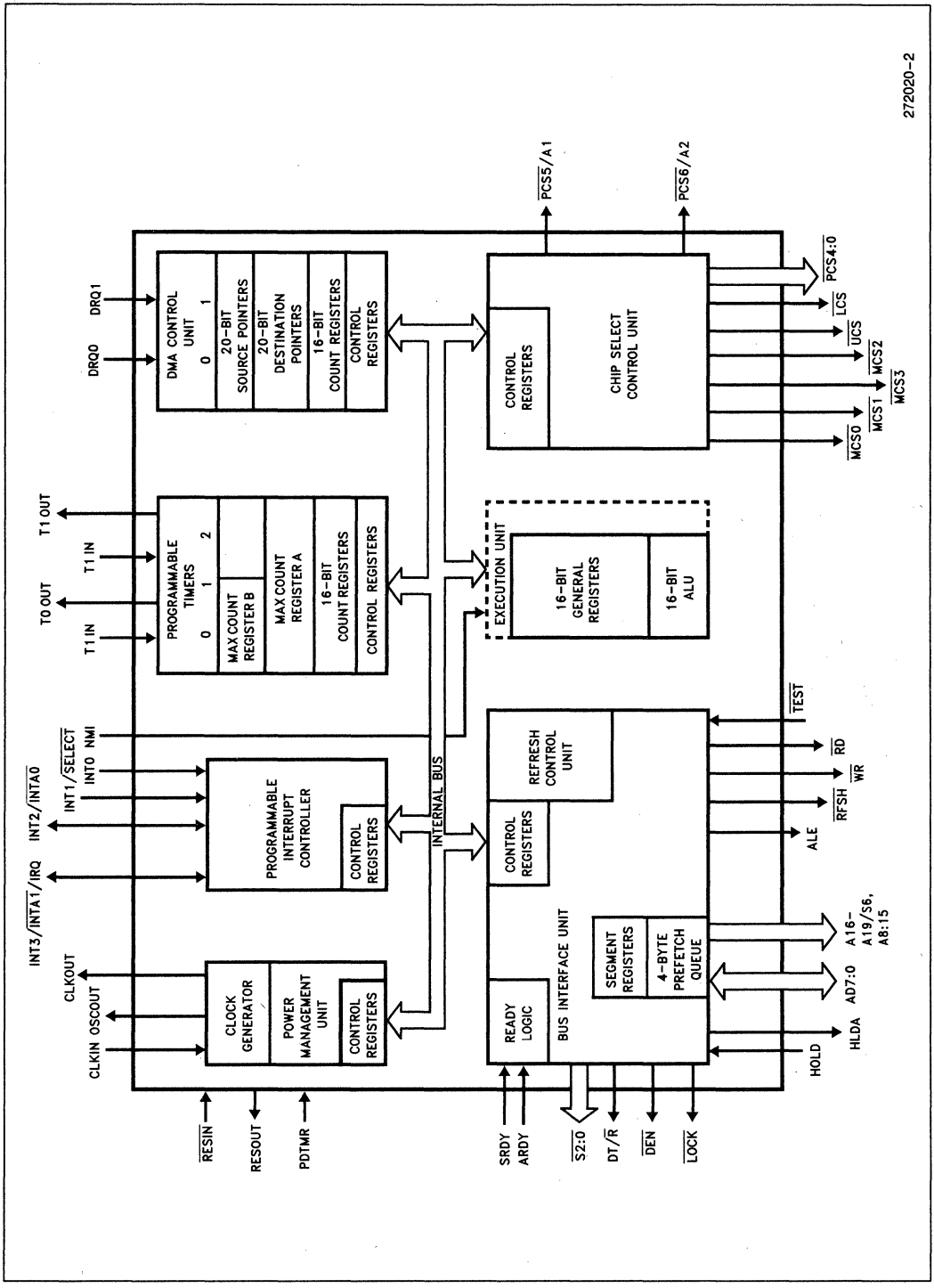


Figure 1. 80C188EA Block Diagram

INTRODUCTION

The 80C188EA is the second product in a new generation of low-power, high-integration microprocessors. It enhances the existing 80C188 by offering new features and new operating modes. The 80C188EA is object code compatible with the 80C186/80C188 embedded processor.

The feature set of the 80C188EA meets the needs of low-power, space-critical applications. Low-power applications benefit from the static design of the CPU core and the integrated peripherals. Minimum current consumption is achieved by providing a Powerdown Mode that halts operation of the device, and freezes the clock circuits. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space-critical applications benefit from the integration of commonly used system peripherals. Two flexible DMA channels perform CPU-independent data transfers. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 128 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters round out the feature set of the 80C188EA.

OVERVIEW

Figure 1 shows a block diagram of the 80C188EA. The Execution Unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instructions, and static operation. The Bus Interface Unit (BIU) is the same as that found on the original 80C188 family products. An independent internal bus is used to allow communication between the BIU and internal peripherals.

80C188EA CORE ARCHITECTURE

Bus Interface Unit

The 80C188EA core incorporates a bus controller that generates local bus control signals. In addition, it employs a HOLD/HLDA protocol to share the local bus with other bus masters.

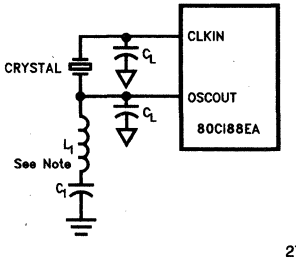
The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information and data (for write operations) information. It is also responsible for reading data off the local bus during a read operation. SRDY and ARDY input pins are provided to extend a bus cycle beyond the minimum four states (clocks).

The 80C188EA local bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the mulitplexed address/data bus.

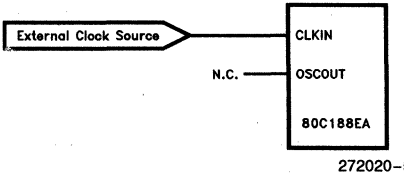
Clock Generator

The 80C188EA provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, and two low-power operating modes.

The oscillator circuit is designed to be used with either a **parallel resonant** fundamental or third-overtone mode crystal network. Alternatively, the oscillator circuit may be driven from an external clock source. Figure 2 shows the various operating modes of the 80C188EA oscillator circuit.



(A) Crystal Connection



(B) Clock Connection

NOTE:
The L_1C_1 network is **only** required when using a third-overtone crystal.

Figure 2. 80C188EA Clock Configurations

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide-by-two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.

The following parameters are recommended when choosing a crystal:

Temperature Range:	Application Specific
ESR (Equivalent Series Resistance):	60Ω max
C0 (Shunt Capacitance of Crystal):	7.0 pF max
C_L (Load Capacitance):	20 pF ± 5 pF
Drive Level:	2 mW max

80C188EA PERIPHERAL ARCHITECTURE

The 80C188EA has integrated several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexible and provide logical interconnections between supporting units (e.g., the interrupt control unit supports interrupt requests from the timer/counters or DMA channels).

The list of integrated peripherals include:

- 4-Input Interrupt Control Unit
- 3-Channel Timer/Counter Unit
- 2-Channel DMA Unit
- 13-Output Chip-Select Unit
- Refresh Control Unit
- Power Management logic

The registers associated with each integrated peripheral are contained within a 128 x 16 register file called the Peripheral Control Block (PCB). The PCB can be located in either memory or I/O space on any 256 byte address boundary.

Figure 3 provides a list of the registers associated with the PCB when the processor's Interrupt Control Unit is in Master Mode. In Slave Mode, the definitions of some registers change. Figure 4 provides register definitions specific to Slave Mode.

Interrupt Control Unit

The 80C188EA can receive interrupts from a number of sources, both internal and external. The Interrupt Control Unit (ICU) serves to merge these requests on a priority basis, for individual service by the CPU. Each interrupt source can be independently masked by the Interrupt Control Unit or all interrupts can be globally masked by the CPU.

Internal interrupt sources include the Timers and DMA channels. External interrupt sources come from the four input pins INT3:0. The NMI interrupt pin is not controlled by the ICU and is passed directly to the CPU. Although the timers only have one request input to the ICU, separate vector types are generated to service individual interrupts within the Timer Unit.

Timer/Counter Unit

The 80C188EA Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms, generate timed interrupts, etc.

PCB Offset	Function
00H	Reserved
02H	Reserved
04H	Reserved
06H	Reserved
08H	Reserved
0AH	Reserved
0CH	Reserved
0EH	Reserved
10H	Reserved
12H	Reserved
14H	Reserved
16H	Reserved
18H	Reserved
1AH	Reserved
1CH	Reserved
1EH	Reserved
20H	Reserved
22H	End of Interrupt
24H	Poll
26H	Poll Status
28H	Interrupt Mask
2AH	Priority Mask
2CH	In-Service
2EH	Interrupt Request
30H	Interrupt Status
32H	Timer Control
34H	DMA0 Int. Control
36H	DMA1 Int. Control
38H	INT0 Control
3AH	INT1 Control
3CH	INT2 Control
3EH	INT3 Control

PCB Offset	Function
40H	Reserved
42H	Reserved
44H	Reserved
46H	Reserved
48H	Reserved
4AH	Reserved
4CH	Reserved
4EH	Reserved
50H	Timer 0 Count
52H	Timer 0 Compare A
54H	Timer 0 Compare B
56H	Timer 0 Control
58H	Timer 1 Count
5AH	Timer 1 Compare A
5CH	Timer 1 Compare B
5EH	Timer 1 Control
60H	Timer 2 Count
62H	Timer 2 Compare
64H	Reserved
66H	Timer 2 Control
68H	Reserved
6AH	Reserved
6CH	Reserved
6EH	Reserved
70H	Reserved
72H	Reserved
74H	Reserved
76H	Reserved
78H	Reserved
7AH	Reserved
7CH	Reserved
7EH	Reserved

PCB Offset	Function
80H	Reserved
82H	Reserved
84H	Reserved
86H	Reserved
88H	Reserved
8AH	Reserved
8CH	Reserved
8EH	Reserved
90H	Reserved
92H	Reserved
94H	Reserved
96H	Reserved
98H	Reserved
9AH	Reserved
9CH	Reserved
9EH	Reserved
A0H	UMCS
A2H	LMCS
A4H	PACS
A6H	MMCS
A8H	MPCS
AAH	Reserved
ACH	Reserved
AEH	Reserved
B0H	Reserved
B2H	Reserved
B4H	Reserved
B6H	Reserved
B8H	Reserved
BAH	Reserved
BCH	Reserved
BEH	Reserved

PCB Offset	Function
C0H	DMA0 Src. Lo
C2H	DMA0 Src. Hi
C4H	DMA0 Dest. Lo
C6H	DMA0 Dest. Hi
C8H	DMA0 Count
CAH	DMA0 Control
CCH	Reserved
CEH	Reserved
D0H	DMA1 Src. Lo
D2H	DMA1 Src. Hi
D4H	DMA1 Dest. Lo
D6H	DMA1 Dest. Hi
D8H	DMA1 Count
DAH	DMA1 Control
DCH	Reserved
DEH	Reserved
E0H	Refresh Base
E2H	Refresh Time
E4H	Refresh Control
E6H	Reserved
E8H	Reserved
EAH	Reserved
ECH	Reserved
EEH	Reserved
F0H	Power-Save
F2H	Power Control
F4H	Reserved
F6H	Step ID
F8H	Reserved
FAH	Reserved
FCH	Reserved
FEH	Relocation

Figure 3. 80C188EA Peripheral Control Block Registers

PCB Offset	Function
20H	Interrupt Vector
22H	Specific EOI
24H	Reserved
26H	Reserved
28H	Interrupt Mask
2AH	Priority Mask
2C	In-Service
2E	Interrupt Request
30	Interrupt Status
32	TMR0 Interrupt Control
34	DMA0 Interrupt Control
36	DMA1 Interrupt Control
38	TMR1 Interrupt Control
3A	TMR2 Interrupt Control
3C	Reserved
3E	Reserved

Figure 4. 80C188EA Slave Mode Peripheral Control Block Registers

DMA Control Unit

The 80C188EA DMA Contol Unit provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O space in any combination: memory to memory, memory to I/O, I/O to I/O or I/O to memory. Each data transfer consumes two bus cycles (a minimum of eight clocks), one cycle to fetch data and the other to store data. The chip-select/ready logic may be programmed to point to the memory or I/O space subject to DMA transfers in order to provide hardware chip-select lines. DMA cycles run at higher priority than general processor execution cycles.

Chip-Select Unit

The 80C188EA Chip-Select Unit integrates logic which provides up to 13 programmable chip-selects to access both memories and peripherals. In addition, each chip-select can be programmed to automatically terminate a bus cycle independent of the condition of the SRDY and ARDY input pins. The chip-select lines are available for all memory and I/O bus cycles, whether they are generated by the CPU, the DMA unit, or the Refresh Control Unit.

Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 9-bit address generator is maintained by the RCU with the address presented on the A9:1 address lines during the refresh bus cycle. Address bits A19:13 are programmable to allow the refresh address block to be located on any 8 Kbyte boundary.

Power Management

The 80C188EA has three operational modes to control the power consumption of the device. They are Power Save Mode, Idle Mode, and Powerdown Mode.

Power Save Mode divides the processor clock by a programmable value to take advantage of the fact that current is linearly proportional to frequency. An unmasked interrupt, NMI, or reset will cause the 80C188EA to exit Power Save Mode.

Idle Mode freezes the clocks of the Execution Unit and the Bus Interface Unit at a logic zero state while all peripherals operate normally.

Powerdown Mode freezes all internal clocks at a logic zero level and disables the crystal oscillator. All internal registers hold their values provided V_{CC} is maintained. Current consumption is reduced to transistor leakage only.

ONCE™ Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C188EA has a test mode available which forces all output and input/output pins to be placed in the high-impedance state. ONCE stands for "ON Circuit Emulation". The ONCE mode is selected by forcing the $\overline{UCS}$ and $\overline{LCS}$ pins LOW (0) during a processor reset (these pins are weakly held to a HIGH (1) level) while $\overline{RESIN}$ is active.

DIFFERENCES BETWEEN THE 80C188 AND THE 80C188EA

The 80C188EA is intended as a direct functional upgrade for 80C188 designs. In many cases, it will be possible to replace an existing 80C188 with little or no hardware redesign. The following sections describe differences in pinout, operating modes, and AC and DC specifications to keep in mind.

Pinout Compatibility

The 80C188EA requires a PDTMR pin to time the processor's exit from Powerdown Mode. The original pin arrangement for the 80C188 in the PLCC package did not have any spare leads to use for PDTMR, so the DT/$\overline{R}$ pin was sacrificed. The arrangement of all the other leads in the 68-lead PLCC is identical between the 80C188 and the 80C188EA. DT/$\overline{R}$ may be readily synthesized by latching the $\overline{S1}$ status output. Therefore, upgrading a PLCC 80C188 to PLCC 80C188EA is particularly straightforward. You must connect a capacitor to the 80C188EA PDTMR pin in order to use Powerdown Mode.

The 80-lead QFP (EIAJ) pinouts are distinctly different between the 80C188 and the 80C188EA. In addition to the PDTMR pin, the 80C188EA has more power and ground pins and the overall arrangement of pins was shifted. A new circuit board layout for the 80C188EA is required.

Operating Modes

The 80C188 has two operating modes, Compatible and Enhanced. Compatible Mode is a pin-to-pin replacement for the NMOS 80188, except for numerics coprocessing. In Enhanced Mode, the processor has a Refresh Control Unit and the Power-Save feature. The 80C188EA does not have different operating modes. All 80C188EA features are present in regular operation.

TTL vs CMOS Inputs

The inputs of the 80C188EA are rated for CMOS switching levels for improved noise immunity, but the 80C188 inputs are rated for TTL switching levels. In particular, the 80C188EA requires a minimum V_{IH} of 3.5V to recognize a logic one while the 80C188 requires a minimum V_{IH} of only 1.9V (assuming 5.0V operation). The solution is to drive the 80C188EA with true CMOS devices, such as those from the HC and AC logic families, or to use pullup resistors where the added current draw is not a problem.

Timing Specifications

80C188EA timing relationships are expressed in a simplified format over the 80C188. The AC performance of an 80C188EA at a specified frequency will be very close to that of an 80C188 at the same frequency. Check the timings applicable to your design prior to replacing the 80C188.

PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the 80C188EA in the Plastic Leaded Chip Carrier (PLCC) package and Quad Flat Pack (QFP) package. For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

Pin Descriptions

Each pin or logical set of pins is described in Table 2. There are three columns for each entry in the Pin Description Table.

The **Pin Name** column contains a mnemonic that describes the pin function. Negation of the signal name (for example, $\overline{RESIN}$) denotes a signal that is active low.

The **Pin Type** column contains two kinds of information. The first symbol indicates whether a pin is power (P), ground (G), input only (I), output only (O) or input/output (I/O). Some pins have multiplexed functions (for example, A19/S6). Additional symbols indicate additional characteristics for each pin. Table 4 lists all the possible symbols for this column.

Input pins may be either synchronous or asynchronous. Asynchronous pins require that setup and hold times be met only in order to guarantee *recognition* at a particular clock edge. Synchronous pins require that setup and hold times be met to guarantee proper *operation*. For example, missing the setup or hold time for the SRDY pin (a synchronous input) will result in a system failure or lockup. Input pins may also be edge- or level-sensitive. The possible characteristics for input pins are S(E), S(L), A(E) and A(L).

Output states are dependent upon the current activity of the processor. There are four operational states that are different from regular operation: bus hold, reset, Idle Mode, and Powerdown Mode. Appropriate characteristics for these states are also indicated in this column, with the legend for all possible characteristics in Table 1.

Finally, the **Pin Description** column contains a text description of each pin.

As an example, consider AD7:0. I/O signifies the pins are bidirectional. S(L) signifies that the input function is synchronous and level-sensitive. H(Z) signifies that, as outputs, the pins are high-impedance upon acknowledgement of bus hold. R(Z) signifies that the pins float during reset. P(X) signifies that the pins retain their states during Powerdown Mode.

Table 1. Pin Description Nomenclature

Symbol	Description
P	Power Pin (Apply + V_{CC} Voltage)
G	Ground (Connect to V_{SS})
I	Input Only Pin
O	Output Only Pin
I/O	Input/Output Pin
S(E)	Synchronous, Edge Sensitive
S(L)	Synchronous, Level Sensitive
A(E)	Asynchronous, Edge Sensitive
A(L)	Asynchronous, Level Sensitive
H(1)	Output Driven to V_{CC} during Bus Hold
H(0)	Output Driven to V_{SS} during Bus Hold
H(Z)	Output Floats during Bus Hold
H(Q)	Output Remains Active during Bus Hold
H(X)	Output Retains Current State during Bus Hold
R(WH)	Output Weakly Held at V_{CC} during Reset
R(1)	Output Driven to V_{CC} during Reset
R(0)	Output Driven to V_{SS} during Reset
R(Z)	Output Floats during Reset
R(Q)	Output Remains Active during Reset
R(X)	Output Retains Current State during Reset
I(1)	Output Driven to V_{CC} during Idle Mode
I(0)	Output Driven to V_{SS} during Idle Mode
I(Z)	Output Floats during Idle Mode
I(Q)	Output Remains Active during Idle Mode
I(X)	Output Retains Current State during Idle Mode
P(1)	Output Driven to V_{CC} during Powerdown Mode
P(0)	Output Driven to V_{SS} during Powerdown Mode
P(Z)	Output Floats during Powerdown Mode
P(Q)	Output Remains Active during Powerdown Mode
P(X)	Output Retains Current State during Powerdown Mode

Table 2. 80C188EA Pin Descriptions

Name	Type	Description
V_{CC}		**POWER** connections consist of six pins which must be shorted externally to a V_{CC} board plane.
V_{SS}		**GROUND** connections consist of five pins which must be shorted externally to a V_{SS} board plane.
CLKIN	I A(E)	**CLocK INput** is an input for an external clock. An external oscillator operating at two times the required 80C188EA operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O H(Q) R(Q) P(Q)	**OSCillator OUTput** is only used when using a crystal to generate the external clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin is not to be used as 2X clock output for non-crystal applications (i.e., this pin is N.C. for non-crystal applications). OSCOUT does not float in ONCE mode.
CLKOUT	O H(Q) R(Q) P(Q)	**CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transistions every falling edge of CLKIN.
$\overline{\text{RESIN}}$	I A(L)	**RESet IN** causes the 80C188EA to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the 80C188EA begins fetching opcodes at memory location 0FFFF0H.
RESOUT	O H(0) R(1) P(0)	**RESet OUTput** that indicates the 80C188EA is currently in the reset state. RESOUT will remain active as long as $\overline{\text{RESIN}}$ remains active. When tied to the $\overline{\text{TEST}}$/BUSY pin, RESOUT forces the 80C188EA into Numerics Mode.
PDTMR	I/O A(L) H(WH) R(Z) P(1)	**Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the 80C188EA waits after an exit from power down before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I A(E)	**Non-Maskable Interrupt** input causes a Type 2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{\text{TEST}}$	I A(E)	$\overline{\text{TEST}}$ is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (low).
AD7:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed **Address** and **Data** bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle.
A15:8	O H(Z) R(Z) P(Z)	These pins provide **Address** information throughout the entire bus cycle.
A18:16 A19/S6	H(Z) R(Z) P(X)	These pins provide multiplexed **Address** during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. A18:16 are driven to a logic 0 during the data phase of the bus cycle. Also during the data phase, S6 is driven to a logic 0 to indicate a CPU-initiated bus cycle or logic 1 to indicate a DMA-initiated bus cycle or a refresh cycle.

Table 2. 80C188EA Pin Descriptions (Continued)

Name	Type	Description
$\overline{S2:0}$	O H(Z) R(Z) P(1)	Bus cycle **Status** are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ Bus Cycle Initiated 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive (no bus activity)
ALE/QS0	O H(0) R(0) P(0)	**Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle. In Queue Status Mode, QS0 provides queue status information along with QS1.
$\overline{RFSH}$	O H(Z) R(Z) P(1)	**ReFreSH** output signals that a refresh cycle is in progress.
$\overline{RD}/\overline{QSMD}$	I/O H(Z) R(WH) P(1)	**ReaD** output signals that the accessed memory or I/O device must drive data information onto the data bus. Upon reset, this pin has an alternate function. As $\overline{QSMD}$, it enables **Queue Status Mode** when grounded. In Queue Status Mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide the following information about processor/instruction queue interaction: QS1 QS0 Queue Operation 0 0 No Queue Operation 0 1 First Opcode Byte Fetched from the Queue 1 1 Subsequent Byte Fetched from the Queue 1 0 Empty the Queue
$\overline{WR}$/QS1	O H(Z) R(Z) P(1)	**WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device. In Queue Status Mode, QS1 provides queue status information along with QS0.
ARDY	I A(L) S(L)	**Asychronous ReaDY** is an input to signal for the end of a bus cycle. ARDY is asynchronous on rising CLKOUT and synchronous on falling CLKOUT. ARDY or SRDY must be active to terminate any 80C188EA bus cycle, unless they are ignored due to correct programming of the Chip Select Unit.
SRDY	I S(L)	**Synchronous ReaDY** is an input to signal for the end of a bus cycle. ARDY or SRDY must be active to terminate any 80C188EA bus cycle, unless they are ignored due to correct programming of the Chip Select Unit.
$\overline{DEN}$	O H(Z) R(Z) P(1)	**Data ENable** output to control the enable of bidirectional transceivers when buffering an 80C188EA system. $\overline{DEN}$ is active only when data is to be transferred on the bus.

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Table 2. 80C188EA Pin Descriptions (Continued)

Name	Type	Description
DT/$\overline{R}$	O H(Z) R(Z) P(X)	**Data Transmit/Receive** output controls the direction of a bi-directional buffer when buffering an 80C188EA system. DT/$\overline{R}$ is only available for the QFP (EIAJ) package (S80C188EA).
$\overline{LOCK}$	I/O H(Z) R(WH) P(1)	**LOCK** output indicates that the bus cycle in progress is not to be interrupted. The 80C188EA will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low.
HOLD	I A(L)	**HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The 80C188EA will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
HLDA	O H(1) R(0) P(0)	**HoLD Acknowledge** output to indicate that the 80C188EA has relinquish control of the local bus. When HLDA is asserted, the 80C188EA will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly.
$\overline{UCS}$	O H(1) R(1) P(1)	**Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH. During a processor reset, $\overline{UCS}$ and $\overline{LCS}$ are used to enable ONCE Mode.
$\overline{LCS}$	O H(1) R(1) P(1)	**Lower Chip Select** will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. $\overline{LCS}$ is inactive after a reset. During a processor reset, $\overline{UCS}$ and $\overline{LCS}$ are used to enable ONCE Mode.
$\overline{MCS3:0}$	O H(1) R(1) P(1) A(L)	If enabled, these pins comprise a block of **Mid-Range Chip Select** outputs which will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user.
$\overline{PCS4:0}$	O H(1) R(1) P(1)	**Peripheral Chip Selects** go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user.
$\overline{PCS5}$/A1 $\overline{PCS6}$/A2	0 H(1)/H(X) R(1) P(1)	These pins provide a multiplexed function. As additional **Peripheral Chip Selects,** they go active whenever the address of a memory or I/O bus cycle is within the address limitations by the user. They may also be programmed to provide latched **Address** A2:1 signals.
T0OUT T1OUT	O H(Q) R(1) P(Q)	**Timer OUTput** pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.
T0IN T1IN	I A(L) A(E)	**Timer INput** is used either as clock or control signals, depending on the timer mode selected.

Table 2. 80C188EA Pin Descriptions (Continued)

Name	Type	Description
DRQ0 DRQ1	I A(L)	**DMA ReQuest** is asserted by an external request when it is prepared for a DMA transfer.
INT0 INT1/$\overline{\text{SELECT}}$	I A(E,L)	Maskable **INTerrupt** input will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with $\overline{\text{INTA0}}$ and $\overline{\text{INTA1}}$ to interface with an external slave controller. INT1 becomes $\overline{\text{SELECT}}$ when the ICU is configured for Slave Mode.
INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$/IRQ	I/O A(E,L) /H(1) R(Z) /P(1)	These pins provide multiplexed functions. As inputs, they provide a maskable **INTerrupt** that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an **INTerrupt Acknowledge** handshake signal to allow interrupt expansion. INT3/$\overline{\text{INTA1}}$ becomes **IRQ** when the ICU is configured for Slave Mode.
N.C.	—	**No Connect.** For compatibility with future products, do not connect to these pins.

80C188EA PINOUT

Tables 3 and 4 list the 80C188EA pin names with package location for the 68-pin Plastic Leaded Chip Carrier (PLCC) component. Figure 5 depicts the complete 80C188EA pinout (PLCC package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 5 and 6 list the 80C188EA pin names with package location for the 80-pin Quad Flat Pack (EIAJ) component. Figure 6 depicts the complete 80C188EA (EIAJ QFP package) as viewed from the top side of the component (i.e., contacts facing down).

Table 3. PLCC Pin Names with Package Location

Address/Data Bus	
Name	**Location**
AD0	17
AD1	15
AD2	13
AD3	11
AD4	8
AD5	6
AD6	4
AD7	2
A8	16
A9	14
A10	12
A11	10
A12	7
A13	5
A14	3
A15	1
A16	68
A17	67
A18	66
A19/S6	65

Bus Control	
Name	**Location**
ALE/QS0	61
$\overline{\text{RFSH}}$	64
$\overline{\text{S0}}$	52
$\overline{\text{S1}}$	53
$\overline{\text{S2}}$	54
$\overline{\text{RD}}$/QSMD	62
$\overline{\text{WR}}$/QS1	63
ARDY	55
SRDY	49
$\overline{\text{DEN}}$	39
$\overline{\text{LOCK}}$	48
HOLD	50
HLDA	51

Power	
Name	**Location**
V_{SS}	26, 60
V_{CC}	9, 43

Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	24
RESOUT	57
CLKIN	59
OSCOUT	58
CLKOUT	56
$\overline{\text{TEST}}$	47
PDTMR	40
NMI	46
INT0	45
INT1/SELECT	44
INT2/$\overline{\text{INTA0}}$	42
INT3/$\overline{\text{INTA1}}$/IRQ	41

I/O	
Name	**Location**
$\overline{\text{UCS}}$	34
$\overline{\text{LCS}}$	33
$\overline{\text{MCS0}}$	38
$\overline{\text{MCS1}}$	37
$\overline{\text{MCS2}}$	36
$\overline{\text{MCS3}}$	35
$\overline{\text{PCS0}}$	25
$\overline{\text{PCS1}}$	27
$\overline{\text{PCS2}}$	28
$\overline{\text{PCS3}}$	29
$\overline{\text{PCS4}}$	30
$\overline{\text{PCS5}}$/A1	31
$\overline{\text{PCS6}}$/A2	32
T0OUT	22
T0IN	20
T1OUT	23
T1IN	21
DRQ0	18
DRQ1	19

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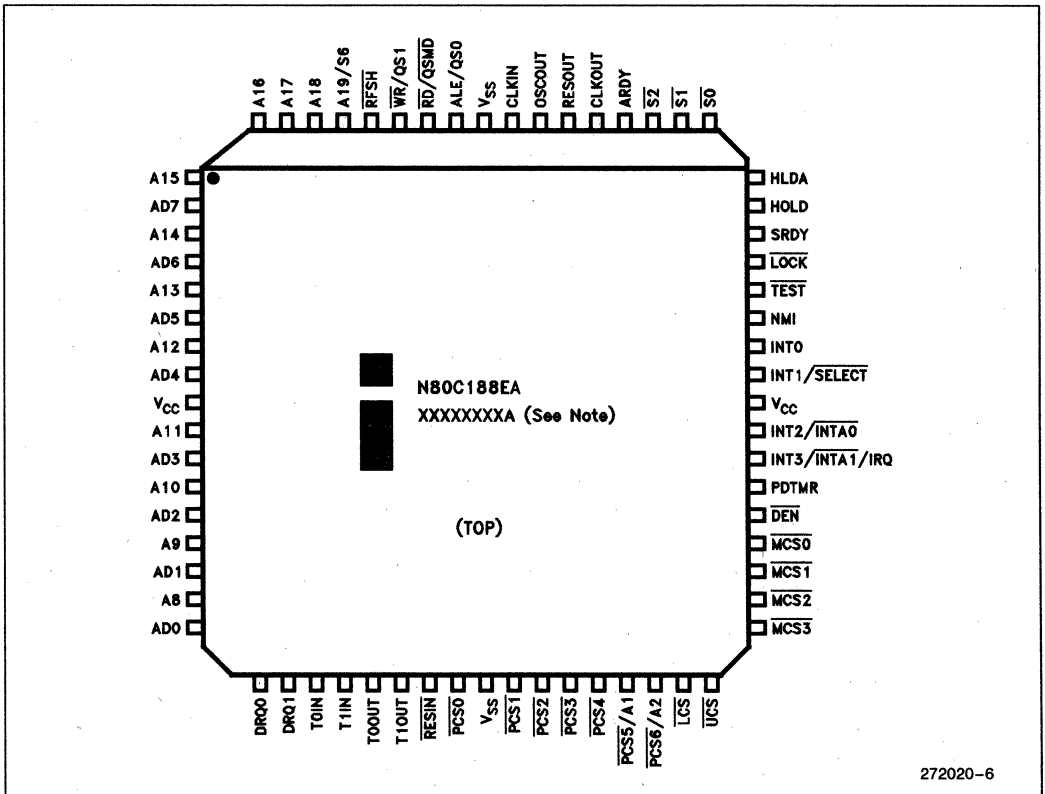
Table 4. PLCC Package Locations with Pin Name

Location	Name	Location	Name	Location	Name	Location	Name
1	A15	18	DRQ0	35	$\overline{MCS3}$	52	$\overline{S0}$
2	AD7	19	DRQ1	36	$\overline{MCS2}$	53	$\overline{S1}$
3	A14	20	T0IN	37	$\overline{MCS1}$	54	$\overline{S2}$
4	AD6	21	T1IN	38	$\overline{MCS0}$	55	ARDY
5	A13	22	T0OUT	39	$\overline{DEN}$	56	CLKOUT
6	AD5	23	T1OUT	40	PDTMR	57	RESOUT
7	A12	24	$\overline{RESIN}$	41	INT3/$\overline{INTA1}$/	58	OSCOUT
8	AD4	25	$\overline{PCS0}$		IRQ	59	CLKIN
9	V_{CC}	26	V_{SS}	42	INT2/$\overline{INTA0}$	60	V_{SS}
10	A11	27	$\overline{PCS1}$	43	V_{CC}	61	ALE/QS0
11	AD3	28	$\overline{PCS2}$	44	INT1/SELECT	62	$\overline{RD}$/$\overline{QSMD}$
12	A10	29	$\overline{PCS3}$	45	INT0	63	$\overline{WR}$/QS1
13	AD2	30	$\overline{PCS4}$	46	NMI	64	$\overline{RFSH}$
14	A9	31	$\overline{PCS5}$/A1	47	$\overline{TEST}$	65	A19/S6
15	AD1	32	$\overline{PCS6}$/A2	48	LOCK	66	A18
16	A8	33	$\overline{LCS}$	49	SRDY	67	A17
17	AD0	34	$\overline{UCS}$	50	HOLD	68	A16
				51	HLDA		



NOTE:
The nine-character alphanumeric code (XXXXXXXXA) underneath the product number is the Intel FPO number.

Figure 5. 68-Lead PLCC Pinout Diagram

Table 5. QFP (EIAJ) Pin Name with Package Location

Address/Data Bus	
Name	**Location**
AD0	64
AD1	66
AD2	68
AD3	70
AD4	74
AD5	76
AD6	78
AD7	80
A8	65
A9	67
A10	69
A11	71
A12	75
A13	77
A14	79
A15	1
A16	3
A17	4
A18	5
A19/S6	6

Bus Control	
Name	**Location**
ALE/QS0	10
$\overline{RFSH}$	7
$\overline{S0}$	23
$\overline{S1}$	22
$\overline{S2}$	21
$\overline{RD}/\overline{QSMD}$	9
$\overline{WR}$/QS1	8
ARDY	20
SRDY	27
DT/$\overline{R}$	37
$\overline{DEN}$	39
$\overline{LOCK}$	28
HOLD	26
HLDA	25

Power	
Name	**Location**
V_{SS}	12, 13, 24, 53, 62
V_{CC}	2, 33, 34, 44, 72, 73

Processor Control	
Name	**Location**
$\overline{RESIN}$	55
RESOUT	18
CLKIN	16
OSCOUT	17
CLKOUT	19
$\overline{TEST}$	29
PDTMR	38
NMI	30
INT0	31
INT1/$\overline{SELECT}$	32
INT2/$\overline{INTA0}$	35
INT3/$\overline{INTA1}$/IRQ	36
N.C.	11, 14, 15, 63

I/O	
Name	**Location**
$\overline{UCS}$	45
$\overline{LCS}$	46
$\overline{MCS0}$	40
$\overline{MCS1}$	41
$\overline{MCS2}$	42
$\overline{MCS3}$	43
$\overline{PCS0}$	54
$\overline{PCS1}$	52
$\overline{PCS2}$	51
$\overline{PCS3}$	50
$\overline{PCS4}$	49
$\overline{PCS5}$/A1	48
$\overline{PCS6}$/A2	47
T0OUT	57
T0IN	59
T1OUT	56
T1IN	58
DRQ0	61
DRQ1	60

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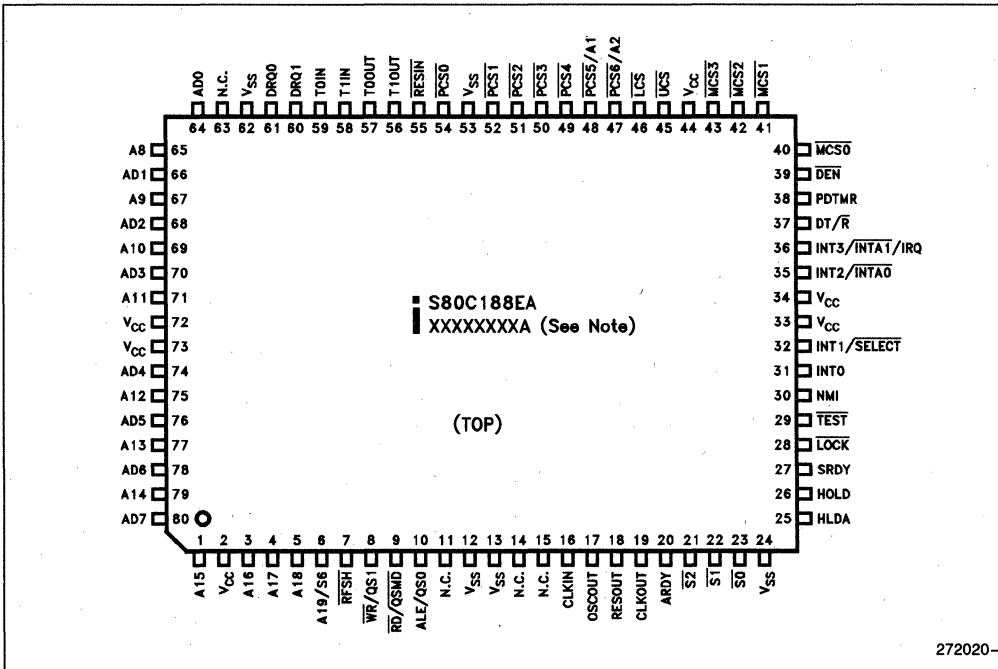
Table 6. QFP (EIAJ) Package Location with Pin Names

Location	Name	Location	Name	Location	Name	Location	Name
1	A15	21	$\overline{S2}$	41	$\overline{MCS1}$	61	DRQ0
2	V_{CC}	22	$\overline{S1}$	42	$\overline{MCS2}$	62	V_{SS}
3	A16	23	$\overline{S0}$	43	$\overline{MCS3}$	63	N.C.
4	A17	24	V_{SS}	44	V_{CC}	64	AD0
5	A18	25	HLDA	45	$\overline{UCS}$	65	A8
6	A19/S6	26	HOLD	46	$\overline{LCS}$	66	AD1
7	$\overline{RFSH}$	27	SRDY	47	$\overline{PCS6}$/A2	67	A9
8	$\overline{WR}$/QS1	28	$\overline{LOCK}$	48	$\overline{PCS5}$/A1	68	AD2
9	$\overline{RD}$/$\overline{QSMD}$	29	$\overline{TEST}$	49	$\overline{PCS4}$	69	A10
10	ALE/QS0	30	NMI	50	$\overline{PCS3}$	70	AD3
11	N.C.	31	INT0	51	$\overline{PCS2}$	71	A11
12	V_{SS}	32	INT1/$\overline{SELECT}$	52	$\overline{PCS1}$	72	V_{CC}
13	V_{SS}	33	V_{CC}	53	V_{SS}	73	V_{CC}
14	N.C.	34	V_{CC}	54	$\overline{PCS0}$	74	AD4
15	N.C.	35	INT2/$\overline{INTA0}$	55	$\overline{RESIN}$	75	A12
16	CLKIN	36	INT3/$\overline{INTA1}$/	56	T1OUT	76	AD5
17	OSCOUT		IRQ	57	T0OUT	77	A13
18	RESOUT	37	DT/$\overline{R}$	58	T1IN	78	AD6
19	CLKOUT	38	PDTMR	59	T0IN	79	A14
20	ARDY	39	$\overline{DEN}$	60	DRQ1	80	AD7
		40	$\overline{MCS0}$				



NOTE:
The nine-character alphanumeric code (XXXXXXXXA) underneath the product number is the Intel FPO number.

Figure 6. Quad Flat Pack (EIAJ) Pinout Diagram

PACKAGE THERMAL SPECIFICATIONS

The 80C188EA is specified for operation when T_C (the case temperature) is within the range of 0°C to 85°C (PLCC package) or 0°C to 106°C (QFP-EIAJ) package. T_C may be measured in any environment to determine whether the 80C188EA is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P \times \theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 7 for the 68-pin Plastic Leaded Chip Carrier (PLCC) package.

Table 8 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies. P (the maximum power consumption, specified in watts) is calculated by using the maximum ICC as tabulated in the DC specifications and V_{CC} of 5.5V.

Table 7. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow Linear ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PLCC)	29	25	21	19	17	16.5
θ_{CA} (QFP)	66	63	60.5	59	58	57

Table 8. Maximum T_A at Various Airflows (in °C)

		Airflow Linear ft/min (m/sec)					
	T_F (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A (PLCC)	25	78	80	81	82	82.5	83
	32	74	76	78	79	79.5	80
	40	70	72	74	75	76	76.5
T_A (QFP)	25	84	85.5	86	87	87	87.5
	32	77.5	79	80	80.5	81	81.5
	40	70	71.5	73	74	74	75

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ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

Absolute Maximum Ratings*

Storage Temperature ..... −65°C to +150°C

Case Temperature under Bias ... −65°C to +150°C

Supply Voltage with Respect to V_{SS} ..... −0.5V to +6.5V

Voltage on Other Pins with Respect to V_{SS} ..... −0.5V to V_{CC} + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.5	5.5	V
T_F	Input Clock Frequency			
	80C188EA20	0	40	MHz
	80C188EA16	0	32	MHz
	80C188EA12	0	25	MHz
T_C	Case Temperature under Bias			
	N80C188EA (PLCC)	0	+100	°C
	S80C188EA (QFP)	0	+114	°C

Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80C188EA based circuit board should contain separate power (V_{CC}) and ground (V_{SS}) planes. All V_{CC} and V_{SS} pins **must** be connected to the appropriate plane. Pins identified as "N.C." must not be connected in the system. Decoupling capacitors should be placed near the 80C188EA. The value and type of decoupling capacitors is application and board layout dependent. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Always connect any unused input pins to an appropriate signal level. In particular, unused interrupt pins (NMI, INT3:0) should be connected to V_{SS} to avoid unwanted interrupts. **Leave any unused output pin or any "N.C." pin unconnected.**

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage for All Pins	−0.5	0.3 V_{CC}	V	
V_{IH}	Input High Voltage for All Pins	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 3 mA (min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −2 mA (min)
V_{HYR}	Input Hysterisis on $\overline{RESIN}$	0.30		V	
I_{IL1}	Input Leakage Current (except $\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$, and $\overline{LOCK}$)		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{IL2}	Input Leakage Current $\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$, and $\overline{LOCK}$)	−275		μA	V_{IN} = 0.7 V_{CC} (Note 1)
I_{OL}	Output Leakage Current		±10	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 2)
I_{CC}	Supply Current Cold (RESET) 80C188EA20 80C188EA16 80C188EA12		 100 80 62.5	 mA mA mA	(Note 3)
I_{ID}	Supply Current In Idle Mode 80C188EA20 80C188EA16 80C188EA12		 70 56 44	 mA mA mA	
I_{PD}	Supply Current In Powerdown Mode 80C188EA20 80C188EA16 80C188EA12		 100 100 100	 μA μA μA	
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 4)
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz

NOTES:
1. $\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$ and $\overline{LOCK}$, and have internal pullups that are only activated during RESET. Loading these pins above I_{OL} = −275 μA will cause the 80C188EA to enter alternate modes of operation.
2. Output pins are floated using HOLD or ONCE Mode.
3. Measured at worst case temperature and V_{CC} with all outputs loaded as specified in the AC Test Conditions, and with the device in RESET ($\overline{RESIN}$ held low). RESET is worst case for I_{CC}.
4. Output capacitance is the capacitive load of a floating output pin.

I_{CC} VERSUS FREQUENCY AND VOLTAGE

The current (I_{CC}) consumption of the 80C188EA is essentially composed of two components; I_{PD} and I_{CCS}.

I_{PD} is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or V_{CC} (no clock applied to the device). I_{PD} is equal to the Powerdown current and is typically less than 50 μA.

I_{CCS} is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since I_{CCS} is typically much greater than I_{PD}, I_{PD} can often be ignored when calculating I_{CC}.

I_{CCS} is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: V = Device operating voltage (V_{CC})

C_{DEV} = Device capacitance

f = Device operating frequency

$I_{CCS} = I_{CC}$ = Device current

Measuring C_{DEV} on a device like the 80C188EA would be difficult. Instead, C_{DEV} is calculated using the above formula by measuring I_{CC} at a known V_{CC} and frequency (see Table 9). Using this C_{DEV} value, I_{CC} can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical I_{CC} when operating at 20 MHz, 4.8V.

$$I_{CC} = I_{CCS} = 4.8 \times 0.515 \times 20 \approx 49 \text{ mA}$$

PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: t = desired delay in **seconds**

C_{PD} = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132$ μF is required. Round up to standard (available) capacitive values.

NOTE:
The above equation applies to delay times greater than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperature will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

Table 9. C_{DEV} Values

Parameter	Typ	Max	Units	Notes
C_{DEV} (Device in Reset)	0.515	0.905	mA/V*MHz	1, 2
C_{DEV} (Device in Idle)	0.391	0.635	mA/V*MHz	1, 2

1. Max C_{DEV} is calculated at −40°C, all floating outputs driven to V_{CC} or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical C_{DEV} is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

AC SPECIFICATIONS

AC Characteristics—80C188EA20

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	40	MHz	1
T_C	CLKIN Period	25	∞	ns	1
T_{CH}	CLKIN High Time	10	∞	ns	1, 2
T_{CL}	CLKIN Low Time	10	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	17	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	22	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{RD}$, $\overline{WR}$	3	27	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	22	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, AD15:8, AD7:0, $\overline{INTA1:0}$, $\overline{S2:0}$	3	27	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, A15:8, AD7:0	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		ns	1, 9
T_{CLIS}	A15:8, AD7:0, ARDY, SRDY, DRQ1:0	10		ns	1, 10
T_{CLIH}	A15:8, AD7:0, ARDY, SRDY, DRQ1	3		ns	1, 10
T_{CLIS}	HOLD	10		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	10		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (from CLKIN)	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 16 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 17 for rise and fall times outside 50 pF.
6. See Figure 17 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C188EA operation (SRDY, AD7:0).

AC SPECIFICATIONS (Continued)

AC Characteristics—80C188EA16

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	32	MHz	1
T_C	CLKIN Period	31.25	∞	ns	1
T_{CH}	CLKIN High Time	10	∞	ns	1, 2
T_{CL}	CLKIN Low Time	10	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	20	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	23	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{RD}$, $\overline{WR}$	3	28	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	23	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, A15:8, AD7:0, $\overline{INTA1:0}$, $\overline{S2:0}$	3	28	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, A15:8, AD7:0	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		ns	1, 9
T_{CLIS}	A15:8, AD7:0, ARDY, SRDY, DRQ1:0	10		ns	1, 10
T_{CLIH}	A15:8, AD7:0, ARDY, SRDY, DRQ1:0	3		ns	1, 10
T_{CLIS}	HOLD	10		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	10		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (from CLKIN)	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 16 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 17 for rise and fall times outside 50 pF.
6. See Figure 17 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C188EA operation (SRDY, AD7:0).

AC SPECIFICATIONS (Continued)

AC Characteristics—80C188EA12

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	25	MHz	1
T_C	CLKIN Period	40	∞	ns	1
T_{CH}	CLKIN High Time	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	23	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, $\overline{LOCK}$, A19:16	3	25	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{RD}$, $\overline{WR}$	3	30	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	25	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, A15:8, AD7:0, $\overline{INTA1:0}$, $\overline{S2:0}$	3	30	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, A15:8, AD7:0	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		ns	1, 9
T_{CLIS}	A15:8, AD7:0, ARDY, SRDY, DRQ1:0	10		ns	1, 10
T_{CLIH}	A15:8, AD7:0, ARDY, SRDY, DRQ1:0	3		ns	1, 10
T_{CLIS}	HOLD	10		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	10		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (to CLKIN)	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 16 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 17 for rise and fall times outside 50 pF.
6. See Figure 17 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C188EA operation (SRDY, AD7:0).

AC SPECIFICATIONS (Continued)

Relative Timings (80C188EA20, 16, 12)

Symbol	Parameter	Min	Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Rising to ALE Falling	T − 15		ns	
T_{AVLL}	Address Valid to ALE Falling	½T − 10		ns	
T_{PLLL}	Chip Selects Valid to ALE Falling	½T − 10		ns	1
T_{LLAX}	Address Hold from ALE Falling	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{RHLH}	$\overline{RD}$ Rising to ALE Rising	½T − 10		ns	1
T_{WHLH}	$\overline{WR}$ Rising to ALE Rising	½T − 10		ns	1
T_{AFRL}	Address Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Falling to $\overline{RD}$ Rising	(2*T) − 5		ns	2
T_{WLWH}	$\overline{WR}$ Falling to $\overline{WR}$ Rising	(2*T) − 5		ns	2
T_{RHAV}	$\overline{RD}$ Rising to Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHDEX}	$\overline{WR}$ Rising to $\overline{DEN}$ Rising	½T − 10		ns	1
T_{WHPH}	$\overline{WR}$ Rising to Chip Select Rising	½T − 10		ns	1, 4
T_{RHPH}	$\overline{RD}$ Rising to Chip Select Rising	½T − 10		ns	1, 4
T_{PHPL}	$\overline{CS}$ Inactive to $\overline{CS}$ Active	½T − 10		ns	1
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		ns	5
T_{OVRH}	ONCE ($\overline{UCS}$, $\overline{LCS}$) Active to $\overline{RESIN}$ Rising	T		ns	3
T_{RHOX}	ONCE ($\overline{UCS}$, $\overline{LCS}$) to $\overline{RESIN}$ Rising	T		ns	3

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Not tested.
4. Not applicable to latched A2:1. These signals change only on falling T_1.
5. For write cycle followed by read cycle.

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 7. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

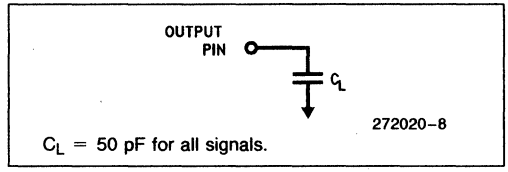

Figure 7. AC Test Load

AC TIMING WAVEFORMS

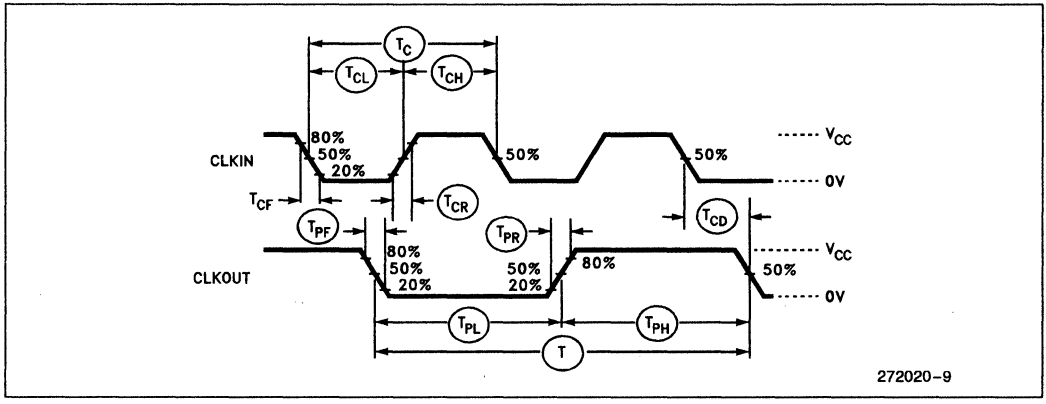

Figure 8. Input and Output Clock Waveform

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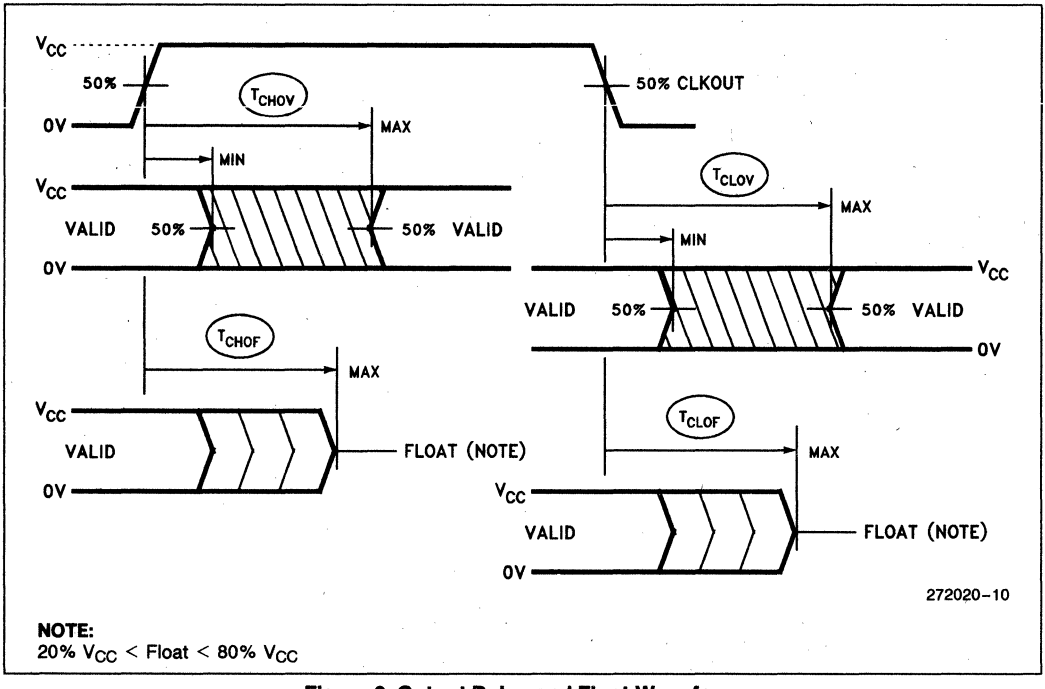
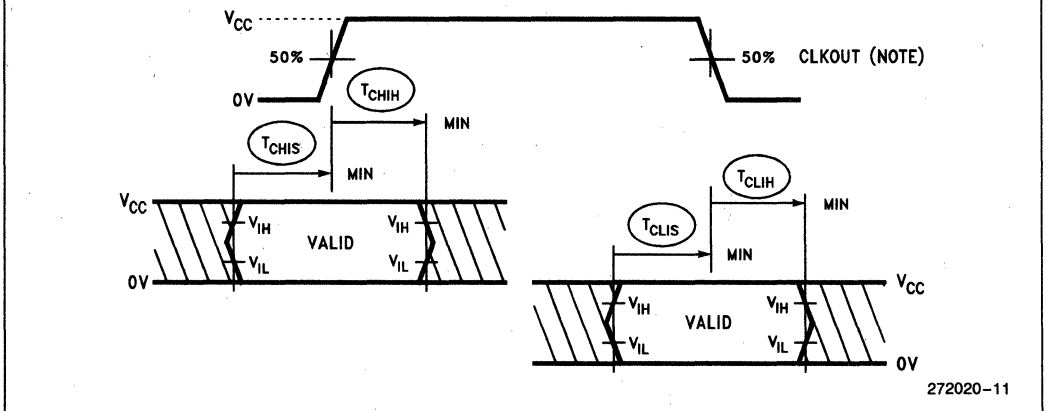


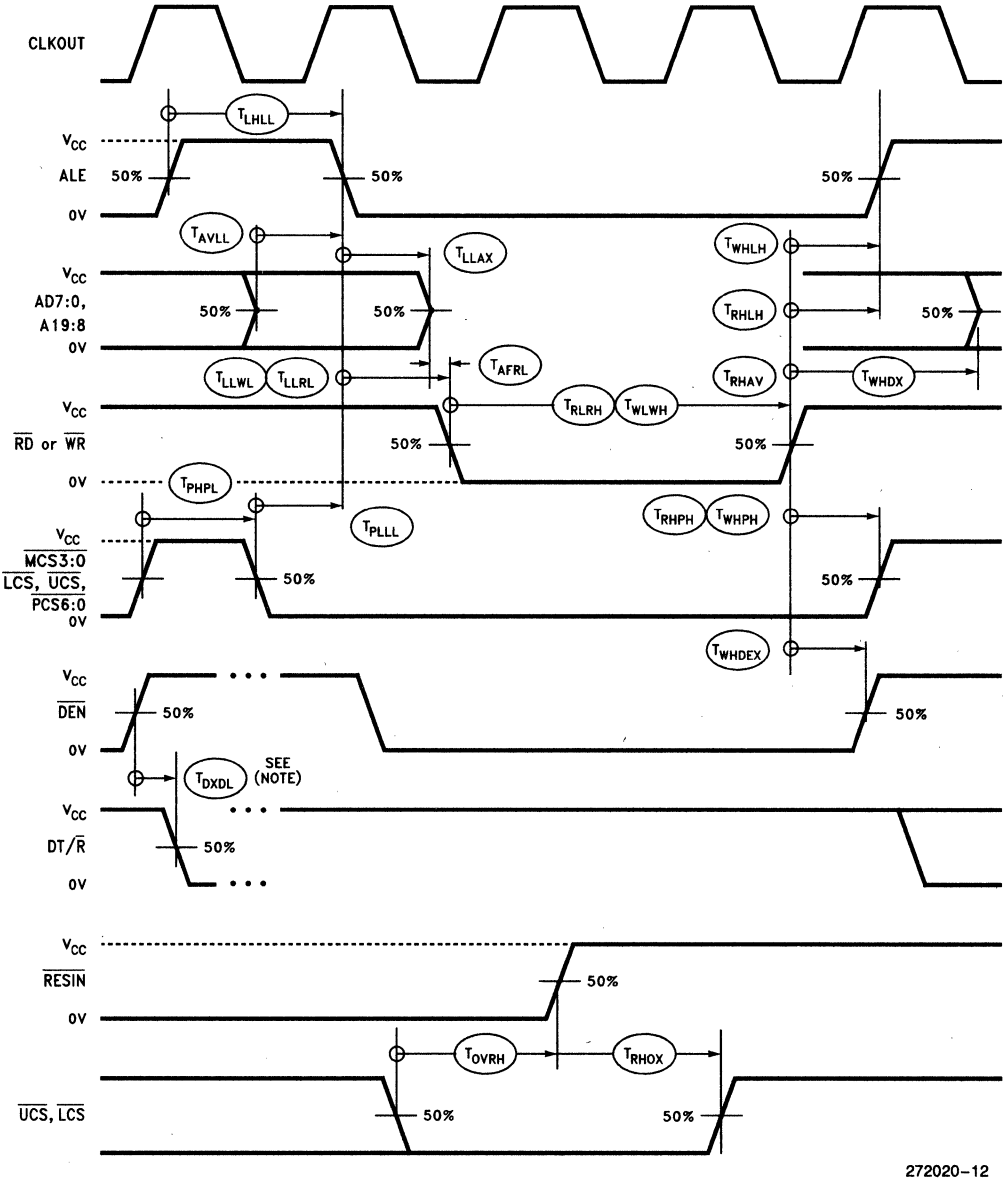
NOTE:
20% V_{CC} < Float < 80% V_{CC}

Figure 9. Output Delay and Float Waveform



NOTE:
RESIN measured to CLKIN, not CLKOUT

Figure 10. Input Setup and Hold



NOTE:
T_{DXDL} for write cycle followed by read cycle.

Figure 11. Relative Signal Waveform

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DERATING CURVES

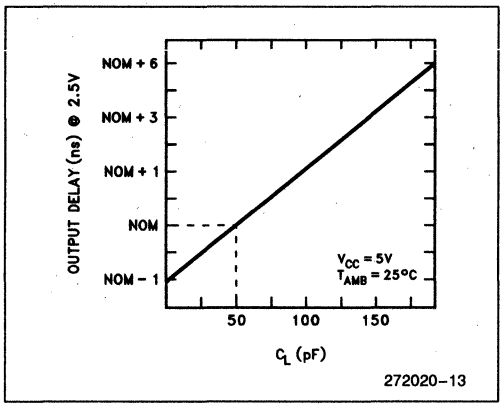


Figure 12. Typical Output Delay Variations Versus Load Capacitance

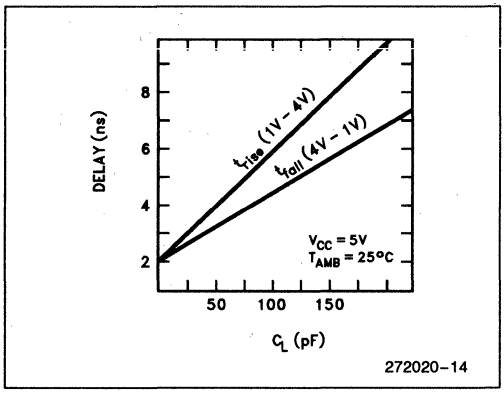


Figure 13. Typical Rise and Fall Variations Versus Load Capacitance

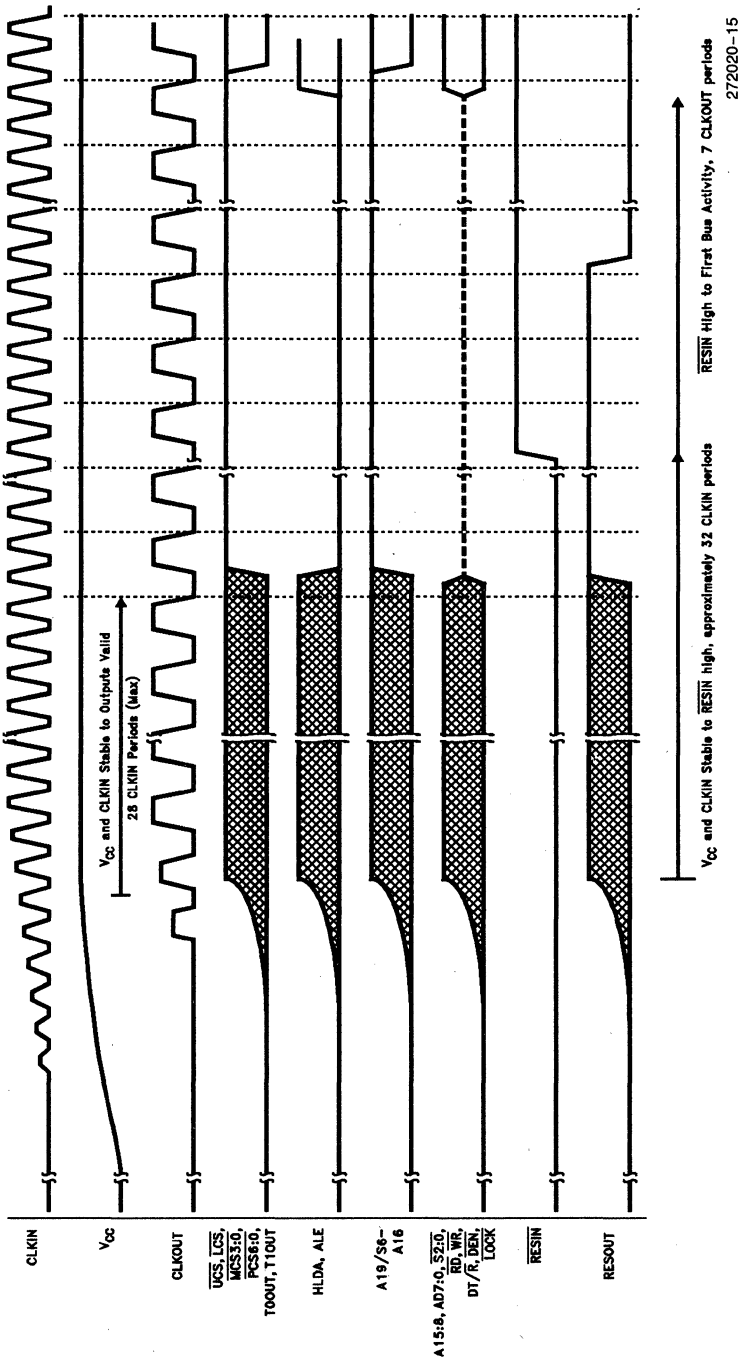
RESET

The 80C188EA will perform a reset operation any time the $\overline{RESIN}$ pin is active. The $\overline{RESIN}$ pin is actually synchronized before it is presented internally, which means that the clock must be operating before a reset can take effect. From a power-on state, $\overline{RESIN}$ must be held active (low) in order to guarantee correct initialization of the 80C188EA. **Failure to provide $\overline{RESIN}$ while the device is powering up will result in unspecified operation of the device.**

Figure 14 shows the correct reset sequence when first applying power to the 80C188EA. An external clock connected to CLKIN must not exceed the V_{CC} threshold being applied to the 80C188EA. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the 80C188EA. When attaching a crystal to the device, $\overline{RESIN}$ must remain active until both V_{CC} and CLKOUT are stable (the length of time is application specific and depends on the startup characteristics of the crystal circuit). The $\overline{RESIN}$ pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that $\overline{RESIN}$ is never really sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Figure 15 shows the timing sequence when $\overline{RESIN}$ is applied after V_{CC} is stable and the device has been operating. Note that a reset will terminate all activity and return the 80C188EA to a known operating state. Any bus operation that is in progress at the time $\overline{RESIN}$ is asserted will terminate immediately (note that most control signals will be driven to their inactive state first before floating).

While $\overline{RESIN}$ is active, signals $\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$ and $\overline{LOCK}$, are configured as inputs and weakly held high by internal pullup transistors. Forcing $\overline{UCS}$ and $\overline{LCS}$ low selects ONCE Mode. Forcing $\overline{QSMD}$ low selects Queue Status Mode. Forcing $\overline{LOCK}$ low is prohibited and results in unspecified operation.



NOTE:
CLKOUT synchronization occurs approximately 1½ CLKIN periods after RESIN is sampled low.

Figure 14. 80C188EA Powerup Reset

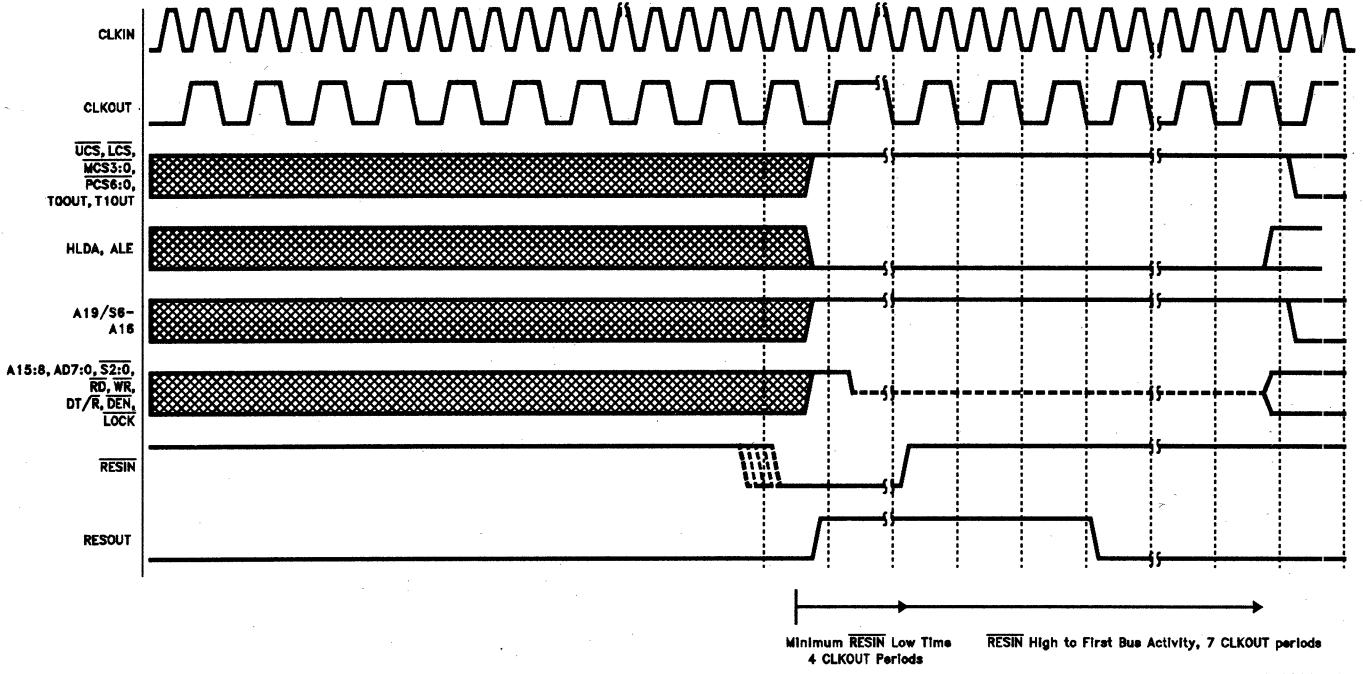
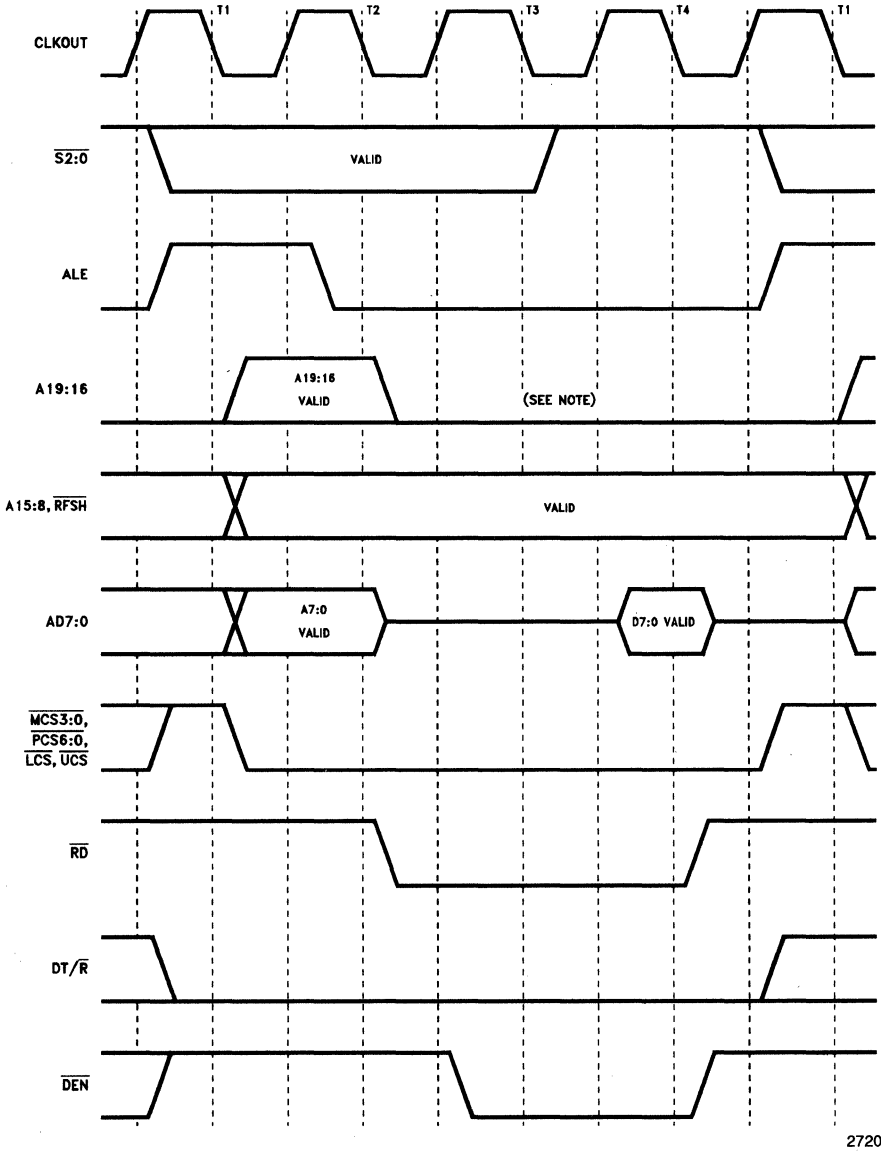


Figure 15. 80C188EA Warm Reset

NOTE:
CLKOUT resynchronization occurs approximately 1½ CLKIN periods after RESIN is sampled low. If RESIN is sampled low while CLKOUT is transitioning high, then CLKOUT will remain high for two CLKIN periods. If RESIN is sampled low while CLKOUT is transitioning high, then CLKOUT will not be affected.

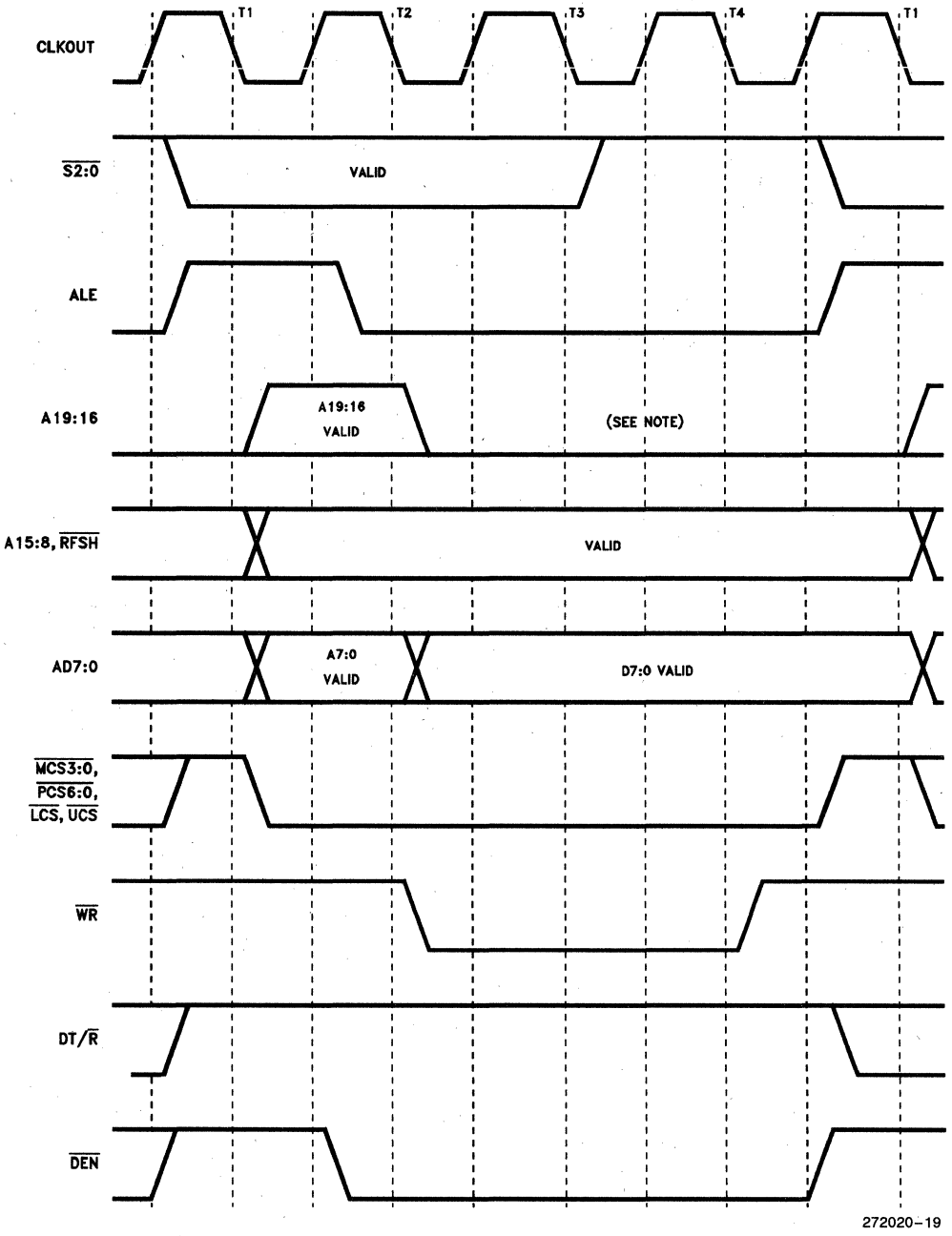
BUS CYCLE WAVEFORMS

Figures 16 through 22 present the various bus cycles that are generated by the 80C188EA. What is shown in the figure is the relationship of the various bus signals to CLKOUT. These figures along with the information present in **AC Specifications** allow the user to determine all the critical timing analysis needed for a given application.



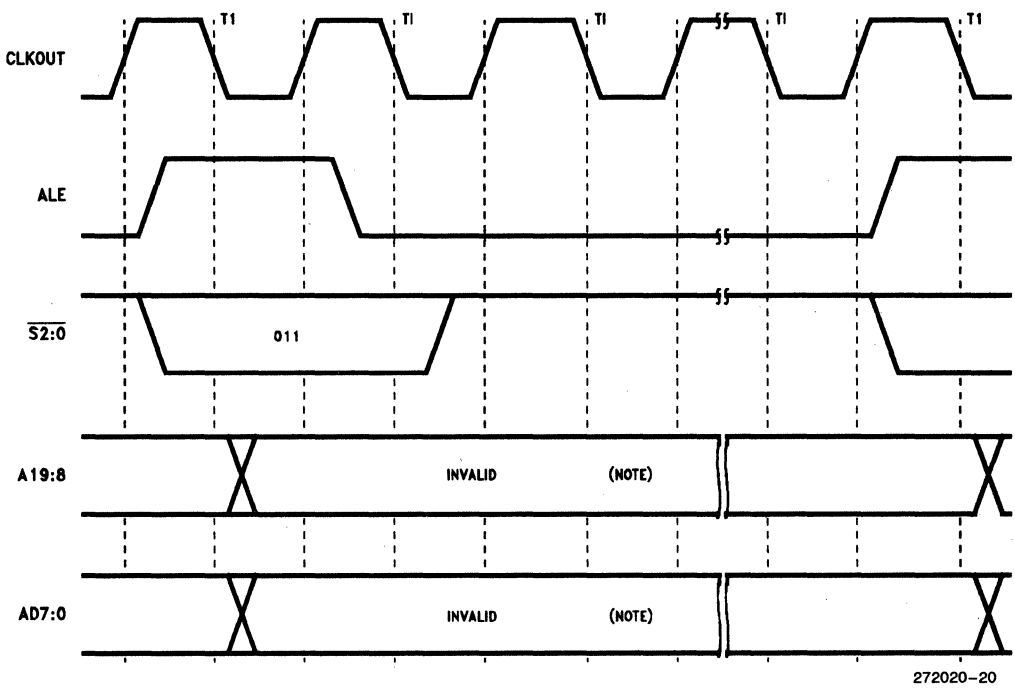
NOTE:
During the data phase of the bus cycle, A19/S6 is driven high for a DMA or refresh cycle.

Figure 16. Read, Fetch and Refresh Cycle Waveform



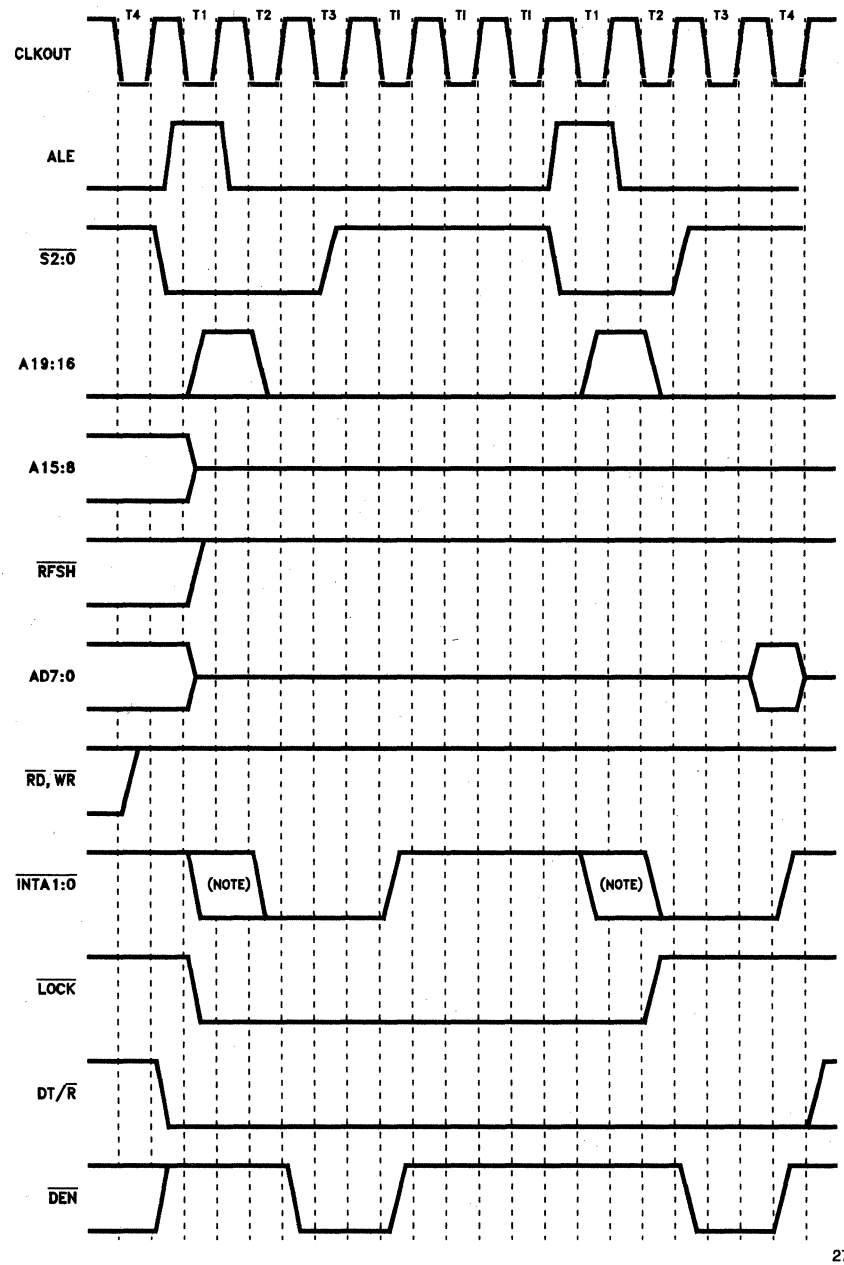
NOTE:
During the data phase of the bus cycle, A19/S6 is driven high for a DMA cycle.

Figure 17. Write Cycle Waveform



NOTE:
The address driven is typically the location of the next instruction prefetch. The 80C188EA drives these pins to 0 during Idle and Powerdown Modes.

Figure 18. Halt Cycle Waveform



NOTE:
INTA occurs one clock later in Slave Mode.

Figure 19. INTA Cycle Waveform

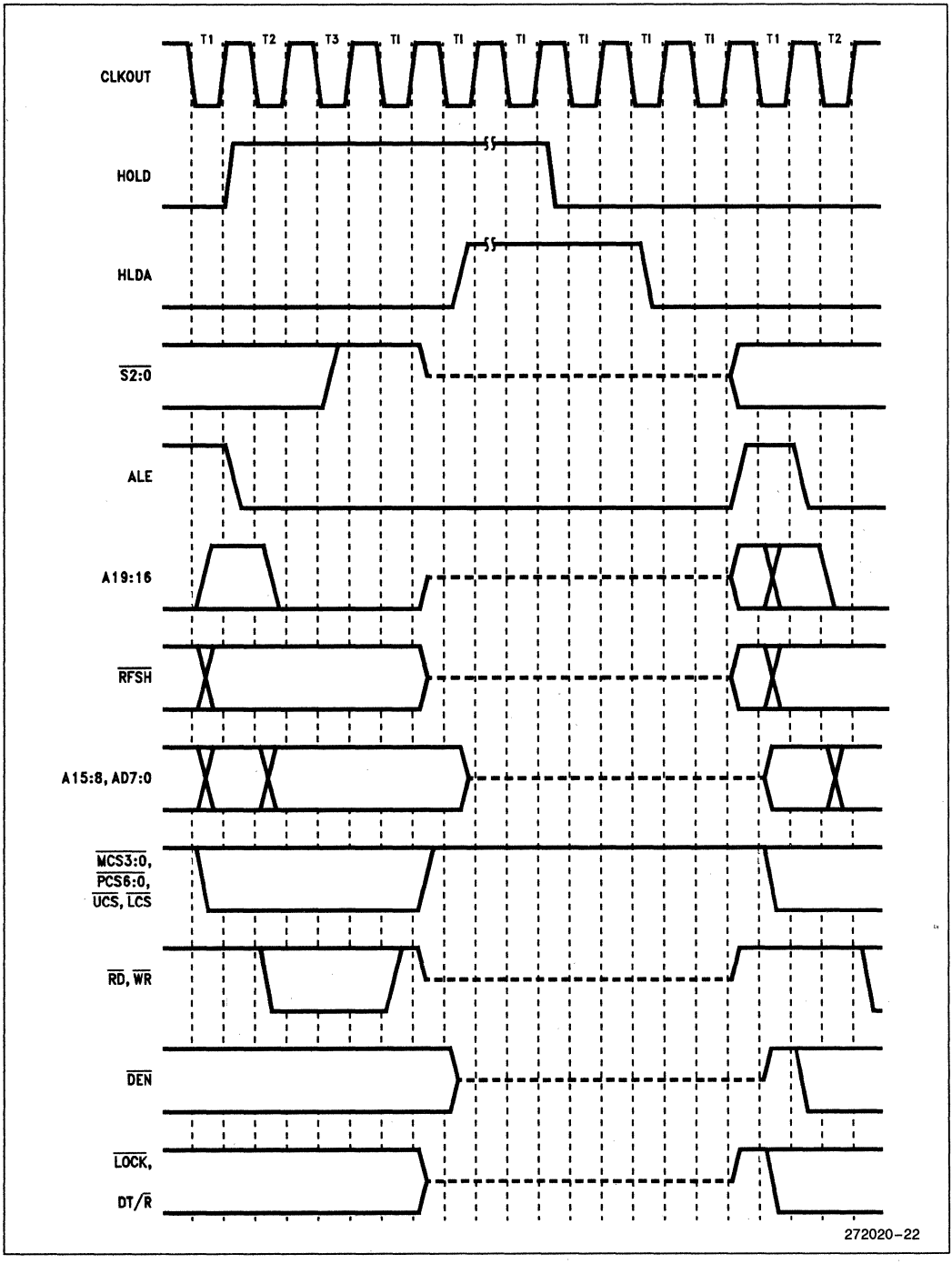


Figure 20. HOLD/HLDA Waveform

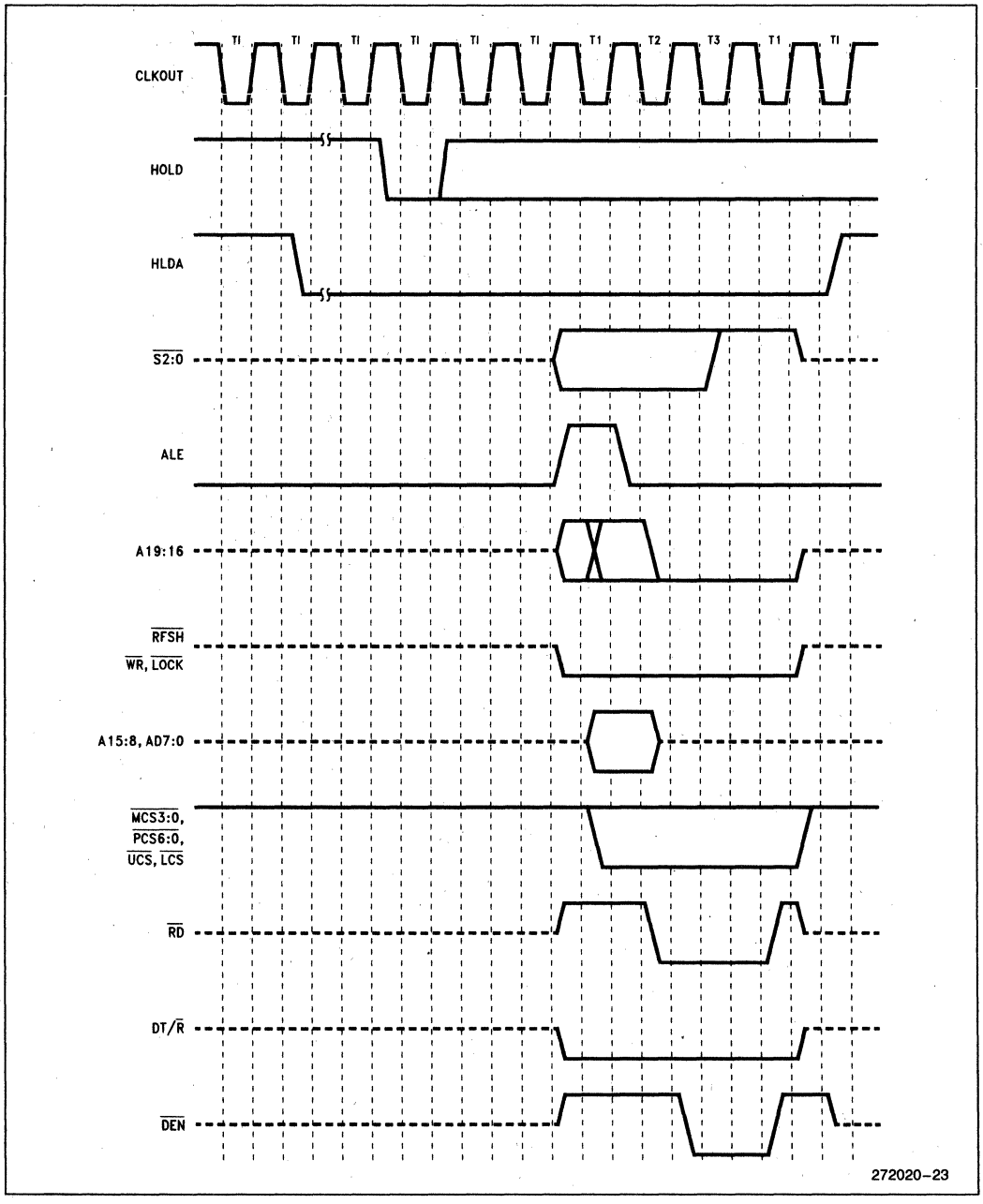
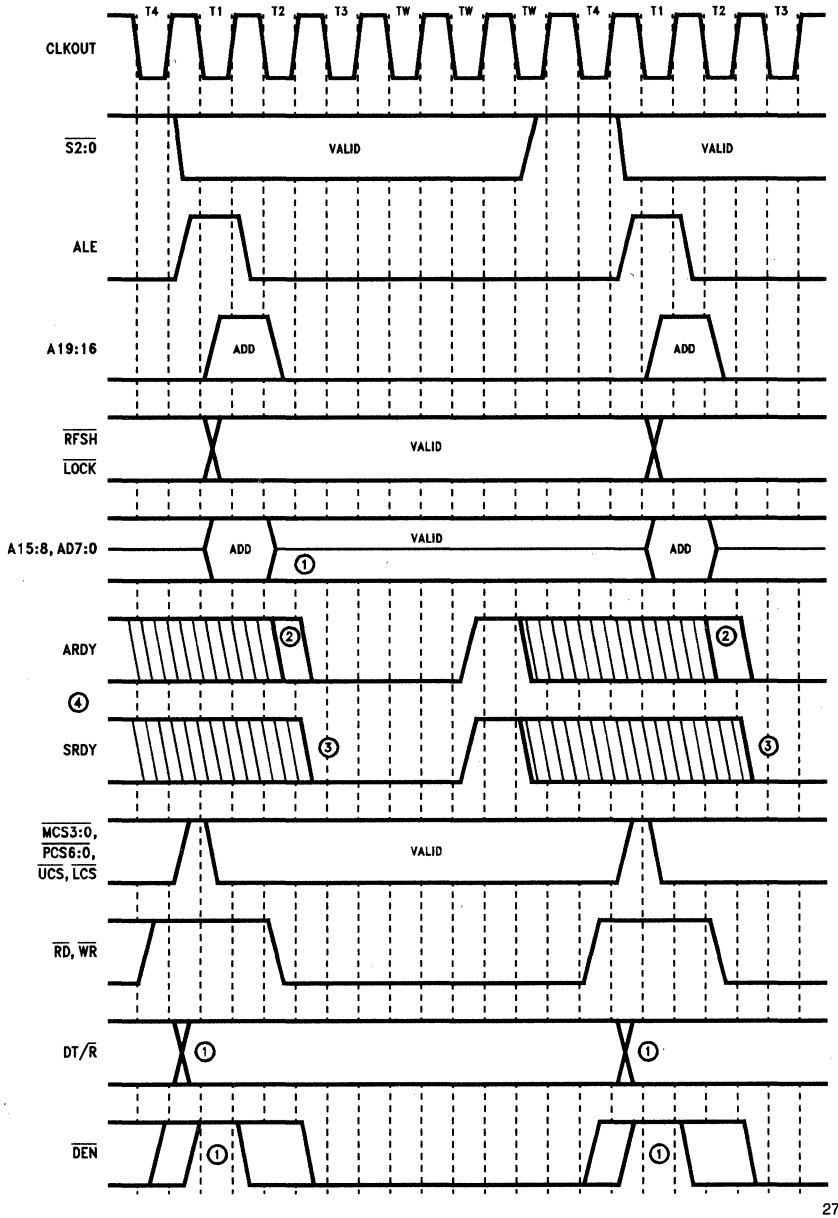


Figure 21. DRAM Refresh Cycle During Hold Acknowledge



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NOTES:
1. Generalized diagram for READ or WRITE.
2. ARDY low by either edge causes a wait state. Only rising ARDY is fully synchronized.
3. SRDY low causes a wait state. SRDY must meet setup and hold times to ensure correct device operation.
4. Either ARDY or SRDY active high will terminate a bus cycle.

Figure 22. Ready Waveform

REGISTER BIT SUMMARY

Figures 23 through 30 present the bit definition of each register that is active (not reserved) in the Peripheral Control Block (PCB). Each register can be thought to occupy one word (16-bits) of either memory or I/O space, although not all bits in the register necessarily have a function. A register bit is **not** guaranteed to return a specific logic value if an "X" appears for the bit definition (i.e., if a zero was written to the register bit it may not be returned as a zero when read). Furthermore, a 0 must be written to any bit that is indicated by an "X" to ensure compatibility with future products or potential product changes.

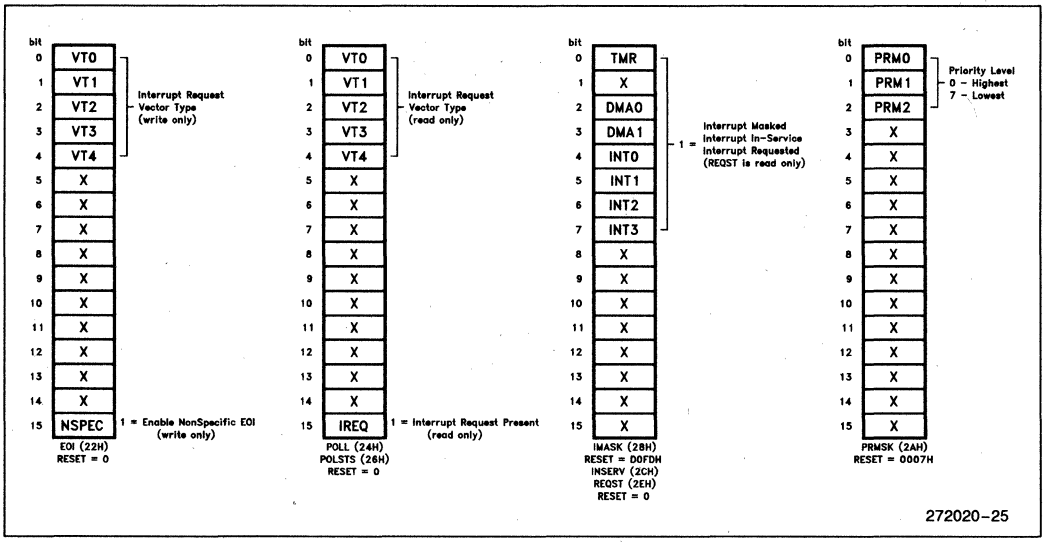

Figure 23. Interrupt Control Unit Registers (Master Mode)

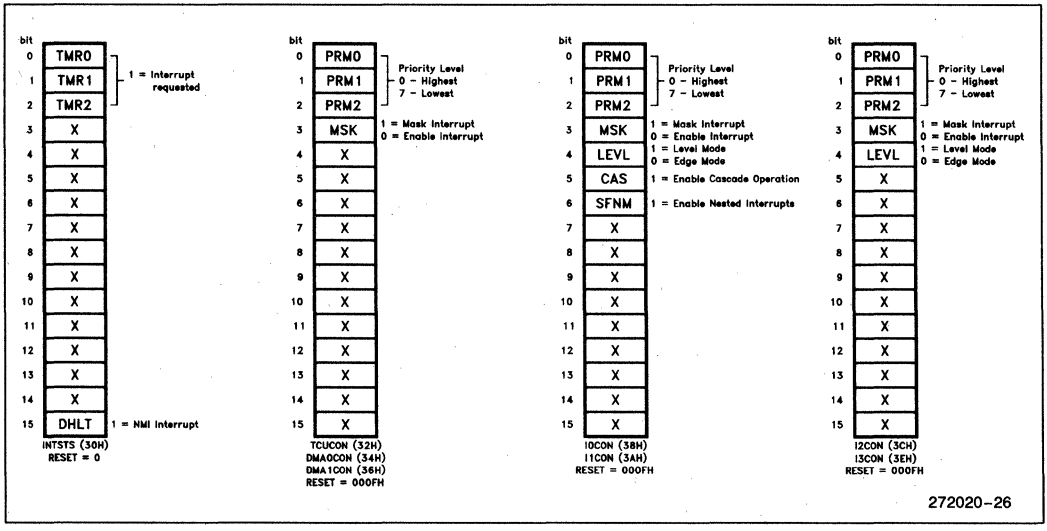

Figure 24. Interrupt Control Unit Registers (Master Mode)

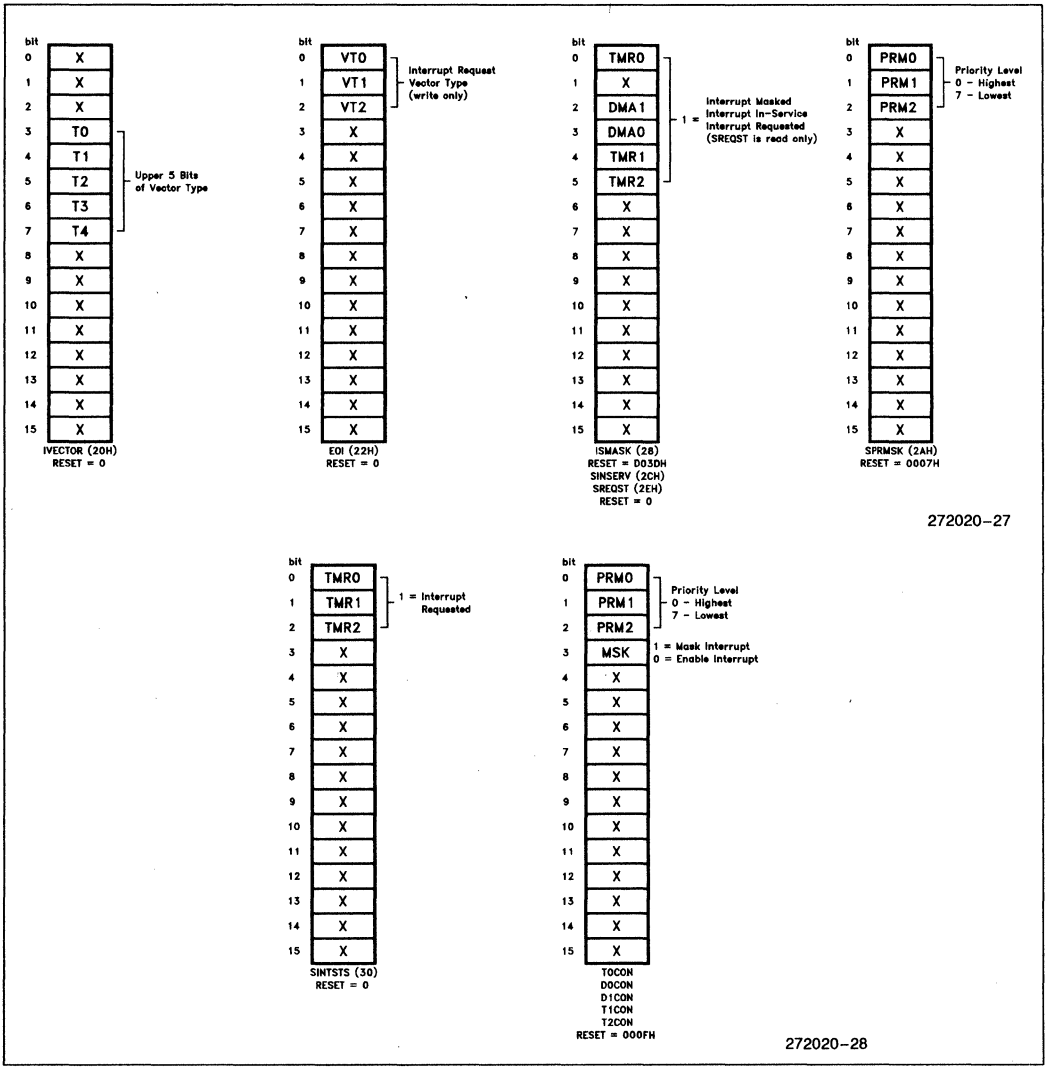

Figure 25. Interrupt Control Unit Registers (Slave Mode)

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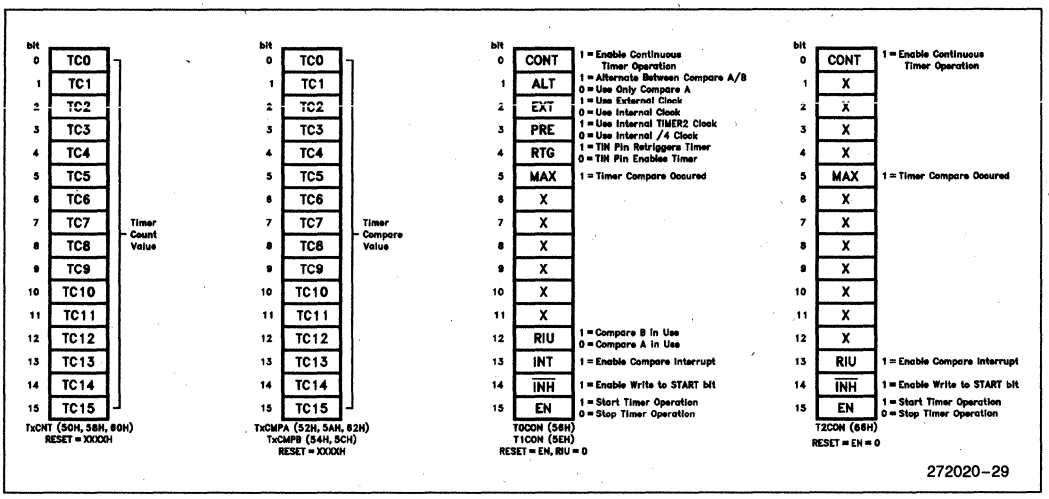

Figure 26. Timer Control Unit Registers

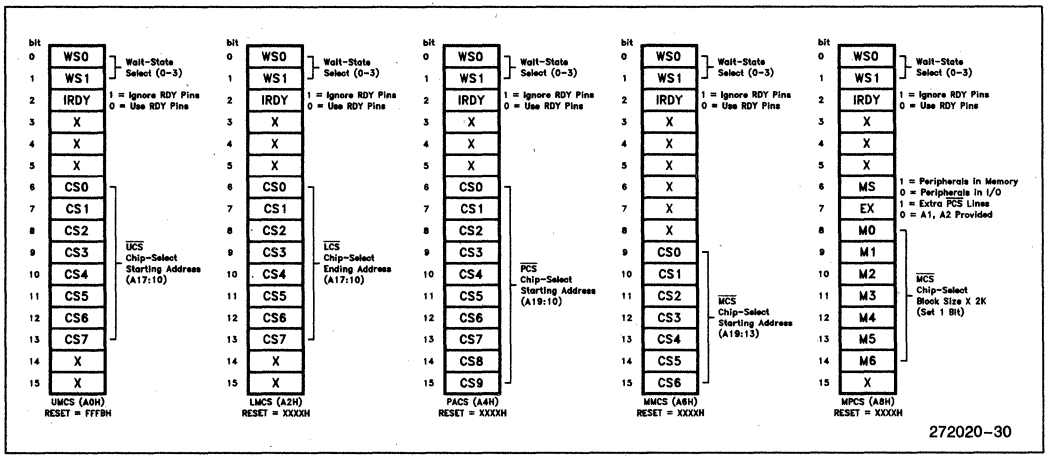

Figure 27. Chip-Select Unit Registers

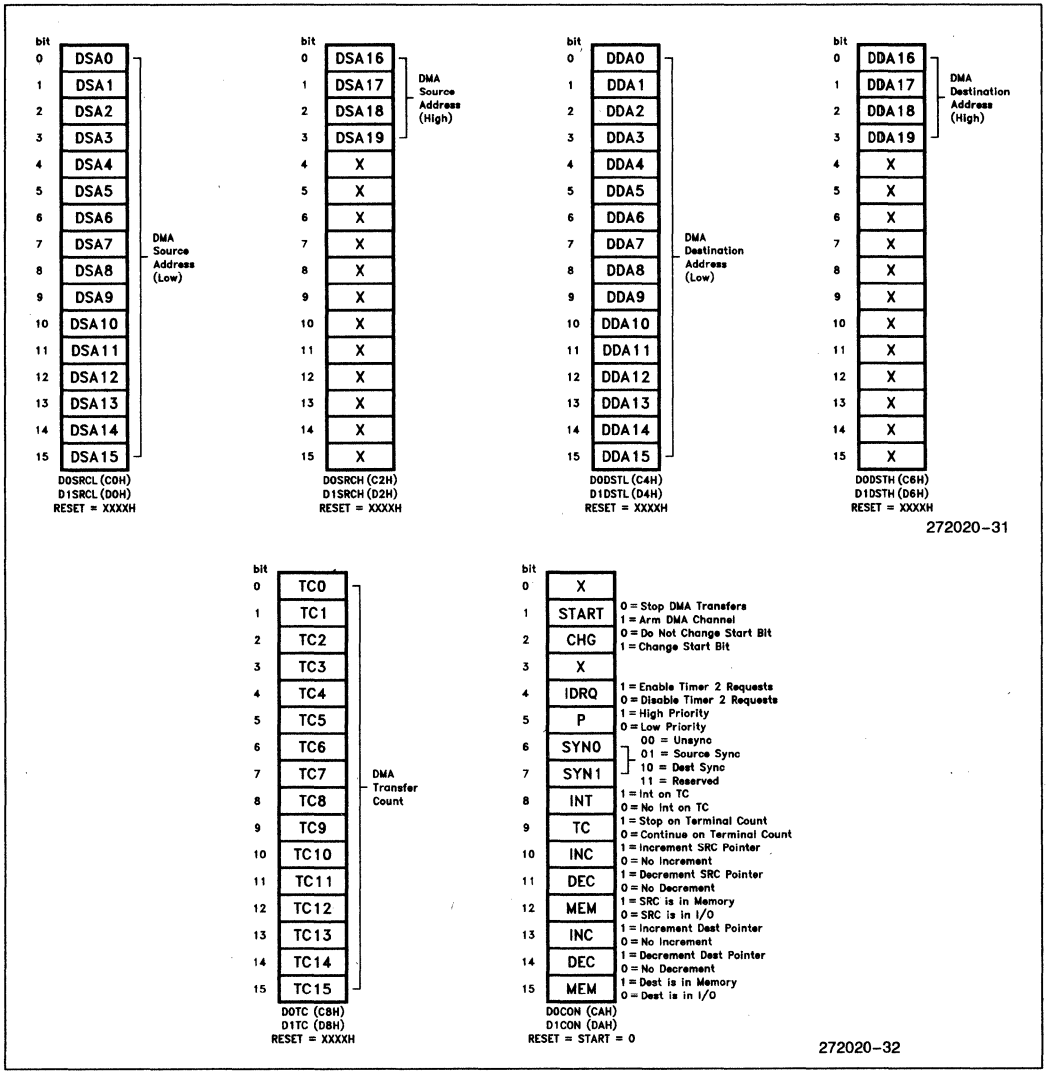

Figure 28. DMA Unit Registers

24

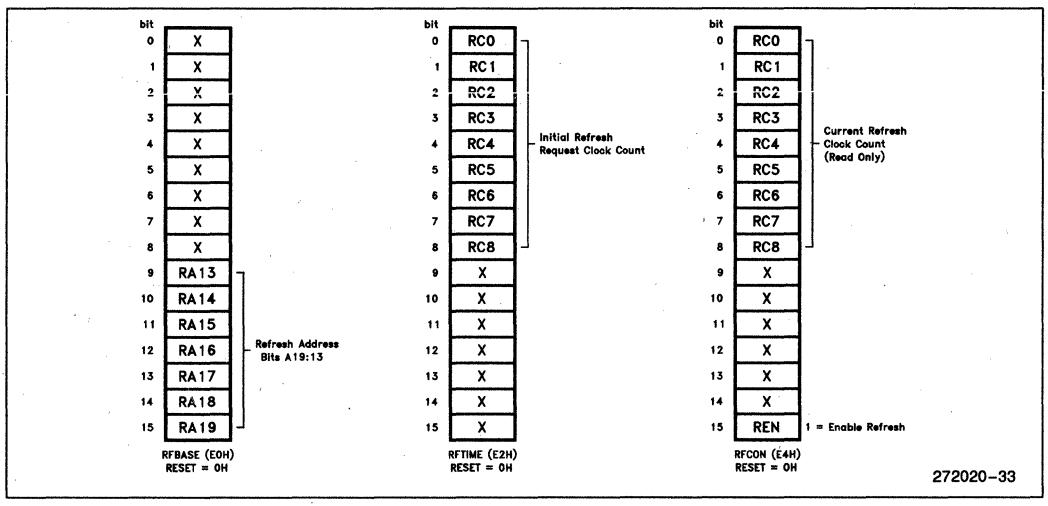

Figure 29. Refresh Control Unit Registers

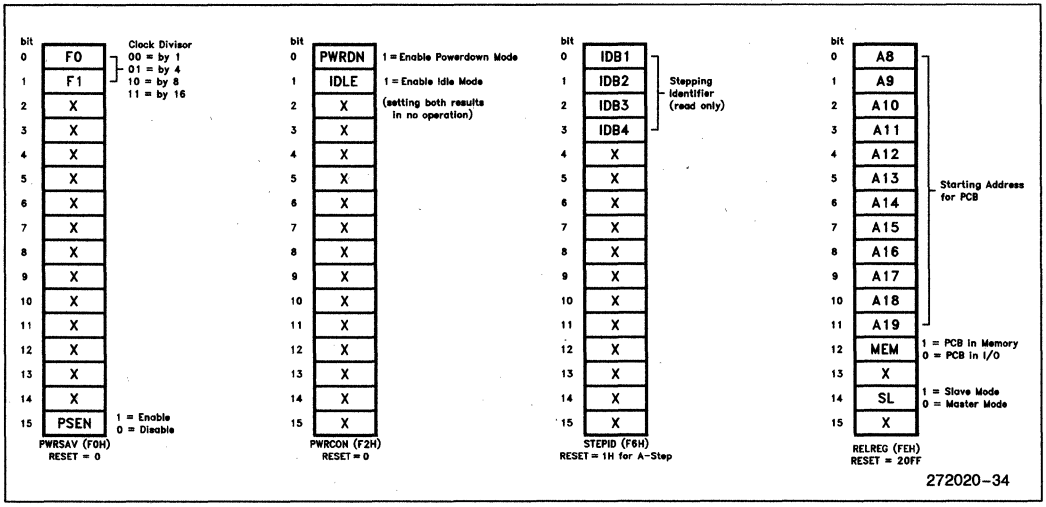

Figure 30. Power Management, Relocation and Stepping Registers

80C188EA EXPRESS

The Intel EXPRESS program offers an extended temperature range as an enhancement to the 80C188EA operational specifications. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the standard commercial temperature range, operational characteristics are guaranteed over a temperature range corresponding to 0°C to +70°C ambient. With the extended temperature range option, operational characteristics are guaranteed over a temperature range corresponding to −40°C to +85°C ambient.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 9. All AC and DC specifications are the same for both commercial and EXPRESS parts.

Table 9. Prefix Identification

Prefix	Package Type	Temperature Range
N	PLCC	Commercial
S	QFP (EIAJ)	Commercial
TN	PLCC	Extended
TS	QFP (EIAJ)	Extended

80C188EA EXECUTION TIMINGS

A determination of 80C188EA program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the **minimum** execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With an 8-bit BIU, the 80C188 may not have sufficient bus performance to ensure that an adequate number of bytes will reside in the queue most of the time. Therefore, actual program execution time will be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1000100w	mod reg r/m			2/12*	
Register/memory to register	1000101w	mod reg r/m			2/9*	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12/13	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3/4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8*	
Accumulator to memory	1010001w	addr-low	addr-high		9*	
Register/memory to segment register	10001110	mod 0 reg r/m			2/13	
Segment register to register/memory	10001100	mod 0 reg r/m			2/15	
PUSH = Push:						
Memory	11111111	mod 110 r/m			20	
Register	01010 reg				14	
Segment register	000reg110				13	
Immediate	011010s0	data	data if s=0		14	
PUSHA = Push All	01100000				68	
POP = Pop:						
Memory	10001111	mod 000 r/m			24	
Register	01011 reg				14	
Segment register	000reg111	(reg≠01)			12	
POPA = Pop All	01100001				83	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17*	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10*	
Variable port	1110110w				8*	
OUT = Output to:						
Fixed port	1110011w	port			9*	
Variable port	1110111w				7*	
XLAT = Translate byte to AL	11010111				15	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		26	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		26	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				13	
POPF = Pop flags	10011101				12	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16*	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16*	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15*	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16*	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16*	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15*	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10*	
Register with register/memory	0011100w	mod reg r/m			3/10*	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10*	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10*	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
ARITHMETIC (Continued)						
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26–28	
Register-Word					35–37	
Memory-Byte					32–34	
Memory-Word					41–43*	
IMUL = Integer multiply (signed):	1111011w	mod 101 r/m				
Register-Byte					25–28	
Register-Word					34–37	
Memory-Byte					31–34	
Memory-Word					40–43*	
IMUL = Integer Immediate multiply (signed)	011010s1	mod reg r/m	data	data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w	mod 110 r/m				
Register-Byte					29	
Register-Word					38	
Memory-Byte					35	
Memory-Word					44*	
IDIV = Integer divide (signed):	1111011w	mod 111 r/m				
Register-Byte					44–52	
Register-Word					53–61	
Memory-Byte					50–58	
Memory-Word					59–67*	
AAM = ASCII adjust for multiply	11010100	00001010			19	
AAD = ASCII adjust for divide	11010101	00001010			15	
CBW = Convert byte to word	10011000				2	
CWD = Convert word to double word	10011001				4	
LOGIC						
Shift/Rotate Instructions:						
Register/Memory by 1	1101000w	mod TTT r/m			2/15	
Register/Memory by CL	1101001w	mod TTT r/m			5+n/17+n	
Register/Memory by Count	1100000w	mod TTT r/m	count		5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR					
AND = **And:**						
Reg/memory and register to either	001000dw	mod reg r/m			3/10*	
Immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0010010w	data	data if w=1		3/4	8/16-bit

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
TEST = And function to flags, no result:						
Register/memory and register	1000010w	mod reg r/m			3/10*	
Immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	4/10*	
Immediate data and accumulator	1010100w	data	data if w=1		3/4	8/16-bit
OR = Or:						
Reg/memory and register to either	000010dw	mod reg r/m			3/10*	
Immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0000110w	data	data if w=1		3/4	8/16-bit
XOR = Exclusive or:						
Reg/memory and register to either	001100dw	mod reg r/m			3/10*	
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0011010w	data	data if w=1		3/4	8/16-bit
NOT = Invert register/memory	1111011w	mod 010 r/m			3/10*	
STRING MANIPULATION						
MOVS = Move byte/word	1010010w				14*	
CMPS = Compare byte/word	1010011w				22*	
SCAS = Scan byte/word	1010111w				15*	
LODS = Load byte/wd to AL/AX	1010110w				12*	
STOS = Store byte/wd from AL/AX	1010101w				10*	
INS = Input byte/wd from DX port	0110110w				14	
OUTS = Output byte/wd to DX port	0110111w				14	
Repeated by count in CX (REP/ REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	11110010	1010010w			8+8n*	
CMPS = Compare string	1111001z	1010011w			5+22n*	
SCAS = Scan string	1111001z	1010111w			5+15n*	
LODS = Load string	11110010	1010110w			6+11n*	
STOS = Store string	11110010	1010101w			6+9n*	
INS = Input string	11110010	0110110w			8+8n*	
OUTS = Output string	11110010	0110111w			8+8n*	
CONTROL TRANSFER						
CALL = Call:						
Direct within segment	11101000	disp-low	disp-high		19	
Register/memory indirect within segment	11111111	mod 010 r/m			17/27	
Direct intersegment	10011010	segment offset			31	
		segment selector				
Indirect intersegment	11111111	mod 011 r/m	(mod ≠ 11)		54	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

***NOTE:**
Clock cycles shown for byte transfer. For word operations, add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
JMP = Unconditional jump:						
Short/long	11101011	disp-low			14	
Direct within segment	11101001	disp-low	disp-high		14	
Register/memory indirect within segment	11111111	mod 100 r/m			11/21	
Direct intersegment	11101010	segment offset			14	
		segment selector				
Indirect intersegment	11111111	mod 101 r/m	(mod ≠ 11)		34	
RET = Return from CALL:						
Within segment	11000011				20	
Within seg adding immed to SP	11000010	data-low	data-high		22	
Intersegment	11001011				30	
Intersegment adding immediate to SP	11001010	data-low	data-high		33	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					19	
L = 1					29	
L > 1					26 + 20(n − 1)	
LEAVE = Leave Procedure	11001001				8	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
CONTROL TRANSFER (Continued)			
INT = **Interrupt:**			
Type specified	11001101 | type	47	
Type 3	11001100	45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110	48/4	
IRET = Interrupt return	11001111	28	
BOUND = Detect value out of range	01100010 | mod reg r/m	33-35	
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

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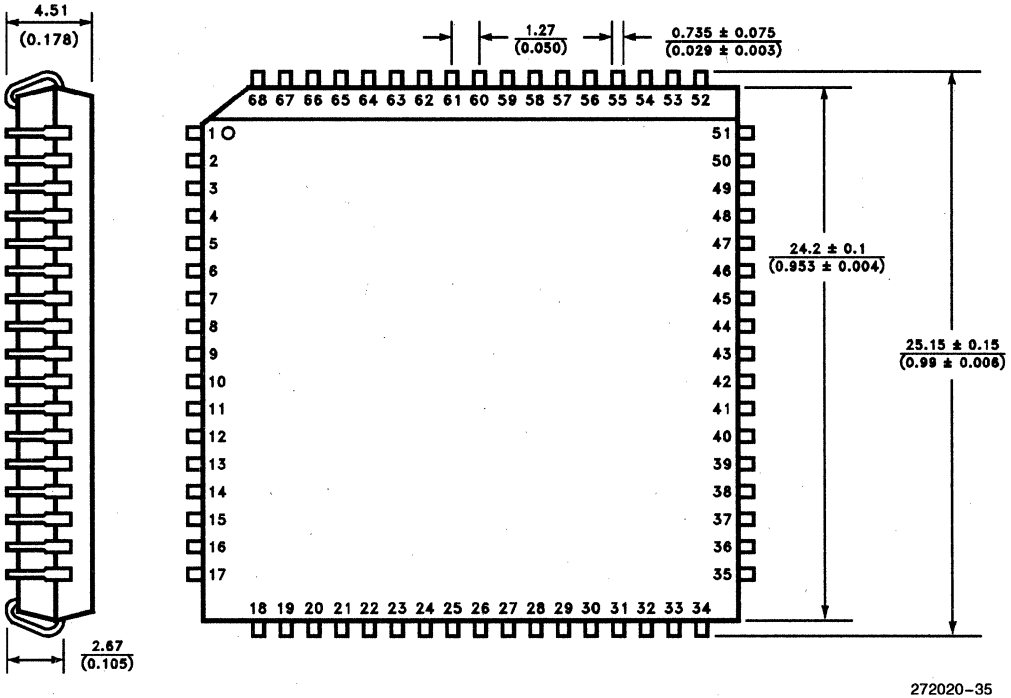
REG is assigned according to the following table:

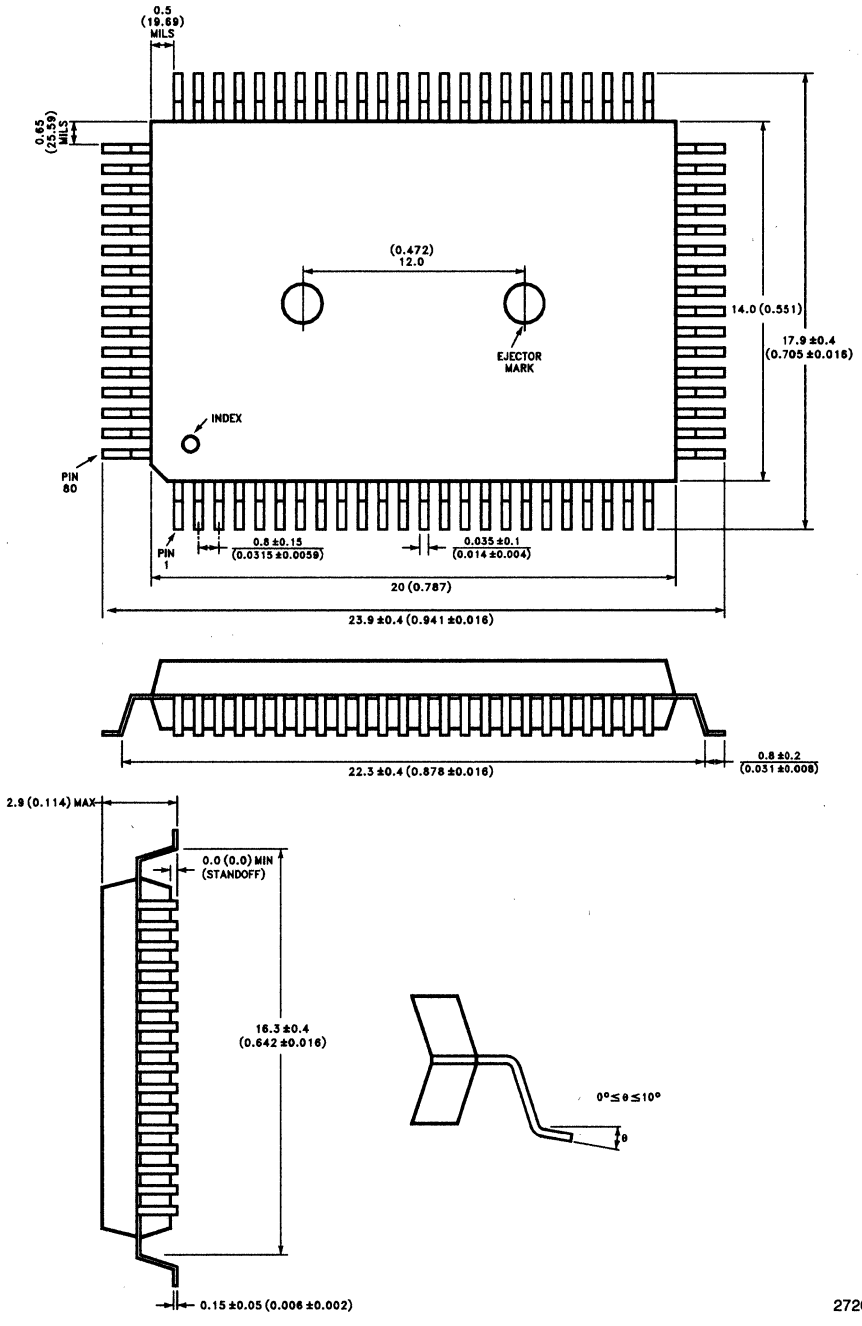
16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.



NOTE:
Units are mm/(inches).

Figure 31. PLCC Principal Dimensions



NOTE:
Units are mm (inches) unless specified.

Figure 32. QFP (EIAJ) Principal Dimensions

REVISION HISTORY

Intel 80C188EA devices are marked with a 9-character alphanumeric Intel FPO number underneath the product number. This data sheet (272020-002) is valid for 80C188EA devices with an "A" or "B" as the ninth character in the FPO number, as illustrated in Figure 5 for the 68-lead PLCC package and Figure 6 for the 84-lead QFP (EIAJ) package. Such devices may also be identified by reading a value of 01H or 02H from the STEPID register.

The following changes were made between the -001 and -002 versions of the 80C188EA data sheets. The -002 data sheet applies to any 80C188EA with a "B" alpha character after the FPO number. The FPO number location is shown in Figures 5 and 6.

1. Much of the information provided in the -001 version of the data sheet has been removed. Detail descriptions of part functionality may be found in the 80C188EA User's Manual.

ERRATA

An 80C188EA with a STEPID value of 01H or 02H has the following known errata. A device with a STEPID of 01H or 02H can be visually identified by noting the presence of an "A" or "B" alpha character, respectively, next to the FPO number. The FPO number location is shown in Figures 5 and 6.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the INTA1 line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistently, it is dependent on interrupt timing.

80C188EB-20, -16, -13, -8
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSOR

- Full Static Operation
- True CMOS Inputs and Outputs
- −40°C to +85°C Operating Temperature Range
- Low System Cost 8-Bit Interface

- **Integrated Feature Set**
  - Low-Power Static CPU Core
  - Two Independent UARTs each with an Integral Baud Rate Generator
  - Two 8-Bit Multiplexed I/O Ports
  - Programmable Interrupt Controller
  - Three Programmable 16-Bit Timer/Counters
  - Clock Generator
  - Ten Programmable Chip Selects with Integral Wait-State Generator
  - Memory Refresh Control Unit
  - System Level Testing Support (ONCE™ Mode)
- **Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O**
- **Speed Versions Available:**
  - 20 MHz (80C188EB-20)
  - 16 MHz (80C188EB-16)
  - 13 MHz (80C188EB-13)
  - 8 MHz (80C188EB-8)
- **Low-Power Operating Modes:**
  - Idle Mode Freezes CPU Clocks but keeps Peripherals Active
  - Powerdown Mode Freezes All Internal Clocks
- **Complete System Development Support**
  - ASM86 Assembler, PL/M 86, Pascal 86, Fortran 86, C-86, and System Utilities
  - In-Circuit Emulator (ICE™-188EB)
- **Available In:**
  - 80-Pin Quad Flat Pack (TS80C188EB)
  - 84-Pin Plastic Leaded Chip Carrier (TN80C188EB)

The 80C188EB is a second generation CHMOS High-Integration microprocessor. It has features that are new to the 80C188 family and include a STATIC CPU core, an enhanced Chip Select decode unit, two independent Serial Channels, I/O ports, and the capability of Idle or Powerdown low power modes.

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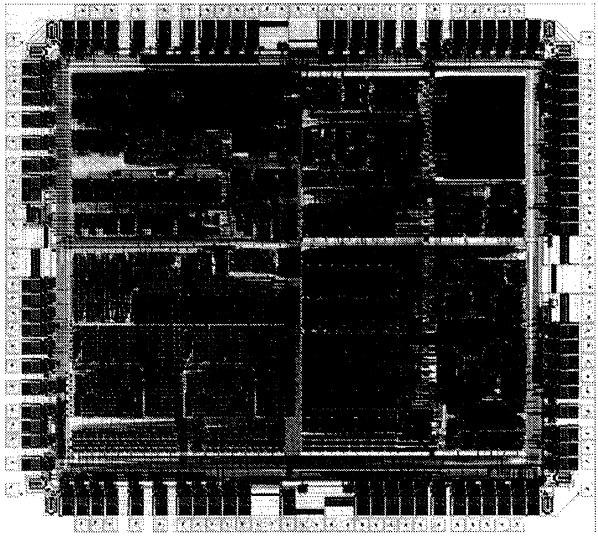

270885-36

May 1992
Order Number: 270885-003

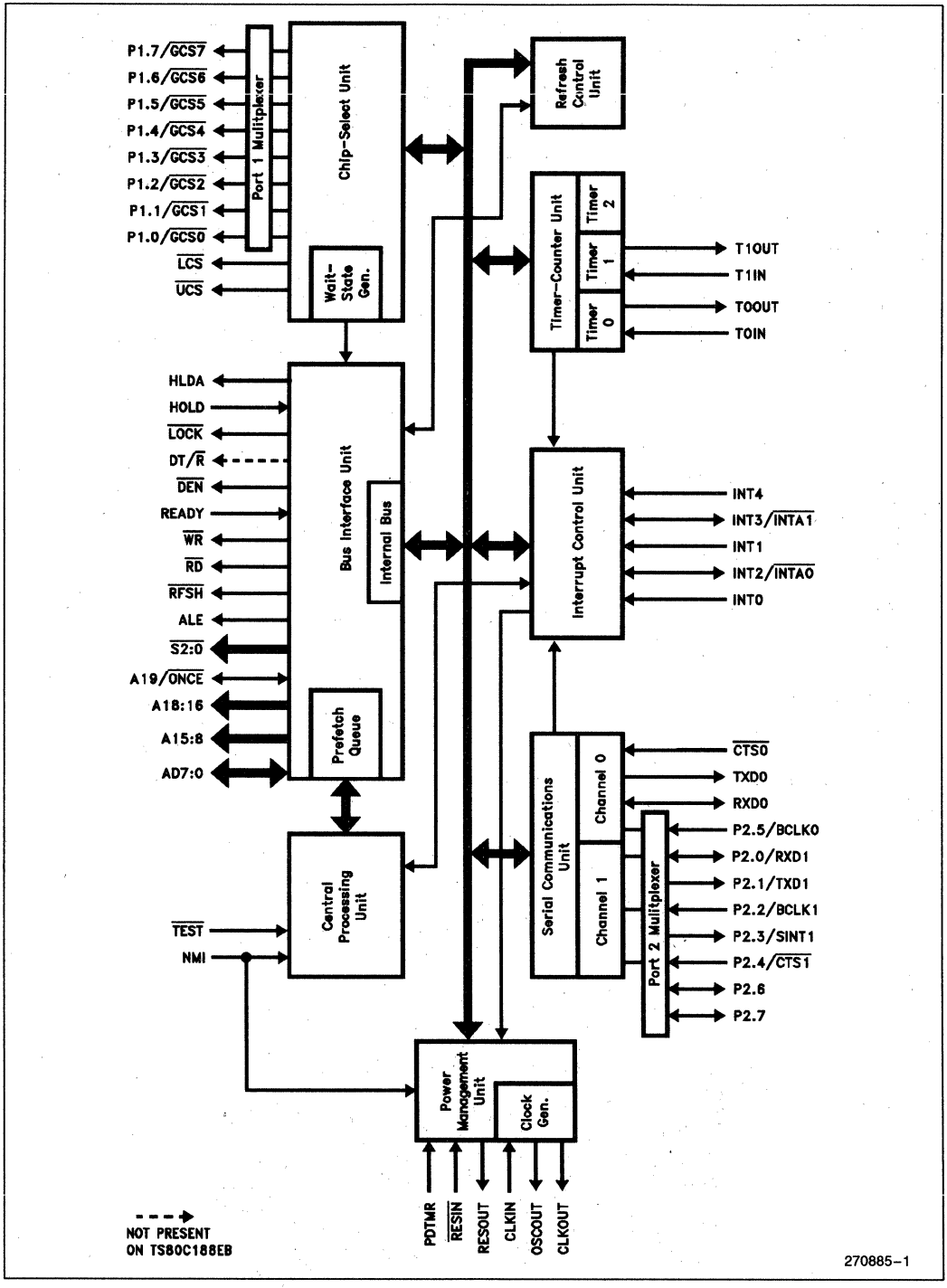

Figure 1. 80C188EB Block Diagram

INTRODUCTION

The 80C188EB is the first product in a new generation of low-power, high-integration microprocessors. It enhances the existing 186 family by offering new features and new operating modes. The 80C188EB is object code compatible with the 80C186/80C188 microprocessors. The 80C188EB has an 8-bit external data bus but still retains a 16-bit internal bus. An 8-bit external bus reduces system cost by requiring that only single byte-wide memories be used.

The feature set of the 80C188EB meets the needs of low power, space critical applications. Low-Power applications benefit from the static design of the CPU core and the integrated peripherals. Minimum current consumption is achieved by providing a Powerdown mode that halts operation of the device, and freezes the clock circuits. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space critical applications benefit from the integration of commonly used system peripherals. Two serial channels are provided for services such as diagnostics, inter-processor communication, modem interface, terminal display interface, and many others. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 129 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters and sixteen multiplexed I/O port pins round out the feature set of the 80C188EB.

OVERVIEW

Figure 1 shows a block diagram of the 80C188EB. The Execution Unit (EU) is an enhanced 8088 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instruction, and full static operation. The Bus Interface Unit (BIU) is the same as that found on the original 188 family products, except the queue-status mode has been deleted and buffer interface control has been changed to ease system design timings. An independent internal bus is used to allow communication between the BIU and internal peripherals.

BUS INTERFACE UNIT

The 80C188EB core incorporates a bus controller that generates local bus control signals. In addition, it employs a HOLD/HLDA protocol to share the local bus with other bus masters.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information, and data (for write operations) information. It is also responsible for reading data off the local bus during a read operation. A READY input pin is provided to extend a bus cycle beyond the minimum four states (clocks).

The 80C188EB local bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. (Both $\overline{DEN}$ and DT/$\overline{R}$ are available on the TN80C188EB device, only $\overline{DEN}$ is available on the TS80C188EB device.) This capability allows the addition of transceivers for simple buffering of the mulitplexed address/data bus.

CLOCK GENERATOR

The 80C188EB provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, and two low-power operating modes.

The oscillator circuit is designed to be used with either a **parallel resonant** fundamental or third-overtone mode crystal network. Alternatively, the oscillator circuit may be driven from an external clock source. Figure 2 shows the various operating modes of the 80C188EB oscillator circuit.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide-by-two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.

The following parameters are recommended when choosing a crystal:

Temperature Range:	Application Specific
ESR (Equivalent Series Resistance):	40Ω max
C0 (Shunt Capacitance of Crystal):	7.0 pF max
C_L (Load Capacitance):	20 pF ± 2 pF
Drive Level:	1 mW max

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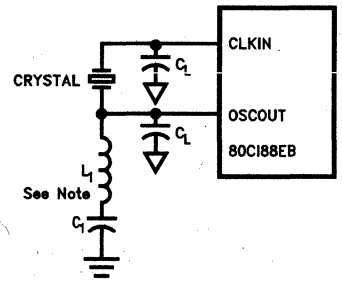
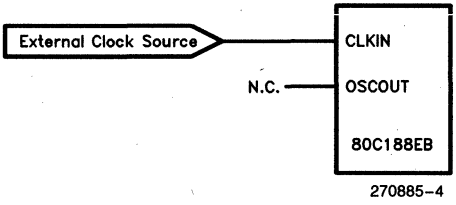


270885-3

(A) Crystal Connection



270885-4

(B) Clock Connection

NOTE:
The L_1C_1 network is **only** required when using a third-overtone crystal.

Figure 2. 80C188EB Clock Configurations

80C188EB Peripheral Architecture

The 80C188EB has integrated several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexible and provide logical interconnections between supporting units (e.g., the interrupt control unit supports interrupt requests from the timer/counters or serial channels).

The list of integrated peripherals includes:

- 7-Input Interrupt Control Unit
- 3-Channel Timer/Counter Unit
- 2-Channel Serial Communications Unit
- 10-Output Chip-Select Unit
- I/O Port Unit
- Refresh Control Unit
- Power Management Unit

The registers associated with each integrated peripheral are contained within a 128 x 16 register file called the Peripheral Control Block (PCB). The PCB can be located in either memory or I/O space on any 256 Byte address boundary.

The starting address of the PCB is controlled by a relocation register and can overlap any of the memory or I/O regions programmed into the Chip Select Unit. In this case, the overlapped chip select will not go active when the PCB is read or written.

Figure 3 provides a list of the registers associated with the PCB. The Register Bit Summary at the end of this specification individually lists all of the registers and identifies each of their programming attributes.

INTERRUPT CONTROL UNIT

The 80C188EB can receive interrupts from a number of sources, both internal and external. The interrupt control unit serves to merge these requests, on a priority basis, for individual service by the CPU. Each interrupt source can be independently masked by the Interrupt Control Unit (ICU) or all interrupts can be globally masked by the CPU.

Internal interrupt sources include the Timers and Serial channel 0. External interrupt sources come from the five input pins INT4:0. The NMI interrupt pin is not controlled by the ICU and is passed directly to the CPU. Although the Timer and Serial channel each have only one request input to the ICU, separate vector types are generated to service individual interrupts within the Timer and Serial channel units.

TIMER/COUNTER UNIT

The 80C188EB Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms, generate timed interrupts. etc.

PCB Offset	Function
00H	Reserved
02H	End Of Interrupt
04H	Poll
06H	Poll Status
08H	Interrupt Mask
0AH	Priority Mask
0CH	In-Service
0EH	Interrupt Request
10H	Interrupt Status
12H	Timer Control
14H	Serial Control
16H	INT4
18H	INT0 Control
1AH	INT1 Control
1CH	INT2 Control
1EH	INT3 Control
20H	Reserved
22H	Reserved
24H	Reserved
26H	Reserved
28H	Reserved
2AH	Reserved
2CH	Reserved
2EH	Reserved
30H	Timer0 Count
32H	Timer0 Compare A
34H	Timer0 Compare B
36H	Timer0 Control
38H	Timer1 Count
3AH	Timer1 Compare A
3CH	Timer1 Compare B
3EH	Timer1 Control

PCB Offset	Function
40H	Timer2 Count
42H	Timer2 Compare
44H	Reserved
46H	Timer2 Control
48H	Reserved
4AH	Reserved
4CH	Reserved
4EH	Reserved
50H	Reserved
52H	Port0 Pin
54H	Port0 Control
56H	Port0 Latch
58H	Port1 Direction
5AH	Port1 Pin
5CH	Port1 Control
5EH	Port1 Latch
60H	Serial0 Baud
62H	Serial0 Count
64H	Serial0 Control
66H	Serial0 Status
68H	Serial0 RBUF
6AH	Serial0 TBUF
6CH	Reserved
6EH	Reserved
70H	Serial1 Baud
72H	Serial1 Count
74H	Serial1 Control
76H	Serial1 Status
78H	Serial1 RBUF
7AH	Serial1 TBUF
7CH	Reserved
7EH	Reserved

PCB Offset	Function
80H	GCS0 Start
82H	GCS0 Stop
84H	GCS1 Start
86H	GCS1 Stop
88H	GCS2 Start
8AH	GCS2 Stop
8CH	GCS3 Start
8EH	GCS3 Stop
90H	GCS4 Start
92H	GCS4 Stop
94H	GCS5 Start
96H	GCS5 Stop
98H	GCS6 Start
9AH	GCS6 Stop
9CH	GCS7 Start
9EH	GCS7 Stop
A0H	LCS Start
A2H	LCS Stop
A4H	UCS Start
A6H	UCS Stop
A8H	Relocation
AAH	Reserved
ACH	Reserved
AEH	Reserved
B0H	Refresh Base
B2H	Refresh Time
B4H	Refresh Control
B6H	Refresh Address
B8H	Power Control
BAH	Reserved
BCH	Step ID
BEH	Reserved

PCB Offset	Function
C0H	Reserved
C2H	Reserved
C4H	Reserved
C6H	Reserved
C8H	Reserved
CAH	Reserved
CCH	Reserved
CEH	Reserved
D0H	Reserved
D2H	Reserved
D4H	Reserved
D6H	Reserved
D8H	Reserved
DAH	Reserved
DCH	Reserved
DEH	Reserved
E0H	Reserved
E2H	Reserved
E4H	Reserved
E6H	Reserved
E8H	Reserved
EAH	Reserved
ECH	Reserved
EEH	Reserved
F0H	Reserved
F2H	Reserved
F4H	Reserved
F6H	Reserved
F8H	Reserved
FAH	Reserved
FCH	Reserved
FEH	Reserved

Figure 3. 80C188EB Peripheral Control Block Registers

SERIAL COMMUNICATIONS UNIT

The Serial Control Unit (SCU) of the 80C188EB contains two independent channels. Each channel is identical in operation except that only channel 0 is supported by the integrated interrupt controller (channel 1 has an external interrupt pin). Each channel has its own baud rate generator that is independent of the Timer/Counter Unit, and can be internally or externally clocked up at one half the 80C188EB operating frequency.

Independent baud rate generators are provided for each of the serial channels. For the asynchronous modes, the generator supplies an 8x baud clock to both the receive and transmit register logic. A 1x baud clock is provided in the synchronous mode.

CHIP-SELECT UNIT

The 80C188EB Chip-Select Unit (CSU) integrates logic which provides up to ten programmable chip-selects to access both memories and peripherals. In addition, each chip-select can be programmed to automatically insert additional clocks (wait-states) into the current bus cycle and automatically terminate a bus cycle independent of the condition of the READY input pin.

I/O PORT UNIT

The I/O Port Unit (IPU) on the 80C188EB supports two 8-bit channels of input, output, or input/output operation. Port 1 is multiplexed with the chip select pins and is output only. Most of Port 2 is multiplexed with the serial channel pins. Port 2 pins are limited to either an output or input function depending on the operation of the serial pin it is multiplexed with.

REFRESH CONTROL UNIT

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests.

A 12-bit address generator is maintained by the RCU and is presented on the A12:1 address lines during the refresh bus cycle. Address bits A19:13 are programmable to allow the refresh address block to be located on any 8 Kbyte boundary.

POWER MANAGEMENT UNIT

The 80C188EB Power Management Unit (PMU) is provided to control the power consumption of the device. The PMU provides three power modes: Active, Idle, and Powerdown.

Active Mode indicates that all units on the 80C188EB are functional and the device consumes maximum power (depending on the level of peripheral operation). Idle Mode freezes the clocks of the Execution and Bus units at a logic zero state (all peripherals continue to operate normally).

The Powerdown mode freezes all internal clocks at a logic zero level and disables the crystal oscillator. All internal registers hold their values provided V_{CC} is maintained. Current consumption is reduced to just transistor junction leakage.

ONCE™ Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C188EB has a test mode available which forces all output and input/output pins to be placed in the high-impedance state. ONCE stands for "ON Circuit Emulation". The ONCE mode is selected by forcing the A19/$\overline{ONCE}$ pin LOW (0) during a processor reset (this pin is weakly held to a HIGH (1) level while $\overline{RESIN}$ is active).

PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the 80C188EB in the Plastic Leaded Chip Carrier (PLCC) package and Quad Flat Pack (QFP) package. For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

Pin Descriptions

The 80C188EB pins are described in this section. Table 1 presents the legend for interpreting the pin descriptions in Table 2. Figure 4 provides an example pin description entry. The "I/O" signifies that the pins are bidirectional (i.e., have both an input and output function). The "S" indicates that, as an input, the signal is synchronized to CLKOUT for proper operation. The "H(Z)" indicates that these pins will float while the processor is in the Hold Acknowledge state. R(Z) indicates that these pins will float while $\overline{\text{RESIN}}$ is low. P(X) Indicates that these pins will retain their current value when Idle or Powerdown Modes are entered.

All pins float while the processor is in the ONCE™ Mode, except OSCOUT (OSCOUT is required for crystal operation).

Name	Type	Description
AD7:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed ADDRESS and DATA bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8-bit data information are transferred during the data phase of the bus cycle.

Figure 4. Example Pin Description Entry

Table 1. Pin Description Nomenclature

Symbol	Description
I	Input Only Pin
O	Output Only Pin
I/O	Pin can be either input or output
—	Pin "must be" connected as described
S(..)	Synchronous. Input must meet setup and hold times for proper operation of the processor. The pin is: S(E) edge sensitive S(L) level sensitive
A(..)	Asynchronous. Input must meet setup and hold only to guarantee recognition. The pin is: A(E) edge sensitive A(L) level sensitive
H(..)	While the processor's bus is in the Hold Acknowledge state, the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Z) floats H(Q) remains active H(X) retains current state
R(..)	While the processor's $\overline{\text{RES}}$ line is low, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Z) floats R(WH) weak pullup R(WL) weak pulldown
P(..)	While Idle or Powerdown modes are active, the pin: P(1) is driven to V_{CC} P(0) is driven to V_{SS} P(Z) floats P(Q) remains active(1) P(X) retains current state

NOTE:
1. Any pin that specifies P(Q) are valid for Idle Mode. All pins are P(X) for Powerdown Mode.

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Table 2. 80C188EB Pin Descriptions

Name	Type	Description
V_{CC}		**POWER** connections consist of four pins which must be shorted externally to a V_{CC} board plane.
V_{SS}		**GROUND** connections consist of six pins which must be shorted externally to a V_{SS} board plane.
CLKIN	I A(E)	**CLocK INput** is an input for an external clock. An external oscillator operating at two times the required 80C188EB operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O H(Q) R(Q) P(Q)	**OSCillator OUTput** is only used when using a crystal to generate the external clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin is not to be used as 2X clock output for non-crystal applications (i.e., this pin is N.C. for non-crystal applications). OSCOUT does not float in ONCE mode.
CLKOUT	O H(Q) R(Q) P(Q)	**CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transistions every falling edge of CLKIN.
$\overline{\text{RESIN}}$	I A(L)	**RESet IN** causes the 80C188EB to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the 80C188EB begins fetching opcodes at memory location 0FFFF0H.
RESOUT	O H(0) R(1) P(0)	**RESet OUTput** that indicates the 80C188EB is currently in the reset state. RESOUT will remain active as long as $\overline{\text{RESIN}}$ remains active.
PDTMR	I/O A(L) H(WH) R(Z) P(1)	**Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the 80C188EB waits after an exit from power down before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I A(E)	**Non-Maskable Interrupt** input causes a TYPE-2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{\text{TEST}}$	I A(E)	**TEST** is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (LOW).
AD7:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed **Address** and **Data** bus. During the address phase of the bus cycle, address bits 0 through 7 are presented on the bus and can be latched using ALE. 8-bit data information is transferred during the data phase of the bus cycle.
A15:8	O H(Z) R(Z) P(X)	These pins provide **Address** information throughout the entire bus cycle.

Table 2. 80C188EB Pin Descriptions (Continued)

Name	Type	Description
A18:16 A19/$\overline{ONCE}$	I/O H(Z) R(W1) P(X)	These pins provide multiplexed ADDRESS during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. These pins are driven to a logic 0 during the data phase of the bus cycle. During a processor reset ($\overline{RESIN}$ active), A19/$\overline{ONCE}$ is used to enable ONCE mode. A18:16 must not be driven low during reset or improper 80C188EB operation may result.
$\overline{S2:0}$	O H(Z) R(Z) P(1)	Bus cycle **Status** are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ Bus Cycle Initiated 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive (no bus activity)
ALE	O H(0) R(0) P(0)	**Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle.
$\overline{RFSH}$	O H(Z) R(Z) P(1)	**ReFreSH** output signals that a refresh bus cycle is in progress.
$\overline{RD}$	O H(Z) R(Z) P(1)	**ReaD** output signals that the accessed memory or I/O device must drive data information onto the data bus.
$\overline{WR}$	O H(Z) R(Z) P(1)	**WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device.
READY	I A(L) S(L)	**READY** input to signal the completion of a bus cycle. READY must be active to terminate any 80C188EB bus cycle, unless it is ignored by correctly programming the Chip-Select Unit.
$\overline{DEN}$	O H(Z) R(Z) P(1)	**Data ENable** output to control the enable of bi-directional transceivers when buffering a 80C188EB system. $\overline{DEN}$ is active only when data is to be transferred on the bus.

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Table 2. 80C188EB Pin Descriptions (Continued)

Name	Type	Description
DT/$\overline{R}$	O H(Z) R(Z) P(X)	**Data Transmit/Receive** output controls the direction of a bi-directional buffer when buffering an 80C188EB system. DT/$\overline{R}$ is only available for the PLCC package (TN80C188EB).
$\overline{LOCK}$	I/O H(Z) R(W1) P(1)	**LOCK** output indicates that the bus cycle in progress is not to be interrupted. The 80C188EB will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low.
HOLD	I A(L)	**HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The 80C188EB will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
HLDA	O H(1) R(0) P(0)	**HoLD Acknowledge** output to indicate that the 80C188EB has relinquish control of the local bus. When HLDA is asserted, the 80C188EB will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly.
$\overline{UCS}$	O H(1) R(1) P(1)	**Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH.
$\overline{LCS}$	O H(1) R(1) P(1)	**Lower Chip Select** will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. $\overline{LCS}$ is inactive after a reset.
P1.0/$\overline{GCS0}$ P1.1/$\overline{GCS1}$ P1.2/$\overline{GCS2}$ P1.3/$\overline{GCS3}$ P1.4/$\overline{GCS4}$ P1.5/$\overline{GCS5}$ P1.6/$\overline{GCS6}$ P1.7/$\overline{GCS7}$	O H(X)/H(1) R(1) P(X)/P(1)	These pins provide a multiplexed function. If enabled, each pin can provide a **Generic Chip Select** output which will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. When not programmed as a Chip-Select, each pin may be used as a general purpose output **Port.** As an output port pin, the value of the pin can be read internally.
T0OUT T1OUT	O H(Q) R(1) P(Q)	**Timer OUTput** pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.
T0IN T1IN	I A(L) A(E)	**Timer INput** is used either as clock or control signals, depending on the timer mode selected.

Table 2. 80C188EB Pin Descriptions (Continued)

Name	Type	Description
INT0 INT1 INT4	I A(E,L)	Maskable **INTerrupt** input will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with $\overline{\text{INTA0}}$ and $\overline{\text{INTA1}}$ to interface with an external slave controller.
INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$	I/O A(E,L) /H(1) R(Z) /P(1)	These pins provide a multiplexed function. As inputs, they provide a maskable **INTerrupt** that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an INTERRUPT ACKNOWLEDGE handshake signal to allow interrupt expansion.
P2.7 P2.6	I/O A(L) H(X) R(Z) P(X)	BI-DIRECTIONAL, open-drain **Port** pins.
$\overline{\text{CTS0}}$ P2.4/$\overline{\text{CTS1}}$	I A(L)	**Clear-To-Send** input is used to prevent the transmission of serial data on their respective TXD signal pin. $\overline{\text{CTS1}}$ is multiplexed with an input only port function.
TXD0 P2.1/TXD1	O H(X)/H(Q) R(1) P(X)/P(Q)	**Transmit Data** output provides serial data information. TXD1 is multiplexed with an output only **Port** function. During synchronous serial communications, TXD will function as a clock output.
RXD0 P2.0/RXD1	I/O A(L) R(Z) H(Q) P(X)	**Receive Data** input accepts serial data information. RXD1 is multiplexed with an input only **Port** function. During synchronous serial communications, RXD is bi-directional and will become an output for transmission or data (TXD becomes the clock).
P2.5/BCLK0 P2.2/BCLK1	I A(L)/A(E)	**Baud CLocK** input can be used as an alternate clock source for each of the integrated serial channels. BCLKx is multiplexed with an input only **Port** function, and cannot exceed a clock rate greater than one-half the operating frequency of the 80C188EB.
P2.3/SINT1	O H(X)/H(Q) R(0) P(X)/P(Q)	**Serial INTerrupt** output will go active to indicate serial channel 1 requires service. SINT1 is multiplexed with an output only **Port** function.

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80C188EB PINOUT

Tables 3 and 4 list the 80C188EB pin names with package location for the 84-pin Plastic Leaded Chip Carrier (PLCC) component. Figure 5 depicts the complete 80C188EB pinout (PLCC package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 5 and 6 list the 80C188EB pin names with package location for the 80-pin Quad Flat Pack (QFP) component. Figure 6 depicts the complete 80C188EB (QFP package) as viewed from the top side of the component (i.e., contacts facing down).

Table 3. PLCC Pin Names with Package Location

Address/Data Bus	
Name	**Location**
AD0	61
AD1	66
AD2	68
AD3	70
AD4	72
AD5	74
AD6	76
AD7	78
A8	62
A9	67
A10	69
A11	71
A12	73
A13	75
A14	77
A15	79
A16	80
A17	81
A18	82
A19/$\overline{\text{ONCE}}$	83

Bus Control	
Name	**Location**
ALE	6
$\overline{\text{RFSH}}$	7
$\overline{\text{S0}}$	10
$\overline{\text{S1}}$	9
$\overline{\text{S2}}$	8
$\overline{\text{RD}}$	4
$\overline{\text{WR}}$	5
READY	18
$\overline{\text{DEN}}$	11
DT/$\overline{\text{R}}$	16
$\overline{\text{LOCK}}$	15
HOLD	13
HLDA	12

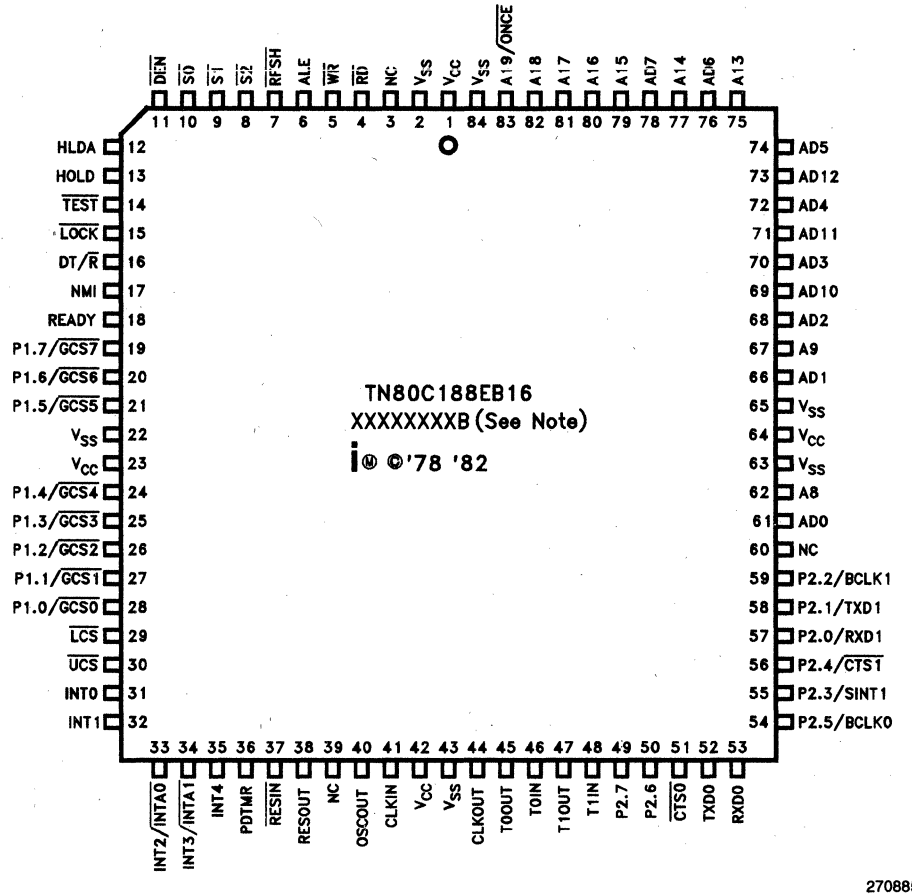
Power	
Name	**Location**
V_{SS}	2, 22, 43, 63, 65, 84
V_{CC}	1, 23, 42, 64

Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	37
RESOUT	38
CLKIN	41
OSCOUT	40
CLKOUT	44
$\overline{\text{TEST}}$	14
NC	60
NC	39
NC	3
PDTMR	36
NMI	17
INT0	31
INT1	32
INT2/$\overline{\text{INTA0}}$	33
INT3/$\overline{\text{INTA1}}$	34
INT4	35

I/O	
Name	**Location**
$\overline{\text{UCS}}$	30
$\overline{\text{LCS}}$	29
P1.0/$\overline{\text{GCS0}}$	28
P1.1/$\overline{\text{GCS1}}$	27
P1.2/$\overline{\text{GCS2}}$	26
P1.3/$\overline{\text{GCS3}}$	25
P1.4/$\overline{\text{GCS4}}$	24
P1.5/$\overline{\text{GCS5}}$	21
P1.6/$\overline{\text{GCS6}}$	20
P1.7/$\overline{\text{GCS7}}$	19
T0OUT	45
T0IN	46
T1OUT	47
T1IN	48
RXD0	53
TXD0	52
P2.5/BCLK0	54
$\overline{\text{CTS0}}$	51
P2.0/RXD1	57
P2.1/TXD1	58
P2.2/BCLK1	59
P2.3/SINT1	55
P2.4/$\overline{\text{CTS1}}$	56
P2.6	50
P2.7	49

Table 4. PLCC Package Locations with Pin Name

Location	Name	Location	Name	Location	Name	Location	Name
1	V_{CC}	22	V_{SS}	43	V_{SS}	64	V_{CC}
2	V_{SS}	23	V_{CC}	44	CLKOUT	65	V_{SS}
3	NC	24	P1.4/$\overline{GCS4}$	45	T0OUT	66	AD1
4	$\overline{RD}$	25	P1.3/$\overline{GCS3}$	46	T0IN	67	A9
5	$\overline{WR}$	26	P1.2/$\overline{GCS2}$	47	T1OUT	68	AD2
6	ALE	27	P1.1/$\overline{GCS1}$	48	T1IN	69	A10
7	$\overline{RFSH}$	28	P1.0/$\overline{GCS0}$	49	P2.7	70	AD3
8	$\overline{S2}$	29	$\overline{LCS}$	50	P2.6	71	A11
9	$\overline{S1}$	30	$\overline{UCS}$	51	$\overline{CTS0}$	72	AD4
10	$\overline{S0}$	31	INT0	52	TXD0	73	A12
11	$\overline{DEN}$	32	INT1	53	RXD0	74	AD5
12	HLDA	33	INT2/$\overline{INTA0}$	54	P2.5/BCLK0	75	A13
13	HOLD	34	INT3/$\overline{INTA1}$	55	P2.3/SINT1	76	AD6
14	$\overline{TEST}$	35	INT4	56	P2.4/$\overline{CTS1}$	77	A14
15	$\overline{LOCK}$	36	PDTMR	57	P2.0/RXD1	78	AD7
16	DT/$\overline{R}$	37	$\overline{RESIN}$	58	P2.1/TXD1	79	A15
17	NMI	38	RESOUT	59	P2.2/BCLK1	80	A16
18	READY	39	NC	60	NC	81	A17
19	P1.7/$\overline{GCS7}$	40	OSCOUT	61	AD0	82	A18
20	P1.6/$\overline{GCS6}$	41	CLKIN	62	A8	83	A19/$\overline{ONCE}$
21	P1.5/$\overline{GCS5}$	42	V_{CC}	63	V_{SS}	84	V_{SS}



NOTE:
This is the FPO number location (indicated by the X's).

Figure 5. 84-Pin Plastic Leaded Chip Carrier Pinout Diagram

Table 5. QFP Pin Name with Package Location

Address/Data Bus	
Name	**Location**
AD0	10
AD1	15
AD2	17
AD3	19
AD4	21
AD5	23
AD6	25
AD7	27
A8	11
A9	16
A10	18
A11	20
A12	22
A13	24
A14	26
A15	28
A16	29
A17	30
A18	31
A19/$\overline{\text{ONCE}}$	32

Bus Control	
Name	**Location**
ALE	38
$\overline{\text{RFSH}}$	39
$\overline{\text{S0}}$	42
$\overline{\text{S1}}$	41
$\overline{\text{S2}}$	40
$\overline{\text{RD}}$	36
$\overline{\text{WR}}$	37
READY	49
$\overline{\text{DEN}}$	43
$\overline{\text{LOCK}}$	47
HOLD	45
HLDA	44

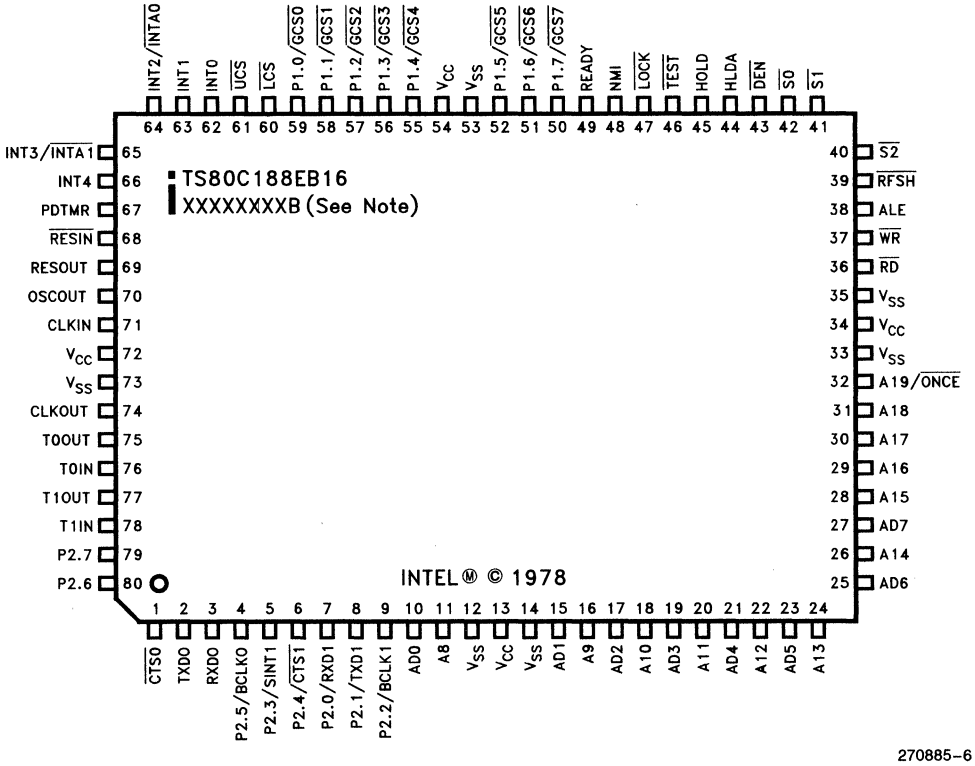
Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	68
RESOUT	69
CLKIN	71
OSCOUT	70
CLKOUT	74
$\overline{\text{TEST}}$	46
PDTMR	67
NMI	48
INT0	62
INT1	63
INT2/$\overline{\text{INTA0}}$	64
INT3/$\overline{\text{INTA1}}$	65
INT4	66

Power	
Name	**Location**
V_{SS}	12, 14, 33, 35, 53, 73
V_{CC}	13, 34, 54, 72

I/O	
Name	**Location**
$\overline{\text{UCS}}$	61
$\overline{\text{LCS}}$	60
P1.0/$\overline{\text{GCS0}}$	59
P1.1/$\overline{\text{GCS1}}$	58
P1.2/$\overline{\text{GCS2}}$	57
P1.3/$\overline{\text{GCS3}}$	56
P1.4/$\overline{\text{GCS4}}$	55
P1.5/$\overline{\text{GCS5}}$	52
P1.6/$\overline{\text{GCS6}}$	51
P1.7/$\overline{\text{GCS7}}$	50
T0OUT	75
T0IN	76
T1OUT	77
T1IN	78
RXD0	3
TXD0	2
P2.5/BCLK0	4
$\overline{\text{CTS0}}$	1
P2.0/RXD1	7
P2.1/TXD1	8
P2.2/BCLK1	9
P2.3/SINT1	5
P2.4/$\overline{\text{CTS1}}$	6
P2.6	80
P2.7	79

Table 6. QFP Package Location with Pin Names

Location	Name	Location	Name	Location	Name	Location	Name
1	$\overline{CTS0}$	21	AD4	41	$\overline{S1}$	61	$\overline{UCS}$
2	TXD0	22	A12	42	$\overline{S0}$	62	INT0
3	RXD0	23	AD5	43	$\overline{DEN}$	63	INT1
4	P2.5/BCLK0	24	A13	44	HLDA	64	INT2/$\overline{INTA0}$
5	P2.3/SINT1	25	AD6	45	HOLD	65	INT3/$\overline{INTA1}$
6	P2.4/$\overline{CTS1}$	26	A14	46	$\overline{TEST}$	66	INT4
7	P2.0/RXD1	27	AD7	47	$\overline{LOCK}$	67	PDTMR
8	P2.1/TXD1	28	A15	48	NMI	68	$\overline{RESIN}$
9	P2.2/BCLK1	29	A16	49	READY	69	RESOUT
10	AD0	30	A17	50	P1.7/$\overline{GCS7}$	70	OSCOUT
11	A8	31	A18	51	P1.6/$\overline{GCS6}$	71	CLKIN
12	V_{SS}	32	A19/$\overline{ONCE}$	52	P1.5/$\overline{GCS5}$	72	V_{CC}
13	V_{CC}	33	V_{SS}	53	V_{SS}	73	V_{SS}
14	V_{SS}	34	V_{CC}	54	V_{CC}	74	CLKOUT
15	AD1	35	V_{SS}	55	P1.4/$\overline{GCS4}$	75	T0OUT
16	A9	36	$\overline{RD}$	56	P1.3/$\overline{GCS3}$	76	T0IN
17	AD2	37	$\overline{WR}$	57	P1.2/$\overline{GCS2}$	77	T1OUT
18	A10	38	ALE	58	P1.1/$\overline{GCS1}$	78	T1IN
19	AD3	39	$\overline{RFSH}$	59	P1.0/$\overline{GCS0}$	79	P2.7
20	A11	40	$\overline{S2}$	60	$\overline{LCS}$	80	P2.6



NOTE:
This is the FPO number location (indicated by the X's).

Figure 6. Quad Flat Pack Pinout Diagram

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PACKAGE THERMAL SPECIFICATIONS

The 80C188EB is specified for operation when T_C (the case temperature) is within the range of −40°C to +100°C (PLCC package) or −40°C to +114°C (QFP package). T_C may be measured in any environment to determine whether the 80C188EB is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P*\theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 7 for the 84-pin Plastic Leaded Chip Carrier (PLCC) package.

Table 8 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies. P (the maximum power consumption, specified in watts) is calculated by using the maximum ICC as tabulated in the DC specifications and V_{CC} of 5.5V.

Table 7. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow Linear ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PLCC)	30	24	21	19	17	16.5
θ_{CA} (QFP)	58	47	43	40	38	36

Table 8. Maximum T_A at Various Airflows (in °C)

		Airflow Linear ft/min (m/sec)					
	T_F (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A (PLCC)	16	91.5	93.5	94	94.5	95.5	95.5
	26	88.5	91	92	92.5	93.5	93.5
	32	85	87.5	89.5	90.5	91.5	92
T_A (QFP)	16	98	101	102	103	103.5	104
	26	92	96	97.5	99	99.5	100
	32	85	90.5	92.5	94	95	96

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	−65°C to +150°C
Case Temp Under Bias	−65°C to +120°C
Supply Voltage with respect to V_{SS}	−0.5V to +6.5V
Voltage on other Pins with respect to V_{SS}	−0.5V to V_{CC} +0.5V

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.5	5.5	V
T_F	Input Clock Frequency			
	80C188EB-20	0	40	MHz
	80C188EB-16	0	32	MHz
	80C188EB-13	0	26.08	MHz
	80C188EB	0	16	MHz
T_C	Case Temperature Under Bias			
	TN80C188EB-XX (PLCC)	−40	+100	°C
	TS80C188EB-XX (QFP)	−40	+114	°C

RECOMMENDED CONNECTIONS

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80C188EB-based circuit board should include separate power (V_{CC}) and ground (V_{SS}) planes. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "NC" must not be connected in the system. Liberal decoupling capacitance should be placed near the 80C188EB. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by placing the decoupling capacitors as close as possible to the 80C188EB V_{CC} and V_{SS} package pins.

Always connect any unused input to an appropriate signal level. In particular, unused interrupt inputs (INT0:4) should be connected to V_{CC} through a pull-up resistor (in the range of 50 KΩ). **Leave any unused output pin or any NC pin unconnected.**

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	−0.5	0.3*V_{CC}	V	
V_{IH}	Input High Voltage	0.7*V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 3 mA (Min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −2 mA (Min)
V_{HYR}	Input Hysterisis on $\overline{RESIN}$	0.50		V	
I_{LI1}	Input Leakage Current for pins: AD7:0, READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$, NMI, INT4:0, T0IN, T1IN, RXD0, $\overline{BCLK0}$, $\overline{CTS0}$, RXD1, $\overline{BCLK1}$, $\overline{CTS1}$, P2.6, P2.7		±15	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LI2}	Input Leakage Current for pins: A19/$\overline{ONCE}$, A18:16, $\overline{LOCK}$	−0.275	−5.0	mA	V_{IN} = 0.7 V_{CC} (Note 1)
I_{LO}	Output Leakage Current		±15	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 2)
I_{CC}	Supply Current Cold (RESET) 80C188EB-20		108	mA	(Note 3)
	80C188EB-16		90	mA	(Note 3)
	80C188EB-13		73	mA	(Note 3)
	80C188EB-8		45	mA	(Note 3)
I_{ID}	Supply Current Idle 80C188EB-20		76	mA	(Note 4)
	80C188EB-16		63	mA	(Note 4)
	80C188EB-13		48	mA	(Note 4)
	80C188EB-8		31	mA	(Note 4)
I_{PD}	Supply Current Powerdown 80C188EB-20		100	μA	(Note 5)
	80C188EB-16		100	μA	(Note 5)
	80C188EB-13		100	μA	(Note 5)
	80C188EB-8		100	μA	(Note 5)
CIN	Input Pin Capacitance	0	15	pF	T_F = 1 MHz
COUT	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 6)

NOTES:
1. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
2. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
3. Measured with the device in RESET and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or V_{SS}.
4. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or V_{SS}.
5. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or V_{SS}.
6. Output Capacitance is the capacitive load of a floating output pin.

I_{CC} VERSUS FREQUENCY AND VOLTAGE

The current (I_{CC}) consumption of the 80C188EB is essentially composed of two components; I_{PD} and I_{CCS}.

I_{PD} is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or V_{CC} (no clock applied to the device). I_{PD} is equal to the Powerdown current and is typically less than 50 μA.

I_{CCS} is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since I_{CCS} is typically much greater than I_{PD}, I_{PD} can often be ignored when calculating I_{CC}.

I_{CCS} is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: V = Device operating voltage (V_{CC})

C_{DEV} = Device capacitance

f = Device operating frequency

$I_{CCS} = I_{CC}$ = Device current

Measuring C_{DEV} on a device like the 80C188EB would be difficult. Instead, C_{DEV} is calculated using the above formula by measuring I_{CC} at a known V_{CC} and frequency (see Table 9). Using this C_{DEV} value, I_{CC} can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical I_{CC} when operating at 10 MHz, 4.8V.

$$I_{CC} = I_{CCS} = 4.8 \times 0.583 \times 10 \approx 28 \text{ mA}$$

PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: t = desired delay in **seconds**

C_{PD} = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132$ μF is required. Round up to standard (available) capacitive values.

NOTE:
The above equation applies to delay times greater than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperature will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

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Table 9. Device Capacitance (C_{DEV}) Values

Parameter	Typ	Max	Units	Notes
C_{DEV} (Device in Reset)	0.583	1.02	mA/V*MHz	1, 2
C_{DEV} (Device in Idle)	0.408	0.682	mA/V*MHz	1, 2

1. Max C_{DEV} is calculated at −40°C, all floating outputs driven to V_{CC} or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical C_{DEV} is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

AC SPECIFICATIONS

AC Characteristics—80C188EB-20

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	40	MHz	1
T_C	CLKIN Period	25	∞	ns	1
T_{CH}	CLKIN High Time	10	∞	ns	1, 2
T_{CL}	CLKIN Low Time	10	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	17	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{RFSH}$, $\overline{LOCK}$, A19:16	3	20	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$	3	25	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	20	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD7:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$, A15:8	3	25	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:8	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, AD7:0, A15:8	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD7:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD7:0	3		ns	1, 10
T_{CLIS}	HOLD	10		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A19:8 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C188EB operation.

AC SPECIFICATIONS (Continued)

AC Characteristics—80C188EB-16

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	32	MHz	1
T_C	CLKIN Period	31.25	∞	ns	1
T_{CH}	CLKIN High Time	10	∞	ns	1, 2
T_{CL}	CLKIN Low Time	10	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	20	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{RFSH}$, $\overline{LOCK}$, A19:16	3	22	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$	3	27	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	22	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD7:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$, A15:8	3	27	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:8	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, AD7:0, A15:8	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD7:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD7:0	3		ns	1, 10
T_{CLIS}	HOLD	10		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A19:8 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C188EB operation.

AC SPECIFICATIONS (Continued)

AC Characteristics—80C188EB-13

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	26.08	MHz	1
T_C	CLKIN Period	38.34	∞	ns	1
T_{CH}	CLKIN High Time	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	23	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{RFSH}$, $\overline{LOCK}$, A19:16	3	25	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$	3	30	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	25	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD7:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$, A15:8	3	30	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, AD7:0, A15:8	0	25	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0, T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD7:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD7:0	3		ns	1, 10
T_{CLIS}	HOLD	10		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A8:0 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C188EB operation.

AC SPECIFICATIONS (Continued)

AC Characteristics—80C188EB-8

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	16	MHz	1
T_C	CLKIN Period	62.5	∞	ns	1
T_{CH}	CLKIN High Time	15	∞	ns	1, 2
T_{CL}	CLKIN Low Time	15	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	27	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{RFSH}$, $\overline{LOCK}$, A19:16	3	30	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$	3	35	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	30	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD7:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$, A15:8	3	35	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, AD7:0, A15:8	0	35	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0 T1:0IN, READY, $\overline{CTS1:0}$, P2.6, P2.7	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, BCLK1:0 T1:0IN, READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD7:0, READY	10		ns	1, 10
T_{CLIH}	READY, AD7:0	3		ns	1, 10
T_{CLIS}	HOLD	10		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 13 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 14 for rise and fall times outside 50 pF.
6. See Figure 14 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A19:8 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C188EB operation.

AC SPECIFICATIONS (Continued)

Relative Timings (80C188EB-20, -16, -13, -8)

Symbol	Parameter	Min	Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Rising to ALE Falling	T − 15		ns	
T_{AVLL}	Address Valid to ALE Falling	½T − 10		ns	
T_{PLLL}	Chip Selects Valid to ALE Falling	½T − 10		ns	1
T_{LLAX}	Address Hold from ALE Falling	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{WHLH}	$\overline{WR}$ Rising to ALE Rising	½T − 10		ns	1
T_{AFRL}	Address Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Falling to $\overline{RD}$ Rising	(2*T) − 5		ns	2
T_{WLWH}	$\overline{WR}$ Falling to $\overline{WR}$ Rising	(2*T) − 5		ns	2
T_{RHAV}	$\overline{RD}$ Rising to Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHPH}	$\overline{WR}$ Rising to Chip Select Rising	½T − 10		ns	1
T_{RHPH}	$\overline{RD}$ Rising to Chip Select Rising	½T − 10		ns	1
T_{PHPL}	$\overline{CS}$ Inactive to $\overline{CS}$ Active	½T − 10		ns	1
T_{OVRH}	$\overline{ONCE}$ Active to $\overline{RESIN}$ Rising	T		ns	3
T_{RHOX}	$\overline{ONCE}$ Hold from $\overline{RESIN}$ Rising	T		ns	3

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Not tested.

AC SPECIFICATIONS (Continued)

Serial Port Mode 0 Timings (80C188EB-20, 16, -13, -8)

Symbol	Parameter	Min	Max	Unit	Notes
T_{XLXL}	TXD Clock Period	T (n + 1)		ns	1, 2
T_{XLXH}	TXD Clock Low to Clock High (n > 1)	2T − 35	2T + 35	ns	1
T_{XLXH}	TXD Clock Low to Clock High (n = 1)	T − 35	T + 35	ns	1
T_{XHXL}	TXD Clock High to Clock Low (n > 1)	(n − 1) T − 35	(n − 1) T + 35	ns	1, 2
T_{XHXL}	TXD Clock High to Clock Low (n = 1)	T − 35	T + 35	ns	1
T_{QVXH}	RXD Output Data Setup to TXD Clock High (n > 1)	(n − 1) T − 35		ns	1, 2
T_{QVXH}	RXD Output Data Setup to TXD Clock High (n = 1)	T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (n > 1)	2T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (n = 1)	T − 35		ns	1
T_{XHQZ}	RXD Output Data Float after Last TXD Clock High		T + 20	ns	1
T_{DVXH}	RXD Input Data Setup to TXD Clock High	T + 20		ns	1
T_{XHDX}	RXD Input Data Hold after TXD Clock High	0		ns	1

NOTES:
1. See Figure 12 for waveforms.
2. n is the value of the BxCMP register ignoring the iCLK bit (i.e., ICLK = 0).

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AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 7. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

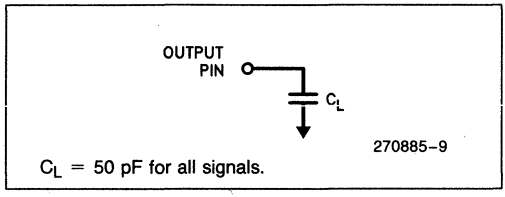


Figure 7. AC Test Load

AC TIMING WAVEFORMS

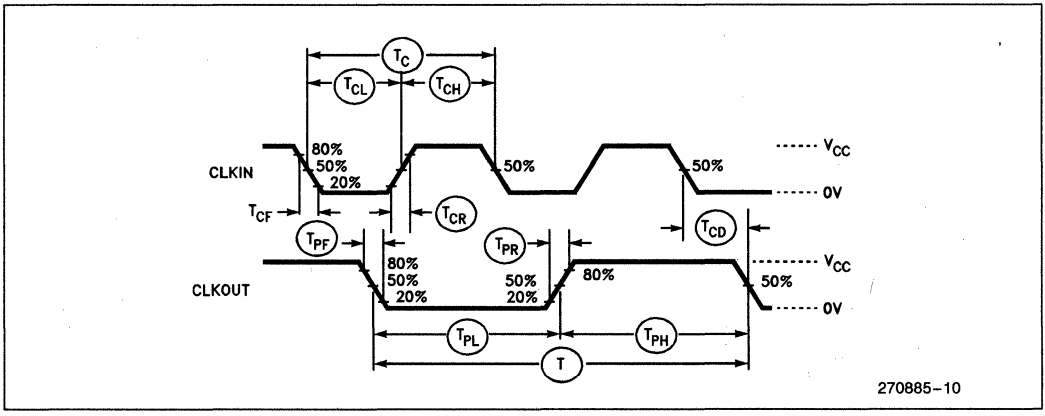
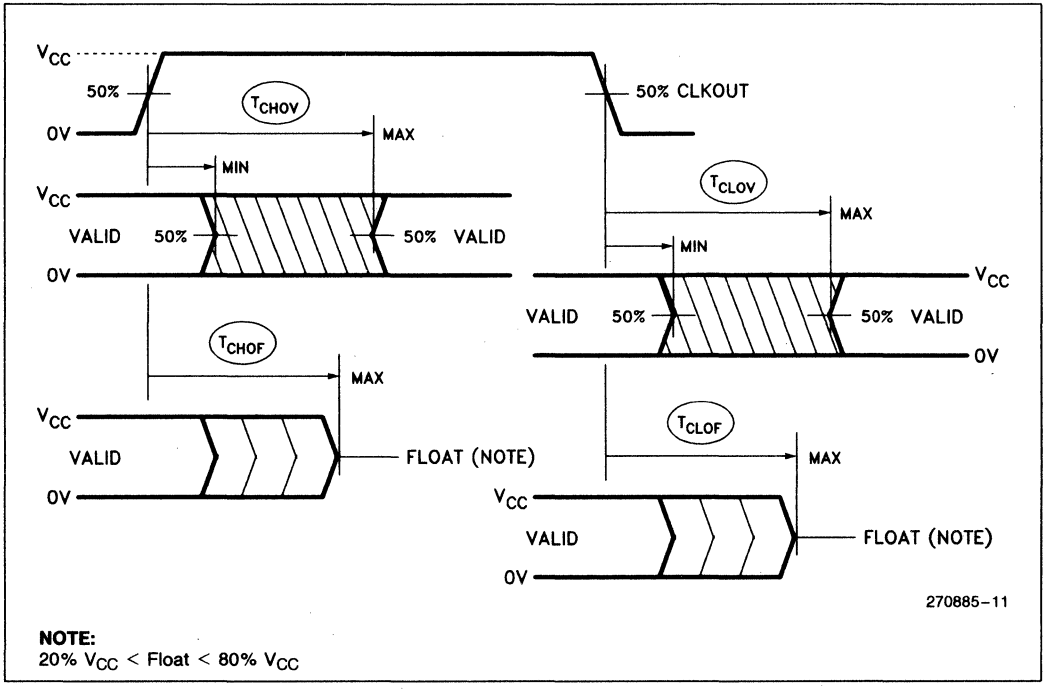


Figure 8. Input and Output Clock Waveform



NOTE:
20% V_{CC} < Float < 80% V_{CC}

Figure 9. Output Delay and Float Waveform

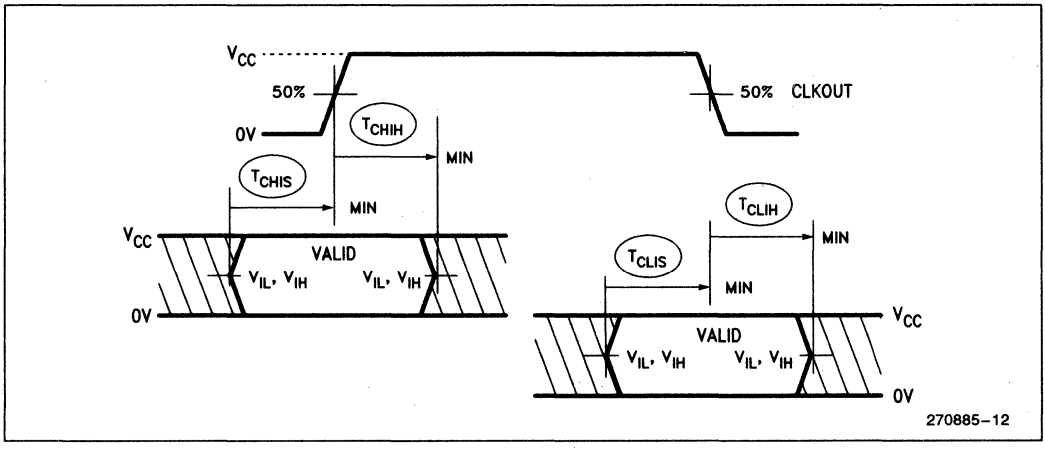


Figure 10. Input Setup and Hold

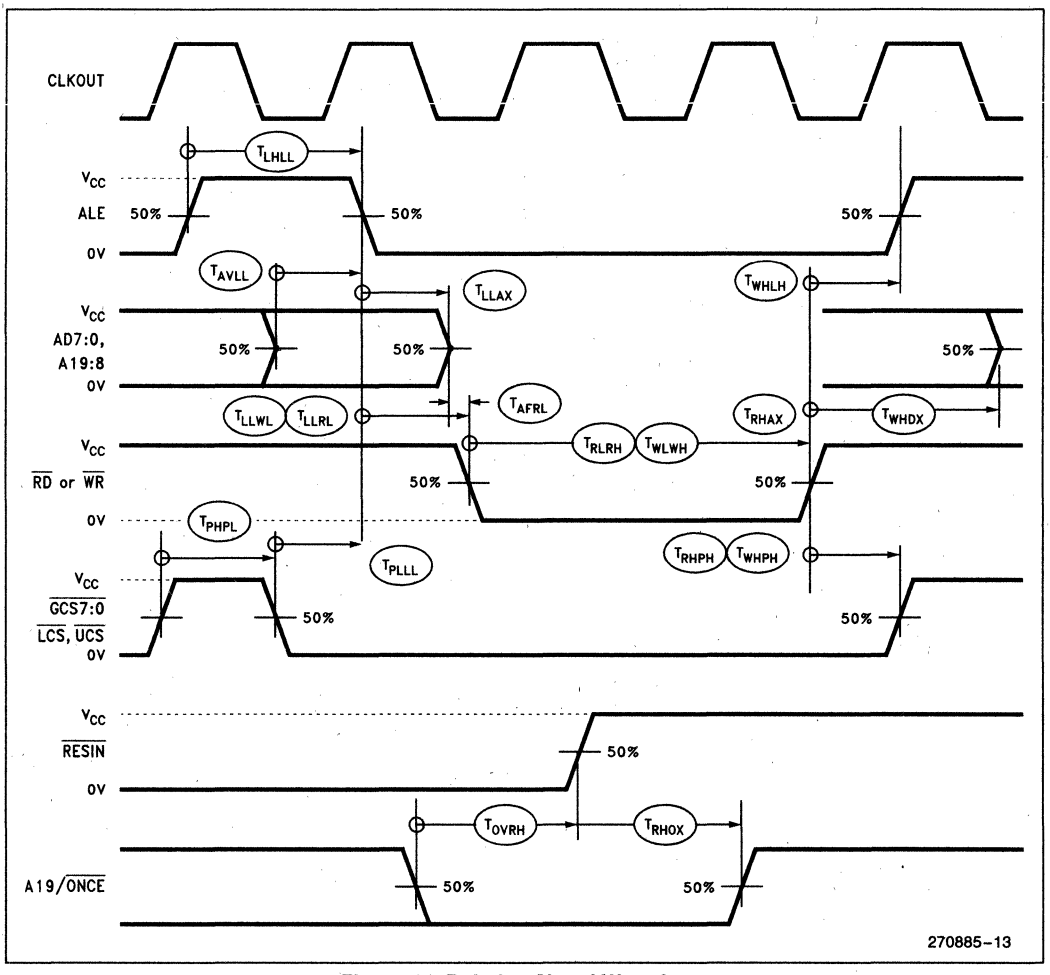


Figure 11. Relative Signal Waveform

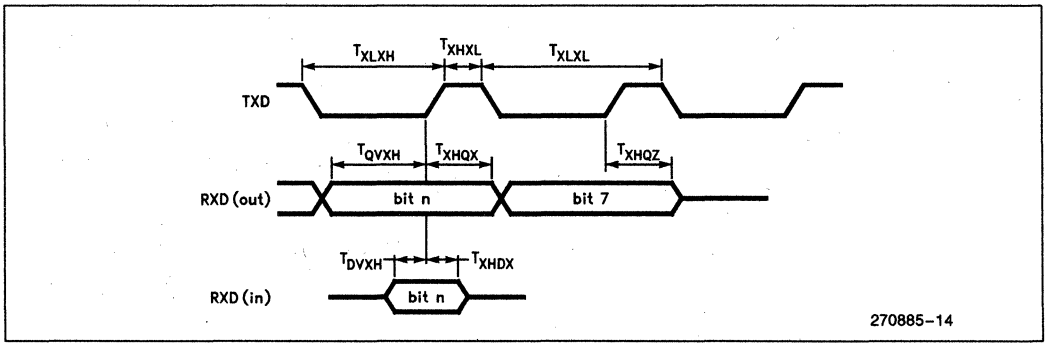
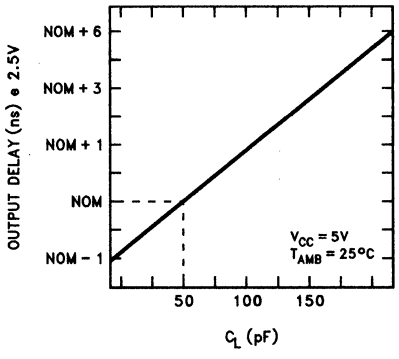


Figure 12. Serial Port Mode 0 Waveform

DERATING CURVES

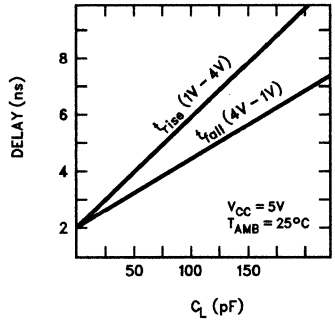
TYPICAL OUTPUT DELAY VARIATIONS VERSUS LOAD CAPACITANCE



270885-15

Figure 13

TYPICAL RISE AND FALL VARIATIONS VERSUS LOAD CAPACITANCE



270885-16

Figure 14

24

RESET

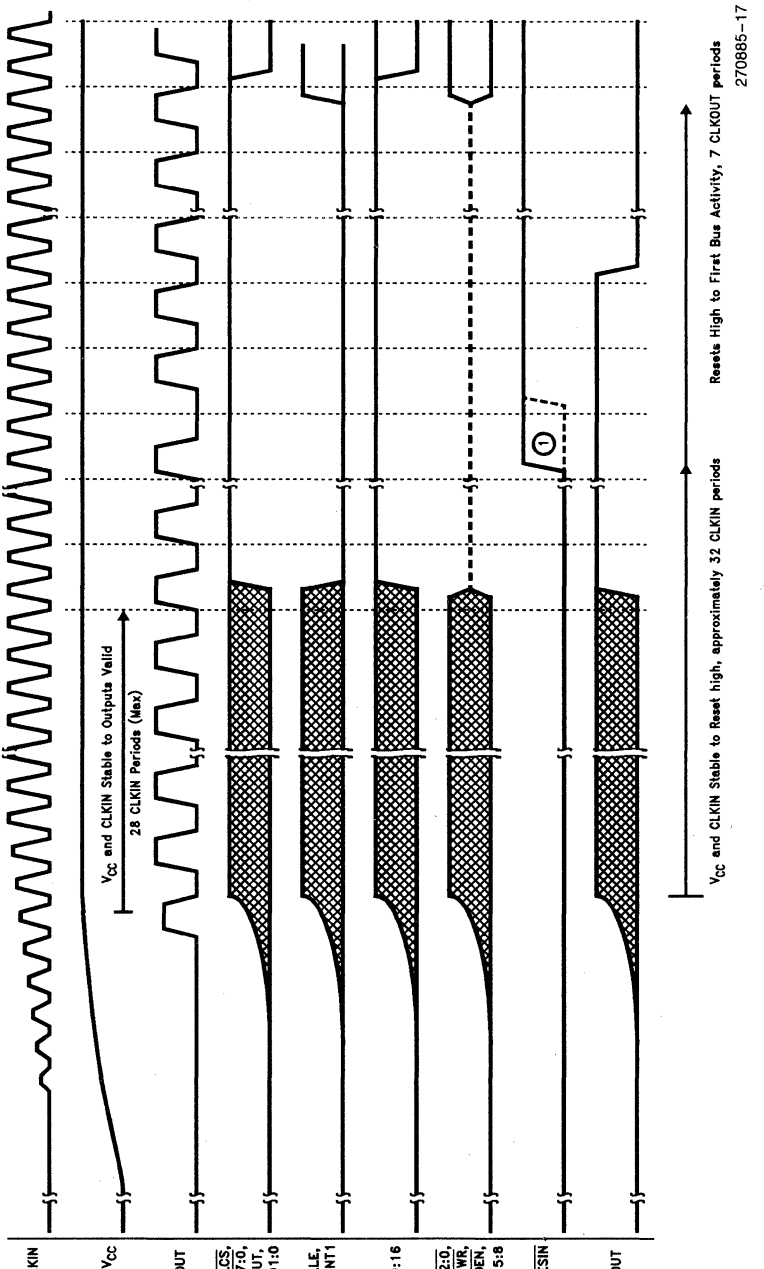
The 80C188EB will perform a reset operation any time the $\overline{RESIN}$ pin active. The $\overline{RESIN}$ pin is actually synchronized before it is presented internally, which means that the clock must be operating before a reset can take effect. From a power-on state, $\overline{RESIN}$ must be held active (low) in order to guarantee correct initialization of the 80C188EB. **Failure to provide $\overline{RESIN}$ while the device is powering up will result in unspecified operation of the device.**

Figure 15 shows the correct reset sequence when first applying power to the 80C188EB. An external clock connected to CLKIN must not exceed the V_{CC} threshold being applied to the 80C188EB. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the 80C188EB. When attaching a crystal to the device, $\overline{RESIN}$ must remain active until both V_{CC} and CLKOUT are stable (the length of time is application specific and depends on the startup characteristics of the crystal circuit). The $\overline{RESIN}$ pin is designed to operate correctly using an RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that $\overline{RESIN}$ is never really sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Figure 16 shows the timing sequence when $\overline{RESIN}$ is applied after V_{CC} is stable and the device has been operating. Note that a reset will terminate all activity and return the 80C188EB to a known operating state. Any bus operation that is in progress at the time $\overline{RESIN}$ is asserted will terminate immediately (note that most control signals will be driven to their inactive state first before floating).

While $\overline{RESIN}$ is active, bus signals $\overline{LOCK}$, A19/$\overline{ONCE}$, and A18:16 are configured as inputs and weakly held high by internal pullup transistors. Only 19/$\overline{ONCE}$ can be overdriven to a low and is used to enable $\overline{ONCE}$ Mode. Forcing $\overline{LOCK}$ or A18:16 low at any time while $\overline{RESIN}$ is low is prohibited and will cause unspecified device operation.

COLD RESET WAVEFORMS



NOTE:
CLKOUT synchronization occurs on the rising edge of RESIN. If RESIN is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If RESIN is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.

Figure 15

WARM RESET WAVEFORMS

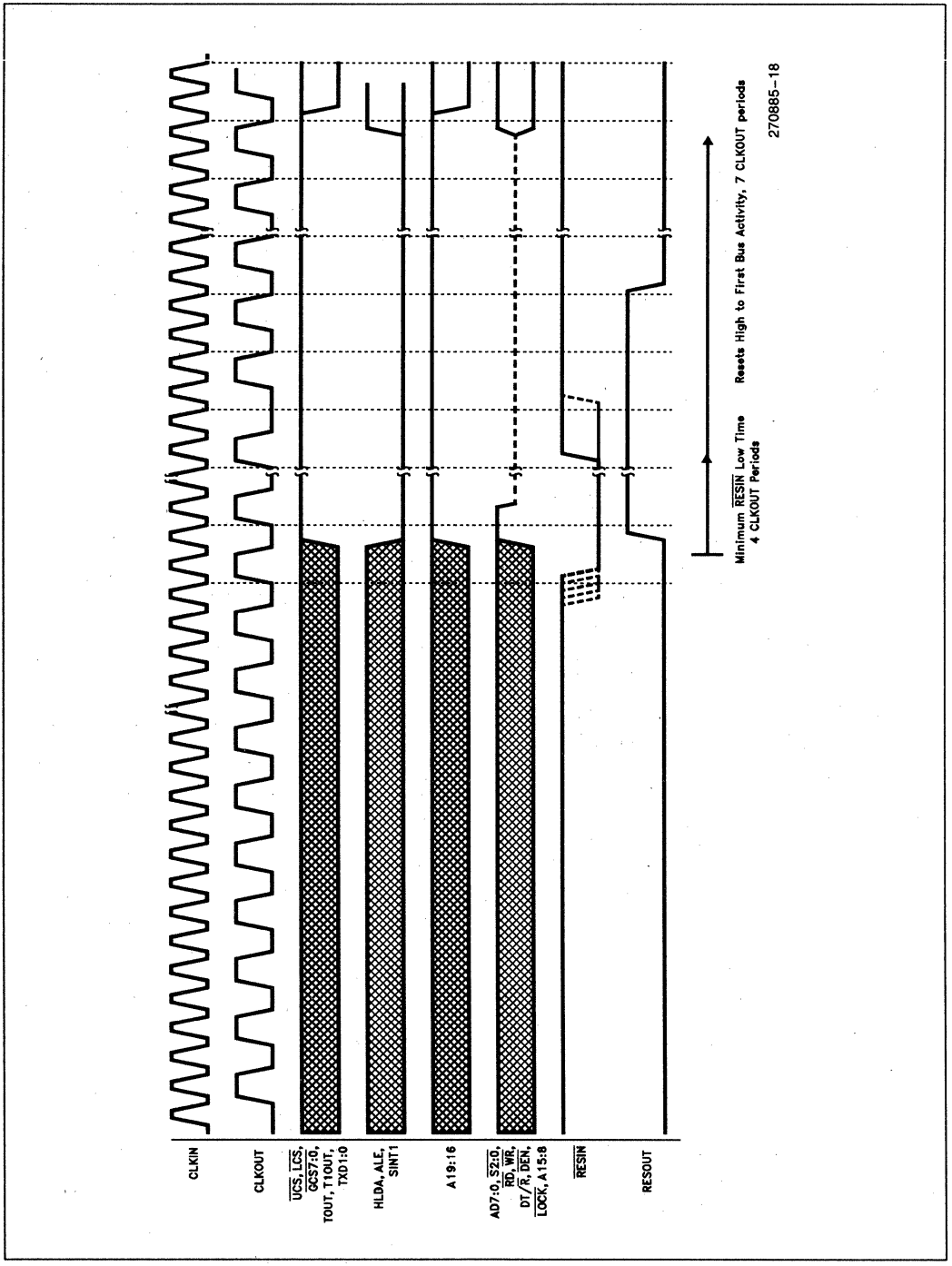


Figure 16

BUS CYCLE WAVEFORMS

Figures 17 through 23 present the various bus cycles that are generated by the 80C188EB. What is shown in the figure is the relationship of the various bus signals to CLKOUT. These figures along with the information present in **AC Specifications** allow the user to determine all the critical timing analysis needed for a given application.

MEMORY READ, I/O READ, INSTRUCTION FETCH, AND REFRESH WAVEFORM

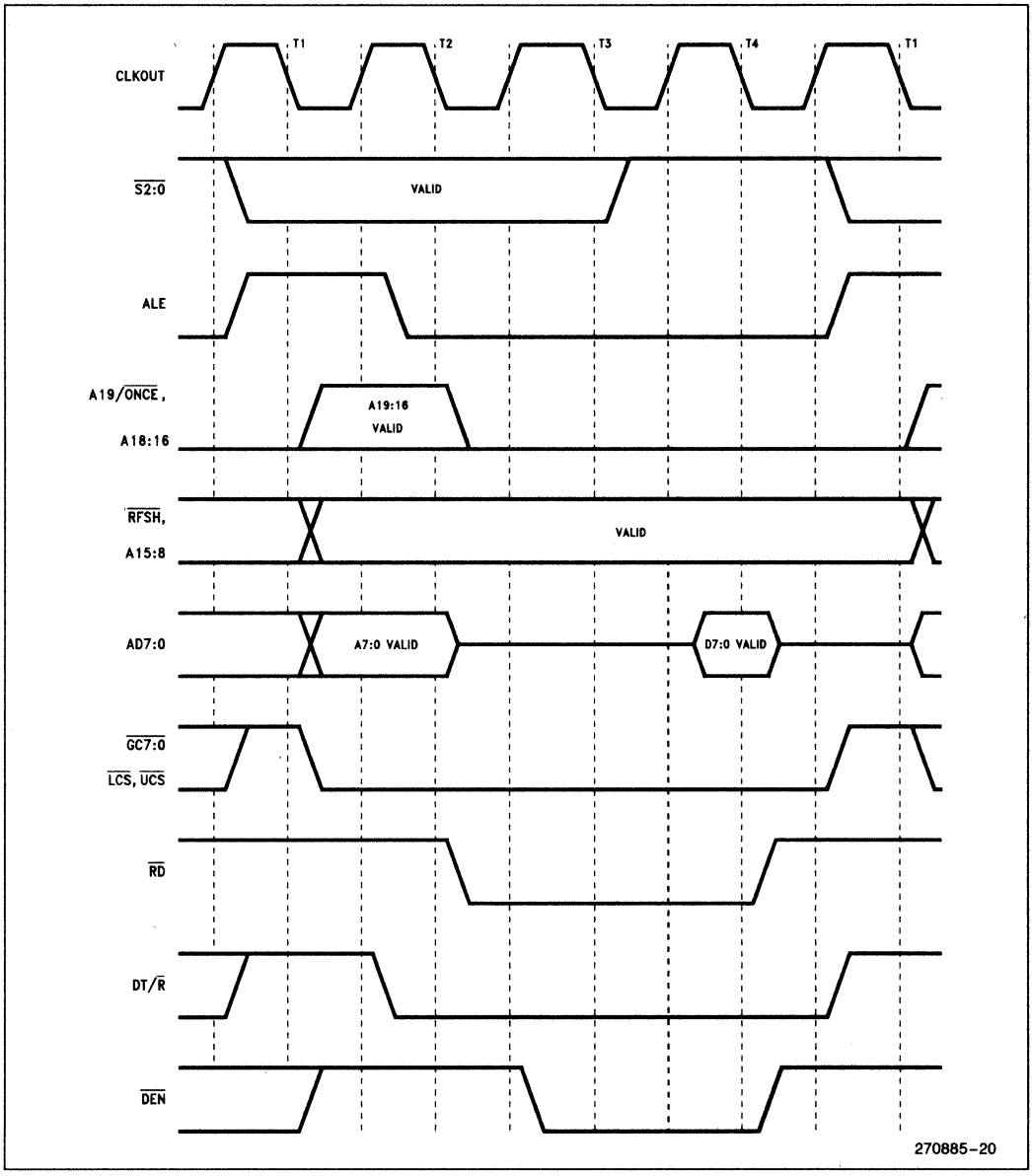


Figure 17

MEMORY WRITE AND I/O WRITE CYCLE WAVEFORM

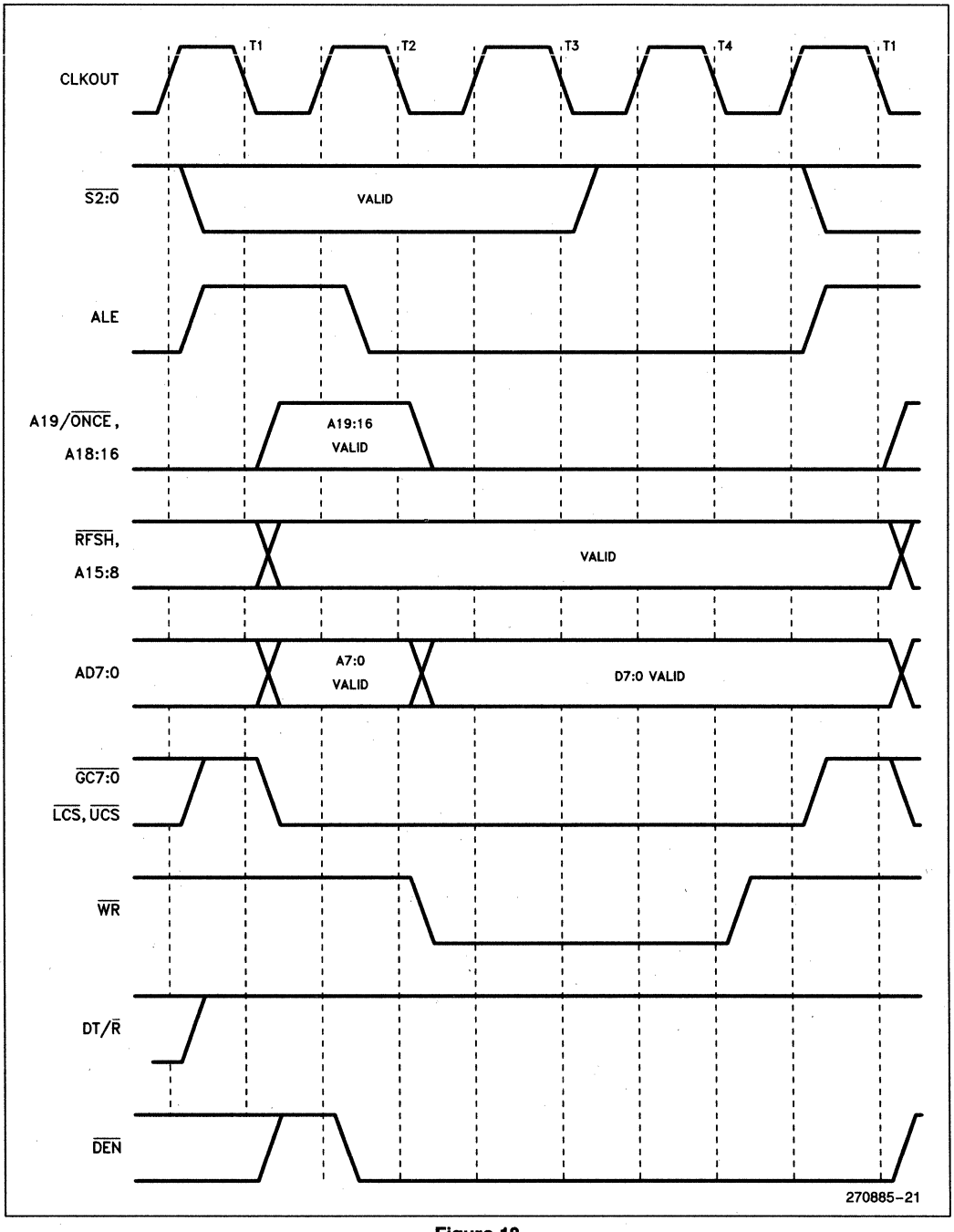
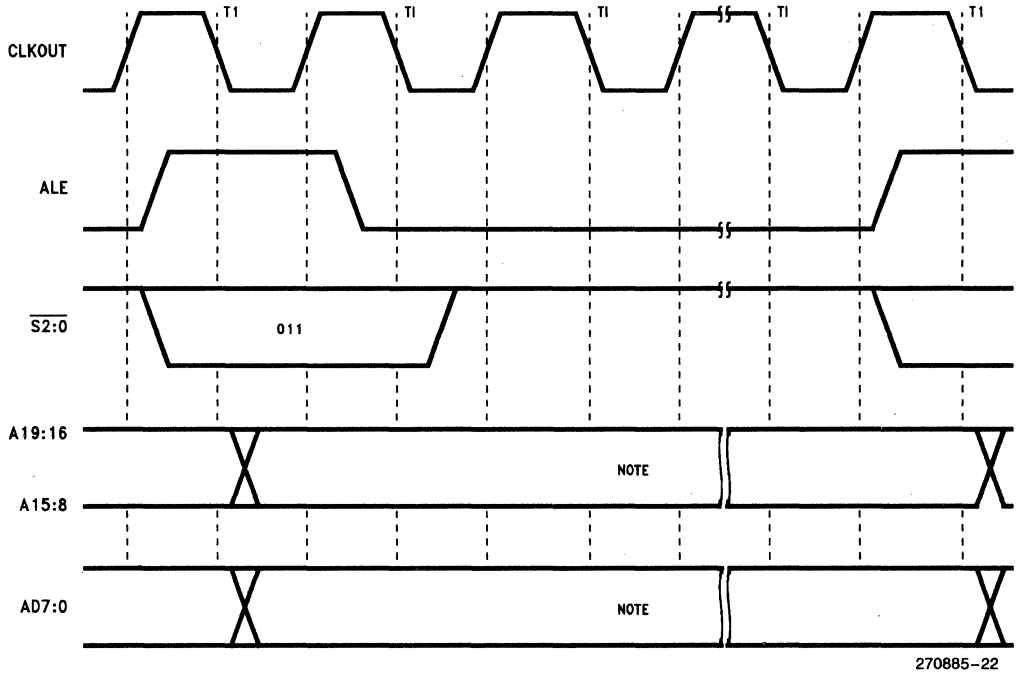


Figure 18

HALT CYCLE WAVEFORM



NOTE:
The address driven is typically the location of the next instruction prefetch.

Figure 19

CASCADE MODE INTERRUPT ACKNOWLEDGE CYCLE WAVEFORM

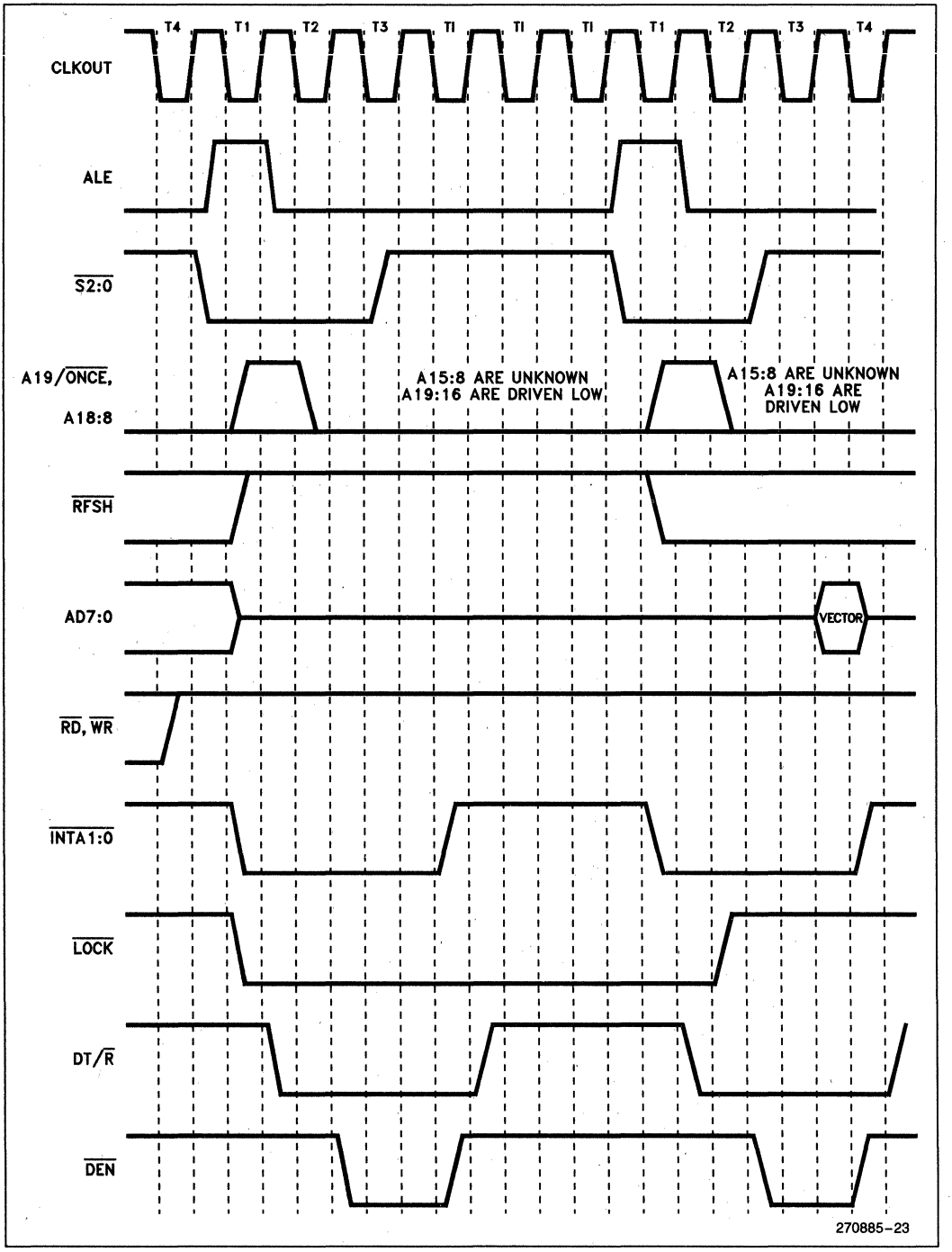


Figure 20

HOLD/HLDA CYCLE WAVEFORMS

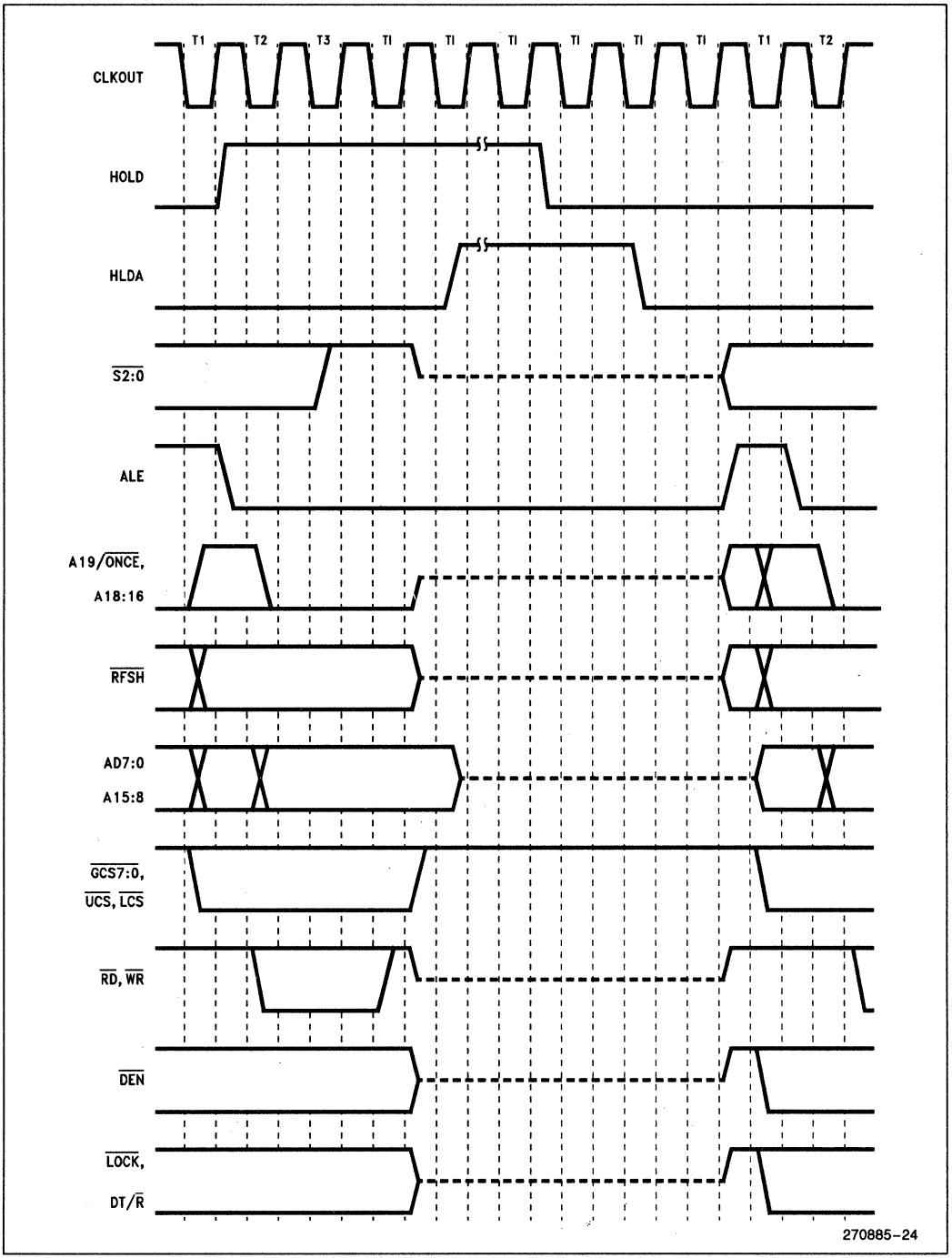
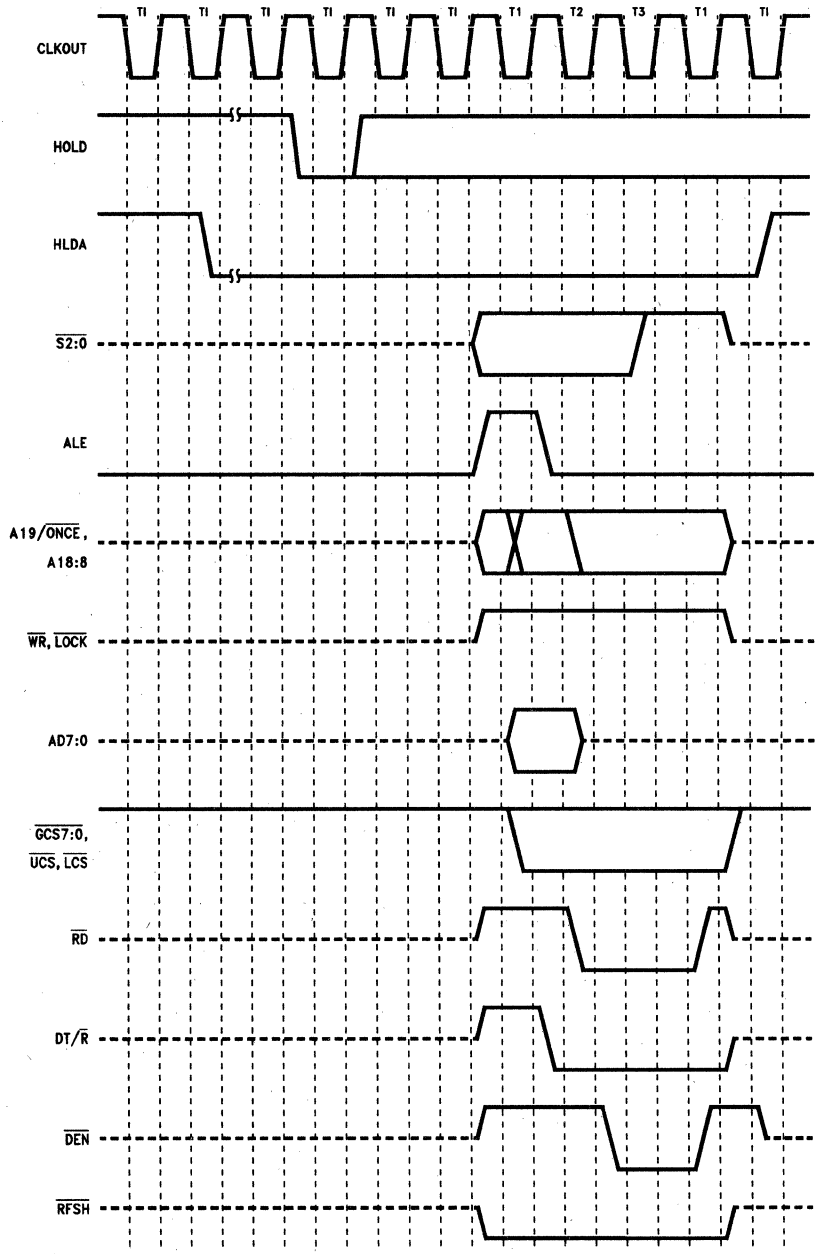


Figure 21

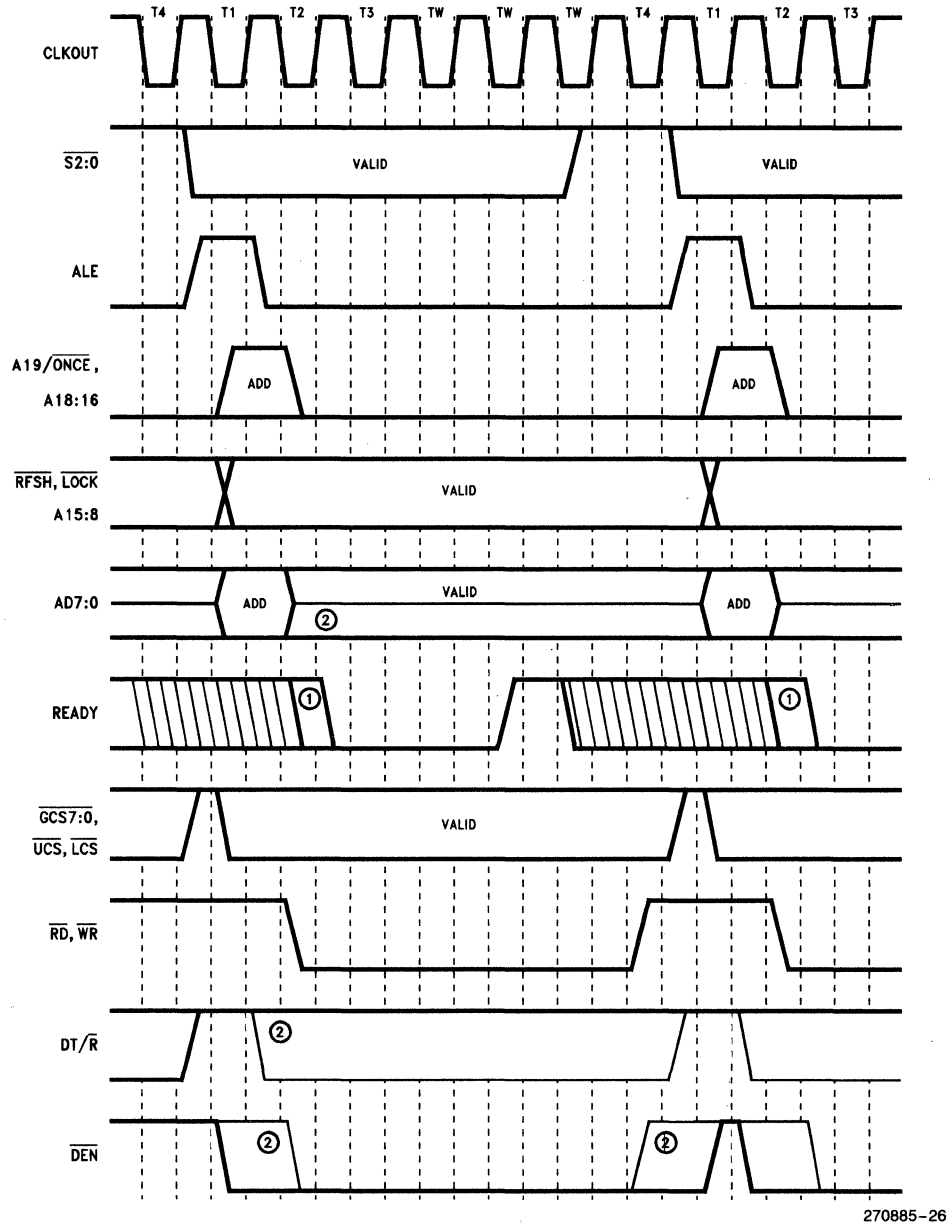
REFRESH DURING HLDA CYCLE WAVEFORM



NOTES:
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.

Figure 22

READY CYCLE WAVEFORM



NOTES:
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.

Figure 23

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REGISTER BIT SUMMARY

Figures 24 through 31 present the bit definition of each register that is active (not reserved) in the Peripheral Control Block (PCB). Each register can be thought to occupy one word (16-bits) of either memory or I/O space, although not all bits in the register necessarily have a function. A register bit is **not** guaranteed to return a specific logic value if an "X" appears for the bit definition (i.e., if a zero was written to the register bit it may not be returned as a zero when read). Furthermore, a 0 must be written to any bit that is indicated by an "X" to ensure compatibility with future products or potential product changes.

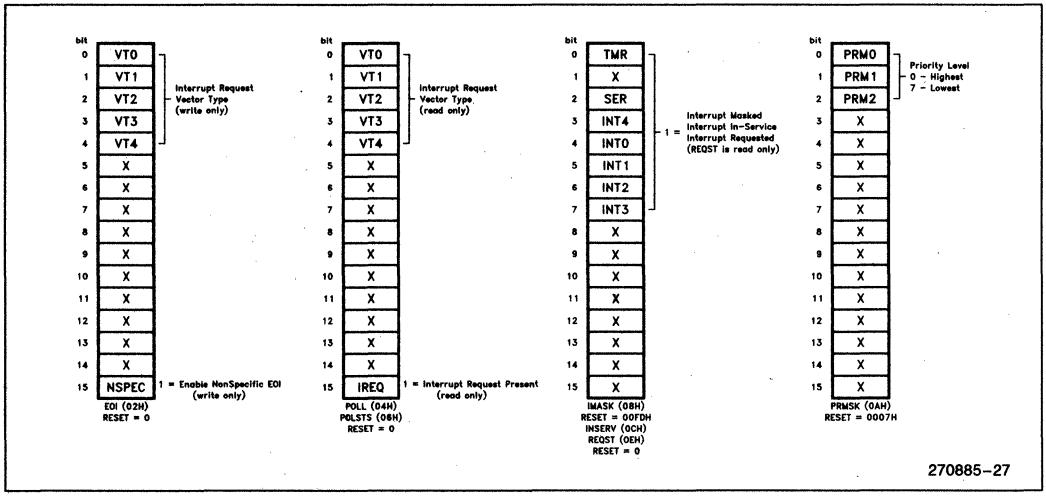

Figure 24. Interrupt Control Unit Registers

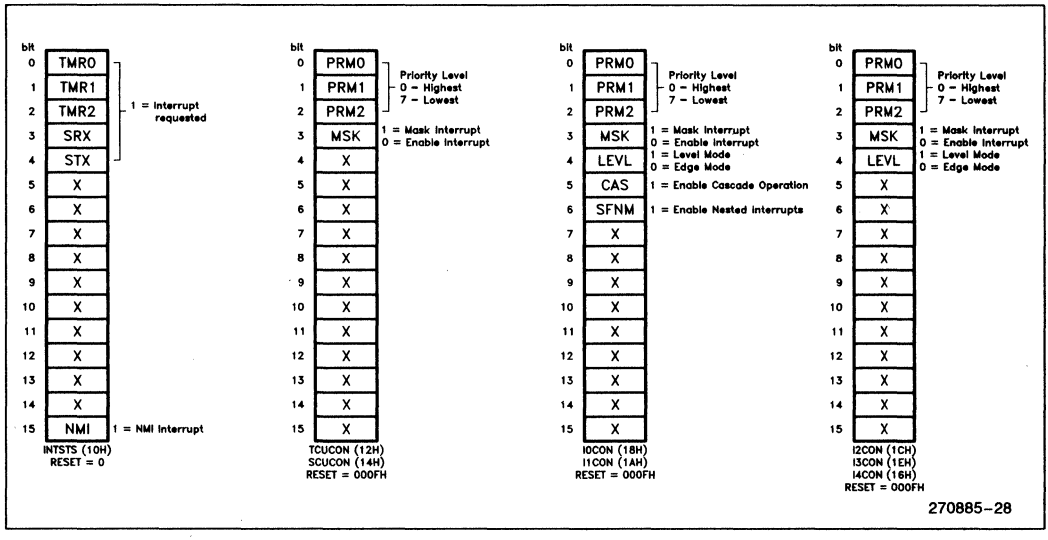

Figure 25. Interrupt Control Unit Registers

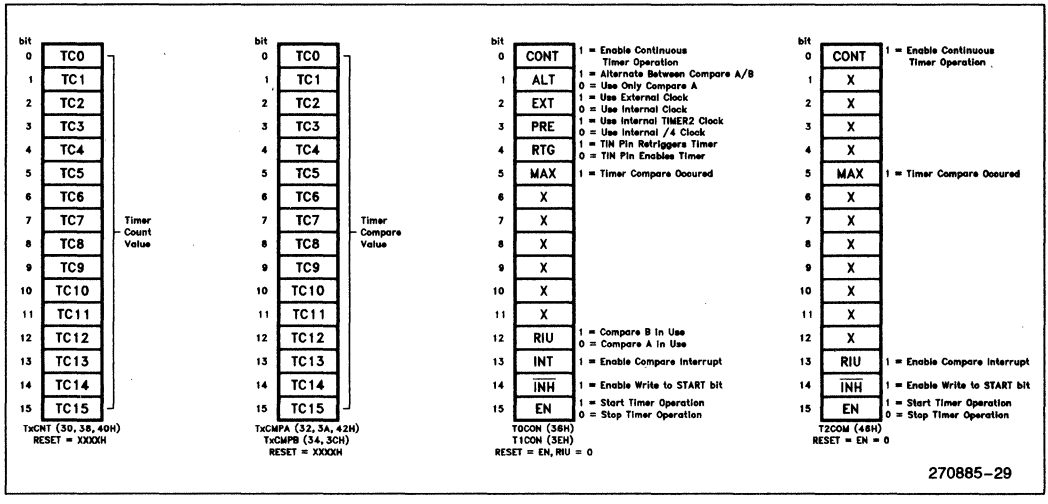

Figure 26. Timer Control Unit Registers

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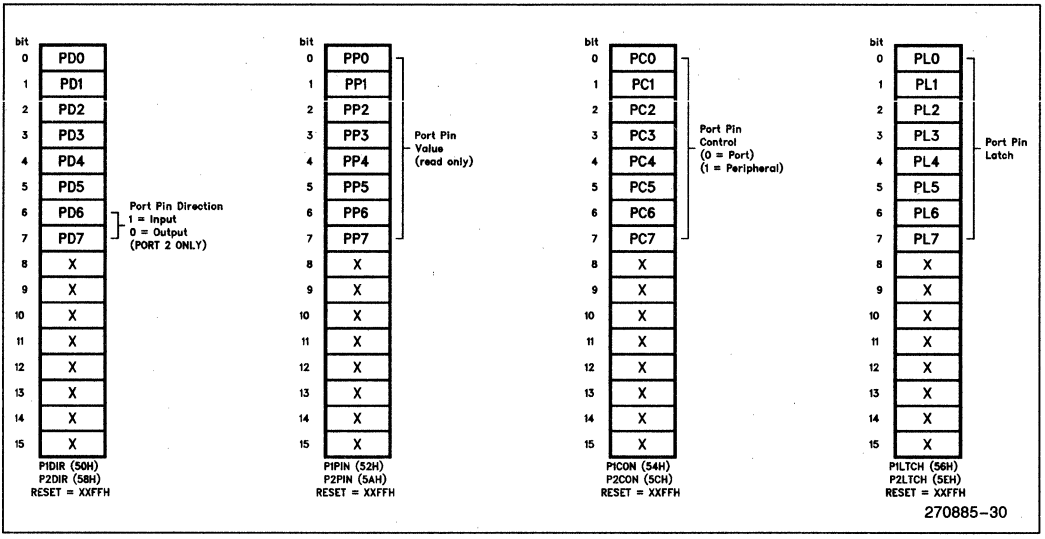

Figure 27. I/O Port Unit Registers

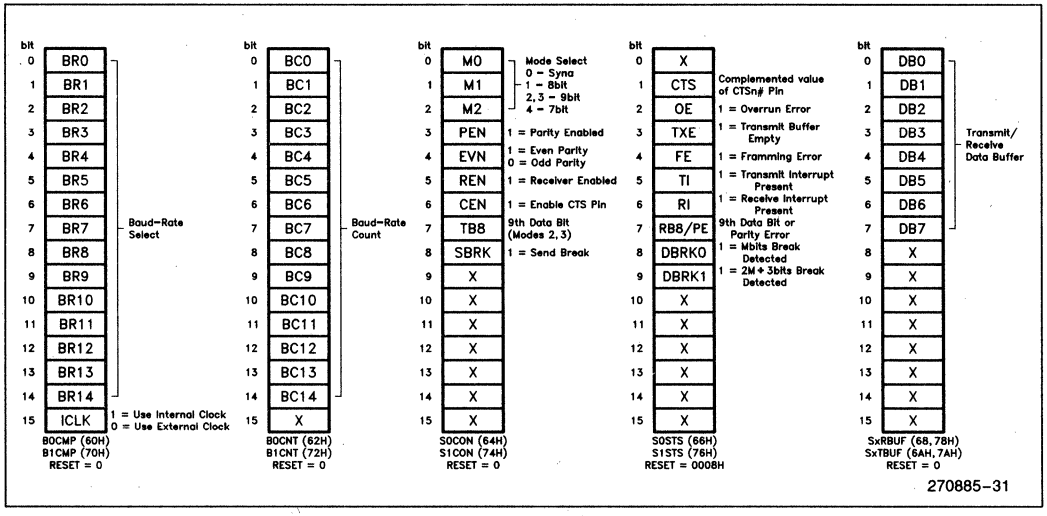

Figure 28. Serial Communications Unit Registers

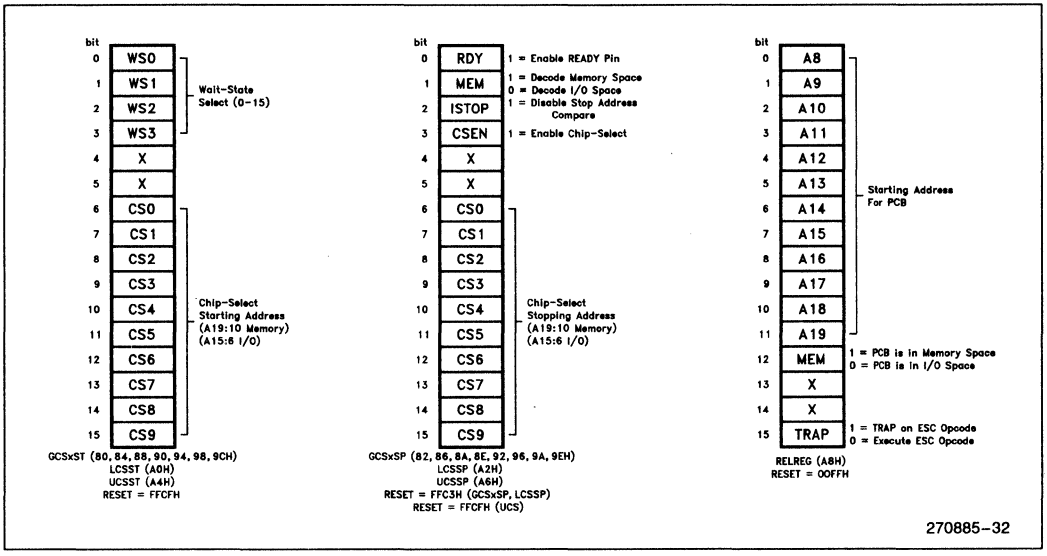

Figure 29. Chip-Select Unit Registers

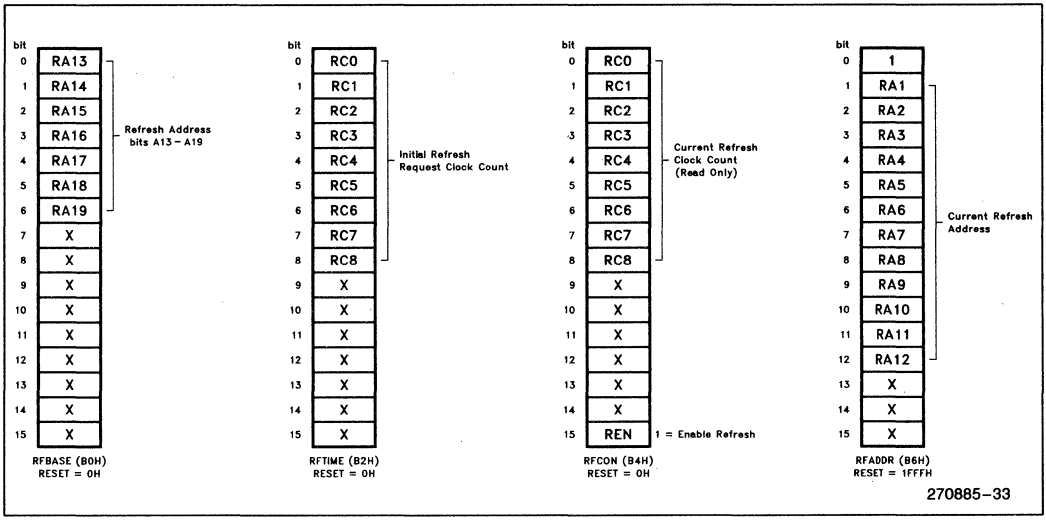

Figure 30. Refresh Control Unit Registers

24

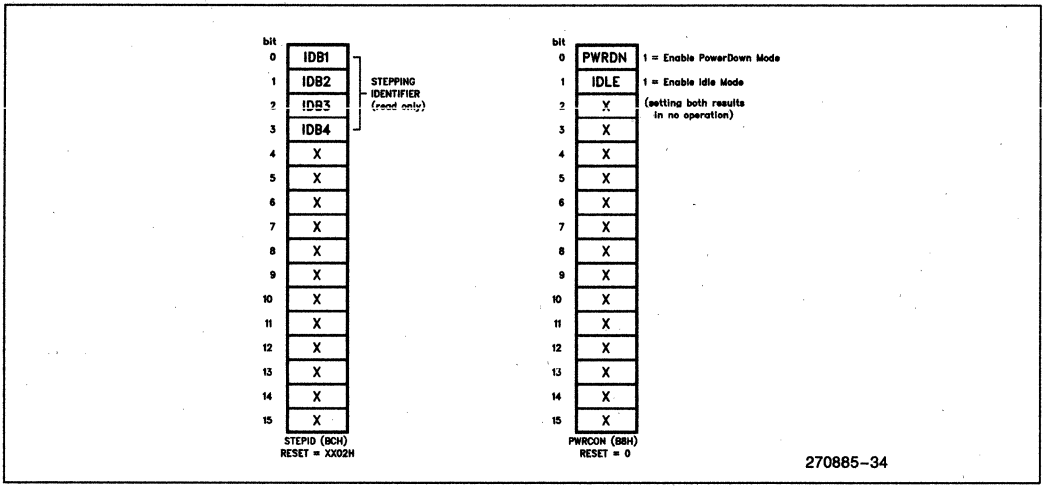

Figure 31. Power Management Unit Registers

80C188EB EXECUTION TIMINGS

A determination of 80C188EB program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

The 80C188EB 8-bit BIU is noticeably limited in its performance relative to the execution unit. A sufficient number of prefetched bytes may not reside in the prefetch queue much of the time. Therefore, actual program execution time will be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1000100w	mod reg r/m			2/12	
Register/memory to register	1000101w	mod reg r/m			2/9	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12–13	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3–4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8	
Accumulator to memory	1010001w	addr-low	addr-high		9	
Register/memory to segment register	10001110	mod 0 reg r/m			2/9	
Segment register to register/memory	10001100	mod 0 reg r/m			2/11	
PUSH = Push:						
Memory	11111111	mod 1 1 0 r/m			16	
Register	01010 reg				10	
Segment register	000reg 110				9	
Immediate	011010s0	data	data if s=0		10	
PUSHA = Push All	01100000				36	
POP = Pop:						
Memory	10001111	mod 0 0 0 r/m			20	
Register	01011 reg				10	
Segment register	000reg 111	(reg≠01)			8	
POPA = Pop All	01100001				51	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10	
Variable port	1110110w				8	
OUT = Output to:						
Fixed port	1110011w	port			9	
Variable port	1110111w				7	
XLAT = Translate byte to AL	11010111				11	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		18	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		18	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				9	
POPF = Pop flags	10011101				8	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10	
Register with register/memory	0011100w	mod reg r/m			3/10	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26–28	
Register-Word					35–37	
Memory-Byte					32–34	
Memory-Word					41–43	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
ARITHMETIC (Continued)			
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w | mod 1 0 1 r/m		
Register-Byte		25–28	
Register-Word		34–37	
Memory-Byte		31–34	
Memory-Word		40–43	
IMUL = Integer immediate multiply (signed)	0 1 1 0 1 0 s 1 | mod reg r/m | data | data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w | mod 1 1 0 r/m		
Register-Byte		29	
Register-Word		38	
Memory-Byte		35	
Memory-Word		44	
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w | mod 1 1 1 r/m		
Register-Byte		44–52	
Register-Word		53–61	
Memory-Byte		50–58	
Memory-Word		59–67	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0	19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1 | 0 0 0 0 1 0 1 0	15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0	2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1	4	
LOGIC			
Shift/Rotate Instructions:			
Register/Memory by 1	1 1 0 1 0 0 0 w | mod TTT r/m	2/15	
Register/Memory by CL	1 1 0 1 0 0 1 w | mod TTT r/m	5+n/17+n	
Register/Memory by Count	1 1 0 0 0 0 0 w | mod TTT r/m | count	5+n/17+n	
	TTT Instruction 0 0 0 ROL 0 0 1 ROR 0 1 0 RCL 0 1 1 RCR 1 0 0 SHL/SAL 1 0 1 SHR 1 1 1 SAR		
AND = **And:**			
Reg/memory and register to either	0 0 1 0 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 0 0 r/m | data | data if w=1	4/16	
Immediate to accumulator	0 0 1 0 0 1 0 w | data | data if w=1	3/4	8/16-bit
TEST = **And function to flags, no result:**			
Register/memory and register	1 0 0 0 0 1 0 w | mod reg r/m	3/10	
Immediate data and register/memory	1 1 1 1 0 1 1 w | mod 0 0 0 r/m | data | data if w=1	4/10	
Immediate data and accumulator	1 0 1 0 1 0 0 w | data | data if w=1	3/4	8/16-bit
OR = **Or:**			
Reg/memory and register to either	0 0 0 0 1 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 0 0 1 r/m | data | data if w=1	4/16	
Immediate to accumulator	0 0 0 0 1 1 0 w | data | data if w=1	3/4	8/16-bit

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
XOR = Exclusive or:						
Reg/memory and register to either	001100dw	mod reg r/m			3/10	
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	4/16	
Immediate to accumulator	0011010w	data	data if w=1		3/4	8/16-bit
NOT = Invert register/memory	1111011w	mod 010 r/m			3/10	
STRING MANIPULATION						
MOVS = Move byte/word	1010010w				14	
CMPS = Compare byte/word	1010011w				22	
SCAS = Scan byte/word	1010111w				15	
LODS = Load byte/wd to AL/AX	1010110w				12	
STOS = Store byte/wd from AL/AX	1010101w				10	
INS = Input byte/wd from DX port	0110110w				14	
OUTS = Output byte/wd to DX port	0110111w				14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	11110010	1010010w			8+8n	
CMPS = Compare string	1111001z	1010011w			5+22n	
SCAS = Scan string	1111001z	1010111w			5+15n	
LODS = Load string	11110010	1010110w			6+11n	
STOS = Store string	11110010	1010101w			6+9n	
INS = Input string	11110010	0110110w			8+8n	
OUTS = Output string	11110010	0110111w			8+8n	
CONTROL TRANSFER						
CALL = Call:						
Direct within segment	11101000	disp-low	disp-high		15	
Register/memory indirect within segment	11111111	mod 010 r/m			13/19	
Direct intersegment	10011010	segment offset			23	
		segment selector				
Indirect intersegment	11111111	mod 011 r/m	(mod ≠ 11)		38	
JMP = Unconditional jump:						
Short/long	11101011	disp-low			14	
Direct within segment	11101001	disp-low	disp-high		14	
Register/memory indirect within segment	11111111	mod 100 r/m			11/17	
Direct intersegment	11101010	segment offset			14	
		segment selector				
Indirect intersegment	11111111	mod 101 r/m	(mod ≠ 11)		26	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
RET = **Return from CALL:**						
Within segment	11000011				16	
Within seg adding immed to SP	11000010	data-low	data-high		18	
Intersegment	11001011				22	
Intersegment adding immediate to SP	11001010	data-low	data-high		25	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110 000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22 + 16(n − 1)	
LEAVE = Leave Procedure	11001001				8	
INT = **Interrupt:**						
Type specified	11001101	type			47	
Type 3	11001100				45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110				48/4	
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33–35	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

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INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	
	(TTT LLL are opcode to processor extension)		

Shaded areas indicate instructions not available in 8086/8088 microsystems.

FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

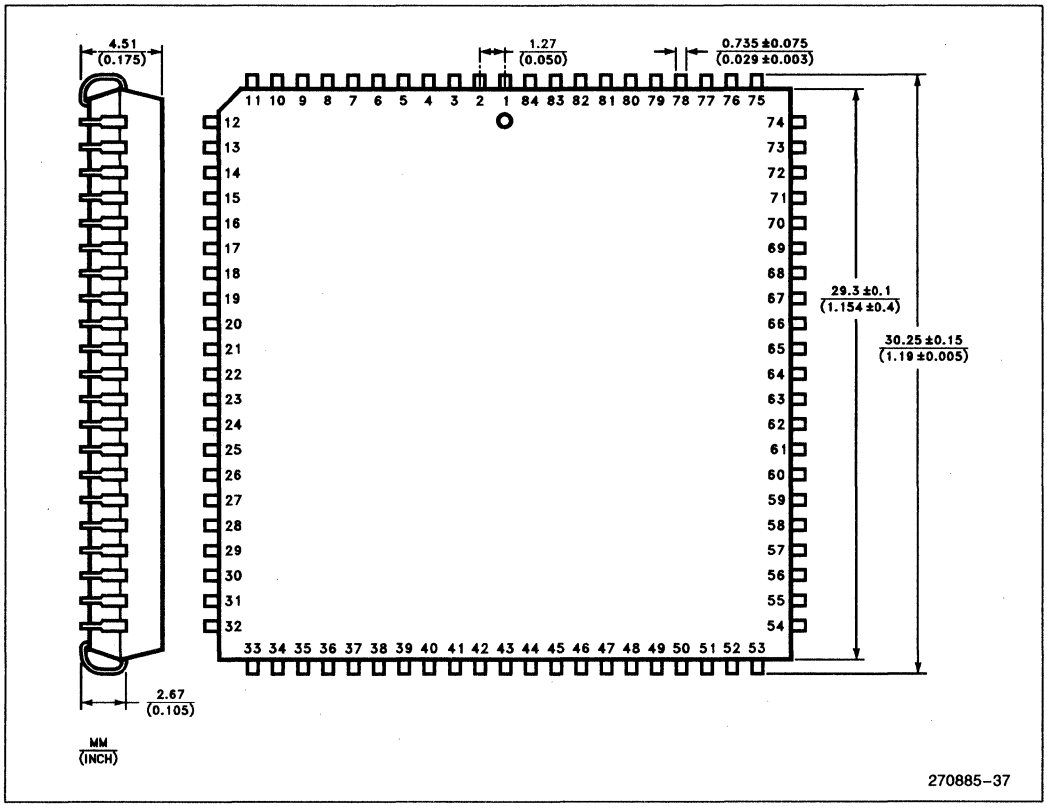

Figure 32. PLCC Principal Dimensions

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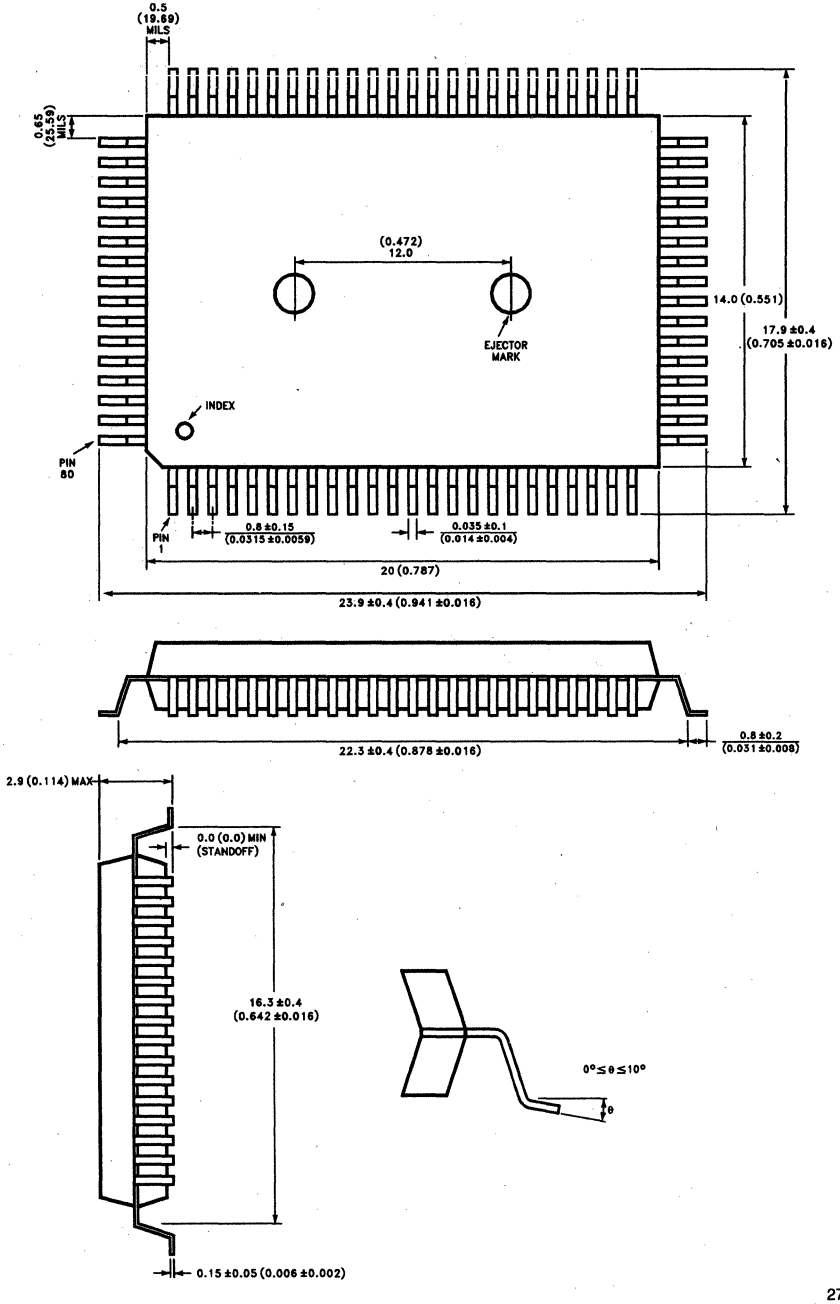

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NOTE:
Units are mm (inches) unless specified.

Figure 33. QFP Principal Dimensions

ERRATA

An 80C188EB with a STEPID value of 0001H has the following known errata. A device with a STEPID of 0001H can be visually identified by noting the **absence** of an alpha character next to the FPO number or by the **presence** of an **"A"** alpha character next to the FPO number. The FPO number location is shown in Figures 5 and 6.

1. A19/$\overline{\text{ONCE}}$ is not latched by the rising edge of $\overline{\text{RESIN}}$. A19/$\overline{\text{ONCE}}$ must remain active (LOW) at all times to remain in the ONCE™ Mode. Removing A19/$\overline{\text{ONCE}}$ after $\overline{\text{RESIN}}$ is high will return all output pins to a driving state, however, the 80C188EB will remain in a reset state.
2. During interrupt acknowledge (INTA) bus cycles, the bus controller will ignore the state of the READY pin if the previous bus cycle ignored the state of the READY pin. This errata can only occur if the Chip-Select Unit is being used. All active chip-selects must be programmed to use READY (RDY bit must be programmed to a 1) if wait-states are required for INTA bus cycles.
3. CLKOUT will transition off the **rising** edge of CLKIN rather than the falling edge of CLKIN. This does not affect any bus timings other than T_{CICO}.
4. $\overline{\text{RESIN}}$ has a hysterisis of only 130 mV. It is recommended that $\overline{\text{RESIN}}$ be driven with a Schmitt triggered device to avoid processor lockup during reset when using an RC circuit.
5. SINT1 will only go active for one clock period when a receive or transmit interrupt is pending (i.e., it does not remain active until the S1STS register is read). If SINT1 is to be connected to any of the 80C188EB interrupt lines (INT0–INT4), then it must be latched by user logic.

An 80C188EB with a STEPID value of 0001H or 0002H has the following known errata. Otherwise, an 80C188EB with a STEPID value of 0002H has no known errata (as of this publication). A device with a STEPID of 0002H can be visually identified by noting the presence of a "B" or "C" alpha character next to the FPO number. The FPO number location is shown in Figures 5 and 6.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the $\overline{\text{INTA1}}$ line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistantly, it is dependent on interrupt timing.

REVISION HISTORY

The following changes have been made between the -001 version and this -002 version of the 80C188EB data sheet. This -002 data sheet applies to any 80C188EB with a "B" alpha character after the FPO number. The FPO number location is shown in Figures 5 and 6.

1. The data sheet was changed from a Product Preview version to an Advanced Information version.
2. Figures 1, 5, 6, 8, 12, 17, 19, 20, 21, 22, 23, 29, and 31 and Table 1 were updated to correct for errors.
3. The DC specifications table has changed. Also, notes 3, 4 and 5 have been changed/added.
4. Graphs for I_{CC} versus Frequency have been changed to equations with supporting text.
5. Graphs for PDTMR pin capacitance have been changed to equations with supporting text.
6. AC Hold timings have been changed from 0 ns to 3 ns.
7. READY input setup time has been changed from 13 ns to 10 ns.
8. Serial port MODE 0 timings have been changed.
9. Various typing errors have been corrected throughout the document.

The following changes were made between the -002 and -003 versions of the 80C188EB data sheets. The -003 data sheet applies to any 80C188EB with a "B" alpha character after the FPO number. The FPO number location is shown in Figures 5 and 6.

1. 20 MHz Electrical, DC and AC Specifications were added to the appropriate sections.
2. The following 80C186EB Core Architecture sections were deleted:
   Register Set
   Instruction Set
   Memory Organization
   Addressing Modes
   Data Types
   Interrupts
3. Most of the 80C188EB Peripheral Architecture sections were condensed along with the Register Bit Summary section.
4. Most of the Tables and Figures have been renumbered due to edits.

80C188EC-16, -13
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSOR

- **Full Static Operation**
- **True CMOS Inputs and Outputs**
- **−40°C to +85°C Operating Temperature Range**

- **Integrated Feature Set:**
  - **Low-Power, Static, Enhanced 8088 CPU Core**
  - **Two Independent DMA Supported UARTs, each with an Integral Baud Rate Generator**
  - **Four Independent DMA Channels**
  - **24 Multiplexed I/O Port Pins**
  - **Two 8259A Compatible Programmable Interrupt Controllers**
  - **Three Programmable 16-Bit Timer/ Counters**
  - **32-Bit Watchdog Timer**
  - **Ten Programmable Chip Selects with Integral Wait-State Generator**
  - **Memory Refresh Control Unit**
  - **Power Management Unit**
  - **On-Chip Oscillator**
  - **System Level Testing Support (ONCE™ Mode)**
- **Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O**
- **Low-Power Operating Modes:**
  - **Idle Mode Freezes CPU Clocks but Keeps Peripherals Active**
  - **Powerdown Mode Freezes All Internal Clocks**
  - **Powersave Mode Divides All Clocks by Programmable Prescalar**
- **Complete System Development Support**
  - **ASM86 Assembler, PL/M 86, Pascal86, Fortran 86, iC-86 and System Utilities**
  - **In-Circuit Emulator (ICE™-186EC)**
- **Package Types:**
  - **100-Pin EIAJ Quad Flat Pack (QFP) (S80C188EC)**
  - **100-Pin Plastic Quad Flat Pack (PQFP) (KU80C188EC)**
- **Speed Versions Available:**
  - **16 MHz (80C188EC-16)**
  - **13 MHz (80C188EC-13)**

The 80C188EC is a member of the 186 Integrated Processor Family. The 186 Integrated Processor Family incorporates several different VLSI devices all of which share a common CPU architecture: the 8086/8088. The 80C188EC uses the latest high density CHMOS technology to integrate several of the most common system peripherals with an enhanced 8088 CPU core to create a powerful system on a single monolithic silicon die.

June 1992
Order Number: 272076-002

80C188EC-16, -13
16-Bit High Integration Embedded Processor

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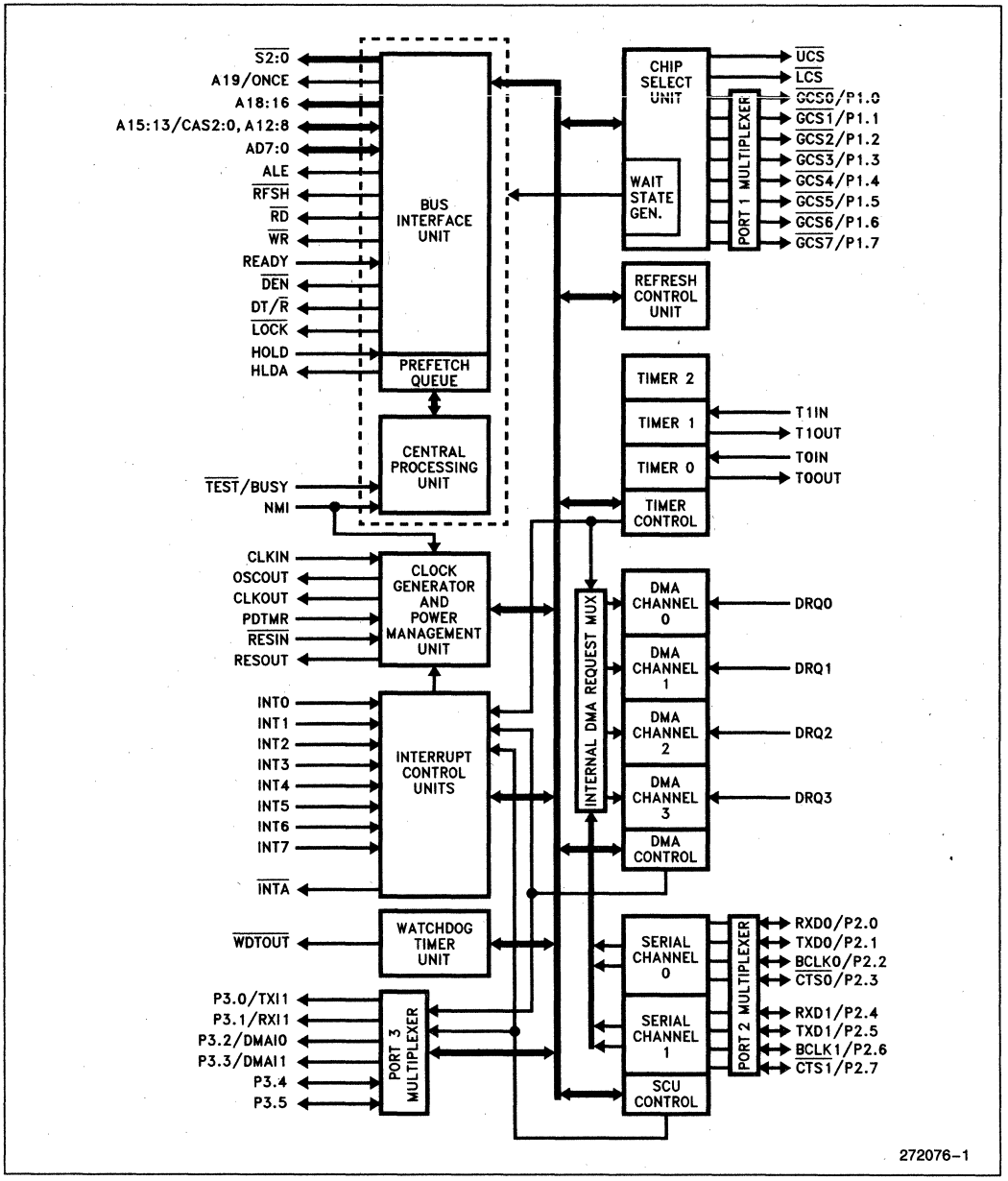


Figure 1. 80C188EC Block Diagram

INTRODUCTION

The 186 Integrated Processor Family incorporates a wide range of VLSI devices tailored to suit the needs of embedded system designers. All 186 Family devices share a common CPU architecture: the industry standard 8086/8088. Code developed on other "X86" platforms can be ported with little or no modification to any of the 186 Integrated Processor Family devices.

Each of the 186 Integrated Processor Family devices adds a full complement of peripherals to the 8086/8088 CPU core. The type of peripherals and level of integration vary between family members. A complete 186 Family system can often be designed with just the addition of RAM, ROM and simple glue logic. The space savings afforded by high-integration are critical as designers continue to strive for smaller size and portability.

The 80C188EC is one of the highest integration members of the 186 Integrated Processor Family. Two serial ports are provided for services such as interprocessor communication, diagnostics and modem interfacing. Four DMA channels allow for high speed data movement as well as support of the onboard serial ports. A flexible chip select unit simplifies memory and peripheral interfacing. The three general purpose timer/counters can be used for a variety of time measurement and waveform generation tasks. A watchdog timer is provided to insure system integrity even in the most hostile of environments. Two 8259A compatible interrupt controllers handle internal interrupts, and, up to 57 external interrupt requests. A DRAM refresh unit and 24 multiplexed I/O ports round out the feature set of the 80C188EC.

OVERVIEW

Figure 1 shows a block diagram of the 80C188EC. The execution unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhanced execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instructions and full static operation. The bus interface unit (BIU) is the same as that found on the original 186 family products, except the queue-status mode has been deleted and buffer interface control has been changed to ease system design timings. An independent internal bus is used for communication between the BIU and on-chip peripherals.

80C188EC CORE ARCHITECTURE

Bus Interface Unit

The 80C188EC core incorporates a bus controller that generates local bus control signals. In addition, it employs a HOLD/HLDA protocol to share the local bus with other bus masters.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information and data (for write operations) information. It is also responsible for reading data from the local bus during a read operation. A ready input pin is provided to extend a bus cycle beyond the minimum four states (clocks).

The 80C188EC bus controller also generates two control signals ($\overline{DEN}$) and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus.

Clock Generator

The 80C188EC provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter and three low-power operating modes.

The oscillator circuit is designed to be used with either a parallel resonant fundamental or third-overtone mode crystal network. Alternatively, the oscillator circuit may be driven from an external clock source. Figure 2 shows the various operating modes of the 80C188EC oscillator circuit.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide-by-two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC timings are referenced to CLKOUT.

The following parameters are recommended when choosing a crystal:

Temperature Range:	Application Specific
ESR (Equivalent Series Res.):	40Ω max
C0 (Shunt Capacitance of Crystal):	7.0 pF max
C_L (Load Capacitance):	20 pF ±2 pF
Drive Level:	1 mW (max)

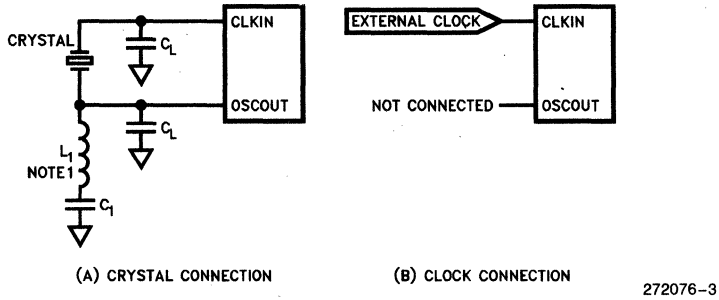
80C188EC Peripheral Architecture

The 80C188EC integrates several common system peripherals with a CPU core to create a compact, yet powerful system. The integrated peripherals are designed to be flexbile and provide logical interconnections between supporting units (e.g., the DMA unit can accept requests from the Serial Communications Unit).

The list of integrated peripherals includes:

- Two cascaded, 8259A compatible, Programmable Interrupt Controllers
- 3-Channel Timer/Counter Unit
- 2-Channel Serial Communications Unit
- 4-Channel DMA Unit
- 10-Output Chip-Select Unit
- 32-bit Watchdog Timer Unit
- I/O Port Unit
- Refresh Control Unit
- Power Management Unit

The registers associated with each integrated peripheral are contained within a 128 x 16-bit register file called the Peripheral Control Block (PCB). The base address of the PCB is programmable and can be located on any 256 byte address boundary in either memory or I/O space.



NOTE:
1. The LC network is only required when using a third overtone crystal.

Figure 2. 80C188EC Clock Connections

Figure 3 provides a list of the registers associated with the PCB. The Register Bit Summary individually lists all of the registers and identifies each of their programming attributes.

Programmable Interrupt Controllers

The 80C188EC utilizes two 8259A compatible Programmable Interrupt Controllers (PIC) to manage both internal and external interrupts. The 8259A modules are configured in a master/slave arrangement.

Seven of the external interrupt pins, INT0 through INT6, are connected to the master 8259A module. The eighth external interrupt pin, INT7, is connected to the slave 8259A module.

There are a total of 11 internal interrupt sources from the integrated peripherals: 4 Serial, 4 DMA, and 3 Timer/Counter.

Timer/Counter Unit

The 80C188EC Timer/Counter Unit (TCU) provides three 16-bit programmable timers. Two of these are highly flexible and are connected to external pins for external control or clocking. The third timer is not connected to any external pins and can only be clocked internally. However, it can be used to clock the other two timer channels. The TCU can be used to count external events, time external events, generate non-repetitive waveforms or generate timed interrupts.

Serial Communications Unit

The Serial Communications Unit (SCU) of the 80C188EC contains two independent channels. Each channel is identical in operation except that only channel 0 is directly supported by the integrated interrupt controller (the channel 1 interrupts are routed to external interrupt pins). Each channel has its own baud rate generator and can be internally or externally clocked up to one half the 80C188EC operating frequency. Both serial channels can request service from the DMA unit thus providing block reception and transmission without CPU intervention.

Independent baud rate generators are provided for each of the serial channels. For the asynchronous modes, the generator supplies an 8x baud clock to both the receive and transmit shifting register logic. A 1x baud clock is provided in the synchronous mode.

PCB Offset	Function
00H	Master PIC Port 0
02H	Master PIC Port 1
04H	Slave PIC Port 0
06H	Slave PIC Port 1
08H	Reserved
0AH	SCU Int. Req. Ltch.
0CH	DMA Int. Req. Ltch.
0EH	TCU Int. Req. Ltch.
10H	Reserved
12H	Reserved
14H	Reserved
16H	Reserved
18H	Reserved
1AH	Reserved
1CH	Reserved
1EH	Reserved
20H	WDT Reload High
22H	WDT Reload Low
24H	WDT Count High
26H	WDT Count Low
28H	WDT Clear
2AH	WDT Disable
2CH	Reserved
2EH	Reserved
30H	T0 Count
32H	T0 Compare A
34H	T0 Compare B
46H	T0 Control
38H	T1 Count
3AH	T1 Compare A
3CH	T1 Compare B
3EH	T1 Control

PCB Offset	Function
40H	T2 Count
42H	T2 Compare
44H	Reserved
46H	T2 Control
48H	Port 3 Direction
4AH	Port 3 Pin State
4CH	Port 3 Mux Control
4EH	Port 3 Data Latch
50H	Port 1 Direction
52H	Port 1 Pin State
54H	Port 1 Mux Control
56H	Port 1 Data Latch
58H	Port 2 Direction
5AH	Port 2 Pin State
5CH	Port 2 Mux Control
5EH	Port 2 Data Latch
60H	SCU 0 Baud
62H	SCU 0 Count
64H	SCU 0 Control
66H	SCU 0 Status
68H	SCU 0 RBUF
6AH	SCU 0 TBUF
6CH	Reserved
6EH	Reserved
70H	SCU 1 Baud
72H	SCU 1 Count
74H	SCU 1 Control
76H	SCU 1 Status
78H	SCU 1 RBUF
7AH	SCU 1 TBUF
7CH	Reserved
7EH	Reserved

PCB Offset	Function
80H	GCS0 Start
82H	GCS0 Stop
84H	GCS1 Start
86H	GCS1 Stop
88H	GCS2 Start
8AH	GCS2 Stop
8CH	GCS3 Start
8EH	GCS3 Stop
90H	GCS4 Start
92H	GCS4 Stop
94H	GCS5 Start
96H	GCS5 Stop
98H	GCS6 Start
9AH	GCS6 Stop
9CH	GCS7 Start
9EH	GCS7 Stop
A0H	LCS Start
A2H	LCS Stop
A4H	UCS Start
A6H	UCS Stop
A8H	Relocation Register
AAH	Reserved
ACH	Reserved
AEH	Reserved
B0H	Refresh Base Addr.
B2H	Refresh Time
B4H	Refresh Control
B6H	Refresh Address
B8H	Power Control
BAH	Reserved
BCH	Step ID
BEH	Powersave

PCB Offset	Function
C0H	DMA 0 Source Low
C2H	DMA 0 Source High
C4H	DMA 0 Dest. Low
C6H	DMA 0 Dest. High
C8H	DMA 0 Count
CAH	DMA 0 Control
CCH	DMA Module Pri.
CEH	DMA Halt
D0H	DMA 1 Source Low
D2H	DMA 1 Source High
D4H	DMA 1 Dest. Low
D6H	DMA 1 Dest. High
D8H	DMA 1 Count
DAH	DMA 1 Control
DCH	Reserved
DEH	Reserved
E0H	DMA 2 Source Low
E2H	DMA 2 Source High
E4H	DMA 2 Dest. Low
E6H	DMA 2 Dest. High
E8H	DMA 2 Count
EAH	DMA 2 Control
ECH	Reserved
EEH	Reserved
F0H	DMA 3 Source Low
F2H	DMA 3 Source High
F4H	DMA 3 Dest. Low
F6H	DMA 3 Dest. High
F8H	DMA 3 Count
FAH	DMA 3 Control
FCH	Reserved
FEH	Reserved

Figure 3. 80C188EC Peripheral Control Block Registers

DMA Unit

The four channel Direct Memory Access (DMA) Unit is comprised of two modules with two channels each. All four channels are identical in operation. DMA transfers can take place from memory to memory, I/O to memory, memory to I/O or I/O to I/O. DMA requests can be external (on the DRQ pins), internal (from Timer 2 or a serial channel) or software initiated.

The DMA unit transfers data as bytes only. Each data transfer requires two bus cycles, one to fetch data and one to deposit. The minimum clock count for each transfer is 8, but this will vary depending on synchronization and wait states.

Chip-Select Unit

The 80C188EC Chip-Select Unit (CSU) integrates logic which provides up to ten programmable chip-selects to access both memories and peripherals. In addition, each chip-select can be programmed to automatically insert additional clocks (wait states) into the current bus cycle, and/or automatically terminate a bus cycle independent of the condition of the READY input pin.

I/O Port Unit

The I/O Port Unit on the 80C188EC supports two 8-bit channels and one 6-bit channel of input, output or input/output operation. Port 1 is multiplexed with the chip select pins and is output only. Port 2 is multiplexed with the pins for serial channels 1 and 2. All Port 2 pins are input/output. Port 3 has a total of 6 pins: four that are multiplexed with DMA and serial port interrupts and two that are non-multiplexed, open drain I/O.

Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates a periodic memory read bus cycle to keep dynamic or pseudo-static memory refreshed. A 9-bit counter controls the number of clocks between refresh requests. A 12-bit address generator is maintained by the RCU and is presented on the A12:1 address lines during the refresh bus cycle. Address bits A19:13 are programmable to allow the refresh address block to be located on any 8 Kbyte boundary.

Watchdog Timer Unit

The Watchdog Timer Unit (WDT) allows for graceful recovery from unexpected hardware and software upsets. The WDT consists of a 32-bit counter that decrements every clock cycle. If the counter reaches zero before being reset, the $\overline{\text{WDTOUT}}$ pin is pulled low for four clock cycles. Logically ANDing the $\overline{\text{WDTOUT}}$ pin with the power-on reset signal allows the WDT to reset the device in the event of a WDT timeout. If a less drastic method of recovery is desired, $\overline{\text{WDTOUT}}$ can be connected directly to NMI or one of the INT input pins. The WDT may also be used as a general purpose timer.

Power Management Unit

The 80C188EC Power Management Unit (PMU) is provided to control the power consumption of the device. The PMU provides four power management modes: Active, Powersave, Idle and Powerdown.

Active Mode indicates that all units on the 80C188EC are operating at ½ the CLKIN frequency.

Idle Mode freezes the clocks of the Execution and Bus units at a logic zero state (all peripherals continue to operate normally).

The Powerdown Mode freezes all internal clocks at a logic zero level and disables the crystal oscillator.

In Powersave Mode, all internal clock signals are divided by a programmable prescalar (up to $\frac{1}{64}$ the normal frequency). Powersave Mode can be used with Idle Mode as well as during normal (Active Mode) operation.

ONCE™ Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the 80C188EC has a test mode available which forces all output and input/output pins to be placed in the high-impedance state. ONCE stands for "ON Circuit Emulation". The ONCE mode is selected by forcing the A19/S6/$\overline{\text{ONCE}}$ pin low during a processor reset (this pin is weakly held high during reset to prevent inadvertant entrance into ONCE Mode).

PACKAGE INFORMATION

This section describes the pin functions, pinout and thermal characteristics for the 80C188EC in both the Plastic Quad Flat Pack (JEDEC PQFP) and the EIAJ Quad Flat Pack (QFP). For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

Pin Descriptions

Each pin or logical set of pins is described in Table 2. There are four columns for each entry in the Pin Description Table. The following sections describe each column.

Column 1: Pin Name

In this column is a mnemonic that describes the pin function. Negation of the signal name (i.e. $\overline{\text{RESIN}}$) implies that the signal is active low.

Column 2: Pin Type

A pin may be either power (P), ground (G), input only (I), output only (O) or input/output (I/O). Please note that some pins have more than 1 function. A19/S6/$\overline{\text{ONCE}}$, for example, is normally an output but functions as an input during reset. For this reason A19/S6/$\overline{\text{ONCE}}$ is classified as an input/output pin.

Column 3: Input Type (for I and I/O types only)

There are two different types of input pins on the 80C188EC: asynchronous and synchronous. **Asynchronous** pins require that setup and hold times be met only to *guarantee recognition*. **Synchronous** input pins require that the setup and hold times be met to *guarantee proper operation*. Stated simply, missing a setup or hold on an asynchronous pin will result in something minor (i.e. a timer count will be missed) whereas missing a setup or hold on a synchronous pin will result in system failure (the system will "lock up").

An input pin may also be edge or level sensitive.

Column 4: Output States (for O and I/O types only)

The state of an output or I/O pin is dependent on the operating mode of the device. There are four modes of operation that are different from normal active mode: Bus Hold, Reset, Idle Mode, Powerdown Mode. This column describes the output pin state in each of these modes.

The legend for interpreting the information in the Pin Descriptions is shown in Table 1.

As an example, please refer to the table entry for AD12:0. The "I/O" signifies that the pins are bidirectional (i.e. have both an input and output function). The "S" indicates that, as an input the signal must be synchronized to CLKOUT for proper operation. The "H(Z)" indicates that these pins will float while the processor is in the Hold Acknowledge state. R(Z) indicates that these pins will float while $\overline{\text{RESIN}}$ is low. P(0) and I(0) indicate that these pins will drive 0 when the device is in either Powerdown or Idle Mode.

Some pins, the I/O Ports for example, can be programmed to perform more than one function. Multifunction pins have a "/" in their signal name between the different functions (i.e. P3.0/RXI1). If the input pin type or output pin state differ between functions, then that will be indicated by separating the state (or type) with a "/" (i.e. H(X)/H(Q)). In this example when the pin is configured as P3.0 then its hold output state is H(X); when configured as RXI1 its output state is H(Q).

All pins float while the processor is in the ONCE Mode (with the exception of OSCOUT).

Table 1. Pin Description Nomenclature

Symbol	Description
P	Power Pin (apply + V_{CC} voltage)
G	Ground (connect to V_{SS})
I	Input only pin
O	Output only pin
I/O	Input/Output pin
S(E)	Synchronous, edge sensitive
S(L)	Synchronous, level sensitive
A(E)	Asynchronous, edge sensitive
A(L)	Asynchronous, level sensitive
H(1)	Output driven to V_{CC} during bus hold
H(0)	Output driven to V_{SS} during bus hold
H(Z)	Output floats during bus hold
H(Q)	Output remains active during bus hold
H(X)	Output retains current state during bus hold
R(WH)	Output weakly held at V_{CC} during reset
R(1)	Output driven to V_{CC} during reset
R(0)	Output driven to V_{SS} during reset
R(Z)	Output floats during reset
R(Q)	Output remains active during reset
R(X)	Output retains current state during reset
I(1)	Output driven to V_{CC} during Idle Mode
I(0)	Output driven to V_{SS} during Idle Mode
I(Z)	Output floats during Idle Mode
I(Q)	Output remains active during Idle Mode
I(X)	Output retains current state during Idle Mode
P(1)	Output driven to V_{CC} during Powerdown Mode
P(0)	Output driven to V_{SS} during Powerdown Mode
P(Z)	Output floats during Powerdown Mode
P(Q)	Output remains active during Powerdown Mode
P(X)	Output retains current state during Powerdown Mode

Table 2. 80C188EC Pin Descriptions

Pin Name	Pin Type	Input Type	Output States	Pin Description
V_{CC}	P	—	—	**POWER** +5V ±10% power supply connection
V_{SS}	G	—	—	**GROUND**
CLKIN	I	A(E)	—	**CLocK INput** is the external clock input. An external oscillator operating at two times the required 80C188EC operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O	—	H(Q) R(Q) I(Q) P(X)	**OSCillator OUTput** is only used when using a crystal to generate the internal clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin can not be used as 2X clock output for non-crytsal applications (i.e. this pin is not connected for non-crystal applications).
CLKOUT	O	—	H(Q) R(Q) I(Q) P(X)	**CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transitions every falling edge of CLKIN.
$\overline{RESIN}$	I	A(L)	—	**RESet IN** causes the 80C188EC to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the 80C188EC begins fetching opcodes at memory location 0FFFF0H.
RESOUT	O	—	H(0) R(1) I(0) P(0)	**RESet OUTput** that indicates the 80C188EC is currently in the reset state. RESOUT will remain active as long as $\overline{RESIN}$ remains active.
PDTMR	I/O	A(L)	H(WH) R(Z) P(WH) I(WH)	**Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the 80C188EC waits after an exit from Powerdown before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I	A(E)	—	**Non-Maskable Interrupt** input causes a TYPE-2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{TEST}$	I	A(E)	—	**TEST** is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (LOW).
A19/S6/$\overline{ONCE}$	I/O	A(L)	H(Z) R(WH) I(0) P(0)	This pin drives address bit 19 during the address phase of the bus cycle. During T2 and T3 this pin functions as status bit 6. S6 is low to indicate CPU bus cycles and high to indicate DMA or refresh bus cycles. During a processor reset ($\overline{RESIN}$ active) this pin becomes the ONCE input pin. Holding this pin low during reset will force the part into ONCE Mode.

Table 2. 80C188EC Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
A18/S5 A17/S4 A16/S3	I/O	A(L)	H(Z) R(WH) I(0) P(0)	These pins drive address information during the address phase of the bus cycle. During T2 and T3 these pins drive status information (which is always 0 on the 80C188EC). These pins are used as inputs during factory test; driving these pins low during reset will cause unspecified operation.
A15/CAS2 A14/CAS1 A13/CAS0 A12:8	I/O	S(L)	H(Z) R(Z) I(0) P(0)	These pins are part of the ADDRESS bus. During the address phase of the bus cycle, address bits 15 through 8 are presented on these pins and can be latched using ALE. Pins AD15:13/CAS2:0 drive the 82C59 slave address information during interrupt acknowledge cycles.
AD7:0	I/O	S(L)	H(Z) R(Z) I(0) P(0)	These pins provide a multiplexed ADDRESS and DATA bus. During the address phase of the bus cycle, address bits 0 through 7 are presented on the bus and can be latched using ALE. 8-bit data information is transferred during the data phase of the bus cycle.
$\overline{S2:0}$	O	—	H(Z) R(1) I(1) P(1)	Bus cycle Status are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ **Bus Cycle Initiated** 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Instruction Queue Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive (No bus activity)
ALE	O	—	H(0) R(0) I(0) P(0)	**Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle.
$\overline{RFSH}$	O	—	H(Z) R(Z) I(1) P(1)	**ReFreSH** output signals that a refresh bus cycle is in progress.
$\overline{RD}$	O	—	H(Z) R(Z) I(1) P(1)	**ReaD** output signals that the accessed memory or I/O device should drive data information onto the data bus.

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Table 2. 80C188EC Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
$\overline{WR}$	O	—	H(Z) R(Z) I(1) P(1)	**WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device.
READY	I	A(L) S(L) (Note 1)	—	**READY** input to signal the completion of a bus cycle. READY must be active to terminate any 80C188EC bus cycle, unless it is ignored by correctly programming the Chip-Select unit.
$\overline{DEN}$	O	—	H(Z) R(Z) I(1) P(1)	**Data ENable** output to control the enable of bi-directional transceivers when buffering a 80C188EC system. $\overline{DEN}$ is active only when data is to be transferred on the bus.
DT/$\overline{R}$	O	—	H(Z) R(Z) I(X) P(X)	**Data Transmit/Receive** output controls the direction of a bi-directional buffer when buffering an 80C188EC system.
$\overline{LOCK}$	I/O	A(L)	H(Z) R(Z) I(X) P(X)	**LOCK** output indicates that the bus cycle in progress is not interruptable. The 80C188EC will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low.
HOLD	I	A(L)	—	**HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The 80C188EC will relinquish control of the local bus between instruction boundaries that are not LOCKed.
HLDA	O	—	H(1) R(0) I(0) P(0)	**HoLD Acknowledge** output to indicate that the 80C188EC has relinquished control of the local bus. When HLDA is asserted, the 80C188EC will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly.
$\overline{UCS}$	O	—	H(1) R(1) I(1) P(1)	**Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address range programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH.

Table 2. 80C188EC Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
$\overline{LCS}$	O	—	H(1) R(1) I(1) P(1)	**Lower Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address range programmed by the user. $\overline{LCS}$ is inactive after a reset.
P1.0/$\overline{GCS0}$ P1.1/$\overline{GCS1}$ P1.2/$\overline{GCS2}$ P1.3/$\overline{GCS3}$ P1.4/$\overline{GCS4}$ P1.5/$\overline{GCS5}$ P1.6/$\overline{GCS6}$ P1.7/$\overline{GCS7}$	O	—	H(X)/H(1) R(1) I(X)/I(1) P(X)/P(1)	These pins provide a multiplexed function. If enabled, each pin can provide a **General purpose Chip Select** output which will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. When not programmed as a Chip-Select, each pin may be used as a general purpose output port.
T0OUT T1OUT	O	—	H(Q) R(1) I(Q) P(X)	**Timer OUTput** pins can be programmed to provide single clock or continuous waveform generation, depending on the timer mode selected.
T0IN T1IN	I	A(L) A(E)	—	**Timer INput** is used either as clock or control signals, depending on the timer mode selected. This pin may be either level or edge sensitive depending on the programming mode.
INT7:0	I	A(L) A(E)	—	**Maskable INTerrupt** input will cause a vector to a specific Type interrupt routine. The INT6:0 pins can be used as cascade inputs from slave 8259A devices. The INT pins can be configured as level or edge sensitive.
$\overline{INTA}$	O	—	H(1) R(1) I(1) P(1)	**INTerrupt Acknowledge** output is a handshaking signal used by external 82C59A-2 Programmable Interrupt Controllers.
P3.5 P3.4	I/O	A(L)	H(X) R(Z) I(X) H(X)	Bidirectional, open-drain port pins.
P3.3/DMAI1 P3.2/DMAI0	O	—	H(X) R(0) I(Q) P(X)	**DMA Interrupt** output goes active to indicate that the channel has completed a transfer. DMAI1 and DMAI0 are multiplexed with output only port functions.
P3.1/TXI1	O	—	H(X)/H(Q) R(0) I(Q) P(X)	**Transmit Interrupt** output goes active to indicate that serial channel 1 has completed a transfer. TXI1 is multiplexed with an output only Port function.

Table 2. 80C188EC Pin Descriptions (Continued)

Pin Name	Pin Type	Input Type	Output States	Pin Description
P3.0/RXI1	O	—	H(X)/H(Q) R(0) I(Q) P(X)	**Receive Interrupt** output goes active to indicate that serial channel 1 has completed a reception. RXI1 is multiplexed with an output only port function.
$\overline{\text{WDTOUT}}$	O	—	H(Q) R(1) I(Q) P(X)	**WatchDog Timer OUTput** is driven low for four clock cycles when the watchdog timer reaches zero. $\overline{\text{WDTOUT}}$ may be ANDed with the power-on reset signal to reset the 80C188EC when the watchdog timer is not properly reset.
P2.7/$\overline{\text{CTS1}}$ P2.3/$\overline{\text{CTS0}}$	I/O	A(L)	H(X) R(Z) I(X) P(X)	**Clear-To-Send** input is used to prevent the transmission of serial data on the TXD signal pin. $\overline{\text{CTS1}}$ and $\overline{\text{CTS0}}$ are multiplexed with an I/O Port function.
P2.6/BCLK1 P2.2/BCLK0	I/O	A(L)/ A(E)	H(X) R(Z) I(X) P(X)	**Baud CLocK** input can be used as an alternate clock source for each of the integrated serial channels. The BCLK inputs are multiplexed with I/O Port functions. The BCLK input frequency cannot exceed ½ the operating frequency of the 80C188EC.
P2.5/TXD1 P2.1/TXD0	I/O	A(L)	H(Q) R(Z) I(X)/I(Q) P(X)	**Transmit Data** output provides serial data information. The TXD outputs are multiplexed with I/O Port functions. During synchronous serial communications, TXD will function as a clock output.
P2.4/RXD1 P2.0/RXD0	I/O	A(L)	H(X)/H(Q) R(Z) I(X)/I(Q) P(X)	**Receive Data** input accepts serial data information. The RXD pins are multiplexed with I/O Port functions. During synchronous serial communications, RXD is bi-directional and will become an output for transmission of data (TXD becomes the clock).
DRQ3:0	I	A(L)	—	**DMA ReQuest** input pins are used to request a DMA transfer. The timing of the request is dependent on the programmed synchronization mode.

NOTE:
1. READY is A(E) for the rising edge of CLKOUT, S(E) for the falling edge of CLKOUT.

80C188EC Pinout

Tables 3 and 4 list the 80C188EC pin names with package location for the 100-pin Plastic Quad Flat Pack (PQFP) component. Figure 4 depicts the complete 80C188EC pinout (PQFP) package as viewed from the top side of the component (i.e. contacts facing down).

Tables 5 and 6 list the 80C188EC pin names with package location for the 100-pin EIAJ Quad Flat Pack (QFP) component. Figure 5 depicts the complete 80C188EC (QFP package) as viewed from the top side of the component (i.e. contacts facing down).

Table 3. 80C188EC PQFP Pin Functions with Location

AD Bus	
Name	**Pin**
AD0	73
AD1	72
AD2	71
AD3	70
AD4	66
AD5	65
AD6	64
AD7	63
A8	60
A9	59
A10	58
A11	57
A12	56
A13/CAS0	55
A14/CAS1	54
A15/CAS2	53
A16/S3	77
A17/S4	76
A18/S5	75
A19/S6/$\overline{\text{ONCE}}$	74

No Connect
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Bus Control	
Name	**Pin**
ALE	52
$\overline{\text{RFSH}}$	51
$\overline{\text{S0}}$	78
$\overline{\text{S1}}$	79
$\overline{\text{S2}}$	80
$\overline{\text{RD}}$	50
$\overline{\text{WR}}$	49
READY	85
$\overline{\text{DEN}}$	47
DT/$\overline{\text{R}}$	46
$\overline{\text{LOCK}}$	48
HOLD	44
HLDA	45
$\overline{\text{INTA}}$	34

Power and Ground	
Name	**Pin**
V_{CC}	13
V_{CC}	14
V_{CC}	38
V_{CC}	62
V_{CC}	67
V_{CC}	69
V_{CC}	86
V_{SS}	12
V_{SS}	15
V_{SS}	37
V_{SS}	39
V_{SS}	61
V_{SS}	68
V_{SS}	87

Processor Control	
Name	**Pin**
$\overline{\text{RESIN}}$	8
RESOUT	7
CLKIN	10
OSCOUT	11
CLKOUT	6
$\overline{\text{TEST}}$	83
PDTMR	9
NMI	82
INT0	30
INT1	31
INT2	32
INT3	33
INT4	40
INT5	41
INT6	42
INT7	43

I/O	
Name	**Pin**
$\overline{\text{UCS}}$	88
$\overline{\text{LCS}}$	89
P1.7/$\overline{\text{GCS7}}$	90
P1.6/$\overline{\text{GCS6}}$	91
P1.5/$\overline{\text{GCS5}}$	92
P1.4/$\overline{\text{GCS4}}$	93
P1.3/$\overline{\text{GCS3}}$	94
P1.2/$\overline{\text{GCS2}}$	95
P1.1/$\overline{\text{GCS1}}$	96
P1.0/$\overline{\text{GCS0}}$	97
P2.7/$\overline{\text{CTS1}}$	23
P2.6/BCLK1	22
P2.5/TXD1	21
P2.4/RXD1	20
P2.3/$\overline{\text{CTS0}}$	19
P2.2/BCLK0	18
P2.1/TXD0	17
P2.0/RXD0	16
P3.5	29
P3.4	28
P3.3/DMAI1	27
P3.2/DMAI0	26
P3.1/TXI1	25
P3.0/RXI1	24
T0IN	3
T0OUT	2
T1IN	5
T1OUT	4
DRQ0	98
DRQ1	99
DRQ2	100
DRQ3	1
$\overline{\text{WDTOUT}}$	36

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Table 4. PQFP Pin Locations with Pin Name

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DRQ3	26	DMAI0/P3.2	51	$\overline{RFSH}$	76	A17/S4
2	T0OUT	27	DMAI1/P3.3	52	ALE	77	A16/S3
3	T0IN	28	P3.4	53	A15	78	$\overline{S0}$
4	T1OUT	29	P3.5	54	A14	79	$\overline{S1}$
5	T1IN	30	INT0	55	A13	80	$\overline{S2}$
6	CLKOUT	31	INT1	56	A12	81	V_{SS}
7	RESOUT	32	INT2	57	A11	82	NMI
8	$\overline{RESIN}$	33	INT3	58	A10	83	$\overline{TEST}$
9	PDTMR	34	$\overline{INTA}$	59	A9	84	V_{CC}
10	CLKIN	35	N.C.	60	A8	85	READY
11	OSCOUT	36	$\overline{WDTOUT}$	61	V_{SS}	86	V_{CC}
12	V_{SS}	37	V_{SS}	62	V_{CC}	87	V_{SS}
13	V_{CC}	38	V_{CC}	63	AD7	88	$\overline{UCS}$
14	V_{CC}	39	V_{SS}	64	AD6	89	$\overline{LCS}$
15	V_{SS}	40	INT4	65	AD5	90	P1.7/$\overline{GCS7}$
16	P2.0/RXD0	41	INT5	66	AD4	91	P1.6/$\overline{GCS6}$
17	P2.1/TXD0	42	INT6	67	V_{CC}	92	P1.5/$\overline{GCS5}$
18	P2.2/BCLK0	43	INT7	68	V_{SS}	93	P1.4/$\overline{GCS4}$
19	P2.3/$\overline{CTS0}$	44	HOLD	69	V_{CC}	94	P1.3/$\overline{GCS3}$
20	P2.4/RXD1	45	HLDA	70	AD3	95	P1.2/$\overline{GCS2}$
21	P2.5/TXD1	46	DT/$\overline{R}$	71	AD2	96	P1.1/$\overline{GCS1}$
22	P2.6/BCLK1	47	$\overline{DEN}$	72	AD1	97	P1.0/$\overline{GCS0}$
23	P2.7/$\overline{CTS1}$	48	$\overline{LOCK}$	73	AD0	98	DRQ0
24	P3.0/RXI1	49	$\overline{WR}$	74	A19/S6/$\overline{ONCE}$	99	DRQ1
25	P3.1/TXI1	50	$\overline{RD}$	75	A18/S5	100	DRQ2

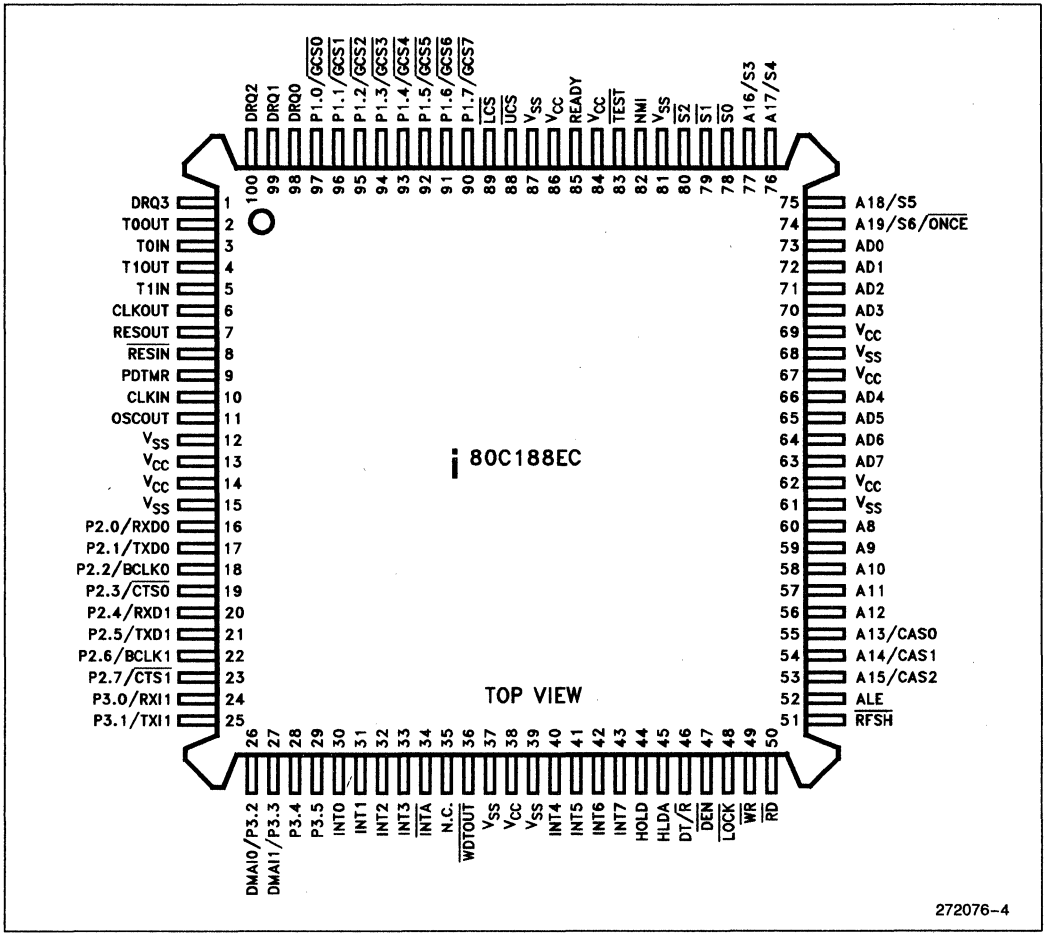

Figure 4. 100-Pin Plastic Quad Flat Pack Package (PQFP)

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Table 5. QFP Pin Names with Package Location

AD Bus	
Name	**Pin**
AD0	76
AD1	75
AD2	74
AD3	73
AD4	69
AD5	68
AD6	67
AD7	66
A8	63
A9	62
A10	61
A11	60
A12	59
A13/CAS0	58
A14/CAS1	57
A15/CAS2	56
A16/S3	80
A17/S4	79
A18/S5	78
A19/S6/$\overline{\text{ONCE}}$	77

No Connect
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Bus Control	
Name	**Pin**
ALE	55
$\overline{\text{RFSH}}$	54
$\overline{\text{S0}}$	81
$\overline{\text{S1}}$	82
$\overline{\text{S2}}$	83
$\overline{\text{RD}}$	53
$\overline{\text{WR}}$	52
READY	88
$\overline{\text{DEN}}$	50
DT/$\overline{\text{R}}$	49
$\overline{\text{LOCK}}$	51
HOLD	47
HLDA	48
$\overline{\text{INTA}}$	37

Power and Ground	
Name	**Pin**
V_{CC}	16
V_{CC}	17
V_{CC}	41
V_{CC}	65
V_{CC}	70
V_{CC}	72
V_{CC}	87
V_{CC}	89
V_{SS}	15
V_{SS}	18
V_{SS}	40
V_{SS}	42
V_{SS}	64
V_{SS}	71
V_{SS}	84
V_{SS}	90

Processor Control	
Name	**Pin**
$\overline{\text{RESIN}}$	11
RESOUT	10
CLKIN	13
OSCOUT	14
CLKOUT	9
$\overline{\text{TEST}}$	86
PDTMR	12
NMI	85
INT0	33
INT1	34
INT2	35
INT3	36
INT4	43
INT5	44
INT6	45
INT7	46

I/O	
Name	**Pin**
$\overline{\text{UCS}}$	91
$\overline{\text{LCS}}$	92
P1.7/$\overline{\text{GCS7}}$	93
P1.6/$\overline{\text{GCS6}}$	94
P1.5/$\overline{\text{GCS5}}$	95
P1.4/$\overline{\text{GCS4}}$	96
P1.3/$\overline{\text{GCS3}}$	97
P1.2/$\overline{\text{GCS2}}$	98
P1.1/$\overline{\text{GCS1}}$	99
P1.0/$\overline{\text{GCS0}}$	100
P2.7/$\overline{\text{CTS1}}$	26
P2.6/BCLK1	25
P2.5/TXD1	24
P2.4/RXD1	23
P2.3/$\overline{\text{CTS0}}$	22
P2.2/BCLK0	21
P2.1/TXD0	20
P2.0/RXD0	19
P3.5	32
P3.4	31
P3.3/DMAI1	30
P3.2/DMAI0	29
P3.1/TXI1	28
P3.0/RXI1	27
T0IN	6
T0OUT	5
T1IN	8
T1OUT	7
DRQ0	1
DRQ1	2
DRQ2	3
DRQ3	4
$\overline{\text{WDTOUT}}$	39

Table 6. QFP Package Location with Pin Names

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	DRQ0	26	P2.7/$\overline{CTS1}$	51	$\overline{LOCK}$	76	AD0
2	DRQ1	27	P3.0/RXI1	52	$\overline{WR}$	77	A19/S6/$\overline{ONCE}$
3	DRQ2	28	P3.1/TXI1	53	$\overline{RD}$	78	A18/S5
4	DRQ3	29	DMAI0/P3.2	54	$\overline{RFSH}$	79	A17/S4
5	T0OUT	30	DMAI1/P3.3	55	ALE	80	A16/S3
6	T0IN	31	P3.4	56	A15	81	$\overline{S0}$
7	T1OUT	32	P3.5	57	A14	82	$\overline{S1}$
8	T1IN	33	INT0	58	A13	83	$\overline{S2}$
9	CLKOUT	34	INT1	59	A12	84	V_{SS}
10	RESOUT	35	INT2	60	A11	85	NMI
11	$\overline{RESIN}$	36	INT3	61	A10	86	$\overline{TEST}$
12	PDTMR	37	$\overline{INTA}$	62	A9	87	V_{CC}
13	CLKIN	38	N.C.	63	A8	88	READY
14	OSCOUT	39	$\overline{WDTOUT}$	64	V_{SS}	89	V_{CC}
15	V_{SS}	40	V_{SS}	65	V_{CC}	90	V_{SS}
16	V_{CC}	41	V_{CC}	66	AD7	91	$\overline{UCS}$
17	V_{CC}	42	V_{SS}	67	AD6	92	$\overline{LCS}$
18	V_{SS}	43	INT4	68	AD5	93	P1.7/$\overline{GCS7}$
19	P2.0/RXD0	44	INT5	69	AD4	94	P1.6/$\overline{GCS6}$
20	P2.1/TXD0	45	INT6	70	V_{CC}	95	P1.5/$\overline{GCS5}$
21	P2.2/BCLK0	46	INT7	71	V_{SS}	96	P1.4/$\overline{GCS4}$
22	P2.3/$\overline{CTS0}$	47	HOLD	72	V_{CC}	97	P1.3/$\overline{GCS3}$
23	P2.4/RXD1	48	HLDA	73	AD3	98	P1.2/$\overline{GCS2}$
24	P2.5/TXD1	49	DT/$\overline{R}$	74	AD2	99	P1.1/$\overline{GCS1}$
25	P2.6/BCLK1	50	$\overline{DEN}$	75	AD1	100	P1.0/$\overline{GCS0}$

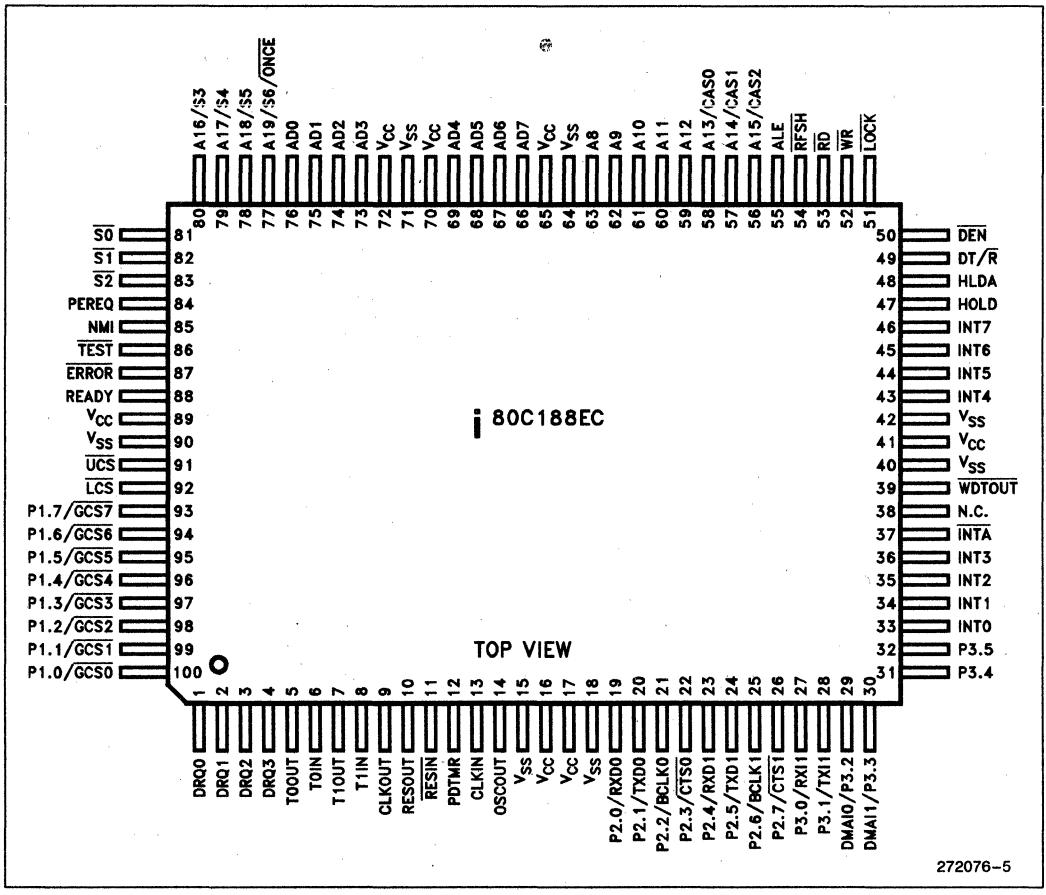

Figure 5. Quad Flat Pack (EIAJ) Pinout Diagram

PACKAGE THERMAL SPECIFICATIONS

The 80C188EC is specified for operation when T_C (the case temperature) is within the range of −40°C to +100°C. T_C may be measured in any environment to determine whether the 80C188EC is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P * \theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 7 for the 100-pin Quad Flat Pack (QFP) package.

Table 8 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies. P (the maximum power consumption—specified in Watts) is calculated by using the maximum I_{CC} and V_{CC} of 5.5V.

Table 7. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow in ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PQFP)	27.0	22.0	18.0	15.0	14.0	13.5
θ_{CA} (QFP)	64.5	55.5	51.0	TBD	TBD	TBD

Table 8. Maximum T_A at Various Airflows (in °C)

		Airflow in ft/min (m/sec)					
	T_F (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PQFP)	TBD	TBD	TBD	TBD	TBD	TBD	TBD
θ_{CA} (QFP)	TBD	TBD	TBD	TBD	TBD	TBD	TBD

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ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Storage Temperature ..... −65°C to +150°C

Case Temperature Under Bias... −65°C to +100°C

Supply Voltage
with Respect to V_{SS} ..... −0.5V to +6.5V

Voltage on Other Pins
with Respect to V_{SS} ..... −0.5V to V_{CC} + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.5	5.5	V
T_F	Input Clock Frequency			
	80C188EC-16	0	32	MHz
	80C188EC-13	0	26.08	MHz
T_C	Case Temperature Under Bias			
	KU80C188EC-XX (PQFP)	−40°C	+100	°C
	S80C188EC-XX (QFP)	−40°C	+100	°C

Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80C188EC-based circuit board should include separate power (V_{CC}) and ground (V_{SS}) planes. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Liberal decoupling capacitance should be placed near the 80C188EC. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by placing the decoupling capacitors as close as possible to the 80C188EC V_{CC} and V_{SS} package pins.

Always connect any unused input to an appropriate signal level. In particular, unused interrupt inputs (NMI, INT0:7) should be connected to V_{SS} through a pull-down resistor. Leave any unused output pin unconnected.

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	−0.5	0.3*V_{CC}	V	
V_{IH}	Input High Voltage	0.7*V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 3 mA (Min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −2 mA (Min)
V_{HYR}	Input Hysteresis on $\overline{RESIN}$	0.5		V	
I_{LI}	Input Leakage Current for Pins: AD15:0, READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$, NMI, INT7:0, T0IN, T1IN, P2.7–P2.0, P3.5–P3.0, DRQ3:0		±15	μA	0 ≤ V_{IN} ≤ V_{CC}
I_{LIU}	Input Leakage for Pins with Pullups Active During Reset: A19:16, $\overline{LOCK}$	−0.2	−5	mA	V_{IN} = 0.7 V_{CC} (Note 1)
I_{LO}	Output Leakage for Floated Output Pins		±15	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 2)
I_{CC}	Supply Current Cold (in RESET) 80C188EC-16 80C188EC-13		 85 70	 mA mA	(Note 3)
I_{ID}	Supply Current in Idle Mode 80C188EC-16 80C188EC-13		 60 50	 mA mA	(Note 4)
I_{PD}	Supply Current in Powerdown Mode 80C188EC-16 80C188EC-13		 100 100	 μA μA	(Note 5)
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 6)

NOTES:
1. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
2. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
3. Measured with the device in RESET and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
4. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
5. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or GND.
6. Output Capacitance is the capacitive load of a floating output pin.

I_{CC} versus Frequency and Voltage

The I_{CC} consumed by the 80C188EC is composed of two components:

1. I_{PD}—The quiescent current that represents internal device leakage. Measured with all inputs at either V_{CC} or ground and no clock applied.
2. I_{CCS}—The switching current used to charge and discharge internal parasitic capacitance when changing logic levels. I_{CCS} is related to both the frequency of operation and the device supply voltage (V_{CC}). I_{CCS} is given by the formula:

$$\text{Power} = V * I = V^2 * C_{DEV} * f$$
$$\therefore I_{CCS} = V * C_{DEV} * f$$

Where:

V = Supply Voltage (V_{CC})

C_{DEV} = Device Capacitance

f = Operating Frequency

Measuring C_{PD} on a device like the 80C188EC would be difficult. Instead, C_{PD} is calculated using the above formula with I_{CC} values measured at known V_{CC} and frequency. Using the C_{PD} value, the user can calculate I_{CC} at any voltage and frequency within the specified operating range.

Example. Calculate typical I_{CC} at 14 MHz, 5.2V V_{CC}.

$I_{CC} = I_{PD} + I_{CCS}$
$= 0.1\text{ mA} + 5.2V * 0.77 * 14\text{ MHz}$
$= 56.2\text{ mA}$

PDTMR Pin Delay Calculation

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown Mode. A delay is required only when using the on chip oscillator to allow the crystal or resonator circuit to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e. a device reset while in Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized.

To calculate the value of capacitor to use to provide a desired delay, use the equation:

$$440 \times t = C_{PD}\ (5V, 25°C)$$

Where:

t = desired delay in **seconds**
C_{PD} = capacitive load on PDTMR in **microfarads**

Example. For a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6} = 0.132\ \mu F$ is required. Round up to a standard (available) capacitor value.

NOTE:
The above equation applies to delay time longer than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% to −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperatures will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

Parameter	Target Typical	Target Max	Units	Notes
CPD	0.77	1.37	mA/V*MHz	1, 2
CPD (Idle Mode)	0.55	0.96	mA/V*MHz	1, 2

NOTES:
1. Maximum C_{PD} is measured at −40°C with all outputs loaded as specified in the AC test conditions and the device in reset (or Idle Mode). Due to tester limitations, CLKOUT and OSCOUT also have 50 pF loads that increase I_{CC} by V*C*F.
2. Typical C_{PD} is calculated at 25°C assuming no loads on CLKOUT or OSCOUT and the device in reset (or Idle Mode).

AC SPECIFICATIONS

AC Characteristics—80C188EC-16

Symbol	Parameter	TARGET Min	TARGET Max	Unit	Notes
INPUT CLOCK					
TF	CLKIN Frequency	0	32	MHz	1
TC	CLKIN Period	31.25	∞	ns	1
TCH	CLKIN High Time	10	∞	ns	1, 2
TCL	CLKIN Low Time	10	∞	ns	1, 2
TCR	CLKIN Rise Time	1	10	ns	1, 3
TCF	CLKIN Fall Time	1	10	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	20	ns	1, 4
T	CLKOUT Period		2 * TC	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{RFSH}$, $\overline{LOCK}$, A19:16	3	22	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$, $\overline{NCS}$, $\overline{WDTOUT}$	3	27	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	22	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GSC7:0}$, $\overline{LCS}$, $\overline{UCS}$, A15:8, AD7:0, $\overline{INTA}$, $\overline{S2:0}$	3	27	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	25	ns	1
T_{CLOF}	$\overline{DEN}$, A15:8, AD7:0	0	25	ns	1
INPUT REQUIREMENTS					
T_{CHIS}	$\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, BCLK1:0, P3.4, P3.5	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, DRQ1:0, BCLK1:0, P3.4, P3.5	3		ns	1, 9
T_{CLIS}	AD7:0, READY	10		ns	1, 10
T_{CLIH}	AD7:0, READY	3		ns	1, 10
T_{CLIS}	HOLD, DRQ3:0	10		ns	1, 9
T_{CLIH}	HOLD, DRQ3:0	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 16 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 17 for rise and fall times outside 50 pF.
6. See Figure 17 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C188EC operation.

AC Characteristics—80C188EC-13

Symbol	Parameter	TARGET Min	TARGET Max	Unit	Notes
INPUT CLOCK					
TF	CLKIN Frequency	0	26.08	MHz	1
TC	CLKIN Period	38.34	∞	ns	1
TCH	CLKIN High Time	12	∞	ns	1, 2
TCL	CLKIN Low Time	12	∞	ns	1, 2
TCR	CLKIN Rise Time	1	10	ns	1, 3
TCF	CLKIN Fall Time	1	10	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	23	ns	1, 4
T	CLKOUT Period		2 * TC	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	6	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	6	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{RFSH}$, $\overline{LOCK}$, A19:16	3	25	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$, $\overline{WDTOUT}$	3	30	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	25	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{NCS}$, $\overline{INTA}$, $\overline{S2:0}$, A15:8, AD7:0	3	30	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, A15:8, AD7:0	0	30	ns	1
INPUT REQUIREMENTS					
T_{CHIS}	$\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, BCLK1:0, P3.4, P3.5	10		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, T1IN, T0IN, READY, $\overline{CTS1:0}$, DRQ3:0, BCLK1:0, P3.4, P3.5	3		ns	1, 9
T_{CLIS}	AD7:0, READY	10		ns	1, 10
T_{CLIH}	AD7:0, READY	3		ns	1, 10
T_{CLIS}	HOLD, DRQ3:0	10		ns	1, 9
T_{CLIH}	HOLD, DRQ3:0	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 16 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 17 for rise and fall times outside 50 pF.
6. See Figure 17 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A19:16 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80C188EC operation.

Relative Timings—80C188EC-16, 13

Symbol	Parameter	TARGET Min	TARGET Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Active Pulse Width	T − 15		ns	
T_{AVLL}	AD Valid Setup before ALE Falls	½T − 10		ns	
T_{PLLL}	Chip Select Valid before ALE Falls	½T − 10		ns	1
T_{LLAX}	AD Hold after ALE Falls	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{WHLH}	$\overline{WR}$ Rising to Next ALE Rising	½T − 10		ns	1
T_{AFRL}	AD Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Active Pulse Width	2T − 5		ns	2
T_{WLWH}	$\overline{WR}$ Active Pulse Width	2T − 5		ns	2
T_{RHAX}	$\overline{RD}$ Rising to Next Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHPH}	$\overline{WR}$ Rise to Chip Select Rise	½T − 10		ns	1
T_{RHPH}	$\overline{RD}$ Rise to Chip Select Rise	½T − 10		ns	1
T_{PHPL}	Chip Select Inactive to Next Chip Select Active	½T − 10		ns	1
T_{OVRH}	$\overline{ONCE}$ Active Setup to $\overline{RESIN}$ Rising	T		ns	
T_{RHOX}	$\overline{ONCE}$ Hold after $\overline{RESIN}$ Rise	T		ns	
T_{IHIL}	$\overline{INTA}$ High to Next $\overline{INTA}$ Low during INTA Cycle	4T − 5		ns	4
T_{ILIH}	$\overline{INTA}$ Active Pulse Width	2T − 5		ns	2, 4
T_{CVIL}	CAS2:0 Setup before 2nd $\overline{INTA}$ Pulse Low	8T		ns	2, 4
T_{ILCX}	CAS2:0 Hold after 2nd $\overline{INTA}$ Pulse Low	4T		ns	2, 4
T_{IRES}	Interrupt Resolution Time		150	ns	3
T_{IRLH}	IR Low Time to Reset Edge Detector	50		ns	
T_{IRHIF}	IR Hold Time after 1st $\overline{INTA}$ Falling	25		ns	4, 5

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Interrupt resolution time is the delay between an unmasked interrupt request going active and the interrupt output of the 82C59A module going active. This is not directly measureable by the user. For interrupt pin INT7 the delay from an active signal to an active input to the CPU would actually be twice the T_{IRES} value since the signal must pass through two 82C59A modules.
4. See INTA Cycle Waveforms for definition.
5. To guarantee interrupt is not spurious.

Serial Port Mode 0 Timings—80C188EC-16, 13

Symbol	Parameter	TARGET Min	TARGET Max	Unit	Notes
RELATIVE TIMINGS					
T_{XLXL}	TXD Clock Period	T (n + 1)		ns	1, 2
T_{XLXH}	TXD Clock Low to Clock High (N > 1)	2T − 35	2T + 35	ns	1
T_{XLXH}	TXD Clock Low to Clock High (N = 1)	T − 35	T + 35	ns	1
T_{XHXL}	TXD Clock High to Clock Low (N > 1)	(n − 1) T − 35	(n − 1) T + 35	ns	1, 2
T_{XHXL}	TXD Clock High to Clock Low (N = 1)	T − 35	T + 35	ns	1
T_{QVXH}	RXD Output Data Setup to TXD Clock High (N > 1)	(n − 1)T − 35		ns	1, 2
T_{QVXH}	RXD Output Data Setup to TXD Clock High (N = 1)	T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (N > 1)	2T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (N = 1)	T − 35		ns	1
T_{XHQZ}	RXD Output Data Float after Last TXD Clock High		T + 20	ns	1
T_{DVXH}	RXD Input Data Setup to TXD Clock High	T + 20		ns	1
T_{XHDX}	RXD Input Data Setup after TXD Clock High	0		ns	1

NOTES:
1. See Figure 15 for Waveforms.
2. n is the value in the BxCMP register ignoring the ICLK bit.

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 9. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms for AC specification definitions, test pins and illustrations.

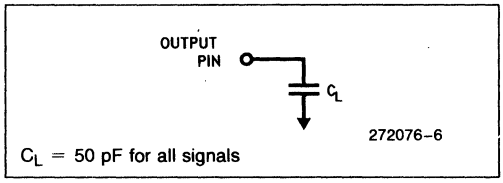

Figure 6. AC Test Load

AC TIMING WAVEFORMS

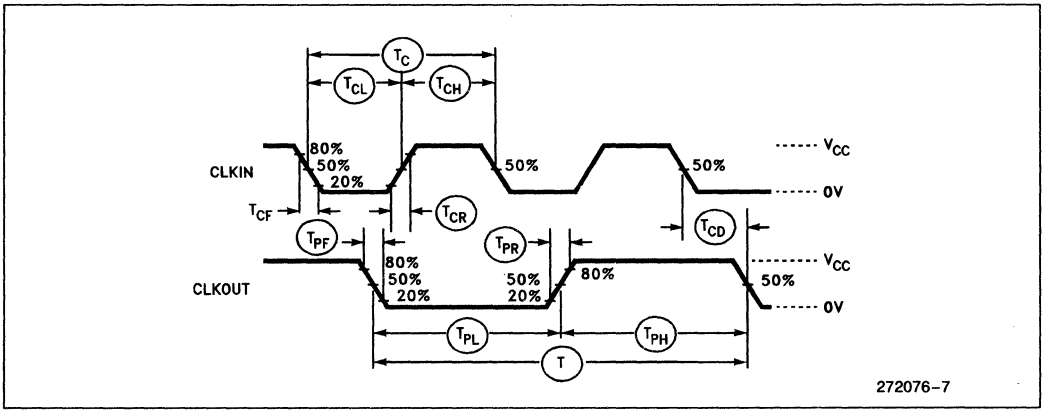

Figure 7. Input and Output Clock Waveforms

24

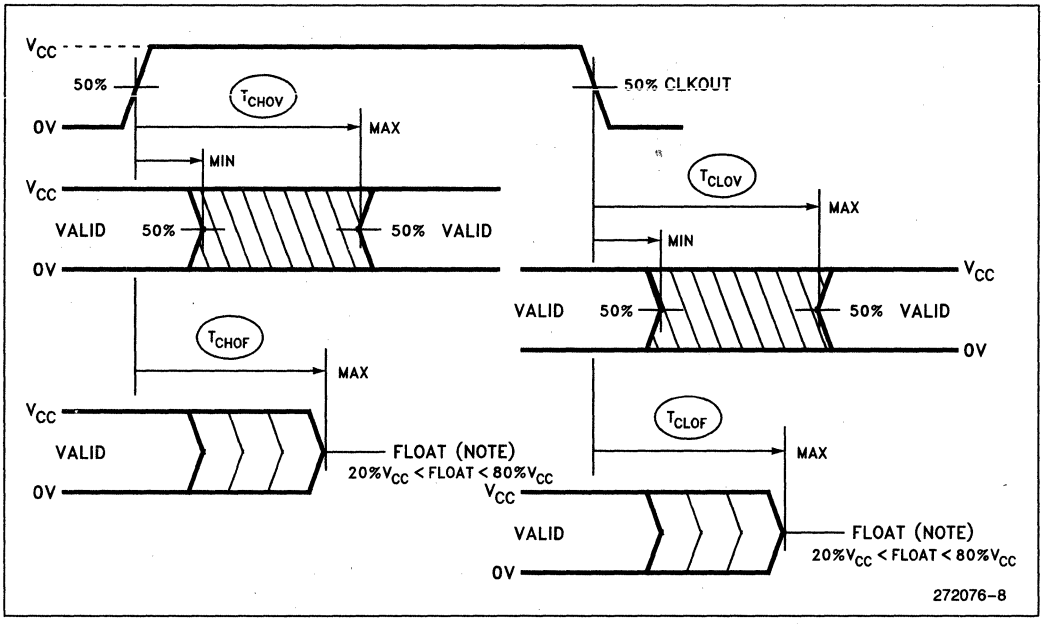

Figure 8. Output Delay and Float Waveforms

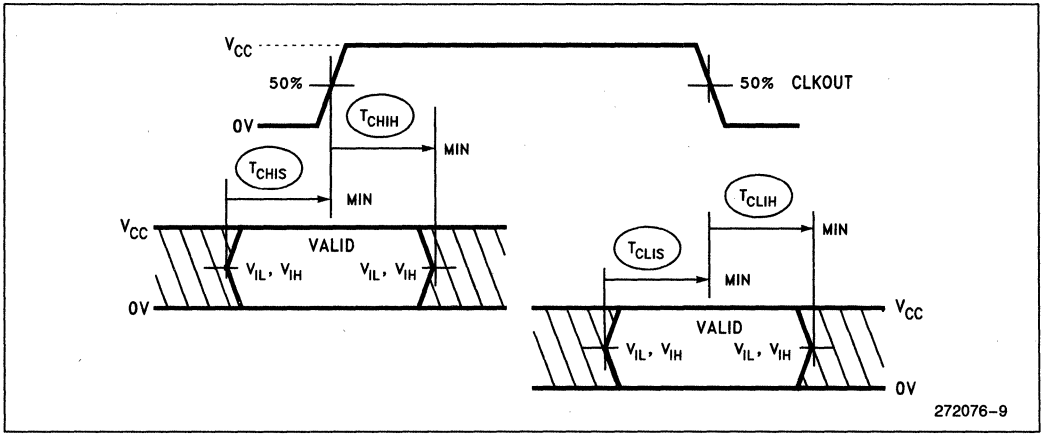

Figure 9. Input Setup and Hold

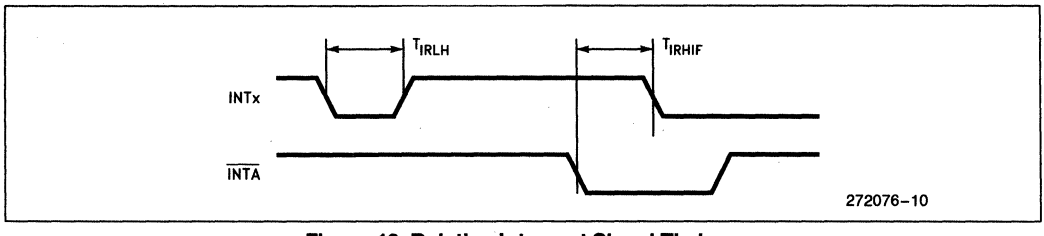

Figure 10. Relative Interrupt Signal Timings

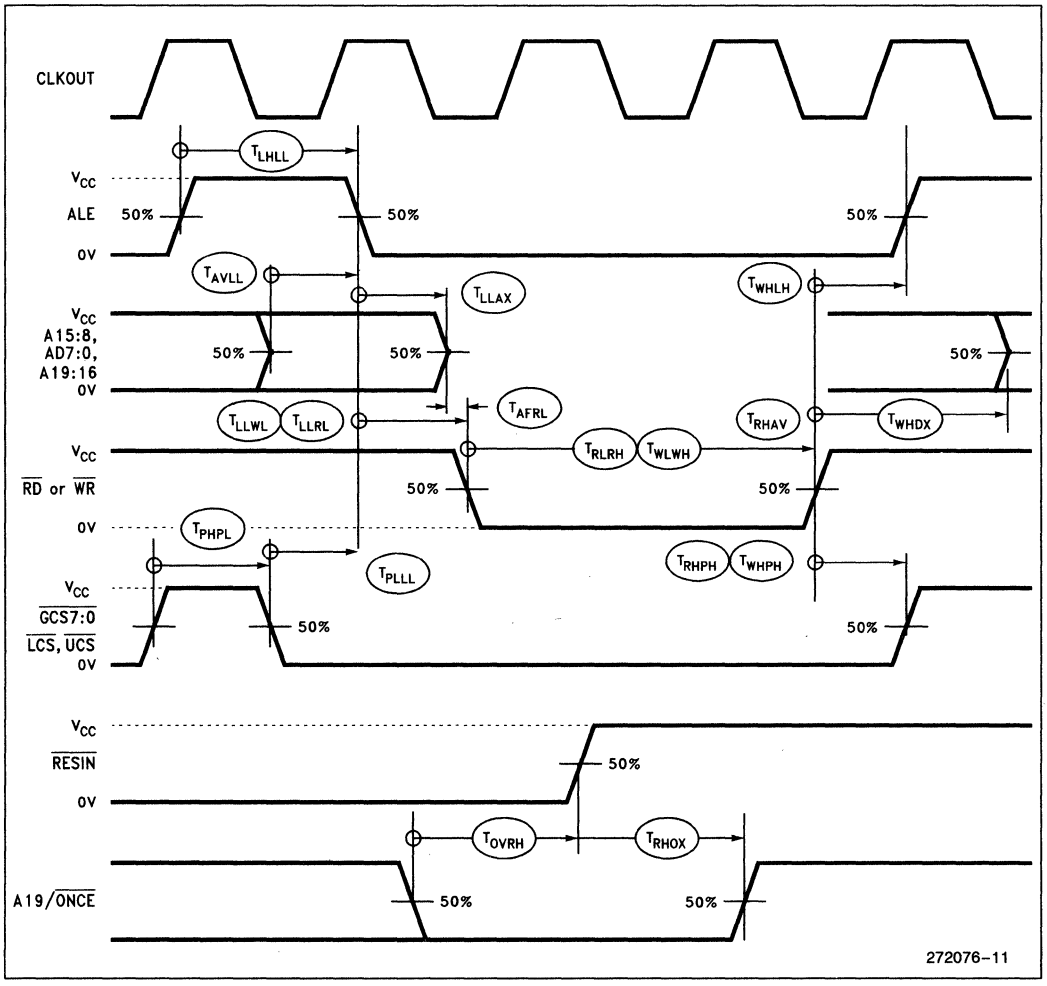

Figure 11. Relative Signal Waveform

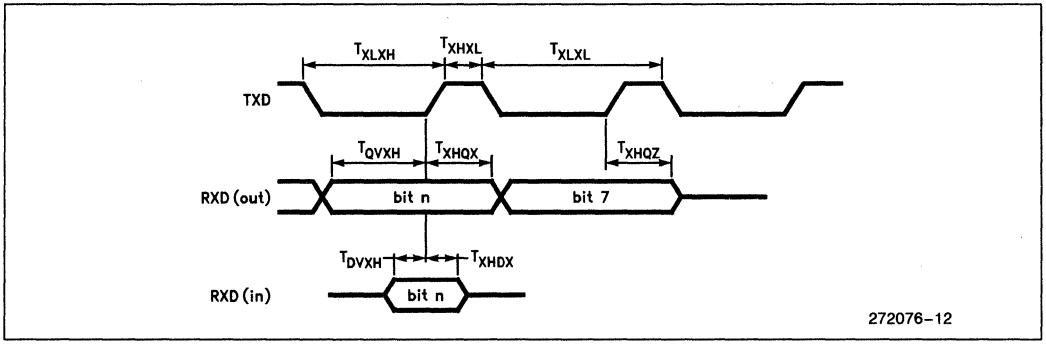

Figure 12. Serial Port Mode 0 Waveform

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DERATING CURVES

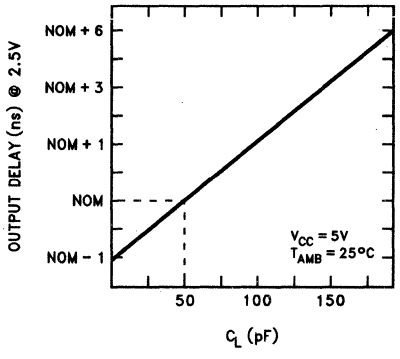


Figure 13. Typical Output Delay Variations vs Load Capacitance

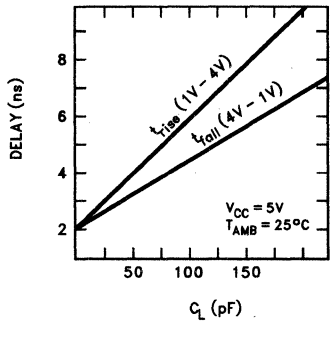


Figure 14. Typical Rise and Fall Variations vs Load Capacitance

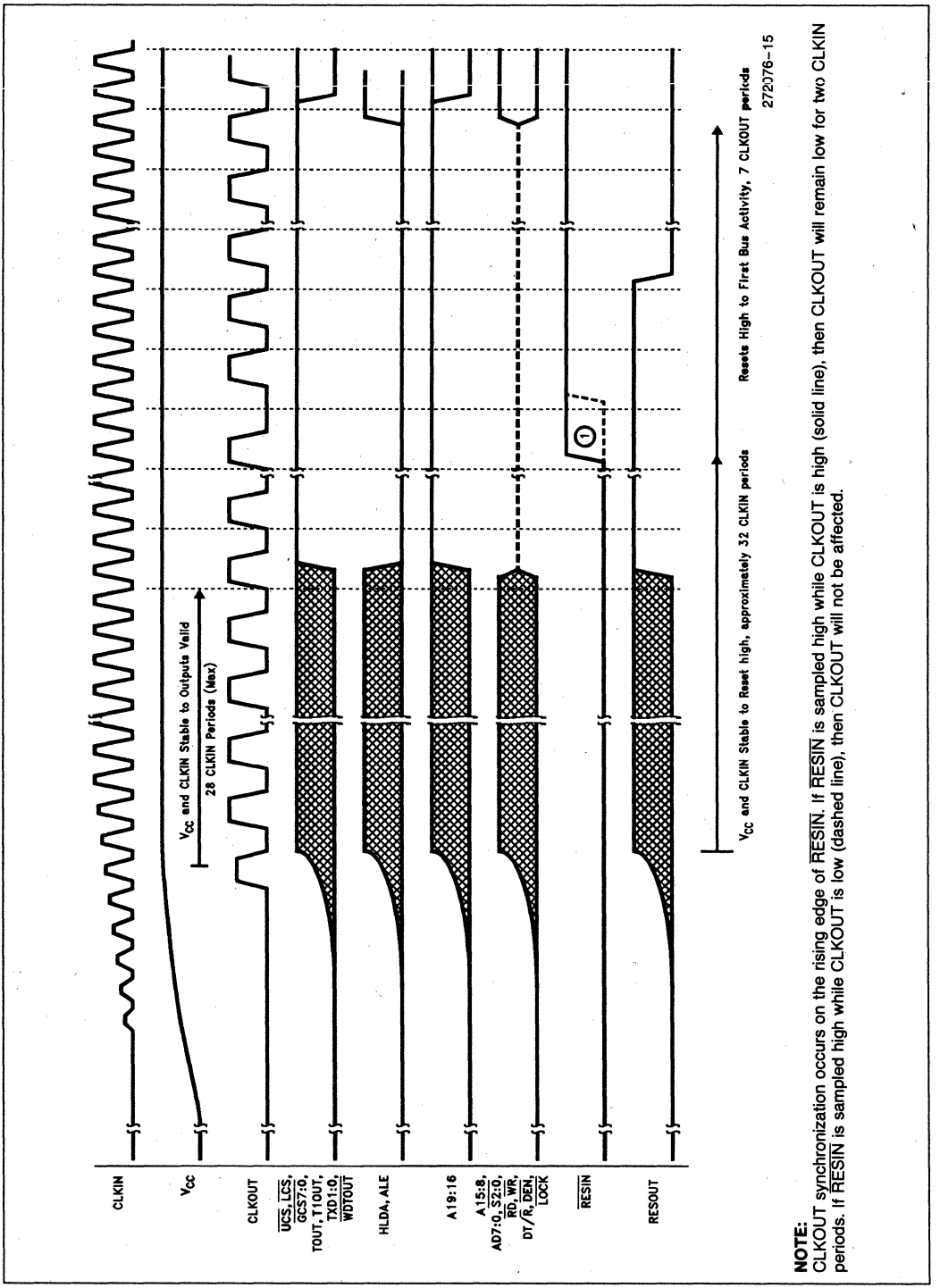
RESET

The 80C188EC will perform a reset operation any time the $\overline{RESIN}$ pin is active. The $\overline{RESIN}$ pin is synchronized before it is presented internally, which means that the clock must be operating before a reset can take effect. From a power-on state, $\overline{RESIN}$ must be held active (low) in order to guarantee correct initialization of the 80C188EC. **Failure to provide $\overline{RESIN}$ while the device is powering up will result in unspecified operation of the device.**

Figure 15 shows the correct reset sequence when first applying power to the 80C188EC. An external clock connected to CLKIN must not exceed the V_{CC} threshold being applied to the 80C188EC. This is normally not a problem if the clock driver is supplied with the same V_{CC} that supplies the 80C188EC. When attaching a crystal to the device, $\overline{RESIN}$ must remain active until both V_{CC} and CLKOUT are stable (the length of time is application specific and depends on the startup characteristics of the crystal circuit). The $\overline{RESIN}$ pin is designed to operate correctly using a RC reset circuit, but the designer must ensure that the ramp time for V_{CC} is not so long that $\overline{RESIN}$ is never sampled at a logic low level when V_{CC} reaches minimum operating conditions.

Figure 16 shows the timing sequence when $\overline{RESIN}$ is applied after V_{CC} is stable and the device has been operating. Note that a reset will terminate all activity and return the 80C188EC to a known operating state. Any bus operation that is in progress at the time $\overline{RESIN}$ is asserted will terminate immediately (note that most control signals will be driven to their inactive state first before floating).

While $\overline{RESIN}$ is active, bus signals $\overline{LOCK}$, A19/S16/$\overline{ONCE}$ and A18:16 are configured as inputs and weakly held high by internal pullup transistors. Only A19/$\overline{ONCE}$ can be overdriven to a low and is used to enable the ONCE™ Mode. Forcing $\overline{LOCK}$ or A18:16 low at any time while $\overline{RESIN}$ is low is prohibited and will cause unspecified device operation.



NOTE:
CLKOUT synchronization occurs on the rising edge of RESIN. If RESIN is sampled high while CLKOUT is high (solid line), then CLKOUT will remain low for two CLKIN periods. If RESIN is sampled high while CLKOUT is low (dashed line), then CLKOUT will not be affected.

Figure 15. Cold Reset Waveforms

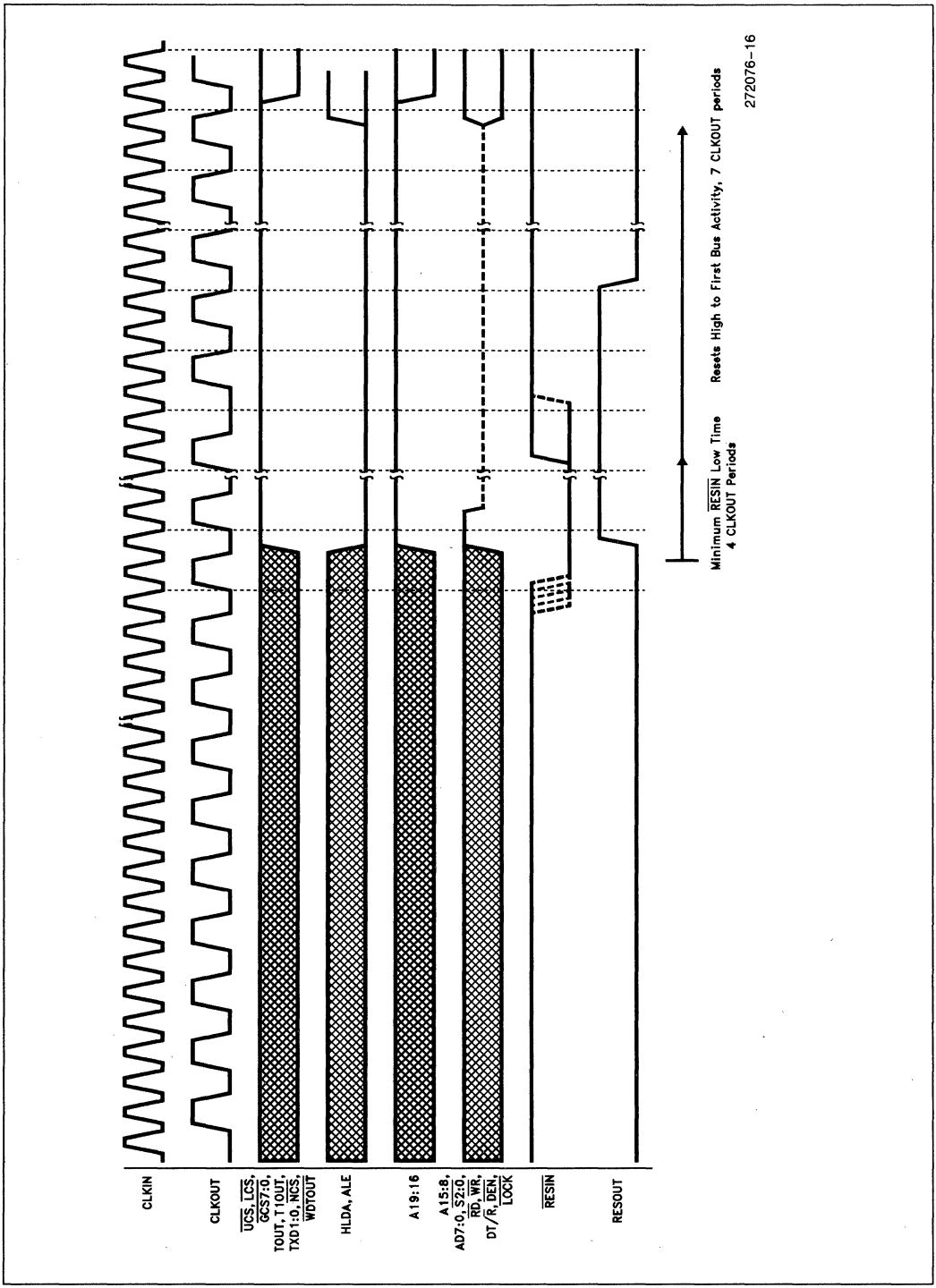


Figure 16. Warm Reset Waveforms

BUS CYCLE WAVEFORMS

Figures 17 through 29 present the various bus cycles that are generated by the 80C188EC. What is shown in the figure is the relationship of the various bus signals to CLKOUT. These figures along with the information present in Section 4.5, AC Specifications, allow the user to determine all the critical timing analysis needed for a given application.

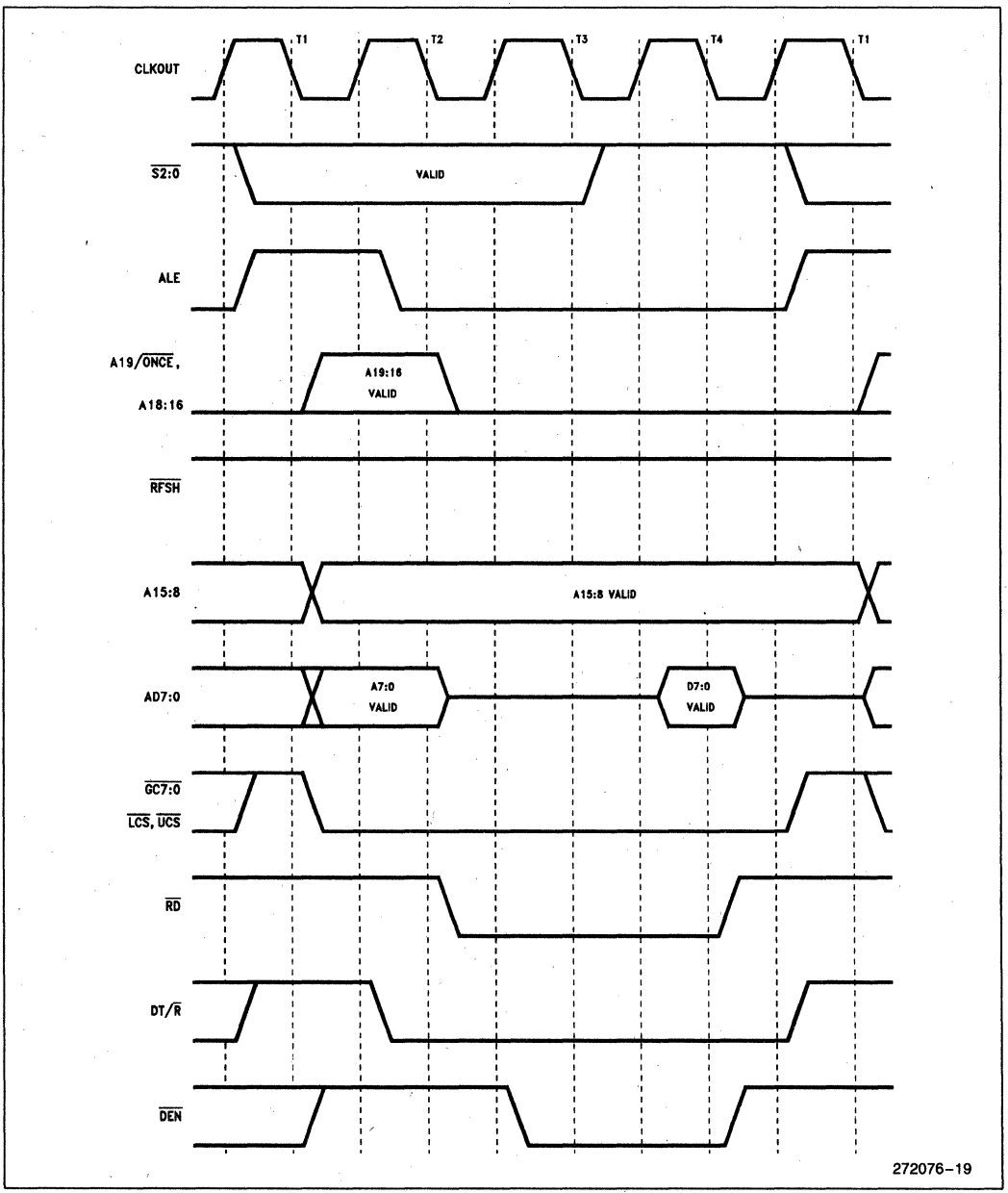


Figure 17. Memory Read, I/O Read, Instruction Fetch and Refresh Waveform

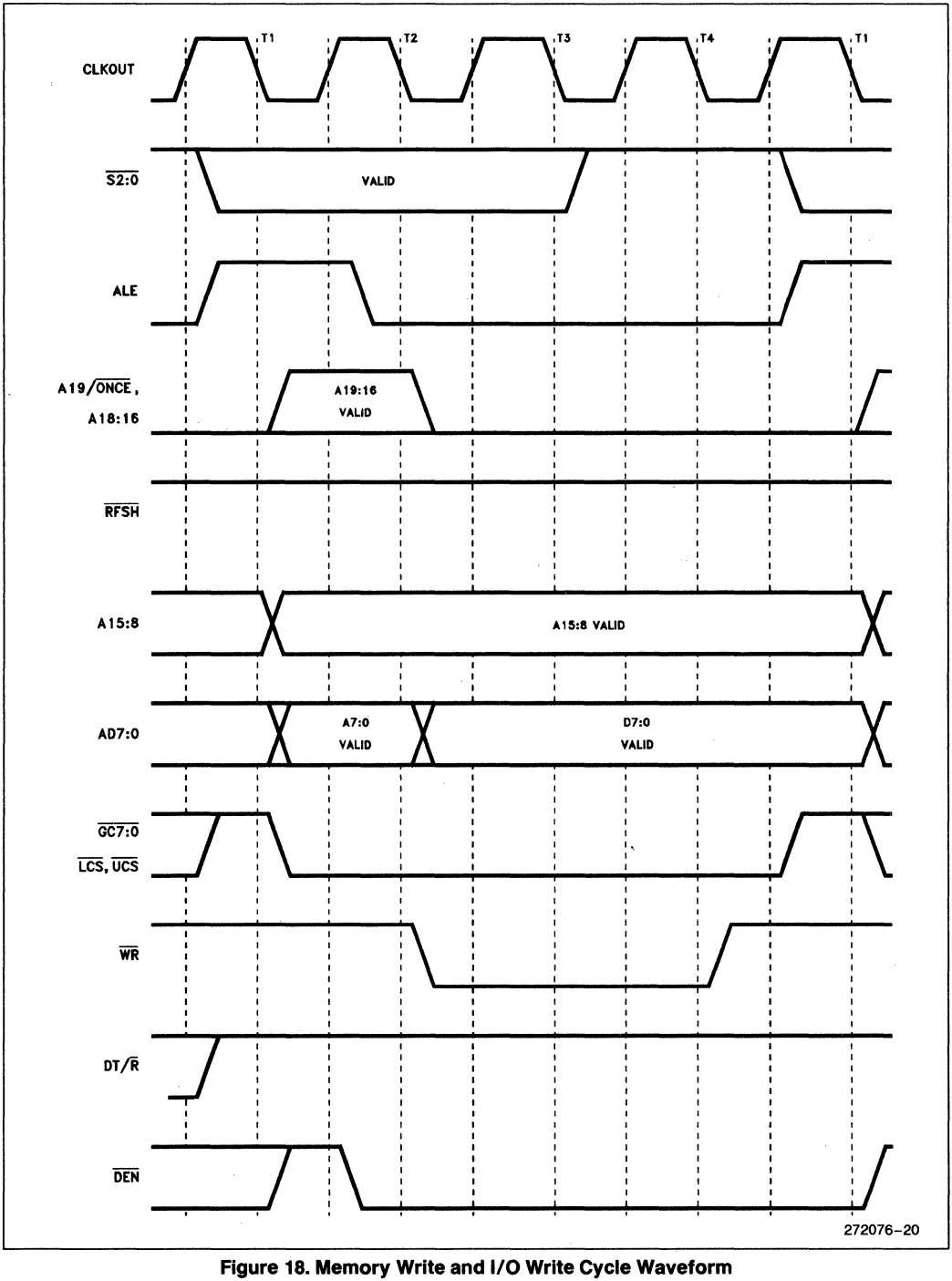
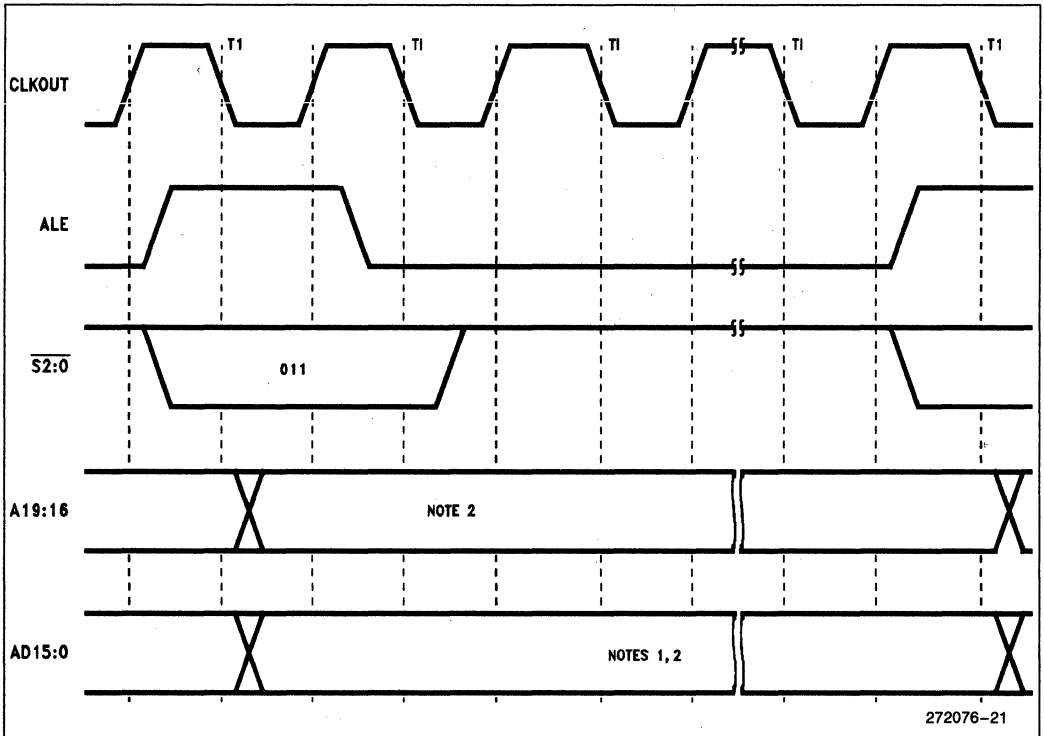


Figure 18. Memory Write and I/O Write Cycle Waveform



NOTES:
1. Address information is invalid. If previous bus cycle was a read, then the AD15:0 lines will float during T1. Otherwise, the AD15:0 lines will continue to drive during T1 (data is invalid). All other control lines are in their inactive state.
2. All address lines drive zeros while in Powerdown or Idle Mode.

Figure 19. Halt Cycle Waveform

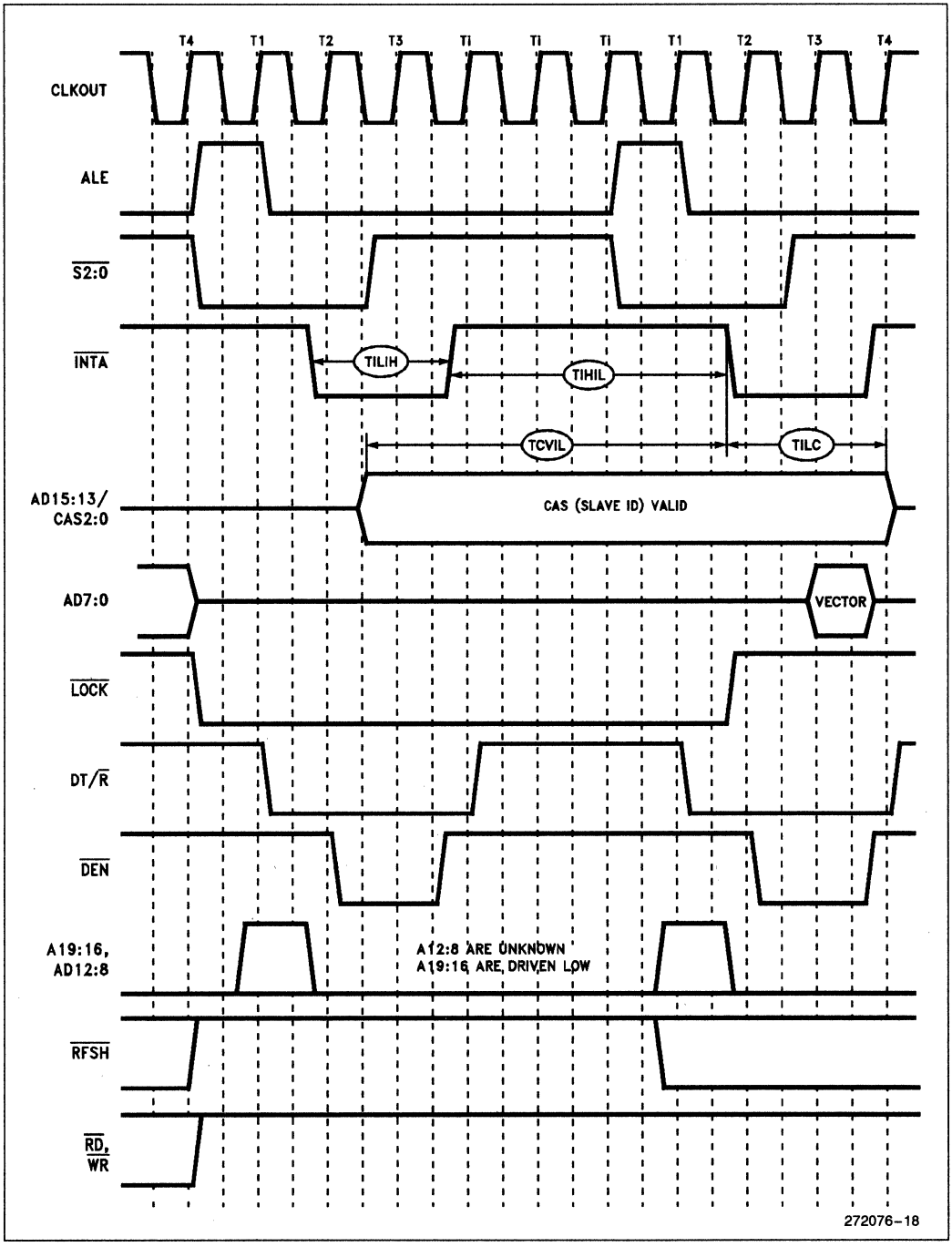


Figure 20. Interrupt Acknowledge Cycle Waveform

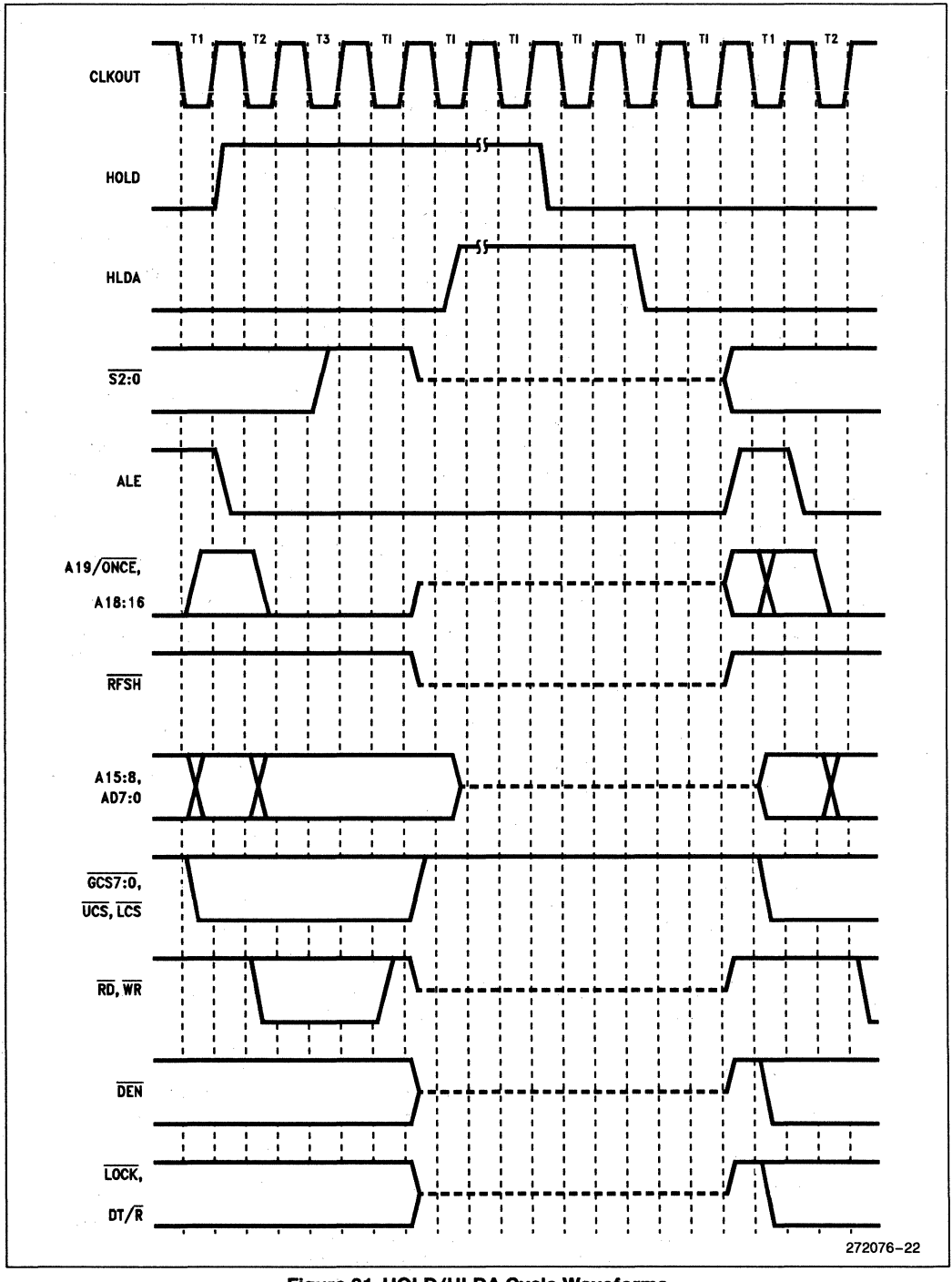


Figure 21. HOLD/HLDA Cycle Waveforms

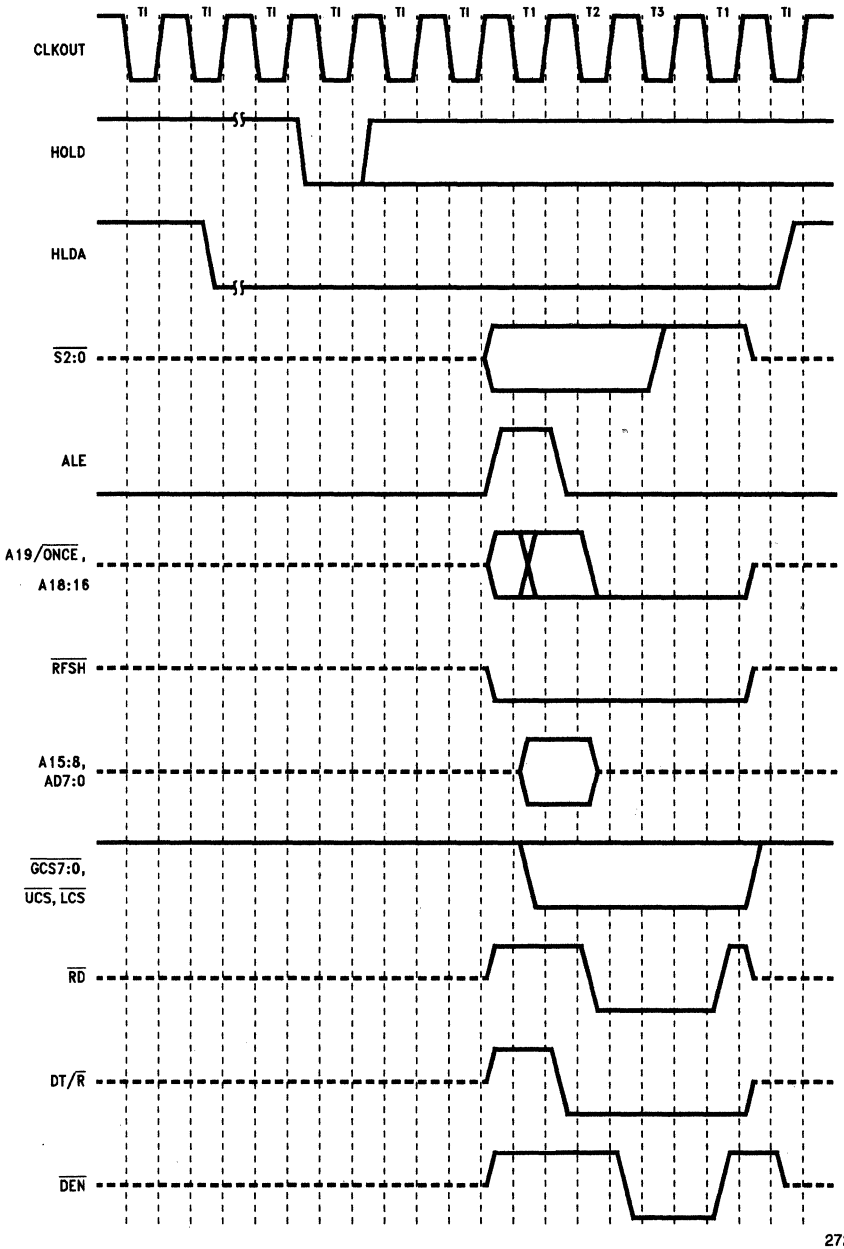
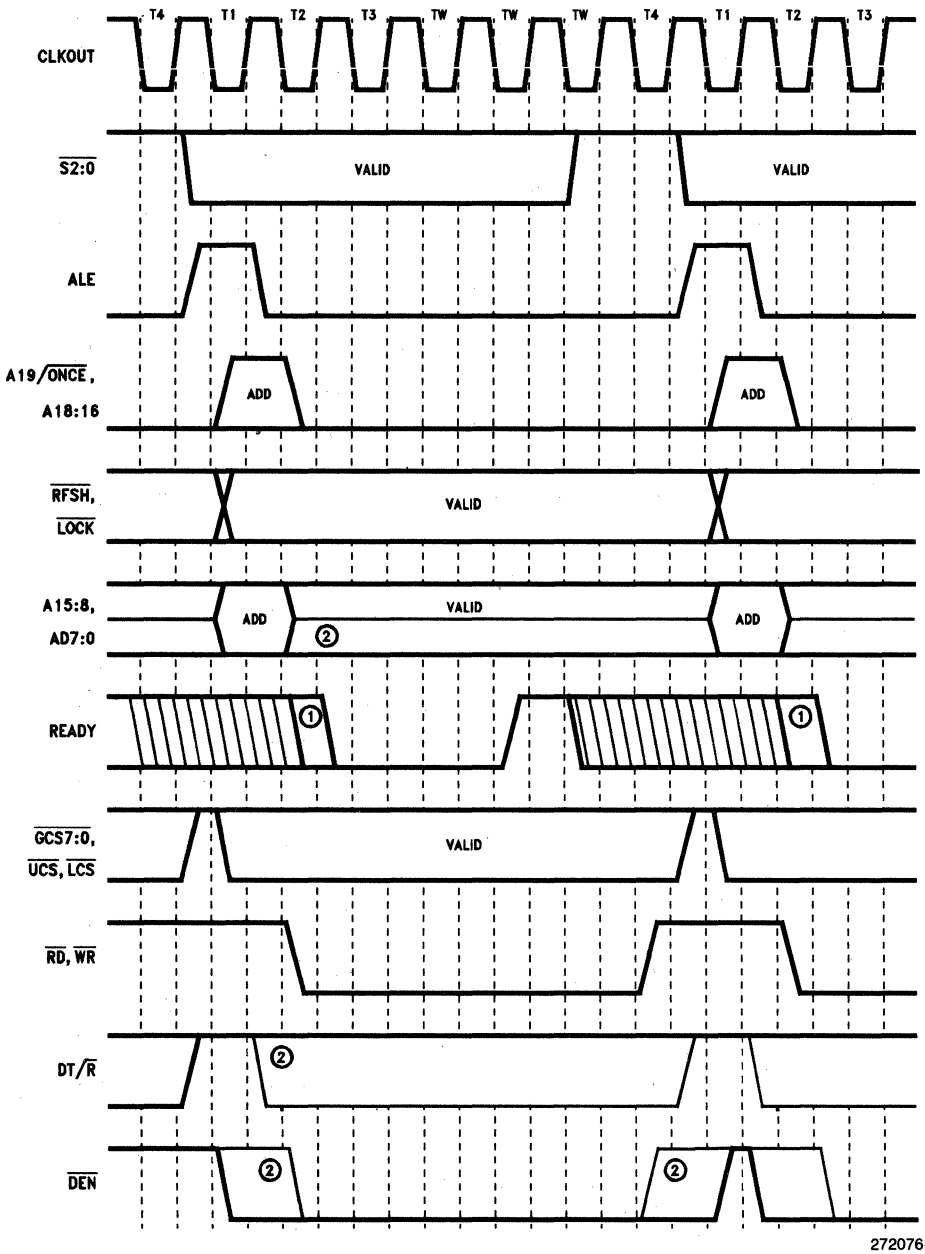


Figure 22. Refresh during HLDA Waveforms



NOTES:
1. READY must be low by either edge to cause a wait state.
2. Lighter lines indicate READ cycles, darker lines indicate WRITE cycles.

Figure 23. Ready Cycle Waveforms

REGISTER BIT SUMMARY

Figures 24 through 37 present the bit definition of each register that is active (not reserved) in the Peripheral Control Block (PCB). Each register can be thought to occupy one word (16-bits) of either memory or I/O space, although not all bits in the register necessarily have a function. A register bit is not guaranteed to return a specific logic value if an "X" appears for the bit definition (i.e., if a zero was written to the register bit it may not be returned as a zero when read). Furthermore, a 0 must be written to any bit that is indicated by an "X" to ensure compatibility with future products or potential product changes. Any register bit that has a specific value in it (a "0" or a "1"), must be written to that value in order to guarantee proper operation of the 80C188EC.

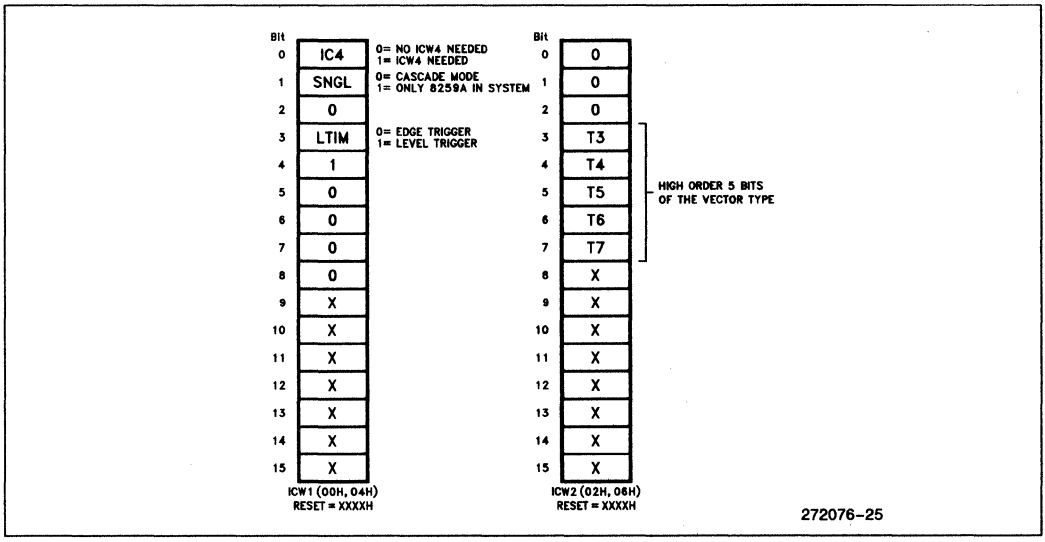


Figure 24. 8259A Module Initialization Command Words (ICWs)

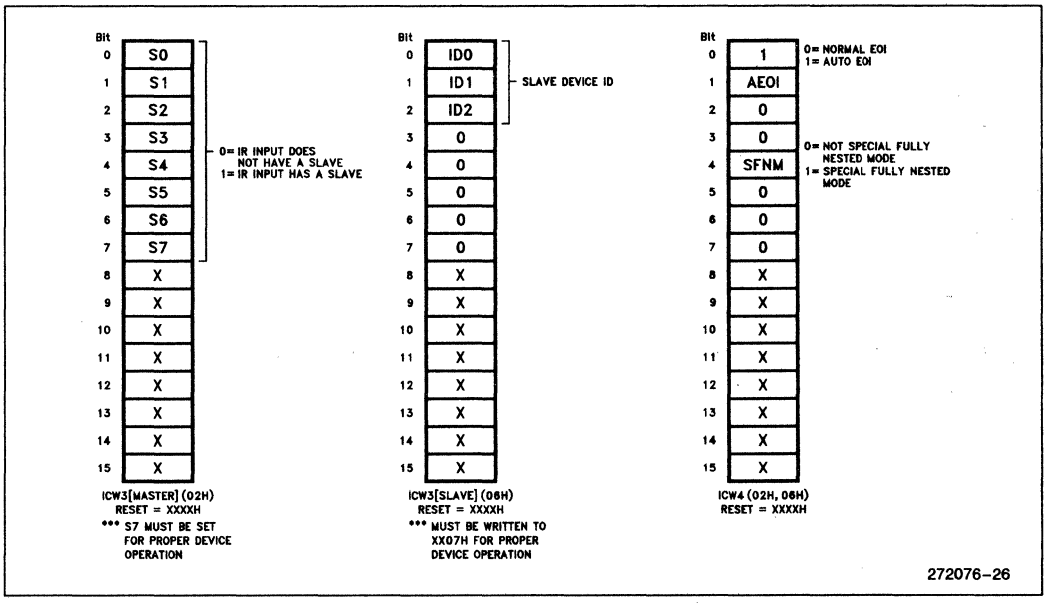


Figure 25. 8259A Module Initialization Command Words (ICWs) (Continued)

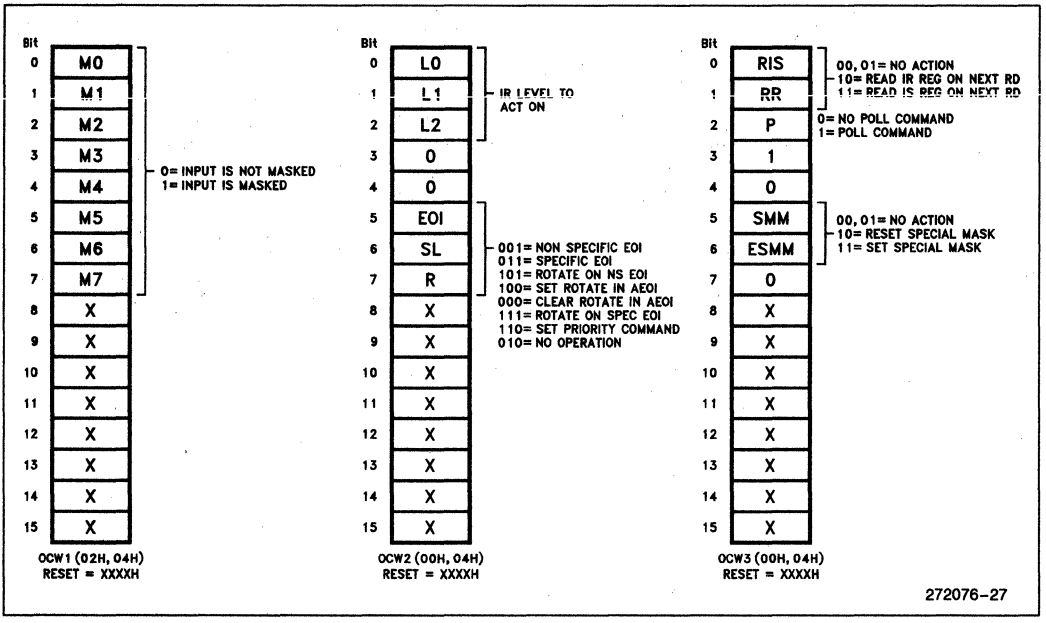


Figure 26. 8259A Module Operation Command Words

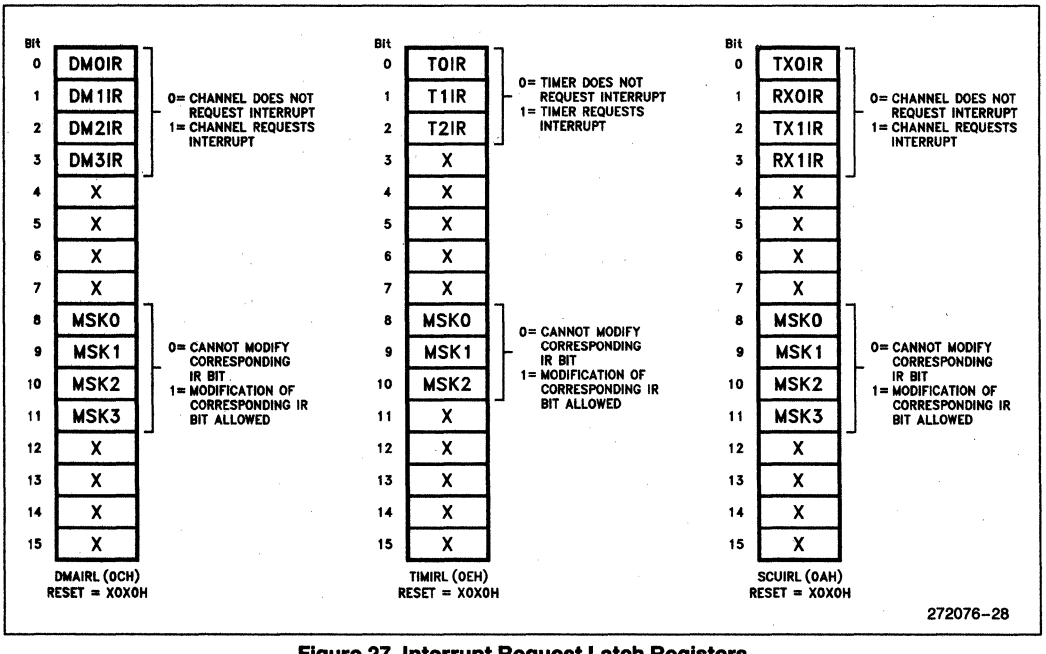


Figure 27. Interrupt Request Latch Registers

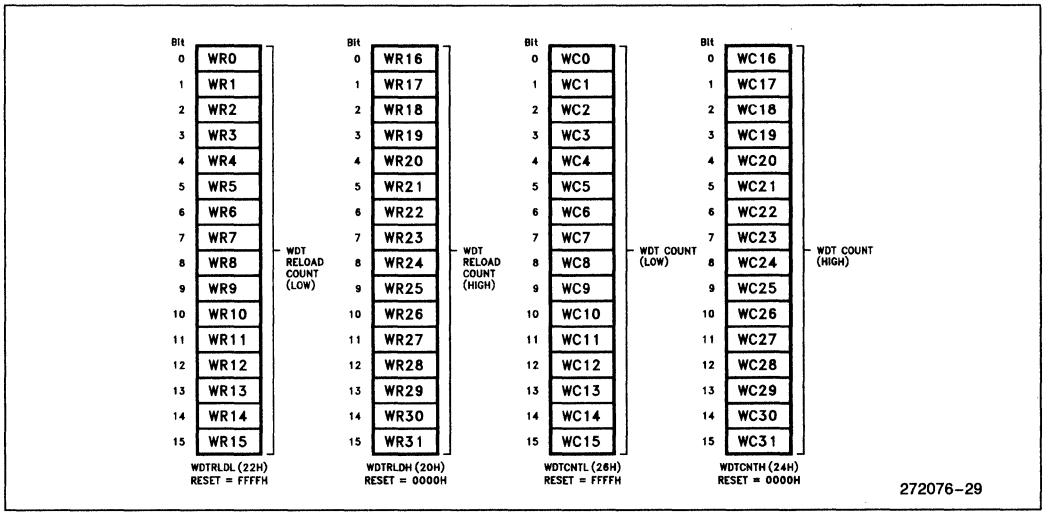


Figure 28. Watchdog Timer Registers

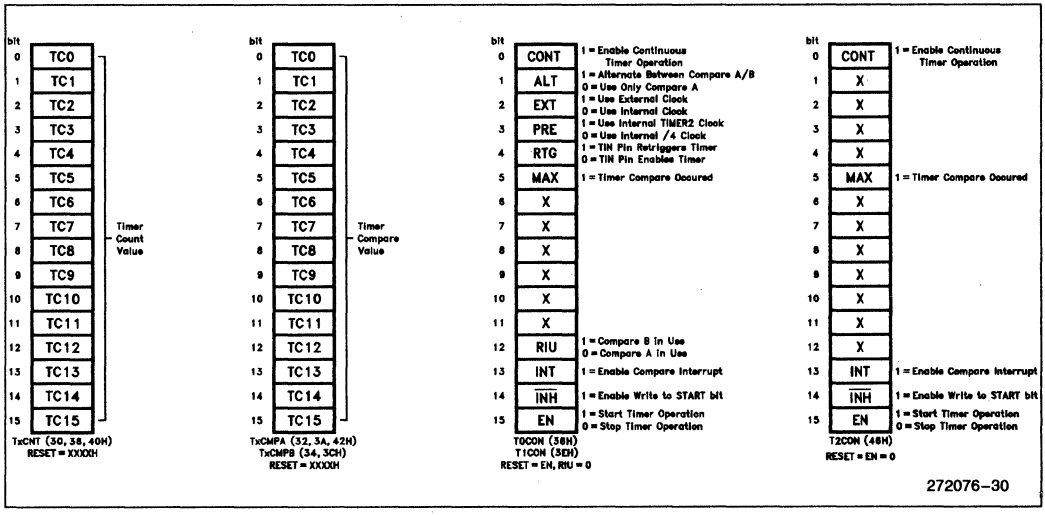


Figure 29. Timer Control Unit Registers

24

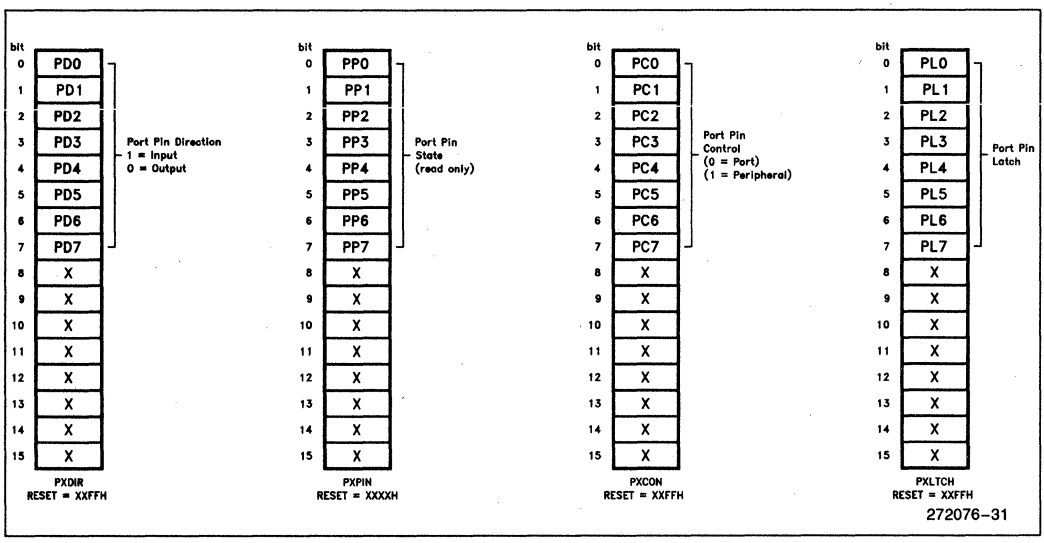


Figure 30. I/O Port Unit Registers

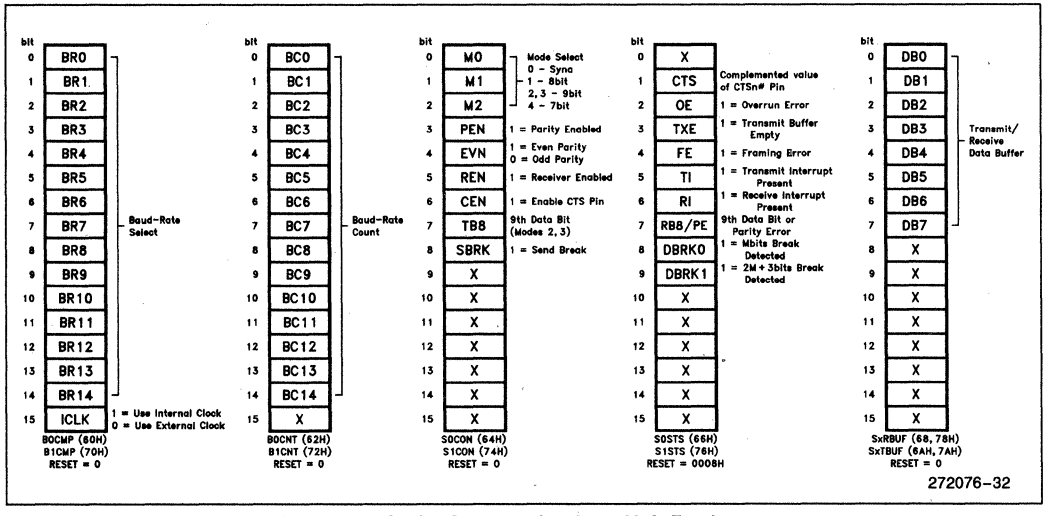


Figure 31. Serial Communications Unit Registers

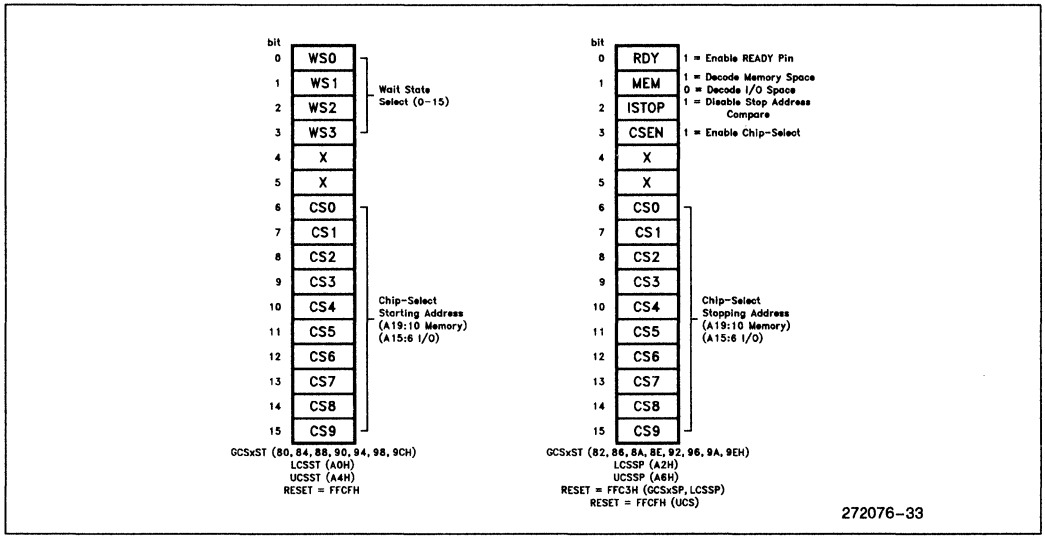


Figure 32. Chip-Select Unit Registers

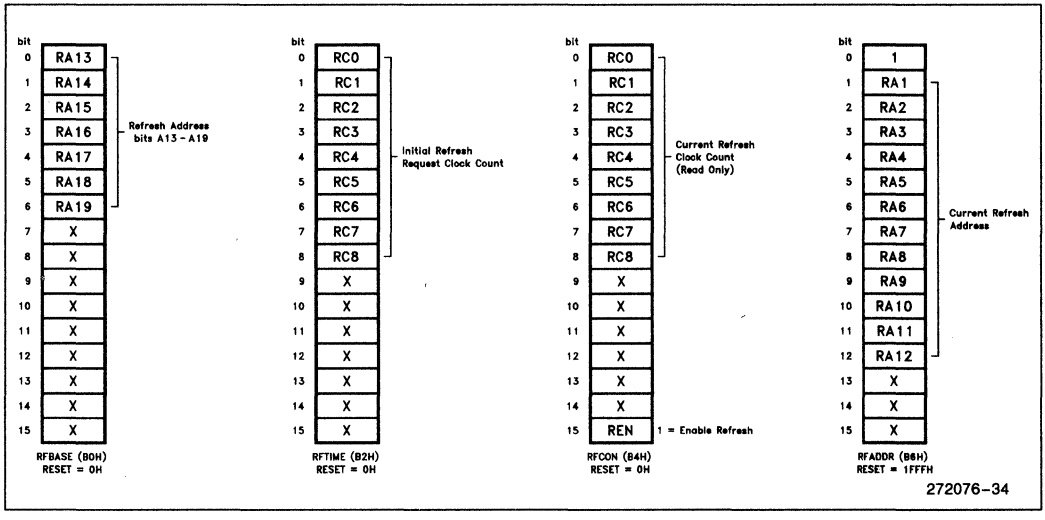


Figure 33. Refresh Control Unit Registers

24

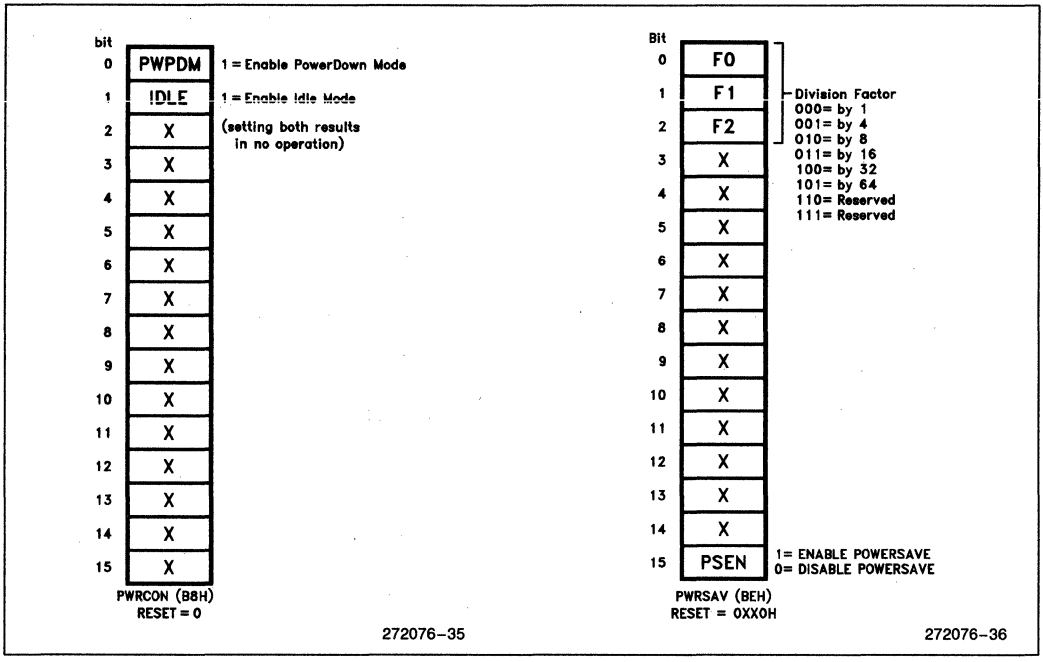


Figure 34. Power Management Unit Registers

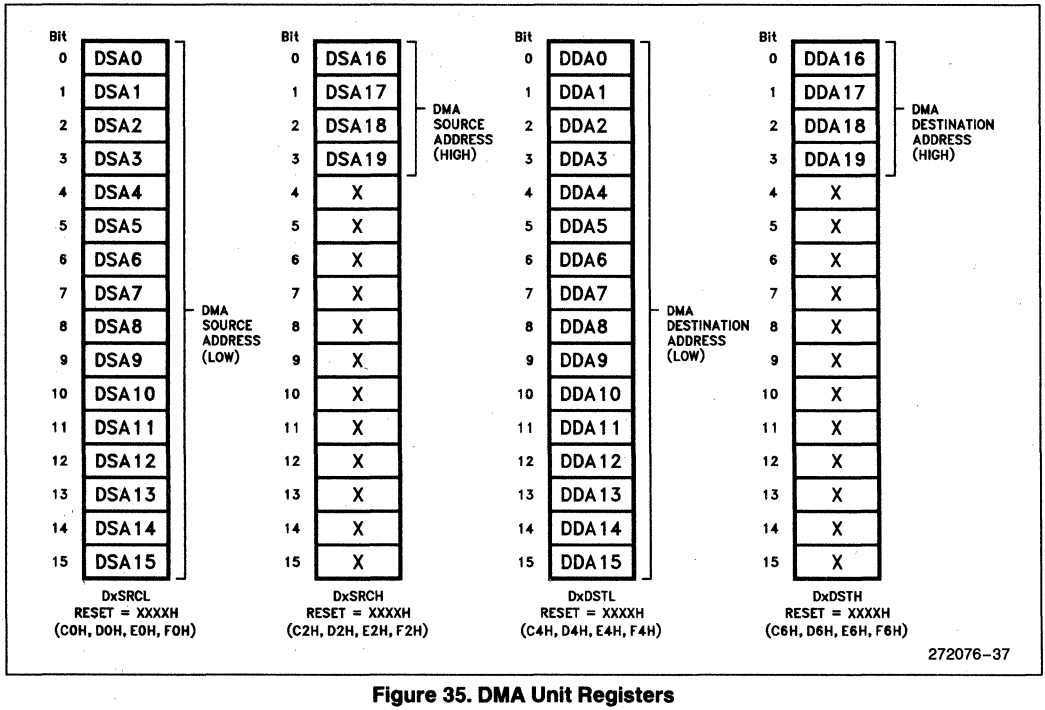


Figure 35. DMA Unit Registers

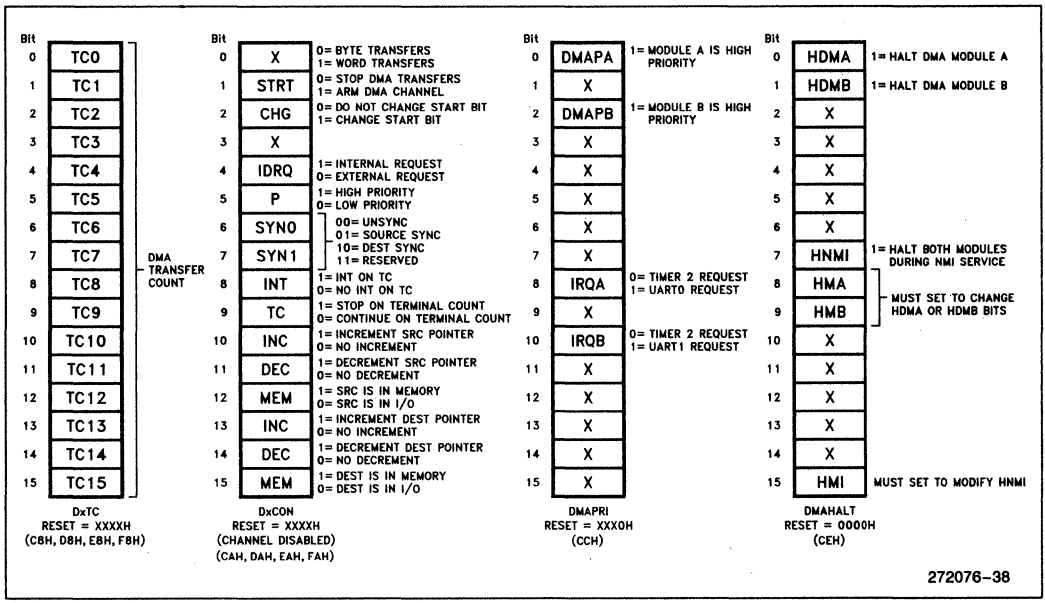


Figure 36. DMA Unit Registers (Continued)

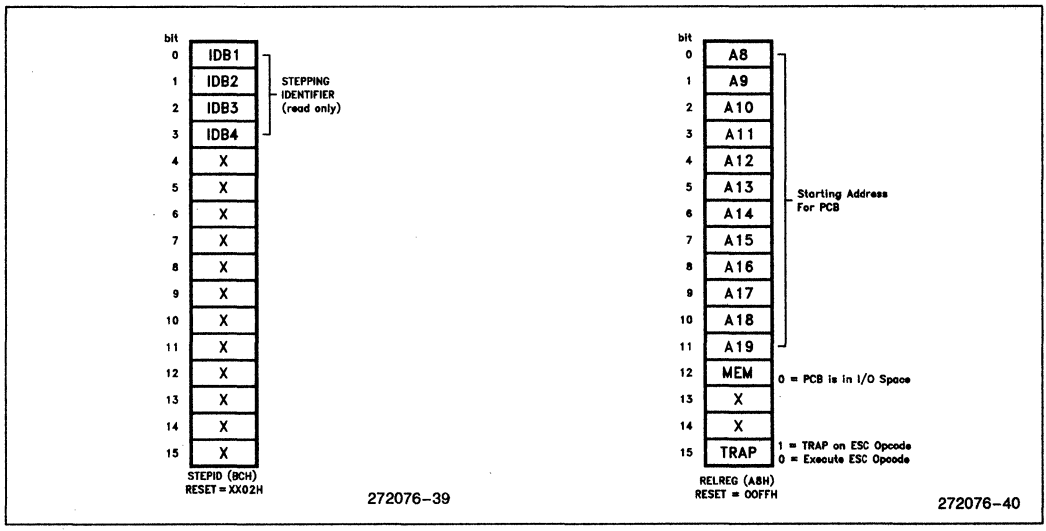


Figure 37. Relocation and Stepping Identifier Registers

24

80C188EC EXECUTION TIMINGS

A determination of 80C188EC program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the **minimum** execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1000100w	mod reg r/m			2/12*	
Register/memory to register	1000101w	mod reg r/m			2/9*	
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	12–13	8/16-bit
Immediate to register	1011w reg	data	data if w=1		3–4	8/16-bit
Memory to accumulator	1010000w	addr-low	addr-high		8*	
Accumulator to memory	1010001w	addr-low	addr-high		9*	
Register/memory to segment register	10001110	mod 0 reg r/m			2/13	
Segment register to register/memory	10001100	mod 0 reg r/m			2/15	
PUSH = Push:						
Memory	11111111	mod 110 r/m			20	
Register	01010 reg				14	
Segment register	000reg110				13	
Immediate	011010s0	data	data if s=0		14	
PUSHA = Push All	01100000				68	
POP = Pop:						
Memory	10001111	mod 000 r/m			24	
Register	01011 reg				14	
Segment register	000reg111	(reg≠01)			12	
POPA = Pop All	01100001				83	
XCHG = Exchange:						
Register/memory with register	1000011w	mod reg r/m			4/17*	
Register with accumulator	10010 reg				3	
IN = Input from:						
Fixed port	1110010w	port			10*	
Variable port	1110110w				8*	
OUT = Output to:						
Fixed port	1110011w	port			9*	
Variable port	1110111w				7*	
XLAT = Translate byte to AL	11010111				15	
LEA = Load EA to register	10001101	mod reg r/m			6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		26	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		26	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				3	
PUSHF = Push flags	10011100				13	
POPF = Pop flags	10011101				12	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word transfers add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16*	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10*	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16*	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15*	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16*	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10*	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16*	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15*	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10*	
Register with register/memory	0011100w	mod reg r/m			3/10*	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10*	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10*	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26–28	
Register-Word					35–37	
Memory-Byte					32–34	
Memory-Word					41–43*	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word transfers add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
ARITHMETIC (Continued)						
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w	mod 1 0 1 r/m				
Register-Byte					25–28	
Register-Word					34–37	
Memory-Byte					31–34	
Memory-Word					40–43*	
IMUL = Integer immediate multiply (signed)	0 1 1 0 1 0 s 1	mod reg r/m	data	data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w	mod 1 1 0 r/m				
Register-Byte					29	
Register-Word					38	
Memory-Byte					35	
Memory-Word					44*	
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w	mod 1 1 1 r/m				
Register-Byte					44–52	
Register-Word					53–61	
Memory-Byte					50–58	
Memory-Word					59–67*	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0			19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0			15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0				2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1				4	
LOGIC						
Shift/Rotate Instructions:						
Register/Memory by 1	1 1 0 1 0 0 0 w	mod TTT r/m			2/15	
Register/Memory by CL	1 1 0 1 0 0 1 w	mod TTT r/m			5+n/17+n	
Register/Memory by Count	1 1 0 0 0 0 0 w	mod TTT r/m	count		5+n/17+n	
	TTT Instruction 0 0 0 ROL 0 0 1 ROR 0 1 0 RCL 0 1 1 RCR 1 0 0 SHL/SAL 1 0 1 SHR 1 1 1 SAR					
AND = **And:**						
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m			3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1		3/4	8/16-bit
TEST = **And function to flags, no result:**						
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m			3/10*	
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1	4/10*	
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1		3/4	8/16-bit
OR = **Or:**						
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m			3/10*	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1		3/4	8/16-bit

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word transfers add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
XOR = Exclusive or:						
Reg/memory and register to either	001100dw	mod reg r/m			3/10*	
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	4/16*	
Immediate to accumulator	0011010w	data	data if w=1		3/4	8/16-bit
NOT = Invert register/memory	1111011w	mod 010 r/m			3/10*	
STRING MANIPULATION						
MOVS = Move byte/word	1010010w				14*	
CMPS = Compare byte/word	1010011w				22*	
SCAS = Scan byte/word	1010111w				15*	
LODS = Load byte/wd to AL/AX	1010110w				12*	
STOS = Store byte/wd from AL/AX	1010101w				10*	
INS = Input byte/wd from DX port	0110110w				14	
OUTS = Output byte/wd to DX port	0110111w				14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	11110010	1010010w			8+8n*	
CMPS = Compare string	1111001z	1010011w			5+22n*	
SCAS = Scan string	1111001z	1010111w			5+15n*	
LODS = Load string	11110010	1010110w			6+11n*	
STOS = Store string	11110010	1010101w			6+9n*	
INS = Input string	11110010	0110110w			8+8n*	
OUTS = Output string	11110010	0110111w			8+8n*	
CONTROL TRANSFER						
CALL = Call:						
Direct within segment	11101000	disp-low	disp-high		19	
Register/memory indirect within segment	11111111	mod 010 r/m			17/27	
Direct intersegment	10011010	segment offset			31	
		segment selector				
Indirect intersegment	11111111	mod 011 r/m	(mod ≠ 11)		54	
JMP = Unconditional jump:						
Short/long	11101011	disp-low			14	
Direct within segment	11101001	disp-low	disp-high		14	
Register/memory indirect within segment	11111111	mod 100 r/m			11/21	
Direct intersegment	11101010	segment offset			14	
		segment selector				
Indirect intersegment	11111111	mod 101 r/m	(mod ≠ 11)		34	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word transfers add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
RET = **Return from CALL:**						
Within segment	11000011				20	
Within seg adding immed to SP	11000010	data-low	data-high		22	
Intersegment	11001011				30	
Intersegment adding immediate to SP	11001010	data-low	data-high		33	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					19	
L = 1					29	
L > 1					26 + 20(n − 1)	
LEAVE = Leave Procedure	11001001				8	
INT = **Interrupt:**						
Type specified	11001101	type			47	
Type 3	11001100				45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110				48/4	
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33-35	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

NOTE:
*Clock cycles shown for byte transfers. For word transfers add 4 clock cycles for all memory transfers.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	
	(TTT LLL are opcode to processor extension)		

Shaded areas indicate instructions not available in 8086/8088 microsystems.

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

80L188EA-13, -8
16-BIT HIGH INTEGRATION EMBEDDED PROCESSOR

- 3V Operation, V_{CC} = 2.7V–5.5V
- Full Static Operation
- True CMOS Inputs and Outputs

- Integrated Feature Set
  - Static 186 CPU Core
  - Power Save, Idle and Powerdown Modes
  - Clock Generator
  - 2 Independent DMA Channels
  - 3 Programmable 16-Bit Timers
  - Dynamic RAM Refresh Control Unit
  - Programmable Memory and Peripheral Chip Select Logic
  - Programmable Wait State Generator
  - Local Bus Controller
  - System-Level Testing Support (High Impedance Test Mode)
- Speed Versions Available:
  - 13 MHz (80L188EA13)
  - 8 MHz (80L188EA8)
- Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O
- Complete System Development Support
  - All 8086/8088 and 80C188 Family Software Development Tools Can Be Used for 80L188EA System Development
    - ASM86 Assembler, iC-86, Pascal-86, FORTRAN-86, PL/M-86, and System Utilities
    - In-Circuit-Emulator (ICE™-186)
- Available in the Following Packages:
  - 68-Pin Plastic Leaded Chip Carrier (PLCC)
  - 80-Pin EIAJ Quad Flat Pack (QFP)
- Available in EXPRESS Extended Temperature Range (−40°C to +85°C)

The 80L188EA is the 3V version of the 80C188EA Embedded Processor. By reducing V_{CC}, further power savings can be realized over the standard 80C188EA, making the 80L188EA ideal for portable, battery-powered applications.

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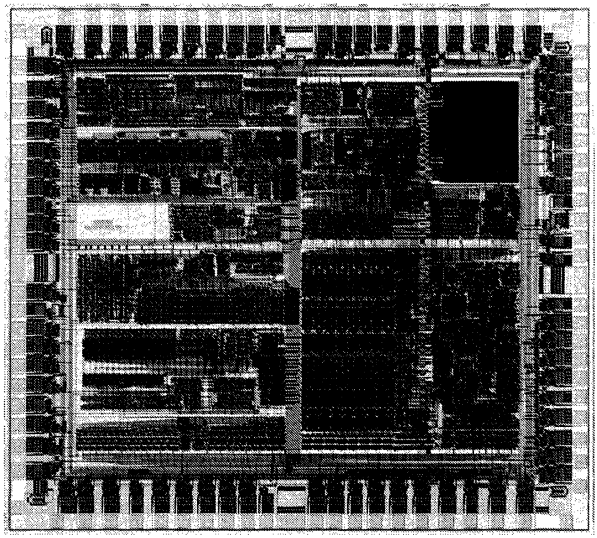

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June 1992
Order Number: 272022-002

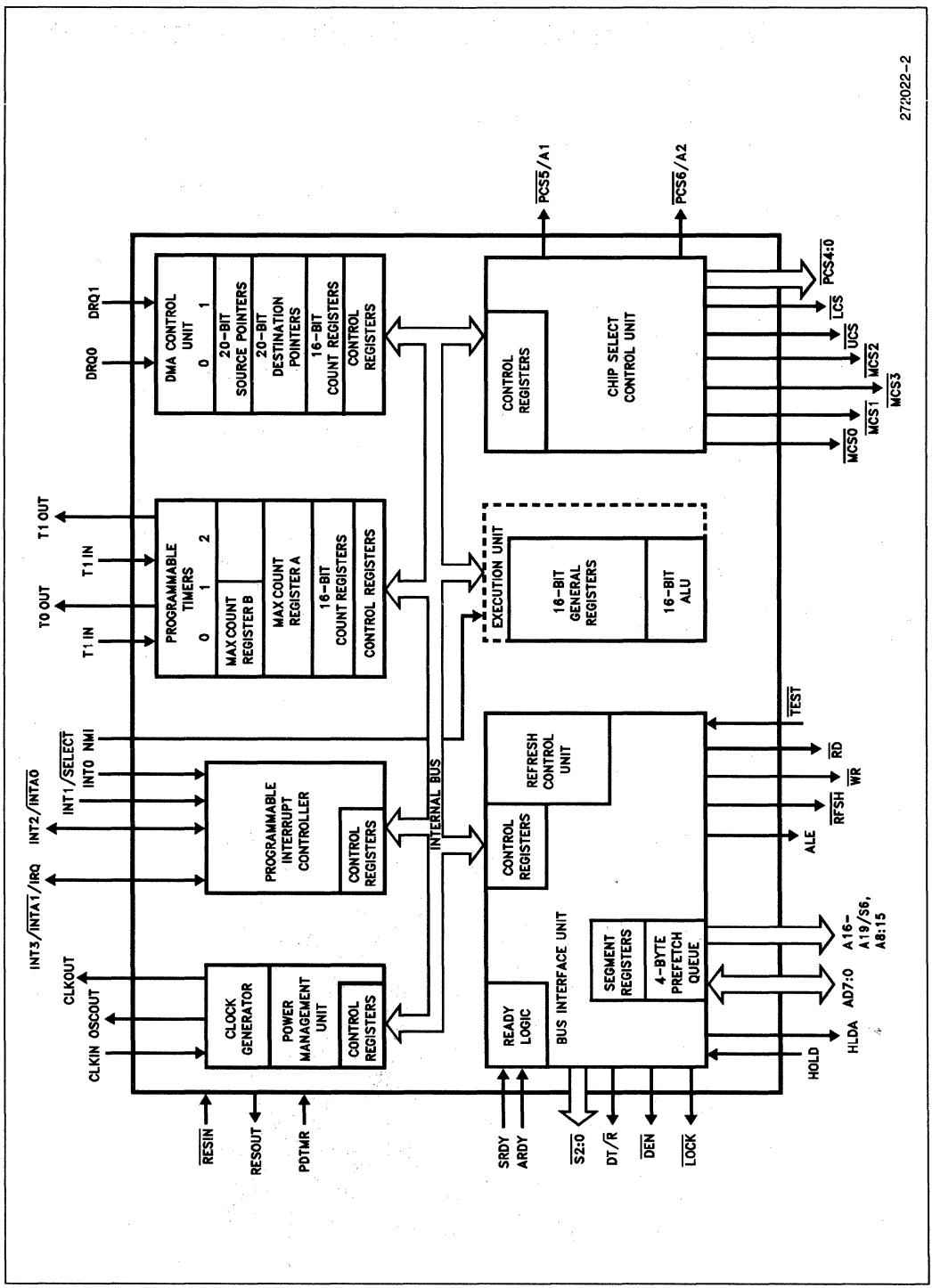

Figure 1. 80L188EA Block Diagram

INTRODUCTION

The 80L188EA is the second member of the 186 Integrated Processor Family to go to 3V operation, following the 80L188EB. The 80L188EA is the 3V version of the 80C188EA. The 80L188EA is functionally compatible with the industry standard 80C188 embedded processor. Current 80C188 users can easily upgrade their designs to use the 80L188EA and benefit from the reduced power consumption of 3V operation.

The feature set of the 80L188EA meets the needs of battery-powered applications. Battery-powered applications benefit from the static CPU core and peripherals. Minimum current consumption is achieved by combining low voltage operation along with the features of the Power Management Unit, thus maximizing battery life. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space-critical applications benefit from the integration of commonly used system peripherals. Two flexible DMA channels perform CPU-independent data transfers. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 128 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters round out the feature set of the 80L188EA.

OVERVIEW

Figure 1 shows a block diagram of the 80L188EA. The Execution Unit (EU) is an enhanced 8086 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instructions, and static operation. The Bus Interface Unit (BIU) is the same as that found on the original 80C188 family products. An independent internal bus is used to allow communication between the BIU and internal peripherals.

Pinout Compatibility

The 80L188EA requires a PDTMR pin to time the processor's exit from Powerdown Mode. The original pin arrangement for the 80C188 in the PLCC package did not have any spare leads to use for PDTMR, so the DT/$\overline{R}$ pin was sacrificed. The arrangement of all the other leads in the 68-lead PLCC is identical between the 80C188 and the 80L188EA. DT/$\overline{R}$ may be readily synthesized by latching the $\overline{S1}$ status output. Therefore, upgrading a PLCC 80C188 to PLCC 80L188EA is particularly straightforward. You must connect a capacitor to the 80L188EA PDTMR pin in order to use Powerdown Mode.

The 80-lead QFP (EIAJ) pinouts are distinctly different between the 80C188 and the 80L188EA. In addition to the PDTMR pin, the 80L188EA has more power and ground pins and the overall arrangement of pins was shifted. A new circuit board layout for the 80L188EA is required.

Operating Modes

The 80C188 has two operating modes, Compatible and Enhanced. Compatible Mode is a pin-to-pin replacement for the NMOS 80188, except for numerics coprocessing. In Enhanced Mode, the processor has a Refresh Control Unit and the Power-Save feature. The 80L188EA does not have different operating modes. All 80L188EA features are present in regular operation.

PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the 80L188EA in the Plastic Leaded Chip Carrier (PLCC) package and Quad Flat Pack (QFP) package. For complete package specifications and information, see the Intel Packaging Outlines and Dimensions Guide (Order Number: 231369).

Pin Descriptions

Each pin or logical set of pins is described in Table 2. There are three columns for each entry in the Pin Description Table.

The **Pin Name** column contains a mnemonic that describes the pin function. Negation of the signal name (for example, $\overline{RESIN}$) denotes a signal that is active low.

The **Pin Type** column contains two kinds of information. The first symbol indicates whether a pin is power (P), ground (G), input only (I), output only (O) or input/output (I/O). Some pins have multiplexed functions (for example, A19/S6). Additional symbols indicate additional characteristics for each pin. Table 4 lists all the possible symbols for this column.

Input pins may be either synchronous or asynchronous. Asynchronous pins require that setup and hold times be met only in order to guarantee *recognition* at a particular clock edge. Synchronous pins require that setup and hold times be met to guarantee proper *operation*. For example, missing the setup or hold time for the SRDY pin (a synchronous input) will re-

sult in a system failure or lockup. Input pins may also be edge- or level-sensitive. The possible characteristics for input pins are S(E), S(L), A(E) and A(L).

Output states are dependent upon the current activity of the processor. There are four operational states that are different from regular operation: bus hold, reset, Idle Mode, and Powerdown Mode. Appropriate characteristics for these states are also indicated in this column, with the legend for all possible characteristics in Table 1.

Finally, the **Pin Description** column contains a text description of each pin.

As an example, consider AD7:0. I/O signifies the pins are bidirectional. S(L) signifies that the input function is synchronous and level-sensitive. H(Z) signifies that, as outputs, the pins are high-impedance upon acknowledgement of bus hold. R(Z) signifies that the pins float during reset. P(X) signifies that the pins retain their states during Powerdown Mode.

Table 1. Pin Description Nomenclature

Symbol	Description
P	Power Pin (Apply $+V_{CC}$ Voltage)
G	Ground (Connect to V_{SS})
I	Input Only Pin
O	Output Only Pin
I/O	Input/Output Pin
S(E)	Synchronous, Edge Sensitive
S(L)	Synchronous, Level Sensitive
A(E)	Asynchronous, Edge Sensitive
A(L)	Asynchronous, Level Sensitive
H(1)	Output Driven to V_{CC} during Bus Hold
H(0)	Output Driven to V_{SS} during Bus Hold
H(Z)	Output Floats during Bus Hold
H(Q)	Output Remains Active during Bus Hold
H(X)	Output Retains Current State during Bus Hold
R(WH)	Output Weakly Held at V_{CC} during Reset
R(1)	Output Driven to V_{CC} during Reset
R(0)	Output Driven to V_{SS} during Reset
R(Z)	Output Floats during Reset
R(Q)	Output Remains Active during Reset
R(X)	Output Retains Current State during Reset
I(1)	Output Driven to V_{CC} during Idle Mode
I(0)	Output Driven to V_{SS} during Idle Mode
I(Z)	Output Floats during Idle Mode
I(Q)	Output Remains Active during Idle Mode
I(X)	Output Retains Current State during Idle Mode
P(1)	Output Driven to V_{CC} during Powerdown Mode
P(0)	Output Driven to V_{SS} during Powerdown Mode
P(Z)	Output Floats during Powerdown Mode
P(Q)	Output Remains Active during Powerdown Mode
P(X)	Output Retains Current State during Powerdown Mode

Table 2. 80L188EA Pin Descriptions

Name	Type	Description
V_{CC}		**POWER** connections consist of six pins which must be shorted externally to a V_{CC} board plane.
V_{SS}		**GROUND** connections consist of five pins which must be shorted externally to a V_{SS} board plane.
CLKIN	I A(E)	**CLocK INput** is an input for an external clock. An external oscillator operating at two times the required 80L188EA operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O H(Q) R(Q) P(Q)	**OSCillator OUTput** is only used when using a crystal to generate the external clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin is not to be used as 2X clock output for non-crystal applications (i.e., this pin is N.C. for non-crystal applications). OSCOUT does not float in ONCE mode.
CLKOUT	O H(Q) R(Q) P(Q)	**CLocK OUTput** provides a timing reference for inputs and outputs of the processor, and is one-half the input clock (CLKIN) frequency. CLKOUT has a 50% duty cycle and transistions every falling edge of CLKIN.
$\overline{\text{RESIN}}$	I A(L)	**RESet IN** causes the 80L188EA to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT with CLKIN before the 80L188EA begins fetching opcodes at memory location 0FFFF0H.
RESOUT	O H(0) R(1) P(0)	**RESet OUTput** that indicates the 80L188EA is currently in the reset state. RESOUT will remain active as long as $\overline{\text{RESIN}}$ remains active.
PDTMR	I/O A(L) H(WH) R(Z) P(1)	**Power-Down TiMeR** pin (normally connected to an external capacitor) that determines the amount of time the 80L188EA waits after an exit from power down before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I A(E)	**Non-Maskable Interrupt** input causes a Type 2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{\text{TEST}}$	I A(E)	$\overline{\text{TEST}}$ is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (low).
AD7:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed **Address** and **Data** bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE. 8- or 16-bit data information is transferred during the data phase of the bus cycle.
A15:8	O H(Z) R(Z) P(Z)	These pins provide **Address** information throughout the entire bus cycle.
A18:16 A19/S6	H(Z) R(Z) P(X)	These pins provide multiplexed **Address** during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. A18:16 are driven to a logic 0 during the data phase of the bus cycle. Also during the data phase, S6 is driven to a logic 0 to indicate a CPU-initiated bus cycle or logic 1 to indicate a DMA-initiated bus cycle or a refresh cycle.

Table 2. 80L188EA Pin Descriptions (Continued)

Name	Type	Description
$\overline{S2:0}$	O H(Z) R(Z) P(1)	Bus cycle **Status** are encoded on these pins to provide bus transaction information. $\overline{S2:0}$ are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ Bus Cycle Initiated 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive (no bus activity)
ALE/QS0	O H(0) R(0) P(0)	**Address Latch Enable** output is used to strobe address information into a transparent type latch during the address phase of the bus cycle. In Queue Status Mode, QS0 provides queue status information along with QS1.
$\overline{RFSH}$	O H(Z) R(Z) P(1)	**ReFreSH** output signals that a refresh cycle is in progress.
$\overline{RD}/\overline{QSMD}$	I/O H(Z) R(WH) P(1)	**ReaD** output signals that the accessed memory or I/O device must drive data information onto the data bus. Upon reset, this pin has an alternate function. As $\overline{QSMD}$, it enables **Queue Status Mode** when grounded. In Queue Status Mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide the following information about processor/instruction queue interaction: QS1 QS0 Queue Operation 0 0 No Queue Operation 0 1 First Opcode Byte Fetched from the Queue 1 1 Subsequent Byte Fetched from the Queue 1 0 Empty the Queue
$\overline{WR}$/QS1	O H(Z) R(Z) P(1)	**WRite** output signals that data available on the data bus are to be written into the accessed memory or I/O device. In Queue Status Mode, QS1 provides queue status information along with QS0.
ARDY	I A(L) S(L)	**Asychronous ReaDY** is an input to signal for the end of a bus cycle. ARDY is asynchronous on rising CLKOUT and synchronous on falling CLKOUT. ARDY or SRDY must be active to terminate any 80L188EA bus cycle, unless they are ignored due to correct programming of the Chip Select Unit.
SRDY	I S(L)	**Synchronous ReaDY** is an input to signal for the end of a bus cycle. ARDY or SRDY must be active to terminate any 80L188EA bus cycle, unless they are ignored due to correct programming of the Chip Select Unit.
$\overline{DEN}$	O H(Z) R(Z) P(1)	**Data ENable** output to control the enable of bidirectional transceivers when buffering an 80L188EA system. $\overline{DEN}$ is active only when data is to be transferred on the bus.

Table 2. 80L188EA Pin Descriptions (Continued)

Name	Type	Description
DT/$\overline{R}$	O H(Z) R(Z) P(X)	**Data Transmit/Receive** output controls the direction of a bi-directional buffer when buffering an 80L188EA system. DT/$\overline{R}$ is only available for the QFP (EIAJ) package (S80L188EA).
$\overline{LOCK}$	I/O H(Z) R(WH) P(1)	**LOCK** output indicates that the bus cycle in progress is not to be interrupted. The 80L188EA will not service other bus requests (such as HOLD) while $\overline{LOCK}$ is active. This pin is configured as a weakly held high input while $\overline{RESIN}$ is active and must not be driven low.
HOLD	I A(L)	**HOLD** request input to signal that an external bus master wishes to gain control of the local bus. The 80L188EA will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
HLDA	O H(1) R(0) P(0)	**HoLD Acknowledge** output to indicate that the 80L188EA has relinquish control of the local bus. When HLDA is asserted, the 80L188EA will (or has) floated its data bus and control signals allowing another bus master to drive the signals directly.
$\overline{UCS}$	O H(1) R(1) P(1)	**Upper Chip Select** will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, $\overline{UCS}$ is configured to be active for memory accesses between 0FFC00H and 0FFFFFH. During a processor reset, $\overline{UCS}$ and $\overline{LCS}$ are used to enable ONCE Mode.
$\overline{LCS}$	O H(1) R(1) P(1)	**Lower Chip Select** will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. $\overline{LCS}$ is inactive after a reset. During a processor reset, $\overline{UCS}$ and $\overline{LCS}$ are used to enable ONCE Mode.
$\overline{MCS3:0}$	O H(1) R(1) P(1) A(L)	If enabled, these pins comprise a block of **Mid-Range Chip Select** outputs which will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user.
$\overline{PCS4:0}$	O H(1) R(1) P(1)	**Peripheral Chip Selects** go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user.
$\overline{PCS5}$/A1 $\overline{PCS6}$/A2	0 H(1)/H(X) R(1) P(1)	These pins provide a multiplexed function. As additional **Peripheral Chip Selects,** they go active whenever the address of a memory or I/O bus cycle is within the address limitations by the user. They may also be programmed to provide latched **Address** A2:1 signals.
T0OUT T1OUT	O H(Q) R(1) P(Q)	**Timer OUTput** pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.
T0IN T1IN	I A(L) A(E)	**Timer INput** is used either as clock or control signals, depending on the timer mode selected.

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Table 2. 80L188EA Pin Descriptions (Continued)

Name	Type	Description
DRQ0 DRQ1	I A(L)	**DMA ReQuest** is asserted by an external request when it is prepared for a DMA transfer.
INT0 INT1/$\overline{\text{SELECT}}$	I A(E,L)	Maskable **INTerrupt** input will cause a vector to a specific Type interrupt routine. To allow interrupt expansion, INT0 and/or INT1 can be used with $\overline{\text{INTA0}}$ and $\overline{\text{INTA1}}$ to interface with an external slave controller. INT1 becomes $\overline{\text{SELECT}}$ when the ICU is configured for Slave Mode.
INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$/IRQ	I/O A(E,L) /H(1) R(Z) /P(1)	These pins provide multiplexed functions. As inputs, they provide a maskable **INTerrupt** that will cause the CPU to vector to a specific Type interrupt routine. As outputs, each is programmatically controlled to provide an **INTerrupt Acknowledge** handshake signal to allow interrupt expansion. INT3/$\overline{\text{INTA1}}$ becomes **IRQ** when the ICU is configured for Slave Mode.
N.C.	—	**No Connect.** For compatibility with future products, do not connect to these pins.

80L188EA PINOUT

Tables 3 and 4 list the 80L188EA pin names with package location for the 68-pin Plastic Leaded Chip Carrier (PLCC) component. Figure 2 depicts the complete 80L188EA pinout (PLCC package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 5 and 6 list the 80L188EA pin names with package location for the 80-pin Quad Flat Pack (EIAJ) component. Figure 3 depicts the complete 80L188EA (EIAJ QFP package) as viewed from the top side of the component (i.e., contacts facing down).

Table 3. PLCC Pin Names with Package Location

Address/Data Bus	
Name	**Location**
AD0	17
AD1	15
AD2	13
AD3	11
AD4	8
AD5	6
AD6	4
AD7	2
A8	16
A9	14
A10	12
A11	10
A12	7
A13	5
A14	3
A15	1
A16	68
A17	67
A18	66
A19/S6	65

Bus Control	
Name	**Location**
ALE/QS0	61
$\overline{\text{RFSH}}$	64
$\overline{\text{S0}}$	52
$\overline{\text{S1}}$	53
$\overline{\text{S2}}$	54
$\overline{\text{RD}}$/$\overline{\text{QSMD}}$	62
$\overline{\text{WR}}$/QS1	63
ARDY	55
SRDY	49
$\overline{\text{DEN}}$	39
$\overline{\text{LOCK}}$	48
HOLD	50
HLDA	51

Power	
Name	**Location**
V_{SS}	26, 60
V_{CC}	9, 43

Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	24
RESOUT	57
CLKIN	59
OSCOUT	58
CLKOUT	56
$\overline{\text{TEST}}$	47
PDTMR	40
NMI	46
INT0	45
INT1/SELECT	44
INT2/$\overline{\text{INTA0}}$	42
INT3/$\overline{\text{INTA1}}$/IRQ	41

I/O	
Name	**Location**
$\overline{\text{UCS}}$	34
$\overline{\text{LCS}}$	33
$\overline{\text{MCS0}}$	38
$\overline{\text{MCS1}}$	37
$\overline{\text{MCS2}}$	36
$\overline{\text{MCS3}}$	35
$\overline{\text{PCS0}}$	25
$\overline{\text{PCS1}}$	27
$\overline{\text{PCS2}}$	28
$\overline{\text{PCS3}}$	29
$\overline{\text{PCS4}}$	30
$\overline{\text{PCS5}}$/A1	31
$\overline{\text{PCS6}}$/A2	32
T0OUT	22
T0IN	20
T1OUT	23
T1IN	21
DRQ0	18
DRQ1	19

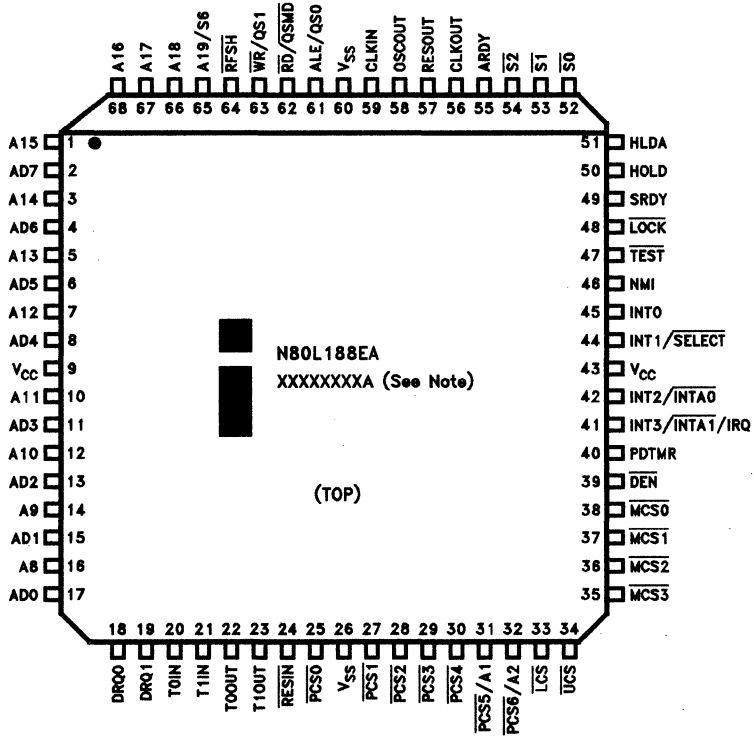
Table 4. PLCC Package Locations with Pin Name

Location	Name
1	A15
2	AD7
3	A14
4	AD6
5	A13
6	AD5
7	A12
8	AD4
9	V_{CC}
10	A11
11	AD3
12	A10
13	AD2
14	A9
15	AD1
16	A8
17	AD0

Location	Name
18	DRQ0
19	DRQ1
20	T0IN
21	T1IN
22	T0OUT
23	T1OUT
24	$\overline{RESIN}$
25	$\overline{PCS0}$
26	V_{SS}
27	$\overline{PCS1}$
28	$\overline{PCS2}$
29	$\overline{PCS3}$
30	$\overline{PCS4}$
31	$\overline{PCS5}$/A1
32	$\overline{PCS6}$/A2
33	$\overline{LCS}$
34	$\overline{UCS}$

Location	Name
35	$\overline{MCS3}$
36	$\overline{MCS2}$
37	$\overline{MCS1}$
38	$\overline{MCS0}$
39	$\overline{DEN}$
40	PDTMR
41	INT3/$\overline{INTA1}$/ IRQ
42	INT2/$\overline{INTA0}$
43	V_{CC}
44	INT1/SELECT
45	INT0
46	NMI
47	$\overline{TEST}$
48	LOCK
49	SRDY
50	HOLD
51	HLDA

Location	Name
52	$\overline{S0}$
53	$\overline{S1}$
54	$\overline{S2}$
55	ARDY
56	CLKOUT
57	RESOUT
58	OSCOUT
59	CLKIN
60	V_{SS}
61	ALE/QS0
62	$\overline{RD}$/$\overline{QSMD}$
63	$\overline{WR}$/QS1
64	$\overline{RFSH}$
65	A19/S6
66	A18
67	A17
68	A16



NOTE:
The nine-character alphanumeric code (XXXXXXXXA) underneath the product number is the Intel FPO number.

Figure 2. 68-Lead PLCC Pinout Diagram

Table 5. QFP (EIAJ) Pin Name with Package Location

Address/Data Bus	
Name	**Location**
AD0	64
AD1	66
AD2	68
AD3	70
AD4	74
AD5	76
AD6	78
AD7	80
A8	65
A9	67
A10	69
A11	71
A12	75
A13	77
A14	79
A15	1
A16	3
A17	4
A18	5
A19/S6	6

Bus Control	
Name	**Location**
ALE/QS0	10
$\overline{\text{RFSH}}$	7
$\overline{\text{S0}}$	23
$\overline{\text{S1}}$	22
$\overline{\text{S2}}$	21
$\overline{\text{RD}}$/$\overline{\text{QSMD}}$	9
$\overline{\text{WR}}$/QS1	8
ARDY	20
SRDY	27
DT/$\overline{\text{R}}$	37
$\overline{\text{DEN}}$	39
$\overline{\text{LOCK}}$	28
HOLD	26
HLDA	25

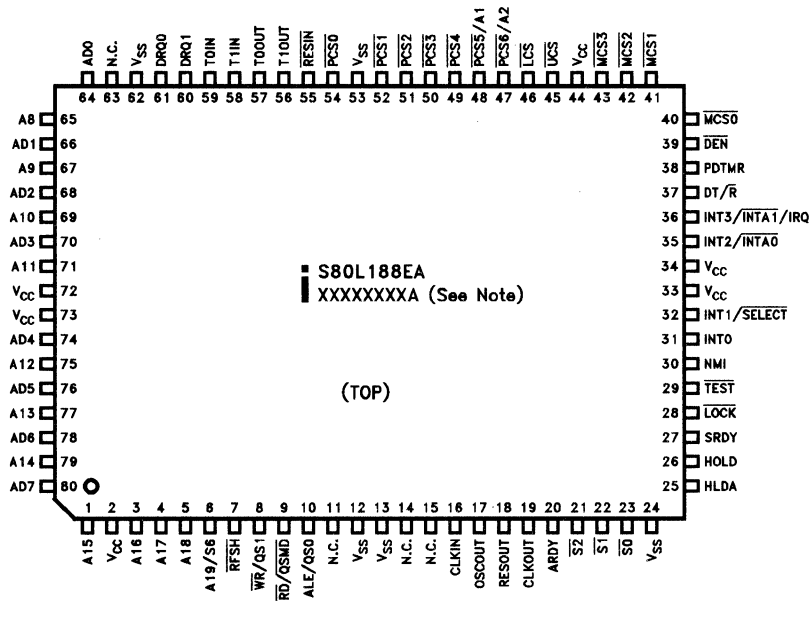
Power	
Name	**Location**
V_{SS}	12, 13, 24, 53, 62
V_{CC}	2, 33, 34, 44, 72, 73

Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	55
RESOUT	18
CLKIN	16
OSCOUT	17
CLKOUT	19
$\overline{\text{TEST}}$	29
PDTMR	38
NMI	30
INT0	31
INT1/$\overline{\text{SELECT}}$	32
INT2/$\overline{\text{INTA0}}$	35
INT3/$\overline{\text{INTA1}}$/ IRQ	36
N.C.	11, 14, 15, 63

I/O	
Name	**Location**
$\overline{\text{UCS}}$	45
$\overline{\text{LCS}}$	46
$\overline{\text{MCS0}}$	40
$\overline{\text{MCS1}}$	41
$\overline{\text{MCS2}}$	42
$\overline{\text{MCS3}}$	43
$\overline{\text{PCS0}}$	54
$\overline{\text{PCS1}}$	52
$\overline{\text{PCS2}}$	51
$\overline{\text{PCS3}}$	50
$\overline{\text{PCS4}}$	49
$\overline{\text{PCS5}}$/A1	48
$\overline{\text{PCS6}}$/A2	47
T0OUT	57
T0IN	59
T1OUT	56
T1IN	58
DRQ0	61
DRQ1	60

Table 6. QFP (EIAJ) Package Location with Pin Names

Location	Name	Location	Name	Location	Name	Location	Name
1	A15	21	$\overline{S2}$	41	$\overline{MCS1}$	61	DRQ0
2	V_{CC}	22	$\overline{S1}$	42	$\overline{MCS2}$	62	V_{SS}
3	A16	23	$\overline{S0}$	43	$\overline{MCS3}$	63	N.C.
4	A17	24	V_{SS}	44	V_{CC}	64	AD0
5	A18	25	HLDA	45	$\overline{UCS}$	65	A8
6	A19/S6	26	HOLD	46	$\overline{LCS}$	66	AD1
7	$\overline{RFSH}$	27	SRDY	47	$\overline{PCS6}$/A2	67	A9
8	$\overline{WR}$/QS1	28	$\overline{LOCK}$	48	$\overline{PCS5}$/A1	68	AD2
9	$\overline{RD}$/$\overline{QSMD}$	29	$\overline{TEST}$	49	$\overline{PCS4}$	69	A10
10	ALE/QS0	30	NMI	50	$\overline{PCS3}$	70	AD3
11	N.C.	31	INT0	51	$\overline{PCS2}$	71	A11
12	V_{SS}	32	INT1/$\overline{SELECT}$	52	$\overline{PCS1}$	72	V_{CC}
13	V_{SS}	33	V_{CC}	53	V_{SS}	73	V_{CC}
14	N.C.	34	V_{CC}	54	$\overline{PCS0}$	74	AD4
15	N.C.	35	INT2/$\overline{INTA0}$	55	$\overline{RESIN}$	75	A12
16	CLKIN	36	INT3/$\overline{INTA1}$/	56	T1OUT	76	AD5
17	OSCOUT		IRQ	57	T0OUT	77	A13
18	RESOUT	37	DT/$\overline{R}$	58	T1IN	78	AD6
19	CLKOUT	38	PDTMR	59	T0IN	79	A14
20	ARDY	39	$\overline{DEN}$	60	DRQ1	80	AD7
		40	$\overline{MCS0}$				



NOTE:
The nine-character alphanumeric code (XXXXXXXXA) underneath the product number is the Intel FPO number.

Figure 3. Quad Flat Pack (EIAJ) Pinout Diagram

PACKAGE THERMAL SPECIFICATIONS

The 80L188EA is specified for operation when T_C (the case temperature) is within the range of 0°C to 85°C (PLCC package) or 0°C to 106°C (QFP-EIAJ) package. T_C may be measured in any environment to determine whether the 80L188EA is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P \times \theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 7 for the 68-pin Plastic Leaded Chip Carrier (PLCC) package.

Table 8 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies. P (the maximum power consumption, specified in watts) is calculated by using the maximum ICC as tabulated in the DC specifications and V_{CC} of 5V.

Table 7. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow Linear ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PLCC)	29	25	21	19	17	16.5
θ_{CA} (QFP)	66	63	60.5	59	58	57

Table 8. Maximum T_A at Various Airflows (in °C)

		Airflow Linear ft/min (m/sec)					
	T_F (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A (PLCC)	25	78	80	81	82	82.5	83
	32	74	76	78	79	79.5	80
	40	70	72	74	75	76	76.5
T_A (QFP)	25	84	85.5	86	87	87	87.5
	32	77.5	79	80	80.5	81	81.5
	40	70	71.5	73	74	74	75

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +150°C
Case Temperature under Bias ... −65°C to +150°C
Supply Voltage with Respect to V_{SS} ..... −0.5V to +6.5V
Voltage on Other Pins with Respect to V_{SS} ..... −0.5V to V_{CC} + 0.5V

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	5.5	V
T_F	Input Clock Frequency			
	80L188EA13	0	26	MHz
	80L188EA8	0	16	MHz
T_C	Case Temperature under Bias			
	N80L188EA (PLCC)	0	+100	°C
	S80L188EA (QFP)	0	+114	°C

RECOMMENDED CONNECTIONS

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80L188EA based circuit board should contain separate power (V_{CC}) and ground (V_{SS}) planes. All V_{CC} and V_{SS} pins **must** be connected to the appropriate plane. Pins identified as "N.C." must not be connected in the system. Decoupling capacitors should be placed near the 80L188EA. The value and type of decoupling capacitors is application and board layout dependent. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Always connect any unused input pins to an appropriate signal level. In particular, unused interrupt pins (NMI, INT3:0) should be connected to V_{SS} to avoid unwanted interrupts. **Leave any unused output pin or any "N.C." pin unconnected.**

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage for All Pins	−0.5	0.3 V_{CC}	V	
V_{IH}	Input High Voltage for All Pins	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6 mA (min)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −1 mA (min)
V_{HYR}	Input Hysterisis on $\overline{RESIN}$	0.30		V	
I_{IL1}	Input Leakage Current (except $\overline{RD}/QSMD$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{LOCK}$, and $\overline{TEST}$)		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{IL2}	Input Leakage Current ($\overline{RD}/QSMD$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{LOCK}$, and $\overline{TEST}$)	−275		μA	V_{IN} = 0.7 V_{CC} (Note 1)
I_{OL}	Output Leakage Current		±10	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 2)
I_{CC5}	Supply Current (RESET, 5.5V) 80L188EA-13 80L188EA-8		 40	 mA mA	 (Note 3) (Note 3)
I_{CC3}	Supply Current (RESET, 2.7V) 80L188EA-13 80L188EA-8		 20	 mA mA	 (Note 3) (Note 3)
I_{ID5}	Supply Current Idle (5.5V) 80L188EA-13 80L188EA-8		 28	 mA mA	
I_{ID3}	Supply Current Idle (2.7V) 80L188EA-13 80L188EA-8		 14	 mA mA	
I_{PD5}	Supply Current Powerdown (5.5V) 80L188EA-13 80L188EA-8		 100 100	 μA μA	
I_{PD3}	Supply Current Powerdown (2.7V) 80L188EA-13 80L188EA-8		 50 50	 μA μA	
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 4)

NOTES:
1. $\overline{RD}/QSMD$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{TEST}$ and $\overline{LOCK}$, and have internal pullups that are only activated during RESET. Loading these pins above I_{OL} = −275 μA will cause the 80L188EA to enter alternate modes of operation.
2. Output pins are floated using HOLD or ONCE Mode.
3. Measured at worst case temperature and V_{CC} with all outputs loaded as specified in the AC Test Conditions, and with the device in RESET ($\overline{RESIN}$ held low).
4. Output capacitance is the capacitive load of a floating output pin.

I_{CC} VERSUS FREQUENCY AND VOLTAGE

The current (I_{CC}) consumption of the 80L188EA is essentially composed of two components; I_{PD} and I_{CCS}.

I_{PD} is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or V_{CC} (no clock applied to the device). I_{PD} is equal to the Powerdown current and is typically less than 50 μA.

I_{CCS} is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since I_{CCS} is typically much greater than I_{PD}, I_{PD} can often be ignored when calculating I_{CC}.

I_{CCS} is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: V = Device operating voltage (V_{CC})

C_{DEV} = Device capacitance

f = Device operating frequency

$I_{CCS} = I_{CC}$ = Device current

Measuring C_{DEV} on a device like the 80L188EA would be difficult. Instead, C_{DEV} is calculated using the above formula by measuring I_{CC} at a known V_{CC} and frequency (see Table 9). Using this C_{DEV} value, I_{CC} can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical I_{CC} when operating at 20 MHz, 4.8V.

$$I_{CC} = I_{CCS} = 4.8 \times 0.515 \times 20 \approx 49 \text{ mA}$$

PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{\text{RESIN}}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{\text{RESIN}}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: t = desired delay in **seconds**

C_{PD} = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132$ μF is required. Round up to standard (available) capacitive values.

NOTE:
The above equation applies to delay times greater than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperature will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

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Table 9. C_{DEV} Values

Parameter	Typ	Max	Units	Notes
C_{DEV} (Device in Reset)	0.515	0.905	mA/V*MHz	1, 2
C_{DEV} (Device in Idle)	0.391	0.635	mA/V*MHz	1, 2

1. Max C_{DEV} is calculated at −40°C, all floating outputs driven to V_{CC} or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical C_{DEV} is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

AC SPECIFICATIONS

AC Characteristics—80L188EA13

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	26	MHz	1
T_C	CLKIN Period	38.5	∞	ns	1
T_{CH}	CLKIN High Time	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	45	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	15	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	15	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{LOCK}$	3	27	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{RD}$, $\overline{WR}$	3	32	ns	1, 4, 6, 8
T_{CHOV3}	$\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{BHE}$, A19:16	3	30	ns	1, 4, 6, 11
T_{CLOV1}	$\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT	3	27	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{INTA1:0}$	3	32	ns	1, 4, 6
T_{CLOV3}	$\overline{BHE}$, $\overline{DEN}$, A19:16	3	30	ns	1, 4, 6
T_{CLOV4}	A15:8, AD7:0	3	34	ns	1, 4, 6
T_{CLOV5}	$\overline{S2:0}$	3	38	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, AD15:0	0	35	ns	1

NOTES:
1. See **AC Timing Waveforms,** for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 9 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 10 for rise and fall times outside 50 pF.
6. See Figure 10 for rise and fall times.
7. T_{CHOV1} applies to $\overline{LOCK}$ only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L186EA operation (SRDY, AD15:0).
11. T_{CHOV3} applies to $\overline{RFSH}$ and A19:16 only after a HOLD release.

AC SPECIFICATIONS

AC Characteristics—80L188EA13 (Continued)

Symbol	Parameter	Min	Max	Units	Notes
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	25		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		ns	1, 9
T_{CLIS}	AD15:0, ARDY, SRDY, DRQ1:0	25		ns	1, 10
T_{CLIH}	AD15:0, ARDY, SRDY, DRQ1:0	3		ns	1, 10
T_{CLIS}	HOLD	25		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	25		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (from CLKIN)	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 9 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 10 for rise and fall times outside 50 pF.
6. See Figure 10 for rise and fall times.
7. T_{CHOV1} applies to $\overline{LOCK}$ after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L186EA operation (SRDY, AD15:0).
11. T_{CHOV3} applies to $\overline{RFSH}$ and A19:16 only after a HOLD release.

AC SPECIFICATIONS

AC Characteristics—80L188EA8

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	16	MHz	1
T_C	CLKIN Period	62.5	∞	ns	1
T_{CH}	CLKIN High Time	12	∞	ns	1, 2
T_{CL}	CLKIN Low Time	12	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	50	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	15	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	15	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{LOCK}$	3	30	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{RD}$, $\overline{WR}$	3	35	ns	1, 4, 6, 8
T_{CHOV3}	$\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{RFSH}$, A19:16	3	30	ns	1, 4, 6, 11
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	30	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{MCS3:0}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{PCS6:0}$, $\overline{INTA1:0}$	3	35	ns	1, 4, 6
T_{CLOV3}	$\overline{RFSH}$, $\overline{DEN}$, A19:16	3	30	ns	1, 4, 6
T_{CLOV4}	A15:8, AD7:0	3	35	ns	1, 4, 6
T_{CLOV5}	S2:0	3	40	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, A15:8, AD7:0	0	35	ns	1

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 9 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 10 for rise and fall times outside 50 pF.
6. See Figure 10 for rise and fall times.
7. T_{CHOV1} applies to $\overline{LOCK}$ and only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L188EA operation (SRDY, AD7:0).
11. T_{CHOV3} applies to $\overline{RFSH}$ and A19:16 only after a HOLD release.

AC SPECIFICATIONS

AC Characteristics—80L188EA8 (Continued)

Symbol	Parameter	Min	Max	Units	Notes
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	25		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT3:0, T1:0IN, ARDY	3		ns	1, 9
T_{CLIS}	A15:8, AD7:0, ARDY, SRDY, DRQ1:0	25		ns	1, 10
T_{CLIH}	A15:8, AD7:0, ARDY, SRDY, DRQ1:0	3		ns	1, 10
T_{CLIS}	HOLD	25		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9
T_{CLIS}	$\overline{RESIN}$ (to CLKIN)	25		ns	1, 9
T_{CLIH}	$\overline{RESIN}$ (to CLKIN)	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measured at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 9 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 10 for rise and fall times outside 50 pF.
6. See Figure 10 for rise and fall times.
7. T_{CHOV1} applies to $\overline{LOCK}$ and only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L188EA operation (SRDY, AD7:0).
11. T_{CHOV3} applies to $\overline{RFSH}$ and A19:16 only after a HOLD release.

AC SPECIFICATIONS

Relative Timings—80L188EA-13, -8

Symbol	Parameter	Min	Max	Unit	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Rising to ALE Falling	T − 15		ns	
T_{AVLL}	Address Valid to ALE Falling	½T − 10		ns	
T_{PLLL}	Chip Selects Valid to ALE Falling	½T − 10		ns	1
T_{LLAX}	Address Hold from ALE Falling	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{RHLH}	$\overline{RD}$ Rising to ALE Rising	½T − 10		ns	1
T_{WHLH}	$\overline{WR}$ Rising to ALE Rising	½T − 10		ns	1
T_{AFRL}	Address Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Falling to $\overline{RD}$ Rising	(2*T) − 5		ns	2
T_{WLWH}	$\overline{WR}$ Falling to $\overline{WR}$ Rising	(2*T) − 5		ns	2
T_{RHAV}	$\overline{RD}$ Rising to Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHDEX}	$\overline{WR}$ Rising to $\overline{DEN}$ Rising	½T − 10		ns	1
T_{WHPH}	$\overline{WR}$ Rising to Chip Select Rising	½T − 10		ns	1, 4
T_{RHPH}	$\overline{RD}$ Rising to Chip Select Rising	½T − 10		ns	1, 4
T_{PHPL}	$\overline{CS}$ Inactive to $\overline{CS}$ Active	½T − 10		ns	1
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		ns	5
T_{OVRH}	ONCE ($\overline{UCS}$, $\overline{LCS}$) Active to $\overline{RESIN}$ Rising	T		ns	3
T_{RHOX}	ONCE ($\overline{UCS}$, $\overline{LCS}$) to $\overline{RESIN}$ Rising	T		ns	3

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.
3. Not tested.
4. Not applicable to latched A2:1. These signals change only on falling T_1.
5. For write cycle followed by read cycle.

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 4. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

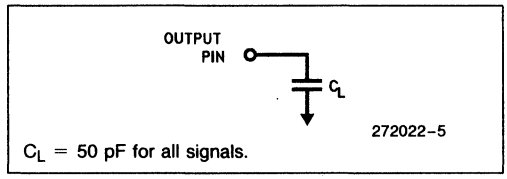

Figure 4. AC Test Load

AC TIMING WAVEFORMS

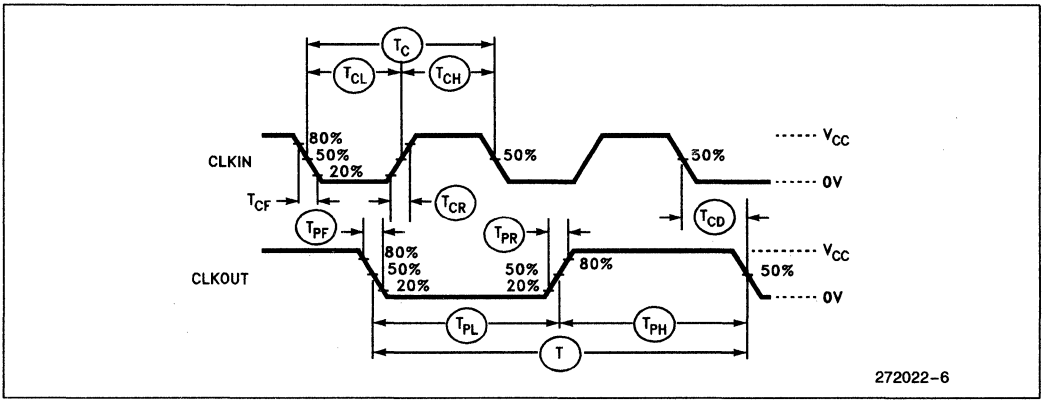

Figure 5. Input and Output Clock Waveform

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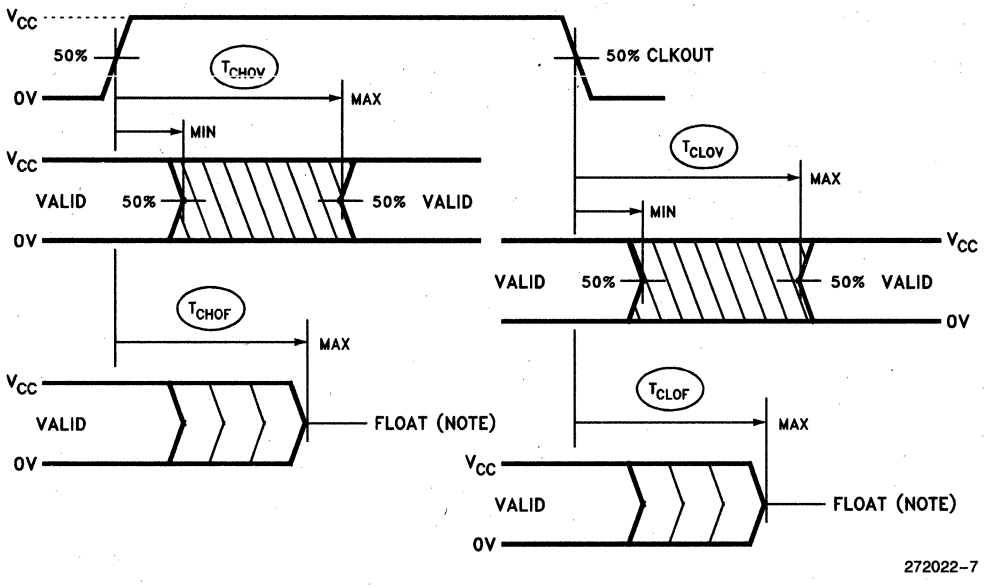
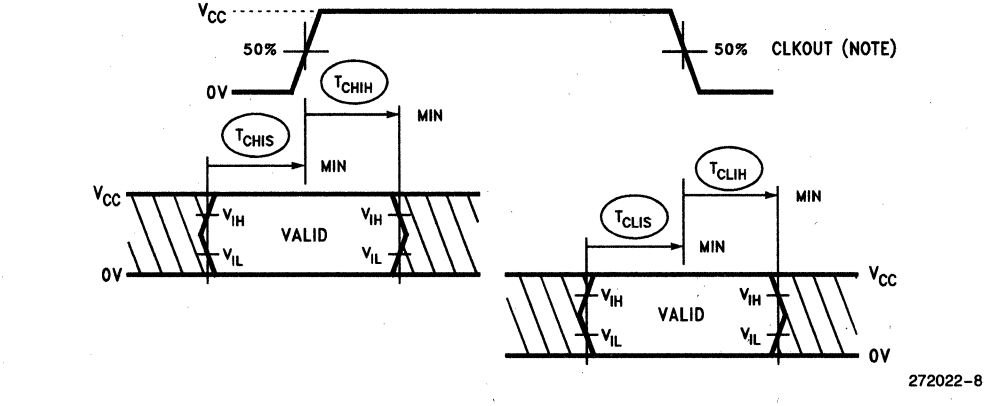


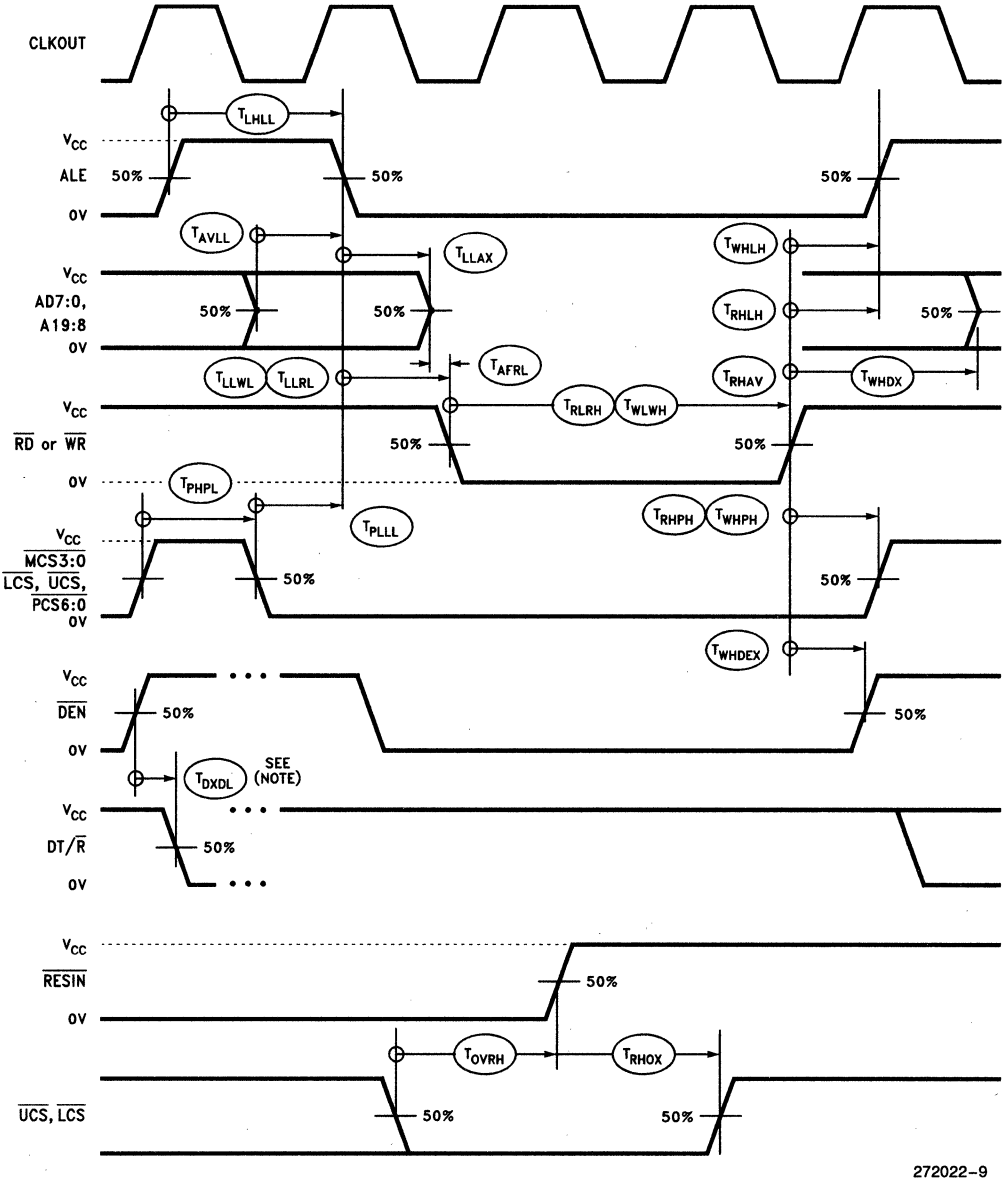
NOTE:
20% V_{CC} < Float < 80% V_{CC}

Figure 6. Output Delay and Float Waveform



NOTE:
RESIN measured to CLKIN, not CLKOUT

Figure 7. Input Setup and Hold



NOTE:
T_{DXDL} for write cycle followed by read cycle

Figure 8. Relative Signal Waveform

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DERATING CURVES

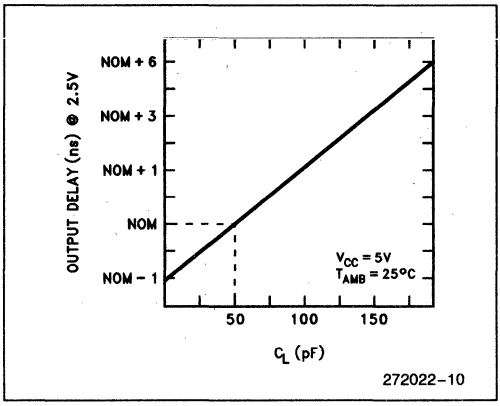


Figure 9. Typical Output Delay Variations Versus Load Capacitance

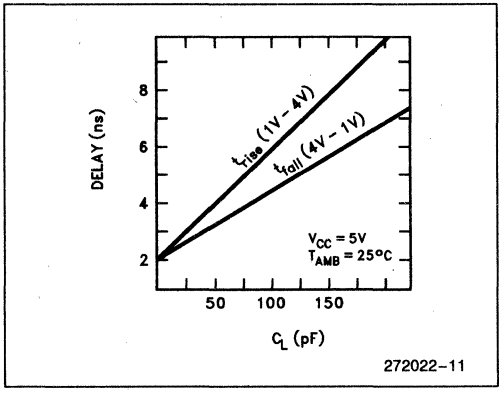


Figure 10. Typical Rise and Fall Variations Versus Load Capacitance

80L188EA EXPRESS

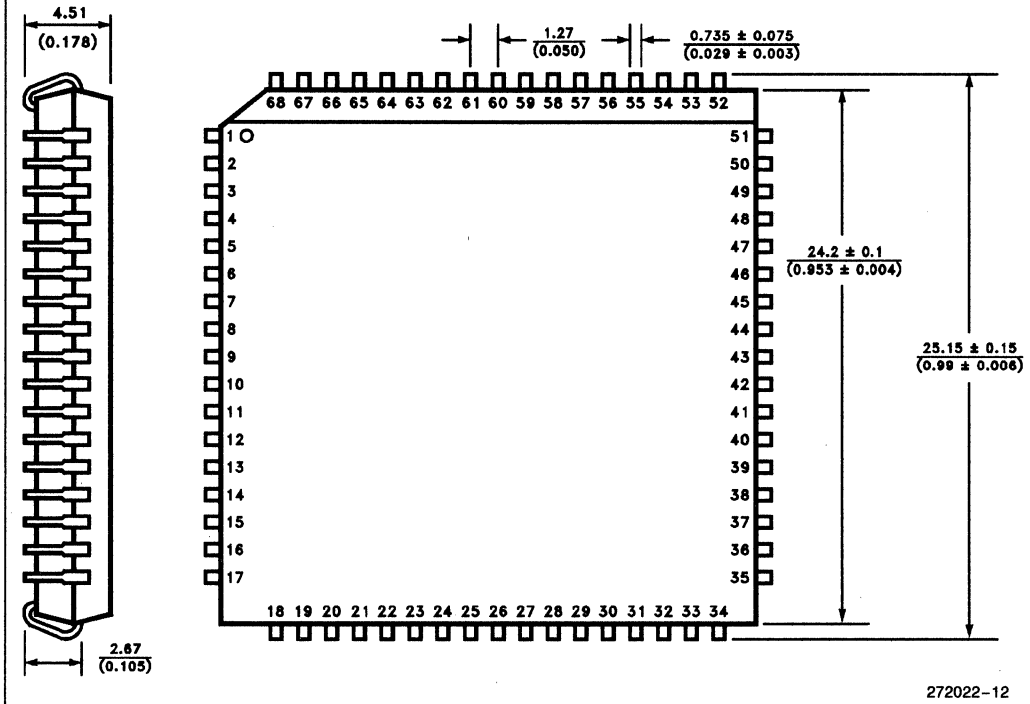
The Intel EXPRESS program offers an extended temperature range as an enhancement to the 80L188EA operational specifications. EXPRESS products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the standard commercial temperature range, operational characteristics are guaranteed over a temperature range corresponding to 0°C to +70°C ambient. With the extended temperature range option, operational characteristics are guaranteed over a temperature range corresponding to −40°C to +85°C ambient.

Package types and EXPRESS versions are identified by a one- or two-letter prefix to the part number. The prefixes are listed in Table 10. All AC and DC specifications are the same for both commercial and EXPRESS parts.

Table 10. Prefix Identification

Prefix	Package Type	Temperature Range
N	PLCC	Commercial
S	QFP (EIAJ)	Commercial
TN	PLCC	Extended
TS	QFP (EIAJ)	Extended



NOTE:
Units are mm/(inches).

Figure 11. PLCC Principal Dimensions

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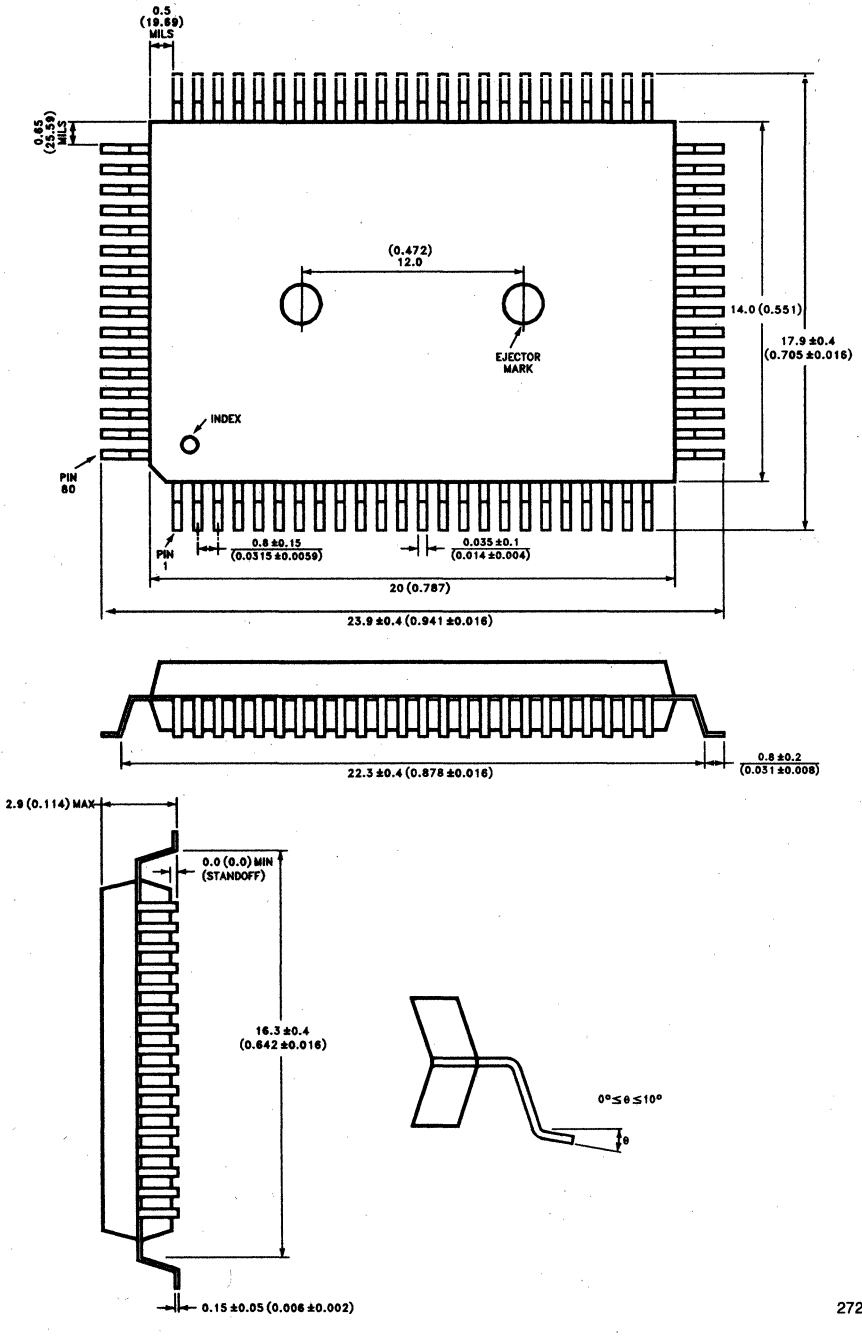


NOTE:
Units are mm (inches) unless specified.

Figure 12. QFP (EIAJ) Principal Dimensions

REVISION HISTORY

Intel 80L188EA devices are marked with a 9-character alphanumeric Intel FPO number underneath the product number. This data sheet (272022-001) is valid for 80L188EA devices with an "A" as the ninth character in the FPO number, as illustrated in Figure 2 for the 68-lead PLCC package and Figure 3 for the 80-lead QFP (EIAJ) package. Such devices may also be identified by reading a value of 01H from the STEPID register.

The following changes were made from revision −001 to −002 of this datasheet.

1. AC and DC specifications for 13 MHz parts were added.

An 80L188EA with a STEPID value of 01H or 02H has the following known errata. A device with a STEPID of 01H or 02H can be visually identified by noting the presence of a "A" or "B" alpha character, respectively, next to the FPO number. The FPO number location is shown in Figures 2 and 3.

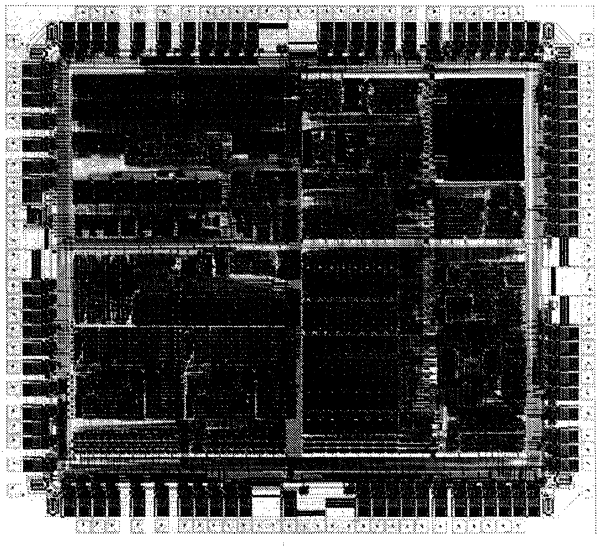
1. An internal condition with the interrupt controller can cause no acknowledge cycle on the INTA1 line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistantly, it is dependent on interrupt timing.

80L188EB-13, -8
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSOR

- 3V Operation, V_{CC} = 2.7V–5.5V
- Full Static Operation
- True CMOS Inputs and Outputs
- −40°C to +85°C Operating Temperature Range
- Low System Cost 8-Bit Interface

- **Integrated Feature Set**
  - Low-Power Static CPU Core
  - Two Independent UARTs each with an Integral Baud Rate Generator
  - Two 8-Bit Multiplexed I/O Ports
  - Programmable Interrupt Controller
  - Three Programmable 16-Bit Timer/Counters
  - Clock Generator
  - Ten Programmable Chip Selects with Integral Wait-State Generator
  - Memory Refresh Control Unit
  - System Level Testing Support (ONCE™ Mode)
- **Direct Addressing Capability to 1 Mbyte Memory and 64 Kbyte I/O**
- **Speed Version Available:**
  - 13 MHz (80L188EB-13)
  - 8 MHz (80L188EB-8)
- **Low-Power Operating Modes:**
  - Idle Mode Freezes CPU Clocks but keeps Peripherals Active
  - Powerdown Mode Freezes All Internal Clocks
- **Complete System Development Support**
  - ASM86 Assembler, PL/M 86, Pascal 86, Fortran 86, C-86, and System Utilities
  - In-Circuit Emulator (ICE™-188EB)
- **Available In:**
  - 80-Pin Quad Flat Pack (TS80L188EB)
  - 84-Pin Plastic Leaded Chip Carrier (TN80L188EB)

The 80L188EB is the 3V version of the 80C188EB embedded processor. By reducing V_{CC}, further power savings can be realized over the standard 80C188EB making the 80L188EB ideal for battery-powered portable applications.



270920-1

May 1992
Order Number: 270920-003

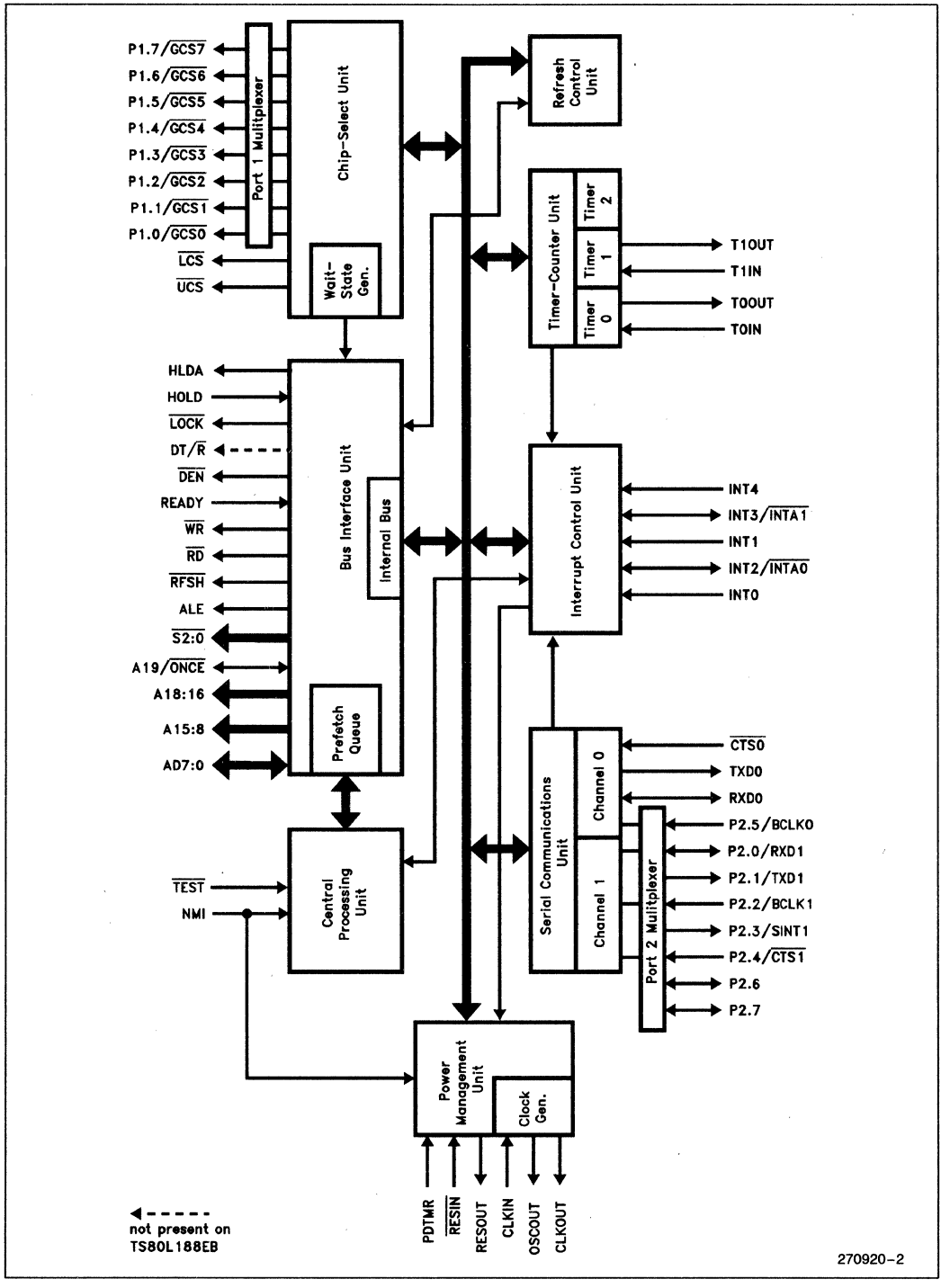


Figure 1. 80L188EB Block Diagram

INTRODUCTION

The 80L188EB is the first product in a new generation of low-power, high-integration microprocessors. It enhances the existing 186 family by offering new features and new operating modes. The 80L188EB is object code compatible with the 80C186/80C188 microprocessors. The 80L188EB has an 8-bit external data bus but still retains a 16-bit internal bus. An 8-bit external bus reduces system cost by requiring that only single byte-wide memories be used.

The feature set of the 80L188EB meets the needs of battery-powered applications. Battery-powered applications benefit from the static CPU core and peripherals. Minimum current consumption is achieved by combining low voltage operation along with the features of the power management unit, thus maximizing battery life. Peripheral design enhancements ensure that non-initialized peripherals consume little current.

Space critical applications benefit from the integration of commonly used system peripherals. Two serial channels are provided for services such as diagnostics, inter-processor communication, modem interface, terminal display interface and many others. A flexible chip select unit simplifies memory and peripheral interfacing. The interrupt unit provides sources for up to 129 external interrupts and will prioritize these interrupts with those generated from the on-chip peripherals. Three general purpose timer/counters and sixteen multiplexed I/O port pins round out the feature set of the 80L188EB.

OVERVIEW

Figure 1 shows a block diagram of the 80L188EB. The Execution Unit (EU) is an enhanced 8088 CPU core that includes: dedicated hardware to speed up effective address calculations, enhance execution speed for multiple-bit shift and rotate instructions and for multiply and divide instructions, string move instructions that operate at full bus bandwidth, ten new instructions and full static operation. The Bus Interface Unit (BIU) is the same as that found on the original 188 family products, except the queue-status mode has been deleted and buffer interface control has been changed to ease system design timings. An independent internal bus is used to allow communication between the BIU and internal peripherals.

PACKAGE INFORMATION

This section describes the pins, pinouts, and thermal characteristics for the 80L188EB in the Plastic Leaded Chip Carrier (PLCC) package and Quad Flat Pack (QFP) package. For complete package specifications and information, see the Intel Packaging handbook (Order Number: 240800).

80L188EB PINOUT

Tables 1 and 2 list the 80L188EB pin names with package location for the 84-pin Plastic Leaded Chip Carrier (PLCC) component. Figure 2 depicts the complete 80L188EB pinout (PLCC package) as viewed from the top side of the component (i.e., contacts facing down).

Tables 3 and 4 list the 80L188EB pin names with package location for the 80-pin Quad Flat Pack (QFP) component. Figure 3 depicts the complete 80L188EB (QFP package) as viewed from the top side of the component (i.e., contacts facing down).

Table 1. PLCC Pin Names with Package Location

Address/Data Bus	
Name	**Location**
AD0	61
AD1	66
AD2	68
AD3	70
AD4	72
AD5	74
AD6	76
AD7	78
A8	62
A9	67
A10	69
A11	71
A12	73
A13	75
A14	77
A15	79
A16	80
A17	81
A18	82
A19/$\overline{\text{ONCE}}$	83

Bus Control	
Name	**Location**
ALE	6
$\overline{\text{RFSH}}$	7
$\overline{\text{S0}}$	10
$\overline{\text{S1}}$	9
$\overline{\text{S2}}$	8
$\overline{\text{RD}}$	4
$\overline{\text{WR}}$	5
READY	18
$\overline{\text{DEN}}$	11
DT/$\overline{\text{R}}$	16
$\overline{\text{LOCK}}$	15
HOLD	13
HLDA	12

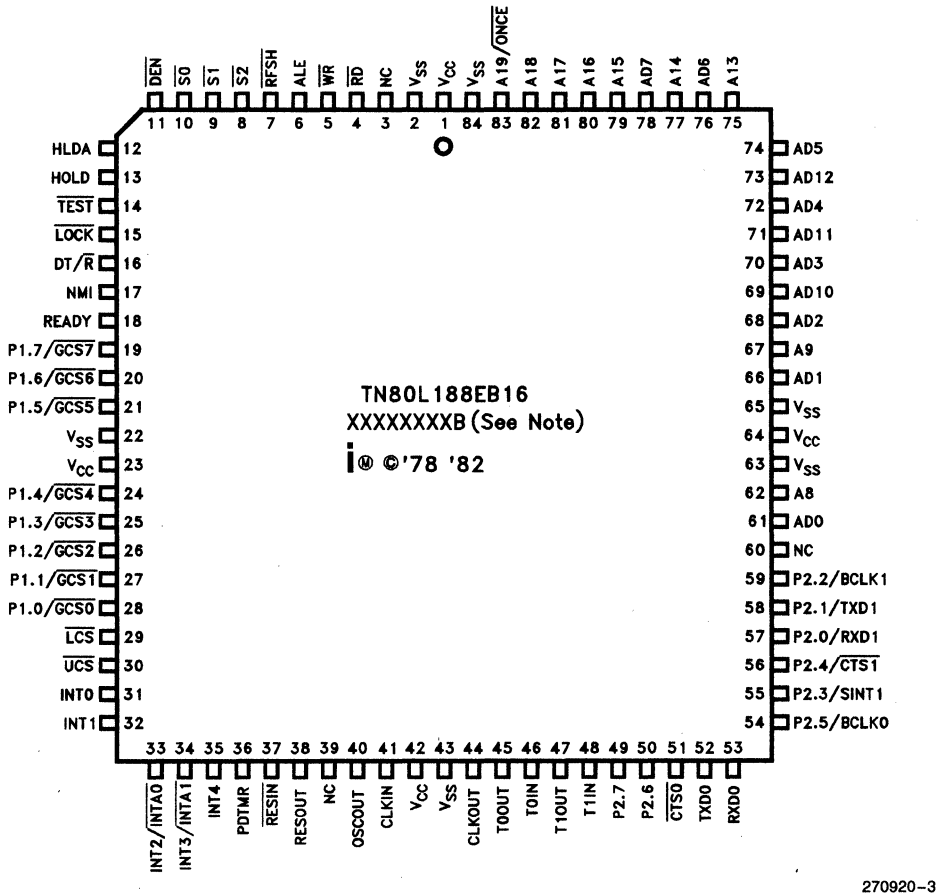
Power	
Name	**Location**
V_{SS}	2, 22, 43, 63, 65, 84
V_{CC}	1, 23, 42, 64

Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	37
RESOUT	38
CLKIN	41
OSCOUT	40
CLKOUT	44
$\overline{\text{TEST}}$	14
NC	60
NC	39
NC	3
PDTMR	36
NMI	17
INT0	31
INT1	32
INT2/$\overline{\text{INTA0}}$	33
INT3/$\overline{\text{INTA1}}$	34
INT4	35

I/O	
Name	**Location**
$\overline{\text{UCS}}$	30
$\overline{\text{LCS}}$	29
P1.0/$\overline{\text{GCS0}}$	28
P1.1/$\overline{\text{GCS1}}$	27
P1.2/$\overline{\text{GCS2}}$	26
P1.3/$\overline{\text{GCS3}}$	25
P1.4/$\overline{\text{GCS4}}$	24
P1.5/$\overline{\text{GCS5}}$	21
P1.6/$\overline{\text{GCS6}}$	20
P1.7/$\overline{\text{GCS7}}$	19
T0OUT	45
T0IN	46
T1OUT	47
T1IN	48
RXD0	53
TXD0	52
P2.5/BCLK0	54
$\overline{\text{CTS0}}$	51
P2.0/RXD1	57
P2.1/TXD1	58
P2.2/BCLK1	59
P2.3/SINT1	55
P2.4/$\overline{\text{CTS1}}$	56
P2.6	50
P2.7	49

Table 2. PLCC Package Locations with Pin Name

Location	Name	Location	Name	Location	Name	Location	Name
1	V_{CC}	22	V_{SS}	43	V_{SS}	64	V_{CC}
2	V_{SS}	23	V_{CC}	44	CLKOUT	65	V_{SS}
3	NC	24	P1.4/$\overline{GCS4}$	45	T0OUT	66	AD1
4	$\overline{RD}$	25	P1.3/$\overline{GCS3}$	46	T0IN	67	A9
5	$\overline{WR}$	26	P1.2/$\overline{GCS2}$	47	T1OUT	68	AD2
6	ALE	27	P1.1/$\overline{GCS1}$	48	T1IN	69	A10
7	$\overline{RFSH}$	28	P1.0/$\overline{GCS0}$	49	P2.7	70	AD3
8	$\overline{S2}$	29	$\overline{LCS}$	50	P2.6	71	A11
9	$\overline{S1}$	30	$\overline{UCS}$	51	$\overline{CTS0}$	72	AD4
10	$\overline{S0}$	31	INT0	52	TXD0	73	A12
11	$\overline{DEN}$	32	INT1	53	RXD0	74	AD5
12	HLDA	33	INT2/$\overline{INTA0}$	54	P2.5/BCLK0	75	A13
13	HOLD	34	INT3/$\overline{INTA1}$	55	P2.3/SINT1	76	AD6
14	$\overline{TEST}$	35	INT4	56	P2.4/$\overline{CTS1}$	77	A14
15	$\overline{LOCK}$	36	PDTMR	57	P2.0/RXD1	78	AD7
16	DT/$\overline{R}$	37	$\overline{RESIN}$	58	P2.1/TXD1	79	A15
17	NMI	38	RESOUT	59	P2.2/BCLK1	80	A16
18	READY	39	NC	60	NC	81	A17
19	P1.7/$\overline{GCS7}$	40	OSCOUT	61	AD0	82	A18
20	P1.6/$\overline{GCS6}$	41	CLKIN	62	A8	83	A19/$\overline{ONCE}$
21	P1.5/$\overline{GCS5}$	42	V_{CC}	63	V_{SS}	84	V_{SS}



NOTE:
This is the FPO number location (indicated by the X's).

Figure 2. 84-Pin Plastic Leaded Chip Carrier Pinout Diagram

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Table 3. QFP Pin Name with Package Location

Address/Data Bus	
Name	**Location**
AD0	10
AD1	15
AD2	17
AD3	19
AD4	21
AD5	23
AD6	25
AD7	27
A8	11
A9	16
A10	18
A11	20
A12	22
A13	24
A14	26
A15	28
A16	29
A17	30
A18	31
A19/$\overline{\text{ONCE}}$	32

Bus Control	
Name	**Location**
ALE	38
$\overline{\text{RFSH}}$	39
$\overline{\text{S0}}$	42
$\overline{\text{S1}}$	41
$\overline{\text{S2}}$	40
$\overline{\text{RD}}$	36
$\overline{\text{WR}}$	37
READY	49
$\overline{\text{DEN}}$	43
$\overline{\text{LOCK}}$	47
HOLD	45
HLDA	44

Processor Control	
Name	**Location**
$\overline{\text{RESIN}}$	68
RESOUT	69
CLKIN	71
OSCOUT	70
CLKOUT	74
$\overline{\text{TEST}}$	46
PDTMR	67
NMI	48
INT0	62
INT1	63
INT2/$\overline{\text{INTA0}}$	64
INT3/$\overline{\text{INTA1}}$	65
INT4	66

Power	
Name	**Location**
V_{CC}	13, 34, 54, 72
V_{SS}	12, 14, 33, 35, 53, 73

I/O	
Name	**Location**
$\overline{\text{UCS}}$	61
$\overline{\text{LCS}}$	60
P1.0/$\overline{\text{GCS0}}$	59
P1.1/$\overline{\text{GCS1}}$	58
P1.2/$\overline{\text{GCS2}}$	57
P1.3/$\overline{\text{GCS3}}$	56
P1.4/$\overline{\text{GCS4}}$	55
P1.5/$\overline{\text{GCS5}}$	52
P1.6/$\overline{\text{GCS6}}$	51
P1.7/$\overline{\text{GCS7}}$	50
T0OUT	75
T0IN	76
T1OUT	77
T1IN	78
RXD0	3
TXD0	2
P2.5/BCLK0	4
$\overline{\text{CTS0}}$	1
P2.0/RXD1	7
P2.1/TXD1	8
P2.2/BCLK1	9
P2.3/SINT1	5
P2.4/$\overline{\text{CTS1}}$	6
P2.6	80
P2.7	79

Table 4. QFP Package Location with Pin Names

Location	Name	Location	Name	Location	Name	Location	Name
1	$\overline{CTS0}$	21	AD4	41	$\overline{S1}$	61	$\overline{UCS}$
2	TXD0	22	A12	42	$\overline{S0}$	62	INT0
3	RXD0	23	AD5	43	$\overline{DEN}$	63	INT1
4	P2.5/BCLK0	24	A13	44	HLDA	64	INT2/$\overline{INTA0}$
5	P2.3/SINT1	25	AD6	45	HOLD	65	INT3/$\overline{INTA1}$
6	P2.4/$\overline{CTS1}$	26	A14	46	$\overline{TEST}$	66	INT4
7	P2.0/RXD1	27	AD7	47	$\overline{LOCK}$	67	PDTMR
8	P2.1/TXD1	28	A15	48	NMI	68	$\overline{RESIN}$
9	P2.2/BCLK1	29	A16	49	READY	69	RESOUT
10	AD0	30	A17	50	P1.7/$\overline{GCS7}$	70	OSCOUT
11	A8	31	A18	51	P1.6/$\overline{GCS6}$	71	CLKIN
12	V_{SS}	32	A19/$\overline{ONCE}$	52	P1.5/$\overline{GCS5}$	72	V_{CC}
13	V_{CC}	33	V_{SS}	53	V_{SS}	73	V_{SS}
14	V_{SS}	34	V_{CC}	54	V_{CC}	74	CLKOUT
15	AD1	35	V_{SS}	55	P1.4/$\overline{GCS4}$	75	T0OUT
16	A9	36	$\overline{RD}$	56	P1.3/$\overline{GCS3}$	76	T0IN
17	AD2	37	$\overline{WR}$	57	P1.2/$\overline{GCS2}$	77	T1OUT
18	A10	38	ALE	58	P1.1/$\overline{GCS1}$	78	T1IN
19	AD3	39	$\overline{RFSH}$	59	P1.0/$\overline{GCS0}$	79	P2.7
20	A11	40	$\overline{S2}$	60	$\overline{LCS}$	80	P2.6

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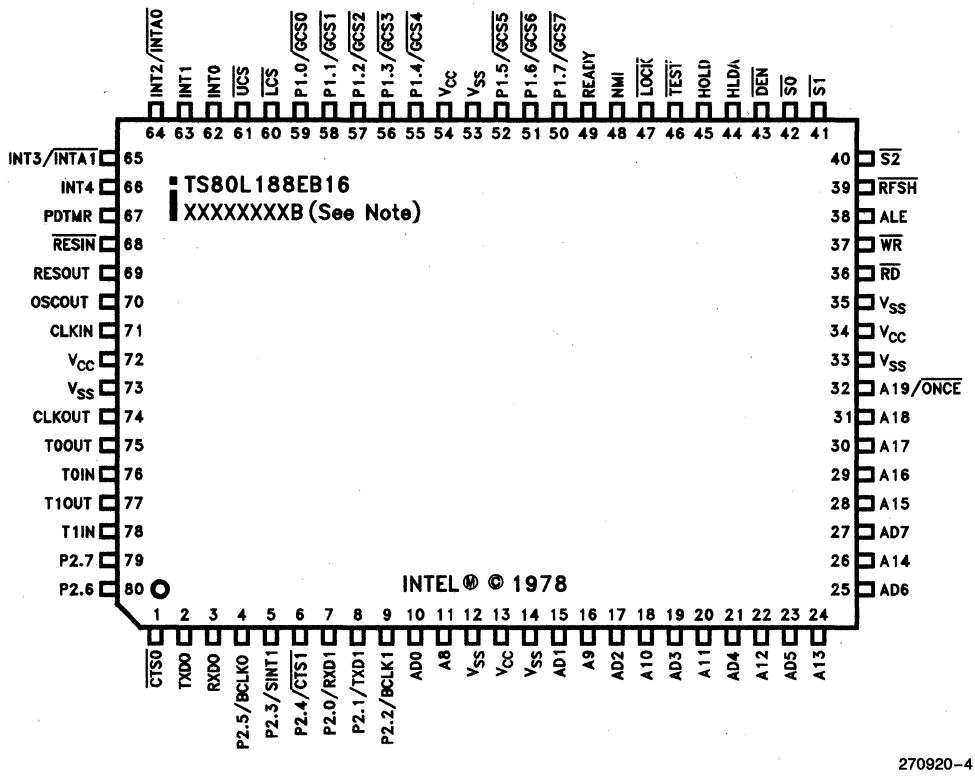

NOTE:
This is the FPO number location (indicated by the X's).

Figure 3. Quad Flat Pack Pinout Diagram

PACKAGE THERMAL SPECIFICATIONS

The 80L188EB is specified for operation when T_C (the case temperature) is within the range of −40°C to +100°C (PLCC package) or −40°C to +114°C (QFP package). T_C may be measured in any environment to determine whether the 80L188EB is within the specified operating range. The case temperature must be measured at the center of the top surface.

T_A (the ambient temperature) can be calculated from θ_{CA} (thermal resistance from the case to ambient) with the following equation:

$$T_A = T_C - P^*\theta_{CA}$$

Typical values for θ_{CA} at various airflows are given in Table 5 for the 84-pin Plastic Leaded Chip Carrier (PLCC) package.

Table 6 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies. P (the maximum power consumption, specified in watts) is calculated by using the maximum ICC as tabulated in the DC specifications and V_{CC} of 5V.

Table 5. Thermal Resistance (θ_{CA}) at Various Airflows (in °C/Watt)

	Airflow Linear ft/min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
θ_{CA} (PLCC)	30	24	21	19	17	16.5
θ_{CA} (QFP)	58	47	43	40	38	36

Table 6. Maximum T_A at Various Airflows (in °C)

		Airflow Linear ft/min (m/sec)					
	T_F (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A (PLCC)	16	91.5	93.5	94	94.5	95.5	95.5
T_A (QFP)	16	98	101	102	103	103.5	104

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	−65°C to +150°C
Case Temp Under Bias	−65°C to +120°C
Supply Voltage wrt V_{SS}	−0.5V to +6.5V
Voltage on other Pins with respect to V_{SS}	−0.5V to V_{CC} +0.5V

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	5.5	V
T_F	Input Clock Frequency			
	80L188EB-13	0	26	MHz
	80L188EB-8	0	16	MHz
T_C	Case Temperature Under Bias			
	N80L188EB-X (PLCC)	−40	+100	°C
	S80L188EB-X (QFP)	−40	+114	°C

RECOMMENDED CONNECTIONS

Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every 80L188EB-based circuit board should include separate power (V_{CC}) and ground (V_{SS}) planes. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "NC" must not be connected in the system. Liberal decoupling capacitance should be placed near the 80L188EB. The processor can cause transient power surges when its output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by placing the decoupling capacitors as close as possible to the 80L188EB V_{CC} and V_{SS} package pins.

Always connect any unused input to an appropriate signal level. In particular, unused interrupt inputs (INT0:4) should be connected to V_{CC} through a pull-up resistor (in the range of 50 KΩ). **Leave any unused output pin or any NC pin unconnected.**

DC SPECIFICATIONS

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	−0.5	0.3*V_{CC}	V	
V_{IH}	Input High Voltage	0.7*V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6 mA (Min) (Note 1)
V_{OH}	Output High Voltage	V_{CC} − 0.5		V	I_{OH} = −1 mA (Min) (Note 1)
V_{HYR}	Input Hysterisis on $\overline{RESIN}$	0.50		V	
I_{LI1}	Input Leakage Current for pins: AD15:0, READY, HOLD, $\overline{RESIN}$, CLKIN, $\overline{TEST}$, NMI, INT4:0, T0IN, T1IN, RXD0, $\overline{BCLK0}$, $\overline{CTS0}$, RXD1, $\overline{BCLK1}$, $\overline{CTS1}$, Sint1, P2.6, P2.7		±15	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LI2}	Input Leakage Current for pins: A19/$\overline{ONCE}$, A18:16, $\overline{LOCK}$	−0.275	−0.5	μA	V_{IN} = 0.7 V_{CC} (Note 2)
I_{LO}	Output Leakage Current		±15	μA	0.45 ≤ V_{OUT} ≤ V_{CC} (Note 3)
I_{CC5}	Supply Current (RESET, 5.5V) 80L188EB-13 80L188EB-8		 70 45	 mA mA	 (Note 4) (Note 4)
I_{CC3}	Supply Current (RESET, 2.7V) 80L188EB-13 80L188EB-8		 36 22	 mA mA	 (Note 4) (Note 4)
I_{ID5}	Supply Current Idle (5.5V) 80L188EB-13 80L188EB-8		 48 31	 mA mA	 (Note 5) (Note 5)
I_{ID3}	Supply Current Idle (2.7V) 80L188EB-13 80L188EB-8		 24 15	 mA mA	 (Note 5) (Note 5)
I_{PD5}	Supply Current Powerdown (5.5V) 80L188EB-13 80L188EB-8		 100 100	 μA μA	 (Note 6) (Note 6)
I_{PD3}	Supply Current Powerdown (2.7V) 80L188EB-13 80L188EB-8		 30 30	 μA μA	 (Note 6) (Note 6)
C_{IN}	Input Pin Capacitance	0	15	pF	T_F = 1 MHz
C_{OUT}	Output Pin Capacitance	0	15	pF	T_F = 1 MHz (Note 7)

NOTES:
1. I_{OL} and I_{OH} measured at V_{CC} = 2.7V.
2. These pins have an internal pull-up device that is active while $\overline{RESIN}$ is low and ONCE Mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory test mode.
3. Tested by outputs being floated by invoking ONCE Mode or by asserting HOLD.
4. Measured with the device in RESET and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or V_{SS}.
5. Measured with the device in HALT (IDLE Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or V_{SS}.
6. Measured with the device in HALT (Powerdown Mode active) and at worst case frequency, V_{CC}, and temperature with **ALL** outputs loaded as specified in AC Test Conditions, and all floating outputs driven to V_{CC} or V_{SS}.
7. Output Capacitance is the capacitive load of a floating output pin.

I_{CC} VERSUS FREQUENCY AND VOLTAGE

The current (I_{CC}) consumption of the 80L188EB is essentially composed of two components: I_{PD} and I_{CCS}.

I_{PD} is the **quiescent** current that represents internal device leakage, and is measured with all inputs or floating outputs at GND or V_{CC} (no clock applied to the device). I_{PD} is equal to the Powerdown current and is typically less than 50 μA.

I_{CCS} is the **switching** current used to charge and discharge parasitic device capacitance when changing logic levels. Since I_{CCS} is typically much greater than I_{PD}, I_{PD} can often be ignored when calculating I_{CC}.

I_{CCS} is related to the voltage and frequency at which the device is operating. It is given by the formula:

$$\text{Power} = V \times I = V^2 \times C_{DEV} \times f$$

$$\therefore I = I_{CC} = I_{CCS} = V \times C_{DEV} \times f$$

Where: V = Device operating voltage (V_{CC})

C_{DEV} = Device capacitance

f = Device operating frequency

$I_{CCS} = I_{CC}$ = Device current

Measuring C_{DEV} on a device like the 80C188EB would be difficult. Instead, C_{DEV} is calculated using the above formula by measuring I_{CC} at a known V_{CC} and frequency (see Table 7). Using this C_{DEV} value, I_{CC} can be calculated at any voltage and frequency within the specified operating range.

EXAMPLE: Calculate the typical I_{CC} when operating at 8 MHz, 3V.

$$I_{CC} = I_{CCS} = 3 \times 0.583 \times 8 \approx 14 \text{ mA}$$

PDTMR PIN DELAY CALCULATION

The PDTMR pin provides a delay between the assertion of NMI and the enabling of the internal clocks when exiting Powerdown. A delay is required only when using the on-chip oscillator to allow the crystal or resonator circuit time to stabilize.

NOTE:
The PDTMR pin function does not apply when $\overline{RESIN}$ is asserted (i.e., a device reset during Powerdown is similar to a cold reset and $\overline{RESIN}$ must remain active until after the oscillator has stabilized).

To calculate the value of capacitor required to provide a desired delay, use the equation:

$$440 \times t = C_{PD} \quad (5V, 25°C)$$

Where: t = desired delay in **seconds**

C_{PD} = capacitive load on PDTMR in **microfarads**

EXAMPLE: To get a delay of 300 μs, a capacitor value of $C_{PD} = 440 \times (300 \times 10^{-6}) = 0.132$ μF is required. Round up to standard (available) capacitive values.

NOTE:
The above equation applies to delay times greater than 10 μs and will compute the **TYPICAL** capacitance needed to achieve the desired delay. A delay variance of +50% or −25% can occur due to temperature, voltage, and device process extremes. In general, higher V_{CC} and/or lower temperature will decrease delay time, while lower V_{CC} and/or higher temperature will increase delay time.

Table 7. Device Capacitance (C_{DEV}) Values

Parameter	Typ	Max	Units	Notes
C_{DEV} (Device in Reset)	0.583	1.02	mA/V*MHz	1, 2
C_{DEV} (Device in Idle)	0.408	0.682	mA/V*MHz	1, 2

1. Max C_{DEV} is calculated at −40°C, all floating outputs driven to V_{CC} or GND, and all outputs loaded to 50 pF (including CLKOUT and OSCOUT).
2. Typical C_{DEV} is calculated at 25°C with all outputs loaded to 50 pF except CLKOUT and OSCOUT, which are not loaded.

AC SPECIFICATIONS

AC Characteristics—(80L188EB-8)

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	16	MHz	1
T_C	CLKIN Period	62.5	∞	ns	1
T_{CH}	CLKIN High Time	15	∞	ns	1, 2
T_{CL}	CLKIN Low Time	15	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	50	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	15	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	15	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{RFSH}$, $\overline{LOCK}$, A19:16	3	30	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$	3	35	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	30	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, AD7:0, $\overline{NCS}$, $\overline{INTA1:0}$, $\overline{S2:0}$, A15:8	3	35	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, AD7:0, A15:8	0	35	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, T1:OIN, P2.6, P2.7 READY, $\overline{CTS1:0}$, BCLK1:0	25		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, T1:OIN, BCLK1:0 READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD7:0, READY	25		ns	1, 10
T_{CLIH}	READY, AD7:0	3		ns	1, 10
T_{CLIS}	HOLD	25		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 10 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 11 for rise and fall times outside 50 pF.
6. See Figure 11 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A19:8 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L188EB operation.

AC SPECIFICATIONS

AC Characteristics—(80L188EB-13)

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK					
T_F	CLKIN Frequency	0	26	MHz	1
T_C	CLKIN Period	38.5	∞	ns	1
T_{CH}	CLKIN High Time	15	∞	ns	1, 2
T_{CL}	CLKIN Low Time	15	∞	ns	1, 2
T_{CR}	CLKIN Rise Time	1	8	ns	1, 3
T_{CF}	CLKIN Fall Time	1	8	ns	1, 3
OUTPUT CLOCK					
T_{CD}	CLKIN to CLKOUT Delay	0	40	ns	1, 4
T	CLKOUT Period		$2*T_C$	ns	1
T_{PH}	CLKOUT High Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PL}	CLKOUT Low Time	(T/2) − 5	(T/2) + 5	ns	1
T_{PR}	CLKOUT Rise Time	1	10	ns	1, 5
T_{PF}	CLKOUT Fall Time	1	10	ns	1, 5
OUTPUT DELAYS					
T_{CHOV1}	ALE, $\overline{S2:0}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{RFSH}$, $\overline{LOCK}$, A19:16	3	25	ns	1, 4, 6, 7
T_{CHOV2}	$\overline{GCS0:7}$, $\overline{LCS}$, $\overline{UCS}$, $\overline{RD}$, $\overline{WR}$	3	30	ns	1, 4, 6, 8
T_{CLOV1}	$\overline{RFSH}$, $\overline{DEN}$, $\overline{LOCK}$, RESOUT, HLDA, T0OUT, T1OUT, A19:16	3	25	ns	1, 4, 6
T_{CLOV2}	$\overline{RD}$, $\overline{WR}$, $\overline{GCS7:0}$, $\overline{LCS}$, $\overline{UCS}$, A15:8, AD7:0, $\overline{NCS}$, $\overline{INTA1:0}$	3	30	ns	1, 4, 6
T_{CLOV3}	$\overline{S2:0}$	3	35	ns	1, 4, 6
T_{CHOF}	$\overline{RD}$, $\overline{WR}$, $\overline{RFSH}$, DT/$\overline{R}$, $\overline{LOCK}$, $\overline{S2:0}$, A19:16	0	30	ns	1
T_{CLOF}	$\overline{DEN}$, AD7:0, A15:8	0	35	ns	1
SYNCHRONOUS INPUTS					
T_{CHIS}	$\overline{TEST}$, NMI, INT4:0, T1:OIN, P2.6, P2.7 READY, $\overline{CTS1:0}$, BCLK1:0	20		ns	1, 9
T_{CHIH}	$\overline{TEST}$, NMI, INT4:0, T1:OIN, BCLK1:0 READY, $\overline{CTS1:0}$	3		ns	1, 9
T_{CLIS}	AD7:0, READY	20		ns	1, 10
T_{CLIH}	READY, AD7:0	3		ns	1, 10
T_{CLIS}	HOLD	20		ns	1, 9
T_{CLIH}	HOLD	3		ns	1, 9

NOTES:
1. See **AC Timing Waveforms**, for waveforms and definition.
2. Measure at V_{IH} for high time, V_{IL} for low time.
3. Only required to guarantee I_{CC}. Maximum limits are bounded by T_C, T_{CH} and T_{CL}.
4. Specified for a 50 pF load, see Figure 10 for capacitive derating information.
5. Specified for a 50 pF load, see Figure 11 for rise and fall times outside 50 pF.
6. See Figure 11 for rise and fall times.
7. T_{CHOV1} applies to $\overline{RFSH}$, $\overline{LOCK}$ and A19:8 only after a HOLD release.
8. T_{CHOV2} applies to $\overline{RD}$ and $\overline{WR}$ only after a HOLD release.
9. Setup and Hold are required to guarantee recognition.
10. Setup and Hold are required for proper 80L188EB operation.

AC SPECIFICATIONS (Continued)

Relative Timings (80L188EB-13, -8)

Symbol	Parameter	Min	Max	Units	Notes
RELATIVE TIMINGS					
T_{LHLL}	ALE Rising to ALE Falling	T − 15		ns	
T_{AVLL}	Address Valid to ALE Falling	½T − 10		ns	
T_{PLLL}	Chip Selects Valid to ALE Falling	½T − 10		ns	1
T_{LLAX}	Address Hold from ALE Falling	½T − 10		ns	
T_{LLWL}	ALE Falling to $\overline{WR}$ Falling	½T − 15		ns	1
T_{LLRL}	ALE Falling to $\overline{RD}$ Falling	½T − 15		ns	1
T_{WHLH}	$\overline{WR}$ Rising to ALE Rising	½T − 10		ns	1
T_{AFRL}	Address Float to $\overline{RD}$ Falling	0		ns	
T_{RLRH}	$\overline{RD}$ Falling to $\overline{RD}$ Rising	(2*T) − 5		ns	2
T_{WLWH}	$\overline{WR}$ Falling to $\overline{WR}$ Rising	(2*T) − 5		ns	2
T_{RHAX}	$\overline{RD}$ Rising to Address Active	T − 15		ns	
T_{WHDX}	Output Data Hold after $\overline{WR}$ Rising	T − 15		ns	
T_{WHPH}	$\overline{WR}$ Rising to Chip Select Rising	½T − 10		ns	1
T_{RHPH}	$\overline{RD}$ Rising to Chip Select Rising	½T − 10		ns	1
T_{PHPL}	$\overline{CS}$ Active to $\overline{CS}$ Inactive	½T − 10		ns	1
T_{OVRH}	$\overline{ONCE}$ Active to $\overline{RESIN}$ Rising	1T		ns	
T_{RHOX}	$\overline{ONCE}$ Hold from $\overline{RESIN}$ Rising	1T		ns	

NOTES:
1. Assumes equal loading on both pins.
2. Can be extended using wait states.

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AC SPECIFICATIONS (Continued)

Serial Port Mode 0 Timings (80L188EB-13, -8)

Symbol	Parameter	Min	Max	Units	Notes
T_{XLXL}	TXD Clock Period	T(N + 1)		ns	1, 2
T_{XLXH}	TXD Clock Low to Clock High (N > 1)	2T − 35	2T + 35	ns	1, 2
T_{XLXH}	TXD Clock Low to Clock High (N = 1)	T − 35	T + 35	ns	1, 2
T_{XHXL}	TXD Clock High to Clock Low (N > 1)	T(N − 1) − 35	T(N − 1) + 35	ns	2
T_{XHXL}	TXD Clock High to Clock Low (N = 1)	T − 35	T + 35	ns	2
T_{QVXH}	RXD Output Data Setup to TXD Clock High (n > 1)	T(N − 1) − 35		ns	1, 2
T_{QVXH}	RXD Output Data Setup to TXD Clock High (n = 1)	T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (n > 1)	2T − 35		ns	1
T_{XHQX}	RXD Output Data Hold after TXD Clock High (n = 1)	T − 35		ns	1
T_{XHQZ}	RXD Output Data Float after Last TXD Clock High		T + 20	ns	1
T_{DVXH}	RXD Input Data Setup to TXD Clock High	T + 20		ns	1
T_{XHDX}	RXD Input Data Hold after TXD Clock High	0		ns	1

NOTES:
1. See Figure 9 for waveforms.
2. n is the value of the BxCMP register ignoring the iCLK bit (i.e., ICLK = 0).

AC TEST CONDITIONS

The AC specifications are tested with the 50 pF load shown in Figure 4. See the Derating Curves section to see how timings vary with load capacitance.

Specifications are measured at the $V_{CC}/2$ crossing point, unless otherwise specified. See AC Timing Waveforms, for AC specification definitions, test pins, and illustrations.

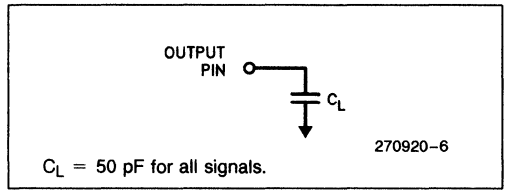

Figure 4. AC Test Load

AC TIMING WAVEFORMS

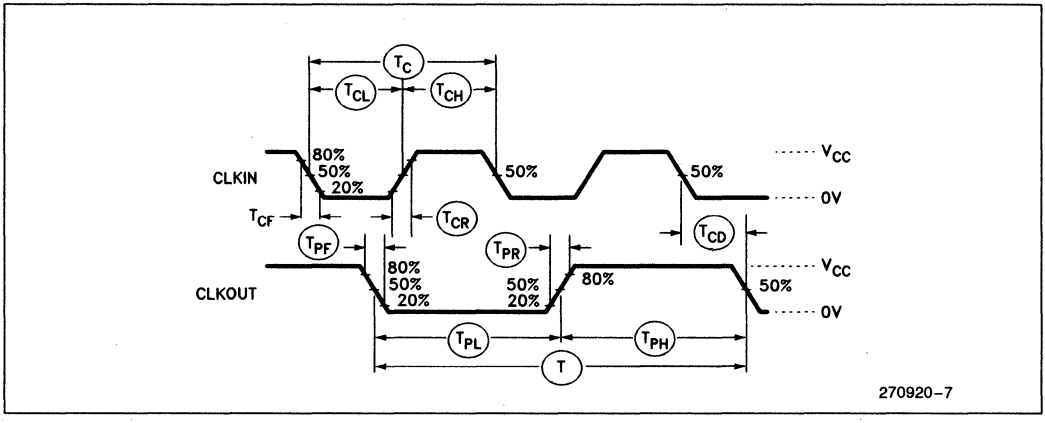

Figure 5. Input and Output Clock Waveform

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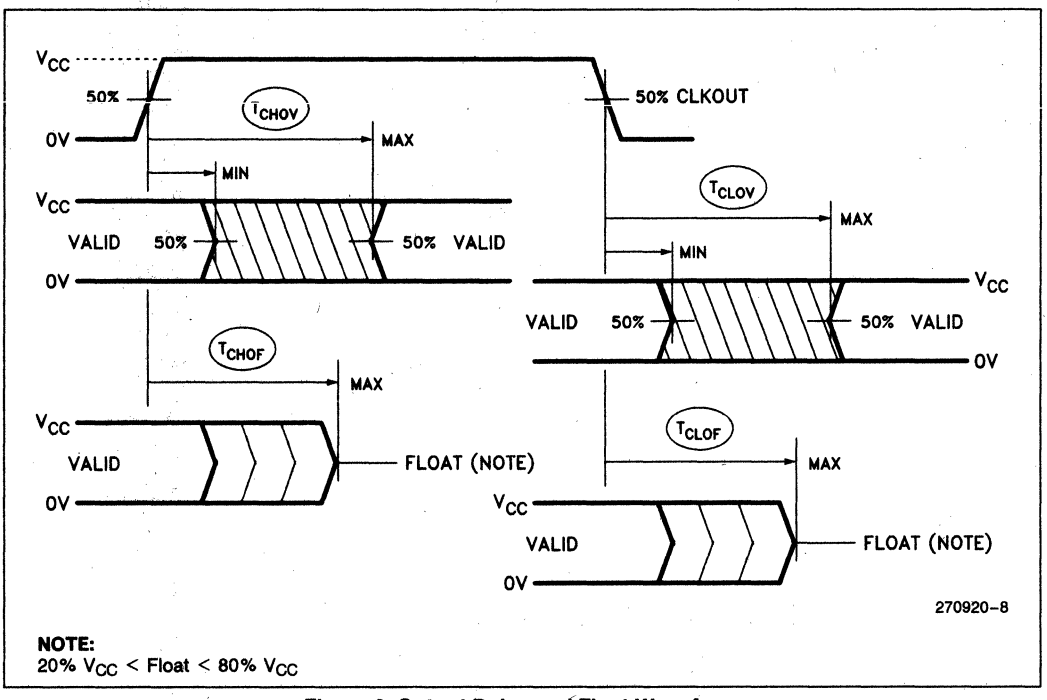

NOTE:
20% V_{CC} < Float < 80% V_{CC}

Figure 6. Output Delay and Float Waveform

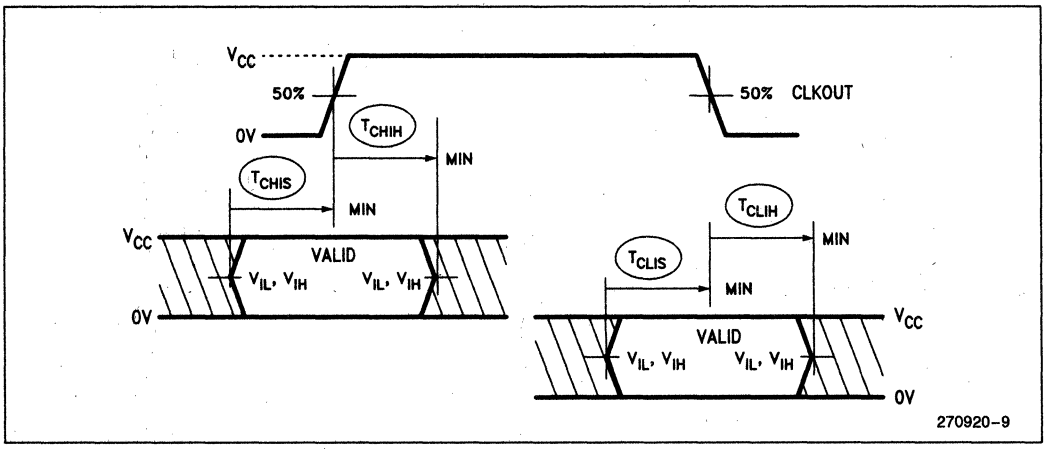

Figure 7. Input Setup and Hold

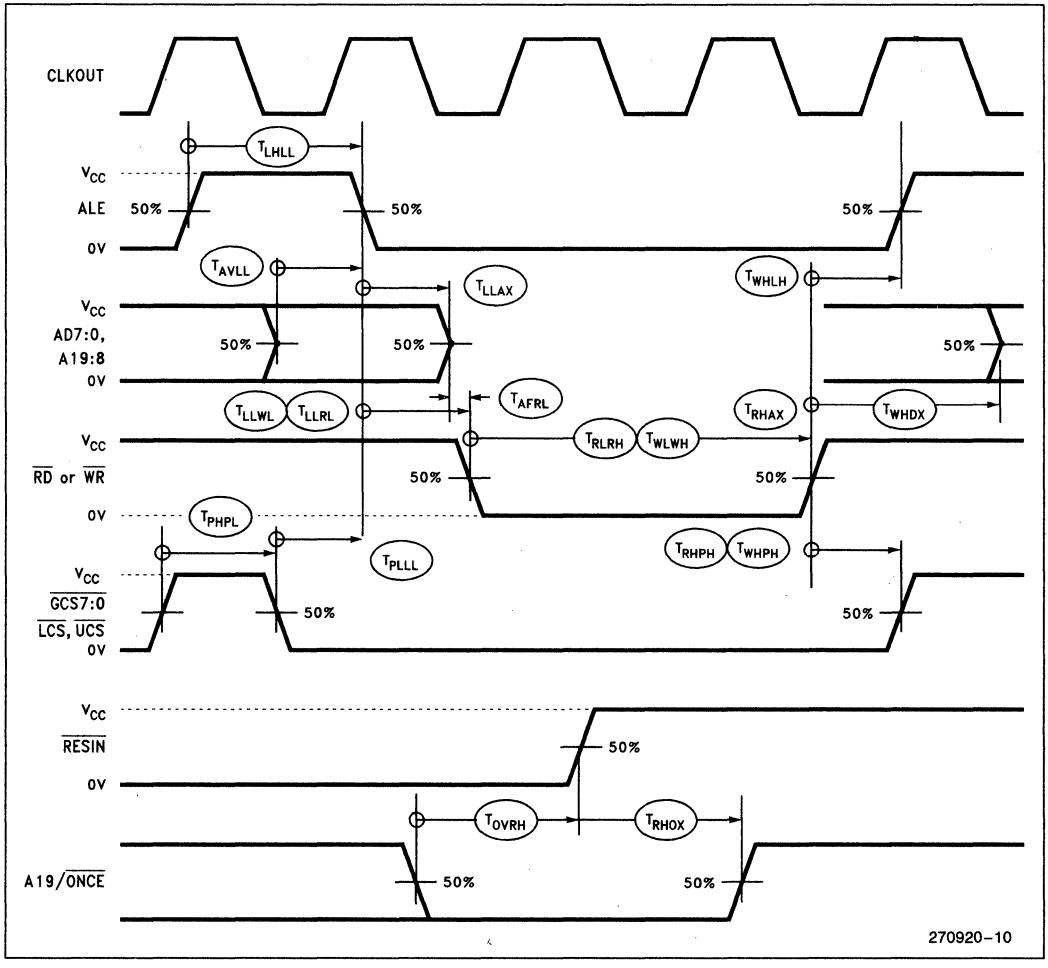

Figure 8. Relative Signal Waveform

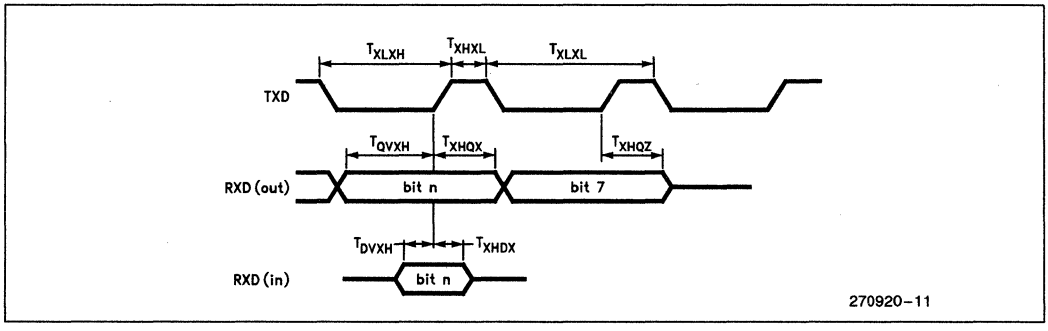

Figure 9. Serial Port Mode 0 Waveform

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DERATING CURVES

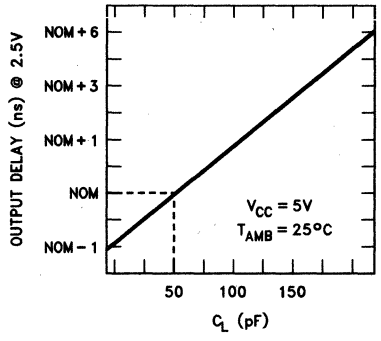

Figure 10. Typical Output Delay Variations vs Load Capacitance

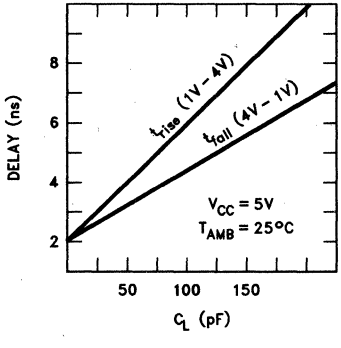

Figure 11. Typical Rise and Fall Variations vs Load Capacitance

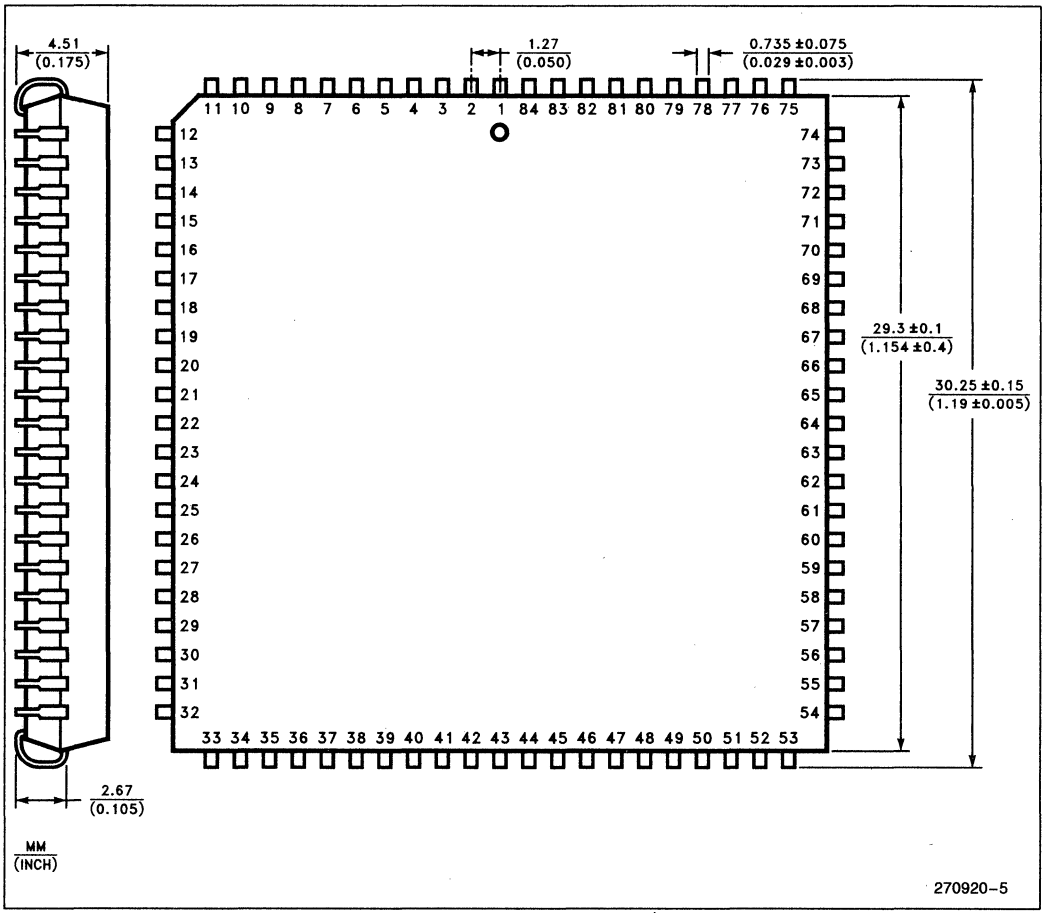

Figure 12. PLCC Principal Dimensions

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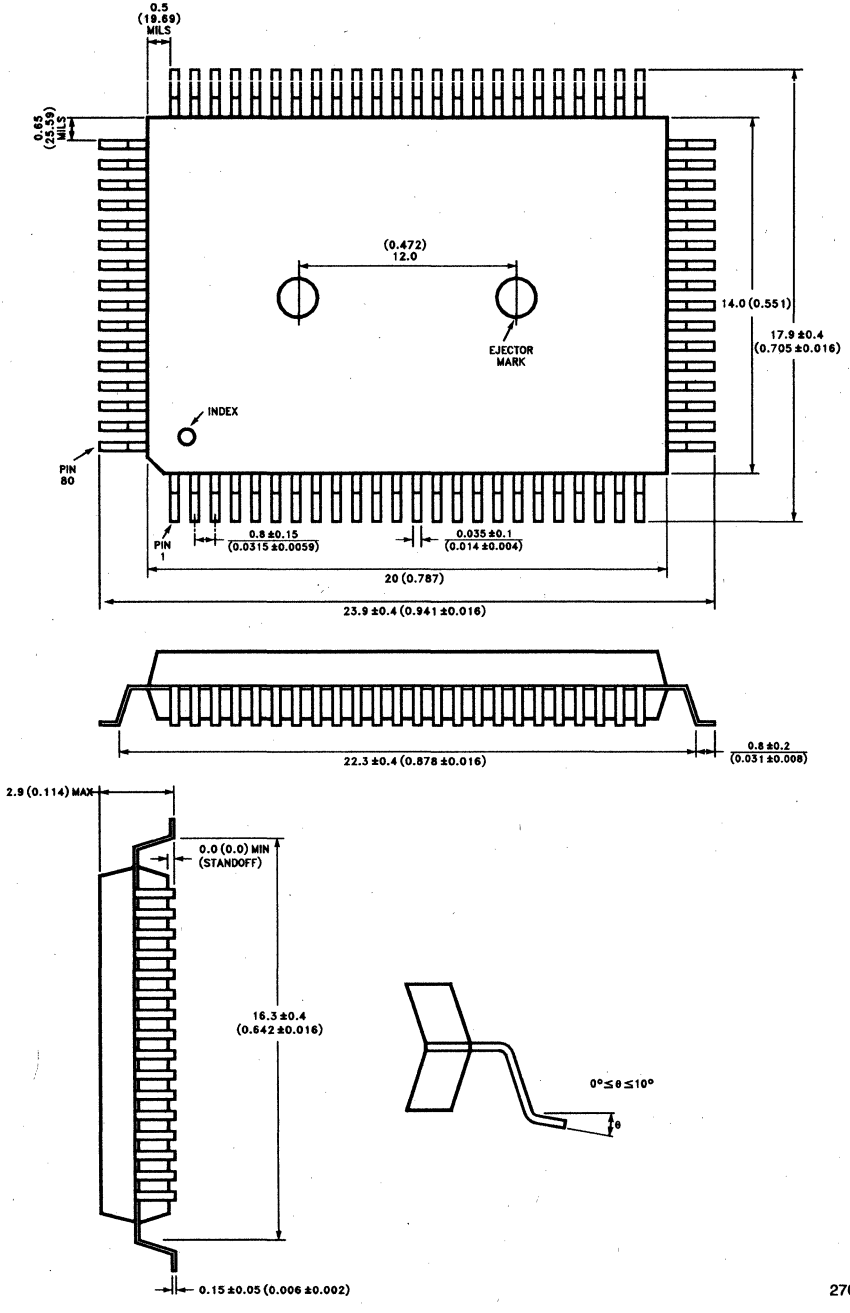

NOTE:
Units are mm (inches) unless specified.

Figure 13. QFP Principal Dimensions

ERRATA

An 80L188EB with a STEPID value of 0001H has the following known errata. A device with a STEPID of 0001H can be visually identified by noting the **absence** of an alpha character next to the FPO number or by the **presence** of an **"A"** alpha character next to the FPO number. The FPO number location is shown in Figures 2 and 3.

1. A19/$\overline{\text{ONCE}}$ is not latched by the rising edge of $\overline{\text{RESIN}}$. A19/$\overline{\text{ONCE}}$ must remain active (LOW) at all times to remain in the ONCE™ Mode. Removing A19/$\overline{\text{ONCE}}$ after $\overline{\text{RESIN}}$ is high will return all output pins to a driving state, however, the 80L188EB will remain in a reset state.
2. During interrupt acknowledge (INTA) bus cycles, the bus controller will ignore the state of the READY pin if the previous bus cycle ignored the state of the READY pin. This errata can only occur if the Chip-Select Unit is being used. All active chip-selects must be programmed to use READY (RDY bit must be programmed to a 1) if wait-states are required for INTA bus cycles.
3. CLKOUT will transition off the **rising** edge of CLKIN rather than the falling edge of CLKIN. This does not affect any bus timings other than T_{CICO}.
4. $\overline{\text{RESIN}}$ has a hysterisis of only 130 mV. It is recommended that $\overline{\text{RESIN}}$ be driven with a Schmitt triggered device to avoid processor lockup during reset when using an RC circuit.
5. SINT1 will only go active for one clock period when a receive or transmit interrupt is pending (i.e., it does not remain active until the S1STS register is read). If SINT1 is to be connected to any of the 80L188EB interrupt lines (INT0–INT4), then it must be latched by user logic.

An 80L186EB with a STEPID value of 0001H or 0002H has the following known errata. Otherwise, an 80L186EB with a STEPID value of 0002H has no known errata (as of this publication). A device with a STEPID of 0002H can be visually identified by noting the presence of a "B" or "C" alpha character next to the FPO number. The FPO number location is shown in Figures 2 and 3.

1. An internal condition with the interrupt controller can cause no acknowledge cycle on the $\overline{\text{INTA1}}$ line in response to INT1. This errata only occurs when Interrupt 1 is configured in cascade mode and a higher priority interrupt exists. This errata will not occur consistantly, it is dependent on interrupt timing.

REVISION HISTORY

The following changes have been made between the -001 version and this (-002) version of the 80L188EB data sheet. This -002 data sheet applies to any 80L188EB with a "B" alpha character after the FPO number. The FPO number location is shown in Figures 2 and 3.

1. The data sheet was changed from a Product Preview version to an Advanced Information version.
2. The DC specifications table has changed. Also notes have been changed/added.
3. Graphs for I_{CC} versus Frequency have been changed to equations with supporting text.
4. Graphs for PDTMR pin capacitance have been changed to equations with supporting text.
5. Serial port MODE 0 timings have been changed.
6. Various typing errors have been corrected throughout the document.

The following changes were made between the -002 and -003 versions of the 80L186EB data sheets. The -003 data sheet applies to any 80L186EB with a "B" alpha character after the FPO number. The FPO number location is shown in Figures 2 and 3.

1. 13 MHz Electrical, DC and AC Specifications were added to the appropriate sections.
2. The timing T_{CLOV3} was added to the AC Specifications for $\overline{S2:0}$.
3. An errata appearing on both A and B steppings (INTA1) was added.

82188
INTEGRATED BUS CONTROLLER FOR 8086, 8088, 80186, 80188 PROCESSORS

- **Provides Flexibility in System Configurations**
  - **— Supports 8087 Math Coprocessor in 8 MHz 80186 and 80188 Systems**
  - **— Provides a Low-cost Interface for 8086, 8088 Systems to an 82586 LAN Coprocessor or 82730 Text Coprocessor**
- **Facilitates Interface to one or more Multimaster Busses**
- **Supports Multiprocessor, Local Bus Systems**
- **Allows use of 80186/80188 High-Integration Features**
- **3-State, Command Output Drivers**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**
- **Available in Plastic DIP or Cerdip Package**

(See Packaging Outlines and Dimensions, Order #231369)

The 82188 Integrated Bus Controller (IBC) is a 28-pin HMOS III component for use with 80186, 80188, 8086 and 8088 systems. The IBC provides command and control timing signals plus a configurable $\overline{RQ}/\overline{GT} \longleftrightarrow$ HOLD-HLDA converter. The device may be used to interface an 8087 Math Coprocessor with an 80186 or 80188 Processor. Also, an 82586 Local Area Network (LAN) Coprocessor or 82730 Text Coprocessor may be interfaced to an 8086 or 8088 with the IBC.

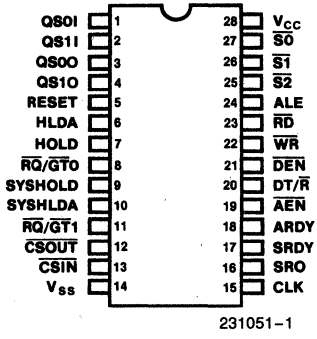

Figure 1.
82188 Pin Configuration

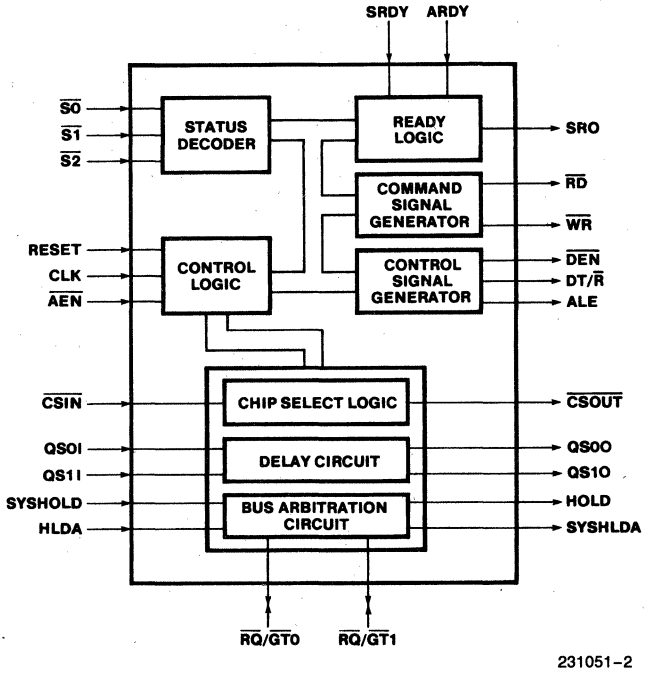

Figure 2.
82188 Block Diagram

August 1989
Order Number: 231051-005

PIN DESCRIPTIONS

Symbol	Pin No.	Type	Name and Function
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	27 26 25	I	**Status Input Pins** $\overline{S0}$–$\overline{S2}$ correspond to the status pins of the CPU. The 82188 uses the status lines to detect and identify the processor bus cycles. The 82188 decodes $\overline{S0}$–$\overline{S2}$ to generate the command and control signals. $\overline{S0}$–$\overline{S2}$ are also used to insert 3 wait states into the SRO line during the first 256 80186 bus cycles after RESET. A HIGH input on all three lines indicates that no bus activity is taking place. The status input lines contain weak internal pull-up devices.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0	0	0	interrupt acknowledge
0	0	1	read I/O
0	1	0	write I/O
0	1	1	halt
1	0	0	instruction fetch
1	0	1	read data from memory
1	1	0	write data to memory
1	1	1	passive (no bus cycle)

CLK	15	I	**CLOCK** CLK is the clock signal generated by the CPU or clock generator device. CLK edges establish when signals are sampled and generated.
RESET	5	I	**RESET** RESET is a level triggered signal that corresponds to the system reset signal. The signal initializes an internal bus cycle counter, thus enabling the 82188 to insert internally generated wait states into the SRO signal during system initialization. The 82188 mode is also determined during RESET. $\overline{RD}$, $\overline{WR}$, and $\overline{DEN}$ are driven HIGH during RESET regardless of $\overline{AEN}$. RESET is active HIGH.
$\overline{AEN}$	19	I	**Address Enable** This signal enables the system command lines when active. If $\overline{AEN}$ is inactive (HIGH), $\overline{RD}$, $\overline{WR}$, and $\overline{DEN}$ will be tri-stated and ALE will be driven LOW (DT/$\overline{R}$ will not be effected). $\overline{AEN}$ is an asynchronous signal and is active LOW.
ALE	24	O	**Address Latch Enable** This signal is used to strobe an address into address latches. ALE is active HIGH and latch should occur on the HIGH to LOW transition. ALE is intended for use with transparent D-type latches.
$\overline{DEN}$	21	O	**Data Enable** This signal is used to enable data transceivers located on either the local or system data bus. The signal is active LOW. $\overline{DEN}$ is tri-stated when $\overline{AEN}$ is inactive.
DT/$\overline{R}$	20	O	**Data TRANSMIT/RECEIVE** This signal establishes the direction of data flow through the data transceivers. A HIGH on this line indicates TRANSMIT (write to I/O or memory) and a LOW indicates RECEIVE (Read from I/O or memory).

PIN DESCRIPTIONS (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RD}$	23	O	**READ** This signal instructs an I/O or memory device to drive its data onto the data bus. The $\overline{RD}$ signal is similiar to the $\overline{RD}$ signal of the 80186(80188) in Non-Queue-Status Mode. $\overline{RD}$ is active LOW and is tri-stated when $\overline{AEN}$ is inactive.
$\overline{WR}$	22	O	**WRITE** This signal instructs an I/O or memory device to record the data presented on the data bus. The $\overline{WR}$ signal is similiar to the $\overline{WR}$ signal of the 80186(80188) in Non-Queue-Status Mode. $\overline{WR}$ is active LOW and is tri-stated when $\overline{AEN}$ is inactive.
HOLD	7	O	**HOLD** The HOLD signal is used to request bus control from the 80186 or 80188. The request can come from either the 8087 ($\overline{RQ}/\overline{GT}O$) or from the third processor (SYSHOLD). The signal is active HIGH.
HLDA	6	I	**HOLD Acknowledge** 80186 MODE–This line serves to translate the HLDA output of the 80186(80188) to the appropriate signal of the device requesting the bus. HLDA going active (HIGH) indicates that the 80186 has relinquished the bus. If the requesting device is the 8087, HLDA will be translated into the grant pulse of the $\overline{RQ}/\overline{GT}O$ line. If the requesting device is the optional third processor, HLDA will be routed into the SYSHLDA line. This pin also determines the mode in which the 82188 will operate. If this line is HIGH during the falling edge of RESET, the 82188 will enter the 8086 mode. If LOW, the 82188 will enter the 80186 mode. For 8086 mode, this pin should be strapped to V_{CC}.
$\overline{RQ}/\overline{GT}O$	8	I/O	**Request/Grant O** $\overline{RQ}/\overline{GT}O$ is connected to $\overline{RQ}/\overline{GT}O$ of the 8087 Numeric Coprocessor. When initiated by the 8087, $\overline{RQ}/\overline{GT}O$ will be translated to HOLD-HLDA to acquire the bus from the 80186(80188). This line is bidirectional, and is active LOW. $\overline{RQ}/\overline{GT}O$ has a weak internal pull-up device to prevent erroneous request/grant signals.
$\overline{RQ}/\overline{GT}1$	11	I/O	**Request/Grant 1** 80186 Mode–In 80186 Mode, $\overline{RQ}/\overline{GT}1$ allows a third processor to take control of the local bus when the 8087 has bus control. For a HOLD-HLDA type third processor, the 82188's $\overline{RQ}/\overline{GT}1$ line should be connected to the $\overline{RQ}/\overline{GT}1$ line of the 8087. 8086 MODE–In 8086 Mode, $\overline{RQ}/\overline{GT}1$ is connected to either $\overline{RQ}/\overline{GT}O$ or $\overline{RQ}/\overline{GT}1$ of the 8086. $\overline{RQ}/\overline{GT}1$ will start its request/grant sequence when the SYSHOLD line goes active. In 8086 Mode, $\overline{RQ}/\overline{GT}1$ is used to gain bus control from the 8086 or 8088. $\overline{RQ}/\overline{GT}1$ is a bidirectional line and is active LOW. This line has a weak internal pull-up device to prevent erroneous request/grant signals.

PIN DESCRIPTIONS (Continued)

Symbol	Pin No.	Type	Name and Function
SYSHOLD	9	I	**System Hold** 80186 MODE–SYSHOLD serves as a hold input for an optional third processor in an 80186(80188)-8087 system. If the 80186(80188) has bus control, SYSHOLD will be routed to HOLD to gain control of the bus. If the 8087 has bus control, SYSHOLD will be translated to $\overline{RQ}/\overline{GT}1$ to gain control of the bus. 8086 MODE–SYSHOLD serves as a hold input for a coprocessor in an 8086 or 8088 system. SYSHOLD is translated to $\overline{RQ}/\overline{GT}1$ of the 82188 to allow the coprocessor to take control of the bus. SYSHOLD may be an asynchronous signal.
SYSHLDA	10	O	**System Hold Acknowledge** SYSHLDA serves as a hold acknowledge line to the processor or coprocessor connected to it. The device connected to the SYSHOLD-SYSHLDA lines is allowed the bus when SYSHLDA goes active (HIGH).
SRDY	17	I	**Synchronous Ready** The SRDY input serves the same function as SRDY of the 80186(80188). The 82188 combines SRDY with ARDY to form a synchronized ready output signal (SRO). SRDY must be synchronized external to the 82188 and is active HIGH. If tied to V_{CC}, SRO will remain active (HIGH) after the first 256 80186 cycles following RESET. If only ARDY is to be used, SRDY should be tied LOW.
ARDY	18	I	**Asynchronous Ready** The ARDY input serves the same function as ARDY of the 80186(80188). ARDY may be an asynchronous input, and is active HIGH. Only the rising edge of ARDY is synchronized by the 82188. The falling edge must be synchronized external to the 82188. If connected to V_{CC}, SRO will remain active (HIGH) after the first 256 80186 bus cycles following RESET. If only SRDY is to be used, ARDY should be connected LOW.
SRO	16	O	**Synchronous READY Output** SRO provides a synchronized READY signal which may be interfaced directly with the SRDY of the 80186(80188) and READY of the 8087. The SRO signal is an accumulation of the synchronized ARDY signal, the SRDY signal, and the internally generated wait state signal.
QS0I QS1I	1 2	I	**Queue-Status Inputs** QS0I, QS1I are connected to the Queue-Status lines of the 80186(80188) to allow synchronization of the queue-status signals to 8087 timing requirements.
QS0O QS1O	3 4	O	**Queue-Status Outputs** QS0O, QS1O are connected to the queue-status pins of the 8087. The signals produced meet 8087 Queue-Status input requirements.

PIN DESCRIPTIONS (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{CSIN}$	13	I	**Chip-Select input** $\overline{CSIN}$ is connected to one of the chip-select lines of the 80186(80188). $\overline{CSIN}$ informs the 82188 that a bank select is taking place. The 82188 routes this signal to the chip-select output ($\overline{CSOUT}$). $\overline{CSIN}$ is active LOW. This line is not used when memory and I/O device addresses are decoded external to the 80186(80188).
$\overline{CSOUT}$	12	O	**Chip-Select Output** This signal is used as a chip-select line for a bank of memory devices. It is active when $\overline{CSIN}$ is active or when the 8087 has bus control. $\overline{CSOUT}$ is active LOW.

FUNCTIONAL DESCRIPTION

BUS CONTROLLER

The 82188 Integrated Bus Controller (IBC) generates system control and command signals. The signals generated are determined by the Status Decoding Logic. The bus controller logic interprets status lines $\overline{S0}$–$\overline{S2}$ to determine what type of bus cycle is taking place. The appropriate signals are then generated by the Command and Control Signal Generators.

The Address Enable ($\overline{AEN}$) line allows the command and control signals to be disabled. When $\overline{AEN}$ is inactive (HIGH), the command signals and $\overline{DEN}$ will be tri-stated, and ALE will be held low (DT/$\overline{R}$ will be uneffected). $\overline{AEN}$ inactive will allow other systems to take control of the bus. Control and command signals respond to a change in the $\overline{AEN}$ signal within 40 ns.

The command signals consist of $\overline{RD}$ and $\overline{WR}$. The 82188's $\overline{RD}$ and $\overline{WR}$ signals are similiar to $\overline{RD}$ and $\overline{WR}$ of the 80186(80188) in the non-Queue-Status Mode. These command signals do not differentiate between memory and I/O devices. $\overline{RD}$ and $\overline{WR}$ can be conditioned by $\overline{S2}$ of the 80186(80188) to obtain separate signals for I/O and memory devices. $\overline{RD}$ is asserted during INTA cycles, unlike $\overline{RD}$ on the 80186(80188).

The control commands consist of Data Enable ($\overline{DEN}$), Data Transmit/Receive (DT/$\overline{R}$), and Address Latch Enable (ALE). The control commands are similiar to those generated by the 80186(80188). $\overline{DEN}$ determines when the external bus should be enabled onto the local bus. DT/$\overline{R}$ determines the direction of the data transfer, and ALE determines when the address should be strobed into the latches (used for demultiplexing the address bus). DT/$\overline{R}$ does not go to an inactive (high) state at the end of bus cycles, unlike DT/$\overline{R}$ on the 80186(80188).

MODE SELECT

The 82188 Integrated Bus Controller (IBC) is configurable. The device has two modes: 80186 Mode and 8086 Mode. Selecting the mode of the device configures the Bus Arbitration Logic (see BUS ARBITRATION section for details). In 80186 Mode, the 82188 IBC may be used as a bus controller/interface device for an 80186(80188), 8087, and optional third processor system. In 8086 Mode, the 82188 IBC may be used as an interface device allowing a maximum mode 8086(8088) to interface with a coprocessor that uses a HOLD-HLDA bus exchange protocol.

The mode of the 82188 is determined during RESET. If the HLDA line is LOW at the falling edge of RESET (as in the case when tied to the HLDA line of the 80186 or 80188), the 82188 will enter into 80186 Mode. If the HLDA line is HIGH at the falling edge of RESET, the 82188 will enter 8086 Mode. In 8086 Mode, only the Bus Arbitration Logic is used. The eight pins used in 8086 Mode are: SYSHOLD, SYSHLDA, HLDA, CLK, RESET, $\overline{RQ}/\overline{GT}1$, V_{CC}, and V_{SS}. The other pins may be left unconnected.

BUS ARBITRATION

The Bus Exchange Logic interfaces up to three sets of bus exchange signals:

- HOLD-HLDA
- SYSHOLD-SYSHLDA
- $\overline{RQ}/\overline{GT}0$ ($\overline{RQ}/\overline{GT}1$)

This logic executes translating, routing, and arbitrating functions. The logic translates HOLD-HLDA signals to $\overline{RQ}/\overline{GT}$ signals and $\overline{RQ}/\overline{GT}$ signals to HOLD-HLDA signals. The logic also determines which set of bus exchange signals are to be interfaced. The mode of the 82188 and the priority of the devices requesting the bus determine the routing of the bus exchange signals.

80186 MODE

In 80186 Mode, a system may have three potential bus masters: the 80186 or 80188 CPU, the 8087 Numerics Coprocessor, and a third processor (such as the 82586 LAN or 82730 Text Coprocessor). The third processor may have either a HOLD-HLDA or $\overline{RQ}/\overline{GT}$ bus exchange protocol. The possible bus exchange signal connections and paths for 80186 Mode are shown in Figures 3 & 4 and Tables 1 & 2, respectively. If no HOLD-HLDA type third processor is used, SYSHOLD should be tied LOW to prevent an erroneous SYSHOLD signal. In 80186 mode, the bus priorities are:

Highest Priority.....Third Processor
Second Highest Priority.....8087
Default Priority.....80186

— THREE-PROCESSOR SYSTEM OPERATION (HOLD-HLDA TYPE THIRD PROCESSOR)

In the configuration shown in Figure 3, the third processor requests the bus by sending SYSHOLD HIGH. The 82188 will route (and translate if necessary) the request to the current bus master. This includes routing the request to HOLD if the 80186(80188) is the current bus master or routing and translating the request to $\overline{RQ}/\overline{GT}1$ if the 8087 is in control of the bus. The third processor's request is not passed through the 8087 if the 80186 is the bus master (see Table 1).

The 8087 requests the bus using $\overline{RQ}/\overline{GT}0$. The request pulse from the 8087 will be translated and routed to HOLD if the 80186 is the bus master. If the third processor has control of the bus, the grant pulse to the 8087 will be delayed until the third processor relinquishes the bus (sending SYSHOLD LOW). In this case, HOLD will remain HIGH during the third processor-to-8087 bus control transfer. The 80186 will not be granted the bus until both coprocessors have released it.

Table 1. Bus Exchange Paths (80186 Mode) (HOLD-HLDA Type 3rd Proc)

Requesting Device	Current Bus Master		
	80186	8087	3rd Proc
80186	n/a	n/a	n/a
8087	$\overline{RQ}/\overline{GT}0 \longleftrightarrow \frac{HOLD}{HLDA}$	n/a	n/a
3rd Proc	$\frac{SYSHOLD}{SYSHLDA} \longleftrightarrow \frac{HOLD}{HLDA}$	$\frac{SYSHOLD}{SYSHLDA} \longleftrightarrow \overline{RQ}/\overline{GT}1$	n/a

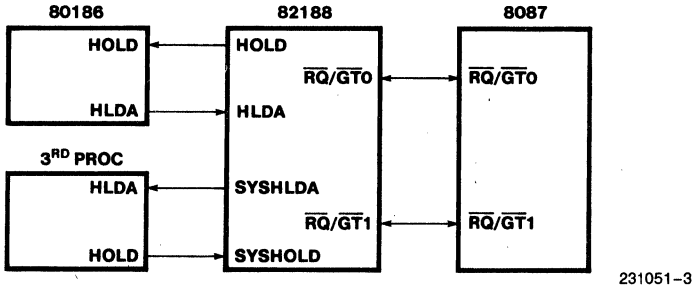

Figure 3.
Bus Exchange Signal Connections (80186 Mode) for a Three Local Processor System (HOLD-HLDA Type 3rd Proc)

Table 2. Bus Exchange Paths (80186 Mode) ($\overline{RQ}/\overline{GT}$ Type 3rd Proc)

Requesting Device	Current Bus Master		
	80186	8087	3rd Proc
80186	n/a	n/a	n/a
8087	$\overline{RQ}/\overline{GT}0 \longleftrightarrow \frac{HOLD}{HLDA}$	n/a	n/a
3rd Proc	$\overline{RQ}/\overline{GT}1 \longleftrightarrow \overline{RQ}/\overline{GT}0 \longleftrightarrow \frac{HOLD}{HLDA}$	$\overline{RQ}/\overline{GT}1$	n/a

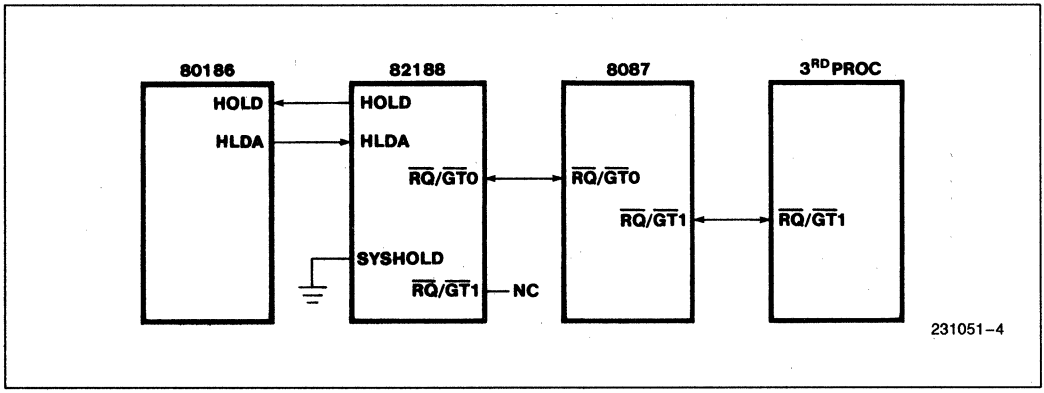

Figure 4.
Bus Exchange Signal Connections (80186 Mode) for a Three Local Processor System ($\overline{RQ}/\overline{GT}$ Type 3rd Proc)

When the bus is requested from the 80186(80188), a bus priority decision is made. This decision is made when the HLDA line goes active. Upon receipt of the HLDA signal, the highest-priority requesting device will be acknowledged the bus. For example, if the 8087 initially requested the bus, the bus will be granted to the third processor if SYSHOLD became active before HLDA was received by the 82188. In this case, the grant pulse to the 8087 will be delayed until the third processor relinquishes the bus.

— THREE-PROCESSOR SYSTEM OPERATION ($\overline{RQ}/\overline{GT}$ TYPE THIRD PROCESSOR)

In the configuration shown in Figure 4, the third processor requests the bus by initiating a request/grant sequence with the 8087's $\overline{RQ}/\overline{GT}1$ line. The 8087 will grant the bus if it is the current bus master or will pass the request on if the 80186 is the current bus master (see Table 2). In this configuration, the 82188's Bus Arbitration Logic translates $\overline{RQ}/\overline{GT}0$ to HOLD-HLDA. The 8087 provides the bus arbitration in this configuration.

8086 MODE

The 8086 Mode allows an 8086, 8088 system to contain both $\overline{RQ}/\overline{GT}$ and HOLD-HLDA type coprocessors simultaneously. In 8086 Mode, two possible bus masters may be interfaced by the 82188; an 8086 or 8088 CPU and a coprocessor which uses a HOLD-HLDA bus exchange protocol (typically an 82586 LAN Coprocessor or an 82730 Text Coprocessor). The bus exchange signal connections for 8086 Mode are shown in Figure 5. Bus arbitration signals used in the 8086 Mode are:

- $\overline{RQ}/\overline{GT}1$
- SYSHOLD
- SYSHLDA

In 8086 Mode, no arbitration is necessary since only two devices are interfaced. The coprocessor has bus priority over the 8086(8088). SYSHOLD-SYSHLDA are routed and translated directly to $\overline{RQ}/\overline{GT}1$. $\overline{RQ}/\overline{GT}1$ of the 82188 may be tied to either $\overline{RQ}/\overline{GT}0$ or $\overline{RQ}/\overline{GT}1$ of the 8086(8088).

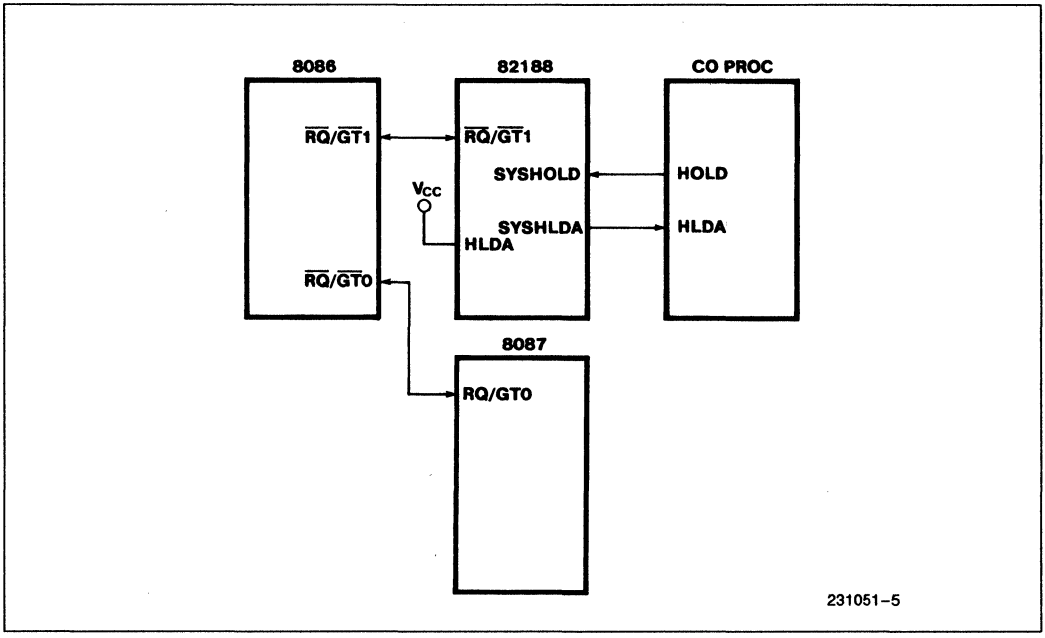

Figure 5. Bus Exchange Signal Connections (8086 Mode)

QUEUE-STATUS DELAY

The Queue-Status Delay logic is used to delay the queue-status signals from the 80186(80188) to meet 8087 queue-status timing requirements. QS0I, QS1I correspond to the queue-status lines of the 80186(80188). The 82188 delays these signals by one clock phase. The delayed signals are interfaced to the 8087 queue-status lines by QS0O, QS1O.

CHIP-SELECT

The Chip-Select Logic allows the utilization of the chip select circuitry of the 80186(80188). Normally, this circuitry could not be used in an 80186(80188)-8087 system since the 8087 contains no chip select circuitry. The Chip-Select Logic contains two external connections: Chip-Select Input ($\overline{CSIN}$) and Chip-Select Output ($\overline{CSOUT}$). $\overline{CSOUT}$ is active when either $\overline{CSIN}$ is active or when the 8087 has control of the bus.

By using $\overline{CSOUT}$ to select memory containing data structures, no external decoding is necessary. The 80186 may gain access to this memory bank through the $\overline{CSIN}$ line while the 8087 will automatically obtain access when it becomes the bus master. Note that this configuration limits the amount of memory accessible by the 8087 to the physical memory bank selected by $\overline{CSOUT}$. Systems where the 8087 must access the full 1 Megabyte address space must use an external decoding scheme.

READY

The Ready logic allows two types of Ready signals: a Synchronous Ready Signal (SRDY) and an Asynchronous Ready Signal (ARDY). These signals are similiar to SRDY and ARDY of the 80186. Wait states will be inserted when both SRDY and ARDY are LOW. Inserting wait states allows slower memory and I/O devices to be interfaced to the 80186(80188)-8087 system.

ARDY's LOW-to-HIGH transition is synchronized to the CPU clock by the 82188. The 82188 samples ARDY at the beginning of T2, T3 and Tw until sampled HIGH. Note that ARDY of the 82188 is sampled one phase earlier than ARDY of the 80186. ARDY's falling edge must be synchronous to the CPU clock. ARDY allows an easy interface with devices that emit an asynchronous ready signal.

The SRDY signal allows direct interface to devices that emit a synchronized ready signal. SRDY must be synchronized to the CPU clock for both of its transitions. SRDY is sampled in the middle of T2, T3 and in the middle of each Tw. An 82188-80186(80188)'s SRDY setup time is 30 ns longer than the 80186(80188)'s SRDY setup time. SRDY eliminates the half-clock cycle penalty necessary for ARDY to be internally sychronized.

The sychronized ready output (SRO) is the accumulation of SRDY, ARDY, and the internal wait-state

generator. SRO should be connected to SRDY of the 80186(80188) (with 80186(80188)'s ARDY tied LOW), and READY of the 8087.

SRDY	ARDY	SRO
0	0	0
1	X	1
X	1	1

The internal wait state generator allows for synchronization between the 80186(80188) and 8087 in 80186 mode. Upon RESET, the 82188 automatically inserts 3 wait-states per 80186(80188) bus cycle, overlapped with any externally produced wait-states created by ARDY and SRDY.

Since the 8087 has no provision for internal wait-state generation, only externally created wait states will be effective. The 82188, upon RESET, will inject 3 wait states for each of the first 256 80186(80188) bus cycles onto the SRO line. This will allow the 8087 to match the 80186(80188)'s timing.

The internally-generated wait states are overlapped with those produced by the SRDY and ARDY lines. Overlapping the injected wait states insures a minimum of three wait states for the first 256 80186(80188) bus cycles after RESET. Systems with a greater number of wait states will not be affected. Internal wait state generation by the 82188 will stop on the 256th 80186(80188) bus cycle after RESET. To maintain sychronization between the 80186(80188) and 8087, the following conditions are necessary:

- The 80186(80188)'s control block must be mapped in I/O space before it is written to or read from.
- All memory chip-select lines must be set to 0 WAIT STATES, EXTERNAL READY ALSO USED within the first 256 80186(80188) bus cycles after RESET.

An equivalent READY logic diagram is shown in Figure 6.

SYSTEM CONSIDERATIONS

In any 82188 configuration, clock compatibility must be considered. Depending on the device, a 50% or a 33% duty-cycle clock is needed. For example, the 80186 and 80188 (as well as the 82188, 82586, and 82730) requires a 50% duty-cycle clock. The 8086, 8088 and their 'kit' devices' (8087, 8089, 82C88, and 8289) clock requirements, on the other hand, require a 33% duty-cycle clock signal. The system designer must make sure clock requirements of all the devices in the system are met.

Figure 7 demonstrates the usage of the 82188 in 80186 Mode where it is used to interface an 8087 into an 80186 system. In this case, the clock requirements of the 8087 are met by specifying the 10 MHz (8087-1) device, but clocking the system at a maximum rate of 8 MHz.

Status bit six (S6) from the main processor (8086, 8088, 80186, or 80188) is used by the 8087 to track the instruction flow. S6 is multiplexed with address bit 19 (A19). If the third processor generates only 16 bits of address, S6 is not generated. A19/S6 must be driven high by external circuitry during the status portion of bus cycles controlled by the third processor.

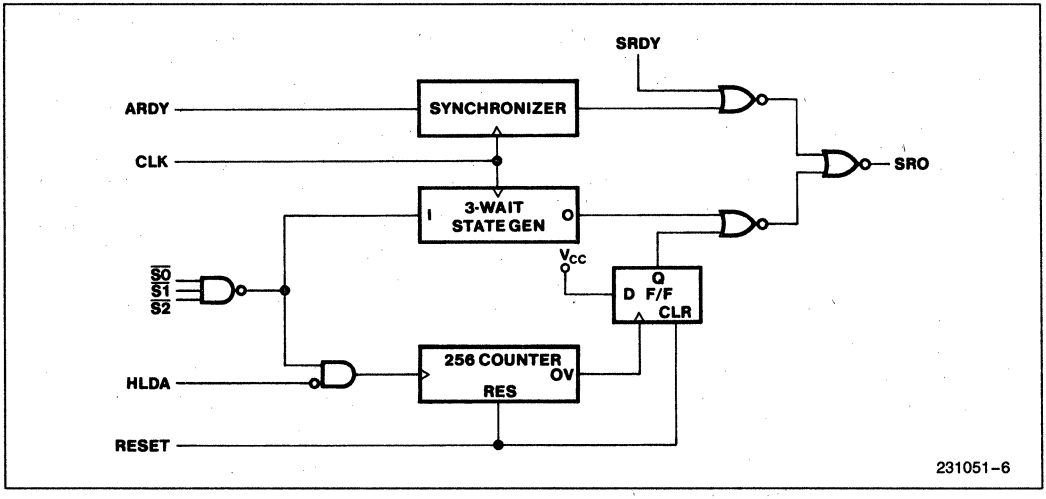

Figure 6. Equivalent 82188 READY Circuit

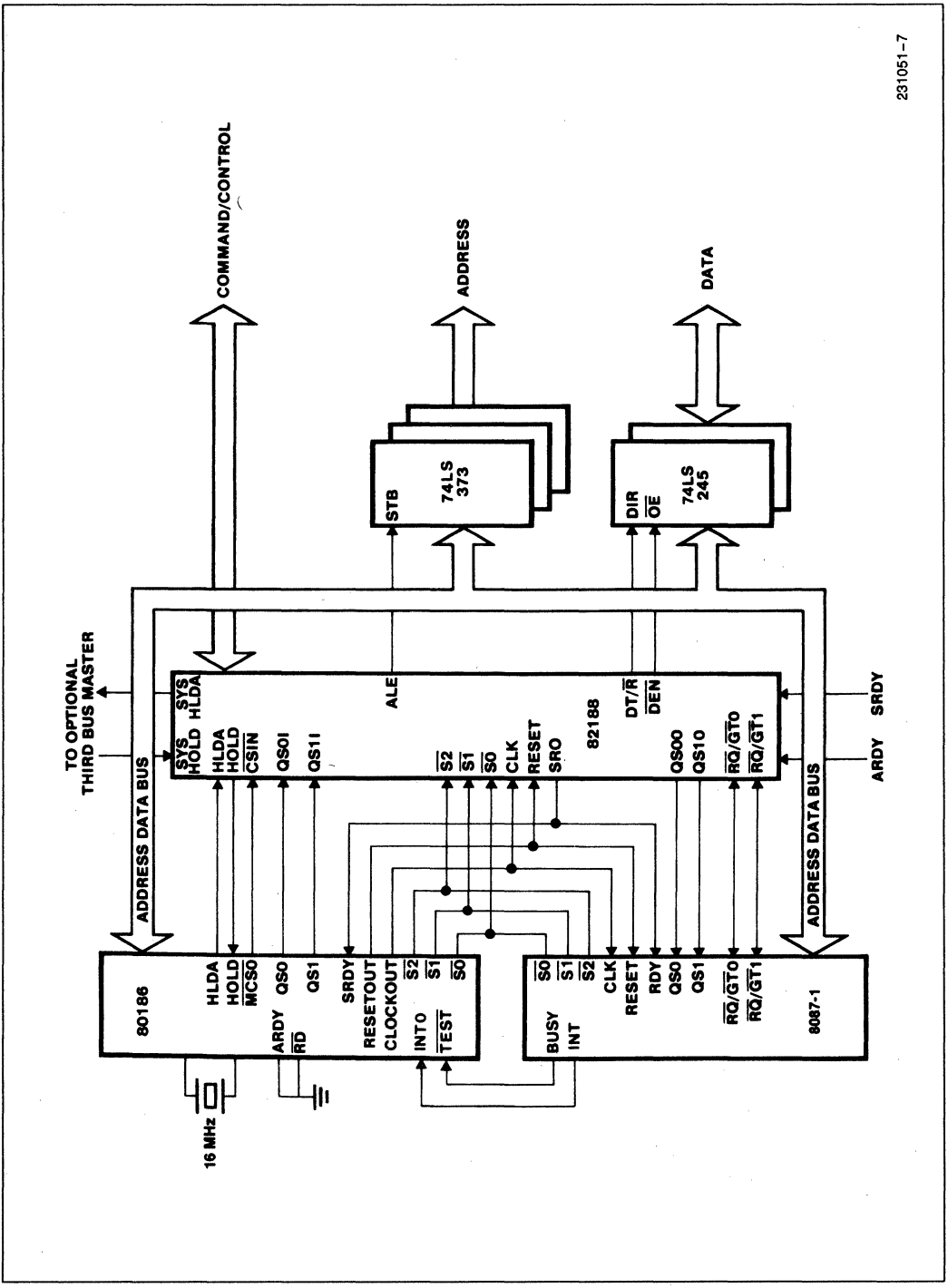

Figure 7.
80186/8087-1 System Using the 82188 in 80186 Mode

ABSOLUTE MAXIMUM RATINGS *

Temperature Under Bias .....0°C to 70°C
Storage Temperature.....−65°C to 150°C
Case Temperature .....0°C to +85°C
Voltage on any Pin with
Respect to GND .....−1.0V to 7.0V
Power Dissipation.....0.7 Watts

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Units	Test Cond.
V_{IL}	Input Low Voltage	−0.5	+0.8	volts	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	volts	
V_{OL}	Output Low Voltage		0.45	volts	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		volts	I_{OH} = −400 μA
I_{CC}	Power Supply Current		100	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	μA	$0V < V_{IN} < V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45 < V_{OUT} < V_{CC}$
V_{CLI}	CLK Input Low Voltage	−0.5	+0.6	volts	
V_{CHI}	CLK Input High Voltage	3.9	V_{CC} +1.0	volts	
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		20	pF	

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, T_{CASE} = 0°C to +85°C)

TIMING REQUIREMENTS

Symbol	Parameter	Min	Max	Units	Notes
TCLCL	Clock Period	125	500	ns	
TCLCH	Clock LOW Time	½TCLCL-7.5		ns	
TCHCL	Clock HIGH Time	½TCLCL-7.5		ns	
TARYHCL	ARDY Active Setup Time	20		ns	
TCHARYL	ARDY Hold Time	15		ns	8
TARYLCH	ARDY Inactive Setup Time	35		ns	
TSRYHCL	SRDY Input Setup Time	65,50		ns	1
TSVCH	STATUS Active Setup Time	55		ns	
TSXCL	STATUS Inactive Setup Time	50		ns	
TQIVCL	QS0I, QS1I Setup Time	15		ns	
THAVGV	HLDA Setup Time	50		ns	
TSHVCL	SYSHOLD Asynchronous Setup Time	25		ns	
TGVCH	$\overline{RQ}/\overline{GT}$ Input Setup Time	0		ns	6

TIMING RESPONSES

Symbol	Parameter	Min	Max	Units	Notes
TSVLH	STATUS Valid to ALE Delay		30	ns	4
TCHLL	ALE Inactive Delay		30	ns	
TCLML	$\overline{RD}$, $\overline{WR}$ Active Delay	10	70	ns	
TCLMH	$\overline{RD}$, $\overline{WR}$ Inactive Delay	10	55	ns	
TSVDTV	STATUS to DT/$\overline{R}$ Delay		30	ns	3
TCLDTV	DT/$\overline{R}$ Active Delay		55	ns	3
TCHDNV	$\overline{DEN}$ Active Delay	10	55	ns	
TCHDNX	$\overline{DEN}$ Inactive Delay	10	55	ns	
TCLQOV	QS0O, QS1O Delay	5	50	ns	
TCHHV	HOLD Delay		50	ns	2,6
TCLSAV	SYSHLDA Delay		50	ns	6
TCLGV	$\overline{RQ}$/$\overline{GT}$ Output Delay		40	ns	6
TGVHV	$\overline{RQ}$/$\overline{GT}$0 To HOLD Delay		50	ns	2,6
TCLLH	ALE Active Delay		30	ns	4
TAELCV	Command Enable Delay		40	ns	
TAEHCX	Command Disable Delay		40	ns	
TCHRO	SRO Output Delay	5	30	ns	5,6
TSRYHRO	SRDY To SRO Delay		30	ns	5
TCSICSO	$\overline{CSIN}$ To $\overline{CSOUT}$ Delay		30	ns	
TCLCSOV	CLK Low to $\overline{CSOUT}$ Delay	10		ns	
TCLCSOH	CLK Low to $\overline{CSOUT}$ Inactive Delay	10		ns	

NOTES (applicable to both spec listing and timing diagrams):
1. TSRYHOL = (80186's) TSRYCL + 30 ns=65 ns for 6 MHz operation and 50 ns for 8 MHz operation.
2. Timing not tested.
3. DT/$\overline{R}$ will be asserted to the latest of TSVDTV & TCLDTV.
4. ALE will be asserted to the latest of TSVLH & TCLLH.
5. SRO will be asserted to the latest of TCHRO & TSRYHRO.
6. CL = 20–100 pF
7. Address/Data bus shown for reference only.
8. The falling edge of ARDY must be synchronized to CLK.

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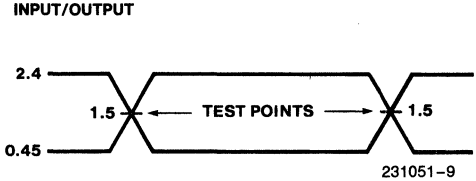
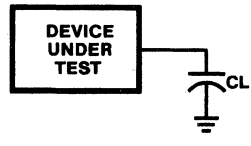
A.C. TESTING INPUT, OUTPUT WAVEFORM

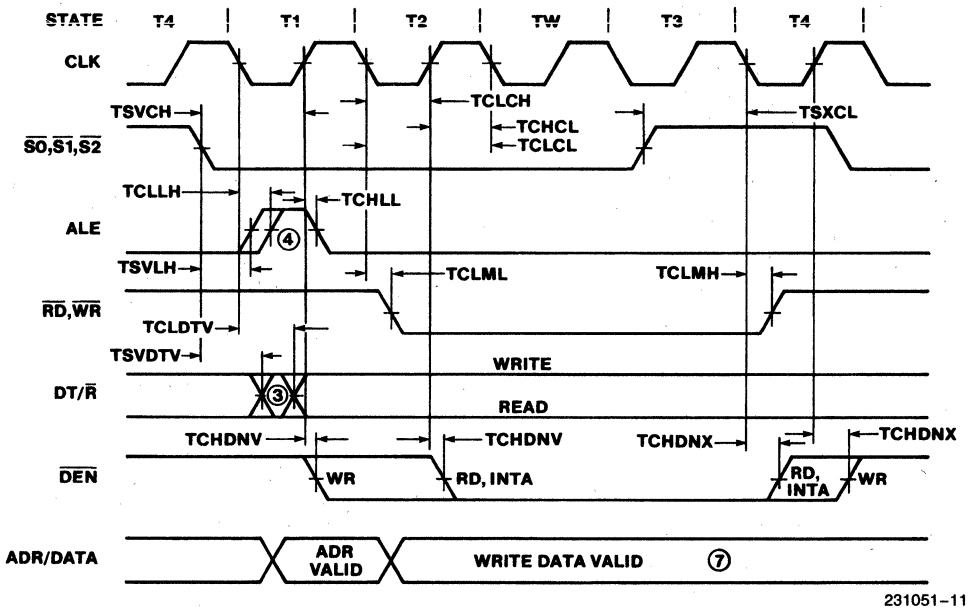


A.C. Testing: Inputs are driven at 2.4V for a Logic '1' and 0.45V for a Logic '0'.

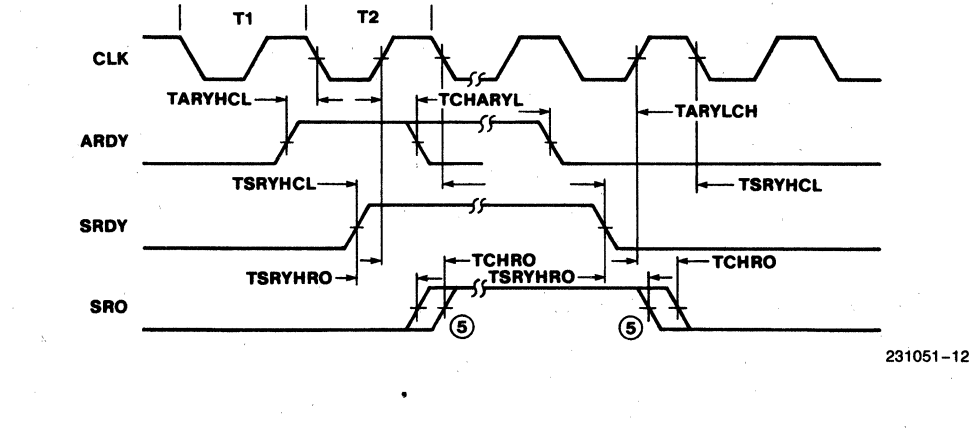
A.C. TESTING LOAD CIRCUIT



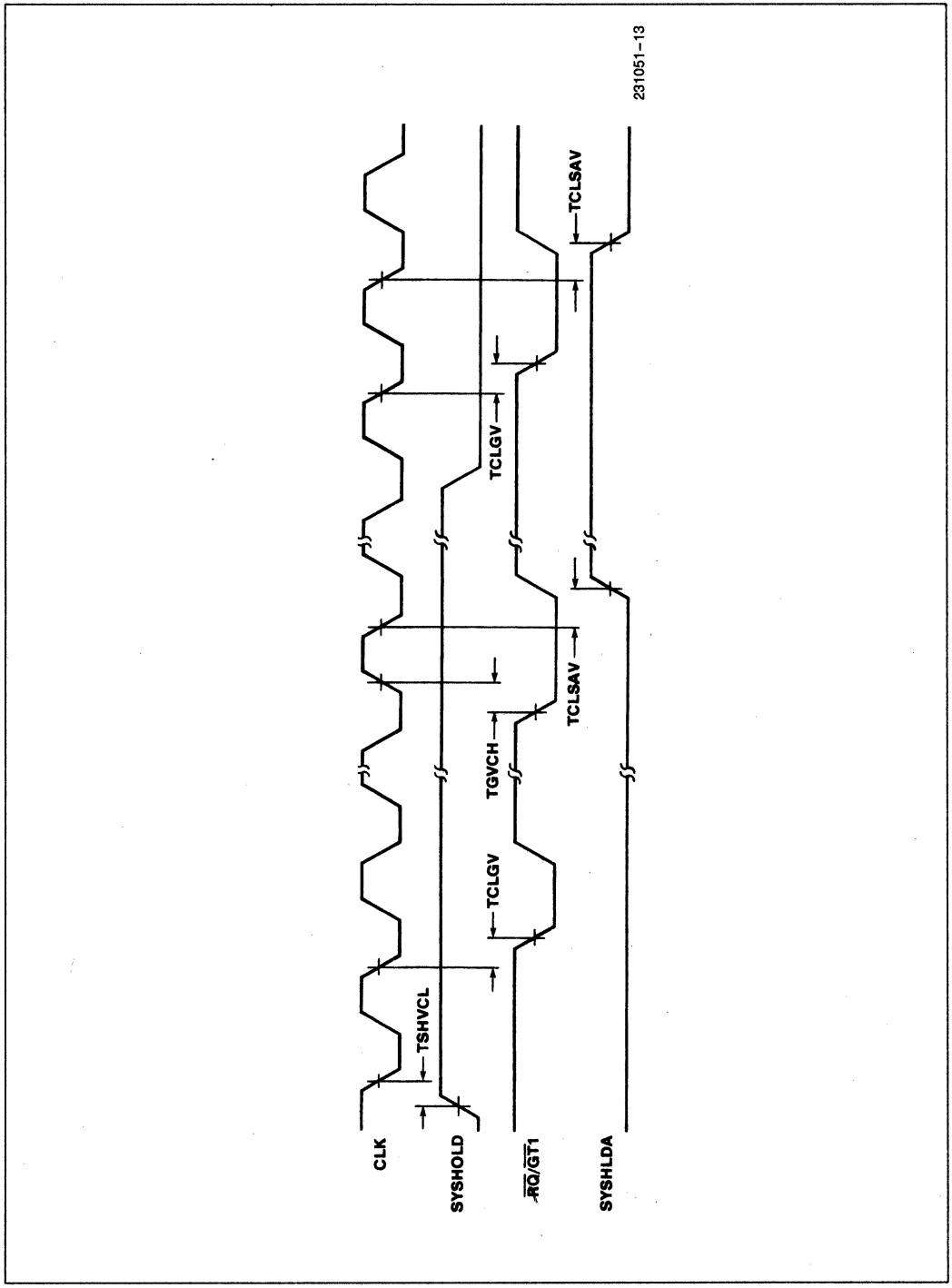
C_L includes Jig Capacitance
C_L = 20–200 pF unless otherwise noted



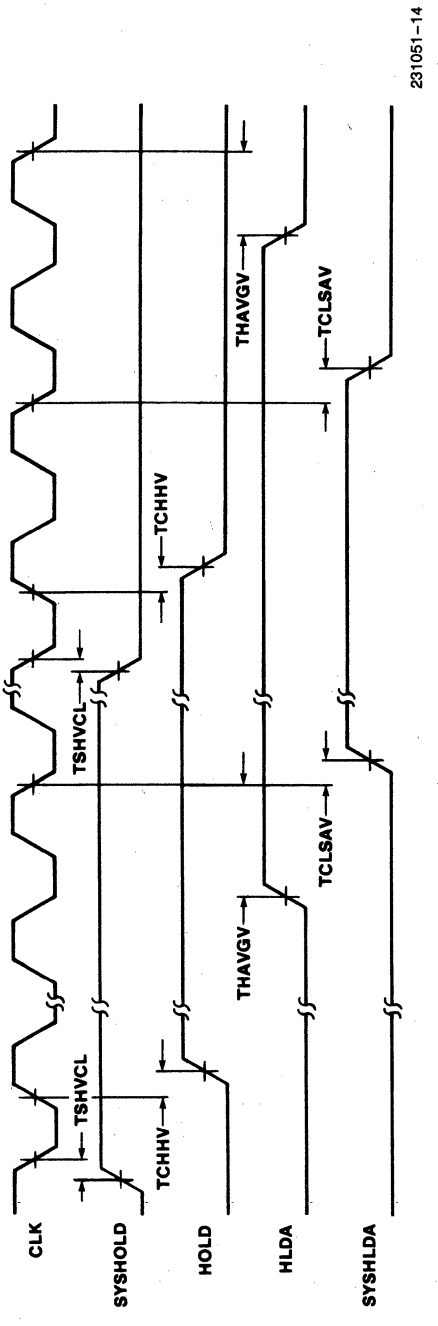
Command and Control Waveforms–80186 Mode



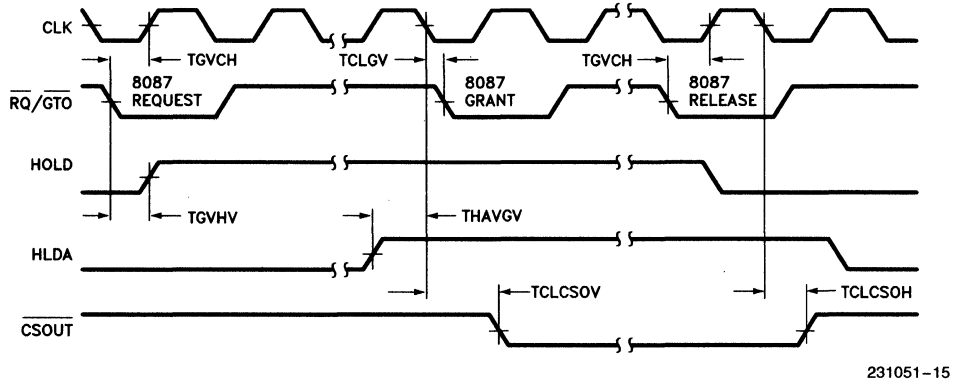
READY Timing–80186 Mode



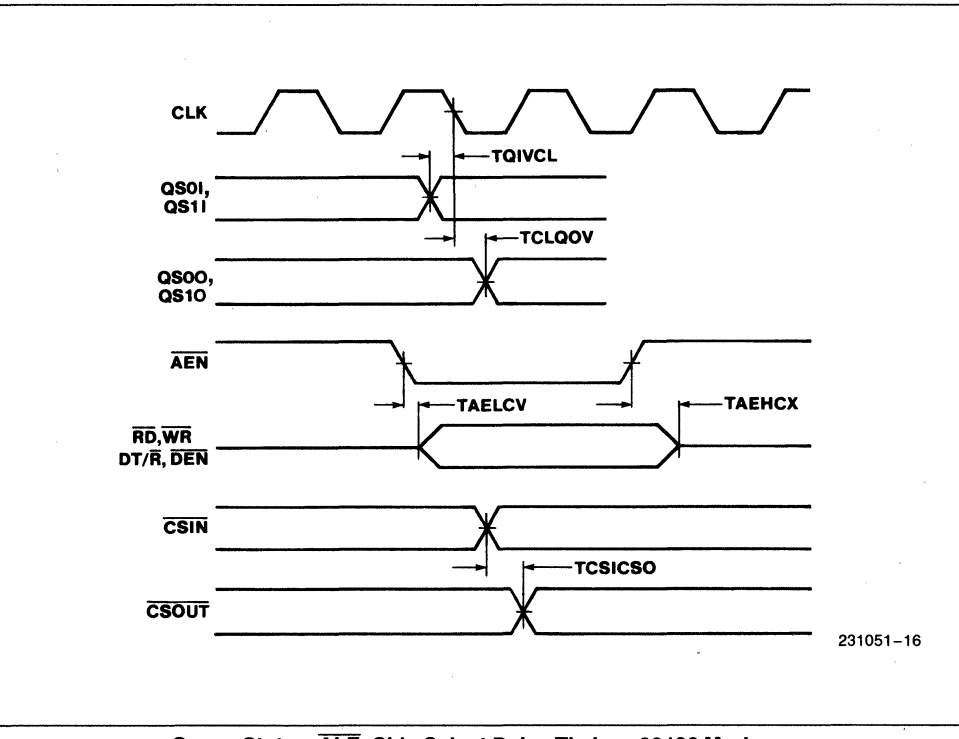
SYSHOLD-SYSHLDA to $\overline{RQ}/\overline{GT}1$ Timing–80186 Mode and 8086 Mode



SYSHOLD-SYSHLDA To HOLD-HLDA Timing–80186 Mode



RQ/GT0 to HOLD-HLDA Timing–80186 Mode



Queue Status, ALE, Chip Select Delay Timing–80186 Mode

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REVISION HISTORY

The sections significantly revised since version -004 are:

Bus Controller	Added note describing $\overline{RD}$ during $\overline{INTA}$ and DT/$\overline{R}$ compared to the 80186/80188.
System Considerations	Use of 82188 with 80186 and 8087-1, all at 8 MHz, is clarified.

The sections significantly revised since version -002 are:

AC Characteristics	T_{QIVCL} (min.) changed from 10 ns to 15 ns. Minimum timings for T_{CLML}, T_{CLMH}, and T_{CHDNV} changed from 0 ns to 10 ns. T_{CHDNX} (min.) changed from 5 ns to 10 ns. Minimum timings or T_{SVDTV}, T_{CLDTV}, and T_{CLLH} are no longer indicated (they were 0 ns). T_{CLCSOV} and T_{CLCSOH} added.

80186/80188 Development Support Tools

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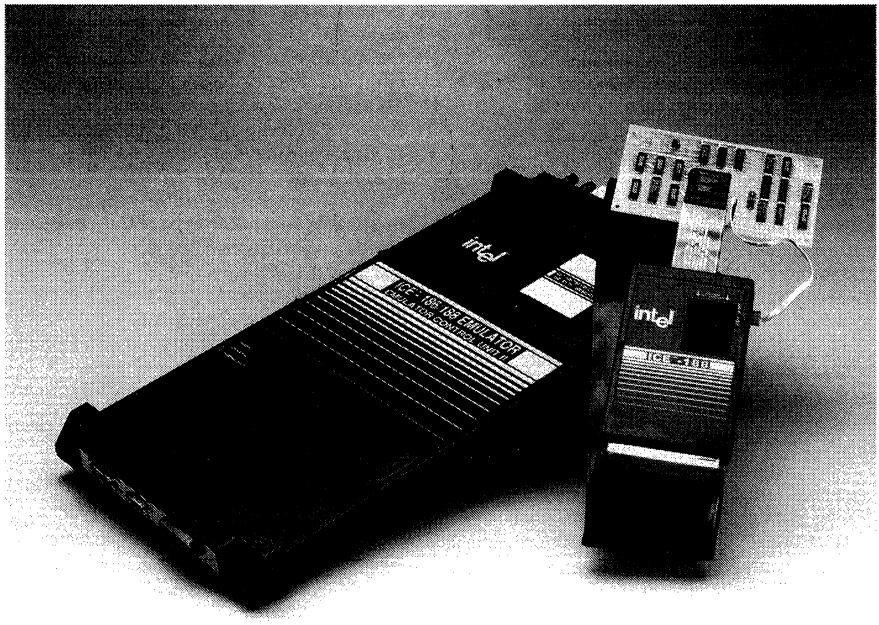
ICE™-186/188 FAMILY IN-CIRCUIT EMULATOR



281422-1

INCLUDING PARADIGM DEBUG/ICE WINDOWED INTERFACE

PRODUCT OVERVIEW

The Intel ICE™-186/188 family of In-Circuit Emulators deliver outstanding 16 MHz and 20 MHz real-time emulation for the 80C186/80C188 family of microprocessors: 80C186EB/C188EB, 80C186XL/C188XL, 80C186EA/C188EA, 80C186EC/C188EC, 80C186/C188, and 80186/188. The emulator is a versatile and efficient tool for developing, debugging, and testing products designed with Intel microprocessors. Included with the emulator is the standard Intel Windowed Interface and the Paradigm DEBUG/ICE Interface (based on Borland's Turbo Debugger), allowing you to choose the interface best suited for your needs. Both interfaces support Intel, Borland, and Microsoft languages including C++ to meet your embedded design needs and accelerate your time to market.

25

FEATURES

- Reliable full speed emulation up to 16 MHz and 20 MHz
- One probe, jumper-configurable for 186 or 188 support
- Two powerful windowed human interfaces with mouse support
- Source level debug with source code window, symbolic debug. and watch window operations
- Supports Intel, Borland, and Microsoft languages including C++

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Turbo Debugger is a registered trademark of Borland International.
Microsoft and MS-DOS are registered trademarks of Microsoft Corporation.
Link and Locate++ is a registered trademark of Systems and Software. Inc.

September 1992
Order Number: 281422-001

intel

ICE™-186/188 FAMILY IN-CIRCUIT EMULATOR

- 512K or 1 MB of zero wait-state mapped memory
- 4K frames dynamic trace buffer can be displayed without stopping emulation
- Powerful GO command with two-level breakpoints. event counters and single stepping capability
- 80C187 numberic coprocessor support
- Emulation support for all Intel component packages
- High speed RS-232C and GPIB communication link
- Stand Alone Self Test (SAST) unit for software development and self test
- Complete Intel service and support

PRODUCT HIGHLIGHTS

- Superior Intel component bondout and advanced cable technology ensures accurate and reliable high speed emulation
- Zero power consumption difference between using the emulator and the component
- Supports debugging target systems with 80C187 numeric coprocessor
- Supports all Intel software products, including C, assembler, and PL/M. Also accepts Microsoft and Borland object code. including C++, when used in conjunction with either Paradigm Systems LOCATE or Systems and Software, Inc. LINK and LOCATE++
- Paradigm DEBUG/ICE product includes Paradigm LOCATE, OMFCVT and TDCONVRT: everything necessary to support your embedded application
- Includes two powerful windowed human interfaces: the standard Intel interface and the Paradigm DEBUG/ICE interface, based on Borland's Turbo Debugger
- Each windowed interface enables user to open multiple windows simul- taneously, providing source code, watch variables, memory, and trace information
- Display and modify all on-chip peripheral registers
- Powerful GO command permits precise emulation control through versatile event recognition, condi- tional constructs, and internal actions (e.g., full trace buffer, event counters)
- Set software breakpoints easily in source code, hardware breakpoints on execution and bus addresses; memory and I/O cycles
- Break and trace on address and/or data specification based on single value, range, or "don't cares"
- Flexible STEP command, enabling forward/ reverse stepping and into or over function calls
- Define all or sections of map memory as Guarded, ICE, or User
- 4K trace buffer collects both execution and data bus activity in real-time. Display either instructions, cycles, or both
- Stand Alone Self Test (SAST) Unit in conjunction with emulator map mem- ory facilitates early software debug- ging and emulator confidence testing
- 512K and 1 MB zero wait-state memory modules can be used in place of target memory for code debugging
- Programmable fastbreak for monitoring target system while in emulation
- Refresh, DMA, and HOLD/HOLDA cycles honored when emulator halted
- RS-232C serial link provides transfer rate up to 57.6 Kbytes per second. GPIB driver (in conjunction with a user supplied National Instruments (IEEE-488) GPIB communication board) provides parallel transfers at rates up to 115 Kbytes per second
- Logic analyzer support included via a 60-pin connector to emulator
- All component packages supported, either directly on the probe or through adapters
- World-wide service, support, and training available

BENEFITS

- Supports low power application needs. Probe draws low power current, supports true CMOS voltage input/output
- Both the Intel and Paradigm windowed interfaces increase productivity for both expert and casual users. Pull-down menus, on-line help, and mouse support simplify debugging and speeds up learning curve
- Source code window automatically updated when emulator halts, high-lighting next instruction to be executed
- Software and hardware breakpoints may be set directly in the source code window to facilitate precise emulation control
- Emulator can track user-defined program variables using the watch window. Emulator tracks the variable, not the user!
- Intel interface offers "C"-based macro commands to facilitate customized or repeated debug sessions. Extremely useful for automated manufacturing, testing and debugging

ICE™-186/188 FAMILY IN-CIRCUIT EMULATOR

- Powerful trace collection and display commands allow user to collect and display only the trace information pertinent to the debug session; no unwanted trace data filling up trace buffer
- Dynamic trace allows user to view trace buffer or modify trace conditions without stopping emulation
- Software developers may debug application code before target hardware is available using the Stand Alone Self Test (SAST) Unit with emulator map memory
- Early debugging of ROM memory simplified using emulator map memory. Memory addressable in 32 Kbyte increments. Supports debugging ROM-based applications over entire 1MB addressing range
- Mappable I/O ports, addressable in 4 Kbyte increments, enable user to debug suspect I/O behavior. PC resources allow data 'input' from keyboard and data 'output' to the screen
- Source code window displays source code in original high-level language used to produce the object code. Simplifies and accelerates debug process
- Investigate privileged processor information during emulation using the Fastbreak feature (e.g., PCB, registers, target memory)
- DRAM refresh signals continue even when emulator halted and ensures DRAM memory not lost or corrupted. Also permits emulation in cost-sensitive applications that do not include DRAM controllers
- Continuous timer function while emulator halted allows emulator to respond to on-chip and external interrupts in real-time. Useful for critical applications where continuous interrupt-service is a requirement
- Detailed timing of specific events possible using a logic analyzer connected to the emulator. An external sync signal can trigger the logic analyzer, enabling complex event triggering

SERVICE, SUPPORT, AND TRAINING

- Intel offers full array of seminars, classes, workshops, field application engineering expertise, hotline technical support, and on-site service
- Software support contract available, providing technical software information, telephone support, automatic software and manual updates, 'iComments' publication and a development tools Trouble-Shooting Guide
- 90-day software warranty and one year hardware support package are standard. Includes technical hardware information, telephone support, warranty on parts, labor, material, and on-site hardware support
- Intel Development Tools offers a 30-day, money-back guarantee to customers who are dissatisfied with their Intel development tool

SUMMARY

The ICE™-186/188 family of In-Circuit Emulators provide a versatile and efficient tool for developing, debugging, and testing products designed with the 80C186/80C188 family of micropro- cessors. The emulator includes numerous productivity boosting features to enable you to move your products to market as quickly as possible. Intel, the inventor of the 80C186/80C188 family of micropro- cessors, offers the most complete line of development tools from a single vendor to meet all of your development needs for your embedded design.

PHYSICAL DESCRIPTION AND CHARACTERISTICS

For all the ICE-18x emulators the maximum probe power draw from the target is 90 mA (same as the component).

ICE-18xEAXL

Table 1. ICE-18xEAXL Physical Characteristics

Unit	Width		Height		Length	
	In.	Cm	In.	Cm	In.	Cm
Emulator Control Unit	10.4	26.4	1.7	4.32	0.7	52.6
Power Supply	7.7	19.6	4.1	10.4	11.0	27.9
Memory Module	4.8	12.1	0.6	1.4	5.2	13.2
User Probe	4.0	10.2	0.65	1.6	7.0	17.8
User Probe Adapter Cable					3.4	8.6
Stand Alone Self Test	4.3	10.9	0.60	1.5	6.7	17.0
Serial Cable					144.0	366.0

ICE-18xEB:

Table 2. ICE-18xEB Physical Characteristics

Unit	Width		Height		Length	
	In.	Cm	In.	Cm	In.	Cm
Emulator Control Unit	10.4	26.4	1.7	4.3	20.7	52.6
Power Supply	7.7	19.6	4.1	10.4	11.0	27.9
Memory Module	4.8	12.1	0.6	1.4	5.2	13.2
User Probe	4.0	10.2	0.65	1.6	7.0	17.8
User Probe Adapter Cable					3.4	8.6
Stand Alone Self Test	4.3	10.9	0.60	1.5	6.7	17.0
Serial Cable					144.0	366.0

ICE™-186/188 FAMILY IN-CIRCUIT EMULATOR

ICE-18xEC:

Table 3. ICE-18xEC Physical Characteristics

Unit	Width		Height		Length	
	In.	Cm	In.	Cm	In.	Cm
Emulator Control Unit	10.4	26.4	1.7	4.3	20.7	52.6
Power Supply	7.7	19.6	4.1	10.4	11.0	27.9
Memory Module	4.8	12.1	0.6	1.4	5.2	13.2
User Probe	4.0	10.2	0.65	1.6	7.0	17.8
User Probe Adapter Cable					3.4	8.6
Stand Alone Self Test	4.3	10.9	0.60	1.5	6.7	17.0
Serial Cable					144.0	366.0

HOST SYSTEM REQUIREMENTS

	Intel Interface	Paradigm IDI:BUGiICE Interface
Computer	IBM PC, PS/2 or compatible, i386 recommended	IBM PC, PS/2 or compatible, i386 recommended
Operating System	MS-DOS/PC-DOS 3.3/5.0	MS-DOS/PC-DOS 3.0 or later
System RAM	520 Kbytes	384 Kbytes
Expanded Memory	1.5 MB(1)	Recommended for optimal performance
Hard Disk	3 MB	1 MB
Communication	Serial Port (COM1 or COM2) supporting at least 9600 Baud Rate OR National Instruments GPIB-PCIIA board	Serial Port (COM1 or COM2) supporting at least 9600 Baud Rate OR National Instruments GPIB-PCIIA board
Math Coprocessor	Required	Not required

Note 1: Above Board managed by EMM.slts driver recommended. otber memory managers conforming to the Lotus/Intel/ Microsoft Expanded Memory specifications. version 3.2 or later. arc available.

ORDERING INFORMATION

Emulator (Host)	Component Support	Speed (MHz)	Description
ICE18XEAXLP (DOS)	80C186XL/C188XL 80C186EA/C188EA 80C186/C188 80186/188	16	68-pin PLCC. Includes Control Unit, probe, power supply. SAST, Intel and Paradigm interfaces and PLCC to LCC adapter. Requires MEM512 or MEM1MB memory option.
ICE18XEAXLP20 (DOS)	80C186XL/C188XL 80C186EA/C188EA	20	68-pin PLCC Includes Control Unit, probe, power supply SAST, Intel and Paradigm interfaces. PLCC to LCC adapter and 512K Map Memory.
ICE18XEBP (DOS)	80C186EB/C188EB	16	84-pin PLCC. Includes Control Unit, probe, power supply, SAST and Intel and Paradigm interfaces. Requires MEM512 or MEM1MB memory option.
ICE18XEBP20 (DOS)	80C186EB/C188EB	20	84-pin PLCC includes Control Unit, probe, power supply, SAST and Intel and Paradigm interfaces and 512K Map Memory.
ICE18XECQ (DOS)	80C186EC/C188EC	16	100-pin QFP. Includes Control Unit, probe, power supply, SAST, and Intel and Paradigm interfaces. Requires MEM512 or MEM1MB memory option.

Probe (Host)	Component Support	Speed (MHz)	Description
UP18XEANLP (DOS)	80C186XL/C188NL 80C186EA/C188EA 80C186/C188 80186/188	16	68-pin PLCC. Includes probe, SAST, Intel and Paradigm interfaces and PLCC to LCC adapter.
UP18XEBP (DOS)	80C186EB/C188EB	16	84-pin PLCC. Includes probe. SAST and Intel and Paradigm Interfaces.
UP18XECQ (DOS)	80C186EC/C188EC	16	100-pin QFP. Includes probe, SAST, and Intel and Paradigm Interfaces.

Memory	Memory Size	Description
MEM512	512 KBytes	512K Emulator Map Memory for ICE-18x Emulators
MEM1MB	1 MByte	1 MB Emulator Map Memory for ICE-18x Emulators

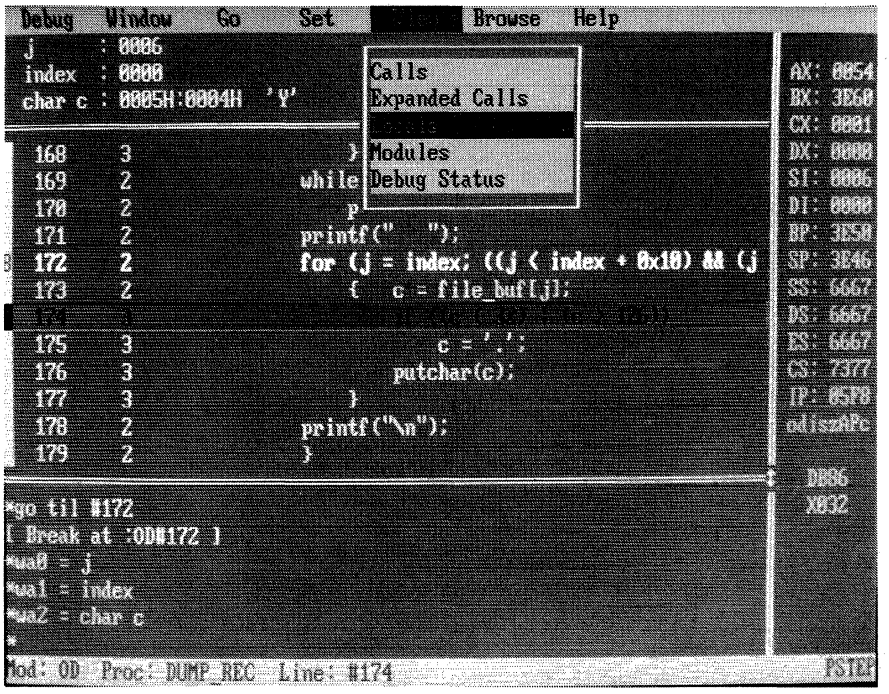
ICE™-186/188 FAMILY IN-CIRCUIT EMULATOR

Emulator Software (Host)	Description
PDICE18XKIT (DOS)	Paradigm Debug/ICE Software for old ICE186N, ICE188N, ICE18616N and ICE18816N emulators. Based on Borland Turbo Debugger. Supports all Emulator Control Units.
PDICE18XEBKIT (DOS)	Paradigm Debug/IcE Software for ICE18XEBP and ICE18XEBP20 emulators. Based on Borland Turbo Debugger.
SWICE18XKIT(1) (DOS)	Intel Windowed Human Interface for old ICE186N, ICE188N, ICE18616N and ICE18816N emulators. Supports all Emulator Control Units.
SWICE18XEAXLKIT(1) (DOS)	Intel Windowed Human Interface for ICE18XEAXLP and ICE18XEAXLP20 emulators.
SWICE18XEBKIT(1) (DOS)	Intel Windowed Human Interface for ICE18XEBP and ICE18XEBP20 emulators.
SWICE18XECKIT(1) (DOS)	Intel Windowed Human Interface for ICE18XECQ emulator.
SWICE18XDIAG(1) (DOS)	Emulator Confidence Tests for ALL ICE-18 and UP18x products. Supports all Emulator Control Units.

Note 1: Available as S/T update only. Call 1-800-874-6835.

Adapters	Emulator Support	Description
ICEXEBONCE	ICE18XEBP ICE18XEBP20	84-pin PLCC ONCE adapter for On-Circuit Emulation.
ICEXEAXLONCE	ICE18XEAXLP ICE18XEAXL20	68-pin PLCC ONCE adapter for On-Circuit Emulation.
ICEXLCC	ICE18XEAXLP ICE18XEAXLP20	Adapter to convert probe from 68-pin PLCC to 68-pin LCC.
ICEXPGA	ICE18XEAXLP ICE18XEAXLP20	Adapter to convert probe from 68-pin PLCC to 68-pin PGA.
I18XEBCONV80Q	ICE18XEAXLP ICE18XEAXLP20	Conversion kit to convert probe from 84-pin PLCC to 80-pin QFP.
I18XXLCONV80Q	ICE18XEAXLP ICE18XEAXLP20	Conversion kit to convert probe from 84-pin PLCC to 68-pin PLCC to 80-pin QFP.
I18XECCONV100PQ	ICE18XECQ	Conversion kit to convert probe from 100-pin QFP to 100-pin PQFP.
QI18XXLCONV80Q	ICE18XEAXL	EA 80-QFP to XL 80-QFP conversion kits.

80C86/80C186 SOFTWARE DEVELOPMENT TOOLS



280809-1

Intel supports application development for the 80C86/80C186 family of microprocessors* with a complete set of development languages and utilities. Intel software tools generate fast and efficient code and are designed to give maximum control over the processor. Most importantly they can decrease the design time of an embedded system and accelerate your product's time-to-market.

FEATURES

- Macro assembler for high-performance code
- ANSI C compiler with numerous processor-specific extensions.
- PL/M compiler for high-level language programs with support for many low-level hardware functions
- Linker to link Intel-generated compiler and assembler modules together
- Locator to generate files with absolute addresses for execution from ROM-based systems
- Windowed, interactive source level debugger that works with all Intel languages
- AEDIT Source Code and text editor
- Library manager for creating and maintaining object module libraries
- Complete 8087/80C187 numeric libraries, including software emulator support
- Object-to-hex conversion utility for EPROM support

*80C86/8088, 80186/80188, 80C186/80C188, 80C186EB/80C188EB, 80C186XL/80C188XL, 80C186EA/80C188EA, 80C186EC/80C188EC, Real Mode 80286, and real mode Intel386™ microprocessors.

August 1992
Order Number: 280809-005

ASM-86 MACRO ASSEMBLER

ASM-86 is used to translate symbolic assembly language source into relocatable object code where utmost speed, small code size and hardware control are critical.

HIGHLIGHTS AND BENEFITS

- Macro facility saves development and maintenance time, since common code sequences need only be developed once.
- Simplified instruction set makes program development easier.
- Saves development time by performing extensive checks on consistent usage of variables and labels. Inconsistencies are detected when the program is assembled, before linking or debugging is started.

iC-86 COMPILER

Intel's iC-86 brings the full power of the C programming language to embedded applications based on the 80C86/80C186 family of microprocessors. iC-86 can also be used to develop real mode programs to be executed on the 80C286 or the Intel386™ microprocessors.

HIGHLIGHTS AND BENEFITS

- Generates compact efficient code — easily loaded into ROM-based systems.
- Highly optimized with four levels of optimization, including a jump optimizer and improved register manipulation via register history.
- Produces ROMable code — can be loaded directly into embedded target systems. Libraries completely ROMable, retargetable, and reentrant.
- Supports small, compact, medium, and large memory segmentation models. Allows memory modules to be mixed using "near" and "far" pointers.
- Extensive debug information, including type information and symbols, increases programming productivity.
- Built-in functions for automatic machine code generation improve compile-time and run-time performance. Eliminates need for in-line assembly code or making calls to assembly functions. Allows registers, I/O ports, interrupts and the numerics chips to be controlled directly in C and not in assembly code.
- ANSI C-conforming. Fully linkable with other Intel 80C86/80C186 languages such as ASM and PL/M. Allows programmers to choose optimal language(s) for application.

PL/M-86 COMPILER

PL/M-86 is a high-level programming language designed to support the software requirements of advanced 16-bit microprocessors. The PL/M language provides both the productivity advantages of a high-level language and access to the low-level hardware features found in the assembly language.

HIGHLIGHTS AND BENEFITS

- Modular and structured programming support. Final applications easier to understand, maintain, and support.
- Includes extensive list of built-in functions, e.g., TYPE CONVERSION functions, STRING manipulations, and functions for interrogating hardware flags.
- Define interrupt handling procedures using the INTERRUPT attribute. Compiler generates code to save and restore all registers for interrupt procedures.
- Compile-time options to increase flexibility of PL/M compiler. Options include four optimization levels, conditional compilation, inclusion of common PL/M source files from disk, symbol cross-referencing, and optional assembly language code in list file.
- Supports seven data types. Allows compiler to perform signed, unsigned, and floating-point arithmetic.
- Object modules compatible with all other object modules generated by Intel 80C86/80C186 languages.

LINK-86 TOOLS

Link-86 combines multiple object modules into a single program and resolve references between independently compiled modules. Both tools can increase productivity by enabling the user to use modular programming, making applications easier to design, test, and maintain.

HIGHLIGHTS AND BENEFITS

- Incremental linking allows new modules to be easily added to existing software.
- Final linked module can be either a bound load-time- locatable module or a relocatable module.
- .EXE option allows modules to be generated that can be executed directly in a DOS system.
- Standard modules can be reused in different applications, decreasing software development time.

LOC-86 TOOLS

The LOC-86 tool converts relocatable 80C86/ 80C186 object modules into absolute object modules. Both will allow you to assign addresses.

HIGHLIGHTS AND BENEFITS

- Default address assignment algorithm automatically assigns absolute addresses to object modules prior to loading code into target system. Frees user from concern regarding the final arrangement of the object code in memory.
- User has ability to override the control and specify absolute addresses for various Segments, Classes, and Groups in memory.
- User can reserve various parts of memory.
- Simplifies set up of bootstrap loader and initialization code for ROM-based systems. Very important and beneficial for embedded application development.
- Optional print file containing diagnostic information helpful in debugging may be generated.

LIB-86 TOOLS

Both Lib-86 creates and maintains libraries of software object modules. Standard modules can be placed in a library and linked to your application using the LINK-86 tool.

OH-86 OBJECT-TO-HEXADECIMAL CONVERTER

The OH-86 utiltity converts Intel 80C86/186 object modules into standard hexadecimal format, allowing the code to be loaded directly into PROM using industry standard PROM programmers.

NUMERICS SUPPORT LIBRARIES

The 8027/80C187 numerics libraries fully support the 8087 and 80C187 math coprocessors, with or without the math coprocessor in the final system; numeric functions may be processed by the math coprocessor or by the corresponding software emulator.

Numerics Software Emulator

- For applications without a math coprocessor
- Executes instructions as though coprocessor present; functionality identical to math coprocessor.
- Ideal for prototyping and debugging floating point application code independent of hardware; supports portable code.

Numerics Support Library

- For applications with a math coprocessor
- Provide Intel ASM, C, PL/M, and FORTRAN users with enhanced numeric data processing capability; easy to do floating point math.

HIGHLIGHTS AND BENEFITS

- 4 functionally distinct libraries support floating point operations.
  - Common elementary function library: algebraic, logarithmic, exponential, trignometric and hyperbolic operations on real and complex numbers. Real-to-integer conversions
  - Initialization library: Set up the numerics processing environment (math coprocessor or software emulator).
  - Decimal conversion library: Converts floating point numbers from one binary storage format to another, from ASCII decimal strings to binary floating point format, or vise- versa.
  - Error handling library: Simplifies coding numerics exception handlers.
- All support library modules in OMF-86 format; can be linked with object output of any Intel language.
- All library routines reentrant and ROMable.
- Meets industry standard (ANSI/IEEE standard for binary floating point arithmetic, 754-1985)

DB-86 SOURCE LEVEL DEBUGGER

DB-86 is a DOS-hosted, high-level source code debugger for programs written in C, PL/M, FORTRAN, and Pascal. Its powerful, source-oriented interface allows users to focus their efforts on finding bugs, not learning how to use the debug environment.

HIGHLIGHTS AND FEATURES

- Drop-down menus and on-line help decrease learning time for beginning users.
- Watch windows, conditional breakpoints, trace points and fixed and temporary breakpoints can be set and modified as needed.
- Browse Source and Call Stack, review processor registers, observe watch window variables — all accessed via a pull down menu or single keystroke.
- Uses extensive debug information available in Intel languages to display program variables in their respective type formats.
- Provides support for overlayed programs and the math coprocessors.

intel

AEDIT SOURCE CODE AND TEXT EDITOR

Aedit is a full-screen text editing system designed specifically for software engineers and technical writers. The output file is the pure ASCII text (or HEX code) you input — no special characters or proprietary formats. Its numerous features and advanced capabilities make it an excellent tool to support the 80C86/80C186 development environment.

HIGHLIGHTS AND BENEFITS

- Complete range of editing support—from document processing to HEX code entry and modification
- Supports system escape for quick execution of PC-DOS System level commands
- Full macro support for complex or repetitive editing tasks
- Supports multiple operating systems including DOS and iRMX
- Dual file support with optional split-screen windowing
- No limit to file size or line length
- Quick response with an easy to use menu driven interface
- Configurable and extensible for complete control of the editing process.

WORLDWIDE SERVICE, SUPPORT, AND TRAINING

To augment its development tools, Intel offers a full array of seminars, classes, and workshops, field application engineering expertise, hotline technical support and on-site service.

Intel also offers a Software Support package which includes technical software information, telephone support, automatic distribution of software and documentation updates, access to the "Tooltalk" electronic bulletin board. "iComments" publication, remote diagnostic software, and a development tools troubleshooting guide.

Intel's Hardware Support package includes technical hardware information, telephone support, warranty on parts, labor, material, and on-site hardware support.

SUMMARY

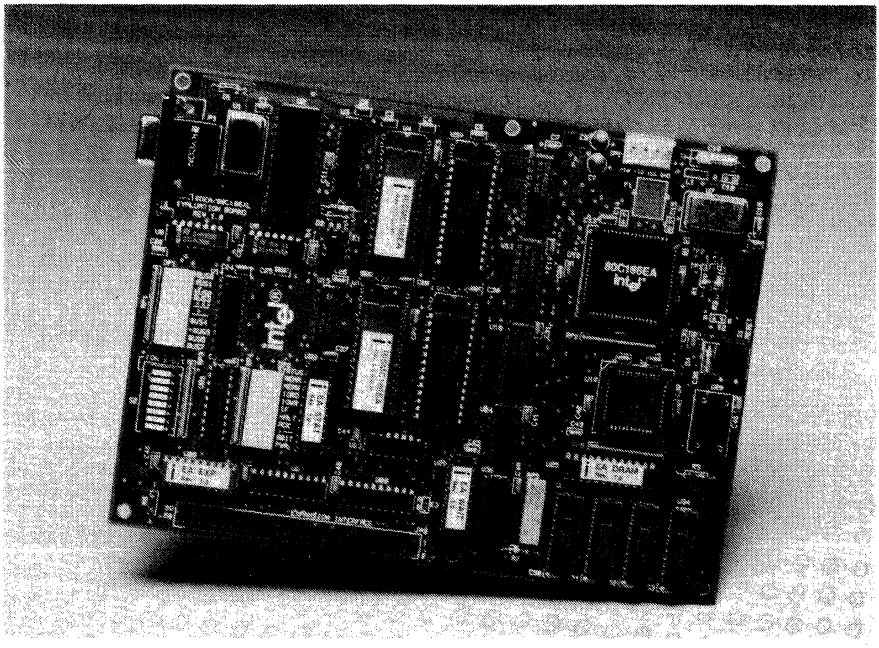
Intel provides a complete software development toolset that delivers full access to the 80C86/80C186 microprocessors. The development tools are easy to use, yet powerful, with productivity boosting features such as source-level symbolic debugging and an up-to-date user interface. Each tool is designed to help you move quickly your application from the lab to the market.

ORDERING INFORMATION

80C86/80C186

D86ASM86KIT	ASM-86	Assember for PC XT or AT system (or compatible) running DOS 3.0 or higher
D86C86NL	iC-86	Software Package for IBM PC XT/AT running PC DOS 3.0 or higher
D86PLM86NL	PL/M-86	Software Package for IBM PC XT/AT running PC DOS 3.0 or higher
D86EDNL	AEDIT	AEDIT Source Code Editor for IBM PC XT/AT running PC DOS 3.0 or higher

EV80C186EA/XL Evaluation Board



272049-01

Low Cost Code Evaluation Tool

Intel's EV80C186EA/XL evaluation board provides a hardware environment for code execution and software debugging. The board features the 80C186EA CHMOS*, 16-bit embedded microprocessor and the necessary peripheral logic to allow you to take full advantage of the —EA and —XL. Powerdown and Idle Modes are a key feature of the 80C186EA/C188EA for those 186 designs which are power consumption sensitive. The 80C186XL/C188XL device is an extension of the highly successful 80C186/C188 device with the added capabilities of a static, low power design and maximum 20 MHz operation. The EV80C186EA/XL provides 20 MHz execution of your code using one wait state. Plus, it can be quickly configured for an 80C188EA, 80C186XL or 80C188XL.

Popular features such as single-step program execution and sixteen software breakpoints are standard on the EV80C186EA/XL. Intel provides a complete code development environment using assembler (ASM-86) as well as high-level languages such as Intel's iC-86, FORTRAN-86, Pascal-86 or PL/M-86 to accelerate your development schedules.

The evaluation board is hosted on an IBM PC* or BIOS-compatible computer. The source code for the on-board monitor (written in ASM-86) is public domain. The program is about 2K, and can be modified to be included in your target hardware. In this way, the provided PC host software can be used throughout the development phase. In addition, there are retargetable debuggers available from Third Party vendors to further enhance your debug process.

*CHMOS is a patented Intel process.
**IBM PC, XT, AT and DOS are registered trademarks of International Business Machines Corporation.

September 1991
Order Number: 272049-001

EV80C186EA/XL Evaluation Board

EV80C186EA/XL Features

- 20 MHz, One Wait State Execution Speed
- 32 Kbytes of SRAM/ROMsim (Expandable)
- 512 Kbytes of DRAM
- All-CMOS Board for Low Power
- Supports Intel Flash Memory
- Sixteen Software Breakpoints
- Two Single-Step Modes
- RS-232C Communication Link
- Concurrent Interrogation of Memory and Registers
- Easily Re-configured to Support 80C188EA, 80C186XL, 80C188XL
- High-Level Language Support

Full Speed Execution

The EV80C186EA/XL executes your code from on-board ROMsim at 20 MHz with one wait state. By changing oscillators on the evaluation board, any execution speed up to 20 MHz can be evaluated. The board's host interface baud rate is not affected by this frequency change.

32 Kbytes of ROMsim

The board comes with 32 Kbytes of SRAM to be used as ROMsim for your code and for data memory as needed. The SRAM sockets support up to 128 Kbytes of SRAM.

512 Kbytes of DRAM

The EV80C186EA/XL comes with 512 Kbytes of DRAM; the necessary control logic is already there. The monitor utilizes the Refresh Control Unit and will set up the DRAM refresh controller for you.

Supports Intel Flash Memory

The EPROM sockets optionally accommodate 128 Kbytes of Flash Memory. The EV80C186EA/XL provides switched V_{PP} for program and erase cycles.

Totally CMOS Board

The EV80C186EA/XL board is built totally with CMOS components, including programmable logic devices. Its power consumption is therefore low, requiring 5V at 400 mA. The board also requires ±12V at 100 mA.

Concurrent Interrogation of Memory and Registers

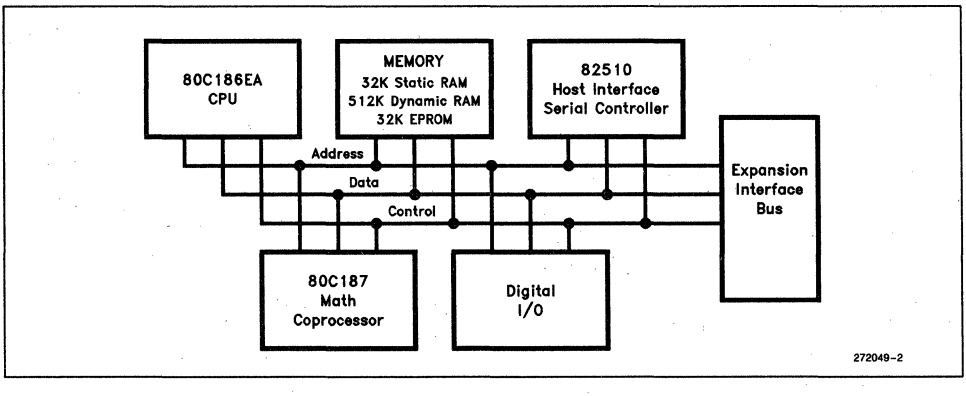
The monitor for the EV80C186EA/XL allows you to read and modify external memory and read internal registers while your code is running in the board. You may only modify internal registers while your code is halted.

Sixteen Software Breakpoints

There are sixteen breakpoints available which automatically subsitute an INT3 instruction for your code instruction at the breakpoint location. The substitution occurs when execution is started. If the processor is halted or a breakpoint is reached, your code is restored in the ROMsim.

Two Step Modes

There are two single-step modes available. The first stepping mode uses the Trap Flag feature of the X86 architecture. The second mode also uses the Trap Flag except for subroutine calls which are treated as one indivisible instruction by placing an INT3 after them.



EV80C186EA/XL Evaluation Board

High-Level Language Support

The host software for the EV80C186EA/XL board is able to load absolute object code generated by ASM-86, iC-86, FORTRAN-86, Pascal-86 or PL/M-86, all of which are available from Intel.

RS-232C Communication Link

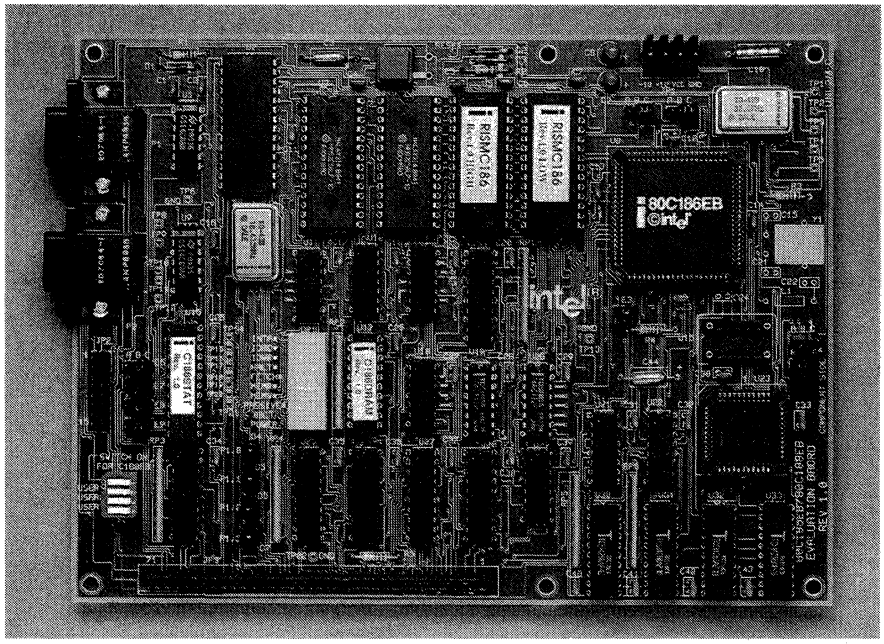
The EV80C186EA/XL communicates with the host using an Intel 82510 Asynchronous Serial Controller provided on board.

Personal Computer Requirements

The EV80C186EA/XL Evaluation Board is hosted on an IBM PC, XT, AT* or BIOS-compatible personal computer. The PC must meet the following minimum requirements:

- 512 Kbytes of Memory
- A Serial Port (COM1 or COM2) at 9600 Baud
- One 360 Kbyte Floppy Disk Drive
- ASM-86, iC-86, FORTRAN-86, Pascal 86 or PL/M-86
- PC DOS 3.1 or Later
- A text editor such as AEDIT

EV80C186EB Evaluation Board



270882-1

Low Cost Code Evaluation Tool

Intel's EV80C186EB evaluation board provides a hardware environment for code execution and software debugging at a relatively low cost. The board features the 80C186EB CHMOS*, 16-bit embedded processor, a new member of the industry standard 80186 family. The 80C186EB features two independent serial channels providing a serial link for easy interprocessor communications, diagnostic and modem interfacing for today's "Mobile Office." This static design also features power management modes for power consumption sensitive designs. The board allows you to take full advantage of the power of the 80186 family. The EV80C186EB provides zero wait state, 16 MHz execution of your code. Plus, it can be quickly reconfigured to use an 80C188EB, allowing for exact analysis of code execution speeds in a particular application.

Popular features such as single-step program execution and sixteen software breakpoints are standard on the EV80C186EB. Intel provides a complete code development environment using assembler (ASM-86) as well as high-level languages such as Intel's iC-86, FORTRAN-86, Pascal-86 or PL/M-86 to accelerate development schedules.

The evaluation board is hosted on an IBM PC** or BIOS-compatible computer. The source code for the on-board monitor (written in ASM-86) is public domain. The program is about 2K, and can be modified to be included in your target hardware. In this way, the provided PC host software can be used throughout the development phase. In addition, there are retargetable debuggers available from Third Party vendors to further enhance your debug process.

*CHMOS is a patented Intel process.
**IBM PC, XT, AT and DOS are registered trademarks of International Business Machines Corporation.

October 1991
Order Number: 270882-003

EV80C186EB Evaluation Board

EV80C186EB Features

- Zero Wait State 16.0 MHz Execution Speed
- 32 Kbytes of SRAM/ROMsim
- 512 Kbytes of DRAM
- All-CMOS board for Low Power
- Concurrent Interrogation of Memory and Registers
- Sixteen Software Breakpoints
- Two Single-Step Modes
- High-Level Language Support
- RS-232C Communication Link
- Easily Re-configured to Support 80C188EB

Full Speed Execution

The EV80C186EB executes your code from on-board ROMsim at 16.0 MHz with zero wait states. By changing oscillators on the EV80C186EB, any execution speed up to 16 MHz can be evaluated. The board's host interface baud rate is not affected by this frequency change.

32 Kbytes of ROMsim

The board comes with 32 Kbytes of SRAM to be used as ROMsim for your code and for data memory as needed.

512 Kbytes of DRAM

The EV80C186EB comes with 512 Kbytes of DRAM; the necessary control logic is already there. The monitor utilizes the Refresh Control Unit and will set up the DRAM refresh controller for you.

Totally CMOS Board

The EV80C186EB board is built totally with CMOS components. Its power consumption is therefore low, requiring 5V at 400 mA. The board also requires ±12V at 15 mA.

Concurrent Interrogation of Memory and Registers

The monitor for the EV80C186EB allows you to read and modify external memory and read internal registers while your code is running in the board. You may only modify internal registers while your code is halted.

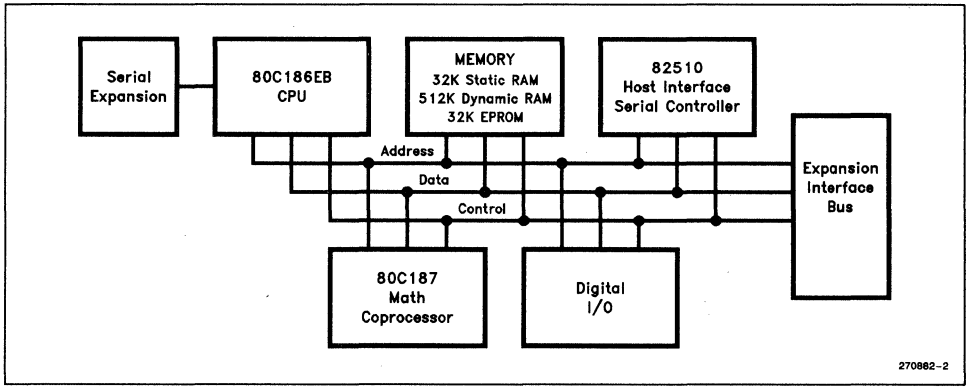
Sixteen Software Breakpoints

There are sixteen breakpoints available which automatically substitute an INT3 instruction for your code instruction at the breakpoint location. The substitution occurs when execution is started. If processor is halted or a breakpoint is reached, your code is restored in the ROMsim.

Two Step Modes

There are two single-step modes available. The first stepping mode uses the Trap Flag feature of the X86 architecture.

The second mode also uses the Trap Flag except for subroutine calls which are treated as one indivisible instruction by placing an INT3 after them.



EV80C186EB Evaluation Board

High-Level Language Support

The host software for the EV80C186EB board is able to load absolute object code generated by ASM-86, iC86, FORTRAN-86, Pascal-86 or PL/M-86, all of which are available from Intel.

RS-232C Communication Link

The EV80C186EB communicates with the host using an Intel 82510 Asynchronous Serial Controller provided on board.

Personal Computer Requirements

The EV80C186EB Evaluation Board is hosted on an IBM PC XT, AT** or BIOS-compatible personal computer. The PC must meet the following minimum requirements:

- 512 Kbytes of Memory
- One 360 Kbyte Floppy Disk Drive
- PC DOS 3.1 or Later
- A Serial Port (COM1 or COM2) at 9600 Baud
- ASM-86, iC-86, FORTRAN-86, Pascal-86 or PL/M-86
- A text editor such as AEDIT

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EV80C186EC Evaluation Board

Low Cost Code Evaluation Tool

Intel's EV80C186EC evaluation board provides a hardware environment for code execution and software debugging. The board features the 80C186EC CHMOS*, 16-bit embedded microprocessor and all necessary memory and peripheral logic. The 80C186EC is the highest integration member of the highly successful 80C186/C188 family of embedded microprocessors. The EV80C186EC evaluation board provides 16 MHz, zero wait state, execution of your code. A dip switch configures the EV80C186EC for use with the 80C188EC for applications requiring an 8-bit data bus.

Popular features such as single-step program execution and software breakpoints are standard on the EV80C186EC. Intel provides a complete code development environment including ASM-86, iC-86, FORTRAN-86, Pascal-86 and PL/M-86.

The evaluation board is hosted on an IBM PC** or compatible computer. The source code for the on-board monitor (written in ASM-86) is public domain. The program is about 2 Kbytes in length and can be modified for inclusion in your target hardware. In addition, there are retargetable debuggers available from third party vendors to further enhance your development process.

EV80C186EC Features

- 16 MHz, Zero Wait State Execution Speed
- 64 Kbytes of SRAM (Expandable)
- 512 Kbytes of DRAM
- All-CMOS Board for Low Power
- Supports Intel Flash Memory
- Sixteen Software Breakpoints
- Two Single-Step Modes
- RS-232C Communications Link
- Concurrent Interrogation of Memory and Registers
- Easily Reconfigurable to Support 80C188EC
- High-Level Language Support

Full Speed Execution

The EV80C186EC executes your code from the on-board RAM at 16 MHz with no wait states. By changing oscillators on the evaluation board, any execution speed up to 16 MHz can be evaluated. The boards host interface rate is independent of CPU frequency.

32 Kbytes of SRAM

The EV80C186EC comes with 64 Kbytes of SRAM for your code and data. The SRAM sockets will accept up to 128 Kbyte SRAMs when expansion is necesary.

512 Kbytes of DRAM

The EV80C186EC comes with 512 Kbytes of DRAM; the necessary control logic is already there. The monitor uses the on-chip Refresh Control Unit and sets up the DRAM controller automatically.

Supports Intel Flash Memory

The EPROM sockets optionally accommodate the 28F001BX-T 128 Kbyte Flash Memory. The EV80C186EC provides an on-board V_{PP} switching circuit and built in programming procedures.

Totally CMOS Board

The EV80C186EC is built entirely with CMOS components, including programmable logic devices. Its power consumption is therefore low, requiring 5V at 500 mA. The board also requires ±12V at 100 mA.

Concurrent Interrogation of Memory and Registers

The monitor for the EV80C186EA/XL allows you to read and modify external memory and read internal registers while your code is running on the board. You may only modify internal registers while your code is halted.

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September 1991
Order Number: 272083-001

Sixteen Software Breakpoints

There are sixteen breakpoints available which automatically substitute an INT3 instruction for your code instruction at the breakpoint location. The substitution occurs when execution is started. If the processor is halted or a breakpoint is reached, your code is restored in the RAM.

Two Step Modes

There are two single-step modes available. The first stepping mode uses the Trap Flag feature of the X86 architecture. The second mode also uses the Trap Flag except for subroutine calls which are treated as one indivisible instruction by placing an INT3 after them.

High-Level Language Support

The host software for the EV80C186EA/XL board is able to load absolute object code generated by ASM-96, iC-86, FORTRAN-86, Pascal-86 or PL/M-86, all of which are available from Intel.

RS-232C Communication Link

The EV80C186EA/XL communicates with the host using an Intel 82510 Asynchronous Serial Controller provided on board.

Personal Computer Requirements

The EV80C186EC Evaluation Board is hosted on an IBM, PC, XT, AT** or compatible personal computer. The PC must meet the minimum requirements:

—512 Kbytes of Memory

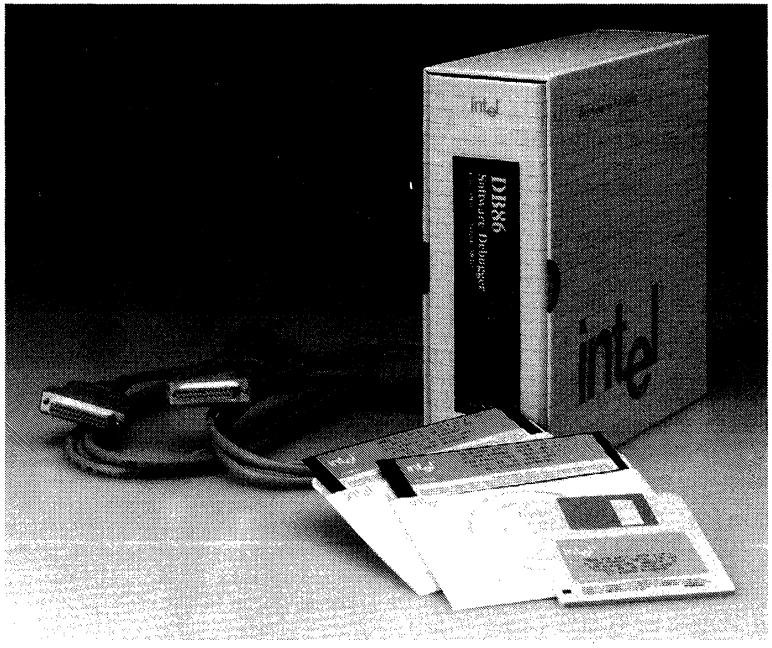
—A Serial Port (COM1 and COM2) at 9600 Baud

—One 360 Kbyte Floppy Disk Drive

—ASM-86, iC-86, FORTRAN-86, Pascal-86 or PL/M-86

—PC DOS** 3.1 or Later

DB86A ARTIC SOFTWARE DEBUGGER



280914-1

Multitasking Source Level Debugger

The DB86A ARTIC debugger from Intel is a powerful source-level debugger designed to support the development of multitasking applications targeted to run on the full family of IBM* ARTIC cards. The DB86A ARTIC debugger is hosted on an IBM PC/AT*, PS/2* or compatible computer running DOS or OS/2* (DOS compatibility box only). Using an RS232 link to an IBM ARTIC card, the debugger contains control and monitoring capabilities for on-target software debugging. The DB86A debugger delivers an optimum debugging environment for application code generated by IBM C/2*, IBM MASM/2*, Microsoft C*, and Microsoft MASM*.

The DB86A debugger features a contemporary windowed human interface, symbolic source level debug, tasking controls, extensive breakpoint modes, and flexible stepping capabilities. This multitasking debug environment boosts productivitiy by allowing you to focus efforts on finding bugs more quickly, and reducing time-to-market.

DB86A Debugger Features

- Menu-driven Windowed Human Interface
- Source Level Debug with various Source Window and Watch Window Operations
- Multitasking Debug Support
- High-level and Assembly Language Symbolic Debugging
- Extensive Breakpoint and Stepping Capabilities
- Powerful Procedural Command Language
- On-line Help Facility
- Built-in Assembler and Disassembler
- Memory and Register Manipulations
- Intel Service and Support

August 1992
Order Number: 280927-002

intel.

FEATURES

Windowed Human Interface

The DB86A Artic Debugger offers a windowed user interface that is easy for both experienced and new users.

Pull-down menus provide a set of commonly used debug operations, shortening learning curves. Many debugging functions can be executed with a single key stroke. Custom debug commands and the command line interface offer experienced users increased efficiency. Multiple windows simultaneously display source code, watch variables, and registers. Source breakpoints support the point-and-shoot technique of debugging, or breakpoints can be easily set through the source window. When the debugger completes a breakpoint or stepping operation, the various windows are updated. The watch window can track up to six program variables. The on-line help facility provides command syntax and explanation as well as error descriptions.

Event Monitor Capability

DB86A provides many ways to monitor events. There are four conditional breakpoints, ten source breakpoints, ten temporary breakpoints, and ten passpoints. Each type of breakpoint meets different debugging needs. The stepping commands not only allow execution of one machine-level instruction or one high-level language statement at a time, they also permit stepping over or stepping through a procedure until it returns.

Procedural Command Language

The command language of the DB86A debugger provides control constructs, procedures, and debug variables allowing the user to extend and customize the functionality of the debugger. Control constructs (e.g. If...else, do...while) facilitate the grouping of a sequence of debugger commands and control the execution of the sequence. For debug sequences that are repeated frequently, the user can define debug procedures containing a sequence of debugger commands, control constructs, and debug variables. DB86A debugger comes with a set of predefined debug procedures that display various ARTIC system data structures such as interface blocks, task tables, and task control block tables.

Multitasking Debug Support

The DB86A debugger delivers control and monitor capabilities to simplify multitasking debug. You can download multiple tasks to the target system, and easily select any task for viewing and debugging.

Corresponding windows are automatically updated when a task hits a breakpoint. Tasks can be suspended and resumed. Breakpoints can be set for all, or for specific tasks. Qualifiers are provided with the debugger commands to facilitate multitasking debug.

Symbolic Debug Capabilities

The debugger makes full use of the symbolic and typing information passed by the code translators. Source code symbolics are enabled in debugging operations and displays. The debugger supports easy browsing through modules in each task. The Callstack feature creates a snapshot of the active call chain, and call stack browsing lets you navigate through the source code of the procedure call chain. Task memory and registers can be displayed and modified easily. An on-line assembler is provided for in-target code patching.

Worldwide Service, Support, and Training

To augment its development tools, Intel offers field application engineering expertise, hotline technical support, and on-site service.

Intel also offers software support which includes technical software information, telephone support, automatic distributions of software and documentation updates, *iCOMMENTS* magazine, remote diagnostic software, and a development tools troubleshooting guide.

Intel Development Tools also offers a 30-day, money-back guarantee to customers who are not satisfied after purchasing any Intel development tool.

SPECIFICATIONS

Host System Requirements

IBM PC/AT or IBM PS/2 or fully compatible computers with the following minimum configurations:

- Minimum of 900Kbytes free hard disk space for DB86A
- 640Kbytes of RAM recommended; DB86A uses a minimum of 360Kbytes of RAM
- A serial port (COM1 or COM2)
- DOS V3.3 or later, OS/2 V1.2 (DOS Compatibility Box Only)
- One floppy drive capable of reading 5.25" diskettes or 3.5" diskettes

Target System Requirements

- One ARTIC RS232 serial port
- 8 Kbytes free RAM on the target ARTIC Board for DB86A debug support task
- Target system containing one of the following ARTIC cards:
  IBM Realtime Interface Coprocessor
  IBM Realtime Interface Coprocessor Multiport
  IBM Realtime Interface Coprocessor Multiport Model 2
  IBM X.25 Interface Coprocessor/2
  IBM Realtime Interface Coprocessor Multiport/2
  IBM Realtime Interface Coprocessor Portmaster/A

i376™ Processor and Peripherals Data Sheets

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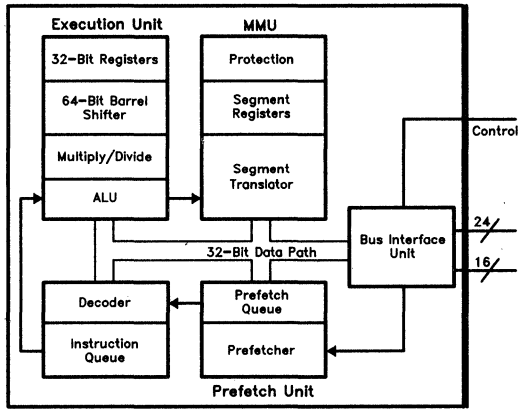
376™ HIGH PERFORMANCE 32-BIT EMBEDDED PROCESSOR

- **Full 32-Bit Internal Architecture**
  - **— 8-, 16-, 32-Bit Data Types**
  - **— 8 General Purpose 32-Bit Registers**
  - **— Extensive 32-Bit Instruction Set**
- **High Performance 16-Bit Data Bus**
  - **— 16 or 20 MHz CPU Clock**
  - **— Two-Clock Bus Cycles**
  - **— 16 Mbytes/Sec Bus Bandwidth**
- **16 Mbyte Physical Memory Size**
- **High Speed Numerics Support with the 80387SX**
- **Low System Cost with the 82370 Integrated System Peripheral**
- **On-Chip Debugging Support Including Break Point Registers**
- **Complete Intel Development Support**
  - **— C, PL/M, Assembler**
  - **— ICE™-376, In-Circuit Emulator**
  - **— iRMK™ Real Time Kernel**
  - **— iSDM™ Debug Monitor**
  - **— DOS Based Debug**
- **Extensive Third-Party Support:**
  - **— Languages: C, Pascal, FORTRAN, BASIC and ADA***
  - **— Hosts: VMS*, UNIX*, MS-DOS*, and Others**
  - **— Real-Time Kernels**
- **High Speed CHMOS IV Technology**
- **Available in 100 Pin Plastic Quad Flat-Pack Package and 88-Pin Pin Grid Array**
  (See Packaging Outlines and Dimensions #231369)

INTRODUCTION

The 376 32-bit embedded processor is designed for high performance embedded systems. It provides the performance benefits of a highly pipelined 32-bit internal architecture with the low system cost associated with 16-bit hardware systems. The 80376 processor is based on the 80386 and offers a high degree of compatibility with the 80386. All 80386 32-bit programs not dependent on paging can be executed on the 80376 and all 80376 programs can be executed on the 80386. All 32-bit 80386 language translators can be used for software development. With proper support software, any 80386-based computer can be used to develop and test 80376 programs. In addition, any 80386-based PC-AT* compatible computer can be used for hardware prototyping for designs based on the 80376 and its companion product the 82370.



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80376 Microarchitecture

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1.0 PIN DESCRIPTION

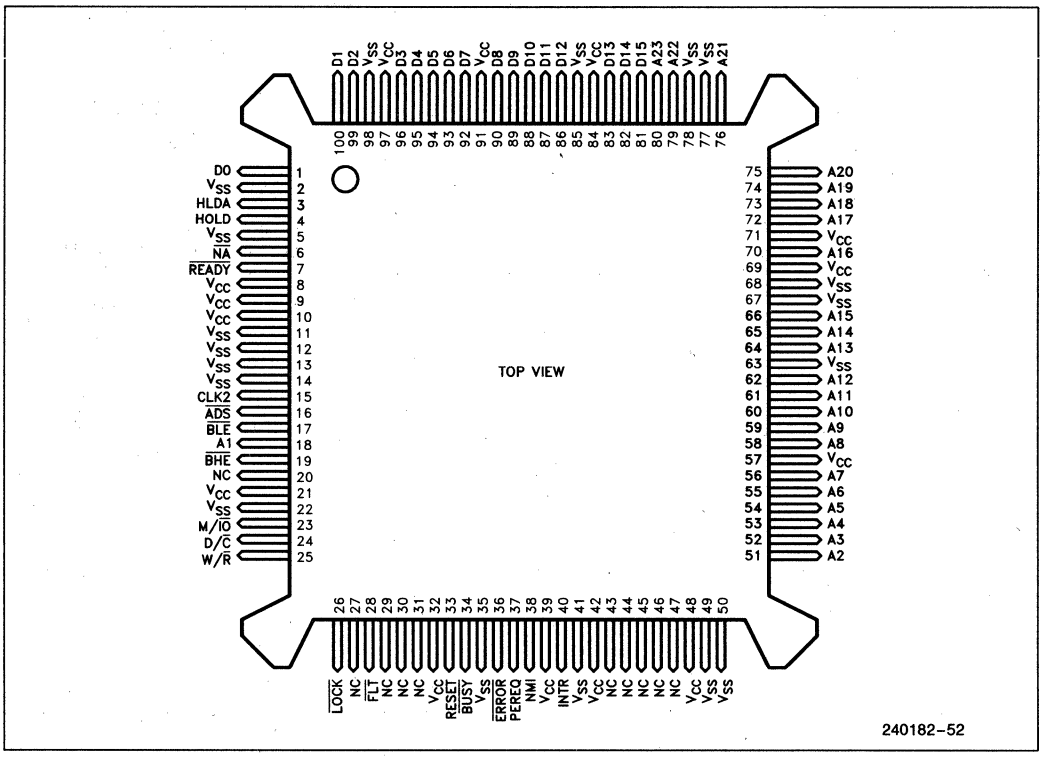

Figure 1.1. 80376 100-Pin Quad Flat-Pack Pin Out (Top View)

Table 1.1. 100-Pin Plastic Quad Flat-Pack Pin Assignments

Address		Data		Control		N/C	V_{CC}	V_{SS}
A_1	18	D_0	1	$\overline{ADS}$	16	20	8	2
A_2	51	D_1	100	$\overline{BHE}$	19	27	9	5
A_3	52	D_2	99	$\overline{BLE}$	17		10	11
A_4	53	D_3	96	$\overline{BUSY}$	34	29	21	12
A_5	54	D_4	95	CLK2	15	30	32	13
A_6	55	D_5	94	D/$\overline{C}$	24	31	39	14
A_7	56	D_6	93	$\overline{ERROR}$	36	43	42	22
A_8	58	D_7	92	$\overline{FLT}$	28	44	48	35
A_9	59	D_8	90	HLDA	3	45	57	41
A_{10}	60	D_9	89	HOLD	4	46	69	49
A_{11}	61	D_{10}	88	INTR	40	47	71	50
A_{12}	62	D_{11}	87	$\overline{LOCK}$	26		84	63
A_{13}	64	D_{12}	86	M/$\overline{IO}$	23		91	67
A_{14}	65	D_{13}	83	$\overline{NA}$	6		97	68
A_{15}	66	D_{14}	82	NMI	38			77
A_{16}	70	D_{15}	81	PEREQ	37			78
A_{17}	72			$\overline{READY}$	7			85
A_{18}	73			$\overline{RESET}$	33			88
A_{19}	74			W/$\overline{R}$	25			
A_{20}	75							
A_{21}	76							
A_{22}	79							
A_{23}	80							

Top View
(Component Side)

	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	V_{CC}	V_{SS}	N/C	A1	$\overline{ADS}$	$\overline{READY}$	HOLD	D0	D2	V_{SS}	V_{CC}	V_{SS}	V_{CC}	1
2	V_{SS}	V_{CC}	M/$\overline{IO}$	$\overline{BHE}$	$\overline{BLE}$	CLK2	$\overline{NA}$	HLDA	D1	D3	V_{SS}	V_{CC}	V_{SS}	2
3	V_{CC}	D/$\overline{C}$										D4	V_{CC}	3
4	V_{SS}	W/$\overline{R}$										D6	D5	4
5	V_{CC}	$\overline{LOCK}$										D7	D8	5
6	V_{SS}	RESET										D9	D10	6
7	PEREQ	$\overline{BUSY}$										D11	D12	7
8	$\overline{ERROR}$	NMI										D13	D14	8
9	V_{SS}	INTR										D15	A23	9
10	V_{CC}	A2										A21	A22	10
11	V_{SS}	A3										V_{SS}	V_{CC}	11
12	V_{SS}	A4	A5	A7	A8	A10	A13	A15	A17	A18	A20	V_{CC}	V_{SS}	12
13	V_{CC}	V_{SS}	V_{CC}	A6	A9	A11	A12	A14	A16	A19	V_{CC}	V_{SS}	V_{CC}	13
	N	M	L	K	J	H	G	F	E	D	C	B	A	

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Bottom View
(Pin Side)

	A	B	C	D	E	F	G	H	J	K	L	M	N	
01	V_{CC}	V_{SS}	V_{CC}	V_{SS}	D_2	D_0	HOLD	$\overline{READY}$	$\overline{ADS}$	A_1	N/C	V_{SS}	V_{CC}	01
02	V_{SS}	V_{CC}	V_{SS}	D_3	D_1	HLDA	$\overline{NA}$	CLK2	$\overline{BLE}$	$\overline{BHE}$	M/$\overline{IO}$	V_{CC}	V_{SS}	02
03	V_{CC}	D_4										D/$\overline{C}$	V_{CC}	03
04	D_5	D_6										W/$\overline{R}$	V_{SS}	04
05	D_8	D_7										$\overline{LOCK}$	V_{CC}	05
06	D_{10}	D_9										RESET	V_{SS}	06
07	D_{12}	D_{11}										$\overline{BUSY}$	PEREQ	07
08	D_{14}	D_{13}										NMI	$\overline{ERROR}$	08
09	A_{23}	D_{15}										INTR	V_{SS}	09
10	A_{22}	A_{21}										A_2	V_{CC}	10
11	V_{CC}	V_{SS}										A_3	V_{SS}	11
12	V_{SS}	V_{CC}	A_{20}	A_{18}	A_{17}	A_{15}	A_{13}	A_{10}	A_8	A_7	A_5	A_4	V_{SS}	12
13	V_{CC}	V_{SS}	V_{CC}	A_{19}	A_{16}	A_{14}	A_{12}	A_{11}	A_9	A_6	V_{CC}	V_{SS}	V_{CC}	13
	A	B	C	D	E	F	G	H	J	K	L	M	N	

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Figure 1.2. 80376 88-Pin Grid Array Pin Out

Table 1.2. 88-Pin Grid Array Pin Assignments

Pin	Label	Pin	Label	Pin	Label	Pin	Label
2H	CLK2	12D	A_{18}	2L	M/$\overline{IO}$	11A	V_{CC}
9B	D_{15}	12E	A_{17}	5M	$\overline{LOCK}$	13A	V_{CC}
8A	D_{14}	13E	A_{16}	1J	$\overline{ADS}$	13C	V_{CC}
8B	D_{13}	12F	A_{15}	1H	$\overline{READY}$	13L	V_{CC}
7A	D_{12}	13F	A_{14}	2G	$\overline{NA}$	1N	V_{CC}
7B	D_{11}	12G	A_{13}	1G	HOLD	13N	V_{CC}
6A	D_{10}	13G	A_{12}	2F	HLDA	11B	V_{SS}
6B	D_9	13H	A_{11}	7N	PEREQ	2C	V_{SS}
5A	D_8	12H	A_{10}	7M	$\overline{BUSY}$	1D	V_{SS}
5B	D_7	13J	A_9	8N	$\overline{ERROR}$	1M	V_{SS}
4B	D_6	12J	A_8	9M	INTR	4N	V_{SS}
4A	D_5	12K	A_7	8M	NMI	9N	V_{SS}
3B	D_4	13K	A_6	6M	RESET	11N	V_{SS}
2D	D_3	12L	A_5	2B	V_{CC}	2A	V_{SS}
1E	D_2	12M	A_4	12B	V_{CC}	12A	V_{SS}
2E	D_1	11M	A_3	1C	V_{CC}	1B	V_{SS}
1F	D_0	10M	A_2	2M	V_{CC}	13B	V_{SS}
9A	A_{23}	1K	A_1	3N	V_{CC}	13M	V_{SS}
10A	A_{22}	2J	$\overline{BLE}$	5N	V_{CC}	2N	V_{SS}
10B	A_{21}	2K	$\overline{BHE}$	10N	V_{CC}	6N	V_{SS}
12C	A_{20}	4M	W/$\overline{R}$	1A	V_{CC}	12N	V_{SS}
13D	A_{19}	3M	D/$\overline{C}$	3A	V_{CC}	1L	N/C

The following table lists a brief description of each pin on the 80376. The following definitions are used in these descriptions:

- $\overline{\ }$ The named signal is active LOW.
- I Input signal.
- O Output signal.
- I/O Input and Output signal.
- — No electrical connection.

Symbol	Type	Name and Function
CLK2	I	**CLK2** provides the fundamental timing for the 80376. For additional information see **Clock** in Section 4.1.
RESET	I	**RESET** suspends any operation in progress and places the 80376 in a known reset state. See **Interrupt Signals** in Section 4.1 for additional information.
D_{15}–D_0	I/O	**DATA BUS** inputs data during memory, I/O and interrupt acknowledge read cycles and outputs data during memory and I/O write cycles. See **Data Bus** in Section 4.1 for additional information.
A_{23}–A_1	O	**ADDRESS BUS** outputs physical memory or port I/O addresses. See **Address Bus** in Section 4.1 for additional information.
W/$\overline{R}$	O	**WRITE/READ** is a bus cycle definition pin that distinguishes write cycles from read cycles. See **Bus Cycle Definition Signals** in Section 4.1 for additional information.
D/$\overline{C}$	O	**DATA/CONTROL** is a bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles which are: interrupt acknowledge, halt, and instruction fetching. See **Bus Cycle Definition Signals** in Section 4.1 for additional information.
M/$\overline{IO}$	O	**MEMORY I/O** is a bus cycle definition pin that distinguishes memory cycles from input/output cycles. See **Bus Cycle Definition Signals** in Section 4.1 for additional information.
$\overline{LOCK}$	O	**BUS LOCK** is a bus cycle definition pin that indicates that other system bus masters are denied access to the system bus while it is active. See **Bus Cycle Definition Signals** in Section 4.1 for additional information.
$\overline{ADS}$	O	**ADDRESS STATUS** indicates that a valid bus cycle definition and address (W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{BHE}$, $\overline{BLE}$ and A_{23}–A_1) are being driven at the 80376 pins. See **Bus Control Signals** in Section 4.1 for additional information.
$\overline{NA}$	I	**NEXT ADDRESS** is used to request address pipelining. See **Bus Control Signals** in Section 4.1 for additional information.
$\overline{READY}$	I	**BUS READY** terminates the bus cycle. See **Bus Control Signals** in Section 4.1 for additional information.
$\overline{BHE}$, $\overline{BLE}$	O	**BYTE ENABLES** indicate which data bytes of the data bus take part in a bus cycle. See **Address Bus** in Section 4.1 for additional information.
HOLD	I	**BUS HOLD REQUEST** input allows another bus master to request control of the local bus. See **Bus Arbitration Signals** in Section 4.1 for additional information.

Symbol	Type	Name and Function
HLDA	O	**BUS HOLD ACKNOWLEDGE** output indicates that the 80376 has surrendered control of its local bus to another bus master. See **Bus Arbitration Signals** in Section 4.1 for additional information.
INTR	I	**INTERRUPT REQUEST** is a maskable input that signals the 80376 to suspend execution of the current program and execute an interrupt acknowledge function. See **Interrupt Signals** in Section 4.1 for additional information.
NMI	I	**NON-MASKABLE INTERRUPT REQUEST** is a non-maskable input that signals the 80376 to suspend execution of the current program and execute an interrupt acknowledge function. See **Interrupt Signals** in Section 4.1 for additional information.
$\overline{BUSY}$	I	**BUSY** signals a busy condition from a processor extension. See **Coprocessor Interface Signals** in Section 4.1 for additional information.
$\overline{ERROR}$	I	**ERROR** signals an error condition from a processor extension. See **Coprocessor Interface Signals** in Section 4.1 for additional information.
PEREQ	I	**PROCESSOR EXTENSION REQUEST** indicates that the processor extension has data to be transferred by the 80376. See **Coprocessor Interface Signals** in Section 4.1 for additional information.
$\overline{FLT}$	I	**FLOAT,** when active, forces all bidirectional and output signals, including HLDA, to the float condition. FLOAT is not available on the PGA package. See **Float** for additional information.
N/C	—	**NO CONNECT** should always remain unconnected. Connection of a N/C pin may cause the processor to malfunction or be incompatible with future steppings of the 80376.
V_{CC}	I	**SYSTEM POWER** provides the +5V nominal D.C. supply input.
V_{SS}	I	**SYSTEM GROUND** provides 0V connection from which all inputs and outputs are measured.

2.0 ARCHITECTURE OVERVIEW

The 80376 supports the protection mechanisms needed by sophisticated multitasking embedded systems and real-time operating systems. The use of these protection mechanisms is completely optional. For embedded applications not needing protection, the 80376 can easily be configured to provide a 16 Mbyte physical address space.

Instruction pipelining, high bus bandwidth, and a very high performance ALU ensure short average instruction execution times and high system throughput. The 80376 is capable of execution at sustained rates of 2.5–3.0 million instructions per second.

The 80376 offers on-chip testability and debugging features. Four break point registers allow conditional or unconditional break point traps on code execution or data accesses for powerful debugging of even ROM based systems. Other testability features include self-test and tri-stating of output buffers during RESET.

The Intel 80376 embedded processor consists of a central processing unit, a memory management unit and a bus interface. The central processing unit consists of the execution unit and instruction unit. The execution unit contains the eight 32-bit general registers which are used for both address calculation and data operations and a 64-bit barrel shifter used to speed shift, rotate, multiply, and divide operations. The instruction unit decodes the instruction opcodes and stores them in the decoded instruction queue for immediate use by the execution unit.

The Memory Management Unit (MMU) consists of a segmentation and protection unit. Segmentation allows the managing of the logical address space by providing an extra addressing component, one that allows easy code and data relocatability, and efficient sharing.

The protection unit provides four levels of protection for isolating and protecting applications and the operating system from each other. The hardware enforced protection allows the design of systems with a high degree of integrity and simplifies debugging.

Finally, to facilitate high performance system hardware designs, the 80376 bus interface offers address pipelining and direct Byte Enable signals for each byte of the data bus.

2.1 Register Set

The 80376 has twenty-nine registers as shown in Figure 2.1. These registers are grouped into the following six categories:

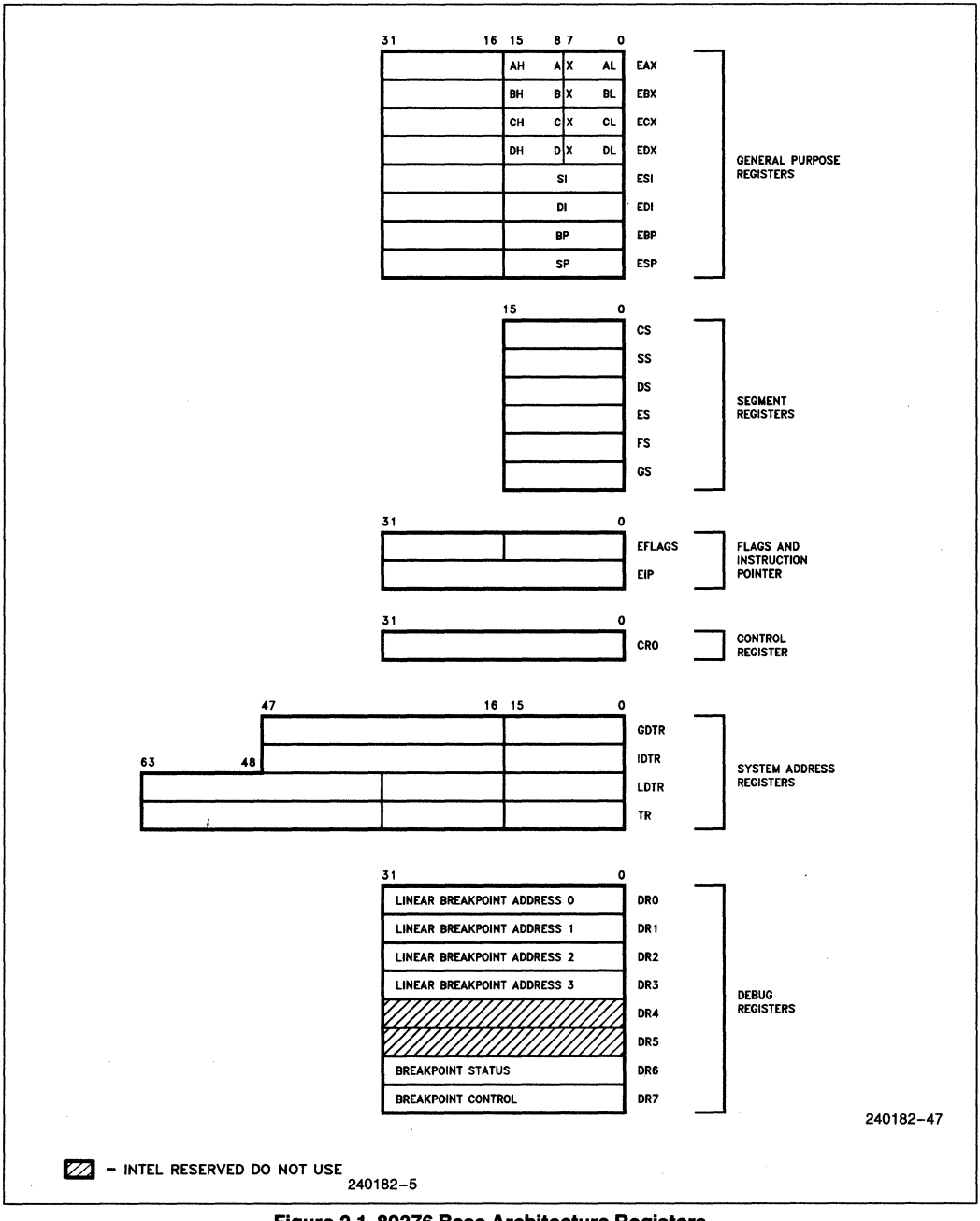

Figure 2.1. 80376 Base Architecture Registers

General Registers: The eight 32-bit general purpose registers are used to contain arithmetic and logical operands. Four of these (EAX, EBX, ECX and EDX) can be used either in their entirety as 32-bit registers, as 16-bit registers, or split into pairs of separate 8-bit registers.

Segment Registers: Six 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data.

Flags and Instruction Pointer Registers: These two 32-bit special purpose registers in Figure 2.1 record or control certain aspects of the 80376 processor state. The EFLAGS register includes status and control bits that are used to reflect the outcome of many instructions and modify the semantics of some instructions. The Instruction Pointer, called EIP, is 32 bits wide. The Instruction Pointer controls instruction fetching and the processor automatically increments it after executing an instruction.

Control Register: The 32-bit control register, CR0, is used to control Coprocessor Emulation.

System Address Registers: These four special registers reference the tables or segments supported by the 80376/80386 protection model. These tables or segments are:

GDTR (Global Descriptor Table Register),
IDTR (Interrupt Descriptor Table Register),
LDTR (Local Descriptor Table Register),
TR (Task State Segment Register).

Debug Registers: The six programmer accessible debug registers provide on-chip support for debugging. The use of the debug registers is described in Section 2.11 **Debugging Support**.

EFLAGS REGISTER

The flag Register is a 32-bit register named EFLAGS. The defined bits and bit fields within EFLAGS, shown in Figure 2.2, control certain operations and indicate the status of the 80376 processor. The function of the flag bits is given in Table 2.1.

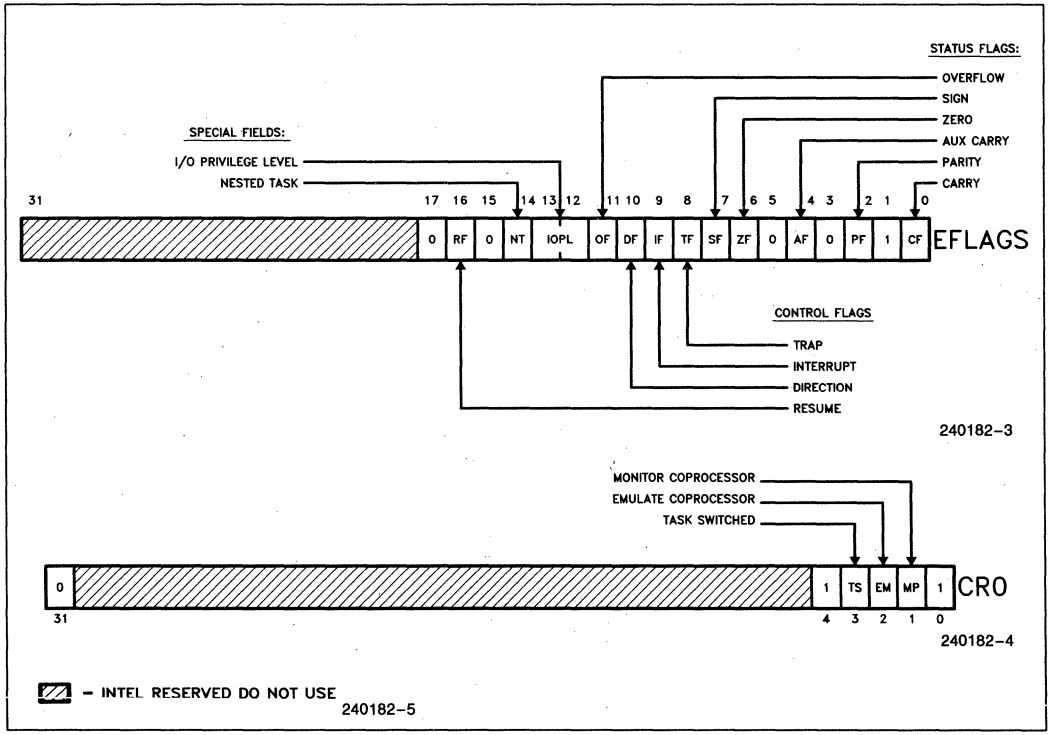

Figure 2.2. Status and Control Register Bit Functions

Table 2.1. Flag Definitions

Bit Position	Name	Function
0	CF	**Carry Flag**—Set on high-order bit carry or borrow; cleared otherwise.
2	PF	**Parity Flag**—Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise.
4	AF	**Auxiliary Carry Flag**—Set on carry from or borrow to the low order four bits of AL; cleared otherwise.
6	ZF	**Zero Flag**—Set if result is zero; cleared otherwise.
7	SF	**Sign Flag**—Set equal to high-order bit of result (0 if positive, 1 if negative).
8	TF	**Single Step Flag**—Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	**Interrupt-Enable Flag**—When set, external interrupts signaled on the INTR pin will cause the CPU to transfer control to an interrupt vector specified location.
10	DF	**Direction Flag**—Causes string instructions to auto-increment (default) the appropriate index registers when cleared. Setting DF causes auto-decrement.
11	OF	**Overflow Flag**—Set if the operation resulted in a carry/borrow into the sign bit (high-order bit) of the result but did not result in a carry/borrow out of the high-order bit or vice-versa.
12, 13	IOPL	**I/O Privilege Level**—Indicates the maximum CPL permitted to execute I/O instructions without generating an exception 13 fault or consulting the I/O permission bit map. It also indicates the maximum CPL value allowing alteration of the IF bit.
14	NT	**Nested Task**—Indicates that the execution of the current task is nested within another task (see **Task Switching**).
16	RF	**Resume Flag**—Used in conjunction with debug register breakpoints. It is checked at instruction boundaries before breakpoint processing. If set, any debug fault is ignored on the next instruction. It is reset at the successful completion of any instruction except IRET, POPF, and those instructions causing task switches.

CONTROL REGISTER

The 80376 has a 32-bit control register called CR0 that is used to control coprocessor emulation. This register is shown in Figures, 2.1 and 2.2. The defined CR0 bits are described in Table 2.2. Bits 0, 4 and 31 of CR0 have fixed values in the 80376. These values cannot be changed. Programs that load CR0 should always load bits 0, 4 and 31 with values previously there to be compatible with the 80386.

Table 2.2. CR0 Definitions

Bit Position	Name	Function
1	MP	**Monitor Coprocessor Extension**—Allows WAIT instructions to cause a processor extension not present exception (number 7).
2	EM	**Emulate Processor Extension**—When set, this bit causes a processor extension not present exception (number 7) on ESC instructions to allow processor extension emulation.
3	TS	**Task Switched**—When set, this bit indicates the next instruction using a processor extension will cause exception 7, allowing software to test whether the current processor extension context belongs to the current task (see **Task Switching**).

2.2 Instruction Set

The instruction set is divided into nine categories of operations:

Data Transfer
Arithmetic
Shift/Rotate
String Manipulation
Bit Manipulation
Control Transfer
High Level Language Support
Operating System Support
Processor Control

These 80376 processor instructions are listed in Table 8.1 **80376 Instruction Set and Clock Count Summary**.

All 80376 processor instructions operate on either 0, 1, 2 or 3 operands; an operand resides in a register, in the instruction itself, or in memory. Most zero operand instructions (e.g. CLI, STI) take only one byte. One operand instructions generally are two bytes long. The average instruction is 3.2 bytes long. Since the 80376 has a 16-byte prefetch instruction queue an average of 5 instructions can be prefetched. The use of two operands permits the following types of common instructions:

Register to Register
Memory to Register
Immediate to Register
Memory to Memory
Register to Memory
Immediate to Memory

The operands are either 8-, 16- or 32-bit long.

2.3 Memory Organization

Memory on the 80376 is divided into 8-bit quantities (bytes), 16-bit quantities (words), and 32-bit quantities (dwords). Words are stored in two consecutive bytes in memory with the low-order byte at the lowest address. Dwords are stored in four consecutive bytes in memory with the low-order byte at the lowest address. The address of a word or Dword is the byte address of the low-order byte. For maximum performance word and dword values should be at even physical addresses.

In addition to these basic data types the 80376 processor supports segments. Memory can be divided up into one or more variable length segments, which can be shared between programs.

ADDRESS SPACES

The 80376 has three types of address spaces: **logical, linear,** and **physical.** A **logical** address (also known as a **virtual** address) consists of a selector and an offset. A selector is the contents of a segment register. An offset is formed by summing all of the addressing components (BASE, INDEX, and DISPLACEMENT), discussed in Section 2.4 **Addressing Modes,** into an effective address.

Every selector has a **logical base** address associated with it that can be up to 32 bits in length. This 32-bit **logical base** address is added to either a 32-bit offset address or a 16-bit offset address (by using the ***address length prefix***)to form a final 32-bit **linear** address. This final **linear** address is then truncated so that only the lower 24 bits of this address are used to address the 16 Mbytes physical memory address space. The **logical base** address is stored in one of two operating system tables (i.e. the Local Descriptor Table or Global Descriptor Table).

Figure 2.3 shows the relationship between the various address spaces.

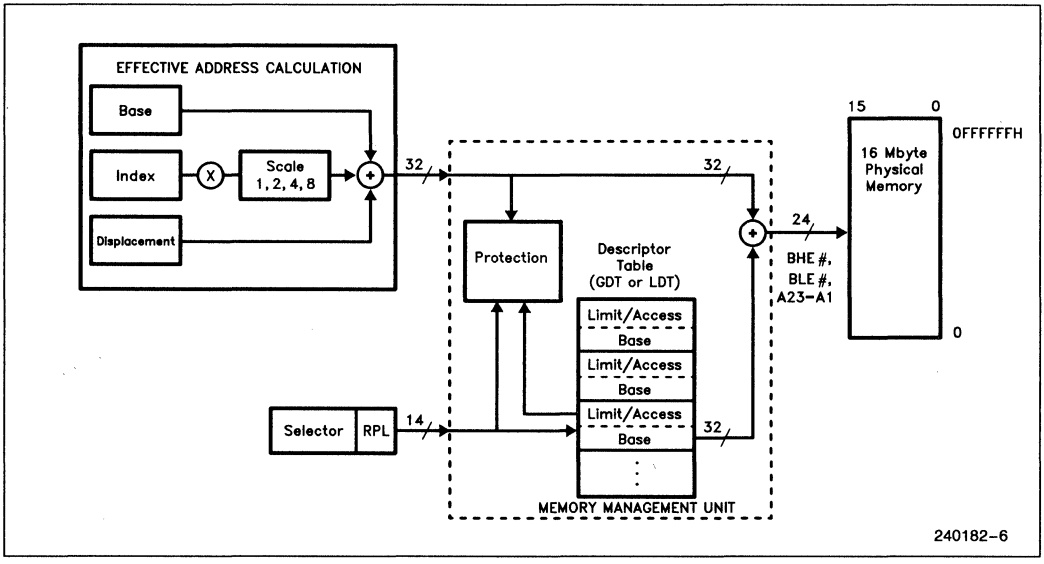

Figure 2.3. Address Translation

SEGMENT REGISTER USAGE

The main data structure used to organize memory is the segment. On the 80376, segments are variable sized blocks of linear addresses which have certain attributes associated with them. There are two main types of segments, code and data. The simplest use of segments is to have one code and data segment. Each segment is 16 Mbytes in size overlapping each other. This allows code and data to be directly addressed by the same offset.

In order to provide compact instruction encoding and increase processor performance, instructions do not need to explicitly specify which segment register is used. The segment register is automatically chosen according to the rules of Table 2.3 (Segment Register Selection Rules). In general, data references use the selector contained in the DS register, stack references use the SS register and instruction fetches use the CS register. The contents of the Instruction Pointer provide the offset. Special segment override prefixes allow the explicit use of a given segment register, and override the implicit rules listed in Table 2.3. The override prefixes also allow the use of the ES, FS and GS segment registers.

There are no restrictions regarding the overlapping of the base addresses of any segments. Thus, all 6 segments could have the base address set to zero. Further details of segmentation are discussed in Section 3.0 Architecture.

Table 2.3. Segment Register Selection Rules

Type of Memory Reference	Implied (Default) Segment Use	Segment Override Prefixes Possible
Code Fetch	CS	None
Destination of PUSH, PUSHF, INT, CALL, PUSHA Instructions	SS	None
Source of POP, POPA, POPF, IRET, RET Instructions	SS	None
Destination of STOS, MOVS, REP STOS, REP MOVS Instructions (DI is Base Register)	ES	None
Other Data References, with Effective Address Using Base Register of:		
[EAX]	DS	CS, SS, ES, FS, GS
[EBX]	DS	CS, SS, ES, FS, GS
[ECX]	DS	CS, SS, ES, FS, GS
[EDX]	DS	CS, SS, ES, FS, GS
[ESI]	DS	CS, SS, ES, FS, GS
[EDI]	DS	CS, SS, ES, FS, GS
[EBP]	SS	CS, SS, ES, FS, GS
[ESP]	SS	CS, SS, ES, FS, GS

2.4 Addressing Modes

The 80376 provides a total of 8 addressing modes for instructions to specify operands. The addressing modes are optimized to allow the efficient execution of high level languages such as C and FORTRAN, and they cover the vast majority of data references needed by high-level languages.

Two of the addressing modes provide for instructions that operate on register or immediate operands:

Register Operand Mode: The operand is located in one of the 8-, 16- or 32-bit general registers.

Immediate Operand Mode: The operand is included in the instruction as part of the opcode.

The remaining 6 modes provide a mechanism for specifying the effective address of an operand. The linear address consists of two components: the segment base address and an effective address. The effective address is calculated by summing any combination of the following three address elements (see Figure 2.3):

DISPLACEMENT: an 8-, 16- or 32-bit immediate value following the instruction.

BASE: The contents of any general purpose register. The base registers are generally used by compilers to point to the start of the local variable area. Note that if the ***Address Length Prefix*** is used, only BX and BP can be used as a BASE register.

INDEX: The contents of any general purpose register except for ESP. The index registers are used to access the elements of an array, or a string of characters. The index register's value can be multiplied by a scale factor, either 1, 2, 4 or 8. The scaled index is especially useful for accessing arrays or structures. Note that if the ***Address Length Prefix*** is used, no Scaling is available and only the registers SI and DI can be used to INDEX.

Combinations of these 3 components make up the 6 additional addressing modes. There is no performance penalty for using any of these addressing combinations, since the effective address calculation is pipelined with the execution of other instructions. The one exception is the simultaneous use of BASE and INDEX components which requires one additional clock.

As shown in Figure 2.4, the effective address (EA) of an operand is calculated according to the following formula:

$$EA = BASE_{Register} + (INDEX_{Register} \times scaling) + DISPLACEMENT$$

1. **Direct Mode:** The operand's offset is contained as part of the instruction as an 8-, 16- or 32-bit DISPLACEMENT.
2. **Register Indirect Mode:** A BASE register contains the address of the operand.
3. **Based Mode:** A BASE register's contents is added to a DISPLACEMENT to form the operand's offset.
4. **Scaled Index Mode:** An INDEX register's contents is multiplied by a SCALING factor which is added to a DISPLACEMENT to form the operand's offset.
5. **Based Scaled Index Mode:** The contents of an INDEX register is multiplied by a SCALING factor and the result is added to the contents of a BASE register to obtain the operand's offset.
6. **Based Scaled Index Mode with Displacement:** The contents of an INDEX register are multiplied by a SCALING factor, and the result is added to the contents of a BASE register and a DISPLACEMENT to form the operand's offset.

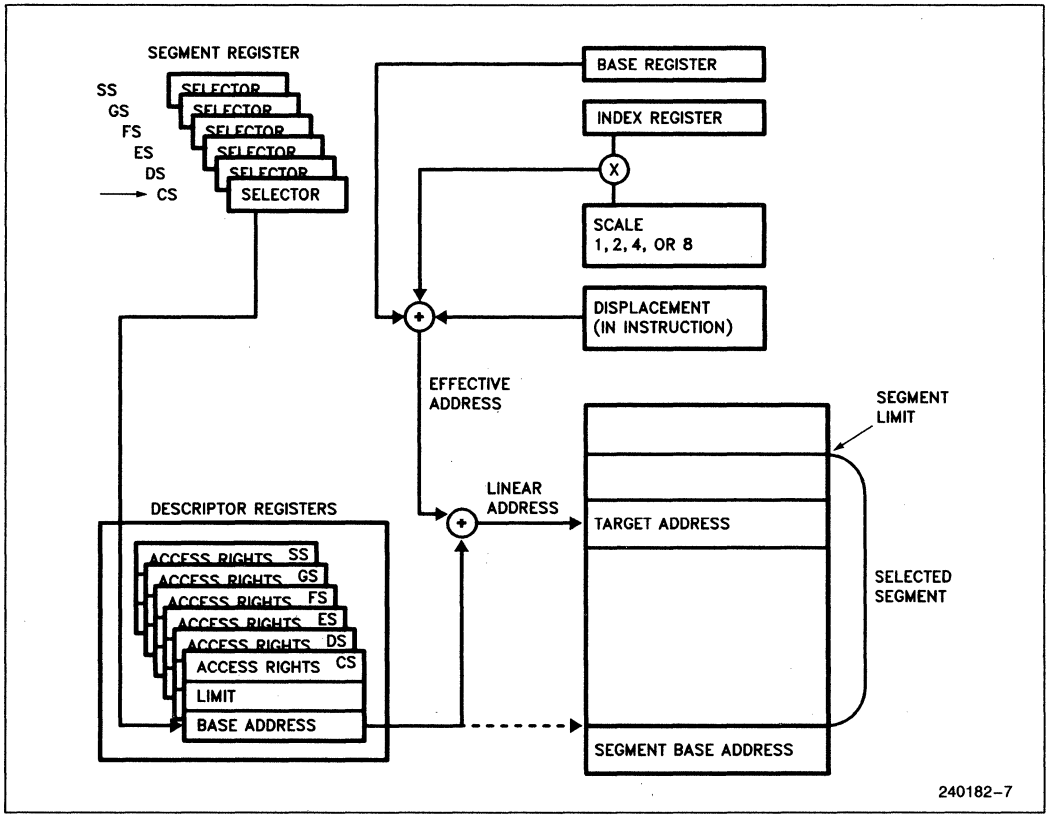

Figure 2.4. Addressing Mode Calculations

GENERATING 16-BIT ADDRESSES

The 80376 executes code with a default length for operands and addresses of 32 bits. The 80376 is also able to execute operands and addresses of 16 bits. This is specified through the use of override prefixes. Two prefixes, the **Operand Length Prefix** and the **Address Length Prefix,** override the default 32-bit length on an individual instruction basis. These prefixes are automatically added by assemblers. The Operand Length and Address Length Prefixes can be applied separately or in combination to any instruction.

The 80376 normally executes 32-bit code and uses either 8- or 32-bit displacements, and any register can be used as based or index registers. When executing 16-bit code (by prefix overrides), the displacements are either 8 or 16 bits, and the base and index register conform to the 16-bit model. Table 2.4 illustrates the differences.

Table 2.4. BASE and INDEX Registers for 16- and 32-Bit Addresses

	16-Bit Addressing	32-Bit Addressing
BASE REGISTER	BX, BP	Any 32-Bit GP Register
INDEX REGISTER	SI, DI	Any 32-Bit GP Register except ESP
SCALE FACTOR	None	1, 2, 4, 8
DISPLACMENT	0, 8, 16 Bits	0, 8, 32 Bits

2.5 Data Types

The 80376 supports all of the data types commonly used in high level languages:

Bit:	A single bit quantity.
Bit Field:	A group of up to 32 contiguous bits, which spans a maximum of four bytes.
Bit String:	A set of contiguous bits, on the 80376 bit strings can be up to 16 Mbits long.
Byte:	A signed 8-bit quantity.
Unsigned Byte:	An unsigned 8-bit quantity.
Integer (Word):	A signed 16-bit quantity.
Long Integer (Double Word):	A signed 32-bit quantity. All operations assume a 2's complement representation.
Unsigned Integer (Word):	An unsigned 16-bit quantity.
Unsigned Long Integer (Double Word):	An unsigned 32-bit quantity.
Signed Quad Word:	A signed 64-bit quantity.
Unsigned Quad Word:	An unsigned 64-bit quantity.
Pointer:	A 16- or 32-bit offset only quantity which indirectly references another memory location.
Long Pointer:	A full pointer which consists of a 16-bit segment selector and either a 16- or 32-bit offset.
Char:	A byte representation of an ASCII Alphanumeric or control character.
String:	A contiguous sequence of bytes, words or dwords. A string may contain between 1 byte and 16 Mbytes.
BCD:	A byte (unpacked) representation of decimal digits 0–9.
Packed BCD:	A byte (packed) representation of two decimal digits 0–9 storing one digit in each nibble.

When the 80376 is coupled with a numerics Coprocessor such as the 80387SX then the following common Floating Point types are supported.

Floating Point: A signed 32-, 64- or 80-bit real number representation. Floating point numbers are supported by the 80387SX numerics coprocessor.

Figure 2.5 illustrates the data types supported by the 80376 processor and the 80387SX coprocessor.

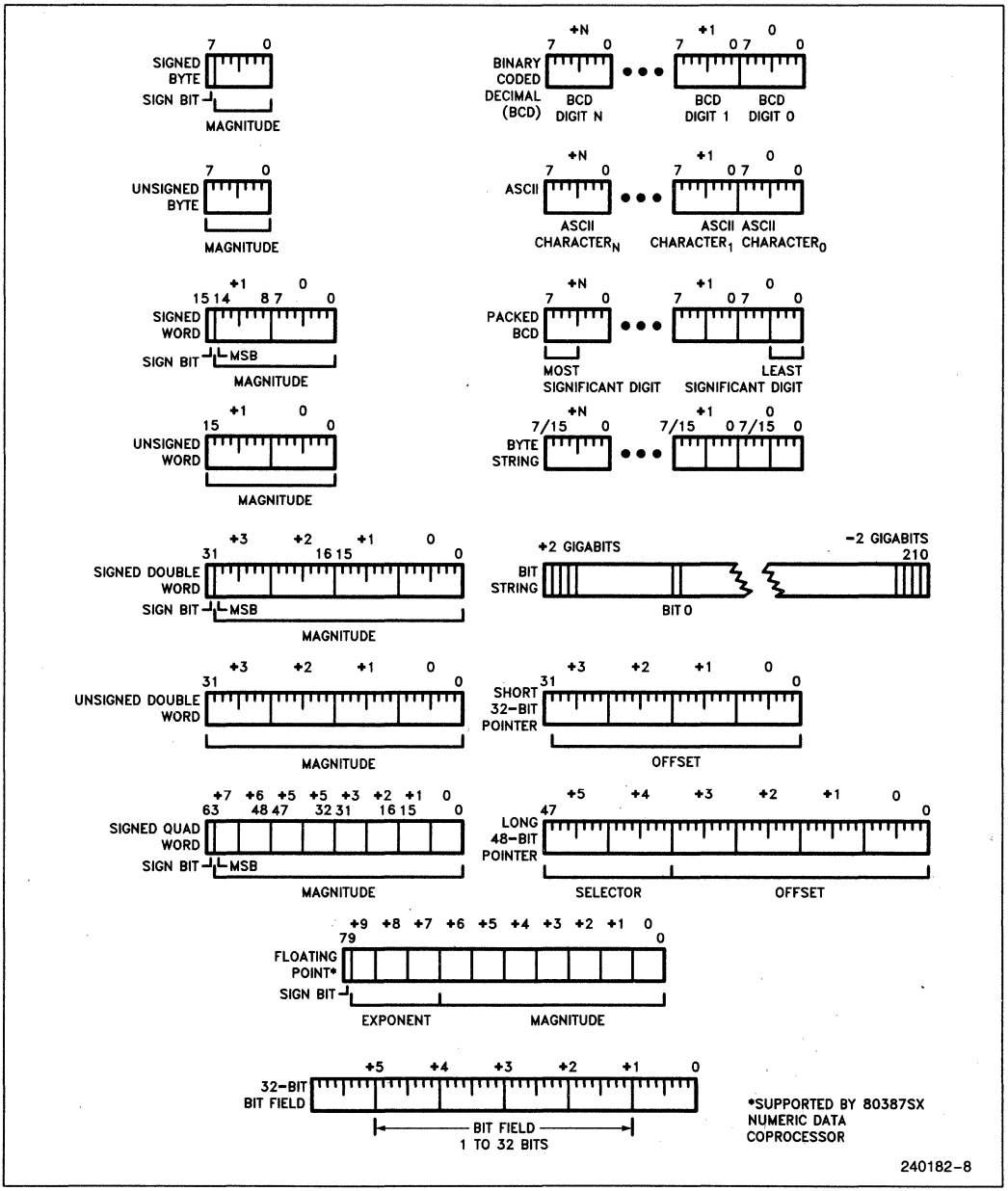

Figure 2.5. 80376 Supported Data Types

2.6 I/O Space

The 80376 has two distinct physical address spaces: physical memory and I/O. Generally, peripherals are placed in I/O space although the 80376 also supports memory-mapped peripherals. The I/O space consists of 64 Kbytes which can be divided into 64K 8-bit ports, 32K 16-bit ports, or any combination of ports which add to no more than 64 Kbytes. The M/$\overline{IO}$ pin acts as an additional address line, thus allowing the system designer to easily determine which address space the processor is accessing. Note that the I/O address refers to a physical address.

The I/O ports are accessed by the IN and OUT instructions, with the port address supplied as an immediate 8-bit constant in the instruction or in the DX register. All 8-bit and 16-bit port addresses are zero extended on the upper address lines. The I/O instructions cause the M/$\overline{IO}$ pin to be driven LOW. I/O port addresses 00F8H through 00FFH are reserved for use by Intel.

2.7 Interrupts and Exceptions

Interrupts and exceptions alter the normal program flow in order to handle external events, report errors or exceptional conditons. The difference between interrupts and exceptions is that interrupts are used to handle asynchronous external events while exceptions handle instruction faults. Although a program can generate a software interrupt via an INT N instruction, the processor treats software interrupts as exceptions.

Hardware interrupts occur as the result of an external event and are classified into two types: maskable or non-maskable. Interrupts are serviced after the execution of the current instruction. After the interrupt handler is finished servicing the interrupt, execution proceeds with the instruction immediately **after** the interrupted instruction.

Exceptions are classified as faults, traps, or aborts depending on the way they are reported, and whether or not restart of the instruction causing the exception is suported. **Faults** are exceptions that are detected and serviced **before** the execution of the faulting instruction. **Traps** are exceptions that are reported immediately **after** the execution of the instruction which caused the problem. **Aborts** are exceptions which do not permit the precise location of the instruction causing the exception to be determined. Thus, when an interrupt service routine has been completed, execution proceeds from the instruction immediately following the interrupted instruction. On the other hand the return address from an exception/fault routine will always point at the instruction causing the exception and include any leading instruction prefixes. Table 2.5 summarizes the possible interrupts for the 80376 and shows where the return address points to.

The 80376 has the ability to handle up to 256 different interrupts/exceptions. In order to service the interrupts, a table with up to 256 interrupt vectors must be defined. The interrupt vectors are simply pointers to the appropriate interrupt service routine. The interrupt vectors are 8-byte quantities, which are put in an Interrupt Descriptor Table. Of the 256 possible interrupts, 32 are reserved for use by Intel and the remaining 224 are free to be used by the system designer.

INTERRUPT PROCESSING

When an interrupt occurs the following actions happen. First, the current program address and the Flags are saved on the stack to allow resumption of the interrupted program. Next, an 8-bit vector is supplied to the 80376 which identifies the appropriate entry in the interrupt table. The table contains either an Interrupt Gate, a Trap Gate or a Task Gate that will point to an interrupt procedure or task. The user supplied interrupt service routine is executed. Finally, when an IRET instruction is executed the old processor state is restored and program execution resumes at the appropriate instruction.

The 8-bit interrupt vector is supplied to the 80376 in several different ways: exceptions supply the interrupt vector internally; software INT instructions contain or imply the vector; maskable hardware interrupts supply the 8-bit vector via the interrupt acknowledge bus sequence. Non-Maskable hardware interrupts are assigned to interrupt vector 2.

Maskable Interrupt

Maskable interrupts are the most common way to respond to asynchronous external hardware events. A hardware interrupt occurs when the INTR is pulled HIGH and the Interrupt Flag bit (IF) is enabled. The processor only responds to interrupts between instructions (string instructions have an "interrupt window" between memory moves which allows interrupts during long string moves). When an interrupt occurs the processor reads an 8-bit vector supplied by the hardware which identifies the source of the interrupt (one of 224 user defined interrupts).

Table 2.5. Interrupt Vector Assignments

Function	Interrupt Number	Instruction Which Can Cause Exception	Return Address Points to Faulting Instruction	Type
Divide Error	0	DIV, IDIV	Yes	FAULT
Debug Exception	1	Any Instruction	Yes	TRAP*
NMI Interrupt	2	INT 2 or NMI	No	NMI
One-Byte Interrupt	3	INT	No	TRAP
Interrupt on Overflow	4	INTO	No	TRAP
Array Bounds Check	5	BOUND	Yes	FAULT
Invalid OP-Code	6	Any Illegal Instruction	Yes	FAULT
Device Not Available	7	ESC, WAIT	Yes	FAULT
Double Fault	8	Any Instruction That Can Generate an Exception		ABORT
Coprocessor Segment Overrun	9	ESC	No	ABORT
Invalid TSS	10	JMP, CALL, IRET, INT	Yes	FAULT
Segment Not Present	11	Segment Register Instructions	Yes	FAULT
Stack Fault	12	Stack References	Yes	FAULT
General Protection Fault	13	Any Memory Reference	Yes	FAULT
Intel Reserved	14–15	—	—	—
Coprocessor Error	16	ESC, WAIT	Yes	FAULT
Intel Reserved	17–32			
Two-Byte Interrupt	0–255	INT n	No	TRAP

*Some debug exceptions may report both traps on the previous instruction, and faults on the next instruction.

Interrupts through Interrupt Gates automatically reset IF, disabling INTR requests. Interrupts through Trap Gates leave the state of the IF bit unchanged. Interrupts through a Task Gate change the IF bit according to the image of the EFLAGs register in the task's Task State Segment (TSS). When an IRET instruction is executed, the original state of the IF bit is restored.

Non-Maskable Interrupt

Non-maskable interrupts provide a method of servicing very high priority interrupts. When the NMI input is pulled HIGH it causes an interrupt with an internally supplied vector value of 2. Unlike a normal hardware interrupt no interrupt acknowledgement sequence is performed for an NMI.

While executing the NMI servicing procedure, the 80376 will not service any further NMI request, or INT requests, until an interrupt return (IRET) instruction is executed or the processor is reset. If NMI occurs while currently servicing an NMI, its presence will be saved for servicing after executing the first IRET instruction. The disabling of INTR requests depends on the gate in IDT location 2.

Software Interrupts

A third type of interrupt/exception for the 80376 is the software interrupt. An INT n instruction causes the processor to execute the interrupt service routine pointed to by the n^{th} vector in the interrupt table.

A special case of the two byte software interrupt INT n is the one byte INT 3, or breakpoint interrupt. By inserting this one byte instruction in a program, the user can set breakpoints in his program as a debugging tool.

A final type of software interrupt, is the single step interrupt. It is discussed in **Single-Step Trap** (page 22).

INTERRUPT AND EXCEPTION PRIORITIES

Interrupts are externally-generated events. Maskable Interrupts (on the INTR input) and Non-Maskable Interrupts (on the NMI input) are recognized at instruction boundaries. When NMI and maskable INTR are **both** recognized at the **same** instruction boundary, the 80376 invokes the NMI service routine first. If, after the NMI service routine has been invoked, maskable interrupts are still enabled, then the 80376 will invoke the appropriate interrupt service routine.

As the 80376 executes instructions, it follows a consistent cycle in checking for exceptions, as shown in Table 2.6. This cycle is repeated as each instruction is executed, and occurs in parallel with instruction decoding and execution.

INSTRUCTION RESTART

The 80376 fully supports restarting all instructions after faults. If an exception is detected in the instruction to be executed (exception categories 4 through 9 in Table 2.6), the 80376 device invokes the appropriate exception service routine. The 80376 is in a state that permits restart of the instruction.

DOUBLE FAULT

A Double fault (exception 8) results when the processor attempts to invoke an exception service routine for the segment exceptions (10, 11, 12 or 13), but in the process of doing so, detects an exception.

2.8 Reset and Initialization

When the processor is Reset the registers have the values shown in Table 2.7. The 80376 will then start executing instructions near the top of physical memory, at location 0FFFFF0H. A short JMP should be executed within the segment defined for power-up (see Table 2.7). The GDT should then be initialized for a start-up data and code segment followed by a far JMP that will load the segment descriptor cache with the new descriptor values. The IDT table, after reset, is located at physical address 0H, with a limit of 256 entries.

RESET forces the 80376 to terminate all execution and local bus activity. No instruction execution or bus activity will occur as long as Reset is active. Between 350 and 450 CLK2 periods after Reset becomes inactive, the 80376 will start executing instructions at the top of physical memory.

Table 2.6. Sequence of Exception Checking

Consider the case of the 80376 having just completed an instruction. It then performs the following checks before reaching the point where the next instruction is completed:

1. Check for Exception 1 Traps from the instruction just completed (single-step via Trap Flag, or Data Breakpoints set in the Debug Registers).
2. Check for external NMI and INTR.
3. Check for Exception 1 Faults in the next instruction (Instruction Execution Breakpoint set in the Debug Registers for the next instruction).
4. Check for Segmentation Faults that prevented fetching the entire next instruction (exceptions 11 or 13).
5. Check for Faults decoding the next instruction (exception 6 if illegal opcode; or exception 13 if instruction is longer than 15 bytes, or privilege violation (i.e. not at IOPL or at CPL = 0).
6. If WAIT opcode, check if TS = 1 and MP = 1 (exception 7 if both are 1).
7. If ESCape opcode for numeric coprocessor, check if EM = 1 or TS = 1 (exception 7 if either are 1).
8. If WAIT opcode or ESCape opcode for numeric coprocessor, check $\overline{\text{ERROR}}$ input signal (exception 16 if $\overline{\text{ERROR}}$ input is asserted).
9. Check for Segmentation Faults that prevent transferring the entire memory quantity (exceptions 11, 12, 13).

Table 2.7. Register Values after Reset

Flag Word (EFLAGS)	uuuu0002H	(Note 1)
Machine Status Word (CR0)	uuuuuuu1H	(Note 2)
Instruction Pointer (EIP)	0000FFF0H	
Code Segment (CS)	F000H	(Note 3)
Data Segment (DS)	0000H	(Note 4)
Stack Segment (SS)	0000H	
Extra Segment (ES)	0000H	(Note 4)
Extra Segment (FS)	0000H	
Extra Segment (GS)	0000H	
EAX Register	0000H	(Note 5)
EDX Register	Component and Stepping ID	(Note 6)
All Other Registers	Undefined	(Note 7)

NOTES:
1. EFLAG Register. The upper 14 bits of the EFLAGS register are undefined, all defined flag bits are zero.
2. CR0: The defined 4 bits in the CR0 is equal to 1H.
3. The Code Segment Register (CS) will have its Base Address set to 0FFFF0000H and Limit set to 0FFFFH.
4. The Data and Extra Segment Registers (DS and ES) will have their Base Address set to 000000000H and Limit set to 0FFFFH.
5. If self-test is selected, the EAX should contain a 0 value. If a value of 0 is not found the self-test has detected a flaw in the part.
6. EDX register always holds component and stepping identifier.
7. All unidentified bits are Intel Reserved and should not be used.

2.9 Initialization

Because the 80376 processor starts executing in protected mode, certain precautions need be taken during initialization. Before any far jumps can take place the GDT and/or LDT tables need to be setup and their respective registers loaded. Before interrupts can be initialized the IDT table must be setup and the IDTR must be loaded. The example code is shown below:

```
; ***************************************************************
;
; This is an example of startup code to put either an 80376,
; 80386SX or 80386 into flat mode. All of memory is treated as
; simple linear RAM. There are no interrupt routines. The
; Builder creates the GDT-alias and IDT-alias and places them,
; by default, in GDT[1] and GDT[2].  Other entries in the GDT
; are specified in the Build file.  After initialization it jumps
; to a C startup routine. To use this template, change this jmp
; address to that of your code, or make the label of your code
; "c_startup".
;
; This code was assembled and built using version 1.2 of the
; Intel RLL utilities and Intel 386ASM assembler.
;
;             ***    This code was tested    ***
;
; ***************************************************************
```

```
NAME FLAT                ; name of the object module

EXTRN    c_startup:near ; this is the label jmped to after init

pe_flag       equ 1
data_selc     equ 20h    ; assume code is GDT[3], data GDT[4]

INIT_CODE    SEGMENT ER PUBLIC USE32     ; Segment base at 0ffffff80h

PUBLIC GDT_DESC

gdt_desc    dq  ?

PUBLIC    START

start:
    cld                          ; clear direction flag
    smsw bx                      ; check for processor (80376) at reset
    test bl,1                    ; use SMSW rather than MOV for speed
    jnz pestart
realstart                        ; is an 80386 and in real mode
    db 66h                       ; force the next operand into 32-bit mode.
    mov eax,offset gdt_desc      ; move address of the GDT descriptor into eax
    xor ebx,ebx                  ; clear ebx
    mov bh,ah                    ; load 8 bits of address into bh
    move bl,al                   ; load 8 bits of address into bl
    db 67h
    db 66h                       ; use the 32-bit form of LGDT to load
    lgdt cs:[ebx]                ; the 32-bits of address into the GDTR
    smsw ax                      ; go into protected mode (set PE bit)
    or al,pe_flag
    lmsw ax
    jmp next                     ; flush prefetch queue
pestart:
    mov ebx,offset gdt_desc
    xor eax,eax
    mov ax,bx                    ; lower portion of address only
    lgdt cs:[eax]
    xor ebx,ebx                  ; initialize data selectors
    mov bl,data_selc             ; GDT[3]
    mov ds,bx
    mov ss,bx
    mov es,bx
    mov fs,bx
    mov gs,bx
    jmp pejump
next:
    xor ebx,ebx                  ; initialize data selectors
    mov bl,data_selc             ; GDT[3]
    mov ds,bx
    mov ss,bx
    mov es,bx
    mov fs,bx
    mov gs,bx
    db 66h                       ; for the 80386, need to make a 32-bit jump
pejump:
    jmp far ptr c_startup        ; but the 80376 is already 32-bit.

    org 70h                      ; only if segment base is at 0ffffff80h
    jmp short start
INIT_CODE ENDS
END
```

This code should be linked into your application for boot loadable code. The following build file illustrates how this is accomplished.

```
FLAT; -- build program id

SEGMENT
    *segments (dpl=0),              -- Give all user segments a DPL of 0.
    _phantom_code_ (dpl=0),         -- These two segments are created by
    _phantom_data_ (dpl=0),         -- the builder when the FLAT control is used.
    init_code  (base=0ffffff80h); -- Put startup code at the reset vector area.

GATE
    gl3 (entry=13, dpl=0, trap),        -- trap gate disables interrupts
    i32 (entry=32, dpl=0, interrupt),  -- interrupt gates doesn't

TABLE
    -- create GDT

    GDT (LOCATION = GDT_DESC,       -- In a buffer starting at GDT_DESC,
                                    -- BLD386 places the GDT base and
                                    -- GDT limit values. Buffer must be
                                    -- 6 bytes long. The base and limit
                                    -- values are places in this buffer
                                    -- as two bytes of limit plus
                                    -- four bytes of base in the format
                                    -- required for use by the LGDT
                                    -- instruction.
        ENTRY = (3:_phantom_code_,      -- Explicitly place segment
                 4:_phantom_data_,      -- entries into the GDT.
                 5:code32,
                 6:data,
                 7:init_code)
        );
TASK

    MAIN_TASK
        (
         DPL  = 0,                  -- Task privilege level is 0.
         DATA = DATA,               -- Points to a segment that
                                    -- indicates initial DS value.
         CODE = main,               -- Entry point is main, which
                                    -- must be a public id.

         STACKS = (DATA),           -- Segment id points to stack
                                    -- segment. Sets the initial SS:ESP.
         NO INTENABLED,             -- Disable interrupts.
         PRESENT                    -- Present bit in TSS set to 1.
        );

    MEMORY
        (RANGE = (EPROM = ROM(0ffff8000h..0ffffffffh),
                  DRAM = RAM(0..0ffffh)),
        ALLOCATE = (EPROM = (MAIN_TASK)));

END
```

```
asm386 flatsim.a38 debug
asm386 application.a38 debug
bnd386 application.obj,flatsim.obj nolo debug oj (application.bnd)
bld386 application.bnd bf (flatsim.bld) bl flat
```

Commands to assemble and build a boot-loadable application named "application.a38". The initialization code is called "flatsim.a38", and build file is called "application.bld".

2.10 Self-Test

The 80376 has the capability to perform a self-test. The self-test checks the function of all of the Control ROM and most of the non-random logic of the part. Approximately one-half of the 80376 can be tested during self-test.

Self-Test is initiated on the 80376 when the RESET pin transitions from HIGH to LOW, and the $\overline{BUSY}$ pin is LOW. The self-test takes about 2^{20} clocks, or approximately 33 ms with a 16 MHz 80376 processor. At the completion of self-test the processor performs reset and begins normal operation. The part has successfully passed self-test if the contents of the EAX register is zero. If the EAX register is not zero then the self-test has detected a flaw in the part. If self-test is not selected after reset, EAX may be non-zero after reset.

2.11 Debugging Support

The 80376 provides several features which simplify the debugging process. The three categories of on-chip debugging aids are:

1. The code execution breakpoint opcode (0CCH).
2. The single-step capability provided by the TF bit in the flag register, and
3. The code and data breakpoint capability provided by the Debug Registers DR0–3, DR6, and DR7.

BREAKPOINT INSTRUCTION

A single-byte software interrupt (Int 3) breakpoint instruction is available for use by software debuggers. The breakpoint opcode is 0CCh, and generates an exception 3 trap when executed.

DEBUG REGISTERS

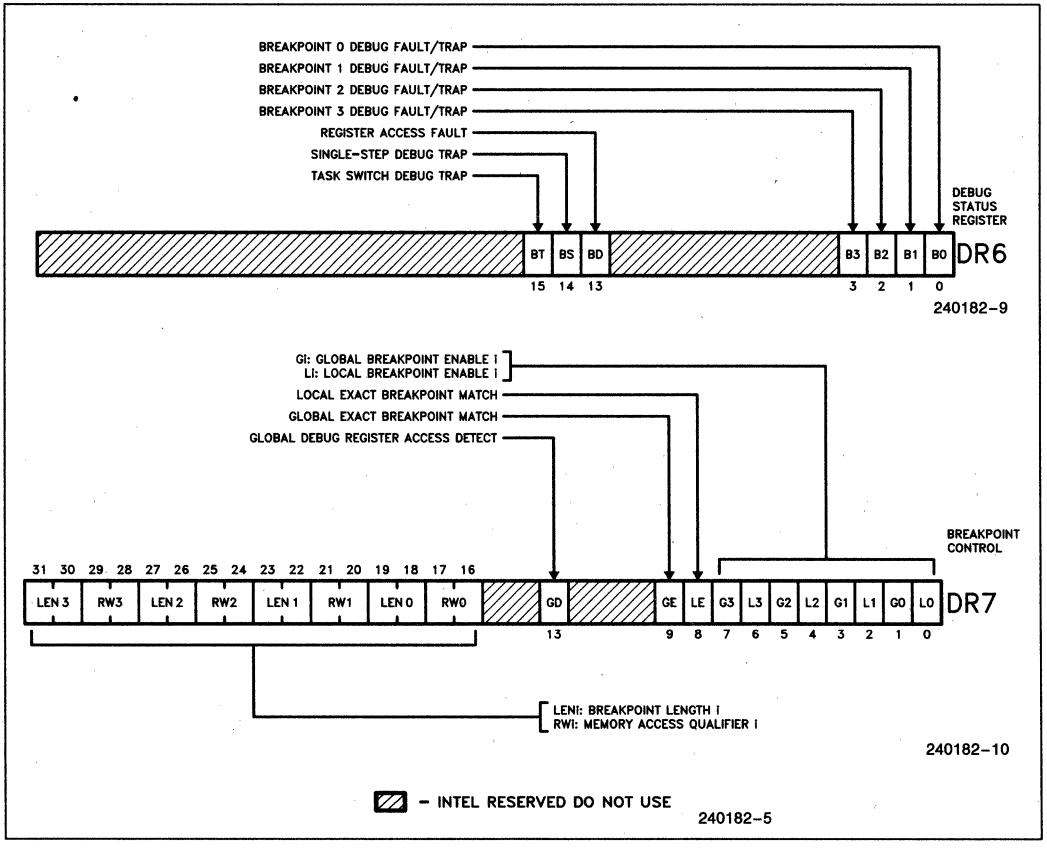

Figure 2.6. Debug Registers

SINGLE-STEP TRAP

If the single-step flag (TF, bit 8) in the EFLAG register is found to be set at the end of an instruction, a single-step exception occurs. The single-step exception is auto vectored to exception number 1.

The Debug Registers are an advanced debugging feature of the 80376. They allow data access breakpoints as well as code execution breakpoints. Since the breakpoints are indicated by on-chip registers, an instruction execution breakpoint can be placed in ROM code or in code shared by several tasks, neither of which can be supported by the INT 3 breakpoint opcode.

The 80376 contains six Debug Registers, consisting of four breakpoint address registers and two breakpoint control registers. Initially after reset, breakpoints are in the disabled state; therefore, no breakpoints will occur unless the debug registers are programmed. Breakpoints set up in the Debug Registers are auto-vectored to exception 1. Figure 2.6 shows the breakpoint status and control registers.

3.0 ARCHITECTURE

The Intel 80376 Embedded Processor has a physical address space of 16 Mbytes (2^{24} bytes) and allows the running of virtual memory programs of almost unlimited size (16 Kbytes × 16 Mbytes or 256 Gbytes (2^{38} bytes)). In addition the 80376 provides a sophisticated memory management and a hardware-assisted protection mechanism.

3.1 Addressing Mechanism

The 80376 uses two components to form the logical address, a 16-bit selector which determines the linear base address of a segment, and a 32-bit effective address. The selector is used to specify an index into an operating system defined table (see Figure 3.1). The table contains the 32-bit base address of a given segment. The linear address is formed by adding the base address obtained from the table to the 32-bit effective address. This value is truncated to 24 bits to form the physical address, which is then placed on the address bus.

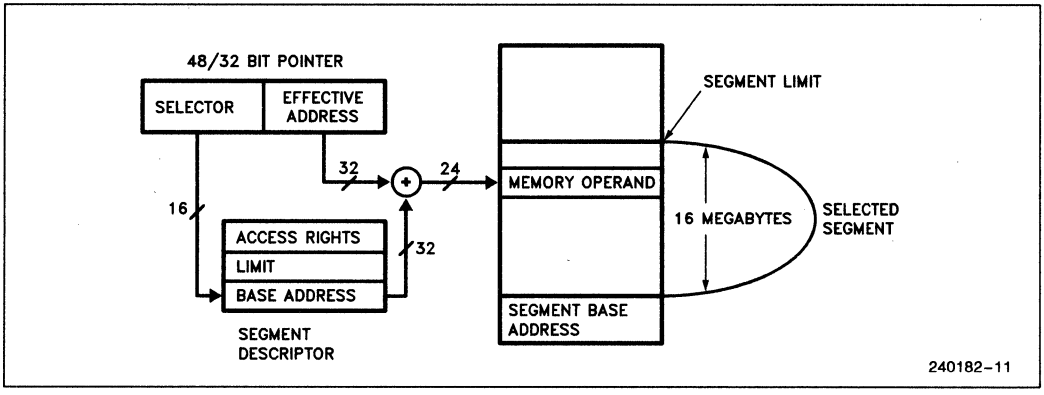

Figure 3.1. Address Calculation

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3.2 Segmentation

Segmentation is one method of memory management and provides the basis for protection in the 80376. Segments are used to encapsulate regions of memory which have common attributes. For example, all of the code of a given program could be contained in a segment, or an operating system table may reside in a segment. All information about each segment, is stored in an 8-byte data structure called a descriptor. All of the descriptors in a system are contained in tables recognized by hardware.

TERMINOLOGY

The following terms are used throughout the discussion of descriptors, privilege levels and protection:

PL: **Privilege Level**—One of the four hierarchical privilege levels. Level 0 is the most privileged level and level 3 is the least privileged.

RPL: **Requestor Privilege Level**—The privilege level of the original supplier of the selector. RPL is determined by the least two significant bits of a selector.

DPL: **Descriptor Privilege Level**—This is the least privileged level at which a task may access that descriptor (and the segment associated with that descriptor). Descriptor Privilege Level is determined by bits 6:5 in the Access Right Byte of a descriptor.

CPL: **Current Privilege Level**—The privilege level at which a task is currently executing, which equals the privilege level of the code segment being executed. CPL can also be determined by examining the lowest 2 bits of the CS register, except for conforming code segments.

EPL: **Effective Privilege Level**—The effective privilege level is the least privileged of the RPL and the DPL. EPL is the numerical maximum of RPL and DPL.

Task: One instance of the execution of a program. Tasks are also referred to as processes.

DESCRIPTOR TABLES

The descriptor tables define all of the segments which are used in an 80376 system. There are three types of tables on the 80376 which hold descriptors: the Global Descriptor Table, Local Descriptor Table, and the Interrupt Decriptor Table. All of the tables are variable length memory arrays, they can range in size between 8 bytes and 64 Kbytes. Each table can hold up to 8192 8-byte descriptors. The upper 13 bits of a selector are used as an index into the descriptor table. The tables have registers associated with them which hold the 32-bit linear base address, and the 16-bit limit of each table.

Each of the tables have a register associated with it: GDTR, LDTR and IDTR; see Figure 3.2. The LGDT, LLDT and LIDT instructions load the base and limit of the Global, Local and Interrupt Descriptor Tables into the appropriate register. The SGDT, SLDT and SIDT store these base and limit values. These are privileged instructions.

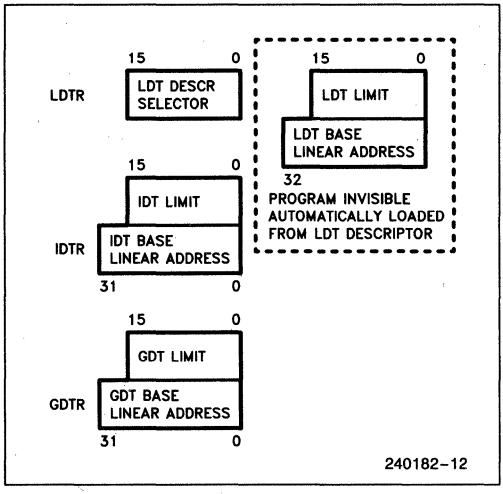


Figure 3.2. Descriptor Table Registers

Global Descriptor Table

The Global Descriptor Table (GDT) contains descriptors which are possibly available to all of the tasks in a system. The GDT can contain any type of segment descriptor except for interrupt and trap descriptors. Every 80376 system contains a GDT. A simple 80376 system contains only 2 entries in the GDT; a code and a data descriptor. For maximum performance, descriptor tables should begin on even addresses.

The first slot of the Global Descriptor Table corresponds to the null selector and is not used. The null selector defines a null pointer value.

Local Descriptor Table

LDTs contain descriptors which are associated with a given task. Generally, operating systems are designed so that each task has a separate LDT. The LDT may contain only code, data, stack, task gate, and call gate descriptors. LDTs provide a mechanism for isolating a given task's code and data segments from the rest of the operating system, while the GDT contains descriptors for segments which are common to all tasks. A segment cannot be accessed by a task if its segment descriptor does not exist in either the current LDT or the GDT. This pro-

vides both isolation and protection for a task's segments, while still allowing global data to be shared among tasks.

Unlike the 6-byte GDT or IDT registers which contain a base address and limit, the visible portion of the LDT register contains only a 16-bit selector. This selector refers to a Local Descriptor Table descriptor in the GDT (see Figure 2.1).

INTERRUPT DESCRIPTOR TABLE

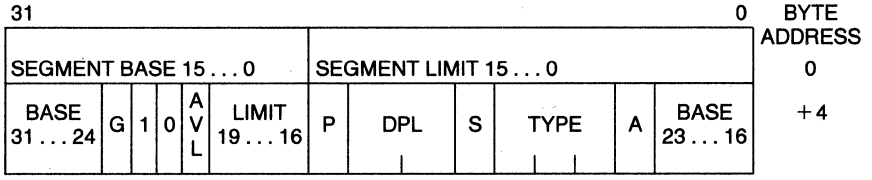
The third table needed for 80376 systems is the Interrupt Descriptor Table. The IDT contains the descriptors which point to the location of up to 256 interrupt service routines. The IDT may contain only task gates, interrupt gates and trap gates. The IDT should be at least 256 bytes in size in order to hold the descriptors for the 32 Intel Reserved Interrupts. Every interrupt used by a system must have an entry in the IDT. The IDT entries are referenced by INT instructions, external interrupt vectors, and exceptions.

DESCRIPTORS

The object to which the segment selector points to is called a descriptor. Descriptors are eight-byte quantities which contain attributes about a given region of linear address space. These attributes include the 32-bit logical base address of the segment, the 20-bit length and granularity of the segment, the protection level, read, write or execute privileges, and the type of segment. All of the attribute information about a segment is contained in 12 bits in the segment descriptor. Figure 3.3 shows the general format of a descriptor. All segments on the the 80376 have three attribute fields in common: the Present bit (P), the Descriptor Privilege Level bits (DPL) and the Segment bit (S). P=1 if the segment is loaded in physical memory, if P = 0 then any attempt to access the segment causes a not present exception (exception 11). The DPL is a two-bit field which specifies the protection level, 0–3, associated with a segment.

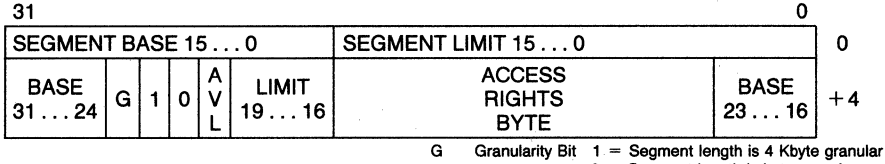
The 80376 has two main categories of segments: system segments, and non-system segments (for code and data). The segment bit, S, determines if a given segment is a system segment, a code segment or a data segment. If the S bit is 1 then the segment is either a code or data segment, if it is 0 then the segment is a system segment.

Note that although the 80376 is limited to a 16-Mbyte Physical address space (2^{24}), its base address allows a segment to be placed anywhere in a 4-Gbyte linear address space. When writing code for the 80376, users should keep code portability to an 80386 processor (or other processors with a larger physical address space) in mind. A segment base address can be placed anywhere in this 4-Gbyte linear address space, but a physical address will be



BASE Base Address of the segment
LIMIT The length of the segment
P Present Bit 1 = Present 0 = Not Present
DPL Descriptor Privilege Level 0–3
S Segment Descriptor: 0 = System Descriptor, 1 = Code or Data Descriptor
TYPE Type of Segment
A Accessed Bit
G Granularity Bit 1 = Segment length is 4 Kbyte Granular
0 = Segment length is byte granular
0 Bit must be zero (0) for compatibility with future processors
AVL Available field for user or OS

Figure 3.3. Segment Descriptors



G Granularity Bit 1 = Segment length is 4 Kbyte granular
0 = Segment length is byte granular
0 Bit must be zero (0) for compatibility with future processors
AVL Available field for user or OS

Figure 3.4. Code and Data Descriptors

Table 3.1. Access Rights Byte Definition for Code and Data Descriptors

Bit Position	Name	Function	
7	Present (P)	P = 1 Segment is mapped into physical memory. P = 0 No mapping to physical memory exits	
6–5	Descriptor Privilege Level (DPL)	Segment privilege attribute used in privilege tests.	
4	Segment Descriptor (S)	S = 1 Code or Data (includes stacks) segment descriptor S = 0 System Segment Descriptor or Gate Descriptor	
3 2 1	Executable (E) Expansion Direction (ED) Writable (W)	E = 0 Descriptor type is data segment: ED = 0 Expand up segment, offsets must be ≤ limit. ED = 1 Expand down segment, offsets must be > limit. W = 0 Data segment may not be written into. W = 1 Data segment may be written into.	If Data Segment (S = 1, E = 0)
3 2 1	Executable (E) Conforming (C) Readable (R)	E = 1 Descriptor type is code segment: C = 1 Code segment may only be executed when CPL ≥ DPL and CPL remains unchanged. R = 0 Code segment may not be read. R = 1 Code segment may be read.	If Code Segment (S = 1, E = 1)
0	Accessed (A)	A = 0 Segment has not been accessed. A = 1 Segment selector has been loaded into segment register or used by selector test instructions.	

generated that is a truncated version of this linear address. Truncation will be to the maximum number of address bits. It is recommended to place EPROM at the highest physical address and DRAM at the lowest physical addresses.

Code and Data Descriptors (S = 1)

Figure 3.4 shows the general format of a code and data descriptor and Table 3.1 illustrates how the bits in the Access Right Byte are interpreted.

Code and data segments have several descriptor fields in common. The accessed bit, A, is set whenever the processor accesses a descriptor. The granularity bit, G, specifies if a segment length is 1-byte-granular or 4-Kbyte-granular. Base address bits 31–24, which are normally found in 80386 descriptors, are not made externally available on the 80376. They do not affect the operation of the 80376. The A_{31}–A_{24} field should be set to allow an 80386 to correctly execute with EPROM at the upper 4096 Mbytes of physical memory.

System Descriptor Formats (S = 0)

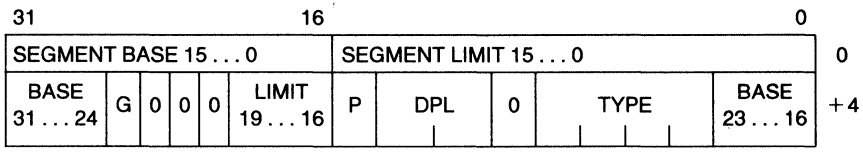
System segments describe information about operating system tables, tasks, and gates. Figure 3.5 shows the general format of system segment descriptors, and the various types of system segments. 80376 system descriptors (which are the same as 80386 descriptor types 2, 5, 9, B, C, E and F) contain a 32-bit logical base address and a 20-bit segment limit.

Selector Fields

A selector has three fields: Local or Global Descriptor Table Indicator (TI), Descriptor Entry Index (Index), and Requestor (the selector's) Privilege Level (RPL) as shown in Figure 3.6. The TI bit selects either the Global Descriptor Table or the Local Descriptor Table. The Index selects one of 8K descriptors in the appropriate descriptor table. The RPL bits allow high speed testing of the selector's privilege attributes.

Segment Descriptor Cache

In addition to the selector value, every segment register has a segment descriptor cache register associated with it. Whenever a segment register's contents are changed, the 8-byte descriptor associated with that selector is automatically loaded (cached) on the chip. Once loaded, all references to that segment use the cached descriptor information instead of reaccessing the descriptor. The contents of the descriptor cache are not visible to the programmer. Since descriptor caches only change when a segment register is changed, programs which modify the descriptor tables must reload the appropriate segment registers after changing a descriptor's value.



Type	Defines	Type	Defines
0	Invalid	8	Invalid
1	Reserved	9	Available 80376/80386 TSS
2	LDT	A	Undefined (Intel Reserved)
3	Reserved	B	Busy 80376/80386 TSS
4	Reserved	C	80376/80386 Call Gate
5	Task Gate (80376/80386 Task)	D	Undefined (Intel Reserved)
6	Reserved	E	80376/80386 Interrupt Gate
7	Reserved	F	80376/80386 Trap Gate

Figure 3.5. System Descriptors

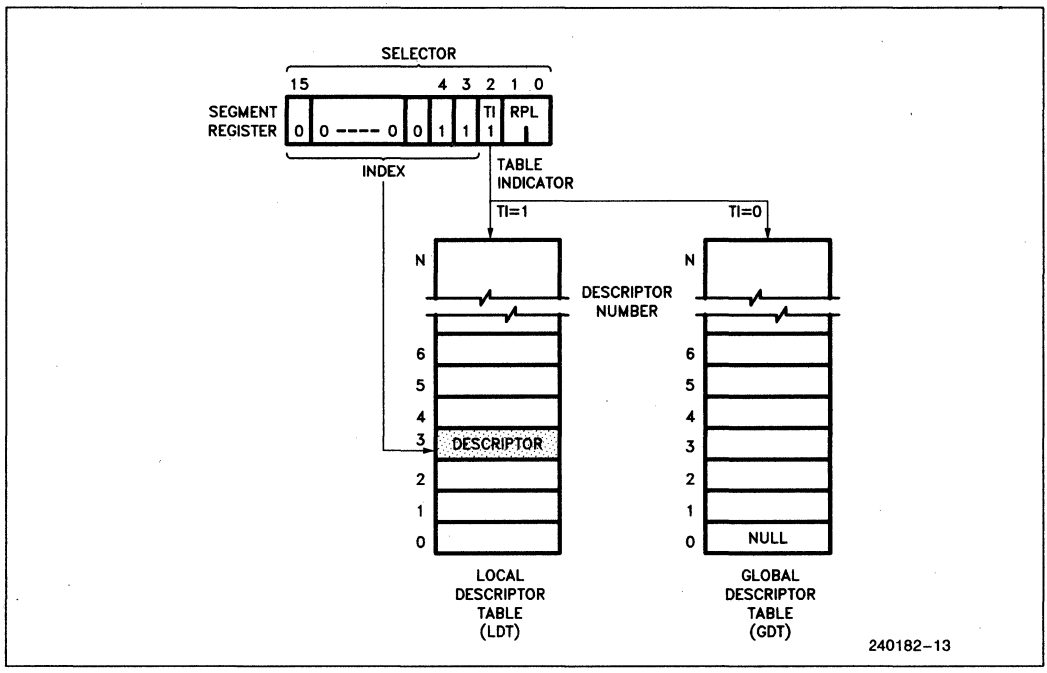


Figure 3.6. Example Descriptor Selection

3.3 Protection

The 80376 offers extensive protection features. These protection features are particularly useful in sophisticated embedded applications which use multitasking real-time operating systems. For simpler embedded applications these protection capabilities can be easily bypassed by making all applications run at privilege level (PL) 0.

RULES OF PRIVILEGE

The 80376 controls access to both data and procedures between levels of a task, according to the following rules.

—Data stored in a segment with privilege level **p** can be accessed only by code executing at a privilege level at least as privileged as **p.**

—A code segment/procedure with privilege level **p** can only be called by a task executing at the same or a lesser privilege level than **p.**

PRIVILEGE LEVELS

At any point in time, a task on the 80376 always executes at one of the four privilege levels. The Current Privilege Level (CPL) specifies what the task's privilege level is. A task's CPL may only be changed

by control transfers through gate descriptors to a code segment with a different privilege level. Thus, an application program running at PL = 3 may call an operating system routine at PL = 1 (via a gate) which would cause the task's CPL to be set to 1 until the operating system routine was finished.

Selector Privilege (RPL)

The privilege level of a selector is specified by the RPL field. The selector's RPL is only used to establish a less trusted privilege level than the current privilege level of the task for the use of a segment. This level is called the task's effective privilege level (EPL). The EPL is defined as being the least privileged (numerically larger) level of a task's CPL and a selector's RPL. The RPL is most commonly used to verify that pointers passed to an operating system procedure do not access data that is of higher privilege than the procedure that originated the pointer. Since the originator of a selector can specify any RPL value, the Adjust RPL (ARPL) instruction is provided to force the RPL bits to the originator's CPL.

I/O Privilege

The I/O privilege level (IOPL) lets the operating system code executing at CPL = 0 define the least privileged level at which I/O instructions can be used. An exception 13 (General Protection Violation) is generated if an I/O instruction is attempted when the CPL of the task is less privileged than the IOPL. The IOPL is stored in bits 13 and 14 of the EFLAGS register. The following instructions cause an exception 13 if the CPL is greater than IOPL: IN, INS, OUT, OUTS, STI, CLI and LOCK prefix.

Descriptor Access

There are basically two types of segment accesses: those involving code segments such as control transfers, and those involving data accesses. Determining the ability of a task to access a segment involves the type of segment to be accessed, the instruction used, the type of descriptor used and CPL, RPL, and DPL as described above.

Any time an instruction loads a data segment register (DS, ES, FS, GS) the 80376 makes protection validation checks. Selectors loaded in the DS, ES, FS, GS registers must refer only to data segment or readable code segments.

Finally the privilege validation checks are performed. The CPL is compared to the EPL and if the EPL is more privileged than the CPL, an exception 13 (general protection fault) is generated.

The rules regarding the stack segment are slightly different than those involving data segments. Instructions that load selectors into SS must refer to data segment descriptors for writeable data segments. The DPL and RPL must equal the CPL of all other descriptor types or a privilege level violation will cause an exception 13. A stack not present fault causes an exception 12.

PRIVILEGE LEVEL TRANSFERS

Inter-segment control transfers occur when a selector is loaded in the CS register. For a typical system most of these transfers are simply the result of a call or a jump to another routine. There are five types of control transfers which are summarized in Table 3.2. Many of these transfers result in a privilege level transfer. Changing privilege levels is done only by control transfers, using gates, task switches, and interrupt or trap gates.

Control transfers can only occur if the operation which loaded the selector references the correct descriptor type. Any violation of these descriptor usage rules will cause an exception 13.

CALL GATES

Gates provide protected indirect CALLs. One of the major uses of gates is to provide a secure method of privilege transfers within a task. Since the operating system defines all of the gates in a system, it can ensure that all gates only allow entry into a few trusted procedures.

Table 3.2. Descriptor Types Used for Control Transfer

Control Transfer Types	Operation Types	Descriptor Referenced	Descriptor Table
Intersegment within the same privilege level	JMP, CALL, RET, IRET*	Code Segment	GDT/LDT
Intersegment to the same or higher privilege level Interrupt within task may change CPL	CALL	Call Gate	GDT/LDT
	Interrupt Instruction, Exception, External Interrupt	Trap or Interrupt Gate	IDT
Intersegment to a lower privilege level (changes task CPL)	RET, IRET*	Code Segment	GDT/LDT
	CALL, JMP	Task State Segment	GDT
Task Switch	CALL, JMP	Task Gate	GDT/LDT
	IRET** Interrupt Instruction, Exception, External Interrupt	Task Gate	IDT

*NT (Nested Task bit of flag register) = 0
**NT (Nested Task bit of flag register) = 1

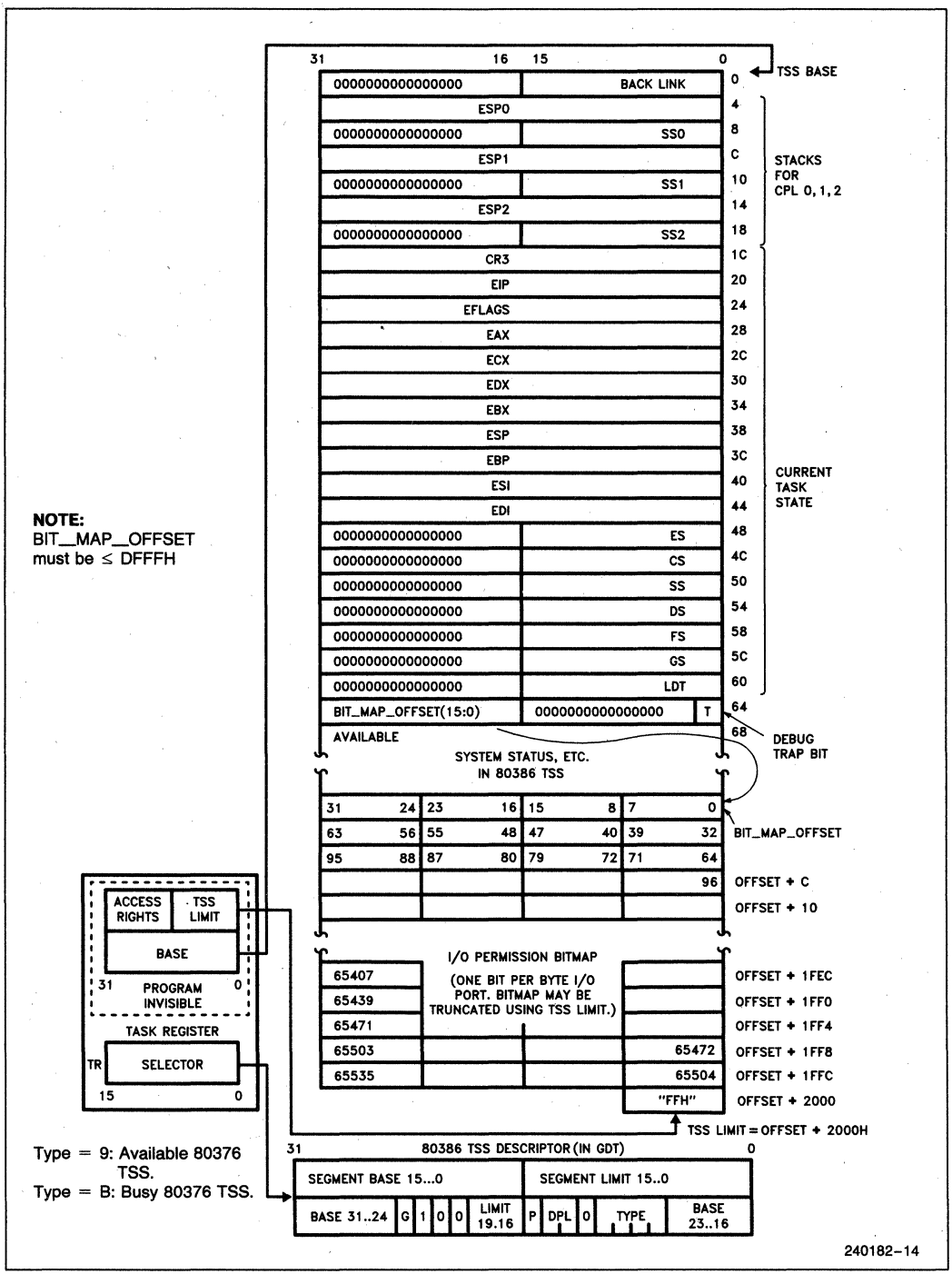


Figure 3.7. 80376 TSS And TSS Registers

TASK SWITCHING

A very important attribute of any multi-tasking operating system is its ability to rapidly switch between tasks or processes. The 80376 directly supports this operation by providing a task switch instruction in hardware. The 80376 task switch operation saves the entire state of the machine (all of the registers, address space, and a link to the previous task), loads a new execution state, performs protection checks, and commences execution in the new task. Like transfer of control by gates, the task switch operation is invoked by executing an inter-segment JMP or CALL instruction which refers to a Task State Segment (TSS), or a task gate descriptor in the GDT or LDT. An INT n instruction, exception, trap or external interrupt may also invoke the task switch operation if there is a task gate descriptor in the associated IDT descriptor slot. For simple applications, the TSS and task switching may not be used. The TSS or task switch will not be used or occur if no task gates are present in the GDT, LDT or IDT.

The TSS descriptor points to a segment (see Figure 3.7) containing the entire 80376 execution state. A task gate descriptor contains a TSS selector. The limit of an 80376 TSS must be greater than 64H, and can be as large as 16 Mbytes. In the additional TSS space, the operating system is free to store additional information as the reason the task is inactive, the time the task has spent running, and open files belonging to the task. For maximum performance, TSS should start on an even address.

Each Task must have a TSS associated with it. The current TSS is identified by a special register in the 80376 called the Task State Segment Register (TR). This register contains a selector referring to the task state segment descriptor that defines the current TSS. A hidden base and limit register associated with the TSS descriptor is loaded whenever TR is loaded with a new selector. Returning from a task is accomplished by the IRET instruction. When IRET is executed, control is returned to the task which was interrupted. The current executing task's state is saved in the TSS and the old task state is restored from its TSS.

Several bits in the flag register and CR0 register give information about the state of a task which is useful to the operating system. The Nested Task bit, NT, controls the function of the IRET instruction. If NT = 0 the IRET instruction performs the regular return. If NT = 1, IRET performs a task switch operation back to the previous task. The NT bit is set or reset in the following fashion:

> When a CALL or INT instruction initiates a task switch, the new TSS will be marked busy and the back link field of the new TSS set to the old TSS selector. The NT bit of the new task is set by CALL or INT initiated task switches. An interrupt that does not cause a task switch will clear NT (The NT bit will be restored after execution of the interrupt handler). NT may also be set or cleared by POPF or IRET instructions.

The 80376 task state segment is marked busy by changing the descriptor type field from TYPE 9 to TYPE 0BH. Use of a selector that references a busy task state segment causes an exception 13.

The coprocessor's state is not automatically saved when a task switch occurs. The Task Switched Bit, TS, in the CR0 register helps deal with the coprocessor's state in a multi-tasking environment. Whenever the 80376 switches tasks, it sets the TS bit. The 80376 detects the first use of a processor extension instruction after a task switch and causes the processor extension not available exception 7. The exception handler for exception 7 may then decide whether to save the state of the coprocessor.

The T bit in the 80376 TSS indicates that the processor should generate a debug exception when switching to a task. If T = 1 then upon entry to a new task a debug exception 1 will be generated.

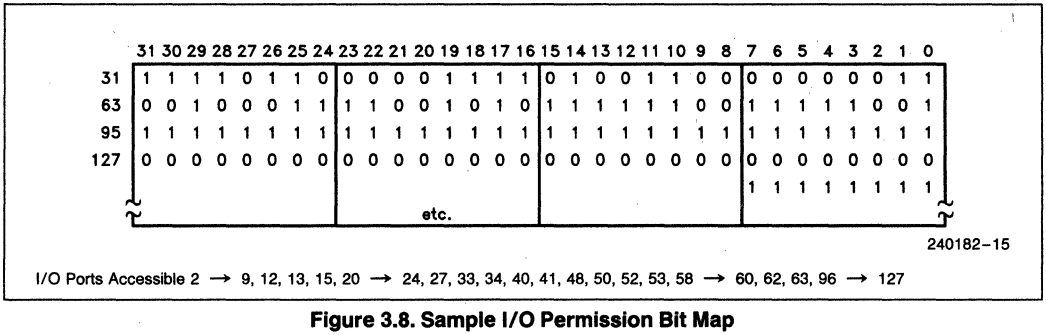


Figure 3.8. Sample I/O Permission Bit Map

PROTECTION AND I/O PERMISSION BIT MAP

The I/O instructions that directly refer to addresses in the processor's I/O space are IN, INS, OUT and OUTS. The 80376 has the ability to selectively trap references to specific I/O addresses. The structure that enables selective trapping is the ***I/O Permission Bit Map*** in the TSS segment (see Figures 3.7 and 3.8). The I/O permission map is a bit vector. The size of the map and its location in the TSS segment are variable. The processor locates the I/O permission map by means of the **I/O map base** field in the fixed portion of the TSS. The **I/O map base** field is 16 bits wide and contains the offset of the beginning of the I/O permission map.

If an I/O instruction (IN, INS, OUT or OUTS) is encountered, the processor first checks whether CPL $\leq$ IOPL. If this condition is true, the I/O operation may proceed. If not true, the processor checks the I/O permission map.

Each bit in the map corresponds to an I/O port byte address; for example, the bit for port 41 is found at **I/O map base** +5 linearly, (5 $\times$ 8 = 40), bit offset 1. The processor tests all the bits that correspond to the I/O addresses spanned by an I/O operation; for example, a double word operation tests four bits corresponding to four adjacent byte addresses. If any tested bit is set, the processor signals a general protection exception. If all the tested bits are zero, the I/O operations may proceed.

It is not necessary for the I/O permission map to represent all the I/O addresses. I/O addresses not spanned by the map are treated as if they had one-bits in the map. The **I/O map base** should be at least one byte less than the TSS limit and the last byte beyond the I/O mapping information must contain all 1's.

Because the I/O permission map is in the TSS segment, different tasks can have different maps. Thus, the operating system can allocate ports to a task by changing the I/O permission map in the task's TSS.

IMPORTANT IMPLEMENTATION NOTE:
Beyond the last byte of I/O mapping information in the I/O permission bit map **must** be a byte containing all 1's. The byte of all 1's must be within the limit of the 80376's TSS segment (see Figure 3.7).

4.0 FUNCTIONAL DATA

The Intel 80376 embedded processor features a straightforward functional interface to the external hardware. The 80376 has separate parallel buses for data and address. The data bus is 16 bits in width, and bidirectional. The address bus outputs 24-bit address values using 23 address lines and two-byte enable signals.

The 80376 has two selectable address bus cycles: pipelined and non-pipelined. The pipelining option allows as much time as possible for data access by

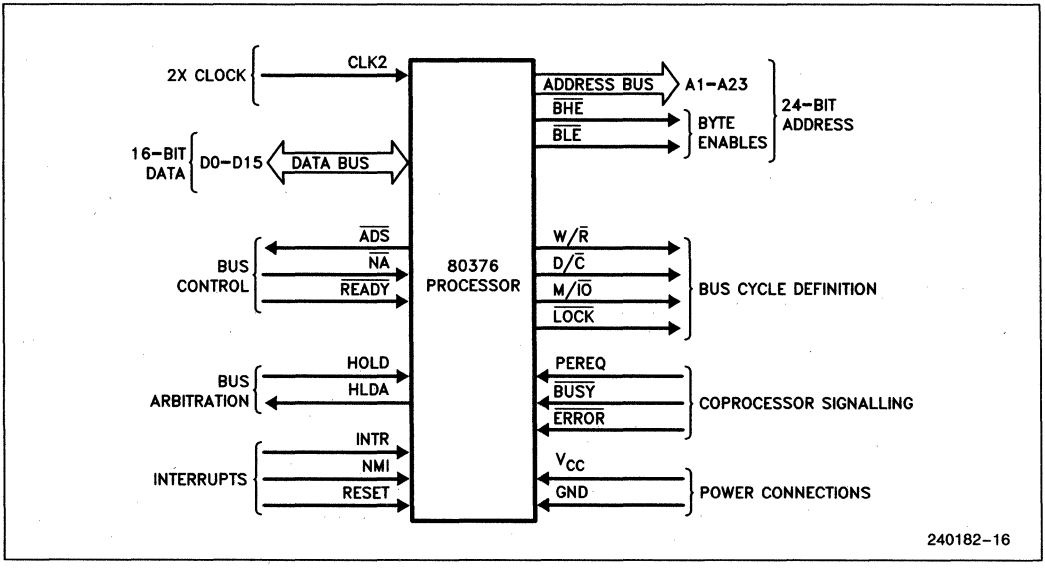


Figure 4.1. Functional Signal Groups

starting the pending bus cycle before the present bus cycle is finished. A non-pipelined bus cycle gives the highest bus performance by executing every bus cycle in two processor clock cycles. For maximum design flexibility, the address pipelining option is selectable on a cycle-by-cycle basis.

The processor's bus cycle is the basic mechanism for information transfer, either from system to processor, or from processor to system. 80376 bus cycles perform data transfer in a minimum of only two clock periods. On a 16-bit data bus, the maximum 80376 transfer bandwidth at 16 MHz is therefore 16 Mbytes/sec. However, any bus cycle will be extended for more than two clock periods if external hardware withholds acknowledgement of the cycle.

The 80376 can relinquish control of its local buses to allow mastership by other devices, such as direct memory access (DMA) channels. When relinquished, HLDA is the only output pin driven by the 80376, providing near-complete isolation of the processor from its system (all other output pins are in a float condition).

4.1 Signal Description Overview

Ahead is a brief description of the 80376 input and output signals arranged by functional groups.

The signal descriptions sometimes refer to A.C. timing parameters, such as "t_{25} Reset Setup Time" and "t_{26} Reset Hold Time." The values of these parameters can be found in Tables 6.4 and 6.5.

CLOCK (CLK2)

CLK2 provides the fundamental timing for the 80376. It is divided by two internally to generate the internal processor clock used for instruction execution. The internal clock is comprised of two

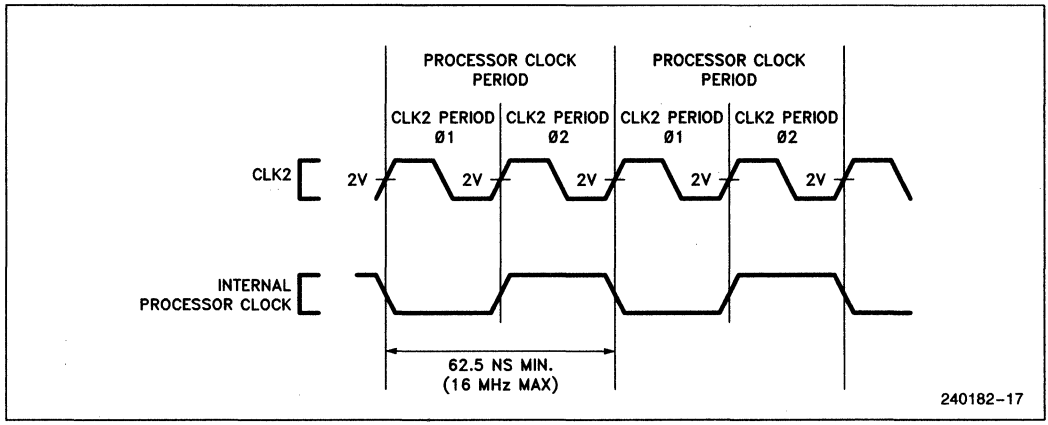


Figure 4.2. CLK2 Signal and Internal Processor Clock

phases, "phase one" and "phase two". Each CLK2 period is a phase of the internal clock. Figure 4.2 illustrates the relationship. If desired, the phase of the internal processor clock can be synchronized to a known phase by ensuring the falling edge of the RESET signal meets the applicable setup and hold times t_{25} and t_{26}.

DATA BUS (D_{15}–D_0)

These three-state bidirectional signals provide the general purpose data path between the 80376 and other devices. The data bus outputs are active HIGH and will float during bus hold acknowledge. Data bus reads require that read-data setup and hold times t_{21} and t_{22} be met relative to CLK2 for correct operation.

ADDRESS BUS ($\overline{BHE}$, $\overline{BLE}$, A_{23}–A_1)

These three-state outputs provide physical memory addresses or I/O port addresses. A_{23}–A_{16} are LOW during I/O transfers except for I/O transfers automatically generated by coprocessor instructions. During coprocessor I/O transfers, A_{22}–A_{16} are driven LOW, and A_{23} is driven HIGH so that this address line can be used by external logic to generate the coprocessor select signal. Thus, the I/O address driven by the 80376 for coprocessor commands is 8000F8H, and the I/O address driven by the 80376 processor for coprocessor data is 8000FCH or 8000FEH.

The address bus is capable of addressing 16 Mbytes of physical memory space (000000H through 0FFFFFFH), and 64 Kbytes of I/O address space (000000H through 00FFFFH) for programmed I/O. The address bus is active HIGH and will float during bus hold acknowledge.

The Byte Enable outputs $\overline{BHE}$ and $\overline{BLE}$ directly indicate which bytes of the 16-bit data bus are involved with the current transfer. $\overline{BHE}$ applies to D_{15}–D_8 and $\overline{BLE}$ applies to D_7–D_0. If both $\overline{BHE}$ and $\overline{BLE}$ are asserted, then 16 bits of data are being transferred. See Table 4.1 for a complete decoding of these signals. The byte enables are active LOW and will float during bus hold acknowledge.

Table 4.1. Byte Enable Definitions

$\overline{BHE}$	$\overline{BLE}$	Function
0	0	Word Transfer
0	1	Byte Transfer on Upper Byte of the Data Bus, D_{15}–D_8
1	0	Byte Transfer on Lower Byte of the Data Bus, D_7–D_0
1	1	Never Occurs

BUS CYCLE DEFINITION SIGNALS (W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$)

These three-state outputs define the type of bus cycle being performed: W/$\overline{R}$ distinguishes between write and read cycles, D/$\overline{C}$ distinguishes between data and control cycles, M/$\overline{IO}$ distinguishes between memory and I/O cycles, and $\overline{LOCK}$ distinguishes between locked and unlocked bus cycles. All of these signals are active LOW and will float during bus acknowledge.

The primary bus cycle definition signals are W/$\overline{R}$, D/$\overline{C}$ and M/$\overline{IO}$, since these are the signals driven valid as $\overline{ADS}$ (Address Status output) becomes active. The $\overline{LOCK}$ signal is driven valid at the same time the bus cycle begins, which due to address pipelining, could be after $\overline{ADS}$ becomes active. Exact bus cycle definitions, as a function of W/$\overline{R}$, D/$\overline{C}$ and M/$\overline{IO}$ are given in Table 4.2.

$\overline{LOCK}$ indicates that other system bus masters are not to gain control of the system bus while it is active. $\overline{LOCK}$ is activated on the CLK2 edge that begins the first locked bus cycle (i.e., it is not active at the same time as the other bus cycle definition pins) and is deactivated when ready is returned to the end of the last bus cycle which is to be locked. The beginning of a bus cycle is determined when $\overline{READY}$ is returned in a previous bus cycle and another is pending ($\overline{ADS}$ is active) or the clock in which $\overline{ADS}$ is driven active if the bus was idle. This means that it follows more closely with the write data rules when it is valid, but may cause the bus to be locked longer than desired. The $\overline{LOCK}$ signal may be explicitly activated by the LOCK prefix on certain instructions. $\overline{LOCK}$ is always asserted when executing the XCHG instruction, during descriptor updates, and during the interrupt acknowledge sequence.

BUS CONTROL SIGNALS ($\overline{ADS}$, $\overline{READY}$, $\overline{NA}$)

The following signals allow the processor to indicate when a bus cycle has begun, and allow other system hardware to control address pipelining and bus cycle termination.

Address Status ($\overline{ADS}$)

This three-state output indicates that a valid bus cycle definition and address (W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{BHE}$, $\overline{BLE}$ and A_{23}–A_1) are being driven at the 80376 pins. $\overline{ADS}$ is an active LOW output. Once $\overline{ADS}$ is driven active, valid address, byte enables, and definition signals will not change. In addition, $\overline{ADS}$ will remain active until its associated bus cycle begins (when $\overline{READY}$ is returned for the previous bus cycle when running pipelined bus cycles). $\overline{ADS}$ will float during bus hold acknowledge. See sections **Non-Pipelined Bus Cycles** and **Pipelined Bus Cycles** for additional information on how $\overline{ADS}$ is asserted for different bus states.

Transfer Acknowledge ($\overline{READY}$)

This input indicates the current bus cycle is complete, and the active bytes indicated by $\overline{BHE}$ and $\overline{BLE}$ are accepted or provided. When $\overline{READY}$ is sampled active during a read cycle or interrupt acknowledge cycle, the 80376 latches the input data and terminates the cycle. When $\overline{READY}$ is sampled active during a write cycle, the processor terminates the bus cycle.

Table 4.2. Bus Cycle Definition

M/$\overline{IO}$	D/$\overline{C}$	W/$\overline{R}$	Bus Cycle Type	Locked?
0	0	0	INTERRUPT ACKNOWLEDGE	Yes
0	0	1	Does Not Occur	—
0	1	0	I/O DATA READ	No
0	1	1	I/O DATA WRITE	No
1	0	0	MEMORY CODE READ	No
1	0	1	HALT: Address = 2, $\overline{BHE}$ = 1, $\overline{BLE}$ = 0 — SHUTDOWN: Address = 0, $\overline{BHE}$ = 1, $\overline{BLE}$ = 0	No
1	1	0	MEMORY DATA READ	Some Cycles
1	1	1	MEMORY DATA WRITE	Some Cycles

$\overline{READY}$ is ignored on the first bus state of all bus cycles, and sampled each bus state thereafter until asserted. $\overline{READY}$ must eventually be asserted to acknowledge every bus cycle, including Halt Indication and Shutdown Indication bus cycles. When being sampled, $\overline{READY}$ must always meet setup and hold times t_{19} and t_{20} for correct operation.

Next Address Request ($\overline{NA}$)

This is used to request pipelining. This input indicates the system is prepared to accept new values of $\overline{BHE}$, $\overline{BLE}$, A_{23}–A_1, W/$\overline{R}$, D/$\overline{C}$ and M/$\overline{IO}$ from the 80376 even if the end of the current cycle is not being acknowledged on $\overline{READY}$. If this input is active when sampled, the next bus cycle's address and status signals are driven onto the bus, provided the next bus request is already pending internally. $\overline{NA}$ is ignored in clock cycles in which $\overline{ADS}$ or $\overline{READY}$ is activated. This signal is active LOW and must satisfy setup and hold times t_{15} and t_{16} for correct operation. See **Pipelined Bus Cycles** and **Read and Write Cycles** for additional information.

BUS ARBITRATION SIGNALS (HOLD, HLDA)

This section describes the mechanism by which the processor relinquishes control of its local buses when requested by another bus master device. See **Entering and Exiting Hold Acknowledge** for additional information.

Bus Hold Request (HOLD)

This input indicates some device other than the 80376 requires bus mastership. When control is granted, the 80376 floats A_{23}–A_1, $\overline{BHE}$, $\overline{BLE}$, D_{15}–D_0, $\overline{LOCK}$, M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$ and $\overline{ADS}$, and then activates HLDA, thus entering the bus hold acknowledge state. The local bus will remain granted to the requesting master until HOLD becomes inactive. When HOLD becomes inactive, the 80376 will deactivate HLDA and drive the local bus (at the same time), thus terminating the hold acknowledge condition.

HOLD must remain asserted as long as any other device is a local bus master. External pull-up resistors may be required when in the hold acknowledge state since none of the 80376 floated outputs have internal pull-up resistors. See **Resistor Recommendations** for additional information. HOLD is not recognized while RESET is active but is recognized during the time between the high-to-low transistion of RESET and the first instruction fetch. If RESET is asserted while HOLD is asserted, RESET has priority and places the bus into an idle state, rather than the hold acknowledge (high-impedance) state.

HOLD is a level-sensitive, active HIGH, synchronous input. HOLD signals must always meet setup and hold times t_{23} and t_{24} for correct operation.

Bus Hold Acknowledge (HLDA)

When active (HIGH), this output indicates the 80376 has relinquished control of its local bus in response to an asserted HOLD signal, and is in the bus Hold Acknowledge state.

The Bus Hold Acknowledge state offers near-complete signal isolation. In the Hold Acknowledge state, HLDA is the only signal being driven by the 80376. The other output signals or bidirectional signals (D_{15}–D_0, $\overline{BHE}$, $\overline{BLE}$, A_{23}–A_1, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$ and $\overline{ADS}$) are in a high-impedance state so the requesting bus master may control them. These pins remain OFF throughout the time that HLDA remains active (see Table 4.3). Pull-up resistors may be desired on several signals to avoid spurious activity when no bus master is driving them. See **Resistor Recommendations** for additional information.

When the HOLD signal is made inactive, the 80376 will deactivate HLDA and drive the bus. One rising edge on the NMI input is remembered for processing after the HOLD input is negated.

Table 4.3. Output Pin State during HOLD

Pin Value	Pin Names
1	HLDA
Float	$\overline{LOCK}$, M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, A_{23}–A_1, $\overline{BHE}$, $\overline{BLE}$, D_{15}–D_0

Hold Latencies

The maximum possible HOLD latency depends on the software being executed. The actual HOLD latency at any time depends on the current bus activity, the state of the $\overline{LOCK}$ signal (internal to the CPU) activated by the $\overline{LOCK}$ prefix, and interrupts. The 80376 will not honor a HOLD request until the current bus operation is complete.

The 80376 breaks 32-bit data or I/O accesses into 2 internally locked 16-bit bus cycles; the $\overline{LOCK}$ signal is not asserted. The 80376 breaks unaligned 16-bit or 32-bit data or I/O accesses into 2 or 3 internally locked 16-bit bus cycles. Again the $\overline{LOCK}$ signal is not asserted but a HOLD request will not be recognized until the end of the entire transfer.

Wait states affect HOLD latency. The 80376 will not honor a HOLD request until the end of the current bus operation, no matter how many wait states are required. Systems with DMA where data transfer is critical must insure that $\overline{\text{READY}}$ returns sufficiently soon.

COPROCESSOR INTERFACE SIGNALS (PEREQ, $\overline{\text{BUSY}}$, $\overline{\text{ERROR}}$)

In the following sections are descriptions of signals dedicated to the numeric coprocessor interface. In addition to the data bus, address bus, and bus cycle definition signals, these following signals control communication between the 80376 and the 80387SX processor extension.

Coprocessor Request (PEREQ)

When asserted (HIGH), this input signal indicates a coprocessor request for a data operand to be transferred to/from memory by the 80376. In response, the 80376 transfers information between the coprocessor and memory. Because the 80376 has internally stored the coprocessor opcode being executed, it performs the requested data transfer with the correct direction and memory address.

PEREQ is a level-sensitive active HIGH asynchronous signal. Setup and hold times, t_{29} and t_{30}, relative to the CLK2 signal must be met to guarantee recognition at a particular clock edge. This signal is provided with a weak internal pull-down resistor of around 20 KΩ to ground so that it will not float active when left unconnected.

Coprocessor Busy ($\overline{\text{BUSY}}$)

When asserted (LOW), this input indicates the coprocessor is still executing an instruction, and is not yet able to accept another. When the 80376 encounters any coprocessor instruction which operates on the numerics stack (e.g. load, pop, or arithmetic operation), or the WAIT instruction, this input is first automatically sampled until it is seen to be inactive. This sampling of the $\overline{\text{BUSY}}$ input prevents overrunning the execution of a previous coprocessor instruction.

The F(N)INIT, F(N)CLEX coprocessor instructions are allowed to execute even if $\overline{\text{BUSY}}$ is active, since these instructions are used for coprocessor initialization and exception-clearing.

$\overline{\text{BUSY}}$ is an active LOW, level-sensitive asynchronous signal. Setup and hold times, t_{29} and t_{30}, relative to the CLK2 signal must be met to guarantee recognition at a particular clock edge. This pin is provided with a weak internal pull-up resistor of around 20 KΩ to V_{CC} so that it will not float active when left unconnected.

$\overline{\text{BUSY}}$ serves an additional function. If $\overline{\text{BUSY}}$ is sampled LOW at the falling edge of RESET, the 80376 processor performs an internal self-test (see **Bus Activity During and Following Reset.** If $\overline{\text{BUSY}}$ is sampled HIGH, no self-test is performed.

Coprocessor Error ($\overline{\text{ERROR}}$)

When asserted (LOW), this input signal indicates that the previous coprocessor instruction generated a coprocessor error of a type not masked by the coprocessor's control register. This input is automatically sampled by the 80376 when a coprocessor instruction is encountered, and if active, the 80376 generates exception 16 to access the error-handling software.

Several coprocessor instructions, generally those which clear the numeric error flags in the coprocessor or save coprocessor state, do execute without the 80376 generating exception 16 even if $\overline{\text{ERROR}}$ is active. These instructions are FNINIT, FNCLEX, FNSTSW, FNSTSWAX, FNSTCW, FNSTENV and FNSAVE.

$\overline{\text{ERROR}}$ is an active LOW, level-sensitive asynchronous signal. Setup and hold times t_{29} and t_{30}, relative to the CLK2 signal must be met to guarantee recognition at a particular clock edge. This pin is provided with a weak internal pull-up resistor of around 20 KΩ to V_{CC} so that it will not float active when left unconnected.

INTERRUPT SIGNALS (INTR, NMI, RESET)

The following descriptions cover inputs that can interrupt or suspend execution of the processor's current instruction stream.

Maskable Interrupt Request (INTR)

When asserted, this input indicates a request for interrupt service, which can be masked by the 80376 Flag Register IF bit. When the 80376 responds to the INTR input, it performs two interrupt acknowledge bus cycles and, at the end of the second, latches an 8-bit interrupt vector on D_7-D_0 to identify the source of the interrupt.

INTR is an active HIGH, level-sensitive asynchronous signal. Setup and hold times, t_{27} and t_{28}, relative to the CLK2 signal must be met to guarantee recognition at a particular clock edge. To assure recognition of an INTR request, INTR should remain active until the first interrupt acknowledge bus cycle begins. INTR is sampled at the beginning of every instruction. In order to be recognized at a particular instruction boundary, INTR must be active at least eight CLK2 clock periods before the beginning of the execution of the instruction. If recognized, the 80376 will begin execution of the interrupt.

Non-Maskable Interrupt Request (NMI)

This input indicates a request for interrupt service which cannot be masked by software. The non-maskable interrupt request is always processed according to the pointer or gate in slot 2 of the interrupt table. Because of the fixed NMI slot assignment, no interrupt acknowledge cycles are performed when processing NMI.

NMI is an active HIGH, rising edge-sensitive asynchronous signal. Setup and hold times, t_{27} and t_{28}, relative to the CLK2 signal must be met to guarantee recognition at a particular clock edge. To assure recognition of NMI, it must be inactive for at least eight CLK2 periods, and then be active for at least eight CLK2 periods before the beginning of the execution of an instruction.

Once NMI processing has begun, no additional NMI's are processed until after the next IRET instruction, which is typically the end of the NMI service routine. If NMI is re-asserted prior to that time, however, one rising edge on NMI will be remembered for processing after executing the next IRET instruction.

Interrupt Latency

The time that elapses before an interrupt request is serviced (interrupt latency) varies according to several factors. This delay must be taken into account by the interrupt source. Any of the following factors can affect interrupt latency:

1. If interrupts are masked, and INTR request will not be recognized until interrupts are reenabled.
2. If an NMI is currently being serviced, an incoming NMI request will not be recognized until the 80376 encounters the IRET instruction.
3. An interrupt request is recognized only on an instruction boundary of the 80376 ***Execution Unit*** except for the following cases:
   - — Repeat string instructions can be interrupted after each iteration.
   - — If the instruction loads the Stack Segment register, an interrupt is not processed until after the following instruction, which should be an ESP load. This allows the entire stack pointer to be loaded without interruption.
   - — If an instruction sets the interrupt flag (enabling interrupts), an interrupt is not processed until after the next instruction.

   The longest latency occurs when the interrupt request arrives while the 80376 processor is executing a long instruction such as multiplication, division or a task-switch.
4. Saving the Flags register and CS:EIP registers.
5. If interrupt service routine requires a task switch, time must be allowed for the task switch.
6. If the interrupt service routine saves registers that are not automatically saved by the 80376.

RESET

This input signal suspends any operation in progress and places the 80376 in a known reset state. The 80376 is reset by asserting RESET for 15 or more CLK2 periods (80 or more CLK2 periods before requesting self-test). When RESET is active, all other input pins except $\overline{FLT}$ are ignored, and all other bus pins are driven to an idle bus state as shown in Table 4.4. If RESET and HOLD are both active at a point in time, RESET takes priority even if the 80376 was in a Hold Acknowledge state prior to RESET active.

RESET is an active HIGH, level-sensitive synchronous signal. Setup and hold times, t_{25} and t_{26}, must be met in order to assure proper operation of the 80376.

Table 4.4. Pin State (Bus Idle) during RESET

Pin Name	Signal Level during RESET
$\overline{ADS}$	1
$D_{15}-D_0$	Float
$\overline{BHE}$, $\overline{BLE}$	0
$A_{23}-A_1$	1
W/$\overline{R}$	0
D/$\overline{C}$	1
M/$\overline{IO}$	0
$\overline{LOCK}$	1
HLDA	0

4.2 Bus Transfer Mechanism

All data transfers occur as a result of one or more bus cycles. Logical data operands of byte and word lengths may be transferred without restrictions on physical address alignment. Any byte boundary may be used, although two physical bus cycles are performed as required for unaligned operand transfers.

The 80376 processor address signals are designed to simplify external system hardware. $\overline{BHE}$ and $\overline{BLE}$ provide linear selects for the two bytes of the 16-bit data bus.

Byte Enable outputs $\overline{BHE}$ and $\overline{BLE}$ are asserted when their associated data bus bytes are involved with the present bus cycle, as listed in Table 4.5.

Table 4.5. Byte Enables and Associated Data and Operand Bytes

Byte Enable	Associated Data Bus Signals
$\overline{BHE}$	$D_{15}-D_8$ (Byte 1—Most Significant)
$\overline{BLE}$	D_7-D_0 (Byte 0—Least Significant)

Each bus cycle is composed of at least two bus states. Each bus state requires one processor clock period. Additional bus states added to a single bus cycle are called wait states. See **Bus Functional Description** for additional information.

4.3 Memory and I/O Spaces

Bus cycles may access physical memory space or I/O space. Peripheral devices in the system may either be memory-mapped, or I/O-mapped, or both. As shown in Figure 4.3, physical memory addresses range from 000000H to 0FFFFFFH (16 Mbytes) and I/O addresses from 000000H to 00FFFFH (64 Kbytes). Note the I/O addresses used by the automatic I/O cycles for coprocessor communication are 8000F8H to 8000FFH, beyond the address range of programmed I/O, to allow easy generation of a coprocessor chip select signal using the A_{23} and M/$\overline{IO}$ signals.

OPERAND ALIGNMENT

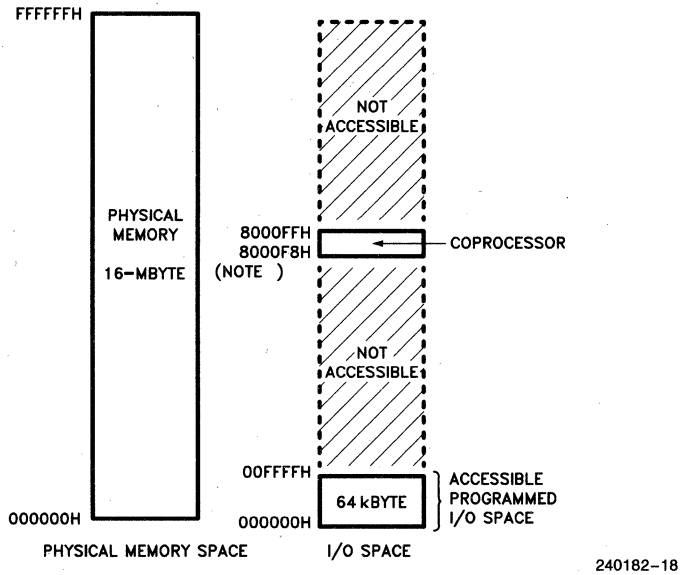
With the flexibility of memory addressing on the 80376, it is possible to transfer a logical operand that spans more than one physical Dword or word of memory or I/O. Examples are 32-bit Dword or 16-bit word operands beginning at addresses not evenly divisible by 2.

Operand alignment and size dictate when multiple bus cycles are required. Table 4.6 describes the transfer cycles generated for all combinations of logical operand lengths and alignment.

Table 4.6. Transfer Bus Cycles for Bytes, Words and Dwords

	Byte-Length of Logical Operand								
	1	2				4			
Physical Byte Address in Memory (Low-Order Bits)	xx	00	01	10	11	00	01	10	11
Transfer Cycles	b	w	lb, hb	w	hb, l,b	lw, hw	hb, lb, mw	hw, lw	mw, hb, lb

Key: b = byte transfer
w = word transfer
l = low-order portion
m = mid-order portion
x = don't care
h = high-order portion



NOTE:
Since A_{23} is HIGH during automatic communication with coprocessor, A_{23} HIGH and M/$\overline{IO}$ LOW can be used to easily generate a coprocessor select signal.

Figure 4.3. Physical Memory and I/O Spaces

4.4 Bus Functional Description

The 80376 has separate, parallel buses for data and address. The data bus is 16 bits in width, and bidirectional. The address bus provides a 24-bit value using 23 signals for the 23 upper-order address bits and 2 Byte Enable signals to directly indicate the active bytes. These buses are interpreted and controlled by several definition signals.

The definition of each bus cycle is given by three signals: M/$\overline{IO}$, W/$\overline{R}$ and D/$\overline{C}$. At the same time, a valid address is present on the byte enable signals, $\overline{BHE}$ and $\overline{BLE}$, and the other address signals A_{23}–A_1. A status signal, $\overline{ADS}$, indicates when the 80376 issues a new bus cycle definition and address.

Collectively, the address bus, data bus and all associated control signals are referred to simply as "the bus". When active, the bus performs one of the bus cycles below:

1. Read from memory space
2. Locked read from memory space
3. Write to memory space
4. Locked write to memory space
5. Read from I/O space (or coprocessor)
6. Write to I/O space (or coprocessor)
7. Interrupt acknowledge (always locked)
8. Indicate halt, or indicate shutdown

Table 4.2 shows the encoding of the bus cycle definition signals for each bus cycle. See **Bus Cycle Definition Signals** for additonal information.

When the 80376 bus is not performing one of the activities listed above, it is either Idle or in the Hold Acknowledge state, which may be detected by external circuitry. The idle state can be identified by the 80376 giving no further assertions on its address strobe output ($\overline{ADS}$) since the beginning of its most recent bus cycle, and the most recent bus cycle having been terminated. The hold acknowledge state is identified by the 80376 asserting its hold acknowledge (HLDA) output.

The shortest time unit of bus activity is a bus state. A bus state is one processor clock period (two CLK2 periods) in duration. A complete data transfer occurs during a bus cycle, composed of two or more bus states.

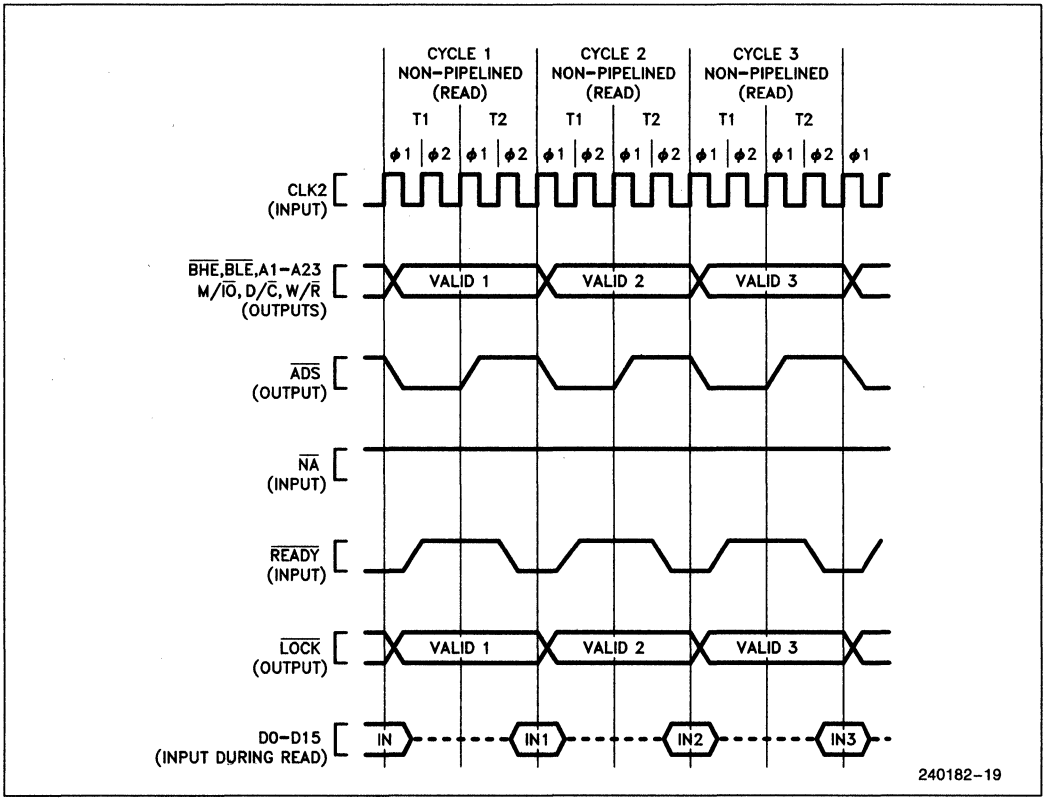


Figure 4.4. Fastest Read Cycles with Non-Pipelined Timing

The fastest 80376 bus cycle requires only two bus states. For example, three consecutive bus read cycles, each consisting of two bus states, are shown by Figure 4.4. The bus states in each cycle are named T1 and T2. Any memory or I/O address may be accessed by such a two-state bus cycle, if the external hardware is fast enough.

Every bus cycle continues until it is acknowledged by the external system hardware, using the 80376 $\overline{\text{READY}}$ input. Acknowledging the bus cycle at the end of the first T2 results in the shortest bus cycle, requiring only T1 and T2. If $\overline{\text{READY}}$ is not immediately asserted however, T2 states are repeated indefinitely until the $\overline{\text{READY}}$ input is sampled active.

The pipelining option provides a choice of bus cycle timings. Pipelined or non-pipelined cycles are selectable on a cycle-by-cycle basis with the Next Address ($\overline{\text{NA}}$) input.

When pipelining is selected the address ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ and A_{23}–A_1) and definition (W/$\overline{\text{R}}$, D/$\overline{\text{C}}$, M/$\overline{\text{IO}}$ and $\overline{\text{LOCK}}$) of the next cycle are available before the end of the current cycle. To signal their availability, the 80376 address status output ($\overline{\text{ADS}}$) is asserted. Figure 4.5 illustrates the fastest read cycles with pipelined timing.

Note from Figure 4.5 the fastest bus cycles using pipelining require only two bus states, named **T1P** and **T2P**. Therefore pipelined cycles allow the same data bandwidth as non-pipelined cycles, but address-to-data access time is increased by one T-state time compared to that of a non-pipelined cycle.

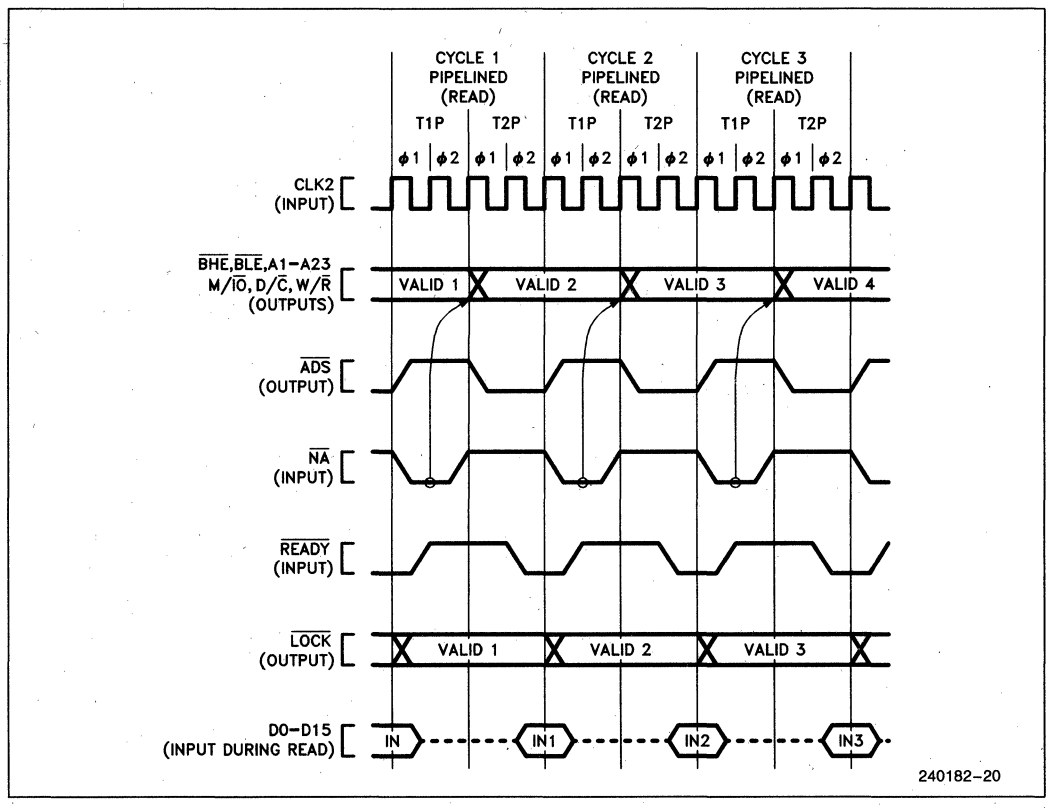


Figure 4.5. Fastest Read Cycles with Pipelined Timing

READ AND WRITE CYCLES

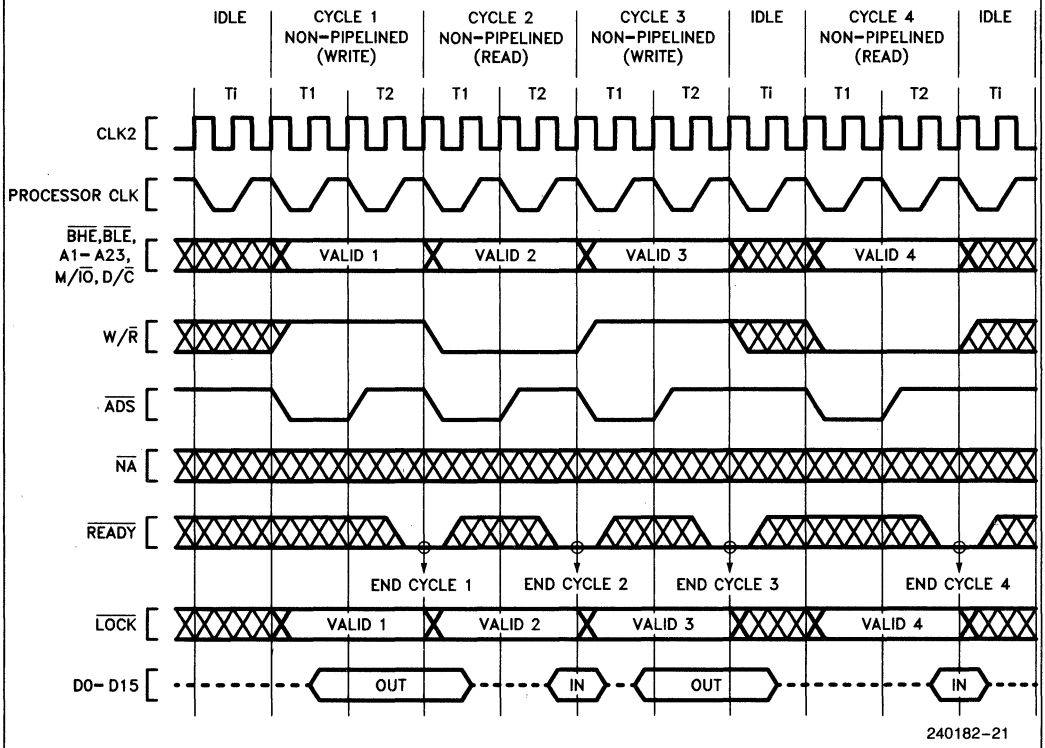
Data transfers occur as a result of bus cycles, classified as read or write cycles. During read cycles, data is transferred from an external device to the processor. During write cycles, data is transferred from the processor to an external device.

Two choices of bus cycle timing are dynamically selectable: non-pipelined or pipelined. After an idle bus state, the processor always uses non-pipelined timing. However the $\overline{NA}$ (Next Address) input may be asserted to select pipelined timing for the next bus cycle. When pipelining is selected and the 80376 has a bus request pending internally, the address and definition of the next cycle is made available even before the current bus cycle is acknowledged by $\overline{READY}$.

Terminating a read or write cycle, like any bus cycle, requires acknowledging the cycle by asserting the $\overline{READY}$ input. Until acknowledged, the processor inserts wait states into the bus cycle, to allow adjustment for the speed of any external device. External hardware, which has decoded the address and bus cycle type, asserts the $\overline{READY}$ input at the appropriate time.

At the end of the second bus state within the bus cycle, $\overline{READY}$ is sampled. At that time, if external hardware acknowledges the bus cycle by asserting $\overline{READY}$, the bus cycle terminates as shown in Figure 4.6. If $\overline{READY}$ is negated as in Figure 4.7, the 80376 executes another bus state (a wait state) and $\overline{READY}$ is sampled again at the end of that state. This continues indefinitely until the cycle is acknowledged by $\overline{READY}$ asserted.

When the current cycle is acknowledged, the 80376 terminates it. When a read cycle is acknowledged, the 80376 latches the information present at its data pins. When a write cycle is acknowledged, the write data of the 80376 remains valid throughout phase one of the next bus state, to provide write data hold time.



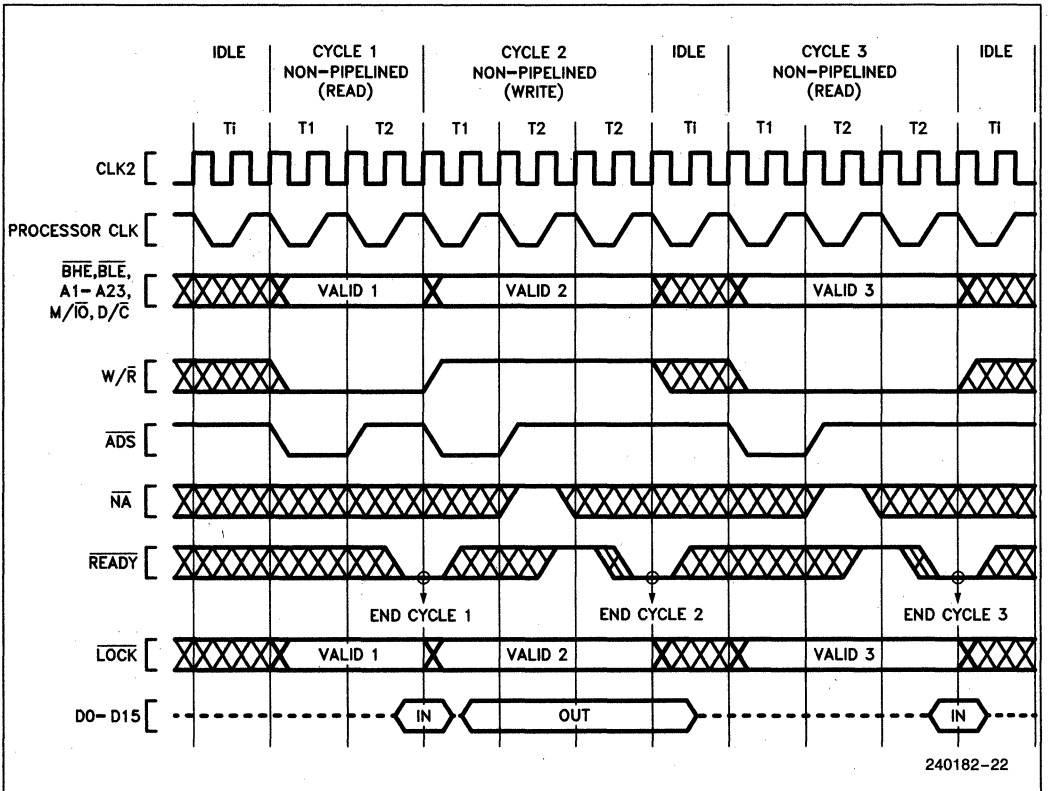
Idle states are shown here for diagram variety only. Write cycles are not always followed by an idle state. An active bus cycle can immediately follow the write cycle.

Figure 4.6. Various Non-Pipelined Bus Cycles (Zero Wait States)

Non-Pipelined Bus Cycles

Any bus cycle may be performed with non-pipelined timing. For example, Figure 4.6 shows a mixture of non-pipelined read and write cycles. Figure 4.6 shows that the fastest possible non-pipelined cycles have two bus states per bus cycle. The states are named T1 and T2. In phase one of T1, the address signals and bus cycle definition signals are driven valid and, to signal their availability, address strobe ($\overline{ADS}$) is simultaneously asserted.

During read or write cycles, the data bus behaves as follows. If the cycle is a read, the 80376 floats its data signals to allow driving by the external device being addressed. **The 80376 requires that all data bus pins be at a valid logic state (HIGH or LOW) at the end of each read cycle, when $\overline{READY}$ is asserted. The system MUST be designed to meet this requirement.** If the cycle is a write, data signals are driven by the 80376 beginning in phase two of T1 until phase one of the bus state following cycle acknowledgement.



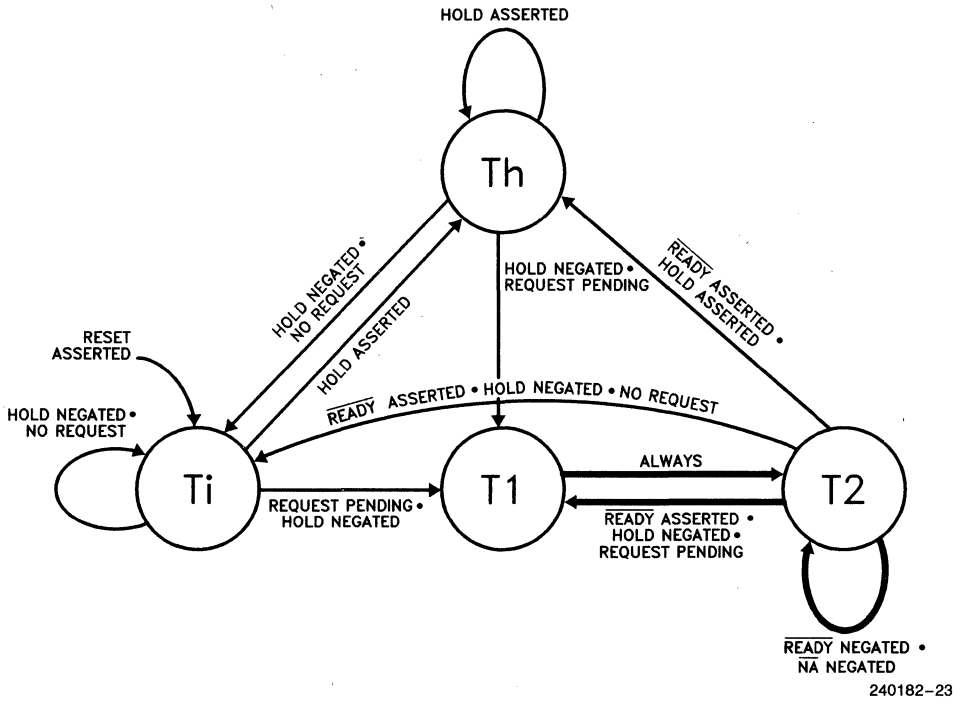
Idle states are shown here for diagram variety only. Write cycles are not always followed by an idle state. An active bus cycle can immediately follow the write cycle.

Figure 4.7. Various Non-Pipelined Bus Cycles (Various Number of Wait States)

Figure 4.7 illustrates non-pipelined bus cycles with one wait state added to Cycles 2 and 3. $\overline{READY}$ is sampled inactive at the end of the first T2 in Cycles 2 and 3. Therefore Cycles 2 and 3 have T2 repeated again. At the end of the second T2, $\overline{READY}$ is sampled active.

When address pipelining is not used, the address and bus cycle definition remain valid during all wait states. When wait states are added and it is desirable to maintain non-pipelined timing, it is necessary to negate $\overline{NA}$ during each T2 state except the last one, as shown in Figure 4.7, Cycles 2 and 3. If $\overline{NA}$ is sampled active during a T2 other than the last one, the next state would be T2I or T2P instead of another T2.

When address pipelining is not used, the bus states and transitions are completely illustrated by Figure 4.8. The bus transitions between four possible states, T1, T2, T_i, and T_h. Bus cycles consist of T1 and T2, with T2 being repeated for wait states. Otherwise the bus may be idle, T_i, or in the hold acknowledge state T_h.



Bus States:
T1—first clock of a non-pipelined bus cycle (80376 drives new address and asserts $\overline{ADS}$).
T2—subsequent clocks of a bus cycle when $\overline{NA}$ has not been sampled asserted in the current bus cycle.
Ti—idle state.
Th—hold acknowledge state (80376 asserts HLDA).
The fastest bus cycle consists of two states: T1 and T2.
Four basic bus states describe bus operation when not using pipelined address.

Figure 4.8. 80376 Bus States (Not Using Pipelined Address)

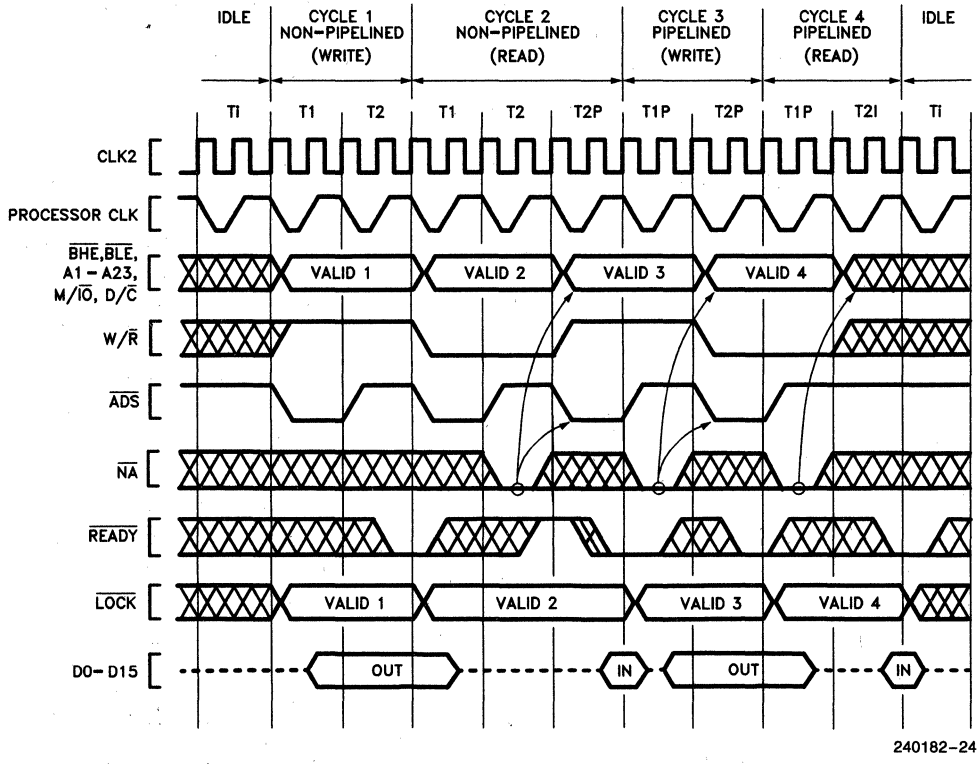
Bus cycles always begin with T1. T1 always leads to T2. If a bus cycle is not acknowledged during T2 and $\overline{NA}$ is inactive, T2 is repeated. When a cycle is acknowledged during T2, the following state will be T1 of the next bus cycle if a bus request is pending internally, or T_i if there is no bus request pending, or T_h if the HOLD input is being asserted.

Use of pipelining allows the 80376 to enter three additional bus states not shown in Figure 4.8. Figure 4.12 is the complete bus state diagram, including pipelined cycles.

Pipelined Bus Cycles

Pipelining is the option of requesting the address and the bus cycle definition of the next internally pending bus cycle before the current bus cycle is acknowledged with $\overline{READY}$ asserted. $\overline{ADS}$ is asserted by the 80376 when the next address is issued. The pipelining option is controlled on a cycle-by-cycle basis with the $\overline{NA}$ input signal.

Once a bus cycle is in progress and the current address has been valid for at least one entire bus state, the $\overline{NA}$ input is sampled at the end of every phase one until the bus cycle is acknowledged. During non-pipelined bus cycles $\overline{NA}$ is sampled at the end of phase one in every T2. An example is Cycle 2 in Figure 4.9, during which $\overline{NA}$ is sampled at the end of phase one of every T2 (it was asserted once during the first T2 and has no further effect during that bus cycle).



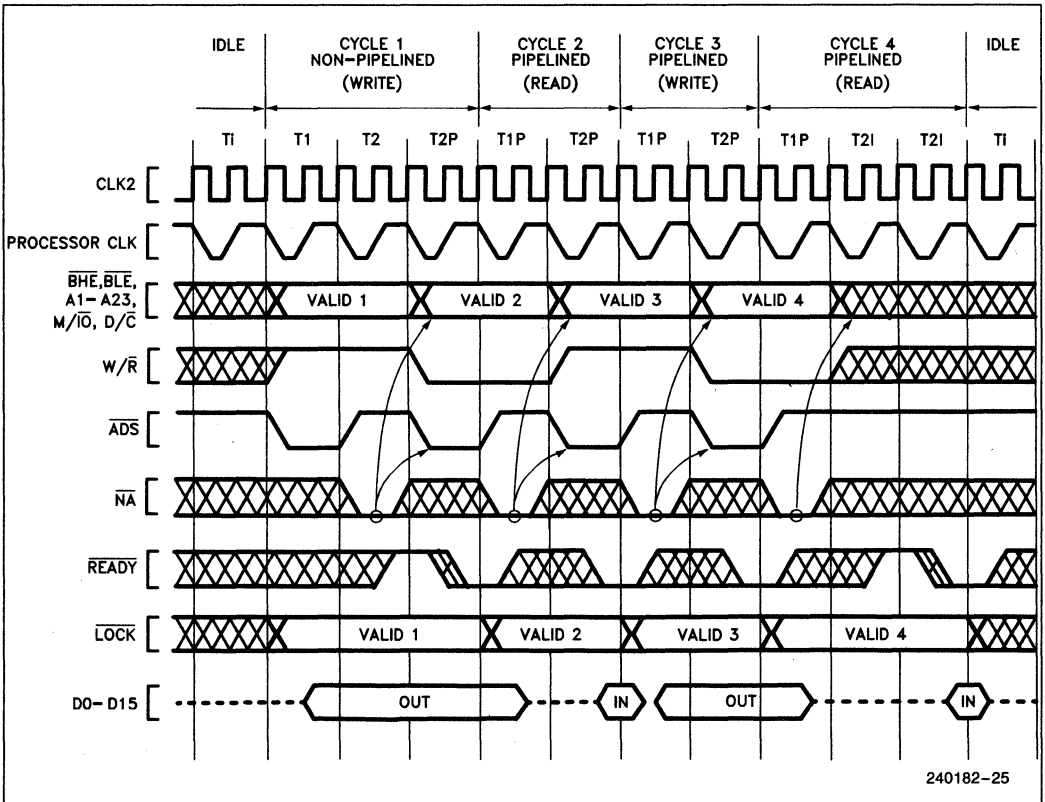
Following any idle bus state (Ti), bus cycles are non-pipelined. Within non-pipelined bus cycles, $\overline{NA}$ is only sampled during wait states. Therefore, to begin pipelining during a group of non-pipelined bus cycles requires a non-pipelined cycle with at least one wait state (Cycle 2 above).

Figure 4.9. Transitioning to Pipelining during Burst of Bus Cycles

If $\overline{NA}$ is sampled active, the 80376 is free to drive the address and bus cycle definition of the next bus cycle, and assert $\overline{ADS}$, as soon as it has a bus request internally pending. It may drive the next address as early as the next bus state, whether the current bus cycle is acknowledged at that time or not.

Regarding the details of pipelining, the 80376 has the following characteristics:

1. The next address and status may appear as early as the bus state after $\overline{NA}$ was sampled active (see Figures 4.9 or 4.10). In that case, state T2P is entered immediately. However, when there is not an internal bus request already pending, the next address and status will not be available immediately after $\overline{NA}$ is asserted and T2I is entered instead of T2P (see Figure 4.11 Cycle 3). Provided the current bus cycle isn't yet acknowledged by $\overline{READY}$ asserted, T2P will be entered as soon as the 80376 does drive the next address and status. External hardware should therefore observe the $\overline{ADS}$ output as confirmation the next address and status are actually being driven on the bus.
2. Any address and status which are validated by a pulse on the 80376 $\overline{ADS}$ output will remain stable on the address pins for at least two processor clock periods. The 80376 cannot produce a new address and status more frequently than every two processor clock periods (see Figures 4.9, 4.10 and 4.11).
3. Only the address and bus cycle definition of the very next bus cycle is available. The pipelining capability cannot look further than one bus cycle ahead (see Figure 4.11, Cycle 1).



Following any idle bus state (Ti) the bus cycle is always non-pipelined and $\overline{NA}$ is only sampled during wait states. To start, address pipelining after an idle state requires a non-pipelined cycle with at least one wait state (cycle 1 above). The pipelined cycles (2, 3, 4 above) are shown with various numbers of wait states.

Figure 4.10. Fastest Transition to Pipelined Bus Cycle Following Idle Bus State

The complete bus state transition diagram, including pipelining is given by Figure 4.12. Note it is a superset of the diagram for non-pipelined only, and the three additional bus states for pipelining are drawn in bold.

The fastest bus cycle with pipelining consists of just two bus states, T1P and T2P (recall for non-pipelined it is T1 and T2). T1P is the first bus state of a pipelined cycle.

Initiating and Maintaining Pipelined Bus Cycles

Using the state diagram Figure 4.12, observe the transitions from an idle state, T_i, to the beginning of a pipelined bus cycle T1P. From an idle state, T_i, the first bus cycle must begin with T1, and is therefore a non-pipelined bus cycle. The next bus cycle will be pipelined, however, provided $\overline{NA}$ is asserted and the first bus cycle ends in a T2P state (the address and status for the next bus cycle is driven during T2P). The fastest path from an idle state to a pipelined bus cycle is shown in bold below:

T_i, T_i,	**T1-T2-T2P,**	**T1P-T2P,**
idle states	non-pipelined cycle	pipelined cycle

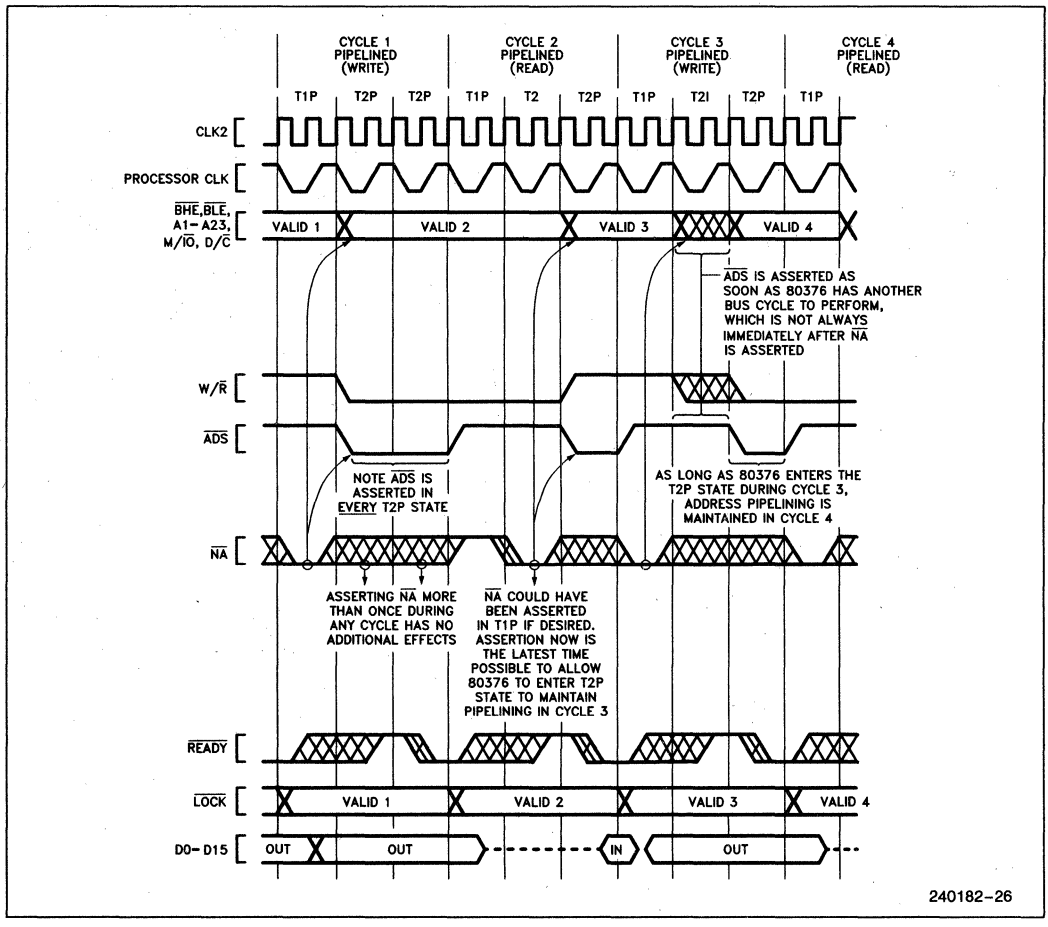


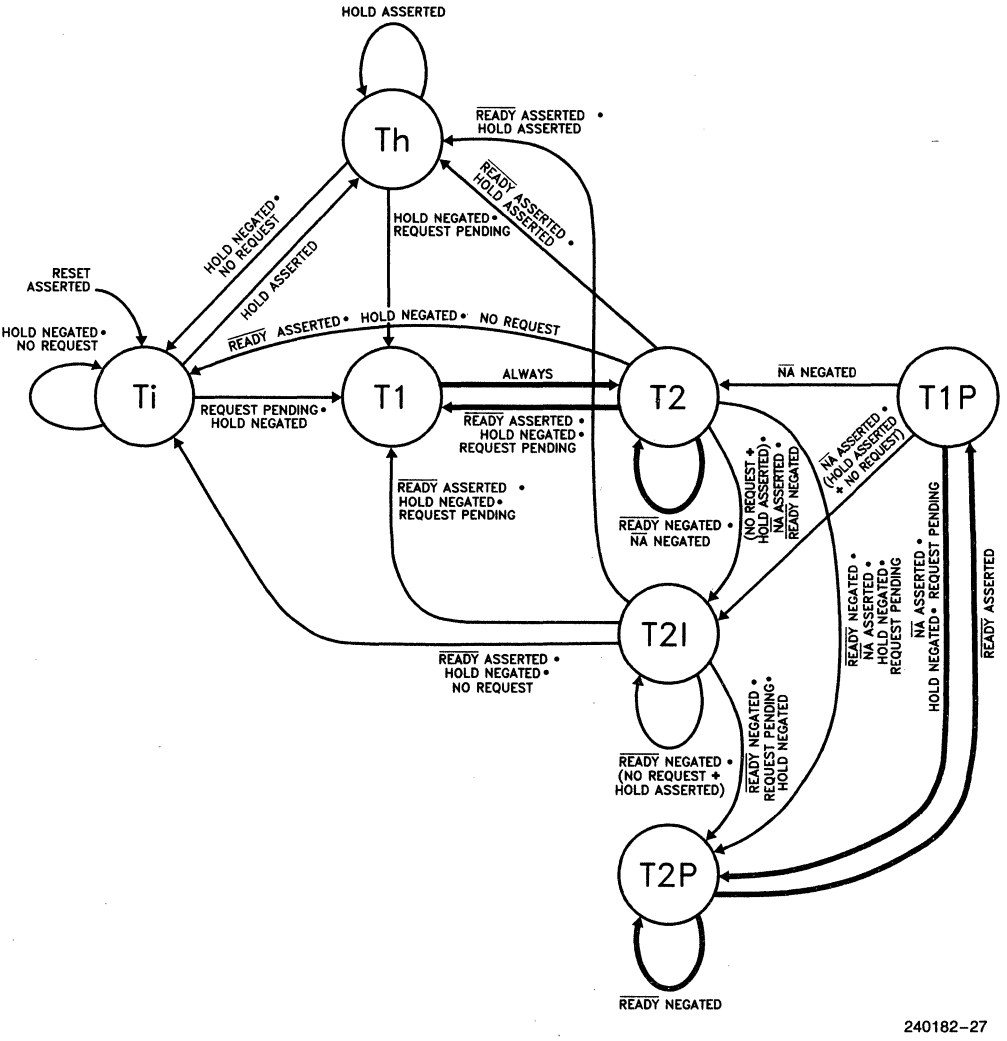
Figure 4.11. Details of Address Pipelining during Cycles with Wait States

T1–T2–T2P are the states of the bus cycle that establishes address pipelining for the next bus cycle, which begins with T1P. The same is true after a bus hold state, shown below:

T_h, T_h, T_h,	T1–T2–T2P,	T1P–T2P,
hold aknowledge states	non-pipelined cycle	pipelined cycle

The transition to pipelined address is shown functionally by Figure 4.10, Cycle 1. Note that Cycle 1 is used to transition into pipelined address timing for the subsequent Cycles 2, 3 and 4, which are pipelined. The $\overline{NA}$ input is asserted at the appropriate time to select address pipelining for Cycles 2, 3 and 4.

Once a bus cycle is in progress and the current address and status has been valid for one entire bus state, the $\overline{NA}$ input is sampled at the end of every phase one until the bus cycle is acknowledged.



Bus States:

T1—first clock of a non-pipelined bus cycle (80376 drives new address, status and asserts $\overline{ADS}$).
T2—subsequent clocks of a bus cycle when $\overline{NA}$ has not been sampled asserted in the current bus cycle.
T2I—subsequent clocks of a bus cycle when $\overline{NA}$ has been sampled asserted in the current bus cycle but there is not yet an internal bus request pending (80376 will not drive new address, status or assert $\overline{ADS}$).
T2P—subsequent clocks of a bus cycle when $\overline{NA}$ has been sampled asserted in the current bus cycle and there is an internal bus request pending (80376 drives new address, status and asserts $\overline{ADS}$).
T1P—first clock of a pipelined bus cycle.
Ti—idle state.
Th—hold acknowledge state (80376 asserts HLDA).

Asserting $\overline{NA}$ for pipelined bus cycles gives access to three more bus states: T2I, T2P and T1P.
Using pipelining the fastest bus cycle consists of T1P and T2P.

Figure 4.12. 80376 Processor Complete Bus States (Including Pipelining)

Sampling begins in T2 during Cycle 1 in Figure 4.10. Once $\overline{NA}$ is sampled active during the current cycle, the 80376 is free to drive a new address and bus cycle definition on the bus as early as the next bus state. In Figure 4.10, Cycle 1 for example, the next address and status is driven during state T2P. Thus Cycle 1 makes the transition to pipelined timing, since it begins with T1 but ends with T2P. Because the address for Cycle 2 is available before Cycle 2 begins, Cycle 2 is called a pipelined bus cycle, and it begins with T1P. Cycle 2 begins as soon as $\overline{READY}$ asserted terminates Cycle 1.

Examples of transition bus cycles are Figure 4.10, Cycle 1 and Figure 4.9, Cycle 2. Figure 4.10 shows transition during the very first cycle after an idle bus state, which is the fastest possible transition into address pipelining. Figure 4.9, Cycle 2 shows a transition cycle occurring during a burst of bus cycles. In any case, a transition cycle is the same whenever it occurs: it consists at least of T1, T2 ($\overline{NA}$ is asserted at that time), and T2P (provided the 80376 has an internal bus request already pending, which it almost always has). T2P states are repeated if wait states are added to the cycle.

Note that only three states (T1, T2 and T2P) are required in a bus cycle performing a **transition** from non-pipelined into pipelined timing, for example Figure 4.10, Cycle 1. Figure 4.10, Cycles 2, 3 and 4 show that pipelining can be maintained with two-state bus cycles consisting only of T1P and T2P.

Once a pipelined bus cycle is in progress, pipelined timing is maintained for the next cycle by asserting $\overline{NA}$ and detecting that the 80376 enters T2P during the current bus cycle. The current bus cycle must end in state T2P for pipelining to be maintained in the next cycle. T2P is identified by the assertion of $\overline{ADS}$. Figures 4.9 and 4.10 however, each show pipelining ending after Cycle 4 because Cycle 4 ends in T2I. This indicates the 80376 didn't have an internal bus request prior to the acknowledgement of Cycle 4. If a cycle ends with a T2 or T2I, the next cycle will not be pipelined.

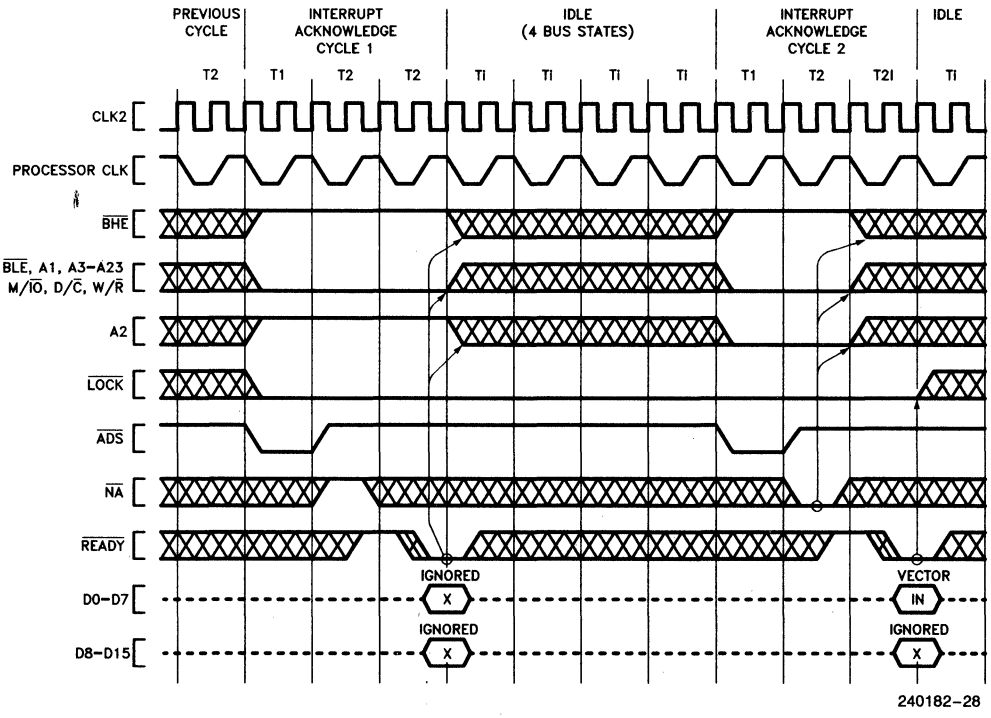
Realistically, pipelining is almost always maintained as long as $\overline{NA}$ is sampled asserted. This is so because in the absence of any other request, a code prefetch request is always internally pending until the instruction decoder and code prefetch queue are completely full. Therefore pipelining is maintained for long bursts of bus cycles, if the bus is available (i.e., HOLD inactive) and $\overline{NA}$ is sampled active in each of the bus cycles.

INTERRUPT ACKNOWLEDGE (INTA) CYCLES

In repsonse to an interrupt request on the INTR input when interrupts are enabled, the 80376 performs two interrupt acknowledge cycles. These bus cycles are similar to read cycles in that bus definition signals define the type of bus activity taking place, and each cycle continues until acknowledged by $\overline{READY}$ sampled active.

The state of A_2 distinguishes the first and second interrupt acknowledge cycles. The byte address driven during the first interrupt acknowledge cycle is 4 (A_{23}–A_3, A_1, $\overline{BLE}$ LOW, A_2 and $\overline{BHE}$ HIGH). The byte address driven during the second interrupt acknowledge cycle is 0 (A_{23}–A_1, $\overline{BLE}$ LOW and $\overline{BHE}$ HIGH).

The $\overline{LOCK}$ output is asserted from the beginning of the first interrupt acknowledge cycle until the end of the second interrupt acknowledge cycle. Four idle bus states, T_i, are inserted by the 80376 between the two interrupt acknowledge cycles for compatibility with the interrupt specification T_{RHRL} of the 8259A Interrupt Controller and the 82370 Integrated Peripheral.



Interrupt Vector (0–255) is read on D0–D7 at end of second Interrupt Acknowledge bus cycle.
Because each Interrupt Acknowledge bus cycle is followed by idle bus states, asserting $\overline{NA}$ has no practical effect. Choose the approach which is simplest for your system hardware design.

Figure 4.13. Interrupt Acknowledge Cycles

During both interrupt acknowledge cycles, D_{15}–D_0 float. No data is read at the end of the first interrupt acknowledge cycle. At the end of the second interrupt acknowledge cycle, the 80376 will read an external interrupt vector from D_7–D_0 of the data bus. The vector indicates the specific interrupt number (from 0–255) requiring service.

HALT INDICATION CYCLE

The 80376 execution unit halts as a result of executing a HLT instruction. Signaling its entrance into the halt state, a halt indication cycle is performed. The halt indication cycle is identified by the state of the bus definition signals and a byte address of 2. See the **Bus Cycle Definition Signals** section. The halt indication cycle must be acknowledged by $\overline{READY}$ asserted. A halted 80376 resumes execution when INTR (if interrupts are enabled), NMI or RESET is asserted.

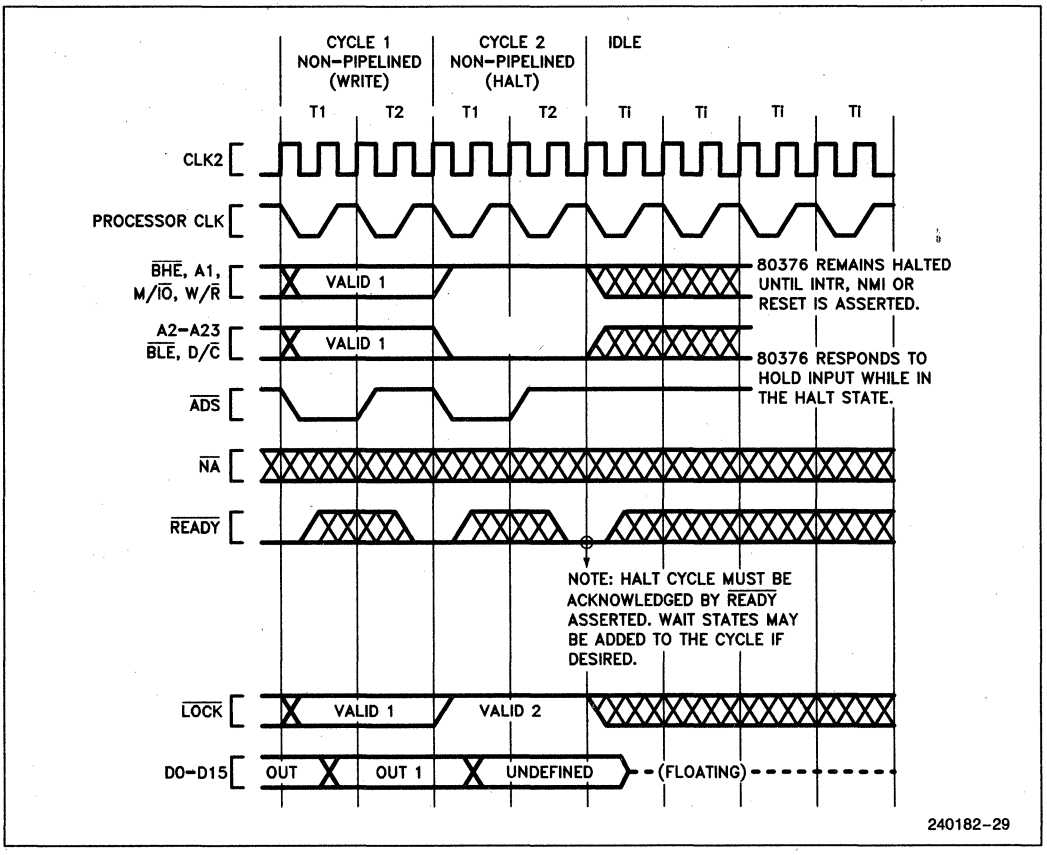


Figure 4.14. Example Halt Indication Cycle from Non-Pipelined Cycle

SHUTDOWN INDICATION CYCLE

The 80376 shuts down as a result of a protection fault while attempting to process a double fault. Signaling its entrance into the shutdown state, a shutdown indication cycle is performed. The shutdown indication cycle is identified by the state of the bus definition signals shown in **Bus Cycle Definition Signals** and a byte address of 0. The shutdown indication cycle must be acknowledged by $\overline{\text{READY}}$ asserted. A shutdown 80376 resumes execution when NMI or RESET is asserted.

ENTERING AND EXITING HOLD ACKNOWLEDGE

The bus hold acknowledge state, T_h, is entered in response to the HOLD input being asserted. In the bus hold acknowledge state, the 80376 floats all outputs or bidirectional signals, except for HLDA. HLDA is asserted as long as the 80376 remains in the bus hold acknowledge state. In the bus hold acknowledge state, all inputs except HOLD and RESET are ignored.

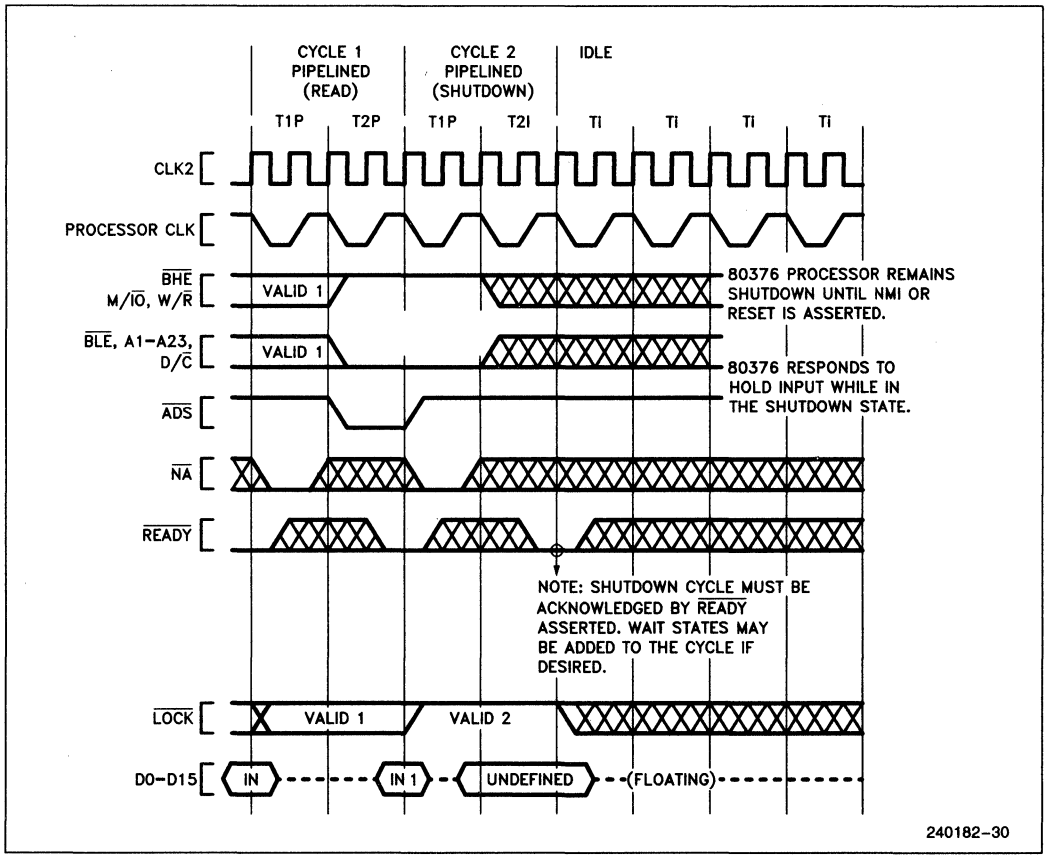


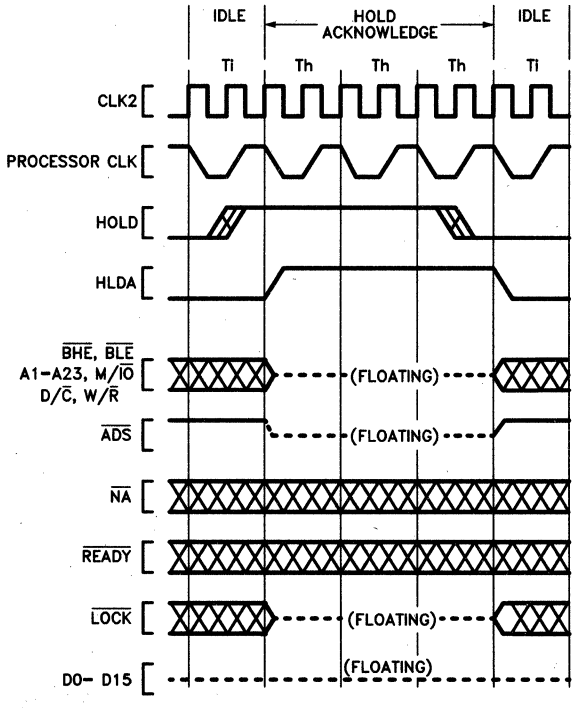
Figure 4.15. Example Shutdown Indication Cycle from Non-Pipelined Cycle

T_h may be entered from a bus idle state as in Figure 4.16 or after the acknowledgement of the current physical bus cycle if the LOCK signal is not asserted, as in Figures 4.17 and 4.18.

T_h is exited in response to the HOLD input being negated. The following state will be T_i as in Figure 4.16 if no bus request is pending. The following bus state will be T1 if a bus request is internally pending, as in Figures 4.17 and 4.18. T_h is exited in response to RESET being asserted.

If a rising edge occurs on the edge-triggered NMI input while in T_h, the event is remembered as a non-maskable interrupt 2 and is serviced when T_h is exited unless the 80376 is reset before T_h is exited.

26



NOTE:
For maximum design flexibility the 80376 has no internal pull-up resistors on its outputs. Your design may require an external pullup on $\overline{ADS}$ and other 80376 outputs to keep them negated during float periods.

Figure 4.16. Requesting Hold from Idle Bus

RESET DURING HOLD ACKNOWLEDGE

RESET being asserted takes priority over HOLD being asserted. If RESET is asserted while HOLD remains asserted, the 80376 drives its pins to defined states during reset, as in **Table 4.5, Pin State During Reset,** and performs internal reset activity as usual.

If HOLD remains asserted when RESET is inactive, the 80376 enters the hold acknowledge state before performing its first bus cycle, provided HOLD is still asserted when the 80376 processor would otherwise perform its first bus cycle. If HOLD remains asserted when RESET is inactive, the $\overline{BUSY}$ input is still sampled as usual to determine whether a self test is being requested.

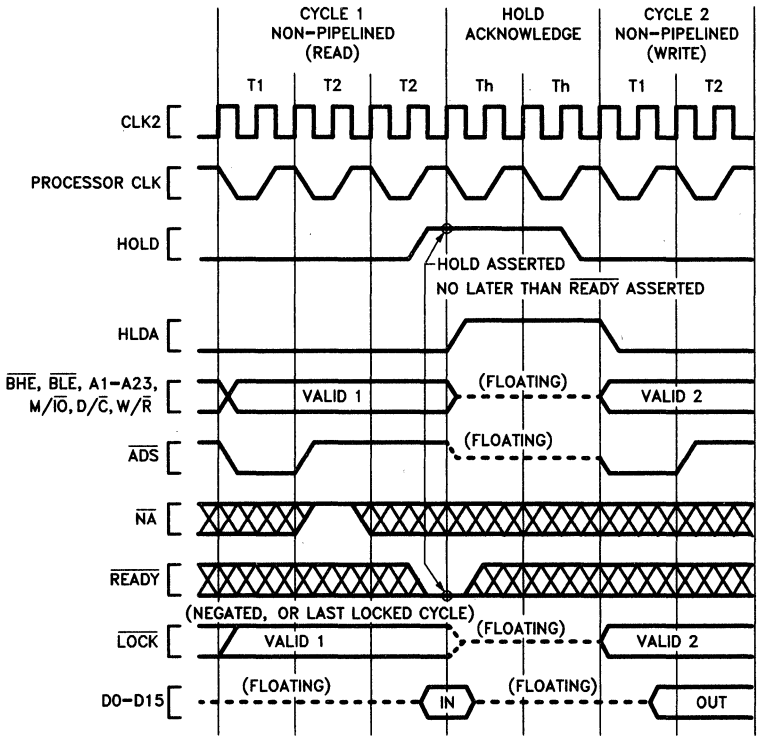
FLOAT

Activating the $\overline{FLT}$ input floats all 80376 bidirectional and output signals, including HLDA. Asserting $\overline{FLT}$ isolates the 80376 from the surrounding circuitry. When an 80376 in a PQFP surface-mount package is used without a socket, it cannot be removed from the printed circuit board. The $\overline{FLT}$ input allows the 80376 to be electrically isolated to allow testing of external circuitry. This technique is known as ONCE™ for "ON-Circuit Emulation".

ENTERING AND EXITING FLOAT

$\overline{FLT}$ is an asynchronous, active-low input. It is recognized on the rising edge of CLK2. When recognized, it aborts the current bus cycle and floats the outputs of the 80376 (Figure 4.20). $\overline{FLT}$ must be held low for a minimum of 16 CLK2 cycles. Reset should be asserted and held asserted until after $\overline{FLT}$ is deasserted. This will ensure that the 80376 will exit float in a valid state.

Asserting the $\overline{FLT}$ input unconditionally aborts the current bus cycle and forces the 80376 into the FLOAT mode. Since activating $\overline{FLT}$ unconditionally forces the 80376 into FLOAT mode, the 80376 is not



NOTE:
HOLD is a synchronous input and can be asserted at any CLK2 edge, provided setup and hold (t_{23} and t_{24}) requirements are met. This waveform is useful for determining Hold Acknowledge latency.

Figure 4.17. Requesting Hold from Active Bus ($\overline{NA}$ Inactive)

guaranteed to enter FLOAT in a valid state. After deactivating $\overline{FLT}$, the 80376 is not guaranteed to exit FLOAT mode in a valid state. This is not a problem as the $\overline{FLT}$ pin is meant to be used only during ONCE. After exiting FLOAT, the 80376 must be reset to return it to a valid state. Reset should be asserted before $\overline{FLT}$ is deasserted. This will ensure that the 80376 will exit float in a valid state.

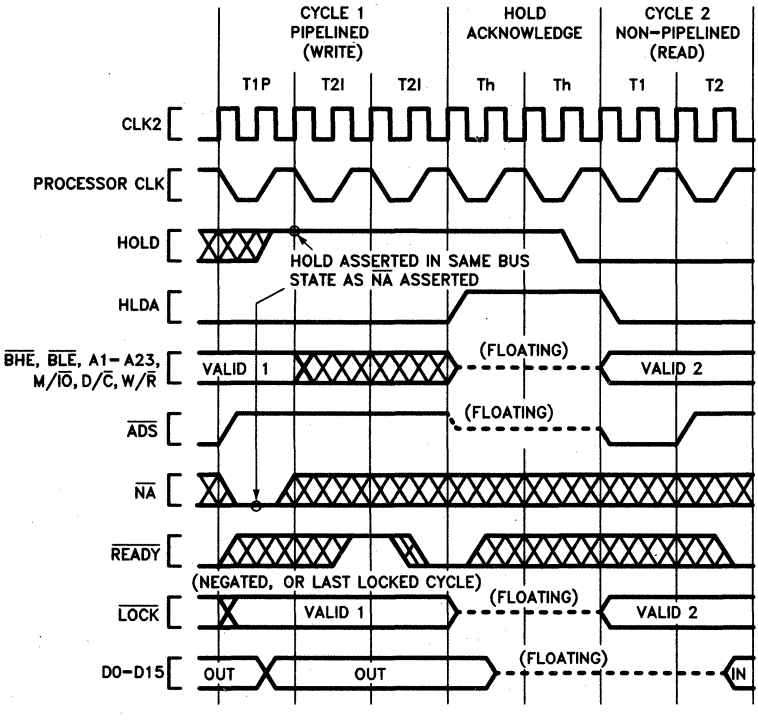
$\overline{FLT}$ has an internal pull-up resistor, and if it is not used it should be unconnected.

BUS ACTIVITY DURING AND FOLLOWING RESET

RESET is the highest priority input signal, capable of interrupting any processor activity when it is asserted. A bus cycle in progress can be aborted at any stage, or idle states or bus hold acknowledge states discontinued so that the reset state is established.

RESET should remain asserted for at least 15 CLK2 periods to ensure it is recognized throughout the 80376, and at least 80 CLK2 periods if a 80376 self-test is going to be requested at the falling edge. RESET asserted pulses less than 15 CLK2 periods may not be recognized. RESET pulses less than 80 CLK2 periods followed by a self-test may cause the self-test to report a failure when no true failure exists.

Provided the RESET falling edge meets setup and hold times t_{25} and t_{26}, the internal processor clock phase is defined at that time as illustrated by Figure 4.19 and Figure 6.7.

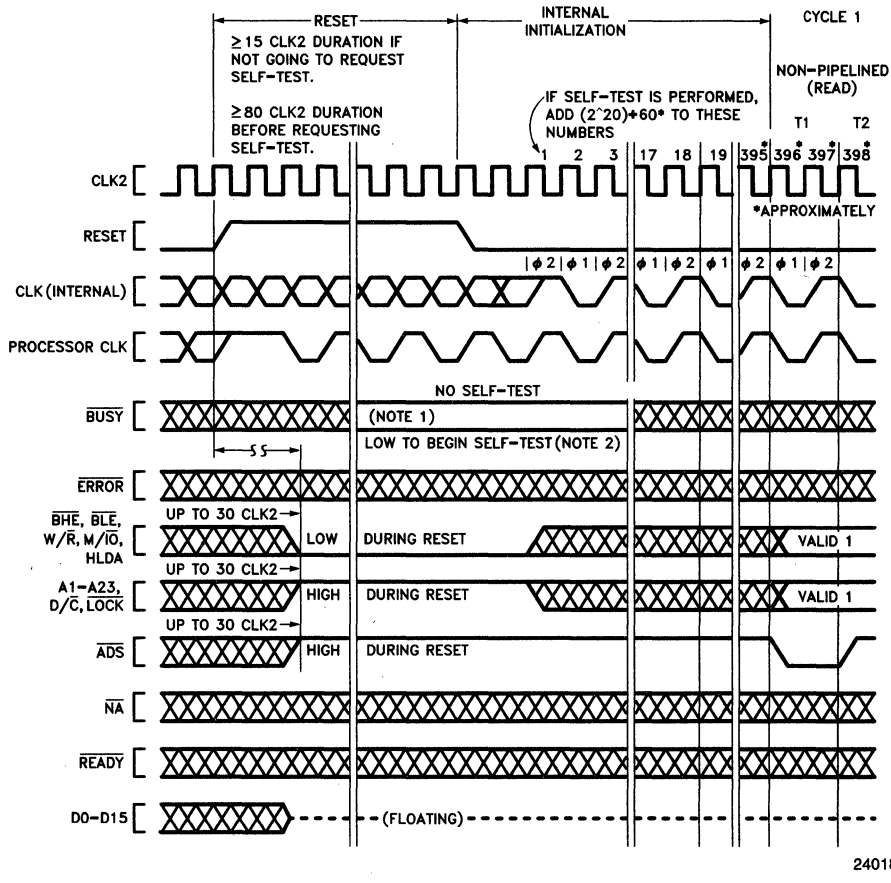


NOTE:
HOLD is a synchronous input and can be asserted at any CLK2 edge, provided setup and hold (t_{23} and t_{24}) requirements are met. This waveform is useful for determining Hold Acknowledge latency.

Figure 4.18. Requesting Hold from Idle Bus ($\overline{NA}$ Active)

An 80376 self-test may be requested at the time RESET goes inactive by having the $\overline{BUSY}$ input at a LOW level as shown in Figure 4.19. The self-test requires (2^{20} + approximately 60) CLK2 periods to complete. The self-test duration is not affected by the test results. Even if the self-test indicates a problem, the 80376 attempts to proceed with the reset sequence afterwards.

After the RESET falling edge (and after the self-test if it was requested) the 80376 performs an internal initialization sequence for approximately 350 to 450 CLK2 periods.



NOTES:
1. BUSY should be held stable for 8 CLK2 periods before and after the CLK2 period in which RESET falling edge occurs.
2. If self-test is requested, the 80376 outputs remain in their reset state as shown here.

Figure 4.19. Bus Activity from Reset until First Code Fetch

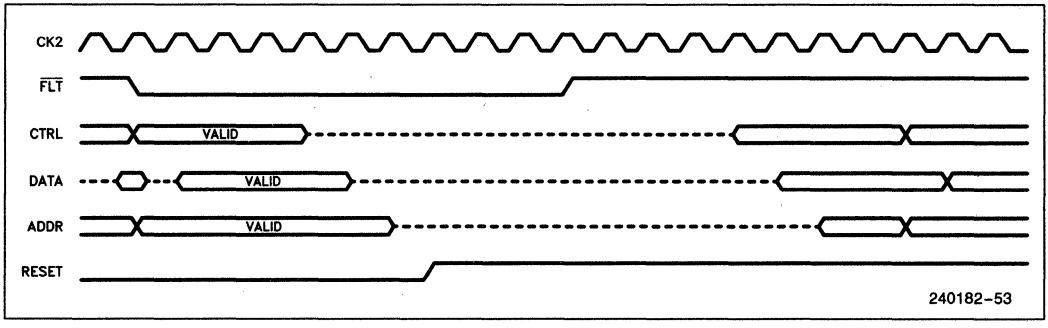


Figure 4.20. Entering and Exiting FLOAT

4.5 Self-Test Signature

Upon completion of self-test (if self-test was requested by driving $\overline{BUSY}$ LOW at the falling edge of RESET) the EAX register will contain a signature of 00000000H indicating the 80376 passed its self-test of microcode and major PLA contents with no problems detected. The passing signature in EAX, 00000000H, applies to all 80376 revision levels. Any non-zero signature indicates the 80376 unit is faulty.

4.6 Component and Revision Identifiers

To assist 80376 users, the 80376 after reset holds a component identifier and revision identifier in its DX register. The upper 8 bits of DX hold 33H as identification of the 80376 component. (The lower nibble, 03H, refers to the Intel386™ architecture. The upper nibble, 30H, refers to the third member of the Intel386 family). The lower 8 bits of DX hold an 8-bit unsigned binary number related to the component revision level. The revision identifier will, in general, chronologically track those component steppings which are intended to have certain improvements or distinction from previous steppings. The 80376 revision identifier will track that of the 80386 where possible.

The revision identifier is intended to assist 80376 users to a practical extent. However, the revision identifier value is not guaranteed to change with every stepping revision, or to follow a completely uniform numerical sequence, depending on the type or intention of revision, or manufacturing materials required to be changed. Intel has sole discretion over these characteristics of the component.

Table 4.7. Component and Revision Identifier History

80376 Stepping Name	Revision Identifier
A0	05H
B	08H

4.7 Coprocessor Interfacing

The 80376 provides an automatic interface for the Intel 80387SX numeric floating-point coprocessor. The 80387SX coprocessor uses an I/O mapped interface driven automatically by the 80376 and assisted by three dedicated signals: $\overline{BUSY}$, $\overline{ERROR}$ and PEREQ.

As the 80376 begins supporting a coprocessor instruction, it tests the $\overline{BUSY}$ and $\overline{ERROR}$ signals to determine if the coprocessor can accept its next instruction. Thus, the $\overline{BUSY}$ and $\overline{ERROR}$ inputs eliminate the need for any "preamble" bus cycles for communication between processor and coprocessor. The 80387SX can be given its command opcode immediately. The dedicated signals provide instruction synchronization, and eliminate the need of using the 80376 WAIT opcode (9BH) for 80387SX instruction synchronization (the WAIT opcode was required when the 8086 or 8088 was used with the 8087 coprocessor).

Custom coprocessors can be included in 80376 based systems by memory-mapped or I/O-mapped interfaces. Such coprocessor interfaces allow a completely custom protocol, and are not limited to a set of coprocessor protocol "primitives". Instead, memory-mapped or I/O-mapped interfaces may use all applicable 80376 instructions for high-speed coprocessor communication. The $\overline{BUSY}$ and $\overline{ERROR}$ inputs of the 80376 may also be used for the custom coprocessor interface, if such hardware assist is desired. These signals can be tested by the 80376 WAIT opcode (9BH). The WAIT instruction will wait until the $\overline{BUSY}$ input is inactive (interruptable by an NMI or enabled INTR input), but generates an exception 16 fault if the $\overline{ERROR}$ pin is active when the $\overline{BUSY}$ goes (or is) inactive. If the custom coprocessor interface is memory-mapped, protection of the addresses used for the interface can be provided with the segmentation mechanism of the 80376. If the custom interface is I/O-mapped, protection of the interface can be provided with the 80376 IOPL (I/O Privilege Level) mechanism.

The 80387SX numeric coprocessor interface is I/O mapped as shown in Table 4.8. Note that the 80387SX coprocessor interface addresses are beyond the 0H-0FFFFH range for programmed I/O. When the 80376 supports the 80387SX coprocessor, the 80376 automatically generates bus cycles to the coprocessor interface addresses.

Table 4.8 Numeric Coprocessor Port Addresses

Address in 80376 I/O Space	80387SX Coprocessor Register
8000F8H	Opcode Register
8000FCH	Operand Register
8000FEH	Operand Register

SOFTWARE TESTING FOR COPROCESSOR PRESENCE

When software is used to test coprocessor (80387SX) presence, it should use only the following coprocessor opcodes: FNINIT, FNSTCW and FNSTSW. To use other coprocessor opcodes when a coprocessor is known to be not present, first set EM = 1 in the 80376 CR0 register.

5.0 PACKAGE THERMAL SPECIFICATIONS

The Intel 80376 embedded processor is specified for operation when case temperature is within the range of 0°C–115°C for both the ceramic 88-pin PGA package and the plastic 100-pin PQFP package. The case temperature may be measured in any environment, to determine whether the 80376 is within specified operating range. The case temperature should be measured at the center of the top surface.

The ambient temperature is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from the θ_{jc} and θ_{ja} from the following equations:

$$T_J = T_C + P^*\theta_{jc}$$

$$T_A = T_j - P^*\theta_{ja}$$

$$T_C = T_a + P^*[\theta_{ja} - \theta_{jc}]$$

Values for θ_{ja} and θ_{jc} are given in Table 5.1 for the 100-lead fine pitch. θ_{ja} is given at various airflows. Table 5.2 shows the maximum T_a allowable (without exceeding T_c) at various airflows. Note that T_a can be improved further by attaching "fins" or a "heat sink" to the package. P is calculated using the maximum ***cold*** I_{cc} of 305 mA and the maximum V_{CC} of 5.5V for both packages.

Table 5.1. 80376 Package Thermal Characteristics Thermal Resistances (°C/Watt) θ_{jc} and θ_{ja}

Package	θ_{jc}	θ_{ja} Versus Airflow-ft/min (m/sec)					
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
100-Lead Fine Pitch	7.5	34.5	29.5	25.5	22.5	21.5	21.0
88-Pin PGA	2.5	29.0	22.5	17.0	14.5	12.5	12.0

Table 5.2. 80376 Maximum Allowable Ambient Temperature at Various Airflows

Package	θ_{jc}	T_A(°C) vs Airflow-ft/min (m/sec)					
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
100-Lead Fine Pitch	7.5	70	78	85	90	92	93
88-Pin PGA	2.5	70	81	90	95	98	99

6.0 ELECTRICAL SPECIFICATIONS

The following sections describe recommended electrical connections for the 80376, and its electrical specifications.

6.1 Power and Grounding

The 80376 is implemented in CHMOS IV technology and has modest power requirements. However, its high clock frequency and 47 output buffers (address, data, control, and HLDA) can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean on-chip power distribution at high frequency, 14 V_{CC} and 18 V_{SS} pins separately feed functional units of the 80376.

Power and ground connections must be made to all external V_{CC} and GND pins of the 80376. On the circuit board, all V_{CC} pins should be connected on a V_{CC} plane and all V_{SS} pins should be connected on a GND plane.

POWER DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitors should be placed near the 80376. The 80376 driving its 24-bit address bus and 16-bit data bus at high frequencies can cause transient power surges, particularly when driving large capacitive loads. Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the 80376 and decoupling capacitors as much as possible.

RESISTOR RECOMMENDATIONS

The $\overline{\text{ERROR}}$, $\overline{\text{FLT}}$ and $\overline{\text{BUSY}}$ inputs have internal pull-up resistors of approximately 20 KΩ and the PEREQ input has an internal pull-down resistor of approximately 20 KΩ built into the 80376 to keep these signals inactive when the 80387SX is not present in the system (or temporarily removed from its socket).

In typical designs, the external pull-up resistors shown in Table 6.1 are recommended. However, a particular design may have reason to adjust the resistor values recommended here, or alter the use of pull-up resistors in other ways.

Table 6.1. Recommended Resistor Pull-Ups to V_{CC}

Pin	Signal	Pull-Up Value	Purpose
16	$\overline{ADS}$	20 KΩ ± 10%	Lightly Pull $\overline{ADS}$ Inactive during 80376 Hold Acknowledge States
26	$\overline{LOCK}$	20 KΩ ± 10%	Lightly Pull $\overline{LOCK}$ Inactive during 80376 Hold Acknowledge States

OTHER CONNECTION RECOMMENDATIONS

For reliable operation, always connect unused inputs to an appropriate signal level. N/C pins should always remain **unconnected. Connection of N/C pins to V_{CC} or V_{SS} will result in incompatibility with future steppings of the 80376.**

Particularly when not using interrupts or bus hold (as when first prototyping), prevent any chance of spurious activity by connecting these associated inputs to GND:

—INTR
—NMI
—HOLD

If not using address pipelining connect the $\overline{NA}$ pin to a pull-up resistor in the range of 20 KΩ to V_{CC}.

6.2 Absolute Maximum Ratings

Table 6.2. Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	−65°C to +150°C
Case Temperature under Bias	−65°C to +120°C
Supply Voltage with Respect to V_{SS}	−0.5V to +6.5V
Voltage on Other Pins	−0.5V to (V_{CC} + 0.5)V

Table 6.2 gives a stress ratings only, and functional operation at the maximums is not guaranteed. Functional operating conditions are given in **Section 6.3, D.C. Specifications,** and **Section 6.4, A.C. Specifications.**

Extended exposure to the Maximum Ratings may affect device reliability. Furthermore, although the 80376 contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

6.3 D.C. Specifications

ADVANCE INFORMATION SUBJECT TO CHANGE

Table 6.3: 80376 D.C. Characteristics

Functional Operating Range: V_{CC} = 5V ±10%; T_{CASE} = 0°C to 115°C for 88-pin PGA or 100-pin PQFP

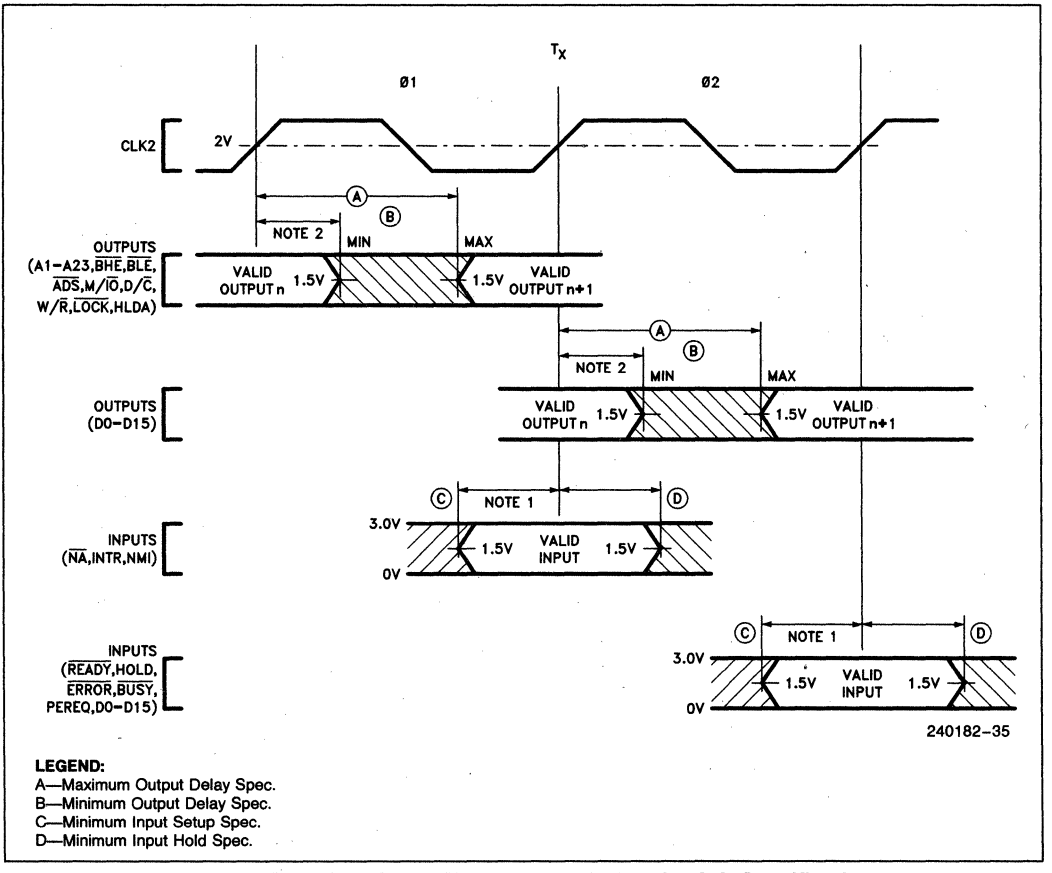
Symbol	Parameter	Min	Max	Unit
V_{IL}	Input LOW Voltage	−0.3	+0.8	V(1)
V_{IH}	Input HIGH Voltage	2.0	V_{CC} +0.3	V(1)
V_{ILC}	CLK2 Input LOW Voltage	−0.3	+0.8	V(1)
V_{IHC}	CLK2 Input HIGH Voltage	V_{CC} − 0.8	V_{CC} + 0.3	V(1)
V_{OL}	Output LOW Voltage			
I_{OL} = 4 mA:	A_{23}–A_1, D_{15}–D_0		0.45	V(1)
I_{OL} = 5 mA:	$\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA		0.45	V(1)
V_{OH}	Output High Voltage			
I_{OH} = −1 mA:	A_{23}–A_1, D_{15}–D_0	2.4		V(1)
I_{OH} = −0.2 mA:	A_{23}–A_1, D_{15}–D_0	V_{CC} − 0.5		V(1)
I_{OH} = −0.9 mA:	$\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA	2.4		V(1)
I_{OH} = −0.18 mA:	$\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$ $\overline{ADS}$, HLDA	V_{CC} − 0.5		V(1)
I_{LI}	Input Leakage Current (For All Pins except PEREQ, $\overline{BUSY}$, $\overline{FLT}$ and $\overline{ERROR}$)		±15	μA, 0V ≤ V_{IN} ≤ V_{CC}(1)
I_{IH}	Input Leakage Current (PEREQ Pin)		200	μA, V_{IH} = 2.4V(1, 2)
I_{IL}	Input Leakage Current ($\overline{BUSY}$ and $\overline{ERROR}$ Pins)		−400	μA, V_{IL} = 0.45V(3)
I_{LO}	Output Leakage Current		±15	μA, 0.45V ≤ V_{OUT} ≤ V_{CC}(1)
I_{CC}	Supply Current CLK2 = 32 MHz CLK2 = 40 MHz		 275 305	 mA, I_{CC} typ = 175 mA(4) mA, I_{CC} typ = 200 mA(4)
C_{IN}	Input Capacitance		10	pF, F_C = 1 MHz(5)
C_{OUT}	Output or I/O Capacitance		12	pF, F_C = 1 MHz(5)
C_{CLK}	CLK2 Capacitance		20	pF, F_C = 1 MHz(5)

NOTES:
1. Tested at the minimum operating frequency of the device.
2. PEREQ input has an internal pull-down resistor.
3. $\overline{BUSY}$, $\overline{FLT}$ and $\overline{ERROR}$ inputs each have an internal pull-up resistor.
4. I_{CC} max measurement at worse case load, V_{CC} and temperature (0°C).
5. Not 100% tested.

The A.C. specifications given in Table 6.4 consist of output delays, input setup requirements and input hold requirements. All A.C. specifications are relative to the CLK2 rising edge crossing the 2.0V level.

A.C. specification measurement is defined by Figure 6.1. Inputs must be driven to the voltage levels indicated by Figure 6.1 when A.C. specifications are measured. 80376 output delays are specified with minimum and maximum limits measured as shown. The minimum 80376 delay times are hold times provided to external circuitry. 80376 input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct 80376 processor operation.

Outputs $\overline{NA}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{BHE}$, $\overline{BLE}$, A_{23}–A_1 and HLDA only change at the beginning of phase one. D_{15}–D_0 (write cycles) only change at the beginning of phase two. The $\overline{READY}$, HOLD, $\overline{BUSY}$, $\overline{ERROR}$, PEREQ and D_{15}–D_0 (read cycles) inputs are sampled at the beginning of phase one. The $\overline{NA}$, INTR and NMI inputs are sampled at the beginning of phase two.



LEGEND:
A—Maximum Output Delay Spec.
B—Minimum Output Delay Spec.
C—Minimum Input Setup Spec.
D—Minimum Input Hold Spec.

Figure 6.1. Drive Levels and Measurement Points for A.C. Specifications

6.4 A.C. Specifications

Table 6.4. 80376 A.C. Characteristics at 16 MHz

Functional Operating Range: V_{CC} = 5V ±10%; T_{CASE} = 0°C to 115°C for 88-pin PGA or 100-pin PQFP

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Operating Frequency	4	16	MHz		Half CLK2 Freq
t_1	CLK2 Period	31	125	ns	6.3	
t_{2a}	CLK2 HIGH Time	9		ns	6.3	At 2(3)
t_{2b}	CLK2 HIGH Time	5		ns	6.3	At (V_{CC} − 0.8)V(3)
t_{3a}	CLK2 LOW Time	9		ns	6.3	At 2V(3)
t_{3b}	CLK2 LOW Time	7		ns	6.3	At 0.8V(3)
t_4	CLK2 Fall Time		8	ns	6.3	(V_{CC}−0.8)V to 0.8V(3)
t_5	CLK2 Rise Time		8	ns	6.3	0.8V to (V_{CC}−0.8)(3)
t_6	A_{23}–A_1 Valid Delay	4	36	ns	6.5	C_L = 120 pF(4)
t_7	A_{23}–A_1 Float Delay	4	40	ns	6.6	(1)
t_8	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Valid Delay	4	36	ns	6.5	C_L = 75 pF(4)
t_9	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Float Delay	4	40	ns	6.6	(1)
t_{10}	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Valid Delay	6	33	ns	6.5	C_L = 75 pF(4)
t_{11}	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	6	35	ns	6.6	(1)
t_{12}	D_{15}–D_0 Write Data Valid Delay	4	40	ns	6.5	C_L = 120 pF(4)
t_{13}	D_{15}–D_0 Write Data Float Delay	4	35	ns	6.6	(1)
t_{14}	HLDA Valid Delay	4	33	ns	6.6	C_L = 75 pF(4)
t_{15}	$\overline{NA}$ Setup Time	5		ns	6.4	
t_{16}	$\overline{NA}$ Hold Time	21		ns	6.6	
t_{19}	$\overline{READY}$ Setup Time	19		ns	6.4	
t_{20}	$\overline{READY}$ Hold Time	4		ns	6.4	
t_{21}	Setup Time D_{15}–D_0 Read Data	9		ns	6.4	
t_{22}	Hold Time D_{15}–D_0 Read Data	6		ns	6.4	
t_{23}	HOLD Setup Time	26		ns	6.4	
t_{24}	HOLD Hold Time	5		ns	6.4	
t_{25}	RESET Setup Time	13		ns	6.7	
t_{26}	RESET Hold Time	4		ns	6.7	

Table 6.4. 80376 A.C. Characteristics at 16 MHz (Continued)
Functional Operating Range: V_{CC} = 5V ±10%; T_{CASE} = 0°C to 115°C for 88-pin PGA or 100-pin PQFP

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{27}	NMI, INTR Setup Time	16		ns	6.4	(2)
t_{28}	NMI, INTR Hold Time	16		ns	6.4	(2)
t_{29}	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Setup Time	16		ns	6.4	(2)
t_{30}	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Hold Time	5		ns	6.4	(2)

NOTES:
1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, tc assure recognition within a specific CLK2 period.
3. These are not tested. They are guaranteed by design characterization.
4. Tested with C_L set to 50 pF and derated to support the indicated distributed capacitive load. See Figures 6.8 through 6.10 for capacitive derating curves.
5. The 80376 does not have t_{17} or t_{18} timing specifications.

Table 6.5. 80376 A.C. Characteristics at 20 MHz
Functional Operating Range: V_{CC} = 5V ±10%; T_{CASE} = 0°C to 115°C for 88-pin PGA or 100-pin PQFP

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Operating Frequency	4	20	MHz		Half CLK2 Frequency
t_1	CLK2 Period	25	125	ns	6.3	
t_{2a}	CLK2 HIGH Time	8		ns	6.3	At 2V(3)
t_{2b}	CLK2 HIGH Time	5		ns	6.3	At (V_{CC} − 0.8)V(3)
t_{3a}	CLK2 LOW Time	8		ns	6.3	At 2V(3)
t_{3b}	CLK2 LOW Time	6		ns	6.3	At 0.8V(3)
t_4	CLK2 Fall Time		8	ns	6.3	(V_{CC}−0.8V) to 0.8V(3)
t_5	CLK2 Rise Time		8	ns	6.3	0.8V to (V_{CC}−0.8)(3)
t_6	A_{23}–A_1 Valid Delay	4	30	ns	6.5	C_L = 120 pF(4)
t_7	A_{23}–A_1 Float Delay	4		ns	6.6	(1)
t_8	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Valid Delay	4	30	ns	6.5	C_L = 75 pF(4)
t_9	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Float Delay	4	32	ns	6.6	(1)
t_{10a}	M/$\overline{IO}$, D/$\overline{C}$ Valid Delay	6	28	ns	6.5	C_L = 75 pF(4)
t_{10b}	W/$\overline{R}$, $\overline{ADS}$ Valid Delay	6	26	ns	6.5	C_L = 75 pF(4)
t_{11}	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	6	30	ns	6.6	(1)
t_{12}	D_{15}–D_0 Write Data Valid Delay	4	38	ns	6.5	C_L = 120 pF
t_{13}	D_{15}–D_0 Write Data Float Delay	4	27	ns	6.6	(1)

Table 6.5. 80376 A.C. Characteristics at 20 MHz (Continued)
Functional Operating Range: V_{CC} = 5V ±10%; T_{CASE} = 0°C to 115°C for 88-pin PGA or 100-pin PQFP

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{14}	HLDA Valid Delay	4	28	ns	6.5	C_L = 75 pF(4)
t_{15}	$\overline{NA}$ Setup Time	5		ns	6.4	
t_{16}	$\overline{NA}$ Hold Time	12		ns	6.4	
t_{19}	$\overline{READY}$ Setup Time	12		ns	6.4	
t_{20}	$\overline{READY}$ Hold Time	4		ns	6.4	
t_{21}	D_{15}–D_0 Read Data Setup Time	9		ns	6.4	
t_{22}	D_{15}–D_0 Read Data Hold Time	6		ns	6.4	
t_{23}	HOLD Setup Time	17		ns	6.4	
t_{24}	HOLD Hold Time	5		ns	6.4	
t_{25}	RESET Setup Time	12		ns	6.7	
t_{26}	RESET Hold Time	4		ns	6.7	
t_{27}	NMI, INTR Setup Time	16		ns	6.4	(2)
t_{28}	NMI, INTR Hold Time	16		ns	6.4	(2)
t_{29}	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Setup Time	14		ns	6.4	(2)
t_{30}	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Hold Time	5		ns	6.4	(2)

NOTES:
1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. These are not tested. They are guaranteed by design characterization.
4. Tested with C_L set to 50 pF and derated to support the indicated distributed capacitive load. See Figures 6.8 through 6.10 for capacitive derating curves.
5. The 80376 does not have t_{17} or t_{18} timing specifications.

A.C. TEST LOADS

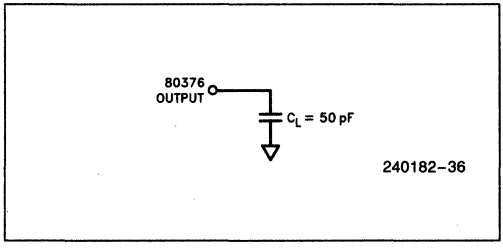


Figure 6.2. A.C. Test Loads

A.C. TIMING WAVEFORMS

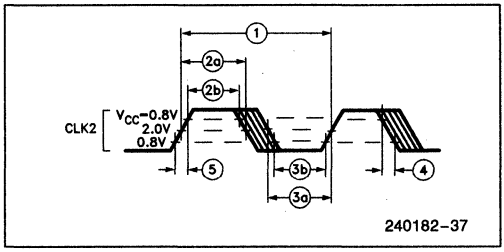


Figure 6.3. CLK2 Waveform

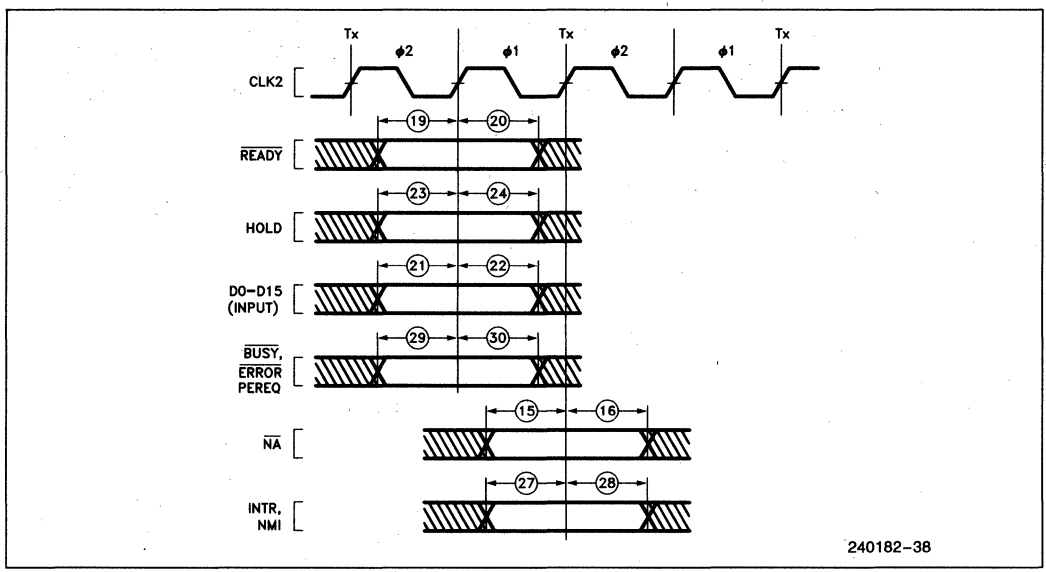


Figure 6.4. A.C. Timing Waveforms—Input Setup and Hold Timing

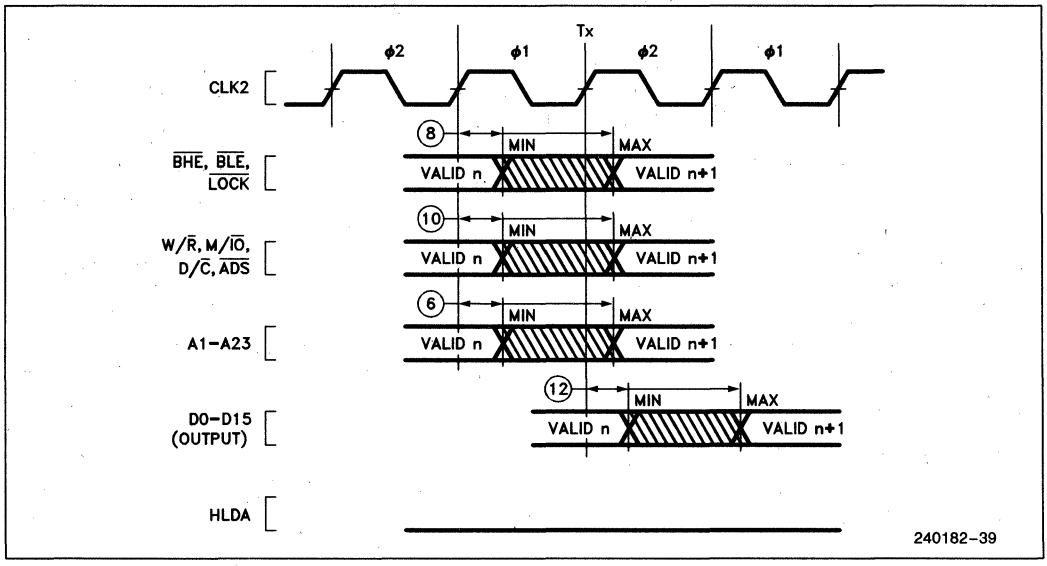


Figure 6.5. A.C. Timing Waveforms—Output Valid Delay Timing

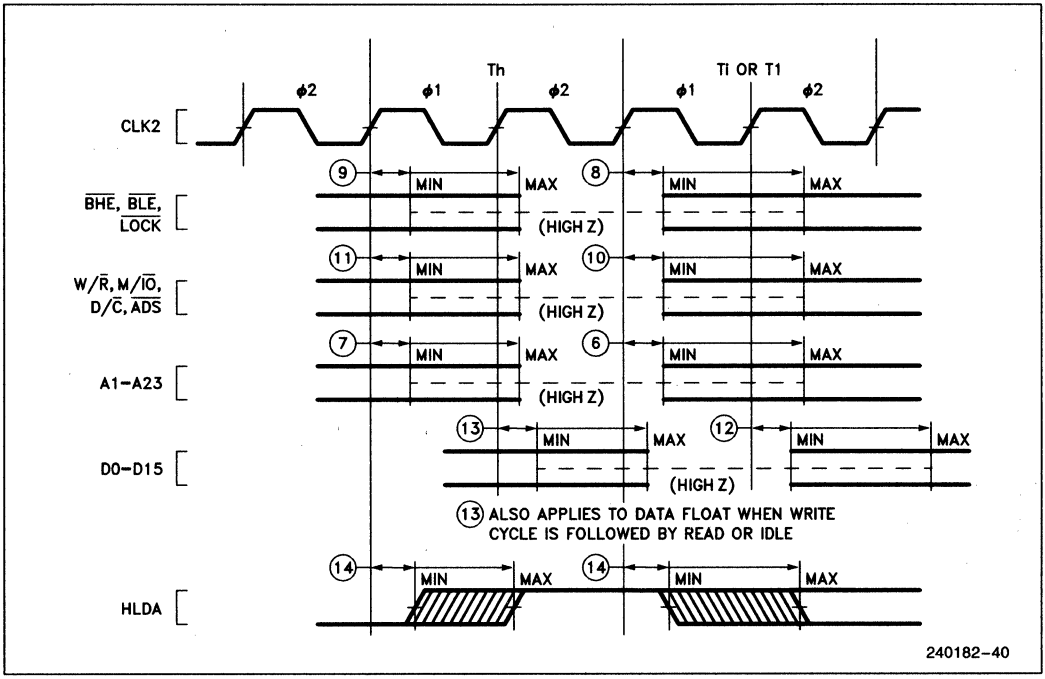
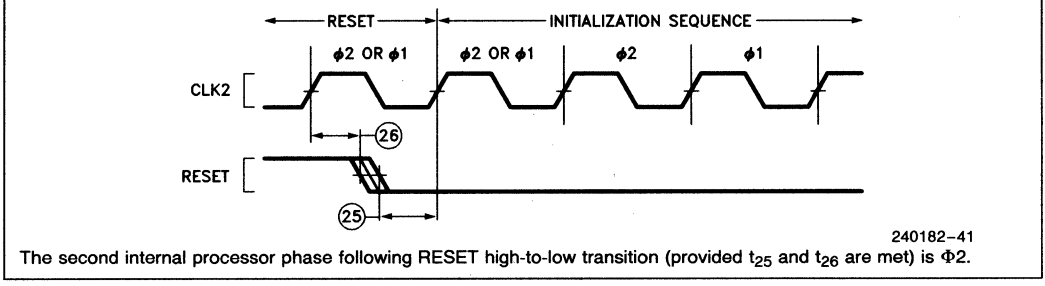


Figure 6.6. A.C. Timing Waveforms—Output Float Delay and HLDA Valid Delay Timing



The second internal processor phase following RESET high-to-low transition (provided t_{25} and t_{26} are met) is Φ2.

Figure 6.7. A.C. Timing Waveforms—RESET Setup and Hold Timing, and Internal Phase

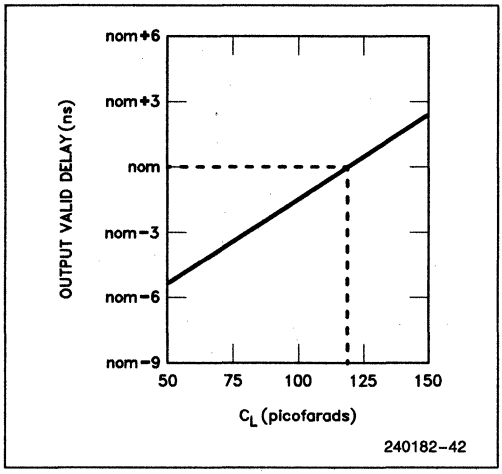


Figure 6.8. Typical Output Valid Delay versus Load Capacitance at Maximum Operating Temperature (C_L = 120 pF)

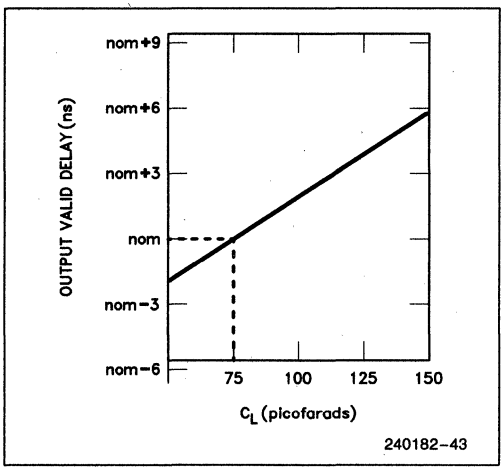


Figure 6.9. Typical Output Valid Delay versus Load Capacitance at Maximum Operating Temperature (C_L = 75 pF)

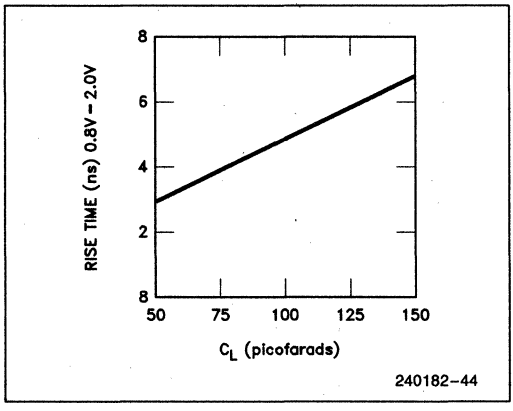


Figure 6.10. Typical Output Rise Time versus Load Capacitance at Maximum Operating Temperature

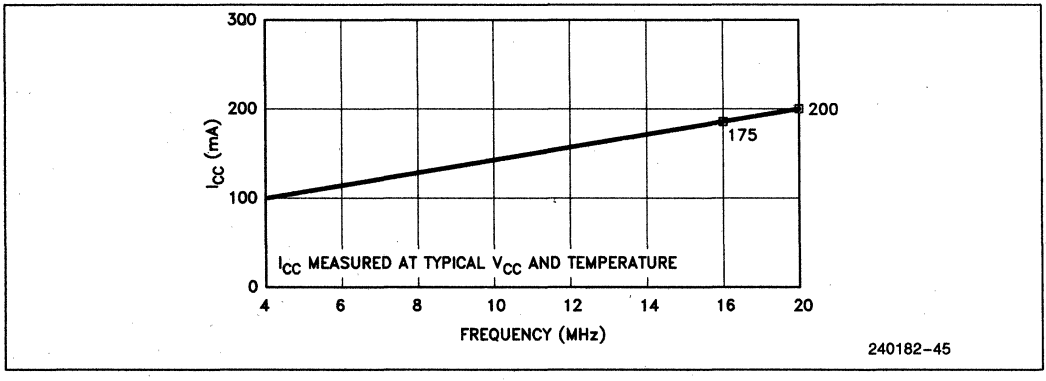


Figure 6.11. Typical I_{CC} vs Frequency

6.5 Designing for the ICE™-376 Emulator

The 376 embedded processor in-circuit emulator product is the ICE-376 emulator. Use of the emulator requires the target system to provide a socket that is compatible with the ICE-376 emulator. The 80376 offers two different probes for emulating user systems: an 88-pin PGA probe and a 100-pin fine pitch flat-pack probe. The 100-pin fine pitch flat-pack probe requires a socket, called the 100-pin PQFP, which is available from 3-M Textool (part number 2-0100-07243-000). The ICE-376 emulator probe attaches to the target system via an adapter which replaces the 80376 component in the target system. Because of the high operating frequency of 80376 systems and of the ICE-376 emulator, there is no buffering between the 80376 emulation processor in the ICE-376 emulator probe and the target system. A direct result of the non-buffered interconnect is that the ICE-376 emulator shares the address and data bus with the user's system, and the RESET signal is intercepted by the ICE emulator hardware. In order for the ICE-376 emulator to be functional in the user's system without the Optional Isolation Board (OIB) the designer must be aware of the following conditions:

1. The bus controller must only enable data transceivers onto the data bus during valid read cycles of the 80376, other local devices or other bus masters.
2. Before another bus master drives the local processor address bus, the other master must gain control of the address bus by asserting HOLD and receiving the HLDA response.
3. The emulation processor receives the RESET signal 2 or 4 CLK2 cycles later than an 80376 would, and responds to RESET later. Correct phase of the response is guaranteed.

In addition to the above considerations, the ICE-376 emulator processor module has several electrical and mechanical characteristics that should be taken into consideration when designing the 80376 system.

Capacitive Loading: ICE-376 adds up to 27 pF to each 80376 signal.

Drive Requirements: ICE-376 adds one FAST TTL load on the CLK2, control, address, and data lines. These loads are within the processor module and are driven by the 80376 emulation processor, which has standard drive and loading capability listed in Tables 6.3 and 6.4.

Power Requirements: For noise immunity and CMOS latch-up protection the ICE-376 emulator processor module is powered by the user system. The circuitry on the processor module draws up to 1.4A including the maximum 80376 I_{CC} from the user 80376 socket.

80376 Location and Orientation: The ICE-376 emulator processor module may require lateral clearance. Figure 6.12 shows the clearance requirements of the iMP adapter and Figure 6.13 shows the clearance requirements of the 88-pin PGA adapter. The

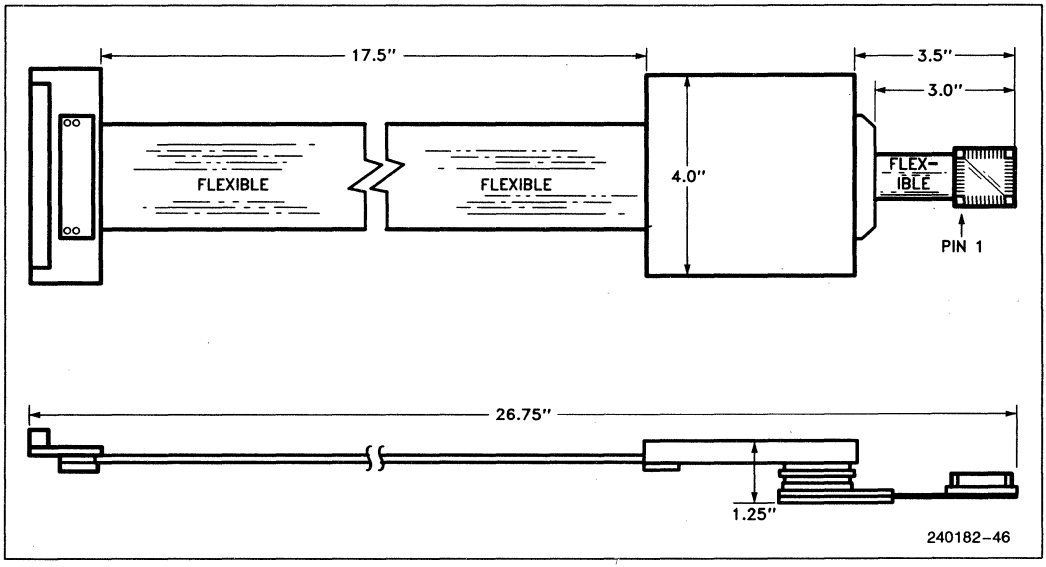


Figure 6.12. Preliminary ICE™-376 Emulator User Cable with PQFP Adapter

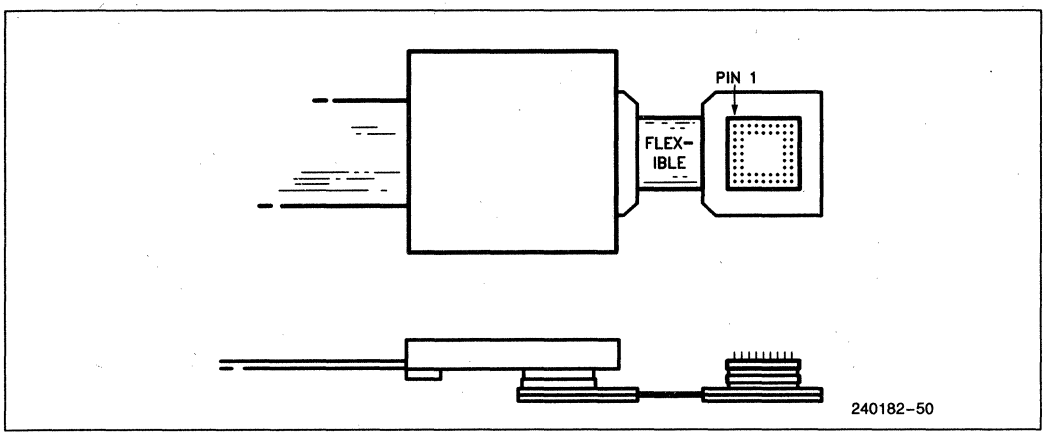


Figure 6.13. ICE™-376 Emulator User Cable with 88-Pin PGA Adapter

optional isolation board (OIB), which provides extra electrical buffering and has the same lateral clearance requirements as Figures 6.12 and 6.13, adds an additional 0.5 inches to the vertical clearance requirement. This is illustrated in Figure 6.14.

Optional Isolation Board (OIB) and the CLK2 speed reduction: Due to the unbuffered probe design, the ICE-376 emulator is susceptible to errors on the user's bus. The OIB allows the ICE-376 emulator to function in user systems with faults (shorted signals, etc.). After electrical verification the OIB may be removed. When the OIB is installed, the user system must have a maximum CLK2 frequency of 20 MHz.

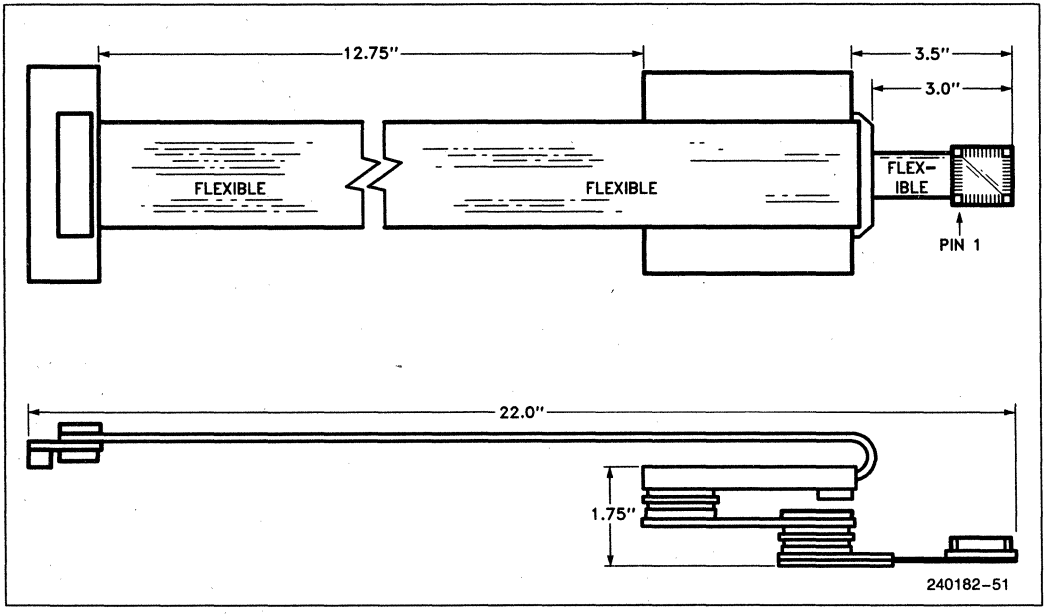


Figure 6.14. ICE™-376 Emulator User Cable with OIB and PQFP Adapter

7.0 DIFFERENCES BETWEEN THE 80376 AND THE 80386

The following are the major differences between the 80376 and the 80386.

1. The 80376 generates byte selects on $\overline{BHE}$ and $\overline{BLE}$ (like the 8086 and 80286 microprocessors) to distinguish the upper and lower bytes on its 16-bit data bus. The 80386 uses four-byte selects, $\overline{BE0}$–$\overline{BE3}$, to distinguish between the different bytes on its 32-bit bus.
2. The 80376 has no bus sizing option. The 80386 can select between either a 32-bit bus or a 16-bit bus by use of the $\overline{BS16}$ input. The 80376 has a 16-bit bus size.
3. The $\overline{NA}$ pin operation in the 80376 is identical to that of the $\overline{NA}$ pin on the 80386 with one exception: the $\overline{NA}$ pin of the 80386 cannot be activated on 16-bit bus cycles (where $\overline{BS16}$ is LOW in the 80386 case), whereas $\overline{NA}$ can be activated on any 80376 bus cycle.
4. The contents of all 80376 registers at reset are identical to the contents of the 80386 registers at reset, except the DX register. The DX register contains a component-stepping identifier at reset, i.e.

   in 80386, after reset DH = 03H indicates 80386
   DL = revision number;
   in 80376, after reset DH = 33H indicates 80376
   DL = revision number.

5. The 80386 uses A_{31} and M/$\overline{IO}$ as a select for numerics coprocessor. The 80376 uses the A_{23} and M/$\overline{IO}$ to select its numerics coprocessor.
6. The 80386 prefetch unit fetches code in four-byte units. The 80376 prefetch unit reads two bytes as one unit (like the 80286 microprocessor). In $\overline{BS16}$ mode, the 80386 takes two consecutive bus cycles to complete a prefetch request. If there is a data read or write request after the prefetch starts, the 80386 will fetch all four bytes before addressing the new request.
7. The 80376 has no paging mechanism.
8. The 80376 starts executing code in what corresponds to the 80386 protected mode. The 80386 starts execution in real mode, which is then used to enter protected mode.
9. The 80386 has a virtual-86 mode that allows the execution of a real mode 8086 program as a task in protected mode. The 80376 has no virtual-86 mode.
10. The 80386 maps a 48-bit logical address into a 32-bit physical address by segmentation and paging. The 80376 maps its 48-bit logical address into a 24-bit physical address by segmentation only.
11. The 80376 uses the 80387SX numerics coprocessor for floating point operations, while the 80386 uses the 80387 coprocessor.
12. The 80386 can execute from 16-bit code segments. The 80376 can **only** execute from 32-bit code Segments.
13. The 80376 has an input called $\overline{FLT}$ which three-states all bidirectional and output pins, including HLDA, when asserted. It is used with ON Circuit Emulation (ONCE).

8.0 INSTRUCTION SET

This section describes the 376 embedded processor instruction set. Table 8.1 lists all instructions along with instruction encoding diagrams and clock counts. Further details of the instruction encoding are then provided in the following sections, which completely describe the encoding structure and the definition of all fields occurring within 80376 instructions.

8.1 80376 Instruction Encoding and Clock Count Summary

To calculate elapsed time for an instruction, multiply the instruction clock count, as listed in Table 8.1 below, by the processor clock period (e.g. 50 ns for an 80376 operating at 20 MHz). The actual clock count of an 80376 program will average 10% more

than the calculated clock count due to instruction sequences which execute faster than they can be fetched from memory.

Instruction Clock Count Assumptions:

1. The instruction has been prefetched, decoded, and is ready for execution.
2. Bus cycles do not require wait states.
3. There are no local bus HOLD requests delaying processor acess to the bus.
4. No exceptions are detected during instruction execution.
5. If an effective address is calculated, it does not use two general register components. One register, scaling and displacement can be used within the clock counts showns. However, if the effective address calculation uses two general register components, add 1 clock to the clock count shown.
6. Memory reference instruction accesses byte or aligned 16-bit operands.

Instruction Clock Count Notation

— If two clock counts are given, the smaller refers to a register operand and the larger refers to a memory operand.

—n = number of times repeated.

—m = number of components in the next instruction executed, where the entire displacement (if any) counts as one component, the entire immediate data (if any) counts as one component, and all other bytes of the instruction and prefix(es) each count as one component.

Misaligned or 32-Bit Operand Accesses:

— If instructions accesses a misaligned 16-bit operand or 32-bit operand on even address add:

2* clocks for read or write.

4** clocks for read and write.

— If instructions accesses a 32-bit operand on odd address add:

4* clocks for read or write.

8** clocks for read and write.

Wait States:

Wait states add 1 clock per wait state to instruction execution for each data access.

Table 8.1. 80376 Instruction Set Clock Count Summary

Instruction	Format	Clock Counts	Number of Data Cycles	Notes
GENERAL DATA TRANSFER				
MOV = Move:				
Register to Register/Memory	1000100w | mod reg r/m	2/2*	0/1*	a
Register/Memory to Register	1000101w | mod reg r/m	2/4*	0/1*	a
Immediate to Register/Memory	1100011w | mod 000 r/m | immediate data	2/2*	0/1*	a
Immediate to Register (Short Form)	1011 w reg | immediate data	2	2	
Memory to Accumulator (Short Form)	1010000w | full displacement	4*	1*	a
Accumulator to Memory (Short Form)	1010001w | full displacement	2*	1*	a
Register/Memory to Segment Register	10001110 | mod sreg3 r/m	22/23*	0/6*	a,b,c
Segment Register to Register/Memory	10001100 | mod sreg3 r/m	2/2*	0/1*	a
MOVSX = Move with Sign Extension				
Register from Register/Memory	00001111 | 1011111w | mod reg r/m	3/6*	0/1*	a
MOVZX = Move with Zero Extension				
Register from Register/Memory	00001111 | 1011011w | mod reg r/m	3/6*	0/1*	a
PUSH = Push:				
Register/Memory	11111111 | mod 110 r/m	7/9*	2/4*	a
Register (Short Form)	01010 reg	4	2	a
Segment Register (ES, CS, SS or DS)	000 sreg2 110	4	2	a
Segment Register (FS or GS)	00001111 | 10 sreg3 000	4	2	a
Immediate	011010s0 | immediate data	4	2	a
PUSHA = Push All	01100000	34	16	a
POP = Pop				
Register/Memory	10001111 | mod 000 r/m	7/9*	2/4*	a
Register (Short Form)	01011 reg	6	2	a
Segment Register (ES, SS or DS)	000 sreg 2 111	25	6	a, b, c
Segment Register (FS or GS)	00001111 | 10 sreg 3 001	25	6	a, b, c
POPA = Pop All	01100001	40	16	a
XCHG = Exchange				
Register/Memory with Register	1000011w | mod reg r/m	3/5**	0/2**	a, m
Register with Accumulator (Short Form)	10010 reg	3	0	
IN = Input from:				
Fixed Port	1110010w | port number	6*	1*	f,k
		26*	1*	f,l
Variable Port	1110110w	7*	1*	f,k
		27*	1*	f,l
OUT = Output to:				
Fixed Port	1110011w | port number	4*	1*	f,k
		24*	1*	f,l
Variable Port	1110111w	5*	1*	f,k
		26*	1*	f,l
LEA = Load EA to Register	10001101 | mod reg r/m	2		

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number of Data Cycles	Notes
SEGMENT CONTROL				
LDS = Load Pointer to DS	11000101 | mod reg r/m	26*	6*	a, b, c
LES = Load Pointer to ES	11000100 | mod reg r/m	26*	6*	a, b, c
LFS = Load Pointer to FS	00001111 | 10110100 | mod reg r/m	29*	6*	a, b, c
LGS = Load Pointer to GS	00001111 | 10110101 | mod reg r/m	29*	6*	a, b, c
LSS = Load Pointer to SS	00001111 | 10110010 | mod reg r/m	26*	6*	a, b, c
FLAG CONTROL				
CLC = Clear Carry Flag	11111000	2		
CLD = Clear Direction Flag	11111100	2		
CLI = Clear Interrupt Enable Flag	11111010	8		f
CLTS = Clear Task Switched Flag	00001111 | 00000110	5		e
CMC = Complement Carry Flag	11110101	2		
LAHF = Load AH into Flag	10011111	2		
POPF = Pop Flags	10011101	7		a, g
PUSHF = Push Flags	10011100	4		a
SAHF = Store AH into Flags	10011110	3		
STC = Set Carry Flag	11111001	2		
STD = Set Direction Flag	11111101	2		
STI = Set Interrupt Enable Flag	11111011	8		f
ARITHMETIC				
ADD = Add				
Register to Register	000000dw | mod reg r/m	2		
Register to Memory	0000000w | mod reg r/m	7**	2**	a
Memory to Register	0000001w | mod reg r/m	6*	1*	a
Immediate to Register/Memory	100000sw | mod000 r/m | immediate data	2/7**	0/2**	a
Immediate to Accumulator (Short Form)	0000010w | immediate data	2		
ADC = Add with Carry				
Register to Register	000100dw | mod reg r/m	2		
Register to Memory	0001000w | mod reg r/m	7**	2**	a
Memory to Register	0001001w | mod reg r/m	6*	1*	a
Immediate to Register/Memory	100000sw | mod010 r/m | immediate data	2/7**	0/2**	a
Immediate to Accumulator (Short Form)	0001010w | immediate data	2		
INC = Increment				
Register/Memory	1111111w | mod000 r/m	2/6**	0/2**	a
Register (Short Form)	01000 reg	2		
SUB = Subtract				
Register from Register	001010dw | mod reg r/m	2		

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number Of Data Cycles	Notes
ARITHMETIC (Continued)				
Register from Memory	0010100w | mod reg r/m	7**	2**	a
Memory from Register	0010101w | mod reg r/m	6*	1	a
Immediate from Register/Memory	100000sw | mod101 r/m | immediate data	2/7**	0/1**	a
Immediate from Accumulator (Short Form)	0010110w | immediate data	2		
SBB = Subtract with Borrow				
Register from Register	000110dw | mod reg r/m	2		
Register from Memory	0001100w | mod reg r/m	7**	2**	a
Memory from Register	0001101w | mod reg r/m	6*	1*	a
Immediate from Register/Memory	100000sw | mod011 r/m | immediate data	2/7**	0/2**	a
Immediate from Accumulator (Short Form)	0001110w | immediate data	2		
DEC = Decrement				
Register/Memory	1111111w | reg001 r/m	2/6**	0/2**	a
Register (Short Form)	01001 reg	2		
CMP = Compare				
Register with Register	001110dw | mod reg r/m	2		
Memory with Register	0011100w | mod reg r/m	5*	1*	a
Register with Memory	0011101w | mod reg r/m	6**	2**	a
Immediate with Register/Memory	100000sw | mod111 r/m | immediate data	2/5*	0/1*	a
Immediate with Accumulator (Short Form)	0011110w | immediate data	2		
NEG = Change Sign	1111011w | mod011 r/m	2/6*	0/2*	a
AAA = ASCII Adjust for Add	00110111	4		
AAS = ASCII Adjust for Subtract	00111111	4		
DAA = Decimal Adjust for Add	00100111	4		
DAS = Decimal Adjust for Subtract	00101111	4		
MUL = Multiply (Unsigned)				
Accumulator with Register/Memory	1111011w | mod100 r/m			
Multiplier—Byte		12–17/15–20	0/1	a,n
—Word		12–25/15–28*	0/1*	a,n
—Doubleword		12–41/17–46*	0/2*	a,n
IMUL = Integer Multiply (Signed)				
Accumulator with Register/Memory	1111011w | mod101 r/m			
Multiplier—Byte		12–17/15–20	0/1	a,n
—Word		12–25/15–28*	0/1*	a,n
—Doubleword		12–41/17–46*	0/2*	a,n
Register with Register/Memory	00001111 | 10101111 | mod reg r/m			
Multiplier—Byte		12–17/15–20	0/1	a,n
—Word		12–25/15–28*	0/1*	a,n
—Doubleword		12–41/17–46*	0/2*	a,n
Register/Memory with Immediate to Register	011010s1 | mod reg r/m | immediate data			
—Word		13–26/14–27*	0/1*	a,n
—Doubleword		13–42/16–45*	0/2*	a,n

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number Of Data Cycles	Notes
ARITHMETIC (Continued)				
DIV = Divide (Unsigned)				
Accumulator by Register/Memory	1111011w mod110 r/m			
Divisor—Byte		14/17	0/1	a, o
—Word		22/25*	0/1*	a, o
—Doubleword		38/43*	0/2*	a, o
IDIV = Integer Divide (Signed)				
Accumulator by Register/Memory	1111011w mod111 r/m			
Divisor—Byte		19/22	0/1	a, o
—Word		27/30*	0/1	a, o
—Doubleword		43/48*	0/2*	a, o
AAD = ASCII Adjust for Divide	11010101 00001010	19		
AAM = ASCII Adjust for Multiply	11010100 00001010	17		
CBW = Convert Byte to Word	10011000	3		
CWD = Convert Word to Double Word	10011001	2		
LOGIC				
Shift Rotate Instructions				
Not Through Carry (**ROL, ROR, SAL, SAR, SHL,** and **SHR**)				
Register/Memory by 1	1101000w mod TTT r/m	3/7**	0/2**	a
Register/Memory by CL	1101001w mod TTT r/m	3/7**	0/2**	a
Register/Memory by Immediate Count	1100000w mod TTT r/m immed 8-bit data	3/7**	0/2**	a
Through Carry (**RCL** and **RCR**)				
Register/Memory by 1	1101000w mod TTT r/m	9/10**	0/2**	a
Register/Memory by CL	1101001w mod TTT r/m	9/10**	10/2**	a
Register/Memory by Immediate Count	1100000w mod TTT r/m immed 8-bit data	9/10**	0/2**	a
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR			
SHLD = Shift Left Double				
Register/Memory by Immediate	00001111 10100100 mod reg r/m immed 8-bit data	3/7**	0/2**	
Register/Memory by CL	00001111 10100101 mod reg r/m	3/7**	0/2**	
SHRD = Shift Right Double				
Register/Memory by Immediate	00001111 10101100 mod reg r/m immed 8-bit data	3/7**	0/2**	
Register/Memory by CL	00001111 10101101 mod reg r/m	3/7**	0/2**	
AND = And				
Register to Register	001000dw mod reg r/m	2		

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number of Data Cycles	Notes
LOGIC (Continued)				
Register to Memory	0010000w mod reg r/m	7**	2**	a
Memory to Register	0010001w mod reg r/m	6*	1*	a
Immediate to Register/Memory	1000000w mod100 r/m immediate data	2/7**	0/2**	a
Immediate to Accumulator (Short Form)	0010010w immediate data	2		
TEST = And Function to Flags, No Result				
Register/Memory and Register	1000010w mod reg r/m	2/5*	0/1*	a
Immediate Data and Register/Memory	1111011w mod000 r/m immediate data	2/5*	0/1*	a
Immediate Data and Accumulator (Short Form)	1010100w immediate data	2		
OR = Or				
Register to Register	000010dw mod reg r/m	2		
Register to Memory	0000100w mod reg r/m	7**	2**	a
Memory to Register	0000101w mod reg r/m	6*	1*	a
Immediate to Register/Memory	1000000w mod001 r/m immediate data	2/7**	0/2**	a
Immediate to Accumulator (Short Form)	0000110w immediate data	2		
XOR = Exclusive Or				
Register to Register	001100dw mod reg r/m	2		
Register to Memory	0011000w mod reg r/m	7**	2**	a
Memory to Register	0011001w mod reg r/m	6*	1*	a
Immediate to Register/Memory	1000000w mod110 r/m immediate data	2/7**	0/2**	a
Immediate to Accumulator (Short Form)	0011010w immediate data	2		
NOT = Invert Register/Memory	1111011w mod010 r/m	2/6**	0/2**	a
STRING MANIPULATION				
CMPS = Compare Byte Word	1010011w	10*	2*	a
INS = Input Byte/Word from DX Port	0110110w	9** 29**	1** 1**	a,f,k a,f,l
LODS = Load Byte/Word to AL/AX/EAX	1010110w	5*	1*	a
MOVS = Move Byte Word	1010010w	7**	2**	a
OUTS = Output Byte/Word to DX Port	0110111w	8** 28**	1** 1**	a,f,k a,f,l
SCAS = Scan Byte Word	1010111w	7*	1*	a
STOS = Store Byte/Word from AL/AX/EX	1010101w	4*	1*	a
XLAT = Translate String	11010111	5*	1*	a
REPEATED STRING MANIPULATION Repeated by Count in CX or ECX				
REPE CMPS = Compare String (Find Non-Match)	11110011 1010011w	5 + 9n**	2n**	a

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number of Data Cycles	Notes
REPEATED STRING MANIPULATION (Continued)				
REPNE CMPS = Compare String				
(Find Match)	11110010 1010011w	5 + 9n**	2n**	a
REP INS = Input String	11110011 0110110w	7 + 6n*	1n*	a,f,k
		27 + 6n*	1n*	a,f,l
REP LODS = Load String	11110011 1010110w	5 + 6n*	1n*	a
REP MOVS = Move String	11110011 1010010w	7 + 4n**	2n**	a
REP OUTS = Output String	11110011 0110111w	6 + 5n*	1n*	a,f,k
		26 + 5n*	1n*	a,f,l
REPE SCAS = Scan String				
(Find Non-AL/AX/EAX)	11110011 1010111w	5 + 8n*	1n*	a
REPNE SCAS = Scan String				
(Find AL/AX/EAX)	11110010 1010111w	5 + 8n*	1n*	a
REP STOS = Store String	11110011 1010101w	5 + 5n*	1n*	a
BIT MANIPULATION				
BSF = Scan Bit Forward	00001111 10111100 mod reg r/m	10 + 3n**	2n**	a
BSR = Scan Bit Reverse	00001111 10111101 mod reg r/m	10 + 3n**	2n**	a
BT = Test Bit				
Register/Memory, Immediate	00001111 10111010 mod 100 r/m immed 8-bit data	3/6*	0/1*	a
Register/Memory, Register	00001111 10100011 mod reg r/m	3/12*	0/1*	a
BTC = Test Bit and Complement				
Register/Memory, Immediate	00001111 10111010 mod 111 r/m immed 8-bit data	6/8*	0/2*	a
Register/Memory, Register	00001111 10111011 mod reg r/m	6/13*	0/2*	a
BTR = Test Bit and Reset				
Register/Memory, Immediate	00001111 10111010 mod 110 r/m immed 8-bit data	6/8*	0/2*	a
Register/Memory, Register	00001111 10110011 mod reg r/m	6/13*	0/2*	a
BTS = Test Bit and Set				
Register/Memory, Immediate	00001111 10111010 mod 101 r/m immed 8-bit data	6/8*	0/2*	a
Register/Memory, Register	00001111 10101011 mod reg r/m	6/13*	0/2*	a
CONTROL TRANSFER				
CALL = Call				
Direct within Segment	11101000 full displacement	9 + m*	2	j
Register/Memory				
Indirect within Segment	11111111 mod 010 r/m	9 + m/12 + m	2/3	a, j
Direct Intersegment	10011010 unsigned full offset, selector	42 + m	9	c, d, j

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number of Data Cycles	Notes
CONTROL TRANSFER (Continued)				
(Direct Intersegment)				
Via Call Gate to Same Privilege Level		64 + m	13	a,c,d,j
Via Call Gate to Different Privilege Level, (No Parameters)		98 + m	13	a,c,d,j
Via Call Gate to Different Privilege Level, (x Parameters)		106 + 8x + m	13 + 4x	a,c,d,j
From 386 Task to 386 TSS		392	124	a,c,d,j
Indirect Intersegment	11111111 mod 011 r/m	46 + m	10	a,c,d,j
Via Call Gate to Same Privilege Level		68 + m	14	a,c,d,j
Via Call Gate to Different Privilege Level, (No Parameters)		102 + m	14	a,c,d,j
Via Call Gate to Different Privilege Level, (x Parameters)		110 + 8x + m	14 + 4x	a,c,d,j
From 386 Task to 386 TSS		399	130	a,c,d,j
JMP = Unconditional Jump				
Short	11101011 8-bit displacement	7 + m		j
Direct within Segment	11101001 full displacement	7 + m		j
Register/Memory Indirect within Segment	11111111 mod 100 r/m	9 + m/14 + m	2/4	a,j
Direct Intersegment	11101010 unsigned full offset, selector	37 + m	5	c,d,j
Via Call Gate to Same Privilege Level		53 + m	9	a,c,d,j
From 386 Task to 386 TSS		395	124	a,c,d,j
Indirect Intersegment	11111111 mod 101 r/m	37 + m	9	a,c,d,j
Via Call Gate to Same Privilege Level		59 + m	13	a,c,d,j
From 386 Task to 386 TSS		401	124	a,c,d,j

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number of Data Cycles	Notes
CONTROL TRANSFER (Continued)				
RET = Return from CALL:				
Within Segment	11000011	12 + m	2	a,j,p
Within Segment Adding Immediate to SP	11000010 | 16-bit displ	12 + m	2	a,j,p
Intersegment	11001011	36 + m	4	a,c,d,j,p
Intersegment Adding Immediate to SP	11001010 | 16-bit displ	36 + m	4	a,c,d,j,p
to Different Privilege Level				
Intersegment		80	4	c,d,j,p
Intersegment Adding Immediate to SP		80	4	c,d,j,p
CONDITIONAL JUMPS				
NOTE: Times Are Jump "Taken or Not Taken"				
JO = Jump on Overflow				
8-Bit Displacement	01110000 | 8-bit displ	7 + m or 3		j
Full Displacement	00001111 | 10000000 | full displacement	7 + m or 3		j
JNO = Jump on Not Overflow				
8-Bit Displacement	01110001 | 8-bit displ	7 + m or 3		j
Full Displacement	00001111 | 10000001 | full displacement	7 + m or 3		j
JB/JNAE = Jump on Below/Not Above or Equal				
8-Bit Displacement	01110010 | 8-bit displ	7 + m or 3		j
Full Displacement	00001111 | 10000010 | full displacement	7 + m or 3		j
JNB/JAE = Jump on Not Below/Above or Equal				
8-Bit Displacement	01110011 | 8-bit displ	7 + m or 3		j
Full Displacement	00001111 | 10000011 | full displacement	7 + m or 3		j
JE/JZ = Jump on Equal/Zero				
8-Bit Displacement	01110100 | 8-bit displ	7 + m or 3		j
Full Displacement	00001111 | 10000100 | full displacement	7 + m or 3		j
JNE/JNZ = Jump on Not Equal/Not Zero				
8-Bit Displacement	01110101 | 8-bit displ	7 + m or 3		j
Full Displacement	00001111 | 10000101 | full displacement	7 + m or 3		j
JBE/JNA = Jump on Below or Equal/Not Above				
8-Bit Displacement	01110110 | 8-bit displ	7 + m or 3		j
Full Displacement	00001111 | 10000110 | full displacement	7 + m or 3		j
JNBE/JA = Jump on Not Below or Equal/Above				
8-Bit Displacement	01110111 | 8-bit displ	7 + m or 3		j
Full Displacement	00001111 | 10000111 | full displacement	7 + m or 3		j
JS = Jump on Sign				
8-Bit Displacement	01111000 | 8-bit displ	7 + m or 3		j
Full Displacement	00001111 | 10001000 | full displacement	7 + m or 3		j

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format			Clock Counts	Number of Data Cycles	Notes
CONDITIONAL JUMPS (Continued)						
JNS = Jump on Not Sign						
8-Bit Displacement	01111001	8-bit displ		7 + m or 3		j
Full Displacement	00001111	10001001	full displacement	7 + m or 3		j
JP/JPE = Jump on Parity/Parity Even						
8-Bit Displacement	01111010	8-bit displ		7 + m or 3		j
Full Displacement	00001111	10001010	full displacement	7 + m or 3		j
JNP/JPO = Jump on Not Parity/Parity Odd						
8-Bit Displacement	01111011	8-bit displ		7 + m or 3		j
Full Displacement	00001111	10001011	full displacement	7 + m or 3		j
JL/JNGE = Jump on Less/Not Greater or Equal						
8-Bit Displacement	01111100	8-bit displ		7 + m or 3		j
Full Displacement	00001111	10001100	full displacement	7 + m or 3		j
JNL/JGE = Jump on Not Less/Greater or Equal						
8-Bit Displacement	01111101	8-bit displ		7 + m or 3		j
Full Displacement	00001111	10001101	full displacement	7 + m or 3		j
JLE/JNG = Jump on Less or Equal/Not Greater						
8-Bit Displacement	01111110	8-bit displ		7 + m or 3		j
Full Displacement	00001111	10001110	full displacement	7 + m or 3		j
JNLE/JG = Jump on Not Less or Equal/Greater						
8-Bit Displacement	01111111	8-bit displ		7 + m or 3		j
Full Displacement	00001111	10001111	full displacement	7 + m or 3		j
JECXZ = Jump on ECX Zero	11100011	8-bit displ		9 + m or 5		j
(Address Size Prefix Differentiates JCXZ from JECXZ)						
LOOP = Loop ECX Times	11100010	8-bit displ		11 + m		j
LOOPZ/LOOPE = Loop with Zero/Equal	11100001	8-bit displ		11 + m		j
LOOPNZ/LOOPNE = Loop While Not Zero	11100000	8-bit displ		11 + m		j
CONDITIONAL BYTE SET						
NOTE: Times Are Register/Memory						
SETO = Set Byte on Overflow						
To Register/Memory	00001111	10010000	mod 000 r/m	4/5*	0/1*	a
SETNO = Set Byte on Not Overflow						
To Register/Memory	00001111	10010001	mod 000 r/m	4/5*	0/1*	a
SETB/SETNAE = Set Byte on Below/Not Above or Equal						
To Register/Memory	00001111	10010010	mod 000 r/m	4/5*	0/1*	a

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number of Data Cycles	Notes
CONDITIONAL BYTE SET (Continued)				
SETNB = Set Byte on Not Below/Above or Equal				
To Register/Memory	00001111 10010011 mod000 r/m	4/5*	0/1*	a
SETE/SETZ = Set Byte on Equal/Zero				
To Register/Memory	00001111 10010100 mod000 r/m	4/5*	0/1*	a
SETNE/SETNZ = Set Byte on Not Equal/Not Zero				
To Register/Memory	00001111 10010101 mod000 r/m	4/5*	0/1*	a
SETBE/SETNA = Set Byte on Below or Equal/Not Above				
To Register/Memory	00001111 10010110 mod000 r/m	4/5*	0/1*	a
SETNBE/SETA = Set Byte on Not Below or Equal/Above				
To Register/Memory	00001111 10010111 mod000 r/m	4/5*	0/1*	a
SETS = Set Byte on Sign				
To Register/Memory	00001111 10011000 mod000 r/m	4/5*	0/1*	a
SETNS = Set Byte on Not Sign				
To Register/Memory	00001111 10011001 mod000 r/m	4/5*	0/1*	a
SETP/SETPE = Set Byte on Parity/Parity Even				
To Register/Memory	00001111 10011010 mod000 r/m	4/5*	0/1*	a
SETNP/SETPO = Set Byte on Not Parity/Parity Odd				
To Register/Memory	00001111 10011011 mod000 r/m	4/5*	0/1*	a
SETL/SETNGE = Set Byte on Less/Not Greater or Equal				
To Register/Memory	00001111 10011100 mod000 r/m	4/5*	0/1*	a
SETNL/SETGE = Set Byte on Not Less/Greater or Equal				
To Register/Memory	00001111 01111101 mod000 r/m	4/5*	0/1*	a
SETLE/SETNG = Set Byte on Less or Equal/Not Greater				
To Register/Memory	00001111 10011110 mod000 r/m	4/5*	0/1*	a
SETNLE/SETG = Set Byte on Not Less or Equal/Greater				
To Register/Memory	00001111 10011111 mod000 r/m	4/5*	0/1*	a
ENTER = Enter Procedure	11001000 16-bit displacement, 8-bit level			
L = 0		10		a
L = 1		14	1	a
L > 1		17 + 8(n − 1)	4(n − 1)	a
LEAVE = Leave Procedure	11001001	6		a

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number of Data Cycles	Notes
INTERRUPT INSTRUCTIONS				
INT = Interrupt:				
Type Specified	11001101 | type			
Via Interrupt or Trap Gate to Same Privilege Level		71	14	c,d,j,p
Via Interrupt or Trap Gate to Different Privilege Level		111	14	c,d,j,p
From 386 Task to 386 TSS via Task Gate		467	140	c,d,j,p
Type 3	11001100			
Via Interrupt or Trap Gate to Same Privilege Level		71	14	c,d,j,p
Via Interrupt or Trap Gate to Different Privilege Level		111	14	c,d,j,p
From 386 Task to 386 TSS via Task Gate		308	138	c,d,j,p
INTO = Interrupt 4 if Overflow Flag Set	11001110			
If OF = 1:		3		
If OF = 0				
Via Interrupt or Trap Gate to Same Privilege Level		71	14	c,d,j,p
Via Interrupt or Trap Gate to Different Privilege Level		111	14	c,d,j,p
From 386 Task to 386 TSS via Task Gate		413	138	c,d,j,p

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number Of Data Cycles	Notes
INTERRUPT INSTRUCTIONS (Continued)				
Bound = Out of Range Interrupt 5 if Detect Value	01100010 | mod reg r/m			
if in Range		10	0	a,c,d,j,o,p
if Out of Range:				
Via Interrupt or Trap Gate to Same Privilege Level		71	14	c,d,j,p
Via Interrupt or Trap Gate to Different Privilege Level		111	14	c,d,j,p
From 386 Task to 386 TSS via Task Gate		398	138	c,d,j,p
INTERRUPT RETURN				
IRET = Interrupt Return	11001111			
To the Same Privilege Level (within Task)		42	5	a,c,d,j,p
To Different Privilege Level (within Task)		86	5	a,c,d,j,p
From 386 Task to 386 TSS		328	138	c,d,j,p
PROCESSOR CONTROL				
HLT = HALT	11110100	5		b
MOV = Move to and from Control/Debug/Test Registers				
CR0 from register	00001111 | 00100010 | 11 eee reg	10		b
Register from CR0	00001111 | 00100000 | 11 eee reg	6		b
DR0–3 from Register	00001111 | 00100011 | 11 eee reg	22		b
DR6–7 from Register	00001111 | 00100011 | 11 eee reg	16		b
Register from DR6–7	00001111 | 00100001 | 11 eee reg	14		b
Register from DR0–3	00001111 | 00100001 | 11 eee reg	22		b
NOP = No Operation	10010000	3		
WAIT = Wait until $\overline{\text{BUSY}}$ Pin is Negated	10011011	6		

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number of Data Cycles	Notes
PROCESSOR EXTENSION INSTRUCTIONS				
Processor Extension Escape	11011TTT | mod LLL r/m TTT and LLL bits are opcode information for coprocessor.	See 80387SX Data Sheet		a
PREFIX BYTES				
Address Size Prefix	01100111	0		
LOCK = Bus Lock Prefix	11110000	0		f
Operand Size Prefix	01100110	0		
Segment Override Prefix				
CS:	00101110	0		
DS:	00111110	0		
ES:	00100110	0		
FS:	01100100	0		
GS:	01100101	0		
SS:	00110110	0		
PROTECTION CONTROL				
ARPL = Adjust Requested Privilege Level				
From Register/Memory	01100011 | mod reg r/m	20/21**	2**	a
LAR = Load Access Rights				
From Register/Memory	00001111 | 00000010 | mod reg r/m	17/18*	1*	a,c,i,p
LGDT = Load Global Descriptor				
Table Register	00001111 | 00000001 | mod 010 r/m	13**	3*	a,e
LIDT = Load Interrupt Descriptor				
Table Register	00001111 | 00000001 | mod 011 r/m	13**	3*	a,e
LLDT = Load Local Descriptor				
Table Register to Register/Memory	00001111 | 00000000 | mod 010 r/m	24/28*	5*	a,c,e,p
LMSW = Load Machine Status Word				
From Register/Memory	00001111 | 00000001 | mod 110 r/m	10/13*	1*	a,e
LSL = Load Segment Limit				
From Register/Memory	00001111 | 00000011 | mod reg r/m			
Byte-Granular Limit		24/27*	2*	a,c,i,p
Page-Granular Limit		29/32*	2*	a,c,i,p
LTR = Load Task Register				
From Register/Memory	00001111 | 00000000 | mod 001 r/m	27/31*	4*	a,c,e,p
SGDT = Store Global Descriptor				
Table Register	00001111 | 00000001 | mod 000 r/m	11*	3*	a
SIDT = Store Interrupt Descriptor				
Table Register	00001111 | 00000001 | mod 001 r/m	11*	3*	a
SLDT = Store Local Descriptor Table Register				
To Register/Memory	00001111 | 00000000 | mod 000 r/m	2/2*	4*	a

Table 8.1. 80376 Instruction Set Clock Count Summary (Continued)

Instruction	Format	Clock Counts	Number of Data Cycles	Notes
PROTECTION CONTROL (Continued)				
SMSW = Store Machine Status Word	00001111 | 00000001 | mod 1 0 0 r/m	2/2*	1*	a, c
STR = Store Task Register				
To Register/Memory	00001111 | 00000000 | mod 0 0 1 r/m	2/2*	1*	a
VERR = Verify Read Accesss				
Register/Memory	00001111 | 00000000 | mod 1 0 0 r/m	10/11**	2**	a,c,i,p
VERW = Verify Write Accesss	00001111 | 00000000 | mod 1 0 1 r/m	15/16**	2**	a,c,i,p

NOTES:
a. Exception 13 fault (general violation) will occur if the memory operand in CS, DS, ES, FS or GS cannot be used due to either a segment limit violation or access rights violation. If a stack limit is violated, and exception 12 (stack segment limit violation or not present) occurs.
b. For segment load operations, the CPL, RPL and DPL must agree with the privilege rules to avoid an exception 13 fault (general protection violation). The segments's descriptor must indicate "present" or exception 11 (CS, DS, ES, FS, GS not present). If the SS register is loaded and a stack segment not present is detected, an exception 12 (stack segment limit violation or not present occurs).
c. All segment descriptor accesses in the GDT or LDT made by this instruction will automatically assert $\overline{\text{LOCK}}$ to maintain descriptor integrity in multiprocessor systems.
d. JMP, CALL, INT, RET and IRET instructions referring to another code segment will cause an exception 13 (general protection violation) if an applicable privilege rule is volated.
e. An exception 13 fault occurs if CPL is greater than 0.
f. An exception 13 fault occurs if CPL is greater than IOPL.
g. The IF bit of the flag register is not updated if CPL is greater than IOPL. The IOPL field of the flag register is updated only if CPL = 0.
h. Any violation of privelege rules as applied to the selector operand does not cause a protection exception; rather, the zero flag is cleared.
i. If the coprocessor's memory operand violates a segment limit or segment access rights, an exception 13 fault (general protection exception) will occur before the ESC instruction is executed. An exception 12 fault (stack segment limit violation or no present) will occur if the stack limit is violated by the operand's starting address.
j. The destination of a JMP, CALL, INT, RET or IRET must be in the defined limit of a code segment or an exception 13 fault (general protection violation) will occur.
k. If CPL $\leq$ IOPL
l. If CPL > IOPL
m. $\overline{\text{LOCK}}$ is automatically asserted, regardless of the presence or absence of the $\overline{\text{LOCK}}$ prefix.
n. The 80376 uses an early-out multiply algorithm. The actual number of clocks depends on the position of the most significant bit in the operand (multiplier). Clock counts given are minimum to maximum. To calculate actual clocks use the following formula:

Actual Clock = if m < > 0 then max ([$\log_2$ |m|], 3) + 9 clocks:
if m = 0 then 12 clocks (where m is the multiplier)

o. An exception may occur, depending on the value of the operand.
p. $\overline{\text{LOCK}}$ is asserted during descriptor table accesses.

8.2 INSTRUCTION ENCODING

Overview

All instruction encodings are subsets of the general instruction format shown in Figure 8.1. Instructions consist of one or two primary opcode bytes, possibly an address specifier consisting of the "mod r/m" byte and "scaled index" byte, a displacement if required, and an immediate data field if required.

Within the primary opcode or opcodes, smaller encoding fields may be defined. These fields vary according to the class of operation. The fields define such information as direction of the operation, size of the displacements, register encoding, or sign extension.

Almost all instructions referring to an operand in memory have an addressing mode byte following the primary opcode byte(s). This byte, the mod r/m byte, specifies the address mode to be used. Certain encodings of the mod r/m byte indicate a second addressing byte, the scale-index-base byte, follows the mod r/m byte to fully specify the addressing mode.

Addressing modes can include a displacement immediately following the mod r/m byte, or scaled index byte. If a displacement is present, the possible sizes are 8, 16 or 32 bits.

If the instruction specifies an immediate operand, the immediate operand follows any displacement bytes. The immediate operand, if specified, is always the last field of the instruction.

Figure 8.1 illustrates several of the fields that can appear in an instruction, such as the mod field and the r/m field, but the Figure does not show all fields. Several smaller fields also appear in certain instructions, sometimes within the opcode bytes themselves. Table 8.2 is a complete list of all fields appearing in the 80376 instruction set. Further ahead, following Table 8.2, are detailed tables for each field.

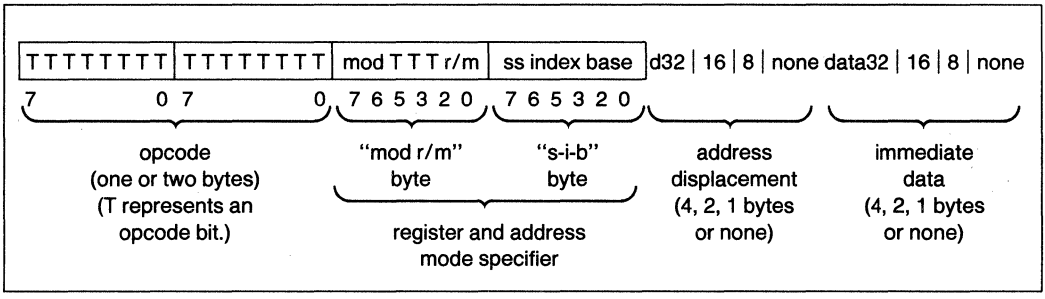


Figure 8.1. General Instruction Format

Table 8.2. Fields within 80376 Instructions

Field Name	Description	Number of Bits
w	Specifies if Data is Byte or Full Size (Full Size is either 16 or 32 Bits	1
d	Specifies Direction of Data Operation	1
s	Specifies if an Immediate Data Field Must be Sign-Extended	1
reg	General Register Specifier	3
mod r/m	Address Mode Specifier (Effective Address can be a General Register)	2 for mod; 3 for r/m
ss	Scale Factor for Scaled Index Address Mode	2
index	General Register to be used as Index Register	3
base	General Register to be used as Base Register	3
sreg2	Segment Register Specifier for CS, SS, DS, ES	2
sreg3	Segment Register Specifier for CS, SS, DS, ES, FS, GS	3
tttn	For Conditional Instructions, Specifies a Condition Asserted or a Condition Negated	4

Note: Table 8.1 shows encoding of individual instructions.

16-Bit Extensions of the Instruction Set

Two prefixes, the operand size prefix (66H) and the effective address size prefix (67H), allow overriding individually the default selection of operand size and effective address size. These prefixes may precede any opcode bytes and affect only the instruction they precede. If necessary, one or both of the prefixes may be placed before the opcode bytes. The presence of the operand size prefix (66H) and the effective address prefix will allow 16-bit data operation and 16-bit effective address calculations.

For instructions with more than one prefix, the order of prefixes is unimportant.

Unless specified otherwise, instructions with 8-bit and 16-bit operands do not affect the contents of the high-order bits of the extended registers.

Encoding of Instruction Fields

Within the instruction are several fields indicating register selection, addressing mode and so on.

ENCODING OF OPERAND LENGTH (w) FIELD

For any given instruction performing a data operation, the instruction will execute as a 32-bit operation. Within the constraints of the operation size, the w field encodes the operand size as either one byte or the full operation size, as shown in the table below.

w Field	Operand Size with 66H Prefix	Normal Operand Size
0	8 Bits	8 Bits
1	16 Bits	32 Bits

ENCODING OF THE GENERAL REGISTER (reg) FIELD

The general register is specified by the reg field, which may appear in the primary opcode bytes, or as the reg field of the "mod r/m" byte, or as the r/m field of the "mod r/m" byte.

Encoding of reg Field When w Field is not Present in Instruction

reg Field	Register Selected with 66H Prefix	Register Selected During 32-Bit Data Operations
000	AX	EAX
001	CX	ECX
010	DX	EDX
011	BX	EBX
100	SP	ESP
101	BP	EBP
110	SI	ESI
111	DI	EDI

Encoding of reg Field When w Field is Present in Instruction

Register Specified by reg Field with 66H Prefix		
reg	Function of w Field	
	(when w = 0)	(when w = 1)
000	AL	AX
001	CL	CX
010	DL	DX
011	BL	BX
100	AH	SP
101	CH	BP
110	DH	SI
111	BH	DI

Register Specified by reg Field without 66H Prefix		
reg	Function of w Field	
	(when w = 0)	(when w = 1)
000	AL	EAX
001	CL	ECX
010	DL	EDX
011	BL	EBX
100	AH	ESP
101	CH	EBP
110	DH	ESI
111	BH	EDI

ENCODING OF THE SEGMENT REGISTER (sreg) FIELD

The sreg field in certain instructions is a 2-bit field allowing one of the CS, DS, ES or SS segment registers to be specified. The sreg field in other instructions is a 3-bit field, allowing the FS and GS segment registers to be specified also.

2-Bit sreg2 Field

2-Bit sreg2 Field	Segment Register Selected
00	ES
01	CS
10	SS
11	DS

3-Bit sreg3 Field

3-Bit sreg3 Field	Segment Register Selected
000	ES
001	CS
010	SS
011	DS
100	FS
101	GS
110	do not use
111	do not use

ENCODING OF ADDRESS MODE

Except for special instructions, such as PUSH or POP, where the addressing mode is pre-determined, the addressing mode for the current instruction is specified by addressing bytes following the primary opcode. The primary addressing byte is the "mod r/m" byte, and a second byte of addressing information, the "s-i-b" (scale-index-base) byte, can be specified.

The s-i-b byte (scale-index-base byte) is specified when using 32-bit addressing mode and the "mod r/m" byte has r/m = 100 and mod = 00, 01 or 10. When the sib byte is present, the 32-bit addressing mode is a function of the mod, ss, index, and base fields.

The primary addressing byte, the "mod r/m" byte, also contains three bits (shown as TTT in Figure 8.1) sometimes used as an extension of the primary opcode. The three bits, however, may also be used as a register field (reg).

When calculating an effective address, either 16-bit addressing or 32-bit addressing is used. 16-bit addressing uses 16-bit address components to calculate the effective address while 32-bit addressing uses 32-bit address components to calculate the effective address. When 16-bit addressing is used, the "mod r/m" byte is interpreted as a 16-bit addressing mode specifier. When 32-bit addressing is used, the "mod r/m" byte is interpreted as a 32-bit addressing mode specifier.

Tables on the following three pages define all encodings of all 16-bit addressing modes and 32-bit addressing modes.

Encoding of Normal Address Mode with "mod r/m" byte (no "s-i-b" byte present):

mod r/m	Effective Address
00 000	DS:[EAX]
00 001	DS:[ECX]
00 010	DS:[EDX]
00 011	DS:[EBX]
00 100	s-i-b is present
00 101	DS:d32
00 110	DS:[ESI]
00 111	DS:[EDI]
01 000	DS:[EAX + d8]
01 001	DS:[ECX + d8]
01 010	DS:[EDX + d8]
01 011	DS:[EBX + d8]
01 100	s-i-b is present
01 101	SS:[EBP + d8]
01 110	DS:[ESI + d8]
01 111	DS:[EDI + d8]

mod r/m	Effective Address
10 000	DS:[EAX + d32]
10 001	DS:[ECX + d32]
10 010	DS:[EDX + d32]
10 011	DS:[EBX + d32]
10 100	s-i-b is present
10 101	SS:[EBP + d32]
10 110	DS:[ESI + d32]
10 111	DS:[EDI + d32]
11 000	register—see below
11 001	register—see below
11 010	register—see below
11 011	register—see below
11 100	register—see below
11 101	register—see below
11 110	register—see below
11 111	register—see below

Register Specified by reg or r/m during Normal Data Operations:		
mod r/m	function of w field	
	(when w = 0)	(when w = 1)
11 000	AL	EAX
11 001	CL	ECX
11 010	DL	EDX
11 011	BL	EBX
11 100	AH	ESP
11 101	CH	EBP
11 110	DH	ESI
11 111	BH	EDI

Register Specified by reg or r/m during 16-Bit Data Operations: (66H Prefix)		
mod r/m	function of w field	
	(when w = 0)	(when w = 1)
11 000	AL	AX
11 001	CL	CX
11 010	DL	DX
11 011	BL	BX
11 100	AH	SP
11 101	CH	BP
11 110	DH	SI
11 111	BH	DI

Encoding of 16-bit Address Mode with "mod r/m" Byte Using 67H Prefix

mod r/m	Effective Address
00 000	DS:[BX + SI]
00 001	DS:[BX + DI]
00 010	SS:[BP + SI]
00 011	SS:[BP + DI]
00 100	DS:[SI]
00 101	DS:[DI]
00 110	DS:d16
00 111	DS:[BX]
01 000	DS:[BX + SI + d8]
01 001	DS:[BX + DI + d8]
01 010	SS:[BP + SI + d8]
01 011	SS:[BP + DI + d8]
01 100	DS:[SI + d8]
01 101	DS:[DI + d8]
01 110	SS:[BP + d8]
01 111	DS:[BX + d8]

mod r/m	Effective Address
10 000	DS:[BX + SI + d16]
10 001	DS:[BX + DI + d16]
10 010	SS:[BP + SI + d16]
10 011	SS:[BP + DI + d16]
10 100	DS:[SI + d16]
10 101	DS:[DI + d16]
10 110	SS:[BP + d16]
10 111	DS:[BX + d16]
11 000	register—see below
11 001	register—see below
11 010	register—see below
11 011	register—see below
11 100	register—see below
11 101	register—see below
11 110	register—see below
11 111	register—see below

Encoding of 32-bit Address Mode ("mod r/m" byte and "s-i-b" byte present):

mod base	Effective Address
00 000	DS:[EAX + (scaled index)]
00 001	DS:[ECX + (scaled index)]
00 010	DS:[EDX + (scaled index)]
00 011	DS:[EBX + (scaled index)]
00 100	SS:[ESP + (scaled index)]
00 101	DS:[d32 + (scaled index)]
00 110	DS:[ESI + (scaled index)]
00 111	DS:[EDI + (scaled index)]
01 000	DS:[EAX + (scaled index) + d8]
01 001	DS:[ECX + (scaled index) + d8]
01 010	DS:[EDX + (scaled index) + d8]
01 011	DS:[EBX + (scaled index) + d8]
01 100	SS:[ESP + (scaled index) + d8]
01 101	SS:[EBP + (scaled index) + d8]
01 110	DS:[ESI + (scaled index) + d8]
01 111	DS:[EDI + (scaled index) + d8]
10 000	DS:[EAX + (scaled index) + d32]
10 001	DS:[ECX + (scaled index) + d32]
10 010	DS:[EDX + (scaled index) + d32]
10 011	DS:[EBX + (scaled index) + d32]
10 100	SS:[ESP + (scaled index) + d32]
10 101	SS:[EBP + (scaled index) + d32]
10 110	DS:[ESI + (scaled index) + d32]
10 111	DS:[EDI + (scaled index) + d32]

NOTE:
Mod field in "mod r/m" byte; ss, index, base fields in "s-i-b" byte.

ss	Scale Factor
00	x1
01	x2
10	x4
11	x8

index	Index Register
000	EAX
001	ECX
010	EDX
011	EBX
100	no index reg**
101	EBP
110	ESI
111	EDI

****IMPORTANT NOTE:**
When index field is 100, indicating "no index register," then ss field MUST equal 00. If index is 100 and ss does not equal 00, the effective address is undefined.

ENCODING OF OPERATION DIRECTION (d) FIELD

In many two-operand instructions the d field is present to indicate which operand is considered the source and which is the destination.

d	Direction of Operation
0	Register/Memory <- - Register "reg" Field Indicates Source Operand; "mod r/m" or "mod ss index base" Indicates Destination Operand
1	Register <- - Register/Memory "reg" Field Indicates Destination Operand; "mod r/m" or "mod ss index base" Indicates Source Operand

ENCODING OF SIGN-EXTEND (s) FIELD

The s field occurs primarily to instructions with immediate data fields. The s field has an effect only if the size of the immediate data is 8 bits and is being placed in a 16-bit or 32-bit destination.

s	Effect on Immediate Data8	Effect on Immediate Data 16|32
0	None	None
1	Sign-Extend Data8 to Fill 16-Bit or 32-Bit Destination	None

ENCODING OF CONDITIONAL TEST (tttn) FIELD

For the conditional instructions (conditional jumps and set on condition), tttn is encoded with n indicating to use the condition (n = 0) or its negation (n = 1), and ttt giving the condition to test.

Mnemonic	Condition	tttn
O	Overflow	0000
NO	No Overflow	0001
B/NAE	Below/Not Above or Equal	0010
NB/AE	Not Below/Above or Equal	0011
E/Z	Equal/Zero	0100
NE/NZ	Not Equal/Not Zero	0101
BE/NA	Below or Equal/Not Above	0110
NBE/A	Not Below or Equal/Above	0111
S	Sign	1000
NS	Not Sign	1001
P/PE	Parity/Parity Even	1010
NP/PO	Not Parity/Parity Odd	1011
L/NGE	Less Than/Not Greater or Equal	1100
NL/GE	Not Less Than/Greater or Equal	1101
LE/NG	Less Than or Equal/Greater Than	1110
NLE/G	Not Less or Equal/Greater Than	1111

ENCODING OF CONTROL OR DEBUG REGISTER (eee) FIELD

For the loading and storing of the Control and Debug registers.

When Interpreted as Control Register Field

eee Code	Reg Name
000	CR0
010	Reserved
011	Reserved
Do not use any other encoding	

When Interpreted as Debug Register Field

eee Code	Reg Name
000	DR0
001	DR1
010	DR2
011	DR3
110	DR6
111	DR7
Do not use any other encoding	

9.0 REVISION HISTORY

The sections significantly revised since version -003 are:

Section 1.0 Added $\overline{FLT}$ pin.

Section 4.4 Added description of FLOAT operation and ONCE Mode. Figure 4.20 is new.

Section 4.6 Added revision identifier information for change to CHMOS IV manufacturing process.

Section 5.0 Both packages now specified for 0°C–115°C case temperature operation. Thermal resistance values changed.

Section 6.3 I_{CC} Max. specifications changed from 400 mA (cold) and 360 mA (hot) to 275 mA (cold, 16 MHz) and 305 mA (cold, 20 MHz).

Section 6.4 HLDA Valid Delay, t_{14}, min. changed from 6 ns to 4 ns. Added 20 MHz A.C. specifications in Table 6.5. Replaced Capacitive Derating Curves in Figures 6.8–6.10 to reflect new manufacturing process. Replaced I_{CC} vs. Frequency data (Figure 6.11) to reflect new specifications.

The sections significantly revised since version -002 are:

Section 1.0 Modified table 1.1. to list pins in alphabetical order.

The sections significantly revised since version -001 are:

Section 2.0 Figure 2.0 was updated to show the 16-bit registers SI, DI, BP and SP.

Section 2.1 Figure 2.2 was updated to show the correct bit polarity for bit 4 in the CR0 register.

Section 2.1 Tables 2.1 and 2.2 were updated to include additional information on the EFLAGs and CR0 registers.

Section 2.3 Figure 2.3 was updated to more accurately reflect the addressing mechanism of the 80376.

Section 2.6 In the subsection **Maskable Interrupt** a paragraph was added to describe the effect of interrupt gates on the IF EFLAGs bit.

Section 2.8 Table 2.7 was updated to reflect the correct power up condition of the CR0 register.

Section 2.10 Figure 2.6 was updated to show the correct bit positions of the BT, BS and BD bits in the DR6 register.

Section 3.0 Figure 3.1 was updated to clearly show the address calculation process.

Section 3.2 The subsection **DESCRIPTORS** was elaborated upon to clearly define the relationship between the linear address space and physical address space of the 80376.

Section 3.2 Figures 3.3 and 3.4 were updated to show the AVL bit field.

Section 3.3 The last sentence in the first paragraph of subsection **PROTECTION AND I/O PERMISSION BIT MAP** was deleted. This was an incorrect statement.

Section 4.1 In the Subsection **ADDRESS BUS ($\overline{BHE}$, $\overline{BLE}$, A_{23}–A_1** last sentence in the first paragraph was updated to reflect the numerics operand addresses as 8000FCH and 8000FEH. Because the 80376 sometimes does a double word I/O access a second access to 8000FEH can be seen.

Section 4.1 The Subsection **Hold Lantencies** was updated to describe how 32-bit and unaligned accesses are internally locked but do not assert the $\overline{LOCK}$ signal.

Section 4.2 Table 4.6 was updated to show the correct active data bits during a $\overline{BLE}$ assertion.

9.0 REVISION HISTORY (Continued)

Section 4.4 This section was updated to correctly reflect the pipelining of the address and status of the 80376 as opposed to "Address Pipelining" which occurs on processors such as the 80286.

Section 4.6 Table 4.7 was updated to show the correct Revision number, 05H.

Section 4.7 Table 4.8 was updated to show the numerics operand register 8000FEH. This address is seen when the 80376 does a DWORD operation to the port address 8000FCH.

Section 5.0 In the first paragraph the case temperatures were updated to reflect the 0°C–115°C for the ceramic package and 0°C–110°C for the plastic package.

Section 6.2 Table 6.2 was updated to reflect the Case Temperature under Bias specification of −65°C–120°C.

Section 6.4 Figure 6.8 vertical axis was updated to reflect "Output Valid Delay (ns)".

Section 6.4 Figure 6.11 was updated to show typical I_{CC} vs Frequency for the 80376.

Section 8.1 The clock counts and opcodes for various instructions were updated to their correct values.

Section 8.2 The section **INSTRUCTION ENCODING** was appended to the data sheet.

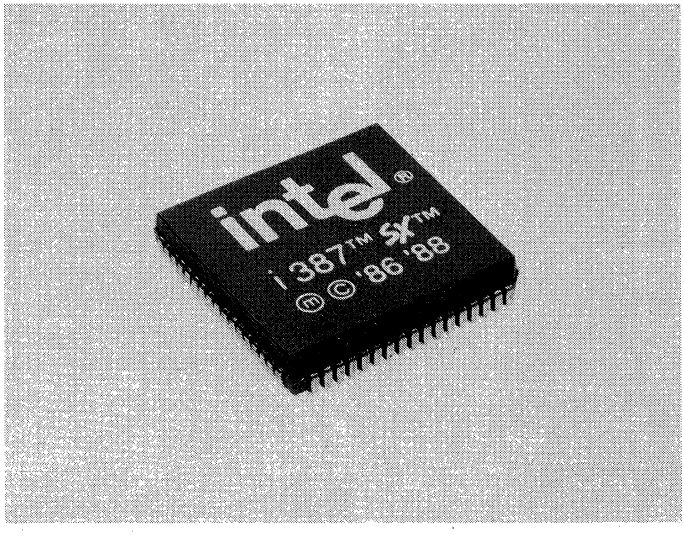
Intel387™ SX MATH COPROCESSOR

- **New Automatic Power Management**
  - **Low Power Consumption**
  - **Typically 100 mA in Dynamic Mode, and 4 mA in Idle Mode**
- **Socket Compatible with Intel387 Family of Math CoProcessors**
  - **Hardware and Software Compatible**
  - **Supported by Over 2100 Commercial Software Packages**
  - **10% to 15% Performance Increase on Whetstone and Livermore Benchmarks**
- **Compatible with the Intel386™ SX Microprocessor**
  - **Extends CPU Instruction Set to Include Trigonometric, Logarithmic, and Exponential**
- **High Performance 80-Bit Internal Architecture**
- **Implements ANSI/IEEE Standard 754-1985 for Binary Floating-Point Arithmetic**
- **Available in a 68-Pin PLCC Package**

  See Intel Packaging Specification, Order #231369

The Intel387™ SX Math CoProcessor is an extension to the Intel386™ SX microprocessor architecture. The combination of the Intel387™ SX with the Intel386™ SX microprocessor dramatically increases the processing speed of computer application software that utilizes high performance floating-point operations. An internal Power Management Unit enables the Intel387™ SX to perform these floating-point operations while maintaining very low power consumption for portable and desktop applications. The internal Power Management Unit effectively reduces power consumption by 95% when the device is idle.

The Intel387™ SX Math CoProcessor is available in a 68-pin PLCC package, and is manufactured on Intel's advanced 1.0 micron CHMOS IV technology.



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For the complete data sheet on this product, refer to the 1993 Microprocessors handbook.

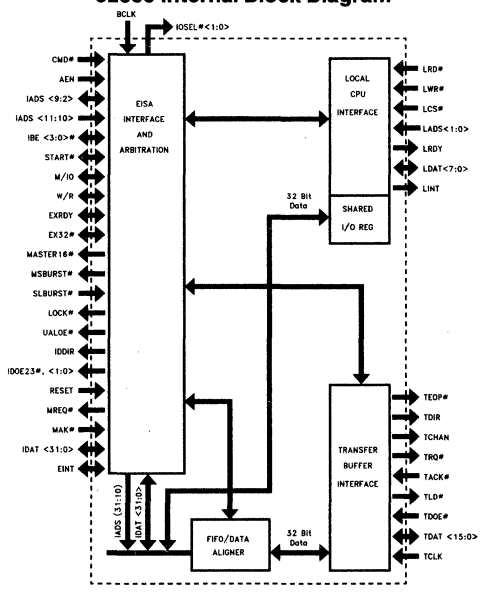
October 1992
Order Number: 240225-009

82355
BUS MASTER INTERFACE CONTROLLER (BMIC)

- **Designed for use in 32-Bit EISA Bus Master Expansion Board Designs**
  - **— Integrates Three Interfaces (EISA, Local CPU, and Transfer Buffer)**
- **Supports 16- and 32-Bit Burst Transfers**
  - **— 33 Mbytes/Sec Maximum Data Transfers**
- **Supports 32-Bit Non-Burst and Mismatched Data Size Transfers**
- **Supports 32-Bit EISA Addressability (4 Gigabyte)**
- **Two independent Data Transfer Channels with 24-Byte FIFOs**
  - **— Expansion Board Timing and EISA Timing Operate Asynchronously**
- **Supports Peek/Poke Operation with the Ability to Access Individual Locations in EISA Memory or I/O space**
- **Automatically Handles Misaligned Doubleword Data Transfers with No Performance Penalty**
- **Supports Automatic Handling of Complete EISA Bus Master Protocol**
  - **— EISA Arbitration/Preemption**
  - **— Cycle Timing and Execution**
  - **— Byte Alignment**
  - **— 1K Boundary Detection**
- **Supports Local Data Transfer Protocol Similar to Traditional DMA**
- **Supports a General Purpose Command and Status Interface**
  - **— Local and EISA System Interrupt Support**
  - **— General Purpose Information Transfers**
  - **— Set-and-Test-Functions in I/O Space (Semaphore Function)**
  - **— Supports the EISA Expansion Board ID Function**
- **Supports Decode of Slot Specific and General I/O Addresses**
- **132-Pin JEDEC PQFP Package**

  (See Packaging Specification Order #240800, Package Type NG)

82355 Internal Block Diagram



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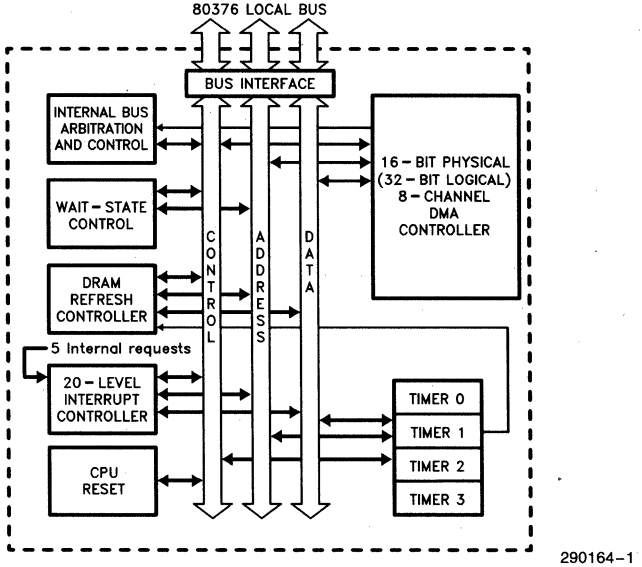
82370
INTEGRATED SYSTEM PERIPHERAL

- **High Performance 32-Bit DMA Controller for 16-Bit Bus**
  - **— 16 MBytes/Sec Maximum Data Transfer Rate at 16 MHz**
  - **— 8 Independently Programmable Channels**
- **20-Source Interrupt Controller**
  - **— Individually Programmable Interrupt Vectors**
  - **— 15 External, 5 Internal Interrupts**
  - **— 82C59A Superset**
- **Four 16-Bit Programmable Interval Timers**
  - **— 82C54 Compatible**
- **Software Compatible to 82380**
- **Programmable Wait State Generator**
  - **— 0 to 15 Wait States Pipelined**
  - **— 1 to 16 Wait States Non-Pipelined**
- **DRAM Refresh Controller**
- **80376 Shutdown Detect and Reset Control**
  - **— Software/Hardware Reset**
- **High Speed CHMOS III Technology**
- **100-Pin Plastic Quad Flat-Pack Package and 132-Pin Pin Grid Array Package**

  (See Packaging Handbook Order #240800-001, Package Type NG or Package Type A)
- **Optimized for Use with the 80376 Microprocessor**
  - **— Resides on Local Bus for Maximum Bus Bandwidth**
  - **— 16 MHz Clock**

The 82370 is a multi-function support peripheral that integrates system functions necessary in an 80376 environment. It has eight channels of high performance 32-bit DMA (32-bit internal, 16-bit external) with the most efficient transfer rates possible on the 80376 bus. System support peripherals integrated into the 82370 provide Interrupt Control, Timers, Wait State generation, DRAM Refresh Control, and System Reset logic.

The 82370's DMA Controller can transfer data between devices of different data path widths using a single channel. Each DMA channel operates independently in any of several modes. Each channel has a temporary data storage register for handling non-aligned data without the need for external alignment logic.



Internal Block Diagram

For the complete data sheet on this product, refer to the 1993 Microprocessors handbook.

September 1991
Order Number: 290164-005

82596DX AND 82596SX HIGH-PERFORMANCE 32-BIT LOCAL AREA NETWORK COPROCESSOR

- **Performs Complete CSMA/CD Medium Access Control (MAC) Functions—Independently of CPU**
  - **— IEEE 802.3 (EOC) Frame Delimiting**
  - **— HDLC Frame Delimiting**
- **Supports Industry Standard LANs**
  - **— IEEE TYPE 10BASE-T (TPE), IEEE TYPE 10BASE5 (Ethernet*), IEEE TYPE 10BASE2 (Cheapernet), IEEE TYPE 1BASE5 (StarLAN), and the Proposed Standard TYPE 10BASE-F**
  - **— Proprietary CSMA/CD Networks Up to 20 Mb/s**
- **On-Chip Memory Management**
  - **— Automatic Buffer Chaining**
  - **— Buffer Reclamation after Receipt of Bad Frames; Optional Save Bad Frames**
  - **— 32-Bit Segmented or Linear (Flat) Memory Addressing Formats**
- **82586 Software Compatible**
- **Optimized CPU Interface**
  - **— 82596DX Bus Interface Optimized to Intel's 32-Bit i386™DX**
  - **— 82596SX Bus Interface Optimized to Intel's 16-Bit i386™SX**
  - **— Supports Big Endian and Little Endian Byte Ordering**
- **High-Performance 16-/32-Bit Bus Master Interface**
  - **— 66-MB/s Bus Bandwidth**
  - **— 33-MHz Clock, Two Clocks Per Transfer**
  - **— Bus Throttle Timers**
  - **— Transfers Data at 100% of Serial Bandwidth**
  - **— 128-Byte Receive FIFO, 64-Byte Transmit FIFO**
- **Network Management and Diagnostics**
  - **— Monitor Mode**
  - **— 32-Bit Statistical Counters**
- **Self-Test Diagnostics**
- **Configurable Initialization Root for Data Structures**
- **High-Speed, 5-V, CHMOS** IV Technology**
- **132-Pin Plastic Quad Flat Pack (PQFP) and PGA Package**

  (See Packaging Specifications Order Number: 240800-001, Package Type KU and A)

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*Ethernet is a registered trademark of Xerox Corporation.
**CHMOS is a patented process of Intel Corporation.

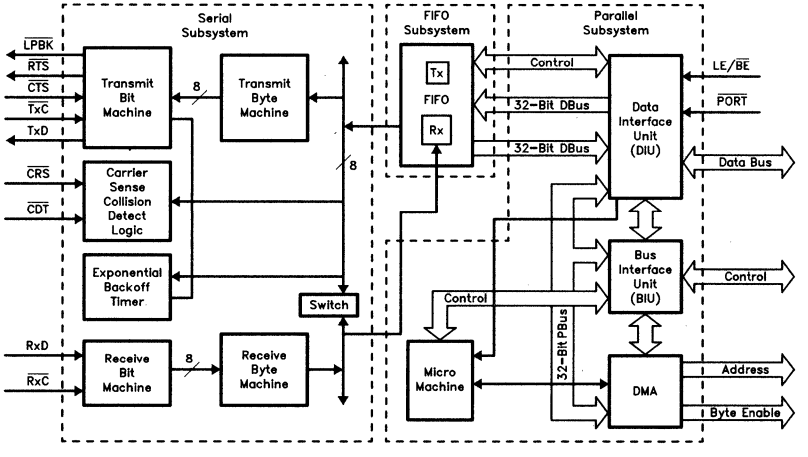

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Figure 1. 82596DX/SX Block Diagram

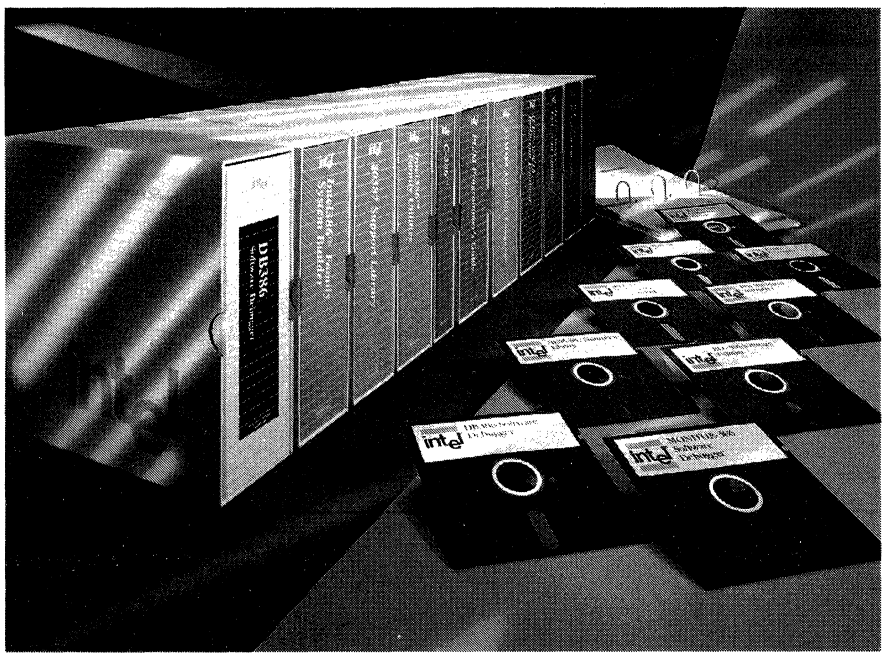
For the complete data sheet on this product, refer to the 1993 Connectivity handbook.

October 1992
Order Number: 290219-005

i376™ Processor Development Tools

27

INTEL386™ AND INTEL486™ FAMILY DEVELOPMENT SUPPORT



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COMPREHENSIVE DEVELOPMENT SUPPORT FOR THE INTEL386™ AND INTEL486™ FAMILIES OF MICROPROCESSORS

The perfect complement to the Intel386™ and i486™ microprocessor family is a comprehensive development solution. Intel provides a complete, synergistic hardware and software development toolset, that delivers full access to the power of the Intel386 and i486 microprocessor family architectures.

Intel development tools are easy to use, yet powerful, with an up-date user interface and productivity boosting features such as symbolic debugging. Each tool is designed to help move your application from the lab to the market.

If what interests you is getting the best product to market in as little time as possible, Intel is the choice.

27

August 1992
Order Number: 280808-007

intel

FEATURES

- Comprehensive support for the full 32 bit Intel386 and Intel486 microprocessor architectures—includes protected mode, 4 gigabyte physical memory addressing, and Intel486 microprocessor on-chip cache and numerics
- In-circuit emulators provide a standard windowed interface that is common across Intel debug tools and architectures
- Emulators also feature a source line display and symbolics to allow debugging in the context of the original program
- Intel high-level languages provide architectural extensions for manipulating hardware directly without assembly language routines
- Languages provide a common object code format (Intel OMF386™) that supports symbolic debug and permits the intermixing of modules written in various languages
- ROM-able code is output directly from the language tools, significantly reducing the effort necessary to integrate software into the final target system
- Extensive support for the Intel family of math coprocessors
- Operation in DOS IBM PC AT and PS/2 Model 60 and 80, running DOS.

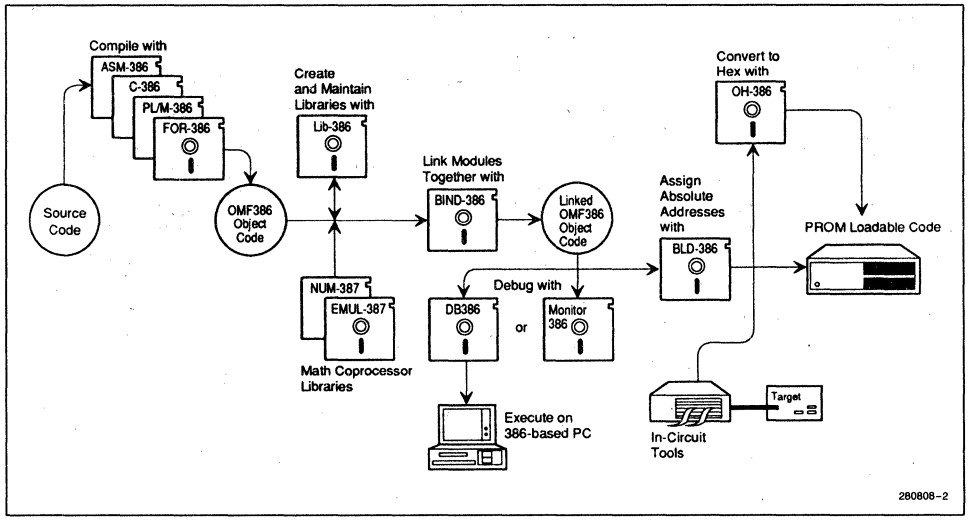

Figure 1: Intel Microprocessor Development Environment

FEATURES

ASM-386/486 MACRO ASSEMBLER

Intel's ASM 386 macro assembler for the Intel386 and Intel486 Families offers many features normally found only in high-level languages. The macro facility in ASM 386 saves development time by allowing common program sequences to be coded only once. The assembly language is strongly typed, performing extensive checks on the usage of variables and labels.

Other Intel ASM 386 features include:

- "High-level" assembler mnemonics to simplify the language
- Structures and records for data representation
- Support for Intel's standard object code format for source-level symbolic debug, and for linking object modules from other Intel386 and Intel486 microprocessor languages
- Full support for processor and math coprocessor instruction sets
- A "MOD486" switch for support of the i486 microprocessor instructions
- 16 bit or 32 bit address overrides
- Supports development for Virtual 86, Real, 286 Protected, and 386 Protected modes

iC386/486 COMPILER

Intel's iC-386 compiler combines the power of C programming language with special features for architectural support and code efficiency. The compiler produces code for Intel386 and Intel486 processors from C source files, and conforms to the 1989 ANSI standard (ANS X3.159-1989) for the C programming language.

Key Intel iC-386 features include:

- Controls to tailor the compilation for each step of your application development process
- In-line versions of many ANSI-standard library functions
- Expanded memory support (LIM Version 3.0 and higher) for large applications
- Object code (including supplied run-time libraries) suitable for ROM
- Three different levels of optimization
- A choice of three segmentation memory models (small, compact, and flat) to create compact and efficient code
- In-line processor-specific functions and time-saving macros that provide access to the special features of the Intel386 and Intel486 processors
- In-line floating-point instructions for the Intel387™ numerics coprocessor and Intel486 processor floating-point unit
- Time-saving macros and functions to help assembly language routines interface with Intel's high-level programming languages
- The standard C run-time library plus libraries for floating-point support and the iRMX® III C interface library
- An easy interface to Intel's non-C programming languages
- Support for source-level debugging
- Programming with subsystems, allowing mixed segmentation memory models
- Extensions to the 1989 ANSI C standard for compatibility with previous versions Intel C
- Fast and efficient functions for common programming tasks

PL/M-386/486 COMPILER

Intel's PL/M-386 is a structured high-level system implementation language for the Intel386 and Intel486 Families. PL/M-386 supports the implementation of protected operating system software by providing built-in procedures and variables to access the Intel386 and Intel486 architectures. For efficient code generation, PL/M-386 features four levels of optimization, a virtual symbol table, and four models of program size and memory usage.

Other Intel PL/M-386 features include:

- The ability to define a procedure as an interrupt handler as well as facilities for generating interrupts
- Direct support of input and output from microprocessor ports
- Upward compatibility with Intel PL/M-86 and PL/M-286 source code
- A "MOD486" compiler switch for Intel486 microprocessor instruction generation

PL/M-386 combines the benefits of a high-level language with the ability to access the Intel386 and Intel486 architectures. For the development of systems software, PL/M-386 is a costeffective alternative to assembly language programming.

FORTRAN-386/486 COMPILER

Intel's FORTRAN-386 compiler is a cross-compiler that supports the entire Intel386 family of components and Intel486 microprocessors (when operating in the 386 chip mode) microprocessors.

FORTRAN-386 features high-level support for floating-point calculations, transcendentals, interrupt procedures, and run-time exception handling. FORTRAN-386 meets the ANSI FORTRAN-77 language subset specification and supports extensions endorsed by the Department of Defense (DOD), extensions that support programs written for the ANSI FORTRAN 66 standard, and extensions that support the Intel386 microprocessor and related numerics coprocessors.

To aid in the development and debugging process, the compiler generates warning and error messages and an optional listing file. The listing file can include symbol cross-reference tables and a listing of the generated Intel386 microprocessor assembly-language instructions. Library routines are reentrant and ROMable.

Other Intel FORTRAN-386 compiler features include:

- Object code can be configured to reside in either RAM or ROM
- The program code can be optimized for execution speed or memory size
- Source-level debugging is supported via the rich symbolics provided in the object module format (Intel OMF386)
- Support for the proposed REALMATH IEEE floating point standard

RLL-386/486 RELOCATION, LINKAGE, AND LIBRARY TOOLS

The RLL 386™ relocation, linkage, and library tools feature comprehensive support of the full Intel386 and Intel486 architectures. The tools link separate modules, build object libraries, link in Intel387 support, build tasks to execute under protected mode, or multitasking, memory protected software. RLL-386 supports loadable, linkable, and bootloadable Intel object module formats; and supports all segmentation models. RLL-386 consists of the following:

Binder — for linking multiple object modules into a single program and resolving references between modules.

Builder — for producing absolute object modules, assigning addresses, and creating protected mode data structures.

Librarian — for creating and maintaining libraries of object modules.

EMUL-387, NUM-387 NUMERICS SUPPORT LIBRARIES

Intel's EMUL-387 and NUM-387 Numerics Libraries fully support the Intel387™, Intel 387 DX, Intel 387 SX math coprocessors and the Intel486 internal numerics unit—whether an actual math coprocessor is used in the final system or not.

For Intel386 microprocessor based applications without a math coprocessor, EMUL-387, a numerics software emulator, will execute instructions as though the coprocessor were present. Its functionality is identical to that of the math coprocessor. It is ideal for prototyping and debugging floating-point application software independent of hardware. Further, this permits portability of application code regardless of the presence of math coprocessor hardware in target systems.

For applications with a math coprocessor, NUM-387 numerics support library provides Intel's ASM 386, C-386, PL/M-386, and FORTRAN-386 language users with enhanced numeric data processing capability. With the library, it is easy for programs to do floating point arithmetic. Programmers can bind in library modules to do trigonometric, logarithmic and other numeric functions.

The user is guaranteed accurate, reliable results for all appropriate inputs.

Intel's NUM-387 support library is a collection of four functionally distinct libraries:

- Common elementary function library routines perform algebraic, logarithmic, exponential, trigonometric, and hyperbolic operations on real and complex numbers, as well as real-to-integer conversions; the routines extend the ranges of the coprocessor instructions
- Initialization library routines set up the numerics processing environment for the Intel386 family of processors with an Intel387, DX, or SX or true software emulator
- Decimal conversion library routines convert floating-point numbers from one Intel387, DX, or SX binary storage format to another, or from ASCII decimal strings to Intel387, DX, or SX binary floating-point format and vice versa
- Exception handling library routines make writing numerics exception handlers easier

All support library modules are in Intel386 microprocessor object module format (Intel OMF-386) so they can be linked with the object output of any Intel language. All routines are reentrant and ROMable.

By using Intel's NUM-387, the user is guaranteed that the numeric software meets industry standard (ANSI/IEEE standard for binary floating point arithmetic, 754-1985) and is portable, thus maintaining software investment.

DB-386 Software Debugger

Intel's DB-386 is a PC-based software development environment with source-level symbolic debug capabilities for object modules produced by Intel's assembler and high-level language compilers. This software debug environment allows Intel386 microprocessor code to be executed and debugged directly on a Intel386 DX or Intel386 SX microprocessor based PC, without any additional target hardware required. With Intel's standard windowed human interface, users can focus their efforts on finding bugs rather than spending time learning and manipulating the debug environment.

Other Intel DB-386 features include:

- A run-time interface allows protected-mode Intel386 microprocessor programs to be executed directly on a Intel386 DX or Intel386 SX microprocessor based PC
- Drop-down menus make the tool easy to learn for new or casual users. A command line interface is also provided for more complex problems
- Watch windows (which display user-specified variables), trace points, and breakpoints (including fixed, temporary, and conditional) can be set and modified as needed
- The user can browse source and callstacks, observe processor registers, and access watch window variables by either pull down menus or by a single keystroke, using function keys
- The user need not know whether a variable is an unsigned integer, a real, or a structure—the debugger uses the wealth of typing information available in Intel languages to display program variables in their respective type formats
- DB-386 supports the Intel486 microprocessor when operated in the Intel386 microprocessor mode

Intel386 and Intel486 Family In-Circuit Tools

Intel in-circuit emulators are used in many different debug environments including the design and test of: PC BIOS software and motherboard hardware, Intel386 and Intel486 based single board computers, and application and operating system software for DOS-based, ROM-based, and UNIX-based systems.

The Intel386 and Intel486 In-Circuit Emulators (ICE™) take advantage of exclusive Intel technology to provide accurate emulation for Intel's 80386 SX, 80386 DX, 80376, and 80486 microprocessors. Special access to internal processor states provides information not available to emulators which simply monitor the external buses. Emulators which do not have access to the internal processor conditions cannot guarantee accurate display of instructions executed by the microprocessor. With an Intel In-circuit Emulator you can be certain that the emulator is displaying accurate execution history, even when executing code from the on-chip cache memory of the Intel486.

The DOS hosted Intel386 DX and Intel386 SX emulators feature a windowed, menu-driven, human interface which provides easy access to the powerful features of these emulators. This makes it easy for novice or infrequent users to get the most out of every debug session. This interface features multiple windows which

allow you to simultaneously view source code, assembly code, memory, trace, variables, and registers. This interface is fully symbolic when used with Intel languages.

All of the emulators feature a combination of powerful and flexible breakpoints. The products use a combination of software breakpoints, hardware breakpoints, and on-chip debug registers to provide a rich set of recognition logic. Flexible breakpoints make it possible to set breakpoints on instruction execution and/or any possible bus event.

Trace filtering provides the ability to select the information captured in the trace buffer. ICE-386 SX allows capture of solely bus cycle information or both bus cycle and execution information. In addition, the ICE-386 DX can filter wait-state information from the trace buffer. ICE-486 provides the most flexible trace collection by allowing capture of information by any combination of bus cycle type including filtering of wait states, by instructions only, or by both bus cycles and instructions.

Other features of Intel emulators include:

- Unparalleled support of the Intel386 and Intel486 architectures, notably the native protected mode
- Emulation at clock speeds to 33 MHz, and full featured trigger and trace capabilities
- The Intel386 family emulators are convertible using removable probes to support the 80386 DX and 80386 SX microprocessors. The Intel486 processor is also supported via a product upgrade.

Relocatable Expanded Memory

Designed to enhance your existing ICE-486 and the ICD-486 debugger (REM486 is included with ICE-486 and an option for ICD-486). This optional relocatable expansion memory board adds 2 Mbyte of memory which the ICE or ICD can use in place of memory on the user target board.

ONCE™-386 and Transmuter Adapters

If you have a surface mount Intel386 SX microprocessor design using 100-pin PQFP parts, Intel ICE emulators have on-circuit emulation (ONCE™) capability. With surface mounted components, the ICE-386 SX emulator cabling clamps over the part, tri-stating the component, and allowing the emulator to operate. This allows you to debug manufactured boards without resoldering. For early target load development, a transmuter adapter can be used. The transmuter provides a better connection technique for debugging systems where the adapter cable will have to be attached and removed many times (like in prototype development).

ICD-486 In-Circuit Debugger

The ICD-486 In-circuit Debugger provides a low-cost alternative for full speed in-target Intel486 development. ICD-486 implements a subset of ICE functionality including: symbolic debugging, debug of high-speed cached applications, software and debug register breakpoints, and in-circuit operation.

Worldwide Service, Support, and Training

To augment its developing tools, Intel offers field application engineering expertise, hotline technical support, and on-site service.

Intel also offers Software Support which includes technical software information, automatic distributions of software and documentation updates, *iCOMMENTS* publication, remote diagnostic software, and development tools troubleshooting guide.

Intel's 90-day Hardware Support package includes technical hardware information, telephone support, warranty on parts, labor, material, and on-site hardware support.

Intel Development Tools also offers a 30-day, money-back guarantee to customers who are not satisfied after purchasing any Intel development tool.

FEATURES

PRODUCT SUPPORT MATRIX

Product	Component			Host
	i486	386 DX	386 SX	DOS 3.x and 5.0
ASM-386 Macro Assembler	✓	✓	✓	✓
iC-386 Compiler	✓	✓	✓	✓
PL/M-386 Compiler	✓	✓	✓	✓
FORTRAN-386 Compiler	✓	✓	✓	✓
RLL-386 Relocation, Linkage, Library, Support Tools	✓	✓	✓	✓
NUM-387 Libraries	✓	✓	✓	✓
EMUL-387 Libraries	NA	✓	✓	✓
In-Circuit Emulators	✓	✓	✓	✓
In-Circuit Debugger	✓			✓
DB-386 Software Debugger	✓	✓	✓	✓

ORDERING INFORMATION

386™/i486™ FAMILY DOS HOSTED DEVELOPMENT KIT ORDER CODES

Software Order Codes

All software supports 386 and 486 microprocessor families except where indicated.

DKIT386C Compiler Software Development Kit (See following content list).

D86ASM386NL ASM macro assembler for PC-DOS systems.

D86C386NL DOS resident, ANSI standard (ANS X3.159-1989) C compiler.

D86PLM386NL DOS resident PL/M compiler.

D86FOR386NL DOS resident Fortan Compiler.

D86RLL386NL DOS resident software development package. Contains Binder (for linking separately compiled modules), a Builder (for configuring protected multi-tasking systems), a cross reference Mapper, and a Librarian. Use this tool in conjunction with Intel's 80386 compilers and macro assembler.

DB386 DOS S/W debugger.

The Intel Basic Software Development Kit for the DOS hosted environment includes:

iC386 compiler
ASM386 assembler
RLL386 relocation linker and locator
NUM387 numerics library
EMUL387 math coprocessor emulator library
DB386 software debugger
OMF386LOAD loader development object module format documentation

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ORDERING INFORMATION

IN-CIRCUIT TOOL ORDER CODES

All In-circuit emulator codes include: control unit, power supply, processor module, Stand-Alone Self Test board, bus Isolation Board, and DOS host software and serial interface cable.

ICE386SX25V	ICE-386 SX In-circuit emulator for the Intel386 SX component to 25 MHz.
pICE386SX20D	ICE-386 SX In-circuit emulator for the 80386 SX component to 20 MHz.
pICE386DX25DZ	ICE-386 DX In-circuit emulator for the 80386 DX component to 25 MHz.
ICE386DX33D	ICE-386 DX In-circuit emulator for the 80386 DX component to 33 MHz.
ICD48650D	In-circuit debugger for the 80486 microprocessor to 50 MHz.
pICE48633DZ	ICE-486 In-circuit emulator for the 80486 component to 33 MHz.

ICE CONVERSION KITS

KBASECONC	Converts ICE-486 to ICE-376, ICE-386 SX, or ICE-386 DX.
KBASECONV	Converts ICE-386 SX or ICE-386 DX to ICE-486.
TOICE386SX20D	Converts ICE-386 DX to ICE-386 SX 20 MHz.
TOICE386DX25D	Converts ICE-386 SX to ICE-386 DX 20 MHz.
TOICE48633D	Converts ICE-386 SX or ICE-386 DX to ICE-486 33 MHz.

ADDITIONAL TOOL ORDER CODES

386SXONCE Kit	100 pin PQFP to 132 pin PGA adaptor kit.
REM486A	2 Mbyte relocatable expansion memory option for ICD-486 (included with ICE-486).

To order your Intel Development Tool product, for more information, or for the number of your nearest sales office or distributor, call 800-874-6835 (North America). For literature on other Intel products call 800-548-4725 (North America). Outside of North America, please contact your local Intel sales office or distributor for more information.

intel®

TRANS 186 → 376 ASSEMBLY CODE TRANSLATOR

270919-1

To Order TRANS 186 → 376 Software, contact your local Intel sales office

TRANS 186 → 376 PRESERVES YOUR PROGRAMMING INVESTMENT

When your embedded application outgrows the 80C186 family, TRANS 186 → 376 is ready to help you upgrade to the 376™ Embedded Processor. TRANS 186 → 376 is a DOS-based tool to automate the translation of Intel ASM86 source code to ASM386 source code. This program can actually help protect the man-years of investment in your original 86 software.

TRANS 186 → 376 LOWERS THE 32-BIT BARRIER

TRANS 186 → 376 accepts 16-bit source code written for any member of the 8086/8088 and 80C186/80C188 families. The output source code, with its 32-bit offsets, is suitable for Protected Mode execution on the 376 Embedded Processor or any 386™, 386SX, or 486™ microprocessor. The time you save by recycling your software can be applied toward system enhancements.

You control TRANS 186 → 376 operation from either the DOS command line or a control file. Major control switches cover:

- Choice of FLAT model or LARGE16 memory environment
- Redefinition of segments
- Optional 32-bit data declaration

TRANS 186 → 376 translates your routines on a line-by-line basis, converting as much code as possible. Whenever the tool does not have enough information to make conversions, it highlights the code section with messages, alerting you to edit by hand. TRANS 186 → 376 can write the ASM86 source code as comments in the ASM386 source file for side-by-side comparison.

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* PC AT and PC-DOS are trademarks of IBM.
**MS-DOS is a trademark of Microsoft Corporation.

November 1990
Order Number: 270919-001

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TRANS 186 → 376 ASSEMBLY CODE TRANSLATOR

TRANS 186 → 376 COMPLEMENTS OTHER DEVELOPMENT TOOLS

Upon request, TRANS 186 → 376 generates a build file for the Intel System Builder, BLD386. This allows you to get your software running with only minimal BLD386 experience. A 72-page manual accompanies the TRANS 186 → 376 tool. The manual coverage includes:

- Practical tips on the overall conversion process
- Initializing the CPU and generating Protected Mode data structures
- Producing code for emulators and debuggers

Your 80C186 experience can release the power of the 376 Embedded Processor with the TRANS 186 → 376 Assembly Language Translator as your partner.

System requirements: PC AT* or compatible computer with PC-DOS* or MS-DOS** operating system version 3.0 or later, hard disk, and 512K RAM.

CAN 82527 Data Sheet 28

82527
SERIAL COMMUNICATIONS CONTROLLER CONTROLLER AREA NETWORK PROTOCOL

Automotive

- **Supports CAN Specification 2.0**
  - **— Standard Data and Remote Frames**
  - **— Extended Data and Remote Frames**
- **Programmable Global Mask**
  - **— Standard Message Identifier**
  - **— Extended Message Identifier**
- **15 Message Objects of 8-Byte Data Length**
  - **— 14 Tx/Rx Buffers**
  - **— 1 Rx Buffer with Programmable Mask**
- **Flexible CPU Interface**
  - **— 8-Bit Multiplexed**
  - **— 16-Bit Multiplexed**
  - **— 8-Bit Non-Multiplexed (Synchronous/Asynchronous)**
  - **— Serial Interface**
- **Programmable Bit Rate**
- **Programmable Clock Output**
- **Flexible Interrupt Structure**
- **Flexible Status Interface**
- **Configurable Output Driver**
- **Configurable Input Comparator**
- **Two 8-Bit Bidirectional I/O Ports**
- **44-Lead PLCC Package**
- **Pinout Compatibility with the 82526**

The 82527 serial communications controller is a highly integrated device that performs serial communication according to the CAN protocol. It performs all serial communication functions such as transmission and reception of messages, message filtering, transmit search, and interrupt search with minimal interaction from the host microcontroller, or CPU.

The 82527 is Intel's first device to support the standard and extended message frames in CAN Specification 2.0 Part B. It has the capability to transmit, receive, and perform message filtering on extended message frames. Due to the backwardly compatible nature of CAN Specification 2.0, the 82527 also fully supports the standard message frames in CAN Specification 2.0 Part A.

The 82527 features a powerful CPU interface that offers flexibility to directly interface to many different CPUs. It can be configured to interface with CPUs using an 8-bit multiplexed, 16-bit multiplexed, or 8-bit non-multiplexed address/data bus for Intel and non-Intel architectures. A flexible serial interface is also available when a parallel CPU interface is not required.

The 82527 provides storage for 15 message objects of 8-byte data length. Each message object can be configured as either transmit or receive except for the last message object. The last message object is a receive-only buffer with a special mask design to allow select groups of different message identifiers to be received.

The 82527 also implements a global masking feature for message filtering. This feature allows the user to globally mask any identifier bits of the incoming message. The programmable global mask can be used for both standard and extended messages.

The 82527 offers hardware, or pinout, compatibility with the 82526. It is pin-to-pin compatible with the 82526 except for pins 9, 30, and 44. These pins are used as chip selects on the 82526 and are used as CPU interface mode selection pins on the 82527.

The 82527 is fabricated using Intel's reliable CHMOS III 5V technology and is available in a 44-lead PLCC for the automotive temperature range (−40°C to +125°C).

NOTICE:

This is a PREVIEW DATA SHEET. The A.C. and D.C. parameters contained within this data sheet may change after full automotive temperature characterization of the device has been performed. Contact your local sales office before finalizing the Timing and D.C. characteristics of a design to verify you have the latest information.

August 1992
Order Number: 272250-001

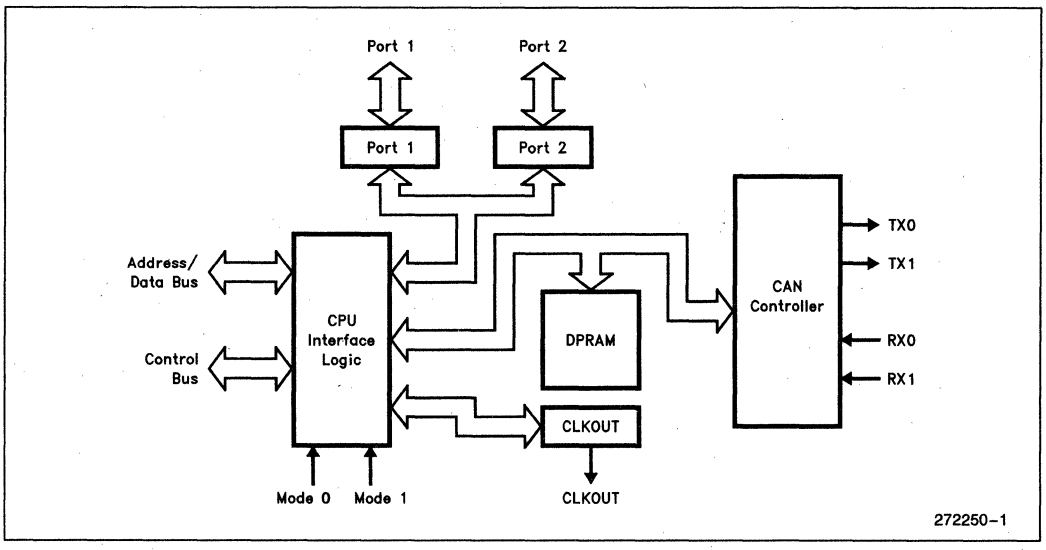

Figure 1. 82527 Block Diagram

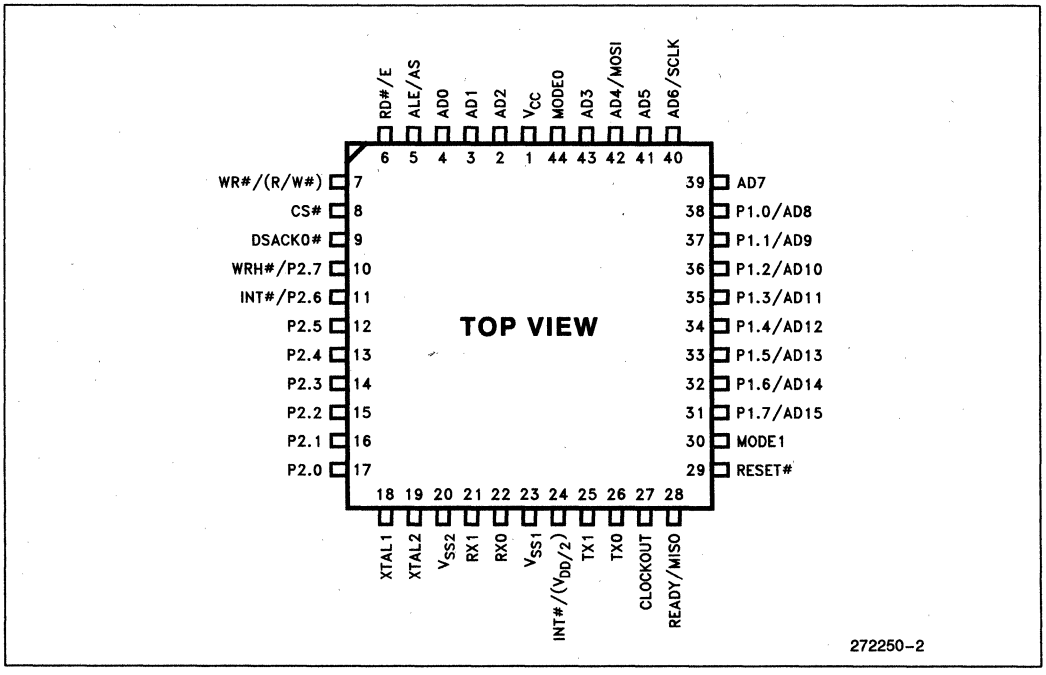

Figure 2. 44-Pin PLCC Package

PIN DESCRIPTION

The 82527 pins are described in this section. Table 1 presents the legend for interpreting the pin types.

Table 1. Pin Type Legend

Symbol	Description
I	Input only pin
O	Output only pin
I/O	Pin can be either input or output

PIN DESCRIPTIONS

Pin #	Pin Name	Pin Type	Pin Description
23	V_{SS1}	Ground	GROUND connection must be shorted externally to a V_{SS} board plane. Provides digital ground.
20	V_{SS2}	Ground	GROUND connection must be shorted externally to a V_{SS} board plane. Provides ground for analog comparator.
1	V_{CC}	Power	POWER connection must be shorted externally to + 5V DC. Provides power for entire device.
18	XTAL1	I	Input for an external clock. XTAL1 (along with XTAL2) are the crystal connections to an internal oscillator.
19	XTAL2	O	Push-pull output from the internal oscillator. XTAL2 (along with XTAL1) are the crystal connections to an internal oscillator. If an external oscillator is used XTAL2 must be floated, or not be connected. XTAL2 must not be used as a clock output to drive other CPUs.
27	CLKOUT	O	Programmable clock output. This output may be used to drive the oscillator of the host microcontroller.
29	RESET#	I	A falling edge (high-to-low) transition causes a hardware reset.
8	CS#	I	A low level on this pin enables CPU access to the 82527 device.
24	INT# (V_{DD}/2)	O O	The interrupt pin is an open-drain output to the host microcontroller. V_{DD}/2 is the power supply for the ISO low speed physical layer. The function of this pin is determined by the MUX bit in the CPU Interface Register (Address 02H) as follows: MUX = 1: pin 24 = V_{DD}/2, pin 11 = INT# MUX = 0: pin 24 = INT#
22 21	RX0 RX1	I I	Inputs from the CAN bus line(s) to the input comparator. A recessive level is read when RX0 > RX1. A dominant level is read when RX1 > RX0. When the CoBy bit (Bus Configuration register) is programmed as a "1", the input comparator is bypassed and RX0 is the CAN bus line input.
26 25	TX0 TX1	O O	Serial data push-pull output to the CAN bus line. During a recessive bit TX0 is high and TX1 is low. During a dominant bit TX0 is low and TX1 is high.

Pin #	Pin Name	Pin Type	Pin Description
4 3 2 43 42 41 40 39	AD0/A0/ICP AD1/A1/CP AD2/A2/CSAS AD3/A3/STE AD4/A4/MOSI AD5/A5 AD6/A6/SCLK AD7/A7	I/O-I-I I/O-I-I I/O-I-I I/O-I I/O-I I/O-I I/O-I-I I/O-I-I	Address/Data bus in 8-bit multiplexed mode. Address bus in 8-bit non-multiplexed mode. Low byte of A/D bus in 16-bit multiplexed mode. In Serial Interface mode pins AD0-3 have the following meaning: AD0: ICP Idle Clock Polarity AD1: CP Clock Phase AD2: CSAS Chip Select Active State AD3: STE Sync Transmit Enable AD6: SCLK Serial Clock Input AD4: MOSI Serial Data Input
38 37 36 35 34 33 32 31	AD8/D0/P1.0 AD9/D1/P1.1 AD10/D2/P1.2 AD11/D3/P1.3 AD12/D4/P1.4 AD13/D5/P1.5 AD14/D6/P1.6 AD15/D7/P1.7	I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O	High byte of A/D bus in 16-bit multiplexed mode. Data bus in 8-bit non-multiplexed mode. Low speed I/O port. P1 pins in 8-bit multiplexed mode and serial mode. Port pins have weak pullups until the port is configured by writing to 9FH and AFH.
17 16 15 14 13 12 11 10	P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6/INT# P2.7/WRH#	I/O I/O I/O I/O I/O I/O I/O-O I/O-I	P2 in all modes. P2.6 is INT# when MUX = 1 and is open-drain. P2.7 is WRH# in 16-bit multiplexed mode.
44 30	Mode0 Mode1	I I	These pins select one of the four parallel interfaces: **Mode1 Mode0** 0 0 8-bit multiplexed — Intel 0 0 Serial Interface mode entered when RD# = 0, WR# = 0 upon reset. 0 1 16-bit multiplexed — Intel 1 0 8-bit multiplexed — non-Intel 1 1 8-bit non-multiplexed **Note:** *When RD# = 0, WR# = 0 serial interface mode is entered.
5	ALE/AS	I-I	ALE used for Intel modes. AS used for non-Intel modes.
6	RD# E	I I	RD# used for Intel modes. E used for non-Intel modes.
7	WR# R/W#	I I	WR# used for Intel modes. R/W# used for non-Intel modes.
28	READY MISO	O O	READY is an output to synchronize accesses from the host microcontroller to the 82527. READY is an open-drain output to the host microcontroller. MISO is the serial data output for the serial interface mode.
9	DSACK0#	O	DSACK0# is an output to synchronize accesses from the host microcontroller to the 82527.

ELECTRICAL CHARACTERISTICS

D.C. Characteristics V_{CC} = 5V ±10%; T_A = −40°C to +125°C

Symbol	Parameter	Min	Max	Conditions
V_{IL}	Input Low Voltage (All except XTAL1, XTAL2, RX0, RX1)	−0.5V	0.8V	
V_{IH}	Input High Voltage (All except XTAL1, XTAL2, RX0, RX1, RESET#)	3.0V	V_{CC} + 0.5V	
V_{IH1}	Input High Voltage (RESET#)	3.0V	V_{CC} + 0.5V	
V_{OL}	Output Low Voltage (All Outputs except TX0, TX1)		0.45V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage (All Outputs except TX0, TX1, CLOCKOUT)	V_{CC} − 0.8V		I_{OH} = −200 μA
V_{OHR1}	Output High Voltage (CLOCKOUT)	0.8 V_{CC}		I_{OH} = −80 μA
I_{LK}	Input Leakage Current		±10 μA	$V_{SS} < V_{IN} < V_{CC}$
C_{IN}	PIN Capacitance*		10 pF	f_{XTAL} = 1 KHz
I_{CC}	Supply Current		100 mA	f_{XTAL} = 16 MHz
I_{SLEEP}	Sleep Current with $V_{DD}/2$ Output Enabled, No Load with $V_{DD}/2$ Output Disabled	 700 μA 100 μA		
I_{PD}	Powerdown Current XTAL1 Driven	10μA		

NOTE:
*Typical value based on characterization data.

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PHYSICAL LAYER SPECIFICATIONS Load Condition: 100 pF

D.C. Characteristics V_{CC} = 5V ±10%; T_A = −40°C to +125°C

RX0/RX1	Min	Max	Conditions
Input Voltage	−0.5V	V_{CC} + 0.5V	
Common Mode Range	V_{SS} + 1V	V_{CC} − 1V	
Delay Dominant to Recessive		35 ns	−100 mV to +100 mV differential
Delay Recessive to Dominant		35 ns	+100 mV to −100 mV differential
Differential Input Threshold		±100 mV	
If the comparator is bypassed by setting the CoBy bit to one in the Bus Configuration Register, the Input Delay is:		10 ns	
TX0/TX1			
Source Current on Each TX0, TX1	−10 mA		V_{OUT} = V_{CC} − 1.0V
Sink Current on Each TX0, TX1	10 mA		V_{OUT} = 1.0V
Rise Time		25 ns	C_{LOAD} = 100 pF
Fall Time		25 ns	C_{LOAD} = 100 pF
V_{DD}/2			
V_{DD}/2	2.38V	2.62V	$I_{OUT} \leq 75\ \mu A$, V_{CC} = 5V

CLOCKOUT SPECIFICATIONS

Load Condition: 50 pF

Parameter	Min	Max
CLOCKOUT Frequency	XTAL/15	XTAL

A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

Symbol	Parameter	Min	Max
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	5 MHz
t_{AVLL}	Address Valid to ALE Low	33 ns	
t_{LLAX}	Address Hold after ALE Low	22.5 ns	
t_{RHDZ}	Data Float after RD# High	0 ns	45 ns
t_{RLDV}	RD# Low to Data Valid (Only for Registers 02H, 04H, 05H)	0 ns	45 ns
t_{RLRH}	RD# Pulse Width This time is long enough to initiate a double read cycle by loading the High Speed Registers (04H, 05H), but is too short to READ from 04H and 05H (See t_{RLDV})	40 ns	
t_{RLYH}	RD# Low to READY High (for registers except 02H, 04H, 05H) for Read Cycle without a Previous Write for Read Cycle with a Previous Write		 $2\ t_{MCLK}$ + 145 ns $4\ t_{MCLK}$ + 145 ns
t_{QVWH}	Data Setup to WR# High	30 ns	
t_{WHQX}	Input Data Hold after WR# High	20 ns	
t_{WHDV}	WR# High to Output Data Valid on Port 1/2	t_{MCLK}	$2\ t_{MCLK}$ + 100 ns
t_{WHLH}	WR# High to Next ALE High	0 ns	
t_{WLWH}	WR# Pulse Width	40 ns	
t_{LHLL}	ALE High Time	30 ns	
t_{CLYV}	CS# Low to READY Setup Condition: Load Capacitance on the READY Output: 50 pF		32 ns
t_{WLYH}	WR# Low to READY High for a Write Cycle if No Previous Write is Pending		145 ns
t_{WHYH}	End of Last Write to READY High for a Write Cycle if a Previous Write Cycle is Active	$3\ t_{MCLK}$ + 145 ns	$4\ t_{MCLK}$ + 145 ns
t_{LLRL}	ALE Low to RD# Low	0 ns	

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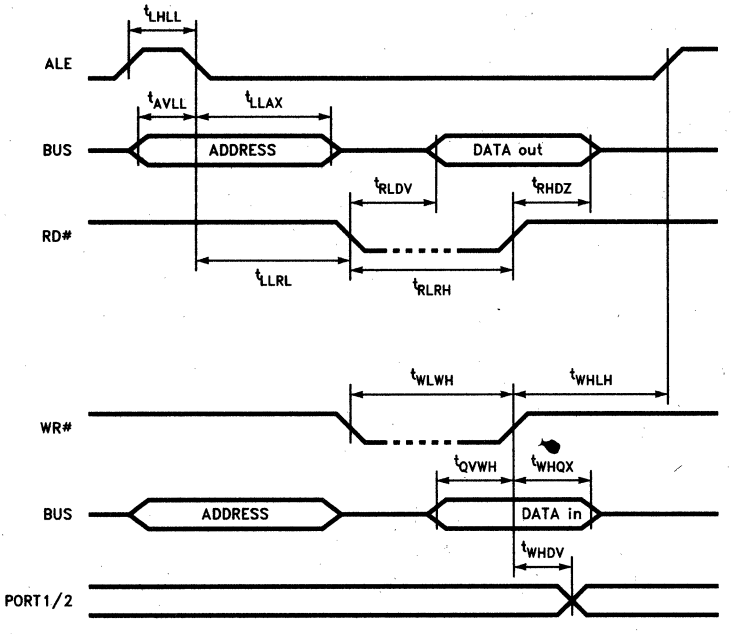
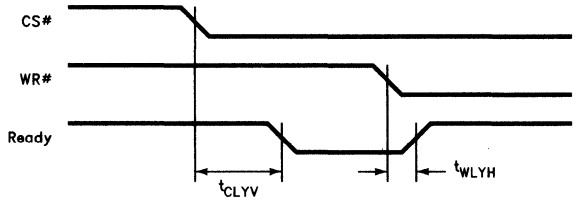
A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)



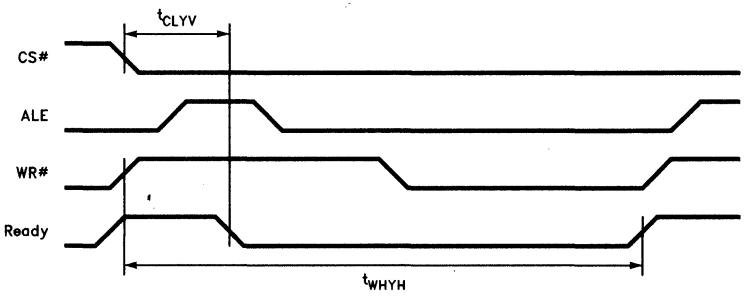
A.C. Characteristics for 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)

Ready Output Timing for a Write Cycle if No Previous Write is Pending



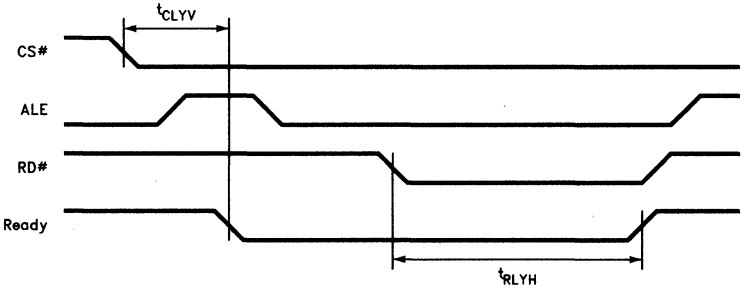
272250-4

Ready Output Timing for a Write Cycle if a Previous Write Cycle is Active



272250-5

Ready Output Timing for a Read Cycle



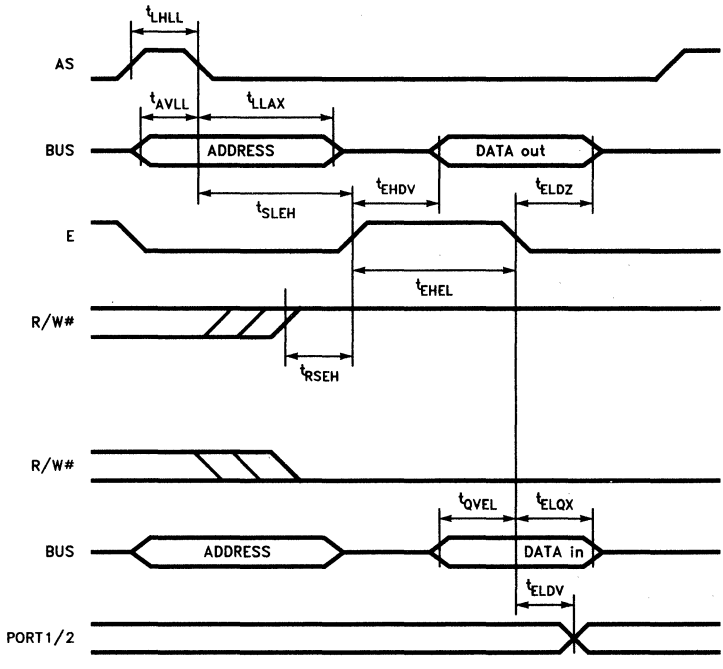
272250-6

A.C. Characteristics for 8-Bit Multiplexed Non-Intel Mode (Mode 2)

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

Symbol	Parameter	Min	Max
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	5 MHz
t_{AVSL}	Address Valid to AS Low	33 ns	
t_{SLAX}	Address Hold after AS Low	22.5 ns	
t_{ELDZ}	Data Float after E Low	0 ns	45 ns
t_{EHDV}	E High to Data Valid	0 ns	45 ns
	for Read Cycle without a Previous Write for Ready Cycle with a Previous Write (for Registers except for 02H, 04H, 05H)		$2\ t_{MCLK} + 145$ ns $4\ t_{MCLK} + 145$ ns
t_{QVEL}	Data Setup to E Low	30 ns	
t_{ELQX}	Input Data Hold after E Low	20 ns	
t_{ELDV}	E Low to Output Data Valid on Port 1/2	$t_{MCLK} + 100$ ns	$2\ t_{MCLK} + 100$ ns
t_{EHEL}	E High Time (only for Registers 02H, 04H, 05H)	45 ns	
	for Write Cycle with Previous Write (for Registers except for 02H, 04H, 05H)	$4\ t_{MCLK} + 145$ ns	
t_{SHSL}	AS High Time	30 ns	
t_{RSEH}	Setup Time of R/W# to E High	30 ns	
t_{SLEH}	AS Low to E High	0 ns	

A.C. Characteristics for 8-Bit Multiplexed Non-Intel Mode (Mode 2) (Continued)



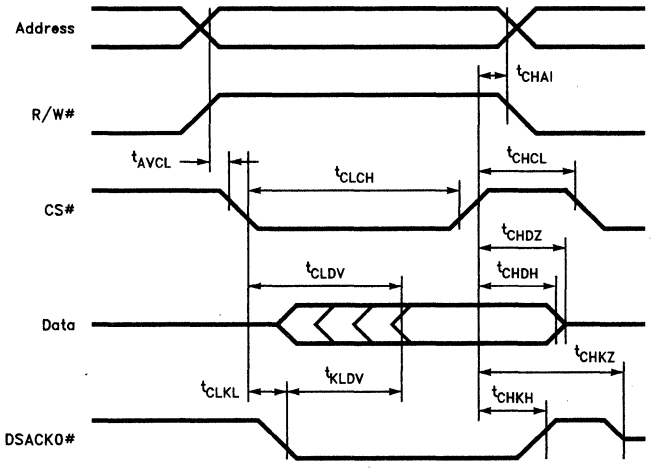
A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous (Mode 3)

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

Symbol	Parameter	Min	Max
$1/t_{XTAL}$	Osciliator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	5 MHz
t_{AVCL}	Address or R/W# Valid to CS# Low Setup	3 ns	
t_{CLDV}	CS# Low to Data Valid for High Speed Registers (02H, 04H, 05H)	0 ns	65 ns
	For Low Speed Registers (Read Cycle without Previous Write)	0 ns	2 t_{MCLK} + 145 ns
	For Low Speed Registers (Read Cycle with Previous Write)	0 ns	4 t_{MCLK} + 145 ns
t_{KLDV}	DSACK0# Low to Output Data Valid	<0 ns	23 ns
t_{CHDV}	82527 Input Data Hold after CS# High	25 ns	
t_{CHDH}	82527 Output Data Hold after CS# High	0 ns	
t_{CHDZ}	CS# High to Output Data Float	0 ns	35 ns
t_{CHKH}	CS# High to DSACK0# = V_{IH} (with 3.3 KΩ Pullup and 100 pF Load)	0 ns	55 ns
t_{CHKZ}	CS# High to DSACK0# Float	0 ns	100 ns
t_{CHCL}	CS# Width between Successive Cycles	25 ns	
t_{CHAI}	CS# High to Address or R/W# Invalid	5 ns	
t_{CLCH}	CS# Width Low	65 ns	
t_{DVCH}	CPU Write Data Valid to CS# High	32 ns	
t_{CLKL}	CS# Low to DSACK0# Low for High Speed Registers and Low Speed Registers Write Access without Previous Write	0 ns	65 ns
	for Write Access with a Previous Write	0 ns	2 t_{MCLK} + 145 ns

A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous (Mode 3) (Continued)

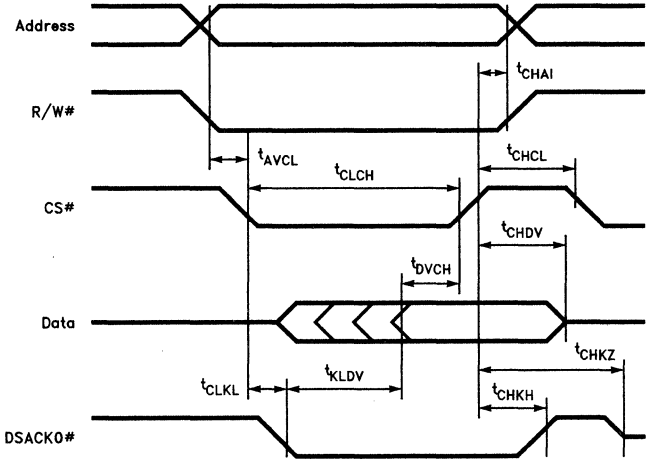
Timing of the Asynchronous Mode (Read Cycle)



272250-10

A.C. Characteristics for 8-Bit Non-Multiplexed Asynchronous (Mode 3)

Timing of the Asynchronous Mode (Write Cycle)



272250-11

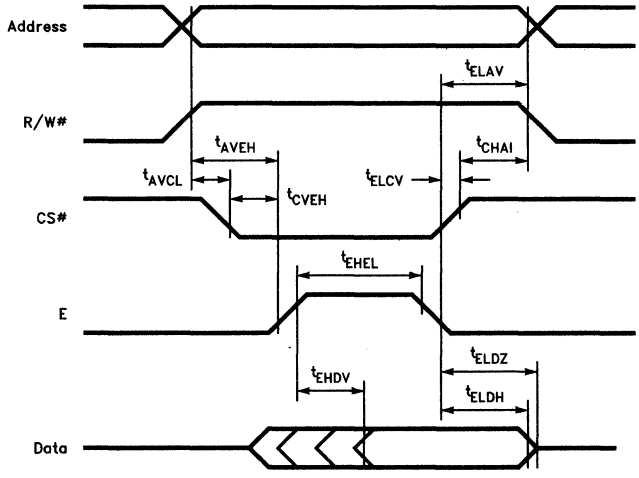
A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

Symbol	Parameter	Min	Max
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	5 MHz
t_{EHDV}	E High to Data Valid out of High Speed Register (02H, 04H, 05H)		65 ns
	Read Cycle without Previous Write for Low Speed Registers		$2\ t_{MCLK}$ + 145 ns
	Read Cycle with Previous Write for Low Speed Registers		$4\ t_{MCLK}$ + 145 ns
t_{ELDH}	Data Hold after E Low for a Read Cycle	5 ns	
t_{ELDZ}	Data Float after E Low	0 ns	35 ns
t_{ELDV}	Data Hold after E Low for a Write Cycle	25 ns	
t_{AVEH}	Address and R/W# to E Setup	25 ns	
t_{ELAV}	Address and R/W# Valid after E Falls	15 ns	
t_{CVEH}	CS# Valid to E High	0 ns	
t_{ELCV}	CS# Valid after E Low	0 ns	
t_{DVEL}	Data Setup to E Low	55 ns	
t_{EHEL}	E Active Width	100 ns	
t_{AVAL}	Start of a Write Cycle after a Previous Write Access	$2\ t_{MCLK}$	

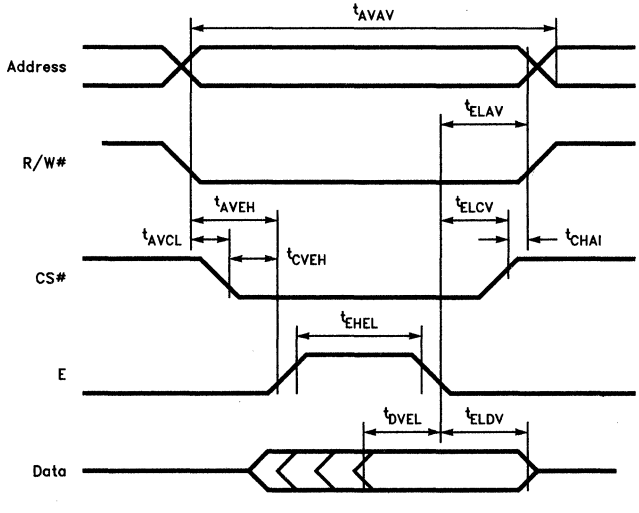
A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)

Timing of the Synchronous Mode (Read Cycle)



A.C. Characteristics for 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)

Timing of the Synchronous Mode (Write Cycle)

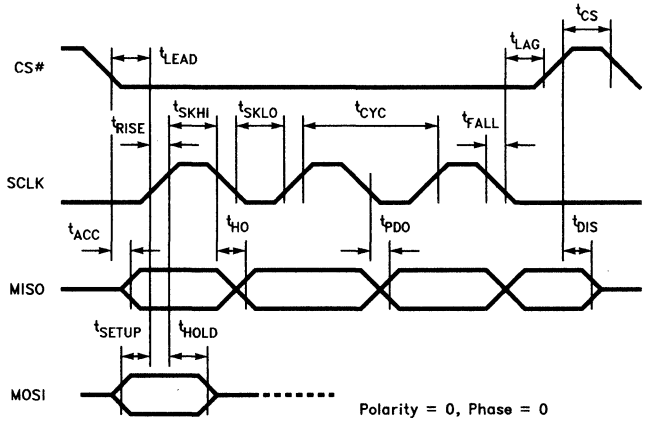


A.C. Characteristics for Serial Interface Mode

Conditions: V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = −40°C to +125°C, C_L = 100 pF

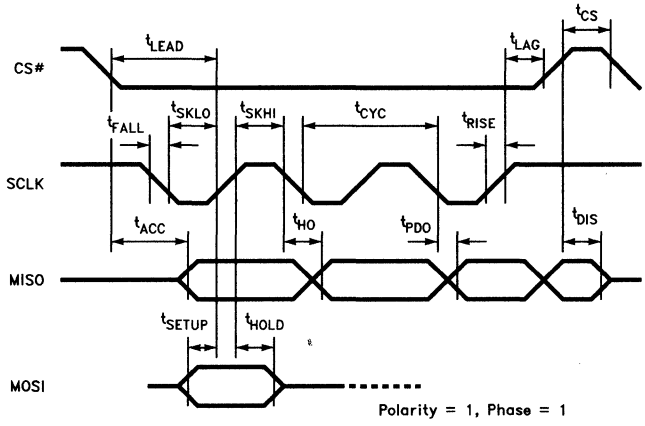
Symbol	Parameter	Min	Max
SCLK	SPI Clock	0.5 MHz	4.2 MHz
t_{CYC}	1/SCLK	238 ns	2000 ns
t_{SKHI}	Minimum Clock High Time	119 ns	
t_{SKLO}	Minimum Clock Low Time	119 ns	
t_{LEAD}	ENABLE Lead Time	70 ns	
t_{LAG}	Enable Lag Time	109 ns	
t_{ACC}	Access Time		60 ns
t_{PDO}	Maximum Data Out Delay Time		84 ns
t_{HO}	Minimum Data Out Hold Time	0 ns	
t_{DIS}	Maximum Data Out Disable Time		665 ns
t_{SETUP}	Minimum Data Setup Time	59 ns	
t_{HOLD}	Minimum Data Hold Time	109 ns	
t_{RISE}	Maximum Time for Input to go from V_{OL} to V_{OH}		100 ns
t_{FALL}	Maximum Time for Input to go from V_{OH} to V_{OL}		100 ns
t_{CS}	Minimum Time between Consecutive CS# Assertions	670 ns	

A.C. Characteristics for Serial Interface Mode



Polarity = 0, Phase = 0

272250-12

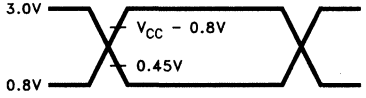


Polarity = 1, Phase = 1

272250-13

A.C. TESTING INPUT

Input, Output Waveforms



272250-14

NOTE:
AC Inputs during testing are driven at V_{CC} − 0.5V for a Logic "1" and 0.1V for a Logic "0". Timing measurements are made at V_{IH} Min for a Logic "1" and V_{OL} Max for a Logic "0".

CAN 82527 Development Tool

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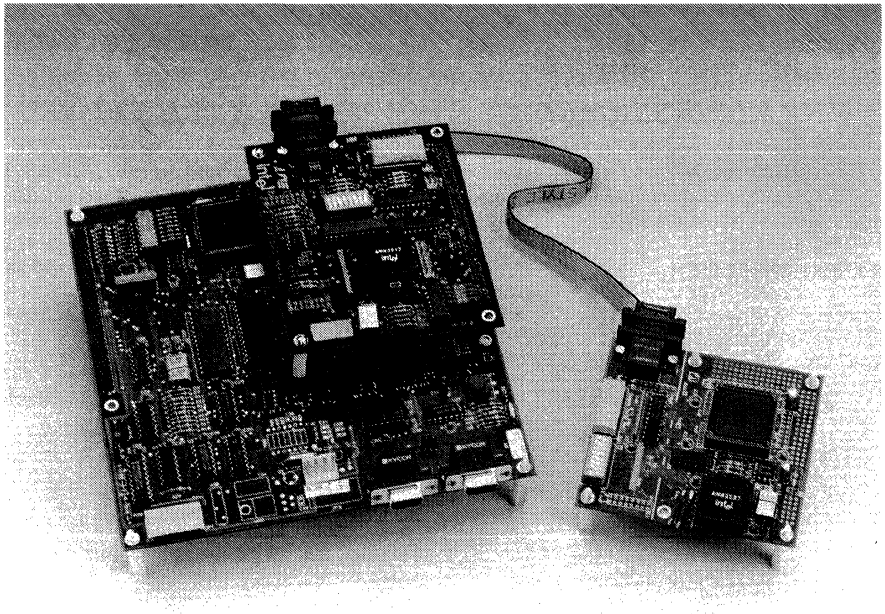
EV82527 EVALUATION KIT



272263-01

The EV82527 evaluation kit demonstrates the capabilities of the 82527 serial communications controller and the Controller Area Network (CAN) protocol. This evaluation kit represents a quick approach to learning the features of the 82527 device and CAN Specification 2.0 29-bit message identifiers.

DESCRIPTION

The EV82527 evaluation kit features the 82527 device and the CAN protocol, Specification 2.0. The 82527 device implements CAN Specification 2.0 and is optimized to allow the host microcontroller to remain dedicated to its application control function. The host microcontroller interface to the 82527 is analogous to that of a RAM. The transmission, reception and error confinement routines are hardwired in the 82527 and are transparent to the user.

FEATURES

The EV82527 evaluation kit consists of three boards: an EV87C196KR motherboard, an 82527 daughterboard and a DV82527 satellite board, plus a software monitor that assembles MCS®-96 code online.

- The motherboard is a fully functional evaluation board which contains the host microcontroller, the Intel 87C196KR.
- The daughterboard is configured with an RS-485 CAN bus interface and can be easily adapted to other physical layer implementations.
- The daughterboard communicates with a DV82527 satellite board acting as an additional network node. The satellite board requires no host-CPU programming and uses dip switches to choose various communication options.

BENEFITS

- Quick setup and installation
- Interfaces to high performance 16-bit host-CPU

October 1992
Order Number: 272263-001

intel

EV82527 EVALUATION KIT

- Assists the development of CAN application software
- Demonstrates CAN Specification 2.0 protocol and features
- Uses standard Personal Computer host

87C196KR MOTHERBOARD

Assembly language programs for the 87C196KR motherboard may be downloaded to the microcontroller and executed. The monitor program has the following features:

- Program loading
- Program disassembly
- In-monitor assembler that allows program to be written on-line
- 16 breakpoints
- Single-stepping
- Specific commands to interrogate 82527 messages and status

The 87C916KR is a powerful 16-bit microcontroller with high speed I/O, an A/D converter, full duplex serial I/O (synchronous and asynchronous), 768 bytes of RAM and 16 Kbytes of EPROM.

82527 DAUGHTERBOARD

The interface between the 82527 CAN device and the 87C196KR microcontroller is completed by connecting the mother and daughterboards together. The 82527 device interfaces to the 87C196KR using either an 8- or 16-bit multiplexed address/data bus.

CAN bus communication utilizes the on-board RS-485 interface or connects to a user defined physical interface.

The two 8-bit I/O ports of the 82527 device connect to dip switches or LED displays allowing the user to change or monitor the operation of the 82527 and the 87C196KR devices.

DV82527 SATELLITE BOARD

The daughterboard connects to a satellite board via a cable serving as the CAN bus. It executes a series of fixed programs which are user-selected dip switches. The satellite board receives and transmits one-byte messages of either 11- or 29-bit message identifier format. Messages may use one of four possible message identifiers. The satellite sends remote frames as well.

The reception and transmission of satellite board messages is monitored on LED displays.

PERSONAL COMPUTER REQUIREMENTS

The EV82527 evaluation kit is hosted on an IBM PC AT, XT or BIOS-compatible clone. The PC must meet the following requirements:

- 512 Kbytes of memory
- One 1.2 Meg floppy Disk Drive
- MS-DOS 3.0 or later
- A serial (COM1 or COM2) at 9600 baud
- ASM-96, iC-96 or PL/M-96 or any 8096 Assembler/Compiler that generates Object Module Format code
- A text editor such as AEDIT

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