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Chip Sets

82430LX/82430NX PCIset

- Supports the Pentium™ Processor at 60 and 66 MHz (82430LX)
- Supports the Pentium Processor at iCOMP™ Index 735\90 MHz, Pentium Processor at iCOMP Index 815\100 MHz, and Pentium Processor at iCOMP Index 610\75 MHz
- Supports Uni-Processor (UP) or Dual-Processor (DP) Configurations
- Interfaces the Host and Standard Buses to the PCI Local Bus
  - Up to 132 MBytes/Sec Transfer Rate
  - Full Concurrency Between CPU Host Bus and PCI Bus Transactions
- Integrated Cache Controller Provided for Optional Second Level Cache
  - 256 KByte or 512 KByte Cache
  - Write-Back or Write-Through Policy (82430LX)
  - Write-Back Policy (82430NX)
  - Standard or Burst SRAM
- Integrated Tag RAM for Cost Savings on Second Level Cache
- Supports the Pipelined Address Mode of the Pentium Processor for Higher Performance
- Provides a 64-Bit Interface to DRAM Memory
  - From 2 MBytes to 512 MBytes of Main Memory
  - 70 ns and 60 ns DRAMs Supported
- Optional ISA or EISA Standard Bus Interface
  - Single Component ISA Controller
  - Two Component EISA Bus Interface
  - Minimal External Logic Required
- Supports Burst Read and Writes of Memory from the CPU and PCI Buses
- Five Integrated Write Posting and Read Prefetch Buffers Increase CPU and PCI Performance
- Host CPU Writes to PCI Converted to Zero Wait-State PCI Bursts with Optional TRDY# Connection
- Integrated Low Skew Host Bus Clock Driver for Cost and Board Space Savings
- PCIset Operates Synchronous to the CPU and PCI Clocks
- Byte Parity Support for the Host and Main Memory Buses
  - Optional Parity on the Second Level Cache

The 82430LX/82430NX PCIsets provide the Host/PCI bridge, cache/main memory controller, and an I/O subsystem core (either PCI/EISA or PCI/ISA bridge) for the next generation of high-performance personal computers based on the Pentium processor. System designers can take advantage of the power of the PCI Local bus for the local I/O while maintaining access to the large base of EISA and ISA expansion cards, and corresponding software applications. Extensive buffering and buffer management within the bridges ensures maximum efficiency in all three bus environments (Host CPU, PCI, and EISA/ISA Buses).

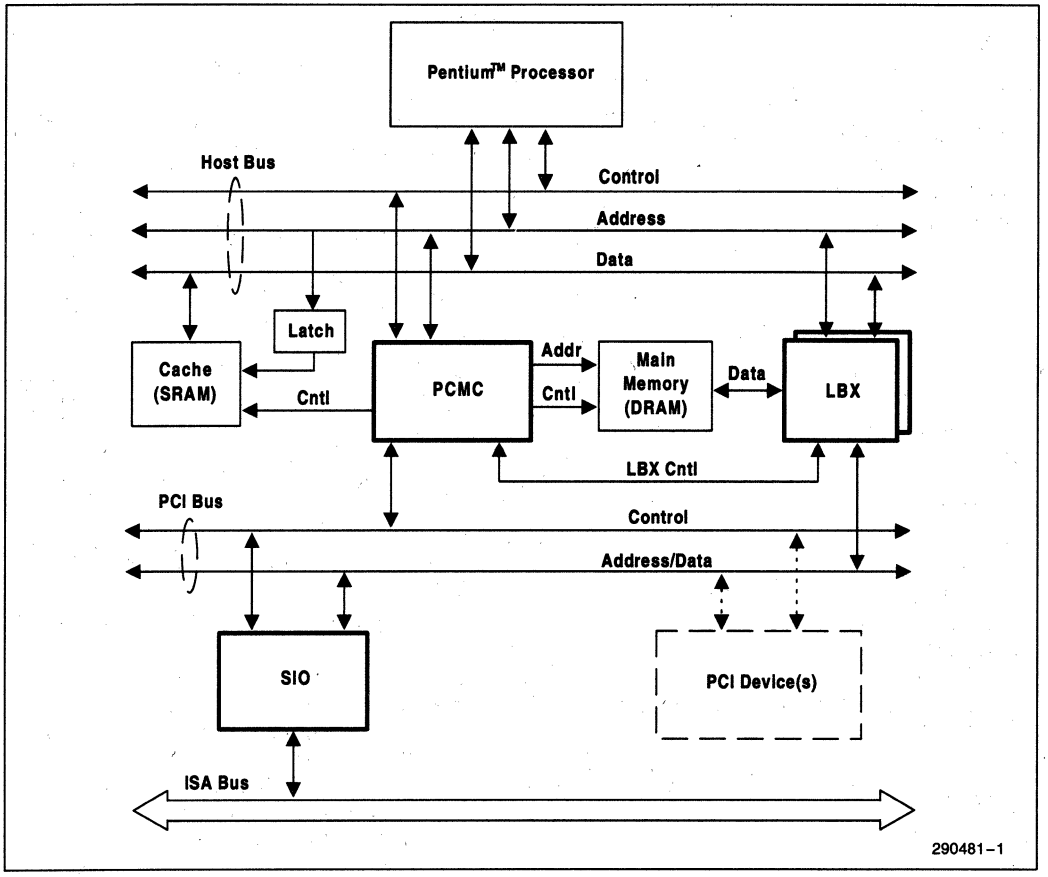
The 82430LX PCIset consists of the 82434LX PCI/Cache Memory Controller (PCMC) and the 82433LX Local Bus Accelerator (LBX) components, plus, either a PCI/ISA bridge or a PCI/EISA bridge. The PCMC and LBX provide the core cache and main memory architecture and serve as the Host/PCI bridge. For an ISA-based system, the 82430LX PCIset includes the 82378ZB System I/O (SIO) component as the PCI/ISA bridge. For an EISA-based system, the 82430LX PCIset includes the 82375EB/SB PCI/EISA Bridge (PCEB) and the 82374EB/SB EISA System Component (ESC). The PCEB and ESC work in tandem to form the complete PCI/EISA bridge. Both the ISA and EISA-based systems are shown on the following pages.

The 82430NX PCIset consists of the 82434NX PCI/Cache Memory Controller (PCMC) and the 82433NX Local Bus Accelerator (LBX) components, plus, either a PCI/ISA bridge or a PCI/EISA bridge. For an ISA-based system, the 82430NX PCIset includes the 82378ZB System I/O (SIO) component as the PCI/ISA bridge. For the DP ISA based system, the 82430NX PCIset includes the 82379AB. For UP or DP EISA-based systems, the 82430NX PCIset includes the 82375EB/SB PCI/EISA Bridge (PCEB) and the 82374EB/SB EISA System Component (ESC).

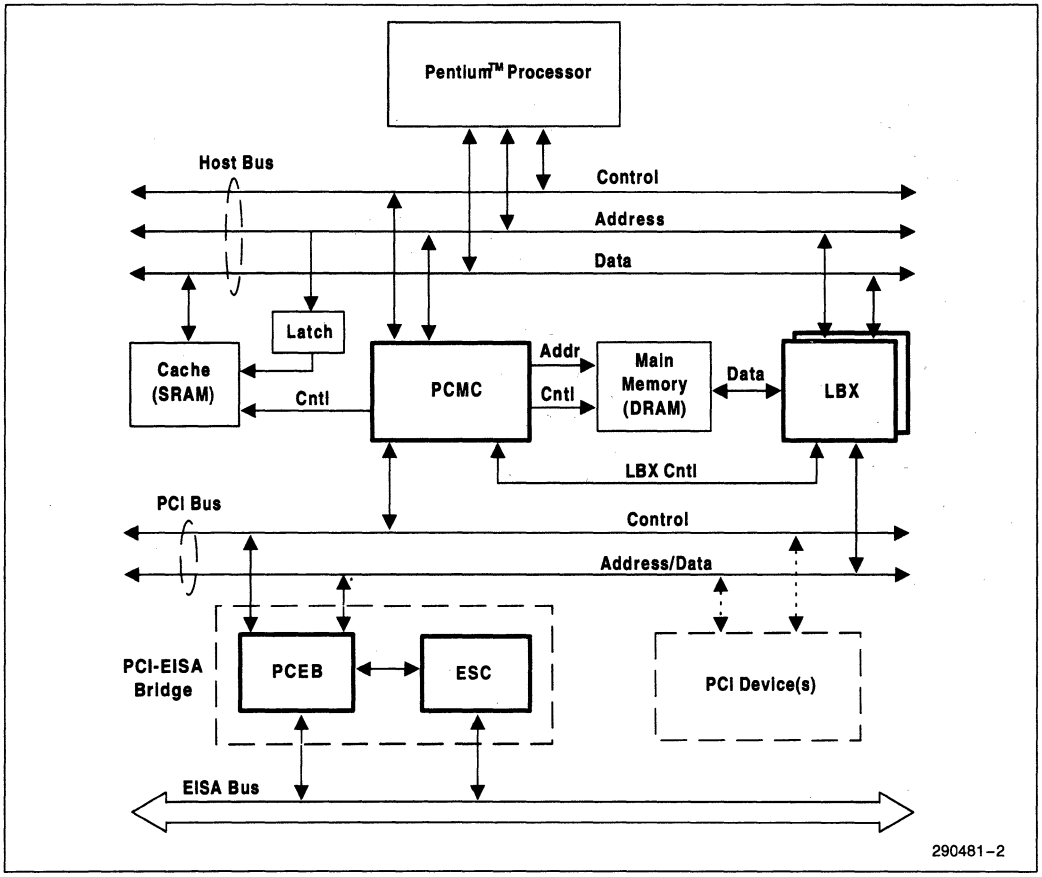
This document describes both the 82430LX and 82430NX. Unshaded areas describe the 82434LX. Shaded areas, like this one, describe 82430NX operations that differ from the 82434LX.

The complete documents for these products can be ordered by calling 1-800-548-4725. Refer to 290482 (Cache/Memory Subsystem) and 290483 (EISA Bridge).

November 1994
Order Number: 290481-005



82430LX or 82430NX PCIset ISA Block Diagram



82430LX or Uni-Processor 82430NX PCIset EISA Block Diagram

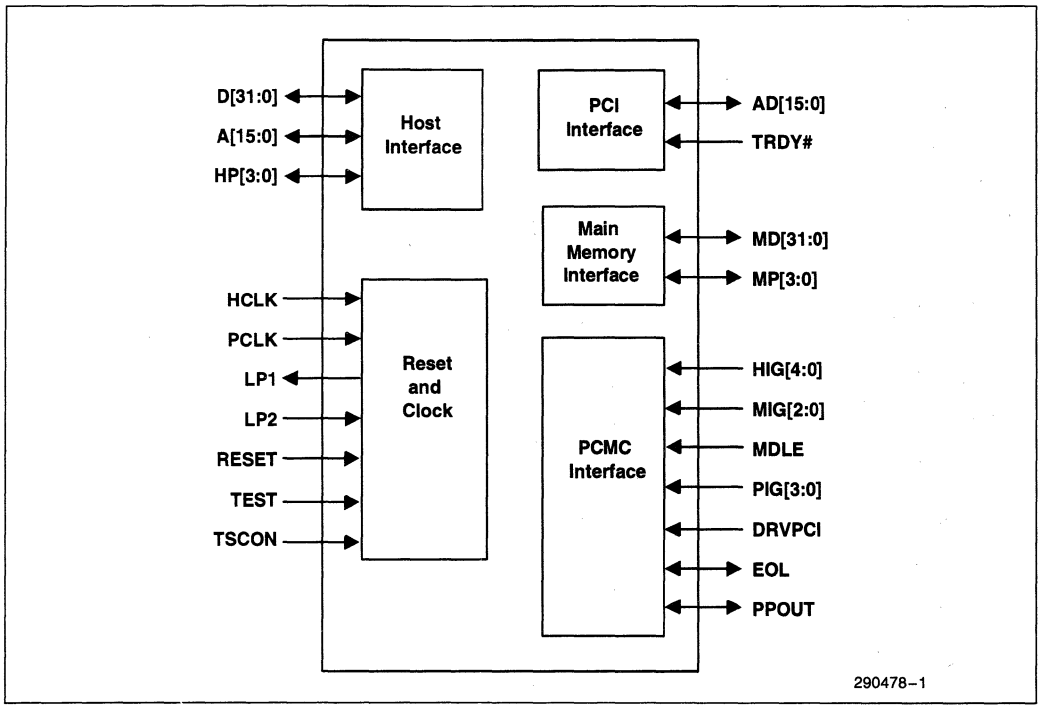
82433LX/82433NX
LOCAL BUS ACCELERATOR (LBX)

- Supports the Full 64-bit Pentium™ Processor Data Bus at Frequencies up to 66 MHz (82433LX and 82433NX)
- Drives 3.3V Signal Levels on the CPU Data and Address Buses (82433NX)
- Provides a 64-Bit Interface to DRAM and a 32-Bit Interface to PCI
- Five Integrated Write Posting and Read Prefetch Buffers Increase CPU and PCI Performance
  - — CPU-to-Memory Posted Write Buffer 4 Qwords Deep
  - — PCI-to-Memory Posted Write Buffer Two Buffers, 4 Dwords Each
  - — PCI-to-Memory Read Prefetch Buffer 4 Qwords Deep
  - — CPU-to-PCI Posted Write Buffer 4 Dwords Deep
  - — CPU-to-PCI Read Prefetch Buffer 4 Dwords Deep
- CPU-to-Memory and CPU-to-PCI Write Posting Buffers Accelerate Write Performance
- Dual-Port Architecture Allows Concurrent Operations on the Host and PCI Buses
- Operates Synchronously to the CPU and PCI Clocks
- Supports Burst Read and Writes of Memory from the Host and PCI Buses
- Sequential CPU Writes to PCI Converted to Zero Wait-State PCI Bursts with Optional TRDY# Connection
- Byte Parity Support for the Host and Memory Buses
  - — Optional Parity Generation for Host to Memory Transfers
  - — Optional Parity Checking for the Secondary Cache
  - — Parity Checking for Host and PCI Memory Reads
  - — Parity Generation for PCI to Memory Writes
- 160-Pin QFP Package

Two 82433LX or 82433NX Local Bus Accelerator (LBX) components provide a 64-bit data path between the host CPU/Cache and main memory, a 32-bit data path between the host CPU bus and PCI Local Bus, and a 32-bit data path between the PCI Local Bus and main memory. The dual-port architecture allows concurrent operations on the host and PCI Buses. The LBXs incorporate three write posting buffers and two read prefetch buffers to increase CPU and PCI performance. The LBX supports byte parity for the host and main memory buses. The 82433NX is intended to be used with the 82434NX PCI/Cache/Memory Controller (PCMC). The 82433LX is intended to be used with the 82434LX PCMC. During bus operations between the host, main memory and PCI, the PCMC commands the LBXs to perform functions such as latching address and data, merging data, and enabling output buffers. Together, these three components form a "Host Bridge" that provides a full function dual-port data path interface, linking the host CPU and PCI bus to main memory.

This document describes both the 82433LX and 82433NX. Shaded areas, like this one, describe the 82433NX operations that differ from the 82433LX.

December 1994
Order Number: 290478-004



LBX Simplified Block Diagram

82433LX/82433NX
LOCAL BUS ACCELERATOR (LBX)

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1.0 ARCHITECTURAL OVERVIEW

The 82430 PCIset consists of the 82434LX PCMC and 82433LX LBX components plus either a PCI/ISA bridge or a PCI/EISA bridge. The 82430NX PCIset consists of the 82434NX PCMC and 82433NX LBX components plus either a PCI/ISA bridge or a PCI/EISA bridge. The PCMC and LBX provide the core cache and main memory architecture and serves as the Host/PCI bridge. An overview of the PCMC follows the system overview section.

The Local Bus Accelerator (LBX) provides a high performance data and address path for the 82430LX/82430NX PCIset. The LBX incorporates five integrated buffers to increase the performance of the Pentium processor and PCI master devices. Two LBXs in the system support the following areas:

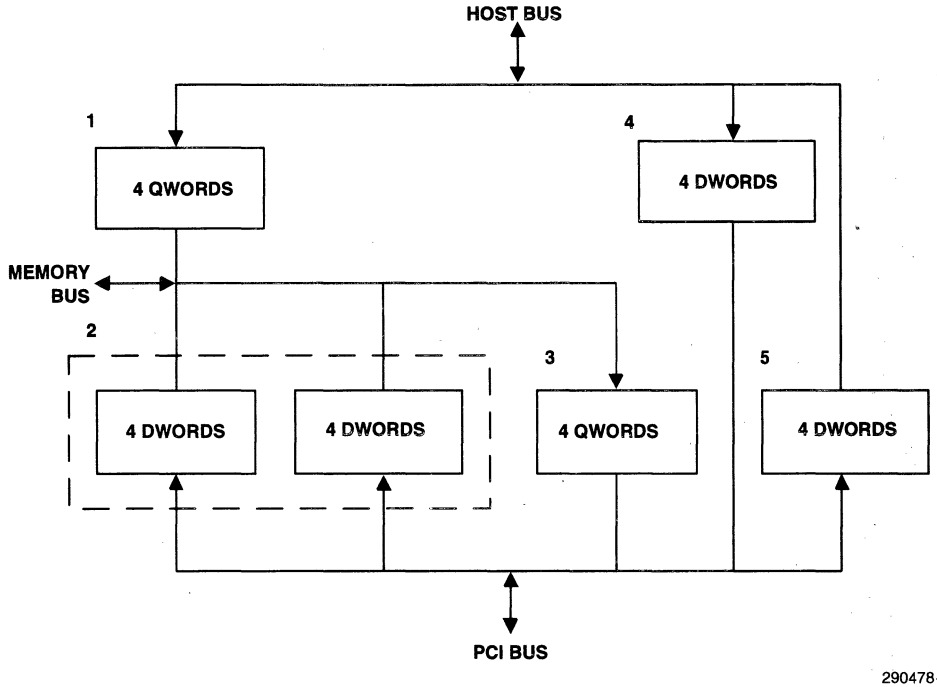
1. 64-bit data and 32-bit address bus of the Pentium processor.
2. 32-bit multiplexed address/data bus of PCI.
3. 64-bit data bus of the main memory.

In addition, the LBXs provide parity support for the three areas noted above (discussed further in Section 1.4).

1.1 Buffers in the LBX

The LBX components have five integrated buffers designed to increase the performance of the Host and PCI Interfaces of the 82430LX/82430NX PCIset.

With the exception of the PCI-to-Memory write buffer and the CPU-to-PCI write buffer, the buffers in the LBX store data only, addresses are stored in the PCMC component.



NOTES:

1. **CPU-to-Memory Posted Write Buffer:** This buffer is 4 Qwords deep, enabling the Pentium processor to write back a whole cache line in 4-1-1-1 timing, a total of 7 CPU clocks.
2. **PCI-to-Memory Posted Write Buffer:** A PCI master can post two consecutive sets of 4 Dwords (total of one cache line) or two single non-consecutive transactions.
3. **PCI-to-Memory Read Prefetch Buffer:** A PCI master to memory read transaction will cause this prefetch buffer to read up to 4 Qwords of data from memory, allowing up to 8 Dwords to be read onto PCI in a single burst transaction.
4. **CPU-to-PCI Posted Write Buffer:** The Pentium processor can post up to 4 Dwords into this buffer. The TRDY# connect option allows zero-wait state burst writes to PCI, making this buffer especially useful for graphic write operations.
5. **CPU-to-PCI Read Prefetch Buffer:** This prefetch buffer is 4 Dwords deep, enabling faster sequential Pentium processor reads when targeting PCI.

Figure 1. Simplified Block Diagram of the LBX Data Buffers

1.2 Control Interface Groups

The LBX is controlled by the PCMC via the control interface group signals. There are three interface groups: Host, Memory, and PCI. These control groups are signal lines that carry binary codes which the LBX internally decodes in order to implement specific functions such as latching data and steering data from PCI to memory. The control interfaces are described below.

1. **Host Interface Group:** These control signals are named HIG[4:0] and define a total of 29 (30 for the 82433NX) discrete commands. The PCMC sends HIG commands to direct the LBX to perform functions related to buffering and storing host data and/or address.
2. **Memory Interface Group:** These control signals are named MIG[2:0] and define a total of 7 discrete commands. The PCMC sends MIG commands to direct the LBX to perform functions related to buffering, storing, and retiring data to memory.
3. **PCI Interface Group:** These control signals are named PIG[3:0] and define a total of 15 discrete commands. The PCMC sends PIG commands to direct the LBX to perform functions related to buffering and storing PCI data and/or address.

1.3 System Bus Interconnect

The architecture of the 82430/82430NX PCIset splits the 64-bit memory and host data buses into logical halves in order to manufacture LBX devices with manageable pin counts. The two LBXs interface to the 32-bit PCI AD[31:0] bus with 16 bits each. Each LBX connects to 16 bits of the AD[31:0] bus and 32-bits of both the MD[0:63] bus and the D[0:63] bus. The lower order LBX (LBXL) connects to the low word of the AD[31:0] bus, while the high order LBX (LBXH) connects to the high word of the AD[31:0] bus.

Since the PCI connection for each LBX falls on 16-bit boundaries, each LBX does not simply connect to either the low Dword or high Dword of the Qword memory and host buses. Instead, the low order LBX buffers the first and third words of each 64-bit bus while the high order LBX buffers the second and fourth words of the memory and host buses.

As shown in Figure 2, LBXL connects to the first and third words of the 64-bit main memory and host data buses. The same device also drives the first 16 bits of the host address bus, A[15:0]. The LBXH device connects to the second and fourth words of the 64-bit main memory and host data buses. Correspondingly, LBXH drives the remaining 16 bits of the host address bus, A[31:16].

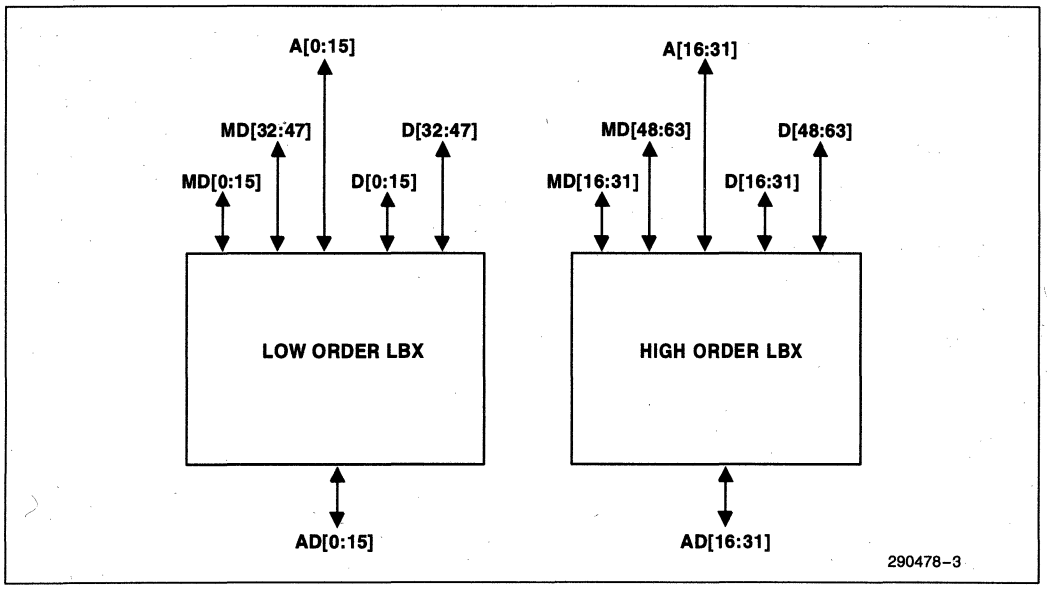


Figure 2. Simplified Interconnect Diagram of LBXs to System Buses

1.4 PCI TRDY# Interface

The PCI control signals do not interface to the LBXs, instead these signals connect to the 82434LX PCMC component. The main function of the LBXs PCI interface is to drive address and data onto PCI when the CPU targets PCI and to latch address and data when a PCI master targets main memory.

The TRDY# option provides the capability for zero-wait state performance on PCI when the Pentium processor performs sequential writes to PCI. This option requires that PCI TRDY# be connected to each LBX, for a total of two additional connections in the system. These two TRDY# connections are in addition to the single TRDY# connection that the PCMC requires.

1.5 Parity Support

The LBXs support byte parity on the host bus (CPU and second level cache) and main memory buses (local DRAM). The LBXs support parity during the address and data phases of PCI transactions to/from the host bridge.

2.0 SIGNAL DESCRIPTIONS

This section provides a detailed description of each signal. The signals (Figure 3) are arranged in functional groups according to their associated interface.

The '#' symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When '#' is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used extensively. This is done to avoid confusion when working with a mixture of 'active-low' and 'active-high' signals. The term **assert**, or **assertion** indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term **negate**, or **negation** indicates that a signal is inactive.

The following notations are used to describe the signal type.

in Input is a standard input-only signal.

out Totem Pole output is a standard active driver.

t/s Tri-State is a bi-directional, tri-state input/output pin.

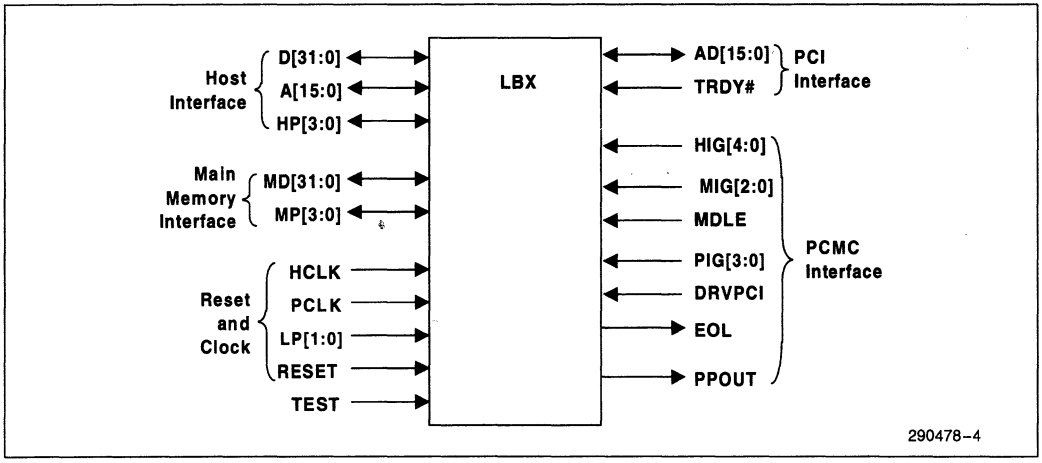


Figure 3. LBX Signals

2.1 Host Interface Signals

Signal	Type	Description
A[15:0]	t/s	**ADDRESS BUS:** The bi-directional A[15:0] lines are connected to the address lines of the host bus. The high order LBX (determined at reset time using the EOL signal) is connected to A[31:16], and the low order LBX is connected to A[15:0]. The host address bus is common with the Pentium processor, second level cache, PCMC and the two LBXs. During CPU cycles A[31:3] are driven by the CPU and A[2:0] are driven by the PCMC, all are inputs to the LBXs. During inquire cycles the LBX drives the PCI master address onto the host address lines A[31:0]. This snoop address is driven to the CPU and the PCMC by the LBXs to snoop L1 and the integrated second level tags, respectively. During PCI configuration cycles bound for the PCMC, the LBXs will send or receive the configuration data to/from the PCMC by copying the host data bus to/from the host address bus. The LBX drives both halves of the Qword host data bus with data from the 32-bit address during PCMC configuration read cycles. The LBX drives the 32-bit address with either the low Dword or the high Dword during PCMC configuration write cycles. In the 82433NX, these pins contain weak internal pull-down resistors. The high order 82433NX LBX samples A11 at the falling edge of reset to configure the LBX for PLL test mode. When A11 is sampled low, the LBX is in normal operating mode. When A11 is sampled high, the LBX drives the internal HCLK from the PLL on the EOL pin. Note that A11 on the high order LBX is connected to the A27 line on the CPU address bus. This same address line is used to put the PCMC into PLL test mode.
D[31:0]	t/s	**HOST DATA:** The bi-directional D[31:0] lines are connected to the data lines of the host data bus. The high order LBX (determined at reset time using the EOL signal) is connected to the host data bus D[63:48] and D[31:16] lines, and the low order LBX is connected to the host data bus D[47:32] and D[15:0] lines. In the 82433LX, these pins contain weak internal pull-up resistors. In the 82433NX, these pins contain weak internal pull-down resistors.
HP[3:0]	t/s	**HOST DATA PARITY:** HP[3:0] are the bi-directional byte parity signals for the host data bus. The low order parity bit HP[0] corresponds to D[7:0] while the high order parity bit HP[3] corresponds to D[31:24]. The HP[3:0] signals function as parity inputs during write cycles and as parity outputs during read cycles. Even parity is supported and the HP[3:0] signals follow the same timings as D[31:0]. In the 82433LX, these pins contain weak internal pull-up resistors. In the 82433NX, these pins contain weak internal pull-down resistors.

2.2 Main Memory (Dram) Interface Signals

Signal	Type	Description
MD[31:0]	t/s	**MEMORY DATA BUS:** MD[31:0] are the bi-directional data lines for the memory data bus. The high order LBX (determined at reset time using the EOL signal) is connected to the memory data bus MD[63:48] and MD[31:16] lines, and the low order LBX is connected to the memory data bus MD[47:32] and MD[15:0] lines. The MD[31:0] signals drive data destined for either the host data bus or the PCI bus. The MD[31:0] signals input data that originated from either the host data bus or the PCI bus. These pins contain weak internal pull-up resistors.
MP[3:0]	t/s	**MEMORY PARITY:** MP[3:0] are the bi-directional byte enable parity signals for the memory data bus. The low order parity bit MP[0] corresponds to MD[7:0] while the high order parity bit MP[3] corresponds to MD[31:24]. The MP[3:0] signals are parity outputs during write cycles to memory and parity inputs during read cycles from memory. Even parity is supported and the MP[3:0] signals follow the same timings as MD[31:0]. These pins contain weak internal pull-up resistors.

2.3 PCI Interface Signals

Signal	Type	Description
AD[15:0]	t/s	**ADDRESS AND DATA:** AD[15:0] are bi-directional data lines for the PCI bus. The AD[15:0] signals sample or drive the address and data on the PCI bus. The high order LBX (determined at reset time using the EOL signal) is connected to the PCI bus AD[31:16] lines, and the low order LBX is connected to the PCI AD[15:0] lines.
TRDY#	in	**TARGET READY:** TRDY# indicates the selected (targeted) device's ability to complete the current data phase of the bus operation. For normal operation, TRDY# is tied asserted low. When the TRDY# option is enabled in the PCMC (for zero wait-state PCI burst writes), TRDY# should be connected to the PCI bus.

2.4 PCMC Interface Signals

Signal	Type	Description
HIG[4:0]	in	**HOST INTERFACE GROUP:** These signals are driven from the PCMC and control the host interface of the LBX. The 82433LX decodes the binary pattern of these lines to perform 29 unique functions (30 for the 83433NX). These signals are synchronous to the rising edge of HCLK.
MIG[2:0]	in	**MEMORY INTERFACE GROUP:** These signals are driven from the PCMC and control the memory interface of the LBX. The LBX decodes the binary pattern of these lines to perform 7 unique functions. These signals are synchronous to the rising edge of HCLK.
PIG[3:0]	in	**PCI INTERFACE GROUP:** These signals are driven from the PCMC and control the PCI interface of the LBX. The LBX decodes the binary pattern of these lines to perform 15 unique functions. These signals are synchronous to the rising edge of HCLK.
MDLE	in	**MEMORY DATA LATCH ENABLE:** During CPU reads from DRAM, the LBX uses a clocked register to transfer data from the MD[31:0] and MP[3:0] lines to the D[31:0] and HP[3:0] lines. MDLE is the clock enable for this register. Data is clocked into this register when MDLE is asserted. The register retains its current value when MDLE is negated. During CPU reads from main memory, the LBX tri-states the D[31:0] and HP[3:0] lines on the rising edge of MDLE when HIG[4:0] = NOPC.
DRVPCI	in	**DRIVE PCI BUS:** This signals enables the LBX to drive either address or data information onto the PCI AD[15:0] lines.

2.4 PCMC Interface Signals (Continued)

Signal	Type	Description
EOL	t/s	**End Of Line:** This signal is asserted when a PCI master read or write transaction is about to overrun a cache line boundary. The low order LBX will have this pin connected to the PCMC (internally pulled up in the PCMC). The high order LBX connects this pin to a pull-down resistor. With one LBX EOL line being pulled down and the other LBX EOL pulled up, the LBX samples the value of this pin on the negation of the RESET signal to determine if it's the high or low order LBX.
PPOUT	t/s	**LBX PARITY:** This signal reflects the parity of the 16 AD lines driven from or latched into the LBX, depending on the command driven on PIG[3:0]. The PCMC uses PPOUT from both LBXs (called PPOUT[1:0]) to calculate the PCI parity signal (PAR) for CPU to PCI transactions during the address phase of the PCI cycle. The LBX uses PPOUT to check the PAR signal for PCI master transactions to memory during the address phase of the PCI cycle. When transmitting data to PCI the PCMC uses PPOUT to calculate the proper value for PAR. When receiving data from PCI the PCMC uses PPOUT to check the value received on PAR. If the L2 cache does not implement parity, the LBX will calculate parity so the PCMC can drive the correct value on PAR during L2 reads initiated by a PCI master. The LBX samples the PPOUT signal at the negation of reset and compares that state with the state of EOL to determine whether the L2 cache implements parity. The PCMC internally pulls down PPOUT[0] and internally pulls up PPOUT[1]. The L2 supports parity if PPOUT[0] is connected to the high order LBX and PPOUT[1] is connected to the low order LBX. The L2 is defined to not support parity if these connections are reversed, and for this case, the LBX will calculate parity. For normal operations either connection allows proper parity to be driven to the PCMC.

2.5 Reset and Clock Signals

Signal	Type	Description
HCLK	in	**HOST CLOCK:** HCLK is input to the LBX to synchronize command and data from the host and memory interfaces. This input is derived from a buffered copy of the PCMC HCLKx output.
PCLK	in	**PCI CLOCK:** All timing on the LBX PCI interface is referenced to the PCLK input. All output signals on the PCI interface are driven from PCLK rising edges and all input signals on the PCI interface are sampled on PCLK rising edges. This input is derived from a buffered copy of the PCMC PCLK output.
RESET	in	**RESET:** Assertion of this signal resets the LBX. After RESET has been negated the LBX configures itself by sampling the EOL and PPOUT pins. RESET is driven by the PCMC CPURST pin. The RESET signal is synchronous to HCLK and must be driven directly by the PCMC.
LP1	out	**LOOP 1:** Phase Lock Loop Filter pin. The filter components required for the LBX are connected to these pins.
LP2	in	**LOOP 2:** Phase Lock Loop Filter pin. The filter components required for the LBX are connected to these pins.
TEST	in	**TEST:** The TEST pin must be tied low for normal system operation.
TSCON	in	**TRI-STATE CONTROL:** This signal enables the output buffers on the LBX. This pin must be held high for normal operation. If TSCON is negated, all LBX outputs will tri-state.

3.0 FUNCTIONAL DESCRIPTION

3.1 LBX Post and Prefetch Buffers

This section describes the five write posting and read prefetching buffers implemented in the LBX. The discussion in this section refers to the operation of both LBXs in the system.

3.1.1 CPU-TO-MEMORY POSTED WRITE BUFFER

The write buffer is a queue 4 Qwords deep, it loads Qwords from the CPU and stores Qwords to memory. It is 4 Qwords deep to accommodate write-backs from the first or second level cache. It is organized as a simple FIFO. Commands driven on the HIG[4:0] lines store Qwords into the buffer, while commands on the MIG[2:0] lines retire Qwords from the buffer. While retiring Qwords to memory, the DRAM controller unit of the PCMC will assert the appropriate MA, CAS[7:0]#, and WE# signals. The PCMC keeps track of full/empty states, status of the data and address.

Byte parity for data to be written to memory is either propagated from the host bus or generated by the LBX. The LBX generates parity for data from the second level cache when the second level cache does not implement parity.

3.1.2 PCI-TO-MEMORY POSTED WRITE BUFFER

The buffer is organized as 2 buffers (4 Dwords each). There is an address storage register for each buffer. When an address is stored one of the two buffers is allocated and subsequent Dwords of data are stored beginning at the first location in that buffer. Buffers are retired to memory strictly in order, Qword at a time.

Commands driven on the PIG[3:0] lines post addresses and data into the buffer. Commands driven on HIG[4:0] result in addresses being driven on the host address bus. Commands driven on MIG[2:0] result in data being retired to DRAM.

For cases where the address targeted by the first Dword is odd, i.e. A[2] = 1, and the data is stored in an even location in the buffer, the LBX correctly aligns the Dword when retiring the data to DRAM. In other words the buffer is capable of retiring a Qword to memory where the data in the buffer is shifted by 1 Dword (Dword is position 0 shifted to 1, 1 shifted to 2 etc.). The DRAM controller of the PCMC asserts the correct CAS[7:0]# signals depending on the PCI C/BE[3:0]# signals stored in the PCMC for that Dword.

The End Of Line (EOL) signal is used to prevent PCI master writes from bursting past the cache line boundary. The device that provides "warning" to the PCMC is the low order LBX. This device contains the PCI master write low order address bits necessary to determine how many Dwords are left to the end of the line. Consequently, the LBX protocol uses the EOL signal from the low order LBX to provide this "end-of-line" warning to the PCMC, so that it may retry a PCI master write when it bursts past the cache line boundary. This protocol is described fully in Section 3.3.6.

The LBX calculates Dword parity on PCI write data, sending the proper value to the PCMC on PPOUT. The LBX generates byte parity on the MP signals for writing into DRAM.

3.1.3 PCI-TO-MEMORY READ PREFETCH BUFFER

This buffer is organized as a line buffer (4 Qwords) for burst transfers to PCI. The data is transferred into the buffer a Qword at a time and read out a Dword at a time. The LBX then effectively decouples the memory read rate from the PCI rate to increase concurrence.

Each new transaction begins by storing the first Dword in the first location in the buffer. The starting Dword for reading data out of the buffer onto PCI must be specified within a Qword boundary; that is the first requested Dword on PCI could be an even or odd Dword. If the snoop for a PCI master read results in a write-back from first or second level caches, this write back is sent directly to PCI and main memory. The following two paragraphs describe this process for cache line write-backs.

Since the write-back data from L1 is in linear order, writing into the buffer is straightforward. Only those Qwords to be transferred into PCI are latched into the PCI-to-memory read buffer. For example, if the address targeted by PCI is in the 3rd or 4th Qword in the line, the first 2 Qwords of write back data are discarded and not written into the read buffer. The primary cache write-back must always be written

completely to the CPU-to-Memory posted Write Buffer.

If the PCI master read data is read from the secondary cache, it is not written back to memory. Write-backs from the second level cache, when using burst SRAMs, are in Pentium processor burst order (the order depending on which Qword of the line is targeted by the PCI read). The buffer is directly addressed when latching second level cache write-back data to accommodate this burst order. For example, if the requested Qword is Qword 1, then the burst order is 1-0-3-2. Qword 1 is latched in buffer location 0, Qword 0 is discarded, Qword 3 is latched into buffer location 2 and Qword 2 is latched into buffer location 1.

Commands driven on MIG[2:0] and HIG[4:0] enter data into the buffer from the DRAM interface and the host interface (i.e. the caches), respectively. Commands driven on the PIG[3:0] lines drive data from the buffer onto the PCI AD[31:0] lines.

Parity driven on the PPOUT signal is calculated from the byte parity received on the host bus or the memory bus, whichever is the source. If the second level cache is the source of the data and does not implement parity, the parity driven on PPOUT is generated by the LBX from the second level cache data. If main memory is the source of the read data, PCI parity is calculated from the DRAM byte parity. Main memory must implement byte parity to guarantee correct PCI parity generation.

3.1.4 CPU-TO-PCI POSTED WRITE BUFFER

The CPU-to-PCI Posted Write Buffer is 4 Dwords deep. The buffer is constructed as a simple FIFO, with some performance enhancements. An address is stored in the LBX with each Dword of data. The structure of the buffer accommodates the packetization of writes to be burst on PCI. This is accomplished by effectively discarding addresses of data Dwords driven within a burst. Thus, while an address is stored for each Dword, an address is not necessarily driven on PCI for each Dword. The PCMC determines when a burst write may be performed based on consecutive addresses. The buffer also enables consecutive bytes to be merged within a single Dword, accommodating byte, word, and misaligned Dword string store and string move operations. Qword writes on the host bus are stored within the buffer as two individual Dword writes, with separate addresses.

The storing of an address with each Dword of data allows burst writes to be retried easily. In order to retry transactions, the FIFO is effectively "backed up" by one Dword. This is accomplished by making the FIFO physically one entry larger than it is logically. Thus, the buffer is physically 5 entries deep (an entry consists of an address and a Dword of data), while logically it is considered full when 4 entries have been posted. This design allows the FIFO to be backed up one entry when it is logically full.

Commands driven on HIG[4:0] post addresses and data into the buffer, and commands driven on PIG[3:0] retire addresses and data from the buffer and drive them onto the PCI AD[31:0] lines. As discussed previously, when bursting, not all addresses are driven onto PCI.

Data parity driven on the PPOUT signal is calculated from the byte parity received on the host bus. Address parity driven on PPOUT is calculated from the address received on the host bus.

3.1.5 CPU-TO-PCI READ PREFETCH BUFFER

This prefetch buffer is organized as a single buffer 4 Dwords deep. The buffer is organized as a simple FIFO. reads from the buffer are sequential; the buffer does not support random access of its contents. To support reads of less than a Dword the FIFO read pointer can function with or without a pre-increment. The pointer can also be reset to the first entry before a Dword is driven. When a Dword is read, it is driven onto both halves of the host data bus.

Commands driven on the HIG[4:0] lines enable read addresses to be sent onto PCI, the addresses are driven using PIG[3:0] commands. Read data is latched into the LBX by commands driven on the PIG[3:0] lines and the data is driven onto the host data bus using commands driven on the HIG[4:0] lines.

The LBX calculates Dword parity on PCI read data, sending the proper value to the PCMC on PPOUT. The LBX does not generate byte parity on the host data bus when the CPU reads PCI.

3.2 LBX Interface Command Descriptions

This section describes the functionality of the HIG, MIG and PIG commands driven by the PCMC to the LBXs.

3.2.1 HOST INTERFACE GROUP: HIG[4:0]

The Host Interface commands are shown in Table 1. These commands are issued by the host interface of the PCMC to the LBXs in order to perform the following functions:

- Reads from CPU-to-PCI read prefetch buffer when the CPU reads from PCI.
- Stores write-back data to PCI-to-memory read prefetch buffer when PCI read address results in a hit to a modified line in first or second level caches.
- Posts data to CPU-to-memory write buffer in the case of a CPU to memory write.
- Posts data to CPU-to-PCI write buffer in the case of a CPU to PCI write.
- Drives host address to Data lines and data to address lines for programming the PCMC configuration registers.

Table 1. HIG Commands

Command	Code	Description
NOPC	00000b	No Operation on CPU Bus
CMR	11100b	CPU Memory Read
CPRF	00100b	CPU Read First Dword from CPU-to-PCI Read Prefetch Buffer
CPRA	00101b	CPU Read Next Dword from CPU-to-PCI Read Prefetch Buffer, Toggle A
CPRB	00110b	CPU Read Next Dword from CPU-to-PCI Read Prefetch Buffer, Toggle B
CPRQ	00111b	CPU Read Qword from CPU-to-PCI Read Prefetch Buffer
SWB0	01000b	Store Write-Back Data Qword 0 to PCI-to-Memory Read Buffer
SWB1	01001b	Store Write-Back Data Qword 1 to PCI-to-Memory Read Buffer
SWB2	01010b	Store Write-Back Data Qword 2 to PCI-to-Memory Read Buffer
SWB3	01011b	Store Write-Back Data Qword 3 to PCI-to-Memory Read Buffer
PCMWQ	01100b	Post to CPU-to-Memory Write Buffer Qword
PCMWFQ	01101b	Post to CPU-to-Memory Write and PCI-to-Memory Read Buffer First Qword
PCMWNQ	01110b	Post to CPU-to-Memory Write and PCI-to-Memory Read Buffer Next Qword
PCPWL	10000b	Post to CPU-to-PCI Write Low Dword
MCP3L	10011b	Merge to CPU-to-PCI Write Low Dword 3 Bytes
MCP2L	10010b	Merge to CPU-to-PCI Write Low Dword 2 Bytes
MCP1L	10001b	Merge to CPU-to-PCI Write Low Dword 1 Byte
PCPWH	10100b	Post to CPU-to-PCI Write High Dword
MCP3H	10111b	Merge to CPU-to-PCI Write High Dword 3 Bytes
MCP2H	10110b	Merge to CPU-to-PCI Write High Dword 2 Bytes
MCP1H	10101b	Merge to CPU-to-PCI Write High Dword 1 Byte
LCPRAD	00001b	Latch CPU-to-PCI Read Address
DPRA	11000b	Drive Address from PCI A/D Latch to CPU Address Bus
DPWA	11001b	Drive Address from PCI-to-Memory Write Buffer to CPU Address Bus
ADCPY	11101b	Address to Data Copy in the LBX
DACPYH	11011b	Data to Address Copy in the LBX High Dword
DACPYL	11010b	Data to Address Copy in the LBX Low Dword
PSCD	01111b	Post Special Cycle Data
DRVFF	11110b	Drive FF..FF (All 1's) onto the Host Data Bus
PCPWHC	00011b	Post to CPU-to-PCI Write High Dword Configuration

NOTE:
All other patterns are reserved.

NOPC No Operation is performed on the host bus by the LBX hence it tri-states its host bus drivers.

CMR This command effectively drives DRAM data onto the host data bus. The LBX acts as a transparent latch in this mode, depending on MDLE for latch control. With the MDLE signal high the CMR command will cause the LBXs to buffer memory data onto the host bus. When MDLE is low. The LBX will drive onto the host bus whatever memory data that was latched when MDLE was negated.

CPRF This command reads the first Dword of the CPU-to-PCI read prefetch buffer. The read pointer of the FIFO is set to point to the first Dword. The Dword is driven onto the high and low halves of the host data bus.

CPRA This command increments the read pointer of the CPU-to-PCI read prefetch buffer FIFO and drives that Dword onto the host bus when it is driven after a CPRF or CPRB command. If driven after another CPRA command, the LBX drives the current Dword while the read pointer of the FIFO is not incremented. The Dword is driven onto the upper and lower halves of the host data bus.

CPRB This command increments the read pointer of the CPU-to-PCI read prefetch buffer FIFO and drives that Dword onto the host bus when it is driven after a CPRA command. If driven after another CPRB command, the LBX drives the current Dword while the read pointer of the FIFO is not incremented. The Dword is driven onto the upper and lower halves of the host data bus.

CPRQ This command drives the first Dword stored in the CPU-to-PCI read prefetch buffer onto the lower half of the host data bus, and drives the second Dword onto the upper half of the host data bus, regardless of the state of the read pointer. The read pointer is not affected by this command.

SWB0 This command stores a Qword from the host data lines into location 0 of the PCI-to-Memory Read Buffer. Parity is either generated for the data or propagated from the host bus based on the state of the PPOUT signals sampled at the negation of RESET when the LBXs were initialized.

SWB1 This command, (similar to SWB0), stores a Qword from the host data lines into location 1 of the PCI-to-Memory Read Buffer. Parity is either generated from the data or propagated from the host bus based on the state of the PPOUT signal sampled at the falling edge of RESET.

SWB2 This command, (similar to SWB0), stores a Qword written back from the first or second level cache into location 2 of the PCI-to-memory read buffer. Parity is either generated from the data or propagated from the host bus based on the state of the PPOUT signal sampled at the falling edge of RESET.

SWB3 This command stores a Qword from the host data lines into location 3 of the PCI-to-Memory Read Buffer. Parity is either generated for the data or propagated from the host bus based on the state of the PPOUT signal sampled at the falling edge of RESET.

PCMWQ This command posts one Qword of data from the host data lines to CPU-to-Memory Write Buffer in case of a CPU memory write or a write-back from the second level cache.

PCMWFQ If the PCI Memory read address leads to a hit on a modified line in the first level cache, then a write-back is scheduled and this data has to be written into the CPU-to-Memory Write Buffer and PCI-to-Memory Read Buffer at the same time. The write-back of the first Qword is done by this command to both the buffers.

PCMWNQ This command follows the previous command to store or post subsequent write-back Qwords.

PCPWL This command posts the low Dword of a CPU-to-PCI write. The CPU-to-PCI Write Buffer stores a Dword of PCI address for every Dword of data. Hence, this command also stores the address of the Low Dword in the address location for the data. Address bit 2 (A2) is not stored directly. This command assumes a value of 0 for A2 and this is what is stored.

MCP3L This command merges the 3 most significant bytes of the low Dword of the host data bus into the last Dword posted to the CPU-to-PCI write buffer. The address is not modified.

MCP2L This command merges the 2 most significant bytes of the low Dword of the host data bus into the last Dword posted to the CPU-to-PCI write buffer. The address is not modified.

MCP1L This command merges the most significant byte of the low Dword of the host data bus into the last Dword posted to the CPU-to-PCI write buffer. The address is not modified.

PCPWH This command posts the upper Dword of a CPU-to-PCI write, with its address, into the address location. Hence, to do a Qword write PCPWL has to be followed by a PCPWH. Address bit 2 (A2) is not stored directly. This command forces a value of 1 for A2 and this is what is stored.

MCP3H This command merges the 3 most significant bytes of the high Dword of the host data bus into the last Dword posted to the CPU-to-PCI Write Buffer. The address is not modified.

MCP2H This command merges the 2 most significant bytes of the high Dword of the host data bus into the last Dword posted to the CPU-to-PCI Write Buffer. The address is not modified.

MCP1H This command merges the most significant byte of the high Dword of the host data bus into the last Dword posted to the CPU-to-PCI Write Buffer. The address is not modified.

LCPRAD This command latches the host address to drive on PCI for a CPU-to-PCI read. It is necessary to latch the address in order to drive inquire addresses on the host address bus before the CPU address is driven onto PCI.

DPRA The PCI memory read address is latched in the PCI A/D latch by a PIG command LCPRAD, this address is driven onto the host address bus by DPRA. Used in PCI to memory read transaction.

DPWA The DPWA command drives the address of the current PCI Master Write Buffer onto the host address bus. This command is potentially driven for multiple cycles. When it is no longer driven, the read pointer will increment to point to the next buffer, and a subsequent DPWA command will read the address from that buffer.

ADCPY This command drives the host data bus with the host address. The address is copied on the high and low halves of the Qword data bus; i.e. A[31:0] is copied onto D[31:0] and D[63:32]. This command is used when the CPU writes to the PCMC configuration registers.

DACPYH This command drives the host address bus with the high Dword of host data. This command is used when the CPU writes to the PCMC configuration registers.

DACPYL This command drives the host address bus with the low Dword of host data. This command is used when the CPU writes to the PCMC configuration registers.

PSCD This command is used to post the value of the Special Cycle code into the CPU-to-PCI Posted Write Buffer. The value is driven onto the A[31:0] lines by the PCMC, after acquiring the address bus by asserting AHOLD. The value on the A[31:0] lines is posted into the DATA location in the CPU-to-PCI Posted Write Buffer.

DRVFF This command causes the LBX to drive all "1s" (i.e. FFFFFFFFh) onto the host data bus. It is used for CPU reads from PCI that terminate with master abort.

PCPWHC This command posts the high half of the CPU data bus. The LBXs post the high half of the data bus even if A2 from the PCMC is low. This command is used during configuration writes when using PCI configuration access mechanism #1.

3.2.2 MEMORY INTERFACE GROUP: MIG[2:0]

The Memory Interface commands are shown in Table 2. These commands are issued by the DRAM controller of the PCMC to perform the following functions:

- Retires data from CPU-to-Memory Write Buffer to DRAM.
- Stores data into PCI-to-Memory Read Buffer when the PCI read address is targeted to DRAM.
- Retires PCI-to-Memory Write Buffer to DRAM.

Table 2. MIG Commands

Command	Code	Description
NOPM	000b	No Operation on Memory Bus
PMRFQ	001b	Place into PCI-to-Memory Read Buffer First Qword
PMRNQ	010b	Place into PCI-to-Memory Read Buffer Next Qword
RCMWQ	100b	Retire CPU-to-Memory Write Buffer Qword
RPMWQ	101b	Retire PCI-to-Memory Write Buffer Qword
RPMWQS	110b	Retire PCI-to-Memory Write Buffer Qword Shifted
MEMDRV	111b	Drive Latched Data Onto Memory Bus for 1 Clock Cycle

NOTE:
All other patterns are reserved.

NOPMN Operation on the memory bus. The LBX tri-states its drivers driving the memory bus.

PMRFQ The PCI-to-Memory read address targets memory if there is a miss on first and second caches. This command stores the first Qword of data starting at the first location in the buffer. This buffer is 8 Dwords or 1 cache line deep.

PMRNQ This command stores subsequent Qwords from memory starting at the next available location in the PCI-to-Memory Read Buffer. It is always used after PMRFQ.

RCMWQ This command retires one Qword from the CPU-to-Memory Write Buffer to DRAM. The address is stored in the address queue for this buffer in the PCMC.

RPMWQ This command retires one Qword of data from one line of the PCI-to-Memory write buffer to DRAM. When all the valid data in one buffer is retired, the next RPMWQ (or RPMWQS) will read data from the next buffer.

RPMWQS This command retires one Qword of data from one line of PCI-to-Memory write buffer to DRAM. For this command the data in the buffer is shifted by one Dword (Dword in position 0 is shifted to 1, 1 to 2 etc.). This is because the address targeted by the first Dword of the write could be an odd Dword (i.e., address bit[2] is a 1). To retire a misaligned line this command has to be used for all the data in the buffer. When all the valid data in one buffer is retired, the next RPMWQ (or RPMWQS) will read data from the next buffer.

MEMDRV For a memory write operation the data on the memory bus is required for more than one clock cycle hence all DRAM retires are latched and driven to the memory bus in subsequent cycles by this command.

3.2.3 PCI INTERFACE GROUP: PIG[3:0]

The PCI Interface commands are shown in Table 3. These commands are issued by the PCI master/slave interface of the PCMC to perform the following functions:

- Slave posts address and data to PCI-to-Memory Write Buffer.
- Slave sends PCI-to-Memory read data on the AD bus.
- Slave latches PCI master memory address so that it can be gated to the host address bus.
- Master latches CPU-to-PCI read data from the AD bus.
- Master retires CPU-to-PCI write buffer.
- Master sends CPU-to-PCI address to the AD bus.

The PCI AD[31:0] lines are driven by asserting the signal DRVPCI. This signal is used for both master and slave transactions.

Parity is calculated on either the value being driven onto PCI or the value being received on PCI, depending on the command. In Table 3, the PAR column has been included to indicate the value that the PPOUT signals are based on. An "I" indicates that the PPOUT signals reflect the parity of the AD lines as inputs to the LBX. An "O" indicates that the PPOUT signals reflect the value being driven on the PCI AD lines. See Section 3.3.4 for the timing relationship between the PIG[3:0] command, the AD[31:0] lines, and the PPOUT signals.

Table 3. PIG Commands

Command	Code	PAR	Description
PPMWA	1000b	I	Post to PCI-to-Memory Write Buffer Address
PPMWD	1001b	I	Post to PCI-to-Memory Write Buffer Data
SPMRH	1101b	O	Send PCI Master Read Data High Dword
SPMRL	1100b	O	Send PCI Master Read Data Low Dword
SPMRN	1110b	O	Send PCI Master Read Data Next Dword
LCPRF	0000b	I	Latch CPU Read from PCI into Read Prefetch Buffer First Dword
LCPRA	0001b	I	Latch CPU Read from PCI into Prefetch Buffer Next Dword, A Toggle
LCPRB	0010b	I	Latch CPU Read from PCI into Prefetch Buffer Next Dword, B Toggle
DCPWA	0100b	O	Drive CPU-to-PCI Write Buffer Address
DCPWD	0101b	O	Drive CPU-to-PCI Write Buffer Data
DCPWL	0110b	O	Drive CPU-to-PCI Write Buffer Last Data
DCCPD	1011b	O	Discard Current CPU-to-PCI Write Buffer Data
BCPWR	1010b	O	Backup CPU-to-PCI Write Buffer for Retry
SCPA	0111b	O	Send CPU-to-PCI Address
LPMA	0011b	I	Latch PCI Master Address

NOTE:
All other patterns are reserved.

PPMWA This command selects a new buffer and places the PCI master address latch value into the address register for that buffer. The next PPMWD command posts write data in the first location of this newly selected buffer. This command also causes the EOL logic to decrement the count of Dwords remaining in the line.

PPMWD This command stores the value in the AD latch into the next data location in the currently selected buffer. This command also causes the EOL logic to decrement the count of Dwords remaining in the line.

SPMRH This command sends the high order Dword from the first Qword of the PCI-to-Memory Read Buffer onto PCI. This command also causes the EOL logic to decrement the count of Dwords remaining in the line.

SPMRL This command sends the low order Dword from the first Qword of the PCI-to-Memory Read Buffer onto PCI. This command also selects the Dword alignment for the transaction and causes the EOL logic to decrement the count of Dwords remaining in the line.

SPMRN This command sends the next Dword from the PCI-to-Memory Read Buffer onto PCI. This command also causes the EOL logic to decrement the count of Dwords remaining in the line. This command is used for the second and all subsequent Dwords of the current transaction.

LCPRF This command acquires the value of the AD[31:0] lines into the first location in the CPU-to-PCI Read Prefetch Buffer until a different command is driven.

LCPRA When driven after a LCPRF or LCPRB command, this command latches the value of the AD[31:0] lines into the next location into the CPU-to-PCI Read Prefetch Buffer. When driven after another LCPRA command, this command latches the value on AD[31:0] into the same location in the CPU-to-PCI Read Prefetch Buffer, overwriting the previous value.

LCPRB When driven after a LCPRA command, this command latches the value of the AD[31:0] lines into the next location into the CPU-to-PCI Read Prefetch Buffer. When driven after another LCPRB command, this command latches the value on AD[31:0] into the same location in the CPU-to-PCI Read Prefetch Buffer, overwriting the previous value.

DCPWA This command drives the next address in the CPU-to-PCI Write Buffer onto PCI. The read pointer of the FIFO is not incremented.

DCPWD This command drives the next data Dword in the CPU-to-PCI Write Buffer onto PCI. The read pointer of the FIFO is incremented on the next PCLK if TRDY# is asserted.

DCPWL This command drives the previous data Dword in the CPU-to-PCI Write Buffer onto PCI. This is the data which was driven by the last DCPWD command. The read pointer of the FIFO is not incremented.

DCCPD This command discards the current Dword in the CPU-to-PCI Write Buffer. This is used to clear write data when the write transaction terminates with master abort, where TRDY# is never asserted.

BCPWR For this command the CPU-to-PCI Write Buffer is "backed up" one entry such that the address/data pair last driven with the DCPWA and DCPWD commands will be driven again on the AD[31:0] lines when the commands are driven again. This command is used when the target has retried the write cycle.

SCPA This command drives the value on the host address bus onto PCI.

LPMA This command stores the previous AD[31:0] value into the PCI master address latch. If the EOL logic determines that the requested Dword is the last Dword of a line, then the EOL signal will be asserted; otherwise the EOL signal will be negated.

3.3 LBX Timing Diagrams

This section describes the timing relationship between the LBX control signals and the interface buses.

3.3.1 HIG[4:0] COMMAND TIMING

The commands driven on HIG[4:0] can cause the host address bus and/or the host data bus to be driven and latched. The following timing diagram illustrates the timing relationship between the driven command and the buses. The "host bus" in Figure 4 could be address and/or data.

Note that the Drive command takes two cycles to drive the host data bus, but only one to drive the address. When the NOPC command is sampled, the LBX takes only one cycle to release the host bus.

The Drive commands in Figure 4 are any of the following:

CMR	**CPRF**	**CPRA**	**CPRB**
CPRQ	**DPRA**	**DPWA**	**ADCPY**
DACPYH	**DACPYL**	**DRVFF**	

The Latch command in Figure 4 is any of the following:

SWB0	**SWB1**	**SWB2**	**SWB3**
PCMWQ	**PCMWFQ**	**PCMWNQ**	**PCPWL**
MCP3L	**MCP2L**	**MCP1L**	**PCPWH**
MCP3H	**MCP2H**	**LCPRAD**	**PSCD**

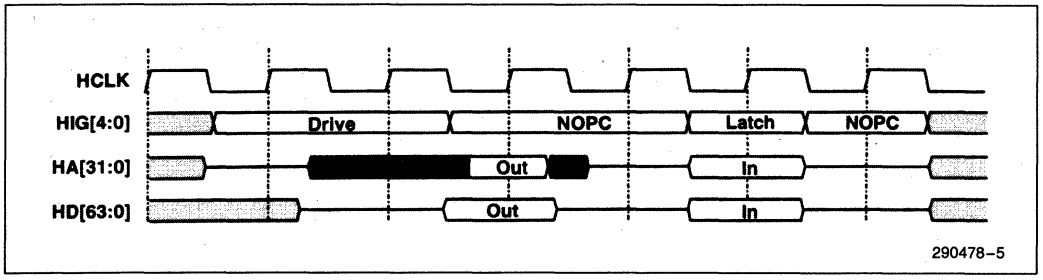


Figure 4. HIG[4:0] Command Timing

3.3.2 HIG[4:0] MEMORY READ TIMING

Figure 5 illustrates the timing relationship between the HIG[4:0], MIG[2:0], CAS[7:0]#, and MDLE signals for DRAM memory reads. The delays shown in the diagram do not represent the actual AC timings, but are intended only to show how the delay affects the sequencing of the signals.

When the CPU is reading from DRAM, the HIG[4:0] lines are driven with the CMR command that causes the LBX to drive memory data onto the HD bus. Until the MD bus is valid, the HD bus is driven with invalid data. When CAS[7:0]# assert, the MD bus becomes valid after the DRAM CAS[7:0]# access time. The MD and MP lines are directed through a synchronous register inside the LBX to the HD and HP lines. MDLE acts as a clock enable for this register. When MDLE is asserted, the LBX samples the MD and MP lines. When MDLE is negated, the MD and HD register retains its current value.

The LBX releases the HD bus based on sampling the NOPC command on the HIG[4:0] lines and MDLE being asserted. By delaying the release of the HD bus until MDLE is asserted, the LBX provides hold time for the data with respect to the write enable strobes (CWE[7:0]#) of the second level cache.

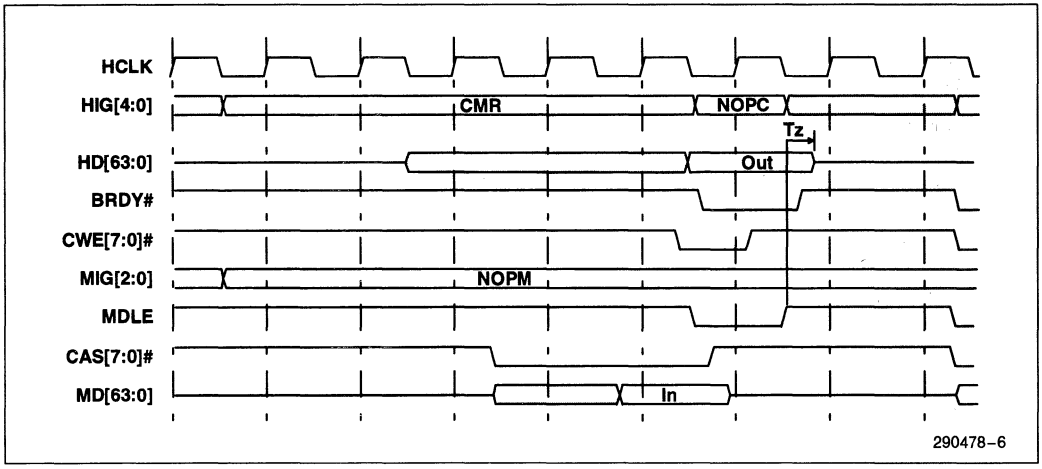


Figure 5. CPU Read from Memory

3.3.3 MIG[2:0] COMMAND

Figure 6 illustrates the timing of the MIG[2:0] commands with respect to the MD bus, CAS[7:0]#, and WE#. Figure 6 shows the MD bus transitioning from a read to a write cycle.

The Latch command in Figure 6 is any of the following:
PMRFQ PMRNQ

The Retire command in Figure 6 is any of the following:
RCMWQ RPMWQ RPMWQS

The data on the MD bus is sampled at the end of the first cycle into the LBX based on sampling the Latch command. The CAS[7:0]# signals can be negated in the next cycle. The WE# signal is asserted in the next cycle. The required delay between the assertion of WE# and the assertion of CAS[7:0]# means that the MD bus has 2 cycles to turn around; hence the NOPM command driven in the second clock. The LBX starts to drive the MD bus based on sampling the Retire command at the end of the third clock. After the Retire command is driven for 1 cycle, the data is held at the output by the MEMDRV command. The LBX releases the MD bus based on sampling the NOPM command at the end of the sixth clock.

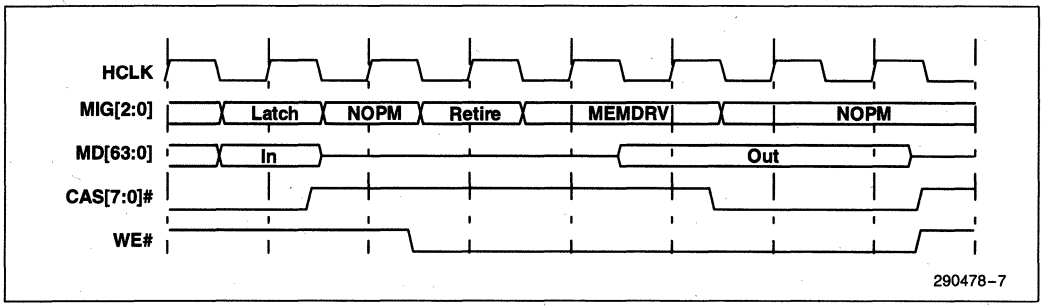


Figure 6. MIG[2:0] Command Timing

3.3.4 PIG[3:0] COMMAND, DRVPCI, AND PPOUT TIMING

Figure 7 illustrates the timing of the PIG[3:0] commands, the DRVPCI signal, and the PPOUT[1:0] signal relative to the PCI AD[31:0] lines.

The Drive commands in Figure 7 are any of the following:
SPMRH SPMRL SPMRN
DCPWA DCPWD DCPWL
SCPA

The Latch commands in Figure 7 are any of the following:
PPMWA PPMWD LPMA

The following commands do not fit in either category, although they function like Latch type commands with respect to the PPOUT[1:0] signals. They are described in Section 3.3.5.

LCPRF LCPRA LCPRB

The DRVPCI signal is driven synchronous to the PCI bus, enabling the LBXs to initiate driving the PCI AD[31:0] lines one clock after DRVPCI is asserted. As shown in Figure 7, if DRVPCI is asserted in cycle N, the PCI AD[31:0] lines are driven in cycle N+1. The negation of the DRVPCI signal causes the LBXs to asynchronously release the PCI bus, enabling the LBXs to cease driving the PCI AD[31:0] lines in the same clock that DRVPCI is negated. As shown in Figure 7, if DRVPCI is negated in cycle N, the PCI AD[31:0] lines are released in cycle N.

PCI address and data parity is available at the LBX interface on the PPOUT lines from the LBX. The parity for data flow from PCI to LBX is valid 1 clock cycle after data on the AD bus. The parity for data flow from LBX to PCI is valid in the same cycle as the data. When the AD[31:0] lines transition from input to output, there is no conflict on the parity lines due to the dead cycle for bus turnaround. This is illustrated in the sixth and seventh clock of Figure 7.

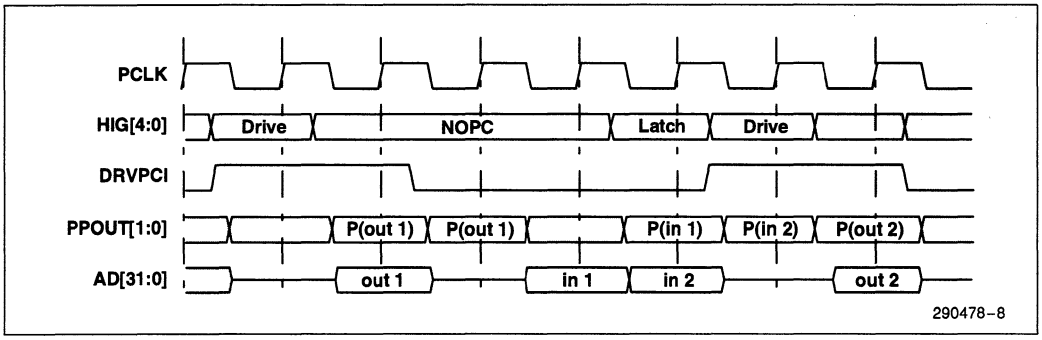


Figure 7. PIG[3:0] Command Timing

3.3.5 PIG[3:0]: READ PREFETCH BUFFER COMMAND TIMING

The structure of the CPU-to-PCI read prefetch buffer requires special considerations due to the partition of the PCMC and LBX. The PCMC interfaces only to the PCI control signals, while the LBXs interface only to the data. Therefore, it is not possible to latch a Dword of data into the prefetch buffer after it is qualified by TRDY#. Instead, the data is repetitively latched into the same location until TRDY# is sampled asserted. Only after TRDY# is sampled asserted is data valid in the buffer. A toggling mechanism is implemented to advance the write pointer to the next Dword after the current Dword has been qualified by TRDY#.

Other considerations of the partition are taken into account on the host side as well. When reading from the buffer, the command to drive the data onto the host bus is sent before it is known that the entry is valid. This method avoids the wait-state that would be introduced by waiting for an entry's TRDY# to be asserted before sending the command to drive the entry onto the host bus. The FIFO structure of the buffer also necessitates a toggling scheme to advance to the next buffer entry after the current entry has been successfully driven. Also, this method gives the LBX the ability to drive the same Dword twice, enabling reads of less than a Dword to be serviced by the buffer; reads of individual bytes of a Dword would read the same Dword 4 times.

The HIG[4:0] and PIG[3:0] lines are defined to enable the features described previously. The LCPRF PIG[3:0] command latches the first PCI read Dword into the first location in the CPU-to-PCI read prefetch buffer. This command is driven until TRDY# is sampled asserted. The valid Dword would then be in the first location of the buffer. The cycle after TRDY# is sampled asserted, the PCMC drives the LCPRA command on the PIG[3:0] lines. This action latches the value on the PCI AD[31:0] lines into the *next* Dword location in the buffer. Again, the LCPRA command is driven until TRDY# is sampled asserted. Each cycle the LCPRA command is driven, data is latched into the same location in the buffer. When TRDY# is sampled asserted, the PCMC drives the LCPRB command on the PIG[3:0] lines. This latches the value on the AD[31:0] lines into the next location in the buffer, the one *after* the location that the previous LCPRA command latched data into. After TRDY# has been sampled asserted again, the command switches back to LCPRA. In this way, the same location in the buffer can be filled repeatedly until valid, and when it is known that the location is valid, the next location can be filled.

The commands for the HIG[4:0], CPRF, CPRA, and CPRB, work exactly the same way. If the same command is driven, the same data is driven. Driving an appropriately different command results in the next data being driven. Figure 8 illustrates the usage of these commands.

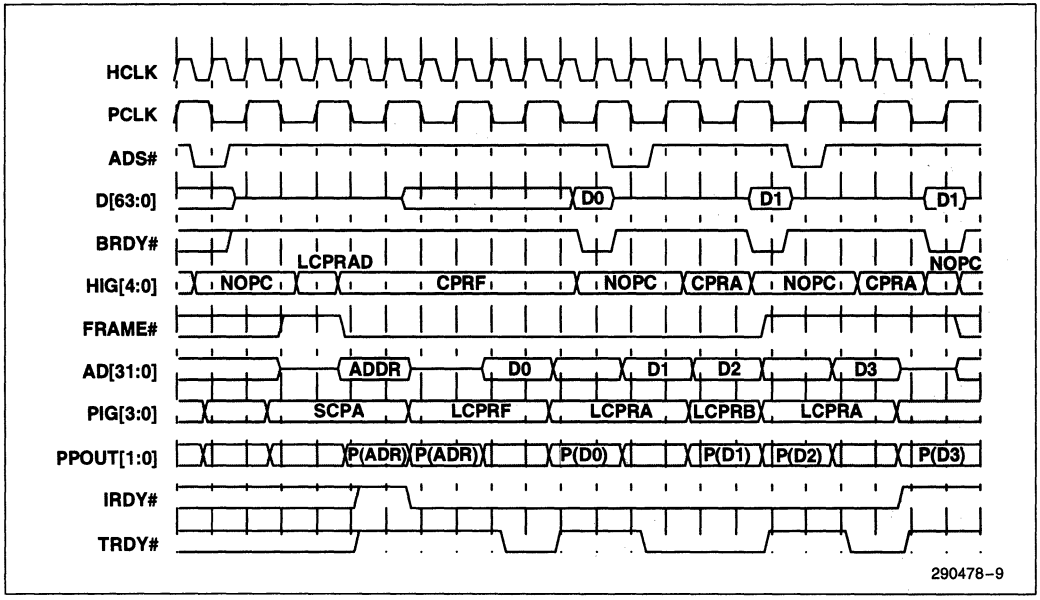


Figure 8. PIG[3:0] CPU-to-PCI Read Prefetch Buffer Commands

Figure 8 shows an example of how the PIG commands function on the PCI side. The LCPRF command is driven on the PIG[3:0] lines until TRDY# is sampled asserted at the end of the fifth PCI clock. The LCPRA command is then driven until TRDY# is again sampled asserted at the end of the seventh PCI clock. TRDY# is sampled asserted again so LCPRB is driven only once. Finally, LCPRA is driven again until the last TRDY# is asserted at the end of the tenth PCI clock. In this way, 4 Dwords are latched in the read CPU-to-PCI prefetch buffer.

Figure 8 also shows an example of how the HIG commands function on the host side of the LBX. Two clocks after sampling the CPRF command, the LBX drives the host data bus. The data takes two cycles to become stable. The first data driven in this case is invalid, since the data has not arrived on PCI. The data driven on the host bus changes in the seventh host clock, since the LCPRF command has been driven on the PIG[3:0] lines the previous cycle, latching a new value into the first location of the read prefetch buffer. At this point the data is not the correct value, since TRDY# has not yet been asserted on PCI. The LCPRF command is driven again in the fifth PCI clock while TRDY# is sampled asserted at the end of this clock. The requested data for the read is then latched into the first location of the read prefetch buffer and driven onto the host data bus, becoming valid at the end of CPU clock 12. The BRDY# signal can therefore be driven asserted in this clock. The following read transaction (issued in CPU clock 15) requests the next Dword, and so the CPRA command is driven on the HIG[4:0] lines, advancing to read the next location in the read prefetch buffer. As the correct data is already there, the command is driven only once for this transaction. The next read transaction requests data in the same Dword as the previous. Therefore, the CPRA command is driven again, the buffer is not advanced, and the same Dword is driven onto the host bus.

3.3.6 PIG[3:0]: END-OF-LINE WARNING SIGNALS: EOL

When posting PCI master writes, the PCMC must be informed when the line boundary is about to be overrun, as it has no way of determining this itself (recall that the PCMC does not receive any address bits from PCI). The low order LBX determines this, as it contains the low order bits of the PCI master write address and also tracks how many Dwords of write data have been posted. Therefore, the low order LBX component sends the "end-of-line" warning to the PCMC. This is accomplished with the EOL signal driven from the low order LBX to the PCMC. Figure 9 illustrates the timing of this signal.

1. The FRAME# signal is sampled asserted in the first cycle. The LPMA command is driven on the PIG[3:0] signals to hold the address while it is being decoded (e.g. in the MEMCS# decode circuit of the 82378 SIO). The first data (D0) remains on the bus until TRDY# is asserted in response to MEMCS# being sampled asserted in the third clock.
2. The PPMWA command is driven in response to sampling MEMCS# asserted. TRDY# is asserted in this cycle indicating that D0 has been latched at the end of the fourth clock. The action of the PPMWA command is to transfer the PCI address captured in the PCI AD latch at the end of the first clock to the posting buffer, and open the PCI AD latch in order to capture the data. This data will be posted to the write buffer in the following cycle by the PPMWD command.
3. The EOL signal is first negated when the LPMA command is driven on the PIG[3:0] signals. However, if the first data Dword accepted is also the last that should be accepted, the EOL signal will be asserted in the third clock. This is the "end-of-line" indication. In this case, the EOL signal is asserted as soon as the LPMA command has been latched. The action by the PCMC in response is to negate TRDY# and assert STOP# in the fifth clock. Note that the EOL signal is asserted even before the MEMCS# signal is sampled asserted in this case. The EOL signal will remain asserted until the next time the LPMA command is driven.
4. If the second Dword is the last that should be accepted, the EOL signal will be asserted in the fifth clock to negate TRDY# and assert STOP# on the following clock. The EOL signal is asserted in response to the PPMWA command being sampled, and relies on the knowledge that TRDY# for the first Dword of data will be sampled asserted by the master in the same cycle (at the end of the fourth clock). Therefore, to prevent a third assertion of TRDY# in the sixth clock, the EOL signal must be asserted in the fifth clock.

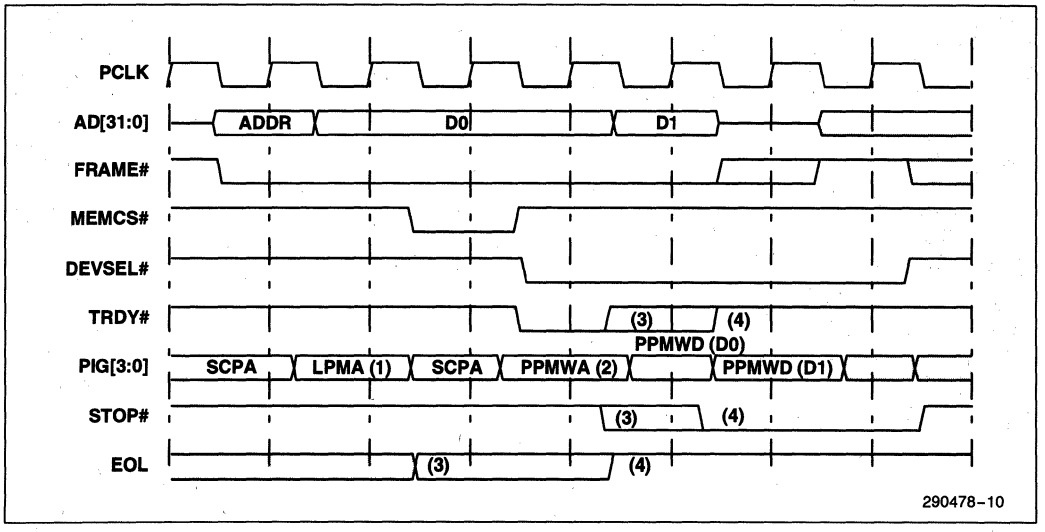


Figure 9. EOL Signal Timing for PCI Master Writes

A similar sequence is defined for PCI master reads. While it is possible to know when to stop driving read data due to the fact that the read address is latched into the PCMC before any read data is driven on PCI, the use of the EOL signal for PCI master reads simplifies the logic internal to the PCMC. Figure 10 illustrates the timing of EOL with respect to the PIG[3:0] commands to drive out PCI read data.

Note that unlike the PCI master write sequence, the STOP# signal is asserted with the last data transfer, not after.

1. The LPMA command sampled at the end of the second clock causes the EOL signal to assert if there is only one Dword left in the line, otherwise it will be negated. The first TRDY# will also be the last, and the STOP# signal will be asserted with TRDY#.
2. The SPMRH command causes the count of the number of Dwords left in the line to be decremented. If this count reaches one, the EOL signal is asserted. The next TRDY# will be the last, and STOP# is asserted with TRDY#.

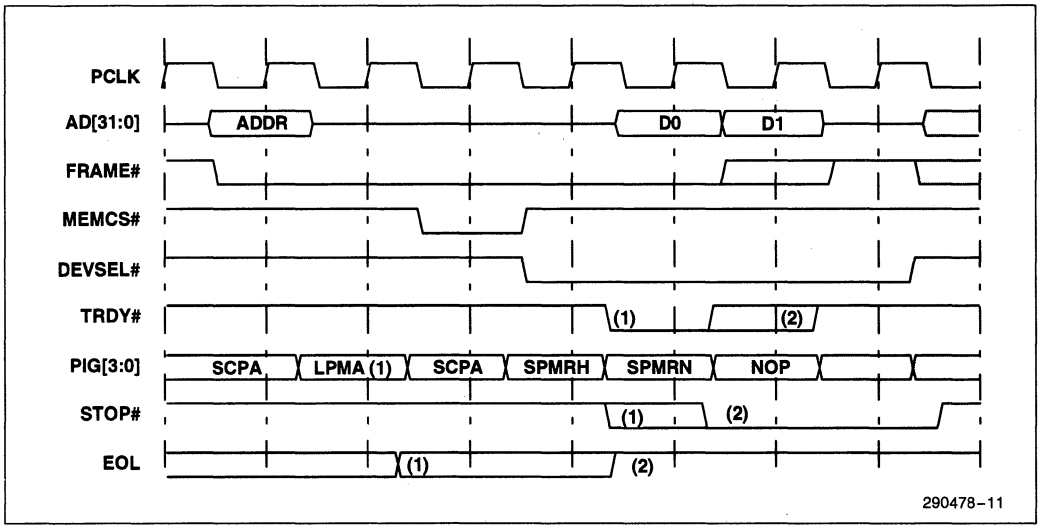


Figure 10. EOL Signal Timing for PCI Master Reads

3.4 PLL Loop Filter Components

As shown in Figure 11, loop filter components are required on the LBX components. A 4.7 KΩ 5% resistor is typically connected between pins LP1 and LP2. Pin LP2 has a path to the PLLAGND pin through a 100Ω 5% series resistor and a 0.01 μF 10% series capacitor. The ground side of capacitor C1 and the PLLVSS pin should connect to the ground plane at a common point. All PLL loop filter traces should be kept to minimal length and should be wider than signal traces. Inductor L1 is connected to the 5V power supply on both the 82433LX and 82433NX.

Some circuit boards may require filtering the power circuit to the LBX PLL. The circuit shown in Figure 11 will typically enable the LBX PLL to have higher noise immunity than without. Pin PLLVDD is connected to the 5V V_{CC} through a 10Ω 5% resistor. The PLLVDD and PLLVSS pins are bypassed with a 0.01 μF 10% series capacitor.

The high order 82433NX LBX samples A11 at the falling edge of reset to configure the LBX for PLL test mode. When A11 is sampled low, the LBX is in normal operating mode. When A11 is sampled high, the LBX drives the internal HCLK from the PLL on the EOL pin. Note that A11 on the high order LBX is connected to the A27 line on the CPU address bus. This same address line is used to put the PCMC into PLL test mode.

	Mercury 60 MHz	Mercury 66 MHz	Neptune
R1	4.7 KΩ	2.2 KΩ	4.7 KΩ
R2	100Ω	100Ω	100Ω
C2	0.01 μF	0.01 μF	0.01 μF
R3	10Ω	10Ω	10Ω
C1	0.47 μF	0.47 μF	0.47 μF
C1[1]	0.01 μF	0.01 μF	0.01 μF

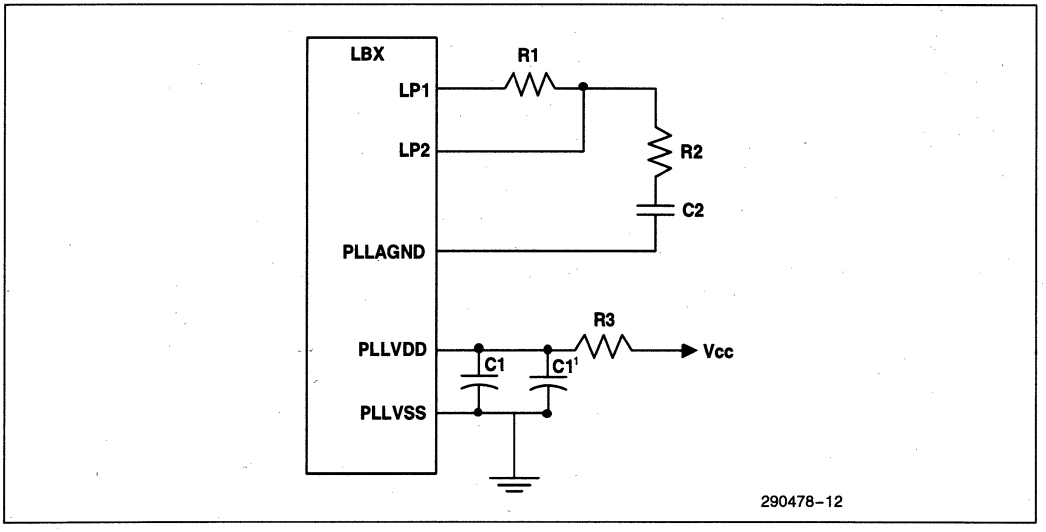


Figure 11. Loop Filter Circuit

3.5 PCI Clock Considerations

There is a 1.25 ns clock skew specification between the PCMC and the LBX that must be adhered to for proper operation of the PCMC/LBX timing. As shown in Figure 12, the PCMC drives PCLKOUT to an external clock driver which supplies copies of PCLK to PCI devices, the LBXs, and back to the PCMC. The skew specification is defined as the difference in timing between the signal that appears at the PCMC PCLKIN input pin and the signal that appears at the LBX PCLK input pin. For both the low order LBX and the high order LBX, the PCLK rising and falling edges must not be more than 1.25 ns apart from the rising and falling edge of the PCMC PCLKIN signal.

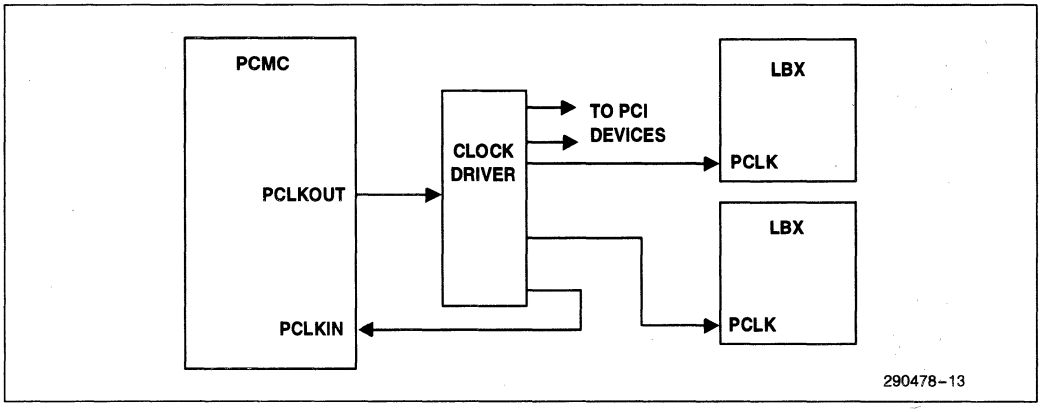


Figure 12. Clock Considerations

4.0 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Table 4 lists stress ratings only. Functional operation at these maximums is not guaranteed. Functional operation conditions are given in Sections 4.2 and 4.3.

Extended exposure to the Absolute Maximum Ratings may affect device reliability.

Case Temperature under Bias .....0°C to +85°C

Storage Temperature .....−40°C to +125°C

Voltage on Any Pin
with Respect to Ground.....−0.3 to V_{CC} + 0.3V

Supply Voltage
with Respect to V_{SS} .....−0.3 to +7.0V

Maximum Power Dissipation: 1.4W (82433LX)

Maximum Total Power Dissipation .1.4W (82433NX)

Maximum Power Dissipation, V_{CC3} .....430 mW

The maximum total power dissipation in the 82433NX on the V_{CC} and V_{CC3} pins is 1.4W. The V_{CC3} pins may draw as much as 430 mW, however, total power will not exceed 1.4W.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2 Thermal Characteristics

The LBX is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the package are given in the following tables.

Table 4. Thermal Resistance

Parameter	Air Flow Rate (Linear Feet per Minute)		
	0	400	600
θ_{JA} (°C/Watt)	51.9	37.1	34.8
θ_{JC} (°C/Watt)		10	

4.3 DC Characteristics

Host Interface Signals
A[15:0](t/s), D[31:0](t/s), HIG[4:0](in), HP[3:0](t/s)

Main Memory (DRAM) Interface Signals
MD[31:0](t/s), MP[3:0](t/s), MIG[2:0](in), MDLE(in)

PCI Interface Signals
AD[15:0](t/s), TRDY#(in), PIG[3:0](in), DRVPCI(in), EOL(t/s), PPOUT(t/s)

Reset and Clock Signals
HCLK(in), PCLK(in), RESET(in), LP1(out), LP2(in), TEST(in)

4.3.1 82433LX LBX DC CHARACTERISTICS

Functional Operating Range: V_{CC} = 4.75 V to 5.25V; T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Typical	Max	Unit	Notes
V_{IL1}	Input Low Voltage	−0.3		0.8	V	1
V_{IH1}	Input High Voltage	2.0		V_{CC} + 0.3	V	1
V_{IL2}	Input Low Voltage	−0.3		0.3 × V_{CC}	V	2
V_{IH2}	Input High Voltage	0.7 × V_{CC}		V_{CC} + 0.3	V	2
V_{OL1}	Output Low Voltage			0.4	V	3
V_{OH1}	Output High Voltage	2.4			V	3
V_{OL2}	Output Low Voltage			0.5	V	4
V_{OH2}	Output High Voltage	V_{CC} − 0.5			V	4
I_{OL1}	Output Low Current			1	mA	5
I_{OH1}	Output High Current	−1			mA	5
I_{OL2}	Output Low Current			3	mA	6
I_{OH2}	Output High Current	−2			mA	6

Functional Operating Range: V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C (Continued)

Symbol	Parameter	Min	Typical	Max	Unit	Notes
I_{OL3}	Output Low Current			3	mA	7
I_{OH3}	Output High Current	−1			mA	7
I_{IH}	Input Leakage Current			+10	μA	
I_{IL}	Input Leakage Current			−10	μA	
C_{IN}	Input Capacitance		4.6		pF	
C_{OUT}	Output Capacitance		4.3		pF	
$C_{I/O}$	I/O Capacitance		4.6		pF	

NOTES:
1. V_{IL1} and V_{IH1} apply to the following signals: AD[15:0], A[15:0], D[31:0], HP[3:0], MD[31:0], MP[3:0], TRDY#, RESET, HCLK, PCLK
2. V_{IL2} and V_{IH2} apply to the following signals: HIG[4:0], PIG[3:0], MIG[2:0], MDLE, DRVPCI
3. V_{OL1} and V_{OH1} apply to the following signals: AD[15:0], A[15:0], D[31:0], HP[3:0], MD[31:0], MP[3:0]
4. V_{OL2} and V_{OH2} apply to the following signals: PPOUT, EOL
5. I_{OL1} and I_{OH1} apply to the following signals: PPOUT, EOL
6. I_{OL2} and I_{OH2} apply to the following signals: AD[15:0]
7. I_{OL3} and I_{OH3} apply to the following signals: A[15:0], D[31:0], HP[3:0], MD[31:0], MP[3:0]

4.3.2 82433NX LBX DC CHARACTERISTICS

Functional Operating Range: V_{CC} = 4.75V to 5.25V; V_{CC3} = 3.135 to 3.465V, T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Typical	Max	Unit	Notes
V_{IL1}	Input Low Voltage	−0.3		0.8	V	1
V_{IH1}	Input High Voltage	2.0		V_{CC} + 0.3	V	1
V_{IL2}	Input Low Voltage	−0.3		0.3 x V_{CC}	V	2
V_{IH2}	Input High Voltage	0.7 x V_{CC}		V_{CC} + 0.3	V	2
V_{IL3}	Input Low Voltage	−0.3		0.8	V	3
V_{IH3}	Input High Voltage	2.0		V_{CC3} + 0.3	V	3
V_{OL1}	Output Low Voltage			0.4	V	4
V_{OH1}	Output High Voltage	2.4			V	4
V_{OL2}	Output Low Voltage			0.5	V	5
V_{OH2}	Output High Voltage	V_{CC} − 0.5			V	5
I_{OL1}	Output Low Current			1	mA	6
I_{OH1}	Output High Current	−1			mA	6
I_{OL2}	Output Low Current			3	mA	7
I_{OH2}	Output High Current	−2			mA	7

Functional Operating Range: V_{CC} = 4.75V to 5.25V; V_{CC3} = 3.135V to 3.465V, T_{CASE} = 0°C to +85°C (Continued)

Symbol	Parameter	Min	Typical	Max	Unit	Notes
I_{OL3}	Output Low Current			3	mA	8
I_{OH3}	Output High Current	−1			mA	8
I_{IH}	Input Leakage Current			+10	μA	
I_{IL}	Input Leakage Current			−10	μA	
C_{IN}	Input Capacitance		4.6		pF	
C_{OUT}	Output Capacitance		4.3		pF	
$C_{I/O}$	I/O Capacitance		4.6		pF	

NOTES:
1. V_{IL1} and V_{IH1} apply to the following signals: AD[15:0], MD[31:0], MP[3:0], TRDY#, RESET, HCLK, PCLK
2. V_{IL2} and V_{IH2} apply to the following signals: HIG[4:0], PIG[3:0], MIG[2:0], MDLE, DRVPCI
3. V_{IL3} and V_{IH3} apply to the following signals: A[15:0], D[31:0], HP[3:0]
4. V_{OL1} and V_{OH1} apply to the following signals: AD[15:0], A[15:0], D[31:0], HP[3:0], MD[31:0], MP[3:0]
5. V_{OL2} and V_{OH2} apply to the following signals: PPOUT, EOL
6. I_{OL1} and I_{OH1} apply to the following signals: PPOUT, EOL
7. I_{OL2} and I_{OH2} apply to the following signals: AD[15:0]
8. I_{OL3} and I_{OH3} apply to the following signals: A[15:0], D[31:0], HP[3:0], MD[31:0], MP[3:0]
9. The output buffers for A[15:0], D[31:0] and HP[3:0] are powered with V_{CC3} and therefore drive 3.3V signal levels.

4.4 82433LX AC Characteristics

The AC specifications given in this section consist of propagation delays, valid delays, input setup requirements, input hold requirements, output float delays, output enable delays, clock high and low times and clock period specifications. Figure 13 through Figure 21 define these specifications. Sections 4.3.1 through 4.3.3 list the AC Specifications.

In Figure 13 through Figure 21 VT = 1.5V for the following signals: MD[31:0], MP[3:0], D[31:0], HP[3:0], A[15:0], AD[15:0], TRDY#, HCLK, PCLK, RESET, TEST.

VT = 2.5V for the following signals: HIG[4:0], PIG[3:0], MIG[2:0], MDLE, DRVPCI, PPOUT, EOL.

4.4.1 HOST AND PCI CLOCK TIMING, 66 MHZ (82433LX)

Functional Operating Range: V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C

Symbol	Parameter	Min	Max	Figure	Notes
t1a	HCLK Period	15	20	18	
t1b	HCLK High Time	5		18	
t1c	HCLK Low Time	5		18	
t1d	HCLK Rise Time		1.5	19	
t1e	HCLK Fall Time		1.5	19	
t1f	HCLK Period Stability		±100		ps[1]
t2a	PCLK Period	30		18	
t2b	PCLK High Time	12		18	
t2c	PCLK Low Time	12		18	
t2d	PCLK Rise Time		3	19	
t2e	PCLK Fall Time		3	19	
t3	HCLK to PCLK Skew	−7.2	5.8	21	

NOTE:
1. Measured on rising edge of adjacent clocks at 1.5 Volts.

4.4.2 COMMAND TIMING, 66 MHZ (82433LX)

Functional Operating Range: V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C

Symbol	Parameter	Min	Max	Figure	Notes
t10a	HIG[4:0] Setup Time to HCLK Rising	5.4		15	
t10b	HIG[4:0] Hold Time from HCLK Rising	0		15	
t11a	MIG[2:0] Setup Time to HCLK Rising	5.4		15	
t11b	MIG[2:0] Hold Time from HCLK Rising	0		15	
t12a	PIG[3:0] Setup Time to PCLK Rising	15.6		15	
t12b	PIG[3:0] Hold Time from PCLK Rising	−1.0		15	
t13a	MDLE Setup Time to HCLK Rising	5.7		15	
t13b	MDLE Hold Time to HCLK Rising	−0.3		15	
t14a	DRVPCI Setup Time to PCLK Rising	6.5		15	
t14b	DRVPCI Hold Time from PCLK Rising	−0.5		15	
t15a	RESET Setup Time to HCLK Rising	3.1		15	
t15b	RESET Hold Time from HCLK Rising	0.3		15	

4.4.3 ADDRESS, DATA, TRDY#, EOL, TEST, TSCON AND PARITY TIMING, 66 MHz (82433LX)

Functional Operating Range: V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C

Symbol	Parameter	Min	Max	Figure	Notes
t20a	AD[15:0] Output Enable Delay from PCLK Rising	2		17	
t20b	AD[15:0] Valid Delay from PCLK Rising	2	11	14	1
t20c	AD[15:0] Setup Time to PCLK Rising	7		15	
t20d	AD[15:0] Hold Time from PCLK Rising	0		15	
t20e	AD[15:0] Float Delay from DRVPCI Falling	2	10	16	
t21a	TRDY# Setup Time to PCLK Rising	7		15	
t21b	TRDY# Hold Time from PCLK Rising	0		15	
t22a	D[31:0], HP[3:0] Output Enable Delay from HCLK Rising	0	7.7	17	2
t22b	D[31:0], HP[3:0] Float Delay from HCLK Rising	3.1	15.5	16	
t22c	D[31:0], HP[3:0] Float Delay from MDLE Rising	2	11.0	16	3
t22d	D[31:0], HP[3:0] Valid Delay from HCLK Rising	0	7.7	14	2
t22e	D[31:0], HP[3:0] Setup Time to HCLK Rising	3.0		15	
t22f	D[31:0], HP[3:0] Hold Time from HCLK Rising	0.3		15	
t23a	HA[15:0] Output Enable Delay from HCLK Rising	0	15.2	17	
t23b	HA[15:0] Float Delay from HCLK Rising	0	15.2	16	
t23c	HA[15:0] Valid Delay from HCLK Rising	0	16	14	7
t23cc	HA[15:0] Valid Delay from HCLK Rising	0	14.5		8
t23d	HA[15:0] Setup Time to HCLK Rising	15		15	4
t23e	HA[15:0] Setup Time to HCLK Rising	4.1		15	5
t23f	HA[15:0] Hold Time from HCLK Rising	0.3		15	
t24a	MD[31:0], MP[3:0] Valid Delay from HCLK Rising	0	12.0	14	6
t24b	MD[31:0], MP[3:0] Setup Time to HCLK Rising	4.0		15	
t24c	MD[31:0], MP[3:0] Hold Time from HCLK Rising	0.4		15	
t25	EOL, PPOUT Valid Delay from PCLK Rising	2.3	17.2	14	2
t26a	All Outputs Float Delay from TSCON Falling	0	30	16	
t26b	All Outputs Enable Delay from TSCON Rising	0	30	17	

NOTES:
1. Min: 0 pF, Max: 50 pF
2. 0 pF
3. When NOPC command sampled on previous rising HCLK on HIG[4:0]
4. CPU to PCI Transfers
5. When ADCPY command is sampled on HIG[4:0]
6. 50 pF
7. When DACPYL or DACPYH commands are sampled on HIG[4:0]
8. Inquire cycle

4.4.4 HOST AND PCI CLOCK TIMING, 60 MHz (82433LX)

Functional Operating Range: V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Max	Figure	Notes
t1a	HCLK Period	16.6	20	18	
t1b	HCLK High Time	5.5		18	
t1c	HCLK Low Time	5.5		18	
t1d	HCLK Rise Time		1.5	19	
t1e	HCLK Fall Time		1.5	19	
t1f	HCLK Period Stability		±100		ps[1]
t2a	PCLK Period	33.33		18	
t2b	PCLK High Time	13		18	
t2c	PCLK Low Time	13		18	
t2d	PCLK Rise Time		3	19	
t2e	PCLK Fall Time		3	19	
t3	PCLK to PCMC PCLKIN: Input to Input Skew	−7.2	5.8	21	

NOTES:
1. Measured on rising edge of adjacent clocks at 1.5 Volts

4.4.5 COMMAND TIMING, 60 MHZ (82433LX)

Functional Operating Range: V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Max	Figure	Notes
t10a	HIG[4:0] Setup Time to HCLK Rising	6.0		15	
t10b	HIG[4:0] Hold Time from HCLK Rising	0		15	
t11a	MIG[2:0] Setup Time to HCLK Rising	6.0		15	
t11b	MIG[2:0] Hold Time from HCLK Rising	0		15	
t12a	PIG[3:0] Setup Time to PCLK Rising	16.0		15	
t12b	PIG[3:0] Hold Time from PCLK Rising	0		15	
t13a	MDLE Setup Time to HCLK Rising	5.9		15	
t13b	MDLE Hold Time to HCLK Rising	−0.3		15	
t14a	DRVPCI Setup Time to PCLK Rising	7.0		15	
t14b	DRVPCI Hold Time from PCLK Rising	−0.5		15	
t15a	RESET Setup Time to HCLK Rising	3.4		15	
t15b	RESET Hold Time from HCLK Rising	0.4		15	

4.4.6 ADDRESS, DATA, TRDY#, EOL, TEST, TSCON AND PARITY TIMING, 60 MHz (82433LX)

Functional Operating Range: V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Max	Figure	Notes
t20a	AD[15:0] Output Enable Delay from PCLK Rising	2		17	
t20b	AD[15:0] Valid Delay from PCLK Rising	2	11	14	1
t20c	AD[15:0] Setup Time to PCLK Rising	7		15	
t20d	AD[15:0] Hold Time from PCLK Rising	0		15	
t20e	AD[15:0] Float Delay from DRVPCI Falling	2	10	16	
t21a	TRDY# Setup Time to PCLK Rising	7		15	
t21b	TRDY# Hold Time from PCLK Rising	0		15	
t22a	D[31:0], HP[3:0] Output Enable Delay from HCLK Rising	0	7.9	17	2
t22b	D[31:0], HP[3:0] Float Delay from HCLK Rising	3.1	15.5	16	
t22c	D[31:0], HP[3:0] Float Delay from MDLE Rising	2	11.0	16	3
t22d	D[31:0], HP[3:0] Valid Delay from HCLK Rising	0	7.8	14	2
t22e	D[31:0],HP[3:0] Setup Time to HCLK Rising	3.4		15	
t22f	D[31:0], HP[3:0] Hold Time from HCLK Rising	0.3		15	
t23a	HA[15:0] Output Enable Delay from HCLK Rising	0	15.2	17	
t23b	HA[15:0] Float Delay from HCLK Rising	0	15.2	16	
t23c	HA[15:0] Valid Delay from HCLK Rising	0	18.5	14	7
t23cc	HA[15:0] Valid Delay from HCLK Rising	0	15.5		8
t23d	HA[15:0] Setup Time to HCLK Rising	15.0		15	4
t23e	HA[15:0] Setup Time to HCLK Rising	4.1		15	5
t23f	HA[15:0] Hold Time from HCLK Rising	0.3		15	
t24a	MD[31:0], MP[3:0] Valid Delay from HCLK Rising	0	12.0	14	6
t24b	MD[31:0], MP[3:0] Setup Time to HCLK Rising	4.4		15	
t24c	MD[31:0], MP[3:0] Hold Time from HCLK Rising	1.0		15	
t25	EOL, PPOUT Valid Delay from PCLK Rising	2.3	17.2	14	2
t26a	All Outputs Float Delay from TSCON Falling	0	30	16	
t26b	All Outputs Enable Delay from TSCON Rising	0	30	17	

NOTES:
1. Min: 0 pF, Max: 50 pF
2. 0 pF
3. When NOPC command sampled on previous rising HCLK on HIG[4:0]
4. CPU to PCI Transfers
5. When ADCPY command is sampled on HIG[4:0]
6. 50 pF
7. When DACPYL or DACPYH commands are sampled on HIG[4:0]
8. Inquire cycle

4.4.7 TEST TIMING (82433LX)

Functional Operating Range: V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Max	Figure	Notes
t30	All Test Signals Setup Time to HCLK/PCLK Rising	10.0			In PLL Bypass Mode
t31	All Test Signals Hold Time to HCLK/PCLK Rising	12.0			In PLL Bypass Mode
t32	Test Setup Time to HCLK/PCLK Rising	15.0		15	
t33	Test Hold Time to HCLK/PCLK Rising	5.0		15	
t34	PPOUT Valid Delay from PCLK Rising	0.0	500	15	In PLL Bypass Mode

4.5 82433NX AC Characteristics

The AC specifications given in this section consist of propagation delays, valid delays, input setup requirements, input hold requirements, output float delays, output enable delays, clock high and low times and clock period specifications. Figure 13 through Figure 21 define these specifications. Section 4.5 lists the AC Specifications.

In Figure 13 through Figure 21 VT = 1.5V for the following signals: MD[31:0], MP[3:0], D[31:0], HP[3:0], A[15:0], AD[15:0], TRDY#, HCLK, PCLK, RESET, TEST.

VT = 2.5V for the following signals: HIG[4:0], PIG[3:0], MIG[2:0], MDLE, DRVPCI, PPOUT, EOL.

4.5.1 HOST AND PCI CLOCK TIMING, (82433NX)

Functional Operating Range: V_{CC} = 4.75V to 5.25V; V_{CC3} = 3.135V to 3.465V, T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Max	Figure	Notes
t1a	HCLK Period	15	20	18	
t1b	HCLK High Time	5		18	
t1c	HCLK Low Time	5		18	
t1d	HCLK Rise Time		1.5	19	
t1e	HCLK Fall Time		1.5	19	
t1f	HCLK Period Stability		±100		ps[1]
t2a	PCLK Period	30		18	
t2b	PCLK High Time	12		18	
t2c	PCLK Low Time	12		18	
t2d	PCLK Rise Time		3	19	
t2e	PCLK Fall Time		3	19	
t3	HCLK to PCLK Skew	−7.2	5.8	21	

NOTE:
1. Measured on rising edge of adjacent clocks at 1.5 Volts.

4.5.2 COMMAND TIMING, (82433NX)

Functional Operating Range: V_{CC} = 4.75V to 5.25V; V_{CC3} = 3.135V to 3.465V, T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Max	Figure	Notes
t10a	HIG[4:0] Setup Time to HCLK Rising	5.5		15	
t10b	HIG[4:0] Hold Time from HCLK Rising	0		15	
t11a	MIG[2:0] Setup Time to HCLK Rising	5.5		15	
t11b	MIG[2:0] Hold Time from HCLK Rising	0		15	
t12a	PIG[3:0] Setup Time to PCLK Rising	14.5		15	
t12b	PIG[3:0] Hold Time from PCLK Rising	0.0		15	
t13a	MDLE Setup Time to HCLK Rising	5.5		15	
t13b	MDLE Hold Time to HCLK Rising	−0.3		15	
t14a	DRVPCI Setup Time to PCLK Rising	7.0		15	
t14b	DRVPCI Hold Time from PCLK Rising	−0.5		15	
t15a	RESET Setup Time to HCLK Rising	3.4		15	
t15b	RESET Hold Time from HCLK Rising	0.4		15	

4.5.3 ADDRESS, DATA, TRDY#, EOL, TEST, TSCON AND PARITY TIMING, (82433NX)

Functional Operating Range: V_{CC} = 4.75V to 5.25V; V_{CC3} = 3.135V to 3.465V, T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Max	Figure	Notes
t20a	AD[15:0] Output Enable Delay from PCLK Rising	2		17	
t20b	AD[15:0] Valid Delay from PCLK Rising	2	11	14	1
t20c	AD[15:0] Setup Time to PCLK Rising	7		15	
t20d	AD[15:0] Hold Time from PCLK Rising	0		15	
t20e	AD[15:0] Float Delay from DRVPCI Falling	2	10	16	
t21a	TRDY# Setup Time to PCLK Rising	7		15	
t21b	TRDY# Hold Time from PCLK Rising	0		15	
t22a	D[31:0], HP[3:0] Output Enable Delay from HCLK Rising	0	7.5	17	2
t22b	D[31:0], HP[3:0] Float Delay from HCLK Rising	3.1	15.5	16	
t22c	D[31:0], HP[3:0] Float Delay from MDLE Rising	2	9.5	16	3
t22d	D[31:0], HP[3:0] Valid Delay from HCLK Rising	0	7.5	14	2
t22e	D[31:0],HP[3:0] Setup Time to HCLK Rising	3.1		15	
t22f	D[31:0], HP[3:0] Hold Time from HCLK Rising	0.3		15	

Functional Operating Range: V_{CC} = 4.75V to 5V; V_{CC3} = 3.135V to 3.465V, T_{CASE} = 0°C to +85°C (Continued)

Symbol	Parameter	Min	Max	Figure	Notes
t23a	HA[15:0] Output Enable Delay from HCLK Rising	0	13.5	17	
t23b	HA[15:0] Float Delay from HCLK Rising	0	13.5	16	
t23c	HA[15:0] Valid Delay from HCLK Rising	0	17.5	14	7
t23cc	HA[15:0] Valid Delay from HCLK Rising	0	13.5		8
t23d	HA[15:0] Setup Time to HCLK Rising	15		15	4
t23e	HA[15:0] Setup Time to HCLK Rising	4.2		15	5
t23f	HA[15:0] Hold Time from HCLK Rising	0.3		15	
t24a	MD[31:0], MP[3:0] Valid Delay from HCLK Rising	0	12.0	14	6
t24b	MD[31:0], MP[3:0] Setup Time to HCLK Rising	4.4		15	
t24c	MD[31:0], MP[3:0] Hold Time from HCLK Rising	1.0		15	
t25	EOL, PPOUT Valid Delay from PCLK Rising	2.3	17.2	14	2
t26a	All Outputs Float Delay from TSCON Falling	0	30	16	
t26b	All Outputs Enable Delay from TSCON Rising	0	30	17	

NOTE:
1. Min: 0 pF, Max: 50 pF
2. 0 pF
3. When NOPC command sampled on previous rising HCLK on HIG[4:0]
4. CPU to PCI Transfers
5. When ADCPY command is sampled on HIG[4:0]
6. 50 pF
7. When DACPYL or DACPYH commands are sampled on HIG[4:0]
8. Inquire cycle

4.5.4 TEST TIMING (82433NX)

Functional Operating Range: V_{CC} = 4.75V to 5.25V; V_{CC3} = 3.135V to 3.465V, T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Max	Figure	Notes
t30	All Test Signals Setup Time to HCLK/PCLK Rising	10.0			In PLL Bypass Mode
t31	All Test Signals Hold Time to HCLK/PCLK Rising	12.0			In PLL Bypass Mode
t32	Test Setup Time to HCLK/PCLK Rising	15.0		15	
t33	Test Hold Time to HCLK/PCLK Rising	5.0		15	
t34	PPOUT Valid Delay from PCLK Rising	0.0	500	15	In PLL Bypass Mode

4.5.5 TIMING DIAGRAMS

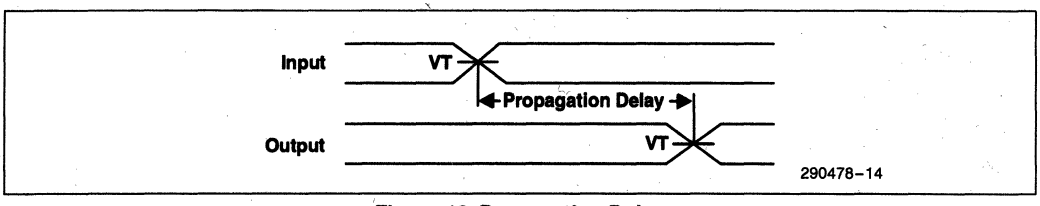


Figure 13. Propagation Delay

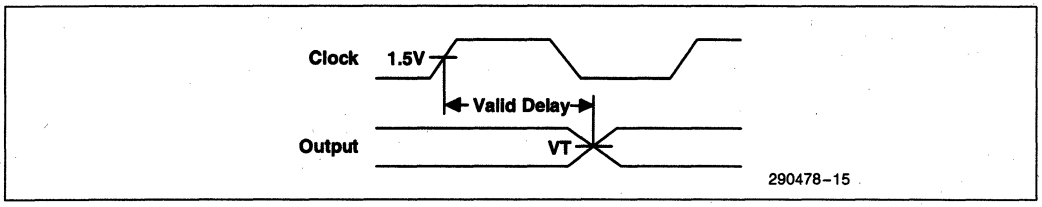


Figure 14. Valid Delay from Rising Clock Edge

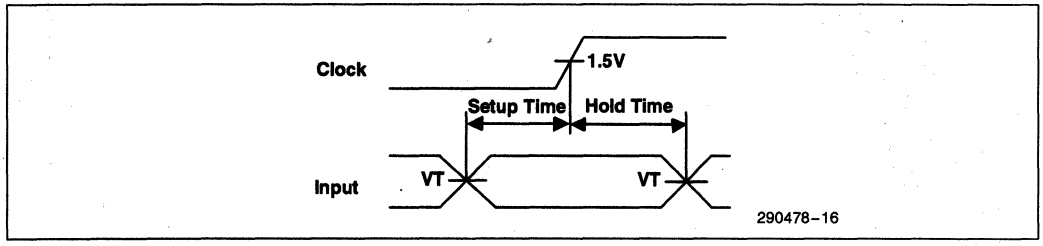


Figure 15. Setup and Hold Times

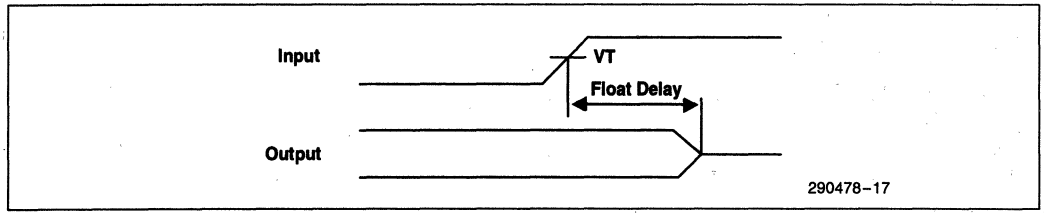


Figure 16. Float Delay

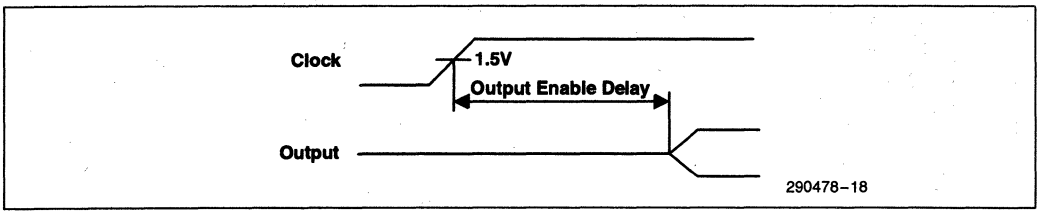


Figure 17. Output Enable Delay

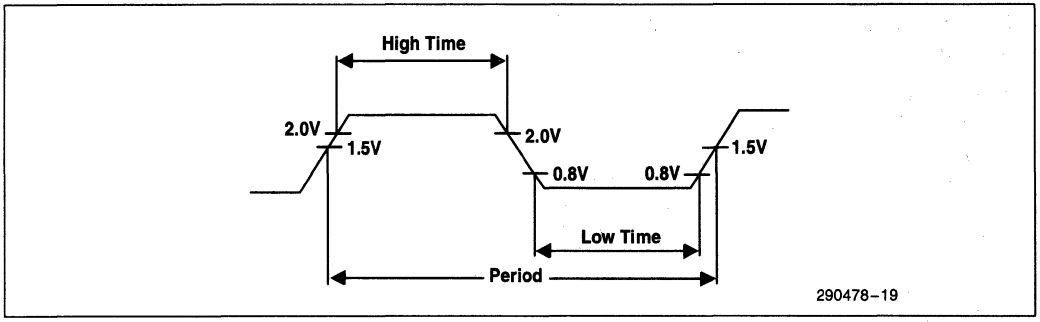


Figure 18. Clock High and Low Times and Period

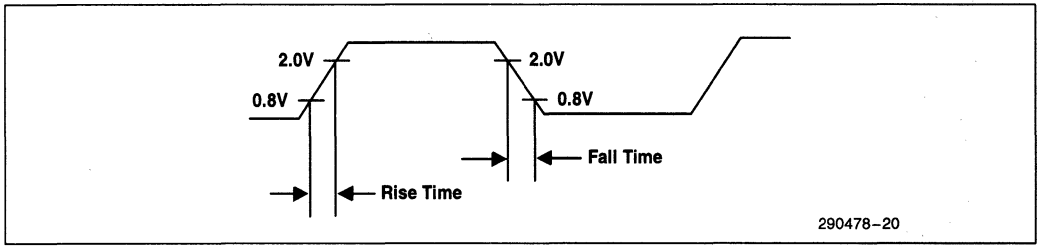


Figure 19. Clock Rise and Fall Times

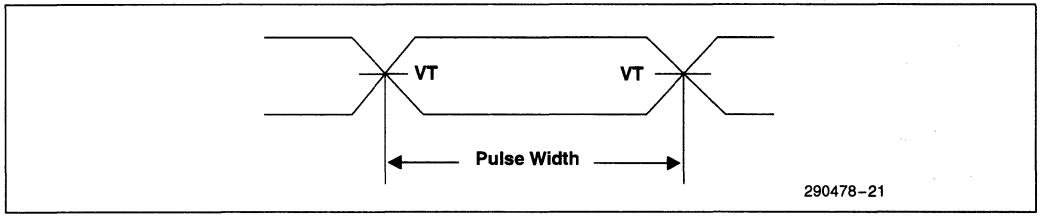


Figure 20. Pulse Width

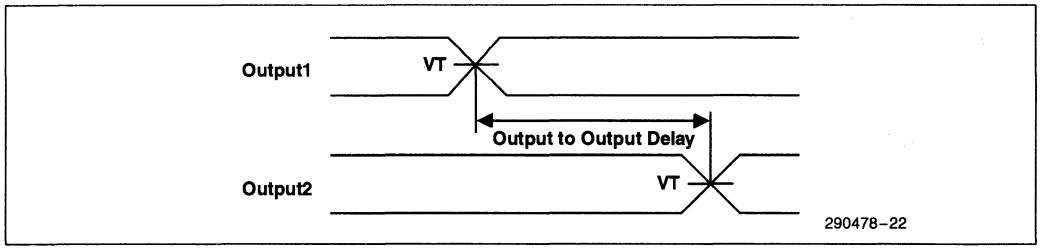


Figure 21. Output to Output Delay

5.0 PINOUT AND PACKAGE INFORMATION

5.1 Pin Assignment

Pins 1, 22, 41, 61, and 150 are VDD3 pins on the 82433NX. These pins must be connected to the 3.3V power supply. All other VDD pins on the 82433NX must be connected to the 5V power supply.

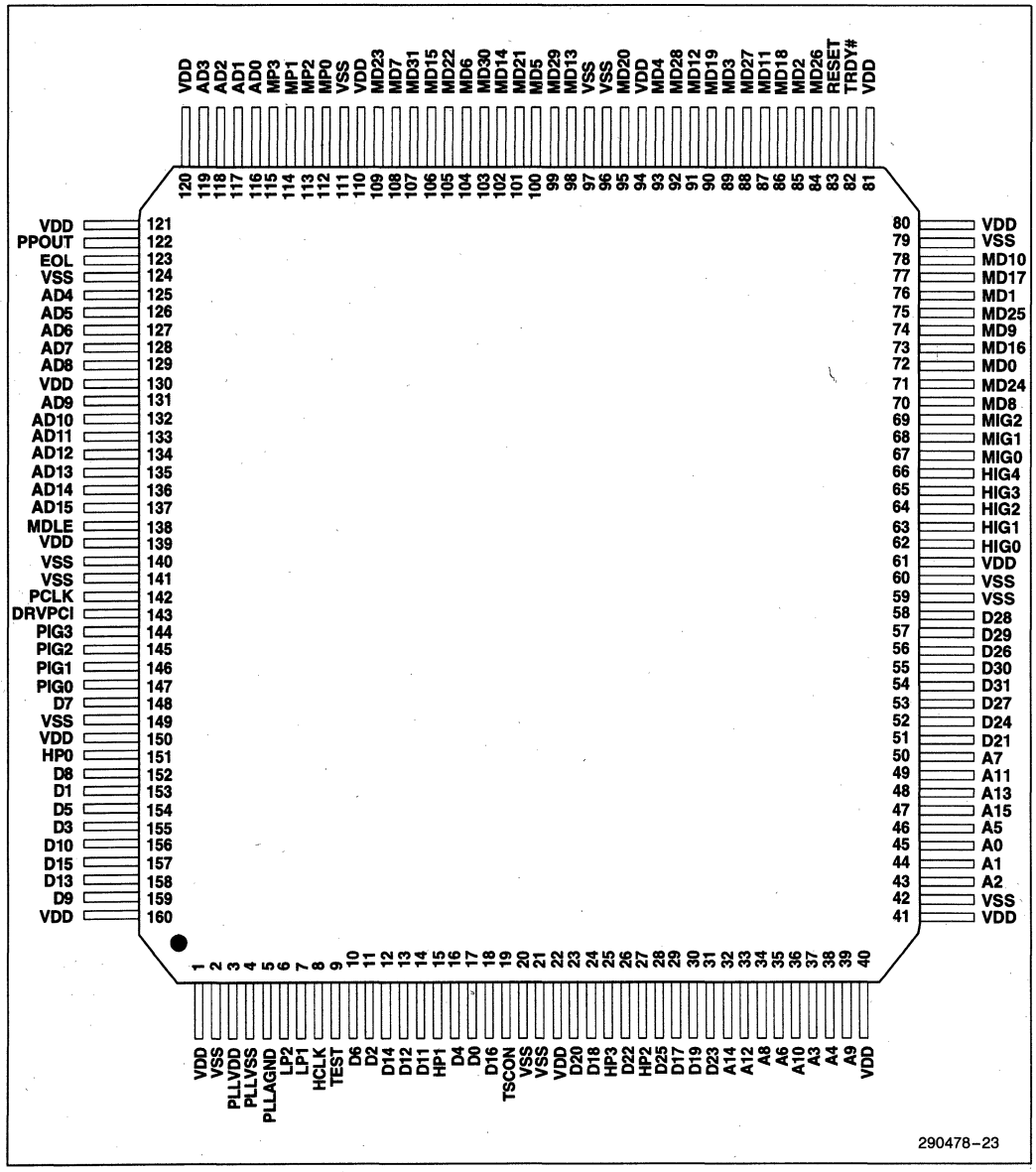


Figure 22. 82433LX and 82433NX Pin Assignment

Table 5. 82433LX and 82433NX Numerical Pin Assignment

Pin Name	Pin #	Type
V_{DD} (82433LX) V_{DD3} (82433NX)	1	V
V_{SS}	2	V
$PLLV_{DD}$	3	V
$PLLV_{SS}$	4	V
PLLAGND	5	V
LP2	6	in
LP1	7	out
HCLK	8	in
TEST	9	in
D6	10	t/s
D2	11	t/s
D14	12	t/s
D12	13	t/s
D11	14	t/s
HP1	15	t/s
D4	16	t/s
D0	17	t/s
D16	18	t/s
TSCON	19	in
V_{SS}	20	V
V_{SS}	21	V
V_{DD} (82433LX V_{DD3} (82433NX)	22	V
D20	23	t/s
D18	24	t/s
HP3	25	t/s

Pin Name	Pin #	Type
D22	26	t/s
HP2	27	t/s
D25	28	t/s
D17	29	t/s
D19	30	t/s
D23	31	t/s
A14	32	t/s
A12	33	t/s
A8	34	t/s
A6	35	t/s
A10	36	t/s
A3	37	t/s
A4	38	t/s
A9	39	t/s
V_{DD}	40	V
V_{DD} (82433LX) $V_{DD}3$ (82433NX)	41	V
V_{SS}	42	V
A2	43	t/s
A1	44	t/s
A0	45	t/s
A5	46	t/s
A15	47	t/s
A13	48	t/s
A11	49	t/s
A7	50	t/s

Pin Name	Pin #	Type
D21	51	t/s
D24	52	t/s
D27	53	t/s
D31	54	t/s
D30	55	t/s
D26	56	t/s
D29	57	t/s
D28	58	t/s
V_{SS}	59	V
V_{SS}	60	V
V_{DD} (82433LX) V_{DD3} (82433NX)	61	V
HIG0	62	in
HIG1	63	in
HIG2	64	in
HIG3	65	in
HIG4	66	in
MIG0	67	in
MIG1	68	in
MIG2	69	in
MD8	70	t/s
MD24	71	t/s
MD0	72	t/s
MD16	73	t/s
MD9	74	t/s
MD25	75	t/s

Table 5. 82433LX and 82433NX Numerical Pin Assignment (Continued)

Pin Name	Pin #	Type
MD1	76	t/s
MD17	77	t/s
MD10	78	t/s
V_{SS}	79	V
V_{DD}	80	V
V_{DD}	81	V
TRDY#	82	in
RESET	83	in
MD26	84	t/s
MD2	85	t/s
MD18	86	t/s
MD11	87	t/s
MD27	88	t/s
MD3	89	t/s
MD19	90	t/s
MD12	91	t/s
MD28	92	t/s
MD4	93	t/s
V_{DD}	94	V
MD20	95	t/s
V_{SS}	96	V
V_{SS}	97	V
MD13	98	t/s
MD29	99	t/s
MD5	100	t/s
MD21	101	t/s
MD14	102	t/s
MD30	103	t/s
MD6	104	t/s

Pin Name	Pin #	Type
MD22	105	t/s
MD15	106	t/s
MD31	107	t/s
MD7	108	t/s
MD23	109	t/s
V_{DD}	110	V
V_{SS}	111	V
MP0	112	t/s
MP2	113	t/s
MP1	114	t/s
MP3	115	t/s
AD0	116	t/s
AD1	117	t/s
AD2	118	t/s
AD3	119	t/s
V_{DD}	120	V
V_{DD}	121	V
PPOUT	122	t/s
EOL	123	t/s
V_{SS}	124	V
AD4	125	t/s
AD5	126	t/s
AD6	127	t/s
AD7	128	t/s
AD8	129	t/s
V_{DD}	130	V
AD9	131	t/s
AD10	132	t/s

Pin Name	Pin #	Type
AD11	133	t/s
AD12	134	t/s
AD13	135	t/s
AD14	136	t/s
AD15	137	t/s
MDLE	138	in
V_{DD}	139	V
V_{SS}	140	V
V_{SS}	141	V
PCLK	142	in
DRVPCI	143	in
PIG3	144	in
PIG2	145	in
PIG1	146	in
PIG0	147	in
D7	148	t/s
V_{SS}	149	V
V_{DD} (82433LX) $V_{DD}3$ (82433NX)	150	V
HP0	151	t/s
D8	152	t/s
D1	153	t/s
D5	154	t/s
D3	155	t/s
D10	156	t/s
D15	157	t/s
D13	158	t/s
D9	159	t/s
V_{DD}	160	V

Table 6. 82433LX and 82433NX Alphabetical Pin Assignment List

Pin Name	Pin #	Type
A0	45	t/s
A1	44	t/s
A2	43	t/s
A3	37	t/s
A4	38	t/s
A5	46	t/s
A6	35	t/s
A7	50	t/s
A8	34	t/s
A9	39	t/s
A10	36	t/s
A11	49	t/s
A12	33	t/s
A13	48	t/s
A14	32	t/s
A15	47	t/s
AD0	116	t/s
AD1	117	t/s
AD2	118	t/s
AD3	119	t/s
AD4	125	t/s
AD5	126	t/s
AD6	127	t/s
AD7	128	t/s
AD8	129	t/s
AD9	131	t/s
AD10	132	t/s
AD11	133	t/s
AD12	134	t/s

Pin Name	Pin #	Type
AD13	135	t/s
AD14	136	t/s
AD15	137	t/s
D0	17	t/s
D1	153	t/s
D2	11	t/s
D3	155	t/s
D4	16	t/s
D5	154	t/s
D6	10	t/s
D7	148	t/s
D8	152	t/s
D9	159	t/s
D10	156	t/s
D11	14	t/s
D12	13	t/s
D13	158	t/s
D14	12	t/s
D15	157	t/s
D16	18	t/s
D17	29	t/s
D18	24	t/s
D19	30	t/s
D20	23	t/s
D21	51	t/s
D22	26	t/s
D23	31	t/s
D24	52	t/s
D25	28	t/s

Pin Name	Pin #	Type
D26	56	t/s
D27	53	t/s
D28	58	t/s
D29	57	t/s
D30	55	t/s
D31	54	t/s
DRVPCI	143	in
EOL	123	t/s
HCLK	8	in
HIG0	62	in
HIG1	63	in
HIG2	64	in
HIG3	65	in
HIG4	66	in
HP0	151	t/s
HP1	15	t/s
HP2	27	t/s
HP3	25	t/s
LP1	7	out
LP2	6	in
MD0	72	t/s
MD1	76	t/s
MD2	85	t/s
MD3	89	t/s
MD4	93	t/s
MD5	100	t/s
MD6	104	t/s
MD7	108	t/s
MD8	70	t/s

Table 6. 82433LX and 82433NX Alphabetical Pin Assignment List (Continued)

Pin Name	Pin #	Type
MD9	74	t/s
MD10	78	t/s
MD11	87	t/s
MD12	91	t/s
MD13	98	t/s
MD14	102	t/s
MD15	106	t/s
MD16	73	t/s
MD17	77	t/s
MD18	86	t/s
MD19	90	t/s
MD20	95	t/s
MD21	101	t/s
MD22	105	t/s
MD23	109	t/s
MD24	71	t/s
MD25	75	t/s
MD26	84	t/s
MD27	88	t/s
MD28	92	t/s
MD29	99	t/s
MD30	103	t/s
MD31	107	t/s
MDLE	138	in
MIG0	67	in

Pin Name	Pin #	Type
MIG1	68	in
MIG2	69	in
MP0	112	t/s
MP1	114	t/s
MP2	113	t/s
MP3	115	t/s
PCLK	142	in
PIG0	147	in
PIG1	146	in
PIG2	145	in
PIG3	144	in
PLLAGND	5	V
$PLLV_{DD}$	3	V
$PLLV_{SS}$	4	V
PPOUT	122	t/s
RESET	83	in
TEST	9	in
TRDY	82	in
TSCON	19	in
V_{DD} (82433LX) $V_{DD}3$ (82433NX)	1	V
V_{DD} (82433LX) $V_{DD}3$ (82433NX)	22	V
V_{DD}	40	V
V_{DD} (82433LX) $V_{DD}3$ (82433NX)	41	V
V_{DD} (82433LX) $V_{DD}3$ (82433NX)	61	V

Pin Name	Pin #	Type
V_{DD}	80	V
V_{DD}	81	V
V_{DD}	94	V
V_{DD}	110	V
V_{DD}	120	V
V_{DD}	121	V
V_{DD}	130	V
V_{DD}	139	V
V_{DD} (82433LX) $V_{DD}3$ (82433NX)	150	V
V_{DD}	160	V
V_{SS}	2	V
V_{SS}	20	V
V_{SS}	21	V
V_{SS}	42	V
V_{SS}	59	V
V_{SS}	60	V
V_{SS}	79	V
V_{SS}	96	V
V_{SS}	97	V
V_{SS}	111	V
V_{SS}	124	V
V_{SS}	140	V
V_{SS}	141	V
V_{SS}	149	V

5.2 Package Information

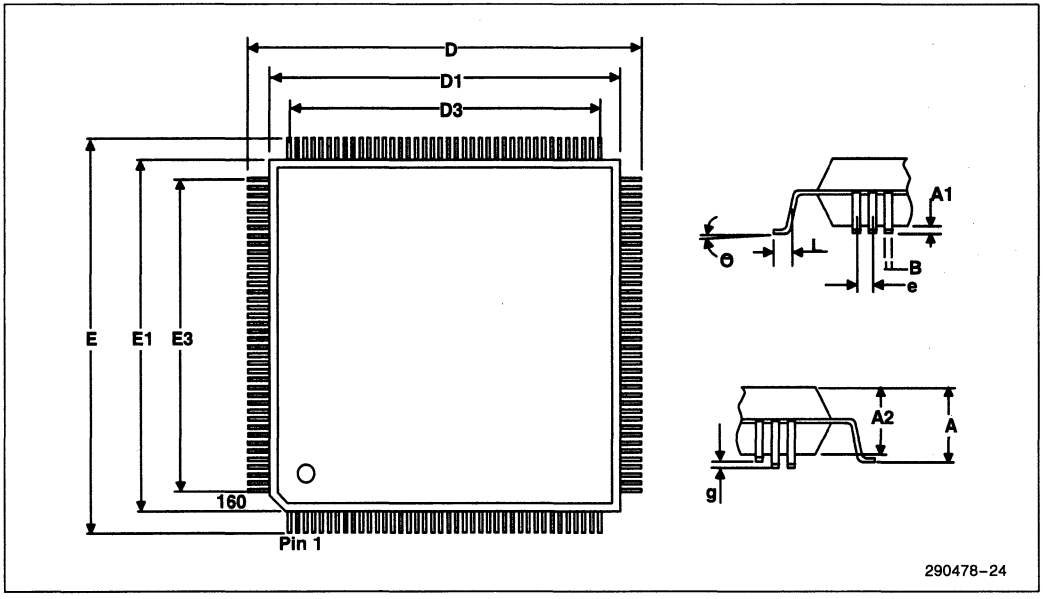


Figure 23. 82433LX and 82433NX 160-Pin QFP Package

Table 7. 160-Pin QFP Package Values

Symbol	Min Value (mm)	Max Value (mm)
A		4.45
A1	0.25	0.65
A2	3.30	3.80
B	0.20	0.40
D	31.00	32.40
D1	27.80	28.20
D3		25.55

Symbol	Min Value (mm)	Max Value (mm)
E	31.60	32.40
E1	27.80	28.20
E3		25.55
e		0.65
L	0.60	1.00
θ	0°	10°
g		0.1

6.0 TESTABILITY

The TSCON pin may be used to help test circuits surrounding the LBX. During normal operations, the TSCON pin must be tied to VCC or connected to VCC through a pull-up resistor. All LBX outputs are tri-stated when the TSCON pin is held low or grounded.

6.1 NAND Tree

A NAND tree is provided in the LBX for Automated Test Equipment (ATE) board level testing. The NAND tree allows the tester to set the connectivity of each of the LBX signal pins.

The following steps must be taken to put the LBX into PLL bypass mode and enable the NAND tree. First, to enable PLL bypass mode, drive RESET inactive, TEST active, and the DCPWA command (0100) on the PIG[3:0] lines. Then drive PCLK from low to high. DRVPCI must be held low on all rising edges of PCLK during testing in order to ensure that the LBX does not drive the AD[15:0] lines. The host and memory buses are tri-stated by driving NOPM (000) and NOPC (00000) on the MIG[2:0] and HIG[4:0] lines and driving two rising edges on HCLK. A rising edge on PCLK with RESET high will cause the LBXs to exit PLL bypass mode. TEST must remain high throughout the use of the NAND tree. The combination of TEST and DRVPCI high with a rising edge of PCLK must be avoided. TSCON must be driven high throughout testing since driving it low would tri-state the output of the NAND tree. A 10 ns hold time is required on all inputs sampled by PCLK or HCLK when in PLL bypass mode.

6.1.1 TEST VECTOR TABLE

The following test vectors can be applied to the 82433LX and 82433NX to put it into PLL bypass mode and to enable NAND tree testing.

6.1.2 NAND TREE TABLE

Table 9 shows the sequence of the NAND tree in the 82433LX and 82433NX. Non-inverting inputs are driven directly into the input of a NAND gate in the tree. Inverting inputs are driven into an inverter before going into the NAND tree. The output of the NAND tree is driven on the PPOUT pin.

Table 8. Test Vectors to put LBX Into PLL Bypass and Enable NAND Tree Testing

LBX Pin/Vector#	1	2	3	4	5	6	7	8	9	10	11
PCLK	0	1	0	0	1	1	1	1	1	1	1
PIG[3:0]	0h	0h	0h	4h	4h	4h	4h	4h	4h	4h	4h
RESET	1	1	1	0	0	0	1	1	1	1	1
HCLK	0	0	0	0	0	0	0	1	0	1	0
MIG[2:0]	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
HIG[4:0]	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h	0h
TEST	1	1	1	1	1	1	1	1	1	1	1
DRVPCI	0	0	0	0	0	0	0	0	0	0	0

Table 9. NAND Tree Sequence

Order	Pin #	Signal	Non-Inverting
1	10	D6	Y
2	11	D2	Y
3	12	D14	Y
4	13	D12	Y
5	14	D11	Y
6	15	HP1	Y
7	16	D4	Y
8	17	D0	Y
9	18	D16	Y
10	23	D20	Y
11	24	D18	Y
12	25	HP3	Y
13	26	D22	Y
14	27	HP2	Y
15	28	D25	Y
16	29	D17	Y
17	30	D19	Y
18	31	D23	Y
19	32	A14	Y
20	33	A12	Y
21	34	A8	Y
22	35	A6	Y
23	36	A10	Y
24	37	A3	Y
25	38	A4	Y
26	39	A9	Y
27	43	A2	Y
28	44	A1	Y
29	45	A0	Y
30	46	A5	Y
31	47	A15	Y
32	48	A13	Y
33	49	A11	Y
34	50	A7	Y
35	51	D21	Y
36	52	D24	Y
37	53	D27	Y
38	54	D31	Y
39	55	D30	Y
40	56	D26	Y
41	57	D29	Y
42	58	D28	Y
43	62	HIG0	Y
44	63	HIG1	Y
45	64	HIG2	Y
46	65	HIG3	Y
47	66	HIG4	Y
48	67	MIG0	N
49	68	MIG1	N
50	69	MIG2	N
51	70	MD8	N
52	71	MD24	N
53	72	MD0	N
54	73	MD16	N
55	74	MD9	N
56	75	MD25	N
57	76	MD1	N
58	77	MD17	N
59	78	MD10	N
60	82	TRDY#	Y
61	83	RESET	N
62	84	MD26	N
63	85	MD2	N
64	86	MD18	N
65	87	MD11	N
66	88	MD27	N
67	89	MD3	N
68	90	MD19	N
69	91	MD12	N
70	92	MD28	N
71	93	MD4	N
72	95	MD20	N
73	98	MD13	N
74	99	MD29	N
75	100	MD5	N
76	101	MD21	N
77	102	MD14	N
78	103	MD30	N

Table 9. NAND Tree Sequence (Continued)

Order	Pin #	Signal	Non-Inverting
79	104	MD6	N
80	105	MD22	N
81	106	MD15	N
82	107	MD31	N
83	108	MD7	N
84	109	MD23	N
85	112	MP0	N
86	113	MP2	N
87	114	MP1	N
88	115	MP3	N
89	116	AD0	Y
90	117	AD1	Y
91	118	AD2	Y
82	119	AD3	Y
93	123	EOL	Y
94	125	AD4	Y
95	126	AD5	Y
96	127	AD6	Y
97	128	AD7	Y
98	129	AD8	Y
99	131	AD9	Y
100	132	AD10	Y
101	133	AD11	Y
102	134	AD12	Y
103	135	AD13	Y
104	136	AD14	Y
105	137	AD15	Y
106	138	MDLE	Y
107	143	DRVPCI	N
108	144	PIG3	N
109	145	PIG2	N
110	146	PIG1	N
111	147	PIG0	N
112	148	D7	Y
113	151	HP0	Y
114	152	D8	Y
115	153	D1	Y
116	154	D5	Y
117	155	D3	Y
118	156	D10	Y
119	157	D15	Y
120	158	D13	Y
121	159	D9	Y

6.2 PLL Test Mode

The high order 82433NX LBX samples A11 at the falling edge of reset to configure the LBX for PLL test mode. When A11 is sampled low, the LBX is in normal operating mode. When A11 is sampled high, the LBX drives the internal HCLK from the PLL on the EOL pin.

82434LX/82434NX PCI, CACHE AND MEMORY CONTROLLER (PCMC)

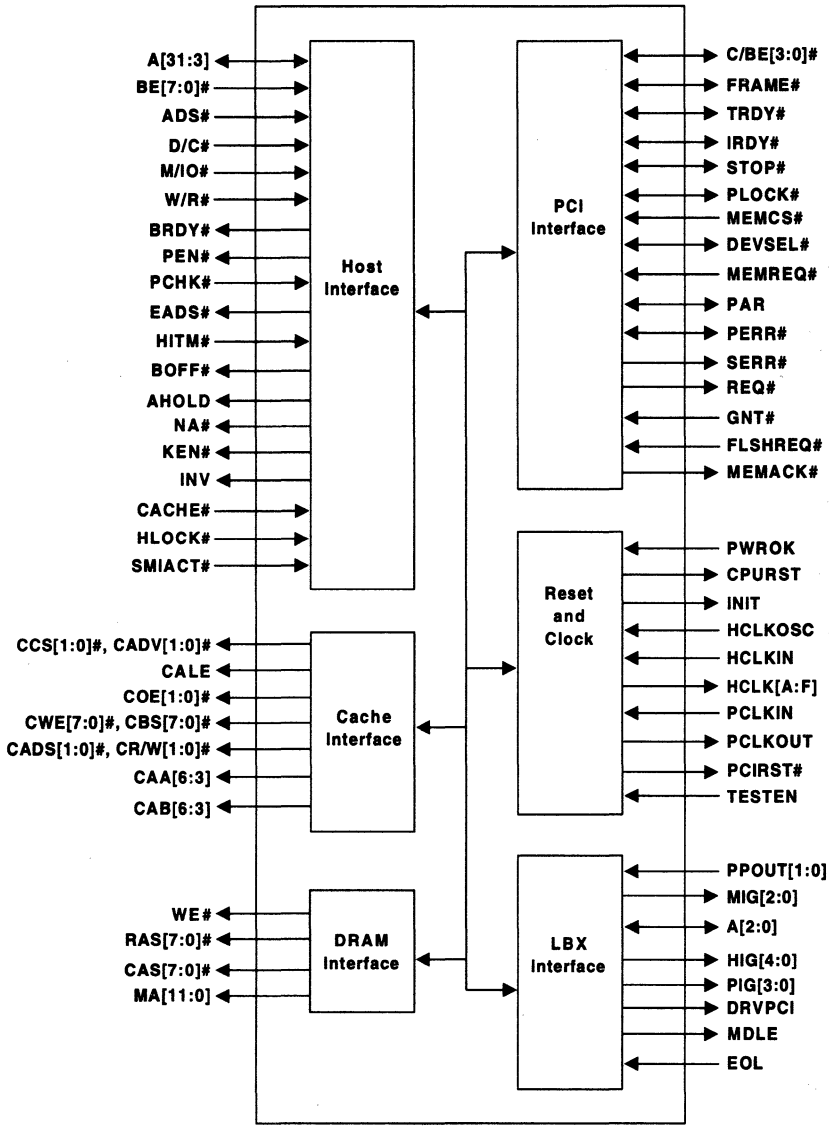
- Supports the Pentium™ Processor at iCOMP™ Index 510\60 MHz and iCOMP Index 567\66 MHz
- Supports the Pentium Processor at iCOMP Index 735\90 MHz, iCOMP Index 815\100 MHz, and iCOMP Index 610\75 MHz
- Supports Pipelined Addressing Capability of the Pentium Processor
- The 82430NX Drives 3.3V Signal Levels on the CPU and Cache Interfaces
- High Performance CPU/PCI/Memory Interfaces via Posted Write and Read Prefetch Buffers
- Fully Synchronous PCI Interface with Full Bus Master Capability
- Supports the Pentium Processor Internal Cache in Either Write-Through or Write-Back Mode
- Programmable Attribute Map of DOS and BIOS Regions for System Flexibility
- Integrated Low Skew Clock Driver for Distributing Host Clock
- Integrated Second Level Cache Controller
  - Integrated Cache Tag RAM
  - Write-Through and Write-Back Cache Modes for the 82434LX
  - Write-Back for the 82434NX
  - 82434NX Supports Low-Power Cache Standby
  - Direct Mapped Organization
  - Supports Standard and Burst SRAMs
  - 256-KByte and 512-KByte Sizes
  - Cache Hit Cycle of 3-1-1-1 on Reads and Writes Using Burst SRAMs
  - Cache Hit Cycle of 3-2-2-2 on Reads and 4-2-2-2 on Writes Using Standard SRAMs
- Integrated DRAM Controller
  - Supports 2 MBytes to 192 MBytes of Cacheable Main Memory for the 82434LX
  - Supports 2 MBytes to 512 MBytes of Cacheable Main Memory for the 82434NX
  - Supports DRAM Access Times of 70 ns and 60 ns
  - CPU Writes Posted to DRAM 4-1-1-1
  - Refresh Cycles Decoupled from ISA Refresh to Reduce the DRAM Access Latency
  - Six RAS# Lines (82434LX)
  - Eight RAS# Lines (82434NX)
  - Refresh by RAS#-Only, or CAS-Before-RAS#, in Single or Burst of Four
- Host/PCI Bridge
  - Translates CPU Cycles into PCI Bus Cycles
  - Translates Back-to-Back Sequential CPU Memory Writes into PCI Burst Cycles
  - Burst Mode Writes to PCI in Zero PCI Wait-States (i.e. Data Transfer Every Cycle)
  - Full Concurrency Between CPU-to-Main Memory and PCI-to-PCI Transactions
  - Full Concurrency Between CPU-to-Second Level Cache and PCI-to-Main Memory Transactions
  - Same Cache and Memory System Logic Design for ISA and EISA Systems
  - Cache Snoop Filter Ensures Data Consistency for PCI-to-Main Memory Transactions
- 208-Pin QFP Package

*Other brands and names are the property of their respective owners.

December 1994
Order Number: 290479-004

This document describes both the 82434LX and 82434NX. Unshaded areas describe the 82434LX. Shaded areas, like this one, describe 82434NX operations that differ from the 82434LX.

The 82434LX/82434NX PCI, Cache, Memory Controllers (PCMC) integrate the cache and main memory DRAM control functions and provide bus control for transfers between the CPU, cache, main memory, and the PCI Local Bus. The cache controller supports write-back (or write-through for 82434LX) cache policy and cache sizes of 256-KBytes and 512-KBytes. The cache memory can be implemented with either standard or burst SRAMs. The PCMC cache controller integrates a high-performance Tag RAM to reduce system cost.



NOTE:
RAS[7:6]# and MA11 are only on the 82434NX. CCS[1:0] functionality is only on the 82434NX.

Simplified Block Diagram of the PCMC

82434LX/82434NX PCI, CACHE AND MEMORY CONTROLLER (PCMC)

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1.0 ARCHITECTURAL OVERVIEW

This section provides an 82430LX/82430NX PCIset system overview that includes a description of the bus hierarchy and bridges between the buses. The 82430LX PCIset consists of the 82434LX PCMC and 82433LX LBX components plus either a PCI/ISA bridge or a PCI/EISA bridge. The 82430NX PCIset consists of the 82434NX PCMC and 82433NX LBX components plus either a PCI/ISA bridge or a PCI/EISA bridge. The PCMC and LBX provide the core cache and main memory architecture and serve as the Host/PCI bridge. An overview of the PCMC follows the system overview section.

1.1 System Overview

The 82430LX/82430NX PCIset provides the Host/PCI bridge, cache and main memory controller, and an I/O subsystem core (either PCI/EISA or PCI/ISA bridge) for the next generation of high-performance personal computers based on the Pentium processor. System designers can take advantage of the power of the PCI (Peripheral Component Interconnect) local bus while maintaining access to the large base of EISA and ISA expansion cards. Extensive buffering and buffer management within the bridges ensures maximum efficiency in all three buses (Host CPU, PCI, and EISA/ISA Buses).

For an ISA-based system, the PCIset includes the System I/O (82378IB SIO) component (Figure 1) as the PCI/ISA bridge. For an EISA-based system (Figure 2), the PCIset includes the PCI-EISA bridge (82375EB PCEB) and the EISA System Component (82374EB ESC). The PCEB and ESC work in tandem to form the complete PCI/EISA bridge.

1.1.1. BUS HIERARCHY—CONCURRENT OPERATIONS

Systems based on the 82430LX/82430NX PCIset contain three levels of buses structured in the following hierarchy:

- Host Bus as the execution bus
- PCI Bus as a primary I/O bus
- ISA or EISA Bus as a secondary I/O bus.

This bus hierarchy allows concurrency for simultaneous operations on all three buses. Data buffering permits concurrency for operations that crossover into another bus. For example, the Pentium processor could post data destined to the PCI in the LBX. This permits the Host transaction to complete in minimum time, freeing up the Host Bus for further transactions. The Pentium processor does not have to wait for the transfer to complete to its final destination. Meanwhile, any ongoing PCI Bus transactions are permitted to complete. The posted data is then transferred to the PCI Bus when the PCI Bus is available. The LBX implements extensive buffering for Host-to-PCI, Host-to-main memory, and PCI-to-main memory transactions. In addition, the PCEB/ESC chip set and the SIO implement extensive buffering for transfers between the PCI Bus and the EISA and ISA Buses, respectively.

Host Bus

Designed to meet the needs of high-performance computing, the Host Bus features:

- 64-bit data path
- 32-bit address bus with address pipelining
- Synchronous frequencies of 60 MHz and 66 MHz
- Synchronous frequency of 50 MHz (82430NX)
- Burst read and write transfers
- Support for first level and second level caches
- Capable of full concurrency with the PCI and memory subsystems
- Byte data parity
- Full support for Pentium processor machine check and DOS compatible parity reporting
- Support for Pentium processor System Management Mode (SMM).

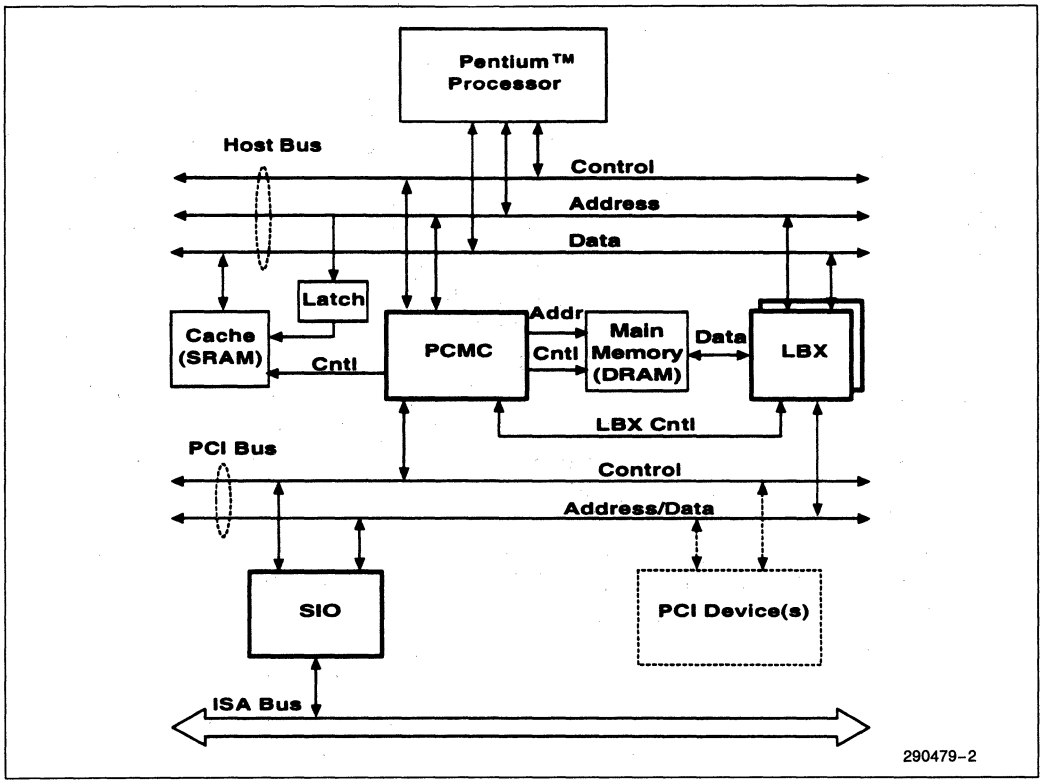


Figure 1. Block Diagram of a 82430LX/82430NX PCIset ISA System

PCI Bus

The PCI Bus is designed to address the growing industry needs for a standardized *local bus* that is not directly dependent on the speed and the size of the processor bus. New generations of personal computer system software such as Windows™ and Win-NT™ with sophisticated graphical interfaces, multi-tasking, and multi-threading bring new requirements that traditional PC I/O architectures cannot satisfy. In addition to the higher bandwidth, reliability and robustness of the I/O subsystem are becoming increasingly important. PCI addresses these needs and provides a future upgrade path. PCI features include:

- Processor independent
- Multiplexed, burst mode operation
- Synchronous at frequencies up to 33 MHz
- 120 MByte/sec usable throughput (132 MByte/sec peak) for a 32-bit data path

- Low latency random access (60 ns write access latency to slave registers from a master parked on the bus)
- Capable of full concurrency with the processor/memory subsystem
- Full multi-master capability allowing any PCI master peer-to-peer access to any PCI slave
- Hidden (overlapped) central arbitration
- Low pin count for cost effective component packaging (multiplexed address/data)
- Address and data parity
- Three physical address spaces: memory, I/O, and configuration
- Comprehensive support for autoconfiguration through a defined set of standard configuration functions.

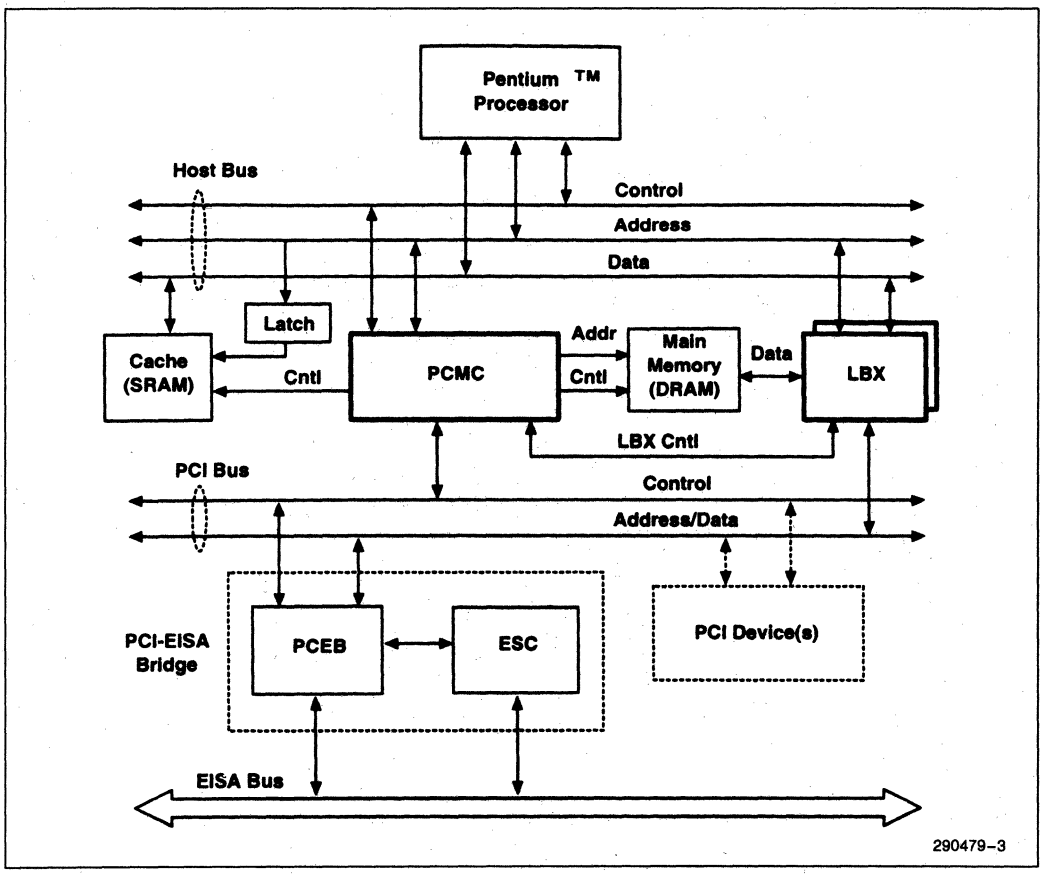


Figure 2. Block Diagram of the 82430LX/82430NX PCIset EISA System

ISA Bus

Figure 1 represents a system using the ISA Bus as the second level I/O bus. It allows personal computer platforms built around the PCI as a primary I/O bus to leverage the large ISA product base. The ISA Bus has 24-bit addressing and a 16-bit data path.

EISA Bus

Figure 2 represents a system using the EISA Bus as the second level I/O bus. It allows personal computer platforms built around the PCI as a primary I/O bus to leverage the large EISA/ISA product base. Combinations of PCI and EISA buses, both of which can be used to provide expansion functions, will satisfy even the most demanding applications.

Along with compatibility for 16-bit and 8-bit ISA hardware and software, the EISA bus provides the following key features:

- 32-bit addressing and 32-bit data path
- 33 MByte/sec bus bandwidth
- Multiple bus master support through efficient arbitration
- Support for autoconfiguration.

1.1.2 BUS BRIDGES

Host/PCI Bridge Chip Set (PCMC and LBX)

The PCMC and LBX enhance the system performance by allowing for concurrency between the Host CPU Bus and PCI Bus, giving each greater bus throughput and decreased bus latency. The LBX contains posted write buffers for Host-to-PCI, Host-to-main memory, and PCI-to-main memory transfers. The LBX also contains read prefetch buffers for Host reads of PCI, and PCI reads of main memory. There are two LBXs per system. The LBXs are controlled by commands from the PCMC. The PCMC/LBX Host/PCI bridge chip set is covered in more detail in Section 1.2, PCMC Overview.

PCI-EISA Bridge Chip Set (PCEB and ESC)

The PCEB provides the master/slave functions on both the PCI Bus and the EISA Bus. Functioning as a bridge between the PCI and EISA buses, the PCEB provides the address and data paths, bus controls, and bus protocol translation for PCI-to-EISA and EISA-to-PCI transfers. Extensive data buffering in both directions increase system performance by maximizing PCI and EISA Bus efficiency and allowing concurrency on the two buses. The PCEB's buffer management mechanism ensures data coherency. The PCEB integrates central bus control functions including a programmable bus arbiter for the PCI Bus and EISA data swap buffers for the EISA Bus. Integrated system functions include PCI parity generation, system error reporting, and programmable PCI and EISA memory and I/O address space mapping and decoding. The PCEB also contains a BIOS Timer that can be used to implement timing loops. The PCEB is intended to be used with the ESC to provide an EISA I/O subsystem interface.

The ESC integrates the common I/O functions found in today's EISA-based PCs. The ESC incorporates the logic for EISA Bus controller, enhanced seven channel DMA controller with scatter-gather support, EISA arbitration, 14 level interrupt controller, Advanced Programmable Interrupt Controller (APIC), five programmable timer/counters, non-maskable-interrupt (NMI) control, and power management. The ESC also integrates support logic to decode peripheral devices (e.g., the flash BIOS, real time clock, keyboard/mouse controller, floppy controller, two serial ports, one parallel port, and IDE hard disk drive).

PCI/ISA Bridge (SIO):

The SIO component provides the bridge between the PCI Bus and the ISA Bus. The SIO also integrates many of the common I/O functions found in today's ISA-based PCs. The SIO incorporates the logic for a PCI interface (master and slave), ISA interface (master and slave), enhanced seven channel DMA controller that supports fast DMA transfers and scatter-gather, data buffers to isolate the PCI Bus from the ISA Bus and to enhance performance, PCI and ISA arbitration, 14 level interrupt controller, a 16-bit BIOS timer, three programmable timer/counters, and non-maskable-interrupt (NMI) control logic. The SIO also provides decode for peripheral devices (e.g., the flash BIOS, real time clock, keyboard/mouse controller, floppy controller, two serial ports, one parallel port, and IDE hard disk drive).

1.2 PCMC Overview

The PCMC (along with the LBX) provides three basic functions: a cache controller, a main memory DRAM controller, and a Host/PCI bridge. This section provides an overview of these functions. Note that, in this document, operational descriptions assume that the PCMC and LBX components are used together.

1.2.1 CACHE OPERATIONS

The PCMC provides the control for a second level cache memory array implemented with either standard asynchronous SRAMs or synchronous burst SRAMs. The data memory array is external to the PCMC and located on the Host address/data bus. Since the Pentium processor contains an internal cache, there can be two separate caches in a Host subsystem. The cache inside the Pentium processor is referred to as the first level cache (also called primary cache). A detailed description of the first level cache is beyond the scope of this document. The PCMC cache control circuitry and associated external memory array is referred to as the second level cache (also called secondary cache). The second level cache is unified, meaning that both CPU data and instructions are stored in the cache. The 82434LX PCMC supports both write-through and write-back caching policies and the 82434NX supports write-back.

The optional second level cache memory array can be either 256-KBytes or 512-KBytes in size. The cache is direct-mapped and is organized as either 8K or 16K cache lines of 32 bytes per line.

In addition to the cache data RAM, the second level cache contains a 4K set of cache tags that are internal to the PCMC. Each tag contains an address that is associated with the corresponding data sector (2 lines for a 256 KByte cache and 4 lines for a 512 KByte cache) and two status bits for each line in the sector.

During a main memory read or write operation, the PCMC first searches the cache. If the addressed code or data is in the cache, the cycle is serviced by the cache. If the addressed code or data is not in the cache, the cycle is forwarded to main memory.

For the write-through (82434LX only) and write-back (both 82434LX and 82434NX) policies, the cache operation is determined by the CPU read or write cycle as follows:

Write Cycle

If the caching policy is write-through and the write cycle hits in the cache, both the cache and main memory are updated. Upon a cache miss, only main memory is updated. The cache is not updated (no write-allocate).

If the caching policy is write-back and the write cycle hits in the cache, only the cache is updated; main memory is not affected. Upon a cache miss, only main memory is updated. The cache is not updated (no write-allocate).

Read Cycle

Upon a cache hit, the cache operation is the same for both write-through and write-back. In this case, data is transferred from the cache to the CPU. Main memory is not accessed.

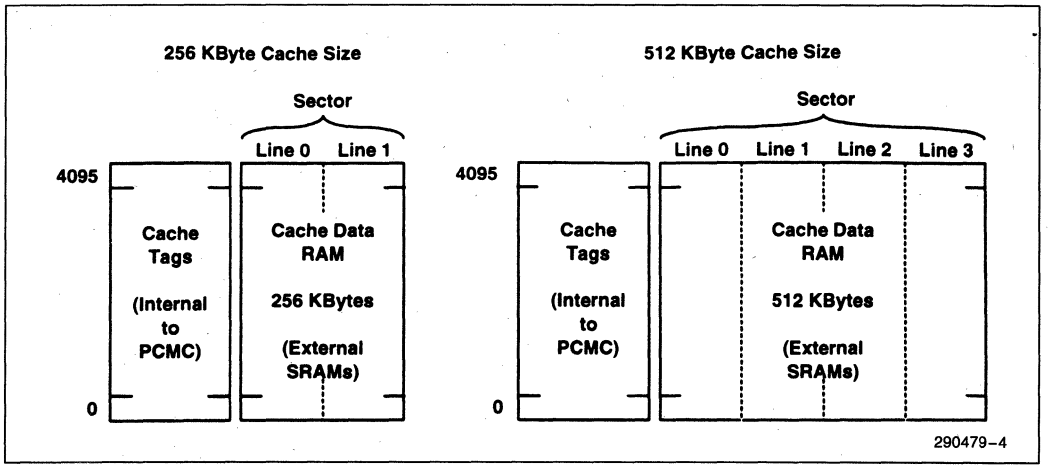


Figure 3. Second Level Cache Organization

If the read cycle causes a cache miss, the line containing the requested data is transferred from main memory to the cache and to the CPU. In the case of a write-back cache, if the cache line fill is to a sector containing one or more modified lines, the modified lines are written back to main memory and the new line is brought into the cache. For a modified line write-back operation, the PCMC transfers the modified cache lines to main memory via a write buffer in the LBX. Before writing the last modified line from the write buffer to main memory, the PCMC updates the first and second level caches with the new line, allowing the CPU access to the requested data with minimum latency.

1.2.1.1 Cache Consistency

The Snoop mechanism in the PCMC ensures data consistency between cache (both first level and second level) and main memory. The PCMC monitors PCI master accesses to main memory and when needed, initiates an inquire (snoop) cycle to the first and second level caches. The snoop mechanism guarantees that consistent data is always delivered to both the host CPU and PCI masters.

1.2.2 ADDRESS/DATA PATHS

Address paths between the CPU/cache and PCI and data paths between the CPU/cache, PCI, and main memory are supplied by two LBX components. The LBX is a companion component to the PCMC. Together, they form a Host/PCI bridge. The PCMC (via the PCMC/LBX interface signals), controls the address and data flow through the LBXs. Refer to the LBX data sheet for more details on the address and data paths.

Data is transferred to and from the PCMC internal registers via the PCMC address lines. When the Host CPU performs a write operation, the data is sent to the LBXs. When the PCMC decodes the cycle as an access to one of its internal registers, it asserts AHOLD to the CPU and instructs the LBXs to copy the data onto the Host address lines. When the PCMC decodes a Host read as an access to a PCMC internal register, it asserts AHOLD to the CPU. The PCMC then places the register data on its address lines and instructs the LBX to copy the data on the Host address bus to the Host data bus. When the register data is on the Host data bus, the PCMC negates AHOLD and completes the cycle.

1.2.2.1 Read/Write Buffers

The LBX provides an interface for the CPU address and data buses, PCI Address/Data bus, and the main memory DRAM data bus. There are three posted write buffers and one read-prefetch buffers implemented in the LBXs to increase performance and to maximize concurrency. The buffers are:

- CPU-to-Main Memory Posted Write Buffer (4 Qwords)
- CPU-to-PCI Posted Write Buffer (4 Dwords)
- PCI-to-Main Memory Posted Write Buffer (2 x 4 Dwords)
- PCI-to-Main Memory Read Prefetch Buffer (line buffer, 4 Qwords).

Refer to the LBX data sheet for details on the operation of these buffers.

1.2.3 HOST/PCI BRIDGE OPERATIONS

The PCMC permits the Host CPU to access devices on the PCI Bus. These accesses can be to PCI I/O space, PCI memory space, or PCI configuration space.

As a PCI device, the PCMC can be either a master initiating a PCI Bus operation or a target responding to a PCI Bus operation. The PCMC is a PCI Bus master for Host-to-PCI cycles and a target for PCI-to-main memory transfers. Note that the PCMC does not permit peripherals to be located on the Host Bus. CPU I/O cycles, other than to PCMC internal registers, are forwarded to the PCI Bus and PCI Bus accesses to the Host Bus are not supported.

When the CPU initiates a bus cycle to a PCI device, the PCMC becomes a PCI Bus master and translates the CPU cycle into the appropriate PCI Bus cycle. The Host/PCI Posted write buffer in the LBXs permits the CPU to complete CPU-to-PCI Dword memory writes in three CPU clocks (1 wait-state), even if the PCI Bus is currently busy. The posted data is written to the PCI device when the PCI Bus is available.

When a PCI Bus master initiates a main memory access, the PCMC (and LBXs) become the target of the PCI Bus cycle and responds to the read/write access. During PCI-to-main memory accesses, the PCMC automatically performs cache snoop operations on the Host Bus, when needed, to maintain data consistency.

As a PCI device, the PCMC contains all of the required PCI configuration registers. The Host CPU reads and writes these registers as described in Section 3.0, Register Description.

1.2.4 DRAM MEMORY OPERATIONS

The PCMC contains a DRAM controller that supports CPU and PCI master accesses to main memory. The PCMC DRAM interface supplies the control signals and address lines and the LBXs supply the data path. DRAM parity is generated for main memory writes and checked for memory reads.

For the 82434LX, the memory array is 64-bits wide and ranges in size from 2 MBytes–192 MBytes. The array can be implemented with either single-sided or double-sided SIMMs. DRAM SIMM sizes of 256K x 36, 1M x 36, and 4M x 36 are supported.

For the 82434NX, the memory array is 64-bits wide and ranges in size from 2 MBytes–512 MBytes. The array can be implemented with either single-sided or double-sided SIMMs. DRAM SIMM sizes of 256K x 36, 1M x 36, 4M x 36, and 16M x 36 are supported.

To provide optimum support for the various cache configurations, and the resultant mix of bus cycles, the system designer can select between 0-active RAS# and 1-active RAS# modes. These modes affect the behavior of the RAS# signal following either CPU-to-main memory cycles or PCI-to-main memory cycles.

The PCMC also provides programmable memory and cacheability attributes on 14 memory segments of various sizes in the ISA compatibility range (512 KByte–1 MByte address range). Access rights to these memory segments from the PCI Bus are controlled by the expansion bus bridge.

The PCMC permits a gap to be created in main memory within the 1 MByte–16 MBytes address range, accommodating ISA devices which are mapped into this range (e.g., ISA LAN card or an ISA frame buffer).

1.2.5 3.3V SIGNALS

The 82434NX PCMC drives 3.3V signal levels on the CPU and second level cache interfaces. Thus, no extra logic (i.e. 5V/3.3V translation) is required when interfacing to 3.3V processors and SRAMs. Six of the power pins on the 82434NX are VDD3 pins. These pins are connected to a 3.3V power supply. The VDD3 pins power the output buffers on the CPU and second level cache interfaces. The VDD3 pins also power the output buffers for the HCLK[A-F] outputs.

2.0 SIGNAL DESCRIPTIONS

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The states of all of the signals during hard reset are provided in Section 8.0, System Clocking and Reset.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used extensively. This is done to avoid confusion when working with a mixture of "active-low" and "active-high" signals. The term **assert**, or **assertion** indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term **negate**, or **negation** indicates that a signal is inactive.

The following notations are used to describe the signal type.

in Input is a standard input-only signal

out Totem pole output is a standard active driver

o/d Open drain

t/s Tri-State is a bi-directional, tri-state input/output pin

s/t/s Sustained tri-state is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives a s/t/s pin low must drive it high for at least one clock before letting it float. A new agent can not start driving a s/t/s signal any sooner than one clock after the previous owner tri-states it. An external pull-up is required to sustain the inactive state until another agent drives it and must be provided by the central resource.

2.1 Host Interface

Signal	Type	Description
A[31:0]	t/s	**ADDRESS BUS:** A[31:0] are the address lines of the Host Bus. A[31:3] are connected to the CPU A[31:3] lines and to the LBXs. A[2:0] are only connected to the LBXs. Along with the byte enable signals, the A[31:3] lines define the physical area of memory or I/O being accessed. During CPU cycles, the A[31:3] lines are inputs to the PCMC. They are used for address decoding and second level cache tag lookup sequences. Also during CPU cycles, A[2:0] are outputs and are generated from BE[7:0]#. A[27:24] provide hardware strapping options for test features. For more details on theses options, refer to Section 11.0 Testability. During inquire cycles, A[31:5] are inputs from the LBXs to the CPU and the PCMC to snoop the first and the second level cache tags, respectively. In response to a Flush or Flush Acknowledge Special Cycle, the PCMC asserts AHOLD and drives the addresses of the second level cache lines to be written back to main memory on A[18:7]. During CPU to PCI configuration cycles, the PCMC drives A[31:0] with the PCI configuration space address that is internally derived from the CPU physical I/O address. All PCMC internal configuration registers are accessed via A[31:0]. During CPU reads from PCMC internal configuration registers, the PCMC asserts AHOLD and drives the contents of the addressed register on A[31:0]. The PCMC then signals the LBXs to copy this value from the address lines onto the host data lines. During writes to PCMC internal configuration registers, the PCMC asserts AHOLD and signals the LBXs to copy the write data onto the A[31:0] lines. Finally, when in deturbo mode, the PCMC periodically asserts AHOLD and then drives A[31:0] to valid logic levels to keep these lines from floating for an extended period of time. A[31:28] provide hardware strapping options at powerup. For more details on strapping options, refer to Section 8.0, System Clocking and Reset. A[27:24] provide hardware strapping options for test features. For more details on these options, refer to Section 11.0 Testability.

Signal	Type	Description
BE[7:0]#	in	**BYTE ENABLES:** The byte enables indicate which byte lanes on the CPU data bus carry valid data during the current bus cycle. In the case of cacheable reads, all 8 bytes of data are driven to the Pentium processor, regardless of the state of the byte enables. The byte enable signals indicate the type of special cycle when M/IO# = D/C# = 0 and W/R# = 1. During special cycles, only one byte enable is asserted by the CPU. The following table depicts the special cycle types and their byte enable encodings: **Special Cycle Type** — **Asserted Byte Enable** Shutdown — BE0# Flush — BE1# Halt/Stop Grant — BE2# Write Back — BE3# Flush Acknowledge — BE4# Branch Trace Message — BE5# When the PCMC decodes a Shutdown Special Cycle, it asserts AHOLD, drives 000...000 (the PCI Shutdown Special Cycle Encoding) on the A[31:0] lines and signals the LBXs to latch the host address bus. The PCMC then drives a Special Cycle on PCI, signaling the LBXs to drive the latched address (00...00) on the AD[31:0] lines during the data phase. The PCMC then asserts INIT for 16 HCLKs. In response to Flush and Flush Acknowledge Special Cycles, the PCMC internally inspects the Valid and Modified bits for each of the Second Level Cache Sectors. If a line is both valid and modified, the PCMC drives the cache address of the line on the A[18:7] and CAA/CAB[6:3] lines and writes the line back to main memory. The valid and modified bits are both reset to 0. All valid and unmodified lines are simply marked invalid. In response to a write back special cycle, the PCMC simply returns BRDY# to the CPU. The second level cache will be written back to main memory in response to the following flush special cycle. If BE2# is asserted during a special cycle, the 82434NX uses A4 to determine if the cycle is a Halt or Stop Grant Special Cycle. If A4 = 0, the cycle is a Halt Special Cycle and if A4 = 1, the cycle is a Stop Grant Special cycle. In response to a halt special cycle, the PCMC asserts AHOLD, drives 000...001 (the PCI halt special cycle encoding) on the A[31:0] lines, and signals the LBXs to latch the host address bus. The PCMC then drives a special cycle on PCI, signaling the LBXs to drive the latched address (00...01) on the AD[31:0] lines during the data phase. When the 82434NX PCMC detects a CPU Stop Grant Special Cycle (M/IO# = 0, D/C# = 0, W/R# = 1, A4 = 1, BE[7:0]# = FBh), it generates a PCI Stop Grant Special cycle, with 0002h in the message field (AD[15:0]) and 0012h in the message dependent data field (AD[31:16]) during the first data phase (IRDY# asserted).
ADS#	in	**ADDRESS STROBE:** The Pentium processor asserts ADS# to indicate that a new bus cycle is beginning. ADS# is driven active in the same clock as the address, byte enable, and cycle definition signals. The PCMC ignores a floating low ADS# that may occur when BOFF# is asserted as the CPU is asserting ADS#.

Signal	Type	Description
BRDY#	out	**BURST READY:** BRDY# indicates that the system has responded in one of three ways: 1. valid data has been placed on the Pentium processor data pins in response to a read, 2. CPU write data has been accepted by the system, or 3. the system has responded to a special cycle.
NA#	out	**NEXT ADDRESS:** The PCMC asserts NA# for one clock when the memory system is ready to accept a new address from the CPU, even if all data transfers for the current cycle have not completed. The CPU may drive out a pending cycle two clocks after NA# is asserted and has the ability to support up to two outstanding bus cycles.
AHOLD	out	**ADDRESS HOLD:** The PCMC asserts AHOLD to force the Pentium processor to stop driving the address bus so that either the PCMC or LBXs can drive the bus. During PCI master cycles, AHOLD is asserted to allow the LBXs to drive a snoop address onto the address bus. If the PCI master locks main memory, AHOLD remains asserted until the PCI master locked sequence is complete and the PCI master negates PLOCK#. AHOLD is asserted during all accesses to PCMC internal configuration registers to allow configuration register accesses to occur over the A[31:0] lines. When in deturbo mode, the PCMC periodically asserts AHOLD to prevent the processor from initiating bus cycles in order to emulate a slower system. The duration of AHOLD assertion in deturbo mode is controlled by the Deturbo Frequency Control Register (offset 51h). When PWROK is negated, the PCMC asserts AHOLD to allow the strapping options on A[31:28] to be read. For more details on strapping options, see the System Clocking and Reset section.
EADS#	out	**EXTERNAL ADDRESS STROBE:** The PCMC asserts EADS# to indicate to the Pentium processor that a valid snoop address has been driven onto the CPU address lines to perform an inquire cycle. During PCI master cycles, the PCMC signals the LBXs to drive a snoop address onto the host address lines and then asserts EADS# to cause the CPU to sample the snoop address.
INV	out	**INVALIDATE:** The INV signal specifies the final state (invalid or shared) that a first level cache line transitions to in the event of a cache line hit during a snoop cycle. When snooping the caches during a PCI master write, the PCMC asserts INV with EADS#. When INV is asserted with EADS#, an inquire hit results in the line being invalidated. When snooping the caches during a PCI master read, the PCMC does not assert INV with EADS#. In this case, an inquire cycle hit results in a line transitioning to the shared state.
BOFF#	out	**BACKOFF:** The PCMC asserts BOFF# to force the Pentium processor to abort all outstanding bus cycles that have not been completed and float its bus in the next clock. The PCMC uses this signal to force the CPU to re-order a write-back due to a snoop cycle around a currently outstanding bus cycle. The PCMC also asserts BOFF# to obtain the CPU data bus for write-back cycles from the secondary cache due to a snoop hit. The CPU remains in bus hold until BOFF# is negated.
HITM#	in	**HIT MODIFIED:** The Pentium processor asserts HITM# to inform the PCMC that the current inquire cycle hit a modified line. HITM# is asserted by the Pentium processor two clocks after the assertion of EADS# if the inquire cycle hits a modified line in the primary cache.

Signal	Type	Description
M/IO# D/C# W/R#	in	**BUS CYCLE DEFINITION (MEMORY/INPUT-OUTPUT, DATA/CONTROL, WRITE/READ):** M/IO, D/C# and W/R# define Host Bus cycles as shown in the table below. **M/IO# D/C# W/R# Bus Cycle Type** Low Low Low Interrupt Acknowledge Low Low High Special Cycle Low High Low I/O Read Low High High I/O Write High Low Low Code Read High Low High Reserved High High Low Memory Read High High High Memory Write Interrupt acknowledge cycles are forwarded to the PCI Bus as PCI interrupt acknowledge cycles (i.e. C/BE[3:0]# = 0000 during the address phase). All I/O cycles and any memory cycles that are not directed to memory controlled by the PCMC DRAM controller are forwarded to PCI. The Pentium processor generates six different types of special cycles. The special cycle type is encoded on the BE[7:0]# lines.
HLOCK#	in	**HOST BUS LOCK:** The Pentium processor asserts HLOCK# to indicate the current bus cycle is locked. HLOCK# is asserted in the first clock of the first locked bus cycle and is negated after the BRDY# is returned for the last locked bus cycle. The Pentium processor guarantees HLOCK# to be negated for at least one clock between back-to-back locked operations. When a CPU locked cycle is directed to main memory, the PCMC guarantees that once the locked operation begins in main memory, the CPU has exclusive access to main memory (i.e., PCI master accesses to main memory will not be initiated until the CPU locked operation completes). When a CPU locked cycle is directed to PCI, the PCMC arbitrates for PLOCK# (PCI LOCK#) before initiating the cycle on PCI, except when the cycle is to the memory range defined by the Frame Buffer Range Register and the No Lock Requests bit in that register is set to 1.
CACHE#	in	**CACHEABILITY:** The Pentium processor asserts CACHE# to indicate the internal cacheability of a read cycle or that a write cycle is a burst write-back cycle. If the CPU drives CACHE# inactive during a read cycle, the returned data is not cached, regardless of the state of KEN#. The CPU asserts CACHE# for cacheable data reads, cacheable code fetches, and cache line write-backs. CACHE# is driven along with the cycle definition pins.
KEN#	out	**CACHE ENABLE:** The PCMC asserts KEN# to indicate to the CPU that the current cycle is cacheable. KEN# is asserted for all accesses to memory ranges 0–512-KBytes and 1024-KBytes to the top of main memory controlled by the PCMC when the Primary Cache Enable bit is set to 1, except in the following case: KEN# is not asserted for accesses to the top 64-KByte of main memory controlled by the PCMC when the SMRAM Enable bit in the DRAM Control Register (Offset 57h) is set to 1 and the area is not write protected. If the area is write protected and cacheable, KEN# is asserted for code read cycles, but is not asserted during data read cycle. KEN# is asserted for any CPU access within the range of 512-KBytes–1024-KBytes if the corresponding Cache Enable bit in the PAM[6:0] Registers (offsets 59h–5Fh) is set to 1. When the Pentium processor indicates that the current read cycle can be cached by asserting CACHE# and the PCMC responds with KEN#, the cycle is converted into a burst cache line fill. The CPU samples KEN# with the first of either BRDY# or NA#.

Signal	Type	Description
SMIACT#	in	**SYSTEM MANAGEMENT INTERRUPT ACTIVE:** The Pentium processor asserts SMIACT# to indicate that the processor is operating in System Management Mode (SMM). When the SMRAM Enable bit in the DRAM Control Register (offset 57h) is set to 1, the PCMC allows CPU accesses SMRAM as permitted by the SMRAM Space Register at configuration space offset 72h.
PEN#	out	**PARITY ENABLE:** The PEN# signal, along with the MCE bit in CR4 of the Pentium processor, determines whether a machine check exception will be taken by the CPU as a result of a parity error on a read cycle. The PCMC asserts PEN# during DRAM read cycles if the MCHK on DRAM/L2 Cache Data Parity Error Enable bit in the Error Command Register (offset 70h) is set to 1. The PCMC asserts PEN# during CPU second level cache read cycles if the MCHK on DRAM/L2 Cache Data Parity Error Enable and the L2 Cache Parity Enable bits in the Error Command Register (offset 70h) are both set to 1.
PCHK#	in	**DATA PARITY CHECK:** PCHK# is sampled by the PCMC to detect parity errors on CPU read cycles from main memory if the Parity Error Mask Enable bit in the DRAM Control Register (offset 57h) is reset to 0. PCHK# is sampled by the PCMC to detect parity errors on CPU read cycles from the second level cache if the L2 Cache Parity Enable bit in the Error Command Register (offset 70h) is set to 1. If incorrect parity was detected on a data read, the PCHK# signal is asserted by the Pentium processor two clocks after BRDY# is returned. PCHK# is asserted for one clock for each clock in which a parity error was detected.

2.2 DRAM Interface

Signal	Type	Description
RAS[5:0]#	out	**ROW ADDRESS STROBES:** The RAS[5:0]# signals are used to latch the row address on the MA[10:0] lines into the DRAMs. Each RAS[5:0]# signal corresponds to one DRAM row. The 82434LX PCMC supports up to 6 rows in the DRAM array. Each row is eight bytes wide. These signals drive the RAS# lines of the DRAM array directly, without external buffers.
RAS[7:6]#	out	**ROW ADDRESS STROBES:** The 82434NX supports up to eight rows of DRAM. RAS[7:6]# are used with RAS[5:0] to latch the row address on the MA[11:0] lines into the DRAMs. Each row is eight bytes wide. These signals drive the RAS# lines of the DRAM array directly, without external buffers.
CAS[7:0]#	out	**COLUMN ADDRESS STROBES:** The CAS[7:0]# signals are used to latch the column address on the MA[10:0] lines into the DRAMs. Each CAS[7:0]# signal corresponds to one byte of the eight byte-wide array. These signals drive the CAS# lines of the DRAM array directly, without external buffers. In a minimum configuration, each CAS[7:0]# line only has one SIMM load, while the maximum configuration has 6 SIMM loads.
WE#	out	**DRAM WRITE ENABLE:** WE# is asserted during both CPU and PCI master writes to main memory. During burst writes to main memory, WE# is asserted before the first assertion of CAS[7:0]# and is negated with the last CAS[7:0]#. The WE# signal is externally buffered to drive the WE# inputs on the DRAMs.
MA[10:0]	out	**DRAM MULTIPLEXED ADDRESS:** MA[10:0] provide the row and column address to the DRAM array. The 82434LX uses MA[10:0] for the complete DRAM address bus. The MA[10:0] lines are externally buffered to drive the multiplexed address lines of the DRAM array.
MA11	out	**DRAM MULTIPLEXED ADDRESS:** MA11 provides the extra addressability for the 16M x 36 SiMMs that are supported by the 82434NX. MA[11:0] provide the row and column address to the DRAM array. Like MA[10:0], MA11 is externally buffered to drive the multiplexed address lines of the DRAM array.

2.3 Cache Interface

Signal	Type	Description
CALE	out	**CACHE ADDRESS LATCH ENABLE:** CALE controls the external latch between the host address lines and the cache address lines. CALE is asserted to open the external latch, allowing the host address lines to propagate to the cache address lines. CALE is negated to latch the cache address lines.
CADS[1:0]#, CR/W[1:0]#	out	This signal pin has two functions, depending on the type of SRAMs used for the second level cache. **CACHE ADDRESS STROBE:** CADS[1:0]# are used with burst SRAMs. When asserted, CADS[1:0]# cause the burst SRAMs to latch the cache address on the rising edge of HCLK. CADS[1:0]# are glitch-free synchronous signals. CADS[1:0]# functionality is selected by the SRAM type bit in the Secondary Cache Control Register. Two copies of this signal are provided for timing reasons only. **CACHE READ/WRITE:** CR/W# provide read/write control to the second level cache when using asynchronous dual-byte select SRAMs. This functionality is selected by the SRAM Type and Cache Byte Control Bits in the Secondary Cache Control Register. The two copies of this signal are always driven to the same logic level.
CADV[1:0]#, CCS[1:0]#	out	This signal pin has two functions. The Cache Chip Select function is only enabled when the SRAM connectivity bit (bit 2) in the SCC Register is set to 1. **CACHE ADVANCE:** CADV[1:0]# are used with burst SRAMs to advance the internal two bit address counter inside the SRAMs to the next address of the burst sequence. Two copies of this signal are provided for timing reasons only. The two copies are always driven to the same logic level. **CACHE CHIP SELECT:** CCS[1:0]# are used with asynchronous SRAMs to de-select the SRAMs, placing them in a low power standby mode. When the CPU runs a halt or stop grant special cycle, the 82434NX negates CCS[1:0]#, placing the second level cache in a power saving mode. The PCMC then asserts CCS[1:0]# (activating the SRAMs) when the CPU asserts ADS#. When using burst SRAMs, only CCS1# implements the CCS# function. CADV0# retains the address advance function. CCS1# serve two purposes with burst SRAMs: 1) It is used (along with CADS[1:0]#) to place the SRAMs in a low power standby mode. When the CPU runs a halt or stop grant special cycle, the 82434NX negates CCS1# and asserts CADS[1:0]# for one clock, placing the SRAMs in a power saving mode. The PCMC then asserts CCS1# so that the next ADS# from the CPU places the SRAMs in an active mode. 2) CCS1# is used to block pipelined cycles from the SRAMs when the SRAMs are servicing a cycle. After NA# is asserted, the PCMC negates CCS1# preventing the SRAMs from sampling a new address. CCS1# is asserted again when the SRAMs have completed the current cycle.
CAA[6:3] CAB[6:3]	out	**CACHE ADDRESS [6:3]:** CAA[6:3] and CAB[6:3] are connected to address lines A[3:0] on the second level cache SRAMs. CAA[4:3] and CAB[4:3] are used with standard SRAMs to advance through the burst sequence. CAA[6:5] and CAB[6:5] are used during second level cache write-back cycles to address the modified lines within the addressed sector. Two copies of these signals are provided for timing reasons only. The two copies are always driven to the same logic level.

Signal	Type	Description
COE[1:0]#	out	**CACHE OUTPUT ENABLE:** COE[1:0]# are asserted when data is to be read from the second level cache and are negated at all other times. Two copies of this signal are provided for timing reasons only. The two copies are always driven to the same logic level.
CWE[7:0]#, CBS[7:0]#	out	This signal pin has two functions, depending on the type of SRAMs used for the second level cache. **CACHE WRITE ENABLES:** CWE[7:0]# are asserted to write data to the second level cache SRAMs on a byte-by-byte basis. CWE7# controls the most significant byte while CWE0# controls the least significant byte. These signals are cache write enables when using burst SRAMs (SRAM Type bit in SCC Register is 1) or when using asynchronous SRAMs (SRAM Type bit in SCC Register is 0) and the Cache Byte Control Bit is 1. **CACHE BYTE SELECTS:** The CBS[7:0]# lines provide byte control to the secondary cache when using dual-byte select asynchronous SRAMs. These signals are Cache Byte select lines when the SRAM Type and Cache Byte Control Bits in the SCC Register are both 0.

2.4 PCI Interface

Signal	Type	Description
C/BE[3:0]#	t/s	**PCI BUS COMMAND AND BYTE ENABLES:** C/BE[3:0]# are driven by the current bus master during the address phase of a PCI cycle to define the PCI command, and during the data phase as the PCI byte enables. The PCI commands indicate the current cycle type, and the PCI byte enables indicate which byte lanes carry meaningful data. C/BE[3:0]# are outputs of the PCMC during CPU cycles that are directed to PCI. C/BE[3:0]# are inputs when the PCMC acts as a slave. The command encodings and types are listed below. **C/BE[3:0]# — Command** 0000 — Interrupt Acknowledge 0001 — Special Cycle 0010 — I/O Read 0011 — I/O Write 0100 — Reserved 0101 — Reserved 0110 — Memory Read 0111 — Memory Write 1000 — Reserved 1001 — Reserved 1010 — Configuration Read 1011 — Configuration Write 1100 — Memory Read Multiple 1101 — Reserved 1110 — Memory Read Line 1111 — Memory Write and Invalidate

Signal	Type	Description
FRAME#	s/t/s	**CYCLE FRAME:** FRAME# is driven by the current bus master to indicate the beginning and duration of an access. FRAME# is asserted to indicate that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is negated, the transaction is in the final data phase. FRAME# is an output of the PCMC during CPU cycles which are directed to PCI. FRAME# is an input to the PCMC when the PCMC acts as a slave.
IRDY#	s/t/s	**INITIATOR READY:** The assertion of IRDY# indicates the current bus master's ability to complete the current data phase. IRDY# works in conjunction with TRDY# to indicate when data has been transferred. On PCI, data is transferred on each clock that both IRDY# and TRDY# are asserted. During read cycles, IRDY# is used to indicate that the master is prepared to accept data. During write cycles, IRDY# is used to indicate that the master has driven valid data on the AD[31:0] lines. Wait states are inserted until both IRDY# and TRDY# are asserted together. IRDY# is an output of the PCMC when the PCMC is the PCI master. IRDY# is an input to the PCMC when the PCMC acts as a slave.
TRDY#	s/t/s	**TARGET READY:** TRDY# indicates the target device's ability to complete the current data phase of the transaction. It is used in conjunction with IRDY#. A data phase is completed on each clock that TRDY# and IRDY# are both sampled asserted. During read cycles, TRDY# indicates that valid data is present on AD[31:0] lines. During write cycles, TRDY# indicates the target is prepared to accept data. Wait states are inserted on the bus until both IRDY# and TRDY# are asserted together. TRDY# is an output of the PCMC when the PCMC is the PCI slave. TRDY# is an input to the PCMC when the PCMC is a master.
DEVSEL#	s/t/s	**DEVICE SELECT:** When asserted, DEVSEL# indicates that the driving device has decoded its address as the target of the current access. DEVSEL# is an output of the PCMC when PCMC is a PCI slave and is derived from the MEMCS# input. MEMCS# is generated by the expansion bus bridge as a decode to the main memory address space. During CPU-to-PCI cycles, DEVSEL# is an input. It is used to determine if any device has responded to the current bus cycle, and to detect a target abort cycle. Master-Abort termination results if no subtractive decode agent exists in the system, and no one asserts DEVSEL# within a programmed number of clocks.
STOP#	s/t/s	**STOP:** STOP# indicates that the current target is requesting the master to stop the current transaction. This signal is used in conjunction with DEVSEL# to indicate disconnect, target-abort, and retry cycles. When PCMC is acting as a master on PCI, if STOP# is sampled active on a rising edge of PCLKIN, FRAME# is negated within a maximum of 3 clock cycles. STOP# may be asserted by the PCMC in three cases. If a PCI master attempts to access main memory when another PCI master has locked main memory, the PCMC asserts STOP# to signal retry. The PCMC detects this condition when sampling FRAME# and LOCK# both active during an address phase. When a PCI master is reading from main memory, the PCMC asserts STOP# when the burst cycle is about to cross a cache line boundary. When a PCI master is writing to main memory, the PCMC asserts STOP# upon filling either of the two PCI-to-main memory posted write buffers. Once asserted, STOP# remains asserted until FRAME# is negated.

Signal	Type	Description
PLOCK#	s/t/s	**PCI LOCK:** PLOCK# is used to indicate an atomic operation that may require multiple transactions to complete. PCI provides a mechanism referred to as "resource lock" in which only the target of the PCI transaction is locked. The assertion of GNT# on PCI does not guarantee control of the PLOCK# signal. Control of PLOCK# is obtained under its own protocol. When the PCMC is the PCI slave, PLOCK# is sampled as an input on the rising edge of PCLKIN when FRAME# is sampled active. If PLOCK# is sampled asserted, the PCMC enters into a locked state and remains in the locked state until PLOCK# is sampled negated on a following rising edge of PCLKIN, when FRAME# is sampled asserted.
REQ#	out	**REQUEST:** The PCMC asserts REQ# to indicate to the PCI bus arbiter that the PCMC is requesting use of the PCI Bus in response to a CPU cycle directed to PCI.
GNT#	in	**GRANT:** When asserted, GNT# indicates that access to the PCI Bus has been granted to the PCMC by the PCI Bus arbiter.
MEMCS#	in	**MAIN MEMORY CHIP SELECT:** When asserted, MEMCS# indicates to the PCMC that a PCI master cycle is targeting main memory. MEMCS# is generated by the expansion bus bridge. MEMCS# is sampled by the PCMC on the rising edge of PCLKIN on the first and second cycle after FRAME# has been asserted.
FLSHREQ#	in	**FLUSH REQUEST:** When asserted, FLSHREQ# instructs the PCMC to flush the CPU-to-PCI posted write buffer in the LBXs and to disable further posting to this buffer as long as FLSHREQ# remains active. The PCMC acknowledges completion of the CPU-to-PCI write buffer flush operation by asserting MEMACK#. MEMACK# remains asserted until FLSHREQ# is negated. FLSHREQ# is driven by the expansion bus bridge and is used to avoid deadlock conditions on the PCI Bus.
MEMREQ#	in	**MEMORY REQUEST:** When asserted, MEMREQ# instructs the PCMC to flush the CPU-to-PCI and CPU-to-main memory posted write buffers and to disable posting in these buffers as long as MEMREQ# is active. The PCMC acknowledges completion of the flush operations by asserting MEMACK#. MEMACK# remains asserted until MEMREQ# is negated. MEMREQ# is driven by the expansion bus bridge.
MEMACK#	out	**MEMORY ACKNOWLEDGE:** When asserted, MEMACK# indicates the completion of the operations requested by an active FLSHREQ# and/or MEMREQ#.
PAR	t/s	**PARITY:** PAR is an even parity bit across the AD[31:0] and C/BE[3:0]# lines. Parity is generated on all PCI transactions. As a master, the PCMC generates even parity on CPU writes to PCI, based on the PPOUT[1:0] inputs from the LBXs. During CPU read cycles from PCI, the PCMC checks parity by checking the value sampled on the PAR input with the PPOUT[1:0] inputs from the LBXs. As a slave, the PCMC generates even parity on PAR, based on the PPOUT[1:0] inputs during PCI master reads from main memory. During PCI master writes to main memory, the PCMC checks parity by checking the value sampled on PAR with the PPOUT[1:0] inputs.

Signal	Type	Description
PERR#	s/t/s	**PARITY ERROR:** PERR# may be pulsed by any agent that detects a parity error during an address phase, or by the master or the selected target during any data phase in which the AD lines are inputs. The PERR# signal is enabled when the PERR# on Receiving Data Parity Error bit in the Error Command Register (offset 70h) and the Parity Error Enable bit in the PCI Command Register (offset 04h) are both set to 1. When enabled, CPU-to-PCI write data is checked for parity errors by sampling the PERR# signal two PCI clocks after data is driven. Also, when enabled, PERR# is asserted by the PCMC when it detects a data parity error on CPU read data from PCI and PCI master write data to main memory. PERR# is neither sampled nor driven by the PCMC when either the PERR# on Receiving Data Parity Error bit in the Error Command Register or the Parity Error Enable bit in the PCI Command Register is reset to 0.
SERR#	o/d	**SYSTEM ERROR:** SERR# may be pulsed by any agent for reporting errors other than parity. SERR# is asserted by the PCMC whenever a serious system error (not necessarily a PCI error) occurs. The intent is to have the PCI central agent (for example, the expansion bus bridge) assert NMI to the processor. Control over the SERR# signal is provided via the Error Command Register (offset 70h) when the Parity Error Enable bit in the PCI Command Register (offset 04h) is set to 1. When the SERR# DRAM/L2 Cache Data Parity Error bit is set to 1, SERR# is asserted upon detecting a parity error on CPU read cycles from DRAM. If the L2 Cache Parity bit is also set to 1, SERR# will be asserted upon detecting a parity error on CPU read cycles from the second level cache. The Pentium processor indicates these parity errors to the PCMC via the PCHK# signal. When the SERR# on PCI Address Parity Error bit is set to 1, the PCMC asserts SERR# if a parity error is detected during the address phase of a PCI master cycle. When the SERR# on Received PCI Data Parity bit is set to 1, the PCMC asserts SERR# if a parity error is detected on PCI during a CPU read from PCI. During CPU to PCI write cycles, when the SERR# on Transmitted PCI Data Parity Error bit is set to 1, the PCMC asserts SERR# in response to sampling PERR# active. When the SERR# on Received Target Abort bit is set to 1, the PCMC asserts SERR# when the PCMC receives a target abort on a PCMC initiated PCI cycle. If the Parity Error Enable bit in the PCI Command Register is reset to 0, SERR# is disabled and is never asserted by the PCMC.

2.5 LBX Interface

Signal	Type	Description
HIG[4:0]	out	**HOST INTERFACE GROUP:** HIG[4:0] are outputs of the PCMC used to control the LBX HA (Host Address) and HD (Host Data) buses. Commands driven on HIG[4:0] cause the host data and/or address lines to be either driven or latched by the LBXs. See the 82433LX (LBX) Local Bus Accelerator Data Sheet for a listing of the HIG[4:0] commands.
MIG[2:0]	out	**MEMORY INTERFACE GROUP:** MIG[2:0] are outputs of the PCMC and control the LBX MD (Memory Data) bus. Commands driven on the MIG[2:0] lines cause the memory data lines to be either driven or latched by the LBXs. See the 82433LX (LBX) Local Bus Accelerator Data Sheet for a listing of the MIG[2:0] commands.
MDLE	out	**MEMORY DATA LATCH ENABLE:** During CPU reads from main memory, MDLE is used to control the latching of memory read data on the CPU data bus. MDLE is negated as CAS[7:0]# are negated to close the latch between the memory data bus and the host data bus. During CPU reads from main memory, the PCMC closes the memory data to host data latch in the LBXs as BRDY# is asserted and opens the latch after the CPU has sampled the data.
PIG[3:0]	out	**PCI INTERFACE GROUP:** PIG[3:0] are outputs of the PCMC used to control the LBX AD (PCI Address/Data) bus. Commands driven on the PIG[3:0] lines cause the AD lines to be either driven or latched. See the 82433LX (LBX) Local Bus Accelerator Data Sheet for a listing of the PIG[3:0] commands.
DRVPCI	out	**DRIVE PCI:** DRVPCI acts as an output enable for the LBX AD lines. When sampled asserted, the LBXs begin driving the PCI AD lines. When negated, the AD lines on the LBXs are tri-stated. The LBX AD lines are tri-stated asynchronously from the falling edge of DRVPCI.
EOL	in	**END OF LINE:** EOL is asserted by the low order LBX when a PCI master read or write transaction is about to overrun a cache line boundary. EOL has an internal pull-up resistor inside the PCMC. The low order LBX EOL signal connects to this PCMC input. The high order LBX EOL signal is connected to ground through an external pull-down resistor.
PPOUT[1:0]	in	**PCI PARITY OUT:** These signals reflect the parity of the 32 AD lines driven from or latched in the LBXs, depending on the command driven on PIG[3:0]. The PPOUT0 pin has a weak internal pull-down resistor. The PPOUT1 pin has a weak internal pull-up resistor.

2.6 Reset And Clock

Signal	Type	Description
HCLKOSC	in	**HOST CLOCK OSCILLATOR:** The HCLKOSC input is driven externally by a crystal oscillator. The PCMC generates six copies of HCLK from HCLKOSC (HCLKA–HCLKF). During power-up, HCLKOSC must stabilize for 1 ms before PWROK is asserted. If an external clock driver is used to clock the CPU, PCMC, LBXs and second level cache SRAMs instead of the HCLKA–HCLKF outputs, HCLKOSC must be tied either high or low.
HCLKA–HCLKF	out	**HOST CLOCK OUTPUTS:** HCLKA–HCLKF are six low skew copies of the host clock. These outputs eliminate the need for an external low skew clock driver.

Signal	Type	Description
HCLKIN	in	**HOST CLOCK INPUT:** All timing on the host, DRAM and second level cache interfaces is based on HCLKIN. If an external clock driver is used to clock the CPU, PCMC, LBXs and second level cache SRAMs, the externally generated clock must be connected to HCLKIN. During power-up HCLKIN must stabilize for 1 ms before PWROK is asserted.
CPURST	out	**CPU HARD RESET:** The CPURST pin is asserted in response to one of two conditions. **Powerup** 82434LX: During powerup the 82434LX asserts CPURST when PWROK is negated. When PWROK is asserted, the 82434LX first ensures that it has been initialized before negating CPURST. 82434NX: During powerup, the 82434NX PCMC negates CPURST while PWROK is negated. When PWROK is asserted, the 82434NX asserts CPURST for 2 ms. **Software** CPURST is also asserted when the System Hard Reset Enable bit in the Turbo-Reset Control Register (I/O address 0CF9h) is set to 1 and the Reset CPU bit toggles from 0 to 1 (82434LX and 82434NX). CPURST is driven synchronously to the rising edge of HCLKIN.
INIT	out	**INITIALIZATION:** INIT is asserted in response to any one of two conditions. When the System Hard Reset Enable bit in the Turbo-Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, the PCMC initiates a soft reset by asserting INIT. The PCMC also initiates a soft reset by asserting INIT in response to a shutdown special cycle. In both cases, INIT is asserted for a minimum of 2 Host clocks.
PWROK	in	**POWER OK:** When asserted, PWROK is an indication to the PCMC that power and HCLKIN have stabilized for at least 1 ms. PWROK can be driven asynchronously. 82434LX: When PWROK is negated, the 82434LX asserts both CPURST and PCIRST#. When PWROK is driven high, the 82434LX ensures that it is initialized before negating CPURST and PCIRST#. 82434NX: When PWROK is negated, the 82434NX negates CPURST and asserts PCIRST#. When PWROK is asserted, the 82434NX asserts CPURST for 2 ms. PCIRST# is negated 1 ms after PWROK is asserted.
PCLKOUT	out	**PCI CLOCK OUTPUT:** PCLKOUT is internally generated by a Phase Locked Loop (PLL) that divides the frequency of HCLKIN by 2. This output must be buffered externally to generate multiple copies of the PCI Clock. One of the copies must be connected to the PCLKIN pin.

Signal	Type	Description
PCLKIN	in	**PCI CLOCK INPUT:** An internal PLL locks PCLKIN in phase with HCLKIN. All timing on the PCMC PCI interface is referenced to the PCLKIN input. All output signals on the PCI interface are driven from PCLKIN rising edges and all input signals on the PCI interface are sampled on PCLKIN rising edges.
PCIRST#	out	**PCI RESET:** PCIRST# is asserted to initiate hard reset on PCI. PCIRST# is asserted in response to one of two conditions. **Power-up** During power-up the PCMC asserts PCIRST# when PWROK is negated. 82434LX: When PWROK is asserted the PCMC will first ensure that it has been initialized before negating PCIRST#. 82434NX: When PWROK is negated, the 82434NX asserts PCIRST#. The 82434NX then negates PCIRST# 1 ms after PWROK is asserted. **Software** PCIRST# is also asserted when the System Hard Reset Enable bit in the Turbo/Reset Control Register is set to 1 and the Reset CPU bit toggles from 0 to 1 (82434LX and 82434NX). PCIRST# is driven asynchronously.
TESTEN	in	**TEST ENABLE:** TESTEN must be tied low for normal system operation.

3.0 REGISTER DESCRIPTION

The 82434LX/82434NX PCMC contains two sets of software accessible registers. These registers are accessed via the Host CPU I/O address space. The PCMC also contains a set of configuration registers that reside in PCI configuration space and are used to specify PCI configuration, DRAM configuration, cache configuration, operating parameters and optional system features (see Section 3.2, PCI Configuration Space Mapped Registers). The PCMC internal registers (both I/O Mapped and Configuration registers) are only accessible by the Host CPU and cannot be accessed by PCI masters. The registers can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field).

Some of the PCMC registers described in this section contain reserved bits. These bits are labeled "R". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.

In addition to reserved bits within a register, the PCMC contains address locations in the PCI configuration space that are marked "Reserved" (Table 1). The PCMC responds to accesses to these address locations by completing the Host cycle. When a reserved register location is read, 0000h is returned. Writes to reserved registers have no affect on the PCMC.

Upon receiving a hard reset via the PWROK signal, the PCMC sets its internal configuration registers to predetermined **default** states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, cache configuration, operating parameters and optional system features that are applicable, and to program the PCMC registers accordingly.

The following nomenclature is used for access attributes.

RO **Read Only.** If a register is read only, writes to this register have no effect.

R/W **Read/Write.** A register with this attribute can be read and written.

R/WC **Read/Write Clear.** A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.

3.1 I/O Mapped Registers

The 82434LX PCMC contains three registers that reside in the CPU I/O address space—the Configuration Space Enable (CSE) Register, the Turbo-Reset Control (TRC) Register and the Forward (FORW) Register. These registers can not reside in PCI configuration space because of the special functions they perform. The CSE Register enables/disables the configuration space and, hence, can not reside in that space. The TRC Register enables/disables deturbo mode which effectively slows the processor to accommodate software programs that rely on the slow speed of PC/XT systems to time certain events. The FORW Register determines which of the possible hierarchical PCI Buses a cycle is directed. The 82434LX uses mechanism #2 for accessing PCI configuration space.

The 82434NX PCMC contains five registers that reside in the CPU I/O address spacethe Configuration Address (CONFADD) Register, the Configuration Space Enable (CSE) Register, the Turbo-Reset Control (TRC) Register, the Forward (FORW) Register, and the PCI Mechanism Control (PMC) Register. The CSE, TRC, and FORW Registers are the same for both the 82434LX and 82434NX PCMCs. The 82434NX can use either Configuration Access Mechanism #1 or #2 for accessing PCI configuration space. When Configuration Access Mechanism #1 is used (See Section 3.2, PCI Configuration Space Mapped Registers), The CONFADD Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data (CONFDATA) window. The CSE and FORW Registers are used for Configuration Access Mechanism #2. The PCI Mechanism Control (PMC) Register selects whethenConfiguration Access Mechanism 1 or 2 is used (see the Rev 2.0 PCI Local Bus Specification).

3.1.1 CONFADD—CONFIGURATION ADDRESS REGISTER

I/O Address: 0CF8h Accessed as a Dword
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

CONFADD is a 32-bit register used in Configuration Access Mechanism #1. It is accessed only when referenced as a Dword and PCAMS in the PMC Register is set to 1. Byte or Word references "pass through" the CONFADD Register to the I/O locations "behind" it. For example a byte access to 0CF8h will access the CSE Register, while a word access to CF8h will access both the CSE and TRC Registers. The CONFADD Register contains the Bus Number, Device Number, Function Number, and Register Number where the CONFDATA window is located.

Bit	Description
31	**CONFIGURATION ENABLE (CONE)—R/W:** When CONE = 1, accesses to PCI configuration space are enabled, if the PCAMS bit of the PMC register is also 1. When CONE = 0, accesses to PCI configuration space are disabled, if the PCAMS bit is 1. If the PCAMS bit is 0, this bit has no effect.
30:24	**RESERVED**
23:16	**BUS NUMBER (BUSNUM)—R/W:** When the BUSNUM is programmed to 00h, the target of the Configuration Cycle is either the PCMC or the PCI Local Bus that is directly connected to the PCMC. PCI Access Mechanism #1 can generate either type 0 or type 1 configuration cycles on PCI. A type 0 Configuration Cycle is generated on PCI if the Bus Number is programmed to 00h and the PCMC is not the target. If the Bus Number is non-zero a type 1 configuration cycle is generated on PCI with the Bus Number mapped to AD[23:16] during the address phase.
15:11	**DEVICE NUMBER (DEVNUM)—R/W:** This field selects one agent on the PCI Bus selected by the Bus Number. During a Type 1 Configuration cycle this field is mapped to AD[15:11]. During a Type 0 Configuration Cycle this field is decoded and one of AD[31:17] is driven to a 1. The PCMC is always Device Number 0.
10:8	**FUNCTION NUMBER (FUNCNUM)—R/W:** This field is mapped to AD[10:8] during PCI configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed.
7:2	**REGISTER NUMBER (REGNUM)—R/W:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. REGNUM is mapped to AD[7:2] during PCI configuration cycles.
1:0	**RESERVED**

3.1.2 CSE—CONFIGURATION SPACE ENABLE REGISTER

I/O Address: 0CF8h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The CSE Register enables/disables configuration space access and provides access to specific functions within a PCI agent. The register is located in the CPU I/O address space. The PCMC, as a Host/PCI Bridge, supports multi-function devices on the PCI Bus. The function number permits individual configuration spaces for up to eight functions within an agent. The register is located in the CPU I/O address space.

Bit	Description
7:4	**KEY FIELD (KEY)—R/W:** This field is used only when the PCI Mechanism Control Register (PMC) indicates Configuration Access Mechanism 2 is to be used. When the key field is programmed to 0h, the PCI configuration space is disabled. When the key field is programmed to a non-zero value, all CPU accesses to CnXXh (where n is a non zero value) are forwarded to PCI as configuration space accesses. Additionally, when the key field is programmed to a non-zero value, all CPU accesses to C0XXh are intercepted by the PCMC and directed to a PCMC internal register.
3:1	**FUNCTION NUMBER (FN)—R/W:** For multi-function devices, this field selects a particular function within a PCI device. During a configuration cycle, bits[3:1] become part of the PCI Bus address and correspond to AD[10:8].
0	**RESERVED**

3.1.3 TRC—TURBO-RESET CONTROL REGISTER

I/O Address: 0CF9h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The TRC Register is an 8-bit read/write register that selects turbo/deturbo mode of the CPU, initiates PCI Bus and CPU reset cycles, and initiates the CPU Built In Self Test (BIST). TRC is located in CPU I/O address space.

Bit	Description
7:3	**RESERVED**
2	**RESET CPU (RCPU)—R/W:** RCPU is used to initiate a hard reset or soft reset to the CPU. During a hard reset, the PCMC asserts CPURST and PCIRST#. The PCMC initiates a hard reset when this register is programmed for a hard reset or when the PWROK signal is asserted. During a soft reset, the PCMC asserts INIT. The PCMC initiates a soft reset when this register is programmed for a soft reset and in response to a shutdown special cycle. Note that a hard reset initializes the entire system and invalidates the CPU cache. A soft reset initializes only the CPU. The contents of the CPU cache are unaffected. This bit is used in conjunction with bit 1 of this register. Bit 1 must be set up prior to writing a 1 to this register. Thus, two write operations are required to initiate a reset using this bit. The first write operation programs bit 1 to the appropriate state while setting this bit to 0. The second write operation keeps bit 1 at the programmed state (1 or 0) while setting this bit to a 1. When RCPU transitions from a 0 to a 1, a hard reset is initiated if bit 1 = 1 and a soft reset is initiated if bit 1 = 0.
1	**SYSTEM HARD RESET ENABLE (SHRE)—R/W:** This bit is used in conjunction with bit 2 of this register to initiate either a hard or soft reset. When SHRE = 1, the PCMC initiates a hard reset to the CPU when bit 2 transitions from 0 to 1. When SHRE = 0, the PCMC initiates a soft reset when bit 2 transitions from 0 to 1.
0	**DETURBO MODE (DM)—R/W:** This bit enables and disables deturbo mode. When DM = 1, the PCMC is in the deturbo mode. In this mode, the PCMC periodically asserts the AHOLD signal to slow down the effective speed of the CPU. The AHOLD duty cycle is programmable through the Deturbo Frequency Control (DFC) Register. When DM = 0, the deturbo mode is disabled. Deturbo mode can be used to maintain backward compatibility with older software packages that rely on the operating speed of older processors. For accurate speed emulation, caching should be disabled. If caching is disabled during runtime, the following steps should be performed to make sure that modified lines have been flushed from the cache to main memory before entering deturbo mode. Disable the primary cache via the PCE bit in the HCS Register. This prevents the KEN# signal from being asserted, which prevents any further first and second level cache line fills. At this point, software executes the WBINVD instruction to flush the caches, and then sets DM to 1. When exiting the deturbo mode, the system software must first set DM to 0, then enable first and second level caching by writing to the HCS Register.

3.1.4 FORW—FORWARD REGISTER

I/O Address: 0CFAh
Default Value: 00h
Attribute: Read/Write
Size: 8 Bits

This 8-bit register specifies which PCI Bus configuration space is enabled in a multiple PCI Bus configuration. The default value for the FORW Register enables the configuration space of the PCI Bus connected to the PCMC.

Bit	Description
7:0	**FORWARD BUS NUMBER—R/W:** When this register value is 00h, the configuration space of the PCI Bus connected to the PCMC is enabled and the PCMC initiates a type 0 configuration cycle. If the value of this register is not 00h, the PCMC initiates a type 1 configuration cycle to forward the cycle (via one or more PCI/PCI Bridges) to the PCI Bus specified by the contents of this register. For non-zero values, bits[7:0] are mapped to AD[23:16], respectively.

3.1.5 PMC—PCI MECHANISM CONTROL REGISTER

I/O Address: 0CFBh
Default Value: 00h
Access: Read/Write
Size: 8 bits

The PMC Register selects whether PCI Configuration Access Mechanism 1 or 2 is to be used. The register is located in the CPU I/O address space.

Bit	Description
7:1	**RESERVED**
0	**PCI CONFIGURATION ACCESS MECHANISM SELECT (PCAMS)—R/W:** When PCAMS = 0, the PCMC uses to PCI Configuration Access Mechanism #2. When PCAMS = 1, the PCMC uses to PCI Configuration Access Mechanism #1. The CONFADD and CONFDATA Registers are only accessible when PCAMS = 1.

3.1.6 CONFDATA—CONFIGURATION DATA REGISTER

I/O Address: 0CFCh
Default Value: 00h
Access: Read/Write
Size: 32 bits

CONFDATA is a 32 bit read/write window into configuration space. The portion of configuration space that is referenced by CONFDATA is determined by the contents of CONFADD.

Bit	Description
31:0	**CONFIGURATION DATA WINDOW (CDW)—R/W:** When using Configuration Access Mechanism #1 if bit 31 of CONFADD is 1 any I/O reference that falls in the CONFDATA I/O space will be mapped to configuration space using the contents of CONFADD.

3.2 PCI Configuration Space Mapped Registers

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space—**Configuration Read** and **Configuration Write**. While memory and I/O spaces are supported by the Pentium processor, configuration space is not supported. For PCI configuration space access, the PCMC translates the Pentium processor I/O cycles into PCI configuration cycles. Table 1 shows the PCMC configuration space.

Table 1. PCMC Configuration Space

Address Offset	Register Symbol	Register Name	Access
00–01h	VID	Vendor Identification	RO
02–03h	DID	Device Identification	RO
04–05h	PCICMD	Command Register	R/W
06–07h	PCISTS	Status Register	RO, R/WC
08h	RID	Revision Identification	RO
09h	RLPI	Register-Level Programming Interface	RO
0Ah	SCCD	Sub-Class Code	RO
0Bh	BCCD	Base Class Code	RO
0Ch	—	Reserved	—
0Dh	MLT	Master Latency Timer	R/W
0Eh	—	Reserved	—
0Fh	BIST	BIST Register	RO
10–4Fh	—	Reserved	—
50h	HCS	Host CPU Selection	R/W
51h	DFC	Deturbo Frequency Control	R/W
52h	SCC	Secondary Cache Control	R/W
53h	HBC	Host Read/Write Buffer Control	R/W
54h	PBC	PCI Read/Write Buffer Control	R/W
55h	—	Reserved	—
56h	—	Reserved	—
57h	DRAMC	DRAM Control	R/W
58h	DRAMT	DRAM Timing	R/W
59–5Fh	PAM[6:0]	Programmable Attribute Map (7 Registers)	R/W
60–65h	DRB[5:0]	DRAM Row Boundary (6 Registers)	R/W
66–67h	DRB[7:6]	DRAM Row Boundary (2 Registers)	R/W
68–6Bh	DRBE	DRAM Row Boundary Extension	R/W
6C–6Fh	—	Reserved	—
70h	ERRCMD	Error Command	R/W

Table 1. PCMC Configuration Space (Continued)

Address Offset	Register Symbol	Register Name	Access
71h	ERRSTS	Error Status	R/WC
72h	SMRS	SMRAM Space Control	R/W
73–77h	—	Reserved	—
78–79h	MSG	Memory Space Gap	R/W
7A–7B	—	Reserved	—
7C–7Fh	FBR	Frame Buffer Range	R/W
80–FFh	—	Reserved	—

NOTE:
Shaded rows indicate register differences between the 82434LX and 82434NX devices. For non-shaded rows, the registers are the same for the two devices.

3.2.1 CONFIGURATION SPACE ACCESS MECHANISM

The 82434LX supports Configuration Space Access Mechanism #2 and the 82434NX supports both configuration space access mechanisms #1 and #2. The mechanism is selected via the PCAMS bit in the PMC Register. The bus cycles used to access PCMC internal configuration registers are described in Section 7.0, PCI Interface.

3.2.1.1 Access Mechanism #1:

For configuration access mechanism #1, the 82434NX PCMC uses the CONFADD and CONFDATA Registers. Note that while the CONFADD and PMC Register address spaces overlap, the CONFADD Register is referenced only by a Dword read or write to CF8h. This allows the PMC Register to be accessed by a byte write to CFBh, even when using configuration access mechanism #1.

To reference a configuration register with access mechanism #1, a Dword I/O write loads the CONFADD Register with a 32-bit value that specifies the PCI Bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed (Figure 4). Bit 31 of the CONFADD Register must be 1 to enable a configuration cycle. CONFDATA then becomes a four byte window of configuration space specified by the contents of the CONFADD Register. A read or write to CONFDATA results in the PCMC translating CONFADD into a PCI configuration cycle.

Type 0 Access

If the BUSNUM field is 0, a Type 0 configuration cycle is performed on the PCI. Bus CONFADD[10:2] are mapped directly to AD[10:2]. The DEVNUM field is decoded onto AD[31:17] and AD[15:11] (for accesses to device 1, AD17 is asserted; for accesses to device #2, AD18 is asserted; etc.). The PCMC is Device #0 and does not pass its configuration cycles to the PCI Bus. Thus, AD16 is never asserted. For accesses to device 15, AD31 is asserted, etc. This mapping allows the same Device Number to activate the same AD line in either configuration access mechanism. All other AD lines are 0.

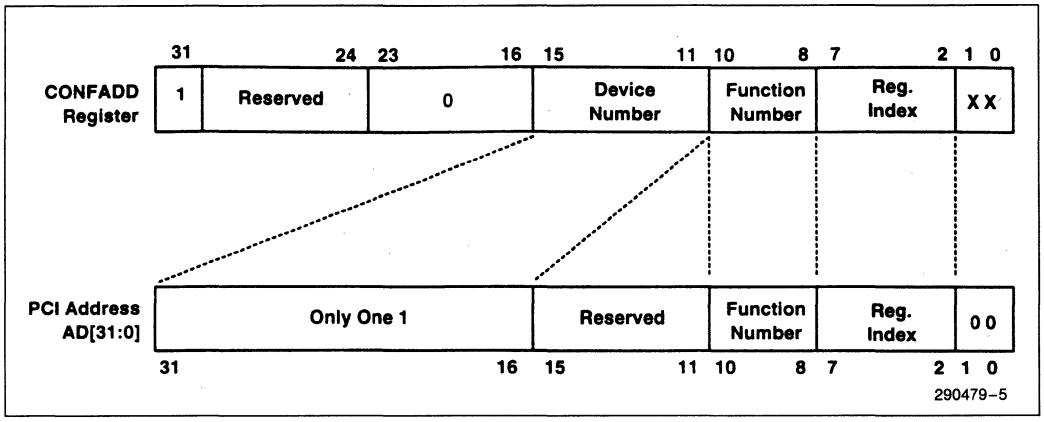


Figure 4. Mechanism #1 Type 0 Configuration Address to PCI Address Mapping

Type 1 Access

If the BUSNUM field of the CONFADD Register is non-zero, a Type 1 configuration cycle is performed on the PCI Bus. CONFADD[23:2] are mapped directly to AD[23:2] (Figure 5). AD[1:0] are driven to 01 to indicate a Type 1 Configuration cycle. All other lines are driven to 0.

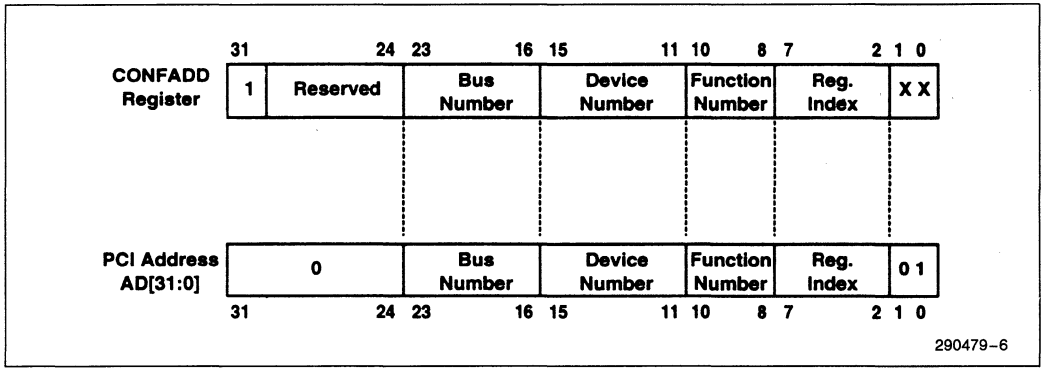


Figure 5. Mechanism #1 Type 1 Configuration Address to PCI Address Mapping

3.2.1.2 Access Mechanism #2

The 82434LX/82434NX PCMC uses the CSE and Forward Registers for configuration access mechanism #2. When PCI configuration space is enabled via the CSE Register, the PCMC maps PCI configuration space into 4-KBytes of CPU I/O space. Each PCI device has its own 256-Byte configuration space. When configuration space is enabled, CPU accesses to I/O locations CXXXh are translated into configuration space accesses. In this mode, the PCMC translates all I/O cycles in the C100h–CFFFh range into configuration cycles on the PCI Bus. I/O accesses within the C000h–C0FFh range are intercepted by the PCMC and are directed to the PCMC internal configuration registers. These cycles are not forwarded to the PCI Bus.

When configuration space access is disabled, CPU accesses to I/O locations CXXXh are forwarded to the PCI Bus I/O space. CPU cycles to I/O locations other than CXXXh are unaffected by whether the configuration mode is enabled or disabled. These cycles are always treated as ordinary I/O cycles by the PCMC.

Type 0 Access

If the Forward Register contains 00h a Type 0 configuration access is generated on the PCI Bus (Figure 6). For type 0 configuration cycles, AD[1:0] = 00. Host CPU address bits A[7:2] are not translated and become AD[7:2] on the PCI Bus. AD[7:2] select one of the 256 8-bit I/O locations in the PCI configuration space. The FUNCTION NUMBER field from the CSE Register (CSE[3:1]) is driven on AD[10:8]. Host CPU address bits A[11:8] are mapped to an IDSEL input for each of the 16 possible PCI devices. The IDSEL input for each PCI device must be hard-wired to one of the AD[31:16] signals on the PCI Bus. AD16 is reserved for the PCMC. When CPU address A[11:8] = Fh, PCI address bits A31 = 1 and A[30:16] = 00h. Other devices on the PCI Bus should not use AD16. Note that when A[11:8] = 0h, an access to the PCMC internal registers occurs and the cycle is not forwarded to the PCI Bus.

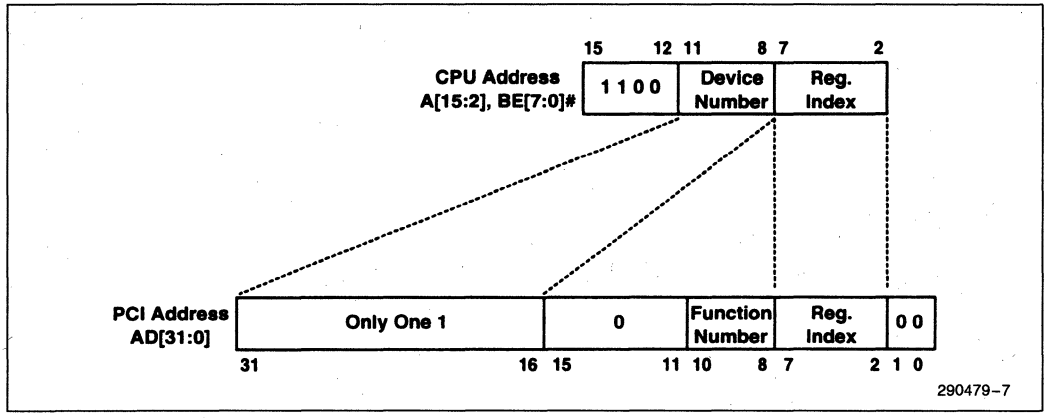


Figure 6. Mechanism #2 Type 0 Host-to-PCI Address Mapping

Type 1 Access

If the Forward Register is non-zero a Type 1 configuration access is generated on PCI. For type 1 configuration cycles, AD[1:0] = 01. AD[10:2] are generated the same as for the type 0 configuration cycle. Host CPU address bits A[11:8] contain the specific device number and are mapped to AD[14:11]. AD[23:16] contain the Bus Number of the PCI Bus that is to be accessed and corresponds to the Forward Address Register bits [7:0].

During a Type 1 configuration access AD[1:0] = 01 (Figure 7). The Register Index and Function Number are mapped to the AD lines the same way in Type 1 configuration access as in a Type 0 configuration access. CPU address bits A[11:8] are mapped directly to PCI lines AD[14:11] as the Device Number. The contents of the Forward Register are mapped to AD[23:16] to form the Bus Number.

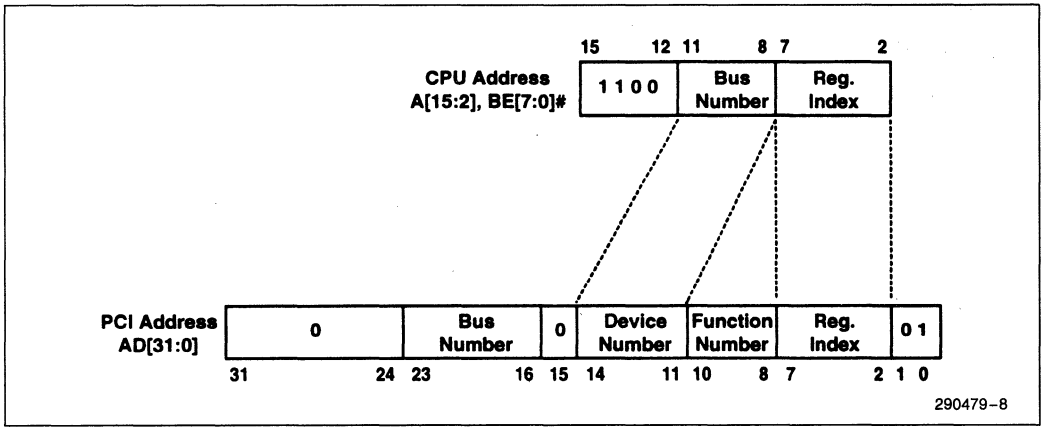


Figure 7. Mechanism #2 Type 1 Host-to-PCI Address Mapping

3.2.2 VID—VENDOR IDENTIFICATION REGISTER

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device. Writes to this register have no effect.

Bits	Description
15:0	**VENDOR IDENTIFICATION NUMBER:** This is a 16-bit value assigned to Intel.

3.2.3 DID—DEVICE IDENTIFICATION REGISTER

Address Offset: 02–03h
Default Value: 04A3h
Attribute: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bits	Description
15:0	**DEVICE IDENTIFICATION NUMBER:** This is a 16 bit value assigned to the PCMC.

3.2.4 PCICMD—PCI COMMAND REGISTER

Address Offset: 04–05h
Default: 06h
Attribute: Read/Write
Size: 16 bits

This 16-bit register provides basic control over the PCMC's ability to respond to PCI cycles. The PCICMD Register enables and disables the SERR# signal, the parity error signal (PERR#), PCMC response to PCI special cycles, and enables and disables PCI master accesses to main memory.

Bits	Description
15:9	**RESERVED**
8	**SERR# ENABLE (SERRE):** SERRE enables/disables the SERR# signal. When SERRE = 1 and PERRE = 1, SERR# is asserted if the PCMC detects a PCI Bus address/data parity error, or main memory (DRAM) or cache parity error, and the corresponding errors are enabled in the Error-Command Register. When SERRE = 1 and bit 7 in the Error Command Register is set to 1, the PCMC asserts SERR# when it detects a target abort on a PCMC-initiated PCI cycle. When SERRE = 0, SERR# is never asserted.
7	**RESERVED**
6	**PARITY ERROR ENABLE (PERRE):** PERRE controls the PCMC's response to PCI parity errors. This bit is a master enable for bit 3 of the ERRCMD Register. PERRE works in conjunction with the SERRE bit to enable SERR# assertion when the PCMC detects a PCI bus parity error, or a main memory or cache parity error.
5:3	**RESERVED**
2	**BUS MASTER ENABLE (BME):** The PCMC does not support disabling of its bus master capability on the PCI Bus. This bit is always set to 1, permitting the PCMC to function as a PCI Bus master. Writes to this bit position have no affect.
1	**MEMORY ACCESS ENABLE (MAE):** This bit enables/disables PCI master access to main memory (DRAM). When MAE = 1, the PCMC permits PCI masters to access main memory if the MEMCS# signal is asserted. When MAE = 0, the PCMC does not respond to PCI master main memory accesses (MEMCS# asserted).
0	**I/O ACCESS ENABLE (IOAE):** The PCMC does not respond to PCI I/O cycles, hence this command is not supported. PCI master access to I/O space on the Host Bus is always disabled.

3.2.5 PCISTS—PCI STATUS REGISTER

Address Offset: 06–07h
Default Value: 40h
Attribute: Read Only, Read/Write Clear
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI master abort, PCI target abort, and DRAM or cache parity error. PCISTS also indicates the DEVSEL# timing that has been set by the PCMC hardware. Bits[15:12] are read/write clear and bits[10:9] are read only.

Bits	Attribute	Description
15		**RESERVED**
14	R/WC	**SIGNALED SYSTEM ERROR (SSE):** When the PCMC asserts the SERR# signal, this bit is also set to 1. Software sets SSE to 0 by writing a 1 to this bit.
13	R/WC	**RECEIVED MASTER ABORT STATUS (RMAS):** When the PCMC terminates a Host-to-PCI transaction (PCMC is a PCI master), which is not a special cycle, with a master abort, this bit is set to 1. Software resets this bit to 0 by writing a 1 to it.
12	R/WC	**RECEIVED TARGET ABORT STATUS (RTAS):** When a PCMC-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. The PCMC also asserts SERR# if the SERR# Target Abort bit in the ERRCMD Register is 1. Software resets RTAS to 0 by writing a 1 to it.
11		**RESERVED**
10:9	RO	**DEVSEL# TIMING (DEVT):** This 2-bit field indicates the timing of the DEVSEL# signal when the PCMC responds as a target. The PCI specification defines three allowable timings for assertion of DEVSEL#: 00 = fast, 01 = medium, and 10 = slow (DEVT = 11 is reserved). DEVT indicates the slowest time that a device asserts DEVSEL# for any bus command, except configuration read and write cycles. Note that these two bits determine the slowest time that the PCMC asserts DEVSEL#. However, the PCMC can also assert DEVSEL# in medium time. The PCMC asserts DEVSEL# in response to sampling MEMCS# asserted. The PCMC samples MEMCS# one and two clocks after FRAME# is asserted. If MEMCS# is asserted one PCI clock after FRAME# is asserted, then the PCMC responds with DEVSEL# in slow time.
8	R/WC	**DATA PARITY DETECTED (DPD):** This bit is set to 1 when all of the following conditions are met: 1). The PCMC asserted PERR# or sampled PERR# asserted. 2). The PCMC was the bus master for the operation in which the error occurred. 3). The PERRE bit in the Command Register is set to 1. Software resets DPD to 0 by writing a 1 to it.
7:0		**RESERVED**

3.2.6 RID—REVISION IDENTIFICATION REGISTER

Address Offset: 08h
Default Value: 03h for A–3 Stepping (82434LX)
01h for A–1 Stepping (82434LX)
10h for A–0 Stepping (82434NX)
11h for A–1 Stepping (82434NX)
Attribute: Read Only
Size: 8 bits

This register contains the revision number of the PCMC. These bits are read only and writes to this register have no effect. For the A–2 Stepping of the 82434LX, this value is 03h.

For the A–1 Stepping of the 82434NX, this value is 11h.

Bits	Description
7:0	**REVISION IDENTIFICATION NUMBER:** This is an 8-bit value that indicates the revision identification number for the PCMC.

3.2.7 RLPI—REGISTER-LEVEL PROGRAMMING INTERFACE REGISTER

Address Offset: 09h
Default Value: 00h
Attribute: Read Only
Size: 8 bits

This register defines the PCMC as having no defined register-level programming interface.

Bits	Description
7:0	**REGISTER-LEVEL PROGRAMMING INTERFACE (RLPI):** The value of 00h defines the PCMC as having no defined register-level programming interface.

3.2.8 SUBC—SUB-CLASS CODE REGISTER

Address Offset: 0Ah
Default Value: 00h
Attribute: Read Only
Size: 8 bits

This register defines the PCMC as a host bridge.

Bits	Description
7:0	**SUB-CLASS CODE (SCCD):** The value of this register is 00h defining the PCMC as host bridge.

3.2.9 BASEC—BASE CLASS CODE REGISTER

Address Offset: 0Bh
Default Value: 06h
Attribute: Read Only
Size: 8 bits

This register defines the PCMC as a bridge device.

Bits	Description
7:0	**BASE CLASS CODE (BCCD):** The value in this register is 06h defining the PCMC as bridge device.

3.2.10 MLT—MASTER LATENCY TIMER REGISTER

Address Offset: 0Dh
Default Value: 20h
Attribute: Read/Write
Size: 8 bits

MLT is an 8-bit register that controls the amount of time the PCMC, as a bus master, can burst data on the PCI Bus. MLT is used when the PCMC becomes the PCI Bus master and is cleared and suspended when the PCMC is not asserting FRAME#. When the PCMC asserts FRAME#, the counter is enabled and begins counting. If the PCMC finishes its transaction before the count expires, the MLT count is ignored. If the count expires before the transaction completes, the PCMC initiates a transaction termination as soon as its GNT# is removed. The number of clocks programmed in the MLT represents the guaranteed time slice (measured in PCI clocks) allotted to the PCMC, after which it must surrender the bus as soon as its GNT# is taken away. The number of clocks in the Master Latency Timer is the count value field multiplied by 16.

Bits	Description
7:4	**MASTER LATENCY TIMER COUNT VALUE:** If GNT# is negated after the burst cycle is initiated, the PCMC limits the duration of the burst cycle to the number of PCI Bus clocks specified by this field multiplied by 16.
3:0	**RESERVED**

3.2.11 BIST—BIST REGISTER

Address Offset: 0Fh
Default Value: 0h
Attribute: Read Only
Size: 8 bits

The BIST function is not supported by the PCMC. Writes to this register have no affect.

Bits	Attribute	Description
7	RO	**BIST SUPPORTED:** This read only bit is always set to 0, disabling the BIST function. Writes to this bit position have no affect.
6	RW	**START BIST:** This function is not supported and writes have no affect.
5:4		**RESERVED**
3:0	RO	**COMPLETION CODE:** This read only field always returns 0 when read and writes have no affect.

3.2.12 HCS—HOST CPU SELECTION REGISTER

Address Offset: 50h
Default Value: 82h (82434LX)
A2h (83434NX)
Access: Read/Write, Read Only
Size: 8 bits

The HCS Register is used to specify the Host CPU type and speed. This 8-bit register is also used to enable and disable the first level cache.

Bits	Access	Description
7:5	RO	**HOST CPU TYPE (HCT):** This field defines the Host CPU type. **82434LX** These bits are hardwired to 100 which selects the Pentium processor. All other combinations are reserved. **82434NX** In the 82434NX, these bits are reserved. Reads and writes to these bits have no effect.
4:3		**RESERVED**
2	R/W	**FIRST LEVEL CACHE ENABLE (FLCE):** FLCE enables and disables the first level cache. When FLCE = 1, the PCMC responds to CPU cycles with KEN# asserted for cacheable memory cycles. When FLCE = 0, KEN# is always negated. This prevents new cache line fills to either the first level or second level caches.
1:0	R/W	**HOST OPERATING FREQUENCY (HOF):** The DRAM refresh rate is adjusted according to the frequency selected by this field. For the 82434LX, only bit 0 is used and bit 1 is reserved. **82434LX** Bit 1 is reserved. If bit 0 is 1, the 82434LX supports a 66 MHz CPU. If bit 0 is 0, the 82434LX supports a 60 MHz CPU. **82434NX** These bits select the Host CPU frequency supported as follows: **Bits[1:0] Host CPU Frequency** 00 Reserved 01 50 MHz 10 60 MHz 11 66 MHz

3.2.13 DFC—DETURBO FREQUENCY CONTROL REGISTER

Address Offset: 51h
Default Value: 80h
Attribute: Read/Write
Size: 8 bits

Some software packages rely on the operating speed of the processor to time certain system events. To maintain backward compatibility with these software packages, the PCMC provides a mechanism to emulate a slower operating speed. This emulation is achieved with the PCMC's deturbo mode. The deturbo mode is enabled and disabled via the DM bit in the Turbo-Reset Control Register. When the deturbo mode is enabled, the PCMC periodically asserts AHOLD to slow down the effective speed of the CPU. The duty cycle of the AHOLD active period is controlled by the DFC Register.

Bits	Description
7:6	**DETURBO MODE FREQUENCY ADJUSTMENT VALUE:** This 8-bit value effectively defines the duty cycle of the AHOLD signal. DFC[7:6] are programmable and DFC[5:0] are 0. The value programmed into this register is compared against a free running 8-bit counter running at 1/8 the CPU clock. When the counter is greater than the value specified in this register, AHOLD is asserted. AHOLD is negated when the counter value is equal to or smaller than the contents of this register. AHOLD is negated when the counter rolls over to 00h. The deturbo emulation speed is directly proportional to the value in this register. Smaller values in this register yield slower deturbo emulation speed. The value of 00h is reserved.
5:0	**RESERVED**

3.2.14 SCC—SECONDARY CACHE CONTROL REGISTER

Address Offset: 52h
Default Value: SSS01R10 (82434LX)
SSS01010 (82434NX)
(S = Strapping option)
Attribute: Read/Write
Size: 8 bits

This 8-bit register defines the secondary cache operations. The SCC Register enables and disables the second level cache, adjusts cache size, selects the cache write policy, and defines the cache SRAM type. After hard reset, SCC[7:5] contain the opposite of the signal levels sampled on the Host address lines A[31:29].

Bits	Description
7:6	**SECONDARY CACHE SIZE (SCS):** This field defines the size of the second level cache. The values sampled on the A[31:30] lines at the rising edge of the PWROK signal are inverted and stored in this field. **Bits[7:6] — Secondary Cache Size** 00 — Cache not populated 01 — Reserved 10 — 256-KBytes 11 — 512-KBytes

Bits	Description
5	**SRAM TYPE (SRAMT):** This bit selects between standard SRAMs or burst SRAMS to implement the second level cache. When SRAMT = 0, standard SRAMs are selected. When SRAMT = 1, burst SRAMs are selected. This bit reflects the signal level on the A29 pin at the rising edge of the PWROK signal. This value can be overwritten with subsequent writes to the SCC Register.
4	**82434LX: SECONDARY CACHE ALLOCATION (SCA):** SCA controls when the PCMC performs line fills in the second level cache. When SCA is set to 0, only CPU reads of cacheable main memory with CACHE# asserted are cached in the second level cache. When SCA is set to 1, all CPU reads of cacheable main memory are cached in the second level cache.
3	**CACHE BYTE CONTROL (CBC):** When programmed for asynchronous SRAMs, this bit defines whether the cache uses individual write enables per byte or has a single write enable and byte select lines per byte. When CBC is set to 1, write enable control is used. When CBC is set to 0, byte select control is used.
2	**82434LX: RESERVED** **82434NX: SRAM CONNECTIVITY (SRAMC):** This bit enables different connectivities for the second level cache. When SRAMC is set to 0, the second level cache is in 82434LX compatible mode and all connections between the PCMC and second level cache SRAMs are the same as the 82434LX. When asynchronous SRAMs are used, setting this bit to 1 enables the CCS[1:0]# functionality. CCS[1:0]# are used with asynchronous SRAMs to de-select the SRAMs, placing them in a low power standby mode. When the CPU runs a halt or stop grant special cycle, the 82434NX negates CCS[1:0]#, placing the second level cache in a power saving mode. The PCMC then asserts CCS[1:0]# (activating the SRAMs) when the CPU asserts ADS#. When using burst SRAMs, setting this bit to 1 enables the CCS1# functionality and indicates to the PCMC that no external address latch is present.
1	**82434LX: SECONDARY CACHE WRITE POLICY (SCWP):** SCWP selects between write-back and write-through cache policies for the second level cache. When SCWP = 0 and the second level cache is enabled (bit 0 = 1), the second level cache is configured for write-through mode. When SCWP = 1 and the second level cache is enabled (bit 0 = 1), the second level cache is configured for write-back mode. **82434NX: RESERVED:** Secondary cache write-through mode is not supported. The secondary cache is always in write-back mode and this bit has no affect. SCWP can be set to 0, however, the 82434NX will still operate the secondary cache in write-back mode.
0	**SECONDARY CACHE ENABLE (SCE):** SCE enables and disables the secondary cache. When SCE = 1, the secondary cache is enabled. When SCE = 0, the secondary cache is disabled. When the secondary cache is disabled, the PCMC forwards all main memory cycles to the DRAM interface. Note that setting this bit to 0 does not affect existing valid cache lines. If a cache line contains modified data, the data is not written back to memory. Valid lines in the cache remain valid. When the secondary cache is disabled, the CWE[7:0]# lines remain negated. COE[1:0]# may still toggle. When system software disables secondary caching through this register during run-time, the software should first flush the second level cache. This process is accomplished by first disabling first level caching via the PCE bit in the HCS Register. This prevents the KEN# signal from being asserted, which disables any further line fills. At this point, software executes the WBINVD instruction to flush the caches. When the instruction completes, bit 0 of this register can be reset to 0, disabling the secondary cache. The first level cache can then be enabled by writing the PCE bit in the HCS Register.

3.2.15 HBC—HOST READ/WRITE BUFFER CONTROL

Address Offset: 53h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The HBC Register enables and disables Host-to-main memory and Host-to-PCI posting of write cycles. When posting is enabled, the write buffers in the LBX devices post the data that is destined for either main memory or PCI. This register also permits a CPU-to-main memory read cycle to be performed before any pending posted write data is written to memory.

Bits	Description
7:4	**RESERVED**
3	**READ-AROUND-WRITE ENABLE (RAWCM):** If enabled, the PCMC, during a CPU read cycle to memory where posted write cycles are pending, internally snoops the write buffers. If the address of the read differs from the posted write addresses, the PCMC initiates the memory read cycle ahead of the pending posted memory write. When RAWCM = 0, the pending posted write is written to memory before the memory read is performed. When RAWCM = 1, the PCMC initiates the memory read ahead of the pending posted memory writes.
2	**RESERVED**
1	**HOST-TO-PCI POSTING ENABLE (HPPE):** This bit enables/disables the posting of Host-to-PCI write data in the LBX posting buffers. When HPPE = 1, up to 4 Dwords of data can be posted to PCI. HPPE = 0 is reserved. Buffering is disabled and each CPU write does not complete until the PCI transaction completes (TRDY# is asserted).
0	**82434LX: HOST-TO-MEMORY POSTING ENABLE (HMPE):** This bit enables/disables the posting of Host-to-main memory write data in the LBX buffers. When HMPE = 1, the CPU can post a single write or a burst write (4 Qwords). The CPU burst write completes at 4-1-1-1 when the second level cache is in write-back mode and at 3-1-1-1 when the second level cache is either disabled or in write-through mode. When HMPE = 0, Host-to-main memory posting is disabled and the CPU write cycles do not complete until the data is written to memory. **82434NX: RESERVED:** For the 82434NX, posting is always enabled and this bit has no affect. The CPU can post a single write or burst write (4 Qwords). HMPE can be set to 0, however, the 82434NX will still allow posting of CPU-to-main memory writes.

3.2.16 PBC—PCI READ/WRITE BUFFER CONTROL REGISTER

Address Offset: 54h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The PBC Register enables and disables PCI-to-main memory write posting and permits single CPU-to-PCI writes to be assembled into PCI burst cycles.

Bits	Description
7:3	**RESERVED**
2	**LBXs CONNECTED TO TRDY#:** The TRDY# pin on the LBXs can be connected either to the PCI TRDY# signal or to ground. The cycle time for CPU-to-PCI writes is improved if TRDY# is connected to the LBXs. Since there are two LBXs used in a system, connecting this signal to the LBXs increases the electrical loading of TRDY# by two loads. When the LBXs are externally hard-wired to TRDY#, this bit should be set to 1. Note that this should be done prior to the first Host-to-PCI write or data corruption will occur. Setting this bit to 1 enables the capability of CPU-to-PCI writes at 2-1-1-1 . . . (PCI clocks). When this bit is 0, the LBXs are not connected to TRDY# and CPU-to-PCI writes are completed at 2-2-2-2 . . . timing.
1	**PCI BURST WRITE ENABLE (PBWE):** This bit enables and disables PCI Burst memory write cycles for back-to-back sequential CPU memory write cycles to PCI. When PBWE is set to 1, PCI burst writes are enabled. When PBWE is reset to 0, PCI burst writes are disabled and each single CPU write to PCI invokes a single PCI write cycle (each cycle has an associated FRAME# sequence).
0	**PCI-TO-MEMORY POSTING ENABLE (PMPE):** This bit enables and disables posting of PCI-to-memory write cycles. The posting occurs in a pair of four Dword-deep buffers in the LBXs. When PMPE is set to 1, these buffers are used to post PCI-to-main memory write data. When PMPE is reset to 0, PCI write transactions to main memory are limited to single transfers. The PCMC asserts STOP# with the first TRDY# to disconnect the PCI Master.

3.2.17 DRAMC—DRAM CONTROL REGISTER

Address Offset: 57h
Default Value: 31h
Attribute: Read/Write
Size: 8 bits

This 8-bit register controls main memory DRAM operating modes and features.

Bits	Description
7:6	**82434LX: RESERVED** **82434NX: DRAM BURST TIMING (DBT):** The DRAM interface can be configured for 3 different burst timings. The CAS# pulse width for X-3-3-3 timing is one clock shorter than the CAS# pulse width for X-4-4-4 timing. **Bits[7:6] Burst Timing** 0 0 X-4-4-4 Read/Write timing (default) 0 1 X-4-4-4 Read, X-3-3-3 Write timing 1 0 Reserved 1 1 X-3-3-3 Read/Write timing
5	**PARITY ERROR MASK (PERRM):** When PERRM = 1, parity errors generated during DRAM read cycles initiated by either the CPU request or a PCI Master are masked. This bit affects bits 0 and 1 of the Error Command Register and the ability of the PCMC to respond to PCHK# and assert SERR# when a DRAM parity error occurs. When PERRM is reset to 0, parity errors are not masked.
4	**0-ACTIVE RAS# MODE:** This bit determines if the DRAM page for a particular row remains open (i.e. RAS# remains asserted after a DRAM cycle) enabling the possibility that the next DRAM access may be either a page hit, a page miss, or a row miss. The DRAM interface is then in 1-active RAS# mode. If this bit is reset to 0, RAS# remains asserted after a DRAM cycle. If this bit is set to 1, RAS# is negated after every DRAM cycle, resulting in a row miss for every DRAM cycle. The DRAM interface is then in 0-active RAS# mode.
3	**SMRAM ENABLE (SMRE):** When SMRE = 1, CPU accesses to SMM space are qualified with the SMIACT# pin of the CPU. The location of this space is determined by the SBS field of the SMRAM Register. Read and write cycles to SMM space function normally if SMIACT# is asserted. If SMIACT# is negated when accessing this space, the cycle is forwarded to PCI. When SMRE = 0, accesses to SMM space are treated normally and SMIACT# has no effect. SMRE must be set to 1 to enable the use of the SMRAM Register at configuration space offset 72h.
2	**BURST OF FOUR REFRESH (BFR):** When BFR is set to 1, refreshes are performed in sets of four, at a frequency 1/4 of the normal refresh rate. The PCMC defers refreshes to idle times, if possible. When BFR is reset to 0, single refreshes occur at 15.6 μs refresh rate.
1	**82434LX: REFRESH TYPE (RT):** When RT = 1, the PCMC uses CAS#-before-RAS# timing to refresh the DRAM array. For this refresh type, the PCMC does not supply refresh addresses. When RT = 0, RAS# Only refresh is used and the PCMC drives refresh addresses on the MA[10:0] lines. RAS# only refresh can be used with any type of second level cache configuration (i.e., no second level cache is present, or either a burst SRAM or standard SRAM second level cache is implemented). CAS#-before-RAS# refresh should not be used when a standard SRAM second level cache is implemented. **82434NX: REFRESH TYPE (RT):** In addition to above, when RT = 0, RAS# only refresh is used and the PCMC drives refresh addresses on the MA[11:0] lines. Also, CAS#-before-RAS# refresh can be used with a standrad SRAM second level cache.
0	**REFRESH ENABLE (RE):** When RE is set to 1, the main memory array is refreshed as configured via bits 1 and 2 of this register. When RE is reset to 0, DRAM refresh is disabled. Note that disabling refresh results in the loss of DRAM data.

3.2.18 DRAMT—DRAM TIMING REGISTER

Address Offset: 58h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

For the 82434LX, this register controls the leadoff latency for CPU DRAM accesses.

For the 82434NX, this register provides additional control over DRAM timings. One additional wait-state can be independently added before the assertion of RAS#, the assertion of the first CAS#, or both. This is to allow more flexibility in the layout of the motherboard and in the selection of DRAM speed grades.

Bits	Description
7:2	**RESERVED**
1	**82434LX: RESERVED** **82434NX: RAS# WAIT-STATE (RWS):** When RWS = 1, one additional wait state will be inserted before RAS# is asserted for row misses or page misses in 1-Active RAS mode and all cycles in 0-Active RAS mode. This provides additional MA[11:0] setup time to RAS# assertion.
0	**CAS# WAIT-STATE (CWS):** When CWS = 1, one additional wait state will be inserted before the first assertion of CAS# within a burst cycle. There is no additional delay between CAS# assertions. This provides additional MA[11:0] setup time to CAS# assertion. The CWS bit is typically reset to 0 for 60 MHz operation and set to 1 for 66 MHz operation.

3.2.19 PAM—PROGRAMMABLE ATTRIBUTE MAP REGISTERS (PAM[6:0])

Address Offset: 59–5Fh
Default Value: PAM0 = 0Fh, PAM[1:6] = 00h
Attribute: Read/Write

The PCMC allows programmable memory and cacheability attributes on 14 memory segments of various sizes in the 512 KByte–1 MByte address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Three bits are used to specify cacheability and memory attributes for each memory segment. These attributes are:

RE: **Read Enable.** When RE = 1, the CPU read accesses to the corresponding memory segment are directed to main memory. Conversely, when RE = 0, the CPU read accesses are directed to PCI.

WE: **Write Enable.** When WE = 1, the CPU write accesses to the corresponding memory segment are directed to main memory. Conversely, when WE = 0, the CPU write accesses are directed to PCI.

CE: **Cache Enable.** When CE = 1, the corresponding memory segment is cacheable. CE must not be set to 1 when RE is reset to 0 for any particular memory segment. When CE = 1 and WE = 0, the corresponding memory segment is cached in the first and second level caches only on CPU coded read cycles.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only. The characteristics for memory segments with these read/write attributes are described in Table 2.

Table 2. Attribute Definition

Read/Write Attribute	Definition
Read Only	Read cycles: CPU cycles are serviced by the DRAM in a normal manner. Write cycles: CPU initiated write cycles are ignored by the DRAM interface as well as the cache. Instead, the cycles are passed to PCI for termination. Areas marked as Read Only are cacheable for Code accesses only. These regions may be cached in the second level cache, however as noted above, writes are forwarded to PCI, effectively write protecting the data.
Write Only	Read cycles: All read cycles are ignored by the DRAM interface as well as the second level cache. CPU-initiated read cycles are passed onto PCI for termination. The write only state can be used while copying the contents of a ROM, accessible on PCI, to main memory for shadowing, as in the case of BIOS shadowing. Write cycles: CPU write cycles are serviced by the DRAM and cache in a normal manner.
Read/Write	This is the normal operating mode of main memory. Both read and write cycles from the CPU and PCI are serviced by the DRAM and cache interface.
Disabled	All read and write cycles to this area are ignored by the DRAM and cache interface. These cycles are forwarded to PCI for termination.

Each PAM Register controls two regions, typically 16-KByte in size. Each of these regions have a 4-bit field. The four bits that control each region have the same encoding and are defined in Table 3.

Table 3. Attribute Bit Assignment

Bits[7,3] Reserved	Bits[6,2] Cache Enable	Bits[5,1] Write Enable	Bits[4,0] Read Enable	Description
x	x	0	0	DRAM Disabled, Accesses Directed to PCI
x	0	0	1	Read Only, DRAM Write Protected, Non-Cacheable
x	1	0	1	Read Only, DRAM Write Protected, Cacheable for Code Accesses Only
x	0	1	0	Write Only
x	0	1	1	Read/Write, Non-Cacheable
x	1	1	1	Read/Write, Cacheable

NOTE:
To enable PCI master access to the DRAM address space from C0000h to FFFFFh the MEMCS# configuration registers of the ISA or EISA bridge must be properly configured. These registers must correspond to the PAM Registers in the PCMC.

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process the BIOS can be shadowed in main memory to increase the system performance. When a BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The CPU then does a write of the same address, which is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus.

Table 4. PAM Registers and Associated Memory Segments

PAM Reg	Attribute Bits		Memory Segment		Comments		Offset
PAM0[3:0]	R	CE	WE	RE	080000h–09FFFFh	512K–640K	59h
PAM0[7:4]	R	CE	WE	RE	0F0000h–0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	CE	WE	RE	0C0000h–0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	CE	WE	RE	0C4000h–0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	CE	WE	RE	0C8000h–0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	CE	WE	RE	0CC000h–0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	CE	WE	RE	0D0000h–0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	CE	WE	RE	0D4000h–0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	CE	WE	RE	0D8000h–0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	CE	WE	RE	0DC000h–0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	CE	WE	RE	0E0000h–0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	CE	WE	RE	0E4000h–0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	CE	WE	RE	0E8000h–0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	CE	WE	RE	0EC000h–0EFFFFh	BIOS Extension	5Fh

DOS Application Area (00000h-9FFFh)

The 640-KByte DOS application area is split into two regions. The first region is 0–512-KByte and the second region is 512–640 KByte. Read, write, and cacheability attributes are always enabled and are not programmable for the 0–512 KByte region.

Video Buffer Area (A0000h-BFFFFh)

This 128-KByte area is not controlled by attribute bits. CPU-initiated cycles in this region are always forwarded to PCI for termination. This area is not cacheable.

Expansion Area (C0000h-DFFFFh)

This 128-KByte area is divided into eight 16-KByte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled Memory that is disabled is not remapped. Cacheability status can also be specified for each segment.

Extended System BIOS Area (E0000h-EFFFFh)

This 64-KByte area is divided into four 16-KByte segments. Each segment can be assigned independent cacheability, read, and write attributes. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000h-FFFFFh)

This area is a single 64-KByte segment. This segment can be assigned cacheability, read, and write attributes. When disabled, this segment is not remapped.

Extended Memory Area (100000h-FFFFFFFFh)

The extended memory area can be split into several parts:

- Flash BIOS area from 4 GByte to 4 GByte–512-KByte (aliased on ISA at 16 MBytes–15.5 MBytes)
- DRAM Memory from 1 MByte to a maximum of 192 MBytes
- PCI Memory space from the top of DRAM to 4 GByte – 512-KByte
- Memory Space Gap between the range of 1 MByte up to 15.5 MBytes
- Frame Buffer Range mapped into PCI Memory Space or the Memory Space Gap.

On power-up or reset the CPU vectors to the Flash BIOS area, mapped in the range of 4 GByte to 4 GByte – 512-KByte. This area is physically mapped on the expansion bus. Since these addresses are in the upper 4 GByte range, the request is directed to PCI.

The DRAM memory space can occupy extended memory from a minimum of 2 MBytes up to 192 MBytes. This memory is cacheable.

The address space on PCI between the Flash BIOS (4 GByte to 4 GByte – 512 KByte) and the top of DRAM (including any remapped memory) may be occupied by PCI memory. This memory space is not cacheable.

3.2.20 DRB—DRAM ROW BOUNDARY REGISTERS

Address Offset:	60–65h (82434LX) 60–67h (82434NX)
Default Value:	02h
Attribute:	Read/Write
Size:	8 bits

Note the address offset for each DRB Register is DRB0 = 60h, DRB1 = 61h, DRB2 = 62h, DRB3 = 63h, DRB4 = 64h, DRB5 = 65h, DRB6 = 66h, and DRB7 = 67h.

3.2.20.1 82434LX Description

The PCMC supports 6 rows of DRAM. Each row is 64 bits wide. The DRAM Row Boundary Registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the boundary addresses in MBytes.

DRB0 = Total amount of memory in row 0 (in MBytes)
DRB1 = Total amount of memory in row 0 + row 1 (in MBytes)
DRB2 = Total amount of memory in row 0 + row 1 + row 2 (in MBytes)
DRB3 = Total amount of memory in row 0 + row 1 + row 2 + row 3 (in MBytes)
DRB4 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 (in MBytes)
DRB5 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 (in MBytes)

The DRAM array can be configured with 256K x 36, 1M x 36 and 4M x 36 SIMMs. Each register defines an address range that will cause a particular RAS# line to be asserted (e.g. if the first DRAM row is 2 MBytes in size then accesses within the 0 MByte–2 MBytes range will cause RAS0# to be asserted). The DRAM Row

Boundary (DRB) Registers are programmed with an 8-bit upper address limit value. This upper address limit is compared to A[27:20] of the Host address bus, for each row, to determine if DRAM is being targeted. Since this value is 8 bits and the resolution is 1 MByte, the total bits compared span a 256 MByte space. However, only 192 MBytes of main memory is supported.

Bits	Description
7:0	**ROW BOUNDARY ADDRESS IN MBYTES:** This 8-bit value is compared against address lines A[27:20] to determine the upper address limit of a particular row, i.e. DRB − previous DRB = row size.

Row Boundary Address in MBytes

These 8-bit values represent the upper address limits of the six rows (i.e., this row - previous row = row size). Unpopulated rows have a value equal to the previous row (row size = 0). The value programmed into DRB5 reflects the maximum amount of DRAM in the system. Memory remapped at the top of DRAM, as a result of setting the Memory Space Gap Register, is not reflected in the DRB Registers. The top of memory is always determined by the value written into DRB5 added to the memory space gap size (if enabled).

As an example of a general purpose configuration where 3 physical rows are configured for either single-sided or double-sided SIMMs, the memory array would be configured like the one shown in Figure 8. In this configuration, the PCMC drives two RAS# signals directly to the SIMM rows. If single-sided SIMMs are populated, the even RAS# signal is used and the odd RAS# is not connected. If double-sided SIMMs are used, both RAS# signals are used.

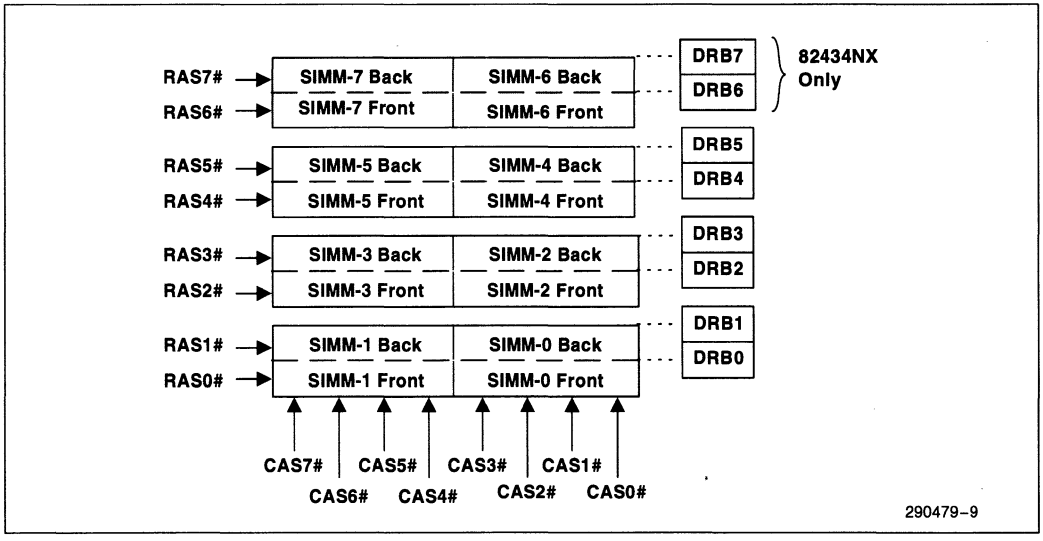


Figure 8. SIMMs and Corresponding DRB Registers

The following 2 examples describe how the DRB Registers are programmed for cases of single-sided and double-sided SIMMs on a motherboard having a total of 6 SIMM sockets.

Example #1

The memory array is populated with six single-sided 256-KByte x 36 SIMMs. Two SIMMs are required for each populated row making each populated row 2 MBytes in size. Filling the array yields 6 MBytes total DRAM. The DRB Registers are programmed as follows:

DRB0 = 02h populated
DRB1 = 02h empty row, not double-sided SIMMs
DRB2 = 04h populated
DRB3 = 04h empty row, not double-sided SIMMs
DRB4 = 06h populated
DRB5 = 06h empty row, not double-sided SIMMs, maximum memory = 6 MBytes.

Example #2

As an another example, if the first four SIMM sockets are populated with 2 MBytes x 36 double-sided SIMMs and the last two SIMM sockets are populated with 4 MBytes x 36 single-sided SIMMs then filling the array yields 64 MBytes total DRAM. The DRB Registers are programmed as follows:

DRB0 = 08h populated with 8 MBytes, ½ of the double-sided SIMMs
DRB1 = 10h the other 8 MBytes of the double-sided SIMMs
DRB2 = 18h populated with 8 MBytes, ½ of the double-sided SIMMs
DRB3 = 20h the other 8 MBytes of the double-sided SIMMs
DRB4 = 40h populated with 32 MBytes
DRB5 = 40h empty row, not double-sided SIMMs, maximum memory = 64 MBytes.

3.2.20.2 82434NX Description

The PCMC supports 8 rows of DRAM. Each row is 64 bits wide. The DRAM Row Boundary Registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers are concatenated with the associated nibble of the DRBE Register to form 12 bit quantities that represent the row boundary addresses in MBytes.

DRBE[3:0] | | DRB0 = Total amount of memory in row 0 (in MBytes)
DRBE[7:4] | | DRB1 = Total amount of memory in row 0 + row 1 (in MBytes)
DRBE[11:8] | | DRB2 = Total amount of memory in row 0 + row 1 + row 2 (in MBytes)
DRBE[15:12] | | DRB3 = Total amount of memory in row 0 + row 1 + row 2 + row 3 (in MBytes)
DRBE[19:16] | | DRB4 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 (in MBytes)
DRBE[23:20] | | DRB5 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 (in Bytes)
DRBE[27:24] | | DRB6 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 + row 6 (in MBytes)
DRBE[31:28] | | DRB7 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 + row 6 + row 7 (in MBytes)

The DRAM array can be configured with 256K x 36, 1M x 36, 4M x 36, and 16M x 36 SIMMs. Each register defines an address range that will cause a particular RAS# line to be asserted (e.g. if the first DRAM row is 2 MBytes in size then accesses within the 0 to 2 MBytes range will cause RAS0# to be asserted). The DRAM Row Boundary (DRB) Registers are programmed with an 8-bit upper address limit value. The DRBE Register extends the programming model of this mechanism to 12 bits, however only 10 bits are implemented at this time. This upper address limit is compared to A[29:20] of the Host address bus, for each row, to determine if DRAM is being targeted. Since this value is 10 bits and the resolution is 1 MByte, the total bits compared span a 1 GByte space. However, other resource limits in the PCMC cap the total usable DRAM space at 512 MBytes.

Bits	Description
7:0	**ROW BOUNDARY ADDRESS IN MBYTES:** This 8-bit value is concatenated with a nibble from the DRBE Register and then compared against address lines A[29:20] to determine the upper address limit of a particular row (i.e. DRB − previous DRB = row size).

Row Boundary Address in MBytes

These 10-bit values represent the upper address limits of the 8 rows (i.e., this row - previous row = row size). Unpopulated rows have a value equal to the previous row (row size = 0). The value programmed into DRBE[31:28] || DRB7 reflects the maximum amount of DRAM in the system. Memory remapped at the top of DRAM, as a result of setting the Memory Space Gap Register, is not reflected in the DRB Registers. The top of memory is determined by the value written into DRBE[31:28] || DRB7 added to the memory space gap size (if enabled). If DRBE[31:28] || DRB7 plus the memory space gap is greater than 512 MBytes then 512 MBytes of DRAM are available.

The following 2 examples describe how the DRB Registers are programmed for cases of single-sided and double-sided SIMMs on a motherboard having a total of 8 SIMM sockets.

Example #1

The memory array is populated with eight single-sided 256-KByte x 36 SIMMs. Two SIMMs are required for each populated row making each populated row 2 MBytes in size. Filling the array yields 8 MBytes total DRAM. The DRB Registers are programmed as follows:

DRBE[3:0] = 0h	DRB0 = 02h	populated
DRBE[7:4] = 0h	DRB1 = 02h	empty row, not double-sided SIMMs
DRBE[11:8] = 0h	DRB2 = 04h	populated
DRBE[15:12] = 0h	DRB3 = 04h	empty row, not double-sided SIMMs
DRBE[19:16] = 0h	DRB4 = 06h	populated
DRBE[23:20] = 0h	DRB5 = 06h	empty row, not double-sided SIMMs
DRBE[27:24] = 0h	DRB6 = 08h	populated
DRBE[31:28] = 0h	DRB7 = 08h	empty row, not double-sided SIMMs, max memory = 8 MBytes.

Example #2

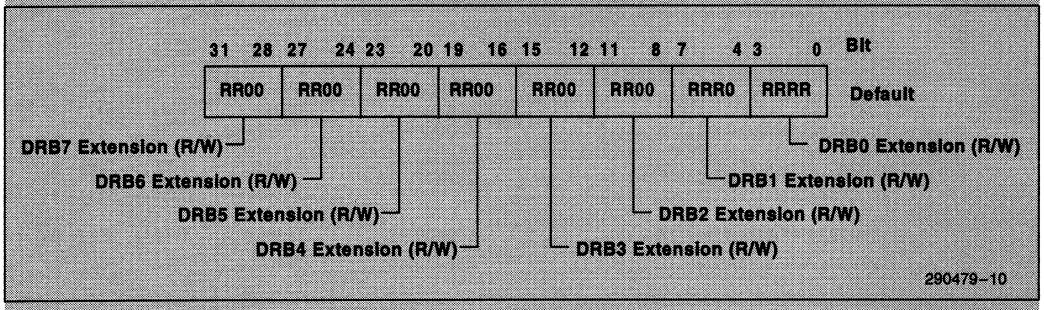
As an another example, if the first four SIMM sockets are populated with 2 MByte x 36 double-sided SIMMs and the last four SIMM sockets are populated with 16 MByte x 36 single-sided SIMMs then filling the array yields 288 MBytes total DRAM. The DRB Registers are programmed as follows:

DRBE[3:0] = 0h	DRB0 = 08h	populated with 8 MBytes, ½ of double-sided SIMMs
DRBE[7:4] = 0h	DRB1 = 10h	the other 8 MBytes of the double-sided SIMMs
DRBE[11:8] = 0h	DRB2 = 18h	populated with 8 MBytes, ½ of double-sided SIMMs
DRBE[15:12] = 0h	DRB3 = 20h	the other 8 MBytes of the double-sided SIMMs
DRBE[19:16] = 0h	DRB4 = A0h	populated with 128 MBytes
DRBE[23:20] = 0h	DRB5 = A0h	empty row, not double-sided SIMMs
DRBE[27:24] = 1h	DRB6 = 20h	populated with 128 MBytes
DRBE[31:28] = 1h	DRB7 = 20h	empty row, not double-sided SIMMs, max memory = 288 MBytes.

3.2.21 DRBE—DRAM ROW BOUNDARY EXTENSION REGISTER

Address Offset: 68-6Bh
Default Value: 0000h
Attribute: Read/Write
Size: 32 bits

The DRBE Register is not implemented in the 82434LX. This register contains an extension for each of the DRAM Row Boundary (DRB) Registers. Each nibble of the DRBE Register is concatenated with a DRB Register (see DRB Register section for details on the use of the DRB and DRBE Registers).



Bits	Description
31:0	**EXTENSIONS FOR DRB0 THROUGH DRB7:** Each nibble corresponds to a DRB. The nibble of the DRBE and its corresponding DRB are concatenated and used to indicate the boundaries between rows of DRAM.

3.2.22 ERRCMD—ERROR COMMAND REGISTER

Address Offset: 70h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The Error Command Register controls the PCMC responses to various system errors. Bit 6 of the PCICMD Register is the master enable for bit 3 of this register. Bit 6 of the PCICMD Register must be set to 1 to enable the error reporting function defined by bit 3 of this register. Bits 6 and 8 of the PCICMD Register are the master enables for bits 7, 6, 5, 4, and 1 of this register. Both bits 6 and 8 of the PCICMD Register must be set to 1 to enable the error reporting functions defined by bits 7, 6, 5, 4, and 1 of this register.

Bits	Description
7	**SERR# ON RECEIVED TARGET ABORT:** When this bit is set to 1 (and bit 8 of the PCICMD Register is 1), the PCMC asserts SERR# upon receiving a target abort. When this bit is set to 0, the PCMC is disabled from asserting SERR# upon receiving a target abort.
6	**SERR# ON TRANSMITTED PCI DATA PARITY ERROR:** When this bit is set to 1 (and bits 6 and 8 of the PCICMD Register are both 1), the PCMC asserts SERR# when it detects a data parity error as a result of a CPU-to-PCI write (PERR# detected asserted). When this bit is set to 0, the PCMC is disabled from asserting SERR# when data parity errors are detected via PERR#.
5	**82434LX: RESERVED** **82434NX: SERR# ON RECEIVED PCI DATA PARITY ERROR:** When this bit is set to 1 (and bits 6 and 8 of the PCICMD Register are both 1), the PCMC asserts SERR# when it detects a data parity error as a result of a CPU-to-PCI read (PAR incorrect with received data). In this case, the SERR# signal is asserted when parity errors are detected on PCI return data. When this bit is set to 0, the PCMC is disabled from asserting SERR# when data parity errors are detected during a CPU-to-PCI read.
4	**82434LX: RESERVED** **82434NX: SERR# ON PCI ADDRESS PARITY ERROR:** When this bit is set to 1 (and bits 6 and 8 of the PCICMD Register are both 1), the PCMC asserts SERR# when it detects an address parity error on PCI transactions. When this bit is set to 0, the PCMC is disabled from asserting SERR# when address parity errors are detected on PCI transactions.
3	**82434LX: RESERVED** **82434NX: PERR# ON RECEIVING A DATA PARITY ERROR:** This bit indicates whether the PERR# signal is implemented in the system. When this bit is set to 1 (and bit 6 of the PCICMD Register is 1), the PCMC asserts PERR# when it detects a data parity error (PAR incorrect with received data), either from a CPU-to-PCI read or a PCI master write to memory. When this bit is set to 0 (or bit 6 of the PCICMD Register is set to 0), the PERR# signal is not asserted by the PCMC.
2	**L2 CACHE PARITY ENABLE:** This bit indicates that the second level cache implements parity. When this bit is set to 1, bits 0 and 1 of this register control the checking of parity errors during CPU reads from the second level cache. If this bit is 0, parity is not checked when the CPU reads from the second level cache (PCHK# ignored) and neither bit 1 nor bit 0 apply.
1	**SERR# ON DRAM/L2 CACHE DATA PARITY ERROR ENABLE:** This bit enables/disables the SERR# signal for parity errors on reads from main memory or the second level cache. When this bit is set to 1 and bit 0 of this register is set to 1 (and bits 6 and 8 of the PCICMD Register are set to 1), SERR# is enabled upon a PCHK# assertion from the CPU when reading from main memory or the second level cache. The processor indicates that a parity error was received by asserting PCHK#. The PCMC then latches status information in the Error Status Register and asserts SERR#. When this bit is 0, SERR# is not asserted upon detecting a parity error. Bits[1:0] = 10 is a reserved combination. 0 = Disable assertion of SERR# upon detecting a DRAM/second level cache read parity error. 1 = Enable assertion of SERR# upon detecting a DRAM/second level cache read parity error.
0	**MCHK ON DRAM/L2 CACHE DATA PARITY ERROR ENABLE:** When this bit is set to 1, PEN# is asserted for data returned from main memory or the second level cache. The processor indicates that a parity error was received by asserting the PCHK# signal. In addition, the processor invokes a machine check exception, if enabled via the MCE bit in CR4 in the Pentium processor. The PCMC then latches status information in the Error Status register. When this bit is 0, PEN# is not asserted. Bits[1:0] = 10 is a reserved combination.

3.2.23 ERRSTS—ERROR STATUS REGISTER

Address Offset: 71h
Default Value: 00h
Attribute: Read/Write Clear
Size: 8 bits

The Error Status Register is an 8-bit register that reports the occurrence of PCI, second level cache, and DRAM parity errors. This register also reports the occurrence of a CPU shutdown cycle.

Bits	Description
7	**RESERVED**
6	**PCI TRANSMITTED DATA PARITY ERROR:** The PCMC sets this bit to a 1 when it detects a data parity error (PERR# asserted) as a result of a CPU-to-PCI write. Software resets this bit to 0 by writing a 1 to it.
5	**82434LX: RESERVED** **82434NX: PCI RECEIVED DATA PARITY ERROR:** The PCMC sets this bit to a 1 when it detects a data parity error (PAR incorrect with received data) as a result of a CPU-to-PCI read. Software resets this bit to 0 by writing a 1 to it.
4	**82434LX: RESERVED** **82434NX: PCI ADDRESS PARITY ERROR:** The PCMC sets this bit to a 1 when it detects an address parity error (PAR incorrect with received address and C/BE# lines) on a PCI master transaction. Software resets this bit to 0 by writing a 1 to it.
3	**MAIN MEMORY DATA PARITY ERROR:** The PCMC sets this bit to a 1 when it detects a parity error from the CPU PCHK# signal resulting from a CPU-to-main memory read. Software resets this bit to 0 by writing a 1 to it.
2	**L2 CACHE DATA PARITY ERROR:** The PCMC sets this bit to a 1 when it detects a parity error from the CPU PCHK# signal resulting from a CPU read access that hit in the second level cache. Software resets this bit to 0 by writing a 1 to it.
1	**RESERVED**
0	**SHUTDOWN CYCLE DETECTED:** The PCMC sets this bit to a 1 when it detects a shutdown special cycle on the Host Bus. Under this condition the PCMC drives a shutdown special cycle on PCI and asserts INIT. Software resets this bit to 0 by writing a 1 to it.

3.2.24 SMRS—SMRAM SPACE REGISTER

Address Offset: 72h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The PCMC supports a 64-KByte SMRAM space that can be selected to reside at the top of main memory, segment A0000–AFFFFh or segment B0000–BFFFFh. The SMM space defined by this register is not cacheable. This register defines a mechanism that allows the CPU to execute code out of the SMM space at either A0000h or B0000h while accessing the frame buffer on PCI. The SMRAM Enable bit in the DRAM Control Register must be 1 to enable the features defined by this register. Register bits[5:3] apply only when segment A0000-AFFFFh or B0000-BFFFFh are selected.

Bits	Description
7:6	**RESERVED**
5	**OPEN SMRAM SPACE (OSS):** When OSS = 1, the CPU can access SMM space without being in SMM mode. That is, accesses to SMM space are permitted even with SMIACT# negated. This bit is intended to be used during POST to allow the CPU to initialize SMRAM space before the first SMI# interrupt is issued.
4	**CLOSE SMRAM SPACE (CSS):** When CSS = 1 and SMRAM is enabled, CPU code accesses to the SMM memory range are directed to SMM space in main memory and data accesses are forwarded to PCI. This bit allows the CPU to read and write the frame buffer on PCI while executing SMM code. When CSS = 0 and SMRAM is enabled, all accesses to the SMRAM memory range, both code and data, are directed to SMRAM (main memory).
3	**LOCK SMRAM SPACE (LSS):** When LSS = 1, this bit prevents the SMM space from being manually opened, effectively disabling bit 5 of this register. Only a power-on reset can set this bit to 0.
2:0	**SMM BASE SEGMENT (SBS):** This field defines the 64 KByte base segment where SMM space is located. The memory that is defined by this field is non-cacheable.

Bits[2:0]	SMRAM Location	Bits[2:0]	SMRAM Location
000	Top of main memory	100	Reserved
001	Reserved	101	Reserved
010	A0000–AFFFFh	110	Reserved
011	B0000–BFFFFh	111	Reserved

3.2.25 MSG—MEMORY SPACE GAP REGISTER

Address Offset: 78-79h
Default Value: 00h
Attribute: Read/Write
Size: 16 bits

The Memory Space Gap Register defines the starting address and size of a gap in main memory. This register accommodates ISA devices that have their memory mapped into the 1 MByte–15.5 MByte range (e.g., an ISA LAN card or an ISA frame buffer). The Memory Space Gap Register defines a hole in main memory that transfers the cycles in this address space to the PCI Bus instead of main memory. This area is not cacheable.

The memory space gap starting address must be a multiple of the memory space gap size. For example, a 2 MByte gap must start at 2, 4, 6, 8, 10, 12, or 14 MBytes.

NOTE:
Memory that is disabled by the gap created by this register is remapped to the top of memory. This remapped memory is accessible, except in the case where this would cause the top of main memory to exceed 192 MBytes (or 512 MBytes for the 82434NX).

Bits	Description
15	**MEMORY SPACE GAP ENABLE (MSGE):** MSGE enables and disables the memory space gap. When MSGE is set to 1, the CPU accesses to the address range defined by this register are forwarded to PCI bus. The size of the gap created in main memory causes a corresponding amount of DRAM to be remapped at the top of main memory (top specified by DRB Registers). If the Frame Buffer Range is programmed below 16 MBytes and within main memory space, the MSG register must include the Frame Buffer Range. When MSGE is reset to 0, the memory space gap is disabled.
14:12	**MEMORY SPACE GAP SIZE (MSGS):** This 3 bit field defines the size of the memory space gap. If the Frame Buffer Range is programmed below 16 MBytes and within main memory space, this register must include the frame buffer range. The amount of main memory specified by these bits is remapped to the top of main memory. **Bit[14:12] Memory Gap Size** 000 1 MByte 001 2 MBytes 011 4 MBytes 111 8 MBytes **NOTE:** All other combinations are reserved.
11:8	**RESERVED**
7:4	**MEMORY SPACE GAP STARTING ADDRESS (MSGSA):** These 4 bits define the starting address of the memory space gap in the space from 1 MByte–16 MBytes. These bits are compared against A[23:20]. The memory space gap starting address must be a multiple of the memory space gap size. For example, a 2 MBytes gap must start at 2, 4, 6, 8, 10, 12, or 14 MBytes.
3:0	**RESERVED**

3.2.26 FBR—FRAME BUFFER RANGE REGISTER

Address Offset: 7C-7Fh
Default Value: 0000h
Attribute: Read/Write
Size: 32 bits

This 32-bit register enables and disables a frame buffer area and provides attribute settings for the frame buffer area. The attributes defined in this register are intended to increase the performance of the frame buffer. The FBR Register can be used to accommodate PCI devices that have their memory mapped onto PCI from the top of main memory to 4 GByte–512-KByte range (e.g., a linear frame buffer). If the Frame Buffer Range is located within the 1 MByte–16 MBytes main memory region where DRAM is populated, the Memory Space Gap Register must be programmed to include the Frame Buffer Range.

Bits	Description
31:20	**BUFFER OFFSET (BO):** BO defines the starting address of the frame buffer address space in increments of 1 MByte. This 12-bit field is compared directly against A[31:20]. The frame buffer range can either be located at the top of memory, including remapped memory or within the memory space gap (i.e., frame buffer range programmed below 16 MBytes and within main memory space. When bits [31:20] = 0000h and bit 12 = 0, all features defined by this register are disabled.
19:14	**RESERVED**
13	**BYTE MERGING (BM):** Byte merging permits CPU-to-PCI byte writes to the LBX posted write buffer to be combined into a single transfer on the PCI Bus, when appropriate. When BM is set to 1, byte merging on CPU-to-PCI posted write cycles is enabled. When BM is reset to 0, byte merging is disabled.
12	**128K VGA RANGE ATTRIBUTE ENABLE (VRAE):** When VRAE = 1, the attributes defined in this register (bits [13, 10:7]) also apply to the VGA memory range of A0000h–BFFFFh regardless of the value programmed in the Buffer Offset field. When VRAE = 0, the attributes do not apply to the VGA memory range. Note that this bit only affects the mentioned attributes of the VGA memory range and does not enable or disable accesses to the VGA memory range.
11:10	**RESERVED**
9	**NO LOCK REQUESTS (NLR):** When NLR is set to 1, the PCMC never requests exclusive access to a PCI resource via the PCI LOCK# signal in the range defined by this register. When NLR is reset to 0, exclusive access via the PCI LOCK# signal in the range defined by this register is enabled.
8	**RESERVED**
7	**TRANSPARENT BUFFER WRITES (TBW):** When set to a 1, this bit indicates that writes to the Frame Buffer Range need not be flushed for deadlock or coherence reasons on synchronization events (i.e., PCI master reads, and the FLSHBUF#/MEMREQ# protocol). When reset to 0, this bit indicates that upon synchronization events, flushing is required for Frame Buffer writes posted in the CPU-to-PCI Write Buffer in the LBX
6:4	**RESERVED**
3:0	**BUFFER RANGE (BR):** These bits define the size of the frame buffer address space, allowing up to 16 MBytes of frame buffer. If the Frame Buffer Range is within the memory space gap, the buffer range is limited to 8 MBytes and must be included within the memory space gap. The bits listed below in the Reserved Buffer Offset (BO) Bits column are ignored by the PCMC for the corresponding buffer sizes. **Bits[3:0] — Buffer Size — Reserved Buffer Offset (BO) Bits** 0000 — 1 MByte — None 0001 — 2 MBytes — [20] 0011 — 4 MBytes — [21:20] 0111 — 8 MBytes — [22:20] 1111 — 16 MBytes — [23:20] **NOTE:** (all other combinations are reserved)

4.0 PCMC ADDRESS MAP

The Pentium processor has two distinct physical address spaces: Memory and I/O. The memory address space is 4 GBytes and the I/O address space is 64 KBytes. The PCMC maps accesses to these address spaces as described in this section.

4.1 CPU Memory Address Map

Figure 9 shows the address map for the 4 GByte Host CPU memory address space. Depending on the address range and whether a memory gap is enabled via the MSG Register, the PCMC forwards CPU memory accesses to either main memory or PCI memory. Accesses forwarded to main memory invoke operations on the DRAM interface and accesses forwarded to PCI memory invoke operations on PCI. Mapping to the PCI Bus permits PCI or EISA/ISA Bus-based memory.

The main memory size ranges from 2 MBytes–192 MBytes for the 82434LX and 2 MBytes–512 MBytes for the 82434NX. Memory accesses above 192 MBytes (512 MBytes for the 82434NX) are always forwarded to PCI. In addition, a memory gap can be created in the 1 MByte–16 MBytes region that provides a window to PCI-based memory. The location and size of the gap is programmable. Accesses to addresses in the gap are ignored by the DRAM controller and forwarded to PCI. Note that CPU memory accesses that are forwarded to PCI (including the Memory Space Gap) are not cacheable. Only main memory controlled by the PCMC DRAM interface is cacheable.

4.2 System Management RAM—SMRAM

The PCMC supports the use of main memory as System Management RAM (SMRAM) enabling the use of System Management Mode. This function is enabled and disabled via the DRAM Control Register. When this function is disabled, the PCMC memory map is defined by the DRB and PAM Registers. When SMRAM is enabled, the PCMC reserves the top 64-KBytes of main memory for use as SMRAM.

SMRAM can also be placed at A0000–AFFFFh or B0000–BFFFFh via the SMRAM Space Register. Enhanced SMRAM features can also be enabled via this register. PCI masters can not access SMRAM when it is programmed to the A or B segments.

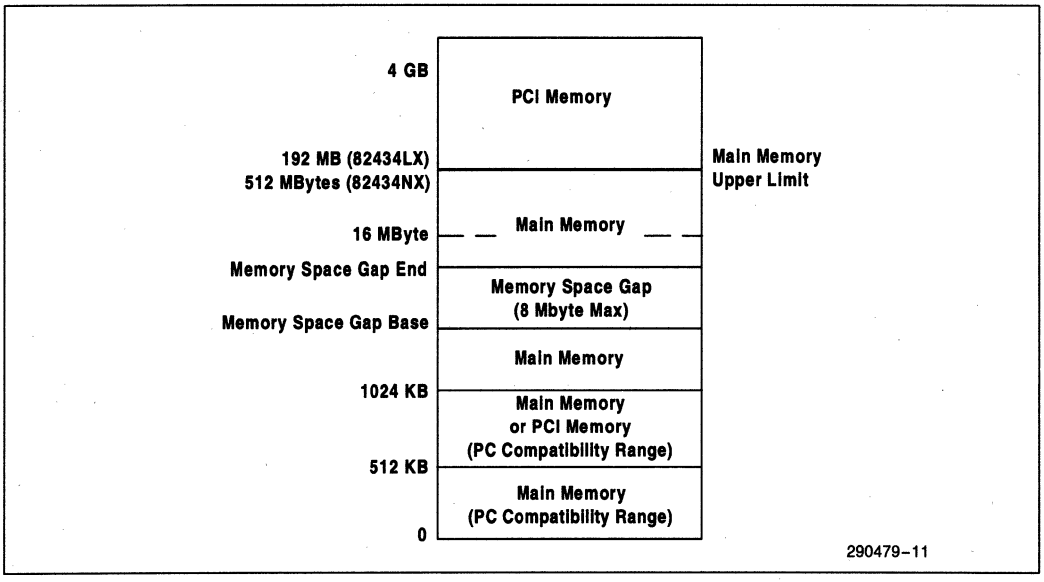


Figure 9. CPU Memory Address Map—Full Range

However, PCI masters can access SMRAM when the top of memory is selected.

When the 82434NX PCMC detects a CPU stop grant special cycle (M/IO# = 0, D/C# = 0, W/R# = 1, A4 = 1, BE[7:0]# = FBh), it generates a PCI Stop Grant Special cycle, with 0002h in the message field (AD[15:0]) and 0012h in the message dependent data field (AD[31:16]) during the first data phase (IRDY# asserted).

4.3 PC Compatibility Range

The PC Compatibility Range is the first MByte of the Memory Map. The 512 KByte–1 MByte range is subdivided into several regions as shown in Figure 10. Each region is provided with programmable attributes in the PAM Registers. The attributes are Read Enable (RE), Write Enable (WE) and Cache Enable (CE). The attributes determine readability, writeability and cacheability of the corresponding memory region. When the associated bit in the PAM Register is set to a 1, the attribute is enabled and when set to a 0 the attribute is disabled. The following rules apply for cacheability in the first level and second level caches:

1. If RE = 1, WE = 1, and CE = 1, the region is cacheable in the first level and second level caches.
2. If RE = 1, WE = 0, and CE = 1, the region is cacheable only on code reads (i.e., D/C# = 0). Data reads do not result in a line fill. Writes to the region are not serviced by the secondary cache, but are forwarded to PCI.

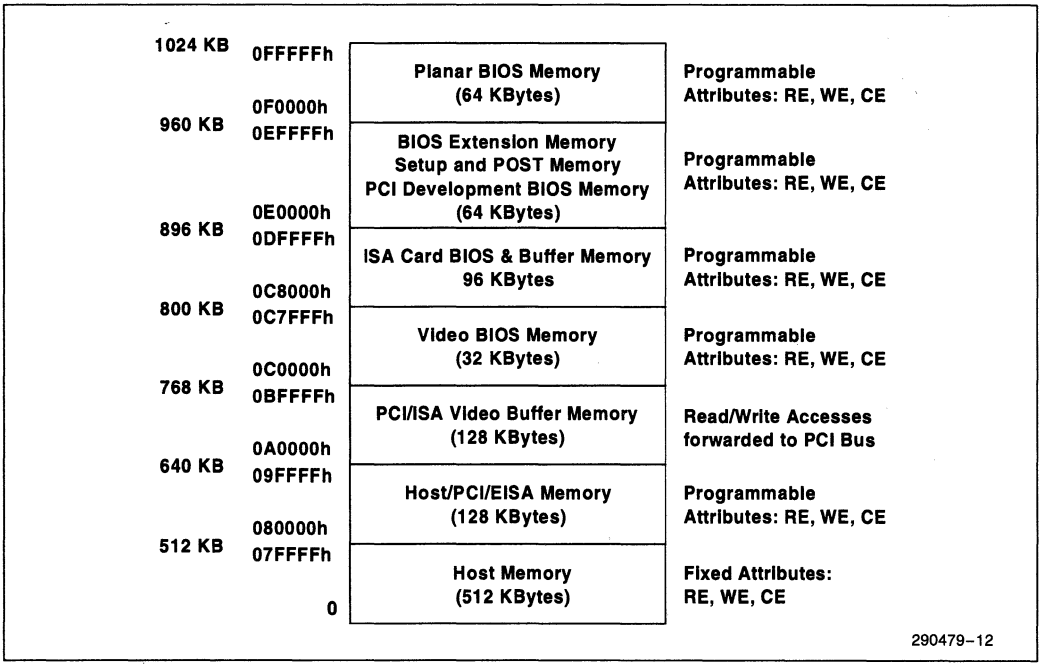
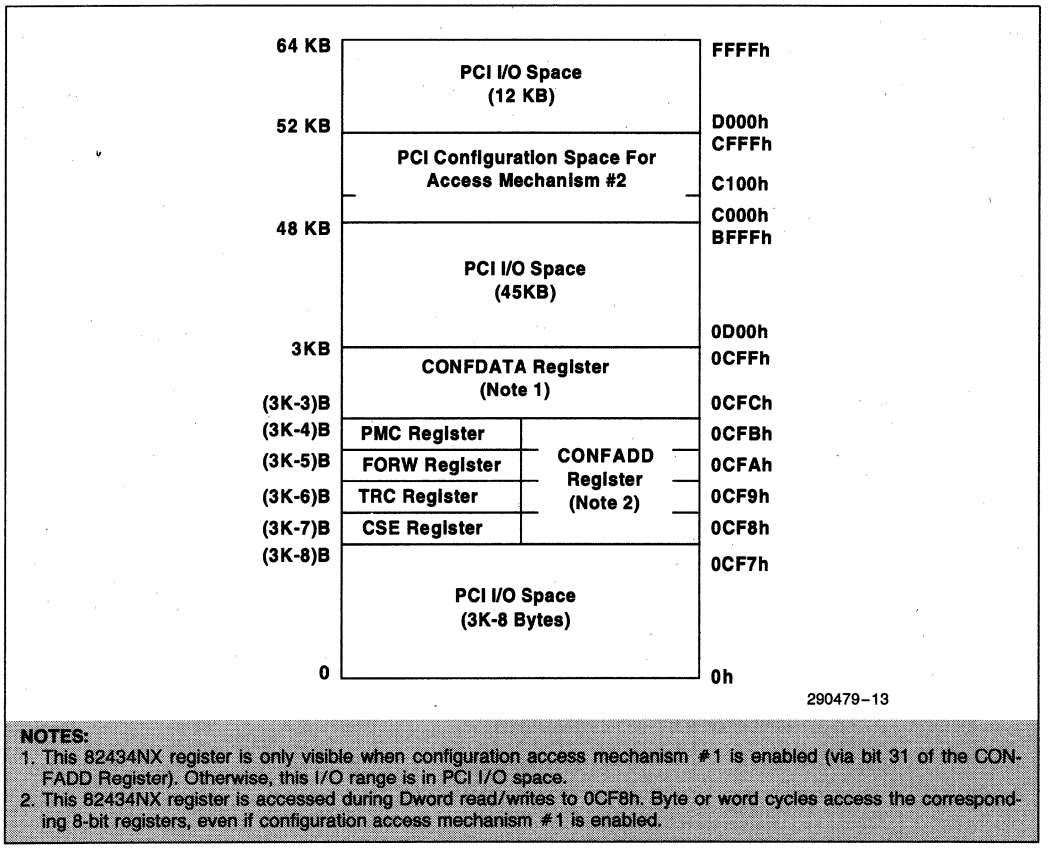


Figure 10. CPU Memory Address Map—PC Compatibility Range

The RE and WE bits for each region are used to shadow BIOS ROM in main memory for improved system performance. To shadow a BIOS area, RE is reset to 0 and WE is set to 1. RE is set to 1 and WE is reset to 0. Any writes to the BIOS area are forwarded to PCI.

4.4 I/O Address Map

I/O devices (other than the PCMC) are not supported on the Host Bus. The PCMC generates PCI Bus cycles for all CPU I/O accesses, except to the PCMC internal registers. Figure 11 shows the mapping for the CPU I/O address space. For the 82434LX, three PCMC registers are located in the CPU I/O address space—the Configuration Space Enable (CSE) Register, the Turbo-Reset Control (TRC) Register, and the Forward (FORW) Register.



NOTES:
1. This 82434NX register is only visible when configuration access mechanism #1 is enabled (via bit 31 of the CONFADD Register). Otherwise, this I/O range is in PCI I/O space.
2. This 82434NX register is accessed during Dword read/writes to 0CF8h. Byte or word cycles access the corresponding 8-bit registers, even if configuration access mechanism #1 is enabled.

Figure 11. CPU I/O Address Map

For the 82434NX, six PCMC registers are located in the CPU I/O address space—the Configuration Space Enable (CSE) Register, the Configuration Address Register (CONFADD), the Turbo-Reset Control (TRC) Register, the Forward (FORW) Register, the PCI Mechanism Control (PMC) Register, and the Configuration Data (CONFDATA) Register.

Except for the I/O locations of the above mentioned registers, all other CPU I/O accesses are mapped to either PCI I/O space or PCI configuration space. If the access is to PCI I/O space, the PCI address is the same as the CPU address. If the access is to PCI configuration space, the CPU address is mapped to a configuration space address as described in Section 3.0, Register Description.

If configuration space is enabled via the CSE Register (access mechanism #2), the PCMC maps accesses in the address range of C100h to CFFFh to PCI configuration space. Accesses to the PCMC configuration register range (C000h to C0FFh) are intercepted by the PCMC and not forwarded to PCI. If the configuration space is disabled in the CSE Register, CPU accesses to the configuration address range (C000h to CFFFh) are forwarded to PCI I/O space.

5.0 SECOND LEVEL CACHE INTERFACE

This section describes the second level cache interface for the 82434LX Cache (Section 5.1) and the 82434NX Cache (Section 5.2). The differences are in the following areas:

1. The 82434LX supports both write-through and write-back cache policies. The 82434NX only supports the write-back policy.
2. The 82434LX timings are for 60 and 66 MHz and the 82434NX timings are for 50, 60, and 66 MHz. Note that the cycle latencies for 60 and 66 MHz are the same for both devices.
3. When burst SRAMs are used to implement the secondary cache, address latches are not needed for the 82434NX type SRAM connectivity. However, a control bit has been added to the 82434NX that permits address latches for 82434LX type SRAM connectivity.
4. A low-power second level cache standby mode has been added to the 82434NX.
5. There are new or changed cache control bits as indicated by the shading in Section 3.0, Register Description. For example, the 82434NX supports zero wait-state cache at 50 MHz via the zero wait-state control bit.

NOTE:

- Second level cache sizes and organization are the same for the 82434LX and 82434NX.
- The general operation of the second level cache write-back policy is the same for the 82434LX and 82434NX. For example, the Valid and Modified bits operate the same for both devices. In addition, snoop operations are the same for both devices, as well as the handling of flush, flush acknowledge, and write-back special cycles.

1

5.1 82434LX Cache

The 82434LX PCMC integrates a high performance write-back/write-through second level cache controller providing integrated tags and a full first level and second level cache coherency mechanism. The second level cache controller can be configured to support either a 256-KByte cache or a 512 KByte cache using either synchronous burst SRAMs or standard asynchronous SRAMs. The cache is direct mapped and can be configured to support either a write-back or write-through write policy. Parity on the second level cache data SRAMs is optional.

The 82434LX contains 4096 address tags. Each tag represents a *sector* in the second level cache. If the second level cache is 256-KByte, each tag represents two cache lines. If the second level cache is 512-KByte, each tag represents four cache lines. Thus, in the 256-KByte configuration each sector contains two lines. In the 512-KByte configuration, each sector contains four lines. *Valid* and *modified* status bits are kept on a per line basis. Thus, in the case of a 256-KByte cache each tag has two valid bits and two modified bits associated with it. In the case of a 512-KByte cache each tag has four valid and four modified bits associated with it. Upon a CPU read cache miss, the PCMC inspects the valid and modified bits within the addressed sector and writes back to main memory only the lines marked both valid and modified. All of the lines in the sector are then invalidated. The line fill will then occur and the valid bit associated with the allocated line will be set. Only the requested line will be fetched from main memory and written into the cache. If no write-back is required, all of the lines in the sector are marked invalid. The line fill then occurs and the valid bit associated with the allocated line will be set. Lines are not allocated on write misses. When a CPU write hits a line in the second level cache, the modified bit for the line is set.

The second level cache is optional to allow the 82434LX PCMC to be used in a low cost configuration. A 256-KByte cache is implemented with a single bank of eight 32K x 9 SRAMs if parity is supported or 32K x 8 SRAMs if parity is not supported on the cache. A 512-KByte cache is implemented with four 64K x 18 SRAMs if parity is supported or 64K x 16 SRAMs if parity is not supported on the cache. Two 74AS373 latches complete the cache. Only main memory controlled by the PCMC DRAM interface is cached. Memory on PCI is not cached.

Figure 12 and Figure 13 depict the organization of the internal tags in the PCMC configured for a 256 KByte cache and a 512-KByte cache.

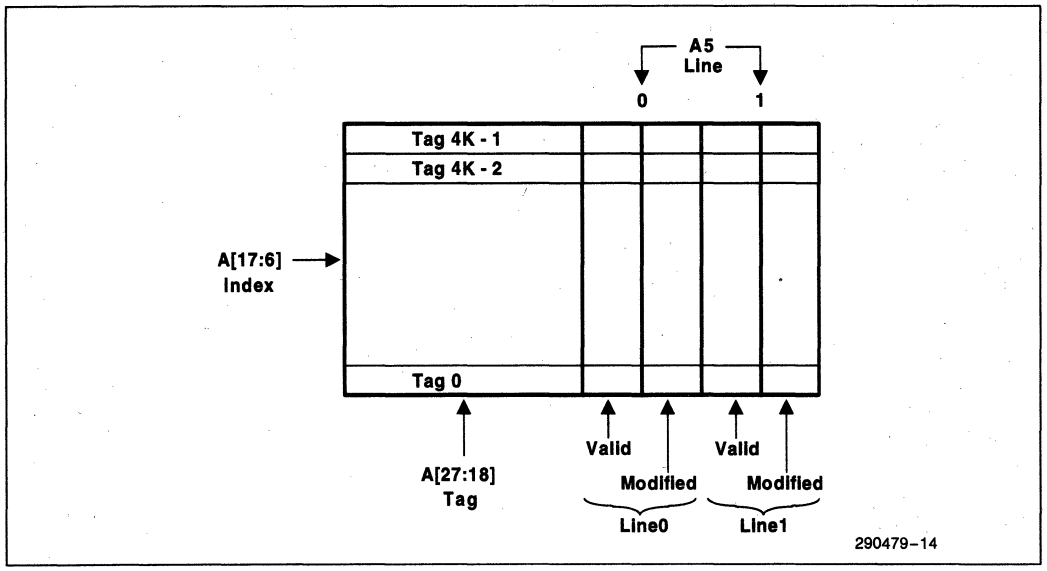


Figure 12. PCMC Internal Tags with 256-KByte Cache

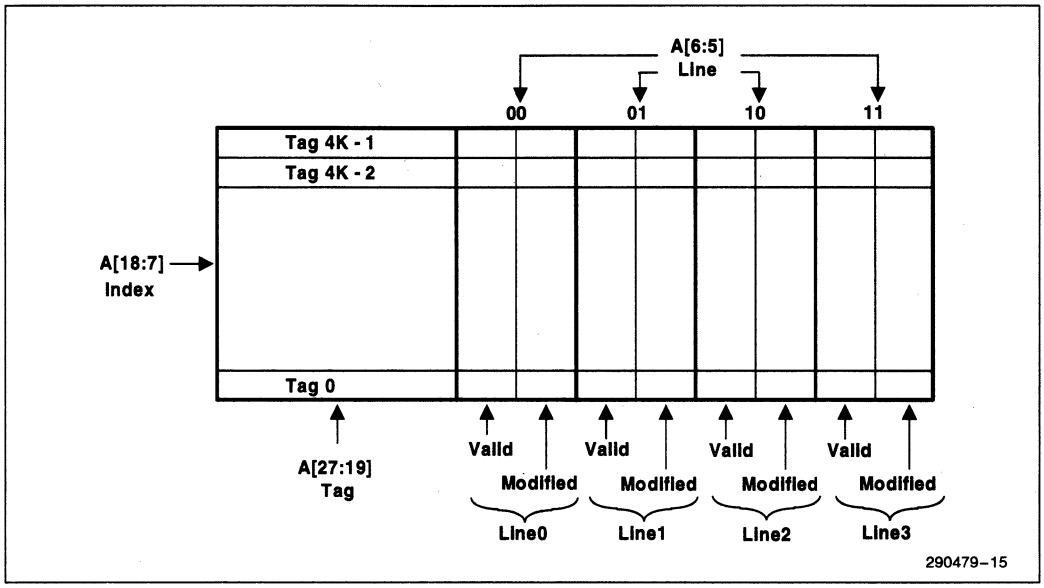


Figure 13. PCMC Internal Tags with 512-KByte Cache

In the 256-KByte cache configuration A[17:6] form the tag RAM index. The ten tag bits read from the tag RAM are compared against A[27:18] from the host address bus. Two valid bits and two modified bits are kept per tag in this configuration. Host address bit 5 is used to select between lines 0 and 1 within a sector. In the 512-KByte cache configuration A[18:7] form the tag RAM index. The nine bits read from the tag RAM are compared against A[27:19] from the host bus. Four valid bits and four modified bits are kept per tag. Host address bits 5 and 6 are used to select between lines 0, 1, 2 and 3 within a sector.

The Secondary Cache Controller Register at offset 52h in configuration space controls the secondary cache size, write and allocation policies, and SRAM type. The cache can also be enabled and disabled via this register.

Figure 14 through Figure 18 show the connections between the PCMC and the external cache data SRAMs and latches.

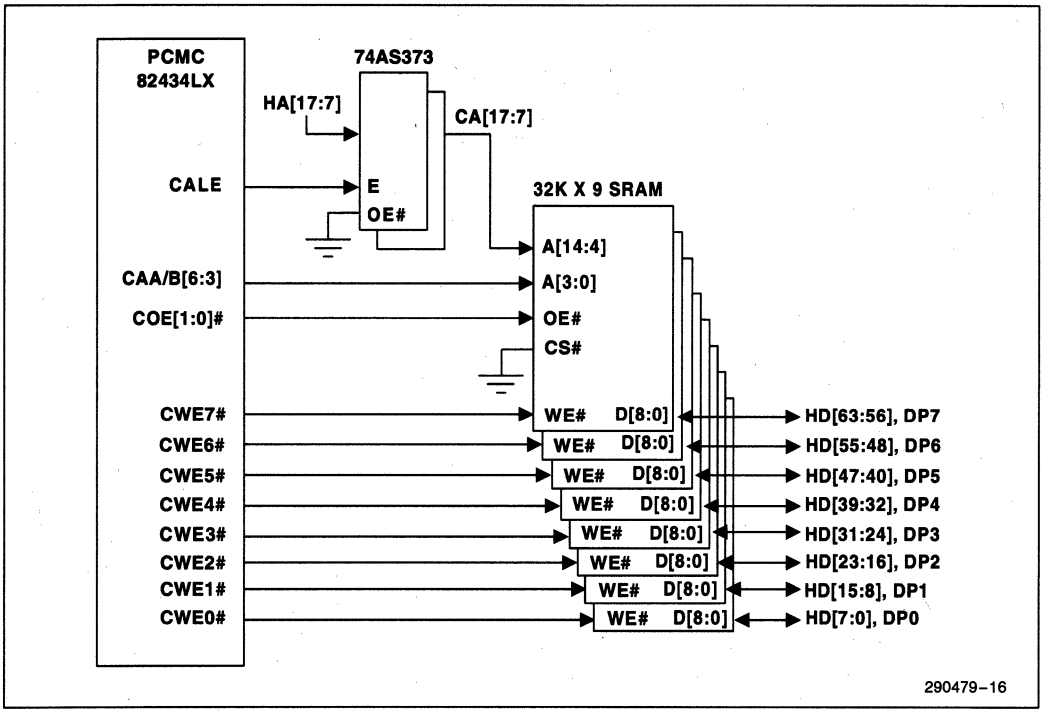


Figure 14. 82434LX Connections to 256-KByte Cache with Standard SRAM

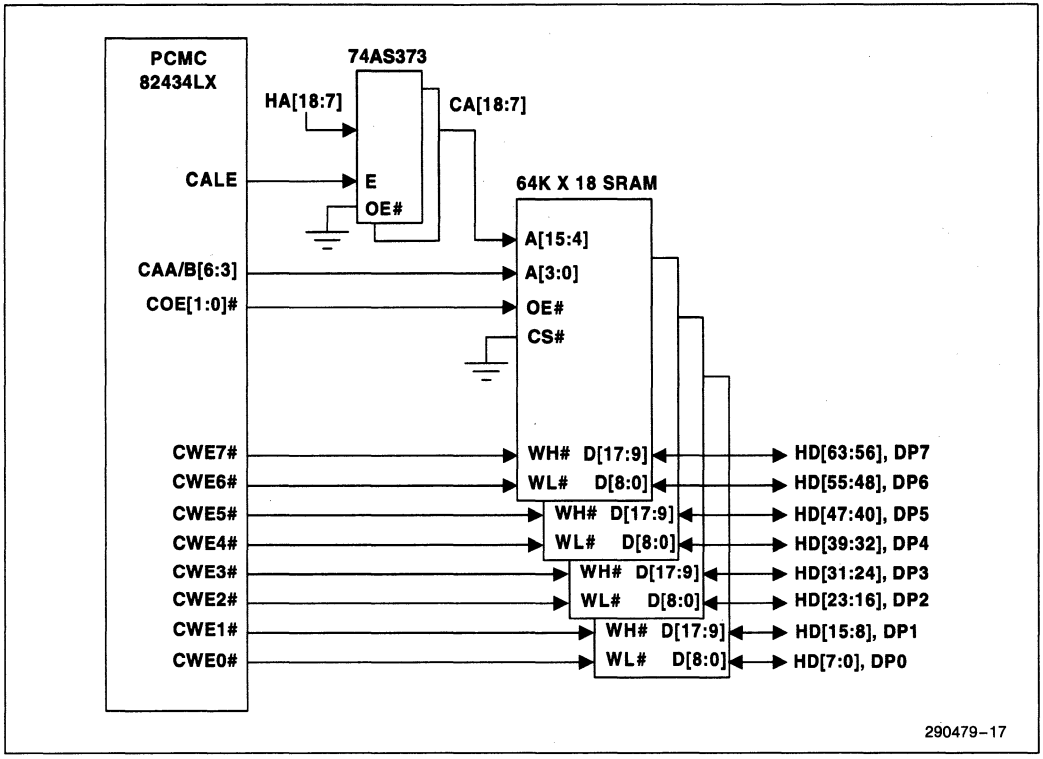


Figure 15. 82434LX Connections to 512-KByte Cache with Standard SRAM

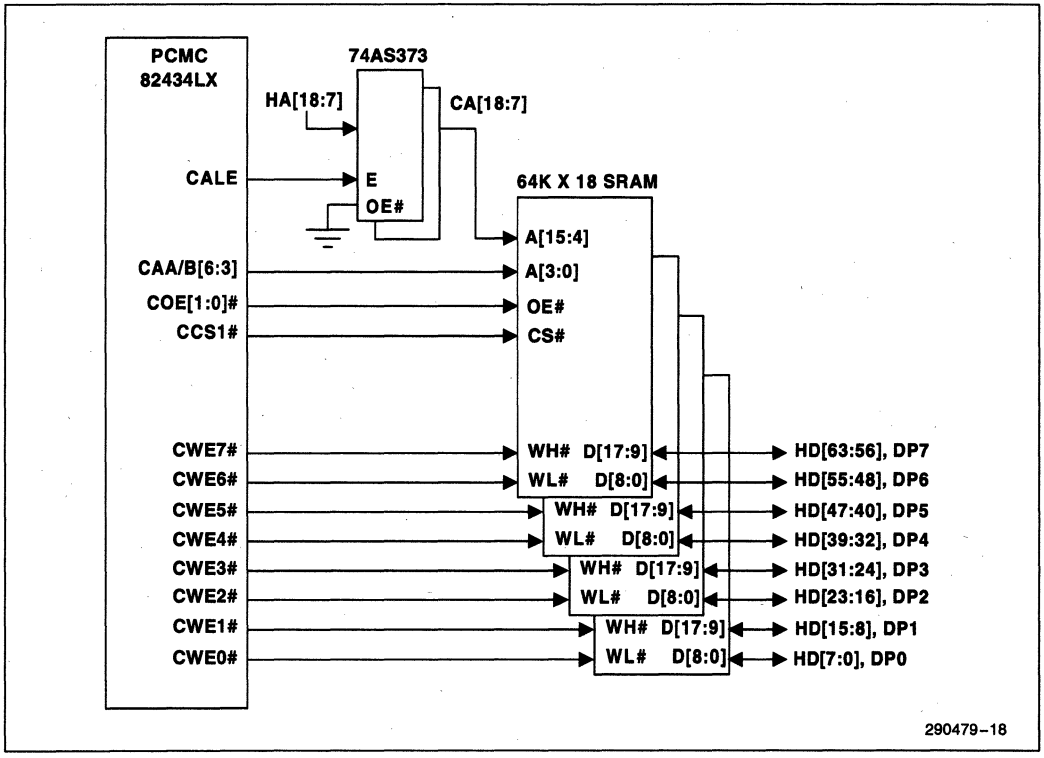


Figure 16. 82434LX Connections to 512-KByte Cache with Dual-Byte Select Standard SRAMs

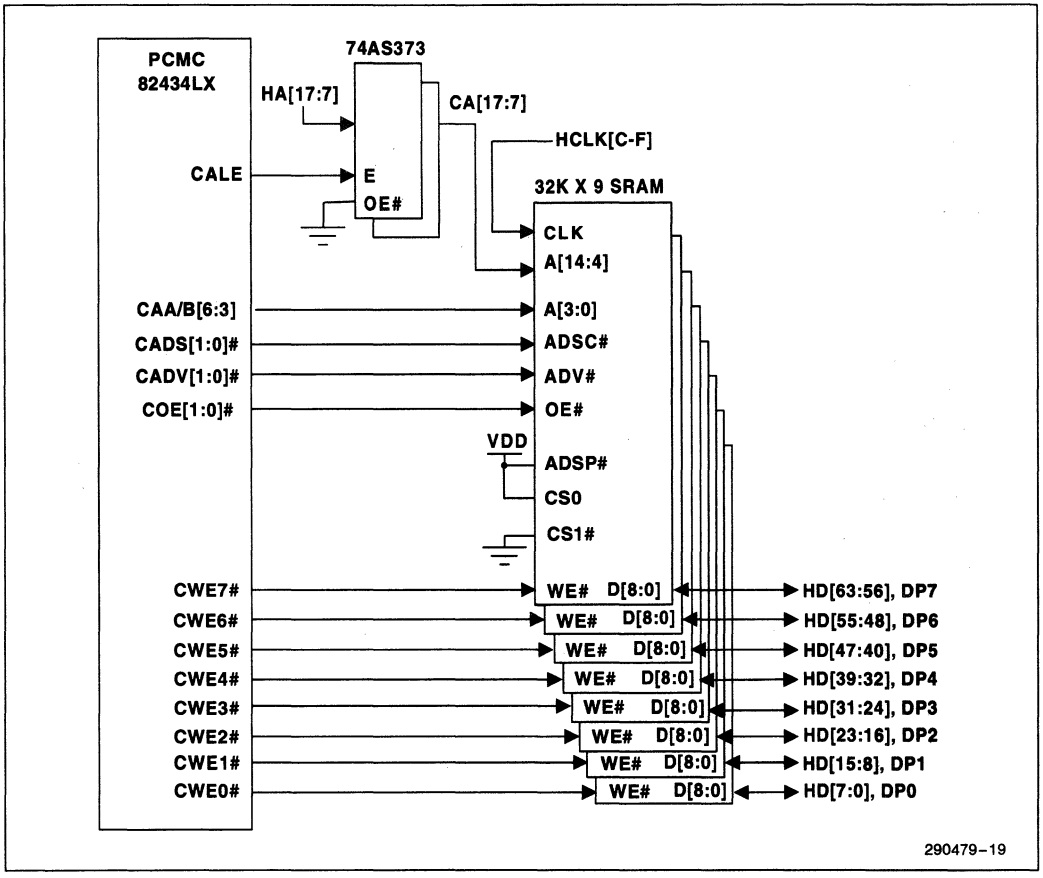


Figure 17. 82434LX Connections to 256-KByte Cache with Burst SRAM

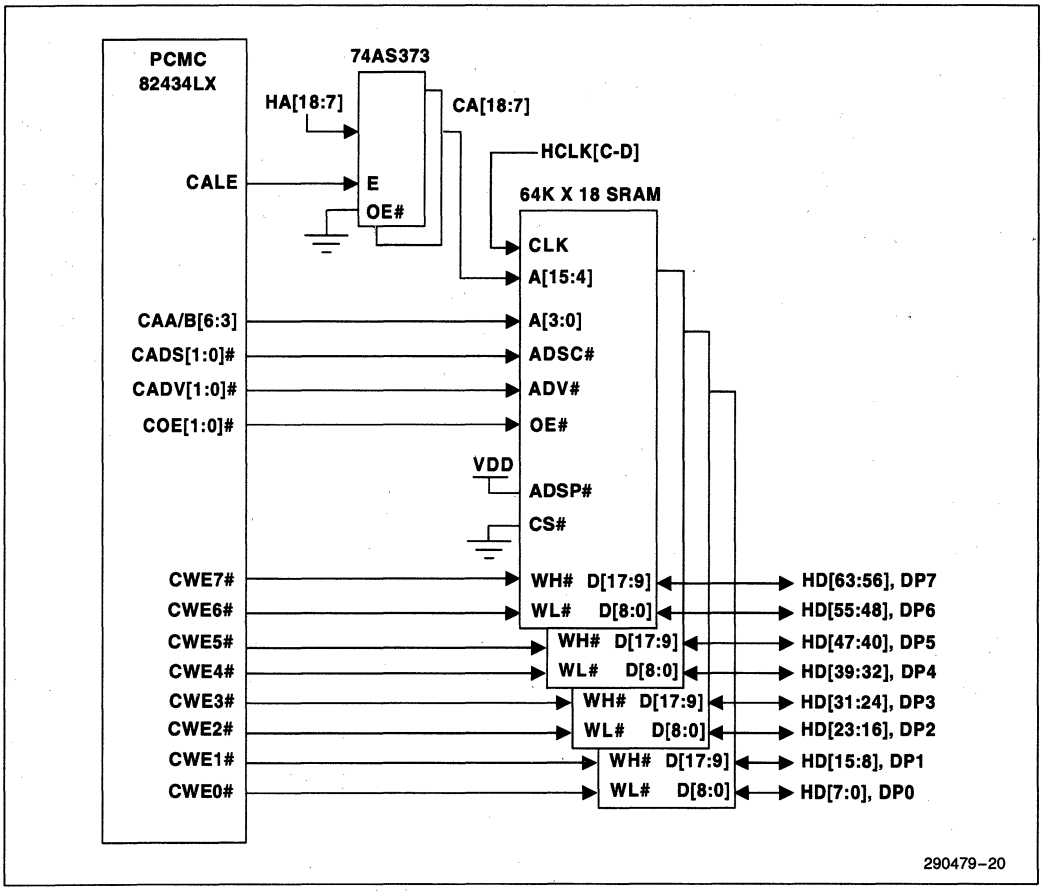


Figure 18. 82434LX Connections for 512-KByte Cache with Burst SRAM

When CALE is asserted, HA[18:7] flow through the address latch. When CALE is negated the address is captured in the latch allowing the processor to pipeline the next bus cycle onto the address bus. Two copies of CA[6:3], COE#, CADS# and CADV# are provided to reduce capacitive loading. Both copies should be used when the second level cache is implemented with eight 32K x 8 or 32K x 9 SRAMs. Either both copies or only one copy can be used with 64K x 18 or 64K x 16 SRAMs as determined by the system board layout and timing analysis. The two copies are always driven to the same logic level. CAA[4:3] and CAB[4:3] are used to count through the Pentium processor burst order when standard SRAMs are used to implement the cache.

With burst SRAMs, the address counting is provided inside the SRAMs. In this case, CAA[4:3] and CAB[4:3] are only used at the beginning of a cycle to load the initial low order address bits into the burst SRAMs. During CPU accesses, host address lines 6 and 5 are propagated to the CAA[6:5] and CAB[6:5] lines and are internally latched. When a CPU read cycle forces a line replacement in the second level cache, all modified lines within the addressed sector are written back to main memory. The PCMC uses CAA[6:5] and CAB[6:5] to select among the lines within the sector. The Cache Output Enables (COE[1:0]#) are asserted to enable the SRAMs to drive data onto the host data bus. The Cache Write Enables (CWE[7:0]#) allow byte control during CPU writes to the second level cache.

An asynchronous SRAM 512-KByte cache can be implemented with two different types of SRAM byte control. Figure 15 depicts the PCMC connections to a 512 KByte cache using 64K x 18 SRAMs or 64K x 16 SRAMs with two write enables per SRAM. Each SRAM has a high and low write enable. Figure 16 depicts the PCMC connections to a 512-KByte cache using 64K x 18 SRAMs or 64K x 16 SRAMs with two byte select lines per SRAM. Each SRAM has a high and low byte select.

The type of cache byte control (write enable or byte select) is programmed in the Cache Byte Control bit in the Secondary Cache Control Register at configuration space offset 52h. When this bit is set to 0, byte select control is used. In this mode, the CBS[7:0]# lines are multiplexed onto pins 90, 91, and 95-100 and CR/W[1:0]# pins are multiplexed onto pins 93 and 94. When this bit is set to 1, byte write enable control is used. In this mode, the CWE[7:0]# lines are multiplexed onto pins 90, 91, and 95-100. CADS[1:0]# and CADV[1:0]# are only used with burst SRAMs. The Cache Address Strobes (CADS[1:0]#) are asserted to cause the burst SRAMs to latch the cache address at the beginning of a second level cache access. CADS[1:0]# can be connected to either ADSP# or ADSC# on the SRAMs. The Cache Advance signals (CADV[1:0]#) are asserted to cause the burst SRAMs to advance to the next address of the burst sequence.

5.1.1 CLOCK LATENCIES (82434LX)

Table 5 and Table 6 list the latencies for various CPU transfers to or from the second level cache for standard SRAMs and burst SRAMs. Standard SRAM access times of 12 ns and 15 ns are recommended for 66 MHz and 60 MHz operation, respectively. Burst SRAM clock access times of 8 ns and 9 ns are recommended for 66 MHz and 60 MHz operation, respectively. Precise SRAM timing requirements should be determined by system board electrical simulation with SRAM I/O buffer models.

Table 5. Second Level Cache Latencies with Standard SRAM (82434LX)

Cycle Type	HCLK Count
Burst Read	3-2-2-2
Burst Write	4-2-2-2
Single Read	3
Single Write	4
Pipelined Back to Back Burst Reads	3-2-2-2/3-2-2-2
Burst Read followed by Pipelined Write	3-2-2-2/4

Table 6. Second Level Cache Latencies with Burst SRAM (82434LX)

Cycle Type	HCLK Count
Burst Read	3-1-1-1
Burst Write	3-1-1-1
Single Read	3
Single Write	3
Pipelined Back to Back Burst Reads	3-1-1-1/1-1-1-1
Read Followed by Pipelined Write	3-1-1-1/2

5.1.2 STANDARD SRAM CACHE CYCLES (82434LX)

The following sections describe the activity of the second level cache interface when standard asynchronous SRAMs are used to implement the cache.

5.1.2.1 Burst Read (82434LX)

Figure 19 depicts a burst read from the second level cache with standard SRAMs. The CPU initiates the read cycle by driving address and status onto the bus and asserting ADS#. Initially, the CA[6:3] are a propagation delay from the host address lines A[6:3]. Upon sampling W/R# active and M/IO# inactive, while ADS# is asserted, the PCMC asserts COE# to begin a read cycle from the SRAMs. CALE is negated, latching the address lines on the SRAM address inputs, allowing the CPU to pipeline a new address onto the bus. CA[4:3] cycle through the Pentium processor burst order, completing the cycle. PEN# is asserted with the first BRDY# and negated with the last BRDY# if parity is implemented on the second level cache data SRAMs and the MCHK DRAM/Second Level Cache Data Parity bit in the Error Command Register (offset 70h) is set.

Figure 20 depicts a burst read from the second level cache with standard 16- or 18-bit wide dual-byte select SRAMs. A single read cycle from the second level cache is very similar to the first transfer of a burst read cycle. CALE is not negated throughout the cycle. COE# is asserted as shown above, but is negated with BRDY#.

When the Secondary Cache Allocation (SCA) bit in the Secondary Cache Control Register is set to 1, the PCMC performs a line fill in the secondary cache, even if the CACHE# signal from the CPU is inactive. In this case, AHOLD is asserted to prevent the CPU from beginning a new cycle while the second level cache line fill is completing.

Back-to-back pipelined burst reads from the second level cache are shown in the Figure 21.

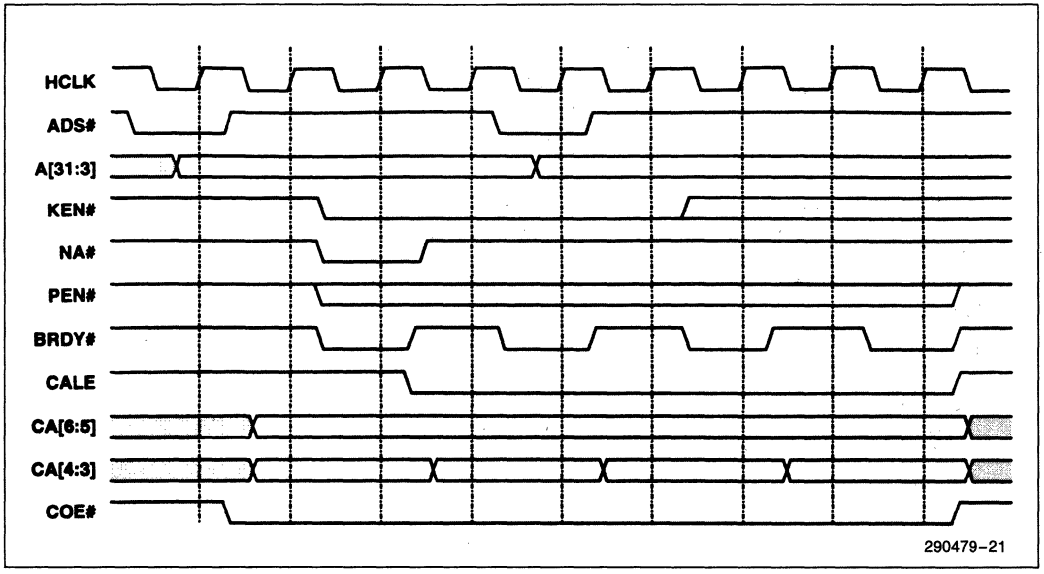


Figure 19. CPU Burst Read from Second Level Cache with Standard SRAM (82434LX)

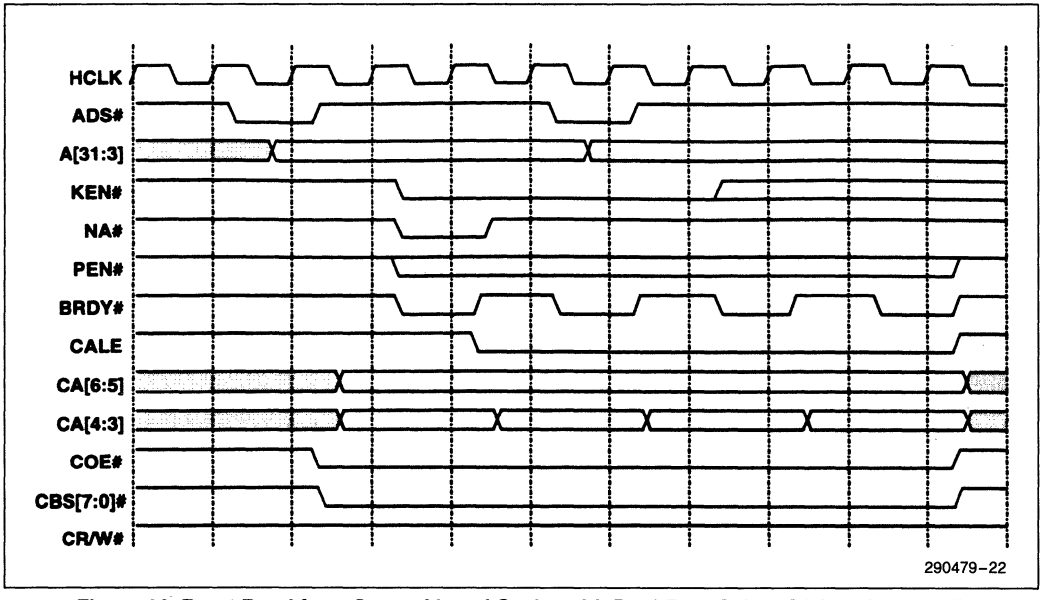


Figure 20. Burst Read from Second Level Cache with Dual-Byte Select SRAMs (82434LX)

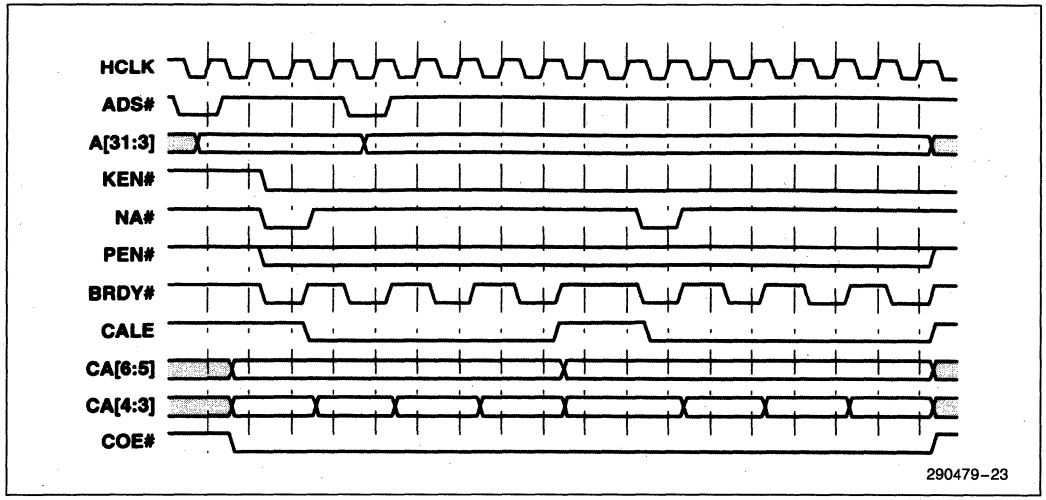


Figure 21. Pipelined Back-to-Back Burst Reads from Second Level Cache with Standard SRAM (82434LX)

Due to assertion of NA#, the CPU drives a new address onto the bus before the first cycle is complete. In this case, the second cycle is a hit in the second level cache. Immediately upon completion of the first read cycle, the PCMC begins the second cycle. When the first cycle completes, the PCMC drives the new address to the SRAMs on CA[6:3] and asserts CALE. The second cycle is very similar to the first, completing at a rate of 3-2-2-2. The cache address lines must be held at the SRAM address inputs until the first cycle completes. Only after the last BRDY# is returned, can CALE be asserted and CA[6:3] be changed. Thus, the pipelined cycle completes at the same rate as a non-pipelined cycle.

5.1.2.2 Burst Write (82434LX)

A burst write cycle is used to write back a cache line from the first level cache to either the second level cache or DRAM. Figure 22 depicts a burst write cycle to the second level cache with standard SRAMs. The CPU initiates the write cycle by driving address and status onto the bus and asserting ADS#. Initially, the CA[6:3] propagate from the host address lines A[6:3]. CALE is negated, latching the address lines on the SRAM address inputs, allowing the CPU to pipeline a new address onto the bus. Burst write cycles from the Pentium processor always begin with the low order Qword and advances to the high order Qword. CWE[7:0]# are generated from an internally delayed version of HCLK, providing address setup time to CWE[7:0]# falling and data setup time to CWE[7:0]# rising edges. HIG[4:0] are driven to PCMWQ (Post CPU to Memory Write Buffer Qword) only when the PCMC is programmed for a write-through write policy. When programmed for write-back mode, the modified bit associated with the line is set within the PCMC. The single write cycle is very similar to the first write of a burst write cycle. A burst read cycle followed by a pipelined write cycle with standard SRAMs is depicted in Figure 24.

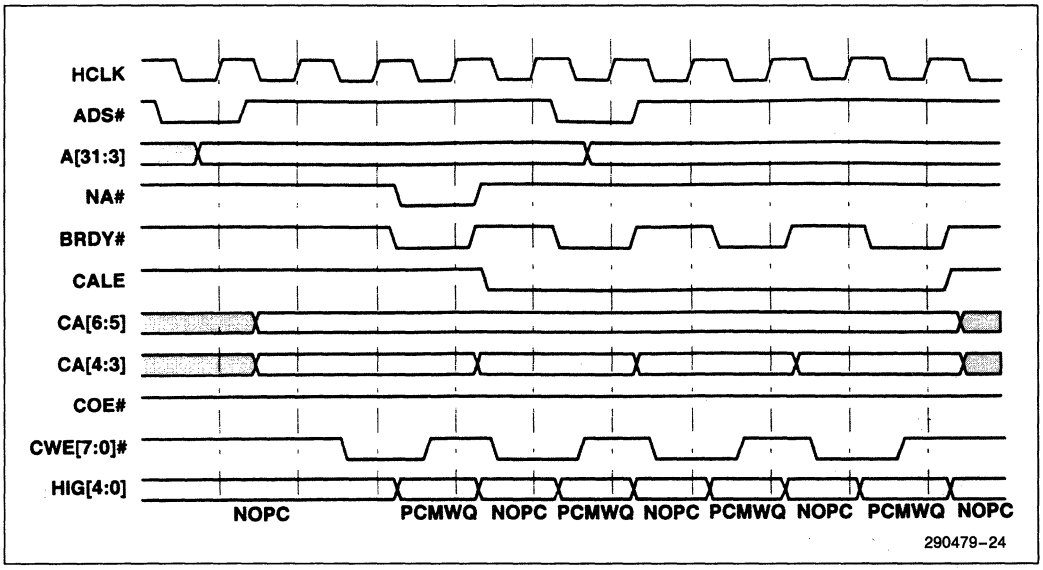


Figure 22. Burst Write to Second Level Cache with Standard SRAM (82434LX)

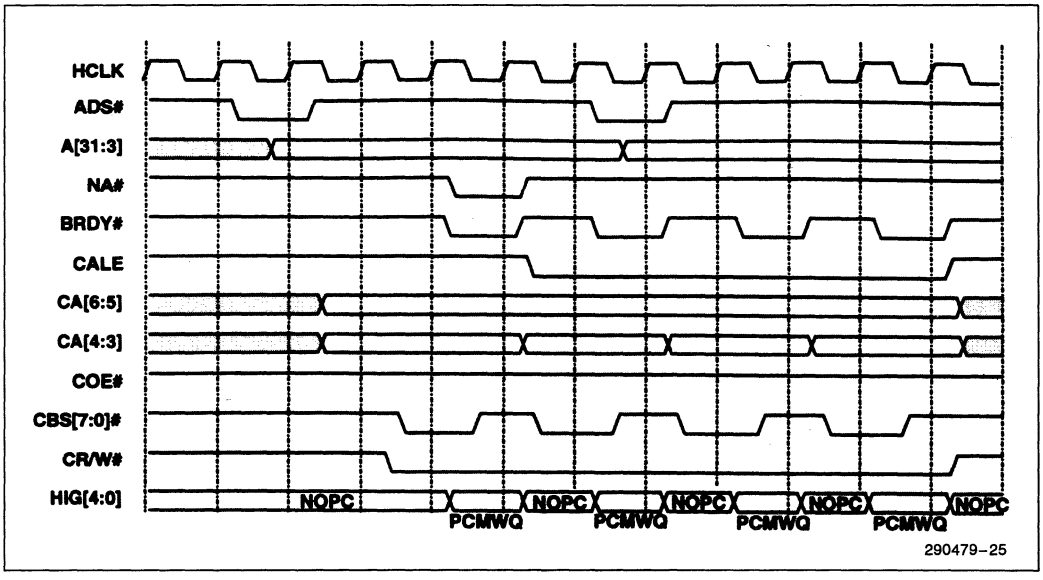


Figure 23. Burst Write to Second Level Cache with Dual-Byte Select Standard SRAMs (82434LX)

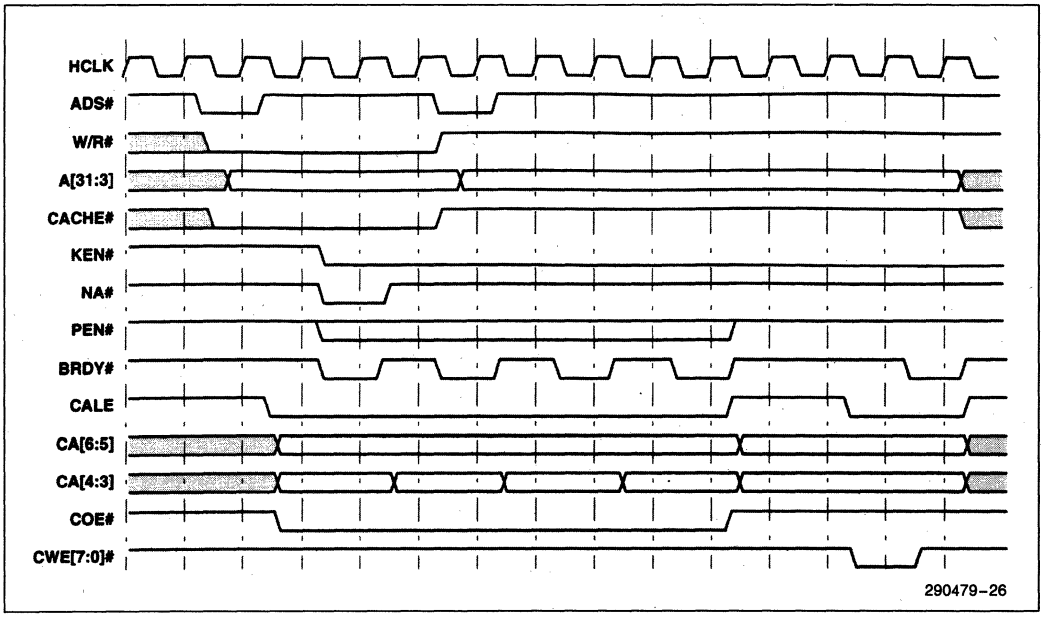


Figure 24. Burst Read Followed by Pipelined Write with Standard SRAM (82434LX)

5.1.2.3 Cache Line Fill (82434LX)

If the CPU issues a memory read cycle to cacheable memory that is not in the second level cache, a first and second level cache line fill occurs. Figure 25 depicts a CPU read cycle that results in a line fill into the first and second level caches.

Figure 27 depicts the host bus activity during a CPU read cycle that forces a write-back from the second level cache to the CPU-to-memory posted write buffer as the DRAM read cycle begins.

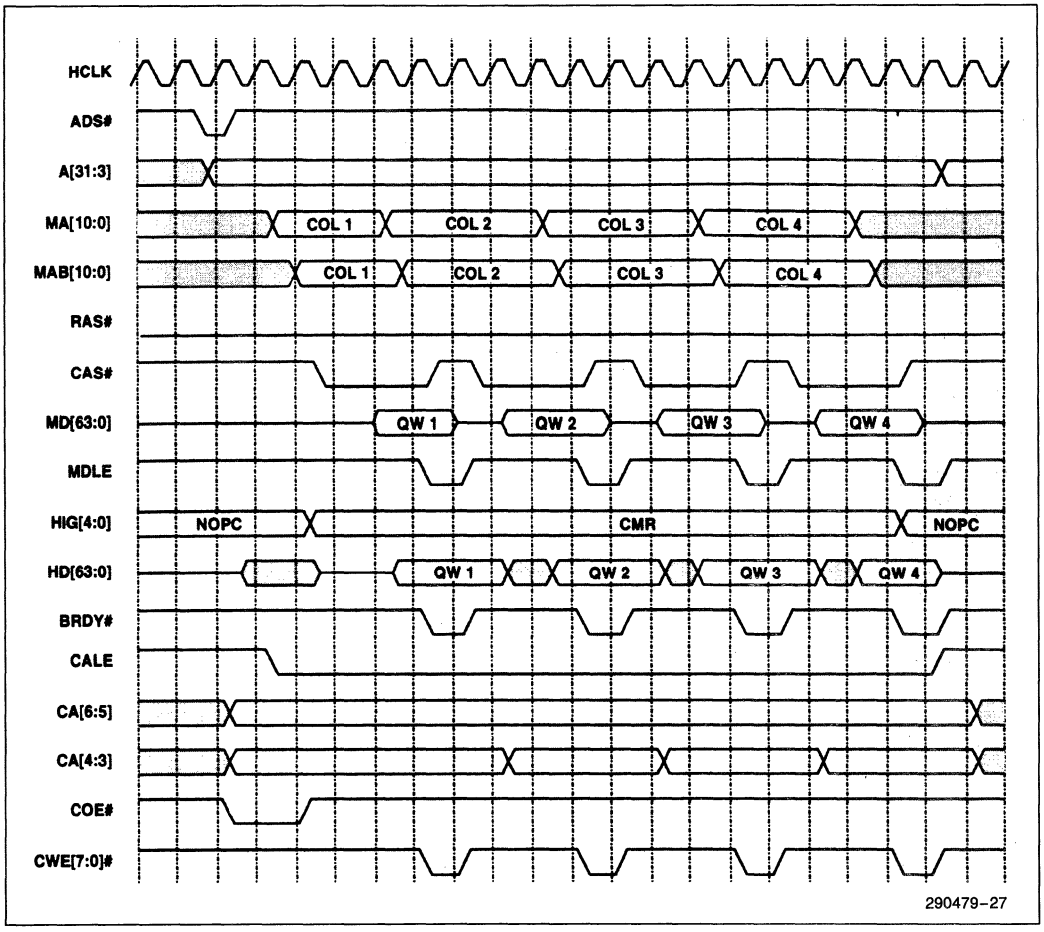


Figure 25. Cache Line Fill with Standard SRAM, DRAM Page Hit (82434LX)

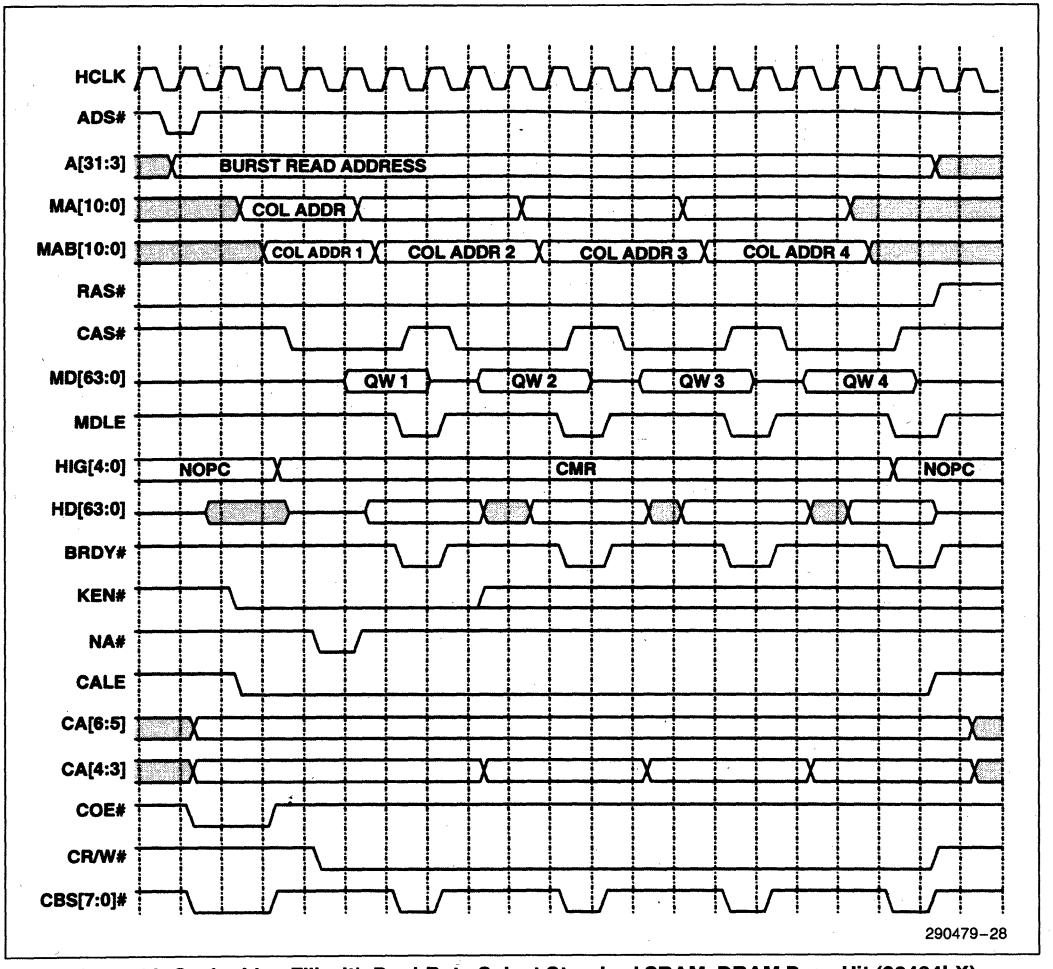


Figure 26. Cache Line Fill with Dual-Byte Select Standard SRAM, DRAM Page Hit (82434LX)

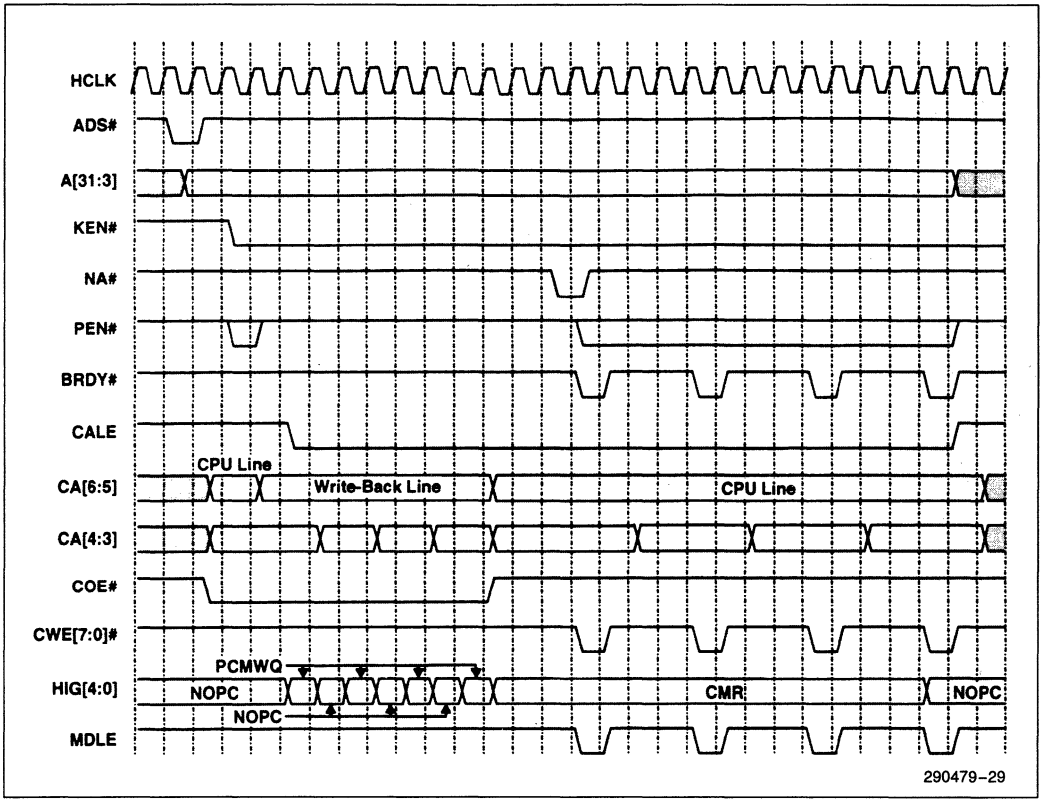


Figure 27. CPU Cache Read Miss, Write-Back, Line Fill with Standard SRAM (82434LX)

The CPU issues a memory read cycle that misses in the second level cache. In this instance, a modified line in the second level cache must be written back to main memory before the new line can be filled into the cache. The PCMC inspects the valid and modified bits for each of the lines within the addressed sector and writes back only the valid lines within the sector that are in the modified state. During the write-back cycle, CA[4:3] begin with the initial value driven by the Pentium processor and proceed in the Pentium processor burst order. CA[6:5] are used to count through the lines within the addressed sector. When two or more lines must be written back to main memory, CA[6:5] count in the direction from line 0 to line 3. CA[6:5] advance to the next line to be written back to main memory, skipping lines that are not modified. Figure 23 depicts the case of just one of the lines in a sector being written back to main memory. In this case, the entire line can be posted in the CPU-to-Main memory posted write buffer by driving the HIG[4:0] lines to the PCMWQ command as each Qword is read from the cache. At the same time, the required DRAM read cycle is beginning. As soon as the de-allocated line is written into the posted write buffer, the HIG[4:0] lines are driven to CMR (CPU Memory Read) to allow data to propagate from the DRAM data lines to the CPU data lines. The CWE[7:0]# lines are not generated from a delayed version of HCLK (as they are in the case of CPU to second level cache burst write), but from ordinary HCLK rising edges. CMR is driven on the HIG[4:0] lines

throughout the DRAM read portion of the cycle. With the fourth assertion of BRDY# the HIG[4:0] lines change to NOPC. The LBXs however, do not tri-state the host data lines until MDLE rises. CWE[7:0]# and MDLE track such that MDLE will not rise before CWE[7:0]#. Thus, the LBXs continue to drive the host data lines until CWE[7:0]# are negated. CA[6:3] remain at the valid values until the clock after the last BRDY#, providing address hold time to CWE[7:0]# rising.

PEN# is asserted as shown if the MCHK DRAM/L2 Cache Data Parity Error bit in the Error Command Register (offset 70h) is set. If the second level cache supports parity, PEN# is always asserted during CPU read cycles in the third clock in case the cycle hits in the cache.

If more than one line must be written back to main memory, the PCMC fills the CPU-to-Main Memory Posted Write Buffer and loads another Qword into the buffer as each Qword write completes into main memory. The writes into DRAM proceed as page hit write cycles from one line to the next, completing at a rate of X-4-4-4-5-4-4-4-5-4-4-4 for a three line write-back. All modified lines except for the last one to be written back are posted and written to memory before the DRAM read cycle begins. The last line to be written back is posted as the DRAM read cycle begins. Thus, the read data is returned to the CPU before the last line is retired to memory.

The line which was written into the second level cache is marked valid and unmodified by the PCMC. All the other lines in the sector are marked invalid. A subsequent CPU read cycle which hits in the same sector (but a different line) in the second level cache would then simply result in a line fill without any write-back.

5.1.3 BURST SRAM CACHE CYCLES (82434LX)

The following sections show the activity of the second level cache interface when burst SRAMs are used for the second level cache.

5.1.3.1 Burst Read (82434LX)

Figure 28 depicts a burst read from the second level cache with burst SRAMs.

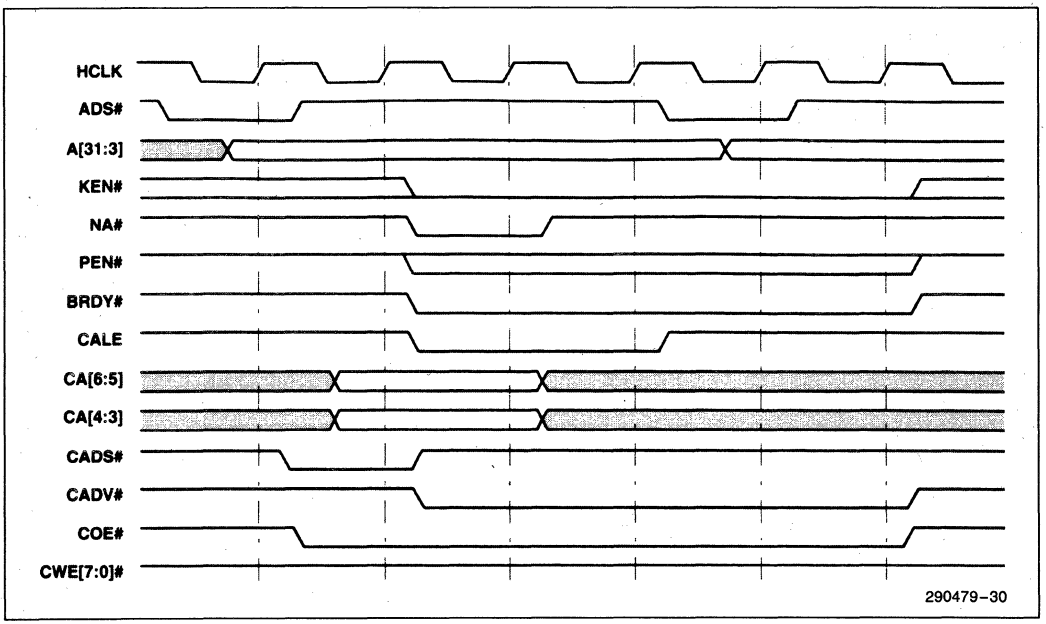


Figure 28. CPU Burst Read from Second Level Cache with Burst SRAM (82434LX)

The cycle begins with the CPU driving address and status onto Host Bus and asserting ADS#. The PCMC asserts CADS# and COE# in the second clock. After the address is latched by the burst SRAMs and the PCMC determines that no write-back cycles are required from the second level cache, CALE is negated. Back-to-back burst reads from the second level cache are shown in Figure 29.

When the Secondary Cache Allocation (SCA) bit in the Secondary Cache Control Register is set to 1, the PCMC performs a line fill in the secondary cache, even if the CACHE# signal from the CPU is negated. In this case, AHOLD is asserted to prevent the CPU from beginning a new cycle while the second level cache line fill is completing.

Back-to-back burst reads which hit in the second level cache complete at a rate of 3-1-1-1/1-1-1-1 with burst SRAMs. As the last BRDY# is being returned to the CPU, the PCMC asserts CADS# causing the SRAMs to latch the new address. This allows the data for the second cycle to be transferred to the CPU on the clock after the first cycle completes.

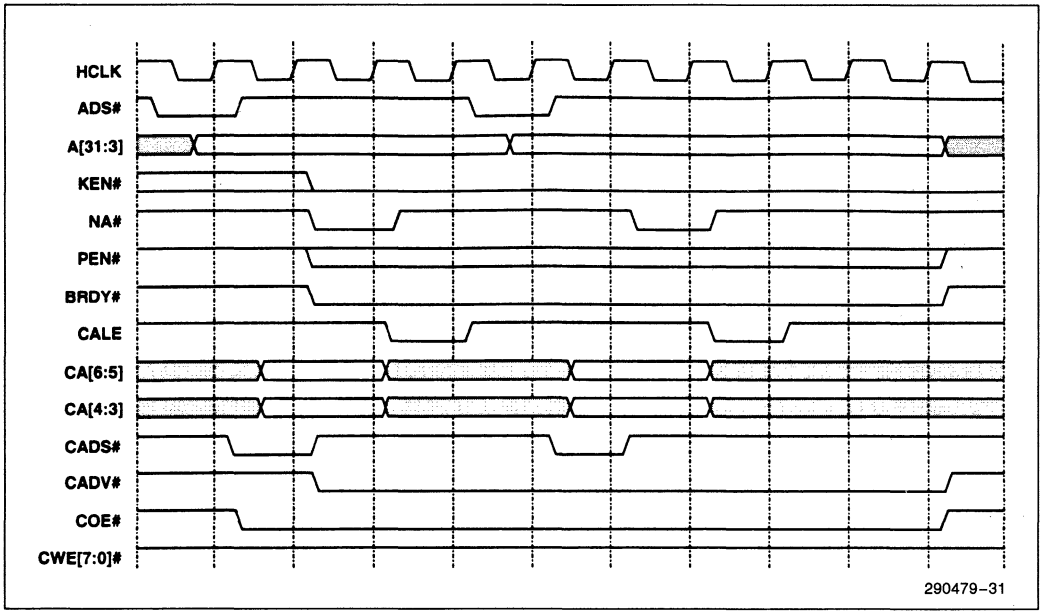


Figure 29. Pipelined Back-to-Back Burst Reads from Second Level Cache (82434LX)

5.1.3.2 Burst Write (82434LX)

A burst write cycle is used to write back a line from the first level cache to either the second level cache or DRAM. A burst write cycle from the first level cache to the second level cache is shown in Figure 30.

The Pentium processor always writes back lines starting with the low order Qword advancing to the high order Qword. CADS# is asserted in the second clock. CWE[7:0]# and BRDY# are asserted in the third clock. CADV# assertion is delayed by one clock relative to the burst read cycle. HIG[4:0] are driven to PCMWQ (Post CPU-to-Memory Write Buffer Qword) only when the PCMC is programmed for a write-through write policy. When programmed for write-back mode, the modified bit associated with the line is set within the PCMC. The single write is very similar to the first write in a burst write. CADS# is asserted in the second clock. BRDY# and CWE[7:0]# are asserted in the third clock. A burst read cycle followed by a pipelined single write cycle is depicted in Figure 31.

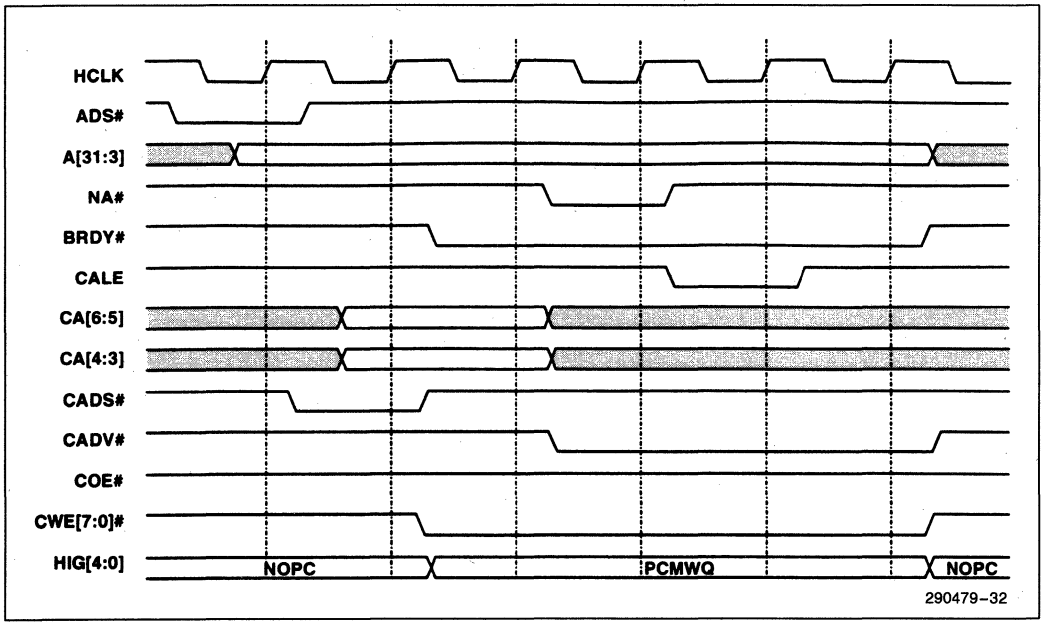


Figure 30. Burst Write to Second Level Cache with Burst SRAM (82434LX)

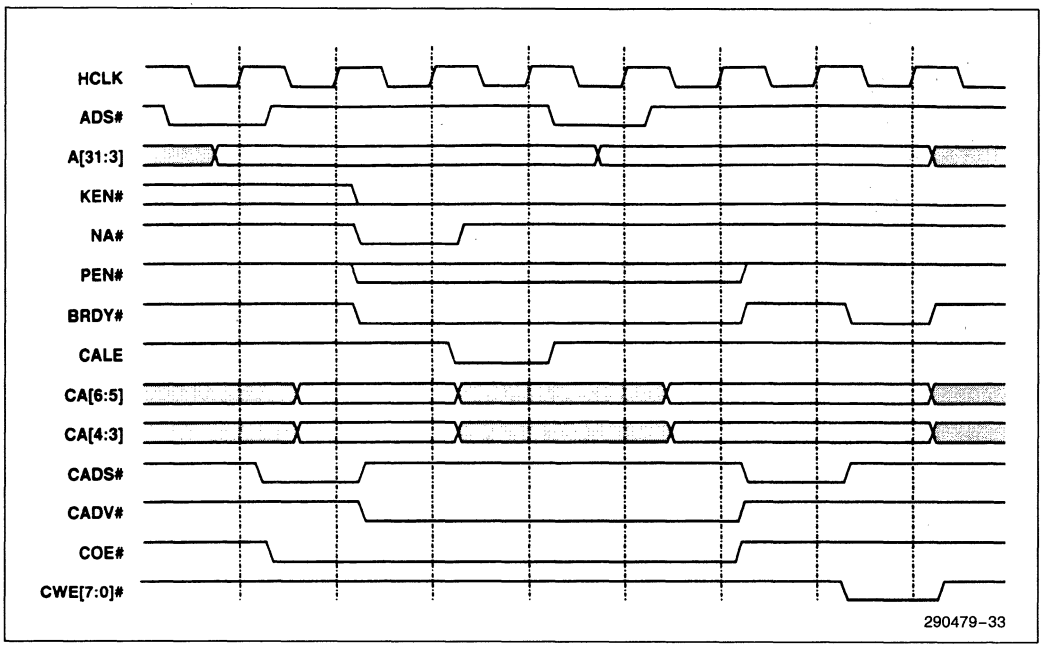


Figure 31. Burst Read Followed by Pipelined Single Write Cycle with Burst SRAM (82434LX)

5.1.3.3 Cache Line Fill (82434LX)

If the CPU issues a memory read cycle to cacheable memory which does not hit in the second level cache, a cache line fill occurs. Figure 32 depicts a first and second level cache line fill with burst SRAMs.

Figure 33 depicts a CPU read cycle which forces a write-back in the second level cache.

Figure 32. Cache Line Fill with Burst SRAM, DRAM Page Hit, 7-4-4-4 Timing (82434LX)

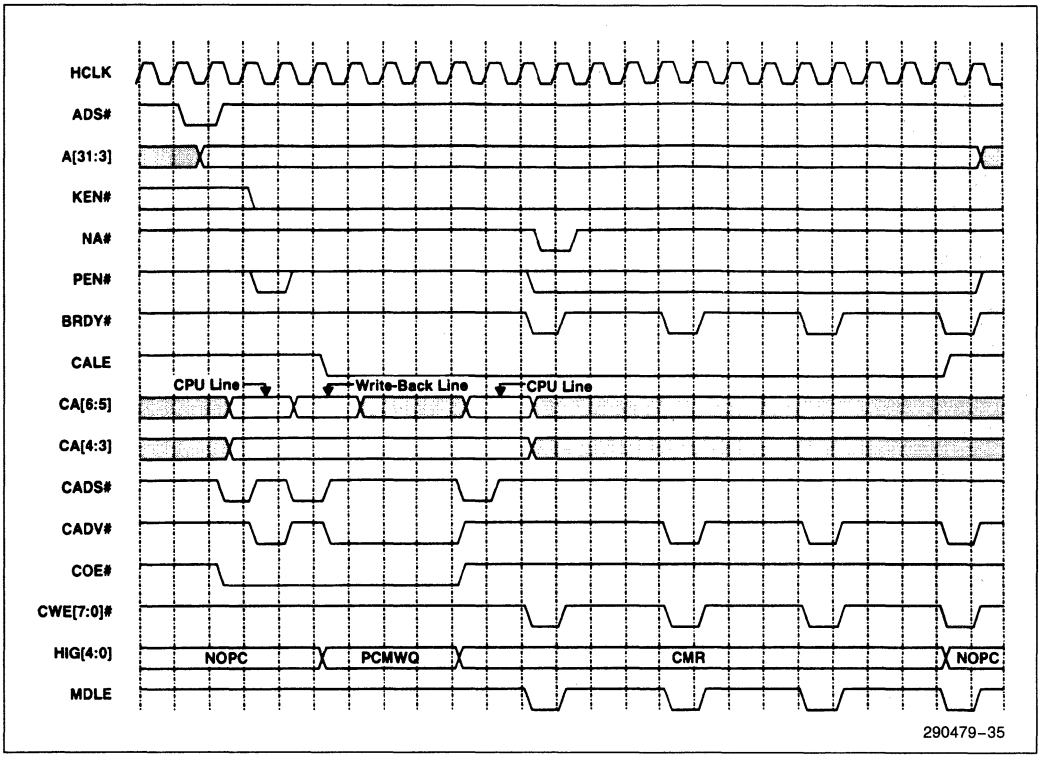


Figure 33. CPU Cache Read Miss, Write-Back, Line Fill with Burst SRAM (82434LX)

The CPU issues a memory read cycle which misses in the second level cache. In this instance, a modified line in the second level cache must be written back to main memory before the new line can be filled into the cache. The PCMC inspects the valid and modified bits for each of the lines within the addressed sector and writes back only the valid lines within the sector that are marked modified. CA[6:5] are used to count through the lines within the addressed sector. When two or more lines must be written back to main memory, CA[6:5] count in the direction from line 0 to line 3 after each line is written back. Figure 29 depicts the case of just one

of the lines in a sector being written back to main memory. In this case, the entire line can be posted in the CPU-to-Memory Posted Write Buffer by driving the HIG[4:0] lines to PCMWQ as each Qword is read from the cache. At the same time, the required DRAM read cycle is beginning. After the de-allocated line is written into the posted write buffer, the HIG[4:0] lines are driven to CMR (CPU Memory Read) to allow data to propagate from the DRAM data lines to the CPU data lines. Figure 29 assumes that the read from DRAM is a page hit and thus the first Qword is already read from the DRAMs when the transfer from cache to the CPU to Memory posting buffer is complete. The rest of the DRAM cycle completes at a -4-4-4 rate. CADV# is asserted with the last three BRDY# assertions. CMR is driven on the HIG[4:0] lines throughout the DRAM read portion of the cycle. Upon the fourth assertion of BRDY# the HIG[4:0] lines change to NOPC.

PEN# is asserted as shown if the MCHK DRAM/L2 Cache Data Parity Error bit in the Error Command Register (offset 70h) is set. If the second level cache supports parity, PEN# is always asserted during CPU read cycles in clock 3 in case the cycle hits in the cache.

If more than one line must be written back to main memory, the PCMC fills the CPU-to-Main Memory Posted Write Buffer and loads another Qword into the buffer as each Qword write completes into main memory. The writes into DRAM proceed as page hit write cycles from one line to the next, completing at a rate of X-4-4-4-5-4-4-4-5-4-4-4 for a three line write-back when programmed for X-4-4-4 DRAM write timing or X-3-3-3-4-3-3-3-4-3-3-3 when programmed for X-3-3-3 DRAM write timing. All modified lines except for the last one to be written back to memory are posted and retired to memory before the DRAM read cycle begins. The last line to be written back is posted as the DRAM read cycle begins. Thus, the read data is returned to the CPU before the last line is retired to memory.

The line which was written into the second level cache is marked valid and unmodified by the PCMC. All the other lines in the block are marked invalid. A subsequent CPU read cycle which hits the same sector (but a different line) in the second level cache results in a line fill without any write-back.

5.1.4 SNOOP CYCLES

Snoop cycles are the same for the 82434LX and 82434NX. The inquire cycle is used to probe the first level and second level caches when a PCI master attempts to access main memory. This is done to maintain coherency between the first and second level caches and main memory. When a PCI master first attempts to access main memory a snoop request is generated inside the PCMC. The PCMC supports up to two outstanding cycles on the CPU address bus at a time. Outstanding cycles include both CPU initiated cycles and snoop cycles. Thus, if the Pentium processor pipelines a second cycle onto the host address bus, the PCMC will not issue a snoop cycle until the first CPU cycle terminates. If the PCMC were to initiate a snoop cycle before the first CPU cycle were complete then for a brief period of time, three cycles would be outstanding. Thus, a snoop request is serviced with a snoop cycle only when either no cycle is outstanding on the CPU bus or one cycle is outstanding.

Snoop cycles are performed by driving the PCI master address onto the CPU address bus and asserting EADS#. The Pentium processor then performs a tag lookup to determine if the addressed memory is in the first level cache. At the same time the PCMC performs an internal tag lookup to determine if the addressed memory is in the second level cache. Table 7 describes how a PCI master read from main memory is serviced by the PCMC.

Table 7. Data Transfers for PCI Master Reads from Main Memory

Snoop Result		Action
First Level Cache	**Second Level Cache**	
Miss	Miss	Data is transferred from DRAM to PCI.
Miss	Hit Unmodified Line	Data is transferred directly from second level cache to PCI. The line remains valid and unmodified in the second level cache.
Miss	Hit Modified Line	Data is transferred directly from second level cache to PCI. Line remains valid and modified in the second level cache. The line is not written to DRAM.
Hit Unmodified Line	Miss	Data is transferred from DRAM to PCI.
Hit Unmodified Line	Hit Unmodified Line	Data is transferred directly from second level cache to PCI. The line remains valid and unmodified in the second level cache.
Hit Unmodified Line	Hit Modified Line	Data is transferred directly from second level cache to PCI. Line remains valid and modified in the second level cache. The line is not written to DRAM.
Hit Modified Line	Miss	A write-back from first level cache occurs. The data is sent to both PCI and the CPU-to-Memory Posted Write Buffer. The CPU-to-Memory Posted Write Buffer is then written to memory.
Hit Modified Line	Hit Unmodified Line	A write-back from first level cache occurs. The data is posted to PCI and written into the second level cache. When the second level cache is in write-back mode, the line is marked modified and is not written to DRAM. When the second level cache is in write-through mode, the line is posted and then written to DRAM.
Hit Modified Line	Hit Modified Line	A write-back from first level cache occurs. The data is posted to PCI and written into the second level cache. The line is not written to DRAM. This scenario can only occur when the second level cache is in write-back mode.

PCI master write cycles never result in a write directly into the second level cache. A snoop hit to a modified line in either the first level or second level cache results in a write-back of the line to main memory. The line is invalidated and the PCI write to main memory occurs after the write-back completes. The other lines in the sector are not written back to main memory or invalidated. A PCI master write snoop hit to an unmodified line in either the first level or second level cache results in the line being invalidated. Table 8 describes the actions taken by the PCMC when a PCI master writes to main memory.

Table 8. Data Transfers for PCI Master Writes to Main Memory

Snoop Result		Action
First Level Cache	Second Level Cache	
Miss	Miss	The PCI master write data is transferred from PCI to DRAM.
Miss	Hit Unmodified Line	The PCI master write data is transferred from PCI to DRAM. The line is invalidated in the second level cache.
Miss	Hit Modified Line	A write-back from second level cache to DRAM occurs. The PCI master write data is then written to DRAM. The line is invalidated in the second level cache.
Hit Unmodified Line	Miss	The first level cache line is invalidated. The PCI master write data is written to DRAM.
Hit Unmodified Line	Hit Unmodified Line	The line is invalidated in both the first level and second level caches. The PCI master write data is written to DRAM.
Hit Unmodified Line	Hit Modified Line	The first level cache line is invalidated. The second level cache line is written back to main memory and invalidated. The PCI master write data is then written to DRAM.
Hit Modified Line	Miss	The first level cache line is written back to DRAM and invalidated. The PCI master write data is then written to DRAM.
Hit Modified Line	Hit Unmodified Line	The first level cache line is written back to DRAM and invalidated. The second level cache line is invalidated. The PCI master write data is then written to DRAM.
Hit Modified Line	Hit Modified Line	The first level cache line is written back to DRAM and invalidated. The second level cache line is invalidated. The PCI master write data is then written to DRAM.

A snoop hit results in one of three transfers; a write-back from the first level cache posted to the LBXs, a write-back from the second level cache posted to the LBXs or a write-back from the first level cache posted to the LBXs and written to the second level cache. A snoop cycle that does not result in a write-back is depicted in Figure 34.

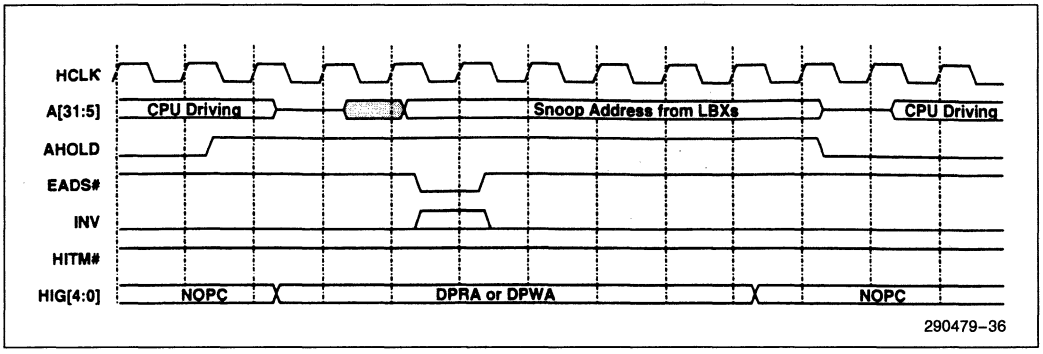


Figure 34. Snoop Hit to Unmodified Line in First Level Cache or Snoop Miss

The PCMC begins to service the snoop request by asserting AHOLD, causing the Pentium processor to tri-state the address bus in the clock after assertion. In the case of a PCI master read cycle, the PCMC drives the DPRA (Drive PCI Read Address) command onto the HIG[4:0] lines causing the LBXs to drive the PCI address onto the host address bus. For a write cycle, the PCMC drives the DPWA (Drive PCI Write Address to CPU Address Bus) command on the HIG[4:0] lines, also causing the LBXs to begin driving the host address bus. The PCMC then asserts EADS#, initiating the snoop cycle to the CPU. The INV signal is asserted by the PCMC only during snoops due to PCI master writes. INV remains negated during snoops due to PCI master reads. If the snoop results in a hit to a modified line in the first level cache, the Pentium processor asserts HITM#. The PCMC samples the HITM# signal two clocks after the CPU samples EADS# asserted to determine if the snoop hit in the first level cache. By this time the PCMC has completed an internal tag lookup to determine if the line is in the second level cache. Since this snoop does not result in a write-back, the NOPC command is driven on the HIG[4:0] lines, causing the LBXs to tri-state the address bus. The sequence ends with AHOLD negation.

If the Pentium processor asserts ADS# in the same clock as the PCMC asserts AHOLD, the PCMC will assert BOFF# in two cases. First, if the snoop cycle hits a modified line in the first level cache, the PCMC will assert BOFF# for 1 HCLK to re-order the write-back around the currently sending cycle. Second, if the snoop requires a write-back from the second level cache, the PCMC will assert BOFF# to enable the write-back from the secondary cache SRAMs.

Figure 35 depicts a snoop hit to a modified line in the first level cache due to a PCI master memory read cycle.

The snoop cycle begins when the PCMC asserts AHOLD causing the CPU to tri-state the address bus. The PCMC drives the DPRA (Drive PCI Read Address) command on to the HIG[4:0] lines causing the LBXs to drive the PCI address onto the host address bus. The PCMC then asserts EADS#, initiating the snoop to the first level cache. INV is not asserted since this is a PCI master read cycle. INV is only asserted with EADS# when the snoop cycle is in response to a PCI master write cycle. As the CPU is sampling EADS# asserted, the PCMC latches the address. Two clocks later, the PCMC completes the

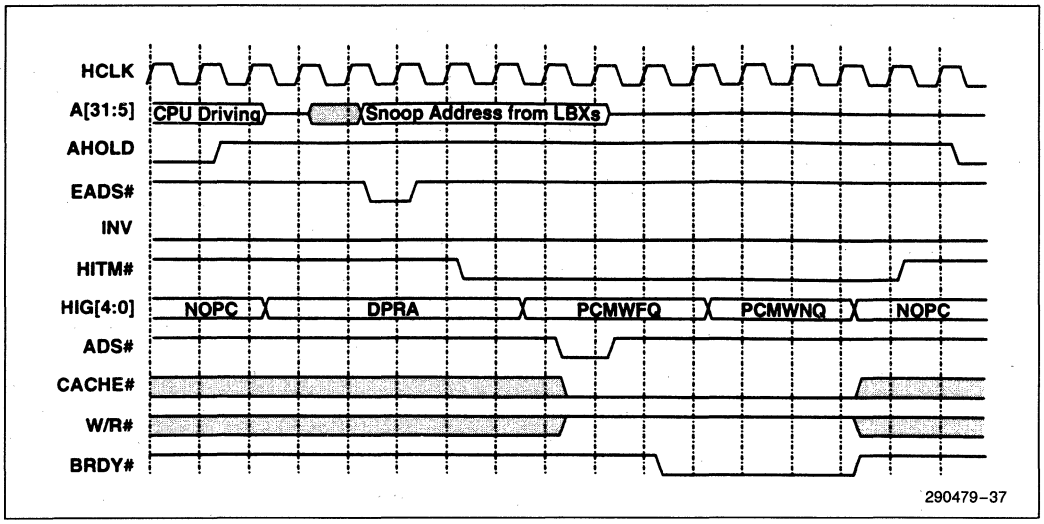


Figure 35. Snoop Hit to Modified Line in First Level Cache, Post Memory and PCI

internal tag lookup to determine if the line is in the second level cache. In this instance, the snoop hits a modified line in the first level cache and misses in the second level cache. Thus, the second level cache is not involved in the write-back cycle. The PCMC allows the LBXs to stop driving the address lines by driving NOPC command on the HIG[4:0] lines. The CPU then drives the write-back cycle onto the bus by asserting ADS# and driving the write-back data on the data lines even though AHOLD is still asserted. The write-back into the LBX buffers occurs at a rate of 3-1-1-1. The PCMC drives PCMWFQ on the HIG[4:0] lines for one clock causing the write data to be posted to both PCI and main memory. For the next three clocks, the HIG[4:0] lines are driven to PCMWNQ, posting the final three Qwords to both PCI and main memory.

A similar transfer from first level cache to the LBXs occurs when a snoop due to a PCI master write hits a modified line in the first level cache. In this case, the write-back is transferred to the CPU-to-Memory Posted Write Buffer. If the line is in the second level cache, it is invalidated. The cycle is similar to the snoop cycle shown above with two exceptions. The PCMC drives the DPWA command on the HIG[4:0] lines instead of the DPRA command. During the four clocks where the PCMC drives BRDY# active to the CPU, it also drives PCMWQ on the HIG[4:0] lines, causing the write to be posted to main memory.

In both of the above cases where a write-back from the first level cache is required, AHOLD is asserted until the write-back is complete. If the CPU has begun a read cycle directed to PCI and the snoop results in a hit to a modified line in the first level cache, BOFF# is asserted for one clock to abort the CPU read cycle and re-order the write-back cycle before the read cycle.

When a PCI master read or write cycle hits a modified line in the second level cache and either misses in the first level cache or hits an unmodified line in the first level cache, a write-back from the second level cache to the LBXs occurs. When a PCI master write snoop hits an unmodified line in the second level cache and either misses in the first level cache or hits an unmodified line in the first level cache, no data transfer from the second level cache occurs. The line is simply invalidated. In the case of a PCI master write cycle, the line is invalidated in both the first level and second level caches. In the case of a PCI master memory read cycle, neither cache is invalidated. A PCI master read from main memory which hits either a modified or unmodified line in the second level cache is shown in Figure 36.

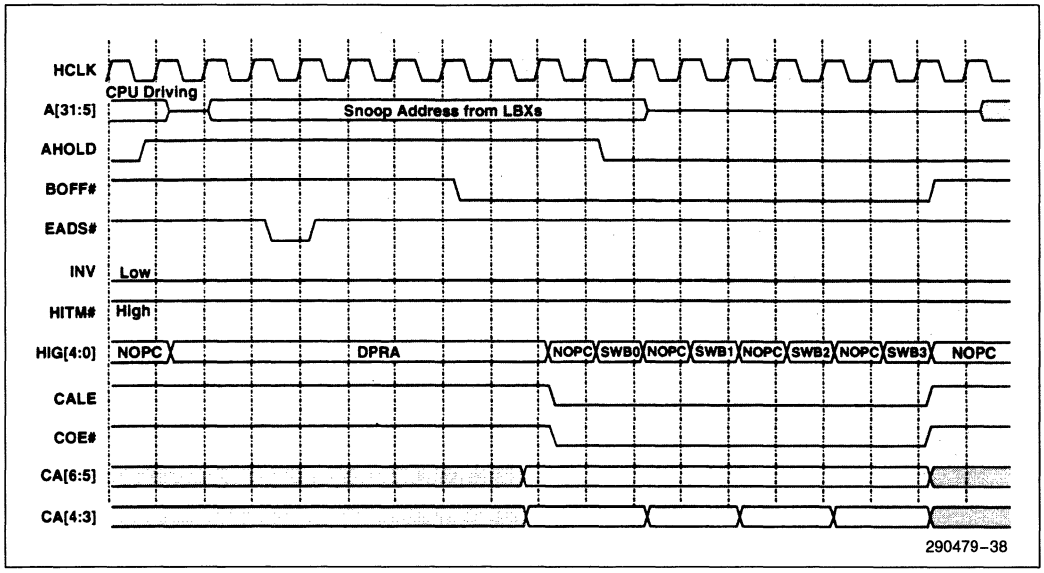


Figure 36. Snoop Hit to Modified Line in Second Level Cache, Store in PCI Read Prefetch Buffer

The snoop cycle begins with the PCMC asserting AHOLD, causing the CPU to tri-state the host address bus. The PCMC drives the DPRA command enabling the LBXs to drive the snoop address onto the host address bus. The PCMC asserts EADS#. INV is not asserted in this case since the snoop cycle is in response to a PCI master read cycle. If the snoop were in response to a PCI master write cycle then INV would be asserted with EADS#. Two clocks after the CPU samples EADS# active, the PCMC completes the internal tag lookup. In this case the snoop hit either an unmodified line or a modified line in the second level cache. Since HITM# is inactive, the snoop did not hit in the first level cache. The PCMC then schedules a read from the second level cache to be written to the LBXs. When the CPU burst cycle completes the PCMC negates the control signals to the second level cache and asserts CALE opening the cache address latch and allowing the snoop address to flow through to the SRAMs. The second level cache executes a read sequence which completes at 3-2-2-2 in the case of standard SRAMs and 3-1-1-1 in the case of burst SRAMs. During all snoop cycles where a write-back from the second level cache is required, BOFF# is asserted throughout the write-back cycle. This prevents the deadlock that would occur if the CPU is in the middle of a non-postable write and the data bus is required for the second level cache write-back.

When using burst SRAMs, the read from the SRAMs follows the Pentium processor burst order. However, the memory to PCI read prefetch buffer in the LBXs is organized as a FIFO and cannot accept data out of order. The SWB0, SWB1, SWB2 and SWB3 commands are used to write data into the buffer in ascending order. In the above example, the PCI master requests a data item which hits Qword 0 in the cache, thus CA[4:3] count through the following sequence: 0, 1, 2, 3 (00, 01, 10, 11). If the PCI mas-

ter requests a data item that hits Qword 1, the SWB0 command is sent via the HIG[4:0] lines to store Qword 1in the first buffer location. The next read from the cache is not in ascending order, thus a NOPC is sent on the HIG[4:0] lines. This Qword is not posted in the buffer. The next read from the cache is to Qword 3. SWB2 is sent on the HIG[4:0] lines. The final read from the cache is Qword 2. SWB1 is sent on the HIG[4:0] lines. Thus, Qword 1 is placed in entry 0 in the buffer, Qword 2 is placed in entry 1 in the buffer and Qword 3 is placed in entry 2 in the buffer. The ordering between the Qwords read from the cache and the HIG[4:0] commands when using burst SRAMs is summarized in Table 9.

Table 9. HIG[4:0] Command Sequence for Second Level Cache to PCI Master Read Prefetch Buffer Transfer

Burst Order from Cache	HIG[4:0] Command Sequence
0, 1, 2, 3	SWB0, SWB1, SWB2, SWB3
1, 0, 3, 2	SWB0, NOPC, SWB2, SWB1
2, 3, 0, 1	SWB0, SWB1, NOPC, NOPC
3, 2, 1, 0	SWB0, NOPC, NOPC, NOPC

When using standard asynchronous SRAMs, the read from the SRAMs occurs in a linear burst order. Thus, CAA[4:3] and CAB[4:3] count in a linear burst order and the Store Write Buffer commands are sent in linear order. The burst ends at the cache line boundary and does not wrap around and continue with the beginning of the cache line.

A PCI master write cycle which hits a modified line in the second level cache and either hits an unmodified line in the first level cache or misses in the first level cache will also cause a transfer from the second level cache to the LBXs. In this case, the read from the SRAMs is posted to main memory and the line is invalidated in the second level cache. The cycle would differ only slightly from the above cycle. INV would be asserted with EADS#. Instead of the DPRA command, the PCMC would use the DPWA command to drive the snoop address onto the host address bus. The write would be posted to the DRAM, thus the PCMC would drive the PCMWQ command on the HIG[4:0] lines to post the write to DRAM.

A snoop cycle can result in a write-back from the first level cache to both the second level and LBXs in the case of a PCI master read cycle which hits a modified line in the first level cache and hits either a modified or unmodified line in the second level cache. The line is written to both the second level cache and the memory to PCI read prefetch buffer. The cycle is shown in Figure 37.

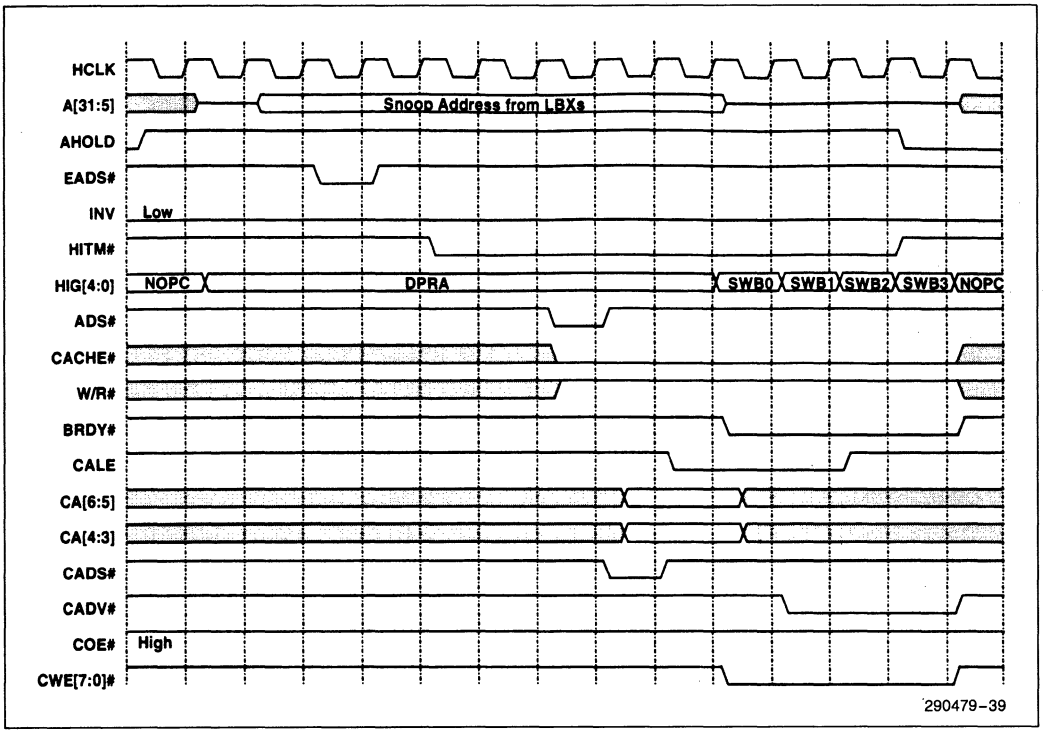


Figure 37. Snoop Hit to Modified Line in First Level Cache, Write-Back from First Level Cache to Second Level Cache and Send to PCI

This cycle is shown for the case of a second level cache with burst SRAMs. In this case, as it completes the second level cache tag lookup, the PCMC samples HITM# active. The write-back is written to the second level cache and simultaneously stored in the memory to PCI prefetch buffer. In the case shown in Figure 33, the PCI master requests a data item which is contained in Qword 0 of the cache line. Note that a write-back from the first level cache always starts with Qword 0 and finishes with Qword 3. Thus the HIG[4:0] lines are sequenced through the following order: SWB0, SWB1, SWB2, SWB3. If the PCI master requests a data item which is contained in Qword 1, the HIG[4:0] lines sequence through the following order: NOPC, SWB0, SWB1, SWB2. If the PCI master requests a data item which is contained in Qword 2, the HIG[4:0] lines sequence through the following order: NOPC, NOPC, SWB0, SWB1. If the PCI master requests a data item which is contained in Qword 3, the HIG[4:0] lines sequence through the following order: NOPC, NOPC, NOPC, SWB0. AHOLD is negated after the write-back cycle is complete.

If the CPU has begun a read cycle directed to PCI and the snoop results in a hit to a modified line in the first level cache, BOFF# is asserted for one clock to abort the CPU read cycle and re-order the write-back cycle before the pending read cycle.

5.1.5 FLUSH, FLUSH ACKNOWLEDGE AND WRITE-BACK SPECIAL CYCLES

There are three special cycles that affect the second level cache, flush, flush acknowledge, and write-back. If the processor executes an INVD instruction, it will invalidate all unmodified first level cache lines and issue a flush special cycle. If the processor executes a WBINVD instruction, it will write back all modified first level cache lines, invalidate the first level cache, and issue a write-back special cycle followed by a flush special cycle. If the Pentium processor FLUSH# pin is asserted, the CPU will write-back all modified first level cache lines, invalidate the first level cache, and issue a flush acknowledge special cycle.

The second level cache behaves the same way in response to the flush special cycle and flush acknowledge special cycle. Each tag is read and the valid and modified bits are examined. If the line is both valid and modified it is written back to main memory and the valid bit for that line is reset. All valid and unmodified lines are simply marked invalid. The PCMC advances to the next tag when all lines within the current sector have been examined. BRDY# is returned to the Pentium processor after all modified lines in the second level cache have been written back to main memory and all of the valid bits for the second level cache are reset. The sequence of write-back cycles will only be interrupted to service a PCI master cycle.

The write-back special cycle is ignored by the PCMC because all modified lines will be written back to main memory by the following flush special cycle. Upon decoding a write-back special cycle, the PCMC simply returns BRDY# to the Pentium processor.

5.2 82434NX Cache

The 82434NX PCMC integrates a high performance write-back second level cache controller, tag RAM and a full first and second level cache coherency mechanism. The cache is either 256 KBytes or 512 KBytes using either synchronous burst SRAMs or standard asynchronous SRAMs. Parity on the data SRAMs is optional. The cache uses a write-back write policy. Write-through mode is not supported.

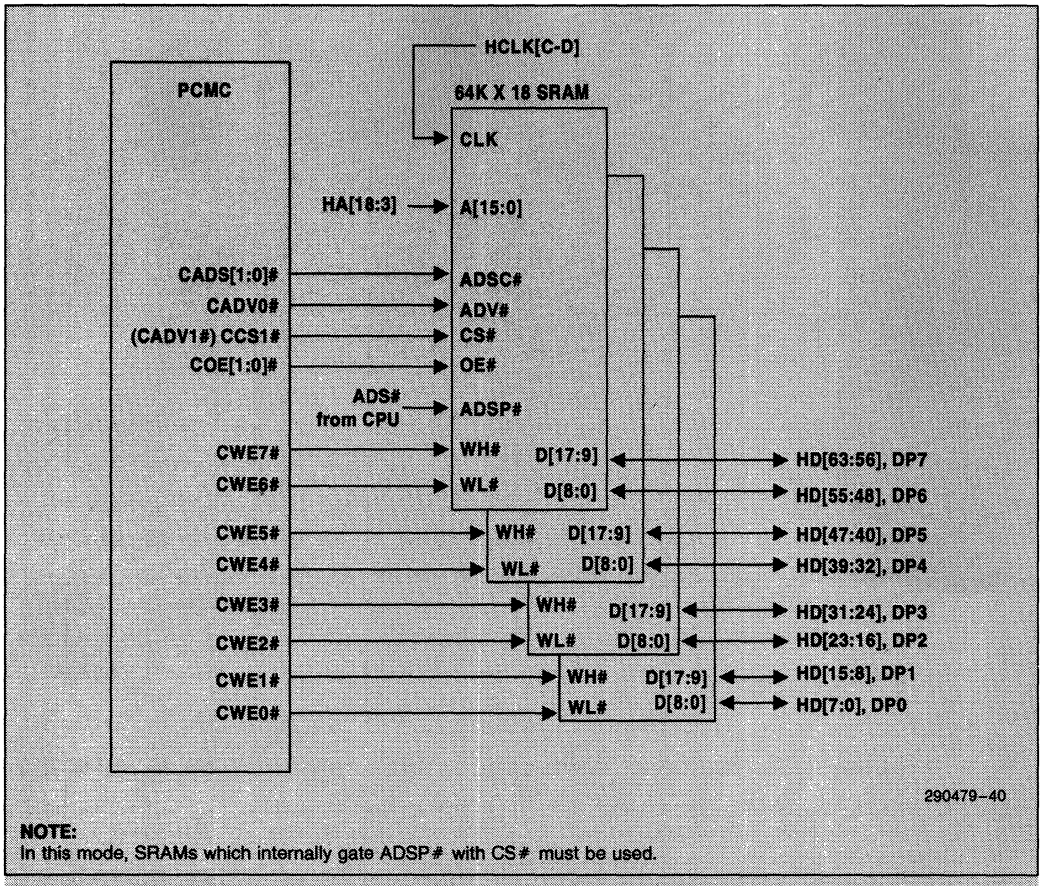
The 82434NX PCMC supports a direct mapped secondary cache. The PCMC contains 4096 tags. Each tag represents a sector in the cache. If the cache is 512 KB, each sector contains four cache lines. If the cache is 256 KB, each sector contains two cache lines. *Valid* and *Modified* bits are kept on a per line basis. The 82434NX Tag RAM is 1 bit wider than the 82434LX Tag RAM.

The PCMC can be configured to cache main memory on read cycles even when CACHE# is not asserted. When bit 4 in the Secondary Cache Control Register (offset 52h) is set to 1, all accesses to main memory, except those to SMM memory or any range marked non-cacheable via the PAM registers, are cached in the secondary cache. Accesses with CACHE# asserted result in a line fill in both the first and second level cache while accesses with CACHE# negated result in a line fill only in the second level cache. When bit 4 in the SCC Register is set to 0, only access with CACHE# asserted can generate a first and second level cache line fill.

When a Halt or Stop Grant Special Cycle is detected from the CPU, the 82434NX PCMC places the second level cache into the low power stand-by mode by deselecting the SRAMs and then generates the corresponding special cycle on PCI. (i.e., if the CPU cycle was a halt special cycle then the PCMC generates a halt special cycle on PCI and if the CPU cycle is a stop grant special cycle the PCMC generates a stop grant special cycle on PCI).

When a burst SRAM secondary cache is implemented, bit 2 of the Secondary Cache Control Register (offset 52h) is used to select between 82434LX SRAM connectivity and the new 82434NX SRAM connectivity. When set to 0, the secondary cache interface is in 82430-compatible mode. (i.e., the four low order address lines on the SRAMs are connected to CAA/B[6:3] on the PCMC. When set to 1, second level cache stand-by is enabled and no latch is used between the host CPU address lines and the SRAM address lines. All of the SRAM address lines are then connected directly to the CPU address lines. Write-back addresses are driven by the PCMC over the host address lines. When a standard SRAM secondary cache is implemented, bit 2 of the Secondary Cache Control Register (offset 52h) is used to enable second level cache stand-by. The default value of this bit is 0.

Figure 38 and Figure 41 show the connections between the PCMC and the external cache data SRAMs and latch for the case of an asynchronous SRAM cache.



NOTE:
In this mode, SRAMs which internally gate ADSP# with CS# must be used.

Figure 38. 512 KByte Secondary Cache, Synchronous Burst SRAM (82434NX)

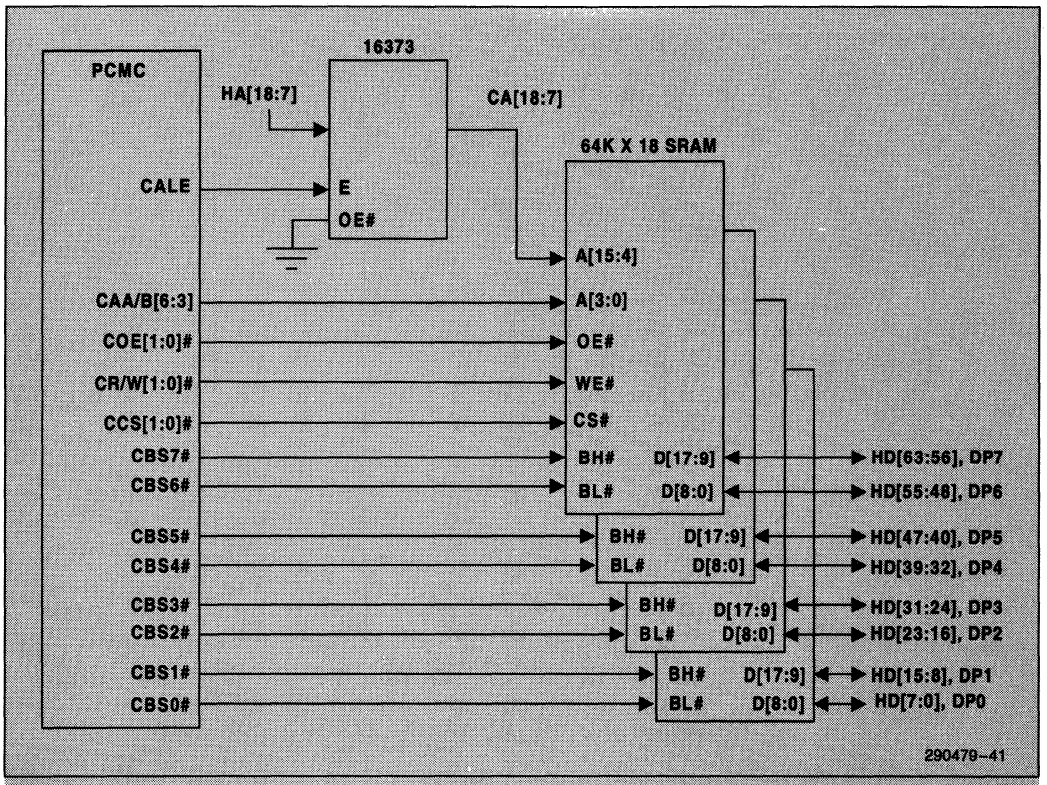


Figure 39. 512 KByte Secondary Cache, Standard Dual-Byte-Select (Asynch) SRAM, 50, 60 & 66 MHz

Figure 38 depicts the PCMC connections to a 512 KByte burst SRAM secondary cache when the PCMC is configured for 50, 60, or 66 MHz operation. Host address lines HA[18:3] are connected directly to the SRAM address lines, A[15:0]. ADS# from the CPU is connected to ADSP# on the SRAMs. CADV0# implements the address advance (ADV#) functionality. A new signal, CCS#, is multiplexed onto the CADV1# pin. When bit 2 in the SCC register is set to 1, SRAMs containing logic which gates ADSP# with CS# must be used. When negated, CCS# prevents the SRAMs from latching a new address due to a pipelined ADS# from the CPU during cache line fills. Note that, unlike the burst SRAM configuration with the 82430 PCIset, no external latch is used between the CPU address bus and the SRAM address lines. The SRAM Connectivity bit (bit 2) in the Secondary Cache Control register (offset 52h) must be set to 1 when using this cache configuration.

If the tag lookup results in a miss in the cache and the sector to be replaced contains one or more modified lines, the PCMC drives the write-back address from the A[18:3] lines on the host bus. Although not used in the write-back, A[31:19] (or A[31:18] in the case of a 256 KB cache) are driven to valid logic levels by the PCMC.

Figure 39 depicts the 82434NX PCMC connections to a 512 KByte standard asynchronous SRAM secondary cache. Figure 40 depicts the 82434NX connections to a 256 KByte asynchronous SRAM secondary cache. Host address lines HA[18:7] are driven through an external latch to form the upper SRAM address lines, CA[18:7]. CA[6:3] are driven from the PCMC. Figure 41 depicts the 82434NX PCMC connections to a 512 KByte standard SRAM secondary cache with dual-write-enable SRAMs.

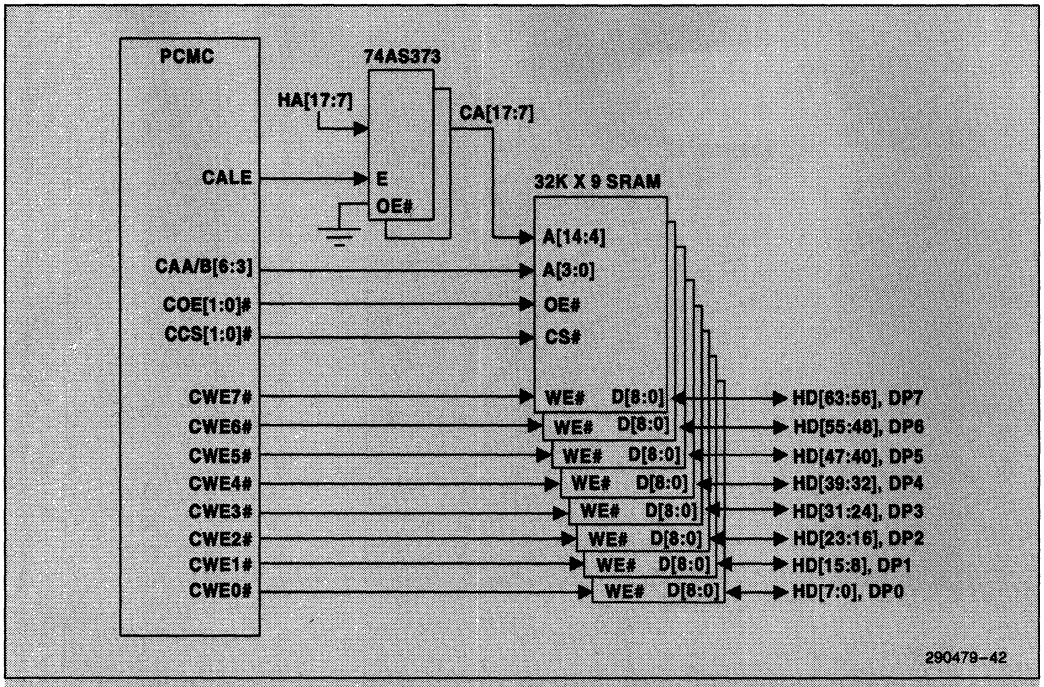


Figure 40. 82434NX Connections to 256 KByte Cache with Standard SRAM

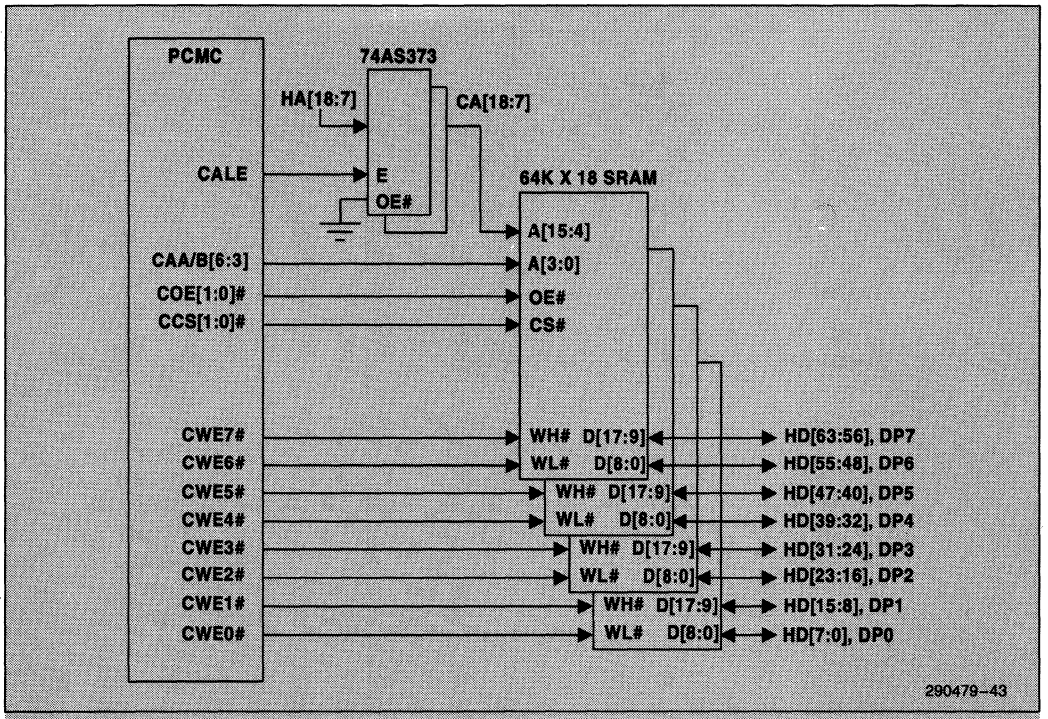


Figure 41. 82434NX Connections to 512 KByte Cache with Standard SRAM

5.2.1 CYCLE LATENCY SUMMARY (82434NX)

Table 10 and Table 11 summarize the clock latencies for CPU memory cycles which hit in the secondary cache.

Table 10. Secondary Cache Latencies with Synchronous Burst SRAM

Cycle Type	50, 60 and 66 MHz
Burst Read	3-1-1-1
Burst Write	3-1-1-1
Single Read	3
Single Write	3
Pipelined Back-to-Back Burst Reads	3-1-1-1-1-1-1-1
Burst Read Followed by Pipelined Write	3-1-1-1-2

Table 11. Secondary Cache Latencies with Standard Asynchronous SRAM (82434NX)

Cycle Type	50, 60 and 66 MHz
Burst Read	3-2-2-2
Burst Write	4-2-2-2
Single Read	3
Single Write	4
Pipelined Back-to-Back Burst Reads	3-2-2-2-3-2-2-2
Burst Read Followed by Pipelined Write	3-2-2-2-4

The 60 MHz and 66 MHz asynchronous SRAM latencies require 15 ns and 12 ns SRAMs, respectively. The 82434NX PCMC supports asynchronous SRAMs at 50 MHz. The 50 MHz (1 wait-state) timings require 20 ns SRAMs. The burst SRAMs speeds for 66 MHz, 60 MHz and 50 MHz operation are 8 ns, 9 ns, and 13 ns clock-to-output valid into a 0 pF test load. The SRAM access times listed in this paragraph are recommendations. Actual access time requirements are a function of system board layout and routing and should be validated with electrical simulation.

5.2.2 STANDARD SRAM CACHE CYCLES (82434NX)

At 50, 60 and 66 MHz, the timing of the second level cache interface with standard asynchronous SRAMs is identical to the timing in the 82430LX PCIset. Compared to the 82434LX second level cache, one additional connection can be made from the PCMC to the SRAMs. The CCS[1:0]# pins, in the case of asynchronous SRAMs, are multiplexed onto the CADV[1:0]# pins. These are then connected to the SRAM CS# pins. The two copies are functionally identical. The two copies are provided for timing reasons. These pins allow the PCMC to deselect the SRAMs, putting them into standby mode. When a halt special cycle or a stop grant special cycle is detected from the CPU, the PCMC negates CCS[1:0]#, placing the SRAMs into the low power standby mode. The PCMC then generates a halt or stop grant special cycle on PCI.

5.2.3 SECOND LEVEL CACHE STANDBY

When the PCMC detects a halt or stop grant special cycle from the CPU, it first places the second level cache into the low power stand-by mode by deselecting the SRAMs and then generates a halt or stop grant special cycle on PCI.

With a standard SRAM secondary cache, a halt or stop grant special cycle from the CPU causes the PCMC to negate CCS[1:0]#, deselecting the SRAMs and placing them in a low power standby mode. When the cache is in stand-by mode, the first bus cycle from the CPU brings the cache out of stand-by and into active mode, enabling the SRAMs to service the cycle in the case of a hit to the cache. The PCMC asserts CCS[1:0]# as a propagation delay from the falling edge of ADS#. CCS[1:0]# are then left asserted until the next halt or stop grant special cycle is occurs. When exiting the powerdown state, the PCMC ignores the Secondary Cache Leadoff wait-states bit and executes a 3-2-2-2 read or 4-2-2-2 write in order to allow the SRAMs time to power up. In the case of a read cycle, COE[1:0]# are asserted in clock two as in the case of ordinary read cycles.

When the SRAMs are powered down, the PCMC asserts CCS[1:0]# when performing a snoop cycle, regardless of whether the cycle hits in the second level cache. The PCMC then negates CCS# after the snoop cycle is complete.

With a burst SRAM secondary cache, a halt or stop grant special cycle from the CPU causes the PCMC to negate CCS# and assert CADS[1:0]#, deselecting the SRAMs, placing them in a low power standby mode. CCS# is then asserted and is left asserted by the PCMC. Thus, when the first cycle is driven from the CPU, the SRAMs sample ADSP# and CS# active, placing them in active mode and initiating the first access.

If the SRAMs are required to service a snoop, they are brought out of power-down when the PCMC asserts CADS[1:0]#. The PCMC always asserts CADS[1:0]# with CCS# negated after a snoop cycle is complete, regardless of whether the SRAMs were powered down prior to the snoop cycle.

5.2.4 SNOOP CYCLES

For snoop operations, refer to Section 5.1, 82434LX Cache.

5.2.5 FLUSH, FLUSH ACKNOWLEDGE, AND WRITE-BACK SPECIAL CYCLES

For flush, flush acknowledge, and write-back special cycles, refer to Section 5.1, 82434LX Cache.

6.0 DRAM INTERFACE

This section describes the DRAM interface for the 82434LX DRAM Interface (Section 6.1) and the 82434NX DRAM Interface (Section 6.2). The differences are in the following areas:

1. Increased maximum DRAM memory size to 512 MBytes. An extra address line (MA11) has been added to the 82434NX.
2. Two additional RAS# lines for a total of eight (RAS[0:7]#.
3. Addition of 50 MHz host-bus optimized DRAM timing sets. Thus, the 82434LX supports 60 and 66 MHz frequencies and the 82434NX supports 50, 60, and 66 MHz.

6.1 82434LX DRAM Interface

The 82434LX PCMC integrates a high performance DRAM controller supporting from 2–192 MBytes of main memory. The PCMC generates the RAS#, CAS#, WE# and multiplexed addresses for the DRAM array, while the data path to DRAM is provided by two 82433LX LBXs. The DRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers are given in Section 3.0, Register Description. A brief overview of the registers which configure the DRAM interface is provided in this section.

The 82434LX controls a 64-bit memory array (72-bit including parity) ranging in size from 2 MBytes up to 192 MBytes using industry standard 36-bit wide memory modules with fast page-mode DRAMs. Both single- and double-sided SIMMs are supported. The eleven multiplexed address lines, MA[10:0] allow the PCMC to support 256K x 36, 1M x 36, and 4M x 36 SIMMs. The PCMC has six RAS# lines enabling the support of up to six rows of DRAM. Eight CAS# lines allow byte control over the array during read and write operations. The PCMC supports 70 and 60 ns DRAMs. The PCMC DRAM interface is synchronous to the CPU clock and supports page mode accesses to efficiently transfer data in bursts of four Qwords.

The DRAM interface of the PCMC is configured by the DRAM Control Mode Register (offset 57h) and the six DRAM Row Boundary (DRB) Registers (offsets 60h–65h). The DRAM Control Mode Register contains bits to configure the DRAM interface for RAS# modes and refresh options. In addition, DRAM Parity Error Reporting and System Management RAM space can be enabled and disabled. When System Management RAM is enabled, if SMIACT# from the Pentium processor is not asserted, all CPU read and write accesses to SMM memory are directed to PCI. The SMRAM Space Register at configuration space offset 72h provides additional control over the SMRAM space. The six DRB Registers define the size of each row in the memory array, enabling the PCMC to assert the proper RAS# line for accesses to the array.

CPU-to-Memory write posting and read-around-write operations are enabled and disabled via the Host Read/Write Buffer Control Register (offset 53h). PCI-to-Memory write posting is enabled and disabled via the PCI Read/Write Buffer Control Register (offset 54h). PCI master reads from main memory always result in the PCMC and LBXs reading the requested data and prefetching the next seven Dwords.

Seven Programmable Attribute Map (PAM) Registers (offsets 59h–5Fh) are used to specify the cacheability and read/write status of the memory space between 512 KBytes and 1 MByte. Each PAM Register defines a specific address area enabling the system to selectively mark specific memory ranges as cacheable, read-only, write-only, read/write or disabled. When a memory range is disabled, all CPU accesses to that range are directed to PCI.

Two other registers also affect the DRAM interface, the Memory Space Gap Register (offsets 78h–79h) and the Frame Buffer Range Register (offsets 7Ch–7Fh). The Memory Space Gap Register is used to place a logical hole in the memory space between 1 MByte to 16 MBytes to accommodate memory mapped ISA boards. The Frame Buffer Range Register, is used to map a linear frame buffer into the Memory Space Gap or above main memory. When enabled, accesses to these ranges are never directed to the DRAM interface, but are always directed to PCI.

6.1.1 DRAM CONFIGURATIONS

Figure 42 illustrates a 12-SIMM configuration which supports single-sided SIMMs. A row in the DRAM array is made up of two SIMMs which share a common RAS# line. SIMM0 and SIMM1 are connected to RAS0# and therefore, comprise row 0. SIMM10 and SIMM11 form row 5. Within any given row, the two SIMMs must be the same size. Among the six rows, SIMM densities can be mixed in any order. That is, there are no restrictions on the ordering of SIMM densities among the six rows.

The low order LBX (LBXL) is connected to byte lanes 5, 4, 1, and 0 of the host and memory data buses, and the lower two bytes of the PCI AD bus. The high order LBX (LBXH) is connected to byte lanes 7, 6, 3, and 2 of the host and memory data buses, and the upper two bytes of the PCI AD bus. Thus, SIMMs connected to LBXL are connected to CAS[5:4,1:0]# and SIMMs connected to LBXH are connected to CAS[7:6, 3:2]#.

The MA[10:0] and WE# lines are externally buffered to drive the large capacitance of the memory array. Three buffered copies of the MA[10:0] and WE# signals are required to drive the six row array.

Figure 43 illustrates a 6-SIMM configuration that supports either single- or double-sided SIMMs. In this configuration, single- and double-sided SIMMs can be mixed. For example, if single-sided SIMMs are installed into the sockets marked SIMM0 and SIMM1, then RAS0# is connected to the SIMMs and RAS1# is not connected. Row 0 is then populated and row 1 is empty. Two double-sided SIMMs could then be installed in the sockets marked SIMM2 and SIMM3, populating rows 2 and 3.

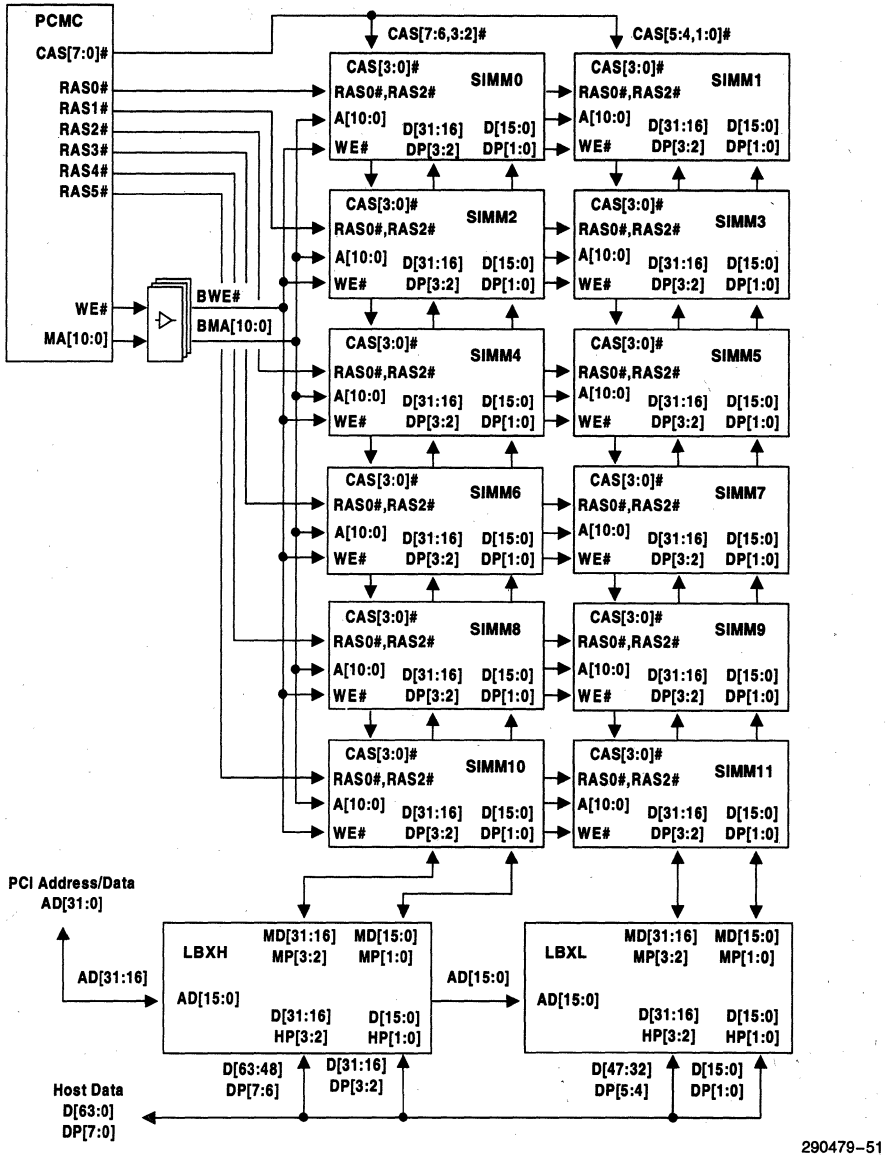
6.1.2 DRAM ADDRESS TRANSLATION

The 82434LX multiplexed row/column address to the DRAM memory array is provided by the MA[10:0] signals. The MA[10:0] bits are derived from the host address bus as defined by Table 12.

MA[10:0] are translated from the host address A[24:3] for all memory accesses, except those targeted to memory that has been remapped as a result of the creation of a memory space gap in the lower extended memory area. In the case of a cycle targeting remapped memory, the least significant bits come directly from the host address, while the more significant bits depend on the memory space gap start address, gap size, and the size of main memory.

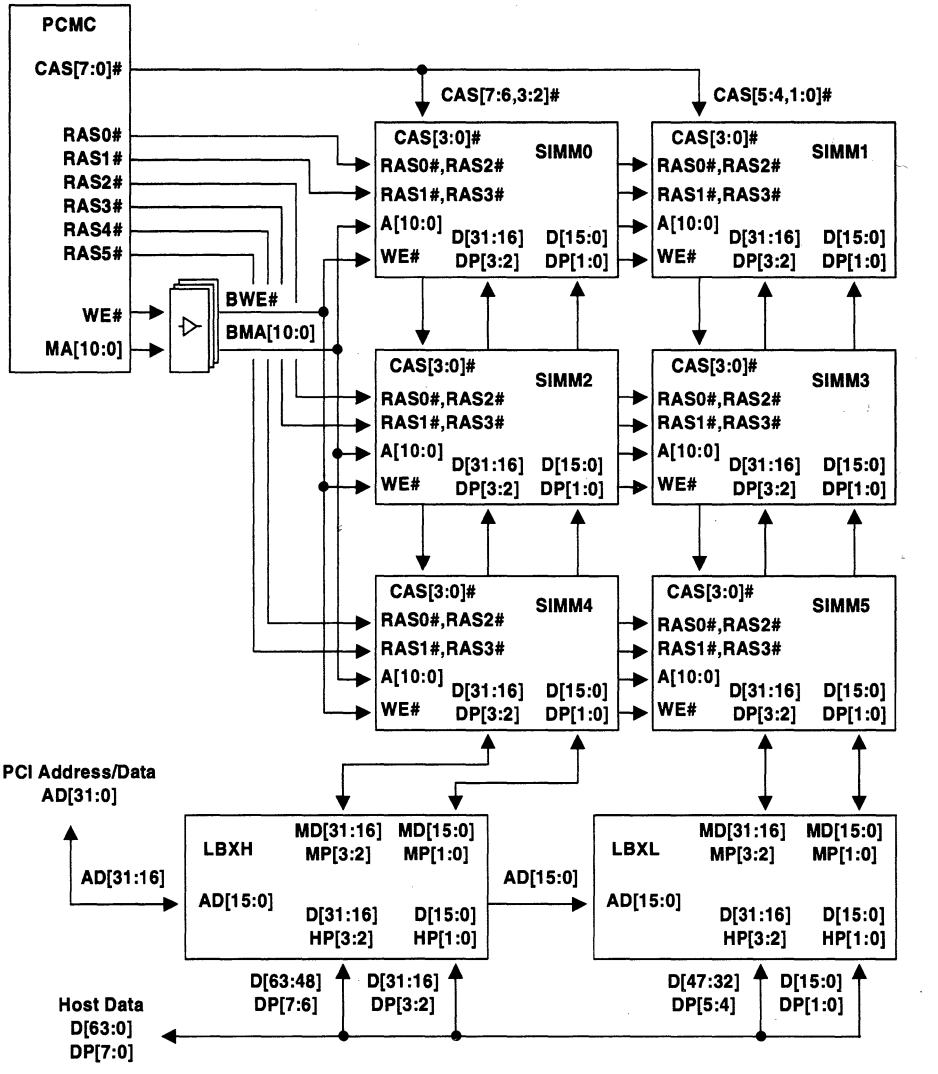
Table 12. DRAM Address Translation

Memory Address, MA[10:0]	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Row Address	A24	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column Address	A23	A21	A11	A10	A9	A8	A7	A6	A5	A4	A3



NOTE:
The figure shows the connections for the 82434LX. For the 82434NX, there are two additional RAS lines (RAS[7:6]#) and one additional address line (MA11).

Figure 42. 82434LX DRAM Configuration Supporting Single-Sided SIMMs



NOTE:
The figure shows the connections for the 82434LX. For the 82434NX, there are two additional RAS lines (RAS[7:6]#) and one additional address line (MA11).

Figure 43. 82434LX DRAM Configuration Supporting Single- or Double-Sided SIMMs

6.1.3 CYCLE TIMING SUMMARY

The 82434LX PCMC DRAM performance is summarized in Table 13 for all CPU read and write cycles.

Table 13. CPU to DRAM Performance Summary

Cycle Type	Burst, x-4-4-4 Timing	Single, x-4-4-4 Timing
Read Page Hit	7-4-4-4	7
Read Row Miss	11-4-4-4	11
Read Page Miss	14-4-4-4	14
Posted Write, WT L2	3-1-1-1	3
Posted Write, WB L2	4-1-1-1	4
Write Page Hit	12-4-4-4	12
Write Row Miss	13-4-4-4	13
Write Page Miss	16-4-4-4	16
0-Active RAS# Mode Read	10-4-4-4	10
0-Active RAS# Mode Write	12-4-4-4	12

CPU writes to the CPU-to-Memory Posted Write Buffer are completed at 3-1-1-1 when the second level cache is configured for write-through mode and 4-1-1-1 when the cache is configured for write-back mode. Table 14 shows the refresh performance in CPU clocks.

Table 14. Refresh Cycle Performance

Refresh Type	Hidden Refresh	RAS# only Refresh	CAS# before RAS#
Single	12	13	14
Burst of Four	48	52	56

6.1.4 CPU TO DRAM BUS CYCLES

This section describes the CPU-to-DRAM cycles for the 82434LX.

6.1.4.1 Read Page Hit

Figure 44 depicts a CPU burst read page hit from DRAM. The 82434LX PCMC decodes the CPU address as a page hit and drives the column address onto the MA[10:0] lines. CAS[7:0]# are then asserted to cause the DRAMs to latch the column address and begin the read cycle. CMR (CPU Memory Read) is driven on the HIG[4:0] lines to enable the memory data to host data path through the LBXs. The PCMC advances the MA[1:0] lines through the Pentium processor burst order, negating and asserting CAS[7:0]# to read each Qword. The host data is latched on the falling edge of MDLE, when CAS[7:0]# are negated. The latch is opened again when MDLE is sampled asserted by the LBXs. The LBXs tri-state the host data bus when HIG[4:0] change to NOPC and MDLE rises. A single read page hit from DRAM is similar to the first read of this sequence. The HIG[4:0] lines are driven to NOPC when BRDY# is asserted.

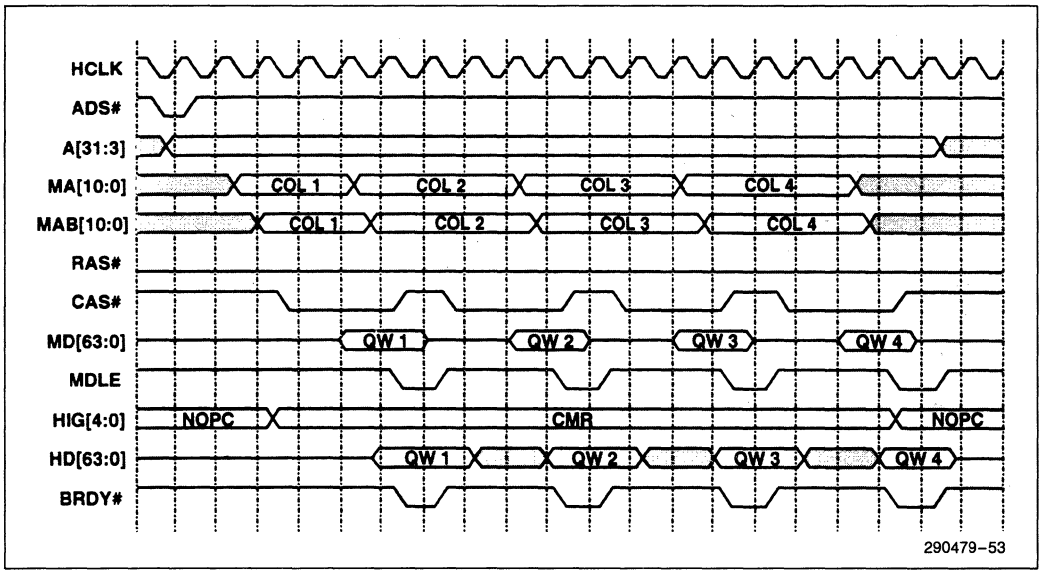


Figure 44. Burst DRAM Read Cycle-Page Hit

6.1.4.2 Read Page Miss

Figure 45 depicts a CPU burst read page miss from DRAM. The 82434LX decodes the CPU address as a page miss and switches from initially driving the column address to driving the row address on the MA[10:0] lines. RAS# is then negated to precharge the DRAMs and then asserted to cause the DRAMs to latch the new row address. The PCMC then switches the MA[10:0] lines to drive the column address and asserts CAS[7:0]#. CMR (CPU Memory Read) is driven on the HIG[4:0] lines to enable the memory data to host data path through the LBXs. The PCMC advances the MA[1:0] lines through the Pentium processor burst order, negating and asserting CAS[7:0]# to read each Qword. The host data is latched on the falling edge of MDLE, when CAS[7:0]# are negated. The latch is opened again when MDLE is sampled asserted by the LBXs. The LBXs tri-state the host data bus when HIG[4:0] change to NOPC and MDLE rises. A single read page miss from DRAM is similar to the first read of this sequence. The HIG[4:0] lines are driven to NOPC when BRDY# is asserted.

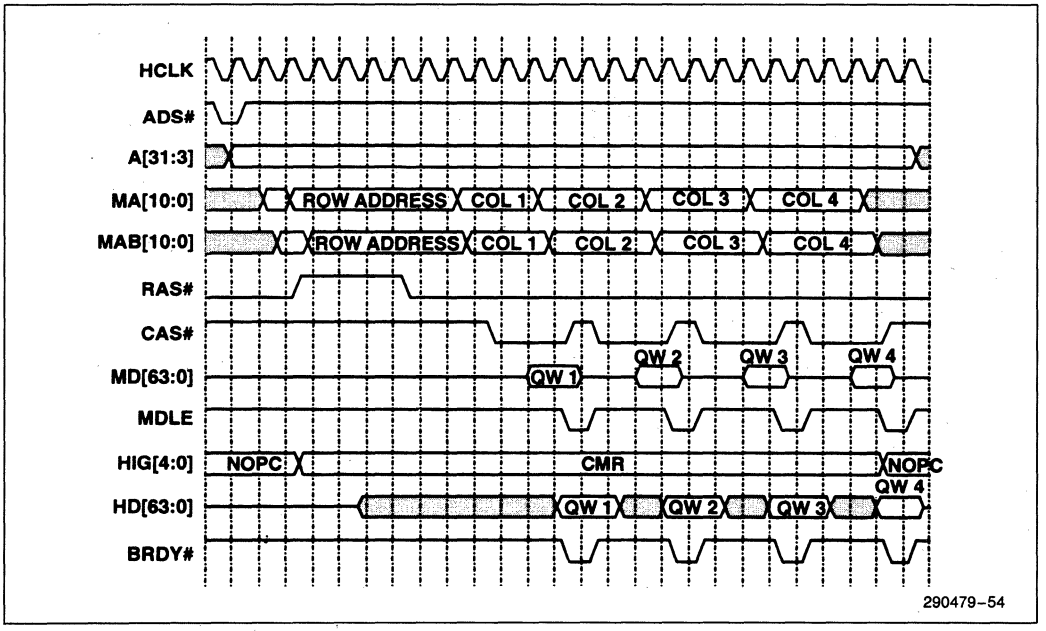


Figure 45. DRAM Read Cycle-Page Miss

6.1.4.3 Read Row Miss

Figure 46 depicts a CPU burst read row miss from DRAM. The 82434LX decodes the CPU address as a row miss and switches from initially driving the column address to driving the row address on the MA[10:0] lines. The RAS# signal that was asserted is negated and the RAS# for the currently accessed row is asserted. The PCMC then switches the MA[10:0] lines to drive the column address and asserts CAS[7:0]#. CMR (CPU Memory Read) is driven on the HIG[4:0] lines to enable the memory data to host data path through the LBXs. The PCMC advances the MA[1:0] lines through the Pentium processor burst order, negating and asserting CAS[7:0]# to read each Qword. The host data is latched on the falling edge of MDLE, when CAS[7:0]# are negated. The latch is opened again when MDLE is sampled asserted by the LBXs. The LBXs tri-state the host data bus when HIG[4:0] change to NOPC and MDLE rises. A single read row miss from DRAM is similar to the first read of this sequence. The HIG[4:0] lines are driven to NOPC when BRDY# is asserted.

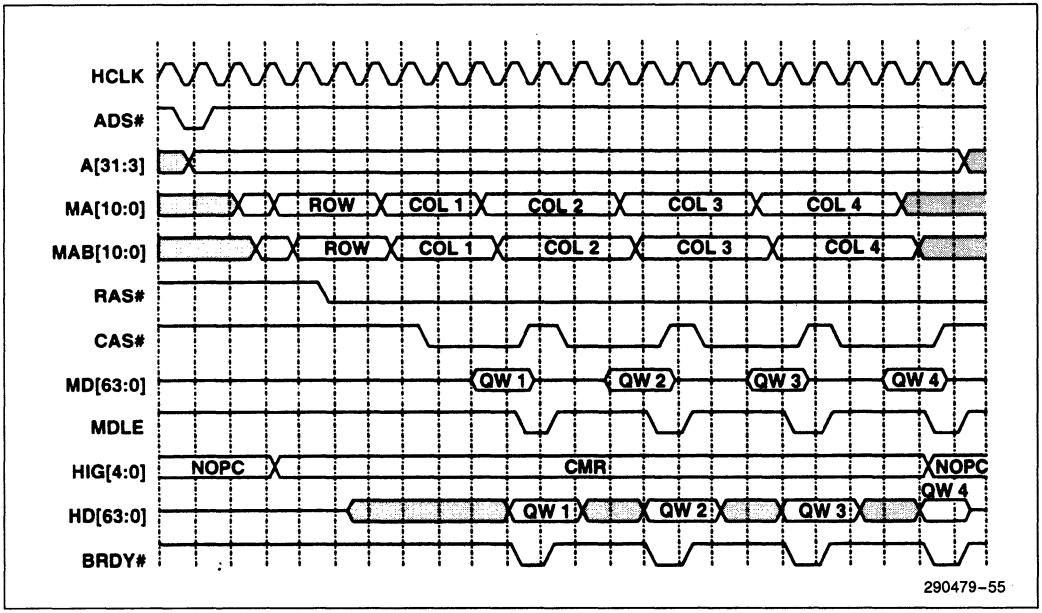


Figure 46. Burst DRAM Read Cycle-Row Miss

6.1.4.4 Write Page Hit

Figure 47 depicts a CPU burst write page hit from DRAM. The 82434LX decodes the CPU write cycle as a DRAM page hit. The HIG[4:0] lines are driven to PCMWQ to post the write to the LBXs. In the figure, the write cycle is posted to the CPU-to-Memory Posted Write Buffer at 4-1-1-1. The write is posted at 4-1-1-1 when the second level cache is configured for a write-back policy. The write is posted to DRAM at 3-1-1-1 when the second level cache is configured for a write-through policy. When the cycle is decoded as a page hit, the PCMC asserts WE# and drives the RCMWQ command on MIG[2:0] to enable the LBXs to drive the first Qword of the write onto the memory data lines. MEMDRV is then driven to cause the LBXs to continue to drive the first Qword for three more clocks. CAS[7:0]# are then negated and asserted to perform the writes to the DRAMs as the MA[1:0] lines advance through the Pentium processor burst order. A single write is similar to the first write of the burst sequence. MIG[2:0] are driven to NOPM in the clock after CAS[7:0]# are asserted.

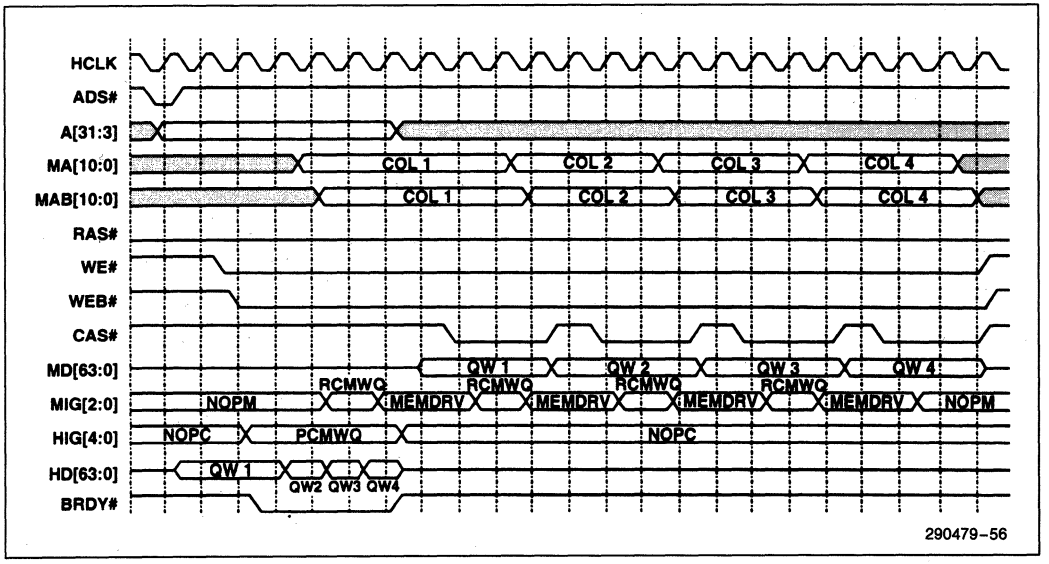


Figure 47. Burst DRAM Write Cycle-Page Hit

6.1.4.5 Write Page Miss

Figure 48 depicts a CPU burst write page miss to DRAM. The 82434LX decodes the CPU write cycle as a DRAM page miss. The HIG[4:0] lines are driven to PCMWQ to post the write to the LBXs. In the figure, the write cycle is posted to the CPU-to-Memory Posted Write Buffer at 4-1-1-1. The write is posted at 4-1-1-1 when the second level cache is configured for a write-back policy. The write is posted to DRAM at 3-1-1-1 when the second level cache is configured for a write-through policy. When the cycle is decoded as a page miss, the PCMC switches the MA[10:0] lines from the column address to the row address and asserts WE#. The PCMC drives the RCMWQ command on MIG[2:0] to enable the LBXs to drive the first Qword of the write onto the memory data lines. MEMDRV is then driven to cause the LBXs to continue to drive the first Qword. The RAS# signal for the currently decoded row is negated to precharge the DRAMs. RAS# is then asserted to cause the DRAMs to latch the row address. The PCMC then switches the MA[10:0] lines to the column address and asserts CAS[7:0]# to initiate the first write. CAS[7:0]# are then negated and asserted to perform the writes to the DRAMs as the MA[1:0] lines advance through the Pentium processor burst order. A single write is similar to the first write of the burst sequence. MIG[2:0] are driven to NOPM in the clock after CAS[7:0]# are asserted.

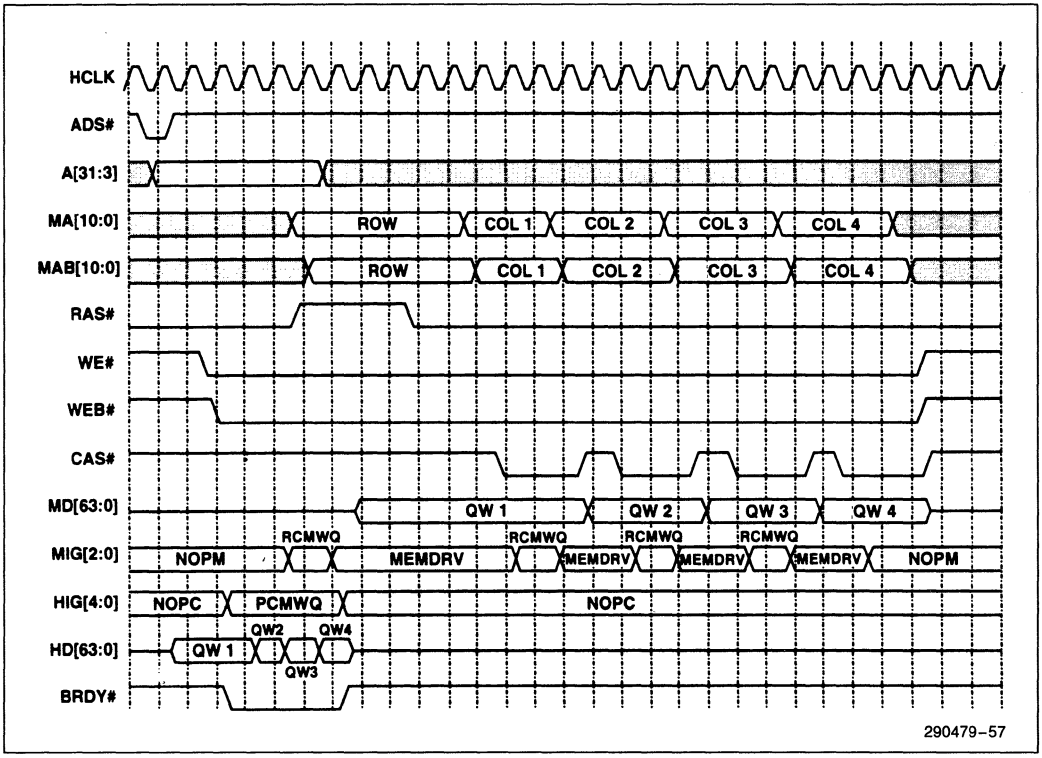


Figure 48. Burst DRAM Write Cycle-Page Miss

6.1.4.6 Write Row Miss

Figure 49 depicts a CPU burst write row miss to DRAM. The 82434LX decodes the CPU write cycle as a DRAM row miss. The HIG[4:0] lines are driven to PCMWQ to post the write to the LBXs. In the figure, the write cycle is posted to the CPU-to-Memory Posted Write Buffer at 4-1-1-1. The write is posted at 4-1-1-1 when the second level cache is configured for a write-back policy. The write is posted to DRAM at 3-1-1-1 when the second level cache is configured for a write-through policy. When the cycle is decoded as a row miss, the PCMC negates the already active RAS# signal, switches the MA[10:0] lines from the column address to the row address and asserts the RAS# signal for the currently decoded row. The PCMC asserts WE# and drives the RCMWQ command on MIG[2:0] to enable the LBXs to drive the first Qword of the write onto the memory data lines. MEMDRV is then driven to cause the LBXs to continue to drive the first Qword. The PCMC then switches the MA[10:0] lines to the column address and asserts CAS[7:0]# to initiate the first write. CAS[7:0]# are then negated and asserted to perform the writes to the DRAMs as the MA[1:0] lines advance through the Pentium processor burst order. A single write is similar to the first write of the burst sequence. MIG[2:0] are driven to NOPM in the clock after CAS[7:0]# are asserted.

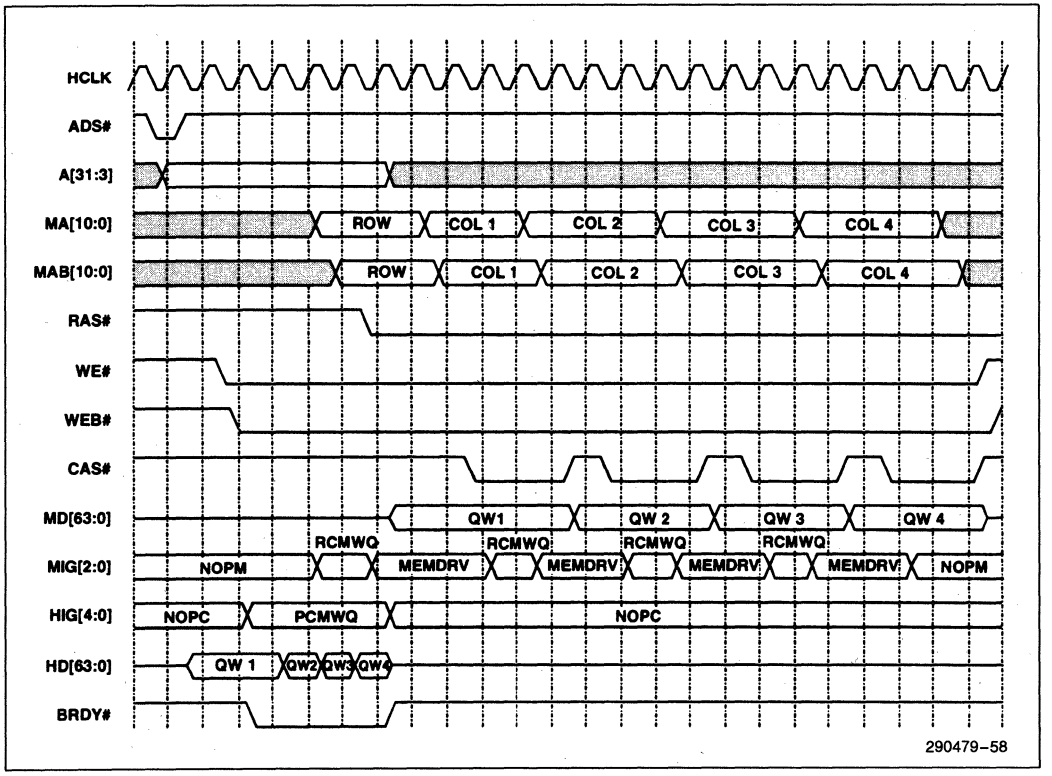


Figure 49. Burst DRAM Write Cycle-Row Miss

6.1.4.7 Read Cycle, 0-Active RAS# Mode

When in 0-active RAS# mode, every CPU cycle to DRAM results in a RAS# and CAS# sequence. RAS# is always negated after a cycle completes. Figure 50 depicts a CPU burst read cycle from DRAM where the 82434LX is configured for 0-active RAS# mode. When in 0-active RAS# mode, the PCMC defaults to driving the row address on the MA[10:0] lines. The PCMC asserts the RAS# signal for the currently decoded row causing the DRAMs to latch the row address. The PCMC then switches the MA[10:0] lines to drive the column address and asserts CAS[7:0]#. CMR (CPU Memory Read) is driven on the HIG[4:0] lines to enable the memory data to host data path through the LBXs. The PCMC advances the MA[1:0] lines through the Pentium processor burst order, negating and asserting CAS[7:0]# to read each Qword. The host data is latched on the falling edge of MDLE, when CAS[7:0]# are negated. The latch is opened again when MDLE is sampled asserted by the LBXs. The LBXs tri-state the host data bus when HIG[4:0] change to NOPC and MDLE rises. A single read row miss from DRAM is similar to the first read of this sequence. The HIG[4:0] lines are driven to NOPC when BRDY# is asserted. RAS# is negated with CAS[7:0]#.

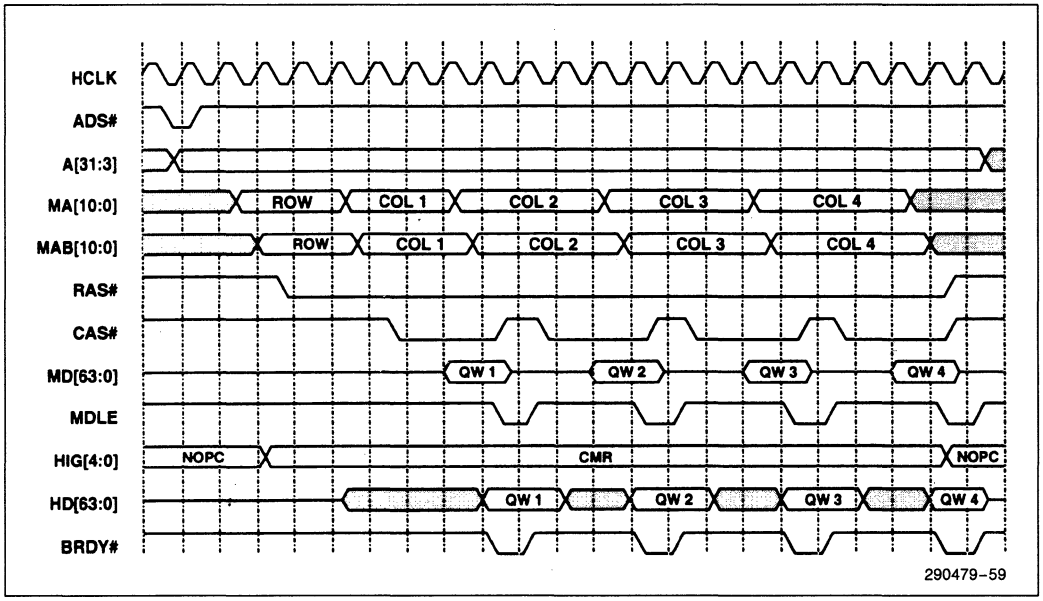


Figure 50. Burst DRAM Read Cycle, 0-Active RAS# Mode

6.1.4.8 Write Cycle, 0-Active RAS# Mode

When in 0-active RAS# mode, every CPU cycle to DRAM results in a RAS# and CAS# sequence. RAS# is always negated after a cycle completes. Figure 51 depicts a CPU Burst Write Cycle to DRAM where the 82434LX is configured for 0-active RAS# mode. The HIG[4:0] lines are driven to PCMWQ to post the write to the LBXs. In the figure, the write cycle is posted to the CPU-to-Memory Posted Write Buffer at 4-1-1-1. The write is posted at 4-1-1-1 when the second level cache is configured for a write-back policy. The write is posted to DRAM at 3-1-1-1 when the second level cache is configured for a write-through policy. When in 0-active RAS# mode, the PCMC defaults to driving the row address on the MA[10:0] lines. The PCMC asserts the RAS# signal for the currently decoded row causing the DRAMs to latch the row address. The PCMC asserts WE# and drives the RCMWQ command on MIG[2:0] to enable the LBXs to drive the first Qword of the write onto the memory data lines. MEMDRV is then driven to cause the LBXs to continue to drive the first Qword. The PCMC then switches the MA[10:0] lines to the column address and asserts CAS[7:0]# to initiate the first write. CAS[7:0]# are then negated and asserted to perform the writes to the DRAMs as the MA[1:0] lines advance through the Pentium processor burst order. A single write is similar to the first write of the burst sequence. MIG[2:0] are driven to NOPM in the clock after CAS[7:0] are asserted.

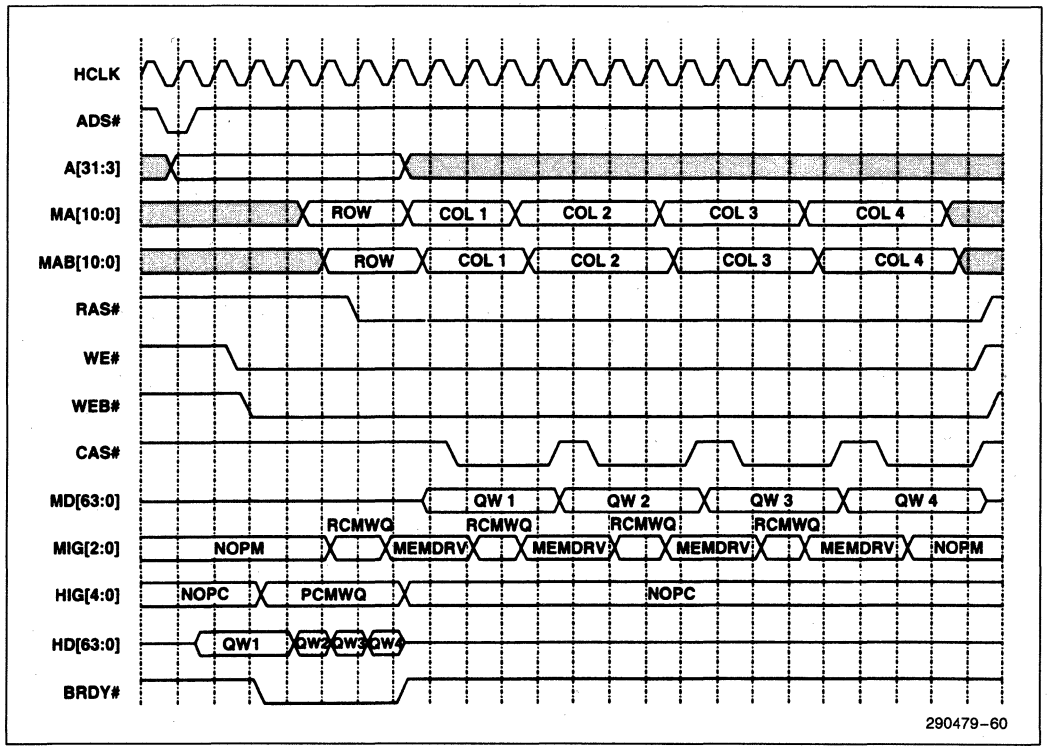


Figure 51. Burst DRAM Write Cycle, 0-Active RAS# Mode

6.1.5 REFRESH

The refresh of the DRAM array can be performed by either using RAS#-only or CAS#-before-RAS# refresh cycles. When programmed for CAS#-before-RAS# refresh, hidden refresh cycles are initiated when possible. RAS# only refresh can be used with any type of second level cache configuration (i.e., no second level cache is present, or either a burst SRAM or standard SRAM second level cache is implemented). CAS#-before-RAS# refresh can be enabled when either no second level cache is present or a burst SRAM second level cache is implemented. CAS#-before-RAS# refresh should not be used when a standard SRAM second level cache is implemented. The timing of internally generated refresh cycles is derived from HCLK and is independent of any expansion bus refresh cycles.

The DRAM controller contains an internal refresh timer which periodically requests the refresh control logic to perform either a single refresh or a burst of four refreshes. The single refresh interval is 15.6 μs. The interval for burst of four refreshes is four times the single refresh interval, or 62.4 μs. The PCMC is configured for either single or burst of four refresh and either RAS#-only or CAS#-before-RAS# refresh via the DRAM Control Register (offset 57h).

To minimize performance impact, refresh cycles are partially deferred until the DRAM interface is idle. The deferment of refresh cycles is limited by the DRAM maximum RAS# low time of 100 μs. Refresh cycles are initiated such that the RAS# maximum low time is never violated.

Hidden refresh cycles are run whenever all eight CAS# lines are active when the refresh cycle is internally requested. Normal CAS#-before-RAS# refresh cycles are run whenever the DRAM interface is idle when the refresh is requested, or when any subset of the CAS# lines is inactive as the refresh is internally requested.

To minimize the power surge associated with refreshing a large DRAM array the DRAM interface staggers the assertion of the RAS# signals during both CAS#-before-RAS# and RAS#-only refresh cycles. The order of RAS# edges is dependent on which RAS# was most recently asserted prior to the refresh sequence. The RAS# that was active will be the last to be activated during the refresh sequence. All RAS[5:0]# lines are negated at the end of refresh cycles, thus, the first DRAM cycle after a refresh sequence is a row miss.

6.1.5.1 RAS#-Only Refresh-Single

Figure 52 depicts a RAS#-only refresh cycle when the 82434LX is programmed for single refresh cycles. The diagram shows a CPU read cycle completing as the refresh timing inside the PCMC generates a refresh request. The refresh address is driven on the MA[10:0] lines. Since the CPU cycle was to row 0, RAS0# is negated. RAS1# is the first to be asserted. RAS2# through RAS5# are then asserted sequentially while RAS0# is driven high, precharging the DRAMs in row 0. RAS0# is then asserted after RAS5#. Each RAS# line is asserted for six host clocks.

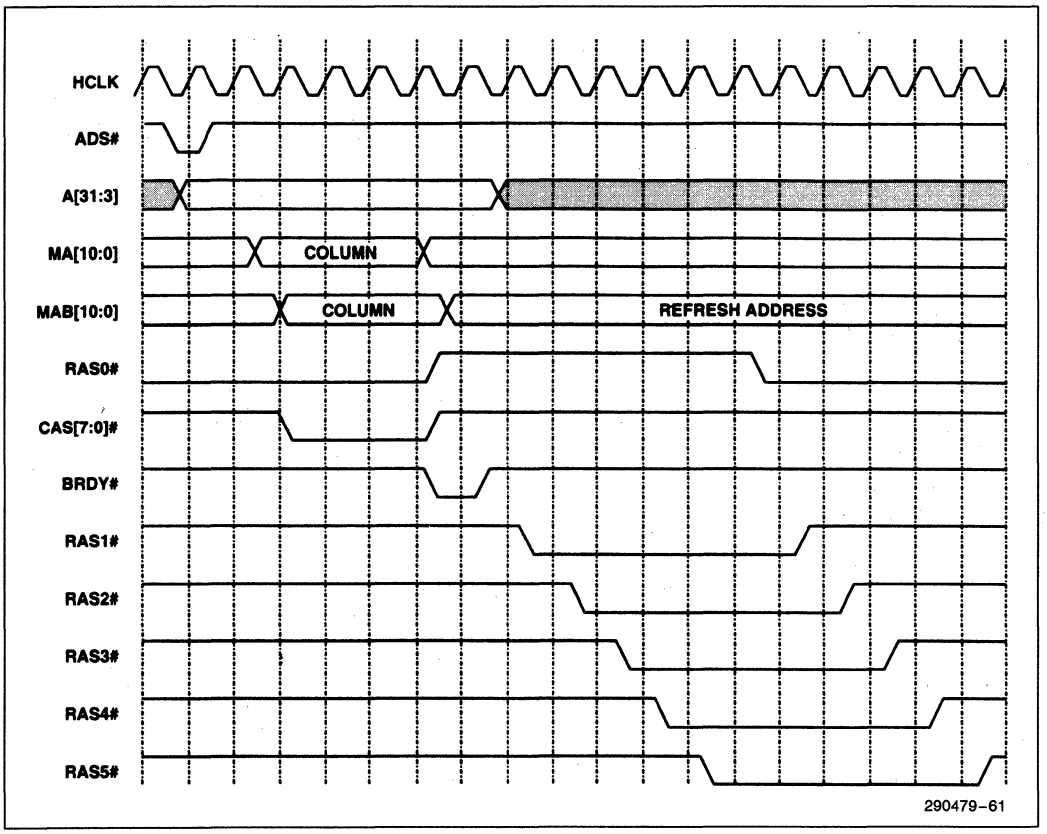


Figure 52. RAS# Only Refresh-Single

6.1.5.2 CAS#-before-RAS# Refresh-Single

Figure 53 depicts a CAS#-before-RAS# refresh cycle when the 82434LX is programmed for single refresh cycles. The diagram shows a CPU read cycle completing as the refresh timing inside the PCMC generates a refresh request. The CPU read cycle is less than a Qword, therefore a hidden refresh is not initiated. After the CPU read cycle completes, all of the RAS# and CAS# lines are negated. The PCMC then asserts CAS[7:0]# and then sequentially asserts the RAS# lines, starting with RAS1# since RAS0# was the last RAS# line asserted. Each RAS# line is asserted for six clocks.

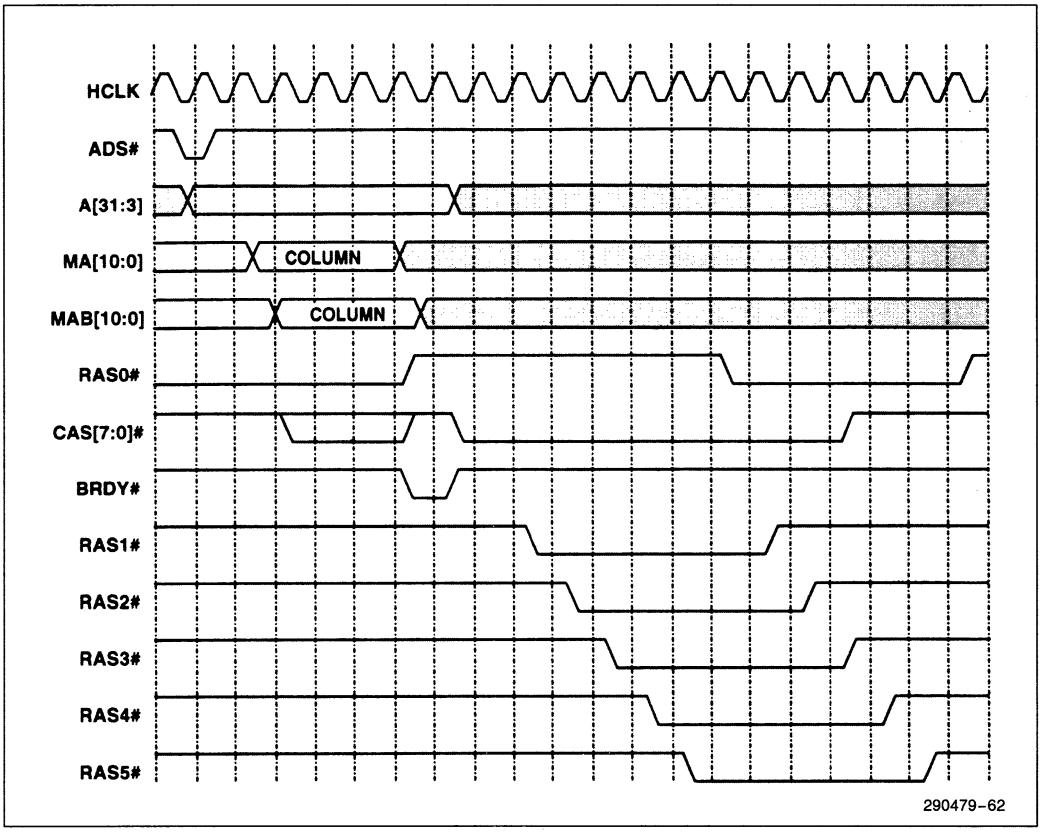


Figure 53. CAS#-before-RAS# Refresh-Single

6.1.5.3 Hidden Refresh-Single

Figure 54 depicts a hidden refresh cycle which takes place after a DRAM read page hit cycle. The diagram shows a CPU read cycle completing as the refresh timing inside the 82434LX generates a refresh request. The CPU read cycle is an entire Qword, therefore a hidden refresh is initiated. After the CPU read cycle completes, RAS# is negated, but all eight CAS# lines remain asserted. The PCMC then sequentially asserts the RAS# lines, starting with RAS1# since RAS0# was the last active RAS# line. Each RAS# line is asserted for six clocks.

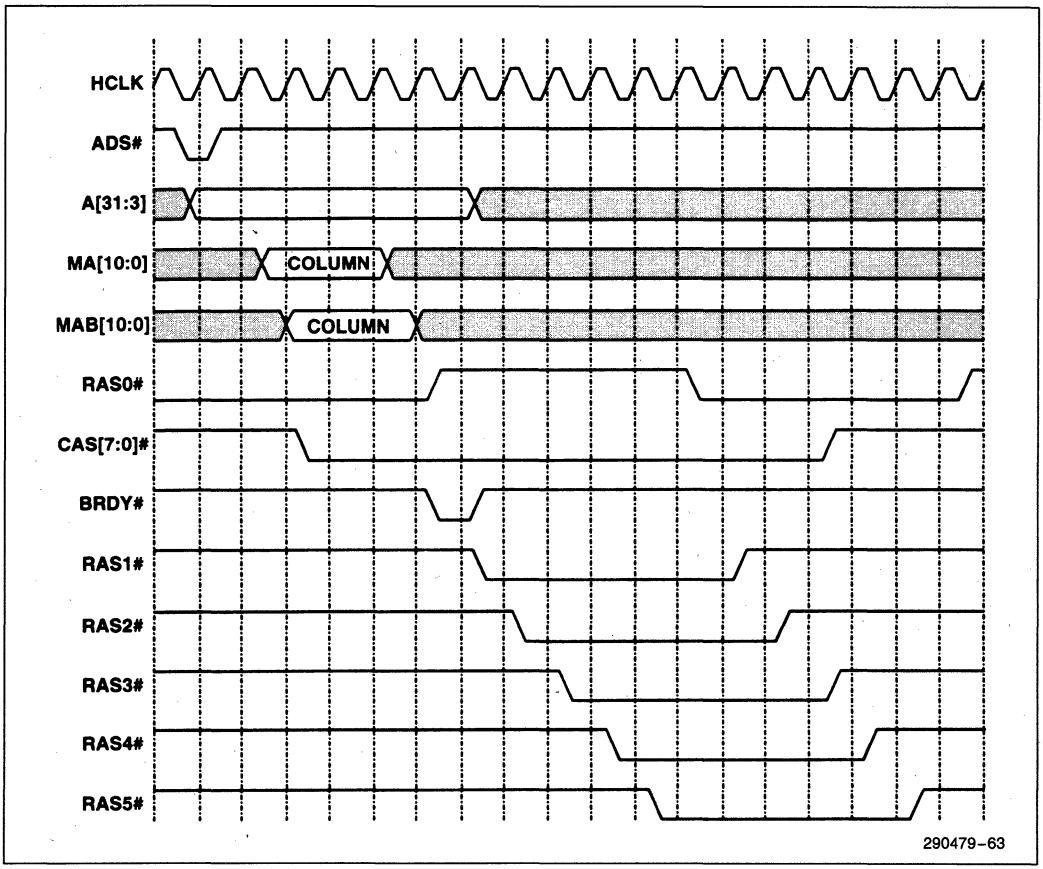


Figure 54. Hidden Refresh-Single

6.2 82434NX DRAM Interface

This section describes the 82434NX DRAM interface. Changes in the 82430NX PCIset from the 82430 PCIset include:

1. Increased maximum DRAM memory size to 512 MBytes. The 82430NX PCIset increases the maximum memory array size from 192 MBytes to 512 MBytes.
2. Two additional row address lines (RAS[7:6]#) for a total of eight (RAS[7:0]#).
3. Addition of 50 MHz host-bus optimized DRAM timing sets.
4. Three additional registers are added to support the increased memory sizeDRAM Row Boundary Registers 6 and 7 (DRB[7:6]) and the DRAM Row Boundary Extension (DRBE) Register.
5. Modified MA[11:0] timing to provide more MA[11:0] setup time to CAS[7:0]# assertion.

6.2.1 DRAM ADDRESS TRANSLATION

The MA[11:0] lines are translated from the host address lines A[26:3] for all memory accesses, except those targeted to memory that has been remapped as a result of the creation of a memory space gap in the lower extended memory area. In the case of a cycle targeting remapped memory, the least significant bits come directly from the host address, while the more significant bits depend on the memory space gap start address, gap size, and the size of main memory.

Table 15. DRAM Address Translation

Memory Address MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Column Address	A25	A23	A21	A11	A10	A9	A8	A7	A6	A5	A4	A3
Row Address	A26	A24	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12

6.2.2 CYCLE TIMING SUMMARY

The 82434NX PCMC DRAM performance for 50 MHz Host bus clock is summarized in Table 13 for all CPU read and write cycles. The 60/66 MHz MA[11:0] timings when in X-4-4-4 mode have one difference from the 82434LX MA[11:0] timings. The MA lines switch to the next address in the burst sequence one clock sooner than in the 82434LX, providing more MA[11:0] setup time to CAS[7:0]# assertion. The 60/66 MHz DRAM timings for write cycles have been improved by 1 clock for all leadoffs. The 50 MHz timings shown below are selected by HOF = 00, DBT = 11, RWS = 0 and CWS = 0.

Table 16. CPU to DRAM Performance Summary for 50 MHz Host Bus Clock

Cycle Type	x-3-3-3 Timing(1)
Read (Page Hit/Row Miss/ Page Miss)	6/10/12-3-3-3
Posted Write	4-1-1-1
Write (Page Hit/Row Miss/ Page Miss)	10/11/13-3-3-3
0-Active RAS# Mode Reads	9-3-3-3
0-Active RAS# Mode Writes	9-3-3-3

NOTES:
1. Single cycle timings are identical to these leadoff timings.

Table 17. Refresh Cycle Performance (Independent of CPU frequency)

Refresh Type	Hidden Refresh	RAS# Only Refresh	CAS#-Before-RAS#
Single	16	17	18
Burst of Four	64	68	72

6.2.3 CPU TO DRAM BUS CYCLES

In this section, all timing diagrams are for 50 MHz DRAM timing, 1-Active RAS mode. The 60/66 MHz MA[11:0] timings when in X-4-4-4 mode have one difference from the 82434LX MA[11:0] timings. The MA lines switch to the next address in the burst sequence one clock sooner than in the 82434LX. The write cycle leadoffs are 1 clock earlier for 82430NX than 82430 (the MIGs and CAS timings improved by 1 clock). The 0-Active RAS# modes closely resemble the row miss cases. In 0-Active RAS# mode, RAS# is asserted one clock sooner than is shown in the row miss timing diagrams.

6.2.3.1 Burst DRAM Read Page Hit

Figure 55 depicts a CPU burst read page hit to DRAM. The 82434NX decodes the CPU address as a page hit and drives the column address onto the MA[11:0] lines. CAS[7:0]# are then asserted for two CLKs and negated for one CLK. CMR (CPU Memory Read) is driven on the HIG[4:0] lines to enable the memory data to host data path through the LBXs. The PCMC advances the MA[1:0] lines through the processor burst order, negating and asserting CAS[7:0]# to read each Qword. The MD[63:0] data is sampled with HCLK in the LBXs when MDLE is asserted, and driven on the host bus the following cycle to meet the setup time of the CPU. BRDY# is then asserted. When MDLE is negated, the LBX continues to drive the latched HD[63:0] to ensure that the data hold time to CWE[7:0]# is met for standard SRAMs. The LBXs tri-state the host data bus when HIG[4:0] change to NOPC and MDLE rises. A single read page hit from DRAM is similar to the first read of this sequence. The HIG[4:0] lines are driven to NOPC when the last BRDY# is asserted.

The diagram also shows the typical control signal timing for a burst SRAM line fill operation. Note that CCS# inactive will mask any new ADS# (caused by the NA# assertion) to the burst SRAMs.

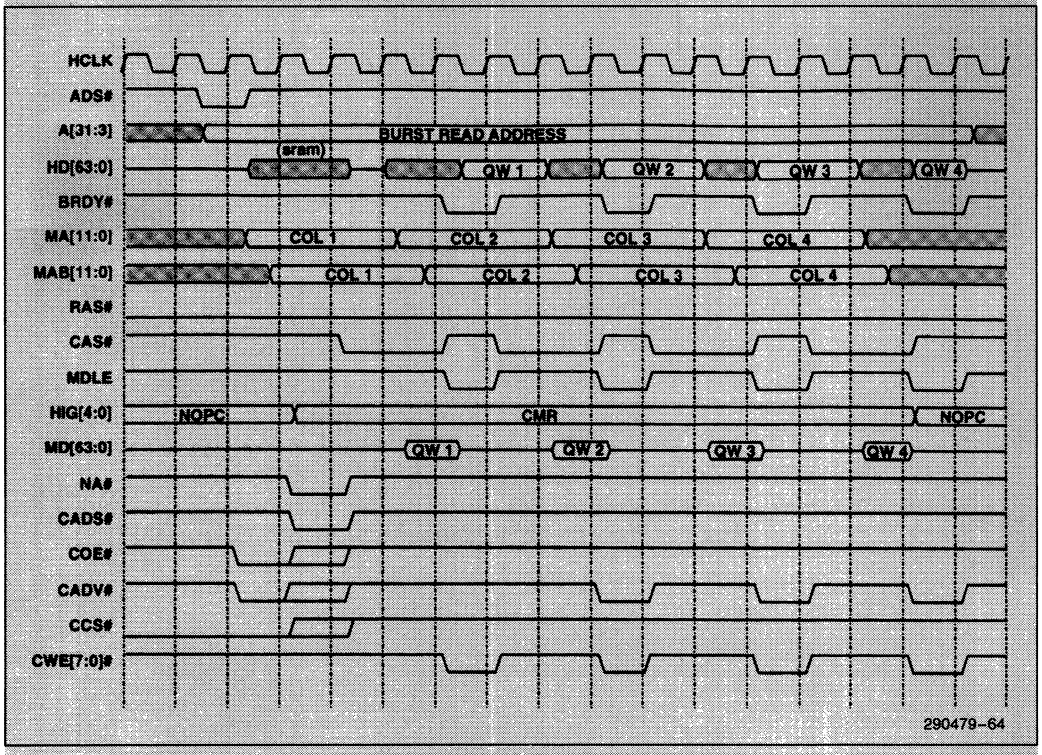


Figure 55. Burst DRAM Read Cycle-Page Hit

6.2.3.2 Burst DRAM Read Page Miss

Figure 56 depicts a CPU to DRAM burst read page miss cycle. The 82434NX decodes the CPU address as a page miss and switches from initially driving the column address to driving the row address on the MA[11:0] lines. RAS# is then negated to precharge the DRAMs and then asserted to latch the new DRAM row address. The PCMC then switches the MA[11:0] lines to drive the column address and asserts CAS[7:0]#. CMR (CPU Memory Read) is driven on the HIG[4:0] lines to enable the memory data to host data path through the LBXs. The PCMC advances the MA[1:0] lines through the microprocessor burst order, negating and asserting CAS[7:0]# to read each Qword. The MD[63:0] data is sampled with HCLK in the LBXs when MDLE is asserted, and driven on the host bus the following cycle to meet the setup time of the CPU. BRDY# is then asserted. When MDLE is negated, the LBX continues to drive the latched HD[63:0] to ensure that the data hold time to CWE[7:0]# is met for standard SRAMs. The LBXs tri-state the host data bus when HIG[4:0] change to NOPC and MDLE rises. The HIG[4:0] lines are driven to NOPC when the last BRDY# is asserted.

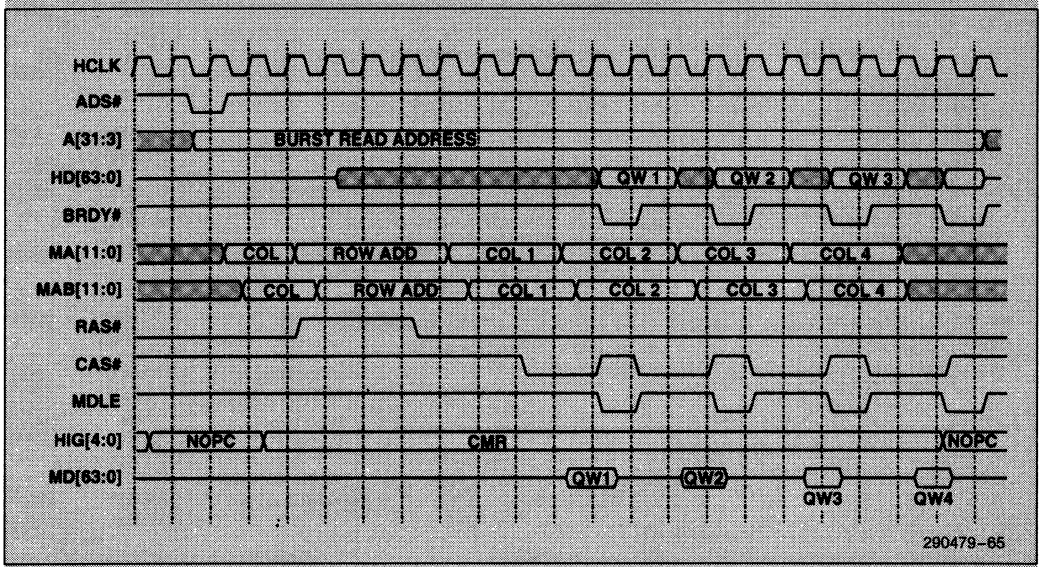


Figure 56. Burst DRAM Read Cycle-Page Miss

6.2.3.3 Burst DRAM Read Row Miss

Figure 57 depicts a CPU to DRAM burst read row miss cycle. The 82434NX decodes the CPU address as a row miss and switches from initially driving the column address to driving the row address on the MA[11:0] lines. The RAS# signal that was asserted is negated and the RAS# for the currently accessed row is asserted (RAS# is asserted 1 clock earlier in 0-Active RAS# Mode.) The PCMC then switches the MA[11:0] lines to drive the column address and asserts CAS[7:0]#. CMR (CPU Memory Read) is driven on the HIG[4:0] lines to enable the memory data to host data path through the LBXs. The PCMC advances the MA[1:0] lines through the microprocessor burst order, negating and asserting CAS[7:0]# to read each Qword. The MD[63:0] data is sampled with HCLK in the LBXs when MDLE is asserted, and driven on the host bus the following cycle to meet the setup time of the CPU. BRDY# is then asserted. When MDLE is negated, the LBX continues to drive the latched HD[63:0] to ensure that the data hold time to CWE[7:0]# is met for standard SRAMs. The LBXs tri-state the host data bus when HIG[4:0] change to NOPC and MDLE rises. A single read row miss from DRAM is similar to the first read of this sequence. The HIG[4:0] lines are driven to NOPC when the last BRDY# is asserted.

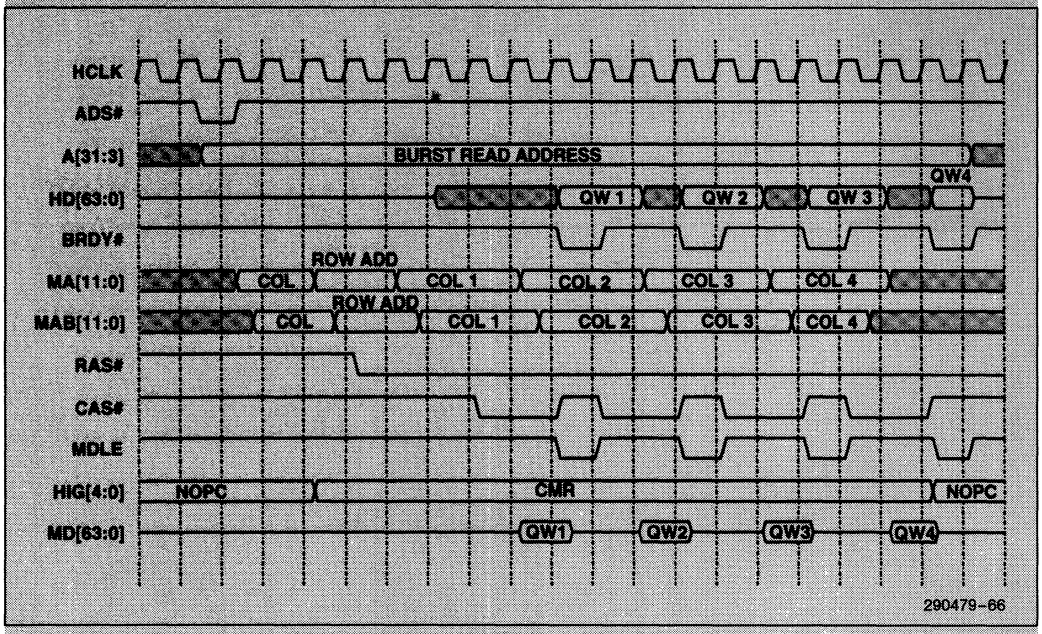


Figure 57. Burst DRAM Read Cycle-Row Miss

6.2.3.4 Burst DRAM Write Page Hit

Figure 58 depicts a CPU burst write page hit to DRAM. The 82434NX decodes the CPU write cycle as a DRAM page hit. The HIG[4:0] lines are driven to PCMWQ to post the write to the LBXs. In the figure, the write cycle is posted to the CPU-to-Memory Posted Write Buffer at 3-1-1-1. When the cycle is decoded as a page hit, the PCMC asserts WE# and drives the RCMWQ command on MIG[2:0] to enable the LBXs to drive the first Qword of the write onto the memory data lines. MEMDRV is then driven to cause the LBXs to continue to drive the first Qword for two more clocks. CAS[7:0]# are then negated and asserted to perform the writes to the DRAMs as the MA[1:0] lines advance through the Pentium processor burst order. A single write is similar to the first write of the burst sequence. The MIG[2:0] lines are driven to NOPM in the clock when the last CAS[7:0]# are asserted.

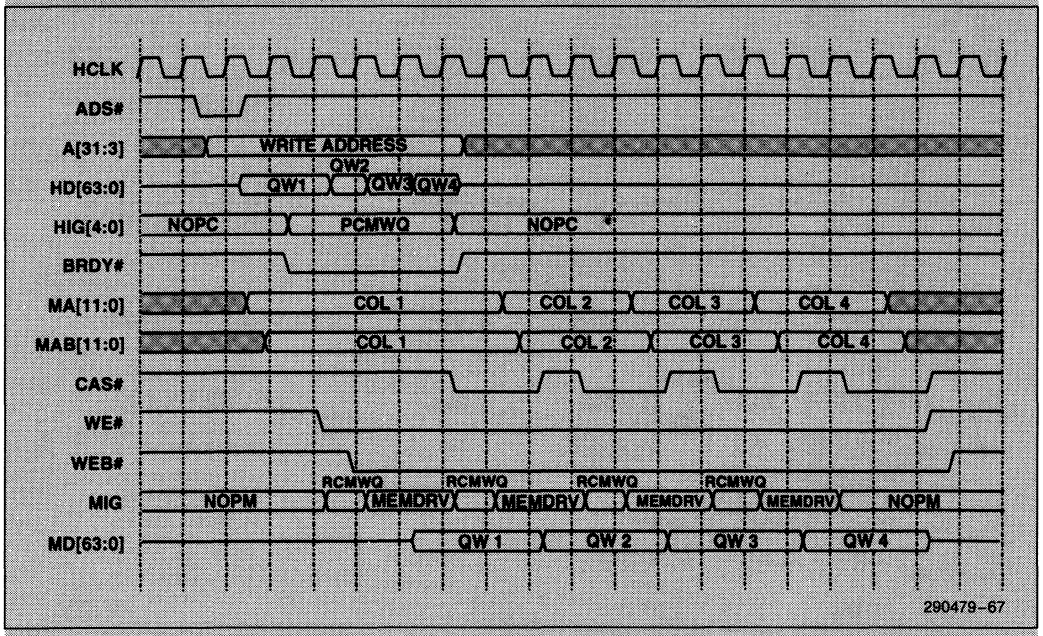


Figure 58. Burst DRAM Write Page Miss

6.2.3.5 Burst DRAM Write Page Miss

Figure 59 depicts a CPU burst write page miss to DRAM. The 82434NX decodes the CPU write cycle as a DRAM page miss and drives the PCMWQ command [HIG[4:0] lines] to post the write data to the LBXs. In the figure, the write cycle is posted to the CPU-to-Memory Posted Write Buffer at 3-1-1-1. When the cycle is decoded as a page miss, the PCMC switches the MA[11:0] lines from the column address to the row address and asserts WE# in clock 4. The PCMC drives the RCMWQ command on MIG[2:0] to enable the LBXs to drive the first Qword of the write onto the memory data lines. MEMDRV is then driven to cause the LBXs to continue to drive the first Qword. The RAS# signal for the currently decoded row is negated to precharge the DRAMs. RAS# is then asserted to cause the DRAMs to latch the row address. The PCMC then switches the MA[11:0] lines to the column address and asserts CAS[7:0]# to initiate the first write. CAS[7:0]# are then negated and asserted to perform the writes to the DRAMs as the MA[1:0] lines advance through the Pentium processor burst order. A single write is similar to the first write of the burst sequence. The MIG[2:0] lines are driven to NOPM in the clock when the last CAS[7:0]# are asserted.

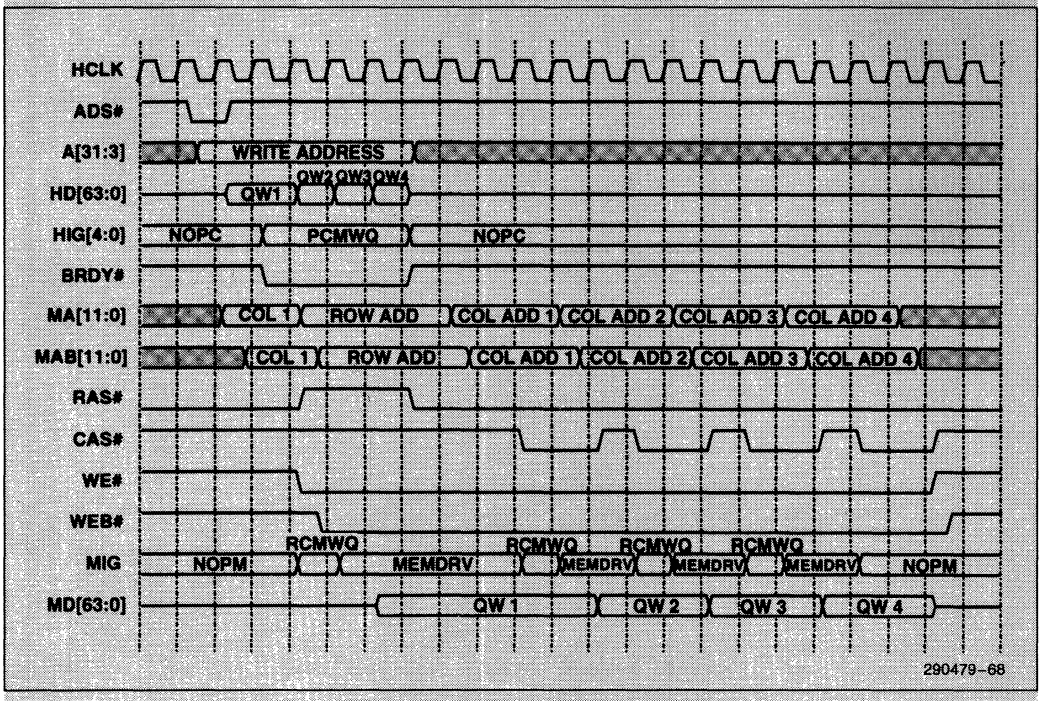


Figure 59. Burst DRAM Write Cycle-Page Miss

6.2.3.6 Burst DRAM Write Row Miss

Figure 60 depicts a CPU burst write row miss to DRAM. The 82434NX decodes the CPU write cycle as a DRAM row miss and the HIG[4:0] lines are driven to PCMWQ to post the write data into LBXs. When the cycle is decoded as a row miss, the PCMC negates the already active RAS# signal, switches the MA[11:0] lines from the column address to the row address and asserts the RAS# signal for the currently decoded row. The PCMC asserts WE# and drives the RCMWQ command on MIG[2:0] to enable the LBXs to drive the first Qword of the write onto the memory data lines. MEMDRV is then driven to cause the LBXs to continue to drive the first Qword. The PCMC then switches the MA[11:0] lines to the column address and asserts CAS[7:0]# to initiate the first write. CAS[7:0]# are then negated and asserted to perform the writes to the DRAMs as the MA[1:0] lines advance through the microprocessor burst order. A single write is similar to the first write of the burst sequence. The MIG[2:0] lines are driven to NOPM in the clock when the last CAS[7:0]# are asserted.

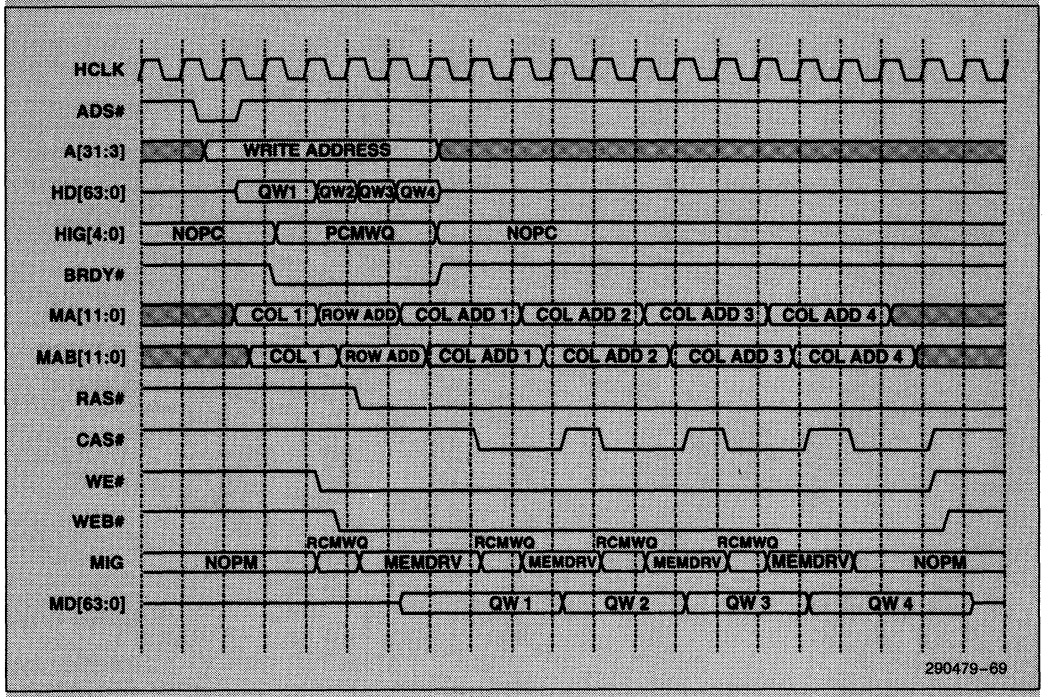


Figure 60. Burst DRAM Write Cycle-Row Miss

6.2.4 REFRESH

The refresh of the DRAM array can be performed by either using RAS#-only or CAS#-before-RAS# refresh cycles. When programmed for CAS#-before-RAS# refresh, hidden refresh cycles are initiated when possible. The timing of internally generated refresh cycles is derived from HCLK and is independent of any expansion bus refresh cycles.

The DRAM controller contains an internal refresh timer which periodically requests the refresh control logic to perform either a single refresh or a burst of four refreshes. The single refresh interval is 15.6 μs. The interval for burst of four refreshes is four times the single refresh interval, or 62.4 μs. The PCMC is configured for either single or burst of four refresh and either RAS#-only or CAS#-before RAS# refresh via the DRAM Control Register (offset 57h).

To minimize performance impact, refresh cycles are partially deferred until the DRAM interface is idle. Refresh cycles are initiated such that the RAS# maximum active time is never violated.

Hidden refresh cycles are run whenever all eight CAS# lines are active at the end of a read transaction when the refresh cycle is internally requested. Normal CAS#-before-RAS# refresh cycles are run whenever the DRAM interface is idle when the refresh is requested, or when any subset of the CAS# lines is inactive as the refresh is internally requested.

To minimize the power surge for refreshing a large DRAM array, the DRAM interface staggers the assertion and negation of the RAS# signals during both CAS#-before-RAS# and RAS#-only refresh cycles. The order of RAS# edges is dependent on which RAS# was most recently asserted prior to the refresh sequence. The RAS# that was active will be the last to be activated during the refresh sequence. All RAS[7:0]# lines are negated at the end of refresh cycles, making the first DRAM cycle after a refresh sequence a row miss.

6.2.4.1 RAS#-Only Refresh—Single

Figure 61 depicts a RAS#-only refresh cycle when the 82434NX is programmed for single refresh cycles. The diagram shows a cycle completing as the refresh timer inside the PCMC generates a refresh request. The refresh address is driven on the MA[11:0] lines. Since the cycle was to row 0, RAS0# is negated. RAS1# is the first to be asserted. RAS2# through RAS7# are then asserted sequentially while RAS0# is driven high, precharging the DRAMs in row 0. RAS0# is then asserted after RAS7#. Each RAS# line is asserted for eight host clocks.

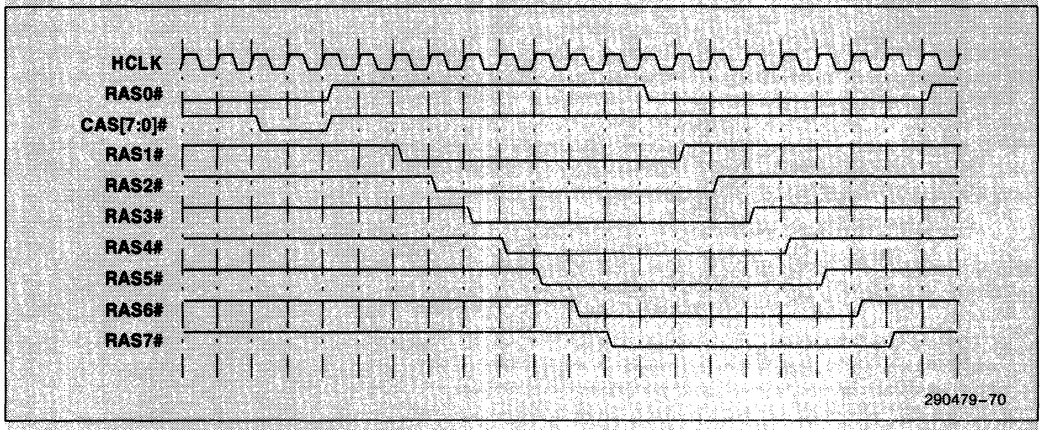


Figure 61. RAS#-Only Refresh—Single

6.2.4.2 CAS#-before-RAS# Refresh—Single

Figure 62 depicts a CAS#-before-RAS# refresh cycle when the 82434NX is programmed for single refresh cycles. The diagram shows a write cycle completing as the refresh timer inside the PCMC generates a refresh request. The cycle is less than a Qword, therefore a hidden refresh is not initiated. After the cycle completes, all of the RAS# and CAS# lines are negated. The PCMC then asserts CAS[7:0]# and then sequentially asserts the RAS# lines, starting with RAS1# since RAS0# was the last RAS# line asserted. Each RAS# line is asserted for eight clocks.

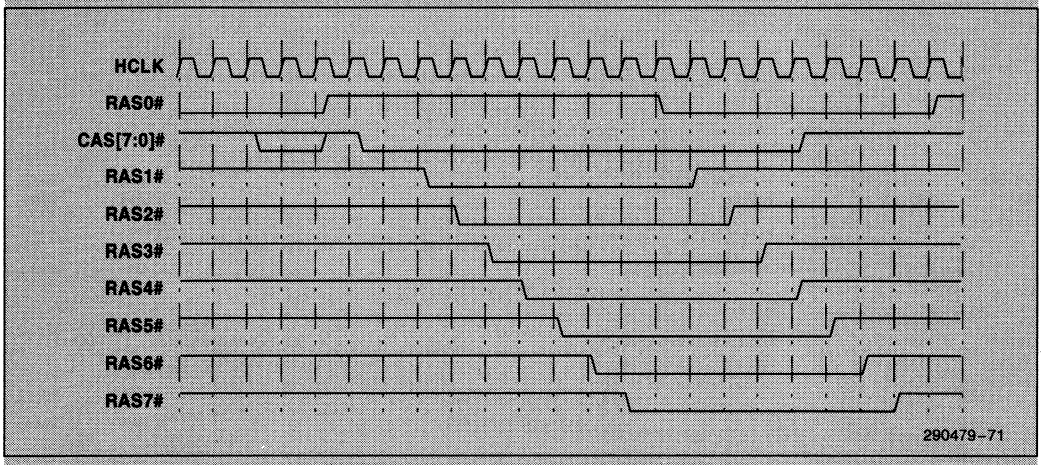


Figure 62. CAS#-Before-RAS# Refresh—Single

6.2.4.3 Hidden Refresh-Single

Figure 63 depicts a hidden refresh cycle which takes place after a DRAM read page hit cycle. The diagram shows a read cycle completing as the refresh timing inside the 82434NX PCMC generates a refresh request. The cycle is an entire Qword; therefore, a hidden refresh is initiated. After the cycle completes, RAS# is negated, but all eight CAS# lines remain asserted. The PCMC then sequentially asserts the RAS# lines, starting with RAS1# since RAS0# was the last active RAS# line. Each RAS# line is asserted for eight clocks.

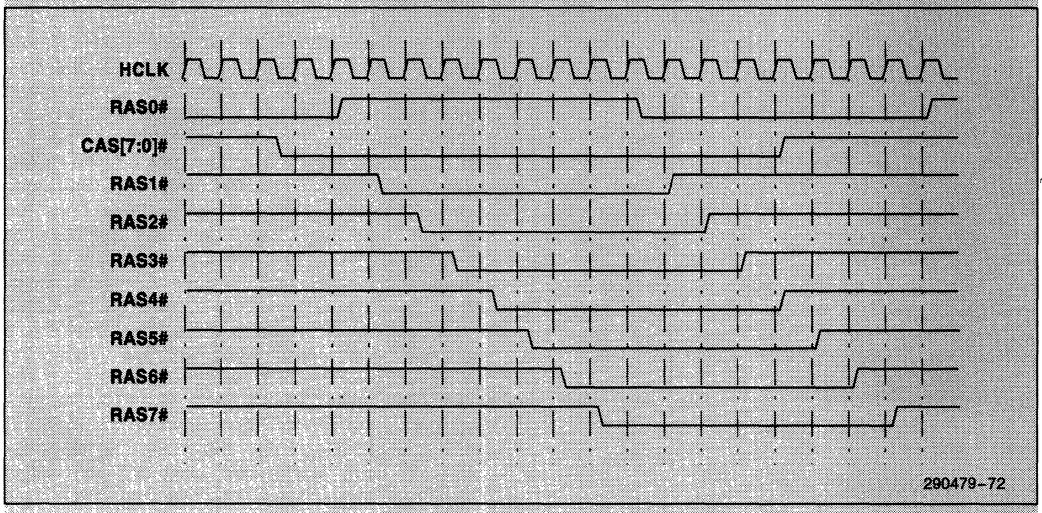


Figure 63. Hidden Refresh—Single

7.0 PCI INTERFACE

The description in this section applies to both the 82434LX and 82434NX.

7.1 PCI Interface Overview

The PCMC and LBXs form a high performance bridge from the Pentium processor to PCI and from PCI to main memory. During PCI-to-main memory cycles, the PCMC and LBXs act as a target on the PCI Bus, allowing PCI masters to read from and write to main memory. During CPU cycles, the PCMC acts as a PCI master. The CPU can then read and write I/O, memory and configuration spaces on PCI. When the CPU accesses I/O mapped and configuration space mapped PCMC registers, the PCMC intercepts the cycles and does not forward them to PCI. Although these CPU cycles do not result in a PCI bus cycle, they are described in this section since most of the PCMC internal registers are mapped into PCI configuration space.

7.2 CPU-to-PCI Cycles

7.2.1 CPU WRITE TO PCI

Figure 64 depicts a series of CPU memory writes which are posted to PCI. The CPU initiates the cycles by asserting ADS# and driving the memory address onto the host address lines. The PCMC asserts NA# in the clock after ADS# allowing the Pentium processor to drive another cycle onto the host bus two clocks later. The PCMC decodes the memory address and drives PCPWL on the HIG[4:0] lines, posting the host address bus and the low Dword of the data bus to the LBXs. The PCMC asserts BRDY#, terminating the CPU cycle with one wait state. Since NA# is asserted in the second clock of the first cycle, the Pentium processor does not insert an idle cycle after this cycle completes, but immediately drives the next cycle onto the bus. Thus, the Pentium processor maximum Dword write bandwidth of 89 MBytes/second is achieved during back-to-back Dword writes cycles. Each of the following write cycles is posted to the LBXs in three clocks.

In this example, the PCMC is parked on PCI and therefore, does not need to arbitrate for the bus. When parked, the PCMC drives the SCPA command on the PIG[3:0] lines and asserts DRVPCI, causing the host address lines to be driven on the PCI AD[31:0] lines. After the write is posted, the PCMC drives the DCPWA command on the PIG[3:0] lines to drive the previously posted address onto the AD[31:0] lines. The PCMC then drives DCPWD onto the PIG[3:0] lines, to drive the previously posted write data onto the AD[31:0] lines. As this is occurring on PCI, the second write cycle is being posted on the host bus. In this case, the second write is to a sequential and incrementing address. Thus, the PCMC leaves FRAME# asserted, converting the write cycle into a PCI burst cycle. The PCMC continues to drive the DCPWD command on the PIG[3:0] lines. The LBXs advance the posted write buffer pointer to point to the next posted Dword when DCPWD is sampled on PIG[3:0] and TRDY# is sampled asserted. Therefore, if the target inserts a wait-state by negating TRDY#, the LBXs continue to drive the data for the current transfer. The remaining writes are posted on the host bus, while the PCMC and LBXs complete the writes on PCI.

CPU I/O write cycles to PCI differ from the memory write cycle described here in that I/O writes are never posted. BRDY# is asserted to terminate the cycle only after TRDY# is sampled asserted, completing the cycle on PCI.

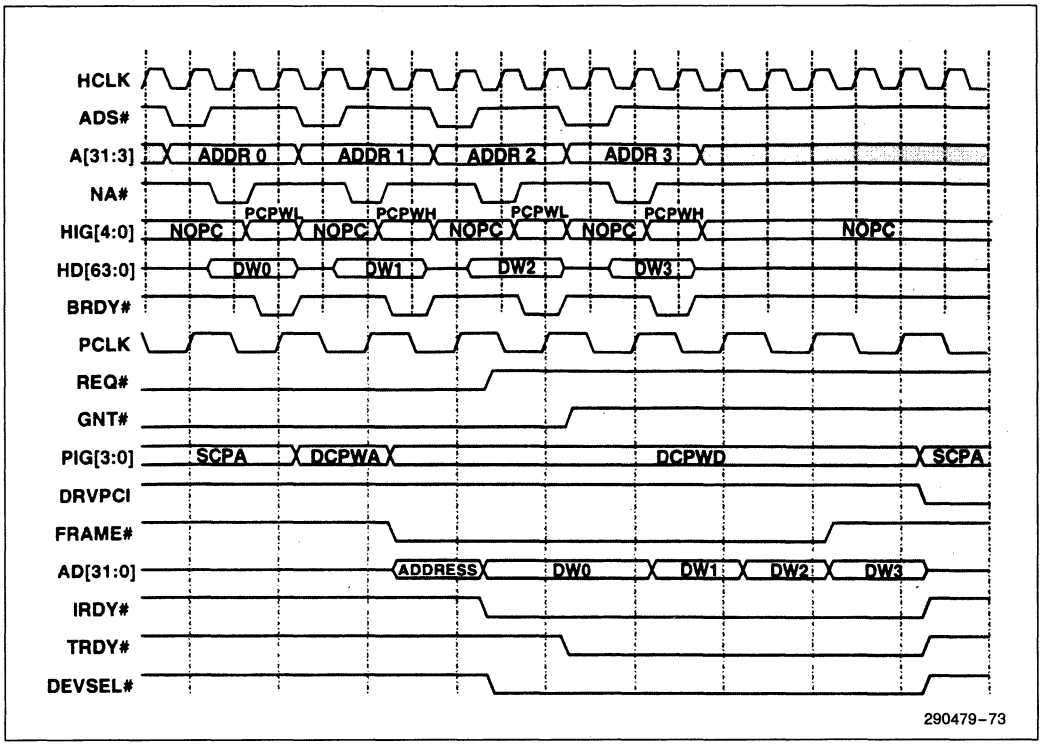


Figure 64. CPU Memory Writes to PCI

7.3 Register Access Cycles

The PCMC contains two registers which are mapped into I/O space, the Configuration Space Enable Register (I/O port CF8h) and the Turbo-Reset Control Register (I/O port CF9h). All other internal PCMC configuration registers are mapped into PCI configuration space. Configuration space must be enabled by writing a non-zero value to the Key field in the CSE Register before accesses to these registers can occur. These registers are mapped to locations C000h through C0FFh in PCI configuration space. If the Key field is programmed with 0h, CPU I/O cycles to locations C000h through CFFFh are forwarded to PCI as ordinary I/O cycles. Externally, accesses to the I/O mapped registers and the configuration space mapped registers use the same bus transfer protocol. Only the PCMC internal decode of the cycle differs. NA# is never asserted during PCMC configuration register or PCI configuration register access cycles. See Section 3.2, PCI Configuration Space Mapped Registers for details on the PCMC configuration space mapping mechanism.

7.3.1 CPU WRITE CYCLE TO PCMC INTERNAL REGISTER

A write to an internal PCMC register (either CSE Register, TRC Register or a configuration space-mapped register) is shown in Figure 65. The cycle begins with the address, byte enables and status signals (W/R#, D/C# and M/IO#) being driven to a valid state indicating an I/O write to either CF8h to access the CSE register, CF9h to access the TRC Register or C0XXh when configuration space is enabled to access a PCMC internal configuration register. The PCMC decodes the cycle and asserts AHOLD to tri-state the CPU address lines. The PCMC signals the LBXs to copy either the upper Dword or the lower Dword of the data bus onto the address lines. The PCMC makes the decision on which Dword to copy based on the BE[7:0]# lines. The HIG[4:0] lines are driven to DACPYH or DACPYL depending on whether the lower Dword of the data bus or the upper Dword of the data bus needs to be copied onto the address bus. The LBXs sample the HIG[4:0] command, and drive the data onto the address lines. The PCMC samples the A[31:0] lines on the second rising edge of HCLK after the LBXs begin driving the data. Finally, the PCMC negates AHOLD and asserts BRDY#, terminating the cycle.

If the write is to the CSE Register and the Key field is programmed to 0000b then configuration space is disabled. If the Key field is programmed to a non-zero value then configuration space is enabled.

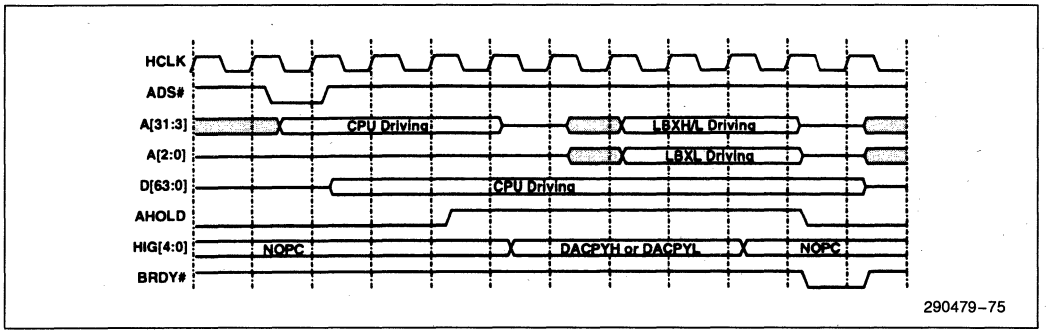


Figure 65. CPU Write to a PCMC Configuration Register

7.3.2 CPU READ FROM PCMC INTERNAL REGISTER

A read from an internal PCMC register (either CSE Register, TRC Register or a configuration space-mapped register) is shown in Figure 66. The I/O read cycle is from either CF8h to access the CSE register, CF9h to access the TRC Register or C0XXh when configuration space is enabled to access a configuration space-mapped register. The PCMC decodes the cycle and asserts AHOLD to tri-state the CPU address lines. The PCMC then drives the contents of the addressed register onto the A[31:0] lines. One byte is enabled on each rising HCLK edge for four consecutive clocks. The PCMC signals the LBXs that the current cycle is a read from an internal PCMC register by issuing the ADCPY command to the LBXs over the HIG[4:0] lines. The LBXs sample the HIG[4:0] command and copy the address lines onto the data lines. Finally, the PCMC negates AHOLD, and asserts BRDY# terminating the cycle.

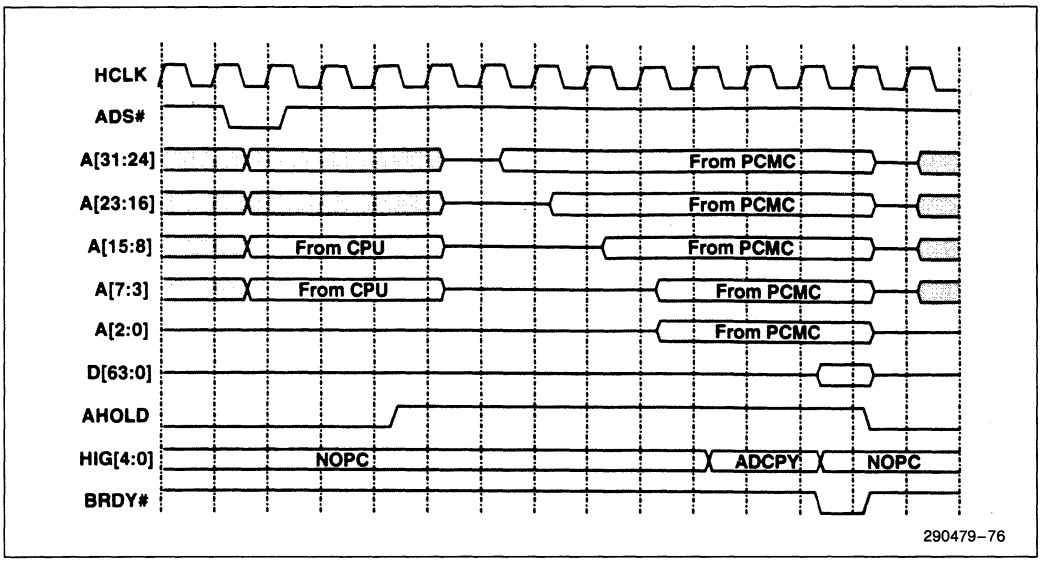


Figure 66. CPU Read from PCMC Configuration Register

7.3.3 CPU WRITE TO PCI DEVICE CONFIGURATION REGISTER

In order to write to or read from a PCI device configuration register the Key field in the CSE register must be programmed to a non-zero value, enabling configuration space. When configuration space is enabled, PCI device configuration registers are accessed by CPU I/O accesses within the range of CnXXh where each PCI device has a unique non-zero value of n. This allows a separate configuration space for each of 15 devices on PCI. Recall that when configuration space is enabled, the PCMC configuration registers are mapped into I/O ports C000h through C0FFh.

A write to a PCI device configuration register is shown in Figure 67. The PCMC internally latches the host address lines and byte enables. The PCMC asserts AHOLD to tri-state the CPU address bus and drives the address lines with the translated address for the PCI configuration cycle. The translation is described in Section 3.2, PCI Configuration Space Mapped Registers. On the HIG[4:0] lines, the PCMC signals the LBXs to latch either the upper Dword of the host data bus or the lower Dword of the host data bus to be driven onto PCI during the data phase of the PCI cycle. On the PIG[3:0] lines, the PCMC signals the LBXs to drive the latched host address lines on the PCI AD[31:0] lines. The upper two bytes of the address lines are used during configuration as IDSEL signals for the PCI devices. The IDSEL pin on each PCI device is connected to one of the AD[31:17] lines.

The PCMC drives the command for a configuration write (1011) onto the C/BE[3:0]# lines and asserts FRAME# for one PCI clock. The PCMC drives the PIG[3:0] lines signaling the LBXs to drive the contents of the PCI write buffer onto the PCI AD[31:0] lines. This command is driven for only one PCI clock before returning to the SCPA command on the PIG[3:0] lines. The LBXs continue to drive the AD[31:0] lines with the valid write data as long as DRVPCI is asserted. The PCMC then asserts IRDY# and waits until sampling the TRDY# signal active. When TRDY# is sampled asserted, the PCMC negates DRVPCI tri-stating the LBX AD[31:0] lines. BRDY# is asserted for one clock to terminate the CPU cycle.

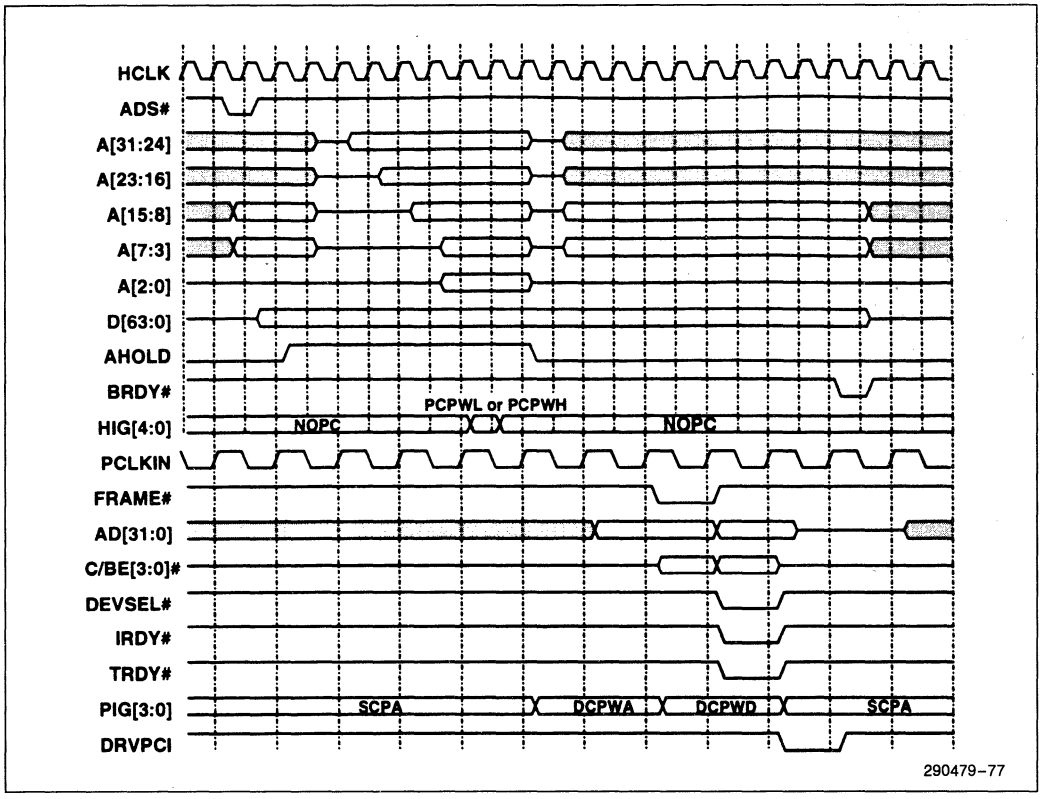


Figure 67. CPU Write to PCI Device Configuration Register

7.3.4 CPU READ FROM PCI DEVICE CONFIGURATION REGISTER

In order to write to or read from a PCI device configuration register the Key field in the CSE register must be programmed to a non-zero value, enabling configuration space. When configuration space is enabled, PCI device configuration registers are accessed by CPU I/O accesses within the range of CnXXh where each PCI device has a unique non-zero value of n. This allows a separate configuration space for each of 15 devices on PCI. Recall that when configuration space is enabled, the PCMC configuration registers occupy I/O addresses C0XXH.

A CPU read from a PCI device configuration register is shown in Figure 68. The PCMC internally latches the host address lines and byte enables. The PCMC asserts AHOLD to tri-state the CPU address bus. The PCMC drives the address lines with the translated address for the PCI configuration cycle. The translation is described in Section 3.2, PCI Configuration Space Mapped Registers. On the PIG[3:0] lines, the PCMC signals the LBXs to drive the latched host address lines on the PCI AD[31:0] lines. The upper two bytes of the address lines are used during configuration as IDSEL signals for the PCI devices. The IDSEL pin on each PCI device is connected to one of the AD[31:17] lines.

The PCMC drives the command for a configuration read (1010) onto the C/BE[3:0]# lines and asserts FRAME# for one PCI clock. The PCMC drives the PIG[3:0] lines signaling the LBXs to latch the data on the PCI AD[31:0] lines into the CPU-to-PCI first read prefetch buffer. The PCMC then drives the HIG[4:0] lines signaling the LBXs to drive the data from the buffer onto the host data lines. The PCMC asserts IRDY# and waits until sampling TRDY# active. After TRDY# is sampled active, BRDY# is asserted for one clock to terminate the CPU cycle.

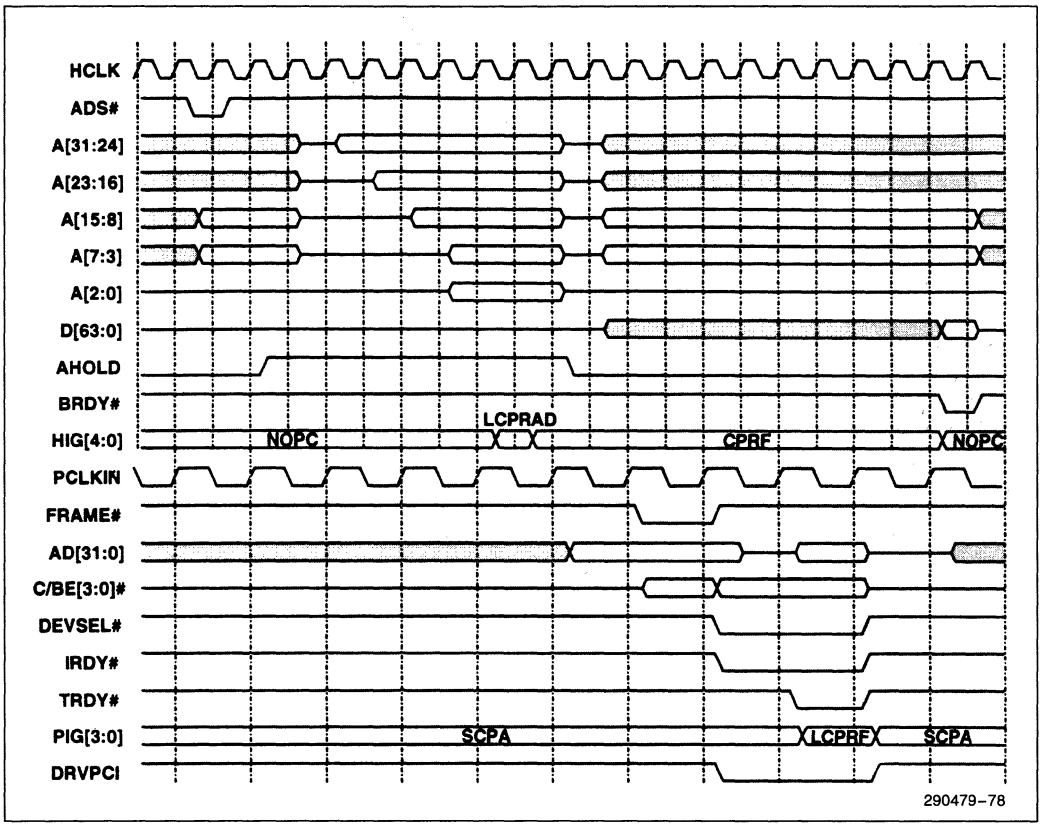


Figure 68. CPU Read from PCI Device Configuration Register

During system initialization, the CPU typically attempts to read from the configuration space of all 15 possible PCI devices to detect the presence of the devices. If no device is present, DEVSEL# is not be asserted and the cycle is terminated, returning FF ... FFh to the CPU. Figure 69 depicts an attempted read from a configuration register of a non-existent device. If no device responds then the PCMC aborts the cycle and sends the DRVFF command over the HIG[4:0] lines causing the LBXs to drive FF ... FFh onto the host data lines.

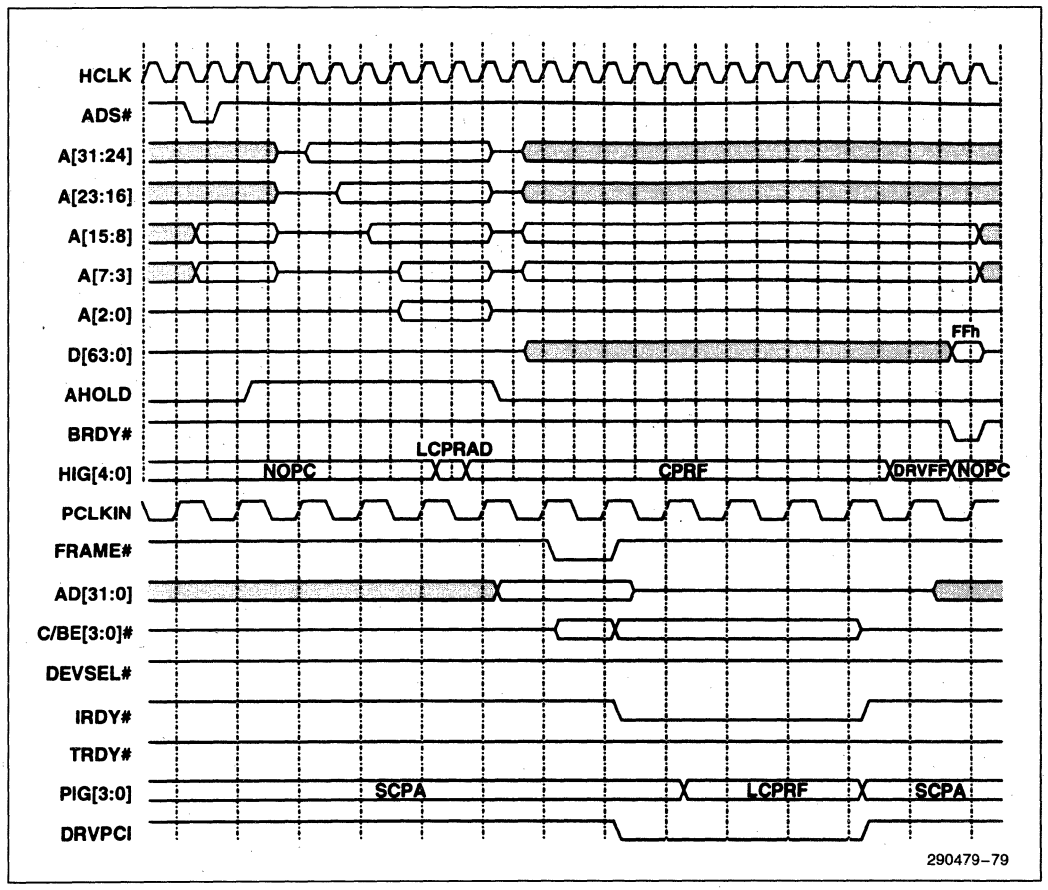


Figure 69. CPU Attempted Configuration Read from Non-Existent PCI Device

7.4 PCI-to-Main Memory Cycles

7.4.1 PCI MASTER WRITE TO MAIN MEMORY

Figure 70 depicts a PCI master burst write to main memory. The PCI master begins by driving the address on the AD[31:0] lines and asserting FRAME#. Upon sampling FRAME# active, the PCMC drives the LCPA command on the PIG[3:0] lines causing the LBXs to retain the address that was latched on the previous PCLK rising edge. The PCMC then samples MEMCS# active, indicating that the cycle is directed to main memory. The PCMC drives the PPMWA command on the PIG[3:0] lines to move the latched PCI address into the write buffer address register. The PCMC then drives the DPWA command on the HIG[4:0] lines enabling the LBXs to drive the PCI master write address onto the host address bus. The PCMC asserts EADS# to initiate a first level cache snoop cycle and simultaneously begins an internal second level cache snoop cycle. Since the snoop is a result of a PCI master write, INV is asserted with EADS#. HITM# remains negated and the snoop either hits an unmodified line or misses in the second level cache, thus no write-back cycles are required. If the snoop hit an unmodified line in either the first or second level cache, the line is invalidated. The cycle is immediately forwarded to the DRAM interface. The four posted Dwords are written to main memory as two Qwords with two CAS[7:0]# cycles. In this example, the DRAM interface is configured for X-3-3-3 write timing, thus each CAS[7:0]# low pulse is two HCLKs in length.

The PCMC disconnects the cycle by asserting STOP# when one of the two four-Dword-deep PCI-to-Memory Posted Write Buffers is full. If the master terminates the cycle before sampling STOP# asserted, then IRDY#, STOP# and DEVSEL# are negated when FRAME# is sampled negated. If the master intended to continue bursting, then the master negates FRAME# when it samples STOP# asserted. IRDY#, STOP# and DEVSEL# are then negated one clock later.

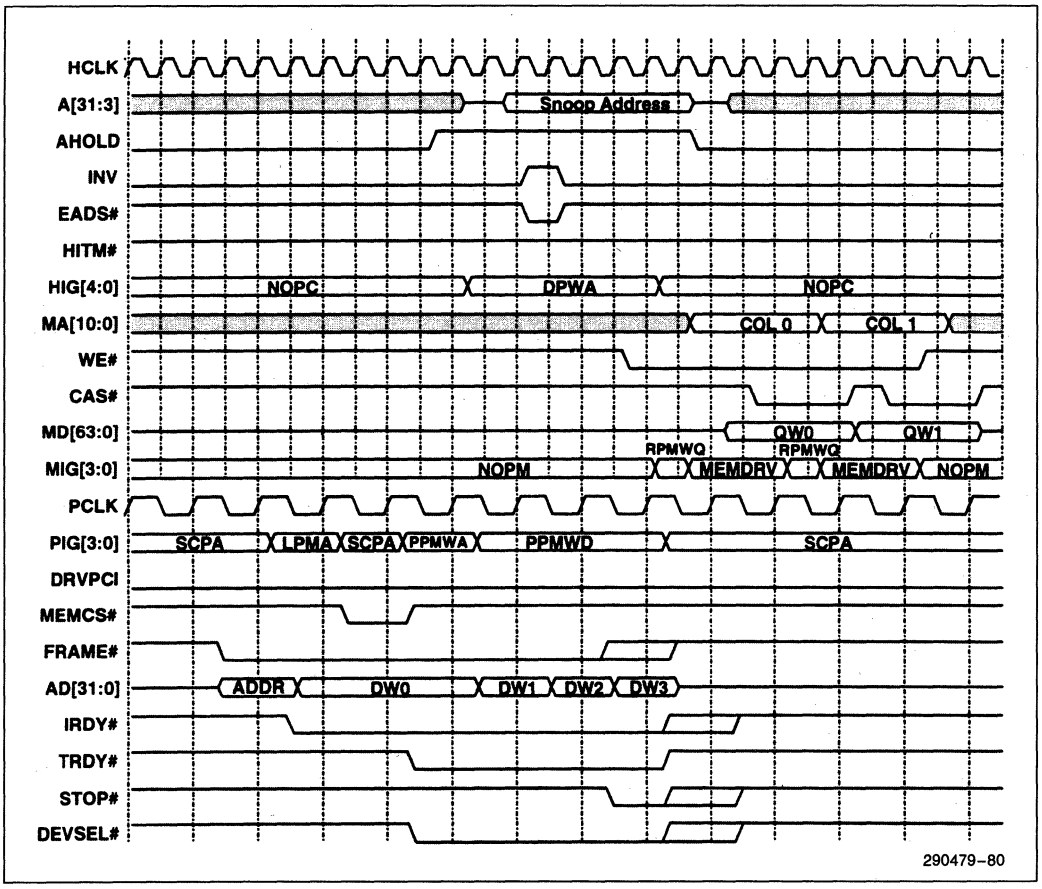


Figure 70. PCI Master Write to Main Memory-Page Hit

7.4.2 PCI MASTER READ FROM MAIN MEMORY

Figure 71 depicts a PCI master read from main memory. The PCI master initiates the cycle by driving the read address on the AD[31:0] lines and asserting FRAME#. The PCMC drives the LPMA command on the PIG[3:0] lines causing the LBXs to retain the address latched on the previous PCLK rising edge. The PCMC drives the DPRA command on the HIG[4:0] lines enabling the LBXs to drive the read address onto the host address lines. The snoop cycle misses in the second level cache and either hits an unmodified line or misses in the first level cache. The cycle is then forwarded to the DRAM interface. A read of four Qwords is performed. Each Qword is posted in the PCI-Memory Read Prefetch Buffer. The data is then driven onto PCI in an eight Dword burst cycle. If the master terminates the cycle before sampling STOP#, then IRDY#, STOP# and DEVSEL# are all negated after FRAME# is sampled inactive. If the master intended to continue bursting, then the master negates FRAME# when it samples STOP# asserted and IRDY#, STOP# and DEVSEL# are negated one clock later.

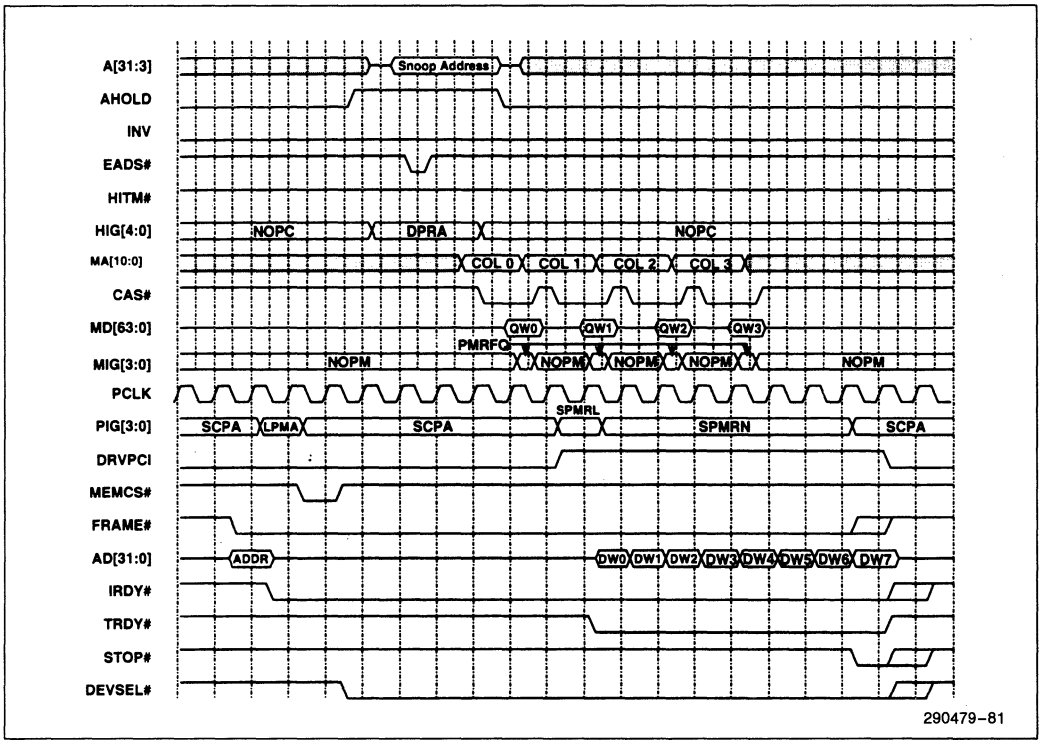


Figure 71. PCI Master Read from Main Memory-Page Hit

8.0 SYSTEM CLOCKING AND RESET

8.1 Clock Domains

The 82434LX and 82434NX PCMCs and 82433LX and 82433NX LBXs operate based on two clocks, HCLK and PCLK. The CPU, second level cache, and the DRAM interfaces operate based on HCLK. The PCI interface timing is based on PCLK.

8.2 Clock Generation and Distribution

Figure 72 shows an example of the 82434LX and 82434NX PCMC host clock distribution in the CPU, cache and memory subsystem. HCLK is distributed to the CPU, PCMC, LBXs and the second level cache SRAMs (in the case of a burst SRAM second level cache).

The host clock originates from an oscillator which is connected to the HCLKOSC input on the PCMC. The PCMC generates six low skew copies of HCLK, HCLKA–HCLKF. Figure 72 shows an example of a host clock distribution scheme for a uni-processor system. In this figure, clock loading is balanced with each HCLK output driving two loads in the system. Each clock output should drive a trace of length *k* with stubs at the end of the trace of length *l* connecting to the two loads. The *l* and *k* parameters should be matched for each of the six clock outputs to minimize overall system clock skew. One of the HCLK outputs is used to clock the PCMC and the Pentium processor. Because the clock driven to the PCMC HCLKIN input and the Pentium processor CLK input originates with the same HCLK output, clock skew between the PCMC and the CPU can be kept lower than between the PCMC and other system components. Another copy of HCLK is used to clock the LBXs. A 256 KByte burst SRAM second level cache can be implemented with eight 32 KByte x 9 synchronous SRAMs. The four remaining copies of HCLK are used to clock the SRAMs. Each HCLK output drives two SRAMs. A 512 KByte second level cache is implemented with four 64 KByte x 18 synchronous SRAMs. Two of the four extra copies are used to clock the SRAMs while the other two are unused. Any one of the HCLK outputs can be used to clock the PCMC and Pentium processor, the two LBXs or any pair of SRAMs. All six copies are identical in drive strength.

Figure 73 depicts the PCI clock distribution.

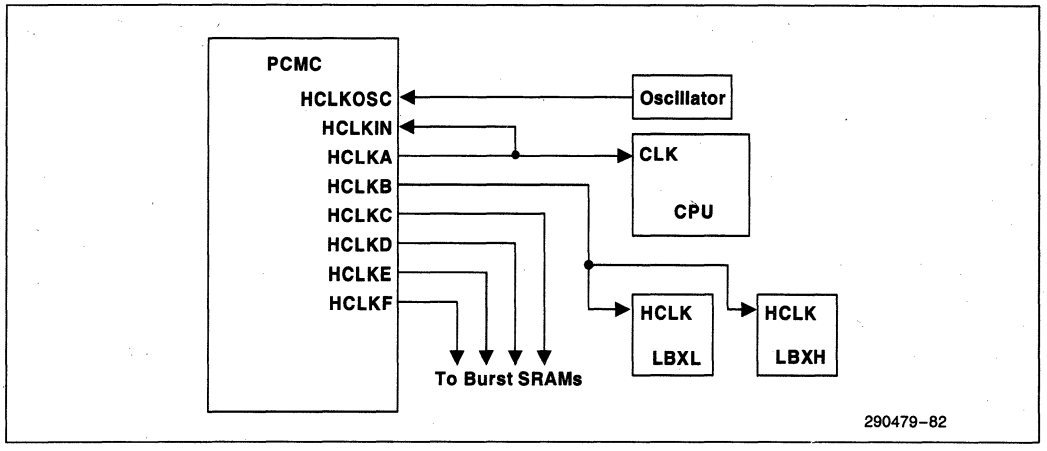


Figure 72. HCLK Distribution Example

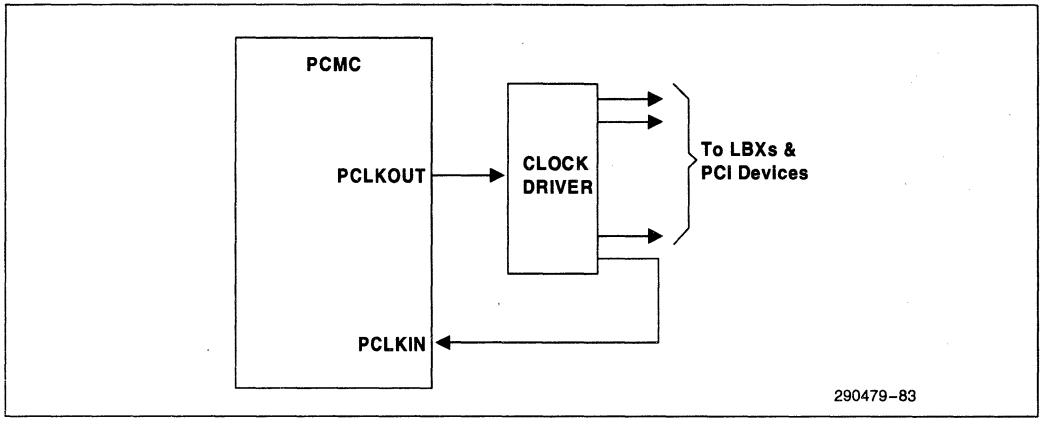


Figure 73. PCI Clock Distribution

The PCMC generates PCLKOUT with an internal Phase Locked Loop (PLL). The PCLKOUT signal is buffered using a single component to produce several low skew copies of PCLK to drive the LBXs and other devices on PCI. One of the outputs of the clock driver is directed back to the PCLKIN input on the PCMC. The PLL locks the rising edges of PCLKIN in phase with the rising edges of HCLKIN. The PLL effectively compensates for the delay of the external clock driver. The resulting PCI clock is one half the frequency of HCLK. Timing for all of the PCI interface signals is based on PCLKIN. All PCI interface inputs are sampled on PCLKIN rising edges and all outputs transition as valid delays from PCLKIN rising edges. Clock skew between the PCLKIN pin on the PCMC and the PCLK pins on the LBXs must be kept within 1.25 ns to guarantee proper operation of the LBXs.

8.3 Phase Locked Loop Circuitry

The 82434LX and 82434NX PCMCs each contain two internal Phase Locked Loops (PLLs). Loop filters and power supply decoupling circuitry must be provided externally. Figure 74 shows the PCMC connections to the external PLL circuitry.

One of the PCMC internal Phase Locked Loops (PLL) locks onto the HCLKIN input. The PLL is used by the PCMC in generating and sampling timing critical signals. An external loop filter is required. The PLLARC1 and PLLARC2 pins connect to the external HCLK loop filter. Two resistors and a capacitor form the loop filter. The loop filter circuitry should be placed as close as possible to the PCMC loop filter pins. The PLL also has dedicated power and ground pins, PLLAVDD, PLLAVSS and PLLAGND. These power pins require a low noise supply. PLLAVDD, PLLAVSS and PLLAGND must be connected to the RC network shown in Figure 74.

The second PCMC internal Phase Locked Loop (PLL) locks the PCLKIN input in phase with the HCLKIN input. The PLL is used by the PCMC to keep the PCI clock in phase with the host clock. An external loop filter is required. The PLLBRC1 and PLLBRC2 pins connect to the external PCLK loop filter. Two resistors and a capacitor form the loop filter. The loop filter circuitry should be placed as close as possible to the PCMC loop filter pins. The PLL also has dedicated power and ground pins, PLLBVDD, PLLBVSS and PLLBGND. These power pins require a low noise supply. PLLBVDD, PLLBVSS and PLLBGND must be connected to the RC network shown in Figure 74.

The resistance and capacitance values for the external PLL circuitry are listed below.

R1 = 10 KΩ ± 5%

R2 = 150Ω ± 5%

R3 = 33Ω ± 5%

C1 = 0.01 μF ± 10%

C2 = 0.47 μF ± 10%

An additional 0.01 μF capacitor in parallel with C2 will help to improve noise immunity.

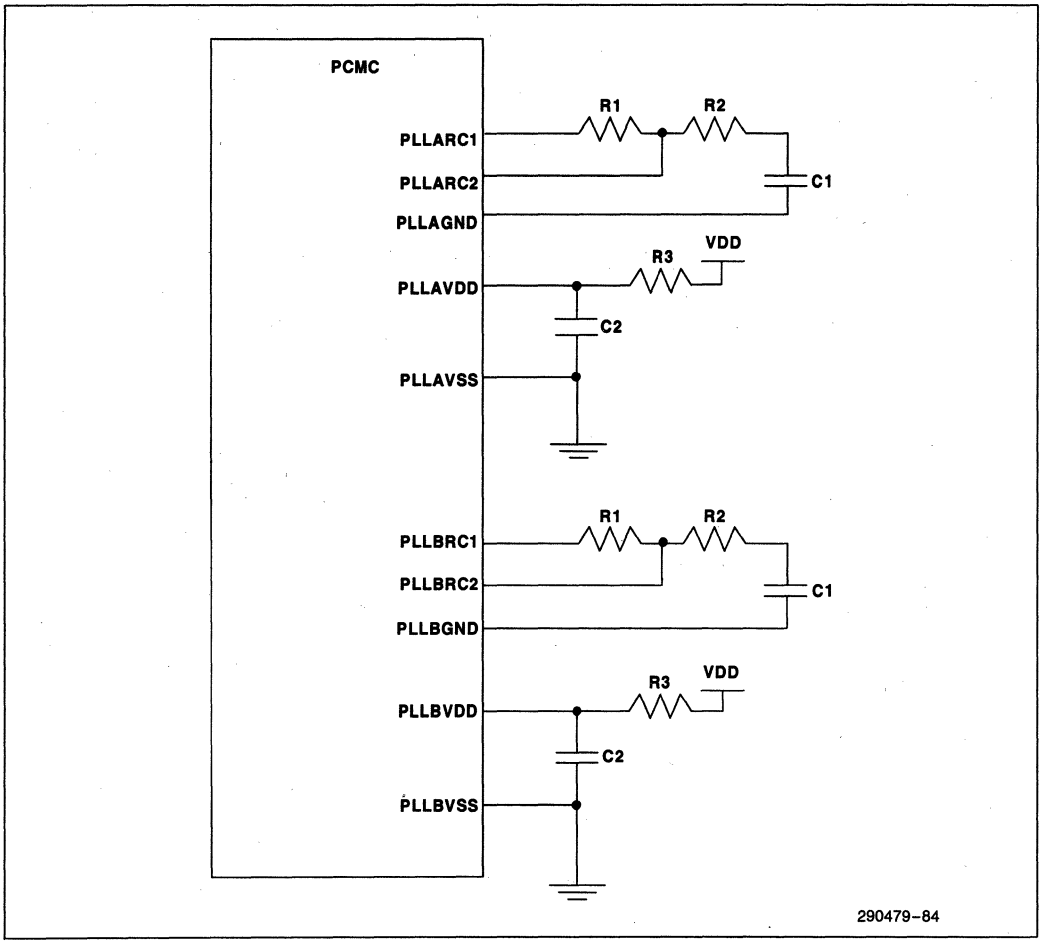


Figure 74. PCMC PLL Circuitry Connections

8.4 System Reset

Figure 75 shows the 82434LX and 82434NX PCMC system reset connections. The 82434LX and 82434NX PCMC reset logic monitors PWROK and generates CPURST, PCIRST# and INIT.

When asserted, PWROK is an indicator to the PCMC that VDD and HCLK have stabilized long enough for proper system operation. CPURST is asserted to initiate hard reset. INIT is asserted to initiate soft reset. PCIRST# is asserted to reset devices on PCI.

Hard reset is initiated by the PCMC in response to one of two conditions. First, hard reset is initiated when power is first applied to the system. PWROK must be driven inactive and must not be asserted until 1 ms after VDD and HCLK have stabilized at their AC and DC specifications. While PWROK is negated, the 82434LX asserts CPURST and PCIRST#. PWROK can be asserted asynchronously. When PWROK is asserted, the 82434LX first ensures that it has been completely initialized before negating CPURST and PCIRST#. CPURST is negated synchronously to the rising edge of HCLK. PCIRST# is negated asynchronously.

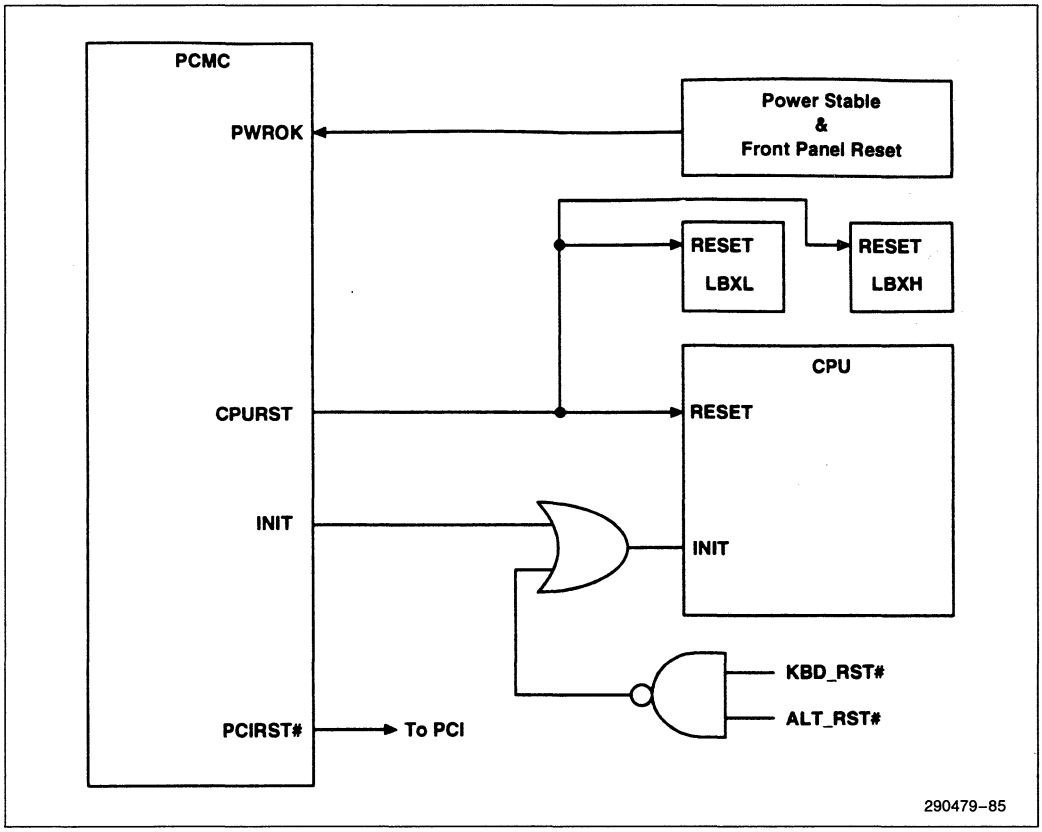


Figure 75. PCMC System Reset Logic

When PWROK is negated, the PCMC asserts AHOLD causing the CPU to tri-state the host address lines. Address lines A[31:29] are sampled by the PCMC 1 ms after the rising edge of PWROK. The values sampled on A[31:30] are inverted inside the PCMC and then stored in Configuration Register 52h bits 7 and 6. The A[31:30] strapping options are depicted in Table 18.

Table 18. A[31:30] Strapping Options

A[31:30]	Configuration Register 52h, Bits[7:6]	Secondary Cache Size
11	00	Not Populated
10	01	Reserved
01	10	256 KByte Cache
00	11	512 KByte Cache

The value sampled on A29 is inverted inside the PCMC and stored in the SRAM Type Bit (bit 5) in the SCC Register. A28 is required to be pulled high for compatibility with future versions of the PCMC.

The PCMC also initiates hard reset when the System Hard Reset Enable bit in the Turbo-Reset Control Register (I/O address CF9h) is set to 1 and the Reset CPU bit toggles from 0 to 1. The PCMC drives CPURST and PCIRST# active for a minimum of 1 ms.

Table 19 shows the state of all 82434LX PCMC output and bi-directional signals during hard reset. During hard reset both CPURST and PCIRST# are asserted. When the hard reset is due to PWROK negation, AHOLD is asserted. The PCMC samples the strapping options on the A[31:29] lines 1 ms after the rising edge of PWROK. When hard reset is initiated via a write to the Turbo-Reset Control Register (I/O port CF9h) AHOLD remains negated throughout the hard reset. Table 19 also applies to the 82434NX, with the exception of the signals listed in Section 8.5, 82434NX Reset Sequencing.

Table 19. 82434LX Output and I/O Signal States During Hard Reset

Signal	State	Signal	State
A[31:0]	Input	IRDY#	Input
AHOLD	High/Low	KEN#	Undefined
BOFF#	High	MA[10:0]	Undefined
BRDY#	High	MDLE	High
CAA[6:3]	Undefined	MEMACK#	High-Z
CAB[6:3]	Undefined	MIG[2:0]	Low
CADS[1:0]#	High	NA#	High
CADV[1:0]#	High	PAR	Input
CALE	High	PEN#	High
CAS[7:0]#	High	PERR#	Input
COE[1:0]#	High	PLOCK#	Input
CWE[7:0]#	High	PIG3	Low
C/BE[3:0]#	Input	PIG[2:0]	High
DEVSEL#	Input	RAS[5:0]#	High
DRVPCI	Low	REQ#	High-Z
EADS#	High	SERR#	Input
FRAME#	Input	STOP#	Input
HIG[4:0]	Low	TRDY#	Input
INIT	Low	WE#	High
INV	Low		

Soft reset is initiated by the PCMC in response to one of two conditions. First, when the System Hard Reset Enable bit in the TRC Register is reset to 0, and the Reset CPU bit toggles from 0 to 1, the PCMC initiates soft reset by asserting INIT for a minimum of 2 HCLKs. Second, the PCMC initiates a soft reset upon detecting a shutdown cycle from the CPU. In this case, the PCMC first broadcasts a shutdown special cycle on PCI and then asserts INIT for a minimum of 2 HCLKs.

8.5 82434NX Reset Sequencing

When PWROK is negated, the 82434NX PCMC drives the following signals low—BRDY#, NA#, AHOLD, EADS#, INV, BOFF#, KEN#, PEN#, CPURST, INIT, CALE, CADS[1:0]#, CADV[1:0]#, CAA[6:3], CAB[6:3], COE[1:0]#, CWE[7:0]#. HCLK[A:F] are driven as soon as the 3.3V supply is active. Note that CWE[7:0]# low prevents the second level cache data RAMs from driving the data bus, even though COE[1:0]# are also driven low. Also, note that BOFF# driven low causes the CPU to tri-state all outputs to the 82434NX PCMC and 82433NX LBX, except HITM#, SMIACT#, and PCHK#. This minimizes the number of signals that the CPU may drive to the PCMC when the 3.3V supply is active and the 5V supply is not active.

Figure 76 shows how the 82434NX sequences CPURST and PCIRST# in response to PWROK assertion.

Some PCI devices may drive 3.3V friendly signals directly to 3.3V devices that are not 5V tolerant. If such signals are powered from the 5V supply they must be driven low when PCIRST# is asserted. Some of these signals may need to be driven high before CPURST is negated. PCIRST# is negated 1 ms before CPURST to allow time for this to occur.

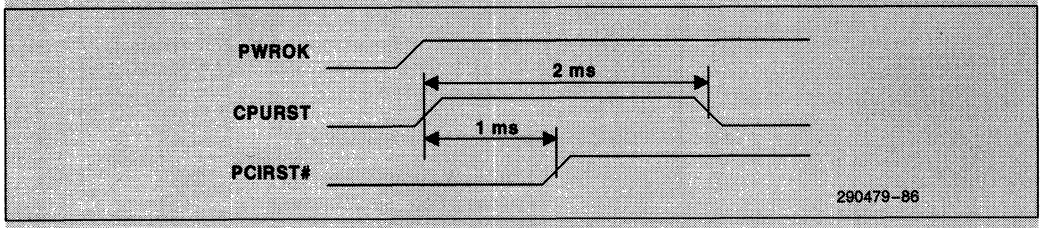


Figure 76. 82434NX Reset Sequencing at Power-Up

9.0 ELECTRICAL CHARACTERISTICS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

9.1 Absolute Maximum Ratings

Case Temperature under Bias .....0°C to +85°C

Storage Temperature .....−55°C to +150°C

Voltage on Any Pin
with Respect to Ground.....−0.3 to V_{CC} + 0.3V

Supply Voltage
with Respect to V_{SS} .....−0.3 to +6.5V

Maximum Total Power Dissipation 2.0W

Maximum Power Dissipation, $V_{CC}3$ .....470 mW

The Maximum total power dissipation in the 82434NX on the V_{CC} and $V_{CC}3$ pins is 2.0W. The $V_{CC}3$ pins may draw as much as 470 mW, however, total power will not exceed 2.0W.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

9.2 Thermal Characteristics

The 82434LX and 82434NX PCMCs are designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the package are given in Table 20.

Table 20. PCMC Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)				
	0 (0)	0.5 (98.4)	1.0 (196.9)	2.0 (393.7)	5.0 (984.3)
θ_{JA} (°C/Watt)	31	27	24.5	23	19
θ_{JC} (°C/Watt)	8.6				

9.3 82434LX DC Characteristics

Functional Operating Range (V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL1}	Input Low Voltage	−0.3	0.8	V	Note 1, V_{CC} = 4.75V
V_{IH1}	Input High Voltage	2.2	V_{CC} + 0.3	V	Note 1, V_{CC} = 5.25V
V_{IL2}	Input Low Voltage	−0.3	1.35	V	Note 2, V_{CC} = 4.75V
V_{IH2}	Input High Voltage	3.85	V_{CC} + 0.3	V	Note 2, V_{CC} = 5.25V
V_{T1}	Schmitt Trigger Threshold Voltage, Falling Edge	0.7	1.35	V	Note 3, V_{CC} = 5.0V
V_{T1+}	Schmitt Trigger Threshold Voltage, Falling Edge	1.4	2.2	V	Note 3, V_{CC} = 5.0V
V_{H1}	Hysteresis Voltage	0.3	1.2	V	Note 3, V_{CC} = 5.0V
V_{T2-}	Schmitt Trigger Threshold Voltage, Falling Edge	1.25	2.3	V	Note 3, V_{CC} = 5.0V
V_{T2+}	Schmitt Trigger Threshold Voltage, Rising Edge	2.3	3.7	V	Note 3, V_{CC} = 5.0V
V_{H2}	Hysterersis Voltage	0.3	1.2	V	Note 3, V_{CC} = 5.0V

Functional Operating Range (V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C) (Continued)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OL1}	Output Low Voltage		0.5	V	Note 4
V_{OH1}	Output High Voltage	V_{CC} − 0.5		V	Note 4
V_{OL2}	Output Low Voltage		0.4	V	Note 5
V_{OH2}	Output High Voltage	2.4		V	Note 5
I_{OL1}	Output Low Current		1	mA	Note 6
I_{OH1}	Output High Current	−1		mA	Note 6
I_{OL2}	Output Low Current		3	mA	Note 7
I_{OH2}	Output High Current	−2		mA	Note 7
I_{OL3}	Output Low Current		6	mA	Note 8
I_{OH3}	Output High Current	−2		mA	Note 8
I_{OL4}	Output Low Current		3	mA	Note 9
I_{OH4}	Output High Current	−1		mA	Note 9
I_{IH}	Input Leakage Current		+10	uA	
I_{IL}	Input Leakage Current		−10	uA	
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz

NOTES:
1. V_{IL1} and V_{IH1} apply to the following signals: A[31:0], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, PCHK#, HITM#, CACHE#, SMIACT#, PCLKIN, HCLKIN, HCLKOSC, FLSHBUF#, MEMCS#, SERR#, PERR#, MEMREQ#, GNT#, PLOCK#, STOP#, IRDY#, TRDY#, FRAME#, C/BE[3:0]#.
2. V_{IL2} and V_{IH2} apply to the following signals: PPOUT[1:0], EOL.
3. V_{T1-}, V_{T1+} and V_{H1} apply to PWROK. V_{T2-}, V_{T2+} and V_{H2} apply to TESTEN.
4. V_{OL1} and V_{OH1} apply to the following signals: HIG[4:0], MIG[2:0], PIG[3:0], DRVPCI, MDLE, PCIRST#.
5. V_{OL2} and V_{OH2} apply to the following signals: REQ#, MEMACK#, FRAME#, C/BE[3:0]#, TRDY#, IRDY#, STOP#, PLOCK#, DEVSEL#, PAR, PERR#, SERR#, BOFF#, AHOLD, BRDY#, NA#, EADS#, KEN#, INV, A[31:0], PCLKOUT, HCLKA–HCLKF, CALE, COE[1:0]#, CWE[7:0]#, CADV[1:0]#, CADS[1:0]#, CAA[6:3], CAB[6:3], RAS[5:0]#, CAS[7:0]#, MA[10:0], WE#.
6. I_{OL1} and I_{OH1} apply to the following signals: HIG[4:0], MIG[2:0], PIG[3:0], DRVPCI, MDLE, PCIRST#.
7. I_{OL2} and I_{OH2} apply to the following signals: C/BE[3:0]#, REQ#, MEMACK#, MA[10:0], WE#.
8. I_{OL3} and I_{OH3} apply to the following signals: FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, DEVSEL#, PAR, PERR#, SERR#.
9. I_{OL4} and I_{OH4} apply to the following signals: BOFF#, AHOLD, BRDY#, NA#, EADS#, KEN#, INV, CPURST, INIT, A[31:0], PCLKOUT, CALE, COE[1:0]#, CADS[1:0]#, CADV[1:0]#, CWE[7:0]#, CAA[6:3], CAB[6:3], RAS[5:0]#, CAS[7:0]#.

9.4 82434NX DC Characteristics

Functional Operating Range (V_{CC} = 5V ±5%; $V_{CC}3$ = 3.135 to 3.465 V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL1}	Input Low Voltage	−0.3	0.8	V	Note 1, V_{CC} = 4.75V
V_{IH1}	Input High Voltage	2.2	V_{CC} + 0.3	V	Note 1, V_{CC} = 5.25V
V_{IL2}	Input Low Voltage	−0.3	1.35	V	Note 2, V_{CC} = 4.75V
V_{IH2}	Input High Voltage	3.85	V_{CC} + 0.3	V	Note 2, V_{CC} = 5.25V
V_{IL3}	Input Low Voltage	−0.3	0.8	V	Note 3, V_{ccq} = 3.135V
V_{IH3}	Input High Voltage	2.2	V_{CC} + 0.3	V	Note 3, V_{ccq} = 3.465V
V_{T1}	Schmitt Trigger Threshold Voltage, Falling Edge	0.7	1.35	V	Note 4, V_{CC} = 5.0V
V_{T1+}	Schmitt Trigger Threshold Voltage, Rising Edge	1.4	2.2	V	Note 4, V_{CC} = 5.0V
V_{H1}	Hysteresis Voltage	0.3	1.2	V	Note 4, V_{CC} = 5.0V
V_{T2-}	Schmitt Trigger Threshold Voltage, Falling Edge	1.25	2.3	V	Note 4, V_{CC} = 5.0V
V_{T2+}	Schmitt Trigger Threshold Voltage, Rising Edge	2.3	3.7	V	Note 4, V_{CC} = 5.0V
V_{H2}	Hysterersis Voltage	0.3	1.2	V	Note 4, V_{CC} = 5.0V
V_{OL1}	Output Low Voltage		0.5	V	Note 5
V_{OH1}	Output High Voltage	V_{CC} − 0.5		V	Note 5
V_{OL2}	Output Low Voltage		0.4	V	Note 6
V_{OH2}	Output High Voltage	2.4		V	Note 6
I_{OL1}	Output Low Current		1	mA	Note 7
I_{OH1}	Output High Current	−1		mA	Note 7
I_{OL2}	Output Low Current		3	mA	Note 8

Functional Operating Range (V_{CC} = 5V ±5%; $V_{CC}3$ = 3.135 to 3.465 V; T_{CASE} = 0°C to +85°C) (Continued)

Symbol	Parameter	Min	Max	Unit	Test Conditions
I_{OH2}	Output High Current	−2		mA	Note 8
I_{OL3}	Output Low Current		6	mA	Note 9
I_{OH3}	Output High Current	−2		mA	Note 9
I_{OL4}	Output Low Current		3	mA	Note 10
I_{OH4}	Output High Current	−1		mA	Note 10
I_{IH}	Input Leakage Current		+10	uA	
I_{IL}	Input Leakage Current		−10	uA	
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz

NOTES:
1. V_{IL1} and V_{IH1} apply to the following signals: BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, PCHK#, HITM#, CACHE#, SMIACT#, PCLKIN, HCLKOSC, FLSHBUF#, MEMCS#, SERR#, PERR#, MEMREQ#, GNT#, PLOCK#, STOP#, IRDY#, TRDY#, FRAME#, C/BE[3:0]#.
2. V_{IL2} and V_{IH2} apply to the following signals: PPOUT[1:0], EOL.
3. VIL3 and VIH3 apply to the following signals: A[31:0], HCLKIN.
4. V_{T1-}, V_{T1+} and V_{H1} apply to PWROK. V_{T2-}, V_{T2+} and V_{H2} apply to TESTEN.
5. V_{OL1} and V_{OH1}apply to the following signals: HIG[4:0], MIG[2:0], PIG[3:0], DRVPCI, MDLE, PCIRST#.
6. V_{OL2} and V_{OH2} apply to the following signals: REQ#, MEMACK#, FRAME#, C/BE[3:0]#, TRDY#, IRDY#, STOP#, PLOCK#, DEVSEL#, PAR, PERR#, SERR#, BOFF#, AHOLD, BRDY#, NA#, EADS#, KEN#, INV, A[31:0], PCLKOUT, HCLKA–HCLKF, CALE, COE[1:0]#, CWE[7:0]#, CADV[1:0]#, CADS[1:0]#, CAA[6:3], CAB[6:3], RAS[7:0]#, CAS[7:0]#, MA[11:0], WE#.
7. I_{OL1} and I_{OH1} apply to the following signals: HIG[4:0], MIG[2:0], PIG[3:0], DRVPCI, MDLE, A[31:8], A[2:0], PCIRST#.
8. I_{OL2} and I_{OH2} apply to the following signals: C/BE[3:0]#, REQ#, MEMACK#, MA[11:0], WE#.
9. I_{OL3} and I_{OH3} apply to the following signals: FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, DEVSEL#, PAR, PERR#, SERR#.
10. I_{OL4} and I_{OH4} apply to the following signals: BOFF#, AHOLD, BRDY#, NA#, EADS#, KEN#, INV, CPURST, INIT, A[7:3], PCLKOUT, CALE, COE[1:0]#, CADS[1:0]#, CADV[1:0]#, CWE[7:0]#, CAA[6:3], CAB[6:3], RAS[7:0]#, CAS[7:0]#.
11. The output buffers for BRDY#, NA#, AHOLD, EADS#, INV, BOFF#, KEN#, PEN#, CPURST, INIT, CALE, CADS[1:0], CADV[1:0]#, CAA[6:3], CAB[6:3], COE[1:0]#, CWE[7:0]#, A[31:3] AND HCLK[A:F] are powered with $V_{CC}3$ and therefore drive 3.3V signal levels.

9.5 82434LX AC Characteristics

The AC characteristics given in this section consist of propagation delays, valid delays, input setup requirements, input hold requirements, output float delays, output enable delays, output-to-output delays, pulse widths, clock high and low times and clock period specifications. Figure 77 through Figure 85 define these specifications. Section 9.5 lists the 82434LX AC Characteristics. Output test loads are listed in the right column.

In Figure 77 through Figure 85, VT = 1.5V for the following signals:

A[31:0], BE[7:0]#, PEN#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, PCHK#, HITM#, EADS#, BRDY#, BOFF#, AHOLD, NA#, KEN#, INV, CACHE#, SMIACT#, INIT, CPURST, CALE, CADV[1:0]#, COE[1:0]#, CWE[7:0]#, CADS[1:0]#, CAA[6:3], CAB[6:3], WE#, RAS[5:0]#, CAS[7:0]#, MA[10:0], C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, GNT#, DEVSEL#, MEMREQ#, PAR, PERR#, SERR#, REQ#, MEMCS#, FLSHBUF#,MEMACK#, PWROK, HCLKIN, HCLKA–HCLKF, PCLKIN, PCLKOUT.

VT = 2.5V for the following signals:

PPOUT[1:0], EOL, HIG[4:0], PIG[3:0], MIG[2:0], DRVPCI, MDLE, PCIRST#.

9.5.1 HOST CLOCK TIMING, 66 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C)

Symbol	Parameter	Min	Max	Figure	Notes
t1a	HCLKOSC High Time	6.0		82	
t1b	HCLKOSC Low Time	5.0		82	
t2a	HCLKIN Period	15	20	82	
t2b	HCLKIN Period Stability		±100		ps(1)
t2c	HCLKIN High Time	4		82	
t2d	HCLKIN Low Time	4		82	
t2e	HCLKIN Rise Time		1.5	83	
t2f	HCLKIN Fall Time		1.5	83	
t3a	HCLKA–HCLKF Output-to-Output Skew		0.5	85	0 pF
t3b	HCLKA–HCLKF High Time	5.0		85	0 pF
t3c	HCLKA–HCLKF Low Time	5.0		85	0 pF

NOTE:
1. Measured on rising edge of adjacent clocks at 1.5V.

9.5.2 CPU INTERFACE TIMING, 66 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C)

Symbol	Parameter	Min	Max	Fig	Notes
t10a	ADS#, HITM#, W/R#, M/IO#, D/C#, HLOCK#, CACHE#, BE[7:0]#, SMIACT# Setup Time to HCLKIN Rising	4.6		79	
t10b	ADS#, HITM#, W/R#, M/IO#, D/C#, HLOCK#, CACHE#, BE[7:0]#, SMIACT# Hold Time from HCLKIN Rising	0.8		79	
t11a	PCHK# Setup Time to HCLKIN Rising	4.3		79	
t11b	PCHK# Hold Time from HCLKIN Rising	1.1		79	
t12a	A[18:3] Rising Edge Setup Time to HCLKIN Rising	4.5		79	Setup to HCLKIN rising when ADS# is sampled active by PCMC.
t12aa	A[18:3] Falling Edge Setup Time to HCLKIN Rising	3.2		79	Setup to HCLKIN Rising when ADS# is Sampled Active by PCMC.
t12ab	A[18:3] Rising Edge Setup Time to HCLKIN Rising	4.7			Setup to HCLKIN Rising when ADS# is Sampled Active by PCMC.
t12ac	A[18:3] Falling Edge Setup Time to HCLKIN Rising	4.1			Setup to HCLKIN Rising when ADS# is Sampled Active by PCMC.
t12b	A[31:0] Hold Time from HCLKIN Rising	0.5		79	Hold from HCLKIN rising two clocks after ADS# is sampled active by PCMC.
t12c	A[31:0] Setup Time to HCLKIN Rising	6.5		79	Setup to HCLKIN rising when EADS# is sampled active by the CPU.
t12d	A[31:0] Hold Time from HCLKIN Rising	1.5		79	Hold from HCLKIN rising when EADS# is sampled active by the CPU.

Functional Operating Range (V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C) (Continued)

Symbol	Parameter	Min	Max	Fig	Notes
t12e	A[31:0] Output Enable from HCLKIN Rising	0	13	81	
t12f	A[31:0] Valid Delay from HCLKIN Rising	1.3	13	78	0 pF
t12g	A[31:0] Float Delay from HCLKIN Rising	0	13	80	
t12h	A[2:0] Propagation Delay from BE[7:0]#	1	16	77	0 pF
t13a	BRDY# Rising Edge Valid Delay from HCLKIN Rising	1.7	7.8	78	0 pF
t13b	BRDY# Falling Edge Valid Delay from HCLKIN Rising	1.7	7.6	78	0 pF
t14	NA# Valid Delay from HCLKIN Rising	1.3	7.8	78	0 pF
t15a	AHOLD Valid Delay from HCLKIN Rising	1.3	7.1	78	0 pF
t15b	BOFF# Valid Delay from HCLKIN Rising	1.8	7.1	78	
t16a	EADS#, INV, PEN# Valid Delay from HCLKIN Rising	1.3	7.4	78	0 pF
t16b	CPURST Rising Edge Valid Delay from HCLKIN Rising	0.9	7.5	78	
t16c	CPURST Falling Edge Valid Delay from HCLKIN Rising	0.9	7.0	78	
t16d	KEN# Valid delay from HCLKIN Rising	1.3	7.6	78	
t17	INIT High Pulse Width	2 HCLKs		84	Soft reset via TRC register or CPU shutdown special cycle
t18	CPURST High Pulse Width	1 ms		84	Hard reset via TRC register, 0 pF

9.5.3 SECOND LEVEL CACHE STANDARD SRAM TIMING, 66 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C)

Symbol	Parameter	Min	Max	Fig	Notes
t20a	CAA[6:3]/CAB[6:3] Propagation Delay from A[6:3]	0	8.5	77	0 pF
t20b	CAA[6:3]/CAB[6:3] Valid Delay from HCLKIN Rising	0	7.2	78	0 pF
t21a	COE[1:0]# Falling Edge Valid Delay from HCLKIN Rising	0	9	78	0 pF
t21b	COE[1:0]# Rising Edge Valid Delay from HCLKIN Rising	0	5.5	78	0 pF
t22a	CWE[7:0]#/CBS[7:0]# Falling Edge Valid Delay from HCLKIN Rising	2	14	78	CPU burst or single write to second level cache, 0 pF
t22b	CWE[7:0]#/CBS[7:0]# Rising Edge Valid Delay from HCLKIN Rising	3	14	78	CPU burst or single write to second level cache, 0 pF
t22c	CWE[7:0]#/CBS[7:0]# Valid Delay from HCLKIN Rising	1.4	7.7	78	Cache line Fill, 0 pF
t22d	CWE[7:0]#/CBS[7:0]# Low Pulse Width	1 HCLK		84	0 pF
t22e	CWE[7:0]#/CBS[7:0]# Driven High before CALE Driven High	-1		85	Last write to second level cache during cache line fill, 0 pF
t22f	CAA[4:3]/CAB[4:3] Valid before CWE[7:0]# Falling	1.5		85	CPU burst write to second level cache, 0 pF
t23	CALE Valid Delay from HCLKIN Rising	0	7.5	78	0 pF
t24	CR/W[1:0]# Valid Delay from HCLKIN Rising	1.5	7.6	78	0 pF
t25	CBS[1:0]# Valid Delay from HCLKIN Rising; Reads from Cache SRAMs	1.0	12.0	78	0 pF

9.5.4 SECOND LEVEL CACHE BURST SRAM TIMING, 66 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C)

Symbol	Parameter	Min	Max	Fig	Notes
t30a	CAA[6:3]/CAB[6:3] Propagation Delay from A[6:3]	0	8.5	77	0 pF
t30b	CAA[6:3]/CAB[6:3] Valid Delay from HCLKIN Rising	0	7.0	78	0 pF
t31	CADS[1:0]# Valid Delay from HCLKIN Rising	1.5	7.7	78	0 pF
t32	CADV[1:0]# Valid Delay from HCLKIN Rising	1.5	7.1	78	0 pF
t33	CWE[7:0]# Valid Delay from HCLKIN Rising	1.0	9.0	78	0 pF
t34a	COE[1:0]# Falling Edge Valid Delay from HCLKIN Rising	0	9.0	78	0 pF
t34b	COE[1:0]# Rising Edge Valid Delay from HCLKIN Rising	0	5.5	78	0 pF
t35	CALE Valid Delay from HCLKIN Rising	0	7.5	78	0 pF

9.5.5 DRAM INTERFACE TIMING, 66 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C)

Symbol	Parameter	Min	Max	Fig	Notes
t40a	RAS[5:0]# Valid Delay from HCLKIN Rising	0	7.5	78	50 pF
t40b	RAS[5:0]# Pulse Width High	4 HCLKs − 5		84	RAS# precharge at beginning of page miss cycle, 50 pF
t41a	CAS[7:0]# Valid Delay from HCLKIN Rising	0	7.5	78	50 pF
t41b	CAS[7:0]# Pulse Width High	1 HCLKIN − 5		84	CAS# precharge during burst cycles, 50 pF
t42	WE# Valid Delay from HCLKIN Rising	0	21	78	50 pF
t43a	MA[10:0] Propagation Delay from A[23:3]	0	23	77	50 pF
t43b	MA[10:0] Valid Delay from HCLKIN Rising	0	10.1	78	50 pF

9.5.6 PCI CLOCK TIMING, 66 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C)

Symbol	Parameter	Min	Max	Fig	Notes
t50a	PCLKOUT High Time	13		82	20 pF
t50b	PCLKOUT Low Time	13		82	20 pF
t51a	PCLKIN High Time	12		82	
t51b	PCLKIN Low Time	12		82	
t51c	PCLKIN Rise Time		3	83	
t51d	PCLKIN Fall Time		3	83	

9.5.7 PCI INTERFACE TIMING, 66 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C)

Symbol	Parameter	Min	Max	Fig	Notes
t60a	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Valid Delay from PCLKIN Rising	2	11	78	Min: 0 pF Max: 50 pF
t60b	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Output Enable Delay from PCLKIN Rising	2		81	
t60c	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Float Delay from PCLKIN Rising	2	28	80	
t60d	C/BE[3:0]#, FRAME#, PLOCK#, PAR, PERR#, SERR#, Setup Time to PCLKIN Rising	7		79	
t60da	TRDY#, IRDY# Setup Time to PCLKIN Rising	8.1		77	
t60db	STOP#, DEVSEL# Setup Time to PCLKIN Rising	8.5		77	
t60e	C/BE[3:0]#, FRAME#, PLOCK#, PAR, PERR#, SERR# Hold Time from PCLKIN Rising	0		77	
t61a	REQ#, MEMACK# Valid Delay from PCLKIN Rising	2	12	78	Min: 0 pF Max: 50 pF
t61b	REQ#, MEMACK# Output Enable Delay from PCLKIN Rising	2		81	
t61c	REQ#, MEMACK# Float Delay from PCLKIN Rising	2	28	80	
t62a	FLSHREQ#, MEMREQ# Setup Time to PCLKIN Rising	12		79	
t62b	FLSHREQ#, MEMREQ# Hold Time from PCLKIN Rising	0		79	
t63a	GNT# Setup Time to PCLKIN Rising	10		79	
t63b	GNT# Hold Time from PCLKIN Rising	0		79	
t64a	MEMCS# Setup Time to PCLKIN Rising	7		79	
t64b	MEMCS# Hold Time from PCLKIN Rising	0		79	
t65	PCIRST# Low Pulse Width	1 ms		84	Hard Reset via TRC Register, 0 pF

9.5.8 LBX INTERFACE TIMING, 66 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.9V to 5.25V; T_{CASE} = 0°C to +70°C)

Symbol	Parameter	Min	Max	Fig	Notes
t70	HIG[4:0] Valid Delay from HCLKIN Rising	0.8	6.5	78	0 pF
t71	MIG[2:0] Valid Delay from HCLKIN Rising	0.9	6.5	78	0 pF
t72	PIG[3:0] Valid Delay from PCLKIN Rising	0.7	10.9	78	0 pF
t73	PCIDRV Valid Delay from PCLKIN Rising	1	13.5	78	0 pF
t74a	MDLE Falling Edge Valid Delay from HCLKIN Rising	0.6	5.6	78	0 pF
t74b	MDLE Rising Edge Valid Delay from HCLKIN Rising	0.6	6.8	85	0 pF
t75a	EOL, PPOUT[1:0] Setup Time to PCLKIN Rising	7.7		79	
t75b	EOL, PPOUT[1:0] Hold Time from PCLKIN Rising	1.0		79	

9.5.9 HOST CLOCK TIMING, 60 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t1a	HCLKOSC High Time	6.0		82	
t1b	HCLKOSC Low Time	5.0		82	
t2a	HCLKIN Period	16.66	20	82	
t2b	HCLKIN Period Stability		±100		ps(1)
t2c	HCLKIN High Time	4		82	
t2d	HCLKIN Low Time	4		82	
t2e	HCLKIN Rise Time		1.5	83	
t2f	HCLKIN Fall Time		1.5	83	
t3a	HCLKA–HCLKF Output-to-Output Skew		0.5	85	0 pF
t3b	HCLKA–HCLKF High Time	5.0		82	0 pF
t3c	HCLKA–HCLKF Low Time	5.0		82	0 pF

NOTE:
1. Measured on rising edge of adjacent clocks at 1.5V.

9.5.10 CPU INTERFACE TIMING, 60 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t10a	ADS#, HITM#, W/R#, M/IO#, D/C#, HLOCK#, CACHE#, BE[7:0]#, SMIACT# Setup Time to HCLKIN Rising	4.6		79	
t10b	ADS#, HITM#, W/R#, M/IO#, D/C#, HLOCK#, CACHE#, BE[7:0]#, SMIACT# Hold Time from HCLKIN Rising	1.1		79	
t11a	PCHK# Setup Time to HCLKIN Rising	4.3		79	
t11b	PCHK# Hold Time from HCLKIN Rising	1.1		79	
t12a	A[18:3] Rising Edge Setup Time to HCLKIN Rising	4.5		79	Setup to HCLKIN rising when ADS# is sampled active by PCMC.
t12aa	A[18:3] Falling Edge Setup Time to HCLKIN Rising	3.2		79	Setup to HCLKIN Rising when ADS# is Sampled Active by PCMC.
t12ab	A[18:3] Rising Edge Setup Time to HCLKIN Rising	4.7		79	Setup to HCLKIN Rising when ADS# is Sampled Active by PCMC.
t12ac	A[18:3] Falling Edge Setup Time to HCLKIN Rising	4.1		79	Setup to HCLKIN Rising when ADS# is Sampled Active by PCMC.
t12b	A[31:0] Hold Time from HCLKIN Rising	0.5		79	Hold from HCLKIN rising two clocks after ADS# is sampled active by PCMC.
t12c	A[31:0] Setup Time to HCLKIN Rising	6.5		79	Setup to HCLKIN rising when EADS# is sampled active by the CPU.
t12d	A[31:0] Hold Time from HCLKIN Rising	1.5		79	Hold from HCLKIN rising when EADS# is sampled active by the CPU.
t12e	A[31:0] Output Enable from HCLKIN Rising	0	13	81	
t12f	A[31:0] Valid Delay from HCLKIN Rising	1.3	13	78	0 pF
t12g	A[31:0] Float Delay from HCLKIN Rising	0	13	80	

Functional Operating Range (V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C) (Continued)

Symbol	Parameter	Min	Max	Fig	Notes
t12h	A[2:0] Propagation Delay from BE[7:0]#	1	16	77	0 pF
t13a	BRDY# Rising Edge Valid Delay from HCLKIN Rising	2.1	7.9	78	0 pF
t13b	BRDY# Falling Edge Valid Delay from HCLKIN Rising	2.1	7.9	78	0 pF
t14	NA# Valid Delay from HCLKIN Rising	1.4	8.4	78	0 pF
t15a	AHOLD Valid Delay from HCLKIN Rising	2.0	7.6	78	0 pF
t15b	BOFF# Valid Delay from HCLKIN Rising	2.0	7.6	78	
t16a	EADS#, INV, PEN# Valid Delay from HCLKIN Rising	2.0	8.0	78	0 pF
t16b	CPURST Rising Edge Valid Delay from HCLKIN Rising	1.2	7.5	78	
t16c	CPURST Falling Edge Valid Delay from HCLKIN Rising	1.2	7.5	78	
t16d	KEN# Valid delay from HCLKIN Rising	1.7	8.2	78	
t17	INIT High Pulse Width	2 HCLKs		84	Soft reset via TRC register or CPU shutdown special cycle
t18	CPURST High Pulse Width	1 ms		84	Hard reset via TRC register, 0 pF

9.5.11 SECOND LEVEL CACHE STANDARD SRAM TIMING, 60 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t20a	CAA[6:3]/CAB[6:3] Propagation Delay from A[6:3]	0	8.5	77	0 pF
t20b	CAA[6:3]/CAB[6:3] Valid Delay from HCLKIN Rising	0	7.2	78	0 pF
t21a	COE[1:0]# Falling Edge Valid Delay from HCLKIN Rising	0	9	78	0 pF
t21b	COE[1:0]# Rising Edge Valid Delay from HCLKIN Rising	0	5.5	78	0 pF
t22a	CWE[7:0]#/CBS[7:0]# Falling Edge Valid Delay from HCLKIN Rising	2	14	78	CPU burst or single write to second level cache, 0 pF
t22b	CWE[7:0]#/CBS[7:0]# Rising Edge Valid Delay from HCLKIN Rising	3	15	78	CPU burst or single write to second level cache, 0 pF
t22c	CWE[7:0]#/CBS[7:0]# Valid Delay from HCLKIN Rising	1.4	7.7	78	Cache line Fill, 0 pF
t22d	CWE[7:0]#/CBS[7:0]# Low Pulse Width	1 HCLK		84	0 pF
t22e	CWE[7:0]#/CBS[7:0]# Driven High before CALE Driven High	−1		85	Last write to second level cache during cache line fill, 0 pF
t22f	CAA[4:3]/CAB[4:3] Valid before CWE[7:0]# Falling	1.5		85	CPU burst write to second level cache, 0 pF
t23	CALE Valid Delay from HCLKIN Rising	0	8	78	0 pF
t24	CR/W[1:0]# Valid Delay from HCLKIN Rising	1.5	8.2	78	0 pF
t25	CBS[1:0]# Valid Delay from HCLKIN Rising; Reads from Cache SRAMs	1.0	12.0	78	0 pF

9.5.12 SECOND LEVEL CACHE BURST SRAM TIMING, 60 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t30a	CAA[6:3]/CAB[6:3] Propagation Delay from A[6:3]	0	8.5	77	0 pF
t30b	CAA[6:3]/CAB[6:3] Valid Delay from HCLKIN Rising	0	8.2	78	0 pF
t31	CADS[1:0]# Valid Delay from HCLKIN Rising	1.5	8.2	78	0 pF
t32	CADV[1:0]# Valid Delay from HCLKIN Rising	1.5	8.2	78	0 pF
t33	CWE[7:0]# Valid Delay from HCLKIN Rising	1.0	10.5	78	0 pF
t34a	COE[1:0]# Falling Edge Valid Delay from HCLKIN Rising	0	9.5	78	0 pF
t34b	COE[1:0]# Rising Edge Valid Delay from HCLKIN Rising	0	6.0	78	0 pF
t35	CALE Valid Delay from HCLKIN Rising	0	8.5	78	0 pF

9.5.13 DRAM INTERFACE TIMING, 60 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t40a	RAS[5:0]# Valid Delay from HCLKIN Rising	0	8.0	78	50 pF
t40b	RAS[5:0]# Pulse Width High	4 HCLKs−5		84	RAS# precharge at beginning of page miss cycle, 50 pF
t41a	CAS[7:0]# Valid Delay from HCLKIN Rising	0	8.0	78	50 pF
t41b	CAS[7:0]# Pulse Width High	1 HCLK−5		84	CAS# precharge during burst cycles, 50 pF
t42	WE# Valid Delay from HCLKIN Rising	0	21	78	50 pF
t43a	MA[10:0] Propagation Delay from A[23:3]	0	23	77	50 pF
t43b	MA[10:0] Valid Delay from HCLKIN Rising	0	10.7	78	50 pF

9.5.14 PCI CLOCK TIMING, 60 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t50a	PCLKOUT High Time	13		82	20 pF
t50b	PCLKOUT Low Time	13		82	20 pF
t51a	PCLKIN High Time	12		82	
t51b	PCLKIN Low Time	12		82	
t51c	PCLKIN Rise Time		3	83	
t51d	PCLKIN Fall Time		3	83	

9.5.15 PCI INTERFACE TIMING, 60 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t60a	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Valid Delay from PCLKIN Rising	2	11	78	Min: 0 pF Max: 50 pF
t60b	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Output Enable Delay from PCLKIN Rising	2		81	
t60c	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Float Delay from PCLKIN Rising	2	28	80	
t60d	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Setup Time to PCLKIN Rising	9		79	
t60e	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Hold Time from PCLKIN Rising	0		79	
t61a	REQ#, MEMACK# Valid Delay from PCLKIN Rising	2	12	78	Min: 0 pF Max: 50 pF
t61b	REQ#, MEMACK# Output Enable Delay from PCLKIN Rising	2		81	
t61c	REQ#, MEMACK# Float Delay from PCLKIN Rising	2	28	80	
t62a	FLSHREQ#, MEMREQ# Setup Time to PCLKIN Rising	12		79	

Functional Operating Range (V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C) (Continued)

Symbol	Parameter	Min	Max	Fig	Notes
t62b	FLSHREQ#, MEMREQ# Hold Time from PCLKIN Rising	0		79	
t63a	GNT# Setup Time to PCLKIN Rising	10		79	
t63b	GNT# Hold Time from PCLKIN Rising	0		79	
t64a	MEMCS# Setup Time to PCLKIN Rising	7		79	
t64b	MEMCS# Hold Time from PCLKIN Rising	0		79	
t65	PCIRST# Low Pulse Width	1 ms		84	Hard Reset via TRC Register, 0 pF

9.5.16 LBX INTERFACE TIMING, 60 MHz (82434LX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t70	HIG[4:0] Valid Delay from HCLKIN Rising	0.8	6.7	78	0 pF
t71	MIG[2:0] Valid Delay from HCLKIN Rising	0.9	6.5	78	0 pF
t72	PIG[3:0] Valid Delay from PCLKIN Rising	1.5	12	78	0 pF
t73	PCIDRV Valid Delay from PCLKIN Rising	1	13	78	0 pF
t74a	MDLE Falling Edge Valid Delay from HCLKIN Rising	0.6	6.8	78	0 pF
t74b	MDLE Rising Edge Valid Delay from HCLKIN Rising	0.6	6.8	85	0 pF
t75a	EOL, PPOUT[1:0] Setup Time to PCLKIN Rising	7.7		79	
t75b	EOL, PPOUT[1:0] Hold Time from PCLKIN Rising	1.0		79	

9.6 82434NX AC Characteristics

The AC characteristics given in this section consist of propagation delays, valid delays, input setup requirements, input hold requirements, output float delays, output enable delays, output-to-output delays, pulse widths, clock high and low times and clock period specifications. Figure 77 through Figure 85 define these specifications. Output test loads are listed in the right column.

In Figure 77 through Figure 85, VT = 1.5V for the following signals:

A[31:0], BE[7:0]#, PEN#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, PCHK#, HITM#, EADS#, BRDY#, BOFF#, AHOLD, NA#, KEN#, INV, CACHE#, SMIACT#, INIT, CPURST, CALE, CADV[1:0]#, COE[1:0]#, CWE[7:0]#, CADS[1:0]#, CAA[6:3], CAB[6:3], WE#, RAS[5:0]#, CAS[7:0]#, MA[10:0], C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, GNT#, DEVSEL#, MEMREQ#, PAR, PERR#, SERR#, REQ#, MEMCS#, FLSHBUF#, MEMACK#, PWROK, HCLKIN, HCLKA–HCLKF, PCLKIN, PCLKOUT.

VT = 2.5V for the following signals:

PPOUT[1:0], EOL, HIG[4:0], PIG[3:0], MIG[2:0], DRVPCI, MDLE, PCIRST#

9.6.1 HOST CLOCK TIMING, 66 MHz (82434NX), PRELIMINARY

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t1a	HCLKOSC High Time	6.0		82	
t1b	HCLKOSC Low Time	5.0		82	
t2a	HCLKIN Period	15	20	82	
t2b	HCLKIN Period Stability		±100		ps(1)
t2c	HCLKIN High Time	4		82	
t2d	HCLKIN Low Time	4		82	
t2e	HCLKIN Rise Time		1.5	83	
t2f	HCLKIN Fall Time		1.5	83	
t3a	HCLKA–HCLKF Output-to-Output Skew		0.5	85	0 pF
t3b	HCLKA–HCLKF High Time	5.0		82	0 pF
t3c	HCLKA–HCLKF Low Time	5.0		82	0 pF

NOTES:
1. Measured on rising edge of adjacent clocks at 1.5V.

9.6.2 CPU INTERFACE TIMING, 66 MHz (82434NX), PRELIMINARY

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to + 85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t10a	ADS#, W/R#, Setup Time to HCLKIN Rising	4.6		79	
t10b	BE[7:0]# Setup Time to HCLKIN Rising	4.6		79	
t10c	HITM# Setup Time to HCLKIN Rising	6.4		79	
t10d	CACHE#, M/IO# Setup Time to HCLKIN Rising	4.6		79	
t10e	D/C# Setup Time to HCLKIN Rising	4.0		79	
t10f	HLOCK#, SMIACT#, Setup Time to HCLKIN Rising	4.0		79	
t10g	HITM#, M/IO#, D/C#, Hold Time from HCLKIN Rising	0.7		79	
t10h	W/R#, HLOCK#, Hold Time from HCLKIN Rising	0.8		79	
t10i	ADS#, BE[7:0]# Hold Time from HCLKIN Rising	1.1		79	
t10j	CACHE#, SMIACT# Hold Time from HCLKIN Rising	1.1		79	
t11a	PCHK# Setup Time to HCLKIN Rising	4.3		79	
t11b	PCHK# Hold Time from HCLKIN Rising	1.1		79	
t12a	A[31:0] Setup Time to HCLKIN Rising	2.7		79	Setup to HCLKIN rising when ADS# is sampled active by PCMC.
t12b	A[31:0] Hold Time from HCLKIN Rising	0.5			HOLD from HCLKIN Rising two clocks after ADS# is sampled active by PCMC
t12c	A[31:0] Setup Time to HCLKIN Rising	6.0		79	Setup to HCLKIN rising when EADS# is sampled active by the CPU.

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C) (Continued)

Symbol	Parameter	Min	Max	Fig	Notes
t12d	A[31:0] Hold Time from HCLKIN Rising	1.5		79	Hold from HCLKIN rising when EADS# is sampled active by the CPU.
t12e	A[31:0] Output Enable from HCLKIN Rising	0	13	81	
t12f	A[31:0] Valid Delay from HCLKIN Rising	1.3	13	78	0 pF
t12g	A[31:0] Float Delay from HCLKIN Rising	0	13	80	
t12h	A[2:0] Propagation Delay from BE[7:0]#	1.0	16	77	0 pF
t13a	BRDY# Rising Edge Valid Delay from HCLKIN Rising	1.6	7.5	78	0 pF
t13b	BRDY# Falling Edge Valid Delay from HCLKIN Rising	1.6	7.5	78	0 pF
t14	NA# Valid Delay from HCLKIN Rising	.9	7.6	78	0 pF
t15a	AHOLD Valid Delay from HCLKIN Rising	1.5	7.0	78	0 pF
t15b	BOFF# Valid Delay from HCLKIN Rising	1.5	7.0	78	0 pF
t16a	EADS#, INV, PEN# Valid Delay from HCLKIN Rising	1.5	7.5	78	0 pF
t16b	CPURST Rising Edge Valid Delay from HCLKIN Rising	1.2	7.0	78	0 pF
t16c	CPURST Falling Edge Valid Delay from HCLKIN Rising	1.2	7.0	78	0 pF
t16d	KEN# Valid delay from HCLKIN Rising	1.5	7.5	78	0 pF
t17	INIT High Pulse Width	2 HCLKs		84	0 pF
t18	CPURST High Pulse Width	1 ms		84	0 pF; Hard reset via TRC register

9.6.3 SECOND LEVEL CACHE STANDARD SRAM TIMING, 66 MHz (82434NX), PRELIMINARY

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t20a	CAA[6:3]/CAB[6:3] Propagation Delay from A[6:3]	0	8.5	77	0 pF
t20b	CAA[6:3]/CAB[6:3] Valid Delay from HCLKIN Rising	0	7.2	78	0 pF
t21a	COE[1:0]# Falling Edge Valid Delay from HCLKIN Rising	0	9	78	0 pF
t21b	COE[1:0]# Rising Edge Valid Delay from HCLKIN Rising	0	5.5	78	0 pF
t22a	CWE[7:0]#/CBS[7:0]# Falling Edge Valid Delay from HCLKIN Rising	2	14	78	CPU burst or single write to second level cache, 0 pF
t22b	CWE[7:0]#/CBS[7:0]# Rising Edge Valid Delay from HCLKIN Rising	3	14	78	CPU burst or single write to second level cache, 0 pF
t22c	CWE[7:0]#/CBS[7:0]# Valid Delay from HCLKIN Rising	1.0	7.7	78	Cache line Fill, 0 pF
t22d	CWE[7:0]#/CBS[7:0]# Low Pulse Width	1 HCLK		84	0 pF
t22e	CWE[7:0]#/CBS[7:0]# Driven High before CALE Driven High	−1		85	Last write to second level cache during cache line fill, 0 pF
t22f	CAA[4:3]/CAB[4:3] Valid before CWE[7:0]# Falling	1.5		85	CPU burst write to second level cache, 0 pF
t23	CALE Valid Delay from HCLKIN Rising	0	8.0	78	0 pF
t24	CR/W[1:0]# Valid Delay from HCLKIN Rising	1.5	8.2	78	0 pF
t25	CBS[1:0]# Valid Delay from HCLKIN Rising; Reads from Cache SRAMs	1.0	12.0	78	0 pF
t26a	CCS[1:0]# Propagation Delay from ADS# Falling		7.0	77	0 pF; First access after powerdown
t26b	CCS[1:0]# Valid Delay from HCLKIN Rising	1.5	8.2	78	0 pF; Entering powerdown

9.6.4 SECOND LEVEL CACHE BURST SRAM TIMING, 66 MHz (82434NX), PRELIMINARY

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t30a	CAA[6:3]/CAB[6:3] Propagation Delay from A[6:3]	0	8.5	77	0 pF
t30b	CAA[6:3]/CAB[6:3] Valid Delay from HCLKIN Rising	0	8.2	78	0 pF
t31	CADS[1:0]# Valid Delay from HCLKIN Rising	1.5	8.0	78	0 pF
t32	CADV[1:0]# Valid Delay from HCLKIN Rising	1.5	8.0	78	0 pF
t33	CWE[7:0]# Valid Delay from HCLKIN Rising	1.5	9.0	78	0 pF
t34a	COE[1:0]# Falling Edge Valid Delay from HCLKIN Rising	0.5	9.0	78	0 pF
t34b	COE[1:0]# Rising Edge Valid Delay from HCLKIN Rising	0.5	6.0	78	0 pF
t35	CALE Valid Delay from HCLKIN Rising	0	8.0	78	0 pF

9.6.5 DRAM INTERFACE TIMING, 66 MHz (82434NX), PRELIMINARY

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t40a	RAS[7:0]# Valid Delay from HCLKIN Rising	0	8.0	78	50 pF
t40b	RAS[7:0]# Pulse Width High	4 HCLKs−5		84	RAS# precharge at beginning of page miss cycle, 50 pF
t41a	CAS[7:0]# Valid Delay from HCLKIN Rising	0	8.0	78	50 pF
t41b	CAS[7:0]# Pulse Width High	1 HCLKIN−5		84	CAS# precharge during burst cycles, 50 pF
t42	WE# Valid Delay from HCLKIN Rising	0	21	78	50 pF
t43a	MA[10:0] Propagation Delay from A[23:3]	0	23	77	50 pF
t43b	MA[10:0] Valid Delay from HCLKIN Rising	0	10.7	78	50 pF
t43c	MA11 Propagation Delay from A[25:24]	0	28.0	77	50 pF
t43d	MA11 Valid Delay from HCLKIN Rising	0	12	78	50 pF

9.6.6 PCI CLOCK TIMING, 66 MHz (82434NX), PRELIMINARY

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t50a	PCLKOUT High Time	13		82	20 pF
t50b	PCLKOUT Low Time	13		82	20 pF
t51a	PCLKIN High Time	12		82	
t51b	PCLKIN Low Time	12		82	
t51c	PCLKIN Rise Time		3	83	
t51d	PCLKIN Fall Time		3	83	

9.6.7 PCI INTERFACE TIMING, 66 MHz (82434NX), PRELIMINARY

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t60a	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Valid Delay from PCLKIN Rising	2	11	78	Min: 0 pF Max: 50 pF
t60b	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Output Enable Delay from PCLKIN Rising	2		81	
t60c	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Float Delay from PCLKIN Rising	2	28	80	
t60d	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Setup Time to PCLKIN Rising	7		79	
t60e	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Hold Time from PCLKIN Rising	0		79	
t61a	REQ#, MEMACK# Valid Delay from PCLKIN Rising	2	12	78	Min: 0 pF Max: 50 pF
t61b	REQ#, MEMACK# Output Enable Delay from PCLKIN Rising	2		81	
t61c	REQ#, MEMACK# Float Delay from PCLKIN Rising	2	28	80	
t62a	FLSHREQ#, MEMREQ# Setup Time to PCLKIN Rising	12		79	
t62b	FLSHREQ#, MEMREQ# Hold Time from PCLKIN Rising	0		79	

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C) (Continued)

Symbol	Parameter	Min	Max	Fig	Notes
t63a	GNT# Setup Time to PCLKIN Rising	10		79	
t63b	GNT# Hold Time from PCLKIN Rising	0		79	
t64a	MEMCS# Setup Time to PCLKIN Rising	7		79	
t64b	MEMCS# Hold Time from PCLKIN Rising	0		79	
t65	PCIRST# Low Pulse Width	1 ms		84	Hard Reset via TRC Register,0 pF

1

9.6.8 LBX INTERFACE TIMING, 66 MHz (82434NX), PRELIMINARY

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t70	HIG[4:0] Valid Delay from HCLKIN Rising	0.8	6.5	78	0 pF
t71	MIG[2:0] Valid Delay from HCLKIN Rising	0.9	6.5	78	0 pF
t72	PIG[3:0] Valid Delay from PCLKIN Rising	1.5	12	78	0 pF
t73	PCIDRV Valid Delay from PCLKIN Rising	1	13	78	0 pF
t74a	MDLE Falling Edge Valid Delay from HCLKIN Rising	0.6	6.0	78	0 pF
t74b	MDLE Rising Edge Valid from HCLKIN Rising	0.6	6.0	85	0 pF
t75a	EOL, PPOUT[1:0] Setup Time to PCLKIN Rising	7.7		79	
t75b	EOL, PPOUT[1:0] Hold Time from PCLKIN Rising	1.0		79	

9.6.9 HOST CLOCK TIMING, 50 and 60 MHz (82434NX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t1a	HCLKOSC High Time	6.0		82	
t1b	HCLKOSC Low Time	5.0		82	
t2a	HCLKIN Period	16.66	20	82	
t2b	HCLKIN Period Stability		±100		ps(1)
t2c	HCLKIN High Time	4		82	
t2d	HCLKIN Low Time	4		82	
t2e	HCLKIN Rise Time		1.5	83	
t2f	HCLKIN Fall Time		1.5	83	
t3a	HCLKA–HCLKF Output-to-Output Skew		0.5	85	0 pF
t3b	HCLKA–HCLKF High Time	5.0		82	0 pF
t3c	HCLKA–HCLKF Low Time	5.0		82	0 pF

NOTES:
1. Measured on rising edge of adjacent clocks at 1.5V.

9.6.10 CPU INTERFACE TIMING, 50 AND 60 MHz (82434NX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t10a	ADS#, W/R#, Setup Time to HCLKIN Rising	4.6		79	
t10b	BE[7:0]# Setup Time to HCLKIN Rising	4.6		79	
t10c	HITM# Setup Time to HCLKIN Rising	6.8		79	
t10d	CACHE#, M/IO# Setup Time to HCLKIN Rising	4.6		79	
t10e	D/C# Setup Time to HCLKIN Rising	4.6		79	
t10f	HLOCK#, SMIACT#, Setup Time to HCLKIN Rising	4.6		79	
t10g	HITM#, M/IO#, D/C#, Hold Time from HCLKIN Rising	0.7		79	
t10h	W/R#, HLOCK# Hold from HCLKIN Rising	0.8		79	
t10i	ADS#, BE[7:0]# Hold Time from HCLKIN Rising	0.9		79	
t10j	CACHE#, SMIACT# Hold Time from HCLKIN Rising	1.1		79	
t11a	PCHK# Setup Time to HCLKIN Rising	4.3		79	
t11b	PCHK# Hold Time from HCLKIN Rising	1.1		79	
t12a	A[31:0] Setup Time to HCLKIN Rising	3.0		79	Setup to HCLKIN rising when ADS# is sampled active by PCMC.
t12b	A[31:0] Hold Time from HCLKIN Rising	0.5		79	HOLD from HCLKIN Rising two clocks after ADS# is sampled active by PCMC
t12c	A[31:0] Setup Time to HCLKIN Rising	6.5		79	Setup to HCLKIN rising when EADS# is sampled active by the CPU.
t12d	A[31:0] Hold Time from HCLKIN Rising	1.5		79	Hold from HCLKIN rising when EADS# is sampled active by the CPU.

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C) (Continued)

Symbol	Parameter	Min	Max	Fig	Notes
t12e	A[31:0] Output Enable from HCLKIN Rising	0	13	81	
t12f	A[31:0] Valid Delay from HCLKIN Rising	1.3	13	78	0 pF
t12g	A[31:0] Float Delay from HCLKIN Rising	0	13	80	
t12h	A[2:0] Propagation Delay from BE[7:0]#	1.0	16	77	0 pF
t13a	BRDY# Rising Edge Valid Delay from HCLKIN Rising	2.1	7.9	78	0 pF
t13b	BRDY# Falling Edge Valid Delay from HCLKIN Rising	2.1	7.9	78	0 pF
t14	NA# Valid Delay from HCLKIN Rising	1.4	8.4	78	0 pF
t15a	AHOLD Valid Delay from HCLKIN Rising	2.0	7.6	78	0 pF
t15b	BOFF# Valid Delay from HCLKIN Rising	2.0	7.6	78	0 pF
t16a	EADS#, INV, PEN# Valid Delay from HCLKIN Rising	2.0	8.0	78	0 pF
t16b	CPURST Rising Edge Valid Delay from HCLKIN Rising	1.2	7.5	78	0 pF
t16c	CPURST Falling Edge Valid Delay from HCLKIN Rising	1.2	7.5	78	0 pF
t16d	KEN# Valid delay from HCLKIN Rising	1.7	8.2	78	0 pF
t17	INIT High Pulse Width	2 HCLKs		84	0 pF
t18	CPURST High Pulse Width	1 ms		84	0 pF; Hard reset via TRC register

9.6.11 SECOND LEVEL CACHE STANDARD SRAM TIMING, 50 AND 60 MHz (82434NX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t20a	CAA[6:3]/CAB[6:3] Propagation Delay from A[6:3]	0	8.5	77	0 pF
t20b	CAA[6:3]/CAB[6:3] Valid Delay from HCLKIN Rising	0	7.2	78	0 pF
t21a	COE[1:0]# Falling Edge Valid Delay from HCLKIN Rising	0	9.0	78	0 pF
t21b	COE[1:0]# Rising Edge Valid Delay from HCLKIN Rising	0	5.5	78	0 pF
t22a	CWE[7:0]#/CBS[7:0]# Falling Edge Valid Delay from HCLKIN Rising	2	14	78	CPU burst or single write to second level cache, 0 pF
t22b	CWE[7:0]#/CBS[7:0]# Rising Edge Valid Delay from HCLKIN Rising	3	15	78	CPU burst or single write to second level cache, 0 pF
t22c	CWE[7:0]#/CBS[7:0]# Valid Delay from HCLKIN Rising	1.4	7.7	78	Cache line Fill, 0 pF
t22d	CWE[7:0]#/CBS[7:0]# Low Pulse Width	14		84	0 pF
t22e	CWE[7:0]#/CBS[7:0]# Driven High before CALE Driven High	-1		85	Last write to second level cache during cache line fill, 0 pF
t22f	CAA[4:3]/CAB[4:3] Valid before CWE[7:0]# Falling	1.5		85	CPU burst write to second level cache, 0 pF
t23	CALE Valid Delay from HCLKIN Rising	0	8	78	0 pF
t24	CR/W[1:0]# Valid Delay from HCLKIN Rising	1.5	8.2	78	0 pF
t25	CBS[1:0]# Valid Delay from HCLKIN Rising; Reads from Cache SRAMs	1.0	12.0	78	0 pF
t26a	CCS[1:0]# Propagation Delay from ADS# Falling		7.0	77	0 pF; First access after powerdown
t26b	CCS[1:0]# Valid Delay from HCLKIN Rising	1.5	8.2	78	0 pF; Entering powerdown

9.6.12 SECOND LEVEL CACHE BURST SRAM TIMING, 50 AND 60 MHz (82434NX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t30a	CAA[6:3]/CAB[6:3] Propagation Delay from A[6:3]	0	8.5	77	0 pF
t30b	CAA[6:3]/CAB[6:3] Valid Delay from HCLKIN Rising	0	8.2	78	0 pF
t31	CADS[1:0]# Valid Delay from HCLKIN Rising	1.5	8.2	78	0 pF
t32	CADV[1:0]# Valid Delay from HCLKIN Rising	1.5	8.2	78	0 pF
t33	CWE[7:0]# Valid Delay from HCLKIN Rising	1.0	10.5	78	0 pF
t34a	COE[1:0]# Falling Edge Valid Delay from HCLKIN Rising	0	9.5	78	0 pF
t34b	COE[1:0]# Rising Edge Valid Delay from HCLKIN Rising	0	6.0	78	0 pF
t35	CALE Valid Delay from HCLKIN Rising	0	8.5	78	0 pF

9.6.13 DRAM INTERFACE TIMING, 50 AND 60 MHz (82434NX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t40a	RAS[7:0]# Valid Delay from HCLKIN Rising	0	8.0	78	50 pF
t40b	RAS[7:0]# Pulse Width High	4 HCLKs–5		84	RAS# precharge at beginning of page miss cycle, 50 pF
t41a	CAS[7:0]# Valid Delay from HCLKIN Rising	0	8.0	78	50 pF
t41b	CAS[7:0]# Pulse Width High	1 HCLK–5		84	CAS# precharge during burst cycles, 50 pF
t42	WE# Valid Delay from HCLKIN Rising	0	21	78	50 pF
t43a	MA[10:0] Propagation Delay from A[23:3]	0	23	77	50 pF
t43b	MA[10:0] Valid Delay from HCLKIN Rising	0	10.7	78	50 pF
t43c	MA11 Propagation Delay from A[25:24]	0	24.3	77	50 pF
t43d	MA11 Valid Delay from HCLKIN Rising	0	12	78	50 pF

9.6.14 PCI CLOCK TIMING, 50 AND 60 MHz (82434NX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t50a	PCLKOUT High Time	13		82	20 pF
t50b	PCLKOUT Low Time	13		82	20 pF
t51a	PCLKIN High Time	12		82	
t51b	PCLKIN Low Time	12		82	
t51c	PCLKIN Rise Time		3	83	
t51d	PCLKIN Fall Time		3	83	

9.6.15 PCI INTERFACE TIMING, 50 AND 60 MHz (82434NX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t60a	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Valid Delay from PCLKIN Rising	2	11	78	Min: 0 pF Max: 50 pF
t60b	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Output Enable Delay from PCLKIN Rising	2		81	
t60c	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Float Delay from PCLKIN Rising	2	28	80	
t60d	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Setup Time to PCLKIN Rising	9		79	
t60e	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, PERR#, SERR#, DEVSEL# Hold Time from PCLKIN Rising	0		79	
t61a	REQ#, MEMACK# Valid Delay from PCLKIN Rising	2	12	78	Min: 0 pF Max: 50 pF
t61b	REQ#, MEMACK# Output Enable Delay from PCLKIN Rising	2		81	
t61c	REQ#, MEMACK# Float Delay from PCLKIN Rising	2	28	80	
t62a	FLSHREQ#, MEMREQ# Setup Time to PCLKIN Rising	12		79	
t62b	FLSHREQ#, MEMREQ# Hold Time from PCLKIN Rising	0		79	
t63a	GNT# Setup Time to PCLKIN Rising	10		79	
t63b	GNT# Hold Time from PCLKIN Rising	0		79	
t64a	MEMCS# Setup Time to PCLKIN Rising	7		79	
t64b	MEMCS# Hold Time from PCLKIN Rising	0		79	
t65	PCIRST# Low Pulse Width	1 ms		84	Hard Reset via TRC Register, 0 pF

9.6.16 LBX INTERFACE TIMING, 50 AND 60 MHz (82434NX)

Functional Operating Range (V_{CC} = 4.75V to 5.25V; $V_{CC}3$ = 3.135V to 3.465V; T_{CASE} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Fig	Notes
t70	HIG[4:0] Valid Delay from HCLKIN Rising	0.8	6.7	78	0 pF
t71	MIG[2:0] Valid Delay from HCLKIN Rising	0.9	6.5	78	0 pF
t72	PIG[3:0] Valid Delay from PCLKIN Rising	1.5	12	78	0 pF
t73	PCIDRV Valid Delay from PCLKIN Rising	1	13	78	0 pF
t74a	MDLE Falling Edge Valid Delay from HCLKIN Rising	0.6	6.8	78	0 pF
t74b	MDLE Rising Edge Valid Delay from HCLKIN Rising	0.6	6.8	85	0 pF
t75a	EOL, PPOUT[1:0] Setup Time to PCLKIN Rising	7.7		79	
t75b	EOL, PPOUT[1:0] Hold Time from PCLKIN Rising	1.0		79	

1

9.6.17 TIMING DIAGRAMS

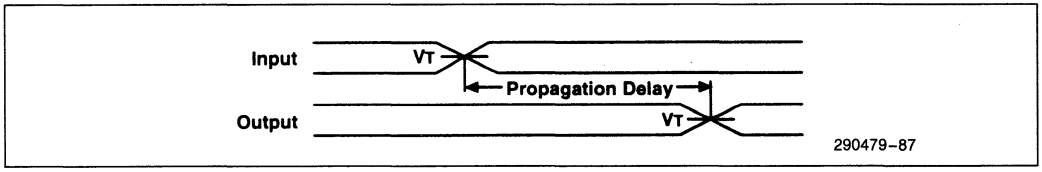


Figure 77. Propagation Delay

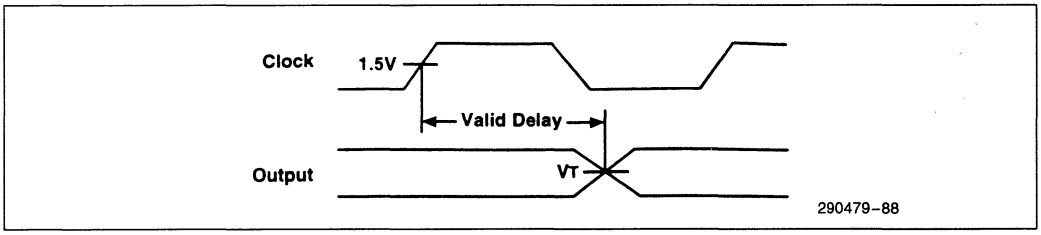


Figure 78. Valid Delay from Rising Clock Edge

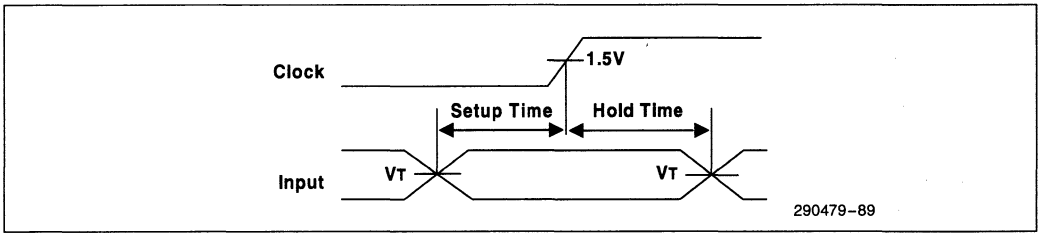


Figure 79. Setup and Hold Times

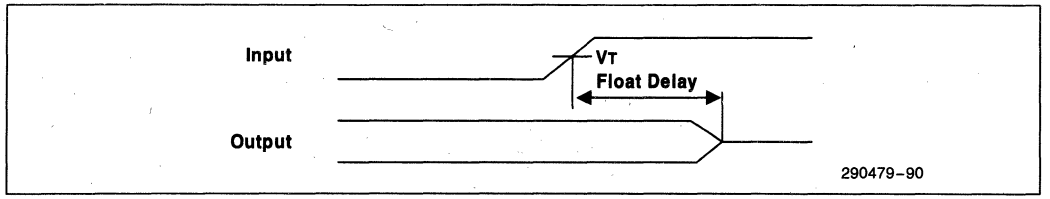


Figure 80. Float Delay

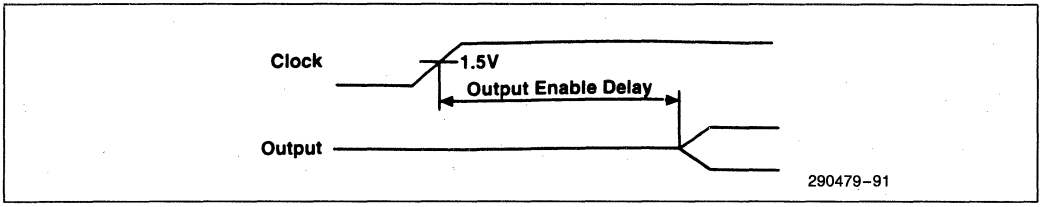


Figure 81. Output Enable Delay

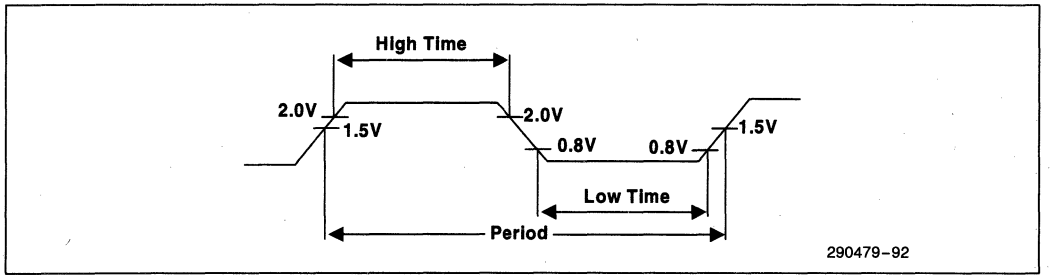


Figure 82. Clock High and Low Times and Period

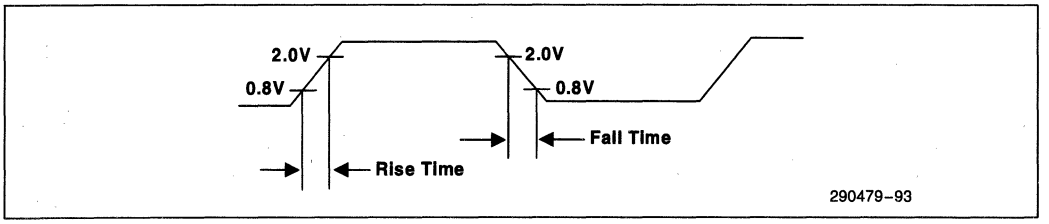


Figure 83. Clock Rise and Fall Times

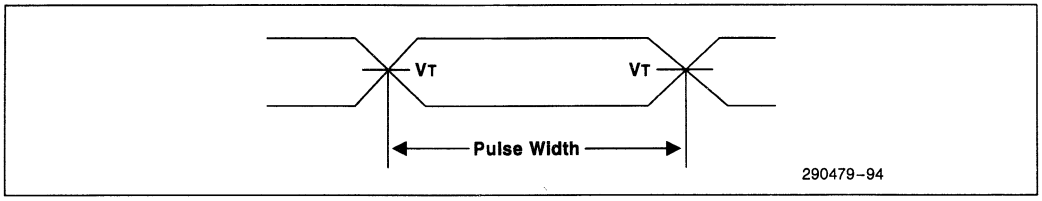


Figure 84. Pulse Width

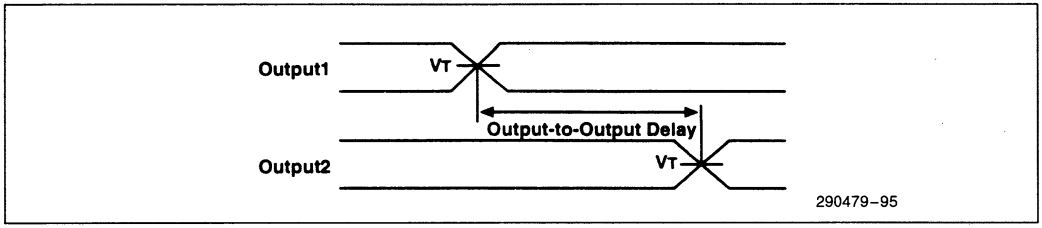
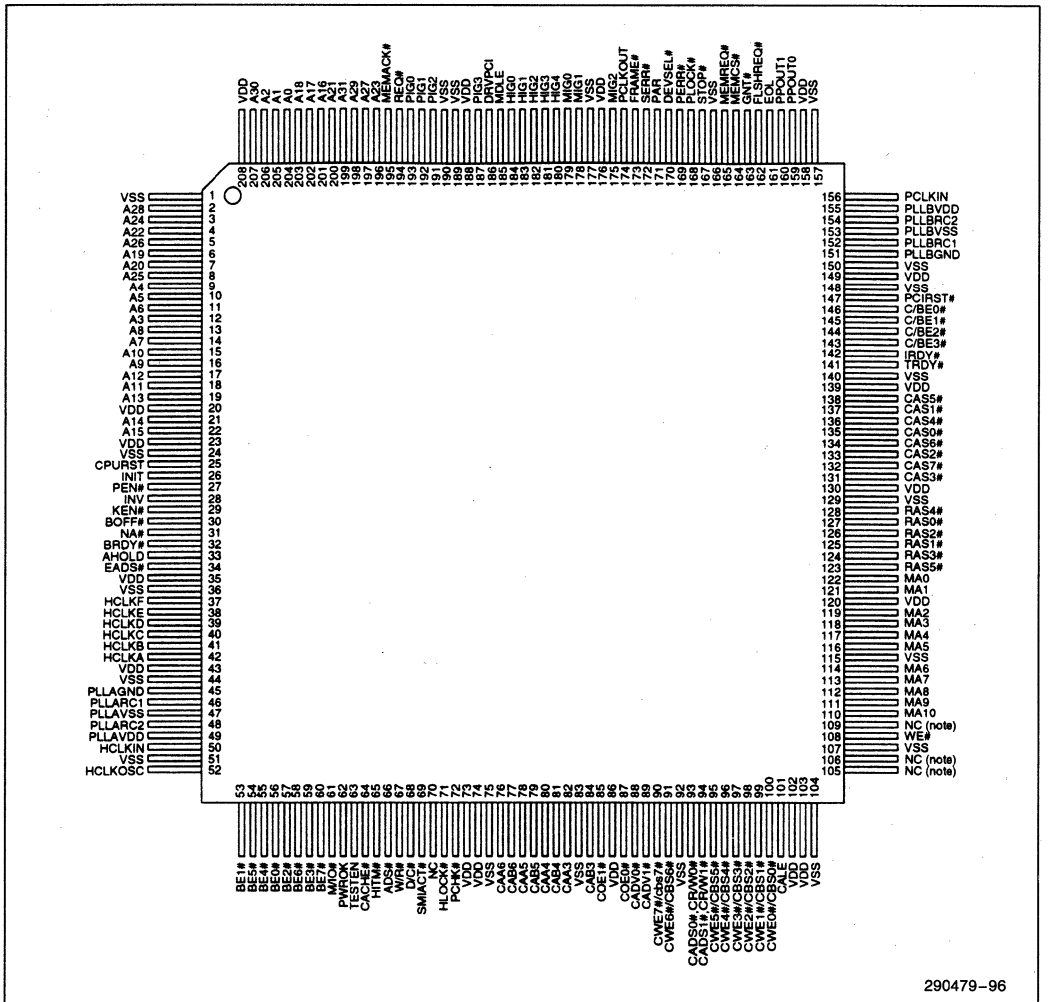


Figure 85. Output-to-Output Delay

10.0 PINOUT AND PACKAGE INFORMATION

10.1 Pin Assignment

Except for the pins listed in Figure 86 notes, the pin assignment for the 82434LX and 82434NX are the same.



NOTES:

1. For the 82434NX, pin 105 = RAS6#, 106 = RAS7#, and 109 = MA11. These pins are no connects for the 82434LX and are signal connections for the 82434NX.
2. For the 82434NX, pins 23, 35, 43, 74, 86, and 102 are 3.3V VDD pins (i.e., VDD3). These pins are VDD pins for the 82434LX.

Figure 86. PCMC Pin Assignment

Table 21. 82434LX Alphabetical Pin Assignment

Pin Name	Pin #	Type
A0	204	t/s
A1	205	t/s
A2	206	t/s
A3	12	t/s
A4	9	t/s
A5	10	t/s
A6	11	t/s
A7	14	t/s
A8	13	t/s
A9	16	t/s
A10	15	t/s
A11	18	t/s
A12	17	t/s
A13	19	t/s
A14	21	t/s
A15	22	t/s
A16	201	t/s
A17	202	t/s
A18	203	t/s
A19	6	t/s
A20	7	t/s
A21	200	t/s
A22	4	t/s
A23	196	t/s
A24	3	t/s
A25	8	t/s
A26	5	t/s
A27	197	t/s
A28	2	t/s
A29	198	t/s
A30	207	t/s
A31	199	t/s
ADS#	66	in
AHOLD	33	out
BE0#	56	in
BE1#	53	in
BE2#	57	in
BE3#	59	in
BE4#	55	in
BE5#	54	in
BE6#	58	in
BE7#	60	in
BOFF#	30	out
BRDY#	32	out
CAA3	82	out
CAA4	80	out
CAA5	78	out
CAA6	76	out
CAB3	84	out
CAB4	81	out
CAB5	79	out
CAB6	77	out
CACHE#	64	in
CADS0#,CR/W0#	93	out
CADS1#,CR/W1#	94	out
CADV0# (82434LX) CADV0#/CCS0# (82434NX)	88	out
CADV1# (82434LX) CADV1#/CCS1# (82434NX)	89	out
CALE	101	out
CAS0#	135	out
CAS1#	137	out
CAS2#	133	out
CAS3#	131	out
CAS4#	136	out
CAS5#	138	out
CAS6#	134	out
CAS7#	132	out
CBE0#	146	t/s
CBE1#	145	t/s
CBE2#	144	t/s
CBE3#	143	t/s
COE0#	87	out
COE1#	85	out
CPURST	25	out
CWE0#/CBS0#	100	out
CWE1#/CBS1#	99	out
CWE2#/CBS2#	98	out
CWE3#/CBS3#	97	out
CWE4#/CBS4#	96	out
CWE5#/CBS5#	95	out
CWE6#/CBS6#	91	out
CWE7#/CBS7#	90	out
D/C#	68	in
DEVSEL#	170	s/t/s
DRVPCI	186	out
EADS#	34	out
EOL	161	in
FLSHREQ#	162	in
FRAME#	173	s/t/s
GNT#	163	in
HCLKA	42	out
HCLKB	41	out
HCLKC	40	out
HCLKD	39	out
HCLKE	38	out
HCLKF	37	out
HCLKIN	50	in

Table 21. 82434LX Alphabetical Pin Assignment (Continued)

Pin Name	Pin #	Type
HCLKOSC	52	in
HIG0	184	out
HIG1	183	out
HIG2	182	out
HIG3	181	out
HIG4	180	out
HITM#	65	in
HLOCK#	71	in
INIT	26	out
INV	28	out
IRDY#	142	s/t/s
KEN#	29	out
M/IO#	61	in
MA0	122	out
MA1	121	out
MA2	119	out
MA3	118	out
MA4	117	out
MA5	116	out
MA6	114	out
MA7	113	out
MA8	112	out
MA9	111	out
MA10	110	out
MA11 (82434NX only)	109	out
MDLE	185	out
MEMACK#	195	out
MEMCS#	164	in
MEMREQ#	165	in
MIG0	179	out
MIG1	178	out
MIG2	175	out
NA#	31	out
NC	70	NC
NC (82434LX only)	105	NC
NC (82434LX only)	106	NC
NC (82434LX only)	109	NC
PAR	171	t/s
PCHK#	72	in
PCIRST#	147	out
PCLKIN	156	in
PCLKOUT	174	out
PEN#	27	out
PERR#	169	s/o/d
PIG0	193	out
PIG1	192	out
PIG2	191	out
PIG3	187	out
PLLAGND	45	V
PLLARC1	46	in
PLLARC2	48	in
PLLAVDD	49	V
PLLAVSS	47	V
PLLBGND	151	V
PLLBRC1	152	in
PLLBRC2	154	in
PLLBVDD	155	V
PLLBVSS	153	V
PLOCK#	168	s/t/s
PPOUT0	159	in
PPOUT1	160	in
PWROK	62	in
RAS0#	127	out
RAS1#	125	out
RAS2#	126	out
RAS3#	124	out
RAS4#	128	out
RAS5#	123	out
RAS6# (82434NX only)	105	out
RAS7# (82434NX only)	106	out

Table 21. 82434LX Alphabetical Pin Assignment (Continued)

Pin Name	Pin #	Type
REQ#	194	out
SERR#	172	s/o/d
SMIACT#	69	in
STOP#	167	s/t/s
TESTEN	63	in
TRDY#	141	s/t/s
V_{DD}	20	V
V_{DD} (82434LX) V_{DD3} (82434NX)	23	V
V_{DD} (82434LX) V_{DD3} (82434NX)	35	V
V_{DD} (82434LX) V_{DD3} (82434NX)	43	V
V_{DD}	73	V
V_{DD} (82434LX) V_{DD3} (82434NX)	74	V
V_{DD} (82434LX) V_{DD3} (82434NX)	86	V
V_{DD} (82434LX) V_{DD3} (82434NX)	102	V

Pin Name	Pin #	Type
V_{DD}	103	V
V_{DD}	120	V
V_{DD}	130	V
V_{DD}	139	V
V_{DD}	149	V
V_{DD}	158	V
V_{DD}	176	V
V_{DD}	188	V
V_{DD}	208	V
V_{SS}	1	V
V_{SS}	24	V
V_{SS}	36	V
V_{SS}	44	V
V_{SS}	51	V
V_{SS}	75	V
V_{SS}	83	V

Pin Name	Pin #	Type
V_{SS}	92	V
V_{SS}	104	V
V_{SS}	107	V
V_{SS}	115	V
V_{SS}	129	V
V_{SS}	140	V
V_{SS}	148	V
V_{SS}	150	V
V_{SS}	157	V
V_{SS}	166	V
V_{SS}	177	V
V_{SS}	189	V
V_{SS}	190	V
W/R#	67	in
WE#	108	out

Table 22. Numerical Pin Assignment

Pin #	Pin Name	Type
1	V_{SS}	V
2	A28	t/s
3	A24	t/s
4	A22	t/s
5	A26	t/s
6	A19	t/s
7	A20	t/s
8	A25	t/s
9	A4	t/s
10	A5	t/s
11	A6	t/s
12	A3	t/s
13	A8	t/s
14	A7	t/s
15	A10	t/s
16	A9	t/s
17	A12	t/s
18	A11	t/s
19	A13	t/s
20	V_{DD}	V
21	A14	t/s
22	A15	t/s
23	V_{DD} (82434LX) V_{DD3} (82434NX)	V
24	V_{SS}	V
25	CPURST	out
26	INIT	out
27	PEN#	out
28	INV	out
29	KEN#	out
30	BOFF#	out
31	NA#	out
32	BRDY#	out
33	AHOLD	out
34	EADS#	out
35	V_{DD} (82434LX) V_{DD3} (82434NX)	V
36	V_{SS}	V
37	HCLKF	out
38	HCLKE	out
39	HCLKD	out
40	HCLKC	out
41	HCLKB	out
42	HCLKA	out
43	V_{DD} (82434LX) V_{DD3} (82434NX)	V
44	V_{SS}	V
45	PLLAGND	V
46	PLLARC1	in
47	PLLAVSS	V
48	PLLARC2	in
49	PLLAVDD	V
50	HCLKIN	in
51	V_{SS}	V
52	HCLKOSC	in
53	BE1#	in
54	BE5#	in
55	BE4#	in
56	BE0#	in
57	BE2#	in
58	BE6#	in
59	BE3#	in
60	BE7#	in
61	M/IO#	in
62	PWROK	in
63	TESTEN	in
64	CACHE#	in
65	HITM#	in
66	ADS#	in
67	W/R#	in
68	D/C#	in
69	SMIACT#	in
70	NC	NC
71	HLOCK#	in
72	PCHK#	in
73	V_{DD}	V
74	V_{DD} (82434LX) V_{DD3} (82434NX)	V
75	V_{SS}	V
76	CAA6	out
77	CAB6	out
78	CAA5	out
79	CAB5	out
80	CAA4	out
81	CAB4	out
82	CAA3	out
83	V_{SS}	V
84	CAB3	out
85	COE1#	out
86	V_{DD} (82434LX) V_{DD3} (82434NX)	V
87	COE0#	out
88	CADV0# (82434LX) CADV0#/CCS0# (82434NX)	out
89	CADV1# (82434LX) CADV1#/CCS1# (82434NX)	out

Table 22. Numerical Pin Assignment (Continued)

Pin #	Pin Name	Type
90	CWE7#/CBS7#	out
91	CWE6#/CBS6#	out
92	V_{SS}	V
93	CADS0#,CR/W0#	out
94	CADS1#,CR/W1#	out
95	CWE5#/CBS5#	out
96	CWE4#/CBS4#	out
97	CWE3#/CBS3#	out
98	CWE2#/CBS2#	out
99	CWE1#/CBS1#	out
100	CWE0#/CBS0#	out
101	CALE	out
102	V_{DD} (82434LX) V_{DD3} (82434NX)	V
103	V_{DD}	V
104	V_{SS}	V
105	NC (82434LX) RAS6# (82434NX)	NC out
106	NC (82434LX) RAS7# (82434NX)	NC out
107	V_{SS}	V
108	WE#	out
109	NC (82434LX) MA11 (82434NX)	NC out
110	MA10	out
111	MA9	out
112	MA8	out
113	MA7	out
114	MA6	out
115	V_{SS}	V
116	MA5	out
117	MA4	out
118	MA3	out

Pin #	Pin Name	Type
119	MA2	out
120	V_{DD}	V
121	MA1	out
122	MA0	out
123	RAS5#	out
124	RAS3#	out
125	RAS1#	out
126	RAS2#	out
127	RAS0#	out
128	RAS4#	out
129	V_{SS}	V
130	V_{DD}	V
131	CAS3#	out
132	CAS7#	out
133	CAS2#	out
134	CAS6#	out
135	CAS0#	out
136	CAS4#	out
137	CAS1#	out
138	CAS5#	out
139	V_{DD}	V
140	V_{SS}	V
141	TRDY#	s/t/s
142	IRDY#	s/t/s
143	CBE3#	t/s
144	CBE2#	t/s
145	CBE1#	t/s
146	CBE0#	t/s
147	PCIRST#	out
148	V_{SS}	V
149	V_{DD}	V
150	V_{SS}	V

Pin #	Pin Name	Type
151	PLLBGND	V
152	PLLBRC1	in
153	PLLBVSS	V
154	PLLBRC2	in
155	PLLBVDD	V
156	PCLKIN	in
157	V_{SS}	V
158	V_{DD}	V
159	PPOUT0	in
160	PPOUT1	in
161	EOL	in
162	FLSHREQ#	in
163	GNT#	in
164	MEMCS#	in
165	MEMREQ#	in
166	V_{SS}	V
167	STOP#	s/t/s
168	PLOCK#	s/t/s
169	PERR#	s/o/d
170	DEVSEL#	s/t/s
171	PAR	t/s
172	SERR#	s/o/d
173	FRAME#	s/t/s
174	PCLKOUT	out
175	MIG2	out
176	V_{DD}	V
177	V_{SS}	V
178	MIG1	out
179	MIG0	out
180	HIG4	out
181	HIG3	out
182	HIG2	out

Table 22. Numerical Pin Assignment (Continued)

Pin #	Pin Name	Type
183	HIG1	out
184	HIG0	out
185	MDLE	out
186	DRVPCI	out
187	PIG3	out
188	V_{DD}	V
189	V_{SS}	V
190	V_{SS}	V
191	PIG2	out

Pin #	Pin Name	Type
192	PIG1	out
193	PIG0	out
194	REQ#	out
195	MEMACK#	out
196	A23	t/s
197	A27	t/s
198	A29	t/s
199	A31	t/s
200	A21	t/s

Pin #	Pin Name	Type
201	A16	t/s
202	A17	t/s
203	A18	t/s
204	A0	t/s
205	A1	t/s
206	A2	t/s
207	A30	t/s
208	V_{DD}	V

10.2 Package Characteristics

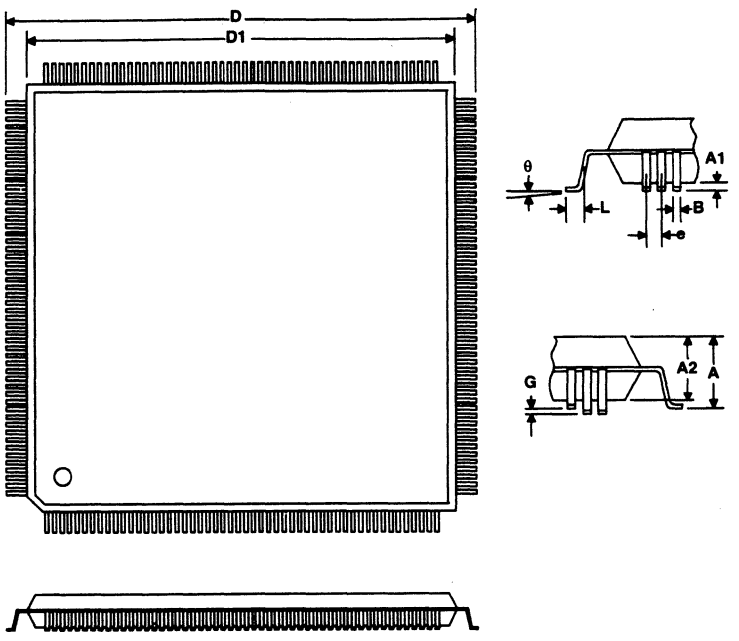


Figure 87. 208-Pin Quad Flatpack (QFP) Dimensions

Table 23. 82434LX Package Dimensions

Symbol	Description	Value (mm)
A	Seating Height	3.5 (max)
A1	Stand-Off Height	0.20–0.50
A2	Package Height	3.0 (nominal)
B	Lead Width	0.18 +0.1/−0.05
D	Package Length and Width, Including Pins	30.6 ± 0.3
D1	Package Length and Width, Excluding Pins	28 ± 0.1
e	Linear Lead Pitch	0.5 ± 0.1
G	Lead Coplanarity	0.1 (max)
L	Lead Length	0.5 ± 0.2
θ	Lead Angle	0°–10°

Table 24. 82434NX Package Dimensions

Symbol	Description	Value (mm)
A	Seating Height	3.7 (max)
A1	Stand-Off Height	0.05–0.50
A2	Package Height	3.45 (max)
B	Lead Width	0.13–0.27
D	Package Length and Width, Including Pins	30.6 ± 0.3
D1	Package Length and Width, Excluding Pins	28 ± 0.1
e	Linear Lead Pitch	0.5 (nominal)
G	Lead Coplanarity	0.1 (max)
L	Lead Length	0.5 ± 0.2
θ	Lead Angle	0°–10°

11.0 TESTABILITY

A NAND tree is provided in the 82434LX and 82434NX PCMCs for Automated Test Equipment (ATE) board level testing. The NAND tree allows the tester to test the connectivity of a subset of the PCMC signal pins.

For the 82434LX, the output of the NAND tree is driven on pin 109. The NAND tree is enabled when A24 = 1, A25 = 0, A26 = 1, and TESTEN = 1 at the rising edge of PWROK. PLL Bypass mode is enabled when A24 = 1, and TESTEN = 1 at the rising edge of PWROK. In PLL Bypass mode, the 82434LX and 82434NX PCMC AC specifications are affected as follows:

1. Output valid delays increase by 20 ns.
2. All hold times are 20 ns.
3. Setup times and propagation delays are unaffected.
4. Input clock high and low times are 100 ns.

In both the NAND tree test mode and PLL Bypass mode, TESTEN must remain asserted throughout the testing. A[28:24] should be set up at least 1 HCLK before the rising edge of PWROK and held at least 3 HCLKs after PWROK. Table 11 shows the order of the NAND tree inside the PCMC.

When not in NAND Tree test mode, the 82434LX drives the output of the host clock PLL onto pin 109.

82434NX Test Modes

The state of A[28:24], TESTEN, CPURST, and PWROK can place the 82434NX PCMC into two test modes. When PWROK is low, A[27:24] and TESTEN directly control the mode of operation of the PCMC. When PWROK is high, the state of A[27:24] and TESTEN are latched and the PCMC remains in the indicated mode until PWROK is again negated. The high order LBX samples the state of A27 on the falling edge of CPURST.

When PWROK is low and both TESTEN and A27 are low, the 82434NX drives MA11 onto pin 109. If both TESTEN and A27 are low when PWROK transitions from low to high, the PCMC continues to drive MA11 onto pin 109. If the high order LBX samples A27 low on the falling edge of CPURST, it will tri-state pin 123.

When PWROK is low, TESTEN is low, and A27 is high the PCMC drives the output of the host clock PLL onto pin 109. Observing pin 109 when in this mode indicates if the host clock PLL has locked onto the correct frequency. If TESTEN is low and A27 is high when PWROK transitions from low to high the PCMC continues to drive the output of the host clock PLL onto pin 109, regardless of the values of TESTEN and A27. If the high order LBX samples A27 high on the falling edge of CPURST, it drives the output of its host clock PLL onto pin 123. No phase delay information can be inferred from these outputs.

When PWROK is low, TESTEN is high, A26 is high, A25 is low, A28 is high and A24 is high, the PCMC will drive the output of the NAND tree onto pin 109. If TESTEN is high, A26 is high, and A25 is low when PWROK transitions from low to high, the PCMC continues to drive the output of the NAND tree onto pin 109.

A27 must be pulled low via a pulldown resistor to ground for normal operation.

Table 25. NAND Tree Order

Order	Pin #	Signal
1	141	TRDY#
2	142	IRDY#
3	143	CBE3#
4	144	CBE2#
5	145	CBE1#
6	146	CBE0#
7	159	PPOUT0
8	160	PPOUT1
9	161	EOL
10	162	FLSHBUF#
11	163	GNT#
12	164	MEMCS#
13	165	MEMREQ#
14	167	STOP#
15	168	PLOCK#
16	169	PERR#
17	170	DEVSEL#
18	171	PAR
19	172	SERR#
20	173	FRAME#
21	194	REQ#
22	196	A23
23	197	A27
24	198	A29
25	199	A31
26	200	A21
27	201	A16
28	202	A17
29	203	A18
30	204	A0
31	205	A1
32	206	A2
33	207	A30
34	2	A28
35	3	A24
36	4	A22
37	5	A26
38	6	A19
39	7	A20
40	8	A25
41	9	A4
42	10	A5
43	11	A6
44	12	A3
45	13	A8
46	14	A7
47	15	A10
48	16	A9
49	17	A12
50	18	A11
51	19	A13
52	21	A14
53	22	A15
54	53	BE1#
55	54	BE5#
56	55	BE4#
57	56	BE0#
58	57	BE2#
59	58	BE6#
60	59	BE3#
61	60	BE7#
62	61	M/IO#
63	64	CACHE#
64	65	HITM#
65	66	ADS#
66	67	W/R#
67	68	D/C#
68	69	SMIACT#
69	71	HLOCK#
70	72	PCHK#
71	63	TESTEN

ADDITIONAL TESTING NOTES:

1. HCLKOUT[6:1] can be toggled via HCLKIN.
2. CAx[6:3] are flow through outputs via A[6:3] after PWROK transitions high.
3. MA[10:0] are flow through outputs via A[13:3] after PWROK transitions high.
4. CAS[7:0]# outputs can be tested by performing a DRAM read cycle.
5. PCLKOUT can be tested in PLL bypass mode, frequency is HCLK/2.
6. PCIRST is the NAND Tree output of Tree Cell 6.
7. INIT is the NAND Tree output of Tree Cell 53.

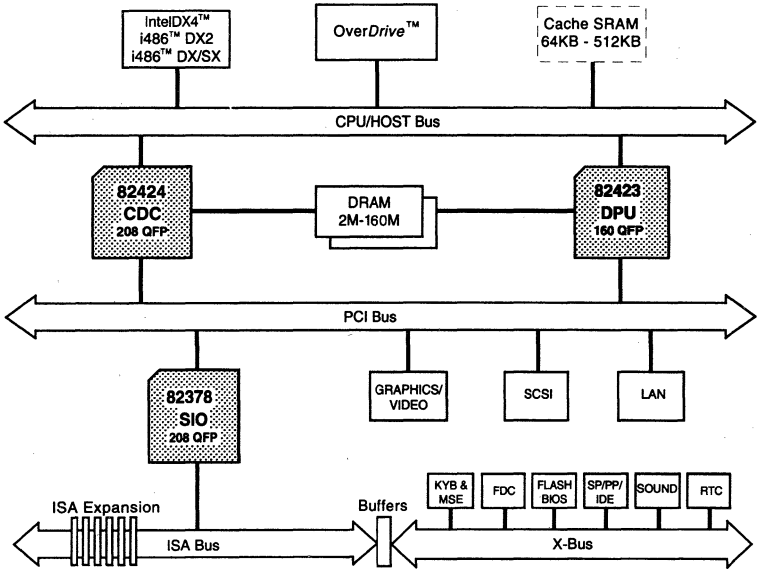
82420 PCIset

Intel's 82420 PCIset enables workstation level of performance for Intel486™ CPU desktop systems. The Peripheral Component Interconnect Bus (PCI) is driving a new architecture for PC's—eliminating the I/O bottleneck of standard expansion busses. PCI provides a glueless interface for high performance peripherals such as graphics, SCSI, LAN and video to be placed onto a fast local bus. By utilizing this technology and incorporating read/write bursts along with write buffers into the 82420 PCIset, a new level of performance is now possible for today's Intel486 CPU desktop systems.

The Intel 82420 PCIset is comprised of three components: the 82424ZX Cache DRAM Controller (CDC), the 82423TX Data Path Unit (DPU), and the 82378ZB System I/O (SIO). The CDC and DPU provide the core system architecture while the SIO is a PCI master/slave agent which bridges the core architecture to the ISA standard expansion bus. Intel also offers two components, the 82374EB (ESC) and 82375EB (PCEB), that work in conjunction to bridge the PCI bus to the EISA expansion bus. Refer to the ESC and PCEB data sheets for information regarding the EISA bridge components.

The chip set supports the Intel486 CPU family as well as Intel's future OverDrive™ processor for the Intel486 DX2 CPU. The high performance memory subsystem supports concurrent operation between PCI bus masters while the CPU accesses memory. An integrated second level cache can be programmed for write-through or write-back operation.

82420 PCIset



290467-1

The complete document for this product can be ordered by calling 1-800-548-4725.

November 1994
Order Number: 290467-005

Product Highlights

82424ZX—Cache DRAM Controller (CDC)

- Concurrent Linefill during Copyback Cycles
- Supports Intel486 CPU Family and OverDrive Processors
- Supports OverDrive Upgrade
- 64K–512K Level 2 Cache Support
- Level 2 Cache Configurable as Write-Back or Write-Through
- 208-Pin QFP Package

82423TX—Data Path Unit (DPU)

- Highly Integrated
- Four Dword Write Buffers
- Zero Wait-States for CPU Write Cycles
- PCI Burst Write Capability
- 160-Pin QFP Package

82378ZB—System I/O Component (SIO)

- Supports Fast DMA Type A, B, or F Cycles
- Supports DMA Scatter/Gather
- Arbitration Logic for Four PCI Masters
- Reusable across Multiple Platforms
- Directly Drives Six External ISA Slots
- Integrates Many of Today's Common I/O Functions
- 208-Pin QFP Package

Product Description

The 82424ZX Cache DRAM Controller (CDC) is a single-chip bridge from the CPU to the PCI bus. It provides the integrated functionality of a second level cache controller, a DRAM controller, and a PCI bus controller. It also features an optimized memory subsystem. The CDC is a dual ported device with one port as the host port and the other as the PCI port.

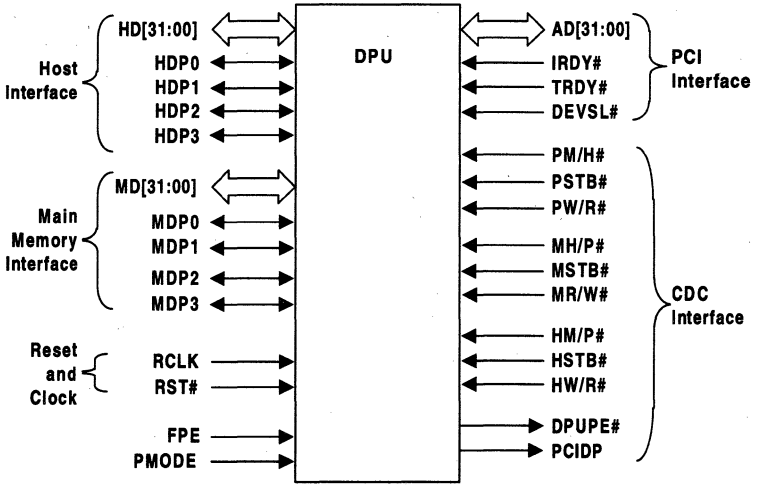
The 82423TX Data Path Unit (DPU) integrates the host data, memory data, and PCI data interface, DPU control/parity and four deep posted write buffers. With glue and buffers integrated directly into the DPU, the Intel 82420 PCIset reduces board space requirements. The DPU's posted write buffers allow CPU write cycles to be executed as 0 wait-states.

The 82378ZB System I/O (SIO) is a dual ported device which acts as a bridge between the PCI and standard ISA I/O bus. The SIO integrates the functionality of an ISA controller, PCI controller, fast 32-bit DMA controller, and standard system I/O functions.

82423TX
DATA PATH UNIT (DPU)

- **A 32-bit High Performance Host/PCI/ Memory Data Path**
- **Operates Synchronously to the CPU and PCI Clocks**
- **Dual-Port Architecture Allows Concurrent Operations on the Host and PCI Buses**
- **Burst Read of Memory from the Host and PCI Buses**
- **Host-to-Memory and Host-to-PCI Post Buffers Permit Zero Wait-State Write Performance**
- **Byte Parity Support for the Host and Memory Buses**
  - **— Optional Parity Generation for Host-to-Memory Transfers**
  - **— Optional Parity Checking Residing on the Host Data Bus**
  - **— Parity Checking for Host and PCI Memory Reads**
  - **— Parity Generation for PCI-to-Memory Writes**
- **Force Bad Parity to Memory Capability for Diagnostic Purposes**

The 82423TX Data Path Unit (DPU) provides the 32-bit data path connections between the Host (CPU/cache), main memory, and the Peripheral Component Interconnect (PCI) Bus. The dual-port architecture allows concurrent operations on the Host and PCI Buses. Two 4-Dword deep Post buffers permit Host posting of data to main memory and the PCI Bus. The DPU supports byte parity for the Host and main memory buses. The DPU is intended to be used with the 82424ZX Cache DRAM Controller (CDC). During bus operations between the Host, main memory, and PCI, the CDC provides the address paths and bus controls. The CDC also controls the data flow through the DPU. Together, these two chips provide a full function dual-port data path connection to main memory and forms a Host/PCI bridge.



290472-1

The complete document for this product can be ordered by calling 1-800-548-4725. Ask for order number 290467.

November 1994
Order Number: 290472-003

82424ZX CACHE AND DRAM CONTROLLER (CDC)

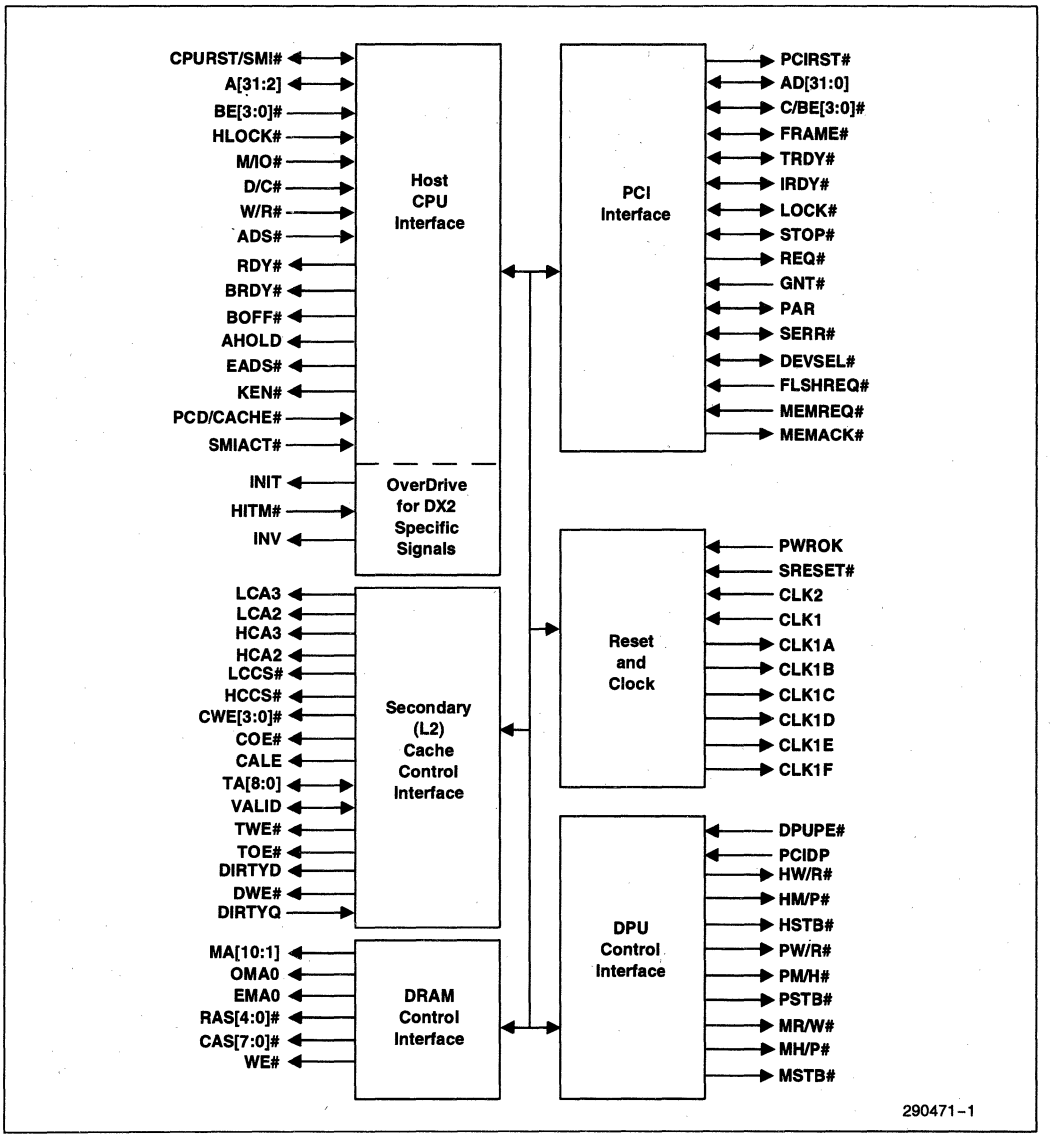
- Supports 25/33 MHz Intel486™ SX, Intel487™ SX, Intel486 DX, Intel486 DX2, IntelDX4™, OverDrive™ for Intel486 and OverDrive for DX2 Processors
- Fully Backward Compatible with Intel 82424TX
- Synchronous, 25/33 MHz PCI Bus Interface Capable of Supporting Bus Masters
- Supports OverDrive Upgrade Socket
- Programmable Attribute Map for First 1 MByte of Main Memory
- Posted Write Buffers for Improved Performance
- Integrated DRAM Controller
  - 2 to 160 MByte Main Memory Using 70 ns Fast Page Mode SIMM Memory
  - Decoupled Refresh Cycles to Reduce DRAM Access Latency
- Integrated Cache Controller
  - Write-Through and Write-Back Cache Options
  - 64 KB, 128 KB, 256 KB, and 512 KB Cache Sizes Using Standard SRAMS
  - Burst Line Fill of 2-1-1-1 from Secondary Cache at 25 and 33 MHz
  - Zero Wait-State Write to L2 Cache for a Cache Write Hit
  - Main Memory Posting at Zero Wait-States, Enabling Optimum Write-Through Cache Performance
  - Concurrent Cache Line Replacement from Secondary Cache in Write-Back Mode
- PCI Bridge
  - Translates CPU Cycles into PCI Bus Cycles
  - Translates Back-to-Back Sequential Memory Write Cycles into PCI Burst Cycles
  - Separate PCI-to-Main Memory Port Allows Concurrent/Independent CPU and PCI Bus Operations
  - Zero Wait-State Write Posting into the DPU for Fast Graphics Transfers
  - Integrated Snoop Filter
- Complete Support for SL Enhanced Intel486 CPUs
  - SMM Space Remapping to TOM, A0000 and B0000 Segments
  - Stop Grant Cycle Translation from Host-to-PCI Bus

1

The 82424ZX Cache DRAM Controller (CDC) integrates the cache and main memory DRAM control functions and provides the address paths and bus control for transfers between the Host (CPU/cache), main memory, and the Peripheral Component Interconnect (PCI) Bus. The 82424ZX is completely backward compatible with the 82424TX. The Dual-ported architecture permits concurrent operations on the Host and PCI Buses. The cache controller supports both write-through and write-back cache policies and cache sizes from 64 to 512 KBytes. The cache memory can be implemented using standard asynchronous SRAMs. The dual-ported main memory DRAM controller interfaces DRAM to the Host Bus and the PCI Bus. The CDC supports a two-way interleaved DRAM organization for optimum performance. The CDC is intended to be used with the 82423TX Data Path Unit (DPU). The DPU provides 32-bit data paths between the Host, main memory, and the PCI. Together, these two components provide a full function dual-port data path connection to main memory and form a Host/PCI Bridge.

The complete document for this product can be ordered by calling 1-800-548-4725 and ask for order number 290467.

November 1994
Order Number: 290471-004



Simplified CDC Block Diagram

82420EX PCISET DATA SHEET
82425EX PCI SYSTEM CONTROLLER (PSC) AND 82426EX ISA BRIDGE (IB)

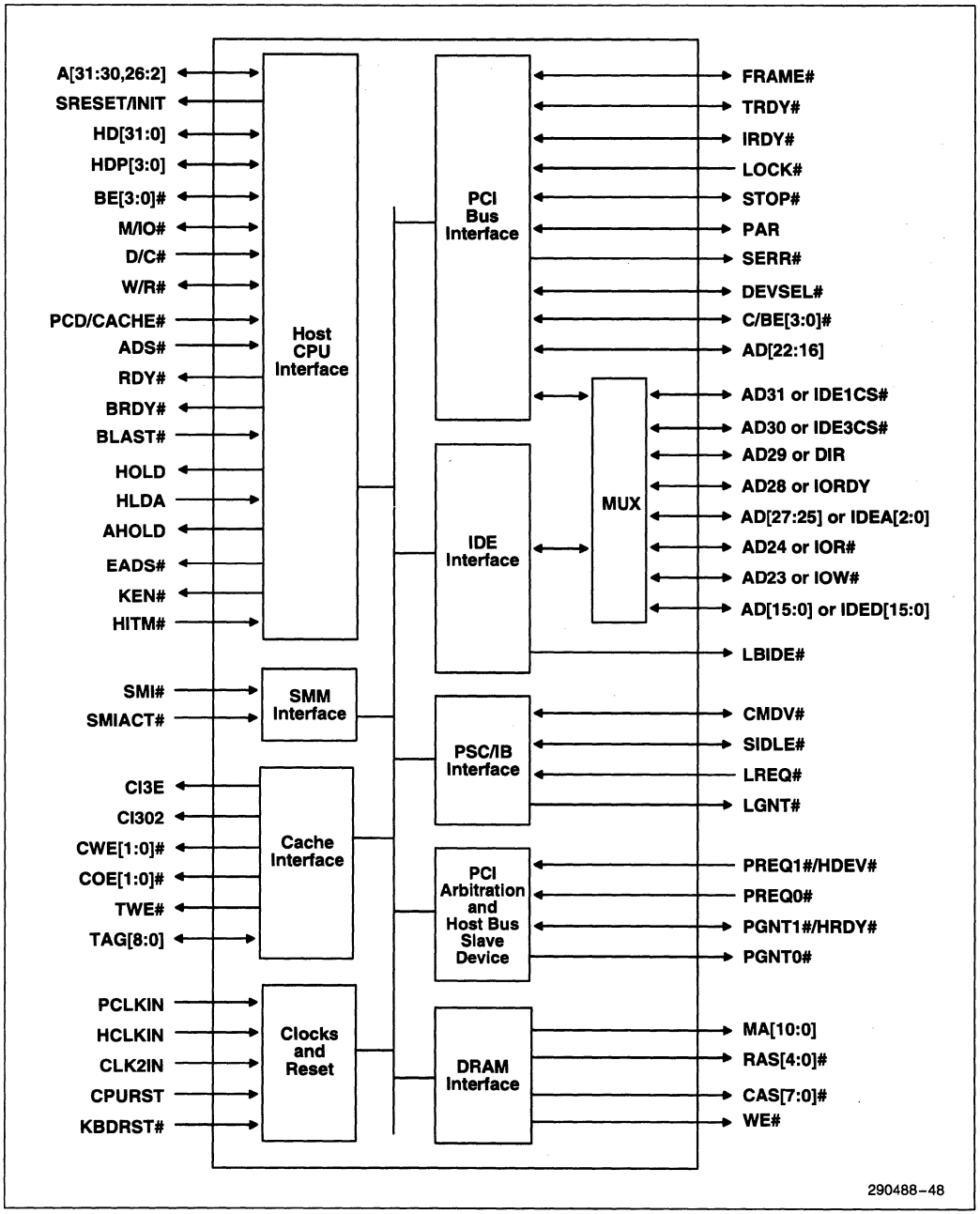
- Host CPU
  - 25–33 MHz Intel486™ and OverDrive™ Processors
  - L1 Write-Back Support
- Integrated DRAM Controller
  - 1 to 128 MByte Main Memory
  - 70 ns Fast Page Mode DRAM SIMMs Supported
  - Supports 256 KByte, 1 MByte, and 4 MByte Double and Single Sided SIMMs
  - Read Page Hit Timing of 3-2-2-2 at 33 MHz
  - Burst Mode PCI Master Accesses
  - Decoupled Refresh Reduces DRAM Latency
  - Five RAS Lines
- Integrated L2 Cache Controller
  - Write-Back and Write-Through Cache Policies
  - Direct Mapped Organization
  - 64, 128, 256 or 512 KByte Cache Sizes
  - Programmable Zero Wait-State L2 Cache Read and Write Accesses
  - Two Banks Interleaved or a Single Bank Non-Interleaved Operation
  - No VALID Bit Required
- 25/33 MHz PCI Bus Interface
  - Two Bus Masters
  - PCI Auto Configuration Support
- Host/PCI Bridge
  - Converts Back-to-Back Sequential Memory Writes to PCI Burst Writes
  - CPU Memory Write Posting to PCI
- PCI Local Bus IDE Interface
  - Supports Mode 3 Timing
- Programmable Attribute Map for First 1 MByte of Main Memory
- 100% ISA Compatible
  - Directly Drives 5 ISA Slots
- Two 8237 DMA Controllers
  - 7 DMA Channels
  - 27-bit Addressability
  - Compatible DMA Transfers
- One 82C54 Timer/Counter
  - System Timer
  - Refresh Request
  - Speaker Tone
- Two 82C59 Interrupt Controllers
  - 14 Interrupts
  - Edge/Level Sense is Programmable per Channel
  - PCI Interrupt Steering for Plug and Play Compatibility
- X-Bus Peripheral Support
  - RTC, KBC, BIOS Chip Selects
  - Control for Lower X-Bus Transceiver
  - Integrates Mouse Interrupt
  - Coprocessor Error Reporting
- Non-Maskable Interrupts (NMI)
  - PCI System Errors
  - Main Memory Parity Errors
  - ISA Parity Errors
- System Power Management (Intel SMM Support)
  - Programmable System Management Interrupt (SMI)—Hardware Events, Software Events, EXTSMI#
  - Programmable CPU Clock Control
  - Fast On/Off Mode
- Generates System Clocks
- 160-Pin QFP Package for IB
- 208-Pin QFP Package for PSC

December 1994
Order Number: 290488-003

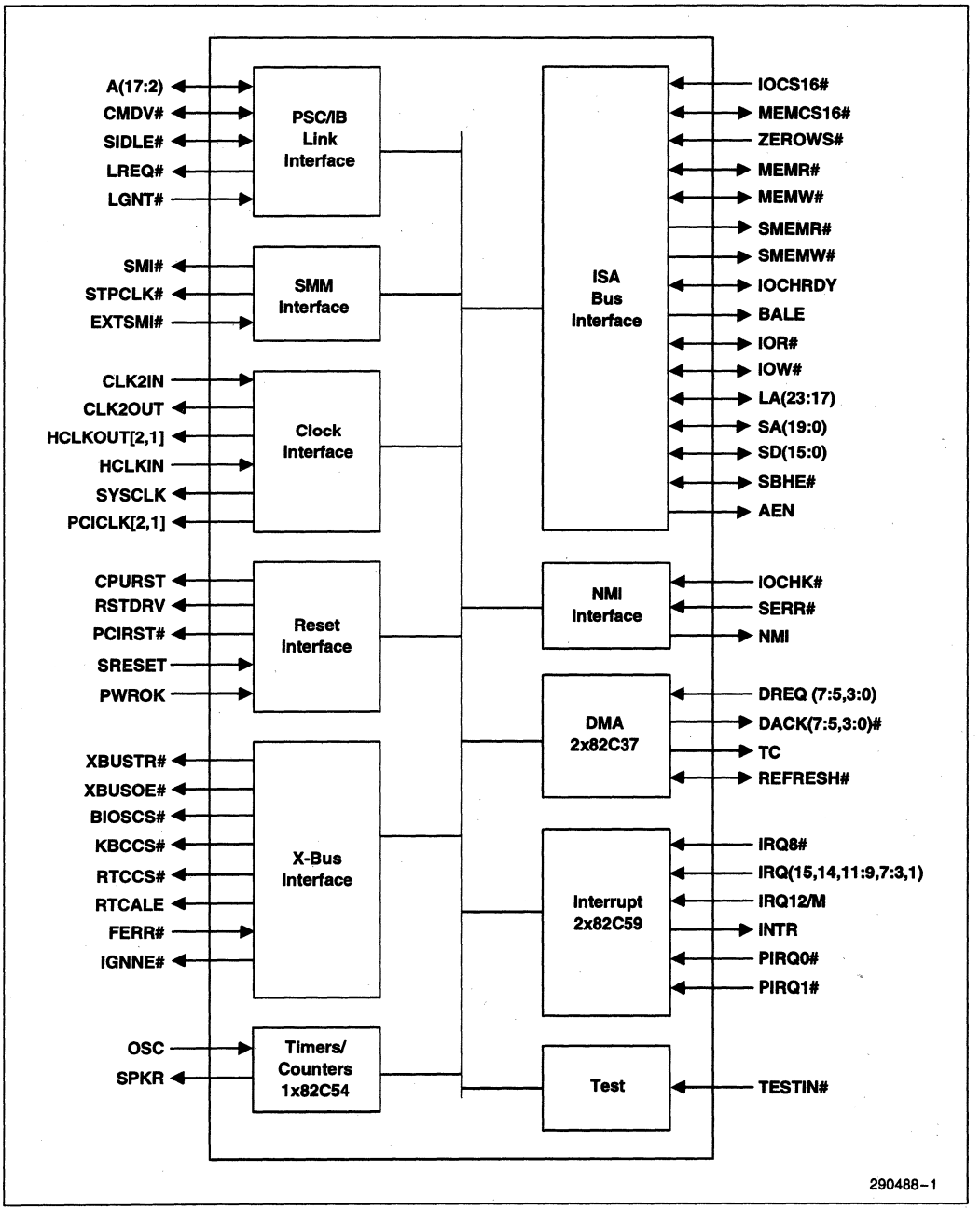
The 82420EX PCIset is the foundation for the **Value Flexible Motherboard** solution for entry-level Intel486™ processor-based PCI systems. The Value Flexible Motherboard solution, including 82420EX, Intel486 processor, 82091AA Advanced Integrated Peripherals, 82C42 Keyboard Controller, Flash BIOS, and Plug & Play software, drives PCI into the mainstream. The 82420EX PCIset is a highly integrated solution enabling low cost, small form factor motherboard designs. All Intel486 processors and upgrades are supported, including L1 write-back and Intel SMM power management. PCI Local Bus IDE is incorporated for higher performance IDE at no additional cost.

The 82420EX was designed from the ground up for PCI performance. It consists of two components—the 82425EX PCI System Controller (PSC) and the 82426EX ISA Bridge (IB). The PSC integrates the L2 cache controller and the DRAM controller. The cache controller supports both write-through and write-back cache policies and cache sizes from 64 KBytes to 512 KBytes in an interleaved or non-interleaved configuration. The DRAM controller interfaces main memory to the Host Bus and the PCI Bus. The PSC supports a two-way interleaved DRAM organization for optimum performance. Up to ten single-sided SIMMs or four double-sided and two single-sided SIMMs provide a maximum of 128 MBytes of main memory. The PSC provides memory write posting to PCI for enhanced CPU-to-PCI memory write performance. In addition, the PSC provides a high performance PCI Local Bus IDE interface.

The IB is the bridge between the ISA Bus and Host Bus, and integrates the common I/O functions found in today's ISA-based PC systems—a seven channel DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, Intel SMM power management support, and control logic for NMI generation. The IB also provides the decode for external BIOS, real time clock, and keyboard controller. Edge/Level interrupts and interrupt steering are supported for PCI plug and play compatibility. The IB integrates the ISA address and data path, reducing TTL and system cost. In addition, the integration of system clock generation logic eliminates the need for external host and PCI clock drivers.



82425EX PCI System Controller (PSC) Block Diagram



82426EX ISA Bridge (IB) Block Diagram

82420EX PCISET DATA SHEET
82425EX PCI SYSTEM CONTROLLER (PSC) AND 82426EX ISA BRIDGE (IB)

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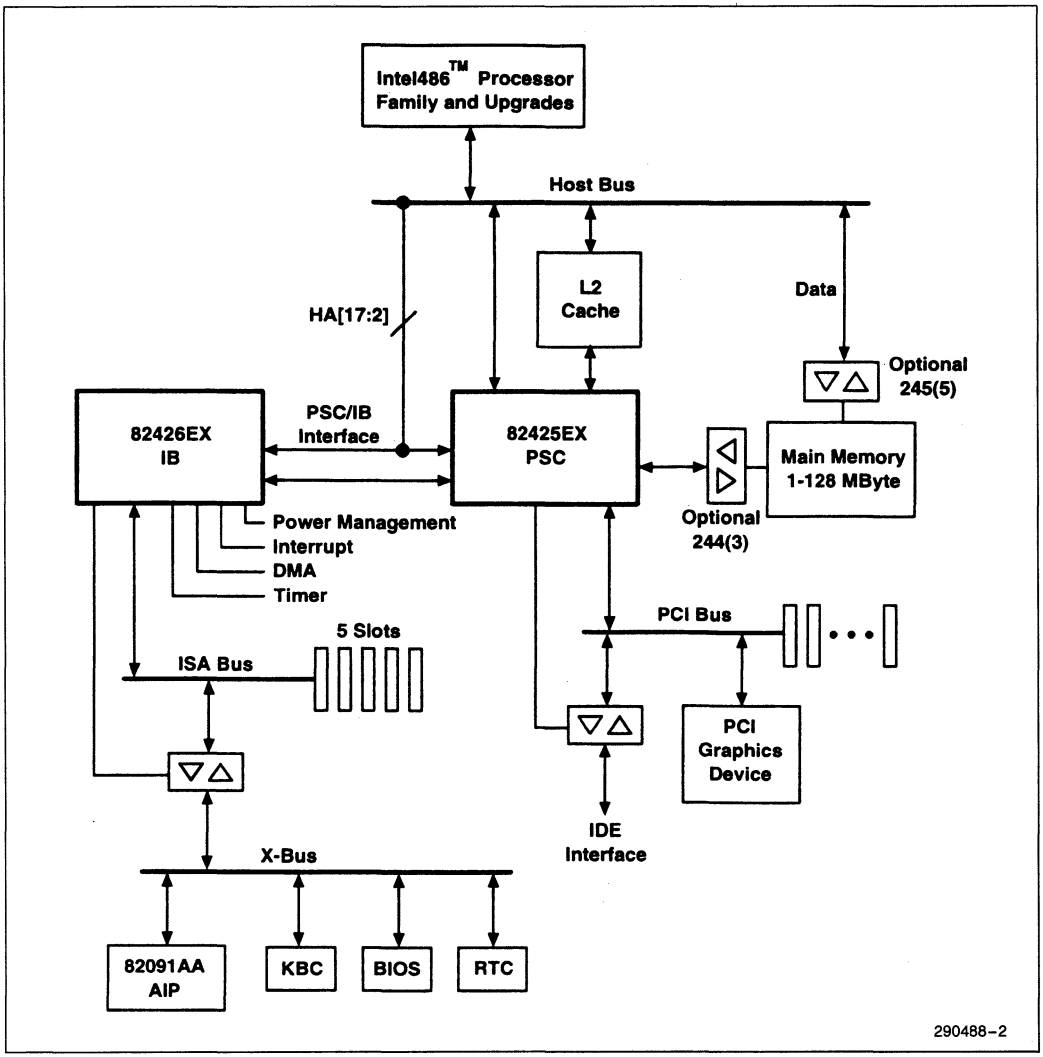


Figure 1. Example System Block Diagram

1.0 PINOUT INFORMATION

This section provides the PSC and IB pin assignment and package information. For each device, the pin assignments are listed in both alphabetical and numerical order.

1.1 PSC Pin Assignment

The PSC package is a 208-pin Quad Flatpack (QFP). Figure 2 shows the pin assignment on the package. Tables 1 and 2 list the pin assignments alphabetically and numerically, respectively.

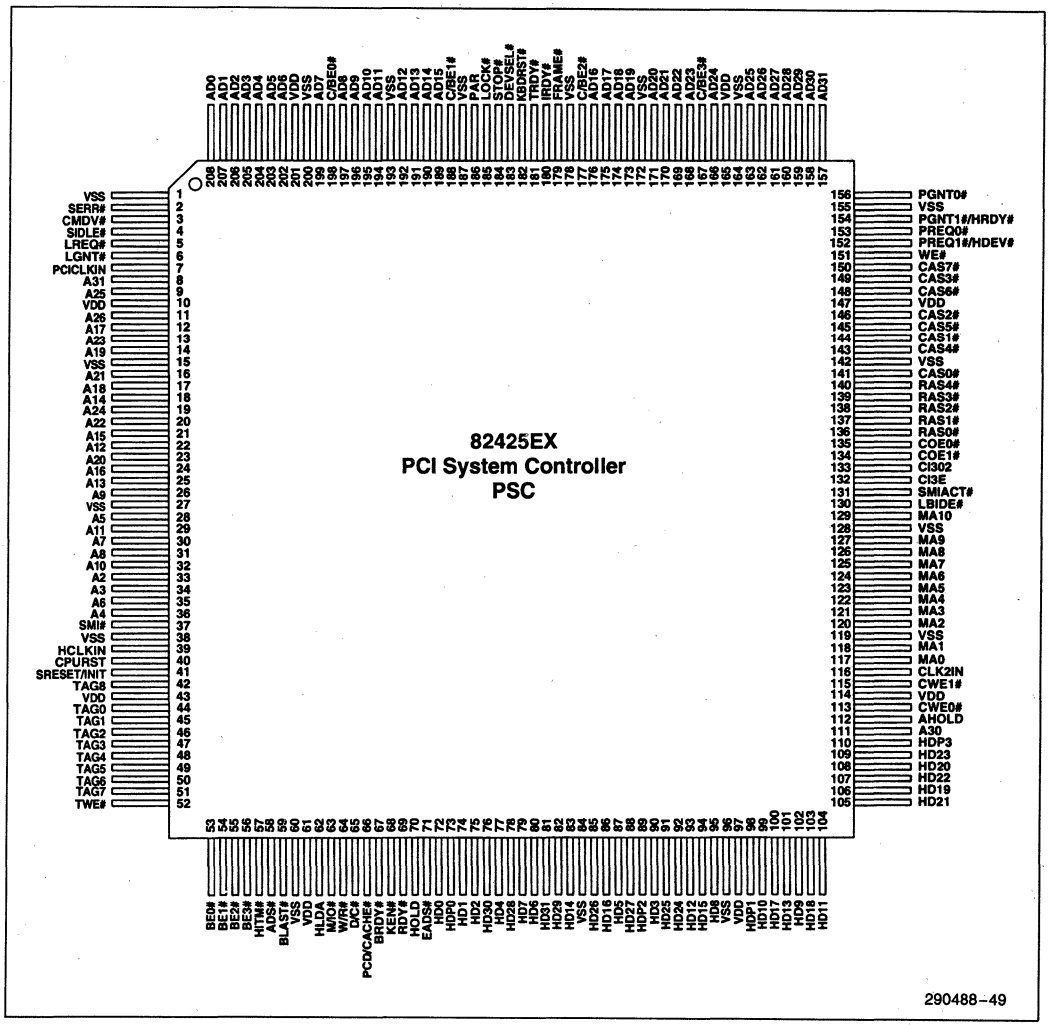


Figure 2. PSC Pin Assignment

Table 1. Alphabetical PSC Pin Assignment List

Pin Name	Pin #	I/O
A2	33	I/O
A3	34	I/O
A4	36	I/O
A5	28	I/O
A6	35	I/O
A7	30	I/O
A8	31	I/O
A9	26	I/O
A10	32	I/O
A11	29	I/O
A12	22	I/O
A13	25	I/O
A14	18	I/O
A15	21	I/O
A16	24	I/O
A17	12	I/O
A18	17	I/O
A19	14	I/O
A20	23	I/O
A21	16	I/O
A22	20	I/O
A23	13	I/O
A24	19	I/O
A25	9	I/O
A26	11	I/O
A30	111	I/O
A31	8	I/O
AD0	208	I/O
AD1	207	I/O
AD2	206	I/O
AD3	205	I/O
AD4	204	I/O

Pin Name	Pin #	I/O
AD5	203	I/O
AD6	202	I/O
AD7	199	I/O
AD8	197	I/O
AD9	196	I/O
AD10	195	I/O
AD11	194	I/O
AD12	192	I/O
AD13	191	I/O
AD14	190	I/O
AD15	189	I/O
AD16	176	I/O
AD17	175	I/O
AD18	174	I/O
AD19	173	I/O
AD20	171	I/O
AD21	170	I/O
AD22	169	I/O
AD23	168	I/O
AD24	166	I/O
AD25	163	I/O
AD26	162	I/O
AD27	161	I/O
AD28	160	I/O
AD29	159	I/O
AD30	158	I/O
AD31	157	I/O
ADS#	58	I
AHOLD	112	O
BE0#	53	I/O
BE1#	54	I/O
BE2#	55	I/O

Pin Name	Pin #	I/O
BE3#	56	I/O
BLAST#	59	I
BRDY#	67	O
C/BE0#	198	I/O
C/BE1#	188	I/O
C/BE2#	177	I/O
C/BE3#	167	I/O
CAS0#	141	O
CAS1#	144	O
CAS2#	146	O
CAS3#	149	O
CAS4#	143	O
CAS5#	145	O
CAS6#	148	O
CAS7#	150	O
CI3E	132	O
CI3O2	133	O
CLK2IN	116	I
CMDV#	3	I/O
COE0#	135	O
COE1#	134	O
CPURST	40	I
CWE0#	113	O
CWE1#	115	O
D/C#	65	I
DEVSEL#	183	s/t/s
EADS#	71	O
FRAME#	179	s/t/s
HCLKIN	39	I
HD0	72	I/O
HD1	74	I/O
HD2	75	I/O

Pin Name	Pin #	I/O
HD3	90	I/O
HD4	77	I/O
HD5	87	I/O
HD6	80	I/O
HD7	79	I/O
HD8	95	I/O
HD9	102	I/O
HD10	99	I/O
HD11	104	I/O
HD12	93	I/O
HD13	101	I/O
HD14	83	I/O
HD15	94	I/O
HD16	86	I/O
HD17	100	I/O
HD18	103	I/O
HD19	106	I/O
HD20	108	I/O
HD21	105	I/O
HD22	107	I/O
HD23	109	I/O
HD24	92	I/O
HD25	91	I/O
HD26	85	I/O
HD27	88	I/O
HD28	78	I/O
HD29	82	I/O
HD30	76	I/O
HD31	81	I/O
HDP0	73	I/O
HDP1	98	I/O
HDP2	89	I/O

Table 1. Alphabetical PSC Pin Assignment List (Continued)

Pin Name	Pin #	I/O
HDP3	110	I/O
HITM#	57	I
HLDA	62	I
HOLD	70	O
IRDY#	180	s/t/s
KBDRST#	182	I
KEN#	68	O
LBIDE#	130	O
LGNT#	6	O
LOCK#	185	I
LREQ#	5	I
M/IO#	63	I/O
MA0	117	O
MA1	118	O
MA2	120	O
MA3	121	O
MA4	122	O
MA5	123	O
MA6	124	O
MA7	125	O
MA8	126	O

Pin Name	Pin #	I/O
MA9	127	O
MA10	129	O
PAR	186	I/O
PCD/ CACHE	66	I
PCICLKIN	7	I
PGNT0#	156	O
PGNT1#/ HRDY#	154	I/O
PREQ0#	153	I
PREQ1#/ HDEV#	152	I
RAS0#	136	O
RAS1#	137	O
RAS2#	138	O
RAS3#	139	O
RAS4#	140	O
RDY#	69	O
SERR#	2	OD
SIDLE#	4	I/O
SMI#	37	I

Pin Name	Pin #	I/O
SMIACT#	131	I
SRESET/ INIT	41	O
STOP#	184	s/t/s
TAG0	44	I/O
TAG1	45	I/O
TAG2	46	I/O
TAG3	47	I/O
TAG4	48	I/O
TAG5	49	I/O
TAG6	50	I/O
TAG7	51	I/O
TAG8	42	I/O
TRDY#	181	s/t/s
TWE#	52	O
V_{DD}	10	V
V_{DD}	43	V
V_{DD}	61	V
V_{DD}	97	V
V_{DD}	147	V
V_{DD}	114	V

Pin Name	Pin #	I/O
V_{DD}	165	V
V_{DD}	201	V
V_{SS}	1	V
V_{SS}	15	V
V_{SS}	27	V
V_{SS}	38	V
V_{SS}	60	V
V_{SS}	84	V
V_{SS}	96	V
V_{SS}	119	V
V_{SS}	128	V
V_{SS}	142	V
V_{SS}	155	V
V_{SS}	164	V
V_{SS}	172	V
V_{SS}	178	V
V_{SS}	187	V
V_{SS}	193	V
V_{SS}	200	V
WE#	151	O
W/R#	64	I/O

Table 2. Numerical PSC Pin Assignment List

Pin Name	Pin #	I/O
V_{SS}	1	V
SERR#	2	OD
CMDV#	3	I/O
SIDLE#	4	I/O
LREQ#	5	I
LGNT#	6	O
PCICLKIN	7	I
A31	8	I/O
A25	9	I/O
V_{DD}	10	V
A26	11	I/O
A17	12	I/O
A23	13	I/O
A19	14	I/O
V_{SS}	15	V
A21	16	I/O
A18	17	I/O
A14	18	I/O
A24	19	I/O
A22	20	I/O
A15	21	I/O
A12	22	I/O
A20	23	I/O
A16	24	I/O
A13	25	I/O
A9	26	I/O
V_{SS}	27	V
A5	28	I/O
A11	29	I/O
A7	30	I/O

Pin Name	Pin #	I/O
A8	31	I/O
A10	32	I/O
A2	33	I/O
A3	34	I/O
A6	35	I/O
A4	36	I/O
SMI#	37	I
V_{SS}	38	V
HCLKIN	39	I
CPURST	40	I
SRESET/ INIT	41	O
TAG8	42	I/O
V_{DD}	43	V
TAG0	44	I/O
TAG1	45	I/O
TAG2	46	I/O
TAG3	47	I/O
TAG4	48	I/O
TAG5	49	I/O
TAG6	50	I/O
TAG7	51	I/O
TWE#	52	O
BE0#	53	I/O
BE1#	54	I/O
BE2#	55	I/O
BE3#	56	I/O
HITM#	57	I
ADS#	58	I
BLAST#	59	I
V_{SS}	60	V

Pin Name	Pin #	I/O
V_{DD}	61	V
HLDA	62	I
M/IO#	63	I/O
W/R#	64	I/O
D/C#	65	I
PCD/ CACHE#	66	I
BRDY#	67	O
KEN#	68	O
RDY#	69	O
HOLD	70	O
EADS#	71	O
HD0	72	I/O
HDP0	73	I/O
HD1	74	I/O
HD2	75	I/O
HD30	76	I/O
HD4	77	I/O
HD28	78	I/O
HD7	79	I/O
HD6	80	I/O
HD31	81	I/O
HD29	82	I/O
HD14	83	I/O
V_{SS}	84	V
HD26	85	I/O
HD16	86	I/O
HD5	87	I/O
HD27	88	I/O
HDP2	89	I/O
HD3	90	I/O

Pin Name	Pin #	I/O
HD25	91	I/O
HD24	92	I/O
HD12	93	I/O
HD15	94	I/O
HD8	95	I/O
V_{SS}	96	V
V_{DD}	97	V
HDP1	98	I/O
HD10	99	I/O
HD17	100	I/O
HD13	101	I/O
HD9	102	I/O
HD18	103	I/O
HD11	104	I/O
HD21	105	I/O
HD19	106	I/O
HD22	107	I/O
HD20	108	I/O
HD23	109	I/O
HDP3	110	I/O
A30	111	I/O
AHOLD	112	O
CWE0#	113	O
V_{DD}	114	V
CWE1#	115	O
CLK2IN	116	I
MA0	117	O
MA1	118	O
V_{SS}	119	V
MA2	120	O

Table 2. Numerical PSC Pin Assignment List (Continued)

Pin Name	Pin #	I/O
MA3	121	O
MA4	122	O
MA5	123	O
MA6	124	O
MA7	125	O
MA8	126	O
MA9	127	O
V_{SS}	128	V
MA10	129	O
LBIDE#	130	O
SMIACT#	131	I
C13E	132	O
C13O2	133	O
COE1#	134	O
COE0#	135	O
RAS0#	136	O
RAS1#	137	O
RAS2#	138	O
RAS3#	139	O
RAS4#	140	O
CAS0#	141	O
V_{SS}	142	V

Pin Name	Pin #	I/O
CAS4#	143	O
CAS1#	144	O
CAS5#	145	O
CAS2#	146	O
V_{DD}	147	V
CAS6#	148	O
CAS3#	149	O
CAS7#	150	O
WE#	151	O
PREQ1# / HDEV#	152	I
PREQ0#	153	I
PGNT1# / HRDY#	154	I/O
V_{SS}	155	V
PGNT0#	156	O
AD31	157	I/O
AD30	158	I/O
AD29	159	I/O
AD28	160	I/O
AD27	161	I/O
AD26	162	I/O
AD25	163	I/O
V_{SS}	164	V

Pin Name	Pin #	I/O
V_{DD}	165	V
AD24	166	I/O
C/BE3#	167	I/O
AD23	168	I/O
AD22	169	I/O
AD21	170	I/O
AD20	171	I/O
V_{SS}	172	V
AD19	173	I/O
AD18	174	I/O
AD17	175	I/O
AD16	176	I/O
C/BE2#	177	I/O
V_{SS}	178	V
FRAME#	179	s/t/s
IRDY#	180	s/t/s
TRDY#	181	s/t/s
KBDRST#	182	I
DEVSEL#	183	s/t/s
STOP#	184	s/t/s
LOCK#	185	I
PAR	186	I/O

Pin Name	Pin #	I/O
V_{SS}	187	V
C/BE1#	188	I/O
AD15	189	I/O
AD14	190	I/O
AD13	191	I/O
AD12	192	I/O
V_{SS}	193	V
AD11	194	I/O
AD10	195	I/O
AD9	196	I/O
AD8	197	I/O
C/BE0#	198	I/O
AD7	199	I/O
V_{SS}	200	V
V_{DD}	201	V
AD6	202	I/O
AD5	203	I/O
AD4	204	I/O
AD3	205	I/O
AD2	206	I/O
AD1	207	I/O
AD0	208	I/O

1.2 IB Pin Assignment

The IB package is a 160-pin Quad Flatpack (QFP). Figure 3 shows the package pin assignment. Table 3 and Table 4 list the pin assignment alphabetically and numerically, respectively.

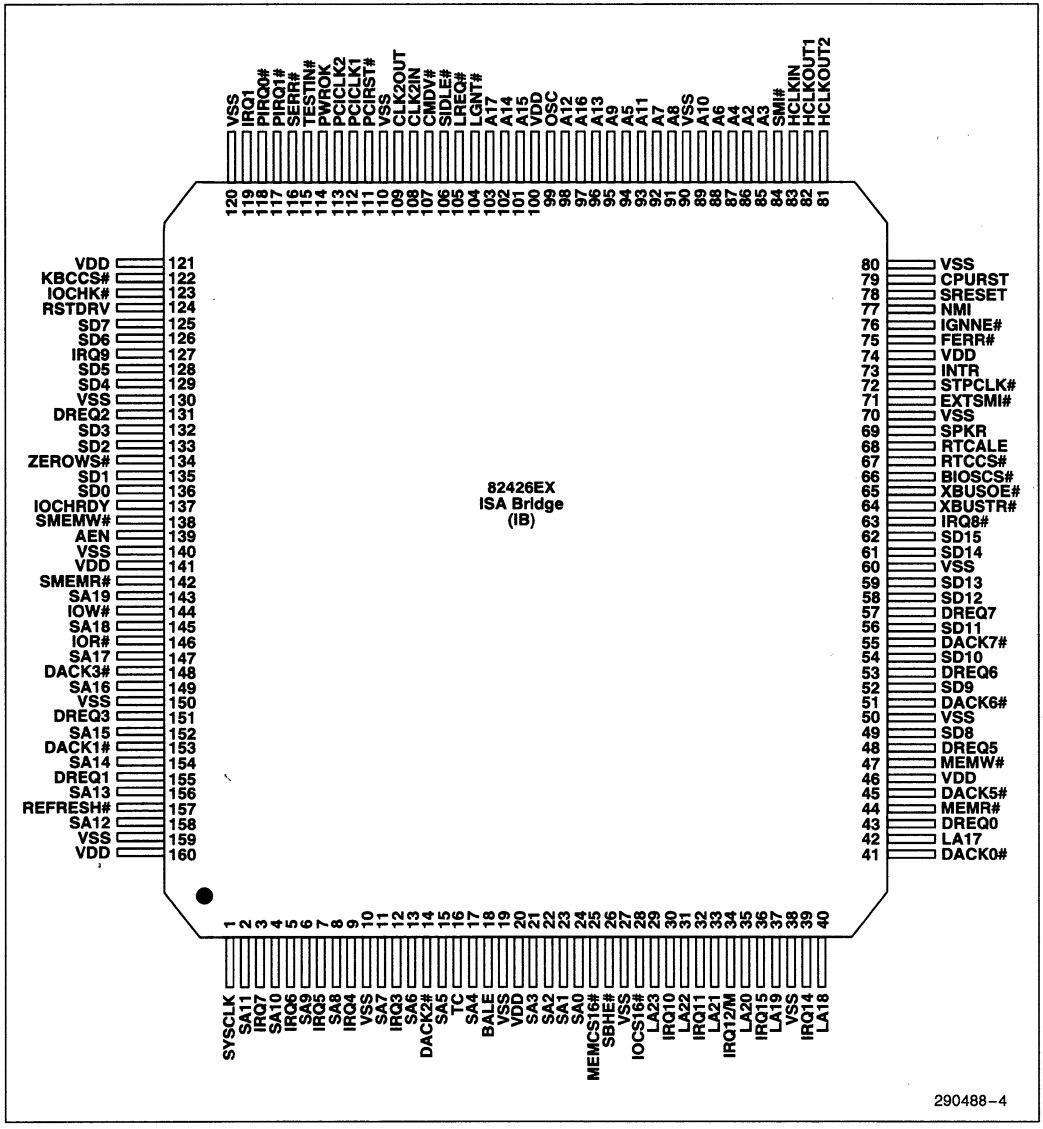


Figure 3. IB Pin Assignment

Table 3. Alphabetical IB Pin Assignment List

Pin Name	Pin #	I/O
A2	86	I/O
A3	85	I/O
A4	87	I/O
A5	94	I/O
A6	88	I/O
A7	92	I/O
A8	91	I/O
A9	95	I/O
A10	89	I/O
A11	93	I/O
A12	98	I/O
A13	96	I/O
A14	102	I/O
A15	101	I/O
A16	97	I/O
A17	103	I/O
AEN	139	O
BALE	18	O
BIOSCS#	66	O
CLK2IN	108	I
CLK2OUT	109	O
CMDV#	107	I/O
CPURST	79	O
DACK0#	41	O
DACK1#	153	O
DACK2#	14	O
DACK3#	148	O
DACK5#	45	O
DACK6#	51	O
DACK7#	55	O
DREQ0	43	I
DREQ1	155	I
DREQ2	131	I
DREQ3	151	I
DREQ5	48	I
DREQ6	53	I
DREQ7	57	I
EXTSMI#	71	IS
FERR#	75	I
HCLKIN	83	I
HCLKOUT1	82	O
HCLKOUT2	81	O
IGNNE#	76	O
INTR	73	O
IOCHK#	123	I
IOCHRDY	137	I/O
IOCS16#	28	I
IOR#	146	I/O
IOW#	144	I/O
IRQ1	119	I
IRQ3	12	I
IRQ4	9	I
IRQ5	7	I
IRQ6	5	I
IRQ7	3	I
IRQ8#	63	I
IRQ9	127	I
IRQ10	30	I
IRQ11	32	I
IRQ12/M	34	I
IRQ14	39	I
IRQ15	36	I
KBCCS#	122	O
LA17	42	I/O
LA18	40	I/O
LA19	37	I/O
LA20	35	I/O
LA21	33	I/O
LA22	31	I/O
LA23	29	I/O
LGNT#	104	I
LREQ#	105	O
MEMCS16#	25	I/O
MEMR#	44	I/O
MEMW#	47	I/O
NMI	77	O
OSC	99	I
PCICLK1	112	O
PCICLK2	113	O
PCIRST#	111	O
PIRQ0#	118	I
PIRQ1#	117	I
PWROK	114	IS
REFRESH#	157	I/O
RSTDRV	124	O
RTCALE	68	O
RTCCS#	67	O
SA0	24	I/O
SA1	23	I/O
SA2	22	I/O
SA3	21	I/O
SA4	17	I/O
SA5	15	I/O
SA6	13	I/O
SA7	11	I/O
SA8	8	I/O
SA9	6	I/O
SA10	4	I/O
SA11	2	I/O
SA12	158	I/O
SA13	156	I/O
SA14	154	I/O
SA15	152	I/O
SA16	149	I/O
SA17	147	I/O
SA18	145	I/O
SA19	143	I/O
SBHE#	26	I/O
SD0	136	I/O
SD1	135	I/O
SD2	133	I/O
SD3	132	I/O
SD4	129	I/O
SD5	128	I/O
SD6	126	I/O
SD7	125	I/O
SD8	49	I/O
SD9	52	I/O
SD10	54	I/O
SD11	56	I/O

Table 3. Alphabetical IB Pin Assignment List (Continued)

Pin Name	Pin #	I/O
SD12	58	I/O
SD13	59	I/O
SD14	61	I/O
SD15	62	I/O
SERR#	116	I
SIDLE#	106	I/O
SMEMR#	142	O
SMEMW#	138	O
SMI#	84	O
SPKR	69	O

Pin Name	Pin #	I/O
SRESET	78	I
STPCLK#	72	O
SYSCLK	1	O
TC	16	O
TESTIN#	115	I
V_{DD}	20	V
V_{DD}	46	V
V_{DD}	74	V
V_{DD}	100	V
V_{DD}	121	V

Pin Name	Pin #	I/O
V_{DD}	141	V
V_{DD}	160	V
V_{SS}	10	V
V_{SS}	19	V
V_{SS}	27	V
V_{SS}	38	V
V_{SS}	50	V
V_{SS}	60	V
V_{SS}	70	V
V_{SS}	80	V

Pin Name	Pin #	I/O
V_{SS}	90	V
V_{SS}	110	V
V_{SS}	120	V
V_{SS}	130	V
V_{SS}	140	V
V_{SS}	150	V
V_{SS}	159	V
XBUSOE#	65	O
XBUSTR#	64	O
ZEROWS#	134	I

Table 4. Numerical IB Pin Assignment List

Pin Name	Pin #	I/O	Pin Name	Pin #	I/O	Pin Name	Pin #	I/O	Pin Name	Pin #	I/O
SYSCLK	1	O	LA22	31	I/O	SD14	61	I/O	A8	91	I/O
SA11	2	I/O	IRQ11	32	I	SD15	62	I/O	A7	92	I/O
IRQ7	3	I	LA21	33	I/O	IRQ8#	63	I	A11	93	I/O
SA10	4	I/O	IRQ12/M	34	I	XBUSTR#	64	O	A5	94	I/O
IRQ6	5	I	LA20	35	I/O	XBUSOE#	65	O	A9	95	I/O
SA9	6	I/O	IRQ15	36	I	BIOSCS#	66	O	A13	96	I/O
IRQ5	7	I	LA19	37	I/O	RTCCS#	67	O	A16	97	I/O
SA8	8	I/O	V_{SS}	38	V	RTCALE	68	O	A12	98	I/O
IRQ4	9	I	IRQ14	39	I	SPKR	69	O	OSC	99	I
V_{SS}	10	V	LA18	40	I/O	V_{SS}	70	V	V_{DD}	100	V
SA7	11	I/O	DACK0#	41	O	EXTSMI#	71	I	A15	101	I/O
IRQ3	12	I	LA17	42	I/O	STPCLK#	72	O	A14	102	I/O
SA6	13	I/O	DREQ0	43	I	INTR	73	O	A17	103	I/O
DACK2#	14	O	MEMR#	44	I/O	V_{DD}	74	V	LGNT#	104	I
SA5	15	I/O	DACK5#	45	O	FERR#	75	I	LREQ#	105	O
TC	16	O	V_{DD}	46	V	IGNNE#	76	O	SIDLE#	106	I/O
SA4	17	I/O	MEMW#	47	I/O	NMI	77	O	CMDV#	107	I/O
BALE	18	O	DREQ5	48	I	SRESET	78	I	CLK2IN	108	I
V_{SS}	19	V	SD8	49	I/O	CPURST	79	O	CLK2OUT	109	O
V_{DD}	20	V	V_{SS}	50	V	V_{SS}	80	V	V_{SS}	110	V
SA3	21	I/O	DACK6#	51	O	HCLKOUT2	81	O	PCIRST#	111	O
SA2	22	I/O	SD9	52	I/O	HCLKOUT1	82	O	PCICLK1	112	O
SA1	23	I/O	DREQ6	53	I	HCLKIN	83	I	PCICLK2	113	O
SA0	24	I/O	SD10	54	I/O	SMI#	84	O	PWROK	114	I
MEMCS16#	25	I/O	DACK7#	55	O	A3	85	I/O	TESTIN#	115	I
SBHE#	26	I/O	SD11	56	I/O	A2	86	I/O	SERR#	116	I
V_{SS}	27	V	DREQ7	57	I	A4	87	I/O	PIRQ1#	117	I
IOCS16#	28	I	SD12	58	I/O	A6	88	I/O	PIRQ0#	118	I
LA23	29	I/O	SD13	59	I/O	A10	89	I/O	IRQ1	119	I
IRQ10	30	I	V_{SS}	60	V	V_{SS}	90	V	V_{SS}	120	V

Table 4. Numerical IB Pin Assignment List (Continued)

Pin Name	Pin #	I/O
V_{DD}	121	V
KBCCS#	122	O
IOCHK#	123	I
RSTDRV	124	O
SD7	125	I/O
SD6	126	I/O
IRQ9	127	I
SD5	128	I/O
SD4	129	I/O
V_{SS}	130	V

Pin Name	Pin #	I/O
DREQ2	131	I
SD3	132	I/O
SD2	133	I/O
ZEROWS#	134	I
SD1	135	I/O
SD0	136	I/O
IOCHRDY	137	I/O
SMEMW#	138	O
AEN	139	O
V_{SS}	140	V

Pin Name	Pin #	I/O
V_{DD}	141	V
SMEMR#	142	O
SA19	143	I/O
IOW#	144	I/O
SA18	145	I/O
IOR#	146	I/O
SA17	147	I/O
DACK3#	148	O
SA16	149	I/O
V_{SS}	150	V

Pin Name	Pin #	I/O
DREQ3	151	I
SA15	152	I/O
DACK1#	153	O
SA14	154	I/O
DREQ1	155	I
SA13	156	I/O
REFRESH#	157	I/O
SA12	158	I/O
V_{SS}	159	V
V_{DD}	160	V

2.0 SIGNAL DESCRIPTION

This section contains a detailed description of each signal. The PSC signals are presented first, followed by the IB signals. The signals are arranged in functional groups according to their interface.

Note that the "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used extensively. This is done to avoid confusion when working with a mixture of "active-low" and "active-high" signals. The term **assert**, or **assertion** indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term **negate**, or **negation** indicates that a signal is inactive.

The following notations are used to describe signal types.

Signal Type	Description
I	**Input.** Standard input-only signal.
IS	**Input.** Schmitt Trigger
O	**Totem Pole Output.** Standard active driver.
OD	**Open Drain.** Input/Output
I/O	**Input/Output.** Bi-directional, tri-state pin.
s/t/s	**Sustained Tri-state.** Active low, tri-state signal with a pullup. Must be driven high for a clock before tri-state. Turn-around time must be maintained.

2.1 PSC Signals

2.1.1 HOST CPU INTERFACE SIGNALS (PSC)

Name	Type	Description
SRESET/ INIT	O	**SOFT RESET/INITIALIZE:** This is the soft reset output of the PSC and should be connected to the SRESET or INIT input to the CPU, depending on the CPU type.
A[31:30, 26:2]	I/O	**HOST ADDRESS:** A[31:30,26:2] are used as inputs to the PSC for CPU driven cycles. A[31:30,26:4] are outputs during Snoop cycles. Note that A[29:27] are not driven by the PSC. These signal lines must be externally driven low by either weak pull-down resistors or by driving these lines low when HLDA is active asserted. A[17:2] are also used for PSC/IB Link Interface transfers. These signals are tri-stated after a hard reset.
HD[31:0]	I/O	**HOST DATA:** HD[31:0] are connected to the host CPU data bus. These signals are inputs after a hard reset.
HDP[3:0]	I/O	**HOST DATA PARITY:** HP[3:0] are bi-directional parity signals for the host data bus. These signals provide parity to the PSC during main memory read cycles. The PSC sends parity information to main memory during non-CPU main memory write cycles. These signals are tri-stated after a hard reset.
BE[3:0]#	I/O	**BYTE ENABLE:** The Byte Enable signals indicate active bytes during read and write cycles. These signals are tri-stated after a hard reset.
M/IO# D/C# W/R#	I/O I I/O	**BUS CYCLE DEFINITION (Memory/Input-Output, Data/Code, Write/Read:** These signals define the Host Bus cycle. Note that special cycles are identified by BE[3:0]# and A[4:2]. These signals are tri-stated after a hard reset.

2.1.1 HOST CPU INTERFACE SIGNALS (PSC) (Continued)

Name	Type	Description
PCD/ CACHE#	I	**PAGE CACHE DISABLE/CACHE:** This multiplexed signal pin has two functions, depending on the type of CPU used. The **PCD** input signal, when asserted, indicates the current cycle can not be cached in the L2 cache during a cache line fill operation. When PCD is asserted the line will not be cached in L1 or L2. The **CACHE#** signal is active along with the first ADS# until the first RDY# or BRDY#. For line fills, the functionality of the CACHE# signal is identical to that of the PCD signal. During write-back cycles, CACHE# is always asserted at the beginning of the line write-back. The beginning of a write-back cycle is uniquely identified by active ADS#, W/R# and CACHE#. Beginning of the snoop write-back is identified by the ADS#, W/R#, CACHE# and HITM# being active.
ADS#	I	**ADDRESS STATUS:** The ADS# input indicates that the bus cycle definition signals (M/IO#, D/C#, W/R#), BE[3:0]#, and A[31:30, 26:2] are available on their corresponding pins.
RDY#	O	**READY:** RDY# indicates that the current non-burst bus cycle is complete. This signal is negated after a hard reset.
BRDY#	O	**BURST READY:** BRDY performs the same function during a burst cycle that RDY# performs during a non-burst cycle. This signal is negated after hard reset.
BLAST#	I	**BURST LAST:** BLAST# indicates the end of a burst access for CPU-initiated cycles.
HOLD	O	**HOLD:** The PSC asserts HOLD to the CPU to request ownership of the Host Bus. This signal is negated after a hard reset.
HLDA	I	**HOLDA:** HLDA must be asserted by the CPU for the PSC to grant a new master on the PCI or ISA Buses. When HLDA is negated, the CPU is the Host Bus master and the PSC is the PCI Bus master. When HLDA is negated, the PSC is also the master on the PSC/IB link interface.
AHOLD	O	**ADDRESS HOLD:** The AHOLD output signal forces the CPU to float its address bus in the next clock. The PSC asserts this signal in preparation to perform a PSC/IB Interface transfer, when SRESET needs to be asserted, or upon Deturbo logic requests. This signal is negated after a hard reset.
EADS#	O	**EXTERNAL ADDRESS:** EADS#, when asserted, indicates that an external address has been driven onto the CPU address lines. This address is used to perform an internal cache snoop cycle. This signal is negated after a hard reset.
KEN#	O	**CACHE ENABLE:** KEN#, when asserted, indicates whether the current cycle is cacheable in the CPU internal (L1 or primary) cache. This signal is negated after a hard reset.
HITM#	I	**HIT MODIFIED:** HITM#, when asserted, indicates that a hit to a modified data cache has occurred during the snoop cycle. A pull-up is used to keep HITM# negated, when not used.

2.1.2 SECONDARY CACHE SIGNALS (PSC)

Name	Type	Description
CI3E CI3O2	O	**CACHE INDEX SIGNALS:** The Cache Index signals generate the burst sequence required by the CPU during secondary cache accesses. The PSC latches the starting burst address and internally generates subsequent dword addresses for the entire cache line. The CI3E signal is always used for cache index bit 3. When used in a bank interleaved configuration, CI3O2 is used to drive cache index bit 3 to the odd bank, and CI3E is used to drive bit 3 to the even bank. When used in non-interleaved mode (only one bank), CI3O2 is used to drive cache index bit 2.
CWE[1:0]#	O	**CACHE WRITE ENABLE:** CWE[1:0]# are used to enable single writes and line fills to be written into the L2 cache. CWE0# is driven to all SRAMs in the even bank and CWE1# is driven to all SRAMs in the odd bank. The chip select signals of the SRAMs are asserted based on the byte enable signals and the W/R# signal, which are gated externally. Thus, only the bytes selected by the CPU are written. When programmed for non-interleaved mode, CWE[1:0]# mirror each other and are asserted to both banks. These signals are negated after a hard reset.
COE[1:0]#	O	**CACHE OUTPUT ENABLE:** COE[1:0]# are used to perform read cycles from the cache data SRAMs. COE0# is connected to the output enable pins of the cache data SRAMs of the even bank. COE1# is connected to the output enable pins of the cache data SRAMs of the odd bank. When programmed for non-interleaved mode, COE[1:0]# mirror each other and are asserted to both banks. These signals are negated after a hard reset.
TWE#	O	**TAG WRITE ENABLE:** TWE# is connected to the tag SRAM write enable (WE#) pin. TWE# is asserted during CPU read-miss cycles when a cache line is allocated and during write-hit cycles, when the Dirty (Modified) bit of the tag is updated. This signal is negated after a hard reset.
TAG[8:0]	I/O	**CACHE TAG:** TAG[8:0] are directly connected to the tag SRAM data bus. The L2 cache size determines the relationship between TAG[7:0] and the A[26:16] host address signals (see Section 4.0, Functional Description). TAG8 is always used as the Dirty (Modified) bit for the write-back L2 cache.

2.1.3 PCI SIGNALS (PSC)

Name	Type	Description
AD[31:0]	I/O	**ADDRESS/DATA:** AD[31:0] are connected to the PCI multiplexed address/data bus. These signals are also multiplexed with the IDE interface (refer to the section on PCI Bus IDE Signals). These signals are driven high after a hard reset.
C/BE[3:0]#	I/O	**BUS COMMAND/BYTE ENABLE:** PCI Bus commands (C) and Byte Enables (BE[3:0]#) are multiplexed on the same pins. PCI local bus command encoding and types are listed in Section 4.0, Functional Description. These signals are driven high after a hard reset.
FRAME#	I/O s/t/s	**FRAME:** FRAME# is an output when the PSC is a master on the PCI bus. FRAME indicates that a PCI cycle has started. This signal is tri-stated after a hard reset.
TRDY#	I/O s/t/s	**TARGET READY:** TRDY# is an input when PSC is a master on the PCI Bus. TRDY# is an output when the PSC acts as a PCI slave. TRDY# indicates that the target device is ready. This signal is tri-stated after a hard reset.
IRDY#	I/O s/t/s	**INITIATOR READY:** IRDY# is an output when PSC is a PCI master. IRDY# is an input when the PSC is a PCI slave. IRDY# indicates that the initiator of the cycle is ready. This signal is tri-stated after a hard reset.
LOCK#	I	**LOCK:** LOCK# indicates an exclusive bus operation and may require multiple transactions to complete. The PSC supports a bus type of LOCK only. Thus, when a PCI master locks the PCI Bus, it owns the system for the duration of the locked transactions.
STOP#	I/O s/t/s	**STOP:** STOP# indicates that the current bus target is requesting the master to stop the current transaction. STOP# is used for disconnect, retry, and abort sequences on the PCI Bus. This signal is tri-stated after a hard reset.
PAR	I/O	**PARITY:** PAR is driven by the PSC, as a PCI master, during the address and data phases for a write cycle and during the address phase for a read cycle. When the PSC is a PCI slave, parity is driven by the PSC for the data phase of a PCI read cycle. Parity is even parity across AD[31:0] and C/BE[3:0]#. PAR lags the corresponding address or data phase by 1 PCICLK. This signal is asserted after a hard reset.
SERR#	OC	**SYSTEM ERROR:** SERR#, when driven by the PSC, indicates that either a main memory parity error occurred or the PSC, as a master, received a target abort.
DEVSEL#	I/O s/t/s	**DEVICE SELECT:** DEVSEL#, when asserted, indicates that a PCI slave device has decoded the bus cycle address as the target of the current access. The PSC drives DEVSEL# based on the main memory address range being accessed by a PCI master. As an input, DEVSEL# indicates whether any device on the bus has been selected. This signal is tri-stated after a hard reset.

2.1.4 SYSTEM POWER MANAGEMENT (SMM) SIGNALS (PSC)

Name	Type	Description
SMI#	I	**SYSTEM MANAGEMENT INTERRUPT:** SMI#, when asserted, indicates that there is an active SMI#. It is used, along with SMIACT#, to block SRESET.
SMIACT#	I	**SYSTEM MANAGEMENT INTERRUPT ACTIVE:** SMIACT# indicates that the system is running in system management mode. SMIACT# is used by the PSC to access the SMRAM for CPU-initiated cycles. While SMIACT# is active, SRESET and A20M# must be blocked.

2.1.5 DRAM CONTROL SIGNALS (PSC)

Name	Type	Description
MA[10:0]	O	**MULTIPLEXED DRAM ADDRESS:** The MA[10:0] bus provides row and column address information to the main memory DRAMs.
RAS[4:0]#	O	**ROW ADDRESS STROBE:** Each of the RAS[4:0]# output signals corresponds to one DRAM row of four or eight bytes. These signals are used to latch the row addresses on the MA[10:0] bus into the DRAMs. RAS[4:0]# drive the DRAMs directly, without any external buffers. These signals are negated after a hard reset.
CAS[7:0]#	O	**COLUMN ADDRESS STROBE:** CAS[7:0]# are used to latch the column addresses on the MA[10:0] bus into the DRAMs. CAS[7:0]# drive the DRAMs directly, without any external buffers. These signals are negated after a hard reset.
WE#	O	**DRAM WRITE ENABLE:** WE# is externally buffered when MA[10:0] are externally buffered. This signal is asserted after a hard reset.

2.1.6 PSC/IB LINK INTERFACE (PSC)

See Section 2.2.7, PSC/IB Link Interface Signals (IB).

2.1.7 PCI BUS ARBITRATION/HOST BUS SLAVE DEVICE (PSC)

Name	Type	Description
PREQ1#/ HDEV#	I	**REQUEST1/HOST DEVICE:** This multiplexed signal has two functions. **PREQ1#** is used by the PCI master to gain control of the PCI Bus. This signal can be externally cascaded to support multiple PCI masters. The **HDEV#** function is used when the PSC is programmed to support a Host Bus slave device.
PREQ0#	I	**REQUEST0:** PREQ0# is used by PCI master to gain control of the PCI Bus. This signal can be externally cascaded to support multiple PCI masters.
PGNT1# HRDY#	I/O	**GRANT1/HOST READY: PGNT1#** is driven by the PSC to grant control of the PCI Bus to a PCI master. PGNT1# can be externally cascaded to support multiple PCI masters. The **HRDY#** function is used when the PSC is programmed to support a Host Bus slave device. This signal is driven high during and after a hard reset.
PGNT0#	O	**GRANT0:** PGNT0# is driven by the PSC to grant control of the PCI Bus to a PCI master. PGNT0# can be externally cascaded to support multiple PCI masters. This signal is driven high during and after a hard reset.

2.1.8 PCI BUS IDE (PSC)

LBIDE# is the only signal dedicated to PCI Bus IDE support. This pin is used to control the output enable of the 245 data transceivers and 244 control signal buffer. The other signals that support the IDE are shared with the PCI AD lines.

PCI Signal ADName	PCI IDE Signal Name	Type	Description
NA	LBIDE#	O	**LOCAL BUS IDE:** LBIDE# controls the output enables of the data transceivers and control signal buffers during accesses to the PCI local bus IDE path.
AD31	IDE1CS#	O	**IDE 1XX CHIP SELECT:** When the primary PCI local bus IDE is enabled, this signal is asserted for accesses to I/O addresses 1F0–1F7h. When the secondary PCI local bus IDE is enabled, this signal is asserted for an I/O cycle to addresses 170–177h.
AD30	IDE3CS#	O	**IDE 3XX CHIP SELECT:** When the primary PCI local bus IDE is enabled, this signal is asserted for accesses to I/O addresses 3F6,3F7h. When the secondary PCI local bus IDE is enabled this signal is asserted for accesses to I/O addresses 376,377h.
AD29	DIR	O	**DIRECTION:** DIR controls the direction of the data transceivers connected to the IDE connector. This signal is driven high for IDE reads and low for IDE writes.
AD28	IORDY	I	**IO READY:** IORDY allows the IDE drive to extend the cycle. The IDE cycle is held in wait-states as long as IORDY is sampled low. This input is synchronous to the first sample point, but asynchronous to subsequent sample points.
AD(27:25)	IDEA(2:0)	O	**IDE ADDRESS [2:0]:** These outputs are the A[2:0] signals that select individual ports on the IDE drive.
AD24	IOR#	O	**I/O READ STROBE:** IOR# is asserted for PCI local bus IDE I/O read cycles.
AD23	IOW#	O	**I/O WRITE STROBE:** IOW# is asserted for PCI local bus IDE I/O write cycles.
AD(15:0)	IDED(15:0)	I/O	**IDE DATA:** These bi-directional signals output data during IDE write cycles and input data during PCI local bus IDE read cycles.

2.1.9 CLOCKS AND RESET (PSC)

Name	Type	Description
PCICLKIN	I	**PCI CLOCK INPUT:** PCICLKIN is the clock input used by the PCI interface. PCI clock frequency can be configured to be the same or half the Host Bus frequency.
HCLKIN	I	**HOST BUS CLOCK INPUT:** HCLKIN is used for the Host Bus, L2 cache, PSC/IB Link and DRAM interfaces. Host Bus frequency can be configured to be the same or twice the PCI clock frequency.
CLK2IN	I	**CLOCK 2 INPUT:** CLK2IN is a 2X clock that is used during L2 cache writes.
CPURST	I	**CPU RESET:** CPURST is used as an input to place the PSC in a known state. CPURST is driven by the IB when PWROK is negated or when hard reset is driven by software through the TRC Register.
KBDRST#	I	**KEYBOARD RESET:** This signal is an input from the keyboard controller and is used to generate a soft reset to the CPU.

2.2 IB Signals

2.2.1 ISA INTERFACE SIGNALS (IB)

Name	Type	Description
BALE	O	**BUS ADDRESS LATCH ENABLE:** BALE is asserted by the IB to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. This signal is negated after a hard reset.
AEN	O	**ADDRESS ENABLE:** AEN is asserted during DMA cycles to prevent I/O slaves from mis-interpreting DMA cycles as valid I/O cycles. This signal is also asserted during IB-initiated refresh cycles. This signal is negated after a hard reset.
SYSCLK	O	**SYSTEM CLOCK:** Refer to the Clock signal descriptions.
IOCHRDY	I/O	**I/O CHANNEL READY:** Resources on the ISA Bus negate IOCHRDY to indicate that additional time (wait-states) is required to complete the cycle. This signal is normally high on the ISA Bus. IOCHRDY is an input when the IB owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave or during DMA transfers. IOCHRDY is output when an external ISA Bus master owns the ISA Bus and is accessing main memory or an IB register. As an IB output, IOCHRDY is negated from the falling edge of the ISA commands. After data is available for an ISA master read or the IB latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, the IB tri-states IOCHRDY. The IB does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. IOCHRDY is tri-stated upon CPURST.
IOCS16#	I	**16-BIT I/O CHIP SELECT:** This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles.
IOCHK#	I	**I/O CHANNEL CHECK:** IOCHK# can be driven by any resource on the ISA Bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA Bus. If IOCHK# is asserted and NMIs are enabled (via the NMISC and NMIERTC Registers), an NMI is generated to the CPU.

2.2.1 ISA INTERFACE SIGNALS (IB) (Continued)

Name	Type	Description
IOR#	I/O	**I/O READ:** IOR# asserted indicates to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when the IB owns the ISA Bus. IOR# is an input when an external ISA master owns the ISA Bus. This signal is negated after a hard reset.
IOW#	I/O	**I/O WRITE:** IOW# asserted indicates to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when the IB owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. This signal is negated after a hard reset.
LA[23:17]	I/O	**UNLATCHED ADDRESS:** These bi-directional address lines allow accesses to physical memory on the ISA Bus up to 16 MBytes. LA[23:17] are outputs when the IB owns the ISA Bus. The LA[23:17] lines become inputs when an ISA master owns the ISA Bus. The LA[23:17] signals are driven to an unknown state after a hard reset.
SA[19:0]	I/O	**SYSTEM ADDRESS BUS:** SA[19:0] are outputs when the IB owns the ISA Bus. SA[19:0] are inputs when an external ISA master owns the ISA Bus. Note that SA[19:17] have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used. SA[19:0] are driven to an unknown state after a hard reset.
SBHE#	I/O	**SYSTEM BYTE HIGH ENABLE:** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when the IB owns the ISA Bus and an input when an external ISA master owns the ISA Bus. This signal is at an unknown state after a hard reset.
MEMCS16#	OD	**MEMORY CHIP SELECT 16:** ISA slaves that are 16-bit memory devices drive this signal low. MEMCS16# is an input when the IB owns the ISA Bus. MEMCS16# is an output when an ISA Bus master owns the ISA Bus. The IB drives this signal low during ISA master to main memory cycles.
MEMR#	I/O	**MEMORY READ:** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when the IB is a master on the ISA Bus and an input when an ISA master, other than the IB, owns the ISA Bus. This signal is also driven by the IB during refresh cycles. For DMA cycles, the IB, as a master, asserts MEMR#. This signal is tri-stated after a hard reset.
MEMW#	I/O	**MEMORY WRITE:** MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when the IB owns the ISA Bus and an input when an ISA master, other than the IB, owns the ISA Bus. For DMA cycles, the IB, as a master, asserts MEMW#. This signal is tri-stated after a hard reset.
SMEMR#	O	**STANDARD MEMORY READ:** The IB asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1 MByte range (00000000–000FFFFFh) during DMA compatible, IB master, or ISA master cycles, the IB asserts SMEMR#. SMEMR# is a delayed version of MEMR#. This signal is negated after a hard reset.
SMEMW#	O	**STANDARD MEMORY WRITE:** The IB asserts SMEMW# to request an ISA memory slave to accept data from the data lines. If the access is below the 1 MByte range (00000000–000FFFFFh) during DMA compatible, IB master, or ISA master cycles, the IB asserts SMEMW#. SMEMW# is a delayed version of MEMW#. This signal is negated after a hard reset.

2.2.1 ISA INTERFACE SIGNALS (IB) (Continued)

Name	Type	Description
ZEROWS#	I	**ZERO WAIT-STATES:** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. If IOCHRDY is negated and ZEROWS# is asserted during the same clock, then ZEROWS# is ignored and wait-states are added as a function of IOCHRDY (i.e., IOCHRDY has precedence over ZEROWS#).
SD[15:0]	I/O	**SYSTEM DATA:** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. These signals are tri-stated after a hard reset.

2.2.2 NMI SIGNALS (IB)

Name	Type	Description
NMI	O	**NON-MASKABLE INTERRUPT:** NMI is used to force a non-maskable interrupt to the CPU. The IB generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. NMI generation can be globally disabled. This signal is negated after a hard reset.
SERR#	I	**SYSTEM ERROR:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the IB generates a non-maskable interrupt (NMI) to the CPU.

2.2.3 DMA SIGNALS (IB)

Name	Type	Description
DREQ [3:0,7:5]	I	**DMA REQUEST:** The DREQ lines are used to request DMA service from the IB's DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA Command Register. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted.
DACK# [3:0, 7:5]	O	**DMA ACKNOWLEDGE:** The DACK output lines indicate that a request for DMA service has been granted by the IB or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA Command Register. These signals are negated after a hard reset.
TC	O	**TERMINAL COUNT:** The IB asserts TC to DMA slaves as a terminal count indicator. This signal is negated after a hard reset.
REFRESH#	I/O	**REFRESH:** As an output, REFRESH# asserted indicates when a refresh cycle is in progress. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when the IB DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. This signal is tri-stated after a hard reset.

2.2.4 TIMER/COUNTER SIGNALS (IB)

Name	Type	Description
SPKR	O	**SPEAKER DRIVE:** This signal drives an external speaker driver device, which in turn drives the ISA system speaker. This signal can be enabled/disabled via the NMI Status and Control Register. When enabled, the SPKR signal is the output of counter 2. This signal is negated after a hard reset.
OSC	I	**OSCILLATOR:** The oscillator is the 14.31818 MHz ISA clock signal. It is used by the internal 82C54 Timer, counters 0, 1, and 2.

2.2.5 INTERRUPT CONTROLLER SIGNALS (IB)

Name	Type	Description
IRQ[15,14, 11:9,7:3,1]	IS	**INTERRUPT REQUEST:** The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU. The assertion mode (edge or level triggered) is selected via the Edge/Level Triggered 1 Register and Edge/Level Triggered 2 Register. For edge triggered mode, a low-to-high transition on the IRQ line is recognized as an interrupt request. For level triggered mode, a low level on the IRQ line is recognized as an interrupt request. IRQ[8#,2:0] and the internal IRQ13 (FERR#) are not programmable through the ELCR registers. These IRQ's, with the exception of IRQ8#, are always active high edge triggered and can not be modified by software. IRQ8# is always active low edge sensitive. A low-to-high transition on IRQ1 is latched by the IB. The IB continues to generate an internal IRQ1 to the 8259 core until a CPURST or an I/O read access to port 60h is detected. These signals are placed in edge triggered mode after a hard reset.
IRQ8#	IS	**INTERRUPT REQUEST 8:** IRQ8# is always an active low edge triggered interrupt input (i.e. this interrupt can not be modified by software).
IRQ12/M	IS	**INTERRUPT REQUEST 12/MOUSE INTERRUPT:** Refer to the X-Bus Signal Description.
PIRQ[0,1]#	IS	**PROGRAMMABLE INTERRUPT REQUEST:** The PIRQ0 and PIRQ1 signals can be shared with interrupts IRQ[15,14,12:9,7:3]. The routing is controlled by the PIRQ Route Control Registers. Each PIRQx# line has a separate Route Control Register. These signals require external pull-up resistors.
INTR	O	**CPU INTERRUPT:** The IB asserts INTR to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or HCLKIN. The interrupt controller must be programmed following reset to ensure that INTR is at a known state. This signal is negated after a hard reset.

2.2.6 X-BUS SIGNALS (IB)

Name	Type	Description
XBUSTR#	O	**X-BUS DATA TRANSMIT/RECEIVE:** XBUSTR# is tied directly to the direction control of a 74F245 that buffers the X-Bus data (XD[7:0]). XBUSTR# is asserted for all I/O read cycles, regardless if the access is to an IB supported device. XBUSTR# is asserted for memory cycles only if BIOS space has been decoded. This signal is negated after a hard reset.
XBUSOE#	O	**X-BUS OUTPUT ENABLE:** XBUSOE# is tied directly to the output enable of a 74F245 that buffers the X-Bus data (XD[7:0]), from the system data bus, SD[7:0]. XBUSOE# is asserted anytime an IB supported X-Bus device is decoded, and the devices decode is enabled in the X-Bus Chip Select Enable Register (XBCSA Register). This signal is negated after a hard reset.
KBCCS#	O	**KEYBOARD CONTROLLER CHIP SELECT:** This signal is asserted during read or write accesses to KBC locations 60h, 62h, 64h, or 66h. This signal is negated after a hard reset.
BIOSCS#	O	**BIOS CHIP SELECT:** This signal is asserted during read or write accesses to BIOS. During DMA cycles, BIOSCS# is not generated. This signal is negated after a hard reset.
RTCCS#	O	**REAL TIME CLOCK CHIP SELECT:** This signal is asserted during read or write accesses to RTC location 71h. RTCALE can be tied to a pair of external OR gates to generate the real time clock read and write command signals. This signal is negated after a hard reset.
RTCALE	O	**REAL TIME CLOCK ADDRESS LATCH:** RTCALE latches the appropriate memory address into the RTC. A write to port 70h with the appropriate RTC memory address that will be written to or read from, causes RTCALE to be asserted. RTCALE is asserted based on IOW# falling, and remains asserted for two SYSCLKs. This signal is negated after a hard reset.
IGNNE#	O	**IGNORE ERROR:** This signal is connected to the ignore error pin on the CPU. IGNNE# is only used if the IB coprocessor error reporting function is enabled in the XBCSA Register (bit 5 = 1). This signal is negated after a hard reset.
FERR#	IS	**NUMERIC COPROCESSOR ERROR:** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the CPU. FERR# is only used if the IB coprocessor error reporting function is enabled in the XBCSA Register (bit 5 = 1). FERR# has a weak internal pull-up resistor to ensure a high level when the coprocessor error function is disabled.
IRQ12/M	IS	**INTERRUPT REQUEST/MOUSE INTERRUPT:** In addition to providing the standard interrupt function as described in the signal description for IRQ[15,14, 11:9, 7:3, 1], the IRQ12/M signal also provides a mouse interrupt function. The X-Bus Chip Select Register determines the functionality of IRQ12/M. An internal IRQ12 interrupt continues to be generated until a reset or an I/O read access to address 60h (falling edge of IOR#) is detected. After a reset, this pin provides the standard IRQ12 function.

2.2.7 PSC/IB LINK INTERFACE SIGNALS (IB)

Name	Type	Description
CMDV#	I/O	**COMMAND VALID:** The link master (PSC or IB) asserts CMDV# to indicate the beginning of a link transfer. The PSC negates this signal after a hard reset. CMDV# is used along with SIDLE# to set the PSC/IB system clock configuration during a PWROK hard reset. These inputs are strapped to the appropriate levels, sampled while PWROK is inactive, and latched when PWROK goes active (see Section 4.0, Functional Description).
SIDLE#	I/O	**SLAVE IDLE:** The link slave (PSC or IB) asserts SIDLE# to indicate that it is available for data transfers. The IB asserts this signal after a hard reset. SIDLE# is used along with CMDV# to set the PSC/IB system clock configuration during PWROK hard reset. These inputs are strapped to the appropriate levels, sampled while PWROK is inactive, and latched when PWROK goes active (see Section 4.0, Functional Description).
LREQ#	O	**LINK REQUEST:** The IB asserts LREQ# to request a link transfer. This signal is negated after a hard reset.
LGNT#	I	**LINK GRANT:** The PSC asserts LGNT# to grant the IB a link transfer. This signal is negated after a hard reset.
A[17:2]	I/O	**HOST ADDRESS/LINK:** For PSC/IB Link transfers, A[17:2] transfer data/commands between the IB and PSC. These signals are tri-stated after a hard reset.

2.2.8 SYSTEM POWER MANAGEMENT (SMM) SIGNALS (IB)

Name	Type	Description
SMI#	O	**SYSTEM MANAGEMENT INTERRUPT:** SMI# is an active low synchronous output that is asserted by the IB in response to one of many enabled hardware or software events. SMI# is ORed externally with SRESET and driven to the CPU. This signal is negated after a hard reset.
STPCLK#	O	**STOP CLOCK:** STPCLK# is an active low synchronous output that is asserted by the IB in response to one of many enableable hardware or software events. STPCLK# connects directly to the CPU. This signal is negated after a hard reset.
EXTSMI#	I	**EXTERNAL SYSTEM MANAGEMENT INTERRUPT:** EXTSMI# is a falling edge triggered input to the IB indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to the IB. However, when the setup and hold times are met it is only required to be asserted for one HCLKIN. Once negated it must remain negated for at least four HCLKINs in order to allow the edge detect logic to reset.

2.2.9 SYSTEM CLOCK SIGNALS (IB)

Name	Type	Description
CLK2IN	I	**2X CLOCK IN:** CLK2IN is a 2X clock input. CLK2IN is divided as shown in Section 4.0, Functional Description, to generate HCLKIN, PCICLK, and SYSCLK.
CLK2OUT	O	**2X Clock Out:** CLK2OUT is a delayed version of CLK2IN. The PSC uses this clock.
HCLKOUT[2,1]	O	**HOST CLOCK OUT:** HCLKOUT[2,1] provide the reference clock for the IB, PSC, and CPU devices. The IB divides the CLK2IN input to generate HCLKOUT[2,1]. Either HCLKOUT2 or HCLKOUT1 is routed back to the IB's HCLKIN input providing the IB with its HCLKIN reference.
HCLKIN	I	**HOST CLOCK IN:** This 1X clock input provides the fundamental timing and internal operating frequency for the IB. This signal is connected as a feedback from the HCLKOUT outputs. The IB operates at 25 MHz or 33 MHz, depending on the frequency of the CLK2IN input.
PCICLK[2,1]	O	**PCI CLOCK OUT:** PCICLK[2,1] provide the reference clock for the PSC and PCI devices. The IB divides the CLK2IN input to generate PCICLK[2,1]. The PCI Bus operates at 25 MHz or 33 MHz, depending on the frequency of the CLK2IN input.
SYSCLK	O	**ISA SYSTEM CLOCK:** SYSCLK is the reference clock for the ISA Bus. It drives the ISA Bus directly. The SYSCLK frequencies supported are 8 MHz and 8.33 MHz.

2.2.10 SYSTEM RESET SIGNALS (IB)

Name	Type	Description
PWROK	I	**POWER OK:** When asserted, PWROK is an indication to the IB that power and CLK2IN have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the IB asserts CPURST, PCIRST# and RSTDRV. The IB also uses the rising edge of PWROK to sample the CMDV# and SIDLE# signals to determine the HCLKIN, PCICLK, and SYSCLK divisor values.
CPURST	O	**CPU RESET:** The IB asserts CPURST to reset the CPU, IB, and PSC. The IB asserts CPURST during power-up and when a hard reset sequence is initiated through the TRC Register. If a hard reset is initiated through the TRC register, the IB resets it's internal registers and signals to their default state, but maintains its clock divisor values.
SRESET	I	**Soft Reset:** SRESET is used internally by the IB.
PCIRST#	O	**PCI RESET:** The IB asserts PCIRST# to reset devices that reside on the PCI bus. The IB asserts PCIRST# during power-up and when a hard reset sequence is initiated through the TRC register. PCIRST# is driven asynchronously relative to PCICLK.
RSTDRV	O	**RESET DRIVE:** The IB asserts RSTDRV to reset devices that reside on the ISA Bus. The IB asserts this signal during a hard reset and during power-up.

2.2.11 TEST SIGNALS (IB)

Name	Type	Description
TESTIN#	I	**TEST:** The TESTIN# signal is used to tri-state all of the IB outputs. During normal operation, this input should be pulled up.

3.0 REGISTER DESCRIPTION

The 82420EX PCIset contains I/O control registers, PCI configuration registers, and ISA Compatible registers. These registers are discussed in this section.

The PCIset, upon receiving a hard reset, sets its internal registers to pre-determined **default** states. The default values are indicated in the individual register descriptions. Note that the default state of some ISA-Compatible register bits is indeterminate after a hard reset.

The following notation is used to describe register access attributes:

RO **Read Only.** If a register is read only, writes have no effect.

WO **Write Only.** If a register is write only, reads have no effect.

R/W **Read/Write.** A register with this attribute can be read and written. Note that individual bits in some read/write registers may be read only.

3.1 Register Access

Table 5, Table 6, and Table 7 show the I/O assignments for the I/O Control Registers, PCI Configuration Registers, and the ISA-Compatible Registers. Little-endian ordering is used for all multi-byte accesses (i.e., lower addresses contain the least significant parts of the fields).

NOTE:
Aliasing of the 90–9Fh address range to 80–8Fh is enabled/disabled in the ISA Controller Recovery Timer Register. When aliasing is enabled, the IB aliases I/O accesses in the 90–9Fh range to the 80–8Fh range. In this case, the IB only forwards write accesses to these locations to the ISA Bus. When aliasing is disabled, the IB allows both read and write accesses to the 90–9Fh range to be forwarded to the ISA Bus (i.e. they are no longer considered IB internal registers). Note that port 92h is always a distinct ISA register in the 90–9Fh range and is always forwarded to the ISA Bus. In addition, when aliasing is disabled, ISA master accesses to the 90h–9Fh range are ignored by the IB.

I/O Control Registers

The I/O control registers (Table 5) are located in the CPU I/O space and can only be accessed by the CPU. The TRC and CONFDATA Registers can be accessed as byte, word, or dword quantities. The CONFADD Register can only be accessed as a dword quantity.

The CONFADD and CONFDATA Registers are used to access PCI configuration space. This is accomplished in two steps. First, the PCI configuration address is written to the CONFADD Register using the PCI configuration space access mechanism 1 address field definitions. Second, configuration register data is read/written from/to the CONFDATA Register address location.

The address written to the CONFADD Register contains five programmable fields (Bus Number, Device Number, Function Number, Configuration Register Offset, and the configuration enable bit—bit 31). If the Device Number = 05, the Bus Number = 00, and bit 31 = 1, subsequent CONFDATA Register accesses, read/write the PCI configuration register pointed to by the Register Offset field. If the Register Offset field points to a reserved register location, reads return all 0's to the CPU and writes are ignored by the PSC. If bit 31 = 1, but the Device Number\05, a PCI configuration cycle is run on the PCI Bus. If bit 31 = 0 (regardless of the Bus Number or Device Number values), the access to the CONFDATA Register location is forwarded to the PCI Bus and, if unclaimed on PCI, forwarded to ISA as a normal access to I/O address 0CFCh.

Table 5. I/O Control Registers

I/O Address	Mnemonic	Register	Register Access	Bus Master
0CF8h	CONFADD	Configuration Address	R/W	CPU Only
0CFCh	CONFDATA	Configuration Data	R/W	CPU Only
0CF9h	TRC	Turbo/Reset Control	R/W	CPU Only

Mechanism 1 PCI Configuration Address Fields

31	30 24	23 16	15 11	10 8	7 2	1 0
	Reserved	Bus Number	Device Number	Function Number	Register Offset	0 0

NOTE:
Device number = 05 is equivalent to IDSEL 16. Thus, other PCI devices cannot use IDSEL 16.

PCI Configuration Registers

The PCI configuration registers are located in the 82420EX PCIset's PCI configuration space and can only be accessed by the CPU. These registers (Table 6) can be accessed as byte, word, or dword quantities. The addresses for the configuration registers in the table are PCI configuration space offset values. The CPU accesses PCI configuration space (all PCI devices including the PSC) using mechanism 1 configuration access. For a detailed description of the PCI mechanism 1 configuration access, refer to the PCI Local Bus Specification document.

Some of the PCI configuration registers contain reserved bits. When reserved bits are read, a value of 0 is returned. In addition, the PCI configuration space includes reserved I/O locations. When reserved I/O locations are read, a value of 00h is returned. Writes to reserved bits or reserved I/O locations have no affect.

ISA-Compatible Registers

The ISA Compatible registers (Table 7) include DMA registers, timer registers, interrupt control registers, non-maskable interrupt, X-Bus support, and advanced power management control. These registers can be accessed by the CPU, a PCI master, or an ISA master as shown in Table 7. CPU or PCI masters can access the ISA-Compatible registers as 8-bit, 16-bit, 24-bit, or 32-bit quantities. However, only the first active BE[3:0]# is processed by the PSC. The remaining active byte enables in the same cycle are ignored. ISA Bus masters access the registers as 8-bit quantities. Unless otherwise stated in the individual register description, reserved bits must be written with a 0 and these bits return a 0 when read.

Table 6. PCI Configuration Register

Configuration Offset	Mnemonic	Register	Register Access	Bus Master
00–01h	VID	Vendor Identification	RO	CPU Only
02–03h	DID	Device Identification	RO	CPU Only
04–05h	PCICOM	PCI Command	R/W	CPU Only
06–07h	DS	Device Status	R/WC	CPU Only
08h	RID	Revision Identification	RO	CPU Only
09–3Fh	—	Reserved	—	—
40h	PCICON	PCI Control	R/W	CPU Only
41–43h	—	Reserved	—	—
44h	HDEVCON	Host Device Control	R/W	CPU Only
45–47h	—	Reserved	—	—
48–49h	LBIDE	PCI Local Bus IDE Control	R/W	CPU Only
4A–4Bh	—	Reserved	—	—
4Ch	IORT	ISA I/O Recovery Timer	R/W	CPU Only
4Dh	PREV	Part Revision Identification	R/W	CPU Only
4Eh	XBCSA	X-Bus Chip Select Enable A	R/W	CPU Only
4Fh	—	Reserved	—	—
50h	HOSTSEL	Host Bus Select	R/W	CPU Only
51h	DFC	Deturbo Frequency Control Register	R/W	CPU Only
52–53h	SCC	Secondary Cache Control	R/W	CPU Only
54–55h	—	Reserved	—	—
56–57h	DRAMC	DRAM Control	R/W	CPU Only
58h	—	Reserved	—	—

Table 6. PCI Configuration Register (Continued)

Configuration Offset	Mnemonic	Register	Register Access	Bus Master
59–5Fh	PAM	Programmable Attribute Map Registers	R/W	CPU Only
60–64h	DRB	DRAM Row Boundary Registers	R/W	CPU Only
65h	—	Reserved	—	—
66h	PIRQ0RC	PIRQ0 Route Control	R/W	CPU Only
67h	PIRQ1RC	PIRQ1 Route Control	R/W	CPU Only
68h	DMH	DRAM Memory Hole	R/W	CPU Only
69h	TOM	Top of Memory	R/W	CPU Only
6A–6Fh	—	Reserved	—	—
70h	SMRAMCON	SMRAM Control	R/W	CPU Only
71–9Fh	—	Reserved	—	—
A0h	SMICNTL	SMI Control	R/W	CPU Only
A1h	—	Reserved	R/W	CPU Only
A2–A3h	SMIEN	SMI Enable	R/W	CPU Only
A4–A7h	SEE	System Event Enable	R/W	CPU Only
A8h	FTMR	Fast Off Timer	R/W	CPU Only
A9	—	Reserved	—	—
AA–ABh	SMIREQ	SMI Request	R/W	CPU Only
ACh	CTLTMRL	Clock Throttle STPCLK# Low Timer	R/W	CPU Only
ADh	—	Reserved	—	—
AEh	CTLTMRH	Clock Throttle STPCLK# High Timer	R/W	CPU Only
AF–FFh	—	Reserved	—	—

Table 7. ISA-Compatible Registers

Address	FEDC	BA98	7654	3210	Register Name	Access Type	Bus Access
0000h	0000	0000	000x	0000	DMA1 CH0 Base and Current Address	r/w	CPU/PCI
0001h	0000	0000	000x	0001	DMA1 CH0 Base and Current Count	r/w	CPU/PCI
0002h	0000	0000	000x	0010	DMA1 CH1 Base and Current Address	r/w	CPU/PCI
0003h	0000	0000	000x	0011	DMA1 CH1 Base and Current Count	r/w	CPU/PCI
0004h	0000	0000	000x	0100	DMA1 CH2 Base and Current Address	r/w	CPU/PCI
0005h	0000	0000	000x	0101	DMA1 CH2 Base and Current Count	r/w	CPU/PCI
0006h	0000	0000	000x	0110	DMA1 CH3 Base and Current Address	r/w	CPU/PCI
0007h	0000	0000	000x	0111	DMA1 CH3 Base and Current Count	r/w	CPU/PCI
0008h	0000	0000	000x	1000	DMA1 Status (r), Command (w)	r/w	CPU/PCI
0009h	0000	0000	000x	1001	DMA1 Request	wo	CPU/PCI
000Ah	0000	0000	000x	1010	DMA1 Write Single Mask Bit	wo	CPU/PCI
000Bh	0000	0000	000x	1011	DMA1 Channel Mode	wo	CPU/PCI
000Ch	0000	0000	000x	1100	DMA1 Clear Byte Pointer	wo	CPU/PCI
000Dh	0000	0000	000x	1101	DMA1 Master Clear	wo	CPU/PCI
000Eh	0000	0000	000x	1110	DMA1 Clear Mask	wo	CPU/PCI
000Fh	0000	0000	000x	1111	DMA1 Write All Mask Bits	r/w	CPU/PCI
0020h	0000	0000	001x	xx00	INT 1 Control	r/w	CPU/PCI/ISA
0021h	0000	0000	001x	xx01	INT 1 Mask	r/w	CPU/PCI/ISA
0040h	0000	0000	010x	0000	Timer Counter 1 - Counter 0 Count	r/w	CPU/PCI/ISA
0041h	0000	0000	010x	0001	Timer Counter 1 - Counter 1 Count	r/w	CPU/PCI/ISA
0042h	0000	0000	010x	0010	Timer Counter 1 - Counter 2 Count	r/w	CPU/PCI/ISA
0043h	0000	0000	010x	0011	Timer Counter 1 Command Mode	wo	CPU/PCI/ISA
0060h[1]	0000	0000	0110	00x0	Reset X-Bus IRQ12/M and IRQ1	r	CPU/PCI/ISA
0061h	0000	0000	0110	0xx1	NMI Status and Control	r/w	CPU/PCI/ISA

Table 7. ISA-Compatible Registers (Continued)

Address	FEDC	BA98	7654	3210	Register Name	Access Type	Bus Access
0070h[1]	0000	0000	0111	0xx0	CMOS RAM Address and NMI Mask	wo	PCI/ISA
0080h[2]	0000	0000	100x	0000	DMA Page Register (Reserved)	r/w	CPU/PCI/ISA
0081h	0000	0000	100x	0001	DMA Channel 2 Page	r/w	CPU/PCI/ISA
0082h	0000	0000	1000	0010	DMA Channel 3 Page	r/w	CPU/PCI/ISA
0083h	0000	0000	100x	0011	DMA Channel 1 Page	r/w	CPU/PCI/ISA
0084h[2]	0000	0000	100x	0100	DMA Page Register (Reserved)	r/w	CPU/PCI/ISA
0085h[2]	0000	0000	100x	0101	DMA Page Register (Reserved)	r/w	CPU/PCI/ISA
0086h[2]	0000	0000	100x	0110	DMA Page Register (Reserved)	r/w	CPU/PCI/ISA
0087h	0000	0000	100x	0111	DMA Channel 0 Page	r/w	CPU/PCI/ISA
0088h[2]	0000	0000	100x	0100	DMA Page Register (Reserved)	r/w	CPU/PCI/ISA
0089h	0000	0000	100x	1001	DMA Channel 6 Page	r/w	CPU/PCI/ISA
008Ah	0000	0000	100x	1010	DMA Channel 7 Page	r/w	CPU/PCI/ISA
008Bh	0000	0000	100x	1011	DMA Channel 5 Page	r/w	CPU/PCI/ISA
008Ch[2]	0000	0000	100x	1100	DMA Page Register (Reserved)	r/w	CPU/PCI/ISA
008Dh[2]	0000	0000	100x	1101	DMA Page Register (Reserved)	r/w	CPU/PCI/ISA
008Eh[2]	0000	0000	100x	1110	DMA Page Register (Reserved)	r/w	CPU/PCI/ISA
008Fh	0000	0000	100x	1111	DMA Low Page Register Refresh	r/w	CPU/PCI/ISA
00A0h	0000	0000	101x	xx00	INT 2 Control	r/w	CPU/PCI/ISA
00A1h	0000	0000	101x	xx01	INT 2 Mask	r/w	CPU/PCI/ISA
00B2h	0000	0000	1011	0010	Advanced Power Management Control	r/w	CPU Only
00B3h	0000	0000	1011	0011	Advanced Power Management Status	r/w	CPU/PCI
00C0h	0000	0000	1100	000x	DMA2 CH0 Base and Current Address	r/w	CPU/PCI
00C2h	0000	0000	1100	001x	DMA2 CH0 Base and Current Count	r/w	CPU/PCI
00C4h	0000	0000	1100	010x	DMA2 CH1 Base and Current Address	r/w	CPU/PCI

Table 7. ISA-Compatible Registers (Continued)

Address	FEDC	BA98	7654	3210	Register Name	Access Type	Bus Access
00C6h	0000	0000	1100	011x	DMA2 CH1 Base and Current Count	r/w	CPU/PCI
00C8h	0000	0000	1100	100x	DMA2 CH2 Base and Current Address	r/w	CPU/PCI
00CAh	0000	0000	1100	101x	DMA2 CH2 Base and Current Count	r/w	CPU/PCI
00CCh	0000	0000	1100	110x	DMA2 CH3 Base and Current Address	r/w	CPU/PCI
00CEh	0000	0000	1100	111x	DMA2 CH3 Base and Current Count	r/w	CPU/PCI
00D0h	0000	0000	1101	000x	DMA2 Status(r) Command(w)	r/w	CPU/PCI
00D2h	0000	0000	1101	001x	DMA2 Request	wo	CPU/PCI
00D4h	0000	0000	1101	010x	DMA2 Write Single Mask Bit	wo	CPU/PCI
00D6h	0000	0000	1101	011x	DMA2 Write Mode Register	wo	CPU/PCI
00D8h	0000	0000	1101	100x	DMA2 Clear Byte Pointer	wo	CPU/PCI
00DAh	0000	0000	1101	101x	DMA2 Master Clear	wo	CPU/PCI
00DCh	0000	0000	1101	110x	DMA2 Clear Mask	wo	CPU/PCI
00DEh	0000	0000	1101	111x	DMA2 Write All Mask Bits	r/w	CPU/PCI
00F0h[1]	0000	0000	1111	0000	Coprocessor Error	wo	CPU/PCI/ISA
0481h	0000	0100	1000	0001	DMA CH2 High Page Register	r/w	CPU/PCI/ISA
0482h	0000	0100	1000	0010	DMA CH3 High Page Register	r/w	CPU/PCI/ISA
0483h	0000	0100	1000	0011	DMA CH1 High Page Register	r/w	CPU/PCI/ISA
0487h	0000	0100	1000	0111	DMA CH0 High Page Register	r/w	CPU/PCI/ISA
0489h	0000	0100	1000	1001	DMA CH6 High Page Register	r/w	CPU/PCI/ISA
048Ah	0000	0100	1000	1010	DMA CH7 High Page Register	r/w	CPU/PCI/ISA
048Bh	0000	0100	1000	1011	DMA CH5 High Page Register	r/w	CPU/PCI/ISA
04D0h	0000	0100	1101	0000	INT-1 Edge/Level Control	r/w	CPU/PCI/ISA
04D1h	0000	0100	1101	0001	INT-2 Edge/Level Control	r/w	CPU/PCI/ISA

NOTES:
1. Read and write accesses to these locations are always forwarded to the ISA Bus.
2. Write accesses to these locations are forwarded to the ISA Bus. Read Accesses are not forwarded to the ISA Bus. If programmed in the ISA I/O Recovery Timer Register, the IB will not alias the 90–9Fh address range with the 80–8Fh address range. In this case, accesses to the 90–9Fh address range are forwarded to the ISA Bus for both reads and writes (i.e. they are no longer considered IB registers).

3.2 I/O Control Registers

There are three I/O control registers (CONFADD, CONFDATA, and TRC) and these registers are all located in the CPU I/O space.

3.2.1 CONFADD—CONFIGURATION ADDRESS REGISTER

IO Address: 0CF8h
Default Value: 00000000h
Attribute: Read/Write
Size: 32 Bits

The CONFADD Register contains the address information for the next PCI configuration space access. Once the address is programmed into this register, the CPU can access the selected device register by a read/write to the CONFDATA Register. Only dword accesses are permitted to this register.

Bit	Description
31	**PCI Configuration Space Enable (CONFE):** This bit enables/disables access to the PCI configuration space. When CONFE = 1, PCI configuration space access is enabled. When CONFE = 0 (default), PCI configuration space access is disabled. When disabled, accesses to the CONFDATA Register, if not claimed on the PCI Bus, are forwarded to the ISA Bus.
30:24	**Reserved**
23:16	**Bus Number (BUSNUM):** This field selects the PCI Bus to be accessed. The PCI Bus behind the PSC is bus number 0 (00h). Thus, this field must be 00h for access to the PCIset's configuration registers.
15:11	**Device Number (DEVNUM):** This field selects the PCI Bus device to be accessed. The PSC uses this field to drive the IDSEL lines that select a specific PCI device during initialization. The IDSEL lines are only driven when BUSNUM = 00h. Otherwise, the PSC sends the configuration to a PCI-to-PCI bridge device. This field must be 05h for access to the PCIset's configuration registers (which is equivalent to IDSEL 16). Note that other PCI devices cannot use IDSEL 16.
10:8	**Function Number (FUNCNUM):** A device connected to the PCI Bus can have up to eight functions. This field selects a particular function within a device and must be 000 for access to the PCIset's configuration registers.
7:2	**Register Number (REGNUM):** This field is the configuration register offset address and indexes a dword in configuration space. REGNUM is used during initialization to select a specific device configuration registers.
1:0	**Reserved:** Fixed at 00.

3.2.2 CONFDATA—CONFIGURATION DATA REGISTER

IO Address: 0CFCh
Default Value: 00000000h
Attribute: Read/Write
Size: 32 Bits

The CONFDATA Register contains the data that is sent or received during a PCI configuration space access. Note that a read or write to this register accesses the PCI configuration space location specified by the contents of the CONFADD Register. CONFDATA supports CPU byte, word, and dword accesses.

3.2.3 TRC—TURBO/RESET CONTROL REGISTER

IO Address: 0CF9h
Default Value: 00h
Attribute: Read/Write
Size: 8 Bits

The TRC Register provides a means of generating soft or hard resets. During a hard reset, CPURST, PCIRST#, and RSTDRV are asserted for approximately 1 ms. A hard reset is initiated when this register is programmed for a hard reset or PWROK is asserted. During a soft reset, SRESET is asserted for a minimum of 16 Host Bus clocks. This register also selects the CPU De-Turbo mode. The TRC Register can only be accessed by the CPU with 8 bit IN or OUT instructions. Note that it is illegal for a PCI master or an ISA master to access the TRC Register.

Bit	Description
7:3	**Reserved:** Must be 0 when programming this register.
2	**Reset CPU (RCPU):** RCPU is used to initiate a hard reset or soft reset to the CPU, depending on the state of bit 1 of this register. Bit 1 must be set up prior to writing a 1 to bit 2. Thus, two write operations are required to initiate a reset. The first write programs bit 1 to the appropriate state while setting this bit to 0. The second write operation keeps bit 1 at its programmed state while setting this bit to a 1. When RCPU transitions from a 0 to a 1, a hard reset is initiated if bit 1 = 1 and a soft reset is initiated if bit 1 = 0.
1	**Reset CPU Mode (RCPUM):** This bit is used in conjunction with bit 2 of this register to initiate either a hard or soft reset. When RCPUM = 1, the PSC initiates a hard reset to the CPU when bit 2 transitions from 0 to 1. When RCPUM = 0, the PSC initiates a soft reset when bit 2 transitions from a 0 to a 1.
0	**Deturbo Mode (DM):** This bit enables/disables deturbo mode. When DM = 1, the 82420EX PCIset is in deturbo mode. In this mode, the PSC periodically asserts HOLD. The frequency of the HOLD assertion is fixed at once in 1024 Host Clocks. The duty cycle of the HOLD active period is controlled by the Deturbo Frequency Control (DFC) Register. When DM = 0, the Deturbo mode is disabled. Note that the deturbo counter does not start until HLDA is returned by the CPU. Deturbo mode can be used to maintain backward compatibility with older software packages that rely on the operating speed of the older processors. For accurate speed emulation, L1 caching should be disabled. If L1 is disabled during runtime, the following steps should be performed to make sure that all dirty data has been flushed from the cache to main memory before entering deturbo mode. Disable the L1 cache via the L1EN bit in the HOSTSEL Register. This prevents the KEN# signal from being asserted, which effectively disables the L1 cache. Thus, no new L1 cache line fills will occur. At this point, software executes the **WBINVD** of **INVD** instruction to flush the L1 cache, and then sets DM to 1. When exiting the deturbo mode, the system software must first set DM to 0, then enable L1 caching by writing to the HOSTSEL Register.

3.3 PCI Configuration Registers

This section describes the PCI configuration registers of the 82420 PCIset. The registers are listed in the order that they appear in Table 6.

3.3.1 VID—VENDOR IDENTIFICATION REGISTER

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only
Size: 16 Bits

This 16-bit register, combined with the Device Identification Register, uniquely identifies any PCI device. The VID Register contains the vendor identification number assigned to Intel. Writes to this register have no effect.

3.3.2 DID—DEVICE IDENTIFICATION REGISTER

Address Offset: 02–03h
Default Value: 0486h
Attribute: Read Only
Size: 16 Bits

This 16-bit register, combined with the Vendor Identification register, uniquely identifies any PCI device. The 16-bit value in this register is the device number assigned to the 82425EX PSC. Writes to this register have no effect.

3.3.3 PCICOM—PCI COMMAND REGISTER

Address Offset: 04–05h
Default Value: 0007h
Attribute: Read/Write
Size: 16 Bits

This 16-bit register enables/disables the SERR# signal.

Bit	Description
15:9	**Reserved**
8	**SERR# Enable (SERRE):** SERRE enables/disables the SERR# signal. When SERRE = 1, SERR# is asserted if the PCIset detects a parity error during a main memory read cycle or a target abort is received on a PSC-initiated PCI cycle. When SERRE = 0, SERR# is never asserted.
7:0	**Not Used:** Defaults to 07h for compatibility reasons.

3.3.4 DS—DEVICE STATUS REGISTER

Address Offset: 06–07h
Default Value: 0200h
Attribute: Read Only and Read/Write Clear
Size: 16 Bits

DS is a 16-bit status register that reports the occurrence of a PCI master abort, PCI target abort, and main memory or cache parity errors. PCISTS also indicates the DEVSEL# timing that has been set by the PSC hardware.

Bit	Attribute	Description
15	R/WC	**Main Memory Parity Error (MMPERR):** When the PSC detects a parity error, this bit is set to 1. Software sets this bit to 0 by writing a 1 to it.
14	R/WC	**SERR# Status (SERRS):** When the PSC asserts the SERR# signal, this bit is set to a 1. Note that the SERR# signal is enabled/disabled in the PCICOM Register. When SERR# is enabled (via the PCICOM Register) and the PSC detects a parity error on a main memory read cycle or receives a target abort during a PSC-initiated PCI cycle, the PSC sets this bit to a 1.
13	R/WC	**Master Abort Status (MAS):** When a PSC-initiated PCI configuration cycle is not claimed, the PSC master aborts the cycle and sets this bit to a 1. For a CPU read, the PSC returns all 1s. When a memory cycle above 16 MBytes and not in an enabled BIOS region is not claimed, the PSC master-aborts the cycle and sets this bit to a 1. Software sets this bit to 0 by writing a 1 to it. **NOTE:** When a PSC-initiated PCI memory access under 16 MBytes or in an enabled BIOS range above 16 MBytes is not claimed, the PSC master aborts the cycle and forwards the cycle to ISA. When a PSC-initiated PCI I/O access is not claimed, the PSC master aborts the cycle and forwards the cycle to ISA. For these master aborts, the MAS bit is not set to 1.
12	R/WC	**Received Target Abort Status (RTAS):** When a PSC-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. In addition, when the SERRE bit in the PCICOM Register is set to a 1 (enabling SERR#), the PSC asserts the SERR# signal. Software sets this bit to 0 by writing a 1 to it. Note that if the target aborted cycle is an I/O or memory read, the PSC completes the CPU cycle by returning RDY#.
11		**Reserved**
10:9	RO	**DEVSEL# Timing (DEVT):** This 2-bit field indicates the timing of the DEVSEL# signal when the PSC responds as a target. The PCI specification defines three allowable timings for assertion of DEVSEL#: 00 = fast, 01 = medium, and 10 = slow (DEVT = 11 is reserved). DEVT indicates the slowest time that a device asserts DEVSEL# for any bus command, except configuration read and write cycles. The 82420EX PCIset implements medium speed DEVSEL# timing and, therefore, bits[10:9] = 01 when read.
8:0		**Reserved**

3.3.5 RID—REVISION IDENTIFICATION REGISTER

Address Offset: 08h
Default Value: 00h
Attribute: Read Only
Size: 8 Bits

This register contains the revision number of the PSC. The Fabrication House ID Number and Revision Number correspond to bits 7-5 and the lower nibble respectively of the Revision Identification Register as follows:

bits 7-5 (upper 3 bits) Fabrication House ID Number
bits 3-0 (lower nibble) Revision Number

3.3.6 PCICON—PCI CONTROL REGISTER

Address Offset: 40h
Default Value: 00h
Attribute: Read /Write
Size: 8 Bits

The PCICON register enables/disables target abort and main memory DRAM parity error reporting. This register also selects the subtractive decode sample point, enables/disables PCI write buffers, and controls PCI bursting of consecutive CPU-to-PCI write cycles and byte merging.

Bit	Description
7	**Reserved**
6	**Target Abort Error Enable (TAEE):** When ATEE = 1 and a PSC-initiated cycle is target aborted, the PSC asserts SERR# for a PCI Clock. When TAEE = 0 (default) and a PSC-initiated cycle is target aborted, the PSC does not assert SERR#.
5	**DRAM Parity Error Enable (DPEE):** When DPEE = 1 and a main memory parity error is detected, the PSC asserts SERR# for a PCI Clock. When DPEE = 0 (default) and a main memory parity error is detected, the PSC will not assert SERR#.
4:3	**Subtractive Decode Sample Point (SDSP):** The SDSP field determines the DEVSEL# sample point, after which an inactive DEVSEL# results in the PSC forwarding the unclaimed PCI cycle to the ISA Bus (subtractive decoding). This setting should match the slowest device in the system. The values for this field and associated sampling point meaning are shown below. **Bits[4:3] — Sampling Point** 00 — Slow (default) 01 — Typical 10 — Fast 11 — Reserved
2	**PCI Posted Write Buffer Enable (PPBE):** When PPBE = 1, the PCI posted write buffers are enabled. When PPBE = 0 (default), the PCI posted write buffers are disabled.

Bit	Description
1	**CPU-to-PCI Bursting Enable (CPBE):** This bit enables/disables PCI burst cycles for CPU-to-PCI write cycles. When CPBE = 1, back-to-back sequential CPU memory writes are sent out on the PCI Bus as a burst cycle. When CPBE = 0 (default), CPU write cycles are always sent out on the PCI Bus as separate PCI memory write cycles.
0	**CPU-to-PCI Byte Merging (CPME):** Byte merging permits the PSC to merge the data of consecutive CPU-to-PCI byte/word writes within the same dword address, into the same posted write buffer location. The merged collection of bytes is then sent over the PCI Bus as a single dword. Byte merging is performed in the compatible VGA range only (0A0000–0BFFFFh). When CPME = 1, back-to-back CPU memory byte/word write cycles within the same dword address (in the 0A0000–0BFFFFh range) are merged into a single posted write buffer location. When CPME = 0 (default), or when the address location is outside of the VGA range, each memory write is stored in a separate posted write buffer location and sent separately over the PCI Bus. Some PCI graphics cards memory map their I/O location in the A0000h to B0000h memory region. If consecutive, multiple 8 or 16 bit write cycles are made to the add-in card at a memory mapped I/O location between A0000h–BFFFFh, the PSC will merge the data if the PSC is programmed for byte merging. The first write cycle will be written to the add-in card. However, subsequent write cycles will be overwritten in the PSC and never reach the add-in card. Because the consecutive, multiple write cycles are to the same address, the PSC will "merge" (overwrite the previous data) as long as the PCI bus is unavailable, causing the add-in card to not receive all the intended write cycles. Byte merging should be disabled when used with graphics cards that memory map I/O locations in the compatibility Video buffer area (A0000h–BFFFFh). Byte merging enhances graphics performances when used in operating systems that write to the video memory area in 8- or 16-bit writes (e.g. DOS). For operating systems that write to the video memory area in 32-bit writes, byte merging is not necessary.

3.3.7 HOSTDEV—HOST DEVICE CONTROL REGISTER

Address Offset: 44h
Default Value: 00h
Attribute: Read /Write
Size: 8 Bits

The HOSTDEV Register indicates to the PSC if there is a slave device, other than the PSC, that resides on the Host Bus. If there is another slave device present, the PSC sampling points for HDEV# and HRDY# are set in this register.

Bit	Description
7:3	**Reserved**
2	**Host Device Present (HDEVP):** When HDEVP = 1, there is a Host Bus slave device present. This device can claim any I/O or memory range that is not positively decoded by the PSC by asserting HDEV#. When HDEVP = 0 (default), there is no host bus slave device in the system.
1	**HDEV# Signal Sampling Point (HDEVSP):** HDEVSP specifies the maximum delay for HDEV# response and this bit only has meaning when HDEVP = 1. When HDEVSP = 1 (and HDEVP = 1), the PSC assumes that the Host Bus slave device asserts HDEV# with Host Bus fast timing (i.e., HDEV# can be asserted as late as one host clock after ADS# is asserted). In this case, the PSC samples HDEV# in the host cycle after ADS# and, if not asserted, forwards the cycle to the PCI Bus. When HDEVSP = 0 (and HDEVSP = 1), the PSC assumes that the Host Bus slave device asserts HDEV# with Host Bus slow timing (i.e., HDEV# can be asserted as late as two host clocks after ADS# is asserted). In this case, the PSC samples HDEV# in the host cycle after ADS# and one host cycle later and if not asserted, forwards the cycle to the PCI Bus.
0	**HRDY# Maximum Signal Sampling Point (HRDYSP):** HDEVSP specifies the delay from HRDY# to RDY# and this bit only has meaning when HDEVP = 1. When HRDYSP = 1 (and HDEVP = 1), the PSC assumes that the Host Bus slave device asserts HRDY# with Host Bus fast timing (i.e., Host RDY# is asserted in the same host clock as HRDY# is asserted). When HRDYSP = 0 (and HDEVP = 1), the PSC assumes that the Host Bus slave device asserts HRDY# with host bus slow timing (i.e., Host RDY# is asserted one host clock after HRDY# is asserted). Note that, when HDEVP = 0, HRDYSP has no meaning.

3.3.8 LBIDE—PCI LOCAL BUS IDE CONTROL REGISTER

Address Offset: 48–49h
Default Value: 0000h
Attribute: Read /Write
Size: 16 Bits

The LBIDE Register controls the PSC's IDE interface. The register determines when the PCI Local Bus IDE path will be used and the timing characteristics of the PCI Local Bus IDE cycle.

Bit	Description
15:13	**Reserved**
12:10	**Recover Time (RCT[2:0]):** This field controls the minimum time from the time IORDY is sampled asserted on the first cycle to the IOx# assertion of the next cycle. This recovery time mechanism applies to all cycles using the fast timing bank, even if the next cycle is a compatible cycle. For example, if a first cycle is a data port access using the fast timing bank and the next cycle is to a control or status port, LBIDE# is negated and the full setup protocol occurs prior to the second cycle. Normally, this setup protocol is longer than the programmed recovery time. However, if the setup protocol is shorter, the proper recovery time must still be met. The value of this field determines the minimum number of PCI clocks between the last IORDY sample point and the IOx# strobe of the next cycle. RCT[2:0] Bits[12:10] / Recovery Time: 000 = 8; 001 = 7; 010 = 6; 011 = 5; 100 = 4; 101 = 3; 110 = Note; 111 = Note **NOTE:** The recovery time is 3 PCI clocks.
9:8	**IORDY Sample Point (ISP[1:0]):** This field determines the number of clocks between IOx# assertion and the first IORDY sample point (see the following table). IORDY is sampled for the first time on the programmed number of clocks (number of low-to-high clock transitions) following the assertion of IOx#. If IORDY is negated when sampled, wait-states are inserted until IORDY is sampled asserted. ISP[1:0] Bits[9:8] / IORDY Sampling Point: 00 = 6 Clocks (default); 01 = 5 Clocks; 10 = 4 Clocks; 11 = 3 Clocks
7:6	**Reserved**
5:4	**IORDY Sample Point Enable Drive Select (ISPEDS[1:0]):** ISPEDS[1:0] enable/disable the sampling of IORDY for drive 0 and 1. When this feature is enabled for a drive (via this field), and the drive is selected (via a copy of bit 4 of 1x6h), all accesses to the enabled I/O address range sample IORDY. The IORDY sample point is specified by the ISP[1:0] field. When the drive is disabled (0), IORDY sampling is disabled. The internal IORDY signal is forced asserted guaran-teeing that IORDY is sampled asserted at the first sample point as specified by the ISP[1:0] field. ISPEDS[1:0] Bits[5:4] / IORDY Sampling Point Enable Drive Select: 00 = Neither Drive Enabled (default); 01 = Drive 0 Enabled; 10 = Drive 1 Enabled; 11 = Both Drives Enabled

Bit	Description
3:2	**Fast Timing Bank Drive Select 1 (FTBDS1):** FTBDS[1:0] enable/disable the fast timing PCI local bus IDE path for drive 0 and 1. When this feature is enabled for a drive (via this field), and the drive is selected (via a copy of bit 4 of 1x6h), all accesses to the enabled I/O address range will use the fast timing bank PCI local bus IDE path. Note that accesses to all non-data ports of the enabled I/O address range use the 8-bit compatible timing PCI local bus path. When the drive is disabled (0), accesses to the data port of the selected I/O address range use the 16-bit compatible timing PCI local bus path. **Bits[3:2] — Fast Timing Bank Select** 00 — Neither Drive Enabled (default) 01 — Drive 0 Enabled 10 — Drive 1 Enabled 11 — Both Drives Enabled
1:0	**Primary/Secondary PCI IDE Enable (IDEE):** This field enables/disables the PCI IDE, and, if enabled, selects the primary/secondary IDE address that is used as shown below. Accesses to the unselected address range (primary/secondary) are forwarded to the ISA Bus. **Bits[1:0] — Primary/Secondary IDE Address Select** 00 — IDE Disabled (default) 01 — Primary: 1F0–1F7h, 3F6h,3F7h 10 — Secondary: 170–177H, 376h, 377h 11 — Reserved

LBIDE Programming Information

The BIOS code will assess the CPU frequency and drive capabilities, and then program the timing fields appropriately. Table 8 shows the typical settings of the various cycle timing bits for the supported CPU frequencies and IDE modes. The table assumes that the drives are utilizing IORDY. If IORDY is not utilized, additional wait-states may be deleted via the ISP bits.

Table 8. Typical Register Settings for Different CPU Frequencies

PCI Frequency	IDE Mode	RCT(2:0)		ISP(1:0)		Cycle Length (ns) 1x Clock Mode(1)
		Bits[12:10]	Clocks	Bits[9:8]	Clocks	
20	1	100	4	10	4	400(1)
25	1	101	6	10	4	400
33	1	001	7	00	6	390
20	2	110	2	11	3	300(2)
25	2	110	2	10	4	280(2)
33	2	101	3	01	5	240
20	3	110	2	11	3	300(2)
25	3	110	2	11	3	240(2)
33	3	101	3	10	4	210

NOTES:
1. The clock modes are determined by strapping options at powerup and the mode is reflected in the HOSTSEL Register.
2. Cycle times are governed by the inherent RDY#, ADS#, and address decoding delay between back-to-back cycles rather than the programmed value in the RCT field.

3.3.9 IORT—ISA I/O RECOVERY TIMER REGISTER

Address Offset: 4Ch
Default Value: 4Dh
Attribute: Read/Write
Size: 8 bits

The IORT Register provides ISA I/O recovery time control and enables/disables the aliasing of addresses 80–8Fh and 90–9Fh. The I/O recovery mechanism in the IB adds recovery delay between CPU or PCI master originated 8-bit and 16-bit I/O cycles to the ISA Bus. The IB automatically forces a minimum delay of 3.5 SYSCLKs between back-to-back 8 and 16 bit I/O cycles to the ISA Bus. This delay is measured from the rising edge of the I/O command (IOR# or IOW#) to the falling edge of the next I/O command. If a delay of greater than 3.5 SYSCLKs is required, the ISA I/O Recovery Time Register can be programmed to increase the delay in increments of SYSCLKs. No additional delay is inserted for back-to-back I/O "sub-cycles" generated as a result of byte assembly or disassembly. This register defaults to 8- and 16-bit recovery enabled with one SYSCLK clock added to the standard I/O recovery.

Bit	Description
7	**DMA Reserved Page Register Aliasing Disable (DMAAD):** When DMAAD = 0 (default), the IB aliases I/O accesses in the 90–9Fh range to the 80–8Fh range. In this case, the IB only forwards CPU/PCI write accesses to the 90–9Fh range to the ISA Bus. When DMAAD = 1, the IB forwards both CPU/PCI read and write accesses to these address locations to the ISA Bus (i.e. the I/O address locations are no longer considered IB internal registers). Note, that port 92h is always a distinct ISA register in the 90–9Fh range and is always forwarded to the ISA Bus. When DMAAD = 1, ISA master accesses to the 90–9Fh range are ignored by the IB. When this bit is set to 1, the IB does not re-load the power management Fast Off-Timer with its original value when accesses to the 90–9Fh address range are decoded.
6	**8-Bit I/O Recovery Select (IOR8E):** When IOR8E = 1, bits[5:3] select the I/O recovery time. When IOR8E = 0, programmable recovery times are disabled and the standard recovery time of 3.5 SYSCLKS is inserted.
5:3	**8-Bit I/O Recovery Times (IOR8):** This 3-bit field defines the recovery time for 8-bit I/O as shown Below. Programmable delays between back-to-back 8-bit PCI or CPU cycles to ISA I/O slaves are shown in terms of additional ISA clock recovery cycles (SYSCLK). The selected delay programmed into this field is enabled/disabled via bit 6 of this register.
2	**16-Bit I/O Recovery Enable (IOR16E):** When IOR16E = 1, bits[1:0] select the I/O recovery time. When IOR16E = 0, programmable recovery times are disabled and the standard recovery time of 3.5 SYSCLKS is inserted.

Bits[5:3]	8-Bit I/O Recover Time	Bits[5:3]	8-Bit I/O Recover Time
000	8 SYSCLKs	100	4 SYSCLKs
001	1 SYSCLKs (default)	101	5 SYSCLKs
010	2 SYSCLKs	110	6 SYSCLKs
011	3 SYSCLKs	111	7 SYSCLKs

Bit	Description
1:0	**16-Bit I/O Recovery Times (IOR16):** This 2-bit field defines the recovery time for 16-bit I/O as shown below. Programmable delays between back-to-back 16-bit PCI or CPU cycles to ISA I/O slaves are shown in terms of additional ISA clock recovery cycles (SYSCLK). The selected delay programmed into this field is enabled/disabled via bit 2 of this register. **Bits[1:0] — 16-Bit I/O Recover Time** 00 — 4 SYSCLKs 01 — 1 SYSCLKs (default) 10 — 2 SYSCLKs 11 — 3 SYSCLKs

3.3.10 PREV—PART REVISION REGISTER

Address Offset: 4Dh
Default Value: 00h
Attribute: Read/Write. Read Only
Size: 8 bits

This register provides the device stepping information for the IB and enables/disables DMA and ISA master accesses to DRAM BIOS locations E0000–EFFFFh. Bits 0 and 1 in this register are hardwired and write accesses have no effect.

Bit	Attribute	Description
7:5		**IB Fabrication House ID**
4	R/W	**E0000–EFFFFh ISA Forwarding Enable:** When bit 4 = 1 (and bit 6 in the XBCSA Register is set to 0), ISA master and DMA accesses to memory locations E0000–EFFFFh are forwarded to main memory. When bit 4 = 0 (default), ISA master and DMA accesses to this memory region are confined to the ISA Bus. Note that if bit 6 = 1 in the XBCSA Register, memory accesses to memory locations E0000–EFFFFh are always confined to the ISA Bus, regardless of the setting of bit 4 of this register.
3:0	RO	**Revision ID:** This field contains the device stepping information for the 82426EX IB.

3.3.11 XBCSA—X-BUS CHIP SELECT A REGISTER

Address Offset: 4Eh
Default Value: 03h
Attribute: Read/Write
Size: 8 bits

This register enables/disables accesses to the real time clock (RTC), keyboard controller (KBC), and BIOS. Disabling any of these bits prevents the chip select and X-Bus output enable control signal (XBUSOE#) for that device from being generated. The XBCSA Register also provides coprocessor error and mouse functions.

Bit	Description
7	**Extended BIOS Enable (EXBIOSE):** When EXBIOSE = 1 (enabled), CPU or PCI master accesses to locations FFF80000–FFFDFFFFh, that are not claimed by a PCI device are forwarded to the ISA Bus and results in the generation of BIOSCS# and XBUSOE#. Note that forwarding this region at the top of 4 GBytes to the ISA Bus (24-bit addressing) results in aliasing this 384 KByte region to the top of the 16 MByte ISA memory space. To avoid contention, ISA add-in memory must not be present in this space. When EXBIOSE = 0 (disabled: default), BIOSCS# or XBUSOE# are not generated. CPU accesses to locations FFF80000–FFFDFFFFh, that are not claimed by PCI devices are master-aborted by the PSC. Note that the Master Abort Status bit is set to 1 (DS Register). For reads, data of all 1's is returned to the CPU. PCI master accesses to locations FFF80000–FFFDFFFFh that are not claimed by PCI devices are ignored by the PSC.
6	**Lower BIOS Enable (LBIOSE):** When LBIOSE = 1 (enabled: default), CPU, PCI master, or ISA master accesses to the lower 64 KByte BIOS block at the top of 1 MByte (E0000–EFFFFh), or the aliases at the top of 4 GByte, that are not claimed by PCI devices, result in the generation of BIOSCS# and XBUSOE#. Note that forwarding this region at the top of 4 GBytes to the ISA Bus (24-bit addressing) results in aliasing this region to the top of the 16 MByte ISA memory space. To avoid contention, ISA add-in memory must not be present in this space. When LBIOSE = 0 (disabled: default), BIOSCS# or XBUSOE# are not generated during these accesses. Also, when LBIOSE = 0 (and bit 4 is 1 in the IB's PREV Register), ISA master or DMA accesses to this region are forwarded to main memory. CPU accesses to the lower 64 KByte BIOS region (0FFFE0000–0FFFEFFFFh) that are not claimed by PCI devices are master-aborted by the PSC. The Master Abort Status bit is set to 1 (DS Register). For reads, data of all 1's is returned to the CPU. PCI master accesses to the lower 64 KByte BIOS region (0FFFE0000–0FFFEFFFFh), that are not claimed by PCI devices, are ignored by the PSC.
5	**Coprocessor Error Function Enable (CPEE):** This bit enables/disables the coprocessor error support. When CPEE = 1 (enabled), the FERR# input, when asserted, triggers IRQ13 (internal). FERR# also gates the IGNNE# output. This bit defaults to disabled (0).
4	**IRQ12/M Mouse Function Enable (IRQ12/ME):** When bit 4 = 1, IRQ12/M provides the mouse function. When bit 4 = 0 (default), IRQ12/M provides the standard IRQ12 interrupt function.
3	**Reserved:** Must be set to 0.
2	**BIOS Memory Write Protect (BIOSWP):** When BIOSWP = 1 (read/write access), BIOSCS# is asserted for BIOS memory read and write cycles in the decoded BIOS region. When BIOSWP = 0 (write protect: default), BIOSCS# is only asserted for BIOS read cycles.
1	**Keyboard Controller Address Enable (KBCAE):** When KBCAE = 1 (enabled: default), the keyboard controller chip select signal (KBCCS#) and the XBUSOE# signals are generated for accesses to the keyboard controller address locations 60h, 62h, 64h, and 66h. When KBCAE = 0 (disabled), KBCCS# and XBUSOE# are not generated for these accesses.
0	**RTC Address Enable (RTCAE):** When RTCAE = 1 (enabled: default), the RTCCS#, RTCALE, and XBUSOE# signals are generated for accesses to the RTC address locations 70–77h. When RTCAE = 0 (disable), the RTCCS#, RTCALE, and XBUSOE# signals are not generated for accesses to these addresses.

3.3.12 HOSTSEL—HOST SELECT REGISTER

Address Offset: 50h
Default Value: 00000xx0 (x = Depends on hardware strapping options)
Attribute: Read/Write
Size: 8 Bits

The HOSTSEL Register enables/disables the L1 cache, indicates the clock configuration selected by hardware strapping options, and selects the L1 caching policy.

Bit	Description
7:4	**Reserved**
3	**L1 Caching Policy Select (L1CPSEL):** L1CPSEL selects the caching policy for the L1 cache. When L1CPSEL = 1, the L1 caching policy is write-back and when L1CPSEL = 0, the caching policy is write-through.
2:1	**Clock Configuration Status (CLKCONFS):** Clock configuration is determined by hardware strapping options on the SIDLE# and CMDV# signal pins at power-up (see Section 4.15, Clocks). This field is read only. CLKCONFS indicates the clock mode and frequencies selected by the strapping options. **Bits[2:1] — HCLK — PCICLK — Clock Mode** 00 — 25 MHz — 25 MHz — 1x 01 — 33 MHz — 33 MHz — 1x 10 — Reserved 11 — Reserved
0	**L1 Cache Enable (L1CE):** L1CE enables/disables the first level cache in the CPU. When L1CE = 1 (enable), the PSC responds to the CPU with KEN# asserted for cacheable memory cycles. When L1CE = 0 (disable), the KEN# signal is always negated to the CPU. This prevents new cache line fills to either the first level or second level caches.

3.3.13 DFC—DETURBO FREQUENCY CONTROL REGISTER

Address Offset: 51h
Default Value: 80h
Attribute: Read /Write
Size: 8 Bits

Some old software packages that rely on the operating speed of the processor do not work on today's faster systems. To maintain backward compatibility with these software packages, the 82420EX PCIset provides a mechanism to emulate the operating speed of PC/AT systems. This emulation is achieved with the deturbo mode (enabled/disabled via the Turbo/Reset Control Register). When the deturbo mode is enabled, the PSC periodically asserts the HOLD signal to slow down the effective speed of the CPU. The frequency of the HOLD assertion is fixed to once in 1024 Host Clocks. The duty cycle of the HOLD active period is controlled by the DFC Register.

Bit	Description
7:0	**Deturbo Mode Frequency Adjustment Value:** This 8-bit value effectively defines the duty cycle of the HOLD signal. The value programmed into this register is compared against a free running 8-bit counter running at 1/4 the CPU clock. When the counter is greater than the value specified in this register, HOLD is asserted to the CPU. HOLD is negated when the counter value is equal to or smaller than the contents of this register. HOLD is negated when the counter rolls over to 00h. Note that the deturbo counter does not start until HLDA is returned by the CPU. The deturbo emulation speed is directly proportional to the value in this register. The smaller the value in this register the lower the deturbo emulation speed.

3.3.14 SCC—SECONDARY (L2) CACHE CONTROL REGISTER

Address Offset: 52–53h
Default Value: 0000h
Attribute: Read /Write
Size: 16 Bits

This 16-bit register defines the L2 cache operations. SCC enables/disables the L2 cache, adjusts cache size, selects the cache write policy, defines the cache SRAM type, and selects various read/write cache cycle times. In addition, a cache miss can be forced for each access permitting software to initialize the cache. Cache hits can also be forced permitting software to determine the size of the L2 cache memory.

NOTE:
The L2 timings must be programmed at least as fast as the DRAM timings.

Bit	Description
15:13	**Reserved**
12	**Hit Dirty Write Cycle Timing (HDWRTIME):** When HDWRTIME = 1, the PSC performs 0 wait-state accesses (2-1-1-1) for hit dirty write cycles. When HDWRTIME = 0 (default), the access time for write hit dirty cycles is determined by WRTIME (bit 11). See Section 3.3.14.1.
11	**Write Cycle Timing (WRTIME):** When WRTIME = 1, the timing for PSC L2 cache write accesses is 3-2-2-2. In this case, the WRTIME bit is ignored for write hit dirty cycles. When WRTIME = 0 (default), the timing for PSC L2 cache write accesses is 4-2-2-2. See Section 3.3.14.1.
10:9	**Subsequent Read Timing (SUBRD):** This field determines the access time for subsequent reads to the L2 cache as shown below. **Bits[10:9] — Subsequent Cache Read Timing** 00 — X-3-3-3 (default) 01 — X-2-2-2 10 — X-1-1-1 11 — Reserved
8	**Initial Read Timing (INITRD):** This bit determines the access time for initial reads to the L2 cache. When INITRD = 1, the initial read timing is 2-X-X-X. When INITRD = 0 (default), the initial read timing is 3-X-X-X.

Bit	Description
7	**Reserved**
6	**Cache Force Hit (L2FHIT):** When L2FHIT = 0, the cache operation is normal. When L2FHIT = 1, the L2 data SRAMs are accessed, for cacheable data reads and writes, as if they were main memory. Since all data reads and writes hit the cache, none of the data cycles go to main memory. Thus, BIOS can determine the L2 cache size and configuration during POST. While L2FHIT = 1 forces a hit for cacheable data cycles, all code reads are forced to be non-cacheable. Thus, the CPU can perform code read cycles from main memory without the L2 cache generating write-back cycles and without the L2 generating code-read-allocate cycles (that may interfere with the L2 sizing algorithm). When in L2FHIT mode, the primary (L1) cache must be disabled. L2 configuration is determined by setting the cache in Interleaved mode and performing line write/read. The L2 cache size is determined by setting L2SIZE (from 64 KBytes and up) and performing a write to location (K + cache-size) and a read to location (K). When L2SIZE = 000, the L2FHIT bit has no effect.
5	**L2 Cache Force Miss Clean (L2FMISS):** When L2FMISS = 0 (default), the L2 Cache operation is normal. When L2FMISS = 1, all cacheable accesses to L2 are forced to be a cache miss. This bit is used to initialize the cache with valid locations. BIOS can set this bit and read a block of main memory equal to the cache size. This fills the cache with valid data. Once the cache is initialized, software sets this bit to 0, and the PSC keeps the cache coherent with main memory. When L2SIZE = 000 (L2 disabled), the L2FMISS bit has no effect.
4	**Cache Configuration (L2CONF):** This bit determines the configuration of the L2 cache SRAMs. For an interleaved memory configuration, L2CONF = 1 and for a non-interleaved configuration, L2CONF = 0 (default).
3	**Cache Write Policy (L2WPOL):** This bit determines the L2 cache policy. When WRPOL = 1, the L2 cache policy is write-back. When WRPOL = 0 (default), the cache policy is write-through.
2:0	**Cache Size (L2SIZE):** This field determines the L2 cache size as shown below.

Bits[2:0]	Cache Size	Bits[2:0]	Cache Size
000	L2 Cache Disabled (default)	100	512 KBytes
001	64 KBytes	101	Reserved
010	128 KBytes	110	Reserved
011	256 KBytes	111	Reserved

3.3.14.1 L2 Write Timing

Bits 11 and 12 control the write timing for the L2 cache controller. Bit 12 = 1, bit 11 = 0 is an invalid combination which will cause the PSC to lock up. The following table shows the various bit 11, 12 combinations and how they program the L2 cache controller write timings.

Bit 12	Bit 11	L2 Cache Write Timing
0	0	4-2-2-2
0	1	3-2-2-2
1	0	Invalid
1	1	2-1-1-1 (hit dirty write cycles)

3.3.15 DRAMC—DRAM CONTROL REGISTER

Address Offset: 56–57h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

The DRAMC Register selects various DRAM interface timing parameters. This register also enables/disables fast page mode for DRAM access, enables/disables CAS pipelining, and provides a refresh test option.

NOTE:
The L2 timings must be programmed at least as fast as the DRAM timings.

Bit	Description
15	**Muxed Address Hold Time (MAH):** This bit determines the number of clocks from RAS# or CAS# active before MA can be changed. When MAH is 1, the hold time is 0.5 active clocks and, when MAH is 0 (default), the hold time is 1.0 active clock.
14	**Muxed Address Setup Time (MASU):** This bit determines the number of clocks from Muxed Address driven to RAS# or CAS# active. When MASU is 1, the address setup is 0.5 active clocks and, when MASU is 0 (default), the address setup is 1.0 active clocks.
13	**CAS Write Timing (CASWR):** This bit determines the number of clocks CAS# remains active during a write access, and inactive between accesses as shown below. **Bit 13** — **Active, Inactive Clocks** 0 — 2 Active, 1 Inactive (default) 1 — 1 Active, 1 Inactive
12:11	**CAS Read Timing (CASRD):** This field determines the number of clocks CAS# remains active during a read access and inactive between accesses as shown below. **Bits[12:11]** — **Active, Inactive Clocks** 00 — 3 Active, 1 Inactive (default) 01 — 2 Active, 1 Inactive 10 — 1.5 Active, 0.5 Inactive 11 — 1 Active, 1 Inactive
10:8	**RAS Precharge Timing (RASPRE):** This field determines the minimum number of Host Bus clocks that RAS# remains inactive as shown below. **Bits[10:8]** — **RAS Pre-Charge Time** — **Bits[10:8]** — **RAS Pre-Charge Time** 000 — 4 Clocks (default) — 100 — 1.5 Clocks 001 — 3 Clocks — 101 — 1 Clock 010 — 2 Clocks — 110 — Reserved 011 — Reserved — 111 — Reserved
7:6	**Reserved**
5	**Pipelined CAS Enable (PCASEN):** When PCASEN = 1, the DRAM controller does not provide any time between CAS[3:0]# negation and CAS[7:4]# assertion (interleaved row only). When PCASEN = 0 (default), the DRAM controller provides 1 Host Bus clock between CAS[3:0]# negation and CAS[7:4]# assertion (interleaved row only).

Bit	Description
4	**Refresh Test Enable (REFTSTE):** When REFTST = 1, a test mode for the refresh generator is enabled. In this mode, a refresh request is generated every 32 HCLK cycles. When REFTST = 0 (default), the DRAM controller generates a refresh cycle every 15 μs.
3	**Fast Page Write Enable (FPWE):** This bit permits the PSC to keep the currently accessed DRAM page active following a CPU write cycle. When FPWE = 1, the PSC keeps the page open (keeps RAS# asserted) following a write cycle to main memory. When FPWE = 0 (default), the PSC closes the page (negates RAS#) following a write cycle to main memory, creating a row miss for every CPU write.
2	**Fast Page Data Read Enable (FPDRE):** This bit permits the PSC to keep the currently accessed DRAM page active following a CPU data read cycle. When FPDRE = 1, the PSC keeps the page open (keeps RAS# asserted) following a data read cycle to main memory. When FPDRE = 0 (default), the PSC closes the page (negates RAS#) following a data read cycle to main memory, creating a row miss for every CPU data read.
1	**Fast Page Code Read Enable (FPCRE):** This bit permits the PSC to keep the currently accessed DRAM page active following a CPU code read cycle. When FPCRE = 1, the PSC keeps the page open (keeps RAS# asserted) following a code read cycle to main memory. When FPCRE = 0 (default), the PSC closes the page (negates RAS#) following a code read cycle to main memory, creating a row miss for every CPU code read.
0	**Reserved**

3.3.16 PAM[6:0]—PROGRAMMABLE ATTRIBUTE MAP REGISTERS

Address Offset: PAM6(5Fh), PAM5(5Eh), PAM4(5Dh), PAM3(5Ch)
PAM2(5Bh), PAM1(5Ah) PAM0(59h)
Default Value: PAM[6:0] = 00h
Attribute: Read/Write

The 82420EX PCIset allows programmable memory and cacheability attributes on 13 memory segments of various sizes in the ISA compatibility hole—640 KByte to 1 MByte address range. Seven Programmable Attribute Map (PAM) Registers support these features. Four bits specify cacheability and memory attributes for each memory segment. These attributes are:

RE Read Enable. When RE = 1, the CPU read accesses to the corresponding memory segment are directed to main memory. Conversely, when RE = 0, the CPU read accesses are forwarded to PCI and, if not claimed on PCI, are forwarded to ISA.

WE Write Enable. When WE = 1, the PCI write accesses to the corresponding memory segment are directed to main memory. Conversely, when WE = 0, the CPU write accesses forwarded to PCI and, if not claimed on PCI, are forwarded to ISA.

CE Cache Enable. When CE = 1, the corresponding memory segment is cacheable. It is illegal to set CE = 1 and RE = 0 for the same segment. When CE = 1 and WE = 0, the corresponding memory range is not cached in the L1 cache (KEN# is negated on CPU accesses). However, it is cached and write protected in the L2 cache. The L2 cache handles cached write protected ranges as follows:

Code read (L2 miss): L2 line is allocated, data is read from main memory.
Data read (L2 miss): data is read from main memory.
Any read (L2 hit): data is read from the L2 cache
Any write: subtractively decoded to PCI Bus.

PE PCI Enable. When PE = 1, the corresponding memory range is accessible by PCI masters, as a function of the RE, WE and CE bits setting. When PE = 0, the corresponding memory range is inaccessible by PCI masters (the PCI master cycles are either claimed by PCI slaves or sent to ISA).

Each PAM Register controls two ranges as shown in Table 9.

NOTE:
The combination RE = 0 and CE = 1 is illegal.

Table 9. PAM Registers and Associated Memory Ranges

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]						Reserved	59h
PAM0[7:4]	PE	CE	WE	RE	0F0000–0FFFFFh	BIOS Area	59h
PAM1[3:0]	PE	CE	WE	RE	0C0000–0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	PE	CE	WE	RE	0C4000–0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	PE	CE	WE	RE	0C8000–0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	PE	CE	WE	RE	0CC000–0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	PE	CE	WE	RE	0D0000–0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	PE	CE	WE	RE	0D4000–0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	PE	CE	WE	RE	0D8000–0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	PE	CE	WE	RE	0DC000–0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	PE	CE	WE	RE	0E0000–0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	PE	CE	WE	RE	0E4000–0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	PE	CE	WE	RE	0E8000–0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	PE	CE	WE	RE	0EC000–0EFFFFh	BIOS Extension	5Fh

DOS Application Area (00000h–9FFFFh)

The 640 KByte DOS application area always has read, write, and cacheability attributes enabled and are not programmable for the 0–640 KByte region.

Video Buffer Area (A0000h–BFFFFh)

This 128 KByte area is not controlled by attribute bits. It is always subtractively decoded to ISA.

Expansion Area (C0000h–DFFFFh)

This 128 KByte area is divided into eight 16 KByte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled (memory that is disabled is not remapped elsewhere). Cacheability status can also be specified for each segment.

Extended System BIOS Area (E0000h–EFFFFh)

This 64 KByte area is divided into four 16 KByte segments. Each segment can be assigned independent cacheability, read, and write attributes. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000h–FFFFFh)

This area is a single 64 KByte segment. This segment can be assigned cacheability, read, and write attributes and PCI enabled.

Extended Memory Area (100000h–FFFFFFFFh)

The extended memory area can be split into several parts;

- BIOS area from 4 GByte to (4 GByte minus 512 KByte) (aliased on ISA at 16 MByte minus 15.5 MByte)
- Main memory from 1 MByte to a maximum of 128 MBytes
- PCI memory space from TOM to 128 MBytes or, (2 GBytes minus 128 MBytes) to (2 GByte plus 128 MByte), or 4 GByte to (4 GByte minus 128 MByte)

On power-up or reset the CPU vectors to the Flash BIOS area, mapped in the range of 4 GByte to 4 GByte–512 KByte. However, this area is physically mapped on ISA. Since these addresses are in the upper 4 GByte range, the request is directed to PCI. The 82420EX PCIset strips the upper address bits to effectively map the BIOS on ISA in the area between 16 MByte to 15.5 MByte.

The main memory space can occupy extended memory from a minimum of 1 MByte up to 128 MBytes. This memory is cacheable. The following areas may be occupied by PCI memory: the address space on PCI from TOM to 128 MBytes, between the Flash BIOS (4 GByte minus 512 KByte) and (4 GByte minus 128 MByte), and the range from (2 GBytes minus 128 MBytes) to (2 GByte plus 128 MByte) may be occupied by PCI memory. This memory space is not cacheable.

3.3.17 DRB—DRAM ROW BOUNDARY REGISTERS

Address Offset: DRB4(64h), DRB3(63h) DRB2(62h)
DRB1(61h), DRB0(60h)
Default Value: 01h (for each DRB)
Access: Read/Write
Size: 8 bits

The PSC supports up to 5 rows of DRAM. When populated, each row contains 32 (non-interleaved) or 64 (interleaved) bits of data. The DRAM Row Boundary registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the amount of memory in MBytes.

DRB0 = Total amount of memory in row 0 (in MBytes)
DRB1 = Total amount of memory in row 0 + row 1 (in MBytes)
DRB2 = Total amount of memory in row 0 + row 1 + row 2 (in MBytes)
DRB3 = Total amount of memory in row 0 + row 1 + row 2 + row 3 (in MBytes)
DRB4 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row4 (in MBytes)

The DRAM array can be configured with SIMMs that have address depths of 256 KByte, 1 MByte, and 4 MByte. Each register defines an address range that causes a particular RAS# line to assert (e.g. if the first DRAM row is 2 MBytes in size, then accesses within the 0 to 2 MByte range causes the RAS0# line to be asserted). The DRAM Row Boundary (DRB) Registers are programmed with an 8-bit upper address limit value.

Bit	Description
7:0	**Memory Boundary in MBytes:** This 8-bit value is used to determine the upper address limit of this row (i.e., this row - previous row = row size). Unpopulated rows have a value equal to the previous row (row size = 0). The value programmed into DRB4 always reflects the maximum amount of DRAM in the system.

Example 1:
If SIMM0 contains a 256K x 36 SIMM,(which is equivalent to 1 MByte DRAM), DRB0 is set to 01h. If this is the only SIMM in the system, DRB[4:1] are each set to 01h.

Example 2:
One way to achieve maximum main memory is to populate SIMMs 0-3 with 8M x 36 double-sided SIMMs (which have 32 MBytes each). In this case, DRB[4:0] would be programmed as follows: DRB0 = 20h, DRB1 = 40h, DRB2 = 60h, DRB3 = 80h, DRB4 = 80h.

3.3.18 PIRQ1RC/PIRQ0RC—PIRQ ROUTE CONTROL REGISTERS

Address Offset: 66h (PIRQ0RC)
67h (PIRQ1RC)
Default Value: PIRQ0RC 80h
PIRQ1RC 80h
Attribute: Read/Write
Size: 8 bits

The PIRQ1RC/PIRQ0RC Registers control the routing of PIRQ[1:0] signals to the internal IRQ inputs of the interrupt controller. Each PIRQx# can be independently routed to any one of 11 interrupts. One or both PIRQx# lines can be routed to the same IRQx input. Note that the IRQ selected through bits[3:0] must be set to level sensitive mode in the corresponding ELCR Register.

Bit	Description
7	**PIRQx Interrupt Signal Routing Enable:** When bit 7 = 0 (enabled), PIRQx# is routed to the IRQ selected by bits[3:0] of this register. When bit 7 = 1 (disabled: default), the PIRQx# signal is not routed to any IRQ line.
6:4	**Reserved:** Read as zeros.
3:0	**PIRQx Interrupt Signal Routing:** When bit 7 = 0, bits[3:0] select how each PIRQx# is routed to each internal 8259 IRQx. The routing for different values of this field are shown below.

Bits[3:0]	PIRQx Interrupt Routing	Bits[3:0]	PIRQx Interrupt Routing
0000	Reserved (default)	1000	Reserved
0001	Reserved	1001	IRQ9
0010	Reserved	1010	IRQ10
0011	IRQ3	1011	IRQ11
0100	IRQ4	1100	IRQ12
0101	IRQ5	1101	Reserved
0110	IRQ6	1110	IRQ14
0111	IRQ7	1111	IRQ15

3.3.19 DMH—DRAM MEMORY HOLE REGISTER

Address Offset: 68h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The DMH Register defines a hole in main memory between 1 MByte and 16 MBytes. ISA memory accesses to the region defined by the memory hole are not forwarded to main memory. The ISA cycle is confined to the ISA Bus.

Bit	Description
7	**Memory Hole Enable (MHE):** When MHOLEE = 1, the memory hole is enabled and all ISA master and DMA accesses within the programmed hole are confined to the ISA Bus. All CPU and PCI master accesses within the hole are forwarded to the PCI/ISA Bus. When MHOLEE = 0 (default), the memory hole is disabled.
6:4	**Memory Hole Size (MHSIZE):** This field selects the memory hole size as shown in the table below.
3:0	**Memory Hole Start Address (MHSTRT):** This four bit field defines the starting address of the memory hole. Bits[3:0] correspond to A[23:20], respectively. The memory hole starting address can be between 1 MByte and 16 MBytes, with 1 MByte granularity. Note that the top of the memory hole range must be below 16 MBytes. It is the responsibility of the BIOS to set the hole size and starting address accordingly.

Bits[6:4]	Memory Hole Size	Bits[6:4]	Memory Hole Size
000	1 MByte (default)	100	Reserved
001	2 MBytes	101	Reserved
010	Reserved	110	Reserved
011	4 MBytes	111	8 MBytes

3.3.20 TOM—TOP OF MEMORY

Address Offset: 69h
Default Value: 02h
Attribute: Read/Write
Size: 8 bits

The 82420EX PCIset supports up to 128 MBytes of system memory. The Top Of Memory Register must be set by the BIOS to the value of the DRB4 Register plus the memory hole size. For example, the top of memory for a system with 16 MBytes of DRAMs, and a 1 MByte Hole (somewhere between 1 and 16 MBytes), is at 17 MBytes.

The TOM Register is programmed with an 8-bit upper address limit value. This upper address limit is compared to A[31:30,26:20] of the Host address bus to determine if main memory is being targeted. When A[31:30,26:20] < TOM, and the access is not to the memory hole, main memory is being targeted. Otherwise, a PCI or ISA region is being targeted. Bits[7:0] of this register correspond to A[31:30,26:20].

Note that SMRAM can be placed at the top of memory between TOM-64 KByte and TOM. Note, also, that the maximum supported DRAM size is 128 MBytes minus the Memory Hole size.

For use with operating systems other than Windows*, DOS*, and OS/2*, the TOM register should not be programmed with a value of greater than 127M.

*Other brands and names are the property of their respective owners.

3.3.21 SMRAMCON—SMRAM CONTROL REGISTER

Address Offset: 70h
Default Value: 00h
Attribute: Read/Write
Size: 8 Bits

The SMRAMCON Register sets the SMRAM location and attributes. SMRAM is always located in main memory and it is always non-cacheable. The memory block that shares the same bus address range with SMRAM is also non-cacheable (even if it is defined as cacheable by other configuration settings).

Bit	Description
7	**Reserved**
6	**SMRAM Space Open (SMOPN):** This bit manually opens SMRAM space. When SMOPN = 1, CPU accesses (only CPU accesses) to SMRAM are re-mapped (see SMBASE description). BIOS uses this bit to manually open the SMRAM when the CPU is not in SMM. SMOPN is used by the BIOS to initialize the SMRAM. Setting the SMOPN bit to 1 has no effect when the CPU is in SMM (SMLCK bit is 1) or when the CPU is not the current system master (HLDA = 1).
5	**SMRAM Close (SMCLS):** This bit manually closes SMRAM space. The SMI handler uses SMCLS to access the physical memory block that shares the same bus address range with SMRAM. When SMCLS = 1, re-mapping of SMRAM (code and data) is disabled. This permits the CPU to access the data in system memory that is aliased by SMM memory, even when the CPU is in SMM. Note that SMCLS affects data accesses only; code read cycles are not affected.
4	**SMRAM Lock (SMLCK):** SMLCK locks SMRAM space from manual opening. When SMLCK = 1, the SMOPN function is disabled, as well as write protecting the SMBASE. The SMLCK bit is a write once bit. This means that once set, this bit cannot be cleared by software. Only a CPURST clears this bit. SMLCK permits BIOS, after initialization is complete, to protect the SMRAM from other programs. Once SMLCK is set to 1, no manual opens of the SMRAM are possible.
3	**Reserved**
2:0	**SMRAM Base Address (SMBASE):** SMBASE selects the SMRAM segment. Based on this selection, the SMRAM address is re-mapped as shown below. The setting of the SMRAM range forces the CPU bus range to be non-cacheable, regardless of other bit settings. The following table describes some SMBASE values and attributes.

Bits[2:0]	CPU Range	DRAM Range	Non-CPU Cycles Are Sent to:	Comments
000				Reserved
001				Reserved
010	A0000–AFFFFh	A0000–AFFFFh	Subtractively to PCI/ISA	PCI/ISA graphic frame buffer region. Region can not be used as SMRAM if it is also used as a graphic frame buffer of a Host Bus device.
011	B0000–BFFFFh	B0000–BFFFFh		
100	C0000–CFFFFh	A0000–AFFFFh	Main memory or subtractively PCI/ISA, Function of registers setting.	
101	D0000–DFFFFh	A0000–AFFFFh		
110	E0000–EFFFFh	A0000–AFFFFh		
111	F0000–FFFFFh	A0000–AFFFFh		

3.3.22 SMICNTL—SMI CONTROL REGISTER

Address Offset: A0h
Default Value: 08h
Attribute: Read/Write
Size: 8 Bits

The SMICNTL Register provides Fast Off Timer control, STPCLK# enable/disable, and throttle control. This register also enables/disables the system management interrupt (SMI).

NOTE:
Bits[4:3] = 01 can be used to freeze the Fast Off Timer when in SMM. Freezing the Fast Off Timer prevents time-outs from occurring while executing SMM code. This prevents the system from being confused by asynchronous events that could happen while servicing SMM code.

Bit	Description
7:5	**Reserved**
4:3	**Fast Off Timer Control (CTMRCNTL):** This field enables/disables the Fast Off Timer and when enabled, selects the timer's counting granularity as shown below. **Bits[4:3]** / **Count Granularity for 33 MHz Host Bus Operation** / **Count Granularity for 25 MHz Host Bus Operation** 00 / 1 Minute / 1.32 Minutes 01 / Disabled (default) / Disabled (default) 10 / 1 HCLKIN / 1 HCLKIN 11 / 1 msec / 1.32 msec
2	**STPCLK# Signal Throttle Enable (CSTPCLKTHE):** This bit enables/disables control of the STPCLK# high/low times by the clock throttle timers. When bit 2 = 1, the STPCLK# signal throttle control is enabled. When enabled (and bit 1 = 1, enabling the STPCLK# signal), the high and low times for the STPCLK# signal are controlled by the Clock Throttle STPCLK# High Timer and Clock Throttle STPCLK# Low Timer Registers, respectively. When bit 2 = 0 (default), the throttle control of the STPCLK# signal is disabled.
1	**STPCLK# Signal Enable (CSTPCLKE):** This bit permits software to place the CPU into a low power state. When bit 1 = 1, the STPCLK# signal is enabled and a read from the APMC Register causes STPCLK# to be asserted. When bit 1 = 0 (default), the STPCLK# signal is disabled and is negated (high). Software can set this bit to 0 by writing a 0 to it.
0	**SMI# Gate (CSMIGATE):** When bit 0 = 1, the SMI# signal is enabled and a system management interrupt condition causes the SMI# signal to be asserted. When bit 0 = 0 (default), the SMI# signal is masked and negated. This bit only affects the SMI# signal and does not affect the detection/recording of SMI events (i.e., this bit does not affect the SMI status bits in the SMIREQ Register). Thus, SMI conditions can be pending when this bit is set to 1. If an SMI is pending when this bit is set to 1, the SMI# signal is asserted.

3.3.23 SMIEN—SMI ENABLE REGISTER

Address Offset: A2–A3h
Default Value: 0000h
Attribute: Read/Write
Size: 16 Bits

This register enables the generation of SMI (asserting the SMI# signal) for the associated hardware events (bits[5:0]), external SMI signal (bit 6), and software events (bit 7). When a hardware event is enabled, the occurrence of a corresponding event results in the assertion of SMI#, if enabled via the SMICNTL Register. The SMI# is asserted independent of the current power state (Power-On or Fast Off). The default for all sources in this register is disabled.

Bit	Description
15:8	**Reserved**
7	**APMC Write SMI Enable:** This bit enables SMI for writes to the APMC Register. When bit 7 = 1, writes to the APMC Register generate an SMI. When bit 7 = 0, writes to the APMC Register do not generate an SMI.
6	**EXTSMI# Signal SMI Enable:** When bit 6 = 1, asserting the EXTSMI# input signal generates an SMI. When bit 6 = 0, asserting EXTSMI# does not generate an SMI.
5	**Fast Off Timer SMI Enable:** This bit enables the Fast Off Timer to generate an SMI. When bit 5 = 1, the timer generates an SMI when it decrements to zero. When bit 5 = 0, the timer does not generate an SMI.
4	**IRQ12 SMI Enable (PS/2 Mouse Interrupt):** This bit enables the IRQ12 signal to generate an SMI. When bit 4 = 1, asserting the IRQ12 input signal generates an SMI. When bit 4 = 0, asserting IRQ12 does not generate an SMI.
3	**IRQ8 SMI Enable (RTC Alarm Interrupt):** This bit enables the IRQ8 signal to generate an SMI. When bit 3 = 1, asserting the IRQ8 input signal generates an SMI. When bit 3 = 0, asserting IRQ8 does not generate an SMI.
2	**IRQ4 SMI Enable (COM2/COM4 Interrupt or Mouse):** This bit enables the IRQ4 signal to generate an SMI. When bit 2 = 1, asserting the IRQ4 input signal generates an SMI. When bit 2 = 0, asserting IRQ4 does not generate an SMI.
1	**IRQ3 SMI Enable (COM1/COM3 Interrupt or Mouse):** This bit enables the IRQ3 signal to generate an SMI. When bit 1 = 1, asserting the IRQ3 input signal generates an SMI. When bit 1 = 0, asserting IRQ3 does not generate an SMI.
0	**IRQ1 SMI Enable (Keyboard Interrupt):** This bit enables the IRQ1 signal to generate an SMI. When bit 0 = 1, asserting the IRQ1 input signal generates an SMI. When bit 0 = 0, asserting IRQ1 does not generate an SMI.

3.3.24 SEE—SYSTEM EVENT ENABLE

Address Offset: A4–A7h
Default Value: 00000000h
Attribute: Read/Write
Size: 32 Bits

This register enables hardware events as system events or break events for power management control. Note that all of the functional bits in the SEE Register provide system event control. In addition, all bits provide break event control. The default for each system/break event in this register is disabled.

System Events: Activity by these events can keep the system from powering down. When a system event is enabled, the corresponding hardware event activity prevents a Fast Off powerdown condition. Anytime the corresponding hardware event occurs (signal is asserted), the Fast Off Timer is re-loaded with its initial count.

Break Events: These events can awaken a powered down system. When a break event is enabled, the corresponding hardware event activity powers up the system by negating STPCLK#. Note that STPCLK# is not negated until the stop grant special cycle has been generated by the CPU. Thus, from the time that STPCLK# is asserted until the stop grant cycle is returned, the occurrence of subsequent break events are latched in the IB.

NOTE:

Bit 30 in this register is used as a global break event and should be set to 1 if ISA cards that generate IRQ's by driving them low and then high and keeping them high until another interrupt is generated, are supported. Refer to the bit description.

SRESET is always enabled as a break event. However, SRESET only causes a break event after a stop grant special cycle has been received. If SRESET is asserted while STPCLK# is active and then negated before the stop grant cycle is received, SRESET does not cause a break event.

Bit	Description
31	**Fast Off SMI Enable (FSMIEN):** When bit 31 = 1 (enabled), an SMI causes a system event that re-loads the Fast Off Timer and a break event that negates the STPCLK# signal. When bit 31 = 0 (disabled), an SMI does not re-load the Fast Off Timer or negate the STPCLK# signal.
30	**INTR Enable (FINTREN):** When bit 30 of this register is set to 1, INTR will be used as a global break event. In this case, any IRQ that is generated will cause the system to power-up via the negation of STPCLK#, regardless of the state of bits 0, 1, and 3 through 15 in this register. When this bit is set to 0, INTR is not used as a break event and bits 0, 1, and 3 through 15 can be used to individually enable/disable break events. Note that this bit has no effect on the setting of system events and only effects the break event function.
29	**Fast Off NMI Enable (FNMIEN):** When bit 29 = 1 (enabled), an NMI (e.g., parity error) causes a system event that re-loads the Fast Off Timer and a break event that negates the STPCLK# signal. When bit 29 = 0 (disabled), an SMI does not re-load the Fast Off Timer or negate the STPCLK# signal.
28:16	**Reserved**

Bit	Description
15:3	**Fast Off IRQ[15:3] Enable:** These bits are used to prevent the system from entering Fast Off and break any current powerdown state when the selected hardware interrupt occurs. When a bit = 1 (enabled), the corresponding interrupt causes a system event that re-loads the Fast Off Timer and a break event that negates the STPCLK# signal. When a bit = 0 (disabled), the corresponding interrupt does not re-load the Fast Off Timer or negate the STPCLK# signal.
2	**Reserved**
1:0	**Fast Off IRQ[1:0] Enable:** These bits are used to prevent the system from entering Fast Off and break any current powerdown state when the selected hardware interrupt occurs. When a bit = 1, the corresponding interrupt causes a system event that re-loads the Fast Off Timer and a break event that negates the STPCLK# signal. When a bit = 0 (disabled), the corresponding interrupt does not re-load the Fast Off Timer or negate the STPCLK# signal.

3.3.25 FTMR—FAST OFF TIMER REGISTER

Address Offset: A8h
Default Value: 0Fh
Attribute: Read/Write
Size: 8 Bits

The Fast Off Timer is used to indicate (through an SMI) that the system has been idle for a pre-programmed period of time. The Fast Off Timer consists of a count-down timer and the count down value programmed into this register. The Fast Off Timer count down value is (x + 1) where x equals the value programmed in the Fast Off Timer register and the unit of measurement is in minutes or msec, depending on the value of bits 4–3 in the SMI Control register. The Fast Off Timer count down value is loaded into the Fast Off Timer when an enabled system event occurs. When the timer expires, an SMI special cycle is generated. When the Fast Off Timer is enabled (bits[4:3] = 00, 10, or 11 in the SMICNTL register), the timer counts down from the Fast Off Timer count down value. The count time interval is programmable (via the SMICNTL Register). When the Fast Off Timer reaches 00h, an SMI is generated and the timer is re-loaded with the Fast Off Timer count down value. If an enabled system event occurs before the Fast Off Timer reaches 00h, the Fast Off Timer is re-loaded with the Fast Off Timer count down value. Note that the Fast Off Timer should never be programmed to a value of 00h.

NOTE:
Before writing to the FTMR Register, the Fast Off Timer must be stopped by setting bits[4:3] to 01 in the SMICNTL Register. The Fast Off Timer will begin decrementing when the these bits are subsequently set to 00, 10, or 11.

Bit	Description
7:0	**Fast Off Timer Value:** Bits[7:0] contain value x, where the Fast Off Timer count down value is (x + 1). A read from the FTMR Register returns the value last written.

3.3.26 SMIREQ—SMI REQUEST REGISTER

Address Offset: AA–ABh
Default Value: 00h
Attribute: Read/Write
Size: 16 Bits

The SMIREQ Register contains status bits indicating the cause of an SMI. When an enabled event causes an SMI, the IB automatically sets the corresponding event's status bit to 1. Software sets the status bits to 0 by writing a 0 to them.

The SMI handler can query the status bits to see what caused the SMI and then branch to the appropriate routine. As the individual routines complete, the handler resets the appropriate status bit by writing a 0 to the corresponding bit.

Each of the SMIREQ bits is set by the IB in response to the activation of the corresponding SMI event. If the SMI event is still active when the corresponding SMIREQ bit is set to 0, the IB does not set the status bit back to a 1 (i.e., there is only one status indication per active SMI event).

When an IRQx signal is asserted, the corresponding RIRQx bit is set to a 1. If the IRQx signal is still active when software sets the RIRQx bit to 0, RIRQx is not set back to a 1. The IRQx may be negated before software sets the RIRQx bit to 0. If the RIRQx bit is set to 0 at the same time a new IRQx is activated, RIRQx remains set to 1. This indicates to the SMI handler that a new SMI event has been detected.

NOTE:
The SMIREQ bits are set, cleared, or read independently of each other and independently of the CSMIGATE bit in the SMICNTL Register.

Bit	Description
15:8	**Reserved**
7	**APM SMI Status (RAPMC):** The IB sets this bit to 1 to indicate that a write to the APM Control Register caused an SMI. Software sets this bit to a 0 by writing a 0 to it.
6	**EXTSMI# SMI Status (REXT):** The IB sets this bit to 1 to indicate that EXTSMI# caused an SMI. Software sets this bit to a 0 by writing a 0 to it.
5	**Fast Off Timer Expired Status (RFOT):** The IB sets this bit to 1 to indicate that the Fast Off Timer expired and caused an SMI. Software sets this bit to a 0 by writing a 0 to it.
4	**IRQ12 Request SMI Status (RIRQ12):** The IB sets this bit to 1 to indicate that IRQ12 caused an SMI. Software sets this bit to a 0 by writing a 0 to it.
3	**IRQ8# Request SMI Status:** The IB sets this bit to 1 to indicate that IRQ8# caused an SMI. Software sets this bit to a 0 by writing a 0 to it.
2	**IRQ4 Request SMI Status:** The IB sets this bit to 1 to indicate that IRQ4 caused an SMI. Software sets this bit to a 0 by writing a 0 to it.
1	**IRQ3 Request SMI Status:** The IB sets this bit to 1 to indicate that IRQ3 caused an SMI. Software sets this bit to a 0 by writing a 0 to it.
0	**IRQ1 Request SMI Status:** The IB sets this bit to 1 to indicate that IRQ1 caused an SMI. Software sets this bit to a 0 by writing a 0 to it.

3.3.27 CTLTMRL—CLOCK THROTTLE STPCLK# LOW TIMER

Address Offset: ACh
Default Value: 00h
Attribute: Read/Write
Size: 8 Bits

The duration of the STPCLK# asserted period when bit 2 in the SMICNTL Register is set to 1 is (x + 1) where x equals the value programmed in this register. The value in this register plus 1 is loaded into the STPCLK# Timer when STPCLK# is asserted. However, the timer does not start until the Stop Grant Bus Cycle is received. The STPCLK# timer counts using a 32 μs clock.

Bit	Description
7:0	**Clock Throttle STPCLK# Low Timer Value:** Bits[7:0] define the value x, where the Clock Throttle STPCLK# Low Timer count down value is (x + 1). (x + 1) defines the duration of the STPCLK# asserted period during clock throttling.

3.3.28 CTLTMRH—CLOCK THROTTLE STPCLK# HIGH TIMER

Address Offset: AEh
Default Value: 00h
Attribute: Read/Write
Size: 8 Bits

The duration of the STPCLK# negated period when bit 2 in the SMICNTL Register is set to 1 is (x + 1) where x equals the value programmed in this register. The value in this register plus 1 is loaded into the STPCLK# Timer when STPCLK# is negated. The STPCLK# timer counts using a 32 μs clock.

Bit	Description
7:0	**Clock Throttle STPCLK# High Timer Value:** Bits[7:0] define the value x, where the Clock Throttle STPCLK# High Timer count down value is (x + 1). (x + 1) defines the duration of the STPCLK# negated period during clock throttling.

3.4 ISA-Compatible Registers

This section describes the ISA-Compatible registers consisting of the DMA, interrupt controller, timer/counter, X-Bus control, NMI control, clock/reset, and advanced power management registers. Some of the registers are only accessible from the CPU/PCI Buses while others can be accessed by the CPU, PCI, or ISA Buses (see Table 7).

3.4.1 DMA REGISTER DESCRIPTION

The IB contains DMA circuitry that incorporates the functionality of two 82C37 DMA controllers. The two DMA controllers consist of two logical channel groupschannels [3:0] (Controller 1DMA1) and channels [7:4] (Controller 2DMA2).

This section describes the DMA registers. Unless otherwise stated, a CPURST sets each register to its default value. In addition, the DMA Master Clear Command (address 00Dh for channels [3:0] and 0DAh for channels [7:4]) permits software to set the DMA Command, DMA Status, DMA Request, and internal First/Last Flip-Flop Registers to their default values. The DMA Master Clear Command also sets the mask registers to their default values.

3.4.1.1 DCOM—DMA Command Register

I/O Address: Channels [3:0]—08h
Channels [7:4]—0D0h
Default Value: 00h
Attribute: Write Only
Size: 8 bits

This 8-bit register enables/disables the DMA channel groups, selects the priority scheme for responding to DMA requests, and selects the DMA request signal (DREQ) sense level. Following a CPURST or DMA Master Clear, both DMA1 and DMA2 are enabled in fixed priority and the DREQ sense level is active high.

Bit	Description
7	**DACK# Active Level (DACK[3:0,(7:5)] #):** Bit 7 controls the DMA channel request acknowledge (DACK#) assertion level. When bit 1 = 1, DACK# is an active high signal. When bit 1 = 0 (default), DACK# is an active low signal.
6	**DREQ Sense Assert Level (DREQ[3:0, (7:5)]):** Bit 6 controls the DREQx signal assertion level that the DMA controller detects as an active DMA channel request. Note that the DREQ channel assertion sensitivity is assigned by channel group, not per individual channel. When bit 6 = 0 (default), the DREQx sense assert level is active high. When bit 6 = 1, the DREQx sense assert level is active low. Following CPURST, the DREQx sense assert level is active high.
5	**Reserved:** Must be 0 when programming this register.
4	**DMA Group Arbitration Priority:** For priority resolution, the DMA consists of two logical channel groups—channels [3:0] (Controller 1—DMA1) and channels [7:4] (Controller 2—DMA2). Each group can be assigned fixed or rotating priority. Thus, both groups can be assigned fixed priority, one group can be assigned fixed priority and the other rotating priority, or both groups can be assigned rotating priority. When bit 4 = 0 (default), fixed priority is assigned to the channel. For fixed priority, the priority ordering is 0 (highest priority), 1, 2, 3, 5, 6, and 7 (lowest priority). Channels [3:0] of DMA-1 assume the priority position of Channel 4 in DMA-2, thus taking priority over channels 5, 6, and 7. Following CPURST, each group is initialized in fixed priority. When bit 4 = 1, rotating priority is assigned to the channel group. For rotating priority, the priority chain rotates so that the last channel serviced is assigned the lowest priority in the channel group ([3:0] or [7:5]). Channels [3:0] rotate as a group of 4. They are always placed between Channel 5 and Channel 7 in the priority list. Channel [7:5] rotate as part of a group of 4. That is, channels [7:5] form the first three positions in the rotation, while channels [3:0] comprise the fourth position in the arbitration.
3	**Reserved:** Must be 0 when programming this register.
2	**DMA Channel Group Enable:** When bit 2 = 1, the DMA channel group is disabled. Note that disabling channel group [7:4] also disables channel group [3:0], which is cascaded through channel 4. When bit 2 = 0 (default), the DMA channel group is enabled. Following CPURST, both channel groups are enabled.
1:0	**Reserved:** Must be 0 when programming this register.

3.4.1.2 DCM—DMA Channel Mode Register

I/O Address: Channels [3:0]—0Bh
Channels [7:4]—0D6h
Default Value: Bits[7:2] = 0, Bits[1:0] = undefined
Attribute: Write Only
Size: 8 bits

The Channel Mode Register controls DMA transfer type, transfer mode, address increment/decrement, and autoinitialization. The DMA transfer mode for channel 4 defaults to cascade and cannot be programmed for any mode other than DMA transfer mode.

Bit	Description
7:6	**DMA Transfer Mode:** Bits[7:6] select the DMA transfer mode as shown below. **Bits[7:6] — DMA Transfer Mode** 00 — Demand (default) 01 — Single 10 — Block 11 — Cascade
5	**Address Increment/Decrement Select:** Bit 5 controls address increment/decrement during multi-byte DMA transfers. When bit 5 = 0 (default), address increment is selected. When bit 5 = 1, address decrement is selected.
4	**Autoinitialize Enable:** When bit 4 = 1, the DMA restores the base page, address, and word count information to their respective current registers following a terminal count (TC). When bit 4 = 0 (default), the autoinitialize feature is disabled and the DMA does not restore the above mentioned registers.
3:2	**DMA Transfer Type:** This field selects verify, write, or read data transfer types as shown below. Write transfers move data from an I/O device to memory. Read transfers move data from memory to an I/O device. Verify transfers are pseudo transfers; addresses are generated as in a normal read or write transfer. However, with Verify transfers, the ISA memory and I/O cycle lines are not driven. When the channel is programmed for cascade (bits[7:6] = 11), the transfer type bits are irrelevant. **Bits[3:2] — DMA Transfer Type** 00 — Verify (default) 01 — Write 10 — Read 11 — Illegal: do not write
1:0	**DMA Channel Select:** This field select the DMA Channel Mode Register that will be written by bits[7:2] as shown below. These bits are undefined after a hard reset. **Bits[1:0] — DMA Channel Select** 00 — Channel 0(4) 01 — Channel 1(5) 10 — Channel 2(6) 11 — Channel 3(7)

3.4.1.3 DREQ—DMA Request Register

I/O Address: Channels [3:0]—09h
Channels [7:4]—0D2h
Default Value: Bits[1:0] = undefined, Bits[7:2] = 0
Attribute: Write Only
Size: 8 bits

The DMA Request Register is used by software to initiate a DMA request. The DMA responds to the software request as though DREQx is asserted. These requests are non-maskable and subject to prioritization by the priority encoder. When a TC is generated, the channel's request bit is set to 0. For software DMA requests, the channel must be in Block Mode. Note that the DMA Request Register status for DMA1 and DMA2 can be obtained from bits[7:4] of the DMA Status Register. The request bit for each channel is set to its default value by a CPURST or a Master Clear. The register is not affected by the RSTDRV output.

Bit	Description
7:3	**Reserved:** Must Be 0 when programming this register.
2	**DMA Channel Service Request:** When bit 2 = 1, a software DMA transfer is requested for the channel specified by bits[1:0]. When bit 2 = 0 (default), software DMA transfers are not requested for the channel specified by bits[1:0].
1:0	**DMA Channel Select:** This field selects the DMA channel to be written by bit 2 as shown below. **Bits[1:0] — DMA Channel Select** 00 — Channel 0(4) 01 — Channel 1(5) 10 — Channel 2(6) 11 — Channel 3(7)

3.4.1.4 WSMB—Write Single Mask Bit Register

I/O Address: Channels [3:0]—0Ah
Channels [7:4]—0D4h
Default Value: Bits[1:0] = undefined, Bit 2 = 1, Bits[7:3] = 0
Attribute: Write Only
Size: 8 bits

The WSMB Register permits the masking of the incoming DMA requests (DREQx) for each channel. A channel's mask bit is automatically set when the Current Byte/Word Count Register reaches terminal count, unless the channel is programmed for autoinitialization. This register is set to its default value by a CPURST or a Master Clear. Setting the entire register disables all DMA requests until a Clear Mask Register instruction allows them to occur. This instruction format is similar to the format used with the DMA Request Register.

NOTE:
Individually masking DMA channel 4 (DMA controller 2, channel 0) automatically masks DMA channels [3:0], as this channel group is logically cascaded onto channel 4. Setting this mask bit disables the incoming DREQ's for channels [3:0].

Bit	Description
7:3	**Reserved:** Must be 0 when programming this register.
2	**Channel Mask Select:** When bit 2 = 1 (default), DREQ is masked (disabled) for the channel selected by bits[1:0]. When bit 2 = 0, DREQ is not masked (enabled) for the channel selected by bits[1:0].
1:0	**DMA Channel Select:** This field selects the DMA channel to be written by bit 2 as shown below. **Bits[1:0] — DMA Channel Select** 00 — Channel 0(4) 01 — Channel 1(5) 10 — Channel 2(6) 11 — Channel 3(7)

3.4.1.5 WAMB—Write All Mask Bits Register

I/O Address: Channels [3:0]—0Fh
Channels [7:4]—0DEh
Default Value: Bit[3:0] = 1, Bit[7:4] = 0
Attribute: Read/Write
Size: 8 bits

This register enables/disables the incoming DREQx signals. All four channels can be simultaneously enabled/disabled instead of enabling/disabling each channel individually, as is the case with the Write Single Mask Bit Register.

Unlike the WSMB Register, the WAMB Register includes a status read to check the current mask status of the selected DMA channel group. A channel's mask bit is automatically set to 1 when the Current Byte/Word Count Register reaches terminal count, unless the channel is programmed for autoinitialization. All mask bits are set to 1 (disable) by CPURST or a Master Clear. Setting these bits to 1 disables all DMA requests until a Clear Mask Register instruction enables the requests.

NOTES:

1. Individually masking DMA channel 4 (DMA controller 2, channel 0) automatically masks DMA channels [3:0], as this channel group is logically cascaded onto channel 4.
2. Masking DMA controller 2 with a write to address 0DEh also masks DREQ assertions from the DMA controller, as this channel group is logically cascaded onto channel 4. When DMA channel 4 is masked, so are DMA channels [3:0].

Bit	Description
7:4	**Reserved:** Must be 0 when programming this register.
3:0	**Channel Mask Bits:** Setting the bit(s) to a 1 (default) disables the corresponding DREQ(s). Setting the bit(s) to a 0 enables the corresponding DREQ(s). When read, bits[3:0] indicate the DMA channel [3:0] ([7:4]) mask status.

3.4.1.6 DS—DMA Status Register

I/O Address: Channels [3:0]—08h
Channels [7:4]—0D0h
Default Value: 00h
Attribute: Read Only
Size: 8 bits

This register indicates which channels have reached terminal count and which channels have a pending DMA request.

Bit	Description
7:4	**Channel Request Status:** When a valid DMA request is pending for a channel (on its DREQ signal line), the corresponding bit is set to 1. When a DMA request is not pending for a particular channel, the corresponding bit is set to 0. The source of the DREQ may be hardware or a software request. Note that channel 4 does not have DREQ or DACK lines, so the response for a read of DMA2 status for channel 4 is irrelevant.
3:0	**Channel Terminal Count Status:** When a channel reaches terminal count (TC), its status bit is set to 1. If TC has not been reached, the status bit is set to 0. Note that channel 4 is programmed for cascade, and is not used for a DMA transfer. Therefore, the TC bit response for a status read on DMA2 for channel 4 is irrelevant. Bits[3:0] are set to 0 upon CPURST and on a read of the DS Register.

3.4.1.7 DB&CA—DMA Base And Current Address Registers (8237 Compatible Segment)

I/O Address: DMA Channel 0—000h, DMA Channel 1—002h, DMA Channel 2—004h,
DMA Channel 3—006h, DMA Channel 4—0C0h, DMA Channel 5—0C4h,
DMA Channel 6—0C8h, DMA Channel 7—0CCh
Default Value: Undefined
Attribute: Read/Write
Size: 16 bits per channel

Each channel has a 16-bit Current Address Register. This register contains the value of the 16 least significant bits of the full 27-bit address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address Register during the transfer. The Host CPU reads/writes the register in successive 8-bit bytes. This register is not accessible by ISA Bus masters. The programmer must issue the Clear Byte Pointer Flip-Flop Command to reset the internal byte pointer and correctly align the write prior to programming the Current Address Register. After clearing the Byte Pointer Flip-Flop, the first read/write accesses the low byte (bits[7:0]), and the second read/write accesses the high byte (bits[15:8]). Note that a mixed sequence of read and write cycles continues to toggle the Byte Pointer Flip-Flop, and successive reads and writes from this register alternate between the low byte and the high byte. An autoinitialize re-initializes the Current Address Register back to its original value following a TC. Autoinitialize occurs only after a TC.

Each channel has a Base Address Register located at the same address as the corresponding Current Address Register. These registers store the original value of their associated Current Address Registers. During autoinitialize these values are used to restore the Current Address Registers to the original values. The Base Registers are written simultaneously with their corresponding Current Address Register in successive 8-bit bytes. The Base Registers are write only.

Bit	Description
15:0	**Base and Current Address[15:0]:** These bits represent the 16 least significant address bits used during DMA transfers. Together with the DMA Low Page Register, they form the ISA-Compatible 24-bit DMA address. As an extension of the ISA-Compatible functionality, the DMA High Page Register completes the 27-bit DMA address generation, supporting DMA transfers throughout the full 128 MBytes of main memory. Upon CPURST or Master Clear, the value of these bits are undefined.

3.4.1.8 DB&CBW—DMA Base And Current Byte/Word Count Registers (8237 Compatible Segment)

I/O Address: DMA Channel 0—001h, DMA Channel 1—003h, DMA Channel 2—005h, DMA Channel 3—007h, DMA Channel 4—0C2h, DMA Channel 5—0C6h, DMA Channel 6—0CAh, DMA Channel 7—0CEh
Default Value: Undefined
Attribute: Read/Write
Size: 16 bits per channel

Each channel has a 16-bit Current Byte/Word Count Register that determines the number of transfers to be performed. The actual number of transfers is one more than the number programmed in the Current Byte/Word Count Register (i.e., programming a count of 100 results in 101 transfers). The byte/word count is decremented after each transfer. The intermediate value of the byte/word count is stored in the register during the transfer. When the value in the register goes from 0000h to FFFFh, a TC is generated.

Following the end of a DMA service, the register may also be re-initialized by an autoinitialization back to its original value. Autoinitialize can only occur when a TC occurs. If it is not autoinitialized, this register has a count of FFFFh after TC.

For transfers to/from an 8-bit I/O, the byte/word count indicates the number of bytes to be transferred. This applies to DMA channels [3:0]. For transfers to/from a 16-bit I/O, with shifted address, the byte/word count indicates the number of 16-bit words to be transferred. This applies to DMA channels [7:5].

Each channel has a Base Byte/Word Count Register located at the same I/O address as the corresponding Current Byte/Word Count Register. These registers store the original value of their associated Current Byte/Word Count Registers. During autoinitialize, these values are used to restore the Current Registers to their original values. The Base Registers are written simultaneously with their corresponding Current Register in successive 8-bit bytes. The Base Registers cannot be read by external agents.

Bit	Description
15:0	**Base and Current Byte/ Word Count:** These bits represent the 16 byte/word count bits used when counting down a DMA transfer. Upon CPURST or Master Clear, the value of these bits are undefined.

3.4.1.9 DMLPG—DMA Memory Low Page Registers

I/O Address: DMA Channel 0—087h, DMA Channel 1—083h, DMA Channel 2—081h, DMA Channel 3—082h, DMA Channel 5—08Bh, DMA Channel 6—089h, DMA Channel 7—08Ah
Default Value: Undefined
Attribute Read/Write
Size: 8 bits per channel

Each channel has an 8-bit Low Page Register. The DMA memory Low Page Register contains bits[23:16] of the 27-bit address. The register works in conjunction with the DMA controller's High Page Register and Current Address Register to define the complete address (27 bits) for the DMA channel. This register is static throughout the DMA transfer. Following an autoinitialization, this register retains the original programmed value. Autoinitialize takes place only after a TC.

Bit	Description
7:0	**DMA Low Page Address Bits[23:16]:** These bits represent the eight second most significant address bits when forming the 27-bit address for a DMA transfer. Upon CPURST or Master Clear, the value of these bits are undefined.

3.4.1.10 DMHPG—DMA Memory High Page Register

I/O Address: DMA Channel 0—487h, DMA Channel 1—483h, DMA Channel 2—481h, DMA Channel 3—482h, DMA Channel 5—48Bh, DMA Channel 6—489h, DMA Channel 7—48Ah
Default Value: Undefined
Attribute Read/Write
Size: 8 bits per channel

Each channel has an 8-bit High Page Register. The DMA Memory High Page Register contains the three most significant bits of the 27-bit address. The register works in conjunction with the Current Address Register and Low Page Register to define the complete 27-bit address for the DMA channel. This register is static throughout the DMA transfer. Following an autoinitialization, this register retains the original programmed value. Autoinitialize occurs only after a TC.

Bit	Description
7:3	**Reserved:** Must be 0 when programming this register.
2:0	**DMA High Page [26:24]:** These bits represent the three most significant address bits when forming the 27-bit address for a DMA transfer. Following the programming of a channel's Current Address Register or Low Page Register, this register is initialized to 00h. Upon CPURST or Master Clear, the value of these bits are undefined.

3.4.1.11 DCLBP—DMA Clear Byte Pointer Register

I/O Address: Channels [3:0]—00Ch
Channels [7:4]—0D8h
Default Value: Undefined
Attribute: Write Only
Size: 8 bits

Writing to this register executes the Clear Byte Pointer Command. This command is executed prior to writing/reading new address or word count information to/from the DMA. This command initializes the byte pointer flip-flop to a known state so that subsequent byte accesses to the 16-bit register contents address upper and lower bytes in the correct sequence.

The clear byte pointer command clears the internal flip-flop used to address the upper or lower byte of the 16-bit Address and Word Count Registers. The latch is also cleared at power-on by CPURST and by the Master Clear Command. The Host CPU may read or write a 16-bit DMA controller register by performing two consecutive accesses to the I/O port. The Clear Byte Pointer Command precedes the first access. The first I/O write to the register address loads the least significant byte, and the second access automatically accesses the most significant byte.

Bit	Description
7:0	**Clear Byte Pointer:** No specific pattern. The command is invoked with a write to the I/O address.

3.4.1.12 DMCL—DMA Master Clear Register

I/O Address: Channel [3:0]—00Dh
Channel [7:4]—0DAh
Default Value: Undefined
Attribute: Write Only
Size: 8 bit

This software command has the same effect as the hardware reset. The Command, Status, Request, and Internal First/Last Flip-Flop registers are cleared and the Mask Register is set. The DMA controller enters the idle cycle.

Bit	Description
7:0	**Master Clear Command:** No specific pattern. This command is invoked with a write to the I/O address.

3.4.1.13 DCLM—DMA Clear Mask Register

I/O Address: Channel [3:0]—00Eh
Channel [7:4]—0DCh
Default Value: Undefined
Attribute: Write Only
Size: 8 bit

This command clears the mask bits of all four channels, enabling them to accept DMA requests. I/O port 0Eh is used for channels 0–3 and I/O port 0DCh is used for channels 4–7.

Bit	Description
7:0	**Clear Mask Register Command:** No specific pattern. This command is invoked with a write to the I/O port address.

3.4.2 TIMER/COUNTER REGISTER DESCRIPTION

There are three counters that are equivalent to those found in the 82C54 Programmable Interval Timer. The counters are controlled by timer/counter registers that can be accessed from either the CPU, PCI Bus, or ISA Bus.

3.4.2.1 TCW—Timer Control Word Register

I/O Address: 043h
Default Value: Undefined
Attribute: Write Only
Size: 8 bits

The Timer Control Word Register specifies the counter selection, the operating mode, the counter byte programming order and size of the count value, and whether the counter counts down in a 16-bit binary or binary-coded decimal (BCD) format. After writing the control word, a new count can be written at any time. The new value takes effect according to the programmed mode.

There are six programmable counting modes. Typically, Timer Counters 0 and 2 are programmed for Mode 3, the Square Wave Mode, while Counter 1 is programmed in Mode 2, the Rate Generator Mode.

Two latch commands are selected through the Timer Control Word Register. The Read Back Command is selected when bits[7:6] = 11 and the Counter Latch Command is selected when bits[5:4] = 00. When either of these two commands are selected, the meaning of the other bits in the register changes.

Following CPURST, the control words for each register are undefined and each timer must be programmed for the counters to be in a known state. Note however, that some counter/timer functions are set to known states following CPURST. Each counter OUT signal is set to 0 (and the Timer Counter 2 OUT status bit in the NMISC Register is 0). The SPKR output, interrupt controller input IRQ0 (internal), and the internally generated refresh request are each set to 0 following CPURST.

Bit	Description
7:6	**Counter Select:** The Counter Selection bits select the counter the control word acts upon or the Read Back Command as shown below. **Bits[7:6] — Counter Select** 00 — Counter 0 01 — Counter 1 10 — Counter 2 11 — Read Back Command
5:4	**Read/Write Select:** This field selects the count register read/write programming mode or the Counter Latch Command as shown below. The read/write programming selection chosen indicates the programming sequence that must follow when initializing the counter specified in bits[7:6]. If a counter is programmed to read/write two byte counts, note that a program must not transfer control between writing the first and second byte to another routine that also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count. The count must be completely loaded with both bytes. Note that the actual counter programming occurs by accessing I/O addresses 040h, 041h, and 042h for counters 0, 1, and 2, respectively. **Bits[5:4] — Read/Write Programming Select** 00 — Counter Latch Command 01 — R/W Least Significant Byte (LSB) 10 — R/W Most Significant Byte (MSB) 11 — R/W LSB, Then MSB
3:1	**Counter Mode Selection:** This field selects one of six possible modes of operation for the counter as shown below. **Bits[3:1] — Counter Mode** 000 — Out Signal On End of Count 001 — Hardware Re-triggerable one-shot X10 — Rate Generator (divide by n counter) X11 — Square Wave Output 100 — Software Triggered Strobe 101 — Hardware Triggered Strobe
0	**Binary/BCD Countdown Select:** When bit 0 = 0, a binary countdown is used. The largest possible binary count is 2^{16}. When bit 0 = 1, a binary-coded decimal (BCD) count is used. The largest BCD count allowed is 10^4.

Read Back Command

The Read Back Command provides the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. The Read Back Command is written to the Timer Control Word Register that latches the current states of the above mentioned variables. The value of the counter and its status may then be read by I/O access to the counter address.

Status and/or count may be latched on one, two, or all three of the counters by selecting the counter during the register write. The count latched remains latched until read, regardless of further latch commands. The count must be read before newer latch commands latch a new count. The status latched by the Read Back Command also remains latched until after a read of the Counter Access Ports Register. Thus, the status and count are unlatched only after a counter read of the Timer Status Byte Format Register, the Counter Access Ports Register, or the Timer Status Byte Register and Counter Access Ports Register in succession.

Both count and status of the selected counter(s) may be latched simultaneously by setting both bit 5 and bit 4 to 0. This is functionally the same as issuing two consecutive, separate Read Back Commands. As mentioned above, if multiple count and/or status Read Back Commands are issued to the same counter(s) without any intervening reads, all but the first are ignored.

If both count and status of a counter are latched, the first read operation from that counter returns the latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two byte counts) returns the latched count. Subsequent reads return an unlatched count.

Bit	Description
7:6	**Read Back Command:** When bits[7:6] = 11 during a write to the Timer Control Word Register, the Read Back Command is selected. As noted above, the normal meanings (mode, countdown, R/W select) of the bits in the control register at I/O address 043h change when the Read Back Command is selected. Following the Read Back Command, I/O reads from the selected counter's I/O addresses produce the current latch status, the current latched count, or both if bits[5:4] = 00.
5	**Latch Count of Selected Counters:** When bit 5 = 1, the count is not latched. When bit 5 = 0, the current count value of the selected counters is latched.
4	**Latch Status of Selected Counters:** When bit 4 = 1, the status is not latched. When bit 4 = 0, the status of the selected counters is latched. The status byte format is described in Section 3.4.2.2, Interval Timer Status Byte Format Register.
3	**Counter 2 Select:** When bit 3 = 1, Counter 2 is selected for the latch command selected with bits 4 and 5. When bit 3 = 0, status and/or count is not latched.
2	**Counter 1 Select:** When bit 2 = 1, Counter 1 is selected for the latch command selected with bits 4 and 5. When bit 2 = 0, status and/or count is not latched.
1	**Counter 0 Select:** When bit 1 = 1, Counter 0 is selected for the latch command selected with bits 4 and 5. When bit 1 = 0, status and/or count is not latched.
0	**Reserved:** Must be 0 when programming this register.

Counter Latch Command

The Counter Latch Command latches the current count value at the time the command is issued. This command is used to insure that the count read from the counter is accurate (particularly when reading a two-byte count). The count value is then read from each counter's count register (via the Counter Access Ports Register). One, two, or all three counters may be latched with one Counter Latch Command.

If a Counter is latched once and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read is the count at the time the first Counter Latch Command was issued.

The count must be read according to the programmed format. Specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads).

NOTES:

1. If a counter is programmed to read/write two byte counts, a program must not transfer control between reading the first and second byte to another routine that also reads from that same counter. Otherwise, an incorrect count will be read. Finish reading the latched two-byte count before transferring control to another routine.
2. The Timer Counter Register bit definitions are different during the Counter Latch Command than for a normal Timer Counter Register write.

Bit	Description
7:6	**Counter Selection:** This field selects the counter for latching by the Counter Latch Command as shown below. **Bits[7:6] — Counter Select** 00 — Counter 0 01 — Counter 1 10 — Counter 2 11 — Not Used; Do Not Write
5:4	**Counter Latch Command:** When bits[5:4] = 00 during a write to the Timer Control Word Register, the Counter Latch Command is selected. As noted above, the normal meanings (mode, countdown, R/W select) of the bits in the control register at I/O address 043h change when the Counter Latch Command is selected. Following the Counter Latch Command, I/O reads from the selected counter's I/O addresses produce the current latched count.
3:0	**Reserved:** Must be 0 when programming this register.

3.4.2.2 TMSTAT—Interval Timer Status Byte Format Register

I/O Address: Counter 0—040h
Counter 1—041h
Counter 2—042h
Default Value: Bits[6:0] = undefined, Bit 7 = 0
Attribute: Read Only
Size: 8 bits per counter

Each counter's status byte can be read following an Interval Timer Read Back Command. The Read Back Command is programmed through the Timer Control Word Register. If latch status is chosen (bit 4 = 0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register returns the status byte. The status byte returns the countdown type (either BCD or binary), the counter operational mode, the read/write selection status, the Null count (also referred to as the count register status), and the current state of the counter OUT pin.

Bit	Description
7	**Counter OUT Pin State:** When bit 7 = 1, the OUT pin of the counter is 1. When bit 7 = 0 (default) , the OUT pin of the counter is 0.
6	**Count Register Status:** Null Count (also referred to as the Count Status Register) indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode. However, until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before the load time, the count value returned does not reflect the new count written to the register. When bit 6 = 0, the count has been transferred from CR to CE and is available for reading. When bit 6 = 1, the Null count condition exists. The count has not been transferred from CR to CE and is not yet available for reading.
5:4	**Read/Write Selection Status:** Bits[5:4] reflect the read/write selection made through bits[5:4] of the Timer Control Word Register. The binary codes returned during the status read match the codes used to program the counter read/write selection. **Bits[5:4] — Read/Write Programming Select Status** 00 — Counter Latch Command 01 — R/W Least Significant Byte (LSB) 10 — R/W Most Significant Byte (MSB) 11 — R/W LSB, Then MSB
3:1	**Mode Selection Status:** Bits[3:1] return the counter mode programming made through bits[3:1] of the Timer Control Word Register. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. **Bits[3:1] — Counter Mode** 000 — Out Signal On End of Count 001 — Hardware Re-triggerable one-shot X10 — Rate Generator (divide by n counter) X11 — Square Wave Output 100 — Software Triggered Strobe 101 — Hardware Triggered Strobe
0	**Countdown Type Status:** Bit 0 reflects the current countdown type—either 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

3.4.2.3 CAPS—Counter Access Ports Register

I/O Address: Counter 0, System Timer—040h
Counter 1, Refresh Request—041h
Counter 2, Speaker Tone—042h
Default Value: Undefined
Attribute: Read/Write
Size: 8 bits per counter

These I/O addresses provide access for a) writing count values to the Count Registers, b) reading the current count value from the counter by either an I/O read, after a counter-latch command, or after a Read Back Command, and c) reading the status byte following a Read Back Command.

Bit	Description
7:0	**Counter Port Byte:** Each counter I/O address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined by the Timer Control Word Register. This register I/O address also reads the current count from the Count Register and returns the status of the counter programming following a Read Back Command.

3.4.3 INTERRUPT CONTROLLER REGISTER DESCRIPTION

The 82420EX PCIset contains an ISA-Compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The interrupt registers control the operation of the interrupt controller and can be accessed from the CPU or PCI Bus. In addition, some of the registers can be accessed from the ISA Bus.

3.4.3.1 ICW1—Initialization Command Word 1 Register

I/O Address: INT CNTRL-1—020h
INT CNTRL-2—0A0h
Default Value: Undefined
Attribute: Write Only
Size: 8 bits per controller

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence. Addresses 020h and 0A0h are referred to as the base addresses of CNTRL-1 and CNTRL-2, respectively. An I/O write to the CNTRL-1 or CNTRL-2 base address with bit 4 equal to 1 is interpreted as ICW1. For the 82420EX PCIset-based ISA systems, three I/O writes to "base address + 1" must follow the ICW1. The first write to "base address + 1" performs ICW2, the second write performs ICW3, and the third write performs ICW4. ICW1 starts the initialization sequence during which the following automatically occur:

1. The Interrupt Mask Register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.
5. If IC4 was set to 0, then all functions selected by ICW4 are set to 0. However, in the IB implementation, ICW4 must be programmed and IC4 must be set to a 1.

ICW1 has three significant functions in the IB interrupt controller configuration. ICW4 is needed, so bit 0 must be programmed to a 1. Since there are two interrupt controllers in the system, bit 1 (SNGL) must be programmed to a 0 on both CNTRL-1 and CNTRL-2, to indicate a cascade configuration. The IB provides separate registers (ELCR Registers) to program level or edge sensitive interrupt IRQ lines. Thus, bit 3 (LTIM in the 82C59) is not used. Bit 4 must be a 1 when programming ICW1. This bit indicates that ICW1, and not OCW2 or OCW3, will be programmed during the write to this port.

Bit	Description
7:5	**ICW/OCW Select:** Bits[7:5] are MCS-85 implementation specific bits. These bits are not used and should be 000 when programming the interrupt controller.
4	**ICW/OCW Select:** Bit 4 = 1 selects ICW1. OCW2 and OCW3 are also addressed at the same port as ICW1. A "1" on this bit at any time will force the interrupt controller to interpret the write as an ICW1. The controller will then expect to see ICW2, ICW3, and ICW4. After the fixed initialization sequence to ICW1, ICW2, ICW3, and ICW4, the controller base address is used to write to OCW2 and OCW3. Bit 4 is a "0" on writes to these registers.
3	**Edge/Level Bank Select (LTIM):** This bit is disabled. Its 82C59 Interrupt Controller function is replaced by the Edge/Level Triggered Control Registers (ELCR). The ELCR registers allow the interrupts to be programmed for edge or level mode on an interrupt by interrupt basis.
2	**ADI:** Bit 2 (ADI) is a MCS-85 implementation specific bit. This bit is not used and should be 0 when programming the IB.
1	**Single/Cascade Select (SNGL):** SNGL must be programmed to a 0 to indicate that two interrupt controllers are operating in cascade mode on the IB.
0	**ICW4 Write Required (ICW4):** This bit must be set to a 1. IC4 indicates that ICW4 needs to be programmed. The IB requires that ICW4 be programmed to indicate that the controllers are operating in an 80x86 type system.

3.4.3.2 ICW2—Initialization Command Word 2 Register

I/O Address: INT CNTRL-1—021h
INT CNTRL-2—0A1h
Default Value: Undefined
Attribute: Write Only
Size: 8 bits per controller

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the Host CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for CNTRL-1 and 70h for CNTRL-2.

Bit	Description
7:3	**Interrupt Vector Base Address:** Bits[7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input. For CNTRL-1, a typical value is 00001b, and for CNTRL-2, 01110b. The interrupt controller combines a binary code representing the interrupt level to receive service with this base address to form the interrupt vector that is driven onto the bus. For example, the complete interrupt vector for IRQ0 (CNTRL-1), would be 0000 1000b (CNTRL-1 [7:3] = 00001b and 000b representing IRQ0). This vector is used by the CPU to point to the address information that defines the start of the interrupt routine.
2:0	**Interrupt Request Level:** When writing ICW2, this field should be 000. During an interrupt acknowledge cycle, this field is programmed by the interrupt controller with the interrupt code representing the interrupt level to be serviced. This interrupt code is combined with bits[7:3] to form the complete interrupt vector driven onto the data bus during the second INTA# cycle. The 3-bit binary codes are: 000 represents IRQ0 (IRQ8), 001 IRQ1 (IRQ9), 010 IRQ2 (IRQ10), 011 IRQ3 (IRQ11), 100 IRQ4 (IRQ12), 101 IRQ5(IRQ13), 110 IRQ6(IRQ14), and 111 IRQ7 (IRQ15).

3.4.3.3 ICW3—Initialization Command Word 3 Register

I/O Address: INT CNTRL-1—021h
Default Value: Undefined
Attribute: Write Only
Size: 8 bits

The meaning of ICW3 differs between CNTRL-1 and CNTRL-2. On CNTRL-1, the master controller, ICW3 indicates which CNTRL-1 IRQ line physically connects the INTR output of CNTRL-2 to CNTRL-1. ICW3 must be programmed to 04h, indicating the cascade of the CNTRL-2 INTR output to the IRQ2 input of CNTRL-1.

An interrupt request on IRQ2 causes CNTRL-1 to enable CNTRL-2 to present the interrupt vector address during the second interrupt acknowledge cycle.

Bit	Description
7:3	**Not Used:** Must be 0.
2	**Cascaded Interrupt Controller IRQ Connection:** Bit 2 must always be programmed to a 1. This bit indicates that CNTRL-2, the slave controller, is cascaded on interrupt request line two (IRQ2). When an interrupt request is asserted to CNTRL-2, the IRQ goes through the priority resolver. After the slave controller priority resolution is finished, the INTR output of CNTRL-2 is asserted. However, this INTR assertion does not go directly to the CPU. Instead, the INTR assertion cascades into IRQ2 on CNTRL-1. IRQ2 must go through the priority resolution process on CNTRL-1. If it wins the priority resolution on CNTRL-1 and the CNTRL-1 INTR signal is asserted to the CPU, the returning interrupt acknowledge cycle is really destined for CNTRL-2. The interrupt was originally requested at CNTRL-2, so the interrupt acknowledge is destined for CNTRL-2, and not a response for IRQ2 on CNTRL-1. When an interrupt request from IRQ2 wins the priority arbitration, in reality an interrupt from CNTRL-2 has won the arbitration. Because bit 2 of ICW3 on the master is set to 1, the master knows which identification code to broadcast on the internal cascade lines, alerting the slave controller that it is responsible for driving the interrupt vector during the second INTA# pulse.
1:0	**Not Used:** Must be 0.

3.4.3.4 ICW3—Initialization Command Word 3 Register

I/O Address: INT CNTRL-2—0A1h
Default Value: Undefined
Attribute: Write Only
Size: 8 bits

On CNTRL-2 (the slave controller), ICW3 is the slave identification code broadcast by CNTRL-1 from the trailing edge of the first INTA# pulse to the trailing edge of the second INTA# pulse. CNTRL-2 compares the value programmed in ICW3 with the incoming identification code. The code is broadcast over three internal cascade lines. ICW3 must be programmed to 02h for CNTRL-2. When 010b is broadcast by CNTRL-1 during the INTA# sequence, CNTRL-2 assumes responsibility for broadcasting the interrupt vector during the second interrupt acknowledge cycle.

As an illustration, consider an interrupt request on IRQ2 of CNTRL-1. By definition, a request on IRQ2 must have been asserted by CNTRL-2. If IRQ2 wins the priority resolution on CNTRL-1, the interrupt acknowledge cycle returned by the CPU following the interrupt is destined for CNTRL-2, not CNTRL-1. CNTRL-1 will see the INTA# signal, and knowing that the actual destination is CNTRL-2, will broadcast a slave identification code across the internal cascade lines. CNTRL-2 compares this incoming value with the 010b stored in ICW3. Following a positive decode of the incoming message from CNTRL-1, CNTRL-2 drives the appropriate interrupt vector onto the data bus during the second interrupt acknowledge cycle.

Bit	Description
7:3	**Reserved:** Must be 0 when programming this register.
2:0	**Slave Identification Code:** The Slave Identification code must be programmed to 010b during the initialization sequence. The code stored in ICW3 is compared to the incoming slave identification code broadcast by the master controller during interrupt acknowledge cycles.

3.4.3.5 ICW4—Initialization Command Word 4 Register

I/O Address: INT CNTRL-1—021h
INT CNTRL-2—0A1h
Default Value: 01h
Attribute: Write Only
Size: 8 bits

Both interrupt controllers must have ICW4 programmed as part of their initialization sequence. Minimally, the microprocessor mode bit (bit 0) must be set to a 1 to indicate an Intel architecture-based platform. Failure to program this bit will result in improper controller operation during interrupt acknowledge cycles. Additionally, the Automatic End of Interrupt (AEOI) may be selected, as well as the Special Fully Nested Mode (SFNM) of operation.

Bit	Description
7:5	**Reserved:** Must be zero when programming this register.
4	**Special Fully Nested Mode (SFNM):** When bit 4 = 1, the special fully nested mode is enabled. When bit 4 = 0, the special fully nested mode is disabled (this is the normal mode).
3	**Buffered Mode (BUFM):** Must be 0 (non-buffered mode).
2	**Master/Slave in Buffered Mode:** Must be 0.
1	**Automatic End of Interrupt (AEO):** When bit 1 = 1, the automatic end of interrupt mode is selected. When bit 1 = 0, the normal end of interrupt is selected. This bit should normally be programmed to 0.
0	**Microprocessor Mode:** The Microprocessor Mode bit must be programmed to 1 to indicate that the interrupt controller is operating in an Intel Architecture-based system. Never program this bit to 0.

3.4.3.6 OCW1—Operational Control Word 1 Register

I/O Address: INT CNTRL-1—021h
INT CNTRL-2—0A1h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

OCW1 sets and clears the mask bits in the Interrupt Mask Register (IMR). Each interrupt request line may be selectively masked or unmasked any time after initialization. Note that masking IRQ2 on CNTRL-1 also masks all of controller 2's interrupt requests (IRQ[15:8]). Reading OCW1 returns the controller's mask status.

The IMR stores the bits that mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input does not affect the interrupt request lines of lower priority. Unlike status reads of the ISR and IRR, for reading the IMR, no OCW3 is needed. The output data bus contains the IMR when a read occurs to I/O address 021h or 0A1h (OCW1). All writes to OCW1 must occur following the ICW1-ICW4 initialization sequence, since the same I/O addresses are used for OCW1, ICW2, ICW3 and ICW4.

Bit	Description
7:0	**Interrupt Request Mask (Mask [7:0]):** When a 1 is written to any bit in this register, the corresponding IRQx line is masked. For example, if bit 4 = 1, IRQ4 is masked. Interrupt requests on IRQ4 will not set channel 4's interrupt request register (IRR) bit as long as the channel is masked. When a bit = 0 (default), the corresponding IRQx mask bit is cleared, and interrupt requests are accepted by the controller. Note that masking IRQ2 on CNTRL-1 also masks the interrupt requests from CNTRL-2, which is physically cascaded to IRQ2.

Bit	Interrupt	Bit	Interrupt
0	IRQ0	4	IRQ4
1	IRQ1	5	IRQ5
2	IRQ2	6	IRQ6
3	IRQ3	7	IRQ7

3.4.3.7 OCW2—Operational Control Word 2 Register

I/O Address: INT CNTRL-1—020h
INT CNTRL-2—0A0h
Default Value: Bit[4:0] = undefined, Bit[7:5] = 001
Attribute: Write Only
Size: 8 bits

OCW2 controls both the Rotate Mode and the End of Interrupt Mode, and combinations of the two. OCW2 also selects individual interrupt channels during three of the seven commands. The three low order bits (labeled L2, L1 and L0) are used when bit 6 is set to a 1 during the command. Following a CPURST or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7:5</td><td>Rotate and EOI Codes: These three bits control the Rotate and End of Interrupt modes and combinations of the two as shown below. Bit 7 = R(rotate), Bit 6 = SL, and Bit 5 = EOI.

<table>
<tr><th>Bits[7:5]</th><th>Rotate and EOI Modes</th><th>Bit[7:5]</th><th>Rotate and EOI Modes</th></tr>
<tr><td>001</td><td>Non-Specific EOI Command</td><td>000</td><td>Rotate in Auto EOI Mode (clear)</td></tr>
<tr><td>011</td><td>Specific EOI Command</td><td>111</td><td>Rotate on Specific EOI Command*</td></tr>
<tr><td>101</td><td>Rotate on Non-Specific EOI Command</td><td>110</td><td>Set Priority Command*</td></tr>
<tr><td>100</td><td>Rotate in Auto EOI Mode (set)</td><td>010</td><td>No Operation</td></tr>
</table>
NOTE:
*Interrupt Select Levels are used.</td></tr>
<tr><td>4:3</td><td>OCW2 Select: When selecting OCW2, bits 3 and 4 must both be 0. If bit 4 is a 1, the interrupt controller interprets the write to this port as an ICW1. Therefore, always ensure that these bits are both 0 when writing an OCW2.</td></tr>
<tr><td>2:0</td><td>Interrupt Level Select (L2, L1, L0): L2, L1, and L0 determine the interrupt level acted on when the SL bit is active. A simple binary code, outlined below, selects the channel for the command to act on. When the SL bit is inactive, these bits do not have a defined function. In this case, programming L2, L1 and L0 to 0 is sufficient.

<table>
<tr><th>Bits[2:0]</th><th>Interrupt Level</th><th>Bits[2:0]</th><th>Interrupt Level</th></tr>
<tr><td>000</td><td>IRQ0(8)</td><td>100</td><td>IRQ4(12)</td></tr>
<tr><td>001</td><td>IRQ1(9)</td><td>101</td><td>IRQ5(13)</td></tr>
<tr><td>010</td><td>IRQ2(10)</td><td>110</td><td>IRQ6(14)</td></tr>
<tr><td>011</td><td>IRQ3(11)</td><td>111</td><td>IRQ7(15)</td></tr>
</table></td></tr>
</table>

3.4.3.8 OCW3—Operational Control Word 3 Register

I/O Address: INT CNTRL-1—020h
INT CNTRL-2—0A0h
Default Value: Bit[6,0] = 0, Bit[7,4:2] = undefined, Bit[5,1] = 1
Attribute: Read/Write
Size: 8 bits

OCW3 serves three important functions—Enable Special Mask Mode, Poll Mode control, and IRR/ISR register read control. First, OCW3 is used to set or reset the Special Mask Mode (SMM). The Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/disabling of the other channel's mask bits.

Second, the Poll Mode is enabled when a write to OCW3 is issued with bit 2 equal to 1. The next I/O read to the interrupt controller is treated like an interrupt acknowledge—a binary code representing the highest priority level interrupt request is released onto the bus.

Third, OCW3 provides control for reading the In-Service Register (ISR) and the Interrupt Request Register (IRR). Either the ISR or IRR is selected for reading with a write to OCW3. Bits 0 and 1 carry the encoded command to select either register. The next I/O read to the OCW3 port address returns the register status specified during the previous write. The register specified for a status read is retained by the interrupt controller. Therefore, a write to OCW3 prior to every status read command is unnecessary, provided the status read desired is from the register selected with the last OCW3 write.

Bit	Description
7	**Reserved:** Must be zero when programming this register.
6	**Special Mask Mode (SMM):** If SMME = 1 and SMM = 1 the interrupt controller enters Special Mask Mode. If SMME = 1 and SMM = 0 (default), the interrupt controller is in normal mask mode. When SMME = 0, SMM has no effect.
5	**Special Mask Mode Enable (SMME):** When ESMM = 1 (default), the SMM bit is enabled to set or reset the Special Mask Mode. When ESMM = 0, the SMM bit becomes a "don't care".
4:3	**OCW3 Select:** When selecting OCW3, bit 3 must be a 1 and bit 4 must be 0. If bit 4 = 1, the interrupt controller interprets the write to this port as an ICW1. Therefore, always ensure that bits[4:3] = 01 when writing an OCW3.
2	**Poll Mode Command:** When bit 2 = 0, the Poll command is not issued. When bit 2 = 1, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	**Register Read Command:** Bits[1:0] provide control for reading the In-Service Register (ISR) and the Interrupt Request Register (IRR). When bit 1 = 0, bit 0 does not affect the register read selection. When bit 1 = 1, bit 0 selects the register status returned following an OCW3 read. If bit 0 = 0, the IRR is read. If bit 0 = 1, the ISR is read. Following ICW initialization, the default OCW3 I/O address read is "read IRR". To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read.

3.4.3.9 ELCR1—Edge/Level Triggered Register

I/O Address: INT CNTRL-1—4D0h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The ELCR1 Register selects either edge triggered or level sensitive operations for the IRQ[7:3] signals. In edge triggered mode, the interrupt is recognized by a low to high transition. In level sensitive mode, the interrupt is recognized by a low level. Note that IRQ0, IRQ1 and IRQ2 are not programmable and are always edge sensitive. The default for IRQ[7:3] is edge triggered.

Bit	Description
7:3	**Bit 7 - Bit 3: IRQ[7:3] ECL:** Bit 7 to bit 3 select edge trigger or level sensitive modes for IRQ[7:3], respectively. When a bit is 1, the corresponding IRQx is in the level sensitive mode and when a bit is 0, the corresponding IRQx is in the edge trigger mode.
2:0	**Reserved:** Must be 0 when programming this register.

3.4.3.10 ELCR2—Edge/Level Triggered Register

I/O Address: INT CNTRL-2—4D1h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The ELCR2 Register selects either edge triggered or level sensitive operations for the IRQ[15,14,12:9] signals. In edge triggered mode, the interrupt is recognized by a low to high transition. In level sensitive mode, the interrupt is recognized by a low level. Note that IRQ13 and IRQ8 are not programmable and are always edge sensitive. The default for IRQ[15,14,12:9] is edge triggered.

Bit	Description
7:6	**Bit 7 - Bit 6: IRQ[15,14] ECL:** Bit 7 and bit 6 select edge trigger or level sensitive modes for IRQ[15,14], respectively. When a bit is 1, the corresponding IRQx is in the level sensitive mode and when a bit is 0, the corresponding IRQx is in the edge trigger mode.
5	**Reserved:** Must be 0 when programming this register.
4:1	**Bit 4 - Bit 1: IRQ[12:9] ECL:** Bit 4 to bit 1 select edge trigger or level sensitive modes for IRQ[12:9], respectively. When a bit is 1, the corresponding IRQx is in the level sensitive mode and when a bit is 0, the corresponding IRQx is in the edge trigger mode.
0	**Reserved:** Must be zero when programming this register.

3.4.4 X-BUS REGISTER DESCRIPTION

There are two X-Bus registers described in this section—the Reset X-Bus IRQ[12,1] Register and the Coprocessor Error Register. These registers can be accessed from the CPU, PCI Bus, or ISA Bus.

3.4.4.1 RIRQ—Reset IRQ[12,1]

I/O Address: 60h
Default Value: NA
Attribute: Read only
Size: 8 bits

Address locations 60h and aliased address 62h are used to clear the mouse interrupt (IRQ12) and keyboard interrupt (IRQ1). When the mouse interrupt function is enabled (bit 4 in the X-Bus Chip Select Register is 1), the mouse interrupt function is provided on the IRQ12/M input signal. In this mode, a mouse interrupt generates an interrupt through IRQ12 to the Host CPU. A read of 60h releases IRQ12. If bit 4 = 0 in the X-Bus Chip Select Register, a read of 60h or 62h has no effect on IRQ12/M. Note, however, that a read of these addresses always clears the keyboard interrupt (IRQ1). Reads and writes to this register flow through to the ISA Bus.

Bit	Description
7:2	**Reset IRQ[12,1]:** No specific pattern. A read of address 60h executes the command.
1:0	**Reset IRQ[12,1]:** No specific pattern. A read of address 60h executes the command.

3.4.4.2 CPERR—Coprocessor Error Register

I/O Address: F0h
Default Value: NA
Attribute: Write only
Size: 8 bits

Writes to this address are monitored by the IB. Writing to address F0h causes the IB to drive IGNNE# low to the CPU (informing the CPU to ignore future coprocessor errors). The IB also negates IRQ13 (internal to the IB). Note, that IGNNE# is not asserted unless FERR# is active. Reads and writes to this register flow through to the ISA Bus.

Bit	Description
7:0	**Ignore Coprocessor Error Command:** No special pattern required: A write to address F0h executes the command.

3.4.5 NMI REGISTER DESCRIPTION

An NMI is an interrupt requiring immediate attention and has priority over the normal interrupt lines (IRQx). The IB indicates error conditions by generating a non-maskable interrupt. NMI interrupts (special cycles) are caused by the following conditions:

1. System errors on the PCI Bus. SERR# is driven low by a PCI resource when this error occurs.
2. Parity errors on the add-in memory boards on the ISA expansion bus. IOCHK# is driven low when this error occurs.
3. Main memory parity errors, through the SERR# signal.

There are two 8-bit registers that support NMI—The NMI Status and Control (NMISC) Register and the NMI Enable and Real Time Clock Address (NMIERTC) Register. These registers can be accessed from the CPU, PCI Bus, or ISA Bus. Note that masking the NMI signal for all sources via the NMIERCT Register does not affect the input NMI status conditions (i.e., bits 6 and 7 in the NMISC Register). This means that, if NMI is masked and then unmasked, an NMI will occur if an NMI had previously been detected. To ensure that all NMI requests are serviced, the NMI service routine software flow should be as follows:

1. NMI is detected by the CPU on the rising edge of the NMI input.
2. The CPU reads NMI status via the NMISC Register to determine the NMI source. Software may then set the status bits that caused the NMI to 0. Between the time the CPU reads the NMI sources and sets them to a 0, an NMI may have been generated by another source. In this case, the NMI signal remains asserted. If this happens, the new NMI source will not be recognized by the because there was no edge on NMI.
3. Software must then disable the NMI signals in the NMIERTC Register. This causes the NMI output to transition low then high if there are any pending NMI sources.

3.4.5.1 NMISC—NMI Status and Control Register

I/O Address: 061h
Default Value: 00U0 0000
Attribute: Read/Write
Size: 8 bits

This register provides status of various system components, speaker counter (Counter 2) output control, and gates the counter output that drives the SPKR signal.

Bit		Description
7	RO	**SERR# NMI Source Status:** System agents on the PCI Bus (PCI devices or main memory) assert the SERR# signal to report system errors. When the SERR# signal is asserted (and bit 2 of this register is 0), this bit is set to a 1. In addition, if bit 7 of the NMIERTC Register is 1, an NMI is generated. Software can clear this bit and the interrupt by setting bit 2 to 0 and then setting bit 2 to 1. This bit is read only. When writing to this register, bit 7 must be 0.
6	RO	**IOCHK# NMI Source Status:** Expansion boards on the ISA Bus assert IOCHK# to request high priority servicing (e.g., parity errors on memory cards). When the IOCHK# signal is asserted (and bit 3 of this register is 0), this bit is set to a 1. In addition, if bit 7 of the NMIERTC Register is 1, an NMI is generated. Software can clear this bit and the interrupt by setting bit 3 to 0 and then setting bit 3 to 1. This bit is read only. When writing to this register, bit 6 must be 0.
5	RO	**Timer Counter 2 OUT Status:** This bit reflects the current state of the Interval Timer Counter 2 OUT signal. Counter 2 must be programmed following a CPURST for this bit to have a determinate value. This bit is read only. When writing to this register, bit 5 must be 0.
4	RO	**Refresh Cycle Toggle:** The Refresh Cycle Toggle signal toggles from either 0 to 1 or 1 to 0 following every refresh cycle. This bit is read only. When writing to this register, bit 4 must be 0.
3	R/W	**IOCHK# NMI Enable:** When bit 3 = 1, IOCHK# NMI's are disabled and cleared, and bit 6 of this register is disabled (always reads 0). When bit 3 = 0 (default), bit 6 is enabled and, if bit 7 of the NMIERTC Register is 1, the IOCHK# NMI is enabled.
2	R/W	**PCI SERR# Enable:** When bit 2 = 1, SERR# NMI's are disabled and cleared, and bit 7 of this register is disabled (always reads 0). When bit 2 = 0 (default), bit 7 is enabled and, if bit 7 of the NMIERTC Register is 1, the SERR# NMI is enabled.
1	R/W	**Speaker Data Enable:** This bit enables/disables the SPKR output signal. When bit 1 = 1, the SPKR output signal is enabled and equivalent to the Counter 2 OUT signal. When bit 1 = 0 (default), the SPKR output is disabled and always 0.
0	R/W	**Timer Counter 2 Enable:** When bit 0 = 1, Timer Counter 2 counting is enabled. When bit 0 = 0 (default), Counter 2 counting is disabled.

3.4.5.2 NMIERTC—NMI Enable and Real Time Clock Address Register

I/O Address: 070h
Default Value: Bit[6:0] = undefined, Bit 7 = 1
Attribute: Write Only
Size: 8 bits

This register enables/disables all NMIs and provides a real time clock address pointer field to address memory locations. Do not modify the contents of this register without considering the effects on the state of the other bits. Reads and writes to this register address flow through to the ISA Bus.

Bit	Description
7	**NMI Enable (NMIE):** This bit provides a mask of the NMI output signal. When bit 7 = 1 (default), NMI is disabled for all sources and the NMI signal is negated. When bit 7 = 0, NMIs are enabled. Setting this bit to 1 does not clear or disable the NMI status conditions. Thus, if NMI is disabled then enabled via this register, an NMI will occur if one of the NMI status bits (6 or 7) is set in the NMISC Register.
6:0	**Real time Clock Address:** Used by the Real Time Clock on the Base I/O component to address memory locations.

3.4.6 POWER MANAGEMENT REGISTER DESCRIPTION

This section describes two power management registers—APMS and APMC Registers. These registers are located in normal I/O space and must be accessed (via the CPU or PCI Bus) with 8 bit accesses. Note that the rest of the power management registers are located in PCI configuration space (see Section 3.3, PCI Configuration Registers).

3.4.6.1 APMC—Advanced Power Management Control Port

I/O Address: 0B2h
Default Value: 00h
Attribute: Read/Write
Size: 8 Bits

This register passes data (APM Commands) between the OS and the SMI handler. In addition, writes can generate an SMI and reads can cause STPCLK# to be asserted. The IB operation is not affected by the data in this register.

Bit	Description
7:0	**APM Control Port (APMC):** Writes to this register store data in the APMC Register and reads return the last data written. In addition, writes generate an SMI, if bit 7 of the SMIEN Register and bit 0 of the SMICNTL Register are both is set to 1. Reads cause the STPCLK# signal to be asserted, if bit 1 of the SMICNTL Register is set to 1. Reads do not generate an SMI.

3.4.6.2 APMS—Advanced Power Management Status Port

I/O Address: 0B3h
Default Value: 00h
Attribute: Read/Write
Size: 8 Bits

This register passes status information between the OS and the SMI handler. The IB operation is not affected by the data in this register.

Bit	Description
7:0	**APM Status Port (APMS):** Writes store data in this register and reads return the last data written.

4.0 FUNCTIONAL DESCRIPTION

This section describes the 82420EX PCIset functions and hardware interfaces including the PCIset memory and I/O address map, system arbitration, DMA, interrupt controller, Timer/counter, power management, and clock/reset. The Clock/Reset section also covers the strapping options for the different hardware configuration modes and provides tables listing the state of each 82420EX PCIset output or bi-directional signal during a hard reset. The Host Bus, PCI Bus, ISA Bus, X-Bus, and the PSC/IB Link interfaces are described. The L2 cache and main memory DRAM interfaces and associated memory arrays are covered.

4.1 Memory and I/O Address Map

The 82420EX PCIset interfaces to three system Buses—CPU, PCI, and ISA Buses. The 82425EX PSC provides positive decode for certain I/O and memory space accesses on the CPU and PCI Buses. These decodes include accesses to the PCI Local Bus IDE (CPU only), main memory (CPU, ISA, and PCI), ISA-Compatible registers (CPU, ISA, and PCI), and the PSC's I/O Control Registers (CPU only). In addition, the PSC subtractively decodes certain CPU/PCI cycles.

The 82426EX IB provides positive decode for certain ISA I/O and memory space accesses. These decodes include accesses to the ISA-Compatible registers (for ISA master and DMA initiated cycles), main memory (for ISA and DMA initiated cycles), BIOS, X-Bus, and system events for SMM support. Note that DMA devices and ISA masters can not access the PCI or CPU Buses.

4.1.1 MEMORY ADDRESS MAP

The PSC positively decodes accesses to main memory space (128 MBytes maximum as programmed in the DRB Registers). Accesses in the following ranges are forwarded to the PCI Bus: TOM to 128 MBytes, (2 GByte minus 128 MByte) to (2 GByte plus 128 MByte), and 4 GByte to (4 GByte minus 128 MByte).

All other memory spaces are not intended for use.

NOTE:
The PSC does not decode host CPU address signals A[29:27].

All CPU/PCI accesses to the 0–640 KByte main memory region are forwarded to main memory (Table 10). Accesses to the video region (640–768 KBytes) are subtractively decoded to the ISA Bus. Accesses to the 768 KByte to 1 MByte region are controlled by attribute bits in the PAM Registers. Accesses to the region between 1 MByte and 128 MByte are either sent to main memory or subtractively decoded to either PCI or ISA.

Table 10. CPU/PCI 0 to 128 MByte Address Map

Memory Segment	Decode
16–128 MBytes	Positive decode(1,2)
Top of Hole to 16 MBytes	Positive decode(1,2)
Bottom of Hole to the Top of Hole	Subtractive decode
1 MByte to the Bottom of Hole	Positive decode(1,2)
768 KByte to 1 MByte	Positive decode or subtractively decoded to ISA(3)
640–768 KByte (Video)	Subtractively decoded to ISA
0–640 KByte	Positive decode(4)

NOTES:
1. As programmed in the DRAM Row Boundary Register.
2. For memory accesses that are > top of DRAM <16M, the PSC subtractively decodes and forwards to ISA.
3. The 82420EX allows 13 programmable memory and cacheability attributes on 13 memory segments of various sizes in the ISA compatiblity hole (768 KBytes to 1 MByte). Refer to the PAM Register description.
4. Always in DRAM.

All ISA master and DMA accesses to memory locations 0–640 KByte are forwarded to main memory. ISA memory accesses from 1 MByte to the top of memory are forwarded to main memory, except for accesses to the programmable memory hole. ISA accesses from 768 KByte to 1 MByte (except for E0000–EFFFFh, if forwarding is enabled) and accesses above the top of main memory are confined to the ISA Bus.

Table 11. DMA and ISA Master Accesses to Main Memory

Memory Space	Response
Top of main memory to 128 MByte	Confine to ISA
1 MByte to top of main memory	Forward to main memory(1)
768 KBytes to 1 MByte	Confine to ISA(2)
640–768 KByte (video)	Confine to ISA
0–640 KByte	Forward to main memory

NOTES:
1. Except accesses to programmed memory hole.
2. If bit 6 is 0 in the XBCSA Register and bit 6 is 1 in the PIRQ0 Register, accesses to E0000–EFFFFh are forwarded to main memory.

The 82420EX supports one hole in main memory, as defined by the MEMHOLE Register. CPU accesses in the memory hole are forwarded to the PCI Bus and, if not claimed, forwarded to the ISA Bus. PCI master accesses in the memory hole are subtractively decoded to ISA, if necessary. ISA master accesses are confined to the ISA Bus.

4.1.2 BIOS MEMORY SPACE

The 82420EX PCIset supports 512 KBytes of BIOS space. This includes the normal 128 KByte space plus an additional 384 KByte BIOS space (known as the enlarged BIOS area). All BIOS regions that are not shadowed in main memory are subtractively decoded.

The 128 KByte BIOS memory space is located at 000E0000–000FFFFFh (top of 1 MByte), and is aliased at FFFE0000–FFFFFFFFh (top of 4 GByte). This 128 KByte block is split into two 64 KByte blocks. CPU/PCI accesses to the top 64 KByte region (000F0000–000FFFFFh) that are not claimed by main memory or PCI, are forwarded to ISA. The subsequent ISA cycle always generates a BIOS chip select (asserts BIOSCS#).

CPU/PCI accesses to the bottom 64 KByte region (000E0000–000EFFFFh) that are not claimed by main memory or PCI are forwarded to ISA. The subsequent ISA cycle generates a BIOS chip select, if lower BIOS is enabled (via the XBCSA Register).

The additional 384 KByte region resides at FFF80000–FFFDFFFFh. When enabled (via the XBCSA Register), CPU/PCI memory accesses to this region are subtractively decoded to the ISA Bus and BIOS chip select is generated.

All ISA BIOS accesses within the F0000–FFFFFh region are confined to the ISA Bus, even if BIOS is shadowed in main memory. Accesses to the E0000–EFFFFh region are confined to the ISA Bus, when this BIOS region is enabled (via the XBCSA Register). When the region is disabled, accesses are forwarded to main memory, if forwarding is enabled (via the PREV Register). Note that bit 6 in the XBCSA Register overrides bit 4 in the PREV Register.

4.1.3 VIDEO FRAME BUFFER

The Video Frame Buffer can be mapped in the following ranges:

1. In the standard VGA range.
2. In a defined memory hole. In this case, DRAM size is limited to 128 MByte Memory minus the hole size. For example, if there is a 2 MByte Frame Buffer hole, somewhere between 1 MByte and 16 MByte, then the maximum DRAM size allowed is 128 MByte minus 2 MByte equal 126 MByte.
3. Above Top of Memory, but under 128 MByte. In this case, maximum DRAM size is limited to 128 MByte minus the Frame Buffer Size.
4. Above 128 MByte. There are three non-aliased ranges above 128 MByte, which can be used for Frame Buffer:

   (2 GByte minus 128 MByte) to 2 GByte — When HA[31:27] = 01111

   2 GByte to (2 GByte plus 128 MByte) — When HA[31:27] = 10000

   (4 GByte minus 128 MByte) to (4 GByte minus .5 MByte) — When HA[31:27] = 11111

4.1.4 I/O ACCESSES

The PSC positively decodes access to the I/O control registers, PCI configuration registers, and ISA-Compatible Registers. For details concerning accessing these registers, see Section 3.0, Register Description. In addition, the PSC positively decodes CPU I/O accesses to the IDE ports, when enabled. For IDE port accesses, see Section 4.5, PCI Local Bus IDE.

4.1.5 SMRAM: PROTECTED SMM MEMORY BLOCK

The 82420EX PCIset supports a dedicated 64 KBytes of SMM memory, called SMRAM. The SMRAM is accessible only when certain conditions are met. In normal operations, the SMRAM is hidden. SMRAM can be located at the A0000–F0000h segment. The SMRAM can be enabled/disabled and programmed via the SMRAM Control Register.

When SMRAM is hidden, the whole memory space can be accessed, excluding the SMRAM block. When the SMRAM is visible, most of the memory space is visible, in addition to the SMRAM block. Only the memory block that shares the same bus address ranges with SMRAM cannot be accessed in this case.

SMRAM is visible under the following conditions:

- The CPU is in SMM, performing a memory cycle in the SMRAM range, while the SMRAM is not manually closed. This is indicated by SMIACT# = 0, HLDA = 0, HA is in the SMRAM range (as programmed by SMBASE field of the SMRAMCON Register), and SMCLS = 0. The SMCLS bit only affects data cycles and is ignored for code read cycles.

- The CPU is not in SMM, performing a memory cycle in the SMRAM range, while the SMRAM is manually opened. This is indicated by SMIACT# = 1, HLDA = 0, HA is in the SMRAM range, and the SMOPN = 1.
- On each CPU access when SMIACT# is asserted (or SMOPN = 1), the main memory address is compared to the selected SMM memory address as determined by the SMBASE field. These bits allow the user to select from eight different 64 KByte main memory locations used for SMM memory.

4.2 PSC/IB Link Interface

The PSC and IB communicate using the PSC/IB interface. Interface communications include CPU/PCI accesses of the IB internal registers, CPU/PCI cycles forwarded to the ISA Bus, and ISA master or DMA accesses to main memory. The PSC/IB Link interface is a point-to-point communication connection between the PSC and the IB.

Four sideband signals synchronize data flow and bus ownership—Link Request (LREQ#), Link Grant (LGNT#), Command Valid (CMDV#), and Slave Idle (SIDLE#). LREQ# and LGNT# are used by the IB to arbitrate for link mastership. Only the IB drives LREQ# while only the PSC drives LGNT#. CMDV# is driven by the current link master, while SIDLE# is driven by the current link slave. Commands, addresses, and data are transferred between the PSC and IB using the host address bus signals (A[17:2]).

4.3 Host CPU Interface

The 82420EX PCIset provides a host interface to all of the Intel486 family of processors and upgrades.

4.3.1 HOST BUS SLAVE DEVICE

The PCIset can be configured (via the HOST Device Control Register) to support an Intel486 Host Bus Slave device (specifically, a graphics device). Two special signals (HDEV# and HRDY#) as defined by the VL Bus specification are used in the interface to the Host Bus slave. The PSC can be configured to monitor HDEV# for all memory and I/O ranges that are not positively decoded by the PSC. The PSC can be configured to monitor HRDY# and return RDY# to the CPU, based on HRDY#. The host device may include an I/O range, memory range or both I/O and memory ranges. In all cases, these ranges must not be programmed (positively decoded) by the PSC. The host device's memory ranges are non-cacheable.

NOTES:

1. DMA, ISA Masters and PCI masters cannot access the Host Bus device.
2. The PSC does not contain a time-out mechanism to recover a cycle when HDEV# is asserted but HRDY# is not asserted. When the Host Bus device asserts HDEV#, it is assumed that the HRDY# assertion will follow.
3. Host Bus Device—Read and Write fastest timing. During a CPU read (fastest timing programmed), the Host Bus device must not start driving the data bus until two Host Bus clocks after the active ADS# period. This is required so the L2 cache can drive the data bus for a 0 wait-state L2 read. During a CPU write, the Host Bus device can respond with HRDY# in the cycle following ADS#, to achieve a 0 wait-state write cycle.
4. If the Host bus slave device is implemented on the motherboard, the graphics controller and video DAC chip must be accessed through the host bus. The graphics ROM must also be accessed through the host bus or integrated into system BIOS. If the graphics ROM is not integrated into system BIOS, and the graphics ROM is shadowed into DRAM, the host device must not respond with HDEV# when the graphics ROM area is accessed. If the graphics ROM is not shadowed, the PSC PAM registers must be programmed not to respond to the graphics ROM area.
5. If the host bus slave device is implemented using a connector, the graphics controller and video DAC chip must be accessed through the host bus. The graphics ROM can be accessed through the ISA bus. However, when accessing the ROM BIOS, the card in the connector must latch the address with ADS#.
6. Not all host bus slave devices use all of the host address lines for decode. If this is the case, note that PCI memory and system memory is limited by the number of address lines used by the host bus device for decode (e.g. if [25:2] are only used by the host device, usable system memory is limited to 64 MByte, as the host device will alias anything above 64 MByte).

4.3.2 L1 CACHE SUPPORT

The 82420EX PCIset provides signals that support the CPU's L1 cache. For the S-Series CPUs, the signals are the PCD, KEN#, and EADS# signals. For the D-Series and P24T CPUs, the signals are the KEN#, EADS#, CACHE#, and HITM#. The P24T and the D-Series CPUs include certain signals that are not connected to the PCIset. These signals are fixed to 1 or 0, depending on the system configuration as discussed in Table 12.

4.3.3 SOFT AND HARD RESETS

The 82420EX PCIset generates soft reset (SRESET) and hard resets (PCIRST#, RSTDRV, and CPURST).

Soft Reset

SRESET/INIT is generated under the following conditions:

1. Programming the TRC Register (see TRC Register Description).
2. Keyboard KBDRST#: This signal from the keyboard controller is used to generate a soft reset to the CPU via the PSC's SRESET/INIT signal.
3. Shutdown special cycle: When the CPU executes a shutdown special cycle, SRESET is generated.

Hard Reset

The IB generates a hard reset under two conditions:

1. PWROK; When PWROK is driven low, the IB asserts PCIRST#, RSTDRV, and CPURST. These hard reset signals remain asserted until 2 HCLKIN cycles after the rising edge of PWROK.
2. Programming the TRC Register (see TRC Register description).

Reset Distribution

Figure 4 and Figure 5 show how the hard and soft resets are distributed in the system. The specific implementation depends on the CPU type as shown in the figures.

To ensure that SMI# is not generated during SRESET, an external "OR" gate must be used as shown in Figure 6.

Table 12. L1 Cache Signals Not Connected to the PSC

Signal	Description
INV	INV input is tied to 1 for P24T and D-Series processor configuration. When INV = 1, the cache line is invalidated as a result of snoop-hit cycle.
HIT	The CPU asserts HIT to indicate that an Inquire cycle hits a line. The PSC only needs to know when the L1 cache line needs to perform write-back, as a result of Inquire cycle. Since the need to perform write backs is indicated by HITM#, the HIT is not needed in the PSC.
FLUSH#	The PSC does not support L1 hardware flush. Since SMRAM must be configured in a non-cacheable region, there is no need for automatic FLUSH# in a 82420 PCIset-based system. Therefore, FLUSH# can be tied to 1. The PSC recognizes the FLUSH special cycles and responds with RDY# to allow external logic to activate FLUSH# (if desired).
BLEN#	BLEN# is tied to 0 for P24T and D-Series configurations to enable bursted write-back cycles.
WB/WT#	WB/WT# is tied to 1 for P24T and D-Series configurations to set all cache lines in write-back mode. Individual lines can be configured in write-through mode by software only.
EWBE#	P24T External Write Buffer Empty input is used to enforce correct cycle ordering in concurrent systems. In 82420 PCIset-based systems, there is only a single active master at a time. Thus, the PSC does not use the EWBE# signal.
PWT	PWT is used as an indication to cache a line in a write-through mode. The PSC L2 Cache update mode can not be set on a line by line basis and thus PWT is not used.

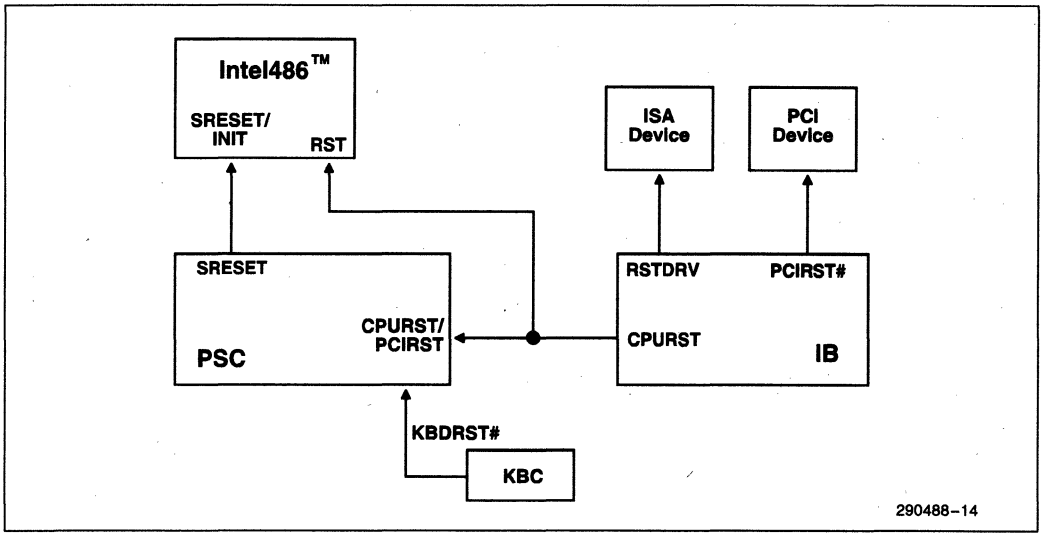


Figure 4. Reset Distribution for CPU's with Hard Reset and Soft Reset Inputs

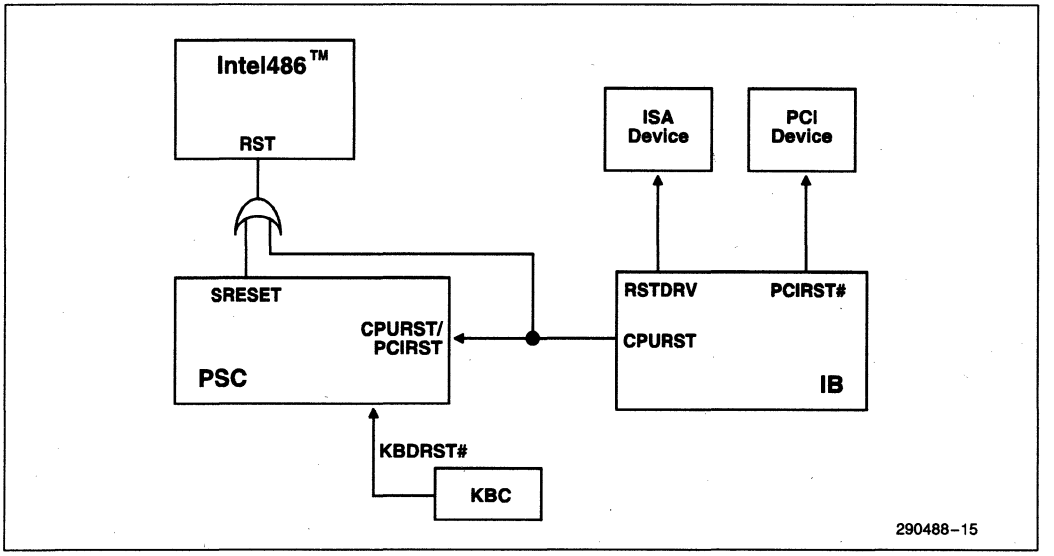


Figure 5. Reset Distribution for CPU's with One Reset Input

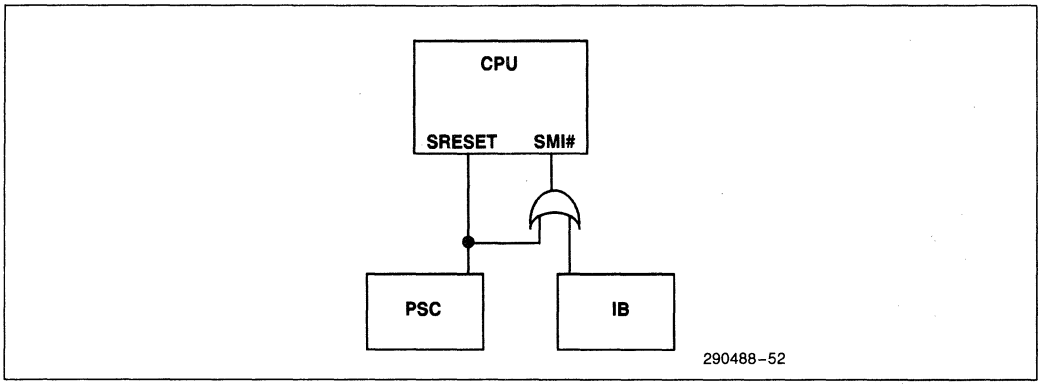


Figure 6. SMI# Gated with SRESET

4.3.4 KEYBOARD CONTROLLER (A20)

The 82420EX supports the generation of A20M# via the keyboard controller. To support the generation of A20M#, external logic may be required (Figure 7), depending on system requirements. "OR" gates 1 and 2 ensure that A20M# is negated during a SRESET or CPURST, respectively. "OR" gate 2 is not required if the KBC firmware forces KBCA20M# high during a hard reset. "OR" gate 3 and the inverter ensure that A20M# is negated when SMIACT# is asserted. "OR" gate 3 and the inverter are not required if the SMRAM is located under 1 MByte or at an even 1 MByte boundary and the SMRAM code does not need to go above the 1 MByte range while in SMM mode.

4.4 PCI Interface

The PSC has a standard master/slave PCI Bus interface. As a PCI device, the PSC can be either a master initiating a PCI Bus operation or a target responding to a PCI Bus operation. The PSC is a PCI Bus master for Host-to-PCI accesses and a target for PCI-to-Main memory accesses (or accesses that are forwarded to the ISA Bus). The Host can read or write configuration spaces, PCI memory space, and PCI I/O space.

NOTES:

1. PCI-to-Host accesses are not permitted. However, PCI-to-Main memory cycles that require the L1/L2 caches to be snooped, do invoke Host Bus cycles.
2. ISA-to-PCI accesses are not permitted.

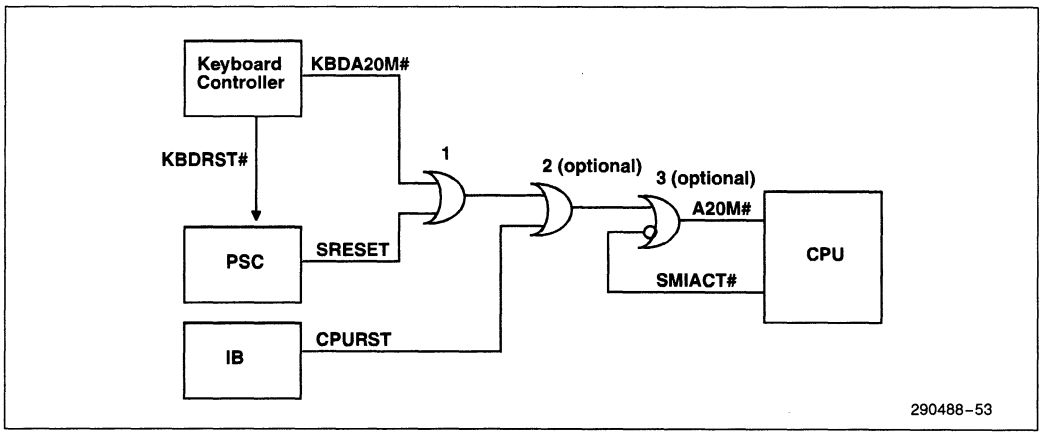


Figure 7. System Connection for Keyboard A20M# Generation

4.4.1 PCI BUS CYCLES SUPPORT

When the host initiates a bus cycle to a PCI device, the PSC becomes a PCI Bus master and translates the CPU cycle into the appropriate PCI Bus cycle. Post buffers permit the CPU to complete Host-to-PCI writes in zero wait-states.

When a PCI Bus master initiates a main memory access, the PSC becomes the target of the PCI Bus cycle and responds to the read/write access. As a PCI master, the PSC generates address parity for read and write cycles, and data parity for write cycles. As a target, the PSC generates data parity for read cycles. During PCI-to-Main memory accesses, the PSC automatically performs cache snoop operations on the Host Bus, if needed, to maintain data consistency.

PCI Bus commands indicate to the target the type of transaction desired by the master. These commands are presented on the C/BE[3:0]# signals during the address phase of a transfer. Table 13 summarizes The PSC's support of the PCI Bus commands.

PSC Supports Other PCI Bridges

The PCI Bus specification supports bridges that connect the system's local PCI Bus with other remote busses (PCI or others). The PSC supports the ability to connect bus bridges onto the local PCI Bus.

One type of PCI bridge interfaces the local PCI Bus to a set of slave (only) devices. In this case, the bridge performs protocol translation and may include write buffers (pointing away from the local PCI). An example of such a bridge is the PCI-to-PCMCIA bridge device (PPEC).

A second type of PCI bridge interfaces the local PCI Bus with another bus that supports masters and slaves—a remote PCI Bus. This type of bridge can generally include write buffers (and pre-fetchers) that are pointing in both directions (to local PCI Bus and away from local PCI Bus).

Table 13. Supported PCI Bus Commands

C/BE[3:0]#	Command Type	Supported As Target	Supported As Master
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	—	—
0101	Reserved	—	—
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	—	—
1001	Reserved	—	—
1010	Configuration Read	No	Yes
1011	Configuration Write	No	Yes
1100	Memory Read Multiple	Yes(1)	No
1101	Dual Address Cycle	No	No
1110	Memory Read Line	Yes(1)	No
1111	Memory Write and Invalidate	Yes(2)	No

NOTES:
1. As a target, the PSC treats this command as a memory read command.
2. As a target, the PSC treats this command as a memory write command.

The PSC supports PCI-to-PCI bridges, with the following restrictions:

- The 82420EX PCIset does not allow more than a single active master in the entire system. This restriction prevents a remote PCI Bus master from performing an exclusive access that is claimed by the bridge (the target is on the local PCI Bus), while there is another active master in the system (that may be performing another exclusive access on the local PCI Bus).
- When a master is granted, it is guaranteed that the PSC's PCI write buffers are empty. Since the PSC does not know the status of other bridges's buffers (that point to the PCI) while it grants the CPU, the other bridge's buffers must be disabled.

4.4.2 HOST TO PCI CYCLES

Host bus accesses to PCI Bus are always in the Host Bus address range, as defined by A[31:30,26:2] and the four BE lines. The PCI address lines are driven during the address phase. AD[29:27] lines are driven to the value of A[30], during Host accesses to PCI.

The PSC has the ability to burst up to 32 back-to-back CPU memory writes on the PCI Bus. This function is controlled by the PCICON Register. The PSC is capable of merging 8/16-bit graphic write cycles to the same dword address into the same posted write buffer location (controlled by the PCICON Register). The merged data is then driven as a single dword cycle on the PCI Bus. Byte merging is performed in the compatible VGA range only.

4.4.3 PCI CYCLE TERMINATIONS

The PSC performs a master abort, received target abort, signaled target abort, and a disconnect (as either a master or slave) as described in this section.

Master Abort—PSC as a Master

The PSC performs two types of master abort when a PCI cycle is not claimed by PCI Bus devices.

Master-Abort of Type 1 is performed by the PSC for the following conditions:

- When the memory address is lower than 16 MBytes.
- When the memory address is higher than 16 MBytes, but it is an enabled BIOS range.
- When the I/O address is lower than 64 KBytes.

Type 1 master abort actions:

- Master abort is performed.
- The cycle is forwarded to the ISA Bus.

Master abort of Type 2 is performed by the PSC for the following conditions:

- When the memory address is higher than 16 Mbytes, and it is not an enabled BIOS range.
- I/O address is above 64 KBytes.
- When a configuration access to a PCI device is not claimed.

Type 2 master abort actions:

- Master abort is performed.
- Master abort status bit (DS Register) is set.
- For reads, data of all 1's is returned to the CPU.
- For writes, RDY# is activated to complete the CPU cycle.

Received Target Abort—PSC as a Master:

When a PSC driven cycle is target aborted, the PSC sets the Received Target Abort status bit to 1 (in the DS Register). In addition, when SERR# is enabled, this signal is asserted for a single PCICLK. RDY# is asserted to complete the CPU cycle.

NOTE:
When the CPU attempts an access configuration registers and the function number is not 000, data of all 1's is returned (if it is a read cycle) and Target Abort Status bit is set.

Disconnect—PSC as a Master

When the PSC, as a PCI master, generates a burst memory write, it can be disconnected by the PCI target. The PSC will retry the disconnected cycle before any arbitration changes can be performed, since the PSC write buffers must be emptied and the on-going CPU access must be completed before an arbitration transfer can take place.

Disconnect—PSC as a Target

The PSC, as a PCI target, performs a disconnect when burst PCI master accesses are destined to the ISA Bus. The disconnect is performed at the completion of the first data phase. In addition, for burst PCI master cycles to main memory, the PSC performs a disconnect at the completion of the last data phase in a line boundary.

4.4.4 EXCLUSIVE CYCLES

The PSC, as a PCI master, never performs LOCKed cycles. The CPU does not return active HLDA while it is performing a LOCKed sequence. Also, the CPU is the only active master, as long as HLDA is inactive. Thus, the PSC does not need to drive LOCK to guarantee the CPU atomic LOCK sequence. Note that the 82420EX PCIset supports a bus locking mechanism (i.e., when a PCI master performs locked accesses, the arbitration is not changed, until the locked sequence is completed).

4.4.5 Parity Support

As a master, the PSC generates address parity for read and write cycles, and data parity for write cycles. As a slave, the PSC generates data parity for read cycles. Even parity is generated using the PAR line in the PCICLK following the PCI address or data phase.

The PSC does not check parity or generate SERR#, based on the PCI parity. The PSC only generates SERR# (if enabled via the PCICOM Register), when a main memory read results in a parity error. When a main memory parity error is detected, the PSC activates SERR#, if enabled, for a single PCICLK.

When a main memory parity error is detected and SERR# generation is enabled, the DPE bit in the DS Register is set to 1. When SERR# is activated, the SERRS bit in the DS Register is set to 1.

4.5 PCI Local Bus Ide

The PSC has a full-function PCI Local Bus IDE Controller capable of generating high speed PCI Local Bus IDE cycles. The PCI IDE address, control, and data signals are multiplexed with the PCI AD signals (Figure 8). They are buffered by external TTL devices to drive the IDE connector. Only CPU accesses to IDE can use the PCI local bus path. PCI masters and ISA masters can not access the drive connected to the PCI Local Bus.

The PSC's IDE interface supports one IDE connector (two drives). An additional IDE connector could be connected to the ISA or PCI Bus. The PCI IDE interface can be programmed at either the primary address (1F0h–1F7h, 3F6h, 3F7h) or secondary address (170h–177h, 376h, 377h) locations.

The selected IDE's data port, as well as the control/status ports, are accessed through the PCI Local Bus path. The PSC provides data steering to route data between the IDE data bus and the correct Host Bus byte lane. However, the PSC does not support multiple assembly/disassembly cycles for data size mismatches. Data size matching is guaranteed by the IDE device driver. The PSC assumes that all data port accesses (1F0h, 170h) are 16 bits wide. If an 8-bit IDE drive is accessed, the PSC still drives 16 bits onto the PCI AD signals for data port writes to IDE, and drive HD(15:0) for data port reads. Accesses to the PCI Local Bus control and status ports are assumed to be 8-bit accesses and the PSC steers the data to the appropriate byte lane. Table 14 shows the I/O addresses for the various IDE data, control, and status ports:

The PSC controls the timing of the high speed accesses to the PCI IDE connector and provides programmable timing fields (via the LBIDE Register). This allows the PCI local bus IDE timing to be programmed to cover 25 MHz and 33 MHz PCI frequencies, and IDE Modes 1, 2, and 3. The programmable timing also allows additional flexibility in the event that still faster IDE modes are defined in the future. Note that, the faster timing applies to data port accesses only. Accesses to all other ports, except the data port, run with compatible timings.

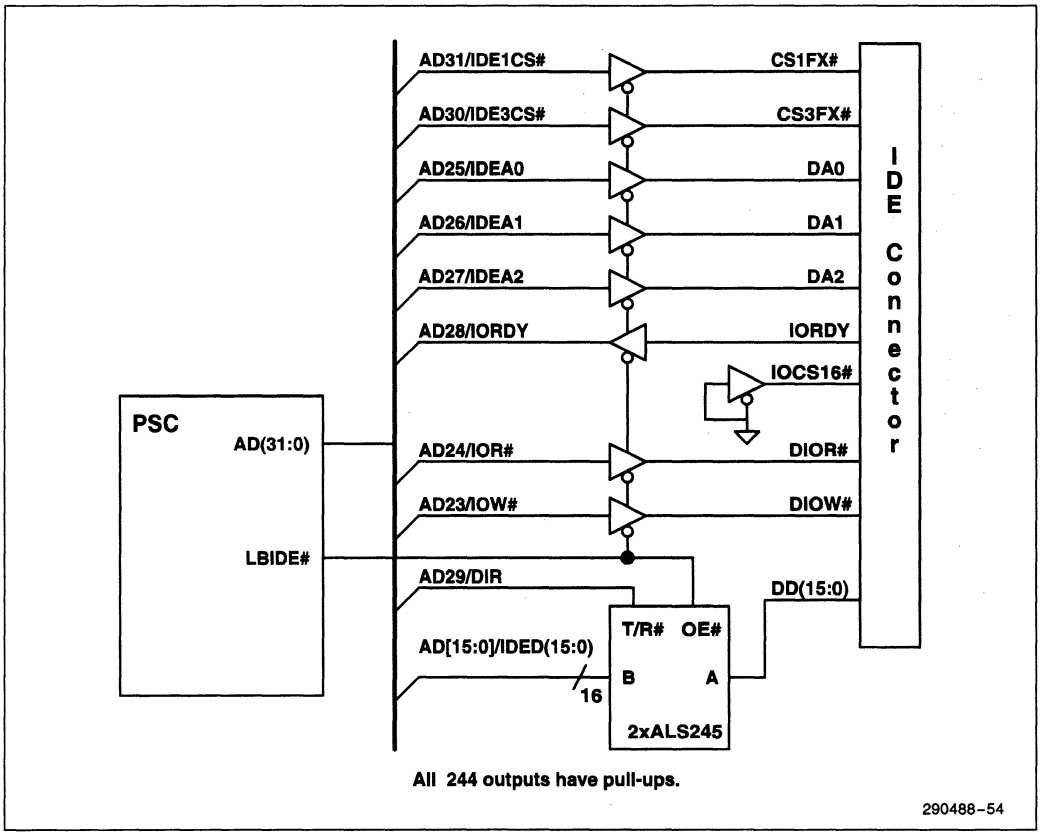


Figure 8. PSC PCI Local Bus IDE Connection

The PSC supports one connector that can be assigned at the primary or secondary address. This one connector can support two drives. The drive is selected through the Drive, Head port at I/O address 1x6h. The CPU writes bit 4 to a 0 to select drive 0, and writes bit 4 to a 1 to select drive 1. The PSC snoops writes to the enabled 1x6h (1F6h for primary, 176h for secondary) and keeps its own copy of bit 4 of I/O 1x6h. The fast timing bank can be programmed to apply to data port accesses to either drive 0, drive 1, or both. Accesses to the non-selected drive run with compatible timings.

Typically in a PC, when reading from port 3x7h, bits[6:0] are provided by the IDE drive and bit 7 is provided by the floppy disk controller as a reflection of the DSKCHG from the floppy disk drive. This occurs for both the primary and secondary locations. The PSC handles CPU I/O reads to port 3x7h in a unique fashion. For example, when the primary address range is enabled, the PSC splits the read to 3F7h and generates both a PSC/IB link interface bus cycle as well as a PCI Local Bus IDE cycle. The PSC takes bit 7 from the link cycle, merges it with bits[6:0] from the PCI local bus IDE cycle, and returns the complete 8 bits to the CPU. If the primary address range is not enabled, only the PSC/IB link interface bus cycle is generated. The same operation applies to 377h reads, when the secondary address range is enabled. This feature permits the PCI Local Bus IDE to be used in a system where, for example, the AIP is placed on an add-in card.

Table 14. IDE I/O Addresses

I/O Address	Port Function (R/W)
1x0h	Data
1x1h	Error/Features
1x2h	Sector Count
1x3h	Sector Number
1x4h	Cylinder Low
1x5h	Cylinder High
1x6h	Drive, Head
1x7h	Status/Command
3x6h	Alternate Status/Device Control
3x7h	Drive Address

NOTE:
x = F for Primary and 7 for Secondary

4.6 ISA Interface

The IB incorporates a fully ISA Bus compatible master and slave interface. The IB directly drives five ISA slots without external data or address buffers. The ISA interface also provides byte swap logic, I/O recovery support, wait-state generation, and SYSCLK generation. The ISA interface supports the following cycle types:

- CPU or PCI master initiated I/O and memory cycles to the ISA Bus.
- DMA compatible cycles between main memory and ISA I/O and between ISA I/O and ISA memory.
- ISA refresh cycles initiated by either the IB or an external ISA master.
- ISA master-initiated memory cycles to main memory and ISA master-initiated I/O cycles to the internal IB registers.

NOTES:

1. The IB does not grant the ISA Bus to an ISA master before gaining ownership of the system (i.e. Host and PCI Buses).
2. All cycles forwarded to main memory run as 16-bit extended cycles (i.e. IOCHRDY is negated until the cycle completes). Because the ISA Bus size is different from the main memory bus size, the data steering logic inside the IB steers the data to the correct byte lanes.

I/O Recovery Support

The I/O recovery mechanism in the IB is used to add additional recovery delay between the CPU or PCI master initiated 8-bit and 16-bit I/O cycles to the ISA Bus. The IB automatically forces a minimum delay of 3.5 SYSCLKs between back-to-back 8- and 16-bit I/O cycles to the ISA Bus. This delay is measured from the rising edge of the I/O command (IOR# or IOW#) to the falling edge of the next I/O command. If a delay of greater than 3.5 SYSCLKs is required, the ISA I/O Recovery Timer Register can be programmed to increase the delay in increments of SYSCLKs. No additional delay is inserted for back-to-back I/O sub-cycles generated as a result of byte assembly or disassembly.

SYSCLK Generation

The IB generates the ISA system clock (SYSCLK). SYSCLK is a divided down version of HCLKOUT and has a frequency of either 8.00 or 8.33 MHz, depending on the HCLKOUT frequency. The clock divisor value is determined by strapping options as discussed in the Clock section.

For CPU or PCI initiated cycles to the ISA Bus, SYSCLK is stretched to synchronize BALE falling to the rising edge of SYSCLK. During CPU or PCI initiated cycles to the IB, BALE is normally driven high, synchronized to the rising edge of SYSCLK and then driven low to initiate the cycle on the ISA Bus. However, if the cycle is aborted, BALE remains high and is not driven low until the next cycle to the ISA Bus.

Data Byte Swapping (ISA Master or DMA to ISA Device)

The data swap logic is integrated in the IB. For slaves that reside on the ISA Bus, data swapping is performed if the slave (I/O or memory) and ISA Bus master (or DMA) sizes differ and the upper (odd) byte of data is being accessed. The data swapping direction is determined by the cycle type (read or write). Table 15 shows when data swapping is provided during DMA and ISA master cycles to ISA slaves.

Table 15. DMA Data Swap

DMA I/O Device Size	ISA Memory Slave Size	Swap	Comments (I/O) ⟷ Memory
8-bit	8-bit	No	SD[7:0] ⟷ SD[7:0]
8-bit	16-bit	No	SD[7:0] ⟷ SD[7:0]
8-bit	16-bit	Yes	SD[7:0] ⟷ SD[15:8]
16-bit	8-bit	No	Not Supported
16-bit	16-bit	No	SD[15:0] ⟷ SD[15:0]

Table 16. 16-bit Master to 8-bit Slave Data Swap

SBHE#	SA0	SD[15:8]	SD[7:0]	Comments
0	0	Odd	Even	Word Transfer (data swapping not required)
0	1	Odd	Odd	Byte Swap(1, 2)
1	0	—	Even	Byte Transfer (data swapping not required)
1	1	—	—	Not Allowed

NOTES:
1. For ISA master read cycles, the IB swaps the data from the lower byte to the upper byte.
2. For ISA master write cycles, the IB swaps the data from the upper byte to the lower byte.

Wait-State Generation

The IB adds wait-states to the following cycles, if IOCHRDY is sampled negated (low). Wait-states are added as long as IOCHRDY remains low.

- During Refresh and IB master cycles (not including DMA) to the ISA Bus.
- During DMA compatible transfers between ISA I/O and ISA memory only.

For ISA master cycles targeted for the IB's internal registers or main memory, the IB always extends the cycle by driving IOCHRDY low until the transaction is complete.

Cycle Shortening

The IB shortens the following cycles, if ZEROWS# is sampled asserted (low).

- During IB master cycles (not including DMA) to 8-bit and 16-bit ISA memory.
- During IB master cycles (not including DMA) to 8-bit ISA I/O only.

For ISA master cycles targeted for the IB's internal registers or main memory, the IB does not assert ZEROWS#. If IOCHRDY and ZEROWS# are sampled low at the same time, IOCHRDY will take precedence and wait-states will be added.

4.7 X-Bus

The 82420EX PCIset provides the decode (chip selects) and X-Bus buffer control (XBUSOE# and XBUSTR#) for a Real Time Clock, Keyboard Controller, and BIOS (Figure 9). The chip selects are generated combinatorially from the ISA SA[16:0] and LA[23:17] address bus. (Note that the ISA master must drive SA[19:16] and LA[23:17] low when accessing I/O space.) The IB also provides PS/2 mouse support via the IRQ12/M signal and coprocessor functions (FERR# and IGNNE#). The chip selects and X-Bus buffer control lines can be enabled/disabled via the XBCSA Configuration Register.

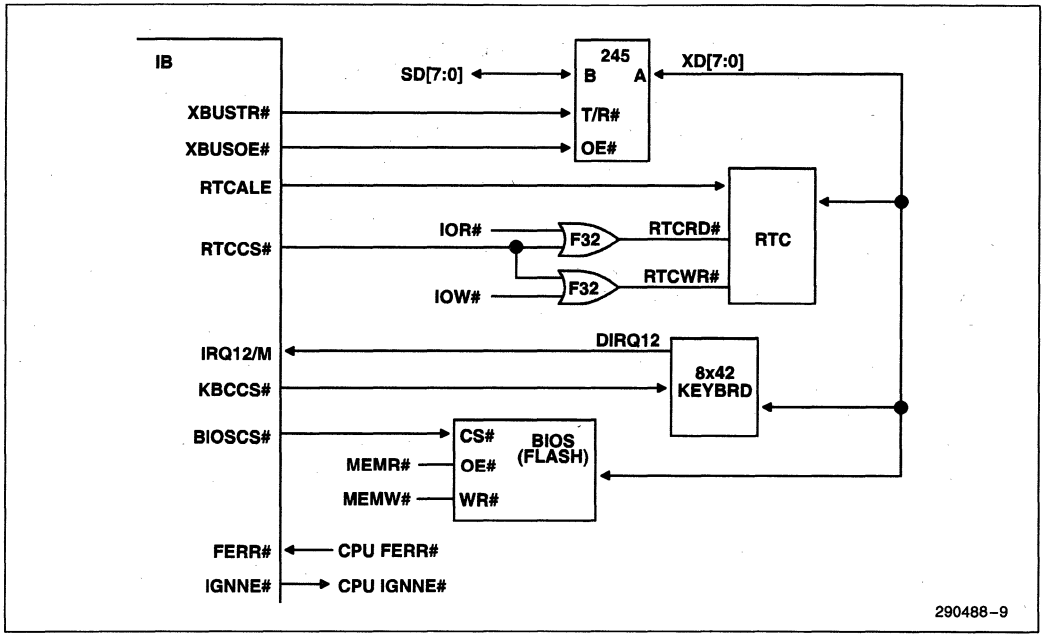


Figure 9. X-Bus Support

4.7.1 COPROCESSOR ERROR FUNCTION

The IB provides coprocessor error support for the CPU (enabled/disabled via the XBCSA Register). FERR# is tied directly to the coprocessor error signal of the CPU. If FERR# is asserted, an internal IRQ13 is generated and the INTR signal is asserted. When a write to I/O location F0h is detected, the IB negates IRQ13 (internal to the IB) and asserts IGNNE#. IGNNE# remains asserted until FERR# is negated. Note, that IGNNE# is not asserted unless FERR# is asserted.

4.7.2 MOUSE FUNCTION

The IB provides a mouse interrupt function (enabled/disabled via the XBCSA Register) on the IRQ12/M input signal. In this mode, a mouse interrupt generates an interrupt through IRQ12 to the Host CPU. The IB informs the CPU of this interrupt via a INTR. A read of 60h or 62h releases IRQ12. If bit 4 = 0 in the XBCSA Register, a read of address 60h or 62h has no effect on IRQ12/M. Reads and writes to this register flow through to the ISA Bus. For additional information, see the IRQ12/M description in the Signal Description.

4.8 System Arbitration

The 82420EX PCIset provides bus arbitration on the Host Bus, PCI Bus, and the PCI/IB Interface (to the ISA Bus). A device that is the master on any bus is the master of the entire system. (i.e., concurrency of more than one active master is not supported).

Signals associated with the system arbitration are the HOLD/HLDA signals (CPU Bus), PREQ[1:0]/PGNT[1:0]# signals (PCI Bus), and the LREQ#/LGNT# signals (PSC/IB Link Interface).

4.8.1 SYSTEM ARBITRATION SCHEME

When there are no active requests, the CPU owns the system. The system arbitration rotates between the PCI Bus, CPU Bus, and Link Interface Bus (on behalf of DMA and ISA Master devices), with the CPU permitted access every other transition.

NOTES:

1. The PSC, as a PCI master, never performs locked cycles. However, locked cycles are supported for PCI masters. When a PCI master performs a locked access, the arbitration is not changed until the locked sequence is completed.
2. After PGNT[1:0]# is asserted by the PSC, it is negated when FRAME# is sampled active (regardless the state of PREQ[1:0]#). The PCI master is expected to continue its current cycle (with potential multiple data phases), and then get-off the PCI Bus. The PSC does not release HOLD until the PCI Bus is idle. When a PCI master is re-tried by the PCI target, PGNT[1:0]# is already negated. Thus, the PCI master must get-off the bus. Since the PSC always gives the bus back to the CPU and the arbitration is rotated, PREQ[1:0]# can remain active as long as the PCI master has cycles to perform.
3. The PSC precludes fast back-to-back PCI master transactions. In addition, the PSC, as a PCI master, does not support fast back-to-back transactions.
4. When the PSC, as a PCI master, is re-tried, target-aborted or master-aborted, by a PCI target, the arbitration mechanism does not assert PGNT[1:0]# or LGNT#.

4.9 DMA Controller

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels (Channels [3:0] and Channels [7:5]). The DMA supports 8/16-bit device size using ISA-compatible timings and 27-bit addressing as an extension of the ISA-compatible specification. The DMA channels can be programmed for either fixed (default) or rotating priority. The DMA controller also generates ISA refresh cycles. DMA Channel 4 is used to cascade the two controllers and default to cascade mode in the DMA Channel Mode (DCM) Register (Figure 10). In addition to accepting requests from DMA slaves, the DMA controller also responds to requests that are initiated by software. Software may initiate a DMA service request by setting any bit in the DMA Channel Request Register to a 1. The DMA controller for Channels [3:0] is referred to as "DMA-1" and the controller for Channels [7:4] is referred to as "DMA-2".

Each DMA channel is hardwired to the compatible settings for DMA device sizechannels [3:0] are hardwired to 8-bit, count-by-bytes transfers and channels [7:5] are hardwired to 16-bit, count-by-words (address shifted) transfers. The IB provides the timing control and data size translation necessary for the DMA transfer between the memory (ISA or main memory) and the ISA Bus I/O. ISA-Compatible DMA timing is supported. The DMA controller also features refresh address generation and auto-initialization following a DMA termination.

Note that a DMA device (I/O device) is always on the ISA Bus, but the memory referenced is located on either an ISA Bus device or in main memory. When the IB is running a DMA cycle, it drives the MEMR# or MEMW# strobes, if the address is less than 16 MBytes (000000–FFFFFFh). The IB always generates ISA-Compatible DMA memory cycles. The SMEMR# and SMEMW# are generated if the address is less than 1 MByte (0000000–00FFFFFh). To avoid aliasing problems when the address is greater than 16 MBytes (1000000–7FFFFFFh), the MEMR# or MEMW# strobe is not generated.

The channels can be programmed for any of four transfer modessingle, block, demand, or cascade. Each of the three active transfer modes (single, block, and demand), can perform three different types of transfers (read, write, or verify). Note that memory-to-memory transfers are not supported by the IB. The DMA supports fixed and rotating channel priorities.

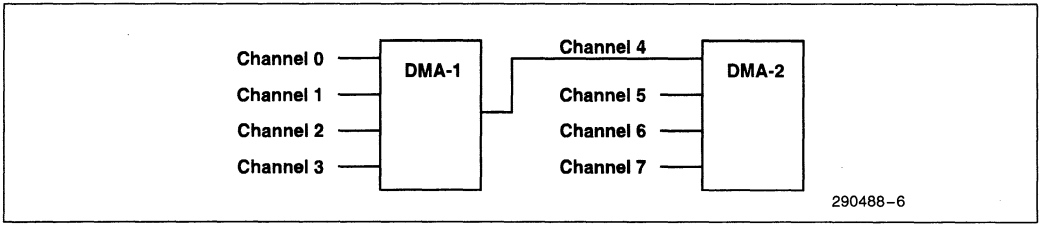


Figure 10. Internal DMA Controller

4.10 Interval Timer

The 82420EX PCIset contains three counters that are equivalent to those found in the 82C54 programmable interval timer. Each counter output provides a key system function. Counter 0 is connected to interrupt controller IRQ0 and provides a system timer interrupt for a time-of-day, diskette time-out, or other system timing functions. Counter 1 generates a refresh request signal and Counter 2 generates the tone for the speaker.

Counter 0 (System Timer)

This counter functions as the system timer by controlling the state of IRQ0 and is typically programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then re-loads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, re-loads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

Counter 1 (Refresh Request Signal)

This counter provides the refresh request signal and is typically programmed for Mode 2 operation. The counter negates refresh request for one counter period (838 ns) during each count cycle. The initial count value is loaded one counter period after being written to the counter I/O address. The counter initially asserts refresh request, and negates it for 1 counter period when the count value reaches 1. The counter then asserts refresh request and continues counting from the initial count value.

Counter 2 (Speaker Tone)

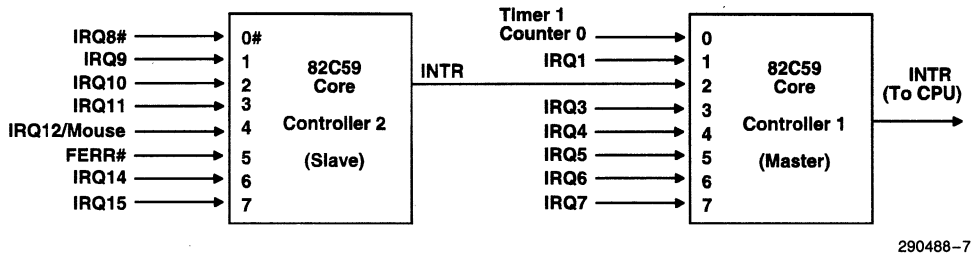
This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to I/O address 061h.

4.11 Interrupt Controller

The 82420EX PCIset contains an ISA-compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The two controllers (CNTRL-1and CNTRL-2) are cascaded allowing thirteen external and three internal interrupts (Figure 11). CNTRL-1 and CNTRL-2 are initialized separately and can be programmed to operate in different modes. CNTRL-1 is connected as the master interrupt controller and CNTRL-2 is connected as the slave interrupt controller. The three internal interrupts are used for internal functions only and are not available to the user. IRQ2 cascades the two controllers. IRQ0 provides a system timer interrupt and is tied to the Interval Timer, Counter 0. IRQ13 is connected internally to FERR# for coprocessor error support. The remaining thirteen interrupt lines (IRQ[15,14,12:9,8#,7:3,1]) are available for external system interrupts. Edge or level sense selection is programmable on an individual channel by channel basis. Interrupt steering permits two programmable interrupts (PIRQ0# and PIRQ1#) to be internally routed (steered) to one of eleven interrupts (IRQ[15,14,12:9,7:3]).

NOTES:

1. The standard external IRQ12 signal function or internally generated IRQ12/Mouse function are selected via the XBCSA Register.
2. The IB translates the CPU generated interrupt acknowledge cycle internally into the two INTA# pulses expected by the interrupt controller system.



NOTE:
IRQ0, IRQ2, and IRQ13 are internally connected and do not appear externally.

Figure 11. Block Diagram of the Interrupt Controller

4.11.1 PROGRAMMING THE INTERRUPT CONTROLLER

The Interrupt Controller accepts two types of command words generated by the CPU or bus master—Initialization Command Word (ICWx) and Operation Command Word (OCWx).

Initialization Command Words (ICWs)

Before normal operation can begin, each interrupt controller in the system must be initialized. In the 82C59, this is a two to four byte sequence. However, for the 82420EX PCIset, each controller must be initialized with a four byte sequence. This four byte sequence is required to configure the interrupt controller correctly for the IB implementation. This implementation is ISA compatible.

The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4. These command registers are discussed in Section 3.0, Register Description. The sequence must be executed for CNTRL-1 and CNTRL-2. ICW1, ICW2, ICW3, and ICW4 must be written in order. Any divergence from this sequence, such as an attempt to program an OCW, will result in improper initialization of the interrupt controller and unexpected, erratic system behavior. It is suggested that CNTRL-2 be initialized first, followed by CNTRL-1.

Operation Command Words (OCWs):

These are the command words which dynamically reprogram the Interrupt Controller to operate in various interrupt modes. OCW1 masks interrupt lines. OCW2 controls rotation in interrupt rotation priority mode and the End of Interrupt (EOI). OCW3 sets up reads of the ISR and IRR, enables/disables the Special Mask Mode (SMM), and sets up the polled interrupt mode. The OCWs can be invoked any time after initialization.

4.11.2 EDGE AND LEVEL INTERRUPT TRIGGERED MODE

In ISA systems, this mode is programmed using bit 3 in ICW1. For the IB, this bit is disabled and the Edge/Level Control Registers (ELCR1 and ELCR2) are included that select edge and level triggered mode per interrupt input. The default programming is equivalent to programming the LTIM bit (ICW1 bit 3) to a 0 (all interrupts selected for edge triggered mode). Note, that IRQ[13,8#,2,1,0] can not be programmed for level sensitive mode.

In both the edge and level triggered modes, the IRQx input must remain active until after the falling edge of the first INTA#. If IRQx is negated before this time, a default IRQ7 occurs when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IRQ inputs. To implement this feature, the IRQ7 routine is used for "clean up" by simply executing a return instruction, thus ignoring the interrupt. If IRQ7 is needed for other purposes, a default IRQ7 can still be detected by reading the ISR. A normal IRQ7 interrupt sets the corresponding ISR bit; a default IRQ7 does not set this bit. If a default IRQ7 routine occurs during a normal IRQ7 routine, however, the ISR remains set. In this case, it is necessary to keep track of whether or not the IRQ7 routine was previously entered. If another IRQ7 occurs, it is a default.

4.11.3 INTERRUPT STEERING

The IB contains two programmable interrupts (PIRQ0 and PIRQ1#) that can be internally routed to one of eleven interrupts (IRQ[15,14,12:9,7:3]) by programming the PIRQx Route Control Registers. One or both PIRQx# lines can be routed to the same IRQx input or interrupt steering can be disabled.

The PIRQx# lines are defined as active low, level sensitive to allow multiple interrupts on a PCI board to share a single line across the connector. When a PIRQx# is routed to a specified IRQ line, the software must change the IRQ's corresponding ELCR bit to level sensitive mode. Note, that this means that the selected IRQ can no longer be used by an ISA device, unless that ISA device can respond as an active low level sensitive interrupt.

4.12 L2 Cache

The L2 cache memory array contains a cache data RAM with a selectable storage capacity of either 64, 128, 256, or 512 KBytes. The cache data RAM is a direct-mapped memory array, write-through or write-back, that can be organized in either an interleaved or non-interleaved configuration. In addition to the cache data RAM, the L2 cache contains a RAM array that holds the tag address and a dirty bit that is associated with each line of data. Table 17 provides a summary of the L2 cache. A valid bit is not used in this architecture. The L2 cache is programmed via the SCC Register.

Table 17. L2 Cache Features

Feature	Description
Organization	Direct mapped
Capacity	64, 128, 256, or 512 KByte
Data Banks	1 or 2, depending on capacity
Line Size	16 bytes
Tag Size	8 bits
Cacheable Main Memory	8 MBytes to 128 MBytes
Allocation Policy	Allocate on CPU reads; no allocate on writes
Cache Policy	Non-cacheable, write-through (WT), and write-back (WB)

4.12.1 L2 CACHE SIZES/PERFORMANCE

The PSC allows four cache sizes. Table 18 shows the tag and data SRAMs used for various user settings. The PSC supports 15 ns tag SRAMs and 20 ns data SRAMs for the L2 cache at all frequencies. Table 19 shows the range of L2 performance achievable.

Table 18. L2 Options and Component List

Cache Size	Data RAMS	Tag Bits/Cacheable Main Memory	Tag Store
64 KByte	8 8K x 8	A[23:16]/16 MB	4K x 9
128 KByte	4 32K x 8	A[24:17]/32 MB	8K x 9
256 KByte	8 32K x 8	A[25:18]/64 MB	32K x 9
512 KByte	4 128K x 8	A[26:19]/128 MB	32K x 9

Table 19. Performance

Cycle Type	Tag Speed	Data Speed	25 MHz	33 MHz	L1
Interleaved Read	15 ns	15 ns/20 ns	2-1-1-1	2-1-1-1	WT/WB
Non-Interleaved Read	15 ns	15 ns	2-1-1-1	2-2-2-2(1)	WT/WB
Non-Interleaved Read	15 ns	20 ns	2-1-1-1	2-2-2-2	WT/WB
Interleaved Write	15 ns	15 ns/20 ns	2-1-1-1(2)	2-1-1-1(2)	WT/WB
Interleaved Write	15 ns	15 ns/20 ns	2-1-1-1(2)	2-1-1-1(2)	WT
Non-Interleaved Write	15 ns	15 ns/20 ns	3-2-2-2	3-2-2-2	WB

NOTES:
1. 2-1-1-1 may be used only with minimum margin design (light Host Bus loading) and 12 ns Data SRAMs.
2. Programmable option and applies to cache hit dirty write cycles.

4.12.2 CACHE OPERATIONS

During a CPU memory read or write operation, the PSC searches the cache first. Then, if required, it searches main memory for addressed data locations. The L2 cache operation is determined by the cache policy (non-cacheable, write-through, or write-back) as determined by the Secondary Cache Control Register (see Section 3.0, Register Description). If the caching policy is non-cacheable, the cache is not accessed.

Write-through and write-back are two caching policies for updating main memory with data in the cache. For these policies, the cache operation is determined by the type of operation as follows:

CPU Write Cycle

If the caching policy is write-through and there is a cache hit, both the cache and main memory are updated. If there is a cache miss, only main memory is updated. The cache is not updated (no write-allocate).

If the caching policy is write-back and there is a cache hit, only the cache is updated; main memory is not affected. If there is a cache miss, only main memory is updated. The cache is not updated (no write-allocate).

CPU Read Cycle

If there is a cache hit, the cache operation is the same for both write-through and write-back. In this case, data is transferred from the cache to the CPU. Main memory is not accessed.

If there is a cache miss, the line containing the requested data is transferred from main memory to the cache. During the cache line update, a line fill (burst read) memory operation containing four dword transfers occurs on the Host Bus to bring in the new line. This occurs for both write-through and write-back. However, in the case of write-back, if the cache line fill is to a dirty line (D=1), the dirty line is first written back to main memory before the new line is brought into the cache. For a dirty line write-back operation, the PSC first performs a read from the dirty cache line and writes the data to main memory. Then, the PSC updates the cache (both L1 and L2 simultaneously) with the new line.

4.12.3 CACHE CONSISTENCY

The Snoop mechanism in the PSC ensures data consistency between cache (both L1 and L2 caches) and main memory. Note that, for write-back cache control, the term "Inquire" is sometimes used to describe the snooping operation. In this document, the term "Snoop" is used for both write-through and write-back cache policies.

The PSC monitors PCI master, ISA master and DMA accesses to main memory and when needed, initiates an inquire (snoop) cycle to the L1 and L2 caches. The snoop mechanism guarantees that consistent data is always delivered to the host CPU, PCI master, ISA master or DMA.

4.12.4 INITIALIZING THE L2 CACHE

The 82420EX PCIset L2 cache architecture does not use a valid bit. Instead, BIOS initializes the L2 cache with valid data. After initialization, the cache controller maintains data coherency between the cache and main memory by keeping all cache lines valid. The PSC cache controller has two special bits to support initialization—Force Hit (SCC Register bit 6) and Force Miss Clean (SCC Register bit 5).

BIOS can use the Force Hit bit to determine the size of the L2 cache. When Force Hit is enabled, BIOS can attempt to alias cache locations on writes. For example, to check a 128 KByte cache size, BIOS writes location "x" with value 00h. BIOS can then write location 128k + x with 11h. With Force Hit enabled and the cache in write-back mode, the write does not access main memory. When a value of 00h is read from location "x", the L2 cache is greater than 128 KBytes. If 11h is read, the L2 cache is smaller than 128 KBytes. This process is repeated for all cache boundaries.

The Force Miss Clean bit causes all accesses to the L2 cache to be treated as a clean miss. This allows BIOS to initialize the L2. At start-up BIOS enables Force Miss Clean and reads a block of memory equal to the cache size. This initializes the L2 cache with data that is coherent with main memory.

4.12.5 CACHE LINE DESCRIPTION

Each line consists of four dwords of data, a tag field and a Dirty (D) bit. The tag field and control bits are read/written by the PSC during normal cache operations and are not accessible by software.

D: Dirty

The Dirty bit is set to 1 by the PSC to indicate that data modified in the cache line has not been written back to main memory.

Tag: Real Address Tag

The PSC uses the Tag field for cache line hit/miss determination. The width of the Tag field is fixed at 8 bits. The table below shows the real address bits that are stored in the Tag field as a function of the cache sizes.

Cache Size	8-Bit Tag
64 KBytes	A[23:16]
128 KBytes	A[24:17]
256 KBytes	A[25:18]
512 KBytes	A[26:19]

Doubleword[3:0]

Each line of the cache data RAM contains four dwords.

4.12.6 L2 CACHE STRUCTURE

The tag is 8 bits plus a dirty bit. Either interleaved or non-interleaved organizations are permitted. The PSC will assert the COE[1:0]# and CWE[1:0]# signals to both banks, even when programmed for non-interleaved mode. The interleaved L2 can provide zero wait-state reads and writes. Figure 12 shows the interconnection between the PSC and an interleaved L2. The PSC has a variety of programmable access timings to support 25 MHz, 33 MHz, and 50 MHz. These options are controlled by the Secondary Cache Control Register (SCC).

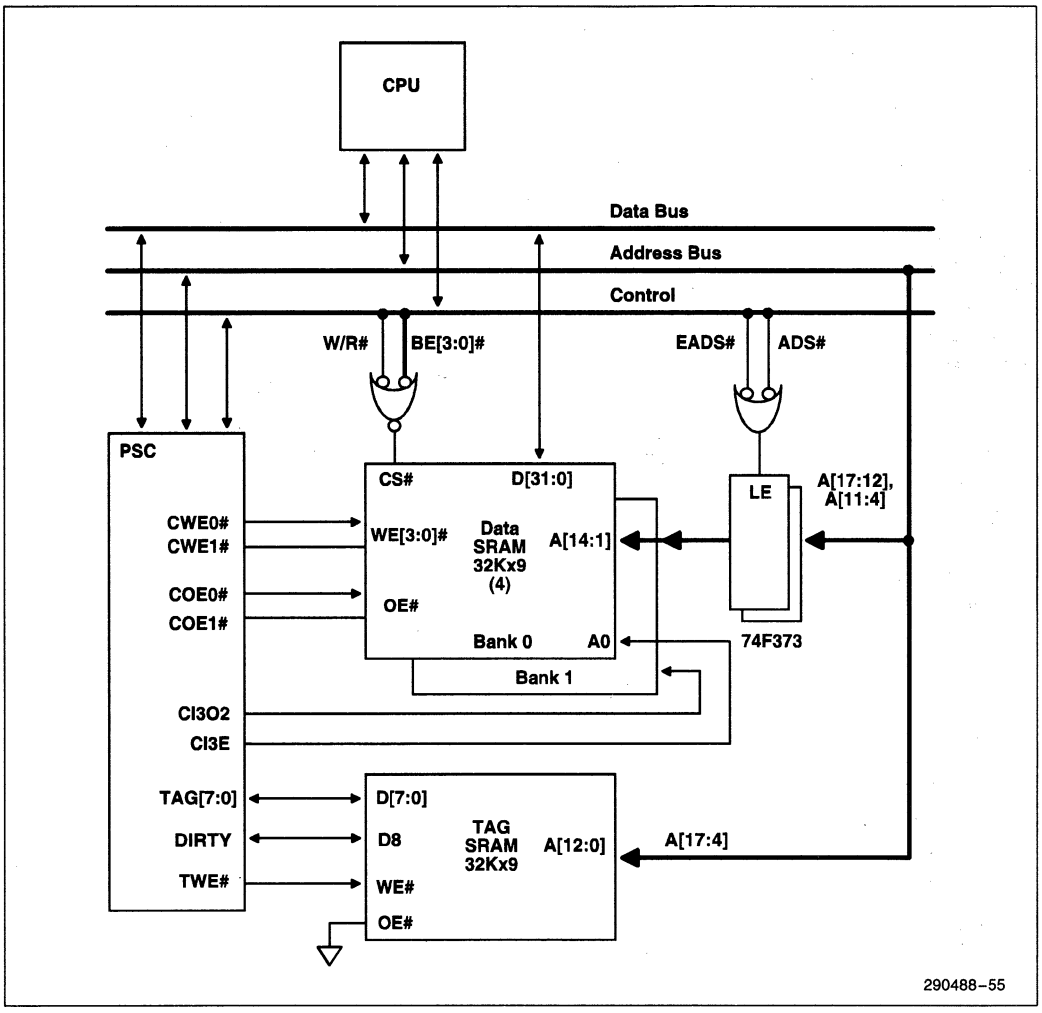


Figure 12. The PSC with an Interleaved L2 (256 KBytes Data)

4.13 Dram Interface

The DRAM controller interfaces main memory to the Host Bus, PCI Bus, and ISA Bus. The PSC provides the control signals, address lines, and data path control. A two-way interleaved DRAM organization is supported for optimum main memory performance. Up to ten single-sided SIMMs or four double-sided and two single-sided SIMMs provide a maximum of 128 MBytes of main memory. The DRAM controller interface is fully configurable through a set of control registers (the DRAM Control Mode Register, the DRAM Memory Hole Register, and the five DRAM Row Boundary [DRB] Registers).

The PSC controls a 64-bit memory array (72-bit including parity) and/or a 32-bit memory array (36-bit including parity) ranging in size from 1 to 128 MBytes using industry standard 36-bit wide memory modules with fast page-mode DRAMs. Both single- and double-sided SIMMs are supported. The eleven multiplexed address lines (MA[10:0]) permit the use of 256Kx36, 1Mx36, and 4Mx36 SIMMs. Both interleaved and non-interleaved rows are supported simultaneously. Five RAS# lines enable up to five rows of DRAM. Eight CAS# lines allow byte control over the array during read and write operations. The PSC supports 70 ns DRAMs. Page mode accesses efficiently transfer data in bursts. Parity support is optional.

The PSC DRAM performance is controlled through programmable wait-states. Various DRAM timing parameters may be set in the DRAM Control Register. Programmable timings support 70 ns DRAMs at 25 MHz and 33 MHz. Programmable parameters include RAS precharge, CAS precharge, CAS low time, MA setup time, and MA hold time. The PSC provides RAS only refresh, de-coupled from ISA refresh, and hidden from any access.

4.13.1 DRAM ADDRESS TRANSLATION

The multiplexed row/column address to the DRAM memory array is provided by the MA[10:0] signals and is derived from the host address bus as defined by Table 20. The page size is 2 KBytes for non-interleaved rows and 4 KBytes for interleaved rows. The page offset address is driven over the MA[8:0] lines when driving the column address. In non-interleaved rows the PSC drives address bit 2 on the MA8 line, minimizing the multiplexing required. The MA[10:0] lines are translated from the address lines A[24:3] for all memory accesses.

4.13.2 DRAM STRUCTURE

Figure 13 illustrates an 8-SIMM configuration supporting single-sided SIMMs. A row in the DRAM array is made up of two SIMMs that share a common RAS# line. SIMM0 and SIMM1 comprise row 0 and are connected to RAS0#. Within any given row, the two SIMMs must be the same size. Among the four rows, SIMM densities can be mixed in any order (i.e., there are no restrictions on the ordering of SIMM densities among the four rows). Any row may also contain a single SIMM (non-interleaved). This allows the user to upgrade the 82420EX PCIset platform one SIMM at a time. Each row is controlled by up to 8 CAS lines. Any row that is populated with only one SIMM must be connected to the low order CAS lines (CAS[3:0]#). The MA[10:0] and WE# lines should be externally buffered if a load of more than two double-sided SIMMs is implemented. Two buffered copies of the signals are recommended to drive the four row array. Three buffered copies of the signals are recommended to drive the five row array.

Figure 14 illustrates a 3-SIMM configuration using one single-sided SIMM in row one, and two double sided SIMMs in row 2. In this configuration, single- and double-sided SIMMs can be mixed. For example, if a single-sided SIMM is installed into the socket marked SIMM0 (connected to RAS0#) and RAS1# is not connected, row 0 is then populated and row 1 is empty. Two double-sided SIMMs could then be installed in the sockets marked SIMM2 and SIMM3, populating rows 2 and 3. For systems with no more than 2 SIMMs, the 244's buffering MA[10:0] and WE#, as well as the 245's on the host data bus, may be omitted. (Note that the 245's on the Host Data Bus are recommended at 50 MHz, regardless of the number of SIMMs.)

Table 20. DRAM Address Translation for Interleaved Rows

MA[10:0]	10	9	8	7	6	5	4	3	2	1	0
Interleaved Rows											
Column Address	A23	A21	A11	A10	A9	A8	A7	A6	A5	A4	A3
Row Address	A24	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12
Non-Interleaved Rows											
Column Address	A23	A21	A2	A10	A9	A8	A7	A6	A5	A4	A3
Row Address	A22	A20	A11	A19	A18	A17	A16	A15	A14	A13	A12

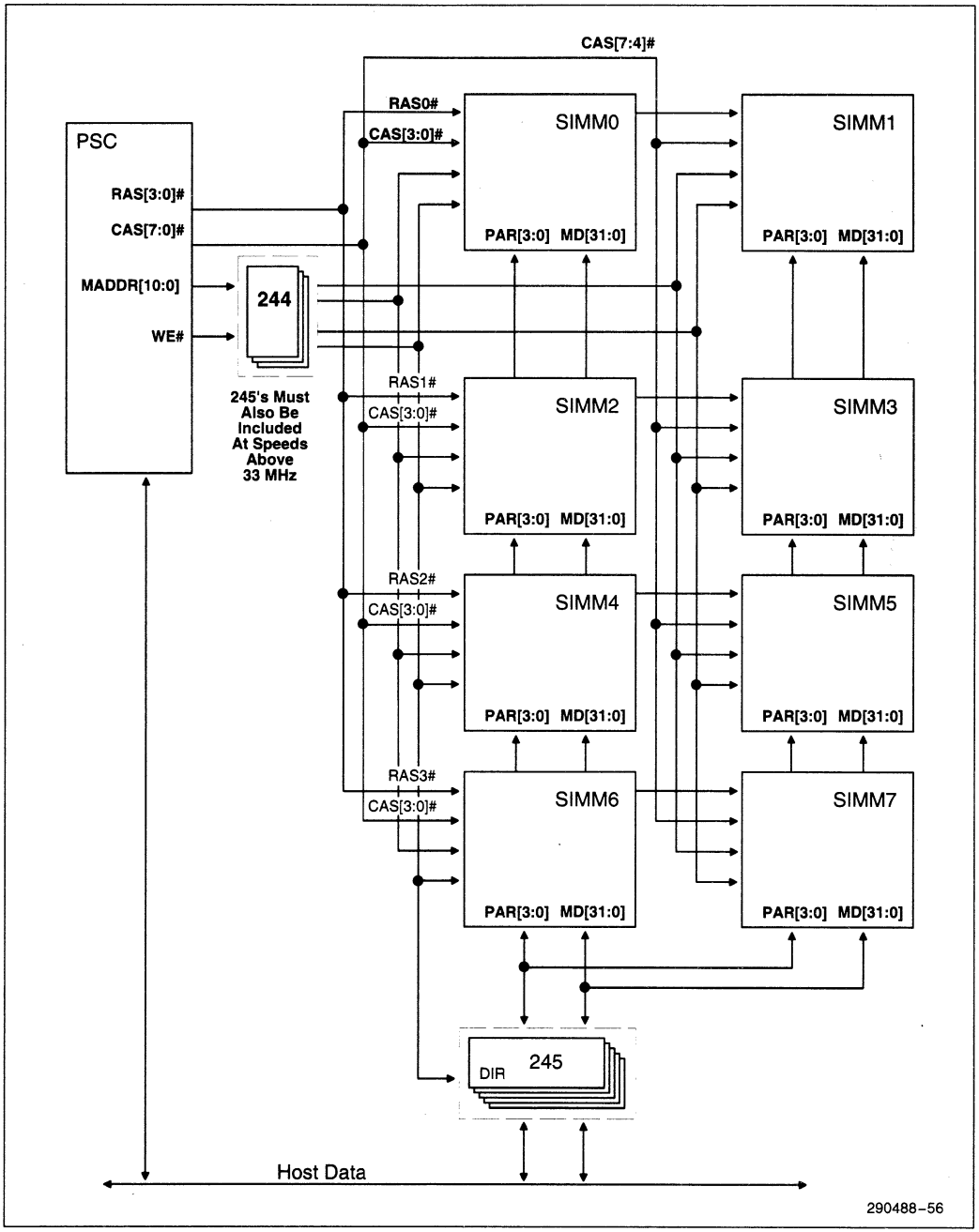


Figure 13. 8-SIMM Configuration Supporting Single-Sided SIMMs

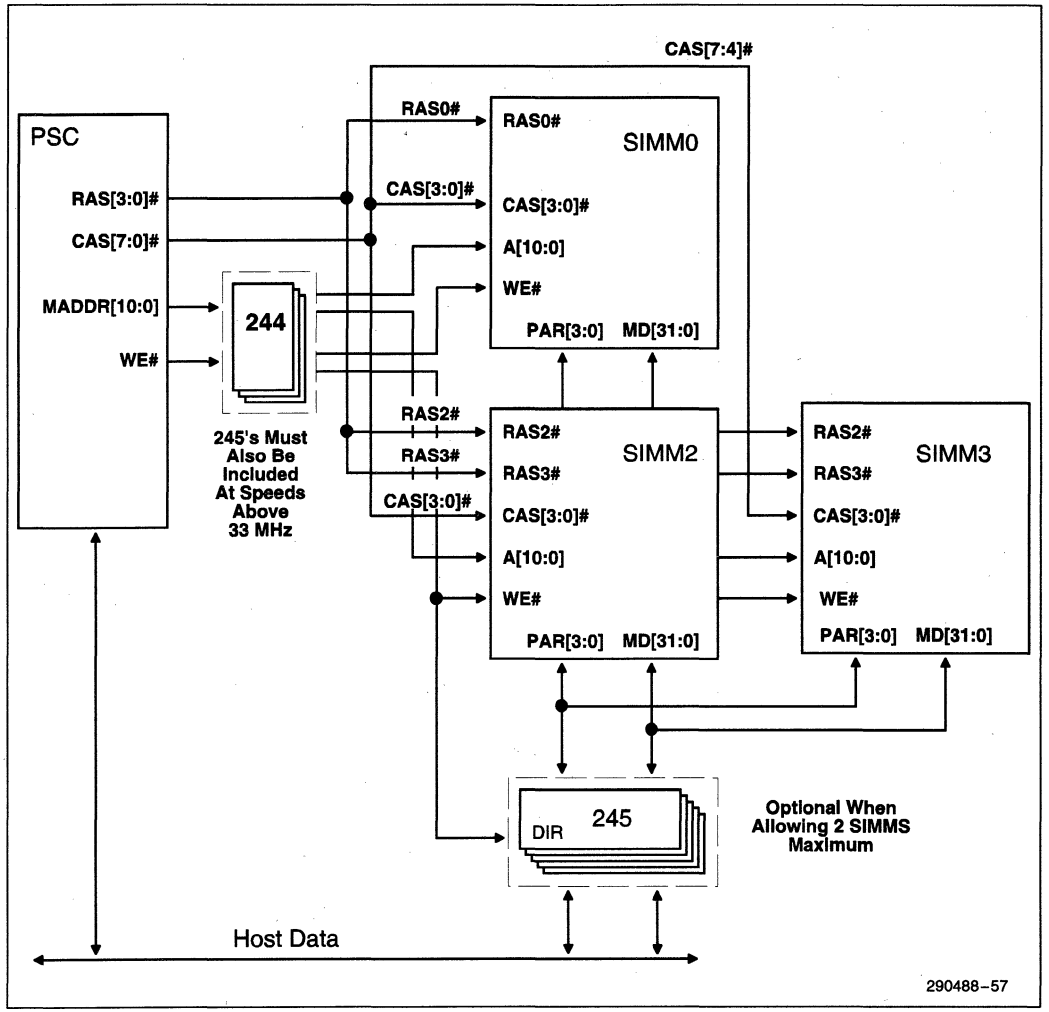


Figure 14. 3-SIMM Configuration (One Single-Sided SIMM in Row One and Two Double-Sided SIMMs in Row Two)

4.13.3 DRAM SIMM SIZE/DENSITY OPTIONS

Providing support for both interleaved and non-interleaved rows gives the user a wide range of DRAM population options. In any row the PSC supports address depths of 256K, 1M, or 4M. Each row may be populated with one or two SIMMs.

4.13.4 DRAM PAGE MODE

The PSC may be programmed to leave the RAS lines active after a DRAM access for faster page mode accesses. The mode is programmed in the DRAM Control Register. When Page Mode is enabled, the RAS lines remain active after the access.

The next access is considered a page hit if the access is to the same page. The PSC has a 2 KByte page size for non-interleaved rows and a 4 KByte page size when accessing an interleaved row. If the page mode is not enabled all accesses are row misses.

4.13.5 PROGRAMMABLE WAIT-STATES

4.13.5.1 RAS Precharge

RAS precharge impacts page miss accesses, as well as the refresh time. In a page miss, the active RAS line must be negated and a new row address strobed into the DRAMs. When negated, RAS precharge determines the number of cycles before the RAS line can be re-asserted. Similarly, the RAS precharge determines the time RAS must be negated before and after refresh.

4.13.5.2 CAS Read Time

CAS read time indicates how long to leave CAS low after asserted during a DRAM read and how long it is negated between access. In the case of interleaved DRAM access, the CAS high time implied by this setting is ignored as this high time is more constrained by the opposite banks low time.

4.13.5.3 CAS Write Time

CAS write time controls the CAS waveform for DRAM writes. The high time defined by the CAS write time setting is ignored for interleaved rows.

4.13.5.4 MA Setup Time

The MA setup time defines the number of cycles after MA is switched before RAS or CAS are driven active. DRAMs latch row and column address when RAS and CAS fall. The setup time of the addresses to RAS/CAS for all DRAMs is 0 ns. The PSC supports direct drive of the MA lines, which removes any external logic between the MA on the PSC and the DRAM. When there is no external buffering, the MA-to-DRAM path and the CAS-to-DRAM path are well matched. In these cases an aggressive MA setup time can be programmed. When the external buffers are present, there could be mismatch in the paths, and a more conservative MA setup should be chosen.

4.13.5.5 MA Hold Time

The MA hold time defines the number of clocks after RAS or CAS have been asserted before MA can be changed. This value is determined in a manner similar to MA setup time. DRAM requirements for 60 ns and 70 ns DRAMs range from 10 ns to 15 ns.

4.13.6 DRAM PERFORMANCE

Table 21 summarizes DRAM performance for various programming options for both 60 ns and 70 ns DRAMs. Other cycle constraints that are met by design include DRAM access from RAS falling and DRAM access from row address, and many others. All accesses shown below assume no wait-states required for other Host Bus devices (L2, etc.). If, as discussed in the previous section, buffers must be turned around and contention with other host devices avoided, the minimum lead off for read page hits will be lengthened by one cycle.

Table 21. DRAM Performance

System	RAS pre-charge	CAS Read	CAS Write	MA Setup	MA Hold	Clock Freq.	Performance No L2	Performance With L2
60 ns DRAM Min	1	1/1	1/1	.5	.5	25 MHz	Ird: 3/5/5-1-1-1 NIrd: 3/5/5-2-2-2 wr: 3/5/5-2-2-2	Ird: 3/5/5-1-1-1 NIrd: 3/5/5-2-2-2 Same as No L2
Margin	1.5	1.5/.5	1/1	1	.5	33 MHz	Ird: 3/6/7-2-2-2 NIrd: 3/6/7-2-2-2 wr: 3/5/6-2-2-2	Ird: 4/6/7-2-2-2 NIrd: 4/6/7-2-2-2 Same as No L2
60 ns DRAM High	1.5	1.5/.5	1/1	.5	.5	25 MHz	Ird: 3/5/6-2-2-2 NIrd: 3/5/6-2-2-2 wr: 3/5/6-2-2-2	Ird: 4/5/6-2-2-2 NIrd: 4/5/6-2-2-2 Same as No L2
Margin	1.5	1.5/.5	1/1	1	1	33 MHz	Ird: 3/7/7-2-2-2 NIrd: 3/7/7-2-2-2 wr: 3/6/7-2-2-2	Ird: 4/7/7-2-2-2 NIrd: 4/7/7-2-2-2 Same as No L2
70 ns DRAM Min	1.5	1.5/.5	1/1	.5	.5	25 MHz	Ird: 3/5/6-2-2-2 NIrd: 3/5/6-2-2-2 wr: 3/5/6-2-2-2	Ird: 4/5/6-2-2-2 NIrd: 4/5/6-2-2-2 Same as No L2
Margin	2	1.5/.5	1/1	1	.5	33 MHz	Ird: 3/6/7-2-2-2 NIrd: 3/6/7-2-2-2 wr: 3/5/7-2-2-2	Ird: 4/6/7-2-2-2 NIrd: 4/6/7-2-2-2 Same as No L2
70 ns DRAM High	2	1.5/.5	1/1	.5	.5	25 MHz	Ird: 3/5/7-2-2-2 NIrd: 3/5/7-2-2-2 wr: 3/5/6-2-2-2	Ird: 4/5/7-2-2-2 NIrd: 4/5/7-2-2-2 Same as No L2
Margin	3	2/1	1/1	1	.5	33 MHz	Ird: 4/7/9-2-2-2 NIrd: 4/7/9-3-3-3 wr: 3/6/8-2-2-2	Ird: 4/7/9-2-2-2 NIrd: 4/7/9-3-3-3 Same as No L2

NOTES
I = Interleaved
NI = Non-Interleaved

4.14 Power Management

The 82420EX PCIset has extensive power management capability permitting a system to operate in a low power state without being powered down. In a typical desktop personal computer there are two states—Power On and Power Off. Leaving a system powered on when not in use wastes power. The 82420EX PCIset provides a Fast On/Off feature that creates a third state called Fast Off (Figure 15). When in the Fast Off state, the system consumes less power than the Power On state.

The 82420EX PCIset's power management architecture is based on three functions—System Management Mode (SMM), Clock Control, and Advanced Power Management (APM). Software (called SMM code) controls the transitions between the Power On state and the Fast Off state. The IB invokes this software by generating an SMI to the CPU (asserting the SMI# signal). A variety of programmable events are provided that can generate an SMI. The SMM code places the system in either the Power On state or the Fast Off state.

A Fast On event is an event that instructs the computer (via an SMI to the CPU) to enter the Power On state in anticipation of system activity by the user. Fast On events are programmable and include moving the mouse, pressing a key on the keyboard, an external hardware event, an incoming call to a system FAX/Modem, a RTC alarm, or the operating system.

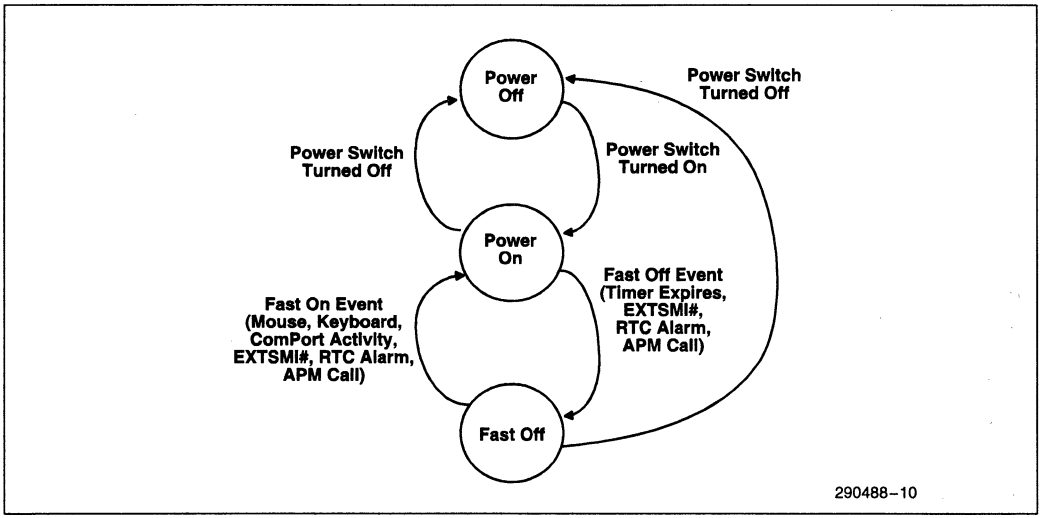


Figure 15. Fast On/Off Flow

4.14.1 SMM MODE

SMM mode is invoked by asserting the SMI# signal to the CPU. The PCIset provides a variety of programmable events that can generate an SMI. When the CPU receives an SMI, it enters SMM mode and executes SMM code out of SMRAM. The SMM code places the system in either the Power On state or the Fast Off state. In the Power On state, the computer system operates normally. In this state one of the four programmable events listed below can trigger an SMI.

1. A global idle timer called the Fast Off timer expires (an indication that the end user has not used the computer for a long period of time).
2. The EXTSMI# pin is asserted.
3. A RTC alarm interrupt is detected.
4. The operating system issues an APM call.

4.14.2 SMI SOURCES

The SMI# signal can be asserted by hardware events, an external SMI event (EXTSMI#), and software events (via the APMC and APMS Registers). Enable/disable bits (in the SMIEN Register) permit each event to be individually masked from generating an SMI. In addition, the SMI# signal can be globally enabled/disabled in the SMICNTL Register. Status of the individual events causing an SMI is provided in the SMIREQ Register. For detailed information on the SMI control/status registers, refer to Section 3.0, Register Description.

Hardware Interrupt Events

Hardware events are enabled/disabled from generating an SMI in the SMIEN Register. The hardware events consist of IRQ[12,8#,4,3,1] and the Fast Off Timer. When enabled, the occurrence of the corresponding hardware event generates an SMI (asserts the SMI# signal), regardless of the current power state of the system.

Fast Off Timer

The Fast Off Timer is used to indicate (through an SMI) that the system has been idle for a pre-programmed period of time. The timer counts down at a selectable rate from a programmed start value and when the count reaches 00h, an SMI is generated. The timer decrement rate can be set to 1 count every minute, ms, or HCLKIN (via the SMICNTL Register) and is re-loaded each time a System Event occurs.

System events are programmable events that can keep the system in the Power On state when there is system activity. These events are indicated by the assertion of IRQ[15:9,8#,7:3,1:0], NMI, or SMI signals.

In addition to system events, *break events* cause the system to transition from a Fast Off state to the Power On state. System events (and break events) are enabled/disabled in the SEE Register. When enabled and the associated hardware event occurs (signal is asserted), the Fast Off Timer is re-loaded with its initial count.

EXTSMI#

The EXTSMI# input pin provides the system designer the capability to invoke SMM with external hardware. For example, the EXTSMI# input could be connect to a "green button" permitting the user to enter the Fast Off state by depressing a button. The EXTSMI# generation of an SMI is enabled/disabled in the SMIEN Register.

Software Events

Software events (accessing the APMx Registers) indicate that the OS is passing power management information to the SMI handler. There are two Advanced Power Management (APM) registersAPM Control (APMC) and APM Status (APMS) Registers. These registers permit software to generate an SMI; by writing to the APMC Register. For example, the APMC can be used to pass an APM command between APM OS and BIOS and the APMS Register could be used to pass data between the OS and the SMI handler. For detailed descriptions of these registers See Section 3.0, Register Description. Note that the two APM Registers are located in normal I/O space. The remaining power management registers are located in PCI configuration space.

4.14.3 SMI (SMI#) AND INTERRUPT (INTR) ORDERING

To maintain the SMI#/INTR order, an interrupt blocking mechanism has been incorporated into the IB. The blocking mechanism blocks interrupt requests that can generate an SMI# from being processed by the interrupt controller until the SMI# has been serviced by the SMM code. This blocking mechanism is selective and only affects the IRQ[12,8#,4,3,1] signals that are enabled to generate an SMI# (via the SMIEN Register). In addition, the blocking mechanism is only invoked if the SMI# signal is unmasked (via the SMICNTL Register). Note that PIRQ[1,0]s routed to one of the dual-purpose interrupt request lines are also affected by the blocking mechanism. Thus, the following criteria applies to the blocking mechanism:

1. The assertion of IRQ[12,8#,4,3,1] are blocked if the interrupt request line is programmed for SMI (i.e., the interrupt request line is enabled for SMI via the SMIEN Register and the SMI# signal is not masked via the CSMIGATE bit in the SMICNTL Register).
2. A blocked IRQ request is unblocked and processed by the interrupt controller when software masks the SMI# signal by setting the CSMIGATE bit to 0 in the SMICNTL Register.
3. IRQs that are already asserted when SMI# is unmasked (CSMIGATE set from a 0 to 1) are not blocked and are processed by the interrupt controller.

The following are BIOS and hardware considerations regarding the SMI#/INTR ordering:

- To process blocked, active IRQs, software (SMM code only) should mask the SMI# signal. If SMI# is masked outside SMM code when an IRQ that can generate an SMI# and the INTR signal is active, the SMI# and INTR order is not guaranteed.
- The SMI software handler should use the SMIREQ Register status bits and not the interrupt controller IRR to dispatch the routine (vector to the appropriate SMI function). By using the SMIREQ Register, the SMI handler has the freedom to mask the SMI# signal before or after the execution of the SMI function. Note that the IRR is updated only when the SMI# signal is masked.
- The IB updates new active SMI sources while the system is in SMM, independent of the state of the mask/unmask of the SMI# signal. When the SMI handler completes the execution of a certain SMI function, it should check whether other active SMI sources exist and service these sources before executing the **RSM** instruction.
- When the SMIREQ Register indicates that all SMI sources are inactive, the SMI handler should unmask the SMI# signal and execute the **RSM** instruction. Note that, all active SMI sources (status bits not set to 0 in the SMIREQ Register), will generate a new SMI# to the CPU when SMI# is unmasked.
- The SMI handler should not check for active SMI sources, or execute the new sources, after the SMI# signal is unmasked. Such an SMI source will generate a new active SMI# and the CPU will latch the new SMI# (and recognize it after **RSM**). Thus, executing the SMI source before **RSM** will cause a spurious SMI# after the **RSM** execution.

4.14.4 CLOCK CONTROL

The CPU can be put in a low power state by asserting the STPCLK# signal. STPCLK# is an interrupt to the CPU. However, for this type of interrupt, the CPU does not generate an interrupt acknowledge cycle. Once the STPCLK# interrupt is executed, the CPU enters the Stop Grant state. In this state, the CPU's internal clocks are disabled and instruction execution is stopped. The Stop Grant state is exited when the STPCLK# signal is negated.

Software can assert STPCLK#, if enabled via the SMICNTL Register, by a read of the APMC Register. Note that STPCLK# can also be periodically asserted by using clock throttling as described below.

The IB automatically negates STPCLK# when a break event occurs (if enabled in the SEE Register) and the CPU stop grant special cycle has been received. Software can negate STPCLK# by disabling STPCLK# in the SMICNTL Register or by a write to the APMC Register.

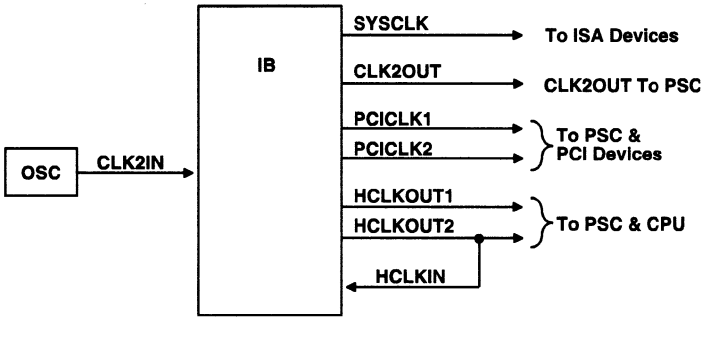
Clock Throttling (Emulating Clock Division)

Clock throttling permits the IB to periodically place the CPU in a low power state. This emulates clock division. When clock throttling is enabled, the CPU runs at full frequency for a pre-defined time period and then is stopped for a pre-defined time period. The Run/Stop time interval ratio emulates the clock division effect from a power/performance point of view. However, clock throttling is more effective than dividing the CPU frequency. For example, if the CPU is in the Stop Grant state and a system break event occurs, the CPU clock returns to full frequency. In addition, there is no recovery time latency to start the clock.

Two programmable 8-bit clock throttle timer control registers set the STPCLK# high (negate) and low (assert) times—the CTLTMRH and CTLTMRL Registers. The timer is clocked by a 32 μs internal clock. This allows a programmable timer interval for both the STPCLK# high and low times of 0-8 ms.

4.15 Clocks

The IB contains a clock generation unit that generates the system clocks. The IB generates HCLKOUTx (host clocks), PCICLKx (PCI clocks), SYSCLK (ISA System clock), and CLK2OUT (delayed version of CLK2IN) signals to the system (Figure 16). An external clock driver is not required. Two HCLKOUT signals and two PCICLK signals are provided to drive the loads. One of the HCLKOUT outputs is fed back to the HCLKIN pin to become the IB clock. CLK2OUT is used by the PSC. The IB uses a 2X clock input (CLK2IN) as the source to generate the system clocks. For CPU or PCI initiated cycles to the ISA Bus, SYSCLK is stretched to synchronize the falling edge BALE to the rising edge of the SYSCLK.



NOTE:
HCLKIN can be connected to either HCLKOUT1 or HCLKOUT2.

Figure 16. System Clock Distribution

There are three clock configurations (strapping options) that set the clock divisors as shown in Table 22. The IB samples the CMDV# and SIDLE# signals on the rising edge of PWROK to determine the clock divisor value. The IB CLK2IN pin is divided by either 1 or 2 to generate HCLKOUT[2,1] and PCICLK[2,1]. One of the HCLKOUT signals is fed back to the HCLKIN input of the IB and divided by either 3, 4, 5, or 6, to generate SYSCLK. Note that the configuration information provided in Table 22 is software accessible in the Host Bus Select Register.

5.0 DESIGN CONSIDERATIONS

Design considerations are chip set related issues which affect all 82420EX PCIset designs. See your Intel representative and the 82420EX PCIset Value Flexible Motherboard Design Guide (297460) for the latest version of the design considerations.

6.0 ELECTRICAL CHARACTERISTICS

This section provides the 82420EX PCIset maximum ratings, DC characteristics and AC characteristics including timing diagrams.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

6.1 Maximum Ratings

Case Temperature Under Bias . . . −65°C to +110°C

Storage Temperature . . . . . −65°C to +150°C

Supply Voltages
with Respect to Ground . . . −0.5V to V_{CC} + 0.5V

Voltage on Any Pin . . . . . −0.5V to V_{CC} + 0.5V

Power Consumption (IB) 0.5W

Power Consumption (PSC) 1.0W

Table 22. Clock Configurations

Strapping Options		CLK2IN	HCLKOUT	HCLKOUT Divisor	PCICLK	PCICLK Divisor	SYSCLK	SYSCLK Divisor
SIDLE#	CMDV#							
0	0	50 MHz	25 MHz	2	25 MHz	2	8.33 MHz	3
0	1	66 MHz	33 MHz	2	33 MHz	2	8.25 MHz	4
1	0	Reserved						
1	1	Reserved						

6.2 PSC and IB DC Characteristics

DC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C)

Symbol	Parameter	Min	Max	Units	Test Conditions	Notes
V_{IL1}	Input Low Voltage	−0.5	0.8	V		
V_{IH1}	Input High Voltage	2.0		V		
V_{IL2}	Input Low Voltage		0.3*V_{CC}	V		10
V_{IH2}	Input High Voltage	0.7*V_{CC}		V		10
V_{T+}	TTL Schmitt Trigger, Rising Threshhold	1.9		V	V_{CC} = 5 V	11
V_{T-}	TTL Schmitt Trigger, Falling Threshhold		1.3	V	V_{CC} = 5 V	11
V_{T+}	Hysteresis Voltage	600		mV	V_{CC} = 5 V	11
V_{OL1}	Output Low Voltage (IB)		0.45	V	I_{OL} = 24 mA	1
V_{OH1}	Output High Voltage (IB)	2.4		V	I_{OH} = −3.0 mA	1
V_{OL2}	Output Low Voltage (IB)		0.4	V	I_{OL} = 4 mA	2
V_{OH2}	Output High Voltage (IB)	2.4		V	I_{OH} = −2 mA	2
V_{OL3}	Output Low Voltage (IB)		0.4	V	I_{OL} = 8 mA	3
V_{OH3}	Output High Voltage (IB)	2.4		V	I_{OH} = −2 mA	3
V_{OL4}	Output Low Voltage (PSC)		0.45	V	I_{OL} = 8 mA	4
V_{OH4}	Output High Voltage (PSC)	2.4		V	I_{OH} = −2 mA	4
V_{OL5}	Output Low Voltage (PSC)		0.45	V	I_{OL} = 4 mA	5
V_{OH5}	Output High Voltage (PSC)	2.4		V	I_{OH} = −2.0 mA	5
V_{OL6}	Output Low Voltage (PSC)		0.4	V	I_{OL} = 4 mA	6
V_{OH6}	Output High Voltage (PSC)	2.4		V	I_{OH} = −4 mA	6
V_{OL7}	Output Low Voltage		0.4	V	I_{OL} = 6 mA	7
V_{OH7}	Output High Voltage	2.4		V	I_{OH} = −2.0 mA	7
V_{OL8}	Output Low Voltage		0.4	V	I_{OL} = 4 mA	8
V_{OH8}	Output High Voltage	0.9*V_{CC}		V	I_{OH} = −2 mA	8
V_{OL9}	Output Low Voltage		0.4	V	I_{OL} = 8 mA	9
V_{OH9}	Output High Voltage	0.9*V_{CC}		V	I_{OH} = −2mA	9
I_{LI1}	Input Leakage Current		±10	A	0V<V_{IN}<V_{CC}	
I_{LI2}	Input Leakage Current		−350	A	0V<V_{IN}<V_{CC}	12
I_{LO}	Output Leakage		±10	A	0.45<V_{IN}<V_{CC}	

DC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C) (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions	Notes
C_{IN}	Capacitance Input		9	pF	@ 1 MHz	
C_{OUT}	Capacitance Output or I/O		9	pF	@ 1 MHz	
I_{CC}	V_{CC} Supply Current (IB)		100	mA		
I_{CC}	V_{CC} Supply Current (PSC)		200	mA		

NOTES:
1. V_{OL1}, V_{OH1} = SD[15:0], SA[19:0], LA[23:17], SBHE#, MEMR#, MEMW#, AEN, SPKR, BALE, SYSCLK, IOR#, IOW#, SMEMR#, SMEMW#, RSTDRV, REFRESH#, IOCHRDY, MEMCS16#, TC, DACK#
2. V_{OL2}, V_{OH2} = XBUSTR#, XBUSOE#, IGNNE#, RTCCS#, KBCCS#, BIOSCS#, RTCALE, INTR, NMI, CMDV#, SIDLE#, LREQ#, SMI#, STPCLK#
3. V_{OL3}, V_{OH3} = A[17:2], HCLKOUT1, HCLKOUT2, PCICLK1, PCICLK2, CPURST, PCIRST#
4. V_{OL4}, V_{OH4} = A[31,26:2], HD[31:0], HDP[3:0], BE[3:0]#, W/R#, RDY#, BRDY#, CI3E, CI3O2, CWE[1:0]#, COE[1:0]#, MA[10:0], RAS[4:0]#, CAS[7:0]#, WE#, LBIDE#
5. V_{OL5} V_{OH5} = HOLD, AHOLD, EADS#, KEN#, TWE#, TAG[8:0], AD[31:0], C/BE[3:0]#, PAR, CMDV#, SIDLE#, LGNT#, PGNT[1:0]
6. V_{OL6}, V_{OH6} = SRESET/INIT
7. V_{OL7}, V_{OH7} = FRAME#, IRDY#, TRDY#, STOP#, SERR#, DEVSEL#
8. V_{OL8}, V_{OH8} = CMDV#, SIDLE#, LREQ#, LGNT#
9. V_{OL9}, V_{OH9} = CLK2OUT, PCICLK1, PCICLK2, HCLKOUT1, HCLKOUT2
10. V_{IL2}, V_{IH2} = HCLKIN (IB), CMDV#, SIDLE#, LGNT#
11. This applies to PWROK, EXTSMI#, FERR#, IRQ[1,3-7,9-11,14,15],IRQ12M, PIRQ[1:0].
12. This applies to pins that include a weak internal pull-up (IRQ8#[IB], FERR#[IB], D/C#[PSC], ADS#[PSC], BLAST#[PSC], HITM#[PSC], SMI#[PSC], SMIACT#[PSC]).

6.3 IB AC Characteristics

This section provides the AC parameters and timing diagrams.

6.3.1 CLOCK/RESET TIMINGS

AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C)

Symbol	Parameter	Min	Max	Units	Notes	Fig
t1a	HCLKIN Period Stability		0.1%			
t1b	HCLKIN Period	30.0	40.0	ns		18
t1c	HCLKIN High/Low Time	8.0		ns		18
t1d	HCLKIN Rise/Fall Time		2.0	ns		18
t1e	HCLKOUT[2,1] Period	30.0	40.0	ns		18
t1f	HCLKOUT[2,1] High/Low Time	12.0		ns		18
t1g	HCLKOUT[2,1] Rise/Fall Time		2.0	ns		18
t1h	CLK2IN Period Stability		0.1%			
t1i	CLK2IN Period	15	20.0	ns		18
t1j	CLK2IN High/Low Time	4.0		ns		18
t1k	CLK2IN Rise/Fall Time		1.5	ns		18
t1l	CLK2OUT Period	15	20	ns		18
t1o	PCICLK[2,1] Period	30	40	ns		18
t1p	PCICLK[2,1] High/Low Time	12.0		ns		18
t1q	PCICLK[2,1] Rise/Fall Time		3.0	ns		18
t1r	OSC Period	67	70	ns		18
t1s	OSC High/Low Time	20		ns		18
	ISA CLOCK TIMINGS					
	SYSCLK					
t1t	Period	120	125	ns		18
t1u	High/Low time	56		ns		18
t1v	Rise/Fall time		4	ns		18
	MISCELLANEOUS CLOCK TIMINGS					
t1w	PCICLK to HCLKOUT Skew		0.4	ns	1	19
	RESET TIMINGS					
t1x	CPURST, PCIRST#, RSTDRV Driven Inactive After PWROK is Driven Active High.	2		HCLKIN		20
t1y	CPURST, PCIRST#, RSTDRV Active Pulse Width. Initiated via the TRC Register.	1		ms		21
t1z	CPURST Valid Delay from HCLKIN Rising	3	17	ns		

NOTES:
1. Except when STPCLK# is active.

6.3.2 PSC/IB LINK INTERFACE TIMINGS

AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C)

Symbol	Parameter	Min	Max	Units	Notes	Fig
t2a	CMDV#, SIDLE# Setup to HCLKIN Rising	11		ns		24
t2b	A[17:2] Setup to HCLKIN Rising	6		ns		24
t2c	SIDLE#, A[17:2] Hold from HCLKIN Rising	2		ns		24
t2c1	CMDV# Hold from HCLKIN Rising	2.6		ns		24
t2d	CMDV#, SIDLE#, A[17:2] Valid Delay from HCLKIN Rising	3	10	ns		25
t2e	LGNT# Setup to HCLKIN Rising	11		ns		24
t2f	LGNT# Hold from HCLKIN Rising	2		ns		24
t2g	LREQ# Valid Delay from HCLKIN Rising	2	9	ns		25
t2h	SIDLE# Driven Valid After CPURST is Driven High	2		HCLKIN		22

6.3.3 SYSTEM POWER MANAGEMENT TIMINGS

AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C)

Symbol	Parameter	Min	Max	Units	Notes	Fig
	SMI#					
t3a	Valid Delay from HCLKIN	2	9	ns		25
t3b	Active Pulse Width	3		HCLKIN		23
t3c	Inactive Pulse Width	4		HCLKIN		23
	EXTSMI#					
t3d	Active Pulse Width	2		HCLKIN		23
t3e	Inactive Pulse Width	4		HCLKIN		23
t3f	Valid Setup to HCLKIN	6		ns		24
t3g	Valid Hold from HCLKIN	2		ns		24
	STPCLK#					
t3h	Valid Delay from HCLKIN	2	10	ns		25
t3i	STPCLK# Inactive Pulse Width	5		HCLKIN		23

6.3.4 ISA BUS AND X-BUS TIMINGS

ISA Bus and X-Bus AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C)

Symbol	Parameter	Min	Max	Units	Type	Size	Notes	Fig
	IB AS MASTER TIMINGS							
	BALE							
t4a	BALE Pulse Width	52		ns	M,I/O	8,16		26,27,28,29
t4b	BALE Driven Active from MEMx#, IOx# Inactive	44		ns	M,I/O	8,16		26,27,28,29
	LA[23:17]							
t5a	LA[23:17] Valid Setup to BALE Inactive	150		ns	M	8,16	7	26,27
t5b	LA[23:17] Valid Hold from BALE Inactive	26		ns	M	8,16		26,27
t5c	LA[23:17] Valid Setup to MEMx# Active	150		ns	M	16		27
t5d	LA[23:17] Valid Setup to MEMx# Active	173		ns	M	8		26
t5e	LA[23:17] Invalid from MEMx# Active	39		ns	M	16		27
t5f	LA[23:17] Invalid from MEMx# Active	39		ns	M	8		26
	SA[19:0], SBHE#							
t6a	SA[19:0], SBHE# Valid Setup to MEMx# Active	90		ns	M	16	13,15	27
t6b	SA[19:0], SBHE# Valid Setup to IOx# Active	100		ns	I/O	16		29
t6c	SA[19:0], SBHE# Setup to MEMx#, IOx# Active	100		ns	M,I/O	8		26,28
t6d	SA[19:0], SBHE# Valid Setup to BALE Inactive	90		ns	M,I/O	8,16	13,15	26,27,28,29
t6e	SA[19:0], SBHE# Valid Hold from MEMx#, IOx# Inactive	51		ns	M,I/O	8,16		26,27,28,29

ISA Bus and X-Bus AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C) (Continued)

Symbol	Parameter	Min	Max	Units	Type	Size	Notes	Fig
	MEMR#, MEMW#, IOR# and IOW#							
t7a	MEMx# Active Pulse Width (std)	225		ns	M	16		27
t7b	IOx# Active Pulse Width (std)	160		ns	I/O	16		29
t7c	MEMx# Active Pulse Width (nws)	105		ns	M	16	1	27
t7d	MEMx# or IOx# Active Pulse Width (std)	520		ns	M,I/O	8		26,28
t7e	MEMx# or IOx# Active Pulse Width (nws)	160		ns	M,I/O	8	1	26,28
t7f	MEMx# Inactive Pulse Width	103		ns	M	16		27
t7g	MEMx# Inactive Pulse Width	163		ns	M	8		26
t7h	IOx# Inactive Pulse Width	163		ns	I/O	8,16		28,29
t7i	MEMx#, IOx# Driven Inactive from IOCHRDY Active	120		ns	M,I/O	8,16		26,27,28,29
	SMEMR# and SMEMW#							
t8a	SMEMR# & SMEMW# Propagation Delay from MEMR# and MEMW#		5	ns	M	8,16		26,27
	Read Data							
t9a	Read Data Driven from MEMR#, IOR# Active	0		ns	M,I/O	8,16		26,28,29
t9b	Read Data Valid Setup to MEMR#, IOR#	20		ns	M,I/O	8,16		26,27,28
t9c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8,16		26,27,28,29
t9d	Read Data Tri-stated from MEMR# and IOR# Inactive		41	ns	M,I/O	8,16		26,27,28,29
	Write Data							
t10a	Write Data Valid Setup to MEMW#, IOW# Active	30		ns	M,I/O	8,16		26,27,28,29
t10b	Write Data Valid Hold from MEMW#, IOW# Inactive	45		ns	M,I/O	8,16		26,27,28,29
t10c	Write Data Tri-Stated from MEMW#, IOW# Inactive		75	ns	M,I/O	8,16		26,27,28,29
t10d	Write Data Driven Valid after Read MEMR#, IOR# Inactive	41		ns	M,I/O	8,16		26,27,28,29

ISA Bus and X-Bus AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C) (Continued)

Symbol	Parameter	Min	Max	Units	Type	Size	Notes	Fig
	MEMCS16#							
t11a	MEMCS16# Driven Active from LA[23:17] Valid		94	ns	M	16		27
t11b	MEMCS16# Inactive from LA[23:17] Valid		91	ns	M	8		26,27
t11c	MEMCS16# Valid Hold from LA[23:17] Invalid	0		ns	M	16		27
t11d	MEMCS16# Driven Active from SA[19:2] Valid		35	ns	M	16		27
	IOCS16#							
t12a	IOCS16# Driven Active from Valid SA[19:0]		123	ns	I/O	16		29
t12b	IOCS16# Inactive from Valid SA[19:0]		91	ns	I/O	8		28,29
t12c	IOCS16# Valid Hold from SA[19:0] Invalid	0		ns	I/O	16		29
t12d	IOCS16# Driven Active from IOx Active		75	ns	I/O	16		29
	ZEROWS#							
t13a	ZEROWS# Driven Active from MEMx# Active		27	ns	M	16		27
t13b	ZEROWS# Driven Active from MEMx#, IOx# Active		80	ns	M,I/O	8		26,28
t13c	ZEROWS# Driven Active from LA[23:17] Valid		180	ns	M	16		27
t13d	ZEROWS# Driven Active from LA[23:17] Valid		300	ns	M	8		26
t13e	ZEROWS# Driven Active from SA[19:0], SBHE# Valid		80	ns	M	16		27
t13f	ZEROWS# Driven Active from SA[19:0], SBHE# Valid		200	ns	M,I/O	8		26,28
	AEN							
t14a	AEN Valid Setup to IOx# Driven Active	111		ns	I/O	8,16		28,29
t14b	AEN Valid Setup to BALE Driven Inactive	111		ns	I/O	8,16		28,29
t14c	AEN Valid Hold from IOx# Driven Inactive	41		ns	I/O	8,16		28,29
	IOCHRDY							
t15a	IOCHRDY Driven Valid from MEMx#, IOx# Active		78	ns	M,I/O	16		27,29
t15b	IOCHRDY Driven Valid from MEMx#, IOx# Active		366	ns	M,I/O	8		26,28
t15e	IOCHRDY Inactive Pulse Width	120	15.6	ns	M,I/O	8,16		26,28,29

ISA Bus and X-Bus AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C) (Continued)

Symbol	Parameter	Min	Max	Units	Type	Size	Notes	Fig
	IB AS SLAVE TIMINGS							
	LA[23:17]							
t16a	LA[23:17] Valid Setup to MEMx# Active	104		ns	M	16		30
t16b	LA[23:17] Invalid from MEMx# Active	28		ns	M	16		30
	SA[19:0],SBHE#							
t17a	SA[19:0],SBHE# Setup to MEMx# Active	23		ns	M	16		30
t17b	SA[19:0],SBHE# Setup to IOx# Active	89		ns	I/O	8		31
t17c	SA[19:0],SBHE# Valid Hold from MEMx#, IOx# Inactive	30		ns	M,I/O	8,16		30,31
	MEMR#, MEMW#, IOR#, IOW#							
t18a	MEMx# Active Pulse Width	214		ns	M	16		30
t18b	IOx# Active Pulse Width	509		ns	I/O	8		31
t18c	MEMx# Inactive Pulse Width	92		ns	M	16		30
t18d	IOx# Inactive Pulse Width	152		ns	I/O	8		31
	Read Data							
t19a	Read Data Valid from IOCHRDY Active		69	ns	M,I/O	8,16		30,31
t19b	Read Data Valid from IOR# Active		69	ns	I/O	8	11	31
t19c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8,16		30,31
t19d	Read Data Tri-State from MEMR#, IOR# Inactive		30	ns	M,I/O	8,16		30,31
	Write Data							
t20a	Write Data Valid Setup to MEMW#, IOW# Active	−54		ns	M,I/O	8,16		30,31
t20b	Write Data Valid Hold from MEMW#, IOW# Inactive	14		ns	M,I/O	8,16		30,31
	MEMCS16#							
t21a	MEMCS16# Driven Active from Valid LA[23:17]		65	ns	M	16		30
t21b	MEMCS16# Float from Valid LA[23:17]		31	ns	M	16		30
t21c	MEMCS16# Valid Hold from LA[23:17] Invalid	0		ns	M	16		30
	IOCHRDY							
t22a	IOCHRDY Inactive from MEMx#, IOx# Active		25	ns	M,I/O	8,16		30,31
t22b	IOCHRDY Float from IOCHRDY Rising		70	ns	M,I/O	8,16	4	30,31
t22c	IOCHRDY Inactive Pulse Width	120	2.5	μs	M,I/O	8,16		30,31

ISA Bus and X-Bus AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C) (Continued)

Symbol	Parameter	Min	Max	Units	Type	Size	Notes	Fig
	INTERRUPT AND NMI TIMINGS							
	NMI Timing							
t23a	SERR#, IOCHK# Active to NMI Driven Active		200	ns				32
	Interrupt Timing							
t24a	IRQ Inactive Pulse Width	100		ns				33
	ISA BUS MASTER TIMINGS							
	DACK#							
t26a	DACK# Inactive from DREQ Inactive	240		ns				34
	Tri-Stating and Driving the Bus							
t27a	IB Tri-States Address, Data, and Control Signals from DACK# Active	0	30	ns				34
t27b	IB Drives Address, Data, and Control Signals from DACK# Inactive	71		ns				34
	SMEMR# and SMEMW#							
t28a	SMEMR# & SMEMW# Valid from MEMR# and MEMW# Valid		20	ns				34
	DATA SWAP LOGIC TIMING (ISA Master to ISA Slave)							
t29a	SD[7:0] to SD[15:8] Propagation Delay		15	ns				35
t29b	SD[15:8] to SD[7:0] Propagation Delay		15	ns				35
t29c	IB Drives Data Bus from IOR#, IOW#, MEMR# or MEMW# Active		20	ns			2	35
t29d	IB Tri-States Bus from IOR#, MEMR#, or SMEMR# Inactive	5	20	ns			2,3	35
t29e	IB Tri-States Bus from IOW#, MEMW#, or SMEMW# Inactive	15	60	ns			2,3	35
	DMA COMPATIBLE TIMINGS							
	DREQ							
t30a	DREQ Active Hold from IOR# Active		558	ns			5	37
t30b	DREQ Active Hold from IOW# Active		315	ns			5	36
	DACK#							
t31a	DACK# Active to IOR# Active	73		ns				37
t31b	DACK# Active to IOW# Active	312		ns				36
t31c	DACK# Active Hold from IOR# Inactive	105		ns				37
t31d	DACK# Active Hold from IOW# Inactive	161		ns				36

ISA Bus and X-Bus AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C) (Continued)

Symbol	Parameter	Min	Max	Units	Type	Size	Notes	Fig
	AEN and BALE							
t32a	AEN Active to IOx# Active	111		ns				36,37
t32b	AEN and BALE Inactive from IOx# Inactive	41		ns				36,37
	LA[23:19], SA[19:0], SBHE#							
t33a	LA[23:19],SA[19:0], SBHE# Valid Setup to MEMx# Active	99		ns				36,37
t33b	LA[23:19],SA[19:0], SBHE# Valid Hold from MEMx# Inactive	51		ns				36,37
	MEMR#, MEMW#, IOR#, IOW#							
t34a	IOW# and MEMW# Active Pulse Width	474		ns				36,37
t34b	MEMR# Active Pulse Width	520		ns				36
t34c	IOR# Active Pulse Width	769		ns				37
t34d	IOW# Inactive Pulse Width (continuous)	469		ns				36
t34e	IOR# Inactive Pulse Width (continuous)	167		ns				37
t34f	IOR# Active to MEMW# Active	235		ns				37
t34g	MEMR# Active to IOW# Active	0		ns				36
t34h	MEMR# Active Hold from IOW# Inactive	50		ns				36
t34i	IOR# Active Hold from MEMW# Inactive	50		ns				37
t34j	MEMx# Active Hold from IOCHRDY Active	120		ns				36,37
	SMEMR# and SMEMW#							
t35a	SMEMR# and SMEMW# Valid from MEMR# and MEMW# Valid		5	ns				36,37
	Read Data							
t36a	Read Data Valid from IOR# Active		237	ns				37
t36b	Read Data Valid Hold from IOR# Inactive	0		ns				37
t36c	Read Data Float from IOR# Inactive		61	ns				37
	Write Data							
t37a	Write Data Valid Setup to IOW# Inactive	252		ns				36
t37b	Write Data Valid Hold from IOW# Inactive	36		ns				36

ISA Bus and X-Bus AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C) (Continued)

Symbol	Parameter	Min	Max	Units	Type	Size	Notes	Fig
	DATA SWAP LOGIC TIMING (ISA to ISA Transaction)							
t38a	SD[7:0] to SD[15:8] Propagation Delay		15	ns				38
t38b	SD[15:8] to SD[7:0] Propagation Delay		15	ns				38
t38c	IB Drives Data Bus from IOR# or MEMR# Active		20	ns			2	38
t38d	IB Tri-States Bus from IOR# or MEMR# Inactive		20	ns			2	38
	TC							
t39a	TC Active Setup to IOx# Inactive	511		ns			6	36,37
t39b	TC Active Hold from IOx# Inactive	71		ns			6	36,37
t39h	TC Pulse Width	700		ns				36,37
	IOCHRDY							
t40b	IOCHRDY Valid from MEMx# Active		315	ns				36,37
t40c	IOCHRDY Inactive Pulse Width	125		ns				36,37
	ISA REFRESH TIMINGS							
	REFRESH#							
t62a	REFRESH# Active Setup to MEMR# Active	120		ns				39,40
t62b	REFRESH# Active Hold from MEMR# Inactive	31	218	ns				39,40
t62c	REFRESH# Driven Active to SA[15:0] Valid	11		ns				39,40
t62d	REFRESH# Active Hold from SA[15:0] Invalid	11		ns				39,40
	AEN							
t63a	AEN Driven Active to MEMR# Active	11		ns				39,40
t63b	AEN Hold from MEMR# Inactive	11		ns				39,40
	SA[15:0]							
t64a	SA[15:0] Valid Setup to MEMR# Active	81		ns				39,40
t64b	SA[15:0] Valid Hold from MEMR# Inactive	36		ns				39,40
t64c	SA[15:0] Valid Float from MEMR# Inactive	45	120	ns			8	40

ISA Bus and X-Bus AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C) (Continued)

Symbol	Parameter	Min	Max	Units	Type	Size	Notes	Fig
	MEMR#, SMEMR#							
t65a	MEMR# Active Pulse Width	225		ns				39,40
t65b	MEMR# Tri-state from MEMR# Inactive	45	120	ns				39,40
t65c	MEMR# Driven Inactive from IOCHRDY Active	120		ns				39,40
t65d	SMEMR# Propagation Delay from MEMR#		5	ns				39,40
	IOCHRDY							
t66a	IOCHRDY Inactive from MEMR# Active		76	ns				39,40
t66b	IOCHRDY Valid from MEMR# Active		76	ns				39,40
t66c	IOCHRDY Active to Inactive	120		ns				39,40
	IB Driving Bus from REFRESH#							
t67a	IB Drives Control and Address from REFRESH# Active	5		ns			8	40
	IB AND ISA MASTER ACCESSES TO THE X-BUS							
	BIOSCS#, KBCCS#, and RTCCS#							
t68a	CS# Driven Active from SA[19:0], LA[23:17] Valid		25	ns				41
t68b	CS# Driven Inactive from SA[16:0], LA[23:17] Invalid		25	ns				41
	XBUSTR# and XBUSOE#							
t69a	XBUSTR# Active from IOR#, MEMR# Active		17	ns				41
t69b	XBUSOE# Active from IOx#, MEMx# Active		29	ns				41
t69c	XBUSTR# Active Setup to XBUSOE# Active	3	12	ns				41
t69d	XBUSOE# Inactive from IOx#, MEMx# Inactive	35	60	ns			9	41
t69e	XBUSTR# Inactive from IOR#, MEMR# Inactive	45	100	ns			9	41
t69f	XBUSOE# Setup to XBUSTR# Inactive	10	45	ns			9	41
t69g	XBUSOE# Inactive from SA[16:0] and LA[23:17]		25	ns			10	41
t69h	XBUSTR# Inactive from IOR#, MEMR# Inactive	15	60	ns			10	41

ISA Bus and X-Bus AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C) (Continued)

Symbol	Parameter	Min	Max	Units	Type	Size	Notes	Fig
	DMA ACCESSES TO X-BUS							
	XBUSTR#							
t70a	XBUSTR# Active from DACKx# Active		25	ns			12,14	42
t70b	XBUSTR# Inactive from DACKx# Inactive	10	65	ns			12	42
	MISCELLANEOUS X-BUS TIMINGS							
	Mouse Timing Support							
t71a	IRQ12/M and IRQ1 Minimum Active Pulse Width (for Mouse Function and Keyboard)	180		ns				43
	Coprocessor Error Support							
t73a	IGNNE# Active from IOW# Active from Port F0h Access		220	ns				43
t73b	IGNNE# Inactive from FERR# Inactive		150	ns				43
	Real Time Clock Timing (RTCALE)							
t75a	RTCALE Pulse Width	200	300	ns				44
t75b	RTCALE Active from IOW# Active		70	ns				44
	Speaker Timing							
t76a	SPKR Valid Delay from OSC Rising		200	ns				45

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the byte lane that the data has been swapped to.
3. Data is tri-stated from the standard memory commands (SMEMR# or SMEMW#), when they are generated.
4. This specification includes both the time the IB drives IOCHRDY active and the time it takes the IB to float IOCHRDY.
5. This applies to the last cycle of a demand mode DMA transfer.
6. Output from IB.
7. 36 ns has been added to the ISA spec to meet ZEROWS# setup requirements.
8. This applies to ISA Master initiated refresh only.
9. IB as a master cycles only.
10. ISA master cycles only.
11. This applies to the IB cycles that IOCHRDY is not driven low.
12. This applies to all DACK# signals.
13. 56 ns has been added to the ISA spec to meet MEMCS16# setup requirements. ISA devices are not suppose to use the SA address as part of their MEMCS16# decode. However, some devices do use SA as part of MEMCS16# decode.
14. X-Bus read
15. For back-to-back "sub cycles" generated as a result of byte assembly or disassembly, this spec is 34 ns.

6.3.5 AC TEST LOADS

Table 23. AC Test Loads

Capacitive Load	Signals
200 pF	REFRESH#, TC, SD[15:0], SA[19:0], SBHE#, LA[23:17], I0CS16#, MASTER#, MEMCS16#, MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW#, AEN, BALE, IOCHRDY, ZEROWS#, RSTDRV, SYSCLK
120 pF	DACK#[7:5,3:0]
50 pF	SPKR, INTR, NMI, BIOSCS#, KBCCS#, RTCCS#, RTCALE, XBUSTR#, XBUSOE#, IGNNE#

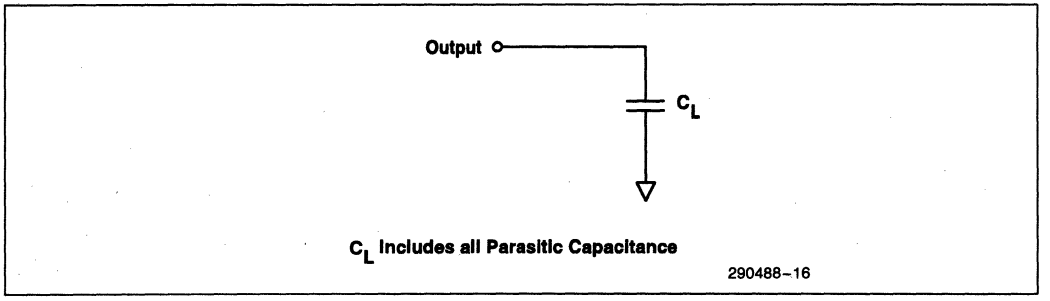


Figure 17. Test Load

6.3.6 AC TIMING WAVEFORMS

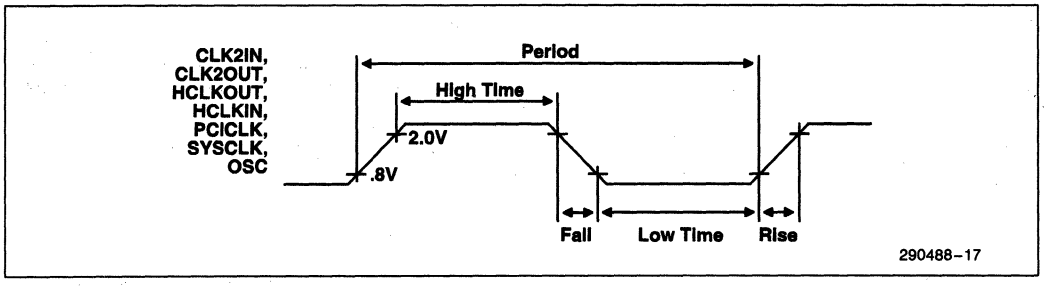


Figure 18. Clock Timing

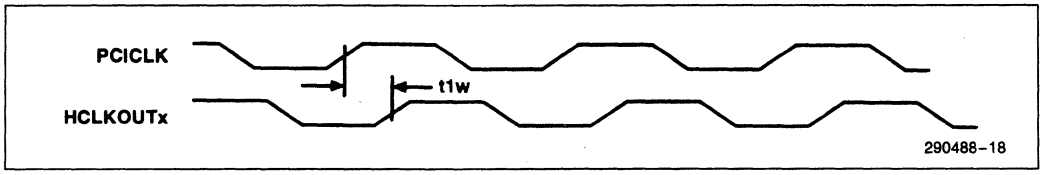


Figure 19. PCICLK-to-HCLKOUT Skew Timing

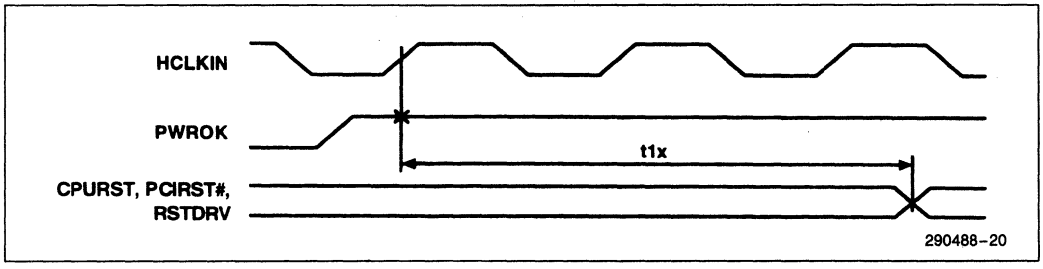


Figure 20. Reset Inactive after PWROK

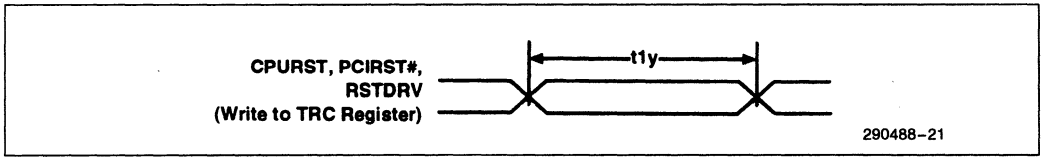


Figure 21. Reset Active Pulse Width

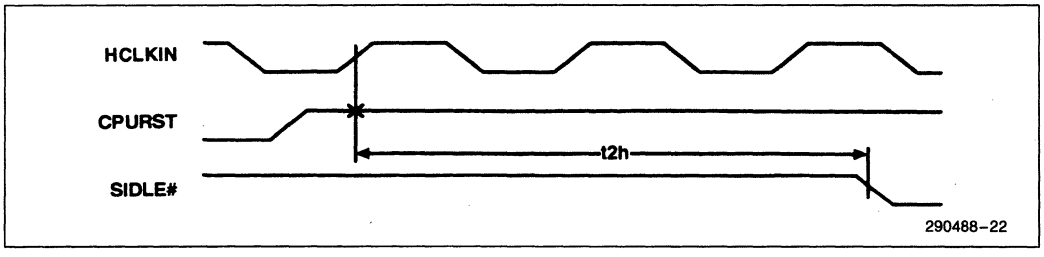


Figure 22. SIDLE# Active after CPURST

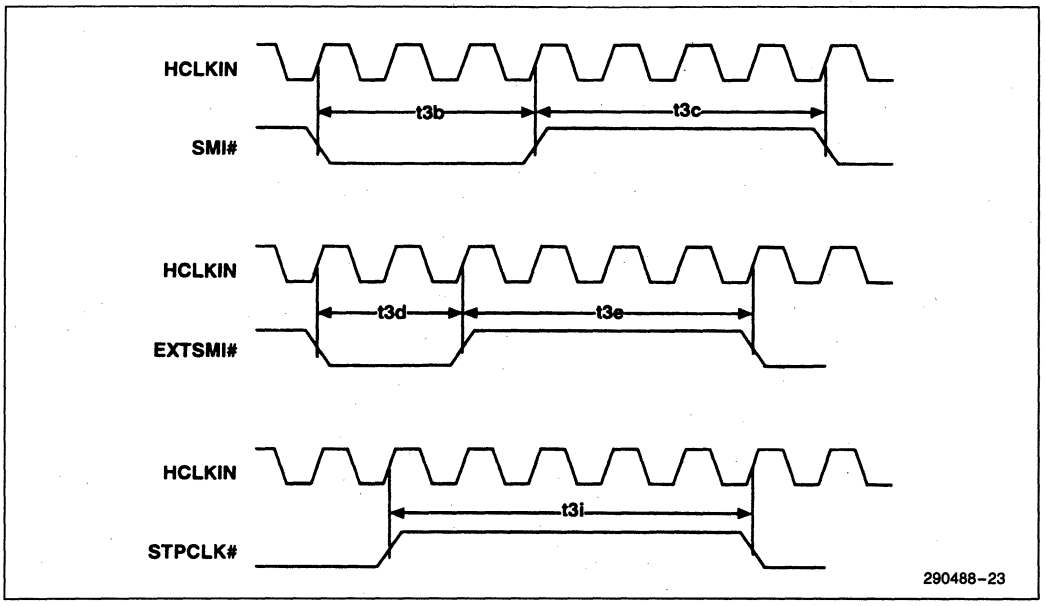


Figure 23. SMI#, EXTSMI#, and STPCLK# Timing

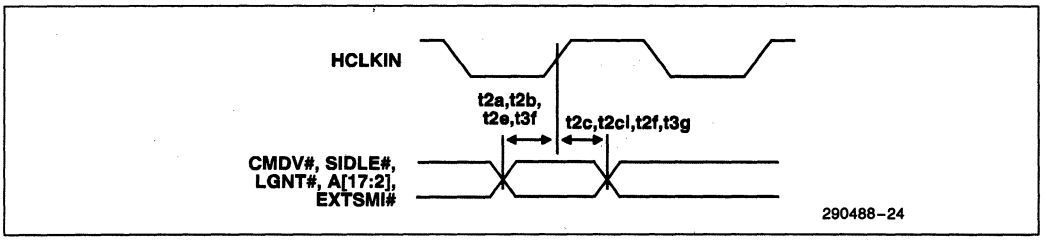


Figure 24. Input to HCLKIN Setup/Hold Times

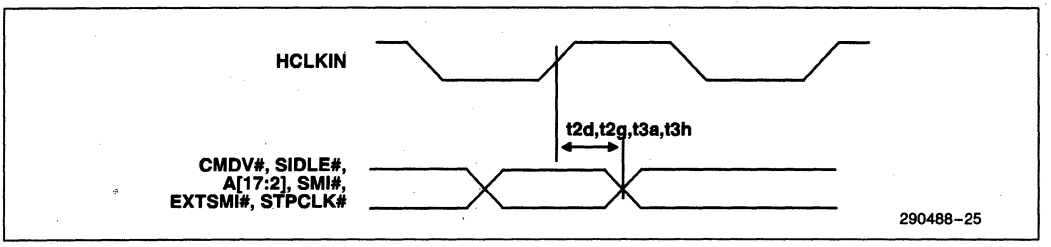


Figure 25. HCLKIN to Output Valid Delay

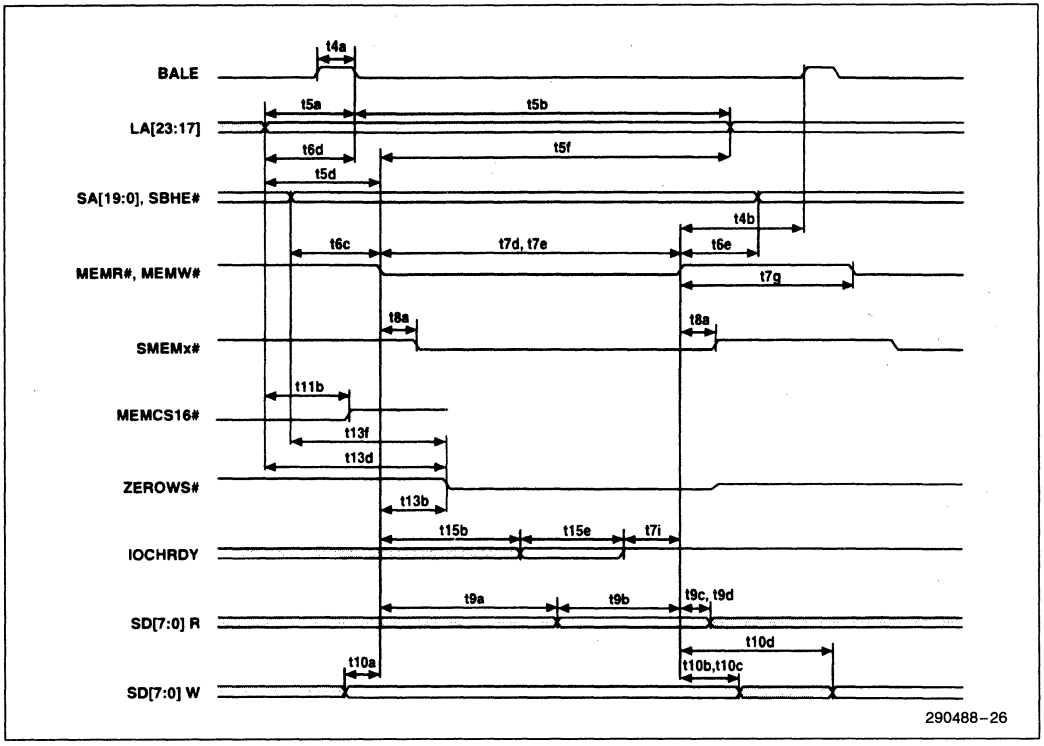


Figure 26. 8-Bit ISA Memory Slave Timing (IB as Master)

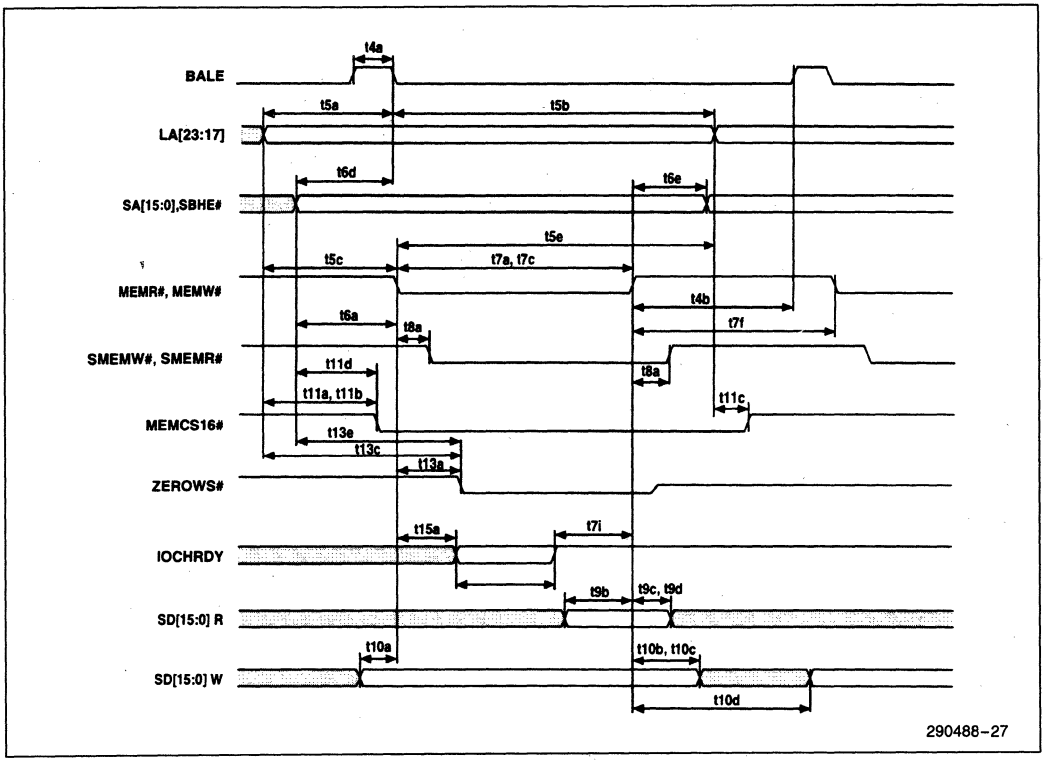


Figure 27. 16-Bit ISA Memory Slave Timing (IB as Master)

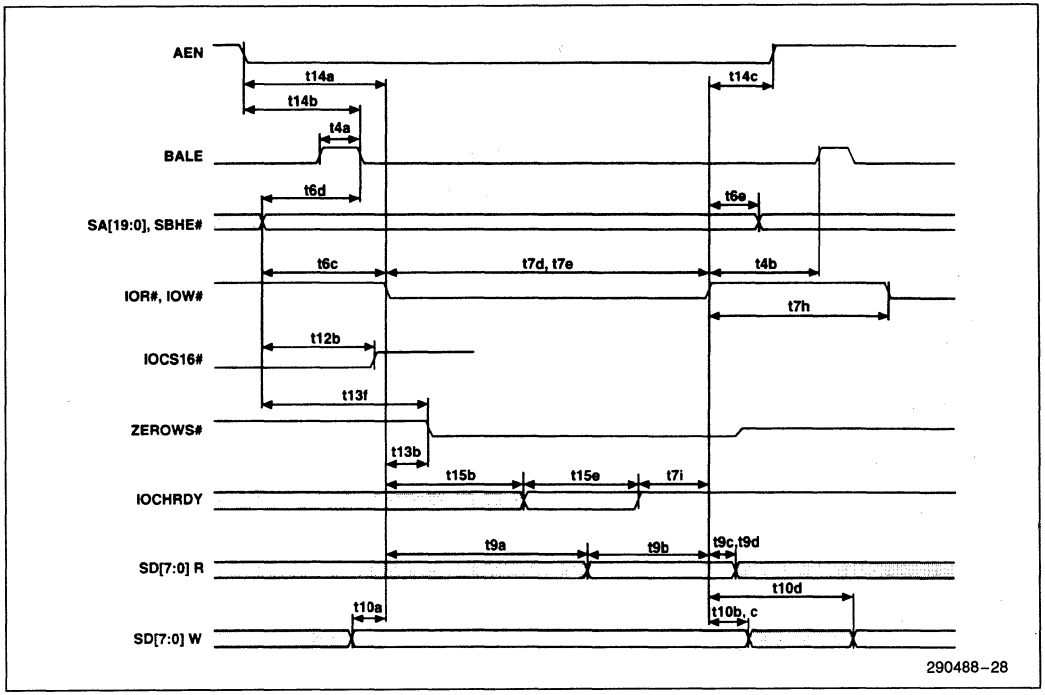


Figure 28. 8-Bit ISA I/O Slave Timing (IB as Master)

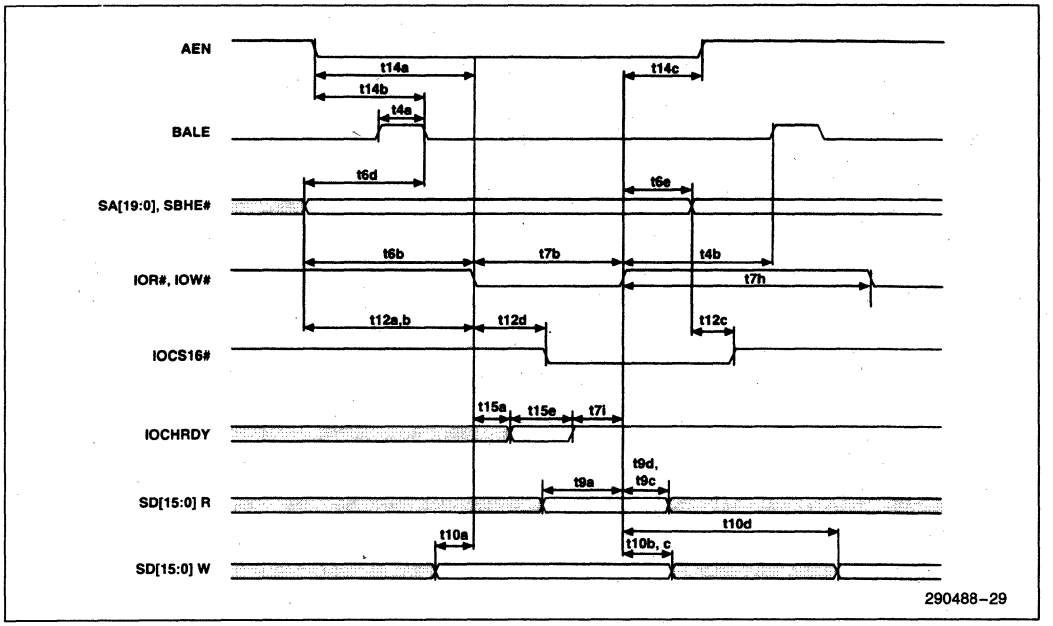


Figure 29. 16-Bit I/O Slave Timing (IB as Master)

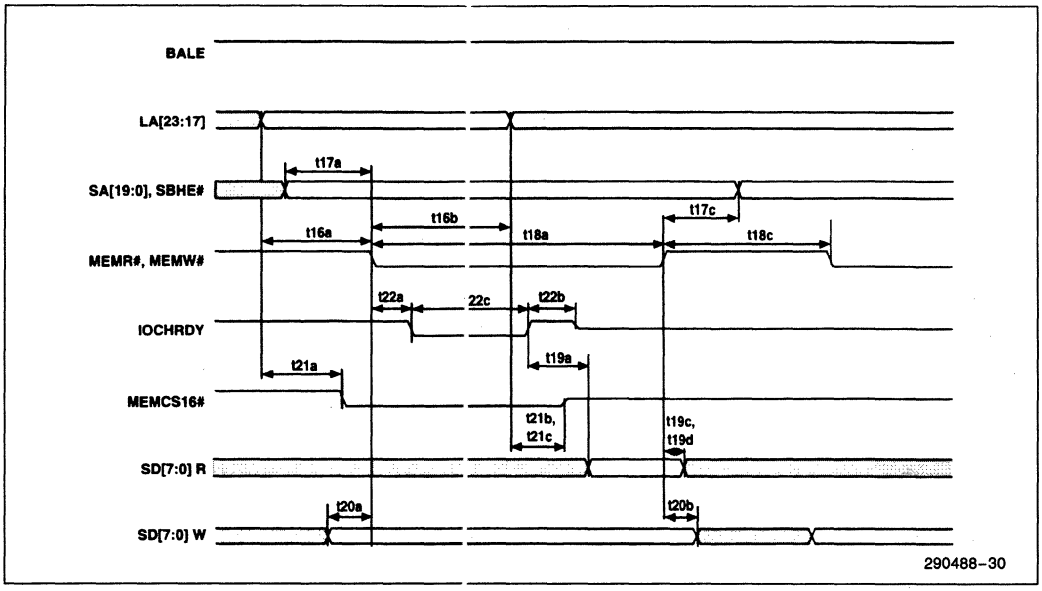


Figure 30. ISA Master Accessing PCI Memory Timing

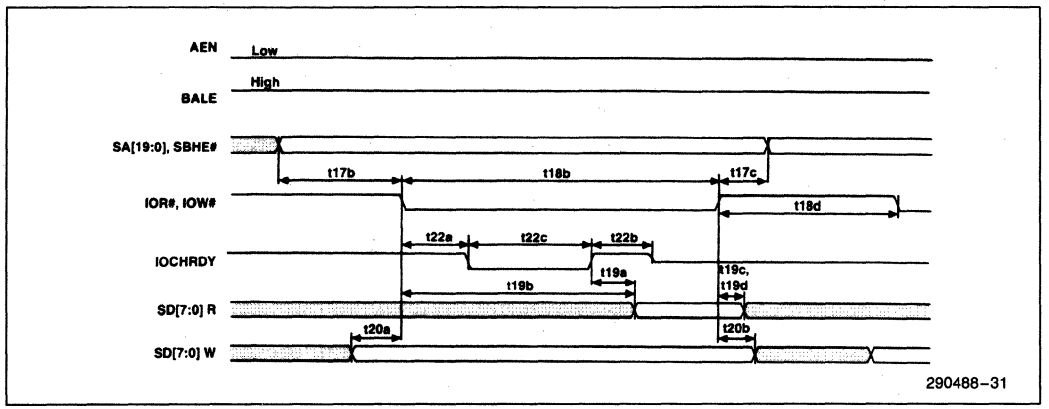


Figure 31. ISA Master Accessing IB Register Timing

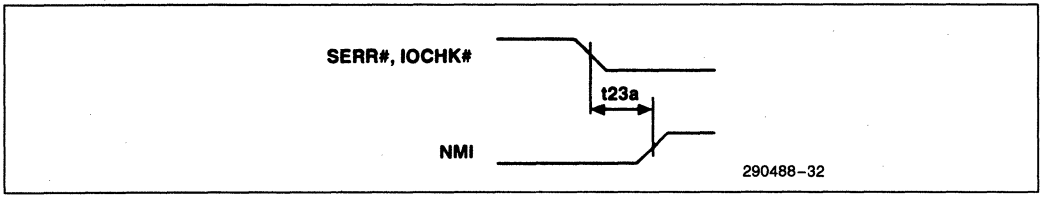


Figure 32. NMI Timing

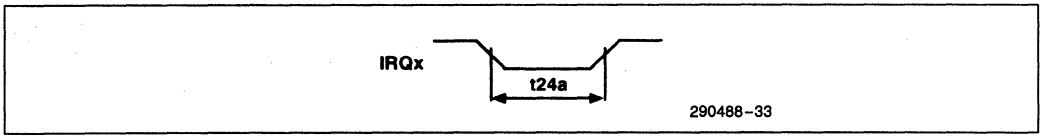


Figure 33. Interrupt Timing

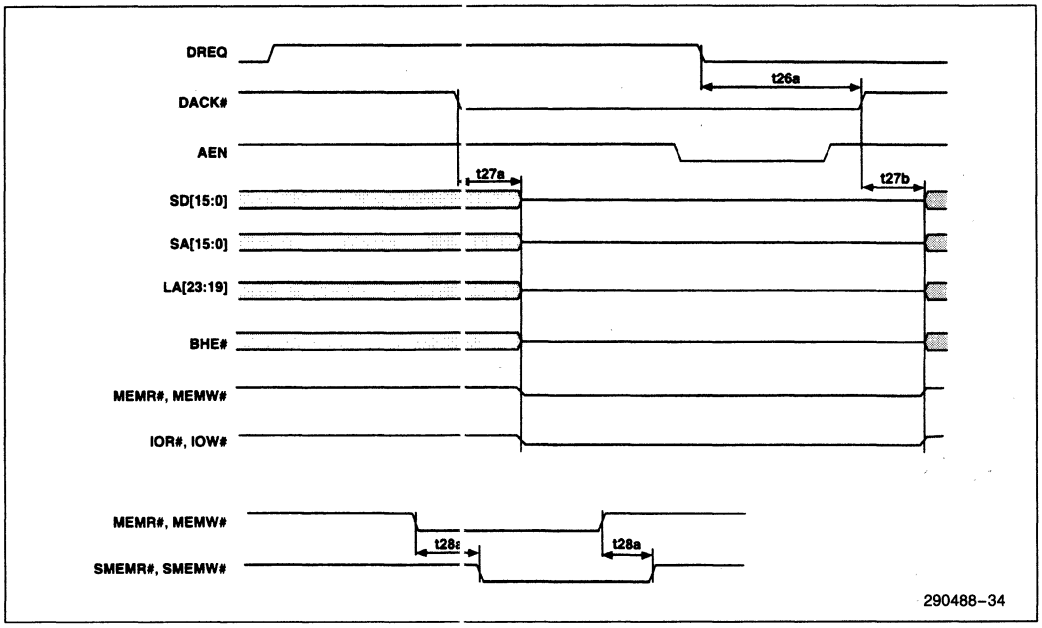


Figure 34. ISA Master Miscellaneous Timing

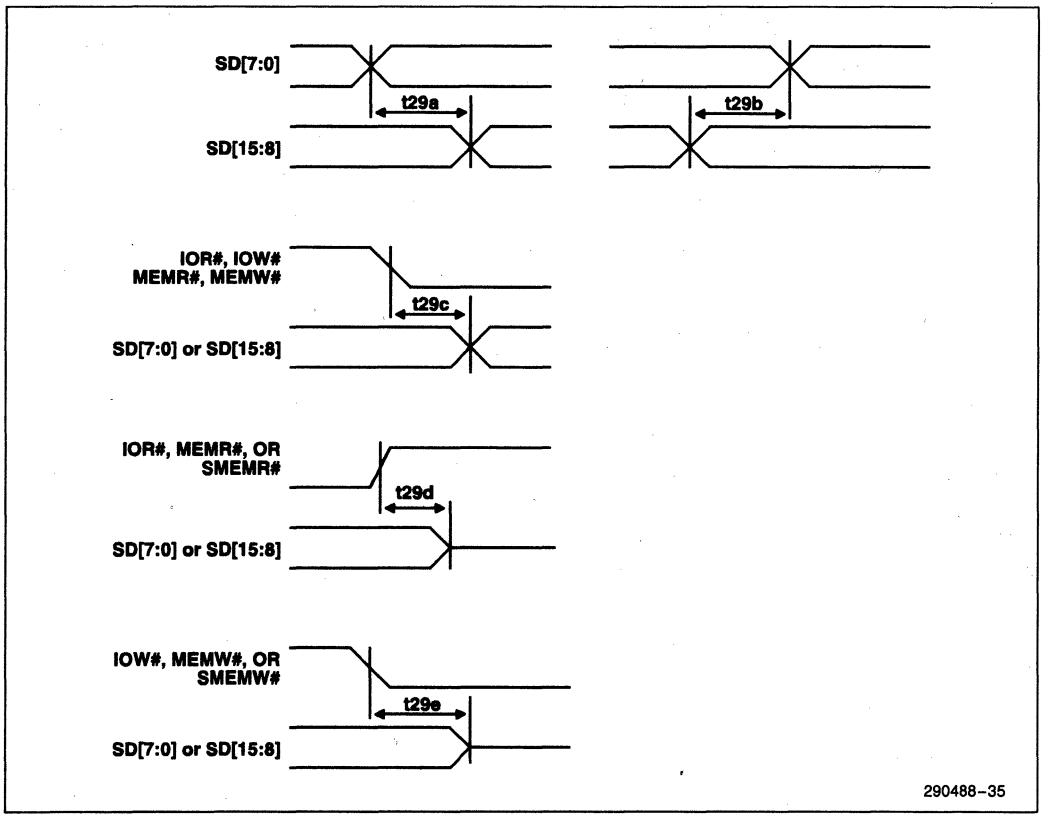


Figure 35. ISA Master Data Swap Timing

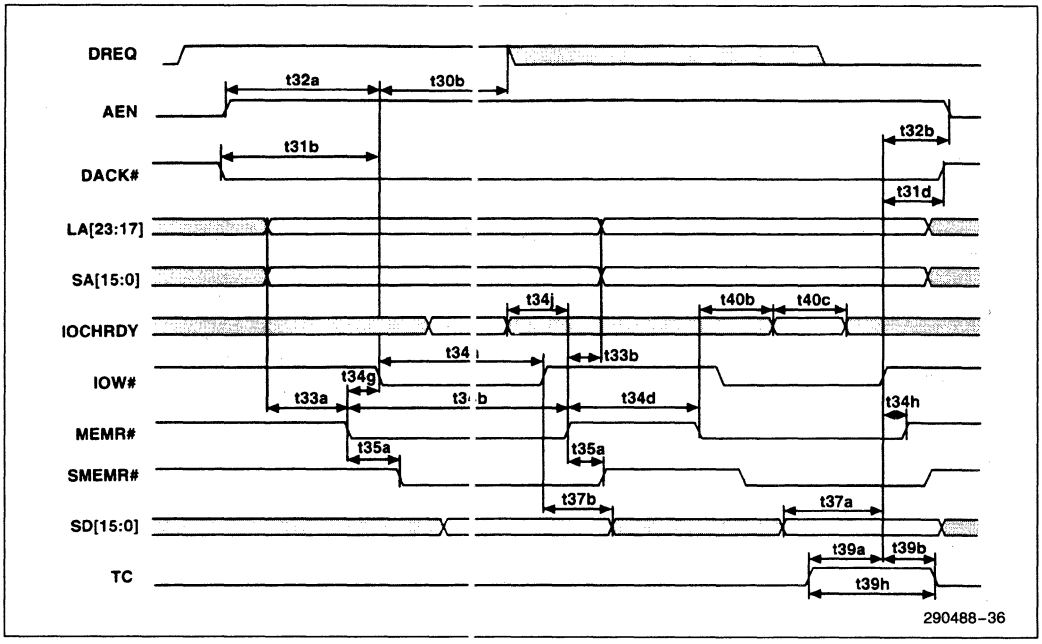


Figure 36. DMA Compatible Timing (Memory Read)

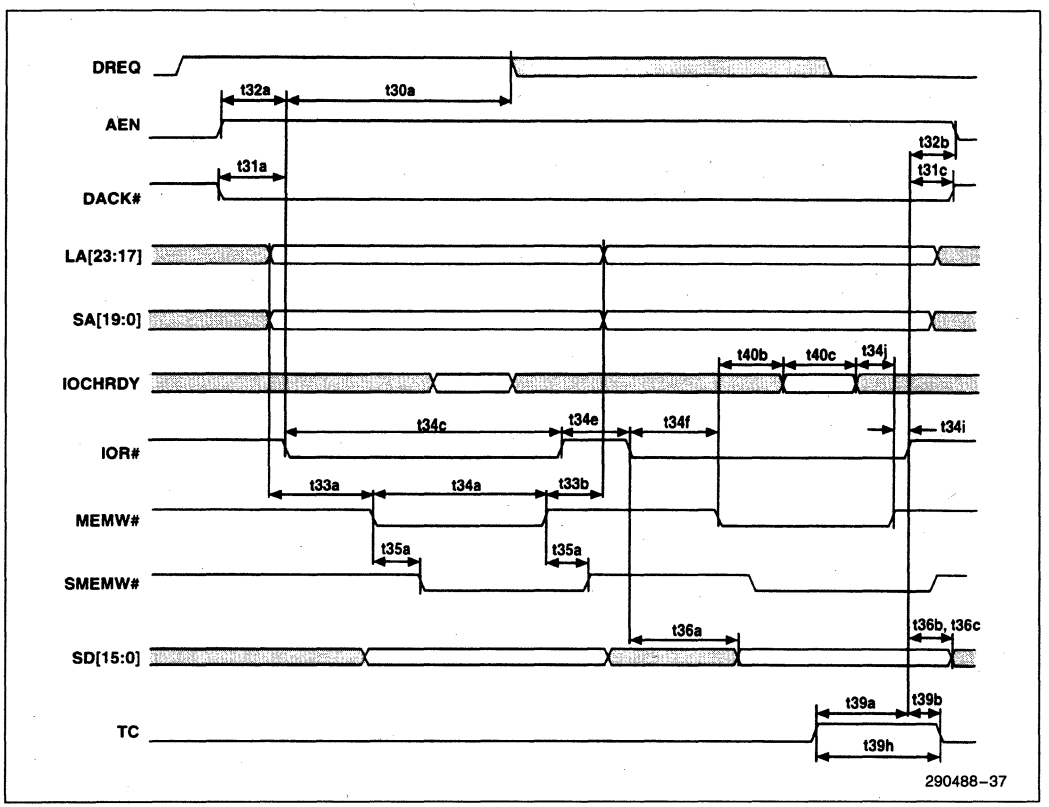


Figure 37. DMA Compatible Timing (Memory Write)

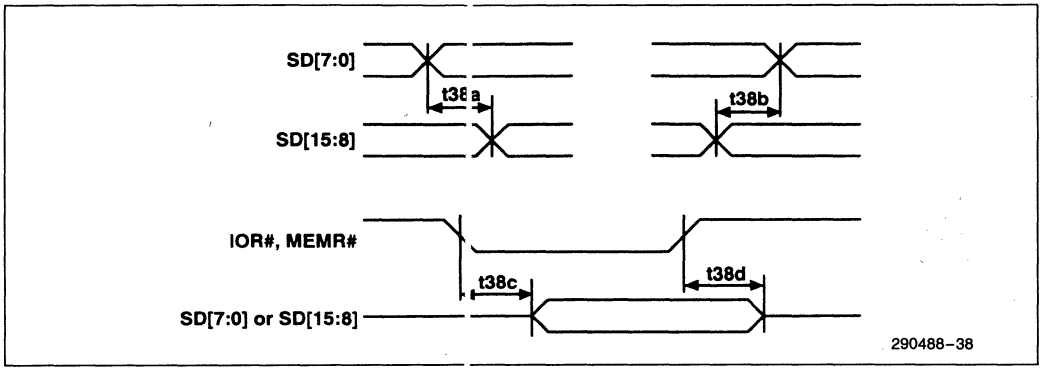


Figure 38. DMA Compatible Timing (Data Swap)

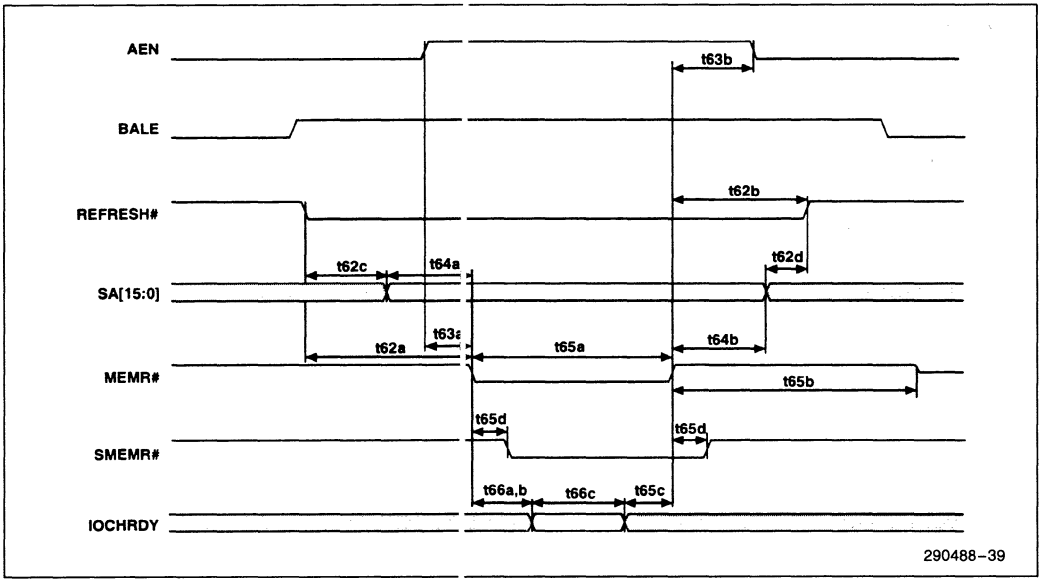


Figure 39. IB Initiated Refresh Timing

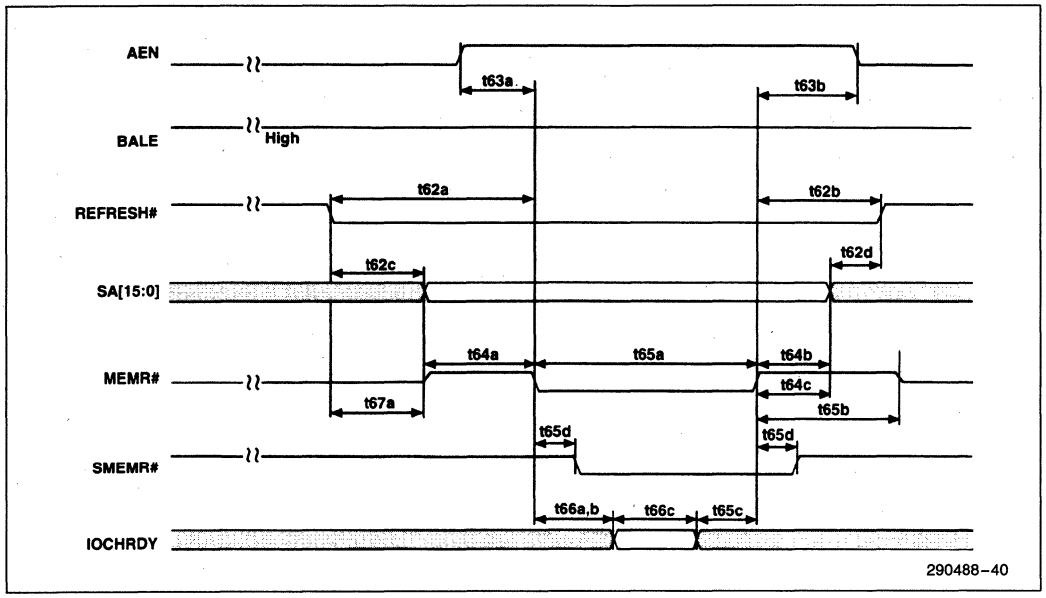


Figure 40. ISA Master-Initiated Refresh Timing

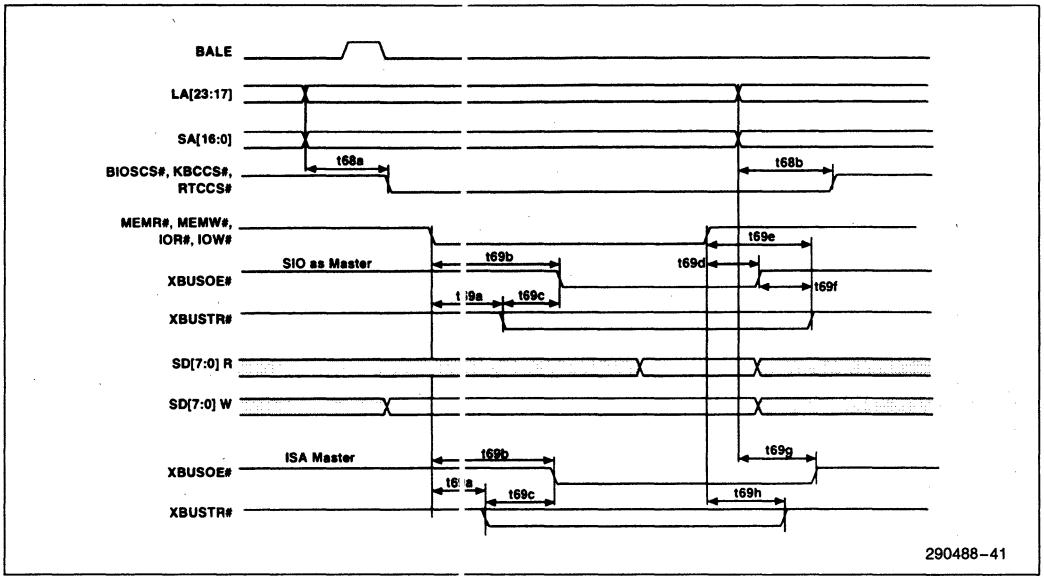


Figure 41. IB and ISA Master Access to X-Bus Timing

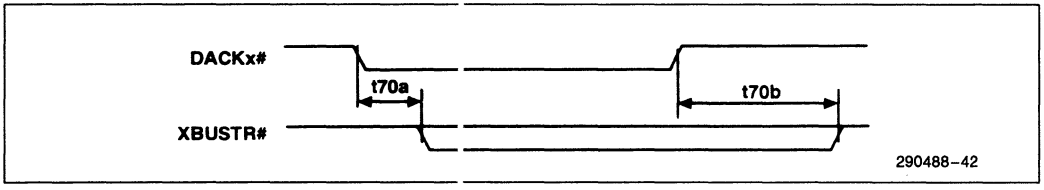


Figure 42. DMA Access to X-Bus Timing

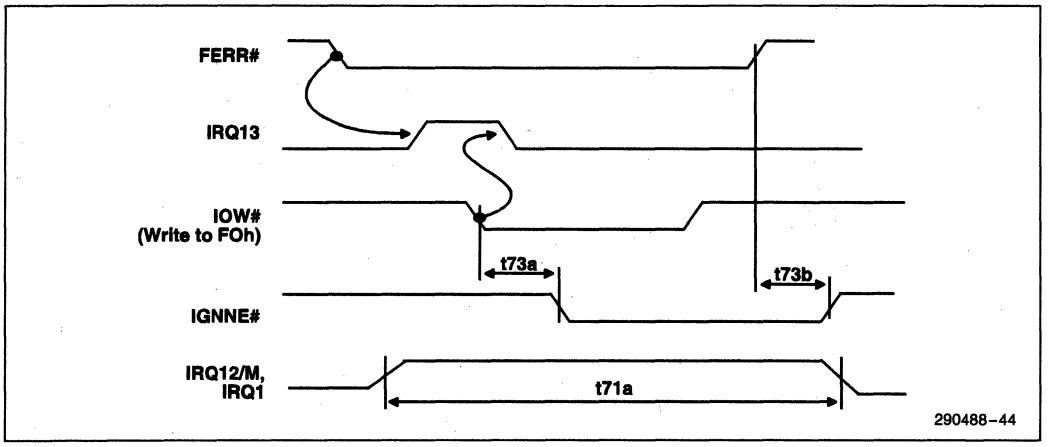


Figure 43. Coprocessor Error and Mouse Support Timing

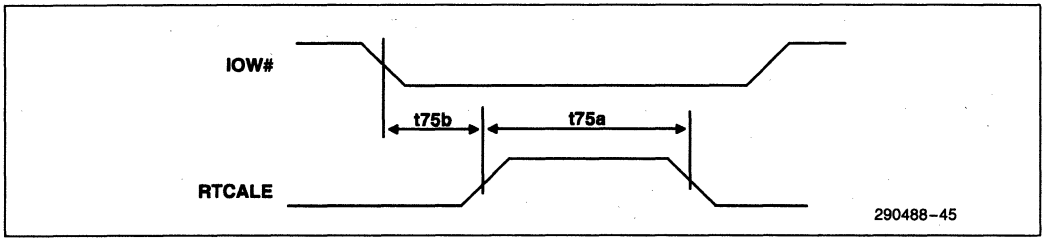


Figure 44. Real Time Clock Timing (RTCALE Generation)

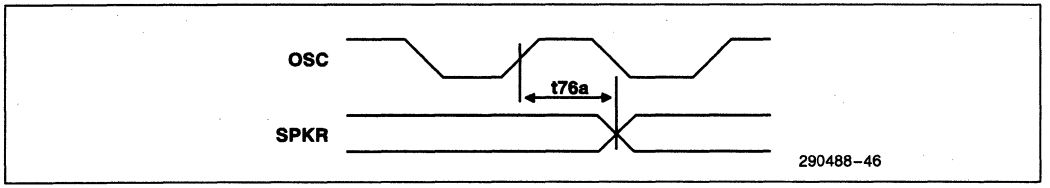


Figure 45. Speaker Timing

6.4 PSC AC Characteristics

This section provides the AC parameters and timing diagrams for the 82425EX PSC.

6.4.1 HOST CLOCK TIMING

AC Characteristics (V_{DD} = 5V ± 5%, T_{CASE} = 0 to 85°C)

Symbol	Parameter	Min	Max	Units	Notes	Fig
t1a	HCLKIN Period Stability		0.1%			
t1b	HCLKIN Period	30.0	40.0	ns		46
t1c	HCLKIN High Time	10.0		ns		46
t1d	HCLKIN Low Time	10.0		ns		46
t1e	HCLKIN Rise Time		2.0	ns		46
t1f	HCLKIN Fall Time		2.0	ns		46
t2a	CLK2IN Period Stability		0.1%			
t2b	CLK2IN Period	15	20.0	ns	Note 1	46

6.4.2 CPU INTERFACE TIMINGS

AC Characteristics (V_{DD} = 5V ±5%, T_{CASE} = 0 to 85 °C)

Symbol	Parameter	Min	Max	Units	Notes	Fig
t10a	HITM#, PCD, HLDA, BE[3:0], SMIACT#, SMI# Setup Time to HCLKIN Rising	10.0		ns		49
t10a1	ADS#, BLAST# Setup Time to HCLKIN Rising	12.0		ns		49
t10b	W/R#, M/IO#, D/C# Setup Time to HCLKIN Rising	14.0		ns		49
t10c	ADS#, HITM#, W/R#, M/IO#, D/C#, PCD, HLDA, BLAST#, BE[3:0]#, SMIACT#, SMI#, HLDA Hold Time from HCLKIN Rising	2.0		ns		49
t11a	HD[31:0], HDP[3:0] Setup Time to HCLKIN Rising	10.0		ns		49
t11b	HD[31:0], HDP[3:0] Hold Time from HCLKIN Rising	2.0		ns		49
t11c	HD[31:0], HDP[3:0] Output Enable from HCLKIN Rising	0.0	12.0	ns		51

AC Characteristics (V_{DD} = 5V ±5%, T_{CASE} = 0 to 85 °C) (Continued)

Symbol	Parameter	Min	Max	Units	Notes	Fig
t11d	HD[31:0], HDP[3:0] Valid Delay from HCLK Rising	3.0	14.0	ns		48
t11e	HD[31:0], HDP[3:0] Float Delay from HCLKIN Rising	0.0	12.0	ns		50
t12a	A[31,26:2] Setup Time to HCLKIN Rising	12.0		ns		49
t12b	A[31,26:2] Hold Time from HCLKIN Rising	2.0		ns		49
t12c	A[31,26:2] Output Enable from HCLKIN Rising	0.0	14.0	ns		51
t12d	A[31,26:2], BE[3:0]#, W/R# Valid Delay from HCLKIN Rising	3.0	14.0	ns		48
t12e	A[31,26:2], BE[3:0]#, W/R# Float Delay from HCLKIN Rising	0.0	12.0	ns		50
t13a	RDY#, BRDY# Rising Edge Valid Delay from HCLKIN Rising	3.0	16.0	ns		48
t13b	RDY#, BRDY# Falling Edge Valid Delay from HCLKIN Rising	3.0	16.0	ns		48
t14	AHOLD Valid Delay from HCLKIN Rising	3.0	11.0	ns		48
t15	EADS#, CPURST, HOLD Valid Delay from HCLKIN Rising	3.0	13.0	ns		49
t15a	KEN# Valid Delay from HCLKIN Rising	3.0	22.0	ns		48
t16a	INIT/SRESET High Pulse Width	16		HCLK		52
t16b	INIT/SRESET Valid Delay from HCLKIN Rising	3.0	13.0	ns		48
t17a	CPURST Setup Time to HCLKIN Rising	10.0		ns	Note 1	49
t17b	CPURST Hold Time to HCLKIN Rising	2.0		ns	Note 1	49
t17c	CPURST Pulse Width	3		HCLK	Note 2	52
t18a	LDEV# Setup Time to HCLKIN Rising	7.0				49
t18b	LDEV# Hold Time to HCLKIN Rising	2.0				49
t18c	LRDY# Early Setup Time to HCLKIN Rising	15.0				49
t18d	LRDY# Late Setup Time to HCLKIN Rising	7.0				49
t18e	LRDY# Hold Time to HCLKIN Rising	2.0				49
t18f	LRDY# to RDY# Propagation Delay	0.0	11.0			47

NOTES:
1. Synchronous Reset
2. Asynchronous Reset

6.4.3 SECOND LEVEL CACHE TIMING

AC Characteristics (V_{DD} = 5V ±5%, T_{CASE} = 0 to 85 °C)

Symbol	Parameter	Min	Max	Units	Notes	Fig
t20a	CI3E/CI3O2 Propagation Delay from A3	0.0	9.0	ns		53
t20b	CI3E/CI3O2 Valid Delay from HCLKIN Rising	3.0	13.0	ns		48
t21a	COE[1:0]# Falling Edge Valid Delay from HCLKIN Rising	3.0	13.0	ns		48
t21b	COE[1:0]# Rising Edge Valid Delay from HCLKIN Rising	3.0	13.0	ns		48
t22a	CWE[1:0]# Falling Edge Valid Delay from HCLKIN Rising	3.0	12.0	ns		48
t22b	CWE[1:0]# Rising Edge Valid Delay from HCLKIN Rising	3.0	13.0	ns		48
t22c	CWE[1:0]# Low Pulse Width	14.0		ns		52
t23	TWE# Valid Delay from HCLKIN Rising	3.0	14.0	ns		48
t24a	TAG[8:0] Valid Delay from HCLK	3.0	17.0	ns		
t24b	TAG[8:0] Setup Time to HCLKIN Rising	4.0		ns		49
t24c	TAG[8:0] Hold Time to HCLKIN Rising	7.0		ns		49

6.4.4 DRAM INTERFACE TIMING

AC Characteristics (V_{DD} = 5V ±5%, T_{CASE} = 0 to 85 °C)

Symbol	Parameter	Min	Max	Units	Notes	Fig
t30a	RAS[4:0]# Valid Delay from HCLKIN Rising	3.0	13.0	ns		48
t30b	RAS[4:0]# Pulse Width High	4		HCLK −5 ns		52
t31a	CAS[7:0]# Valid Delay from HCLKIN Rising	3.0	11.0	ns		48
t31b	CAS[7:0]# Pulse Width High	1		HCLK −2 ns		52
t32	WE# Valid Delay from HCLKIN Rising	3.0	17.0	ns		48
t33a	MA[10:0] Propagation Delay from A[26:5]	0.0	10.0	ns		53
t33b	MA[10:0] Row to Column Switching Delay	0.0	19.0	ns		53
t33c	MA[10:0] Valid Delay from HCLKIN Rising	3.0	15.0	ns		48

6.4.5 PCI TIMING

AC Characteristics (V_{DD} = 5V ±5%, T_{CASE} = 0 to 85 °C)

Symbol	Parameter	Min	Max	Units	Notes	Fig
	PCI Clock Timing					
t41a	Period	30.0		ns		46
t41b	PCLKIN High Time	8.0		ns		46
t41c	PCLKIN Low Time	8.0		ns		46
t41d	PCLKIN Rise Time		3.0	ns		46
t41e	PCLKIN Fall Time		3.0	ns		46
	PCI Interface Timing					
t50a	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, SERR#, DEVSEL# Valid Delay from PCLKIN Rising	2.0	11.0	ns		48
t50b	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, SERR#, DEVSEL# Output Enable Delay from PCLKIN Rising	2.0		ns		
t50c	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, SERR#, DEVSEL# Float Delay from PCLKIN Rising		28.0	ns		
t50d	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, SERR#, DEVSEL# Setup Time to PCLKIN Rising	7.0		ns		49
t50e	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, SERR#, DEVSEL# Hold Time from PCLKIN Rising	0.0		ns		49
t51a	AD[31:0] Setup Time to PCLKIN Rising	7.0		ns		49
t51b	AD[31:0] Hold Time to PCLKIN Rising	0.0		ns		49
t51c	AD[31:0] Valid Delay from PCICLK	2.0	11.0	ns		53
t52a	PREQ0, PREQ1/LDEV# Setup Time to PCLKIN	12.0		ns		49
t52b	PREQ0, PREQ1/LDEV# Hold Time to PCLKIN	2.0		ns		49
t52c	PGNT1, PGNT0 Valid Delay from PCLKIN	2.0	12.0	ns		48
t53a	PWRGOOD Setup Time to HCLKIN Rising	7.0		ns		49
t53b	PWRGOOD Hold Time to HCLKIN Rising	2.0		ns		49

6.4.6 PSC/IB LINK INTERFACE TIMING

AC Characteristics (V_{DD} = 5V ±5%, T_{CASE} = 0 to 85 °C)

Symbol	Parameter	Min	Max	Units	Notes	Fig
t60a	CMDV#, SIDLE# Valid Delay from HCLKIN Rising	3.0	13.0	ns		48
t60b	CMDV#, SIDLE# Setup Time to HCLKIN Rising	11.0		ns		49
t60c	CMDV#, SIDLE# Hold Time to HCLKIN Rising	1.0		ns		49
t61a	LREQ Setup Time to HCLKIN Rising	10.0		ns		49
t61b	LREQ Hold Time to HCLKIN Rising	1.0		ns		49
t62	LGNT Valid Delay from HCLKIN Rising	3.0	13.0	ns		48

6.4.7 PCI BUS IDE TIMING

AC Characteristics (V_{DD} = 5V ±5%, T_{CASE} = 0 to 85 °C)

Symbol	Parameter	Min	Max	Units	Notes	Fig
t70	LBIDE#, IDE1CS#, IDE3CS#, DIR, IOR#, IOW# Valid Delay from PCLKIN Rising	2.0	12.0	ns		48
t71a	IORDY Falling Setup Time to HCLKIN Rising	18.0		ns		49
t71a1	IORDY Rising Setup Time to HCLKIN Rising	8.0		ns		49
t71b	IORDY Hold Time to HCLKIN Rising	2.0		ns		49
t72	IDEA[2:0] Valid Delay from PCLKIN Rising	2.0	12.0	ns		48
t73a	IDED[15:0] Valid Delay from PCLKIN Rising	2.0	12.0	ns		48
t73b	IDED[15:0] Setup Time to HCLKIN Rising	8.0		ns		49
t73c	IDED[15:0] Hold Time to HCLKIN Rising	2.0		ns		49

6.4.8 AC TEST LOADS

Table 24. AC Test Loads

Capacitive Load	Pin
0 pF	RAS[3:0]#, CAS[7:0]#, WE#, MA[10:0]
0 pF	HD[31:0], HDP[3:0], A[31:30,26:2], RDY#, BRDY#, BOFF#, AHOLD, EADS#, INV, KEN#, CPURST, HOLD, A20M#, CI3E, CI3O2, COE[1:0]#, CWE[1:0]#, TWE#, TAG[8:0], CMDV#, SIDLE#, LGNT, PGNT1, PGNT0, LBIDE#, IDE1CS#, IDE3CS#, DIR, IOR#, IOW#

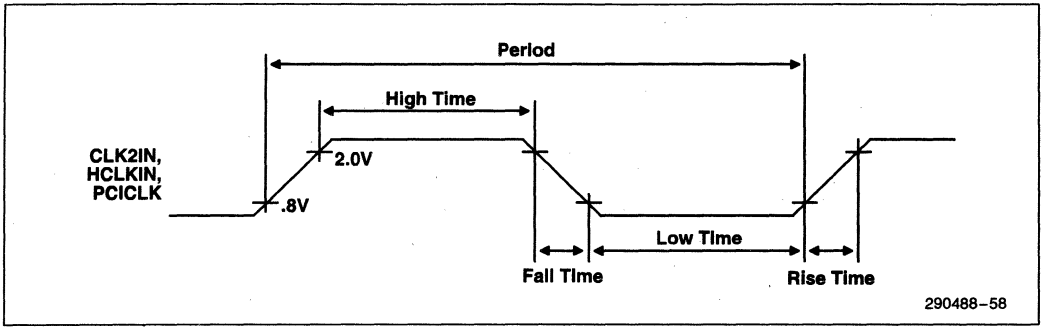


Figure 46. Clock Timing

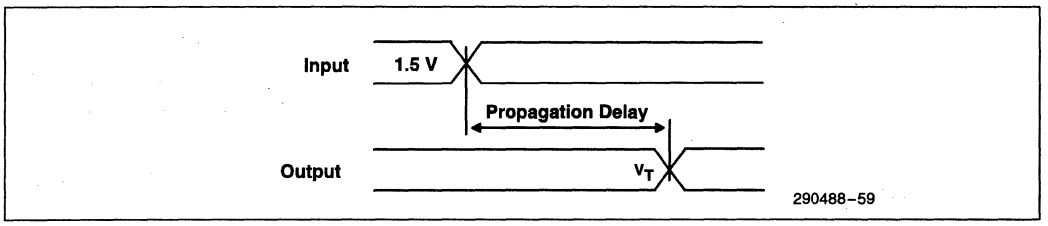


Figure 47. Propagation Delay

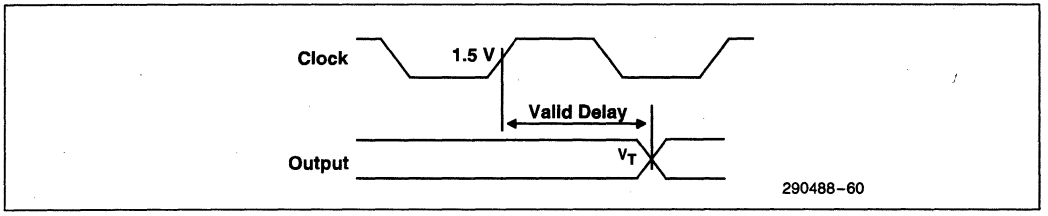


Figure 48. Valid Delay from Rising Clock Edge

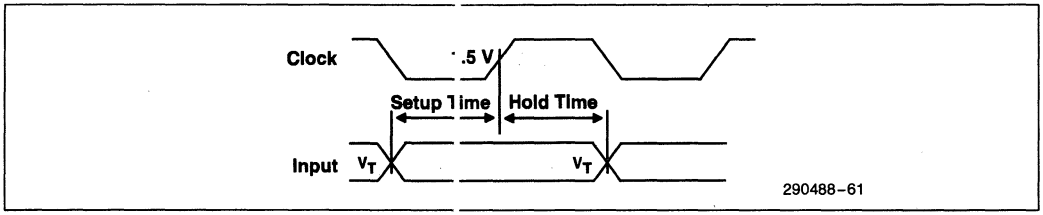


Figure 49. Setup and Hold Times

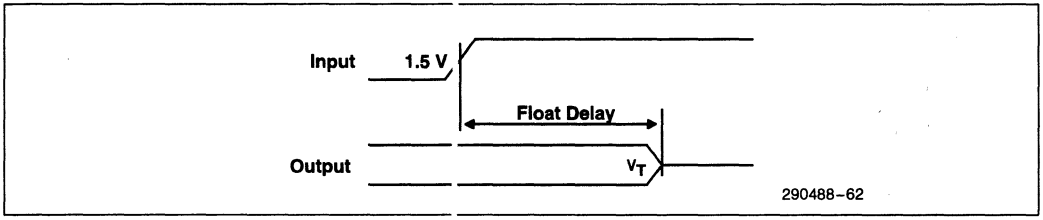


Figure 50. Float Delay

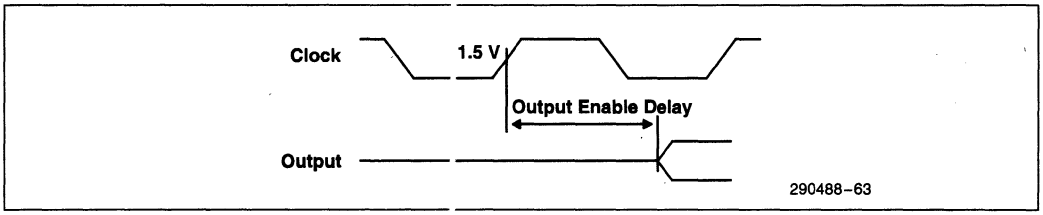


Figure 51. Output Enable Delay

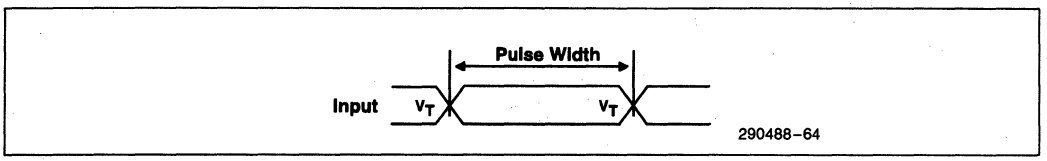


Figure 52. Pulse Width

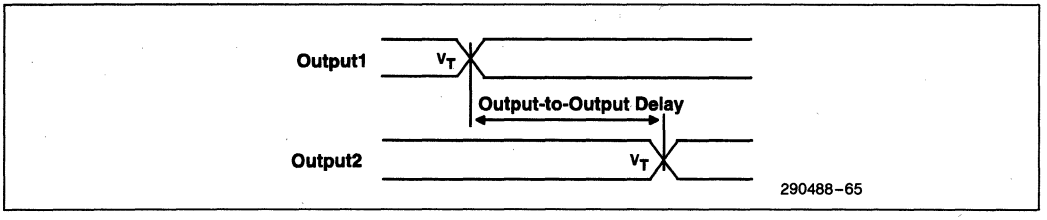


Figure 53. Output-to-Output Delay

7.0 IB AND PSC PACKAGE INFORMATION

Figure 54 shows the package information for the 82426EX IB and Figure 55 shows the package information for the 82425EX PSC.

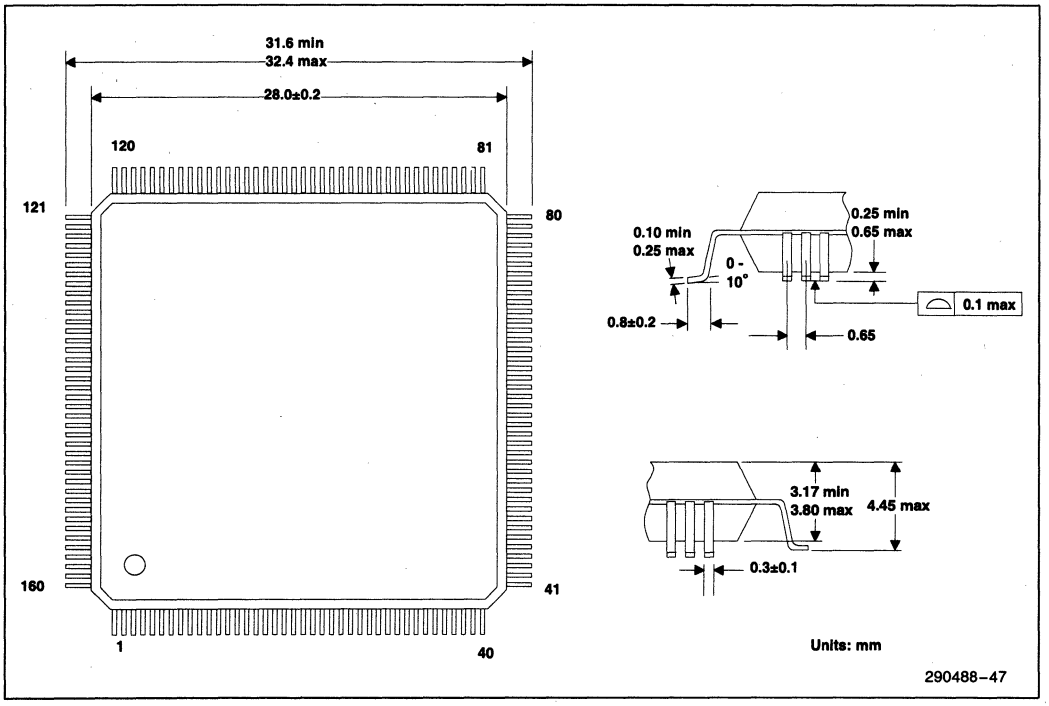


Figure 54. IB Package Dimensions

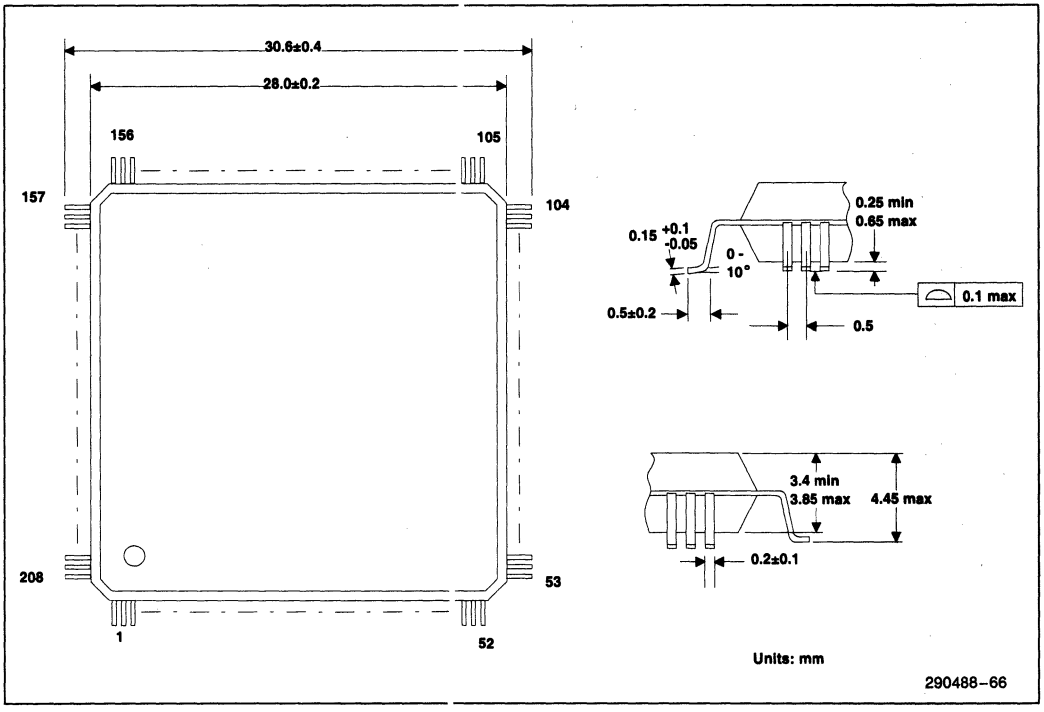


Figure 55. PSC Package Dimensions

7.1 Thermal Characteristics

The 82420EX PCIset is designed for operation at case temperatures between 0°C and 85°C. The thermal resistances of the packages are given in Table 25 and Table 26.

Table 25. PSC Package Thermal Resistance

Parameter	Air Flow (Linear Feet per Minute)		
	0	200	400
θ Junction to Case (°C/Watt)	16	16	16
θ Case to Ambient (°C/Watt)	34	27	23

Table 26. IB Package Thermal Resistance

Parameter	Air Flow (Linear Feet per Minute)		
	0	200	400
θ Junction to Case (°C/Watt)	16	16	16
θ Case to Ambient (°C/Watt)	34	27	23

8.0 TESTABILITY

8.1 PSC Testability

8.1.1 PSC TRI-STATE CONTROL

The PSC can be forced to tri-state all of its output drivers. The LOCK# must be connected to Vcc through a pull-up resistor for normal operation. The PSC will latch the values of LOCK# on the falling edge of CPURST. If these signals have been driven to a logic "0", the PSC will tri-state all of its drivers on the next rising edge of HCLKIN. The PSC will continue to tri-state all drivers until the rising edge of HCKLIN after LOCK# is forced to a logic "1".

8.1.2 PSC NAND TREE

A NAND Tree is provided in the PSC for Automated Test Equipment (ATE) board level testing. The NAND tree allows the tester to set the connectivity of each of the PSC signal pins. While in NAND tree mode, all PSC drivers except A30 are tri-stated. The NAND tree output is driven on pin A30.

NAND tree mode is entered similar to tri-state mode. During CPURST, PREQ0#, like LOCK#, is driven low. NAND tree mode is entered on the rising edge of HCLKIN after CPURST goes inactive.

Table 27 shows the sequence of the NAND tree in the PSC. Non-inverting inputs are driven directly into the input of a NAND gate in the NAND tree.

Table 27. PSC NAND Tree Structure

Tree Output #	Pin #	Pin Name	Type	Comments
	111	A30	NI	A30 is the test mode output
1	39	HCLKIN	NI	End of NAND tree, goes to A30 in test mode
2	208	AD0	NI	
3	207	AD1	NI	
4	206	AD2	NI	
5	205	AD3	NI	
6	204	AD4	NI	
7	203	AD5	NI	
8	202	AD6	NI	
9	199	AD7	NI	
10	198	C/BE0#	NI	
11	197	AD8	NI	
12	196	AD9	NI	
13	195	AD10	NI	
14	194	AD11	NI	
15	192	AD12	NI	
16	191	AD13	NI	
17	190	AD14	NI	
18	189	AD15	NI	
19	188	C/BE1#	NI	
20	186	PAR	NI	
21	184	STOP#	NI	
22	183	DEVSEL#	NI	
23	182	KBDRST#	INV	
24	181	TRDY#	NI	
25	180	IRDY#	NI	
26	179	FRAME#	NI	
27	177	C/BE2#	NI	
28	176	AD16	NI	

Table 27. PSC NAND Tree Structure (Continued)

Tree Output #	Pin #	Pin Name	Type	Comments
29	175	AD17	NI	
30	174	AD18	NI	
31	173	AD19	NI	
32	171	AD20	NI	
33	170	AD21	NI	
34	169	AD22	NI	
35	168	AD23	NI	
36	167	C/BE3#	NI	
37	166	AD24	NI	
38	163	AD25	NI	
39	162	AD26	NI	
40	161	AD27	NI	
41	160	AD28	NI	
42	159	AD29	NI	
43	158	AD30	NI	
44	157	AD31	NI	
45	156	PGNT0#	NI	
46	154	PGNT1#/HRDY#	NI	
47	152	PREQ1#/HDEV#	NI	
48	151	WE#	NI	
49	150	CAS7#	NI	
50	149	CAS3#	INV	
51	148	CAS3#	INV	
52	146	CAS2#	NI	
53	145	CAS5#	NI	
54	144	CAS1#	NI	
55	143	CAS4#	NI	
56	141	CAS0#	NI	

Table 27. PSC NAND Tree Structure (Continued)

Tree Output #	Pin #	Pin Name	Type	Comments
57	140	RAS4#	NI	
58	139	RAS3#	NI	
59	138	RAS2#	NI	
60	137	RAS1#	NI	
61	136	RAS0#	NI	
62	135	COE0#	NI	
63	134	COE1#	NI	
64	133	CI3O2	NI	
65	132	CI3E	NI	
66	131	SMIACT#	INV	
67	130	LBIDE#	NI	
68	129	MA10	NI	
69	127	MA9	NI	
70	126	MA8	NI	
71	125	MA7	NI	
72	124	MA6	NI	
73	123	MA5	NI	
74	122	MA4	NI	
75	121	MA3	NI	
76	120	MA2	NI	
77	118	MA1	NI	
78	117	MA0	NI	
79	116	CLK2IN	NI	
80	115	CWE1#	NI	
81	113	CWE0#	NI	
82	112	AHOLD	NI	
83	110	HDP3	NI	
84	109	HD23	NI	

Table 27. PSC NAND Tree Structure (Continued)

Tree Output #	Pin #	Pin Name	Type	Comments
85	108	HD20	NI	
86	107	HD22	NI	
87	106	HD19	NI	
88	105	HD21	NI	
89	104	HD11	NI	
90	103	HD18	NI	
91	102	HD9	NI	
92	101	HD13	NI	
93	100	HD17	NI	
94	99	HD10	NI	
95	98	HDP1	NI	
96	95	HD8	NI	
97	94	HD15	NI	
98	93	HD12	NI	
99	92	HD24	NI	
100	91	HD25	NI	
101	90	HD3	NI	
102	89	HDP2	NI	
103	88	HD27	NI	
104	87	HD5	NI	
105	86	HD16	NI	
106	85	HD26	NI	
107	83	HD14	NI	
108	82	HD29	NI	
109	81	HD31	NI	
110	80	HD6	NI	
111	79	HD7	NI	
112	78	HD28	NI	

Table 27. PSC NAND Tree Structure (Continued)

Tree Output #	Pin #	Pin Name	Type	Comments
113	77	HD4	NI	
114	76	HD30	INV	
115	75	HD2	NI	
116	74	HD1	NI	
117	73	HDP0	NI	
118	72	HD0	NI	
119	71	EADS#	NI	
120	70	HOLD	NI	
121	69	RDY#	NI	
122	68	KEN#	NI	
123	67	BRDY#	NI	
124	66	PCD/CACHE#	NI	
125	65	D/C#	NI	
126	64	W/R#	NI	
127	63	MI/O#	NI	
128	62	HLDA	NI	
129	59	BLAST#	INV	
130	58	ADS#	INV	
131	57	HITM#	NI	
132	56	BE3#	NI	
133	55	BE2#	NI	
134	54	BE1#	NI	
135	53	BE0#	NI	
136	52	TWE#	NI	
137	51	TAG7	NI	
138	50	TAG6	NI	
139	49	TAG5	NI	
140	48	TAG4	NI	

Table 27. PSC NAND Tree Structure (Continued)

Tree Output #	Pin #	Pin Name	Type	Comments
141	47	TAG3	NI	
142	46	TAG2	NI	
143	45	TAG1	NI	
144	44	TAG0	NI	
145	42	TAG8	NI	
146	41	SRESET/INIT	NI	
147	37	SMI#	INV	
148	36	A4	NI	
149	35	A6	NI	
150	34	A3	NI	
151	33	A2	NI	
152	32	A10	NI	
153	31	A8	NI	
154	30	A7	NI	
155	29	A11	NI	
156	28	A5	NI	
157	26	A9	INV	
158	25	A13	NI	
159	24	A16	NI	
160	23	A20	NI	
161	22	A12	NI	
162	21	A15	NI	
163	20	A22	NI	
164	19	A24	NI	
165	18	A14	NI	
166	17	A18	NI	
167	16	A21	NI	
168	14	A19	NI	

Table 27. PSC NAND Tree Structure (Continued)

Tree Output #	Pin #	Pin Name	Type	Comments
169	13	A23	NI	
170	12	A17	NI	
171	11	A26	NI	
172	9	A25	NI	
173	8	A31	NI	
174	7	PCICLKIN	NI	
175	6	LGNT#	NI	
176	5	LREQ#	NI	
177	4	SIDLE#	NI	
178	3	CMDV#	NI	
179	2	SERR#	NI	Cell furthest from NAND Tree output

NOTES:
NI = Non-Inverting
INV = Inverting

8.1.3 PSC NAND TREE DIAGRAM

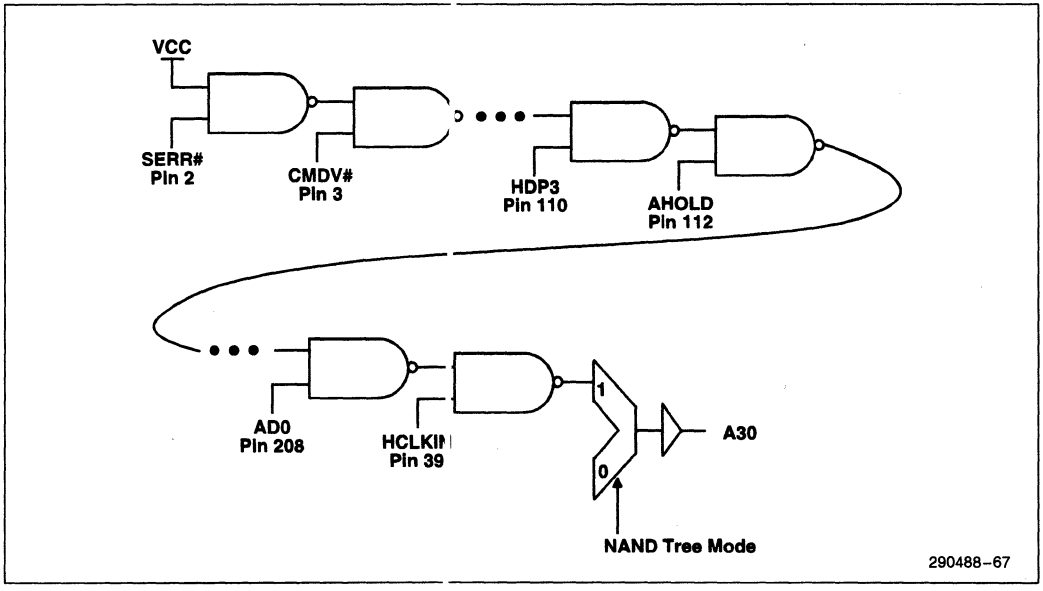


Figure 56. PSC NAND Tree Diagram

8.2 IB Testability

The TESTIN# pin is used to test the IB. During normal operations, the TESTIN# pin must be pulled high through an external pull-up.

8.2.1 IB TRI-STATE

The TESTIN# pin and IRQ3 are used to provide a high impedence tri-state test mode. When the following input combination occurs, all outputs and bidirectional pins are tri-stated, including SPKR:

TESTIN# = 0
IRQ3 = 1
IRQ5 = 0
IRQ6 = 1

The IB must be reset after the bidirectional and output pins have been tri-stated in this manner.

8.2.2 IB NAND TREE

A NAND Tree is provided primarily for VIL/VIH testing. The NAND Tree is also useful for ATE at board level testing. The NAND Tree allows for the tester to test the solder connections for each individual signal pin.

The TESTIN# pin along with IRQ5 and IRQ6 activate the NAND Tree. All outputs and bidirectional pins, except SPKR, are tri-stated when the following input combinations occur:

TESTIN# = 0 and IRQ5 = 1
or
TESTIN# = 0 and IRQ6 = 0

The output pulse train is observed at the SPKR test output, which is not tri-stated while in NAND Tree mode.

The sequence of the ATE test is as follows:

1. Drive TESTIN# low.
2. Drive each input and bidirectional pin noted in Section 8.2.3 high, except for SPKR.
3. Starting with pin 1, SYSCLK, individually drive each pin low. Expect SPKR to toggle with each pin.
4. Turn off tester drivers before driving TESTIN# high.
5. Reset the IB prior to proceeding with further testing.

8.2.3 IB NAND TREE CELL ORDER

NAND Tree cell order is dependent on pin placement. The IB NAND Tree follows pin order around the part from pin 1 to pin 158.

Table 28. I3 NAND Tree Structure

Tree Output #	Pin #	Pin Name	Type	Comments
	69	SPKR	NI	Test Mode Output
1	158	SA12	NI	End of NAND Tree, goes to SPKR in test mode
2	157	REFRESH#	NI	
3	156	SA13	NI	
4	155	DREQ1	NI	
5	154	SA14	NI	
6	153	DACK1#	NI	
7	152	SA15	NI	
8	151	DREQ3	NI	
9	149	SA16	NI	
10	148	DACK3#	NI	
11	147	SA17	NI	
12	146	IOR#	NI	
13	145	SA18	NI	
14	144	IOW#	NI	
15	143	SA19	NI	
16	142	SMEMR#	NI	
17	139	AEN	NI	
18	138	SMEMW#	NI	
19	137	IOCHRDY	NI	
20	136	SD0	NI	
21	135	SD1	NI	
22	134	ZEROWS#	NI	
23	133	SD2	NI	
24	132	SD3	NI	
25	131	DREQ2	NI	
26	129	SD4	NI	
27	128	SD5	NI	
28	127	IRQ9	NI	

Table 28. IB NAND Tree Structure (Continued)

Tree Output #	Pin #	Pin Name	Type	Comments
29	126	SD6	NI	
30	125	SD7	NI	
31	124	RSTDRV	NI	
32	123	IOCHK#	NI	
33	122	KBCCS#	NI	
34	119	IRQ1	NI	
35	118	PIRQ0#	NI	
36	117	PIRQ1#	NI	
37	116	SERR#	NI	
	115	TESTIN#	NI	Not part of NAND tree
38	114	PWROK	NI	
39	113	PCICLK2	NI	
40	112	PCICLK1	NI	
41	111	PCIRST#	NI	
42	109	CLK2OUT	NI	
43	108	CLK2IN	NI	
44	107	CMDV#	NI	
45	106	SIDLE#	NI	
46	105	LREQ#	NI	
47	104	LGNT#	NI	
48	103	A17	NI	
49	102	A14	NI	
50	101	A15	NI	
51	99	OSC	NI	
52	98	A12	NI	
53	97	A16	NI	
54	96	A13	NI	
55	95	A9	NI	
56	94	A5	NI	

Table 28. IB NAND Tree Structure (Continued)

Tree Output #	Pin #	Pin Name	Type	Comments
57	93	A11	NI	
58	92	A7	NI	
59	91	A8	NI	
60	89	A10	NI	
61	88	A6	NI	
62	87	A4	NI	
63	86	A2	NI	
64	85	A3	NI	
65	84	SMI#	NI	
66	83	HCLKIN	NI	
67	82	HCLKOUT1	NI	
68	81	HCLKOUT2	NI	
69	79	CPURST	NI	
70	78	SRESET	NI	
71	77	NMI	NI	
72	76	IGNNE#	NI	
73	75	FERR#	NI	
74	73	INTR	NI	
75	72	STPCLK#	NI	
76	71	EXTSMI#	NI	
77	68	RTCALE	NI	
78	67	RTCCS#	NI	
79	66	BIOSCS#	NI	
80	65	XBUSOE#	NI	
81	64	XBUSTR#	NI	
82	63	IRQ8#	NI	
83	62	SD15	NI	
84	61	SD14	NI	

Table 28. IB NAND Tree Structure (Continued)

Tree Output #	Pin #	Pin Name	Type	Comments
85	59	SD13	NI	
86	58	SD12	NI	
87	57	DREQ7	NI	
88	56	SD11	NI	
89	55	DACK7#	NI	
90	54	SD10	NI	
91	53	DREQ6	NI	
92	52	SD9	NI	
93	51	DACK6#	NI	
94	49	SD8	NI	
95	48	DREQ5	NI	
96	47	MEMW#	NI	
97	45	DACK5#	NI	
98	44	MEMR#	NI	
99	43	DREQ0	NI	
100	42	LA17	NI	
101	41	DACK0#	NI	
102	40	LA18	NI	
103	39	IRQ14	NI	
104	37	LA19	NI	
105	36	IRQ15	NI	
106	35	LA20	NI	
107	34	IRQ12/M	NI	
108	33	LA21	NI	
109	32	IRQ11	NI	
110	31	LA22	NI	
111	30	IRQ10	NI	
112	29	LA23	NI	

Table 28. IB NAND Tree Structure (Continued)

Tree Output #	Pin #	Pin Name	Type	Comments
113	28	IOCS16#	NI	
114	26	SBHE#	NI	
115	25	MEMCS16#	NI	
116	24	SA0	NI	
117	23	SA1	NI	
118	22	SA2	NI	
119	21	SA3	NI	
120	18	BALE	NI	
121	17	SA4	NI	
122	16	TC	NI	
123	15	SA5	NI	
124	14	DACK2#	NI	
125	13	SA6	NI	
126	12	IRQ3	NI	
127	11	SA7	NI	
128	9	IRQ4	NI	
129	8	SA8	NI	
130	7	IRQ5	NI	
131	6	SA9	NI	
132	5	IRQ6	NI	
133	4	SA10	NI	
134	3	IRQ7	NI	
135	2	SA11	NI	
136	1	SYSCLK	NI	Cell furthest from NAND Tree output

8.2.4 IB NAND TREE DIAGRAM

Figure 57 shows the NAND Tree diagram. The only function pin not included in the pin order is SPKR, which is used as the Test Output at the end of the tree.

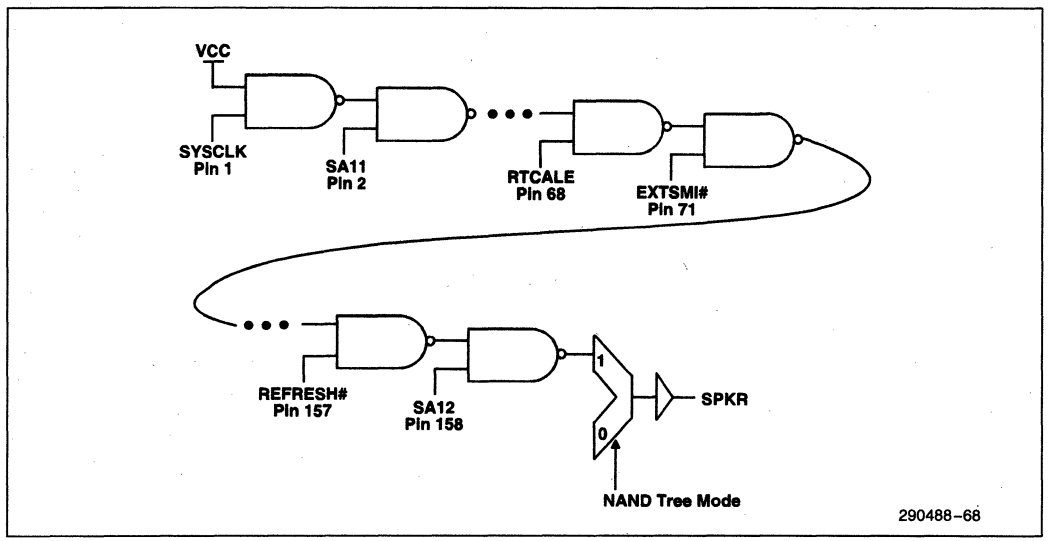


Figure 57. IB NAND Tree Diagram

9.0 REVISION HISTORY

Revision -003 of the 82420EX PCIset data sheet contains updates and improvements to the original version. A revision summary of changes is listed below.

The sections significantly revised since revision -001 are:

Global	The 82420EX PCIset supports host bus operations of 25 and 33 MHz. All references to 50 MHz support have been removed.
Sections 1.1, 1.2, 2.1.1	PGNT1#/HRDY# and M/IO# signal type was incorrectly published. M/IO# and PGNT1#/HRDY# are I/O pins. EXTSMI# and PWROK signal type was incorrectly published. EXTSMI# and PWROK are IS pins. SERR# was added to Table 3.
Section 2.2.4	Pin description for the OSC pin has been added.
Section 3.1	Data returned during accesses to a reserved register location was incorrectly published. Reads return all 0's during accesses to a reserved register location.
Section 3.3.5	More information is provided on the contents of the Revision Identification Register.
Section 3.3.6	The byte merging feature description has been updated.
Section 3.3.10	Part Revision Register description has been updated.
Section 3.3.20	A warning has been added concerning O/S which size system memory directly without the use of system BIOS.

Section 3.3.21	Bits[2:0] = 000 and bits[2:0] = 001 are now reserved configurations in the SMRAM Control Register.
Section 3.3.22	Changes have been made to the Fast Off Timer Count Granularity.
Section 3.3.25	Changes have been made to the Fast Off Timer count down value.
Section 3.3.26	Bits[15:8] were incorrectly omitted from the SMI Request Register. Bits[15:8] are shown as reserved.
Section 3.3.27	Value of the duration of the STPCLK# asserted period has changed.
Section 3.3.28	Value of the duration of the STPCLK# negated period has changed.
Section 4.3.4	Further information has been added to the keyboard controller circuit description.
Section 4.12.1	Table 19 has been updated. New notes have been added to Table 19.
Section 4.13.6	Table 21 has been updated.
Section 5.0	Section 5.0 has been removed. The 82420EX PCIset electrical characteristics will be published as a separate document. See your Intel representative for a copy of the document with the 82420EX PCIset electrical characteristics.
Section 6.0	Section 6.0 is now Section 5.0. Figure 54 and Figure 55 have changed.
Section 6.1	Section 6.1 is now Section 5.1. Table 25 and Table 26 have changed.

The sections significantly revised since revision -002 are:

Section 3.3.22	The description of bit 1 in the SMI Control Register has changed. Software can only set bit 1 to a 0 by writing a 0 to it.
Section 5.0	Section 5.0 has been added. This is a new section titled Design Considerations.
Section 6.0	Section 6.0 has been added. This section includes the AC, DC and mechanical specifications and timings. The following IB specifications have changed since the electrical characteristics were last published in revision -001: t1c (min), t1f (min). The following PSC specifications have changed since the electrical characteristics were last published in revision -001: t1c (min), t1d (min), t41b (min), t41c (min).

82420/82430
PCIset BRIDGE COMPONENT

82378ZB (SIO), 82379AB (SIO.A) FOR ISA BUSES

- Provides the Bridge between the PCI Bus and ISA Bus
- 100% PCI and ISA Compatible
- Enhanced DMA Functions (82378ZB Only)
- Integrated Data Buffers to Improve Performance
- Integrated 16-bit BIOS Timer
- Arbitration for PCI Devices
- Arbitration for ISA Devices
- Integrates the Functionality of One 82C54 Timer
- Integrates the Functionality of Two 82C59 Interrupt Controllers
- Non-Maskable Interrupts (NMI)
- Four Dedicated PCI Interrupts
- Complete Support for SL Enhanced Intel486™ CPU's
- Integrated Power Management Support
  - System Management Interrupts
  - Fast Off Timer
  - STPCLK# Signal to Throttle CPU Clock
  - APM Port
- Provides I/O APIC for Dual-Processor (DP) Support

82374EB/SB (ESC), 82375EB/SB (PCEB) FOR EISA BUSES

- Provides the Bridge between the PCI Bus and EISA Bus
- 100% PCI and EISA Compatible
- Data Buffers Improve Performance
- Data Buffer Management Ensures Data Coherency
- Burst Transfers on both the PCI and EISA Buses
- 32-Bit Data Paths
- PCI and EISA Address Decoding and Mapping
- Programmable Main Memory Address Decoding
- Integrated EISA Compatible Bus Controller
- Supports Eight EISA Slots
- Provides Enhanced DMA Controller
- Provides High Performance Arbitration
- Integrates Support Logic for X-Bus Peripheral and more
- Integrates the Functionality of Two 82C59 Interrupt Controllers and Two 82C54 Timers
- Generates Non-Maskable Interrupts
- Provides BIOS Interface

The 82420/82430 PCIset Bridge components provide a bridge between the PCI to either EISA or ISA buses. The 82378 provides the bridge between PCI bus and the ISA bus while the 82374 and 83275 together provide the bridge between the PCI bus and the EISA bus.

The SIO integrates many of the common I/O functions found in todays ISA based PC systems. The SIO incorporates the logic for a PCI interface (master and slave), ISA interface (master and slave), enhanced seven channel DMA controller and support for other decode logic. The 82379AB adds an APIC for dual-processing Pentium™ Processor systems.

The complete documents for these products can be ordered by calling 1-800-548-4725. Ask for 290473 (ISA Bridge), 290520 (ISA-APIC Bridge), 290483 (EISA Bridge).

November 1994
Order Number: 290509-002

The 82374 EISA System Component (ESC) and 83275 PCI-EISA Bridge (PCEB) together provide the EISA system compatible master/slave functions on both the PCI Local Bus and the EISA Bus and the common I/O functions found in today's EISA systems. The ESC incorporates the logic for an EISA (master and slave) interface, EISA bus controller, enhanced seven channel DMA controller with Scatter-Gather support, EISA arbitration, 14 channel interrupt controller, five programmable timer/counters and non-maskable control logic. The ESC also integrates support logic to decode peripheral devices such as the Flash BIOS, Real Time Clock, Keyboard/Mouse Controller, Floppy Controller, two Serial Ports, one Parallel Port, and IDE Hard Disk Drive. The PCEB provides the address and data paths, bus controls, and bus protocol translation for PCI-to-EISA and EISA-to-PCI transfers. Extensive data buffering in both directions increases system performance by maximizing PCI and EISA Bus efficiency and allowing concurrency on the two buses. The PCEB integrates central bus control functions, PCI parity generation, system error reporting, and programmable PCI and EISA memory and I/O address space mapping and decoding.

82374EB/82374SB EISA SYSTEM COMPONENT (ESC)

- Integrates EISA Compatible Bus Controller
  - Translates Cycles between EISA and ISA Bus
  - Supports EISA Burst and Standard Cycles
  - Supports ISA Zero Wait-State Cycles
  - Supports Byte Assembly/ Disassembly for 8-, 16- and 32-Bit Transfers
  - Supports EISA Bus Frequency of Up to 8.33 MHz
- Supports Eight EISA Slots
  - Directly Drives Address, Data and Control Signals for Eight Slots
  - Decodes Address for Eight Slot Specific AENs
- Provides Enhanced DMA Controller
  - Provides Scatter-Gather Function
  - Supports Type A, Type B, Type C (Burst), and Compatible DMA Transfer
  - Provides Seven Independently Programmable Channels
  - Integrates Two 82C37A Compatible DMA Controllers
- Integrates the Functionality of Two 82C59 Interrupt Controllers and Two 82C54 Timers
  - Provides 14 Programmable Channels for Edge or Level Interrupts
  - Provides 4 PCI Interrupts Routable to any of 11 Interrupt Channels
  - Supports Timer Function for Refresh Request, System Timer, Speaker Tone, Fail Safe Timer, and CPU Speed Control
- Advanced Programmable Interrupt Controller (APIC)
  - Multiprocessor Interrupt Management
  - Separate Bus for Interrupt Messages
- 5V CMOS Technology
- Provides High Performance Arbitration
  - Supports Eight EISA Masters and PCEB
  - Supports ISA Masters, DMA Channels, and Refresh
  - Provides Programmable Arbitration Scheme for Fixed, Rotating, or Combination Priority
- Integrates Support Logic for X-Bus Peripherals
  - Generates Chip Selects/Encoded Chip Selects for Floppy and Keyboard Controller, IDE, Parallel/ Serial Ports, and General Purpose Peripherals
  - Provides Interface for Real Time Clock
  - Generates Control Signals for X-Bus Data Transceiver
  - Integrates Port 92, Mouse Interrupt, and Coprocessor Error Reporting
- Generates Non-Maskable Interrupts (NMI)
  - PCI System Errors
  - PCI Parity Errors
  - EISA Bus Parity Errors
  - Fail Safe Timer
  - Bus Timeout
  - Via Software Control
- Provides BIOS Interface
  - Supports 512 KBytes of Flash or EPROM BIOS on the X-Bus
  - Allows BIOS on PCI
  - Supports Integrated VGA BIOS
- 82374SB System Power Management (Intel SMM Support)
  - Fast On/Off Support via SMI Generation—Hardware Events, Software Events, EXTSMI#, Fast Off Timer, System Events
  - Programmable CPU Clock Control
  - Enables Energy Efficient Desktop Systems
- 208-Pin QFP Package

The complete document for this product can be ordered by calling 1-800-548-4725 and ask for order number 290483.

November 1994
Order Number: 290476-004

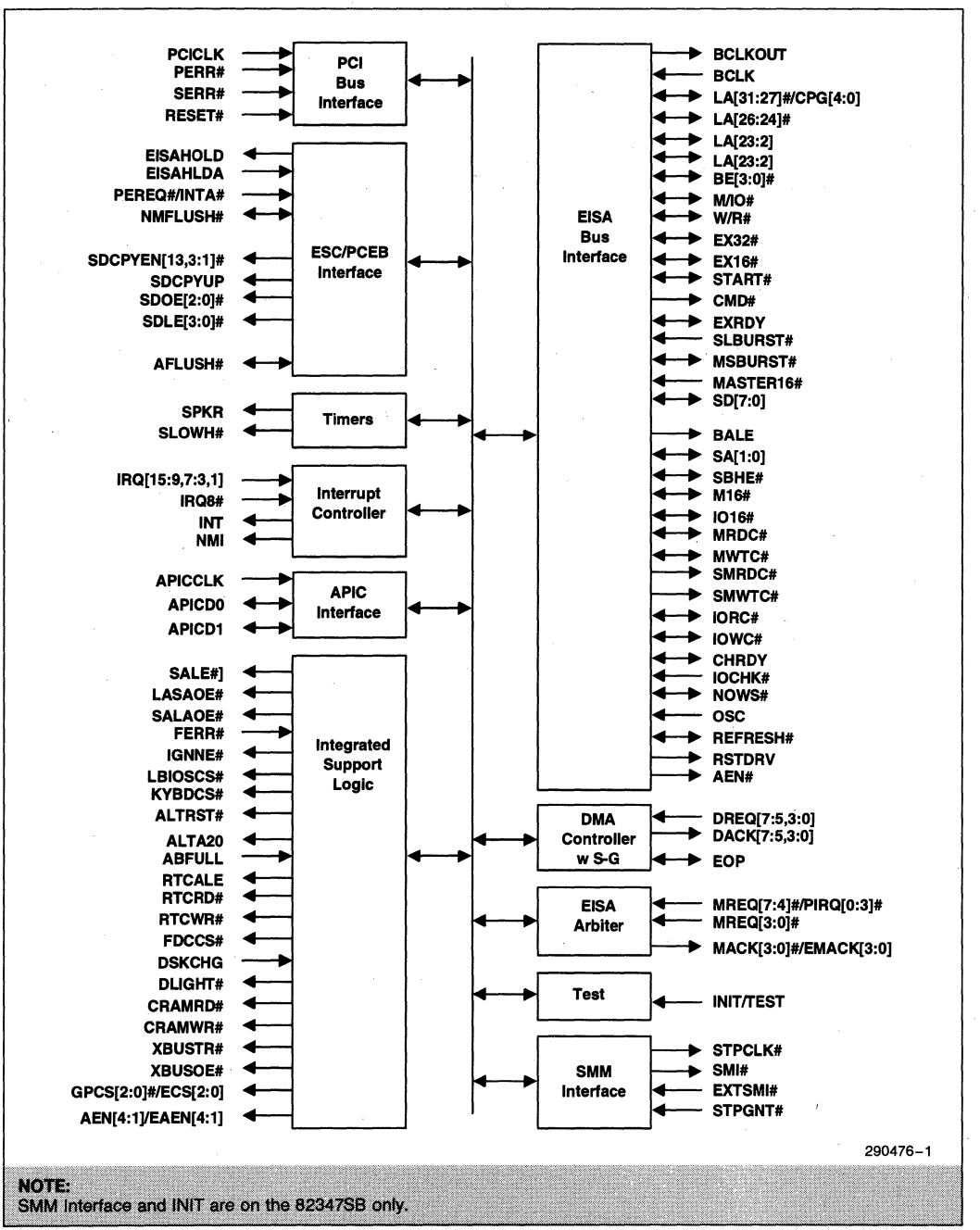
IMPORTANT—READ THIS SECTION BEFORE READING THE REST OF THE DATA SHEET.

This data sheet describes the 82374EB and 82374SB components. All normal text describes the functionality for both components. All features that exist on the 82374SB are shaded as shown below.

This is an example of what the shaded sections that apply only to the 82374SB component look like.

The 82374EB/SB EISA System Component (ESC) provides all the EISA system compatible functions. The ESC with the PCEB provide all the functions to implement an EISA-to-PCI bridge and EISA I/O subsystem. The ESC integrates the common I/O functions found in today's EISA-based PC systems. The ESC incorporates the logic for an EISA (master and slave) interface, EISA bus controller, enhanced seven channel DMA controller with scatter-gather support, EISA arbitration, 14 channel interrupt controller, Advanced Programmable Interrupt Controller (APIC), five programmable timer/counters, and non-maskable-interrupt (NMI) control logic. The ESC also integrates support logic to decode peripheral devices such as the Flash BIOS, real time clock, keyboard/mouse controller, floppy controller, two serial ports, one parallel port, and IDE hard disk drive.

The 82374SB also contains support for SMM power management



NOTE:
SMM Interface and INIT are on the 82347SB only.

Simplified ESC Block Diagram

82375EB/82375SB PCI-EISA BRIDGE (PCEB)

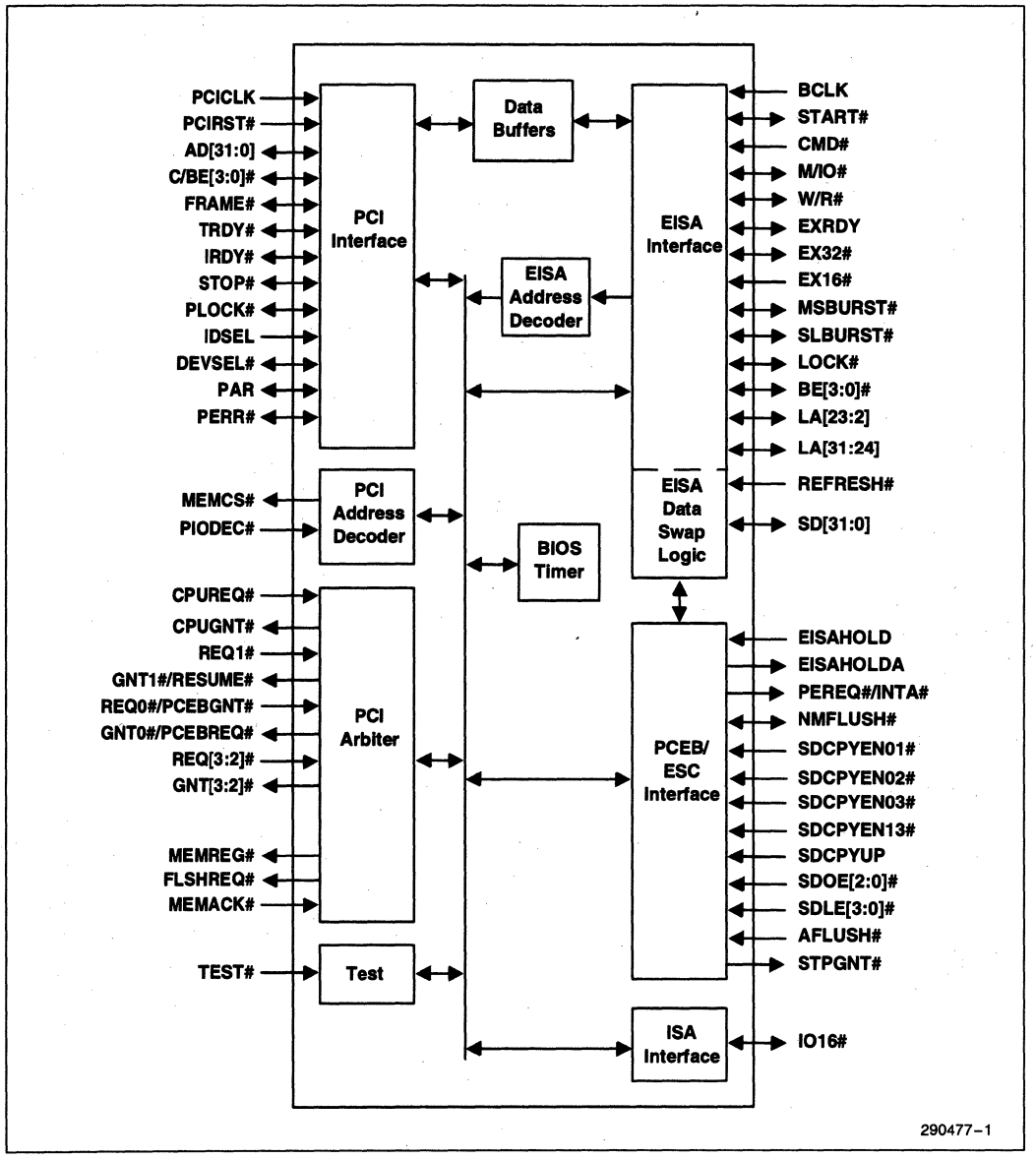
- **Provides the Bridge Between the PCI Local Bus and EISA Bus**
- **100% PCI and EISA Compatible**
  - **— PCI and EISA Master/Slave Interface**
  - **— Directly Drives 10 PCI Loads and 8 EISA Slots**
  - **— Supports PCI from 25 to 33 MHz**
- **Data Buffers Improve Performance**
  - **— Four 32-Bit PCI-to-EISA Posted Write Buffers**
  - **— Four 16-Byte EISA-to-PCI Read/Write Line Buffers**
  - **— EISA-to-PCI Read Prefetch**
  - **— EISA-to-PCI and PCI-to-EISA Write Posting**
- **Data Buffer Management Ensures Data Coherency**
  - **— Flush Posted Write Buffers**
  - **— Flush or Invalidate Line Buffers**
  - **— System-Wide Data Buffer Coherency Control**
- **Burst Transfers on Both the PCI and EISA Buses**
- **32-Bit Data Paths**
- **Integrated EISA Data Swap Buffers**
- **Arbitration for PCI Devices**
  - **— Supports Six PCI Masters**
  - **— Fixed, Rotating, or a Combination of the Two**
  - **— Supports External PCI Arbiter and Arbiter Cascading**
- **PCI and EISA Address Decoding and Mapping**
  - **— Positive Decode of Main Memory Areas (MEMCS# Generation)**
  - **— Four Programmable PCI Memory Space Regions**
  - **— Four Programmable PCI I/O Space Regions**
- **Programmable Main Memory Address Decoding**
  - **— Main Memory Sizes Up to 512 MBytes**
  - **— Access Attributes for 15 Memory Segments in First 1 MByte of Main Memory**
  - **— Programmable Main Memory Hole**
- **Integrated 16-Bit BIOS Timer**

1

The 82375EB/SB PCI-EISA Bridge (PCEB) provides the master/slave functions on both the PCI Local Bus and the EISA Bus. Functioning as a bridge between the PCI and EISA buses, the PCEB provides the address and data paths, bus controls, and bus protocol translation for PCI-to-EISA and EISA-to-PCI transfers. Extensive data buffering in both directions increases system performance by maximizing PCI and EISA Bus efficiency and allowing concurrency on the two buses. The PCEB's buffer management mechanism ensures data coherency. The PCEB integrates central bus control functions including a programmable bus arbiter for the PCI Bus and EISA data swap buffers for the EISA Bus. Integrated system functions include PCI parity generation, system error reporting, and programmable PCI and EISA memory and I/O address space mapping and decoding. The PCEB also contains a BIOS Timer that can be used to implement timing loops. The PCEB is intended to be used with the EISA System Component (ESC) to provide an EISA I/O subsystem interface.

The complete document for this product can be ordered by calling 1-800-548-4725 and ask for order number 290483.

November 1994
Order Number: 290477-004



PCEB Simplified Block Diagram

82378 SYSTEM I/O (SIO)

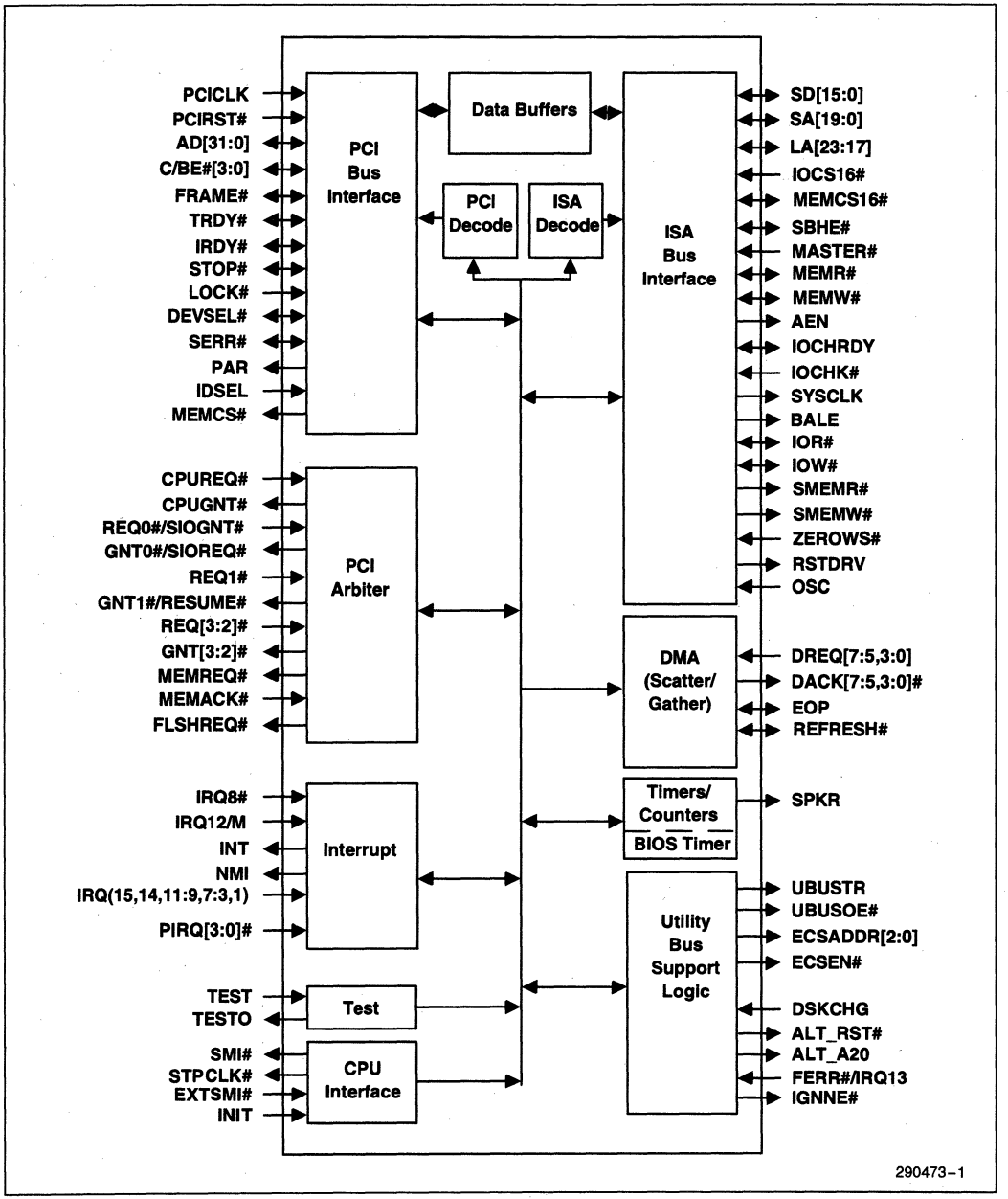
- **Provides the Bridge Between the PCI Bus and ISA Bus**
- **100% PCI and ISA Compatible**
  - **— PCI and ISA Master/Slave Interface**
  - **— Directly Drives 10 PCI Loads and 6 ISA Slots**
  - **— Supports PCI at 25 MHz and 33 MHz**
  - **— Supports ISA from 6 MHz to 8.33 MHz**
- **Enhanced DMA Functions**
  - **— Scatter/Gather**
  - **— Fast DMA Type A, B and F**
  - **— Compatible DMA Transfers**
  - **— 32-bit Addressability**
  - **— Seven Independently Programmable Channels**
  - **— Functionality of Two 82C37A DMA Controllers**
- **Integrated Data Buffers to Improve Performance**
  - **— 8-Byte DMA/ISA Master Line Buffer**
  - **— 32-bit Posted Memory Write Buffer to ISA**
- **Integrated 16-bit BIOS Timer**
- **Non-Maskable Interrupts (NMI)**
  - **— PCI System Errors**
  - **— ISA Parity Errors**
- **Arbitration for ISA Devices**
  - **— ISA Masters**
  - **— DMA and Refresh**
- **Four Dedicated PCI Interrupts**
  - **— Level Sensitive**
  - **— Can be Mapped to Any Unused Interrupt**
- **Arbitration for PCI Devices**
  - **— Six PCI Masters Supported**
  - **— Fixed, Rotating, or a Combination of the Two**
- **Utility Bus (X-Bus) Peripheral Support**
  - **— Provides Chip Select Decode**
  - **— Controls Lower X-Bus Data Byte Transceiver**
- **Integrates the Functionality of One 82C54 Timer**
  - **— System Timer**
  - **— Refresh Request**
  - **— Speaker Tone Output**
- **Integrates the Functionality of Two 82C59 Interrupt Controllers**
  - **— 14 Interrupts Supported**
  - **— Edge/Level Selectable Interrupts: Each Interrupt Individually Programmable**
- **Complete Support for SL Enhanced Intel486 CPU's**
  - **— SMI# Generation Based on System Hardware Events**
  - **— STPCLK# Generation to Power Down the CPU**

1

The 82378 System I/O (SIO) component provides the bridge between the PCI bus and the ISA expansion bus. The SIO also integrates many of the common I/O functions found in today's ISA based PC systems. The SIO incorporates the logic for a PCI interface (master and slave), ISA interface (master and slave), enhanced seven channel DMA controller that supports fast DMA transfers and Scatter/Gather, data buffers to isolate the PCI bus from the ISA bus and to enhance performance, PCI and ISA arbitration, 14 level interrupt controller, a 16-bit BIOS timer, three programmable timer/counters, and Non-Maskable Interrupt (NMI) Control Logic. The SIO also provides decode for peripheral devices such as the Flash BIOS, Real Time Clock, Keyboard/Mouse Controller, Floppy Controller, two Serial Ports, one Parallel Port, and IDE Hard Disk Drive.

The 82378 also supports several Advanced Power Management features such as SMI#, APM Register, Fast On and Fast Off Event Timers, Clock Throttling, and support for an external SMI# Interrupt. The 82378 also supports a total of 6 PCI Masters, and can support up to 4 PCI Interrupts.

December 1994
Order Number: 290473-004



SIO Component Block Diagram

82378 SYSTEM I/O (SIO)

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1.0 ARCHITECTURAL OVERVIEW

The major functions of the SIO component are broken up into blocks as shown in the SIO Component Block Diagram. A description of each block is provided below.

PCI Bus Interface

The PCI Bus Interface provides the interface between the SIO and the PCI bus. The SIO provides both a master and slave interface to the PCI bus. As a PCI master, the SIO runs cycles on behalf of DMA, ISA masters, and the internal data buffer management logic when buffer flushing is required. The SIO will burst a maximum of two Dwords when reading from PCI memory, and one Dword when writing to PCI memory. The SIO does not generate PCI I/O cycles as a master. As a PCI slave, the SIO accepts cycles initiated by PCI masters targeted for the SIO's internal register set or the ISA bus. The SIO will accept a maximum of one data transaction before terminating the transaction. This supports the Incremental Latency Mechanism as defined in the Peripheral Component Interconnect (PCI) Specification.

As a master, the SIO generates address and command signal (C/BE#) parity for read and write cycles, and data parity for write cycles. As a slave, the SIO generates data parity for read cycles. Parity checking is not supported. The SIO also provides support for system error reporting by generating a Non-Maskable-Interrupt (NMI) when SERR# is driven active.

The SIO, as a resource, can be locked by any PCI master. In the context of locked cycles, the entire SIO subsystem (including the ISA bus) is considered a single resource.

The SIO directly supports the PCI Interface running at either 25 MHz or 33 MHz. If a frequency of less than 33 MHz is required (not including 25 MHz), a SYSCLK divisor value (as indicated in the ISA Clock Divisor Register) must be selected that guarantees that the ISA bus frequency does not violate the 6 MHz to 8.33 MHz SYSCLK range.

PCI Arbiter

The PCI arbiter provides support for six PCI masters; the Host Bridge, SIO, and four PCI masters. The arbiter can be programmed for a purely rotating scheme, fixed, or a combination of the two. The Arbiter can also be programmed to support bus parking. This gives the Host Bridge default access to the PCI bus when no other device is requesting service. The arbiter can be disabled if an external arbiter is used.

PCI Decode/ISA Decode

The SIO contains two address decoders; one to decode PCI initiated cycles and one to decode ISA master and DMA initiated cycles. Two decoders are used to allow the PCI and ISA buses to run concurrently.

The SIO is also programmable to provide address decode on behalf of the Host Bridge. When programmed, the SIO monitors the PCI and ISA address buses, and generates a memory chip select signal (MEMCS#) indicating that the current cycle is targeted for system memory residing behind the Host Bridge. This feature can be disabled through software.

Data Buffers

To isolate the slower ISA bus from the PCI bus, the SIO provides two types of data buffers. One Dword deep posted write buffer is provided for the posting of PCI initiated memory write cycles to the ISA bus. The second buffer is a bi-directional, 8-byte line buffer used for ISA master and DMA accesses to the PCI bus. All DMA and ISA master read and write cycles go through the 8-byte line buffer.

The data buffers also provide the data assembly or disassembly when needed for transactions between the PCI and ISA buses.

Buffering is programmable and can be enabled or disabled through software.

ISA Bus Interface

The SIO incorporates a fully ISA-bus compatible master and slave interface. The SIO directly drives six ISA slots without external data or address buffering. The ISA interface also provides byte swap logic, I/O recovery support, wait-state generation, and SYSCLK generation. The SIO supports ISA bus frequencies from 6 MHz to 8.33 MHz.

As an ISA master, the SIO generates cycles on behalf of DMA, Refresh, and PCI master initiated cycles. The SIO supports compressed cycles when accessing ISA slaves (i.e. ZEROWS# asserted). As an ISA slave, the SIO accepts ISA master accesses targeted for the SIO's internal register set or ISA master memory cycles targeted for the PCI bus. The SIO does not support ISA master initiated I/O cycles targeted for the PCI bus.

The SIO also monitors ISA master to ISA slave cycles to generate SMEMR# or SMEMW#, and to support data byte swapping, if necessary.

DMA

The DMA controller incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels. Each channel can be programmed for 8- or 16-bit DMA device size, and ISA-compatible or fast DMA type "A", type "B", or type "F" timings. Full 32-bit addressing is supported as an extension of the ISA-compatible specification. The DMA controller is also responsible for generating ISA refresh cycles.

The DMA controller supports an enhanced feature called Scatter/Gather. This feature provides the capability of transferring multiple buffers between memory and I/O without CPU intervention. In Scatter/Gather mode, the DMA can read the memory address and word count from an array of buffer descriptors, located in system memory, called the Scatter/Gather Descriptor (SGD) Table. This allows the DMA controller to sustain DMA transfers until all of the buffers in the SGD table are read.

Timer Block

The timer block contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. These three counters are combined to provide the System Timer function, Refresh Request, and speaker tone. The three counters use the 14.31818 MHz OSC input for a clock source.

In addition to the three counters, the SIO provides a programmable 16-bit BIOS timer. This timer can be used by BIOS software to implement timing loops. The timer uses the ISA system clock (SYSCLK) divided by 8 as a clock source. An 8:1 ratio between the SYSCLK and the BIOS timer clock is always maintained. The accuracy of the BIOS timer is ±1 ms.

Utility Bus (X-Bus) Logic

The SIO provides four encoded chip selects that are decoded externally to provide chip selects for Flash BIOS, Real Time Clock, Keyboard/Mouse Controller, Floppy Controller, two Serial Ports, one Parallel Port, and an IDE Hard Disk Drive. The SIO provides the control for the buffer that isolates the lower eight bits of the Utility Bus from the lower 8 bits of the ISA bus.

In addition to providing the encoded chip selects and Utility Bus buffer control, the SIO also provides Port 92 functions (Alternate Reset and Alternate A20), Coprocessor error reporting, the Floppy DSKCHG function, and a mouse interrupt input.

Interrupt Controller Block

The SIO provides an ISA compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and 2 internal interrupts are possible.

Test

The test block provides the interface to the test circuitry within the SIO. The test input can be used to tri-state all of the SIO outputs.

2.0 PIN ASSIGNMENT

The SIO package is a 208-pin Quad Flatpack (QFP). The package signals are listed in Table 1. The following notations are used to describe pin types.

Signal Type	Description
I	**Input** is a standard input-only signal.
O	**Totem Pole Output** is a standard active driver.
OD	**Open Drain** Input/Output
IO	**Input/Output** is a bidirectional, tri-state pin.
s/t/s	**Sustained Tri-State** is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives a s/t/s pin low must drive it high for at least one clock before letting it float. A new agent can not start driving a s/t/s signal any sooner than one clock after the previous owner tri-states it. A pull-up sustains the inactive state until another agent drives it and is provided by the central resource.
t/s/o	**Tri-State Output**

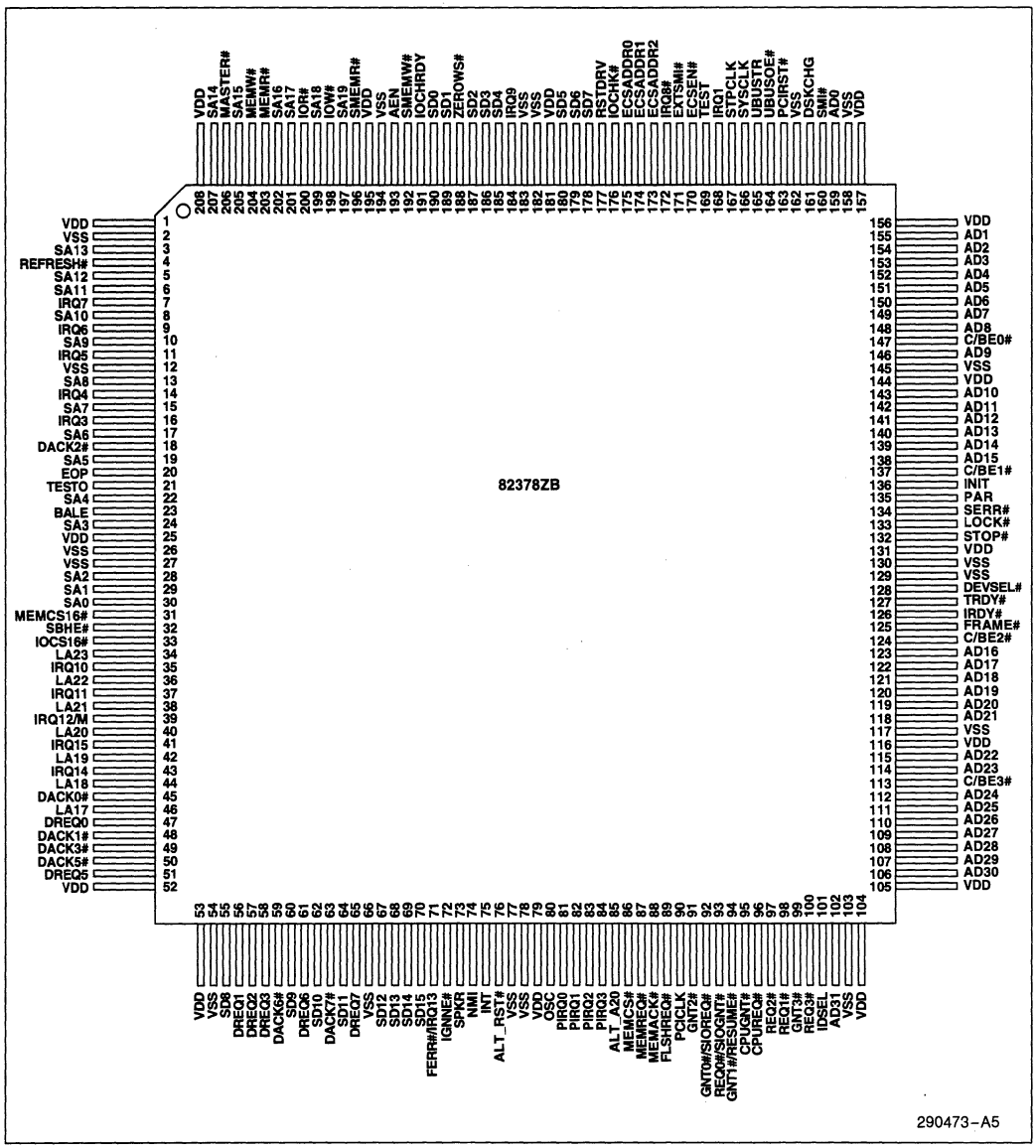

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Figure 1. SIO Package Pinout Diagram

Table 1. Alphabetical Pin Assignment

Pin Name	Pin #	Type
AD0	159	I/O
AD1	155	I/O
AD2	154	I/O
AD3	153	I/O
AD4	152	I/O
AD5	151	I/O
AD6	150	I/O
AD7	149	I/O
AD8	148	I/O
AD9	146	I/O
AD10	143	I/O
AD11	142	I/O
AD12	141	I/O
AD13	140	I/O
AD14	139	I/O
AD15	138	I/O
AD16	123	I/O
AD17	122	I/O
AD18	121	I/O
AD19	120	I/O
AD20	119	I/O
AD21	118	I/O
AD22	115	I/O
AD23	114	I/O
AD24	112	I/O
AD25	111	I/O
AD26	109	I/O
AD27	109	I/O
AD28	108	I/O
AD29	107	I/O
AD30	106	I/O
AD31	102	I/O
AEN	193	O
ALT__A20	85	O
ALT__RST#	76	O

Pin Name	Pin #	Type
BALE	23	O
C/BE0#	147	I/O
C/BE1#	137	I/O
C/BE2#	124	I/O
C/BE3#	113	I/O
CPUGNT#	95	t/s/o
CPUREQ#	96	I
DACK0#	45	O
DACK1#	48	O
DACK2#	18	O
DACK3#	49	O
DACK5#	50	O
DACK6#	59	O
DACK7#	63	O
DEVSEL#	128	I/O (s/t/s)
DREQ0	47	I
DREQ1	56	I
DREQ2	57	I
DREQ3	58	I
DREQ5	51	I
DREQ6	61	I
DREQ7	65	I
DSKCHG	161	I
ECSADDR0	175	O
ECSADDR1	174	O
ECSADDR2	173	O
ECSEN#	170	O
EOP	20	I/O
EXTSMI#	171	I
FERR#/IRQ13	71	I
FLSHREQ#	89	t/s/o
FRAME#	125	I/O (s/t/s)
GNT0#/SIOREQ#	92	t/s/o
GNT1#/RESUME#	94	t/s/o
GNT2#	91	t/s/o

Table 1. Alphabetical Pin Assignment (Continued)

Pin Name	Pin #	Type
GNT3#	99	t/s/o
IDSEL	101	I
IGNNE#	72	O
INIT	136	I
INT	75	O
IOCHK#	176	I
IOCHRDY	191	I/O
IOCS16#	33	I
IOR#	200	I/O
IOW#	198	I/O
IRDY#	126	I/O (s/t/s)
IRQ1	168	I
IRQ3	16	I
IRQ4	14	I
IRQ5	11	I
IRQ6	9	I
IRQ7	7	I
IRQ8#	172	I
IRQ9	184	I
IRQ10	35	I
IRQ11	37	I
IRQ12/M	39	I
IRQ14	43	I
IRQ15	41	I
LA17	46	I/O
LA18	44	I/O
LA19	42	I/O
LA20	40	I/O
LA21	38	I/O
LA22	36	I/O
LA23	34	I/O
LOCK#	133	I (s/t/s)
MASTER#	206	I
MEMACK#	88	I
MEMCS#	86	O

Pin Name	Pin #	Type
MEMCS16#	31	I/O (o/d)
MEMR#	203	I/O
MEMREQ#	87	t/s/o
MEMW#	204	I/O
NMI	74	O
OSC	80	I
PAR	135	O
PCICLK	90	I
PCIRST#	163	I
PIRQ0#	81	I
PIRQ1#	82	I
PIRQ2#	83	I
PIRQ3#	84	I
REFRESH#	4	I/O
REQ0#/SIOGNT#	93	I
REQ1#	98	I
REQ2#	97	I
REQ3#	100	I
RSTDRV	177	O
SA0	30	I/O
SA1	29	I/O
SA2	28	I/O
SA3	24	I/O
SA4	22	I/O
SA5	19	I/O
SA6	17	I/O
SA7	15	I/O
SA8	13	I/O
SA9	10	I/O
SA10	8	I/O
SA11	6	I/O
SA12	5	I/O
SA13	3	I/O
SA14	207	I/O
SA15	205	I/O

Table 1. Alphabetical Pin Assignment (Continued)

Pin Name	Pin #	Type
SA16	202	I/O
SA17	201	I/O
SA18	199	I/O
SA19	197	I/O
SBHE#	32	I/O
SD0	190	I/O
SD1	189	I/O
SD2	187	I/O
SD3	186	I/O
SD4	185	I/O
SD5	180	I/O
SD6	179	I/O
SD7	178	I/O
SD8	55	I/O
SD9	60	I/O
SD10	62	I/O
SD11	64	I/O
SD12	67	I/O
SD13	68	I/O
SD14	69	I/O
SD15	70	I/O
SERR#	134	I
SMEMR#	196	O
SMEMW#	192	O
SMI#	160	O
SPKR	73	O
STOP#	132	I/O (s/t/s)
STPCLK#	167	O
SYSCLK	166	O
TEST	169	I
TEST0	21	O
TRDY#	127	I/O (s/t/s)
UBUSOE#	164	O
UBUSTR	165	O

Pin Name	Pin #	Type
ZEROWS#	188	I
V_{DD}	1	V
V_{DD}	79	V
V_{DD}	104	V
V_{DD}	105	V
V_{DD}	116	V
V_{DD}	131	V
V_{DD}	144	V
V_{DD}	156	V
V_{DD}	157	V
V_{DD}	181	V
V_{DD}	25	V
V_{DD}	52	V
V_{DD}	53	V
V_{DD}	195	V
V_{DD}	208	V
V_{SS}	2	V
V_{SS}	12	V
V_{SS}	26	V
V_{SS}	27	V
V_{SS}	54	V
V_{SS}	66	V
V_{SS}	77	V
V_{SS}	78	V
V_{SS}	103	V
V_{SS}	117	V
V_{SS}	129	V
V_{SS}	130	V
V_{SS}	145	V
V_{SS}	158	V
V_{SS}	162	V
V_{SS}	182	V
V_{SS}	183	V
V_{SS}	194	V

Table 2. Numerical Pin Assignment

Pin Name	Pin #	Type
V_{DD}	1	V
V_{SS}	2	V
SA13	3	I/O
REFRESH#	4	I/O
SA12	5	I/O
SA11	6	I/O
IRQ7	7	I
SA10	8	I/O
IRQ6	9	I
SA9	10	I/O
IRQ5	11	I
V_{SS}	12	V
SA8	13	I/O
IRQ4	14	I
SA7	15	I/O
IRQ3	16	I
SA6	17	I/O
DACK2#	18	O
SA5	19	I/O
EOP	20	I/O
TEST0	21	O
SA4	22	I/O
BALE	23	O
SA3	24	I/O
V_{DD}	25	V
V_{SS}	26	V
V_{SS}	27	V
SA2	28	I/O
SA1	29	I/O
SA0	30	I/O
MEMCS16#	31	I/O (o/d)
SBHE#	32	I/O
IOCS16#	33	I
LA23	34	I/O
IRQ10	35	I

Pin Name	Pin #	Type
LA22	36	I/O
IRQ11	37	I
LA21	38	I/O
IRQ12/M	39	I
LA20	40	I/O
IRQ15	41	I
LA19	42	I/O
IRQ14	43	I
LA18	44	I/O
DACK0#	45	O
LA17	46	I/O
DREQ0	47	I
DACK1#	48	O
DACK3#	49	O
DACK5#	50	O
DREQ5	51	I
V_{DD}	52	V
V_{DD}	53	V
V_{SS}	54	V
SD8	55	I/O
DREQ1	56	I
DREQ2	57	I
DREQ3	58	I
DACK6#	59	O
SD9	60	I/O
DREQ6	61	I
SD10	62	I/O
DACK7#	63	O
SD11	64	I/O
DREQ7	65	I
V_{SS}	66	V
SD12	67	I/O
SD13	68	I/O
SD14	69	I/O
SD15	70	I/O

Table 2. Numerical Pin Assignment (Continued)

Pin Name	Pin #	Type
FERR#/IRQ13	71	I
IGNNE#	72	O
SPKR	73	O
NMI	74	O
INT	75	O
ALT_RST#	76	O
V_{SS}	77	V
V_{SS}	78	V
V_{DD}	79	V
OSC	80	I
PIRQ0#	81	I
PIRQ1#	82	I
PIRQ2#	83	I
PIRQ3#	84	I
ALT_A20	85	O
MEMCS#	86	O
MEMREQ#	87	t/s/o
MEMACK#	88	I
FLSHREQ#	89	t/s/o
PCICLK	90	I
GNT2#	91	t/s/o
GNT0#/SIOREQ#	92	t/s/o
REQ0#/SIOGNT#	93	I
GNT1#/RESUME#	94	t/s/o
CPUGNT#	95	t/s/o
CPUREQ#	96	I
REQ2#	97	I
REQ1#	98	I
GNT3#	99	I
REQ3#	100	I
IDSEL	101	I
AD31	102	I/O
V_{SS}	103	V
V_{DD}	104	V
V_{DD}	105	V

Pin Name	Pin #	Type
AD30	106	I/O
AD29	107	I/O
AD28	108	I/O
AD27	109	I/O
AD26	110	I/O
AD25	111	I/O
AD24	112	I/O
C/BE3#	113	I/O
AD23	114	I/O
AD22	115	I/O
V_{DD}	116	V
V_{SS}	117	V
AD21	118	I/O
AD20	119	I/O
AD19	120	I/O
AD18	121	I/O
AD17	122	I/O
AD16	123	I/O
C/BE2#	124	I/O
FRAME#	125	I/O (s/t/s)
IRDY#	126	I/O (s/t/s)
TRDY#	127	I/O (s/t/s)
DEVSEL#	128	I/O (s/t/s)
V_{SS}	129	V
V_{SS}	130	V
V_{DD}	131	V
STOP#	132	I/O (s/t/s)
LOCK#	133	I (s/t/s)
SERR#	134	I
PAR	135	O
INIT	136	I
C/BE1#	137	I/O
AD15	138	I/O
AD14	139	I/O
AD13	140	I/O

Table 2. Numerical Pin Assignment (Continued)

Pin Name	Pin #	Type
AD12	141	I/O
AD11	142	I/O
AD10	143	I/O
V_{DD}	144	V
V_{SS}	145	V
AD9	146	I/O
C/BE0#	147	I/O
AD8	148	I/O
AD7	149	I/O
AD6	150	I/O
AD5	151	I/O
AD4	152	I/O
AD3	153	I/O
AD2	154	I/O
AD1	155	I/O
V_{DD}	156	V
V_{DD}	157	V
V_{SS}	158	V
AD0	159	I/O
SMI#	160	O
DSKCHG	161	I
V_{SS}	162	V
PCIRST#	163	I
UBUSOE#	164	O
UBUSTR	165	O
SYSCLK	166	O
STPCLK#	167	O
IRQ1	168	I
TEST	169	I
ECSEN#	170	O
EXTSMI#	171	I
IRQ8#	172	I
ECSADDR2	173	O
ECSADDR1	174	O

Pin Name	Pin #	Type
ECSADDR0	175	O
IOCHK#	176	I
RSTDRV	177	O
SD7	178	I/O
SD6	179	I/O
SD5	180	I/O
V_{DD}	181	V
V_{SS}	182	V
V_{SS}	183	V
IRQ9	184	I
SD4	185	I/O
SD3	186	I/O
SD2	187	I/O
ZEROWS#	188	I
SD1	189	I/O
SD0	190	I/O
IOCHRDY	191	I/O
SMEMW#	192	O
AEN	193	O
V_{SS}	194	V
V_{DD}	195	V
SMEMR#	196	O
SA19	197	I/O
IOW#	198	I/O
SA18	199	I/O
IOR#	200	I/O
SA17	201	I/O
SA16	202	I/O
MEMR#	203	I/O
MEMW#	204	I/O
SA15	205	I/O
MASTER#	206	I
SA14	207	I/O
V_{DD}	208	V

3.0 SIGNAL DESCRIPTION

This section contains a detailed description of each signal. The signals are arranged in functional groups according to the interface.

Note that the "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used extensively. This is done to avoid confusion when working with a mixture of "active-low" and "active-high" signals. The term **assert**, or **assertion** indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term **negate**, or **negation** indicates that a signal is inactive.

3.1 PCI Bus Interface Signals

Signal Name	Type	Description
PCICLK	I	**PCI CLOCK:** PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Frequencies supported by the SIO include 25 MHz and 33 MHz.
PCIRST#	I	**PCI RESET:** PCIRST# forces the SIO to a known state. AD[31:0], C/BE[3:0]#, and PAR are always driven low by the SIO synchronously from the leading edge of PCIRST#. The SIO always tri-states these signals from the trailing edge of PCIRST#. If the internal arbiter is enabled (CPUREQ# sampled high on the trailing edge of PCIRST#), the SIO will drive these signals low again (synchronously 2–5 PCICLKs later) until the bus is given to another master. If the internal arbiter is disabled (CPUREQ# sampled low on the trailing edge of PCIRST#), these signals remain tri-stated until the SIO is required to drive them valid as a master or slave. FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, MEMREQ#, FLSHREQ#, CPUGNT#, GNT0#/SIOREQ#, and GNT1#/RESUME# are tri-stated from the leading edge of PCIRST#. FRAME#, IRDY#, TRDY#, STOP#, and DEVSEL# remain tri-stated until driven by the SIO as either a master or a slave. MEMREQ#, FLSHREQ#, CPUGNT#, GNT0#/SIOREQ#, and GNT1#/RESUME# are tri-stated until driven by the SIO. After PCIRST#, MEMREQ# and FLSHREQ# are driven inactive asynchronously from PCIRST# inactive. CPUGNT#, GNT0#/SIOREQ#, and GNT1#/RESUME# are driven based on the arbitration scheme and the asserted REQx#'s. All registers are set to their default values. PCIRST# may be asynchronous to PCICLK when asserted or negated. Although asynchronous, negation must be a clean, bounce-free edge. Note that PCIRST# must be asserted for more than 1 μs.

3.1 PCI Bus Interface Signals (Continued)

Signal Name	Type	Description
AD[31:0]	I/O	**PCI ADDRESS/DATA.** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits). During subsequent clocks, AD[31:0] contain data. A SIO Bus transaction consists of an address phase followed by one or more data phases. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). When the SIO is a target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), the SIO may be asked to supply data on AD[31:0] for a PCI read, or accept data for a PCI write. As a master, the SIO drives a valid address on AD[31:2] during the address phase, and drives write or latches read data on AD[31:0] during the data phase. The SIO always drives AD[1:0] low as a master. AD[31:0] are always driven low by the SIO synchronously from the leading edge of PCIRST#. The SIO always tri-states AD[31:0] from the trailing edge of PCIRST#. If the internal arbiter is enabled (CPUREQ# sampled high on the trailing edge of PCIRST#), the SIO drives AD[31:0] low again (synchronously 2–5 PCICLKs later) until the bus is given to another master. If the internal arbiter is disabled (CPUREQ# sampled low on the trailing edge of PCIRST#), AD[31:0] remain tri-stated until the SIO is required to drive them valid as a master or slave. When the internal arbiter is enabled, the SIO acts as the central resource responsible for driving the AD[31:0] signals when no one is granted the PCI Bus and the bus is idle. When the internal arbiter is disabled, the SIO does not drive AD[31:0] as the central resource. The SIO is always responsible for driving AD[31:0] when it is granted the bus (SIOGNT# and idle bus) and as appropriate when it is the master of a transaction.
C/BE[3:0]#	I/O	**BUS COMMAND AND BYTE ENABLES:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE#[0] applies to byte 0, C/BE[1] to byte 1, C/BE[2] to byte 2, and C/BE#[3] to byte 3. The SIO drives C/BE[3:0]# as an initiator of a PCI Bus cycle and monitors C/BE[3:0]# as a Target. C/BE[3:0]# are always driven low by the SIO synchronously from the leading edge of PCIRST#. The SIO always tri-states C/BE[3:0]# from the trailing edge of PCIRST#. If the internal arbiter is enabled (CPUREQ# sampled high on the trailing edge of PCIRST#), the SIO drives C/BE[3:0]# low again (synchronously 2-5 PCICLKs later) until the bus is given to another master. If the internal arbiter is disabled (CPUREQ# sampled low on the trailing edge of PCIRST#), C/BE[3:0]# remain tri-stated until the SIO is required to drive them valid as a master or slave. When the internal arbiter is enabled, the SIO acts as the central resource responsible for driving the C/BE[3:0]# signals when no one is granted the PCI Bus and the bus is idle. When the internal arbiter is disabled, the SIO does not drive C/BE[3:0]# as the central resource. The SIO is always responsible for driving C/BE[3:0]# when it is granted the bus (SIOGNT# and idle bus) and as appropriate when it is the master of a transaction.

3.1 PCI Bus Interface Signals (Continued)

Signal Name	Type	Description
FRAME#	I/O (s/t/s)	**CYCLE FRAME:** FRAME# is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to the SIO when the SIO is the target. FRAME# is an output when the SIO is the initiator. FRAME# is tri-stated from the leading edge of PCIRST#. FRAME# remains tri-stated until driven by the SIO as either a master or a slave.
TRDY#	I/O (s/t/s)	**TARGET READY:** TRDY# indicates the SIO's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the SIO, as a target, has placed valid data on AD[31:0]. During a write, it indicates the SIO, as a target is prepared to latch data. TRDY is an input to the SIO when the SIO is the initiator and an output when the SIO is a target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated until driven by the SIO as either a master or a slave.
IRDY#	I/O (s/t/s)	**INITIATOR READY:** IRDY# indicates the SIO's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock that both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the SIO has valid data present on AD[31:0]. During a read, it indicates the SIO is prepared to latch data. IRDY is an input to the SIO when the SIO is the target and an output when the SIO is an initiator. IRDY# is tri-stated from the leading edge of PCIRST#. IRDY# remains tri-stated until driven by the SIO as either a master or a slave.
STOP#	I/O (s/t/s)	**STOP:** STOP# indicates that the SIO, as a target, is requesting a master to stop the current transaction. As a master, STOP# causes the SIO to stop the current transaction. STOP# is an output when the SIO is a target and an input when the SIO is an initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by the SIO as either a master or a slave.
LOCK#	I	**LOCK:** LOCK# indicates an atomic operation that may require multiple transactions to complete. LOCK# is always an input to the SIO. When the SIO is the target of a transaction and samples LOCK# negated during the address phase of a transaction, the SIO considers itself a locked resource until it samples LOCK# and FRAME# negated. When other masters attempt accesses while the SIO is locked, the SIO responds with a retry termination. LOCK# is tri-stated during reset.
IDSEL	I	**INITIALIZATION DEVICE SELECT:** IDSEL is used as a chip select during configuration read and write transactions. The SIO samples IDSEL during the address phase of a transaction. If IDSEL is sampled active, and the bus command is a configuration read or write, the SIO responds by asserting DEVSEL# on the next cycle.
DEVSEL#	I/O (s/t/s)	**DEVICE SELECT:** The SIO asserts DEVSEL# to claim a PCI transaction through positive or subtractive decoding. As an output, the SIO asserts DEVSEL# when it samples IDSEL active in configuration cycles to SIO configuration registers. The SIO also asserts DEVSEL# when an internal SIO address is decoded or when the SIO subtractively decodes a cycle. As an input, DEVSEL# indicates the response to a SIO master-initiated transaction. The SIO also samples this signal for all PCI transactions to decide to subtractively decode the cycle. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated until driven by the SIO as either a master or a slave.

3.1 PCI Bus Interface Signals (Continued)

Signal Name	Type	Description
PIRQ[3:0]#	I	**PCI INTERRUPT REQUEST:** PIRQ#s are used to generate asynchronous interrupts to the CPU via the Programmable Interrupt Controllers (82C59s) integrated in the SIO. These signals are defined as level sensitive and are asserted low. The PIRQx# interrupts can be steered into any unused IRQ interrupt. The PIRQx# Route Control Register determines which IRQ interrupt each PCI interrupt is steered into. These pins include a weak internal pull-up resistor.
PAR	O	**CALCULATED PARITY SIGNAL:** PAR is "even" parity and is calculated on 36 bits—AD[31:0] plus C/BE[3:0]#. "Even" parity means that the number of "1"s within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and tri-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all SIO master transactions. It is also an output during the data phase (delayed one clock) when the SIO is the master of a PCI write transaction, and when it is the target of a read transaction. PAR is always driven low by the SIO synchronously from the leading edge of PCIRST#. The SIO always tri-states PAR from the trailing edge of PCIRST#. If the internal arbiter is enabled (CPUREQ# sampled high on the trailing edge of PCIRST#), the SIO drives PAR low again (synchronously 2-5 PCICLKs later) until the bus is given to another master. If the internal arbiter is disabled (CPUREQ# sampled low on the trailing edge of PCIRST#), PAR remains tri-stated until the SIO is required to drive them valid as a master or slave. When the internal arbiter is enabled, the SIO acts as the central resource responsible for driving PAR when no device is granted the PCI Bus and the bus is idle. When the internal arbiter is disabled, the SIO does not drive PAR as the central resource. The SIO is always responsible for driving PAR when it is granted the bus (SIOGNT# and idle bus) and as appropriate when it is the master of a transaction.
SERR#	I	**SYSTEM ERROR:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the SIO generates a non-maskable interrupt (NMI) to the CPU.

3.2 PCI Arbiter Signals

Signal Name	Type	Description
CPUREQ#	I	**CPU REQUEST:** This signal provides the following functions: 1. If CPUREQ# is sampled high on the trailing edge of PCIRST#, the internal arbiter is enabled. If CPUREQ# is sampled low on the trailing edge of PCIRST#, the internal arbiter is disabled. This requires that the host bridge drive CPUREQ# high during PCIRST#. 2. If the SIO's internal arbiter is enabled, this pin is configured as CPUREQ#. An active low assertion indicates that the CPU initiator desires the use of the PCI Bus. If the internal arbiter is disabled, this pin is meaningless after reset. This pin has a weak internal pull-up resistor.
REQ0#/ SIOGNT#	I	**REQUEST 0/SIO GRANT:** If the SIO's internal arbiter is enabled, this pin is configured as REQ0#. An active low assertion indicates that Initiator0 desires the use of the PCI Bus. If the internal arbiter is disabled, this pin is configured as SIOGNT#. When asserted, SIOGNT# indicates that the external PCI arbiter has granted use of the bus to the SIO. This pin has a weak internal pull-up resistor.
REQ1#	I	**REQUEST 1:** If the SIO's internal arbiter is enabled through the Arbiter Configuration Register, then this signal is configured as REQ1#. An active low assertion indicates that Initiator1 desires the use of the PCI Bus. If the internal arbiter is disabled, the SIO ignores REQ1# after reset. This pin has a weak internal pull-up resistor.
CPUGNT#	t/s/o	**CPU GRANT:** If the SIO's internal arbiter is enabled, this pin is configured as CPUGNT#. The SIO's internal arbiter asserts CPUGNT# to indicate that the CPU initiator has been granted the PCI Bus. If the internal arbiter is disabled, this signal is meaningless. CPUGNT# is tri-stated from the leading edge of PCIRST#. CPUGNT# is tri-stated until driven by the SIO. CPUGNT# is driven based on the arbitration scheme and the asserted REQx#'s.
GNT0#/ SIOREQ#	t/s/o	GRANT 0/SIO REQUEST: If the SIO's internal arbiter is enabled, this pin is configured as GNT0#. The SIO's internal arbiter asserts GNT0# to indicate that Initiator0 has been granted the PCI Bus. If the internal arbiter is disabled, this pin is configured as SIOREQ#. The SIO asserts SIOREQ# to request the PCI Bus. GNT0#/SIOREQ# is tri-stated from the leading edge of PCIRST#. GNT0#/SIOREQ# is tri-stated until driven by the SIO. GNT0#/SIOREQ# is driven based on the arbitration scheme and the asserted REQx#'s.
GNT1#/ RESUME#	t/s/o	**GRANT 1/RESUME:** If the SIO's internal arbiter is enabled, this pin is configured as GNT1#. The SIO's internal arbiter asserts GNT1# to indicate that Initiator1 has been granted the PCI Bus. If the internal arbiter is disabled, this pin is configured as RESUME#. The SIO asserts RESUME# to indicate that the conditions causing the SIO to retry the cycle has passed. GNT1#/RESUME# is tri-stated from the leading edge of PCIRST#. GNT1#/RESUME# is tri-stated until driven by the SIO. GNT1#/RESUME# is driven based on the arbitration scheme and the asserted REQx#'s.
REQ2#	I	**REQUEST 2:** This pin is an active low signal that indicates that Initiator2 desires the use of the PCI Bus. This signal has a weak internal pull-up resistor.

3.2 PCI Arbiter Signals (Continued)

Signal Name	Type	Description
REQ3#	I	**REQUEST 3:** This pin is an active low signal that indicates that Initiator3 desires the use of the PCI Bus. This signal has a weak internal pull-up resistor.
GNT2#	t/s/o	**GRANT 2:** This pin is configured as GNT2#. The SIO's internal arbiter asserts GNT2# to indicate that Initiator2 has been granted the PCI Bus. GNT2# is high upon reset.
GNT3#	t/s/o	**GRANT 3:** This pin is configured as GNT3#. The SIO's internal arbiter asserts GNT3# to indicate that Initiator3 has been granted the PCI Bus. GNT3# is high upon reset.
MEMREQ#	t/s/o	**MEMORY REQUEST:** If the SIO is configured in Guaranteed Access Time (GAT) Mode, MEMREQ# will be asserted when an ISA master or DMA is requesting the ISA Bus (along with FLSHREQ#) to indicate that the SIO requires ownership of the main memory. MEMREQ# is tri-stated from the leading edge of PCIRST#. MEMREQ# remains tri-stated until driven by the SIO. After PCIRST, MEMREQ# is driven inactive asynchronously from PCIRST# inactive. The SIO asserts FLSHREQ# concurrently with asserting MEMREQ#. **FLSHREQ# / MEMREQ# / Meaning** 1 / 1 / Idle 0 / 1 / Flush buffers pointing towards PCI to avoid ISA deadlock 1 / 0 / Reserved 0 / 0 / GAT mode. Guarantee PCI Bus immediate access to main memory (this may or may not require the PCI-to-main memory buffers to be flushed first depending on the number of buffers).
FLSHREQ#	t/s/o	**FLUSH REQUEST:** FLSHREQ# is generated by the SIO to command all of the system's posted write buffers pointing towards the PCI Bus to be flushed. This is required before granting the ISA Bus to an ISA master or the DMA. FLSHREQ# is tri-stated from the leading edge of PCIRST#. FLSHREQ# remains tri-stated until driven by the SIO. After PCIRST, FLSHREQ# is driven inactive asynchronously from PCIRST# inactive.
MEMACK#	I	**MEMORY ACKNOWLEDGE:** MEMACK# is the response handshake that indicates to the SIO that the function requested over the MEMREQ# and/or FLSHREQ# signals has been completed. In GAT mode (MEMREQ# and FLSHREQ# asserted), the main memory bus is dedicated to the PCI Bus and the system's posted write buffers pointing towards the PCI Bus have been flushed and are disabled. In non-GAT mode (FLSHREQ# asserted alone), this means the system's posted write buffers have been flushed and are disabled. In either case, the SIO can now grant the ISA Bus to the requester.

3.3 Address Decoder Signal

Signal Name	Type	Description
MEMCS#	O	**MEMORY CHIP SELECT:** MEMCS# is a programmable address decode signal provided to a Host CPU bridge. A CPU bridge can use MEMCS# to forward a PCI cycle to main memory behind the bridge. MEMCS# is driven one PCI clock after FRAME# is sampled active (address phase) and is valid for one clock cycle before going inactive. MEMCS# is high upon reset.

3.4 Power Management Signals

Signal Name	Type	Description
SMI#	O	**SYSTEM MANAGEMENT INTERRUPT:** SMI# is an active low output that is asserted by the SIO in response to one of many enableable hardware or software events. SMI# connects directly to the CPU. The SMI# signal is an asychronous input to the CPU. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system. The CPU responds by entering SMM (System Management Mode). SMI# is deasserted during and following reset.
STPCLK#	O	**STOP CLOCK:** STPCLK# is an active low output that is asserted by the SIO in response to one of many enableable hardware or software events. STPCLK# connects directly to the CPU. The STPCLK# signal is an asynchronous input to the CPU. When the CPU samples STPCLK# asserted it responds by stopping its internal clock. STPCLK# is deasserted during and following reset.
EXTSMI#	I	**EXTERNAL SYSTEM MANAGEMENT INTERRUPT:** EXTSMI# is a falling edge triggered input to the SIO indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# will result in the assertion of the SMI# signal to the CPU. EXTSMI# is an asychronous input to the SIO. However, when the setup and hold times are met, it is only required to be asserted for one PCICLK. Once deasserted, it must remain deasserted for at least four PCICLKs in order to allow the edge detect logic to reset. This pin includes a weak internal pull-up resistor.
INIT	I	**INIT:** INIT is an input to the SIO indicating that the CPU is actually being soft reset. It is connected to the INIT pin of the CPU. This pin includes a weak internal pull-up resistor.

3.5 ISA Interface Signals

Signal Name	Type	Description
AEN	O	**ADDRESS ENABLE:** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA Bus that a DMA transfer is occurring. This signal is also driven high during refresh cycles. AEN is driven low upon reset.

3.5 ISA Interface Signals (Continued)

Signal Name	Type	Description
BALE	O	**BUS ADDRESS LATCH ENABLE:** BALE is an active high signal asserted by the SIO to indicate that the address (SA[19:0], LA[23:17]), AEN and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. BALE is driven low upon reset.
SYSCLK	O	**SYSTEM CLOCK:** SYSCLK is an output of the SIO component. The frequencies supported are 6 MHz to 8.33 MHz.
IOCHRDY	I/O	**I/O CHANNEL READY:** Resources on the ISA Bus assert IOCHRDY to indicate that additional time (wait-states) is required to complete the cycle. This signal is normally high on the ISA Bus. IOCHRDY is an input when the SIO owns the ISA Bus and a PCI agent is accessing an ISA slave or during compatible DMA transfers (compatible cycles only). IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing a PCI slave or an SIO register. As an SIO output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or the SIO latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, the SIO floats IOCHRDY. The 70 ns includes both the drive time and the time it takes the SIO to float IOCHRDY. The SIO does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. IOCHRDY is tri-stated upon reset.
IOCS16#	I	**16-BIT I/O CHIP SELECT:** This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles.
IOCHK#	I	**I/O CHANNEL CHECK:** IOCHK# can be driven by any resource on the ISA Bus. When asserted, it indicates that a parity or an un-correctable error has occurred for a device or memory on the ISA Bus. A NMI will be generated to the CPU if the NMI generation is enabled.
IOR#	I/O	**I/O READ:** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when the SIO owns the ISA Bus. IOR# is an input when an external ISA master owns the ISA Bus. IOR# is driven high upon reset.
IOW#	I/O	**I/O WRITE:** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when the SIO owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. IOW# is driven high upon reset.
LA[23:17]	I/O	**UNLATCHED ADDRESS:** The LA[23:17] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA Bus up to 16 MBytes. LA[23:17] are outputs when the SIO owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. These signals are undefined during DMA type "A", "B", and "F" cycles. The LA[23:17] signals are at an unknown state upon reset.
SA[19:0]	I/O	**SYSTEM ADDRESS BUS:** These bi-directional address lines define the selection with the granularity of one byte within the one Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used. SA[19:0] are outputs when the SIO owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. SA[19:0] are undefined during DMA type "A", 'B", or "F" cycles. SA[19:0] are at an unknown state upon reset.

3.5 ISA Interface Signals (Continued)

Signal Name	Type	Description
SBHE#	I/O	**SYSTEM BYTE HIGH ENABLE:** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when the SIO owns the ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. SBHE# is at an unknown state upon reset.
MEMCS16#	OD	**MEMORY CHIP SELECT 16:** MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. The SIO ignores MEMCS16# during I/O access cycles and refresh cycles. During DMA cycles, this signal is only used by the byte swap logic. MEMCS16# is an input when the SIO owns the ISA Bus. MEMCS16# is an output when an ISA Bus master owns the ISA Bus. The SIO drives this signal low during ISA master to PCI memory cycles. MEMCS16# is at an unknown state upon reset.
MASTER#	I	**MASTER:** An ISA Bus master asserts MASTER# to indicate that it has control of the ISA Bus. Before the ISA master can assert MASTER#, it must first sample DACK# active. Once MASTER# is asserted, the ISA master has control of the ISA Bus until it negates MASTER#.
MEMR#	I/O	**MEMORY READ:** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when the SIO is a master on the ISA Bus. MEMR# is an input when an ISA master, other than the SIO, owns the ISA Bus. This signal is also driven by the SIO during refresh cycles. For compatible timing mode DMA cycles, the SIO, as a master, asserts MEMR# if the address is less than 16 MBytes. This signal is not generated for accesses to addresses greater than 16 MByte. MEMR# is not driven active during DMA type "A", "B", or "F" cycles.
MEMW#	I/O	**MEMORY WRITE:** MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when the SIO owns the ISA Bus. MEMW# is an input when an ISA master, other than the SIO, owns the ISA Bus. For compatible timing mode DMA cycles, the SIO, as a master, asserts MEMW# if the address is less than 16 MBytes. This signal is not generated for accesses to addresses greater than 16 MByte. MEMW# is not driven active during DMA type "A", "B", or "F" cycles.
SMEMW#	O	**SYSTEM MEMORY WRITE:** The SIO asserts SMEMW# to request a memory slave to accept data from the data lines. If the access is below the 1 MByte range (00000000h–000FFFFFh) during DMA compatible, SIO master, or ISA master cycles, the SIO asserts SMEMW#. SMEMW# is a delayed version of MEMW#. SMEMW# is driven high upon reset.
SMEMR#	O	**SYSTEM MEMORY READ:** The SIO asserts SMEMR# to request a memory slave to accept data from the data lines. If the access is below the 1 MByte range (00000000h–000FFFFFh) during DMA compatible, SIO master, or ISA master cycles, the SIO asserts SMEMR#. SMEMR# is a delay version of MEMR#. Upon PCIRST# this signal is low. SMEMR# is driven high upon reset.

3.5 ISA Interface Signals (Continued)

Signal Name	Type	Description
ZEROWS#	I	**ZERO WAIT-STATES:** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles. If IOCHRDY and ZEROWS# are both asserted during the same clock, then ZEROWS# is ignored and wait states are added as a function of IOCHRDY (i.e., IOCHRDY has precedence over ZEROWS#).
OSC	I	**OSCILLATOR:** OSC is the 14.31818 MHz ISA clock signal. It is used by the internal 8254 Timer, counters 0, 1, and 2.
RSTDRV	O	**RESET DRIVE:** The SIO asserts RSTDRV to reset devices that reside on the ISA Bus. The SIO asserts this signal when PCIRST# (PCI Reset) is asserted. In addition, the SIO can be programmed to assert RSTDRV by writing to the ISA Clock Divisor Register. Software should assert the RSTDRV during configuration to reset the ISA Bus when changing the clock divisor. Note that when RSTDRV is generated via the ISA Clock Divisor Register, software must ensure that RSTDRV is driven active for a minimum of 1 μs.
SD[15:0]	I/O	**System DATA:** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. The SIO tri-states SD[15:0] during reset.

3.6 DMA Signals

Signal Name	Type	Description
DREQ [3:0,7:5]	I	**DMA REQUEST:** The DREQ lines are used to request DMA service from the SIO's DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA Command Register (bit 6). When the bit 6 = 0, DREQ[3:0,7:5] are active high and when bit 6 = 1, the signals are active low. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACK signal is asserted.
DACK# [3:0,7:5]	O	**DMA ACKNOWLEDGE:** The DACK output lines indicate that a request for DMA service has been granted by the SIO or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA Command Register (bit 7). When bit 7 = 0, DACK# [3:0,7:5] are active low and when bit 7 = 1, the signals are active high. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER#. If the DMA controller has been programmed for a timing mode other than compatible mode, and another device has requested the bus, and a 4 μs time has elapsed, this line will be negated and the transfer stopped before the transfer is complete. In this case, the transfer is re-started at the next arbitration period that the channel wins the bus. Upon PCIRST#, these lines are set inactive (high).

3.6 DMA Signals (Continued)

Signal Name	Type	Description
EOP	I/O	**END OF PROCESS:** EOP is bi-directional, acting in one of two modes, and is directly connected to the TC line of the ISA Bus. DMA slaves assert EOP to the SIO to terminate DMA cycles. The SIO asserts EOP to DMA slaves as a terminal count indicator. **EOP-IN MODE:** For all transfer types during DMA, the SIO samples EOP. If it is sampled asserted, the transfer is terminated. **TC-OUT MODE:** The SIO asserts EOP after a new address has been output, if the byte count expires with that transfer. The EOP (TC) remains asserted until AEN is negated, unless AEN is negated during an autoinitialization. EOP (TC) is negated before AEN is negated during an autoinitialization. When all the DMA channels are not in use, the EOP signal is in output mode and negated (low). After PCIRST#, EOP is in output mode and inactive.
REFRESH#	I/O	**REFRESH:** As an output, REFRESH# is used by the SIO to indicate when a refresh cycle is in progress. It should be used to enable the SA[15:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when the SIO DMA refresh is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. Upon PCIRST#, this signal is tri-stated.

3.7 Timer Signal

Signal Name	Type	Description
SPKR	O	**SPEAKER DRIVE:** The SPKR signal is the output of counter 2 and is "ANDed" with Port 061h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the ISA system speaker. SPKR has a 24 mA drive capability. Upon reset, its output state is 0.

3.8 Interrupt Controller Signals

Signal Name	Type	Description
IRQ[15,14, 11:9, 7:3,1]	I	**INTERRUPT REQUEST:** The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU. The assertion mode of these inputs depends on the programming of LTIM, bit 3 of ICW1 on both Controller-1 and Controller-2. When LTIM is programmed to a 0, a low-to-high transition on any of that controller's IRQ lines is recognized as an interrupt request. This is "edge-triggered" mode. Edge-triggered mode is the SIO default. When LTIM is programmed to a 1, a high level on any of that controller's IRQ lines is recognized as an interrupt request. This mode is "level-triggered" mode. Upon PCIRST#, the IRQ lines are placed in edge-triggered mode. An active IRQ input must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a DEFAULT IRQ7 occurs when the CPU acknowledges the interrupt. **NOTE:** Refer to the Utility Bus Signal descriptions for IRQ12 and IRQ13 signal descriptions.
IRQ8#	I	**INTERRUPT REQUEST EIGHT SIGNAL:** IRQ8# is an active low interrupt input. The assertion mode of this input depends on the programming of the LTIM bit of ICW1 on both Controller-1 and Controller-2. When the LTIM = 0, a high-to-low transition on IRQ8# is recognized as an interrupt request. This is "edge-triggered" mode. Edge triggered mode is the SIO default. When the LTIM = 1, a low level on IRQ8# is recognized as an interrupt request. This mode is "level-triggered" mode. Upon PCIRST#, IRQ8# will be placed in edge-triggered mode. IRQ8# must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a DEFAULT IRQ7 will occur when the CPU acknowledges the interrupt.
INT	O	**CPU INTERRUPT:** INT is driven by the SIO to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following a reset to ensure that INT is at a known state. Upon PCIRST#, INT is driven low.
NMI	O	**NON-MASKABLE INTERRUPT:** NMI is used to force a non-maskable interrupt to the CPU. The SIO generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real-Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low.

3.9 Utility Bus Signals

Signal Name	Type	Description
UBUSTR	O	**UTILITY DATA BUS TRANSMIT/RECEIVE:** UBUSTR is tied directly to the direction control of a 74F245 that buffers the utility data bus, UD[7:0]. UBUSTR is asserted for all I/O read cycles (regardless if a Utility Bus device has been decoded). UBUSTR is asserted for memory cycles only if BIOS space has been decoded. For PCI and ISA master-initiated read cycles, UBUSTR is asserted from the falling edge of either IOR# or MEMR#, depending on the cycle type (driven from MEMR# only if BIOS space has been decoded). When the rising edge of IOR# or MEMR# occurs, the SIO negates UBUSTR. For DMA read cycles from the Utility Bus, UBUSTR is asserted when DACKx# is asserted and negated when DACKx# is negated. At all other times, UBUSTR is negated. Upon PCIRST#, this signal is driven low.
UBUSOE#	O	**UTILITY DATA BUS OUTPUT ENABLE:** UBUSOE# is tied directly to the output enable of a 74F245 that buffers the utility data bus, UD[7:0], from the system data bus, SD[7:0]. UBUSOE# is asserted anytime a SIO supported Utility Bus device is decoded, and the devices decode is enabled in the Utility Bus Chip Select Enable Registers. UBUSOE# is asserted from the falling edge of the ISA commands (IOR#, IOW#, MEMR#, or MEMW#) for PCI and ISA master-initiated cycles. UBUSOE# is negated from the rising edge of the ISA command signals for SIO-initiated cycles and the SA[16:0] and LA[23:17] address for ISA master-initiated cycles. For DMA cycles, UBUSOE# is asserted when DACK2# is asserted and negated when DACK2# negated. UBUSOE# is not driven active under the following conditions: **NOTES:** 1. During an I/O access to the floppy controller, if DSKCHG is sampled low at reset. 2. If the Digital Output Register is programmed to ignore DACK2#. 3. During an I/O read access to floppy location 3F7h (primary) or 377h (secondary), if the IDE decode space is disabled (i.e. IDE is not resident on the Utility Bus). 4. During any access to a utility bus peripheral in which its decode space has been disabled. Upon a PCIRST#, this signal is driven inactive (high).
ECSADDR [2:0]	O	**ENCODED CHIP SELECTS:** ECSADDR[2:0] are the encoded chip selects and/or control signals for the Utility Bus peripherals supported by the SIO. The binary code formed by the three signals indicates which Utility Bus device is selected. These signals tie to the address inputs of two external 74F138 decoder chips and are driven valid/invalid from the SA[16:0] and LA[23:17] address lines. Upon PCIRST#, these signals are driven high.
ECSEN#	O	**ENCODED CHIP SELECT ENABLE:** ECSEN# is used to determine which of the two external 74F138 decoders is to be selected. ECSEN# is driven low to select decoder 1 and driven high to select decoder 2. This signal is driven valid/invalid from the SA[16:0] and LA[23:17] address lines (except for the generation of RTCALE#, in which case, ECSEN# is driven active based on IOW# falling, and remains active for two SYSCLKs). During a non-valid address or during an access not targeted for the Utility Bus, this signal is driven high. Upon PCIRST#, this signal is driven high.

3.9 Utility Bus Signals (Continued)

<table>
<tr><th>Signal Name</th><th>Type</th><th>Description</th></tr>
<tr><td>ALT_RST#</td><td>O</td><td>ALTERNATE RESET: ALT_RST# is used to reset the CPU under program control. This signal is AND'ed together externally with the reset signal (KBDRST#) from the keyboard controller to provide a software means of resetting the CPU. This provides a faster means of reset than is provided by the keyboard controller. Writing a 1 to bit 0 in the Port 92 Register causes this signal to pulse low for approximately 4 SYSCLKs. Before another ALT_RST# pulse can be generated, bit 0 must be set to 0. Upon PCIRST#, this signal is driven inactive high (bit 0 in the Port 92 Register is set to 0).</td></tr>
<tr><td>ALT_A20</td><td>O</td><td>ALTERNATE A20: ALT_A20 is used to force A20M# to the CPU low for support of real mode compatible software. This signal is externally OR'ed with the A20GATE signal from the keyboard controller and CPURST to control the A20M# input of the CPU. Writing a 0 to bit 1 of the Port 92 Register forces ALT_A20 low. ALT_A20 low drives A20M# to the CPU low, if A20GATE from the keyboard controller is also low. Writing a 1 to bit 1 of the Port 92 Register force ALT_A20 high. ALT_A20 high drives A20M# to the CPU high, regardless of the state of A20GATE from the keyboard controller. Upon reset, this signal is driven low.</td></tr>
<tr><td>DSKCHG</td><td>I</td><td>DISK CHANGE: DSKCHG is tied directly to the DSKCHG signal of the floppy controller. This signal is inverted and driven on SD7 during I/O read cycles to floppy address locations 3F7h (primary) or 377h (secondary) as shown in the table below. Note that the primary and secondary locations are programmed in the Utility Bus Address Decode Enable/Disable Register "A".
<table>
<tr><th>FLOPPYCS# Decode</th><th>IDECSx# Decode</th><th>State of SD7 (output)</th><th>State of UBUSOE#</th></tr>
<tr><td>Enabled</td><td>Enabled</td><td>Tri-stated</td><td>Enabled</td></tr>
<tr><td>Enabled</td><td>Disabled</td><td>Driven via DSKCHG</td><td>Disabled</td></tr>
<tr><td>Disabled</td><td>Enabled</td><td>Tri-stated</td><td>Enabled (note)</td></tr>
<tr><td>Disabled</td><td>Disabled</td><td>Tri-stated</td><td>Disabled</td></tr>
</table>
NOTE:
For this mode to be supported, extra logic is required to disable the U-bus transceiver for accesses to 3F7/377. This is necessary because of potential contention between the Utility Bus buffer and a floppy on the ISA Bus driving the system bus at the same time during shared I/O accesses.

This signal is also used to determine if the floppy controller is present on the Utility Bus. It is sampled on the trailing edge of PCIRST#, and if high, the Floppy is present. For systems that do not support a Floppy via the SIO, this pin should be strapped low. If sampled low, the SD7 function, UBUSOE#, and ECSADDR[2:0] signals will not be enabled for DMA or programmed I/O accesses to the floppy disk controller. This condition overrides the floppy decode enable bits in the Utility Bus Chip Select A.</td></tr>
</table>

3.9 Utility Bus Signals (Continued)

Signal Name	Type	Description
FERR#/ IRQ13	I	**NUMERIC COPROCESSOR ERROR/IRQ13:** This signal has two separate functions, depending on bit 5 in the ISA Clock Divisor Register. This pin functions as a FERR# signal supporting coprocessor errors, if this function is enabled (bit 5 = 1), or as an external IRQ13, if the coprocessor error function is disabled (bit 5 = 0). If programmed to support coprocessor error reporting, this signal is tied to the coprocessor error signal on the CPU. If FERR# is asserted by the coprocessor inside the CPU, the SIO generates an internal IRQ13 to its interrupt controller unit. The SIO then asserts the INT output to the CPU. Also, in this mode, FERR# gates the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active. When FERR# is asserted, the SIO asserts INT to the CPU as an IRQ13. IRQ13 continues to be asserted until a write to F0h has been detected. If the Coprocessor error reporting is disabled, FERR# can be used by the system as IRQ13. Upon PCIRST#, this signal provides the standard IRQ13 function. This signal should be pulled high with an external 8.2 KΩ pull-up resistor if the IRQ13 mode is used or the pin is left floating.
IGNNE#	O	**IGNORE ERROR:** This signal is connected to the ignore error pin of the CPU. IGNNE# is only used if the SIO coprocessor error reporting function is enabled in the ISA Clock Divisor Register (bit 5 = 1). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# is not asserted. IGNNE# is driven high upon a reset.
IRQ12/M	I	**INTERRUPT REQUEST/MOUSE INTERRUPT:** In addition to providing the standard interrupt function as described in the pin description for IRQ[15,14, 11:9, 7:3, 1], this pin also provides a mouse interrupt function. Bit 4 in the ISA Clock Divisor Register determines the functionality of IRQ12/M. When bit 4 = 0, the standard interrupt function is provided and this pin can be tied to the ISA connector. When bit 4 = 1, the mouse interrupt function is provided and this pin can be tied to the DIRQ12 output of the keyboard controller. When the mouse interrupt function is selected, a low to high transition on this signal is latched by the SIO and an INT is generated to the CPU as IRQ12. An interrupt will continue to be generated until a PCIRST# or an I/O read access to address 60h (falling edge of IOR#) is detected. After a PCIRST#, this pin provides the standard IRQ12 function.

3.10 Test Signals

Signal Name	Type	Description
TEST	I	**TEST:** The TEST signal is used to tri-state all of the SIO outputs. During normal operation, this input should be tied to ground.
TESTO	O	**TEST OUTPUT:** This is the output pin used during NAND tree testing.

4.0 REGISTER DESCRIPTION

The SIO contains both PCI configuration registers and non-configuration registers. The configuration registers (Table 3) are located in PCI configuration space and are only accessible from the PCI Bus. Addresses for configuration registers are offset values that appear on AD[7:2] and C/BE#[3:0]. The configuration registers (Section 4.1) can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the fields).

The non-configuration registers (Table 4) include DMA Registers (Section 4.2), Timer Registers (Section 4.3), Interrupt Controller Registers (Section 4.4), and Control Registers (Section 4.5). All of these registers are accessible from the PCI Bus. In addition, some of the registers are accessible from the ISA Bus. Table 4 indicates the bus access for each register. Except for the DMA scatter/gather registers and the BIOS timer registers, the non-configuration registers can only be accessed as byte quantities. If a PCI master attempts a multi-byte access (i.e., more than one Byte Enable signal asserted), the SIO responds with a target-abort. The scatter/gather registers and BIOS timer registers can be accessed as Byte, Word, or Dword quantities.

Some of the SIO configuration and non-configuration registers contain reserved bits. These bits are labeled "Reserved". Software must take care to deal correctly with bit-encoded fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions, and the data then written back.

In addition to reserved bits within a register, the SIO contains address locations in the PCI configuration space that are marked "Reserved" (Table 3). The SIO responds to accesses to these address locations by completing the PCI cycle. However, reads of reserved address locations yield all zeroes and writes have no affect on the SIO.

The SIO, upon receiving a hard reset (PCIRST# signal), sets its internal registers to pre-determined **default** states. The default values are indicated in the individual register descriptions.

Table 3. Configuration Registers

Configuration Offset	Register	Register Access	Bus Access
00h–01h	Vendor Identification	RO	PCI Only
02h–03h	Device Identification	RO	PCI Only
04h–05h	Command	R/W	PCI Only
06h–07h	Device Status	R/W	PCI Only
08h	Revision Identification	RO	PCI Only
09h–3Fh	Reserved	—	PCI Only
40h	PCI Control	R/W	PCI Only
41h	PCI Arbiter Control	R/W	PCI Only
42h	PCI Arbiter Priority Control	R/W	PCI Only
43h	PCI Arbiter Priority Control Extension Register	R/W	PCI Only
44h	MEMCS# Control	R/W	PCI Only
45h	MEMCS# Bottom of Hole	R/W	PCI Only
46h	MEMCS# Top of Hole	R/W	PCI Only
47h	MEMCS# Top of Memory	R/W	PCI Only
48h	ISA Address Decoder Control	R/W	PCI Only
49h	ISA Address Decoder ROM Block Enable	R/W	PCI Only
4Ah	ISA Address Decoder Bottom of Hole	R/W	PCI Only
4Bh	ISA Address Decoder Top of Hole	R/W	PCI Only
4Ch	ISA Controller Recovery Timer	R/W	PCI Only
4Dh	ISA Clock Divisor	R/W	PCI Only
4Eh	Utility Bus Chip Select Enable A	R/W	PCI Only
4Fh	Utility Bus Chip Select Enable B	R/W	PCI Only
50h–53h	Reserved	—	PCI Only
54h	MEMCS# Attribute Register #1	R/W	PCI Only
55h	MEMCS# Attribute Register #2	R/W	PCI Only
56h	MEMCS# Attribute Register #3	R/W	PCI Only
57h	Scatter/Gather Relocation Base Address	R/W	PCI Only
58h–5Fh	Reserved	—	PCI Only

Table 3. Configuration Registers (Continued)

Configuration Offset	Register	Register Access	Bus Access
60h	PIRQ0# Route Control	R/W	PCI Only
61h	PIRQ1# Route Control	R/W	PCI Only
62h	PIRQ2# Route Control	R/W	PCI Only
63h	PIRQ3# Route Control	R/W	PCI Only
64h–7Fh	Reserved	—	PCI Only
80h–81h	BIOS Timer Base Address	R/W	PCI Only
82h–9Fh	Reserved	—	PCI Only
A0h	SMI Control (SMICNTL)	R/W	PCI Only
A1h	Reserved	—	PCI Only
A2h–A3h	SMI Enable (SMIEN)	R/W	PCI Only
A4h–A7h	System Event Enable (SEE)	R/W	PCI Only
A8h	Fast Off Timer (FTMR)	R/W	PCI Only
A9h	Reserved	—	PCI Only
AAh–ABh	SMI Request (SMIREQ)	R/W	PCI Only
ACh	Clock Throttle STPCLK# Low Timer (CTLTMRL)	R/W	PCI Only
ADh	Reserved	—	PCI Only
AEh	Clock Throttle STPCLK# High Timer (CTLTMRH)	R/W	PCI Only
AFh–FFh	Reserved	—	PCI Only

Table 4. Non-Configuration Registers

Address	Function Unit	Register	Register Access	Bus Access
0000h	DMA	DMA1 CH0 Base and Current Address	R/W	PCI Only
0001h	DMA	DMA1 CH0 Base and Current Count	R/W	PCI Only
0002h	DMA	DMA1 CH1 Base and Current Address	R/W	PCI Only
0003h	DMA	DMA1 CH1 Base and Current Count	R/W	PCI Only
0004h	DMA	DMA1 CH2 Base and Current Address	R/W	PCI Only
0005h	DMA	DMA1 CH2 Base and Current Count	R/W	PCI Only
0006h	DMA	DMA1 CH3 Base and Current Address	R/W	PCI Only
0007h	DMA	DMA1 CH3 Base and Current Count	R/W	PCI Only
0008h	DMA	DMA1 Status(R) Command(W)	R/W	PCI Only
0009h	DMA	DMA1 Write Request	WO	PCI Only
000Ah	DMA	DMA1 Write Single Mask Bit	WO	PCI Only
000Bh	DMA	DMA1 Write Mode	WO	PCI Only
000Ch	DMA	DMA1 Clear Byte Pointer	WO	PCI Only
000Dh	DMA	DMA1 Master Clear	WO	PCI Only
000Eh	DMA	DMA1 Clear Mask	WO	PCI Only
000Fh	DMA	DMA1 Read/Write All Mask Register Bits	R/W	PCI Only
0020h	Interrupt	INT 1 Control	R/W	PCI/ISA
0021h	Interrupt	INT 1 Mask	R/W	PCI/ISA
0040h	Timer	Timer Counter 1–Counter 0 Count	R/W	PCI/ISA
0041h	Timer	Timer Counter 1–Counter 1 Count	R/W	PCI/ISA
0042h	Timer	Timer Counter 1–Counter 2 Count	R/W	PCI/ISA
0043h	Timer	Timer Counter 1 Command Mode	WO	PCI/ISA
0060h(2)	Control	Reset UBus IRQ12	RO	PCI/ISA
0061h	Control	NMI Status and Control	R/W	PCI/ISA
0070h(2)	Control	CMOS RAM Address and NMI Mask	WO	PCI/ISA
0078h-007Bh(3,4,5)	Timer	BIOS Timer	R/W	PCI Only
0080h(1)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
0081h	DMA	DMA Channel 2 Page Register	R/W	PCI/ISA
0082h	DMA	DMA Channel 3 Page Register	R/W	PCI/ISA
0083h	DMA	DMA Channel 1 Page Register	R/W	PCI/ISA

Table 4. Non-Configuration Registers (Continued)

Address	Function Unit	Register	Register Access	Bus Access
0084h(1)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
0085h(1)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
0086h(1)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
0087h	DMA	DMA Channel 0 Page Register	R/W	PCI/ISA
0088h(1)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
0089h	DMA	DMA Channel 6 Page Register	R/W	PCI/ISA
008Ah	DMA	DMA Channel 7 Page Register	R/W	PCI/ISA
008Bh	DMA	DMA Channel 5 Page Register	R/W	PCI/ISA
008Ch(1)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
008Dh(1)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
008Eh(1)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
008Fh	DMA	DMA Low Page Register Refresh	R/W	PCI/ISA
0090h(6)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
0092h(2)	Control	Port 92 Register	R/W	PCI/ISA
0094h(6)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
0095h(6)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
0096h(6)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
0098h(6)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
009Ch(6)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
009Dh(6)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
009Eh(6)	DMA	DMA Page Register Reserved	R/W	PCI/ISA
009Fh	DMA	DMA Low Page Register Refresh	R/W	PCI/ISA
00A0h	Interrupt	INT 2 Control Register	R/W	PCI/ISA
00A1h	Interrupt	INT 2 Mask Register	R/W	PCI/ISA
00B2h	P.M.	Advanced Power Management Control Port	R/W	PCI Only
00B3h	P.M.	Advanced Power Management Status Port	R/W	PCI Only
00C0h	DMA	DMA2 CH0 Base and Current Address	R/W	PCI Only
00C2h	DMA	DMA2 CH0 Base and Current Count	R/W	PCI Only
00C4h	DMA	DMA2 CH1 Base and Current Address	R/W	PCI Only
00C6h	DMA	DMA2 CH1 Base and Current Count	R/W	PCI Only
00C8h	DMA	DMA2 CH2 Base and Current Address	R/W	PCI Only

Table 4. Non-Configuration Registers (Continued)

Address	Function Unit	Register	Register Access	Bus Access
00CAh	DMA	DMA2 CH2 Base and Current Count	R/W	PCI Only
00CCh	DMA	DMA2 CH3 Base and Current Address	R/W	PCI Only
00CEh	DMA	DMA2 CH3 Base and Current Count	R/W	PCI Only
00D0h	DMA	DMA2 Status(r) Command(w) Register	R/W	PCI Only
00D2h	DMA	DMA2 Write Request Register	WO	PCI Only
00D4h	DMA	DMA2 Write Single Mask Bit Register	WO	PCI Only
00D6h	DMA	DMA2 Write Mode Register	WO	PCI Only
00D8h	DMA	DMA2 Clear Byte Pointer Register	WO	PCI Only
00DAh	DMA	DMA2 Master Clear Register	WO	PCI Only
00DCh	DMA	DMA2 Clear Mask Register	WO	PCI Only
00DEh	DMA	DMA2 Read/Write All Mask Register Bits	R/W	PCI Only
00F0h(2)	Control	Coprocessor Error Register	WO	PCI/ISA
0372h(2)	Control	Secondary Floppy Disk Digital Output Register	WO	PCI/ISA
03F2h(2)	Control	Primary Floppy Disk Digital Output Register	WO	PCI/ISA
040Ah(3)	DMA	Scatter/Gather Interrupt Status Register	RO	PCI Only
040Bh	DMA	DMA1 Extended Mode Register	WO	PCI/ISA
0410h(3,4)	DMA	CH0 Scatter/Gather Command	WO	PCI Only
0411h(3,4)	DMA	CH1 Scatter/Gather Command	WO	PCI Only
0412h(3,4)	DMA	CH2 Scatter/Gather Command	WO	PCI Only
0413h(3,4)	DMA	CH3 Scatter/Gather Command	WO	PCI Only
0415h(3,4)	DMA	CH5 Scatter/Gather Command	WO	PCI Only
0416h(3,4)	DMA	CH6 Scatter/Gather Command	WO	PCI Only
0417h(3,4)	DMA	CH7 Scatter/Gather Command	WO	PCI Only
0418h(3,4)	DMA	CH0 Scatter/Gather Status	RO	PCI Only
0419h(3,4)	DMA	CH1 Scatter/Gather Status	RO	PCI Only
041Ah(3,4)	DMA	CH2 Scatter/Gather Status	RO	PCI Only
041Bh(3,4)	DMA	CH3 Scatter/Gather Status	RO	PCI Only
041Dh(3,4)	DMA	CH5 Scatter/Gather Status	RO	PCI Only
041Eh(3,4)	DMA	CH6 Scatter/Gather Status	RO	PCI Only
041Fh(3,4)	DMA	CH7 Scatter/Gather Status	RO	PCI Only
0420h–0423h(3,4)	DMA	CH0 Scatter/Gather Descriptor Table Pointer	R/W	PCI Only

Table 4. Non-Configuration Registers (Continued)

Address	Function Unit	Register	Register Access	Bus Access
0424h–0427h(3,4)	DMA	CH1 Scatter/Gather Descriptor Table Pointer	R/W	PCI Only
0428h–042Bh(3,4)	DMA	CH2 Scatter/Gather Descriptor Table Pointer	R/W	PCI Only
042Ch–042Fh(3,4)	DMA	CH3 Scatter/Gather Descriptor Table Pointer	R/W	PCI Only
0434h–0437h(3,4)	DMA	CH5 Scatter/Gather Descriptor Table Pointer	R/W	PCI Only
0438h–043Bh(3,4)	DMA	CH6 Scatter/Gather Descriptor Table Pointer	R/W	PCI Only
043Ch–043Fh(3,4)	DMA	CH7 Scatter/Gather Descriptor Table Pointer	R/W	PCI Only
0481h	DMA	DMA CH2 High Page Register	R/W	PCI/ISA
0482h	DMA	DMA CH3 High Page Register	R/W	PCI/ISA
0483h	DMA	DMA CH1 High Page Register	R/W	PCI/ISA
0487h	DMA	DMA CH0 High Page Register	R/W	PCI/ISA
0489h	DMA	DMA CH6 High Page Register	R/W	PCI/ISA
048Ah	DMA	DMA CH7 High Page Register	R/W	PCI/ISA
048Bh	DMA	DMA CH5 High Page Register	R/W	PCI/ISA
04D0h	Interrupt	Edge/Level Control Register—INT CNTRL 1	R/W	PCI Only
04D1h	Interrupt	Edge/Level Control Register—INT CNTRL 2	R/W	PCI Only
04D6h	DMA	DMA2 Extended Mode Register	WO	PCI/ISA

NOTES:
1. PCI write cycles to these address locations flow through to the ISA Bus. PCI read cycles to these address locations do not flow through to the ISA Bus.
2. PCI read and write cycles to these address locations flow through to the ISA Bus.
3. The I/O address of this register is relocatable. The value shown in this table is the default address location.
4. This register can be accessed as a Byte, Word, or Dword quantity.
5. If this register location is enabled, PCI accesses to the BIOS Timer Register do not flow through to the ISA Bus. If disabled, accesses to this address location flow through to the ISA Bus.
6. When the DMAAC bit in the PCI Control Register is '0', the 82378 will alias I/O accesses in the 80h–8Fh range to the 90h–9Fh range. Write accesses to these address locations flow through to the ISA Bus. Read cycles to these address locations do not flow through to the ISA Bus. When DMAAC = 1, the SIO will only respond to the 80h-8Fh range and read and write accesses to these addresses in the 90h–9Fh range will be forwarded from the PCI bus to the ISA Bus (I/O port 92h is always a distinct register in the 90h–9Fh range and is always fully decoded, regardless of the setting of the DMAAC bit).

4.1 SIO Configuration Register Description

This section describes the SIO configuration registers. These registers include the Mandatory Header Registers (located in the first 64 bytes of configuration space) and the SIO specific registers (located from configuration offset 40h–56h).

4.1.1 VID—VENDOR IDENTIFICATION REGISTER

Address Offset: 00h, 01h
Default Value: 8086h
Attribute: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bits[15:0]: Vendor Identification Number
This is a 16-bit value assigned to Intel.

4.1.2 DID—DEVICE IDENTIFICATION REGISTER

Address Offset: 02h, 03h
Default Value: 0484h
Attribute: Read Only
Size: 16 bits

The DID Register contains the device identification number. This register, along with the Vendor ID, uniquely identifies the SIO. Writes to this register have no effect.

Bits[15:0]: Device Identification Number
This is a 16-bit value assigned to the SIO.

4.1.3 COM—COMMAND REGISTER

Address Offset: 04h–05h
Default Value: 0007h
Attribute: Read/Write
Size: 16 bits

Bits[15:5]: Reserved
Read 0.

Bit 4: PMWE (Postable Memory Write Enable)
Enable Postable memory write, memory write and invalidate, and memory read Pre-fetch commands. The SIO does not support these commands as a master or slave so this bit is not implemented. This bit will always be read as a 0.

Bit 3: SCE (Special Cycle Enable)
When this bit is set to a "1", the SIO will recognize PCI Special Cycles. When set to "0", the SIO will ignore all PCI Special Cycles. This bit MUST be enabled in the 82378ZB if the STPCLK feature is being used.

Bit 2: BME (Bus Master Enable)
Since the SIO always requests the PCI Bus on behalf of ISA masters, DMA, or line buffer PCI requests, this bit is hardwired to a 1 and will always be read as a 1.

Bit 1: MSE (Memory Space Enable)
Enables SIO to accept a PCI-originated memory cycle. Since the SIO always responds to PCI-originated memory cycles (and ISA-bound cycles) by asserting DEVSEL#, this bit is hardwired to a 1 and will always be read as a 1.

Bit 0: IOSE (I/O Space Enable)
Enable SIO to accept a PCI-originated I/O cycle. Since the SIO always responds to a master I/O cycle, this bit is hardwired to a 1 and will always be read as a 1.

4.1.4 DS—DEVICE STATUS REGISTER

Address Offset: 06h, 07h
Default Value: 0200h
Attribute: Read/Write
Size: 16 bits

DSR is a 16-bit status register that reports the occurrence of a PCI master-abort by the SIO or a PCI target-abort when the SIO is a master. The register also indicates the SIO DEVSEL# signal timing that is hardwired in the SIO.

Bit 15: Reserved
Read as 0.

Bit 14: SERRS (SERR# Status)
This bit is set by the PCI devices that assert the SERR# signal. Since SERR# is only an input to the SIO, this bit is not implemented and will always be read as 0.

Bit 13: MA (Master-Abort Status)
When the SIO, as a master, generates a master-abort, MA is set to a 1. Software sets MA to 0 by writing a 1 to this bit location.

Bit 12: RTA (Received Target-Abort Status)
When the SIO is a master on the PCI Bus and receives a target-abort, this bit is set to a 1. Software sets RTA to 0 by writing a 1 to this bit location.

Bit 11: STA (Signaled Target-Abort Status)
This bit is set to a 1 by the SIO when it generates a target-abort.

Bits[10:9]: DEVT (SIO DEVSEL# Timing Status)
This 2-bit field defines the timing for DEVSEL# assertion. These read only bits indicate the SIO's DEVSEL# timing when performing a positive decode. Since the SIO always generates DEVSEL# with medium timing, DEVT = 01. This DEVSEL# timing does not include Configuration cycles.

Bits[8:0]: Reserved
Read as 0's.

4.1.5 RID—REVISION IDENTIFICATION REGISTER

Address Offset: 08h
Default Value: xxh (dependent on Part Revision)
Attribute: Read Only
Size: 4 bits (upper nibble reserved)

This 4-bit register contains the revision number for the SIO. This number indicates the stepping number of the component. Additionally, the upper nibble of the value is reserved. BIOS should mask the upper nibble when reading this register. These bits are read only. Writes to this register have no effect.

Bits[7:4]: Reserved
These 4 bits are reserved.

Bits[3:0]: Revision Identification Number
This is an 4-bit value that indicates the revision identification number for the SIO. Numbers used so far include:
0h: 82378IB A0-Stepping
1h: 82378IB B0-Stepping
WAS NOT IMPLEMENTED. B0 steppings read 0h also. Read the BIOS Timer Base Address Configuration Register to identify between A0 and B0 steppings.
A0 = 0000h
B0 = 0078h
3h: 82378ZB A0-Stepping

4.1.6 PCICON—PCI CONTROL REGISTER

Address Offset: 40h
Default Value: 20h
Attribute: Read/Write
Size: 8 bits

This 8-bit register controls the Line Buffer operation, the SIO's PCI Posted Write Buffer enabling, and the DEVSEL# signal sampling point. The PCICON Register also controls how the SIO responds to INTA cycles on the PCI Bus and if the reserved DMA page registers are aliased from 80h–8Fh to 90h–9Fh.

Bit 7: Reserved
Read as 0.

Bit 6: DMAAC (DMA Reserved Page Register Aliasing Control)
These register bits control whether the SIO will alias I/O accesses in the 80h–8Fh to the 90h–9Fh range. When DMAAC = 0, the SIO will alias I/O accesses in the 80h–8Fh to the 90h–9Fh range (AD4 is not used for decoding the DMA reserved page registers). When DMAAC = 1, the SIO will only respond to the 80h–8Fh range (AD4 is used for decoding the DMA reserved page registers). Read and write accesses to the 90h–9Fh range will be forwarded from the PCI bus to the ISA bus.

NOTE:
I/O port 92h is always a distinct register in the 90h–9Fh range and is always fully decoded, regardless of the setting of this bit.

Bit 5: IAE (Interrupt Acknowledge Enable)
When IAE = 0, the SIO ignores INTA cycles generated on the PCI Bus. However, when disabled, the SIO still responds to accesses to the 8259's register set and allows poll mode functions. When IAE = 1, the SIO responds to INTA cycles in the normal fashion. This bit defaults to a 1 (respond to INTA cycles).

Bits[4:3]: SDSP (Subtractive Decoding Sample Point)
The SDSP field determines the DEVSEL# sample point, after which an inactive DEVSEL# results in the SIO forwarding the unclaimed PCI cycle to the ISA Bus (subtractive decoding). This setting should match the slowest device in the system.

Bit	4	3	Operation
	0	0	Slow sample point
	0	1	Typical sample point
	1	0	Fast sample point
	1	1	Reserved

Bit 2: PPBE (PCI Posted Write Buffer Enable)
When PPBE = 0, the PCI posted write buffer is disabled. When PPBE = 1, the PCI posted write buffer is enabled. This bit defaults to disabled mode (PPBE = 0).

Bit 1: ILBC (ISA Master Line Buffer Configuration)
When ILBC = 0, the Line Buffer is in single transaction mode. When ILBC = 1, the Line Buffer is in 8-byte mode. This bit applies only to ISA Master transfers. This bit defaults to single transaction mode (ILBC = 0).

Bit 0: DLBC (DMA Line Buffer Configuration)
When DLBC = 0, the Line Buffer is in single transaction mode. When DLBC = 1, the Line Buffer is in 8-byte mode. This bit applies only to DMA transfers. This bit defaults to single transaction mode (DLBC = 0).

4.1.7 PAC—PCI ARBITER CONTROL REGISTER

Address Offset:	41h
Default Value:	00h
Attribute:	Read/Write
Size:	8 bits

This 8-bit register controls the operation of the PCI arbiter. The PAC register enables/disables the guaranteed access time mode, controls bus lock cycles, enables/disables CPU bus parking, and controls the master retry timer.

Bits[7:5]: Reserved
Read as 0's.

Bits[4:3]: MRT (Master Retry Timer)
This 2-bit field determines the number of PCICLKs after the first retry that a PCI initiator's Bus request will be unmasked.

Bit	4	3	Operation
	0	0	Timer disabled, retries never masked.
	0	1	Retries unmasked after 16 PCICLK's.
	1	0	Retries unmasked after 32 PCICLK's.
	1	1	Retries unmasked after 64 PCICLK's.

Bit 2: BP (Bus Park)
Set to a 1 the SIO will park CPUREQ# on the PCI bus when it detects the PCI bus idle. If Bus Park is disabled, the SIO takes responsibility for driving AD, C/BE# and PAR upon detection of bus idle state if the internal arbiter is enabled.

Bit 1: BL (Bus Lock)
This bit selects between bus lock and resource lock. When BL = 1, Bus Lock is selected. The arbiter considers the entire PCI bus locked upon initiation of any locked transaction. When BL = 0, resource lock is enabled. A locked agent is considered a locked resource and other agents may continue normal PCI transactions.

Bit 0: GAT (Guaranteed Access Time)
This bit enables/disables the guaranteed access time mode. When GAT = 1, the SIO is configured for Guaranteed Access Time mode. This mode is available in order to guarantee the 2.5 μs CHRDY time-out specification for the ISA Bus. When the SIO is an Initiator on behalf of an ISA master, the PCI and memory busses are arbitrated for in serial and must be owned before the ISA master is given ownership of the ISA Bus. When GAT = 0, the guaranteed access time mode is disabled. When guaranteed access time mode is disabled, the ISA master is first granted the ISA Bus and then the SIO arbitrates for the PCI Bus.

4.1.8 PAPC—PCI ARBITER PRIORITY CONTROL REGISTER

Address Offset: 42h
Default Value: 04h
Attribute: Read/Write
Size: 8 bits

This register controls the PCI arbiter priority scheme. The arbiter supports six masters arranged through four switching banks. This permits the six masters to be arranged in a purely rotating priority scheme, one of twenty-four fixed priority schemes, or a hybrid combination of the fixed and rotating priority schemes. Bits[4:7] enable/disable rotate priority for the four banks. For each bit, a 1 enables the mode and a 0 disables the mode. If both fixed and rotate modes are enabled for the same bank, the bank will be in rotate mode. For example, if both bits 0 and 4 are set to a 1, bank 0 will be in rotate mode.

Bit 7: Bank 3 Rotate Control

Bit 6: Bank 2 Rotate Control

Bit 5: Bank 1 Rotate Control

Bit 4: Bank 0 Rotate Control

Bit 3: Bank 2 Fixed Priority Mode Select B

Bit 2: Bank 2 Fixed Priority Mode Select A

Bit 1: Bank 1 Fixed Priority Mode Select

Bit 0: Bank 0 Fixed Priority Mode Select

Fixed Priority Mode

The fixed bank control bits select which requester is the highest priority device within that particular bank.

Table 5. Fixed Mode Bank Control Bits

Mode	Bank					Priority					
	3	2b	2a	1	0	Highest					Lowest
00	0	0	0	0	0	SIOREQ#	REQ0#	REQ2#	REQ3#	CPUREQ#	REQ1#
01	0	0	0	0	1	REQ0#	SIOREQ#	REQ2#	REQ3#	CPUREQ#	REQ1#
02	0	0	0	1	0	SIOREQ#	REQ0#	REQ2#	REQ3#	REQ1#	CPUREQ#
03	0	0	0	1	1	REQ0#	SIOREQ#	REQ2#	REQ3#	REQ1#	CPUREQ#
04	0	0	1	0	0	CPUREQ#	REQ1#	SIOREQ#	REQ0#	REQ2#	REQ3#
05	0	0	1	0	1	CPUREQ#	REQ1#	REQ0#	SIOREQ#	REQ2#	REQ3#
06	0	0	1	1	0	REQ1#	CPUREQ#	SIOREQ#	REQ0#	REQ2#	REQ3#
07	0	0	1	1	1	REQ1#	CPUREQ#	REQ0#	SIOREQ#	REQ2#	REQ3#
08	0	1	0	0	0	REQ2#	REQ3#	CPUREQ#	REQ1#	SIOREQ#	REQ0#
09	0	1	0	0	1	REQ2#	REQ3#	CPUREQ#	REQ1#	REQ0#	SIOREQ#
0A	0	1	0	1	0	REQ2#	REQ3#	REQ1#	CPUREQ#	SIOREQ#	REQ0#
0B	0	1	0	1	1	REQ2#	REQ3#	REQ1#	CPUREQ#	REQ0#	SIOREQ#
0C–0F	0	1	1	x	x	Reserved					
10	1	0	0	0	0	SIOREQ#	REQ0#	REQ3#	REQ2#	CPUREQ#	REQ1#
11	1	0	0	0	1	REQ0#	SIOREQ#	REQ3#	REQ2#	CPUREQ#	REQ1#
12	1	0	0	1	0	SIOREQ#	REQ0#	REQ3#	REQ2#	REQ1#	CPUREQ#
13	1	0	0	1	1	REQ0#	SIOREQ#	REQ3#	REQ2#	REQ1#	CPUREQ#
14	1	0	1	0	0	CPUREQ#	REQ1#	SIOREQ#	REQ0#	REQ3#	REQ2#
15	1	0	1	0	1	CPUREQ#	REQ1#	REQ0#	SIOREQ#	REQ3#	REQ2#
16	1	0	1	1	0	REQ1#	CPUREQ#	SIOREQ#	REQ0#	REQ3#	REQ2#
17	1	0	1	1	1	REQ1#	CPUREQ#	REQ0#	SIOREQ#	REQ3#	REQ2#
18	1	1	0	0	0	REQ3#	REQ2#	CPUREQ#	REQ1#	SIOREQ#	REQ0#
19	1	1	0	0	1	REQ3#	REQ2#	CPUREQ#	REQ1#	REQ0#	SIOREQ#
1A	1	1	0	1	0	REQ3#	REQ2#	REQ1#	CPUREQ#	SIOREQ#	REQ0#
1B		1	0	1	1	REQ3#	REQ2#	REQ1#	CPUREQ#	REQ0#	SIOREQ#
1C–1F	1	1	1	x	x	Reserved					

Rotating Priority Mode
When any Bank Rotate Control bit is set to a one, that particular bank rotates between the two requesting inputs. Any or all banks can be set in rotate mode. If, within a rotating bank, the highest priority input does not have an active request, then the lower priority input will be granted the bus. However, this does not change the rotation scheme. When the bank toggles, the previously lowest priority input will become the highest priority input. Because of this, the maximum latency a device may encounter would be two complete rotations.

4.1.9 ARBPRIX—PCI ARBITER PRIORITY CONTROL EXTENSION REGISTER

Address Offset: 43h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

This register provides the Fixed Priority Mode select for Bank 3 of the arbiter. The ARBPRIX Register fields are shown.

Bits[7:1]: Reserved
Read as 0.

Bit 0: Bank 3 Fixed Priority Mode Select

0 = REQ2# higher priority
1 = REQ3# higher priority

4.1.10 MEMCSCON—MEMCS# CONTROL REGISTER

Address Offset: 44h
Default value: 00h
Attribute: Read/Write
Size: 8 bits

Bits 0-2 of this register enable MEMCS# blocks. PCI addresses within the enabled blocks result in the generation of MEMCS#. Note that the 0–512 KByte segment does not have RE and WE bits. The 0–512 KByte segment can only be turned off with the MEMCS# Master Enable bit (bit 4). Note also, that when the RE and WE bits are both 0 for a particular segment, the PCI master can not access the segment.

Bits[7:5]: Reserved
Read as 0's.

Bit 4: MEMCS# Master Enable
When the MEMCS# master enable bit is set to a 1, the SIO asserts MEMCS# for all accesses to the defined MEMCS# region (that have been programmed in this register and the MAR1, MAR2, and MAR3 Registers). Also, when this bit is a 1, the positive decoding functions enabled by having the ISA Clock Divisor Register bit 6 = 1 and the Utility Bus Chip Select Register "A" bit 6 = 1 are ignored. Subtractive decoding is provided for these memory areas, instead. When the MEMCS# master enable bit is set to a 0, the entire MEMCS# function is disabled. When this bit is 0, MEMCS# will never be asserted.

Bit 3: Write Enable For 0F0000h–0FFFFFh (Upper 64 KByte BIOS)
When this bit is set to a 1, the SIO generates MEMCS# for PCI master memory write accesses to the address range 0F0000h–0FFFFFh. When this bit is set to a 0, the SIO does not generate MEMCS# for PCI master memory write accesses to the address range 0F0000h–0FFFFFh.

Bit 2: Read Enable For 0F0000h–0FFFFFh (Upper 64 KByte BIOS)
When this bit is set to a 1, the SIO generates MEMCS# for PCI master memory read accesses to the address range 0F0000h–0FFFFFh. When this bit is set to a 0, the SIO does not generate MEMCS# for PCI master memory read accesses to the address range 0F0000h–0FFFFFh.

Bit 1: Write Enable For 080000h–09FFFFh (512 KByte–640 KByte)
When this bit is set to a 1, the SIO generates MEMCS# for PCI master memory write accesses to the address range 080000h–09FFFFh. When this bit is set to a 0, the SIO does not generate MEMCS# for PCI master memory write accesses to the address range 080000h–09FFFFh.

Bit 0: Read Enable For 080000h–09FFFFh (512 KByte–640 KByte)
When this bit is set to a 1, the SIO generates MEMCS# for PCI master memory read accesses to the address range 080000h–09FFFFh. When this bit is set to a 0, the SIO does not generate MEMCS# for PCI master memory read accesses to the address range 080000h–09FFFFh.

4.1.11 MEMCSBOH—MEMCS# BOTTOM OF HOLE REGISTER

Address Offset: 45h
Default value: 10h
Attribute: Read/Write
Size: 8 bits

This register defines the bottom of the MEMCS# hole. MEMCS# is not generated for accesses to addresses within the hole defined by this register and the MCSTOH Register. The hole is defined by the following equation: TOH ≥ address ≥ BOH. TOH is the top of the MEMCS# hole defined by the MCSTOH Register and BOH is the bottom of the MEMCS# hole defined by this register.

For example, to program the BOH at 1 MByte, the value of 10h should be written to this register. To program the BOH at 2 MByte + 64 KByte this register should be programmed to 21h. To program the BOH at 8 MByte this register should be programmed to 80h.

When the TOH < BOH the hole is effectively disabled. It is the responsibility of the programmer to guarantee that the BOH is at or above 1 MB. AD[31:24] must be 0's for the hole, meaning the hole is restricted to be under the 16 MByte boundary. The default value for the BOH and TOH effectively disables the hole.

Bit 7: AD23

Bit 6: AD22

Bit 5: AD21

Bit 4: AD20

Bit 3: AD19

Bit 2: AD18

Bit 1: AD17

Bit 0: AD16

4.1.12 MEMCSTOH—MEMCS# TOP OF HOLE REGISTER

Address Offset: 46h
Default value: 0Fh
Attribute: Read/Write
Size: 8 bits

This register defines the top of the MEMCS# hole. MEMCS# is not generated for accesses to addresses within the hole defined by this register and the MCSBOH Register. The hole is defined by the following equation: TOH ≥ address ≥ BOH. TOH is the top of the MEMCS# hole defined by this register and BOH is the bottom of the MEMCS# hole defined by the MCSBOH Register.

For example, to program the TOH at 1 MByte + 64 KByte, this register should be programmed to 10h. To program the TOH at 2 MByte + 128 KByte this register should be programmed to 21h. To program the TOH at 12 MByte this register should be programmed to BFh.

When the TOH < BOH the hole is effectively disabled. It is the responsibility of the programmer to guarantee that the TOH is above 1 MByte. AD[31:24] must be 0's for the hole, meaning the hole is restricted to be under the 16 MByte boundary. The default value for the BOH and TOH effectively disables the hole.

Bit 7: AD23

Bit 6: AD22

Bit 5: AD21

Bit 4: AD20

Bit 3: AD19

Bit 2: AD18

Bit 1: AD17

Bit 0: AD16

4.1.13 MEMCSTOM—MEMCS# TOP OF MEMORY REGISTER

Address Offset: 47h
Default value: 00h
Attribute: Read/Write
Size: 8 bits

This register determines MEMCS# top of memory boundary. The top of memory boundary ranges up to 512 MBytes, in 2 MByte increments. This register is typically set to the top of main memory. Accesses ≥ 2 MByte and ≤ top of memory boundary results in the assertion of the MEMCS# signal (unless the address resides in the hole programmed by the MCSBOH and MCSTOH Registers). A value of 00h disables this 2 MByte-to-top of memory region. A value of 00h assigns the top of memory to include 2 MByte − 1. A value of FFh assigns the top of memory to include 512 MByte − 1.

Bit 7: AD28

Bit 6: AD27

Bit 5: AD26

Bit 4: AD25

Bit 3: AD24

Bit 2: AD23

Bit 1: AD22

Bit 0: AD21

4.1.14 IADCON—ISA ADDRESS DECODER CONTROL REGISTER

Address Offset: 48h
Default value: 01h
Attribute: Read/Write
Size: 8 bits

This register enables the forwarding of ISA or DMA memory cycles to the PCI Bus. In addition, this register sets the top of the "1 MByte to top of main memory" region.

Bits[7:4]:
The top can be assigned in 1 MByte increments from 1 MByte up to 16 MByte. ISA master or DMA accesses within this region are forwarded to PCI unless they are within the hole.

Bits	7	6	5	4	Top of Memory
	0	0	0	0	1 MByte
	0	0	0	1	2 MByte
	0	0	1	0	3 MByte
	0	0	1	1	4 MByte
	0	1	0	0	5 MByte
	0	1	0	1	6 MByte
	0	1	1	0	7 MByte
	0	1	1	1	8 MByte
	1	0	0	0	9 MByte
	1	0	0	1	10 MByte
	1	0	1	0	11 MByte
	1	0	1	1	12 MByte
	1	1	0	0	13 MByte
	1	1	0	1	14 MByte
	1	1	1	0	15 MByte
	1	1	1	1	16 MByte

Bits[3:0]:
ISA and DMA Memory Cycle To PCI Bus Enables. The memory block is enabled by writing a 1 to the corresponding bit position. Setting the bit to 0 disables the corresponding block. ISA or DMA memory cycles to the enabled blocks result in the ISA cycle being forwarded to the PCI Bus. The BIOSCS# enable bit (bit 6 in the UBCSA Register) for the 896K–960K region overrides the function of bit 3 of this register. If the BIOSCS# bit is set to a 1, the ISA or DMA memory cycle is always contained to ISA, regardless of the setting of bit 3 in this register. If the BIOSCS# bit is disabled, the cycle is forwarded to the PCI bus if bit 3 in this register is enabled. Refer to Section 5.5.1.2 for a complete description of BIOS decoding.

Bit	Memory Block
0	0–512 KByte Memory
1	512–640 KByte Memory
2	640–768 KByte VGA Memory
3	896–960 KByte Low BIOS

4.1.15 IADRBE—ISA ADDRESS DECODER ROM BLOCK ENABLE REGISTER

Address Offset: 49h
Default value: 00h
Attribute: Read/Write
Size: 8 bits

ISA addresses within the enabled ranges result in the ISA memory cycle being forwarded to the PCI Bus. For each bit position, the memory block is enabled if the bit is set to 1 and is disabled if the bit is set to 0. If the memory block is disabled, the ISA cycle is not forwarded to the PCI Bus.

Bit 7: 880–896K Memory Enable

Bit 6: 864–880K Memory Enable

Bit 5: 848–864K Memory Enable

Bit 4: 832–848K Memory Enable

Bit 3: 816–832K Memory Enable

Bit 2: 800–816K Memory Enable

Bit 1: 784–800K Memory Enable

Bit 0: 768–784K Memory Enable

4.1.16 IADBOH—ISA ADDRESS DECODER BOTTOM OF HOLE REGISTER

Address Offset: 4Ah
Default value: 10h
Attribute: Read/Write
Size: 8 bits

This register defines the bottom of the ISA Address Decoder hole. The hole is defined by the following equation: TOH ≥ address ≥ BOH, where BOH is the bottom of the hole address programmed into this register and TOH is the top of the hole address programmed into the IADTOH Register. ISA master or DMA addresses falling within the hole will not be forwarded to the PCI Bus. The hole can be sized in 64 KByte increments and placed anywhere between 1 MByte and 16 MByte on any 64 KByte boundary. It is the responsibility of the programmer to guarantee that the BOH is at or above 1 MByte. A[31:24] must be 0's for the hole, meaning the hole is restricted to be under the 16 MByte boundary. When TOH < BOH, the hole is effectively disabled. The default value for the BOH and TOH disables the hole.

For example, to program the BOH at 1 MByte, this register should be set to 10h. To program the BOH at 2 MBytes, this register should be set to 20h. To program the BOH at 8 MBytes, this register should be set to 80h. These settings are shown in Figure 2.

Bit 7: A23

Bit 6: A22

Bit 5: A21

Bit 4: A20

Bit 3: A19

Bit 2: A18

Bit 1: A17

Bit 0: A16

4.1.17 IADTOH—ISA ADDRESS DECODER TOP OF HOLE REGISTER

Address Offset: 4Bh
Default value: 0Fh
Attribute: Read/Write
Size: 8 bits

This register defines the top of the ISA Address Decoder hole. The hole is defined by the following equation: TOH ≥ address ≥ BOH, where BOH is the bottom of the hole address programmed into the LADBOH Register and TOH is the top of the hole address programmed into this Register. ISA master or DMA addresses falling within the hole will not be forwarded to the PCI Bus. The hole can be sized in 64 KByte increments and placed anywhere between 1 MByte and 16 MByte on any 64 KByte boundary. It is the responsibility of the programmer to guarantee that the TOH is at or above 1 MByte. A[31:24] must be 0's for the hole, meaning the hole is restricted to be under the 16 MByte boundary. When TOH < BOH, the hole is disabled. The default value for the BOH and TOH disables the hole.

For example, to program the TOH at 1 MByte + 64 KByte, this register should be set to 10h. To program the TOH at 2 MByte + 128 KByte, this register should be set to 21h. To program the TOH at 12 MByte, this register should be set to BFh. These settings are shown in Figure 2.

Bit 7: A23

Bit 6: A22

Bit 5: A21

Bit 4: A20

Bit 3: A19

Bit 2: A18

Bit 1: A17

Bit 0: A16

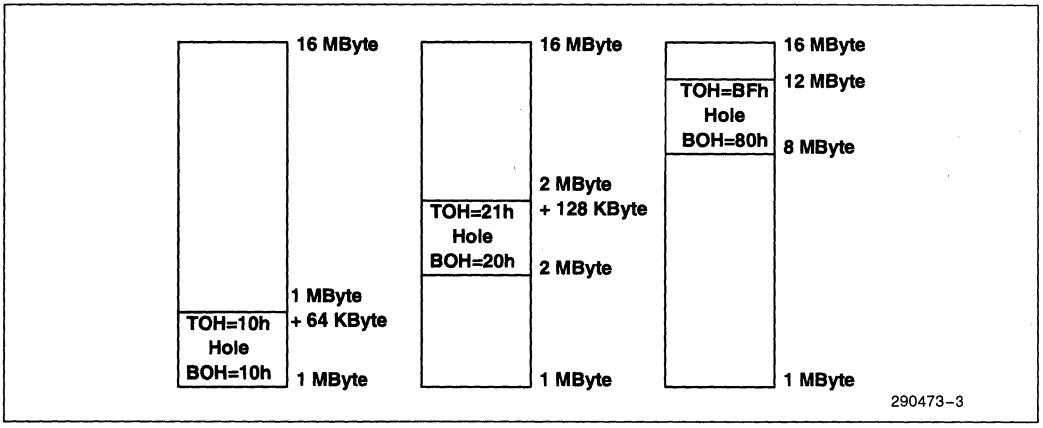


Figure 2. ISA Address Decoder Hole Examples

Table 6. Examples of ISA Decoding

Test Case Description	TOM (48h)	TOH (4Bh)	BOH (4Ah)	Address (hex)	Address	Result
8MB TOM, no hole @ 1M	7xh	0Fh	10h	01000000h 00FFFFFFh 00800000h 007FFFFFh 00100000h 000FFFFFh	16MB 16MB-1 8MB 8MB-1 1MB 1MB-1	To PCI ISA ISA To PCI To PCI ISA (BIOS)
4MB TOM, no hole @ 2M	3xh	1Fh	20h	01000000h 00FFFFFFh 00400000h 003FFFFFh 00200000h 001FFFFFh 00100000h	16MB 16MB-1 4MB 4MB-1 2MB 2MB-1 1MB	To PCI ISA ISA To PCI To PCI To PCI To PCI
1MB TOM, no hole @ 1M	0xh	0Fh	10h	01000000h 00FFFFFFh 00100000h 000FFFFFh	16MB 16MB-1 1MB 1MB-1	To PCI ISA ISA ISA (BIOS)
16MB TOM, 64KB hole @ 15MB	Fxh	F0h	F0h	01000000h 00FFFFFFh 00F10000h 00F0FFFFh 00F00000h 00EFFFFFh 00E10000h 00E0FFFFh 00E00000h 00DFFFFFh	16MB 16MB-1 15MB + 64KB 15MB + 64KB-1 15MB 15MB-1 14MB + 64KB 14MB + 64KB-1 14MB 14MB-1	To PCI To PCI To PCI ISA ISA To PCI To PCI To PCI To PCI To PCI
12MB TOM, 2MB + 128KB hole @ 2MB	Bxh	21h	20h	01000000h 00FFFFFFh 00C00000h 00BFFFFFh 00220000h 0021FFFFh 00210000h 0020FFFFh 00200000h 001FFFFFh 00100000h	16MB 16MB-1 12MB 12MB-1 2MB + 128KB 2MB + 128KB-1 2MB + 64KB 2MB + 64KB-1 2MB 2MB-1 1MB	To PCI ISA ISA To PCI To PCI ISA ISA ISA ISA To PCI To PCI

Table 6. Examples of ISA Decoding (Continued)

Test Case Description	TOM (48h)	TOH (4Bh)	BOH (4Ah)	Address (hex)	Address	Result
5MB TOM, 3MB hole @	4xh	47h	18h	01000000h	16MB	To PCI
				00FFFFFFh	16MB-1	ISA
				00500000h	5MB	ISA
				004FFFFFh	5MB-1	To PCI
				00480000h	4.5MB	To PCI
				0047FFFFh	4.5MB-1	ISA
				00180000h	1.5MB	ISA
				0017FFFFh	1.5MB-1	To PCI
				00100000h	1MB	To PCI

4.1.18 ICRT—ISA CONTROLLER RECOVERY TIMER REGISTER

Address Offset: 4Ch
Default Value: 56h
Attribute: Read/Write
Size: 8 bits

The I/O recovery mechanism in the SIO is used to add additional recovery delay between PCI originated 8-bit and 16-bit I/O cycles to the ISA bus. The SIO automatically forces a minimum delay of five SYSCLKs between back-to-back 8- and 16-bit I/O cycles to the ISA bus. The delay is measured from the rising edge of the I/O command (IOR# or IOW#) to the falling edge of the next BALE. If a delay of greater than five SYSCLKs is required, the ISA I/O Recovery Time Register can be programmed to increase the delay in increments of SYSCLKs. Note that no additional delay is inserted for back-to-back I/O "sub cycles" generated as a result of byte assembly or disassembly. This register defaults to 8- and 16-bit recovery enabled with two clocks added to the standard I/O recovery.

Bit 7: Reserved
Read as 0.

Bit 6: 8-Bit I/O Recovery Enable
This bit enables the recovery times programmed into bits 0 and 1 of this register. When this bit is set to 1, the recovery times shown for bits[5:3] are enabled. When this bit is set to 0, recovery times are disabled.

Bits[5:3]: 8-Bit I/O Recovery Times
This 3-bit field defines the recovery times for 8-bit I/O. Programmable delays between back-to-back 8-bit PCI cycles to ISA I/O slaves is shown in terms of ISA clock cycles (SYSCLK) added to the five minimum. The selected delay programmed into this field is enabled/disabled via bit 6 of this register.

Bit 5	4	3	SYSCLK Added	Total SYSCLKs
0	0	1	+1	6
0	1	0	+2	7
0	1	1	+3	8
1	0	0	+4	9
1	0	1	+5	10
1	1	0	+6	11
1	1	1	+7	12
0	0	0	+8	13

Bit 2: 16-Bit I/O Recovery Enable
This bit enables the recovery times programmed into bits 0 and 1 of this register. When this bit is set to 1, the recovery times shown for bits 0 and 1 are enabled. When this bit is set to 0, recovery times are disabled.

Bits[1:0]: 16-Bit I/O Recovery Times
This 2-bit field defines the recovery time for 16-bit I/O. Programmable delays between back-to-back 16-bit PCI cycles to ISA I/O slaves is shown in terms of ISA clock cycles (SYSCLK) added to the five minimum. The selected delay programmed into this field is enabled/disabled via bit 2 of this register.

Bit 1	Bit 0	SYSCLK Added	Total SYSCLKs
0	1	+1	6
1	0	+2	7
1	1	+3	8
0	0	+4	9

4.1.19 ICD—ISA CLOCK DIVISOR REGISTER

Address Offset: 4Dh
Default Value: 40h
Attribute: Read/Write
Size: 8 bits

This register selects the integer value used to divide the PCI clock (PCICLK) to generate the ISA clock (SYSCLK). In addition, this register provides an ISA Reset bit to software control RSTDRV, a bit to enable/disable the MOUSE function, a bit to enable/disable the coprocessor error support, and a bit to disable the positive decode for the upper 64 KBytes of BIOS at the top of 1 MByte (F0000h–FFFFFh) and aliased regions.

Bit 7: Reserved

Bit 6: Positive Decode of Upper 64 KByte BIOS Enable
This bit enables (bit 6 = 1) and disables (bit 6 = 0) the positive decode of the upper 64 KBytes of BIOS area at the top of 1 MByte (F0000h–FFFFFh) and the aliased regions at the top of 4 GBytes (FFFF0000h–FFFFFFFFh) and 4 GByte-1 MByte (FFEF0000–FFEFFFFFh). When bit 6 = 1, these address regions are positively decoded, unless bit 4 in the MEMCS# Control Register is set to a 1 in which case these regions are subtractively decoded. When bit 6 = 0, these address regions are subtractively decoded. The encoded chip selects for BIOSCS# and the UBUSOE# signal will always be generated when these locations are accessed, regardless of the state of this bit. A reset sets this bit to a 1 (positive decode enabled).

Bit 5: Coprocessor Error Enable
This bit is used to enable and disable the Coprocessor error support. When enabled (bit 5 = 1), the FERR# input, when driven active, triggers an IRQ13 to the SIO's interrupt controller. FERR# is also used to gate the IGNNE# output. When disabled (bit 5 = 0), the FERR# signal can be used as IRQ13 and the coprocessor support is disabled. A reset sets this bit to 0 (coprocessor support disabled).

Bit 4: IRQ12/M Mouse Function Enable
When this bit is set to 1, IRQ12/M provides the mouse function. When this bit is set to 0, IRQ12/M provides the standard IRQ12 interrupt function. A hard reset sets this bit to 0.

Bit 3: RSTDRV Enable
This bit is used to enable RSTDRV on the ISA Bus. When this bit is set to 1, RSTDRV is asserted and remains asserted until this bit is set to a 0. When set to 0, normal operation of RSTDRV is provided. This bit should be used during configuration to reset the ISA Bus when changing the clock divisor. For a reset, this bit defaults to 0. Note that the software must ensure that RSTDRV is asserted for a minimum of 1 μs.

Bit[2:0]: PCICLK-to-ISA SYSCLK Divisor
These bits are used to select the integer that is used to divide the PCICLK down to generate the ISA SYSCLK. Upon reset, these bits are set to 000 (divisor of 4 selected). For PCI frequencies less than 33 MHz (not including 25 MHz), a clock divisor value must be selected that ensures that the ISA Bus frequency does not violate the 6 MHz to 8.33 MHz SYSCLK specification.

Bit 2	Bit 1	Bit 0	Divisor	SYSCLK
0	0	0	4 (33 MHz)	8.33 MHz
0	0	1	3 (25 MHz)	8.33 MHz
0	1	0	Reserved	
0	1	1	Reserved	
1	0	0	Reserved	
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

4.1.20 UBCSA—UTILITY BUS CHIP SELECT A REGISTER

Address Offset: 4Eh
Default Value: 07h
Attribute: Read/Write
Size: 8 bits

This register enables/disables accesses to the RTC, keyboard controller, Floppy Disk controller, IDE, and BIOS locations E0000h–EFFFFh and FFF80000h–FFFDFFFFh. Disabling any of these bits prevents the encoded chip select bits (ECSADDR[2:0]) and utility bus transceiver control signal (UBUSOE#) for that device from being generated.

This register is also used to select which address range (primary or secondary) will be decoded for the resident floppy controller and IDE. This ensures that there is no contention with the Utility bus transceiver driving the system data bus during read accesses to these devices.

Bit 7: Extended BIOS Enable
When bit 7 = 1 (enabled), PCI accesses to locations FFF80000h–FFFDFFFFh result in the generation of the encoded signals (ECSADDR[2:0]) for BIOS. When enabled, PCI master accesses to this area are positively decoded and UBUSOE# is generated. When this bit is disabled (bit 7 = 0), the SIO does not generate the encoded (ECSADDR[2:0]) signals or UBUSOE#.

Bit 6: Lower BIOS Enable
When bit 6 = 1 (enabled), PCI or ISA accesses to the lower 64 KByte BIOS block (E0000h–EFFFFh) at the top of 1 MByte, or the aliases at the top of 4 GByte and 4 GByte–1 MByte results in the generation of the encoded (ECSADDR[2:0]) signals for BIOS. When enabled, PCI master accesses to this area are positively decoded to the ISA Bus, unless bit 4 in the MEMCS# Control Register is set to a 1 in which case these regions are subtractively decoded. Also, when enabled, ISA master or DMA master accesses to this region are not forwarded to the PCI Bus. When this bit is disabled (bit 6 = 0), the SIO does not generate the encoded (ECSADDR[2:0]) signals. Also, when this bit is disabled, ISA master or DMA accesses to this region are forwarded to PCI, if bit 3 in the IADCON Register is set to 1.

Bit 4: IDE Decode Enable
Bit 4 enables/disables IDE locations 1F0h–1F7h (primary) or 170h–177h (secondary) and 3F6h, 3F7h (primary) or 376h, 377h (secondary). When bit 4 = 1, the IDE encoded chip select signals and the Utility Bus transceiver signal (UBUSOE#) are generated for these addresses. When bit 4 = 0, the IDE encoded chip select signals and the Utility Bus transceiver signal (UBUSOE#) are not generated for these addresses.

Bit [5, 3:2]: Floppy Disk Address Locations Enable
Bits 2 and 3 are used to enable or disable the floppy locations as indicated below. A PCIRST# sets bit 2 to 1 and bit 3 to 0. Bit 5 is used to select between the primary and secondary address range used by the Floppy Controller and the IDE. Only primary or only secondary can be programmed at any one time. A PCIRST# sets this bit to 0 (primary).

The following table shows how these bits are used to select the floppy controller:

Address	Bit 5	Bit 3	Bit 2	DSKCHG	ECSADDR[2:0]	FLOPPYCS#
X	X	X	X	0	1 1 1	1
3F0h, 3F1h	0	1	X	1	1 0 0	0
3F2h–3F7h	0	X	1	1	1 0 0	0 (note)
370h, 371h	1	1	X	1	1 0 0	0
372h–37Fh	1	X	1	1	1 0 0	0 (note)

NOTE:
If IDE decode is enabled (bit 4 = 1), all accesses to locations 03F6h and 03F7h (primary) or 0376h and 0377h (secondary) result in the ECSADDR[2:0] signals generating a decode for IDECS1# (FLOPPYCS# is not generated). An external AND gate can be used to tie IDECS1# and FLOPPYCS# together to insure that the floppy is enabled for these accesses. If IDE decode is disabled (bit 4 = 0), and the decode for the floppy is enabled, then the encoded chip selects for the floppy locations are generated.

Bit 1: Keyboard Controller Address Location Enable
Enables (1) or disables (0) the Keyboard controller address locations 60h, 62h, 64h, and 66h. When this bit is set to 0, the Keyboard Controller encoded chip select signals (ECSADDR[2:0]) and the Utility Bus transceiver signal (UBUSOE#) are not generated for these locations.

Bit 0: RTC Address Location Enable
Enables (1) or disables (0) the RTC address locations 70h–77h. When this bit is set to 0, the RTC encoded chip select signals (ECSADDR[2:0]), RTCALE#, RTCCS#, and UBUSOE# signals are not generated for these addresses.

4.1.21 UBCSB—UTILITY BUS CHIP SELECT B REGISTER

Address Offset: 4Fh
Default Value: 4Fh
Attribute: Read/Write
Size: 8 bits

This register is used to enable/disable accesses to the serial ports and parallel port locations supported by the SIO. When disabled, the ECSADDR(2:0) encoded chip select bits and Utility Bus Transceiver control signal (UBUSOE#), for that device, are not generated. This register is also used to disable accesses to port 92 and enable or disable configuration RAM decode.

Bit 7: Configuration RAM Decode Enable
This bit is used to enable (bit 7 = 1) or disable (bit 7 = 0) I/O write accesses to location 0C00h and I/O read/write accesses to locations 0800h–08FFh. When enabled, the encoded chip select signals for generating an external configuration page chip select (CPAGECS#) are generated for accesses to 0C00h. The encoded chip select signals for generating an external configuration memory chip select (CFIGMEMCS#) are generated for accesses to 0800h–08FFh. When bit 7 = 0, configuration RAM decode is disabled and the CPAGECS# and CFIGMEMCS# are not generated for the corresponding accesses.

Bit 6: Port 92 Enable
This bit is used to enable/disable access to Port 92. When bit 6 = 1, Port 92 is enabled. When bit 6 = 0, Port 92 is disabled. When a PCIRST# occurs, this bit is set to 1 (enable).

Bits[5:4]: Parallel Port Enable
These bits are used to select the parallel port address range: (LPT1, LPT2, LPT3, or disable). When a PCIRST# occurs, this field is set to 00 (LPT1).

Bit 5	Bit 4	Function
0	0	3BCh–3BFh (LPT1)
0	1	378h–37Fh (LP2)
1	0	278h–27Fh (LPT3)
1	1	Disabled

Bits[3:2]: Serial Port B Enable
These bits are used to assign serial port B address range: (COM1, COM2, or disable). If either COM1 or COM2 address ranges are selected, the encoded chip select signals [ECSADDR(2:0)] for Port B will be generated. A PCIRST# sets bits[3:2] to 11 (Port B disabled).

Bit 3	2	Function
0	0	3F8h–3FFh (COM1)
0	1	2F8h–2FFh (COM2)
1	0	Reserved
1	1	Port B Disabled

NOTE:
If Serial port A and B are programmed for the same I/O address, the encoded chip select signals, ECSADDR(2:0), for port B are disabled.

Bits[1:0]: Serial Port A Enable
These bits are used to assign serial port A address range: (COM1, COM2, or disable). If either COM1 or COM2 address ranges are selected, the encoded chip select signals (ECSADDR[2:0]) for Port A will be generated. A PCIRST# sets bits[1:0] to 11 (port A disabled).

Bit 1	0	Function
0	0	3F8h–3FFh (COM1)
0	1	2F8h–2FFh (COM2)
1	0	Reserved
1	1	Port A disabled

NOTE:
If Serial port A and B are programmed for the same I/O address, the encoded chip select signals, ECSADDR[2:0], for port B are disabled.

4.1.22 MAR1—MEMCS# ATTRIBUTE REGISTER #1

Address Offset: 54h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

RE—Read Enable. When the RE bit (bit 6, 4, 2, 0) is set to a 1, the SIO generates MEMCS# for PCI master, DMA, or ISA master memory read accesses to the corresponding segment. When the RE bit is set to a 0, the SIO does not generate MEMCS# for PCI master memory read accesses to the corresponding segment. When the RE and WE bits are both 0 (or bit 4 in the MEMCS# Control Register is set to a 0–disabled), the PCI master, DMA, or ISA master can not access the corresponding segment.

WE—Write Enable. When the WE bit (bit 7, 5, 3, 1) is set to a 1, the SIO generates MEMCS# for PCI master, DMA, or ISA master memory write accesses to the corresponding segment. When this bit is set to a 0, the SIO does not generate MEMCS# for PCI master memory write accesses to the corresponding segment. When the RE and WE bits are both 0 (or bit 4 in the MEMCS# Control Register is set to a 0–disabled), the PCI master, DMA, or ISA master can not access the corresponding segment.

Bit 7: 0CC000h–0CFFFFh Exp. ROM: WE

Bit 6: 0CC000h–0CFFFFh Exp. ROM: RE

Bit 5: 0C8000h–0CBFFFh Exp. ROM: WE

Bit 4: 0C8000h–0CBFFFh Exp. ROM: RE

Bit 3: 0C4000h–0C7FFFh Exp. ROM: WE

Bit 2: 0C4000h–0C7FFFh Exp. ROM: RE

Bit 1: 0C0000h–0C3FFFh Exp. ROM: WE

Bit 0: 0C0000h–0C3FFFh Exp. ROM: RE

4.1.23 MAR2—MEMCS# ATTRIBUTE REGISTER #2

Address Offset: 55h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

RE—Read Enable. When the RE bit (bit 6, 4, 2, 0) is set to a 1, the SIO generates MEMCS# for PCI master, DMA, or ISA master memory read accesses to the corresponding segment. When this bit is set to a 0, the SIO does not generate MEMCS# for PCI master memory read accesses to the corresponding segment. When the RE and WE bits are both 0 (or bit 4 in the MEMCS# Control Register is set to a 0–disabled), the PCI master, DMA, or ISA master can not access the corresponding segment.

WE—Write Enable. When the WE bit (bit 7, 5, 3, 1) is set to a 1, the SIO generates MEMCS# for PCI master, DMA, or ISA master memory write accesses to the corresponding segment. When this bit is set to a 0, the SIO does not generate MEMCS# for PCI master memory write accesses to the corresponding segment. When the RE and WE bits are both 0 (or bit 4 in the MEMCS# Control Register is set to a 0–disabled), the PCI master, DMA, or ISA master can not access the corresponding segment.

Bit 7: 0DC000h–0DFFFFh Exp. ROM : WE

Bit 6: 0DC000h–0DFFFFh Exp. ROM : RE

Bit 5: 0D8000h–0DBFFFh Exp. ROM : WE

Bit 4: 0D8000h–0DBFFFh Exp. ROM : RE

Bit 3: 0D4000h–0D7FFFh Exp. ROM : WE

Bit 2: 0D4000h–0D7FFFh Exp. ROM : RE

Bit 1: 0D0000h–0D3FFFh Exp. ROM : WE

Bit 0: 0D0000h–0D3FFFh Exp. ROM : RE

4.1.24 MAR3—MEMCS# ATTRIBUTE REGISTER #3

Address Offset: 56h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

RE—Read Enable. When the RE bit (bit 6, 4, 2, 0) is set to a 1, the SIO generates MEMCS# for PCI master, DMA, ISA master memory read accesses to the corresponding segment. When this bit is set to a 0, the SIO does not generate MEMCS# for PCI master memory read accesses to the corresponding segment. When the RE and WE bits are both 0 (or bit 4 in the MEMCS# Control Register is set to a 0–disabled), the PCI master can not access the corresponding segment.

WE—Write Enable. When the WE bit (bit 7, 5, 3, 1) is set to a 1, the SIO generates MEMCS# for PCI master, DMA, ISA master memory write accesses to the corresponding segment. When this bit is set to a 0, the SIO does not generate MEMCS# for PCI master memory write accesses to the corresponding segment. When the RE and WE bits are both 0 (or bit 4 in the MEMCS# Control Register is set to a 0–disabled), the PCI master can not access the corresponding segment.

Bit 7: 0EC000h–0EFFFFh Lower 64 KByte BIOS: WE

Bit 6: 0EC000h–0EFFFFh Lower 64 KByte BIOS: RE

Bit 5: 0E8000h–0EBFFFh Lower 64 KByte BIOS WE

Bit 4: 0E8000h–0EBFFFh Lower 64 KByte BIOS: RE

Bit 3: 0E4000h–0E7FFFh Lower 64 KByte BIOS: WE

Bit 2: 0E4000h–0E7FFFh Lower 64 KByte BIOS: RE

Bit 1: 0E0000h–0E3FFFh Lower 64 KByte BIOS: WE

Bit 0: 0E0000h–0E3FFFh Lower 64 KByte BIOS: RE

4.1.25 DMA SCATTER/GATHER RELOCATION BASE ADDRESS REGISTER

Address Offset: 57h
Default Value: 04h
Attribute: Read/Write
Size: 8 bits

The value programmed into this register determines the high order I/O address of the Scatter/Gather Command Registers, Scatter/Gather Status Registers, and the Scatter/Gather Descriptor Table Registers. The default value is 04h so the first S/G register default address is at 0410h.

Bit 7: A15

Bit 6: A14

Bit 5: A13

Bit 4: A12

Bit 3: A11

Bit 2: A10

Bit 1: A9

Bit 0: A8

4.1.26 PIRQ[3:0]#—PIRQ ROUTE CONTROL REGISTERS

Register Name: PIRQ0#, PIRQ1#, PIRQ2#, PIRQ3# Route Control

Address Offset: 60h, 61h, 62h, 63h
Default Value: 80h
Attribute: Read/Write
Size: 8 bits

These registers control the routing of PCI Interrupts (PIRQ[0:3]#) to the PC compatible Interrupts. Each PCI interrupt can be independently routed to 1 of 11 compatible interrupts. Note that two or more PCI interrupts (PIRQ[3:0]#) can be steered into the same IRQ signal (the interrupts are level sensitive and can be shared).

Each IRQ to which a PCI Interrupt is steered into must have its interrupt set to level sensitive in the Edge/Level Control Register.

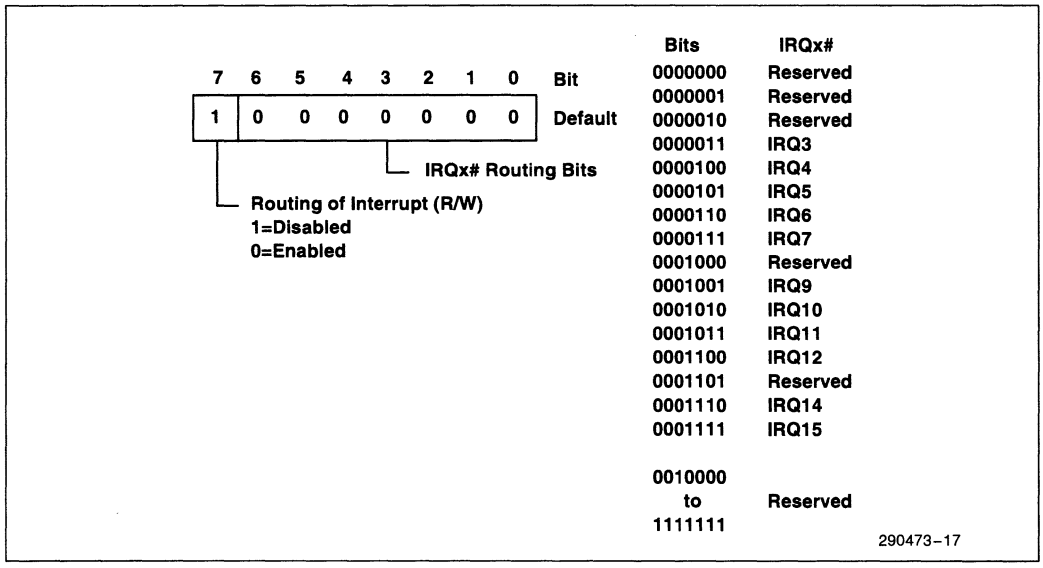


Figure 3. PIRQ Route Control Registers

Bit 7: Routing of Interrupts
When enabled, this bit routes the PCI Interrupt signal to the PC compatible interrupt signal specified in bits[3:0]. At reset, this bit is disabled (set to 1).

Bits[6:4]: Reserved
Read as 0's.

Bits[3:0]: IRQx# Routing Bits
These bits specify which IRQ signal to generate.

4.1.27 BIOS TIMER BASE ADDRESS REGISTER

Address Offset: 80h–81h
Default value: 0078h
Attribute: Read/Write
Size: 16 bits

This register determines the base address for the BIOS Timer Register located in the I/O space. The base address can be set at Dword boundary anywhere in the 64 KByte I/O space. This register also provides the BIOS Timer access enable/disable control bit.

Bits[15:2]: BIOS Timer Base Address
Bits[15:2] correspond to PCI address lines A[15:2].

Bit 1: Reserved

Bit 0: BIOS Timer Access Enable
When bit 0 = 1, access to the BIOS Timer is enabled. When bit 0 = 0, access to the BIOS Timer is disabled. The default value is 0 (disabled).

4.1.28 SMICNTL—SMI CONTROL REGISTER

Address Offset: A0h
Default value: 08h
Attribute: Read/Write
Size: 8 bits

Bit 7: Reserved
Reserved for future Intel use.

Bit 6: Reserved
Reserved for future Intel use.

Bits[5:4]: Reserved
Reserved for future Intel use.

Bit 3: CTMRFRZ
Used to freeze the timers when in SMM. When this bit is set, the Fast Off timer will stop counting. This prevents time-outs from occurring while executing SMM code.

Bit 2: CSTPCLKTH
When set, the STPCLK# throttle is enabled.

Bit 1: CSTPCLKEN
When set, a read from the APMC register will cause STPCLK# to be asserted. CSTPCLKEN will be cleared by writing it to 0 or by any write to the APMC register. Enables SW to put the CPU into a low power state.

Bit 0: CSMIGATE
When this bit is written to "0" SMI# will be deasserted. When this bit is written to a "1", SMI# will be asserted if any SMIs are pending.

4.1.29 SMIEN—SMI ENABLE REGISTER

Address Offset: A2h–A3h
Default value: 0000h
Attribute: Read/Write
Size: 16 bits

The following bits control the enabling of associated hardware events that will generate an SMI. When set to a "1", SMI# will be asserted when the associated event occurs. When bit 7 is set, writes to the APM Control port (APMC) will generate an SMI.

Bits[15:8]: Reserved
Will be read as 0. Writes have no effect.

Bit 7: SAPMCEN
Write to APM Control Port.

Bit 6: SEXTSMIEN
EXTSMI# input asserted.

Bit 5: SFOFFTMREN
Fast Off (Idle) Timer Enable.

Bit 4: SIRQ12EN
PS/2 Mouse Interrupt.

Bit 3: SIRQ8EN
RTC Alarm Interrupt.

Bit 2: SIRQ4EN
COM2/COM4 Interrupt (Mouse).

Bit 1: SIRQ3EN
COM1/COM3 Interrupt (Mouse).

Bit 0: SIRQ1EN
Keyboard Interrupt.

4.1.30 SEE—SYSTEM EVENT ENABLE REGISTER

Address Offset:	A4h, A5h, A6h, A7h
Default value:	00000000h
Attribute:	Read/Write
Size:	32 bits

These bits are used to enable the corresponding hardware events as system events. When set to a "1", anytime the associated hardware event occurs, the Fast Off Timer is reloaded with its initial count. Also, when enabled the associated hardware system event is recognized as a Break Event causing STPCLK# to be deasserted.

Bit 31: FSMIEN
Prevents the system from entering Fast Off and causes STPCLK# to be deasserted when an SMI occurs.

Bit 30: Reserved
Will be read as 0. Writes have no effect.

Bit 29: FNMIEN
Prevents the system from entering Fast Off and causes STPCLK# to be deasserted when an NMI occurs (parity error for example).

Bits[28:16]: Reserved
Will be read as 0. Writes have no effect.

Bits[15:3]: FIRQ[15:3]EN
This prevents the system from entering Fast Off and causes STPCLK# to be deasserted when selected hardware interrupts occur.

Bit 2: Reserved
Will be read as 0. Writes have no effect.

Bits[1:0]: FIRQ[1:0]EN
Prevents the system from entering Fast Off and causes STPCLK# to be deasserted when selected hardware interrupts occur.

4.1.31 FTMR—FAST OFF TIMER

Address Offset:	A8h
Default value:	0Fh
Attribute:	Read/Write
Size:	8 bits

The Fast Off Timer is used to indicate (through an SMI) that the system has been idle for a pre-programmed period of time. The Fast Off Timer consists of a count down timer that is decremented every minute. The value programmed into this register gets loaded into the Fast Off Timer when an enabled system event occurs. Each count represents one minute. When the timer expires, an SMI Special Cycle is generated. Writes to the FTMRLD register cause the Fast Off Timer to be loaded. When this register is read, the value last written to this register is returned.

PROGRAMMER'S NOTE:
Before writing to the FTMRLD register the Fast Off Timer must be stopped by writing a "1" to the CTMRFRZ bit. The Fast Off Timer will begin decrementing when the CTMRFRZ bit is subsequently set to "0".

Bits[7:0]: FTMRLD[7:0]
A write to the FTMRLD register when the Fast Off Timer is stopped (CTMRFRZ = 1) will load the Fast Off Timer with the value being written to FTMRLD register. When the Fast Off Timer is enabled (CTMRFRZ = 0) it counts down from the value loaded into it. When the Fast Off Timer reaches 00h it will trigger an SMI. If an enabled system event occurs before the Fast Off Timer reaches 00h the Fast Off Timer is reloaded with the value stored in the FTMRLD register. A read from the FTMRLD register will return the value last written to this register.

4.1.32 SMIREQ-SMI REQUEST REGISTER

Address Offset: AAh, ABh
Default value: 00h
Attribute: Read/Write
Size: 16 bits

These bits are status bits indicating the cause of the SMI. When an enabled event causes an SMI, the hardware automatically sets the corresponding event's request bit. The request bits are cleared by writing a "0" to them. Only the hardware can set request bits to a "1". In the event that the hardware is trying to set the bit to a "1" at the same time that it is being cleared, the hardware set to "1" will dominate.

Bits[15:8]: Reserved
Reserved for future Intel use.

Bit 7: RAPMC
When set to a "1" indicates that a write to the APM Control Port caused an SMI#.

Bit 6: REXT
When set to a "1", indicates that EXTSMI# was sampled asserted, causing an SMI#.

Bit 5: RFOFFTMR
Fast Off Timer expired causing an SMI#.

Bit 4: RIRQ12
IRQ12 was asserted causing an SMI#.

Bit 3: RIRQ8
IRQ8 was asserted causing an SMI#.

Bit 2: RIRQ4
IRQ4 was asserted causing an SMI#.

Bit 1: RIRQ3
IRQ3 was asserted causing an SMI#.

Bit 0: RIRQ1
IRQ1 was asserted causing an SMI#.

4.1.33 CTLTMRL—CLOCK THROTTLE STPCLK# LOW TIMER

Address Offset: ACh
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The value in this register defines the duration of the STPCLK# asserted period when the CSTPCLKTH bit is set. The value in this register is loaded into the STPCLK# Timer when STPCLK# is asserted. The STPCLK# timer runs off a 32 μs clock. Note that the timer does not begin to count until the Stop Grant Special Cycle is received.

Bits[7:0]: KSTPLOLD[7:0]
The value in this register defines the duration of the STPCLK# asserted period when the CSTPCLKTH bit is set.

4.1.34 CTLTMRH—CLOCK THROTTLE STPCLK# HIGHTIMER

Address Offset: AEh
Default value: 00h
Attribute: Read/Write
Size: 8 bits

The value in this register defines the duration of the STPCLK# deasserted period when the CSTPCLKTH bit is set. The value in this register is loaded into the STPCLK# Timer when STPCLK# is deasserted. The STPCLK# timer runs off a 32 μs clock.

Bits[7:0]: KSTPHILD[7:0]
The value in this register defines the duration of the STPCLK# deasserted period when the CSTPCLKTH bit is set.

4.2 DMA Register Description

The SIO contains DMA circuitry that incorporates the functionality of two 82C37 DMA controllers (DMA1 and DMA2). The DMA registers control the operation of the DMA controllers and are all accessible from the PCI Bus via PCI I/O space. In addition, some of the registers are accessed from the ISA Bus via ISA I/O space. Table 4, at the beginning of Section 4.0 lists the bus access for each register.

This section describes the DMA registers. Unless otherwise stated, a PCIRST# sets each register to its default value. The operation of the DMA is further described in Section 5.4, DMA Controller.

4.2.1 DCOM—DMA COMMAND REGISTER

Address Offset:	Channels 0-3–08h Channels 4–7–0D0h
Default Value:	00h
Attribute:	Write Only
Size:	8 bits

This 8-bit register controls the configuration of the DMA. It is programmed by the microprocessor in the Program Condition and is cleared by PCIRST# or a Master Clear instruction. Note that disabling channels 4–7 also disables channels 0–3, since channels 0–3 are cascaded onto channel 4. The DREQ and DACK# channel assertion sensitivity is assigned by channel group, not per individual channel. For priority resolution, the DMA consists of two logical channel groups—channels 0–3 (Controller 1-DMA1) and channels 4–7 (Controller 2-DMA2). Each group can be assigned fixed or rotating priority. Both groups can be assigned fixed priority, one group can be assigned fixed priority and the second rotating priority, or both groups can be assigned rotating priority. Following a PCIRST# or DMA Master Clear, both DMA1 and DMA2 are enabled in fixed priority, the DREQ sense level is active high, and the DACK# assertion level is active low.

Bit 7: DACK# Assert Level (DACK#[3:0], [7:5])
Bit 7 controls the DMA channel request acknowledge (DACK#) assertion level. Following PCIRST#, the DACK# assertion level is active low. The low level indicates recognition and acknowledgment of the DMA request to the DMA slave requesting service. Writing a 0 to bit 7 assigns active low as the assertion level. When a 1 is written to this bit, a high level on the DACK# line indicates acknowledgment of the request for DMA service to the DMA slave.

Bit 6: DREQ Sense Assert Level (DREQ[3:0], [7:5])
Bit 6 controls the DMA channel request (DREQ) assertion detect level. Following PCIRST#, the DREQ sense assert level is active high. In this condition, an active high level sampled on DREQ is decoded as an active DMA channel request. Writing a 0 to bit 6 assigns active high as the sense assert level. When a 1 is written to this bit, a low level on the DREQ line is decoded as an active DMA channel request.

Bit 5: Reserved
Must be 0.

Bit 4: DMA Group Arbitration Priority
Each channel group is individually assigned either fixed or rotating arbitration priority. At PCIRST#, each group is initialized in fixed priority. Writing a 0 to bit 4 assigns fixed priority to the channel group, while writing a 1 assigns rotating priority to the group.

Bit 3: Reserved
Must be 0.

Bit 2: DMA Channel Group Enable
Writing a 1 to this bit disables the DMA channel group, while writing a 0 to this bit enables the DMA channel group. Both channel groups are enabled following PCIRST#. Disabling channel group 4–7 also disables channel group 0–3, which is cascaded through channel 4.

Bits[1:0]: Reserved
Must be 0.

4.2.2 DCM—DMA CHANNEL MODE REGISTER

Register Name:	DMA Channel Mode
Address Offset:	Channels 0-3–0Bh Channels 4-7–0D6h
Default Value:	Bits[7:2] = 0, Bits[1:0] = undefined
Attribute:	Write Only
Size:	6 bits

Each channel has a 6-bit DMA Channel Mode Register. The Channel Mode Registers provide control over DMA Transfer type, transfer mode, address increment/decrement, and autoinitialization. Bits[1:0] select the appropriate Channel Mode Register and are not stored. Only bits[7:2] are stored in the register. This register is set to its default value upon

PCIRST# or Master Clear. Its default value is Verify transfer, Autoinitialize disable, Address increment, and Demand mode. Channel 4 defaults to cascade mode and cannot be programmed for any mode other than cascade mode.

Bits[7:6]: DMA Transfer Mode
Each DMA channel can be programmed in one of four different modes: single transfer, block transfer, demand transfer and cascade.

Bits	7	6	Transfer Mode
	0	0	Demand mode
	0	1	Single mode
	1	0	Block mode
	1	1	Cascade mode

Bit 5: Address Increment/Decrement Select
Bit 5 controls address increment/decrement during multi-byte DMA transfers. When bit 5 = 0, address increment is selected. When bit 5 = 1, address decrement is selected. Address increment is the default after a PCIRST# cycle or Master Clear command.

Bit 4: Autoinitialize Enable
When bit 4 = 1, the DMA restores the Base Page, Address, and Word count information to their respective current registers following a terminal count (TC). When bit 4 = 0, the autoinitialize feature is disabled and the DMA does not restore the above mentioned registers. A PCIRST# or Master Clear disables autoinitialization (sets bit 4 to 0).

Bits[3:2]: DMA Transfer Type
Verify, write and read transfer types are available. Verify transfer is the default transfer type upon PCIRST# or Master Clear. Write transfers move data from an I/O device to memory. Read transfers move data from memory to an I/O device. Verify transfers are pseudo transfers; addresses are generated as in a normal read or write transfer and the device responds to EOP etc. However, with Verify transfers, the ISA memory and I/O cycle lines are not driven. Bit combination 11 is illegal. When the channel is programmed for cascade ([7:6] = 11) the transfer type bits are irrelevant.

Bits	3	2	Transfer Mode
	0	0	Verify transfer
	0	1	Write transfer
	1	0	Read Transfer
	1	1	Illegal

Bits[1:0]: DMA Channel Select
Bits[1:0] select the DMA Channel Mode Register that will be written by bits[7:2].

Bits	1	0	Channel
	0	0	Channel 0 (4)
	0	1	Channel 1 (5)
	1	0	Channel 2 (6)
	1	1	Channel 3 (7)

4.2.3 DCEM—DMA CHANNEL EXTENDED MODE REGISTER

Address Offset: Channels 0-3–040Bh
Channels 4-7–04D6h
Default Value: Bits[1:0] = undefined,
Bits[3:2] = 00 for DMA1,
Bits[3:2] = 01 for DMA2,
Bits[7:4] = 0
Attribute: Write Only
Size: 6 bits

Each channel has a 6-bit Extended Mode Register. The register is used to program the DMA device data size, timing mode, EOP input/output selection, and Stop Register selection. Bits[1:0] select the appropriate Channel Extend Mode Register and are not stored. Only bits[7:2] are stored in the register. Four timing modes are available: ISA-compatible, "A", "B", and "F". Timings "A", "B", and "F" are extended timing modes and can only be run to main memory. DMA cycles to ISA expansion bus memory defaults to compatible timing if the channel is programmed in an extended timing mode.

The default bit values for each DMA group are selected upon PCIRST#. A Master Clear or any other programming sequence will not set the default register settings. The default programmed values for DMA1 channels 0-3 are 8-bit I/O count by bytes, compatible timing, and EOP output. The default values for DMA2 channels 4-7 are 16-bit I/O count by words with shifted address, compatible timing, and EOP output.

Bit 7: Reserved
Must be 0.

Bit 6: EOP Input/Output Selection
Bit 6 selects whether the EOP signal is to be used as an output during DMA transfers on this channel or an input. EOP is typically used as an output, as was available on the PC/AT. The input function was added to support data communication and other devices that would like to trigger an autoinitialize when a collision or some other event occurs. The direction of EOP is switched when DACK is changed (when a different channel is granted the bus). There may be some overlap of the SIO driving the EOP signal along with the DMA slave. However, during this overlap, both devices drive the signal to a low level (inactive). For example, assume channel 2 is about to go inactive (DACK negating) and channel 1 is about to go active. In addition, assume that channel 2 is programmed for "EOP OUT" and channel 1 is programmed for "EOP IN". When channel 2's DACK is negated and channel 1's DACK is asserted, the SIO may be driving EOP to a low value on behalf of channel 2. At the same time the device connected to channel 1 is driving EOP in to the SIO, also at an inactive level. This overlap only lasts until the SIO EOP output buffer is tri-stated, and does not effect the DMA operation. Upon PCIRST#, bit 6 is set to 0-EOP output selected.

Bits[5:4]: DMA Cycle Timing Mode
The SIO supports four DMA transfer timings: ISA-compatible, type "A", "B", and "F". Each timing and its corresponding code are described below. Upon PCIRST#, compatible timing is selected and the value of these bits is "00". The cycle timings noted below are for a SYSCLK (8.33 MHz, maximum SYSCLK frequency). DMA cycles to ISA expansion bus memory defaults to compatible timing if the channel is programmed in one of the performance timing modes (type "A", "B", or "F").

Bits[5:4] = 00: Compatible Timing
Compatible timing is provided for DMA slave devices, that, due to some design limitation, cannot support one of the faster timings. Compatible timing runs at 9 SYSCLKs (1080 nsec/single cycle) and 8 SYSCLKs (960 nsec/cycle) during the repeated portion of a BLOCK or DEMAND mode transfer.

Bits[5:4] = 01: Type "A" Timing
Type "A" timing is provided to allow shorter cycles to main memory (via the PCI Bus). Type "A" timing runs at 6 SYSCLKs (720 nsec/cycle) during the repeated portion of a BLOCK or DEMAND mode transfer. Type "A" timing varies from compatible timing primarily in shortening the memory operation to the minimum allowed main memory. The I/O portion of the cycle (data setup on write, I/O read access time) is the same as with compatible cycles. The actual active command time is shorter. However, it is expected that the DMA devices that provide the data access time or write data setup time should not require excess IOR# or IOW# command active time. Because of this, most ISA DMA devices should be able to use type "A" timing.

Bits[5:4] = 10: Type "B" Timing
Type "B" timing is provided for 8/16-bit ISA DMA devices that can accept faster I/O timing. Type "B" only works with fast main memory. Type "B" timing runs at 5 SYSCLKs (600 nsec/cycle) during the repeated portion of a BLOCK or DEMAND mode transfer. Type "B" timing requires faster DMA slave devices than compatible timing. In Type "B" timing the cycles are shortened so that the data setup time on I/O write cycles is shortened and the I/O read access time is required to be faster.

Bits[5:4] = 11: Type "F" Timing
Type "F" timing provides high performance DMA transfer capability. Type "F" timing runs at 3 SYSCLKs (360 nsec/single cycle) during the repeated portion of a BLOCK or DEMAND mode transfer, resulting in a maximum data transfer rate of 8.33 MBytes/second.

Bits[3:2]: Addressing Mode
The SIO supports both 8- and 16-bit DMA device data sizes. Three data size options are programmable with bits[3:2]. Both the 8-bit I/O, "count by bytes" mode and the 16-bit I/O, "count by words" (address shifted) mode are ISA compatible. The 16-bit I/O, "count by bytes" mode is offered as an extension of the ISA compatible modes. Bits[3:2] = 10 is reserved. Byte assembly/disassembly is performed by the ISA control unit. Each of the data transfer size modes is discussed below.

Bits[3:2] = 00: 8-bit I/O, "Count By Bytes" Mode
In 8-bit I/O, "count by bytes" mode, the Current Address Register can be programmed to any address. The Current Byte/Word Count Register is programmed with the "number of bytes minus 1" to transfer.

Bits[3:2] = 01: 16-bit I/O, "Count By Words" (Address Shifted) Mode
In "count by words" mode (address shifted), the Current Address Register can be programmed to any even address, but must be programmed with the address value shifted right by one bit. The Low Page and High Page Registers are not shifted during DMA transfers. Thus, the least significant bit of the Low Page register is ignored when the address is driven out onto the bus. The Current Byte/Word Count Register is programmed with the number of words minus 1 to be transferred.

Bits[3:2] = 10: Reserved

Bits[3:2] = 11: 16-Bit I/O, "Count By Bytes" Mode
In 16-bit "count by bytes" mode, the Current Address Register can be programmed to any byte address. For most DMA devices, however, it should be programmed only to even addresses. If the address is programmed to an odd address, the DMA controller does a partial word transfer during the first and last transfer, if necessary. The bus controller does the Byte/Word assembly necessary to write any size memory device. In this mode, the Current Address Register is incremented or decremented by two and the byte count is decremented by the number of bytes transferred during each bus cycle. The Current Byte/Word Count Register is programmed with the "number of bytes minus 1" to be transferred. This mode should only be programmed for 16-bit ISA DMA slaves.

Bits[1:0]: DMA Channel Select
Bits[1:0] select the particular channel that will have its DMA Channel Extend Mode Register programmed with bits[7:2].

Bits	1	0	Channel
	0	0	Channel 0 (4)
	0	1	Channel 1 (5)
	1	0	Channel 2 (6)
	1	1	Channel 3 (7)

4.2.4 DR—DMA REQUEST REGISTER

Address Offset:	Channels 0-3–09h Channels 4-7–0D2h
Default Value:	Bits[1:0] = undefined, Bits[7:2] = 0
Attribute:	Write Only
Size:	4 bits

Each channel has a request bit in one of the two 4-bit DMA Request Registers. The Request Register is used by software to initiate a DMA request. The DMA responds to the software request as though DREQ[x] is asserted. These requests are non-maskable and subject to prioritization by the priority encoder network. Each register bit is set to 1 or 0 separately under software control or is set to 0 upon generation of a TC. The entire register is set to 0 upon PCIRST# or a Master Clear. It is not affected upon a RSTDRV output. To program a bit, the software loads the proper form of the data word. Bits[1:0] determine which channel Request Register will be written. In order to make a software request, the channel must be in Block Mode. The Request Register status for DMA1 and DMA2 is output on bits[7:4] of a Status Register read to the appropriate port.

Bits[7:3]: Reserved
Must be 0.

Bit 2: DMA Channel Service Request
Writing a 0 to bit 2 resets the individual software DMA channel request bit. Writing a 1 to bit 2 sets the request bit. The request bit for each DMA channel is reset to 0 upon a PCIRST# or a Master Clear.

Bits[1:0]: DMA Channel Select
Bits[1:0] select the DMA channel mode register to program with bit 2.

Bits	1	0	Channel
	0	0	Channel 0
	0	1	Channel 1 (5)
	1	0	Channel 2 (6)
	1	1	Channel 3 (7)

4.2.5 MASK REGISTER—WRITE SINGLE MASK BIT

Address Offset: Channels 0-3–0Ah
Channels 4-7–0D4h
Default Value: Bits[1:0] = undefined, Bit 2 = 1, Bits[7:3] = 0
Attribute: Write Only
Size: 1 bit/channel

Each DMA channel has a mask bit that enables/disables an incoming DMA channel service request DREQ[x]. Two 4-bit registers store the current mask status for DMA1 and DMA2. Setting the mask bit disables the incoming DREQ[x] for that channel. Clearing the mask bit enables the incoming DREQ[x]. A channel's mask bit is automatically set when the Current Byte/Word Count register reaches terminal count (unless the channel is programmed for autoinitialization). Each mask bit may also be set or cleared under software control. The entire register is also set by a PCIRST# or a Master Clear. Setting the entire register disables all DMA requests until a clear mask register instruction allows them to occur. This instruction format is similar to the format used with the DMA Request Register.

Individually masking DMA channel 4 (DMA controller 2, channel 0) will automatically mask DMA channels [3:0], as this channel group is logically cascaded onto channel 4. Setting this mask bit disables the incoming DREQ's for channels [3:0].

Bits[7:3]: Reserved
Must be 0.

Bit 2: Channel Mask Select
When bit 2 is set to a 1, DREQ is disabled for the selected channel. When bit 2 is set to a 0, DREQ is enabled for the selected channel.

Bit[1:0]: DMA Channel Select
Bits[1:0] select the DMA Channel Mode Register to program with bit 2.

Bits	1	0	Channel
	0	0	Channel 0 (4)
	0	1	Channel 1 (5)
	1	0	Channel 2 (6)
	1	1	Channel 3 (7)

4.2.6 MASK REGISTER—WRITE ALL MASK BITS

Address Offset: Channels 0-3–0Fh
Channels 4-7–0DEh
Default Value: Bit[3:0] = 1, Bit[7:4] = 0
Attribute: Read/Write
Size: 4 bits

Writing to this register enables/disables incoming DREQ assertions. There are four mask bits per register, one for each channel. This permits all four channels to be simultaneously enabled/disabled instead of enabling/disabling each channel individually, as is the case with the Mask Register—Write Single Mask Bit.

Two 4-bit registers store the current mask status for DMA1 and DMA2. Unlike the Mask Register—Write Single Mask Bit, this register and includes a status read to check the current mask status of the selected DMA channel group. A channel's mask bit is automatically set to 1 when the Current Byte/Word Count Register reaches terminal count (unless the channel is programmed for autoinitialization). Bits[3:0] are set to 1 by a PCIRST# or a Master Clear. Setting bits[3:0] to 1 disables all DMA requests until a clear mask register instruction enables the requests.

Two important points should be taken into consideration when programming the mask registers. First, individually masking DMA channel 4 (DMA controller 2, channel 0) will automatically mask DMA channels [3:0], as this channel group is logically cascaded onto channel 4. Second, masking DMA controller 2 with a write to port 0DEh will also mask DREQ assertions from DMA controller 1 for the same reason. When DMA channel 4 is masked, so are DMA channels 0-3.

Bits[7:4]: Reserved
Must be 0.

Bits[3:0]: Channel Mask Bits
Setting the bit(s) to a 1 disables the corresponding DREQ(s). Setting the bit(s) to a 0 enables the corresponding DREQ(s). Bits[3:0] are set to 1 upon PCIRST# or Master Clear. When read, bits[3:0] indicate the DMA channel [3:0] ([7:4]) mask status.

Bit	Channel
0	0 (4)
1	1 (5)
2	2 (6)
3	3 (7)

NOTE:
Disabling channel 4 also disables channels 0-3 due to the cascade of DMA1 through channel 4 of DMA2.

4.2.7 DS—DMA STATUS REGISTER

Address Offset: Channels 0-3–08h
Channels 4-7–0D0h
Default Value: 00h
Attribute: Read Only
Size: 8 bits

Each DMA controller has a read-only DMA Status Register. This register indicates which channels have reached terminal count and which channels have a pending DMA request. Bits[3:0] are set every time the corresponding TC is reached by that channel. Bits[3:0] are set to 0 upon PCIRST# and on each status read. Bits[7:4] are set whenever their corresponding channel is requesting service.

Bits[7:4]: Channel Request Status
When a valid DMA request is pending for a channel (on its DREQ signal line), the corresponding bit is set to 1. When a DMA request is not pending for a particular channel, the corresponding bit is set to 0. The source of the DREQ may be hardware, a timed-out block transfer, or a software request. Note that channel 4 does not have DREQ or DACK lines, so the response for a read of DMA2 status for channel 4 is irrelevant.

Bit	Channel
4	0
5	1 (5)
6	2 (6)
7	3 (7)

Bits[3:0]: Channel Terminal Count Status
When a channel reaches terminal count (TC), its status bit is set to 1. If TC has not been reached, the status bit is set to 0. Note that channel 4 is programmed for cascade, and is not used for a DMA transfer. Therefore, the TC bit response for a status read on DMA2 for channel 4 is irrelevant.

Bit	Channel
0	0
1	1 (5)
2	2 (6)
3	3 (7)

4.2.8 DMA BASE AND CURRENT ADDRESS REGISTERS (8237 COMPATIBLE SEGMENT)

Address Offset: DMA Channel 0–000h
DMA Channel 1–002h
DMA Channel 2–004h
DMA Channel 3–006h
DMA Channel 4–0C0h
DMA Channel 5–0C4h
DMA Channel 6–0C8h
DMA Channel 7–0CCh
Default Value: All bits undefined
Attribute: Read/Write
Size: 16 bits per channel

Each channel has a 16-bit Current Address Register. This register contains the value of the 16 least significant bits of the full 32-bit address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address Register during the transfer. This register is written to or read from by the PCI Bus or ISA Bus master in successive 8-bit bytes. The programmer must issue the "Clear Byte Pointer Flip-Flop" command to reset the internal byte pointer and correctly align the write prior to programming the Current Address Register. After clearing the Byte Pointer Flip-Flop, the first write to the Current Address Register programs the low byte, bits[7:0], and the second write programs the high byte, bits[15:8]. This procedure also applies to read cycles. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after a TC or EOP.

Each channel has a Base Address Register located at the same port address as the corresponding Current Address Register. These registers store the original value of their associated Current Address Registers. During autoinitialize these values are used to restore the Current Address Registers to their original values. The Base Registers are written simultaneously with their corresponding Current Address Register in successive 8-bit bytes. The Base Registers are write-only.

In Scatter/gather mode, these registers store the lowest 16 bits of the current memory address. During a Scatter/gather transfer, the DMA will load a reserve buffer into the base memory address register.

Bits[15:0]: Base and Current Address [15:0]
These bits represent the 16 least significant address bits used during DMA transfers. Together with the DMA Low Page Register, they form the ISA-compatible 24-bit DMA address. As an extension of the ISA compatible functionality, the DMA High Page Register completes the 32-bit address needed when implementing SIO extensions such as DMA to the PCI Bus slaves that can take advantage of full 32-bit addressability. Upon PCIRST# or Master Clear, the value of these bits is 0000h.

4.2.9 DMA BASE AND CURRENT BYTE/WORD COUNT REGISTERS (8237 COMPATIBLE SEGMENT)

Address Offset:	DMA Channel 0–001h
	DMA Channel 1–003h
	DMA Channel 2–005h
	DMA Channel 3–007h
	DMA Channel 4–0C2h
	DMA Channel 5–0C6h
	DMA Channel 6–0CAh
	DMA Channel 7–0CEh
Default Value:	All bits undefined
Attribute:	Read/Write
Size:	16 bits per channel

Each channel has a 16-bit Current Byte/Word Count Register. This register determines the number of transfers to be performed. The actual number of transfers is one more than the number programmed in the Current Byte/Word Count Register (i.e., programming a count of 100 results in 101 transfers). The Byte/Word count is decremented after each transfer. The intermediate value of the Byte/Word count is stored in the register during the transfer. When the value in the register goes from zero to 0FFFFh, a TC is generated.

Following the end of a DMA service the register may also be re-initialized by an autoinitialization back to its original value. Autoinitialize can only occur when a TC occurs. If it is not autoinitialized, this register has a count of FFFFh after TC.

When the Extended Mode Register is programmed for, or defaulted to, transfers to/from an 8-bit I/O, the Byte/Word count indicates the number of bytes to be transferred.

When the Extended Mode Register is programmed for, or defaulted to, transfers to/from a 16-bit I/O, with shifted address, the Byte/Word count indicates the number of 16-bit words to be transferred.

When the Extended Mode Register is programmed for transfers to/from a 16-bit I/O, the Byte/Word Count indicates the number of bytes to be transferred. The number of bytes does not need to be a multiple of two or four in this case.

Each channel has a Base Byte/Word Count Register located at the same port address as the corresponding Current Byte/Word Count Register. These registers store the original value of their associated Current Byte/Word Count Registers. During Autoinitialize these values are used to restore the Current registers to their original values. The Base registers are written simultaneously with their corresponding Current register in successive 8-bit bytes. The Base registers cannot be read by any external agents.

In Scatter/gather mode, these registers store the 16 bits of the current Byte/Word count. During Scatter/gather transfer, the DMA will load a reserve buffer into the base Byte/Word Count register.

Bits[15:0]: Base and Current Byte/Word Count
These bits represent the 16 byte/word count bits used when counting down a DMA transfer. Upon PCIRST# or Master Clear, the value of these bits is 0000h.

4.2.10 DMA MEMORY BASE LOW PAGE AND CURRENT LOW PAGE REGISTERS

Register Name: DMA Memory Current Low Page Register (Read/Write)
DMA Memory Base Low Page Register (Write Only)
Address Offset: DMA Channel 0–087h
DMA Channel 1–083h
DMA Channel 2–081h
DMA Channel 3–082h
DMA Channel 5–08Bh
DMA Channel 6–089h
DMA Channel 7–08Ah
Default Value: All bits undefined
Size: 8 bits per channel

Each channel has an 8-bit Low Page Register. The DMA memory Low Page Register contains the eight second most-significant bits of the 32-bit address. The register works in conjunction with the DMA controller's High Page Register and Current Address Register to define the complete (32-bit) address for the DMA channel. This 8-bit register is read or written directly. It may also be re-initialized by an autoinitialize back to its original value. Autoinitialize takes place only after a TC or EOP.

Each channel has a Base Low Page Address Register located at the same port address as the corresponding Current Low Page Register. These registers store the original value of their associated Current Low Page Registers. During autoinitialization, these values are used to restore the Current Low Page Registers to their original values. The 8-bit Base Low Page Registers are written simultaneously with their corresponding Current Low Page Register by the microprocessor. The Base Low Page registers are write only.

During Scatter/gather, these registers store the 8 bits from the third byte of the current memory address. During a Scater-Gather transfer, the DMA will load a reserve buffer into the base memory address register.

Bits[7:0]: DMA Low Page and Base Low Page [23:16]
These bits represent the eight second most significant address bits when forming the full 32-bit address for a DMA transfer. Upon PCIRST# or Master Clear, the value of these bits is 00h.

4.2.11 DMA MEMORY BASE HIGH PAGE AND CURRENT HIGH PAGE REGISTERS

Register Name: DMA Memory Current High Page Register (Read/Write)
DMA Memory Base High Page Register (Write Only)
Address Offset: DMA Channel 0–0487h
DMA Channel 1–0483h
DMA Channel 2–0481h
DMA Channel 3–0482h
DMA Channel 5–048Bh
DMA Channel 6–0489h
DMA Channel 7–048Ah
Default Value: All bits undefined
Size: 8 bits per channel

Each channel has an 8-bit Current High Page Register. The DMA memory Current High Page Register contains the eight most significant bits of the 32-bit address. The register works in conjunction with the DMA controller's Current Low Page Register and Current Address Register to define the complete (32-bit) address for the DMA channels and corresponds to the Current Address Register for each channel. This 8-bit register is read or written directly. It may also be autoinitialized back to its original value. Autoinitialize takes place only after a TC or EOP.

This register is set to 0 during the programming of both the Current Low Page Register and the Current Address Register. Thus, if this register is not programmed after the other address and Low Page Registers are programmed, then its value is 00h. In this case, the DMA channel operates the same as an 82C37 (from an addressing standpoint). This is the address compatibility mode.

If the high 8 bits of the address are programmed after the other addresses, then the channel modifies its operation to increment (or decrement) the entire 32-bit address. This is unlike the 82C37 "Page" register in the original PCs which could only increment to a 64 KByte boundary for 8-bit channels or 128 KByte boundary for 16-bit channels. This is extended address mode. In this mode, the ISA Bus controller generates the signals MEMR# and MEMW# only for addresses below 16 MBytes.

Each channel has a Base High Page Register located at the same port address as the corresponding Current High Page Register. These registers store the original value of their associated Current High Page Registers. During autoinitialize, these values are used to restore the Current High Page Registers to their original values. The 8-bit Base High Page Registers are written simultaneously with their corresponding Current High Page Register. The Base High Page Registers are write only.

During Scatter/Gather, these registers store the 8 bits from the highest byte of the current memory address. During a Scatter/Gather transfer, the DMA will load a reserve buffer into the base memory address register.

Bits[7:0]: DMA High Page and Base High Page [31:24]
These bits represent the eight most-significant address bits when forming the full 32-bit address for a DMA transfer. Upon PCIRST# or Master Clear, the value of these bits is 00h.

4.2.12 DMA CLEAR BYTE POINTER REGISTER

Address Offset:	Channels 0–3–00Ch Channels 4–7–0D8h
Default Value:	All bits undefined
Attribute:	Write Only
Size:	8 bits

Writing to this register executes the clear byte pointer command. This command is executed prior to writing or reading new address or word count information to the DMA. This command initializes the byte pointer flip-flop to a known state so that subsequent accesses to register contents will address upper and lower bytes in the correct sequence.

The clear byte pointer command clears the internal latch used to address the upper or lower byte of the 16-bit Address and Word Count Registers. The latch is also cleared at power on by PCIRST# and by the Master Clear command. The Host CPU may read or write a 16-bit DMA controller register by performing two consecutive accesses to the I/O port. The Clear Byte Pointer command precedes the first access. The first I/O write to a register port loads the least significant byte, and the second access automatically accesses the most significant byte.

When DMA registers are being read or written, two Byte Pointer flip-flops are used. One flip-flop is for Channels 0–3 and one for Channels 4–7. Both of these act independently. There are separate software commands for clearing each of them (0Ch for Channels 0–3, 0D8h for Channels 4–7).

Bits[7:0]: Clear Byte Pointer
No specific pattern. Command enabled with a write to the I/O port address.

4.2.13 DMC—DMA MASTER CLEAR REGISTER

Address Offset:	Channel 0–3–00Dh Channel 4–7–0DAh
Default Value:	All bits undefined
Attribute:	Write Only
Size:	8 bit

This software instruction has the same effect as the hardware Reset. The Command, Status, Request, and Internal First/Last Flip-Flop registers are cleared and the Mask Register is set. The DMA controller enters the idle cycle. There are two independent Master Clear Commands; 0Dh acts on Channels 0–3, and 0DAh acts on Channels 4–7.

Bits[7:0]: Master Clear
No specific pattern. Command enabled with a write to the I/O port address.

4.2.14 DCM—DMA CLEAR MASK REGISTER

Address Offset:	Channel 0–3–00Eh Channel 4–7–0DCh
Default Value:	All bits undefined
Attribute:	Write Only
Size:	8 bit

This command clears the mask bits of all four channels, enabling them to accept DMA requests. I/O port 0Eh is used for Channels 0–3 and I/O port 0DCh is used for Channels 4–7.

Bits[7:0]: Clear Mask Register
No specific pattern. Command enabled with a write to the I/O port address.

4.2.15 SCATTER/GATHER COMMAND REGISTER

Register Name: DMA Scatter Gather Command

Address Offset: Channels 0 default address—0410h
Channels 1 default address—0411h
Channels 2 default address—0412h
Channels 3 default address—0413h
Channels 5 default address—0415h
Channels 6 default address—0416h
Channels 7 default address—0417h

Default Value: 00h
Attribute: Write Only, Relocatable
Size: 8 bits

The Scatter/Gather Command Register controls operation of the descriptor table aspect of scatter/gather transfers. This register can be used to start and stop a scatter/gather transfer. The register can also be used to select between IRQ13 and EOP to be asserted following a terminal count. The current scatter/gather transfer status can be read in the scatter/gather channel's corresponding Scatter/Gather Status Register. After a PCIRST# or Master Clear, IRQ13 is disabled and EOP is enabled.

Bit 7: IRQ13/EOP Select
Bit 7, if enabled via bit 6 of this register, selects whether EOP or IRQ13 is asserted at termination caused by a last buffer expiring. The last buffer can be either the last buffer in the list or the last buffer loaded in the DMA while it is suspended. If bit 7 = 1 (and bit 6 = 1), EOP is asserted when the last buffer is completed. If bit 7 = 0 (and bit 6 = 1), IRQ13 is asserted when the last buffer is completed.

EOP can be used to alert an expansion bus I/O device that a scatter/gather termination condition was reached. The I/O device, in turn, can assert its own interrupt request line to invoke a dedicated interrupt handling routine. IRQ13 should be used when the CPU needs to be notified directly.

Following PCIRST#, or Master Clear, the value stored for this bit is "1", and EOP is selected. Bit-6 must be set to a "1" to enable this bit during a S/G Command register write. When bit 6 is a "0" during the write, bit 7 will not have any effect on the current EOP/IRQ13 selection.

Bit 6: IRQ13/EOP Programming Enable
Enabling IRQ13/EOP programming allows initialization or modification of the S/G termination handling bits. When bit 6 = 0, bit 7 does not affect the state of IRQ13 or EOP assertion. When bit 6 = 1, bit 7 determines the termination handling following a terminal count.

Bits[5:2]: Reserved
Must be 0.

Bits[1:0]: Scatter/Gather Commands
This 2-bit field is used to start and stop scatter/gather.

Bits[1:0] = 00: No S/G operation
No S/G command operation is performed. Bits[7:6] may still be used to program IRQ13/EOP selection.

Bits[1:0] = 01: Start S/G Command
The Start command initiates the scatter/gather process. Immediately after the start command is issued (setting bits[1:0] to 01), a request is issued to fetch the initial buffer from the descriptor table to fill the Base Register set in preparation for performing a transfer. The buffer prefetch request has the same priority with respect to other channels as the DREQ it is associated with. Within the channel, DREQ is higher in priority than a prefetch request.

The Start command assumes the Base and Current registers are both empty and will request a prefetch automatically. Note that this command also sets the Scatter/Gather Status Register to S/G Active, Base Empty, Current Empty, not Terminated, and Next Null Indicator to 0. The EOP/IRQ13 bit will still reflect the last value programmed.

Bits[1:0] = 10: Stop S/G Command
The Stop command halts a Scatter/gather transfer immediately. When a Stop command is given, the Terminate bit in the S/G Status register and the DMA channel mask bit are both set.

Bits[1:0] = 11: Reserved

4.2.16 SCATTER/GATHER STATUS REGISTER

Address Offset:	Channels 0 default address—0418h Channels 1 default address—0419h Channels 2 default address—041Ah Channels 3 default address—041Bh Channels 5 default address—041Dh Channels 6 default address—041Eh Channels 7 default address—041Fh
Default Value:	00h
Attribute:	Read Only, Relocatable
Size:	8-bits

The Scatter/Gather Status Register contains information on the scatter/gather transfer status. This register provides dynamic status information on S/G transfer activity, the current and base buffer state, S/G transfer termination, and the End of the List indicator.

An Active bit is set to "1" after the S/G Start command is issued. The Active bit will be "0" before the initial Start command, following a terminal count, and after a S/G Stop command is issued. The Current Register and Base Register Status bits indicate whether the corresponding register has a buffer loaded. It is possible for the Base Register Status to be set while the Current Register Status is cleared. When the Current Register transfer is complete, the Base Register will not be moved into the Current Register until the start of the next data transfer. Thus, the Current Register State is empty (cleared), while the Base Register State is full (set). The Terminate bit is set active after a Stop command, after TC for the last buffer in the list, and both Base and Current Registers have expired. The EOP and IRQ13 bits indicate which end of process indicator will be used to alert the system of an S/G process termination. The EOL status bit is set if the DMA controller has loaded the last buffer of the Link List. Following PCIRST#, or Master Clear, each bit in this register is reset to "0".

Bit 7: Next Link Null Indicator
If the next scatter/gather descriptor fetched from memory during a fetch operation has the EOL value set to 1, the current value of the Next Link Register is not overwritten. Instead, bit 7 of the channel's Scatter/Gather Status Register is set to a 1. If the fetch returns a EOL value set to 0, this bit is set to 0. This status bit is written after every fetch operation. Following PCIRST#, or Master Clear, this bit is set to 0. This bit is also cleared by an S/G Start Command write to the Scatter/Gather Command Register.

Bit 6: Reserved

Bit 5: Issue IRQ13/EOP on Last Buffer
When bit 5 = 0, EOP was either defaulted to at reset or selected through the Scatter/Gather Command Register as the S/G process termination indicator. EOP is issued when a terminal count occurs or following the Stop Command. When bit 5 = 1, an IRQ13 is issued to alert the CPU of this same status.

Bit 4: Reserved

Bit 3: Scatter/Gather Base Register Status
When bit 3 = 0, the Base Register is empty. When bit 3 = 1, the Base Register has a buffer link loaded. Note that the Base Register State may be set while the Current Register state is cleared. This condition occurs when the Current Register expires following a transfer. The Base Register will not be moved into the Current Register until the start of the next DMA transfer.

Bit 2: Scatter/Gather Current Register Status
When bit 2 = 0, the Current Register is empty. When bit 2 = 1, the Current Register has a buffer link loaded and is considered full. Following PCIRST#, bit 2 is set to 0.

Bit 1: Reserved

Bit 0: Scatter/Gather Active
The Scatter/gather Active bit indicates the current S/G transfer status. Bit 0 is set to a 1 after an S/G Start Command is issued. Bit 0 is set to 0 before the Start Command is issued. Bit 0 is 0 after terminal count on the last buffer on the channel is reached. Bit 0 is also 0 after an S/G Stop Command has been issued. Following a PCIRST# or Master Clear, this bit is 0.

4.2.17 SCATTER/GATHER DESCRIPTOR TABLE POINTER REGISTER

Address Offset: Channel 0 default address—0420h–0423h
Channel 1 default address—0424h–0424h
Channel 2 default address—0428h–042Bh
Channel 3 default address—042Ch–042Ch
Channel 5 default address—0434h–0437h
Channel 6 default address—0438h–043Bh
Channel 7 default address—043Ch–043Fh
Default Value: All bits undefined
Attribute: Read/Write, Relocatable
Size: 32 bits

The Scatter/Gather Descriptor Table Pointer Register contains the 32-bit pointer address to the first scatter/gather descriptor entry in the descriptor table in memory. Before the start of a S/G transfer, this register should be programmed to point to the first descriptor in the Scatter/Gather Descriptor Table. Following a S/G Start command, the SIO reads the first SGD entry. Subsequently, at the end of the each buffer block transfer, the contents of the SGD Table pointer registers are incremented by 8 until the end of the SGD Table is reached.

The Scatter/Gather Descriptor Table Pointer Registers can be programmed with a single 32-bit PCI write.

Following a prefetch to the address pointed to by the channel's Scatter/Gather Descriptor Table Pointer Register, the new memory address is loaded into the Base Address Register, the new Byte Count is loaded into the Base Byte Count Register, and the newly fetched next scatter/gather descriptor replaces the current next scatter/gather value.

The end of the Scatter/Gather Descriptor Table is indicated by an End of Table field having a MSB equal to 1. When this value is read during a scatter/gather descriptor fetch, the current scatter/gather descriptor value is not replaced. Instead, bit 7 of the channel's Status Register is set to a 1, when the EOL is read from memory.

Bits[31:0]:
The Scatter/Gather Descriptor Table Pointer Register contains a 32-bit pointer address to the main memory location where the software maintains the Scatter Gather Descriptors for the linked-list buffers. Bits[31:0] correspond to A[31:0] on the PCI.

4.2.18 SCATTER/GATHER INTERRUPT STATUS REGISTER

Address Offset: 040Ah
Default Value: 00h
Attribute: Read Only, Relocatable
Size: 8 bits

The Scatter/Gather Interrupt Status Register is a read only register and is used to indicate the source (channel) of a DMA Scatter/Gather interrupt on IRQ13. The DMA controller drives IRQ13 active after reaching terminal count during a Scatter/Gather transfer. It does not drive IRQ13 active during the initial programming sequence that loads the Base registers.

Bit 7: Channel 7 Interrupt Status
When this bit is set to a 1, Channel 7 has an interrupt due to a Scatter/Gather Transfer; otherwise this bit is set to a 0.

Bit 6: Channel 6 Interrupt Status
When this bit is set to a 1, Channel 6 has an interrupt due to a Scatter/Gather Transfer; otherwise this bit is set to a 0.

Bit 5: Channel 5 Interrupt Status
When this bit is set to a 1, Channel 5 has an interrupt due to a Scatter/Gather Transfer; otherwise this bit is set to a 0.

Bit 4: Reserved
Read as 0.

Bit 3: Channel 3 Interrupt Status
When this bit is set to a 1, Channel 3 has an interrupt due to a Scatter/Gather Transfer; otherwise this bit is set to a 0.

Bit 2: Channel 2 Interrupt Status
When this bit is set to a 1, Channel 2 has an interrupt due to a Scatter/Gather Transfer; otherwise this bit is set to a 0.

Bit 1: Channel 1 Interrupt Status
When this bit is set to a 1, Channel 1 has an interrupt due to a Scatter/Gather Transfer; otherwise this bit is set to a 0.

Bit 0: Channel 0 Interrupt Status
When this bit is set to a 1, Channel 0 has an interrupt due to a Scatter/Gather Transfer; otherwise this bit is set to a 0.

4.3 Timer Register Description

The SIO contains three counters that are equivalent to those found in the 82C54 Programmable Interval Timer. The Timer registers control these counters and can be accessed from either the ISA Bus via ISA I/O space or the PCI Bus via PCI I/O space.

This section describes the counter/timer registers on the SIO. The counter/timer operations are further described in Section 5.7, Timer Unit.

4.3.1 TCW—TIMER CONTROL WORD REGISTER

Address Offset: 043h
Default Value: All bits undefined
Attribute: Write Only
Size: 8 bits

The Timer Control Word Register specifies the counter selection, the operating mode, the counter byte programming order and size of the count value, and whether the counter counts down in a 16-bit or binary-coded decimal (BCD) format. After writing the control word, a new count can be written at any time. The new value will take effect according to the programmed mode.

There are six programmable counting modes. Typically, the SIO Timer Counters 0 and 2 are programmed for Mode 3, the Square Wave Mode, while Counter 1 is programmed in Mode 2, the Rate Generator Mode.

Two special commands are selected through the Timer Control Word Register. The Read Back Command (see Section 4.3.1.1) is selected when bits[7:6] are both 1 and the Counter Latch Command (see Section 4.3.1.2) is selected when bits[5:4] are both 0. When either of these two commands are selected, the meaning of the other bits in the register changes.

Bits 4 and 5 are also used to select the count register programming mode. The read/write selection chosen with the control word indicates the programming sequence that must follow when initializing the specified counter. If a counter is programmed to read/write two byte counts, note that a program must not transfer control between writing the first and second byte to another routine that also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count. The count must always be completely loaded with both bytes.

Bits 6 and 7 are also used to select the counter for the control word being written.

Following PCIRST#, the control words for each register are undefined. Each timer must be programmed to bring it into a known state. However, each counter OUT signal is set to 0 following PCIRST#. The SPKR output, interrupt controller input IRQ0 (internal), bit 5 of port 061h, and the internally generated refresh request are each set to 0 following PCIRST#.

Bits[7:6]: Counter Select
The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1.

Bit	7	6	Function
	0	0	Counter 0 select
	0	1	Counter 1 select
	1	0	Counter 2 select
	1	1	Read Back Command (see Section 4.3.1.1)

Bits[5:4]: Read/Write Select
Bits[5:4] are the read/write control bits. The Counter Latch Command is selected when bits[5:4] are both 0. The read/write options include r/w least significant byte, r/w most significant byte, or r/w the LSB and then the MSB. The actual counter programming is done through the counter I/O port (040h, 041h, and 042h for counters 0, 1, and 2, respectively).

Bit	5	4	Function
	0	0	Counter Latch Command (see Section 4.3.1.2)
	0	1	R/W Least Significant Byte (LSB)
	1	0	R/W Most Significant Byte (MSB)
	1	1	R/W LSB then MSB

Bits[3:1]: Counter Mode Selection
Bits[3:1] select one of six possible modes of operation for the counter as shown below.

Bit 3	2	1	Mode	Function
0	0	0	0	Out signal on end of count (= 0)
0	0	1	1	Hardware retriggerable one-shot
X	1	0	2	Rate generator (divide by n counter)
X	1	1	3	Square wave output
1	0	0	4	Software triggered strobe
1	0	1	5	Hardware triggered strobe

Bit 0: Binary/BCD Countdown Select
When bit 0 = 0, a binary countdown is used. The largest possible binary count is 2^{16}. When bit 0 = 1, a binary coded decimal (BCD) count is used. The largest BCD count allowed is 10^4.

4.3.1.1 Read Back Command

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. The Read Back Command is written to the Timer Control Word Register which latches the current states of the above mentioned variables. The value of the counter and its status may then be read by I/O access to the counter address.

Status and/or count may be latched on one, two, or all three of the counters by selecting the counter during the register write. The count latched remains latched until read, regardless of further latch commands. The count must be read before newer latch commands latch a new count. The status latched by the Read Back Command also remains latched until after a read to the counter's I/O port by reading the Counter Access Ports Register. Thus, the status and count are unlatched only after a counter read of the Timer Status Byte Format Register, the Counter Access Ports Register, or the Timer Status Byte Register and Counter Access Ports Register in succession.

Both count and status of the selected counter(s) may be latched simultaneously by setting both bit 5 and bit 4 to 0. This is functionally the same as issuing two consecutive, separate Read Back Commands. As mentioned above, if multiple count and/or status Read Back Commands are issued to the same counter(s) without any intervening reads, all but the first are ignored.

If both count and status of a counter are latched, the first read operation from that counter returns the latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two byte counts) returns the latched count. Subsequent reads return an unlatched count.

NOTE:
The Timer Counter Register bit definitions are different during the Read Back Command than for a normal Timer Counter Register write.

Bits[7:6]: Read Back Command
When bits[7:6] are both 1, the Read Back Command is selected during a write to the Timer Control Word Register. As noted above, the normal meanings (mode, countdown, r/w select) of the bits in the control register at I/O address 043h change when the Read Back Command is selected. Following the Read Back Command, I/O reads from the selected counter's I/O addresses produce the current latch status, the current latched count, or both if bits 4 and 5 are both 0.

Bit 5: Latch Count of Selected Counters
When bit 5 = 1, the current count value of the selected counters will be latched. When bit 4 = 0, the status will not be latched.

Bit 4: Latch Status of Selected Counters
When bit 4 = 1, the status of the selected counters will be latched. When bit 4 = 0, the status will not be latched. The status byte format is described in Section 4.3.2, Interval Timer Status Byte Format Register.

Bit 3: Counter 2 Select
When bit 3 = 1, Counter 2 is selected for the latch command selected with bits 4 and 5. When bit 3 = 0, status and/or count will not be latched.

Bit 2: Counter 1 Select
When bit 2 = 1, Counter 1 is selected for the latch command selected with bits 4 and 5. When bit 2 = 0, status and/or count will not be latched.

Bit 1: Counter 0 Select
When bit 1 = 1, Counter 0 is selected for the latch command selected with bits 4 and 5. When bit 1 = 0, status and/or count will not be latched.

Bit 0: Reserved
Must be 0.

4.3.1.2 Counter Latch Command

The Counter Latch Command latches the current count value at the time the command is received. This command is used to insure that the count read from the counter is accurate (particularly when reading a two-byte count). The count value is then read from each counter's count register (via the Counter Access Ports Register). One, two or all three counters may be latched with one Counter Latch Command.

If a Counter is latched once and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

The count must be read according to the programmed format. Specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads).

NOTES:

1. If a counter is programmed to read/write two-byte counts, a program must not transfer control between reading the first and second byte to another routine that also reads from that same counter. Otherwise, an incorrect count will be read. Finish reading the latched two-byte count before transferring control to another routine.
2. The Timer Counter Register bit definitions are different during the Counter Latch Command than for a normal Timer Counter Register write.

Bits[7:6]: Counter Selection
Bits 6 and 7 are used to select the counter for latching.

Bit 7	6	Function
0	0	latch counter 0 select
0	1	latch counter 1 select
1	0	latch counter 2 select
1	1	Read Back Command select

Bits[5:4]: Counter Latch Command
When bits[5:4] are both 0, the Counter Latch Command is selected during a write to the Timer Control Word Register. As noted above, the normal meanings (mode, countdown, r/w select) of the bits in the control register at I/O address 043h change when the Counter Latch Command is selected. Following the Counter Latch Command, I/O reads from the selected counter's I/O addresses produce the current latched count.

Bits[3:0]: Reserved
Must be 0.

4.3.2 INTERVAL TIMER STATUS BYTE FORMAT REGISTER

Address Offset:	Counter 0–040h Counter 1–041h Counter 2–042h
Default Value:	Bits[6:0] = X, Bit 7 = 0
Attribute:	Read Only
Size:	8 bits per counter

Each counter's status byte can be read following an Interval Timer Read Back Command. The Read Back Command is programmed through the Timer Control Word Register. If latch status is chosen (bit 4 = 0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register returns the status byte. The status byte returns the countdown type, either BCD or binary; the counter operational mode; the read/write selection status; the Null count, also referred to as the count register status; and the current state of the counter OUT pin.

Bit 7: Counter OUT Pin State
When this bit is a 1, the OUT pin of the counter is also a 1. When this bit is a 0, the OUT pin of the counter is also a 0.

Bit 6: Count Register Status
Null Count, also referred to as the Count Status Register, indicates when the last count written to the Count Register (CR) has been loaded into the Counting Element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before the load time, the count value returned will not reflect the new count written to the register. When bit 6 = 0, the count has been transferred from CR to CE and is available for reading. When bit 6 = 1, the Null count condition exists. The count has not been transferred from CR to CE and is not yet available for reading.

Bits[5:4]: Read/Write Selection Status
Bits[5:4] reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection.

Bit 5	4	Function
0	0	Counter Latch Command
0	1	R/W Least Significant Byte (LSB)
1	0	R/W Most Significant Byte (MSB)
1	1	R/W LSB then MSB

Bits[3:1]: Mode Selection Status
Bits[3:1] return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above.

Bit 3	2	1	Mode Selected
0	0	0	0
0	0	1	1
X	1	0	2
X	1	1	3
1	0	0	4
1	0	1	5

Bit 0: Countdown Type Status
Bit reflects the current countdown type; either 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

4.3.3 COUNTER ACCESS PORTS REGISTER

Address Offset:	Counter 0, System Timer-040h Counter 1, Refresh Request-041h Counter 2, Speaker Tone-042h
Default Value:	All bits undefined
Attribute:	Read/Write
Size:	8 bits per counter

Each of these I/O ports is used for writing count values to the Count Registers; reading the current count value from the counter by either an I/O read, after a counter-latch command, or after a Read Back Command; and reading the status byte following a Read Back Command.

Bits[7:0]: Counter Port Bit[x]
Each counter I/O port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at I/O port address 043h. The counter I/O port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

4.3.4 BIOS TIMER REGISTER

Register Location:	Default = 78h–7Bh (Dword aligned)
Default Value:	0000xxxxh
Attribute:	Read/Write, Programmable
Size:	32 bit

A write to the BIOS Timer initiates a counting sequence. The timer can be initiated by writing either a 16-bit data portion or the entire 32-bit register (the upper 16 bits are don't cares). Bits[15:0] can be written with the initial count value to start the timer or read to check the current count value. It is the programmer's responsiblity to ensure that all 16 bits are written at the same time. After data is written into BIOS timer, the timer will start decrementing until it reaches zero. It will "freeze" at zero until the new count value is written.

The BIOS Timer consists of a single 32-bit register mapped in the I/O space on the location determined by the value written into the BIOS Timer Base Address Register. Bit 0 of the BIOS Timer Base Address Register enables/disables accesses to the BIOS Timer and must be 1 to enable access to the BIOS Timer Register. When the BIOS Timer is enabled, PCI accesses to the BIOS Timer Register do not flow through to the ISA Bus. If the BIOS Timer is disabled, accesses to the addresses assigned to the BIOS Timer Register flow through to the ISA bus. Note, however, that the counter continues to count normally.

Bits[31:16]: Reserved
Read as 0.

Bits[15:0]:
Timer count value.

4.4 Interrupt Controller Register Description

The SIO contains an ISA compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The interrupt registers control the operation of the interrupt controller and can be accessed from the PCI Bus via PCI I/O space. In addition, some of the registers can be accessed from the ISA Bus via ISA I/O space. The bus access for each register is listed in Table 4.

4.4.1 ICW1—INITIALIZATION COMMAND WORD 1 REGISTER

Register Location:	INT CNTRL-1–020h INT CNTRL-2–0A0h
Default Value:	All bits undefined
Attribute:	Write Only
Size:	8 bits per controller

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence. Addresses 020h and 0A0h are referred to as the base addresses of CNTRL-1 and CNTRL-2, respectively.

An I/O write to the CNTRL-1 or CNTRL-2 base address with bit 4 equal to 1 is interpreted as ICW1. For SIO-based ISA systems, three I/O writes to "base address + 1" must follow the ICW1. The first write to "base address + 1" performs ICW2, the second write performs ICW3, and the third write performs ICW4.

ICW1 starts the initialization sequence during which the following automatically occur:

a. The edge sense circuit is reset. This means that following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt.

b. The Interrupt Mask register is cleared.

c. IRQ7 input is assigned priority 7.

d. The slave mode address is set to 7.

e. Special Mask Mode is cleared and Status Read is set to IRR.

f. If IC4 was set to 0, then all functions selected by ICW4 are set to 0. However, ICW4 must be programmed in the SIO implementation of this interrupt controller, and IC4 must be set to a 1.

ICW1 has three significant functions within the SIO interrupt controller configuration. ICW4 is needed, so bit 0 must be programmed to a 1. There are two interrupt controllers in the system, so bit 1, SNGL, must be programmed to a 0 on both CNTRL-1 and CNTRL-2, to indicate a cascade configuration. LTIM, the interrupt controller IRQ edge/level detection control bit, defines the IRQ sensing mode for each controller. When bit 3 is a 0, each IRQ line on the selected controller is programmed for edge-triggered mode. This mode is signified by a low-to-high transition on an IRQ input line. When bit 3 is a 1, the controller is programmed in level-triggered mode, where a high level on an IRQ input indicates the presence of an interrupt request. LTIM is global for each controller. The incoming IRQs are either all edge-triggered or all level-triggered. Bit D4 must be a 1 when programming ICW1. OCW2 and OCW3 are also addressed at the same port as ICW1. This bit indicates that ICW1, and not OCW2 or OCW3, will be programmed during the write to this port.

Bit 2, ADI, and bits[7:5], A7-A5, are specific to an MSC-85 implementation. These bits are not used by the SIO interrupt controllers. Bits[7:5,2] should each be initialized to 0.

In the 82378ZB, bit 3, the LTIM bit, is not used by the interrupt controller and is always read as a 1.

Bits[7:5]: ICW/OCW Select
A7–A5 are MCS-85 implementation specific bits. They are not needed by the SIO. These bits should be 000 when programming the SIO.

Bit 4: ICW/OCW Select
Bit 4 must be a 1 to select ICW1. After the fixed initialization sequence to ICW1, ICW2, ICW3, and ICW4, the controller base address is used to write to OCW2 and OCW3. Bit 4 is a 0 on writes to these registers. A 1 on this bit at any time will force the interrupt controller to interpret the write as an ICW1. The controller will then expect to see ICW2, ICW3, and ICW4.

Bit 3: LTIM (Edge/Level Bank Select)
Ignored for the SIO.

Bit 2: ADI
Ignored for the SIO.

Bit 1: SNGL (Single or Cascade)
SNGL must be programmed to a 0 to indicate that two interrupt controllers are operating in cascade mode on the SIO.

Bit 0: IC4 (ICW4 Write Required)
This bit must be set to a 1. IC4 indicates that ICW4 needs to be programmed. The SIO requires that ICW4 be programmed to indicate that the controllers are operating in an 80x86 type system.

4.4.2 ICW2—INITIALIZATION COMMAND WORD 2 REGISTER

Address Offset:	INT CNTRL-1–021h INT CNTRL-2–0A1h
Default Value:	All bits undefined
Attribute:	Write Only
Size:	8 bits per controller

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the Host CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 04h for CNTRL-1 and 70h for CNTRL-2.

Bits[7:3]: Interrupt Vector Base Address
Bits[7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input. For CNTRL-1, a typical value is 00001, and for CNTRL-2, 10000.

The interrupt controller combines a binary code representing the interrupt level to receive service with this base address to form the interrupt vector that is driven out onto the bus. For example, the complete interrupt vector for IRQ[0] (CNTRL-1), would be 0000 1000b (CNTRL-1 [7:3] = 00001b and 000b representing IRQ[0]). This vector is used by the CPU to point to the address information that defines the start of the interrupt routine.

Bits[2:0]: Interrupt Request Level
When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt code representing the interrupt level to be serviced. This interrupt code is combined with bits[7:3] to form the complete interrupt vector driven onto the data bus during the second INTA# cycle. Section 5.0, Detailed Function Description, outlines each of these codes. The code is a simple three bit binary code: 000 represents IRQ0 (IRQ8), 001 IRQ1 (IRQ9), 010 IRQ2 (IRQ10), and so on until 111 IRQ7 (IRQ15).

4.4.3 ICW3—INITIALIZATION COMMAND WORD 3 REGISTER

Register Name:	Initialization Command Word 3 (Controller 1-Master Unit)
Address Offset:	INT CNTRL-1–021h
Default Value:	All bits undefined
Attribute:	Write Only
Size:	8 bits

The meaning of ICW3 differs between CNTRL-1 and CNTRL-2. On CNTRL-1, the master controller, ICW3 indicates which CNTRL-1 IRQ line physically connects the INT output of CNTRL-2 to CNTRL-1. ICW3 must be programmed to 04h, indicating the cascade of the CNTRL-2 INT output to the IRQ[2] input of CNTRL-1.

An interrupt request on IRQ2 causes CNTRL-1 to enable CNTRL-2 to present the interrupt vector address during the second interrupt acknowledge cycle.

Bits[7:3]:
These bits must be programmed to zero.

Bit 2: Cascaded Interrupt Controller IRQ Connection
Bit 2 must always be programmed to a 1. This bit indicates that CNTRL-2, the slave controller, is cascaded on interrupt request line two (IRQ[2]). When an interrupt request is asserted to CNTRL-2, the IRQ goes through the priority resolver. After the slave

controller priority resolution is finished, the INT output of CNTRL-2 is asserted. However, this INT assertion does not go directly to the CPU. Instead, the INT assertion cascades into IRQ[2] on CNTRL-1. IRQ[2] must go through the priority resolution process on CNTRL-1. If it wins the priority resolution on CNTRL-1 and the CNTRL-1 INT signal is asserted to the CPU, the returning interrupt acknowledge cycle is really destined for CNTRL-2. The interrupt was originally requested at CNTRL-2, so the interrupt acknowledge is destined for CNTRL-2, and not a response for IRQ[2] on CNTRL-1.

When an interrupt request from IRQ[2] wins the priority arbitration, in reality an interrupt from CNTRL-2 has won the arbitration. Because bit 2 of ICW3 on the master is set to 1, the master knows which identification code to broadcast on the internal cascade lines, alerting the slave controller that it is responsible for driving the interrupt vector during the second INTA# pulse.

Bits[1:0]:
These bits must be programmed to zero.

4.4.4 ICW3—INITIALIZATION COMMAND WORD 3 REGISTER

Register Name:	Initialization Command Word 3 (Controller 2-Slave Unit)
Address Offset:	INT CNTRL-2–0A1h
Default Value:	All bits undefined
Attribute:	Write Only
Size:	8 bits

On CNTRL-2 (the slave controller), ICW3 is the slave identification code broadcast by CNTRL-1 from the trailing edge of the first INTA# pulse to the trailing edge of the second INTA# pulse. CNTRL-2 compares the value programmed in ICW3 with the incoming identification code. The code is broadcast over three SIO internal cascade lines. ICW3 must be programmed to 02h for CNTRL-2. When 010b is broadcast by CNTRL-1 during the INTA# sequence, CNTRL-2 assumes responsibility for broadcasting the interrupt vector during the second interrupt acknowledge cycle.

As an illustration, consider an interrupt request on IRQ[2] of CNTRL-1. By definition, a request on IRQ[2] must have been asserted by CNTRL-2. If IRQ[2] wins the priority resolution on CNTRL-1, the interrupt acknowledge cycle returned by the CPU following the interrupt is destined for CNTRL-2, not CNTRL-1. CNTRL-1 will see the INTA# signal, and knowing that the actual destination is CNTRL-2, will broadcast a slave identification code across the internal cascade lines. CNTRL-2 will compare this incoming value with the 010b stored in ICW3. Following a positive decode of the incoming message from CNTRL-1, CNTRL-2 will drive the appropriate interrupt vector onto the data bus during the second interrupt acknowledge cycle.

Bits[7:3]: Reserved
Must be 0.

Bits[2:0]: Slave Identification Code
The Slave Identification code must be programmed to 010b during the initialization sequence. The code stored in ICW3 is compared to the incoming slave identification code broadcast by the master controller during interrupt acknowledge cycles.

4.4.5 ICW4—INITIALIZATION COMMAND WORD 4 REGISTER

Address Offset:	INT CNTRL-1–021h INT CNTRL-2–0A1h
Default Value:	01h
Attribute:	Write Only
Size:	8 bits

Both SIO interrupt controllers must have ICW4 programmed as part of their initialization sequence. Minimally, the microprocessor mode bit, bit 0, must be set to a 1 to indicate to the controller that it is operating in an 80x86 based system. Failure to program this bit will result in improper controller operation during interrupt acknowledge cycles. Additionally, the Automatic End of Interrupt (AEOI) may be selected, as well as the Special Fully Nested Mode (SFNM) of operation.

The default programming for ICW4 is 01h, which selects 80x86 mode, normal EOI, buffered mode, and special fully nested mode disabled.

Bits 2 and 3 must be programmed to 0 for the SIO interrupt controller to function correctly.

Both bit 1, AEOI, and bit 4, SFNM, can be programmed if the system developer chooses to invoke either mode.

Bits[7:5]: Reserved
Must be 0.

Bit 4: SFNM (Special Fully Nested Mode)
Bit 4, SFNM, should normally be disabled by writing a 0 to this bit. If SFNM = 1, the special fully nested mode is programmed.

Bit 3: BUF (Buffered Mode)
Bit 3, BUF, must be programmed to 0 for the SIO. This is non-buffered mode. As illustrated above under bit functionality, different programming options are offered for bits 2 and 3. However, within the SIO interrupt unit, bits 2 and 3 must always be programmed to 00b.

Bit 2: Master/Slave in Buffered Mode
This bit is not used by the SIO interrupt unit. Bit 2 should always be programmed to 0.

Bit 1: AEOI (Automatic End of Interrupt)
This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.

Bit 0: Microprocessor Mode
The Microprocessor Mode bit must be programmed to 1 to indicate that the interrupt controller is operating in an 80x86-based system. Never program this bit to 0.

4.4.6 OCW1—OPERATIONAL CONTROL WORD 1 REGISTER

Address Offset:	INT CNTRL-1–021h INT CNTRL-2–0A1h
Default Value:	00h
Attribute:	Read/Write
Size:	8 bits

OCW1 sets and clears the mask bits in the Interrupt Mask Register (IMR). Each interrupt request line may be selectively masked or unmasked any time after initialization. A single byte is written to this register. Each bit position in the byte represents the same-numbered channel: bit 0 = IRQ[0], bit 1 = IRQ[1] and so on. Setting the bit to a 1 sets the mask, and clearing the bit to a 0 clears the mask. Note that masking IRQ[2] on CNTRL-1 will also mask all of controller 2's interrupt requests (IRQ8–IRQ15). Reading OCW1 returns the controller's mask register status.

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

Unlike status reads of the ISR and IRR, for reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever I/O read is active and the I/O port address is 021h or 0A1h (OCW1).

All writes to OCW1 must occur following the ICW1–ICW4 initialization sequence, since the same I/O ports are used for OCW1, ICW2, ICW3 and ICW4.

Bits[7:0]: Interrupt Request Mask (Mask [7:0])
When a 1 is written to any bit in this register, the corresponding IRQ[x] line is masked. For example, if bit 4 is set to a 1, then IRQ[4] will be masked. Interrupt requests on IRQ[4] will not set channel 4's interrupt request register (IRR) bit as long is the channel is masked.

When a 0 is written to any bit in this register, the corresponding IRQ[x] mask bit is cleared, and interrupt requests will again be accepted by the controller.

NOTE:
Masking IRQ[2] on CNTRL-1 will also mask the interrupt requests from CNTRL-2, which is physically cascaded to IRQ[2].

4.4.7 OCW2—OPERATIONAL CONTROL WORD 2 REGISTER

Address Offset: INT CNTRL-1-020h
INT CNTRL-2-0A0h
Default Value: Bit[4:0] = undefined,
Bit[7:5] = 001
Attribute: Write Only
Size: 8 bits

OCW2 controls both the Rotate Mode and the End of Interrupt Mode, and combinations of the two. The three high order bits in an OCW2 write represent the encoded command. The three low order bits are used to select individual interrupt channels during three of the seven commands. The three low order bits (labeled L2, L1 and L0) are used when bit 6 is set to a 1 during the command.

Following a PCIRST# and ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bits[7:5]: Rotate and EOI Codes
R, SL, EOI-These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition.

Bits 7	6	5	Function
0	0	1	Non-Specific EOI Command
0	1	1	Specific EOI Command
1	0	1	Rotate on Non-Specific EOI Command
1	0	0	Rotate in Auto EOI Mode (Set)
0	0	0	Rotate in Auto EOI Mode (Clear)
1	1	1	*Rotate on Specific EOI Command
1	1	0	*Set Priority Command
0	1	0	No Operation

NOTE:
* L0-L2 Are Used

Bits[4:3]: OCW2 Select
When selecting OCW2, bits 3 and 4 must both be 0. If bit 4 is a 1, the interrupt controller interprets the write to this port as an ICW1. Therefore, always ensure that these bits are both 0 when writing an OCW2.

Bits[2:0]: Interrupt Level Select (L2, L1, L0)
L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case.

Bit 2	1	0	Interrupt Level
0	0	0	IRQ 0(8)
0	0	1	IRQ 1(9)
0	1	0	IRQ 2(10)
0	1	1	IRQ 3(11)
1	0	0	IRQ 4(12)
1	0	1	IRQ 5(13)
1	1	0	IRQ 6(14)
1	1	1	IRQ 7(15)

4.4.8 OCW3—OPERATIONAL CONTROL WORD 3 REGISTER

Address Offset: INT CNTRL-1-020h
INT CNTRL-2-0A0h
Default Value: Bit[6,0] = 0,
Bit[7,4:2] = undefined,
Bit[5,1] = 1
Attribute: Read/Write
Size: 8 bits

OCW3 serves three important functions: Enable Special Mask Mode, Poll Mode control, and IRR/ISR register read control.

First, OCW3 is used to set or reset the Special Mask Mode (SMM). The Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/disabling of the other channel's mask bits.

Second, the Poll Mode is enabled when a write to OCW3 is issued with bit 2 equal to 1. The next I/O read to the interrupt controller is treated like an interrupt acknowledge; a binary code representing the highest priority level interrupt request is released onto the bus.

Third, OCW3 provides control for reading the In-Service Register (ISR) and the Interrupt Request Register (IRR). Either the ISR or IRR is selected for reading with a write to OCW3. Bits 0 and 1 carry the encoded command to select either register. The next I/O read to the OCW3 port address will return the register status specified during the previous write. The register specified for a status read is retained by the interrupt controller. Therefore, a write to OCW3 prior to every status read command is unnecessary, provided the status read desired is from the register selected with the last OCW3 write.

Bit 7: Reserved
Must be 0.

Bit 6: SMM (Special Mask Mode)
If ESMM = 1 and SMM = 1 the interrupt controller enters Special Mask Mode. If ESMM = 1 and SMM = 0, the interrupt controller is in normal mask mode. When ESMM = 0, SMM has no effect.

Bit 5: ESMM (Enable Special Mask Mode)
When ESMM = 1, the SMM bit is enabled to set or reset the Special Mask Mode. When ESMM = 0, the SMM bit becomes a "don't care".

Bits[4:3]: OCW3 Select
When selecting OCW3, bit 3 must be a 1 and bit 4 must be 0. If bit 4 = 1, the interrupt controller interprets the write to this port as an ICW1. Therefore, always ensure that bits[4:3] = 01 when writing an OCW3.

Bit 2: Poll Mode Command
When bit 2 = 0, the Poll command is not issued. When bit 2 = 1, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.

Bits[1:0]: Register Read Command
Bits[1:0] provide control for reading the In-Service Register (ISR) and the Interrupt Request Register (IRR). When bit 1 = 0, bit 0 will not affect the register read selection. When bit 1 = 1, bit 0 selects the register status returned following an OCW3 read. If bit 0 = 0, the IRR will be read. If bit 0 = 1, the ISR will be read. Following ICW initialization, the default OCW3 port address read will be "read IRR". To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read.

Bit	1	0	Function
	0	0	No Action
	0	1	No Action
	1	0	Read IRQ Register
	1	1	Read IS Register

4.5 Control Registers

This section contains NMI registers, a real-time clock register, Port 92 Register, and the Digital Output Register.

4.5.1 NMISC—NMI STATUS AND CONTROL REGISTER

Address Offset: 061h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

This register is used to check the status of different system components, control the output of the speaker counter (Counter 2), and gate the counter output that drives the SPKR signal.

Bits 4, 5, 6, and 7 are read-only. When writing to this port, these bits must be written as 0's. Bit 6 returns the IOCHK# NMI status. This input signal comes from the ISA Bus. It is used for parity errors on memory cards plugged into the bus, and for other high priority interrupts. The current status of bit 3 enables or disables this NMI source. Bit 5 is the current state of the OUT pin of interval Timer 1, Counter 2. Bit 4 toggles from 1-0 or from 0-1 after every Refresh cycle. Following PCIRST#, bits 4 and 6 are both 0. Bit 5 is undetermined until Counter 2 is properly programmed. Bit 7 returns the PCI System Error status (SERR#). If 0, bit 7 indicates that SERR# was not pulsed active by a PCI agent. If 1, bit 7 indicates that SERR# was pulsed active by a PCI agent and that an NMI will be issued to the Host CPU. This NMI can be disabled with bit 2 of this register.

Bits 0–3 are both read and write. Bit 0 is the GATE input signal for Timer 1, Counter 2. The GATE input is used to disable counting in Counter 2. The Counter 2 output is ANDed with bit 1 to form the SPKR output signal. Bit 1 gates the Counter 2 OUT value. When bit 1 is disabled, the SPKR signal is disabled; when bit 1 is enabled, the SPKR output follows the value at the OUT pin of Counter 2. The Counter 2 OUT pin status can be checked by reading port 061h and checking bit 5. Bit 2 is used to enable the System Error (SERR#) signal. Bit 3 enables or disables the incoming IOCHK# NMI signal from the expansion bus. Each of these bits is reset to 0 following PCIRST#.

Bit 7: SERR# Status
Bit 7 is set if a system board agent (PCI devices or main memory) detects a system board error and pulses the PCI SERR# line. This interrupt is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 0 and then set it to 1. This bit is read-only. When writing to port 061h, bit 6 must be a 0.

Bit 6: IOCHK# NMI Source Status
Bit 6 is set if an expansion board asserts IOCHK# on the ISA/SIO bus. This interrupt is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 0 and then set it to 1. This bit is read-only. When writing to port 061h, bit 6 must be a 0.

Bit 5: Timer Counter 2 OUT Status
The Counter 2 OUT signal state is reflected in bit 5. The value on this bit following a read is the current state of the Counter 2 OUT signal. Counter 2 must be programmed following a PCIRST# for this bit to have a determinate value. Bit 5 is read-only. When writing to port 061h, bit 5 must be a 0.

Bit 4: Refresh Cycle Toggle
The Refresh Cycle Toggle signal toggles from either 0 to 1 or 1 to 0 following every refresh cycle. This read-only bit is a 0 following PCIRST#. When writing to port 061h, bit 4 must be a 0.

Bit 3: IOCHK# NMI Enable
When bit 3 = 1, IOCHK# NMI's are disabled and cleared. When bit 3 = 0, IOCHK# NMI's are enabled. Following PCIRST#, bit 3 is reset to 0.

Bit 2: PCI SERR# Enable
When bit 2 = 1, the PCI System Error (SERR#) is disabled and cleared. When bit 2 = 0, SERR# is enabled. Following PCIRST#, bit 2 is a 0.

Bit 1: Speaker Data Enable
Speaker Data Enable is ANDed with the Counter 2 OUT signal to drive the SPKR output signal. When bit 1 = 0, the result of the AND is always 0 and the SPKR output is always 0. When bit 1 = 1, the SPKR output is equivalent to the Counter 2 OUT signal value. Following PCIRST#, bit 1 is a 0.

Bit 0: Timer Counter 2 Enable
When bit 0 = 0, Counter 2 counting is disabled. Counting is enabled when bit 0 = 1. This bit controls the GATE input to Counter 2. Following PCIRST#, the value of this bit is 0.

4.5.2 NMI ENABLE AND REAL-TIME CLOCK ADDRESS REGISTER

Address Offset: 070h
Default Value: Bit[6:0] = undefined, Bit 7 = 1
Attribute: Write Only
Size: 8 bits

The Mask register for the NMI interrupt is at I/O address 070h shown below. The most significant bit enables or disables all NMI sources including IOCHK# and the NMI Port. Write an 80h to port 70h to mask the NMI signal. This port is shared with the real-time clock. The real-time-clock uses the lower six bits of this port to address memory locations. Writing to port 70h sets both the enable/disable bit and the memory address pointer. Do not modify the contents of this register without considering the effects on the state of the other bits. Reads and writes to this register address flow through to the ISA Bus.

Bit 7: NMI Enable
Setting bit 7 to a 1 disables all NMI sources. Setting the bit to a 0 enables the NMI interrupt. Following PCIRST#, this bit is a 1.

Bits[6:0]: Real Time Clock Address
Used by the Real Time Clock on the Base I/O component to address memory locations. Not used for NMI enabling/disabling.

4.5.3 PORT 92 REGISTER

Address Offset: 92h
Default Value: 24h
Attribute: Read/Write
Size: 8 bits

This register is used to support the alternate reset (ALT__RST#) and alternate A20 (ALT__A20) functions. This register is only accessible if bit 6 in the Utility Bus Chip Select B Register is set to a 1. Reads and writes to this register location flow through to the ISA Bus.

Bits[7:6]: Reserved
Returns 00 when read.

Bit 5: Reserved
Returns a 1 when read.

Bit 4: Reserved
Returns a 0 when read.

Bit 3: Reserved
Returns a 0 when read.

Bit 2: Reserved
Returns a 1 when read.

Bit 1: ALT__A20 Signal Control
Writing a 0 to this bit causes the ALT__A20 signal to be driven low. Writing a 1 to this bit causes the ALT__A20 signal to be driven high.

Bit 0: Alternate System Reset
This read/write bit provides an alternate system reset function. This function provides an alternate means to reset the system CPU to effect a mode switch from Protected Virtual Address Mode to the Real Address Mode. This provides a faster means of reset than is provided by the Keyboard controller. This bit is set to a 0 by a system reset. Writing a 1 to this bit will cause the ALT__RST# signal to pulse active (low) for approximately 4 SYSCLK's. Before another ALT__RST# pulse can be generated, this bit must be written back to a 0.

4.5.4 DIGITAL OUTPUT REGISTER

Address Offset: 03F2h (Primary), 0372h (Secondary)
Default Value: Bit[7:4,2:0] = undefined, Bit 3 = 0
Attribute: Write only
Size: 8 bits

This register is used to prevent UBUSOE# from responding to DACK2# during a DMA read access to a floppy controller on the ISA Bus. If a second floppy (residing on the ISA Bus) is using DACK2# in conjunction with a floppy on the utility bus, this prevents the floppy on the utility bus and the utility bus transceiver from responding to an access targeted for the floppy on the ISA Bus. This register is also located in the floppy controller device. Reads and writes to this register location flow through to the ISA Bus.

Bits[7:4]: Not Used
These bits exist in the floppy controller.

Bit 3: DMA Enable
When this bit is a 1, the assertion of DACK# will result in UBUSOE# being asserted. If this bit is 0, DACK2# has no effect on UBUSOE#. This port bit also exists on the floppy controller. This bit defaults to disable (0).

Bits[2:0]: Not Used
These bits exist in the floppy controller.

4.5.5 RESET UBUS IRQ12 REGISTER

Address Offset: 60h
Default Value: N/A
Attribute: Read only
Size: 8 bits

This address location (60h) is used to clear the mouse interrupt function to the CPU. Reads to this address are monitored by the SIO. When the mouse interrupt function is enabled (bit 4 of the ISA Clock Divisor Register is 1), the mouse interrupt function is provided on the IRQ12/M input signal. In this mode, a mouse interrupt generates an interrupt through IRQ13 to the Host CPU. A read of 60h releases IRQ12. If bit 4 = 0 in the ISA Clock Divisor Register, a read of address 60h has no effect on IRQ12/M. Reads and writes to this register flow through to the ISA Bus. For additional information, see the IRQ12/M description in Section 3.0, Signal Description.

Bits[7:0]: Reset IRQ12
No specific pattern. A read of address 60h executes the command.

4.5.6 COPROCESSOR ERROR REGISTER

Address Offset: F0h
Default Value: N/A
Attribute: Write only
Size: 8 bits

This address location (F0h) is used when the SIO is programmed for coprocessor error reporting (bit 5 of the ISA Clock Divisor Register is 1). Writes to this address are monitored by the SIO. In this mode, the SIO generates an interrupt (INT) to the CPU when it receives an error signal (FERR# asserted) from the CPU's coprocessor. Writing address F0h, when FERR# is asserted, causes the SIO to assert IGNNE# and negate IRQ13. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted, writing to address F0h does not effect IGNNE#. Reads and writes to this register flow through to the ISA Bus. For additional information, see the IGNNE# description in Section 3.0, Signal Description.

Bits[7:0]: Reset IRQ12
No specific pattern. A write to address F0h executes the command.

4.5.7 ELCR—EDGE/LEVEL CONTROL REGISTER

Address Offset: INT CNTRL-1–04D0h
INT CNTRL-2–04D1h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The Edge/Level Control Register is used to set the interrupts to be triggered by either the signal edge or the logic level. INT0, INT1, INT2, INT8, INT13 must be set to edge sensitive. After a reset, all the INT signals are set to edge sensitive. Figure 4 shows which bit numbers represent the various INT signals.

Each IRQ to which a PCI interrupt is steered into (see the PIRQ Route Control Register) must have its interrupt set to level sensitive.

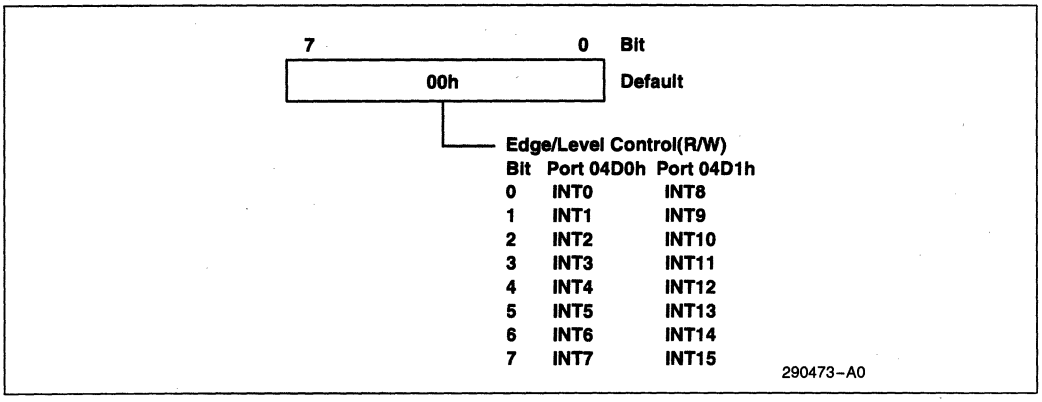


Figure 4. Edge/Level Select Register

Register Location: 04D0h-INT CNTRL-1
04D1h-INT CNTRL-2

04D0h-INT CNTRL-1 Register

Bit[7:0]: Edge/Level Select
These bits select if the interrupts are triggered by either the signal edge or the logic level. A 0 bit represents an edge sensitive interrupt, and a 1 is for level sensitive. The following bits MUST be set to 0:

Port 04D0h (INT-CNTRL-1)

0-INT0	0	Reserved. Read as zero.
1-INT1	0	Reserved. Read as zero.
2-INT2	0	Reserved. Read as zero.
3-INT3	x	
4-INT4	x	
5-INT5	x	
6-INT6	x	
7-INT7	x	

x = selectable to either a 0 or a 1,
0 = edge sensitive, 1 = level sensitive

After reset, this register is set to 00h.

04D1h-INT CNTRL-2 Register

Bit[7:0]: Edge/Level Select
These bits select if the interrupts are triggered by either the signal edge or the logic level. A 0 bit represents an edge sensitive interrupt, and a 1 is for level sensitive. The following bits MUST be set to 0:

Port 04D1h (INT-CNTRL-2)

0-INT8	0	Reserved. Read as zero.
1-INT9	x	
2-INT10	x	
3-INT11	x	
4-INT12	x	
5-INT13	0	Reserved. Read as zero.
6-INT14	x	
7-INT15	x	

x = selectable to either a 0 or a 1,
0 = edge sensitive, 1 = level sensitive

After reset, this register is set to 00h.

4.6. Power Management Registers

This section contains the Power Management Registers located in non-configuration space.

4.6.1 APMC—ADVANCED POWER MANAGEMENT CONTROL PORT

Address Offset: 0B2h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

Bits[7:0]: APMC[7:0]
APM Control Port. Readable/writeable at system I/O address 0B2h. Used to pass an APM command between the OS and the SMI handler. Writes to this port not only store data in the APMC register, but also generate an SMI when the SAPMCEN bit is set. Reads to this port will not generate an SMI. If CSTPCLKEN is set, a read from the APMC will cause STPCLK# to be asserted.

4.6.2 APMS—ADVANCED POWER MANAGEMENT STATUS PORT

Address Offset: 0B3h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

Bits[7:0]: APMS[7:0]
Readable/writeable at system address 0B3h. Used to pass data between the OS and the SMI handler.

5.0 DETAILED FUNCTIONAL DESCRIPTION

5.1 PCI Interface

5.1.1 PCI COMMAND SET

Bus commands indicate to the slave the type of transaction the master is requesting. Bus Commands are encoded on the C/BE[3:0]# lines during the address phase of a PCI cycle.

5.1.2 PCI BUS TRANSFER BASICS

Details of PCI Bus operations can be found in the *Peripheral Component Interconnect (PCI) Specification*. Only details of the PCI Bus unique to the SIO are included in this data sheet.

Table 7. PCI Commands

C/BE[3:0]#	Command Type As Slave	Supported As Slave	Supported As Master
0000	Interrupt Acknowledge	Yes	No
0001	Special Cycle(4)	No/Yes	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	Reserved(3)	No	No
0101	Reserved(3)	No	No
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved(3)	No	No
1001	Reserved(3)	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No(2)	No
1101	Reserved(3)	No	No
1110	Memory Read Line	No(2)	No
1111	Memory Write and Invalidate	No(1)	No

NOTES:
1. Treated as Memory Write.
2. Treated as Memory Read.
3. Reserved Cycles are considered invalid by the SIO and are to be competely ignored. All internal address decoding is ignored and DEVSEL# is never to be asserted.
4. The 82378 responds to a Stop Grant Special Cycle.

5.1.2.1 PCI Addressing

PCI address decoding uses the AD[31:0] signals. AD[31:2] are always used for address decoding while the information contained in the two low order bits AD[1:0] varies for memory, I/O, and configuration cycles.

For I/O cycles, AD[31:0] are decoded to provide a byte address. AD[1:0] are used for generation of DEVSEL# only and indicate the least significant valid byte involved in the transfer. For example, if only BE0# is asserted, AD[1:0] are 00. If only BE3# is asserted, then AD[1:0] are 11. If BE3# and BE2# are asserted, AD[1:0] are 10. If all BEx#'s are asserted, then AD[1:0] are 00. The byte enables determine which byte lanes contain valid data. The SIO requires that PCI accesses to byte-wide internal registers must assert only one byte enable.

When the SIO is the target of any PCI transaction in which BE[3:0]# = 1111, the SIO terminates the cycle normally by asserting TRDY#. No data is written into the SIO during write cycles and the data driven by the SIO during read cycles is indeterminate.

For memory cycles, accesses are decoded as Dword accesses. This means that AD[1:0] are ignored for decoding memory cycles. The byte enables determine which byte lanes contain valid data. When the SIO is a PCI master, it drives 00 on AD[1:0] for all memory cycles.

For configuration cycles, DEVSEL# is a function of IDSEL and AD[1:0]. DEVSEL# is selected during a configuration cycle only if IDSEL is active and both AD[1:0] = 00. The cycle is ignored by the SIO if either AD1 or AD0 is non-zero. Configuration registers are selected as Dwords using AD[7:2]. The byte enables determine which byte lanes contain valid data.

5.1.2.2 DEVSEL# Generation

As a PCI slave, the SIO asserts the DEVSEL# signal to indicate it is the slave of the PCI transaction. DEVSEL# is asserted when the SIO positively or subtractively decodes the PCI transaction. The SIO asserts DEVSEL# (claim the transaction) before it issues any other slave response, i.e., TRDY#, STOP#, etc. After the SIO asserts DEVSEL#, it does not negate DEVSEL# until the same edge that the master uses to negate the final IRDY#.

It is expected that most (perhaps all) PCI target devices will be able to complete a decode and assert DEVSEL# within 1 or 2 clocks of FRAME#. Since the SIO subtractively decodes all unclaimed PCI cycles (except configuration cycles), it provides a configuration option to pull in (by 1 or 2 clocks) the edge when the SIO samples DEVSEL#. This allows faster access to the expansion bus. Use of such an option is limited by the slowest positive decode agent on the bus. This is described in more detail in Section 5.5.1.4, Subtractively Decoded Cycles to ISA.

As a PCI master, the SIO waits for 5 PCICLKs after the assertion of FRAME# for a slave to assert DEVSEL#. If the SIO does not receive DEVSEL# in this time, it will master-abort the cycle. See Section 5.1.3.1, SIO as MasterMaster-Initiated Termination, for further details.

5.1.2.3 Basic PCI Read Cycles (I/O and Memory)

As a PCI master, the SIO only performs memory read transfers (i.e. I/O read transfers are not supported). When reading data from PCI memory, the SIO requests a maximum of 8 bytes via a two data phase burst read cycle to fill its internal 8 byte line buffer. If the line buffer is programmed for single transaction mode, fewer bytes are requested (refer to Section 5.6.1, DMA/ISA Master Line Buffer). Read cycles from PCI memory are generated on behalf of ISA masters and DMA devices.

As a PCI slave, the SIO responds to both I/O read and memory read transfers. For multiple read transactions, the SIO always target-terminates after the first data read transaction by asserting STOP# and TRDY# at the end of the first data phase. For single read transactions, the SIO finishes the cycle in a normal fashion, by asserting TRDY# without asserting STOP#.

5.1.2.4 Basic PCI Write Cycles (I/O and Memory)

As a PCI master, the SIO generates a PCI memory write cycle when it decodes an ISA-originated/PCI-bound memory write cycle. I/O write cycles are never initiated by the SIO. When writing data to PCI memory, the SIO writes a maximum of 4 bytes via a single data transaction write cycle. If the SIO's internal ISA master/DMA line buffer is programmed for single transaction mode, fewer bytes will be generated (refer to Section 5.6.1, DMA/ISA Master Line Buffer). In either case, only one data transaction will be performed. Cycles to PCI memory are generated on behalf of ISA masters, DMA devices, and the SIO when the SIO needs to flush the ISA master/DMA line buffer.

As a PCI master, the SIO drives the AD0 and AD1 signals low during the address phase of the cycle. This is done to indicate to the slave that the address will increment during the transfer. If there is no response on the PCI Bus, the SIO will master-abort due to the DEVSEL# time out.

As a PCI slave, the SIO will respond to both I/O write and memory write transfers. For multiple write transactions, the SIO will always target-terminate after the first data write transaction by asserting STOP# and TRDY# at the end of the first data phase. For single write transactions, the SIO will finish the cycle normally by asserting TRDY# without asserting STOP#.

5.1.2.5 Configuration Cycles

The configuration read or write command defined by the bus control signals C/BE[3:0]# is used to configure the SIO. During the address phase of the configuration read or write command, the SIO will sample its IDSEL (ID select). If IDSEL is active and AD[1:0] are both zero, the SIO generates DEVSEL#. Otherwise, the cycle is ignored by the SIO. During the configuration cycle address phase, bits AD[7:2] and C/BE[3:0]# are used to select particular bytes within a configuration register. Note that IDSEL is normally a "don't care" except during the address phase of a transaction.

NOTE:
An unclaimed configuration cycle is never forwarded to the ISA Bus.

5.1.2.6 Interrupt Acknowledge Cycle

The interrupt acknowledge command is a single byte read implicitly addressed to the SIO's interrupt controller. The address bits are logical "don't cares" during the address phase and the byte enables will indicate to the SIO an 8-bit interrupt vector is to be returned on AD[7:0]. The SIO converts this single cycle transfer into two cycles that the internal 8259 pair can respond to (see Section 5.8, Interrupt Controller). The SIO will hold the PCI Bus in wait states until the 8 bit interrupt vector is returned.

SIO responses to an interrupt acknowledge cycle can be disabled by setting bit 5 in the PCI Control Register to a 0. However, if disabled, the SIO will still respond to accesses to the interrupt register set and allow poll mode functions.

5.1.2.7 Exclusive Access

The SIO marks itself locked anytime it is the slave of the access and LOCK# is sampled negated during the address phase. As a locked slave, the SIO responds to a master only when it samples LOCK# negated and FRAME# asserted. The locking master may negate LOCK# at the end of the last data phase. The SIO unlocks itself when FRAME# and LOCK# are both negated. The SIO will respond by asserting STOP# with TRDY# negated (retry) to all transactions when LOCK# is asserted during the address phase.

Locked cycles are never generated by the SIO.

5.1.2.8 PCI Special Cycle

When the SCE bit (bit 3) in the COM PCI configuration register (configuration offset 04h) is set to a "0", the SIO will ignore all PCI Special Cycles. When the SCE bit is set to a "1", the SIO will recognize PCI Special Cycles.

The only PCI Special Cycle currently recognized is the Stop Grant Special Cycle which is broadcast onto the PCI bus when an S-series processor enters the Stop Grant State. The SCE bit must be set to a "1" when the Stop Clock feature is being used.

5.1.3 TRANSACTION TERMINATION

The SIO supports both Master-initiated Termination as well as Target-initiated Termination.

5.1.3.1 SIO As Master—Master-Initiated Termination

The SIO supports two forms of master-initiated termination:

1. Normal termination of a completed transaction.
2. Abnormal termination due to no slave responding to the transaction (Abort).

Figure 5 shows the SIO performing master-abort termination. This occurs when no slave responds to the SIO's master transaction by asserting DEVSEL# within 5 PCICLK's after FRAME# assertion. This master-abort condition is abnormal and it indicates an error condition. The SIO will not retry the cycle. The Received Master-abort Status bit in the PCI Status Register will be set indicating that the SIO experienced a master-abort condition.

If an ISA master or the DMA is waiting for the PCI cycle to terminate (CHRDY negated), the master-abort condition will cause the SIO to assert CHRDY to terminate the ISA cycle. Note that write data will be lost and the read data will be all 1's at the end of the cycle. This is identical to the way an unclaimed cycle is handled on the "normally ready" ISA Bus. If the line buffer is the requester of the PCI transaction, the master-abort mechanism will end the PCI cycle, but no data will be transferred into or out of the line buffer. The line buffer will not be allowed to retry the cycle.

5.1.3.2 SIO As A Master—Response To Target-Initiated Termination

SIO's response as a master to target-termination:

1. For a target-abort, the SIO will not retry the cycle. If an ISA master or the DMA is waiting for the PCI cycle to complete (CHRDY negated), the target-abort condition will cause the SIO to assert CHRDY and end the cycle on the ISA Bus. If the ISA master or DMA device was reading from PCI memory, the SIO will drive all 1's on the data lines of the ISA Bus. The Received Target-abort Status bit in the PCI Status Register will be set indicating that the SIO experienced a target-abort condition.
2. If the SIO is retried as a master on the PCI Bus, it will remove it's request for 2 PCI clocks before asserting it again to retry the cycle.
3. If the SIO is disconnected as a master on the PCI Bus, it will respond very much as if it had been retried. The difference between retry and disconnect is that the SIO did not see any data phase for the retry. Disconnect may be generated by a PCI slave when the SIO is running a burst memory read cycle to fill it's 8-byte Line Buffer. In this case, the SIO may need to finish a multi-data phase transfer, and thus, must recycle through arbitration as required for a retry. An example of this is when the on-board DMA requests an 8-byte Line Buffer transfer and the SIO is disconnected before the Line Buffer is completely filled.

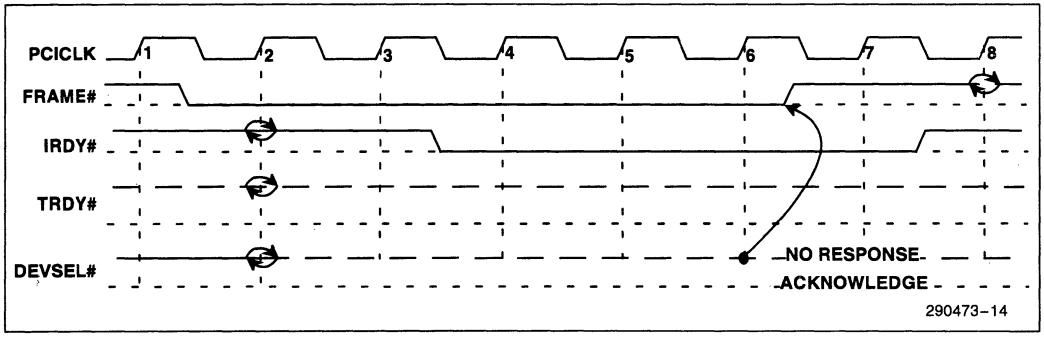


Figure 5. Master—Initiated Termination (Master-Abort)

5.1.3.3 SIO As A Target—Target-Initiated Termination

The SIO supports three forms of Target-initiated Termination:

Disconnect	Disconnect refers to termination requested because the SIO is unable to respond within the latency guidelines of the PCI specification. Note that this is not usually done on the first data phase.
Retry	Retry refers to termination requested because the target is currently in a state which makes it unable to process the transaction.
Abort	Abort refers to termination requested because the target will never be able to respond to the transaction.

The SIO will initiate Disconnect for PCI-originated/ISA-bound cycles after the first data phase due to incremental latency requirements. Since the SIO has only one Posted Write Buffer and every PCI to ISA incremental data phase will take longer than the specified 8 clocks, the SIO will always terminate burst cycles with a disconnect protocol. An example of this is when the SIO receives a burst memory write. Since the SIO only has one Posted Write Buffer, the transaction will automatically be disconnected after the first data phase.

The SIO will retry PCI masters:

1. For memory write cycles when the posted write buffer is full.
2. When the pending PCI cycle initiates some type of buffer management activity.
3. When the SIO is locked as a resource and a PCI master tries to access the SIO without negating the LOCK# signal in the address phase.
4. When the ISA Bus is occupied by an ISA master or DMA.

Target-abort is issued by the SIO when the internal SIO registers are the target of a PCI master I/O cycle and more than one byte enable is active. Accesses to the BIOS Timer Register and the Scatter/Gather Descriptor Table Pointer Registers are exceptions to this rule. Accesses to the Scatter/Gather Descriptor Table Pointer Register must be 32-bits wide and accesses to the BIOS Timer Register must be 16- or 32-bits wide. These accesses will not result in a SIO target-abort. The SIO responds with a target-abort since the registers must be accessed as 8-bit quantities. Target-abort resembles a retry, although the SIO also negates DEVSEL# along with the assertion of STOP#. Bit 11 in the Device Status Register is set to a 1 when the SIO target-aborts.

5.1.4 BUS LATENCY TIME-OUT

5.1.4.1 Master Latency Timer

Because the SIO only bursts a maximum of two Dwords, the PCI master latency timer is not implemented.

5.1.4.2 Target Incremental Latency Mechanism

As a slave, the SIO supports the Incremental Latency Mechanism for PCI to ISA cycles. The PCI specification states that for multi-data phase PCI cycles, if the incremental latency from current data phase (N) to the next data phase (N+1) is greater than 8 PCICLK's, then the slave must manipulate TRDY# and STOP# to stop the transaction upon completion of the current data phase (N). Since all PCI-originated (SIO is a slave)/ISA-bound cycles will require greater than the stated 8 PCICLK's, the SIO will automatically terminate these cycles after the first data phase. Note that latency to the first data phase is not restricted by this mechanism.

5.1.5 PARITY SUPPORT

As a master, the SIO generates address parity for read and write cycles, and data parity for write cycles. As a slave, the SIO generates data parity for read cycles. The SIO does not check parity and does not generate SERR#.

PAR is the calculated parity signal. PAR is "even" parity and is calculated on 36 bits; the 32 AD[31:0] signals plus the 4 C/BE[3:0]# signals. "Even" parity means that the number of 1's within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits, regardless of the valid byte enables. PAR is only guaranteed to be valid one PCI clock after the corresponding address or data phase.

5.1.6 RESET SUPPORT

The PCIRST# pin acts as the SIO hardware reset pin.

During Reset

AD[31:0], C/BE[3:0]#, and PAR are always driven low by the SIO from the leading edge of PCIRST#. FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, MEMREQ#, FLSHREQ#, CPUGNT#, GNT0#/ SIOREQ#, and GNT1#/ RESUME# are tri-stated from the leading edge of PCIRST#.

GNT2# and GNT3# are tri-stated from the leading edge of PCIRST#.

After Reset

AD[31:0], C/BE[3:0]#, and PAR are always tri-stated from the trailing edge of PCIRST#. If the internal arbiter is enabled (CPUREQ# sampled high on the trailing edge of PCIRST#), the SIO will drive these signals low again (synchronously 2-5 PCICLKs later) until the bus is given to another master. If the internal arbiter is disabled (CPUREQ# sampled low on the trailing edge of PCIRST#), these signals remain tri-stated until the SIO is required to drive them valid as a master or slave.

FRAME#, IRDY#, TRDY#, STOP#, and DEVSEL# remain tri-stated until driven by the SIO as either a master or a slave. MEMREQ#, FLSHREQ#, CPUGNT#, GNT0#/SIOREQ#, and GNT1#/RESUME# are tri-stated until driven by the SIO.

GNT2# and GNT3# are tri-stated until driven by the SIO.

After PCIRST, MEMREQ# and FLSHREQ# are driven inactive asynchronously from PCIRST# inactive. CPUGNT#, GNT0#/SIOREQ#, and GNT1#/ RESUME# are driven based on the arbitration scheme and the asserted REQx#'s.

GNT2# and GNT3# are also driven based on the arbitration scheme and the asserted REQx#'s.

5.1.7 DATA STEERING

Data steering logic internal to the SIO provides the assembly/disassembly, copy up/copy down mechanism for cycles between the 32-bit PCI data bus and the 16-bit ISA Bus. The steering logic ensures that the correct bytes are steered to the correct byte lane and that multiple cycles are run where applicable.

5.2 PCI Arbitration Controller

The 82378 contains a PCI Bus arbiter that supports six PCI masters; the Host Bridge, SIO, and four other masters. The SIO's REQ#/GNT# lines are internal. The integrated arbiter can be disabled by asserting CPUREQ# during PCIRST# (see Section 5.2.7, Power-up Configuration). When disabled, the SIO's REQ#, GNT#, and RESUME# signals become visible for an external arbiter. The internal arbiter is enabled upon power-up.

The internal arbiter contains several features that contribute to system efficiency:

- Use of a RESUME# signal to re-enable a backed-off initiator in order to minimize PCI Bus thrashing when the SIO generates a retry (Section 5.2.4.1).
- A programmable timer to re-enable retried initiators after a programmable number of PCICLK's (Section 5.2.4.2).
- The CPU (host bridge) can be optionally parked on the PCI Bus (Section 5.2.5).
- A programmable PCI Bus lock or PCI resource lock function (Section 5.2.6).

The PCI arbiter is also responsible for control of the Guaranteed Access Time (GAT) mode signals (Section 5.2.3.2).

5.2.1 ARBITRATION SIGNAL PROTOCOL

The internal arbiter follows the PCI arbitration method as outlined in the *Peripheral Component Interconnect (PCI) Specification*. The SIO's arbiter is discussed in this section.

5.2.1.1 Back-To-Back Transactions

The SIO as a master does not generate fast back-to-back accesses since it does not know if it is accessing the same target.

The SIO as a target supports fast back-to-back transactions. Note that for back-to-back cycles, the SIO treats positively decoded accesses and subtractively decoded accesses as different targets. Therefore, masters can only run fast back-to-back cycles to positively decoded addresses or to subtractively decoded addresses. Fast back-to-back cycles must not mix positive and subtractive decoded addresses. See the address decoding section to determine what addresses the SIO positively decodes and subtractively decodes.

5.2.2 PRIORITY SCHEME

The PCI arbitration priority scheme is programmable through the PCI Arbiter Priority Control and Arbiter Priority Control Extension Register. The arbiter consists of four banks that can be configured for the six masters to be arranged in a purely rotating priority scheme, one of twenty-four fixed priority schemes, or a hybrid combination (Figure 6).

Note that SIOREQ#/SIOGNT# are SIO internal signals.

The PCI Arbiter Priority Control (PAPC) and PCI Arbiter Priority Control Extension Register bits are shown below:

PCI Arbiter Priority Control Register Bits (PAPC)

Bit	Description
7	Bank 3 Rotate Control
6	Bank 2 Rotate Control
5	Bank 1 Rotate Control
4	Bank 0 Rotate Control
3	Bank 2 Fixed Priority Mode select B
2	Bank 2 Fixed Priority Mode select A
1	Bank 1 Fixed Priority Mode select
0	Bank 0 Fixed Priority Mode select

PCI Arbiter Priority Control Extension Register Bits (ARBPRIX)

Bit	Description
7:1	Reserved. Read as 0
0	Bank 3 Fixed Priority Mode select

PAPC defaults to 04h and ARBPRIX to 00h at reset selecting fixed mode #10 (Table 8) with the CPU the highest priority device guaranteeing access to BIOS.

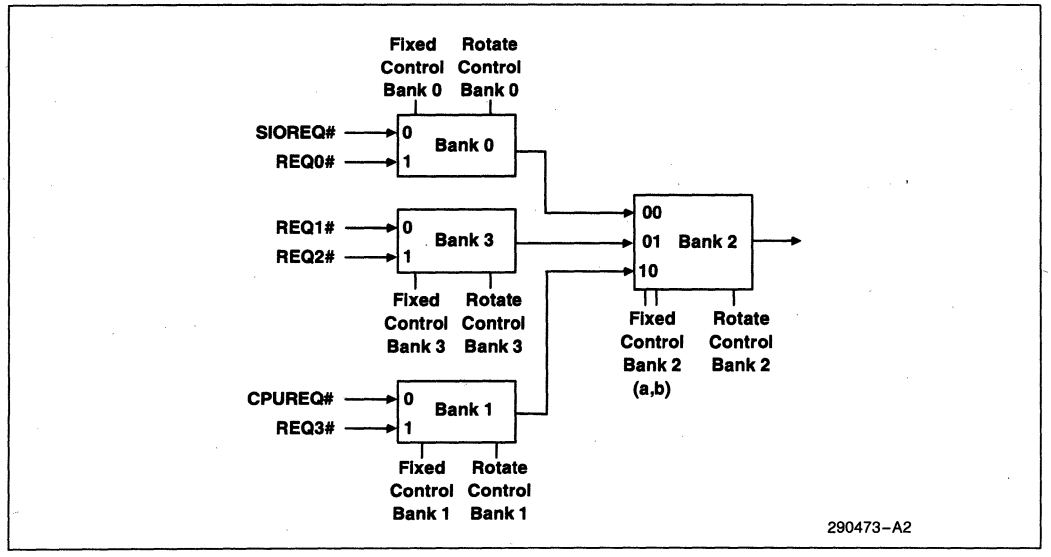


Figure 6. Arbiter Configuration Diagram for 82378ZB

5.2.2.1 Fixed Priority Mode

The 24 selectable fixed priority schemes are listed in Table 8.

Table 8. Fixed Priority Mode Bank Control Bits

Mode	Bank					Priority					
	3	2b	2a	1	0	Highest					Lowest
00	0	0	0	0	0	SIOREQ#	REQ0#	REQ2#	REQ3#	CPUREQ#	REQ1#
01	0	0	0	0	1	REQ0#	SIOREQ#	REQ2#	REQ3#	CPUREQ#	REQ#
02	0	0	0	1	0	SIOREQ#	REQ0#	REQ2#	REQ3#	REQ1#	CPUREQ#
03	0	0	0	1	1	REQ0#	SIOREQ#	REQ2#	REQ3#	REQ1#	CPUREQ#
04	0	0	1	0	0	CPUREQ#	REQ1#	SIOREQ#	REQ0#	REQ2#	REQ3#
05	0	0	1	0	1	CPUREQ#	REQ1#	REQ0#	SIOREQ#	REQ2#	REQ3#
06	0	0	1	1	0	REQ1#	CPUREQ#	SIOREQ#	REQ0#	REQ2#	REQ3#
07	0	0	1	1	1	REQ1#	CPUREQ#	REQ0#	SIOREQ#	REQ2#	REQ3#
08	0	1	0	0	0	REQ2#	REQ3#	CPUREQ#	REQ1#	SIOREQ#	REQ0#
09	0	1	0	0	1	REQ2#	REQ3#	CPUREQ#	REQ1#	REQ0#	SIOREQ#
0A	0	1	0	1	0	REQ2#	REQ3#	REQ1#	CPUREQ#	SIOREQ#	REQ0#
0B	0	1	0	1	1	REQ2#	REQ3#	REQ1#	CPUREQ#	REQ0#	SIOREQ#
0C–0F	0	1	1	x	x	Reserved					
10	1	0	0	0	0	SIOREQ#	REQ0#	REQ3#	REQ2#	CPUREQ#	REQ1#
11	1	0	0	0	1	REQ0#	SIOREQ#	REQ3#	REQ2#	CPUREQ#	REQ1#
12	1	0	0	1	0	SIOREQ#	REQ0#	REQ3#	REQ2#	REQ1#	CPUREQ#
13	1	0	0	1	1	REQ0#	SIOREQ#	REQ3#	REQ2#	REQ1#	CPUREQ#
14	1	0	1	0	0	CPUREQ#	REQ1#	SIOREQ#	REQ0#	REQ3#	REQ2#
15	1	0	1	0	1	CPUREQ#	REQ1#	REQ0#	SIOREQ#	REQ3#	REQ2#
16	1	0	1	1	0	REQ1#	SPUREQ#	SIOREQ#	REQ0#	REQ3#	REQ2#
17	1	0	1	1	1	REQ1#	CPUREQ#	REQ0#	SIOREQ#	REQ3#	REQ2#
18	1	1	0	0	0	REQ3#	REQ2#	CPUREQ#	REQ1#	SIOREQ#	REQ0#
19	1	1	0	0	1	REQ3#	REQ2#	CPUREQ#	REQ1#	REQ0#	SIOREQ#
1A	1	1	0	1	0	REQ3#	REQ2#	REQ1#	CPUREQ#	SIOREQ#	REQ0#
1B		1	0	1	1	REQ3#	REQ2#	REQ1#	CPUREQ#	REQ0#	SIOREQ#
1C–1F	1	1	1	x	x	Reserved					

The fixed bank control bit(s) selects which requester is the highest priority device within that particular bank. For fixed priority mode, bits[7:4] of the PAPC Register and bit zero of ARBPRIX must be 0's (rotate mode disabled).

The selectable fixed priority schemes provide 24 of the 64 possible fixed mode permutations possible for the six masters.

5.2.2.2 Rotating Priority Mode

When any bank rotate control bit is set to a one, that particular bank rotates between the requesting inputs. Any or all banks can be set in rotate mode. If all four banks are set in rotate mode, the six supported masters are all rotated and the arbiter is in a pure rotating priority mode. If, within a rotating bank, the highest priority device (a) does not have an active request, the lower priority device (b or c) will be granted the bus. However, this does not change the rotation scheme. When the bank toggles, device b is the highest priority. Because of this, the maximum latency a device can encounter is two complete rotations.

5.2.2.3 Mixed Priority Mode

Any combination of fixed priority and rotate priority modes can be used in different arbitration banks to achieve a specific arbitration scheme.

5.2.2.4 Locking Masters

When a master acquires the LOCK# signal, the arbiter gives that master highest priority until the LOCK# signal is negated and FRAME# is negated. This ensures that a master that locked a resource will eventually be able to unlock that same resource.

5.2.3 MEMREQ#, FLSHREQ#, AND MEMACK# PROTOCOL

Before an ISA master or the DMA can be granted the PCI Bus, it is necessary that all PCI system posted write buffers be flushed (including the SIO's Posted Write Buffer). Also, since the ISA originated cycle could access memory on the host bridge, it's possible that the ISA master or the DMA could be held in wait states (via IOCHRDY) waiting for the host bridge arbitration for longer than the 2.5 μs ISA specification. The SIO has an optional mode called the Guaranteed Access Time Mode (GAT) that ensures that this timing specification is not violated. This is accomplished by delaying the ISA REQ# signal to the requesting master or DMA until the ISA Bus, PCI Bus, and the System Memory Bus are arbitrated for and owned.

Three PCI sideband signals, MEMREQ#, FLSHREQ#, and MEMACK# are used to support the System Posted Write Buffer Flushing and Guaranteed Access Time mechanisms. The MEMACK# signal is the common acknowledge signal for both mechanisms. Note that when MEMREQ# is asserted, FLSHREQ# is also asserted. Table 9 shows the relationship between MEMREQ# and FLSHREQ#:

Table 9. FLSHREQ#, MEMREQ#

FLSHREQ#	MEMREQ#	Meaning
1	1	Idle
0	1	Flush buffers pointing towards PCI to avoid ISA deadlock
1	0	Reserved
0	0	GAT mode, Guarantee PCI Bus immediate access to main memory

5.2.3.1 Flushing the System Posted Write Buffers

Once an ISA master or the DMA begins a cycle on the ISA Bus, the cycle can not be backed-off. It can only be held in wait states via IOCHRDY. In order to know the destination of ISA master cycles, the cycle needs to begin. However, after the cycle has started, no other device can intervene and gain ownership of the ISA Bus until the cycle has completed and arbitration is performed. A potential deadlock condition exists when an ISA originated cycle to the PCI Bus finds the PCI target inaccessible due to an interacting event that also requires the ISA Bus. To avoid this potential deadlock, all PCI posted write buffers in the system must be disabled and flushed before DACK can be returned. The buffers must remain disabled while the ISA Bus is occupied by an ISA master or the DMA.

When an ISA master or the DMA requests the ISA Bus, the SIO asserts FLSHREQ#. FLSHREQ# is an indication to the system to flush all posted write buffers pointing towards the PCI Bus. The SIO also flushes it's own Posted Write Buffer. Once the posted write buffers have been flushed and disabled, the system asserts MEMACK#. Once the SIO receives the MEMACK# acknowledgment signal, it asserts the DACK signal giving the requesting master the bus. FLSHREQ# stays active as long as the ISA master or DMA owns the ISA Bus.

5.2.3.2 Guaranteed Access Time Mode

Guaranteed Access Time (GAT) Mode is enabled/disabled via the PCI Arbiter Control Register. When this mode is enabled, the MEMREQ# and MEMACK# signals are used to guarantee that the ISA 2.5 μs IOCHRDY specification is not violated.

When an ISA master or DMA slave requests the ISA Bus (DREQ# active), the ISA Bus, the PCI Bus, and the memory bus must be arbitrated for and all three must be owned before the ISA master or DMA slave is granted the ISA Bus. After receiving the DREQ# signal from the ISA master or DMA slave, MEMREQ# and FLSHREQ# are asserted (FLSHREQ# is driven active, regardless of GAT mode being enabled or disabled). MEMREQ# is a request for direct access to main memory. MEMREQ# and FLSHREQ# will be asserted as long as the ISA master or the DMA owns the ISA Bus. When MEMACK# is received by the SIO (all posted write buffers are flushed and the memory bus is dedicated to the PCI interface), it will request the PCI Bus. When it is granted the PCI Bus, it asserts the DACK signal releasing the ISA Bus to the requesting master or the DMA.

The use of MEMREQ#, FLSHREQ#, and MEMACK# does not guarantee functionality with ISA masters that don't acknowledge IOCHRDY. These signals just guarantee the IOCHRDY inactive specification.

NOTE:
Usage of an external arbiter in GAT mode will require special logic in the arbiter.

5.2.4 RETRY THRASHING RESOLVE

When a PCI initiator's access is retried, the initiator releases the PCI Bus for a minimum of two PCI clocks and will then normally request the PCI Bus again. To avoid thrashing the bus with retry after retry, the PCI arbiter provides REQ# masking. The REQ# masking mechanism differentiates between SIO target retries and all other retries.

For initiators which were retried by the SIO as a target, the masked REQ# is flagged to be cleared upon RESUME# active. All other retries trigger the Master Retry Timer, if enabled. Upon expiration of this timer, the mask is cleared.

5.2.4.1 Resume Function (RESUME#)

The conditions under which the SIO forces a retry to a PCI master and will mask the REQ# are:

1. Any required buffer management
2. ISA Bus occupied by ISA master or DMA
3. The PCI to ISA Posted Write Buffer is full
4. The SIO is locked as a resource and LOCK# is asserted during the address process.

The RESUME# signal is pulsed whenever the SIO has retried a PCI cycle for one of the above reasons and that condition has passed. When RESUME# is asserted, the SIO will unmask the REQ#'s that are masked and flagged to be cleared by RESUME#.

If the internal arbiter is enabled, RESUME# is an internal signal. The RESUME# signal becomes visible as an output when the internal arbiter is disabled. This allows an external arbiter to optionally avoid retry thrashing associated with the SIO as a target. The RESUME# signal is asserted for one PCI clock.

5.2.4.2 Master Retry Timer

To re-enable a PCI master's REQ# which resulted in a retry to a slave other than the SIO, a SIO programmable Master Retry Timer has been provided. This timer can be programmed for 0 (disabled), 16, 32, or 64 PCICLKs. Once the SIO has detected that a PCI slave has forced a retry, the timer will be triggered and the corresponding master's REQ# will be masked. All subsequent PCI retries by this REQ# signal will by masked by the SIO. Expiration of this timer will unmask all of the masked requests. This timer has no effect on the request lines that have been masked due to a SIO retry.

If no other PCI masters are requesting the PCI Bus, all of the REQ#'s masked for the timer will be cleared and the timer will be reset. This is necessary to assist the host bridge in determining when to re-enable any disabled posted write buffers.

5.2.5 BUS PARKING

The SIO arbitration logic supplies a mechanism for PCI Bus parking. Parking is only allowed for the device which is tied to CPUREQ# (typically the system CPU). When bus parking is enabled, CPUGNT# will be asserted when no other agent is currently using or requesting the bus. This achieves the minimum PCI arbitration latency possible. Enabling of bus parking is achieved by programming the Arbiter Control Register. REQ0#, REQ1#, and the internal SIOREQ# are not allowed to park on the PCI Bus.

Upon assertion of CPUGNT# due to bus parking enabled and the PCI Bus idle, the CPU (or the parked agent) must ensure that AD[31:0], C/BE[3:0], and (one PCICLK later) PAR are driven. If bus parking is disabled, the SIO takes responsibility for driving the bus when it is idle.

5.2.6 BUS LOCK MODE

As an option, the SIO arbiter can be configured to run in Bus Lock Mode or Resource Lock Mode. The Bus Lock Mode is used to lock the entire PCI Bus. This may improve performance in some systems that frequently run quick read-modify-write cycles. Bus Lock Mode emulates the LOCK environment found in today's PC by restricting bus ownership when the PCI Bus is locked. With Bus Lock enabled, the arbiter recognizes a LOCK# being driven by any initiator and does not allow any other PCI initiator to be granted the PCI Bus until LOCK# and FRAME# are both negated indicating the master released lock. When Bus Lock is disabled, the default resource lock mechanism is implemented (normal resource lock) and a higher priority PCI initiator could intervene between the read and write cycles and run non-exclusive accesses to any unlocked resource.

5.2.7 POWER-UP CONFIGURATION

The SIO's arbiter is enabled if CPUREQ# is sampled high on the trailing edge of PCIRST#. When enabled, the arbiter is set in fixed priority mode 4 with CPU bus parking turned off. Fixed mode 4 guarantees that the CPU will be able to run accesses to the BIOS in order to configure the system, regardless of the state of the other REQ#'s. Note that the Host Bridge should drive CPUREQ# high during the trailing edge of PCIRST#. When the arbiter is enabled, the SIO acts as the central resource responsible for driving the AD[31:0], C/BE[3:0]#, and PAR signals when no one is granted the PCI Bus and the bus is idle. The SIO is always responsible for driving AD[31:0], C/BE[3:0]#, and PAR when it is granted the bus and as appropriate when it is the master of a transaction. After reset, if the arbiter is enabled, CPUGNT#, GNT0#, GNT1#, and the internal SIOGNT# will be driven based on the arbitration scheme and the asserted REQ#'s.

If an external arbiter is present in the system, the CPUREQ# signal should be tied low. When CPUREQ# is sampled low on the trailing edge of PCIRST#, the internal arbiter is disabled. When the internal arbiter is disabled, the SIO does not drive AD[31:0], C/BE[3:0]#, and PAR as the central resource. In this case, the SIO is only responsible for driving AD[31:0], C/BE[3:0]#, and PAR when it is granted the bus. If the SIO's arbiter is disabled, GNT0# becomes SIOREQ#, GNT1# becomes RESUME#, and REQ0# becomes SIOGNT#. This exposes the normally embedded SIO arbitration signals.

NOTE:
Usage of an external arbiter in GAT mode will require special logic in the arbiter.

5.3 ISA Interface

5.3.1 ISA INTERFACE OVERVIEW

The SIO incorporates a fully ISA Bus compatible master and slave interface. The SIO directly drives six ISA slots without external data or address buffers. The ISA interface also provides byte swap logic, I/O recovery support, wait-state generation, and SYSCLK generation.

The ISA interface supports the following types of cycles:

- PCI-initiated I/O and memory cycles to the ISA Bus.
- DMA compatible cycles between PCI memory and ISA I/O and between ISA I/O and ISA memory, DMA type "A", type "B", and type "F" cycles between PCI memory and ISA I/O.
- ISA Refresh cycles initiated by either the SIO or an external ISA master.
- ISA master-initiated memory cycles to the PCI Bus and ISA master-initiated I/O cycles to the internal SIO registers.

The refresh and DMA cycles are shown and described in Section 5.4.

5.3.2 SIO AS AN ISA MASTER

The SIO executes ISA cycles as an ISA master whenever a PCI initiated cycle is forwarded to the ISA Bus. The SIO also acts as an ISA master on behalf of DMA and refresh.

ISYSCLK is an internal 8 MHz clock.

5.3.3 SIO AS AN ISA SLAVE

The SIO operates as an ISA slave when:

- An ISA master accesses SIO internal registers.
- An ISA master accesses PCI memory on the PCI Bus.

5.3.3.1 ISA Master Accesses To SIO Registers

An ISA Bus master has access to SIO internal registers as shown in Table 19. An ISA master to SIO register cycle will always run as an 8-bit extended cycle (IOCHRDY will be held inactive until the cycle is completed).

Table 10. Arbitration Latency

Bus Condition	Arbitration Latency
Parked	0 PCICLKs for Agent 0, 2 PCICLKs for All Other
Not Parked	1 PCICLK for All Agents

5.3.3.2 ISA Master Accesses to PCI Resource

An ISA master can access PCI memory, but not I/O devices residing on the PCI Bus. The ISA/DMA address decoder determines which memory cycles should be directed towards the PCI Bus. During ISA master read cycles to the PCI Bus, the SIO will return all 1's if the PCI cycle is target-aborted or does not respond.

If the SIO is programmed for GAT mode, the SIO arbiter will not grant the ISA Bus before gaining ownership of both the PCI Bus and system memory. However, if the SIO is not programmed in this mode, the SIO does not need to arbitrate for the PCI Bus before granting the ISA Bus to the ISA master. For more details on the arbitration, refer to Section 5.2.2.

All cycles forwarded to a PCI resource will run as 16-bit extended cycles (i.e. IOCHRDY will be held inactive until the cycle is completed).

Because the ISA bus size is different from the PCI bus size, the data steering logic inside the SIO is responsible for steering the data to the correct byte lanes on both buses, and assembling/disassembling the data as necessary.

5.3.4 ISA MASTER TO ISA SLAVE SUPPORT

During ISA master cycles to ISA slaves, the SIO drives several signals to support the transfer:

BALE:

This signal is driven high while the ISA master owns the ISA Bus.

AEN:

This signal is driven low while the ISA master owns the ISA Bus.

SMEMR# and SMEMW#:

These signals are driven active by the SIO whenever the ISA master drives a memory cycle to an address below 1 Mb.

Utility Bus Buffer Control Signals and Chip Select Signals:

These signals are driven active as appropriate whenever an ISA master accesses devices on the Utility Bus. For more details, see Section 5.9.

Data Swap Logic:

The data swap logic inside the SIO is activated as appropriate to swap data between the even and odd byte lanes. This is discussed in further detail in Section 5.3.5.

5.3.5 DATA BYTE SWAPPING

The data swap logic is integrated in the SIO. For slaves that reside on the ISA Bus, data swapping is performed if the slave (I/O or memory) and ISA bus master (or DMA) sizes differ and the upper (odd) byte of data is being accessed. Table 11 shows when data swapping is provided during DMA. Table 12 shows when data swapping is provided during ISA master cycles to 8-bit ISA slaves.

Table 11. DMA Data Swap

DMA I/O Device Size	ISA Memory Slave Size	Swap	Comments I/O	⟷	Memory
8-Bit	8-Bit	No	SD[7:0]	⟷	SD[7:0]
8-Bit	16-Bit	Yes	SD[7:0]	⟷	SD[7:0]
			SD[7:0]	⟷	SD[15:8]
16-Bit	8-Bit	No	Not Supported		
16-Bit	16-Bit	No	SD[15:0]	⟷	SD[15:0]

The SIO monitors the SBHE# and SA0 signals to determine when to swap the data. The SIO ensures that the data is placed on the appropriate byte lane.

Table 12. 16-Bit Master to 8-Bit Slave Data Swap

SBHE#	SA0	SD[15:8]	SD[7:0]	Comments
0	0	Odd	Even	Word Transfer (data swapping not required)
0	1	Odd	Even	Byte Swap(1,2)
1	0	—	Even	Byte Transfer (data swapping not required)
1	1	—	—	Not Allowed

NOTES:
1. For ISA master read cycles, the SIO swaps the data from the lower byte to the upper byte.
2. For ISA master write cycles, the SIO swaps the data from the upper byte to the lower byte.

5.3.6 ISA CLOCK GENERATION

The SIO generates the ISA system clock (SYSCLK). SYSCLK is a divided down version of the PCICLK (see Table 13). The clock divisor value is programmed through the ISA Clock Divisor Register.

Table 13. SYSCLK Generation from PCICLK

PCICLK (MHz)	Divisor (Programmable)	SYSCLK (MHz)
25	3	8.33
33	4 (default)	8.33

NOTE:
For PCI frequencies less than 33 MHz (not including 25 MHz), a clock divisor value must be selected that ensures that the ISA Bus frequency does not violate the 6 MHz to 8.33 MHz SYSCLK specification.

5.3.7 WAIT STATE GENERATION

The SIO will add wait states to the following cycles, if IOCHRDY is sampled active low. Wait states will be added as long as IOCHRDY is low.

- During Refresh and SIO master cycles (not including DMA) to the ISA Bus.
- During DMA compatible transfers between ISA I/O and ISA memory only.

For ISA master cycles targeted for the SIO's internal registers or PCI memory, the SIO will always extend the cycle by driving IOCHRDY low until the transaction is complete.

The SIO will shorten the following cycles, if ZEROWS# is sampled active.

- During SIO master cycles (not including DMA) to 8-bit and 16-bit ISA memory.
- During SIO master cycles (not including DMA) to 8-bit ISA I/O only.

For ISA master cycles targeted for the SIO's internal registers or PCI memory, the SIO will not assert ZEROWS#.

NOTE:
If IOCHRDY and ZEROWS# are sampled active at the same time, IOCHRDY will take precedence and wait-states will be added.

5.3.8 I/O RECOVERY

The I/O recovery mechanism in the SIO is used to add additional recovery delay between PCI originated 8-bit and 16-bit I/O cycles to the ISA Bus. The SIO automatically forces a minimum delay of four SYSCLKs between back-to-back 8- and 16-bit I/O cycles to the ISA Bus. This delay is measured from the rising edge of the I/O command (IOR# or IOW#) to the falling edge of the next BALE. If a delay of greater than four SYSCLKs is required, the ISA I/O Recovery Time Register can be programmed to increase the delay in increments of SYSCLKs. No additional delay is inserted for back-to-back I/O "sub cycles" generated as a result of byte assembly or disassembly .

5.4 DMA Controller

5.4.1 DMA CONTROLLER OVERVIEW

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels (Channels 0–3 and Channels 5–7). DMA Channel 4 is used to cascade the two controllers and will default to cascade mode in the DMA Channel Mode (DCM) Register. In addition to accepting requests from DMA slaves, the DMA controller also responds to requests that are initiated by software. Software may initiate a DMA service request by setting any bit in the DMA Channel Request Register to a 1. The DMA controller for Channels 0–3 is referred to as "DMA-1" and the controller for Channels 4–7 is referred to as "DMA-2".

Each DMA channel may be programmed for 8- or 16-bit DMA device size and ISA-compatible, Type "A", Type "B", or Type "F" transfer timing. Each DMA channel defaults to the compatible settings for DMA device size: channels [3:0] default to 8-bit, count-by-bytes transfers, and channels [7:5] default to 16-bit, count-by-words (address shifted) transfers. The SIO provides the timing control and data size translation necessary for the DMA transfer between the PCI and the ISA Bus. ISA-compatible is the default transfer timing.

Full 32-bit addressing is supported as an extension of the ISA-compatible specification. Each channel includes a 16-bit ISA compatible Current Register which holds the 16 least-significant bits of the 32-bit address, and an ISA compatible Low Page Register which contains the eight second most significant bits. An additional High Page Register contains the eight most significant bits of the 32-bit address.

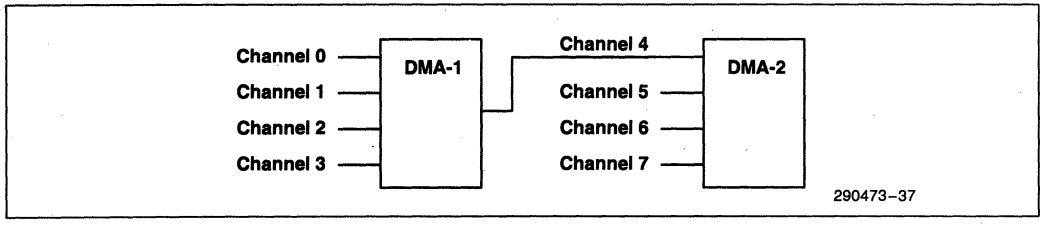


Figure 7. Internal DMA Controller

The DMA controller also features refresh address generation, and auto-initialization following a DMA termination.

The DMA controller receives commands from the ISA Bus arbiter to perform either DMA cycles or refresh cycles. The arbiter determines which requester from among the requesting DMA slaves, the PCI Bus, and refresh should have the bus.

The DMA controller is at any time either in master mode or slave mode. In master mode, the DMA controller is either servicing a DMA slave's request for DMA cycles, or allowing a 16-bit ISA master to use the bus via a cascaded DREQ signal. In slave mode, the SIO monitors both the ISA Bus and the PCI, decoding and responding to I/O read and write commands that address its registers.

Note that a DMA device (I/O device) is always on the ISA Bus, but the memory device is either on the ISA or PCI Bus. If the memory is decoded to be on the ISA Bus, then the DMA cycle will run as a compatible cycle. If the memory is decoded to be on the PCI Bus, the cycle can run as compatible, "A", "B", or "F" type. The ISA controller will not drive a valid address for type "A", "B", and "F" DMA transfers on the ISA Bus.

When the SIO is running a DMA cycle in compatible timing mode, the SIO will drive the MEMR# or MEMW# strobes if the address is less than 16 MBytes (00000000h–00FFFFFFh). These memory strobes will be generated regardless of whether the cycle is decoded for PCI or ISA memory. The SMEMR# and SMEMW# will be generated if the address is less than 1 MBytes (00000000h–000FFFFFh). If the address is greater than 16 MBytes (01000000h–FFFFFFFFh) the MEMR# or MEMW# strobe will not be generated in order to avoid aliasing problems. For type "A", "B", and "F" timing mode DMA cycles, the SIO will only generate the MEMR# or MEMW# strobe when the address is decoded for ISA memory. When this occurs, the cycle converts to compatible mode timing.

During DMA cycles, the ISA controller drives AEN high to prevent the I/O devices from misinterpreting the DMA cycle as a valid I/O cycle. The BALE signal is also driven high during DMA cycles. Also, during DMA memory read cycles to the PCI Bus, the SIO will return all 1's to the ISA Bus if the PCI cycle is either target-aborted or does not respond.

Further details can be found in the 82C37 data sheet.

5.4.2 DMA TIMINGS

ISA Compatible timing is provided for DMA slave devices. Three additional timings are provided for I/O slaves capable of running at faster speeds. These timings are referred to as Type "A", Type "B", and Type "F".

5.4.2.1 Compatible Timing

Compatible timing runs at 8 SYSCLKs during the repeated portion of a Block or Demand mode transfer.

5.4.2.2 Type "A" Timing

Type "A" timing is provided to allow shorter cycles to PCI memory. Type "A" timing runs at 6 SYSCLKs (720 ns/cycle) during the repeated portion of a block or demand mode transfer. This timing assumes an 8.33 MHz SYSCLK. Type "A" timing varies from compatible timing primarily in shortening the memory operation to the minimum allowed by system memory. The I/O portion of the cycle (data setup on write, I/O read access time) is the same as with compatible cycles. The actual active command time is shorter, but it is expected that the DMA devices which provide the data access time or write data setup time should not require excess IOR# or IOW# command active time. Because of this, most ISA DMA devices should be able to use type "A" timing.

5.4.2.3 Type "B" Timing

Type "B" timing is provided for 8-/16-bit ISA DMA devices which can accept faster I/O timing. Type "B" only works with PCI memory. Type "B" timing runs at 5 SYSCLKs (600 ns/cycle) during the repeated portion of a Block or Demand mode transfer. This timing assumes an 8.33 MHz SYSCLK. Type "B" timing requires faster DMA slave devices than compatible timing in that the cycles are shortened so that the data setup time on I/O write cycles is shortened and the I/O read access time is required to be faster. Some of the current ISA devices should be able to support type "B" timing, but these will probably be more recent designs using relatively fast technology.

5.4.2.4 Type "F" Timing

Type "F" timing provides high performance DMA transfer capability. These transfers are mainly for fast I/O devices (i.e. IDE devices). Type "F" timing runs at 3 SYSCLKs (360 ns/cycle) during the repeated portion of a Block or Demand mode transfer.

5.4.2.5 DREQ and DACK# Latency Control

The SIO DMA arbiter maintains a minimum DREQ to DACK# latency on DMA channels programmed to operate in compatible timing mode. This is to support older devices such as the 8272A. The DREQs are delayed by eight SYSCLKs prior to being seen by the arbiter logic. Software requests will not have this minimum request to DACK# latency.

5.4.3 ISA BUS/DMA ARBITRATION

The ISA Bus arbiter evaluates requests for the ISA Bus coming from several different sources. The DMA unit, the refresh counter, and the PCI Bus (primarily the Host CPU) may all request access to the ISA Bus. Additionally, 16-bit ISA masters may request the bus through a cascaded DMA channel.

The SIO ISA arbiter uses a three-way rotating priority arbitration method. At each level, the devices which are considered equal are given a rotating priority. On a fully loaded bus, the order in which the devices are granted bus access is independent of the order in which they assert a bus request. This is because devices are serviced based on their position in the rotation. The arbitration scheme assures that DMA channels access the bus with minimal latency.

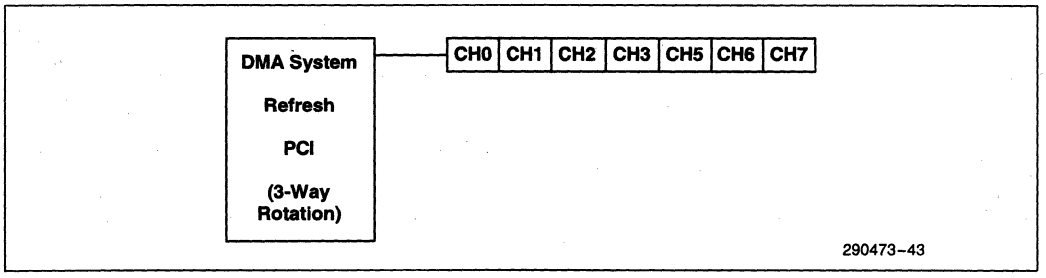


Figure 8. ISA Arbiter with DMA in Fixed Priority

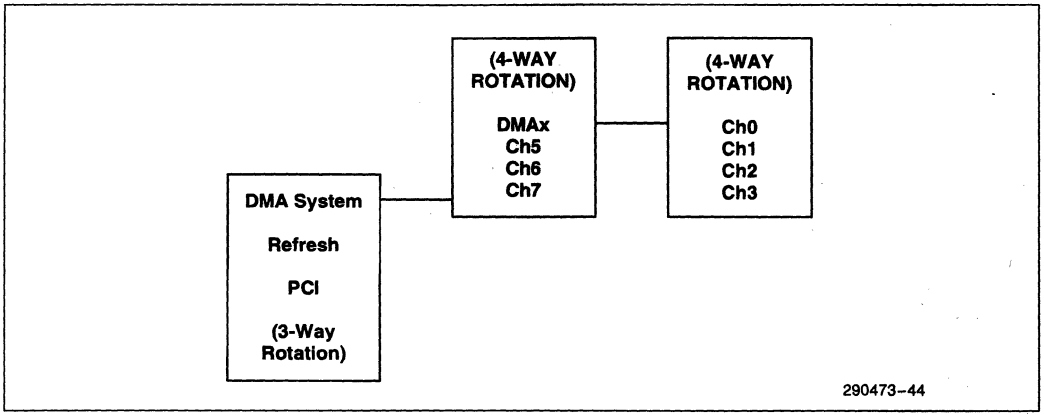


Figure 9. ISA Arbiter with DMA in Rotating Priority

5.4.3.1 Channel Priority

For priority resolution the DMA consists of two logical channel groups: channels 0–3 and channels 4–7 (see Figure 7). Each group may be in either fixed or rotate mode, as determined by the DMA Command Register.

For prioritization purposes, the source of the DMA request is transparent. DMA I/O slaves normally assert their DREQ line to arbitrate for DMA service. However, a software request for DMA service can be presented through each channel's DMA Request Register. A software request is subject to the same prioritization as any hardware request. Please see the detailed register description in Section 4.2.4 for Request Register programming information.

Fixed Priority

The initial fixed priority structure is as follows:

Table 14. Initial Fixed Priority Structure

High Priority . . . . . Low Priority
(0, 1, 2, 3), 5, 6, 7

The fixed priority ordering is 0, 1, 2, 3, 5, 6, and 7. In this scheme, Channel 0 has the highest priority, and channel 7 has the lowest priority. Channels [3:0] of DMA-1 assume the priority position of Channel 4 in DMA-2, thus taking priority over channels 5, 6, and 7.

Rotating Priority

Rotation allows for "fairness" in priority resolution. The priority chain rotates so that the last channel serviced is assigned the lowest priority in the channel group (0–3, 5–7).

Channels 0–3 rotate as a group of 4. They are always placed between Channel 5 and Channel 7 in the priority list.

Channel 5–7 rotate as part of a group of 4. That is, channels (5–7) form the first three positions in the rotation, while channel group (0–3) comprises the fourth position in the arbitration.

Table 15 demonstrates rotation priority.

Table 15. Rotating Priority Example

Programmed Mode	Action	Priority High .....Low
Group (0–3) is in Rotation Mode Group (4–7) is in Fixed Mode	1) Initial Setting	(0, 1, 2, 3), 5, 6, 7
	2) After Servicing Channel 2	(3, 0, 1, 2), 5, 6, 7
	3) After Servicing Channel 3	(0, 1, 2, 3), 5, 6, 7
Group (0–3) is in Rotation Mode Group (4–7) is in Rotation Mode	1) Initial Setting	(0, 1, 2, 3), 5, 6, 7
	2) After Servicing Channel 0	5, 6, 7, (1, 2, 3, 0)
	3) After Servicing Channel 5	6, 7, (1, 2, 3, 0), 5
	4) After servicing Channel 6	7, (1, 2, 3, 0), 5, 6
	5) After servicing Channel 7	(1, 2, 3, 0), 5, 6, 7

NOTE:
The first servicing of channel 0 caused double rotation.

5.4.3.2 DMA Preemption In Performance Timing Modes

A DMA slave device that is not programmed for compatible timing will be preempted from the bus by another device that requests use of the bus. This will occur, regardless of the priority of the pending request. For DMA devices not using compatible timing mode, the DMA controller stops the DMA transfer and releases the bus within 32 BCLK (4 μs) of a preemption. Upon the expiration of the 4 μs timer, the DACK will be inactivated after the current DMA cycle has completed. The bus will then be arbitrated for and granted to the highest priority requester. This feature allows flexibility in programming the DMA for long transfer sequences in a performance timing mode while guaranteeing that vital system services such as refresh are allowed access to the ISA Bus.

The 4 μs timer is not used in compatible timing mode. It is only used for DMA channels programmed for Type "A", Type "B", or Type "F" timing. It is also not used for 16-bit ISA masters cascaded through the DMA DREQ lines.

If the DMA channel that was preempted by the 4 μs timer was operating in Block Mode, an internal bit will be set so that the channel will be arbitrated for again, independent of the state of DREQ.

5.4.3.3. Arbitration during Non-Maskable Interrupts

If a non-maskable interrupt (NMI) is pending, and the CPU is requesting the bus, then the DMA controller will be bypassed each time it comes up for rotation. This will give the CPU the bus bandwidth it requires to process the interrupt as fast as possible.

5.4.3.4 Programmable Guaranteed Access Time Mode (GAT Mode)

The PCI Arbiter Register contains a bit for configuring the SIO in "Guaranteed Access Time Mode" (GAT Mode). This mode guarantees that the 2.5 μs CHRDY time-out specification for ISA masters running cycles to PCI will not be exceeded. When an ISA master or DMA slave arbitrates for the ISA Bus, and the SIO is configured in Guaranteed Access Time Mode, the MEMREQ# pin will be asserted by the PCI arbiter in order to gain ownership of main memory. The arbitration for the PCI and then the main memory bus must be completed prior to granting the DACK# to the ISA master or DMA slave. A MEMACK# signal to the SIO indicates that the SIO now owns main memory and can grant the DACK# to the ISA master or DMA slave. A detailed description is contained in Section 5.2.3.2.

5.4.4 REGISTER FUNCTIONALITY

Please see Section 4.2 for detailed information on register programming, bit definitions, and default values/functions of the DMA registers after a PCIRST#.

DMA Channel 4 is used to cascade the two DMA controllers together and should not be programmed for any mode other than cascade. The DMA Channel Mode Register for channel 4 will default to cascade mode. Special attention should also be take when programming the Command and Mask Registers as related to channel 4.

5.4.4.1 Address Compatibility Mode

Whenever the DMA is operating in address compatibility mode, the addresses do not increment or decrement through the High and Low Page Registers, and the High Page Register is set to 00h. This is compatible with the 82C37 and Low Page Register implementation used in the PC/AT. This mode is set when any of the lower three address bytes of a channel are programmed. If the upper byte of a channel's address is programmed last, the channel will go into extended address mode. In this mode, the high byte may be any value and the address will increment or decrement through the entire 32-bit address.

After PCIRST# is negated, all channels will be set to address compatibility mode. The DMA Master Clear command will also reset the proper channels to address compatibility mode.

5.4.4.2 Summary of DMA Transfer Sizes

Table 16 lists each of the DMA device transfer sizes. The column labeled "Current Byte/Word Count Register" indicates that the register contents represents either the number of bytes to transfer or the number of 16-bit words to transfer. The column labeled "Current Address Increment/Decrement" indicates the number added to or taken from the Current Address register after each DMA transfer cycle. The DMA Channel Mode Register determines if the Current Address Register will be incremented or decremented.

5.4.4.3 Address Shifting when Programmed for 16-Bit I/O Count by Words

To maintain compatibility with the implementation of the DMA in the PC/AT which used the 82C37, the DMA will shift the addresses when the DMA Channel Extended Mode Register is programmed for, or defaulted to, transfers to/from a 16-bit device count-by-words. Note that the least significant bit of the Low Page Register is dropped in 16-bit shifted mode. When programming the Current Address Register when the DMA channel is in this mode, the Current Address must be programmed to an even address with the address value shifted right by one bit. The address shifting is shown in Table 17.

5.4.4.4 Autoinitialize

By programming a bit in the DMA Channel Mode Register, a channel may be set up as an autoinitialize channel. During Autoinitialize initialization, the original values of the Current Page, Current Address and Current Byte/Word Count Registers are automatically restored from the Base Page, Address, and Byte/Word Count Registers of that channel following TC. The Base Registers are loaded simultaneously with the Current Registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in autoinitialize. Following Autoinitialize, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected.

Table 16. DMA Transfer Size

DMA Device Date Size and Word Count	Current Byte/Word Count Register	Current Address Increment/Decrement
8-Bit I/O, Count by Bytes	Bytes	1
16-Bit I/O, Count by Words (Address Shifted)	Words	1
16-Bit I/O, Count by Bytes	Bytes	2

Table 17. Address Shifting in 16-Bit I/O DMA Transfers

Output Address	8-Bit I/O Programmed Address	16-Bit I/O Programmed Address (Shifted)	16-Bit I/O Programmed Address (No Shift)
A0	A0	0	A0
A[16:1]	A[16:1]	A[15:0]	A[16:1]
A[31:17]	A[31:17]	A[31:17]	A[31:17]

NOTE:
The least significant bit of the Low Page Register is dropped in 16-bit shifted mode.

5.4.5 SOFTWARE COMMANDS

There are three additional special software commands which can be executed by the DMA controller. The three software commands are:

1. Clear Byte Pointer Flip-Flop
2. Master Clear
3. Clear Mask Register

They do not depend on any specific bit pattern on the data bus.

5.4.5.1 Clear Byte Pointer Flip-Flop

This command is executed prior to writing or reading new address or word count information to/from the DMA controller. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

When the Host CPU is reading or writing DMA registers, two Byte Pointer Flip-Flops are used; one for channels 0–3 and one for channels 4–7. Both of these act independently. There are separate software commands for clearing each of them (0Ch for channels 0–3, 0D8h for channels 4–7).

5.4.5.2 DMA Master Clear

This software instruction has the same effect as the hardware reset. The Command, Status, Request, and Internal First/Last Flip-Flop Registers are cleared and the Mask Register is set. The DMA controller will enter the idle cycle.

There are two independent master clear commands, 0Dh which acts on channels 0–3, and 0DAh which acts on channels 4–7.

5.4.5.3 Clear Mask Register

This command clears the mask bits of all four channels, enabling them to accept DMA requests. I/O port 00Eh is used for channels 0–3 and I/O port 0DCh is used for channels 4–7.

5.4.6 TERMINAL COUNT/EOP SUMMARY

This is a summary of the events that will happen as a result of a terminal count or external EOP when running DMA in various modes. (See Table 18.)

5.4.7 ISA REFRESH CYCLES

Refresh cycles are generated by two sources: the refresh controller inside the SIO component or by ISA bus masters other than the SIO. The ISA bus controller will enable the address lines SA[15:0] so that when MEMR# goes active, the entire ISA system memory is refreshed at one time. Memory slaves on the ISA Bus must not drive any data onto the data bus during the refresh cycle.

Counter 1 in the timer register set should be programmed to provide a request for refresh about every 15 μs.

Table 18. Terminal Count/EOP Summary Table

Conditions AUTOINIT	No		Yes	
Event				
Word Counter Expired	Yes	X	Yes	X
EOP Input	X	Asserted	X	Asserted
Result				
Status TC	set	set	set	set
Mask	set	set	—	—
SW Request	clr	clr	clr	clr
Current Register	—	—	load	load

NOTES:
load = load current from base
— = no change
X = don't care
clr = clear

5.4.8 SCATTER/GATHER DESCRIPTION

Scatter/Gather (S/G) provides the capability of transferring multiple buffers between memory and I/O without CPU intervention. In Scatter/Gather, the DMA can read the memory address and word count from an array of buffer descriptors, located in system memory (ISA or PCI), called the Scatter/Gather Descriptor (SGD) Table. This allows the DMA controller to sustain DMA transfers until all of the buffers in the SGD Table are transferred.

The S/G Command and Status Registers are used to control the operational aspect of S/G transfers. The SGD Table Pointer Register holds the address of the next buffer descriptor in the SGD Table.

The next buffer descriptor is fetched from the SGD Table by a DMA read transfer. DACK# will not be asserted for this transfer because the IO device is the SIO itself. The SIO will fetch the next buffer descriptor from either PCI memory or ISA memory, depending on where the SGD Table is located. If the SGD table is located in PCI memory, the memory read will use the line buffer to temporarily store the PCI read before loading it into the DMA S/G registers. The line buffer mode (8 byte or single transaction) for the S/G fetch operation will be the same as what is set for all DMA operations. If set in 8 byte mode, the SGD Table fetches will be PCI burst memory reads. The SGD Table PCI cycle fetches are subject to all types of PCI cycle termination (retry, disconnect, target-abort, master-abort). The fetched SGD Table data is subject to normal line buffer coherency management and invalidation. EOP will be asserted at the end of the complete link transfer.

To initiate a typical DMA Scatter/Gather transfer between memory and an I/O device, the following steps are required:

1. Software prepares a SGD Table in system memory. Each SGD is 8 bytes long and consists of an address pointer to the starting address and the transfer count of the memory buffer to be transferred. In any given SGD Table, two consecutive SGDs are offset by 8 bytes and are aligned on a 4-byte boundary.

   Each Scatter/Gather Descriptor for the linked list contains the following information:

   a. Memory Address (buffer start) 4 bytes

   b. Transfer Size (buffer size) 2 bytes

   c. End of Link List 1 bit (MSB)
2. Initialize the DMA Channel Mode and DMA Channel Extended Mode Registers with transfer specific information like 8-/16-bit I/O device, Transfer Mode, Transfer Type, etc.
3. Software provides the starting address of the SGD Table by loading the SGD Table Pointer Register.
4. Engage the Scatter/Gather function by writing a Start command to the S/G Command Register.
5. The Mask register should be cleared as the last step of programming the DMA register set. This is to prevent the DMA from starting a transfer with a partially loaded command description.
6. Once the register set is loaded and the channel is unmasked, the DMA will generate an internal request to fetch the first buffer from the SGD Table.

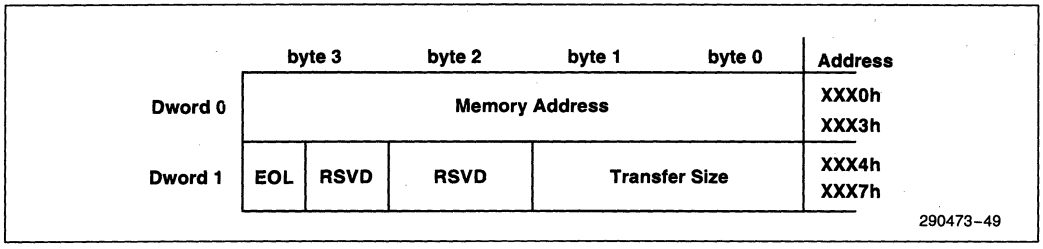


Figure 10. SGD Format

After the above steps are finished, the DMA will then respond to DREQ or software requests. The first transfer from the first buffer moves the memory address and word count from the Base register set to the Current register set. As long as S/G is active and the Base register set is not loaded and the last buffer has not been fetched, the channel will generate a request to fetch a reserve buffer into the Base register set. The reserve buffer is loaded to minimize latency problems going from one buffer to another. Fetching a reserve buffer has a lower priority than completing DMA transfers for the channel.

The DMA controller will terminate a Scatter/Gather cycle by detecting an End of List (EOL) bit in the SGD Table. After the EOL bit is detected, the channel transfers the buffers in the Base and Current register sets, if they are loaded. At terminal count the channel asserts EOP or IRQ13, depending on its programming and set the terminate bit in the S/G Status Register. If the channel asserted IRQ13, then the appropriate bit is set in the S/G Interrupt Status Register. The active bit in the S/G Status Register will be reset and the channel's Mask bit will be set.

5.5 Address Decoding

The SIO contains two address decoders; one to decode PCI master cycles and one to decode DMA/ISA master cycles. Two decoders are required to support the PCI and ISA Buses running concurrently. The PCI address decoder decodes the address from the multiplexed PCI address/data bus. The DMA/ISA master address decoder decodes the address from the ISA address bus for DMA and ISA master cycles. The address decoders determine how the cycle is handled.

1

5.5.1 PCI ADDRESS DECODER

PCI address decoding is always a function of AD[31:2]. The information contained in the two low order bits (AD[1:0]) varies for memory, I/O, and configuration cycles.

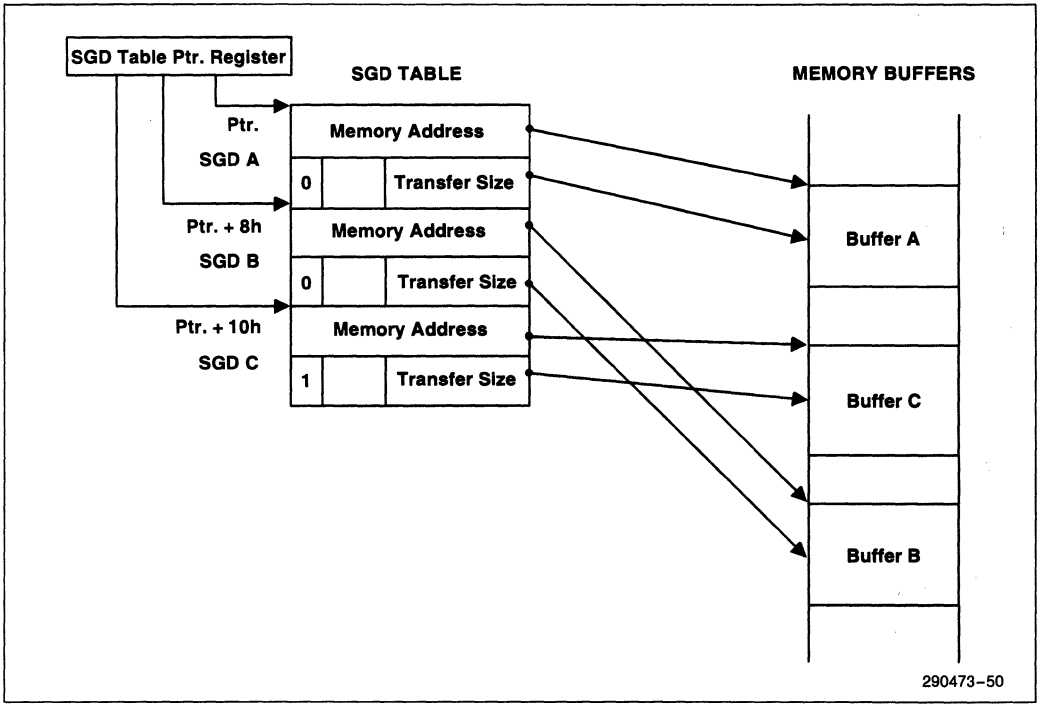


Figure 11. Link List Example

For I/O cycles, AD[31:0] are all decoded to provide a byte address. The byte enables determine which byte lanes contain valid data. The SIO requires that PCI accesses to byte-wide internal registers must assert only one byte enable.

For memory cycles, accesses are decoded as Dword accesses. This means that AD[1:0] are ignored for decoding memory cycles. The byte enables are used only to determine which byte lanes contain valid data.

For configuration cycles, DEVSEL# is a function of IDSEL# and AD[1:0]. DEVSEL# is generated only when AD[1:0] are both zero. If either AD[1:0] are non-zero, the cycle is ignored by the SIO. Individual bytes of a configuration register can be accessed with the byte enables. A particular configuration register is selected using AD[7:2]. Again, the byte enables determine which byte lanes contain valid data.

All PCI cycles decoded in one of the following ways result in the SIO generating DEVSEL#. The PCI master cycle decoder decodes the following addresses based on the settings of the relevant configuration registers:

SIO I/O Addresses: Positively decodes I/O addresses for registers contained within the SIO (exceptions: 60h, 92h, 3F2h, 372h, and F0h).

BIOS Memory Space: Positively decodes BIOS memory space.

MEMCS# Address Decoding: Decodes memory addresses that reside on the other side of the Host bridge and generates the MEMCS# signal. (SIO does not generate DEVSEL# in this case). The address range(s) used for this decoding is selected via the MEMCSCON, MEMCSBOH, MEMCSTOH, MEMCSTOM, MAR1, MAR2, and MAR3 Registers (see Section 4.1).

Subtractively Decoding Cycles to ISA: Subtractively decodes cycles to the ISA Bus. Accesses to registers 60h, 92h, 3F2h, 372h, and F0h are also subtractively decoded to the ISA Bus.

One of the PCI requirements is that, upon power-up, PCI agents do not respond to any address. Typically, the only access to a PCI agent is through the IDSEL configuration mechanism until it is enabled through configuration. The SIO is an exception to this, since it controls access to the BIOS boot code. All addresses decoded by the PCI address decoder, that are enabled after chip reset, are accessible immediately after power-up.

5.5.1.1 SIO I/O Addresses

These addresses are the internal, non-configuration SIO register locations and are shown in the SIO Address Decoding Table, Table 19. These addresses are fixed. Note that the Configuration Registers, listed in Table 3, are accessed with PCI configuration cycles as described in Section 5.1.2.5

In general, PCI accesses to the internal SIO registers will not be broadcast to the ISA Bus. However, PCI accesses to addresses 70h, 60h, 92h, 3F2h, 372h, and F0h are exceptions. Read and write accesses to these SIO locations are broadcast onto the ISA Bus. PCI master accesses to SIO registers will be retried if the ISA Bus is owned by an ISA master or the DMA controller. All of the registers are 8 bit registers. Accesses to these registers must be 8 bit accesses. Target-abort is issued by the SIO when the internal SIO non-configuration registers are the target of a PCI master I/O cycle and more than one byte enable is active. Refer to Table 19 for the SIO Address Decoding Map.

Accesses to the BIOS Timer Register (78h–7Bh) are broadcast to the ISA bus only if this register is disabled. If this register is enabled, the cycle is not broadcast to the ISA bus.

The address decoding logic includes the read/write cycle type. For example, read cycles to write only registers are not positively decoded and get forwarded to the ISA bus via subtractive decoding.

Table 19. SIO Address Decoding

Address	Address				Type	Name	Block
	FEDC	BA98	7654	3210			
0000h	0000	0000	000x	0000	r/w	DMA1 CH0 Base and Current Address	DMA
0001h	0000	0000	000x	0001	r/w	DMA1 CH0 Base and Current Count	DMA
0002h	0000	0000	000x	0010	r/w	DMA1 CH1 Base and Current Address	DMA
0003h	0000	0000	000x	0011	r/w	DMA1 CH1 Base and Current Count	DMA
0004h	0000	0000	000x	0100	r/w	DMA1 CH2 Base and Current Address	DMA
0005h	0000	0000	000x	0101	r/w	DMA1 CH2 Base and Current Count	DMA
0006h	0000	0000	000x	0110	r/w	DMA1 CH3 Base and Current Address	DMA
0007h	0000	0000	000x	0111	r/w	DMA1 CH3 Base and Current Count	DMA
0008h	0000	0000	000x	1000	r/w	DMA1 Status(r) Command(w) Register	DMA
0009h	0000	0000	000x	1001	wo	DMA1 Write Request Register	DMA
000Ah	0000	0000	000x	1010	wo	DMA1 Write Single Mask Bit	DMA
000Bh	0000	0000	000x	1011	wo	DMA1 Write Mode Register	DMA
000Ch	0000	0000	000x	1100	wo	DMA1 Clear Byte Pointer	DMA
000Dh	0000	0000	000x	1101	wo	DMA1 Master Clear	DMA
000Eh	0000	0000	000x	1110	wo	DMA1 Clear Mask Register	DMA
000Fh	0000	0000	000x	1111	r/w	DMA1 Read/Write All Mask Register Bits	DMA
0020h	0000	0000	001x	xx00	r/w	INT 1 Control Register	PIC
0021h	0000	0000	001x	xx01	r/w	INT 1 Mask Register	PIC
0040h	0000	0000	010x	0000	r/w	Timer Counter 1—Counter 0 Count	TC
0041h	0000	0000	010x	0001	r/w	Timer Counter 1—Counter 1 Count	TC
0042h	0000	0000	010x	0010	r/w	Timer Counter 1—Counter 2 Count	TC
0043h	0000	0000	010x	0011	wo	Timer Counter 1 Command Mode Register	TC
0060h	0000	0000	0110	0000	ro	Reset UBus IRQ12	Control
0061h	0000	0000	0110	0xx1	r/w	NMI Status and Control	Control
0070h	0000	0000	0111	0xx0	wo	CMOS RAM Address and NMI Mask Register	Control
0078h(1)	0000	0000	0111	10xx	r/w	BIOS Timer	TC

Table 19. SIO Address Decoding (Continued)

Address	Address				Type	Name	Block
	FEDC	BA98	7654	3210			
0080h	0000	0000	100x	0000	r/w	DMA Page Register (Reserved)	DMA
0081h	0000	0000	100x	0001	r/w	DMA Channel 2 Page Register	DMA
0082h	0000	0000	1000	0010	r/w	DMA Channel 3 Page Register	DMA
0083h	0000	0000	100x	0011	r/w	DMA Channel 1 Page Register	DMA
0084h	0000	0000	100x	0100	r/w	DMA Page Register (Reserved)	DMA
0085h	0000	0000	100x	0101	r/w	DMA Page Register (Reserved)	DMA
0086h	0000	0000	100x	0110	r/w	DMA Page Register (Reserved)	DMA
0087h	0000	0000	100x	0111	r/w	DMA Channel 0 Page Register	DMA
0088h	0000	0000	100x	0100	r/w	DMA Page Register (Reserved)	DMA
0089h	0000	0000	100x	1001	r/w	DMA Channel 6 Page Register	DMA
008Ah	0000	0000	100x	1010	r/w	DMA Channel 7 Page Register	DMA
008Bh	0000	0000	100x	1011	r/w	DMA Channel 5 Page Register	DMA
008Ch	0000	0000	100x	1100	r/w	DMA Page Register (Reserved)	DMA
008Dh	0000	0000	100x	1101	r/w	DMA Page Register (Reserved)	DMA
008Eh	0000	0000	100x	1110	r/w	DMA Page Register (Reserved)	DMA
008Fh	0000	0000	100x	1111	r/w	DMA Low Page Register Refresh	DMA
0090h	0000	0000	100x	0000	r/w	DMA Page Register (Reserved)	DMA
0092h	0000	0000	1001	0010	r/w	System Control Port	Control
0094h	0000	0000	100x	0100	r/w	DMA Page Register (Reserved)	DMA
0095h	0000	0000	100x	0101	r/w	DMA Page Register (Reserved)	DMA
0096h	0000	0000	100x	0110	r/w	DMA Page Register (Reserved)	DMA
0098h	0000	0000	100x	1000	r/w	DMA Page Register (Reserved)	DMA
009Ch	0000	0000	100x	1100	r/w	DMA Page Register (Reserved)	DMA
009Dh	0000	0000	100x	1101	r/w	DMA Page Register (Reserved)	DMA
009Eh	0000	0000	100x	1110	r/w	DMA Page Register (Reserved)	DMA
009Fh	0000	0000	100x	1111	r/w	DMA low page Register Refresh	DMA
00A0h	0000	0000	101x	xx00	r/w	INT 2 Control Register	PIC
00A1h	0000	0000	101x	xx01	r/w	INT 2 Mask Register	PIC
00B2h	0000	0000	1011	0010	r/w	Advanced Power Management Control Port	PM
00B3h	0000	0000	1011	0011	r/w	Advanced Power Management Status Port	PM
00C0h	0000	0000	1100	000x	r/w	DMA2 CH0 Base and Current Address	DMA

Table 19. SIO Address Decoding (Continued)

Address	Address				Type	Name	Block
	FEDC	BA98	7654	3210			
00C2h	0000	0000	1100	001x	r/w	DMA2 CH0 Base and Current Count	DMA
00C4h	0000	0000	1100	010x	r/w	DMA2 CH1 Base and Current Address	DMA
00C6h	0000	0000	1100	011x	r/w	DMA2 CH1 Base and Current Count	DMA
00C8h	0000	0000	1100	100x	r/w	DMA2 CH2 Base and Current Address	DMA
00CAh	0000	0000	1100	101x	r/w	DMA2 CH2 Base and Current Count	DMA
00CCh	0000	0000	1100	110x	r/w	DMA2 CH3 Base and Current Address	DMA
00CEh	0000	0000	1100	111x	r/w	DMA2 CH3 Base and Current Count	DMA
00D0h	0000	0000	1101	000x	r/w	DMA2 Status(r) Command(w) Register	DMA
00D2h	0000	0000	1101	001x	wo	DMA2 Write Request Register	DMA
00D4h	0000	0000	1101	010x	wo	DMA2 Write Single Mask Bit	DMA
00D6h	0000	0000	1101	011x	wo	DMA2 Write Mode Register	DMA
00D8h	0000	0000	1101	100x	wo	DMA2 Clear Byte Pointer	DMA
00DAh	0000	0000	1101	101x	wo	DMA2 Master Clear	DMA
00DCh	0000	0000	1101	110x	wo	DMA2 Clear Mask Register	DMA
00DEh	0000	0000	1101	111x	r/w	DMA2 Read/Write All Mask Register Bits	DMA
00F0h	0000	0000	1111	0000	wo	Coprocessor Error	Control
0372h	0000	0011	0111	0010	wo	Secondary Floppy Disk Digital Output Reg.	Control
03F2h	0000	0011	1111	0001	wo	Primary Floppy Disk Digital Output Reg.	Control
040Ah	0000	0100	0000	1010	ro	Scatter/Gather Interrupt Status Register	DMA
040Bh	0000	0100	0000	1011	wo	DMA1 Extended Mode register	DMA
0410h(1)	0000	0100	0001	0000	wo	CH0 Scatter/Gather Command	DMA
0411h(1)	0000	0100	0001	0001	wo	CH1 Scatter/Gather Command	DMA
0412h(1)	0000	0100	0001	0010	wo	CH2 Scatter/Gather Command	DMA
0413h(1)	0000	0100	0001	0011	wo	CH3 Scatter/Gather Command	DMA
0415h(1)	0000	0100	0001	0101	wo	CH5 Scatter/Gather Command	DMA
0416h(1)	0000	0100	0001	0110	wo	CH6 Scatter/Gather Command	DMA
0417h(1)	0000	0100	0001	0111	wo	CH7 Scatter/Gather Command	DMA
0418h(1)	0000	0100	0001	1000	ro	CH0 Scatter/Gather Status	DMA
0419h(1)	0000	0100	0001	1001	ro	CH1 Scatter/Gather Status	DMA
041Ah(1)	0000	0100	0001	1010	ro	CH2 Scatter/Gather Status	DMA
041Bh(1)	0000	0100	0001	1011	ro	CH3 Scatter/Gather Status	DMA

Table 19. SIO Address Decoding (Continued)

Address	Address				Type	Name	Block
	FEDC	BA98	7654	3210			
041Dh(1)	0000	0100	0001	1101	ro	CH5 Scatter/Gather Status	DMA
041Eh(1)	0000	0100	0001	1110	ro	CH6 Scatter/Gather Status	DMA
041Fh(1)	0000	0100	0001	1111	ro	CH7 Scatter/Gather Status	DMA
0420h(1)	0000	0100	0010	00xx	r/w	CH0 Scatter/Gather Descriptor Table Pointer	DMA
0424h(1)	0000	0100	0010	01xx	r/w	CH1 Scatter/Gather Descriptor Table Pointer	DMA
0428h(1)	0000	0100	0010	10xx	r/w	CH2 Scatter/Gather Descriptor Table Pointer	DMA
042Ch(1)	0000	0100	0010	11xx	r/w	CH3 Scatter/Gather Descriptor Table Pointer	DMA
0434h(1)	0000	0100	0011	01xx	r/w	CH5 Scatter/Gather Descriptor Table Pointer	DMA
0438h(1)	0000	0100	0011	10xx	r/w	CH6 Scatter/Gather Descriptor Table Pointer	DMA
043Ch(1)	0000	0100	0011	11xx	r/w	CH7 Scatter/Gather Descriptor Table Pointer	DMA
0481h	0000	0100	1000	0001	r/w	DMA CH2 High Page Register	DMA
0482h	0000	0100	1000	0010	r/w	DMA CH3 High Page Register	DMA
0483h	0000	0100	1000	0011	r/w	DMA CH1 High Page Register	DMA
0487h	0000	0100	1000	0111	r/w	DMA CH0 High Page Register	DMA
0489h	0000	0100	1000	1001	r/w	DMA CH6 High Page Register	DMA
048Ah	0000	0100	1000	1010	r/w	DMA CH7 High Page Register	DMA
048Bh	0000	0100	1000	1011	r/w	DMA CH5 High Page Register	DMA
04D0	0000	0100	1101	0000	r/w	INT CNTRL-1 Edge Level Control Register	Control
04D1	0000	0100	1101	0001	r/w	INT CNTRL-2 Edge Level Control Register	Control
04D6h	0000	0100	1101	0010	wo	DMA2 Extended Mode Register	DMA

NOTE:
1. The I/O address of this register is relocatable. The value shown in this table is the default address location.

5.5.1.2 BIOS Memory Space

The 128 Kb BIOS memory space is located at 000E0000h to 000FFFFFh (top of 1 Mb), and is aliased at FFFE0000h to FFFFFFFFh (top of 4 Gb) and FFEE0000h to FFEFFFFFh (top of 4 Gb-1 Mb). The aliased regions account for the CPU reset vector and the uncertainty of the state of A20GATE when a software reset occurs. This 128 Kb block is split into two 64 Kb blocks. The top 64 Kb is always enabled while the bottom 64 Kb can be enabled or disabled (the aliases automatically match). Enabling the lower 64 Kb BIOS space (000E0000h to 000EFFFFh, 896 Kb-960 Kb) results in positively decoding this region and enables the BIOSCS# signal generation. The upper 64 Kb is positively decoded only if bit 6 = 1 in the ISA Clock Divisor Register. Otherwise this region is subtractively decoded. Positively decoding these cycles expedites BIOS cycles to the ISA Bus. Note that both of these regions are subtractively decoded if bit 4 in the MEMCS# Control Register is set to a 1.

When PCI master accesses to the 128 Kb BIOS space at 4 Gb-1 Mb are forwarded to the ISA Bus, the LA20 line is driven to a 1 to avoid aliasing at the 15 Mb area. The 4 Gb-1 Mb BIOS decode area accounts for the condition when A20M# is asserted and an ALT-CTRL-DEL reset is generated. The CPU's reset vector will access 4 Gb-1 Mb. When this gets forwarded to ISA, AD[32:24] are truncated and the access is aliased to 16 Mb-1 Mb = 15 Mb space. If ISA memory is present at 15 Mb, there will be contention. Forcing LA20 high aliases this region to 16 Mb. The alias here is permissible since this is the 80286 reset vector location.

In addition to the normal 128 Kb BIOS space, the SIO supports an additional 384 Kb BIOS space. The SIO can support a total of 512 Kb BIOS space. The additional 384 Kb region can only be accessed by PCI masters and resides at FFF80000h to FFFDFFFFh. When enabled via the UBCSA Register, memory accesses within this region will be positively decoded, forwarded to the ISA Bus, and encoded BIOSCS# will be generated. When forwarded to the ISA Bus, the PCI AD[23:20] signals will be propagated to the ISA LA[23:20] lines as all 1's which will result in aliasing this 512 Kb region at the top of the 16 Mb space. To avoid contention, ISA add-in memory must not be present in this space.

All PCI cycles positively decoded in the enabled BIOS space will be broadcast to the ISA Bus. Since the BIOS device is 8 or 16 bits wide and typically has very long access times, PCI burst reads from the BIOS space will invoke "disconnect target termination" semantics after the first data transaction in order to meet the PCI incremental latency guidelines.

The following tables and diagrams describe the operation of the SIO in response to PCI BIOS space accesses.

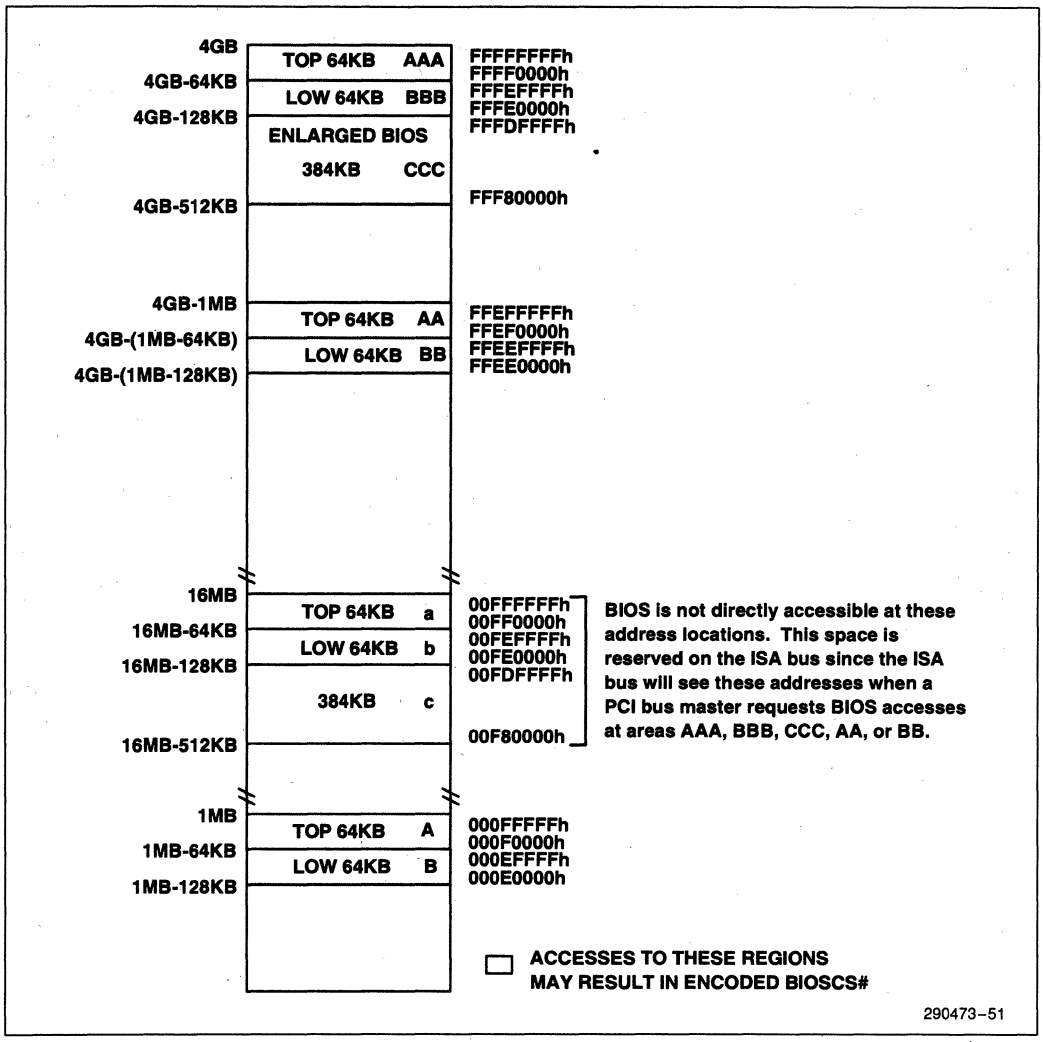


Figure 12. BIOS Space Decode Map

The BIOS space decode map, Figure 12, shows the possible BIOS spaces and the aliases throughout the memory space. The various regions are designated with code letters; "a's" for the top 64 Kb, "b's" for the low 64 Kb, and "c's" for the enlarged space.

Table 20 indicates the SIO's response to PCI BIOS space accesses based on its configuration state.

Table 20. PCI Master BIOS Space Decoding

Master	Region	Top 64 Kb BIOS Positive Decode Enabled(1)	Low 64 Kb BIOS Enabled(2)	Enlarged BIOS Enabled(3)	Encoded BIOSCS# Generated	LA20	Positive PCI Decode	Subtractive PCI Decode
PCI	A	0	x	x	Yes	Pass (0)	No	Yes
PCI	A	1	x	x	Yes	Pass (0)	Yes(5)	No(5)
PCI	B	x	0	x	No	Pass (0)	No	Yes
PCI	B	x	1	x	Yes	Pass (0)	Yes(5)	No(5)
PCI	a	1	x	x	No	Pass (1)	No	Yes
PCI	b	x	0	x	No	Pass (1)	No	Yes
PCI	c	x	x	0	No	Pass (1)	No	Yes
PCI	AA	0	x	x	Yes	1	No	Yes(4)
PCI	AA	1	x	x	Yes	1	Yes(4,5)	No(5)
PCI	BB	x	0	x	No	x	No	No
PCI	BB	x	1	x	Yes	1	Yes(4,5)	No(5)
PCI	AAA	0	x	x	Yes	Pass (1)	No	Yes(4)
PCI	AAA	1	x	x	Yes	Pass (1)	Yes(4,5)	No(5)
PCI	BBB	x	0	x	No	x	No	No
PCI	BBB	x	1	x	Yes	Pass (1)	Yes(4,5)	No(5)
PCI	CCC	x	x	0	No	x	No	No
PCI	CCC	x	x	1	Yes	Pass (1)	Yes(4)	No

NOTES:
1. The column labeled "Top 64 Kb BIOS Positive Decode Enable" shows the value of the ISA Clock Register bit 6. This bit determines the decoding for memory regions A, AA, and AAA (1 = positive, 0 = negative decoding).
   Note that if bit 4 in the MEMCS# Control Register is set to a 1 (Global MEMCS# decode enabled), the positive decoding function enabled by having ISA Clock Register bit 6 = 1 is ignored. Subtractive decoding is provided, instead.
2. The column labeled "Low 64 Kb BIOS Enable" shows the value of the Utility Bus Chip Select Enable A Bit 6. This bit determines whether memory regions B, BB, and BBB are enabled (bit = 1) or disabled (bit = 0).
3. The column labeled "Enlarged BIOS Enabled" shows the value of the Utility Bus Chip Select Enable A Bit 7. This bit determines whether memory region CCC is enabled (bit = 1) or disabled (bit = 0).
4. ISA memory is not allowed to be enabled at the corresponding aliased areas or contention will result.
5. When bit 4 in the MEMCS# Control Register is set to a 1 (Global MEMCS# decode enabled), positive decoding for these areas will be disabled. The SIO will only provide subtractive decoding in this case.

5.5.1.3 MEMCS# Decoding

For MEMCS# decoding, the SIO decodes sixteen ranges. Fourteen of these ranges can be enabled or disabled independently for both read and write cycles. The fifteenth range (0 KB–512 KB) and sixteenth range (programmable from 1 MB up to 512 MB in 2 MB increments) can be enabled or disabled only. Addresses within these enabled regions generate a MEMCS# signal that can be used by the host bridge to know when to forward PCI cycles to main memory. A seventeenth range is available that can be used to identify a "memory hole". Addresses within this hole will not generate a MEMCS#. The address regions are summarized:

- 0 KB to 512 KB Memory (can only be disabled if MEMCS# is completely disabled)
- 512 KB to 640 KB Memory
- (1 MB–64 KB) to 1 MB Memory (BIOS Area)
- 768 KB to 918 KB in 16 KB sections (total of 8 sections)
- 918 KB to 983 KB in 16 KB sections (total of 4 sections)
- 1M-to-programmable boundary on 2 MB increments from 2 MB up to 512 MB
- programmable "memory hole" in 64 KB increments between 1 MB and 16 MB

Table 21 and Figure 13 show the registers and decode areas for MEMCS#.

Table 21. MEMCS# Decoding Register Summary

MAR Registers	Attribute	Memory Segments	Comments
MCSCON[4] = 0	Disable	Disable MEMCS# Function	Enable/Disable MEMCS# Function
MCSCON[4] = 1	Enable	Enable MEMCS# Function	When Enabled, 0 KB to 512 KB Range is also Automatically Enabled (RE/WE)
MCSTOH/ MCSBOH	MEMCS# Hole	100000h–0FFFFFFh	1 MB to 16 MB Hole in MEMCS# Region
MCSTOM	MEMCS# Top	200000h–1FFFFFFFh	2 MB to 512 MB Top of MEMCS# Region
MCSCON[1:0]	[0] = RE[1] = WE	080000h–09FFFFh	512 KB to 640 KB R/W Enable
MCSCON[3:2]	[2] = RE[3] = WE	0F0000h–0FFFFFh	BIOS Area R/W Enable
MAR1[1:0]	[0] = RE[1] = WE	0C0000h–0C3FFFh	ISA Add-On BIOS R/W Enable
MAR1[3:2]	[2] = RE[3] = WE	0C4000h–0C7FFFh	ISA Add-On BIOS R/W Enable
MAR1[5:4]	[4] = RE[5] = WE	0C8000h–0CBFFFh	ISA Add-On BIOS R/W Enable
MAR1[7:6]	[6] = RE[7] = WE	0CC000h–0CFFFFh	ISA Add-On BIOS R/W Enable
MAR2[1:0]	[0] = RE[1] = WE	0D0000h–0D3FFFh	ISA Add-On BIOS R/W Enable
MAR2[3:2]	[2] = RE[3] = WE	0D4000h–0D7FFFh	ISA Add-On BIOS R/W Enable
MAR2[5:4]	[4] = RE[5] = WE	0D8000h–0DBFFFh	ISA Add-On BIOS R/W Enable
MAR2[7:6]	[6] = RE[7] = WE	0DC000h–0DFFFFh	ISA Add-On BIOS R/W Enable
MAR3[1:0]	[0] = RE[1] = WE	0E0000h–0E3FFFh	BIOS Extension R/W Enable
MAR3[3:2]	[2] = RE[3] = WE	0E4000h–0E7FFFh	BIOS Extension R/W Enable
MAR3[5:4]	[4] = RE[5] = WE	0E8000h–0EBFFFh	BIOS Extension R/W Enable
MAR3[7:6]	[6] = RE[7] = WE	0EC000h–0EFFFFh	BIOS Extension R/W Enable

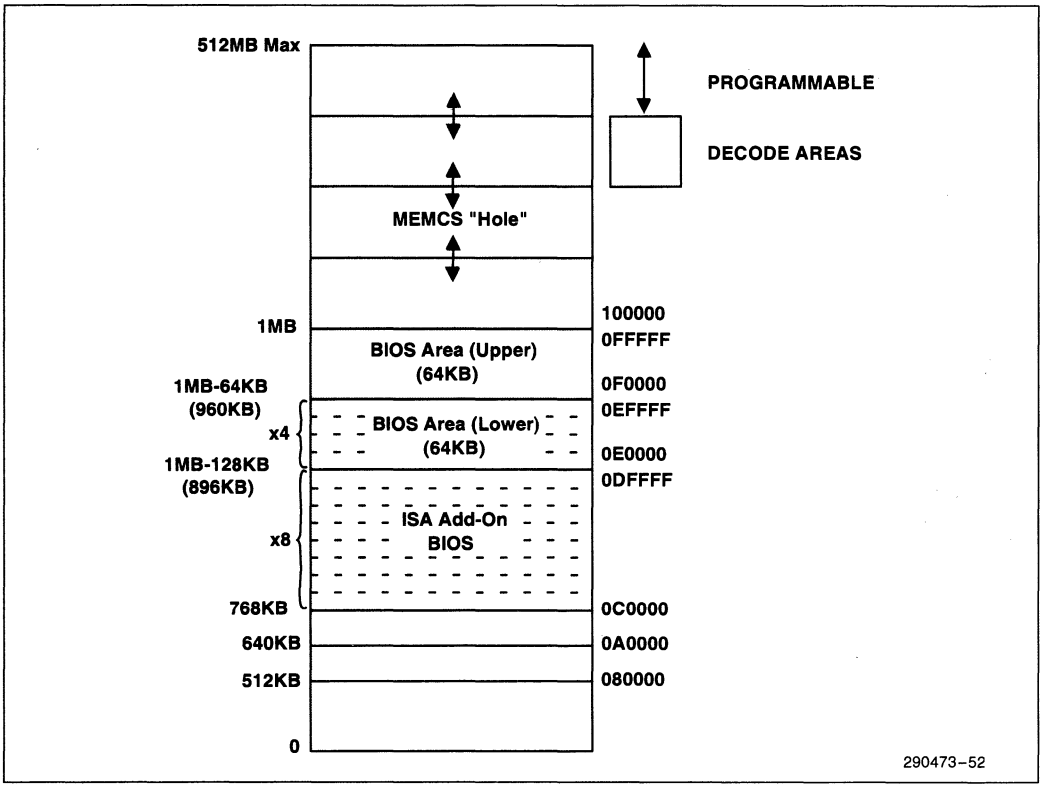


Figure 13. MEMCS# Decode Areas

The SIO generates MEMCS# from the PCI address. MEMCS# is generated from the clock edge after FRAME# is sampled active. MEMCS# will only go active for one PCI clock period. The SIO does not take any other action as a result of this decode other than generating MEMCS#. It is the responsibility of the device using the MEMCS# signal to generate DEVSEL#, TRDY# and any other cycle response. The device using MEMCS# will always generate DEVSEL# on the next clock. This fact can be used to avoid an extra clock delay in the subtractive decoder described in the next section.

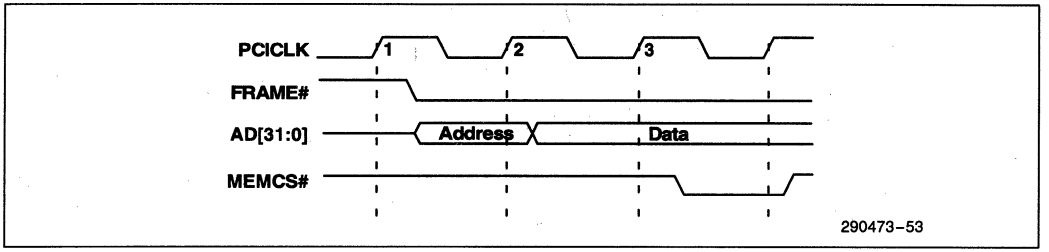


Figure 14. MEMCS# Generation

5.5.1.4 Subtractively Decoded Cycles to ISA

The addresses that reside on the ISA Bus could be highly fragmented. For this reason, subtractive decoding is used to forward PCI cycles to the ISA Bus. An inactive DEVSEL# will cause the SIO to forward the PCI cycle to the ISA Bus. The DEVSEL# sample point can be configured for three different settings. If the "fast" point is selected, the cycle will be forwarded to ISA when DEVSEL# is inactive at the F sample point as shown in Figure 15. If the "typical" point is selected, DEVSEL# will be sampled on both F and T, and if inactive, will be forwarded to the ISA Bus. Likewise, if the "slow" point is selected, DEVSEL# will be sampled at F, T, and S. The sample point should be configured to match the slowest PCI device in the system. This capability reduces the latency to ISA slaves when all PCI devices are "fast" and also allows for devices with slow decoding. Note that when these unclaimed cycles are forwarded to the ISA Bus, the SIO will drive the DEVSEL# active.

Since an active MEMCS# will always result in an active DEVSEL# at the "Slow" sample point, MEMCS# is used as an early indication of DEVSEL#. In this case, if the device using MEMCS# is the only "slow" agent in the system, the sample point can be moved in to the "typical" edge.

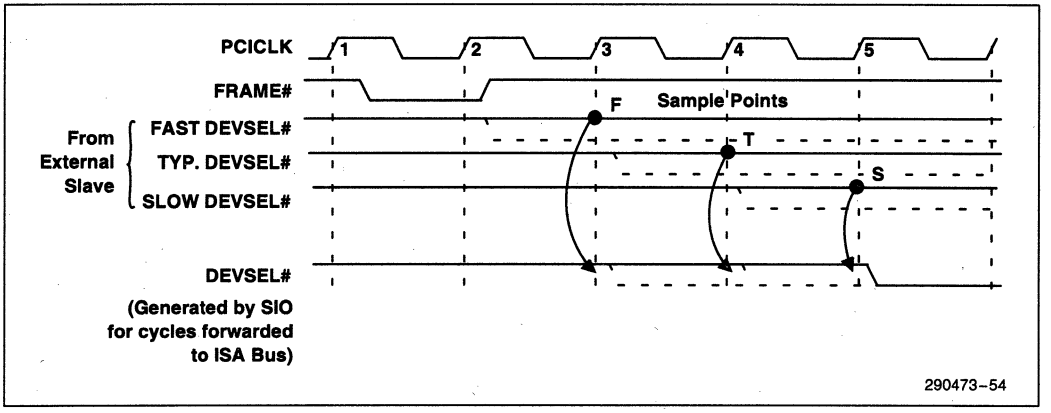


Figure 15. DEVSEL# Generation

Unclaimed PCI cycles with memory addresses above 16M and I/O addresses above 64K will not be forwarded to the ISA Bus. The SIO will not respond with DEVSEL# (BIOS accesses are an exception to this). This is required to avoid the possibility of aliasing. Under this condition, these unclaimed cycles will be recognized as such by the originating master and the master will use "master-abort" semantics to terminate the PCI cycle.

5.5.2 DMA/ISA MASTER CYCLE ADDRESS DECODER

The SIO also contains a decoder which is used to determine the destination of ISA master and DMA master cycles. This decoder provides:

Positive Decode to PCI: Positively decodes addresses to be forwarded to the PCI Bus. This includes addresses residing directly on PCI as well as addresses that reside on the back side of PCI bridges (Host Bridges).

Access to SIO Internal Registers: Positively decodes addresses to registers within the SIO.

BIOS Accesses: Positively decodes BIOS memory accesses and generates encoded BIOSCS#.

Utility Bus Chip Selects: Positively decodes utility bus chip selects.

Subtractive Decode: Subtractively decodes cycles to be contained to the ISA Bus.

5.5.2.1 Positive Decode to PCI

ISA master or DMA addresses that are positively decoded by this decoder will be propagated to the PCI Bus. This is the only way to forward a cycle from an ISA master or the DMA to the PCI Bus. If the cycle is not decoded by this decoder it will *not* be forwarded to the PCI Bus.

This decoder has several memory address regions to positively decode cycles that should be forwarded to the PCI Bus. These regions are listed below. Regions "a" through "e" are fixed and can be enabled or disabled independently. Region "f" defines a space starting at 1M with a programmable upper boundary up to 16 MB. Within this region a hole can be opened. Its size and location are programmable to allow a hole to be opened in the memory space. A memory address above 16 MB will be forwarded to the PCI Bus automatically. This is possible only during DMA cycles in which the DMA has been programmed for 32-bit addressing above 16 MB.

a. Memory: 0 KB–512 KB

b. Memory: 512 KB–640 KB

c. Memory: 640 KB–768 KB (Video buffer)

d. Memory: 768 KB–896 KB in eight 16K sections (Expansion ROM)

e. Memory: 896 KB–960 KB (lower BIOS area)

f. Memory: 1 MB-to-X MB (up to 16 MB) within which a hole can be opened. Accesses to the hole are not forwarded to PCI. The top of the region can be programmed on 64 KByte boundaries up to 16 MB. The hole can be between 64 KB and 8 MB in size in 64 KB increments located on any 64 KB boundary. (Refer to the ISA Address Decoder Register in the register description section, Section 5.5.2)

g. Memory: > 16 MB automatically forwarded to PCI

Figure 16 shows a map of the ISA master/DMA decode regions and Table 22 summarizes the registers used to configure the decoder.

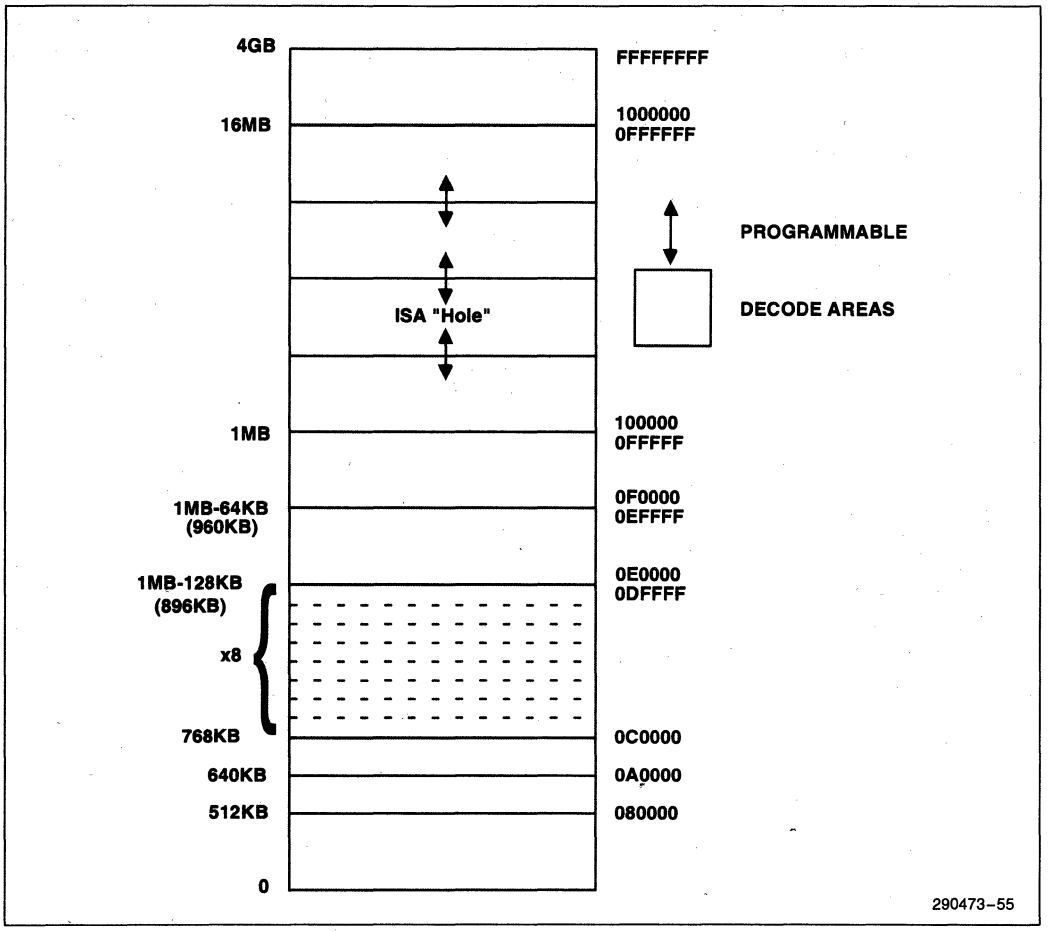


Figure 16. ISA Master/DMA to PCI Bus Decoder Regions

Table 22. ISA Master/DMA to PCI Bus Decoding Register Summary

MAR Registers	Attribute	Memory Segments	Comments
IADCON[7:4]	ISA Memory Top	100000h–0FFFFFFh	1 MB to 16 MB Top of ISA Region
IADTOH/IADBOH	ISA Hole	100000h–0FFFFFFh	1 MB to 16 MB Hole in ISA Region
IADCON[0]	Enable/Disable	000000h–07FFFFh	0 to 512 KB Enable/Disable
IADCON[1]	Enable/Disable	080000h–09FFFFh	512 KB to 640 KB Enable/Disable
IADCON[2]	Enable/Disable	0A0000h–0BFFFFh	640 KB to 768 KB Enable/Disable
IADCON[3]*	Enable/Disable	0E0000h–0EFFFFh	896 KB to 960 KB Lower BIOS Enable/Disable
IADRBE[0]	Enable/Disable	0C0000h–0C3FFFh	ISA Add-On BIOS (Expansion ROM) Enable
IADRBE[1]	Enable/Disable	0C4000h–0C7FFFh	ISA Add-On BIOS (Expansion ROM) Enable
IADRBE[2]	Enable/Disable	0C8000h–0CBFFFh	ISA Add-On BIOS (Expansion ROM) Enable
IADRBE[3]	Enable/Disable	0CC000h–0CFFFFh	ISA Add-On BIOS (Expansion ROM) Enable
IADRBE[4]	Enable/Disable	0D0000h–0D3FFFh	ISA Add-On BIOS (Expansion ROM) Enable
IADRBE[5]	Enable/Disable	0D4000h–0D7FFFh	ISA Add-On BIOS (Expansion ROM) Enable
IADRBE[6]	Enable/Disable	0D8000h–0DBFFFh	ISA Add-On BIOS (Expansion ROM) Enable
IADRBE[7]	Enable/Disable	0DC000h–0DFFFFh	ISA Add-On BIOS (Expansion ROM) Enable

NOTE:
* This can be overridden by bit 6 of the UBCSA Register being set to a 1.

5.5.2.2 SIO Internal Registers

Most of the internal SIO registers are accessible by ISA masters. Table 19 lists the registers that are not accessible by ISA masters. Registers accessed by ISA masters are run as 8-bit extended I/O cycles.

5.5.2.3 BIOS Accesses

The 128K BIOS memory space is located at 000E0000h to 000FFFFFh, and is aliased at FFFE0000h to FFFFFFFFh (top of 4 GB) and FFEE0000h to FFEFFFFFh (top of 4 GB–1 MB). The aliased regions account for the CPU reset vector and the uncertainty of the state of A20GATE when a software reset occurs. This 128K block is split into two 64K blocks. The top 64K is always enabled while the bottom 64K can be enabled or disabled (the aliases automatically match). ISA masters can only access BIOS in the 000E0000 to 000FFFFFh region.

ISA originated accesses to the enabled 64K sections of the BIOS space (000E0000h–000FFFFFh) will activate the encoded BIOSCS# signal. ISA originated cycles will not be forwarded to the PCI Bus. Encoded BIOSCS# is combinatorially generated from the ISA, SA, and LA address bus. Encoded BIOSCS# is disabled during refresh and DMA cycles. The ISA Master/DMA BIOS Decoding Table indicates the SIO's response to BIOS accesses based on the configuration state.

Table 23. ISA Master/DMA BIOS Decoding

Cycle		SIO Configuration			SIO Response		
Master	Region(1)	Top 64 KB PCI Positive Decode Enabled(2)	Low 64 KB BIOS Enabled(3)	Forward Low 64 KB to PCI Enabled(4)	Encoded BIOSCS# Generated	Forward to PCI	Contain to ISA
ISA/DMA	A	x	x	x	Yes	No	Yes
ISA/DMA	B	x	0(5)	0	No	No	Yes
ISA/DMA	B	x	0(5)	1	No	Yes	No
ISA/DMA	B	x	1	x	Yes	No	Yes
ISA/DMA	a	These cycles will be forwarded to PCI dependent on the state of the ISA Address Decoder Configuration Registers. Encoded BIOSCS# will not be generated for any of these cycles.					
ISA/DMA	b						
ISA/DMA	c						

NOTES:
1. The memory sections referenced can be found in Figure 12.
2. The column labeled "Top 64 KB BIOS Positive Decode Enabled" shows the value of the ISA Clock Divisor Configuration Register bit 6. This bit determines how the memory region is decoded (0 = subtractively decoded, 1 = positively decoded).
3. The column labeled "Low 64 KB BIOS Enable" shows the value of the Utility Bus Chip Select Enable A Configuration Register bit 6. This bit determines if the memory region is enabled (bit = 1) or disabled (bit = 0).
4. The column labeled "Forward Low 64 KB to PCI Enables" shows the value of the ISA Address Decoder Control Configuration Register Bit 3. This bit determines whether PCI Bus forwarding is enabled (bit = 1) or disabled (bit = 0).
5. Forward to PCI if IADCON Bit 6 = 1.

5.5.2.4 Utility Bus Encoded Chip Selects

The SIO generates encoded chip selects for certain functions that are located on the utility bus (formerly X-Bus). The encoded chip selects are generated combinatorially from the ISA SA[15:0] address bus. The encoded chip selects are decoded externally (see Figure 19).

The encoded chip select table (Table 24) shows the addresses that result in encoded chip select generation. Chip selects can be enabled or disabled via configuration registers. In general, the addresses shown in Table 24 do not reside in the SIO itself. Write only addresses 70h, 372h, 3F2h are exceptions since particular bits from these registers reside in the SIO. For ISA master cycles, the SIO will respond to writes to address 70h, 372h, and 3F2h by generating IOCHRDY and writing to the appropriate bits.

Note that the SIO monitors read accesses to address 60h to support the mouse function. In this case, IOCHRDY is not generated.

Table 24. Encoded Chip Select Table

Address	Address				Type	Name	Encoded Chip Select
	FEDC	BA98	7654	3210			
0060h	0000	0000	0110	00x0	r/w	Keyboard Controller	KEYBRDCS#
0064h	0000	0000	0110	01x0	r/w	Keyboard Controller	KEYBRDCS#
0070h	0000	0000	0111	0xx0	w	Real Time Clock Address	RTCALE#

Table 24. Encoded Chip Select Table (Continued)

Address	Address				Type	Name	Encoded Chip Select
	FEDC	BA98	7654	3210			
0071h	0000	0000	0111	0xx1	r/w	Real Time Clock Data	RTCCS#
0170h	0000	0001	0111	0000	r/w	Secondary Data Register	IDECS0#
0171h	0000	0001	0111	0001	r/w	Secondary Error Register	IDECS0#
0172h	0000	0001	0111	0010	r/w	Secondary Sector Count Register	IDECS0#
0173h	0000	0001	0111	0011	r/w	Secondary Sector Number Register	IDECS0#
0174h	0000	0001	0111	0100	r/w	Secondary Cylinder Low Register	IDECS0#
0175h	0000	0001	0111	0101	r/w	Secondary Cylinder High Register	IDECS0#
0176h	0000	0001	0111	0110	r/w	Secondary Drive/Head Register	IDECS0#
0177h	0000	0001	0111	0111	r/w	Secondary Status Register	IDECS0#
01F0h	0000	0001	1111	0000	r/w	Primary Data Register	IDECS0#
01F1h	0000	0001	1111	0001	r/w	Primary Error Register	IDECS0#
01F2h	0000	0001	1111	0010	r/w	Primary Sector Count Register	IDECS0#
01F3h	0000	0001	1111	0011	r/w	Primary Sector Number Register	IDECS0#
01F4h	0000	0001	1111	0100	r/w	Primary Cylinder Low Register	IDECS0#
01F5h	0000	0001	1111	0101	r/w	Primary Cylinder High Register	IDECS0#
01F6h	0000	0001	1111	0110	r/w	Primary Drive/Head Register	IDECS0#
01F7h	0000	0001	1111	0111	r/w	Primary Status Register	IDECS0#
0278h	0000	0010	0111	1x00	r/w	LPT3 PP Data Latch	LPTCS#
0279h	0000	0010	0111	1x01	r	LPT3 PP Status	LPTCS#
027Ah	0000	0010	0111	1x10	r/w	LPT3 PP Control	LPTCS#
027Bh	0000	0010	0111	1x11	r/w		LPTCS#
02F8h	0000	0010	1111	1000	r/w	COM2 SP Transmit/Receive Register	COM2CS#
02F9h	0000	0010	1111	1001	r/w	COM2 SP Interrupt Enable Register	COM2CS#
02FAh	0000	0010	1111	1010	r	COM2 SP Interrupt Identification Register	COM2CS#
02FBh	0000	0010	1111	1011	r/w	COM2 SP Line Control Register	COM2CS#
02FCh	0000	0010	1111	1100	r/w	COM2 SP Modem Control Register	COM2CS#
02FDh	0000	0010	1111	1101	r	COM2 SP Line Status Register	COM2CS#
02FEh	0000	0010	1111	1110	r	COM2 SP Modem Status Register	COM2CS#
02FFh	0000	0010	1111	1111	r/w	COM2 SP Scratch Register	COM2CS#

Table 24. Encoded Chip Select Table (Continued)

Address	Address				Type	Name	Encoded Chip Select
	FEDC	BA98	7654	3210			
0370h	0000	0011	0111	0000	r/w	Secondary Floppy Disk Extended Mode Register	FLOPPYCS#
0371h	0000	0011	0111	0001	r/w	Secondary Floppy Disk Extended Mode Register	FLOPPYCS#
0372	0000	0011	0111	0010	w	Secondary Floppy Disk Digital Output Register	FLOPPYCS#
0373h	0000	0011	0111	0011	r/w	Reserved	FLOPPYCS#
0374h	0000	0011	0111	0100	r/w	Secondary Floppy Disk Status Register	FLOPPYCS#
0375h	0000	0011	0111	0101	r/w	Secondary Floppy Disk Data Register	FLOPPYCS#
0376h	0000	0011	0111	0110	r/w	Secondary Alternate Status Register	IDECS1#
0377h	0000	0011	0111	0111	r	Secondary Drive Address Register	IDECS1#
0377h*	0000	0011	0111	011x	r/w	Secondary Floppy Disk Digital Input Register	FLOPPYCS#
0378h	0000	0011	0111	1x00	r/w	LPT2 PP Data Latch	LPTCS#
0379h	0000	0011	0111	1x01	r	LPT2 PP Status	LPTCS#
037Ah	0000	0011	0111	1x10	r/w	LPT2 PP Control	LPTCS#
037Bh	0000	0011	0111	1x11	r/w		LPTCS#
03BCh	0000	0011	1011	1100	r/w	LPT1 PP Data Latch	LPTCS#
03BDh	0000	0011	1011	1101	r	LPT1 PP Status	LPTCS#
03BEh	0000	0011	1011	1110	r/w	LPT1 PP Control	LPTCS#
03BFh	0000	0011	1011	1111	r/w		LPTCS#
03F0h	0000	0011	1111	0000	r/w	Primary Floppy Disk Extended Mode Register	FLOPPYCS#
03F1h	0000	0011	1111	0001	r/w	Primary Floppy Disk Extended Mode Register	FLOPPYCS#
03F2h	0000	0011	1111	0010	w	Primary Floppy Disk Digital Output Register	FLOPPYCS#
03F3h	0000	0011	1111	0011	r/w	Reserved	FLOPPYCS#
03F4h	0000	0011	1111	0100	r/w	Primary Floppy Disk Status Register	FLOPPYCS#
03F5h	0000	0011	1111	0101	r/w	Primary Floppy Disk Data Register	FLOPPYCS#
03F6h	0000	0011	1111	0110	r/w	Primary Drive Alternate Status Register	IDECS1#
03F7h	0000	0011	1111	0111	r	Primary Drive Address Register	IDECS1#
03F7h*	0000	0011	1111	011x	r/w	Primary Floppy Disk Digital Input Register	FLOPPYCS#

Table 24. Encoded Chip Select Table (Continued)

Address	Address				Type	Name	Encoded Chip Select
	FEDC	BA98	7654	3210			
03F8h	0000	0011	1111	1000	r/w	COM1 SP Transmit/Receive Register	COM1CS#
03F9h	0000	0011	1111	1001	r/w	COM1 SP Interrupt Enable Register	COM1CS#
03FAh	0000	0011	1111	1010	r	COM1 SP Interrupt Identification Register	COM1CS#
03FBh	0000	0011	1111	1011	r/w	COM1 SP Line Control Register	COM1CS#
03FCh	0000	0011	1111	1100	r/w	COM1 SP Modem Control Register	COM1CS#
03FDh	0000	0011	1111	1101	r	COM1 SP Line Status Register	COM1CS#
03FEh	0000	0011	1111	1110	r	COM1 SP Modem Status Register	COM1CS#
03FFh	0000	0011	1111	1111	r/w	COM1 SP Scratch Register	COM1CS#
0800h–08FFh	0000	1000	xxxx	xxxx	r/w		CFIGMEMCS#
0C00h	0000	1100	0000	0000	r/w		CPAGECS#

NOTE:
*If both the IDE and Floppy Drive are located on the UBUS, FLOPPYCS# will not be generated, IDECS1# will be generated.

5.5.2.5 Subtractive Decode to ISA

ISA master and DMA cycles not positively decoded by the ISA decoder are contained to the ISA Bus.

5.6 Data Buffering

The SIO contains data buffers to isolate the PCI Bus from the ISA Bus. The buffering is described from two perspectives: PCI master accesses to the ISA Bus (Posted Write Buffer) and DMA/ISA master accesses to the PCI Bus (Line Buffer). Temporarily buffering the data requires buffer management logic to ensure that the data buffers remain coherent.

5.6.1 DMA/ISA MASTER LINE BUFFER

An 8-byte Line Buffer is used to isolate the ISA Bus's slower I/O devices from the PCI Bus. The Line Buffer is bi-directional and is used by ISA masters and the DMA controller to assemble and disassemble data. Only memory data written to or read from the PCI Bus by an ISA master or DMA is assembled/disassembled using this 8 byte line buffer. I/O cycles do not use the buffer.

Bits 0 and 1 of the PCI Control Register set the buffer to operate in either single transaction mode (bit = 0) or 8-byte mode (bit = 1). Note that ISA masters and DMA controllers can have their buffer modes configured separately.

In single transaction mode, the buffer will store only one transaction. For DMA/ISA master writes, this single transaction buffer looks like a posted write buffer. As soon as the ISA cycle is complete, a PCI cycle is scheduled. Subsequent DMA/ISA master writes are held off in wait-states until the buffer is empty. For DMA/ISA master reads, only the data requested is read over the PCI Bus. For instance, if the DMA channel is programmed in 16-bit mode, 16 bits of data will be read from PCI. As soon as the requested data is valid on the PCI bus, it is latched into the Line Buffer and the ISA cycle is then completed, as timing allows. Single transaction mode will guarantee strong read and write ordering through the buffers.

In 8 byte mode, for write data assembly, the Line Buffer acts as two individual 4 byte buffers working in ping pong fashion. For read data disassembly, the Line Buffer acts as one 8 byte buffer.

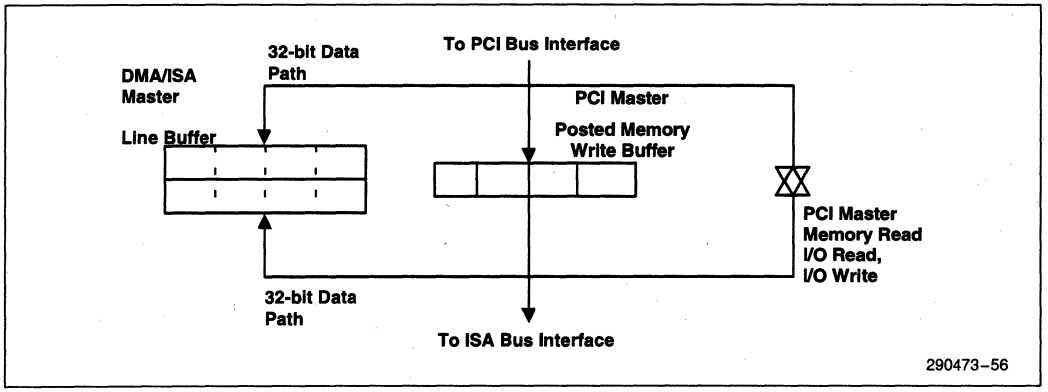


Figure 17. SIO Buffer Diagram

5.6.2 PCI MASTER POSTED WRITE BUFFER

PCI master memory write cycles destined to ISA memory are buffered in a 32-bit Posted Write Buffer. The PCI Memory Write and Memory Write and Invalidate commands are all treated as a memory write and can be posted, subject to the Posted Write Buffer status. The Posted Write Buffer has an address associated with it. A PCI master memory write can be posted any time the posted write buffer is empty and write posting is enabled (bit 2 of the PCI Control Configuration Register is set to a 1). Also, the ISA Bus must not be occupied. If the posted write buffer contains data, the PCI master write cycle is retried. If the posted write buffer is disabled, the SIO's response to a PCI master memory write is dependent on the state of the ISA Bus. If the ISA Bus is available and the posted write buffer is disabled, the cycle will immediately be forwarded to the ISA Bus (TRDY# will not be asserted until the ISA cycle has completed). If the ISA Bus is busy and the posted write buffer is disabled, the cycle is retried.

Memory read and I/O read and I/O write cycles do not use the 32-bit Posted Write Buffer.

5.6.3 BUFFER MANAGEMENT

Any time data is temporarily stored in the buffers between the ISA Bus and the PCI Bus, there are potential data coherency problems.

The SIO contains buffer management circuitry which guarantees data coherency by intercepting synchronization protocol between the buses and managing the buffers before synchronization communication between the buses is complete. The buffers are flushed or invalidated as appropriate before a bus cycle is allowed to occur in cases where data coherency could be lost.

5.6.3.1 DMA/ISA Master Line Buffer—Write State

When the DMA/ISA Master Line Buffer contains data that is to be written to the PCI Bus, it is in the Write State. The 8-byte line buffer is flushed when the line becomes full, when a subsequent write is a line miss, when a subsequent write would overwrite an already valid byte, or when a subsequent cycle is a read. The ISA master or DMA cycle that triggers the buffer flush will be held in wait-states until the flush is complete. The buffer is also flushed whenever there is a change in ISA Bus ownership as indicated by any DACK# signal going inactive.

Once the buffer is scheduled to be flushed to PCI, any PCI cycle to the SIO or ISA Bus will get retried by the SIO.

5.6.3.2 DMA/ISA Master Line Buffer—Read State

When the DMA/ISA Master Line Buffer contains data that has been read from the PCI Bus, it is in the Read State. The data in the buffer will be invalidated when the SIO accepts a PCI memory or I/O write cycle. The line buffer in the read state is also invalidated when a subsequent read is a line miss, or when a subsequent cycle is a write. The line buffer in the read state is not invalidated on a change of ISA ownership. Note that as bytes are disassembled from the line buffer, they are invalidated so that subsequent reads to the same byte will cause a line buffer miss.

5.6.3.3 PCI Master Posted Write Buffer

As soon as a PCI master has posted a memory write into the posted write buffer, the buffer is scheduled to be written to the ISA Bus. Any subsequent PCI master cycles to the SIO (including ISA Bus) will be retried until the posted write buffer is empty.

Prior to granting the ISA Bus to an ISA master or the DMA, the PCI master posted memory write buffer is flushed. Also, as long as the ISA master or DMA owns the ISA Bus, the posted write buffer is disabled. A PCI master write can not be posted while an ISA master or the DMA owns the ISA Bus.

5.7 SIO Timers

5.7.1 INTERVAL TIMERS

The SIO contains three counters that are equivalent to those found in the 82C54 programmable interval timer. The three counters are contained in one SIO timer unit, referred to as Timer-1. Each counter output provides a key system function. Counter 0 is connected to interrupt controller IRQ0 and provides a system timer interrupt for a time-of-day, diskette time-out, or other system timing functions. Counter 1 generates a refresh request signal and Counter 2 generates the tone for the speaker. Note that the 14.31818 MHz counters use OSC for a clock source.

Full details of this counter can be found in the 82C54 data sheet.

Table 25. Interval Timer Functions Table

Interval Timer Functions	
Function	**Counter 0—System Timer**
Gate	Always On
Clock In	1.193 MHz (OSC/12)
Out	INT-1 IRQ0
Function	**Counter 1—Refresh Request**
Gate	Always On
Clock In	1.193 MHz (OSC/12)
Out	Refresh Request
Function	**Counter 2—Speaker Tone**
Gate	Programmable-Port 61h
Clock In	1.193 MHz (OSC/12)
Out	Speaker

5.7.1.1 Interval Timer Address Map

Table 26 shows the I/O address map of the interval timer counters.

Table 26. Interval Timer Counters I/O Address Map

I/O Address	Register Description
040h	System Timer (Counter 0)
041h	Refresh Request (Counter 1)
042h	Speaker Tone (Counter 2)
043h	Control Word Register

Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is typically programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

Counter 1, Refresh Request Signal

This counter provides the refresh request signal and is typically programmed for Mode 2 operation. The counter negates refresh request for one counter period (833 ns) during each count cycle. The initial count value is loaded one counter period after being written to the counter I/O address. The counter initially asserts refresh request, and negates it for 1 counter period when the count value reaches 1. The counter then asserts refresh request and continues counting from the initial count value.

Counter 2, Speaker Tone

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to port 061h (see Section 4.5.1 on the NMI Status and Control Register).

5.7.2 BIOS TIMER

5.7.2.1 Overview

The SIO provides a system BIOS Timer that decrements at each edge of its 1.04 MHz clock (derived by dividing the 8.33 MHz SYSCLK by 8). Since the state of the counter is undefined at power-up, it must be programmed before it can be used. Accesses to the BIOS Timer are enabled and disabled through the BIOS Timer Base Address Register. The timer continues to count even if accesses are disabled.

A BIOS Timer Register is provided to start the timer counter by writing an initial clock value. The BIOS Timer Register can be accessed as a single 16-bit I/O port or as a 32-bit port with the upper 16-bits being "don't care" (reserved). It is up to the software to access the I/O register in the most convenient way. The I/O address of the BIOS Timer Register is software relocatable. The I/O address is determined by the value programmed into the BIOS Timer Base Address Register.

The BIOS Timer clock has a value of 1.04 MHz using an 8.33 MHz SYSCLK input (an 8 to 1 ratio will always exist between SYSCLK and the timer clock). This allows the counting of time intervals from 0 ms to approximately 65 ms. Because of the PCI clock rate, it is possible to start the counter and read the value back in less than 1 μs. The expected value of the expired interval is 0, but depending on the state of the internal clock divisor, the BIOS Timer might indicate that 1 ms has expired. Therefore, accuracy of the counter is $\pm$ 1 μs.

5.7.2.2 BIOS Timer Operations

A write operation to the BIOS Timer Register will initiate the counting sequence. The timer can be initiated by writing either the 16-bit data portion or the whole 32-bit register (upper 16 bits are "don't care"). After initialization, the BIOS timer will start decrementing until it reaches zero. Then it will stop decrementing (and hold a zero value) until initialized again.

After the timer is initialized, the current value can be read at any time and the timer can be reprogrammed (new initial value written), even before it reaches zero.

All write and read operations to the BIOS timer Register should include all 16 counter bits. Separate accesses to the individual bytes of the counter must be avoided since this can cause unexpected results (wrong count intervals).

5.8 Interrupt Controller

The SIO provides an ISA compatible interrupt controller which incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded so that 14 external and two internal interrupts are possible. The master interrupt controller provides IRQ[7:0] and the slave interrupt controller provides IRQ [15:8] (see Figure 18). The two internal interrupts are used for internal functions only and are not available to the user. IRQ2 is used to cascade the two controllers together and IRQ0 is used as a system timer interrupt and is tied to Interval Timer 1, Counter 0. The remaining 14 interrupt lines (IRQ1, IRQ3–IRQ15) are available for external system interrupts. Edge or level sense selection is programmable on a by-controller basis.

The Interrupt Controller consists of two separate 82C59 cores. Interrupt Controller 1 (CNTRL-1) and Interrupt Controller 2 (CNTRL-2) are initialized separately and can be programmed to operate in different modes. The default settings are: 80x86 Mode, Edge Sensitive (IRQ0-15) Detection, Normal EOI, Non-Buffered Mode, Special Fully Nested Mode disabled, and Cascade Mode. CNTRL-1 is connected as the Master Interrupt Controller and CNTRL-2 is connected as the Slave Interrupt Controller.

Note that IRQ13 is generated internally (as part of the coprocessor error support) by the SIO when bit 5 in the ISA Clock Divisor Register is set to a 1. When this bit is set to a 0, then the FERR#/IRQ13 signal is used as an external IRQ13 signal and has the same functionality as the normal IRQ13 signal. IRQ12/M is generated internally (as part of the mouse support) by the SIO when bit 4 in the ISA Clock Divisor Register is set to a 1. When set to a 0, the standard IRQ12 function is provided.

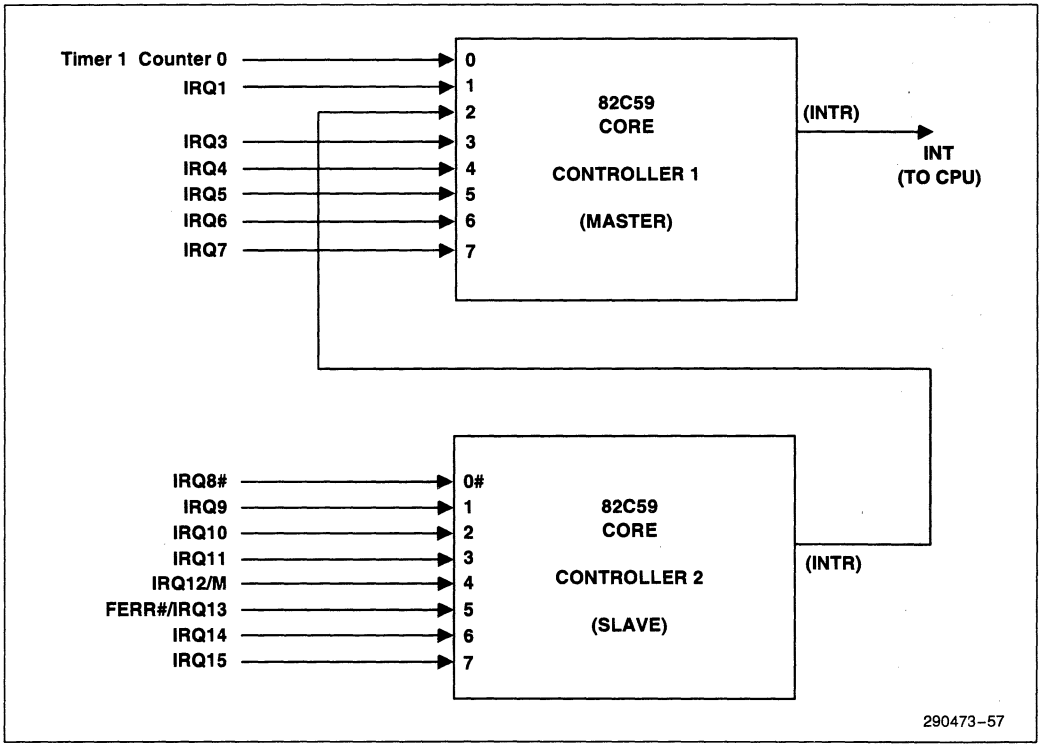


Figure 18. Block Diagram of the Interrupt Controller

Table 27 lists the I/O port address map for the interrupt registers:

Table 27. Interrupt Registers I/O Port Address Map

Interrupts	I/O Address	# of Bits	Register
IRQ[7:0]	0020h	8	CNTRL-1 Control Register
IRQ[7:0]	0021h	8	CNTRL-1 Mask Register
IRQ[15:8]	00A0h	8	CNTRL-2 Control Register
IRQ[15:8]	00A1h	8	CNTRL-2 Mask Register

IRQ0, IRQ2, (and possibly IRQ13 and IRQ12 if the "mouse" or floating point error logic is disabled in the ISA Clock Divisor Register), are connected to the interrupt controllers internally. The other interrupts are always generated internally and their typical functions are shown in Table 28:

Table 28. Typical Interrupt Functions

Priority	Label	Controller	Typical Interrupt Source
1	IRQ0	1	Interval timer 1, Counter 0 OUT
2	IRQ1	1	Keyboard
3–10	IRQ2	1	Interrupt from Controller 2
3	IRQ8#	2	Real Time Clock
4	IRQ9	2	Expansion Bus Pin B04
5	IRQ10	2	Expansion Bus Pin D03
6	IRQ11	2	Expansion Bus Pin D04
7	IRQ12/M	2	Mouse Interrupt
8	FERR#/IRQ13	2	Coprocessor Error
9	IRQ14	2	Fixed Disk Drive Controller Expansion Bus Pin D07
10	IRQ15	2	Expansion Bus Pin D06
11	IRQ3	1	Serial Port 2, Expansion Bus B25
12	IRQ4	1	Serial Port 1, Expansion Bus B24
13	IRQ5	1	Parallel Port 2, Expansion Bus B23
14	IRQ6	1	Diskette Controller, Expansion Bus B22
15	IRQ7	1	Parallel Port 1, Expansion Bus B21

5.8.1 EDGE AND LEVEL TRIGGERED MODES

There are two ELCR registers, one for each 82C59 bank. They are located at I/O ports 04D0h (for the Master Bank, IRQ[0:1,3:7]#) and 04D1h (for the Slave Bank, IRQ[8:15])#. They allow the edge and level sense selection to be made on an interrupt by interrupt basis instead of on a complete bank. Interrupts reserved for ISA use MUST be programmed for edge sensitivity (to ensure ISA compatibility). That is, IRQ (0,1,2,8#,13) must be programmed for edge sensitive operation. The LTIM bit (Edge/Level Bank select, offsets 20h, A0h) is disabled in the SIO. The default programming is equivalent to programming the LTIM bit (ICW1 bit 3) to a 0.

If an ELCR bit is equal to "0", an interrupt request will be recognized by a low to high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt.

If an ELCR bit is equal to "1", an interrupt request will be recognized by a "low" level on the corresponding IRQ input, and there is no need for an edge detection. For level triggered interrupt mode, the interrupt request signal must be removed before the EOI command is issued or the CPU interrupt must be disabled. This is necessary to prevent a second interrupt from occurring.

In both the edge and level triggered modes the IRQ inputs must remain active until after the falling edge of the first INTA#. If the IRQ input goes inactive before this time a DEFAULT IRQ7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IRQ inputs. To implement this feature the IRQ7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IRQ7 is needed for other purposes a default IRQ7 can still be detected by reading the ISR. A normal IRQ7 interrupt will set the corresponding ISR bit, a default IRQ7 won't. If a default IRQ7 routine occurs during a normal IRQ7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IRQ7 routine was previously entered. If another IRQ7 occurs it is a default.

5.8.2 REGISTER FUNCTIONALITY

For a detailed description of the Interrupt Controller register set, please see Section 4.4, Interrupt Controller Register Description.

5.8.3 NON-MASKABLE INTERRUPT (NMI)

An NMI is an interrupt requiring immediate attention and has priority over the normal interrupt lines (IRQx). The SIO indicates error conditions by generating a non-maskable interrupt.

NMI interrupts are caused by the following conditions:

1. System Errors on the PCI Bus. SERR# is driven low by a PCI resource when this error occurs.
2. Parity errors on the add-in memory boards on the ISA expansion bus. IOCHK# is driven low when this error occurs.

The NMI logic incorporates two different 8-bit registers. These registers are addressed at locations 061h and 070h. The status of Port (061h) is read by the CPU to determine which source caused the NMI. Bits set to 1 in these ports show which device requested an NMI interrupt. After the NMI interrupt routine processes the interrupt, the NMI status bits are cleared by the software. This is done by setting the corresponding enable/disable bit high. Port (070H) is the mask register for the NMI interrupts. This register can mask the NMI signal and also disable or enable all NMI sources.

The individual enable/disable bits clear the NMI detect flip-flops when disabled.

All NMI sources can be enabled or disabled by setting Port 070h bit 7 to a 0 or 1. This disable function does not clear the NMI detect flip-flops. This means, if NMI is disabled then enabled via Port 070h, then an NMI will occur when Port 070h is re-enabled if one of the NMI detect flip-flops had been previously set.

To ensure that all NMI requests are serviced, the NMI service routine software needs to incorporate a few very specific requirements. These requirements are due to the edge detect circuitry of the host microprocessor, 80386 or 80486. The software flow would need to be the following:

1. NMI is detected by the processor on the rising edge of the NMI input.
2. The processor will read the status stored in port 061h to determine what sources caused the NMI. The processor may then set to 0 the register bits controlling the sources that it has determined to be active. Between the time the processor reads

the NMI sources and sets them to a 0, an NMI may have been generated by another source. The level of NMI will then remain active. This new NMI source will not be recognized by the processor because there was no edge on NMI.

3. The processor must then disable all NMI's by setting bit 7 of port 070H to a 1 and then enable all NMI's by setting bit 7 of port 070H to a 0. This will cause the NMI output to transition low then high if there are any pending NMI sources. The CPU's NMI input logic will then register a new NMI.

Section 4.5 Control Registers, contains a detailed description of the NMI Status and Control Register (port 061h) and the NMI Enable and Real-Time Clock Address Register at port 070h.

5.9 Utility Bus Peripheral Support

The Utility Bus is a secondary bus buffered from the ISA Bus used to interface with peripheral devices that do not require a high speed interface. The buffer control for the lower 8 data signals is provided by the SIO via two control signals; UBUSOE# and UBUSTR. Figure 19 shows a block diagram of the external logic required as part of the decode and Utility Bus buffer control.

The SIO provides the address decode and three encoded chip selects to support:

1. Floppy Controller
2. Keyboard Controller
3. Real Time Clock
4. IDE Drive
5. 2 Serial Ports (COM1 and COM2)
6. 1 Parallel Port (LPT1, 2, or 3)
7. BIOS Memory
8. Configuration Memory (8 Kbyte I/O Mapped)

The SIO also supports the following functions:

1. Floppy DSKCHG Function
2. Port 92 Function (Alternate A20 and Alternate Reset)
3. Coprocessor Logic (FERR# and IGNNE# Function)

The binary code formed by the three Encoded Chip Selects determines which Utility Bus device is selected. The SIO also provides an Encoded Chip Select Enable signal (ECSEN#) that is used to select between the two external decoders. A zero selects decoder 1 and a one selects decoder 2. The table below shows the address decode for each of the Utility Bus devices.

Table 29. NMI Source Enable/Disable and Status Port Bits

NMI Source	I/O Port Bit for Status Reads	I/O Port Bit for Enable/Disable
IOCHK#	Port 061h, Bit 6	Port 061h, Bit 3
SERR#	Port 061h, Bit 7	Port 061h, Bit 2

Table 30. Encoded Chip Select Summary Table

ECSADDR2	ECSADDR1	ECSADDR0	ECSEN#	Address Decoded	External Chip Select	Note	Cycle Type
Decoder 1							
0	0	0	0	70h, 72h, 74, 76h	RTCALE#		I/O W
0	0	1	0	71h, 73h, 75h, 77h	RTCCS#		I/O R/W
0	1	0	0	60h, 62h, 64h, 66h	KEYBRDCS#		I/O R/W
0	1	1	0	000E0000h–000FFFFFh FFFE0000h–FFFFFFFFh FFF80000h–FFFDFFFFh	BIOSCS#	1	MEM R/W
1	0	0	0	3F0h–3F7h (primary) 370h–377h (secondary)	FLOPPYCS#	2	I/O R/W
1	0	1	0	1F0h–1F7h (primary) 170h–177h (secondary)	IDECS0#	2	I/O R/W
1	1	0	0	3F6h–3F7h (primary) 376h–377h (secondary)	IDECS1#	2	I/O R/W
1	1	1	0	Reserved			
Decoder 2							
0	0	0	1	Reserved			
0	0	1	1	0C00h	CPAGECS#	3	I/O R/W
0	1	0	1	0800h–08FFh	CFIGMEMCS#	3	I/O R/W
0	1	1	1	3F8h–3FFh (COM1) -or- 2F8h–37Fh (COM2)	COMACS#	4	I/O R/W
1	0	0	1	3F8h–3FFh (COM1) -or- 2F8h–37Fh (COM2)	COMBCS#	4	I/O R/W
1	0	1	1	3BCh–3BFh (LPT1) 378h–37Fh (LPT2) 278h–27Fh (LPT3)	LPTCS#	5	I/O R/W
1	1	0	1	Reserved			
1	1	1	1	Idle State			

NOTES:
1. The encoded chip select signals for BIOSCS# will always be generated for accesses to the upper 64 KB at the top of 1 MByte (F0000h–FFFFFh) and its aliases at the top of the 4 GB and 4 GB-1 MByte. Access to the lower 64 KByte (E0000h–EFFFFh) and its aliases at the top of 4 GB and 4GB–1MB can be enabled or disabled through the SIO. An additional 384 KB of BIOS memory at the top of 4 GB (FFFD0000h–FFFDFFFFh) can be enabled for BIOS use.
2. The primary and secondary locations are programmable through the SIO. Only one location range can be enabled at any one time. The floppy and IDE share the same enable and disable bit (i.e. if the floppy is set for primary, the IDE is also set for primary).
3. These signals can be used to select additional configuration RAM.
4. COM1 and COM2 address ranges can be programmed for either port A (COMACS#) or port B (COMBCS#).
5. Only one address range (LPT1, LPT2, or LPT3) can be programmed at any one time.

Port 92h Function

The SIO integrates the Port 92h Register. This register provides the alternate reset (ALTRST) and alternate A20 (ALT_A20) functions. Figure 19 shows how these functions are tied into the system.

DSKCHG Function

DSKCHG is tied directly to the DSKCHG signal of the floppy controller. This signal is inverted and driven onto system data line 7 (SD7) during I/O read cycles to floppy address locations 3F7h (primary) or 377 (secondary) as indicated by Table 31.

Table 31. DSKCHG Summary Table

FLOPPYCS# Decode	IDECSx# Decode	State of SD7 (Output)	State of UBUSOE#
Enabled	Enabled	Tri-stated	Enabled
Enabled	Disabled	Driven via DSKCHG	Disabled
Disabled	Enabled	Tri-stated	Enabled(1)
Disabled	Disabled	Tri-stated	Disabled

NOTE:
1. For this mode to be supported, extra logic is required to disable the U-bus transceiver for accesses to 3F7/377. This is necessary because of potential contention between the Utility bus buffer and a floppy on the ISA Bus driving the system bus at the same time during shared I/O accesses.

Coprocessor Error Support

If bit 5 in the ISA Clock Divisor Register is set to a one, the SIO will support coprocessor error reporting through the FERR#/IRQ13 signal.

FERR# is tied directly to the Coprocessor error signal of the CPU. If FERR# is driven active in this mode (coprocessor error detected by the CPU), an internal IRQ13 is generated and the INT output from the SIO is driven active. When a write to I/O location F0h is detected, the SIO negates IRQ13 and drives IGNNE# active. IGNNE# remains active until FERR# is driven inactive. Note that IGNNE# is not generated unless FERR# is active.

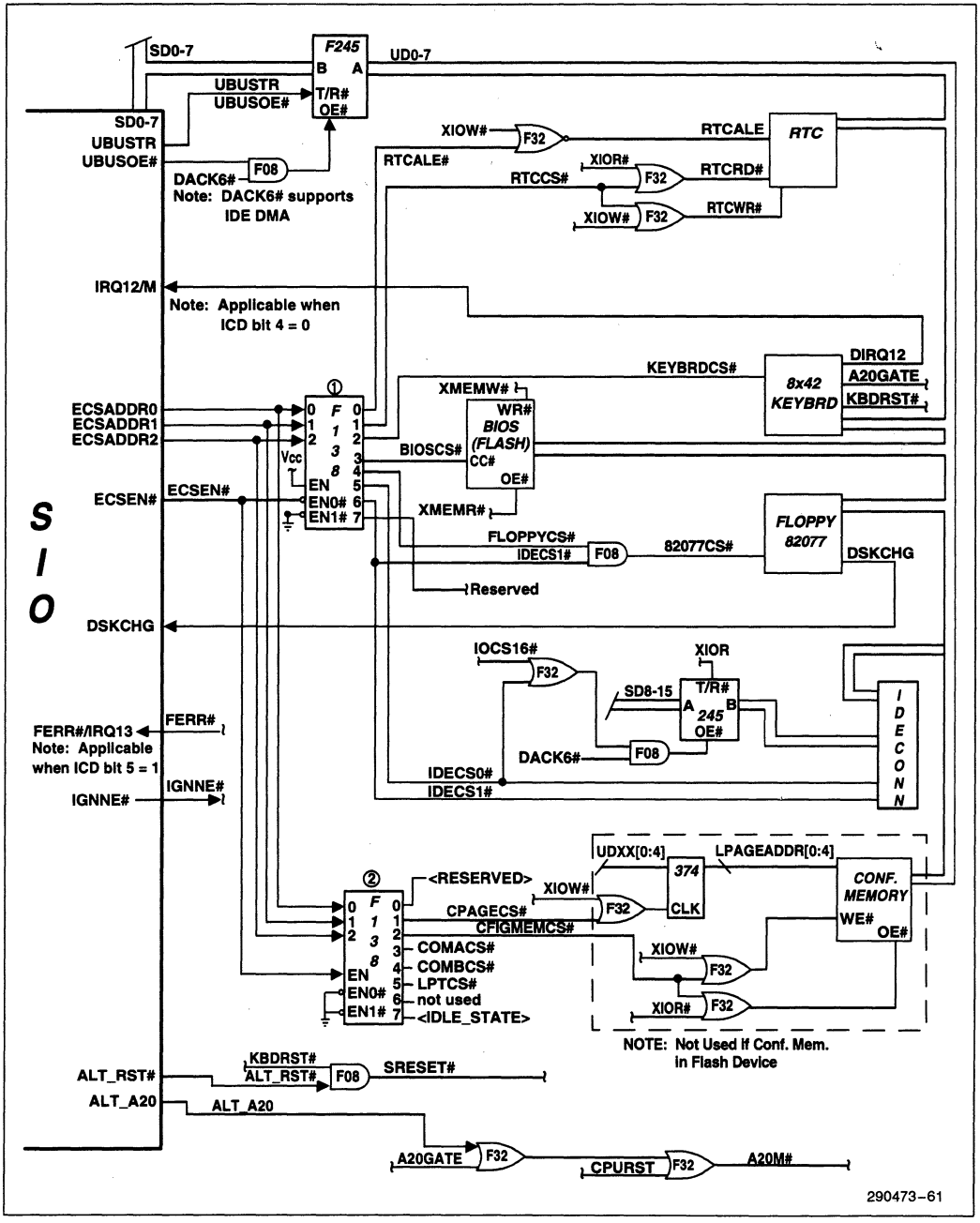


Figure 19. Utility Bus External Support Logic

Utility Bus accesses by the SIO, by an ISA master, and by the DMA is shown in Figure 20 and Figure 21. UBUSOE# and UBUSTR are driven differently for DMA cycles as shown in Figure 21.

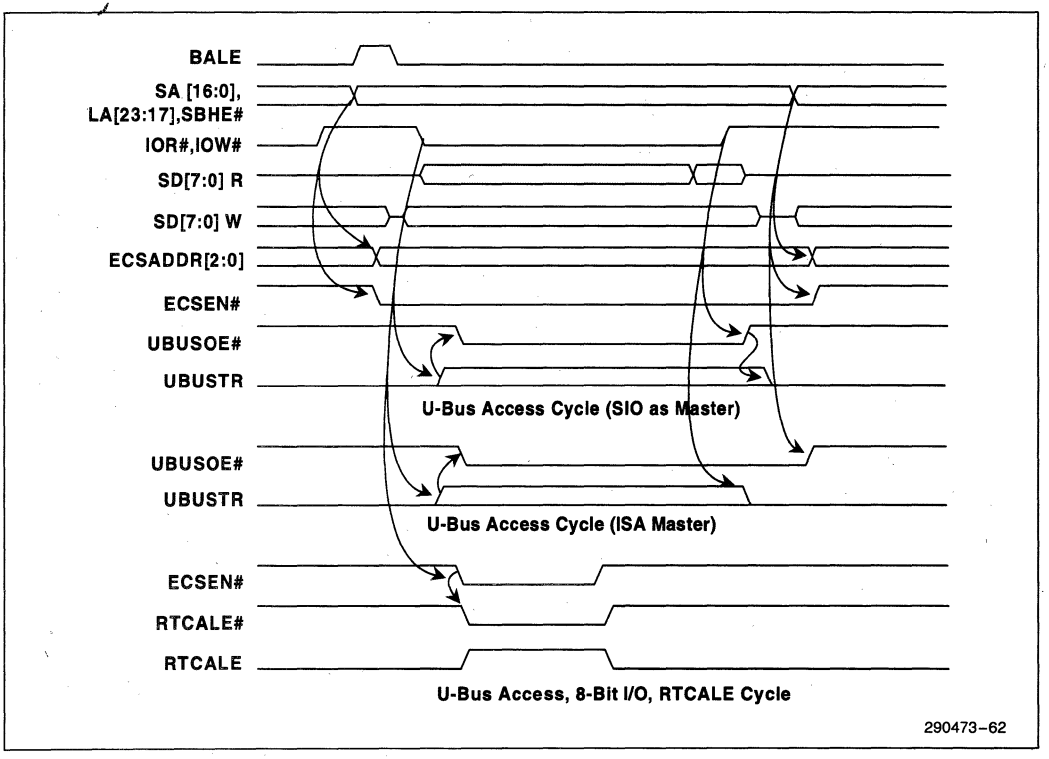


Figure 20. Utility Bus Access (SIO and ISA Master)

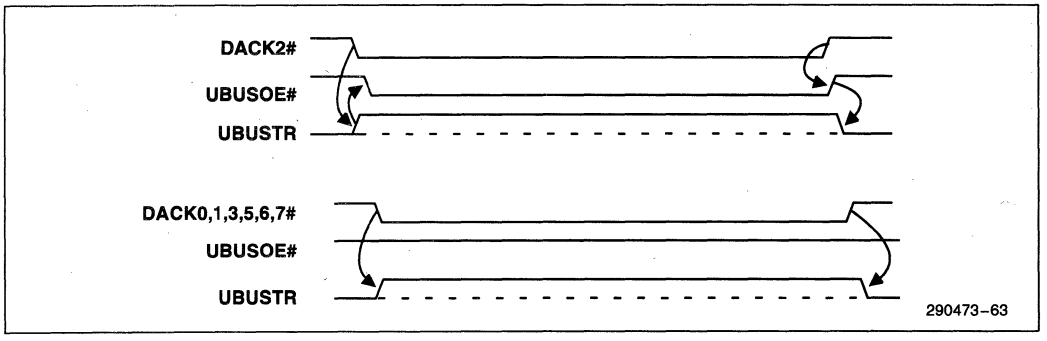


Figure 21. Utility Bus Access (DMA)

5.10 Power Management

The SIO's power management architecture is based around three core functions:

1. SMM (System Management Mode)
2. Clock Throttling
3. APM (Advanced Power Management Interface)

SMM is a mode during which an S Series Processor is executing SMM code from a secure memory space (SMRAM). SMM is invoked through the assertion of an SMI (System Management Interrupt). Physically, this is signaled over the SMI# pin. SMI's are triggered by various hardware and software events. SMRAM is used to store the SMM code which is really the SMI interrupt handler routine.

Clock Throttling will be used to reduce the power consumption of the CPU. STPCLK# is the physical signal used to control the CPU's clock.

APM creates an interface to allow the Operating System to communicate with the SMM code.

Figure 22 shows how the power management signals are connected in a Saturn based system with an S-series CPU.

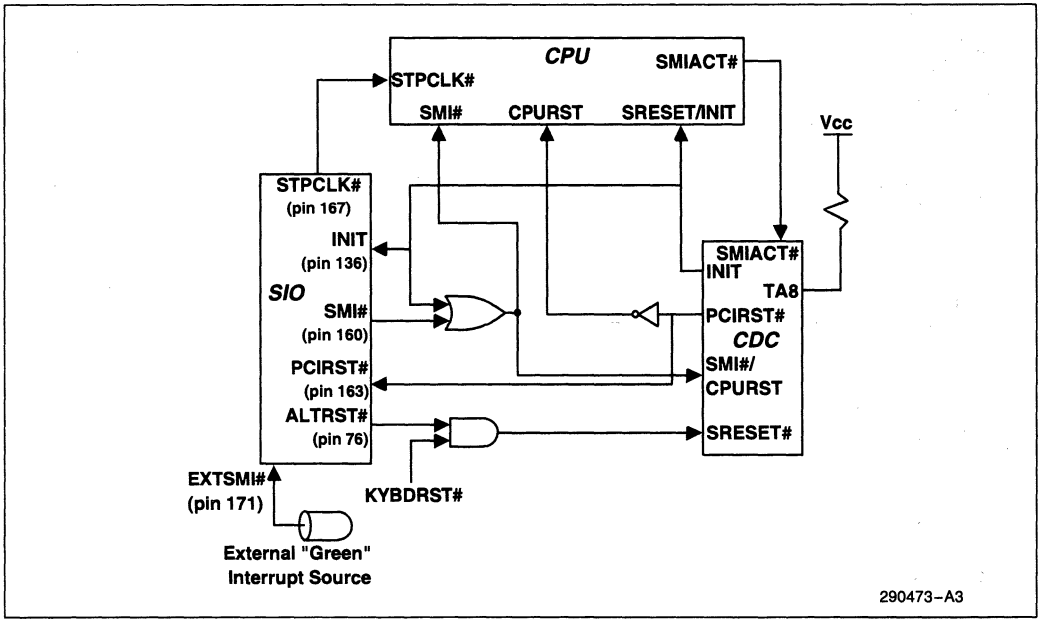


Figure 22. Power Management

6.0 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings*

Case Temperature under Bias . . . −65°C to +110°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltages
with Respect to Ground . . . −0.5V to V_{CC} + 0.5V
Voltage On Any Pin . . . . . −0.5V to V_{CC} + 0.5V

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

7.0 MECHANICAL SPECIFICATIONS

7.1 Package Diagram

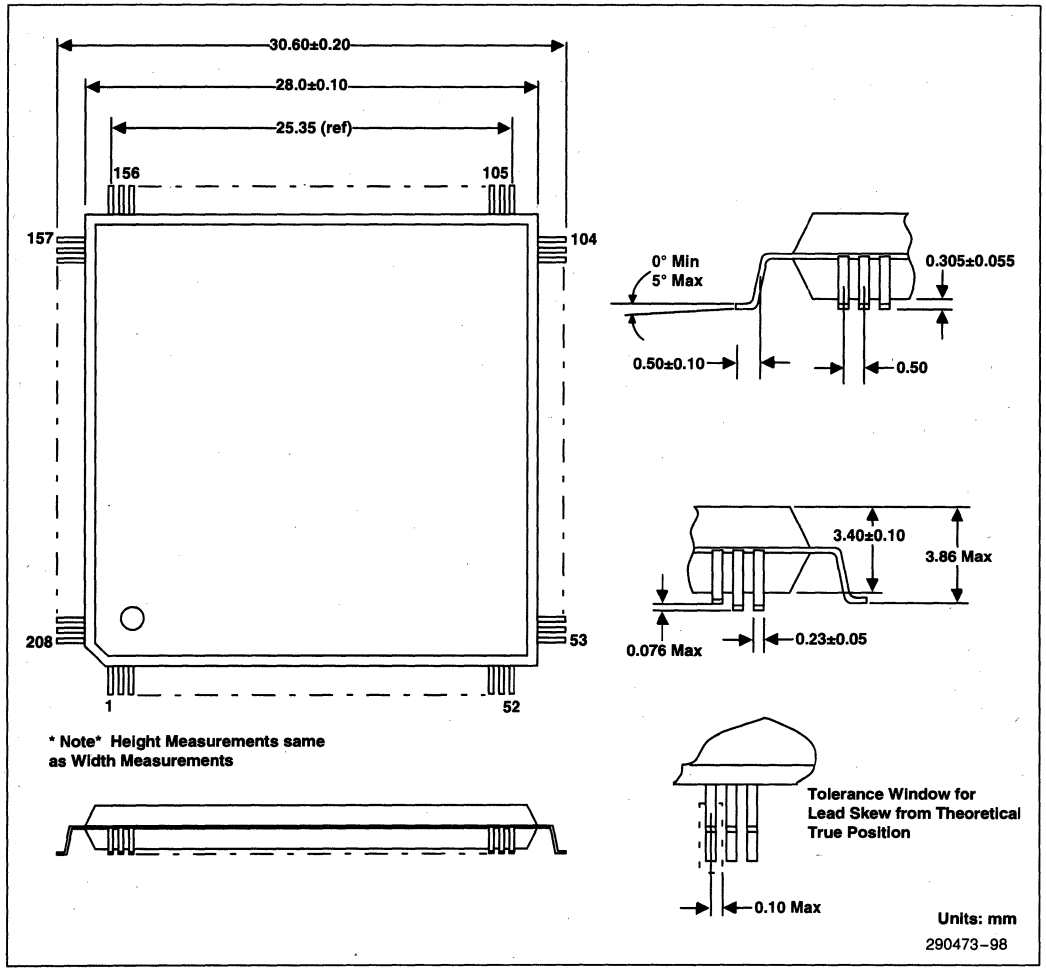


Figure 23. 208-Pin Quad Flat Pack (QFP) Package Dimensions

7.2 Thermal Specifications

Table 32. 82378 QFP Package Thermal Characteristics

Thermal Resistance-°C/Watt			
	Air Flow Rate (Ft./Min)		
Parameter	**0**	**200**	**400**
$\theta_{Junction\ to\ Case}$	6.6	6.6	6.6
$\theta_{Case\ to\ Ambient}$	36.6	27.4	24

8.0 TESTABILITY

The TEST and TESTO pins are used to test the SIO. During normal operations, the TEST pin must be grounded. The test output TESTO may be left as a no-connect (NC).

8.1 Global Tri-State

The TEST pin and IRQ3 are used to provide a high-impedance tri-state test mode. When the following input combination occurs, all outputs and bi-directional pins are tri-stated, with the exception of TESTO:

TEST = "1"
IRQ3 = "1"

The SIO must be reset after the bi-directional and output pins have been tri-stated in this manner.

8.2 NAND Tree

A NAND Tree is provided primarily for V_{IL}/V_{IH} testing. The NAND Tree is also useful for ATE at board level testing. The NAND Tree allows the tester to test the solder connections for each individual signal pin.

The TEST pin, along with IRQ5 or IRQ6, activates the NAND Tree. All bi-directional pins, and certain pure output pins using bi-directional buffers for performance reasons, are tri-stated when the following input combinations occur:

TEST = "1"
IRQ5 = "1"
- or -
TEST = "1"
IRQ6 = "0"

In the 82378, the output pulse train is observed at the TESTO test output. Pure output pins are not included directly in the NAND Tree. As noted in Section 8.3, each output can be expected to toggle after the corresponding node noted next to the pin name toggles from a "1" to a "0".

The sequence of the ATE test is as follows:

1. Drive TEST and IRQ5 high or TEST high and IRQ6 low.
2. Drive each input and bi-directional pin noted in Section 8.3 high.
3. Starting with the pin farthest from TESTO (SA8), individually drive each pin low. Expect TESTO to toggle with each pin. Expect each pure output noted in Section 8.3 to toggle after each corresponding input pin has been driven low.
4. Turn off tester drivers before driving TEST low.
5. Reset the SIO prior to proceeding with further testing.

8.3 NAND Tree Cell Order

Table 33. NAND Tree Cell Order

Tree Output #	Pin #	Pin Name	Notes
	14	IRQ4	Reserved
	21	TESTO	Test Mode Output
1	11	IRQ5	Cell Closest to TESTO
2	10	SA9	
3	9	IRQ6	
4	8	SA10	
5	7	IRQ7	
6	6	SA11	
7	5	SA12	
8	4	REFRESH#	
9	3	SA13	
10	207	SA14	
11	206	MASTER#	
12	205	SA15	
13	204	MEMW#	
14	203	MEMR#	
15	202	SA16	
16	201	SA17	
17	200	IOR#	
18	199	SA18	
19	198	IOW#	
20	197	SA19	
21	196	SMEMR#	
22	193	AEN	
23	192	SMEMW#	
24	191	IOCHRDY	
25	190	SD0	
26	189	SD1	

Table 33. NAND Tree Cell Order (Continued)

Tree Output #	Pin #	Pin Name	Notes
27	188	ZEROWS#	
28	187	SD2	
29	186	SD3	
30	185	SD4	
31	184	IRQ9	
32	180	SD5	
33	179	SD6	
34	178	SD7	
35	177	RSTDRV	
36	176	IOCHK#	
	175	ECSADDR0	NAND Tree Output of Tree Cell 28
	174	ECSADDR1	NAND Tree Output of Tree Cell 29
	173	ECSADDR2	NAND Tree Output of Tree Cell 30
37	172	IRQ8#	
38	171	EXTSMI#	
	170	ECSEN#	NAND Tree Output of Tree Cell 32
	169	TEST	PI = > VCC, TEST must be '1'
39	168	IRQ1	
	167	STPCLK#	
40	166	SYSCLK	
	165	UBUSTR	NAND Tree Output of Tree Cell 33
	164	UBUSOE#	NAND Tree Output of Tree Cell 34
41	163	PCIRST#	
42	161	DSKCHG	
	160	SMI#	
43	159	AD0	
44	155	AD1	
45	154	AD2	
46	153	AD3	

Table 33. NAND Tree Cell Order (Continued)

Tree Output #	Pin #	Pin Name	Notes
47	152	AD4	
48	151	AD5	
49	150	AD6	
50	149	AD7	
51	148	AD8	
52	147	C/BE0#	
53	146	AD9	
54	143	AD10	
55	142	AD11	
56	141	AD12	
57	140	AD13	
58	139	AD14	
59	138	AD15	
60	137	C/BE1#	
61	136	INIT	
62	135	PAR	
63	134	SERR#	
64	133	LOCK#	
65	132	STOP#	
66	128	DEVSEL#	
67	127	TRDY#	
68	126	IRDY#	
69	125	FRAME#	
70	124	C/BE2#	
71	123	AD16	
72	122	AD17	
73	121	AD18	
74	120	AD19	

Table 33. NAND Tree Cell Order (Continued)

Tree Output #	Pin #	Pin Name	Notes
75	119	AD20	
76	118	AD21	
77	115	AD22	
78	114	AD23	
79	113	C/BE3#	
80	112	AD24	
81	111	AD25	
82	110	AD26	
83	109	AD27	
84	108	AD28	
85	107	AD29	
86	106	AD30	
87	102	AD31	
88	101	IDSEL	
89	100	REQ3#	
90	98	REQ1#	
91	97	REQ2#	
92	96	CPUREQ#	
	95	CPUGNT#	NAND Tree Output of Tree Cell 93
	94	GNT1#	NAND Tree Output of Tree Cell 95
93	93	REQ0#	
	92	GNT0#	NAND Tree Output of Tree Cell 100
94	90	PCICLK	
	89	FLSHREQ#	NAND Tree Output of Tree Cell 102
95	88	MEMACK#	
	87	MEMREQ#	NAND Tree Output of Tree Cell 103

Table 33. NAND Tree Cell Order (Continued)

Tree Output #	Pin #	Pin Name	Notes
	86	MEMCS#	NAND Tree Output of Tree Cell 104
	85	ALT_A20	NAND Tree Output of Tree Cell 105
96	84	PIRQ[3]#	
97	83	PIRQ[2]#	
98	82	PIRQ[1]#	
99	81	PIRQ[0]#	
100	80	OSC	
	76	ALT_RST#	NAND Tree Output of Tree Cell 23
	75	INT	NAND Tree Output of Tree Cell 24
	74	NMI	NAND Tree Output of Tree Cell 25
101	73	SPKR	
	72	IGNNE#	NAND Tree Output of Tree Cell 26
102	71	FERR#	
103	70	SD15	
104	69	SD14	
105	68	SD13	
106	67	SD12	
107	65	DREQ7	
108	64	SD11	
109	63	DACK7#	
110	62	SD10	
111	61	DREQ6	
112	60	SD9	
113	59	DACK6#	
114	58	DREQ3	
115	57	DREQ2	
116	56	DREQ1	
117	55	SD8	
118	51	DREQ5	

Table 33. NAND Tree Cell Order (Continued)

Tree Output #	Pin #	Pin Name	Notes
119	50	DACK5#	
120	49	DACK3#	
121	48	DACK1#	
122	47	DREQ0	
123	46	LA17	
124	45	DACK0#	
125	44	LA18	
126	43	IRQ14	
127	42	LA19	
128	41	IRQ15	
129	40	LA20	
130	39	IRQ12/M	
131	38	LA21	
132	37	IRQ11	
133	36	LA22	
134	35	IRQ10	
135	34	LA23	
136	33	IOCS16#	
137	32	SBHE#	
138	31	MEMCS16#	
139	30	SA0	
140	29	SA1	
141	28	SA2	
142	24	SA3	
143	23	BALE	
144	22	SA4	
145	20	EOP	
146	19	SA5	

Table 33. NAND Tree Cell Order (Continued)

Tree Output #	Pin #	Pin Name	Notes
147	18	DACK2#	
148	17	SA6	
149	16	IRQ3	Output signals will transition from high-impedance state to driving state after this pin is driven low.
150	15	SA7	
151	13	SA8	Cell furthest from TESTO Start of NAND Tree

8.4 NAND Tree Diagram

Figure 24 shows the NAND Tree Diagram.

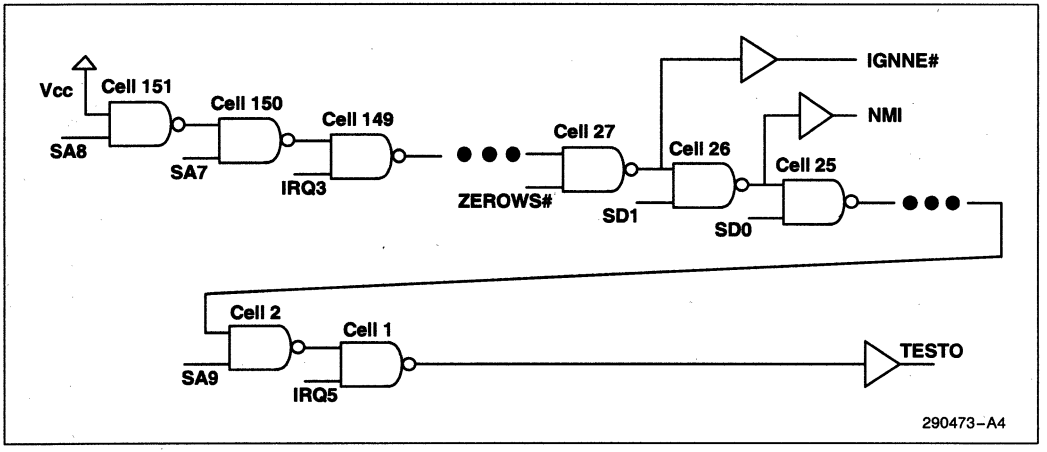


Figure 24. NAND Tree Diagram for 82378

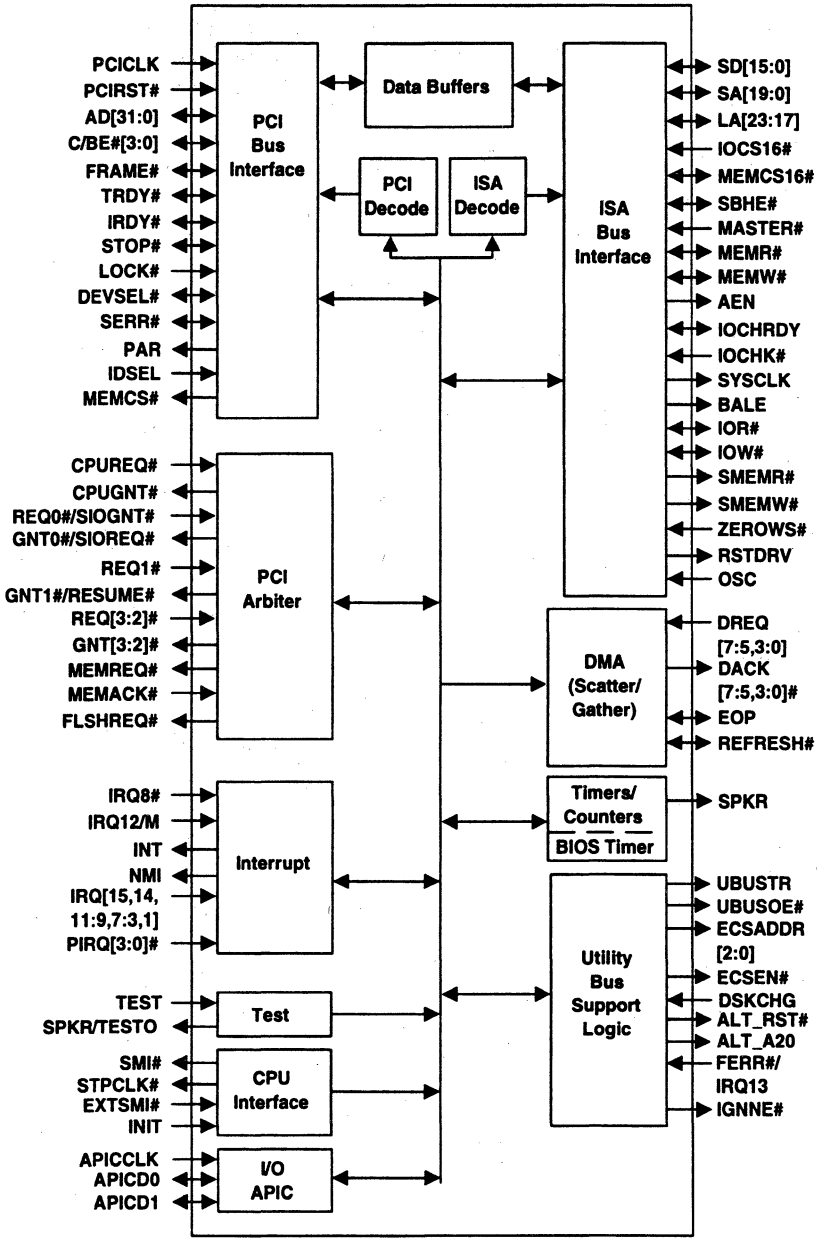
82379AB SYSTEM I/O-APIC (SIO.A)

- **Provides the Bridge between the PCI Bus and ISA Bus**
- **100% PCI and ISA Compatible**
  - **— PCI and ISA Master/Slave Interface**
  - **— Directly Drives 10 PCI Loads and 6 ISA Slots**
  - **— Supports PCI at 25 MHz and 33 MHz**
  - **— Supports ISA from 6 MHz to 8.33 MHz**
- **Enhanced DMA Functions**
  - **— Compatible DMA Transfers**
  - **— 27-Bit Addressability**
  - **— Seven Independently Programmable Channels**
  - **— Functionality of Two 82C37A DMA Controllers**
- **Integrated Data Buffers to Improve Performance**
  - **— 8-Byte DMA/ISA Master Line Buffer**
  - **— 32-Bit Posted Memory Write Buffer to ISA**
- **Integrated 16-Bit BIOS Timer**
- **Non-Maskable Interrupts (NMI)**
  - **— PCI System Errors**
  - **— ISA Parity Errors**
- **Four Dedicated PCI Interrupts**
  - **— Level Sensitive**
  - **— Can be Mapped to Any Unused Interrupt**
- **Arbitration for ISA Devices**
  - **— ISA Masters**
  - **— DMA and Refresh**
- **Arbitration for PCI Devices**
  - **— Six PCI Masters Are Supported**
  - **— Fixed, Rotating, or a Combination of the Two**
- **Utility Bus (X-Bus) Peripheral Support**
  - **— Provides Chip Select Decode**
  - **— Controls Lower X-Bus Data Byte Transceiver**
- **Integrates the Functionality of One 82C54 Timer**
  - **— System Timer**
  - **— Refresh Request**
  - **— Speaker Tone Output**
- **Integrates the Functionality of Two 82C59 Interrupt Controllers**
  - **— 14 Interrupts Supported**
  - **— Edge/Level Selectable Interrupts: Each Interrupt Individually Programmable**
- **Complete Support for SL Enhanced Intel486™ CPU's**
  - **— SMI# Generation Based on System Hardware Events**
  - **— STPCLK# Generation to Power Down the CPU**
- **Integrated I/O Advanced Programmable Interrupt Controller (APIC)**

The 82379AB System I/O-APIC (SIO.A) component provides the bridge between the PCI bus and the ISA expansion bus. The 82379AB also integrates many of the common I/O functions found in today's ISA based PC systems. The 82379AB incorporates the logic for a PCI interface (master and slave), ISA interface (master and slave), enhanced seven channel DMA controller that supports data buffers to isolate the PCI bus from the ISA bus and to enhance performance, PCI and ISA arbitration, 14 level interrupt controller, a 16-bit BIOS timer, three programmable timer/counters, and Non-Maskable Interrupt (NMI) Control Logic. The 82379AB also provides decode for peripheral devices such as the Flash BIOS, Real Time Clock, Keyboard/Mouse Controller, Floppy Controller, two Serial Ports, one Parallel Port, and IDE Hard Disk Drive. The 82379AB supports several Advanced Power Management features such as SMI# Interrupt. The 82379AB also supports a total of 6 PCI Masters, and can support up to 4 PCI Interrupts. The 82379AB incorporates an Advanced Programmable Interrupt Controller (APIC) that communicates with the processor via a dedicated two data bit bus.

The complete document for this product can be ordered by calling 1-800-548-4725.

December 1994
Order Number: 290520-001



290520-1

82379AB Component Block Diagram

82091AA
ADVANCED INTEGRATED PERIPHERAL (AIP)

- **Single-Chip PC Compatible I/O Solution for Notebook and Desktop Platforms:**
  - 82078 Floppy Disk Controller Core
  - Two 16550 Compatible UARTs
  - One Multi-Function Parallel Port
  - IDE Interface
  - Integrated Back Power Protection
  - Integrated Game Port Chip Select
  - 5V or 3.3V Supply Operation with 5V Tolerant Drive Interface
  - Full Power Management Support
  - Supports Type F DMA Transfers for Faster I/O Performance
  - No Wait-State Host I/O Interface
  - Programmable Interrupt Interfaces
  - Single Crystal/Oscillator Clock (24 MHz)
  - Software Detectable Device ID
  - Comprehensive Powerup Configuration
- **The 82091AA is 100 Percent Compatible with EISA, ISA and AT**
- **Host Interface Features**
  - 8-Bit Zero Wait-State ISA Bus Interface
  - DMA with Type F Transfers
  - Five Programmable ISA Interrupt Lines
  - Internal Address Decoder
- **Parallel Port Features**
  - All IEEE Standard 1284 Protocols Supported (Compatibility, Nibble, Byte, EPP, and ECP)
  - Peak Bi-Directional Transfer Rate of 2 MB/sec
  - Provides Interface for Low-Cost Engineless Laser Printer
  - 16-Byte FIFO for ECP
  - Interface Backpower Protection
- **Floppy Disk Controller Features**
  - 100 Percent Software Compatible with Industry Standard 82077SL and 82078
  - Integrated Analog Data Separator 250K, 300K, 500K, and 1 MBits/sec
  - Programmable Powerdown Command
  - Auto Powerdown and Wakeup Modes
  - Integrated Tape Drive Support
  - Perpendicular Recording Support for 4 MB Drives
  - Programmable Write Pre-Compensation Delays
  - 256 Track Direct Address, Unlimited Track Support
  - 16-Byte FIFO
  - Supports 2 or 4 Drives
- **16550 Compatible UART Features**
  - Two Independent Serial Ports
  - Software Compatible with 8250 and 16450 UARTs
  - 16-Byte FIFO per Serial Port
  - Two UART Clock Sources, Supports MIDI Baud Rate
- **IDE Interface Features**
  - Generates Chip Selects for IDE Drives
  - Integrated Buffer Control Logic
  - Dual IDE Interface Support
- **Power Management Features**
  - Transparent to Operating Systems and Applications Programs
  - Independent Power Control for Each Integrated Device
- **100-Pin QFP Package**
  (See Packaging Spec. 240800)

1

The 82091AA Advanced Integrated Peripheral (AIP) is an integrated I/O solution containing a floppy disk controller, 2 serial ports, a multi-function parallel port, an IDE interface, and a game port on a single chip. The integration of these I/O devices results in a minimization of form factor, cost and power consumption. The

Refer to Chapter 2 for the complete document on this product.

December 1994
Order Number: 290486-003

floppy disk controller is the 82078 core. The serial ports are 16550 compatible. The parallel port supports all of the IEEE Standard 1284 protocols (ECP, EPP, Byte, Compatibility, and Nibble). The IDE interface supports 8- or 16-bit programmed I/O and 16-bit DMA. The Host Interface is an 8-bit ISA interface optimized for type "F" DMA and no wait-state I/O accesses. Improved throughput and performance, the 82091AA contains six 16-byte FIFOs–two for each serial port, one for the parallel port, and one for the floppy disk controller. The 82091AA also includes power management and 3.3V capability for power sensitive applications such as notebooks. The 82091AA supports both motherboard and add-in card configurations.

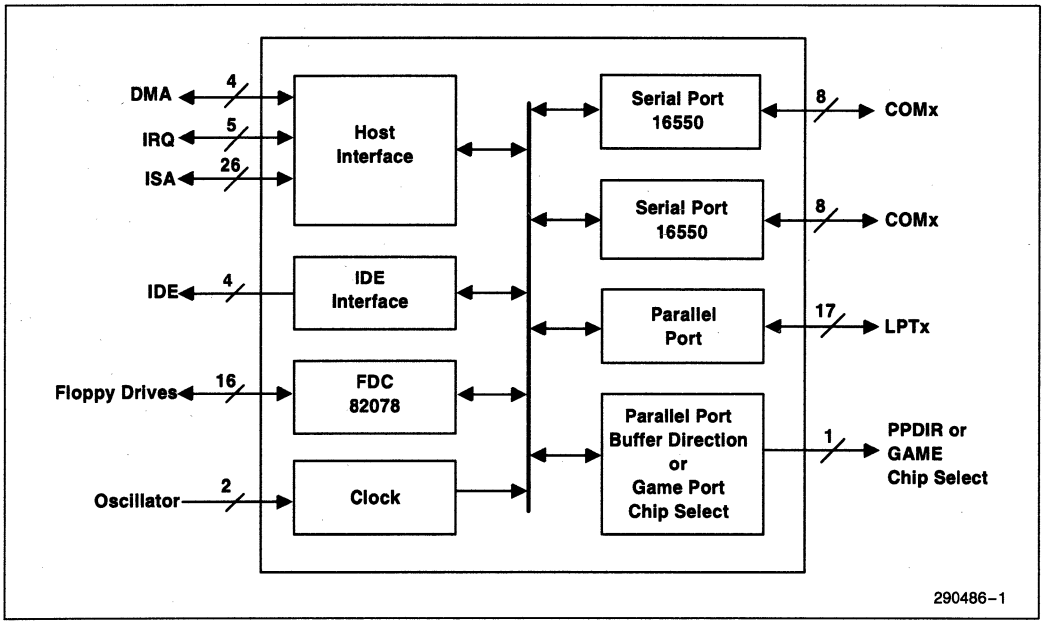


Figure 1. 82091AA Advanced Integrated Peripheral Block Diagram

UPI-C42/UPI-L42
UNIVERSAL PERIPHERAL INTERFACE
CHMOS 8-BIT SLAVE MICROCONTROLLER

- **Pin, Software and Architecturally Compatible with all UPI-41 and UPI-42 Products**
- **Low Voltage Operation with the UPI-L42**
  — Full 3.3V Support
- **Integrated Auto A20 Gate Support**
- **Suspend Power Down Mode**
- **Security Bit Code Protection Support**
- **8-Bit CPU plus ROM/OTP EPROM, RAM, I/O, Timer/Counter and Clock in a Single Package**
- **4096 x 8 ROM/OTP, 256 x 8 RAM 8-Bit Timer/Counter, 18 Programmable I/O Pins**
- **DMA, Interrupt, or Polled Operation Supported**
- **One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface**
- **Fully Compatible with all Intel and Most Other Microprocessor Families**
- **Interchangeable ROM and OTP EPROM Versions**
- **Expandable I/O**
- **Sync Mode Available**
- **Over 90 Instructions: 70% Single Byte**
- **Quick Pulse Programming Algorithm**
  — Fast OTP Programming
- **Available in 40-Lead Plastic, 44-Lead Plastic Leaded Chip Carrier, and 44-Lead Quad Flat Pack Packages**
  (See Packaging Spec., Order #240800, Package Type P, N, and S)

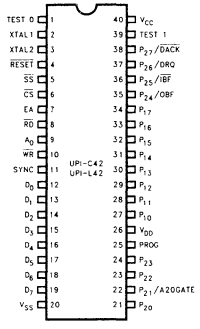
1

The UPI-C42 is an enhanced CHMOS version of the industry standard Intel UPI-42 family. It is fabricated on Intel's CHMOS III-E process. The UPI-C42 is pin, software, and architecturally compatible with the NMOS UPI family. The UPI-C42 has all of the same features of the NMOS family plus a larger user programmable memory array (4K), integrated auto A20 gate support, and lower power consumption inherent to a CHMOS product.

The UPI-L42 offers the same functionality and socket compatibility as the UPI-C42 as well as providing low voltage 3.3V operation.

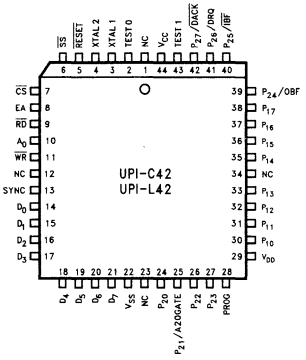
The UPI-C42 is essentially a "slave" microcontroller, or a microcontroller with a slave interface included on the chip. Interface registers are included to enable the UPI device to function as a slave peripheral controller in the MCS Modules and iAPX family, as well as other 8-, 16-, and 32-bit systems.

To allow full user flexibility, the program memory is available in ROM and One-Time Programmable EPROM (OTP).



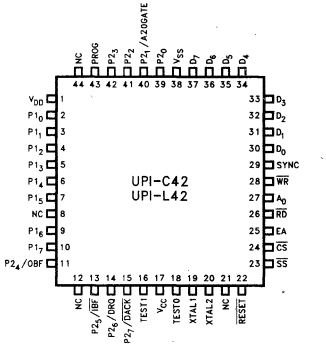
290414-1

Figure 1. DIP Pin Configuration



290414-2

Figure 2. PLCC Pin Configuration



290414-3

Figure 3. QFP Pin Configuration

Refer to Chapter 4 for the complete document on this product.

October 1994
Order Number: 290414-003

PRELIMINARY

82350
EISA Chip Set

January 1994

Order Number: 290220-004

82350 EISA CHIP SET

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1

EISA TERMINOLOGY

ISA BUS— The bus used in Industry Standard Architecture compatible computers. In the context of an EISA system, it refers to the ISA subset of the EISA bus.

EISA BUS— Extended ISA bus, a superset of the ISA bus. It includes all ISA bus features, along with extensions to enhance performance and capabilities.

HOST CPU— The main system processor, located on a separate Host Bus. This uses the EBC and other system board facilities to interface to the EISA bus.

CPU CYCLE— 386 CPU and/or the 82385 subsystem, or 80486 CPU is the master running the cycle.

EISA MASTER— A 16-bit or 32-bit bus master that uses the EISA signal set to generate memory or I/O cycles. The bus controller will convert the EISA control signals to ISA signals, when necessary.

ISA MASTER—A 16-bit bus master that uses the ISA subset of the EISA bus for generation of memory or I/O cycles. This device must understand 8-bit or 16-bit ISA slaves, and route data to the appropriate byte lanes. It is not required to handle any of the signals associated with the extended portion of the EISA bus.

EISA SLAVE— An 8-bit, 16-bit or 32-bit memory or I/O slave device that uses the extended signal set of the EISA bus to accept cycles from various masters. It returns information about its type and width using extended and ISA signals.

ISA SLAVE— A 16-bit or 8-bit slave that uses the ISA subset of the EISA bus to accept cycles from various masters. It returns ISA signals to indicate its type and width.

DMA SLAVE— An I/O device that uses the DMA signals (DREQ, DACK#) of the system board ISP to perform a direct memory access.

ISACMD— The ISA command signals (IORC#, IOWC#, MRDC#, MWTC#)

ASSEMBLY/DISASSEMBLY— This occurs when the master/slave data bus size are mismatched. The EBC runs multiple cycles to route bytes to the appropriate byte lanes (byte swapping). For example, if the 32-bit CPU is accessing an 8-bit slave, the EBC will need to run four cycles to the 8-bit slave and route the bytes to appropriate byte lanes

CYCLE TRANSLATION— This is performed by the EBC when the master and slave are on different busses (Host/EISA/ISA). The EBC will translate the master protocol to the slave protocol (Host master accessing EISA slave).

EISA System Introduction

Extended Industry Standard Architecture (EISA) is a high performance 32-bit architecture based upon the Industry Standard Architecture (ISA) (PC AT*). The wide acceptance of the 32-bit 386 microprocessor family has led to this interest in extending ISA to 32-bits. EISA's advanced capabilities and 32-bit architecture can unleash the full potential of the 386 and i486™ CPUs.

The EISA consortium has defined the EISA bus in response to the demand for a 32-bit high performance ISA compatible system. The open industry standard allows for industry wide participation, compatibility, and differentiation.

EISA brings advances in performance and convenience to the user. It provides 32-bit memory addressing and data transfers for CPU, DMA and bus masters allowing 33 Mbyte/second transfer rate for DMA and bus masters on the EISA bus. EISA provides a specification for auto-configuration of add-in cards that will eliminate the need for jumpers and switches on EISA cards. Interrupts are shareable and programmable. Figure 1 and 2 show the types of busses in an EISA system. A new bus-arbitration makes possible a new generation of intelligent bus master add-in cards that bring advanced applications to PCs.

Since the EISA system is 100% compatible with the ISA 8-bit and 16-bit expansion boards and software, ISA cards can be plugged into the EISA connector slots. The EISA slots can be defined as ISA or EISA for ease of compatibility during configuration. The EISA connector is a superset of the ISA connector maintaining full compatibility with ISA expansion cards and software. Simultaneous use of EISA and ISA add-in boards is available with automatic system and expansion board configuration.

82350 EISA Chip Set Highlights

The Intel 82350 EISA chip set is the industry's first 100% EISA/ISA compatible chip set. The 82350

Intel486 is a trademark of Intel Corporation.

*PC AT is a trademark of International Business Machine Corporation.

EISA chip set supports the 33 MHz and 25 MHz 386 CPU or i486 CPU, 82385 Cache Controller, and optional 80387 numerics coprocessor. The EISA chip set includes three chips:

82352DT	EISA Bus Buffers (EBB) (Optional)
82357	Integrated System Peripheral (ISP)
82358	EISA Bus Controller (EBC)

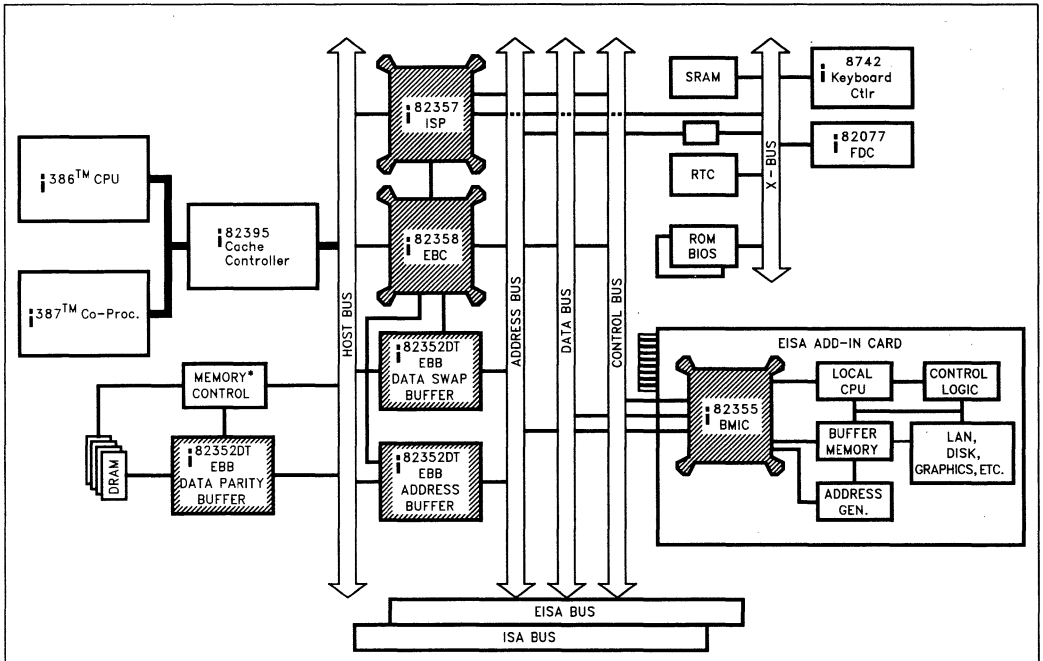
Information on the 82352DT EBB device is located in a separate data sheet.

The ISP performs the DMA functions of the system and is fully compatible with ISA functions. It integrates seven 32-bit DMA channels, five 16-bit timer/counters, two eight channel interrupt controllers, and provides for multiple NMI control and generation. It provides refresh address generation and keeps track of pending refresh requests when the bus is unavailable. The ISP supports multiple EISA bus masters while offering intelligent system arbiter services which grant the bus on a rotational basis.

The EBC is the EISA "engine". It is an intelligent bus controller that controls 8, 16 and 32-bit bus masters and slaves. It provides the state machine interface to Host, ISA and EISA busses and other IC's in the chip set. It offers a simple interface to the 386/i486 CPU and EISA bus. The EBC services as a bridge between the EISA and ISA devices. Data bus size mismatches are handled automatically by the EBC (including byte assembly and disassembly). It also guarantees cache operation on the Host, EISA, and ISA busses.

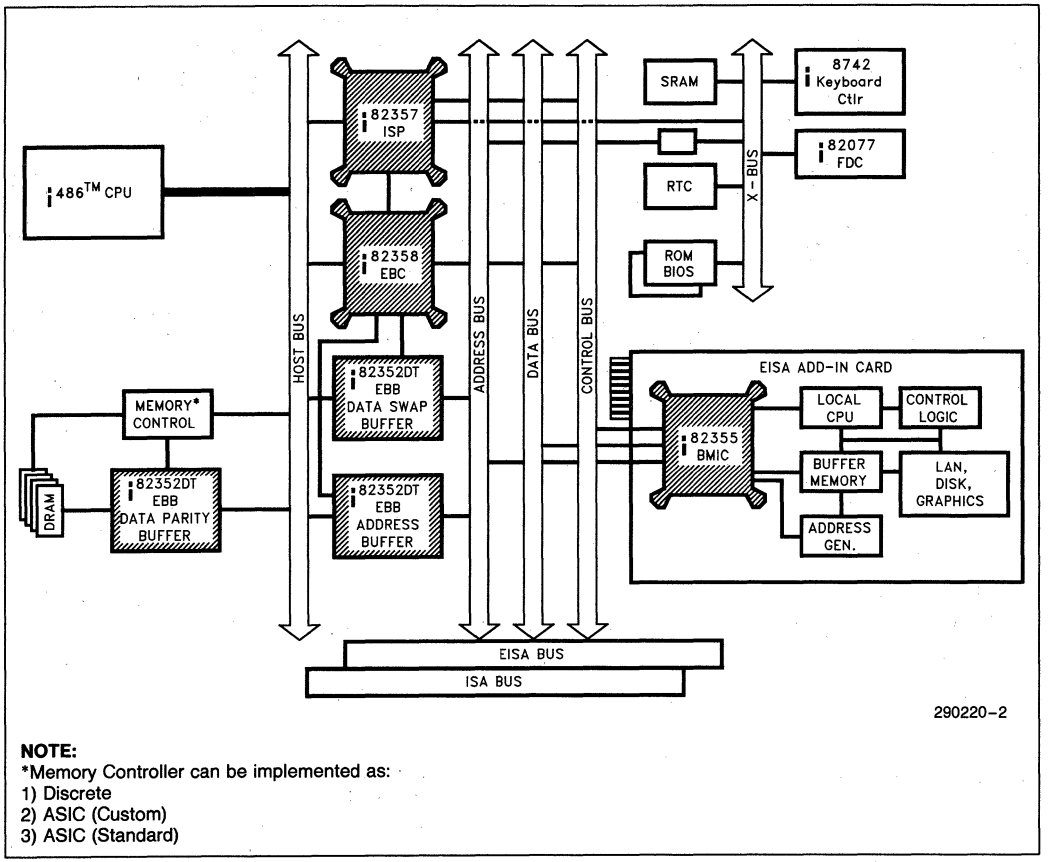
More information on EBC and ISP devices can be found in the data sheets in this document.

The 82355 Bus Master Interface Chip (BMIC) is a new device for add-in cards that takes advantage of the EISA bus master capabilities. Information on the 82355 BMIC is located in a separate data sheet.



NOTE:
*Memory Controller can be implemented as:
1) Discrete
2) ASIC (Custom)
3) ASIC (Standard)

Figure 1. Intel's 386 CPU System with 82350 EISA Chip Set



NOTE:
*Memory Controller can be implemented as:
1) Discrete
2) ASIC (Custom)
3) ASIC (Standard)

Figure 2. Intel's i486™ CPU System with 82350 EISA Chip Set

MECHANICAL DATA

PACKAGING INFORMATION

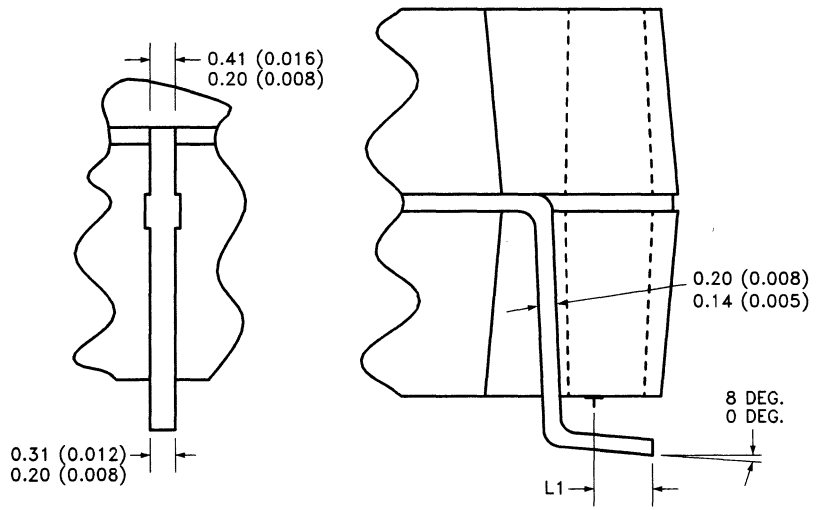
(See Packaging Spec. Order # 231369)

Introduction

The individual components of Intel's EISA Chip Set come in JEDEC standard Gull Wing packages (25 MIL pitch), with "bumpers" on the corners for ease of handling. Please refer to the accompanying table for the package associated with each device, and to the individual component specifications for pinouts. (Note that the individual pinouts are numbered consistently with the numbering scheme depicted in the accompanying figures).

TYPICAL LEAD

Case Outline Drawings
Plastic Fine Pitch Chip Carrier
0.84 mm Pitch

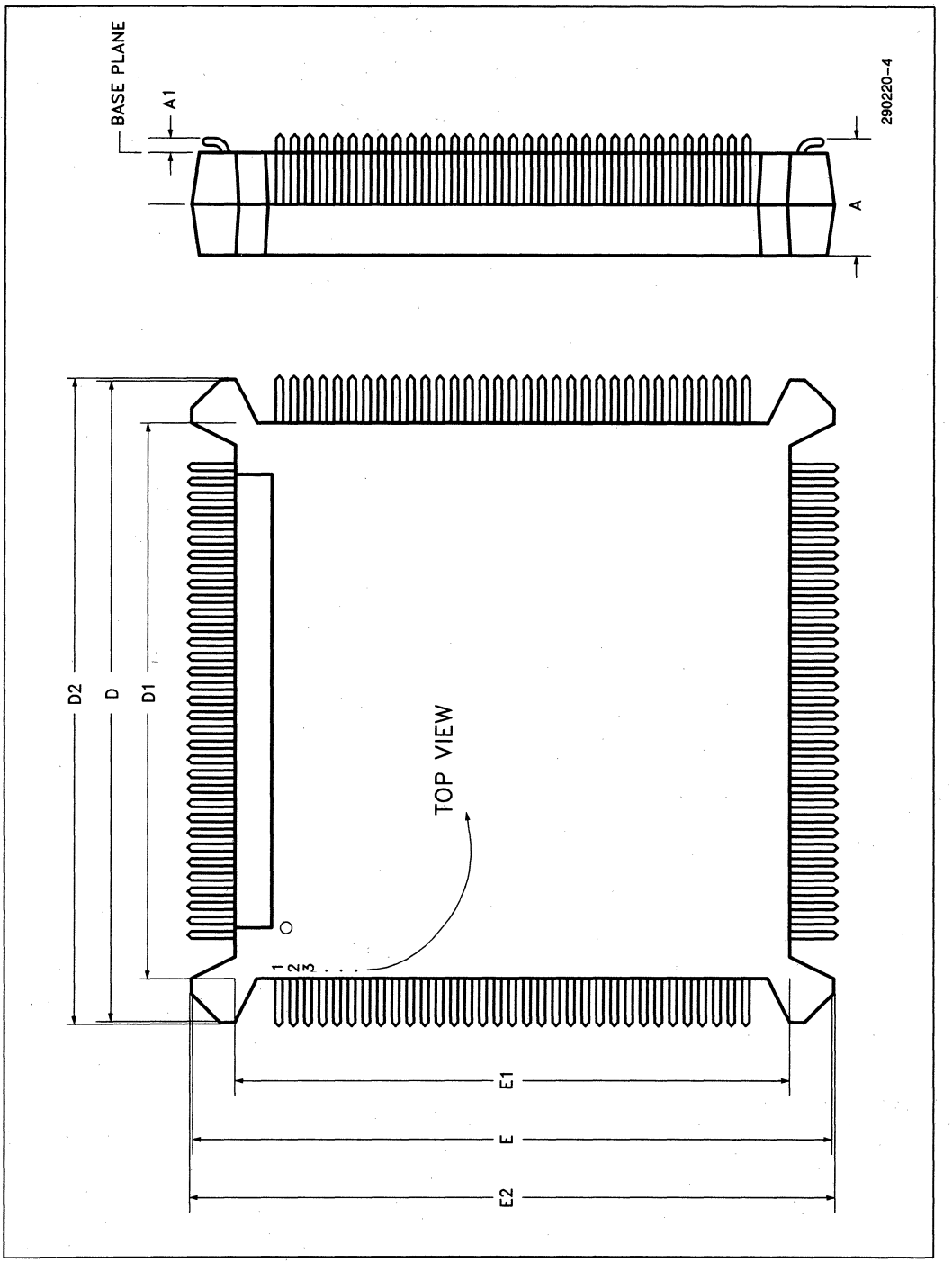


mm (inch)

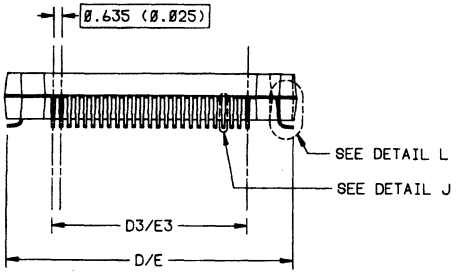
290220-3

Symbol	Description	Inch		mm	
		Min	Max	Min	Max
N	Lead Count	132		132	
A	Package Height	0.160	0.170	4.06	4.32
A1	Standoff	0.020	0.030	0.51	0.76
D, E	Terminal Dimension	1.075	1.085	27.31	27.56
D1, E1	Package Body	0.947	0.953	24.05	24.21
D2, E2	Bumper Distance	1.097	1.103	27.86	28.02
D3, E3	Lead Dimension	0.800 Ref		20.32 Ref	
L1	Foot Length	0.020	0.030	0.51	0.76

PRINCIPAL DIMENSIONS & DATUMS



TERMINAL DETAILS



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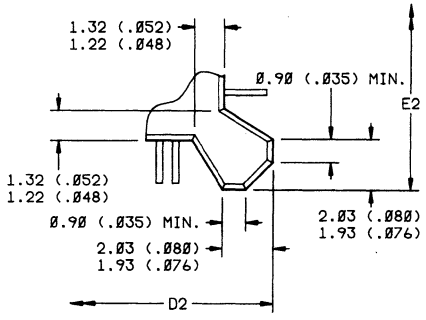
mm (inch)

BUMPER DETAIL



290220-6

mm (inch)

Package Thermal Specification

The 82357 ISP and 82358 EBC are specified for operation when the case temperature is within the range of 0°C to 85°C. The case temperature may be measured in any environment, to determine whether the device is within the specified operating range.

The PQFP case temperature should be measured at the center of the top surface opposite the pins, as shown in the figure below.

PLASTIC QUAD FLAT PACK (PQFP)

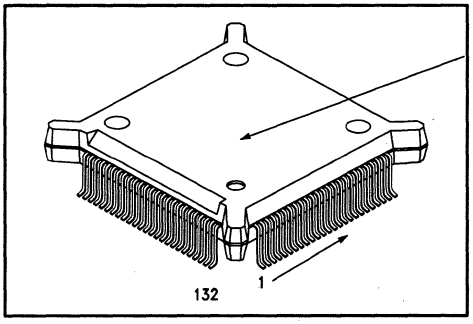


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Table 2. 82357 ISP and 82358 DT EBC PQFP Package Thermal Characteristics

Thermal Resistance— °C/Watt							
Parameter	**Air Flow Rate (ft/min)**						
	0	**50**	**100**	**200**	**400**	**600**	**800**
θ Junction—Case	7	7	7	7	7	7	7
θ Case to Ambient	22	21	19.5	17.5	14.5	12	10

NOTES:
1. Table 2 applies to the PQFP device plugged into a socket or soldered directly into the board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$.

PROCESS NAME:
1.2μ CHMOS III P-well

I_{CC} AT HOT WITH NO RESISTIVE LOADS:
150 mA Max at 85°C.

82352DT
EISA BUS BUFFER (EBB)

- **Designed Specifically for EISA Bus Requirements**
- **Provides Three Modes of Operation**
  - **— Data Latch and Swap Functions Allow Swapping and Assembly of Data between the Host and EISA/ISA Buses on a Byte by Byte Basis (Mode 0)**
  - **— Provides a Buffered Path with Parity Generation/Check between the Host Data Bus and DRAM (Mode 1)**
  - **— Address Latch Functions Provide Latching between the Host and EISA/ISA Buses (LA and SA Addresses) (Mode 3)**
- **120-Pin Quad Flat Pack (QFP)**
- **Similar in Function to Discrete Implementation Using 74F543s/544, 74180s, and 74ALS245s**
- **Replaces 19 Discrete Components**
  - **— Three 82352DTs are Used Per 82350 EISA System**
- **The 82352DT Interfaces Easily to the System**
  - **— Buffer Control for the 32-Bit Mode W/O Parity and the EISA Address Mode is Provided by the 82358 (EISA Bus Controller)**

(See Packaging Specification Order Number 240800, Package Type S)

1

The 82352DT design allows it to replace the multiple address and data latch-buffer/driver ICs used in EISA applications. The EBB provides three modes of operation: a 32-bit mode without parity to replace the EISA data swap buffers, a 32-bit mode with parity to replace the EISA DRAM data parity buffers, and an EISA address mode to replace the host to EISA/ISA address buffers. Mode 2 on the EBB is reserved. The same chip is strapped in three different ways to obtain the three configurations.

82352DT is manufactured and tested for Intel by LSI Logic in accordance with their internal standards.

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

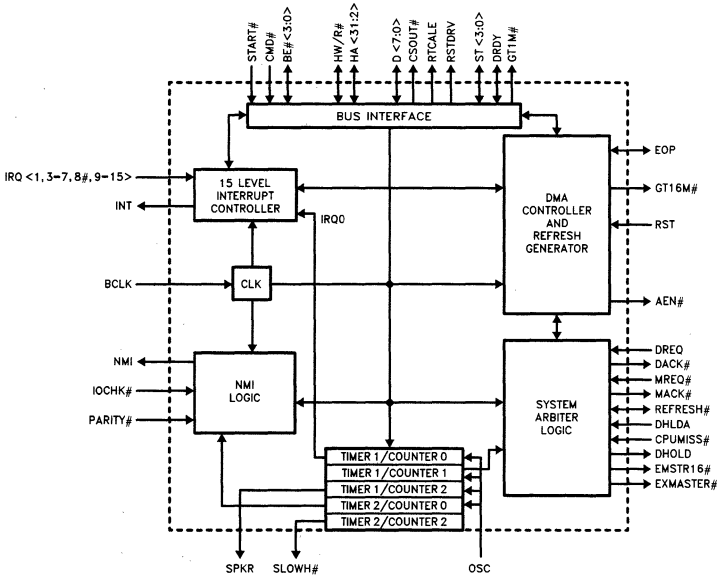
October 1993
Order Number: 290254-007

82357
INTEGRATED SYSTEM PERIPHERAL (ISP)

- **Provides Enhanced DMA Functions**
  - **— ISA/EISA DMA Compatible Cycles**
  - **— All Transfers are Fly-By Transfers**
  - **— 32-Bit Addressability**
  - **— Seven Independently Programmable Channels**
  - **— Provides Timing Control for 8-, 16-, and 32-Bit DMA Data Transfers**
  - **— Provides Timing Control for Compatible, Type "A", Type "B", and Type "C" (Burst) Cycle Types**
  - **— 33 Mbytes/sec Maximum Data Transfer Rate**
  - **— Provides Refresh Address Generation**
  - **— Supports Data Communication Devices and Other Devices That Work from a Ring Buffer in Memory**
  - **— Incorporates the Functionality of Two 82C37A DMA Controllers**
- **Provides High Performance Arbitration**
  - **— For CPU, EISA/ISA Bus Masters, DMA Channels, and Refresh**
- **Incorporates the Functionality of Two 82C59A Interrupt Controllers**
  - **— 14 Independently Programmable Channels for Level-or-Edge Triggered Interrupts**
- **Five Programmable 16-Bit Counter/Timers**
  - **— Generates Refresh Request Signal**
  - **— System Timer Interrupt**
  - **— Speaker Tone Output**
  - **— Fail-Safe Timer**
  - **— Periodic CPU Speed Control**
  - **— 82C54 Programmable Interval Timer Compatible**
- **Provides Logic for Generation/Control of Non-Maskable Interrupts**
  - **— Parity Errors for System and Expansion Board Memory**
  - **— 8 μs and 32 μs Bus Timeout**
  - **— Immediate NMI Interrupt via Software Control**
  - **— Fail-Safe Timer**
- **132-Pin PQFP Package**

  (See Packaging Specifications: Order Number 240800, Package Type NG)

82357 Internal Block Diagram



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Intel486 is a trademark of Intel Corporation.

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

March 1994
Order Number: 290253-006

82358DT
EISA BUS CONTROLLER

- **Supports 82350 and 82350DT Chip Set Based Systems**
  - **— Mode Selectable for Either 82350 or 82350DT Based Systems**
  - **— Mode Defaults to 82350 Based Systems**
- **Socket Compatible with the 82358 (EISA Bus Controller)**
- **Provides EISA/ISA Bus Cycle Compatibility**
  - **— EISA/ISA Standard Memory or I/O Cycles**
  - **— EISA/ISA Wait State Cycles**
  - **— ISA No Wait State Cycles**
  - **— EISA Burst Cycles**
- **Supports Intel386™ & Intel486™ Microprocessors**
- **Translates Host (CPU) and 82359 (DRAM Controller) Cycles to EISA/ISA Bus Cycles**
- **Generates ISA Signals for EISA Masters**
- **Generates EISA Signals for ISA Masters**
- **Supports 8-, 16-, or 32-bit DMA Cycles**
  - **— Type A, B, or C (Burst) Cycles**
  - **— Compatible Cycles**
- **Supports Host and EISA/ISA Refresh Cycles**
- **Generates Control Signals for Address and Data Buffers**
  - **— 82353 (ADP) and 82352 (EBB)**
- **Supports Byte Assembly/Disassembly for 8-, 16-, or 32-Bit Transfers**
- **Selectable Host (CPU) Posted Memory Write Support to EISA/ISA Bus**
- **Cache Controller (82385, 82395) Interface to Maximize Performance for 386 Based Systems**
- **Supports I/O Recovery Mechanism**
- **Generates CPU, 82385, and System Software Resets**
- **132-Pin PQFP Package**
- **Low Power CHMOS Technology**

(See Packaging Specification Order #240800, Package Type NG)

1

The 82358DT EISA Bus Controller is part of Intel's 82350 and 82350DT chip sets. There are five mode or function select pins which allow the 82358DT to be programmed for use in either 82350 or 82350DT based systems. The mode pins also provide support for posted memory write cycles to the EISA/ISA bus and Intel486™ burst support. The 82358DT defaults to 82350 mode and is 100% socket compatible with the 82358 (EBC).

The 82358DT interfaces the 386 and Intel486 microprocessors to the Extended Industry Standard Architecture (EISA) bus. It is used to facilitate bus cycles between the Host (CPU) bus and the EISA/ISA bus. In an 82350 system, the 82358DT interfaces to the cycle address and control signals of the Host bus. In an 82350DT system, the 82358DT interfaces to the cycle address and control signals of the 82359 DRAM controller. The 82358DT generates the appropriate data conversion and alignment control signals to implement an external byte assembly/disassembly mechanism for transferring data of different widths between the Host, EISA, and Industry Standard Architecture (ISA) buses. It also provides the cycle translation between the Host, EISA, and ISA buses.

The 82358DT is tightly coupled with the 82357 DMA controller (ISP) to run 8-. 16-, or 32-Bit EISA/ISA DMA transfers.

The 82358DT features hardware enforced I/O recovery logic to provide I/O recovery time between back- to-back I/O cycles.

The 82358DT provides special cache hardware interface signals to implement a high performance 386 based system with an 82385 or 82395 cache controller.

The 82358DT also provides resets to the Intel486, 80386, 82385, and other devices in the system to provide an integrated synchronous system reset.

Intel486 is a trademark of Intel Corporation.

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

March 1994
Order Number: 290380-004

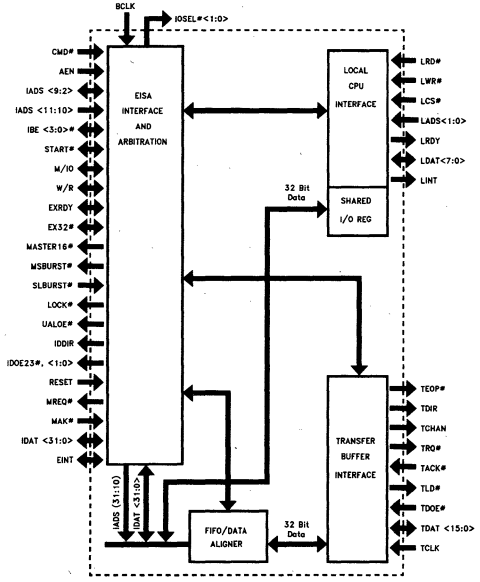
intel®

82355
BUS MASTER INTERFACE CONTROLLER (BMIC)

- Designed for use in 32-Bit EISA Bus Master Expansion Board Designs
  - — Integrates Three Interfaces (EISA, Local CPU, and Transfer Buffer)
- Supports 16- and 32-Bit Burst Transfers
  - — 33 Mbytes/Sec Maximum Data Transfers
- Supports 32-Bit Non-Burst and Mismatched Data Size Transfers
- Supports 32-Bit EISA Addressability (4 Gigabyte)
- Two independent Data Transfer Channels with 24-Byte FIFOs
  - — Expansion Board Timing and EISA Timing Operate Asynchronously
- Supports Peek/Poke Operation with the Ability to Access Individual Locations in EISA Memory or I/O space
- Automatically Handles Misaligned Doubleword Data Transfers with No Performance Penalty
- Supports Automatic Handling of Complete EISA Bus Master Protocol
  - — EISA Arbitration/Preemption
  - — Cycle Timing and Execution
  - — Byte Alignment
  - — 1K Boundary Detection
- Supports Local Data Transfer Protocol Similar to Traditional DMA
- Supports a General Purpose Command and Status Interface
  - — Local and EISA System Interrupt Support
  - — General Purpose Information Transfers
  - — Set-and-Test-Functions in I/O Space (Semaphore Function)
  - — Supports the EISA Expansion Board ID Function
- Supports Decode of Slot Specific and General I/O Addresses
- 132-Pin JEDEC PQFP Package

  (See Packaging Specification Order #240800, Package Type NG)

82355 Internal Block Diagram



290255-1

May 1994
Order Number: 290255-008

82355 Bus Master Interface Controller (BMIC)

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1.0 INTRODUCTION

The 82355 Bus Master Interface Controller (BMIC) is a highly integrated Bus Master designed for use in 32-Bit EISA Bus Master expansion board designs and supports all of the enhancements defined in the EISA specifications required for EISA bus master applications. The BMIC provides a simple, yet, powerful and flexible interface between the functions on the expansion board and the EISA bus. With the help of external buffer devices, the BMIC provides all EISA control, address, and data signals necessary to interface to the EISA bus.

The primary function of the 82355 is to support 16- and 32-bit burst data transfers between functions on the EISA expansion board and the EISA bus. Data transfer rates of up to 33 Mbytes/sec are supported (the fastest transfer rate available on an EISA bus). The following logic on the BMIC supports efficient burst transfers:

- Arbitration logic, for gaining control of the EISA bus
- Two transfer-address and byte counters
- Two data FIFOs, which allow expansion board and EISA bus timing to operate asynchronously
- Data shifters, which align data to specific byte boundaries
- A transfer buffer interface, for the data transfers on the expansion board
- General-purpose command and status interface logic
- Local processor interface, to allow programming by an on-board processor
- EISA slave interface, to allow communication with the EISA system

The BMIC greatly simplifies the design of EISA expansion boards. With the 82355, a board can be implemented with simple logic similar to that used in traditional ISA DMA designs. The EISA standard allows designs with 32-bit data and address buses, burst transfers, and automatic handling of the full EISA bus master protocol.

To maximize system throughput, the 82355 BMIC incorporates three fully concurrent interfaces: EISA interface, Transfer Buffer interface, and Local Processor interface. The EISA interface incorporates two 24-byte FIFOs, and implements the full EISA protocol. The Transfer Buffer interface is optimized for high speed static RAM buffers, and can operate at a maximum frequency of 20 MHz. The Local Processor interface supports a generic slave interface, and allows the local processor to fully program the BMIC for operation. Local processors are supported with the ability to access individual locations in system memory or I/O space; this peek-and-poke feature allows the expansion board to communicate easily with other devices in the system. All three interfaces can operate simultaneously, thus maximizing overall system performance.

Address-generation support for the data transfer buffer logic on the expansion board is provided on-chip. The transfer logic on the expansion board can use a high-speed asynchronous transfer clock. The BMIC handles all synchronization with the EISA bus. A FIFO within the BMIC eliminates performance degradation on burst transfers caused by synchronization delays. The BMIC also provides a set of programmable address comparators that drive external chip selects on the expansion board to assist local devices in decoding I/O address ranges.

1.1 BMIC Terminology/Definitions

EISA BUS MASTER—A 32- or 16-bit device that uses the extended part of the EISA bus to generate memory or I/O cycles.

Downshifting Bus Master—A "downshifting" master is a 32-bit master which can convert to a 16-bit master "on the fly". The BMIC will only downshift from a 32-bit master to a 16-bit master if programmed for burst mode (refer to Section 4.2.1).

EISA READ—A data transfer (burst, non-burst (two BCLK), or mismatched) from system to the expansion board across transfer channel 1.

EISA WRITE—A data transfer (burst, non-burst (two BCLK), or mismatched) from the expansion board to system memory across one of the two transfer channels.

I/O ADDRESS DECODE SUPPORT—Refers to slot specific or general I/O address decoding.

Slot Specific Address Decoding—Refers to the decoding of unique addresses allocated to EISA slot specific expansion boards. These addresses are: X000h–X0FFh, X400h–X4FFh, X800h–X8FFh, and XC00h–XCFFh, where X represents the EISA slot number. EISA slot number "0" is reserved for the EISA system board.

General I/O Address Decoding—Refers to the decoding of addresses allocated to ISA expansion boards. These addresses are: 0100h–03FFh.

LOCAL PROCESSOR—A processor located on the expansion board.

SYSTEM CPU—Processor located on the motherboard.

SYSTEM MEMORY—Memory located on the EISA bus or motherboard.

TRANSFER INTERRUPTION—A transfer interruption is defined as an occurrence resulting in a break in a transfer caused by one of the following conditions: A FIFO pause, a FIFO stall, a channel preemption, a channel clear or suspension, a 1K page break, or a transfer complete (EOP).

FIFO Pause—This is a condition where the EISA bus does not provide or take data at a rate fast enough to keep up with the expansion board transfer buffer logic. During an EISA read, this condition is defined as an empty FIFO. During an EISA write, this condition is defined as a full FIFO. A FIFO pause is considered a preferred condition and under normal operations should occur frequently. A FIFO pause will result in the BMIC negating TRQ# until the FIFO becomes not full during an EISA write or not empty during an EISA read.

FIFO Stall—This is a condition where the transfer buffer logic on the expansion board does not provide or take data at a rate fast enough to keep up with the EISA bus. During an EISA read, this condition is defined as a full FIFO. During an EISA write, this condition is defined as an empty FIFO. Under normal operations, a FIFO stall is expected to be a rare and exceptional event. For additional information regarding a FIFO stall, refer to Section 6.2.

Channel Clear—A channel clear results in the immediate termination of the current transfer and the flushing of the channel's corresponding FIFO. A channel clear is initiated by setting the CFGCL bit in the corresponding channel's Configuration register to a 1. For additional information regarding channel clear, refer to Section 8.2.4.2.

Channel Suspension—This temporarily prevents a channel from proceeding with a transfer. A transfer can be temporarily suspended by setting the CFGSU bit in the corresponding channel's Configuration register to a 1.

Channel Preemption—The BMIC can be preempted from the EISA bus by the 82357 (ISP). The 82357 negates MAK# indicating to the BMIC that it must finish the current bus cycle and relinquish control of the EISA bus by negating MREQ# within 64 BCLK periods. The BMIC is programmable to relinquish the bus within 0, 32, or 64 BCLKs from the negation of MAK# (refer to Section 4.4.2).

1K Page Break—The temporary termination of a burst, non-burst (two BCLK), or mismatched data transfer due to a 1K page address boundary crossing (refer to Section 4.2.2).

Transfer Complete (EOP)—End of process due to the transfer byte count being exhausted or a channel being cleared (channel clear). A transfer complete (EOP) will result in the BMIC asserting TEOP# with the last cycle (refer to Section 5.4).

TRANSFER BUFFER LOGIC—Logic located on the expansion board used to support the transfer and storage of data during BMIC EISA master mode transfers between the expansion board and system memory.

The transfer buffer logic interfaces to the Transfer Buffer Interface of the BMIC. Refer to Section 5.2 for additional information regarding transfer buffer logic.

2.0 BMIC INTERFACE ILLUSTRATION

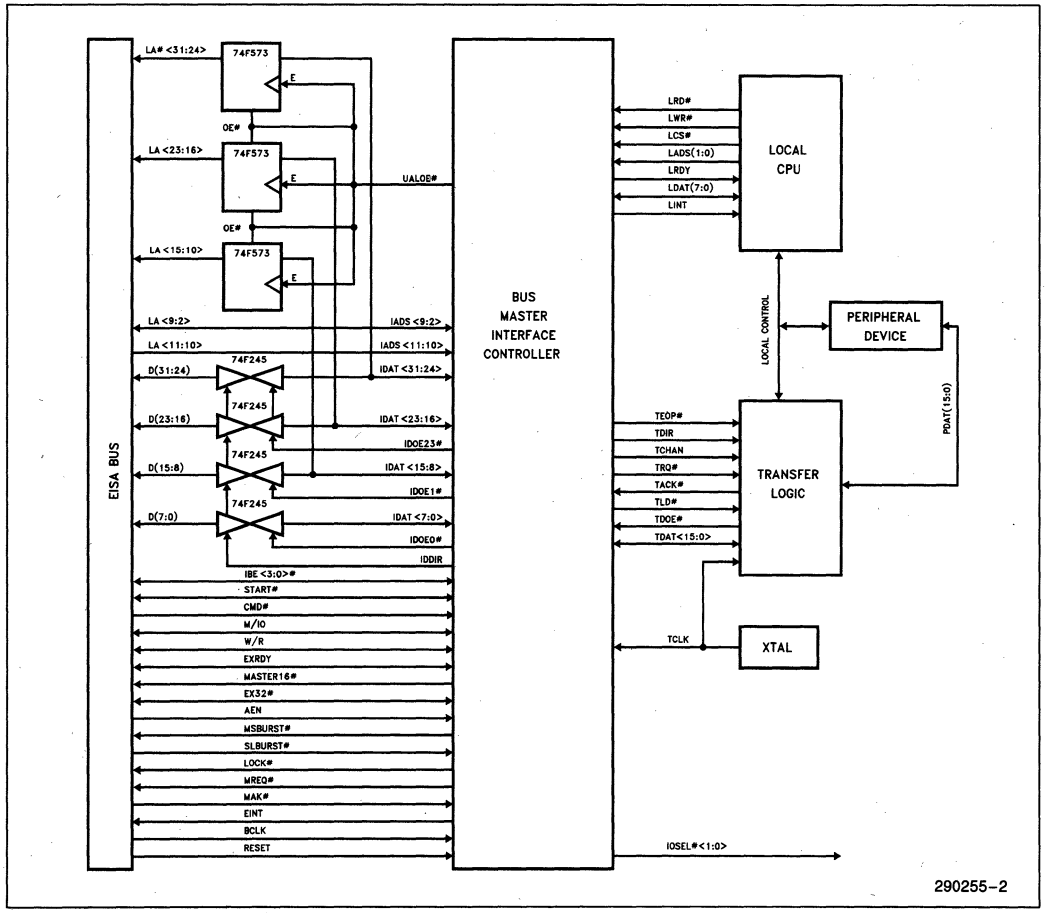


Figure 2-1. BMIC System Interface

3.0 FUNCTIONAL OVERVIEW

The following is a brief discussion of the functional blocks and features of the 82355. The EISA interface, Transfer Buffer interface, FIFO/Data Aligner, and Local interface each have a corresponding detailed section later in this data sheet.

3.1 EISA Master and EISA Slave Operations

In EISA slave mode, the 82355 monitors the EISA address lines <11:2> for general I/O address decoding, slot-specific address decoding, and Shared register accessing. During slave mode operations, all internal registers are accessible through the Local Processor interface, and all Shared registers are accessible through either the Local Processor interface or the EISA interface of the BMIC.

In EISA master mode, the 82355 becomes the master of the EISA bus. It may perform burst, non-burst (two BCLK), mismatched, or Peek/Poke data transfers at this time. During master mode operations, all internal registers are accessible through the Local Processor interface of the BMIC.

The arbiter portion of the BMIC determines which mode the device is in, performs the EISA arbitration, and provides the control signals necessary to regulate the slave and master activities internal to the chip. In slave mode, the arbiter also mediates between the EISA side and the local side during Shared register accesses.

The following is a table of the functions that can be performed during master and slave operations:

	Shared Reg. Accessing	Local CPU Only Reg. Accessing	EISA I/O Address Decoding	Data Transfers
EISA Slave Mode	YES (1, 2)	YES	YES	NO
EISA Master Mode	YES (2)	YES	NO	YES

NOTE:
Shared Reg. Accessing refers to the registers that are accessible through either the EISA interface or Local Processor interface.
Local Processor Only Reg. Accessing refers to the registers that are accessible through the Local Processor interface only.
EISA I/O Address Decoding refers to either general or slot specific I/O decoding support for the expansion board.
Data Transfers refer to either burst, non-burst (two BCLK), mismatched, or peek/poke data transfers.
YES = Can Be Performed
NO = Can Not Be Performed
1 = EISA interface
2 = Local interface

3.2 82355 Internal Architecture Description

The 82355 contains four blocks of control logic. The EISA interface block, Transfer Buffer interface block, FIFO/Data Aligner block, and the Local Processor interface block.

3.2.1 EISA INTERFACE BLOCK

The EISA interface block provides the following functions:

— generates the 32-bit EISA address for burst, non-burst (two BCLK), and peek/poke data transfers
— generates the EISA control signals necessary to implement an EISA 16-bit or 32-bit bus master, and a 32-bit EISA slave
— generates the control signals necessary to enable and disable the external buffer devices
— performs the EISA arbitration and provides the internal control signals required to regulate the slave and master activities of the BMIC
— integrates the registers necessary for the above operations as well as the registers required to provide the configuration and status of the data transfers between the EISA bus and the memory buffer on the expansion board

The EISA memory address range of the 82355 covers the 4 Gigabytes and supports the detection of 1K page address boundaries during burst, non-burst (two BCLK), and mismatched data cycles to and from system memory.

During slave mode, the EISA interface also supports slot specific and general I/O address decode necessary for Shared Register accesses and general decode as required by the expansion board. The shared register addresses are mapped into the slot specific I/O range (C80h-C9Fh).

The EISA interface block contains 43 registers necessary to execute the above functions. A detailed description of the registers and their functions can be found under Register Description (Sections 8.1 and 8.2).

3.2.2 TRANSFER BUFFER INTERFACE BLOCK

The Transfer Buffer interface block provides the group of signals that are required to perform 16-bit data transfers to and from the memory buffer on the expansion board. The protocol used is similar to that found in standard DMA designs. The interface includes a 16-bit data bus (TDAT), seven control signals and a transfer clock (TCLK). The transfer clock can run completely asynchronous to the EISA BCLK signal.

The Transfer Buffer interface block also provides a 16-bit transfer start address which is generated at the beginning of all new data transfers to and from the memory buffer on the expansion board. The 16 TDAT data lines are used to transfer the address.

The Transfer Buffer interface block contains eight registers. A detailed description of the registers and their functions can be found under Register Description (Section 8.2).

3.2.3 FIFO/DATA ALIGNER BLOCK

The FIFO/Data Aligner block is used to isolate and simplify the timing relationships between the EISA bus and the bus master expansion board. This allows the transfer buffer logic and EISA bus timing to operate asynchronously. The FIFO provides the data channel between the EISA bus and the expansion board during BMIC master data transfers and the Data Aligner provides the byte alignment and assembly necessary for the EISA bus.

There are two dual-port, six doubleword wide (24 byte) FIFOs on-board, one per transfer channel. The data is written into the FIFO from either the EISA bus side or the expansion board side, depending on the direction of the transfer. The transfer direction is controlled by a bit in the Transfer Base Count register set.

3.2.4 LOCAL PROCESSOR INTERFACE BLOCK

The Local Processor interface block provides the interface between the BMIC and the local processor. If a local processor is not present, the processor interface can be connected to the ISA bus. The Local Processor interface block is based on an 8086 style slave mode and provides an 8-bit data path for BMIC programming. All of the BMICs internal registers are accessible through this interface.

The Local Processor interface block contains a group of Shared registers used to support general-purpose command and status interactions between the system CPU or EISA bus master and the local processor. In addition to the command/status registers, the CPU interface includes a set of ID registers for EISA expansion board ID support, and a set of Peek/Poke data registers used to hold the data during peek/poke operations.

The local interface portion of the BMIC also contains three 8-bit registers which are used by the local processor to access all of the BMICs internal registers. These registers are mapped into the local processor interface and include a local status register, local data register, and a local index register (refer to Section 3.2.6.1).

The Local Processor block contains 31 registers. A detailed description of the registers and their functions can be found under Register Description (Sections 8.1 and 8.2).

3.2.5 DATA TRANSFER TYPES

The BMIC supports four types of data transfers on the EISA bus: Burst, non-burst (two BCLK), peek/poke or locked exchange, and mismatched. For all of the above transfer types, the addressed slave device can negate EXRDY if wait state timing is required (each wait state is one BCLK).

The primary function of the BMIC is to support 16- and 32-bit burst data transfers between functions on the expansion board and the EISA memory. If the addressed memory is not capable of supporting burst transfers, the BMIC will run either 32-bit non-burst (two BCLK) cycles or, with the support of the 82358 EISA Bus Controller, run mismatched data cycles.

The burst cycle type provides a continuous sequence of one BCLK read or write cycles to and from 16- or 32-bit EISA memory. Burst cycles can not be used with I/O devices or ISA devices (slaves or masters).

The non-burst cycle type provides a continuous sequence of two BCLK read or write transfers to and from 32-bit EISA memory. The BMIC will only respond as a 32-bit master when configured for two BCLK transfers (refer to Section 4.2.1).

The peek/poke and locked exchange feature allows local processor accesses to and from individual I/O space or system memory locations on the EISA bus. The BMIC responds as a 32-bit master and generates two BCLK cycles when configured for peek/poke transfers (refer to Section 4.3). A locked exchange transfer consists of six BCLKs (peek followed by a poke). A peek/poke data transfer has the same timings as a non-burst (two BCLK) data transfer.

The mismatched cycle type provides a means of communicating with 8- or 16-bit EISA or ISA devices. In the event the I/O or memory slave device that has been addressed requires a data size translation, the BMIC will back-off the bus and allow the 82358 EISA Bus Controller to perform the necessary data size translations (refer to Section 4.2.1). The BMIC will generate mismatched cycles as required for all data transfers (burst, non-burst, peek, poke, or locked-exchange).

The following table identifies the BMIC cycle types, master sizes, slave types accessible (memory-I/O), and BCLKs per cycle.

Transfer Type	BMIC Master Size		Slave Type Accessible		BCLKs per Cycle
	16-Bit	32-Bit	I/O	Memory	
Burst	X	X		X	1
Mismatched		X		X	*
Non-Burst		X		X	2
Mismatched		X		X	*
Peek/Poke		X	X	X	2
Mismatched		X	X	X	*
Locked Exchange		X	X	X	6
Mismatched		X	X	X	*

*Depends on slave type/size (EISA/ISA, I/O/Memory, 8-bit/16-bit)

For all of the above transfer types, the addressed slave device can negate EXRDY if wait-state timing is required (each wait-state is one BCLK).

3.2.6 REGISTER ACCESSING

The BMIC provides three distinct groups of registers; the Shared register set, the Local Processor Only register set, and the Index register set. The Shared register set is used by the system CPU or EISA bus master and the local processor for general-purpose command and status interactions and expansion board ID support. The Local Processor only registers are used by the local processor to program the BMIC and provide status for data transfers across the EISA bus and Transfer Buffer interface. The Local Processor Only register set also provides address range decode support for slot specific and general I/O address ranges of interest to the expansion board. The Index register set is used by the local processor as a means of accessing all of the above registers through an indexing scheme.

The Shared register set is accessible through either the EISA interface or the Local Processor interface, the remaining two register sets are accessible through the Local Processor interface only. In the case of contention between the EISA bus and the local processor accessing a Shared register simultaneously, the local processor on the expansion board will have initial priority. Consecutive multiple accesses to the BMIC's shared registers result in a rotational arbitration between the EISA bus and the local processor.

3.2.6.1 Register Accessing through the Local Processor Interface

Register accessing on the local side of the BMIC is accomplished using an indexing procedure. The local interface portion of the BMIC contains two 8-bit registers which are used by the local processor to access all of the BMIC's internal registers. These registers are mapped into the Local Processor interface and include a local data register and a local index register. The registers are selected using the two local address lines (LADS<1:0>). The BMIC's internal register set is read by writing the address of the register to be accessed into the local index register. The register contents are then read through the Local Data register. To write to one of the BMIC's internal registers, the local processor must first write the address of the register to be accessed into the local index register, same as a read, then write the new data value to the Local Data register.

An optional auto-increment mode is supported by the BMIC, which automatically increments the index register after each register read or write. This allows for efficient programming of the register set by using byte string moves. If the Local Index register is given a local index address with bit (7) set high, the local index address will automatically increment each time the Local Data register is read or written.

The Local Status/Control register is directly mapped into the Local Processor interface and is also accessible using the two address lines (LADS<1:0>).

3.2.6.2 Register Accessing through the EISA Interface

The shared registers are mapped directly into the EISA slot-specific I/O space XC80–XC9F. The EISA address lines <11:2> and the byte enables <3:0> are used for decode during shared register accesses.

A standard slave read or write access to the BMIC consists of two BCLKs + one wait-state (one wait-state = one BCLK period). During a slave cycle where the EISA access loses the internal register access through arbitration to the local processor, the cycle will consist of two BCLKs + two wait-states. The BMIC will negate EXRDY for one BCLK for each wait-state required.

3.2.7 INTERRUPTS

The BMIC provides two interrupt request lines, one for the EISA side (EINT), and one for the local side (LINT). The EISA interrupt (EINT) can be programmed for either edge or level-triggered operations. During edge-triggered operations the EINT signal will transition from a low level to a high level. In level-triggered mode, the EISA interrupt signal is an active low open collector output. The local interrupt signal (LINT) can be programmed for either active low or active high level operations and will default to active low operation upon reset. The LINT signal is not an open collector output during active low operations and will require external logic if interrupts need to be tied together on the local side. The EINT and LINT modes of operation are programmed through the Global Configuration register.

3.2.7.1 Interrupt Sources

Several events can trigger each of the two interrupt request signals, and the events can be enabled or disabled on an individual or global basis (refer to Sections 8.1.1.3 and 8.2.2). The system CPU or EISA bus master can only be interrupted by an I/O write from the local processor to the BMIC EISA System Doorbell register. However, the local processor can be interrupted by several sources which are listed below:

— An I/O write from the system CPU or EISA bus master to the BMIC Local Doorbell register.

— The completion of a data transfer on one of the transfer channels.

3.2.7.2 Interrupt Handling

To prevent the BMIC from allowing undetected interrupts from occurring, when servicing an interrupt initiated by the BMIC, all additional interrupts must be disabled prior to reading the Local or EISA System Doorbell Status registers. The interrupts are disabled by writing to the Local or EISA System Doorbell Enable registers, depending on the source of the interrupt.

This is required due to the nature of the interrupt mechanism of the BMIC. All interrupt sources have an edge triggered nature internal to the BMIC, with each event being 'OR'ed together. Additional interrupt sources occurring after the first interrupt will set their appropriate bit in the Status register, but they will not generate an external interrupt until the initial event has been cleared. Thus if the Status register was read first, and another interrupt occurred after this read, the second interrupt would remain undetected in the status register until another event occurred. Disabling of the interrupts prior to reading the status register will prevent this from occurring.

4.0 EISA INTERFACE

4.1 EISA Interface Signals

The BMIC provides a complete interface to the EISA bus and supplies all of the control signals, data lines, and address lines necessary to implement a 16- or 32-bit EISA bus master and a 32-bit EISA slave. This includes a 32-bit data path, a 32-bit address path, and 20 EISA control signals. The BMIC also provides five control signals used to enable and disable the external data buffers and address latches, as shown in Figure 2-1.

The BMIC uses four 74F245 external bidirectional buffers to drive and receive the 32 EISA data and three 74F573 external latches to latch and drive the upper 22 EISA address lines. The external data buffers and address latches should be comprised of "F" or "AS" type logic to meet EISA speed requirements.

The upper 22 EISA addresses are multiplexed through the 22 upper EISA data lines of the BMIC. They are latched externally by the 74F573's. EISA address lines <11:2> and byte enable lines <3:0> are tied directly to the EISA bus. Address lines 10 and 11 are input directly to the BMIC for slave mode address decode. During EISA master operation, lines 10 and 11 are driven indirectly through the external latches.

As a slave, the BMIC receives address lines IADS<11:2> and byte enable lines IBE<3:0># for I/O address decode. Address lines <11:2> are used for slot specific decode and address lines <9:2> are used for general I/O address decode. Address lines <11:2> along with IBE<3:0># are used by the BMIC during Shared register accesses. Address lines <31:12> are not used by the BMIC in slave mode.

The following address lines are used during I/O decoding as shown:
Slot specific I/O address decoding (expansion board)—IADS<11:2>
Slot specific I/O address decoding (shared registers)—IADS<11:2>/IBE<3:0>#
General I/O address decoding (expansion board)—IADS<9:2>

All of the BMIC EISA control signals function as defined in the EISA bus specification. The signals are used to support the following cycles:

BMIC as a Master

	(Cycle Type Performed)			
Master Type	**Burst**	**Non-Burst**	**Mismatched**	**Peek/Poke/Locked Exchange**
32-Bit	X	X	X	X
16-Bit	X			

BMIC as a Slave

1. Responds to EISA shared register accesses as 32-bit slave.
2. Responds to slot specific and general I/O accesses (refer to Section 4.8).

4.2 Transfer Channels

The BMIC contains two identical independent transfer channels which are configurable to run either burst or non-burst (two BCLK) cycles to and from system memory. The BMIC will automatically run non-burst (two BCLK) or mismatched cycles if the memory the BMIC has addressed cannot run burst cycles. Mismatched cycles will be run if data size translation is required.

Channel 0 must be used for EISA READ operation only. Channel 1 can be used for both EISA READ and EISA WRITE operations.

Each channel has three sets of registers to regulate data transfers. These are the Base register group, the Current register group, and the Data Status/ Control register group. This implementation of a triple register set allows a processor to begin programming the next transfer on the channel while the current transfer is being executed.

The Base register set contains seven 8-bit registers. These registers are programmed by the local processor when a transfer is required across one of the channels. Four Transfer Channel Base Address registers are combined to form the starting 32-bit EISA address to be used during the transfer. The remaining three registers are the Transfer Channel Base Count Registers. The Base Count registers are combined to determine the number of transfers (in bytes) to be performed. The number of bytes which can be transferred ranges from 1 byte to 4 Mbytes. The most significant bit of the Transfer Channel Base Count register group is used to control the start of the transfer and the second most significant bit is used to control the direction of the transfer (refer to Section 8.2.3.3).

The Current register set contains seven registers each of which corresponds to a Base register. These registers are loaded from the Base registers. The Transfer Channel Current Address registers contain the 32-bit real-time EISA memory address. The Transfer Channel Current Count registers contain the number of bytes remaining to be transferred on the channel. The current register set is readable by the local processor. However, there are possible coherency problems involved with reading multiple bytes while the current registers are being updated during a transfer. To avoid these problems, a channel's transfer should be temporarily suspended (using the channel's Configuration Register) before trying to read the channel's current register set.

The Status/Control register set contains three registers: the Transfer Channel Strobe register, Transfer Channel Configuration register, and the Transfer Channel Status register. The Transfer Channel Strobe register is used to initiate the transfer of data from the Base register set to the associated Current register set. A transfer request for that channel will be generated following the Current register load. The Transfer Channel Configuration register is used to program the mode of the transfer. The Transfer Channel Status register provides current FIFO and transfer channel status.

To initialize a transfer over either of the two transfer channels, the following steps must be completed:

1. Verify that the Base registers for the desired transfer channel are available.

   The Transfer Channel Base Address and Base Count registers must be available before they can be programmed. This is determined by the status of bits 0 and 1 in the Local Status/Control register. A "1" in either of the two bits indicates that the corresponding channel is currently running a transfer and the Base registers are busy. A "0" indicates that the Base registers are free and available for programming. In the event that the Base registers are not available, the local processor must wait until the data transfer executing on the requested channel has completed, at which time bits "0" or "1" (depending on which channel was programmed) in the Local Status/Control registers will be reset to 0. Programming the Base registers during a Base register Busy state, is illegal and will corrupt the Base register data of the pending transfer. Programming the Transfer Configuration register during a cycle in progress may cause the termination of the transfer, depending on which bit in the register was changed.
2. Program the transfer channel's associated Transfer Base register set with the desired transfer information (Base registers must be available).
3. Initiate the Base register to Current register load and schedule a transfer request by writing to the channel's Transfer Strobe register.

   If a transfer is in progress on the requested channel and a write to the associated channel's Strobe register is done, the Base to Current register load will take place immediately after the data transfer on the requested channel has completed.

4.2.1 BURST AND NON-BURST MODES OF OPERATION

The BMIC can be programmed for burst or non-burst (two BCLK) data transfers to and from EISA memory. This is determined by a write to the Channel Configuration Register.

If burst mode is enabled, the BMIC will look for the SLBURST# signal at the beginning of the transfer to determine if the slave device that was addressed is

capable of running burst cycles. If the slave device does not respond with an active SLBURST# signal, the BMIC will not activate the MSBURST# signal and will proceed with either non-burst (two BCLK) bus cycles or mismatched cycles.

In burst mode, the BMIC can respond as a 16- or 32-bit master. The BMIC informs the system of this capability by driving MASTER16# low from the same BCLK rising edge that START# is asserted. MASTER16# will remain low for one BCLK. The BMIC will automatically "downshift" from a 32- to a 16-bit master if the EX32# signal is sampled inactive and the SLBURST# signal is sampled active at the beginning of a transfer. If EX32# and SLBURST# are sampled active at the beginning of the transfer, the BMIC will proceed with a 32-bit burst transfer.

In non-burst mode, the BMIC will respond as a 32-bit master. The BMIC will look for the EX32# signal at the beginning of the transfer to determine if the system memory it has addressed has the same bus width. If the EX32# signal is not returned (mismatched cycle indicated), the BMIC will "back-off" the bus by floating START#, IBE#<3:0>, and IDAT<31:0> to allow the 82358 EISA Bus Controller to take control of the transfer. The EISA Bus Controller will then proceed to assemble or disassemble the data as needed. The EISA Bus Controller will return the EX32# signal after the mismatched cycle is complete, indicating to the BMIC that a new address can be placed on the bus. If the EX32# signal is sampled active at the beginning of the transfer, the BMIC will proceed with a 32-bit non-burst (two BCLK) transfer.

4.2.2 1K PAGE ADDRESS BOUNDARY DETECTION

During burst, non-burst (two BCLK), and mismatched data cycles, the BMIC provides the support to detect 1K page address boundary crossings. If the BMIC detects that the current cycle is about to cross a 1K page boundary, the transfer will be temporarily terminated on the next cycle. The BMIC will then arbitrate between restarting the transfer on the current channel, selecting the second channel, doing a peek/poke cycle, or preempting the channel (refer to Section 4.4 for information regarding BMIC arbitration).

Example: Transfer = 32-bit transfer and page address boundary is at location 400h = 1024

1. The BMIC detects that the current cycle is about to cross a 1K page address boundary—current address (3FCh = 1020).
2. Address after BMIC has executed the current cycle (400h = 1024).
3. Transfer is temporarily terminated (interrupted).
4. BMIC will now arbitrate between restarting the transfer on a new page, selecting the second channel, doing a peek/poke cycle, or preempting the channel.

4.3 Peek/Poke, Locked Exchange Transfers

To allow the local processor to communicate with other devices in the main system, the BMIC allows the local processor to execute individual I/O or memory cycles over the EISA bus. These cycles can be thought of as being similar to "peek" and "poke" statements in the Basic programming language. These cycles may be reads, writes, or locked exchanges in 8-, 16-, 24-, or 32-bit values. All cycles must be contained within a single doubleword.

The Peek/Poke operation requires the following set of registers: Four 8-bit Peek/Poke Address registers which are combined to provide the 32-bit Peek/Poke address; One 8-bit Peek/Poke Control register which contains the bits defining whether the cycle is I/O or memory, peek (read)/poke (write) or locked exchange, and which byte enables are to be active during the cycle; and four 8-bit Peek/Poke Data registers which are used to hold the data for the Peek/Poke cycle. During all peek/poke or locked exchange cycles, byte enables IBE<3:0># are derived from bits 0–3 in the Peek/Poke Control register set. The lower two bits of the Peek/Poke Address register are ignored. Peek, poke, or locked exchange cycles will not be generated for illegal combinations of byte enables (i.e., 1111, 1010, 0110, 0101, 0100, 0010).

To do an individual write cycle (poke), the local processor must first write to the Peek/Poke Address register set to specify the 32-bit memory address or the 16-bit I/O address. It must then write the data to be transferred into the Peek/Poke Data register set. The data must be placed in the appropriate byte positions in the Data register set so that it goes out on the correct byte lanes during a 32-bit bus master transfer.

Once the appropriate data and address have been programmed, the local processor must write to the Peek/Poke Control register to specify the cycle type and initiate the cycle. After this write to the Peek/Poke Control register, bit 2 in the Local Status/Control register will be set to a 1 by the BMIC to indicate that a peek/poke request is pending and that the peek/poke registers are busy. When the poke cycle has finished executing on the EISA bus, the Peek/Poke status bit 2 in the Local Status/Control register will return to normal (0).

To do an individual read cycle (peek), the local processor must write to the Peek/Poke Address registers, then to the Peek/Poke control register to initiate the read cycle. The Peek/Poke status bit 2 in the Local Status/Control register will be set high by the BMIC and remain active until the peek cycle finishes on the EISA bus. The local processor can then read the data from the Peek/Poke data registers.

NOTE:
When running consecutive peek transfers, the data must be read from the Peek/Poke data registers before each new peek transfer is generated. The BMIC will read the data off the EISA bus from all four byte lanes regardless of which Byte enables (IBE<3:0>#) are active. (Although all bytes are read, the value of the byte enables are important to the system and must be programmed for the peek transfer).

When a locked exchange cycle is requested by the local processor, a peek cycle is scheduled first and then immediately followed by a poke cycle. The LOCK# signal is active during the locked exchange cycle to indicate to the system that no other accesses to the addressed location can be made.

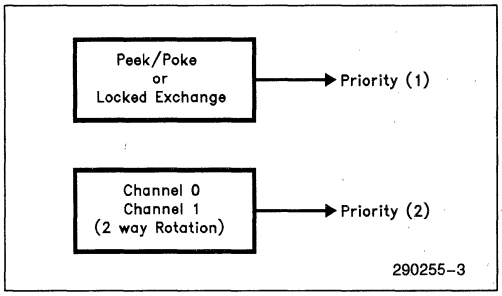
Whenever the BMIC is commanded to do an EISA POKE cycle, the BMIC will assert the MREQ# signal low normally, transfer up to four bytes of data, and release the bus by de-asserting MREQ# high. A potential problem exists, however, when the slave device extends the cycle by de-asserting EXRDY low. If the slave holds this signal low past the time that the BMIC is forced to release MREQ# high (it has been preempted while waiting for the slave to assert EXRDY high), then the BMIC will drive MREQ# back low again immediately after this cycle ends if there is another transfer pending (TBI, PEEK, POKE or LOCKED-EXCHANGE). Note that according to the EISA spec, MREQ* signal description "A bus master must wait at least two BCLKs after releasing the bus before reasserting its MREQx*". To adhere to EISA specifications, it is required that LOCKED-EXCHANGE cycles be used in lieu of POKE cycles.

Any consecutive Peek/Poke or Locked exchange transfers must be initiated only after the previous Peek/Poke or Locked exchange has been completed. This can be accomplished by making sure that bit 2 of the local status/control register is set to a zero before initiating the transfer.

4.4 Arbitration

4.4.1 EISA/BMIC ARBITRATION

The BMIC will begin master mode operation any time a transfer request is pending. If more than one transfer request is pending, the BMIC will service them in the following order. Peek/Poke cycles have the highest priority access to the EISA bus followed by the two data channels. Once the BMIC has gained control of the EISA bus, the BMIC will first perform any peek, poke, or locked exchange transfers that may be pending. If there are no peek, poke, or locked exchange transfers pending, the BMIC will run data transfers initiated by either of the two transfer channels. The two transfer channels have equal priority with respect to each other and are serviced in an alternating fashion. The priorities and assignments are as follows:



The BMIC will maintain ownership of the EISA bus until it has serviced all outstanding data transfer requests or it is preempted from the bus by the removal of the MAK# signal. The BMIC can be configured to relinquish the EISA bus immediately, 4 μs, or 8 μs after a preempt is received. If the BMIC has completed all outstanding data transfer requests prior to the time-out of the preempt timer, it will give up the bus. If the BMIC finishes one task prior to the time-out of the preempt timer, it will start on the next pending transfer request unless the request is a peek, poke, or locked exchange cycle. The BMIC will not start a set of peek, poke, or locked exchange cycles after the MAK# signal has been removed. If a transfer is cut-off due to a preempt timer time-out, the BMIC, upon regaining access to the EISA bus and following its internal arbitration priority scheme, will continue the transfer that was preempted at the point the transfer was cut-off.

When a channel is interrupted for any reason, 1K page break, FIFO stall, channel clear, channel suspend, or transfer complete, the BMIC may immediately relinquish the EISA bus depending on the state of the CFGFF bit in the Channel Configuration register set.

NOTE:
During a FIFO pause, the CFGFF bit in the associated Channel's Configuration register is ignored. The function of the CFGFF bit, as related to the above channel interruptions, is as follows:

If the CFGFF bit = 1, the BMIC will immediately relinquish control of the EISA bus upon the detection of any of the above interruptions. This will occur

regardless if there are additional data transfer requests pending. If there are additional data transfer requests pending, the BMIC will reassert MREQ# a minimum of two BCLKs later to reacquire the EISA bus. The BMIC will follow the arbitration priority scheme outlined above when servicing a data transfer request after a transfer interruption has occurred.

If the CFGFF bit = 0, the BMIC retains ownership of the EISA bus upon detection of a FIFO stall or 1K page break as long as a preempt timer timeout has not occurred. If there are additional data requests pending, the BMIC will immediately perform the pending transfer and then rearbitrate for the EISA bus to complete the interrupted transfer. If there are no additional data requests pending, the BMIC will relinquish ownership of the EISA bus only after the current transfer interruption has been serviced and completed.

4.4.2 BMIC PREEMPT TIMER

The BMIC can be preempted from the EISA bus by the 82357 (ISP). The 82357 negates MAK#, indicating to the BMIC that it must finish the current bus cycle and relinquish control of the EISA bus by negating MREQ# within 64 BCLK periods (8 μs).

The BMIC provides a programmable preempt timer which can be programmed to relinquish the bus within 3, 32, or 64 BCLKs. The preempt timer is programmable through the Global Configuration register.

The following diagrams illustrate the latest the BMIC will start a new transfer after MAK# has been negated.

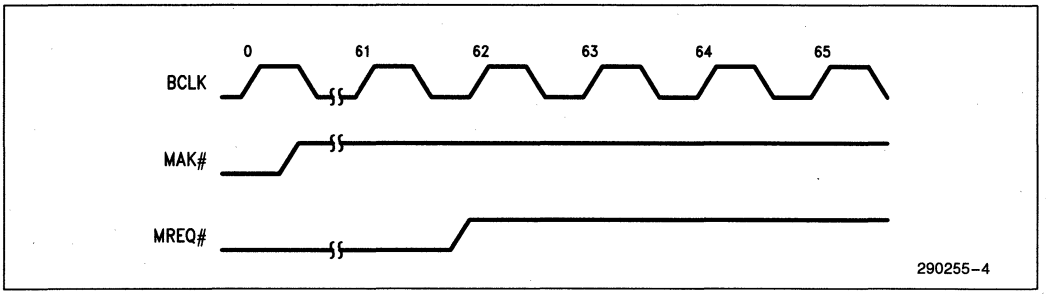
Depending on the type of transfer started, the BMIC will respond as follows:

Assumptions:

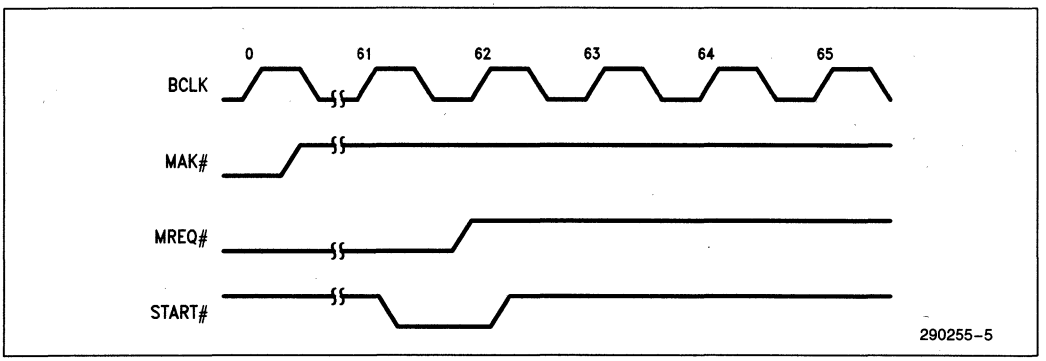
1. The 82357 has negated the MAK# signal at BCLK zero.
2. The preempt timer is programmed to relinquish the EISA bus within 64 BCLKs after the negation of MAK#.
3. Let X = programmed value of preempt delay (in BCLKs).

BMIC Response:

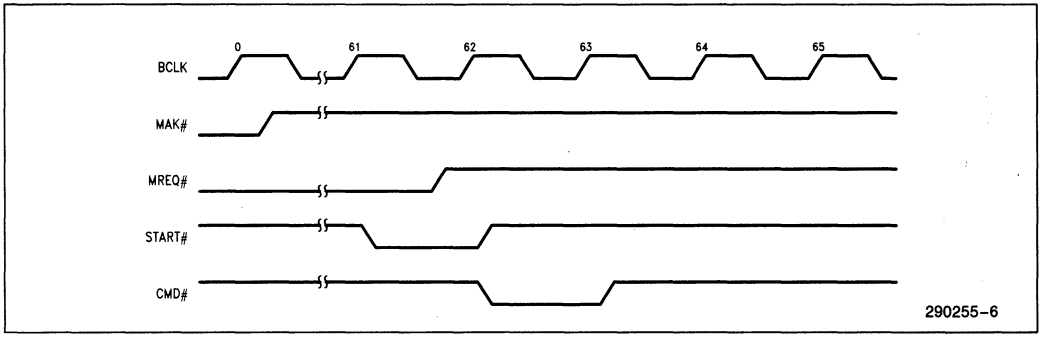
For all transfers, the BMIC will negate MREQ# within (X-2.5) BCLK periods following the MAK# transition to an inactive state (BCLK 61.5).



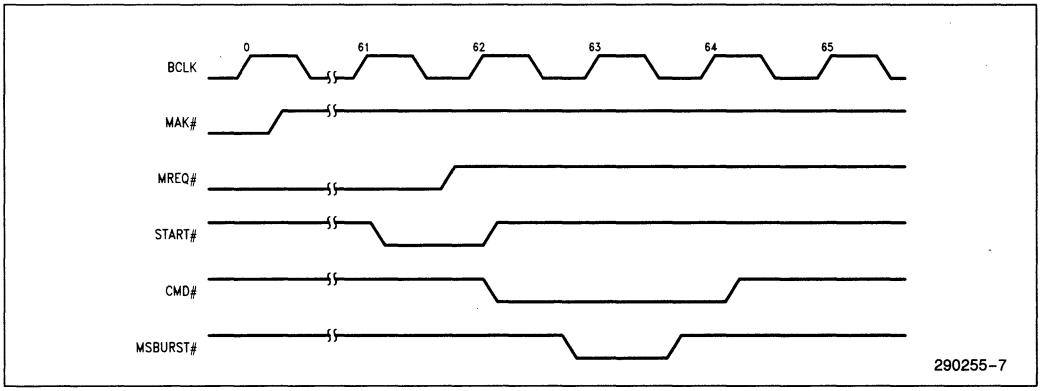
For all transfers, the BMIC may assert START# on any of the first X-3 rising edges of BCLK following the MAK# transition to an inactive state (BCLK 61).



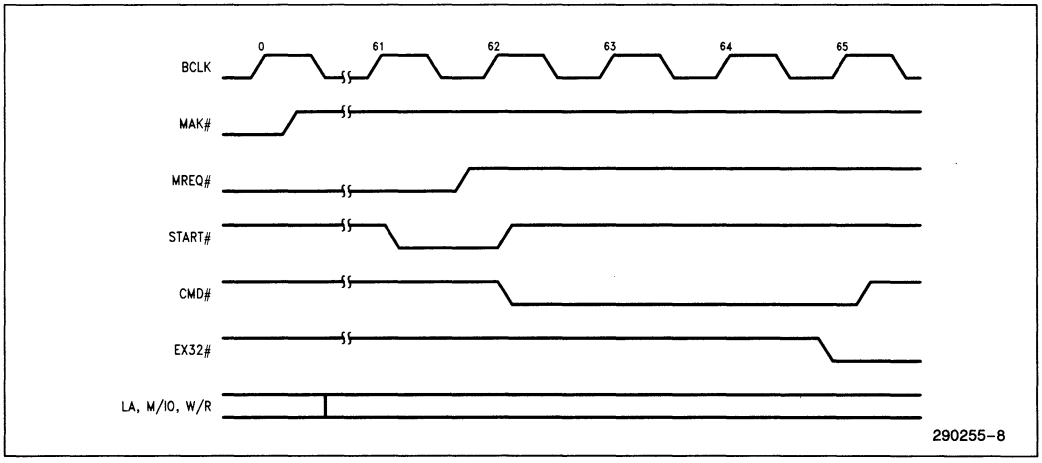
If the last cycle is a non-burst two BCLK cycle, CMD# will become inactive within (X-1) BCLK periods from the inactive transition of MAK# (BCLK 63), this is assuming that EXRDY is active.



If the last cycle is a burst EISA cycle, the BMIC will negate MSBURST# within (X-0.5) BCLK periods from the inactive transition of MAK# (BCLK 63.5). The last CMD# will go inactive within X BCLK periods from the deassertion of MAK# (BCLK 64). This is assuming EXRDY is active.



If the last cycle is mismatched, cycle completion will be controlled by the system. The BMIC will drive the LA address, M/IO, and W/R signals until the falling edge of BCLK after the last CMD# inactive transition.



4.5 EISA Address Incrementer

The Transfer Channel Current Address register set for each channel functions as an address incrementer and is used to generate and track the address of the data during transfers. The register set increments the address according to the number of bytes being transferred during that cycle. The transfer is automatically aligned on doubleword boundaries. The two least significant bits of the starting 32-bit address (A0 and A1) are used to determine the initial address increment value.

For 32-bit transfers, the BMIC provides an initial address increment of 1, 2, 3 or 4 depending on the value of address lines A<1:0>. After the initial increment, the BMIC increments the address by 4 until the last cycle is detected.

The following example illustrates the BMIC address incrementer during a 32-bit master mode transfer.

		EISA Address			
		A3	A2	A1	A0
Start Address	FFFFF001h	0	0	0	1
Initial Increment (Incremented by 3)	FFFFF004h	0	1	0	0
All Increments Following (Incremented by 4)	FFFFF008h FFFFF00Ch	1	0	0	0
		1	1	0	0

The starting address A<1:0> is 01, this means that the initial increment must be 3 in order to align the next increments on doubleword boundaries. The subsequent increments will be by 4 until the last cycle is detected.

For 16-bit transfers, the BMIC provides an initial address increment of 1 or 2 depending on the status of address lines A<1:0>. After the initial increment, the BMIC increments the address by two until the last cycle is detected.

The following example illustrates the BMIC address incrementer during a 16-bit master mode transfer.

		EISA Address			
		A3	A2	A1	A0
Start Address	FFFFF001h	0	0	0	1
Initial Increment (Incremented by 1)	FFFFF002h	0	0	1	0
All Increments Following (Incremented by 2)	FFFFF004h FFFFF006h	0	1	0	0
		0	1	1	0

The starting address A<1:0> is 01, this means that the initial increment must be 1 in order to align the next increments on singleword boundaries. The subsequent increments will be by 2 until the last cycle is detected.

NOTE:
The BMIC internally assembles 32-bit dwords. When a 16-bit burst transfer is preempted, the transfer will stop on a doubleword boundary.

4.6 EISA Byte Decrementer

The Transfer Channel Current Count register set for each channel contains the intermediate value of the byte count during the transfer and is used as the byte decrementer. The decrementer's function is partially based upon the address incrementer. In the above 32-bit incrementer example, the byte count would be decremented by 3 on the first cycle. After the initial decrement, the channel's Current Count register set is decremented by 4 until the last cycle is detected. In the above 16-bit incrementer example, the byte count would be decremented by 1 on the first cycle. After the initial decrement, the channel's Current Count register set is decremented by 2 until the last cycle is detected. Note that the Current Count register does not decrement entirely to zero. Instead, it retains the value of the number of bytes transferred during the last cycle.

4.7 EISA Address Incrementer/Byte Decrementer Illustration

The following table illustrates the various states of (A0, A1) vs the transfer byte-count and the initial address during a 32-bit transfer.

Byte Count	Starting Address	Next Address	Initial Increment	Number of Bytes Left	Last Cycle	Number of Cycles Left
1	XXX 0000	NA	NA	0	Yes	0
	XXX 0001	NA	NA	0	Yes	0
	XXX 0010	NA	NA	0	Yes	0
	XXX 0011	NA	NA	0	Yes	0
2	XXX 0000	NA	NA	0	Yes	0
	XXX 0001	NA	NA	0	Yes	0
	XXX 0010	NA	NA	0	Yes	0
	XXX 0011	XXX 0100	1	1	No	1
3	XXX 0000	NA	NA	0	Yes	0
	XXX 0001	NA	NA	0	Yes	0
	XXX 0010	XXX 0100	2	1	No	1
	XXX 0011	XXX 0100	1	2	No	1
4	XXX 0000	NA	NA	0	Yes	0
	XXX 0001	XXX 0100	3	1	No	1
	XXX 0010	XXX 0100	2	2	No	1
	XXX 0011	XXX 0100	1	3	No	1
5	XXX 0000	XXX 0100	4	1	No	1
	XXX 0001	XXX 0100	3	2	No	1
	XXX 0010	XXX 0100	2	3	No	1
	XXX 0011	XXX 0100	1	4	No	1
6	XXX 0000	XXX 0100	4	2	No	1
	XXX 0001	XXX 0100	3	3	No	1
	XXX 0010	XXX 0100	2	4	No	1
	XXX 0011	XXX 0100	1	5	No	2
7	XXX 0000	XXX 0100	4	3	No	1
	XXX 0001	XXX 0100	3	4	No	1
	XXX 0010	XXX 0100	2	5	No	2
	XXX 0011	XXX 0100	1	6	No	2
8	XXX 0000	XXX 0100	4	4	No	1
	XXX 0001	XXX 0100	3	5	No	2
	XXX 0010	XXX 0100	2	6	No	2
	XXX 0011	XXX 0100	1	7	No	2
9	XXX 0000	XXX 0100	4	5	No	2
	XXX 0001	XXX 0100	3	6	No	2
	XXX 0010	XXX 0100	2	7	No	2
	XXX 0011	XXX 0100	1	8	No	2
10	XXX 0000	XXX 0100	4	6	No	2
	XXX 0001	XXX 0100	3	7	No	2
	XXX 0010	XXX 0100	2	8	No	2
	XXX 0011	XXX 0100	1	9	No	3

NOTES:
1. "X" = Don't Care
2. If the "byte count" is less than or equal to the "initial increment", then the current cycle = the first cycle = the last cycle.
3. If the number of bytes left is less than or equal to 4, then the next cycle = the last cycle.
4. For information regarding byte alignment, refer to Section 6.3.1.

4.8 I/O Address Range Decode Support

The BMIC provides on-board decoder logic, two I/O select pins (IOSEL<1:0>#), and a set of 8-bit I/O Decode Range registers to support both general I/O decode and expansion board slot specific I/O decode. The BMIC also uses the AEN signal when decoding I/O locations.

The set of I/O Decode registers include two I/O Decode Range Base Address registers and two I/O Decode Range Control registers (refer to Section 8.2.6). The I/O Decode registers are used to define the address ranges of interest to the bus master expansion board. Each IOSEL#<1:0> pin has an associated Control and Base register along with an associated address range as defined by the I/O Decode register set.

Through the I/O Decode Range Control register set, the BMIC can be programmed to respond to a select I/O address range as either an 8-bit or 32-bit EISA device. The only control signal provided by the BMIC to the EISA bus during an I/O decode is the EX32# signal. The output state of the EX32# pin on the BMIC will indicate the elected response (low = 32-bit EISA, high = 8-bit EISA). The Control register set controls the size of the I/O decode range, the I/O decode type (slot specific or general I/O), and the I/O decode address latching. The I/O address can be latched by the CMD# signal (de-pipelined) or merely decoded. By latching the I/O address, the associated IOSEL# line will remain active a minimum of 5 ns from the rising edge of CMD#.

The IDOEs do not go active during an IOSEL cycle outside the shared register access space.

The I/O decode range size depends on the value of bits <4:0> in the Control register. Each of these bits masks a corresponding address comparison bit in the Base register. If no bits are masked in the Control register, the BMIC will decode a doubleword address. The bits are masked as follows:

I/O Control Register	I/O Base Register Bit Masked	EISA Address Bit Masked
Bit 0	Bit 0	IADS2
Bit 1	Bit 1	IADS3
Bit 2	Bit 2	IADS4
Bit 3	Bit 3	IADS5
Bit 4	Bit 4, 5	IADS<7:6>

The I/O Decode Range Base Address register contains the address range that is used during the I/O decode address comparison. The following table gives the bits in the I/O Base Address Register and the EISA Address that are used during the comparison:

I/O Base Address Register	(EISA Address Bits)	
	Slot Specific	General I/O
Bit 0	IADS2	IADS2
Bit 1	IADS3	IADS3
Bit 2	IADS4	IADS4
Bit 3	IADS5	IADS5
Bit 4	IADS6	IADS6
Bit 5	IADS7	IADS7
Bit 6	IADS10	IADS8
Bit 7	IADS11	IADS9

If bit 6 in the I/O Decode Range Control register is programmed for General I/O decode, and the two most significant bits in the I/O Decode Range Base Address register are programmed to 0 (IADS<9:8>), I/O decoding for that range will be disabled. This is done to ensure that the I/O address does not conflict with the slot specific address range or the EISA system board address range. The following table summarizes the EISA system I/O address mapping:

I/O Address Range (HEX)	I/O Range Reserved for
0000–00FF	EISA/ISA System Board
0100–03FF	General I/O (ISA Expansion Board)
0400–04FF	ISP (82357)
0500–07FF	General I/O (Alias of 0100h–03FFh)
0800–08FF	EISA System Board
0900–0BFF	General I/O (Alias of 0100h–03FFh)
0C00–0CFF	EISA System Board
0D00–0FFF	General I/O (Alias of 0100h–03FFh)
Slot Specific Range where X = Slot Number	
X000–X0FF	Slot (X)
X100–X3FF	General I/O (Alias of 0100h–03FFh)
X400–X4FF	Slot (X)
X500–X7FF	General I/O (Alias of 0100h–03FFh)
X800–X8FF	Slot (X)
X900–XBFF	General I/O (Alias of 0100h–03FFh)
XC00–XCFF	Slot (X) (BMIC Registers 0C80h–0CAFh)
XD00–XFFF	General I/O (Alias of 0100h–03FFh)

The following is an example of the BMIC programmed for slot specific decode:

I/O Decode Range 0 Control register programmed for (EFh)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(EFh)	1	1	1	0	1	1	1	1

— Bit 7—Respond as a 32-bit EISA slave
— Bit 6—Slot specific decode enabled
— Bit 5—Slot specific address latched by CMD#
— Bit 4—Compare I/O Decode Range 0 Base Address Bits (5) and (4) with EISA address signals IADS7 and IADS6 respectively
— Bit 3—Mask I/O Decode Range 0 Base Address Bit (3)
— Bit 2—Mask I/O Decode Range 0 Base Address Bit (2)
— Bit 1—Mask I/O Decode Range 0 Base Address Bit (1)
— Bit 0—Mask I/O Decode Range 0 Base Address Bit (0)

I/O Decode Range 0 Base Address register programmed for (2-h)

	IADS11	IADS10	IADS7	IADS6	IADS5	IADS4	IADS3	IADS2
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(2-h)	0	0	1	0	—	—	—	—

EISA slot specific address range decoded—X080h through X0BFh where X represents the expansion board slot number

```
      (X080h)                                  (X0BFh)
xxxx000010(00) (00)00throughxxxx000010(11) (11)11
           ↑   ↑                                ↑   ↑
                  EISA Address
                   Bits Masked
                  (IADS<5:2>)
```

Byte enables IBE<3:0># and EISA address lines IADS<1:0> are not used during either slot specific or general I/O decode. During slot specific I/O decode, EISA address lines IADS<9:8> must be 0 to ensure that the I/O address does not conflict with the ISA general I/O address range (0100h–03FFh).

IOSEL0# and EX32# will be driven low by the BMIC if addresses X080h through X0BFh are present on the EISA bus.

AEN is used as part of the decode and must be negated low when a response from the BMIC is required.

5.0 TRANSFER BUFFER INTERFACE

5.1 Transfer Buffer Interface Signals

The Transfer Buffer Interface portion of the BMIC provides the signals essential for interfacing to the expansion board as required for EISA-to-expansion board and expansion board-to-EISA burst data transfers. The Transfer Buffer Interface is designed to interface to a high speed transfer buffer and simple logic similar to that used in traditional DMA designs. This interface includes a 16-bit data bus, one clock input, and seven control signals.

The 16-bit data lines TDAT<15:0> are used by the BMIC to transfer the data to and from the transfer buffer logic on the expansion board during transfers. The data is word aligned. The BMIC automatically assembles the words received from the expansion board into 32-bit dwords for 32-bit transfers over the EISA bus. The data lines are also used by the BMIC to transport internally generated transfer start and real-time addresses to the external logic for use during data transfers (refer to Section 5.3).

The clock input (TCLK) controls the transfer rate between the BMIC and the external transfer buffer logic. The TCLK can be asynchronous to the BCLK.

The seven control signals include:

— Transfer Request (TRQ#): an output to request data transfers over the Transfer Buffer interface.
— Transfer Acknowledge (TACK#): An input to acknowledge data transfers. The TACK# signal may be used by the transfer buffer logic to add wait states to the data cycle.
— Data Transfer Direction (TDIR): An output to inform the external transfer buffer logic as to the direction of the current transfer (EISA read or EISA write).
— Transfer Channel Select (TCHAN): An output to indicate which of the two channels is currently active.
— Transfer Address Counter Load (TLD#): An output to load the current transfer start address to an external address counter, depending on the expansion board application.
— Transfer Data Output Enable (TDOE#): An input that unconditionally disables the BMIC from driving the TDAT<15:0> lines. With this signal, the BMIC can be prevented from driving the TDAT<15:0> lines while the local processor accesses the transfer buffer logic on the expansion board. No handshaking is required, so throughput is increased.
— Transfer End-of-Process (TEOP#): TEOP# is a status output pin that signals the end of a data transfer to the external transfer buffer logic.

NOTE:
Refer to Section 9.4 for additional information regarding the above signals.

5.2 External Transfer Buffer Logic

The Transfer Buffer interface is designed for high speed devices, such as SRAM based designs, or FIFOs. The Transfer Buffer interface data path is 16 bits wide. This requires the transfer clock (TCLK) to run at a speed of 16 MHz to 20 MHz to maintain the EISA maximum data rate of 33 Mbytes/sec. The fast cycle times required on the data Transfer Buffer interface can be implemented in the controlled environment found locally on the expansion board. If two BCLK transfers are used on the EISA side (16 Mbytes/sec), the timing requirements for the transfer buffer can be relaxed, and lower cost implementations can be utilized.

If the transfer buffer controller does dynamic arbitration for the transfer buffer between the BMIC and the peripheral device(s) on the expansion board, the peripheral device accesses should be short enough so that the BMIC's data FIFO can handle the interruption to its data flow without stalling the EISA transfer.

Examples of transfer buffer architecture implementations that could be interfaced to the BMIC include:

— A FIFO implementation which is large enough to buffer the difference in throughput rates between the peripheral device on the expansion board and the EISA Bus. See Section 5.2.1.

— A small high-speed DMA like device that generates addressing for a SRAM based transfer buffer.

— A controller implementation for dual-ported SRAM for high transfer buffer bandwidth.

— A page or nibble-mode dynamic-RAM controller implementation for large, low cost transfer buffers.

— For graphics systems, the frame buffer itself can be used for the transfer buffer with a non-linear address generator for transferring windows in the screen image.

5.2.1 FIFO IMPLEMENTATION

During EISA writes, the BMIC will overread the transfer buffer (read data beyond the number of bytes to be transferred) by a maximum of 28 bytes. These overread bytes may contain valid data (back to back transfers) which will be lost. The data loss can be avoided through software or hardware. The software solution avoids back to back transfers. This implies that there is data for only one transfer in the FIFO at any given time.

The hardware solution requires an external 22-bit Byte Counter and a Flip-Flop. The terminal count of the Byte Counter is used to SET the Flip-Flop which disables BMIC reads to the FIFO. The BMIC will continue to read (overread) "stale" data. The BMIC TEOP# output signal is used to RESET the Flip-Flop enabling BMIC reads to the external FIFO.

5.3 Transfer Interface Start Address Generation

The BMIC provides four 8-bit Transfer Buffer Interface (TBI) registers, two Base and two Current registers, which can be programmed with 16-bit transfer start addresses. Each transfer channel has an associated Base and Current register pair. The Base registers contain the start address and the Current registers provide the real-time address used to track the current transfer. The Current registers will increment by one each time a 16-bit word is transferred across the Transfer Buffer interface.

The 16-bit start address is transferred across the TDAT<15:0> lines to the transfer buffer logic at the beginning of all new data transfers (i.e., each time the TBI Base register set contents are transferred to the TBI Current register set). The contents of the TBI Base registers are transferred to the TBI Current registers after a write to the associated channel's Transfer Strobe register is completed (refer to Section 4.2). The BMIC provides a load signal (TLD#) which can be used to latch the start address into an external address counter for use by the transfer buffer logic.

The BMIC can also be programmed to generate the transfer address each time the associated channel regains the bus, in which case, the address will be the real-time address. By programming the CFGEA bit in the Channel Configuration register to a "1", the start address will be transferred to the transfer buffer logic at the beginning of all new transfers and the real-time address will be transferred each time the associated channel regains the bus. If the CFGEA bit is set to a "0", the transfer start address will be transferred at the beginning of all new transfers and the real-time address will not be transferred.

NOTE:
The TBI Current register set is readable by the local processor. However, there are possible coherency problems involved with reading multiple bytes while the current registers are being updated during a transfer. To avoid these problems, the channel's transfer should be temporarily suspended (using the channel's Configuration Register) before trying to read the channel's TBI Current register set.

5.4 Transfer Buffer Interface Timing Example

Figures 5-1 and 5-2 illustrate the start up and conclusion of a transfer cycle across the Transfer Buffer interface and should be used as a reference when reading the following text.

1. At the start of a data transfer TCHAN and TDIR change to their new values prior to the falling edge of TLD# to set up the cycle. TCHAN and TDIR will not change states as long as TRQ# is asserted.
2. TLD# is asserted until acknowledged by TACK#. The transfer address is transferred to the external logic each time the TBI Base register contents are transferred to the TBI Current register set (new transfer) and, if programmed, each time the current channel regains the bus.
3. The new address is loaded using the TDAT bus during TLD# at point (A). The TDAT bus should be turned on by asserting TDOE# during TLD# if the internal start address is required. Once the external channel address and direction are set up, the data transfer can begin.
4. Data transfer requests are signaled by TRQ# being asserted (low). TRQ# will remain active until the data transfer is completed or a transfer interruption occurs (refer to Section 1.0) followed by TACK# active. During an EISA write, there will be a one TCLK delay between TLD# deasserting and TRQ# asserting as denoted by point (D) in Figure 5-2. This is to allow time for the external buffers to change direction after the TLD# has been completed.
5. Each word transfer to or from the BMIC is acknowledged by the TACK# signal. If TACK# is active at the rising edge of TCLK, one word will be transferred. If TACK# is not active at the rising edge of TCLK, the word that is currently being transferred will be inhibited and a wait state will

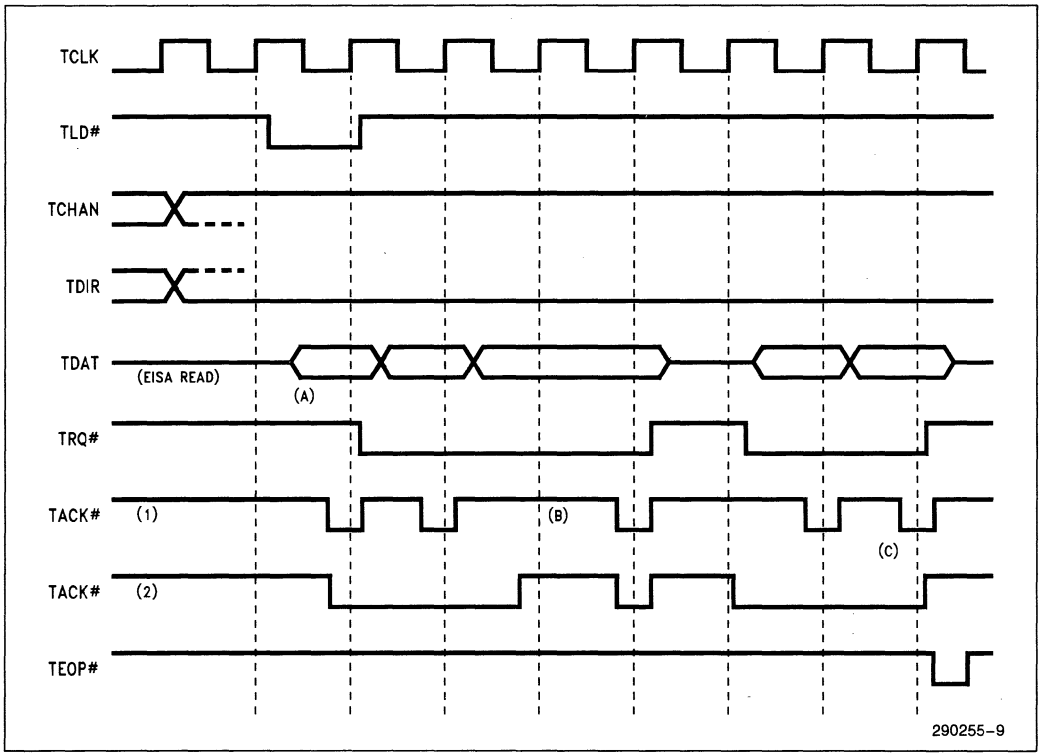


Figure 5-1. Transfer Buffer Interface Timing (EISA READ)

be inserted. This is shown at point (B) in Figure 5-1. Such a wait may be needed when the external transfer buffer logic is arbitrating between the BMIC and the I/O subsystem on the expansion board. Wait states may also be inserted by stretching TCLK at point (C) in both of the figures. Clock stretching is possible as long as the one to one ratio of TCLK to BCLK is not violated.

NOTE:
A long TCLK stretch time will hang the Transfer Buffer interface. Also, TCLK must be running during the time TRQ# is inactive in order for the Transfer Buffer interface to function properly.

As indicated above, TACK# must be stable at the rising edge of TCLK. However, TACK# can assume any convenient pattern at other times. As shown by the first pattern, TACK# (1) pulses low at the TCLK edge that data is transferred. This pattern is particularly useful when TCLK wait-states are desired as indicated at point (B) in Figure 5-1. The alternate pattern (TACK#2) is useful during TCLK stretching since TACK# is always low during TRQ# as shown at point (C). This is effective since the transfer clock edge timing is controlled by the amount TCLK is stretched.

6. TEOP# is asserted at the end of a transfer by the BMIC.

   The BMIC will indicate end-of-process by asserting TEOP# shortly after the negation of the last CMD# in the transfer. During an EISA write transfer, the BMIC will assert TEOP# a maximum of two TCLKs after CMD# is negated. During an EISA read transfer, the BMIC will assert TEOP# typically eight TCLKs after the negation of CMD#. In either case (EISA read or EISA write), the TEOP# signal is delayed from the rising edge of TCLK.

NOTE:
The BMIC will assert the expansion board interrupt signal (LINT) at the end of a transfer, if so programmed in the Transfer Channel Configuration register.

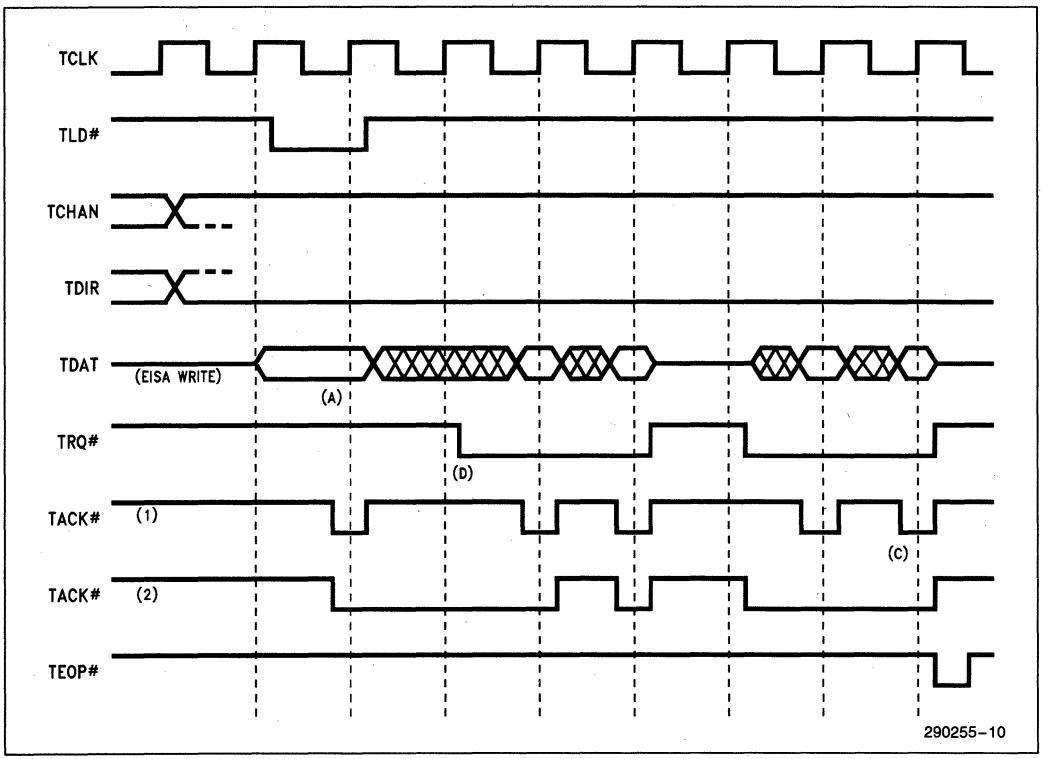


Figure 5-2. Transfer Buffer Interface Timing (EISA WRITE)

6.0 FIFO/DATA ALIGNER

6.1 FIFO/Data Aligner

The BMIC uses two identical FIFOs, one per transfer channel, and a common data aligner for data transfers between system memory and the bus master expansion board. The primary function of the FIFO/Data Aligner Unit is to help isolate and simplify the timing relationships between the EISA bus and the devices on the expansion board.

The FIFO allows the timing on the expansion Board side of the BMIC to be based on a locally generated clock signal. This transfer clock (TCLK) can be independent of the EISA BCLK signal that governs EISA bus timing. The FIFO also provides latency protection for wait states generated on either the EISA bus or expansion board.

The Data Aligner arranges the 16-bit data from the external transfer buffer to any arbitrary byte alignment in system memory. The data aligner also performs the assembly and disassembly of the EISA data during the transfer. The TDAT data assembly and disassembly is done by the Transfer Buffer interface portion of the BMIC.

6.2 FIFOs

Each FIFO on-board the BMIC is 24 bytes in size. The transfer data is written into the FIFOs from either the expansion board or the EISA bus side, depending on the direction of transfer. The data is written into the FIFO as doublewords during the transfer. However, if the data is not doubleword aligned, partial FIFO loads will be done at the beginning or end of a transfer depending on the byte count, address programmed and the direction of the transfer.

The condition of the FIFOs can be determined by a read to the Transfer Channel Status register set. A read to this register will indicate whether the FIFOs are stalled or active. A FIFO stall is defined as a FIFO that is full during an EISA read or empty during an EISA write. In either case, the transfer buffer logic is unable to keep up with the EISA device. If a FIFO stall occurs, the transfer will be stopped and the BMIC will either service the transfer request with the highest priority or relinquish the EISA bus to the system. The BMIC will relinquish the bus to the system if the CFGFF bit in the channel's corresponding Configuration register is set to a 1.

6.3 Data Aligner

6.3.1 EISA BYTE ALIGNMENT

The BMIC automatically handles the byte alignment for the EISA bus in the case of misaligned doubleword boundaries and assumes no performance penalty. The BMIC will do any partial doubleword transfers as required at the beginning and the end of all transfers. The two least significant bits of the 32-bit transfer start address (A1 and A0) are used to provide the byte alignment for both EISA read and EISA write transfers. The following tables illustate the BMIC's byte alignment approach during 32- and 16-bit transfers:

In the following tables "—" represents no data transferred and the digits represent the data items being transferred. The byte alignment for an EISA read is identical to that of an EISA write.

EISA Write (32-bit/12-byte Transfer) and (16-bit/6-byte Transfer)

		(32-Bit)				(16-Bit)			
A1	**A0**	**Output Data to EISA Bus**				**Output Data to EISA Bus**			
Byte Lane	→	**3**	**2**	**1**	**0**	**3**	**2**	**1**	**0**
0	0	03	02	01	00	—	—	01	00
		07	06	05	04	—	—	03	02
		11	10	09	08	—	—	05	04
0	1	02	01	00	—	—	—	00	—
		06	05	04	03	—	—	02	01
		10	09	08	07	—	—	04	03
		—	—	—	11	—	—	—	05
1	0	01	00	—	—	—	—	01	00
		05	04	03	02	—	—	03	02
		09	08	07	06	—	—	05	04
		—	—	11	10	—	—	—	—
1	1	00	—	—	—	—	—	00	—
		04	03	02	01	—	—	02	01
		08	07	06	05	—	—	04	03
		—	11	10	09	—	—	—	05

6.3.2 DATA ASSEMBLY/DISASSEMBLY

Before being placed on either the TDAT or IDAT data buses during an EISA read or EISA write, the data will be assembled or disassembled as required. The IDAT data is assembled and disassembled by the FIFO/data aligner portion of the BMIC and the TDAT data is assembled and disassembled by the Transfer Buffer interface portion of the BMIC. The following paragraphs illustrate the BMIC's assembly and disassembly approach during 32- and 16-bit transfers. The illustration assumes that byte alignment is not required.

During 32-bit EISA read transfers, the 32-bit doublewords are removed from the EISA bus and placed into the FIFO. After flowing through the FIFO, the 32-bit doublewords are copied-down to 16-bit words and then placed on the TDAT bus.

During 32-bit EISA write transfers, the 16-bit words are removed from the TDAT lines, assembled into 32-bit doublewords, and then placed into the FIFO. After flowing through the FIFO, the 32-bit data is placed on the EISA bus. No further assembly or disassembly is required after the FIFO as the data is already in 32-bit doubleword form.

During 16-bit EISA read burst transfers, the 16-bit words are removed from the EISA bus, assembled into 32-bit doublewords, and then placed into the FIFO. After flowing through the FIFO, the 32-bit data is copied-down to 16-bit words and then placed on the TDAT bus.

During 16-bit EISA write burst transfers, the 16-bit words are removed from the TDAT bus, assembled into 32-bit doublewords, and then placed into the FIFO. After flowing through the FIFO, the 32-bit data is copied-down to 16-bit words and then placed on the EISA bus.

7.0 LOCAL PROCESSOR INTERFACE

The BMIC's Local Processor interface is based on an asynchronous, 8-bit interface. All of the slave signals required for a local processor to program the BMIC are provided through this interface. These signals include (LCS#, LRD#, LWR#); two address lines (LADS0 and LADS1) for addressing internal registers; an 8-bit data path (LDAT); an interrupt signal (LINT); and a ready signal (LRDY). LINT allows the BMIC to interrupt the local processor and the ready signal (LRDY) indicates when valid data is available on the LDAT lines (shared register accesses only, see below). If a local processor is not used, the Local Processor interface can be connected to the 8-bit ISA bus (refer to Section 7.3). The choice of the local microprocessor or microcontroller used depends upon the specific application and the degree of performance and data processing needed (refer to Section 7.2).

The Local Processor interface portion of the BMIC contains two 8-bit registers which are used by the local processor to access all of the BMIC's internal registers. These registers are mapped into the Local Processor interface and include a Local Data register and a Local Index register. These registers are selected using the Local Processor interface's two address lines. The Local Status/Control register is also directly mapped into the Local Processor interface and is used to provide the local processor with the interrupt, peek/poke, and Base register status.

The BMIC allows the local processor and the EISA bus to communicate with each other through a set of Command/Status registers. The Command/Status registers are referred to as shared registers and include a set of Mailbox registers, Semaphore ports, and doorbell registers. The mailbox registers are used to pass messages to and from the local processor and the EISA bus and are controlled by the Semaphore ports. The Doorbell register set is used to inform the respective processor of new messages. Also part of the shared register set are the ID registers, which are used to support the EISA expansion board ID function.

The BMIC allows the local processor access to individual locations in system memory or I/O space using the Peek/Poke feature. The local processor can also initiate BMIC burst and non-burst (two BCLK) data transfers to and from system memory.

7.1 Shared Registers—Status/ Command Support

As data transfer rates increase, it is critical that an efficient command and status passing mechanism be implemented so that command and status exchange does not become a new bottleneck to system performance. The BMIC utilizes a high-performance command/status interface between the main system and the local processor to minimize command/status overhead.

The Shared registers are a group of registers accessable by the system CPU or EISA bus master and the local processor for general-purpose command and status interactions and EISA expansion board ID function support. The features of the BMIC command/status support include a pair of semaphore ports, a set of interrupt ports ("doorbell registers"), and a set of mailbox registers. With these functions, many different types of high-performance communication protocols can be defined between the system and the expansion board. The Global

Configuration register, the System Interrupt Enable/Control register, and the ID registers are also part of the shared register set.

7.1.1 SEMAPHORE PORTS

The two semaphore ports are specifically designed to allow set-and-test functions in I/O space. Specifically, the ports are used to lock access to the mailbox registers and to lock access to links in main memory. Each of the semaphore ports consists of two parts: the semaphore flag bit and the semaphore test bit.

When a write occurs to the semaphore flag bit through either the EISA interface or the Local Processor interface, the old value of the semaphore flag bit is copied to the appropriate semaphore test bit. The old value of the semaphore flag bit is then available in the test bit to be read back by the processor. If the value read back from the semaphore test bit is a "1", the requested resource is unavailable for use. If the value read back is a "0", the requested resource is available for use and is now locked by the requesting processor or bus master. In this manner, set-and-test algorithms can be implemented without using the EISA bus lock function. The processor or EISA bus master unlocks the semaphore by simply writing a "0" to the associated semaphore flag bit.

NOTE:
The Semaphore ports and resources are locking only in a software sense, as in any semaphore in main memory. The Semaphore ports are identical and are not associated with either interface (EISA or Local). The protocol for the semaphores and the effect they have on other shared registers, like the Mailbox registers, is strictly a matter of how the system software chooses to use them.

Implementing the semaphore in the BMIC instead of main memory eliminates the need for the BMIC to arbitrate for the EISA bus every time it wishes to update or test the semaphore. Note that the semaphore scheme described here is functional only when a single device on the EISA is communicating with the BMIC; the semaphore coordinates "locks" between the single device and the local processor. In the case that multiple masters attempt to lock access to the BMIC, the masters must first agree amongst themselves which one has the privilege to use the BMIC semaphore port(s).

7.1.2 MAILBOX REGISTERS

A set of 16 8-bit general-purpose mailbox registers are used to pass information between the bus master expansion board and the EISA system. The 16 registers are mapped contiguously in EISA slot-specific I/O space, so they can be accessed as bytes, words, or doublewords. These registers can be used to directly pass command and status information, or they can be used as pointers to larger command blocks in memory.

The mailbox registers can be read or written at any time from either the EISA bus or the Local Processor interface. An internal arbitration is implemented in such a way that if there is a simultaneous read and write from both sides of a mailbox register, then the read operation will not contain indeterminate bits. In other words, when a read operation is done on a mailbox register at the same time as a write operation to that register, the bit pattern that is read will be either the old bit pattern in the mailbox, or the new bit pattern being written, but never some transitory, invalid bit pattern.

7.1.3 DOORBELL REGISTERS

There are two 8-bit doorbell Interrupt/Status registers in the BMIC, one assigned to the EISA side and one assigned to the expansion board side. The EISA System Doorbell register is used by the local processor to request service from the EISA side and the Local Doorbell register is used by the device on the EISA side to send an interrupt request to the local processor on the bus master expansion board. The doorbell Interrupt/Status registers are implemented with "sticky" bits, so that individual bits in the register can be set by the interrupting device or reset by the servicing device without knowledge of the states of the other bits in the register. The eight bits in each doorbell register allow up to eight separate devices or events in each direction to have interrupt requests pending simultaneously. The interrupt requests pending in either of the two Doorbell registers are ORed with the other interrupt sources from within the BMIC, and the result is sent out over one of the two interrupt pins: LINT or EINT.

Each doorbell register has an associated 8-bit Interrupt Enable register used to enable or disable the interrupts on an individual basis. The BMIC also includes a System Interrupt Enable/Control register and a Local Status/Control register used to disable the system (EINT) and local (LINT) interrupts and to verify the status of the system and local interrupts on a global basis (refer to Sections 8.1.1.3.3 and 8.2.2).

The following paragraphs describe the operation of the Local Doorbell Interrupt/Status register. The EISA System Doorbell Interrupt/Status register is similar, but operates in the opposite direction.

Each device or event that can interrupt the bus master expansion board can be assigned a bit position within the BMIC's Local Interrupt/Status Doorbell

register. When the device on the EISA bus wants to send an interrupt request to the bus master expansion board, it writes to the Local Interrupt/Status Doorbell register (from the EISA side) with that device's assigned bit position set active. This will set that bit in the Local Interrupt/Status Doorbell register, but leave the other bits in the register unaffected. If that bit position is not disabled, then the interrupt signal to the local processor will be asserted.

When the local processor services the interrupt, it checks the Local Status/Control Register to determine the source of the interrupt. If the control register indicates that the Local Doorbell register is one of the active interrupt sources, then the local processor can read the Local Doorbell register to determine which bits are active and requesting interrupts. If the local processor decides to service one of the requests from the Local Doorbell register, it can write to the Local Doorbell register with that bit's position set. This action will cause that bit in the Local Doorbell register to reset, but the other bits will remain unaffected. Thus, each bit in the Local Doorbell register is like a set-reset flip-flop, with the EISA bus controlling the "set" input, and the Local Processor interface controlling the "reset" input.

7.2 Local Processor Recommendations

The Local Processor interface to the BMIC will support numerous processors, from the 8088 microprocessor to the 376 embedded processor.

The 80186, 80C186, 80188, and 80C188 family of processors provides a clean interface to the BMIC's Local Processor interface and eliminates the need for additional logic. An on-board programmable wait-state generator eliminates the need for external wait-state generation logic between the processor and the BMIC during non-shared register accesses.

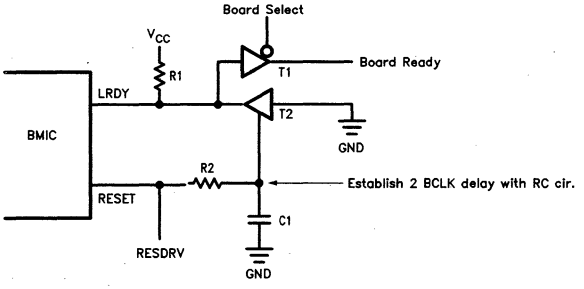
7.3 Requirements for No Local Processor

The BMIC allows for expansion board designs that do not require a local processor. To support the programming of the BMIC in a no local processor board design, the Local Processor interface must be connected to the ISA bus. However, when the ISA bus is used, the BMIC must be informed that there is no local processor and that it must change its function slightly (refer to next section). To inform the BMIC that no local processor is present, LRDY must be driven low during RESET and remain low a minimum of two BCLKs after RESET is negated.

The following circuit can be used to establish the proper LRDY/RESET timing as required for a no local processor design (see Figure 7-1).

7.4 EISA ID Function Support/ Registers

The BMIC provides support for the EISA expansion board ID function. The primary ID implementation takes advantage of the local processor. Upon reset, the local processor executes a routine from its ROM that writes the product identifier for the expansion board to the four 8-bit ID registers in the BMIC. The registers are accessed through the Local Processor interface and are located at local index addresses 00h–03h. On the EISA side, these registers are mapped into the EISA slot specific ID address range XC80h–XC83h.



R1 = 8.2K
R2 = Depends on frequency of BCLK and application implemented.
C1 = Depends on frequency of BCLK and application implemented.
T1 = Active low tri-state buffer
T2 = Active high tri-state buffer

Figure 7-1. LRDY/RESET Circuit with No Local Processor

If the host CPU accesses the ID registers in the BMIC before the local processor has programmed them, the BMIC will return the setup delay ID code 0111XXXXh in the byte 0 ID register located at EISA slot specific I/O address XC80h. The byte 0 ID register should be programmed last by the local processor.

If a local processor is not used, external registers will have to be implemented on the expansion board to hold the expansion board ID value. The BMIC will automatically set its I/O Decode Range 0 Control register to decode 8-bit EISA ID addresses. The IOSEL0# output signal can then be used to trigger external logic on the expansion board to enable ID data onto the IDAT<7:0> data lines. The ID register must be connected as shown in Figure 7-2. The external logic should monitor SA1 and SA0 on the ISA bus to determine which data byte to drive.

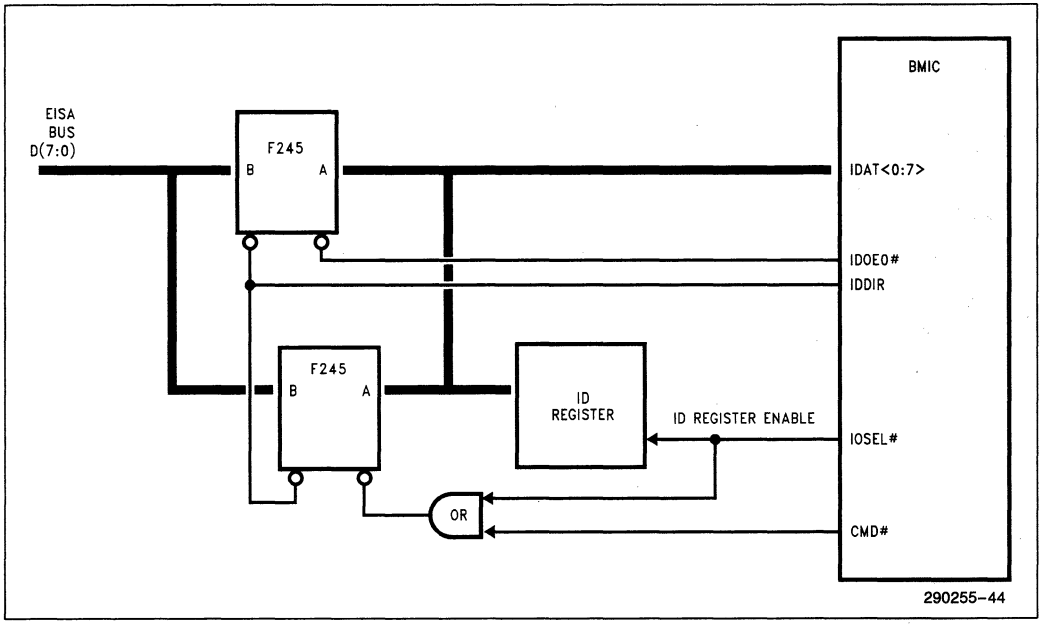


Figure 7-2. IDOE0# Connection during ID Register Access

8.0 REGISTER DESCRIPTION

8.1 Shared Register Description

The following is a table of the Shared register group listing the number of registers, register type (read/write) as related to the local and EISA side, register name, and register size:

Number	EISA	Local Type	Register Name Type	Active Bits per Register
2	R/W	R/W	Semaphore Register	2 Bits
16	R/W	R/W	Mailbox Register	8 Bits
1	R/W	R/W	Local Doorbell Interrupt/Status Register	8 Bits
1	R	R/W	Local Doorbell Enable Register	8 Bits
1	R/W	R/W	EISA System Doorbell Interrupt/Status Register	8 Bits
1	R/W	R	EISA System Doorbell Enable Register	8 Bits
1	R/W	R	System Interrupt Enable/Control Register	8 Bits
1	R	R/W	Global Configuration Register	8 Bits
4	R	R/W	ID Register	8 Bits

8.1.1 COMMAND/STATUS SUPPORT REGISTERS

8.1.1.1 Semaphore Ports (Read/Write)

The BMIC contains two Semaphore ports which can be used to software lock resources between the EISA bus and the local processor. Each semaphore port controls a 1-bit semaphore flag. Upon reset, the Semaphore ports are reset to 0.

Semaphore Port 0 EISA Address—XC8Ah
Semaphore Port 0 Local Index Address—0Ah

Semaphore Port 1 EISA Address—XC8Bh
Semaphore Port 1 Local Index Address—0Bh

						Bit 1	Bit 0
—	—	—	—	—	—		

Bit 7–2 —Reserved, set to 0

Bit 1 —Semaphore Test bit (Read Only)

Bit 0 —Semaphore Flag bit (Read/Write)

Bit (0) reflects the actual value of the semaphore at any given instant. Whenever a write is done to the Semaphore Flag bit (0), its previous value is simultaneously copied to the Semaphore test bit (1). Internal to the BMIC, there are two test bits for each semaphore port: one for the EISA interface and one for the Local Processor interface. To do a test-and-set function, write to the semaphore port with the desired semaphore value in the flag bit. After a write has been completed, read the semaphore port and check the test bit to verify that a collision did not occur.

8.1.1.2 Mailbox Registers (Read/Write)

The mailbox registers are sixteen 8-bit, general purpose registers. The format of the contents of the mailbox registers is user-defined. The Mailbox register set is not initialized to a fixed value upon reset.

EISA Address—XC90h through XC9Fh
Local Index Address—10h through 1Fh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

8.1.1.3 Doorbell Registers

8.1.1.3.1 Local Doorbell Interrupt/Status Register (Read/Write)

This register is implemented with "sticky" bits (refer to Section 7.1.3). The Local Doorbell Interrupt/Status register is used by the EISA bus to send an interrupt request to the expansion board. When read from, this register indicates the status of pending interrupt events. Upon reset, the Doorbell Interrupt/Status register is reset to 0.

EISA Address—XC8Dh
Local Index Address—0Dh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7–0 1 = Doorbell interrupt pending (local CPU read)

Set Doorbell bit (EISA write)

Reset Doorbell bit (Local CPU write)

0 = No doorbell interrupt pending (Local CPU read)

No action (EISA or local CPU write)

Bits 0–7 allow up to eight events or devices on the EISA side to interrupt the local side of the BMIC. The above bits can only be reset by the servicing processor on the local side.

8.1.1.3.2 Local Doorbell Enable Register (Read/Write)

The Local Doorbell Enable register is used by the local processor to enable or disable interrupt requests to the local expansion board. This register is read only from the EISA side. Upon reset, the Doorbell Enable register is set to 0.

EISA Address—XC8Ch
Local Index Address—0Ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7–0 1 = Enable doorbell interrupt for corresponding bit position

0 = Disable doorbell interrupt for corresponding bit position

No action (local CPU write)

Bits 0 through 7 act as interrupt enables for bits 0 through 7 in the Local Doorbell Interrupt/Status register respectively.

8.1.1.3.3 EISA System Doorbell Interrupt/Status Register (Read/Write)

This register is implemented with "sticky" bits (refer to Section 7.1.3). The EISA System Doorbell Interrupt/Status register is used by the expansion board to send an interrupt request to the EISA bus. When read from, this register indicates the status of pending interrupt events. Upon reset, the EISA System Doorbell Interrupt/Status register is reset to 0.

EISA Address—XC8Fh
Local Index Address—0Fh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7–0 1 = Doorbell interrupt pending (EISA read)
Set Doorbell bit (Local CPU write)
Reset Doorbell bit (EISA write)
0 = No doorbell interrupt pending

Bits 7–0 allow up to eight events or devices on the expansion board to send interrupts to the EISA bus. The above bits can only be reset by the servicing processor on the EISA side.

8.1.1.3.4 EISA System Doorbell Enable Register (Read/Write)

The EISA System Doorbell Enable register is used by the EISA processor to enable or disable interrupt requests to the EISA side. This register is read only from the local side. Upon reset, the EISA System Doorbell Enable register is reset to 0.

EISA Address—XC8Eh
Local Index Address—0Eh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7–0 1 = Enable doorbell interrupt for corresponding bit position
0 = Disable doorbell interrupt for corresponding bit position

Bits 0 through 7 act as interrupt enables for bits 0 through 7 in the EISA System Doorbell Interrupt/Status register respectively.

8.1.1.3.5 System Interrupt Enable/Control Register (Read/Write)

This register is used by the processor on the EISA side to disable the EINT signal. The EISA processor also can read this register to determine whether there are any pending interrupt requests in the EISA System Doorbell Interrupt/Status register. This register is read only from the local side. Upon reset, this register is reset to 0.

EISA Address—XC89h
Local Index Address—09h

—	—	—	—	—	—	Bit 1	Bit 0

Bit 7–2 — Reserved, set to 0
Bit 1 — (read-only bit)
1 = Enabled interrupts are pending in EISA System Doorbell Interrupt/Status register
0 = No enabled interrupts are pending in EISA System Doorbell Interrupt/Status register
Bit 0 —
1 = Enable interrupts from System Doorbell register (EISA write)
0 = Disable interrupts from System Doorbell register (EISA write)

8.1.2 GLOBAL CONFIGURATION REGISTER (READ/WRITE)

This register is used to program the type of protocol, edge or level-triggered, that will be used with the EINT and LINT interrupt signals. The Global Configuration register is also used to program the preempt timer and provide four bits for a BMIC hardware revision number. This register is read only from the EISA side. Upon reset, bits 0–3 are reset to 0.

EISA Address—XC88h
Local Index Address—08h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bits 7–4 (read-only)
Hardware revision number of the BMIC

Bit 3
1 = System interrupt pin (EINT) uses edge-triggered protocol (Active high)
0 = System interrupt pin (EINT) uses level-triggered protocol (Active low open collector)

Bit 2
1 = Local interrupt pin (LINT) is set for active high operation
0 = Local interrupt pin (LINT) is set for active low operation

Bits 1, 0 Delay to give up bus after preempt
00 = 3 BCLKs
01 = 32 BCLKs
10 = 64 BCLKs
11 = reserved

EISA Address—XC80h through XC83h (bytes 0–3)
Local Index Address—0h through 3h (bytes 0–3)

8.1.3 ID REGISTERS

The ID register set consists of four 8-bit registers. These registers are programmed at initialization time with the product identifier for the expansion board which contains the BMIC. The registers are mapped as read-only into the EISA ID I/O address range. Upon reset, the ID byte 0 register will contain the value 0111XXXX, which is the EISA ID delay value. The local processor should program byte 0 last. If the external ID support scheme is selected, then these registers are disabled. The bit definitions defined below have significance for the EISA ID protocol but not for any BMIC hardware functionality. Upon reset, ID bytes 1–3 are not initialized to a fixed value.

ID Register Bytes 0–3:

	7	6	5	4	3	2	1	0
Byte 0	—	MCC14	MCC13	MCC12	MCC11	MCC10	MCC24	MCC23
Byte 1	MCC22	MCC21	MCC20	MCC34	MCC33	MCC32	MCC31	MCC30
Byte 2	MCC43	MCC42	MCC41	MCC40	MCC53	MCC52	MCC51	MCC50
Byte 3	MCC63	MCC62	MCC61	MCC60	MCC73	MCC72	MCC71	MCC70

ID Register Byte 0:

Bit 7	—	Reserved
Bits 6–2	MCC1<4:0>	First character of manufacturer's code
Bits 1, 0	MCC2<4:3>	First portion of second character of manufacturer's code

ID Register Byte 1:

Bits 7–5	MCC2<2:0>	Second portion of second character of manufacturer's code
Bits 4–0	MCC3<4:0>	Third character of manufacturer's code

ID Register Byte 2:

Bits 7–4	MCC4<3:0>	First hex digit of product number
Bits 3–0	MCC5<3:0>	Second hex digit of product number

ID Register Byte 3:

Bits 7–4	MCC6<3:0>	Third hex digit of product number
Bits 4–0	MCC7<3:0>	Hexadecimal digit of product revision

8.2 Local Processor Only Registers

The following is a table of the Local Processor Only register group listing the number of registers, register type (read/write) as related to the local side, register name, and register size:

Number	Local Type	Register Name	Active Bits per Register
INDEX REGISTERS			
1	R/W	Local Index Register	8 Bits
1	R/W	Local Data Register	8 Bits
1	R/W	Local Status/Control Register	8 Bits
DATA CHANNEL TRANSFER REGISTERS			
4	R/W	Data Transfer Channel 0 Base Address Register	8 Bits
4	R/W	Data Transfer Channel 1 Base Address Register	8 Bits
4	R	Data Transfer Channel 0 Current Address Register	8 Bits
4	R	Data Transfer Channel 1 Current Address Register	8 Bits
3	R/W	Data Transfer Channel 0 Base Count Register	8 Bits
3	R/W	Data Transfer Channel 1 Base Count Register	8 Bits
3	R	Data Transfer Channel 0 Current Count Register	8 Bits
3	R	Data Transfer Channel 1 Current Count Register	8 Bits
DATA TRANSFER CONTROL/STATUS REGISTERS			
1	W	Channel 0 Transfer Strobe Register	0
1	W	Channel 1 Transfer Strobe Register	0
1	R/W	Channel 0 Configuration Register	8 Bits
1	R/W	Channel 1 Configuration Register	8 Bits
1	R/W	Channel 0 Status Register	6 Bits
1	R/W	Channel 1 Status Register	6 Bits
PEEK/POKE REGISTER			
4	R/W	Peek/Poke Address Register	8 Bits
4	R/W	Peek/Poke Data Register	8 Bits
1	R/W	Peek/Poke Control Register	8 Bits
I/O DECODE REGISTERS			
1	R/W	I/O Decode Range 0 Base Address Register	8 Bits
1	R/W	I/O Decode Range 1 Base Address Register	8 Bits
1	R/W	I/O Decode Range 0 Control Register	8 Bits
1	R/W	I/O Decode Range 1 Control Register	8 Bits
TRANSFER BUFFER INTERFACE (TBI) REGISTERS			
2	R/W	TBI Channel 0 Base Address Register	8 Bits
2	R/W	TBI Channel 1 Base Address Register	8 Bits
2	R	TBI Channel 0 Current Address Register	8 Bits
2	R	TBI Channel 1 Current Address Register	8 Bits

8.2.1 INDEX REGISTERS

The BMIC's register set is accessed using the local Index and Local Data register set (refer to Section 3.2.6.1). The Local Index and Local Data registers are mapped directly into the Local Processor interface of the BMIC.

8.2.1.1 Local Index Register (Read/Write)

The Local Index register contains the address of the BMIC register that is currently being accessed. An optional auto-increment mode is supported through this register, which automatically increments the index register after each Local Data register read or write. Upon reset, the Local Index register is set to 0.

Local Address—1h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 — 1 = Autoincrement local index register after access to local data register
0 = Do not autoincrement

Bits 6–0 — Local index address

8.2.1.2 Local Data Register (Read/Write)

During a BMIC local register access, the value of the register being accessed is passed through this register.

Local Address—0h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

8.2.2 LOCAL STATUS/CONTROL REGISTER (READ/WRITE)

The Local Status/Control register is directly mapped into the Local Processor interface and is accessible using the two address lines (LADS<1:0>). This register provides current local doorbell interrupt status, current Channel 0 and Channel 1 interrupt and Base register status, and current peek/poke cycle status. This register is also used by the local processor on the expansion board to disable and provide the current status of the LINT signal (active or inactive). Bit 4 in this register is read/write and the remaining bits are read only. Upon reset, the Local Status/Control register is reset to 0.

Local Address—2h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 — R 1 = Enabled interrupts are pending in Local Doorbell register
0 = No enabled interrupts are pending in Local Doorbell register

Bit 6 — R 1 = Enabled interrupts are pending from channel 1 events
0 = No enabled interrupts are pending from channel 1 events

Bit 5 — R 1 = Enabled interrupts are pending from channel 0 events
0 = No enabled interrupts are pending from channel 0 events

Bit 4 — R/W 1 = Local interrupts enabled
0 = All local interrupts disabled

Bit 3 — R 1 = Local interrupt signal (LINT) is currently active
0 = LINT signal is currently inactive

Bit 2 — R 1 = Most recent peek/poke command is still pending
0 = Most recent peek/poke command is complete

Bit 1 — R 1 = Base register set for channel 1 is busy
0 = Base register set channel 1 is available

Bit 0 — R 1 = Base register set for channel 0 is busy
0 = Base register set for channel 0 is available

8.2.3 DATA CHANNEL TRANSFER REGISTERS

The Data Channel Transfer register set is used to control burst and standard EISA data transfers. Each transfer channel has a set of Base and Current registers, and also a Transfer Strobe, Configuration, and Status register.

NOTE:
The Base register set and the Transfer Strobe register must be initialized before a transfer can take place. They are not initialized to a fixed value upon reset.

8.2.3.1 Channel 0 and 1 Transfer Base Address Registers (Read/Write)

Each Channel has an associated Base Address register set. The Transfer Base Address registers are programmed with the 32-bit starting address to be used during the data transfer. After the Base registers have been programmed, they should not be programmed again until the contents of the Base registers have been transferred to the Current registers. The Base Address registers are not initialized to a fixed value upon reset.

Channel 0 Local Index Address—43h through 46h (bytes 0 through 3)
Channel 1 Local Index Address—63h through 66h (bytes 0 through 3)

BYTE 3	BYTE 2	BYTE 1	BYTE 0

8.2.3.2 Channel 0 and 1 Transfer Current Address Registers (Read Only)

Each Channel has an associated Current Address register set. The Transfer Current Address registers contain the real-time status of the 32-bit transfer address. The Current Address registers are not initialized to a fixed value upon reset.

NOTE:
The current register set is readable by the local processor. However, there are possible coherency problems involved with reading multiple bytes while the current registers are being updated during a transfer. To avoid these problems, a channel's transfer should be temporarily suspended (using the channel's Configuration Register) before trying to read the channel's current register set.

Channel 0 Local Index Address—53h through 56h (bytes 0 through 3)
Channel 1 Local Index Address—73h through 76h (bytes 0 through 3)

BYTE 3	BYTE 2	BYTE 1	BYTE 0

8.2.3.3 Channel 0 and 1 Transfer Base Count Registers (Read/Write)

Each Channel has an associated Base Count register set. The Transfer Base Count registers are programmed with the number of bytes to be transferred. Each Channel has 22 bits of counter space for a maximum transfer block size of 4 Mbytes. Bits 22 and 23 are used for channel control. The Base Count registers are not initialized to a fixed value upon reset.

Channel 0 Local Address—40h through 42h (bytes 0 through 2)
Channel 1 Local Address—60h through 62h (bytes 0 through 2)

BYTE 2			BYTE 1	BYTE 0
Bit 23	Bit 22	Bit 16–21	Bits 8–15	Bits 0–7

Bit 23 — R/W
- 1 = Start transfer as soon as base register set is copied to current register set
- 0 = Hold transfer after current register set is loaded. Wait for transfer suspend bit 0 to be reset

Bit 22 — W
- 1 = Transfer from bus master expansion board to EISA bus (EISA write)
- 0 = Transfer from EISA bus to bus master expansion board (EISA read). This is applicable only to channel 1 and not for channel 0, as channel 0 can perform EISA WRITE transfers only.

Bits 0–21 — R/W — Transfer byte count

If bit 23 in the Base Count register is not set to a 1, the channel suspend bit (CFGSU) in that channel's corresponding configuration register is automatically set to a 1. The bit will be set during the Base register to Current register transfer. This ensures that a channel request for that channel is not generated. When the local processor resets the channel suspend bit to 0 in the corresponding Configuration register, a transfer request will be generated.

NOTE:
If the initial byte count is programmed to be "0", no transfer request will be generated and no transfer will occur.

8.2.3.4 Channel 0 and 1 Transfer Current Count Registers (Read Only)

Each Channel has an associated Current Count register set. The Transfer Current Count registers contain the 22-bit value representing the number of bytes remaining to be transferred on the channel. This value can be from one byte to four Mbytes. Bit 23 is reserved. Bit 22 is used to indicate the direction of the transfer. Upon reset, the Current Count registers are not initialized. At the end of a transfer, this register contains the value of the number of bytes transferred during the last cycle.

Channel 0 Local Index Address—50h through 52h (bytes 0 through 2)
Channel 1 Local Index Address—70h through 72h (bytes 0 through 2)

BYTE 2			BYTE 1	BYTE 0
Bit 23	Bit 22	Bit 16–21	Bits 8–15	Bits 0–7

Bit 23 — Reserved

Bit 22 — 1 = Current transfer is from bus master expansion board to EISA bus
0 = Current transfer is from EISA bus to bus master expansion board

Bits 0–21 — Current transfer byte count

8.2.4 DATA TRANSFER STATUS/CONTROL REGISTERS

8.2.4.1 Channel 0 and 1 Transfer Strobe Registers (Write Only)

Each channel has an associated Transfer Channel Strobe register. The Strobe register is used to initiate the transfer of information from the Base register set to the Current register set. The act of writing to this register will initiate the Base to Current transfer. There are no bits to this register, the data written to this register is ignored and the register cannot be read.

If bit 23 in the Transfer Base Count Register is set to a 1, the data transfer will be requested immediately. Otherwise, the transfer will wait until the transfer suspend bit CFGSU for the corresponding channel is reset. The transfer suspend bit is located in the Configuration register.

Channel 0 Local Index Address—49h
Channel 1 Local Index Address—69h

8.2.4.2 Channel 0 and 1 Transfer Channel Configuration Registers (Read/Write)

Each channel has an associated Transfer Configuration register. Upon reset, the Configuration registers are reset to 0. The Configuration register set is used to configure the channels as follows:

Channel 0 Local Index Address—48h
Channel 1 Local Index Address—68h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGEA	CFGIE	CFGIT	CFGFF	CFGBR	CFGCL	CFGEI	CFGSU

Bit 7 — CFGEA 1 = Enable real-time address transfer to transfer buffer logic
0 = Disable real-time address transfer to transfer buffer logic

Bit 6 — CFGIE Reserved. This bit must always be written with 0.

Bit 5 — CFGIT 1 = Enable interrupt on transfer complete
0 = Disable interrupt on transfer complete

Bit 4 — CFGFF 1 = Give up ownership of EISA bus if a transfer interruption occurs on this channel
0 = Retain ownership of EISA bus if a transfer interruption occurs on this channel

Bit 3 — CFGBR 1 = Enable EISA burst transfer
0 = Disable burst transfers (channel uses non-burst (2 BCLK) cycle transfers)

Bit 2 — CFGCL 1 = Clear channel
Stop any transfers and flush the data FIFO
0 = No operation
Always returns a 0 when read

Bit 1 — CFGEI Reserved. This bit must always be written with 0.

Bit 0 — CFGSU 1 = Temporarily suspend transfer
0 = Allow transfer to proceed

The CFGEA Bit enables the real-time address transfer to the transfer buffer logic. If the CFGEA bit is set to a 1, the transfer buffer real-time address for the active channel is transferred to the transfer buffer logic each time that channel regains the bus and the start address is transferred each time the Base register contents are loaded into the corresponding Current registers. If the CFGEA bit is set to 0, the address load signal (TLD#) is activated only when the Base is loaded into the Current register (refer to Section 5.3).

The CFGIE Bit is a reserved bit. Zero (0) must always be written at this bit location. This bit can be ignored during register reads.

The CFGIT Bit enables an interrupt on transfer complete (EOP).

The CFGFF Bit controls whether EISA bus ownership is relinquished or maintained after a transfer interruption. When a channel is interrupted for any reason, (1K page break, FIFO stall, channel clear, transfer suspend, or transfer complete), the BMIC may relinquish the EISA bus depending on the state of the CFGFF bit in the above register. The function of the CFGFF bit, as related to the above channel interruptions, is as follows:

If the CFGFF bit = 1, the BMIC will relinquish control of the EISA bus upon the detection of any of the above interruptions. This will occur regardless if there are additional data transfer requests pending. If there are additional data transfer requests pending, the BMIC will reassert MREQ# a minimum of two BCLK's later to reacquire the EISA bus.

If the CFGFF bit = 0, the BMIC retains ownership of the EISA bus upon detection of a FIFO stall or 1K page break as long as a preempt timer timeout has not occurred. If there are additional data requests pending, the BMIC will immediately perform the pending transfer and then rearbitrate for the EISA bus to complete the interrupted transfer. If there are no additional data requests pending, the BMIC will relinquish ownership of the EISA bus only after the current transfer interruption has been serviced and completed.

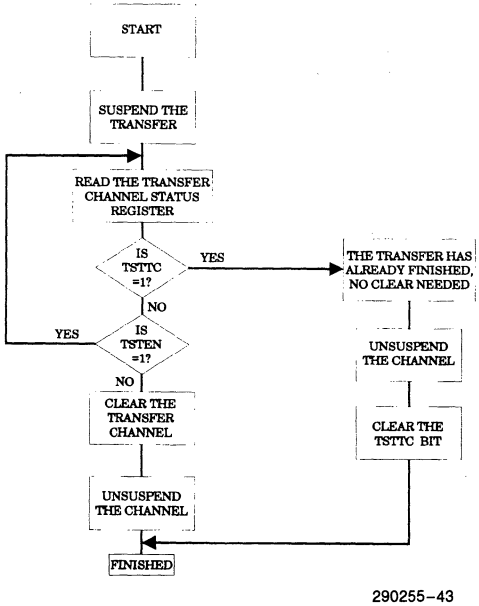
NOTE:
During a FIFO pause, CFGFF is ignored.

The CFGBR Bit defines the type of transfer cycles (burst or non-burst) that can be requested on the transfer channel. If burst cycles have been selected and system memory is unable to run burst cycles, the BMIC will default to non-burst (two BCLK) or mismatched cycles.

The CFGCL Bit is used to generate a channel clear. A channel clear terminates the current transfer and flushes the associated FIFO. The FIFO is reset during the next Base to Current register copy.

Before a channel is issued a clear command, the channel must first be suspended by writing a "1" into Bit 0 (CFGSU) of the Transfer Channel Configuration Register. Next the Transfer Channel Status Register must be read. If the TSTTC (Bit 0) is set to a "1", then the channel has already completed the transfer. The channel is then unsuspended (write a "0" into Bit 0 [CFGSU] of the Transfer Channel Configuration Register), and the TSTTC bit is then cleared.

If the TSTTC bit is a "0", then the TSTEN bit is checked. If this bit is a "1", then the channel has not returned to idle yet, and the Transfer Channel Status Register is re-polled. If the TSTEN bit is a "0", then the channel has successfully returned to idle and can now be cleared with no errors. This is done by setting Bit 2 (CFGCL bit) to a "1" in the Transfer Channel Configuration Register. A flowchart for this operation is shown in the following figure.



NOTE:
TSTTC must ALWAYS be cleared when a Transfer is completed.

Figure 8-1. Channel Clear Flowchart

If a channel is enabled for a transfer during a Channel clear, the BMIC will generate an end of process by asserting TEOP#. If the channel is not enabled for a transfer or the channel clear is preceded by a channel suspend, a TEOP# will not be generated. The channel clear will be active for at least two complete BCLK cycles.

The CFGEI Bit is a reserved bit. Zero (0) must always be written at this bit location. This bit can be ignored during register reads.

The CFGSU Bit is used to temporarily suspend the data transfer.

8.2.4.3 Channel 0 and 1 Transfer Channel Status Registers (Read/Write)

Each channel has an associated Transfer Channel Status register. Bits 2 through 4 are read only and bits 5 through 7 are reserved. Upon reset, the Channel Status register set is reset to "0".

Channel 0 Local Index Address—4Ah
Channel 1 Local Index Address—6Ah

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	TST1K	RSVD	TSTEN	TSTIP	TSTET	TSTTC

Bit 7, 6, 5 —W — Reserved. 0 should be written into these bits during writes. Ignore any data on these bits during register reads

Bit 4 — R — Reserved

Bit 3 — R
- 1 = The transfer channel is enabled for transfer (transfer in progress)
- 0 = The transfer channel is not enabled for transfer (transfer not in progress)

Bit 2 — R
- 1 = A transfer request is active on this channel.
- 0 = No transfer request is active on this channel.

Bit 1 — Reserved. Ignore data at this bit location.

Bit 0 — R/W
- 1 = Transfer completed on this channel (read)
  Reset this bit (write)
- 0 = No transfer completion on this channel (read)
  No action (write)

Bits (7), (6), TST1K, and (4) are reserved. Any data read from these bits should be ignored.

The TSTIP and TSTEN Bits are read only and indicate whether the corresponding channel is requesting a transfer or whether the channel's transfer is currently in progress.

The TSTET Bit is a reserved bit and should be ignored during all register reads. Zero (0) should always be written at this bit location.

The TSTTC Bit is read/write and is used to indicate the current end-of-process status of the transfer. If an EOP occurs, the BMIC will set bit (0) to a "1" and generate an interrupt to the local processor. The BMIC will not generate the interrupt if the CFGIT bit in the channel's corresponding Transfer Configuration register is set to a "0".

NOTE:
The TSTTC bit is implemented as a sticky bit. This bit can be reset by the local processor without affecting the status of the other bits in the register.

8.2.5 PEEK/POKE REGISTERS

The Peek/Poke register set consists of four 8-bit Address registers, four 8-bit Data registers and one Peek/Poke control register. The Address and Data registers are used to define the 32-bit address and data that will be used during the peek/poke cycles, and the Control register is used to request and define the type of cycle that will be generated (peek, poke, or locked exchange). The peek/poke or locked exchange cycle is initiated by writing to the Peek/Poke control register. During Reset, the Peek/Poke Address registers and the Control register are reset to "0".

8.2.5.1 Peek/Poke Address Registers (Read/Write)

The four 8-bit Peek/Poke Address registers contain the 32-bit peek/poke address. Only the lower 16 bits are used for I/O cycles. Address bits 0 and 1 are ignored. Upon reset, this register is reset to "0".

Local Index Address—34h through 37h (bytes 0 through 3)

BYTE 3	BYTE 2	BYTE 1	BYTE 0
Bits 24–31	Bits 16–23	Bits 8–15	Bits 2–7

8.2.5.2 Peek/Poke Data Registers (Read/Write)

The four 8-bit peek/poke data registers hold the data for the peek/poke cycle. Each peek/poke data register is associated with one byte lane. During peek transfers, only those peek/poke data registers whose corresponding byte enable bit is set in the peek/poke control register contain valid data. During poke transfers, the data must be placed in the appropriate register as determined by the corresponding byte enable bit.

Local Index Address—30h through 33h (bytes 0 through 3)

BYTE 3	BYTE 2	BYTE 1	BYTE 0
Bits 24–31	Bits 16–23	Bits 8–15	Bits 0–7

The Shared register timings (t85, t93, t96–t98) are used when accessing the Peek/Poke Data registers.

8.2.5.3 Peek/Poke Control Register (Read/Write)

The Peek/Poke Control register is written to by the local processor when a peek/poke transfer is desired over the EISA bus. Upon reset, this register is reset to "0".

Local Index Address—38h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 — Reserved. Set to 0

Bits 6, 5 — 10 = Do read cycle (peek)
01 = Do write cycle (poke)
11 = Do locked exchange cycle (peek/poke)
00 = Do Nothing (Nop)

Bit 4 — 1 = Do memory cycle
0 = Do I/O cycle

Bit 3, Bit 2, Bit 1, Bit 0 — 1 = Byte enable for given byte lane
0 = Byte disable for given byte lane

Bits (6) and (5) are used to define the type of cycle requested (peek, poke or locked exchange).

Bit (4) defines whether the cycle is memory or I/O.

Bits (3–0) are used to define the byte enables for the doubleword data written to or read from the Peek/Poke data register. Peek/Poke cycles will not be generated for illegal combinations of byte enables.

ILLEGAL COMBINATIONS OF BYTE ENABLES:

Bits 3–0	IBE# <3:0>
0000	1111
0101	1010
1001	0110
1010	0101
1011	0100
1101	0010

NOTE:
Bits 3–0 in the above register are active high whereas the EISA byte enables (IBE# <3:0>) are active low.

8.2.6 I/O RANGE DECODE REGISTERS

The I/O Decode Range register set consists of two I/O Decode Range Base Address registers and two I/O Decode Range Control Registers. The Address registers are used to define the address range of interest to the expansion board and the Control registers are used to define the decode range size, type of decode (slot specific or general), and the response of the local I/O (32-bit EISA or 8-bit EISA). The I/O decode register set controls the two IOSEL# pins on the BMIC. Each pin has an associated Address and Control register.

Upon reset, the I/O Decode Range registers are initialized according to the following table:

Local Processor	*Local Processor Not Present		*Local Processor Present	
Range	**Rng 0**	**Rng 1**	**Rng 0**	**Rng 1**
Control Registers	60h	60h	20h	20h
Address Registers	E0h	00h	00h	00h

*Refer to Section 7.3 for information regarding "local processor present" or "local processor not present".

8.2.6.1 Range 0 and 1 I/O Decode Base Address Registers (Read/Write)

Each Decode range and IOSEL# pin has an associated I/O Decode Range Base Address register.

Range 0 Local Index Address—39h
Range 1 Local Index Address—3Bh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

During general I/O decode, bits 7–0 are used to compare against EISA address lines LA<9:2>. During slot specific decode, bits 7 and 6 are compared against EISA address lines LA<11:10> and bits 5–0 are compared against EISA address lines LA<7:2> (refer to Section 4.8).

8.2.6.2 Range 0 and 1 I/O Decode Control Registers (Read/Write)

Each Decode range and IOSEL# pin has an associated I/O Decode Range Control register.

Range 0 Local Index Address—3Ah
Range 1 Local Index Address—3Ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 — 1 = Respond as a 32-bit EISA I/O device
0 = Respond as an 8-bit EISA I/O device

Bit 6 — 1 = Slot Specific I/O Decode
0 = General I/O Decode

Bit 5 — 1 = IOSEL# held during CMD# active
0 = IOSEL# follows I/O address changes

Bit 4, Bit 3: 1 = Do not compare I/O Range Base Address Register and corresponding EISA address bit (Mask)

Bit 2, Bit 1, Bit 0: 0 = Compare I/O Range Base Address Register with corresponding EISA address bit

Refer to Section 4.8 for a complete description of the I/O Decode Range Control registers and the BMIC decode function in general.

8.2.7 TRANSFER BUFFER INTERFACE (TBI) REGISTERS (READ/WRITE)

The TBI registers are programmed to provide the 16-bit start address of the data transfer for use by the transfer buffer logic (refer to Section 5.3). Each transfer channel has a corresponding TBI Base and Current Address register set. The contents of the TBI Base Address registers are transferred to the TBI Current Address registers during a write to the channel's corresponding Transfer Channel Strobe Register.

8.2.7.1 Channel 0 and 1 TBI Base Address Registers (Read/Write)

The BMIC provides two 8-bit TBI Base Address registers per channel. The registers are programmed with the 16-bit start address of the data in the Transfer Buffer memory space. The TBI Base Address register set is not initialized to a fixed value upon reset.

Channel 0 Local Index Address—4Bh and 4Ch (byte 0 and 1)
Channel 1 Local Index Address—6Bh and 6Ch (byte 0 and 1)

Byte 1	Byte 0

8.2.7.2 Channel 0 and 1 TBI Current Address Registers (Read Only)

The BMIC provides two 8-bit TBI Current Address registers per channel. The TBI Current Address registers contain the 16-bit real-time address of the data transfer. The contents of the Current register set are transferred to the external buffer logic at the beginning of every new data block transfer. The BMIC may also be programmed to transfer the contents of the Current Address register each time the corresponding channel regains control of the bus (refer to Section 5.3). The TBI Current Address register set is reset to "0" upon device reset.

Channel 0 Local Index Address—58h and 59h (byte 0 and 1)
Channel 1 Local Index Address—78h and 79h (byte 0 and 1)

Byte 1	Byte 0

NOTE:
The TBI current registers contain real-time status and may change at anytime. If a stable value is needed while reading a set of these registers, the channel should be temporarily suspended by setting the CFGSU bit in the Channel Configuration register to a "1" before these registers are read.

9.0 DETAILED PIN DESCRIPTION

9.1 EISA Interface Signals

Pin Name	Description
START#	I/O TRI-STATED (EISA CYCLE START STROBE) The START# signal provides timing control at the start of a cycle. During EISA master mode, the BMIC drives this signal low after LA<31:2> and M/IO become valid and negates START# on the rising edge of BCLK after one BCLK cycle time. During EISA slave mode, the BMIC uses this signal to indicate the start of a slave bus cycle. It is sampled on the rising edge of BCLK. Upon reset, this pin is tri-stated and placed in input mode.
CMD#	INPUT (EISA COMMAND STROBE) The CMD# provides timing control within the cycle. The 82358 Bus Controller asserts CMD# on the rising edge of BCLK, simultaneously with the negation of START#. CMD# is held low until the end of the cycle. The BMIC uses CMD# in EISA slave mode for timing control during internal Shared register read/write accesses.
M/IO	I/O TRI-STATED (EISA MEMORY/IO CYCLE STATUS PIN) M/IO is used to indicate that the type of cycle in progress is a memory cycle (high) or I/O cycle (low). M/IO is pipelined from one cycle to the next and must be latched by the addressed memory slave if needed for the whole cycle. During EISA master mode, the BMIC drives this signal. The BMIC will drive this pin high during burst and non-burst (two BCLK) cycles. The value of M/IO in a Peek/Poke or locked exchange cycle depends on the programmed value of bit 4 in the Peek/Poke Control register. During EISA slave mode, the M/IO pin is an input. As a slave, the BMIC will respond only as an I/O device. Upon reset, this pin is tri-stated and placed in input mode.
W/R	I/O TRI-STATED (EISA WRITE/READ CYCLE STATUS PIN) The W/R status signal identifies the cycle as a write (high) or read (low). W/R is pipelined from one cycle to the next and must be latched by the addressed memory slave if needed for the whole cycle. During EISA master mode, the BMIC drives this signal. During EISA slave mode, this pin is an input. Upon reset, W/R is tri-stated and placed in input mode.
EXRDY	I/O OPEN COLLECTOR (EISA READY SIGNAL) EXRDY is used by EISA I/O and memory slaves to request wait states during a cycle. Each wait state is one BCLK period. During EISA master mode, the BMIC first samples this signal on the falling edge of BCLK after CMD# is asserted. If it is low, the BMIC will insert a wait state, and continue inserting wait states as long as EXRDY is low at each successive falling edge of BCLK. During EISA slave mode, the BMIC drives EXRDY inactive until it is ready to complete cycles addressed to it. The EXRDY pin is an open collector output.
EX32#	I/O OPEN COLLECTOR (EISA 32-BIT SLAVE RESPONSE PIN) EX32# is an open collector and is used by memory or I/O slaves to indicate their support of 32-bit transfers. During EISA master mode, the BMIC samples EX32# on the same rising edge of BCLK that START# is deasserted. The BMIC uses this pin to determine if the addressed slave is capable of 32-bit transfers. During peek/poke and non-burst EISA data transfers, the BMIC is a 32-bit master only and will allow the 82358 Bus Controller to do all necessary bus conversions. During EISA slave mode, the BMIC drives EX32# low if it has 32-bit data to send to the EISA bus, otherwise this signal is inactive.

9.1 EISA Interface Signals (Continued)

Pin Name	Description
MASTER16#	OUTPUT OPEN COLLECTOR (EISA 16-BIT MASTER CONTROL) In master mode, the BMIC will assert MASTER16# (at the same time as START#) for one BCLK period when it is capable of downshifting from a 32-bit master to a 16-bit master. The BMIC will downshift if necessary during memory burst transfers only. The BMIC will automatically downshift from a 32- to 16-bit master if the EX32# signal is sampled inactive and the SLBURST# signal is sampled active. MASTER16# has no function in slave mode.
AEN	INPUT (EISA ADDRESS ENABLE SIGNAL) The BMIC uses AEN when in EISA slave mode to qualify I/O addresses. When negated (low), the BMIC uses AEN to decode possible accesses to its general and slot specific I/O space. When asserted (high), the address on the EISA bus will be ignored by the BMIC. AEN is sampled on the falling edge of CMD#. This signal is not used in master mode.
MSBURST#	OUTPUT TRI-STATED (EISA MASTER BURST SIGNAL) The BMIC asserts MSBURST# to indicate to the addressed memory slave that the BMIC will provide burst cycles. If the BMIC samples SLBURST# active on the rising edge of BCLK after START# is asserted, the BMIC will activate MSBURST# on the next BCLK falling edge and will proceed with burst cycles. If the BMIC samples SLBURST negated, MSBURST# will not be activated and the BMIC will proceed with either non-burst (two BCLK) or mismatched cycles, depending on the size of the slave device addressed. This signal is not used in slave mode. Upon reset, this pin is tri-stated.
SLBURST#	INPUT (EISA SLAVE BURST SIGNAL) The BMIC uses this signal in master mode to determine if the addresed slave memory is capable of supporting burst transfers. If the BMIC samples SLBURST# active on the rising edge of BCLK after START# is asserted, the BMIC will proceed with burst cycles. If the BMIC samples SLBURST# negated, either non-burst (two BCLK) or mismatched cycles will be generated.
LOCK#	OUTPUT TRI-STATED (EISA RESOURCE LOCK SIGNAL) The BMIC asserts this signal to guarantee exclusive memory and I/O access during locked peek/poke exchange. Upon reset, this pin is tri-stated.
MREQ#	OUTPUT (EISA MASTER BUS REQUEST SIGNAL) MREQ# is asserted by the BMIC to request EISA bus access. The BMIC will begin driving the bus with the address and control signals on the falling edge of BCLK, two BCLKs after MAK# is sampled active. During an EISA write transfer, MREQ# will not be asserted until the FIFO on the selected channel is full. During an EISA read transfer, MREQ# will be asserted immediately after receiving a transfer request, assuming that a slave cycle is not currently in progress. Upon reset, this pin is driven inactive high.
MAK#	INPUT (EISA MASTER BUS ACKNOWLEDGE SIGNAL) The MAK# signal is asserted by the 82357 (ISP) to grant EISA bus access to the BMIC. The BMIC samples MAK# on the falling edge of BCLK and will begin driving the bus with the address and control signals on the falling edge of BCLK, two BCLKs after MAK# is sampled active. The MAK# signal may be negated by the ISP to indicate to the BMIC that another device requires EISA bus access. The BMIC will negate MREQ# to release the bus within 64 BCLKs (8 μs) of sampling MAK# negated.
EINT	OUTPUT OPEN COLLECTOR (EISA INTERRUPT REQUEST SIGNAL) The EINT line is used by the BMIC to interrupt the system CPU or EISA bus master to request service. EINT can be programmed for either edge or level-triggered operations and is an open collector output in level-triggered mode. Upon reset, EINT is placed in level-triggered mode and floating.
BCLK	INPUT (EISA BUS CLOCK) This clock signal is used by the BMIC to synchronize the EISA control signals and data transfers to the system clock. BCLK typically runs at a frequency of 8.33 MHz with a normal duty cycle of 50%. The BCLK period is sometimes extended by the 82358 (EBC) by up to one BCLK period for synchronization purposes.

9.1 EISA Interface Signals (Continued)

Pin Name	Description
RESET	INPUT (EISA RESET SIGNAL) This signal is used by the BMIC to initialize all of its internal registers and state machines to a known state. This signal is asynchronous with respect to BCLK. To reset the BMIC properly, the RESET signal must be active for eight BCLK periods.
IDAT<31:0>	I/O TRI-STATED (EISA DATA LINES/UPPER 22 ADDRESS LINES) These data signals interface to the EISA bus through external, 74F245 bi-directional TTL buffers. The upper 22 data lines are also multiplexed to function as the upper 22 EISA address lines. The 22 upper address signals are latched into external 74F573 TTL latches during transfers as necessary by the BMIC. Both the external data buffers and the address latches are controlled by the BMIC during all slave and master mode data transfers. Upon reset, these pins are tri-stated.
IADS<11:10>	(INPUT) (EISA ADDRESS INPUT LINES) These two address lines are input only and are only used during slave mode. They are used along with IADS<9:2> and EISA byte enables IBE<3:0># for I/O address decoding. The corresponding EISA output address lines LA<11:10> are part of the upper 22 address lines that are multiplexed and sent out through the upper 22 data lines.
IADS<9:2>	I/O TRI-STATED (EISA LOWER ADDRESS LINES) These eight address lines are part of the lower EISA address lines and are connected directly to the EISA bus. When the BMIC is a master, it drives these lines directly to the EISA bus. The upper 22 addresses are latched from the data bus. IADS<9:2> are pipelined from one cycle to the next and should be latched by the addressed slave if required for the whole cycle. When the BMIC is a slave, it monitors these lines along with EISA address lines IADS<11:10> and EISA byte enables IBE<3:0># for I/O address decoding. Upon reset, these pins are tri-stated and placed in input mode. The following address lines are used during I/O decoding as shown: Slot specific I/O address decoding (expansion board)—IADS<11:2> Slot specific I/O address decoding (shared registers)—IADS<11:2>/IBE<3:0># General I/O address decoding (expansion board)—IADS<9:2>
IBE<3:0>#	I/O TRI-STATED (EISA BYTE ENABLES) IBE#<3:0> are the byte enables of the EISA bus and identify the specific bytes that are active during the current EISA bus cycle. During EISA master mode, the BMIC drives these signals. IBE#<3:0> are pipelined from one cycle to the next and should be latched by the addressed slave if required for the whole cycle. During EISA slave mode, the byte enables are inputs and are used along with EISA address lines IADS<11:2> for internal shared register decoding. Upon reset, these pins are tri-stated and placed in input mode.

9.2 EISA Buffer Control Signals

Pin Name	Description
UALOE#	OUTPUT (EISA UPPER ADDRESS LATCH STROBE AND OUTPUT ENABLE) The UALOE# signal is used by the BMIC to control the external latching of the upper 22 address lines LA<31:10>. UALOE# is designed to be connected to the latch enables and output enables of the 74F573 external address latches. The BMIC updates the external address latches at the beginning of all master mode transfers. The desired address value is placed on the IDAT<31:10> lines and latched by the external latches on the falling edge of UALOE# at the beginning of the transfer. During EISA master mode to enable the EISA address lines <31:10>, the BMIC drives UALOE# low on the rising edge of BCLK, one BCLK prior to the falling edge of START#. UALOE# will remain active until the end of the cycle. During slave mode, the BMIC holds UALOE# high to disable the latches. For additional information with regards to the timing for this signal, refer to the A.C. timing and Basic Function timing sections. Upon reset, this pin is driven inactive high.
IDDIR	OUTPUT (EISA DATA DIRECTION SIGNAL) The IDDIR signal is used by the BMIC to control the direction of the external 74F245 data buffers. During data transfers from the BMIC to the EISA bus, this signal will be driven low. During data transfers from the EISA bus to the BMIC, this signal will be driven high. For additional information regarding the timing for this signal, refer to the A.C. timing and Basic Function timing sections (master and slave). Upon reset, this pin is driven high.
IDOE23# IDOE1# IDOE0#	OUTPUT (EISA DATA BYTE LANE BUFFER ENABLES) The IDOE# signals are used by the BMIC to control the output enables on the external 74F245 data buffers. The IDOE# signals will be driven so that the data buffers are enabled at the appropriate times during master and slave transfers. For additional information with regards to the timing for these signals, refer to the A.C. timing and Basic Function timing sections. Upon reset, these signals are driven inactive high.

9.3 Address Decode Signals

Pin Name	Description
IOSEL#<1:0>	OUTPUT (ADDRESS RANGE DECODE OUTPUTS) The IOSEL# signals are used by the BMIC to enable external logic on the expansion board during slot specific and general purpose I/O decode. These pins become active when the LA<11:2> address lines on the EISA bus contain a value mapped into one of the two possible I/O address decode ranges provided by the BMIC (refer to Section 4.8). Upon reset, these pins are driven inactive high.

9.4 Transfer Buffer Interface Signals

Pin Name	Description
TRQ#	OUTPUT (LOCAL DATA TRANSFER REQUEST SIGNAL) When a data transfer is desired over the Transfer Buffer interface, TRQ# is driven low, indicating to the transfer buffer logic that a transfer is following. TRQ# will remain active until the data transfer is completed or a transfer interruption occurs. Upon reset, this pin is driven inactive high.
TACK#	INPUT (LOCAL DATA TRANSFER ACKNOWLEDGE SIGNAL) External logic uses this signal to acknowledge the transfer of a data item (16-bit word) over the Transfer Buffer interface.
TLD#	OUTPUT (LOCAL ADDRESS COUNTER LOAD SIGNAL) This signal when asserted (low) is used to load the transfer start address and the transfer real-time address into an external address counter as required for data transfers (refer to Section 5.3). TLD# is asserted at the beginning of all new channel accesses to the transfer buffer logic and will remain asserted until acknowledged by TACK#. Upon reset, this pin is driven inactive high.
TDIR	OUTPUT (DATA TRANSFER DIRECTION SIGNAL) This signal is used to inform the transfer buffer logic as to the direction of the current data transfer. When driven (high) data will be transferred from the EISA bus to the expansion board. When driven (low) data will be transferred from the expansion board to the EISA bus. TDIR will be held valid whenever TLD# and TRQ# are active. TDIR will not change states when TRQ# is active. Upon reset, this pin is driven high.
TCHAN	OUTPUT (TRANSFER CHANNEL SELECT SIGNAL) This signal is used by the BMIC to inform the transfer buffer logic as to which channel will be active during the transfer. When driven (low) transfer channel 0 is active and when driven (high) transfer channel 1 is active. TCHAN has the same timings as TDIR and will not change states when TLD# or TRQ# are active. Upon reset, this pin is driven low.
TDAT<15:0>	I/O TRI-STATED (TRANSFER DATA LINES) This bidirectional bus is the BMIC's Transfer Buffer interface data bus. It is used during data transfers between the external transfer buffer logic and the BMIC. The data transferred across the TDAT bus is word aligned. The data lines are also used to transport the transfer address to the transfer buffer logic on the expansion board (refer to Section 5.3). The TDAT bus can be unconditionally disabled by driving the TDOE# signal high. **NOTE:** During EISA write data transfers, the TDAT lines are inputs and operate independent of the value of TDOE#. Upon reset, the TDAT bus is tri-stated.
TDOE#	INPUT (TRANSFER INTERFACE DATA OUTPUT ENABLE) When driven high, this pin can be used by external logic to unconditionally disable the BMIC from driving the TDAT<15:0> lines. This feature eliminates the need for the BMIC to gain prior permission to drive the TDAT bus and also allows external logic the ability to time-share the TDAT bus.
TEOP#	OUTPUT OPEN COLLECTOR (TRANSFER END-OF-PROCESS SIGNAL) This signal is an open collector signal that indicates the end of a transfer to the external transfer buffer logic. TEOP# is driven low by the BMIC to indicate the end of transfer. The TEOP# pin requires an external 2.5K to 3.2K pullup resistor for proper operation.
TCLK	INPUT (TRANSFER CLOCK) All transfer control signals are synchronous to this clock. The frequency should be in the range of 16 MHz to 20 MHz to maintain a 33 Mbyte/sec burst transfer rate over the EISA bus. This clock may be completely asynchronous to the EISA BCLK signal.

9.5 Local Processor Interface Signals

Pin Name	Description
LDAT<7:0>	I/O TRI-STATED (LOCAL PROCESSOR INTERFACE DATA BUS) This bidirectional bus is used to transfer commands and status between the BMIC and the local processor on the expansion board. If a local Processor is not present, this bus will need to be connected to the ISA bus (refer to Section 7.3). Upon reset these pins are tri-stated.
LRD#	INPUT (LOCAL PROCESSOR INTERFACE READ STROBE) The local processor asserts LRD# to indicate to the BMIC that it should drive its data onto the LDAT bus. LRD# is asserted for register access to the BMIC's Local Processor interface. The LADS lines and the LCS# signal must be valid 10 ns before the falling edge of LRD# and remain valid until LRD# is deasserted.
LWR#	INPUT (LOCAL PROCESSOR INTERFACE STROBE) The local processor asserts LWR# to indicate to the BMIC that it may latch data from the LDAT bus. LWR# is asserted for write accesses to the BMIC's Local Processor interface. The LADS lines and the LCS signal must be valid 10 ns before the falling edge of LWR# and remain valid until LWR# is deasserted.
LCS#	INPUT (LOCAL PROCESSOR INTERFACE CHIP) A (low) on this pin enables LWR# and LRD# communication between the BMIC and the local processor on the expansion board. The LRD# and LWR# signals are ignored unless the LCS# signal is active. LCS# must be asserted 10 ns before LRD# and LWR# and remain active until the inactive edge of LRD# and LWR#.
LADS<1:0>	INPUT (LOCAL PROCESSOR ADDRESS SELECT) These address lines are used by the local processor to select the Local Data, Local Index, and Local Status/Control registers. The BMIC uses these registers as part of an indexing scheme to access all of its internal registers (refer to Sections 3.2.6.1 and 8.2.1). **LADS1 LADS0** 0 0 = Local Data register 0 1 = Local Index register 1 0 = Local Status/Control register 1 1 = Reserved
LINT	OUTPUT (LOCAL PROCESSOR INTERRUPT SIGNAL) This signal informs the local processor that an event has occurred which requires the local processor's attention. This pin can be programmed for either active high or active low level operations. After being asserted, LINT will not return to an inactive state until the interrupt has been serviced. The LINT signal is not an open collector output during active low operations and will require external logic if interrupts need to be tied together on the local side. Upon reset, this pin is driven high and placed in active low level mode.
LRDY	I/O (LOCAL PROCESSOR READY) This signal is the acknowledgement from the BMIC to the local processor that it is finished with the current Shared register access cycle. The LRDY pin is also used by external logic to indicate to the BMIC that a local processor is not present. If a local processor is not present, the LRDY signal must be driven low during reset (refer to Section 7.3). If a local processor is present, a weak pullup resistor must be connected to the LRDY output to insure that LRDY is high during the time reset is active.

9.6 Power Supplies

V_{CC} — 11 Power pins

V_{SS} — 13 Ground pins

Total number of power supply pins: 24

10.0 BASIC FUNCTION TIMING DIAGRAMS

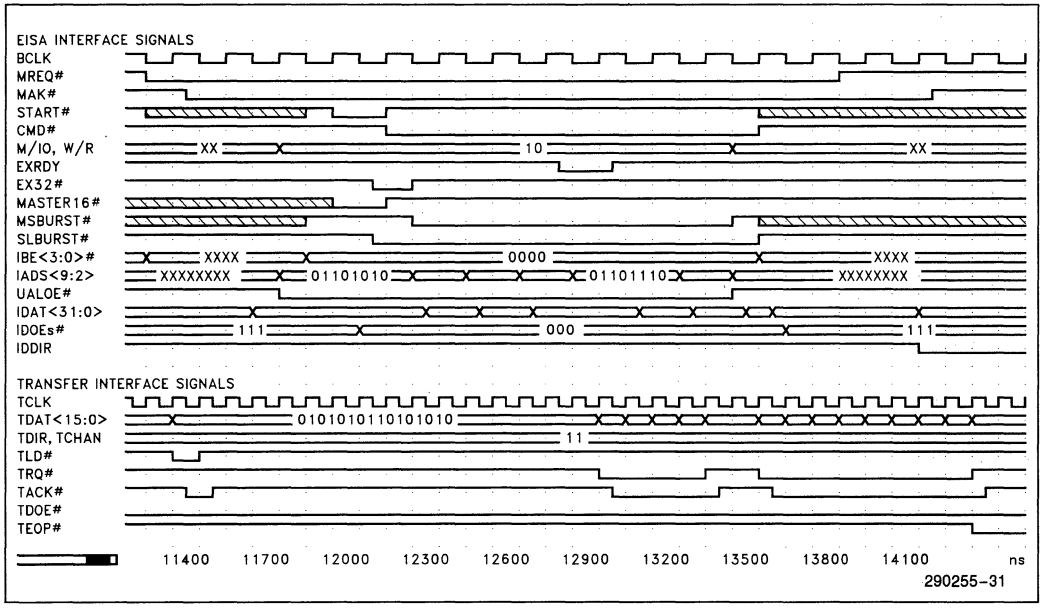


Figure 10-1. 32-Bit Burst Cycle (EISA Read)

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

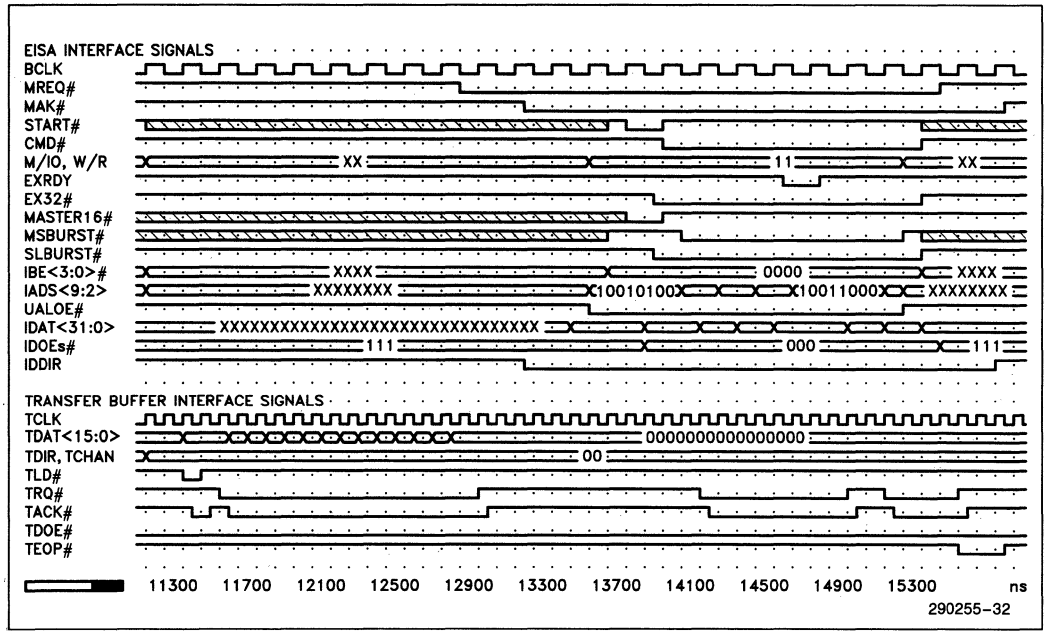


Figure 10-2. 32-Bit Burst Cycle (EISA Write)

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

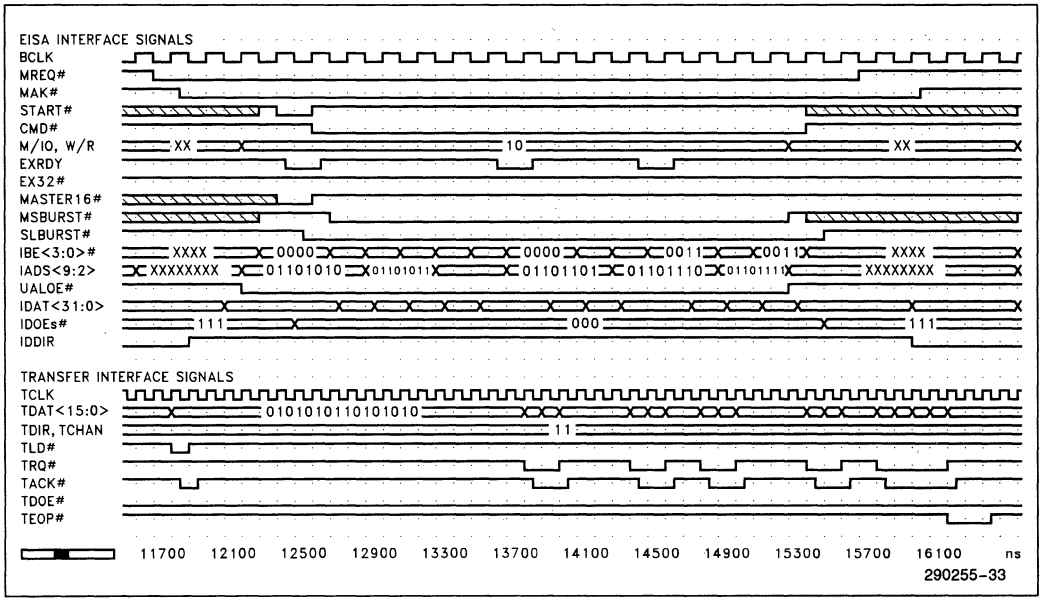


Figure 10-3. 16-Bit Burst Cycle (EISA Read)

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

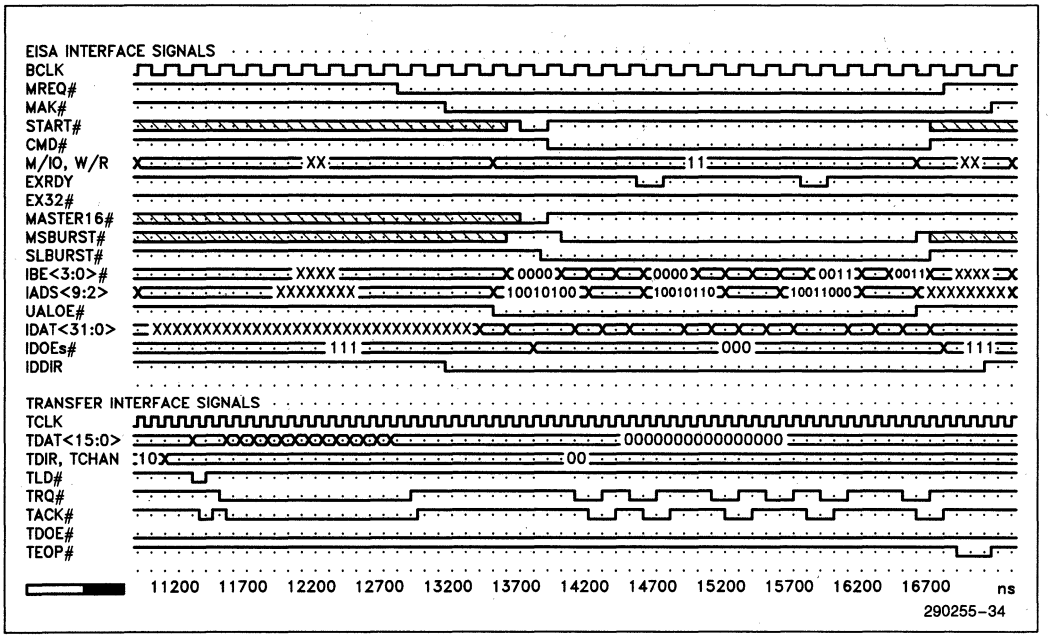


Figure 10-4. 16-Bit Burst Cycle (EISA Write)

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

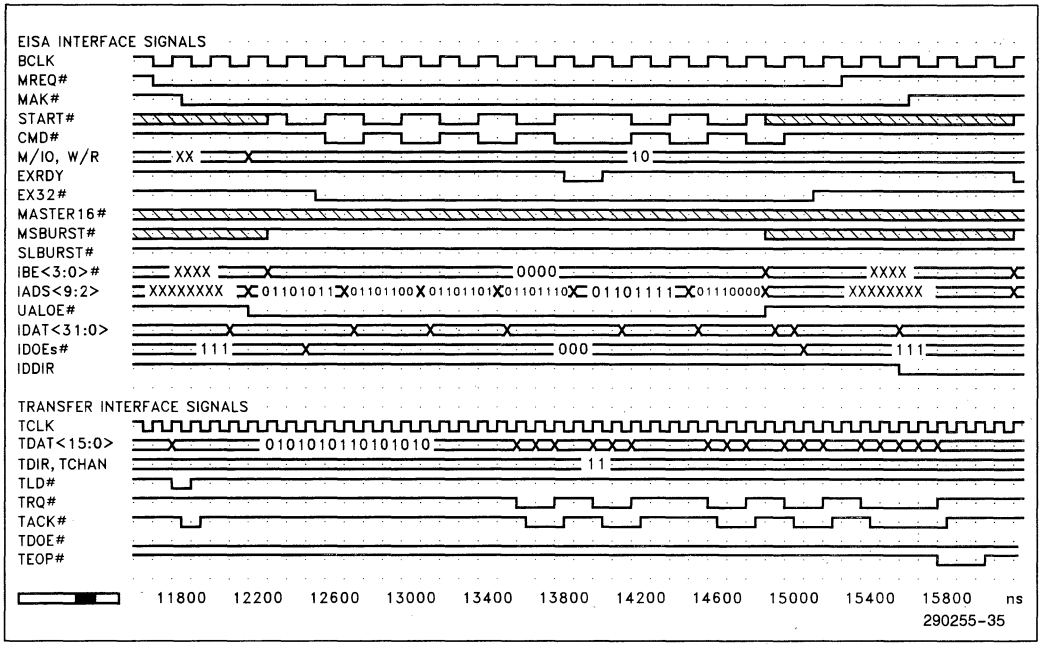


Figure 10-5. 32-Bit Non-Burst Cycle (EISA Read)

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

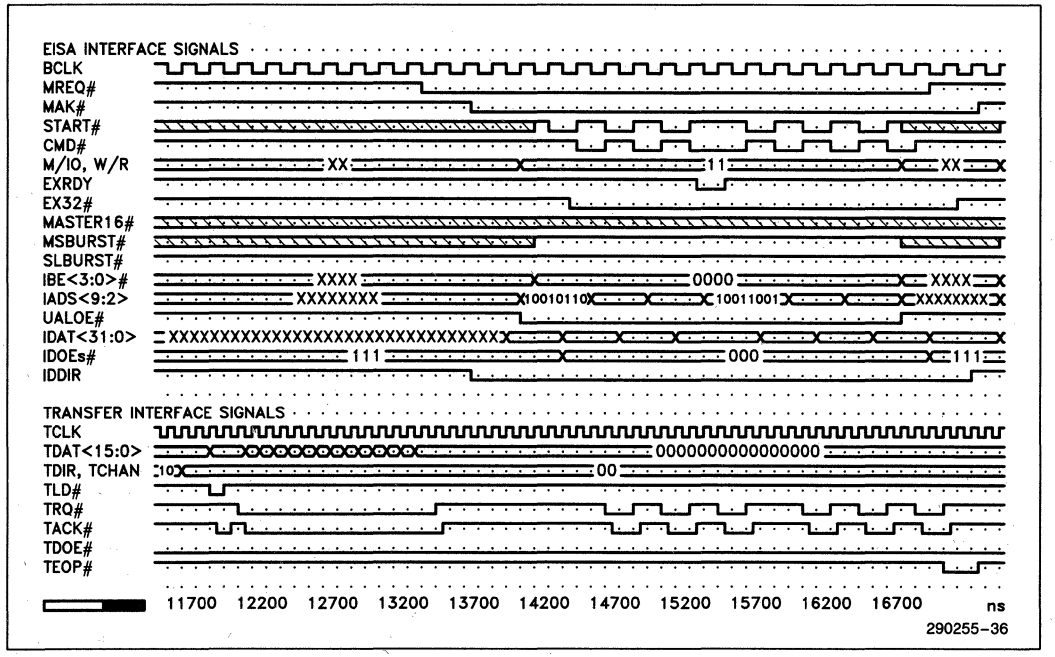


Figure 10-6. 32-Bit Non-Burst Cycle (EISA Write)

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

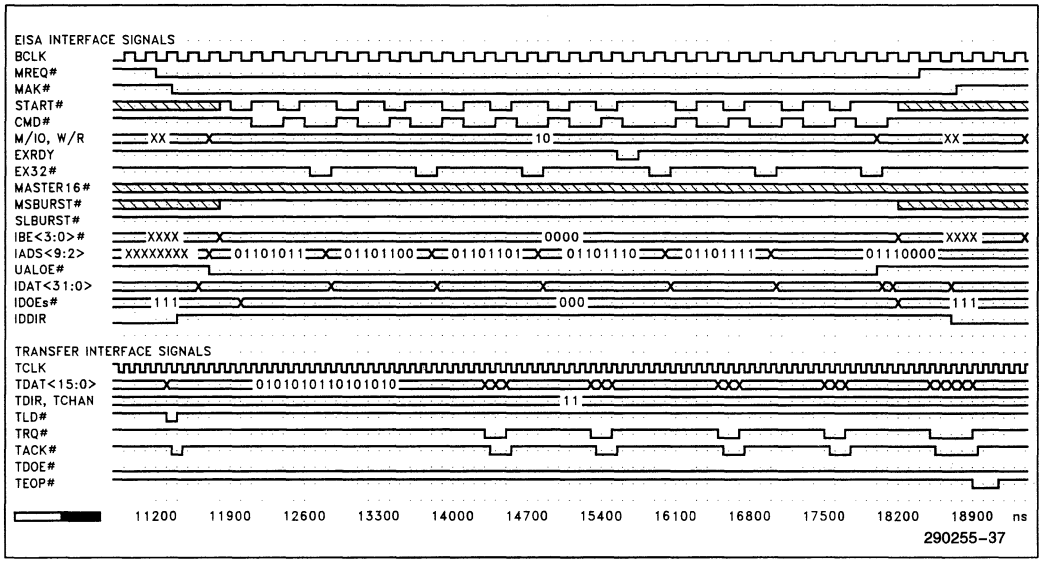


Figure 10-7. Mismatched Cycle (EISA Read)

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

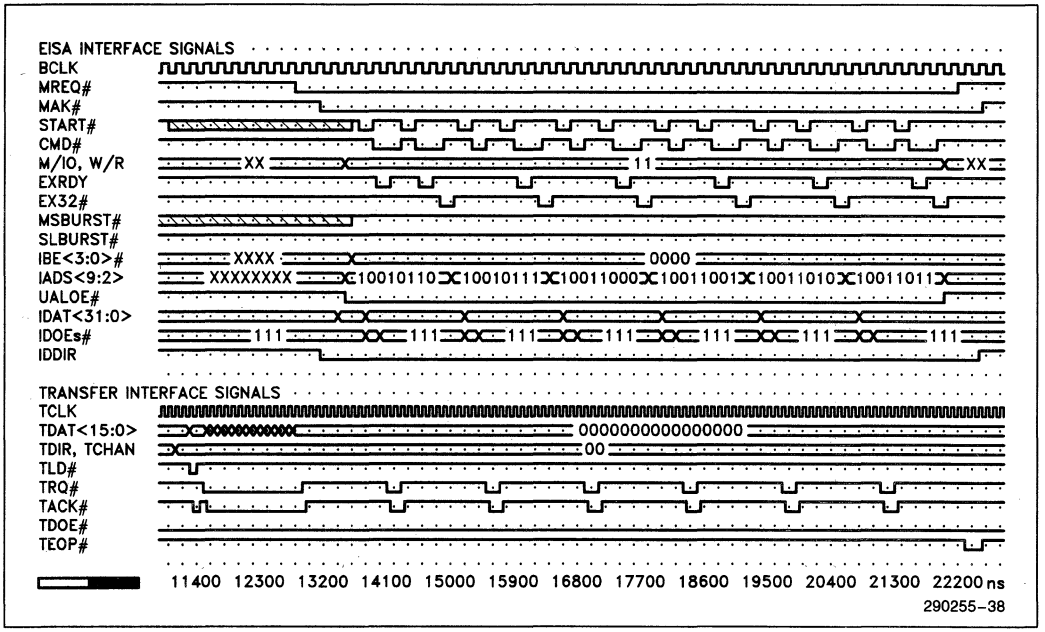


Figure 10-8. Mismatched Cycle (EISA Write)

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

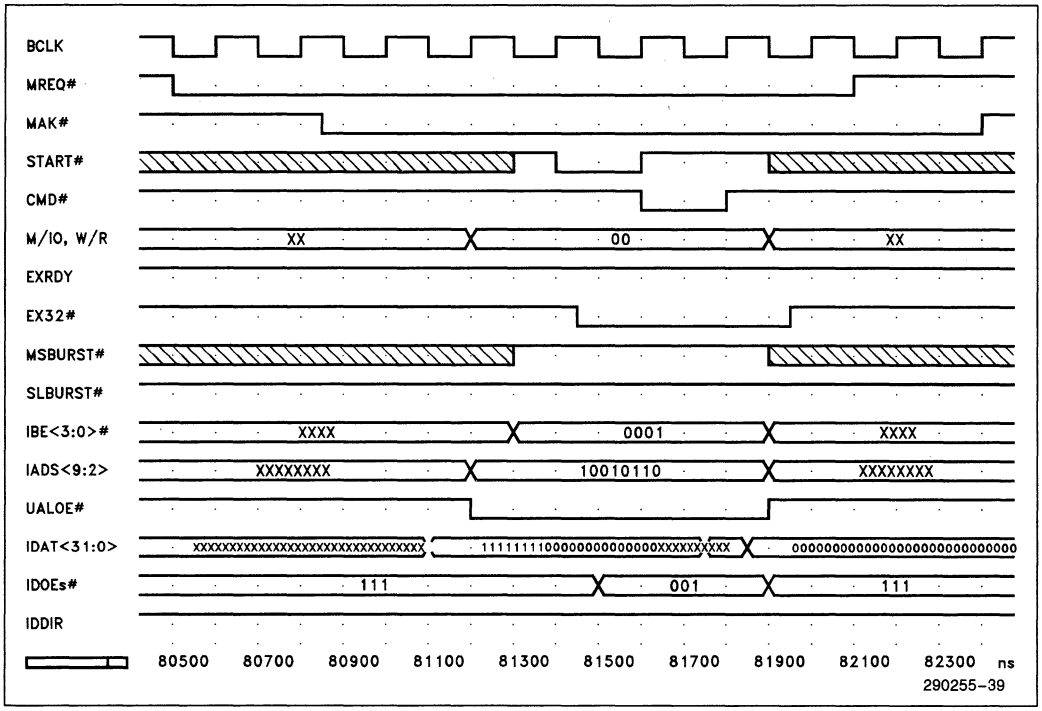


Figure 10-9. I/O Peek Cycle

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

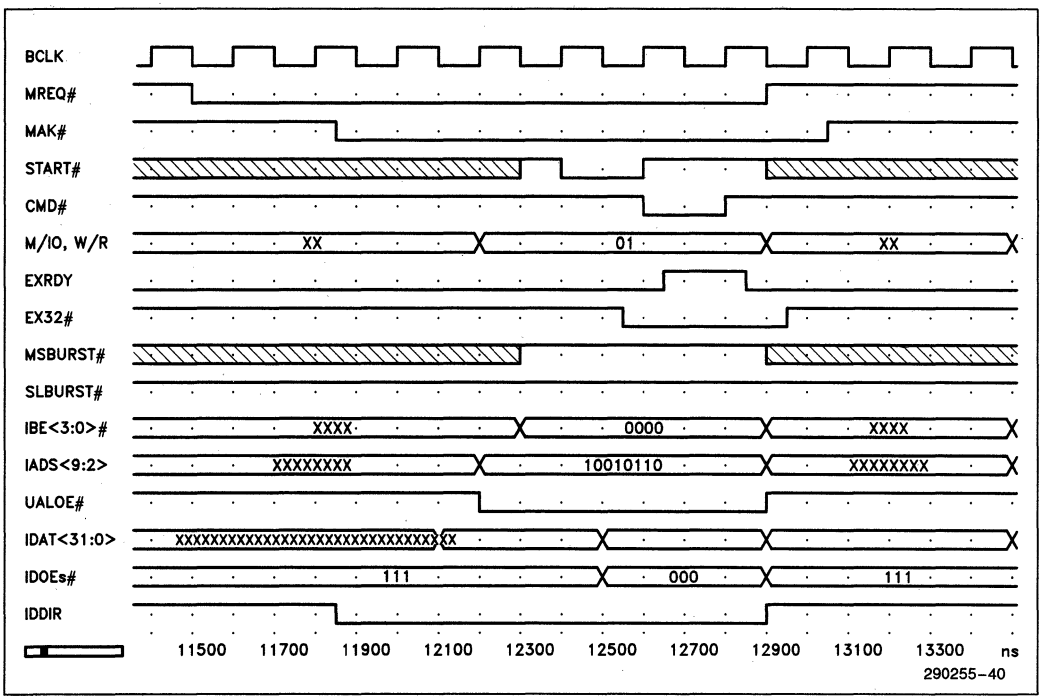


Figure 10-10. I/O Poke Cycle

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

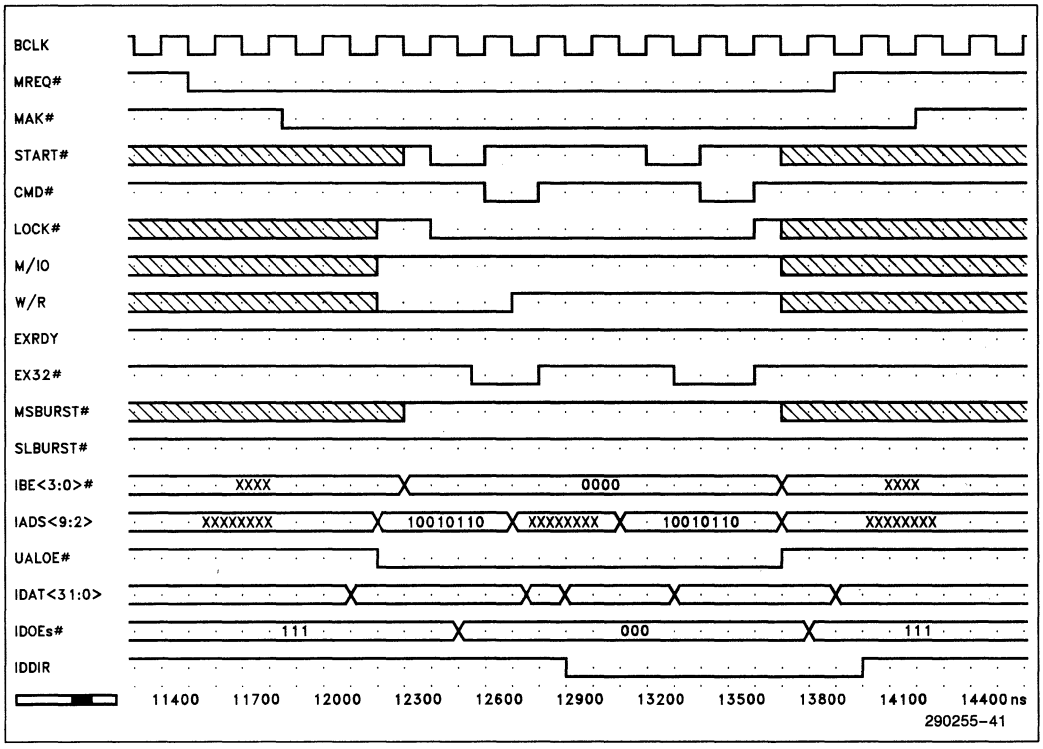


Figure 10-11. Locked Exchange Cycle

10.0 BASIC FUNCTION TIMING DIAGRAMS (Continued)

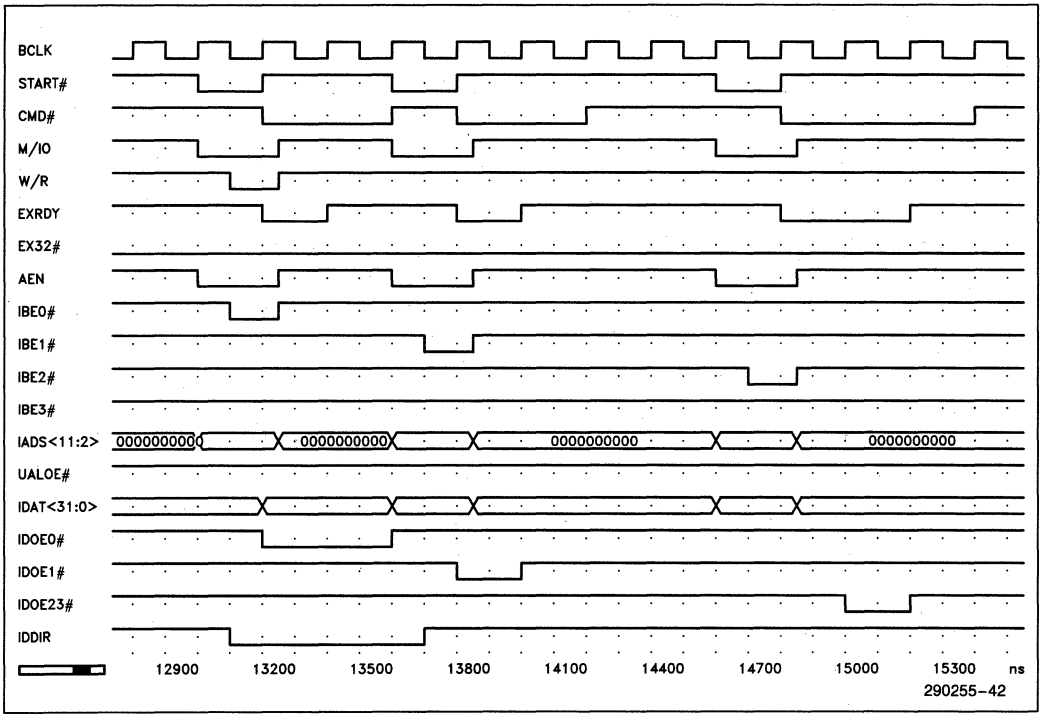


Figure 10-12. Slave Access to BMIC

11.0 D.C. SPECIFICATIONS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

11.1 Maximum Ratings*

Case Temperature under Bias . . . −65°C to +110°C

Storage Temperature . . . . . −65°C to +150°C

Supply Voltages with Respect to Ground . . . . . −0.5V to +6.5V

Voltage on Any Pin . . . . . −0.5V to V_{CC} + 0.5V

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

1

11.2 D.C. Characteristics Table

T_{CASE} = 0°C to 70°C, V_{CC} = 5V ±5%, $T_{AMBIENT}$ = 0°C to 55°C

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{ILC}	CLOCK Input Low	−0.5	0.8	V	
V_{IHC}	CLOCK Input High	2.0	V_{CC}+0.5	V	
V_{OL1}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA
V_{OH1}	Output High Voltage	2.4		V	I_{OH} = −2.5 mA
V_{OL2}	Output Low Voltage		0.45	V	I_{OL} = 6 mA
V_{OH2}	Output High Voltage	2.4		V	I_{OH} = −4 mA
V_{OL3}	Output Low Voltage		0.45	V	I_{OL} = 24 mA
V_{OH3}	Output High Voltage	V_{CC}−0.4		V	I_{OH} = −100 µA
V_{OL4}	Output Low Voltage		0.45	V	I_{OL} = 4.0 mA
V_{OH4}	Output High Voltage	2.4		V	I_{OH} = −2.5 mA
ILI	Input Leakage		±10	µA	
ILO	Output Leakage		±10	µA	
C_{IN}	Capacitance Input		10	pF	@ 1 MHz(2)
C_{OUT}	Capacitance Output or I/O		12	pF	@ 1 MHz(2)
C_{CLK}	BCLK or TCLK		15	pF	@ 1 MHz(2)
I_{CC}	V_{CC} Supply Current		190	mA	(3)

NOTES:

1. V_{OL1} = IDOE23#, IDOE1#, IDOE0#, LRDY, LDAT<7:0>, IDAT<31:0>, TEOP#, TDIR, TCHAN, IOSEL0#, IOSEL1#, TRQ#, TLD#, and TDAT<15:0>
   V_{OL2} = MREQ#, EINT, and LINT
   V_{OL3} = IADS<9:2>, START#, M/IO, W/R, EXRDY, MASTER16#, EX32#, IBE#<3:0>, MSBURST#, and LOCK#
   V_{OL4} = UALOE#, IDDIR
   V_{OH1} = IDOE23#, IDOE1#, IDOE0#, LRDY, LDAT<7:0>, IDAT<31:0>, TDIR, TCHAN, TRQ#, TLD#, IOSEL0#, IOSEL1#, TDAT<15:0>, MREQ#, EINT, LINT, and TEOP#
   V_{OH2} = IADS<9:2>, START#, M/IO, W/R, IBE#<3:0>, MSBURST#, LOCK#, EXRDY, EX32#, and MASTER16#
   V_{OH3} = UALOE#, IDDIR, IDOE23#, IDOE1#, IDOE0#, IADS<9:2>, LRDY, LDAT<7:0>, IDAT<31:0>, TDIR, TCHAN, EINT, IOSEL0#, IOSEL1#, TRQ#, TLD#, TDAT<15:0>, MREQ#, LINT, IADS<9:2>, START#, M/IO, W/R, IBE#<3:0>, MSBURST#, LOCK#, and TEOP#
   V_{OH4} = UALOE#, IDDIR
   The following outputs are open collector: EXRDY, EX32#, MASTER16#, and TEOP#; EINT is an open collector output when programmed for active low operation.
2. Sampled only
3. Tested at V_{CC} = 5.30V and Frequency = BCLK (8.33 MHz) and TCLK (20 MHz)

12.0 A.C. SPECIFICATIONS

12.1 A.C. Characteristics Tables

The A.C. specifications given in the following tables consist of output delays/float times and input setup and hold times.

T_{CASE} = 0°C to 70°C, V_{CC} = 5V ±5%, $T_{AMBIENT}$ = 0°C to 55°C

BCLK Timing

Symbol	Parameter	Min	Max	Units	Notes
t1	Period	120	2500	ns	Typical = 125 ns
t2	High Time	50		ns	Measured @ 2.0V
t3	Low Time	50		ns	Measured @ 0.8V
t4	Rise Time		10	ns	(13)
t5	Fall Time		10	ns	(13)

Reset Timing

Symbol	Parameter	Min	Max	Units	Notes
t6	Pulse Width	8 (t1)		ns	

Master Timing

Symbol	Parameter	Min	Max	Units	Notes
	MREQ#				
t7	Delay ACT/Inact		33	ns	From BCLK Falling
	MAK#				
t8	Setup Time	10		ns	To BCLK Falling
t9	Hold Time	25		ns	From BCLK Falling
	IADS<9:2>, M/IO, W/R				
t10	Delay Valid	2	45	ns	From BCLK Falling(17)
	IADS<9:2>, M/IO, W/R				
t10a	Delay Valid		75	ns	From BCLK Rising(18)
t11	Delay Float		40	ns	From BCLK Falling(7)
	IBE# <3:0>				
t12	Delay Valid	2	45	ns	From BCLK Falling
t13	Delay Float		40	ns	From BCLK Falling(7, 8)
	START#				
t14	Delay Act/Inact		25	ns	From BCLK Rising
t15	Delay Float		40	ns	From BCLK Falling(7, 8)
	EX32#				
t16	Setup Time	15		ns	To BCLK Rising(9)
t17	Hold Time	50		ns	From BCLK Rising(9)
	EXRDY				
t18	Setup Time	15		ns	To BCLK Falling
t19	Hold Time	2		ns	From BCLK Falling
	IDAT<31:0>				
t20	Delay Valid	3	27	ns	From BCLK Falling(1)
t21	Delay Float		25	ns	From BCLK Falling(7, 8)
t22	Setup Time	4		ns	To BCLK Rising(2)
t23	Hold Time	6		ns	From BCLK Rising(2)
	IDAT<31:10>				
t24	Delay Valid		45	ns	From BCLK Falling(10)
	LOCK#				
t25	Delay Act/Inact	2	60	ns	From BCLK Rising
t26	Delay Float		40	ns	From BCLK Falling(7)
	IDOE#				
t27	Delay Act/Inact		25	ns	From BCLK Falling
	UALOE#				
t28a	Delay Active		60	ns	From BCLK Rising
t28b	Delay Inactive		35	ns	From BCLK Falling
	IDDIR				
t29	Delay Act/Inact		40	ns	From BCLK Falling

Master Timing (Burst)

Symbol	Parameter	Min	Max	Units	Notes
	MSBURST#				
t30	Delay ACT/INACT		35	ns	From BCLK Falling
t31	Delay Float		40	ns	From BCLK Rising(8)
	START#, IBE# <3:0>				
t31a	Delay Float		40	ns	From BCLK Rising(19)
	SLBURST#				
t32	Setup Time	15		ns	To BCLK Rising
t33	Hold Time	50		ns	From BCLK Rising
	IDOE#				
t34	Delay Act/Inact		25	ns	From BCLK Rising
	IDAT<31:0>				
t35	Setup Time (Read)	5		ns	To BCLK Rising(2)
t36	Hold Time (Read)	6		ns	From BCLK Rising(2)
t37	Delay Valid	3	27	ns	From BCLK Rising(1)
t38	Delay Invalid	0		ns	From BCLK Rising(1)
	MASTER16#				
t39	Delay Act		50	ns	From BCLK Rising
t40	Delay Float	1	40	ns	From BCLK Rising(7,8)

Slave Timing

Symbol	Parameter	Min	Max	Units	Notes
	IADS<11:12>, M/IO				
t41	Setup Time	120		ns	To CMD# Falling
t42	Hold Time	25		ns	From CMD# Falling
	EX32#				
t43	Delay Act/Float		54	ns	From IADS<11:2>, M/IO
t44	Delay Act/Float		34	ns	From AEN
	AEN				
t45	Setup Time	95		ns	To CMD# Falling
t46	Hold Time	25		ns	From CMD# Falling
	START#				
t47	Pulse Width	110		ns	
	IBE#<3:0>, W/R				
t48	Setup Time	80		ns	To CMD# Falling
t49	Hold Time	25		ns	From CMD# Falling
	EXRDY				
t50	Delay Negated		124	ns	From START# Falling(3)
t51	Delay Float	1	40	ns	From BCLK Falling
	CMD#				
t52	Pulse Width	110		ns	
	IDAT<31:0>				
t53	Setup Time	−35		ns	To CMD# Falling(2)
t54	Hold Time	0		ns	From CMD# Rising(2)
t55	Delay Valid		100	ns	From BCLK Rising(1)
t56	Delay Invalid	0		ns	From CMD# Rising(1)
t57	Delay Float		50	ns	From CMD# Rising
	IDDIR				
t58	Delay Valid		50	ns	From W/R Valid
t59	Delay Invalid	2		ns	From CMD# Rising
	IDOE#				
t60	Delay Act (Read)		25	ns	From CMD# Falling
t61	Delay Inact (Read)		20	ns	From CMD# Rising
t62	Delay Act/Inact (Write)		45	ns	From BCLK Rising
	IOSEL#				
t63	Delay Active		60	ns	From IADS<11:2>
t64	Delay Inactive	5		ns	From CMD# Rising If Latched

Transfer Buffer Interface Timing

Symbol	Parameter	Min	Max	Units	Notes
	TCLK				
t65	Period	50	250	ns	
t66	High Time	18		ns	Measured @ 2.0V
t67	Low Time	20		ns	Measured @ 0.8V
	TRQ#				
t68	Delay Act/Inact		15	ns	From TCLK Rising
	TLD#				
t69	Delay Act/Inact		25	ns	From TCLK Rising
	TEOP#				
t70	Delay Act/Float		25	ns	From TCLK Rising
	TCHAN, TDIR				
t73	Setup Time	25		ns	To TLD# or TRQ# Active(11)
	TACK#				
t74	Setup Time	15		ns	To TCLK Rising
t75	Hold Time	1		ns	To TCLK Rising
	TDAT<15:0>				
t76	Delay Valid	4	25	ns	From TCLK Rising/TDOE# Falling
t77	Delay Float		25	ns	From TCLK/TDOE# Rising
t78	Setup Time	10		ns	To TCLK Rising
t79	Hold Time	1		ns	From TCLK Rising
t80	Ratio of TCLK to BCLK	1.1			

Local Processor Interface Timing (Read Cycle)

Symbol	Parameter	Min	Max	Units	Notes
	LADS<1:0>, LCS#				
t81	Setup Time	10		ns	To LRD# Falling
t82	Hold Time	0		ns	From LRD# Rising
	LRD#				
t83	Pulse Width	150		ns	
	LDAT<7:0>				
t84	Delay Valid		130	ns	From LRD# Falling(4)
t85	Max Delay Valid		2.5 (t1) + 120	ns	From LRD# Falling(5)
t86	Delay Float		40	ns	From LRD# Rising
	LRD# (Inact) to LRD# (Act) or LWR# (Act)				
t87	Recovery Time	60		ns	

Local Processor Interface (Write Cycle)

Symbol	Parameter	Min	Max	Units	Notes
	LADS<1:0>, LCS#				
t88	Setup Time	10		ns	To LWR# Falling
t89	Hold Time	0		ns	From LWR# Rising
	LWR#				
t90	Pulse Width	100		ns	(4)
	LDAT<7:0>				
t91	Setup Time	60		ns	To LWR# Rising(4)
t92	Hold Time	10		ns	From LWR# Rising
t93	Data Valid		70	ns	From LWR# Falling(5)
	LWR# (Inact) to LWR# (Act) or LRD# (Act)				
t94	Recovery Time	60		ns	

Local Processor Ready Timing

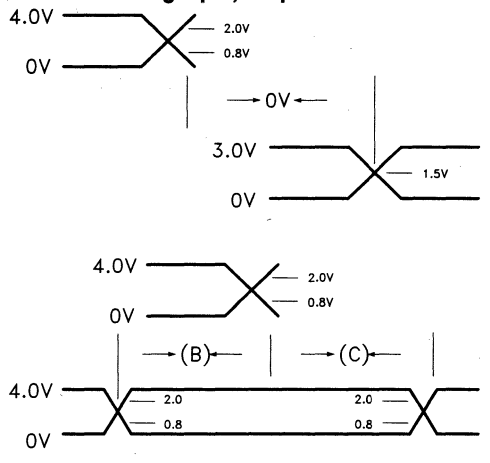
Symbol	Parameter	Min	Max	Units	Notes
	LRDY				
t95	Delay Inactive		50	ns	From LADS and LCS# Valid(5)
	Delay Active				From LRD# or LWR# Active
t96	Max Delay		3.5 (t1)+60	ns	(5, 6)
t97	Max Delay		2.5 (t1)+60	ns	(5, 6)
t98	Min Delay	1.5 (t1)		ns	(5, 6)
	LDAT<7:0>				
t99	Delay Valid		0	ns	From LRDY Rising(5, 12)

NOTES FOR A.C TIMINGS:

1. Specification does not include allowance for 13 ns max. and 2 ns min. into 240 pF for external buffer delay to EISA bus.
2. Specification does not include allowance for 8 ns max. and 1 ns min. into 25 pF for external input delay from EISA bus.
3. Delay includes 40 ns for pull-up rise time (300Ω into 240 pF, 2V rise).
4. Applies to all non-shared registers excluding the Peek/Poke Data registers. LRDY will remain active.
5. Applies to the Peek/Poke Data and Shared Registers. LRDY will be taken inactive as soon as LA<1:0> and LCS# are valid, and remain inactive until valid data is available, or has been written. The deassertion of the local read strobe (LRD#) or local write strobe (LWR#) indicates the end of the current shared register or peek/poke data register access. If the local chip select (LCS#) input remains asserted and the local address selects remain low (LADS<1:0>) after LRD# or LWR# deasserts, a new shared register or peek/poke data register cycle begins. Under these conditions, the LRDY output will become inactive again (driven low) within the time specified by t95.
6. The maximum LRDY delay, 3.5 (t1) + 60 ns from LRD# or LWR#, only occurs if the local processor access loses the internal register access arbitration to an EISA access and if the following BCLK cycle is stretched. Without BCLK stretching, the maximum delay is 2.5 (t1) +60 ns. The minimum LRDY delay is 1.5 (t1). **NOTE:** The maximum BCLK stretch that will be seen by the BMIC is one BCLK period; this is assuming that the bus controller is the 82358 (EBC). If the 82358 is not used as the bus controller, the LRDY and data delay max. specs (t96/t85) will not necessarily be valid.
7. Exiting master mode, the address lines <31:2>, M/IO, LOCK# START#, IBE#<3:0>, MSBURST#, IDAT<31:0>, and W/R will float no later than the falling edge of BCLK after CMD# is deasserted.
8. During a mismatched cycle START#, IBE#<3:0>, and IDAT<31:0> will float from the first falling edge of BCLK after START# is negated.
9. Includes mismatched cycles.
10. Refers to the upper 22 EISA address lines which are multiplexed into the upper 22 data lines IDAT<31:10>. The address will be available for latching into the external address latches 45 ns from the falling edge of BCLK.
11. The TDIR and TCHAN signals are referenced to the falling edge of TRQ# during the cycles that TLD# is not requested.
12. LRDY going active will always be delayed from data valid. The maximum delay seen will be no greater than one (t1) period.
13. Characterized, not tested.
14. Under non-preempt, MREQ# will deassert a minimum of 0.5 BCLKs after the negating edge of the last CMD# of the transfer, depending on the cycle type (refer to the Basic Function Timings, Section 10.0).
15. During an EISA read transfer, the BMIC will assert TEOP# typically eight TCLKs after CMD# is deasserted from the last EISA cycle, indicating end of transfer (refer to the Basic Function Timings, Section 10.0).
16. During an EISA write transfer, the BMIC will assert TEOP# two TCLKs after CMD# is deasserted, indicating end of transfer (refer to the Basic Function Timings, Section 10.0).
17. For address changes while CMD# is active.
18. During an upper address load cycle, at the beginning of a transfer sequence, CMD# is inactive.
19. For "Downshifting Cases" where the transfer is misaligned.

12.2 A.C. Characteristics Waveforms

A.C. Testing Input, Output Waveforms



290255-12

NOTE:
The input waveforms have tr < 2.0 ns from 0.8V to 2.0V

A. Output delay specification referenced from one of the following signals: BCLK, TCLK, CMD#, START#, AEN, IADS<11:2>, W/R, TDOE#, LRD#, LWR#, LADS<1:0>, LCS#, LRD#, or LWR#.

B. Minimum input setup specification referenced to one of the following signals: BCLK, TCLK, CMD#, LWR#, LRD#, TLD#, or TRQ#.

C. Minimum input hold specification referenced to one of the following signals: BCLK, TCLK, CMD#, LWR#, LRD#, TLD#, or TRQ#.

A.C. Testing: All inputs are driven at 4V for a logic "1" and 0V for a logic "0". A.C. Timings are measured from the 0.8V and 2.0V levels on the source signal to either the 0.8V and 2V or 1.5V level on the signal under test; except as noted by the following:

1. BCLK and TCLK high time measurements are made at 2.0V
2. BCLK and TCLK low time measurements are made at 0.8V
3. START#, CMD#, LRD#, and LWR# pulse width measurements are made at 0.8V

A.C. TEST LOADS

CL = 25 pF on IDAT<31:0>, IDOE#, IOSEL#<1:0>, TRQ#, TLD#, TEOP#, TDAT<15:0>, TCHAN, TDIR, LRDY, and LDAT<7:0>

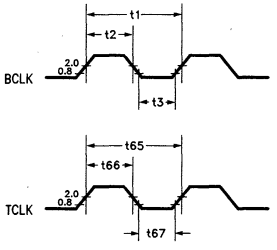
CL = 35 pF on IDDIR

CL = 50 pF on UALOE# and LINT

CL = 120 pF on MREQ# and EINT

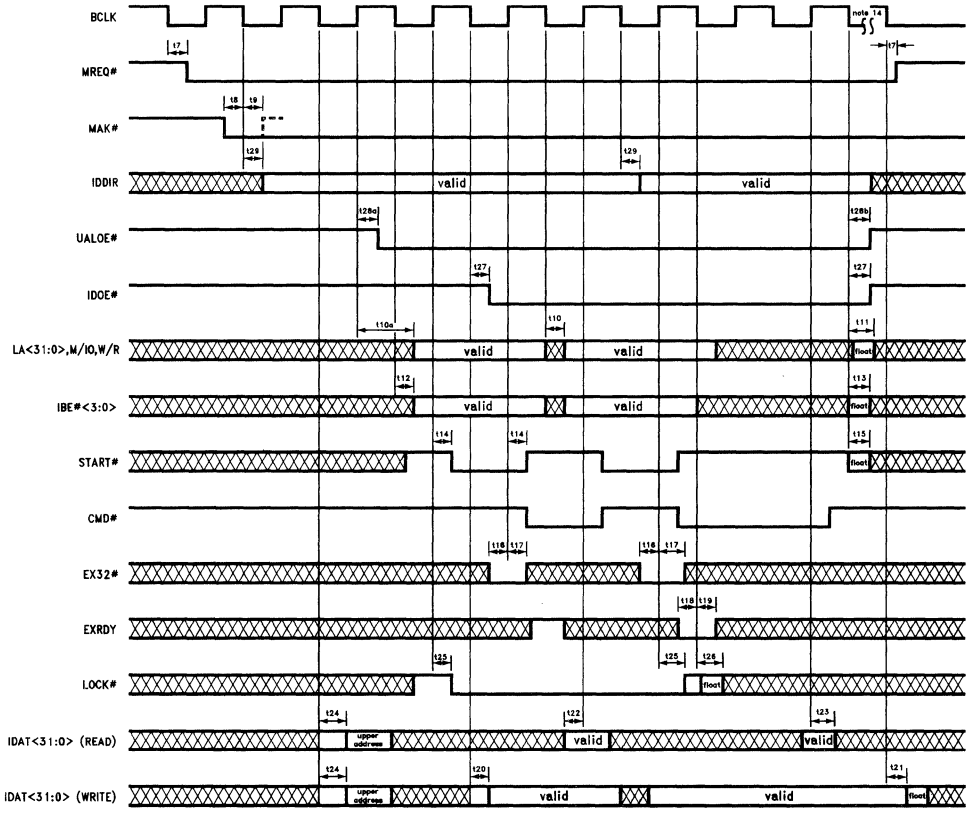
CL = 240 pF on IADS<9:2>, BE#<3:0>, W/R, START#, EX32#, LOCK, MSBURST#, MASTER16#, EXRDY, and M/IO

BCLK, TCLK Timing



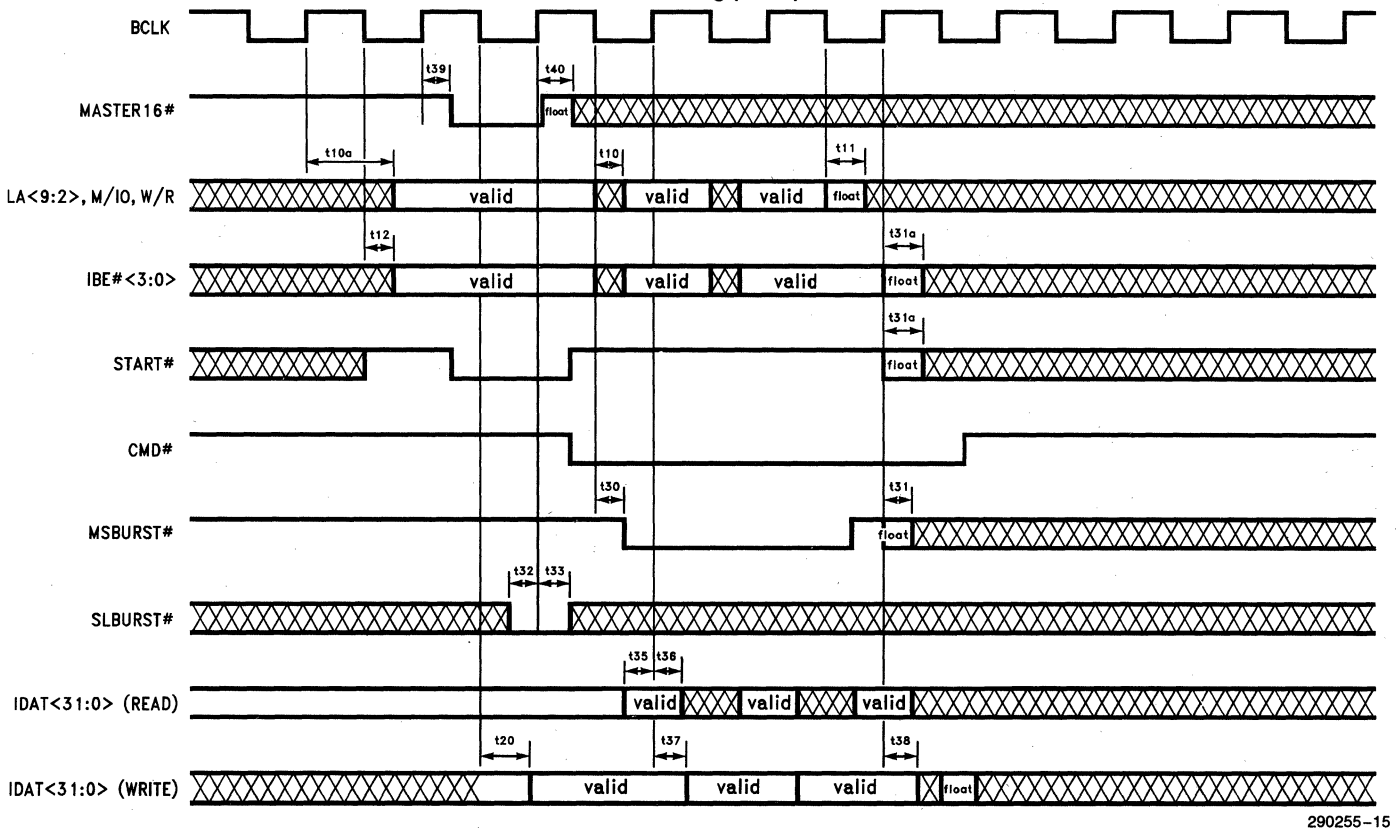
290255-13

Master Timing
(Includes: all Cycle Types—Initial Burst, Non-Burst, Peek/Poke, and Mismatched)

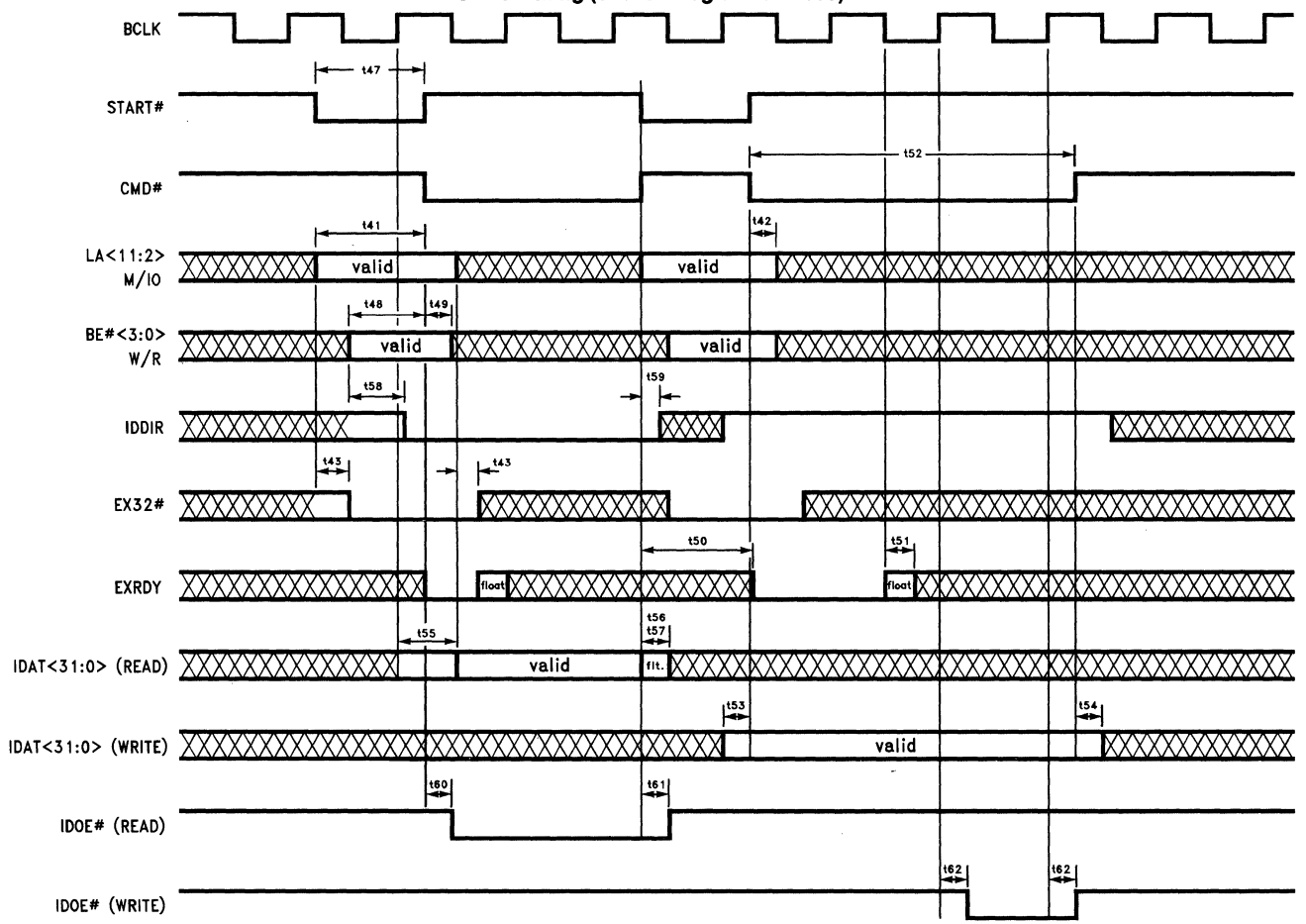


290255-14

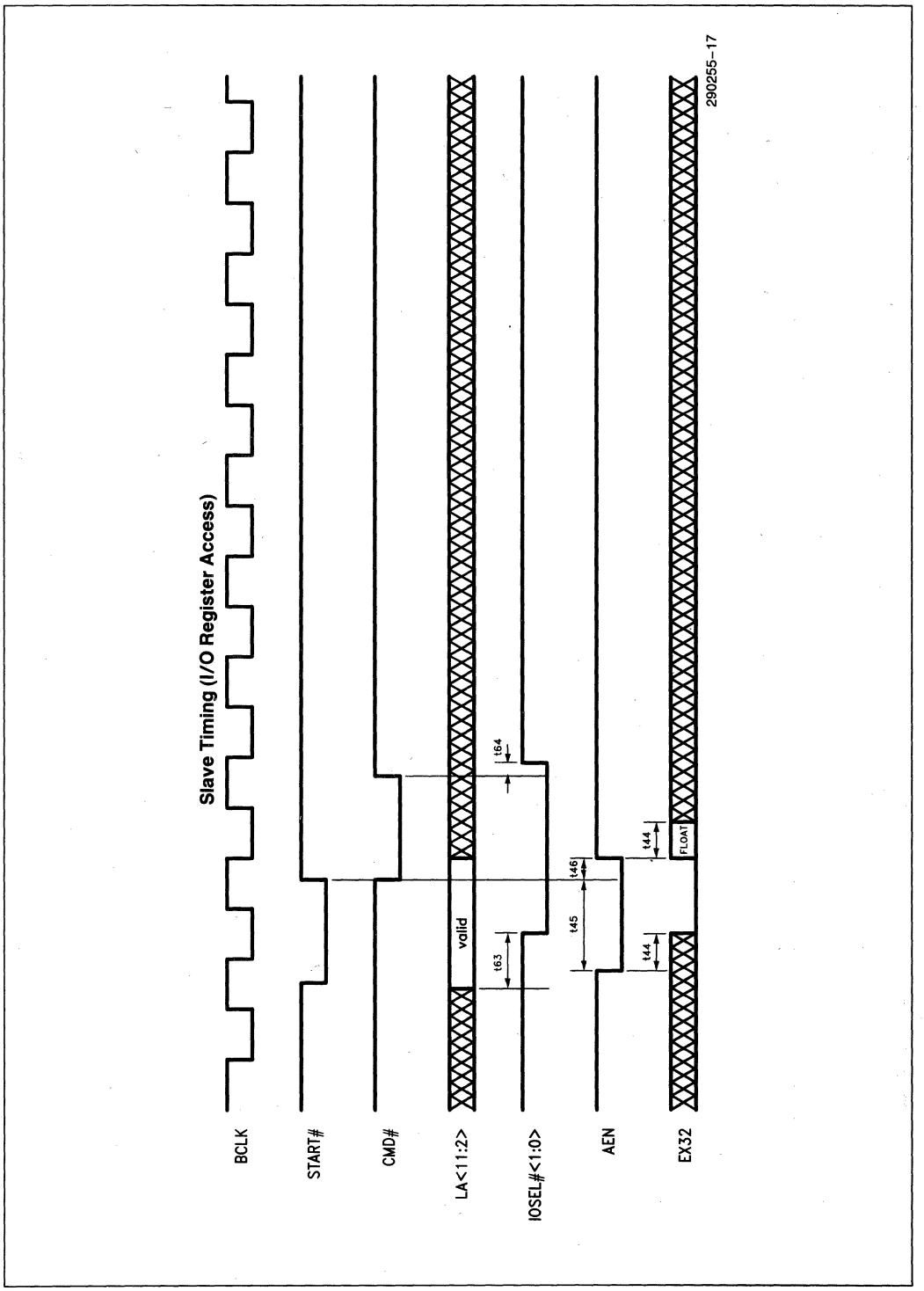
Master Timing (Burst)



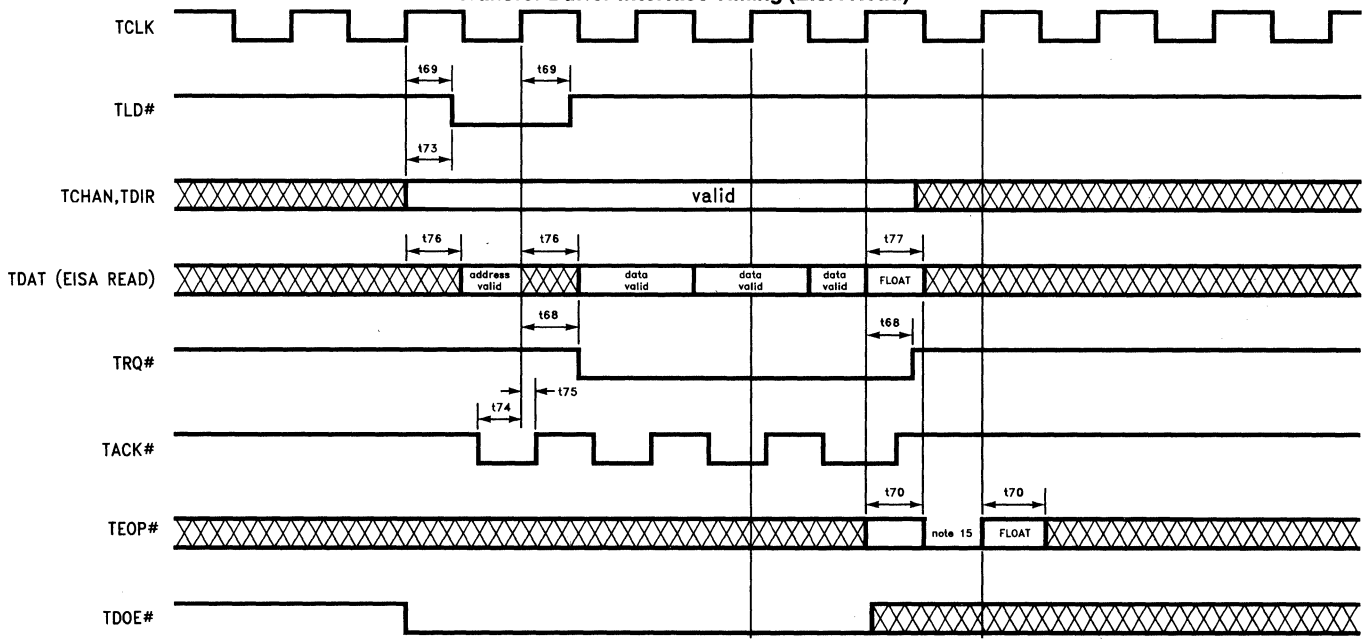
Slave Timing (Shared Register Access)



290255-16

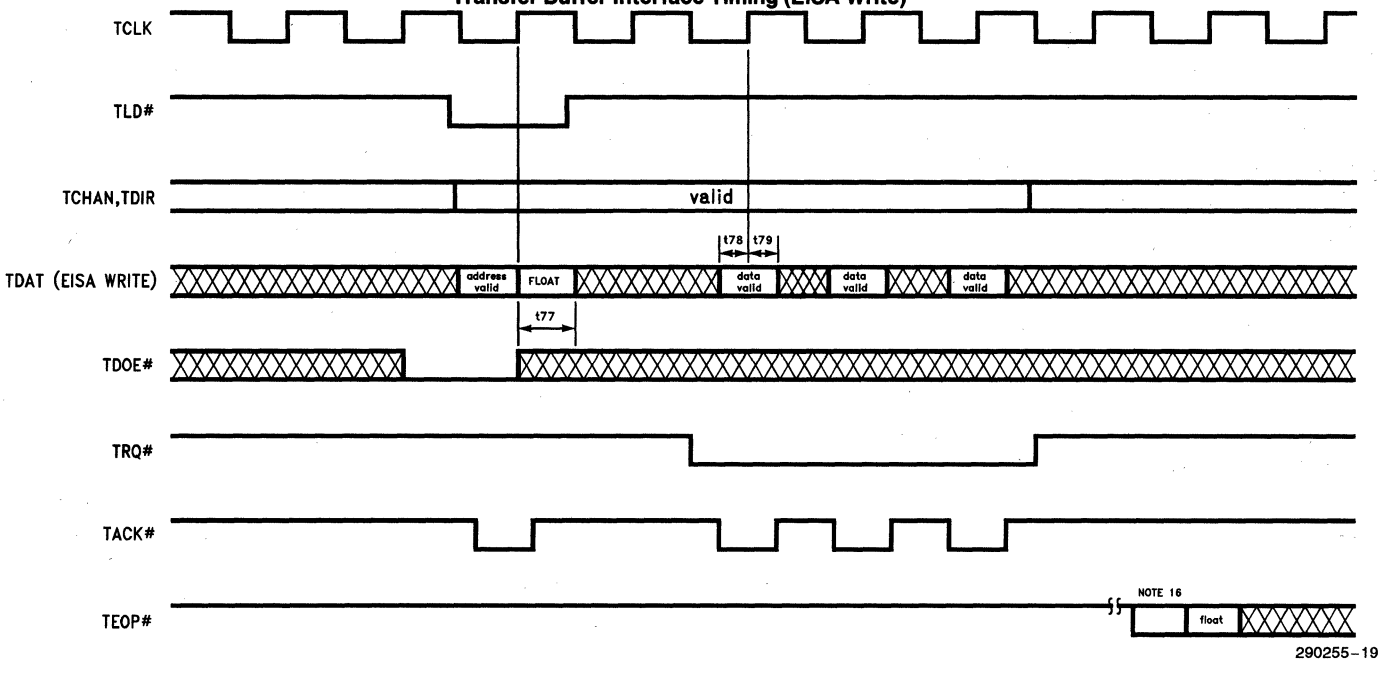

Slave Timing (I/O Register Access)
BCLK
START#
CMD#
LA<11:2>
IOSEL#<1:0>
AEN
EX32
valid
FLOAT
t63
t64
t45
t46
t44
t44
290255-17

Transfer Buffer Interface Timing (EISA Read)

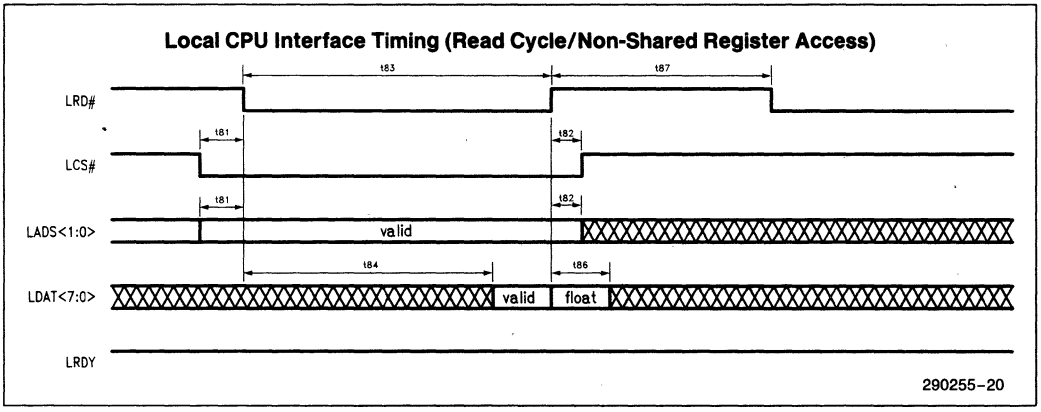


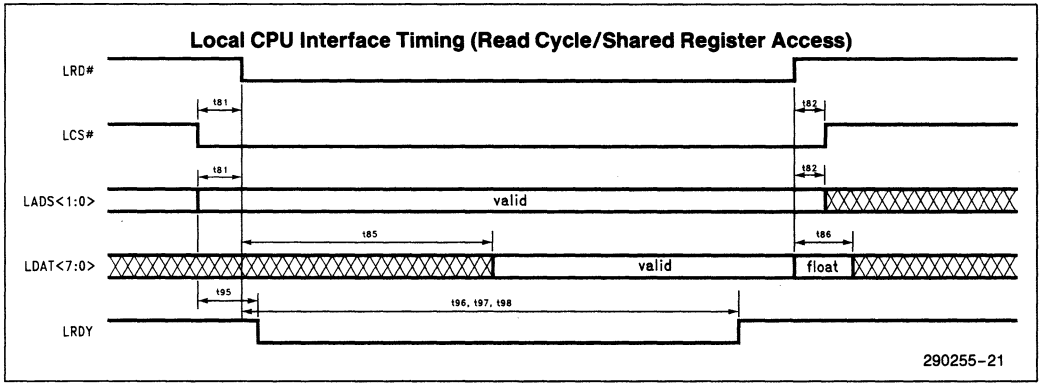
290255-18

Transfer Buffer Interface Timing (EISA Write)

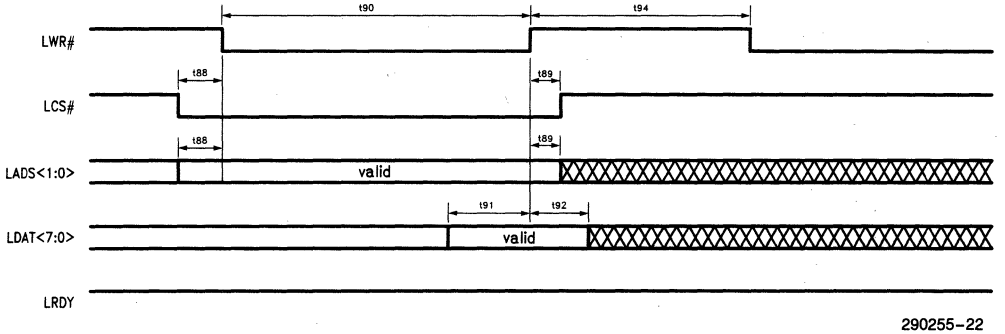


290255-19


Local CPU Interface Timing (Read Cycle/Non-Shared Register Access)
t83
t87
LRD#
t81
t82
LCS#
t81
t82
LADS<1:0>
valid
t84
t86
LDAT<7:0>
valid
float
LRDY
290255-20

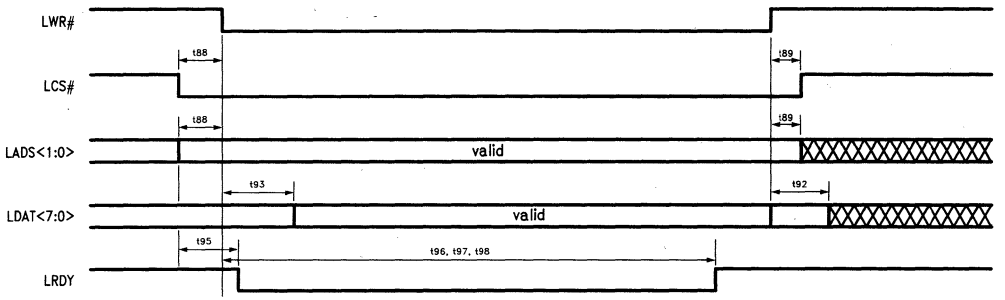

Local CPU Interface Timing (Read Cycle/Shared Register Access)
LRD#
t81
t82
LCS#
t81
t82
LADS<1:0>
valid
t85
t86
LDAT<7:0>
valid
float
t95
t96, t97, t98
LRDY
290255-21

Local CPU Interface Timing (Write Cycle/Non-Shared Register Access)



290255-22

Local CPU Interface Timing (Write Cycle/Shared Register Access)



290255-23

13.0 BMIC PN AND PACKAGE INFORMATION

13.1 Signal Overview

Name = Pin Name, Type = I—Input, O—Output, OC—Open Collector, B—Both Input and Output, BC—Both and Open Collector, Pin = Pin Location

Name	Type	Pin	Description
EISA BUS INTERFACE SIGNALS			
START#	B	84	EISA Start of Cycle
CMD#	I	102	EISA Command Strobe
M/IO	B	81	EISA Memory/IO Cycle Status Signal
W/R	B	80	EISA Write/Read Status Signal
EXRDY	I, OC	103	EISA Ready Signal
EX32#	I, OC	104	EISA 32-Bit Slave Response Signal
MASTER16#	OC	82	EISA 16-Bit Master Control Signal
IBE#<3:0>	B	64, 61, 60 59	EISA Byte Enable Lines
AEN	I	107	EISA Address Enable Signal
MSBURST#	O	96	EISA Master Burst Signal
SLBURST#	I	97	EISA Slave Burst Signal
LOCK#	O	98	EISA Resource Lock Signal
MREQ#	O	99	EISA Bus Master Request Signal
MAK#	I	100	EISA Master Bus Acknowledge Signal
EINT	OC	109	EISA Interrupt Request Signal
BCLK	I	101	EISA Bus Clock
RESET	I	125	EISA Reset Signal
IDAT<31:0>	B	Section	EISA Data Lines
IADS<11:10>	I	105, 106	EISA Address Input Lines
IADS<9:2>	B	57–55, 53, 44, 40–38	EISA Lower Address Lines
EISA BUFFER CONTROL SIGNALS			
UALOE#	O	78	EISA Upper Address Latch and Output Enable
IDDIR	O	79	EISA Data Buffer Direction Signal
IDOE23#	O	75	EISA Data Byte Line Buffer Enable (Bytes 3, 2)
IDOE#<1:0>	O	76, 77	EISA Data Byte Line Buffer Enables (Bytes 1, 0)
TRANSFER BUFFER INTERFACE SIGNALS			
TCLK	I	32	Transfer Clock
TRQ#	O	7	Transfer Data Request Signal
TACK#	I	6	Transfer Data Acknowledge Signal
TDIR	O	3	Transfer Data Direction Signal
TCHAN	O	4	Transfer Data Channel Select Signal
TLD#	O	5	Transfer Address Counter Load Signal
TDOE#	I	2	Transfer Data Bus Output Enable
TEOP#	I, OC	1	Transfer End-of-Process
TDAT<15:0>	B	Section	Transfer Data Bus Lines

13.1 Signal Overview (Continued)

Name = Pin Name, Type = I—Input, O—Output, OC—Open Collector, B—Both Input and Output, BC—Both and Open Collector, Pin = Pin Location

Name	Type	Pin	Description
LOCAL PROCESSOR INTERFACE SIGNALS			
LRD#	I	130	Local Read Signal
LWR#	I	129	Local Write Signal
LCS#	I	128	Local Chip Select Signal
LDAT<7:0>	B	121–118 115–112	Local Data Bus Lines
LADS<1:0>	I	127, 126	Local Address Register Select Signals
LRDY#	B	122	Local Ready Signal
LINT#	O	123	Local Processor Interrupt Signal
MISCELLANEOUS SIGNALS			
IOSEL#<1:0>	O	111, 110	Expansion Board Address Range Decode Signals
POWER PINS			
V_{CC}		108, 124	Power Pins for the Internal Logic
V_{SS}		42, 58	Ground Pins for the Internal Logic
V_{CCB}		12, 23, 41, 63, 74, 83, 94, 117, 132	Power Pins for the Output Buffers
V_{SSB}		13, 22, 33, 43, 54, 62, 73, 85, 95, 116, 131	Ground Pins for the Output Buffers

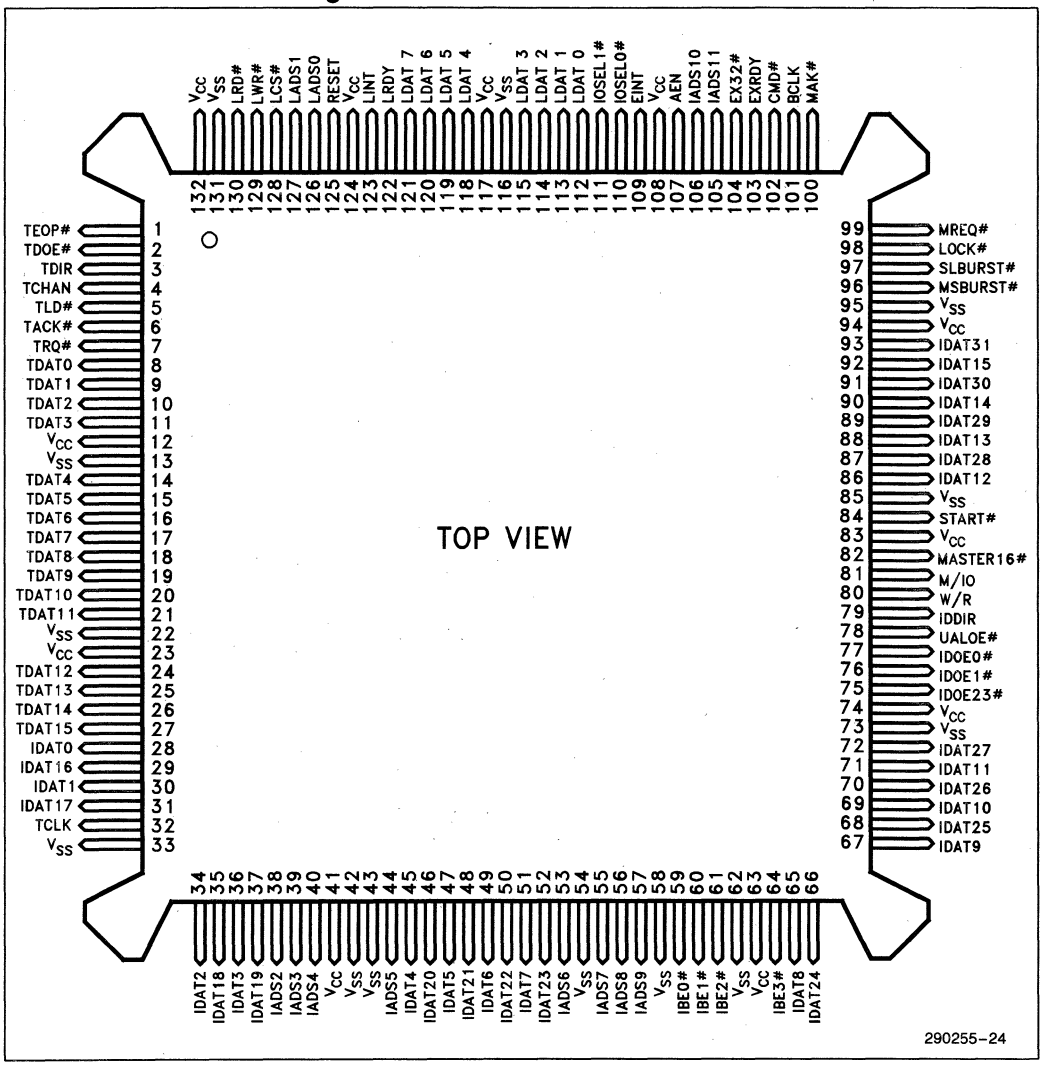
13.2 Device Pinout

I = Input, O = Output, OC = Open Collector, B = Both Input and Output, BC = Both and Open Collector

Device Pinout—132 Lead PQFP

A Row			B Row			C Row			D Row		
Pin	**Label**	**Type**	**Pin**	**Label**	**Type**	**Pin**	**Label**	**Type**	**Pin**	**Label**	**Type**
1	TEOP#	I, OC	34	IDAT2	B	67	IDAT9	B	100	MAK#	I
2	TDOE#	I	35	IDAT18	B	68	IDAT25	B	101	BCLK	I
3	TDIR	O	36	IDAT3	B	69	IDAT10	B	102	CMD#	I
4	TCHAN	O	37	IDAT19	B	70	IDAT26	B	103	EXRDY	I, OC
5	TLD#	O	38	IADS2	B	71	IDAT11	B	104	EX32#	I, OC
6	TACK#	I	39	IADS3	B	72	IDAT27	B	105	IADS11	I
7	TRQ#	O	40	IADS4	B	73	V_{SSB}		106	IADS10	I
8	TDAT0	B	41	V_{CCB}		74	V_{CCB}		107	AEN	I
9	TDAT1	B	42	V_{SS}		75	IDOE23#	O	108	V_{CC}	
10	TDAT2	B	43	V_{SSB}		76	IDOE1#	O	109	EINT	OC
11	TDAT3	B	44	IADS5	B	77	IDOE0#	O	110	IOSEL0#	O
12	V_{CCB}		45	IDAT4	B	78	UALOE#	O	111	IOSEL1#	O
13	V_{SSB}		46	IDAT20	B	79	IDDIR	O	112	LDAT0	B
14	TDAT4	B	47	IDAT5	B	80	W/R	B	113	LDAT1	B
15	TDAT5	B	48	IDAT21	B	81	M/IO	B	114	LDAT2	B
16	TDAT6	B	49	IDAT6	B	82	MASTER16#	OC	115	LDAT3	B
17	TDAT7	B	50	IDAT22	B	83	V_{CCB}		116	V_{SSB}	
18	TDAT8	B	51	IDAT7	B	84	START#	B	117	V_{CCB}	
19	TDAT9	B	52	IDAT23	B	85	V_{SSB}		118	LDAT4	B
20	TDAT10	B	53	IADS6	B	86	IDAT12	B	119	LDAT5	B
21	TDAT11	B	54	V_{SSB}		87	IDAT28	B	120	LDAT6	B
22	V_{SSB}		55	IADS7	B	88	IDAT13	B	121	LDAT7	B
23	V_{CCB}		56	IADS8	B	89	IDAT29	B	122	LRDY	B
24	TDAT12	B	57	IADS9	B	90	IDAT14	B	123	LINT	O
25	TDAT13	B	58	V_{SS}		91	IDAT30	B	124	V_{CC}	
26	TDAT14	B	59	IBE0#	B	92	IDAT15	B	125	RESET	I
27	TDAT15	B	60	IBE1#	B	93	IDAT31	B	126	LADS0	I
28	IDAT0	B	61	IBE2#	B	94	V_{CCB}		127	LADS1	I
29	IDAT16	B	62	V_{SSB}		95	V_{SSB}		128	LCS#	I
30	IDAT1	B	63	V_{CCB}		96	MSBURST#	O	129	LWR#	I
31	IDAT17	B	64	IBE3#	B	97	SLBURST#	I	130	LRD#	I
32	TCLK	I	65	IDAT8	B	98	LOCK#	O	131	V_{SSB}	
33	V_{SSB}		66	IDAT24	B	99	MREQ#	O	132	V_{CCB}	

13.3 132-Pin PQFP Package Pinout



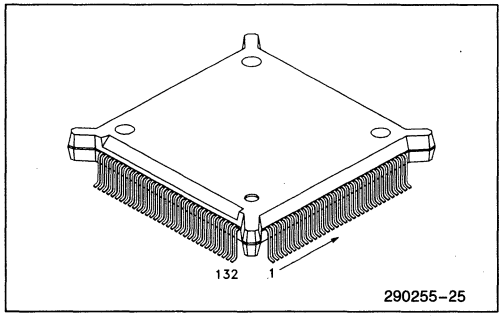
PACKAGING INFORMATION

(See Packaging Specification Order # 240800, Package Type NG)

Introduction

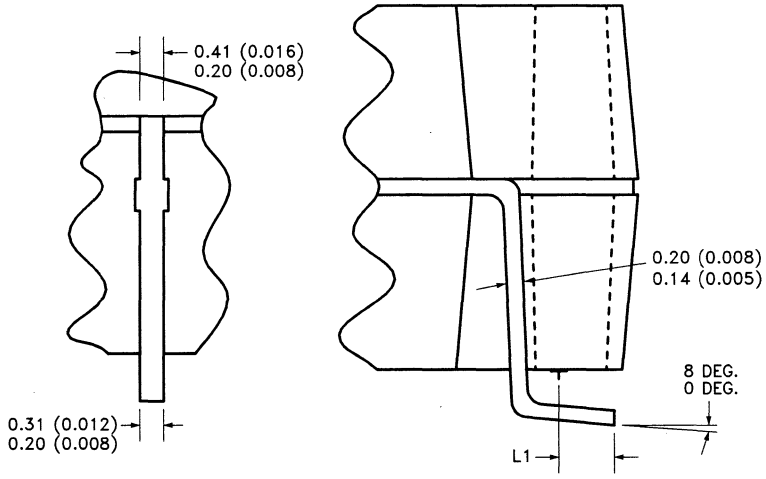
The individual components of Intel's EISA Chip Set come in JEDEC standard Gull Wing packages (25 MIL pitch), with "bumpers" on the corners for ease of handling. Please refer to the accompanying table for the package associated with each device, and to the individual component specifications for pinouts. (Note that the individual pinouts are numbered consistently with the numbering scheme depicted in the accompanying figures.)

PLASTIC QUAD FLAT PACK (PQFP)



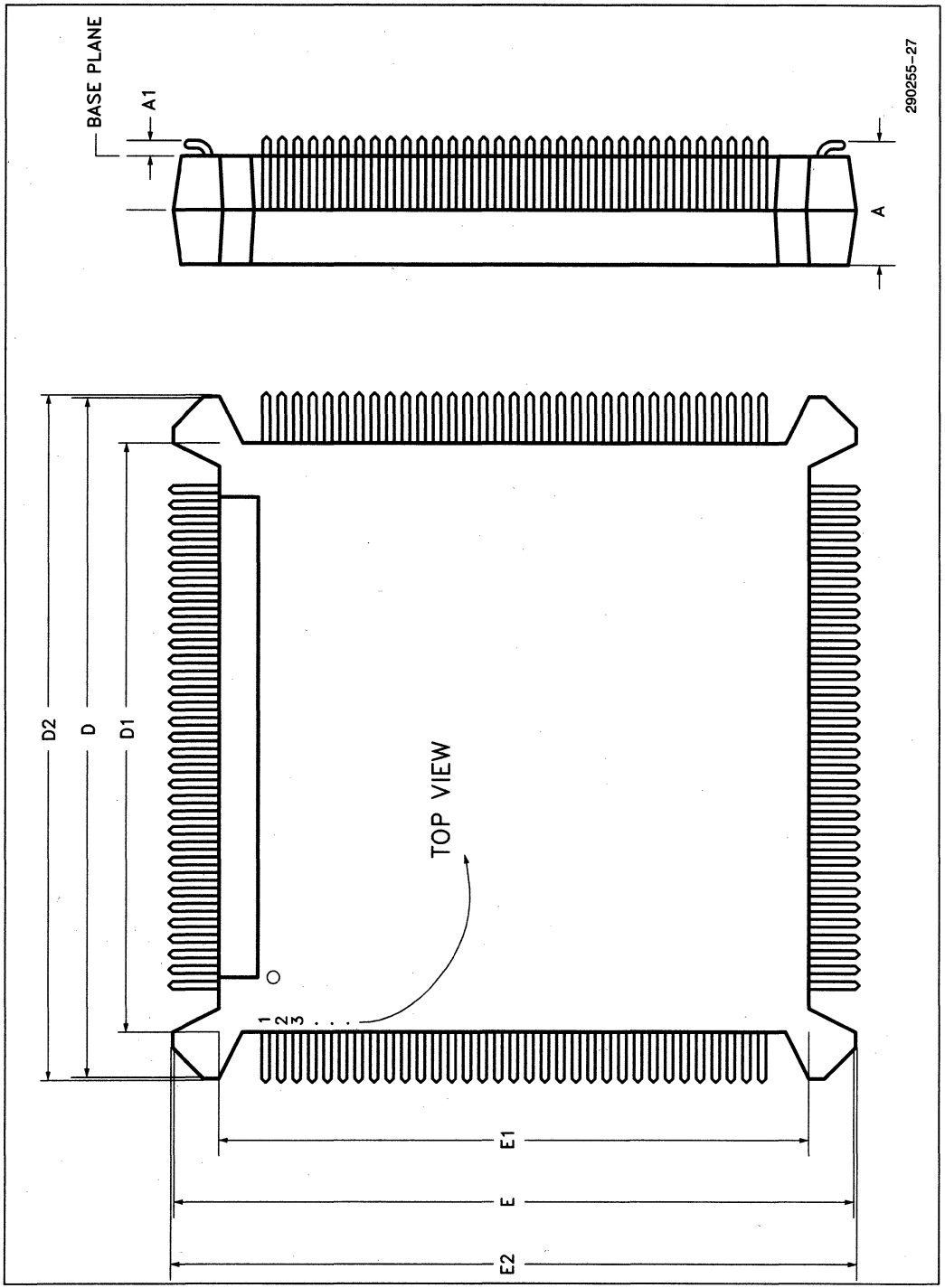
TYPICAL LEAD

Case Outline Drawings
Plastic Fine Pitch Chip Carrier
0.84 mm Pitch

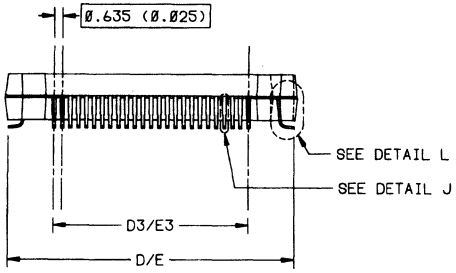


Symbol	Description	Inch		mm	
		Min	Max	Min	Max
N	Lead Count	132		132	
A	Package Height	0.160	0.170	4.06	4.32
A1	Standoff	0.020	0.030	0.51	0.76
D, E	Terminal Dimension	1.075	1.085	27.31	27.56
D1, E1	Package Body	0.947	0.953	24.05	24.21
D2, E2	Bumper Distance	1.097	1.103	27.86	28.02
D3, E3	Lead Dimension	0.800 Ref		20.32 Ref	
L1	Foot Length	0.020	0.030	0.51	0.76

13.4 PRINCIPAL DIMENSIONS & DATUMS



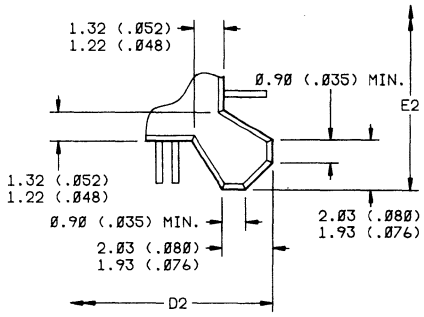
TERMINAL DETAILS



mm (inch)

290255-28

BUMPER DETAIL



mm (inch)

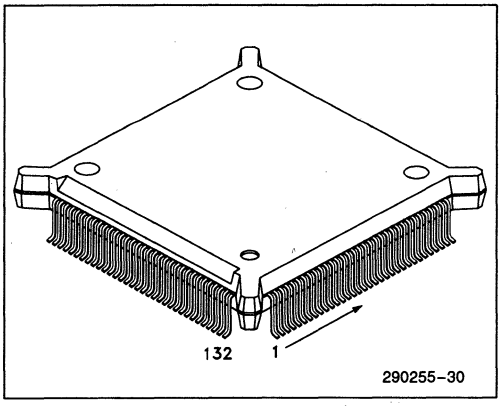
290255-29

13.5 Package Thermal Specification

The 82355 (BMIC) is specified for operation when the case temperature is within the range of 0°C–70°C. The case temperature may be measured in any environment, to determine whether the device is within the specified operating range.

The PQFP case temperature should be measured at the center of the top surface opposite the pins, as shown in the figure below.

PLASTIC QUAD FLAT PACK (PQFP)



82355 PQFP Package Thermal Characteristics

Thermal Resistance—°C/W							
Parameter	Air Flow Rate (ft/min)						
	0	50	100	200	400	600	800
θ Junction—Case	7	7	7	7	7	7	7
θ Case to Ambient	22	21	19.5	17.5	14.5	12	10

NOTES:
1. Table applies to 82355 PQFP plugged into socket or soldered directly into board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$.

Process Name:

1.2μ CHMOS III P-well

I_{CC} at Hot with no Resistive Loads:

150 mA max at 70°C
Measure PQFP case temperature
at center of top surface

14.0 BMIC REGISTER ADDRESS MAP

14.1 Index Register Set

The following registers are mapped directly into the local processor interface:

Local Address	Type	Register Description
0	R/W	Local Data Register
1	R/W	Local Index Register
2	R/W	Local Status/Control Register
3	—	Reserved

14.2 Shared Register Set

EISA Address	Type	Index Address	Type	Register Description
XC80	R	00	R/W	ID Byte 0
XC81	R	01	R/W	ID Byte 1
XC82	R	02	R/W	ID Byte 2
XC83	R	03	R/W	ID Byte 3
XC84	—	04	—	Non BMIC Register (For Expansion Board Use)
XC85	—	05	—	Non BMIC Register (For Expansion Board Use)
XC86	—	06	—	Non BMIC Register (For Expansion Board Use)
XC87	—	07	—	Non BMIC Register (For Expansion Board Use)
XC88	R	08	R/W	Global Configuration Register
XC89	R/W	09	R	System Interrupt Enable/Control Register
XC8A	R/W	0A	R/W	Semaphore Port 0
XC8B	R/W	0B	R/W	Semaphore Port 1
XC8C	R	0C	R/W	Local Doorbell Enable Register
XC8D	R/W	0D	R/W	Local Doorbell Interrupt/Status Register
XC8E	R/W	0E	R	EISA System Doorbell Enable Register
XC8F	R/W	0F	R/W	EISA System Doorbell Interrupt/Status Register
XC90	R/W	10	R/W	Mailbox Register (1)
XC91	R/W	11	R/W	Mailbox Register (2)
XC92	R/W	12	R/W	Mailbox Register (3)
XC93	R/W	13	R/W	Mailbox Register (4)
XC94	R/W	14	R/W	Mailbox Register (5)
XC95	R/W	15	R/W	Mailbox Register (6)
XC96	R/W	16	R/W	Mailbox Register (7)
XC97	R/W	17	R/W	Mailbox Register (8)
XC98	R/W	18	R/W	Mailbox Register (9)
XC99	R/W	19	R/W	Mailbox Register (10)
XC9A	R/W	1A	R/W	Mailbox Register (11)
XC9B	R/W	1B	R/W	Mailbox Register (12)
XC9C	R/W	1C	R/W	Mailbox Register (13)
XC9D	R/W	1D	R/W	Mailbox Register (14)
XC9E	R/W	1E	R/W	Mailbox Register (15)
XC9F	R/W	1F	R/W	Mailbox Register (16)
XCA0–XCAF	R/W	20–2F	—	Reserved

14.3 Processor Only Register Set

Index Address	Type	Register Description
30	R/W	Peek/Poke Data Register Byte 0
31	R/W	Peek/Poke Data Register Byte 1
32	R/W	Peek/Poke Data Register Byte 2
33	R/W	Peek/Poke Data Register Byte 3
34	R/W	Peek/Poke Address Register Byte 0
35	R/W	Peek/Poke Address Register Byte 1
36	R/W	Peek/Poke Address Register Byte 2
37	R/W	Peek/Poke Address Register Byte 3
38	R/W	Peek/Poke Control Register
39	R/W	I/O Decode Range 0 Base Address Register
3A	R/W	I/O Decode Range 0 Control Register
3B	R/W	I/O Decode Range 1 Base Address Register
3C	R/W	I/O Decode Range 1 Control Register
3D	—	Reserved
3E	—	Reserved
3F	—	Reserved
40	R/W	Channel 0 Base Count Register Byte 0
41	R/W	Channel 0 Base Count Register Byte 1
42	R/W	Channel 0 Base Count Register Byte 2
43	R/W	Channel 0 Base Address Register Byte 0
44	R/W	Channel 0 Base Address Register Byte 1
45	R/W	Channel 0 Base Address Register Byte 2
46	R/W	Channel 0 Base Address Register Byte 3
47	—	Reserved
48	R/W	Channel 0 Configuration Register
49	W	Channel 0 Transfer Strobe Register
4A	R/W	Channel 0 Status Register
4B	R/W	Channel 0 TBI Base Address Register Byte 0
4C	R/W	Channel 0 TBI Base Address Register Byte 1
4D	—	Reserved
4E	—	Reserved
4F	—	Reserved
50	R	Channel 0 Current Count Register Byte 0
51	R	Channel 0 Current Count Register Byte 1
52	R	Channel 0 Current Count Register Byte 2
53	R	Channel 0 Current Address Register Byte 0
54	R	Channel 0 Current Address Register Byte 1
55	R	Channel 0 Current Address Register Byte 2
56	R	Channel 0 Current Address Register Byte 3
57	—	Reserved
58	R	Channel 0 TBI Current Address Register Byte 0
59	R	Channel 0 TBI Current Address Register Byte 1
5A	—	Reserved
5B	—	Reserved
5C	—	Reserved
5D	—	Reserved
5E	—	Reserved
5F	—	Reserved

14.3 Processor Only Register Set (Continued)

Index Address	Type	Register Description
60	R/W	Channel 1 Base Count Register Byte 0
61	R/W	Channel 1 Base Count Register Byte 1
62	R/W	Channel 1 Base Count Register Byte 2
63	R/W	Channel 1 Base Address Register Byte 0
64	R/W	Channel 1 Base Address Register Byte 1
65	R/W	Channel 1 Base Address Register Byte 2
66	R/W	Channel 1 Base Address Register Byte 3
67	—	Reserved
68	R/W	Channel 1 Configuration Register
69	W	Channel 1 Transfer Strobe Register
6A	R/W	Channel 1 Status Register
6B	R/W	Channel 1 TBI Base Address Register Byte 0
6C	R/W	Channel 1 TBI Base Address Register Byte 1
6D	—	Reserved
6E	—	Reserved
6F	—	Reserved
70	R	Channel 1 Current Count Register Byte 0
71	R	Channel 1 Current Count Register Byte 1
72	R	Channel 1 Current Count Register Byte 2
73	R	Channel 1 Current Address Register Byte 0
74	R	Channel 1 Current Address Register Byte 1
75	R	Channel 1 Current Address Register Byte 2
76	R	Channel 1 Current Address Register Byte 3
77	—	Reserved
78	R	Channel 1 TBI Current Address Register Byte 0
79	R	Channel 1 TBI Current Address Register Byte 1
7A	—	Reserved
7B	—	Reserved
7C	—	Reserved
7D	—	Reserved
7E	—	Reserved
7F	—	Reserved

NOTES:
1. TBI = Transfer Buffer Interface
2. X = Slot number
3. All the reserved locations, when read, will return a value of no practical use to the user.
4. The "non BMIC" register locations (XC84h–XC87h & 04h–07h) are locations to be used by registers implemented externally on the expansion board. The BMIC will not respond to these locations (XC84h–CC87h) when accessed from the EISA side. However, the BMIC can be programmed to support the decode of the EISA addresses (XC84h–XC87h) through its I/O decode register set (refer to Section 4.8). All "non BMIC" register locations (04h–07h) when read from the local side, will return a value of no practical use to the user.

82355 Revision Summary

The following changes have been made since revision 006:

Section 1.1 EISA READ definitions has been changed from "A data transfer (burst, non-burst (two BCLK), or mismatched) from system to the expansion board across one of the two transfer channels" to "A data transfer (burst, non-burst (two BCLK), or mismatched) from system to the expansion board across Channel 1 transfer channel 1."

Section 4.2 New paragraph added after the first paragraph:

Channel 0 can be used for EISA READ operation only. Channel 1 can be used for both EISA READ and EISA WRITE operations.

Section 8.1.2 Bits 7–4 has been changed to Third hex digit of product number

Bits 4–0 has been changed to Hexadecimal digit of product revision

Section 8.2.3.3 Sentence added to Bit 22:

This is applicable only to channel 1 and not for channel 0, as channel 0 can perform EISA WRITE transfers only.

Section 10.0 Figure 10-1 TDIR, TCHAN timing diagram has changed from 10 to 11.

Figure 10-3 TDIR, TCHAN timing diagram has changed from 10 to 11.

Figure 10-7 TDIR, TCHAN timing diagram has changed from 10 to 11.

The following changes have been made since revision 005:

Section 4.3 New paragraph added at the end. This paragraph reads:

Any consecutive Peek/Poke or Locked exchanged transfers must be initiated only after the previous Peek/Poke or Locked exchange has been completed. This can be accomplished by making sure that bit 2 of the local status/control register is set to a zero before initiating the transfer.

Section 4.8 New paragraph added after the third paragraph. This paragraph reads:

The IDOEs do not go active during an IOSEL cycle outside the shared register access space.

Section 7.4 The third paragraph had two sentences deleted that is replaced with Figure 7-2, IDOEO# Connection during ID Register Access. The sentences that were deleted read as follows:

The external lines connected to the IDAT <7:0> lines should be connected to the bus between the BMIC and the external F245 data buffers. The BMIC will enable the external data buffers to drive byte lane 0 of the EISA bus upon detection of the ID address.

The following changes have been made since revision 004:

Section 4.3 New paragraph added at the end. This paragraph reads:

Whenever the BMIC is commanded to do an EISA POKE cycle, the BMIC will assert the MREQ# signal low normally, transfer up to four bytes of data, and release the bus by de-asserting MREQ# high. A potential problem exists, however, when the slave device extends the cycle by de-asserting EXRDY low. If the slave holds this signal low past the time that the BMIC is forced to release MREQ# high (it has been preempted while waiting for the slave to assert EXRDY high), then the BMIC will drive MREQ# back low again immediately after this cycle ends if there is another transfer pending (TBI, PEEK, POKE or LOCKED-EXCHANGE). Note that according to the EISA spec, "A bus master must wait at least two BCLKs after releasing the bus before re-asserting its MREQx*"(EISA spec, MREQ* signal description). To adhere to EISA specifications, it is required that LOCKED-EXCHANGE cycles be used in lieu of POKE cycles.

Section 8.2.3.4 New sentence added at the end of paragraph one:

At the end of a transfer, this register contains the value of the number of bytes transferred during the last cycle.

Section 8.2.4.2 Two paragraphs added for the CFGCL bit:

Before a channel is issued a clear command, the channel must first be suspended by writing a "1" into Bit 0 (CFGSU) of the Transfer Channel Configuration Register. Next the Transfer Channel Status Register must be read. If the TSTTC (Bit 0) is set to a "1", then the channel has already completed the transfer. The channel is then unsuspended (write a "0" into Bit 0 [CFGSU] of the Transfer Channel Configuration Register), and the TSTTC bit is then cleared.

If the TSTTC bit is a "0", then the TSTEN bit is checked. If this bit is a "1", then the channel has not returned to idle yet, and the Transfer Channel Status Register is repolled. If the TSTEN bit is a "0", then the channel has successfully returned to idle and can now be cleared with no errors. This is done by setting Bit 2 (CFGCL bit) to a 1 in the Transfer Channel Configuration Register. A flowchart for this operation is shown in the following figure.

Figure 8-1 was added to the data sheet.

Section 8.2.4.3 Bit 4 has been changed to reserved.

First paragraph under bit description has been changed to read, "Bits (7), (6), TST1K, and (4) are reserved. Any data read from these bits should be ignored".

The paragraph following this one has been deleted.

Section 11.2 Max Limits on symbols C_{OUT} and C_{CLK} have been changed.

Note 1 has been corrected.

Section 12.1 Symbol t1 has been corrected to read 2500 instead of 250 for max.

Symbol t20 has been corrected to read 3 for min.

Symbol t22 has been corrected to 4 from 7 for min.

Symbol t35 has been corrected to 5 from 7 for min.

Symbol t37 has been corrected to 3 for min.

Symbol t40 has been corrected to 1 for min.

Symbol t50 has been corrected to 124 from 125 for max.

Symbol t51 has been corrected to 1 for min.

Section 12.2 The Local CPU Interface Timing (Read Cycle/Shared Register Access) table has been corrected. The signal LDAT<7:0> has changed one portion from valid to float.

intel®

2

PC I/O Peripherals

82091AA
ADVANCED INTEGRATED PERIPHERAL (AIP)

- **Single-Chip PC Compatible I/O Solution for Notebook and Desktop Platforms:**
  - 82078 Floppy Disk Controller Core
  - Two 16550 Compatible UARTs
  - One Multi-Function Parallel Port
  - IDE Interface
  - Integrated Back Power Protection
  - Integrated Game Port Chip Select
  - 5V or 3.3V Supply Operation with 5V Tolerant Drive Interface
  - Full Power Management Support
  - Supports Type F DMA Transfers for Faster I/O Performance
  - No Wait-State Host I/O Interface
  - Programmable Interrupt Interfaces
  - Single Crystal/Oscillator Clock (24 MHz)
  - Software Detectable Device ID
  - Comprehensive Powerup Configuration
- **The 82091AA is 100 Percent Compatible with EISA, ISA and AT**
- **Host Interface Features**
  - 8-Bit Zero Wait-State ISA Bus Interface
  - DMA with Type F Transfers
  - Five Programmable ISA Interrupt Lines
  - Internal Address Decoder
- **Parallel Port Features**
  - All IEEE Standard 1284 Protocols Supported (Compatibility, Nibble, Byte, EPP, and ECP)
  - Peak Bi-Directional Transfer Rate of 2 MB/sec
  - Provides Interface for Low-Cost Engineless Laser Printer
  - 16-Byte FIFO for ECP
  - Interface Backpower Protection
- **Floppy Disk Controller Features**
  - 100 Percent Software Compatible with Industry Standard 82077SL and 82078
  - Integrated Analog Data Separator 250K, 300K, 500K, and 1 MBits/sec
  - Programmable Powerdown Command
  - Auto Powerdown and Wakeup Modes
  - Integrated Tape Drive Support
  - Perpendicular Recording Support for 4 MB Drives
  - Programmable Write Pre-Compensation Delays
  - 256 Track Direct Address, Unlimited Track Support
  - 16-Byte FIFO
  - Supports 2 or 4 Drives
- **16550 Compatible UART Features**
  - Two Independent Serial Ports
  - Software Compatible with 8250 and 16450 UARTs
  - 16-Byte FIFO per Serial Port
  - Two UART Clock Sources, Supports MIDI Baud Rate
- **IDE Interface Features**
  - Generates Chip Selects for IDE Drives
  - Integrated Buffer Control Logic
  - Dual IDE Interface Support
- **Power Management Features**
  - Transparent to Operating Systems and Applications Programs
  - Independent Power Control for Each Integrated Device
- **100-Pin QFP Package**
  (See Packaging Spec. 240800)

2

The 82091AA Advanced Integrated Peripheral (AIP) is an integrated I/O solution containing a floppy disk controller, 2 serial ports, a multi-function parallel port, an IDE interface, and a game port on a single chip. The integration of these I/O devices results in a minimization of form factor, cost and power consumption. The

floppy disk controller is the 82078 core. The serial ports are 16550 compatible. The parallel port supports all of the IEEE Standard 1284 protocols (ECP, EPP, Byte, Compatibility, and Nibble). The IDE interface supports 8- or 16-bit programmed I/O and 16-bit DMA. The Host Interface is an 8-bit ISA interface optimized for type "F" DMA and no wait-state I/O accesses. Improved throughput and performance, the 82091AA contains six 16-byte FIFOs–two for each serial port, one for the parallel port, and one for the floppy disk controller. The 82091AA also includes power management and 3.3V capability for power sensitive applications such as notebooks. The 82091AA supports both motherboard and add-in card configurations.

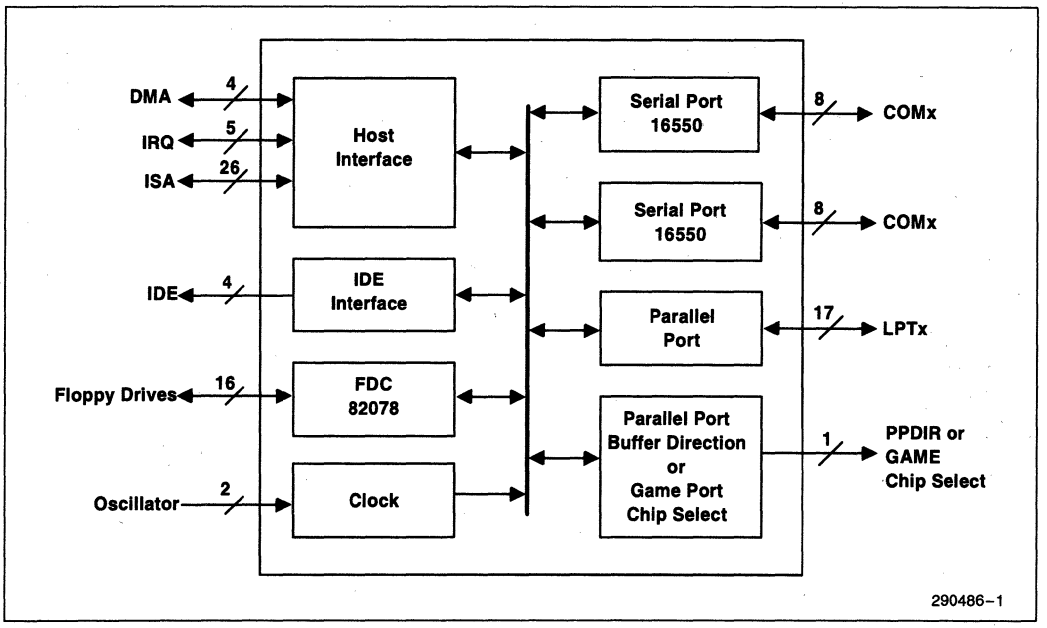


Figure 1. 82091AA Advanced Integrated Peripheral Block Diagram

82091AA
ADVANCED INTEGRATED PERIPHERAL (AIP)

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1.0. OVERVIEW

The major functions of the 82091AA are shown in Figure 1. A brief description of each of these functions is presented in this section.

Host Interface

The 82091AA host interface is an 8-bit direct-drive (24 mA) ISA Bus/X-Bus interface that permits the CPU to access its registers through read/write operations in I/O space. These registers may be accessed by programmed I/O and/or DMA bus cycles. With the exception of the IDE Interface, all functions on the 82091AA require only 8-bit data accesses. The 16-bit access required for the IDE Interface is supported through the appropriate chip selects and data buffer enables from the 82091AA.

Figure 2 shows an example system implementation with the 82091AA located on an ISA Bus add-in card. This add-in card could also be used in a PCI-based system as shown in Figure 3. For motherboard implementations, the 82091AA can be located on the X-Bus as shown in Figure 4.

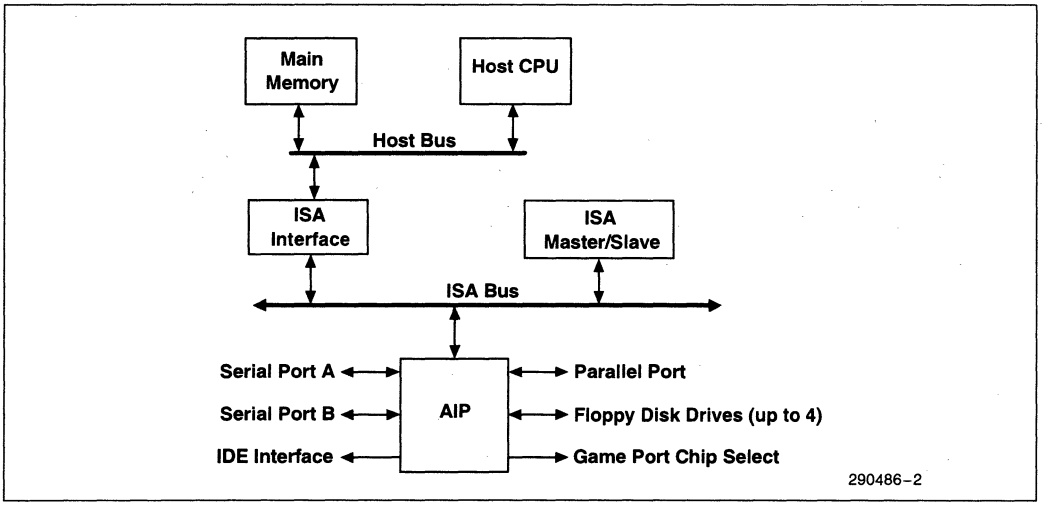


Figure 2. Block Diagram of the 82091AA on the ISA Bus

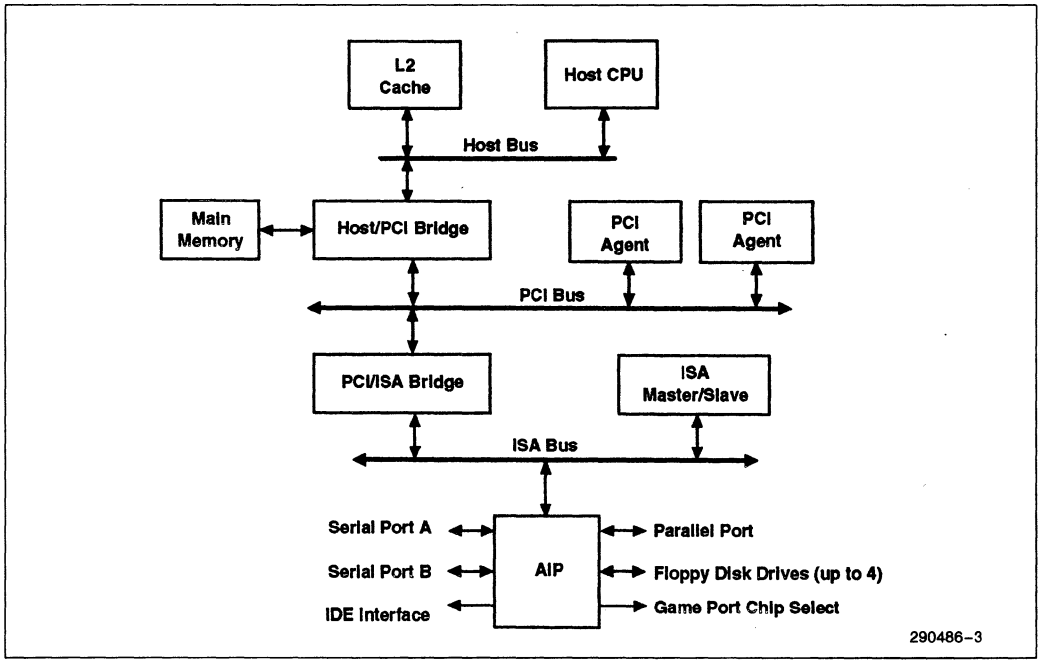


Figure 3. Block Diagram of the 82091AA in a PCI System

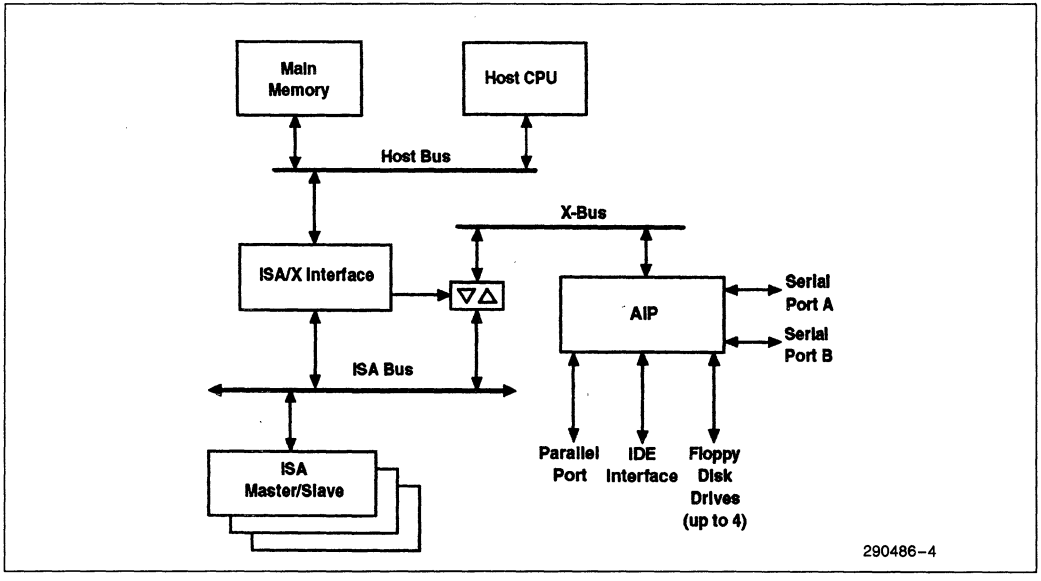


Figure 4. Block Diagram of the 82091AA on the X-Bus

Floppy Disk Controller

The 82091AA's enhanced floppy disk controller (FDC) incorporates several new features allowing for easy implementation in both the portable and desktop markets. It provides a low cost, small form factor solution targeted for 5.0V and 3.3V platforms. The FDC supports up to four drives.

The 82091AA's FDC implements these new features while remaining functionally compatible with 82078/82077SL/82077AA/8272A floppy disk controllers. Together, with a 24-MHz crystal, a resistor package and a device chip select, these devices allow for the most integrated solution available. The integrated analog PLL data separator has better performance than most board level discrete PLL implementations and can be operated at 1 Mbps/500 Kbps/300 Kbps/250 Kbps. A 16-byte FIFO substantially improves system performance and is ideal for multimaster systems (e.g., EISA).

Serial Ports

The 82091AA contains two independent serial ports that provide asynchronous communications that are equivalent to two 16550 UARTs. The serial ports have identical circuitry and provide the serial communication interface to a peripheral device or modem via Serial Port A and Serial Port B. Each serial port can be configured for one of eight address assignments. The standard PC/AT compatible logical address assignments for COM1, COM2, COM3, and COM4 are supported.

The serial ports perform serial-to-parallel conversion on data characters received from a peripheral device or modem, and parallel-to-serial conversion on data characters received from the host. The serial ports can operate in either FIFO mode or non-FIFO mode. In FIFO mode, a 16-byte transmit FIFO holds data from the host to be transmitted on the serial link and a 16-byte receive FIFO that buffers data from the serial link until read by the host.

The serial ports contain programmable baud rate generators that divide the internal reference clock by divisors of 1 to ($2^{16} - 1$), and produce a 16x clock for driving the transmitter and receiver logic. The internal reference clock can be programmed to support MIDI. The serial ports have complete modem-control capability and a prioritized interrupt system.

Parallel Port

The 82091AA provides a multi-function parallel port that transfers information between the host and peripheral device (e.g., printer). The parallel port interface contains nine control/status lines and an 8-bit data bus. The standard PC/AT compatible logical address assignments for LPT1, LPT2, and LPT3 are supported. The parallel port can be configured for one of four modes and supports the following IEEE Standard 1284 parallel interface protocol standards:

Parallel Port Mode	Parallel Interface Protocol
ISA-Compatible Mode	Compatibility, Nibble
PS/2-Compatible Mode	Byte
EPP Mode	EPP
ECP Mode	ECP

For ISA-Compatible and PS/2-Compatible modes, software controls the handshake signals on the parallel port interface to transfer data between the host and peripheral device. Status and Control registers permit software to monitor the state of the peripheral device and generate handshake sequences.

The EPP parallel port interface protocol increases throughput by specifying an automatic handshake sequence. In EPP mode, the 82091AA parallel port automatically generates this handshake sequence in hardware to transfer data between the host and peripheral device.

In addition to a hardware handshake on the parallel port interface, the ECP protocol specification also defines DMA and FIFO capability. To minimize processor overhead data transfer to/from a peripheral device, the 82091AA parallel port, in ECP mode, provides a 16-byte FIFO with DMA capability.

IDE Interface

The 82091AA supports the IDE (Integrated Drive Electronics) interface by providing chip selects and lower data byte control. Two chip selects are used to access registers on the IDE device. Separate lower and upper byte data control signals are provided. With these control signals, minimal external logic is needed to implement 16-bit IDE I/O and DMA interfaces.

Game Port

The 82091AA provides a game port chip select signal for use when the 82091AA is in an add-in card application. This function is assigned to I/O address location 201h. Note that when the 82091AA is located on the motherboard, this feature is not available.

Power Management

82091AA power management provides a mechanism for saving power when the device or a portion of the device is not being used. By programming the appropriate 82091AA registers, software can invoke power management to the entire 82091AA or selected modules within the 82091AA (e.g., floppy disk controller, serial port, or parallel port). There are two methods for applying power management—direct powerdown or auto powerdown. Direct powerdown turns off the clock to a particular module immediately placing that module into a powerdown state. This method removes the clock regardless of the activity or status of the module. When auto powerdown is invoked, the module enters a powerdown state (clock is turned off) after certain conditions are met and the module is in an idle state.

1.1. 3.3V/5V Operating Modes

The 82091AA can operate at a power supply of 3.3V, 5V or a mix of 3.3V and 5V. The mixed power supply mode provides 5V interfaces for the floppy disk controller and parallel port while all other 82091AA interfaces and internal logic (including the floppy disk controller and parallel port internal circuitry) operate at 3.3V. The mixed mode permits 5V floppy disk drives and parallel port peripherals to be used in a 3.3V system without external buffering.

NOTE:
3.3V operation is available only in the 82091AA.

2.0. SIGNAL DESCRIPTION

This section describes the 82091AA signals. The interface signals are shown in Figure 5 and described in the following tables. Signal descriptions are organized by functional group.

Note that the "#" symbol at the end of a signal name indicates the active, or asserted, state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used extensively. This is done to avoid confusion when working with a mixture of "active-low" and "active-high" signals. The term **assert**, or **assertion**, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term **negate**, or **negation**, indicates that a signal is inactive.

The following notations are used to describe pin types:

I Input Pin

O Output Pin

I/O Bi-Directional Pin

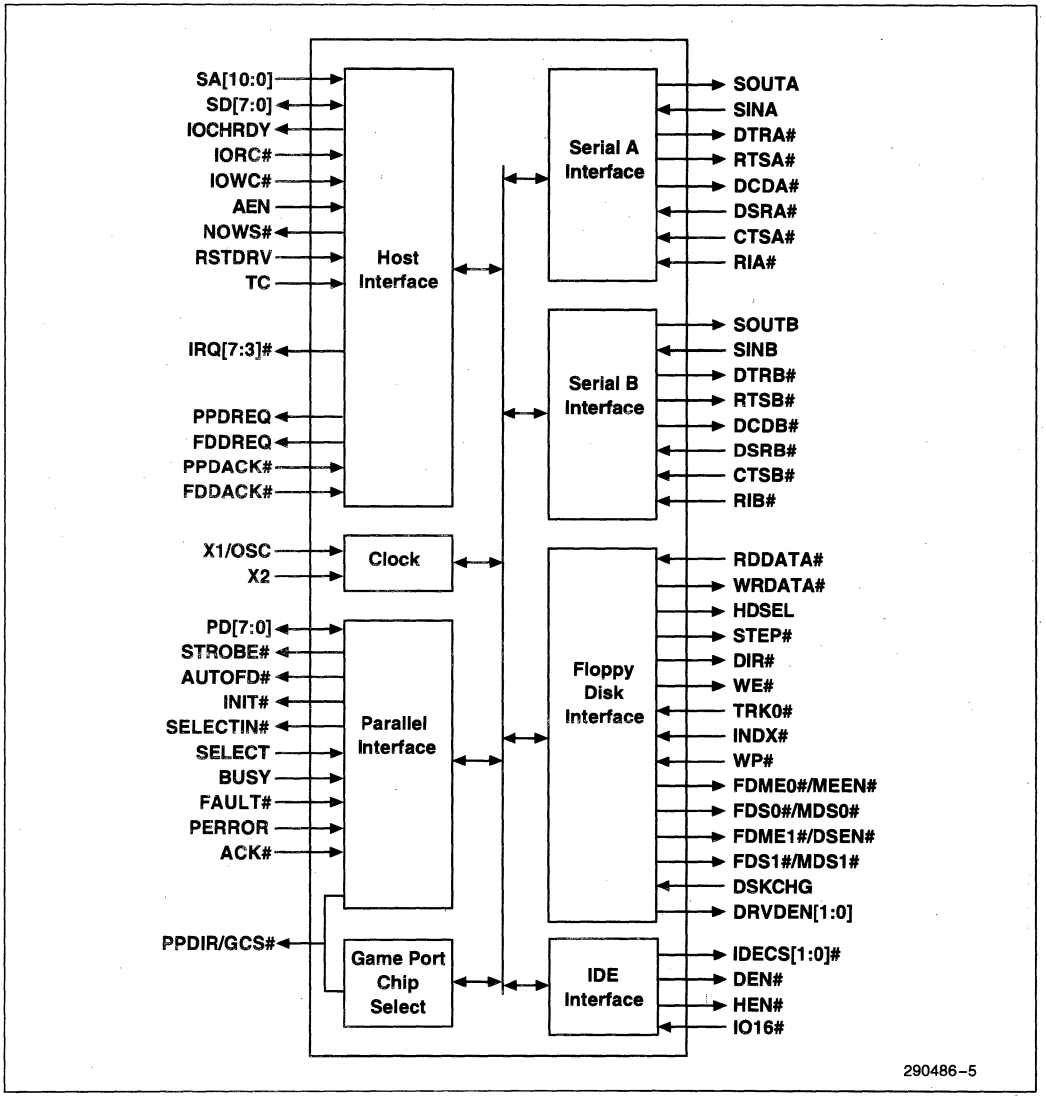


Figure 5. 82091AA Signals

2.1 Host Interface Signals

Signal Name	Type	Description
ISA SIGNALS		
SA[10:0]	I	**SYSTEM ADDRESS BUS:** The 82091AA decodes the standard ISA I/O address space using SA[9:0]. SA10 is used along with SA[9:0] to decode the extended register set of the ECP parallel port. SA[10:0] connects directly to the ISA system address bus.
SD[7:0]	I/O	**SYSTEM DATA BUS:** SD[7:0] is a bi-directional data bus. Data is written to and read from the 82091AA on these signal lines. SD[7:0] connect directly to the ISA system data bus.
IORC#	I	**I/O READ COMMAND STROBE:** IORC# is an I/O access read control signal. When a valid internal address is decoded by the 82091AA and IORC# is asserted, data at the decoded address location is driven onto the SD[7:0] signal lines.
IOWC#	I	**I/O WRITE COMMAND STROBE:** IOWC# is an I/O access write control signal. When a valid internal address is decoded by the 82091AA and IOWC# is asserted, data on the SD[7:0] signal lines is written into the decoded address location at the rising edge of IOWC#.
NOWS#	O	**NO WAIT-STATES:** End data transfer signal. The 82091AA asserts NOWS# when a valid internal address is decoded by the 82091AA and the IORC# or IOWC# signal is asserted. This reduces the total bus cycle time by eliminating the wait-states associated with the default 8-bit I/O cycles. NOWS# is not asserted for IDE accesses or DMA accesses. This is an open drain output pin.
IOCHRDY	O	**I/O CHANNEL READY:** The 82091AA uses this signal for parallel port data transfers when the parallel port is in EPP mode. In this case, the 82091AA negates IOCHRDY to extend the cycle to allow for completion of transfers to/from the peripheral attached to the parallel port. When the parallel port is in EPP mode, the 82091AA negates IOCHRDY to lengthen the ISA Bus cycle if the parallel port BUSY signal is asserted. The 82091AA also uses IOCHRDY during hardware configuration time (see Section 4.0, AIP Configuration). If IOWC#/IORC# is asserted to the 82091AA during hardware configuration time, the 82091AA negates IOCHRDY until hardware configuration time is completed. This is an open drain output pin.
AEN	I	**ADDRESS ENABLE:** AEN is used during DMA cycles to prevent the 82091AA from misinterpreting DMA cycles from valid I/O cycles. When negated, AEN indicates that the 82091AA may respond to address and I/O commands addressed to the 82091AA. When asserted, AEN informs the 82091AA that a DMA transfer is occurring. When AEN is asserted and a xDACK# signal is asserted, the 82091AA responds to the cycle as a DMA cycle.
RSTDRV	I	**RESET DRIVE:** RSTDRV forces the 82091AA to a known state. All 82091AA registers are set to their default state.
X1/OSC	I	**CRYSTAL1/OSCILLATOR:** Main clock input signal can be a 24 MHz crystal connected across X1 and X2 or a 24 MHz TTL level clock input connected to X1.
X2	I	**CRYSTAL2:** This signal pin is connected to one side of the crystal when a crystal oscillator is used to provide the main clock. If an external oscillator/clock is connected to X1, this pin is not used and left unconnected.

2.1 Host Interface Signals (Continued)

Signal Name	Type	Description
DMA SIGNALS		
FDDREQ	O	**FLOPPY DISK CONTROLLER DMA REQUEST:** The 82091AA asserts FDDREQ to request service from a DMA controller for the FDC module. This signal is enabled/disabled by bit 3 of the Digital Output Register (DOR). When disabled, FDDREQ is tri-stated.
FDDACK#	I	**FLOPPY DISK CONTROLLER DMA ACKNOWLEDGE:** The DMA controller asserts this signal to acknowledge the FDC DMA request. When asserted, the IORC# and IOWC# inputs are enabled during DMA transfers. This signal is enabled/disabled by bit 3 of the DOR.
PPDREQ	O	**PARALLEL PORT DMA REQUEST:** Parallel port DMA service request to the system DMA controller. This signal is only used when the parallel port is in ECP hardware mode and is always negated when the parallel port is not in this mode. In ECP hardware mode DMA requests are enabled/disabled by bit 3 of the ECP Extended Control Register (ECR). When disabled, PPDREQ is tri-stated.
PPDACK#	I	**PARALLEL PORT DMA ACKNOWLEDGE:** The DMA controller asserts this signal to acknowledge the parallel port DMA request. When asserted the IORC# and IOWC# inputs are enabled during DMA transfers. This signal is enabled/disabled by bit 3 of the ECR Register.
TC	I	**TERMINAL COUNT:** The system DMA controller asserts TC to indicate it has reached the last programmed data transfer. TC is accepted only when FDDACK# or PPDACK# is asserted.
INTERRUPT SIGNALS		
IRQ3, IRQ4	O	**INTERRUPT 3 AND 4:** IRQ3 and IRQ4 are associated with the serial ports and can be programmed (via the AIPCFG2 Register) to be either active high or active low. These signals can be configured for a particular serial channel via hardware configuration (at powerup) or by software configuration. **Under Hardware Configuration** IRQ3 is used as a serial port interrupt if the serial port is configured at address locations 2F8h–2FFh or 2E8h–2EFh. IRQ4 is used as a serial port interrupt if the serial port is configured at address locations 3F8h–3FFh or 3E8h–3EFh. **Under Software configuration** IRQ3 and IRQ4 are independently configured (i.e., the IRQ does not automatically track the communication port address assignment). These interrupts are enabled/disabled globally via bit 3 of the serial port Modem Control Register (MCR) and for specific conditions via the Interrupt Enable Register (IER). IRQ3 and IRQ4 are tri-stated when not enabled.
IRQ5, IRQ7	O	**INTERRUPT REQUEST 5:** IRQ5 and IRQ7 are associated with the parallel port and can be programmed (via AIPCFG2 Register) to be either active high or active low. Either IRQ5 or IRQ7 is enabled/disabled via PCFG1 Register to signal a parallel port interrupt. The interrupt not selected is disabled and tri-stated. During hardware configuration (see Section 4.0, AIP Configuration), IRQ5 is used if the parallel port is assigned to 278h–27Fh and IRQ7 is used if the parallel port interrupt is assigned to either 3BCh–3BFh or 378h–37Fh.

2.1 Host Interface Signals (Continued)

Signal Name	Type	Description
INTERRUPT SIGNALS (Continued)		
IRQ6	O	**INTERRUPT REQUEST 6:** IRQ6 is associated with the floppy disk controller and can be programmed (via the AIPCFG2 Register) to be either active high or active low. In non-DMA mode this signal is asserted to signal when a data transfer is ready. IRQ6 is also asserted to signal the completion of the execution phase for certain FDC commands. This signal is enabled/disabled by the DMAGATE bit in the Digital Output Register of the FDC. The signal is tri-stated when disabled.

2.2 Floppy Disk Controller Interface

Signal Name	Type	Description
RDDATA#	I	**READ DATA:** Serial data from the disk drive.
WRDATA#	O	**WRITE DATA:** MFM serial data to the disk drive. Precompensation value is selectable through software.
HDSEL	O	**HEAD SELECT:** Selects which side of a disk is to be accessed. When asserted (low), side 1 is selected. When negated (high), side 0 is selected.
STEP#	O	**STEP:** STEP# supplies step pulses (asserted) to the drive to move the head between the tracks during a seek operation.
DIR#	O	**DIRECTION:** Controls the direction the head moves when a step signal is present. The head moves toward the center when DIR# is asserted and away from the center when negated.
WE#	O	**WRITE ENABLE:** WE# is a disk drive control signal. When asserted, WE# enables the head to write to the disk.
TRK0#	I	**TRACK0:** The disk drive asserts this signal to indicate that the head is on track 0.
INDX#	I	**INDEX:** The disk drive asserts this signal to indicate the beginning of the track.
WP#	I	**WRITE PROTECT:** The disk drive asserts this signal to indicate that the disk drive is write-protected.
DSKCHG	I	**DISK CHANGE:** The disk drive asserts this signal to indicate that the drive door has been opened. The state of this signal input is available in the Digital Input Register (DIR#).
DRIVDEN0 DRIVDEN1	O	**DRIVE DENSITY:** These signals are used by the disk drive to configure the drive for the appropriate media density. These signals are controlled by the FDC's Drive Specification Command.

2.2 Floppy Disk Controller Interface (Continued)

Signal Name	Type	Description
FDME1#/ DSEN#(1)	O	**FLOPPY DRIVE MOTOR ENABLE 1, IDLE, OR DRIVE SELECT ENABLE:** This signal pin has two functions(1). FDME1# is the motor enable for drive 1. FDME1# is directly controlled via the Digital Output Register (DOR) and is a function of the mapping based on the BOOTSEL bits in the Tape Drive Register (TDR). The Drive Select Enable (DSEN#) function is only used in a four floppy drive system (see Appendix A, FDC Four Drive Support).
FDS1#/ MDS1(1)	O	**FLOPPY DRIVE SELECT1, POWERDOWN, OR MOTOR DRIVE SELECT 1:** This signal pin has two functions(1). FDS1# is the floppy drive select for drive 1. FDS1# is controlled by the select bits in the DOR and is a function of the mapping based on the BOOTSEL bits in the TDR. The Motor Drive Select 1 (MDS1) function is only used in a four floppy drive system (see Appendix A, FDC Four Drive Support).
FDME0#/ MEEN#(1)	O	**FLOPPY DRIVE MOTOR ENABLE 0 OR MOTOR ENABLE ENABLE:** This signal pin has two functions(1). FDME0# is the motor enable for drive 0. FDME0# is directly controlled via the Digital Output Register (DOR) and is a function of the mapping based on the BOOTSEL bits in the Tape Drive Register (TDR). The Motor Enable Enable (MEEN#) function is only used in a four floppy drive system (see Appendix A, FDC Four Drive Support).
FDS0#/ MDS0(1)	O	**FLOPPY DRIVE SELECT 0 OR MOTOR DRIVE SELECT 0:** This signal pin has two functions(1). FDS0# is the floppy drive select for drive 0. This output is controlled by the drive select bits in the DOR and is a function of the mapping based on BOOTSEL bits in the TDR. The Motor Drive Select 0 (MDS0) function is only used in a four floppy drive system (see Appendix A, FDC Four Drive Support).

NOTE:
1. The function selected for these pins is based on the FDDQTY bit in the FCFG1 Register as shown in the following table.

Signal Pin	2 Drive System (FDDQTY = 0)	4 Drive System (FDDQTY = 1)
FDME1#/DSEN#	FDME1#	DSEN#
FDS1#/MDS1#	FDS1#	MDS1
FDME0#/MEEN#	FDME0#	MEEN#
FDS0#/MDS0	FDS0#	MDS0

When FDDQTY = 1, these signal pins are used to control an external decoder for a four floppy disk drive system as described in Appendix A, FDC Four Drive Support.

2.3 Serial Port Interface

Serial Port A signal names end in the letter A and Serial Port B signal names end in the letter B. Serial Port A and B signals have the same functionality.

Signal Name	Type	Description
CTSA#, CTSB#	I	**CLEAR TO SEND:** When asserted, this signal indicates that the modem or data set is ready to exchange data. The CTS# signal is a modem status input whose condition the CPU can determine by reading the CTS bit in Modem Status Register (MSR) for the appropriate serial port. The CTS bit is the compliment of the CTS# signal. The DCTS bit in the MSR indicates whether the CTS# input has changed state since the previous reading of the MSR. CTS# has no effect on the transmitter.
DCDA#, DCDB#	I	**DATA CARRIER DETECT:** When asserted, this signal indicates that the data carrier has been detected by the modem or data set. The DCD# signal is a modem status whose condition the CPU can determine by reading the DCD bit in the MSR for the appropriate serial port. The DCD bit is the compliment of the DCD# signal. The DDCD bit in the MSR indicates whether the DCD# input has changed state since the previous reading of the MSR. DCD# has no effect on the transmitter.
DSRA#, DSRB#	I	**DATA SET READY:** When asserted, this signal indicates that the modem or data set is ready to establish the communications link with the serial port module. The DSR# signal is a modem status whose condition the CPU can determine by reading the DSR bit in the MSR for the appropriate serial channel. The DSR bit is the compliment of the DSR# signal. The DSR bit in the MSR indicates whether the DSR# input has changed state since the previous reading of the MSR. DSR# has no effect on the transmitter.
DTRA#, DTRB#	I/O	**DATA TERMINAL READY:** DTRA#/DTRB# are outputs during normal system operations. When asserted, this signal indicates to the modem or data set that the serial port module is ready to establish a communications link. The DTR# signal can be asserted via the Modem Control Register (MCR). A hard reset negates this signal. **Hardware Configuration** These signals are only inputs during hardware configuration time (RSTDRV asserted and for a short time after RSTDRV is negated). (See Section 4.0, AIP Configuration.)
RIA#, RIB#	I	**RING INDICATOR:** When asserted, this signal indicates that a telephone ringing signal has been received by the modem or data set. The RI# signal is a modem status input whose condition the CPU can determine by reading the RI bit in the MSR for the appropriate serial channel. The RI bit is the compliment of the RI# signal. The TERI bit in the MSR indicates whether the RI# input has changed from low to high since the previous reading of the MSR.

2.3 Serial Port Interface (Continued)

Signal Name	Type	Description
RTSA#, RTSB#	I/O	**REQUEST TO SEND:** RTSA#/RTSB# are outputs during normal system operations. When asserted, this signal informs the modem or data set that the serial port module is ready to exchange data. The RTS# signal can be asserted via the RTS bit in the Modem Control Register. A hard reset negates this signal. **Hardware Configuration** These signals are only inputs during hardware configuration time (RSTDRV asserted and for a short time after RSTDRV is negated). (See Section 4.0, AIP Configuration.)
SINA, SINB	I	**SERIAL INPUT:** Serial data input from the communications link. (Peripheral device, modem, or data set.)
SOUTA, SOUTB	I/O	**SERIAL OUTPUT:** SOUTA/SOUTB are serial data outputs to the communications link during normal system operations. (Peripheral device, modem, or data set.) The SOUT signal is set to a marking state (logic 1) after a hard reset. **Test Mode** In test mode (selected via the SACFG2 or SBCFG2 Registers), the baudout from the baud rate generator is output on SOUTx. **Hardware Configuration** These signals are only inputs during hardware configuration time (RSTDRV asserted and for a short time after RSTDRV is negated). (See Section 4.0, AIP Configuration.)

2.4 IDE Interface

Signal Name	Type	Description
IO16#	I	**16-BIT I/O:** This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles. The IDE interface asserts this signal to the 82091AA to indicate support for 16-bit transfers. For IDE transfers, the 82091AA asserts HEN# when IO16# is asserted.
IDECS[1:0]#	I/O	**IDE CHIP SELECT:** IDECS[1:0]# are outputs during normal system operation and are chip selects for the IDE interface. IDECS[1:0]# select the Command Block Registers of the IDE device and are decoded from SA[9:3] and AEN. **Hardware Configuration** These signals are only inputs during hardware configuration time (RSTDRV asserted). (See Section 4.0, AIP Configuration.)

2.4 IDE Interface (Continued)

Signal Name	Type	Description
DEN#	I/O	**DATA ENABLE:** DEN# is an output during normal system operations and is a data enable for an external data buffer for all 82091AA and IDE accesses. The SD[7:0] signals can be connected directly to the ISA. In this case, the DEN# signal is not used. However, an external buffer can be used to isolate the SD[7:0] signals from the 240 pF loading of the ISA Bus. With an external buffer implementation, DEN# controls the external buffers for transfers to/from the ISA Bus. **Hardware Configuration** This signal is only an input during hardware configuration time (RSTDRV asserted). (See Section 4.0, AIP Configuration.)
HEN#	I/O	**IDE UPPER DATA TRANSCEIVER ENABLE:** HEN# is an output during normal system operations and is a high byte data transceiver enable signal for the IDE hard disk drive interface. HEN# is asserted for I/O accesses to the IDE data register when the drive asserts IO16#. **Hardware Configuration** This signal is only an input during hardware configuration time (RSTDRV asserted). (See Section 4.0, AIP Configuration.)

2.5 Parallel Port External Buffer Control/Game Port

Signal Name	Type	Description
PPDIR/GCS#	I/O	**PARALLEL PORT DIRECTION (PPDIR) or GAME PORT CHIP SELECT (GCS#):** This signal is an output during normal operations and provides the PPDIR and GCS# functions as follows: **PPDIR** This signal pin functions as a parallel port direction control output when the 82091AA is configured for software motherboard mode (SWMB). For configuration details, see Section 4.0, AIP Configuration. If external buffers are used on PD[7:0], PPDIR can be used to control the buffer direction. The 82091AA drives this signal low when PD[7:0] are outputs and the 82091AA drives this signal high when PD[7:0] are inputs. Note that if a configuration mode other than SWMB is selected, this signal pin is a game port chip select and does not track the PD[7:0] signal direction. **GCS#** This signal pin functions as a game port chip select output when 82091AA configuration is set for Software Add-In (SWAI), Hardware Basic (HWB), or Hardware Extended (HWE) modes. When the host accesses I/O address 201h, GCS# is asserted. **Hardware Configuration** This signal is only an input during hardware configuration time (RSTDRV asserted). (See Section 4.0, AIP Configuration.)

2.6 Parallel Port Interface

The 82091AA parallel port is a multi-function interface that can be configured for one of four hardware modes (see Section 4.0, AIP Configuration). The hardware modes are ISA-Compatible, PS/2-Compatible, EPP, and ECP modes. These parallel port modes support the compatibility, nibble, byte, EPP and ECP parallel interface protocols described in the IEEE 1284 standard. The operation and use of the interface signal pins are a function of the parallel port hardware mode selected and the protocol used.

Table 1 shows a matrix of the 82091AA parallel port signal names and corresponding signal names for each of the protocols. Sections 2.6.1–2.6.5 provide a signal description for the five interface protocols. Note that the 82091AA hardware operations are the same for Compatibility and Nibble protocols. The signals, however, are controlled and used differently via software and the peripheral device.

Table 1. Parallel Port Signal Name Cross Reference

82091AA Signal Names	Compatibility Protocol Signal Names	Nibble Protocol Signal Names	Byte Protocol Signal Names	EPP Protocol Signal Names	ECP Protocol Signal Names
STROBE#	Strobe#	—	HostCLK	Write#	HostClk
BUSY	Busy	PtrBusy	PtrBusy	Wait#	PeriphAck
ACK#	Ack#	PtrClk	PtrClk	Intr	PeriphClk#
SELECT	Select	Xflag	Xflag	Xflag	Xflag
PERROR	PError	AckDataReq	AckDataReq	AckDataReq	AckReverse#
FAULT#	Fault#	DataAvail#	DataAvail#	DataAvail#	PeriphRequest#
INIT#	Init#	—	—	Init#	ReverseRequest#
AUTOFD#	AutoFd#	HostBusy	HostBusy	DStrb#	HostAck
PD[7:0]	Data[8:1]	—	Data[8:1]	Data[8:1]	Data[8:1]
SELECTIN#	SelectIn#	—	—	AStrb#	ECP Mode

NOTE:
Not all parallel port signal pins are used for certain parallel port interface protocols. These signals are labeled "—".

2.6.1 COMPATIBILITY PROTOCOL SIGNAL DESCRIPTION

Except for the data bus, the 82091AA and compatibility protocol signal names are the same. For the data bus, the 82091AA signal names PD[7:0] corresponds to the compatibility protocol signal names Data[8:1].

82091AA Signal Name	Type	Compatibility Protocol Signal Name and Description
STROBE#	O	**STROBE:** The host asserts STROBE# to latch data into the peripheral device's input latch. This signal is controlled via the PCON Register.
BUSY	I	**BUSY:** BUSY is asserted by the peripheral to indicate that the peripheral device is not ready to receive data. The status of this signal line is reported in the PSTAT Register.
ACK#	I	**ACKNOWLEDGE:** The printer asserts this signal to indicate that it has received the data and is ready for new data. The status of this signal line is reported in the PSTAT Register.
SELECT	I	**SELECT:** SELECT is asserted by the peripheral device to indicate that the device is on line. The status of this signal line is reported in the PSTAT Register.
PERROR	I	**PAPER ERROR:** The peripheral device asserts PERROR to indicate that it has encountered an error in the paper path. The exact meaning varies from peripheral device to peripheral device. The status of this signal line is reported in the PSTAT Register.
FAULT#	I	**FAULT:** FAULT# is asserted by the peripheral device to indicate that an error has occurred. The status of this signal line is reported in the PSTAT Register.
INIT#	O	**INITIALIZE:** The host asserts INIT# to issue a hardware reset to the peripheral device. This signal is controlled via the PCON Register.
AUTOFD#	O	**AUTO FEED:** AUTOFD# is asserted by the host to put the peripheral device into auto-line feed mode. This means that when software asserts this signal, the printer is instructed to advance the paper one line for each carriage return encountered. This signal is controlled via the PCON Register.
PD[7:0]	O	**DATA:** Forward channel data.
SELECTIN#	O	**SELECT INPUT:** SELECTIN# is asserted by the host to select a peripheral device. This signal is controlled via the PCON Register.

2.6.2 NIBBLE PROTOCOL SIGNAL DESCRIPTION

The Nibble protocol assigns the following signal operation to the parallel port pins. The name in bold at the beginning of the signal description column is the Nibble protocol signal name. The terms **assert** and **negate** are used in accordance with the 82091AA signal name as described at the beginning of Section 2.0. For example, AUTOFD# (HostBusy) asserted refers to AUTOFD# (HostBusy) at a low level.

82091AA Signal Name	Type	Nibble Protocol Signal Name and Description
STROBE#	O	**STROBE:** The host controls this signal via the PCON Register and STROBE# should be held negated by the host.
BUSY	I	**PRINTER BUSY (PtrBusy):** The peripheral drives this signal to transfer data bits 3 and 7 sequentially. The status of this signal line is reported in the PSTAT Register.
ACK#	I	**PRINTER CLOCK (PtrClk):** The peripheral device asserts ACK# (PtrClk) to indicate to the host that data is available. The signal is subsequently asserted to qualify data being sent to the host. The status of this signal line is reported in the PSTAT Register. If interrupts are enabled via the PCON Register, the assertion of this signal causes a host interrupt to be generated.
SELECT	I	**XFLAG:** The peripheral device drives this signal to transfer data bits 1 and 5 sequentially. The status of this signal line is reported in the PSTAT Register.
PERROR	I	**ACKNOWLEDGE DATA REQUEST (AckDataReq):** This signal is initially high. The peripheral device drives this signal low to acknowledge HostBusy assertion. PERROR is subsequently used to transfer data bits 2 and 6 sequentially. The status of this signal line is reported in the PSTAT Register.
FAULT#	I	**DATA AVAILABLE (DataAvail):** The peripheral device asserts FAULT# (DataAvail) to indicate data availability. Subsequently used to transfer data bits 0 and 4 sequentially. The status of this signal line is reported in the PSTAT Register.
INIT#	O	**INITIALIZE:** The host controls this signal via the PCON Register.
AUTOFD#	O	**HOST BUSY (HostBusy):** The host negates AUTOFD# (HostBusy) in response to ACK# being asserted. This signal is subsequently driven low to enable the peripheral to transfer data to the host. AUTOFD# is then driven high to acknowledge receipt of byte data. This signal is controlled via the PCON Register.
PD[7:0]	O	**DATA:** This 8-bit output data path to the peripheral Host data is written to the peripheral attached to the parallel port interface on these signal lines.
SELECTIN#	O	**SELECT INPUT:** This signal is controlled by the PCON Register.

2.6.3 BYTE MODE SIGNAL DESCRIPTION

The Byte protocol assigns the following signal operation to the parallel port pins. The name in bold at the beginning of the signal description column is the Byte protocol signal name. The terms **assert** and **negate** are used in accordance with the 82091AA signal name as described at the beginning of Section 2.0. For example, STROBE# (HostClk) asserted refers to STROBE# (HostClk) at a low level.

82091AA Signal Name	Type	Byte Protocol Signal Name and Description
STROBE#	O	**HOST CLOCK (HostClk):** This signal is strobed low by the host to acknowledge receipt of data. Note that the peripheral must not interpret this as a latch strobe for forward channel data.
BUSY	I	**PRINTER BUSY (PtrBusy):** The peripheral device asserts BUSY (PtrBusy) to provide forward channel peripheral busy status. The status of this signal line is reported in the PSTAT Register.
ACK#	I	**PRINTER CLOCK (PtrClk):** The peripheral device asserts ACK# (PtrClk) to indicate to the host that data is available. The signal is subsequently asserted to qualify data being sent to the host. The status of this signal line is reported in the PSTAT Register. If interrupts are enabled via the PCON Register, the assertion of this signal causes a host interrupt to be generated.
SELECT	I	**XFLAG:** SELECT (XFLAG) is asserted by the peripheral device to indicate that the device is on line. The status of this signal line is reported in the PSTAT Register.
PERROR	I	**ACKNOWLEDGE DATA REQUEST (AckDataReq):** This signal is initially high. The peripheral device drives this signal low to acknowledge HostBusy assertion. The status of this signal line is reported in the PSTAT Register.
FAULT#	I	**DATA AVAILABILITY (DataAvail):** The peripheral device asserts FAULT# (DataAvail) to indicate data availability. The status of this signal line is reported in the PSTAT Register.
INIT#	O	**INITIALIZE:** The host controls this signal via the PCON Register and INIT# should be held in the negated state.
AUTOFD#	O	**HOST BUSY (HostBusy):** The host negates AUTOFD# (HostBusy) in response to ACK# being asserted.The signal is subsequently driven low to enable the peripheral to transfer data to the host. AUTOFD# is then driven high to acknowledge receipt of nibble data. This signal is controlled via the PCON Register.
PD[7:0]	O	**DATA:** This 8-bit data bus is used for bi-directional data transfer.
SELECTIN#	I/O	**SELECT INPUT:** This signal is controlled by the PCON Register.

2.6.4 ENHANCED PARALLEL PORT (EPP) PROTOCOL SIGNAL DESCRIPTION

EPP protocol assigns the following signal operation to the parallel port pins. The name in bold at the beginning of the signal description column is the EPP mode signal name. The terms **assert** and **negate** are used in accordance with the 82091AA signal name as described at the beginning of Section 2.0. For example, BUSY (Wait#) asserted refers to BUSY (Wait#) being high.

82091AA Signal Name	Type	EPP Protocol Signal Name and Description
STROBE#	O	**WRITE (Write#):** STROBE# (Write#) indicates an address or data read/write operation to the peripheral. The 82091AA drives this signal low for a write and high for a read.
BUSY	I	**WAIT (Wait#):** The peripheral sets BUSY (Wait#) low to indicate that the device is not ready. When BUSY signal is low, the 82091AA negates IOCHRDY on the ISA Bus to lengthen the I/O cycles. The peripheral device sets BUSY (Wait#) high to indicate that transfer of data or address is completed.
ACK#	I	**INTERRUPT REQUEST (Intr):** The peripheral asserts ACK# (Intr) to generate an interrupt the host. When this signal is low and interrupts are enabled via bit 4 of the PCON Register, the 82091AA generates an interrupt request (via either IRQ5 or IRQ7) to the host.
SELECT	I	**SELECT:** SELECT is asserted by the peripheral device to indicate that the device is on line. The status of this signal line is reported in the PSTAT Register.
PERROR	I	**PAPER ERROR:** The peripheral device asserts PERROR to indicate that it has encountered an error in the paper path. The exact meaning varies from peripheral device to peripheral device. The status of this signal line is reported in the PSTAT Register.
FAULT#	I	**FAULT:** FAULT# is asserted by the peripheral device to indicate that an error has occurred. The status of this signal line is reported in the PSTAT Register.
INIT#	O	**INITIALIZE:** The host asserts INIT# to issue a hardware reset to the peripheral device. This signal is controlled via the PCON Register.
AUTOFD#	O	**DATA STROBE (DStrb#):** The 82091AA asserts AUTOFD# (DStrb#) to indicate that valid data is present on PD[7:0] and is used by the peripheral to latch data during write cycles. For reads, the 82091AA reads in data from PD[7:0] when this signal is asserted.
PD[7:0]	I/O	**DATA:** This 8-bit bi-directional bus provides addresses or data during the write cycles and supplies addresses or data to the 82091AA during the read cycles.
SELECTIN#	O	**ADDRESS STROBE (AStrb#):** The 82091AA asserts SELECTIN# (AStrb#) to indicate that a valid address is present on PD[7:0] and is used by the peripheral to latch addresses during write cycles. For reads, the 82091AA reads in an address from PD[7:0] when this signal is asserted.

2.6.5 EXTENDED CAPABILITIES PORT (ECP) PROTOCOL SIGNAL DESCRIPTION

ECP protocol assigns the following signal operation to the parallel port pins. The name in bold at the beginning of the signal description column is the ECP protocol signal name. The terms **assert** and **negate** are used in accordance with the 82091AA signal name as described at the beginning of Section 2.0. For example, STROBE# (HostClk) asserted refers to STROBE# (HostClk) being low.

82091AA Signal Name	Type	ECP Protocol Signal Name and Description
STROBE#	O	**HOST CLOCK (HostClk):** In the forward direction, the 82091AA asserts STROBE# (HostClk) to instruct the peripheral to latch the data on PD[7:0]. During write operations, the peripheral should latch data on the rising edge of STROBE# (HostClk). STROBE# (HostClk) handshakes with BUSY (PeriphAck) during write operations and is negated after the 82091AA detects BUSY (PeriphAck) asserted. STROBE# (HostClk) is not asserted by the 82091AA again until BUSY (PeriphAck) is detected negated. For read operations (reverse direction), STROBE# (HostClk) is not used.
BUSY	I	**PERIPHERAL ACKNOWLEDGE (PeriphAck):** The peripheral device asserts this signal during a host write operation to acknowledge receipt of data. The peripheral device then negates the signal after STROBE# is detected high to terminate the transfer. For host write operations (forward direction), this signal handshakes with STROBE# (HostClk). During a host read operation (reverse direction), BUSY (PeriphAck) is normally low and is driven high by the peripheral to identify Run Length Encoded (RLE) data.
ACK#	I	**PERIPHERAL CLOCK (PeriphClk):** During a peripheral to host transfer (reverse direction), ACK# (PeriphClk) is asserted by the peripheral to indicate data is valid on the data bus and then negated after AUTOFD# is detected high. This signal handshakes with AUTOFD# to transfer data.
SELECT	I	**XFLAG (Xflag):** This signal is asserted by the peripheral to indicate that it is on-line. The status of this signal line is reported in the PSTAT Register.
PERROR	I	**ACKNOWLEDGE REVERSE (AckReverse#):** PERROR (AckReverse#) is driven low by the peripheral to acknowledge a reverse transfer request by the host. This signal handshakes with INIT# (ReverseRequest#). The status of this signal line is reported in the PSTAT Register.
FAULT#	I	**PERIPHERAL REQUEST (PeriphRequest#):** The peripheral asserts FAULT# (PeriphRequest#) to request a reverse transfer. The status of this signal line is reported in the PSTAT Register.
INIT#	O	**REVERSE REQUEST (ReverseRequest#):** The host controls this signal via the PCON Register to indicate the transfer direction. The host asserts this signal to request a reverse transfer direction and negates the signal for a forward transfer direction.
AUTOFD#	O	**HOST ACKNOWLEDGE (HostAck):** The 82091AA asserts AUTOFD# (HostAck) to request data from the peripheral (reverse direction). This signal handshakes with ACK# (PeriphClk). AUTOFD# (HostAck) is negated when the peripheral indicates valid state of the data bus (i.e., ACK# is detected asserted). In the forward direction, AUTOFD# (HostAck) indicates whether PD[7:0] contain an address/RLE or data. The 82091AA asserts this signal to identify an address/RLE transfer and negates it to identify a data transfer.
PD[7:0]	I/O	**DATA:** PD[7:0] is a bi-directional data bus that transfers data, addresses, or RLE data.
SELECTIN#	O	**ECP MODE (ECPmode):** The host (via the PCON Register) negates this signal during ECP mode operation.

2.7 Hard Reset Signal Conditions

Table 1 shows the state of all 82091AA output and bi-directional signals during hard reset (RSTDRV asserted). The strapping options described in Section 4.0, AIP Configuration are sampled when the 82091AA is hard reset.

Table 2. Output and I/O Signal States During a Hard Reset

Signal Name	State
ACK#	—
AEN	—
AUTOFD#	Tri-state
BUSY	—
CTS[A,B]#	—
DCD[A,B]#	High
DEN#	High(1)
DIR#	High
DRVDEN[1:0]0	Low
DSKCHG#	—
DTR[A,B]#	High(1)
FAULT#	—
FDDACK#	—
FDDREQ	Tri-state
FDME0#/MEEN#	High
FDME1#/DSEN#	High
FDS0#/MDS0	High
FDS1#/MDS1	High

Signal Name	State
HDSEL	High
HEN#	High(1)
IDECS[1,0]#	High(1)
INDX#	—
INIT#	Low
IO16#	—
IOCHRDY	Tri-state(2)
IORC#	—
IOWC#	—
IRQ[7:3]	Tri-state
NOWS#	Tri-state
PD[7:0]	Low
PERROR	—
PPDACK#	—
PPDREQ	Tri-state
PPDIR/GCS#	High(1)
RDDATA	—
RI[A,B]#	—

Signal Name	State
RSTDRV	—
RTS[A,B]#	High(1)
SA[10,0]	—
SD[7:0]	Tri-state
SELECT	—
SELECTIN#	Tri-state
SIN[A,B]	—
SOUT[A,B]	High(1)
STEP#	High
STROBE#	Tri-state
TC	—
TRK0#	—
WE#	High
WP#	—
WRDATA#	High
X1/OSC	—
X2	—

NOTES:
1. During and immediately after a hard reset, this signal is an input for hardware configuration. After the hardware configuration time, these signals go to the state specified in the table.
2. If IORC# or IOWC# is asserted, IOCHRDY will be asserted by the IOCHRDY.
3. Dashes represent input signals.

2.8 Power And Ground

Signal Name	Type	Description
V_{SS}	I	**GROUND:** The ground reference for the 82091AA.
V_{CC}	I	**POWER:** The 5V/3.3V(1) modes are selected via strapping options at power-up (see Section 4.2, hardware Configuration). When strapping options (V_{SEL}) are set to 5V, the V_{CC} pins must be connected to 5V. When strapping options are set to 3.3V, the V_{CC} pins must be connected to 3.3V.
V_{CCF}	I	**POWER:** The 5V/3.3V(1) power supply for the 82091AA. In 5V or 3.3V power supply modes (non-mixed mode), the voltage applied to V_{CCF} is the same voltage as applied to V_{CC}. For mixed mode operations, 5V is applied to V_{CCF}. This voltage provides 5V reference for the parallel port and floppy disk controller interfaces. Note that in mixed mode, 3.3V is applied to V_{CC}.

NOTE:
1. 3.3V operation is available only in the 82091AA.

2

3.0 I/O ADDRESS ASSIGNMENTS

The 82091AA assigns CPU I/O address locations to its game port chip select, IDE interface, serial ports, parallel port, floppy disk controller, and the 82091AA configuration registers as indicated in Table 3. Except for the game port chip select (address 201h), address assignments are configurable. For example, the serial port can be assigned to one of eight address blocks. The parallel port can be assigned to one of three address blocks, and the IDE interface and floppy disk controller can be assigned to one of two address blocks. These address assignments are made during 82091AA configuration (either hardware configuration at powerup or a hard reset, or software configuration by programming the 82091AA configuration registers). In addition, the 82091AA configuration registers can be located at one of two address blocks during hardware configuration.

All of the 82091AA address locations are located in the host I/O address space. The address block assignments are shown in Table 3. The first hex address in the Address Block column represents the base address for that particular block.

Table 3. AIP Address Assignments

Address Block (ISA Bus)	Assignment
170–177h	IDE Interface—Secondary Address Block
1F0–1F7h	IDE Interface—Primary Address Block
201h	Game Port Chip Select
220–227h	Serial Port
228–22Fh	Serial Port
238–23Fh	Serial Port
26E–26Fh	82091AA Configuration Registers—Primary Address Block (022–023h on X-Bus)
278–27Fh	Parallel Port
2E8–2EFh	Serial Port
2F8–2FFh	Serial Port
338–33Fh	Serial Port
370–377h	Floppy Disk Controller—Secondary Address Block (376h and 377h are Shared with the IDE Drive Interface Secondary Address)
378–37Fh	Parallel Port
398–399h	82091AA Configuration Registers—Secondary Address Block (024–025h on X-Bus)
3BC–3BFh	Parallel Port (All Mopes Except EPP)
3E8–3EFh	Serial Port
3F0–3F7h	Floppy Disk Controller—Primary Address (3F6h and 3F7h are Shared with the IDE Drive Interface Primary Address)
3F8–3FFh	Serial Port
678–67Ah	Parallel Port (ECP Mode Peripheral Interface Protocol)
778–77Ah	Parallel Port (ECP Mode Peripheral Interface Protocol)
7BC–7BEh	Parallel Port (ECP Mode Peripheral Interface Protocol)

NOTES:
1. The 82091AA does not contain IDE registers. However, the 82091AA provides the address block assignments for accessing the IDE registers that are located in the IDE device.
2. The standard PC/AT* compatible logical I/O address assignments are supported. For example, COM1 (3F8–3FFh) and COM2 (2F8–2FFh) are part of the serial port assignments and LPT1 (3BC–3BFh), LPT2 (378–37Fh), and LPT3 (278–27Fh) are part of the parallel port assignments.

*Other brands and names are the property of their respective owners.

4.0 AIP CONFIGURATION

82091AA configuration consists of setting up overall device operations along with certain functions pertaining to the individual 82091AA modules (parallel port, serial ports, floppy disk controller, and IDE interface). Overall device operations include selecting the clock frequency, power supply voltage, and address assignment for the configuration registers. Overall device operations also enable/disable access to the configuration registers and provide interrupt signal level control. For the individual modules, 82091AA configuration includes module address assignment, interrupt control, module enable/disable, powerdown control, test mode control, module reset, and certain functions specific to each module. The remainder of the functions unique to each module are handled via the individual module registers.

Two methods are provided for configuring the 82091AA—hardware configuration via strapping options at powerup (or whenever RSTDRV is asserted) and software configuration by programming the configuration registers. (For information on hardware configuration, see Section 4.2, Hardware Configuration. For information on software configuration, see Section 4.1, Configuration Registers.)

NOTE:

1. There are four hardware configuration modes—SWMB (Software Motherboard), SWAI (Software Add-In), HWB (Hardware Basic), and HWE (Hardware Extended). Some of these modes can be used without the need for programming the 82091AA configuration registers. Other modes use both hardware configuration strapping options and programming the configuration registers to set up the 82091AA.
2. The 82091AA's operating power supply voltage level, 82091AA clock frequency, and address assignment for the 82091AA configuration registers can only be configured by hardware configuration.

4.1 Configuration Registers

82091AA Configuration Space contains 13 configuration registers. Four of the registers (Product and Revision Identification Registers and the 82091AA Configuration 1 and 2 Registers) provide control and status information for the entire chip. In addition, two registers each for the floppy disk controller, parallel port, serial port A, and serial port B and one register for the IDE interface provide certain module status and control information. The 82091AA configuration registers are indirectly addressed by first writing to the 82091AA Configuration Index Register as described in Section 4.1.1. Thus, the 13 configuration registers occupy two address locations in the host's I/O address space—one for indirectly selecting the specific configuration register and the other for transfering register data. All 82091AA configuration registers are 8-bits wide and are accessed as byte quantities.

Some of the 82091AA Configuration registers described in this section contain reserved bits. These bits are labeled "R". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the value of reserved bit positions must first be read, merged with the new values for other bit positions, and then written back.

In addition to reserved bits within a register, the 82091AA configuration space contains address locations that are labeled "Reserved" (Table 5). While the 82091AA responds to accesses to these I/O addresses by completing the host cycle, writing to a reserved I/O address can result in unintended device operations. Values read from a reserved I/O address should not be used to permit future expansion and upgrades.

During a hard reset (RSTDRV asserted), the 82091AA sets its configuration registers to pre-determined **default** states. The default values are indicated in the individual register descriptions. The following nomenclature is used for register access attributes:

RO **Read Only.** If a register is read only, writes have no effect.

R/W **Read/Write.** A register with this attribute can be read and written. Note that individual bits in some read/write registers may be read only.

4.1.1 CFGINDX, CFGTRGT—CONFIGURATION INDEX REGISTER AND TARGET PORT

I/O Address: Hardware Configurable (see Table 4)
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

CFGINDX and CFGTRGT are used to access 82091AA configuration space where all of the 82091AA configuration registers are located. CFGINDX and CFGTRGT are located in the host I/O address space and the address locations are hardware configurable as shown in Table 4. CFGINDX is an 8-bit register that contains the address index of the 82091AA configuration register to be accessed. CFGTRGT is a port for reading data from or writing data to the configuration register whose index address matches the address stored in the CFGINDX Register. Thus, to access a configuration register, CFGINDX must first be programmed with the index address. A software example is provided in this section demonstrating how to access the configuration registers.

Table 4. Configuration Register Access Addresses

Address Selection	X-Bus Implementation		ISA Bus Implementation	
	Index	Target	Index	Target
Primary Address	22h	23h	26Eh	26Fh
Secondary Address	24h	25h	398h	399h

Table 5 summarizes the 82091AA configuration space. Following the table, is a detailed description of each register. The register descriptions are arranged in the order that they appear in Table 5.

Bit	Description
7:0	**82091AA Configuration Register Address Index:** Bits[7:0] correspond to SD[7:0].

Software Configuration

Access Addresses for the two Software Configuration Modes:

	Index	Target
For SWMB Mode Primary Address:	22h	23h
For SWMB Mode Secondary Address:	24h	25h
For SWAI, HWE, and HWB Modes Primary Address:	26Eh	26Fh
For SWAI, HWE, and HWB Modes Secondary Address:	398h	399h

The following pseudo code sequence could be used to access the configuration registers under SWMB primary address:

Configuration register write: OUT 22h, ConfigRegAddr
OUT 23h, ConfigRegData

Configuration register read: OUT 22h, ConfigRegAddr
IN 23h

Table 5. AIP Configuration Registers

82091AA Configuration Address Index	Abbreviation	Register Name	Access
00h	AIPID	Product Identification	RO
01h	AIPREV	Revision Identification	RO
02h	AIPCFG1	82091AA Configuration 1	R/W
03h	AIPCFG2	82091AA Configuration 2	R/W
04–0Fh	—	Reserved	—
10h	FCFG1	FDC Configuration	R/W
11h	FCFG2	FDC Power Management and Status	R/W
12–1Fh	—	Reserved	—
20h	PCFG	Parallel Port Configuration	R/W
21h	PCFG2	Parallel Port Power Management and Status	R/W
22–2Fh	—	Reserved	—
30h	SACFG1	Serial Port A Configuration	R/W
31h	SACFG2	Serial Port A Power Management and Status	R/W
32–3Fh	—	Reserved	—
40h	SBCFG1	Serial Port B Configuration	R/W
41h	SBCFG2	Serial Port B Power Management and Status	R/W
42–4Fh	—	Reserved	—
50h	ICFG	IDE Configuration	R/W
51–FFh	—	Reserved	—

NOTE:
Writing to a reserved I/O address should not be attempted and can result in unintended device operations.

4.1.2 AIPID—AIP IDENTIFICATION REGISTER

Index Address: 00h
Default Value: A0h
Attribute: Read Only
Size: 8 bits

Bit	Description
7:0	**AIP IDENTIFICATION (AIPID):** A value of A0h is assigned to the 82091AA. This 8-bit register combined with the 82091AA Revision Identification Register uniquely identifies the device.

4.1.3 AIPREV—AIP REVISION IDENTIFICATION

Index Address: 01h
Default Value: 00h
Attribute: Read Only
Size: 8 bits

This register contains two fields that identify the revision of the 82091AA device. The revision number will be incremented for every stepping, even if change is invisible to software.

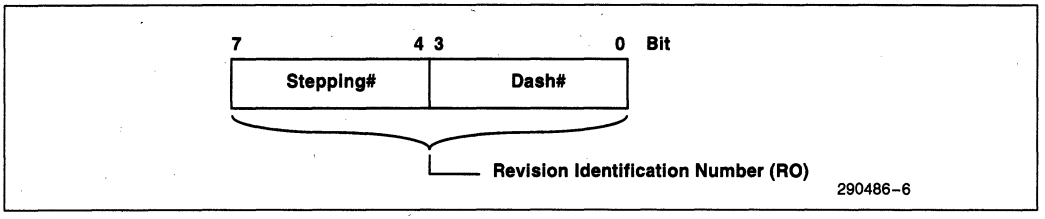


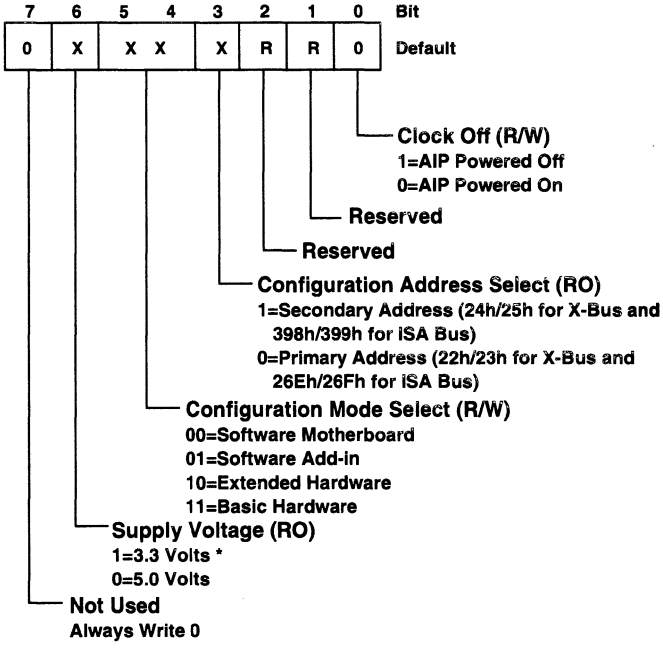
Figure 6. AIP Revision Identification Register

Bit	Description
7:4	**STEP NUMBER:** Contains the hexadecimal representation of the device stepping.
3:0	**DASH NUMBER:** Contains the hexadecimal representation of the dash number of the device stepping.

4.1.4 AIPCFG1—AIP CONFIGURATION 1 REGISTER

Index Address: 02h
Default Value: Depends upon hardware strap
Attribute: Read/Write
Size: 8 bits

The AIPCFG1 Register enables/disables master clock circuitry for power management, enables/disables access to the configuration registers, and selects the 82091AA configuration mode. This register provides status for certain hardware configuration selections—the 82091AA clock frequency, power supply voltage, and address assignment for the configuration registers (address locations of the INDEX and TARGET Registers).



NOTES:
*3.3V operation is available only in the 82091AA.
X = Value is determined by hardware strapping options as described in Section 4.2, Hardware Configuration.

Figure 7. AIP Configuration 1 Register

Bit	Description
7	**NOT USED:** Always write to 0.
6	**VOLTAGE SELECT (VSEL):** This bit indicates whether 3.3V or 5V has been selected for the operating power supply voltage during hardware configuration. A 1 indicates that 3.3V is selected and a 0 indicates that 5V is selected. This bit is read only and writes have no effect. **NOTE:** 3.3V operation is available only in the 82091AA.
5:4	**CONFIGURATION MODE SELECT (CFGMOD):** These bits indicate the configuration mode for the 82091AA. After a hard reset, these bits reflect the mode selected by hardware configuration. If configuration register access is not locked out during hardware configuration, software can change the configuration mode by writing to this field. For configuration mode details, (see Section 4.2, Hardware Configuration). **Bits[5:4] Configuration Mode** 0 0 Software Motherboard (SWMB) 0 1 Software Add-in (SWAI) 1 0 Extended Hardware (HWE) 1 1 Basic Hardware (HWB)
3	**CONFIGURATION ADDRESS SELECT (CFGADS):** This read only bit indicates the address assignment for the 82091AA configuration registers as selected by hardware configuration. Hardware configuration selects between primary addresses (22h/23h and 26Eh/26Fh) and secondary addresses (24h/25h and 398h/399h) for accessing the 82091AA configuration registers. When CFGADS = 0, the primary addresses are selected and when CFGADS = 1, the secondary addresses are selected.
2	**RESERVED**
1	**RESERVED**
0	**CLOCK OFF (CLKOFF):** The CLKOFF bit is used to implement clock circuitry power management. When CLKOFF = 0, the main clock circuitry is powered on. When CLKOFF = 1, the main clock circuitry is powered off. This capability is independent of the 82091AA's powerdown state. Note that auto powerdown mode and powerdown have no effect over the power state of the clock circuitry.

4.1.5 AIPCFG2—AIP CONFIGURATION 2 REGISTER

Index Address: 03h
Default Value: 0000 0RRR
Attribute: Read/Write
Size: 8 bits

This register selects the active signal level for IRQ[7:3]. The interrupt signals can be individually programmed for either active high or active low drive characteristics. The active high mode is ISA (non-share) compatible and has tri-state drive characteristic. The active low mode is EISA (sharable) compatible and has an open collector drive characteristic.

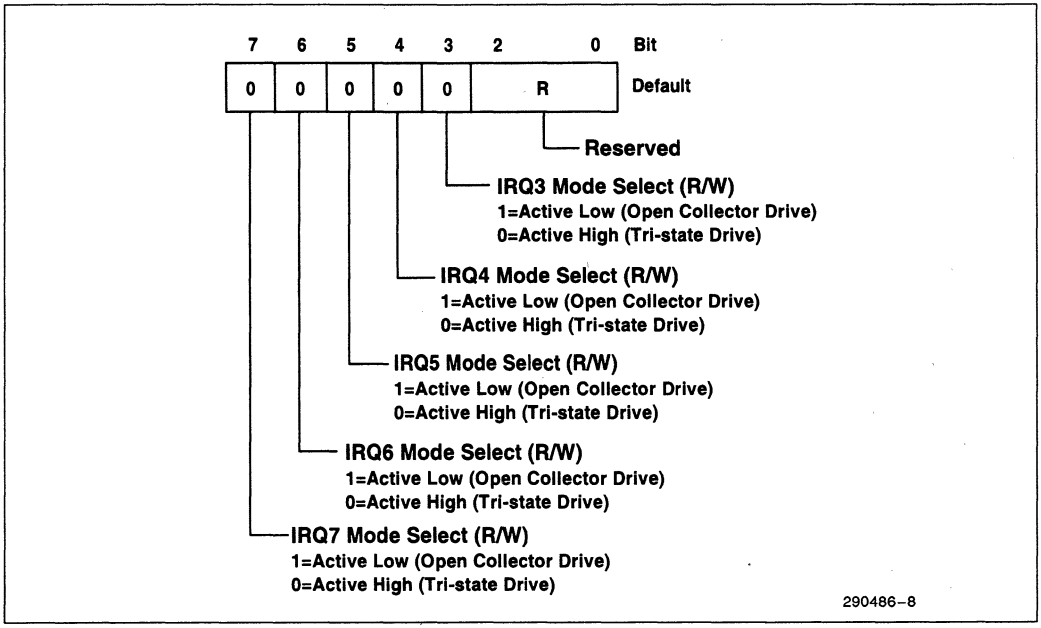


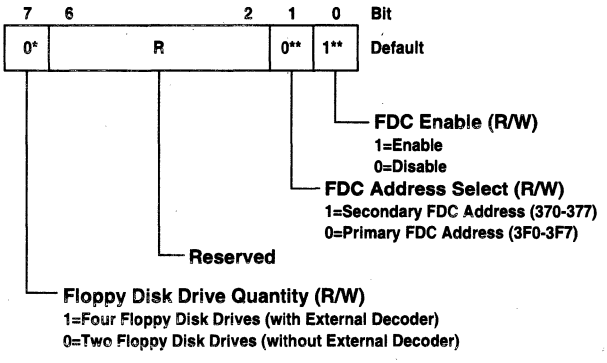
Figure 8. AIP Configuration 2 Register

Bit	Description
7	**IRQ7 MODE SELECT (IRQ7MOD):** When IRQ7MOD = 0, IRQ7 is an active high tri-state drive signal. When IRQ7MOD = 1, IRQ7 is an active low open collector drive signal.
6	**IRQ6 MODE SELECT (IRQ6MOD):** When IRQ6MOD = 0, IRQ6 is an active high tri-state drive signal. When IRQ6MOD = 1, IRQ6 is an active low open collector drive signal.
5	**IRQ5 MODE SELECT (IRQ5MOD):** When IRQ5MOD = 0, IRQ5 is an active high tri-state drive signal. When IRQ5MOD = 1, IRQ5 is an active low open collector drive signal.
4	**IRQ4 MODE SELECT (IRQ4MOD):** When IRQ4MOD = 0, IRQ4 is an active high tri-state drive signal. When IRQ4MOD = 1, IRQ4 is an active low open collector drive signal.
3	**IRQ3 MODE SELECT (IRQ3MOD):** When IRQ3MOD = 0, IRQ3 is an active high tri-state drive signal. When IRQ3MOD = 1, IRQ3 is an active low open collector drive signal.
2:0	**RESERVED**

4.1.6 FCFG1—FDC CONFIGURATION REGISTER

Index Address: 10h
Default Value: 0RRR RR01
Attribute: Read/Write
Size: 8 bits

This register selects between a 2 and 4 floppy drive system, selects primary/secondary ISA address range for the FDC, and enables/disables the FDC. All bits in this register are read/write.



NOTES:
*Default shown is for SWMB, SWAI, and HWB hardware configuration modes. For HWE, the default is determined by hardware strapping options as described in Section 4.2, Hardware Configuration.
**Default shown is for SWMB and SWAI configuration modes. For HWB and HWE configuration modes, the default is determined by hardware strapping options as described in Section 4.2, Hardware Configuration.

Figure 9. FDC Configuration Register

Bit	Description
7	**FLOPPY DISK DRIVE QUANTITY (FDDQTY):** This bit selects between two and four floppy disk drive capability. When FDDQTY = 0, the 82091AA can control two floppy disk drives directly without an external decoder. When FDDQTY = 1, the 82091AA can control four floppy disk drives with an external decoder. When FDDQTY = 1, the PDEN feature in the powerdown command is disabled. For further details, see Appendix A, FDC Four Drive Support. This bit can be configured by hardware extended configuration (HWE) at powerup. For all other hardware configuration modes (SWMB, SWAI, and HWB), the floppy disk drive quantity is not configurable by hardware strapping options and defaults to 2 drives.
6:2	**RESERVED**
1	**FLOPPY DISK CONTROLLER ADDRESS SELECT (FADS):** When FADS = 0, the primary FDC address (3F0–3F7) is selected. When FADS = 1, the secondary FDC address (370–377) is selected. For SWMB and SWAI configuration modes, the default is 0 (primary address). For HWB and HWE hardware configuration modes, the default is determined by signal pin strapping options.
0	**FLOPPY DISK CONTROLLER ENABLE (FEN):** This bit enables/disables the FDC. When FEN = 1, the FDC is enabled. When FEN = 0, the FDC module is disabled. For SWMB and SWAI configuration modes, the default is 1 (enabled). For HWB and HWE hardware configuration modes, the default is determined by signal pin strapping options. Note that, when the FDC is disabled, IRQ6 and FDDREQ are tri-stated.

4.1.7 FCFG2—FDC POWER MANAGEMENT AND STATUS REGISTER

Index Address: 11h
Default Value: RRRR 0000
Attribute: Read/Write
Size: 8 bits

This register enables/disables FDC auto powerdown and can place the FDC into direct powerdown. The register also provides FDC idle status and FDC reset control.

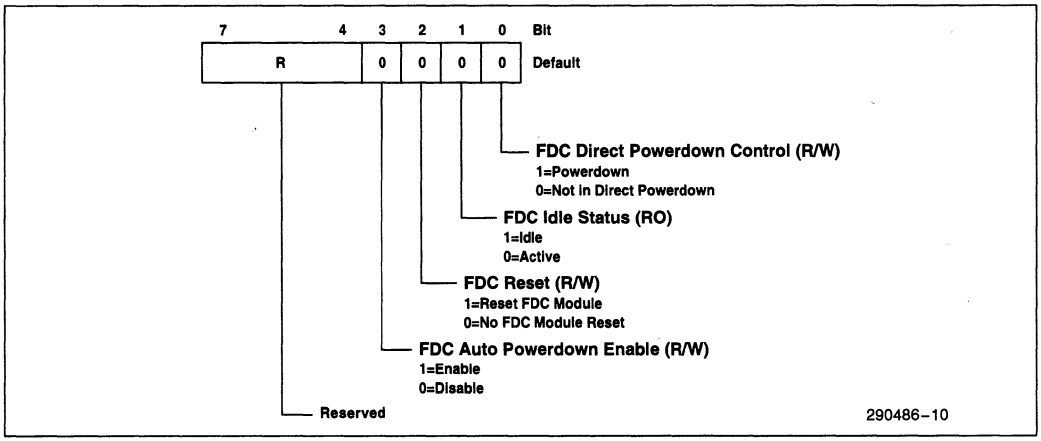


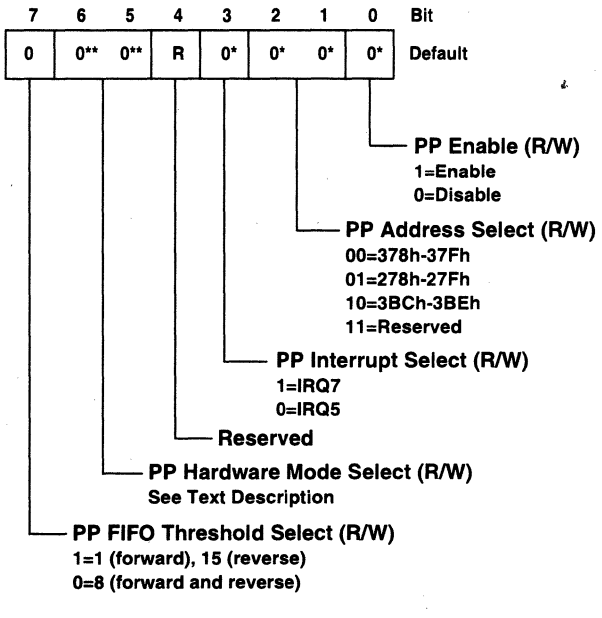
Figure 10. FDC Power Management and Status Register

Bit	Description
7:4	**RESERVED**
3	**FLOPPY DISK AUTO POWERDOWN ENABLE (FAPDN):** This bit is used to enable/disable auto powerdown for the FDC. When FAPDN = 1, the FDC will enter auto powerdown when the required conditions are met. When FAPDN = 0, FDC auto powerdown is disabled.
2	**FLOPPY DISK CONTROLLER RESET (FRESET):** FRESET is a reset for the FDC. When FRESET = 1, the FDC is reset (i.e., all programming and current state information is lost). FRESET = 1 has the same affect on the FDC as a hard reset (asserting the RSTDRV signal). When resetting the FDC via this configuration bit, the software must toggle this bit and ensure the reset active time (FRESET = 1) of 1.13 μs minimum is met.
1	**FLOPPY DISK CONTROLLER IDLE STATUS (FIDLE):** When the FDC is in the idle state, this bit is set to 1 by the 82091AA hardware. In the idle state the FDC's Main Status Register (MSR) = 80h, IRQ6 = inactive, and the head unload timer has expired. When the FDC exits its idle state, this bit is set to 0. This bit is read only.
0	**FLOPPY DISK CONTROLLER POWERDOWN (FDPDN):** When FDPDN is set to 1, the FDC is placed in direct powerdown. Once in powerdown the following procedure should be used to bring the FDC out of powerdown: • Write this bit low • Apply a hardware reset (via bit 2 of this register) or a software reset (via either bit 2 of the FDC's DOR or bit 7 of the FDC's DSR). **NOTE:** A hard reset via the RSTDRV pin also removes the FDC powerdown.

4.1.8 PCFG1—PARALLEL PORT CONFIGURATION REGISTER

Index Address: 20h
Default Value: 000R 0000
Attribute: Read/Write
Size: 8 bits

The PCFG1 Register enables/disables the parallel port, selects the parallel port address, and selects the parallel port interrupt. This register also selects the hardware operation mode for the parallel port.



NOTES:
*Default shown is for SWMB and SWAI configuration modes. For HWB and HWE modes, the default is determined by hardware configuration options as described in Section 4.2, Hardware Configuration.
**Default shown is for SWMB, SWAI, and HWB configuration modes. For HWE mode, the default is determined by hardware configuration options as described in Section 4.2, Hardware Configuration.

Figure 11. Parallel Port Configuration Register

Bit	Description
7	**PARALLEL PORT FIFO THRESHOLD SELECT (PTHRSEL):** This bit controls the FIFO threshold and only affects parallel port operations when the parallel port is in ECP mode or ISA-Compatible FIFO mode. When PTHRSEL = 1, the FIFO threshhold is 1 in the forward direction and 15 in the reverse direction. When PTHRSEL = 0, the FIFO threshold is 8 in both directions. This bit can only be programmed when the parallel port is in ISA-Compatible or PS/2-Compatible mode. These modes can be selected via bits[6:5] of this register or the ECP Extended Control Register (ECR). **NOTE:** In the reverse direction, a threshold of 15/8 means that a request (DMA or Interrupt is enabled) is generated when 15/8 bytes are in the FIFO. In the forward direction, a threshold of 1/8 means that a request is generated when 1/8 byte locations are available.
6:5	**PARALLEL PORT HARDWARE MODE SELECT (PPHMOD):** This field selects the parallel port hardware mode. The ISA-Compatible mode is for compatibility and nibble mode peripheral interface protocols. The PS/2-Compatible mode is for the byte mode peripheral interface protocol. The EPP and ECP modes are for the EPP and ECP mode peripheral interface protocols, respectively. This field can be configured by strapping options at powerup for hardware extended configuration (HWE) mode only. For all other hardware configuration modes (SWMB, SWAI, and HWB), the default is 00 (ISA-Compatible). **Bits [6:5] — Read — Write** 0 0 — ISA-Compatible — ISA-Compatible(1) 0 1 — PS/2-Compatible — PS/2-Compatible(1) 1 0 — EPP — EPP(1, 3) 1 1 — ECP(2) — Reserved; do not write(2) **NOTES:** 1. ISA-Compatible, PS/2-Compatible, and EPP modes are selected via this field or hardware configuration. In addition, ISA-Compatible and PS/2-Compatible modes can be selected via the ECP Extended Control Register (ECR). When the ECR is programmed for one of these two modes (ECR[7:5] = 000, 001), this field is updated to match the selected mode. 2. ECP Mode can not be entered by programming this field. ECP Mode can only be selected through the ECR. When the ECR is programmed for ECP mode, the 82091AA sets this field to 11. 3. Parallel port interface signals controlled by the PCON Register (SELECTIN#, INIT#, AUTOFD#, and STROBE#) should be negated before entering EPP mode.
4	**RESERVED**
3	**PARALLEL PORT IRQ SELECT (PIRQSEL):** When PIRQSEL = 1, IRQ7 is selected as the parallel port interrupt. When PIRQSEL = 0, IRQ5 is selected as the parallel port interrupt. This field can be configured by strapping options at powerup for HWB and HWE modes only. For all other hardware configuration modes (SWMB and SWAI), the default is 0 (IRQ5).

Bit	Description
2:1	**PARALLEL PORT ADDRESS SELECT (PADS):** This field selects the address for the parallel port as follows: **Bits[2:1] / Address / Parallel Port Hardware Mode** 0 0 / 378–37F / All 0 1 / 278–27F / All 1 0 / 3BC–3BE / All except EPP 1 1 / Reserved / None, do not write This field can be configured by strapping options at powerup for HWB and HWE modes only. For all other hardware configuration modes (SWMB and SWAI), the default is 00 (378h–37Fh). Note that the SWMB and SWAI default settings for PIRQSEL (bit 3) and PADS (bits[2,1]) do not match a standard PC/AT* combination for address assignment and interrupt setting. However, for SWMB and SWAI, the parallel port defaults to a disabled condition and this register must be programmed to enable the parallel port (i.e., bit 0 set to 1). At this time, the selections for interrupt and address assignments should be made.
0	**PARALLEL PORT ENABLE (PEN):** When PEN = 0, the parallel port is disabled. When PEN = 1, the parallel port is enabled. This bit can be configured by hardware strapping options at powerup for HWB and HWE modes only. For all other hardware configuration modes (SWMB and SWAI), the default is 0 (disabled). Note that when the parallel port is disabled, IRQ[7,5] and PPDREQ are tri-stated.

4.1.9 PCFG2—PARALLEL PORT POWER MANAGEMENT AND STATUS REGISTER

Index Address: 21h
Default Value: RR0R 0000
Attribute: Read/Write
Size: 8 bits

This register enables/disables parallel port auto powerdown and can place the parallel port into a powerdown mode directly. The register also provides parallel port idle status, resets the parallel port, and reports FIFO underrun or overrun errors.

*Other brands and names are the property of their respective owners.

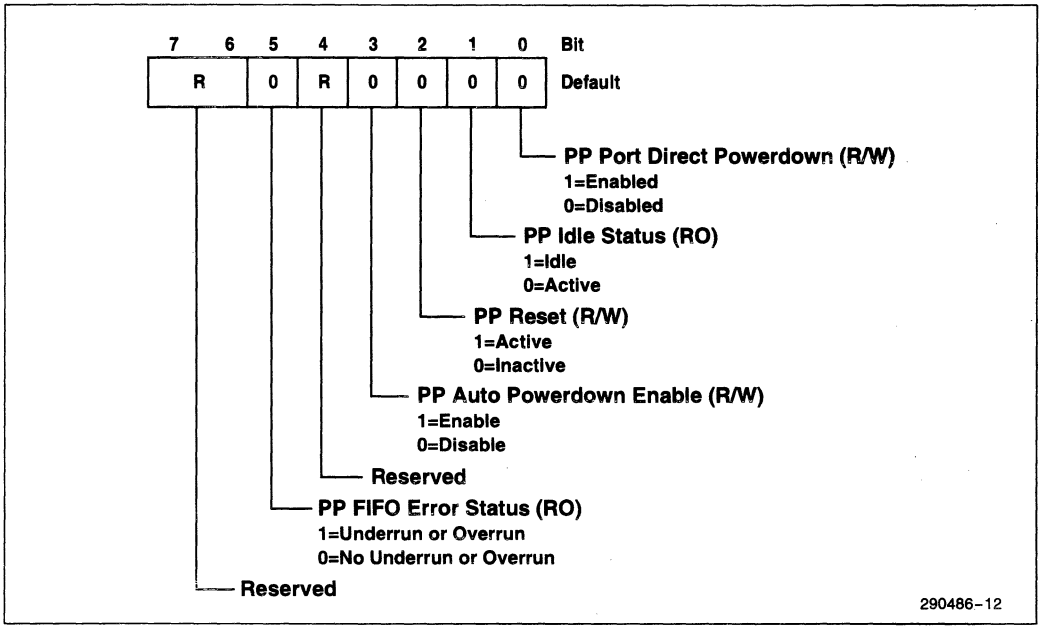


Figure 12. Parallel Port Power Management and Status Register

Bit	Description
7:6	**RESERVED**
5	**PARALLEL PORT FIFO ERROR STATUS (PFERR):** When PFERR = 1, a FIFO underrun or overrun condition has occurred. This bit is read only. Setting PRESET to 1 clears this bit to 0.
4	**RESERVED**
3	**PARALLEL PORT AUTO POWERDOWN ENABLE (PAPDN):** When PAPDN = 1, the parallel port can enter auto powerdown if the required auto powerdown conditions are met. When PAPDN = 0, auto powerdown is disabled.
2	**PARALLEL PORT RESET (PRESET):** When PRESET is set to 1, the parallel port is reset (i.e., all programming and current state information is lost). This is the same state the module would be in after a hard reset (RSTDRV asserted) to the 82091AA. When resetting the parallel port via this configuration bit, the software must toggle this bit and ensure the reset active time (PRESET = 1) of 1.13 μs minimum is met.
1	**PARALLEL PORT IDLE STATUS (PIDLE):** This bit reflects the idle state of the parallel port. When the parallel port is in an idle state (i.e., when the same conditions are met that apply to entering auto powerdown) the 82091AA sets this bit to 1. The parallel port idle state is defined as the FIFO empty and no activity on the parallel port interface. This bit is read only.
0	**PARALLEL PORT DIRECT POWERDOWN (PDPDN):** When PDPDN is set to 1, the parallel port enters direct powerdown. When PDPDN is set to 0, the parallel port is not in direct powerdown. Note that a parallel port module reset (PRESET bit in this register) also brings the parallel port out of the direct powerdown state.

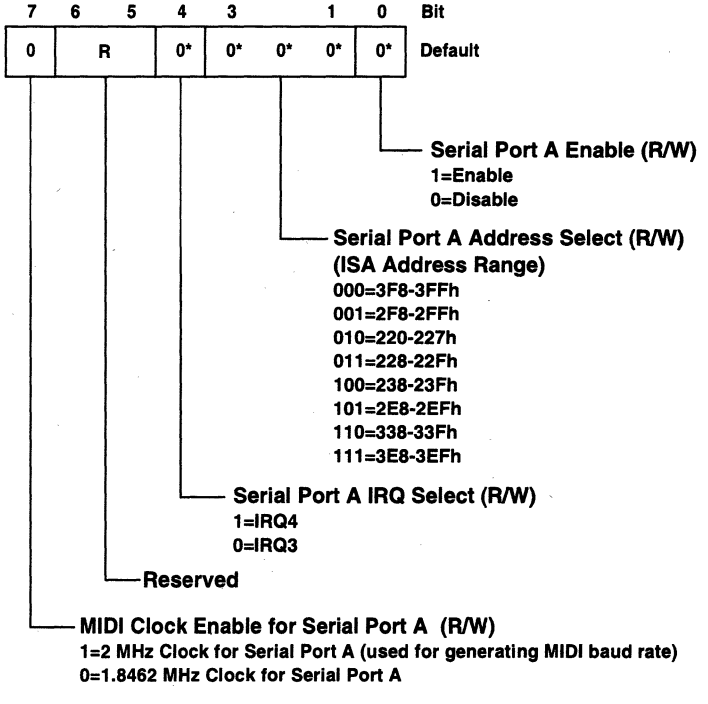
4.1.10 SACFG1—SERIAL PORT A CONFIGURATION REGISTER

Index Address: 30h
Default Value: 0RR0 0000
Attribute: Read/Write
Size: 8 bits

The SACFG1 register enables/disables Serial Port A, selects the Serial Port A address range, and selects between IRQ3 and IRQ4 as the Serial Port A interrupt. This register also selects the appropriate clock frequency for use with MIDI.

NOTES:

1. Through programming of this register and the SBCFG1 Register, the 82091AA permits serial ports A and B to be configured for the same interrupt assignment. However, software must take care in responding to interrupts correctly.
2. It is possible to enable and assign both serial ports to the same address through software. In this configuration, the 82091AA disables serial port B, but does not set serial port B into it's powerdown condition. Although this is a safe configuration for the 82091AA, it is not power conservative and is not recommended.



NOTE:
*Default shown is for SWMB and SWAI hardware configuration modes. For HWB and HWE modes, the default is determined by hardware strapping options as described in Section 4.2, Hardware Configuration.

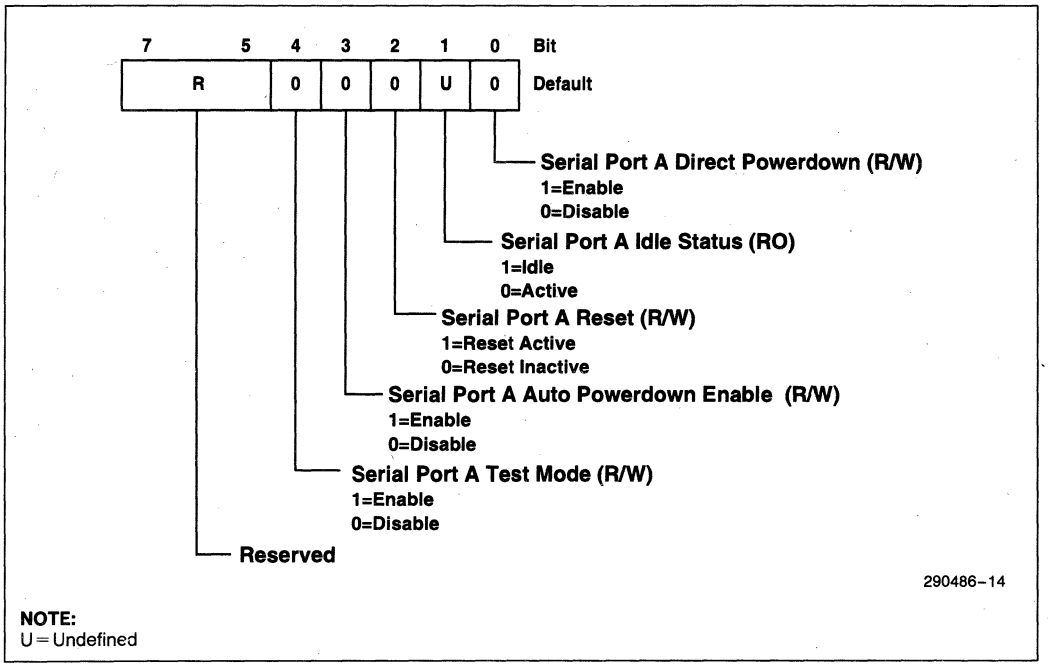
Figure 13. Serial Port A Configuration Register

Bit	Description
7	**MIDI CLOCK FOR SERIAL PORT A ENABLE (SAMIDI):** When SAMIDI = 1, the clock into Serial Port A is changed from 1.8462 MHz–2 MHz. The 2 MHz clock is needed to generate the MIDI baud rate. When SAMIDI = 0, the clock frequency is 1.8462 MHz.
6:5	**RESERVED**
4	**SERIAL PORT A IRQ SELECT (SAIRQSEL):** When SAIRQSEL = 0, IRQ3 is selected for the Serial Port A interrupt. When SAIRQSEL = 1, IRQ4 is selected for the Serial Port A interrupt. This bit can be configured by strapping options at powerup for HWB and HWE modes only. For SWMB and SWAI hardware configuration modes, the default is 0 (IRQ3). Note that, while the default address and IRQ assignments for SWMB and SWAI modes are the same for both serial ports, the serial ports are disabled and programming of this register is required for operation.
3:1	**SERIAL PORT A ADDRESS SELECT (SAADS):** This field selects the ISA address range for Serial Port A as follows: **Bits[3:1] ISA Address Range** 0 0 0 3F8–3FFh 0 0 1 2F8–2FFh 0 1 0 220–227h 0 1 1 228–22Fh 1 0 0 238–23Fh 1 0 1 2E8–2EFh 1 1 0 338–33Fh 1 1 1 3E8–3EFh This field can be configured by strapping options at powerup for HWB and HWE modes only. For SWMB and SWAI hardware configuration modes, the default is 000 (3F8–3FFh). Note that, while the default address and IRQ assignments for SWMB and SWAI modes are the same for both serial ports, the serial ports are disabled and programming of this register is required for operation.
0	**SERIAL PORT A ENABLE (SAEN):** When SAEN = 1, Serial Port A is enabled. When SAEN = 0, Serial Port A is disabled. This bit can be configured by strapping options at powerup for HWB and HWE modes only. For SWMB and SWAI hardware configuration modes, the default is 0 (disabled).

4.1.11 SACFG2—SERIAL PORT A POWER MANAGEMENT AND STATUS REGISTER

Index Address: 31h
Default Value: RRR0 00U0
Attribute: Read/Write
Size: 8 bits

This register enables/disables the Serial Port A module auto powerdown and can place the module into a direct powerdown mode. The register also provides Serial Port A idle status, resets the Serial Port A module, and places Serial Port A into test mode.



NOTE:
U = Undefined

Figure 14. Serial Port A Power Management and Status Register

Bit	Description
7:5	**RESERVED**
4	**SERIAL PORT A TEST MODE (SATEST):** The serial port test mode provides user access to the output of the baud out generator. When SATEST = 1 (and the DLAB bit is 1 in the LCR), the Serial Port A test mode is enabled and the baud rate clock is output on the SOUTA pin (Figure 15). When SATEST = 0, the Serial Port A test mode is disabled.

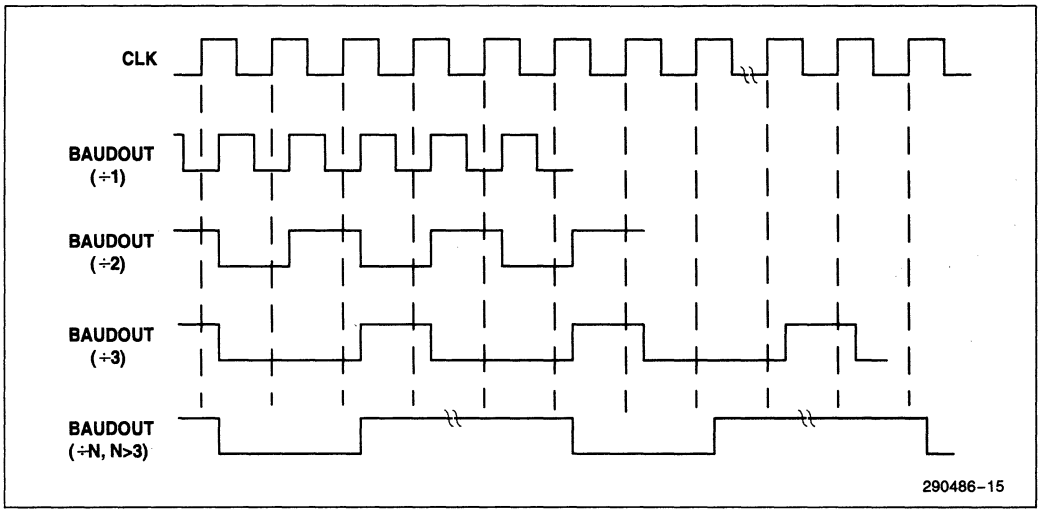


Figure 15. Test Mode Output (SOUTA and SOUTB)

Bit	Description
3	**SERIAL PORT A AUTO POWERDOWN ENABLE (SAAPDN):** This bit enables/disables auto powerdown. When SAAPDN = 1, Serial Port A can enter auto powerdown if the required conditions are met. The required conditions are that the transmit and receive FIFOs are empty and the timeout counter has expired. When SAAPDN = 0, auto powerdown is disabled.
2	**SERIAL PORT A RESET (SARESET):** When SARESET = 1, the Serial Port A module is reset (i.e. all programming and current state information is lost). This is the same state the module would be in after a hard reset (RSTDRV asserted). When resetting the serial port via this configuration bit, the software must toggle this bit and ensure the reset active time (SARESET = 1) of 1.13 μs minimum is met.
1	**SERIAL PORT A IDLE STATUS (SAIDLE):** When Serial Port A is in an idle state the 82091AA sets this bit to 1. Serial Port A is in the idle state when the transmit and receive FIFOs are empty and the timeout counter has expired. Note that these are the same conditions that apply to entering auto powerdown. When serial port A is not in an idle state, the 82091AA sets this bit to 0. Direct powerdown does not affect this bit and in auto powerdown SAIDLE is only set to a 1 if the receive and transmit FIFOs are empty. This bit is read only. During a hard reset (RSTDRV asserted), The 82091AA sets SAIDLE to 0. However, because the serial port is typically initialized by software before the idle conditions are met, the default state is shown as undefined.
0	**SERIAL PORT A DIRECT POWERDOWN (SADPDN):** When SADPDN = 1, Serial Port A is placed in direct powerdown mode. Setting this bit to 0 brings Serial Port A out of direct powerdown mode. Setting bit 2 (SARESET) of this register to 1 will also bring Serial Port A out of the direct powerdown mode. **NOTE:** Direct powerdown resets the receiver and transmitter portions of the serial port including the receive and transmit FIFOs. To ensure that the resetting of the FIFOs does not cause data loss, the SAIDLE bit should be 1 before placing the serial port into direct powerdown.

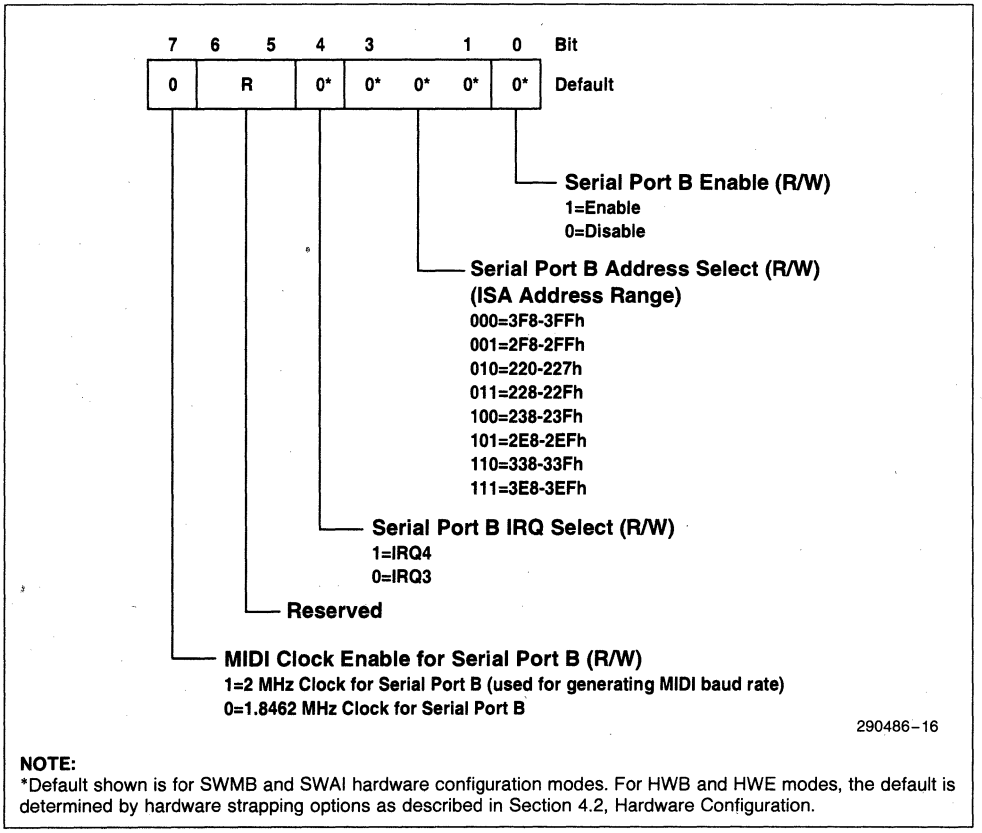
4.1.12 SBCFG1—SERIAL PORT B CONFIGURATION REGISTER

Index Address: 40h
Default Value: 0RR0 0000
Attribute: Read/Write
Size: 8 bits

The SBCFG1 register enables/disables Serial Port B, selects the Serial Port B address range, and selects between IRQ3 and IRQ4 as the Serial Port B interrupt. This register also selects the appropriate clock frequency for use with MIDI.

NOTES:

1. Through programming of this register and the SBCFG1 Register, the 82091AA permits serial ports A and B to be configured for the same interrupt assignment. However, software must take care in responding to interrupts correctly.
2. It is possible to enable and assign both serial ports to the same address through software. In this configuration, the 82091AA disables serial port B, but does not set serial port B into it's powerdown condition. Although this is a safe configuration for the 82091AA, it is not power conservative and is not recommended.



NOTE:
*Default shown is for SWMB and SWAI hardware configuration modes. For HWB and HWE modes, the default is determined by hardware strapping options as described in Section 4.2, Hardware Configuration.

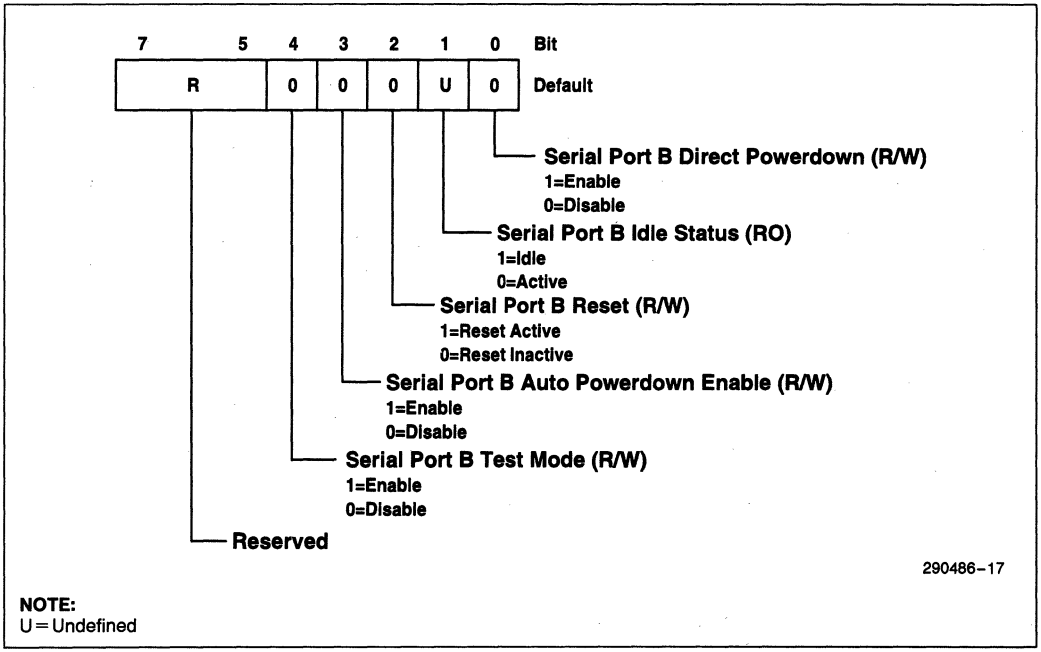
Figure 16. Serial Port B Configuration Register

Bit	Description
7	**MIDI CLOCK FOR SERIAL PORT B ENABLE (SBMIDI):** When SBMIDI = 1, the clock into Serial Port B is changed from 1.8462 MHz to 2 MHz. The 2 MHz clock is needed to generate the MIDI baud rate. When SBMIDI = 0, the clock frequency is 1.8462 MHz. The default value is 0.
6:4	**RESERVED**
4	**SERIAL PORT B IRQ SELECT (SBIRQSEL):** When SBIRQSEL = 0, IRQ3 is selected for the Serial Port B interrupt. When SBIRQSEL = 1, IRQ4 is selected for the Serial Port B interrupt. The default value is 0. This bit can be configured by strapping options at powerup for HWB and HWE modes only. For SWMB and SWAI configuration modes, the default is 0 (IRQ3). Note that, while the default address and IRQ assignments for SWMB and SWAI modes are the same for both serial ports, the serial ports are disabled and programming of this register is required for operation.
3:1	**SERIAL PORT B ADDRESS SELECT (SBADS):** This field selects the ISA address range for Serial Port B as follows: **Bits[3:1] ISA Address Range** 0 0 0 3F8-3FFh 0 0 1 2F8-2FFh 0 1 0 220-227h 0 1 1 228-22Fh 1 0 0 238-23Fh 1 0 1 2E8-2EFh 1 1 0 338-33Fh 1 1 1 3E8-3EFh This field can be configured by strapping options at powerup for HWB and HWE modes only. For SWMB and SWAI configuration modes, the default is 000 (3F8-3FFh). Note that, while the default address and IRQ assignments for SWMB and SWAI modes are the same for both serial ports, the serial ports are disabled and programming of this register is required for operation.
0	**SERIAL PORT B ENABLE (SBEN):** When SBEN = 1, Serial Port B is enabled. When SAEN = 0, Serial Port B is disabled. This bit can be configured by strapping options at powerup for HWB and HWE modes only. For SWMB and SWAI configuration modes, the default is 0 (disabled).

4.1.13 SBCFG2—SERIAL PORT B POWER MANAGEMENT AND STATUS REGISTER

Index Address: 41h
Default Value: RRR0 00U0
Attribute: Read/Write
Size: 8 bits

This register enables/disables the Serial Port B module auto powerdown and can place the module into a powerdown mode directly. The register also provides Serial Port B idle status, resets the Serial Port B module, and enables/disables Serial Port B test mode.



NOTE:
U = Undefined

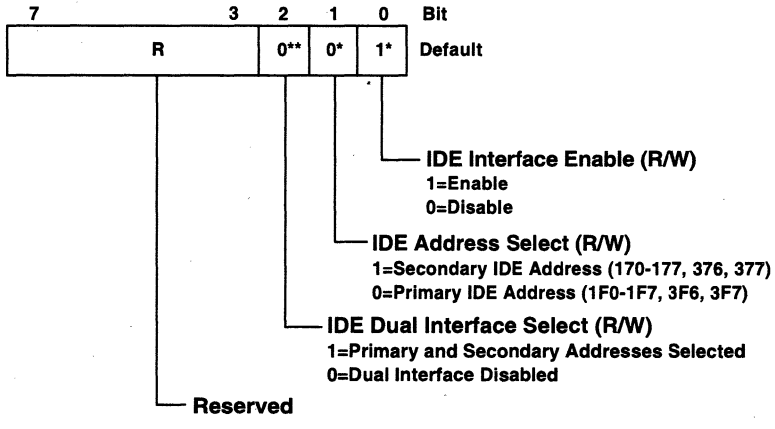
Figure 17. Serial Port B Power Management and Status Register

Bit	Description
7:5	**RESERVED**
4	**SERIAL PORT B TEST MODE (SBTEST):** The serial port test mode provides user access to the output of the baud out generator. When SBTEST = 1 (and the DLAB bit is 1 in the LCR), the Serial Port B test mode is enabled and the baud rate clock is output on the SOUTB pin (Figure 15). When SBTEST = 0, the Serial Port B test mode is disabled.
3	**SERIAL PORT B AUTO POWERDOWN ENABLE (SBAPDN):** This bit enables/disables auto powerdown. When SBAPDN = 1, Serial Port B can enter auto powerdown if the required conditions are met. The required conditions are that the transmit and receive FIFOs are empty and the timeout counter has expired. When SBAPDN = 0, auto powerdown is disabled.
2	**SERIAL PORT B RESET (SBRESET):** When SBRESET = 1, Serial Port B is reset (i.e., all programming and current state information is lost). This is the same state the module would be in after a hard reset (RSTDRV asserted). When resetting the serial port via this configuration bit, the software must toggle this bit and ensure the reset active time (SBRESET = 1) of 1.13 μs minimum is met.
1	**SERIAL PORT B IDLE STATUS (SBIDLE):** When Serial Port B is in an idle state the 82091AA sets this bit to 1. Serial Port B is in the idle state when the transmit and receive FIFOs are empty and the timeout counter has expired. Note that these are the same conditions that apply to entering auto powerdown. When serial port B is not in an idle state, the 82091AA sets this bit to 0. Direct powerdown does not affect this bit and in auto powerdown, this bit is only set to a 1 if the receive and transmit FIFOs are empty. This bit is read only. During a hard reset (RSTDRV asserted), the 82091AA sets this bit to 0. However, because the serial port is typically initialized by software before the idle conditions are met, the defaullt state is shown as undefined.
0	**SERIAL PORT B DIRECT POWERDOWN (SBDPDN):** When SBDPDN = 1, Serial Port B is placed in powerdown mode. Setting this bit to 0 brings the module out of direct powerdown mode. Setting bit 2 (SBRESET) of this register to 1 will also bring Serial Port B out of the direct powerdown mode. **NOTE:** Direct powerdown resets the receiver and transmitter portions of the serial port including the receive and transmit FIFOs. To ensure that the resetting of the FIFOs does not cause data loss, the SBIDLE bit should be 1 before placing the serial port into direct powerdown.

4.1.14 IDECFG—IDE CONFIGURATION REGISTER

Index Address: 50h
Default Value: RRRR R001
Attribute: Read/Write
Size: 8 bits

The IDECFG Register sets up the 82091AA IDE interface. This register enables the IDE interface and selects the address for accessing the IDE.



NOTES:
* Default shown is for SWMB and SWAI configuration modes. For HWB and HWE hardware configuration modes, the default is determined by hardware strapping options as described in Section 4.2, Hardware Configuration.
** Not hardware configurable.

Figure 18. IDE Configuration Register

Bit	Description
7:3	**RESERVED**
2	**IDE DUAL SELECT (IDUAL):** When IDUAL = 0, the IDE address selection is determined by the IADS bit. When IDUAL = 1, both the primary and secondary IDE addresses are selected and the setting of the IADS bit does not affect IDE address selection.
1	**IDE ADDRESS SELECT (IADS):** When IADS = 0, the primary IDE address is selected (1F0h–1F7h, 3F6h, 3F7h). When IADS = 1, the secondary IDE address is selected (1F0h–1F7h, 376h, 377h). For all hardware configuration modes (SWMB, SWAI, HWB, and HWE), the default is determined by signal pin strapping options.
0	**IDE INTERFACE ENABLE (IEN):** When IEN = 0, the IDE interface is disabled (i.e., the IDE chip selects (IDECS[1:0]), DEN#, and HEN# are negated (remain inactive) for accesses to the IDE primary and secondary addresses). When IEN = 1, the IDE interface is enabled. For all hardware configuration modes (SWMB, SWAI, HWB, and HWE), the default is determined by signal pin strapping options.

4.2 Hardware Configuration

Hardware configuration provides a mechanism for configuring certain 82091AA operations at powerup. Four hardware configuration modes provide different levels of configuration depending on the type of application and the degree of hardware/software configuration desired. The hardware configuration modes are:

- Software Motherboard (SWMB)
- Software Add-In (SWAI)
- Hardware Extended (HWE)
- Hardware Basic (HWB)

These modes support a variety of system implementations. For example, with Hardware Basic (HWB) and Hardware Extended (HWE) modes, an extensive set of 82091AA configuration options are available for setting up the 82091AA at powerup. This permits the 82091AA to be used in systems without 82091AA software drivers. For many of these systems, access to the 82091AA configuration registers may not be necessary. As such, access to these registers can be disabled via hardware configuration. This option could be used to prevent software from inadvertently re-configuring the 82091AA.

NOTE:
If the 82091AA is configured in HWB or HWE configuration mode at powerup, and reconfiguration with software is desired, the 82091AA configuration mode must first be changed to SWAI configuration mode by writing the AIPCFG1 register. The 82091AA can then remain in SWAI configuration mode to accomodate software programmable configuration changes as desired.

Software Motherboard (SWMB) and Software Add-In (SWAI) modes provide a minimum hardware configuration in systems where software/firmware drivers are used for configuration. Because access to the 82091AA configuration registers after powerup/hardware configuration is needed, the SWMB and SWAI modes do not provide disabling access to these registers (i.e., the strapping of the HEN# signal has no effect).

The desired hardware configuration mode and options within the mode are selected by strapping certain 82091AA signal pins at powerup. These signal pins are sampled when the 82091AA receives a hard reset (via RSTDRV). This section describes how to select the configuration mode and options within the mode. The section also provides example hardware connection diagrams for the different modes.

4.2.1 SELECTING THE HARDWARE CONFIGURATION MODE

During powerup or a hard reset, four signal pins (DEN#, PPDIR/GCS#, DTRA, and HEN#) select the hardware configuration mode, I/O address assignment for the 82091AA configuration registers, and whether software access to these configuration registers is permitted. The following mnemonics and signal pins are assigned for these functions:

CFGMOD[1,0] **Hardware Configuration Mode.** The 82091AA samples the CFGMOD0 (DEN#) and CFGMOD1 (PPDIR/GCS#) signal pins to select one of the four hardware configuration modes as shown in Table 6.

CFGADS **82091AA Configuration Register Address Assignment.** The 82091AA samples the DTRA# signal (CFGADS function) to determine the address assignment of the 82091AA configuration registers as shown in Table 6. CFGADS works in conjunction with CFGDIS. Note that the 82091AA configuration register address assignment for Hardware Basic mode is not selectable.

CFGDIS **82091AA Configuration Register Disable.** The 82091AA samples CFGDIS (HEN# signal) to enable/disable access to the 82091AA configuration registers as shown in Table 6. Note that CFGDIS only affects the HWE and HWB modes.

NOTE:
For Extended Hardware Configuration, the time immediately following the RSTDRV pulse is required to complete the configuration time. If IORC#/IOWC# are asserted during this time, IOCHRDY will be negated (wait-states inserted) until the 82091AA configuration time expires.

Table 6. AIP Configuration Mode Register Address Assignment

CFGDIS (HEN#)	CFGMOD1 (PPDIR)	CFGMOD0 (DEN#)	CFGADS (DTRA#)	Configuration Mode	Configuration Register ISA Address (INDEX/TARGET)
X	0	0	0	SWMB	22h/23h
X	0	0	1	SWMB	24h/25h
X	0	1	0	SWAI	26Eh/26Fh
X	0	1	1	SWAI	398h/399h
0	1	0	0	HWE	26Eh/26Fh
0	1	0	1	HWE	398h/399h
1	1	0	X	HWE	Access Disabled
0	1	1	n/a	HWB	398h/399h
1	1	1	n/a	HWB	Access Disabled

4.2.2 SELECTING HARDWARE CONFIGURATION MODE OPTIONS

Within each hardware configuration mode, a number of options are available. For the HWB and HWE hardware configuration modes, the user can enable/disable the floppy disk controller and the IDE interface via the IDE chip select pins (see Table 7). If enabled, these signal pins also select the address assignment. For SWMB and SWAI configuration modes, these signal pins have no effect.

Table 7. FDC and IDE Enable/Disable

DDCFG1 (IDECS1#)	DDCFG0 (IDECS0#)	Floppy Disk Controller	IDE
0	0	Disable	Disable
0	1	Enabled (3F6–3F7h; Primary)	Disable
1	0	Enabled (370–377h; Secondary)	Enabled (170–177h; Secondary)
1	1	Enabled (3F6–3F7h; Primary)	Enabled (1F0–1F7h; Primary)

The 82091AA provides additional hardware configuration options through the SOUTA, SOUTB, RTSA#, RTSB#, DTRA#, and DTRB# signal pins as shown in Table 8. In the case of the Hardware Extended Mode, the 82091AA samples the signal pins at two different times (once for HWEa options and again for HWEb options). The timing for signal sampling is discussed in Section 4.2.3, Hardware Configuration Timing Relationships. The options provide configuration of the serial ports, floppy disk controller, parallel port, IDE interface, 82091AA operating power supply voltage, 82091AA clock frequency, and address assignment for the 82091AA configuration registers. Table 8 provides a matrix of the options available for each hardware configuration mode. The configuration options are selected as shown in Table 8 through Table 14.

Note that for the SWAI and SWMB modes, the selection of the operating frequency (CLKSEL), power supply voltage level (VSEL), and 82091AA configuration register address assignment (CFGADS) are the only hardware configuration options (Table 8). In these modes, software/firmware provides the remainder of the 82091AA configuration by programming the 82091AA configuration registers (see Section 4.1, Configuration Registers). For the SWAI and SWMB modes, the 82091AA modules are placed in the following states after powerup or a hard reset:

- Serial ports disabled
- Parallel port disabled
- FDC enabled for two drives (primary address)
- IDE enabled (primary address)

Table 8. Hardware Configuration Mode Option Matrix

Signal Name	Basic Hardware Configuration	Extended Hardware Configuration		Software Add-In Configuration	Software MotherBoard Configuration
	HWB	HWEa	HWEb	SWAI	SWMB
SOUTA	SPCFG0	CLKSEL(3)	SPCFG0	CLKSEL(3)	CLKSEL(3)
SOUTB	SPCFG1	PPMOD0	SPCFG1	—	—
RTSA#	SPCFG2	PPMOD1	SPCFG2	—	—
RTSB#	SPCFG3	FDDQTY	SPCFG3	—	—
DTRA#	PPCFG0	CFGADS	PPCFG0	CFGADS	CDGADS
DTRB#	PPCFG1	VSEL	PPCFG1	VSEL	VSEL

NOTES:
1. HWEa and HWEb reference the switching banks shown in Figure 22.
2. The following mnemonics are used in the table: SPCFGx = serial port configuration, PPCFGx = parallel port configuration, CLKSEL = clock select, PPMODx = parallel port hardware mode, FDDQTY = floppy disk drive quantity, VSEL = power supply voltage select, CFGADS = 82091AA configuration register address assignment select.
3. Always tie this signal low with a 10K resistor.

Table 9. Serial Port Address and Interrupt Assignments

SPCFG3 (RTSB#)	SPCFG2 (RTSA#)	SPCFG1 (SOUTB)	SPCFG0 (SOUTA)	Serial Port B		Serial Port A	
				Address Assignment	Interrupt Assignment	Address Assignment	Interrupt Assignment
0	0	0	0	Disable	—	Disable	—
0	0	0	1	Disable	—	3F8–3FFh	IRQ4
0	0	1	0	Disable	—	2F8–2FFh	IRQ3
0	0	1	1	Disable	—	3E8–3EFh	IRQ4
0	1	0	0	3F8–3FFh	IRQ4	Disable	—
0	1	0	1	3E8–3EFh	IRQ4	Disable	—
0	1	1	0	3F8–3FFh	IRQ4	2F8–2FFh	IRQ3
0	1	1	1	3F8–3FFh	IRQ4(1)	3E8–3EFh	IRQ4(1)
1	0	0	0	2F8–2FFh	IRQ3	Disable	—
1	0	0	1	2F8–2FFh	IRQ3	3F8–3FFh	IRQ4
1	0	1	0	Disable	—	2E8–2EFh	IRQ3
1	0	1	1	2F8–2FFh	IRQ3	3E8–3EFh	IRQ4
1	1	0	0	2E8–2EFh	IRQ3	Disable	—
1	1	0	1	2E8–2EFh	IRQ3	3F8–3FFh	IRQ4
1	1	1	0	2E8–2EFh	IRQ3(1)	2F8–2FFh	IRQ3(1)
1	1	1	1	2E8–2EFh	IRQ3	3E8–3EFh	IRQ4

NOTE:
1. In this configuration, the two serial ports share the same interrupt line. Responding correctly to interrupts generated in this configuration is the exclusive responsibility of software.

Table 10. Parallel Port Address and Interrupt Assignments

PPCFG1 (DTRB#)	PPCFG0 (DTRA#)	Parallel Port Address Assignment	Parallel Port Interrupt Assignment
0	0	Disable	—
0	1	378–37Fh	IRQ7
1	0	278–27Fh	IRQ5
1	1	3BC–3BFh	IRQ7

Table 11. Parallel Port Hardware Mode Select

PPMOD1 (RTSA#)	PPMOD0 (SOUTB)	Mode
0	0	ISA-Compatible
0	1	PS/2-Compatible
1	0	EPP
1	1	Reserved

NOTES:
1. PPMODx hardware configuration is effective in HWE mode only.
2. ECP mode is not selectable via hardware configuration.
3. For EPP mode, address assignment must be either 278h or 378h.

Table 12. AIP Clock Select

CLKSEL (SOUTA)	
0	24 MHz

NOTE:
Always tie this low.

Table 13. AIP Power Supply Voltage

VSEL (DTRB#)	Power Supply Voltage
0	5.0V Operation
1	3.3V Operation

NOTES:
1. VSEL hardware configuration is not available in HWB mode only.
2. To operate the 82091AA and all of the interfaces at 5V or 3.3V, both V_{CC} and V_{CCF} are connected to 5V or 3.3V power supplies, respectively. However, in the mixed mode, hardware configuration (V_{SEL}) is set to 3.3V, V_{CC} is connected to 3.3V, and V_{CCF} connected to 5V.
3. 3.3V operation is available only in the 82091AA.

Table 14. Floppy Drive Quantity Select

FDDQTY (RTSB#)	Number of Supported Floppy Drives
0	2 Floppy Drives
1	4 Floppy Drives

NOTES:
1. FDDQTY hardware configuration is effective in HWE mode only.
2. Four floppy drive support requires external logic to decode.

4.2.3 HARDWARE CONFIGURATION TIMING RELATIONSHIPS

The 82091AA samples all of the hardware configuration signals on the high-to-low transition of RSTDRV. For the HWB, SWMB, and SWAI modes, the 82091AA completes hardware configuration on this sampling (Figure 19). For HWE mode, the 82091AA samples some of the signals twice (Figure 20). The first sampling occurs on the high-to-low transition of RSTDRV. As Figure 22 shows (see Section 4.2.5, Extended Hardware Configuration Mode), the HC367 tri-states its outputs when RSTDRV is negated. This permits the strapping options from the HWEb block to be sampled. A short time after RSTDRV is negated (the time is specified in Section 11.0, Electrical Characteristics), the 82091AA samples the SOUTA, RTSA#, DTRA#, SOUTB, RTSB#, and DTRB# signals.

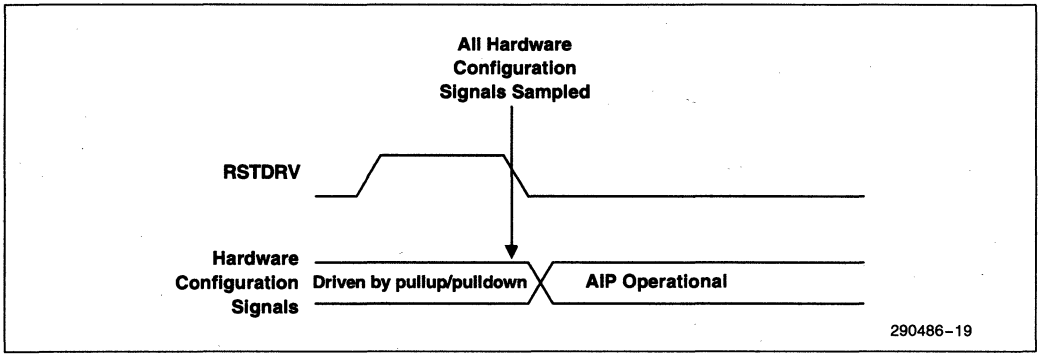


Figure 19. HWB, SWMB, and SWAI Hardware Configuration Mode Timing

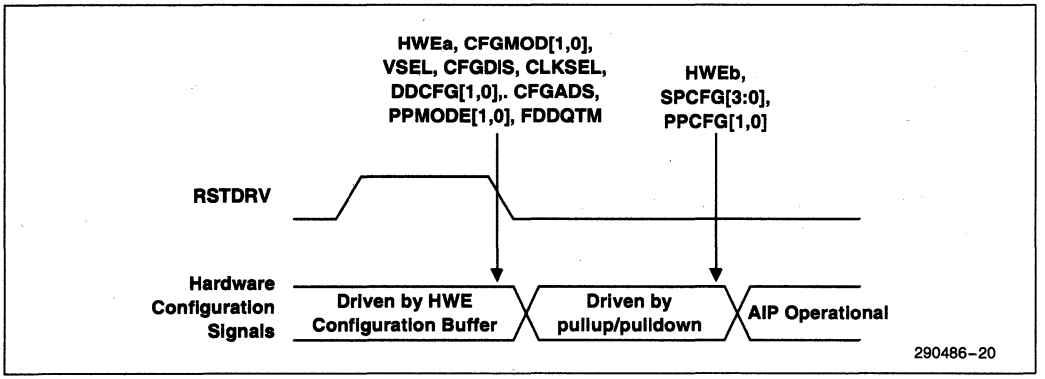


Figure 20. HWE Hardware Configuration Mode Timing

4.2.4 HARDWARE BASIC CONFIGURATION

The Hardware Basic configuration mode permits the user to assign addresses to the serial ports and parallel ports. This is achieved by sampling several of the serial port connections at the end of a hardware reset. The PPDIR/GCS# signal defaults to game port chip select output (GCS#). The 82091AA power supply voltage is not selectable in this mode and is fixed at 5V. The parallel port mode is set to ISA-Compatible. In addition, the FDC floppy drive support is set at two floppy drives. If configuration register access is enabled, the access address is fixed at 398h/399h. To reconfigure the 82091AA using software, the 82091AA configuration mode must be changed to SWAI mode (refer to AIPCFG1 register). Figure 21 shows the implementation of a basic hardware configuration.

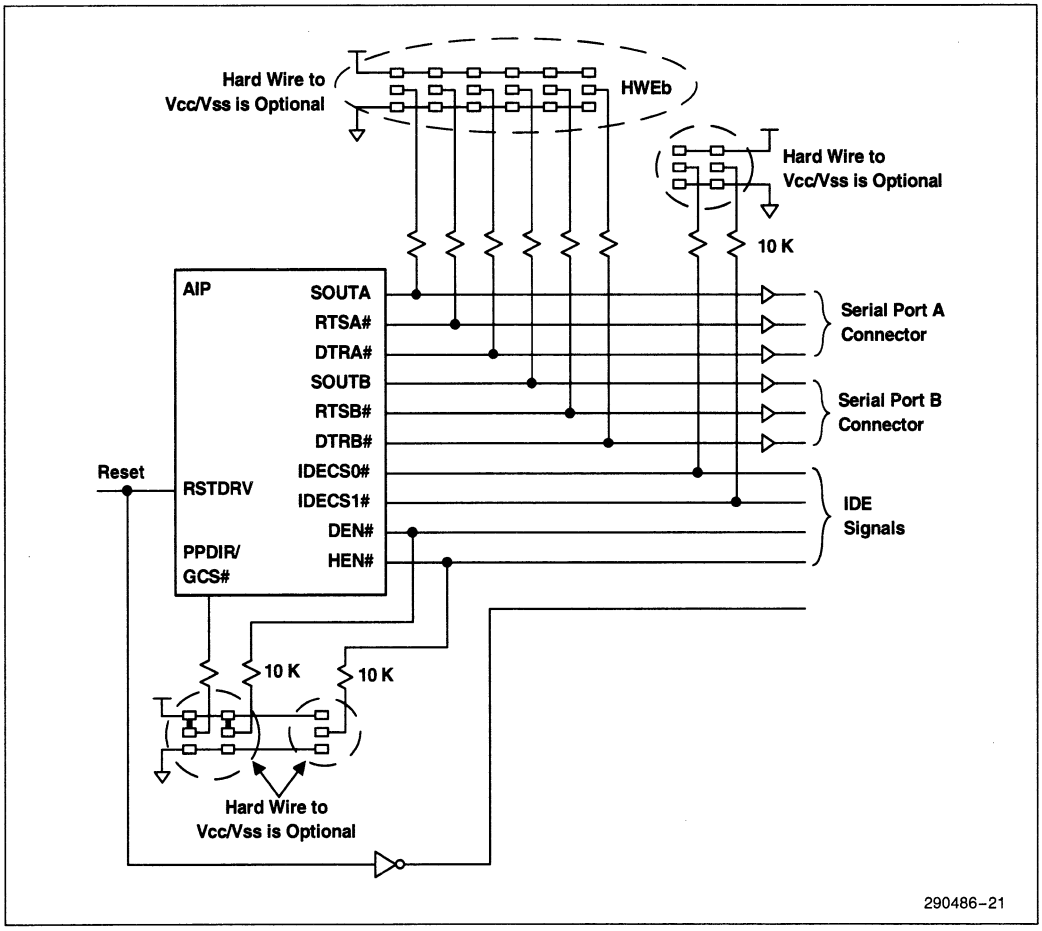


Figure 21. Hardware Basic Configuration

4.2.5 HARDWARE EXTENDED CONFIGURATION MODE

The Hardware Extended configuration mode provides all of the features of the Hardware Basic configuration mode. Additional features in Hardware Extended configuration permit the user to select quantity of floppy drives can be selected for either 2 or 4 floppy drive support. The 82091AA operating voltage is selectable between 3.3V* and 5V. In addition, the parallel port can be configured to operate in ISA-Compatible, PS/2-Compatible, or EPP modes. Hardware extended configuration provides these additional hardware configuration options by sampling the pins on the serial ports at two different times. When RSTDRV is asserted, the HC367 drives the values on SOUTA, RTSA#, DTRA#, SOUTB, RTSB#, and DTRB# (Figure 22). When RTSDRV is negated, the HC367 is disabled and these serial port signals are driven by HWEb pullup/down resistors. The PPDIR/GCS# signal defaults to a game port chip select (GCS#). To reconfigure the 82091AA using software, the 82091AA configuration mode must be changed to SWAI mode (refer to AIPCFG1 register).

NOTE:
*3.3V operation is only available in the 82091AA.

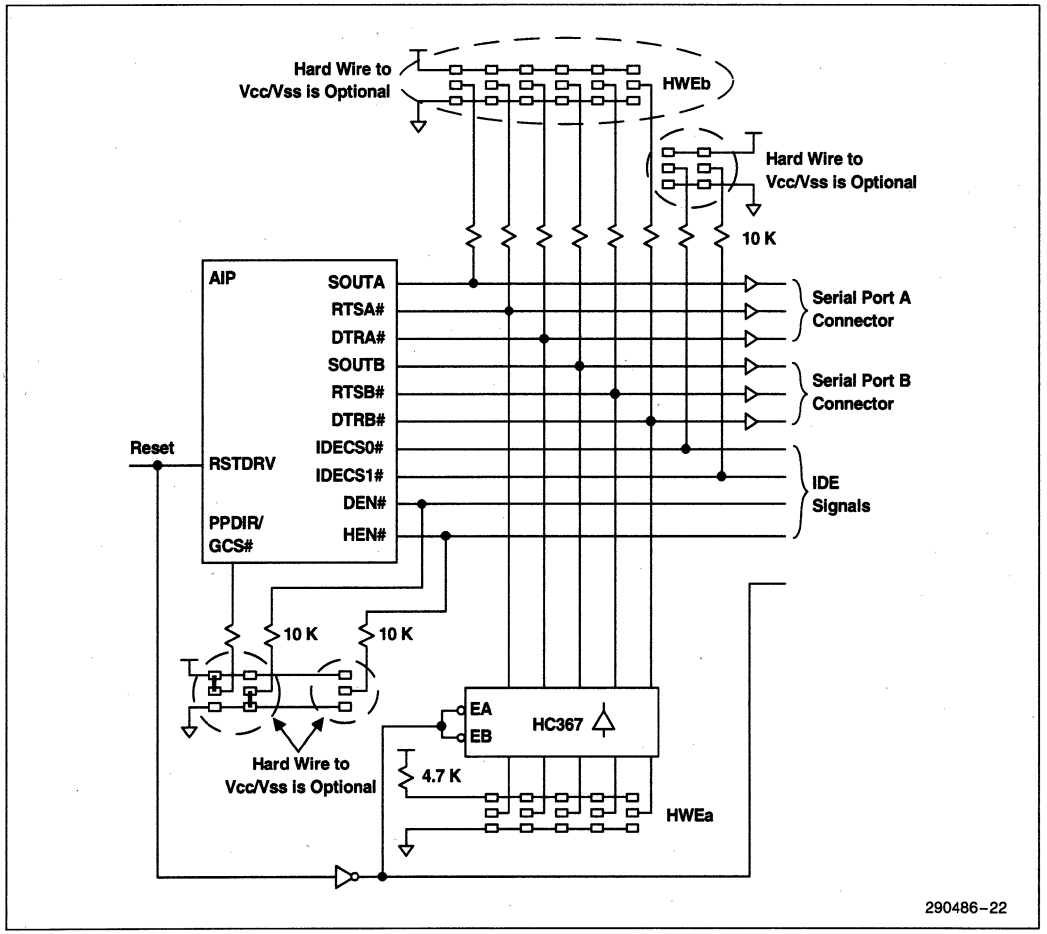


Figure 22. Hardware Extended Configuration

4.2.6 SOFTWARE ADD-IN CONFIGURATION

The Software Add-in configuration mode permits the user to assign the address for the 82091AA configuration registers, and select the power supply voltage for the 82091AA. The 82091AA configuration registers are accessible. The registers are located in the ISA Bus I/O address space and can be selected to be at either 398h/399h or 26Eh/26Fh. The PPDIR/GCS# signal defaults to a game port chip select (GCS#).

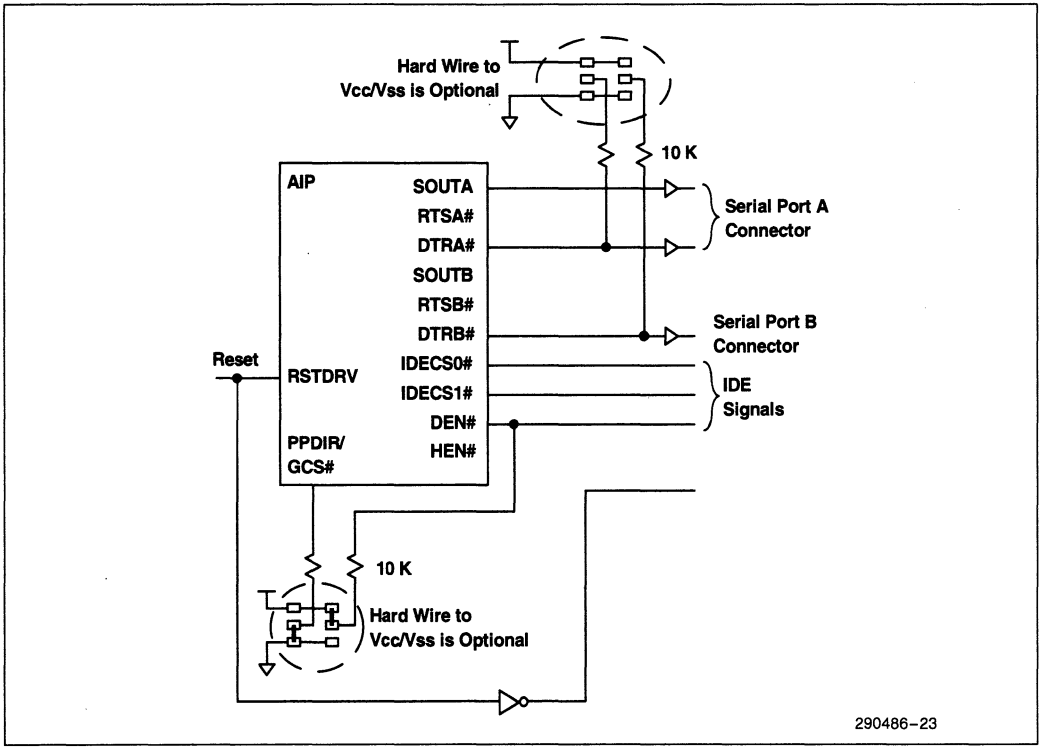


Figure 23. Software Add-In Configuration

4.2.7 SOFTWARE MOTHERBOARD CONFIGURATION

The Software Motherboard configuration mode permits the 82091AA to be located on the motherboard. In this mode, the 82091AA configuration registers are accessible via the X-Bus I/O address space and can be selected to be at either 22h/23h or 24h/25h. In addition, the user selects the power supply voltage for the 82091AA. The PPDIR/GCS# signal defaults to a Parallel Port Direction Control Output (PPDIR).

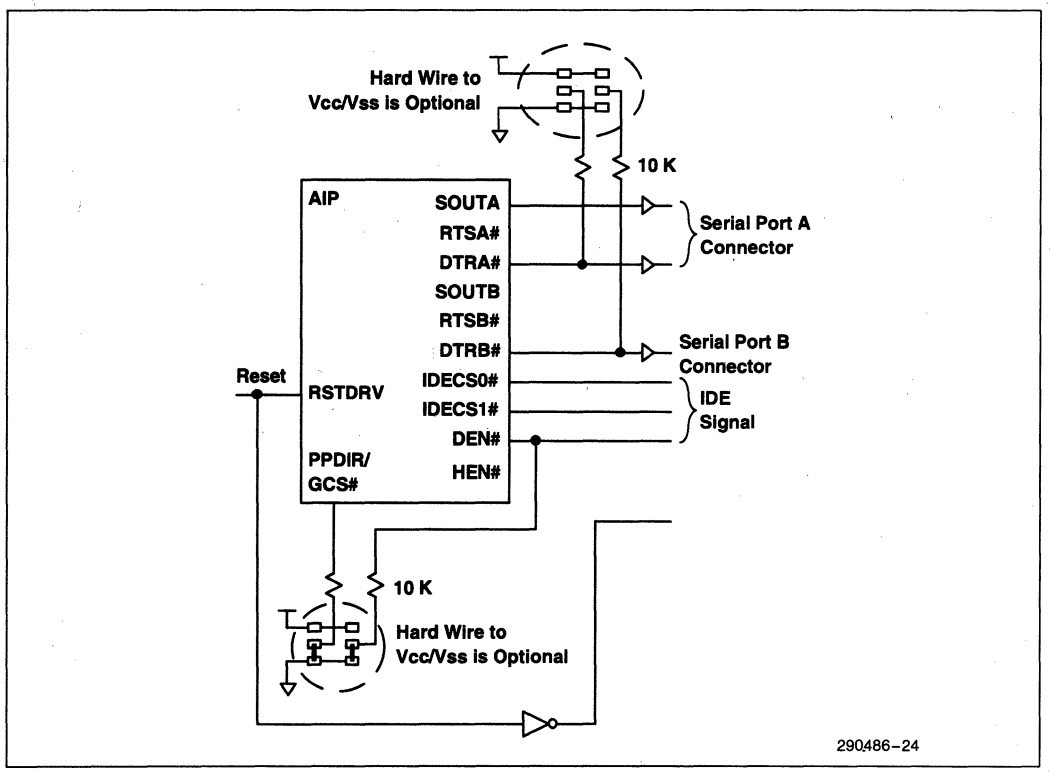


Figure 24. Software Motherboard Hardware Configuration

5.0 HOST INTERFACE

The 82091AA host interface is an 8-bit direct-drive (24 mA) ISA Bus/X-Bus interface that permits the CPU to access its registers through read/write operations in I/O space. These registers may be accessed by programmed I/O and/or DMA bus cycles. With the exception of the IDE Interface, all functions on the 82091AA require only 8-bit data accesses. The 16-bit access required for the IDE Interface is supported through the appropriate chip selects and data buffer enables from the 82091AA. The 82091AA does not participate in 16-bit IDE DMA transfers.

Although the 82091AA has an ISA/X-Bus host interface, there are a few features that differentiate it from conventional ISA/X-Bus peripherals. These features are as follows:

- **Internal, Configurable Chip Select Decode Logic.** SA[9:0] allow full decoding of the ISA I/O address space such that the functional modules contained in the 82091AA can be relocated to the desired I/O address. This feature can be used to resolve potential system configuration conflicts.
- **IOCHRDY for ISA Cycle Extension.** During certain I/O cycles to the parallel port controller in the 82091AA, it is necessary to extend the current bus cycle to match the access time of the device connected to the Parallel Port. The IOCHRDY signal is used by the 82091AA to extend ISA Bus cycles, as needed, according to the ISA protocol. IOCHRDY overrides all other strobes that attempt to shorten the bus cycle.
- **NOWS# for 3 BCLK I/O Cycles.** All programmed I/O accesses to 82091AA registers can be completed in a total of 3 BCLK cycles. This is possible because the 82091AA register access times have been minimized to allow data transfers to occur with shortened read/write control strobes. As a result, the 82091AA is well suited for use in embedded control designs that use an asynchronous microprocessor interface without any particular reference to ISA cycle timings.
- **DMA Transfers:** The 82091AA supports DMA compatible, type A, type B and type F DMA cycles. Some newer system DMA controllers are capable of generating fast DMA cycles (type F) on all DMA channels. If such a controller is used in conjunction with the 82091AA, it will be possible to accomplish a DMA transfer in 2 BCLKs.

The 82091AA ISA data lines (SD[7:0]) can be connected directly to the ISA Bus. If external buffers are used to isolate the SD[7:0] signals from the 240 pF loading of the ISA Bus, the DEN# signal can be used to control the external buffers as shown in Figure 25.

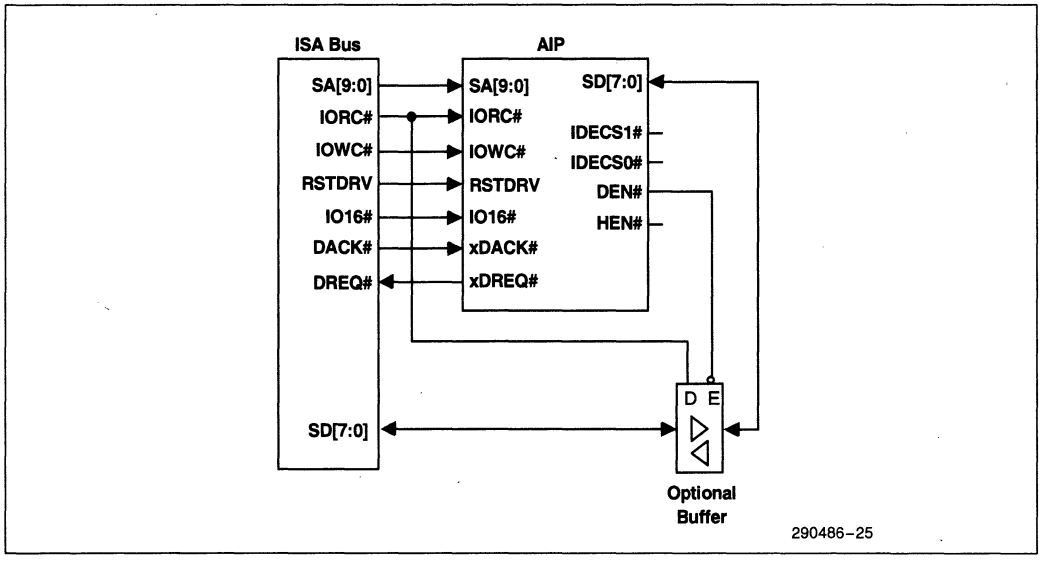


Figure 25. ISA Interface (with Optional Data Buffer)

6.0 PARALLEL PORT

The 82091AA parallel port can be configured for four parallel port modes. These parallel port modes and the associated parallel interface protocols are:

Parallel Port Mode	Parallel Interface Protocol
ISA-Compatible Mode	Compatibility, Nibble
PS/2-Compatible Mode	Byte
EPP Mode	EPP
ECP	ECP

ISA-Compatible, PS/2-Compatible, and EPP modes are selected through 82091AA configuration (see Section 4.0, AIP Configuration). ECP is selected by programming the ECP Extended Control Register (ECR).

In ISA-Compatible mode, the parallel port exactly emulates a standard ISA-style parallel port. The parallel port data bus (PD[7:0]) is uni-directional. The compatibility protocol transfers data to the peripheral device via PD[7:0] (forward direction). Note that the Nibble protocol permits data transfers from the peripheral device (reverse direction) by using four peripheral status signal lines to transfer 4 bits of data at a time.

PS/2-Compatible mode differs from ISA-Compatible mode by providing bi-directional transfers on PD[7:0]. A bit is added to the PCON Register to allow software control of the data transfer direction.

For both the ISA-Compatible and PS/2-Compatible modes, the actual data transfer over the parallel port interface is accomplished by software handshake (i.e., automatic hardware handshake is not used). Software controls data transfer by monitoring handshake signal status from the peripheral device via the PSTAT Register and controlling handshake signals to the peripheral device via the PCON Register.

EPP mode provides bi-directional transfers on PD[7:0]. The 82091AA automatically generates the address and data strobes in hardware.

ECP is a high performance peripheral interface mode. This mode uses an asynchronous automatic handshake to transfer data over the parallel port interface. In addition, the parallel port contains a FIFO for transferring data in ECP mode. The ECP register set contains an Extended Control Register (ECR) that provides a wide range of functions including the ability to operate the parallel port in either ECP, ISA-Compatible, or PS/2-Compatible modes.

NOTE:
In general, this document describes parallel port operations and functions in terms of how the 82091AA parallel port hardware operates. Detailed descriptions of the parallel interface protocols are beyond the scope of this document. Readers should refer to the proposed IEEE Standard 1284 for detailed descriptions of the Compatibility, Nibble, Byte, EPP, and ECP protocols.

Special circuitry on the 82091 prevents it from being powered up or being damaged while a parallel port peripheral is powered on and the 82091 is powered off.

6.1 Parallel Port Registers

This section is organized into three sub-sections—ISA-Compatible and PS/2-Compatible Modes, EPP Mode, and ECP Mode. Since the register sets are similar for ISA-Compatible and PS/2-Compatible modes (differing by a direction control bit in the PCON Register) the register set descriptions are combined. The EPP mode and ECP mode register sets are described separately. Each register set description contains the I/O address assignment and a complete description of the registers and register bits. Note that the PSTAT and PCON Registers are common to all modes and for completeness are repeated in each sub-section. Any difference in bit operations for a particular mode is noted in that particular register description.

The registers provide parallel port control/status information and data paths for transferring data between the parallel port interface and the 8-bit host interface. All registers are accessed as byte quantities. The base address is determined by hardware configuration at powerup (or a hard reset) or via software configuration by programming the 82091AA configuration registers as described in Section 4.0, AIP Configuration. The parallel port can be disabled or configured for a base address of 378h (all modes), 278h (all modes), or 3BCh (all modes except EPP and ECP). This provides the system designer with the option of using additional parallel ports on add-in cards that have fixed address decoding.

Some of the parallel port registers described in this section contain reserved bits. These bits are labeled "R". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the value of reserved bit positions must first be read, merged with the new values for other bit positions, and then written back.

During a hard reset (RSTDRV asserted), the 82091AA registers are set to pre-determined **default** states. The default values are indicated in the individual register descriptions.

The following nomenclature is used for register access attributes:

RO **Read Only**. Note that for registers with read only attributes, writes to the I/O address have no affect on parallel port operations.

R/W **Read/Write**. A register with this attribute can be read and written. Note that individual bits in some read/write registers may be read only.

6.1.1 ISA-COMPATIBLE AND PS/2-COMPATIBLE MODES

This section contains the registers used in ISA-Compatible and PS/2-Compatible modes. The I/O address assignment for this register set is shown in Table 15 and the register descriptions are presented in the order that they appear in the table.

Table 15. Parallel Port Register (ISA-Compatible and PS/2-Compatible)

Parallel Port Register Address Access (AEN = 0) Base +	Abbreviation	Register Name	Access
0h	PDATA	Data Register	R/W
1h	PSTAT	Status Register	RO
2h	PCON	Control Register	R/W

NOTE:
Parallel port base addresses are 278h, 378h and 3BCh.

6.1.1.1 PDATA—Parallel Port Data Register (ISA-Compatible and PS/2-Compatible Modes)

I/O Address: Base + 00h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

ISA-Compatible Mode

The PDATA Register is a uni-directional data port that transfers 8-bit data from the host to the peripheral device (forward transfer). A write to this register drives the written data onto PD[7:0]. Reads of this register should not be performed in ISA-Compatible mode. For a host read of this address location, the 82091AA completes the handshake on the ISA Bus and the value is the last value stored in the PDATA Register.

PS/2-Compatible Mode

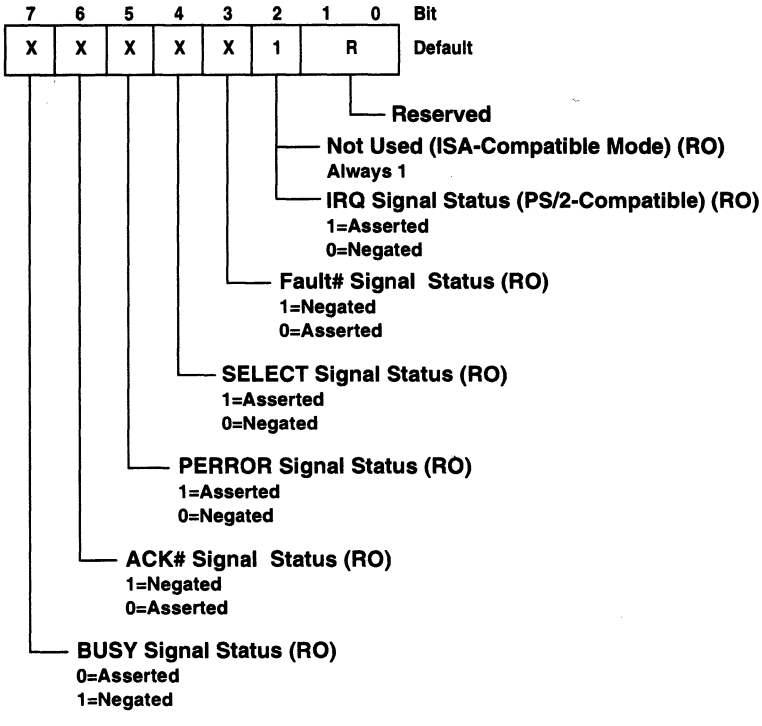
The PDATA Register is a bi-directional data port that transfers 8-bit data between the peripheral device and host. The direction of transfer is determined by the DIR# bit in the PCON Register. If DIR# = 0 (forward direction), and the host writes to this register, the data is stored in the PDATA Register and driven onto PD[7:0]. If DIR# = 1 (reverse direction), a host read of this register returns the data on PD[7:0]. Note that read data is not stored in the PDATA Register.

Bit	Description
7:0	**PARALLEL PORT DATA:** Bits[7:0] correspond to parallel port data lines PD[7:0] and ISA Bus data lines SD[7:0].

6.1.1.2 PSTAT—Status Register (ISA-Compatible and PS/2-Compatible Modes)

I/O Address: Base + 01h
Default Value: XXXX X1RR
Attribute: Read Only
Size: 8 bits

The PSTAT Register provides the status of certain parallel port signals and whether a CPU interrupt has been generated by the parallel port. This register indicates the current state of the BUSY, ACK#, PERROR, SELECT, and FAULT# signals.



NOTE:
X = Default value is determined by signal state at reset.

Figure 26. Status Register (ISA-Compatible and PS/2-Compatible Modes)

Bit	Description
7	**BUSY STATUS (BUSYS):** This bit indicates the state of the parallel port interface BUSY signal. When BUSY is asserted, BUSYS = 0. When BUSY is negated, BUSYS = 1.This bit is an inverted version of the parallel port BUSY signal.
6	**ACK# STATUS (ACKS):** This bit indicates the state of the parallel port interface ACK# signal. This bit indicates when the peripheral has received a data byte and is ready for another. When ACK# is asserted, ACKS = 0. When ACK# is negated, ACKS = 1. Note that if interrupts are enabled (via bit 4 of the PCON Register), the assertion of the ACK# signal generates an interrupt to the CPU.
5	**PERROR STATUS (PERRS):** This bit indicates the state of the parallel port interface PERROR signal. This bit indicates when an error has occurred in the peripheral paper path (e.g., out of paper). When PERROR is asserted, PERRS = 1, When PERROR is negated, PERRS = 0.
4	**SELECT STATUS (SELS):** This bit indicates the state of the parallel port interface SELECT signal. When the SELECT signal is asserted, SELS = 1, When the SELECT signal is negated, SELS = 0.
3	**FAULT# STATUS (FAULTS):** This bit indicates the state of the parallel port interface FAULT# signal being driven by the peripheral device. When the FAULT# signal is asserted, FAULTS = 0. When the FAULT# signal is negated, FAULTS = 1.
2	**PARALLEL PORT INTERRUPT STATUS (PIRQ):** This bit indicates a CPU interrupt by the parallel port. PIRQ indicates that the printer has accepted the previous character and is ready for another. In ISA-Compatible mode, interrupt status is not reported in this register and this bit is always 1. In PS/2-Compatibile mode, if interrupts are enabled via the PCON Register and the ACK# signal is asserted (low-to-high transition), PIRQ is set to a 0 (and an IRQ generated to the CPU). The 82091AA sets PIRQ to 1 when this register is read or by a hard reset. If interrupts are disabled via the PCON Register, this bit is never set to 0.
1:0	**RESERVED**

6.1.1.3 PCON—Control Register (ISA-Compatible And PS/2-Compatible Mode)

I/O Address: Base + 02h
Default Value: RR00 0000
Attribute: Read/Write
Size: 8 bits

The PCON Register controls certain parallel port interface signals and enables/disables parallel port interrupts. This register permits software to control the STROBE#, AUTOFD#, INIT#, and SELECTIN# signals. For PS/2-Compatible mode, this register also controls the direction of transfer on PD[7:0].

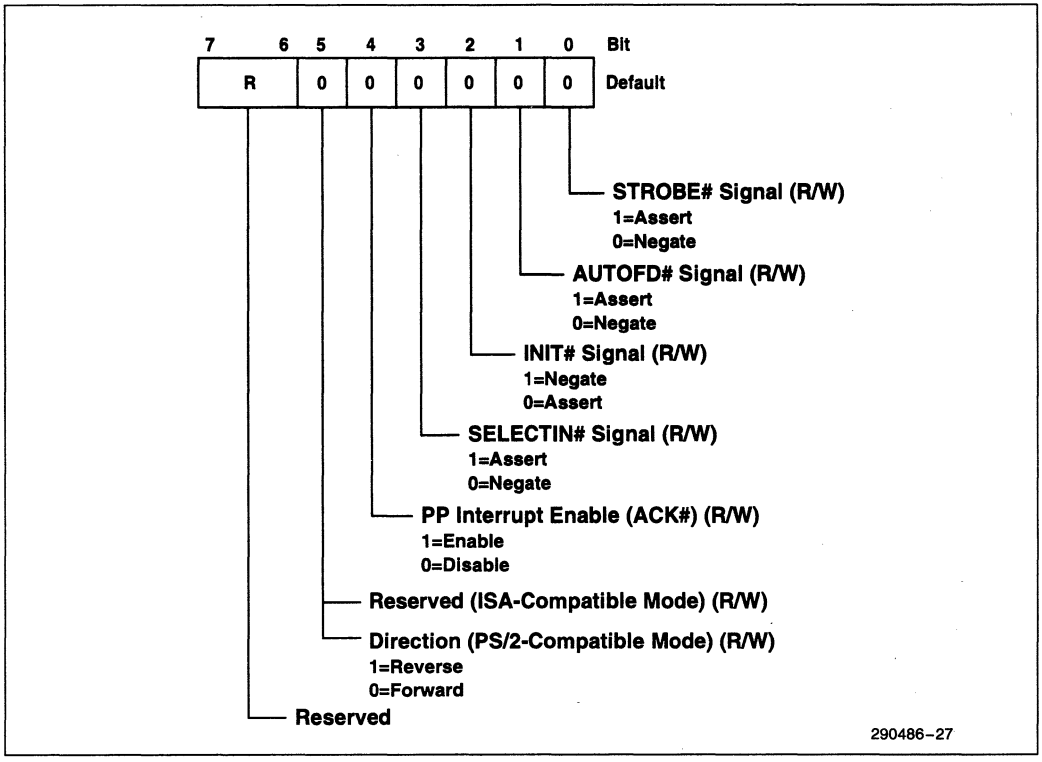


Figure 27. Control Register (ISA-Compatible and PS/2-Compatible Modes)

2

Bit	Description
7:6	**RESERVED**
5	**RESERVED (ISA-COMPATIBLE MODE):** Not used and undefined when read. Writes have no affect on parallel port operations. **DIRECTION (DIR#) (PS/2-COMPATIBLE MODE):** This bit is used to control the direction of data transfer on the parallel port data bus (PD[7:0]). When DIR# = 0, PD[7:0] are outputs. When DIR# = 1, PD[7:0] are inputs.
4	**ACK# INTERRUPT ENABLE (ACKINTEN):** ACKINTEN enables CPU interrupts (via either IRQ5 or IRQ7) to be generated when the ACK# signal on the parallel port interface is asserted. When ACKINTEN = 1, a CPU interrupt is generated when ACK# is asserted. When ACKINTEN = 0, the ACK# interrupt is disabled.
3	**SELECTIN# CONTROL (SELINC):** This bit controls the SELECTIN# signal. SELINC is set to 1 to select the printer. When SELINC = 1, the SELECTIN# signal is asserted, When SELINC = 0, the SELECTIN# signal is negated.
2	**INIT# CONTROL (INITC):** This bit controls the INIT# signal. When INITC = 1, the INIT# signal is negated. When INITC = 0, the INIT# signal is asserted.
1	**AUTOFD# CONTROL (AUTOFDC):** This bit controls the AUTOFD# signal. AUTOFDC is set to 1 to instruct the printer to advance the paper one line each time a carriage return is received. When AUTOFDC = 1, the AUTOFD# signal is asserted. When AUTOFDC = 0, the AUTOFD# signal is negated.
0	**STROBE# CONTROL (STROBEC):** This bit controls the STROBE# signal. The STROBE# signal is set active to instruct the printer to accept the character being presented on the data lines. When STROBEC = 1, the STROBE# signal is asserted. When STROBEC = 0, the STROBE# signal is negated.

6.1.2 EPP MODE

This section contains the registers used in EPP mode. The I/O address assigment for this register set is shown in Table 16 and the register descriptions are presented in the order that they appear in the table.

Table 16. Parallel Port Registers (EPP Mode)

Parallel Port Register Address Access (AEN = 0) Base +	Abbreviation	Register Name	Access
0h	PDATA	Data Register	R/W
1h	PSTAT	Status Register	RO
2h	PCON	Control Register	R/W
3h	ADDSTR	Address Strobe Register	R/W
4h–7h	DATASTR	Data Strobe Registers	R/W

NOTE:
Parallel port base addresses are 278h (LPT2) and 378h (LPT1). Base address 3BCh is not available in EPP or ECP modes.

6.1.2.1 PDATA—Parallel Port Data Register (EPP Mode)

I/O Address: Base + 00h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

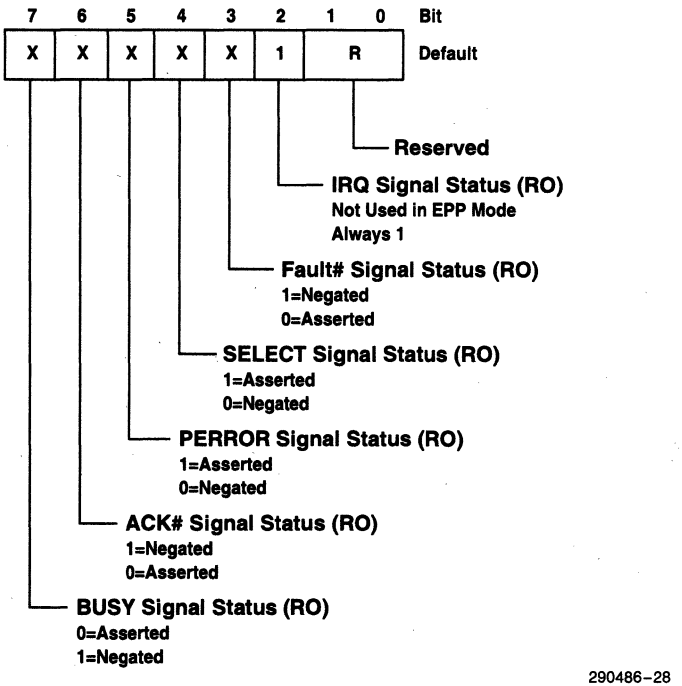
The PDATA Register is a bi-directional data port that transfers 8-bit data between the peripheral device and host. The direction of transfer is determined by the DIR# bit in the PCON Register. If DIR# = 0 (forward direction) and the host writes to this register, the data is stored in the PDATA Register and driven onto PD[7:0]. If DIR# = 1 (reverse direction), a host read of this register returns the data on PD[7:0]. However, read data is not stored in the PDATA Register.

Bit	Description
7:0	**PARALLEL PORT DATA:** Bits[7:0] correspond to parallel port data lines PD[7:0] and ISA Bus data lines.

6.1.2.2 PSTAT—Status Register (EPP Mode)

I/O Address: Base +01h
Default Value: XXXX X1RR
Attribute: Read Only
Size: 8 bits

The PSTAT Register provides the status of certain parallel port signals. It also indicates whether a CPU interrupt has been generated by the parallel port. This register indicates the current state of the BUSY, ACK#, PERROR, SELECT, and FAULT# signals.



NOTE:
X = Default value is determined by signal state at reset.

Figure 28. Status Register (EPP Mode)

Bit	Description
7	**BUSY STATUS (BUSYS):** This bit indicates the state of the parallel port interface BUSY signal. When BUSY is asserted, BUSYS = 0. When BUSY is negated, BUSYS = 1. This bit is an inverted version of the parallel port BUSY signal.
6	**ACK# STATUS (ACKS):** This bit indicates the state of the parallel port interface ACK# signal. This bit indicates when the peripheral has received a data byte and is ready for another. When ACK# is asserted, ACKS = 0. When ACK# is negated, ACKS = 1. Note that if interrupts are enabled (via bit 4 of the PCON Register), the assertion of the ACK# signal generates an interrupt to the CPU.
5	**PERROR STATUS (PERRS):** This bit indicates the state of the parallel port interface PERROR signal. This bit indicates when an error has occurred in the peripheral paper path (e.g., out of paper). When PERROR is asserted, PERRS = 1. When PERROR is negated, PERRS = 0.
4	**SELECT STATUS (SELS):** This bit indicates the state of the parallel port interface SELECT signal. When the SELECT signal is asserted, SELS = 1. When the SELECT signal is negated, SELS = 0.
3	**FAULT# STATUS (FAULTS):** This bit indicates the state of the parallel port interface FAULT# signal being driven by the peripheral device. When the FAULT# signal is asserted, FAULTS = 0. When the FAULT# signal is negated, FAULTS = 1.
2	**PARALLEL PORT INTERRUPT (PIRQ):** In EPP mode interrupt status is not reported in this register and this bit is always 1.
1:0	**RESERVED**

6.1.2.3 PCON—Control Register (EPP Mode)

I/O Address: Base + 02h
Default Value: RR00 0000
Attribute: Read/Write
Size: 8 bits

The PCON Register controls certain parallel port interface signals, enables/disables parallel port interrupts, and selects the direction of data transfer on PD[7:0]. This register permits software to control the INIT# signal. Note that in the EPP parallel interface protocol, the STROBE#, AUTOFD#, and SELECTIN# signals are automatically generated by the parallel port and are not controlled by software.

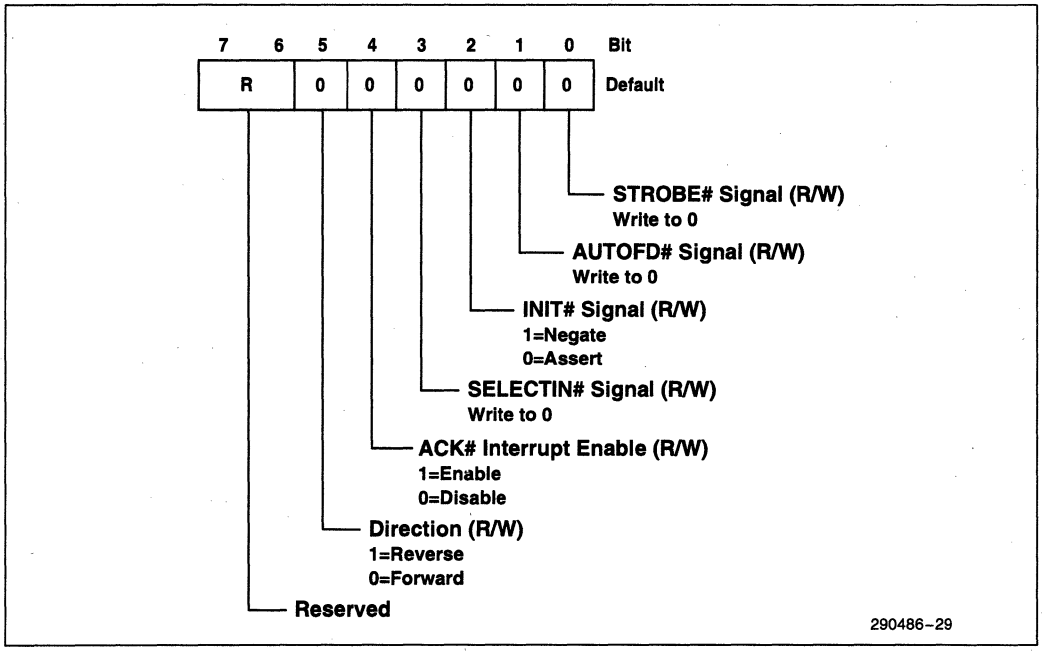


Figure 29. Control Register (EPP Mode)

Bit	Description
7:6	**RESERVED**
5	**DIRECTION (DIR#):** This bit is used to control the direction of data transfer on the parallel port data bus (PD[7:0]). When DIR# = 0 (forward direction), PD[7:0] are outputs. When DIR# = 1 (reverse direction), PD[7:0] are inputs.
4	**ACK# INTERRUPT ENABLE (ACKINTEN):** ACKINTEN enables CPU interrupts (via IRQ5 or IRQ7) to be generated when the ACK# signal on the parallel port interface is asserted. When ACKINTEN = 1, a CPU interrupt is generated when ACK# is asserted. When ACKINTEN = 0, the ACK# interrupt is disabled.
3	**SELECTIN# CONTROL (SELINC):** Write to 0 when programming this register. This bit must be 0 for the parallel port handshake to operate properly.
2	**INIT# CONTROL (INITC):** This bit controls the INIT# signal. When INITC = 1, the INIT# signal is negated. When INITC = 0, the INIT# signal is asserted.
1	**AUTOFD# CONTROL (AUTOFDC):** Write to 0 when programming this register.
0	**STROBE# CONTROL (STROBEC):** Write to 0 when programming this register. This bit must be 0 for the parallel port handshake to operate properly.

6.1.2.4 ADDSTR—EPP Auto Address Strobe Register (EPP Mode)

I/O Address: Base +03h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The ADDSTR Register provides a peripheral address to the peripheral (via PD[7:0]) during a host address write operation and to the host (via PD[7:0]) during a host address read operation. An automatic address strobe is generated on the parallel port interface when data is read from or written to this register.

Bit	Description
7:0	**EPP ADDRESS:** Bits[7:0] correspond to SD[7:0] and PD[7:0].

6.1.2.5 DATASTR—Auto Data Strobe Register (EPP Mode)

I/O Address: Base +04h, 05h, 06h, 07h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The DATASTR Register provides data from the host to the peripheral device (via PD[7:0]) during host write operations and from the peripheral device to the host (via PD[7:0]) during a host read operation. An automatic data strobe is generated on the parallel port interface when data is read from or written to this register. To maintain compatibility with Intel's 82360SL I/O device that has a 32-bit Host Bus interface, four consecutive byte address locations are provided for transferring data.

Bit	Description
7:0	**EPP DATA:** Bits[7:0] correspond to SD[7:0] and PD[7:0].

6.1.3 ECP MODE

This section contains the registers used in ECP mode. The I/O address assignment for this register set is shown in Table 17 and the register descriptions are presented in the order that they appear in the table. The Extended Control Register (ECR) permits various modes of operation. Note that ECR[7:5] = 000 selects ISA-Compatible mode and ECR[7:5] = 001 selects PS/2-Compatibile mode. These modes are discussed in Section 6.1.1, ISA-Compatible and PS/2 Compatible modes. The other modes selected by ECR[7:5] are discussed in this section.

Table 17. Parallel Port Registers (ECP Mode)

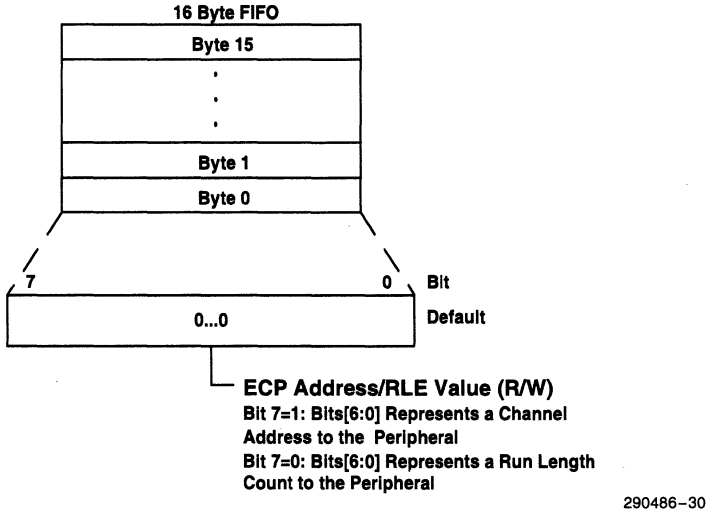
Parallel Port Register Address Access (AEN = 0) Base +	Abbreviation	Register Name	Access	
			ECR[7:5]	Read/Write Attribute
0h	ECPAFIFO	ECP Address/RLE FIFO	011	R/W
1h	PSTAT	Status Register	All	RO
2h	PCON	Control Register	All	R/W
400h	SDFIFO	Standard Parallel Port Data FIFO	010	R/W
400h	ECPDFIFO	ECP Data FIFO	011	R/W
400h	TFIFO	Test FIFO	110	R/W
400h	ECPCFGA	ECP Configuration A	111	R/W
401h	ECPCFGB	ECP Configuration B	111	R/W
402h	ECR	Extended Control Register	All	R/W

NOTES:
1. Parallel port base addresses are 278h, 378h, and 3BCh.
2. A register is accessible when the ECR[7:5] field contains the value specified in the ECR[7:5] column. The register is not accessible if the ECR[7:5] field does not match the value specified in this column. The term "All" means that the register is accessible in all modes selected by ECR[7:5].

6.1.3.1 ECPAFIFO—ECP Address/RLE FIFO Register (ECP Mode)

I/O Address: Base + 00h
Default Value: UUUU UUUU (Undefined)
Attribute: Read/Write
Size: 8 bits

The ECPAFIFO Register provides a channel address or a Run Length Count (RLE) to the peripheral, depending on the state of bit 7. This I/O address location is only used in ECP mode (ECR bits[7:5] = 011). In this mode, bytes written to this register are placed in the parallel port FIFO and transmitted over PD[7:0] using ECP protocol.



NOTE:
U = Undefined

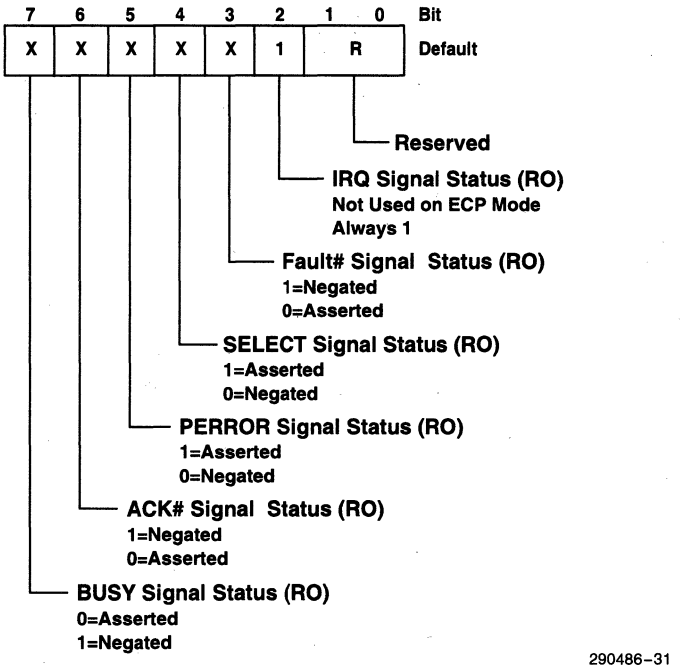
Figure 30. ECP Address/RLE FIFO Register (ECP Mode)

Bit	Description
7:0	**ECP ADDRESS/RLE VALUE:** Bits[7:0] correspond to parallel port data lines PD[7:0] and ISA Bus data lines SD[7:0]. The peripheral device should interpret bits[6:0] as a channel address when bit 7 = 1 and as a run length count when bit 7 = 0. Note that this interpretation is performed by the peripheral device and the value of bit 7 has no affect on 82091AA operations. Note that the 82091AA asserts AUTOFD# to indicate that the information on PD[7:0] represents an ECP address/RLE count. The 82091AA negates AUTOFD# (drives high) when PD[7:0] is transferring data.

6.1.3.2 PSTAT—Status Register (ECP Mode)

I/O Address: Base + 01h
Default Value: XXXX X1RR
Attribute: Read Only
Size: 8 bits

The PSTAT Register provides the status of certain parallel port signals and whether a CPU interrupt has been generated by the parallel port. This register indicates the current state of the BUSY, ACK#, PERROR, SELECT, and FAULT# signals.



NOTE:
X = Default value is determined by the state of the corresponding signal pin at reset.

Figure 31. Status Register (ECP Mode)

Bit	Description
7	**BUSY STATUS (BUSYS):** This bit indicates the state of the parallel port interface BUSY signal. When BUSY is asserted, BUSYS = 0. When BUSY is negated, BUSYS = 1. This is an inverted version of the parallel port BUSY signal. Refer to Section 6.2.3 ECP Mode for more detail.
6	**ACK# STATUS (ACKS):** This bit indicates the state of the parallel port interface ACK# signal. This bit indicates when the peripheral has received a data byte and is ready for another. When ACK# is asserted, ACKS = 0. When ACK# is negated, ACKS = 1. Note that if interrupts are enabled (via bit 4 of the PCON Register), the assertion of the ACK# signal generates an interrupt to the CPU. Refer to Section 6.2.3 ECP Mode for more detail.
5	**PERROR STATUS (PERRS):** This bit indicates the state of the parallel port interface PERROR signal. This bit indicates when an error has occurred in the peripheral paper path (e.g., out of paper). When PERROR is asserted, PERRS = 1, When PERROR is negated, PERRS = 0.
4	**SELECT STATUS (SELS):** This bit is used in all parallel port modes and indicates the state of the parallel port interface SELECT signal. When the SELECT signal is asserted, SELS = 1. When the SELECT signal is negated, SELS = 0.
3	**FAULT# STATUS (FAULTS):** This bit is used in all parallel port modes and indicates the state of the parallel port interface FAULT# signal being driven by the peripheral device. When the FAULT# signal is asserted, FAULTS = 0. When the FAULT# signal is negated, FAULTS = 1.
2	**PARALLEL PORT INTERRUPT (PIRQ):** In ECP mode, interrupt status is not reported in this register and this bit is always 1.
1:0	**RESERVED**

6.1.3.3 PCON—Control Register (ECP Mode)

I/O Address: Base + 02h
Default Value: RR00 0000
Attribute: Read/Write
Size: 8 bits

The PCON Register controls certain parallel port interface signals, enables/disables parallel port interrupts, and selects the direction of data transfer on PD[7:0]. Note that the function of some bits depends on the programming of the ECR.

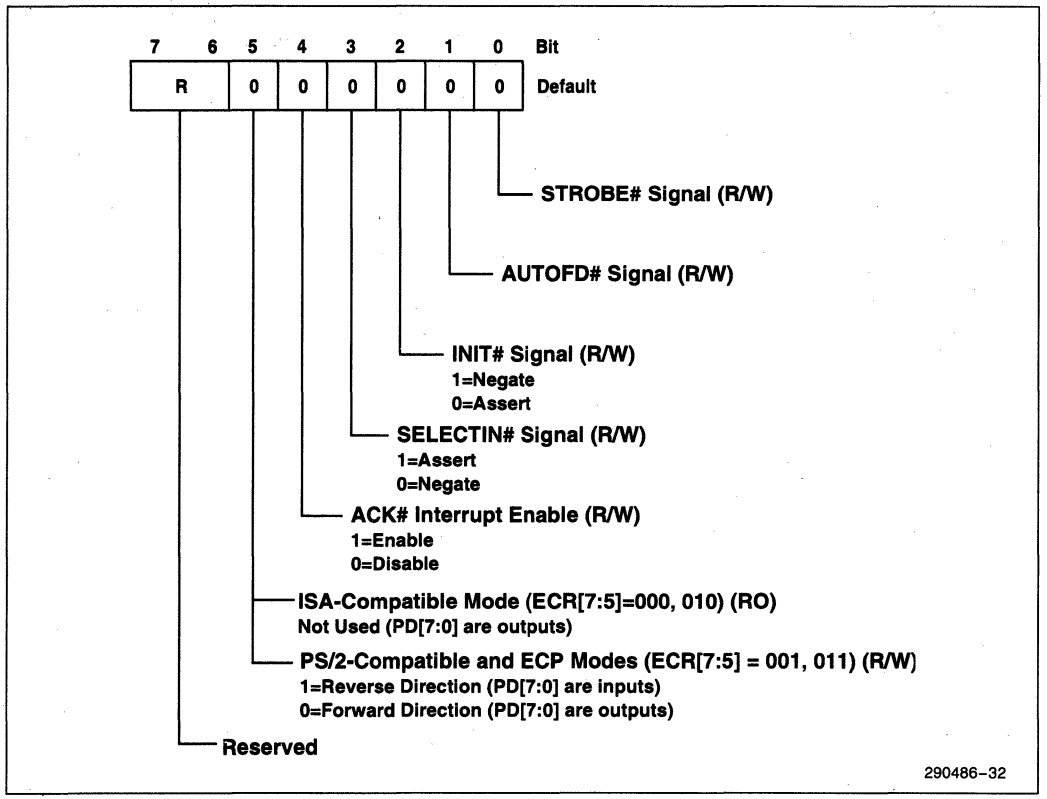


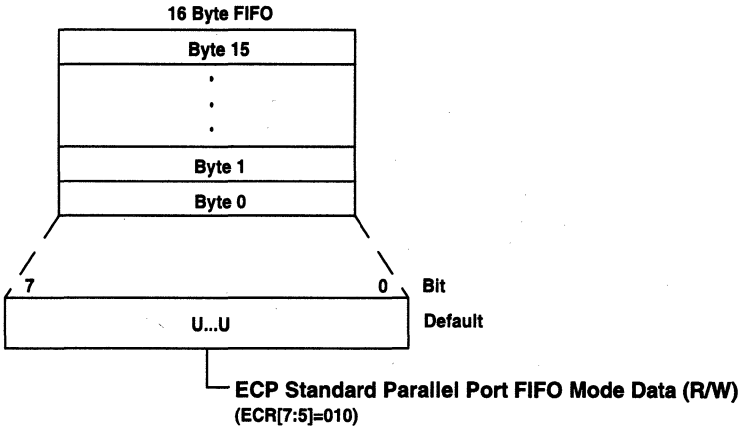
Figure 32. Control Register (ECP Mode)

Bit	Description
7:6	**RESERVED**
5	**DIRECTION (DIR#):** This bit is used to control the direction of data transfer on the parallel port data bus (PD[7:0]). When DIR# = 0 (forward direction), PD[7:0] are outputs. When DIR# = 1 (reverse direction), PD[7:0] are inputs.
4	**INTERRUPT ENABLE (ACK#) (IRQEN):** IRQEN enables interrupts to the CPU to be generated when the ACK# signal on the parallel port interface is asserted and is used in all parallel port interface modes. When IRQEN = 1, a CPU interrupt is generated when ACK# is asserted. When IRQEN = 0, parallel port interrupts are disabled.
3	**SELECTIN# CONTROL (SELINC):** This bit controls the SELECTIN# signal. SELINC is set to 1 to select the printer. When SELINC = 1, the SELECTIN# signal is asserted, When SELINC = 0, the SELECTIN# signal is negated.
2	**INIT# CONTROL (INITC):** This bit controls the INIT# signal When INITC = 1, the INIT# signal is negated. When INITC = 0, the INIT# signal is asserted.
1	**AUTOFD# CONTROL (AUTOFDC):** In ECP mode or ISA-Compatible FIFO mode (ECR[7:5] = 011, 010), this bit has no effect. Refer to Section 6.2.3 ECP Mode for more details.
0	**STROBE# CONTROL (STROBEC):** In ECP mode or ISA-Compatible FIFO mode (ECR[7:5] = 011, 010), this bit has no effect. Refer to Section 6.2.3 ECP Mode for more details.

6.1.3.4 SDFIFO—Standard Parallel Port Data FIFO

I/O Address: Base + 400h and (ECR[7:5] = 010)
Default Value: UUUU UUUU (undefined)
Attribute: Read/Write
Size: 8 bits

SDFIFO is used to transfer data from the host to the peripheral when the ECR Register is set for ISA-Compatible FIFO mode (bits[7:5] = 010). Data bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard ISA-Compatible protocol. Note that bit 5 in the PCON Register must be set to 0 for a forward transfer direction.



NOTE:
U = Undefined

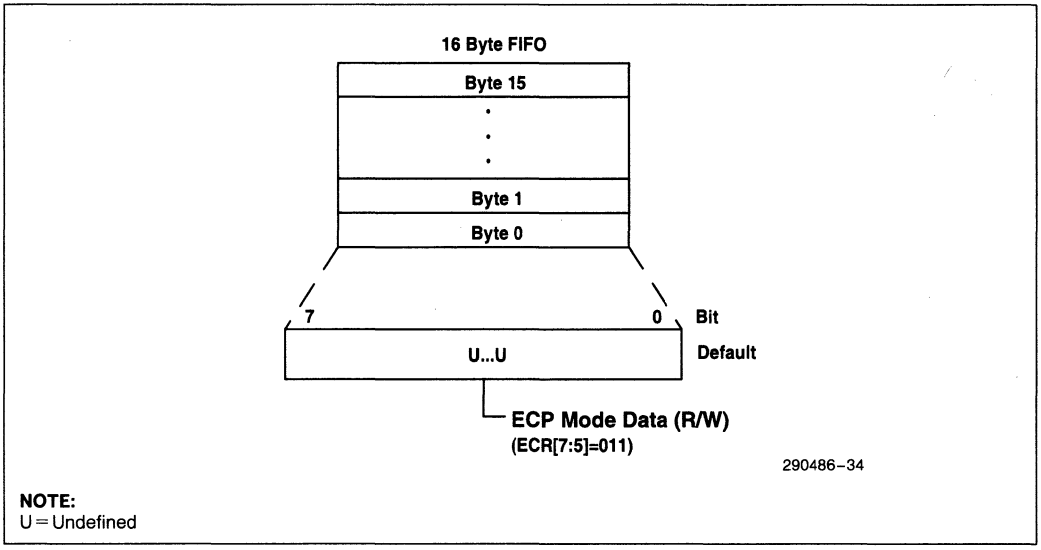
Figure 33. ECP ISA-Compatible Data FIFO

Bit	Description
7:0	**ECP STANDARD PARALLEL PORT DATA:** Bits[7:0] correspond to SD[7:0] and PD[7:0].

6.1.3.5 DFIFO—Data FIFO (ECP Mode)

I/O Address: Base +400h and (ECR[7:5] = 011)
Default Value: UUUU UUUU (undefined)
Attribute: Read/Write
Size: 8 bits

This I/O address location transfers data between the host and peripheral device when the parallel port is in ECP mode (ECR Bits[7:5] = 011). Transfers use the parallel port FIFO. Data is transferred on PD[7:0] via hardware handshakes on the parallel port interface using ECP parallel port interface handshake protocol.



NOTE:
U = Undefined

Figure 34. ECP Data FIFO (ECP Mode)

Bit	Description
7:0	**ECP MODE DATA:** Data bytes written or DMAed from the system to this FIFO in the forward direction (PCON bit 5 = 0) are transmitted to the peripheral by an ECP mode protocol hardware handshake. In the reverse direction (PCON bit 5 = 1) data bytes from the peripheral are transferred to the FIFO using the ECP mode protocol hardware handshake. Reads or DMAs from the FIFO return bytes of ECP data to the system. Bits[7:0] correspond to SD[7:0] and PD[7:0].

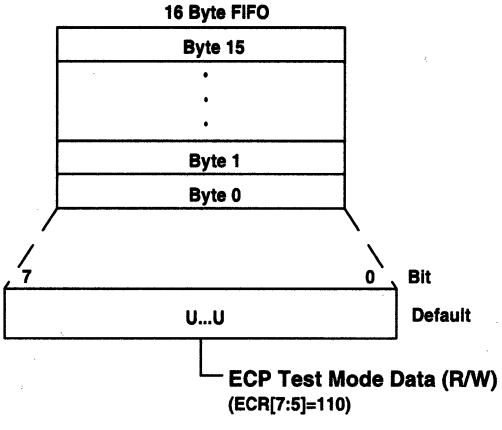
6.1.3.6 TFIFO—ECP Test FIFO Register (ECP Mode)

I/O Address: Base +400 and (ECR[7:5] = 110)
Default Value: UUUU UUUU (undefined)
Attribute: Read/Write
Size: 8 bits

The TFIFO Register provides a test mechanism for the ECP mode FIFO. Test mode is enabled via the ECR Register. In test mode (ECR[7:5] = 110), data can be read, written or DMAed to/from the FIFO by accessing this register I/O address.

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction. The parallel port interface signals are not affected by TFIFO accesses and TFIFO data is not transmitted to PD[7:0]. The test FIFO does not stall when overwritten or underrun. Data is simply re-written or over-run. The full and the empty bits in the ECR always keep track of the correct FIFO state.

The test FIFO transfers data at the maximum ISA rate so that software can generate performance metrics. The FIFO write threshold can be determined by starting with a full TFIFO and emptying it a byte at a time until a service interrupt is set to 1 in the ECR. The FIFO read threshold can be determined by setting the direction bit in the PCON Register to 1, and filling the FIFO a byte at a time until the service interrupt is set to 1 in the ECR.



NOTE:
U = Undefined

Figure 35. ECP Test FIFO Register (ECP Mode)

Bit	Description
7:0	**ECP TEST FIFO** Data: Bits[7:0] correspond to SD[7:0].

6.1.3.7 ECPCFGA—ECP Configuration A Register (ECP Mode)

I/O Address: Base +400h and (ECR[7:5] = 111)
Default Value: 1001 RRRR
Attribute: Read/Write
Size: 8 bits

The ECPCFGA Register provides information about the ECP mode implementation. Access to this register is enabled by programming the ECR Register (ECR[7:5] = 111).

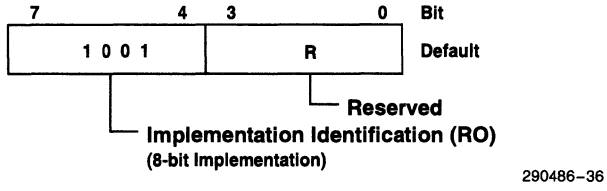


Figure 36. ECP Configuration A Register (ECP Mode)

Bit	Description
7:4	**IMPLEMENTATION IDENTIFICATION (IMPID):** This field is hardwired to 1001 to indicate an 8-bit implementation (bit 4) and an ISA-style interrupt (bit 7). This field is read only and writes have no affect.
3:0	**RESERVED**

6.1.3.8 ECPCFGB—ECP Configuration B Register (ECP Mode)

I/O Address: Base + 401h and (ECR[7:5] = 111)
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The ECPCFGB Register is part of the ECP specification and is implemented in the 82091AA as a scratchpad register. Software can use the fields in this register to maintain system information. Programming these bits does not affect parallel port operations. Access to the ECPCFGB Register is enabled by programming the ECR Register (ECR[7:5] = 111).

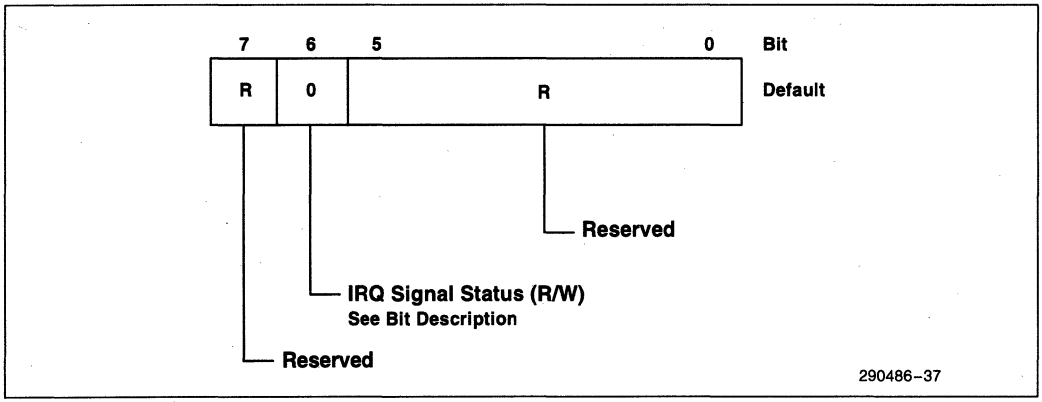


Figure 37. ECP Extended Control Register (ECP Mode)

Bit	Description
7	**RESERVED:** This bit always reads back as 0.
6	**INTRVALUE (INTRV):** This bit returns the value on the ISA IRQ line (IRQ5/IRQ7) to determine possible conflicts. The value of either IRQ5 or IRQ7 is read back based on the parallel port interrupt selection in the 82091AA configuration registers. IRQ5/IRQ7 are tri-stated in ECP configuration mode (ECR[7:5] = 111] to allow the state of the selected parallel port interrupt line to be read back. Note that the ACKINTEN bit in the PCON register must be written to 0 before the interrupt status can be read on this bit.
5:0	**RESERVED:** These bits always read back as 0.

6.1.3.9 ECR ECP—Extended Control Register (ECP Mode)

I/O Address: Base +402h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

This register selects the ECP mode, enables service and error interrupts and provides interrupt status. The ECR also enables/disables DMA operations and provides FIFO empty and FIFO full status. The FIFO empty and FIFO full status bits are also used to report FIFO overrun and underrun conditions.

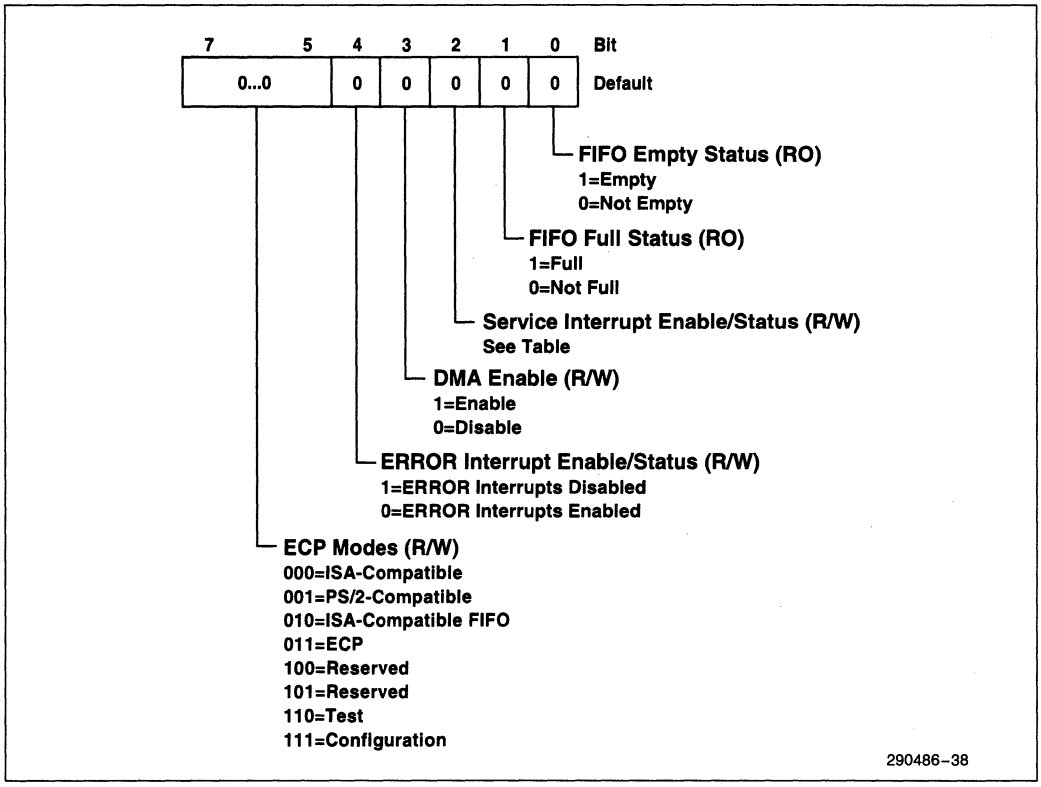


Figure 38. ECP Extended Control Register (ECP Mode)

2

Bit	Description
7:5	**ECP MODE SELECT:** This field selects one of the following ECP Modes: **Mode** **Operation** **0 0 0** **ISA-Compatible Mode.** In this mode the parallel port operates in ISA-Compatible mode. The FIFO is reset and common collector drivers are used on the control lines (STROBE#, AUTOFD#, INIT# and SELECTIN#). Setting the direction bit to 1 in the PCON Register does not affect the parallel port interface. For register descriptions in this mode, See Section 6.1.1, ISA-Compatible and PS/2-Compatible Modes. **0 0 1** **PS/2-Compatible Mode.** In this mode the parallel port operates in PS/2-Compatible mode. The FIFO is reset and common collector drivers are used on the control lines (STROBE#, AUTOFD#, INIT# and SELECTIN#). Unlike mode 000 above, setting the direction bit to 1 in the PCON Register tri-states the data lines and reading the data register returns the value on the PD[7:0]. For register descriptions in this mode, see Section 6.1.1, ISA-Compatible and PS/2-Compatible Modes. **0 1 0** **ISA-Compatible FIFO Mode.** This mode is the same as mode 000 above, except that data is written or DMAed to the FIFO. FIFO data is automatically transmitted using the ISA-style protocol. For this mode, the direction control bit in the PCON register must be 0. **0 1 1** **ECP Mode.** In the forward direction, bytes written to the ECP DFIFO location and bytes written to the ECP AFIFO location are placed in the ECP FIFO and transmitted automatically to the peripheral using ECP protocol. In reverse direction bytes are transferred from PD[7:0] to the ECP FIFO. **1 0 0** **Reserved** **1 0 1** **Reserved** **1 1 0** **Test Mode.** In this mode, the FIFO may be written and read, but the data will not be transmitted on PD[7:0]. **1 1 1** **Configuration Mode.** In this mode, the ECP Configuration A and B Registers are accessible. ECP Mode Switching Guidelines Software will execute P1284 negotiations and all operation prior to a data transfer phase under programmed I/O (using mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (using modes 011 or 010). Setting the mode to 011 or 010 causes the hardware to initiate the data transfer. If the parallel port is in mode 000 or 001, the port can be switched to any other mode. If the parallel port is not in mode 000 or 001, the port can only be switched into mode 000 or 001. The direction and the FIFO threshold can only be changed in modes 000 or 001. Note that the FIFO, FIFO Error, and TC conditions are also reset when the mode is switched to 000 or 001. Once in an extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case, all control signals are negated before the mode switch. In an ECP reverse mode the software waits for all the data to be read from the FIFO before changing to mode 000 or 001.

Bit	Description
4	**ERROR INTERRUPT DISABLE (ERRINTREN):** This bit enables error interrupts to the host. In ECP Mode, When ERRINTREN = 1, interrupts are disabled. When ERRINTREN = 0, interrupts are enabled. When enabled and a high-to-low transition occurs on the FAULT# signal (FAULT# asserted), an interrupt is generated to the host. Note that if this bit is written from a 1 to a 0 while FAULT# is asserted, an interrupt is generated to the host.
3	**DMA ENABLE (DMAEN):** This bit enables/disables DMA. When DMAEN = 1, DMA is enabled and the host uses PPDREQ, PPDACK, and TC to transfer data. When DMAEN = 0, DMA is disabled and the PPDREQ output is tri-stated. In this case, programmed I/O is used to transfer data between the host and the 82091AA FIFO. The Service Interrupt (bit 2) needs to be set to 0 to allow generation of a TC interrupt. This bit must be written to 0 to reset the TC interrupt.
2	**SERVICE INTERRUPT (SERVICEINTR):** This bit enables FIFO and TC service interrupts. When the CPU writes SERVICEINTR = 1, FIFO request interrupts, FIFO error interrupts, and TC interrupts are disabled. Setting this bit to a 0 enables interrupts for one of the four cases listed below. When enabled (set to 0) and one of the four conditions below occurs, the 82091AA sets SERVICEINTR to a 1 and generates an interrupt to the host. 1. During DMA operations (DMAEN = 1), when terminal count is reached (TC asserted). To clear the TC interrupt, switch to ISA-Compatible or PS/2-Compatible mode (write ECR[7:5] to 000, 001) or set DMAEN to 0. 2. In the forward direction and DMAEN = 0, when there is a threshold number of bytes in the FIFO to be written. 3. In the reverse direction and DMAEN = 0, when there is a threshold number of bytes in the FIFO to be read. 4. In either DMA or programmed I/O mode when there is a FIFO overrun or underrun. Reading the SERVICEINTR bit indicates the presence of an active interrupt when this bit has been written to a 0 prior to reading it back. To disable interrupts, the SERVICEINTR bit must be explicitly written to a 1. **NOTE:** The ACK# and FAULT# interrupts can be generated independent of the value of the SERVICEINTR bit. ACK# and FAULT# interrupts are enabled via the ACKINTREN bit in the PCON Register and the ERRINTREN bit in the ECR Registers, respectively. The parallel port IRQ output (IRQ5/IRQ7) is enabled when ACKINTREN = 1 in the PCON Register or when ECR[7:5] = 010, 011, or 110. Otherwise, the IRQ output is tri-stated.
1	**FIFO FULL STATUS (FIFOFS):** This bit indicates when the FIFO is full. When FIFOFS = 1 (and FIFOES = 0), the FIFO is full and cannot accept another byte of data. When FIFOFS = 0, at least one byte location is free in the FIFO. This bit is read only and writes have no affect. When a FIFO overrun or underrun occurs, the 82091AA sets both FIFOES and FIFOFS to 1. To clear the FIFO error condition interrupt, swiitch the parallel port mode from ECP (011) to either ISA-Compatible or PS/2-Compatible modes (000 or 001).
0	**FIFO EMPTY STATUS (FIFOES):** This bit indicates when the FIFO is empty. When FIFOES = 1 (and FIFOFS = 0), the FIFO is empty. When FIFOES = 0, the FIFO contains at least one byte. This bit is read only and writes have no affect. When a FIFO overrun or underrun occurs, the 82091AA sets both FIFOES and FIFOFS to 1. To clear the FIFO error condition interrupt, swiitch the parallel port mode from ECP (011) to either ISA-Compatible or PS/2-Compatible modes (000 or 001).

6.2 Parallel Port Operations

The parallel port can be placed in ISA-Compatible, PS/2-Compatible, or EPP mode by hardware configuration or by writing to the 82091AA's configuration registers (PCFG1 Register). If access to the configuration registers is not disabled by hardware configuration, a hardware configured parallel port mode can be changed by programming the PCFG1 Register.

ECP mode is entered by programming the ECP Extended Control Register (ECR). Writing to this register changes any previously selected parallel port mode (via hardware configuration or writing the PCFG1 Register) to one of the ECP ECR Register modes selected via ECR[7:5]. Note that ECP mode cannot be entered by hardware configuration or programming the 82091AA configuration registers.

6.2.1 ISA-COMPATIBLE AND PS/2-COMPATIBLE MODES

The ISA-Compatible mode is used for standard ISA-type parallel port interfaces. Figure 39 shows the parallel port interface for ISA-Compatible mode. STROBE#, AUTOFD#, INIT#, and SELECTIN# are controlled by software via the PCON Register and the status of SELECT, PERROR, FAULT, ACK#, and BUSY are reported in the PSTAT Register. PD[7:0] are outputs only. Note that for a reverse data transfer using the Nibble protocol, the peripheral device supplies data, 4 bits at a time, using the BUSY, SELECT, PERROR, and FAULT# signals.

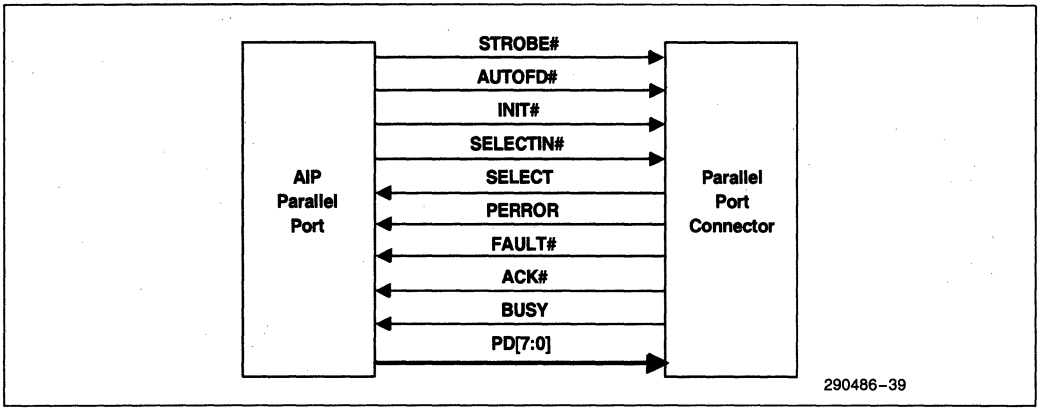


Figure 39. ISA-Compatible Mode

The following general protocol is used when communicating with a printer or other parallel port device.

Software selects the peripheral device by asserting the SELECTIN# signal. The peripheral device, in turn, acknowledges that it is selected by asserting the SELECT signal. The INIT# signal is used to initialize the peripheral device. If an error is encountered during initialization or normal operations, the peripheral device asserts FAULT#. If a printer (or plotter) encounters problems in the paper path, the device asserts PERROR. Other peripheral devices may not use the PERROR signal.

During normal operation, the peripheral device asserts BUSY when it is not ready to receive data. When it has finished processing the previous data, the peripheral device asserts ACK# and negates BUSY. If interrupts are enabled, a low-to-high transition on ACK# when the signal is negated generates an interrupt. If interrupts are not enabled, software must poll the PSTAT Register to determine when ACK# is pulsed.

The parallel port driver software sends data to the peripheral device by writing to the PDATA Register and asserting the STROBE# signal after an appropriate data stabilization interval. After a sufficient setup time has elapsed, software then negates STROBE#. Valid data is read by the peripheral device.

In the PS/2-Compatible mode, data can be written to or read from the parallel port. Figure 40 shows the parallel port interface for PS/2-Compatible mode. The Byte protocol signal names are shown in parenthesis. Before reading or writing the PDATA Register, the direction control bit in the PCON Register must be set to the proper transfer direction on PD[7:0]. During a write to the PDATA Register (with DIR# = 0), data is latched by the PDATA Register and driven onto PD[7:0]. During a parallel port read of the PDATA Register (with DIR# = 1), the data on PD[7:0] is driven onto SD[7:0]. The data is not latched by the PDATA Register during the read cycle.

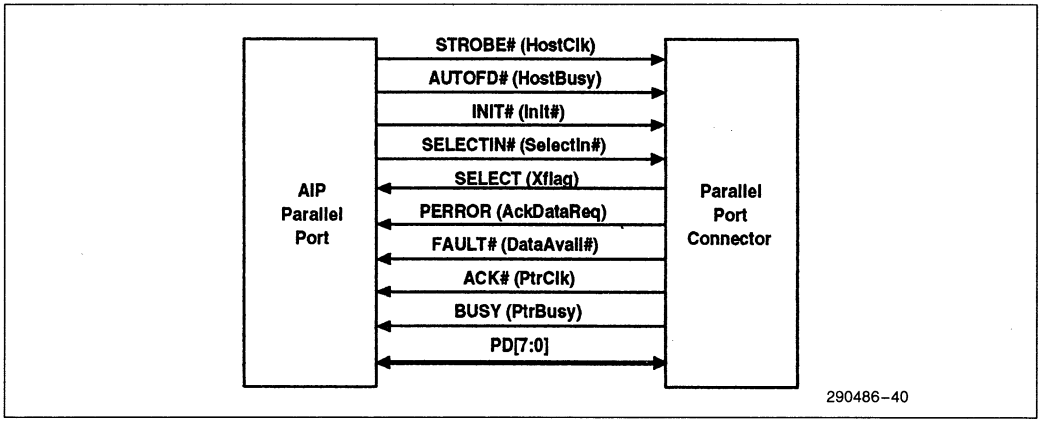


Figure 40. PS/2-Compatible Mode

6.2.2 EPP MODE

The 82091AA is EPP 1.7 compliant. This means EPP cycles will begin with WAIT (Busy) inactive, however, WAIT will still prolong the cycle when active. Figure 41 shows the parallel port interface for EPP mode. The EPP parallel port interface protocol signal names are shown in parenthesis. In EPP mode, the initialization, printer selection, and error signals (PERROR and FAULT#) work the same way as in the ISA-Compatible mode. However, in EPP mode, SELECTIN# and AUTOFD# are automatically generated and become Address Strobe (AStrb#) and Data Strobe (DStrb#), respectively, enabling direct access to parallel port devices. STROBE (Write#) is used to indicate a read or write cycle. Note that BUSY (Wait) is an active low signal in EPP mode rather than an active high signal as in ISA-Compatible mode. In addition, BUSY, in combination with IOCHRDY on the ISA Bus extends clock cycles to enable the completion of a read or write without additional wait states. EPP write and read cycles are shown in Figure 42 and Figure 43.

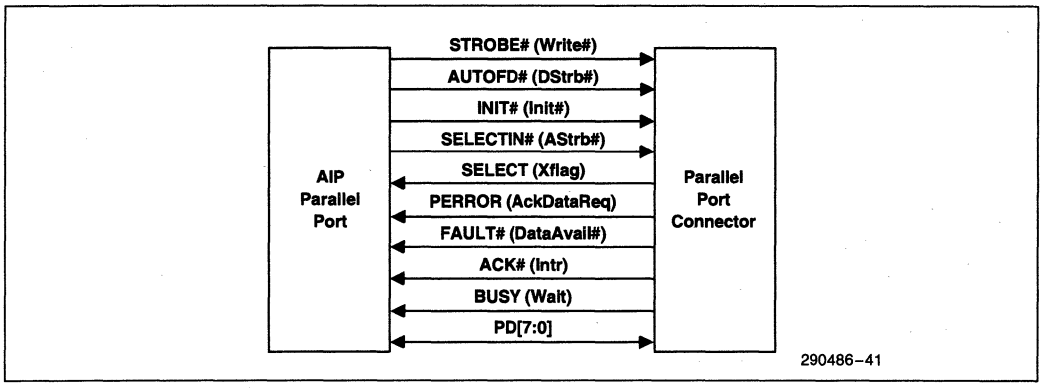


Figure 41. EPP Mode

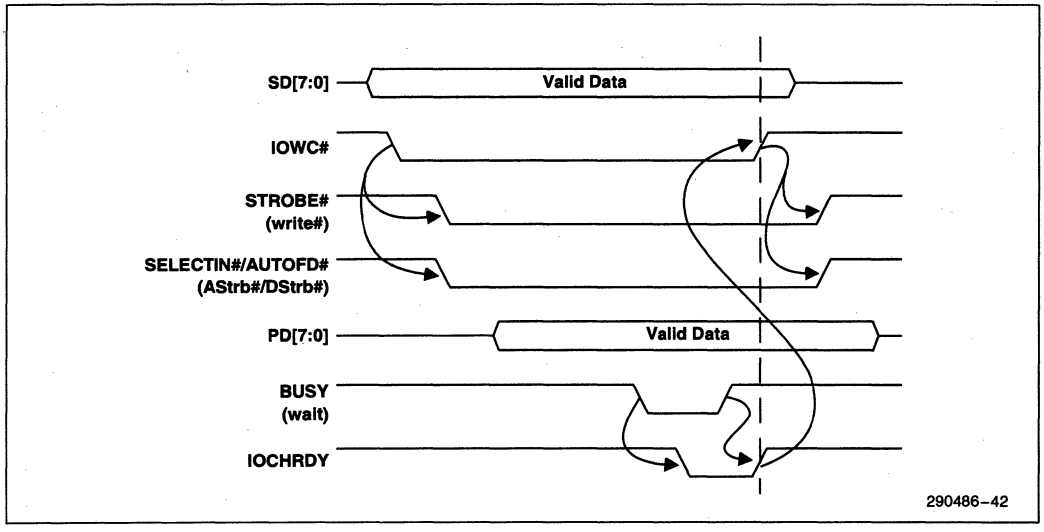


Figure 42. EPP Mode Write Cycle

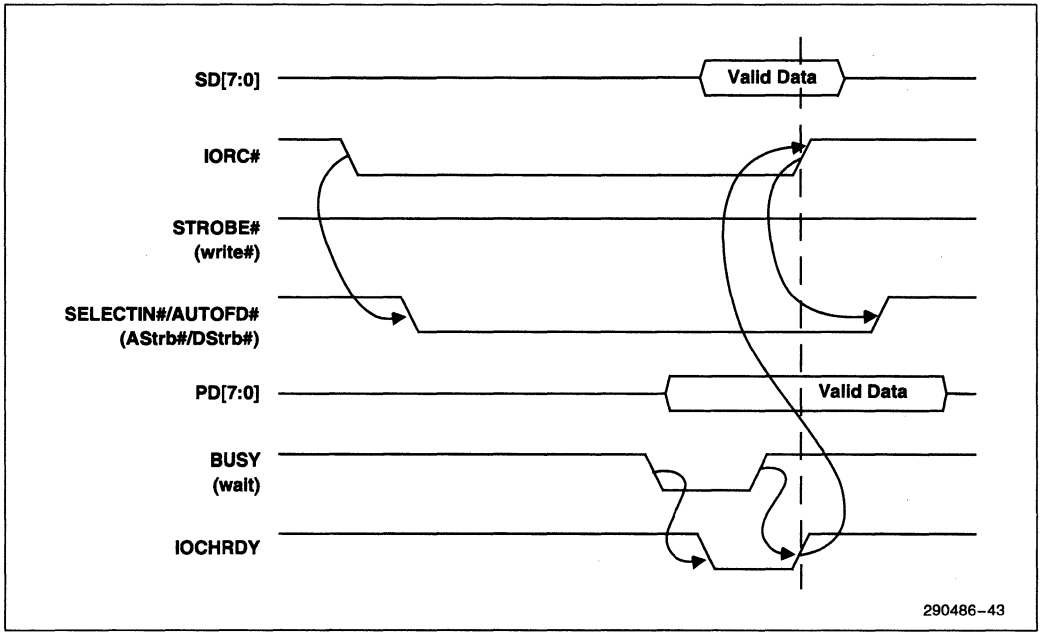


Figure 43. EPP Mode Read Cycle

6.2.3 ECP MODE

Figure 44 shows the parallel port interface for ECP mode with the ECP protocol signal names in parenthesis. The ECP modes are selected by programming the Extended Control Register (ECR bits[7:5]). Two of the modes (Test and Configuration) provide information about the 82091AA's parallel port and are not used for interfacing with a peripheral device. Four peripheral interface modes are selectable via the ECR—ISA-Compatible mode, ISA-Compatible FIFO mode, PS/2-Compatible mode, and ECP mode.

ISA-Compatible and PS/2-Compatible Modes (ECR[7:5] = 000,001)

The ISA-Compatible and PS/2-Compatible mode selections in the ECR are equivalent to selecting these modes via hardware configuration or programming the PCFG1 Register. For these modes the operation is the same as described in Section 6.2.1, ISA-Compatible and PS/2-Compatible Modes.

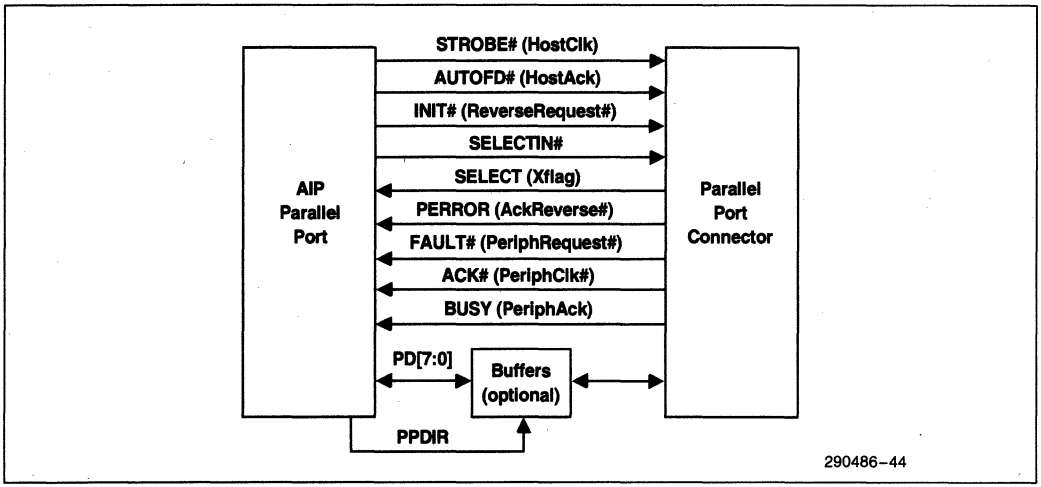


Figure 44. ECP Mode

ISA-Compatible FIFO Mode (ECR[7:5] = 010)

The ISA-Compatible FIFO mode uses the same signaling protocol on the parallel port interface as the ISA-Compatible mode. However, there are two major operational differences. First, data is written to a 16-byte FIFO (via the SDFIFO address location). The FIFO empty and FIFO full bits in the ECR provide FIFO status. In addition, DMA can be used to transfer data to the FIFO by enabling this feature in the ECR.

Second, the data is transferred to the peripheral using an automatic hardware handshake. This handshake emulates the standard ISA-Compatible style software generated handshake (Figure 45). For ISA-Compatible FIFO mode, the 82091AA does not monitor the ACK# signal. Service interrupts are enabled and reported via the ECR. The generation of service interrupts is based on the state of the FIFO and not individual transfers (using ACK#) as is the case in standard ISA-Compatible mode.

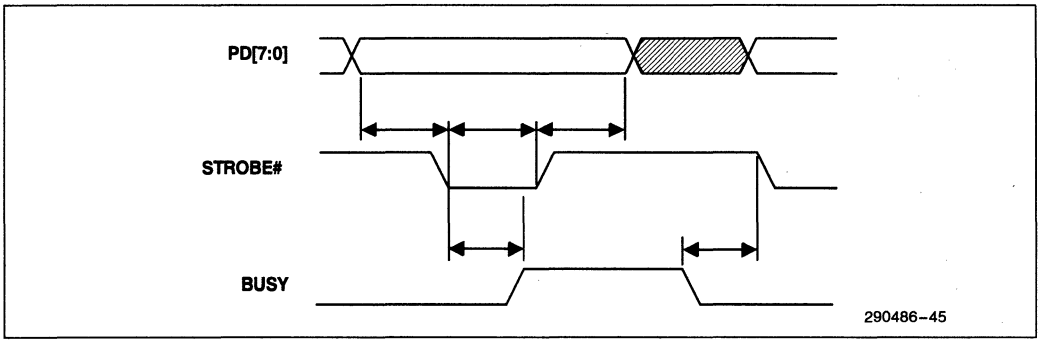


Figure 45. ISA-Compatible Timing

ECP Mode (ECR[7:5] = 011)

When ECR[7:5] = 011, the parallel port operates in ECP mode. In ECP mode, both data and commands (addresses and RLE) are transferred using the parallel port 16-byte FIFO. This information can be either written to or read from the FIFO using DMA or non-DMA ISA Bus transfers. The parallel port interface transfers use an automatic handshake generated by the 82091AA. The host controls the transfer direction by programming the DIR# bit in the PCON Register.

When the host is writing to the peripheral device (forward direction), STROBE#, and BUSY provide the automatic handshake for transfer on the parallel port interface (Figure 46). The peripheral device negates BUSY when it is ready to receive data or commands. AUTOFD# indicates whether PD[7:0] contain data (AUTOFD# is high) or a command (AUTOFD# is low). For commands (address or RLE), the host writes to the ECPAFIFO Register I/O address and for data, the host writes to the DFIFO Register I/O address. The addresses and data are placed in the same 16-byte FIFO. When the FIFO is full and cannot accept more data/addresses, the FIFO Full status bit is set in the ECR.

Data/addresses written to the FIFO are transferred to the peripheral device via PD[7:0]. To begin a transfer on the peripheral interface, the 82091AA checks BUSY to make sure the peripheral is in the ready state. If BUSY is negated, the 82091AA drives PD[7:0] and AUTOFD#, and asserts STROBE# to indicate that the data/command is on PD[7:0]. The peripheral device asserts BUSY to indicate that it is receiving the data/command. BUSY asserted causes the 82091AA to negate STROBE#.

When the host is reading from the peripheral device (reverse direction), AUTOFD# and ACK# provide the automatic handshake for transfer on the parallel port interface (Figure 47). Data/commands from the peripheral device are placed in the parallel port FIFO using this handshake. In this case, BUSY indicates whether PD[7:0] contain data (BUSY is high) or a command (BUSY is low).

The peripheral device asserts ACK# to indicate that a data/command is on PD[7:0]. The 82091AA negates AUTOFD# when it is ready for a peripheral transfer and asserts AUTOFD# to indicate that it is receiving the data/command. AUTOFD# asserted causes the peripheral device to negate ACK#. The peripheral transfers are to the parallel port 16-byte FIFO.

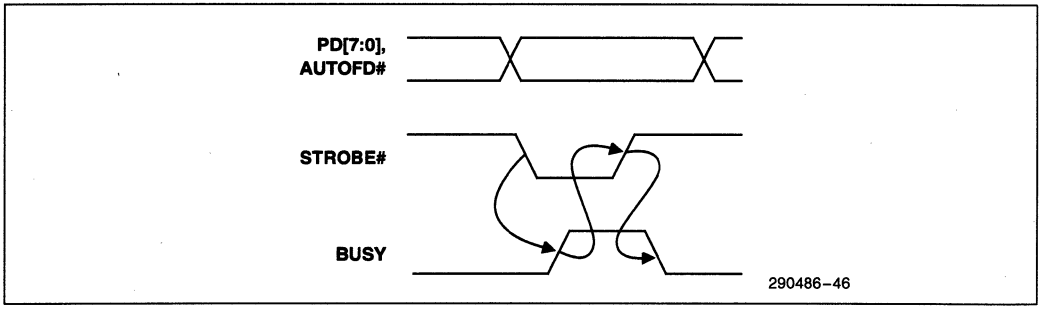


Figure 46. ECP Mode Handshake (Forward Direction)

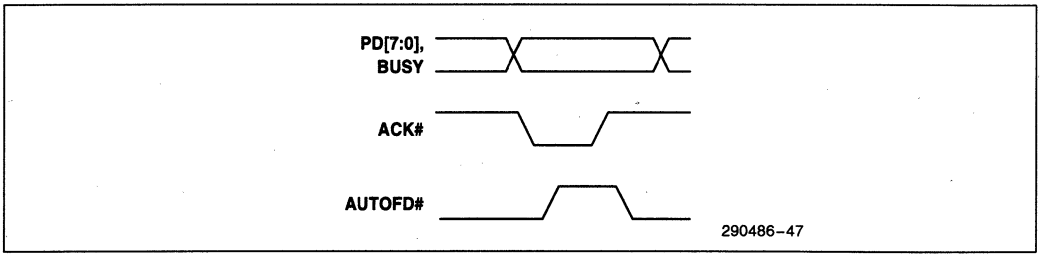


Figure 47. ECP Mode Handshake (Reverse Direction)

Test Mode (ECR[7:5] = 110) and Configuration Mode (ECR7:5] = 111)

The test mode can be used to check the FIFO read and write interrupt thresholds as described in Section 6.1.3.7, TFIFO—ECP Test FIFO Register. Note that for the 82091AA parallel port, the read and write FIFO interrupt thresholds are the same. The FIFO threshold is set by programming the PCFG1 Register in the 82091AA configuration space. The configuration mode is used to access the ECPCFGA and ECPCFGB Registers. This mode must first be set before the ECPCFGA and ECPCFGB Registers can be accessed.

6.2.3.1 FIFO Operations

The parallel port FIFO is used for ECP transfers (ECR[7:5] = 011), ISA-Compatible FIFO transfers (ECR[7:5] = 010), and Test mode (ECR[7:5] = 110). Either DMA or programmed I/O can be used for transfers between the host and the parallel port.

The FIFO threshold value is selected via the 82091AA configuration registers (PCFG1 Register). The threshold is set to either 1 (forward)/15 (reverse) or 8 in both directions. A threshold setting of 1 (forward)/15 (reverse) results in longer periods of time between service request, but requires faster servicing of both read and write requests. A threshold setting of 8 results in more service requests, but tolerates slower servicing of the requests.

In modes 010 and 011, an internal temporary holding register is used in conjunction with the 16-byte FIFO to provide 17 bytes of storage for both forward and reverse transfers. Thus, in the forward direction if the peripheral asserts the BUSY signal during the filling of the FIFO, the host needs to write 17 bytes before the FIFO full flag in the ECR is set to 1. In Test mode (110) only the 16-byte FIFO is used and the temporary holding register is not used.

The FIFO is reset by a hard reset (RSTDRV asserted) or whenever the parallel port is placed in ISA-Compatible or PS/2-Compatible modes. Note that the FIFO threshold can only be changed when the parallel port is in ISA-Compatible or PS/2-Compatible mode.

6.2.3.2 DMA Transfers

The 82091AA contains parallel port DMA request (PPDREQ) and acknowledge (PPDACK#) signals to communicate with a standard PC DMA controller. Before initiating a DMA transfer the direction bit in the PCON Register must be set to the proper direction. To initiate DMA transfers, software sets the DMAEN bit to 1 and the SERVICEINTR bit to 0 in the ECR. The PPDREQ and PPDACK# signals will then be used to fill (forward direction) or empty (reverse direction) the FIFO. When the DMA controller reaches terminal count and asserts the TC signal, an interrupt is generated and the SERVICEINTR bit is set to 1. To reset the TC interrupt, software can either switch the mode to 000 or 001 or write the DMAEN bit to 0.

In DMA mode, if 32 consecutive reads or writes are performed to the FIFO and PPDREQ is still asserted, the 82091AA negates PPDREQ for the length of the last PPDACK#/command pulse to force an arbitration cycle on the ISA Bus.

2

6.2.3.3 Reset FIFO and DMA Terminal Count Interrupt

The following operations are used to reset the parallel port FIFO and TC interrupt

Function	Reset Operations
FIFO	-Changing to modes 000 or 001 -Hard reset
FIFO Error	-Changing to modes 000 or 001 -Hard reset
TC Interrupt	-Changing to modes 000 or 001 -Setting DMAEN to 0 in ECR -Hard reset

6.2.3.4 Programmed I/O Transfers

Programmed I/O (non-DMA) can also be used for transfers between the host and the parallel port FIFO. Software can determine the read/write FIFO thresholds and the FIFO depth by accessing the FIFO in Test mode. To use programmed I/O transfers software sets the direction bit in the PCON Register to the desired direction and sets the DMAEN bit to 0 and the SERVICEINTR bit to 0 in the ECR. The parallel port requests programmed I/O transfers from the host by asserting IRQ5/IRQ7.

In the reverse direction an interrupt occurs when SERVICEINTR = 0 either 8 or 15 bytes (depending on threshold setting) are in the FIFO. IRQ5/IRQ7 can be used in an interrupt-driven system. The host must respond to the interrupt request by reading data from the FIFO.

In the forward direction an interrupt occurs when SERVICEINTR = 0 and there are either 8 or 1 byte locations available in the FIFO (depending on threshold setting). IRQ5/IRQ7 can be used in an interrupt-driven system. The host must respond to the interrupt request by writing data to the FIFO.

6.2.3.5 Data Compression

The 82091AA supports Run Length Encoded (RLE) decompression in hardware and can transfer compressed data to the peripheral. To transfer compressed data to the peripheral (forward direction), the compression count is written to the ECPAFIFO location and the data is written to the ECPDFIFO location. The most significant bit (bit 7) in the byte written to the ECPAFIFO Register informs the peripheral whether the value is a channel address (bit 7 = 1) or a run length count (bit 7 = 0). The RLE count in the ECPAFIFO (bits[6:0]) informs the peripheral of how many times the data in the ECPDFIFO is to be repeated. An RLE count of 0 indicates that only one byte of the data is present and a count of 127 indicates to the peripheral that the next byte should be expanded 128 times. An RLE count of 1 should be avoided as it will cause unnecessary expansions. Note that the 82091AA asserts AUTOFD# to indicate that PD[7:0] contains address/RLE instead of data.

In the reverse direction, the peripheral negates the BUSY signal to indicate that PD[7:0] contains address/RLE. During an address/RLE cycle, the 82091AA checks bit 7 to see if the next byte received needs to be decompressed. If bit 7 is 0, the 82091AA decompresses (replicates) the next data received by the RLE count received on bits[6:0].

6.2.4 PARALLEL PORT EXTERNAL BUFFER CONTROL

A multi-function signal (GCS#/PPDIR) is provided for controlling optional external parallel port data buffers. The PPDIR function is only available when the 82091AA configuration is in software motherboard (SWMB) mode. In this mode, this signal operates as a parallel port direction control signal (PPDIR). Note that, if any other configuration is used (SWAI, HWB, or HWE configuration modes), this multi-function signal operates as a game port chip select (GCS#). In SWMB, PPDIR is low when PD[7:0] are outputs and high when PD[7:0] are inputs. Figure 44 shows an example of external buffers being used when the parallel port is in ECP mode.

External buffering affects the ability of the port to read software security devices. Typically these software secutiry devices are designed to hold the data pins of the parallel port connector at either high or low logic levels when the pins are not being driven by the parallel port. The bit pattern read from the parallel port by the security software may not be correctly transferred through the external buffer.

6.2.5 PARALLEL PORT SUMMARY

Table 18 summarizes the parallel port interrupt, DMA, and parallel port signal drive type for the various modes of operation.

Table 18. Parallel Port Summary

Parallel Port Mode	ECR[7:5]	PD[7:0] Direction	Parallel Port Control Signals Controlled By PCON	IRQ Enable	DMA Enable
ISA-Compatible	000	Output	Open Drain	ACKINTEN	
PS/2-Compatible	001	Bi-directional	Open Drain	ACKINTEN	
EPP	N/A	Bi-directional	Push Pull	ACKINTEN	
ISA-Compatible FIFO	010	Output	Push Pull	Always Enabled	DMAEN
ECP	011	Bi-directional	Push Pull	Always Enabled	DMAEN
ECP Test	110	Output	Push Pull	Always Enabled	DMAEN
ECP Configuration	111	Bi-directional	Push Pull	ACKINTEN	DMAEN

NOTES:
1. The selected IRQ pin (IRQ5/IRQ7) is enabled if ACKINTEN is enabled in the PCON Register. Otherwise, the IRQ pin is tri-stated.
2. PPDREQ is enabled whenever the DMAEN bit is enabled in the ECR, independent of the parallel port mode.

7.0 SERIAL PORT

The two 82091AA serial ports are identical. This section describes the serial port registers and FIFO operations.

7.1 Register Description

The register descriptions in this section apply to both serial port A and serial port B and provide a complete operational description of the serial ports. Table 19 shows the I/O address assignments for the serial port registers. The individual register descriptions follow in the order that they appear in the table. Note that serial port interrupt assignments (IRQ3 or IRQ4) and the base address assignments are made by 82091AA configuration as described in Section 4.0, AIP Configuration.

All registers are accessed as byte quantities. The base address is determined by hardware configuration at powerup (or a hard reset) or via software configuration by programming the 82091AA configuration registers as described in Section 4.0, AIP Configuration. Note that access to certain serial port registers requires prior programming of the DLAB bit in the Line Control Register (LCR).

During a hard reset (RSTDRV asserted), the 82091AA registers are set to pre-determined **default** states. The default values are indicated in the individual register descriptions. Reserved bits in the 82091AA's serial port registers must be programmed to 0 when writing the register and these bits are 0 when read. The following bit notation is used for default settings:

X Default bit position value is determined by conditions on an 82091AA signal pin.

The following nomenclature is used for serial port register access attributes:

RO **Read Only**. Note that for all registers with read only attributes, writes to the I/O address access a different register.

WO **Write Only**. Note that for all registers with write only attributes, reads to the I/O address access a different register.

R/W **Read/Write**. A register with this attribute can be read and written. Note that some read/write registers contain bits that are read only.

Table 19. Serial Port Registers

Register Address Access (AEN = 0)		Abbreviation	Register Name	Access
Base +	DLAB			
0h	0	THR	Transmit Holding Register	WO
0h	0	RBR	Receiver Buffer Register	RO
0h	1	DLL	Divisor Latch LSB	R/W
1h	1	DLM	Divisor Latch MSB	R/W
1h	0	IER	Interrupt Enable Register	R/W
2h	—	IIR	Interrupt Identification Register	RO
2h	—	FCR	FIFO Control Register	WO
3h	—	LCR	Line Control Register	R/W
4h	—	MCR	Modem Control Register	R/W
5h	—	LSR	Line Status Register	R/W
6h	—	MSR	Modem Status Register	R/W
7h		SCR	Scratch Pad Register	R/W

Table 20. Serial Port Register Summary

Bit #	Receiver Buffer Register	Transmitter Holding Register	Interrupt Enable Register	Interrupt Identification Register	FIFO Control Register	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt	0 if Interrupt Pending	FIFO Enable	Word Length Select Bit 0
1	Data Bit 1	Data Bit 1	Enable XMTR Holding Register Empty Interrupt	Interrupt ID Bit	RCVR FIFO Reset	Word Length Select Bit 1
2	Data Bit 2	Data Bit 2	Enable RCVR Line Status Interrupt	Interrupt ID Bit	XMIT FIFO Reset	Number of Stop Bits
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt	Interrupt ID Bit (Non-FIFO = 0)	DMA Mode Select	Parity Enable
4	Data Bit 4	Data Bit 4	0	0	Reserved	Event Parity Select
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Non-FIFO = 0)	RCVR Trigger (LSB)	Set Break
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Non-FIFO = 0)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)

Table 20. Serial Port Register Summary (Continued)

Bit #	Modem Control Register	Line Status Register	Modem Status Register	ScratchPad Register	Divisor Latch - MSB	Divisor Latch - LSB
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready	Bit 1	Bit 1	Bit 9
2	Out 1 Bit	Parity Error (PE)	Trailing Edge Ring Indicator	Bit 2	Bit 2	Bit 10
3	IRQ Enable	Framing Error (FE)	Delta Data Carrier Detect	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

7.1.1 THR(A,B)—TRANSMITTER HOLDING REGISTER

I/O Address: Base +0h (DLAB=0)
Default Value: 00h
Attribute: Write Only
Size: 8 bits

The THR contains data to be transmitted out on the SOUT[A,B] signal line. Bit 0 is the least significant bit and is the first bit serially transmitted. If the serial word length is less than 8 bits (as selected in the LCR), the data word must be written to this register right-justified. Bit positions above the number of bits selected for the word size are discarded (not transmitted).

Bit	Description
7:0	**Transmit Data:** Bits[7:0] correspond to SD[7:0].

7.1.2 RBR(A,B)—RECEIVER BUFFER REGISTER

I/O Address: Base +0h (DLAB=0)
Default Value: 00h
Attribute: Read Only
Size: 8 bits

The RRB contains data received from the SIN[A,B] signal line. Bit 0 is the least significant bit and is the first bit serially received. If the serial word length is less than 8 bits (as selected in the LCR), the data word in this register is right-justified. Bit positions above the number of bits selected for the word size are 0.

Bit	Description
7:0	**Receiver Data:** Bits[7:0] correspond to SD[7:0].

7.1.3 DLL(A,B), DLM(A,B)—DIVISOR LATCHES (LSB AND MSB) REGISTERS

I/O Address: Base +0h,1h (DLAB=1)
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The 82091AA contains two independently programmable baud rate generators. The 24 MHz crystal oscillator frequency input is divided by 13, resulting in a frequency of 1.8462 MHz. This frequency is the input to each baud rate generator and is divided by the divisor of the associated serial port. The output frequency of the baud rate generator (BOUT[A,B]) is 16 x the baud rate.

$$\text{divisor } \# = (\text{frequency input})/(\text{baud rate} \times 16)$$

The output of each baud rate generator drives the transmitter and receiver sections of the associated serial port. Two 8-bit latches per serial port store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is loaded. Table 21 provides decimal divisors to use with crystal frequencies of 24 MHz. Using a divisor of zero is not recommended.

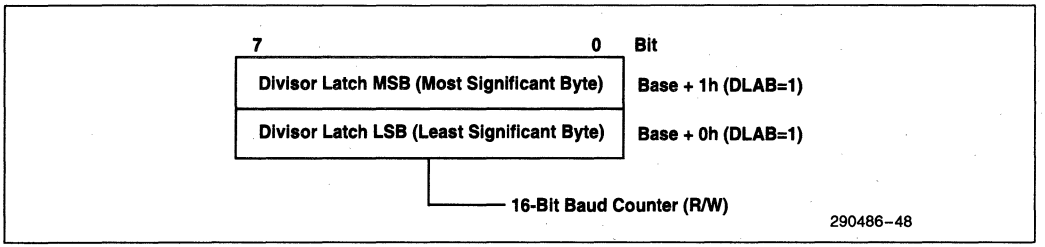


Figure 48. Divisor Latches (LSB and MSB) Registers

Bit	Description
7:0	**Divisor Latch Data:** Bits[7:0] correspond to SD[7:0].

Table 21. AIP Serial Port A and B Divisors, Baud Rates, and Clock Frequencies

	24 MHz Input Divided to 1.8461 MHz	
Baud Rate	**Decimal Divisor for 16x Clock**	**Percent Error**
50	2304	0.1
75	1536	
110	1047	
134.5	857	0.4
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.5
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	3.0
115200	1	—

7.1.4 IER(A,B)—INTERRUPT ENABLE REGISTER

I/O Address: Base + 1h (DLAB = 0)
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

This register enables/disables interrupts for five types of serial port conditions. If a particular condition occurs whose interrupt is disabled in this register, the corresponding interrupt status bit in the IIR will not be set and an interrupt request (IRQ3 or IRQ4) will not be generated.

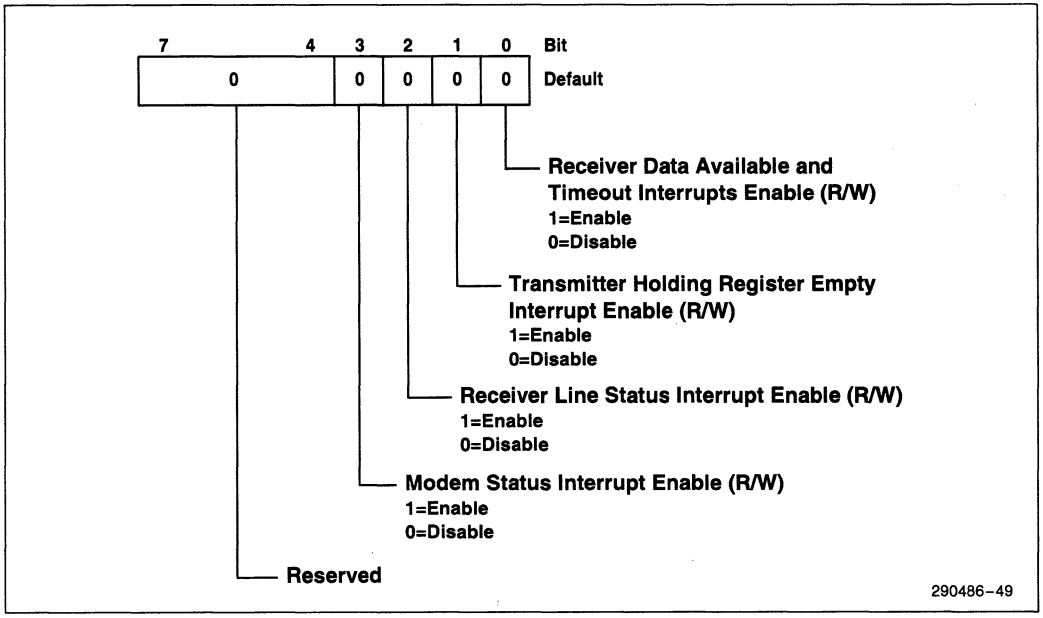


Figure 49. Interrupt Enable Register

Bit	Description
7:4	**RESERVED**
3	**MODEM INTERRUPT ENABLE (MIE):** When MIE = 1, the Modem Status Interrupt is enabled. When MIE = 0, the Modem Status Interrupt is disabled.
2	**RECEIVER INTERRUPT ENABLE (RIE):** When RIE = 1, the Receiver Line Status interrupt is enabled. When RIE = 0, the receiver line status interrupt is disabled.
1	**TRANSMITTER HOLDING REGISTER EMPTY INTERRUPT ENABLE (THEIE):** When THREIE = 1, the Transmitter Holding Register Empty Interrupt is enabled. When THREIE = 0, the Transmitter Holding Register Empty Interrupt is disabled.
0	**RECEIVER DATA AVAILABLE INTERRUPT ENABLE AND TIMEOUT INTERRUPT ENABLE IN FIFO MODE (RAVIE):** When RAVIE = 1, the Received Data Available Interrupt is Enabled. When RAVIE = 0, the Received Data Available Interrupt is disabled. In addition, in the FIFO Mode, this bit enables the Timeout Interrupt when set to 1 and disables the Timeout Interrupt when set to 0.

7.1.5 IIR(A,B)—INTERRUPT IDENTIFICATION REGISTER

I/O Address: Base + 2h
Default Value: 01h
Attribute: Read Only
Size: 8 bits

This register provides interrupt status and indicates whether the serial port receive/transmit FIFOs are enabled (FIFO mode) or disabled (non-FIFO mode). In order to provide minimum software overhead during data character transfers, the serial port prioritizes interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and Modem Status. When the CPU accesses the IIR, the serial port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the serial port records new interrupts, but does not change its current indication until the current access is complete.

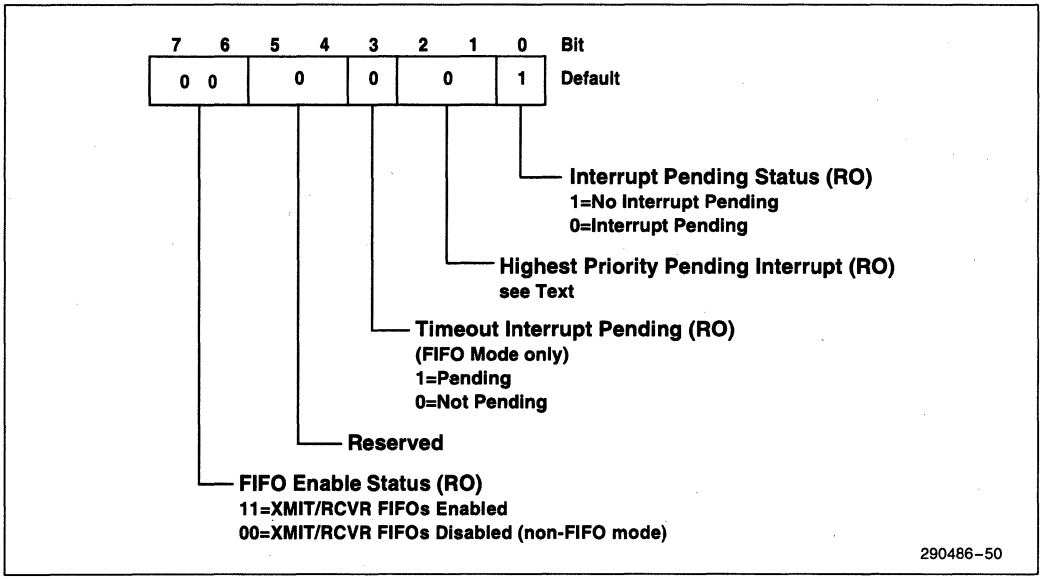


Figure 50. Interrupt Identification Register

Bit	Description
7:6	**FIFO MODE ENABLE STATUS (FIFOES):** This status field indicates whether the serial port is in FIFO mode or non-FIFO mode (FIFO/non-FIFO mode is selected via the FCR). When FIFOES = 11, the serial port is in FIFO mode (FIFOs enabled). When FIFOES = 00, the serial port is in non-FIFO mode (FIFOs disabled). The 82091AA never sets this field to either = 01 or 10.
5:4	**RESERVED**
3	**TIMEOUT INTERRUPT PENDING (TOUTIP)—FIFO MODE ONLY:** In the non-FIFO mode, this bit is 0. In FIFO mode TOUTIP is set to 1 when no characters have been removed from or input to the receive FIFO during the last 4 character times and there is at least 1 character in the FIFO during this time. When a timeout interrupt is pending, the 82091AA sets this bit along with bit 2 of this register.
2:1	**HIGHEST PRIORITY INTERRUPT INDICATOR:** This field identifies the highest priority interrupt pending as indicated in Table 22.
0	**INTERRUPT PENDING STATUS (IPS):** This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When IPS = 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When IPS = 1, no interrupt is pending.

Table 22. Interrupt Priority

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error, or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed from or Input to the RCVR FIFO during the Last 4 Char. Times and there is at least 1 Char. in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source or Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect.	Reading the Modem Status Register

7.1.6 FCR(A,B)—FIFO CONTROL REGISTER

I/O Address: Base +2h
Default Value: 00h
Attribute: Write Only
Size: 8 bits

FCR is a write only register that is located at the same address as the IIR (the IIR is a read only register). FCR enables/disables the transmit/receive FIFOs, clears the transmit/receive FIFOs, and sets the receive FIFO trigger level.

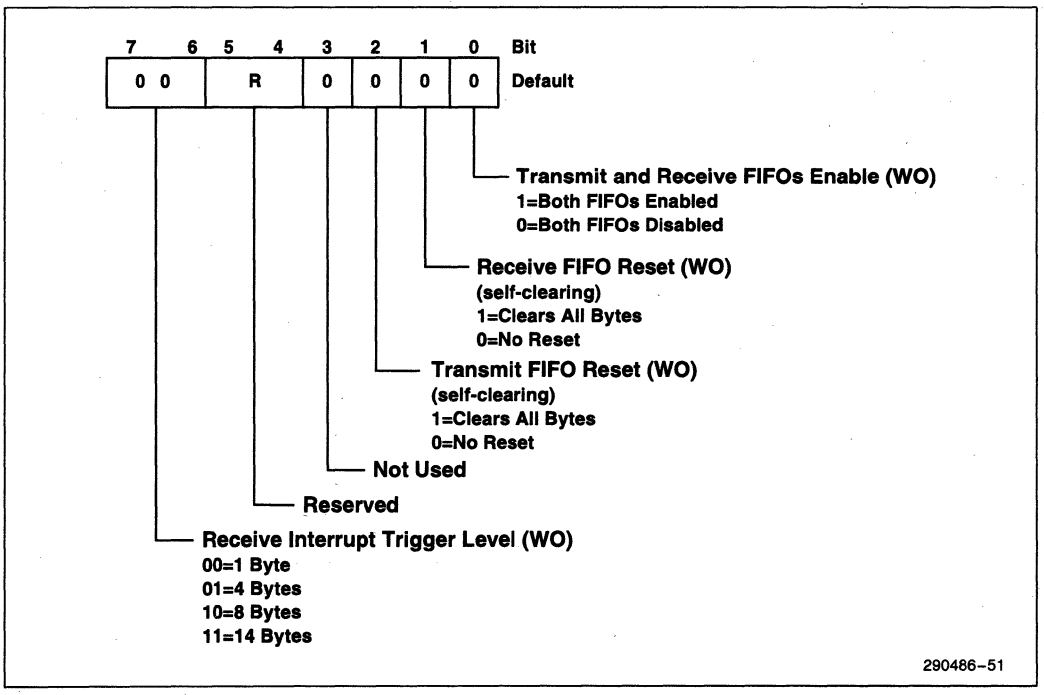


Figure 51. FIFO Control Register

Bit	Description
7:6	**INTERRUPT TRIGGER LEVEL (ITL):** The ITL field indicates the interrupt trigger level. When the number of bytes in the receive FIFO equals the interrupt trigger level programmed into this field and the Received Data Available Interrupt enabled (via the IER), an interrupt will be generated and the appropriate bits set in the IIR. **Bits [7:6] — Trigger Level (Bytes)** 0 0 — 01 (default) 0 1 — 04 1 0 — 08 1 1 — 14
5:4	**RESERVED**
3	**NOT USED:** Writing to this bit causes no change in serial port operations. The serial port does not support DMA operations. Note that the TXRDY# and RXRDY# pins are not available in the 82091AA.
2	**RESET TRANSMITTER FIFO (RESETTF):** When RESETTF is set to a 1, the FIFO counter is set to 0. The shift register is not cleared. When the FIFO is cleared, the 82091AA sets this bit to 0.
1	**RESET RECEIVER FIFO (RESETRF):** When RESETRF is set to a 1, the FIFO counter is set to 0. The shift register is not cleared. When the FIFO is cleared, the 82091AA sets this bit to 0.
0	**TRANSMIT AND RECEIVE FIFO ENABLE (TRFIFOE):** TRFIFOE enables/disables the transmit and receive FIFOs. When TRFIFOE = 1, both FIFOs are enabled (FIFO Mode). When TRFIFOE = 0, the FIFOs are both disabled (non-FIFO MODE). Writing a 0 to this bit clears all bytes in both FIFOs. When changing from FIFO mode to non-FIFO mode and vice versa, data is automatically cleared from the FIFOs. This bit must be written with a 1 when other bits in this register are written or the other bits will not be programmed.

7.1.7 LCR(A,B)—LINE CONTROL REGISTER

I/O Address: Base + 3h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

This register specifies the format of the asynchronous data communications exchange. LCR also enables/disables access to the Baud Rate Generator Divisor latches or the Transmitter Data Holding Register, Receiver Buffer Register, and Interrupt Enable Register.

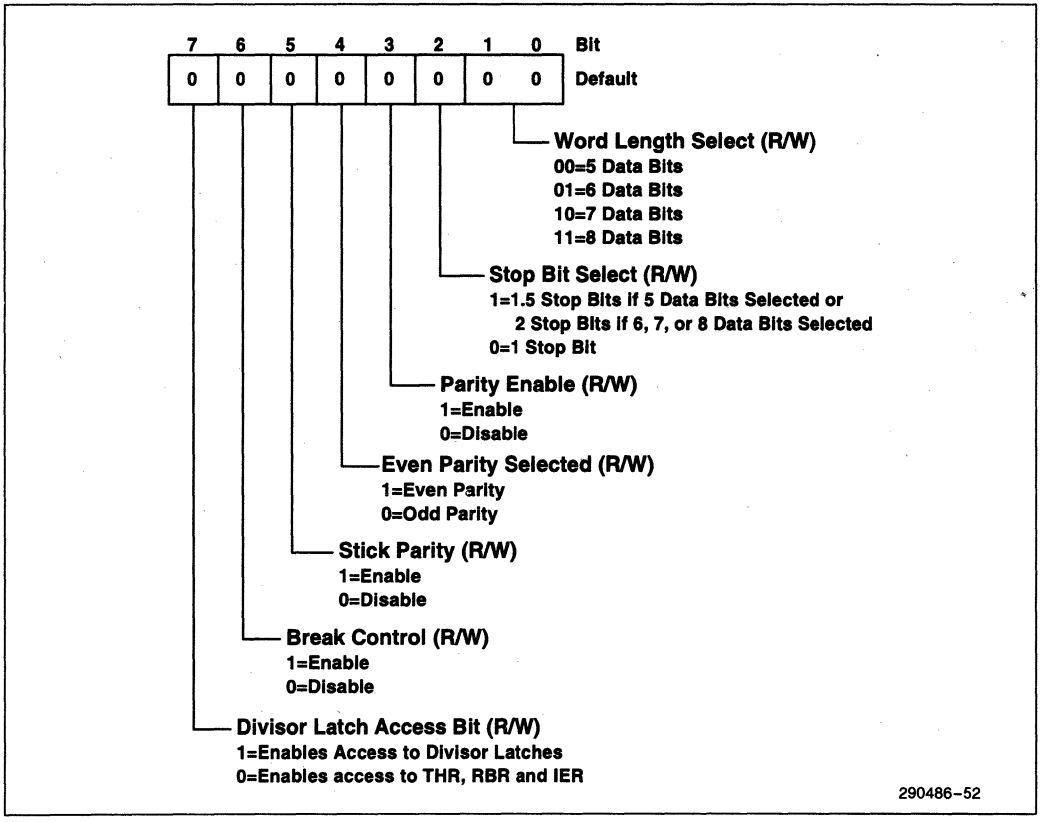


Figure 52. Line Control Register

Bit	Description
7	**DIVISOR LATCH ACCESS BIT (DLAB):** DLAB controls access to the Baud Rate Generator Divisor Latches (and to the Transmit Holding Register, Receiver Buffer Register and Interrupt Enable Register which are located at the same I/O addresses). When DLAB = 1, access to the two Divisor Latches is selected and access to the THR, RBR, and IER is disabled. When DLAB = 0, access to the two Divisor Latches is disabled and access to the THR, RBR, and IER is selected. During test mode operations, DLAB must be set to 1 for the BOUT signal to appear on the SOUT pin.
6	**BREAK CONTROL (BRCON):** When BRCON = 1, a break condition is transmitted from the 82091AA serial port to the receiving device. When BRCON = 1, the serial output (SOUT) is forced to the 'spacing' state (logical 0). BRCON only affects the SOUT signal and has no effect on the transmitter logic. Note that this feature permits the CPU to alert a terminal. If the following sequence is used, no erroneous characters will be transmitted because of the break. 1. Wait for the transmitter to be idle (TEMT = 1). 2. Set break (BRCON = 1) for the appropriate amount of time. If the transmitter will be used to time the break duration, then check that TEMT = 1 before clearing the BRCON. 3. Clear break (BRCON = 0) when normal transmission has to be restored. During the break, the transmitter can be used as a character timer to accurately establish the break duration by sending characters and monitoring THRE and TEMT.
5	**STICKY PARITY (STICPAR):** STICPAR is the Stick Parity bit. When parity is enabled (PAREN = 1) this bit is used in conjunction with EVENPAR to select "Mark" or "Space" Parity. When bits PAREN, EVENPAR and STICPAR are 1, the parity bit is transmitted and checked as a 0 (Space Parity). If bits PAREN and STICPAR are 1 and EVENPAR is 0, the parity bit is transmitted and checked as a 1 (Mark Parity). When STICPAR = 0, stick parity is disabled.
4	**EVEN PARITY SELECT (EVENPAR):** EVENPAR selects between even and odd parity. When parity is enabled (PAREN = 1) and EVENPAR = 0, an odd number of 1s is transmitted or checked in the data word bits and parity bit. When parity is enabled and EVENPAR = 1, an even number of 1s is transmitted or checked.
3	**PARITY ENABLE (PAREN):** This bit enables/disables parity generation and checking. When PAREN = 1, a parity bit is generated (transmit data) or checked (receive data) between the last data bit and stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data bits and the Parity bit are summed.) When PAREN = 0, parity generation and checking is disabled.
2	**STOP BITS (STOPB):** This bit specifies the number of stop bits transmitted with each serial character. When STOPB = 0, one stop bit is generated in the transmitted data. When STOPB = 1 and a 5-bit data length is selected, one and a half stop bits are generated. When STOPB = 1 and either a 6-, 7-, or 8-bit data length is selected, two stop bits are generated. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.
1:0	**SERIAL DATA BITS (SERIALDB):** This field specifies the number of data bits in each transmitted or received serial character as follows: **Bits[1:0] — Data Length** 0 0 — 5 Bits - Default 0 1 — 6 Bits 1 0 — 7 Bits 1 1 — 8 Bits

2

7.1.8 MCR(A,B)—MODEM CONTROL REGISTER

I/O Address: Base + 4h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

This register controls the interface with the modem or data set (or a peripheral device emulating a modem).

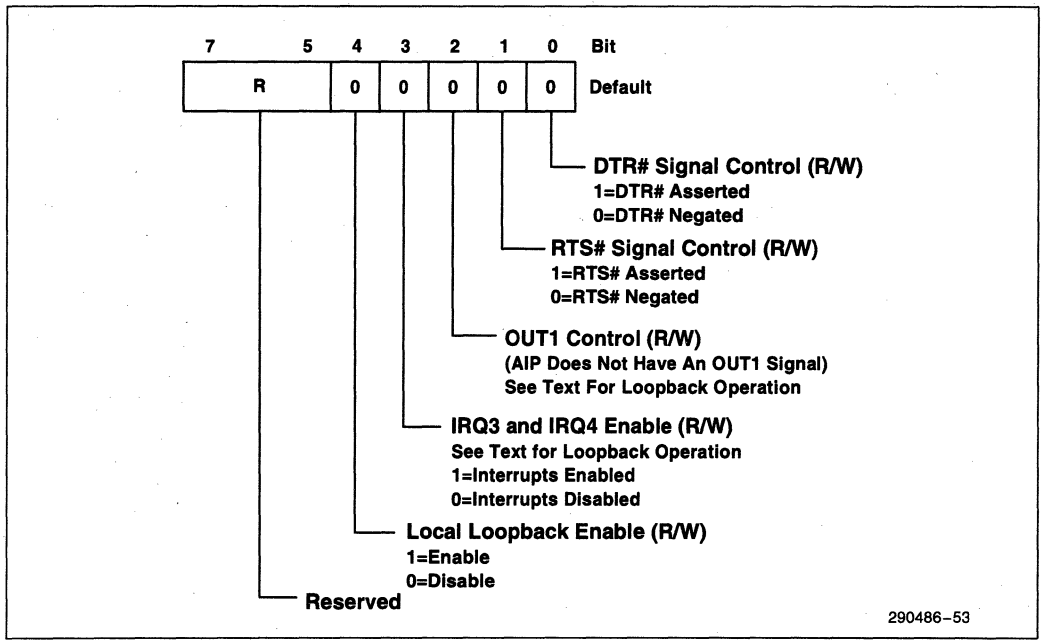


Figure 53. Modem Control Register

Bit	Description
7:5	**RESERVED**
4	**LOOPBACK MODE ENABLE (LME):** LME provides a local loopback feature for diagnostic testing of the serial port module. When LME = 1, the following occurs: 1. The transmitter Serial Output (SOUT) is set to the Marking (logic 1) state. 2. The receiver Serial Input (SIN) is disconnected. 3. The output of the Transmitter Shift Register is "looped back"(connected) to the Receiver Shift Register. 4. The four modem control inputs (DSR#, CTS#, RI and DCD#) are disconnected. 5. The DTRC, RTSC, OUT1C, IE bits in the MCR are internally connected to DSRS, CTSS, RIS, and DCDS in MSR, respectively. 6. The modem control output pins are forced to their high (inactive) state. 7. Data that is transmitted is immediately received. This feature allows the CPU to verify the transmit and received data paths of the serial port. In the loopback mode, the receiver and transmitter interrupts are fully operational. The modem status interrupts are fully operational. The modem status interrupts are also operational, but the interrupt sources are the lower four bits of MCR instead of the four modem control inputs. Writing a 1 to any of these 4 MCR bits (bits[3:0]) causes an interrupt. In Loopback Mode the interrupts are still controlled by the Interrupt Enable Register. The IRQ3 and IRQ4 signal pins are tri-stated in the loopback mode.
3	**INTERRUPT ENABLE (IE):** When IE = 1, the associated interrupt is enabled (either IRQ3 or IRQ4 as selected via the associated serial port configuration register - A or B). In Local Loopback Mode, this bit controls bit 7 of the Modem Status Register.
2	**OUT1 BIT CONTROL (OUT1C):** This bit is the OUT1 bit. It does not have an output pin associated with it. It can be written to and read by the CPU. In Local Loopback Mode, this bit controls bit 6 of the Modem Status Register.
1	**REQUEST TO SEND CONTROL (RTS):** This bit controls the Request to Send (RTS#) output. When RTSC = 1, the RTS# output is asserted. When RTSC = 0, the RTS# output is negated. In Local Loopback Mode, this bit controls bit 4 of the Modem Status Register.
0	**DATA TERMINAL READY CONTROL (DTRC):** This bit controls the Data Terminal Ready (DTR#) output. When DTRC = 1, the DTR# output is asserted. When DTRC = 0, the DTR# output is negated. In Local Loopback Mode, this bit controls bit 5 of the Modem Status Register. **NOTE:** The DTR# and RTS# outputs of the serial port may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the modem or data set.

7.1.9 LSR(A,B)—LINE STATUS REGISTER

I/O Address: Base + 5h
Default Value: 60h
Attribute: Read/Write
Size: 8 bits

This 8-bit register provides data transfer status information to the CPU. Note that the Line Status Register is intended for read operations only. Writing to this register is not recommended and could result in unintended operations. For this reason, the figure shows these bits as RO (read only).

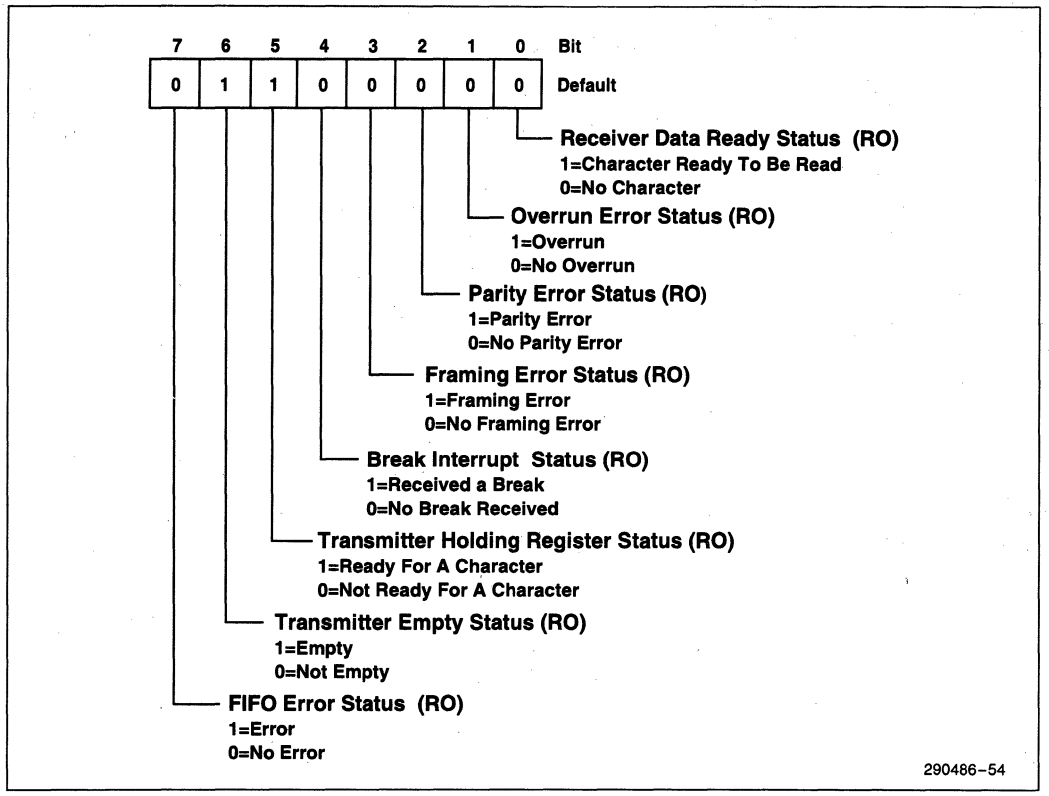


Figure 54. Line Status Register

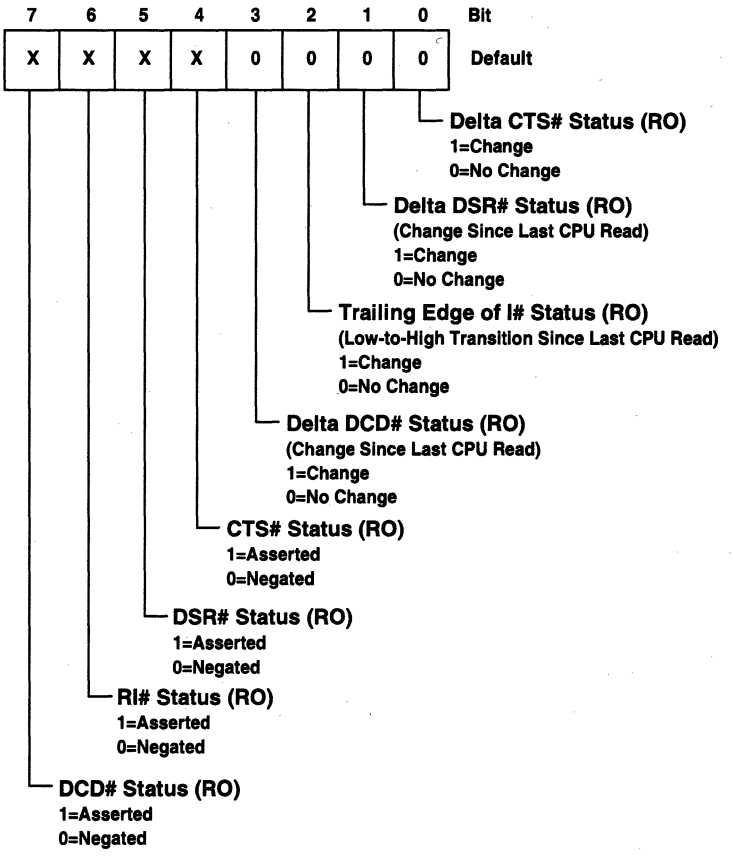
Bit	Description
7	**FIFO ERROR STATUS (FIFOE):** In the non-FIFO Mode this is a 0. In the FIFO Mode, FIFOE is set to 1 when there is at least one parity error, framing error, or break indication in the FIFO. FIFOE is set to 0 when the CPU reads the LSR, if there are no subsequent errors in the FIFO.
6	**TRANSMITTER EMPTY STATUS (TEMT):** This bit is the Transmitter Empty (TEMT) indicator. When the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty, the 82091AA sets TEMT to a 1. When either the THR or TSR contains a data character, TEMT is set to a 0. The default is 0. In FIFO mode, this bit is set to 1 when the transmitter FIFO and the shift register are both empty.

Bit	Description
5	**TRANSMITTER HOLDING REGISTER STATUS (THRE):** This bit is the Transmitter Holding Register Empty (THRE) indicator. THRE indicates that the serial port module is ready to accept a new character for transmission. In addition, this bit causes the serial port module to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set to a 1. THRE is set to 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. THRE is set to 0 when the CPU loads the Transmitter Holding Register. In the FIFO mode, this bit is set to a 1 when the transmit FIFO is empty, and is set to 0 when at least 1 byte is written to the transmit FIFO.
4	**BREAK INTERRUPT STATUS (BI):** This bit is the Break Interrupt (BI) indicator. BI is set to a 1 when the received data input is held in the Spacing state (logic 0) for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). When the CPU reads the contents of the Line Status Register, BI is set to 0. In FIFO mode, this error is associated with the particular character in the FIFO associated with the Break. BI is indicated to the CPU when its associated character is at the top of the FIFO. When break occurs only one character is loaded into the FIFO. Restarting after a break is received requires the SIN pin to be a logical 1 for at least ½ bit times. **NOTE:** Bits[3:0] are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and that interrupt is enabled.
3	**FRAMING ERROR STATUS (FE):** This bit is the Framing Error (FE) indicator. FE indicates that the received character did not have a valid stop bit. FE is set to a 1 when the stop bit following the last data bit or parity bit is 0 (spacing level). FE is set to 0 when the CPU reads the contents of the Line Status Register. In FIFO mode, this error is associated with the particular character in the FIFO that it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a framing error is due to the next start bit, the serial port attempts to resynchronize. In this case, the serial port module samples this start bit twice and, if no FE exists, then the module takes in the rest of the bits.
2	**PARITY ERROR STATUS (PE):** This bit is the Parity Error (PE) indicator. PE indicates that the received data character does not have the correct even or odd parity, as selected by the EVENPAR bit in the Line Status Register. When a parity error is detected, PE is set to 1. PE is set to 0 when the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO that it applies to. This error is indicated to the CPU when its associated character is at the top of the FIFO.
1	**OVERRUN ERROR STATUS (OE):** OE indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register. In this case, the previous character is overwritten. When an overrun is detected, OE is set to 1. when the CPU reads the Line Status Register, OE is set to 0. This bit is read only. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is completely full and the next character has been received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.
0	**RECEIVER DATA READY STATUS (DR):** DR is set to 1 when a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. When the data in the Receiver Buffer Register or FIFO is read, DR is set to 0. This bit is read only.

7.1.10 MSR(A,B)—MODEM STATUS REGISTER

I/O Address: Base + 6h
Default Value: XXXX 0000
Attribute: Read/Write
Size: 8 bits

The MSR provides the current state of the control lines from the Modem (or peripheral device) to the CPU. Bits[7:4] provide the status of the DCD#, RI, DSR#, and CTS# Modem signals. In addition to the current-state information of the Modem signals, bits[3:0] provide change information for these signals. Bits[3:0] are set to a 1 when the corresponding input signal changes state. Bits[3:0] are set to a 0 when the CPU reads the Modem Status Register.



NOTE:
X = Value determined by state of the corresponding modem control signal.

Figure 55. Modem Status Register

Bit	Description
7	**DATA CARRIER DETECT STATUS:** This bit is the compliment of the Data Carrier Detect (DCD#) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to IRQ ENABLE in the MCR.
6	**RING INDICATOR STATUS:** This bit is the compliment of the Ring Indicator (RI) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.
5	**DATA SET READY STATUS:** This bit is the compliment of the Data Set Ready (DSR#) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.
4	**CLEAR TO SEND STATUS:** This bit is the compliment of the Clear to Send (CTS#) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
3	**DELTA DATA CARRIER DETECT STATUS:** This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the DCD# input to the chip has changed state. **NOTE:** Whenever bit 0, 1, 2, or 3 is set to logic 1, a Modem Status Interrupt is generated.
2	**TRAILING EDGE OF RING INDICATOR STATUS:** This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the RI# input to the chip has changed from a low to a high state.
1	**DELTA DATA SET READY STATUS:** This bit is the Delta Data Set Ready (DDSR) indictor. Bit 1 indicates that the DSR# input to the chip has changed state since the last time it was read by the CPU.
0	**DELTA CLEAR TO SEND STATUS:** This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS# input to the chip has changed state since the last time it was read by the CPU.

7.1.11 SCR(A,B)—SCRATCHPAD REGISTER

I/O Address: Base + 7h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

This 8-bit read/write register does not control the serial port module in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Bit	Description
7:0	**SCRATCHPAD DATA:** Bits[7:0] of this register correspond to SD[7:0].

7.2 FIFO Operations

This section describes the FIFO operations for interrupt and polled modes.

7.2.1 FIFO INTERRUPT MODE OPERATION

When the Receive FIFO and receiver interrupts are enabled (FCR0 = 1 and IER0 = 1), receiver interrupts occur as follows:

1. The receive data available interrupt is invoked when the FIFO has reached its programmed trigger level. The interrupt is cleared when the FIFO drops below the programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, the bits are cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR-06h), as before, has higher priority than the received data available (IIR = 04h) interrupt.
4. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the receive FIFO. This bit is set to 0 when the FIFO is empty.

When receiver FIFO and receiver interrupts are enabled, receiver FIFO timeout interrupts occur as follows:

1. A FIFO timeout interrupt occurs, if the following conditions exist:
   a. At least one character is in the FIFO.
   b. The most recent serial character received was longer than 4 continous character times ago (if 2 stop bits are programmed, the second one is included in this time delay).
   c. The most recent CPU read of the FIFO was longer than 4 continous character times ago.

   The maximum time between a received character and a timeout interrupt is 160 ms at 300 baud with a 12-bit receive character (i.e., 1 start, 8 data, 1 parity, and 2 stop bits).
2. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
3. When a timeout interrupt occurs, it is cleared and the timer reset when the CPU reads one character from the receiver FIFO.
4. When a timeout interrupt does not occur, the timeout timer is reset after a new character is received or after the CPU reads the receiver FIFO.

When the transmit FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1), transmit interrupts occur as follows:

1. The transmitter holding register interrupt occurs when the transmit FIFO is empty. The interrupt is cleared as soon as the transmitter holding register is written (1 to 16 characters may be written to the transmit FIFO while servicing the interrupt) or the IIR is read.

Character timeout and receiver FIFO trigger level interrupts have the same priority as the current received data available interrupt. Transmit FIFO empty has the same priority as the current transmitter holding register empty interrupt.

7.2.2 FIFO POLLED MODE OPERATION

With FIFO = 1, setting IER[3:0] to all 0s puts the serial port in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately, either one or both can be in the polled mode of operation.

In this mode, software checks receiver and transmitter status via the LSR. As stated in the register description:

- LSR0 is set as long as there is one byte in the receiver FIFO.
- LSR1 and LSR4 specify which error(s) has occurred. Character error status is handled the same way as interrupt mode. The IIR is not affected since IER2 = 0.
- LSR5 indicates when the transmitter FIFO is empty.
- LSR6 indicates that both the transmitter FIFO and shift register are empty.
- LSR7 indicates whether there are any errors in the receiver FIFO.

8.0 FLOPPY DISK CONTROLLER

The 82091AA's Floppy Disk Controller (FDC) is functionally compatible with 82078/82077SL/82077AA/8272A floppy disk controllers. During 82091AA configuration, the FDC can be configured for either two drive support or four drive support via the FCFG1 Register. This section provides a complete description of the FDC when it is configured for two drive support. Additional information on four drive support is provided in Appendix A, FDC Four Drive Support.

NOTE:
For FDC compatibility and programming guidelines, refer to the 82078 Floppy Disk Controller Data sheet.

8.1 Floppy Disk Controller Registers

The FDC contains seven status, control, and data registers. Table 23 shows the I/O address assignments for the FDC registers and the individual register descriptions follow in the order that they appear in the table. The registers provide control/status information and data paths for transfering data between the floppy disk controller interface and the 8-bit host interface. In some cases, two different registers occupy the same I/O address. In these cases, one register is read only and the other is write only (i.e., a read to the I/O address accesses one register and a write accesses the other register).

All registers are accessed as byte quantities. The base address is determined by hardware configuration at powerup (or a hard reset) or via software configuration by programming the 82091AA configuration registers as described in Section 4.0, AIP Configuration.

During a hard reset (RSTDRV asserted), the 82091AA registers are set to pre-determined **default** states. The default values are indicated in the individual register descriptions. Reserved bits in the FDC registers must be programmed to 0 when writing the register and these bits are 0 when read. The following bit notation is used for default settings:

X Default bit position value is determined by conditions on an 82091AA signal pin.

The following nomenclature is used for register access attributes:

RO **Read Only.** Note that for registers with read only attributes, writes to the I/O address have no affect on floppy disk operations.

WO **Write Only.** Note that for all FDC registers with write only attributes, reads of the I/O address access a different register.

R/W **Read/Write.** A register with this attribute can be read and written. Note that individual bits in some read/write registers may be read only.

Table 23 lists the register accesses that bring the FDC out of a powerdown state. All other registers accesses are possible without waking the part from a powerdown state and reads from these registers reflects the true status as shown in the register description. For writes that do not affect the powerdown state, the FDC retains the data and will subsequently reflect it when the FDC awakens. Note that for accesses that do not affect powerdown, the access may cause a temporary increase in FDC power consumption. The FDC reverts back to low power mode when the access has been completed. None of the extended registers effect the behavior of the powerdown mode.

Table 23. Floppy Disk Controller Registers(1)

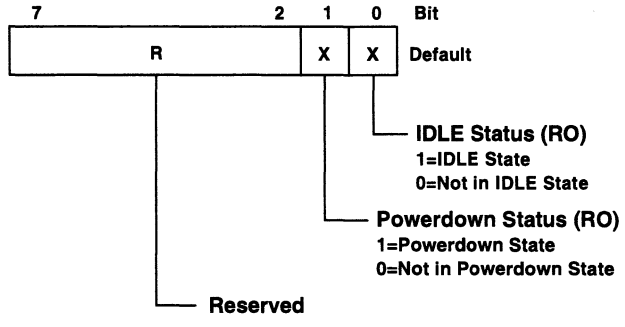
FDC Register Address Access Base +	Abbreviation	Register Name	Access Wakes Up FDC	Access
0h	—	Reserved	—	—
1h	SRB	Status Register B	No	RO
2h	DOR	Digital Output Register	No(2)	R/W
3h	TDR	Tape Drive Register	No	R/W
4h	MSR	Main Status Register	Yes	RO
4h	DSR	Datarate Select Register	No(2)	WO
5h	FIFO	Data FIFO	Yes	R/W
6h	—	Reserved	—	—
7h	DIR#	Digital Input Register	No	RO
7h	CCR	Configuration Control Register		WO

NOTES:
1. The base address is 3F0h (primary address) or 370 (secondary address).
2. While writing to the DOR or DSR does not wake up the FDC, writing any of the motor enable bits in the DOR or invoking a software reset (either via DOR or DSR reset bits) will wake up the FDC.

8.1.1 SRB—STATUS REGISTER B (EREG EN = 1)

I/O Address: Base + 1h
Default Value: RRRR RRXX
Attribute: Read/Write
Size: 8 bits

SRB provides status and control information when auto powerdown is enabled. In the AT/EISA mode the SRB is made available whenever the EREG EN bit in the POWERDOWN MODE Command is set to 1. When EREG EN bit is set to 0, this register is not accessible. In this case, writes have no affect and reads return indeterminate values.



NOTE:
X = Value is determined by the state of the corresponding signal pin.

Figure 56. Status Register B

Bit	Description
7:2	**RESERVED**
1	**POWERDOWN STATUS (PD):** This bit reflects the powerdown state of the FDC module. The 82091AA sets PD to 1 when the FDC is in the powerdown state. When PD = 0, the FDC is not in the powerdown state.
0	**IDLE STATUS (IDLE):** This bit reflects the idle state of the FDC module. The 82091AA sets IDLE to 1 when the FDC is in the idle state. When IDLE = 0, the FDC is not in the idle state.

8.1.2 DOR—DIGITAL OUTPUT REGISTER

I/O Address: Base +2h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The Digital Output Register enables/disables the floppy disk drive motors, selects the disk drives, enables/disables DMA, and provides a FDC module reset. The DOR reset bit and the motor enable bits have to be inactive when the FDC is in powerdown. The DMAGATE# and drive select bits are unchanged. During powerdown, writing to the DOR does not wake up the FDC, except for activating any of the motor enable bits. Setting the motor enable bits to 1 wakes up the FDC.

NOTES:

1. The descriptions in this section for DOR only apply when two-drive support is selected in the FCFG1 Register (FDDQTY = 0). For four-drive support (FDDQTY = 1), refer to Appendix A, FDC Four Drive Support.
2. The drive motor can be enabled separately without selecting the drive. This permits the motor to come up to speed before selecting the drive. Note also that only one drive can be selected at a time. However, the drive should not be selected without enabling the appropriate drive motor via bits[5:4] of this register.

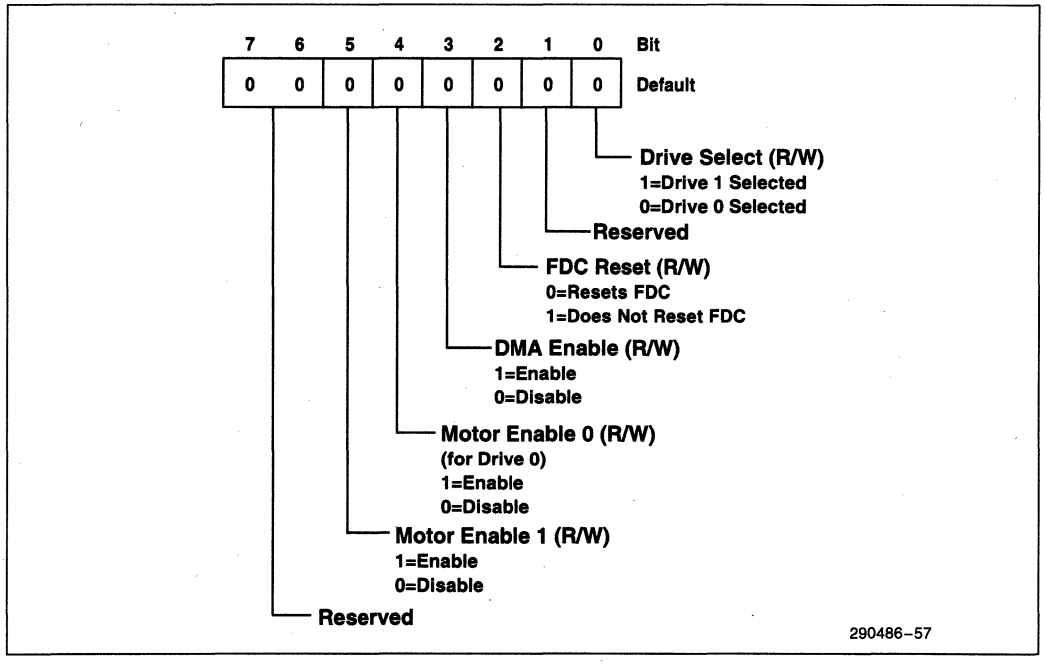


Figure 57. Digital Output Register

Bit	Description
7:6	**RESERVED:** For a two-drive system, these bits are not used and have no affect on FDC operation. For a four drive system, see Appendix A, FDC Four Drive Support.
5	**MOTOR ENABLE 1 (ME1):** This bit controls a motor drive enable signal. ME1 directly controls either the FDME1# signal or FDME0# signal, depending on the state of the BOOTSEL bit in the TDR. When ME1 = 1, the selected motor enable signal (FDME1# or FDME0#) is asserted and when ME1 = 0, the selected motor enable signal is negated.
4	**MOTOR ENABLE 0 (ME0):** This bit controls a motor drive enable signal. ME1 directly controls either the FDME0# signal or FDME1# signal, depending on the state of the BOOTSEL bit in the TDR. When ME0 = 1, the selected motor enable signal (FDME0# or FDME1#) is asserted and when ME0 = 0, the selected motor enable signal is negated.
3	**DMA GATE (DMAGATE):** This bit enables/disables DMA for the FDC. When DMAGATE = 1, DMA for the FDC is enabled. In this mode, FDDREQ, TC, IRQ6, and FDDACK# are enabled. When DMAGATE = 0, DMA for the FDC is disabled. In this mode the IRQ6, and DRQ outputs are tri-stated and the DACK# and TC inputs are disabled to the FDC. Note that the TC input is only disabled to the FDC module. Other functional units in the 82091AA (e.g., parallel port or IDE interface) can still use the TC input signal for DMA activities.
2	**FDC RESET (DORRST):** DORRST is a software reset for the FDC module. When DORRST is set to 0, the basic core of the FDC and the FIFO circuits are cleared conditioned by the LOCK bit in the CONFIGURE Command. This bit is set to 0 by software or a hard reset (RSTDRV asserted). The FDC remains in a reset state until software sets this bit to 1. This bit does not affect the DSR, CCR and other bits of the DOR. DORRST must be held active for at least 0.5 μs at 250 Kbps. This is less than a typical ISA I/O cycle time. Thus, in most systems consecutive writes to this register to toggle this bit allows sufficient time to reset the FDC.
1	**RESERVED:** For a two-drive system, this bit is not used and must be programmed to 0. For a four drive system, see Appendix A, FDC Four Drive Support.
0	**DRIVE SELECT (DS):** This selects the floppy drive by controlling the FDS0# and FDS1# output signals. DS directly controls FDS1 and FDS0 as follows: **Bit 0** — **Output Pin Status** 0 — FDS0# asserted (FDS1 asserted if BOOTSEL = 1) 1 — FDS1# asserted (FDS1 asserted if BOOTSEL = 1)

8.1.3 TDR—ENHANCED TAPE DRIVE REGISTER

I/O Address: Base + 3h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

This register allows the user to assign tape support to a particular drive during initialization. Any future references to that drive number automatically invokes tape support. A hardware reset sets all bits in this register to 0 making drive 0 not available for tape support. A software reset via bit 2 of the DOR does not affect this register. Drive 0 is reserved for the floppy boot drive. Bits[7:2] are only available when EREG EN = 1; otherwise the bits are tri-stated. EREG EN is a bit in the POWERDOWN Command.

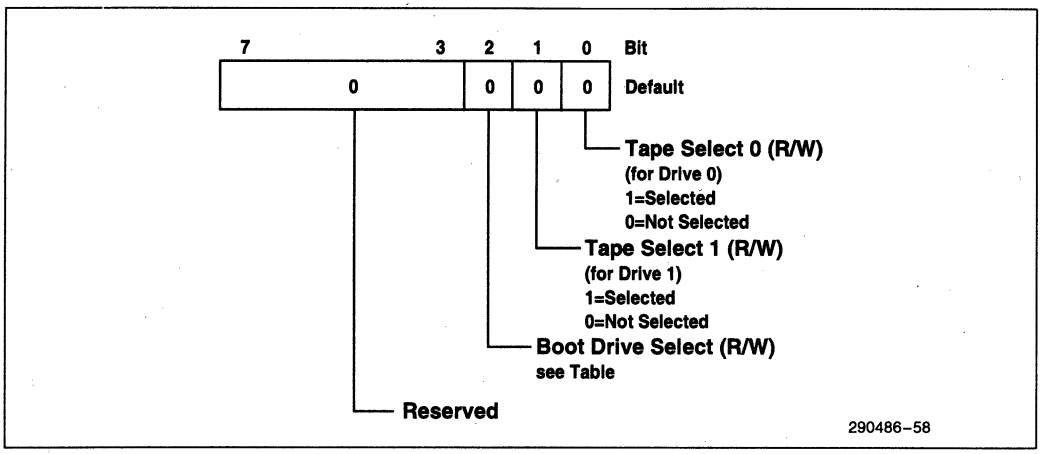


Figure 58. Enhanced Tape Drive Register

Bit	Description
7:3	**RESERVED**
2	**BOOT DRIVE SELECT (BOOTSEL):** The BOOTSEL bit is used to remap the drive selects and motor enables. The functionality is as described below: **BOOTSEL** — **Mapping** 0 — DS0 → FDS0, ME0 → FDME0 (default) DS1 → DS1, ME1 → FDME1 1 — DS0 → DS1, ME0 → FDME1 DS1 → FDS0, ME1 → FDME0 Note that this mapping also applies to a four drive system (FDDQTY = 1 in the FCFG1 Register). In a four drive system, only drive 0 or drive 1 can be selected as the boot drive.
1	**RESERVED:** For a two-drive system, this bit is not used and must be programmed to 0. For a four drive system, see Appendix A, FDC Four Drive Support.
0	**TAPE SELECT (TAPESEL):** This bit is used by software to assign logical drive number 1 to be a tape drive. Other than adjusting precompensation delays for tape support, this bit does not affect the FDC hardware. The bit can be written and read by software as an indication of the tape drive assignment. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive. The tape drive assignment is as follows: **Bit 0** — **Drive Selected** 0 — None (all are floppy disk drives) 1 — Drive 1 is a tape drive.

8.1.4 MSR—MAIN STATUS REGISTER

I/O Address: Base + 4h
Default Value: 00h
Attribute: Read Only
Size: 8 bits

This read only register provides FDC status information. This information is used by software to control the flow of data to and from the FIFO (accessed via the FDCFIFO Register). The MSR indicates when the FDC is ready to send or receive data through the FIFO. During non-DMA transfers, this register should be read before each byte is transferred to or from the FIFO.

After a hard or soft reset or recovery from a powerdown state, the MSR is available to be read by the host. The register value is 00h until the oscillator circuit has stabilized and the internal registers have been initialized. When the FDC is ready to receive a new command, MSR[7:0] = 80h. The worst case time allowed for the MSR to report 80h (i.e., RQM is set to 1) is 2.5 μs after a hard or soft reset.

Main Status Register is used for controlling command input and result output for all commands. Some example values of the MSR are:

- MSR = 80H; The controller is ready to receive a command.
- MSR = 90H; executing a command or waiting for the host to read status bytes (assume DMA mode).
- MSR = D0H; waiting for the host to write status bytes.

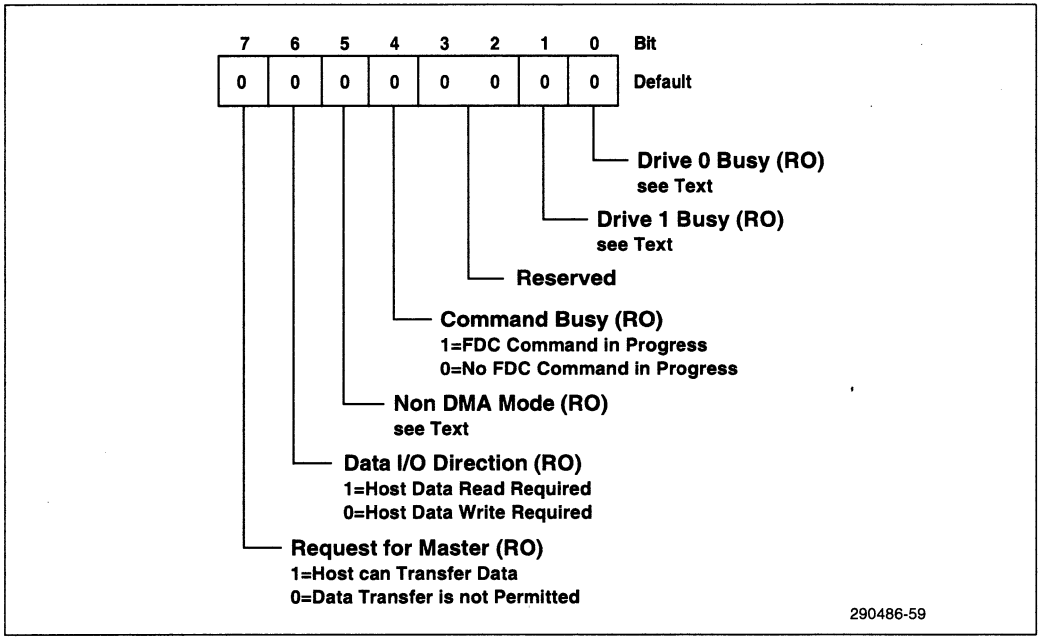


Figure 59. Main Status Register

Bit	Description
7	**REQUEST FOR MASTER (RQM):** When RQM = 1, the FDC is ready to send/receive data through the FIFO (FDCFIFO Register). The FDC sets this bit to 0 after a byte transfer and then sets the bit to 1 when it is ready for the next byte. During non-DMA execution phase, RQM indicates the status of IRQ6.
6	**DIRECTION I/O (DIO):** When RQM = 1, DIO indicates the direction of a data transfer. When DIO = 1, the FDC is requesting a read of the FDCFIFO. When DIO = 0, the FDC is requesting a write to the FDCFIFO.
5	**NON-DMA (NONDMA):** Non-DMA mode is selected via the SPECIFY Command. In this mode, the FDC sets this bit to a 1 during the execution phase of a command. This bit is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.
4	**COMMAND BUSY (CMDBUSY):** CMDBUSY indicates when a command is in progress. When the first byte of the command phase is written, the FDC sets this bit to 1. CMDBUSY is set to 0 after the last byte of the result phase is read. If there is no result phase (e.g., SEEK or RECALIBRATE Commands), CMDBUSY is set to 0 after the last command byte is written.
3:2	**RESERVED:** For a two-drive system, these bits are not used and must be programmed to 0. For a four drive system, see Appendix A, FDC Four Drive Support.
1	**DRIVE 1 BUSY (DRV1BUSY):** The FDC module sets this bit to 1 after the last byte of the command phase of a SEEK or RECALIBRATE Command is issued for drive 1. This bit is set to 0 after the host reads the first byte in the result phase of the SENSE INTERRUPT Command for this drive.
0	**DRIVE 0 BUSY (DRV0BUSY):** The FDC module sets this bit to 1 after the last byte of the command phase of a SEEK or RECALIBRATE Command is issued for drive 0. This bit is set to 0 after the host reads the first byte in the result phase of the SENSE INTERRUPT Command for this drive.

8.1.5 DSR—DATA RATE SELECT REGISTER

I/O Address: Base + 4h
Default Value: 02h
Attribute: Write Only
Size: 8 bits

The DSR selects the data rate, amount of write precompenstion, invokes direct powerdown, and invokes a FDC software reset. This write only register ensures backward compatibility with the Intel series of floppy disk controllers. Changing the data rate changes the timings of the drive control signals. To ensure that drive timings are not violated when changing data rates, choose a drive timing such that the fastest data rate will not violate the timing.

In the default state, the PDOSC bit is low and the oscillator is powered up. When this bit is programmed to a 1, the oscillator is shut off. Hardware reset sets this bit to a 0. Neither of the software resets (via DOR or DSR) have any effect on this bit. Note that PDOSC should only be set to a 1 when the FDC module is in the powerdown state. Otherwise, the FDC will not function correctly and must be hardware reset once the oscillator has turned back on and stabilized. Setting the PDOSC bit has no effect on the clock input to the FDC (the X1 pin). The clock input is separately disabled when the part is powered down. The Save Command checks the status of PDOSC. However the Restore Command will not restore this bit to a 1.

Software resets do not affect the DRATE or PRECOMP bits.

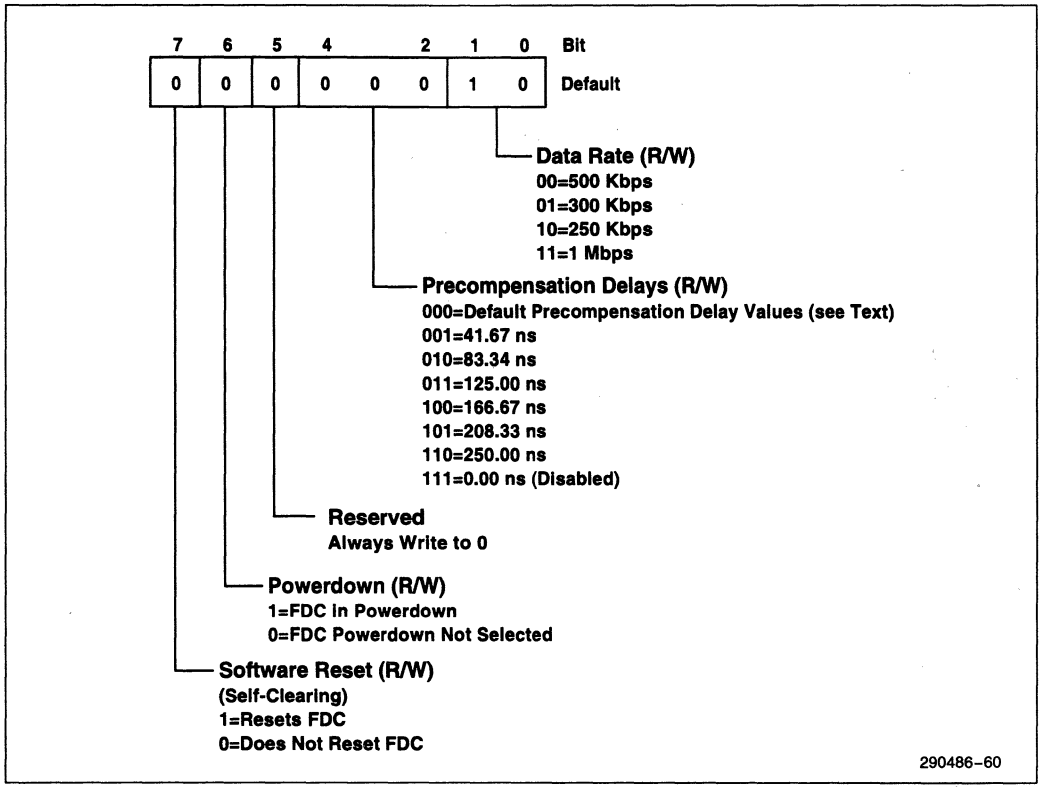


Figure 60. Data Rate Select Register

Bit	Description
7	**SOFTWARE RESET (DSRRST):** DSRRST operates the same as the DORRST bit in the DOR, except that this bit is self clearing.
6	**POWERDOWN (FPD):** FPD provides direct powerdown for the FDC module. When FPD = 1, the FDC module enters the powerdown state, regardless of the state of the module. The FDC module is internally reset and then put into powerdown. No status is saved and any operation in progress is aborted. A hardware or software reset causes the 82091AA to exit the FDC module powerdown state.
5	**RESERVED**
4:2	**PRECOMPENSATION (PRECOMP):** Bits[4:2] adjusts the WRDATA output to the disk to compensate for magnetic media phenomena known as bit shifting. The data patterns that are susceptible to bit shifting are well understood and the FDC compensates the data pattern as it is written to the disk. The amount of precompensation depends on the drive and media but in most cases the default value is acceptable. The FDC module starts pre-compensating the data pattern starting on Track 0. The CONFIGURE Command can change the track where pre-compensating originates. **Bits[4:2] — Precompensation Delays (ns)** 0 0 0 — Default mode 0 0 1 — 41.67 0 1 0 — 83.34 0 1 1 — 125.00 1 0 0 — 166.67 1 0 1 — 208.33 1 1 0 — 250 1 1 1 — 0.00 (disabled) The default precompensation delay mode provides the following delays: **Data Rate — Default Precompensation Delays (ns)** 1 Mbps — 41.67 0.5 Mbps — 125.00 0.3 Mbps — 125.00 0.25 Mbps — 125.00
1:0	**DATA RATE SELECT (DRATESEL):** DRATESEL[1:0] select one of the four data rates as listed below. The default value is 250 Kbps. **Bits[1:0] — Date Rate** 1 1 — 1 Mbps 0 0 — 500 Kbps 0 1 — 300 Kbps 1 0 — 250 Kbps - default

8.1.6 FDCFIFO—FDC FIFO (DATA)

I/O Address: Base + 5h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

All command parameter information and disk data transfers go through the 16-byte FIFO. The FIFO has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the MSR. At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. At the start of the command execution phase, the FDC clears the FIFO of any data to ensure that invalid data is not transferred. An overrun or underrun will terminate the current command and the transfer of data. Disk writes complete the current sector by generating a 00 pattern and valid CRC.

The FIFO defaults to an 8272A compatible mode after a hardware reset (via RSTDRV pin). Software resets (via DOR or DSR) can also place the FDC into 8272A compatible mode, if the LOCK bit is set to 0 (see the definition of the LOCK bit) maintaining PC-AT hardware compatibility. The default values can be changed through the CONFIGURE Command (enable full FIFO operation with threshold control). The FIFO provides the system a larger DMA latency without causing a disk error. The following table gives several examples of the delays with a FIFO. The data is based upon the formula: Threshold# × 1/DATA RATE × 8 − 1.5 μs = DELAY.

FIFO Threshold	Maximum Service Delay (1 Mbps Data Rate)	Maximum Delay to Servicing at 500 Kbps Data Rate
1 byte	1 × 8 μs − 1.5 μs = 6.5 μs	1 × 16 μs − 1.5 μs = 14.5 μs
2 bytes	2 × 8 μs − 1.5 μs = 14.5 μs	2 × 16 μs − 1.5 μs = 30.5 μs
8 bytes	8 × 8 μs − 1.5 μs = 62.5 μs	8 × 16 μs − 1.5 μs = 126.5 μs
15 bytes	15 × 8 μs − 1.5 μs = 118.5 μs	15 × 16 μs − 1.5 μs = 238.5 μs

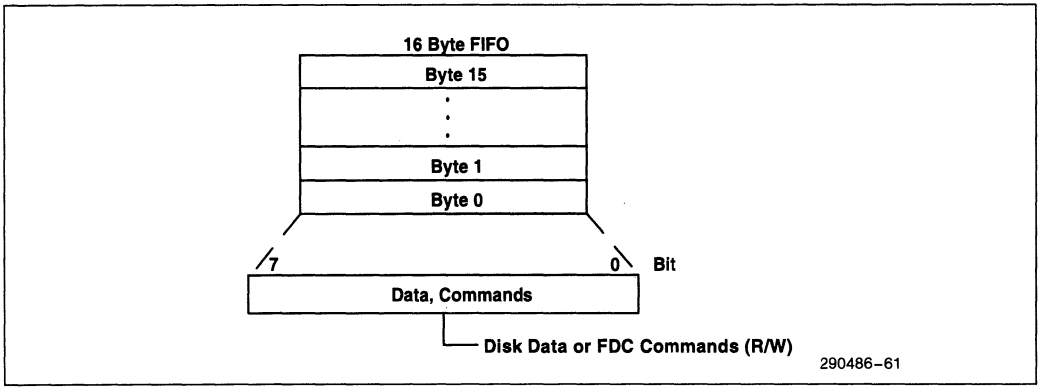


Figure 61. FDC FIFO

Bit	Description
7:0	**FIFO DATA:** Bits[7:0] correspond to SD[7:0].

8.1.7 DIR—DIGITAL INPUT REGISTER

I/O Address: Base +7h
Default Value: 00h
Attribute: Read Only
Size: 8 bits

This register is read only in all modes. In PC-AT mode only bit 7 is driven and all other bits remain tri-stated.

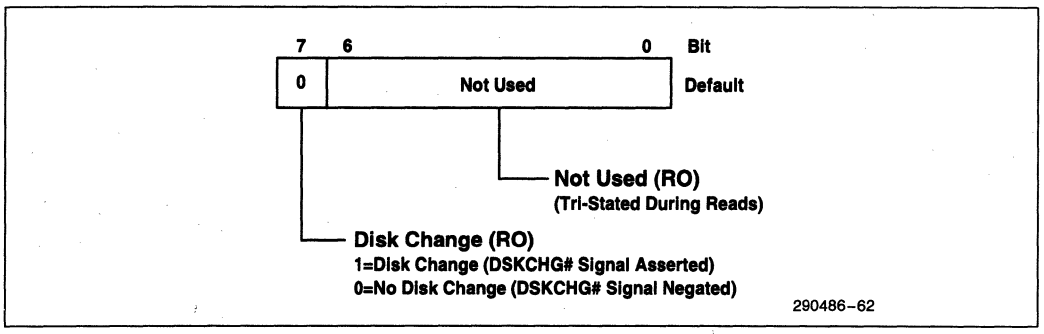


Figure 62. Digital Input Register

Bit	Description
7	**DISK CHANGE (DSKCHG):** This bit monitors a disk change in the floppy disk drive. DSKCHG is set to a 1 when the DSKCHG# signal on the floppy interface is asserted. DSKCHG is set to a 0 when the DSKCHG# signal on the floppy interface is negated. During powerdown, this bit is invalid.
6:0	**NOT USED:** These bits are tri-stated during a read.

8.1.8 CCR—CONFIGURATION CONTROL REGISTER

I/O Address: Base + 7h
Default Value: 02h
Attribute: Write Only
Size: 8 bits

This register sets the data rate.

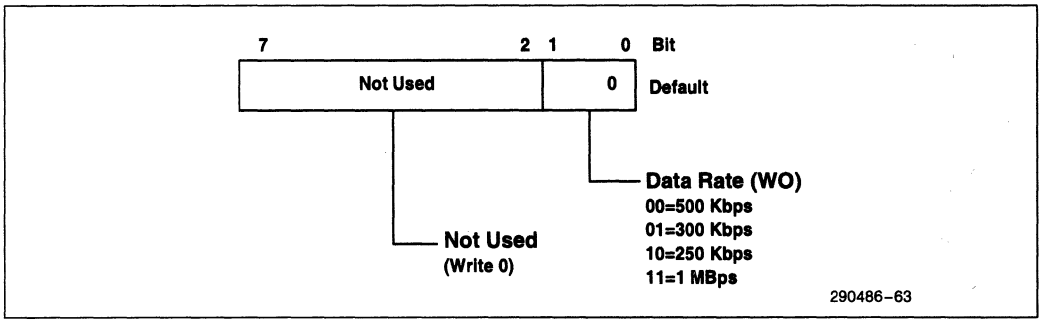


Figure 63. Configuration Control Register

8.2 Reset

There are four sources of FDC reset—a hard reset via the RSTDRV signal and three software resets (via the FCFG2, DOR, and DSR Registers). At the end of the reset, the FDC comes out of the powerdown state. Note that the DOR reset condition remains in effect until software programs the DORRST bit to 1 in the DOR. All operations are terminated and the FDC enters an idle state. Invoking a reset while a disk write activity is in progress will corrupt the data and CRC. On exiting the reset state, various internal registers are cleared, and the FDC waits for a new command. Drive polling will start unless disabled by a new CONFIGURE Command.

8.2.1 HARD RESET AND CONFIGURATION REGISTER RESET

A hard reset (asserting RSTDRV) and a software reset through the FCFG2 Registers have the same affect on the FDC. These resets clear all FDC registers, except those programmed by the SPECIFY command. The DOR reset bit is enabled and must be set to 0 by the host to exit the reset state.

8.2.2 DOR RESET vs DSR RESET

The DOR and DSR resets are functionally the same. The DSR reset is included to maintain 82072 compatibility. Both reset the 8272 core, which affects drive status information. The FIFO circuits are also reset if the LOCK bit is a 0 (see definition of the LOCK bit). The DSR reset is self-clearing (exits the reset state automatically) while the DOR reset remains in the reset state until software writes the DOR reset bit to 0. DOR reset has precedence over the DSR reset. The DOR reset is set automatically when a hard reset or configuration reset occurs. Software must set the DOR reset bit to 0 to exit the reset state.

The AC Specifications gives the minimum amount of time that the DOR reset must be held active. This amount of time that the DOR reset must be held active is dependent upon the data rate. FDC requires that the DOR reset bit must be held active for at least 0.5 μs at 250 Kbps. This is less than a typical ISA I/O cycle time.

8.3 DMA Transfers

DMA transfers are enabled with the SPECIFY Command. When enabled, The FDC initiates DMA transfers by asserting the FDDREQ signal during a data transfer command. The FIFO is enabled directly by asserting FDDACK# and addresses need not be valid.

8.4 Controller Phases

The FDC handles commands in three phases—*command*, *execution* and *result*. Each phase is described in the following sections. When not processing a command, the FDC can be in the *idle*, *drive polling* or *powerdown state*. This section describes the command, execute and result phases.

8.4.1 COMMAND PHASE

After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes must be written to the FDC (as described in Section 8.8, Command Set Description) before the command phase is complete. These bytes of data must be transferred in the order described.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM must be 1 and DIO must be 0, before command bytes may be written. The FDC sets RQM to 0 after each write cycle and keeps the bit at 0 until the received byte is processed. After processing the byte, the FDC sets RQM to 1 again to request the next parameter byte of the command, unless an illegal command condition is detected. After the last parameter byte is received, RQM remains 0, and the FDC automatically enters the next phase (execution or result phase) as defined by the command definition.

The FIFO is disabled during the command phase to retain compatibility with the 8272A, and to provide for the proper handling of the Invalid Command condition.

8.4.2 EXECUTION PHASE

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, threshold is defined as the number of bytes available to the FDC when service is requested from the host, and ranges from 1 to 16. The FIFOTHR parameter, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (e.g., 2) results in longer periods of time between service requests but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (e.g., 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

8.4.2.1 Non-DMA Mode Transfers from the FIFO to the Host

The IRQ6 pin and RQM bits in the Main Status Register are activated when the FIFO contains 16 (or set threshold) bytes, or the last bytes of a full sector transfer have been placed in the FIFO. The IRQ6 pin can be used for interrupt driven systems and RQM can be used for polled sytems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO, then FDC negates the IRQ6 pin and RQM bit.

8.4.2.2 Non-DMA Mode Transfers from the Host to the FIFO

The IRQ6 pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The IRQ6 pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has (threshold) bytes remaining in the FIFO. The IRQ6 pin is also negated if TC and DACK# both go inactive. The FDC enters the result phase after the last byte is taken by the FDC from the FIFO (i.e. FIFO empty condition).

8.4.2.3 DMA Mode Transfers from the FIFO to the Host

The FDC asserts the FDDREQ signal when the FIFO contains 16 (or set threshold) bytes or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The FDC negates FDDREQ when the FIFO is empty. FDDREQ is negated after FDDACK# is asserted for the last byte of a data transfer (or on the active edge of RD#, on the last byte, if no edge is present on FDDACK#).

NOTE:
FDDACK# and TC must overlap for at least 50 ns for proper functionality. A data underrun may occur if FDDREQ is not removed in time to prevent an unwanted cycle.

8.4.2.4 DMA Mode Transfers from the Host to the FIFO

The FDC asserts FDDREQ when entering the execution phase of data transfer commands. The DMA controller must respond by asserting FDDACK# and WR# signals and placing data in the FIFO. FDDREQ remains asserted until the FIFO becomes full. FDDREQ is again asserted when the FIFO has (threshold) bytes remaining in the FIFO. The FDC also negates the FDDREQ when the FIFO becomes empty (qualified by DACK# and TC overlapping by 50 ns) indicating that no more data is required. FDDREQ is negated after FDDACK# is asserted for the last byte of a data transfer (or on the active edge of WR# of the last byte, if no edge is present on DACK#). A data overrun may occur if FDDREQ is not removed in time to prevent an unwanted cycle.

8.4.3 DATA TRANSFER TERMINATION

The FDC supports terminal count explicitly through the TC signal and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector and the FDC will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

NOTE:

When the host is sending data to the FIFO, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must be able to tolerate this. In a DMA system, FDDREQ is removed (negated) as soon as TC is received indicating the termination of the transfer. The reception of TC also generates an interrupt on IRQ6. However, in a non-DMA system the interrupt will not be generated until the FIFO is empty.

The generation of IRQ6 determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete (refer to Section 8.5, Command Set/Descriptions). These bytes of data must be read out for another command to start.

RQM and DIO must both be 1 before the result bytes may be read from the FIFO. After all the result bytes have been read, RQM=1, DIO=0, and CMDBUSY=0 in the MSR. This indicates that the FDC is ready to accept the next command.

8.5 Command Set/Descriptions

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it was invalid, the next time the RQM bit in the MSR register is 1 the DIO and CB bits will also be 1, indicating the FIFO must be read. A result byte of 80h will be read out of the FIFO, indicating an invalid command was issued. After reading the result byte from the FIFO, the FDC returns to the command phase. Table 23 shows the FDC Command set.

Table 24. FDC Command Set

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Read Data										
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	.....			C		.....			Sector ID
	W	.....			H		.....			Information Prior to
	W	.....			R		.....			Command
										Execution
	W	.....			N		.....			
	W	.....			EOT		.....			
	W	.....			GPL		.....			
	W	.....			DTL		.....			
Execution										Data Transfer Between the FDD and System
Result	R	.....			ST 0		.....			Status Information
	R	.....			ST 1		.....			After Command
	R	.....			ST 2		.....			Execution
	R	.....			C		.....			
	R	.....			H		.....			Sector ID
	R	.....			R		.....			Information After
	R	.....			N		.....			Command
										Execution
Read Deleted Data										
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	.....			C		.....			Sector ID
	W	.....			H		.....			Information Prior to
	W	.....			R		.....			Command
										Execution
	W	.....			N		.....			
	W	.....			EOT		.....			
	W	.....			GPL		.....			
	W	.....			DTL		.....			
Execution										Data Transfer Between the FDD and System
Result	R	.....			ST 0		.....			Status Information
	R	.....			ST 1		.....			After Command
	R	.....			ST 2		.....			Execution
	R	.....			C		.....			
	R	.....			H		.....			Sector ID
	R	.....			R		.....			Information After
	R	.....			N		.....			Command
										Execution

2

Table 24. FDC Command Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Write Data										
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	.....			C		.....			Sector ID
	W	.....			H		.....			Information Prior to
	W	.....			R		.....			Command
										Execution
	W	.....			N		.....			
	W	.....			EOT		.....			
	W	.....			GPL		.....			
	W	.....			DTL		.....			
Execution										Data Transfer Between the FDD and System
Result	R	.....			ST 0		.....			Status Information
	R	.....			ST 1		.....			After Command
	R	.....			ST 2		.....			Execution
	R	.....			C		.....			
	R	.....			H		.....			Sector ID
	R	.....			R		.....			Information After
	R	.....			N		.....			Command
										Execution
Write Deleted Data										
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	.....			C		.....			Sector ID
	W	.....			H		.....			Information Prior to
	W	.....			R		.....			Command
										Execution
	W	.....			N		.....			
	W	.....			EOT		.....			
	W	.....			GPL		.....			
	W	.....			DTL		.....			
Execution										Data Transfer Between the FDD and System
Result	R	.....			ST 0		.....			Status Information
	R	.....			ST 1		.....			After Command
	R	.....			ST 2		.....			Execution
	R	.....			C		.....			
	R	.....			H		.....			Sector ID
	R	.....			R		.....			Information After
	R	.....			N		.....			Command
										Execution

Table 24. FDC Command Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4		D3	D2	D1	D0	Remarks
Read Track											
Command	W	0	MFM	0	0		0	0	1	0	Command Codes
	W	0	0	0	0		0	HDS	DS1	DS0	
	W	.....				C		.....			Sector ID
	W	.....				H		.....			Information Prior to
	W	.....				R		.....			Command Execution
	W	.....				N		.....			
	W	.....				EOT					
	W	.....				GPL		.....			
	W	.....				DTL		.....			
Execution											Data Transfer Between the FDD and System. FDC Reads All Sectors From Index Hole to EOT
Result	R	.....				ST 0		.....			Status Information
	R	.....				ST 1		.....			After Command
	R	.....				ST 2		.....			Execution
	R	.....				C		.....			
	R	.....				H		.....			Sector ID
	R	.....				R		.....			Information After
	R	.....				N		.....			Command Execution
Verify											
Command	W	MT	MFM	SK	1		0	1	1	0	Command Codes
	W	EC	0	0	0		0	HDS	DS1	DS0	
	W	.....				C		.....			Sector ID
	W	.....				H		.....			Information Prior to
	W	.....				R		.....			Command Execution
	W	.....				N		.....			
	W	.....				EOT					
	W	.....				GPL		.....			
	W	.....				DTL/SC		.....			
Execution											Data Transfer Between the FDD and System
Result	R	.....				ST 0		.....			Status Information
	R	.....				ST 1		.....			After Command
	R	.....				ST 2		.....			Execution
	R	.....				C		.....			
	R	.....				H		.....			Sector ID
	R	.....				R		.....			Information After
	R	.....				N		.....			Command Execution

2

Table 24. FDC Command Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4		D3	D2	D1	D0	Remarks
Version											
Command	W	0	0	0	1		0	0	0	0	Command Codes
Result	W	1	0	0	1		0	0	0	0	Enhanced Controller
Format Track											
Command	W	0	MFM	0	0		1	1	0	1	Command Codes
	W	0	0	0	0		0	HDS	DS1	DS0	
	W	.....				N		.....			Bytes/Sector
	W	.....				SC		.....			Sector/Cylinder
	W	.....				GPL		.....			Gap 3
	W	.....				D		.....			Filler Byte
Execution For Each Sector Repeat:	W	.....				C		.....			
	W	.....				H		.....			Input Sector
	W	.....				R		.....			Parameters
	W	.....				N		.....			
											FDC Formats an Entire Cylinder
Result	R	.....				ST 0		.....			Status Information
	R	.....				ST 1		.....			after Command
	R	.....				ST 2		.....			Execution
	R	.....				Undefined		.....			
	R	.....				Undefined		.....			
	R	.....				Undefined		.....			
	R	.....				Undefined		.....			
Scan Equal											
Command	W	MT	MFM	SK	1		0	0	0	0	Command Codes
	W	0	0	0	0		0	HDS	DS1	DS0	
	W	.....				C		.....			Sector ID
	W	.....				H		.....			Information Prior
	W	.....				R		.....			to Command
	W	.....				N		.....			Execution
	W	.....				EOT		.....			
	W	.....				GPL		.....			
	W	.....				STP		.....			
Execution											Data Compared Between the FDD and Main-System
Result	R	.....				ST 0		.....			Status Information
	R	.....				ST 1		.....			After Command
	R	.....				ST 2		.....			Execution
	R	.....				C		.....			
	R	.....				H		.....			Sector ID
	R	.....				R		.....			Information After
	R	.....				N		.....			Command Execution

Table 24. FDC Command Set (Continued)

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Scan Low or Equal										
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	.....			C		.....			Sector ID
	W	.....			H		.....			Information Prior
	W	.....			R		.....			to Command
	W	.....			N		.....			Execution
	W	.....			EOT		.....			
	W	.....			GPL		.....			
	W	.....			STP		.....			
Execution										Data Compared Between the FDD and Main-System
Result	R	.....			ST 0		.....			Status Information
	R	.....			ST 1		.....			After Command
	R	.....			ST 2		.....			Execution
	R	.....			C		.....			
	R	.....			H		.....			Sector ID
	R	.....			R		.....			Information After
	R	.....			N		.....			Command Execution
Scan High or Equal										
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	.....			C		.....			Sector ID
	W	.....			H		.....			Information Prior
	W	.....			R		.....			to Command
	W	.....			N		.....			Execution
	W	.....			EOT		.....			
	W	.....			GPL		.....			
	W	.....			STP		.....			
Execution										Data Compared Between the FDD and Main-System
Result	R	.....			ST 0		.....			Status Information
	R	.....			ST 1		.....			After Command
	R	.....			ST 2		.....			Execution
	R	.....			C		.....			
	R	.....			H		.....			Sector ID
	R	.....			R		.....			Information After
	R	.....			N		.....			Command Execution
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS0	DS1	Enhanced Controller
Execution										Head Retracted to Track 0 Interrupt

2

Table 24. FDC Command Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	.....				ST 0				Status Information at the End of Each Seek Operation
	R	.....				PCN				
Specify										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	.....	SRT	.....		.....	HUT		.....	
	W	.....		HLT	.....			ND		
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	.....				ST 3				Status Information About FDD
Drive Specification Command										
Command	W	1	0	0	0	1	1	1	0	Command Code
	W	0	FD1	FD0	PTS	DRT1	DRT0	DT1	DT0	
	:	:	:	:	:	:	:	:	:	0–4 bytes issued
	W	DN	NRP	0	0	0	0	0	0	
Result	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 0
	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 1
	R	0	0	0	0	0	0	0	0	RSVD
	R	0	0	0	0	0	0	0	0	RSVD
Seek										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution	W	.....				NCN				Head is Positioned Over Proper Cylinder on Diskette
Configure										
Command	W	0	0	0	1	0	0	1	1	Command Code
	W	0	0	0	0	0	0	0	0	
	W	0	EIA	EFIFO	POLL	.....	FIFOTHR			
	W	.....				PRETRK				
Relative Seek										
Command	W	1	DIR#	0	0	1	1	1	1	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	.....				RCN				

Table 24. FDC Command Set (Continued)

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
DUMPREG										
Command Execution	W	0	0	0	0	1	1	1	0	Note: Registers placed in FIFO
Result	R	.....				PCN-Drive 0	.....			
	R	.....				PCN-Drive 1	.....			
	R	.....				PCN-Drive 2	.....			
	R	.....				PCN-Drive 3	.....			
	R	.....	SRT	.....		.....	HUT	.....		
	R	.....	.....	HLT		.....	.....		ND	
		.....	.....			SC/EOT	.....			
	R	LOCK	0	0	0	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO		POLL	FIFOTHR	.....		
	R	.....	.....			PRETRK	.....			
Read ID										
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	The First Correct ID Information on the Cylinder is Stored in Data Register
Result	R	.....				ST 0	.....			Status Information
	R	.....				ST 1	.....			After Command
	R	.....				ST 2	.....			Execution
	R	.....				C	.....			
	R	.....				H	.....			Disk Status After the
	R	.....				R	.....			Command has
	R	.....				N	.....			Completed
Perpendicular Mode										
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	0	0	D1	D0	GAP	WGATE	
Lock										
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	
Part ID										
Command	W	0	0	0	1	1	0	0	0	Command Code
Result	R	0	0	0	.....	Stepping	.....		1	Part ID Number
Powerdown Mode										
Command	W	0	0	0	1	0	1	1	1	Command Code
	W	0	0	EREG EN	0	0	FDI TRI	MIN DLY	AUTO PD	
Result	R	0	0	EREG EN	0	0	FDI TRI	MIN DLY	AUTO PD	

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Table 24. FDC Command Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Option										
Command	W	0	0	1	1	0	0	1	1	Command Code
	W	.....		RSVD		.....			ISO	
Save										
Command	W	0	0	1	0	1	1	1	0	Command Code
Result	R	RSVD	RSVD	PD OSC	PC2	PC1	PC0	DRATE1	DRATE0	Save Information to Reprogram the FDC
		0	0	0	0	0	0	0	ISO	
	R	.....			PCN-Drive 0	.....				
	R	.....			PCN-Drive 1	.....				
	R	.....			PCN-Drive 2	.....				
	R	.....			PCN-Drive 3	.....				
	R	.....	SRT	.....		.....	HUT	.....		
	R	.....			HLT	.....			ND	
	R	.....			SC/EOT	.....				
	R	LOCK	0	0	0	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL	—	.....	FIFOTHR	.....	
	R	.....			PRETRK	.....				
	R	0	0	EREG EN	0	RSVD	FDI TRI	MIN DLY	AUTO PD	
	R	.....			DISK/STATUS	.....				
	R	.....			RSVD	.....				
	R	.....			RSVD	.....				
Restore										
Command	W	0	1	0	0	1	1	1	0	Command Code
	W	0	0	0	PC2	PC1	PC0	DRATE1	DRATE0	Restore Original
	W	0	0	0	0	0	0	0	ISO	Register Status
	W	.....			PCN-Drive 0	.....				
	W	.....			PCN-Drive 1	.....				
	W	.....			PCN-Drive 2	.....				
	W	.....			PCN-Drive 3	.....				
	W	.....	SRT	.....		.....	HUT	.....		
	W	.....			HLT	.....			ND	
	W	.....			SC/EOT	.....				
	W	LOCK	0	0	0	D1	D0	GAP	WGATE	
	W	0	EIS	EFIFO	POLL	.....	FIFOTHR	.....		
	W	.....			PRETRK	.....				
	W	0	0	EREG EN	0	RSVD	FDI TRI	MIN DLY	AUTO PD	
	W	.....			DISK/STATUS	.....				
	W	.....			RSVD	.....				
	W	.....			RSVD	.....				

Table 24. FDC Command Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Format and Write										
Command	W	1	MFM	1	0	1	1	0	1	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	.....			N		.....			
	W	.....			SC		.....			
	W	.....			GPL		.....			
	W	.....			D		.....			
Execution	W	.....			C		.....			Input
repeated	W	.....			H		.....			Sector
for each	W	.....			R		.....			Parameters
sector	W	.....			N		.....			
	W	Data Transfer Of N Bytes								FDC Formats and Writes Entire Track
Result	R	.....			ST 0		.....			
	R	.....			ST 1		.....			
	R	.....			ST 2		.....			
	R	.....			Undefined		.....			
	R	.....			Undefined		.....			
	R	.....			Undefined		.....			
	R	.....			Undefined		.....			
Invalid										
Command	W	.....			Invalid Codes		.....			Invalid Command Codes (Noop—FDC goes into Standby State)
Result	R	.....			ST 0		.....			ST 0 = 80

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Parameter Abbreviations

Symbol	Description
AUTO PD	**AUTO POWERDOWN CONTROL:** When AUTO PD = 0, automatic powerdown is disabled. When AUTO PD = 1, automatic powerdown is enabled.
C	**CYLINDER ADDRESS:** The currently selected cylinder address, 0 to 255.
D0, D1	**DRIVE SELECT 0-1:** Designates which drives are Perpendicular drives. A 1 indicates Perpendicular drive.
D	**DATA PATTERN:** The pattern to be written in each sector data field during formatting.
DN	**DONE:** This bit indicates that this is the last byte of the drive specification command. The FDC checks to see if this bit is 1 or 0. When DN = 0, the FDC expects more bytes. DN = 0 FDC expects more subsequent bytes. DN = 1 Terminates the command phase and enters the results phase. An additional benefit is that by setting this bit to 1, a direct check of the current drive specifications can be done.
DIR#	**DIRECTION CONTROL:** When DIR# = 0, the head steps out from the spindle during a relative seek. When DIR# = 1, the head steps in toward the spindle.
DS0, DS1	**DISK DRIVE SELECT:**

DS1	DS0	Drive Slot
0	0	drive 0
0	1	drive 1
1	0	drive 2*
1	1	drive 3*

*Available when FDDQTY = 1 in the FCFG1 Register (see Appendix A, FDC Four Drive Support)

DTL	**SPECIAL SECTOR SIZE:** By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FFh.
DRATE[0:1]	**DATA RATE:** Data rate values from the DSR register.

Symbol **Description**

DRT0, DRT1 **DATA RATE TABLE SELECT:** These two bits select between the different data rate tables. The default is the conventional table. These also provide mapping of the data rates selected in the DSR and CCR. The table below shows this.

Bits in DSR					
DRT1	**DRT0**	**DRATE1**	**DRATE0**	**Data Rate**	**Operation**
0	0	1	1	1 Mbps	Default
		0	0	500 Kbps	
		0	1	300 Kbps	
		1	0	250 Kbps	
0	1	RSVD	RSVD	RSVD	RSVD
1	0	RSVD	RSVD	RSVD	RSVD
1	1	1	1	1 Mbps	Perpendicular mode FDDs
		0	0	500 Kbps	
		0	1	Illegal	
		1	0	250 Kbps	

DT0,DT1 **DRIVE DENSITY SELECT TYPE:** These bits select the outputs on DRVDEN0 and DRVDEN1 (see DRIVE SPECIFICATION Command).

EC **ENABLE COUNT:** When EC = 1, the DTL parameter of the Verify Command becomes SC (Number of sectors per track).

EFIFO **Enable FIFO:** When EFIFO = 0, the FIFO is enabled. EFIFO = 1 puts the FDC in the 8272A compatible mode where the FIFO is disabled.

EIS **ENABLE IMPLIED SEEK:** When EIS = 1, a seek operation is performed before executing any read or write command that requires the C parameter in the command phase. EIS = 0 disables the implied seek.

EOT **END OF TRACK:** The final sector number of the current track.

EREG EN **ENHANCED REGISTER ENABLE:** When EREG EN = 1, the TDR register is extended and SRB is made visible to the user. When EREG EN = 0, the standard registers are used.

FDI TRI **FLOPPY DRIVE INTERFACE TRI-STATE:** When FDI TRI = 0, the output pins of the floppy disk drive interface are tri-stated. This is also the default state. When FDI TRI = 1, the floppy disk drive interface remains unchanged.

Symbol	Description
FD0, FD1	**FLOPPY DRIVE SELECT:** These two bits select which physical drive is being specified. The FDn corresponds to FDSn and FDMEn on the floppy drive interface. The drive is selected independent of the BOOTSEL bit in the TDR. Refer to Section 8.1.3, TDR—Enhanced Tape Drive Register, which explains the distinction between physical drives and their virtual mapping as defined by the BOOTSEL bit.

FD1	FD0	Drive slot
0	0	drive 0
1	0	drive 1
0	1	drive 2*
1	1	drive 3*

*Available if the four floppy drive option is selected in the FCFG1 Register.

GAP	**GAP:** Alters Gap 2 length when using Perpendicular Mode.
GPL	**GAP LENGTH:** The gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	**HEAD ADDRESS:** Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	**HEAD LOAD TIME:** The time interval that FDC waits after loading the head and before initiating a read or write operation. Refer to the SPECIFY Command for actual delays.
HUT	**HEAD UNLOAD TIME:** The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the SPECIFY Command for actual delays.
ISO	**ISO FORMAT:** When ISO = 1, the ISO format is used for all data transfer commands. When ISO = 0, the normal IBM system 34 and perpendicular is used. The default is ISO = 0.
LOCK	**LOCK:** Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE Command can be reset to their default values by a software reset (Reset made by setting the proper bit in the DSR or DOR registers).
MFM	**MFM MODE:** A one selects the double density (MFM) mode. A zero is reserved.

Symbol	Description
MIN DLY	**MINIMUM POWERUP TIME CONTROL:** This bit is active only if AUTO PD bit is enabled. When MIN DLY = 0, a 10 ms minimum powerup time is assigned and when MIN DLY = 1, a 0.5 sec. minimum powerup time is assigned.
MT	**MULTI-TRACK SELECTOR:** When MT = 1, the multi-track operating mode is selected. In this mode, the FDC treats a complete cylinder, under head 0 and 1, as a single track. The FDC operates as if this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.
N	**SECTOR SIZE CODE:** This specifies the number of bytes in a sector. When N = 00h, the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to 07h are allowable. A value of 07h equals a sector size of 16 Kbytes. It is the users responsibility to not select combinations that are not possible with the drive.

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024
..	...
07	16 Kbytes

NCN	**NEW CYLINDER NUMBER:** The desired cylinder number.
ND	**NON-DMA MODE FLAG:** When ND = 1, the FDC operates in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When ND = 0, the FDC operates in DMA mode and interfaces to a DMA controller by means of the DRQ and DACK# signals.
NRP	**NO RESULTS PHASE:** When NRP = 1, the result phase is skipped. When NRP = 0, the result phase is generated.
OW	**OVERWRITTEN:** The bits denoted D0 and D1 of the PERPENDICULAR MODE Command can only be overwritten when OW = 1.

Symbol	Description
PCN	**PRESENT CYLINDER NUMBER:** The current position of the head at the completion of SENSE INTERRUPT STATUS Command.
PC2,PC1,PC0	**PRECOMPENSATION VALUES:** Precompensation values from the DSR register.
PDOSC	**POWERDOWN OSCILLATOR:** When this bit is set, the internal oscillator is turned off.
PTS	**PRECOMPENSATION TABLE SELECT:** This bit selects whether to enable the precompensation value programmed in the DSR or not. In the default state, the value programmed in DSR will be used. More information regarding the precompensation is available in Section 8.1.5. PTS = 0 DSR programmed precompensation delays PTS = 1 No precompensation delay is selected for the corresponding drive.
POLL	**POLLING DISABLE:** When POLL = 1, the internal polling routine is disabled. When POLL = 0, polling is enabled.
PRETRK	**PRECOMPENSATION START TRACK NUMBER:** Programmable from track 00 to FFh.
R	**SECTOR ADDRESS:** The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	**RELATIVE CYLINDER NUMBER:** Relative cylinder offset from present cylinder as used by the RELATIVE SEEK Command.
SC	**NUMBER OF SECTORS:** The number of sectors to be initialized by the FORMAT Command. The number of sectors to be verified during a Verify Command, when EC = 1.
SK	**SKIP FLAG:** When SK = 1, sectors containing a deleted data address mark will automatically be skipped during the execution of a READ DATA Command. If a READ DELETED DATA Command is executed, only sectors with a deleted address mark will be accessed. When SK = 0, the sector is read or written the same as the read and write commands.
SRT	**STEP RATE INTERVAL:** The time interval between step pulses issued by the FDC. Programmable from 0.5 ms to 8 ms, in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY Command for actual delays.
ST0-3	**STATUS REGISTERS 0-3.**Registers within the FDC that store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	**WRITE GATE:** Write gate alters timing of WE, to allow for pre-erase loads in perpendicular drives.

8.5.1 STATUS REGISTER ENCODING

The contents of these registers are available only through a command sequence.

8.5.1.1 Status Register 0

Bit #	Symbol	Name	Description
7,6	IC	Interrupt Code	00 Normal termination of command. The specified command was properly executed and completed without error. 01 Abnormal termination of command. Command execution was started, but was not successful completed. 10 Invalid command. The requested command could not be executed. 11 Abnormal termination caused by Polling.
5	SE	Seek End	The 82091AA completed a SEEK or RECALIBRATE command, or a READ or WRITE with implied seek command.
4	EC	Equipment Check	The TRK pin failed to become a "1" after: 1. 80 step pulses in the RECALIBRATE COMMAND. 2. The RELATIVE SEEK command causes the 82078 to step outward beyond Track 0.
3	—	—	Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

8.5.1.2 Status Register 1

Bit #	Symbol	Name	Description
7	EN	End of Cylinder	The 82078 tried to access a section beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data Command.
6	—	—	Unused. This bit is always "0".
5	DE	Data Error	The 82078 detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/Underrun	Becomes set if the 82078 does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3	—	—	Unused. Ths bit is always "0".
2	ND	No Data	Any one of the following: 1. READ DATA, READ DELETED DATA command, the 82091AA did not find the specified sector. 2. READ ID command, the 82091AA cannot read the ID field without an error. 3. READ TRACK command, the 82091AA cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the 82091AA is executing a WRITE DATA, WRITE DELETED DATA, or FORMAT TRACK command.
0	MA	Missing Address Mark	Any one of the the following: 1. The 82091AA did not detect an ID address mark at the specified track after encountering the index pulse from the INDX# pin twice. 2. The 82091AA cannot detect a data address mark or a deleted data address mark on the specified track.

8.5.1.3 Status Register 2

Bit #	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: 1. READ DATA command, the 82078 encounters a deleted data address mark. 2. READ DELETED DATA command, the 82078 encountered a data address mark.
5	DD	Data Error in Data Field	The 82091AA detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82091AA.
3	—	—	Unused. This bit is always "0".
2	—	—	Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82091AA and is equal to FF hex which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The 82091AA cannot detect a data address mark or a deleted data address mark.

8.5.1.4 Status Register 3

Bit #	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5	—	—	Unused. This bit is always "0".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3	—	—	Unused. This bit is always "0".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

8.5.2 DATA TRANSFER COMMANDS

All of the READ DATA, WRITE DATA and VERIFY type commands use the same parameter bytes and return the same results information. The only difference being the coding of bits[4:0] in the first byte.

An implied seek will be executed if the feature was enabled by the CONFIGURE Command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. A seek portion failure is reflected in the results status normally returned for a READ/WRITE DATA Command. Status Register 0 (ST0) contains the error code and C contains the cylinder that the seek failed.

8.5.2.1 Read Data

A set of nine bytes is required to place the FDC into the Read Data Mode. After the READ DATA Command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the SPECIFY Command), and begins reading ID address marks and ID fields. When the sector address read from the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one, and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC or an implied TC (FIFO overrun/underrun), the FDC stops sending data. However, the FDC will continue to read data from the current sector, check the CRC bytes, and, at the end of the sector, terminate the READ DATA Command.

N determines the number of bytes per sector (Table 25). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128 byte sector and checks for CRC errors. For writes it completes the 128 byte sector by filling in zeroes. If N is not set to 00h, DTL should be set to FFh, and has no impact on the number of bytes transferred.

Table 25. Sector Sizes

N	Sector Size
00	128 Bytes
01	256 Bytes
02	512 Bytes
03	1024 Bytes
...	...
07	16 KBytes

The amount of data that can be handled with a single command to the FDC depends on MT (multi-track) and N (Number of bytes/sector).

Table 26. Effects of MT and N Bits

MT	N	Max. Transfer Capacity	Final Sector Read from Disk
0	1	256 × 26 = 656	26 at side 0 or 1
1	1	256 × 52 = 13312	26 at side 1
0	2	512 × 15 = 7680	15 at side 0 or 1
1	2	512 × 30 = 15360	15 at side 1
0	3	1024 × 8 = 8192	8 at side 0 or 1
1	3	1024 × 16 = 16384	16 at side 1

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at sector 1, side 0 and completing at the last sector of the same track at side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent on the state of the MT bit and EOT byte. Refer to Table 29. The termination must be normal.

At the completion of the READ DATA Command, the head is not unloaded until after the Head Unload Time Interval (specified in the SPECIFY Command) has elapsed. If the host issues another command before the head unloads, the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the INDEX# pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC

code in Status Register 0 to 01 (Abnormal termination), sets the ND bit in Status Register 1 to 1 indicating a sector not found and terminates the READ DATA Command.

After reading the ID and data fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to 01 (Abnormal termination), sets the DE bit flag in Status Register 1 to 1, sets the DD bit in Status Register 2 to 1 if CRC is incorrect in the ID field, and terminates the READ DATA Command.

Table 27 describes the affect of the SK bit on the READ DATA command execution and results.

8.5.2.2 Read Deleted Data

This command is the same as the READ DATA Command, except that it operates on sectors that contain a deleted data address mark at the beginning of a data field. Table 28 describes the affect of the SK bit on the READ DELETED DATA Command execution and results.

Table 27. Skip Bit vs READ DATA Command

SK Bit Value	Data Address Mark Type Encountered	Sector Read	Results CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	No	Normal Termination
0	Deleted Data	Yes	Yes	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	Yes	No	Normal Termination
1	Deleted Data	No	Yes	Normal Termination Sector Not Read ("Skipped")

Except where noted in Table 27, the C or R value of the sector address is automatically incremented (see Table 29).

Table 28. Skip Bit vs READ DELETED DATA Command

SK Bit Value	Data Address Mark Type Encountered	Sector Read	Results CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	Yes	Normal Termination
0	Deleted Data	Yes	No	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	No	Yes	Normal Termination Sector Not Read ("Skipped")
1	Deleted Data	Yes	No	Normal Termination

Except where noted in Table 28, the C or R value of the sector address is automatically incremented (see Table 29).

Table 29. Result Phase

MT	Head	Final Sector Transferred to Host	ID Information at Result Phase			
			C	H	R	N
	0	Less than EOT	NC	NC	R+1	NC
0		Equal to EOT	C+1	NC	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
	0	Less than EOT	NC	NC	R+1	NC
1		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	LSB	01	NC

NOTE:
1. NC = no change; the same value as the one at the beginning of command execution.
2. LSB = least significant bit; the LSB of H is complemented.

8.5.2.3 Read Track

This command is similar to the READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the INDEX# pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag to 1 in Status Register 1 if there is no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (Bits D7 and D5 of the first command byte respectively) should always be set to 0.

This command terminates when the EOT specified number of sectors have been read. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the INDEX# pin, then it sets the IC code in Status Register 0 to 01 (Abnormal termination), sets the MA bit in Status Register 1 to 1, and terminates the command.

8.5.2.4 Write Data

After the WRITE DATA Command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the SPECIFY Command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO, and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The sector number stored in R is incremented by one, and the FDC continues writing to the next data field. The FDC continues this multi-sector write operation. If a terminal count signal is received or a FIFO over/under run occurs while a data field is being written, the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to 01 (Abnormal termination), sets the DE bit of Status Register 1 to 1, and terminates the WRITE DATA Command.

The WRITE DATA Command operates in much the same manner as the READ DATA Command. The following items are the same. Please refer to the READ DATA Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command
- Definition of DTL when N=0 and when N does not=0

8.5.2.5 Verify

The VERIFY Command is used to verify the data stored on a disk. This command acts exactly like a READ DATA Command except that no data is transferred to the host. Data is read from the disk, and CRC is computed and checked against the previously stored value.

Because no data is transferred to the host, the TC signal cannot be used to terminate this command. By setting the EC bit to 1, an implicit TC will be issued to the FDC. This implicit TC occurs when the SC value has decrement to 0 (a SC value of 0 verifies 256 sectors). This command can also be terminated by setting the EC bit to 0 and the EOT value equal to the final sector to be checked. When EC=0, DTL/SC should be programmed to 0FFh. Refer to Table 29 and Table 30 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left that can be read, including side 1 of the disk when MT=1.

Table 30. Verify Command Result Phase

MT	EC	SC/EOT Value	Termination Result
0	0	SC=DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	0	SC=DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC=DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC=DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

NOTE:
When MT=1 and the SC value is greater than the number of remaining formatted sectors on Side 0, verification continues on Side 1 of the disk.

8.5.2.6 Format Track

The FORMAT TRACK Command allows an entire track to be formatted. After a pulse from the INDEX# pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields and data fields, per the IBM* System 34 (MFM). The particular values written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host. That is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number, and sector size, respectively).

After formatting each sector, the host must send new values for C, H, R, and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (inter-leaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the INDEX# pin again and it terminates the command.

Table 31 contains typical values for gap fields that are dependent on the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

Table 31. Typical PC/AT Values for Formatting

Drive Form	MEDIA	Sector Size	N	SC	GPL1	GPL2
5.25″	1.2 MB	512	02	0F	2A	50
	360 KB	512	02	09	2A	50
3.5″	2.88 MB	512	02	24	38	53
	1.44 MB	512	02	18	1B	54
	720 KB	512	02	09	1B	54

NOTES:
1. All values are in hex, except sector size.
2. Gap3 is programmable during reads, writes, and formats.
3. GPL1 = suggested Gap3 values in read and write commands to avoid splice point between data field and ID field of contiguous sections.
4. GPL2 = suggested Gap3 value in FORMAT TRACK Command.

8.5.2.7 Format Field

System 34 Format Double Density

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		C	H	S	N	C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE	Y L	D	E C	O	R C	22x 4E	12x 00	3x A1	FB F8		R C		

ISO Format

GAP 1	SYNC	IDAM		C	H	S	N	C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP 4b
32x 4E	12x 00	3x A1	FE	Y L	D	E C	O	R C	22x 4E	12x 00	3x A1	FB F8		R C		

Perpendicular Format

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		C	H	S	N	C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE	Y L	D	E C	O	R C	41x 4E	12x 00	3x A1	FB F8		R C		

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Figure 64. System 34, ISO and Perpendicular Formats

8.5.3 CONTROL COMMANDS

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete; READ ID, RECALIBRATE and SEEK. The other control commands do not generate an interrupt.

8.5.3.1 READ ID Command

The READ ID Command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the INDEX# pin, it then sets the IC code in Status Register 0 to 01 (Abnormal termination), sets the MA bit in Status Register 1 to 1, and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is recommended that control commands be followed by the SENSE INTERRUPT STATUS Command. Otherwise, valuable interrupt status information will be lost.

8.5.3.2 RECALIBRATE Command

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the TRK0 pin from the FDD. As long as the TRK0 pin is low, the DIR# pin remains 0 and step pulses are issued. When the TRK0 pin goes high, the SE bit in Status Register 0 is set to 1, and the command is terminated. If the TRK0 pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to 1 and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one RECALIBRATE Command to return the head back to physical Track 0.

The RECALIBRATE Command does not have a result phase. The SENSE INTERRUPT STATUS Command must be issued after the RECALIBRATE Command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the busy state, but during the execution phase it is in a non-busy state. At this time another RECALIBRATE Command may be issued, and in this manner, parallel RECALIBRATE operations may be done on up to 2 drives simultaneously.

After powerup, software must issue a RECALIBRATE Command to properly initialize all drives and the controller.

8.5.3.3 DRIVE SPECIFICATION Command

The FDC uses two pins, DRVDEN0 and DRVDEN1 to select the density for modern drives. These signals inform the drive of the type of diskette in the drive. The DRIVE SPECIFICATION Command specifies the polarity of the DRVDEN0 and DRVDEN1 pins. It also enables/disables DSR programmed precompensation.

This command removes the need for a hardware work-around to accommodate differing specifications among drives. By programming this command during BIOS's POST routine, the floppy disk controller internally configures the correct values for DRVDEN0 and DRVDEN1 with corresponding precompensation value and data rate table enabled for the particular type of drive.

This command is protected from software resets. After executing the DRIVE SPECIFICATION Command, subsequent software resets will not clear the programmed parameters. Only another DRIVE SPECIFICATION Command or hard reset can reset it to default values. The 6 LSBs of the last byte of this command are reserved for future use.

The DRATE0 and DRATE1 are values as programmed in the DSR register. See Table 32 for pin decoding at different data rates.

Table 32 describes the drives that are supported with the DT0, DT1 bits of the DRIVE SPECIFICATION Command:

Table 32. DRVDENn Polarities

DT1	DT0	Data Rate	DRVDEN1	DRVDEN0
0*	0*	1 Mbps	1	1
		500 Kbps	0	1
		300 Kbps	1	0
		250 Kbps	0	0
0	1	1 Mbps	1	0
		500 Kbps	0	0
		300 Kbps	1	1
		250 Kbps	0	1
1	0	1 Mbps	1	1
		500 Kbps	0	0
		300 Kbps	1	0
		250 Kbps	0	1
1	1	1 Mbps	1	1
		500 Kbps	0	0
		300 Kbps	0	1
		250 Kbps	1	0

NOTE:
(*) Denotes the default setting

8.5.3.4 SEEK Command

The read/write head within the drive is moved from track to track under the control of the SEEK Command. The FDC compares the PCN which is the current head position with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to 1 (step in), and issues step pulses.

PCN > NCN: Direction signal to drive set to 0 (step out), and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN, then the SE bit in Status Register 0 is set to 1, and the command is terminated.

During the command phase of the seek or recalibrate operation, the FDC is in the busy state, but during the execution phase it is in the non-busy state.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1. SEEK Command;
   Step to the proper track
2. SENSE INTERRUPT STATUS Command;
   Terminate the SEEK Command
3. READ ID.
   Verify head is on proper track
4. Issue READ/WRITE Command.

The SEEK Command does not have a result phase. Therefore, it is highly recommended that the SENSE INTERRUPT STATUS Command be issued after the SEEK Command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return a 0. When exiting DSR Powerdown mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the DSR POWERDOWN Command, it is highly recommended that the user service all pending interrupts through the SENSE INTERRUPT STATUS Command.

8.5.3.5 SENSE INTERRUPT STATUS Command

An interrupt signal on the INT pin is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. READ DATA Command
   b. READ TRACK Command
   c. READ ID Command
   d. READ DELETED DATA Command
   e. WRITE DATA Command
   f. FORMAT TRACK Command
   g. WRITE DELETED DATA Command
   h. VERIFY Command
2. End of SEEK, RELATIVE SEEK or RECALIBRATE Command
3. FDC requires a data transfer during the execution phase in the non-DMA Mode

The SENSE INTERRUPT STATUS Command resets the interrupt signal and via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt. If a SENSE INTERRUPT STATUS Command is issued when no active interrupt condition is present, the status register ST0 will return a value of 80h (invalid command).

The SEEK, RELATIVE SEEK and the RECALIBRATE Commands have no result phase. The SENSE INTERRUPT STATUS Command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a 0. If a SENSE INTERRUPT STATUS is not issued, the drive, will continue to be busy and may effect the operation of the next command.

8.5.3.6 SENSE DRIVE STATUS Command

The SENSE DRIVE STATUS Command obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. STATUS REGISTER 3 contains the drive status information.

8.5.3.7 SPECIFY Command

The SPECIFY Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between the command phase to the execution phase of a READ DATA or Write Data Command. The Head Unload Time (HUT) timer goes from the end of the execution phase to the begining of the result phase of a READ Data or Write Data Command. The values change with the data rate speed selection and are documented in Table 34.

Table 33. Interrupt Identification

SE	IC	Interrupt Due To
0	11	Polling
1	00	Normal Termination of SEEK or RECALIBRATE Command
1	01	Abnormal Termination of SEEK or RECALIBRATE Command

Table 34. Drive Control Delays (ms)

	HUT				SRT			
	1 M	500K	300K	250K	1 M	500K	300K	250K
0	128	256	426	512	8.0	16	26.7	32
1	8	16	26.7	32	7.5	15	25	30
..	..	..	..	..	..	..	..	..
A	80	160	267	320	3.0	6.0	10.2	12
B	88	176	294	352	2.5	5.0	8.3	10
C	96	192	320	384	2.0	4.0	6.68	8
D	104	208	346	416	1.5	3.0	5.01	6
E	112	224	373	448	1.0	2.0	3.33	4
F	120	240	400	480	0.5	1.0	1.67	2

Table 35. Head Load Time (ms)

	HLT			
	1M	500K	300K	250K
00	128	256	426	512
01	1	2	3.3	4
02	2	4	6.7	8
..	..	..	..	..
7E	126	252	420	504
7F	127	254	423	508

The choice of DMA or non-DMA operations is made by the ND bit. When ND = 1, the non-DMA mode is selected, and when ND = 0, the DMA mode is selected. In DMA mode, data transfers are signalled by the DRQ pin. Non-DMA mode uses the RQM bit and the IRQ6 pin to signal data transfers.

8.5.3.8 CONFIGURE Command

Issue the configure command to enable features like the programmable FIFO and set the begining track for precompensation. A CONFIGURE Command need not be issued if the default values of the FDC meets the system requirements.

CONFIGURE DEFAULT VALUES:

EIS	No Implied Seeks
EFIFO	FIFO Disabled
POLL	Polling Enabled
FIFOTHR	FIFO Threshold Set to 1 Byte
PRETRK	Pre-Compensation Set to Track 0

EIS—Enable Implied Seek. When EIS = 1, the FDC will perform a SEEK operation before executing a read/write command. The default value is 0 (no implied seek).

EFIFO—Enable FIFO. When EFIFO = 1, the FIFO is disabled (8272A compatible mode). This means data transfers are asked for on a byte by byte basis. The default value is 1 (FIFO disabled). The threshold defaults to one.

POLL—Disable Polling. When POLL = 1, polling of the drives is disabled. POLL Defaults to 0 (polling enabled). When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR—The FIFO threshold in the execution phase of a read/write command. This is programmable from 1 to 16 bytes. FIFOTHR defaults to one byte. A 00 selects one byte and a 0F selects 16 bytes.

PRETRK—Precompensation start track number. Programmable from track 0 to 255. PRETRK defaults to track 0. A 00h selects track 0 and a FFh selects 255.

8.5.3.9 VERSION Command

The VERSION Command checks to see if the controller is an enhanced type (82077, 82077AA, 82077SL) or the older type (8272A/765A). A value of 90h is returned as the result byte, defining an enhanced FDD controller is in use. No interrupts are generated.

8.5.3.10 RELATIVE SEEK Command

The RELATIVE SEEK Command is coded the same as for the SEEK Command, except for the MSB of the first byte and the DIR# bit.

DIR# Head Step Direction Control

DIR#	ACTION
0	Step Head Out
1	Step Head In

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The RELATIVE SEEK Command differs from the SEEK Command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The SEEK Command is good for drives that support a maximum of 256 tracks. RELATIVE SEEKs cannot be overlapped with other RELATIVE SEEKs. Only one RELATIVE SEEK can be active at a time. Bit 4 of Status Register 0 (EC) will be set to 1 if RELATIVE SEEK attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks and that the host needs to read track 300 and the head is on any track (0–255). If a SEEK Command is issued, the head stops at track 255. If a RELATIVE SEEK Command is issued, the FDC moves the head the specified number of tracks, regardless of the internal cylinder position register (but increments the register). If the head had been on track 40 (D), the maximum track that the FDC could position the head on using RELATIVE SEEK, is 296 (D), the initial track, +256 (D). The maximum count that the head can be moved with a single RELATIVE SEEK Command is 256 (D).

The internal register, PCN, would overflow as the cylinder number crossed track 255 and would contain 40 (D). The resulting PCN value is thus (NCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255(D). It is the users responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued uses the current PCN value, except for the RECALIBRATE Command that only looks for the TRACK0 signal. RECALIBRATE returns an error if the head is farther than 79 due to its limitation of issuing a maximum 80 step pulses. The user simply needs to issue a second RECALIBRATE Command. The SEEK Command and implied seeks function correctly within the 44 (D) track (299–255) area of the extended track area. It is the users responsibility not to issue a new track position that exceeds the maximum track that is present in the extended area.

To return to the standard floppy range (0–255) of tracks, a RELATIVE SEEK is issued to cross the track 255 boundary.

A RELATIVE SEEK Command can be used instead of the normal SEEK Command but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a READ ID Command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands return different cylinder results which may be difficult to keep track of with software without the READ ID Command.

8.5.3.11 DUMPREG Command

The DUMPREG Command is designed to support system run-time diagnostics and application software development and debug. The command returns pertinent information regarding the status of many of the programmed fields in the FDC. This can be used to verify the values initialized in the FDC.

8.5.3.12 PERPENDICULAR MODE Command

An added capability of the FDC is the ability to interface directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method by orienting the magnetic bits vertically. This scheme packs in more data bits for the same area.

The PERPENDICULAR MODE Command allows the system designers to designate specific drives as Perpendicular recording drives. Data transfers be-

tween Conventional and Perpendicular drives are allowed without having to issue PERPENDICULAR MODE Commands between the accesses of the two different drives, nor having to change write precompensation values.

With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 36 describes the effects of the WGATE and GAP bits for the PERPENDICULAR MODE Command.

When both GAP and WGATE equal 0 the PERPENDICULAR MODE Command will have the following effect on the FDC:

1. If any of the new bits D0 and D1 are programmed to 1, the corresponding drive is automatically programmed for Perpendicular mode (ie: GAP2 being written during a write operation, the programmed Data Rate will determine the length of GAP2), and data will be written with 0 ns write precompensation.
2. Any of the new bits (DO/D1) are programmed for 0, the designated drive is programmed for Conventional Mode and data will be written with the currently programmed write precompensation value.
3. Bits D0 and D1 can only be over-written when the OW bit is 1. The status of these bits can be determined by interpreting the eighth result byte of the DUMPREG Command. (Note: if either the GAP or WGATE bit is 1, bits D0 and D1 are ignored.)

Software and Hardware reset have the following effects on the enhanced PERPENDICULAR MODE Command:

1. A software reset (Reset via DOR or DSR registers) only sets GAP and WGATE bits to 0; D0 and D1 retain their previously programmed values.
2. A hardware reset (Reset via pin 32) sets all bits (GAP, Wgate, D0, and D1) to 0 (All Drives Conventional Mode).

8.5.3.13 POWERDOWN MODE Command

The POWERDOWN MODE Command allows the automatic power management and enables the enhanced registers (EREG EN) of the FDC. The use of the command can extend the battery life in portable PC applications. To enable auto powerdown the command may be issued during the BIOS power on self test (POST).

This command includes the ability to configure the FDC into the enhanced mode extending the SRB and TDR registers. These extended registers accommodate bits that give more information about floppy drive interface, allow for boot drive selection, and identify the values of the PD and IDLE status.

As soon as the command is enabled, a 10 ms or a 0.5 sec minimum powerup timer is initiated, depending on whether the MIN DLY bit is set to 0 or 1. This timer is one of the required conditions that has to be satisfied before the FDC will enter auto powerdown.

Table 36. Effects of WGATE and GAP Bits

GAP	WGATE	MODE	VCO Low Time after Index Pulse	Length of Gap2 Format Field	Portion of Gap2 Written by Write Data Operation	Gap2 VCO Low Time for Read Operations
0	0	Conventional Mode	33 Bytes	22 Bytes	0 Bytes	24 Bytes
0	1	Perpendicular Mode (500 Kbps and Lower Data Rates)	33 Bytes	22 Bytes	19 Bytes	24 Bytes
1	0	Reserved (Conventional)	33 Bytes	22 Bytes	0 Bytes	24 Bytes
1	1	Perpendicular Mode (1 Mbps Data Rate)	18 Bytes	41 Bytes	38 Bytes	43 Bytes

NOTE:
When either GAP or WGATE bit is set, the current value of precompensation in the DSR is used.

Any software reset will re-initialize the timer. The timer countdown is also extended by up to 10 ms if the data rate is changed during the timer's countdown. Without this timer, the FDC would have been put to sleep immediately after FDC is idle. The minimum delay gives software a chance to interact with the FDC without incurring an additional overhead due to recovery time.

The command also allows the output pins of the floppy disk drive interface to be tri-stated or left unaltered during auto powerdown. This is done by the FDI TRI bit. In the default condition (FDI TRI = 0) the output pins of the floppy disk drive are tri-stated. Setting this bit leaves the interface unchanged from the normal state.

The results phase returns the values programmed for MIN DLY, FDI TRI and AUTO PD. The auto powerdown mode is disabled by a hardware reset. Software results have no effect on the POWERDOWN MODE Command parameters.

8.5.3.14 PART ID Command

This command can be used to identify the floppy disk controller as an enhanced controller. The first stepping of the FDC (all versions) will yield 0x02 in the result phase of this command. Any future enhancements on these parts will be denoted by the 5 LSBs (0x01 to 0x1F).

8.5.3.15 OPTION Command

The standard IBM format includes an index address field consisting of 80 bytes of GAP 4a, 12 bytes of the sync field, four bytes identifying the IAM and 50 bytes of GAP 1. Under the ISO format most of this preamble is not used. The ISO format allows only 32 bytes of GAP 1 after the index mark. The ISO bit in this command allows the FDC to configure the data transfer commands to recognize this format. The MSBs in this command are reserved for any other enhancements made available to the user in the future.

8.5.3.16 SAVE Command

The first byte corresponds to the values programmed in the DSR with the exception of CLKSEL. The DRATE1, DRATE0 used here are unmapped. The second byte is used for configuring the bits from the OPTION Command. All future enhancements to the OPTION Command will be reflected in this byte as well. The next nine result bytes are explained in the Parameter Abbreviations section after the command summary. The 13th byte is the value associated with the POWERDOWN MODE Command. The disk status is used internally by the FDC. There are two reserved bytes at the end of this command for future use.

This command is similar to the DUMPREG Command but it additionally allows the user to read back the precompensation values as well as the programmed data rate. It also allows the user to read the values programmed in the POWERDOWN MODE Command. The precompensation values will be returned as programmed in the DSR register. This command, used in conjunction with the RESTORE Command, should prove very useful for SMM power management. This command reserves the last two bytes for future enhancements.

2

8.5.3.17 RESTORE Command

Using the RESTORE Command with the SAVE Command, allows the SMM power management to restore the FDC to its original state after a system powerdown. It also serves as a succinct way to provide most of the initialization requirements normally handled by the system. The sequence of initializing the FDC after a reset occurred and assuming a SAVE Command was issued follows:

- Issue the DRIVE SPECIFICATION Command (if the design utilizes this command)
- Issue the RESTORE Command (pass the 16 bytes retrieved previously during SAVE)

The RESTORE Command programs the data rate and precompensation value via the DSR. It then restores the values normally programmed through the CONFIGURE, SPECIFY, and PERPENDICULAR Commands. It also enables the previously selected values for the POWERDOWN Mode Command. The PCN values are set restored to their previous values and the user is responsible for issuing the SEEK and RECALIBRATE Commands to restore the head to the proper location. There are some drives that do not recalibrate in which case the RESTORE Command restores the previous state completely. The PDOSC bit is retrievable using the SAVE Command, however, the system designer must set it correctly. The software must allow at least 20 μs to execute the RESTORE Command. When using the BOOTSEL bits in the TDR, the user must restore or reinitialize these bits to their proper values.

8.5.3.18 FORMAT AND WRITE Command

The FORMAT AND WRITE Command is capable of simultaneously formatting and writing data to the diskette. It is essentially the same as the normal FORMAT Command. With the exception that included in the execution for each sector is not only the C, H, R, and N but also the data transfer of N bytes. The D value is ignored. This command formats the entire track. High speed floppy diskette duplication can be done fast and efficiently with this command. The user can format the diskette and put data on it in a single pass. This is very useful for software duplication applications by reducing the time required to format and copy diskettes.

9.0 IDE INTERFACE

The 82091AA supports the IDE (Integrated Drive Electronics) interface by providing two chip selects, and lower and upper data byte controls. DMA and 16-bit data transfers are supported. Minimal external logic is required to complete the optional 16-bit IDE I/O and DMA interfaces. With external logic, a fully buffered interface is also supported.

9.1 IDE Registers

The 82091AA does not contain IDE registers. All of the IDE device registers are located in the IDE device, except bit 7 of the Drive Address Register which is the Floppy Controller Disk Change status bit and is driven by the 82091AA.

The IDE interface contains two chip selects (IDECS0# and IDECS1#). These signals are asserted for accesses to the Command and Control Block registers located at 01Fxh and 03Fxh, respectively (Table 37).

Table 37. IDE Register Set (Located in IDE Device)

Primary Address	Secondary Address	Chip Select	Registers	Access
1F0h	170h	IDECS0#	Data Register	R/W
1F1h	171h	IDECS0#	Error Register	RO
1F1h	171h	IDECS0#	Write Precomp/Features Register	WO
1F2h	172h	IDECS0#	Sector Count Register	R/W
1F3h	173h	IDECS0#	Sector Number Register	R/W
1F4h	174h	IDECS0#	Cylinder Low Register	R/W
1F5h	175h	IDECS0#	Cylinder High Register	R/W
1F6h	176h	IDECS0#	Drive/Head Register	R/W
1F7h	177h	IDECS0#	Status Register	RO
1F7h	177h	IDECS0#	Command Register	WO
3F6h	376h	IDECS1#	Alternate Status Register	RO
3F6h	376h	IDECS1#	Digital Output Register	WO
3F7h	377h	IDECS1#	Drive Address Register	RO
3F7h	377h	IDECS1#	Not Used	

9.2 IDE Interface Operation

The 82091AA implements the chip select signals for the IDE interface and decodes the standard PC/AT primary and secondary I/O locations.

The 82091AA provides a data buffer enable signal (DEN#) to control the lower data byte path for buffered designs. Buffering the lower data byte path is an application option that requires an external transceiver/buffer. For buffered applications, DEN# controls an external transceiver and enables data bits IDED[7:0] onto the system data bus SD[7:0]. For non-buffered applications (typically the X-Bus configuration), IDED[7:0] are connected directly to the bus and DEN# is not used and becomes a no-connect. For 16-bit applications the upper data byte path (IDED[15:8]) is controlled by the HEN# signal.

Figure 65 shows an example IDE interface without DMA capability. In this case all IDE accesses for setting up the IDE registers and transferring data is programmed via I/O. The 82091AA generates the chip selects (IDECS0# and IDECS1#). The 82091AA also generates the DEN# and HEN# signals to enable the data buffers.

Figure 66 shows an example DMA IDE interface for type "F" DMA cycles. To set up the IDE interface, the host accesses the IDE registers on the IDE device. For programmed I/O accesses, the 82091AA generates the chip selects (IDECS0# and IDECS1#) to access the IDE registers and the DEN# and HEN# signals to control the data buffers. During DMA transfers the DMA handshake is between the DMA controller and IDE device via the DREQ and DACK# signals. The DACK# signal is ORed with the DEN# and HEN# signals to control the upper and lower byte buffers during DMA transfers.

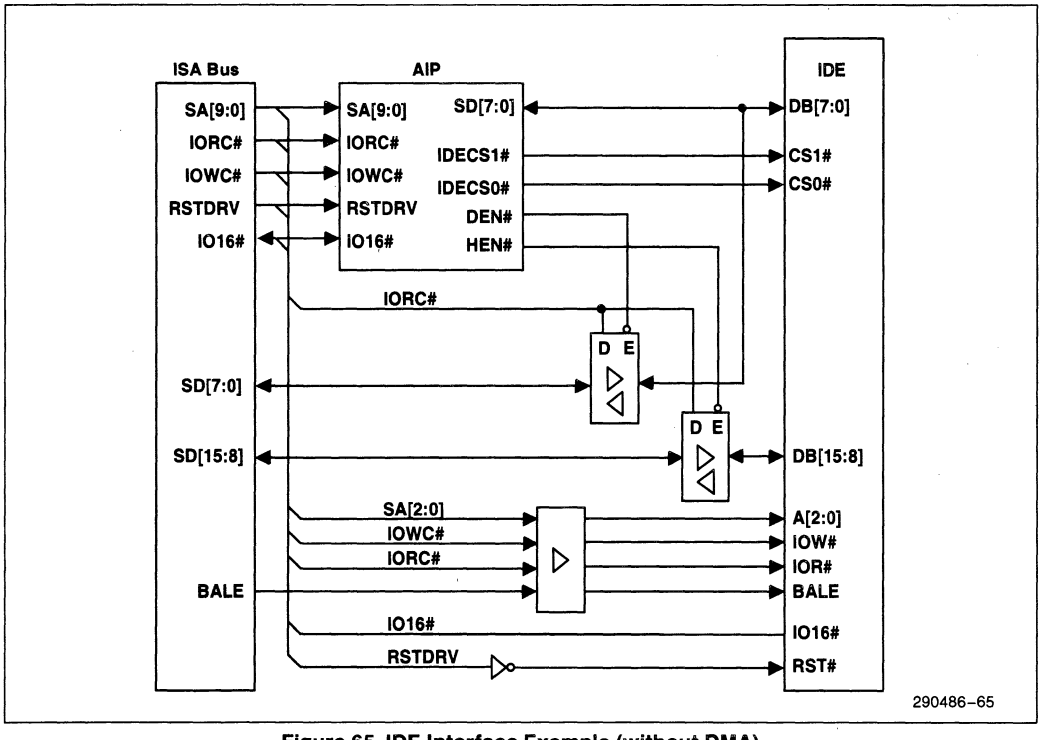


Figure 65. IDE Interface Example (without DMA)

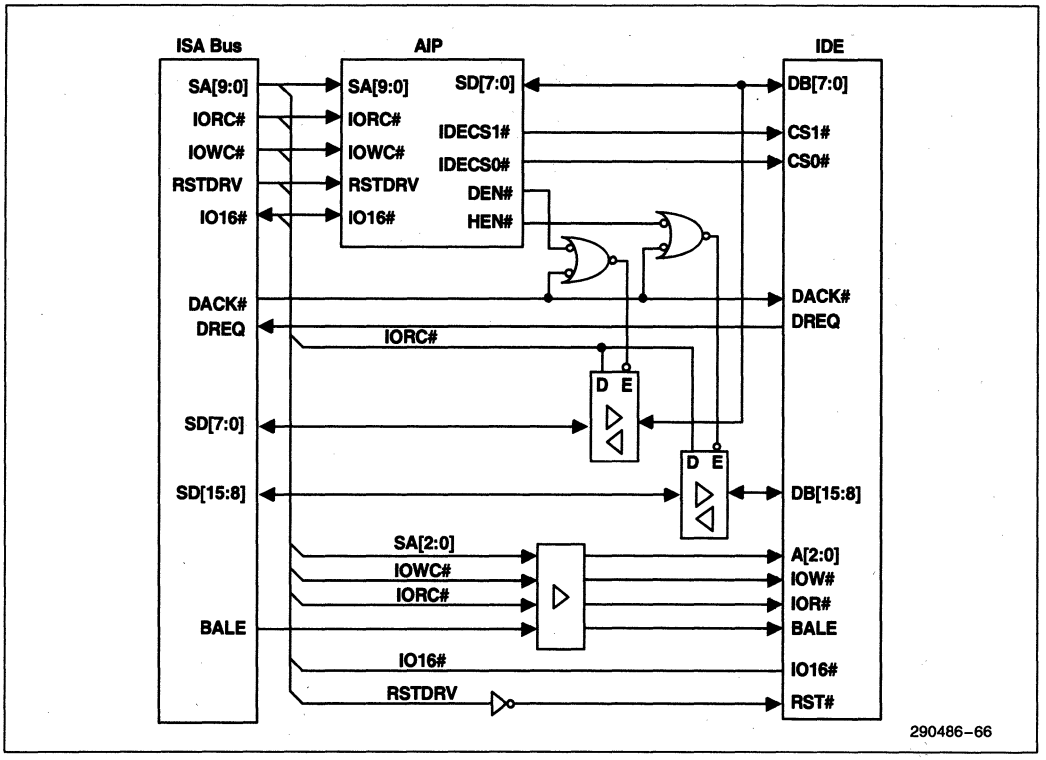


Figure 66. IDE Interface Example (with DMA)

10.0 POWER MANAGEMENT

The 82091AA provides power management capabilities for its primary functional modules (parallel port, floppy disk controller, serial port A, and serial port B). For each module, the 82091AA implements two types of power management—direct powerdown and auto powerdown. Direct powerdown, enabled via control bits in the 82091AA configuration registers, immediately places the module in a powerdown mode by turning off the clock to the associated module. Direct powerdown removes the clock regardless of the activity or status of the module. By contrast, when auto powerdown is enabled (via control bits in the 82091AA configuration registers), the associated module only enters a powerdown mode if it is in an idle state.

NOTE:
The entire 82091AA can be placed in direct powerdown by writing to the CLKOFF bit in the AIPCFG1 Register.

10.1 Power Management Registers

The floppy disk controller, parallel port, serial port A, and serial port B each have two 82091AA configuration registers. For each module, three configuration register bits control power management—xDPDN, xIDLE, and xAPDN.

- xAPDN: auto-powerdown, shuts off the oscillator to the module when the module is idle.
- xIDLE: idle status, a read only pin that indicates idle status.
- xDPDN: direct powerdown, shuts off module oscillator when active regardless of module status.

The 82091AA exits any powerdown mode after a hardware reset (RSTDRV asserted) or reset via the xRESET bit in the 82091AA configuration registers. Direct powerdown can also be exited by writing the corresponding xPDN bit in the configuration register to 0. Auto powerdown is exited by events at the module (e.g., CPU read/write or module interface activity).

NOTE:
The configuration registers also contain the xEN bit. This bit is used to completely disable an unused module. Enabling a disabled module takes much longer than restoring a module from powerdown. Therefore, this bit is not recommend for temporarily disabling a module as a powerdown scheme.

10.2 Clock Power Management

The internal clock circuitry of the 82091AA can be turned on or off as part of a power management scheme. The clock circuitry is controlled via the CLKOFF bit in the AIPCFG1 Register. If an external clock source exists, the user may want to turn off the internal oscillator to save power and provide minimum recovery time.

Auto powerdown and direct powerdown (in each module) have no effect on the state of internal oscillator.

10.3 FDC Power Management

This section describes the FDC direct and auto powerdown modes and recovery from the powerdown modes.

2

Auto Powerdown

Automatic powerdown (APDN) has an advantage over direct powerdown (PDN) since the register contents are not lost under APDN. Automatic powerdown is invoked by either the Auto Powerdown command, or by enabling the FAPDN bit in the FDC configuration register. There are four conditions required before the FDC will enter powerdown:

1. The motor enable pins ME[3:0] must be inactive.
2. The FDC must be in an idle state. FDC idle is indicated by MSR = 80h and the IRQ6 signal is negated (IRQ6 may be asserted even if MSR = 80h due to polling interrupt).
3. The head unload timer (HUT, explained in the SPECIFY Command) must have expired.
4. The auto powerdown timer must have timed out.

An internal timer is initiated when the POWERDOWN MODE Command is executed. The amount of time can be set by the user via the MIN DLY bits in the POWERDOWN MODE Command. The module is then powered down, provided all the remaining conditions are met. A software reset reinitializes the timer. When using the FDC FAPDN bit to enable the automatic powerdown feature, the MIN DLY bit is set to the default condition.

Recovery from Auto Powerdown

When the FDC is in auto powerdown, the module is awakened by a reset or access to the DOR, MSR or FIFO registers. The module remains in auto powerdown mode after a software reset (i.e., it will power-

down again after being idle for the time specified by MIN DLY). However, the FDC does not remain in auto powerdown mode after a hardware reset or DSR reset.

Direct Powerdown

Direct powerdown is invoked via the Powerdown bit in the Data Rate Select Register (bit 6), or the FDPDN bit in the FCFG2 Register. Setting FDPDN to 1 will powerdown the FDC. All status is lost when this type of powerdown mode is used. The FDC exits powerdown mode after any hardware or software reset. Direct powerdown overrides automatic powerdown.

Recovery from Direct Powerdown

The FDC exits the direct powerdown state by setting the FDPDN bit to 0 followed by a software or hardware reset.

After reset, the FDC goes through a normal sequence. The drive status is initialized. The FIFO mode is set to default mode on a hardware or software reset if the LOCK Command has not blocked it. Finally, after a delay, the polling interrupt is issued.

10.4 Serial Port Power Management

This section describes the serial port direct and auto powerdown modes and recovery from the powerdown modes.

Auto Powerdown

When auto powerdown is enabled in the SxCFG2 Register (SxAPDN bit is 1), the serial port enters auto powerdown based on monitoring line interface activity. During auto powerdown, the status of the serial port is maintained (the FIFO and registers are not reset). Access to any serial port register is allowed during auto powerdown. The transmitter and the receiver enter powerdown individually, depending on certain conditions. When there are no characters to transmit (TEMPTY = 1 in the LSR), the transmitter clock is shut off placing the transmitter in auto powerdown. In the case of the receiver, when serial input signal is inactive for approximately 5 character times, indicating that no character is being received, the receiver goes into auto powerdown.

Recovery from Auto Powerdown

The serial port recovers from auto powerdown when either the transmitter or receiver are active. If data is written to the transmitter or data is present at the receiver, the serial port exits from auto powerdown.

Direct Powerdown

Direct Powerdown is invoked via the SxCFG2 Register (setting the SxDPDN bit to 1). When in direct powerdown, the clock to the module is shut off. All registers are accessible while in direct powerdown. A host read of the Receiver Buffer Register or a write to the Transmitter Holding Register should not be performed during powerdown. The SINx input should remain static.

When direct powerdown is invoked, the transmit and receive sections of the serial port are reset, including the transmit and receive FIFOs. Thus, to prevent possible data loss when the FIFOs are reset, software should not invoke direct powerdown until the serial port is in the idle state as indicated by the SxIDLE bit in the SxCFG2 Register.

Recovery from Direct Powerdown

Recovery from direct powerdown is accomplished by writing the SxDPDN bit in the configuration register to 0 or by a module reset.

10.5 Parallel Port Power Management

Auto Powerdown

Auto powerdown is enabled via the PAPDN bit in the PCFG2 Register. When enabled, the parallel port enters auto powerdown when the module is in an idle state. If the parallel port FIFO is being used to transfer data, the parallel port is in an idle state when the FIFO is empty.

Recovery from Auto Powerdown

Recovery from auto powerdown occurs when the FIFO is written or as a result of parallel port interface activity.

Direct Powerdown

Direct powerdown is invoked via the PCFG2 Register (setting the PDPDN bit to 1). When PDPDN = 1, the clock to the printer state machine is disabled and the state machine goes into an idle state.

Recovery from Direct Powerdown

Recovery from direct powerdown is accomplished by setting the PDPDN bit to 0 or the PRESET bit to a 1 in the PCFG2 Register. An 82091AA hard reset (RSTDRV asserted) also brings the part out of direct powerdown.

11.0 ELECTRICAL CHARACTERISTICS

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

11.1 Absolute Maximum Ratings

Storage Temperature ..... −65°C to +150°C
Supply Voltage ..... −0.5V to +8.0V
Voltage on Any Input ..... GND−2V to 6.5V
Voltage on Any Output ... GND−0.5V to V_{CC} +0.5V
Power Dissipation 1W

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

11.2 DC Characteristics

Table 38. DC Specifications (V_{CC} = 5V ±10%, T_{amb} = 0°C to 70°C)

Symbol	Parameter	V_{CC} = +5V ±10			V_{CC} = 3.3V ±0.3V		
		Min(V)	Max(V)	Notes	Min(V)	Max(V)	Notes
V_{ILC}	Input Low Voltage, X1	−0.5	0.8		−0.3	0.8	
V_{IHC}	Input High Voltage, X1	3.9	V_{CC} + 0.5		2.4	V_{CC} + 0.3	
V_{IL}	Input Low Voltage (all pins except X1)	−0.5	0.8		−0.3	0.8	
V_{IH}	Input High Voltage (all pins except X1)	2.0	V_{CC} + 0.5		2.0	V_{CC} + 0.3	
I_{CC}	V_{CC} Supply Current − 1 Mbps FDC Data Rate V_{IL} = 0.45V, V_{IH} = 2.4V		50 mA	1, 2		40 mA	1, 2
I_{CCSB}	I_{CC} in Powerdown		100 µA	3, 4, 5		100 µA	3, 4, 5
I_{IL}	Input Load Current (all input pins)		+10µA −10 µA	6		+10 µA −10 µA	6
I_{OFL}	Data Bus Output Float Leakage		+10 µA −10 µA	7		+10 µA −10 µA	8
I_{BPL}	Parallel Port Back-Power Leakage (All Parallel Port Signals)		+10 µA	9		+10 µA	9

NOTES:
1. Test Conditions: Only the data bus inputs may float. All outputs are open.
2. Test Conditions: Tested while reading a sync field of "00". Outputs not connected to DC loads. This specification reflects the supply current when all modules within the 82091AA are active.
3. Test Conditions: $V_{IL} = V_{SS}$, $V_{IH} = V_{CC}$; Outputs not connected to DC loads.
4. Test Conditions: Typical value with the oscillator off.
5. Test Conditions: All 82091AA modules are in their powerdown state.
6. Test Conditions: 10 µA ($V_{IN} = V_{CC}$), −10µA (V_{IN} = 0V)
7. Test Conditions: $0V < V_{OH} < V_{CC}$
8. Test Conditions: $0.45V < V_{OH} < V_{CC}$
9. Test Conditions: Device in Circuit V_{CC} = 0V, V_{IN} = 5.5V max.

Table 39. Capacitance Specifications (V_{CC} = 5V ±10%, T_{amb} = 0°C to 70°C)

C_{IN}	Input Capacitance	10	pF	F = 1 MHz, T_A = 25°C
C_{IN1}	Clock Input Capacitance	20	pF	Sampled, not 100% Tested
$C_{I/O}$	Input/Output Capacitance	20	pF	

NOTE:
All pins except pins under test are tied to AC ground.

The following pin groupings are used in Table 40 and Table 41.

DMA FDDREQ, PPDREQ

IRQx IRQ3, IRQ4, IRQ5, IRQ6, IRQ7

Serial Port SOUTA, SOUTB, DTRA#, DTRB#, RTSA#, RTSB#

Parallel Port PD[7:0], STROBE#, AUTOFD#, INIT#, SELECTIN#

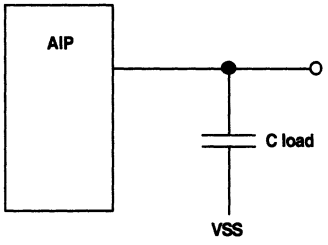
FDC Interface WRDATA, HDSEL#, STEP#, DIR#, WE#, FDME0#, FDME1#, FDS0#, FDS1#, DRVDEN[1:0]

Table 40. V_{OL} Specifications (V_{CC} = 5V ±10%, T_{amb} = 0°C to 70°C)

Symbol	Signal	V_{CC} = 5V ± 10%			V_{CC} 3.3V ± 0.3V		
		Min	Max	I_{OL}	Min	Max	I_{OL}
V_{OL}	SD[7:0]		0.45V	24 mA		0.45V	12 mA
V_{OL}	NOWS#, IOCHRDY		0.45V	24 mA		0.45V	12 mA
V_{OL}	DMA,IRQx		0.45V	12 mA		0.45V	6 mA
V_{OL}	Serial Port		0.45V	4 mA		0.45V	2 mA
V_{OL}	Parallel Port		0.45V	16 mA		0.45V	8 mA
V_{OL}	PPDIR,GCS#		0.45V	4 mA		0.45V	2 mA
V_{OL}	FDC Interface		0.45V	12 mA		0.45V	6 mA
V_{OL}	DEN#,HEN#		0.45V	4 mA		0.45V	2 mA
V_{OL}	IDECS[1:0]#		0.45V	12 mA		0.45V	6 mA

Table 41. V_{OH} Specifications (V_{CC} = 5V ±10%, T_{amb} = 0°C to 70°C)

Symbol	Signal	V_{CC} = 5V ± 10%			V_{CC} 3.3V ± 0.3V		
		Min	Max	I_{OH}	Min	Max	I_{OH}
V_{OH}	SD[7:0]	2.4V		4 mA	2.4V		2 mA
V_{OH}	DMA,IRQx	2.4V		4 mA	2.4V		2 mA
V_{OH}	Serial Port	2.4V		1 mA	2.4V		1 mA
V_{OH}	Parallel Port	2.4V		4 mA	2.4V		50 μA
V_{OH}	PPDIR,GCS#	2.4V		1 mA	2.4V		1 mA
V_{OH}	FDC Interface	2.4V		4 mA	2.4V		2 mA
V_{OH}	DEN#, HEN#	2.4V		1 mA	2.4V		1 mA
V_{OH}	IDECS[1:0]#	2.4V		4 mA	2.4V		2 mA



C load = 50 pF for all logic outputs and
100 pF for the data bus.

290486-67

Figure 67. Load Circuit

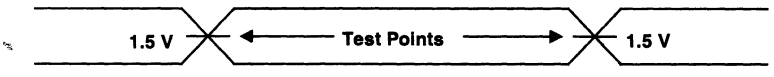


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Figure 68. AC Testing Input, Output

11.3 Oscillator

The 24 MHz clock can be supplied either by a crystal (Figure 69) or a MOS level square wave. All internal timings are referenced to this clock or a scaled count that is data rate dependent. The crystal oscillator must be allowed to run for 10 ms after V_{CC} has reached 4.5V or exiting the POWERDOWN mode to guarantee that it is stable.

Crystal Specifications:

Freq:	24 MHz ± 0.1%
Mode:	Parallel Resonant
	Fundamental Mode
Series Resistance:	< 40Ω
Shunt Capacitance:	< 5 pF
C1, C2:	20 pF–25 pF

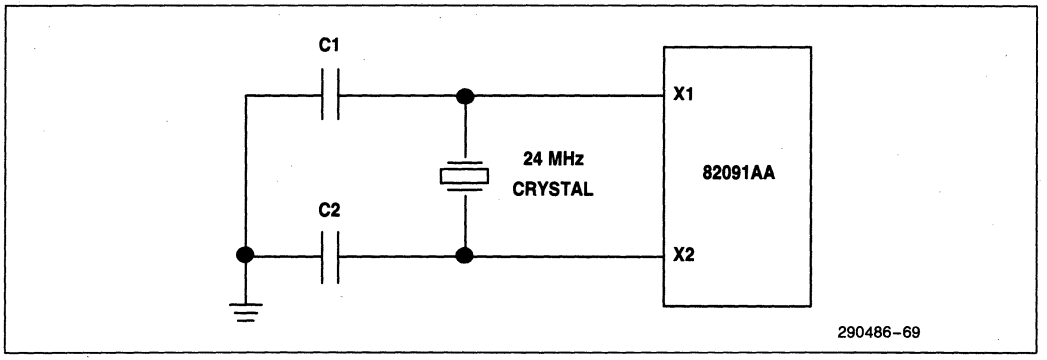


Figure 69. Crystal Connections

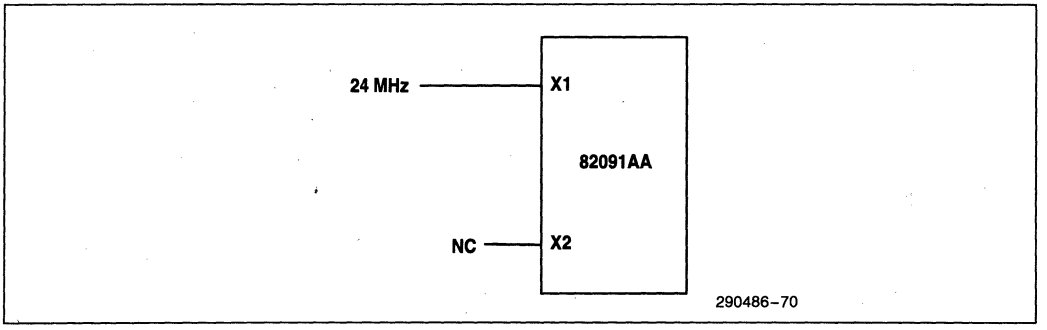


Figure 70. Oscillator Connections

11.4 AC Characteristics

Table 42. AC Specifications (V_{CC} = 5V ± 10%, T_{amb} = 0°C to 70°C)

Symbol	Parameter	24 MHz		Units	Notes	Figure
		Min	Max			
t1a	Clock Rise and Fall Time		10	ns	1	71
t1b	Clock High Time	16		ns	1	71
t1c	Clock Low Time	16		ns	1	71
t1d	Clock Period	41.66	41.66	ns	2	71
t1e	Internal Clock Period				3	

NOTES:
1. Clock input high level test points for clock high time and clock rise/fall times are 3.5V with V_{CC} at 5V ±10% and 2.0V with V_{CC} at 3.3V V_{CC} ±10%. Clock input low level test point for clock low time and clock rise/fall time is 0.8V.
2. Clock input test point for clock period is 0.8V.
3. Certain Floppy Disk Controller module timings are a function of the selected data rate. The nominal values for the internal clock period (t1e) for the various data rates are:

Disk Drive Disk Rate	Internal Clock Period (*nominal values)
	24 MHz
1 Mbps	125 ns
500 Kbps	250 ns
300 Kbps	420 ns
250 Kbps	500 ns

All information contained in ( ) in the following tables represents 3.3V specifications.

Table 43. AC Specifications (V_{CC} = 5V ± 10%, or [3.3V ± 0.3V] T_{amb} = 0°C to 70°C)

Symbol	Parameter	Min	Max	Units	Notes	Figure
	Host					
	SA[10:0]					
t2a	SA[10:0] Setup to IORC#/IOWC# Active	18 (25)		ns		72, 73
t2b	SA[10:0] Hold from IORC#/IOWC# Inactive	0		ns		72, 73
	SD[7:0]					
t3a	SD[7:0] Valid Delay from IORC# Active		70 (100)	ns	1	72
t3b	SD[7:0] Float Delay from IORC# Inactive	5	35 (40)	ns		72
t3c	SD[7:0] Setup to IOWC# Inactive	35		ns		73
t3d	SD[7:0] Hold from IOWC# Inactive	0		ns		73

Table 43. AC Specifications (V_{CC} = 5V ± 10%, or (3.3V ± 0.3V) T_{amb} = 0°C to 70°C) (Continued)

Symbol	Parameter	Min	Max	Units	Notes	Figure
	IOCHRDY					
t4a	IOCHRDY Propagation Delay from IORC#/ IOWC#		55 (75)	ns	EPP	82, 83
t4b	IOCHRDY Propagation Delay from BUSY		34 (65)	ns	EPP	82, 83
	IORC#					
t5a	IORC# Active Pulse Width	90		ns		72
t5b	IORC# Recovery Time	60		ns		72
	IOWC#					
t6a	IOWC# Active Pulse Width	90		ns		73
t6b	IOWC# Recovery Time	60		ns		73
	AEN					
t7a	AEN Setup to IORC#/IOWC# Active	18		ns		72, 73
t7b	AEN Hold from IORC#/IOWC# Inactive	0		ns		72, 73
	NOWS#					
t8a	NOWS# Delay from IORC#/IOWC#		35 (50)	ns		72, 73
	TC					
t9a	TC Active Pulse Width	50		ns	6	74
	RESET					
	RSTDRV					
t10a	RSTDRV Active Pulse Width	0.5		μs		75
t10b	Hardware Configuration Input Setup to RSTDRV Inactive	100		ns	All Configuration Modes	76
t10c	Hardware Configuration Input Hold from RSTDRV Inactive	0			All Configuration Modes	76
	INTERRUPTS					
	RQ[4,3] (Serial Ports)					
t11b	IRQ[4,3] Inactive Delay from IORC#/ IOWC# Active		100	ns	THR wr, RBR rd, MSR rd	90, 91
t11c	IRQ[4,3] Inactive Delay from IORC# Inactive		100	ns	IIR rd, LSR rd	90
t11d	IRQ[4,3] Active Delay from DCD#/DSR#/ CTS#/RI#		80	ns		91

Table 43. AC Specifications (V_{CC} = 5V ± 10%, or (3.3V ± 0.3V) T_{amb} = 0°C to 70°C) (Continued)

Symbol	Parameter	Min	Max	Units	Notes	Figure
INTERRUPTS						
IRQ[7,5] (Parallel Port)						
t12b	IRQ[7,5] Inactive Delay from IORC#/ IOWC# Active		70 (90)	ns	ECP rev, fwd to FIFO	81
t12c	IRQ[7,5] Inactive Delay from IOWC# Inactive		70 (95)	ns	ECP fwd to ECR	81
t12d	IRQ[7,5] Delay from ACK#		70 (90)	ns	All Modes	81
t12e	IRQ[7,5] Delay from FAULT#		70 (90)	ns	ECP	81
IRQ6 (FDC)						
t13b	IRQ6 Inactive Delay from IORC#/ IOWC# Active		t1e + 125	ns	2	80
DMA						
FDDREQ, PPDREQ						
t14a	xDREQ Inactive Delay from xDACK# Active		75 (100)	ns	4	74
t14b	FDREQ Cycle Time (Non-Burst DMA)	6.25		µs	3	74
t14c	xDREQ Active from IORC#/IOWC# Inactive	100		ns		74
t14d	xDREQ Setup IORC#/IOWC#	0		ns	3	74
t14e	xDREQ Delay from IORC#/IOWC# Active		75 (100)	ns	5	74
t14f	FDREQ Inactive Delay from TC Active PPDREQ Inactive Delay from TC Active		110 80 (90)	ns		74
t14g	xDREQ to xDACK# Inactive	⅔ t1e				74
FDDACK#, PPDACK#						
t15a	xDACK# Active Delay from xDREQ Active	0		ns		74
t15b	xDACK# Setup to IORC#/IOWC# Active	18		ns		74
t15c	xDACK# Hold from IORC#/IOWC# Inactive	0		ns		74

2

Table 43. AC Specifications (V_{CC} = 5V ± 10%, or (3.3V ± 0.3V) T_{amb} = 0°C to 70°C) (Continued)

Symbol	Parameter	Min	Max	Units	Notes	Figure
PARALLEL PORT						
PD[7:0]						
t16a	PD[7:0] Delay from IOWC# Inactive		60 (90)	ns	ISA,PS/2 wr	87
t16b	PD[7:0] Delay from IOWC# Active		70 (100)	ns	EPP wr	82
t16c	PD[7:0] Float Delay from IOWC# Inactive	50		ns	EPP wr	82
t16f	PD[7:0] Setup to STROBE# Active	450			ISA FIFO	84
t16g	PD[7:0] Hold from STROBE# Inactive	450			ISA FIFO	84
t16h	PD[7:0] Hold from BUSY Inactive	0			ECP fwd	85
t16i	PD[7:0] Setup to ACK# High	0			ECP rev	86
t16j	PD[7:0] Hold from AUTOFD# Low	0			ECP rev	86
STROBE#						
t17a	STROBE# Delay from IOWC# Inactive		60/ 90		ISA, PS/2	87
t17b	STROBE# Delay from IORC#/IOWC#		60/ 90		EPP	82, 83
t17c	STROBE# Active from BUSY Inactive	500			ISA FIFO	84
t17d	STROBE Active Pulse Width	450			ISA FIFO	84
t17e	STROBE# Active from BUSY Inactive	0			ECP fwd	85
t17f	STROBE# Inactive Delay from BUSY Active	0			ECP fwd	85
AUTOFD#						
t18a	AUTOFD# Delay from IOWC# Inactive		60 (90)	ns	ISA,PS/2	87
t18b	AUTOFD# Delay from IORC#/IOWC#		60 (90)	ns	EPP	82, 83
t18c	AUTOFD# Hold from BUSY Inactive	80		ns	ECP fwd	85
t18d	AUTOFD# Low Delay from ACK# Inactive	0		ns	ECP rev	86
t18e	AUTOFD# High Delay from ACK# Active	0		ns	ECP rev	86
INIT#						
t19a	INIT# Delay from IOWC# Inactive		60 (90)	ns	All Modes	87

Table 43. AC Specifications (V_{CC} = 5V ± 10%, or (3.3V ± 0.3V) T_{amb} = 0°C to 70°C) (Continued)

Symbol	Parameter	Min	Max	Units	Notes	Figure
	SELECTIN#					
t20a	SELECTIN# Delay from IOWC# Inactive#		60 (90)	ns	ISA, PS/2	87
t20b	SELECTIN# Delay from IOWC#/IORC# Active		60 (90)		EPP	82
	BUSY					
t21a	BUSY Active Delay from STROBE# Active		500		ISA, PS/2	84
t21b	BUSY Active Delay from STROBE# Active	0				85
t21c	BUSY Inactive Delay from STROBE# Inactive	0			ECP fwd	85
t21d	BUSY Setup to ACK# Active	0			ECP rev	86
t21f	BUSY Hold from AUTOFD# Inactive	0			ECP rev	86
	ACK#					
t22a	ACK# Active Hold from AUTOFD# High	0			ECP rev	86
t22b	ACK# Inactive Hold from AUTOFD# Low	0			ECP rev	86
	PPDIR/GCS#					
t23a	GCS# Delay from SA[10:0]		60 (90)			89
t23b	PPDIR Delay from IOWC# Inactive		60 (90)		ISA, PS/2, ECP	87
t23c	PPDIR Delay from IOWC# Active		60 (90)		EPP	82
	IDE Interface					
	IDECS[1:0]#					
t24a	IDECSx# Delay from SA[10:0]		40 (70)			88
	DEN#					
t25a	DEN# Delay from SA[10:0]		40 (70)			72, 73, 88
t25b	DEN# Delay from xDACK#		40 (70)			74
	HEN#					
t26a	HEN# Delay from IO16#		35 (65)			88

Table 43. AC Specifications (V_{CC} = 5V ± 10%, or (3.3V ± 0.3V) T_{amb} = 0°C to 70°C) (Continued)

Symbol	Parameter	Min	Max	Units	Notes	Figure
	SERIAL PORTS					
	DTRx#, RTSx#, DCDx#					
t27a	DTRx#/RTSx#/DCDx# Active Delay from IOWC#		55 (70)	ns	MCR wr	91
	FLOPPY DISK CONTROLLER					
	RDDATA#					
t28a	Read Data Pulse Width	50		ns		95
t28c	PLL Data Rate		1M	bits/sec		na
t28d	Lockup Time		64	t28c		na
	WRDATA#					
t29a	Data Width	see note	see note		7	77
	HDSEL#					
t30a	WE# to HDSEL# Change	see note	see note		10	78
	STEP#					
t31a	STEP# Active Time	2.5		µs		78
t31b	STEP# Cycle Time	see note	see note	µs	9	78
	DIR#					
t32a	DIR# Setup to STEP# Active	1		µs	8	78
t32b	DIR# Hold from STEP# Inactive	10		µs		78
	WE#					
t33a	WE# Inactive Delay from RSTDRV Inactive Edge		2	µs		75
	INDEX#					
t34a	INDEX# Pulse Width	5	t1e			78

NOTES:
1. The FDC Status Register's status bits which are not latched may be updated during a host read operation.
2. The timing t13b is specified for the FDC interrupt signal in the polling mode only. These timings in case of the result phase of the read and write commands are microcode dependent.
3. This timing is for FDC FIFO threshold = 1. When FIFO threshold is N bytes, the value should be multiplied by N and subtract 1.5 µs. The value shown is for 1 Mbps, scales linearly with data rate.
4. This timing is a function of the internal clock period (t1e) and is given as (⅔) t1e. The values of t1e are shown in Note 3.
5. If DACK# transitions before RD#, then this specification is ignored. If there is no transition on DACK#, then this becomes the DRQ inactive delay.
6. TC width is defined as the time that both TC and DACK# are active. Note that TC and DACK# must overlap at least 50 ns.

NOTES: (Continued)
7. Based on the internal clock period (t1e). For various data rates, the read and write data width minimum values are:

Disk Drive Data Rate	24 MHz
1 Mbps	150 ns
500 Kbps	360 ns
300 Kbps	615 ns
250 Kbps	740 ns

8.This timing is a function of the selected data rate as follows:

Disk Drive Data Rate	Timing
1 Mbps	1.0 μs Min
500 Kbps	2.0 μs Min
300 Kbps	3.3 μs Min
250 Kbps	4.0 μs Min

9. This value can range from 0.5 ms to 8.0 ms and is dependent upon data rate and the Specify Command value.
10. The minimum MFM values for WE# to HDSEL# change for the various data rates are:

Disk Drive Data Rate	Min MFM Value
1 Mbps	0.5 ms + [8 × GPL]
500 Kbps	1.0 ms + [16 × GPL]
300 Kbps	1.6 ms + [26.66 × GPL]
250 Kbps	2.0 ms + [32 × GPL]

GPL is the size of gap 3 defined in the sixth byte of a Write Command.

11. Based on internal clock period.
12. Jitter tolerance is defined as:
    (Maximum bit shift from nominal position ÷ ¼ period of nominal data rate) × 100 percent is a measure of the allowable bit jitter that may be present and still be correctly detected. The data separator jitter tolerance is measured under dynamic conditions that jitters the bit stream according to a reverse precompensation algorithm.
13. The minimum reset active period for a software reset is dependent on the data rate, after the FDC module has been properly reset using the t10a spec. The minimum software reset period then becomes:

Disk Drive Data Rate	Minimum Software Reset Active Period
	24 MHz
1 Mbps	125 ns
500 Kbps	250 ns
300 Kbps	420 ns
250 Kbps	500 ns

11.4.1 CLOCK TIMINGS

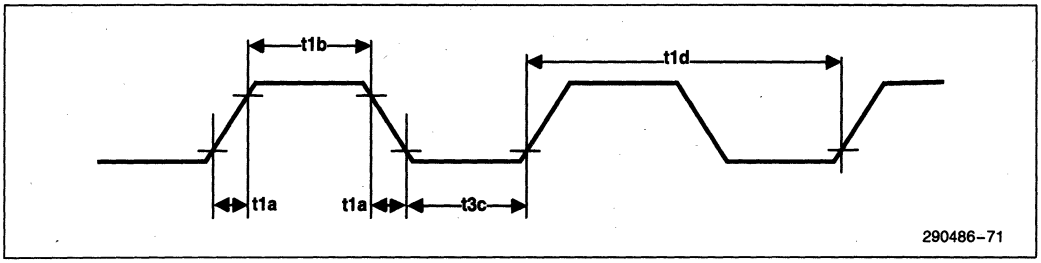


Figure 71. Clock Timing

11.4.2 HOST TIMINGS

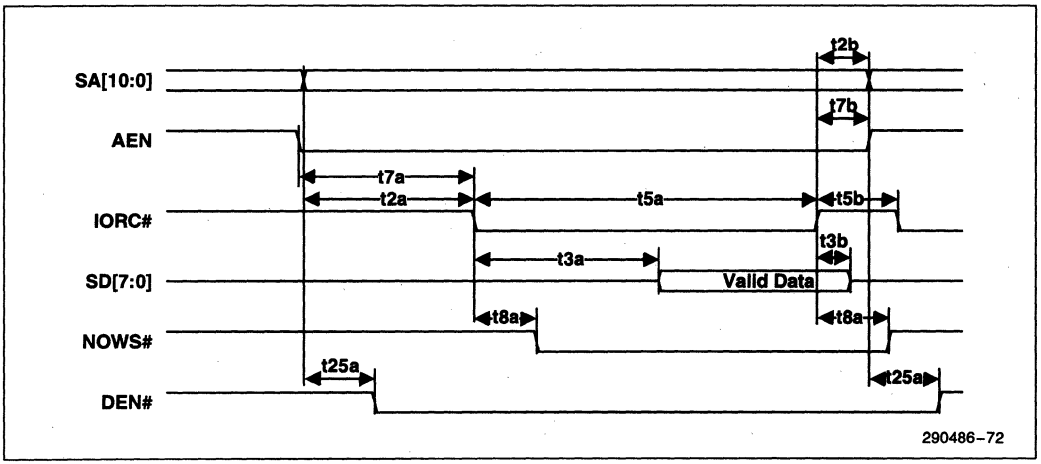


Figure 72. Host Read

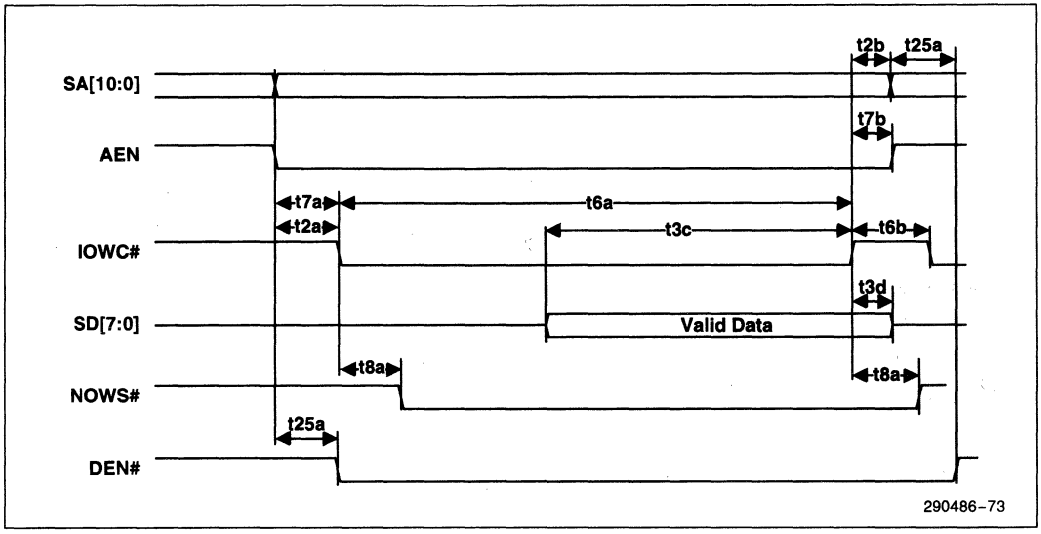


Figure 73. Host Write

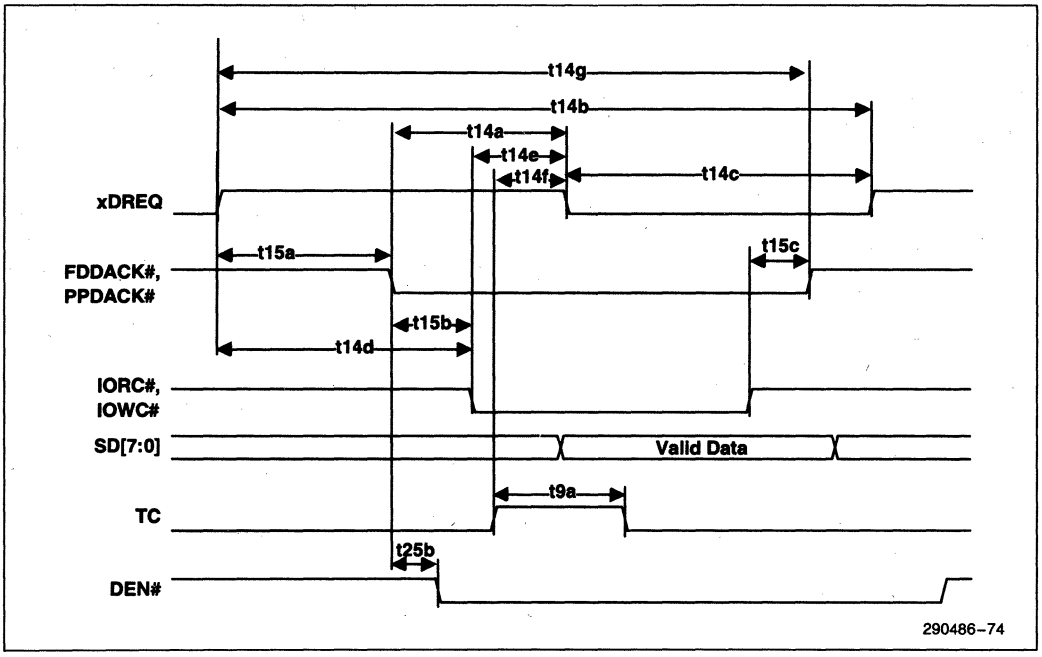
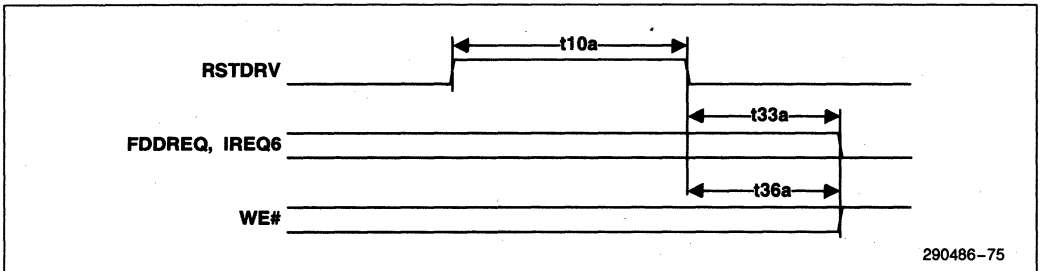


Figure 74. DMA Timing



NOTE:
FDDREQ, IRQ6 depicts the FDC enabled condition under hardware configuration. Otherwise, these signals tri-state with the same timing as IRQ[7,5,4,3].

Figure 75. Reset Timing

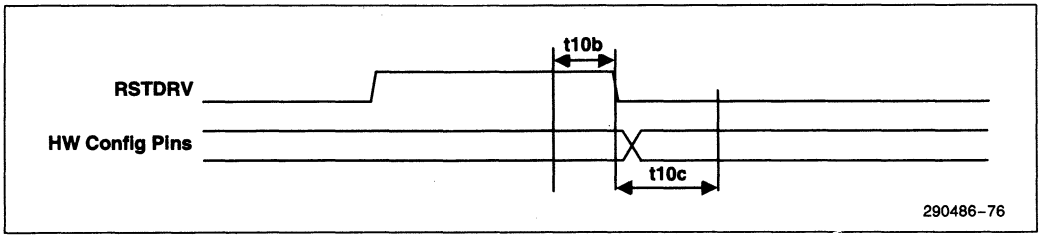


Figure 76. Reset Timing (Hardware Extended Configuration Mode)

11.4.3 FDC TIMINGS

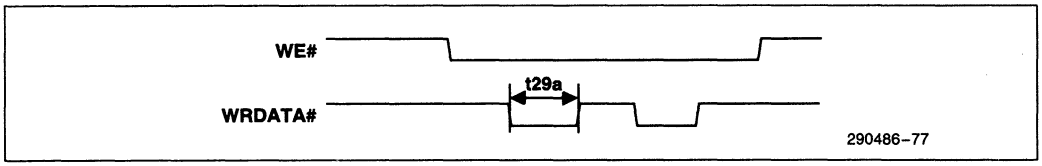
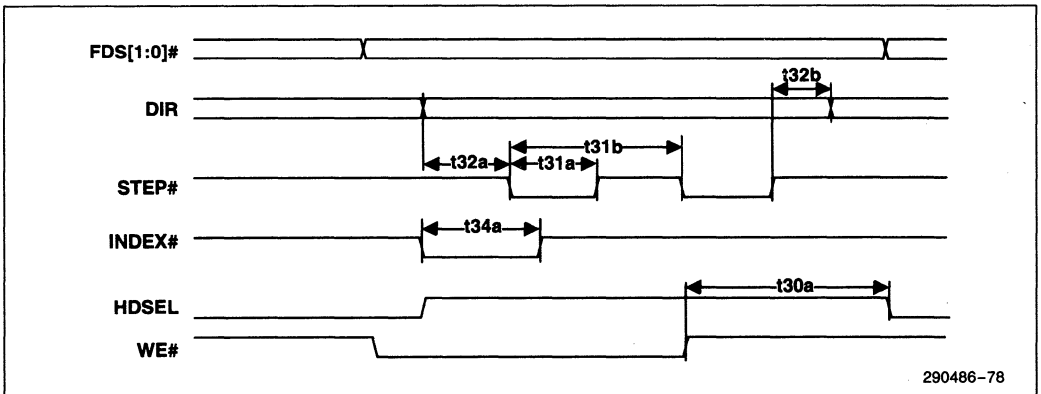


Figure 77. Write Data Timing



NOTE:
For overlapped seeks, only one step pulse per drive selection is issued. Non-overlapped seeks will issue all programmed step pulses.

Figure 78. FDC Drive Control/Timing

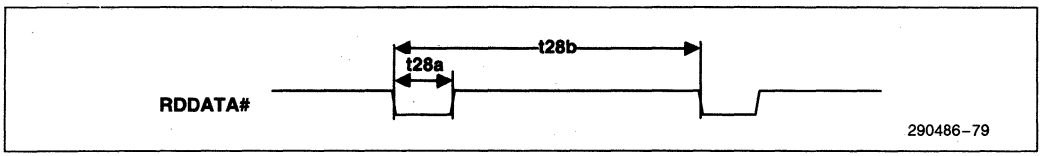


Figure 79. FDC Internal PLL Timing

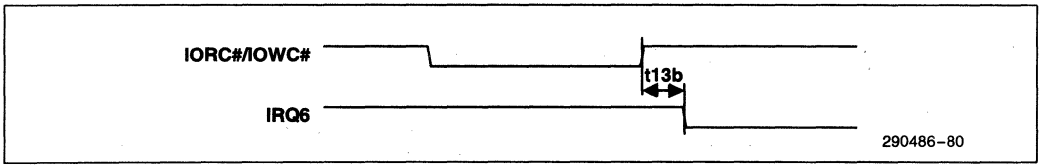


Figure 80. Floppy Disk Controller Interrupts

11.4.4 PARALLEL PORT TIMINGS

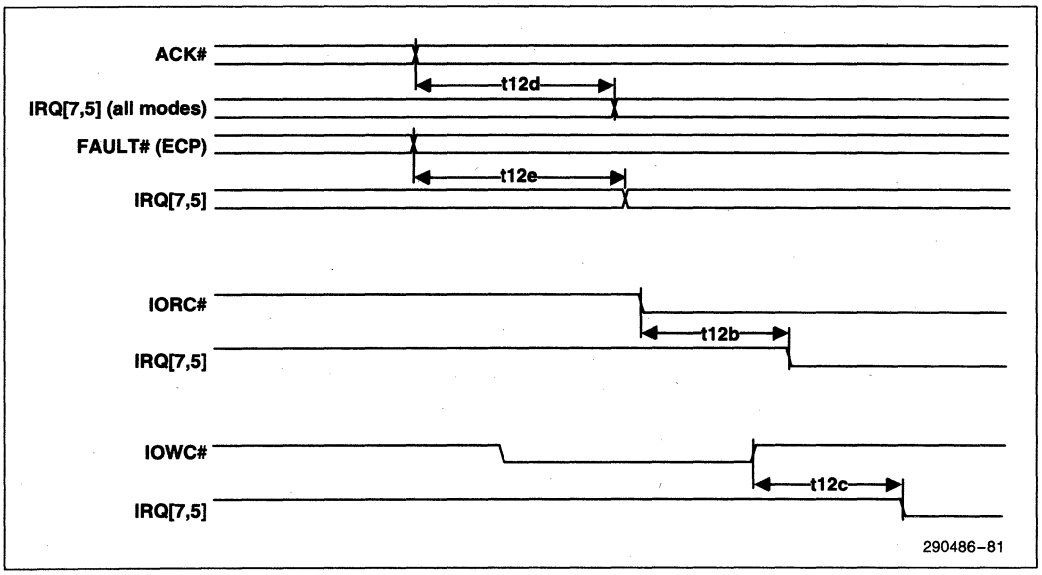


Figure 81. Parallel Port Interrupt Timing

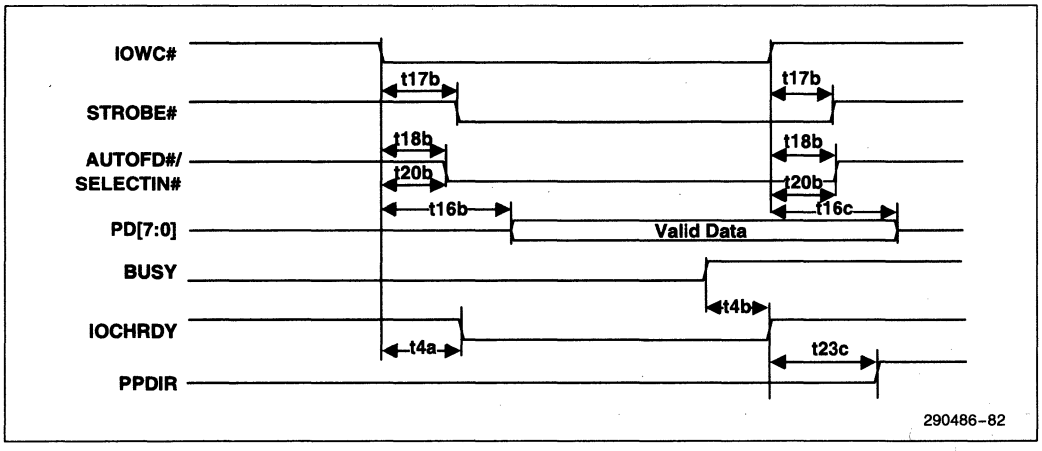


Figure 82. EPP Write Timing

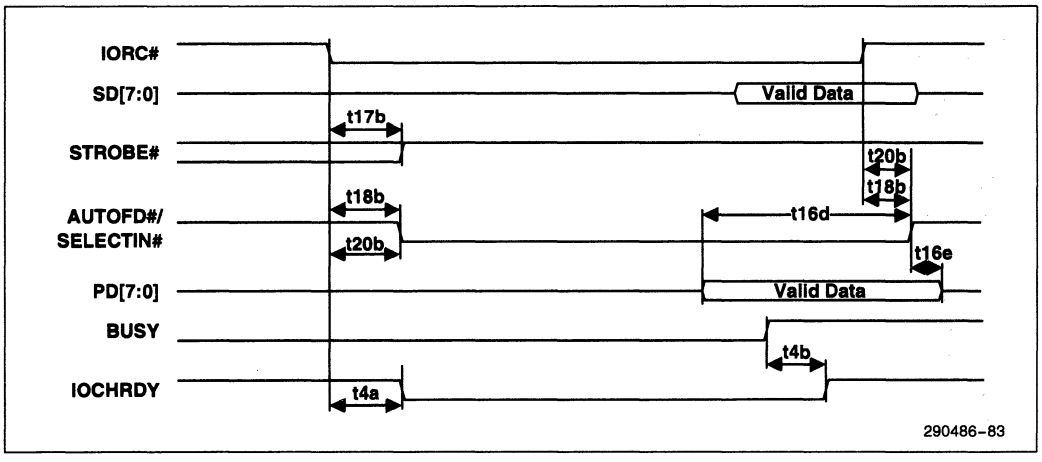


Figure 83. EPP Read Timing

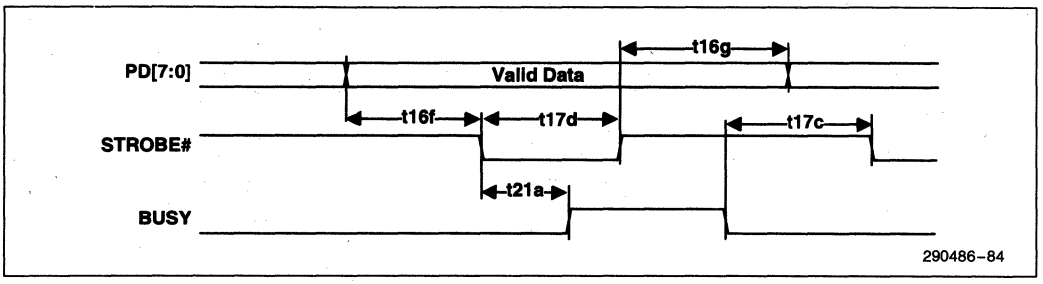


Figure 84. ISA-Compatible FIFO Timing

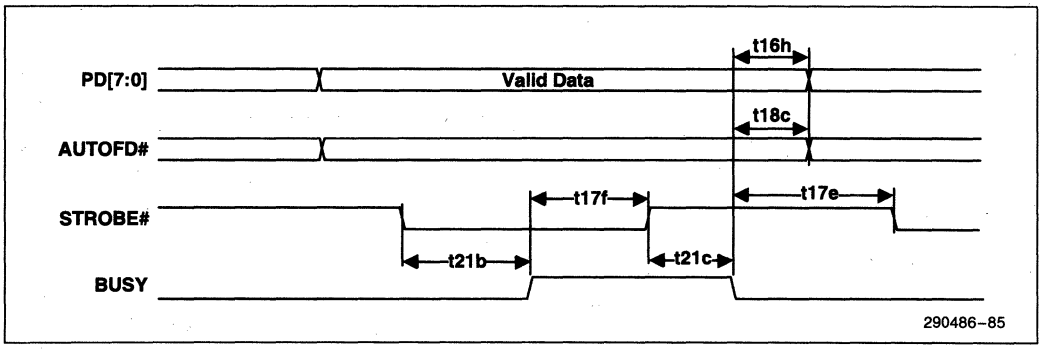


Figure 85. ECP Write Timing (Forward Direction)

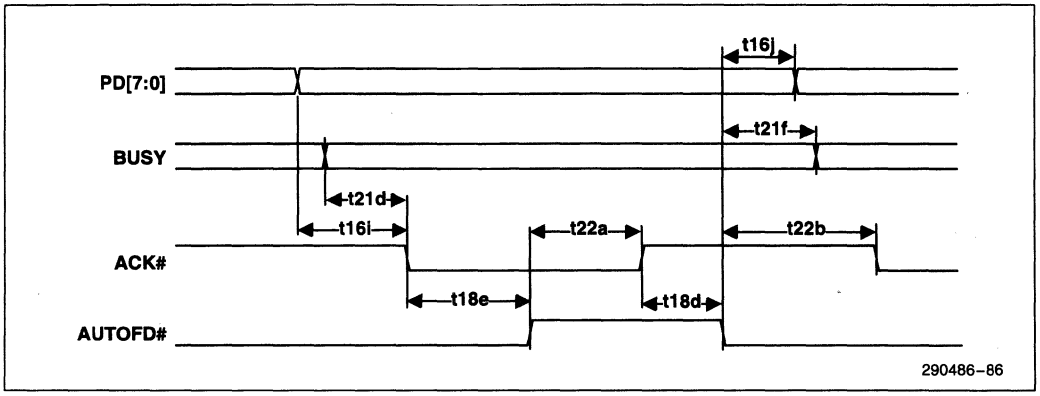


Figure 86. ECP Read Timing (Reverse Direction)

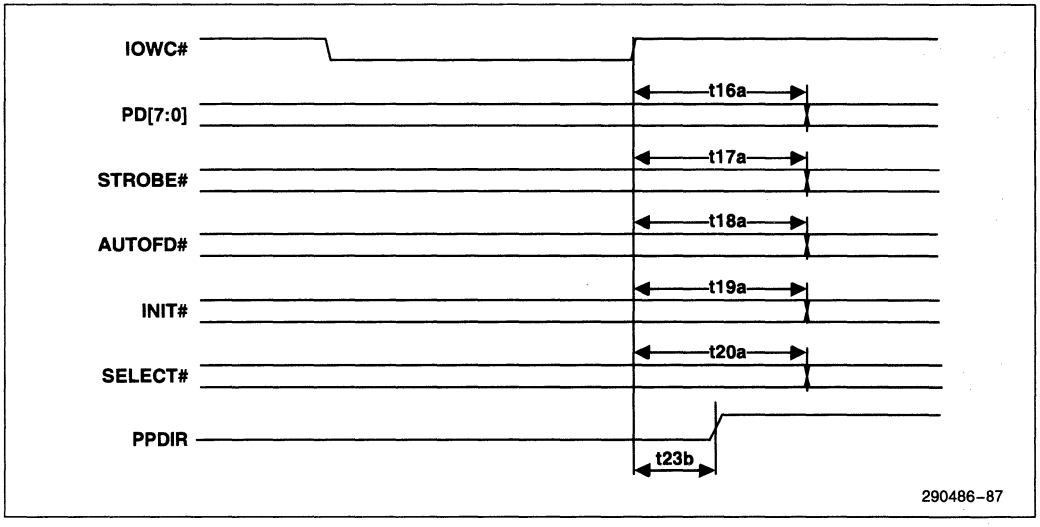


Figure 87. ISA-Compatible Write Timing

11.4.5 IDE TIMINGS

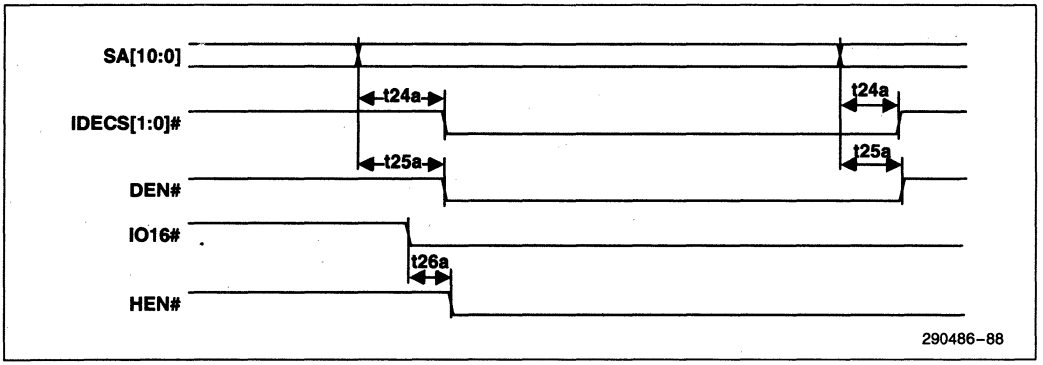


Figure 88. IDE Timing

11.4.6 GAME PORT TIMINGS

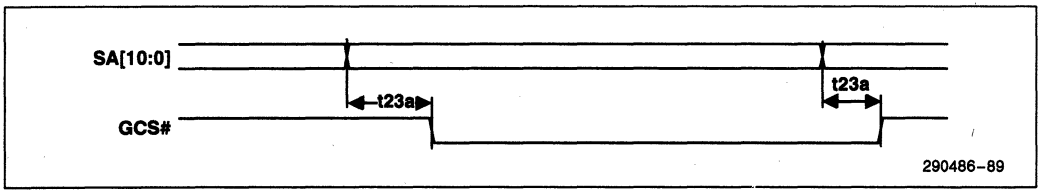


Figure 89. Game Port Timing

11.4.7 SERIAL PORT TIMINGS

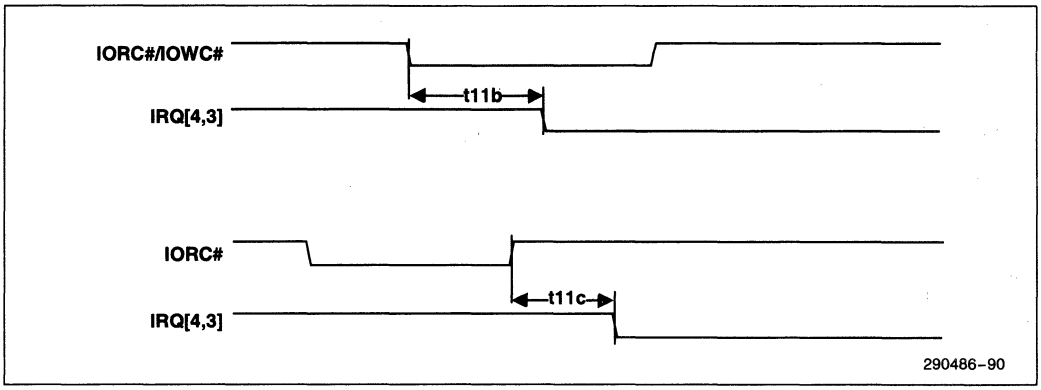


Figure 90. Serial Port Interrupt Timing

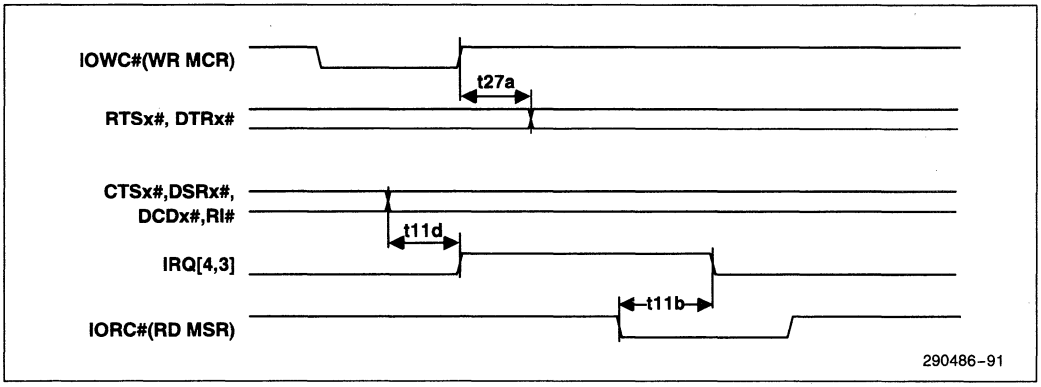


Figure 91. Modem Control Timing

12.0 PINOUT AND PACKAGE INFORMATION

12.1 Pin Assignment

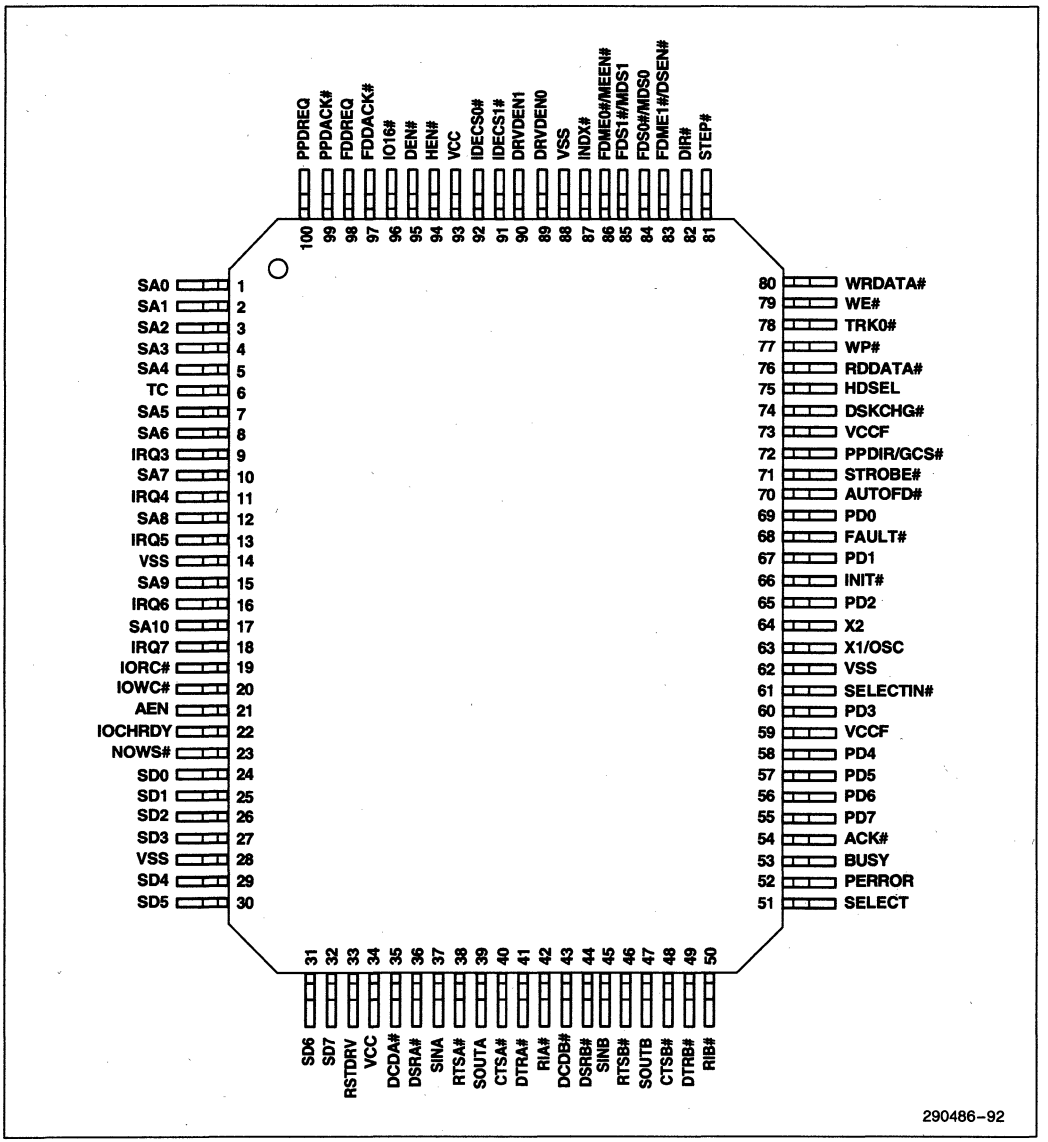


Figure 92. 82091AA Pin Diagram

Table 44. Alphabetical 82091AA Pin Assignment

Signal Name	Pin #	Type
ACK#	54	I
AEN	21	I
AUTOFD#	70	O
BUSY	53	I
CTSA#	40	I
CTSB#	48	I
DCDA#	35	O
DCDB#	43	O
DEN#	95	I/O
DIR#	82	O
DRVDEN0	89	O
DRVDEN1	90	O
DSKCHG#	74	I
DSRA#	36	I
DSRB#	44	I
DTRA#	41	I/O
DTRB#	49	I/O
FAULT#	68	I
FDDACK#	97	I
FDDREQ	98	O
FDME0#/MEEN#	86	O
FDME1#/DSEN#	83	O
FDS0#/MDS0	84	O
FDS1#/MDS1	85	O
HDSEL	75	O
HEN#	94	I/O
IDECS0#	92	I/O
IDECS1#	91	I/O
INDX#	87	I
INIT#	66	O
IO16#	96	I
IOCHRDY	22	O
IORC#	19	I
IOWC#	20	I

Signal Name	Pin #	Type
IRQ3	9	O
IRQ4	11	O
IRQ5	13	O
IRQ6	16	O
IRQ7	18	O
NOWS#	23	O
PD0	69	I/O
PD1	67	I/O
PD2	65	I/O
PD3	60	I/O
PD4	58	I/O
PD5	57	I/O
PD6	56	I/O
PD7	55	I/O
PERROR	52	I
PPDACK#	99	I
PPDREQ	100	O
PPDIR/GCS#	72	I/O
RDDATA#	76	I
RIA#	42	I
RIB#	50	I
RSTDRV	33	I
RTSA#	38	I/O
RTSB#	46	I/O
SA0	1	I
SA1	2	I
SA2	3	I
SA3	4	I
SA4	5	I
SA5	7	I
SA6	8	I
SA7	10	I
SA8	12	I
SA9	15	I

Table 44. Alphabetical 82091AA Pin Assignment (Continued)

Signal Name	Pin #	Type
SA10	17	I
SD0	24	I/O
SD1	25	I/O
SD2	26	I/O
SD3	27	I/O
SD4	29	I/O
SD5	30	I/O
SD6	31	I/O
SD7	32	I/O
SINA	37	I
SINB	45	I
SELECT	51	I
SELECTIN#	61	O
SOUTA	39	I/O
SOUTB	47	I/O
STEP#	81	O

Signal Name	Pin #	Type
STROBE#	71	O
TC	6	I
TRK0#	78	I
V_{CC}	34	V
V_{CC}	93	V
V_{CCF}	59	V
V_{CCF}	73	V
V_{SS}	14	V
V_{SS}	28	V
V_{SS}	62	V
V_{SS}	88	V
WE#	79	O
WP#	77	I
WRDATA#	80	O
X1/OSC	63	I
X2	64	I

Table 45. Numerical 82091AA Pin Assignment

Pin #	Signal Name	Type
1	SA0	I
2	SA1	I
3	SA2	I
4	SA3	I
5	SA4	I
6	TC	I
7	SA5	I
8	SA6	I
9	IRQ3	O
10	SA7	I
11	IRQ4	O
12	SA8	I
13	IRQ5	O
14	V_{SS}	V
15	SA9	I

Pin #	Signal Name	Type
16	IRQ6	O
17	SA10	I
18	IRQ7	O
19	IORC#	I
20	IOWC#	I
21	AEN	I
22	IOCHRDY	O
23	NOWS#	O
24	SD0	I/O
25	SD1	I/O
26	SD2	I/O
27	SD3	I/O
28	V_{SS}	V
29	SD4	I/O
30	SD5	I/O

Table 45. Numerical 82091AA Pin Assignment (Continued)

Pin #	Signal Name	Type
31	SD6	I/O
32	SD7	I/O
33	RSTDRV	I
34	V_{CC}	V
35	DCDA#	O
36	DSRA#	I
37	SINA	I
38	RTSA#	I/O
39	SOUTA	I/O
40	CTSA#	I
41	DTRA#	I/O
42	RIA#	I
43	DCDB#	O
44	DSRB#	I
45	SINB	I
46	RTSB#	I/O
47	SOUTB	I/O
48	CTSB#	I
49	DTRB#	I/O
50	RIB#	I
51	SELECT	I
52	PERROR	I
53	BUSY	I
54	ACK#	I
55	PD7	I/O
56	PD6	I/O
57	PD5	I/O
58	PD4	I/O
59	V_{CCF}	V
60	PD3	I/O
61	SELECTIN#	O
62	V_{SS}	V
63	X1/OSC	I
64	X2	I
65	PD2	I/O

Pin #	Signal Name	Type
66	INIT#	O
67	PD1	I/O
68	FAULT#	I
69	PD0	I/O
70	AUTOFD#	O
71	STROBE#	O
72	PPDIR/GCS#	I/O
73	V_{CCF}	V
74	DSKCHG#	I
75	HDSEL	O
76	RDDATA#	I
77	WP#	I
78	TRK0#	I
79	WE#	O
80	WRDATA#	O
81	STEP#	O
82	DIR#	O
83	FDME1#/DSEN#	O
84	FDS0#/MDS0	O
85	FDS1#/MDS1	O
86	FDME0#/MEEN#	O
87	INDX#	I
88	V_{SS}	V
89	DRVDEN0	O
90	DRVDEN1	O
91	IDECS1#	I/O
92	IDECS0#	I/O
93	V_{CC}	I/O
94	HEN#	V
95	DEN#	I/O
96	IO16#	I
97	FDDACK#	I
98	FDDREQ	O
99	PPDACK#	I
100	PPDREQ	O

12.2 Package Characteristics

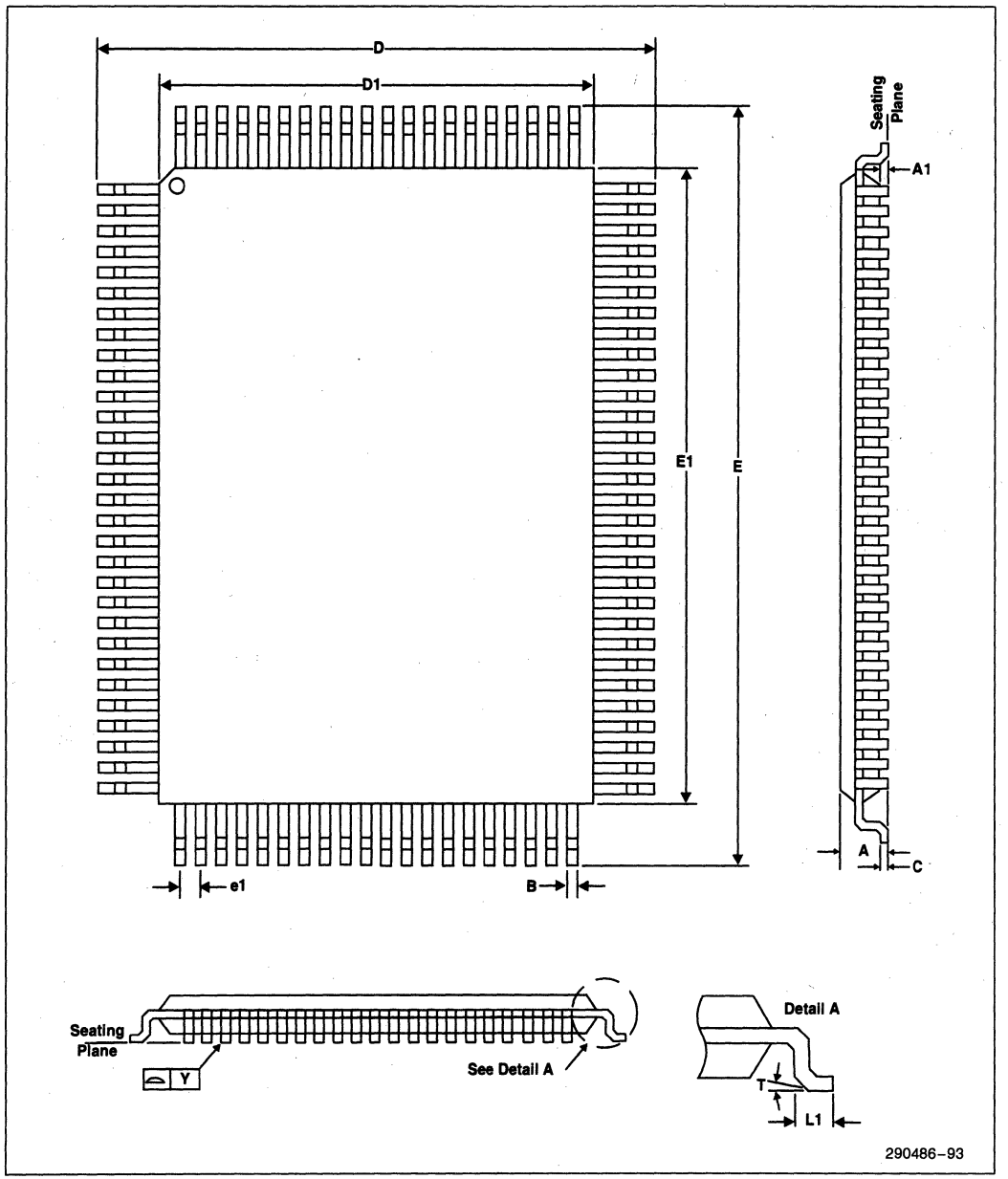


Figure 93. 100-Pin Quad Flat Pack (QFP) Dimensions

Quad Flat Pack Package				
Symbol	Millimeters			
	Minimum	Nominal	Maximum	Notes
A			3.15	
A1	0.0			
B	0.20	0.30	0.40	
C	0.10	0.15	0.20	
D	17.5	17.9	18.3	
D1		14.0		
E	23.5	23.9	24.3	
E1		20.0		
e1	0.53	0.65	0.77	
L1	0.60	0.80	1.00	
N		100		Rectangle
T	0.00		10.0	
Y			0.10	
ISSUE	JEDEC			

13.0 DATA SEPARATOR CHARACTERISTICS FOR FLOPPY DISK MODE

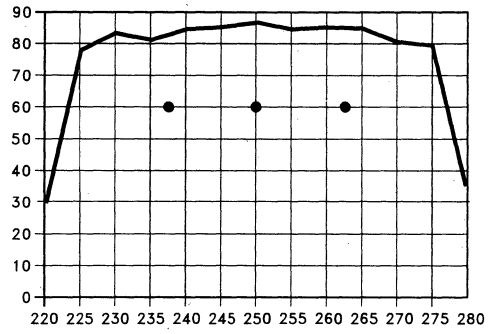


Figure 94. Typical Jitter Tolerance vs Data Rate (Capture Range 250 Kbps)

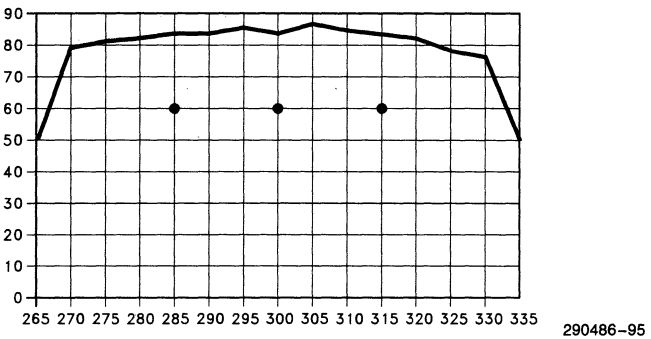


Figure 95. Typical Jitter Tolerance vs Data Rate (Capture Range 300 Kbps)

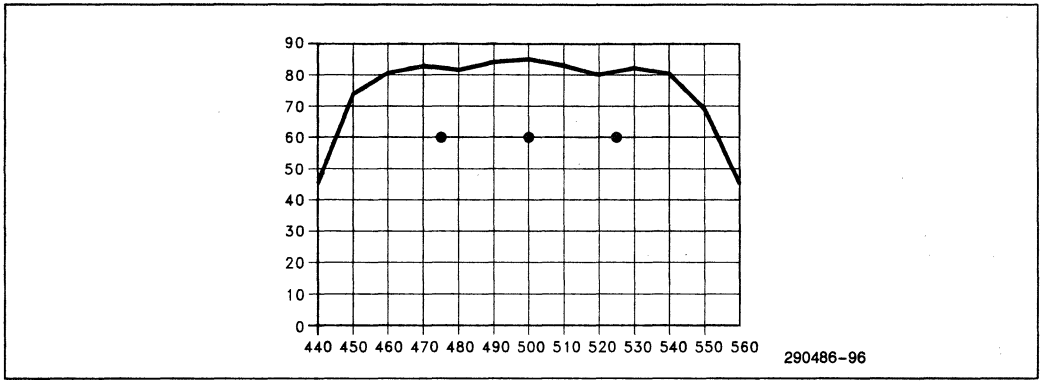


Figure 96. Typical Jitter Tolerance vs Data Rate (Capture Range 500 Kbps)

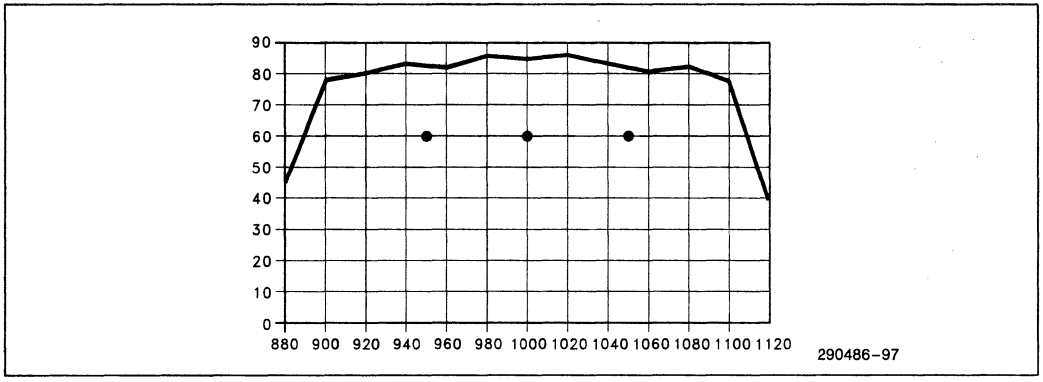


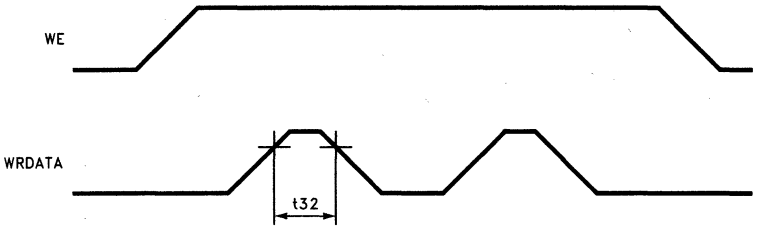
Figure 97. Typical Jitter Tolerance vs Data Range (Capture Range 1 Mbps)

Jitter Tolerance measured in percent. Capture range expressed as a percent of data rate, i.e., ±3% percent.

• = Test Points: 250 Kbps, 300 Kbps, 500 Kbps and 1 Mbps are center, ±5 percent @ 60 percent jitter.

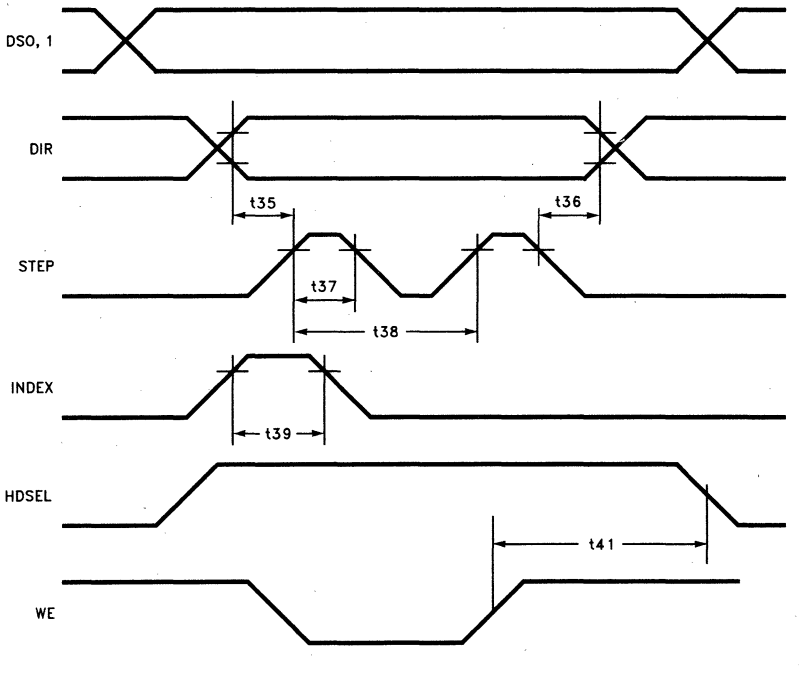
Test points are tested at temparture and V_{CC} limits. Refer to the datasheet. Typical conditions are: room temperature, nominal V_{CC}.

13.1 Write Data Timing



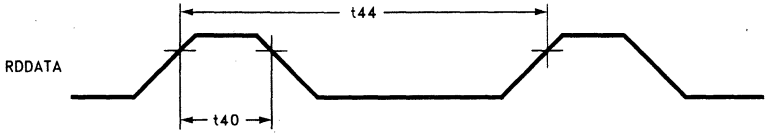
NOTE:
Invert high.

13.2 Drive Control



NOTE:
For overlapped seeks, only one step pulse per drive selection is issued. Non-overlapped seeks will issue all programmed step pulses. Invert high.

13.3 Internal PLL



290486-A0

NOTE:
Invert high.

APPENDIX A
FDC FOUR DRIVE SUPPORT

Section 8.0 of this document completely describes the FDC when the module is configured for two drive support. In addition, the FDC commands in Section 8.0 provide four drive support information. This appendix provides additional information concerning four drive support. The signal pins that are affected by four drive support are described in Section A.1. Note that the FDC signals not discussed in this appendix operate the same for both two and four drive systems. The following registers are described in this appendix; Digital Output Register (DOR), Enhanced Tape Drive Register (TDR), and the Main Status Register (MSR). Some bits in these registers operate differently in a four drive configuration than a two drive configuration.

NOTES:

- The descriptions in this appendix assume that four floppy drive support has been selected by setting FDDQTY to 1 in the AIPCFG1 Register.
- Only drive 0 or drive 1 can be selected as the boot drive.

A.1 Floppy Disk Controller Interface Signals

These signal descriptions are for a four drive system (FDDQTY = 1 in the AIPCFG1 Register). See Section 2.0 for two drive system signal descriptions.

Signal Name	Type	Description
FDME1#/DSEN#(1)	O	**FLOPPY DRIVE MOTOR ENABLE 1, or DRIVE SELECT ENABLE:** In a four drive system, this signal functions as a drive select enable (DSEN#). When DSEN# is asserted, MDS1 and MDS0 reflect the selection of the drive.
FDS1#/MDS1(1)	O	**FLOPPY DRIVE SELECT1, or MOTOR DRIVE SELECT 1:** In a four drive system, this signal functions as a motor drive select (MDS1). MDS1, together with MDS0, indicate which of the four drives is selected, as shown in note 1.
FDME0#/MEEN#(1)	O	**FLOPPY DRIVE MOTOR ENABLE 0 or MOTOR ENABLE ENABLE:** In a four drive system, this signal functions as a motor enable enable (MEEN#). MEEN# is asserted to enable the external decoding of MDS1 and MDS0 for the appropriate motor enable (see note 1).
FDS0#/MDS0(1)	O	**FLOPPY DRIVE SELECT 0 or MOTOR DRIVE SELECT 0:** In a four drive system, this signal functions as motor drive select (MDS0). MDS0, together with MDS1, indicate which of the four drives is selected as shown in note 1.

NOTE:

1. These signal pins are used to control an external decoder for four floppy disk drives as shown below. Refer to the DOR Register Description in Section A.2 for details.

MDS1	MDS0	DSEN# = 0	MEEN# = 0
0	0	Drive 0	ME0
0	1	Drive 1	ME1
1	0	Drive 2	ME2
1	1	Drive 3	ME3

A.2 DOR—Digital Output Register

I/O Address: Base + 2h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

The Digital Output Register enables/disables the floppy disk drive motors, selects the disk drives, enables/disables DMA, and provides a FDC module reset. The DOR reset bit and the Motor Enable bits have to be inactive when the 82091AA's FDC is in powerdown. The DMAGATE# and Drive Select bits are unchanged. During powerdown, writing to the DOR does not wake up the 82091AA's FDC, except for activating any of the motor enable bits. Setting the motor enable bits to 1 will wake up the module. The four internal drive select and four internal motor enable signals are encoded to a total of four output pins as described in Table 47. Figure 99 shows an example of how these four output pins can be decoded to provide four drive select and four motor enable signals. Note that only drive 0 or drive 1 can be used as the boot drive when four disk drives are enabled.

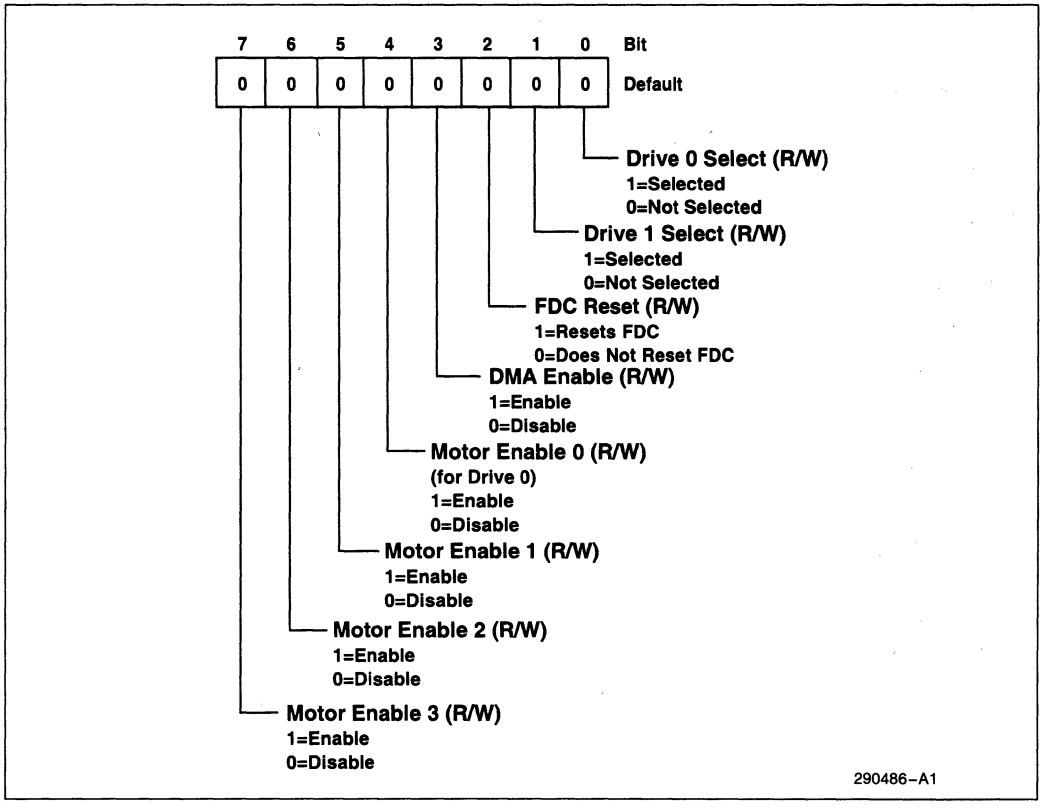


Figure 98. Digital Output Register

Bit	Description
7	**Motor Enable 3 (ME3):** This bit controls a motor drive enable output signal and provides the signal output for the floppy drive 3 motor (via external decoding) as shown in Table 46.
6	**Motor Enable 2 (ME2):** This bit controls a motor drive enable output signal and provides the signal output for the floppy drive 2 motor (via external decoding) as shown in Table 46.
5	**Motor Enable 1 (ME1):** This bit controls a motor drive enable signal and provides the signal output for the floppy drive 1 motor (via external decoding) as shown in Table 46.
4	**Motor Enable 0 (ME0):** This bit controls a motor drive enable signal and provides the signal output for the floppy drive 0 motor (via external decoding) as shown in Table 46.
3	**DMA Gate (DMAGATE):** This bit enables/disables DMA for the FDC. When DMAGATE = 1, DMA for the FDC is enabled. In this mode FDDREQ, TC, IRQ6, and FDDACK# are enabled. When DMAGATE = 0, DMA for the FDC is disabled. In this mode, the IRQ6 and DRQ outputs are tri-stated and the DACK# and TC inputs are disabled to the FDC. Note that the TC input is only disabled to the FDC module. Other functional units in the 82091AA (e.g., parallel port or IDE interface) can still use the TC input signal for DMA activities.
2	**FDC Reset (DORRST):** DORRST is a software reset for the FDC module. When DORRST is set to 0, the basic core of the 82091AA's FDC and the FIFO circuits are cleared conditioned by the LOCK bit in the Configure Command. This bit is set to 0 by software or a hard reset (RSTDRV asserted). The FDC remains in a reset state until software sets this bit to 1. This bit does not affect the DSR, CCR and other bits of the DOR. DORRST must be held active for at least 0.5 μs at 250 Kbps. This is less than a typical ISA I/O cycle time. Thus, in most systems consecutive writes to this register to toggle this bit allows sufficient time to reset the FDC.
1:0	**Drive Select (DS[1:0]):** This field provides the output signals to select a particular floppy drive (via external decoding) as shown in Table 47. Note that the drive motor can be enabled separately without selecting the drive. This permits the motor to come up to speed before selecting the drive. Note also that only one drive can be selected at a time. However, the drive should not be selected without enabling the appropriate drive motor via bits[7:4] of this register.

Table 46. Output Pin Status for Four Disk Drives

	FDC DOR Register Bits						Signal Pins			
Description	**ME3**	**ME2**	**ME1**	**ME0**	**DS1**	**DS0**	**MDS1#**	**MDS0#**	**DSEN#**	**MEEN#**
ME0 and DS0 enable	X	X	X	1	0	0	0	0	0	0
ME1 and DS1 enable	X	X	1	X	0	1	0	1	0	0
ME2 and DS2 enable	X	1	X	X	1	0	1	0	0	0
ME3 and DS3 enable	1	X	X	X	1	1	1	1	0	0
ME0 enable only	X	X	X	1	DS[1:0]≠00		0	0	1	0
ME1 enable only	X	X	1	0	DS[1:0]≠01		0	1	1	0
ME2 enable only	X	1	0	0	DS[1:0]≠10		1	0	1	0
ME3 enable only	1	0	0	0	DS[1:0]≠11		1	1	1	0
No ME or DS enable	0	0	0	0	X	X	1	1	1	1

NOTE:
To enable a particular drive motor and select the drive, the value for DS[1:0] must match the appropriate motor enable bit selected as indicated in the first four rows of the table. For example, to enable the drive 0 motor and select the drive, ME0 is set to 1 and DS[1:0] must be set to 00. To enable the drive motor and keep the drive de-selected the value for DS[1:0] must not match the particular motor enable as shown in the first four rows. For example, to enable the motor for drive 0 while the drive remains de-selected, ME0 is set to 1 and DS[1:0] is set to 01, 10, or 11.

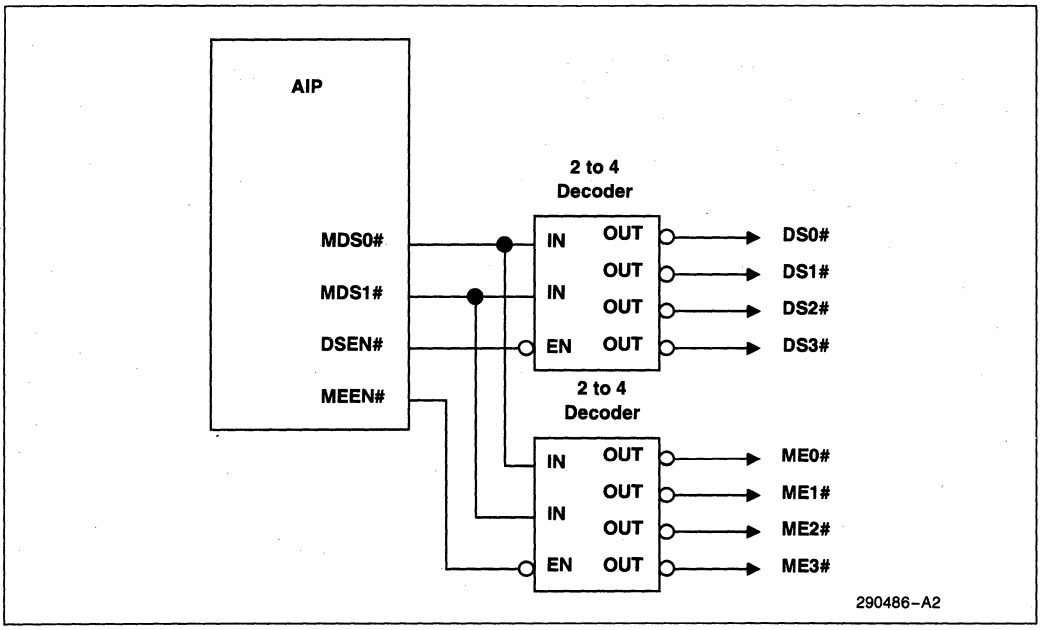


Figure 99. Example External Decoder (Four Drive System)

A.3 TDR—Enhanced Tape Drive Register

I/O Address: Base +3h
Default Value: 00h
Attribute: Read/Write
Size: 8 bits

This register allows the user to assign tape support to a particular drive during initialization. Any future references to that drive number automatically invokes tape support. A hardware reset sets all bits in this register to 0 making drive 0 not available for tape support. A software reset via bit 2 of the DOR does not affect this register. Drive 0 is reserved for the floppy boot drive. Bits[7:2] are only available when EREG EN=1; otherwise the bits are tri-stated.

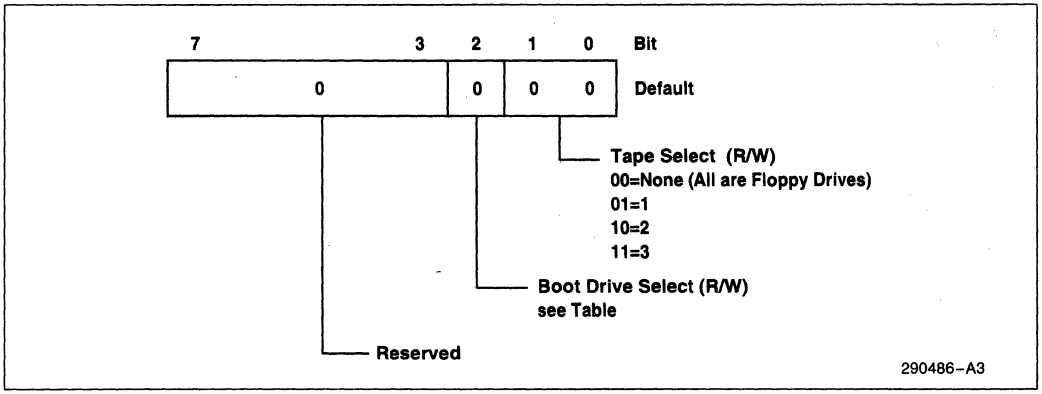


Figure 100. Enhanced Tape Drive Register

Bit	Description
7:3	**Reserved:**
2	**Boot Drive Select (BOOTSEL):** The BOOTSEL bit is used to remap the drive selects and motor enables. The functionality is shown below: **BOOTSEL** **Mapping** 0 DS0 → FDS0, ME0 → FDME0 (default) DS1 → DS1, ME1 → FDME1 1 DS0 → DS1, ME0 → FDME1 DS1 → FDS0, ME1 → FDME0 Only drive 0 or drive 1 can be selected as the boot drive.
1:0	**Tape Select (TAPESEL[1:0]):** These two bits are used by software to assign a logical drive number to be a tape drive. Other than adjusting precompensation delays for tape support, these two bits do not affect the FDC hardware. They can be written and read by software as an indication of the tape drive assignment. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive. The tape drive assignments are as follows: **Bits[1:0]** **Drive Selected** 0 0 None (all are floppy disk drives) 0 1 1 1 0 2 1 1 3

A.4 MSR—Main Status Register

I/O Address: Base + 4h
Default Value: 00h
Attribute: Read Only
Size: 8 bits

This read only register provides FDC status information. This information is used by software to control the flow of data to and from the FIFO (accessed via the FDCFIFO Register). The MSR indicates when the FDC is ready to send or receive data through the FIFO. During non-DMA transfers, this register should be read before each byte is transferred to or from the FIFO.

After a hard or soft reset or recovery from a powerdown state, the MSR is available to be read by the host. The register value is 00h until the oscillator circuit has stabilized and the internal registers have been initialized. When the FDC is ready to receive a new command, MSR[7:0] = 80h. The worst case time allowed for the MSR to report 80h (i.e., RQM is set to 1) is 2.5 μs after a hard or soft reset.

Main Status Register is used for controlling command input and result output for all commands. Some example values of the MSR are:

- MSR = 80H; The controller is ready to receive a command.
- MSR = 90H; Executing a command or waiting for the host to read status bytes (assume DMA mode).
- MSR = D0H; Waiting for the host to write status bytes.

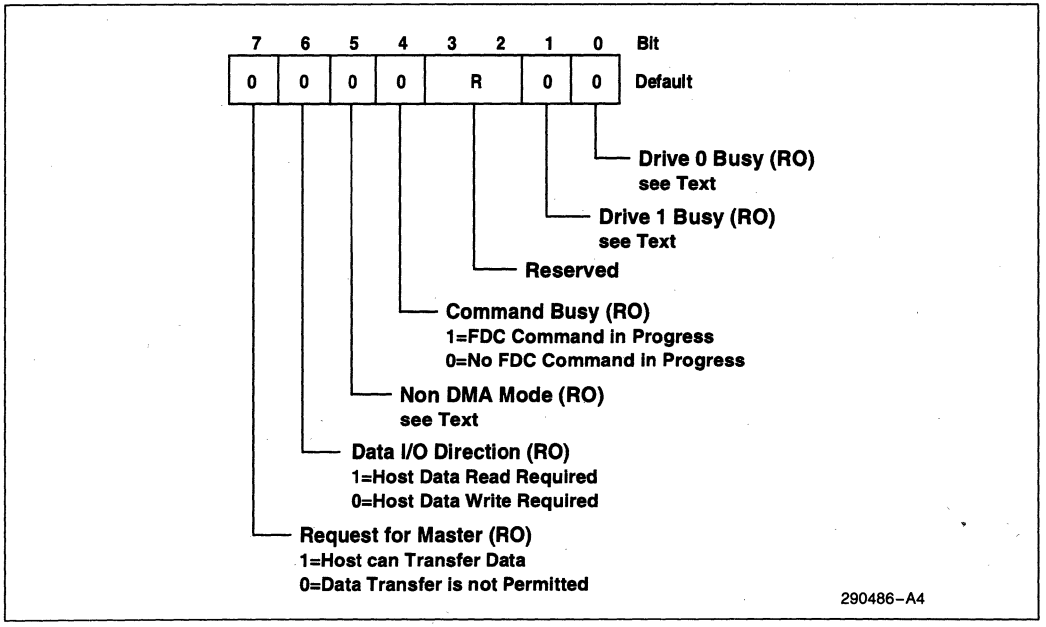


Figure 101. Main Status Register

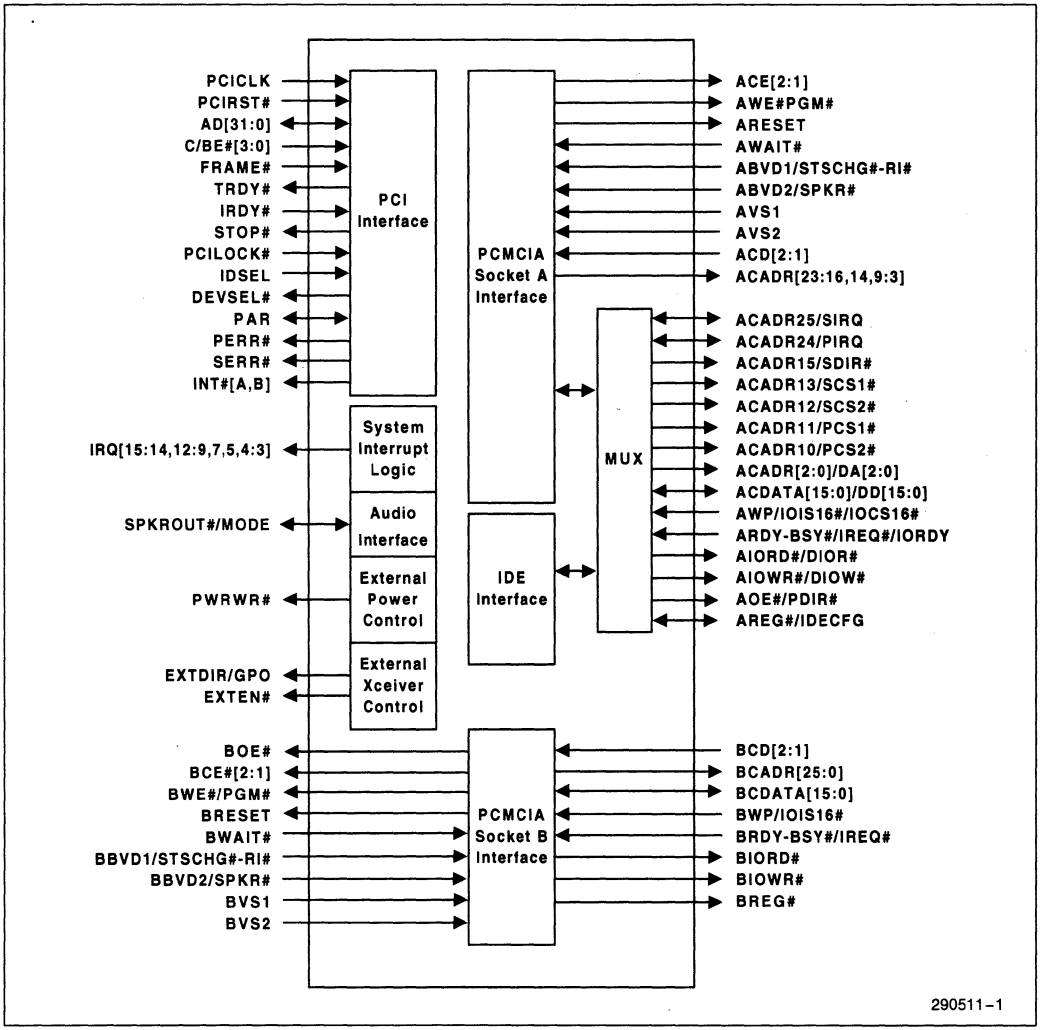
Bit	Description
7	**Request For Master (RQM):** When RQM = 1, the FDC is ready to send/receive data through the FIFO (FDCFIFO Register). The FDC sets this bit to 0 after a byte transfer and then sets the bit to 1 when it is ready for the next byte. During non-DMA execution phase, RQM indicates the status of IRQ6.
6	**Direction I/O (DIO):** When RQM = 1, DIO indicates the direction of a data transfer. When DIO = 1, the FDC is requesting a read of the FDCFIFO. When DIO = 0, the FDC is requesting a write to the FDCFIFO.
5	**NON-DMA (NONDMA):** Non-DMA mode is selected via the SPECIFY Command. In this mode, the FDC sets this bit to a 1 during the execution phase of a command. This bit is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.
4	**Command Busy (CMDBUSY):** CMDBUSY indicates when a command is in progress. When the first byte of the command phase is written, the FDC sets this bit to 1. CMDBUSY is set to 0 after the last byte of the result phase is read. If there is no result phase (e.g., SEEK or RECALIBRATE Commands), CMDBUSY is set to 0 after the last command byte is written.
3	**Drive 3 Busy (DRV1BUSY):** The FDC module sets this bit to 1 after the last byte of the command phase of a SEEK or RECALIBRATE Command is issued for drive 3. This bit is set to 0 after the host reads the first byte in the result phase of the SENSE INTERRUPT Command for this drive.
2	**Drive 2 Busy (DRV1BUSY):** The FDC module sets this bit to 1 after the last byte of the command phase of a SEEK or RECALIBRATE Command is issued for drive 2. This bit is set to 0 after the host reads the first byte in the result phase of the SENSE INTERRUPT Command for this drive.
1	**Drive 1 Busy (DRV1BUSY):** The FDC module sets this bit to 1 after the last byte of the command phase of a SEEK or RECALIBRATE Command is issued for drive 1. This bit is set to 0 after the host reads the first byte in the result phase of the SENSE INTERRUPT Command for this drive.
0	**Drive 0 Busy (DRV0BUSY):** The FDC module sets this bit to 1 after the last byte of the command phase of a SEEK or RECALIBRATE Command is issued for drive 0. This bit is set to 0 after the host reads the first byte in the result phase of the SENSE INTERRUPT Command for this drive.

82092AA
PCI TO PCMCIA/ENHANCED-IDE CONTROLLER

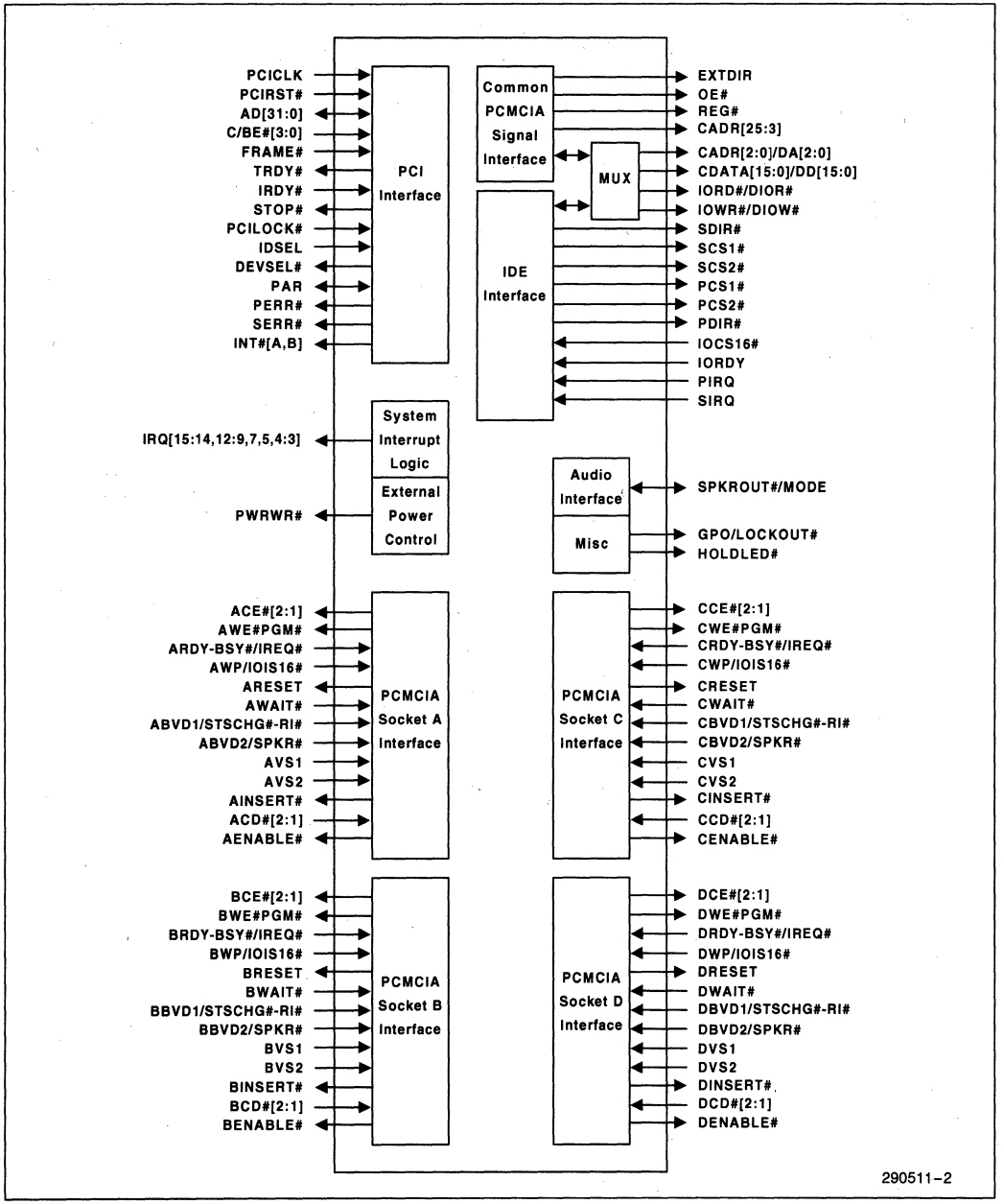
- **Provides the Ultimate Plug and Play Solution for High Performance PCI Desktop Systems**
  - **— Supports Combinations of PCMCIA and Enhanced Local Bus IDE Interfaces**
  - **— Contains a 32-bit PCI Local Bus Slave Interface Running at 25/33 MHz**
  - **— Supports Motherboard and Add-In Card Implementations**
- **Compliant with PCMCIA 2.1/JEIDA 4.1 Interface Standard**
  - **— Supports up to Four 68-pin Standard PC Card Sockets, Cascadable for Additional Sockets**
  - **— Each Socket Interchangeably Supports Either Memory or I/O PC Cards**
  - **— Software Compatible with the Industry Standard 82365SL PCIC**
  - **— Supports PCMCIA-ATA Disk Drive Devices**
  - **— Features Prefetch Read and Post Write Data Buffer for PCMCIA Memory Cycles**
- **System Bus Timings Compatible with Pentium™ Processors and Intel486™ Processors**
  - **— Supports All Intel PCIsets**
  - **— Programmable PCMCIA and IDE Interface Timing**
  - **— Easily Configured to Support Other Standard Architectures**
- **Dual Voltage Operation**
  - **— Each PCMCIA Socket Automatically Configures to Support Either 3.3V or 5.0V PC Cards**
- **Power Management**
  - **— Individual Socket Power Control**
  - **— Hot Insertion and Removal Capability**
- **PCI Local Bus Interfaces for Four Enhanced IDE Devices**
  - **— Provides Write Posting and Read Prefetching to Support High Performance IDE Devices**
  - **— Primary and Secondary IDE Devices can be Independently Programmed for Various Speed Selections**
- **Flexible System Configuration Options**
  - **— Two-Socket Configuration with On-Chip Buffering**
  - **— Four-Socket Configuration with Partial External Buffering**
- **Eliminates the Need for System Configuration Jumpers**
  - **— Address Mapping for PCMCIA 2.1/JEIDA 4.1 PC Card Memory**
  - **— Address Windowing for I/O Space**
  - **— Full 4-GByte PCI Address Range**
  - **— Selectable Interrupt Steering from PC Cards to System Interrupt Lines**
- **208-Pin QFP Package**

The 82092AA is a high-bandwidth, software-configurable bridge that interfaces as many as four PCMCIA/ExCA (PC Memory Card International Association/Exchangeable Card Architecture) PC cards and four enhanced IDE devices to the Peripheral Component Interconnect (PCI) Bus. It is software compatible with the Intel 82365SL PC Card Interface Controller, but features a 32-bit PCI interface for maximum system performance. The PPEC simplifies system design by reducing component count between the PCI Bus, PC cards, and IDE devices, and maximizes system flexibility by providing such benefits as PC card select decoding, multiple memory address translation maps, power management, and I/O interrupt steering. The PPEC also supports auto-configuration, allowing dynamic system setup when inserting and removing PC Cards.

December 1994
Order Number: 290511-002



Mode 0 (Two Socket) Block Diagram



Mode 1 (Four Socket) Block Diagram

82092AA
PCI TO PCMCIA/ENHANCED-IDE CONTROLLER

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1.0 INTRODUCTION

The PPEC is a follow-on product to the Intel industry standard 82365SL PC Card Interface Controller (PCIC) used in mobile systems. It enhances the 82365SL definition by providing a full 32-bit PCI interface for increased system performance, and by supporting up to four PCMCIA sockets and four local bus IDE devices for greater flexibility. The PPEC is 82365SL compatible, and provides a standard system interface for PC Cards at the hardware and data interchange level.

Figure 1 shows a typical PPEC system implementation. The PPEC interfaces directly to the 5.0V PCI Local Bus, and supports four PCMCIA cards and four IDE devices in the configuration that is shown. The PPEC operates as a slave over the full PCI frequency range, but is optimized for 25 MHz and 33 MHz.

PPEC Configuration Modes

The PPEC supports two configuration modes that allow selection of the number of PC Card sockets supported, the number of IDE interfaces supported, and the type of buffering for each socket.

Mode 0 configures the PPEC for two independent PCMCIA sockets, or for one PCMCIA socket and two IDE interfaces. The sockets are internally buffered, and allow hot (power-on) card insertion and extraction. Each of the two IDE interfaces supports two IDE devices.

Mode 1 configures the PPEC for up to four PCMCIA sockets and two IDE interfaces. External buffering is used for the address, data, and shared control signals if fully-buffered interfaces are required. Each of the two IDE interfaces supports two IDE devices, as in Mode 0.

Each PPEC PCMCIA/JEIDA card interface consists of 60 signal and 8 power connections. In Mode 0, each of the two PCMCIA sockets has its own set of signals and buses, but the IDE interface signals are multiplexed with Socket A signals. In Mode 1, one address bus, one data bus, and several control signals are used as common signals for all four sockets, and several IDE interface signals are multiplexed with the common signals.

1.1 Enhanced PCI Local Bus IDE Interface

The local bus IDE interfaces, designated the Primary IDE Interface and the Secondary IDE Interface, and their corresponding drives #0 and #1 are independently programmed to operate in the enhanced (programmable) timing mode, or in standard compatible timing mode. The IDE physical interface is multiplexed with existing PCMCIA signals to reduce cost, and the IDE controller uses internal PCMCIA Post-Write data buffers and separate Read-Prefetch buffers to improve the system performance. The interfaces are externally buffered in both PPEC configuration modes.

The PPEC provides an IDE Hardware Configuration mechanism using the Power-On IDE Configuration Register which is mapped in the PCI configuration space. This allows full use of the PPEC's Enhanced Fast Local Bus IDE without any requirement for BIOS upgrade or modification if the BIOS is not aware of the PPEC IDE.

The higher performance of the PCI local bus IDE architecture with respect to the ISA IDE architecture results from the faster timing modes that are available in the PCI local bus IDE architecture. The PPEC provides improved timing even when the IDE controller is configured to run cycles that correspond to IDE ATA specification timing modes 0, 1 or 2 (which are originally defined for ISA-based systems) because of the proximity to the host CPU, and because of the clock granularity (PCI 33 MHz) at which timing is controlled. A more significant improvement is obtained when the PPEC is configured for the drives that support enhanced timing mode 3 or any arbitrarily-defined faster timing mode.

Enhanced Timing

The PPEC features programmable timing (see Primary and Secondary IDE Timing Control Register descriptions) in the form of clock counts for the following timing parameters:

- T_{su} (address/data set-up time)
- T_{pw} (command pulse width)
- T_{cyc} (overall cycle length)

The programmable timing allows support of currently defined and future IDE Modes, and for optimizations based on PCI clock frequencies other than 33 MHz. IDE Primary and Secondary interface timing is independently controlled, allowing IDE drives with different timing characteristics to be supported by the same physical interface while still operating at their optimum speeds.

Further timing configuration is provided at the level of the Primary and Secondary interface. Each drive (drive 0 and drive 1) can be independently programmed to run in enhanced timing mode or in standard compatible Mode #0, so that any combination of fast and slow drives is possible.

1.2 Internal Register and PCMCIA Address Window Access

The PCI-PCMCIA Bridge PCI Configuration Registers and the PCI-IDE PCI Configuration Registers conform to the Peripheral Component Interconnect (PCI) specification. The specification describes the essential registers that must be supported by PCI devices and functions, and should be referenced for a detailed explanation of the PCI-PCMCIA Bridge and PCI-IDE PCI Configuration Register access.

1.2.1 PCMCIA SOCKET CONFIGURATION REGISTER ACCESS

The PCMCIA Socket Configuration registers, comprised of general setup registers, interrupt registers, I/O mapping control registers, and memory mapping control registers, are used for control of the PCMCIA socket functions. They are a superset of the 82365SL register set, and are accessed using the same indexing method that is used in the 82365SL.

Two read/write ports, an *index port* and a *data port,* are used to access the registers. The index port is written with the register offset that is used to access the register. Data is then written to the register or read from the register via the data port.

The index port address is loaded into the PCI-PCMCIA Bridge Base Address Register, which is located in PCI Configuration space. The data port address is the next location (index port address + 1). When writing to the configuration registers, the index and data registers may be accessed simultaneously with a 16-bit write operation to increase performance. The index value is placed on data bits[7:0], and the data value to be written is placed on data bits[15:8].

The PPEC does not respond to a data port read or write operation unless a valid index has first been written to the index port.

1.2.2 PCMCIA MEMORY WINDOWS

The PPEC supports five independently enabled and configured memory and I/O address mapping windows for each PCMCIA PC Card socket. The windows allow portions of 64 MByte common memory and/or 64 MByte attribute memory spaces on the PC Cards to be mapped to portions of the PCI Memory address. Each window's data bus width, PCMCIA interface timing, software write protect, and enable can be independently controlled. Mapping of each memory window can start and stop on any 4 KByte boundary of PCI memory space within a 16 MByte page.

A Card Memory Page Address Register associated with each socket allows selection of the 16 MByte window page anywhere in the 4 GByte PCI address space (see Figure 2). The PC Card memory offset address is added to the PCI address bits 23:12 to generate the address for the PC Card. The address mapping is compatible with the 82365SL.

A window is opened by writing the PCI Memory start address, PCI Memory stop address, and PC Card memory offset to the window's *System Memory Address Mapping Start, System Memory Address Mapping Stop, and Card Memory Offset Address* high and low byte registers. The Card Memory Page Address Register must be written with the window's 16 MByte page address in PCI memory space, and the window must be enabled in the Address Window Enable Register.

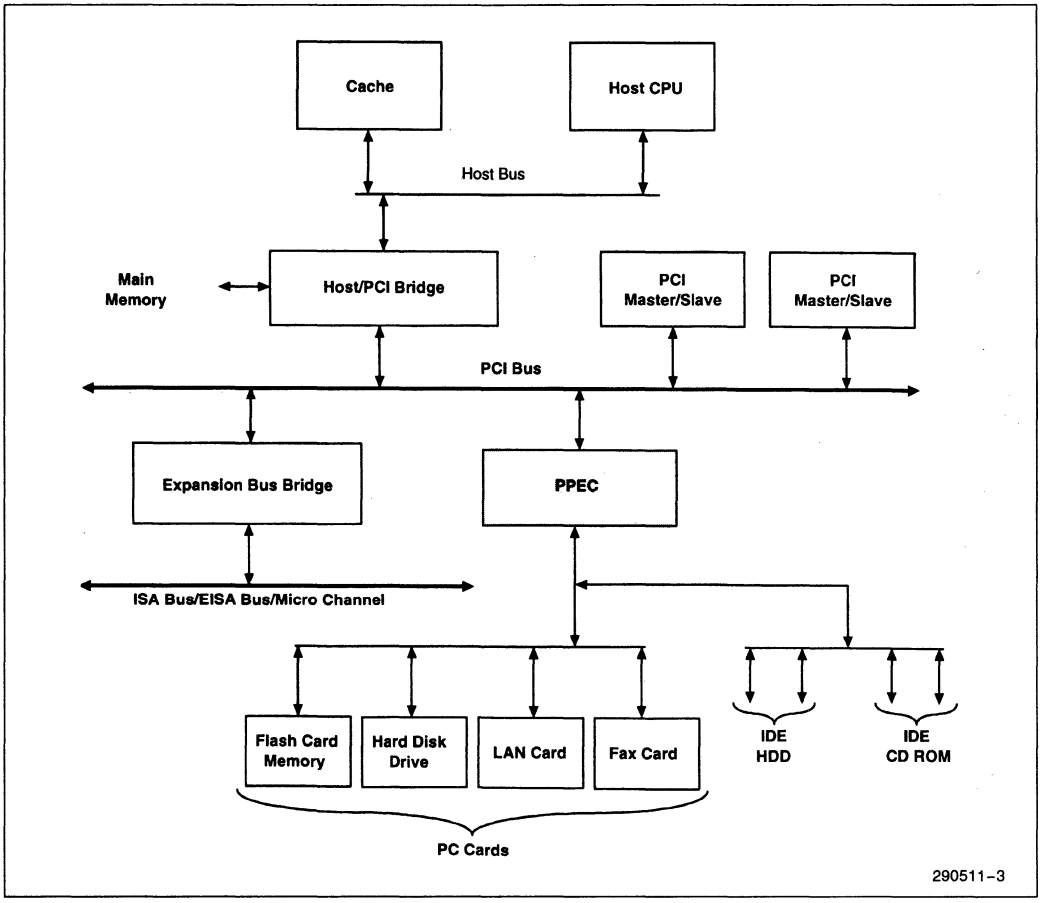


Figure 1. Typical PPEC System Implementation

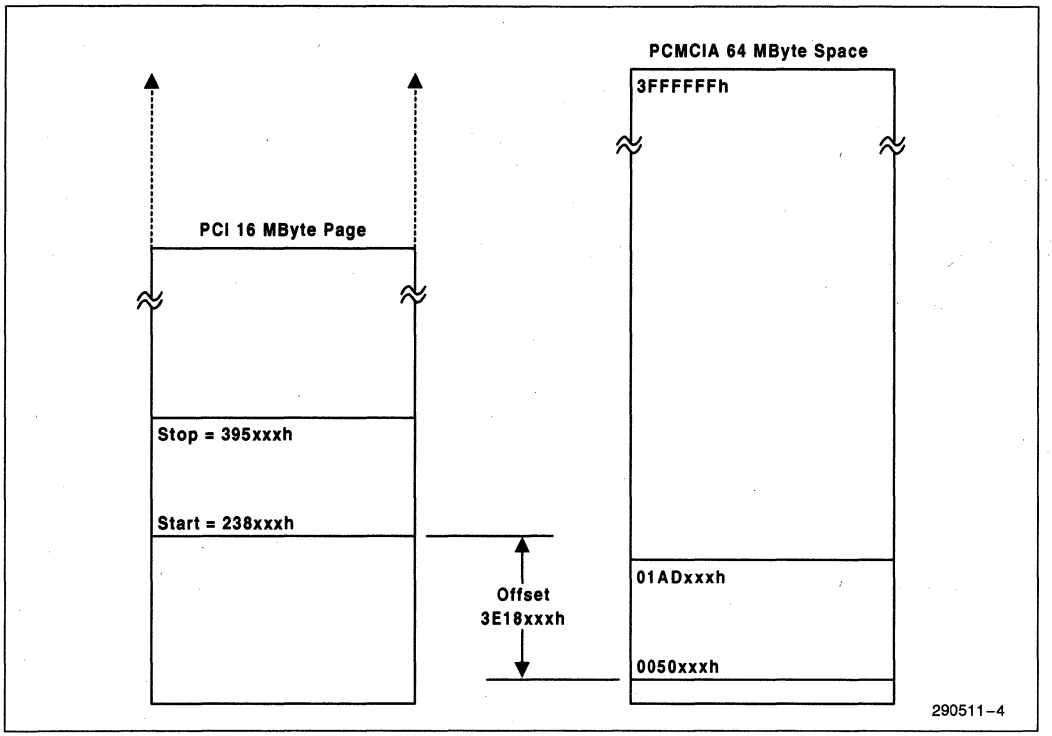


Figure 2. PCMCIA Memory Address Mapping

Common/Attribute Memory Address Mapping

Both Common and Attribute memory can be accessed on the PC Card through any of the PCI Memory address mapping windows according to the state of the *Register Active* bit in the Card Memory Offset Address High Byte Register. When this bit is set to 0, common memory can be accessed; when set to one, attribute memory can be accessed. The PCI memory window to common or attribute memory can be mapped from any PCI address to any PC Card address.

Several PCI Memory address mapping windows to different common memory address spaces can be opened simultaneously. Each of these windows can be configured to use a different timing mode, software write protect, and data width.

1.2.3 PCMCIA I/O WINDOWS

The PPEC features two independently enabled and controlled I/O address windows for each PCMCIA PC Card socket. The windows can be non-contiguous, and each window's I/O data bus width can be independently controlled. The windows have a 1 byte addressing resolution.

I/O addressing of PC Cards is very similar to memory addressing. Each I/O address window has a 16-bit *start address* and a 16-bit *stop address* located in the window's *I/O Address Start* and *I/O Address Stop* high and low byte registers. PCI I/O Address bits[15:0] are compared with the start and stop addresses and must be greater than or equal to the start address, and less than or equal to the stop address for access to the window. PCI address bits[31:16] must be 0 when addressing I/O Cards.

Indirect offset addressing is not supported for I/O windows. PCI I/O Address bits[15:0] are passed directly to the PC Card address pins if they fall within an I/O Window. Bits[25:16] of the PC Card address are driven low.

1.3 Data Buffers

The PPEC features read prefetching and write posting data buffering for up to four Dwords. This allows high speed 32-bit data transfers between the PCI Local Bus and the PPEC, and lower-speed 8-bit and 16-bit data transfers between the PPEC and the PC Cards and the IDE devices. Assembly/disassembly logic translates 32-bit data from the PCI bus into 8- and 16-bit data required by the PCMCIA PC Cards and the IDE devices.

Figure 3 shows a representation of the data buffer and the IDE prefetch buffers. The same physical buffers are used for both PCMCIA/IDE Posted Write operations, and for PCMCIA Prefetch operations. Separate 32-bit latches are used for storing IDE Prefetch data: one for the Primary drive interface, and one for the Secondary drive interface.

The operation of the data buffers is controlled by two bits in the PCI-PCMCIA Configuration Control Register that enable and disable Posted Write Buffer and IDE Prefetch operation. Both modes may be active simultaneously, but the write posting function has priority over the prefetch function.

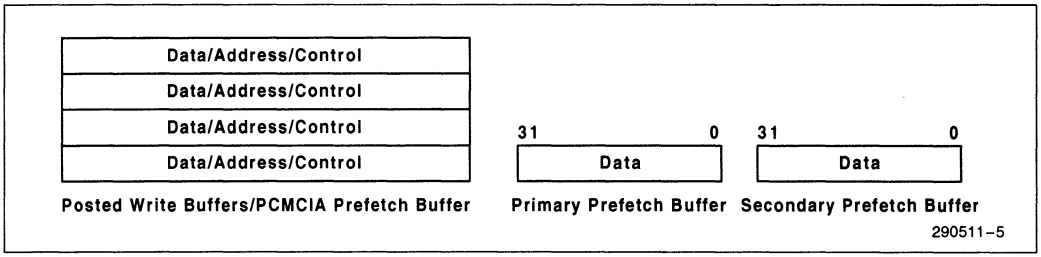


Figure 3. Data and IDE-Prefetch Buffers

Posted Writes and Prefetch Reads for IDE cycles are globally enabled in the PCI-PCMCIA PCI Configuration Control Register, and individually enabled for each IDE device in the PCI-IDE Configuration Control Register. IDE Posted Write cycles operate the same way as PCMCIA Posted Write cycles. However, the PPEC does not support burst data transfers for IDE Posted Write operations.

The data buffers are not used for Attribute Memory cycles because of potential timing dependencies.

1.4 PCMCIA Interface

The PPEC configuration mode is selected by an external 10-20K Ohm resistor on the SPKROUT#/MODE pin. The voltage level applied to the pin is sampled at the end of the reset sequence, and the state is stored internally in the PPEC-PCMCIA PCI Configuration Control Register (PCICON). The pin is then reconfigured as an output to support the SPKROUT function. The AREG#/IDECFG pin is also sampled at the end of the reset sequence to determine whether IDE is supported in Mode 0.

Table 1 shows mode selection with the SPKROUT#/MODE and AREG#/IDECFG pins.

Mode 0

Two PCMCIA sockets are supported in Mode 0. Each socket interface (Socket A and Socket B) has its own data bus, address bus, and control pins.

If the AREG#/IDECFG pin is sampled high at the end of the reset sequence, the Socket A PCMCIA registers are disabled and the Socket A interface pins are reconfigured for IDE support, allowing the implementation of two Fast Local Bus IDE interfaces capable of supporting up to four IDE devices. Signal mapping for the IDE Interface in Mode 0 is described in Section 2.8, IDE Interface Signals.

Mode 1

Four PCMCIA sockets are supported in Mode 1 by allowing sockets A, B, C, and D to share a common data bus (CDATA[15:0]), a common address bus (CADR[25:0]), and four common control signals (REG#, OE#, IORD#, and IOWR#). The other control signals are not shared.

External data buffers for each PCMCIA Socket may be used in Mode 1 to prevent the PC Cards from driving an excessive load, and to allow both 3.3V and 5V cards to be used simultaneously in a system. External buffers for the shared address and control lines are optional. They can be fully buffered for each socket or, by utilizing the INSERT# pins, can be either driven directly by the PPEC, or buffered by a single buffer to increase drive strength. See the *PPEC Design Guide* for specific application information.

Table 1. Configuration Mode Selection

SPKROUT#/MODE	AREG#/IDECFG	Mode	Configuration
0	0	0	2 Fully-Buffered PCMCIA Sockets; No IDE
0	1	0	PCMCIA Socket B Only; Dedicated IDE Interface
1	X	1	4-PCMCIA Sockets; Shared Address, Data, Control

Two Fast Local Bus IDE interfaces can be enabled in Mode 1 by programming the PPEC-IDE Interface PCI Configuration Registers. When an IDE cycle is initiated, the PDIR# and SDIR# pins provide direction control for the external IDE data buffers, and the PCS1#, PCS2#, SCS1# and SCS2# signals enable the IDE devices. The PCMCIA sockets are not affected during IDE cycles because the card enables for each socket remain inactive.

The AREG#/IDECFG pin is ignored in this mode.

1.4.1 CARD INSERTION AND EXTRACTION

The INSERT# function allows the PPEC to prepare for the insertion of a PC Card, preventing the insertion from affecting other sockets in implementations requiring shared signal lines (Mode 1, partially buffered). The INSERT# pin is driven active at least 1.5 μs prior to the PC Card signal-pin contact with a PCMCIA socket by an external circuit described in the PPEC Design Guide.

The PPEC empties the Posted Write Buffers (PWBs) and tri-states the shared PCMCIA address and control lines when a falling edge occurs on INSERT#. The PPEC drives the shared signals after power has been applied to the new PC Card, and normal operation resumes.

When a rising edge occurs on a CDx pin, the PPEC again empties the Posted Write Buffers and tri-states the shared address and control lines, and the dedicated PCMCIA socket signals. A rising edge on INSERT# indicates that the PC Card has been disconnected from the signal pins, allowing the PPEC to drive the shared signals and resume normal PCMCIA operation.

Hot insertion and extraction is possible in Mode 0 because all PCMCIA interface signals are independent of each other in this mode. When a card insertion is detected via the Card Detect inputs (xCD#[2:1]) with the Card Detect interrupt enabled, a Card Status Change interrupt is initiated, and power is applied to the PCMCIA socket under software control. When a card removal is detected via the Card Detect inputs, the voltage to the socket is turned off under software control.

1.4.2 POWER CONTROL

The PPEC implements power management for each PCMCIA socket individually. Socket power management is controlled through the Power Control Register and the VS1/VS2 pins.

1.4.2.1 Power Control Register Operation

The Power Control Register controls the routing of power to the PCMCIA socket and enabling of the PCMCIA socket interface pins. A PCIRST clears all of the bits in this register. A detailed description of all of the bits in this register is found in Section 3.2.1.3. This section describes only the V_{CC} Control and V_{PP} Control bits.

V_{CC} Control

The V_{CC} Control bits in the Power Control Register control power to the PC Cards via an external latch. The control signals $V_{CC}5V$ and $V_{CC}3V$ are routed to the external latch through the ACDATA lines during Power Control Write cycles. The value of these bits is modified by software writes to the Power Control Register or by hardware according to the value of the VS1/VS2 pins. Hardware modifies the V_{CC} Control bits only when the INSERT# signals are asserted, indicating partially buffered, Mode 1 implementations.

The V_{CC} Control bits control V_{CC} routing using the following encoding:

Power Control Register Bits		$V_{CC}5V$	$V_{CC}3V$	Description
Bit 4	Bit 3			
0	0	0	0	No Connect
0	1	0	0	Reserved
1	0	1	0	5.0 V
1	1	0	1	3.3 V

If the INSERT# signals are used in Mode 1 partially-buffered implementations, the VS1/VS2 pins are sampled during a PC Card insertion and are used to determine the values of $V_{CC}5V$ and $V_{CC}3V$. The VS1/VS2 pins affect the V_{CC} Control bits in the following way:

VS1	VS2	Power Control Register Bits		$V_{CC}5V$	$V_{CC}3V$	Description
		Bit 4	Bit 3			
0	0	1	1	0	1	3.3V
0	1	1	1	0	1	3.3V
1	0	0	0	0	0	Not Supported; (SERR# Asserted)
1	1	1	0	1	0	5.0V

In Mode 0 and in fully-buffered Mode 1 implementations, the INSERT# signals are not used, and power control is completely dependent upon software.

V_{PP} Control

The V_{PP} Control bits in the Power Control Register are latched externally, along with the V_{CC} Control bits. They are modified with software writes to the Power Control Register only.

1.4.2.2 External Power Control Latch

The PPEC is designed to directly interface with Maxim's MAX780 Dual-Slot PCMCIA Power Controller. This device provides V_{PP} power and controls V_{CC} power for 2 PCMCIA sockets. Two MAX780's are required for 4-socket implementations. The MAX780 contains an internal register for latching the power control signals provided by the 82365SL and compatible controllers $V_{PP}EN[1:0]$ and $V_{CC}EN[1:0]$. This latch allows the PPEC to write the values of the power control signals via the PCMCIA data lines, thus eliminating the need for dedicated power control signals. If the Maxim device is not used in a system, an external register (74ALS273 or equivalent) is required to latch the power control signals. This external latch, whether implemented using the Maxim device or a 74ALS273, is referred to in this document as the External Power Control Latch.

The following are the signals that transfer power control information to the External Power Control Latch, and the bus signal pins through which they are transferred.

Power Signal	Transfer Pin Name
Power Control Write Signal	PWRWR#
Socket A V_{PP}EN0 Control Signal	ACDATA[0]
Socket A V_{PP}EN1 Control Signal	ACDATA[1]
Socket B V_{PP}EN0 Control Signal	ACDATA[2]
Socket B V_{PP}EN1 Control Signal	ACDATA[3]
Socket A V_{CC}3V Control Signal	ACDATA[4]
Socket A V_{CC}5V Control Signal	ACDATA[5]
Socket B V_{CC}3V Control Signal	ACDATA[6]
Socket B V_{CC}5V Control Signal	ACDATA[7]
Socket C V_{PP}EN0 Control Signal (Mode 1 Only)	ACDATA[8]
Socket C V_{PP}EN1 Control Signal (Mode 1 Only)	ACDATA[9]
Socket D V_{PP}EN0 Control Signal (Mode 1 Only)	ACDATA[10]
Socket D V_{PP}EN1 Control Signal (Mode 1 Only)	ACDATA[11]
Socket C V_{CC}3V Control Signal (Mode 1 Only)	ACDATA[12]
Socket C V_{CC}5V Control Signal (Mode 1 Only)	ACDATA[13]
Socket D V_{CC}3V Control Signal (Mode 1 Only)	ACDATA[14]
Socket D V_{CC}5V Control Signal (Mode 1 Only)	ACDATA[15]

Note that in Mode 1, the ACDATA bus is renamed to CDATA.

The value of the V_{CC}3V and V_{CC}5V signals and V_{PP}EN[1:0] are determined by the control bits in the Power Control register for each socket.

The External Power Control Latch is updated by placing the values of the power control signals onto the corresponding ACDATA lines, and pulsing the PWRWR# signal low. This operation takes place after each of the following conditions:

- A write cycle to any of the Power Control registers
- A high Card Detect pin on a socket having Auto Power enabled
- Rising edge of PCIRST#
- PC Card Reset
- Detection of a PC Card insertion via one of the xINSERT# pins

The PPEC allows any cycle currently taking place on the PCMCIA bus or PCI bus to complete before performing an external power control write cycle, then initiates a write cycle to the external latch. The power control write operation cycle time is 6 PCICLKs, and consists of placing the Power Control bits for all sockets on the ACDATA bus, pulsing the PWRWR# signal for 5 PCICLKs, and holding the data for one additional clock to guarantee hold time. If a PCMCIA-targeted PCI cycle is initiated during an external power control write cycle, the PCI cycle is held in wait-states until the PCMCIA cycle can be executed.

1.4.2.3 Hardware-Initiated Power On Sequence

When the INSERT# pins are used to detect card insertions, the PCMCIA bus is tri-stated until power has been applied to all PC Cards. A condition could exist where a PCI Master device other than the CPU tries to access the PCMCIA bus while the PCMCIA bus is tri-stated, causing the PCI Master to be retried. This would effectively lock out the CPU from the PPEC and prevent the CPU from applying power to the PC Card. To avoid this situation, the PPEC must perform a hardware-initiated power-on sequence to the PC Card whenever the PCMCIA bus is tri-stated due to a PC Card insertion.

The following sequence of events describes a hardware-initiated power-on sequence:

1. INSERT# is detected active for one of the PCMCIA sockets.
2. Line buffers are flushed and the PCMCIA bus is tri-stated.
3. CD1# and CD2# are detected active.
4. The Power Control Register is updated according to the values of VS1/VS2.
5. An external power control write cycle is performed.
6. The PPEC is held for 256 PCICLKs (7.68 μs minimum) to allow V_{CC} voltage to stabilize.
7. The PCMCIA bus and The PPEC resume normal operation.

Any subsequent writes to the Power Control Registers by software override the V_{CC} Control bits set by hardware. If VS1/VS2 indicate the presence of an X.X-only PC Card, the PPEC does not apply power to the card and the PCMCIA bus is held in a tri-state condition until the card is removed. This situation is indicated by HOLDLED# remaining active. If SERR# is enabled, the PPEC asserts SERR# for one PCICLK to alert the system that an error condition exists, and operation can not continue.

1.4.2.4 Auto Power Enable

The Auto Power function in the PPEC is intended to allow hardware to automatically power down a PCMCIA socket based on the Card Detect pins (CDx). With Auto Power enabled, the power control signals $V_{CC}5V$ and $V_{CC}3V$ are active only while both Card Detect inputs are low. As soon as one of the CDx lines goes high indicating that a card is being extracted, an external power control write cycle is initiated to negate the active power control pins. The V_{PP} control pins are automatically negated with the negation of the V_{CC} control pins, independent of the Auto Power function. Software is responsible for debouncing the CDx pins and disabling Auto Power whenever a card is extracted. When the Auto Power function is disabled, the power control signals are not qualified with the Card Detects. The sequence of steps for inserting and extracting a PC Card when using Auto Power is as follows:

1. The default is Auto Power Enable = 0.
2. Software receives a Card Status Change (CSC) interrupt as a result of a card being inserted.
3. Software waits for the CDx pins to become stable.
4. Software reads the VSx pins and sets the V_{CC}/V_{PP} control bits in the Power Control Register.
5. The PPEC issues a write cycle to the external power control latch (Maxim Power Switch or discrete latch).
6. Software waits for power to become stable (50 μs minimum).
7. Software enables the socket interface and sets Auto Power Enable = 1.

Normal operation takes place.

8. The PPEC detects a rising edge on either CDx pin.
9. The PPEC sends a CSC interrupt and issues a write cycle to the external power control latch to disable the socket power. A hardware flag is automatically set, disabling power to the socket.
10. Software waits for the CDx pins to become stable.
11. Software disables the socket interface and sets Auto Power Enable = 0.
12. The PPEC clears the flag that disables power to the socket as a result of step 11.

When the Auto Power bit of the Power Control register (bit 5) is 0, Auto Power is disabled and power is controlled directly from the power control bits without being qualified with CDx. The PPEC does ***not*** prevent software from powering a card to a voltage other than that indicated by the VSx pins. Table 2 summarizes the operation of the PPEC power control.

1.5 PC Card ATA Support

The PCMCIA specification defines a protocol for ATA PC Cards. No special requirements are needed for accesses to PC Card ATA. Accesses to all ATA registers are treated as normal I/O accesses.

1.6 PCI Interface

The PPEC is a PCI target-only device. Its PCI Interface conforms to the Peripheral Component Interconnect (PCI) specification, which should be referenced for an understanding of the interface.
Table 3 identifies the PCI commands that the PPEC supports, and their encoding on signal lines C/BE#[3:0]. The PCI bus signal descriptions in the following section further define the PCI operations that are supported by the PPEC.

1.6.1 PCI SUPPORT

The following sections describe PPEC PCI support. Note that the PPEC is a target-only device, and therefore does not support PCI functions that are defined for PCI masters.

1.6.1.1 Address Decoding

The PPEC uses only positive address decode. The PPEC's PCI-PCMCIA Bridge and PCI-IDE Interface functions both have SLOW DEVSEL# timing response.

Table 2. Power Control Operation

Power Control Register			PPEC Pins		Tri-state Outputs (See Note)	Interface Status Register
Output Enable (Bit 7)	V_{CC} Enable (Bit 4)	Auto Power Enable (Bit 5)	CD1#	CD2#		PC Card Power Active
X	0	X	X	X	OFF	0
0	1	0	0	0	OFF	1
1	1	0	0	0	ON	1
X	1	0	X	1	OFF	1
X	1	0	1	X	OFF	1
0	1	1	0	0	OFF	1
1	1	1	0	0	ON	1
X	1	1	X	1	OFF	0
X	1	1	1	X	OFF	0

NOTE:
For this table, the term Tri-state Outputs includes the PPEC outputs that are unique for a given PCMCIA socket. This includes all of the address, data, and control signals in Mode 0 (2-socket), but does not include the shared address, data, and control signals in Mode 1 (4-socket). The shared PCMCIA signals defined in Mode 1 are enabled and disabled as a function of the INSERT# signals as described in Section 1.4.1.

1.6.1.2 Configuration Cycles

The PPEC supports only Type 0 PCI configuration cycles. As a multifunctional device it supports access to functions numbered 0 and 1. It does not respond to a configuration cycle that accesses functions 2-7, even if the functions are selected with the IDSEL mechanism.

NOTE:
None of the PPEC internal registers or PCMCIA I/O or memory locations can be accessed after PCI reset until PCI Configuration Software (part of BIOS) configures the system resources properly.

1.6.1.3 Burst Transfer Support

The PPEC supports burst transfers to PCMCIA memory and to the IDE I/O Data Port with a post-write buffering mechanism when internal data buffering is enabled.

The PPEC supports only Linear Incrementing burst transfers. Attempts to access the PPEC using burst transfers in a mode other than Linear Incrementing results in subsequent target disconnects, and splitting of the burst cycle into multiple single data phase transfers.

1.6.1.4 Exclusive (Locked) Access Support

The PPEC can be locked as a resource by any PCI Initiator. In the context of locked cycles, the PPEC and the PCMCIA subsystem are considered a single resource. A locked access to any address within the PCMCIA subsystem locks the PPEC.

Note that write-posting and read-prefetch are disabled for PCI locked cycles. Any PCI Initiator access to the PPEC subsystem while it is locked results in retry.

Table 3. PCI Commands

C/BE# [3:0]	Command Type	Supported As Target
0000	Interrupt Acknowledge	No
0001	Special Cycle	No
0010	I/O Read	Yes
0011	I/O Write	Yes
0100	Reserved	N/A(3)
0101	Reserved	N/A(3)
0110	Memory Read	Yes
0111	Memory Write	Yes
1000	Reserved	N/A(3)
1001	Reserved	N/A(3)
1010	Configuration Read	Yes
1011	Configuration Write	Yes
1100	Memory Read Multiple	No(2)
1101	Reserved	N/A(3)
1110	Memory Read Line	No(2)
1111	Memory Write and Invalidate	No(1)

NOTES:
1. Treated as Memory Write.
2. Treated as Memory Read.
3. PPEC does not respond on these commands.

1.6.1.5 Transaction Termination

As a target, the PPEC terminates transactions for the following conditions.

Disconnect

The PPEC responds with a disconnect when it is the target of multiple data phase transactions that cannot be serviced by the internal buffers (i.e., posted for writes or supply prefetched data during read operations). During posting, the PPEC terminates the cycle using disconnect semantics as soon as all posted write buffers are occupied. Similarly, the PPEC disconnects during burst reads as soon as a miss is generated (prefetch data is not available). This is because the next data phases would exceed the 8 PCI clock incremental latency limit while the PCI is kept in wait-states for more that 8 PCI clocks until one of the post write buffers is emptied to its destination, or additional data is fetched from the PCMCIA card or IDE interface.

Retry

The PPEC retries memory write cycles when all post write buffers are full. It also retries any cycle when it is locked as a resource and a PCI master tries to access the PPEC without negating the PCILOCK# signal during the address phase.

Target Abort

The PPEC generates this type of termination during non-aligned Dword I/O transfers with illegal combinations of address and BEx.

1.6.1.6 Parity Generation And Checking

The PPEC supports parity generation and checking for both the address and data phases of cycles in which it positively decodes address. The PPEC asserts the PERR# signal when it recognizes a parity error during bus transactions in which it is involved. The PPEC asserts the SERR# o/d signal for one PCI clock when it detects an address phase parity error, or a PCMCIA interface system error (i.e., when a X.XV-only PC Card is inserted).

1.6.1.7 PCI Memory Cache Support

The PCI can provide basic cache coherency control with two optional PCI signals, SDONE and SBO#. The PPEC does not support those signals, so PCMCIA memory cannot be directly cached. However, alternative schemes can be used (including "shadowing" in main memory and caching locally) to speed access to the read-only PCMCIA memory. This can improve performance of the XIP (eXecute In Place) PCMCIA applications.

1.7 System Interface Functionality

The PPEC can connect to system interrupts in two different ways:

a. via 10 direct system interrupt signals.

b. via 2 PCI interrupt signal lines which require additional routing.

The direct system interrupt mode is provided so that PCMCIA software that requires "ISA compatibility" (i.e. non-shareable IRQ handlers which require specific IRQ level) can run without modifications on Intel Microprocessor Architecture based platforms with PPEC as a PCI-PCMCIA Bridge. In this case, PCI interrupts are not used but the PCMCIA Card interrupts (as well as the Card Status Change interrupt) are configured to connect directly to specific system IRQ lines. On the system side, the PPEC interrupt signals can support either edge (ISA like) or level (active low-EISA, Microchannel, PCI like) triggering. Multiple PC Cards in a system can conflict if they try to utilize the same Edge interrupt Level. By steering them to different interrupt lines, the conflicts can be eliminated.

Designs that are not dependent on this type of software "compatibility" can use PCI interrupts (i.e., interrupt is configured using mechanism "b").

The Global Control Register provides individual bits to enable Edge/Level Mode. The Interrupt and General Control Register contains bits for I/O card Interrupt Steering. The Card Status Change Interrupt Configuration register contains bits for Card Status Change Interrupts.

1.7.1 DIGITAL AUDIO SUPPORT—SPKROUT# SIGNAL

The PPEC supports PC Card digital audio SPKR# signals. These signals are passed through to the SPKROUT# line, which is an exclusive-OR of all SPKR# inputs (from all sockets). In motherboard designs, this output line can be connected to the system speaker driver directly. In add-in card implementations, a cable can be used to access the speaker, or a Piezo electric transducer can be provided on the add-in card.

2.0 PPEC SIGNALS

The signals described in this section are arranged in functional groups. The # symbol at the end of a signal name indicates that the signal's active or asserted state occurs when the signal is at a low voltage level. When # is not present after the signal name, the signal is asserted when it is at the high voltage level.

The terms *assertion* and *negation* are used extensively in this document to minimize confusion when a mixture of *active-low* and *active-high* signals are described. The terms *assert* and *assertion* indicate that a signal is active, independent of whether that level is represented by a high voltage or a low voltage. The terms *negate* and *negation* indicate that a signal is inactive.

The following notation is used to describe the PPEC signal types:

in: A standard input-only signal.

in (ST) A Schmitt Trigger input signal.

out A totem pole output signal.

o/d An open drain input/output signal.

t/s A bi-directional tri-state signal.

t/s/o A uni-directional, tri-state output signal.

s/t/s A sustained tri-state signal. This is an active low tri-state signal that is owned and driven by one and only one agent at a time. The agent that drives a s/t/s signal low must drive it high for at least one clock before letting it float. A new agent can not start driving an s/t/s signal sooner than one clock after the previous owner tri-states it. An external pull-up must be provided by the central resource to sustain the inactive state until another agent drives the signal.

2.1 PCI Bus Interface Signals

Name	Type	Description
PCICLK	in	**PCI CLOCK:** Provides timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. PPEC design is optimized for 25 MHz and 33 MHz PCI bus frequency. **NOTE:** PCMCIA and IDE state machines use PCICLK as a clock reference. This allows simpler design with good granularity for optimized timing, but selection of a PCI clock frequency other than 25 or 33 MHz may impact PCMCIA and IDE interface performance.
PCIRST#	in	**PCI RESET:** Forces the entire PPEC component into a known state. All t/s and s/t/s signals are forced to a high impedance state, and the o/d signals are allowed to float high. All internal PPEC state machines are reset, and all registers are set to their default values. PCIRST# may be asynchronous to PCICLK when asserted or negated. Although asynchronous, negation must be with a clean, bounce-free edge. PCIRST# must be asserted for a minimum 1 ms, and PCICLK must be active during the last 100 μs of the PCIRST# pulse.
AD[31:0]	t/s	**ADDRESS AND DATA:** Address and data are multiplexed on the same PCI pins. During the first clock of a transaction, AD[31:0] transfer a physical address (32 bits). During following clocks, AD[31:0] transfer data. A bus transaction consists of an address phase, followed by one or more data phases. PCI supports write bursts. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB), and AD[31:24] the most significant byte (MSB). The information contained in the two low order address bits varies by address space. In the I/O address space, AD[1:0] are used to provide full byte address. During memory space accesses, these two bits provide information on the type of burst ordering. During configuration space accesses, they identify the type of configuration access. When the PPEC is the target of a PCI cycle, AD[31:0] is input during the address phase of a transaction. During the following data phase(s), the PPEC asserts data on AD[31:0] if a PCI read, or accepts data if a PCI write.

2.1 PCI Bus Interface Signals (Continued)

Name	Type	Description
C/BE# [3:0]	in	**BUS COMMAND AND BYTE ENABLES:** These signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE# [3:0] define the bus command for bus command definitions. During the data phase, C/BE# [3:0] are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE# [0] applies to byte 0, and C/BE# [3] to byte 3. C/BE[3:0] # are not used for address decoding.
FRAME#	in	**CYCLE FRAME:** Driven by the current initiator to indicate the beginning and duration of an access. FRAME# is asserted to indicate that a bus transaction is beginning. Data transfers continue while FRAME# is asserted. When FRAME# is negated, the transaction is in the final data phase.
TRDY#	s/t/s	**TARGET READY:** Asserted by the PPEC as a target to indicate completion of the current data phase. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock during which both TRDY# and IRDY# are sampled asserted. When the PPEC is the target during a read cycle, TRDY# indicates that the PPEC has valid data asserted on AD[31:0]. When it is a target during a write cycle, it indicates that the PPEC is prepared to latch data.
IRDY#	in	**INITIATOR READY:** IRDY# as an input indicates that the current cycle initiator is able to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock during which both IRDY# and TRDY# are sampled asserted. When the PPEC is the target of a write cycle, IRDY# indicates that valid data is present on AD[31:0]. During a read, it indicates that the initiator is prepared to latch data.
STOP#	s/t/s	**STOP:** Indicates that the PPEC, as a target of an PCI cycle, is requesting a master to stop the current transaction. Different semantics of the STOP# signal are defined in the context of other handshake signals (TRDY# and DEVSEL#).
PCILOCK#	in	**PCI LOCK:** Indicates an atomic operation that may require multiple transactions to complete. When PCILOCK# is sampled negated during the address phase of a transaction in which the PPEC is involved, the PPEC's interface becomes a locked resource until it samples PCILOCK# and FRAME# negated. When other masters attempt accesses to PPEC while it is locked, the PPEC responds with a RETRY termination.
IDSEL	in	**INITIALIZATION DEVICE SELECT:** Used as a chip select during configuration read and write transactions. It is sampled during the address phase of a transaction. If the PPEC samples IDSEL active during configuration read or write and address AD[1:0] = 00, it will respond by asserting DEVSEL# on the next cycle.
DEVSEL#	s/t/s	**DEVICE SELECT:** The PPEC asserts DEVSEL# to claim a PCI transaction as a result of positive decode, and when it samples IDSEL active and address AD[1:0] = 00 during configuration cycles to the PPEC configuration registers.
PAR	t/s	**PARITY:** Parity is even across AD[31:0] and C/BE# [3:0]. The PPEC drives PAR during read data phases when it is a target of a PCI cycle. This signal is an input in all other cases. During an address phase or write data phase in which the PPEC is a target, the PPEC samples this signal to compare it with internally generated parity. Note that PAR signal driving and tri-stating is always one clock delayed from the corresponding AD[31:0] signal driving and tri-stating.

2.1 PCI Bus Interface Signals (Continued)

Name	Type	Description
INTA#	o/d	**PCI INTERRUPT REQUEST A:** This is a level sensitive, active low signal that is used to signal interrupts from the PPEC's PCI-PCMCIA functional block. It is enabled in the PPIRR register. The connection of INTA# to the system interrupt controller is system specific. Note that this signal typically requires an external pull-up resistor.
INTB#	o/d	**PCI INTERRUPT REQUEST B:** This is a level sensitive, active low signal that is used to signal interrupts from the PPEC's PCI-IDE Interface functional block. It is enabled in the PPIRR register. The connection of INTB# to the system interrupt controller is system specific. Note that this signal typically requires an external pull-up resistor.
PERR#	s/t/s	**PARITY ERROR:** This is a sustained tri-state signal that is used to report data parity errors during all transactions for which the PPEC positively decodes address. It is typically used by the system logic to generate an NMI. SERR# is pure open drain, and is actively driven for a single PCI clock. The assertion of SERR# is synchronous with the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the negated state is accomplished by a weak pull-up resistor (same value as for s/t/s) which is provided by the system design, and not by the signaling agent or central resource. This pull-up resistor may take two to three clock periods to fully restore SERR#.
SERR#	o/d	**SYSTEM ERROR:** An open-drain signal that is used to report address parity errors during all transactions in which PPEC is involved. It is typically used by the system logic to generate an NMI. SERR# is pure open drain and is actively driven for a single PCI clock. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the negated state is accomplished by a weak pull-up resistor (same value as used for s/t/s) that is provided by the system, and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#.

2.2 System Interrupt Signals

Name	Type	Description
IRQ3	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ3:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ4	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ4:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.

2.2 System Interrupt Signals (Continued)

Name	Type	Description
IRQ5	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ5:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ7	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ7:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ9	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ9:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ10	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ10:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ11	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ11:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ12	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ12:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ14	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ14:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ15	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ15:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt requirements. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.

2.3 Audio Interface And Configuration Mode Selection Signal

Name	Type	Description
SPKROUT# /MODE	t/s or o/d	**SPEAKER OUTPUT OR PCMCIA INTERFACE CONFIGURATION MODE:** SPKROUT# /MODE is configured as an input during reset. The user selects 2-Socket Mode with a weak pull-down resistor (10K) on the signal pin, and selects 4-Socket with a weak pull-up resistor. The PPEC automatically reconfigures the pin as an output for use as SPKROUT# after reading and storing the state of the SPKROUT# /MODE pin at the end of the reset sequence. This signal MUST be connected to an external pull-up or pull-down resistor according to the desired operating mode.

2.4 External Power Control Signal

Name	Type	Description
PWRWR#	out	**POWER CONTROL WRITE:** This signal is a write strobe for the PCMCIA Socket Power Control Logic. It is used to latch V_{CC} and V_{PP} power-control information that is transferred via the PCMCIA Socket A data lines. This signal is active during I/O write access to the PPEC's internal PCMCIA Power Control Registers, and during automatic Power-Control write sequences when reset is active or when the PCMCIA auto-power function is activated.

2.5 PCMCIA Interface Signals

The PPEC supports two PCMCIA socket configuration modes: Mode 0 and Mode 1. The number of sockets supported differs with each mode. The PPEC signals therefore change according to the operating mode.

All t/s and t/s/o PCMCIA signals are implemented using 5V/3.3V configurable buffers.

2.5.1 MODE 0 (TWO-SOCKET) CONFIGURATION MODE SIGNALS

Mode 0 configures the PPEC for two PCMCIA sockets: Socket A and Socket B. PCMCIA function signals are identical for both sockets. However, Socket A signals may be multiplexed with IDE interface signals (see Section 2.6) while Socket B signals are not multiplexed, and the Socket A AREG#/IDECFG signal has two functions while the Socket B REG# signal has one function. Figure 4 shows the PPEC signal pinout for Mode 0.

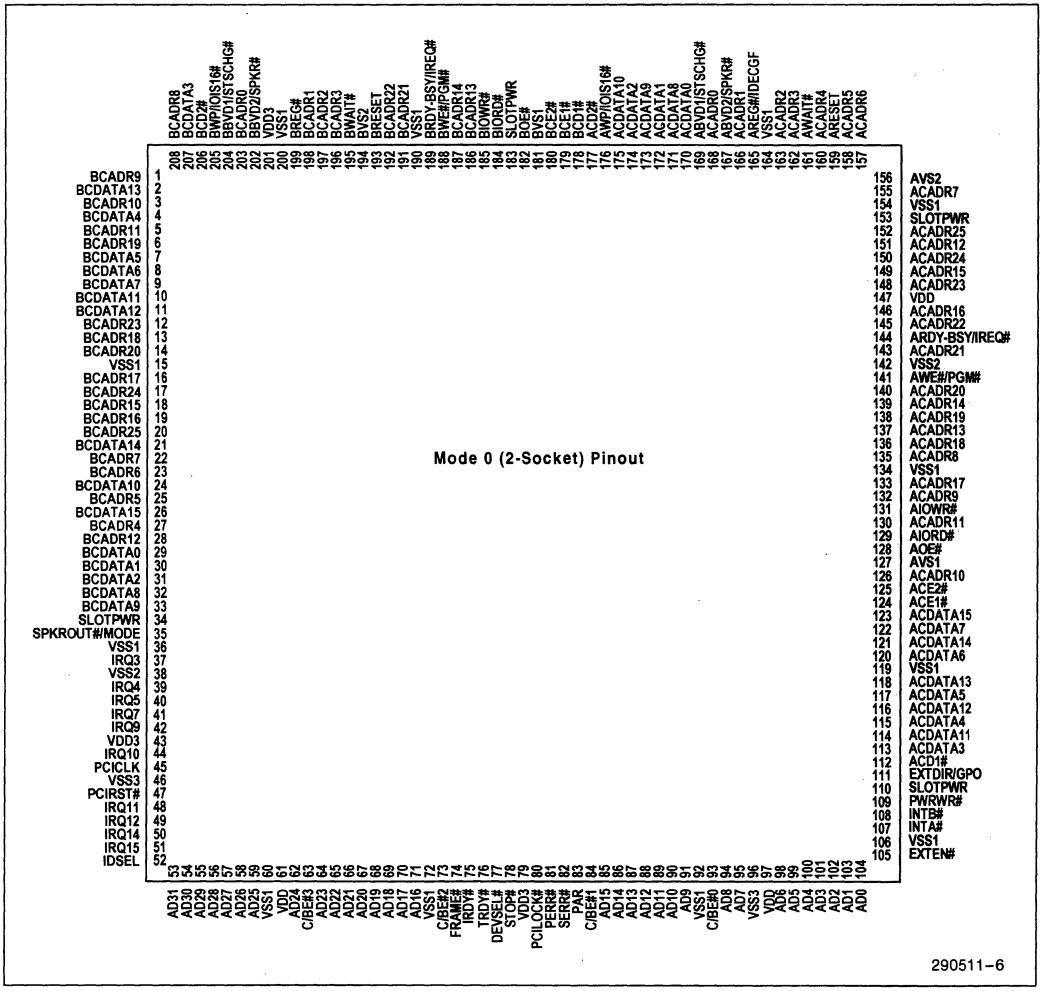


Figure 4. Mode 0 Pinout

2.6 Socket A and B PCMCIA Signals

Name	Type	Description
ACDATA[15:0] BCDATA[15:0]	t/s	**SOCKET A AND SOCKET B DATA BUS SIGNALS [15:0]:** This is a 16-bit data bus that is used for data transfer between the PPEC and the PCMCIA card.
ACADR[25:0] BCADR[25:0]	t/s	**SOCKET A AND SOCKET B ADDRESS BUS SIGNALS [25:0]:** This is a 26-bit address bus that is used for addressing memory locations and attribute memory within a 64 MByte PCMCIA address range, and for addressing I/O within a 64 KByte PCMCIA address range.
AIORD# BIORD#	t/s/o	**SOCKET A AND SOCKET B I/O READ:** The PPEC uses this active low signal and the REG# signal to gate I/O Read data from the PC Card. When low, IORD# gates I/O Read data from a memory PC Card only when the REG# signal is also asserted.
AIOWR# BIOWR#	t/s/o	**SOCKET A AND SOCKET B I/O WRITE:** The PPEC uses this active low signal and the REG# signal to gate I/O Write data to the PC Card. When low, IOWR# gates the I/O Write data to the PC Card only when the REG# signal is also asserted.
AREG#/ IDECFG	t/s/o in	**SOCKET A ATTRIBUTE MEMORY SELECT AND IDE CONFIGURATION:** This signal has two functions. During reset it is configured as an input with the IDE Configuration function. The signal level is sampled at the end of the reset sequence. If it is sampled low, all of the Socket A pins are used for PCMCIA Socket-A interface signals; if it is sampled high, some of Socket A pins are used for IDE interface signals. The status of IDECFG pin when sampled is stored in the PPEC IDE Configuration Register so that it can be used to support BIOS software with enhanced auto-configuration capabilities. If it is sampled low at the end of the reset sequence, the signal is configured after reset as an output with the Attribute Memory Select function. The signal is inactive (high) during all normal accesses to main memory of PC Cards. I/O PC Cards do not respond to IORD# or IOWR# assertion when the AREG# signal is inactive. When it is active (low), access is limited to Attribute Memory when WE# or OE# are active, and to I/O ports when IORD# or IOWR# are active. Configurable memory PC Cards and I/O PC Cards contain configuration and status registers in the Attribute Memory Space. This signal pin MUST be either externally pulled-up (IDE interface) with a weak pull-up resistor (10K Ohm) or pulled down (no IDE interface), depending on the system configuration.
BREG#	t/s/o	**SOCKET B ATTRIBUTE MEMORY SELECT:** This signal is inactive (high) during all normal accesses to what is known as Main Memory of the PC Card. I/O PC Cards do not respond to IORD# or IOWR# when the BREG# signal is inactive. When this signal is active (low), access is limited to Attribute Memory when WE# or OE# are active, and to I/O ports when IORD# or IOWR# are active. Configurable memory PC Cards and I/O PC Cards contain configuration and status registers in the Attribute Memory Space.
AOE# BOE#	t/s/o	**SOCKET A AND SOCKET B OUTPUT ENABLE:** This is an active low signal that gates Memory Read data from memory PC Cards.

2.6 Socket A and B PCMCIA Signals (Continued)

Name	Type	Description
ACE[2:1]# BCE[2:1]#	t/s/o	**SOCKET A AND SOCKET B CHIP ENABLE [2:1]:** These are active low signals that are driven by the PPEC when the socket is enabled. CE1# enables even bytes; CE2# enables odd bytes.
AWE#/PGM# BWE#/PGM#	t/s/o	**SOCKET A AND SOCKET B WRITE ENABLE/PROGRAM:** This signal has a single function with two semantics. In WE# semantics it is used by the host to gate Memory Write data. In PGM# semantics it is used for memory PC Cards that employ programmable memory technologies.
ARDY-BSY#/ IREQ# BRDY-BSY#/ IREQ#	in (ST)	**SOCKET A AND SOCKET B READY/BUSY OR INTERRUPT REQUEST:** This signal has two functions. When a memory card is in use, it has the *Ready/Busy* function. The signal is driven low by the memory PC Card to indicate that the card circuits are busy processing a previous write command. READY/BUSY# is set high when the memory PC Card is ready to accept a new data transfer command. When an I/O card is in use, it has the */IREQ#* interrupt request function. The card asserts IREQ# to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested. The status of this signal is stored in the Interface Status Register.
AWP/IOIS16# BWP/IOIS16#	in	**SOCKET A AND SOCKET B WRITE PROTECT OR CARD IS 16-BIT PORT:** This signal has two functions. For memory PC Cards, it has the *Write Protect* function that reflects the status of the Write Protect switch on the cards. If a memory PC Card switch is present, this signal is asserted by the card when the switch is enabled (write protection desired), and negated when the switch is disabled. If the memory PC Card has no Write Protect switch, the card connects this line to ground or V_{CC}, depending on the condition of the card memory. If the memory PC Card can always be written, the signal pin is connected to ground. If the memory PC Card is permanently Write Protected, the pin is connected to V_{CC}. The status of WP is stored in the Interface Status Register. However, Memory Write Cycle is not blocked by the xWP signal unless the Write Protect bit is set to 1 in the card memory offset Address High Byte Register. For I/O PC Cards, it has the *"Card is 16-Bit Port"* (IOIS16#) function. The signal is asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port that is addressed is capable of 16-bit accesses. This signal is used by the PPEC's data assembly/disassembly logic to determine the number of PCMCIA cycles required to complete data transfer (which from the PCI perspective can be 32-bits wide). If this signal is not asserted during a 16-bit I/O access, the PPEC generates two 8-bit data cycles to the even and odd bytes of the 16-bit word which is requested by the initial cycle. The status of this signal is stored in the Interface Status Register.
ARESET BRESET	t/s/o	**SOCKET A AND SOCKET B RESET:** This signal forces a hard reset to the PC card when asserted.

2.6 Socket A and B PCMCIA Signals (Continued)

Name	Type	Description
AWAIT# BWAIT#	in	**SOCKET A AND SOCKET B BUS CYCLE WAIT:** This signal is driven by the PC card to delay completion of a memory or I/O cycle that is in progress.
ABVD1/ STSCHG# BBVD1/ STSCHG#-	in	**SOCKET A AND SOCKET B BATTERY VOLTAGE DETECT 1/STATUS CHANGE-RING INDICATE:** This signal has three functions. As Battery Voltage Detect 1, it is driven by a memory PC Card that has a battery to indicate the condition of the battery as follows: • When both BVD1 and BVD2 are asserted (high) the battery is in good condition. • When BVD2 is negated while BVD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the memory PC Card is still assured. When BVD1 is negated (low) with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. As CHANGED STATUS (STSCHG#), it is held high the when the *Signal on Change* bit or the *Changed* bit in the Card Status Register on the PC Card is set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. The signal status is stored in the Interface Status Register.
ABVD2/ SPKR# BBVD2/ SPKR#	in	**SOCKET A AND SOCKET B BATTERY VOLTAGE DETECT OR DIGITAL AUDIO:** This signal has two functions. As Battery Voltage Detect, it is driven by a memory PC Card that has a battery to indicate the condition of the battery as follows: • When both BVD1 and BVD2 are asserted (high), the battery is in good condition. • When BVD2 is negated while BVD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the memory PC Card is still assured. When BVD1 is negated (low) with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. As Digital Audio, it is the input for a single amplitude (digital) audio waveform that is intended to drive the system's speaker via the SPKROUT# output pin on the system (host) interface. The status of the Battery Voltage Detect signal is stored in the Interface Status Register.

2.6 Socket A and B PCMCIA Signals (Continued)

Name	Type	Description
AVS1 BVS1	in	**SOCKET A AND SOCKET B CARD VOLTAGE CAPABILITY SENSE # 1:** The PPEC samples this signal and the corresponding xVS2 signal before applying V_{CC} power to the socket to determine the PC card input voltage capability. The signal must be connected to an external pull-up resistor. The status of this signal is stored in the Socket Power Configuration Register
AVS2 BVS2	in	**SOCKET A AND SOCKET B CARD VOLTAGE CAPABILITY SENSE # 1:** The PPEC samples this signal before configuring V_{CC} power to the socket to determine the PC card input voltage capability. If it is sampled high, 5V or 3.3V can be applied to the PC Card depending on the state of VS1. If it is sampled low, the PC Card required voltage is less than 3.3V, which the PPEC does not support. The status of this signal is available in the Socket Power Configuration Register.
ACD[2:1]# BCD[2:1]#	in (ST)	**SOCKET A AND SOCKET B CARD DETECT [2:1]:** These are two Card Detect signals that allow verification of proper card insertion. The signals are positioned at opposite ends of the connector to facilitate the detection process, and are connected to ground in the PC Card. The signals are therefore forced low whenever a card is placed in the socket. The status of the signals are available in the Interface Status Register. These signals have internal pull-up resistors.
EXTEN#	out	**EXTEN#:** This is used only in Mode 0, and only when the IDE Interface is not enabled. When the IDE is enabled in Mode 0, the EXTEN# signal pin is reserved. When low, EXTEN# enables external transceivers that de-couple the PCMCIA power latch from the Socket A CDATA[7:0] data bus signals to allow "hot" insertion and removal.
EXTDIR or GPO	out	**EXTERNAL TRANSCEIVER DIRECTION CONTROL OR GENERAL PURPOSE OUTPUT:** This signal has two functions, depending on whether the IDE Interface is enabled, as determined by the state of IDECFG at the end of the reset sequence. If the IDE Interface is disabled, the EXTDIR signal provides direction control for external transceivers. It is high during read cycles, and low during write cycles. If the IDE Interface is enabled, the GPO provides a general-purpose output. The GPO signal is directly controlled by bit 1 of the Global Security Control Register, and can be used to provide global PC Card LOCK function by controlling an external socket locking mechanism.

NOTE:
The PCMCIA Input Acknowledge (INPACK) signal is not supported by the PPEC.

2.6.1 MODE 1 (FOUR-SOCKET) CONFIGURATION SIGNALS

In Configuration Mode 0, two PC Card sockets are available. In Configuration Mode 1, four PC Card sockets are available, requiring more signals than Mode 0. Figure 5 shows the PPEC signal pinout for Mode 1.

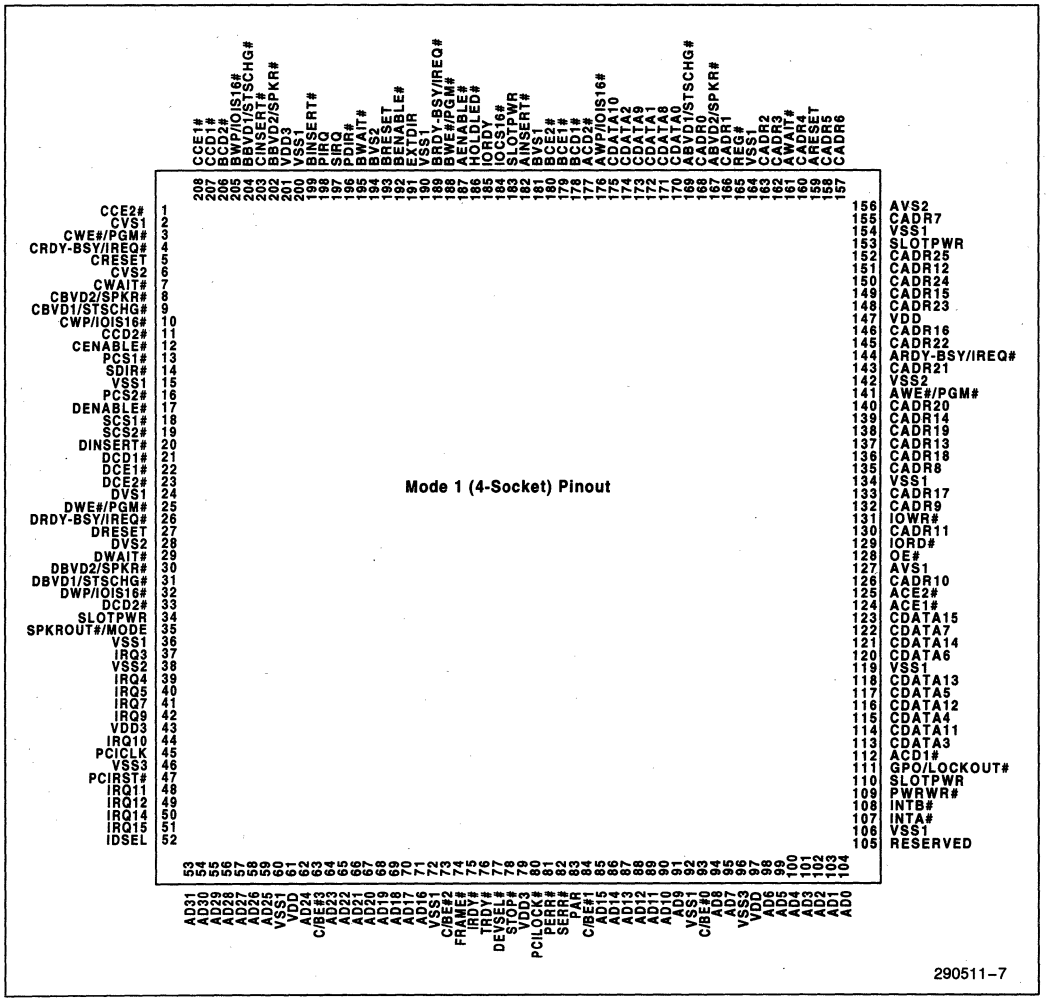


Figure 5. Mode 1 Pinout

Several signals and buses that are dedicated to Socket A in Mode 0 are common to all four sockets in Mode 1, as shown in Table 4.

Table 4. Mode 1 Common Signals

Mode 0 Socket A Signals	Mode 1 Common Socket Signals
ACDATA[15:0]	CDATA [15:0]
ACADR[25:0]	CADR[25:0]
AREG#	REG#
AOE#	OE#
AIORD#	IORD#
AIOWR#	IOWR#

This use of common signals significantly reduces the number of signals (and package pins) that would be required if each socket had it's own dedicated set of signals. It also releases the corresponding Socket B signal pins (BCDATA[15:0], BCADR[25:0], etc.) for use by the following socket-specific signals:

xCE1#	xVS1	xENABLE	xRDY-BUSY#/IREQ#
xCE2#	xVS2	xBVD1	xINSERT
xCD1#	xWP/IOIS16#	xBVD2	xWAIT#
xCD2#	xWE#/PGM#	xRESET	xINSERT#

XINSERT# and HOLDLED# (not listed) are Mode 1 signals that are not used in Mode 0.

All of the signals used in Mode 1 are described in the following table. The sockets have separate, but functionally identical sets of signals. Table 5 lists the PPEC pinout for the various configuration modes.

2.7 Socket A, B, C, and D PCMCIA Signals

Pin Name	Type	Description
CDATA[15:0]	t/s	**COMMON DATA BUS SIGNALS [15:0]:** This is a 16-bit data bus that is used for data transfer between the PPEC and the PCMCIA cards, and the PPEC and IDE drives when the IDE Interface is used. This bus is common to all of the sockets.
CADR[25:0]	t/s	**COMMON ADDRESS BUS SIGNALS [25:0]:** This is a 26-bit address bus that is used for addressing memory locations and attribute memory within a 64 MByte PCMCIA address range, and for addressing I/O within a 64 KByte PCMCIA address range. This bus is common to all of the sockets. If the IDE interface is used, CADR[2:0] transfer IDE register addresses during IDE accesses.
IORD#	t/s/o	**COMMON I/O READ:** The PPEC uses this active low signal and the REG# signal to gate I/O Read data from the PC Card. When low, IORD# gates I/O Read data from a memory PC Card only when the REG# signal is also asserted. This signal is common to all of the sockets.
IOWR#	t/s/o	**COMMON I/O WRITE:** The PPEC uses this active low signal and the REG# signal to gate I/O Write data to the PC Card. When low, IOWR# gates the I/O Write data to the PC Card only when the REG# signal is also asserted. This signal is common to all of the sockets.

2.7 Socket A, B, C, and D PCMCIA Signals (Continued)

Pin Name	Type	Description
REG	t/s/o	**COMMON ATTRIBUTE MEMORY SELECT:** This signal is inactive (high) during all normal accesses to main memory of PC Cards. I/O PC Cards do not respond to IORD# or IOWR# assertion when the AREG# signal is inactive. When it is active (low), access is limited to Attribute Memory when WE# or OE# are active, and to I/O ports when IORD# or IOWR# are active. Configurable memory PC Cards and I/O PC Cards contain configuration and status registers in the Attribute Memory Space. This signal is common to all of the sockets, and requires an external pull-up resistor to prevent the signal from floating during reset.
OE#	t/s/o	**COMMON OUTPUT ENABLE:** This is an active low signal that gates Memory Read data from memory PC Cards. It is common to all of the sockets.
EXTDIR	out	**EXTERNAL TRANSCEIVER DIRECTION CONTROL:** This signal is high during reads, and low during writes, and is used for both high bytes and low bytes. It defaults to write (low) at power-up. EXTDIR is used to control the drive direction of only the PCMCIA transceivers. Separate transceiver controls are provided for the IDE Interface.
ACE#[2:1] BCE#[2:1] CCE#[2:1] DCE#[2:1]	t/s/o	**SOCKET A-D CHIP ENABLE [2:1]:** These are active low signals that are driven by the PPEC when the socket is enabled. CE1# enables even bytes; CE2# enables odd bytes.
AWE#/PGM# BWE#/PGM# CWE#/PGM# DWE#/PGM#	t/s/o	**SOCKET A-D WRITE ENABLE/PROGRAM:** This signal has single function, but with two semantics. In WE# semantics, this signal is used by the host to gate Memory Write data. In PGM# semantics this signal is used for memory PC Cards that employ programmable memory technologies.
ARDY-BSY#/ IREQ BRDY-BSY#/ IREQ# CRDY-BSY#/ IREQ# DRDY-BSY#/ IREQ#	in(ST)	**SOCKET A-D READY/BUSY OR INTERRUPT REQUEST:** This signal has two functions, depending on the card in the socket. When a memory card is in use, it has the *Ready/Busy* function. The signal is driven low by the memory PC Card to indicate that the card circuits are busy processing a previous write command. READY/BUSY# is set high when memory PC Cards are ready to accept a new data transfer command. When an I/O card is in use, it has the */IREQ#* interrupt request function. The card asserts IREQ# to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested. The status of this signal is available in the Interface Status Register.

2.7 Socket A, B, C, and D PCMCIA Signals (Continued)

Pin Name	Type	Description
AWP/IOIS16# BWP/IOIS16# CWP/IOIS16# DWP/IOIS16#	in	**SOCKET A-D WRITE PROTECT OR CARD IS 16-BIT PORT:** This signal has two functions, depending on the type of card in the socket. For memory PC Cards, it has the *Write Protect* function that reflects the status of the Write Protect switch on the cards. If a memory PC Card switch is present, this signal is asserted by the card when the switch is enabled (write protection desired), and negated when the switch is disabled. If the memory PC Card has no Write Protect switch, the card connects this line to ground or to V_{CC}, depending on the condition of the card memory. If the memory PC Card can always be written, the signal pin is connected to ground. If the memory PC Card is permanently Write Protected, the pin is connected to V_{CC}. The status of WP is available in the Interface Status Register. However, Memory Write Cycle is not blocked by the WP signal unless the Write Protect bit is set to 1 in the card memory offset Address High Byte Register. For I/O PC Cards, it has the *"Card is 16-Bit Port"* (IOIS16#) function. The signal is asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port that is addressed is capable of 16-bit accesses. This signal is used by the PPEC's data assembly/disassembly logic to determine the number of PCMCIA cycles required to complete data transfers (which from the PCI perspective can be 32-bits wide). If this signal is not asserted during a 16-bit I/O access, the PPEC generates two 8-bit data cycles to the even and odd bytes of the 16-bit word which is requested by the initial cycle. The status of this signal is available in the Interface Status Register.
ARESET BRESET CRESET DRESET	t/s/o	**SOCKET A-D RESET:** This signal forces a hard reset to the PC card when asserted.
AWAIT# BWAIT# CWAIT# DWAIT#	in	**SOCKET A-D BUS CYCLE WAIT:** This signal is driven by the PC card to delay completion of a memory or I/O cycle that is in progress.

2.7 Socket A, B, C, and D PCMCIA Signals (Continued)

Name	Type	Description
ABVD1/ STSCHG# BBVD1/ STSCHG# CBVD1/ STSCHG# DBVD1/ STSCHG#	in	**SOCKET A-D BATTERY VOLTAGE DETECT 1/STATUS CHANGE:** This signal has three functions. As Battery Voltage Detect 1, it is driven by memory a PC Card that has a battery to indicate the condition of the battery, and is used with BVD2 as follows: • When both BVD1 and BVD2 are asserted (high), the battery is in good condition. • When BVD2 is negated while BVD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the memory PC Card is still assured. When BVD1 is negated (low) with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. As CHANGED STATUS (STSCHG#), it is held high the when the *Signal on Change* bit or the *Changed* bit in the Card Status Register on the PC Card is set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. The signal status is stored in the Interface Status Register.
ABVD2/ SPKR# BBVD2/ SPKR# CBVD2/ SPKR# DBVD2/ SPKR#	in	**SOCKET A-D BATTERY VOLTAGE DETECT OR DIGITAL AUDIO:** This signal has two functions. As Battery Voltage Detect, it is driven by a memory PC Card that has a battery to indicate the condition of the battery as follows: • When both BVD1 and BVD2 are asserted (high), the battery is in good condition. • When BVD2 is negated while BVD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the memory PC Card is still assured. When BVD1 is negated (low) with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. As Digital Audio, it is the input for a single amplitude (digital) audio waveform that is intended to drive the system's speaker via the SPKROUT# output pin on the system (host) interface. The status of the Battery Voltage Detect signal is stored in the Interface Status Register.
AVS1 BVS1 CVS1 DVS1	in	**SOCKET A-D CARD VOLTAGE CAPABILITY SENSE #1:** In Mode 1 partially buffered and non-buffered implementations, the PPEC samples this signal and the corresponding xVS2 signal before applying V_{CC} power to the socket to determine the PC card input voltage capability. The signal must be connected to an external pull-up resistor. The status of this signal is stored in the Socket Power Configuration Register.

2.7 Socket A, B, C, and D PCMCIA Signals (Continued)

Pin Name	Type	Description
AVS2 BVS2 CVS2 DVS2	in	**SOCKET A-D CARD VOLTAGE CAPABILITY SENSE #2:** In Mode 1 partially buffered and non-buffered implementations, the PPEC samples this signal and the corresponding xVS1 signal before applying V_{CC} power to the socket to determine the PC card input voltage capability. The signal must be connected to an external pull-up resistor. The status of this signal is stored in the Socket Power Configuration Register.
ACD[2:1]# BCD[2:1]# CCD[2:1]# DCD[2:1]#	in (ST)	**SOCKET A-D CARD DETECT [2:1]:** These are two Card Detect signals that allow verification of proper card insertion. The signals are positioned at opposite ends of the connector to facilitate the detection process, and are connected to ground in the PC Card. The signals are therefore forced low whenever a card is placed in the host socket. The status of the signals are stored in the Interface Status Register. ADC[2:1]# and BCD[2:1]# have internal pull-up resistors; CCD[2:1]# and DCD[2:1]# require external pull-up resistors.
AENABLE# BENABLE# CENABLE# DENABLE#	out	**SOCKET A-D BUFFER ENABLE:** This signal enables the PC Card socket buffers/ transceivers, and is controlled by the corresponding socket Power Control Register.
AINSERT# BINSERT# CINSERT# DINSERT#	in	**SOCKET A-D CARD INSERTION DETECT:** These signals are used in non-buffered or partially-buffered Mode 1 implementations to provide the PPEC with an early indication that a PC Card is being inserted into a PCMCIA socket. xINSERT# requires an external pull-up resistor, and is connected directly to one of the socket pins which is used normally (in fully buffered configuration) for V_{SS} connection. See the "PPEC Design Guide" for a detailed discussion of the use of these pins.
GPO/ LOCKOUT#	out	**GENERAL PURPOSE OUTPUT/LOCKOUT:** When bit 2 of the Global Security Control Register (GSCTRL) is set to 1, the GPO signal is enabled. When bit 2 of the GSTCTRL register is set to 0, the LOCKOUT# signal is enabled. The default value of bit 2 of the GSCTRL register is 0, enabling the LOCKOUT# signal. The GPO signal is directly controlled by bit 1 of the Global Security Control Register, and can be used to provide global PC Card LOCK function by controlling an external socket locking mechanism. LOCKOUT# is intended for systems that require a locking mechanism for the PCMCIA sockets. When the Lockout feature is selected and LOCKOUT# is active, the CD2# for each socket is treated as an Eject Request pin, and CD1# is internally routed to the circuitry that uses CD2#. This feature does not affect the routing of the CDx# signals to the interrupt generator or to the status registers, so a rising edge on either card detect still generates a Card Status Change interrupt. All other internal circuitry that uses CD1# and CD2#, such as the circuitry that tri-states the PCMCIA bus during a card removal, uses CD1# exclusively while the socket is locked.
HOLDLED#	out	**HOLD LED:** This signal is used to indicate a HOLD condition on the PCMCIA Bus during PC Card insertions and removals in non-buffered or partially-buffered Mode 1 implementations.

2.8 IDE Interface Signal

The PPEC supports two Fast Local Bus IDE interfaces (2 connectors with a total of 4 IDE drives) in both PCMCIA interface configuration modes. For clarity, the IDE interface pins are named and defined in this section independently of the basic signals with which they are multiplexed.

Most of the IDE interface signals are multiplexed with Socket A signals in Mode 0. Table 5 lists the signal pinout for Mode 0 with and without IDE selection.

In Mode 1, the IDE interface is independent of the PCMCIA interface with the exception of the data, address, write, and read strobes which are used for both interfaces as follows:

IDE Signal	PCMCIA Signal
DD[15:0]	CDATA[15:0]
DA[2:0]	CADR[2:0]
DIOW#	IOWR#
DIOR#	IORD#

Figure 2 shows the Mode 1 IDE signals.

2.9 IDE Interface Signals

Name	Type	Description
DD[15:0]	t/s	**DRIVE DATA BUS [15:0]:** This is an 8-bit or 16-bit bi-directional data bus that is located between the IDE interface controller, and the drive. The lower 8 bits are used for 8-bit transfers (registers, ECC bytes and, if the drive supports the Features Register, for 8-bit-only data transfers that may be selected). Data signals DD[7:0] can be used to support the IDE Hardware Configuration feature.
DA[2:0]	out	**DRIVE ADDRESS [2:0]:** This is a 3-bit binary coded address asserted by the host to access a drive register or the drive data port.
DIOR#	out	**DRIVE I/O READ STROBE:** The falling edge of DIOR# enables data from a register or from the drive's data port onto the IDE interface data bus. The rising edge of DIOR# latches data into the PPEC.
DIOW#	out	**DRIVE I/O WRITE STROBE:** The rising edge of DIOW# clocks data from the IDE interface data bus into a register or into the drive's data port.
IOCS16#	in	**I/O CHIP-SELECT 16-BIT:** The assertion of IOCS16# indicates to the PPEC that 16-bit data port has been addressed, and that the drive is prepared to send or receive a 16-bit data word.
IORDY	in	**I/O CHANNEL READY:** This signal is driven low by the currently accessed drive to extend the IDE transfer cycle when the drive is not ready to respond to a data transfer request. When IORDY is not negated, it is in a high impedance state from the perspective of the IDE drive(s). An external pull-up resistor must be provided on the cable side of the IDE Interface.
PCS1#	out	**PRIMARY IDE CHIP SELECT FOR DATA/COMMAND I/O ADDRESS RANGE:** This signal can be asserted only when IDEEN# is asserted (low) during IDE cycles to the appropriate address range as defined by the IDE Address Configuration Registers. It selects Command Block Registers of the drive(s) on the Primary IDE Interface.

2.9 IDE Interface Signals (Continued)

Name	Type	Description
PCS2#	out	**PRIMARY IDE CHIP SELECT FOR CONTROL/STATUS I/O ADDRESS RANGE:** This signal can be asserted only when IDEEN# is asserted (low) during IDE cycles to the appropriate address range as defined by the IDE Address Configuration Registers. It selects Control Block Registers of the drive(s) on the Primary IDE Interface.
SCS1#	out	**SECONDARY IDE CHIP SELECT FOR DATA/COMMAND I/O ADDRESS RANGE:** This signal can be asserted only when IDEEN# is asserted (low) during IDE cycles to the appropriate address range as defined by the IDE Address Configuration Registers. It selects Command Block Registers of the drive(s) on the Secondary IDE Interface.
SCS2#	out	**SECONDARY IDE CHIP SELECT FOR CONTROL/STATUS I/O ADDRESS RANGE:** This signal can be asserted only when IDEEN# is asserted (low) during IDE cycles to the appropriate address range as defined by the IDE Address Configuration Registers. It selects Control Block Registers of the drive(s) on the Secondary IDE Interface.
PIRQ	in	**PRIMARY IDE INTERFACE INTERRUPT REQUEST:** This signal is used by the IDE drives on the Primary connector to interrupt the host processor. It can be routed to any system interrupt, and can therefore be internally OR-ed (within the PPEC) with Secondary IDE interrupt.
SIRQ	in	**SECONDARY IDE INTERFACE INTERRUPT REQUEST:** This signal is used by the IDE drives on the Secondary connector to interrupt the host processor. It can be routed to any system interrupt, and can therefore be internally OR-ed (within the PPEC) with Primary IDE interrupt.
PDIR#	out	**PRIMARY IDE TRANSCEIVER DIRECTION CONTROL:** This signal controls the drive direction of the Primary IDE transceivers. The signal is asserted low only during read access to the Primary IDE registers. It is driven high all other times (during writes to Primary IDE registers, and when the Primary IDE is not accessed.
SDIR#	out	**SECONDARY IDE TRANSCEIVER DIRECTION CONTROL:** This signal controls the drive direction of the Secondary IDE transceivers. The signal is asserted low only during read access to the Secondary IDE registers. It is driven high all other times (during writes to Secondary IDE registers, and when the Secondary IDE is not accessed).

2.10 Pin Cross-Reference List

Table 5 lists the PPEC signals in package pin order according to mode. Note that the signal pinout changes in Mode 0 depending on whether the IDE interface is enabled. In Mode 1, the IDE interface is separate from the socket interfaces with the exception of the IDE DD[15:0] data bus, DA[2:0] address bus, DIOR# read strobe, and DIOW# write strobe which are multiplexed with the CDATA[15:0], CADR[2:0], IORD#, and IOWR# common socket signals.

Table 5. Pin Cross-Reference

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
1	CCE2#	BCADR9	BCADR9
2	CVS1	BCDATA13	BCDATA13
3	CWE#/PGM#	BCADR10	BCADR10
4	CRDY-BSY#/IREQ#	BCDATA4	BCDATA4
5	CRESET	BCADR11	BCADR11
6	CVS2	BCADR19	BCADR19
7	CWAIT#	BCDATA5	BCDATA5
8	CBVD2/SPKR#	BCDATA6	BCDATA6
9	CBVD1/STSCHG#	BCDATA7	BCDATA7
10	CWP/IOIS16#	BCDATA11	BCDATA11
11	CCD2#	BCDATA12	BCDATA12
12	CENABLE#	BCADR23	BCADR23
13	PCS1#	BCADR18	BCADR18
14	SDIR#	BCADR20	BCADR20
15	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
16	PCS2#	BCADR17	BCADR17
17	DENABLE#	BCADR24	BCADR24
18	SCS1#	BCADR15	BCADR15
19	SCS2#	BCADR16	BCADR16
20	DINSERT#	BCADR25	BCADR25
21	DCD1#	BCDATA14	BCDATA14
22	DCE1#	BCADR7	BCADR7
23	DCE2#	BCADR6	BCADR6
24	DVS1	BCDATA10	BCDATA10
25	DWE#/PGM#	BCADR5	BCADR5
26	DRDY-BSY#/IREQ#	BCDATA15	BCDATA15
27	DRESET	BCADR4	BCADR4
28	DVS2	BCADR12	BCADR12

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
29	DWAIT#	BCDATA0	BCDATA0
30	DBVD2/SPKR#	BCDATA1	BCDATA1
31	DBVD1/STSCHG#	BCDATA2	BCDATA2
32	DWP/IOIS16#	BCDATA8	BCDATA8
33	DCD2#	BCDATA9	BCDATA9
34	SLOTPWR (5V or 3.3V)	SLOTPWR (5V or 3.3V)	SLOTPWR (5V or 3.3V)
35	SPKROUT#/MODE	SPKROUT#/MODE	SPKROUT#/MODE
36	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
37	IRQ3	IRQ3	IRQ3
38	V_{SS} (CORE)	V_{SS} (CORE)	V_{SS} (CORE)
39	IRQ4	IRQ4	IRQ4
40	IRQ5	IRQ5	IRQ5
41	IRQ7	IRQ7	IRQ7
42	IRQ9	IRQ9	IRQ9
43	VDD (5V)	VDD (5V)	VDD (5V)
44	IRQ10	IRQ10	IRQ10
45	PCICLK	PCICLK	PCICLK
46	V_{SS} (INPUTS)	V_{SS} (INPUTS)	V_{SS} (INPUTS)
47	PCIRST#	PCIRST#	PCIRST#
48	IRQ11	IRQ11	IRQ11
49	IRQ12	IRQ12	IRQ12
50	IRQ14	IRQ14	IRQ14
51	IRQ15	IRQ15	IRQ15
52	IDSEL	IDSEL	IDSEL
53	AD31	AD31	AD31
54	AD30	AD30	AD30
55	AD29	AD29	AD29
56	AD28	AD28	AD28
57	AD27	AD27	AD27
58	AD26	AD26	AD26
59	AD25	AD25	AD25
60	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
61	VDD (5V)	VDD (5V)	VDD (5V)
62	AD24	AD24	AD24
63	C/BE3	C/BE3	C/BE3
64	AD23	AD23	AD23
65	AD22	AD22	AD22
66	AD21	AD21	AD21
67	AD20	AD20	AD20
68	AD19	AD19	AD19
69	AD18	AD18	AD18
70	AD17	AD17	AD17
71	AD16	AD16	AD16
72	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
73	C/BE2	C/BE2	C/BE2
74	FRAME#	FRAME#	FRAME#
75	IRDY#	IRDY#	IRDY#
76	TRDY#	TRDY#	TRDY#
77	DEVSEL#	DEVSEL#	DEVSEL#
78	STOP#	STOP#	STOP#
79	VDD (5V)	VDD (5V)	VDD (5V)
80	PCILOCK#	PCILOCK#	PCILOCK#
81	PERR#	PERR#	PERR#
82	SERR#	SERR#	SERR#
83	PAR	PAR	PAR
84	C/BE1	C/BE1	C/BE1
85	AD15	AD15	AD15
86	AD14	AD14	AD14
87	AD13	AD13	AD13
88	AD12	AD12	AD12
89	AD11	AD11	AD11
90	AD10	AD10	AD10
91	AD9	AD9	AD9
92	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
93	C/BE0	C/BE0	C/BE0

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
94	AD8	AD8	AD8
95	AD7	AD7	AD7
96	V_{SS} (INPUTS)	V_{SS} (INPUTS)	V_{SS} (INPUTS)
97	VDD (5V)	VDD (5V)	VDD (5V)
98	AD6	AD6	AD6
99	AD5	AD5	AD5
100	AD4	AD4	AD4
101	AD3	AD3	AD3
102	AD2	AD2	AD2
103	AD1	AD1	AD1
104	AD0	AD0	AD0
105	RESERVED	EXTEN#	RESERVED
106	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
107	INTA#	INTA#	INTA#
108	INTB#	INTB#	INTB#
109	PWRWR#	PWRWR#	PWRWR#
110	SLOTPWR (5V or 3.3V)	SLOTPWR (5V or 3.3V)	SLOTPWR (5V or 3.3V)
111	GPO/LOCKOUT#	EXTDIR	GPO
112	ACD1#	ACD1#	RESERVED
113	CDATA3	ACDATA3	DD3
114	CDATA11	ACDATA11	DD11
115	CDATA4	ACDATA4	DD4
116	CDATA12	ACDATA12	DD12
117	CDATA5	ACDATA5	DD5
118	CDATA13	ACDATA13	DD13
119	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
120	CDATA6	ACDATA6	DD6
121	CDATA14	ACDATA14	DD14
122	CDATA7	ACDATA7	DD7
123	CDATA15	ACDATA15	DD15
124	ACE1#	ACE1#	RESERVED
125	ACE2#	ACE2#	RESERVED
126	CADR10	ACADR10	PCS2#
127	AVS1	AVS1	RESERVED

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
128	OE#	AOE#	PDIR#
129	IORD#	AIORD#	DIOR#
130	CADR11	ACADR11	PCS1#
131	IOWR#	AIOWR#	DIOW#
132	CADR9	ACADR9	RESERVED
133	CADR17	ACADR17	RESERVED
134	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
135	CADR8	ACADR8	RESERVED
136	CADR18	ACADR18	RESERVED
137	CADR13	ACADR13	SCS1#
138	CADR19	ACADR19	RESERVED
139	CADR14	ACADR14	RESERVED
140	CADR20	ACADR20	RESERVED
141	AWE#/PGM#	AWE#/PGM#	RESERVED
142	V_{SS} (CORE)	V_{SS} (CORE)	V_{SS} (CORE)
143	CADR21	ACADR21	RESERVED
144	ARDY-BSY#/IREQ#	ARDY-BSY#/IREQ#	IORDY
145	CADR22	ACADR22	RESERVED
146	CADR16	ACADR16	RESERVED
147	VDD (5V)	VDD (5V)	VDD (5V)
148	CADR23	ACADR23	RESERVED
149	CADR15	ACADR15	SDIR#
150	CADR24	ACADR24	PIRQ
151	CADR12	ACADR12	SCS2#
152	CADR25	ACADR25	SIRQ
153	SLOTPWR (5V or 3.3V)	SLOTPWR (5V or 3.3V)	SLOTPWR (5V or 3.3V)
154	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
155	CADR7	ACADR7	RESERVED
156	AVS2	AVS2	RESERVED
157	CADR6	ACADR6	RESERVED
158	CADR5	ACADR5	RESERVED
159	ARESET	ARESET	RESERVED
160	CADR4	ACADR4	RESERVED

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
161	AWAIT#	AWAIT#	RESERVED
162	CADR3	ACADR3	RESERVED
163	CADR2	ACADR2	DA2
164	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
165	REG#	AREG#/IDECFG	AREG#/IDECFG
166	CADR1	ACADR1	DA1
167	ABVD2/SPKR#	ABVD2/SPKR#	RESERVED
168	CADR0	ACADR0	DA0
169	ABVD1/STSCHG#	ABVD1/STSCHG#	RESERVED
170	CDATA0	ACDATA0	DD0
171	CDATA8	ACDATA8	DD8
172	CDATA1	ACDATA1	DD1
173	CDATA9	ACDATA9	DD9
174	CDATA2	ACDATA2	DD2
175	CDATA10	ACDATA10	DD10
176	AWP/IOIS16#	AWP/IOIS16#	IOCS16#
177	ACD2#	ACD2#	RESERVED
178	BCD1#	BCD1#	BCD1#
179	BCE1#	BCE1#	BCE1#
180	BCE2#	BCE2#	BCE2#
181	BVS1	BVS1	BVS1
182	AINSERT#	BOE#	BOE#
183	SLOTPWR (5V or 3.3V)	SLOTPWR (5V or 3.3V)	SLOTPWR (5V or 3.3V)
184	IOCS16#	BIORD#	BIORD#
185	IORDY	BIOWR#	BIOWR#
186	HOLDLED#	BCADR13	BCADR13
187	AENABLE#	BCADR14	BCADR14
188	BWE#/PGM#	BWE#/PGM#	BWE#/PGM#
189	BRDY-BSY#/IREQ#	BRDY-BSY#/IREQ#	BRDY-BSY#/IREQ#
190	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
191	EXTDIR	BCADR21	BCADR21
192	BENABLE#	BCADR22	BCADR22
193	BRESET	BRESET	BRESET

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
194	BVS2	BVS2	BVS2
195	BWAIT#	BWAIT#	BWAIT#
196	PDIR#	BCADR3	BCADR3
197	SIRQ	BCADR2	BCADR2
198	PIRQ	BCADR1	BCADR1
199	BINSERT#	BREG#	BREG#
200	V_{SS} (INPUTS)	V_{SS} (INPUTS)	V_{SS} (INPUTS)
201	VDD (5V)	VDD (5V)	VDD (5V)
202	BBVD2/SPKR#	BBVD2/SPKR#	BBVD2/SPKR#
203	CINSERT#	BCADR0	BCADR0
204	BBVD1/STSCHG#	BBVD1/STSCHG#	BBVD1/STSCHG#
205	BWP/IOIS16#	BWP/IOIS16#	BWP/IOIS16#
206	BCD2#	BCD2#	BCD2#
207	CCD1#	BCDATA3	BCDATA3
208	CCE[1]#	BCADR[8]	BCADR[8]

3.0 PPEC REGISTER DESCRIPTIONS

The PPEC registers consist of PCI configuration registers, and PCMCIA Socket Configuration registers. The PCI configuration registers are classified as PCI-PCMCIA Bridge PCI Configuration Registers, or PCI-IDE Interface PCI Configuration Registers. The PCMCIA Socket Configuration registers are classified as General Setup Registers, Interrupt Registers, I/O Mapping Control Registers, or Memory Mapping Control Registers.

Several PPEC registers contain reserved bits or fields labeled "Reserved" that must be handled correctly by software. During reads, software must mask the reserved bits as undefined. During writes, software must ensure that the values of the reserved bits are preserved by first reading the reserved bits, merging the reserved bit values with the new values of the non-reserved bits, then writing the data.

Several bits are described as "not implemented" in the register descriptions. These bits correspond to PCI-defined functions that are not implemented in the PPEC, but are described to facilitate tracking of PCI-supported features.

3.1 PCI Configuration Registers

The PPEC supports PCI-PCMCIA Bridge and PCI-IDE Interface functions. These functions can be configured independently with two sets of PCI configuration registers in compliance with the PCI Local Bus Specification Revision 2.0. The two sets of configuration registers are accessed through a mechanism defined for multi-functional PCI devices. The PCI-PCMCIA Bridge configuration registers are addressed as a function #0 with AD[10:8] as shown in the following table, and the PCI-IDE Interface configuration registers are addressed as a function #1. Attempted access of a register in the 2–7 function range results in no response by the PPEC and a PCI-master abort.

Functions are accessed by AD[10:8] during the address phase of the configuration cycle as follows:

AD[10:8]	PPEC PCI Function Addressed
000	#0: PCI-PCMCIA Bridge
001	#1: PCI-IDE Interface
010 through 111	none (Reserved)

Note that the control bits for certain PCI functions that are defined in the PCI Specification but not used in the PPEC are shown in the configuration registers, but are described as "not implemented".

Table 6. PCI-PCMCIA Bridge PCI Configuration Registers

Address Offset	Mnemonic	Register Name	Access
00-01h	VENID	Vendor ID	RO
02-03h	DEVID	Device ID	RO
04-05h	PCICMD	PCI Command	R/W
06-07h	PCISTS	PCI Status	RO
08h	REVID	Revision ID	RO
09-0Bh	CCODE	Class Code (CCPIB and CCCB)	RO
0C-0Dh		Reserved	
0Eh	HTYPE	Header Type	RO
0Fh		Reserved	
10-13h	PBBA	PCI-PCMCIA Bridge Base Address	R/W
14-3Bh		Reserved	
3Ch	INTLIN	Interrupt Line	R/W
3Dh	INTPIN	Interrupt Pin	R/W
3E-3Fh		Reserved	
40h	PCICON	PCI Configuration Control	R/W
41-4Fh		Reserved	
50h	PPIRR	PCMCIA-PCI Interrupt Routing Register	
51-FFh		Reserved	

3.1.1 PPEC FUNCTION #0—PCI-PCMCIA BRIDGE PCI CONFIGURATION REGISTERS

The PCI-PCMCIA Bridge PCI Configuration Registers, listed in Table 6, are 8-bit, 16-bit, and 32-bit registers. Particular bytes within 16-bit and 32-bit register are selected with byte enables. Reserved registers and bits are reserved for future use, and writing to them has no effect. When writing to a register with reserved bits, the reserved bits should be read first, then properly masked and written back to prevent future software incompatibility.

3.1.1.1 VENID—Vendor ID

Register Offset: 00h
Default Value: 8086h
Access: Read Only
Size: 16 bits

This is a unique 16 bit value assigned to a vendor that, together with the Device ID, uniquely identifies each PCI device. Writes to this register have no effect.

Bits[15:0]: Vendor Identification
This is a 16-bit value assigned to Intel.

3.1.1.2 DEVID—Device ID

Register Offset: 02h
Default Value: 1221h
Access: Read Only
Size: 16 bits

This is a unique 16 bit value that is assigned to the PCI-PCMCIA Bridge function. The Device ID, together with the Vendor ID, uniquely identifies each PCI device. Writes to this register have no effect.

Bits[15:0]: Device Identification
This value identifies the PCI-PCMCIA Bridge function.

3.1.1.3 PCICMD—PCI Command

Register Offset: 04h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This 16 bit register contains PCI control information.

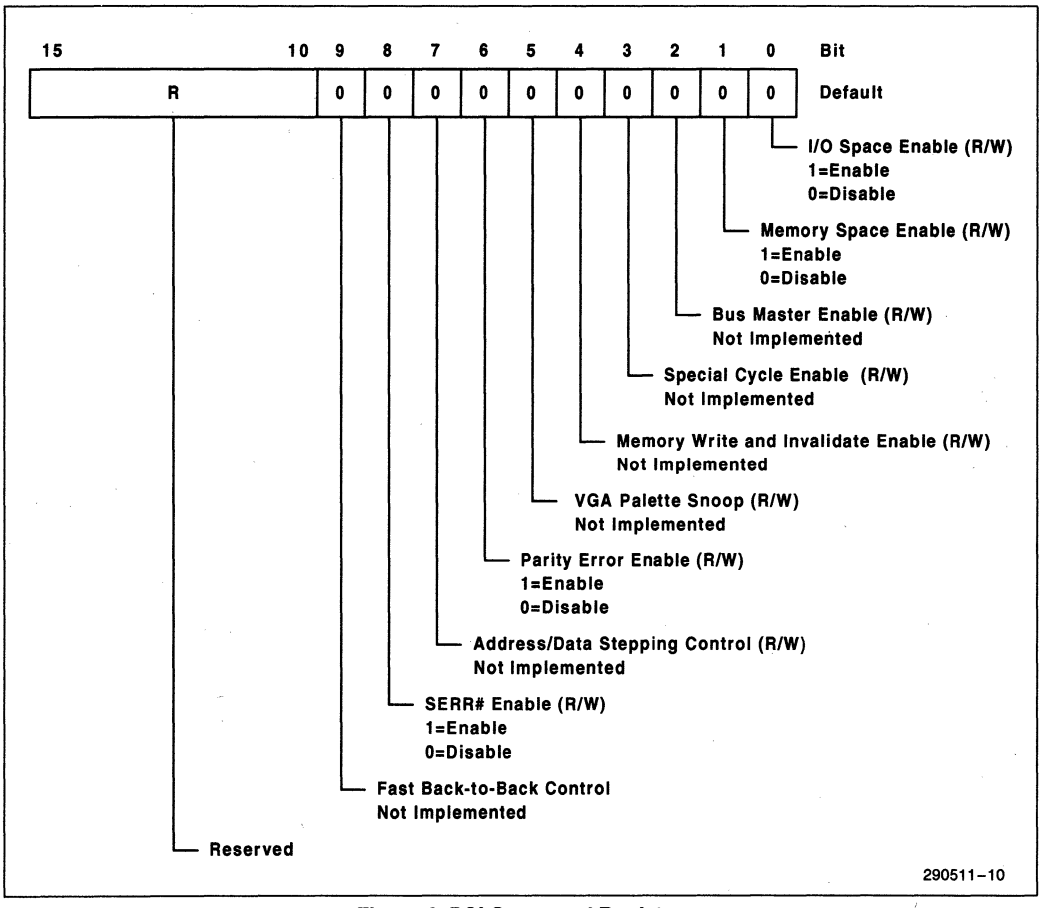


Figure 6. PCI Command Register

Bits[15:10]: Reserved

Bit 9: Fast Back-to-Back Control
This control function can be used only by a PCI master and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 8: SERR# Enable
When this bit is set to 1, the PPEC asserts SERR# when it detects a parity error during an address phase, and when it detects an X.X PC Card in Mode 1, partially-buffered implementations. When this bit is set to 0, SERR# is not asserted for any reason. Reset sets the bit to 0.

Bit 7: Address/Data Stepping Control
This control function can be used only by a PCI master and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 6: Parity Error Enable
This bit controls PPEC response to PCI data parity errors. When this bit is set to 1, the PPEC activates PERR# when it detects a parity error during a data phase. When this bit is set to 0, the PPEC ignores parity errors. Reset sets the bit to 0 and disables data parity checking.

Bit 5: VGA Palette Snoop
This bit is intended only for specific control of PCI-based VGA devices, and is not applicable to the PPEC. The bit is not implemented, and always reads "0".

Bit 4: Memory Write and Invalidate Enable
This control function can be used only by the PCI master, and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 3: Special Cycle Enable
This bit is intended to enable response to supported special cycles. Since the PPEC does not respond to any special cycle, the bit is not implemented and always reads "0".

Bit 2: Bus Master Enable
This bit is intended to enable mastership of the PCI. Since the PPEC cannot be a PCI master, the bit is not implemented and always reads "0".

Bit 1: Memory Space Enable
This bit enables the PPEC to accept PCI-originated memory cycles. When the bit is set to 0, the PPEC does not respond to PCI memory cycles to PCMCIA cards, and the PPEC DEVSEL# logic is inhibited during the memory cycles.

Bit 0: I/O Space Enable
This bit enables the PCI-PCMCIA Bridge to accept PCI-originated I/O cycles. When the bit is set to 0, the PPEC does not respond to PCI master I/O cycles, and the PPEC DEVSEL# logic is inhibited during the I/O cycles.

3.1.1.4 PCISTS—PCI Status

Register Offset:	06h
Default Value:	0480h
Access:	Read Only (*see description)
Size:	16-bits

This 16-bit register is used to record status information for PCI bus-related events. Reads to this register behave normally. Writing bits 11, 14, and 15 to 1 set the bits to 0. The other register bits cannot be written.

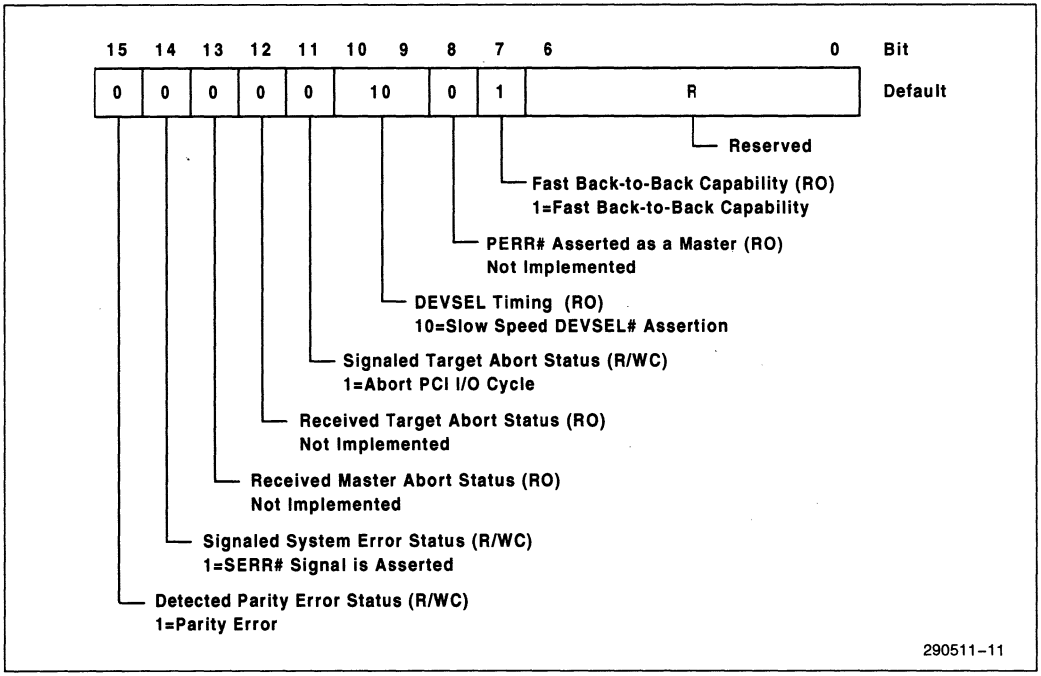


Figure 7. PCI Status Register

Bits 15: Detected Parity Error Status
This bit is to be set whenever the 82092AA as a target detects a parity error during the data phase, even if parity error handling is disabled (as controlled by bit 6 in the *PCI Command* register). DEFAULT=0.

Bit 14: Signaled System Error Status
This bit is used to indicate that PCI device asserted SERR# signal. The 82092AA will assert this bit whenever it generates address phase parity error via SERR# pin. DEFAULT=0.

Bit 13: Received Master Abort Status (not applicable)
Since this control function can be used only by the PCI master it is not implemented and the bit is always read as a "0" (disabled).

Bit 12: Received Target Abort Status (not applicable)
Received Target Abort Sataus by the PCI master. Since this control function can be used only by the PCI master it is not implemented and the bit is always read as a "0" (disabled).

Bit 11: Signaled Target Abort Status
This bit is to be set by PCI target devices when they generate a Target Abort.

The 82092AA generates Target Abort in the case when it is the target of the PCI I/O cycle and address/byte-enable combination is invalid. More details are provided in Section 1.6.1.5, Transaction Termination.

Bit[10:9]: DEVSEL Timing
These read-only bits encode the timing of DEVSEL# when 82092AA responds as a Target. PCI Specification defines three allowable timings for assertion of DEVSEL#: 00b=fast, 01b=medium, and 10b=slow (11b is reserved). These bits are Read-Only and they indicate the slowest time that a device asserts DEVSEL# for any bus command except *Configuration Read* and *Configuration Write*. The 82092AA PCI-IDE function implements medium speed DEVSEL# timing and therefore these bits contain value 01b.

Bit 8: PERR# Asserted as a Master
This control function can be used only by a PCI master. Therefore this control function is not implemented and the bit will be always read as a "0" (disabled).

Bit 7: Fast Back-to-Back Capability
This read-only bit indicates PCI target capability to support fast back-to-back cycles. The 82092AA can support this type of cycle originated by any PCI master and therefore this bit is set to "1". DEFAULT=1.

Bit[6:0]: Reserved

3.1.1.5 REVID—Revision ID

Register Offset:	08h
Default Value:	01h
Access:	Read Only
Size:	8 bits

This 8 bit register contains device revision information. Writes to this register have no effect.

Bits[7:0]: Revision Identification
This is the revision level of the PPEC. The initial PPEC revision level is 01h.

3.1.1.6 CCPIB—Class Code-Programming Interface Byte

Register Offset:	09h
Default Value:	00h
Access:	Read Only
Size:	8 bits

This 8 bit register contains device Programming Interface information related to the Class Code bytes located at 0Ah offset. Writes to this register have no effect.

Bits[7:0]: Programming Interface
There are no specific register-level programming interfaces defined for this Class Code (indicated by register CCCB). Therefore, the value of this field is 0.

3.1.1.7 CCCB—Class Code-Class Code Bytes

Register Offset:	0Ah
Default Value:	0605h
Access:	Read Only
Size:	16 bits

This 16-bit register contains device Class Code bytes in the following format: [BASE CLASS][SUB-CLASS]. Writes to this register have no effect.

Bits[15:8]: Base Class
The value 06h in this field identifies the function class as a *bus bridge*.

Bits[7:0]: Sub-Class
The value 05h in this field identifies the function sub-class as a *PCMCIA bridge*.

3.1.1.8 HTYPE—Header Type

Register Offset: 0Eh
Default Value: 80h
Access: Read Only
Size: 8 bits

This register indicates whether or not the device contains multiple functions, and identifies the layout of bytes 10h through 3Fh in configuration space. Bit 7 indicates a multi-functional device when set to 1. Bits[6:0] specify layout of bytes 10h-3Fh. The PPEC uses layout type #0 as defined in the PCI specification. Writes to this register have no effect.

Bit 7: Multifunction Indicator
This bit is set to 1 to indicate that the PPEC is a multifunctional device.

Bits[6:0]: Byte Layout
This field specifies layout type "0" for bytes 10-3Fh, as defined in the PCI specification.

3.1.1.9 PBBA—PCI-PCMCIA Bridge Base Address

Register Offset: 10h
Default value: 0000 0001h
Access: Read/Write
Size: 32 bits

This register determines the starting address of the PCMCIA Index/Data Socket Configuration registers mapped in the system I/O space. PCMCIA Index/Data Socket Configuration registers allow indirect access to the block of PCMCIA socket control registers which consists of 256 8-bit locations divided into four sub-blocks, each containing 64 8-bit configuration registers that control the operations of particular PCMCIA socket.

PCMCIA Index/Data Registers can be mapped anywhere in 4 GByte I/O space on a Dword boundary. They provide 82365SL-compatible windowing access to the PCMCIA socket control/configuration registers. The 82365SL-compatible PCMCIA configuration registers access via Index/Data registers implies that Index is an 8-bit I/O port located at [BASEADDRESS], and Data is an 8-bit I/O port located at [BASEADDRESS] + 1.

Bits[31:2]: Base Address
This value determines the starting address of the PCMCIA Index/Data Socket Configuration registers mapped in the system I/O space.

Bit 1: Reserved

Bit 0: I/O Space Indicator
This bit is set to 1 to indicate I/O space.

NOTE:
Accesses to locations BASEADDRESS + 2 and BASEADDRESS + 3 are not permitted. These accesses may cause errors that are not reported to the system.

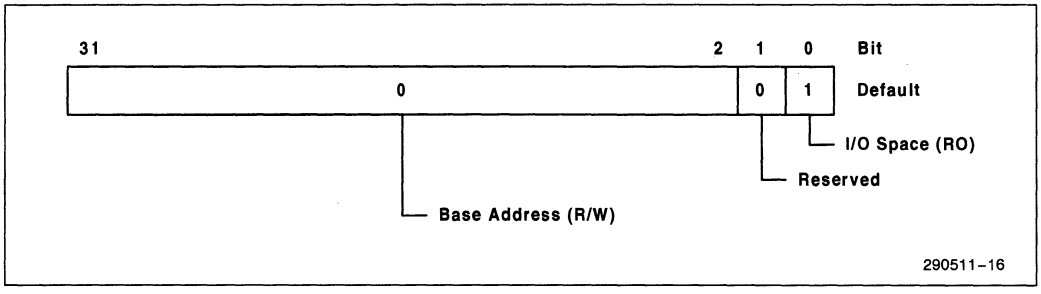


Figure 8. PCI-PCMCIA Bridge Base Address Register

3.1.1.10 INTLIN—Interrupt Line

Register Offset: 3Ch
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register is used to communicate interrupt line routing information. BIOS software must initialize this register during system configuration. The value in this register identifies the interrupt request level of the system interrupt controller(s) to which the PPEC interrupt pin is connected. Device drivers and the operating system can use this information to determine priority and vector information. The value in this register is system architecture specific.

Bits[7:0]: Interrupt Line Identification
The value in this field identifies the interrupt request level of the system interrupt controller(s) to which the PPEC interrupt pin is connected.

NOTE:
The PCI-PCMCIA Bridge can connect to system interrupt controllers in two different ways:

a. via a single PCI interrupt signal line INTA# that requires additional routing (system specific).
b. via 10 direct system interrupt signals.

Mode (b) is provided to allow PCMCIA software that requires "ISA compatibility" (i.e., non-shareable IRQ handlers that require specific IRQ level) to run without modifications on Intel-architecture platforms with the PPEC as a PCI-PCMCIA Bridge. In this case, the PCI interrupt scheme is not used, but the PCMCIA Card interrupts (as well as the Card Status Change interrupt) are configured to connect directly to specific system IRQ lines. The PCI Interrupt Line and the PCMCIA-PCI Interrupt Routing Register (PPIRR) remain in default state 0. Designs that are not dependent on this type of software "compatibility" can use PCI interrupt scheme using mechanism (a).

3.1.1.11 INTPIN—Interrupt Pin

Register Offset: 3Dh
Default Value: 01h
Access: Read Only
Size: 8 bits

This register is used to indicate that the PCI-PCMCIA Bridge uses the INTA# PCI Interrupt Pin for signaling PC Card interrupts (Card Status Change and/or I/O Interrupts). The PCMCIA-PCI Interrupt Routing Register (PPIRR, located at offset 50h) is used to enable (per PC Card) signaling of interrupts using the PCI interrupt scheme.

Bits[7:0]: Interrupt Pin Selection
The value in this field, 01h, identifies the interrupt pin used by the PPEC's PCI-PCMCIA Bridge function as INTA#.

3.1.1.12 PCICON—PCI Configuration Control

Register Offset: 40h
Default Value: XXh
Access: Read/Write
Size: 8 bits

The default is determined by the PCMCIA and IDE configurations as defined in the PCMCIA Interface description in this document.

Bit 0: PCICLK Configuration
This read/write bit defines the system PCICLK frequency. It must be initialized by the system software to provide optimized timing for 25 MHz or 33 MHz. as follows:

1 = 25 MHz PCICLK
0 = 33 MHz PCICLK

Bits[7:6]: Reserved

Bit 5: Enhanced PCMCIA Timing Mode Enable
When set to 1, this bit enables enhanced PCMCIA timing mode. When set to 0, the PPEC timing is 82365SL compatible manner as far as timing control based on the SMSTH0 PCMCIA memory window control register is concerned. The slowest 365 timing is selected and all writes to the enhanced timing mode bits are ignored. When set to 1, the enhanced timing control is enabled.

Bit 4: Global PCMCIA Read-Prefetch Buffering Enable
This bit globally enables PCI to PCMCIA data buffering for Prefetch Read operations when set to 1. When set to 0, buffered operations are disabled.

Bit 3: Global PCMCIA Post-Write Buffering Enable
This bit globally enables PCI to PCMCIA data buffering for Post Write operations when set to 1. When set to 0, buffered operations are disabled.

This register provides read-only configuration information and data buffering enable/disable function.

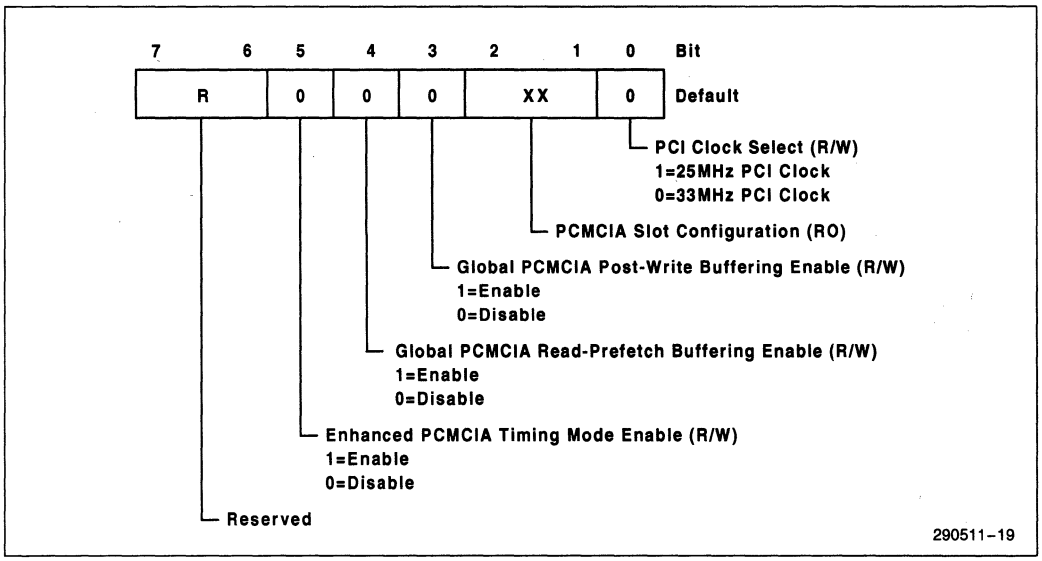


Figure 9. PCI Configuration Control Register

Bits[2:1]: PCMCIA Socket Configuration
These two read-only bits define the PCMCIA socket configuration (i.e., the number of supported sockets based on PCMCIA interface and IDE interface pin configuration) as follows:

Bit2	Bit1	Configuration
0	0	2 PCMCIA Sockets (2-Socket Mode)
0	1	1 PCMCIA Socket And IDE (2-Socket Mode)
1	X	4 PCMCIA Sockets (4-Socket Mode)

3.1.1.13 PPIRR—PCMCIA-PCI Interrupt Routing Register

Register Offset: 50h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register allows mapping of PCMCIA interrupts to either ISA interrupts, or PCI interrupts. Two interrupts, Card Status Interrupt and Card I/O Interrupt, can be generated and independently routed for each socket. When a register bit is set to 0, the corresponding interrupt is routed via one of the 10 system interrupt lines (ISA mechanism) as specified in the Interrupt and General Control Register and the Card Status Change Interrupt Configuration Register. When a bit is set to 1, the corresponding interrupt is routed via INTA# (PCI mechanism).

Bit 7: Socket D Card I/O IRQ Interrupt Routing
This bit selects Card I/O Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 6: Socket D Card Status Change Interrupt Routing
This bit selects Card Status Change Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 5: Socket C Card I/O IRQ Interrupt Routing
This bit selects Card I/O Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 4: Socket C Card Status Change Interrupt Routing
This bit selects Card Status Change Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 3: Socket B Card I/O IRQ Interrupt Routing
This bit selects Card I/O Interrupt routing via the PCI mechanism, or the ISA mechanism.

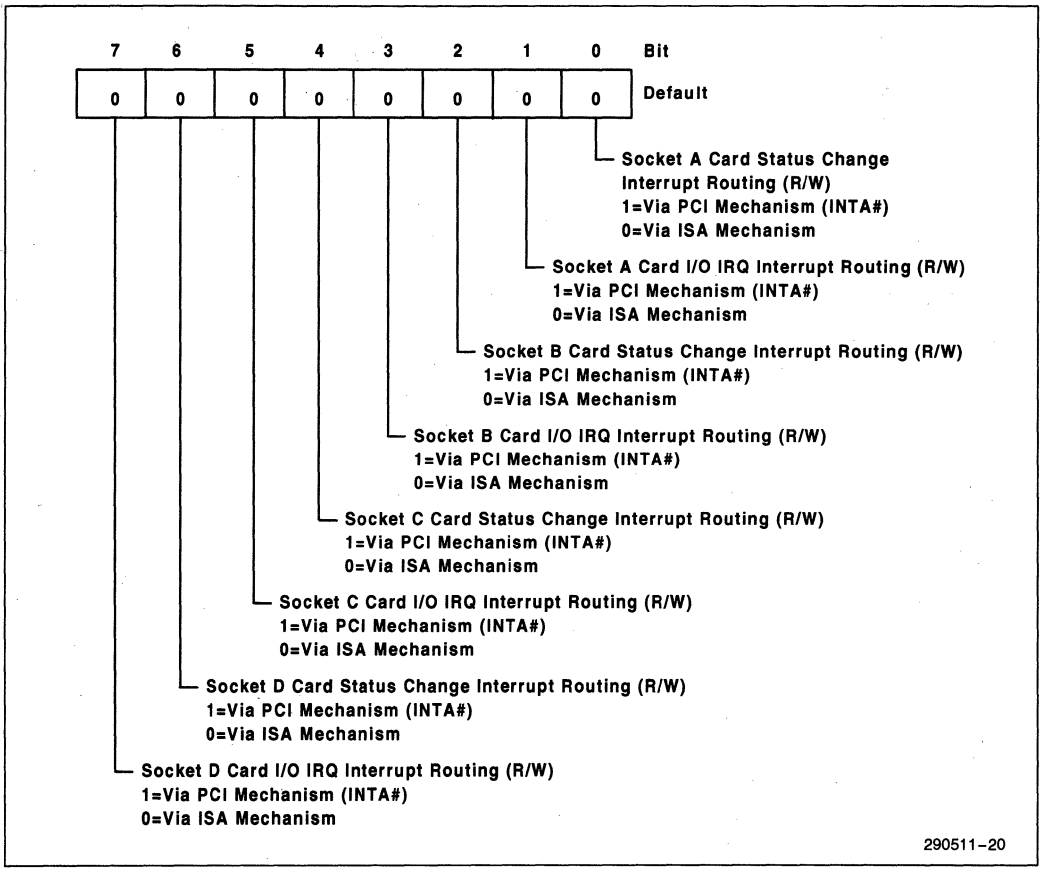


Figure 10. PCMCIA Interrupt Routing Register

Bit 2: Socket B Card Status Change Interrupt Routing
This bit selects Card Status Change Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 1: Socket A Card I/O IRQ Interrupt Routing
This bit selects Card I/O Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 0: Socket A Card Status Change Interrupt Routing
This bit selects Card Status Change Interrupt routing via the PCI mechanism, or the ISA mechanism.

3.1.2 PPEC Function #1—PCI-IDE Interface PCI Configuration Registers

The PCI-PCMCIA Bridge PCI Configuration Registers, listed in Table 7, are 8-bit, 16-bit, and 32-bit registers. Particular bytes within 16-bit and 32-bit registers are selected with byte enables. Reserved registers and bits are reserved for future use, and writing to them has no effect. When writing to a register with reserved bits, the reserved bits should be read first, then properly masked and written back to prevent future software incompatibility.

Table 7. PCI-IDE Interface PCI Configuration Registers

Address Offset	Mnemonic	Register Name	Access
00-01h	VENID	Vendor ID	RO
02-03h	DEVID	Device ID	RO
04-05h	PCICMD	PCI Command	R/W
06-07h	PCISTS	PCI Status	RO
08h	REVID	Revision ID	RO
09-0Bh	CCODE	Class Code (CCPIB and CCCB)	RO
0C-0Dh		Reserved	
0Eh	HTYPE	Header Type	RO
0Fh		Reserved	
10-13h	PDCBA	IDE Base Address #0—Primary IDE Data/Command	R/W
14-17h	PCSBA	IDE Base Address #1—Primary IDE Control/Status	R/W
18-1Bh	SDCBA	IDE Base Address #2—Secondary IDE Data/Command	R/W
1C-1Fh	SCSBA	IDE Base Address #3—Secondary IDE Control/Status	R/W
20-3Bh		Reserved	
3Ch	INTLIN	Interrupt Line	R/W
3Dh	INTPIN	Interrupt Pin	R/W
3E-3Fh		Reserved	
40h	PCICON	PCI Configuration Control	R/W
41-43h		Reserved	
44h	PIDECFG	Power-On IDE Configuration	R/W
45-47h		Reserved	
48-49h	PIDETC	Primary IDE Timing Control	R/W
4A-4Bh	SIDETC	Secondary IDE Timing Control	R/W
4Ch	IIIRR	IDE-ISA Interrupt Routing Register	R/W
4Dh	IDEICS	IDE Interrupt Configuration and Status Register	R/W
50h	PCIRR	IDE-PCI Interrupt Routing Register	R/W
51-FFh		Reserved	

3.1.2.1 VENID—Vendor ID

Register Offset: 00h
Default Value: 8086h
Access: Read Only
Size: 16 bits

This is a unique 16-bit value assigned to a vendor that, together with the Device ID, uniquely identifies each PCI device. Writes to this register have no effect.

Bits[15:0]: Vendor Identification
This is a 16-bit value assigned to Intel.

3.1.2.2 DEVID—Device ID

Register Offset: 02h
Default Value: 1222h
Access: Read Only
Size: 16 bits

This is a unique 16-bit value that is assigned to the PCI-IDE Interface function. Writes to this register have no effect.

Bits[15:0]: Device Identification
This value identifies the PCI-IDE Interface function.

3.1.2.3 PCICMD—PCI Command

Register Offset: 04h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This 16 bit register contains PCI control information.

Bits[15:10]: Reserved

Bit 9: Fast Back-to-Back Control
This control function can be used only by a PCI master and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 8: SERR# Enable
When this bit is set to 1, the PPEC asserts SERR# when it detects a parity error during an address phase, and when it detects an X.X PC Card in Mode 1, partially-buffered implementations. When this bit is set to 0, SERR# is not asserted for any reason. Reset sets the bit to 0.

Bit 7: Address/Data Stepping Control
This control function can be used only by a PCI master and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 6: Parity Error Enable
This bit controls PPEC response to PCI data parity errors. When this bit is set to 1, the PPEC activates PERR# when it detects a parity error during a data phase. When this bit is set to 0, the PPEC ignores parity errors. Reset sets the bit to 0 and disables data parity checking.

Bit 5: VGA Palette Snoop
This bit is intended only for specific control of PCI-based VGA devices, and is not applicable to the PPEC. The bit is not implemented, and always reads "0".

Bit 4: Memory Write and Invalidate Enable
This control function can be used only by the PCI master, and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 3: Special Cycle Enable
This bit is intended to enable response to supported special cycles. Since the PPEC does not respond to any special cycle, the bit is not implemented and always reads "0".

Bit 2: Bus Master Enable
This bit is intended to enable mastership of the PCI. Since the PPEC cannot be a PCI master, the bit is not implemented and always reads "0".

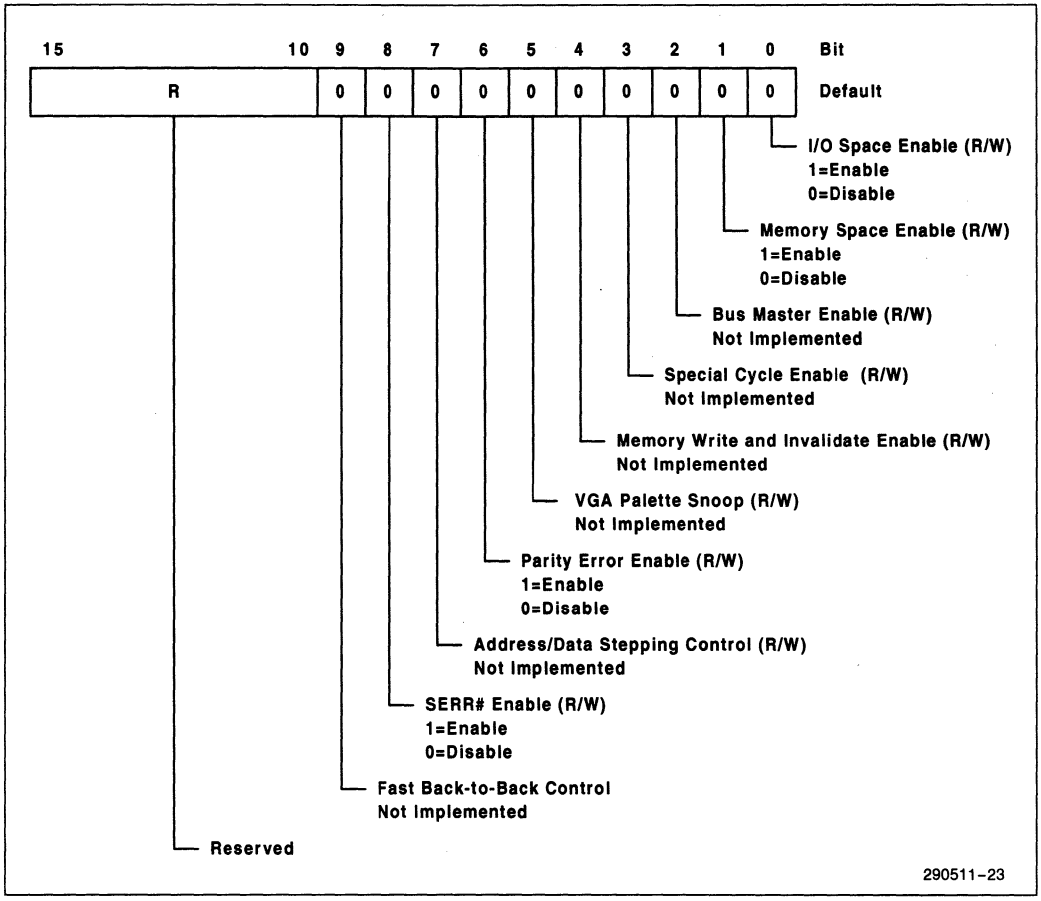


Figure 11. PCI Command Register

2

Bit 1: Memory Space Enable
This bit is intended to enable acceptance of PCI-originated memory cycles. Since the PCI-IDE Interface does not use memory cycles, the bit is not implemented and always reads "0".

Bit 0: I/O Space Enable
This bit enables the PCI-IDE Interface to accept PCI-originated I/O cycles. When the bit is set to 0, the interface does not respond to PCI master I/O cycles, and the PPEC's PCI-IDE DEVSEL# logic is inhibited during the I/O cycles.

3.1.2.4 PCISTS—PCI Status

Register Offset: 06h
Default Value: 0280h
Access: Read Only (see register description)
Size: 16 bits

This 16 bit register is used to record status information for PCI bus-related events. Reads to this register behave normally. Writing bits 11, 14, and 15 to 1 set the bits to 0. The other register bits cannot be written.

Bit 15: Detected Parity Error Status
The PPEC sets this bit to 1 when, as a target, it detects a parity error during a data phase, even if parity error handling is disabled by bit 6 and bit 8 in the PCI Command Register.

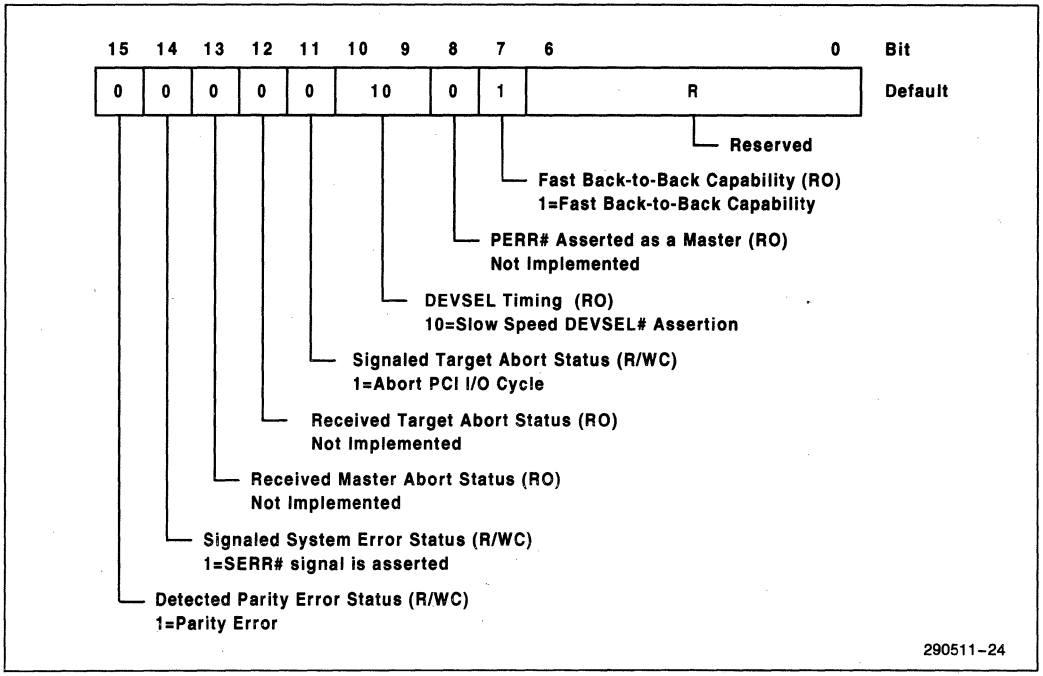


Figure 12. PCI Status Register

Bit 14: Signaled System Error Status
The PPEC sets this bit to 1 whenever it signals an address phase parity error by asserting SERR#.

Bit 13: Received Master Abort Status
This control function can be used only by a PCI master, and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 12: Received Target Abort Status
This control function can be used only by a PCI master, and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 11: Signaled Target Abort Status
The PPEC sets this bit to 1 when it is the target of a PCI I/O cycle, and the address/byte-enable combination is invalid.

Bits[10:9]: DEVSEL Timing
These read-only bits identify the slowest DEVSEL# response time for all bus commands except *configuration read* and *configuration write*, as defined in the PCI Specification. The PPEC implements medium speed DEVSEL# timing for PCI-IDE functions, and the bits are therefore 10b.

Bit 8: PERR# Asserted as a Master
This control function can be used only by a PCI master and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 7: Fast Back-to-Back Capability
This read-only bit is set to 1 to indicate that the PPEC can support fast back-to-back cycles originated by a PCI master.

Bits[6:0]: Reserved

3.1.2.5 REVID—Revision ID

Register Offset: 08h
Default Value: 01h
Access: Read Only
Size: 8 bits

This 8-bit register contains device revision information. Writes to this register have no effect.

Bits[7:0]: Revision Identification
This is the revision level of the PPEC. The initial PPEC revision level is 01h.

3.1.2.6 CCPIB—Class Code-Programming Interface Byte

Register Offset: 09h
Default Value: 00h
Access: Read Only
Size: 8 bits

This 8-bit register contains device Programming Interface information related to the Class Code register located at 0Ah offset. Writes to this register have no effect.

Bits[7:0]: Programming Interface
There are no specific register-level programming interfaces defined for this Class Code (indicated by register CCCB). Therefore, the value of this field is 0.

3.1.2.7 CCCB—Class Code-Class Code Bytes

Register Offset: 0Ah
Default Value: 0101h
Access: Read Only
Size: 16 bits

This 16-bit register contains device Class Code information in the following format: [BASE CLASS][SUB-CLASS]. Writes to this register have no effect.

Bits[15:8]: Base Class
The value 01h in this field identifies the function class as a *mass storage controller.*

Bits[7:0]: Sub-Class
The value 01h in this field identifies the function subclass as an *IDE Controller.*

3.1.2.8 HTYPE—Header Type

Register Offset: 0Eh
Default Value: 80h
Access: Read Only
Size: 8 bits

This register indicates whether or not the device contains multiple functions, and identifies the layout of bytes 10h through 3Fh in configuration space. Bit 7 indicates s multifunctional device when set to 1. Bits[6:0] specify layout of bytes 10h-3Fh. The PPEC uses layout type #0 as defined in the PCI specification. Writes to this register have no effect.

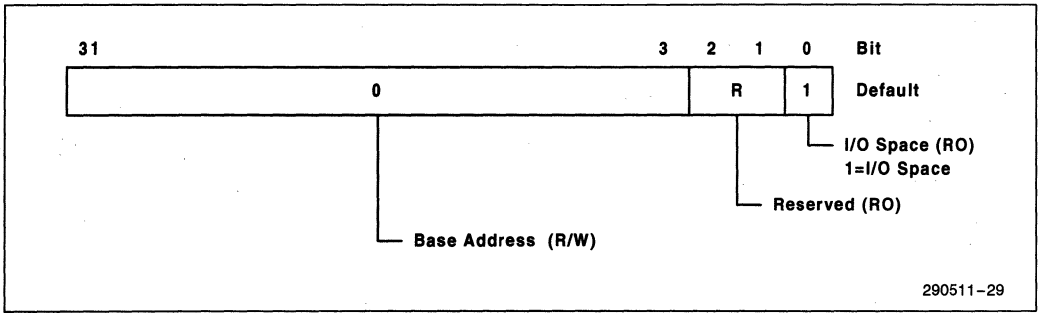


Figure 13. IDE Base Address Register 0

Bit 7: Multifunction Indicator
This bit is set to 1 to indicate that the PPEC is a multifunctional device.

Bits[6:0]: Byte Layout
This field specifies layout type "0" for bytes 10-3Fh, as defined in the PCI Specification.

3.1.2.9 PDCBA—IDE Base Address #0-Primary IDE Data/Command Address Range

Register Offset: 10h
Default value: 0000 0001h
Access: Read/Write
Size: 32 bits

This register determines the starting address of the primary IDE I/O address range for the Data/Command register block. It can be mapped anywhere in 4 GByte space on an 8-byte boundary.

The address range is defined as follows:

BaseAddress ≤ address ≤ BaseAddress +7.

Bits[31:3]: Base Address
This field holds the programmable base address of the primary IDE I/O address range for the Data/Command register block.

Bits[2:1]: Reserved

Bit 0: I/O Space
This read only bit is set to 1 to indicate I/O space.

NOTE:
The PCI-compliant Base Address mechanism can be used for motherboard PPEC/IDE applications with PCI-customized BIOS. For applications that must use IDE functions in an ISA-compatible manner (e.g. PPEC add-in card with system BIOS that does not support PPEC-IDE), the address ranges defined with the four IDE BASE registers can be disabled by selecting the IDE hardware configuration feature in the IDE Power-On Configuration register. This feature allows configuration of IDE addresses for the compatible ranges, and selection of enhanced IDE timing mode. The compatible ranges are:

- Primary Data/Command Ports: 1F0-1F7h
- Primary Control/Status Ports: 3F6h
- Secondary Data/Command Ports: 170-177h
- Secondary Control/Status Ports: 376h

This PPEC feature eliminates the need for custom software for the IDE function, and applies to all four IDE Base Address Registers.

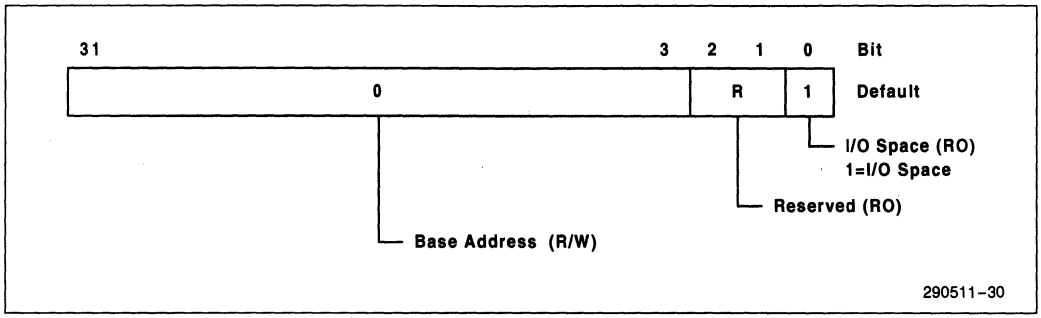


Figure 14. IDE Base Address Register 1

3.1.2.10 PCSBA—IDE Base Address #1-Primary IDE Control/Status Address Range

Register Offset: 14h
Default value: 0000 0001h
Access: Read/Write
Size: 32 bits

This register determines the starting address of the primary IDE I/O address range for the Control/Status register block. It can be mapped anywhere in 4 GByte I/O space on an 8-byte boundary.

The Primary address range is defined as follows:

BaseAddress ≤ address ≤ BaseAddress + 7.

Bits[31:3]: Base Address
This field holds the programmable base address of the primary IDE I/O address range for the Control/Status register block. These bits are read/write which indicates that the size of the required I/O address range is 8 bytes. In practical applications, only a subset of this range (1 byte) is used to access IDE registers.

Bits[2:1]: Reserved

Bit 0: I/O Space
This read only bit is set to 1 to indicate I/O space.

NOTE:
When accessing Control/Status Registers, proper offset must be used – 6h to access address xxx6h (Alternate Status Register).

3.1.2.11 SDCBA—IDE Base Address #2-Secondary IDE Data/Command Address Range

Register Offset: 18h
Default value: 0000 0001h
Access: Read/Write
Size: 32 bits

This register determines the starting address of the secondary IDE I/O address range for the Data/Command register block. It can be mapped anywhere in 4 GByte space on an 8-byte boundary.

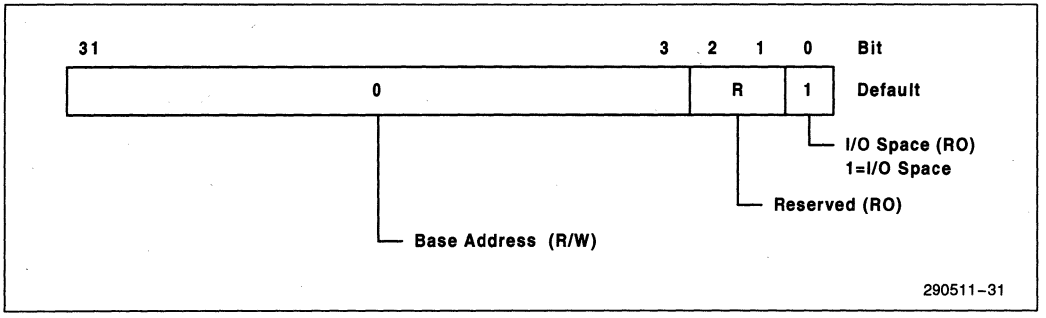


Figure 15. IDE Base Address Register 2

The address range is defined as follows:

BaseAddress ≤ address ≤ BaseAddress + 7.

Bits[31:3]: Base Address
This field holds the programmable base address of the secondary IDE I/O address range for the Data/ Command register block.

Bits[2:1]: Reserved

Bit 0: I/O Space
This read only bit is set to 1 to indicate I/O space.

3.1.2.12 SCSBA—IDE Base Address #3- Secondary IDE Control/Status Address Range

Register Offset: 1Ch
Default value: 0000 0001h
Access: Read/Write
Size: 32 bits

This register determines the starting address of the secondary IDE I/O address range for the Control/ Status register block. It can be mapped anywhere in 4 GByte I/O space on an 8-byte boundary.

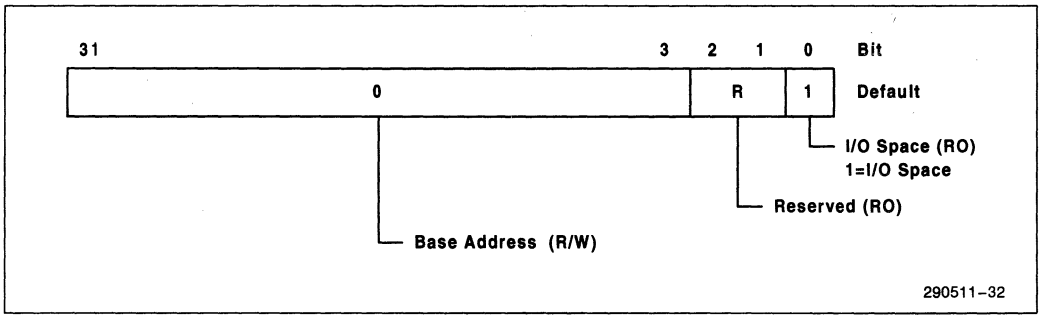


Figure 16. IDE Base Address Register 3

Secondary IDE Control/Status address range is defined as follows:

BaseAddress ≤ address ≤ BaseAddress + 7.

Bits[31:3]: Base Address
This field holds the programmable base address of the secondary IDE I/O address range for the Control/Status register block. These bits are read/write, which indicates that the size of the required I/O address range is 8 bytes. In practical applications, only a subset of this range (2 bytes) is used to access IDE registers.

Bits[2:1]: Reserved

Bit 0: I/O Space
This read only bit is set to 1 to indicate I/O space.

NOTE:
When accessing Control/Status Registers, proper offset must be used–6h to access address xxx6h (Alternate Status Register).

3.1.2.13 INTLIN—Interrupt Line

Register Offset:	3Ch
Default Value:	00h
Access:	Read/Write
Size:	8 bits

This register is used to communicate interrupt line routing information. BIOS software must initialize this register during system configuration. The value in this register identifies the interrupt request level of the system interrupt controller(s) to which the PPEC interrupt pin is connected. Device drivers and the operating system can use this information to determine priority and vector information. The value in this register is system architecture specific.

Bits[7:0]: Interrupt Line Identification
The value in this field identifies the interrupt request level of the system interrupt controller(s) to which the PPEC interrupt pin is connected.

NOTE:
The IDE Interface can connect to system interrupts in two different ways:

a. via a single PCI interrupt signal line (INTB#) that requires additional routing (system specific).

b. via 10 direct system interrupt signals (ISA mechanism).

Mode (b) is provided so that 'ISA compatible' IDE BIOS software can be used without modifications on X86/Pentium™-based platforms with the PPEC as a PCI-IDE Interface Controller. In this case, PCI interrupts are not used. IDE interrupts are configured to connect directly to a specific system IRQ line as specified in the IDE-ISA Interrupt Routing Register (IIIRR). The PCI Interrupt Line Register (INTLN) and the IDE-PCI Interrupt Routing Register (PCIRR) must remain in default state 0. Designs that do not require this software compatibility can use the PCI interrupt mechanism (a).

3.1.2.14 INTPIN—Interrupt Pin

Register Offset: 3Dh
Default Value: 02h
Access: Read Only
Size: 8 bits

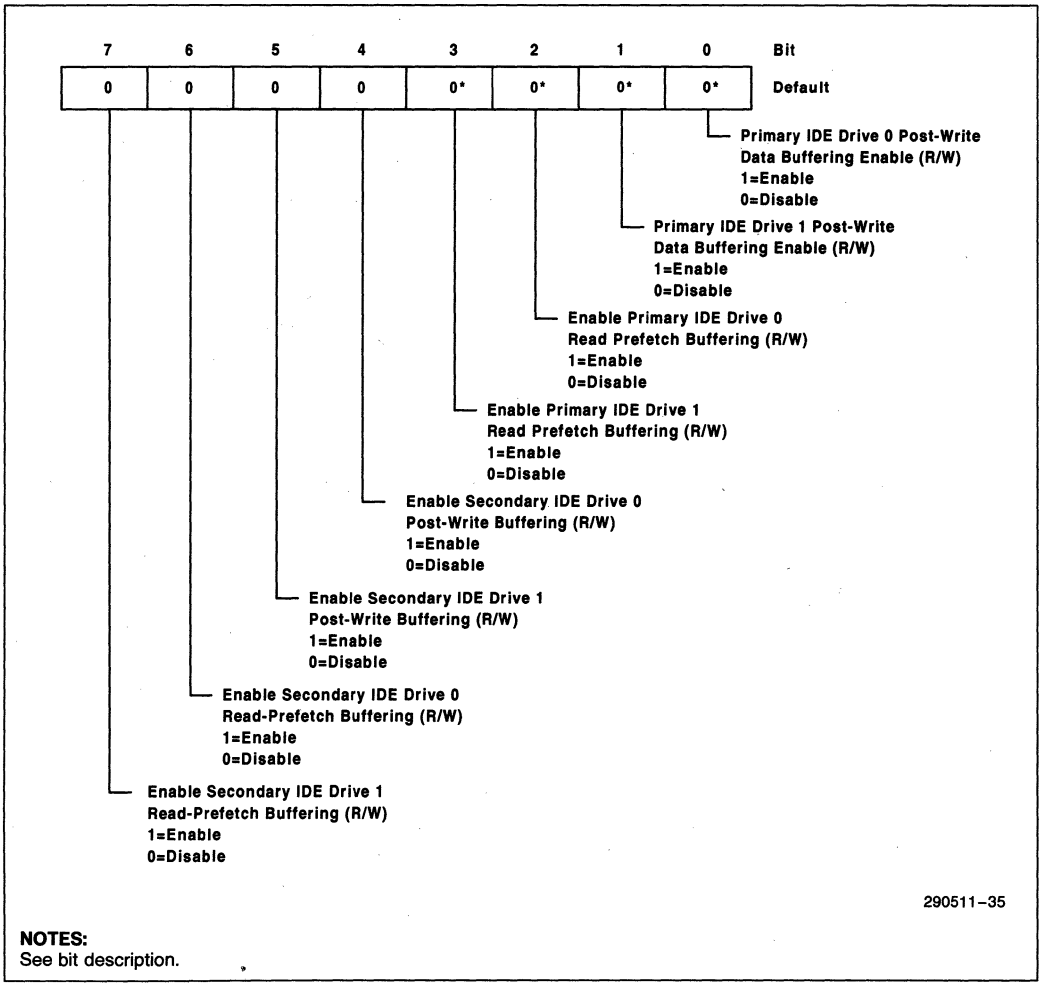
The value in this register, 02h, identifies the interrupt pin used by the PCI-IDE Interface for signaling IDE interrupts (Primary and/or Secondary IRQs) as INTB#. The IDE-PCI Interrupt Routing Register (PCIRR, located at offset 50h) is used to enable (for each IDE interface) interrupt signaling using the PCI interrupt scheme.

Bits[7:0]: Interrupt Pin Selection
The value in this field, 02h, identifies the PCI interrupt pin that is used by the PCI-IDE Interface device function as INTB#.

3.1.2.15 PCICON—PCI Configuration Control

Register Offset: 40h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register provides control of PCI-IDE data buffering.



NOTES:
See bit description.

Figure 17. PCI Configuration Control Register

Bit 7: Enable Secondary IDE Drive 1 Read-Prefetch Buffering
When this bit is set to 1, PCI to secondary IDE Drive 1 data buffering is enabled for Read Prefetch operations. When the bit is set to 0, the buffering is disabled.

Bit 6: Enable Secondary IDE Drive 0 Read-Prefetch Buffering
When this bit is set to 1, PCI to secondary IDE Drive 0 data buffering is enabled for Read Prefetch operations. When the bit is set to 0, the buffering is disabled.

Bit 5: Enable Secondary IDE Drive 1 Post-Write Buffering
When this bit is set to 1, PCI to secondary IDE Drive 1 data buffering is enabled for Post-Write operations. When the bit is set to 0, the buffering is disabled.

Bit 4: Enable Secondary IDE Drive 0 Post-Write Buffering
When this bit is set to 1, PCI to secondary IDE Drive 0 data buffering is enabled for Post-Write operations. When the bit is set to 0, the buffering is disabled.

Bit 3: Enable Primary IDE Drive 1 Read Prefetch Buffering
When this bit is set to 1, PCI to secondary IDE Drive 1 data buffering is enabled for Read Prefetch operations. When the bit is set to 0, the buffering is disabled. The default value of this bit is dependent on the IDE Hardware Configuration feature. If IDE Hardware Configuration is enabled (bit 0 of the PIDECFG register is set to 1), the bit defaults to the value of bit 7 of the PIDECFG register. If IDE Hardware Configuration is not enabled, the bit defaults to 0.

Bit 2: Enable Primary IDE Drive 0 Read Prefetch Buffering
When this bit is set to 1, PCI to primary IDE Drive 0 data buffering is enabled for Read Prefetch operations. When the bit is set to 0, the buffering is disabled. The default value of this bit is dependent on the IDE Hardware Configuration feature. If IDE Hardware Configuration is enabled (bit 0 of the PIDECFG register is set to 1), the bit defaults to the value of bit 7 of the PIDECFG register. If IDE Hardware Configuration is not enabled, the bit defaults to 0.

Bit 1: Enable Primary IDE Drive 1 Post-Write Buffering
When this bit is 1, PCI to secondary IDE Drive 1 Post-Write data buffering is enabled. When this bit is 0, buffering is disabled. The default value of this bit is dependent on the IDE Hardware Configuration feature. If IDE Hardware Configuration is enabled (bit 0 of the PIDECFG register is set to 1), the bit defaults to the value of bit 7 of the PIDECFG register. If IDE Hardware Configuration is not enabled, the bit defaults to 0.

Bit 0: Primary IDE Drive 0 Post-Write Buffering
When this bit is 1, PCI to primary IDE Drive 0 Post-Write data buffering is enabled. When this bit is 0, buffering is disabled. The default value of this bit is dependent on the IDE Hardware Configuration feature. If IDE Hardware Configuration is enabled (bit 0 of the PIDECFG register is set to 1), the bit defaults to the value of bit 7 of the PIDECFG register. If IDE Hardware Configuration is not enabled, the bit defaults to 0.

3.1.2.16 PIDECFG—Power-On IDE Configuration

Register Offset:	44h
Default Value:	xxh
Access:	Read/Write
Size:	8 bits

This register reports the status of the IDE Hardware Configuration signals that are multiplexed on PCMCIA Socket A data lines ACDATA[7:0] when the PPEC operates in Mode 0 (2-socket mode), and on common data lines CDATA[7:0] when the PPEC operates in Mode 1 (4-socket mode). The status of these signals is latched in this register during reset if this feature is enabled by the global IDE Hardware Configuration enable pin. These bits control the preload default value in the IDE timing control registers.

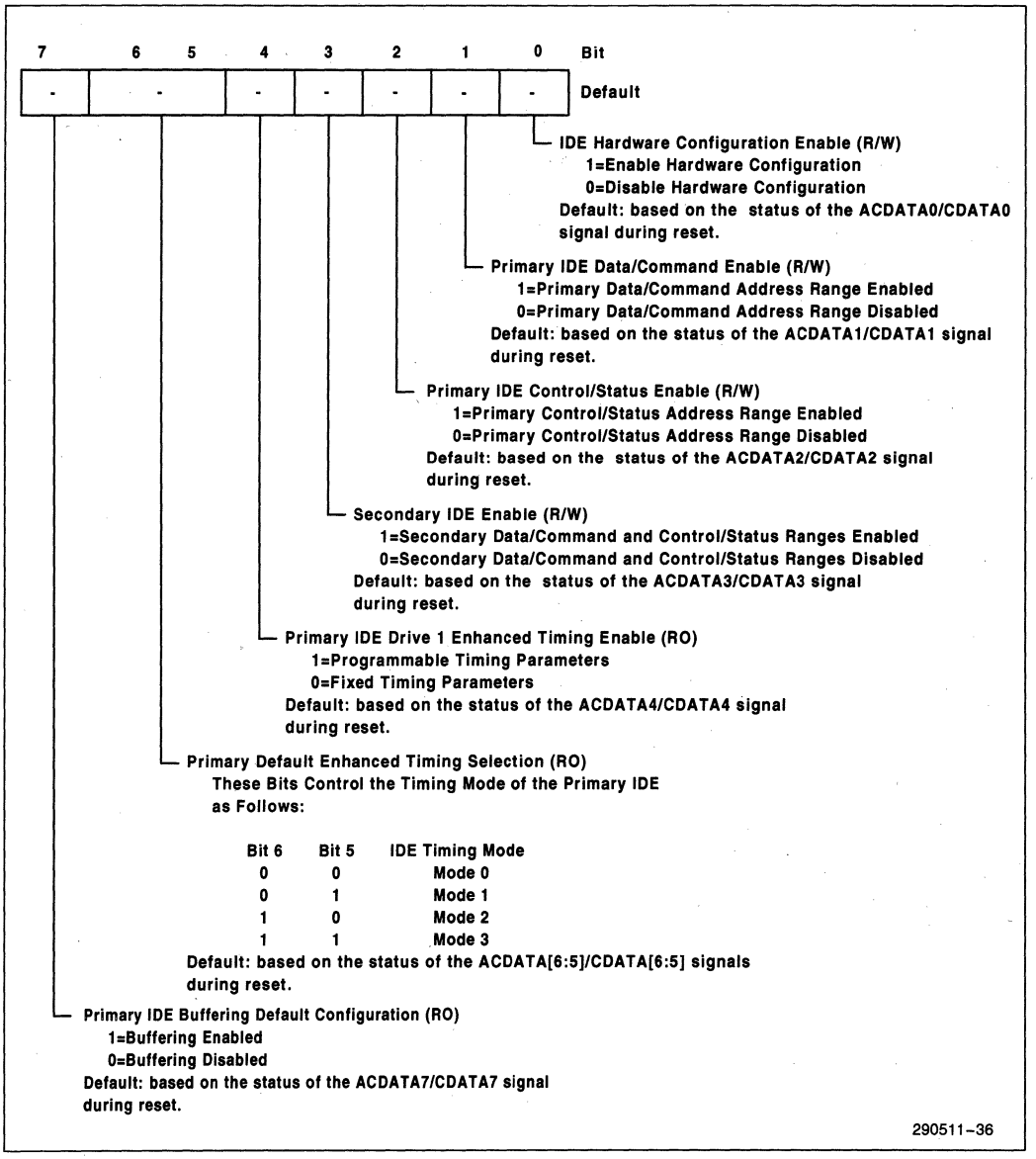


Figure 18. Power-On IDE Configuration Control Register

Bit 7: Primary IDE Buffering Default Configuration
This bit enables IDE data port buffering when set to 1 at the end of the reset sequence if ACDATA0 is externally pulled high, and disables IDE data port buffering when set to 0. If ACDATA0 is externally pulled low at the end of the reset sequence, this bit is not used to configure the IDE interface. After reset, this bit indicates the state of the ACDATA7/ CDATA7 signal at the end of the reset sequence.

Bits[6:5]: Primary Default Enhanced Timing Selection
These bits control the timing mode of the primary IDE interface at the end of the reset sequence if ACDATA0 is externally pulled high, as follows:

Bit 6	Bit 5	IDE Mode Timing
0	0	Mode 0
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

If ACDATA0 is externally pulled low at the end of the reset sequence, these bits are not used to configure the IDE interface. After reset, these bits indicate the states of the ACDATA[6:5]/CDATA[6:5] signals at the end of the reset sequence.

Note that these bits directly define the timing mode for Primary IDE drive 0, and that the same timing is applied to the Primary IDE drive 1 if bit 4 of this register is set to 1.

Bit 4: Primary Drive #1 Enhanced Timing Enable
When this bit is set to 1 at the end of the reset sequence with ACDATA0 externally pulled high, primary drive #1 data port timing is based on programmable timing parameters. When the bit is set to 0 at the end of the reset sequence, the timing is fixed, Mode 0 compatible timing. If ACDATA0 is externally pulled low at the end of the reset sequence, this bit is not used to configure the IDE interface. After reset, this bit indicates the state of the ACDATA4/ CDATA4 signal at the end of the reset sequence.

Bit 3: Secondary IDE Enable
When this bit is 0, all Secondary IDE registers are disabled regardless of whether they are selected from the preset compatible range (170-177h, 376h), or IDE Base Address #2 and #3. When this bit is 1, the Secondary IDE registers are enabled. The default value of this bit is 0 if IDE Hardware Configuration is disabled (bit 0 is sampled low). The default value is the value of ACDATA3 sampled at the end of the reset sequence if IDE Hardware Configuration is enabled (bit 0 is sampled high).

Bit 2: Primary IDE Control/Status Enable
When this bit is 0, the Primary IDE Control/Status register is disabled regardless of whether it is selected from the preset compatible range (3F6h), or IDE Base Address #1. When this bit is 1, the Primary IDE Data/ Command register is enabled. The default value of this bit is 0 if IDE Hardware Configuration is disabled (bit 0 is sampled low). The default value is the value of ACDATA2 sampled at the end of the reset sequence if IDE Hardware Configuration is enabled (bit 0 is sampled high).

Bit 1: Primary IDE Data/Command Enable
When this bit 0, the Primary IDE Data/Command registers are disabled regardless of whether they are selected from the preset compatible range (1F0-1F7h), or IDE Base Address #0. When this bit is 1, the Primary IDE Data/Command registers are enabled. This bit defaults to 0 if IDE Hardware Configuration is disabled (bit 0 is sampled low). The default value is the value of ACDATA1 sampled at the end of the reset sequence if IDE Hardware Configuration is enabled (bit 0 is sampled high).

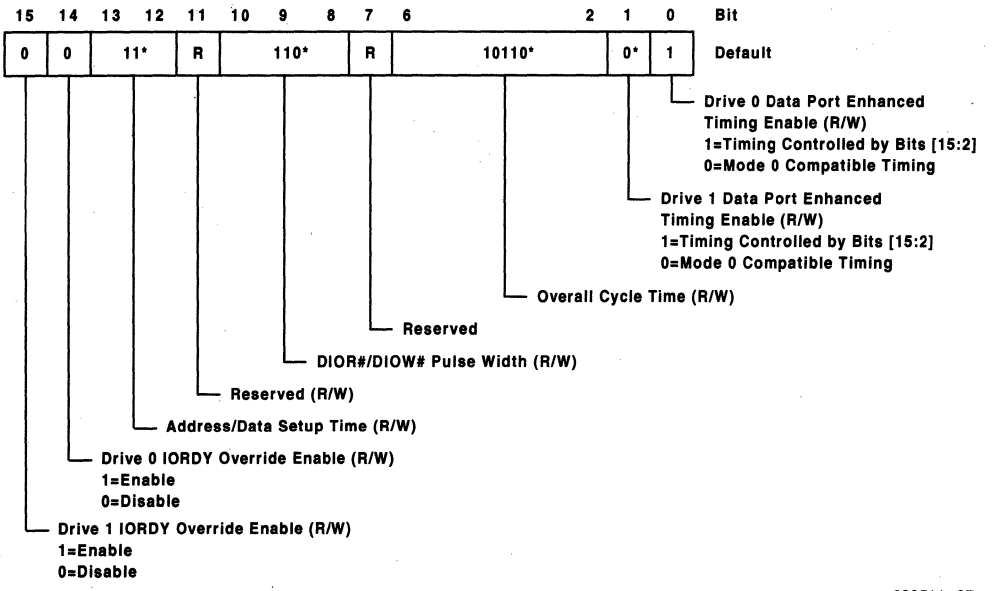
Bit 0: IDE Hardware Configuration Enable
The default value of this bit is determined by the value of the ACDATA0 signal at reset. If ACDATA0 is sampled high at the end of the reset sequence, the default values of hardware configuration bits[7:1] are determined by the values of ACDATA[7:1], the fixed IDE compatible ranges are selected (subject to enable bits[3:1]), and PCI-IDE space defaults to enabled. If ACDATA0 is sampled low, hardware configuration bits[7:1] default to 0, the IDE Base Address registers are selected (subject to enable bits[3:1]), and PCI-IDE I/O space defaults to disabled. A software write to this bit selects between IDE compatible ranges (1) and IDE Base Address registers (0), but does not affect the PCI-IDE I/O space enable.

NOTE:
The Secondary IDE timing and Data Buffering control are not IDE Hardware configurable. They default to the slowest timing mode (Mode 0), and data buffering disabled.

3.1.2.17 PIDETC—Primary IDE Timing Control

Register Offset:	48h
Default value:	xxxxh
Access:	Read/Write
Size:	16 bits

This register determines the timing characteristics and IORDY control of the Primary IDE interface.



NOTE:
See bit description.

Figure 19. Primary IDE Timing Control Register

Bit 15: Drive #1 IORDY Override Enable
When this bit is set to 1, the external IORDY signal is overridden for Primary Drive 1 (i.e., the IORDY signal is asserted internally regardless of the state of the external IORDY signal). When this bit is 0, the external IORDY signal is used to control completion of primary IDE drive #1 accesses.

Bit 14: Drive #0 IORDY Override Enable
When this bit is set to 1, the external IORDY signal is overridden for Primary Drive 0 (i.e., the IORDY signal is asserted internally regardless of the state of the external IORDY signal). When this bit is 0, the external IORDY signal is used to control completion of primary IDE drive #0 accesses.

Bits[13:12]: Address/Data Setup Time
These bits define, in system clock (PCICLK) periods, the address/data setup time with respect to the write/read strobes. If IDE hardware configuration is enabled by bit 0 of the Power-On IDE Configuration Register (PIDECFG), the default value of the bits correspond to the IDE timing mode selected by bits[6:5] of the PIDECFG Register. If IDE hardware configuration is not enabled, the default is 11 = Mode 0.

Bit 11: Reserved

Bits[10:8]: DIOR#/DIOW# Pulse Width
These bits define the width of the Write and Read strobes in system clock (PCICLK) periods. If IDE hardware configuration is enabled by bit 0 of the Power-On IDE Configuration Register (PIDECFG), the default value of the bits correspond to the IDE timing mode selected by bits[6:5] of the PIDECFG Register. If IDE hardware configuration is not enabled, the default is 110 = Mode 0.

Bit 7: Reserved

Bits[6:2]: Overall Cycle Time
Defines the length of the IDE cycle in system clock (PCICLK) periods. If IDE hardware configuration is enabled by bit 0 of the Power-On IDE Configuration Register (PIDECFG), the default value of the bits correspond to the IDE timing mode selected by bits[6:5] of the PIDECFG Register. If IDE hardware is not enabled, the default is 10110 = Mode 0.

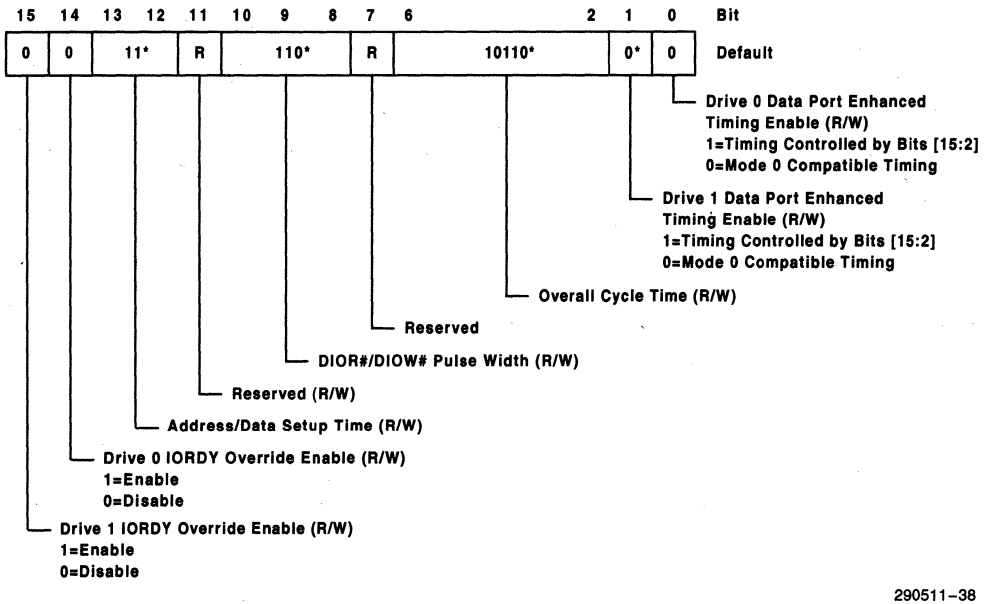
Bit 1: Drive #1 Data Port Enhanced Timing Enable
When this bit is set to 1, IDE Primary Drive 0 access timing is controlled by bits[15:2] of this register. Accesses to other ports is based on compatible timing as defined by Mode 0 in the ATA specification. If IDE hardware configuration is enabled by bit 0 of the Power-On IDE Configuration Register (PIDECFG), the default value of the bit is the value of bit 4 of the PIDECFG Register. If IDE hardware configuration is not enabled, the default is 0. When this bit is set to 0, accesses is based on compatible Mode #0 timing.

Bit 0: Drive #0 Data Port Enhanced Timing Enable
When this bit is set to 1, IDE Primary Drive 0 access timing is controlled by bits[15:2] of this register. Accesses to other ports is based on compatible timing as defined by Mode 0 in the ATA specification. When this bit is set to 0, accesses are based on compatible Mode #0 timing. The default value for this bit is 1.

3.1.2.18 SIDETC—Secondary IDE Timing Control

Register Offset:	4Ah
Default value:	3658h
Access:	Read/Write
Size:	16 bits

This register determines the timing characteristics and IORDY control of the Secondary IDE interface.



NOTES:
See bit description.

Figure 20. Secondary IDE Timing Control Register

Bits 15: Drive #1 IORDY Override Enable
When this bit is set to 1, the external IORDY signal is overridden for IDE Secondary Drive 1 (i.e., the IORDY signal is asserted internally regardless of the state of the external IORDY signal). When this bit is 0, the external IORDY signal is used to control completion of Secondary IDE drive #1 accesses.

Bit 14: Drive #0 IORDY Override Enable
When this bit is set to 1, the external IORDY signal is overridden for IDE Secondary Drive 0 (i.e., the IORDY signal is asserted internally regardless of the state of the external IORDY signal). When this bit is 0, the external IORDY signal is used to control completion of Secondary IDE drive #0 accesses.

Bits[13:12]: Address/Data Setup Time
These bits define, in system clock (PCICLK) periods, the address/data setup time with respect to the write/read strobes.

Bit 11: Reserved

Bits[10:8]: DIOR#/DIOW# Pulse Width.
These bits define the width of the Write and Read strobes in system clock (PCICLK) periods.

Bit 7: Reserved

Bits[6:2]: Overall Cycle Time
These bits define the length of the IDE cycle in system clock (PCICLK) periods.

Bit 1: Drive #1 Data Port Enhanced Timing Enable
When this bit is set to 1, IDE Secondary Drive 1 data port access timing is controlled by bits[15:2] of this register. Accesses to other ports are based on compatible timing as defined by Mode 0 in the ATA specification. When this bit is set to 0, accesses to IDE ports when Drive 0 is active is based on compatible Mode #0 timing.

Bit 0: Drive #0 Data Port Enhanced Timing Enable
When this bit is set to 1, IDE Secondary Drive 0 data port access timing is controlled by bits[15:2] of this register. Accesses to other ports are based on compatible timing as defined by Mode 0 in the ATA specification. When this bit is set to 0, accesses to IDE ports when Drive 0 is active is based on compatible Mode #0 timing.

NOTE:
The Secondary IDE timing mode is not IDE Hardware configurable. It defaults to Mode 0, the slowest timing mode.

2

3.1.2.19 IIIRR—IDE-ISA Interrupt Routing Register

Register Offset: 4Ch
Default Value: XXh
Access: Read/Write
Size: 8 bits

This register selects mapping of the Primary and Secondary IDE Interface interrupt requests to any of 10 ISA-compatible system interrupts.

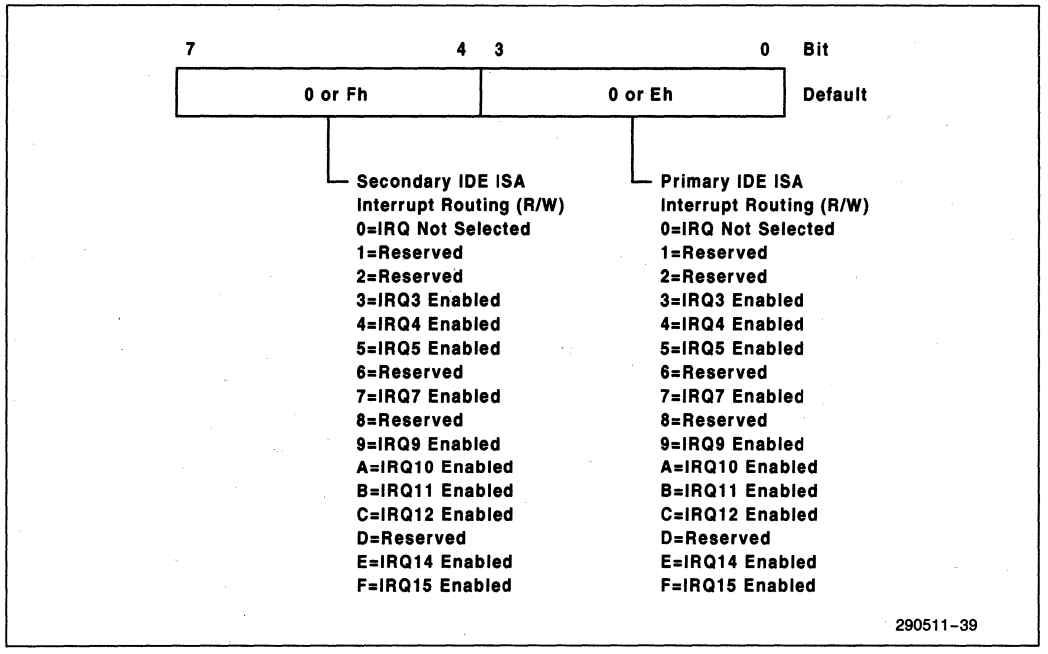


Figure 21. IDE-ISA Interrupt Routing Register

Bits[7:4]: Secondary IDE ISA Interrupt Mapping
This field selects the IRQ level for the Secondary IDE Interface. The default for this field is 0 if IDE Hardware Configuration is disabled (bit 0=0) in the Power-On IDE Configuration Control Register (PIDECFG). The default is Fh if IDE Hardware Configuration is enabled (bit 0=1) and the Secondary address range is enabled.

Bits[3:0]: Primary IDE ISA Interrupt Mapping
This field selects the IRQ level for the Primary IDE Interface. The default for this field is 0 if IDE Hardware Configuration is disabled (bit 0=0) in the Power-On IDE Configuration Control Register (PIDECFG). The default is Eh if IDE Hardware Configuration is enabled (bit 0=1) and the Primary Data/Command address range is enabled.

3.1.2.20 IDEICS—IDE Interrupt Configuration/ Status Register

Register Offset: 4Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register allows selection of edge or level mode for Primary and Secondary interrupts selected via the IIIRR Register, and provides non-latched read-only status of the physical PIRQ and SIRQ signal pins.

Bits[7:4]: Reserved

Bit 3: Secondary IDE System Interrupt Operation Mode
This bit provides the IRQ operation mode for the system interrupt signal selected to be used as a Secondary IDE Interrupt via the IIIRR Register as follows:

1=Level Mode Selected
0=Edge Mode Selected

Bit 2: Primary IDE System Interrupt Operation Mode
This bit provides the IRQ operation mode for the system interrupt signal selected to be used as a Primary IDE Interrupt via the IIIRR Register as follows:

1=Level Mode Selected
0=Edge Mode Selected

Bit 1: Secondary IDE Interrupt Status
This bit provides the status of the SIRQ Secondary IRQ signal as follows:

1=Secondary IDE IRQ active
0=Secondary IDE IRQ inactive

Bit 0: Primary IDE Interrupt Status
This bit provides the status of the SIRQ Primary IRQ signal as follows:

1=Primary IDE IRQ active
0=Primary IDE IRQ inactive

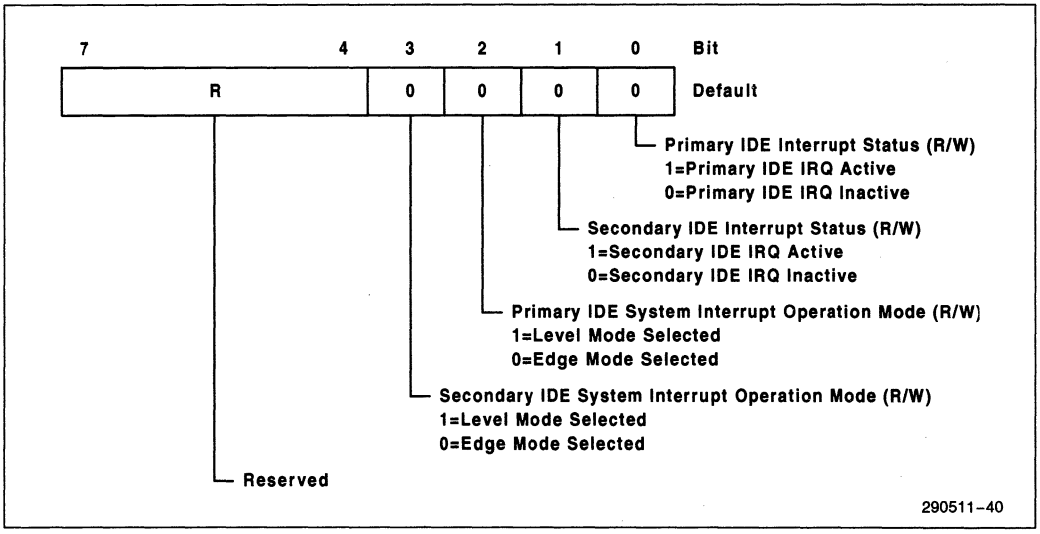


Figure 22. IDE Interrupt Configuration/Status Register

3.1.2.21 PCIRR—IDE-PCI Interrupt Routing Register

Register Offset: 50h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register allows mapping of IDE interrupts to either ISA interrupts, or PCI interrupts. One interrupt can be generated for the primary IDE interface, and another for the secondary IDE interface. Each of the interrupts can be routed independently. When bit 0 or 1 is set to 0, the corresponding interrupt is routed via one of 10 system interrupt lines (ISA mechanism) selected by the IDE ISA Interrupt Mapping Register. When set to 1, the corresponding interrupt is routed via INTB# (PCI mechanism).

Bits[7:2]: Reserved

Bit 1: Secondary IDE Interrupt Routing
This bit selects Secondary IDE Interface Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 0: Primary IDE Interrupt Routing
This bit selects Primary IDE Interface Interrupt routing via the PCI mechanism, or the ISA mechanism.

3.2 PCMCIA Socket Configuration Registers

The PPEC has four identical sets of registers for controlling the four PCMCIA sockets, with each set controlling one socket. Each register set is comprised of four types of registers: General Setup Registers, Interrupt Registers, I/O Mapping Control Registers, and Memory Mapping Control Registers. One set of registers is described in the following sections, with the address offset for each socket shown in each description.

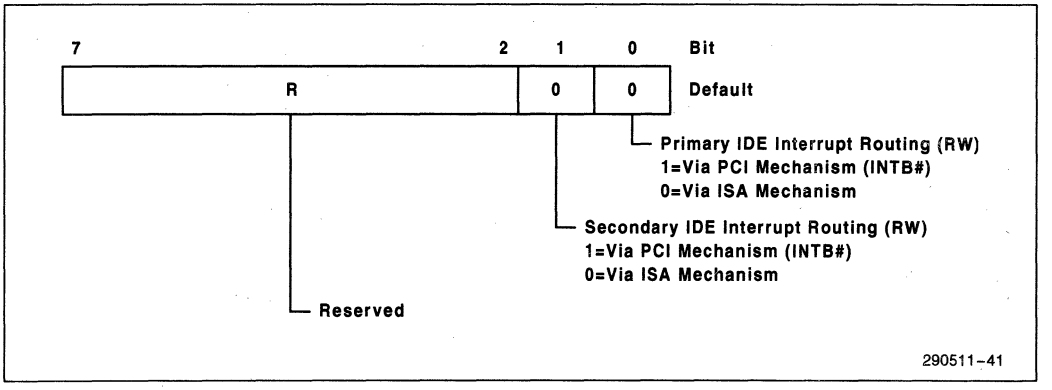


Figure 23. IDE Interrupt Routing Register

3.2.1 GENERAL SETUP REGISTERS

The General Setup Registers, listed in Table 8, are 8-bit registers. Writes to Read Only General Setup registers and register bits have no effect.

Table 8. General Setup Registers

Register Offset Sockets A:D				Mnemonic	Register Name	Access
A	B	C	D			
00	40	80	C0	IDREG	Identification	RO
01	41	81	C1	ISTAT	Interface Status	RO
02	42	82	C2	PCTRL	Power Control	R/W
04	44	84	C4	CSTCH	Card Status Change	R/W
06	46	86	C6	ADWEN	Address Window Enable	R/W
1E	5E	9E	DE	GCTRL	Global Control	R/W
2E	6E	AE	EE	CSCTRL	Global Security Control	R/W
16	56	96	D6	CDGEN	Card Detect and General Control	R/W
26	66	A6	E6	CPAGE	Card Memory Page	R/W

3.2.1.1 IDREG—Identification Register

Register Offset: Socket A—00h
Socket B—40h
Socket C—80h
Socket D—C0h
Default value: 84h
Access: Read/Write
Size: 8 bits

The Identification Register is used by the system software to determine the type of PC Cards supported by the socket.

Bits[7:6]: Interface Type
These bits indicate the type of PC Cards supported by the PPEC at the particular socket as follows:

00 = I/O Only
01 = Memory Only
10 = Memory and I/O
11 = Reserved

These bits do not identify the type of card that is present at the socket.

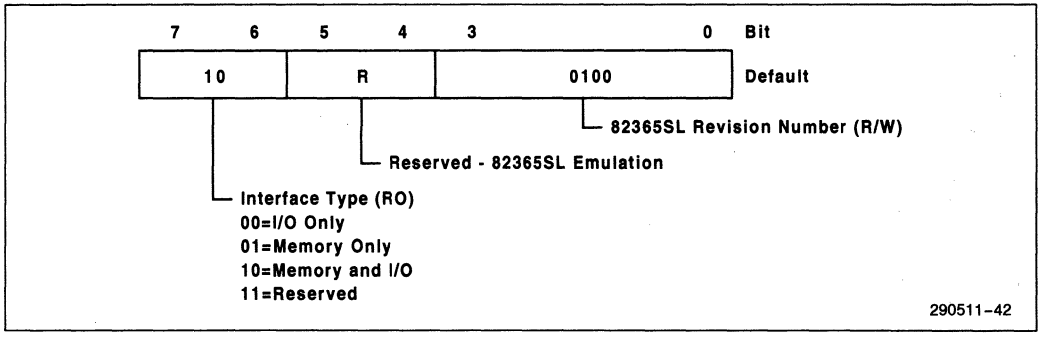


Figure 24. Identification Register

Bits[5:4]: Reserved
These are read/write bits that can be used to store 82365SL-specific information to allow 82365SL emulation.

Bits[3:0]: Reserved—82365SL Revision Information
This read/write field holds 82365SL revision information that allows the PPEC to emulate the 82365SL. Software checks this field before executing code written for the 82365SL.

3.2.1.2 ISTAT—Interface Status Register

Register Offset:	Socket A—01h
	Socket B—41h
	Socket C—81h
	Socket D—C1h
Default value:	XX
Access:	Read-only
Size:	8 bits

The Interface Status Register provides the current status of the PC Card socket interface signals.

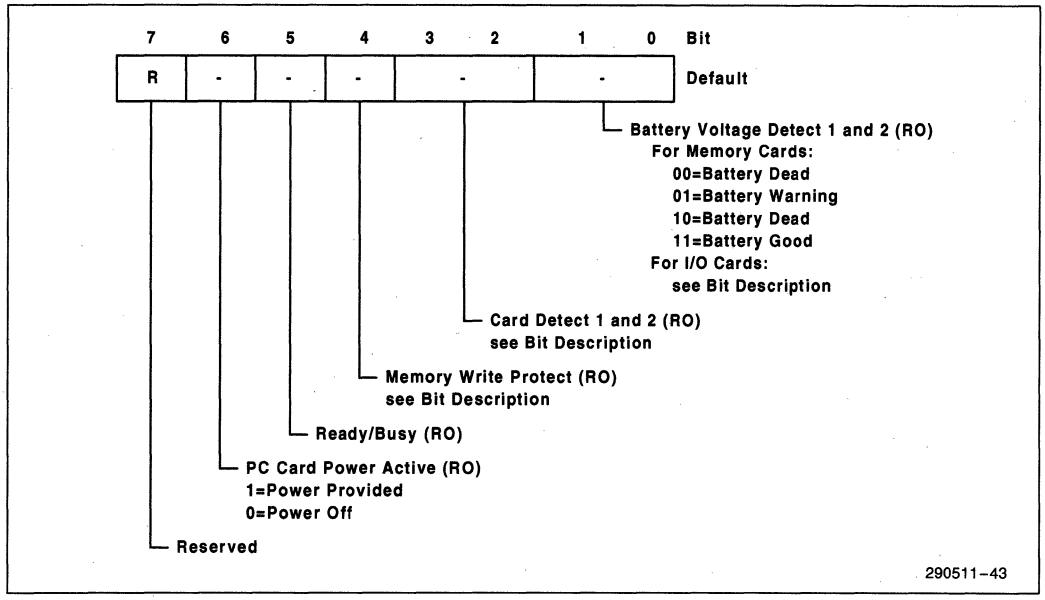


Figure 25. Interface Status Register

Bit 7: Reserved

Bit 6: PC Card Power Active
Indicates the current power status of the socket. If this bit is set to zero, power to the socket is turned off (V_{CC} and V_{PP} are not applied). If the bit is set to one, power is applied to the socket (V_{CC} is applied according to bits[4:3] of the Power Control Register, and V_{PP} is applied according to bits[1:0] of the Power Control Register).

Bit 5: Ready/Busy#
This bit is set to 1 to indicate that the PC Card is ready to accept a data transfer, and set to 0 to indicate that the card is busy completing an operation and cannot accept new data or commands.

Bit 4: Memory Write Protect
This bit indicates the logic level of the WP signal on the memory PC Card interface. However, memory write access to the socket is blocked only if the write protect bit in the associated Card Memory Offset Address Register High byte register is set to one.

Bits[3:2]: Card Detect 1 and 2
These bits indicate, when both are set to 1, that a card is present at the socket and is fully seated. Bit 2 is set to 1 if the CD1 signal on the PC Card interface is active, and bit 3 is set to 1 if the CD2 signal is active. Bits 2 and 3 are set to 0 if the corresponding CD1 and CD2 signals on the PC Card interface are inactive.

Bits[1:0]: Battery Voltage Detect 1 and 2
For memory cards, these bits indicate the status of the battery as follows:

BVD1	BVD2	Status
0	0	Battery Dead
0	1	Battery Dead
1	0	Warning
1	1	Battery Good

For I/O PC Cards, bit 0 indicates the current status of the STSCHG signal from the PC Card. For I/O PC Cards, bit 1 indicates the current state of SPKR signal from the PC Card. Refer to the Interrupt General Control Register bit 7 description for more details.

3.2.1.3 PCTRL—Power Control Register

Register Offset: Socket A—02h
Socket B—42h
Socket C—82h
Socket D—C2h
Default value: xx
Access: Read/Write
Size: 8 bits

This register controls power to the PC card. PCIRST# (PCI reset) clears all bits in this register. Output Enable should not be set until the register has been previously written setting the socket V_{PP} and V_{CC} Power Control bits.

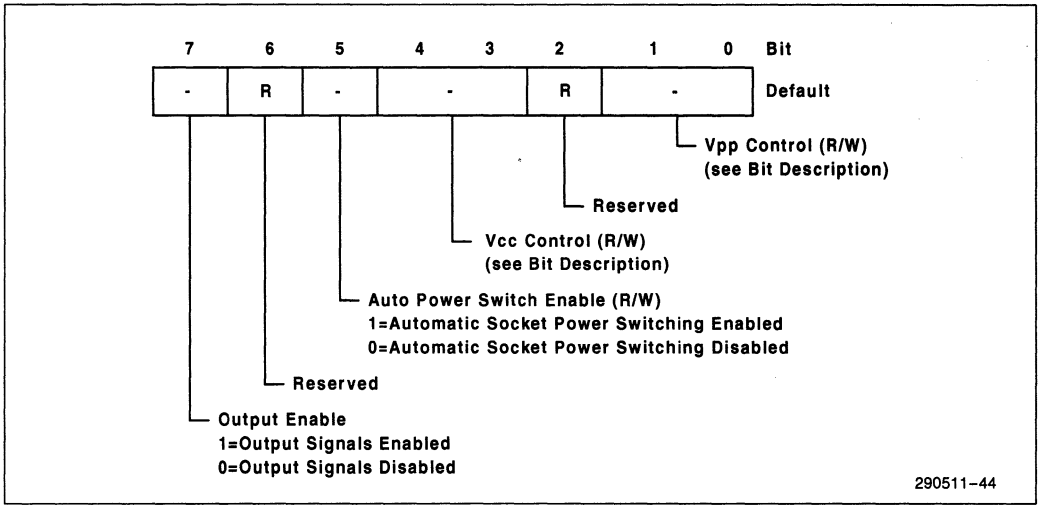


Figure 26. Power Control Register

Bit 7: Output Enable
When this bit is set to 0, the PPEC output signals that are directly connected to the socket (Mode 0) or are shared by other sockets (Mode 1) are tri-stated, and the ENABLE# signal to the socket is inactive. When the bit is set to 1, the signals are not tri-stated, and the ENABLE# signal is asserted. Output Enable should be set to 0 when the socket is not powered.

Bit 6: Reserved

Bit 5: Auto Power Switch Enable
When this bit is set to 0, automatic socket power switching based on card detects is disabled. When the bit is set to 1, automatic socket power switching is enabled. Automatic socket power switching function controls the V_{CC}xV and V_{PP}ENx power control bits. V_{CC} is 5V or 3.3V depending on the sampled states of the VS1 and VS2 signals provided in the Card Detect and General Control Register.

Bits[4:3]: V_{CC} Control
These bits control the power to the PC Card via the external V_{CC}-3V and V_{CC}-5V control logic (External Power Latch). The two bits are encoded as follows:

Bit 4	Bit 3	V_{CC}5V	V_{CC}3V	Description
0	0	0	0	No Connect
0	1	0	0	Reserved
1	0	1	0	5.0V
1	1	0	1	3.3V

Bit 2: Reserved

Bits[1:0]: V_{PP} Control
These bits switch V_{PP} power using the external Vpp control logic (External Power Latch). The two bits are encoded together with bit 4 to implement the following control functions:

Bit 4	Bit 1	Bit 0	V_{PP} EN1	V_{PP} EN0	Applied Voltage
1	0	0	0	0	No Connect
1	0	1	0	1	5.0V
1	1	0	1	0	12.0V
1	1	1	0	0	Reserved
0	x	x	0	0	No Connect

For more details on V_{CC}/V_{PP} control functions, see the Power Control description in Section 1.4.2 of this document.

3.2.1.4 CSTCH—Card Status Change Register

Register Offset: Socket A—04h
Socket B—44h
Socket C—84h
Socket D—C4h
Default value: 00h
Access: Read/Write
Size: 8 bits

This register contains the status of the sources for the Card Status Change Interrupts. These sources can be enabled to generate a Card Status Change Interrupt by setting the corresponding bit in the Card Status Change Interrupt Configuration Register. The bits in this register read back as 0 when the corresponding status enable bits in the Card Status Change Interrupt Configuration Register are set to 0.

When the Explicit Write Back Card Status Change Acknowledge bit is set in the Global Control Register, the acknowledgment of sources for the Card Status Change Interrupt is performed by writing back 1 to the appropriate bit in the Card Status Change Register that was read as a 1. Once the interrupt source is acknowledged by writing a 1 to the bit, the bit reads back as 0. The interrupt signal responding to the card status change remains active, if enabled on a system IRQ line, until all of the bits in this register are zero.

When the Explicit Write Back Card Status Acknowledge bit is not set, the Card Status Change Interrupt remains active, if enabled on a system IRQ line, until the Card Status Change Register is read. The read operation to the Card Status Change Register resets all bits in the register.

If two or more Card Status Change Interrupts are pending or a Card Status Change Interrupt condition occurs while another is being serviced, the PPEC does not generate a second interrupt.

The Interrupt Service Routine must read the Card Status Change Register to ensure that all interrupt requests are serviced before exiting the service routines.

Asserted PCIRST# (PCI reset) clears all bits in this register.

In the following bit descriptions, bits names that are in parenthesis are valid when the interface is configured for I/O PC Cards.

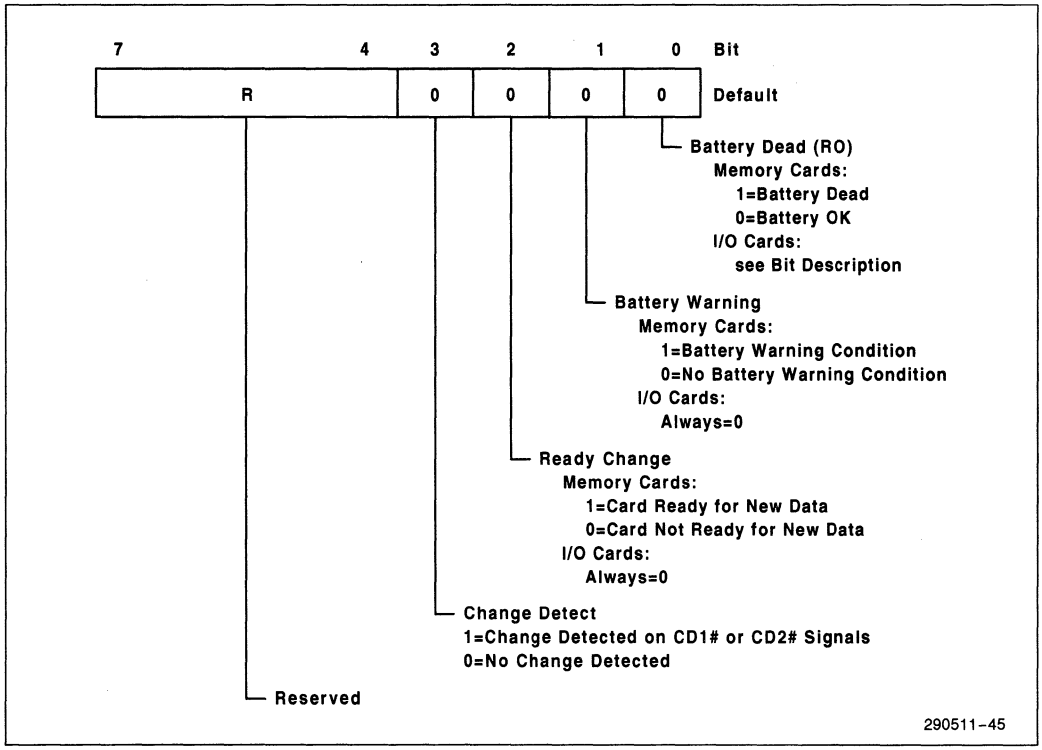


Figure 27. Card Status Change Register

Bits[7:4]: Reserved

Bit 3: Change Detect
This bit is set to 1 when a change occurs in either the CD1# or CD2# signal, or when a Software Interrupt is generated.

Bit 2: Ready Change
This bit is set to 1 when a low-to-high transition occurs on the RDY-BSY# signal, indicating that the memory PC Card is ready to accept a new data transfer. The bit reads 0 for I/O PC Cards.

Bit 1: Battery Warning
This bit is set to 1 when a battery warning condition is detected. The bit reads 0 for I/O PC Cards.

Bit 0: Battery Dead
For memory PC Cards, this bit is set to 1 when a battery dead condition has been detected. For I/O PC Cards, it is set to 1 when the STSCHG# signal from the I/O PC Card has been asserted low. The system software must then read the status change register in the PC Card to determine why the status change signal (STSCHG#) has been asserted.

3.2.1.5 ADWEN—Address Window Enable Register

Register Offset:	Socket A—06h
	Socket B—46h
	Socket C—86h
	Socket D—C6h
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register controls enabling of the memory and I/O mapping windows to the PC Card memory or I/O space. All bits in this register are cleared after reset.

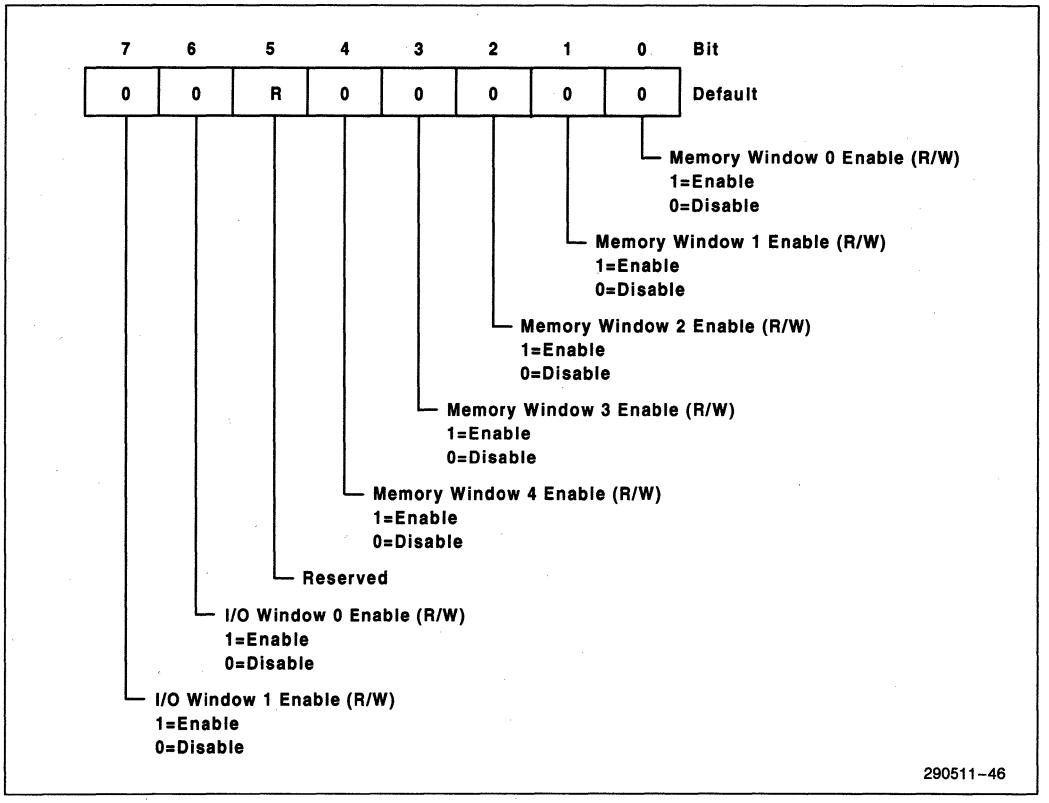


Figure 28. Address Window Enable Register

Bit 7–Bit 6: I/O Window 1 and Window 0 Enables
Bits[7:6] function identically and independently. Bit 7 applies to I/O Window 1; Bit 6 applies to I/O Window 0. When the bits are set to 0, the card enable signals to the PC cards that are accessed through the corresponding I/O windows are inhibited. When set to one, the card enable signals are not inhibited. I/O accesses pass addresses from the system bus directly through to the PC cards. The corresponding Start and Stop register pairs must all be set to the desired window values before setting either of the bits to one.

Bit 5: Reserved

Bit 4–Bit 0: Memory Window 4 - Memory Window 0 Enables
Bits[4:0] function identically and independently. Bit 4 applies to Memory Window 4, bit 3 applies to Memory Window 3, etc. When the bits are set to 0, the card enable signals to PC cards that are accessed through the corresponding memory windows are inhibited. When set to one, the card enable signals are not inhibited. The corresponding start, stop, and offset register pairs must all be set to the desired window values before setting any of the bits to 1. When one of the bits is set to 1 and the system address is within the corresponding window, the computed address will be generated for the accessed PC Card.

3.2.1.6 GCTRL—Global Control Register

Register Offset:	Socket A—1Eh Socket B—5Eh Socket C—9Eh Socket D—DEh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register is not duplicated for each socket, but can be accessed with the Socket A, B, C or D index. PCI reset clears all bits in this register.

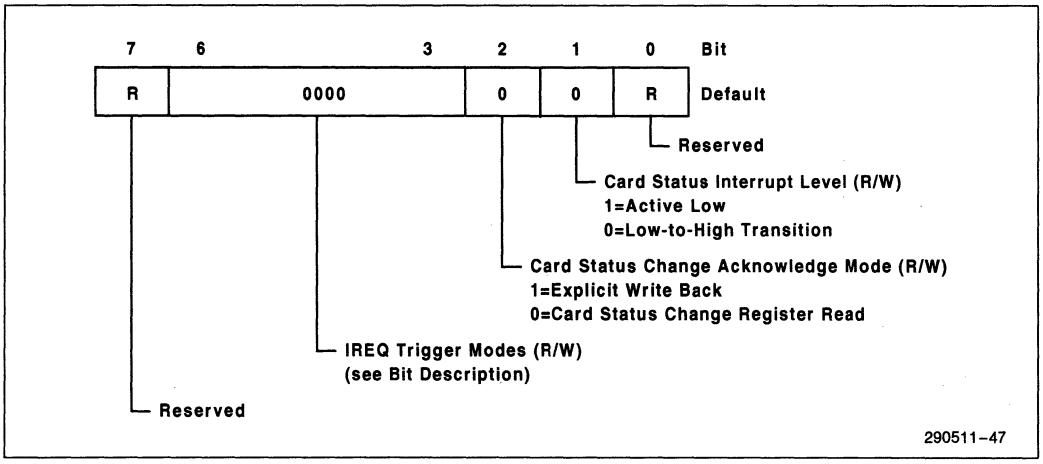


Figure 29. Global Control Register

Bit 7: Reserved

Bits[6:3]: IREQ Trigger Modes
When set to 1, these bits select level mode interrupts for IRQs generated by the particular PC card interrupts. When set to 0 (default), they select edge mode interrupts. Bit 3 is used for Socket A, Bit 4 for Socket B, Bit 5 for Socket C, and Bit 6 for Socket D

Bit 2: Card Status Change Acknowledge Mode
When this bit is set to 1, each Card Status Change Interrupt is acknowledged with an explicit write of 1 to the Card Status Change Register bit that identifies the interrupt. When this bit is set to 0 (default state), each Card Status Change Interrupt is acknowledged by reading the Card Status Change Register. Reading the Card Status Change Register clears the register.

Bit 1: Card Status Interrupt Level
When this bit is set to 1, the mode of the IRQ outputs used to signal the Card Status Change (CSC) Interrupt is active low level. In this mode, the IRQs remain tri-stated until there is a card status change condition, at which time the asserted IRQ output goes low. The IRQ remains low until the interrupt is acknowledged (serviced). Once serviced, the IRQ output will change from low to tri-state.

When this bit is set to its default state of 0, the CSC IRQ outputs are low-to-high edge triggered interrupts. In this mode, the IRQ signals remain tri-stated until enabled for CSC interrupt, at which time the IRQ outputs are asserted low. The outputs stay low until there is a card status change condition, which causes the appropriate IRQ output to transition to the high level. It will remain high until the interrupt is acknowledged (serviced), then transitions to the low state. When disabled, the IRQ signals are tri-stated.

Bit 0: Reserved

3.2.1.7 GSCTRL—Global Security Control Register

Register Offset:	Socket A—2Eh
	Socket B—6Eh
	Socket C—AEh
	Socket D—EEh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register is not duplicated for each socket, but can be accessed with the Socket A, B, C or D index. PCI reset clears all bits in this register.

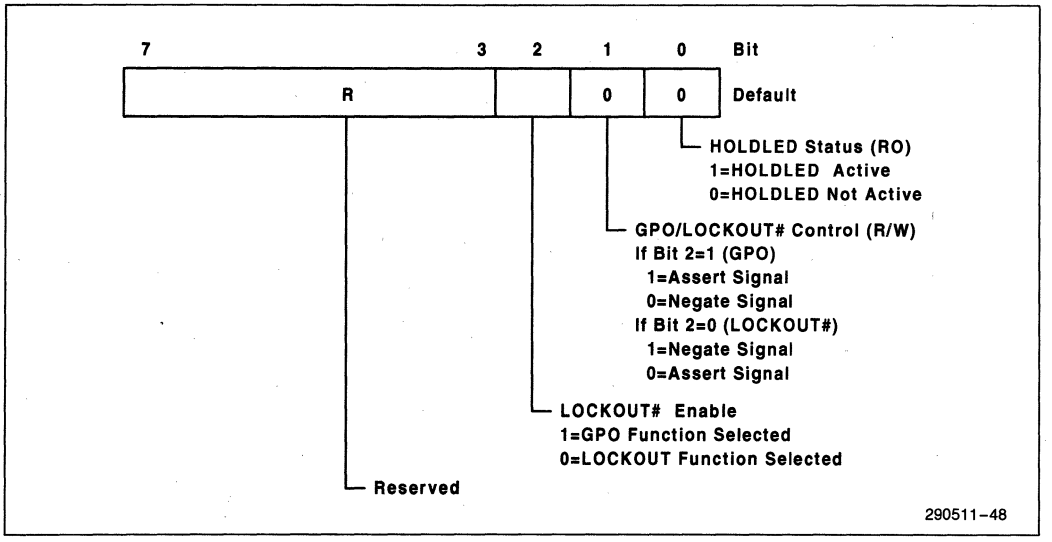


Figure 30. Global Security Control Register

Bits[7:3]: Reserved

Bit 2: Lockout# Enable
This bit configures bit 1 to function as GPO control when set to 1, and as LOCKOUT# control when set to 0.

Bit 1: General Purpose Output Control
When bit 2 is set to 1, this bit allows software control of the General Purpose Output control signal. When bit 2 is set to 0, this bit allows software control of the LOCKOUT# output signal. When bit 2 is 0 (LOCKOUT function) and this bit is 0, the LOCKOUT# signal is asserted, and the xCD2# signals function as "eject request". When bit 2 is 0 and this bit is 1, LOCKOUT# is negated, and the xCD2# signals retain their original function as Card Detect signals. See the PPEC Design Guide for details.

Bit 0: HOLDLED Status
This bit provides the status of the HOLDLED# output signal (pin), and is valid only in Mode 1.

3.2.1.8 CDGEN—Card Detect and General Control Register

Register Offset:	Socket A—16h
	Socket B—56h
	Socket C—96h
	Socket D—D6h
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register is used to reset configuration registers and store voltage select signal status. It is necessary that the Configuration Reset Enable bit is set to 1 by the card detect change interrupt service routine only when a PC Card is inserted, and set to 0 when the card is removed.

Bit 7: VS2 Voltage Select Status
This bit indicates the status of the VS2 multifunctional signal, which is used with VS1 to select proper V_{CC} voltage (5V or 3.3V or disable) at a socket.

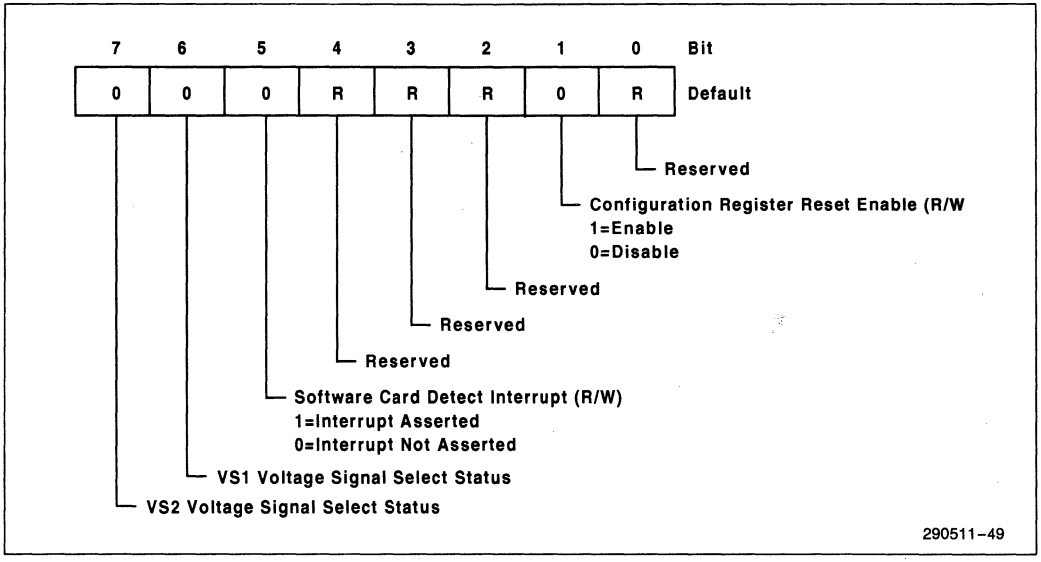


Figure 31. Card Detect and General Control Register

Bit 6: VS1 Voltage Select Status
This bit indicates the status of the VS1 voltage select signal, which is used to select proper V_{CC} voltage (5V or 3.3V or disable) at a socket.

Bit 5: Software Card Detect Interrupt
Setting this bit to 1 causes a Card Detect Card Status Change Interrupt for the associated socket if the Card Detect Enable bit is set to 1 in the Card Status Change Interrupt Configuration Register. The software interrupt functions and is acknowledged in the same manner as the hardware-generated interrupt.

The Hardware Card Detect Card Status Change Interrupt is not affected by the Software Card Detect Interrupt. The previous state of the CD1 and CD2 inputs are latched so that though a Card Detect Card Status Change Interrupt occurs and is serviced and the CD1 and CD2 inputs change from the previous state, a Hardware Card Detect Card Status Change Interrupt is still generated. If the Card Detect Enable bit is set to 0 in the Card Status Change Interrupt Configuration Register, writing a 1 to the Software Card Detect Interrupt bit has no effect.

The Software Card Detect Interrupt bit always reads back as a 0.

Bit 4: Reserved

Bit 3: Reserved

Bit 2: Reserved

Bit 1: Configuration Register Reset Enable
When this bit is set to 0, the configuration register reset function that is based on card detect is disabled. When it is set to 1, a reset pulse is generated to reset the configuration registers for the socket to their default state (zero's) when both the CD1 and CD2 inputs for the socket go high. There is one Configuration Register Reset Enable for each socket.

Bit 0: Reserved

3.2.1.9 CPAGE—Card Memory Page Address Register

Register Offset: Socket A—26h
Socket B—66h
Socket C—A6h
Socket D—E6h
Default value: 00h
Access: Read/Write
Size: 8 bits

This register holds an 8-bit page address that allows selection of a 16 MByte window page in the 4 GByte memory address space in which socket memory windows are mapped. Access to a window is allowed only when the page address in the corresponding Card Memory Page Address Register matches PCI memory address bits A[31:24], indicating a page hit. Reset clears all bits in this register, so that the default page is the first page (i.e., 0-16 MByte address range).

Bits[7:0]: Page Address
Page Address bits[7:0] correspond to system address lines A[31:24]. Access to one of the five memory windows is allowed only if a match between the page address and system address lines A[31:24] occurs.

3.2.2 INTERRUPT REGISTERS

The Interrupt Registers are listed in Table 9. The registers are 8-bit, read/write registers.

Table 9. Interrupt Registers

Register Offset Sockets A:D				Mnemonic	Register Name	Access
A	B	C	D			
03h	43h	83h	C3h	IGENC	Interrupt and General Control	R/W
05h	45h	85h	C5h	CSCICR	Card Status Change Interrupt Configuration	R/W

3.2.2.1 IGENC—Interrupt and General Control Register

Register Offset: Socket A—03h
Socket B—43h
Socket C—83h
Socket D—C3h
Default value: 00h
Access: Read/Write
Size: 8 bits

The Interrupt and General Control Register controls card type selection, card reset, and interrupt steering for the PC Card I/O interrupts.

Bit 7: Reserved

Bit 6: Card Reset
Setting this bit to 0 resets the PC Card by activating the RESET signal to the card. The RESET signal remains active until bit is set to 1.

Bit 5: Card Type
Setting this bit to 1 selects I/O PC Card, enabling the PC Card interface multiplexer to route PC Card I/O signals. Setting the bit to 0 selects Memory PC Card. When the bit is set to 1 (I/O PC Card), the STSCHG# signal from the I/O PC Card is used as the STSCHG status change signal. The current status of the signal is then available to be read from the Interface Status Register (01H), and the STSCHG signal can be configured as a source for the Card Status Change Interrupt.

Bit 4: Reserved

Bits[3:0]: IRQ Level Selection
This field selects interrupt routing for I/O PC Cards only.

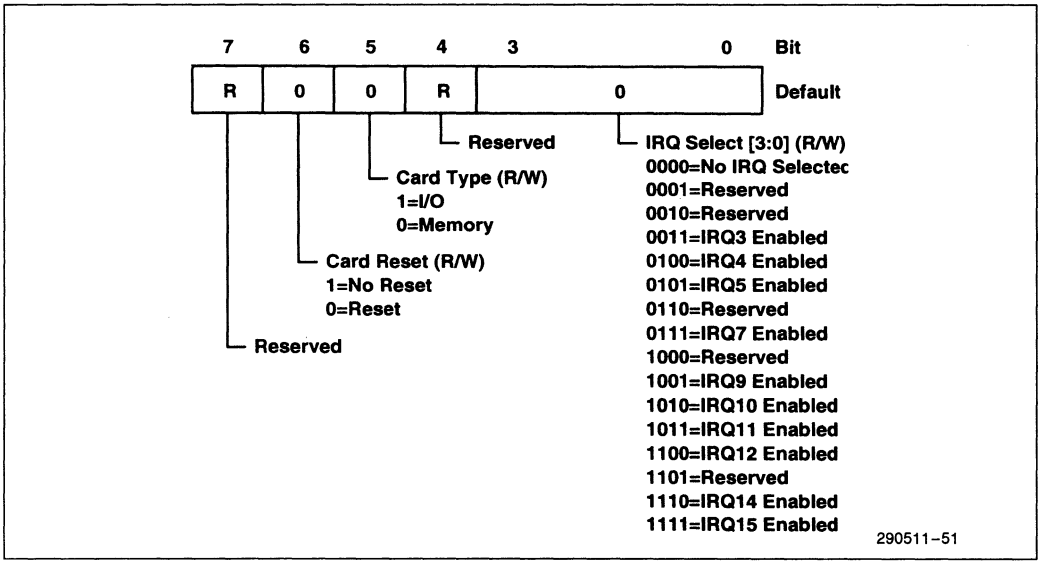


Figure 32. I/O Control Register

3.2.2.2 CSCICR—Card Status Change Interrupt Configuration Register

Register Offset: Socket A—05h
Socket B—45h
Socket C—85h
Socket D—C5h
Default value: 00h
Access: Read/Write
Size: 8 bits

This register controls Card Status Change Interrupt steering and the Card Status Change Interrupt enables.

Bits[7:4]: Card Status Change Interrupt Select
This field selects Card Status Change Interrupt routing.

Bit 3: Card Status Change Interrupt Enable
Setting this bit to 1 enables a Card Status Change Interrupt when a change in the CD1 or CD2 signal occurs, or when a Software Interrupt is generated by writing to bit 5 of the CDGEN register. Setting the bit to 0 disables the generation of a card status change interrupt when the CD1 or CD2 signals change state, or upon software command.

Bit 2: Ready Interrupt Enable
Setting this bit to 1 enables a Card Status Change Interrupt when a low to high transition occurs on the RDY-BSY# signal. Setting the bit to 0 disables the interrupt. The bit has no effect when the interface is configured for I/O PC Cards.

Bit 1: Battery Warning Interrupt Enable
Setting this bit to 1 enables a Card Status Change Interrupt when a battery warning condition is detected. Setting the bit to 0 disables the interrupt.

Bit 0: Battery Dead Enable
Setting this bit to 1 enables a Card Status Change Interrupt when a battery dead condition is detected in a memory PC Card, and when the STSCHG# signal is pulled low by an I/O PC Card. Setting the bit to 0 disables the interrupt.

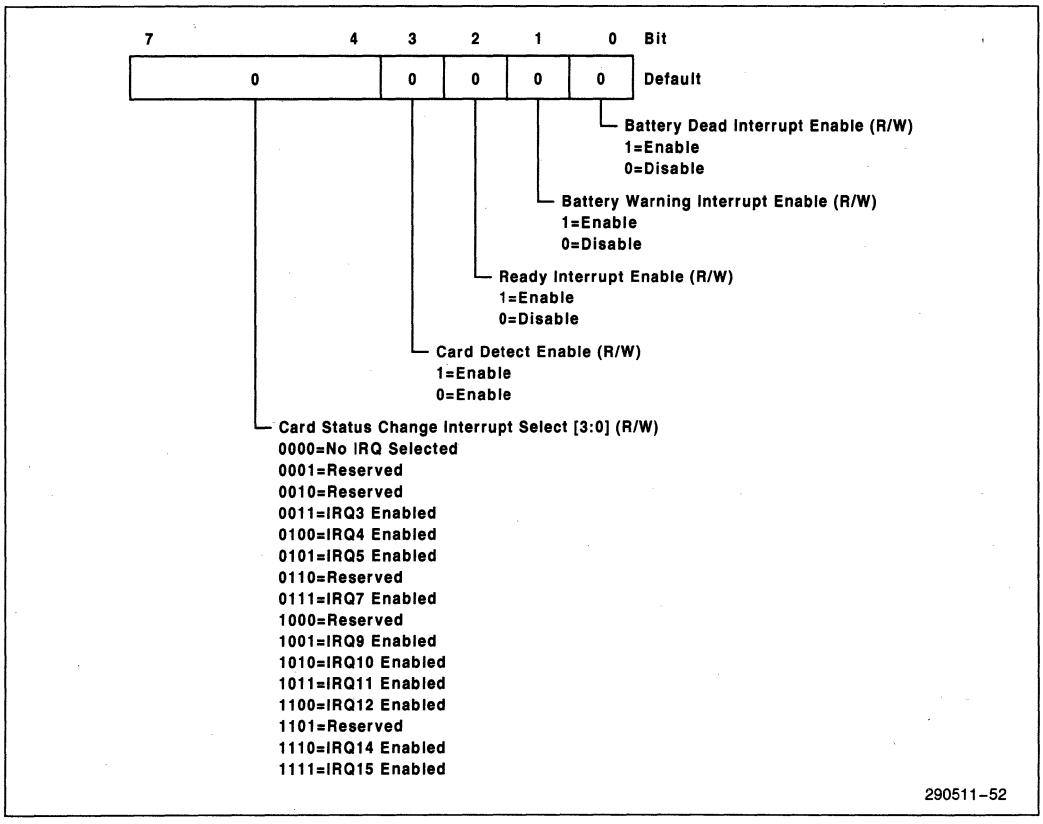


Figure 33. Card Status Change Interrupt Configuration Register

3.2.3 I/O MAPPING CONTROL REGISTERS

The I/O Mapping Control Registers are listed in Table 10. The registers are 8 bit read/write registers that specify data path sizes and start and stop addresses for the two I/O windows.

Table 10. I/O Mapping Control Registers

Register Offset Sockets A:D				Mnemonic	Register Name	Access
A	B	C	D			
07h	47h	87h	C7h	IOCREG	I/O Control	R/W
08h	48h	88h	C8h	IOSL0	I/O Address 0 Start Low Byte	R/W
09h	49h	89h	C9h	IOSH0	I/O Address 0 Start High Byte	R/W
0Ah	4Ah	8Ah	CAh	IOSTL0	I/O Address 0 Stop Low Byte	R/W
0Bh	4Bh	8Bh	CBh	IOSTH0	I/O Address 0 Stop High Byte	R/W
0Ch	4Ch	8Ch	CCh	IOSL1	I/O Address 1 Start Low Byte	R/W
0Dh	4Dh	8Dh	CDh	IOSH1	I/O Address 1 Start High Byte	R/W
0Eh	4Eh	8Eh	CEh	IOSTL1	I/O Address 1 Stop Low Byte	R/W
0Fh	4Fh	8Fh	CFh	IOSTH1	I/O Address 1 Stop High Byte	R/W

3.2.3.1 IOCREG—I/O Control Register

Register Offset: Socket A—07h
Socket B—47h
Socket C—87h
Socket D—C7h
Default value: 00h
Access: Read/Write
Size: 8 bits

This register controls the I/O data path size for I/O windows 0 and 1. In order to be compatible with some software and hardware implementations such as an IDE interface, it is necessary that the PC Card decode two consecutive I/O addresses to determine the cycle data width. To meet the system bus timings, this type of PC Card must decode address lines A[9:0] before the card enable signal becomes active at the interface. The card decodes the address and responds to a 16-bit cycle by asserting the IOIS16# signal. The PPEC qualifies IOIS16# with the card enable signals to control internal data assembly/disassembly logic.

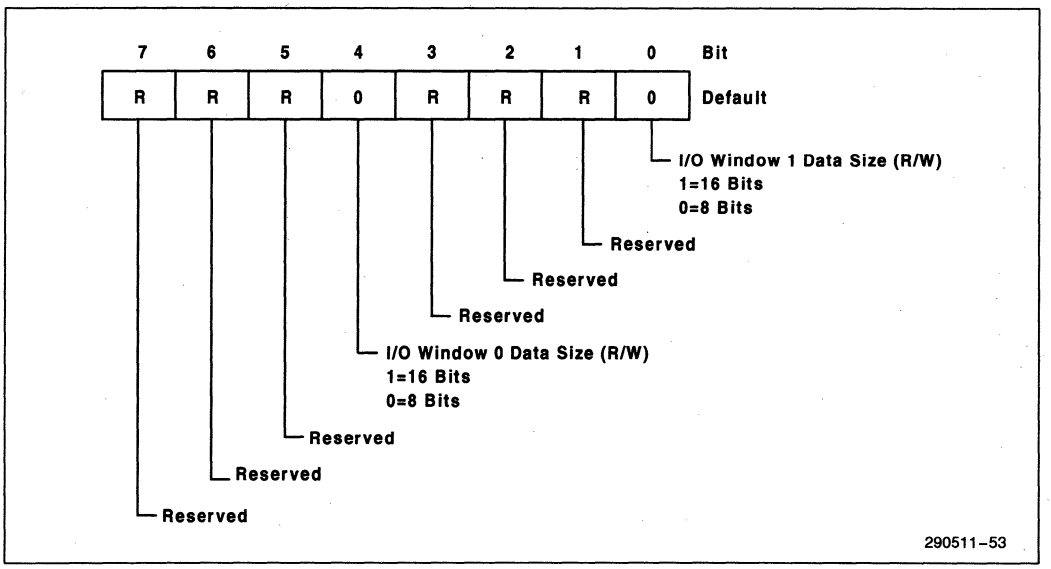


Figure 34. I/O Control Register

Bits[7:5]: Reserved

Bit 4: I/O Window 1 Data Size
This bit selects a 16-bit I/O data path to the PC Card when set to 1, and an 8-bit path when set to 0.

Bits[3:1]: Reserved

Bit 0: I/O Window 0 Data Size
This bit selects a 16-bit I/O data path to the PC Card when set to 1, and an 8-bit path when set to 0.

3.2.3.2 IOSL0—I/O Address 0 Start Low Byte Register

Register Offset:	Socket A—08h
	Socket B—48h
	Socket C—88h
	Socket D—C8h
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the low order address bits that are used to determine the start address of I/O address window 0. This provides a minimum 1 byte window for I/O address window 0 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 0 Start Address Low Bytes
This field holds start address bits A[7:0] of I/O address window 0.

3.2.3.3 IOSH0—I/O Address 0 Start High Byte Register

Register Offset:	Socket A—09h
	Socket B—49h
	Socket C—89h
	Socket D—C9h
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the high order address bits that are used to determine the start address of I/O address window 0.

Bits[7:0]: I/O Window 0 Start Address High Bytes
This field holds start address bits A[15:8] of I/O address window 0.

3.2.3.4 IOSTL0—I/O Address 0 Stop Low Byte Register

Register Offset:	Socket A—0Ah
	Socket B—4Ah
	Socket C—8Ah
	Socket D—CAh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the low order address bits that are used to determine the start address of I/O address window 0. This provides a minimum 1 byte window for I/O address window 0 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 0 Stop Address Low Bytes
This field holds stop address bits A[7:0] of I/O address window 0.

3.2.3.5 IOSTH0—I/O Address 0 Stop High Byte Register

Register Offset:	Socket A—0Bh
	Socket B—4Bh
	Socket C—8Bh
	Socket D—CBh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the high order address bits that are used to determine the stop address of I/O address window 0. This provides a minimum 1 byte window for I/O address window 0 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 0 Stop Address High Bytes
This field holds stop address bits A[15:8] of I/O address window 0.

3.2.3.6 IOSL1—I/O Address 1 Start Low Byte Register

Register Offset: Socket A—0Ch
Socket B—4Ch
Socket C—8Ch
Socket D—CCh
Default value: 00h
Access: Read/Write
Size: 8 bits

This register holds the low order address bits that are used to determine the start address of I/O address window 1. This provides a minimum 1 byte window for I/O address window 0 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 1 Start Address Low Bytes
This field holds start address bits A[7:0] of I/O address window 1.

3.2.3.7 IOSH1—I/O Address 1 Start High Byte Register

Register Offset: Socket A—0Dh
Socket B—4Dh
Socket C—8Dh
Socket D—CDh
Default value: 00h
Access: Read/Write
Size: 8 bits

This register holds the high order address bits that are used to determine the start address of I/O address window 1.

Bits[7:0]: I/O Window 1 Start Address High Bytes
This field holds start address bits A[15:8] of I/O address window 1.

3.2.3.8 IOSTL1—I/O Address 1 Stop Low Byte Register

Register Offset: Socket A—0Eh
Socket B—4Eh
Socket C—8Eh
Socket D—CEh
Default value: 00h
Access: Read/Write
Size: 8 bits

This register holds the low order address bits that are used to determine the start address of I/O address window 1. This provides a minimum 1 byte window for I/O address window 1 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 1 Stop Address Low Bytes
This field holds stop address bits A[7:0] of I/O address window 1.

3.2.3.9 IOSTH1—I/O Address 1 Stop High Byte Register

Register Offset: Socket A—0Fh
Socket B—4Fh
Socket C—8Fh
Socket D—CFh
Default value: 00h
Access: Read/Write
Size: 8 bits

This register holds the high order address bits that are used to determine the stop address of I/O address window 1. This provides a minimum 1 byte window for I/O address window 1 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 1 Stop Address High Bytes
This field holds stop address bits A[15:8] of I/O address window 1.

3.2.4 MEMORY MAPPING CONTROL REGISTERS

The Memory Mapping Control Registers are 8 bit, read/write registers that specify the starting and stopping addresses of the five memory windows. The registers are listed in Table 11.

The registers are identical for each window. Therefore, only one of each type of register is shown in the following descriptions. The addresses for all five windows for each socket are shown, however, in the *Register Offset* section of each register description.

Table 11. Memory Mapping Control Registers

Register Offset Sockets A:D				Mnemonic	Register Name	Access
A	B	C	D			
10h	50h	90h	D0h	SMSL0	System Memory Address Mapping Window 0 Start Low Byte	R/W
18h	58h	98h	D8h	SMSL1	System Memory Address Mapping Window 1 Start Low Byte	R/W
20h	60h	A0h	E0h	SMSL2	System Memory Address Mapping Window 2 Start Low Byte	R/W
28h	68h	A8h	E8h	SMSL3	System Memory Address Mapping Window 3 Start Low Byte	R/W
30h	70h	B0h	F0h	SMSL4	System Memory Address Mapping Window 4 Start Low Byte	R/W
11h	51h	91h	D1h	SMSH0	System Memory Address Mapping Window 0 Start High Byte	R/W
19h	59h	99h	D9h	SMSH1	System Memory Address Mapping Window 1 Start High Byte	R/W
21h	61h	A1h	E1h	SMSH2	System Memory Address Mapping Window 2 Start High Byte	R/W
29h	69h	A9h	E9h	SMSH3	System Memory Address Mapping Window 3 Start High Byte	R/W
31h	71h	B1h	F1h	SMSH4	System Memory Address Mapping Window 4 Start High Byte	R/W
12h	52h	92	D2h	SMSTL0	System Memory Address Mapping Window 0 Stop Low Byte	R/W
1Ah	5Ah	9Ah	DAh	SMSTL1	System Memory Address Mapping Window 1 Stop Low Byte	R/W
22h	62h	A2h	E2h	SMSTL2	System Memory Address Mapping Window 2 Stop Low Byte	R/W
2Ah	6Ah	AAh	EAh	SMSTL3	System Memory Address Mapping Window 3 Stop Low Byte	R/W
32	72h	B2h	F2h	SMSTL4	System Memory Address Mapping Window 4 Stop Low Byte	R/W
13h	53h	93h	D3h	SMSTH0	System Memory Address Mapping Window 0 Stop High Byte	R/W
1Bh	5Bh	9Bh	DBh	SMSTH1	System Memory Address Mapping Window 1 Stop High Byte	R/W
23h	63h	A3h	E3h	SMSTH2	System Memory Address Mapping Window 2 Stop High Byte	R/W

Table 11. Memory Mapping Control Registers (Continued)

Register Offset Sockets A:D				Mnemonic	Register Name	Access
A	B	C	D			
2Bh	6Bh	ABh	EBh	SMSTH3	System Memory Address Mapping Window 3 Stop High Byte	R/W
33h	73h	B3h	F3h	SMSTH4	System Memory Address Mapping Window 4 Stop High Byte	R/W
14h	54h	94h	D4h	OFFL0	Card Memory Offset Address 0 Low Byte	R/W
1Ch	5Ch	9Ch	DCh	OFFL1	Card Memory Offset Address 1 Low Byte	R/W
24h	64h	A4h	E4h	OFFL2	Card Memory Offset Address 2 Low Byte	R/W
2Ch	6Ch	ACh	ECh	OFFL3	Card Memory Offset Address 3 Low Byte	R/W
34h	74h	B4h	F4h	OFFL4	Card Memory Offset Address 4 Low Byte	R/W
15h	55h	95h	D5h	OFFH0	Card Memory Offset Address 0 High Byte	R/W
1Dh	5Dh	9Dh	DDh	OFFH1	Card Memory Offset Address 1 High Byte	R/W
25h	65h	A5h	E5h	OFFH2	Card Memory Offset Address 2 High Byte	R/W
2Dh	6D	ADh	EDh	OFFH3	Card Memory Offset Address 3 High Byte	R/W
35h	75h	B5h	F5h	OFFH4	Card Memory Offset Address 4 High Byte	R/W

3.2.4.1 SMSL[4:0]—System Memory Address Mapping Windows 0-4 Start Low Byte Registers

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	10h	18h	20h	28h	30h
Socket B	50h	58h	60h	68h	70h
Socket C	90h	98h	A0h	A8h	B0h
Socket D	D0h	D8h	E0h	E8h	F0h

Default value: 00h
Access: Read/Write
Size: 8 bits

These five registers hold the low order address bits that determine the start address of the corresponding system memory address mapping windows. The register contents correspond to PCI memory address bits A[19:12], and are used to determine whether memory accesses are valid.

Bits[7:0]: System Memory Window Start Address
This field holds the system memory window start address bits A[19:12].

3.2.4.2 SMSH[4:0]—System Memory Address Mapping Windows 0-4 Start High Byte Registers

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	11h	19h	21h	29h	31h
Socket B	51h	59h	61h	69h	71h
Socket C	91h	99h	A1h	A9h	B1h
Socket D	D1h	D9h	E1h	E9h	F1h

Default value: 00h
Access: Read/Write
Size: 8 bits

These five registers hold the high order address bits that determine the start address of the corresponding system memory address mapping windows. The address bits correspond to PCI memory address bits A[23:20], and are used to determine whether memory accesses are valid. The data path size of each window is controlled by a bit in its corresponding register.

Bit 7: Data Size
This bit selects an 8-bit memory data path to the PC Card when set to 0, and a 16-bit memory data path when set to 1.

Bit 6: Reserved

Bits[5:4]: Scratch Bits

These bits can be used for general-purpose register storage and retrieval.

Bits[3:0]: Memory Window Start Address
These are high order address bits that determine the start address of the system memory address mapping window.

3.2.4.3 SMSTL[4:0]—System Memory Address Mapping Windows 0-4 Stop Low Byte Register

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	12h	1Ah	22h	2Ah	32h
Socket B	52h	59h	62h	6Ah	72h
Socket C	91h	99h	A2h	AAh	B2h
Socket D	D2h	D9h	E2h	EAh	F2h

Default value: 00h
Access: Read/Write
Size: 8 bits

These five registers hold the low order address bits that determine the stop address of the corresponding system memory address mapping windows. The register contents correspond to PCI memory address bits A[19:12], and are used to determine whether memory accesses are valid.

Bits[7:0]: System Memory Window Stop Address
This field holds the system memory window stop address bits A[19:12].

3.2.4.4 SMSTH[4:0]—System Memory Address Mapping Windows 0–4 Stop High Byte Registers

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	13h	1Bh	23h	2Bh	33h
Socket B	53h	5Bh	63h	6Bh	73h
Socket C	93h	9Bh	A3h	ABh	B3h
Socket D	D3h	DBh	E3h	EBh	F3h

Default value: 10100000b
Access: Read/Write
Size: 8 bits

These five registers contain the high order address bits that determine the stop address of the corresponding system memory address mapping windows. The address bits correspond to PCI memory address bits A[23:20], and are used to determine whether memory accesses are valid. Two bits in each of the registers select delays for 16-bit accesses to the corresponding system memory window.

Bits[7:5]: Memory Window Timing Select
PCMCIA timing parameters are independently configured for each Common Memory Window by programming these timing bits. Timing Mode 101 is the default for this field, and cannot be changed (i.e. writes to the bits 5-7 are ignored) until PPEC-PCMCIA PCICON register bit 5 (Enhanced PCMCIA Timing Mode Enable) is set to 1.

Bit 4: Reserved

Bits[3:0]: Memory Window Stop Address
This field holds system memory window stop address bits A23:A20.

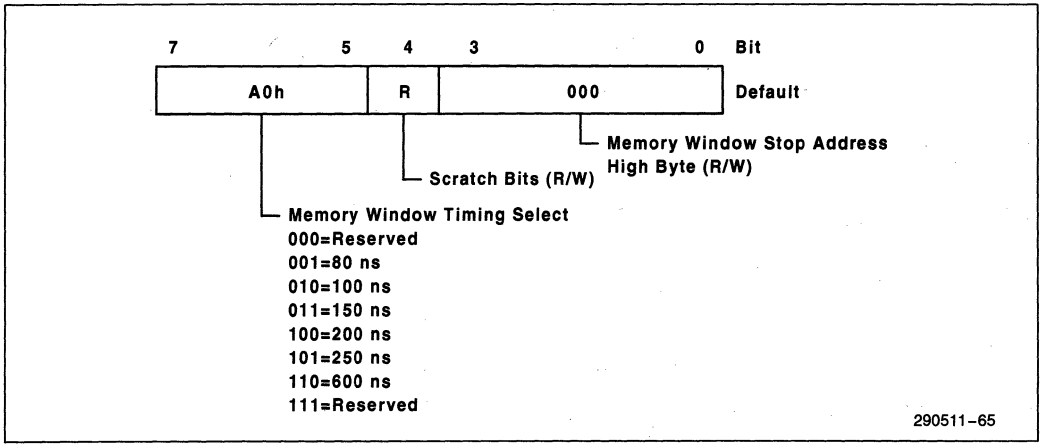


Figure 35. System Memory Address Mapping Windows 0–4 Stop High Byte Registers

3.2.4.5 OFFL[4:0]—Card Memory Offset Address 0-4 Low Byte Registers

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	14h	1Ch	24h	2Ch	34h
Socket B	54h	5Ch	64h	6Ch	74h
Socket C	94h	9Ch	A4h	ACh	B4h
Socket D	D4h	DCh	E4h	ECh	F4h

Default value: 00h
Access: Read/Write
Size: 8 bits

These five registers contain the low order address bits that are added to system address bits A[19:12] to generate the memory addresses for the PC Cards.

Bits[7:0]: Card Memory Offset Address
These bits are added to PCI memory address bits A[19:12] to generate the memory address for the PC Card.

3.2.4.6 OFFH[4:0]—Card Memory Offset Address 0 High Byte Registers

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	15h	1Dh	25h	2Dh	35h
Socket B	55h	5Dh	65h	6Dh	75h
Socket C	95h	9Dh	A5h	ADh	B5h
Socket D	D5h	DDh	E5h	EDh	F5h

Default value: 00h
Access: Read/Write
Size: 8 bits

Bits[5:0] of the registers are added to PCI memory address bits A[23:20] to generate the memory addresses for the PC Cards. The registers also control the PC Card memory software write protect for the corresponding system memory windows, and select whether the memory windows are mapped to attribute memory, or to common memory on the PC Cards.

Bit 7: Write Protect
When this bit is set to 1, write operations to the PC Card through the corresponding system memory window are inhibited. When set to 0, write operations are allowed. The WP Switch on the memory card sets the Memory Write Protect bit in the Interface Status Register, but does not alone block memory write cycles.

Bit 6: Register Active
When this bit is set to 1, accesses to the system memory window result in attribute memory on the PC Card being accessed by asserting REG low. When set to 0, accesses to the system memory result in common memory on the PC Card being accessed by driving REG high.

Bits[5:0]: Card Memory Offset Address
These bits are added to PCI memory address bits A[23:20] to generate the memory address for the PC Card.

4.0 ELECTRICAL CHARACTERISTICS

4.1 Maximum Ratings

Case Temperature Under Bias . . . −65°C to +110°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltages
with Respect to Ground . . . −0.5V to V_{CC} + 0.5V
Voltage On Any Pin . . . . . −0.5V to V_{CC} + 0.5V
Power Dissipation 1.0W

The junction temperature for the PPEC is 95°C with a case temperature of 85°C.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2 Characteristics

4.2.1 PCI INTERFACE DC SPECIFICATIONS

Table 12. PCI Interface DC Characteristics (V_{CC} = 5V*5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
V_{IL}	Input Low Voltage		0.8	V		
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V		
V_{OL}	Output Low Voltage		0.55	V	I_{OL} = 6 mA	
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2.0 mA	
I_{IL}	Low-Level Input Current		−70	μA	V_{IN} = 0.5V	
I_{IH}	High-Level Input Current		70	A	V_{IN} = 2.7V	
C_{IN}	Input Capacitance		10	pF		
C_{OUT}	Output Capacitance		10	pF		
C_{CLK}	PCICLK Input Capacitance		12	pF		
I_{CC}	V_{CC} Supply Current		200	mA		

4.2.2 PCMCIA INTERFACE DC SPECIFICATIONS

Table 13. PCMCIA Interface DC Specifications (V_{CC} = 5V*5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
V_{IL}	Input Low Voltage		0.8	V		
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V		
V_{OL1}	Output Low Voltage		0.5	V	I_{OL} = −8 mA	1
V_{OH1}	Output High Voltage	2.4 2.8	V_{CC}3/5	V	I_{OH} = 4 mA I_{OH} = 2 mA	1,3,4
V_{OL2}	Output Low Voltage		0.5	V	I_{OL} = −4 mA	2
V_{OH2}	Output High Voltage	2.4 2.8	V_{CC}3/5	V	I_{OH} = 2 mA I_{OH} = 1 mA	2,3,4
I_{IL}	Low-level Input Current		−10	A		
I_{IH}	High-level Input Current		10	A		
C_{IN}	Capacitance Input		10	pF		
C_{OUT}	Capacitance Output		10	pF		
I_{CC}	V_{CC} Supply Current		200	mA		

NOTES:
1. V_{OL1} and V_{OH1} apply to PCMCIA signals that are shared in Mode 1: REG#, OE#, IOWR#, IORD#, CDATA[15:0], CADR[25:0].
2. V_{OL2} and V_{OH2} apply to all PCMCIA signals that are not listed in Note 1.
3. V_{OH} = 2.8V is the minimum high-state voltage specified by the PCMCIA specification.
4. V_{CC}3/5 is the voltage applied to the SOCKETPWR pins. This voltage may be set at 5V ±10% or 3.3V ±0.3V.

4.3 AC Characteristics

4.3.1 CLOCK SIGNAL AC SPECIFICATIONS

Table 14. Clock Signal AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Note	Figure
t1a	Cycle Time	30		ns		36
t1b	High Time	12		ns	At 2.0V	36
t1c	Low Time	12		ns	At 0.8V	36
t1d	Rise Time		3	ns	0.8V to 2.0V	36
t1e	Fall Time		3	ns	2.0V to 0.8V	36

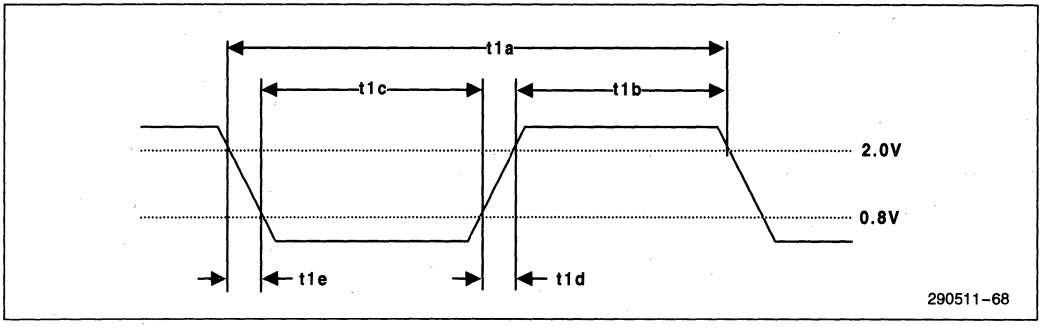


Figure 36. PCICLK Timing

4.3.2 PCI INTERFACE AC SPECIFICATIONS

Table 15. PCI Interface AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Note	Figure
	PCIRST#					
t2a	Pulse Width	1		ms		37
t2b	PCICLK Active Setup to PCIRST# Negated	100		s		37
	AD[31:0], C/BE[3:0], FRAME#, IRDY#, PAR, PERR#, SERR#, TRDY#, DEVSEL#, STOP#, PCILOCK#, IDSEL					
t3a	Delay from PCICLK Rising	2	11	ns		38
t3b	Setup to PCICLK Rising	7		ns		38
t3c	Hold from PCICLK Rising	0		ns		38

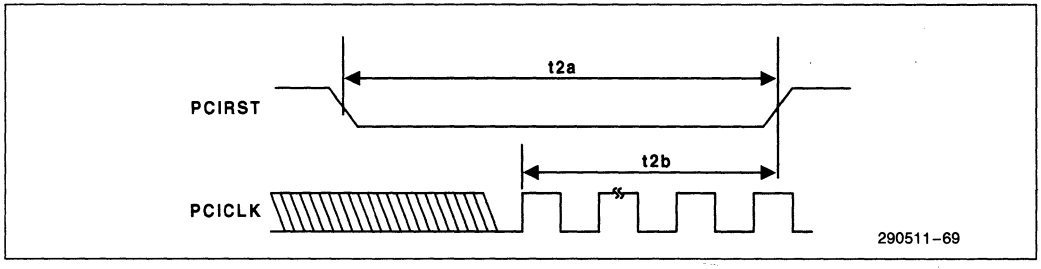


Figure 37. PCIRT# Timing

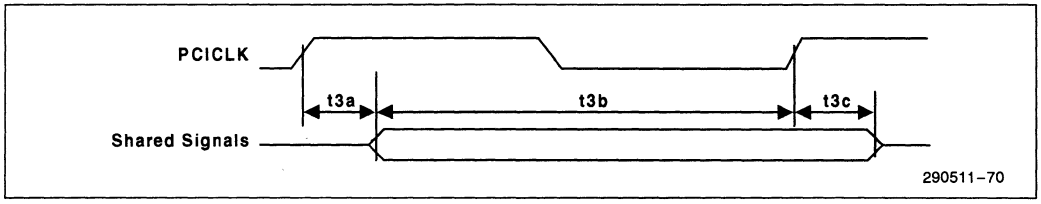


Figure 38. Shared Signal Timing

4.3.3 SYSTEM SIGNAL AC SPECIFICATIONS

Table 16. System Signal AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Note	Figure
	IRQx					
t4a	Card Status change to IRQx/INTx# Valid		2 CLKs + 20	ns	Card Status change can be caused by any CSC event, such as the assertion of BVD[1,0], CD[1,0], STSCHG#, etc.	39
t4b	PC Card IREQ# to IRQx/INTx# Delay		35	ns		39
	SPKROUT#					
t4c	SPKR# to SPKROUT# Delay		35	ns		39

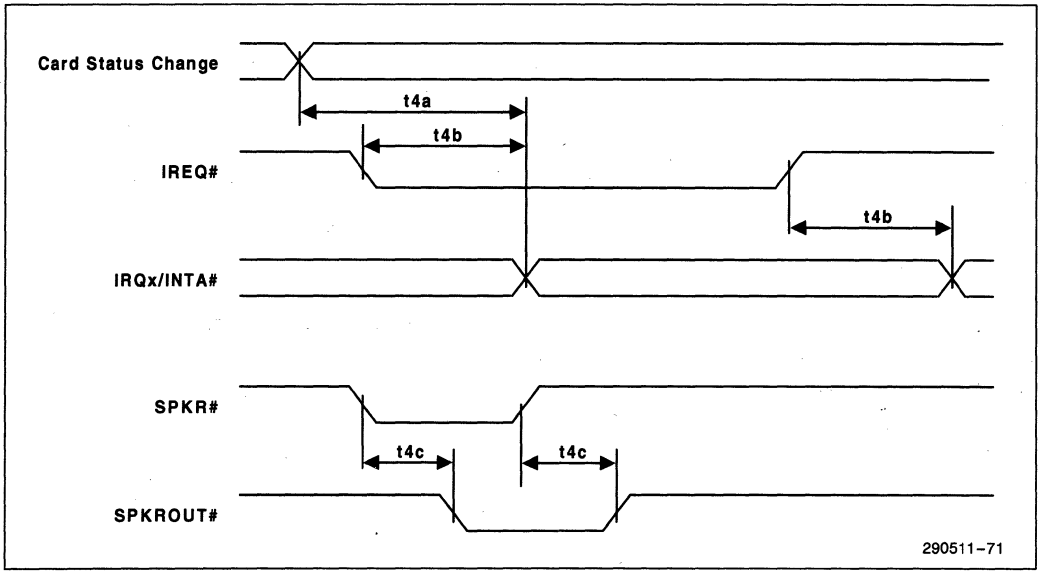


Figure 39. System Signal Timing

4.3.4 POWER WRITE SIGNAL AC CHARACTERISTICS

Table 17. Power Write Signal AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Note	Figure
t5a	Data Valid Setup to PWRWR# Asserted	5		ns		40
t5b	Data Valid Hold from PWRWR# Negated	1		CLK		40
t5c	Pulse Width	5		CLK		40

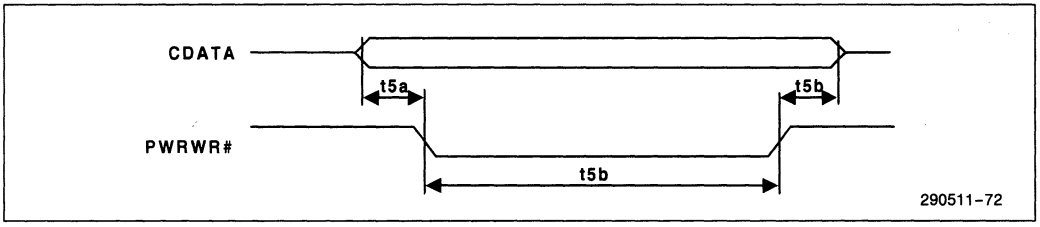


Figure 40. Power Write Signal Timing

4.3.5 PCMCIA MEMORY SIGNAL AC CHARACTERISTICS

Table 18 lists signal timing parameters for memory read and write operations. All of the parameters listed in the table apply to Common Memory operations.

Attribute Memory writes and 5.0V Attribute Memory reads use the timing for 250ns cards (see *Notes* column); 3.3V Attribute Memory reads use the timing for 600 ns cards.

Table 18. PCMCIA Memory Signal AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Note	Figure
	CDATA[15:0]					
t7a	Valid Setup to WE# Asserted	2 CLKs − 20 2 CLKs − 20 2 CLKs − 20 2 CLKs − 20 3 CLKs − 20(1) 4 CLKs − 20(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	42
t7b	Hold from WE# Negated	1 CLK − 10 1 CLK − 10 2 CLKs − 10 2 CLKs − 10 2 CLKs − 10(1) 5 CLKs − 10(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	42

Table 18. PCMCIA Memory Signal AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)
(Continued)

Symbol	Parameter	Min	Max	Unit	Note	Figure
	CADR[25:0],REG#,CE[2:1]#,EXTDIR					
t6a	Valid Setup to OE# Asserted	1 CLK − 20 2 CLKs − 20 2 CLKs − 20 2 CLKs − 20 3 CLKs − 20(1) 4 CLKs − 20(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	41
t6b	Valid Setup to data Latched	4 CLKs − 20 5 CLKs − 20 6 CLKs − 20 8 CLKs − 20 10 CLKs − 20(1) 22 CLKs − 20(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	41
t7c	Valid Setup to WE# Asserted	2 CLKs − 20 2 CLKs − 20 2 CLKs − 20 2 CLKs − 20 3 CLKs − 20(1) 4 CLKs − 20(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	42
t7d	Hold from WE# Negated	1 CLK − 10 1 CLK − 10 2 CLKs − 10 2 CLKs − 10 2 CLKs − 10(1) 5 CLKs − 10(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	42
	OE#					
t6c	OE# Asserted to Data Latched	3 CLKs − 20 3 CLKs − 20 4 CLKs − 20 6 CLKs − 20 7 CLKs − 20(1) 18 CLKs − 20(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	41
t6d	Data Latched to OE# Negated	0		ns		41
	WE#					
t7e	Pulse Width	3 CLKs + 0 3 CLKs + 0 3 CLKs + 0 5 CLKs + 0 6 CLKs + 0(1) 11 CLKs + 0(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	42

Table 18. PCMCIA Memory Signal AC Characteristics
(V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C) (Continued)

Symbol	Parameter	Min	Max	Unit	Note	Figure
	WAIT#					
t6e	WAIT# Negated to Data Latched	1 CLK + 0	2 CLKs + 10	ns	All Cards	41
t7f	WAIT# Negated to WE# Negated	1 CLK + 0	2 CLKs + 10	ns	All Cards	42
t6f	Valid Delay from CADR[25:0] Valid		50			41

NOTES:
1. Applies to Common Memory reads and writes, Attribute Memory writes, and 5.0V Attribute Memory reads.
2. Applies to Common Memory reads and writes, and 3.3V Attribute Memory reads.

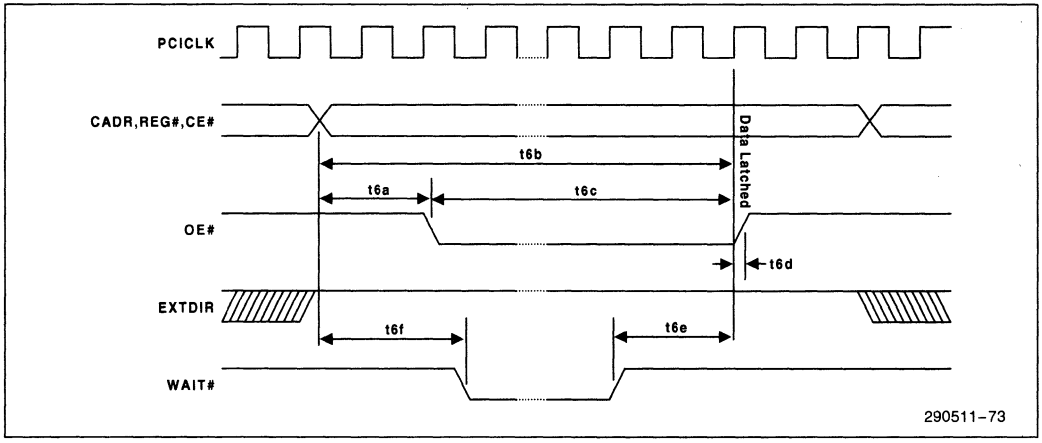


Figure 41. Memory Read Timing

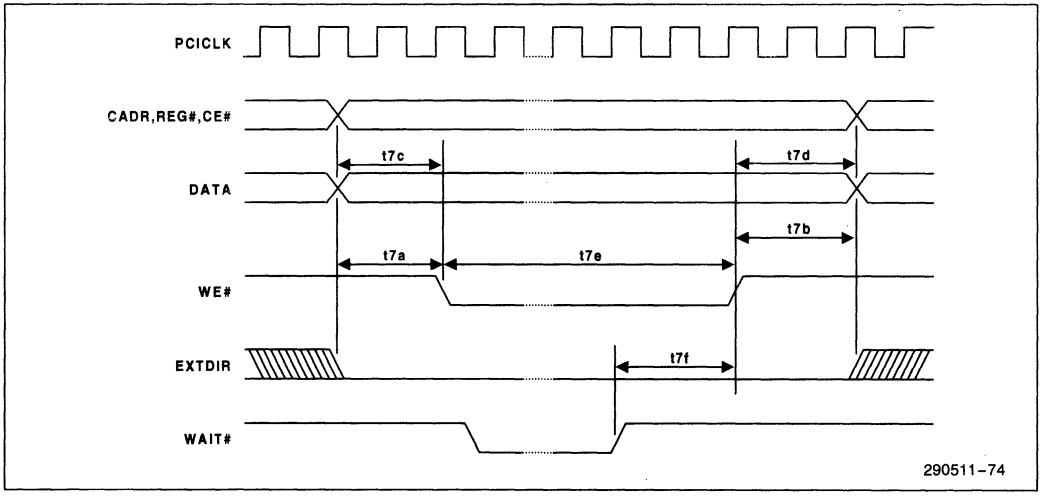


Figure 42. Memory Write Timing

4.3.6 PCMCIA I/O SIGNAL AC CHARACTERISTICS

Table 19 lists signal timing parameters for I/O read and write operations.

Table 19. PCMCIA I/O Signal AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note	Figure
	CDATA[15:0]					
t9a	Valid Setup to IOWR# Asserted	4 CLKs − 20		ns		44
t9b	Hold from IOWR# Negated	2 CLKs − 10		ns		44
	CADR[25:0],REG#,CE[2:1]#,EXTDIR					
t8a	Valid Setup to IORD# Asserted	4 CLKs − 20				43
t8b	Valid Setup to Data Latched	10 CLKs − 20				43
t9c	Valid Setup to IOWR# Asserted	4 CLKs − 20				44
t9d	Hold from IOWR# Negated	2 CLKs − 10				44
	IORD#					
t8c	IORD# Asserted to Data Latched	6 CLKs − 20				43
t8d	Data Latched to OE# Negated	0				43
	IOWR#					
t9e	Pulse Width	6 CLKs + 0				44
	WAIT#					
t8e	WAIT# Negated to Data Latched	1 CLK + 0				43
t9f	WAIT# Negated to IOWR# Negated	1 CLK + 0				44
t8f,t9g	Valid Delay from IORD#/IOWR# Valid		50			43, 44
	IOIS16#					
t10g	Valid Delay from CADR[25:0] Valid		50			44

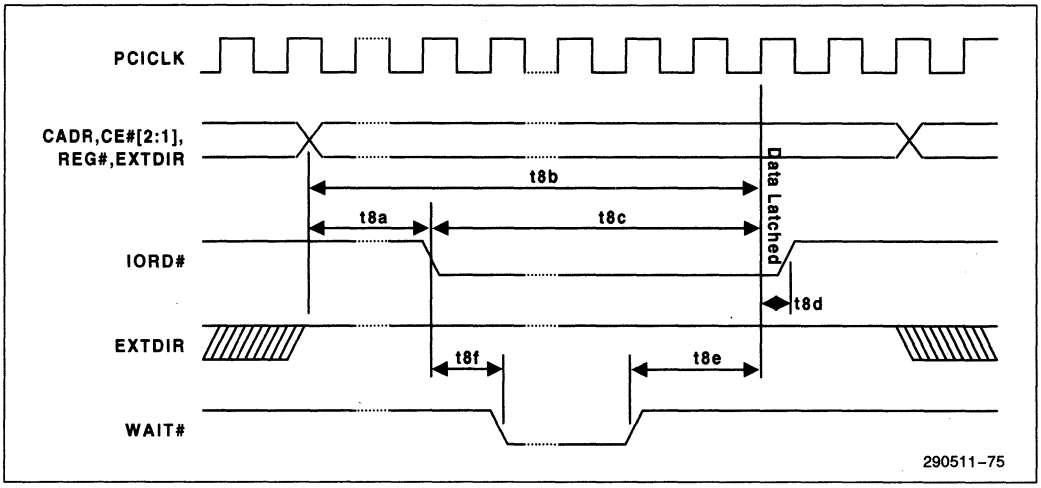


Figure 43. I/O Read Timing

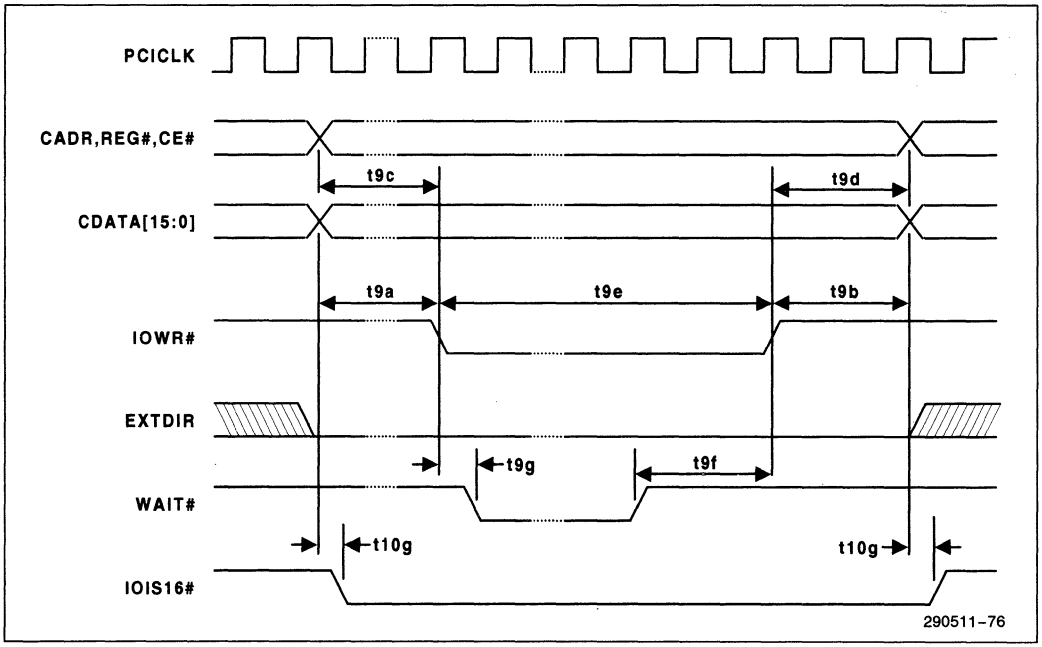


Figure 44. I/O Write Timing

4.3.7 IDE SIGNAL AC CHARACTERISTICS

Table 20 lists signal timing parameters with respect to PCI clock edges for IDE read and write operations. Note that integral number of clock delays are programmable for all IDE signals.

Table 20. IDE Signal AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note	Figure
t10a	DIOR#/DIOW# Delay from PCI Clock	2	20	ns		45
t10b	Address/Data/CS Delay from PCI Clock	2	30	ns		45
T_{pw}	DIOR#/DIOW# Duration	1	8	CLK	Programmable	45
T_{su}	Address/Data/CS Setup to DIOR#/DIOW#	1	4	CLK	Programmable	45
T_{cyc}	Address/Data/CS Cycle Time	5	31	CLK	Programmable	45

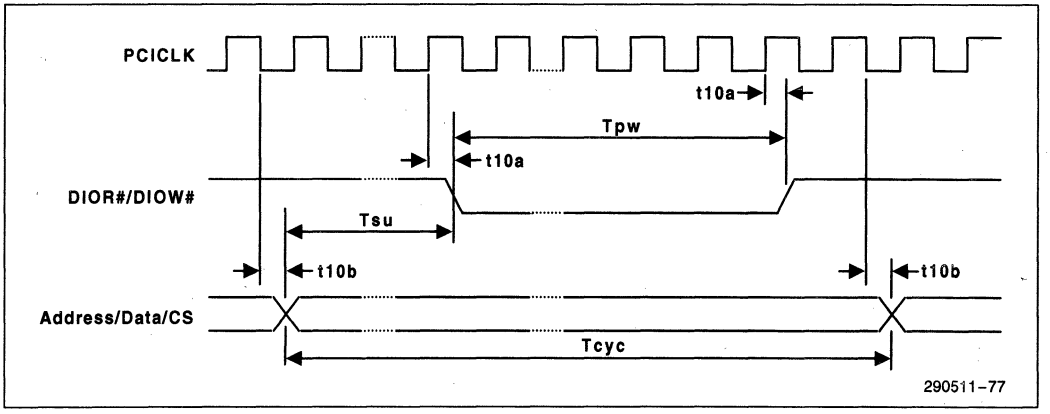


Figure 45. IDE Timing

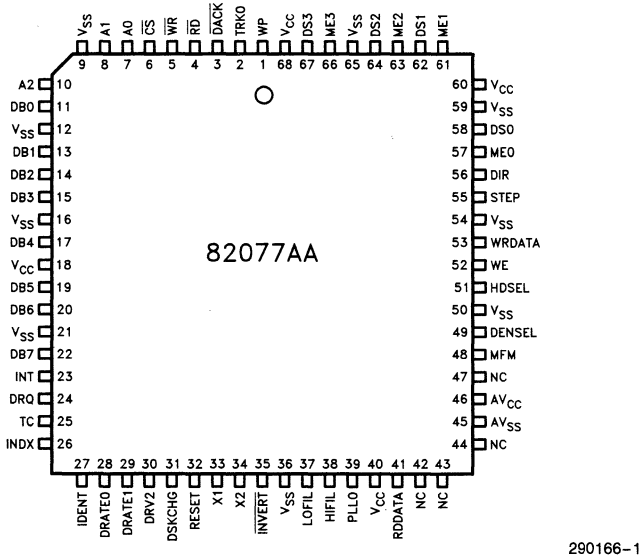
82077AA
CHMOS SINGLE-CHIP FLOPPY DISK CONTROLLER

- **Single-Chip Floppy Disk Solution**
  - **— 100% PC AT* Compatible**
  - **— 100% PS/2* Compatible**
  - **— 100% PS/2 Model 30 Compatible**
  - **— Integrated Drive and Data Bus Buffers**
- **Integrated Analog Data Separator**
  - **— 250 Kbits/sec**
  - **— 300 Kbits/sec**
  - **— 500 Kbits/sec**
  - **— 1 Mbits/sec**
- **High Speed Processor Interface**
- **Perpendicular Recording Support**
- **Integrated Tape Drive Support**
- **12 mA Host Interface Drivers, 40 mA Disk Drivers**
- **Four Fully Decoded Drive Select and Motor Signals**
- **Programmable Write Precompensation Delays**
- **Addresses 256 Tracks Directly, Supports Unlimited Tracks**
- **16 Byte FIFO**
- **68-Pin PLCC**
  (See Packaging Spec., Order #240800, Package Type N)

2

The 82077AA floppy disk controller has completely integrated all of the logic required for floppy disk control. The 82077AA, a 24 MHz crystal, a resistor package and a device chip select implements a PC AT or PS/2 solution. All programmable options default to compatible values. The dual PLL data separator has better performance than most board level/discrete PLL implementations. The FIFO allows better system performance in multi-master systems (e.g. PS/2, EISA). The 82077AA is available in three versions—82077AA-5, 82077AA and 82077AA-1. 82077AA-1 has all features listed in this data sheet. It supports both tape drives and 4 Mb floppy drives. The 82077AA supports 4 Mb floppy drives and is capable of operation at all data rates through 1 Mbps. The 82077AA-5 supports 500/300/250 Kbps data rates for high and low density floppy drives.

The 82077AA is fabricated with Intel's CHMOS III technology and is available in a 68-lead PLCC (plastic) package.



290166-1

Figure 1. 82077AA Pinout

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The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

May 1994
Order Number: 290166-007

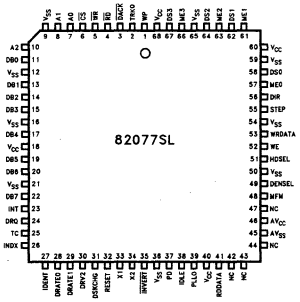
82077SL
CHMOS SINGLE-CHIP FLOPPY DISK CONTROLLER

- **Completely Compatible with Industry Standard 82077AA**
- **Single-Chip Laptop Desktop Floppy Disk Controller Solution**
  - **— 100% PC AT* Compatible**
  - **— 100% PS/2* Compatible**
  - **— 100% PS/2 Model 30 Compatible**
  - **— Fully Compatible with Intel's 386SL Microprocessor SuperSet**
  - **— Integrated Drive and Data Bus Buffers**
- **Power Management Features**
  - **— Application Software Transparency**
  - **— Programmable Powerdown Command**
  - **— Auto Powerdown and Wakeup Modes**
  - **— Two External Power Management Pins**
  - **— Typical Power Consumption in Power Down: 10 μA**
- **High Speed Processor Interface**
- **Integrated Analog Data Separator**
  - **— 250 Kbits/sec**
  - **— 300 Kbits/sec**
  - **— 500 Kbits/sec**
  - **— 1 Mbits/sec**
- **Programmable Crystal Oscillator for On or Off**
- **Integrated Tape Drive Support**
- **Perpendicular Recording Support**
- **12 mA Host Interface Drivers, 40 mA Disk Drivers**
- **Four Fully Decoded Drive Select and Motor Signals**
- **Programmable Write Precompensation Delays**
- **Addresses 256 Tracks Directly, Supports Unlimited Tracks**
- **16 Byte FIFO**
- **68-Pin PLCC**
  (See Packaging Handbook Order Number #240800, Package Type N)

The 82077SL, a 24 MHz crystal, a resistor package, and a device chip select implements a complete laptop solution. All programmable options default to 82077AA compatible values. The dual PLL data separator has better performance than most board level/discrete PLL implementations. The FIFO allows better system performance in multi-master systems (e.g., Microchannel, EISA).

The 82077SL is a superset of 82077AA. The 82077SL incorporates power management features while maintaining complete compatibility with the 82077AA/8272A floppy disk controllers. It contains programmable power management features while integrating all of the logic required for floppy disk control. The power management features are transparent to any application software. The 82077SL is available in three versions—82077SL-5, 82077SL and 82077SL-1. 82077SL-1 has all features listed in this data sheet. It supports both tape drives and 4 MB floppy drives. The 82077SL supports 4 MB floppy drives and is capable of operation at all data rates through 1 Mbps. The 82077SL-5 supports 500/300/250 Kbps data rates for high and low density floppy drives.

The 82077SL is fabricated with Intel's advanced CHMOS III technology and is available in a 68-lead PLCC (plastic) package.



290410-1

Figure 1. 82077SL Pinout

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May 1994
Order Number: 290410-004

82077SL CHMOS Single-Chip Floppy Disk Controller

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Table 1. 82077SL Pin Description

Symbol	Pin #	I/O	Description
HOST INTERFACE			
RESET	32	I	**RESET:** A high level places the 82077SL in a known idle state. All registers are cleared except those set by the Specify command.
$\overline{CS}$	6	I	**CHIP SELECT:** Decodes base address range and qualifies $\overline{RD}$ and $\overline{WR}$ inputs.
A0 A1 A2	7 8 10	I	**ADDRESS:** Selects one of the host interface registers:

A2	A1	A0	Access Type	Register	
0	0	0	R	Status Register A	SRA
0	0	1	R	Status Register B	SRB
0	1	0	R/W	Digital Output Register	DOR
0	1	1	R/W	Tape Drive Register	TDR
1	0	0	R	Main Status Register	MSR
1	0	0	W	Data Rate Select Register	DSR
1	0	1	R/W	Data (First In First Out)	FIFO
1	1	0		Reserved	
1	1	1	R	Digital Input Register	DIR
1	1	1	W	Configuration Control Register	CCR

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	11 13 14 15 17 19 20 22	I/O	**DATA BUS:** Data bus with 12 mA drive
$\overline{RD}$	4	I	**READ:** Control signal
$\overline{WR}$	5	I	**WRITE:** Control signal
DRQ	24	O	**DMA REQUEST:** Requests service from a DMA controller. Normally active high, but goes to high impedance in AT and Model 30 modes when the appropriate bit is set in the DOR.
$\overline{DACK}$	3	I	**DMA ACKNOWLEDGE:** Control input that qualifies the $\overline{RD}$, $\overline{WR}$ inputs in DMA cycles. Normally active low, but is disabled in AT and Model 30 modes when the appropriate bit is set in the DOR.
TC	25	I	**TERMINAL COUNT:** Control line from a DMA controller that terminates the current disk transfer. TC is accepted only while $\overline{DACK}$ is active. This input is active high in the AT, and Model 30 modes and active low in the PS/2 mode.
INT	23	O	**INTERRUPT:** Signals a data transfer in non-DMA mode and when status is valid. Normally active high, but goes to high impedance in AT, and Model 30 modes when the appropriate bit is set in the DOR.
X1 X2	33 34		**CRYSTAL 1,2:** Connection for a 24 MHz fundamental mode parallel resonant crystal. X1 may be driven with a MOS level clock and X2 would be left unconnected.

Table 1. 82077SL Pin Description (Continued)

Symbol	Pin #	I/O	Description
HOST INTERFACE (Continued)			
IDENT	27	I	**IDENTITY:** Upon Hardware RESET, this input (along with MFM pin) selects between the three interface modes. After RESET, this input selects the type of drive being accessed and alters the level on DENSEL. The MFM pin is also sampled at Hardware RESET, and then becomes an output again. Internal pull-ups on MFM permit a no connect. IDENT / MFM / INTERFACE 1 / 1 or NC / AT Mode 1 / 0 / ILLEGAL 0 / 1 or NC / PS/2 Mode 0 / 0 / Model 30 Mode **AT MODE:** Major options are: enables DMA Gate logic, TC is active high, Status Registers A & B not available. **PS/2 MODE:** Major options are: No DMA Gate logic, TC is active low, Status Registers A & B are available. **MODEL 30 MODE:** Major options are: enable DMA Gate logic, TC is active high, Status Registers A & B available. After Hardware reset this pin determines the polarity of the DENSEL pin. IDENT at a logic level of "1", DENSEL will be active high for high (500 Kbps/1 Mbps) data rates (typically used for 5.25″ drives). IDENT at a logic level of "0", DENSEL will be active low for high data rates (typically used for 3.5″ drives). This assumes the $\overline{\text{INVERT}}$ pin to be tied to ground.
DISK CONTROL (All outputs have 40 mA drive capability)			
$\overline{\text{INVERT}}$	35	I	**INVERT:** Strapping option. Determines the polartity of **all** signals in this section. Should be strapped to ground when using the internal buffers and these signals become active LOW. When strapped to VCC, these signals become active high and external inverting drivers and receivers are required.
ME0 ME1 ME2 ME3	57 61 63 66	O	**ME0–3:** Decoded Motor enables for drives 0–3. The motor enable pins are directly controlled via the Digital Output Register.
DS0 DS1 DS2 DS3	58 62 64 67	O	**DRIVE SELECT 0–3:** Decoded drive selects for drives 0–3. These outputs are decoded from the select bits in the Digital Output Register and gated by ME0–3.
HDSEL	51	O	**HEAD SELECT:** Selects which side of a disk is to be used. An active level selects side 1.
STEP	55	O	**STEP:** Supplies step pulses to the drive.
DIR	56	O	**DIRECTION:** Controls the direction the head moves when a step signal is present. The head moves toward the center if active.
WRDATA	53	O	**WRITE DATA:** FM or MFM serial data to the drive. Precompensation value is selectable through software.
WE	52	O	**WRITE ENABLE:** Drive control signal that enables the head to write onto the disk.
DENSEL	49	O	**DENSITY SELECT:** Indicates whether a low (250/300 Kbps) or high (500 Kbps/1 Mbps) data rate has been selected.
DSKCHG	31	I	**DISK CHANGE:** This input is reflected in the Digital Input Register.

Table 1. 82077SL Pin Description (Continued)

Symbol	Pin#	I/O	Description
DISK CONTROL (All outputs have 40 mA drive capability) (Continued)			
DRV2	30	I	**DRIVE2:** This indicates whether a second drive is installed and is reflected in Status Register A.
TRK0	2	I	**TRACK0:** Control line that indicates that the head is on track 0.
WP	1	I	**WRITE PROTECT:** Indicates whether the disk drive is write protected.
INDX	26	I	**INDEX:** Indicates the beginning of the track.
PLL SECTION			
RDDATA	41	I	**READ DATA:** Serial data from the disk. INVERT also affects the polarity of this signal.
MFM	48	I/O	**MFM:** At Hardware RESET, aids in configuring the 82077SL. Internal pull-up allows a no connect if a "1" is required. After reset this pin becomes an output and indicates the current data encoding/decoding mode (Note: If the pin is held at logic level "0" during hardware RESET it must be pulled to "1" after reset to enable the output. The pin can be released on the falling edge of hardware RESET to enable the output). MFM is active high (MFM).
DRATE0 DRATE1	28 29	O	**DATARATE0–1:** Reflects the contents of bits 0,1 of the Data Rate Register. (Drive capability of +6.0 mA @ 0.4V and −4.0 mA @ 2.4V)
PLL0	39	I	**PLL0:** This input optimizes the data separator for either floppy disks or tape drives. A "1" (or V_{CC}) selects the floppy mode, a "0" (or GND) selects tape mode.
POWERDOWN STATUS			
IDLE	38	O	**IDLE:** This pin indicates that the part is in the IDLE state and can be powered down. IDLE state is defined as MSR = 80H, INT = 0, and the head being "unloaded" (as defined in Section 6.2.6). Whenever the part is in this state, IDLE pin is active high. If the part is powered down by the Auto Mode, IDLE pin is set high and if the part is powered down by setting the DSR POWERDOWN bit, IDLE pin is set low.
PD	37	O	**POWERDOWN:** This pin is active high whenever the part is in powerdown state, either via DSR POWERDOWN bit or via the Auto Mode. This pin can be used to disable external oscillator's output.
MISCELLANEOUS			
VCC	18 40 60 68		**Voltage:** +5V
GND	9 12 16 21 36 50 54 59 65		**Ground**
AVCC	46		**Analog Supply**
AVSS	45		**Analog Ground**
NC	42 43 44 47		**No Connection:** These pins **MUST** be left unconnected.

1.0 INTRODUCTION

The 82077SL is a single-chip floppy disk controller for portable PC designs, PC-AT, Microchannel and EISA systems. The 82077SL includes all the power management features necessary to implement a powerful laptop and notebook solution. The 82077SL is fully compatible with the 82077AA. The pin out remains the same with the exception of two new powerdown status pins, PD and IDLE. These pins will replace the LOFIL and HIFIL pins on the 82077AA that are used to connect an external capacitor.

The 82077SL, a 24 MHz crystal, a resistor package and a chip select implement a complete design. The power management features of the 82077SL are designed to be transparent to all application software. The 82077SL will seem awake to the software even when it is in powerdown mode. All drive control signals are fully decoded and have 40 mA drive buffers with selectable polarity. Signals returned from the drive are sent through on-chip input buffers with hysteresis for noise immunity. The integrated analog data separator needs no external compensation of components, yet allows for wide motor variation with exceptionally low soft error rates. The microprocessor interface has 12 mA drive buffers on the data bus plus 100% hardware register compatibility for PC-AT and Microchannel systems. The 16-byte FIFO with programmable thresholds is extremely useful in multi-master systems (Microchannel, EISA) or systems with large bus latency.

Upon hardware reset, (Pin 32) the 82077SL defaults to 8272A functionality. Figure 1-1 is a block diagram of the 82077SL.

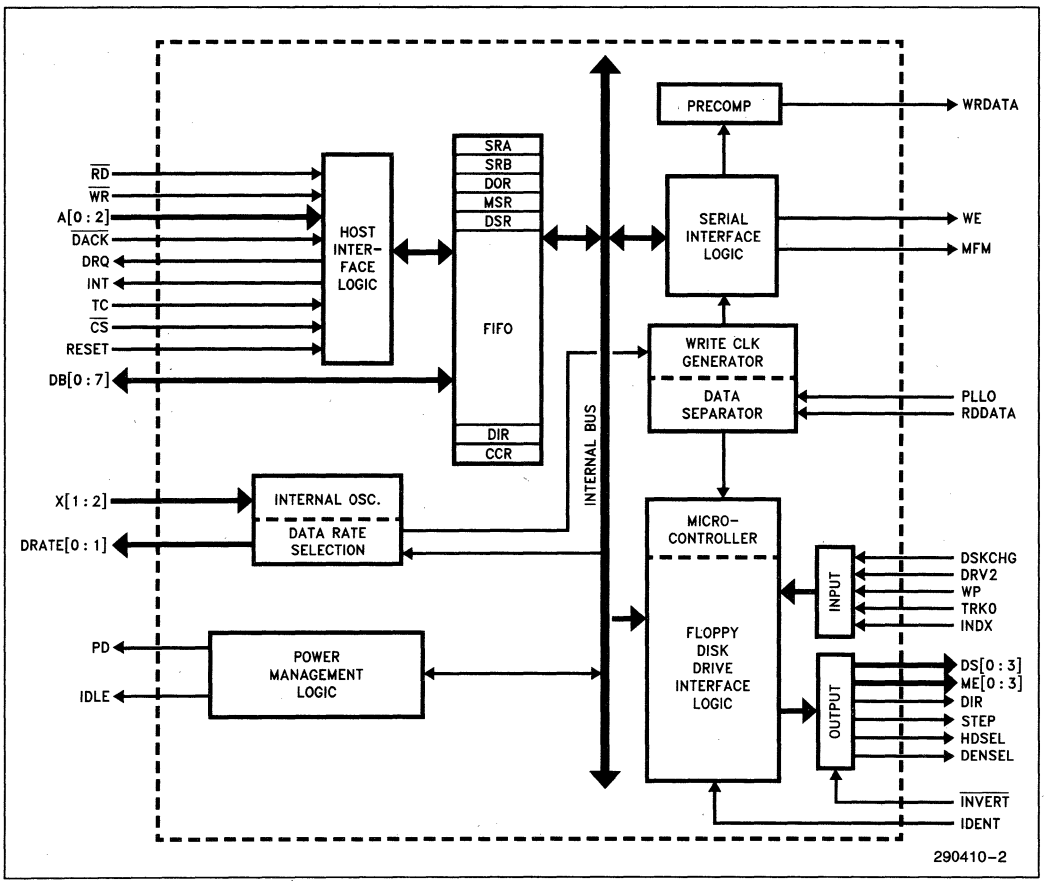


Figure 1-1. 82077SL Block Diagram

1.1 Perpendicular Recording Mode

An added capability of the 82077SL is the ability to interface directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method by orienting the magnetic bits vertically. This scheme packs in more data bits for the same area.

The 82077SL with perpendicular recording drives can read standard 3.5" floppies as well as read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the 82077SL into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires the 1 Mbps data rate of the 82077SL. At this data rate, the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

1.2 Power Management Scheme

While maintaining compatibility with 82077AA, the 82077SL contains a powerful set of features for conserving power. This enables the 82077SL to play an important role in the power sensitive environment of portable personal computers. These features are transparent to any application software.

The 82077SL supports two powerdown modes—direct powerdown and automatic powerdown. Direct powerdown refers to direct action by the software to powerdown without dependence on external factors. Automatic powerdown results from 82077SL's monitoring of the current conditions according to a previously programmed mode. The 82077SL contains a new powerdown command that via programming can be used to invoke auto powerdown. 82077SL is powered down whenever a set of conditions are satisfied. Any hardware reset disables the automatic powerdown command. Software resets have no effect on the POWERDOWN command parameters.

The 82077SL also supports powerdown of its internal crystal oscillator independent of the powerdown modes described above. By setting bit 5 in DSR register, the internal oscillator is turned off. This bit has sole control of the oscillator powerdown. This allows the internal oscillator to be turned off when an external oscillator is used.

2.0 MICROPROCESSOR INTERFACE

The interface consists of the standard asynchronous signals: $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0–A2, INT, DMA control and a data bus. The address lines select between configuration registers, the FIFO and control/status registers. This interface can be switched between PC AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC-AT.

2.1 Status, Data and Control Registers

As shown below, the base address range is supplied via the $\overline{CS}$ pin. For PC-AT or PS/2 designs, the primary and secondary address ranges are 3F0 Hex to 37F Hex and 370 Hex to 377 Hex respectively.

A2	A1	A0	Access Type	Register	
0	0	0	R	Status Register A	SRA
0	0	1	R	Status Register B	SRB
0	1	0	R/W	Digital Output Register	DOR
0	1	1	R/W	Tape Drive Register	TDR
1	0	0	R	Main Status Register	MSR
1	0	0	W	Data Rate Select Register	DSR
1	0	1	R/W	Data (First In First Out)	FIFO
1	1	0		Reserved	
1	1	1	R	Digital Input Register	DIR
1	1	1	W	Configuration Control Register	CCR

In the following sections, the various registers are shown in their powerdown state. The "UC" notation stands for a value that is returned without change from the active mode. The notation " * " means that the value is reflecting the actual status of the 82077SL, but the value is determinable in the powerdown state. "N/A" reflects the values of the pins indicated. "X" indicates that the value is undefined.

2.1.1a STATUS REGISTER A (SRA, PS/2 MODE)

This register is read-only and monitors the state of the interrupt pin and several disk interface pins. This register is part of the register set, and is not accessible in PC-AT mode.

This register can be accessed during powerdown state without waking up the 82077SL from its powerdown state.

Bits	7	6°	5	4°	3	2°	1°C	0
Function	INT PENDING	$\overline{DRV2}$	STEP	$\overline{TRK0}$	HDSEL	$\overline{INDX}$	$\overline{WP}$	DIR
H/W Reset State	0	N/A	0	N/A	0	N/A	N/A	0
Auto PD State	0*	UC	0*	1	0*	1	1	0*

The INT PENDING bit is used by software to monitor the state of the 82077SL INTERRUPT pin. The bits marked with a " ° " reflect the state of drive signals on the cable and are independent of the state of the $\overline{INVERT}$ pin.

The INT PENDING bit is low by definition for 82077SL to be in powerdown. The bits reflecting the floppy disk drive input pins (TRK0, INDEX and WP) are forced to an inactive state. The floppy disk drive outputs (HDSEL, STEP, and DIR) also go to their inactive, default state.

As a read-only register, there is no default value associated with a reset other than some drive bits will change with a reset. The INT PENDING, STEP, HDSEL, and DIR bits will be low after reset.

2.1.1b STATUS REGISTER A (SRA, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	INT PENDING	DRQ	STEP F/F	TRK0	$\overline{HDSEL}$	INDX	WP	$\overline{DIR}$
H/W Reset State	0	0	0	N/A	1	N/A	N/A	1
Auto PD State	0*	0*	0	0	1*	0	0	1*

This register has the following changes in PS/2 Model 30 Mode. Disk interface pins (Bits 0, 1, 2, 3, & 4) are inverted from PS/2 Mode. The DRQ bit monitors the status of the DMA Request pin. The STEP bit is latched with the Step output going active and is cleared with a read to the DIR register, Hardware or Software RESET.

The DRQ bit is low by definition for 82077SL to be in powerdown. The bits reflecting the floppy disk drive input pins (TRK0, INDEX and WP) are forced to reflect an inactive state. The floppy disk drive outputs (HDSEL, STEP, and DIR) also go to their inactive, default state.

2.1.2a STATUS REGISTER B (SRB, PS/2 MODE)

This register is read-only and monitors the state of several disk interface pins. This register is part of the PS/2 register set, and is not accessible in PC-AT mode.

Bits	7	6	5	4	3*	2	1	0
Function	1	1	DRIVE SEL 0	WRDATA TOGGLE	RDDATA TOGGLE	WE	MOT EN1	MOT EN0
H/W Reset State	1	1	0	0	0	0	0	0
Auto PD State	1	1	UC	0	0	0*	0	0

As the only drive input, RDDATA TOGGLE's activity is independent of the $\overline{INVERT}$ pin level and reflects the level as seen on the cable.

The two TOGGLE bits do not read back the state of their respective pins directly. Instead, the pins drive a Flip/Flop which produces a wider and more reliably read pulse. Bits 6 and 7 are undefined and always return a 1.

After any reset, the activity on the TOGGLE pins are cleared. Drive select and Motor bits cleared by the RESET pin and not software resets.

2.1.2b STATUS REGISTER B (SRB, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	$\overline{DRV2}$	$\overline{DS1}$	$\overline{DS0}$	WRDATA F/F	RDDATA F/F	WE F/F	$\overline{DS3}$	$\overline{DS2}$
H/W Reset State	N/A	1	1	0	0	0	1	1
Auto PD State	UC	UC	UC	0	0	0	UC	UC

This register has the following changes in Model 30 Mode. Bits 0, 1, 5, and 6 return the decoded value of the Drive Select bits in the DOR register. Bits 2, 3, and 4 are set by their respective active going edges and are cleared by reading the DIR register. The WRDATA bit is triggered by raw WRDATA signals and is not gated by WE. Bits 2, 3, and 4 are cleared to a low level by either Hardware or Software RESET.

2.1.3 DIGITAL OUTPUT REGISTER (DOR)

The Digital Output Register contains the drive select and motor enable bits, a reset bit and a $\overline{DMA\ GATE}$ bit.

Bits	7	6	5	4	3	2	1	0
Function	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMA $\overline{GATE}$	$\overline{RESET}$	DRIVE SEL1	DRIVE SEL2
H/W Reset State	0	0	0	0	0	0	0	0
Auto PD State	0*	0*	0*	0*	UC	1*	UC	UC

The MOT ENx bits directly control their respective motor enable pins (ME0–3). A one means the pin is active, the $\overline{INVERT}$ pin determines the active level. The DRIVE SELx bits are decoded to provide four drive select lines and only one may be active at a time. A one is active and the $\overline{INVERT}$ pin determines the level on the cable. Standard programming practice is to set both MOT ENx and DRIVE SELx bits at the same time.

Table 2-1 lists a set of DOR values to activate the drive select and motor enable for each drive.

Table 2-1. Drive Activation Values

Drive	DOR Value
0	1CH
1	2DH
2	4EH
3	8FH

The $\overline{DMAGATE}$ bit is enabled only in PC-AT and Model 30 Modes. If $\overline{DMAGATE}$ is set low, the INT and DRQ outputs are tristated and the $\overline{DACK}$ and TC inputs are disabled. $\overline{DMAGATE}$ set high will enable INT, DRQ, TC, and $\overline{DACK}$ to the system. In PS/2 Mode $\overline{DMAGATE}$ has no effect upon INT, DRQ, TC or $\overline{DACK}$ pins and they are always active.

The DOR reset bit and the Motor Enable bits have to be inactive when the 82077SL is in powerdown. The $\overline{DMAGATE}$ and DRIVE SEL bits are unchanged. During powerdown, writing to the DOR does not awaken the 82077SL with the exception of activating any of the motor enable bits. Setting the motor enable bits active (high) will wake up the part.

This $\overline{RESET}$ bit clears the basic core of the 82077SL and the FIFO circuits when the LOCK bit is set to "0" (see Section 5.3.2 for LOCK bit definition). Once set, it remains set until the user clears this bit. This bit is set by a chip reset and the 82077SL is held in a reset state until the user clears this bit. The $\overline{RESET}$ bit has no effect upon this register.

2.1.4 TAPE DRIVE REGISTER (TDR)

Bits	7	6	5	4	3	2	1	0
Function	—	—	—	—	—	—	TAPE SEL1	TAPE SEL0
H/W Reset State	—	—	—	—	—	—	0	0
Auto PD State	—	—	—	—	—	—	UC	UC

This register allows the user to assign tape support to a particular drive during initialization. Any future references to that drive number automatically invokes tape support. Hardware reset clears this register; software resets have not effect. TDR[2:7] are not writable and remain tristated if read. The tape select bits are hardware RESET to zeros, making Drive 0 not available for tape support. Drive 0 is reserved for the floppy boot drive. The tuning of the PLL for tape characteristics can also be done in hardware. If a 0 (GND) is applied to pin 39 (PLL0) the PLL is optimized for tape drives, a 1 (V_{CC}) optimizes the PLL for floppies. This hardware selection mechanism overrides the software selection scheme. A typical hardware application would route the Drive Select pin used for tape drive support to pin 39 (PLL0). For further explanation on optimizing 82077 for tape drives please refer to Section 10.2.4.

2.1.5 DATARATE SELECT REGISTER (DSR)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Function	S/W RESET	POWER DOWN	PDOSC	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
H/W Reset State	0	0	0	0	0	0	1	0
Auto PD State	0	0	UC	UC	UC	UC	UC	UC

This register ensures backward compatibility with the 82072 floppy controller and is write-only. Changing the data rate changes the timings of the drive control signals. To ensure that drive timings are not violated when changing data rates, choose a drive timing such that the fastest data rate will not violate the timing.

This register is identical to the one used in 82077AA with the exception of bit 5. This bit in the 82077SL denoted by PDOSC is used to implement crystal oscillator power management. The internal oscillator in the 82077SL can be programmed to be either powered on or off via the PDOSC bit. This capability is independent of the chip's powerdown state. In other words, auto powerdown mode and powerdown via activating POWERDOWN bit has no effect over the power state of the oscillator.

In the default state the PDOSC bit is low and the oscillator is powered up. When this bit is programmed to a one, the oscillator is shut off. Hardware reset clears this bit to a zero. Neither of the software resets (via DOR or DSR) have any effect on this bit. When an external oscillator is used, this bit can be set to reduce power consumption. When an internal oscillator is used, this bit can be set to turn off the oscillator to conserve power. However, PDOSC must go high only when the part is in the powerdown state, otherwise the part will not function correctly and must be hardware reset once the oscillator has turned back on and stabilized. Setting the PDOSC bit has no effect on the clock input to the 82077SL (the X1 pin). The clock input is separately disabled when the part is powered down.

S/W RESET behaves the same as DOR RESET except that this reset is self clearing.

POWERDOWN bit implements direct powerdown. Setting this bit high will put the 82077SL into the powerdown state regardless of the state of the part. The part is internally reset and then put into powerdown. No status is saved and any operation in progress is aborted. Unlike the 82077AA this mode of powerdown does not turn off the internal oscillator. Any hardware or software reset will exit the 82077SL from this powerdown state. When 82077SL enters powerdown via this state it affects the floppy disk drive interface as suggested in Section 4.2.2. The state of the floppy disk drive pins during powerdown via the DSR register behaves similarly to that during auto powerdown.

PRECOMP 0–2 adjusts the WRDATA output to the disk to compensate for magnetic media phenomena known as bit shifting. The data patterns that are susceptible to bit shifting are well understood and the 82077SL compensates the data pattern as it is written to the disk. The amount of precompensation is dependent upon the drive and media but in most cases the default value is acceptable.

The 82077SL starts precompensating the data pattern starting on Track 0. The CONFIGURE command can change the track that precompensating starts on. Table 2-2 lists the precompensation values that can be selected and Table 2-3 lists the default precompensation values. The default value is selected if the three bits are zeros.

DRATE 0–1 select one of the four data rates as listed in Table 2-4. The default value is 250 Kbps upon a chip ("Hardware") reset. Other ("Software") Resets do not affect the DRATE or PRECOMP bits.

Table 2-2. Precompensation Delays

PRECOMP 432	Precompensation Delay
111	0.00 ns—DISABLED
001	41.67 ns
010	83.34 ns
011	125.00 ns
100	166.67 ns
101	208.33 ns
110	250.00 ns
000	DEFAULT

Table 2-3. Default Precompensation Delays

Data Rate	Precompensation Delays
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

Table 2-4. Data Rates

DRATESEL 1	DRATESEL 0	DATA RATE MFM
1	1	1 Mbps
0	0	500 Kbps
0	1	300 Kbps
1	0	250 Kbps

2.1.6 MAIN STATUS REGISTER (MSR)

Bits	7	6	5	4	3*	2	1	0
Function	RQM	DIO	NON DMA	CMD BSY	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY
H/W Reset State	0	X	X	X	X	X	X	X
Auto PD State	1	0	0	0	0	0	0	0

The Main Status Register is a read-only register and is used for controlling command input and result output for all commands.

RQM—Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

DIO—Indicates the direction of a data transfer once RQM is set. A 1 indicates a read and a 0 indicates a write is required.

NON-DMA—This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

COMMAND BUSY—This bit is set to a one when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (SEEK, RECALIBRATE commands), this bit is returned to a 0 after the last command byte.

DRV x BUSY—These bits are set to ones when a drive is in the seek portion of a command, including seeks, and recalibrates.

2.1.7 FIFO (DATA)

All command parameter information and disk data transfers go through the FIFO. The FIFO is 16 bytes in size and has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to an 8272A compatible mode after a "Hardware" reset (Reset via pin 32). "Software" Resets (Reset via DOR or DSR register) can also place the 82077SL into 8272A compatible mode if the LOCK bit is set to "0" (See section 5.3.2 for the definition of the LOCK bit). This maintains PC-AT hardware compatibility. The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 2.5 gives several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold\#} \times \left| \frac{1}{\text{DATA RATE}} \times 8 \right| - 1.5\ \mu s = \text{DELAY}$$

Table 2-5. FIFO Service Delay

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	$1 \times 8\ \mu s - 1.5\ \mu s = 6.5\ \mu s$
2 bytes	$2 \times 8\ \mu s - 1.5\ \mu s = 14.5\ \mu s$
8 bytes	$8 \times 8\ \mu s - 1.5\ \mu s = 62.5\ \mu s$
15 bytes	$15 \times 8\ \mu s - 1.5\ \mu s = 118.5\ \mu s$

FIFO Threshold Examples	Maximum Delay to Servicing at 500 Kbps Data Rate
1 byte	$1 \times 16\ \mu s - 1.5\ \mu s = 14.5\ \mu s$
2 bytes	$2 \times 16\ \mu s - 1.5\ \mu s = 30.5\ \mu s$
8 bytes	$8 \times 16\ \mu s - 1.5\ \mu s = 126.5\ \mu s$
15 bytes	$15 \times 16\ \mu s - 1.5\ \mu s = 238.5\ \mu s$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the 82077SL enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC.

2.1.8a DIGITAL INPUT REGISTER (DIR, PC-AT MODE)

This register is read only in all modes. In PC-AT mode only bit 7 is driven, all other bits remain tristated.

Bits	7	6	5	4	3*	2	1	0
Function	DSKCHG	—	—	—	—	—	—	—
H/W Reset State	N/A	—	—	—	—	—	—	—
Auto PD State	0	—	—	—	—	—	—	—

DSKCHG monitors the pin of the same name and reflects the opposite value seen on the disk cable, regardless of the value of $\overline{\text{INVERT}}$. The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits remain tristated.

2.1.8b DIGITAL INPUT REGISTER (DIR, PS/2 MODE)

Bits	7	6	5	4	3	2	1	0
Function	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	HIGH $\overline{\text{DENS}}$
H/W Reset State	N/A	1	1	1	1	1	0	1
Auto PD State	0	1	1	1	1	UC	UC	UC

The following is changed in PS/2 Mode: Bits 6, 5, 4, and 3 return a value of "1", and the DRATE SEL1-0 return the value of the current data rate selected (see Table 2-4 for values).

$\overline{\text{HIGH DENS}}$ is low whenever the 500 Kbps or 1 Mbps data rates are selected. This bit is independent of the effects of the IDENT and $\overline{\text{INVERT}}$ pins.

The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits (as applicable) remain unchanged.

Table 2-6 shows the state of the DENSEL pin when $\overline{\text{INVERT}}$ is low.

This pin is set high after a pin RESET and is unaffected by DOR and DSR resets.

Table 2-6. DENSEL Encoding

Data Rate	IDENT*	DENSEL
1 Mbps	0	0
	1	1
500 Kbps	0	0
	1	1
300 Kbps	0	1
	1	0
250 Kbps	0	1
	1	0

*After ("Hardware") Chip Reset

2.1.8c DIGITAL INPUT REGISTER (DIR, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	$\overline{DSK}$ $\overline{CHG}$	0	0	0	$\overline{DMA}$ $\overline{GATE}$	NOPREC	DRATE SEL1	DRATE SEL0
H/W Reset State	N/A	0	0	0	0	0	1	0
Auto PD State	1	0	0	0	UC	UC	UC	UC

The following is changed in Model 30 Mode: Bits 6, 5, and 4 return a value of "0", and Bit 7 ($\overline{DSKCHG}$) is inverted in Model 30 Mode.

The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits (as applicable) remain unchanged.

Bit 3 reflects the value of $\overline{DMAGATE}$ bit set in the DOR register.

Bit 2 reflects the value of NOPREC bit set in the CCR register.

2.1.9a CONFIGURATION CONTROL REGISTER (CCR, PC AT and PS/2 MODES)

This register sets the datarate and is write only. In the PC-AT it is named the DSR.

Bits	7	6	5	4	3	2	1	0
Function	—	—	—	—	—	—	DRATE SEL1	DRATE SEL0
H/W Reset State	—	—	—	—	—	—	1	0
Auto PD State	—	—	—	—	—	—	UC	UC

Refer to the table in the Data Rate Select Register for values. Unused bits should be set to 0.

2.1.9b CONFIGURATION CONTROL REGISTER (CCR, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	—	—	—	—	—	NOPREC	DRATE SEL1	DRATE SEL0
H/W Reset State	—	—	—	—	—	0	1	0
Auto PD State	—	—	—	—	—	UC	UC	UC

NOPREC has no function, and is reset to "0" with a Hardware RESET only.

2.2 RESET

There are three sources of reset on the 82077SL; the RESET pin, a reset generated via a bit in the DOR and a reset generated via a bit in the DSR. All resets take the 82077SL out of the power down state.

On entering the reset state, all operations are terminated and the 82077SL enters an idle state. Activating reset while a disk write activity is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, and the 82077SL waits for a new command. Drive polling will start unless disabled by a new CONFIGURE command.

2.2.1 RESET PIN ("HARDWARE") RESET

The RESET pin is a global reset and clears all registers except those programmed by the SPECIFY command. The DOR Reset bit is enabled and must be cleared by the host to exit the reset state.

2.2.2 DOR RESET vs DSR RESET ("SOFTWARE" RESET)

These two resets are functionally the same. The DSR Reset is included to maintain 82072 compatibility. Both will reset the 8272 core which affects drive status information. The FIFO circuits will also be reset if the LOCK bit is a "0" (See Section 5.3.2 for the definition of the LOCK bit). The DSR Reset clears itself automatically while the DOR Reset requires the host to manually clear it. DOR Reset has precedence over the DSR Reset. The DOR Reset is set automatically upon a pin RESET. The user must manually clear this reset bit in the DOR to exit the reset state.

The t30a specification in the A.C. Specifications gives the minimum amount of time that the DOR reset must be held active. This amount of time that the DOR reset must be held active is dependent upon the data rate. 82077SL requires that the DOR reset bit must be held active for at least 0.5 μs at 250 Kbps. This is less than a typical ISA I/O cycle time.

2.3 DMA Transfers

DMA transfers are enabled with the SPECIFY command and are initiated by the 82077SL by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting $\overline{DACK}$ and addresses need not be valid. $\overline{CS}$ can be held inactive during DMA transfers.

3.0 DRIVE INTERFACE

The 82077SL has integrated all of the logic needed to interface to a floppy disk or a tape drive which use floppy interface. All drive outputs have 40 mA drive capability and all inputs use a receive buffer with hysteresis. The internal analog data separator requires no external components, yet allows for an extremely wide capture range with high levels of read-data jitter, and ISV. The designer needs only to run the 82077SL disk drive signals to the disk or tape drive connector.

3.1 Cable Interface

The $\overline{INVERT}$ pin selects between using the internal buffers on the 82077SL or user supplied inverting buffers. $\overline{INVERT}$ pulled to V_{CC} disables the internal buffers; pulled to ground will enable them. There is no need to use external buffers with the 82077SL in typical PC applications.

The polarity of the DENSEL pin is controlled through the IDENT pin, after hardware reset. For 5.25" drives a high on DENSEL tells the drive that either the 500 Kbps or 1 Mbps data rate is selected. For some 3.5" drives the polarity of DENSEL changes to a low for high data rates. See **Table 2-6 DENSEL Encoding** for $\overline{IDENT}$ pin settings.

Additionally, the two types of drives have different electrical interfaces. Generally, the 5.25" drive uses open collector drivers and the 3.5" drives (as used on PS/2) use totem-pole drivers. The output buffers on the 82077SL do not change between open collector or totem-pole, they are always totem-pole. For design information on interfacing 5.25" and 3.5" drives to a single 82077SL, refer to Section 9.

3.2 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called Data Window, is used to internally sample the serial data. One state of Data Window is used to sample the data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

To support reliable disk reads the data separator must track fluctuations in the read data frequency. Frequency errors primarily arise from two sources: motor rotation speed variation and instantaneous speed variation (ISV). A second condition, and one that opposes the ability to track frequency shifts is the response to bit jitter.

The internal data separator consists of two analog phase lock loops (PLLs) as shown in Figure 3-1. The two PLLs are referred to as the reference PLL and the data PLL. The reference PLL (the master PLL) is used to bias the data PLL (the slave PLL). The reference PLL adjusts the data PLL's operating point as a function of process, junction temperature and supply voltage. Using this architecture it was possible to eliminate the need for external trim components.

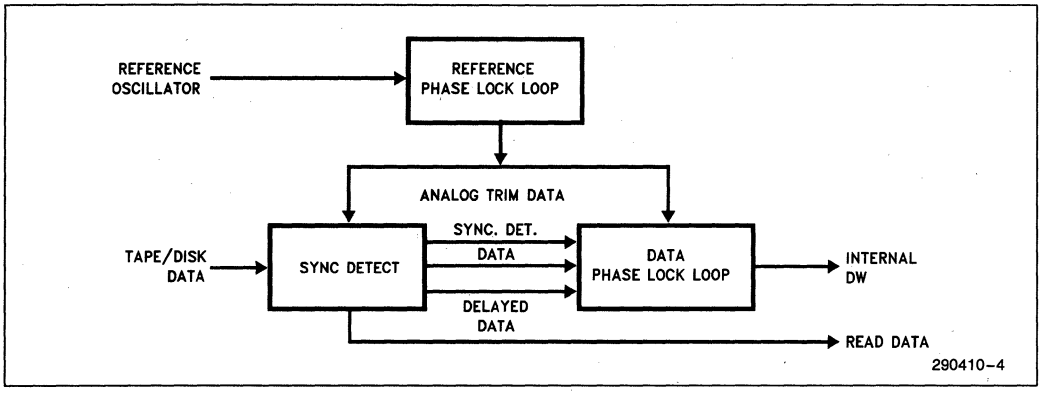


Figure 3-1. Data Separator Block Diagram

PHASE LOCK LOOP OVERVIEW

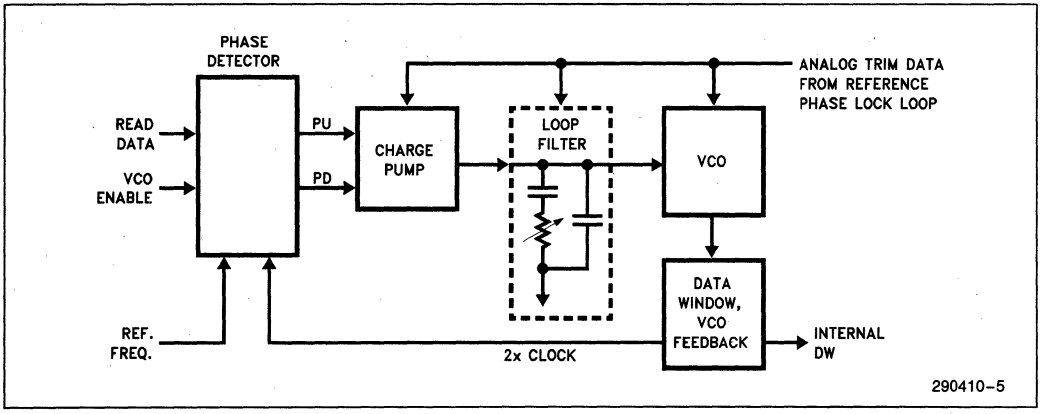


Figure 3-2. Data PLL

Figure 3-2 shows the data PLL. The reference PLL has control over the loop gain by its influence on the charge pump and the VCO. In addition the reference PLL controls the loop filter time constant. As a result the closed loop transfer function of the data PLL is controlled, and immune to the first order, to environmental factors and process variation.

Systems with analog PLLs are often very sensitive to noise. In the design of this data separator many steps were taken to avoid noise sensitivity problems. The analog section of the chip has a separate VSS pin (AVSS) which should be connected externally to a noise free ground. This provides a clean basis for VSS referenced signals. In addition many analog circuit features were employed to make the overall system as insensitive to noise as possible.

3.2.1 JITTER TOLERANCE

The jitter immunity of the system is dominated by the data PLL's response to phase impulses. This is measured as a percentage of the theoretical data window by dividing the maximum readable bit shift by a ¼ bitcell distance. For instance, if the maximum allowable bit shift is 300 ns for a 500 Kbps data stream, the jitter tolerance is 60%. The graph in Figures 13-1 thru 13-4 of the Data Separator Characteristics sections illustrate the jitter tolerance of the 82077SL across each frequency range.

3.2.2 LOCKTIME (tLOCK)

The lock, or settling time of the data PLL is designed to be 64 bit times. This corresponds to 8 sync bytes in the MFM mode. This value assumes that the sync field jitter is 5% the bit cell or less. This level of jitter should be easily achieved for a constant bit pattern, since intersymbol interference should be equal, thus nearly eliminating random bit shifting.

3.2.3 CAPTURE RANGE

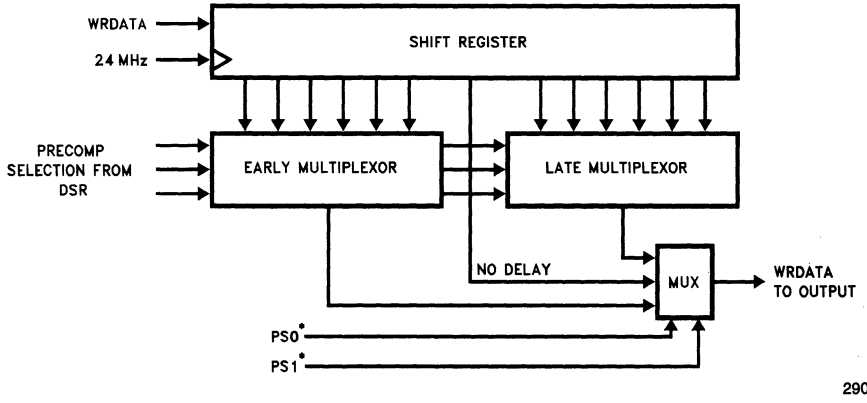
Capture Range is the maximum frequency range over which the data separator will acquire phase lock with the incoming RDDATA signal. In a floppy disk environment, this frequency variation is composed of two components: drive motor speed error and ISV. Frequency is a factor which may determine the maximum level of the ISV (Instantaneous Speed Variation) component. In general, as frequency increases the allowed magnitude of the ISV component will decrease. When determining the capture range requirements, the designer should take the maximum amount of frequency error for the disk drive and double it to account for media switching between drives.

3.3 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. The shifting of bits is a known phenomena of magnetic media and is dependent upon the disk media AND the floppy drive.

The 82077SL monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late (or not at all) relative to the surrounding bits. Figure 3-3 is a block diagram of the internal circuit.

The top block is a 13-bit shift register with the no delay tap being in the center. This allows 6 levels of early and late shifting with respect to nominal. The shift register is clocked at the main clock rate (24 MHz). The output is fed into 2 multiplexors—one for early and one for late. A final stage of multiplexors combines the early, late and normal data stream back into one which is the WRDATA output.



NOTE:
PS0,1 are 8272A control signals but are not available as outputs on the 82077SL.

Figure 3-3. Precompensation Block Diagram

4.0 POWER MANAGEMENT FEATURES

The 82077SL contains power management features that makes it ideal for design of portable personal computers. These features can be classified into power management of the part and that of the internal oscillator. The powerdown of the part is done independently of the internal oscillator in the 82077SL.

4.1 Oscillator Power Management

The 82077SL supports a built-in crystal oscillator that can be programmed to be either powered down or active, independent of the power state of the chip. This capability is implemented by the PDOSC bit in the DSR. When PDOSC is set low, the internal oscillator is on and when it is set high the internal oscillator is off. DSR powerdown does not turn off the oscillator.

When the external oscillator is used, power can be saved by turning off the internal oscillator. If the internal oscillator is used, the oscillator may be powered up (even when the rest of the chip is powered off) allowing the chip to wake up quickly and in a stable state. It is recommended to keep the internal oscillator on even when in the powerdown state. The main reason for this is that the recovery time of the oscillator during wake up may take tens of milliseconds under the worst case, which may create problems with any sensitive application software. In a typical application the internal oscillator should be on unless the system goes into a power saving or standby mode (such a mode request would be made by a system time out or by a user). In this case, the system software would take over and must turn on the oscillator sufficiently ahead of awakening the part.

In the case of the external oscillators, the power up characteristics are similar. If the external source remains active during the time the 82077SL is powered down, then the recovery time effect is minimized. The PD pin can be used to turn off the external source. While the PD pin is active 82077SL does not require a clock source. However, when the PD pin is inactive, the clocking source, once it starts oscillating, must be completely stable to ensure that the 82077SL operates properly.

4.2 Part Power Management

This section deals with the power management of the rest of the chip excluding the oscillator. This shows how powerdown modes and wake up modes are activated.

4.2.1 POWERDOWN MODES

The rest of the chip is powered down in two ways—direct powerdown and automatic powerdown. Direct powerdown results in immediate powerdown of the part without regard to the current state of the part. Automatic powerdown results when certain conditions become true within the part.

4.2.1.a Direct Powerdown

Direct powerdown is conducted via the POWERDOWN bit in the DSR register (bit 6). This mode is compatible to the 82077AA. Programming this bit high will powerdown 82077SL after the part is internally reset. All current status is lost if this type of powerdown mode is used. The part can exit powerdown from this mode via any hardware or software reset. This type of powerdown will override the automatic powerdown. If the part is in automatic powerdown when the DSR powerdown is issued then all the previous status of the part will be lost and the 82077SL will be reset to its default values.

4.2.1.b Auto Powerdown

Automatic powerdown is conducted via a "Set Powerdown Mode" command. There are four conditions required before the part will enter powerdown. All these conditions must be true for the part to initiate the powerdown sequence. These conditions are listed as follows:

1. The motor enable pins ME[0:3] must be inactive,
2. The part must be idle; this is indicated by MSR = 80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupt),
3. The head unload timer (HUT—explained in Section 6.2.6) must have expired, and
4. The auto powerdown timer must have timed out.

The command can be used to enable powerdown by setting the AUTO PD bit in the command to high. The command also provides a capability of programming a minimum power up time via the MIN DLY bit in the command. The minimum power up time refers to a minimum amount of time the part will remain powered up after being awakened or reset. An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down provided all the remaining conditions are met. Any software reset will reinitialize the timer. Changing of data rate extends the auto powerdown timer by up to 10 ms, but only if the data rate is changed during the countdown.

Disabling the auto powerdown mode cancels the timers and holds the 82077SL out of auto powerdown.

4.2.2 WAKE UP MODES

This section describes the conditions for awakening the part from both direct and automatic powerdown. Power conservation or extension of battery life is the main reason power management is required. This means that the 82077SL must be kept in powerdown state as long as possible and should be powered up as late as possible without compromising software transparency.

To keep the part in powerdown mode as late as possible implies that the part should wake up as fast as possible. However, some amount of time is required for the part to exit powerdown state and prepare the internal microcontroller to accept commands. Application software is very sensitive to such a delay and in order to maintain software transparency, the recovery time of the wake up process must be carefully controlled by the system software.

4.2.2.a Wake Up from DSR Powerdown

If the 82077SL enters the powerdown through the DSR powerdown bit, it must be reset to exit. Any form of software or hardware reset will serve, although DSR is recommended. No other register access will awaken the part, including writing to the DOR's motor enable (ME[0:3]) bits.

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened by a software reset, the auto powerdown command (including the minimum delay timer) will once again become effective as previously programmed. If the part is awakened via a hardware reset, the auto powerdown is disabled.

After reset, the part will go through a normal sequence. The drive status will be initialized. The FIFO mode will be set to default mode on a hardware reset or on a software reset if the LOCK command has not blocked it. Finally, after a delay, the polling interrupt will be issued.

4.2.2.b Wake Up from Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the 82077SL resumes operation as though it was never in powerdown. Besides activating the RESET pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part)
2. A read from the MSR register
3. A read or write to the FIFO register

Any of these actions will wake up the part. Once awake, 82077SL will reinitiate the auto powerdown timer for 10 ms or 0.5 sec. (depending on the MIN DLY bit the auto powerdown command). The part will powerdown again when all the powerdown conditions stated in Section 4.2.1b are satisfied.

4.3 Register Behavior

The register descriptions and their values in the powerdown state were given in Section 2.1. Table 4.1 reiterates the AT and PS/2 (including model 30) configuration registers available. It also shows the type of access permitted. In order to maintain software transparency, access to all the registers must be maintained. As Table 4.1 shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in Section 2.1. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed.

4.4 Pin Behavior

The 82077SL is specifically designed for the portable PC systems in which the power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of 82077SL can be divided into two major categories—system interface and floppy disk drive interface. The floppy disk drive pins are disabled such that no power will be drawn through the 82077SL as a result of any voltage applied to the pin within the 82077SL's power supply range. The floppy disk drive interface pins are configurable by the FDI TRI bit in the auto powerdown command. When the bit is set the output pins of the floppy disk drive retain their original state. All other pins are either disabled or unchanged as depicted in Table 4-4. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

4.4.1 SYSTEM INTERFACE PINS

Table 4.2 gives the state of the system interface pins in the powerdown state. Pins unaffected by powerdown are labeled "UC". Input pins are "DISABLED" to prevent them from causing currents internal to the 82077SL when they have indeterminate input values.

Table 4-1. 82077SL Register Behavior

Address	Available Registers		Access Permitted
	PC-AT	PS/2 (Model 30)	
Access to these registers DOES NOT wake up the part			
000	—	SRA	R
001	—	SRB	R
010	DOR*	DOR*	R/W
011	TDR	TDR	R/W
100	DSR*	DSR*	W
110	—	—	—
111	DIR	DIR	R
111	CCR	CCR	W
Access to these registers wakes up the part			
100	MSR	MSR	R
101	FIFO	FIFO	R/W

NOTE:
*Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (either via DOR or DSR reset bits) will wake up the part.

Table 4-2. 82077SL System Interface Pins

System Pins	State in Power Down	System Pins	State in Power Down
Input Pins		**Output Pins**	
$\overline{CS}$	UC	DRQ	UC (Low)
$\overline{RD}$	UC	INT	UC (Low)
$\overline{WR}$	UC	PD	HIGH
A[0:2]	UC	IDLE	High (Auto PD) Low (DSR PD)
DB[0:7]	UC	DB[0:7]	UC
RESET	UC		
IDENT	UC		
$\overline{DACK}$	Disabled		
TC	Disabled		
X[1:2]	Programmable		

Two pins which can be used to indicate the status of the part are IDLE and PD. These pins have replaced the HIFIL and LOFIL pins in the 82077AA. The capacitor required on the 82077AA has been integrated on the chip. Table 4-3 shows how these pins reflect the 82077SL status.

Table 4-3. 82077SL Status Pins

PD	IDLE	MSR	Part Status
1	1	80H	Auto Powerdown
1	0	RQM = 1; MSR[6:0] = X	DSR Powerdown
0	1	80H	Idle
0	0	—	Busy

The IDLE pin indicates when the part is idle state and can be powered down. It is a combination of MSR equalling 80H, the head being unloaded and the INT pin being low. As shown in the table the IDLE pin will be low when the part is in DSR powerdown state. The PD pin is active whenever the part is in the powerdown state. It is active for either mode of powerdown. The PD pin can be used to turn off an external oscillator of other floppy disk drive interface hardware.

4.4.2 FDD INTERFACE PINS

The FDD interface "input" pins during powerdown are disabled or unchanged as shown in Table 4-4. The floppy disk drive "output" pins are programmable by the FDI TRI bit in the auto powerdown command. Setting of the FDI TRI bit in the auto power down command results in the interface retaining its normal state. When this bit is low (default state) all output pins in the FDD interface to the floppy disk drive itself are TRISTATED. Pins used for local logic control or part programming are unaffected. Table 4-4 depicts the state of the floppy disk interface pins in the powerdown state (FDI TRI is low).

Table 4-4. 82077SL FDD Interface Pins

FDD Pins	State in Powerdown	System Pins	State in Powerdown
Input Pins		**Output Pins (FDI TRI = 0)**	
RDDATA	Disabled	ME[0:3]	Tristated
WP	Disabled	DS[0:3]	Tristated
TRK0	Disabled	DIR	Tristated
INDX	Disabled	STEP	Tristated
DRV2	Disabled	WRDATA	Tristated
DSKCHG	Disabled	WE	Tristated
$\overline{INVERT}$	UC	HDSEL	Tristated
MFM	UC	DENSEL	Tristated
		DRATE[0:1]	Tristated

5.0 CONTROLLER PHASES

For simplicity, command handling in the 82077SL can be divided into three phases: Command, Execution and Result. Each phase is described in the following secions.

When there is no command in progress, the 82077SL can be in idle, drive polling or powerdown state.

5.1 Command Phase

After a reset, the 82077SL enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the 82077SL before the command phase is complete (Please refer to Section 6.0 for the command descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the 82077SL, the host must examine the RQM and DIO bits of the Main Status Register. RQM, DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the 82077SL after each write cycle until the received byte is processed. The 82077SL asserts RQM again to request each parameter byte of the command, unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0", and the 82077SL automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to retain compatibility with the 8272A, and to provide for the proper handling of the "Invalid Command" condition.

5.2 Execution Phase

All data transfers to or from the 82077SL occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the SPECIFY command.

Each data byte is transferred by an INT or DRQ depending on the DMA mode. The CONFIGURE command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the 82077SL when service is requested from the host, and ranges from 1 to 16. The parameter FIFOTHR which the user programs is one less, and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request, for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

5.2.1 NON-DMA MODE, TRANSFERS FROM THE FIFO TO THE HOST

The INT pin and RQM bits in the Main Status Register are activated when the FIFO contains (16–<threshold>) bytes, or the last bytes of a full sector transfer have been placed in the FIFO. The INT pin can be used for interrupt driven systems and RQM can be used for polled sytems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The 82077SL will deactivate the INT pin and RQM bit when the FIFO becomes empty.

5.2.2 NON-DMA MODE, TRANSFERS FROM THE HOST TO THE FIFO

The INT pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The INT pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The INT pin will also be deactivated if TC and DACK# both go inactive. The 82077SL enters the result phase after the last byte is taken by the 82077SL from the FIFO (i.e. FIFO empty condition).

5.2.3 DMA MODE, TRANSFERS FROM THE FIFO TO THE HOST

The 82077SL activates the DRQ pin when the FIFO contains (16–<threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The 82077SL will deactivate the DRQ pin when the FIFO becomes empty. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of RD#, on the last byte, if no edge is present on DACK#). A data underrun may occur if DRQ is not removed in time to prevent an unwanted cycle.

5.2.4 DMA MODE, TRANSFERS FROM THE HOST TO THE FIFO

The 82077SL activates the DRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the DACK# and WR# pins and placing data in the FIFO. DRQ remains active until the FIFO becomes full. DRQ is again set true when the FIFO has <threshold> bytes remaining in the FIFO. The 82077SL will also deactivate the DRQ pin when TC becomes true (qualified by DACK#), indicating that no more data is required. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of WR# of the last byte, if no edge is present on DACK#). A data overrun may occur if DRQ is not removed in time to prevent an unwanted cycle.

5.2.5 DATA TRANSFER TERMINATION

The 82077SL supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the 82077SL will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the 82077SL, the internal sector count will be complete when 82077SL reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the 82077SL to read the last 16 bytes from the FIFO. The host must tolerate this delay.

5.3 Result Phase

The generation of INT determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the 82077SL before the result phase is complete. (Refer to Section 6.0 on command descriptions.) These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read from the FIFO. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared. This indicates that the 82077SL is ready to accept the next command.

6.0 COMMAND SET/DESCRIPTIONS

Commands can be written whenever the 82077SL is in the command phase. Each command has a unique set of needed parameters and status results. The 82077SL checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it was invalid, the next time the RQM bit in the MSR register is a "1" the DIO and CB bits will also be "1", indicating the FIFO must be read. A result byte of 80H will be read out of the FIFO, indicating an invalid command was issued. After reading the result byte from the FIFO the 82077SL will return to the command phase. Table 6-1 is a summary of the Command set.

Table 6-1. 82077SL Command Set

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
READ DATA										
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and system
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
READ DELETED DATA										
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and system
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
WRITE DATA										
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the system and FDD
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				

2

Table 6-1. 82077SL Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
WRITE DELETED DATA										
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and system
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
READ TRACK										
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and system. FDC reads all of cylinders contents from index hole to EOT
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
VERIFY										
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL/SC				
Execution										No data transfer takes place
Result	R					ST 0				Status information after Command execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID information after Command execution
	R					R				
	R					N				
VERSION										
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

Table 6-1. 82077SL Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
FORMAT TRACK										
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				N					Bytes/Sector
	W				SC					Sectors/Cylinder
	W				GPL					Gap 3
	W				D					Filler Byte
Execution For Each Sector Repeat:	W				C					Input Sector Parameters
	W				H					
	W				R					
	W				N					
										82077SL formats an entire cylinder
Result	R				ST 0					Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				Undefined					
	R				Undefined					
	R				Undefined					
	R				Undefined					
SCAN EQUAL										
Command	W	MT	MFM	SK	1	0	0	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information Prior to Command Execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared Between the FDO and Main-System
Result	R				ST 0					Status Information After Command Execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID Information After Command Execution
	R				H					
	R				R					
	R				N					

2

Table 6-1. 82077SL Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
SCAN LOW OR EQUAL										
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information
	W				H					Prior to Command
	W				R					Execution
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared Between the FDO and Main-System
Result	R				ST 0					Status Information
	R				ST 1					After Command
	R				ST 2					Execution
	R				C					
	R				H					Sector ID Information
	R				R					After Command
	R				N					Execution
SCAN HIGH OR EQUAL										
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information
	W				H					Prior to Command
	W				R					Execution
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared Between the FDO and Main-System
Result	R				ST 0					Status Information
	R				ST 1					After Command
	R				ST 2					Execution
	R				C					
	R				H					Sector ID Information
	R				R					After Command
	R				N					Execution

Table 6-1. 82077SL Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R					ST 0				Status information at the end of each seek operation
	R					PCN				
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W				SRT				HUT	
	W					HLT				ND
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R					ST 3				Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					NCN				
Execution										Head is positioned over proper Cylinder on Diskette
CONFIGURE										
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL			FIFOTHR		
	W					PRETRK				
RELATIVE SEEK										
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					RCN				

Table 6-1. 82077SL Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
DUMPREG										
Command	W	0	0	0	0	1	1	1	0	*Note
Execution										Registers placed in FIFO
Result	R				PCN-Drive 0					
	R				PCN-Drive 1					
	R				PCN-Drive 2					
	R				PCN-Drive 3					
	R		SRT					HUT		
	R				HLT				ND	
	R				SC/EOT					
	R	LOCK	0	D_3	D_2	D_1	D_0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL			FIFOTHR		
	R				PRETRK					
READ ID										
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R				ST 0					Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				C					
	R				H					Disk status after the Command has completed.
	R				R					
	R				N					
PERPENDICULAR MODE										
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	D_3	D_2	D_1	D0	GAP	WGATE	
LOCK										
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	
POWERDOWN MODE										
Command	W	0	0	0	1	0	1	1	1	Command Codes
	W	0	0	0	0	0	FDI TRI	MIN DLY	AUTO PD	
Result	R	0	0	0	0	0	FDI TRI	MIN DLY	AUTO PD	
INVALID										
Command	W				Invalid Codes					Invalid Command Codes (NoOp — 82077SL goes into Standby State)
Result	R				ST 0					ST 0 = 80H

SC is returned if the last command that was issued was the FORMAT command. EOT is returned if the last command was a READ or WRITE.

NOTE:
These bits are used internally only. They are not reflected in the Drive Select pins. It is the users responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

PARAMETER ABBREVIATIONS

Symbol	Description
AUTO PD	Auto powerdown control. If this bit is 0, then the automatic powerdown is disabled. If it is set to 1, then the automatic powerdown is enabled.
C	Cylinder address. The currently selected cylinder address, 0 to 255.
D_0, D_1 D_2, D_3	Drive Select 0-3. Designates which drives are Perpendicular drives, a "1" indicating Perpendicular drive.
D	Data pattern. The pattern to be written in each sector data field during formatting.
DIR	Direction control. If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.
DS0, DS1	Disk Drive Select.

DS1	DS0	
0	0	drive 0
0	1	drive 1
1	0	drive 2
1	1	drive 3

DTL	Special sector size. By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EC	Enable Count. When this bit is "1" the "DTL" parameter of the Verify Command becomes SC (Number of sectors per track).
EFIFO	Enable FIFO. When this bit is 0, the FIFO is enabled. A "1" puts the 82077SL in the 8272A compatible mode where the FIFO is disabled.
EIS	Enable implied seek. When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.
EOT	End of track. The final sector number of the current track.
FDI TRI	Floppy Drive Interface Tristate: If this bit is 0, then the output pins of the floppy disk drive interface are tristated. This is also the default state. If it is set to 1, then the floppy disk drive interface remains unchanged.
GAP	Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap length. The gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head address. Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head load time. The time interval that 82077SL waits after loading the head and before initiating a read or write operation. Refer to the SPECIFY command for actual delays.
HUT	Head unload time. The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the SPECIFY command for actual delays.
Lock	Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be reset to their default values by a "Software Reset" (Reset made by setting the proper bit in the DSR or DOR registers).
MFM	MFM mode selector. A one selects the double density (MFM) mode.
MIN DLY	Minimum power up time control. This bit is active only if AUTO PD bit is enabled. Setting this bit to a 0, assigns a 10 ms minimum power up time and setting this bit to a 1, assigns a 0.5 sec. minimum power up time.
MT	Multi-track selector. When set, this flag selects the multi-track operating mode. In this mode, the 82077SL treats a complete cylinder, under head 0 and 1, as a single track. The 82077SL operates as if this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the 82077SL finishes operating on the last sector under head 0.

Symbol	Description
N	Sector size code. This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the users responsibility to not select combinations that are not possible with the drive.

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

NCN	New cylinder number. The desired cylinder number.
ND	Non-DMA mode flag. When set to 1, indicates that the 82077SL is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the 82077SL operates in DMA mode, interfacing to a DMA controller by means of the DRQ and DACK# signals.
OW	The bits denoted D_0, D_1, D_2, and D_3 of the **PERPENDICULAR MODE** command can only be overwritten when the OW bit is set to "1".
PCN	Present cylinder number. The current position of the head at the completion of SENSE INTERRUPT STATUS command.
POLL	Polling disable. When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation start track number. Programmable from track 00 to FFH.
R	Sector address. The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative cylinder number. Relative cylinder offset from present cylinder as used by the RELATIVE SEEK command.
SC	Number of sectors. The number of sectors to be initialized by the FORMAT command. The number of sectors to be verified during a Verify Command, when EC is set.

Symbol	Description
SK	Skip flag. When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of READ DATA. If READ DELETED is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step rate interval. The time interval between step pulses issued by the 82077SL. Programmable from 0.5 to 8 milliseconds, in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status register 0–3. Registers within the 82077SL that store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write gate alters timing of WE, to allow for pre-erase loads in perpendicular drives.

6.1 Data Transfer Commands

All of the READ DATA, WRITE DATA and VERIFY type commands use the same parameter bytes and return the same results information. The only difference being the coding of bits 0–4 in the first byte.

An implied seek will be executed if the feature was enabled by the CONFIGURE command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a READ/WRITE DATA command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

6.1.1 READ DATA

A set of nine (9) bytes is required to place the 82077SL into the Read Data Mode. After the READ DATA command has been issued, the 82077SL loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the SPECIFY command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the 82077SL reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one, and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the 82077SL stops sending data, but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector terminate the READ DATA Command.

N determines the number of bytes per sector (see Table 6-2 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the 82077SL transfers the specified number of bytes to the host. For reads, it continues to read the entire 128 byte sector and checks for CRC errors. For writes it completes the 128 byte sector by filling in zeroes. If N is not set to 00 Hex, DTL should be set to FF Hex, and has no impact on the number of bytes transferred.

Table 6-2. Sector Sizes

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
. .	. . .
07	16 Kbytes

The amount of data which can be handled with a single command to the 82077SL depends upon MT (multi-track) and N (Number of bytes/sector).

Table 6-3. Effects of MT and N Bits

MT	N	Max. Transfer Capacity	Final Sector Read from Disk
0	1	256 × 26 = 6,656	26 at side 0 or 1
1	1	256 × 52 = 13,312	26 at side 1
0	2	512 × 15 = 7,680	15 at side 0 or 1
1	2	512 × 30 = 15,360	15 at side 1
0	3	1024 × 8 = 8,192	8 at side 0 or 1
1	3	1024 × 16 = 16,384	16 at side 1

The Multi-Track function (MT) allows the 82077SL to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at the last sector of the same track at Side 1.

If the host terminates a read or write operation in the 82077SL, then the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 6-6. The termination must be normal.

At the completion of the READ DATA Command, the head is not unloaded until after the Head Unload Time Interval (specified in the SPECIFY command) has elapsed. If the host issues another command before the head unloads then the head settling time may be saved between subsequent reads.

If the 82077SL detects a pulse on the IDX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the 82077SL sets the IC code in Status Register 0 to "01" (Abnormal termination), and sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the READ DATA Command.

After reading the ID and Data Fields in each sector, the 82077SL checks the CRC bytes. If a CRC error occurs in the ID or data field, the 82077SL sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the READ DATA Command.

Table 6-4 below describes the affect of the SK bit on the READ DATA command execution and results.

Table 6-4. Skip Bit vs READ DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	No	Normal Termination.
0	Deleted Data	Yes	Yes	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	Yes	No	Normal Termination.
1	Deleted Data	No	Yes	Normal Termination Sector Not Read ("Skipped").

Except where noted in Table 6-4, the C or R value of the sector address is automatically incremented (see Table 6-6).

6.1.2 READ DELETED DATA

This command is the same as the READ DATA command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 6-5 describes the affect of the SK bit on the READ DELETED DATA command execution and results.

Table 6-5. Skip Bit vs READ DELETED DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	Yes	Address Not Incremented. Next Sector Not Searched For.
0	Deleted Data	Yes	No	Normal Termination.
1	Normal Data	No	Yes	Normal Termination Sector Not Read ("Skipped").
1	Deleted Data	Yes	No	Normal Termination.

Except where noted in Table 6-5 above, the C or R value of the sector address is automatically incremented (See Table 6-6).

6.1.3 READ TRACK

This command is similar to the READ DATA command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the IDX pin, the 82077SL starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the 82077SL finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The 82077SL compares the ID information read from each sector with the specified value in the command, and sets the ND flag of Status Register 1 to a "1" if there is no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (Bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors have been read. If the 82077SL does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, then it sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 6-6. Result Phase Table

MT	Head	Final Sector Transferred to Host	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
1	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	LSB	01	NC

NC: no change, the same value as the one at the beginning of command execution.
LSB: least significant bit, the LSB of H is complemented.

6.1.4 WRITE DATA

After the WRITE DATA command has been issued, the 82077SL loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the SPECIFY command), and begins reading ID Fields. When the sector address read from the diskette matches the sector address specified in the command, the 82077SL reads the data from the host via the FIFO, and writes it to the sector's data field.

After writing data into the current sector, the 82077SL computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the 82077SL continues writing to the next data field. The 82077SL continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros.

The 82077SL reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID Fields, it sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the WRITE DATA command.

The WRITE DATA command operates in much the same manner as the READ DATA command. The following items are the same. Please refer to the READ DATA Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command.
- Definition of DTL when N = 0 and when N does not = 0.

6.1.5 WRITE DELETED DATA

This command is almost the same as the WRITE DATA command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

6.1.6 VERIFY

The VERIFY command is used to verify the data stored on a disk. This command acts exactly like a READ DATA command except that no data is transferred to the host. Data is read from the disk, CRC computed and checked against the previously stored value.

Because no data is transferred to the host, TC (pin 25) cannot be used to terminate this command. By setting the EC bit to "1" an implicit TC will be issued to the 82077SL. This implicit TC will occur when the SC value has decrement to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0" DTL/SC should be programmed to 0FFH. Refer to Table 6-6 and Table 6-7 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 6-7. Verify Command Result Phase Table

MT	EC	SC/EOT Value	Termination Result
0	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

NOTE:
If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

6.1.7 FORMAT TRACK

The FORMAT command allows an entire track to be formatted. After a pulse from the IDX pin is detected, the 82077SL starts writing data on the disk including Gaps, Address Marks, ID Fields and Data Fields, per the IBM System 34 (MFM). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID Field for each sector is supplied by the host; that is, four data bytes per sector are needed by the 82077SL for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the 82077SL for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the 82077SL encounters a pulse on the IDX pin again and it terminates the command.

Table 6-8 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

Table 6-8. Typical Values for Formatting

		Sector Size	N	SC	GPL1	GPL2
5.25″ Drives	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		. . .	. . .			
3.5″ Drives	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in read and write commands to avoid splice point between data field and ID field of contiguous sections.
GPL2 = suggested GPL value in FORMAT TRACK command.
*PC-AT values (typical)
**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.

NOTE:
All values except Sector Size are in Hex.

6.1.7.1 Format Fields

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		C	H	S	N	C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP 4b
80x	12x	3x	FC	50x	12x	3x	FE	Y	D	E	O	R	22x	12x	3x	FB		R		
4E	00	C2		4E	00	A1		L		C		C	4E	00	A1	F8		C		

Figure 6-1. System 34 Format Double Density

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		C	H	S	N	C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP 4b
80x	12x	3x	FC	50x	12x	3x	FE	Y	D	E	O	R	41x	12x	3x	FB		R		
4E	00	C2		4E	00	A1		L		C		C	4E	00	A1	F8		C		

Figure 6-2. Perpendicular Format

6.1.8 SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDO} = D_{Processor}$, $D_{FDO} \leq D_{Processor}$, or $D_{FDO} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occurs; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6-9 shows the status of bits SH and SN under various conditions of SCAN.

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector has been encountered.

When either the STP (contiguous sectors STP = 01, or alternate sectors STP = 02) sectors are read or the MT (Multi-Track) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, andf 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to ahve the data available in less than 13 μs (MFM Mode). If an Overrun occurs the FDC terminates the command.

Table 6-9. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDO} = D_{Processor}$
	1	0	$D_{FDO} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDO} = D_{Processor}$
	0	0	$D_{FDO} < D_{Processor}$
	1	0	$D_{FDO} \not> D_{Processor}$
Scan High or Equal	0	1	$D_{FDO} = D_{Processor}$
	0	0	$D_{FDO} > D_{Processor}$
	1	0	$D_{FDO} \not< D_{Processor}$

6.2 Control Commands

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete; READ ID, RECALIBRATE and SEEK. The other control commands do not generate an interrupt.

6.2.1 READ ID

The READ ID command is used to find the present position of the recording heads. The 82077SL stores the values from the first ID Field it is able to read into its registers. If the 82077SL does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, it then sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the SENSE INTERRUPT STATUS command. Otherwise, valuable interrupt status information will be lost.

6.2.2 RECALIBRATE

This command causes the read/write head within the 82077SL to retract to the track 0 position. The 82077SL clears the contents of the PCN counter, and checks the status of the TRK0 pin from the FDD. As long as the TRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the TRK0 pin goes high, the SE bit in Status Register 0 is set to "1", and the command is terminated. If the TRK0 pin is still low after 79 step pulses have been issued, the 82077SL sets the SE and the EC bits of Status Register 0 to "1", and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one RECALIBRATE command to return the head back to physical Track 0.

The RECALIBRATE command does not have a result phase. SENSE INTERRUPT STATUS command must be issued after the RECALIBRATE command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the 82077SL is in the BUSY state, but during the execution phase it is in a NON BUSY state. At this time another RECALIBRATE command may be issued, and in this manner, parallel RECALIBRATE operations may be done on up to 4 drives at once.

Upon power up, the software must issue a RECALIBRATE command to properly initialize all drives and the controller.

6.2.3 SEEK

The read/write head within the drive is moved from track to track under the control of the SEEK Command. The 82077SL compares the PCN which is the current head position with the NCN and performs the following operation if there is a difference:

—PCN < NCN: Direction signal to drive set to "1" (step in), and issues step pulses.

—PCN > NCN: Direction signal to drive set to "0" (step out), and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN, then the SE bit in Status Register 0 is set to "1", and the command is terminated.

During the command phase of the seek or recalibrate operation, the 82077SL is in the BUSY state, but during the execution phase it is in the NON BUSY state.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) SEEK command;	Step to the proper track
2) SENSE INTERRUPT STATUS command;	Terminate the Seek command
3) READ ID.	Verify head is on proper track
4) Issue READ/WRITE command.	

The SEEK command does not have a result phase. Therefore, it is highly recommended that the SENSE INTERRUPT STATUS Command be issued after the SEEK command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return a "0". When exiting DSR POWERDOWN mode, the 82077SL clears the PCN value and the status information to zero. Prior to issuing the DSR POWERDOWN command, it is highly recommended that the user service all pending interrupts through the SENSE INTERRUPT STATUS command.

6.2.4 SENSE INTERRUPT STATUS

An interrupt signal on INT pin is generated by the 82077SL for one of the following reasons:

1. Upon entering the Result Phase of:
   a. READ DATA Command
   b. READ TRACK Command
   c. READ ID Command
   d. READ DELETED DATA Command
   e. WRITE DATA Command
   f. FORMAT TRACK Command
   g. WRITE DELETED DATA Command
   h. VERIFY Command
2. End of SEEK, RELATIVE SEEK or RECALIBRATE Command
3. 82077SL requires a data transfer during the execution phase in the non-DMA Mode

The SENSE INTERRUPT STATUS command resets the interrupt signal and via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt. If a SENSE INTERRUPT STATUS command is issued when no active interrupt condition is present, the status register ST0 will return a value of 80H (invalid command).

Table 6-9. Interrupt Identification

SE	IC	Interrupt Due To
0	11	Polling
1	00	Normal Termination of SEEK or RECALIBRATE command
1	01	Abnormal Termination of SEEK or RECALIBRATE command

The SEEK, RELATIVE SEEK and the RECALIBRATE commands have no result phase. SENSE INTERRUPT STATUS command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a SENSE INTERRUPT STATUS is not issued, the drive, will continue to be BUSY and may effect the operation of the next command.

6.2.5 SENSE DRIVE STATUS

SENSE DRIVE STATUS obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. STATUS REGISTER 3 contains the drive status information.

6.2.6 SPECIFY

The SPECIFY command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between the Head Load signal goes high and the read, write operation starts. The values change with the data rate speed selection and are documented in Table 6-10.

Table 6-10. Drive Control Delays (ms)

	HUT				SRT			
	1M	500K	300K	250K	1M	500K	300K	250K
0	128	256	426	512	8.0	16	26.7	32
1	8	16	26.7	32	7.5	15	25	30
..	..	..	..	..	..	..	..	..
E	112	224	373	448	1.0	2	3.33	4
F	120	240	400	480	0.5	1	1.67	2

	HLT			
	1M	500K	300K	250K
00	128	256	426	512
01	1	2	3.3	4
02	2	4	6.7	8
..	..	..	..	.
7F	126	252	420	504
7F	127	254	423	508

The choice of DMA or NON-DMA operations is made by the ND bit. When this bit is "1", the NON-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signalled by the DRQ pin. Non-DMA mode uses the RQM bit and the INT pin to signal data transfers.

6.2.7 CONFIGURE

Issued to select the special features of the 82077SL. A CONFIGURE command need not be issued if the default values of the 82077SL meet the system requirements.

CONFIGURE DEFAULT VALUES:

EIS — No Implied Seeks
EFIFO — FIFO Disabled
POLL — Polling Enabled
FIFOTHR — FIFO Threshold Set to 1 Byte
PRETRK — Pre-Compensation Set to Track 0

EIS—Enable implied seek. When set to "1", the 82077SL will perform a SEEK operation before executing a read or write command. Defaults to no implied seek.

EFIFO—A "1" puts the FIFO into the 8272A compatible mode where the FIFO is disabled. This means data transfers are asked for on a byte by byte basis. Defaults to "1", FIFO disabled. The threshold defaults to one.

POLL—Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a RESET. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR—The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte "0F" selects 16 bytes.

PRETRK—Pre-compensation start track number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0, "FF" selects 255.

6.2.8 VERSION

The VERSION command checks to see if the controller is an enhanced type or the older type (8272A/765A). A value of 90 H is returned as the result byte, defining an enhanced FDD controller is in use. No interrupts are generated.

6.2.9 RELATIVE SEEK

The command is coded the same as for SEEK, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control.

DIR	Action
0	Step Head Out
1	Step Head In

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The RELATIVE SEEK command differs from the SEEK command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The SEEK command is good for drives that support a maximum of 256 tracks. RELATIVE SEEKs cannot be overlapped with other RELATIVE SEEKs. Only one RELATIVE SEEK can be active at a time. Bit 4 of Status Register 0 (EC) will be set if RELATIVE SEEK attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks and that the host needs to read track 300 and the head is on any track (0–255). If a SEEK command was issued, the head would stop at track 255. If a RELATIVE SEEK command was issued, the 82077SL would move the head the specified number of tracks, regardless of the internal cylinder position register (but would increment the register). If the head had been on track 40 (D), the maximum track that the 82077SL could position the head on using RELATIVE SEEK, would be 296 (D), the initial track, +256 (D). The maximum count that the head can be moved with a single RELATIVE SEEK command is 256 (D).

The internal register, PCN, would overflow as the cylinder number crossed track 255 and would contain 40 (D). The resulting PCN value is thus (NCN + PCN) mod 256. Functionally, the 82077SL starts counting from 0 again as the track number goes above 255(D). It is the users responsibility to compensate 82077SL functions (precompensation track number) when accessing tracks greater than 255. The 82077SL does not keep track that it is working in an "extended track area" (greater than 255). Any command issued would use the current PCN value except for the RECALIBRATE command which only looks for the TRACK0 signal. RECALIBRATE would return an error if the head was farther than 79 due to its limitation of issuing a maximum 80 step pulses. The user simply needs to issue a second RECALIBRATE command. The SEEK command and implied seeks will function correctly within the 44 (D) track (299–255) area of the "extended track area". It is the users responsibility not to issue a new track position that would exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0–255) of tracks, a RELATIVE SEEK would be issued to cross the track 255 boundary.

A RELATIVE SEEK can be used instead of the normal SEEK but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a READ ID command to ensure that the head is physically on the track that software assumes it to be. Different 82077SL commands will return different cylinder results which may be difficult to keep track of with software without the READ ID command.

6.2.10 DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug.

6.2.11 PERPENDICULAR MODE COMMAND

The PERPENDICULAR MODE command should be issued prior to executing READ/WRITE/FORMAT commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 6-11 describes the effects of the WGATE and GAP bits for the PERPENDICULAR MODE command. Upon a reset, the 82077SL will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data rate Select Register. The user must ensure that the two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The format field shown in Figure 5-3 illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the 82077SL, the controller must begin synchronization at the beginning of the Sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, an approximate 2 byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the WRITE DATA case, the 82077SL activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC as shown in Figure 6-1. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP = 0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the PERPENDICULAR MODE command is invoked, 82077SL software behavior from the user standpoint is unchanged.

Table 6-11. Effects of WGATE and GAP Bits

GAP	WGATE	MODE	VCO Low Time after Index Pulse	Length of Gap2 Format Field	Portion of Gap2 Written by Write Data Operation	Gap2 VCO Low Time for Read Operations
0	0	Conventional Mode	33 Bytes	22 Bytes	0 Bytes	24 Bytes
0	1	Perpendicular Mode (500 Kbps Data Rate)	33 Bytes	22 Bytes	19 Bytes	24 Bytes
1	0	Reserved (Conventional)	33 Bytes	22 Bytes	0 Bytes	24 Bytes
1	1	Perpendicular Mode (1 Mbps Data Rate)	18 Bytes	41 Bytes	38 Bytes	43 Bytes

NOTE:
When either GAP or WGATE bit is set, the current value of precompensation in the DSR is used.

6.2.12 POWERDOWN MODE COMMAND

The POWERDOWN MODE command allows the automatic power management of the 82077SL. This especially allows the extension of battery life in portable PC systems. This command should be issued during the BIOS power on self test (POST) to enable auto powerdown.

As soon as the command is enabled, a 10 ms or a 0.5 sec minimum power up timer is initiated depending on whether the MIN DLY bit is set to 0 or 1. This timer is one of the required conditions that has to be satisfied before the part will enter auto powerdown. Any software reset will reinitialize the timer. The timer countdown is also extended by up to 10 ms if the data rate is changed during the timer's countdown. Without this timer 82077SL would have been put to sleep immediately after 82077SL is idle. The minimum delay gives software a chance to interact with 82077SL without incurring an additional overhead due to recovery time.

The command also allows the output pins of floppy disk drive interface to be tristated or left unaltered during auto powerdown. This is done by the FDI TRI bit. In the default condition (FDI TRI = 0) the output pins of the floppy disk drive are tristated. Setting this bit leaves the interface unchanged from the normal state.

The results phase returns the values programmed for MIN DLY, FDI TRI and AUTO PD. The results phase of the auto powerdown mode command has its two most significant bits set to zero to distinguish it from the 82077AA's command of the same value which returns an "Illegal Command" status of 80H. The auto powerdown mode is disabled by a hardware reset. Software results have no effect on the POWERDOWN MODE command parameters.

6.3 Command Set Enhancements

The PERPENDICULAR MODE and DUMPREG commands were enhanced along with the addition of a new LOCK command in the 82077AA. These enhancements also hold for the 82077SL and are explained in this section of the data sheet. The commands were enhanced/added in order to provide protection against older software application package which could inadvertently cause system compatibility problems. The modifications/additions are fully backward compatible with the 82077AA which do not support the enhancements.

6.3.1 PERPENDICULAR MODE

The PERPENDICULAR MODE Command is enhanced to allow the system designers to designate specific drives as Perpendicular recording drives. This enhancement is made so that the system designer does not have to worry about older application software packages which bypass their system's FDC (Floppy Disk Controller) routines. The enhancement will also allow data transfers between Conventional and Perpendicular drives without having to issue PERPENDICULAR MODE commands between the accesses of the two different drives, nor having to change write pre-compensation values. The following is an explanation of how this enhancement is implemented:

With the old implementation, the user must properly program both the PERPENDICULAR MODE command and write pre-compensation value before accessing either a Conventional or Perpendicular drive. These programmed values apply to all drives (D0–D3) which the 82077SL may access. It should also be noted that any form of RESET "Hardware" or "Software" will configure the PERPENDICULAR MODE command for Conventional mode (GAP and WGATE = "0").

With the enhanced implementation, both the GAP and WGATE bits have the same affects as the old implementation except for when they are both programmed for value of "0" (Conventional mode). For the case when both GAP and WGATE equal "0" the PERPENDICULAR MODE command will have the following effect on the 82077SL: 1) If any of the new bits D0, D1, D2, and D3 are programmed to "1" the corresponding drive will automatically be programmed for Perpendicular mode (ie: GAP2 being

Old PERPENDICULAR MODE command:

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
PERPENDICULAR MODE										
Command	W	0	0	0	1	0	0	1	0	Command
	W	0	0	0	0	0	0	GAP	WGATE	Code

NOTE:
For the definition of GAP and WGATE bits see Table 6-11 and Section 6.2.11 of the data sheet.
For the Enhanced PERPENDICULAR MODE command definition see Table 6-1.

written during a write operation, the programmed Data Rate will determine the length of GAP2.), and data will be written with 0 ns write pre-compensation. 2) any of the new bits (D0–D3) that are programmed for "0" the designated drive will be programmed for Conventional Mode and data will be written with the currently programmed write pre-compensation value. 3) Bits D0, D1, D2, and D3 can only be over written when the OW bit is written as a "1". The status of these bits can be determined by interpreting the eighth result byte of the enhanced DUMPREG Command (See Section 6.3.3). (Note: if either the GAP or WGATE bit is a "1", then bits D0–D3 are ignored.)

"Software" and "Hardware" RESET will have the following effects on the enhanced PERPENDICULAR MODE command:

1) "Software" RESETs (Reset via DOR or DSR registers) will only clear GAP and WGATE bits to "0", D3, D2, D1, and D0 will retain their previously programmed values.
2) "Hardware" RESETs (Reset via pin 32) will clear all bits (GAP, Wgate, D0, D1, D2, and D3) to "0" (All Drives Conventional Mode).

6.3.2 LOCK

In order to protect a system with long DMA latencies against older application software packages that can disable the 82077SL's FIFO the following LOCK Command has been has been retained in the 82077SL's command set: [Note: This command should only be used by the system's FDC routines, and ISVs (Independent Software Vendors) should refrain from using it. If an ISV's application calls for having the 82077SL FIFO disabled a CONFIGURE Command should be used to toggle the EFIFO (Enable FIFO) bit. ISV can determine the value of the LOCK bit by interpreting the eighth result byte of an DUMPREG Command (See Section 6.3.3).]

The LOCK command defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to a "1" all subsequent "software" RESETs by the DOR and DSR registers will not change the previously set parameter values in the CONFIGURE command. When the LOCK bit is set to a "0" "software" RESETs by the DOR or DSR registers will return these parameters to their default values (See Section 6.2.7). All "hardware" Resets by pin 32 will set the LOCK bit to a "0" value, and will return EFIFO, FIFOTHR, and PRETRK to their default values. A Status byte is returned immediately after issuing the command byte. This Status byte reflects the value of the Lock bit set by the command byte. (Note: No interrupts are generated at the end of this command.)

6.3.3 ENHANCED DUMPREG COMMAND

To accommodate the new LOCK command and enhanced PERPENDICULAR MODE command the eighth result byte of DUMPREG command has been modified in the following manner:

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
		DUMPREG								
Result	R	**Eighth Result Byte** — Undefined —								Old
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	Enhanced

NOTES:
1. Data bit 7 reflects the status of the new LOCK bit set by the LOCK Command.
2. Data Bits D0–D5 reflect the status for bits D3, D2, D1, D0, GAP and WGATE set by the PERPENDICULAR MODE Command.

7.0 STATUS REGISTER ENCODING

The contents of these registers are available only through a command sequence.

7.1 Status Register 0

Bit No.	Symbol	Name	Description
7, 6	IC	Interrupt Code	00-Normal termination of command. The specified command was properly executed and completed without error. 01-Abnormal termination of command. Command execution was started, but was not successfully completed. 10-Invalid command. The requested command could not be executed. 11-Abnormal termination caused by Polling.
5	SE	Seek End	The 82077SL completed a SEEK or RECALIBRATE command, or a READ or WRITE with implied seek command.
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the RECALIBRATE command. 2. The RELATIVE SEEK command causes the 82077SL to step outward beyond Track 0.
3	—	—	Unused. This bit is always "0".
2	H	Head Address	The current head address.
1, 0	DS1, 0	Drive Select	The current selected drive.

7.2 Status Register 1

Bit No.	Symbol	Name	Description
7	EN	End of Cylinder	The 82077SL tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data Command.
6	—	—	Unused. This bit is always "0".
5	DE	Data Error	The 82077SL detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the 82077SL does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3	—	—	Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. READ DATA, READ DELETED DATA command, the 82077SL did not find the specified sector. 2. READ ID command, the 82077SL cannot read the ID field without an error. 3. READ TRACK command, the 82077SL cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the 82077SL is executing a WRITE DATA, WRITE DELETED DATA, or FORMAT TRACK command.
0	MA	Missing Address Mark	Any one of the following: 1. The 82077SL did not detect an ID address mark at the specified track after encountering the index pulse from the IDX pin twice. 2. The 82077SL cannot detect a data address mark or a deleted data address mark on the specified track.

7.3 Status Register 2

Bit No.	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: 1. READ DATA command, the 82077SL encounters a deleted data address mark. 2. READ DELETED DATA command, the 82077SL encounters a data address mark.
5	DD	Data Error in Data Field.	The 82077SL detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82077SL.
3	—	—	Unused. This bit is always "0".
2	—	—	Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82077SL and is equal to FF hex which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The 82077SL cannot detect a data address mark or a deleted data address mark.

7.4 Status Register 3

Bit No.	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5	—	—	Unused. This bit is always "1".
4	T0	TRACK 0	Indicates the status of the TRK0 pin.
3	—	—	Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1, 0	DS1, 0	Drive Select	Indicates the status of the DS1, DS0 pins.

8.0 COMPATIBILITY

The 82077SL was designed with software compatibility in mind. It is a fully backwards compatible solution with the older generation 8272A and NEC765A/B disk controllers. The 82077SL also implements on-board registers for compatibility with the Personal System/2s as well as PC/AT and PC/XT floppy disk controller subsystems. The 82077SL is fully compatible with Intel's 386SL Microprocessor Superset. The 82077SL represents a superset of features that are available on 82077AA. Upon a hardware reset of the 82077SL, all registers, functions and enhancements default to a PS/2, PC/AT, or PS/2 Model 30 compatible operating mode depending on how the IDENT and MFM pins are sampled during Hardware Reset.

8.1 Register Set Compatibility

The register set contained within the 82077SL is a culmination of hardware registers based on the architectural growth of the IBM personal computer line. Table 8-1 indicates the registers required for compatibility based on the type of computer.

Table 8-1. 82077SL Register Support

82077SL Register	8272A	82072	PC/XT	PC/AT	PS/2	Mod 30
SRA					X	X
SRB					X	X
DOR			X	X	X	X
MSR	X	X	X	X	X	X
DSR		X				
Data (FIFO)	X	X	X	X	X	X
DIR				X	X	X
CCR		X*		X	X	X

*CCR is emulated by DSR in an 82072 PC/AT design.

8.2 PS/2 vs. AT vs. Model 30 Mode

To maintain compatibility between PS/2, PC/AT, and Model 30 environments the IDENT and MFM pins are provided. The 82077SL is placed into the proper mode of operations upon Hardware RESET with the appropriate settings of the IDENT and MFM pins. The proper settings of the IDENT and MFM pins are described in IDENT's pin description. Differences between the three modes are described in the following sections.

8.2.1 PS/2 MODE

IDENT strapped low causes the polarity of DENSEL to be active low for high (500 Kbps/1 Mbps) data rates (typically used for 3.5" drives). This polalrity of DENSEL assumes INVERT# to be low. A comprehensive description of DENSEL behavior is given in Table 2-6.

The $\overline{\text{DMAGATE}}$ bit in the Digital Output Register (DOR) will not cause the DRQ or INT output signals to tristate. This maintains consistency with the operation of the floppy disk controller subsystem in the PS/2 architecture.

TC is an active low input signal that is internally qualified by $\overline{\text{DACK}}$ being active low.

8.2.2 PC/AT MODE

IDENT strapped high causes the polarity of DENSEL to be active high for high (500 Kbps/1 Mbps) data rates (typically used for 5.25" drives). This polarity of DENSEL assumes INVERT# to be low. A comprehensive description of DENSEL behavior is given in Table 2-6.

If the $\overline{\text{DMAGATE}}$ bit is written to a "0" in the Digital Output Register (DOR), DRQ and INT will tristate. If $\overline{\text{DMAGATE}}$ is written to a "1", then DRQ and INT will be driven appropriately by the 82077SL.

TC is an active high input signal that is internally qualified by DACK# being active low.

8.2.3 MODEL 30 MODE

IDENT strapped low causes the polarity of DENSEL to be active low for high (500 Kbps/1 Mbps) data rates (typically used for 3.5" drives). This polarity of DENSEL assumes INVERT# to be low. A comprehensive description of DENSEL behavior is given in Table 2-6.

$\overline{\text{DMAGATE}}$ and TC function the same as in PC/AT Mode.

8.3 Compatibility with the FIFO

The FIFO of the 82077SL is designed to be transparent to non-FIFO disk controller software developed on the older generation 8272A standard. Operation of the 82077SL FIFO can be broken down into two tiers of compatibility. For first tier compatibility, the FIFO is left in the default disabled condition upon a "Hardware" reset (via pin 32). In this mode the FIFO operates in a byte mode and provides complete compability with non-FIFO based software. For second tier compatibility, the FIFO is enabled via the CONFIGURE command. When the FIFO is enabled, it will temporarily enter a byte mode during the command and result phase of disk controller operation. This allows for compatible operation when interrogating the Main Status Register (MSR) for the purpose of transferring a byte at a time to or from the disk controller. For normal disk controller applications, the system designer can still take advantage of the FIFO for time critical data transfers during the execution phase and not create any conflicts with non-FIFO software during the command or result phase.

In some instances, use of the FIFO in any form has conflicted with certain specialized software. An example of a compatibility conflict using the FIFO is with software that monitors the progress of a data transfer during the execution phase. If the software assumed the disk controller was operating in a single byte mode and counted the number of bytes transferred to or from the disk controller to trigger some time dependent event on the disk media (i.e. head position over a specific data field), the same software will not have an identical time relationship if the FIFO is enabled. This is because the FIFO allows data to be queued up, and then burst trans-

ferred across the host bus. To accommodate software of this type, it is recommended that the FIFO be disabled.

8.4 Drive Polling

The 82077SL supports the polling mode of the older generation 8272A. This mode is enabled upon a reset and can be disabled via the CONFIGURE command. This mode is supported for the sole purpose of providing backwards compatibility with software that expects it's presence.

The intended purpose of drive polling dates back to 8" drives as a means to monitor any change in status for each disk drive present in the system. Each of the drives is selected for a period of time and its READY signal sampled. After a delay, the next drive is selected. Since the 82077SL does not support READY in this capacity (internally tied true), the polling sequence is only simulated and does not affect the drive select lines (DS0–DS3) when it is active. If enabled, it occurs whenever the 82077SL is waiting for a command or during SEEKs and RECALIBRATEs (but not IMPLIED SEEKs). Each drive is assumed to be not ready after a reset and a "ready" value for each drive is saved in an internal register as the simulated drive is polled. An interrupt will be generated on the first polling loop because of the initial "not ready" status. This interrupt must be followed with a SENSE INTERRUPT STATUS command from the host to clear the interrupt condition for each of the four logical drives.

9.0 PROGRAMMING GUIDELINES

Programming the 82077SL is identical to any other 8272A compatible disk controller with the exception of some additional commands. For the new designer it is useful to provide some guidelines on how to program the 82077SL. A typical disk operation involves more than issuing a command and waiting for the results. The control of the floppy disk drive is a low level operation that requires software intervention at different stages. New commands and features have been added to the 82077SL to reduce the complexity of this software interface.

9.1 Command and Result Phase Handshaking

Before a command or parameter byte can be issued to the 82077SL, the Main Status Register (MSR) must be interrogated for a ready status and proper FIFO direction. A typical floppy controller device driver should contain a subroutine for sending command or parameter bytes. For this discussion, the routine will be called "Send_byte" with the flowchart shown in Figure 9-1.

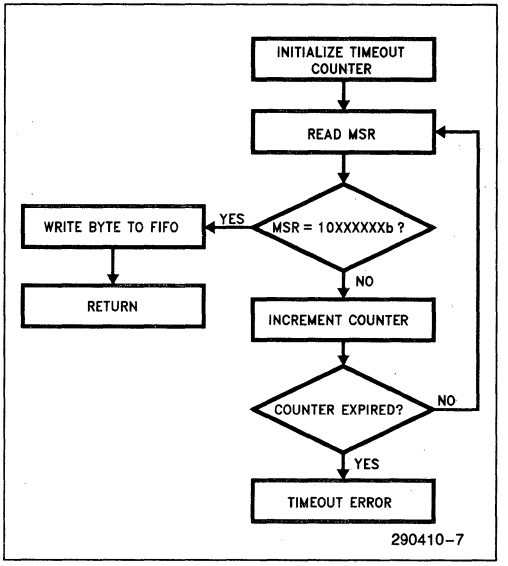


Figure 9-1. Send_Byte Routine

The routine loops until RQM is 1 and DIO is 0 indicating a ready status and FIFO direction is inward. If this condition is true, the 82077SL is ready to accept a command or parameter byte. A timeout counter is used to insure software response within a reasonable amount of time in case of no response by the 82077SL. As a note, the programmer must be careful how the maximum delay is chosen to avoid unnecessary timeouts. For example, if a new command is issued when the 82077SL is in the middle of a polling routine, the MSR will not indicate a ready status for the next parameter byte until the polling sequence completes the loop. This could cause a delay between the first and second bytes of up to 250 μs (@ 250 Kbps). If polling is disabled, this maximum delay is 175 μs. There should also be enough timeout margin to accommodate a shift of the software to a higher speed system. A timeout value that results in satisfactory operation on a 16 MHz CPU might fail when the software is moved to a system with a 25 MHz CPU. A recommended solution is to derive the timeout counter from a system hardware counter that is fixed in frequency from CPU clock to CPU clock.

For reading result bytes from the 82077SL, a similar routine is used. Figure 9-2 illustrates the flowchart for the routine "Get_byte". The MSR is polled until

RQM is 1 and DIO is 1, which indicates a ready status and outward FIFO direction. At this point, the host can read a byte from the FIFO. As in the Send_byte routine, a timout counter should be incorporated in case of a disk controller lock-up condition. For example, if a disk was not inserted into the disk drive at the time of a read operation, the controller would fail to receive the index pulse and lock-up since the index pulses are required for termination of the execution phase.

9.2 Initialization

Initializing the 82077SL involves setting up the appropriate configuration after a reset. Parameters set by the SPECIFY command are undefined after a system reset and will need to be reinitialized. CONFIGURE command parameters default to a known state after a system reset but will need to be reinitialized if the system requirements are different from the default settings. The flowchart for the recommended initialization sequence of the 82077SL is shown in Figure 9-3.

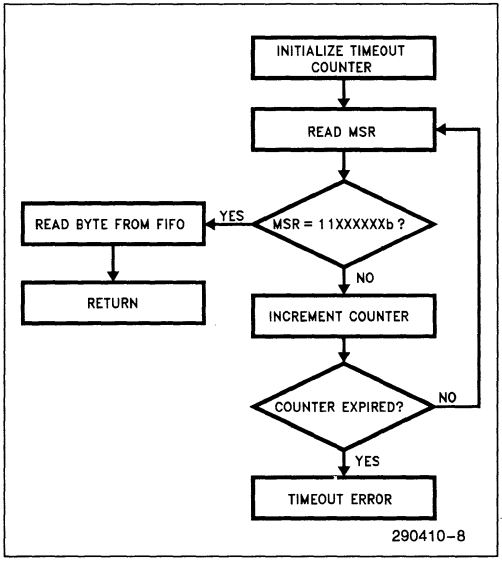


Figure 9-2. Get_Byte Routine

Following a reset of the 82077SL, the Configuration Control Register (CCR) should be reinitialized for the appropriate data rate. An external reset via the RESET pin will cause the data rate and write precompensation values to default to 250 Kbps (10b) and 125 ns (000b) respectively. Since the 125 ns write precompensation value is optimal for the 5¼" and 3½" disk drive environment, most applications will not require the value to be changed in the initialization sequence. As a note, a software reset issued via the DOR or DSR will not affect the data rate or write precompensation values. But it is recommended as a safe programming practice to always program the data rate after a reset, regardless of the type.

Since polling is enabled after a reset of the 82077SL, four SENSE INTERRUPT STATUS commands need to be issued afterwards to clear the status flags for each drive. The flowchart in Figure 9-3 illustrates how the software clears each of the four interrupt status flags internally queued by the 82077SL. It should be noted that although four SENSE INTERRUPT STATUS commands are issued, the INT pin is only active until the first SENSE INTERRUPT STATUS command is executed.

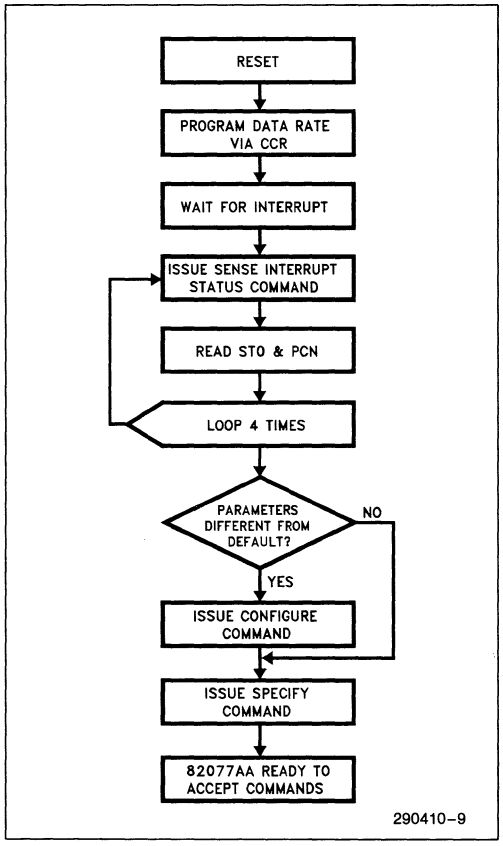


Figure 9-3. Initialization Flowchart

As a note, if the CONFIGURE command is issued within 250 μs of the trailing edge of reset (@ 1 Mbps), the polling mode of the 82077SL can be disabled before the polling initiated interrupt occurs. Since polling stops when the 82077SL enters the command phase, it is only time critical up to the first byte of the CONFIGURE command. If disabled in time, the system software no longer needs to issue the four SENSE INTERRUPT STATUS commands to clear the internal interrupt flags normally caused by polling.

The CONFIGURE command should also be issued if the system requirements are different from the default settings (as described in Section 6.2.7). For example, the CONFIGURE command can be used to enable the FIFO, set the threshold, and enable Implied Seeks.

The non-DMA mode flag, step rate (SRT), head load (HLT), and head unload times (HUT) programmed by the SPECIFY command do not default to a known state after a reset. This behavior is consistent with the 8272A and has been preserved here for compatibility. Thus, it is necessary to always issue a SPECIFY command in the initialization routine.

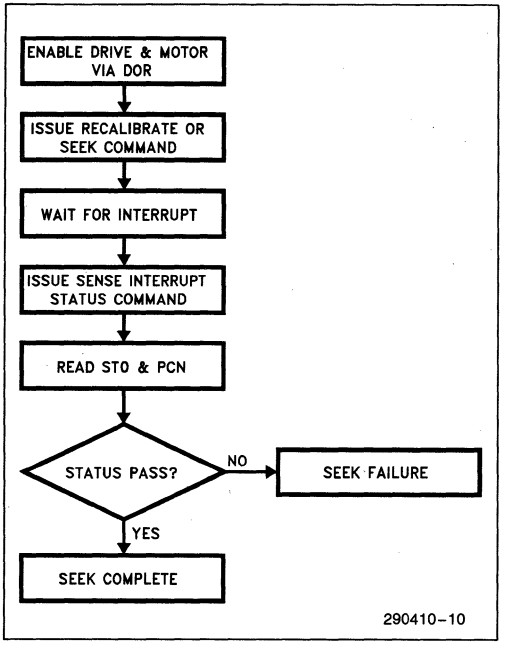


Figure 9-4. Recalibrate and Seek Operations

9.3 Recalibrates and Seeks

Commands that position the disk head are different from the typical READ/WRITE/FORMAT command in the sense that there is no result phase. Once a RECALIBRATE, SEEK, or RELATIVE SEEK command has been issued, the 82077SL will return a ready status in the Main Status Register (MSR) and perform the head positioning operation as a background task. When the seek is complete, the 82077SL will assert the INT signal to request service. A SENSE INTERRUPT STATUS command should then be asserted to clear the interrupt and read the status of the operation. Since the drive and motor enable signals are directly controlled through the Digital Output Register (DOR) on the 82077SL, a write to the DOR will need to precede the RECALIBRATE or SEEK command if the drive and motor is not already enabled. Figure 9-4 shows the flow chart for this operation.

9.4 Read/Write Data Operations

A read or write data operation requires several steps to complete successfully. The motor needs to be turned on, the head positioned to the correct cylinder, the DMA controller initialized, the read or write command initiated, and an error recovery scheme implemented. The flowchart in Figure 9-5 highlights a recommended algorithm for performing a read or write data operation.

Before data can be transferred to or from the diskette, the disk drive motor must be brought up to speed. For most 3½" disk drives, the spin-up time is 300 ms, while the 5¼" drive usually requires about 500 ms due to the increased moment of inertia associated with the larger diameter diskette.

One technique for minimizing the motor spin-up delay in the read data case is to begin the read operation immediately after the motor is turned on. When the motor is not initially up to speed, the internal data separator will fail to lock onto the incoming data stream and report a failure in the status registers. The read operation is then repeated until successful status is obtained. There is no risk of a data integrity problem since the data field is CRC validated. But, it is not recommended to use this technique for the write data operation even though it requires successful reading of the ID field before the write takes place. The data separator performance of the 82077SL is such that locking to the data stream could take place while the motor speed variation is still significant. This could result in errors when an attempt is made to read the disk media by other disk controllers that have a narrower incoming data stream frequency bandwidth.

After the motor has been turned on, the matching data rate for the media inserted into the disk drive should then be programmed to the 82077SL via the Configuration Control Register (CCR). The 82077SL

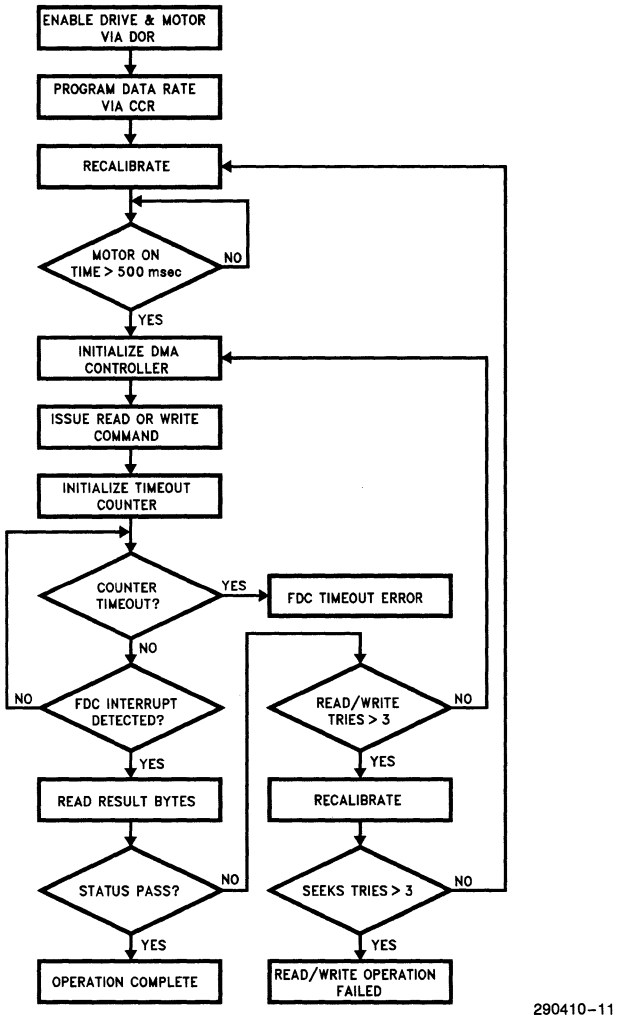


Figure 9-5. Read/Write Operation

is designed to allow a different data rate to be programmed arbitrarily without disrupting the integrity of the device. In some applications, it is required to automatically determine the recorded data rate of the inserted media. One technique for doing this is to perform a READ ID operation at each available data rate until a successful status is returned in the result phase.

If implied seeks are not enabled, the disk drive head must be positioned over the correct cylinder by executing a SEEK command. After the seek is complete, a head settling time needs to be asserted before the read or write operation begins. For most drives, this delay should be a minimum of 15 ms. When using implied seeks, the minimum head settling time can be enforced by the head load time (HLT) parameter designated in the SPECIFY command. For example, a HLT value of 8 will yield an effective head settling time of 16 ms for a programmed data rate of 500 Kbps. Of course if the head is already positioned over the correct cylinder, the head settling time does not need to be enforced.

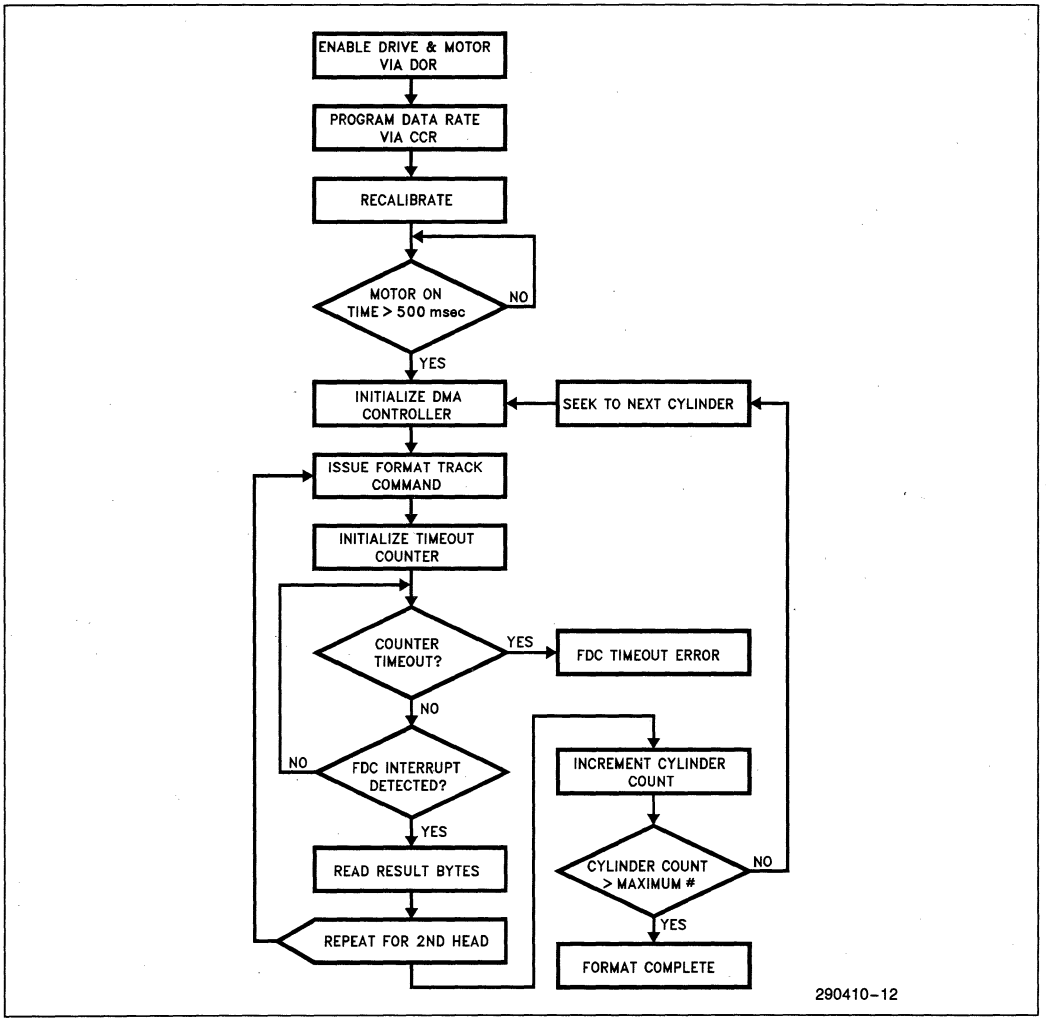


Figure 9-6 Formatting

The DMA controller is then initialized for the data transfer and the read or write command is executed. Typically the DMA controller will assert Terminal Count (TC) when the data transfer is complete. The 82077SL will then complete the current data transfer and assert the INT signal signifying it has entered the result phase. The result phase can also be entered by the 82077SL if an error is encountered or the last sector number equals the End of Track (EOT) parameter.

Based on the algorithm in Figure 9-5, if an error is encountered after reading the result bytes, two more retries are performed by reinitializing the DMA controller and re-issuing the read or write data command. A persisting failure could indicate the seek operation did not achieve proper alignment between the head and the track. The disk head should then be recalibrated and the seek repeated for a maximum of two more tries. Unsuccessful operation after this point should be reported as a disk failure to the operating system.

9.5 Formatting

The disk formatting procedure involves positioning the head on each track and creating a fixed format field used for organizing the data fields. The flowchart in Figure 9-6 highlights the typical format procedure.

After the motor has been turned on and the correct data rate programmed, the disk head is recalibrated to track 0. The disk is then allowed to come up to speed via a 500 ms delay. It is important the disk speed has stabilized before the actual formatting to avoid any data rate frequency variations. Since the format fields contain critical information used by the data separator of the disk controller for synchronization purposes, frequency stability of the data stream is imperative for media interchangeability among different systems.

The ID field data created on the disk during the format process is provided by the DMA controller during the execution phase. The DMA controller is initialized to send the C, H, R and N values for each sector ID field. For example, to format cylinder 7, on head 1, with 9 sectors, and a sector size of 2 (512 bytes), the DMA controller should be programmed to transfer 36 bytes (9 sectors x 4 bytes per sector) with the following data field: 7,1,1,2, 7,1,2,2, 7,1,3,2, ... 7,1,9,2. Since the values provided to the 82077SL during the execution phase of the format command are directly recorded as the ID fields on the disk, the data contents can be arbitrary. Some forms of copy protection have been implemented by taking advantage of this capability.

After each head for a cylinder has been formatted, a seek operation to the next cylinder is performed and the format process is repeated. Since the FORMAT TRACK command does not have implied seek capability, the SEEK command must be used. Also, as discussed in Section 9-2, the head settling time needs to be adhered to after each seek operation.

9.6 Verifies

In some applications, the sector data needs to be verified immediately after each write operation. The verify technique historically used with the 8272A or 82072 disk controller involved reinitializing the DMA controller to perform a read transfer or verify transfer (DACK# is asserted but not RD#) immediately after each write operation. A read command is then to be issued to the disk controller and the resulting status indicates if the CRC validated the previously written data. This technique has the drawback of requiring additional software intervention by having to reprogram the DMA controller between each sector write operation. The 82077SL supports this older verify technique but also provides a new VERIFY command that does not require the use of the DMA controller. This is also available in 82077AA.

To verify a write data transfer or format track operation using the VERIFY command, the software simply issues the command with the same format as a READ DATA command but without the support of the DMA controller. The 82077SL will then perform a disk read operation without a host data transfer. The CRC will be calculated for each sector read and compared against the value stored on the disk. When the VERIFY command is complete, the status register will report any detected CRC errors.

9.7 Powerdown State and Recovery

The two power management modes coupled with the internal oscillator power management forms an important consideration for programming the 82077SL. The recovery of 82077SL and the time it takes to achieve complete recovery depends on how 82077SL is powered down and how it is awakened. The following sections describe all the programming concerns and subtleties involved in using power management features of the 82077SL.

9.7.1 OSCILLATOR POWER MANAGEMENT

Section 4.1 covers the power management scheme involved in powering down of both an internal and an external oscillator. Both types of oscillators face drop out effects and require recovery times on the order of tens of milliseconds (this may be objectionable to some application software). This means that if the oscillator is powered down then it is imperative for the software to assure enough time for the oscillator to recover to a stable state. Oscillator power management must be controlled by the system software especially to maintain software transparency. In cases where the system goes into a standby mode (by user request or system timeout), the power management software can turn off the oscillator to conserve power. Complete recovery from an oscillator powerdown state requires the software to turn on the oscillator sufficiently ahead of awakening the 82077SL.

9.7.2 PART POWER MANAGEMENT

The part powerdown and wake up modes are covered in Section 4.2 in detail. This section is meant to address the programming concerns for the part (excluding the oscillator) during these modes.

9.7.2.a Powerdown Modes

For both types of powerdown modes—DSR powerdown and auto powerdown, if reset is used to exit the part from powerdown then the internal microcontroller will go through a standard sequence: register initialization followed after some delay by an interrupt.

Software transparency in auto powerdown mode is preserved by MSR retaining the value of 80H which indicates that the part is ready to receive a command. This feature allows the part to powerdown while maintaining its responsiveness to any application software.

9.7.2.b Wake Up Modes

Wake up from DSR powerdown results in the part being internally reset and all present status being lost. During DSR powerdown the RQM bit in the MSR is set. A software or hardware reset will wake up the part.

The case for wake up from auto powerdown is different. The BIOS and application software are very sensitive to delays involved in writing the first command bytes to the 82077SL. Most programs have short error timeouts in these cases. Such programs would not tolerate any floppy disk controller that was unable to receive the first byte of a command at any time. The following describes how 82077SL uniquely sustains its software transparency during wake up sequences.

Prior to writing a command to 82077SL, it is first necessary to read the MSR to ensure that the 82077SL is ready (RQM bit must be set) to receive the command. When the part detects a MSR read, it assumes that another command will follow and begins the wake up process. While the part is waking up it does not change the state of the MSR (MSR = 80H) and is able to receive the command in the FIFO. At this point one of the two following scenarios can occur.

— No other command is sent subsequent to the MSR read. The part wakes up and initializes the minimum power up timer. Upon the expiration of this timer the part is once again put in powerdown state.

— Another command follows the MSR read. If the command is send during the part's recovery from powerdown, the part remembers the command, clears the RQM bit (to prevent further bytes being written) and acts on the command once it is fully awake.

If the MSR was not checked prior to writing of a command, the part will proceed as stated above with the RQM bit cleared and the command byte held until the internal microcontroller is ready. Writing the motor enable bits in DOR active will initiate the wake up sequence with RQM set high, ready to receive any command.

As it is clear from the above discussion, the immediate access to the floppy disk controller for the first command byte is vital to software transparency. The recovery of the part from powerdown may involve a delay after the first command byte has been issued. However, all programs have tolerance for the delay after the first command byte is issued. In a powered up chip, it is possible for the microcontroller to be in its "polling loop". As a result the tolerance for this delay provides an excellent window for recovery of the part.

10.0 DESIGN APPLICATIONS

10.1 PC/AT Floppy Disk Controller

This section presents a design application of a PC/AT compatible floppy disk controller. With an 82077SL, a 24 MHz crystal, a resistor package, and a device chip select, a complete floppy disk controller can be built. The 82077SL integrates all the necessary building blocks for a reliable and low cost solution. But before we discuss the design application using the 82077SL, it is helpful to describe the architecture of the original IBM PC/AT floppy disk controller design that uses the 8272A.

10.1.1 PC/AT FLOPPY DISK CONTROLLER ARCHITECTURE

The standard IBM PC/AT floppy disk controller using the 8272A requires 34 devices for a complete solution. The block diagram in Figure 10-1 illustrates the complexity of the disk controller. A major portion of this logic involves the design of the data separator. The reliability of the disk controller is primarily dictated by the performance and stability of the data separator. Discrete board level analog phase lock loops generally offer good bit jitter margins but suffer from instability and tuning problems in the manufacturing stage if not carefully designed. While digital data separator designs offer stability and generally a lower chip count, they suffer from poor performance in the recovery of data.

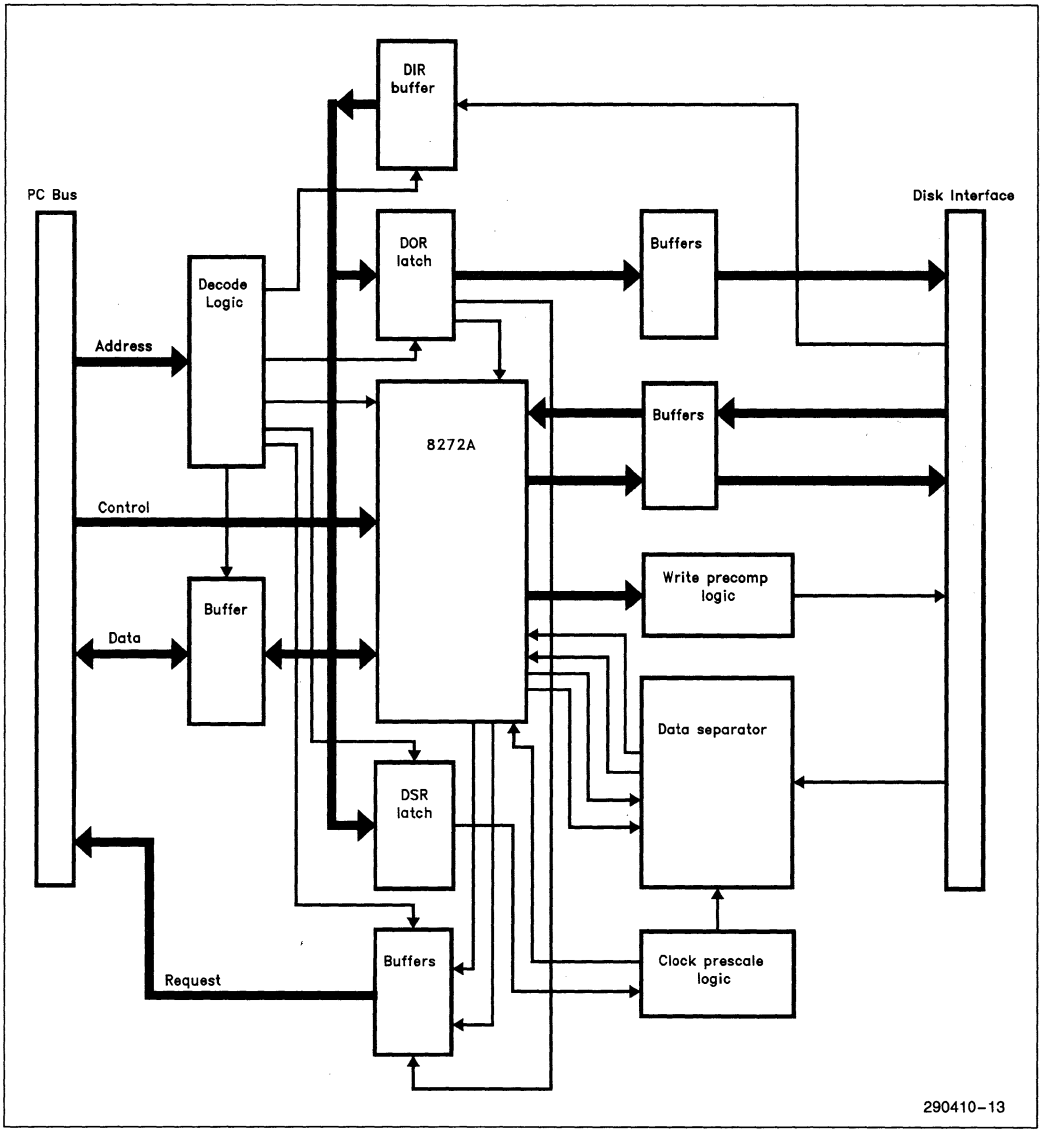


Figure 10-1. Standard IBM PC/AT Floppy Disk Controller

Table 10-1 indicates the drive and media types the IBM PC/AT disk controller can support. This requires the data separator to operate at three different data rates: 250 Kbps, 300 Kbps and 500 Kbps. Clocks to the data separator and disk controller need to be prescaled correspondingly to accommodate each of these data rates. The clock prescaling is controlled by the Data rate Select Register (DSR). Supporting all three data rates can compromise the performance of the phase lock loop (PLL) if steps are not taken in the design to adjust the performance parameters of the PLL with the data rate.

Table 10-1. Standard PC/AT Drives and Media Formats

Capacity	Drive Speed	Data Rate	Sectors	Cylinders
360 Kbyte	300 RPM	250 Kbps	9	40
*360 Kbyte	360 RPM	300 Kbps	9	40
1.2 Mbyte	360 RPM	500 Kbps	15	80

*360 Kbyte diskette in a 1.2 Mbyte drive.

The PC/AT disk controller provides direct control of the drive selects and motors via the Digital Output Register (DOR). As a result, drive selects on the 8272A are not utilized. This places drive selection and motor speed-up control responsibility with the software. The DOR is also used to perform a software reset of the disk controller and tristate the DRQ2 and IRQ6 output signals on the PC bus.

The design of the disk controller also requires address decode logic for the disk controller and register set, buffering for both the disk interface and PC bus, support for write precompensation and monitoring of the disk change signal via a separate read only register (DIR). An I/O address map of the complete register set for the PC/AT floppy disk controller is shown in Table 10-2.

Table 10-2. I/O Address Map for the PC/AT

I/O Address	Access Type	Description
3F0H	—	Unused
3F1H	—	Unused
3F2H	Write	Digital Output Register
3F3H	—	Unused
3F4H	Read	Main Status Register
3F5H	Read/Write	Data Register
3F6H	—	Unused
3F7H	Write	Data Rate Select Register
3F7H	Read	Digital Input Register

10.1.2 82077SL PC/AT SOLUTION

The 82077SL integrates the entire PC/AT controller design with the exception of the address decode on a single chip. The schematic for this solution is shown in Figure 10-2. The chip select for the 82077SL is generated by a 16L8 PAL that is programmed to decode addresses 03F0H thru 03F7H when AEN (Address Enable) is low. The programming equation for the PAL is shown in a ABEL file format in Figure 10-3. An alternative address decode solution could be provided by using a 74LS133 13 input NAND gate and 74LS04 inverter to decode A3–A14 and AEN. Although the PC/AT allows for a 64K I/O address space, decoding down to a 32K I/O address space is sufficient with the existing base of add-in cards.

A direct connection between the disk interface and the 82077SL is provided by on-chip output buffers with a 40 mA sink capability. Open collector outputs from the disk drive are terminated at the disk controller with a 150Ω resistor pack. The 82077SL disk interface inputs contain a schmitt trigger input structure for higher noise immunity. The host interface is a similar direct connection with 12 mA sink capabilities on DB0–DB7, INT and DRQ.

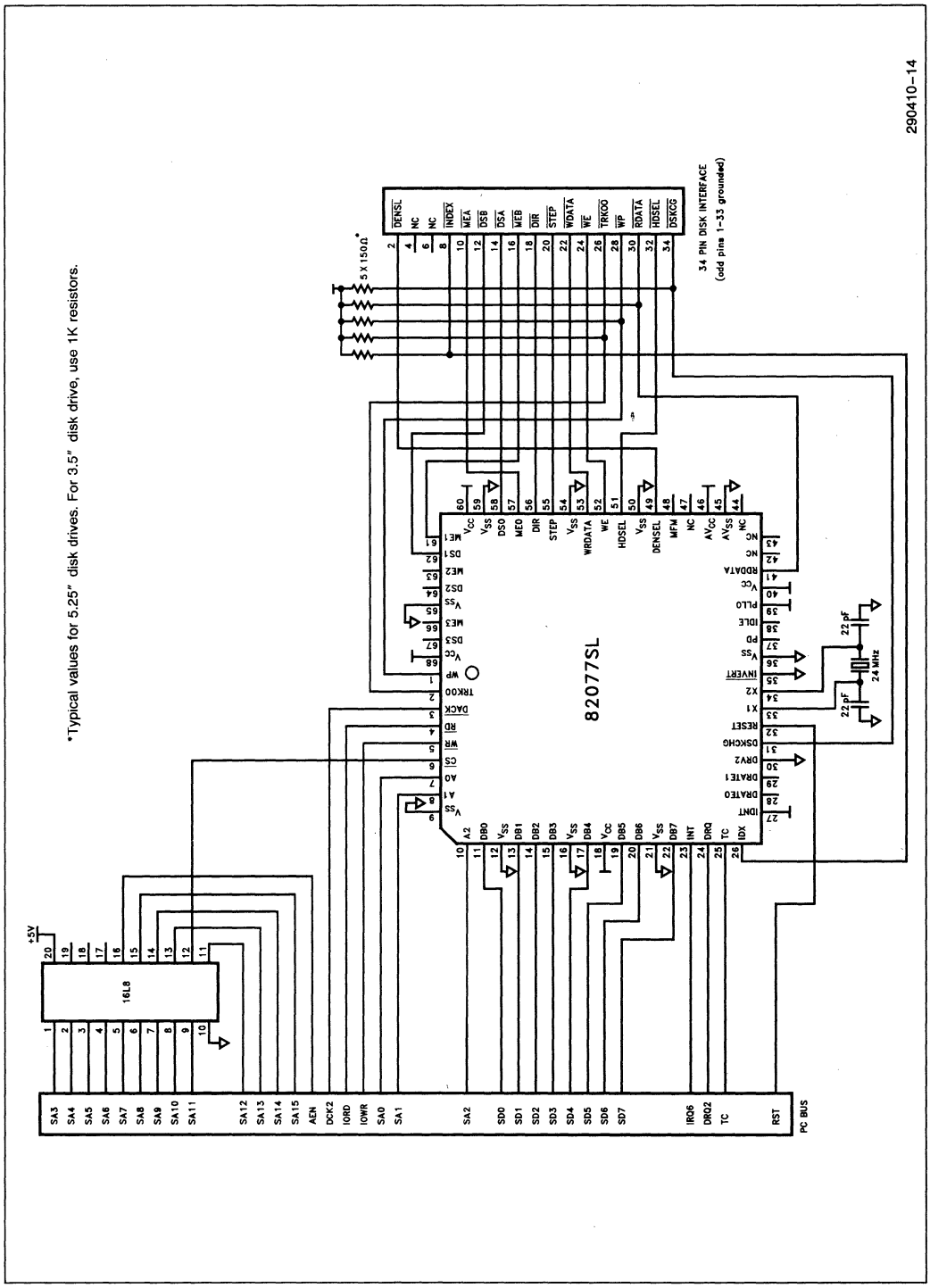


Figure 10-2. 82077SL PC/AT Floppy Disk Controller

```
MODULE PCAT077_LOGIC;

TITLE "82077SL PC/AT FLOPPY DISK CONTROLLER';
PCAT077 DEVICE "P16L8';

GND,VCC                              PIN 10,20;
SA3,SA4,SA5,SA6,SA7,SA8,SA9,SA10     PIN 1,2,3,4,5,6,7,8;
SA11,SA12,SA13,SA14,SA15,AEN         PIN 9,11,13,14,15,16;
CS077_                               PIN 12;

EQUATIONS

"" CHIP SELECT FOR THE 82077SL (3F0H -- 3F7H)

CS077_ = !( !SA15 & !SA14 & !SA13 & !SA12 & !SA11 & !SA10 &
          SA9 & SA8 & SA7 & SA6 & SA5 & SA4 & !SA3 & !AEN);

END PCAT077_LOGIC
```

Figure 10-3. PAL Equation File for a PC/AT Compatible FDC Board

10.2 3.5″ Drive Interfacing

The 82077SL is designed to interface to both 3.5″ and 5.25″ disk drives. This is facilitated by the 82077SL by orienting IDENT to get the proper polarity of DENSEL for the disk drive being used. Typically DENSEL is active high for high (500 Kbps/ 1 Mbps) data rates on 5.25″ drives. And DENSEL is typically active low for high data rates on 3.5″ drives. A complete description of how to orient IDENT to get the proper polarity for DENSEL is given in Table 2-6.

10.2.1 3.5″ DRIVES UNDER THE AT MODE

When interfacing the 82077SL floppy disk controller with a 3.5″ disk drive in a PC/AT application, it is possible that two design changes will need to be implemented for the design discussed in Section 10.1. Most 3.5″ disk drives incorporate a totem pole interface structure as opposed to open collector. Outputs of the disk drive will drive both high or low voltage levels when the drive is selected, and float only when the drive has been deselected. These totem pole outputs generally can only sink or source 4 mA of current. As a result, it is recommended to replace the 150Ω termination resistor pack with a 4.7 KΩ package to pull floating signals inactive. Some other 3.5″ drives do have an open collector interface, but have limited sink capability. In these cases, the drive manufacturer manuals usually suggest a 1 KΩ termination.

A second possible change required under "AT mode" operation involves high capacity 3.5″ disk drives that utilize a density select signal to switch between media recorded at a 250 Kbps and 500 Kbps data rate. The polarity of this signal is typically inverted for 3.5″ drives versus 5.25″ drives. Thus, an inverter can be added between the DENSEL output of the 82077SL and the disk drive interface connector when using 3.5″ drives.

But drives that do not support both data rates or drives with an automatic density detection feature via an optical sensor do not require the use of the DENSEL signal.

Another method is to change the polarity of IDENT with a drive select signal. ORing RESET with the drive select signal (DS0–3) used for the 3.5″ disk drive will produce the proper polarity for DENSEL (assuming INVERT# is low).

10.2.2 3.5″ DRIVES UNDER THE PS/2 MODES

If IDENT is strapped to ground, the DENSEL output signal polarity will reflect a typical 3.5″ drive mode of operation. That is, DENSEL will be high for 250 Kbps or 300 Kbps and low for 500 Kbps or 1 Mbps (assuming INVERT# is low). Thus the only change from the disk interface shown in Figure 10-2 is to replace the 150Ω termination resistor pack with a value of about 10 KΩ. This will prevent excessive current consumption on the CMOS inputs of the 82077SL by pulling them inactive when the drive(s) are deselected.

10.2.3 COMBINING 5.25″ AND 3.5″ DRIVES

If 5.25″ and 3.5″ drives are to be combined in a design, then steps need to be taken to avoid contention problems on the disk interface. Since 3.5″ drives do not have a large sink capability, the 150Ω termination resistor pack required by 5.25″ drives cannot be used with the 3.5″ drive. To accommodate both drives with the same disk controller, the outputs of the 3.5″ drive should be buffered before connecting to the 82077SL disk interface inputs. The 82077SL inputs are then connected to the necessary resistive termination load for the 5.25″ interface.

The block diagram in Figure 10-4 highlights how a combined interface could be designed. In this example, the 5.25″ drive is connected to drive select 0 (DS0) and the 3.5″ drive is connected to drive select 1 (DS1). DS1 is also used to enable a 74LS244 buffer on the output signals of the 3.5″ drive. The drive select logic of the 82077SL is mutually exclusive and prevents the activation of the buffer and 5.25″ drive at the same time. Since the 74LS244 has an I_{OL} of 24 mA, the termination resistor should be increased to 220Ω. This could impact the reliability of the 5.25″ drive interface if the cable lengths are greater than 5 feet.

To accommodate the polarity reversal of the DENSEL signal for 3.5″ drives, it is routed through an inverter for the 3.5″ drive interface. A 1 KΩ pull-up should be placed on the output of the inverter to satisfy the I_{OH} requirements for the 3.5″ drive when using a 74LS04.

10.2.4 OPTIMIZING 82077SL-1 FOR TAPE DRIVE MODE

The floppy disk controller can be configured for the tape drive mode by both hardware and software. Configuring the 82077SL-1 for the tape drive mode refers to optimization of the internal data separator in order to deal with the effect of ISV which is more pronounced on a tape drive than on a floppy disk controller. Hardware selection is done by setting the PLL0 (pin 39) to 0 or GND. This optimizes the data separator for tape drives by changing the loop filter component values and loop gain. TDR selection is disabled under this mode. Software selection of the tape drive mode for the FDC is implemented via setting of the appropriate bits in the tape drive register (TDR). This selection is enabled only while PLL0 is set high. This aids the user in configuring the particular drives as tape drive even when in floppy mode.

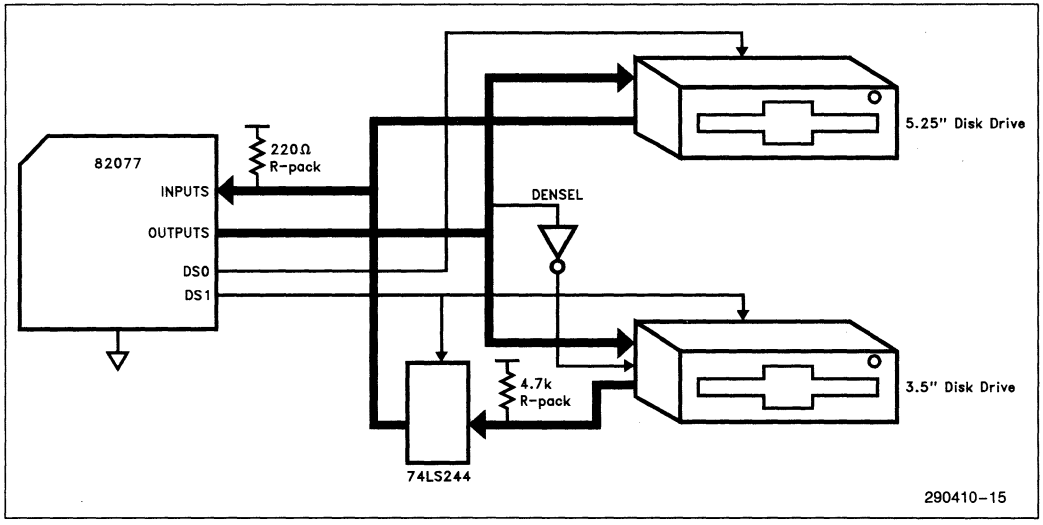


Figure 10-4. Combined 3.5″ and 5.25″ Drive Interface

As shown below the TDR contains two bits which can be utilized to assign tape support to a particular drive during initialization.

7	6	5	4	3	2	1	0
*	*	*	*	*	*	TAPE SEL1	TAPE SEL1

Hardware resets clears this register but it remains unaffected by any software reset. TDR[2:7] remain in a tristated condition and are not readable. Drive 0 is reserved for the floppy boot drive and cannot be configured for tape drives using the TDR (software mechanism). Hardware selection overrides any selection made by the software, i.e., by setting PLL0 to GND, tape drive mode will be selected regardless of the changes made to the TDR. Although the software mechanism does not allow to select drive 0 for tape drive, when PLL0 = 0 any drive can be supported for tape drive.

82077SL-1 has the capability to support up to a total of four drives. Most PC systems today have at least one floppy disk drive. This leaves the possibility of installing up to three tape drives. The following describes a way to configure the floppy disk controller in a multiple tape drive environment. This also depends on whether the system manufacturer wishes to leave certain drive slots fixed for tape drives or variable by the user.

All Tape Drives Are Variable—If the drives chosen as tape drives are variable then the configuration mechanism used is strictly software. After strapping PLL0 high, the bits TDR[0:1] can be programmed during initialization for various drives that can be selected as tape drives. It should be noted that in this case drive 0 cannot be selected as one of the tape drives.

Combination of Fixed/Variable Tape Drives—If any drive can be determined to be fixed then either the motor enable pin or the drive select pin of that particular drive can be used to drive PLL0 to GND when selected. Figure 10-5A and Figure 10-5B show two scenarios where drives that are fixed for tape drive use their motor enable or drive select signals to drive PLL0 to GND.

Figure 10-5C shows by using jumpers flexibility can be incorporated in the system and the drive/s to be fixed for tape drives can be left to the user.

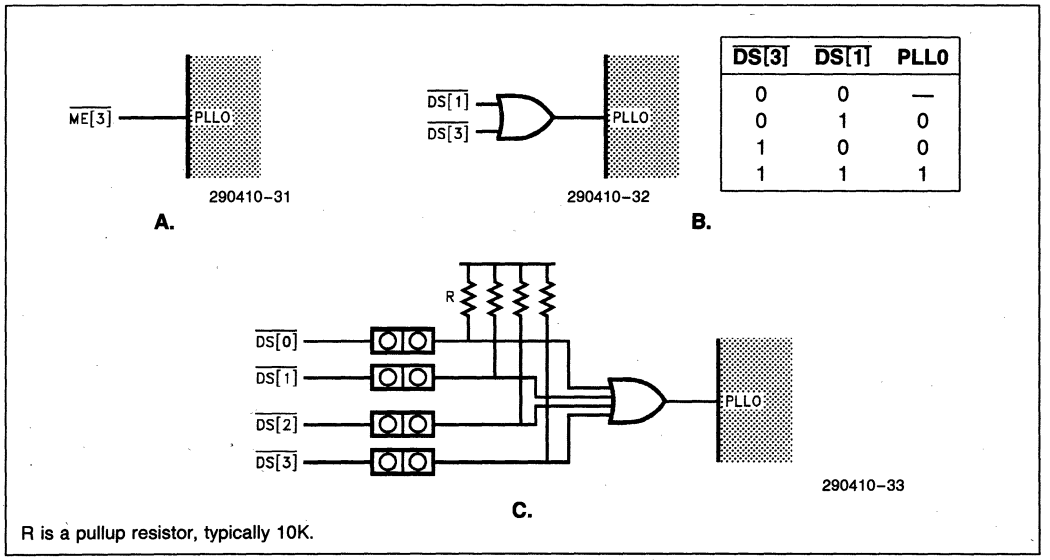


Figure 10-5. Optimizing 82077SL-1 for Tape Drive Mode

11.0 D.C. SPECIFICATIONS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

11.1 Absolute Maximum Ratings

Storage Temperature ..... −65°C to +150°C
Supply Voltage ..... −0.5 to +8.0V
Voltage on Any Input ..... GND − 2V to 6.5V
Voltage on Any Output.. GND − 0.5V to VCC + 0.5V
Power Dissipation ..... 1 Watt

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

11.2 D.C. Characteristics

T_A = 0°C to = 70°C, V_{CC} = +5V ±10%, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{ILC}	Input Low Voltage, X1	−0.5	0.8	V	
V_{IHC}	Input High Voltage, X1	3.9	V_{CC} +0.5	V	
V_{IL}	Input Low Voltage (all pins except X1)	−0.5	0.8	V	
V_{IH}	Input High Voltage (all pins except X1)	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage MFM		0.4	V	I_{OL} = 2.5 mA
	DRATE0-1		0.4	V	I_{OL} = 6.0 mA
	DB0-7, INT and DRQ		0.4	V	I_{OL} = 12 mA
	ME0-3, DS0-3, DIR, STP WRDATA, WE, HDSEL and DENSEL		0.4	V	I_{OL} = 40 mA
V_{OH}	Output High Voltage MFM	3.0		V	I_{OH} = −2.5 mA
	All Other Outputs	3.0		V	I_{OH} = −4.0 mA
	All Outputs	V_{CC} − 0.4		V	I_{OH} = −100 µA
	V_{CC} Supply Current (Total)				
I_{CC1}	1 Mbps Data Rate, V_{IL} = V_{SS}, V_{IH} = V_{CC}		45	mA	(Notes 1, 2)
I_{CC2}	1 Mbps Data Rate, V_{IL} = 0.45, V_{IH} = 2.4		50	mA	(Notes 1, 2)
I_{CC3}	500 Kbps Data Rate, V_{IL} = V_{SS}, V_{IH} = V_{CC}		35	mA	(Notes 1, 2)
I_{CC4}	500 Kbps Data Rate, V_{IL} = 0.45, V_{IH} = 2.4		40	mA	(Notes 1, 2)
I_{CCSB}	I_{CC} in Powerdown		60	µA	(Note 3)
I_{IL}	Input Load Current (all input pins)		10	µA	V_{IN} = V_{CC}
			−10	µA	V_{IN} = 0V
I_{OFL}	Data Bus Output Float Leakage		±10	µA	0.45 < V_{OUT} < V_{CC}

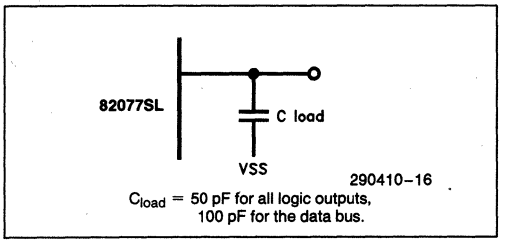
NOTES:
1. The data bus are the only inputs that may be floated.
2. Tested while reading a sync field of "00". Outputs not connected to D.C. Loads.
3. V_{IL} = V_{SS}, V_{IH} = V_{CC}; Outputs not connected to D.C. loads.

Capacitance

C_{IN}	Input Capacitance	10	pF	F = 1 MHz, T_A = 25°C
C_{IN1}	Clock Input Capacitance	20	pF	Sampled, not 100% Tested
$C_{I/O}$	Input/Output Capacitance	20	pF	

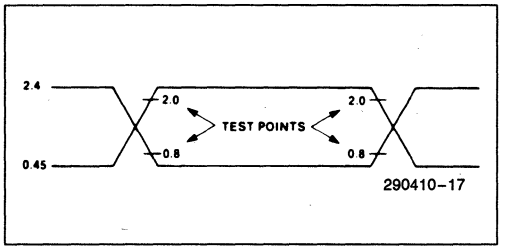
NOTE:
All pins except pins under test are tied to AC ground.

LOAD CIRCUIT



C_{load} = 50 pF for all logic outputs,
100 pF for the data bus.

A. C. TESTING INPUT, OUTPUT WAVEFORM



11.3 Oscillator

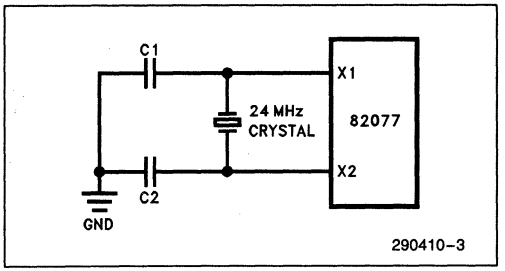


Figure 11-2. Crystal Oscillator Circuit

The 24 MHz clock can be supplied either by a crystal or a MOS level square wave. All internal timings are referenced to this clock or a scaled count which is data rate dependent.

The crystal oscillator must be allowed to run for 10 ms after VCC has reached 4.5V or exiting the POWERDOWN mode to guarantee that it is stable.

Crystal Specifications

Frequency:	24 MHz ±0.1%
Mode:	Parallel Resonant Fundamental Mode
Series Resistance:	Less than 40Ω
Shunt Capacitance:	Less than 5 pF

12.0 A.C. SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit
CLOCK TIMINGS				
t1	Clock Rise Time		10	ns
	Clock Fall Time		10	ns
t2	Clock High Time(7)	16	26	ns
t3	Clock Low Time(7)	16	26	ns
t4	Clock Period	41.66	41.66	ns
t5	Internal Clock Period(3)			
HOST READ CYCLES				
t7	Address Setup to $\overline{RD}$	5		ns
t8	$\overline{RD}$ Pulse Width	90		ns
t9	Address Hold from RD	0		ns
t10	Data Valid from $\overline{RD}$(12)		80	ns
t11	Command Inactive	60		ns
t12	Output Float Delay		35	ns
t13	INT Delay from RD(16)		t5 + 125	ns
t14	Data Hold from $\overline{RD}$	5		ns
HOST WRITE CYCLES				
t15	Address Setup to $\overline{WR}$	5		ns
t16	$\overline{WR}$ Pulse Width	90		ns
t17	Address Hold from WR	0		ns
t18	Command Inactive	60		ns
t19	Data Setup to WR	70		ns
t20	Data Hold from WR	0		ns
t21	INT Delay from WR(16)		t5 + 125	ns
DMA CYCLES				
t22	DRQ Cycle Period(1)	6.5		µs
t23	DACK to DRQ Inactive		75	ns
t23a	DRQ to DACK Inactive	(Note 15)		ns
t24	RD to DRQ Inactive(4)		100	ns
t25	DACK Setup to $\overline{RD}$, $\overline{WR}$	5		ns
t26	DACK Hold from RD, WR	0		ns
t27	DRQ to $\overline{RD}$, $\overline{WR}$ Active(1)	0	6	µs
t28	Terminal Count Width(10)	50		ns
t29	TC to DRQ Inactive		150	ns
RESET				
t30	"Hardware" Reset Width(5)	170		t4
t30a	"Software" Reset Width(5)	(Note 11)		ns
t31	Reset to Control Inactive		2	µs

A.C. SPECIFICATIONS (Continued)

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit
WRITE DATA TIMING				
t32	Write Data Width(6)			ns
DRIVE CONTROL				
t35	DIR Setup to STEP(14)	1.0		µs
t36	DIR Hold from STEP	10		µs
t37	STEP Active Time (High)	2.5		µs
t38	STEP Cycle Time(2)			µs
t39	INDEX Pulse Width	5		t5
t41	WE to HDSEL Change	(Note 13)		ms
READ DATA TIMING				
t40	Read Data Pulse Width	50		ns
f44	PLL Data Rate			
	82077SL-1		1M	bits/sec
	82077SL		1M	bits/sec
	82077SL-5		500K	bits/sec
t44	Data Rate Period = 1/f44			
tLOCK	Lockup Time		64	t44

NOTES:

1. This timing is for FIFO threshold = 1. When FIFO threshold is N bytes, the value should be multiplied by N and subtract 1.5 µs. The value shown is for 1 Mbps, scales linearly with data rate.
2. This value can range from 0.5 ms to 8.0 ms and is dependent upon data rate and the Specify command value.
3. Many timings are a function of the selected data rate. The nominal values for the internal clock period (t5) for the various data rates are:

1 Mbps	3 x oscillator period = 125 ns
500 Kbps	6 x oscillator period = 250 ns
300 Kbps	10 x oscillator period = 420 ns
250 Kbps	12 x oscillator period = 500 ns

4. If $\overline{DACK}$ transitions before $\overline{RD}$, then this specification is ignored. If there is no transition on $\overline{DACK}$, then this becomes the DRQ inactive delay.
5. Reset requires a stable oscillator to meet the minimum active period.
6. Based on the internal clock period (t5). For various data rates, the Write Data Width minimum values are:

1 Mbps	5 x oscillator period −50 ns = 150 ns
500 Kbps	10 x oscillator period −50 ns = 360 ns
300 Kbps	16 x oscillator period −50 ns = 615 ns
250 Kbps	19 x oscillator period −50 ns = 740 ns

7. Test points for clock high time are 3.5V. Due to transitional times, clock high time max and clock low time max cannot be met simultaneously. Clock high time min and clock low time max cannot be met simultaneously.
8. Based on internal clock period (t5).
9. Jitter tolerance is defined as: $\frac{\text{Maximum bit shift from nominal position}}{\text{1/4 period of nominal data rate}} \times 100\%$

It is a measure of the allowable bit jitter that may be present and still be correctly detected. The data separator jitter tolerance is measured under dynamic conditions that jitters the bit stream according to a reverse precompensation algorithm.

10. TC width is defined as the time that both TC and DACK are active.

A.C. SPECIFICATIONS (Continued)

NOTES: (Continued)

11. The minimum reset active period for a software reset is dependent on the data rate, after the 82077SL has been properly reset using the t30 spec. The minimum software reset period then becomes:

1 Mbps	3 x t4 = 125 ns
500 Kbps	6 x t4 = 250 ns
300 Kbps	10 x t4 = 420 ns
250 Kbps	12 x t4 = 500 ns

12. Status Register's status bits which are not latched may be updated during a Host read operation.
13. The minimum MFM values for WE to HDSEL change (t41) for the various data rates are:

1 Mbps	0.5 ms + [8 x GPL]
500 Kbps	1.0 ms + [16 x GPL]
300 Kbps	1.6 ms + [26.66 x GPL]
250 Kbps	2.0 ms + [32 x GPL]

GPL is the size of gap 3 defined in the sixth byte of a Write Command.

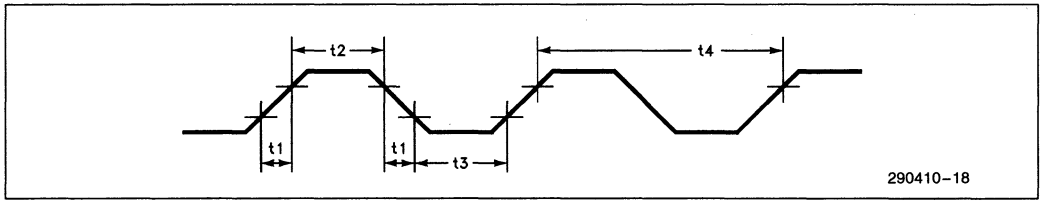
14. This timing is a function of the selected data rate as follows:

1 Mbps	1.0 μs Min
500 Kbps	2.0 μs Min
300 Kbps	3.3 μs Min
250 Kbps	4.0 μs Min

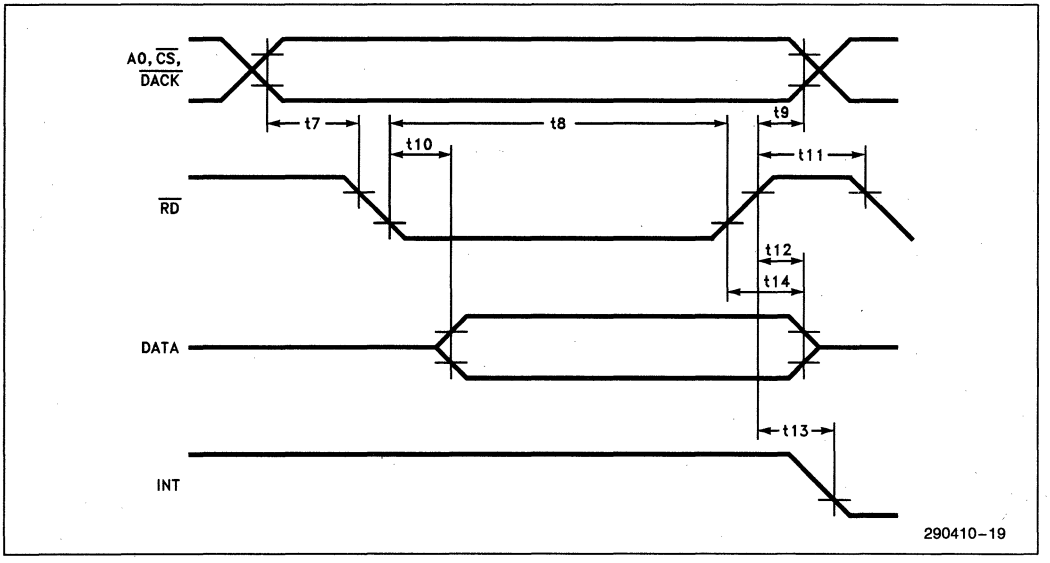
15. This timing is a function of the internal clock period (t5) and is given as (2/3) t5. The values of t5 are shown in Note 3.
16. The timings t13 and t21 are specified for INT signal in the polling mode only. These timings in case of the result phase of the read and write commands are microcode dependent.
17.

Part Specification	Supported Feature	
	Tape Drive Mode	Perpendicular Mode
82077SL-1	Yes	Yes
82077SL		Yes
82077SL-5		

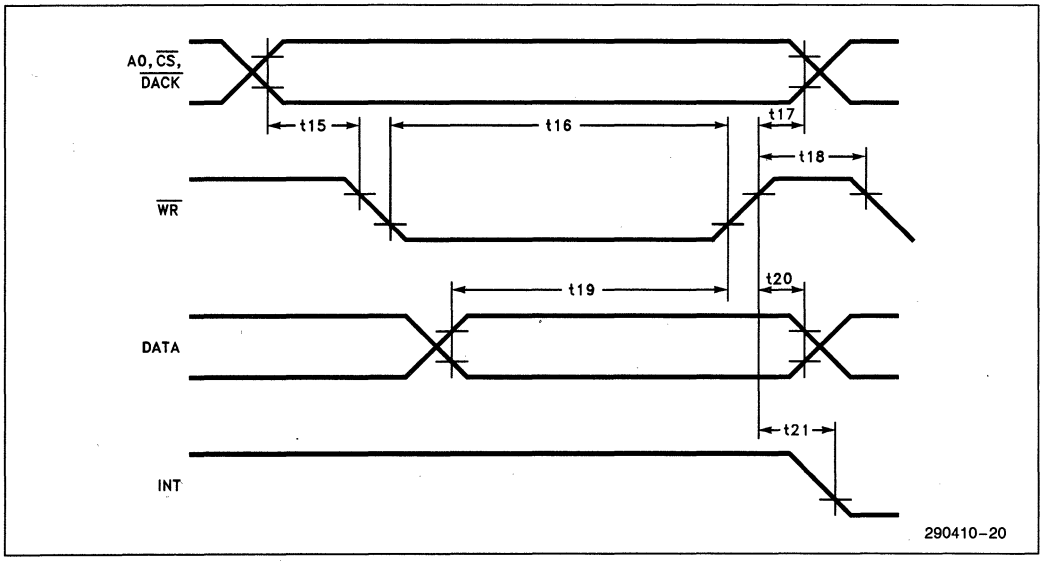
CLOCK TIMINGS



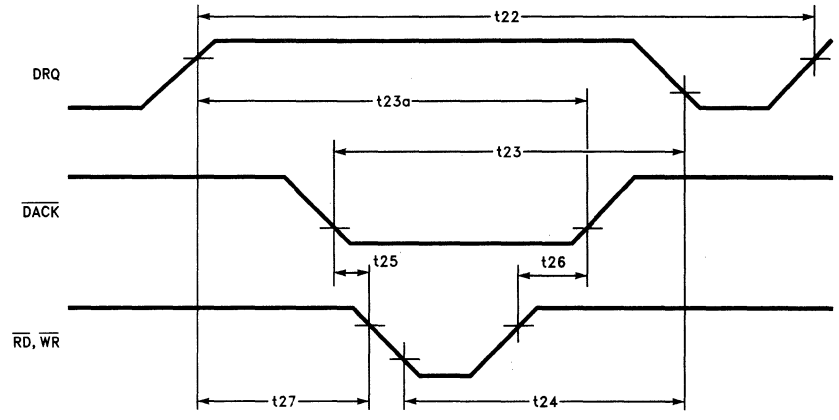
HOST READ CYCLES



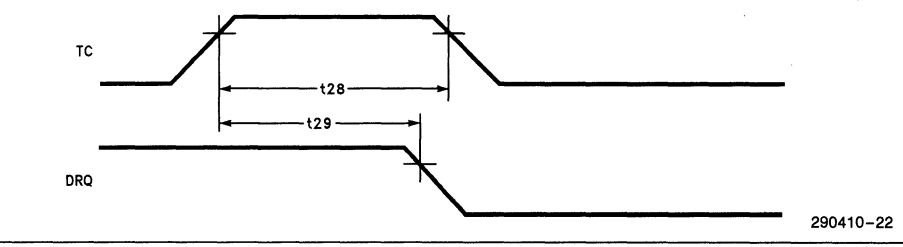
HOST WRITE CYCLES



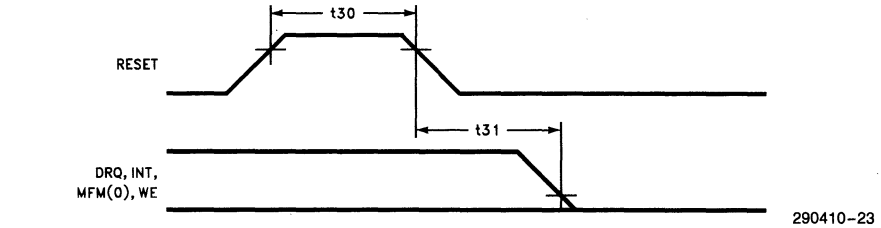
DMA CYCLES



TERMINAL COUNT

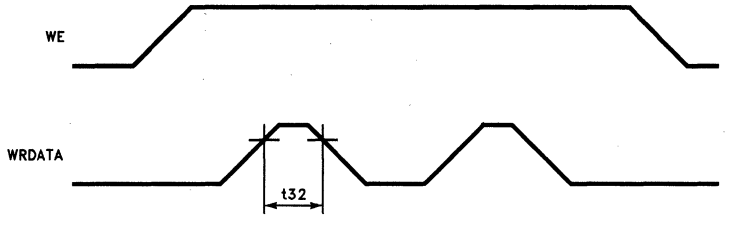


RESET



NOTE:
MFM(0) refers to the MFM pin left open during hardware reset.

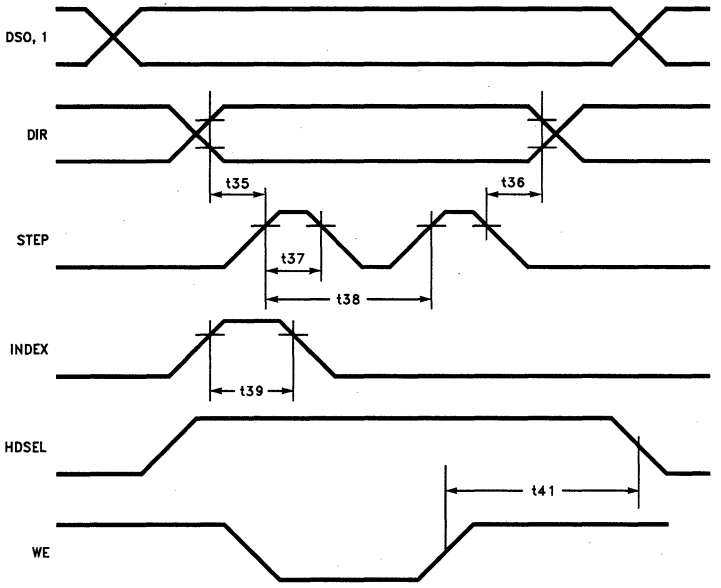
WRITE DATA TIMING



290410-24

NOTE:
Invert high.

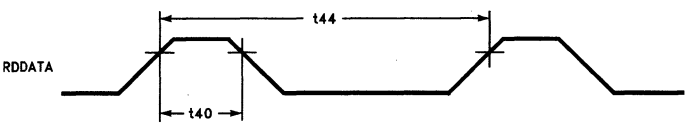
DRIVE CONTROL



290410-25

NOTE:
For overlapped seeks, only one step pulse per drive selection is issued. Non-overlapped seeks will issue all programmed step pulses. Invert high.

INTERNAL PLL



290410-26

NOTE:
Invert high.

13.0 DATA SEPARATOR CHARACTERISTICS FOR FLOPPY DISK MODE

Figure 13-1. Typical Jitter Tolerance vs Data Rate (Capture Range) (250 Kbps)

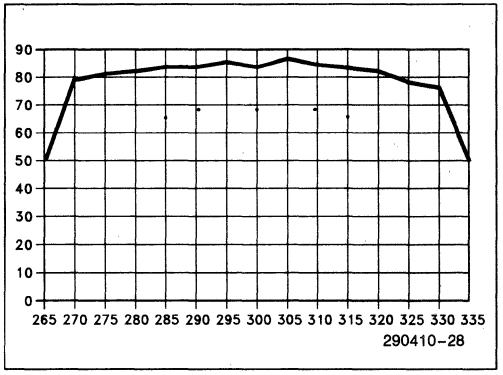


Figure 13-2. Typical Jitter Tolerance vs Data Rate (Capture Range) (300 Kbps)

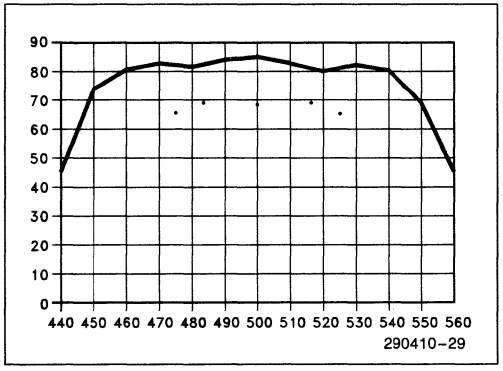


Figure 13-3. Typical Jitter Tolerance vs Data Rate (Capture Range) (500 Kbps)

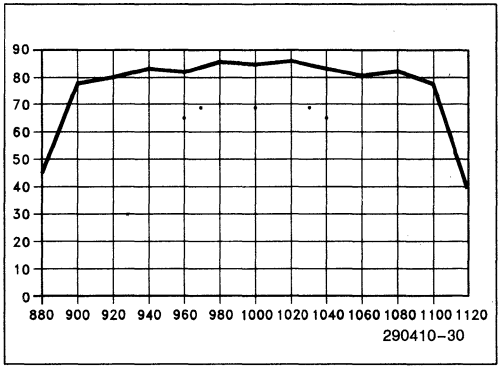


Figure 13-4. Typical Jitter Tolerance vs Data Rate (Capture Range) (1 Mbps), 82077SL-1

Jitter Tolerance measured in percent. See datasheet — Section 3.2.1 capture range expressed as a percent of data rate, i.e., ±3%.

• = Test Points:
  250, 300, 500 Kbps are center, ±3% @ 68% jitter, ±5% @ 65% jitter
  1 Mbps are center, ±3% @ 68% jitter, ±4% @ 63% jitter

Test points are tested at temperature and V_{CC} limits. Refer to the datasheet. Typical conditions are: room temperature, nominal V_{CC}.

14.0 DATA SEPARATOR CHARACTERISTICS FOR TAPE DRIVE MODE

Figure 14-1. Typical Jitter Tolerance vs Data Rate (Capture Range) (±0% ISV, 500 Kbps)

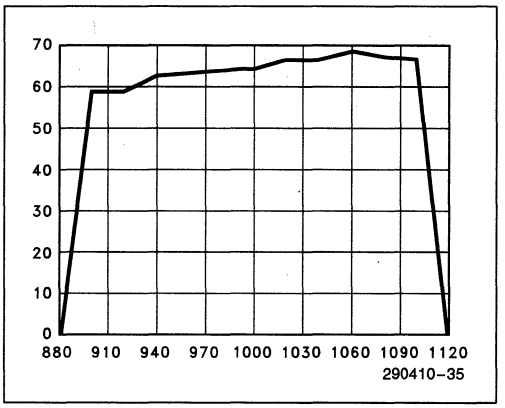


Figure 14-2. Typical Jitter Tolerance vs Data Rate (Capture Range) (±0% ISV, 1 Mbps)

Figure 14-3. Typical Jitter Tolerance vs Data Rate (Capture Range) (±3% ISV, 500 Kbps)

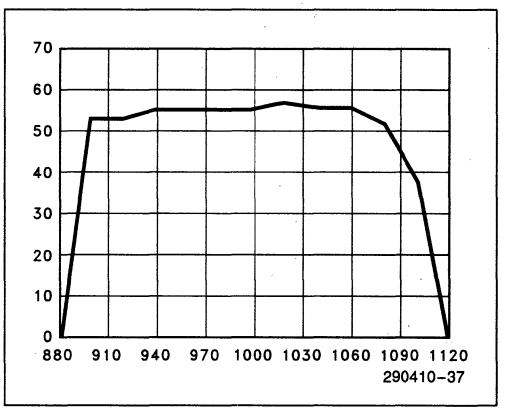


Figure 14-4. Typical Jitter Tolerance vs Data Rate (Capture Range) (±3% ISV, 1 Mbps)

NOTES:
1. Jitter Tolerance measured in percent. See datasheet — Section 3.2.1 capture range expressed as a percent of data rate, i.e., ±5%.
2. Typical conditions are: room temperature, nominal V_{CC}.

15.0 82077SL 68-LEAD PLCC PACKAGE THERMAL CHARACTERISTICS

T_A Ambient Temp. (°C)	Typical Values				θ_{ja} (°C/W)	θ_{jc} (°C/W)
	T_c (°C)	T_j (°C)	I_{cc} (mA)	V_{cc} (V)		
70	75	75	30	5.0	36	5

NOTES:
Case Temperature Formula:
$T_c = T_a + P [\theta_{ja} - \theta_{jc}]$
Junction Temperature Formula:
$T_j = T_c + p [\theta_{jc}]$
P = Power dissipated
θ_{jc} = thermal resistance from the junction to the case.
θ_{ja} = thermal resistance from the junction to the ambient.

82077SL Revision Summary

2

The following changes have been made since revision 004:

All references to the FM Mode have been removed. The 82077SL does not support the FM Mode.

The following changes have been made since revision 003:

1. The 82077SL does not support the FM Mode. All references to the FM Mode have been removed. The 82077SL does not support the FM Mode.

The following changes have been made since revision 002:

Title Page — Second paragraph, last two sentences deleted and replaced with:

The 82077SL is available in three versions—82077SL-5, 82077SL and 82077SL-1. 82077SL-1 has all features listed in this data sheet. It supports both tape drives and 4 MB floppy drives. The 82077SL supports 4 MB floppy drives and is capable of operation at all data rates through 1 Mbps. The 82077SL-5 supports 500/300/250 Kbps data rates for high and low density floppy drives.

Section 2.1.8a — Bit 7 has been changed from DSK to DSKCHG.

Section 2.3 — New sentence added to end of paragraph. This sentence reads, "$\overline{CS}$ can be held inactive during DMA transfers".

Section 6.0 — Addition of Scan Equal, Scan Low or Equal, and Scan High or Equal to Table 6-1.

Section 6.1.8 — New section added, titled "Scan Commands".

Section 12.0 — Timing diagram, DMA Cycles corrected. Symbol t26 corrected on signal $\overline{DACK}$.

82078 CHMOS SINGLE-CHIP FLOPPY DISK CONTROLLER

- **Small Footprint and Low Height Packages**
- **Supports Standard 5.0V as Well as Low Voltage 3.3V Platforms**
  - **— Selectable 3.3V and 5.0V Configuration**
  - **— 5.0V Tolerant Drive Interface**
- **Enhanced Power Management**
  - **— Application Software Transparency**
  - **— Programmable Powerdown Command**
  - **— Save and Restore Commands for 0V Powerdown**
  - **— Auto Powerdown and Wakeup Modes**
  - **— Two External Power Management Pins**
  - **— Consumes No Power While in Powerdown**
- **Programmable Internal Oscillator**
- **Floppy Drive Support Features**
  - **— Drive Specification Command**
  - **— Media ID Capability Provides Media Recognition**
  - **— Drive ID Capability Allows the User to Recognize the Type of Drive**
  - **— Selectable Boot Drive**
  - **— Standard IBM and ISO Format Features**
  - **— Format with Write Command for High Performance in Mass Floppy Duplication**
- **Integrated Host/Disk Interface Drivers**
- **Integrated Analog Data Separator**
  - **— 250 Kbits/sec**
  - **— 300 Kbits/ sec**
  - **— 500 Kbits/ sec**
  - **— 1 Mbits/sec**
  - **— 2 Mbits/sec**
- **Integrated Tape Drive Support**
  - **— Standard 1 Mbps/500 Kbps/ 250 Kbps Tape Drives**
  - **— New 2 Mbps Tape Drive Mode**
- **Perpendicular Recording Support for 4 MB Drives**
- **Fully Decoded Drive Select and Motor Signals**
- **Programmable Write Precompensation Delays**
- **Addresses 256 Tracks Directly, Supports Unlimited Tracks**
- **16 Byte FIFO**
- **Single-Chip Floppy Disk Controller Solution for Portables and Desktops**
  - **— 100% PC-AT* Compatible**
  - **— 100% PS/2* Compatible**
  - **— 100% PS/2 Model 30 Compatible**
  - **— Fully Compatible with Intel's 386SL Microprocessor SuperSet**
  - **— Integrated Drive and Data Bus Buffers**
- **Available in 64 Pin QFP and 44 Pin QFP Package**
  (See Package Specification Order Number 240800, Package Type S)

The 82078 Product Family brings a set of enhanced floppy disk controllers. These include several features that allow for easy implementation in both the portable and desktop market. The current family includes a 64 pin and a 44 pin part in the smaller form factor QFP package. The 3.3V version of the 64 pin part provides an ideal solution for the rapidly emerging 3.3V platforms. It also allows for a 5.0V tolerant floppy drive interface that lets the users retain their normal 5.0V drives. Another version of the 64 pin part provides support for 2 Mbps data rate tape drives.

*Other brands and names are the property of their respective owners.

February 1994
Order Number: 290468-003

Table 1-0. 64 Pin Part Versions

	3.3V	5.0V	2 Mbps Data Rate
82078SL	X	X	
82078-1		X	X

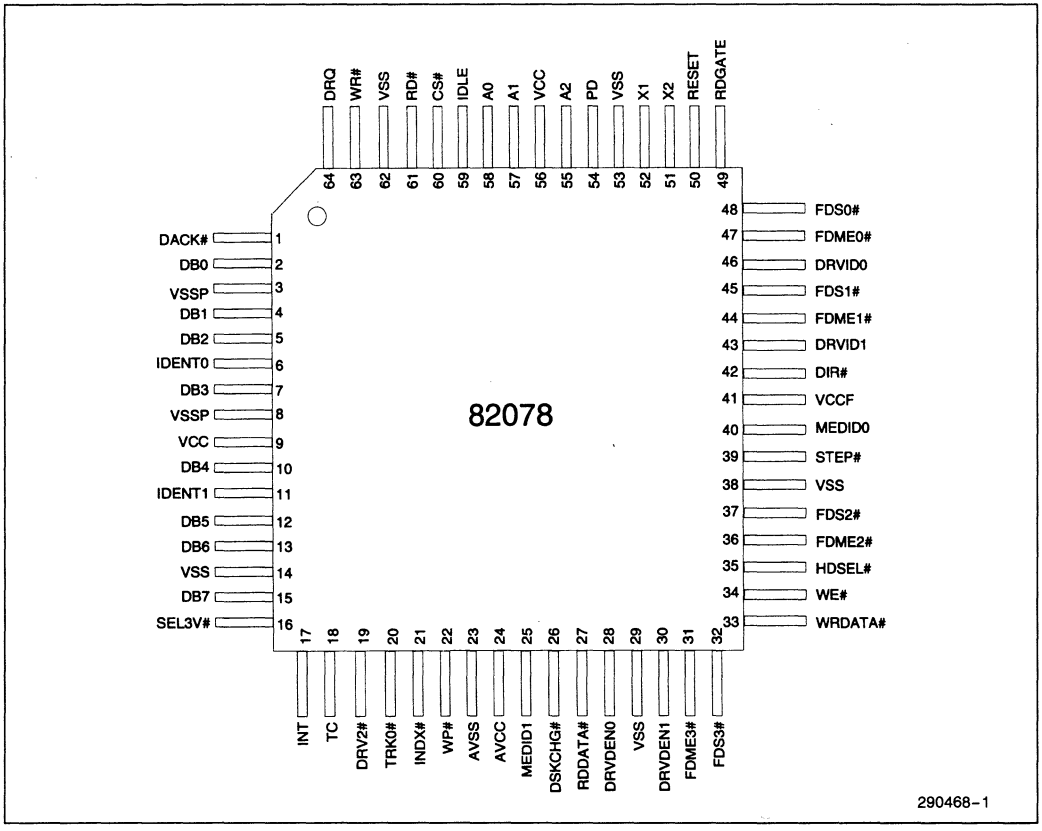
The 44 pin is targeted for platforms that are operated at 3.3V or 5.0V and do not require more than two drive support. The 82078-5 is designed for price sensitive 5.0V designs which do not include 4 MB drive support.

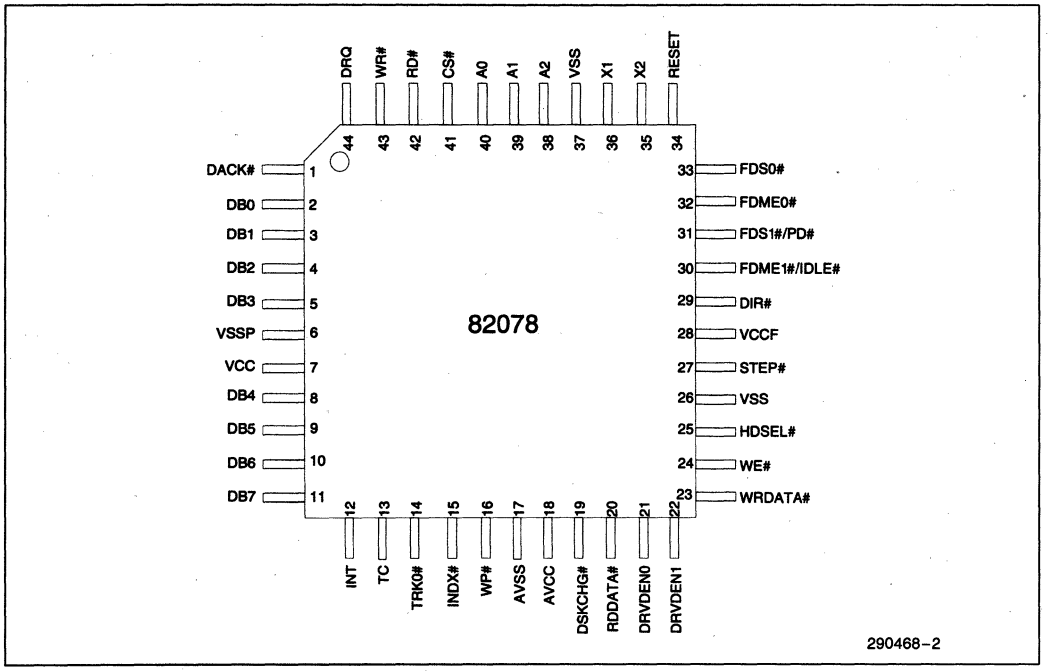
Table 2-0. 44 Pin Part Versions

	3.3V	5.0V	1 Mbps Data Rate
82078		X	X
82078-5		X	
82078-3	X		X

Both parts can be operated at 1 Mbps/500 Kbps/300 Kbps/250 Kbps. Additionally, one version of the 64 pin part provides 2 Mbps data rate operation specific for the new tape drives.

The 82078 is fabricated with Intel's advanced CHMOS III technology.




82078
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WR# 43
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CS# 41
A0 40
A1 39
A2 38
VSS 37
X1 36
X2 35
RESET 34
DACK# 1
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DB1 3
DB2 4
DB3 5
VSSP 6
VCC 7
DB4 8
DB5 9
DB6 10
DB7 11
33 FDS0#
32 FDME0#
31 FDS1#/PD#
30 FDME1#/IDLE#
29 DIR#
28 VCCF
27 STEP#
26 VSS
25 HDSEL#
24 WE#
23 WRDATA#
12 INT
13 TC
14 TRK0#
15 INDX#
16 WP#
17 AVSS
18 AVCC
19 DSKCHG#
20 RDDATA#
21 DRVDEN0
22 DRVDEN1
290468-2

82078 44 PIN
CHMOS SINGLE-CHIP FLOPPY DISK CONTROLLER

- **Small Footprint and Low Height Package**
- **Enhanced Power Management**
  - **— Application Software Transparency**
  - **— Programmable Powerdown Command**
  - **— Save and Restore Commands for Zero-Volt Powerdown**
  - **— Auto Powerdown and Wakeup Modes**
  - **— Two External Power Management Pins**
  - **— Consumes No Power While in Powerdown**
- **Integrated Analog Data Separator**
  - **— 250 Kbps**
  - **— 300 Kbps**
  - **— 500 Kbps**
  - **— 1 Mbps**
- **Programmable Internal Oscillator**
- **Floppy Drive Support Features**
  - **— Drive Specification Command**
  - **— Selectable Boot Drive**
  - **— Standard IBM and ISO Format Features**
  - **— Format with Write Command for High Performance in Mass Floppy Duplication**
- **Integrated Tape Drive Support**
  - **— Standard 1 Mbps/500 Kbps/ 250 Kbps Tape Drives**
- **Perpendicular Recording Support for 4 MB Drives**
- **Integrated Host/Disk Interface Drivers**
- **Fully Decoded Drive Select and Motor Signals**
- **Programmable Write Precompensation Delays**
- **Addresses 256 Tracks Directly, Supports Unlimited Tracks**
- **16 Byte FIFO**
- **Single-Chip Floppy Disk Controller Solution for Portables and Desktops**
  - **— 100% PC/AT* Compatible**
  - **— Fully Compatible with Intel386™ SL**
  - **— Integrated Drive and Data Bus Buffers**
- **Separate 5.0V and 3.3V Versions of the 44 Pin part are Available**
- **Available in a 44 Pin QFP Package**

2

The 82078, a 24 MHz crystal, a resistor package, and a device chip select implements a complete solution. All programmable options default to 82078 compatible values. The dual PLL data separator has better performance than most board level/discrete PLL implementations. The FIFO allows better system performance in multi-master (e.g., Microchannel, EISA).

The 82078 maintains complete software compatibility with the 82077SL/82077AA/8272A floppy disk controllers. It contains programmable power management features while integrating all of the logic required for floppy disk control. The power management features are transparent to any application software.

The 82078 is fabricated with Intel's advanced CHMOS III technology and is also available in a 64-lead QFP package.

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October 1994
Order Number: 290474-003

82078 44 Pin CHMOS Single-Chip Floppy Disk Controller

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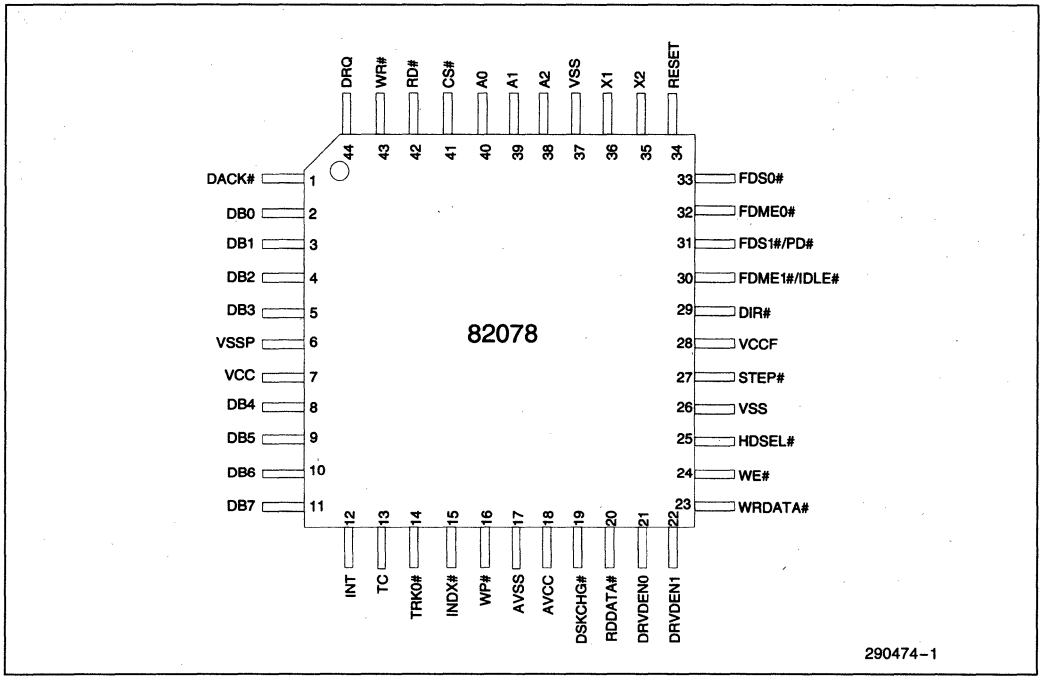

Figure 1-0. 82078 44 Pin Pinout

Table 1.0. 82078 (44 Pin) Description

Symbol	Pin #	I/O	@ H/W Reset	Description
HOST INTERFACE				
RESET	34	I	N/A	**RESET:** A high level places the 82078 in a known idle state. All registers are cleared except those set by the Specify command.
A0 A1 A2	40 39 38	I	N/A	**ADDRESS:** Selects one of the host interface registers: **A2 A1 A0 Access Register** 0 0 0 R Reserved 0 0 1 R/W Status Register B SRB 0 1 0 R/W Digital Output Register DOR 0 1 1 R/W Tape Drive Register TDR 1 0 0 R Main Status Register MSR 1 0 0 W Data Rate Select Register DSR 1 0 1 R/W Data Register (FIFO) FIFO 1 1 0 Reserved 1 1 1 R Digital Input Register DIR 1 1 1 W Configuration Control Register CCR
CS#	41	I	N/A	**CHIP SELECT:** Decodes the base address range and qualifies RD# and WR#.
RD#	42	I	N/A	**READ:** Read control signal for data transfers from the floppy drive to the system.

Table 1.0 82078 (44 Pin) Description (Continued)

Symbol	Pin #	I/O	@ H/W Reset	Description
HOST INTERFACE (Continued)				
WR#	43	I	N/A	**WRITE:** Write control signal for data transfers to the floppy drive from the system.
DRQ	44	O		**DMA REQUEST:** Requests service from a DMA controller. Normally active high, but will go to high impedance in AT and Model 30 modes when the appropriate bit is set in the DOR.
DACK#	1	I	N/A	**DMA ACKNOWLEDGE:** Control input that qualifies the RD#, WR# inputs in DMA cycles. Normally active low, but is disabled in AT and Model 30 modes when the appropriate bit is set in the DOR.
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	2 3 4 5 8 9 10 11	I/O		**DATA BUS:** 12 mA data bus.
INT	12	O		**INTERRUPT:** Signals a data transfer in non-DMA mode and when status is valid. Normally active high, but goes to high impedance when the appropriate bit is set in the DOR.
TC	13	I	N/A	**TERMINAL COUNT:** Control line from a DMA controller that terminates the current disk transfer. TC is effective only when qualified by DACK#. This input is active high.
X1 X2	36 35		N/A	**EXTERNAL CLOCK OR CRYSTAL:** Connection for a 24 MHz fundamental mode parallel resonant crystal. X1 can also be driven by an external clock (external oscillator) which can be either at 48 MHz or 24 MHz. If external oscillator is used then the PDOSC bit can be set to turn off the internal oscillator. Also, if a 48 MHz external oscillator is used then the CLK48 bit must be set in the enhanced CONFIGURE command.
PLL SECTION				
RDDATA#	20	I	N/A	**READ DATA:** Serial data from the floppy disk.
DISK CONTROL				
TRK0#	14	I	N/A	**TRACK0:** This is an active low signal that indicates that the head on track 0.
INDX#	15	I	N/A	**INDEX:** This is an active low signal that indicates the beginning of the track.
WP#	16	I	N/A	**WRITE PROTECT:** This is an active low signal that indicates whether the floppy disk in the drive is write protected.
DSKCHG#	19	I	N/A	**DISK CHANGE:** This is an input from the floppy drive reflected in the DIR.
DRVDEN0, DRVDEN1	21 22	O		**DRIVE DENSITY:** These signals are used by the floppy drive to configure the drive for the appropriate media.
WRDATA#	23	O		**WRITE DATA:** MFM serial data to the drive. Precompensation value is selectable through software.

Table 1.0 82078 (44 Pin) Description (Continued)

Symbol	Pin #	I/O	@ H/W Reset	Description
DISK CONTROL (Continued)				
WE#	24	O		**WRITE ENABLE:** Floppy drive control signal that enables the head to write onto the floppy disk.
STEP#	27	O		**STEP:** Supplies step pulses to the floppy drive to move the head between tracks.
DIR#	29	O		**DIRECTION:** It is an active low signal which controls the direction the head moves when a step signal is present. The head moves inwards towards the center if this signal is active.
HDSEL#	25	O		**HEAD SELECT:** Selects which side of the floppy disk is to be used for the corresponding data transfer. It is active low and an active level selects head 1, otherwise it defaults to head 0.
FDME0#	32	O		**FLOPPY DRIVE MOTOR ENABLE 0:** Decoded motor enable for drive 0. The motor enable pins are directly controlled via the DOR and are a function of the mapping based on BOOTSEL bits in the TDR.
FDME1#/IDLE#	30	O		**FLOPPY DRIVE MOTOR ENABLE** or **IDLE:** One of these is selected based on the level of the 44PDEN bit in the auto powerdown command. **FLOPPY DRIVE MOTOR ENABLE 1:** Decoded motor enable for drive 1. The motor enable pins are directly controlled via the DOR and are a function of the mapping based on BOOTSEL bits in the TDR. **IDLE:** This pin indicates that the part is in the IDLE state and can be powered down. IDLE state is defined as MSR = 80H, INT = 0, and the head being "unloaded" (as defined in the section describing powerdown). Whenever the part is in this state, IDLE pin is active low. If the part is powered down by the Auto Powerdown Mode, IDLE pin is set low. If the part is powered down by setting the DSR POWERDOWN bit, IDLE pin is set high.
FDS0#	33	O		**FLOPPY DRIVE SELECT 0:** Decoded floppy drive select for drive 0. These outputs are decoded from the select bits in the DOR and are a function of the mapping based on BOOTSEL bits in the TDR.
FDS1#/PD#	31	O		**FLOPPY DRIVE MOTOR ENABLE** or **PD:** One of these is selected based on the level of the 44PDEN bit in the auto powerdown command. **FLOPPY DRIVE SELECT 1:** Decoded floppy drive select for drive 1. These outputs are decoded from the select bits in the DOR and are a function of the mapping based on BOOTSEL bits in the TDR. **POWERDOWN:** This pin is active low whenever the part is in powerdown state, either via DSR POWERDOWN bit or via the Auto Powerdown Mode. This pin can be used to disable an external oscillator's output.

Table 1.0. 82078 (44 Pin) Description (Continued)

Symbol	Pin #	I/O	@ H/W Reset	Description
POWER AND GROUND SIGNALS				
V_{CC}	7		N/A	**Power Supply***
V_{SSP}	6		N/A	**GROUND:** 0V
V_{SS}	26 37		N/A	**GROUND:** 0V
AV_{CC}	18		N/A	**ANALOG VOLTAGE**
V_{CCF}	28		N/A	**VOLTAGE:** +5V for a 5V floppy drive, +3.3V for a 3.3V drive.
AV_{SS}	17		N/A	**ANALOG GROUND**

NOTE:
*The digital power supply V_{CC} and the analog power supply AV_{CC} should either be the same or regulated to be within 0.1V of either.

1.0 INTRODUCTION

The 82078 (44 pin) enhanced floppy disk controller incorporates several new features allowing for easy implementation in both the portable and desktop markets. It provides a low cost, small form factor solution targeted for 5.0V and 3.3V platforms that do not require more than two drive support.

The 82078 (44 pin) implements these new features while remaining functionally compatible with 82077SL/82077AA/8272A floppy disk controllers.

Together with a 24 MHz crystal, a resistor package and a device chip select, these devices allow for the most integrated solution available. The integrated analog PLL data separator has better performance than most board level discrete PLL implementations and can be operated at 1 Mbps/500 Kbps/ 300 Kbps/250 Kbps. A 16-byte FIFO substantially improves system performance especially in multi-master systems (e.g. Microchannel, EISA).

Figure 1-1 is a block diagram of the 82078.

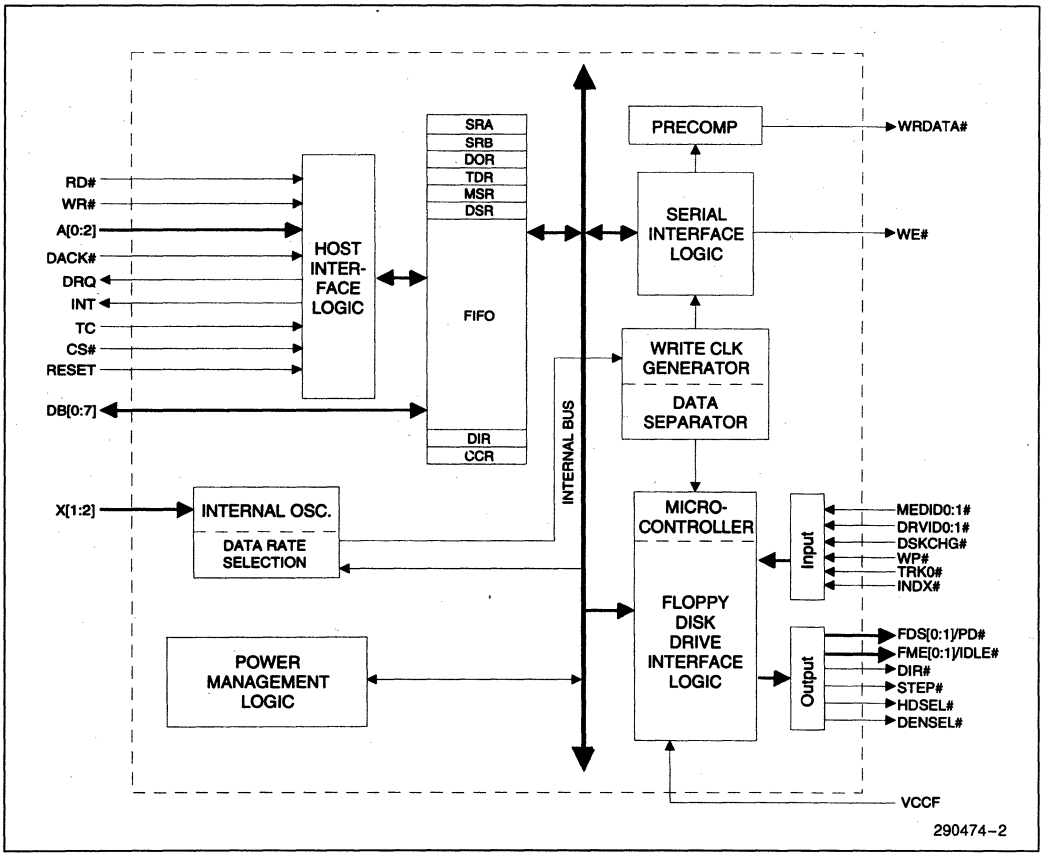

Figure 1-1. 82078 Block Diagram

2.0 MICROPROCESSOR INTERFACE

The interface consists of the standard asynchronous signals: RD#, WR#, CS#, A0–A2, INT, DMA control and a data bus. The address lines select between configuration registers, the FIFO and control/status registers.

2.1 Status, Data, and Control Registers

As shown below, the base address range is supplied via the CS# pin. For PC-AT or PS/2 designs, the primary and secondary address ranges are 3F0 Hex to 3F7 Hex and 370 Hex to 377 Hex respectively.

A2	A1	A0	Access Type	Register	
0	0	0		Reserved	
0	0	1	R/W	Status Register B	SRB
0	1	0	R/W	Digital Output Register	DOR
0	1	1	R/W	Tape Drive Register	TDR
1	0	0	R	Main Status Register	MSR
1	0	0	W	Data Rate Select Register	DSR
1	0	1	R/W	Data (First In First Out)	FIFO
1	1	0		Reserved	
1	1	1	R	Digital Input Register	DIR
1	1	1	W	Configuration Control Register	CCR

In the following sections, the various registers are shown in their powerdown state. The "UC" notation stands for a value that is returned without change from the active mode. The notation "*" means that the value is reflecting the required status (for powerdown). "N/A" means not applicable. "X" indicates that the value is undefined.

2.1.1 STATUS REGISTER B (SRB, EREG EN = 1)

In the AT/EISA mode the SRB is made available whenever the EREG EN bit in the auto powerdown command is set. The register functionality is defined as follows (bits 7 through 3 are reserved):

SRB								
R/W	7	6	5	4	3	2	1	0
R	RSVD	RSVD	RSVD	RSVD	RSVD	IDLEMSK	PD	IDLE
H/W Reset	X	X	X	X	X	0	PD	IDLE
Auto PD	X	X	X	X	X	UC	UC	UC
W	0	0	0	0	0	IDLEMSK	RSVD	RSVD
H/W Reset	N/A	N/A	N/A	N/A	N/A	0	N/A	N/A
Auto PD	N/A	N/A	N/A	N/A	N/A	UC	N/A	N/A

PD and IDLE reflect the inverted values on the corresponding pins when 44PD EN = 1 (these pins are muxed with FDS1 and FDME1). The signal on the IDLE# pin can be masked by setting IDLEMSK bit high in this register. The IDLE bit will remain unaffected. Since some systems will use the IDLE# pin to provide interrupt to the SMM power management, its disabling allows less external interrupt logic and reduction in board space. Only hardware reset will clear the IDLEMSK bit to zero. When the IDLEMSK bit is set, there is no way to distinguish between autopowerdown and DSR powerdown.

NOTE:
The 44 pin versions of the 82078 are designed to support *either* PD# and IDLE# or FDME1# and FDS1#, but not both simultaneously.

IDLEMSK	IDLE# (pin)
0	unmasked
1	masked

2.1.2 DIGITAL OUTPUT REGISTER (DOR)

The Digital Output Register contains the drive select and motor enable bits, a reset bit and a DMAGATE# bit.

Bits	7	6	5	4	3	2	1	0
Function	RSVD	RSVD	MOT EN1	MOT EN0	DMA GATE#	RESET#	RSVD	DRIVE SEL
H/W Reset State	0	0	0	0	0	0	0	0
Auto PD State	0	0	0*	0*	UC	1*	UC	UC

The MOT ENx bits directly control their respective motor enable pins (FDME0–1). The DRIVE SEL bit is decoded to provide four drive select lines and only one may be active at a time. Standard programming practice is to set both MOT ENx and DRIVE SELx bits at the same time.

NOTE:
The 44 pin versions of the 82078 are designed to support *either* PD# and IDLE# or FDME1# and FDS1#, but not both simultaneously.

Table 2-1 lists a set of DOR values to activate the drive select and motor enable for each drive.

Table 2-1. Drive Activation Value

Drive	DOR Value
0	1CH
1	2DH

The DMAGATE# bit is enabled only in PC-AT. If DMAGATE# is set low, the INT and DRQ outputs are tri-stated and the DACK# and TC inputs are disabled. DMAGATE# set high will enable INT, DRQ, TC, and DACK# to the system.

The DOR reset bit and the Motor Enable bits have to be inactive when the 82078 is in powerdown. The DMAGATE# and DRIVE SEL bits are unchanged. During powerdown, writing to the DOR does not awaken the 82078 with the exception of activating any of the motor enable bits. Setting the motor enable bits active (high) will wake up the part.

This RESET# bit clears the basic core of the 82078 and the FIFO circuits when the LOCK bit is set to "0" (see Section 5.3.2 for LOCK bit definitions). Once set, it remains set until the user clears this bit. This bit is set by a chip reset and the 82078 is held in a reset state until the user clears this bit. The RESET# bit has no effect upon the register.

2.1.3 ENHANCED TAPE DRIVE REGISTER (TDR)

TDR								
R/W	**7***	**6***	**5***	**4***	**3***	**2***	**1**	**0**
R	**RSVD**	**RSVD**	**RSVD**	**RSVD**	**RSVD**	**BOOTSEL**	**TAPESEL1**	**TAPESEL0**
H/W Reset	N/A	N/A	N/A	N/A	N/A	0	0	0
Auto PD	N/A	N/A	N/A	N/A	N/A	UC	UC	UC
W	0	0	0	0	0	BOOTSEL	TAPESEL1	TAPESEL0
H/W Reset	N/A	N/A	N/A	N/A	N/A	0	0	0
Auto PD	N/A	N/A	N/A	N/A	N/A	UC	UC	UC

NOTE:
*These bits are only available when EREG EN = 1, otherwise the bits are tri-stated.

This register allows the user to assign tape support to a particular drive during initialization. Any future references to that drive number automatically invokes tape support. Hardware reset clears this register; software resets have no effect. The tape select bits are hardware RESET to zeros, making Drive 0 **not** available for tape support. Drive 0 is reserved for the floppy boot drive.

The BOOTSEL bit in the 44 pin part is used to remap the drive selects and motor enables. The functionality is as described below:

44PD EN	BOOTSEL(TDR)	Mapping
0	0	Default → DS0 → FDS0, ME0 → FDME0 DS1 → FDS1, ME1 → FDME1
0	1	DS0 → FDS1, ME0 → FDME1 DS1 → FDS0, ME1 → FDME0
1	X	DS0 → FDS0, ME0 → FDME0 DS1 → PD, ME1 → IDLE

The 44PD EN bit in the Auto Powerdown command has precedence over the BOOTSEL bit mapping as shown above.

2.1.4 DATARATE SELECT REGISTER (DSR)

Bits	7	6	5	4	3	2	1	0
Function	S/W RESET	POWER DOWN	PDOSC	PRE-COMP2	PRE COMP1	PRE COMP0	DRATE SEL1	DRATE SEL0
H/W Reset State	0	0	0	0	0	0	1	0
Auto PD State	S/W RESET	POWER DOWN	PDOSC	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0

This register ensures backward compatibility with the 82072 floppy controller and is write-only. Changing the data rate changes the timings of the drive control signals. To ensure that drive timings are not violated when changing data rates, choose a drive timing such that the fastest data rate will not violate the timing.

The PDOSC bit is used to implement crystal oscillator power management. The internal oscillator in the 82078 can be programmed to be either powered on or off via PDOSC. This capability is independent of the chip's powerdown state. Auto powerdown mode and powerdown via the POWERDOWN bit have no effect over the power state of the oscillator.

In the default state the PDOSC bit is low and the oscillator is powered up. When this bit is programmed to a one, the oscillator is shut off. Hardware reset clears this bit to a zero. Neither of the software resets (via DOR or DSR) have any effect on this bit. Note, PDOSC should only be set high when the part is in the powerdown state, otherwise the part will not function correctly and must be hardware reset once the oscillator has turned back on and stabilized. Setting the PDOSC bit has no effect on the clock input to the 82078 (the X1 pin). The clock input is separately disabled when the part is powered down. The SAVE command checks the status of PDOSC, however the RESTORE command will not restore the bit high.

S/W RESET behaves the same as DOR RESET except that this reset is self cleaning.

POWERDOWN bit implements direct powerdown. Setting this bit high will put the 82078 into the powerdown state regardless of the state of the part. The part is internally reset and then put into powerdown. No status is saved and any operation in progress is aborted. A hardware or software reset will exit the 82078 from this powerdown state.

PRECOMP 0–2 adjusts the WRDATA output to the disk to compensate for magnetic media phenomena known as bit shifting. The data patterns that are susceptible to bit shifting are well understood and the 82078 compensates the data pattern as it is written to the disk. The amount of pre-compensation is dependent upon the drive and media but in most cases the default value is acceptable.

Table 2-2. Precompensation Delays

PRECOMP	Precompensation Delays
DSR[4,3,2]	x1 @ 24 MHz
111	0.00 ns – Disabled
001	41.67
010	83.34
011	125.00
100	166.67
101	208.33
110	250.00
000	DEFAULT

Table 2-3. Default Precompensation Delays

Data Rate	Precompensation Delays (ns)
1 Mbps	41.67
0.5 Mbps	125
0.3 Mbps	125
0.25 Mbps	125

The 82078 starts pre-compensating the data pattern starting on Track 0. The CONFIGURE command can change the track that pre-compensating starts on. Table 2-2 lists the pre-compensation values that can be selected and Table 2-3 lists the default pre-compensation values. The default value is selected if the three bits are zeroes.

DRATE 0–1 select one of the four data rates as listed in Table 2-4. The default value is 250 Kbps upon after a "Hardware" reset. Other "Software" Resets do not affect the DRATE or PRECOMP bits.

Table 2-4. Data Rates

DRATESEL0	DRATESEL1	DATA RATE
1	1	1 Mbps
0	0	500 Kbps
0	1	300 Kbps
1	0	250 Kbps

2.1.5 MAIN STATUS REGISTER (MSR)

Bits	7	6	5	4	3	2	1	0
Function	RQM	DIO	NON DMA	CMD BSY	RSVD	RSVD	DRV1 BUSY	DRV0 BUSY
H/W Reset State	0	X	X	X	X	X	X	X
Auto PD State	1	0	0	0	0	0	0	0

The Main Status Register is a read-only register and is used for controlling command input and result output for all commands.

RQM—Indicates that the host can transfer data if set to 1. No access is permitted if set to a 0.

DIO—Indicates the direction of a data transfer once RQM is set. A 1 indicates a read and a 0 indicates a write is required.

NON-DMA—This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

COMMAND BUSY—This bit is set to a one when a command is in progress. It goes active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (SEEK, RECALIBRATE commands), the bit returns to a 0 after the last command byte.

DRV x BUSY—These bits are set to ones when a drive is in the seek portion of a command, including seeks and recalibrates.

Some example values of the MSR are:

- MSR = 80H; The controller is ready to receive a command.
- MSR = 90H; executing a command or waiting for the host to read status bytes (assume DMA mode).
- MSR = D0H; waiting for the host to write status bytes.

2.1.6 FIFO (DATA)

All command parameter information and disk data transfers go through the FIFO. The FIFO is 16 bytes in size and has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to an 8272A compatible mode after a "Hardware" reset (Reset via pin 32). "Software" Resets (Reset via DOR or DSR register) can also place the 82078 into 8272A compatible mode if the LOCK bit is set to "0" (See the definition of the LOCK bit), maintaining PC-AT hardware compatibility. The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 2-5 gives several examples of the delays with a FIFO. The data is based upon the following formula:

Threshold# × 1/DATA RATE × 8 − 1.5 μs = DELAY

Table 2-5. Delay Servicing Time

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate*
1 byte	1 × 8 μs − 1.5 μs = 6.5 μs
2 bytes	2 × 8 μs − 1.5 μs = 14.5 μs
8 bytes	8 × 8 μs − 1.5 μs = 62.5 μs
15 bytes	15 × 8 μs − 1.5 μs = 118.5 μs

NOTE:
*Not available on the 82078-5.

FIFO Threshold Examples	Maximum Delay to Servicing at 500 Kbps Data Rate*
1 byte	1 × 16 μs − 1.5 μs = 14.5 μs
2 bytes	2 × 16 μs − 1.5 μs = 30.5 μs
8 bytes	8 × 16 μs − 1.5 μs = 126.5 μs
15 bytes	15 × 16 μs − 1.5 μs = 238.5 μs

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the 82078 enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred. An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC.

2.1.7 DIGITAL INPUT REGISTER (DIR)

Only bit 7 is driven, all other bits remain tri-stated.

Bits	7	6	5	4	3	2	1	0
Function	DSK CHG#	—	—	—	—	—	—	—
H/W Reset State	DSK CHG#	—	—	—	—	—	—	—
Auto PD State	0	—	—	—	—	—	—	—

NOTE:
(—) means these bits are tri-stated.

DSKCHG# monitors the pin of the same name and reflects the opposite value seen on the disk cable. The DSKCHG# bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits remain tri-stated.

2.2 Reset

There are three sources of reset on the 82078; the RESET pin, a reset generated via a bit in the DOR and a reset generated via a bit in the DSR. All resets take the 82078 out of the powerdown state.

In entering the reset state, all operations are terminated and the 82078 enters an idle state. Activating reset while a disk write activity is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, and the 82078 waits for a new command. Drive polling will start unless disabled by a new CONFIGURE command.

2.2.1 RESET PIN ("HARDWARE") RESET

The RESET pin is a global reset and clears all registers except those programmed by the SPECIFY command. The DOR Reset bit is enabled and must be cleared by the host to exit the reset state.

2.2.2 DOR RESET vs DSR RESET ("SOFTWARE" RESET)

These two resets are functionally the same. The DSR Reset is included to maintain 82072 compatibility. Both will reset the 8272 core which affects drive status information. The FIFO circuits will also be reset if the LOCK bit is a "0" (see definition of the LOCK bit). The DSR Reset clears itself automatically while the DOR Reset requires the host to manually clear it. DOR Reset has precedence over the DSR Reset. The DOR Reset is set automatically upon a pin RESET. The user must manually clear this reset bit in the DOR to exit the reset state.

The t30a specification in the A.C. Specifications gives the minimum amount of time that the DOR reset must be held active. This amount of time that the DOR reset must be held active is dependent upon the data rate. 82078 requires that the DOR reset bit must be held active for at least 0.5 μs at 250 Kbps. This is less than a typical ISA I/O cycle time.

2.3 DMA Transfers

DMA transfers are enabled with the SPECIFY command and are initiated by the 82078 by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting DACK# and addresses need not be valid (CS# can be held inactive during DMA transfers).

3.0 DRIVE INTERFACE

The 82078 has integrated all of the logic needed to interface to a floppy disk or a tape drive which use floppy interface. All drive outputs have 12 mA drive capability and all inputs use a receive buffer with hysteresis. The internal analog data separator requires no external components, yet allows for an extremely wide capture range with high levels of read-data jitter, and ISV. The designer needs only to run the 82078 disk drive signals to the disk or tape drive connector.

3.1 Cable Interface

Generally, 5.25" drive uses open collector drivers and 3.5" drives use totem-pole drivers. The output buffers on the 82078 do not change between open collector or totem-pole, they are always totem-pole.

DRVDEN0 and DRVDEN1 connect to pins 2 and 6 or 33 (on most disk drives) to select the data rate sent from the drive to the 82078. The polarity of DRVDEN0 and DRVDEN1 can be programmed through the Drive Specification command (see the command description for more information).

3.2 Host and FDD Interface Drivers

The chart below shows the drive capabilities of the 82078.

Drive Requirement	3.3V (I_{OL}/I_{OH})	5.0V (I_{OL}/I_{OH})
82078 Drivers	FDD = 6 mA/−2 mA SYS = 6 mA/−2 mA	FDD = 12 mA/−4 mA SYS = 12 mA/−4 mA

Today's floppy disk drives have reduced the output buffer's drive requirements on the floppy drive interface to 6 mA per drive at 5.0V. To support 2 drives, the drive output buffer drive capability needs to be 12 mA (at 5.0V). This is a reduction from 40 mA needed on the 82077SL. At 3.3V the 82078 halves the drive capability to 6 mA (3 mA per drive).

The slew rate control on the output buffers of the 82078 has been changed to reduce noise. The di/dt of the output drivers has been controlled such that the noise on the signal is minimized. The transition times are illustrated in the table below:

Signal Edge	Transition Time (ns)
t_{HL}	>5 ns
t_{LH}	>5 ns

NOTE:
*At 5.6V, 0°C, 50 pF load, 10% V_{CC} to 90% V_{CC}.

3.3 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called Data Window, is used to internally sample the serial data. One state of Data Window is used to sample the data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

To support reliable disk reads the data separator must track fluctuations in the read data frequency. Frequency errors primarily arise from two sources: motor rotation speed variation and instantaneous speed variation (ISV). A second condition, and one that opposes the ability to track frequency shifts is the response to bit jitter.

The internal data separator consists of two analog phase lock loops (PLLs) as shown in Figure 3-1. The two PLLs are referred to as the reference PLL and the data PLL. The reference PLL (the master PLL) is used to bias the data PLL (the slave PLL). The reference PLL adjusts the data PLL's operating point as a function of process, junction temperature and supply voltage. Using this architecture it was possible to eliminate the need for external trim components.

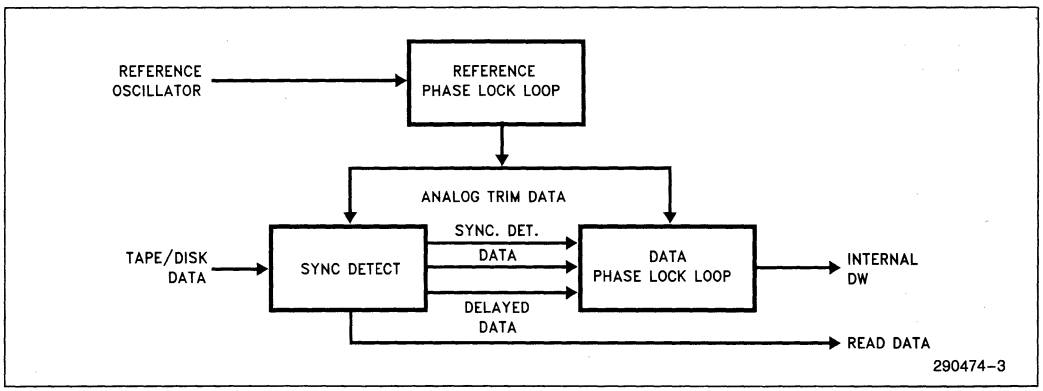

Figure 3-1. Data Separator Block Diagram

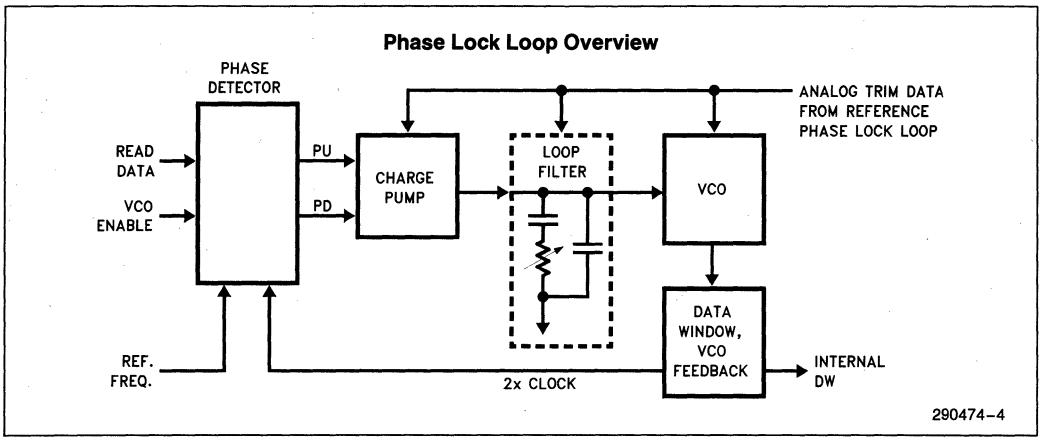

Figure 3-2. Data PLL

Figure 3-2 shows the data PLL. The reference PLL has control over the loop gain by its influence on the charge pump and the VCO. In addition, the reference PLL controls the loop filter time constant. As a result, the closed loop transfer function of the data PLL is controlled, and immune to the first order, to environmental factors and process variation.

Systems with analog PLLs are often very sensitive to noise. In the design of this data separator, many steps were taken to avoid noise sensitivity problems. The analog section of the chip has a separate V_{SS} pin (AV_{SS}) which should be connected externally to a noise free ground. This provides a clean basis for V_{SS} referenced signals. In addition, many analog circuit features were employed to make the overall system as insensitive to noise as possible.

3.3.1 JITTER TOLERANCE

The jitter immunity of the system is dominated by the data PLL's response to phase impulses. This is measured as a percentage of the theoretical data window by dividing the maximum readable bit shift by a ¼ bitcell distance. For instance, if the maximum allowable bit shift is 300 ns for a 500 Kbps data stream, the jitter tolerance is 60%.

3.3.2 LOCKTIME (t_{LOCK})

The lock, or settling time of the data PLL is designed to be 64-bit times (8 sync bytes). The value assumes that the sync field jitter is 5% the bit cell or less. This level of jitter is realistic for a constant bit pattern. Intersymbol interference should be equal, thus nearly eliminating random bit shifting.

3.3.3 CAPTURE RANGE

Capture Range is the maximum frequency range over which the data separator will acquire phase lock with the incoming RDDATA signal. In a floppy disk environment, this frequency variation is composed of two components: drive motor speed error and ISV. Frequency is a factor which may determine the maximum level of the ISV (Instantaneous Speed Variation) component. In general, as frequency increases the allowed magnitude of the ISV component will decrease. When determining the capture range requirements, the designer should take the maximum amount of frequency error for the disk drive and double it to account for media switching between drives.

3.4 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. The shifting of bits is a known phenomena of magnetic media and is dependent upon the disk media AND the floppy drive.

The 82078 monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late (or not at all) relative to the surrounding bits. Figure 3-3 is a block diagram of the internal circuit.

The top block is a 13-bit shift register with the no delay tap being in the center. This allows 6 levels of early and late shifting with respect to nominal. The shift register is clocked at the main clock rate (24 MHz). The output is fed into 2 multiplexors, one for early and one for late. A final stage of multiplexors combines the early, late and normal data stream back into one which is the WRDATA output.

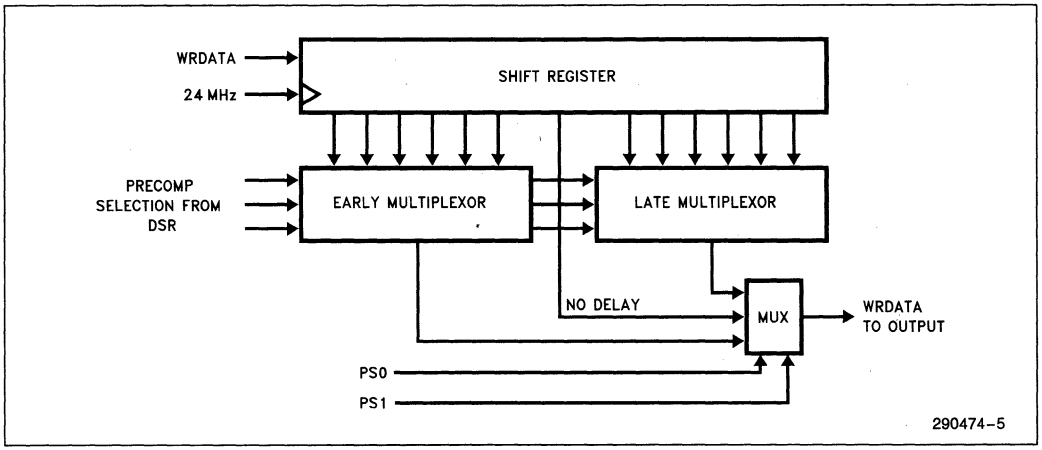

Figure 3-3. Precompensation Block Diagram

4.0 POWER MANAGEMENT FEATURES

The 82078 contains power management features that makes it ideal for design of portable personal computers. These features can be classified into power management of the part and that of the internal oscillator. The powerdown of the part is done independently of the internal oscillator in the 82078.

4.1 Power Management Scheme

The portable market share of the personal computing market has increased significantly. To improve power conservation on portable platforms, designs are migrating from 5.0V to 3.3V. Intel's 82078-3 allows designers to incorporate 3.3V floppy disk controller support in their systems.

The 82078 supports two powerdown modes, direct powerdown and automatic powerdown. Direct powerdown refers to direct action by the software to powerdown without dependence on external factors. Automatic powerdown results from 82078's monitoring of the current conditions according to a previously programmed mode. Any hardware reset disables the automatic POWERDOWN command, however software resets have no effect on the command. The 82078 also supports powerdown of its internal crystal oscillator independent of the powerdown modes described above. By setting bit 5 (PDOSC) in the DSR register, the internal oscillator is turned off. This bit has sole control of the oscillator powerdown, allowing the internal clock to be turned off when an external oscillator is used.

4.2 Oscillator Power Management

The 82078 supports a built-in crystal oscillator that can be programmed to be either powered down or active, independent of the power state of the chip. This capability is implemented by the PDOSC bit in the DSR. When PDOSC is set low, the internal oscillator is on. When PDOSC is set high, the internal oscillator is off. Note, a DSR powerdown does not turn off the oscillator.

When the external oscillator is used, power can be saved by turning off the internal oscillator. If the internal oscillator is used, the oscillator may be powered up (even when the rest of the chip is powered off) allowing the chip to wake up quickly and in a stable state. It is recommended to keep the internal oscillator on even when in the powerdown state. The main reason for this is that the recovery time of the oscillator during wake up may take tens of milliseconds under the worst case, which may create problems with any sensitive application software. In a typical application the internal oscillator should be on unless the system goes into a power saving or standby mode (such a mode request would be made by a system time out or by a user). In this case, the system software would take over and must turn on the oscillator sufficiently ahead of awakening the part.

In the case of the external oscillators, the power up characteristics are similar. If the external source remains active during the time the 82078 is powered down, then the recovery time effect is minimized. The PD# pin can be used to turn off the external source. While the PD# pin is active 82078 does not require a clock source. However, when the PD# pin is inactive, the clocking source, once it starts oscillating, must be completely stable to ensure that the 82078 operates properly.

4.3 Part Power Management

This section deals with the power management of the rest of the chip excluding the oscillator. This section explains powerdown modes and wake up modes.

4.3.1 DIRECT POWERDOWN

Direct powerdown is conducted via the POWERDOWN bit in the DSR register (bit 6). Programming this bit high will powerdown 82078. All status is lost if this type of powerdown mode is used. The part can exit powerdown from this mode via any hardware or software reset. This type of powerdown overrides the automatic powerdown. When the part is in automatic powerdown and the DSR powerdown is issued, the previous status of the part is lost and the 82078 resets to software default values.

4.3.2 AUTO POWERDOWN

Automatic powerdown is conducted via a "Powerdown Mode" command. There are four conditions required before the part will enter powerdown. All of these conditions must be true for the part to initiate the powerdown sequence. These conditions follow:

1. The motor enable pins FDME[0:1] must be inactive.
2. The part must be idle; this is indicated by MSR = 80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupt).
3. The Head Unload Timer (HUT, explained in the SPECIFY command) must have expired.
4. The auto powerdown timer must have timed out.

The command can be used to enable powerdown by setting the AUTO PD bit in the command to high. The command also provides a capability of programming a minimum power up time via the MIN DLY bit in the command. The minimum power up time refers to a minimum amount of time the part will remain powered up after being awakened or reset. An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down provided all the remaining conditions are met. Any software reset will reinitialize the timer. Changing of data rate extends the auto powerdown timer by up to 10 ms, but only if the data rate is changed during the countdown.

Disabling the auto powerdown mode cancels the timers and holds the 82078 out of auto powerdown.

The IDLE# pin can be masked via the IDLEMSK bit in Status Register B (EREG EN = 1).

4.3.3 WAKE UP MODES

This section describes the conditions for awakening the part from both direct and automatic powerdown. Power conservation or extension of battery life is the main reason power management is required. This means that the 82078 must be kept in powerdown state as long as possible and should be powered up as late as possible without compromising software transparency.

To keep the part in powerdown mode as late as possible implies that the part should wake up as fast as possible. However, some amount of time is required for the part to exit powerdown state and prepare the internal microcontroller to accept commands. Application software is very sensitive to such a delay and in order to maintain software transparency, the recovery time of the wake up process must be carefully controlled by the system software.

4.3.3.1 Wake Up from DSR Powerdown

If the 82078 enters the powerdown through the DSR powerdown bit, it must be reset to exit. Any form of software or hardware reset will serve, although DSR is recommended. No other register access will awaken the part, including writing to the DOR's motor enable (FDME[0:1]) bits.

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened by a software reset, the auto powerdown command (including the minimum delay timer) will once again become effective as previously programmed. If the part is awakened via a hardware reset, the auto powerdown is disabled.

After reset, the part will go through a normal sequence. The drive status will be initialized. The FIFO mode will be set to default mode on a hardware reset or on a software reset if the LOCK command has not blocked it. Finally, after a delay, the polling interrupt will be issued.

4.3.3.2 Wake Up from Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the 82078 resumes operation as though it was never in powerdown. Besides activating the RESET pin or

one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part)
2. A read from the MSR register
3. A read or write to the FIFO register

Any of these actions will wake up the part. Once awake, 82078 will reinitiate the auto powerdown timer for 10 ms or 0.5s (depending on the MIN DLY bit the auto powerdown command). The part will powerdown again when all the auto powerdown conditions are satisfied.

4.4 Register Behavior

The register descriptions and their values in the powerdown state are listed in the Microprocessor Interface section. Table 4-1 reiterates the configuration registers available. It also shows the type of access permitted. In order to maintain software transparency, access to all the registers must be maintained. As Table 4-1 shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Table 4-1. 82078 Register Behavior

Address	Available Registers	Access
Access to these registers DOES NOT wake up the part		
000	—	
001	SRB (EREG EN = 1)	R/W
010	DOR*	R/W
011	TDR	R/W
100	DSR*	W
110	—	—
111	DIR	R
111	CCR	W
Access to these registers wakes up the part		
100	MSR	R
101	FIFO	R/W

NOTE:
*Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (either via DOR or DSR reset bits) will wake up the part.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in Section 2.1. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed. None of the extended registers effect the behavior of the powerdown mode.

4.5 Pin Behavior

The 82078 is specifically designed for the portable PC systems in which the power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of 82078 can be divided into two major categories; system interface and floppy disk drive interface. The floppy disk drive pins are disabled such that no power will be drawn through the 82078 as a result of any voltage applied to the pin within the 82078's power supply range. The floppy disk drive interface pins are configurable by the FDI TRI bit in the auto powerdown command. When the bit is set the output pins of the floppy disk drive retain their original state. All other pins are either disabled or unchanged as depicted in Table 4-4. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

4.5.1 System Interface Pins

Table 4-2 gives the state of the system interface pins in the powerdown state. Pins unaffected by powerdown are labeled "UC". Input pins are "DISABLED" to prevent them from causing currents internal to the 82078 when they have indeterminate input values.

Table 4-2. System Interface Pins

System Pins	State In Power Down	System Pins	State In Power Down
Input Pins		Output Pins	
CS#	UC	DRQ	UC (Low)
RD#	UC	INT	UC (Low)
WR#	UC	PD#*	HIGH
A[0:2]	UC	IDLE#*	High (Auto PD) Low (DSR PD)
DB[0:7]	UC	DB[0:7]	UC
RESET	UC		
DACK#	Disabled		
TC	Disabled		
X[1:2]	Programmable		

NOTE:
*These pins are muxed with FDS1 and FDME1 and are only available when 44PD EN = 1.

Two pins which can be used to indicate the status of the part are IDLE# and PD#. Table 4-3 shows how these pins reflect the 82078 status. Note that these pins are only enabled when 44PD EN = 1.

Table 4-3. 82078 Status Pins

PD	IDLE	MSR	Part Status
1	1	80H	Auto Powerdown
1	0	RQM = 1; MSR[6:0] = X	DSR Powerdown
0	1	80H	Idle
0	0	—	Busy

The IDLE# pin indicates when the part is in idle state and can be powered down. It is a combination of MSR equaling 80H, the head being unloaded and the INT pin being low. As shown in the table, the IDLE# pin will be low when the part is in DSR powerdown state. The PD# pin is active whenever the part is in the powerdown state. It is active for either mode of powerdown. The PD# pin can be used to turn off an external oscillator of other floppy disk drive interface hardware.

4.5.2 FDD INTERFACE PINS

The FDD interface "input" pins during powerdown are disabled or unchanged as shown in Table 4-4. The floppy disk drive "output" pins are programmable by the FDI TRI bit in the auto powerdown command. Setting of the FDI TRI bit in the auto power down command results in the interface retaining its normal state. When this bit is low (default state) all output pins in the FDD interface to the floppy disk drive itself are tri-stated. Pins used for local logic control or part programming are unaffected. Table 4-4 depicts the state of the floppy disk interface pins in the powerdown state (FDI TRI is low).

Table 4-4. 82078 FDD Interface Pins

FDD Pins	State In Powerdown	FDD Pins	State In Powerdown
Input Pins		Output Pins (FDI TRI = 0)	
RDDATA#	Disabled	FDME[0:1]#	Tristated
WP#	Disabled	FDS[0:1]#	Tristated
TRK0#	Disabled	DIR#	Tristated
INDX#	Disabled	STEP#	Tristated
DSKCHG#	Disabled	WRDATA#	Tristated
		WE#	Tristated
		HDSEL#	Tristated
		DRVDEN[0:1]	Tristated

5.0 CONTROLLER PHASES

For simplicity, command handling in the 82078 can be divided into three phases: Command, Execution and Result. Each phase is described in the following sections.

When there is no command in progress, the 82078 can be in idle, drive polling or powerdown state.

5.1 Command Phase

After a reset, the 82078 enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the 82078 before the command phase is complete (Please refer to Section 6.0 for the command descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the 82078, the host must examine the RQM and DIO bits of the Main Status Register. RQM, DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the 82078 after each write cycle until the received byte is processed. The 82078 asserts RQM again to request each parameter byte of the command, unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0", and the 82078 automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to retain compatibility with the 8272A, and to provide for the proper handling of the "Invalid Command" condition.

5.2 Execution Phase

All data transfers to or from the 82078 occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the SPECIFY command.

Each data byte is transferred by an INT or DRQ depending on the DMA mode. The CONFIGURE command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, (threshold) is defined as the number of bytes available to the 82078 when service is requested from the host, and ranges from 1 to 16. The parameter FIFOTHR which the user programs is one less, and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request, for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

5.2.1 NON-DMA MODE, TRANSFERS FROM THE FIFO TO THE HOST

The INT pin and RQM bits in the Main Status Register are activated when the FIFO contains 16 (or set threshold) bytes, or the last bytes of a full sector transfer have been placed in the FIFO. The INT pin can be used for interrupt driven systems and RQM can be used for polled sytems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO, then 82078 deactivates the INT pin and RQM bit.

5.2.2 NON-DMA MODE, TRANSFERS FROM THE HOST TO THE FIFO

The INT pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The INT pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has (threshold) bytes remaining in the FIFO. The INT pin will also be deactivated if TC and DACK# both go inactive. The 82078 enters the result phase after the last byte is taken by the 82078 from the FIFO (i.e. FIFO empty condition).

5.2.3 DMA MODE, TRANSFERS FROM THE FIFO TO THE HOST

The 82078 activates the DRQ pin when the FIFO contains 16 (or set threshold) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The 82078 will deactivate the DRQ pin when the FIFO becomes empty. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of RD#, on the last byte, if no edge is present on DACK#) Note that DACK# and TC must overlap for at least 50 ns for proper functionality.

5.2.4 DMA MODE, TRANSFERS FROM THE HOST TO THE FIFO

The 82078 activates the DRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the DACK# and WR# pins and placing data in the FIFO. DRQ remains active until the FIFO becomes full. DRQ is again set true when the FIFO has (threshold) bytes remaining in the FIFO. The 82078 will also deactivate the DRQ pin when TC becomes true (qualified by DACK# by overlapping by 50 ns), indicating that no more data is required. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of WR# of the last byte, if no edge is present on DACK#).

5.2.5 DATA TRANSFER TERMINATION

The 82078 supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multisector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the 82078 will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the 82078, the internal sector count will be complete when 82078 reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the 82078 to read the last 16 bytes from the FIFO. The host must tolerate this delay.

5.3 Result Phase

The generation of INT determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the 82078 before the result phase is complete. (Refer to Section 6.0 on command descriptions.) These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read from the FIFO. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared. This indicates that the 82078 is ready to accept the next command.

6.0 COMMAND SET/DESCRIPTIONS

Commands can be written whenever the 82078 is in the command phase. Each command has a unique set of needed parameters and status results. The 82078 checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it was invalid, the next time the RQM bit in the MSR register is a "1" the DIO and CB bits will also be "1", indicating the FIFO must be read. A result byte of 80H will be read out of the FIFO, indicating an invalid command was issued. After reading the result byte from the FIFO the 82078 will return to the command phase. Table 6-1 is a summary of the Command set.

Table 6-1. 82078 Command Set

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
READ DATA										
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information Prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer Between the FDD and System
Result	R					ST 0				Status Information After Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information After Command Execution
	R					R				
	R					N				
READ DELETED DATA										
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information Prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer Between the FDD and System
Result	R					ST 0				Status Information After Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information After Command Execution
	R					R				
	R					N				
WRITE DATA										
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information Prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer Between the FDD and System
Result	R					ST 0				Status Information After Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information After Command Execution
	R					R				
	R					N				

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Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
WRITE DELETED DATA										
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information Prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer Between the FDD and System
Result	R					ST 0				Status Information After Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information After Command Execution
	R					R				
	R					N				
READ TRACK										
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information Prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer Between the FDD and System. FDC Reads All Sectors from Index Hole to EOT
Result	R					ST 0				Status Information After Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information After Command Execution
	R					R				
	R					N				
VERIFY										
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information Prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL/SC				
Execution										No Data Transfer Takes Place
Result	R					ST 0				Status Information After Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information After Command Execution
	R					R				
	R					N				
VERSION										
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
FORMAT TRACK										
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				N					Bytes/Sector
	W				SC					Sectors/Cylinder
	W				GPL					Gap3
	W				D					Filler Byte
Execution For Each Sector Repeat:	W				C					Input Sector Parameters
	W				H					
	W				R					
	W				N					
										82078 Formats an Entire Cylinder
Result	R				ST 0					Status Information After Command Execution
	R				ST 1					
	R				ST 2					
	R				Undefined					
	R				Undefined					
	R				Undefined					
	R				Undefined					
SCAN EQUAL										
Command	W	MT	MFM	SK	1	0	0	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information Prior to Command Execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared Between the FDO and Main-System
Result	R				ST 0					Status Information After Command Execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID Information After Command Execution
	R				H					
	R				R					
	R				N					

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Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
SCAN LOW OR EQUAL										
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information
	W				H					Prior to Command
	W				R					Execution
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared Between the FDO and Main-System
Result	R				ST 0					Status Information
	R				ST 1					After Command
	R				ST 2					Execution
	R				C					
	R				H					Sector ID Information
	R				R					After Command
	R				N					Execution
SCAN HIGH OR EQUAL										
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information
	W				H					Prior to Command
	W				R					Execution
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared Between the FDO and Main-System
Result	R				ST 0					Status Information
	R				ST 1					After Command
	R				ST 2					Execution
	R				C					
	R				H					Sector ID Information
	R				R					After Command
	R				N					Execution

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS0	DS1	Enhanced Controller
Execution										Head Retracted to Track 0 Interrupt
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R					ST 0				Status Information at the End of Each Seek Operation
	R					PCN				
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W			SRT				HUT		
	W				HLT				ND	
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R					ST 3				Status Information About FDD
DRIVE SPECIFICATION COMMAND										
Command	W	1	0	0	0	1	1	1	0	Command Codes
Phase	W	0	FD1	FD0	PTS	DRT1	DRT0	DT1	DT0	
	:	:	:	:	:	:	:	:	:	0–4 Bytes Issued
	W	DN	NRP	0	0	0	0	0	0	
Result	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 0
Phase	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 1
	R	0	0	0	0	0	0	0	0	RSVD
	R	0	0	0	0	0	0	0	0	RSVD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					NCN				
Execution										Head is Positioned Over Proper Cylinder on Diskette
CONFIGURE										
Command	W	0	0	0	1	0	0	1	1	Command Code
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL			FIFOTHR		
	W				PRETRK					
RELATIVE SEEK										
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					RCN				

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Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
DUMPREG										
Command Execution	W	0	0	0	0	1	1	1	0	*Note Registers Placed in FIFO
Result	R				PCN-Drive 0					
	R				PCN-Drive 1					
	R				RSVD					
	R				RSVD					
	R		SRT				HUT			
	R				HLT				ND	
	R				SC/EOT					
	R	LOCK	0	0	0	D_1	D_0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL		FIFOTHR			
	R				PRETRK					
READ ID										
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The First Correct ID Information on the Cylinder is Stored in Data Register
Result	R				ST 0					Status Information After Command Execution
	R				ST 1					
	R				ST 2					
	R				C					
	R				H					Disk Status After the Command has Completed
	R				R					
	R				N					
PERPENDICULAR MODE										
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	0	0	D_1	D0	GAP	WGATE	
LOCK										
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	
PART ID										
Command	W	0	0	0	1	1	0	0	0	Command Code
Result	R	0	1	0		—STEPPING—			1	Part ID Number
POWERDOWN MODE										
Command	W	0	0	0	1	0	1	1	1	Command Code
	W	0	0	EREG EN	44PD EN	0	FDI TRI	MIN DLY	AUTO PD	
Result	R	0	0	EREG EN	44PD EN	0	FDI TRI	MIN DLY	AUTO PD	
OPTION										
Command	W	0	0	1	1	0	0	1	1	Command Code
	W				—RSVD—				ISO	

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
					SAVE					
Command Phase	W	0	0	1	0	1	1	1	0	Command Code
Result Phase	R	RSVD	SEL 3V#*	PD OSC	PC2	PC1	PC0	DRATE1	DRATE0	Save Info to Reprogram the FDC
	R	0	0	0	0	0	0	0	ISO	
	R				PCN-Drive 0					
	R				PCN-Drive 1					
	R				RSVD					
	R				RSVD					
	R		SRT					HUT		
	R				HLT				ND	
	R				SC/EOT					
	R	LOCK	0	0	0	D_1	D_0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL			FIFOTHR		
	R				PRETRK					
	R	0	0	EREG EN	44PD EN	RSVD	FDI TRI	MIN DLY	AUTO PD	
	R				DISK/STATUS					
	R				RSVD					
					RESTORE					
Command Phase	W	0	1	0	0	1	1	1	0	Command Code
	W	0	SEL 3V#*	0	PC2	PC1	PC0	DRATE1	DRATE0	Restore Original
	W	0	0	0	0	0	0	0	ISO	Register Status
	W				PCN-Drive 0					
	W				PCN-Drive 1					
	W				RSVD					
	W				RSVD					
	W		SRT					HUT		
	W				HLT				ND	
	W				SC/EOT					
	W	LOCK	0	0	0	D_1	D_0	GAP	WGATE	
	W	0	EIS	EFIFO	POLL			FIFOTHR		
	W				PRETRK					
	W	0	0	EREG EN	44PD EN	RSVD	FDI TRI	MIN DLY	AUTO PD	
	W				DISK/STATUS					
	W				RSVD					
	W				RSVD					

NOTE:
*For the 82078, 82078-5, SEL3V# = 1. For the 82078-3, SEL3V# = 0.

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Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
FORMAT AND WRITE										
Command	W	1	MFM	1	0	1	1	0	1	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				N					
	W				SC					
	W				GPL					
	W				D					
Execution	W				C					
Repeated	W				H					Input
for each	W				R					Sector
Sector	W				N					Parameters
	W	Data Transfer of N Bytes								
										82078 Formats and Writes Entire Track
Result	R				ST 0					
Phase	R				ST 1					
	R				ST 2					
	R				Undefined					
	R				Undefined					
	R				Undefined					
	R				Undefined					
INVALID										
Command	W				Invalid Codes					Invalid Command Codes (NoOp — 82078 Goes into Standby State)
Result	R				ST 0					ST 0 = 80H

Parameter Abbreviations

Symbol **Description**

44PD EN — Powerdown pin status. This bit allows the PD and IDLE pins to be available at FDS1 and FDME1 instead of the DS1 and ME1 pins. The BOOTSEL bit in the 44 pin part remaps the drive selects and motor enables when this bit is low. See the table below for functionality:

44PD EN	BOOTSEL(TDR)	Mapping
0	0	Default → DS0 → FDS0, ME0 → FDME0 DS1 → FDS1, ME1 → FDME1
0	1	DS0 → FDS1, ME0 → FDME1 DS1 → FDS0, ME1 → FDME0
1	X	DS0 → FDS0, ME0 → FDME0 DS1 → PD, ME1 → IDLE

AUTO PD — Auto powerdown control. If this bit is 0, then the automatic powerdown is disabled. If it is set to 1, then the automatic powerdown is enabled.

C — Cylinder address. The currently selected cylinder address, 0 to 255.

D0, D1 — Drive Select 0–3. Designates which drives are Perpendicular drives, a "1" indicating Perpendicular drive.

D — Data pattern. The pattern to be written in each sector data field during formatting.

DN — Done. This bit indicates that this is the last byte of the drive specification command. The 82078 checks to see if this bit is high or low. If it is low, it expects more bytes.

DN = 0 82078 expects more subsequent bytes.

DN = 1 Terminates the command phase and jumps to the results phase. An additional benefit is that by setting this bit high, a direct check of the current drive specifications can be done.

DIR — Direction control. If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.

DS0, DS1 — Disk Drive Select.

DS1	DS0	
0	0	drive 0
0	1	drive 1
1	0	RSVD
1	1	RSVD

DTL — Special sector size. By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.

DRATE[0:1] — Data rate values from the DSR register.

DRT0, DRT1 Data rate table select. These two bits select between the different data rate tables. The default is the conventional table. These also provide mapping of the data rates selected in the DSR and CCR. The table below shows this.

Bits in DSR/CCR					
DRT0	**DRT1**	**DRATE1**	**DRATE0**	**Data Rate**	**Operation**
0	0	1	1	1 Mbps	Default
		0	0	500 Kbps	
		0	1	300 Kbps	
		1	0	250 Kbps	
0	1	RSVD	RSVD	RSVD	RSVD
1	0	RSVD	RSVD	RSVD	RSVD
1	1	1	1	1 Mbps	Perpendicular mode FDDs
		0	0	500 Kbps	
		0	1	RSVD	
		1	0	250 Kbps	

DT0, DT1 Drive density select type. These bits select the outputs on DRVDEN0 and DRVDEN1 based on mode of operation that was selected via the IDENT1 and IDENT0 pins. More information is available in the Design Applications section.

EC Enable Count. When this bit is "1" the "DTL" parameter of the Verify Command becomes SC (Number of sectors per track).

EFIFO Enable FIFO. When this bit is 0, the FIFO is enabled. A "1" puts the 82078 in the 8272A compatible mode where the FIFO is disabled.

EIS Enable implied seek. When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.

EOT End of track. The final sector number of the current track.

EREG EN Enhanced Register Enable.

EREG EN = 1 The TDR register is extended and SRB is made visible to the user.

EREG EN = 0 Standard registers are used.

FDI TRI Floppy Drive Interface Tristate: If this bit is 0, then the output pins of the floppy disk drive interface are tri-stated. This is also the default state. If it is set to 1, then the floppy disk drive interface remains unchanged.

FD0, FD1 Floppy drive select. These two bits select which physical drive is being specified. The FDn corresponds to FDSn and FDMEn on the floppy drive interface. The drive is selected independent of the BOOTSELn bits. Please refer to Section 2.1.1 which explains the distinction between physical drives and their virtual mapping as defined by the BOOTSEL1 and BOOTSEL0 bits.

FD1	**FD0**	**Drive Slot**
0	0	drive 0
0	1	drive 1
1	0	RSVD
1	1	RSVD

GAP Alters Gap2 length when using Perpendicular Mode.

GPL Gap length. The Gap3 size. (Gap3 is the space between sectors excluding the VCO synchronization field).

HDS Head address. Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.

HLT Head load time. The time interval that 82078 waits after loading the head and before initiating a read or write operation. Refer to the SPECIFY command for actual delays.

HUT Head unload time. The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the SPECIFY command for actual delays.

ISO ISO Format: If this bit is set high the ISO format is used for all data transfer commands. When this bit is set low the normal IBM system 34 and perpendicular is used. The default is ISO = 0.

Lock — Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be reset to their default values by a "Software Reset" (Reset made by setting the proper bit in the DSR or DOR registers).

MFM — MFM mode. A one selects the double density (MFM) mode. A zero is reserved.

MIN DLY — Minimum power up time control. This bit is active only if AUTO PD bit is enabled. Setting this bit to a 0, assigns a 10 ms minimum power up time and setting this bit to a 1, assigns a 0.5s minimum power up time.

MT — Multi-track selector. When set, this flag selects the multi-track operating mode. In this mode, the 82078 treats a complete cylinder, under head 0 and 1, as a single track. The 82078 operates as if this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the 82078 finishes operating on the last sector under head 0.

N — Sector size code. This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16K. It is the users responsibility to not select combinations that are not possible with the drive.

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024
..	...
07	16 Kbytes

NCN — New cylinder number. The desired cylinder number.

ND — Non-DMA mode flag. When set to 1, indicates that the 82078 is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the 82078 operates in DMA mode, interfacing to a DMA controller by means of the DRQ and DACK# signals.

NRP — No Results phase. When this bit is set high the result phase is skipped. When this bit is low the result phase will be generated.

OW — The bits denoted D0, D1, D2, and D3 of the PERPENDICULAR MODE command can only be overwritten when the OW bit is set to "1".

PCN — Present cylinder number. The current position of the head at the completion of SENSE INTERRUPT STATUS command.

PC2, PC1, PC0 — Precompensation values from the DSR register.

PDOSC — When this bit is set, the internal oscillator is turned off.

PTS — Precompensation table select. This bit selects whether to enable the precompensation value programmed in the DSR or not. In the default state, the value programmed in DSR will be used.

PTS = 0 DSR programmed precompensation delays

PTS = 1 No precompensation delay is selected for the corresponding drive.

POLL — Polling disable. When set, the internal polling routine is disabled. When clear, polling is enabled.

PRETRK — Precompensation start track number. Programmable from track 00 to FFH.

R — Sector address. The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.

RCN — Relative cylinder number. Relative cylinder offset from present cylinder as used by the RELATIVE SEEK command.

SC — Number of sectors. The number of sectors to be initialized by the FORMAT command. The number of sectors to be verified during a Verify Command, when EC is set.

SK — Skip flag. When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of READ DATA. If READ DELETED is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.

SRT — Step rate interval. The time interval between step pulses issued by the 82078. Programmable from 0.5 ms to 8 ms, in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.

ST0–3 — Status registers 0–3. Registers within the 82078 that store status information after a command has been executed. This status information is available to the host during the result phase after command execution.

STEPPING — These bits identify the stepping of the 82078.

WGATE — Write gate alters timing of WE, to allow for pre-erase loads in perpendicular drives.

6.1 Data Transfer Commands

All of the READ DATA, WRITE DATA and VERIFY type commands use the same parameter bytes and return the same results information. The only difference being the coding of bits 0–4 in the first byte.

An implied seek will be executed if the feature was enabled by the CONFIGURE command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a READ/WRITE DATA command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

6.1.1 READ DATA

A set of nine (9) bytes is required to place the 82078 into the Read Data Mode. After the READ DATA command has been issued, the 82078 loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the SPECIFY command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the 82078 reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one, and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the 82078 stops sending data, but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector terminate the READ DATA Command.

N determines the number of bytes per sector (see Table 6-2). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the 82078 transfers the specified number of bytes to the host. For reads, it continues to read the entire 128 byte sector and checks for CRC errors. For writes it completes the 128 byte sector by filling in zeroes. If N is not set to 00 Hex, DTL should be set to FF Hex, and has no impact on the number of bytes transferred.

Table 6-2. Sector Sizes

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
—	—
07	16 Kbytes

The amount of data which can be handled with a single command to the 82078 depends upon MT (multi-track) and N (Number of bytes/sector).

Table 6-3. Effects of MT and N Bits

MT	N	Max. Transfer Capacity	Final Sector Read from Disk
0	1	256 × 26 = 6656	26 at side 0 or 1
1	1	256 × 52 = 13312	26 at side 1
0	2	512 × 15 = 7680	15 at side 0 or 1
1	2	512 × 30 = 15360	15 at side 1
0	3	1024 × 8 = 8192	8 at side 0 or 1
1	3	1024 × 16 = 16384	16 at side 1

The Multi-Track function (MT) allows the 82078 to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at the last sector of the same track at Side 1.

If the host terminates a read or write operation in the 82078, then the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 6-6. The termination must be normal.

At the completion of the READ DATA Command, the head is not unloaded until after the Head Unload Time Interval (specified in the SPECIFY command) has elapsed. If the host issues another command before the head unloads then the head settling time may be saved between subsequent reads.

If the 82078 detects a pulse on the INDX# pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the 82078 sets the IC code in Status Register 0 to "01" (Abnormal termination), and sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the READ DATA Command.

After reading the ID and Data Fields in each sector, the 82078 checks the CRC bytes. If a CRC error occurs in the ID or data field, the 82078 sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the READ DATA Command.

Table 6-4 below describes the affect of the SK bit on the READ DATA command execution and results.

Table 6-4. Skip Bit vs READ DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	No	Normal Termination.
0	Deleted Data	Yes	Yes	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	Yes	No	Normal Termination.
1	Deleted Data	No	Yes	Normal Termination Sector Not Read ("Skipped").

Except where noted in Table 6-4, the C or R value of the sector address is automatically incremented (see Table 6-6).

6.1.2 READ DELETED DATA

This command is the same as the READ DATA command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 6-5 describes the affect of the SK bit on the READ DELETED DATA command execution and results.

Table 6-5. Skip Bit vs READ DELETED DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	Yes	Normal Termination.
0	Deleted Data	Yes	No	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	No	Yes	Normal Termination Sector Not Read ("Skipped").
1	Deleted Data	Yes	No	Normal Termination.

Except where noted in Table 6-5 above, the C or R value of the sector address is automatically incremented (see Table 6-6).

6.1.3 READ TRACK

This command is similar to the READ DATA command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the INDX# pin, the 82078 starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the 82078 finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The 82078 compares the ID information read from each sector with the specified value in the command, and sets the ND flag of Status Register 1 to a "1" if there is no comparison.

Multi-track or skip operations are not allowed with this command. The MT and SK bits (Bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors have been read. If the 82078 does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the INDX# pin, then it sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 6-6. Result Phase Table

MT	Head	Final Sector Transferred to Host	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
1	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	LSB	01	NC

NOTES:
NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

6.1.4 WRITE DATA

After the WRITE DATA command has been issued, the 82078 loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the SPECIFY command), and begins reading ID Fields. When the sector address read from the diskette matches the sector address specified in the command, the 82078 reads the data from the host via the FIFO, and writes it to the sector's data field.

After writing data into the current sector, the 82078 computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the 82078 continues writing to the next data field. The 82078 continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros.

The 82078 reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID Fields, it sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the WRITE DATA command.

The WRITE DATA command operates in much the same manner as the READ DATA command. The following items are the same. Please refer to the READ DATA Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command.
- Definition of DTL when N = 0 and when N does not = 0.

6.1.5 WRITE DELETED DATA

This command is almost the same as the WRITE DATA command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

6.1.6 VERIFY

The VERIFY command is used to verify the data stored on a disk. This command acts exactly like a READ DATA command except that no data is transferred to the host. Data is read from the disk, CRC computed and checked against the previously stored value.

Because no data is transferred to the host, TC (pin-25) cannot be used to terminate this command. By setting the EC bit to "1" an implicit TC will be issued to the 82078. This implicit TC will occur when the SC value has decrement to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0" DTL/SC should be programmed to 0FFH. Refer to Table 6-6 and Table 6-7 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 6-7. Verify Command Result Phase Table

MT	EC	SC/EOT Value	Termination Result
0	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

NOTE:
If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

6.1.7 FORMAT TRACK

The FORMAT command allows an entire track to be formatted. After a pulse from the INDX# pin is detected, the 82078 starts writing data on the disk including Gaps, Address Marks, ID Fields and Data Fields, per the IBM System 34 (MFM). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID Field for each sector is supplied by the host; that is, four data bytes per sector are needed by the 82078 for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the 82078 for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the 82078 encounters a pulse on the INDX# pin again and it terminates the command.

Table 6-8 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

Table 6-8. Typical PC-AT Values for Formatting

Drive Form	MEDIA	Sector Size	N	SC	GPL1	GPL2
5.25″	1.2M	512	02	0F	2A	50
	360K	512	02	09	2A	50
3.5″	2.88M	512	02	24	38	53
	1.44M	512	02	18	1B	54
	720K	512	02	09	1B	54

NOTE:
All values except Sector Size are in Hex.

Gap3 is programmable during reads, writes, and formats.

GPL1 = suggested Gap3 values in read and write commands to avoid splice point between data field and ID field of contiguous sections.

GPL2 = suggested Gap3 value in FORMAT TRACK command.

6.1.7.1 Format Fields

Table 6-9. System 34 Format Double Density

GAP 4a 80x 4E	SYNC 12x 00	IAM 3x C2	IAM FC	GAP1 50x 4E	SYNC 12x 00	IDAM 3x A1	IDAM FE	CYL	HD	SEC	NO	CRC	GAP2 22x 4E	SYNC 12x 00	DATA AM 3x A1	DATA AM FB F8	DATA	CRC	GAP3	GAP 4b

Table 6-10. ISO Format

GAP1 32x 4E	SYNC 12x 00	IDAM 3x A1	IDAM FE	CYL	HD	SEC	NO	CRC	GAP2 22x 4E	SYNC 12x 00	DATA AM 3x A1	DATA AM FB F8	DATA	CRC	GAP3	GAP 4b

Table 6-11. Perpendicular Format

GAP 4a 80x 4E	SYNC 12x 00	IAM 3x C2	IAM FC	GAP1 50x 4E	SYNC 12x 00	IDAM 3x A1	IDAM FE	CYL	HD	SEC	NO	CRC	GAP2 41x 4E	SYNC 12x 00	DATA AM 3x A1	DATA AM FB F8	DATA	CRC	GAP3	GAP 4b

6.2 Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur, the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

Table 6-12. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \not> D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} \not< D_{Proceeeor}$

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command, If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6-12 shows the status of bits SH and SN under various conditions of SCAN.

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors STP = 01, or alternate sectors STP = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 13 μs. If an Overrun occurs the FDC terminates the command.

6.3 Control Commands

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete; READ ID, RECALIBRATE and SEEK. The other control commands do not generate an interrupt.

6.3.1 READ ID

The READ ID command is used to find the present position of the recording heads. The 82078 stores the values from the first ID Field it is able to read into its registers. If the 82078 does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the INDX# pin, it then sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the SENSE INTERRUPT STATUS command. Otherwise, valuable interrupt status information will be lost.

2

6.3.2 RECALIBRATE

This command causes the read/write head within the 82078 to retract to the track 0 position. The 82078 clears the contents of the PCN counter, and checks the status of the TRK0 pin from the FDD. As long as the TRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the TRK0 pin goes high, the SE bit in Status Register 0 is set to "1", and the command is terminated. If the TRK0 pin is still low after 79 step pulses the command is terminated. Disks capable of handling more than 80 tracks per side may require more than one RECALIBRATE command to return the head back to physical Track 0.

The RECALIBRATE command does not have a result phase. SENSE INTERRUPT STATUS command must be issued after the RECALIBRATE command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the 82078 is in the BUSY state, but during the execution phase it is in a NON BUSY state. At this time another RECALIBRATE command may be issued, and in this manner, parallel RECALIBRATE operations may be done on up to 2 drives at once.

Upon power up, the software must issue a RECALIBRATE command to properly initialize all drives and the controller.

6.3.3 DRIVE SPECIFICATION COMMAND

The 82078 uses two pins, DRVDEN0 and DRVDEN1 to select the density for modern drives. These signals inform the drive of the type of diskette in the drive. The Drive Specification command specifies the polarity of the DRVDEN0 and DRVDEN1 pins. It also enables or disables DSR programmed precompensation.

This command removes the need for a hardware workaround to accommodate differing specifications among drives. By programming this command during BIOS's POST routine, the floppy disk controller will internally configure the correct values for DRVDEN0 and DRVDEN1 with corresponding precompensation value and data rate table enabled for the particular type of drive.

This command is protected from software resets. After executing the DRIVE SPEC command, subsequent software resets will not clear the programmed parameters. Only another DRIVE SPEC command or H/W reset can reset it to default values. The 6 LSBs of the last byte of this command are reserved for future use.

The DRATE0 and DRATE1 are values as programmed in the DSR register. The DENSEL is high for high data rates (1 Mbps and 500 Kbps) and low for low data rates (300 Kbps and 250 Kbps).

The following table describes the drives that are supported with the DT0, DT1 bits of the Drive Specification command:

DRVDENn Polarities

DT0	DT1	Data Rate	DRVDEN0	DRVDEN1
0*	0*	1 Mbps	1	1
		500 Kbps	1	0
		300 Kbps	0	1
		250 Kbps	0	0
0	1	1 Mbps	1	1
		500 Kbps	0	0
		300 Kbps	0	1
		250 Kbps	1	0
1	0	1 Mbps	0	1
		500 Kbps	0	0
		300 Kbps	1	1
		250 Kbps	1	0
1	1	1 Mbps	1	1
		500 Kbps	0	0
		300 Kbps	1	0
		250 Kbps	0	1

NOTE:
(*) Denotes the default setting.

6.3.4 SEEK

The read/write head within the drive is moved from track to track under the control of the SEEK command. The 82078 compares the PCN which is the current head position with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in), and issues step pulses.

PCN > NCN: Direction signal to drive set to "0" (step out), and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN, then the SE bit in Status Register 0 is set to "1", and the command is terminated.

During the command phase of the seek or recalibrate operation, the 82078 is in the BUSY state, but during the execution phase it is in the NON BUSY state.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1. SEEK command; Step to the proper track
2. SENSE INTERRUPT STATUS command; Terminate the Seek command
3. READ ID. Verify head is on proper track
4. Issue READ/WRITE command.

The SEEK command does not have a result phase. Therefore, it is highly recommended that the SENSE INTERRUPT STATUS command be issued after the SEEK command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return a "0". When exiting DSR POWERDOWN mode, the 82078 clears the PCN value and the status information to zero. Prior to issuing the DSR POWERDOWN command, it is highly recommended that the user service all pending interrupts through the SENSE INTERRUPT STATUS command.

6.3.5 SENSE INTERRUPT STATUS

An interrupt signal on INT pin is generated by the 82078 for one of the following reasons:

1. Upon entering the Result Phase of:
   a. READ DATA Command
   b. READ TRACK Command
   c. READ ID Command
   d. READ DELETED DATA Command
   e. WRITE DATA Command

f. FORMAT TRACK Command
g. WRITE DELETED DATA Command
h. VERIFY Command

2. End of SEEK, RELATIVE SEEK or RECALIBRATE Command
3. 82078 requires a data transfer during the execution phase in the non-DMA Mode

The SENSE INTERRUPT STATUS command resets the interrupt signal and via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt. If a SENSE INTERRUPT STATUS command is issued when no active interrupt condition is present, the status register ST0 will return a value of 80H (invalid command).

Table 6-13. Interrupt Indentification

SE	IC	Interrupt Due To
0	11	Polling
1	00	Normal Termination of SEEK or RECALIBRATE command
1	01	Abnormal Termination of SEEK or RECALIBRATE command

The SEEK, RELATIVE SEEK and the RECALIBRATE commands have no result phase. SENSE INTERRUPT STATUS command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a SENSE INTERRUPT STATUS is not issued, the drive, will continue to be BUSY and may effect the operation of the next command.

6.3.6 SENSE DRIVE STATUS

SENSE DRIVE STATUS obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. STATUS REGISTER 3 contains the drive status information.

6.3.7 SPECIFY

The SPECIFY command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between the command phase to the execution phase of a read/write data command. The Head Unload Time (HUT) timer starts at the end of the execution phase to the beginning of the result phase of a read/write command. The values change with the data rate speed selection and are documented in Table 6-14.

Table 6-14. Drive Control Delays (ms)

	HUT				SRT			
	1M	500K	300K	250K	1M	500K	300K	250K
0	128	256	426	512	8.0	16	26.7	32
1	8	16	26.7	32	7.5	15	25	30
—	—	—	—	—	—	—	—	—
A	80	160	267	320	3.0	6.0	10.2	12
B	88	176	294	352	2.5	5.0	8.35	10
C	96	192	320	384	2.0	4.0	6.68	8
D	104	208	346	416	1.5	3.0	5.01	6
E	112	224	373	448	1.0	2.0	3.33	4
F	120	240	400	480	0.5	1.0	1.67	2

Table 6-15. Head Load Time (ms)

	HLT			
	1M	500K	300K	250K
00	128	256	426	512
01	1	2	3.3	4
02	2	4	6.7	8
—	—	—	—	—
7E	126	252	420	504
7F	127	254	423	508

The choice of DMA or NON-DMA operations is made by the ND bit. When this bit is "1", the NON-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signalled by the DRQ pin. Non-DMA mode uses the RQM bit and the INT pin to signal data transfers.

6.3.8 CONFIGURE

Issue the configure command to enable features like the programmable FIFO and set the beginning track for pre-compensation. A CONFIGURE command need not be issued if the default values of the 82078 meet the system requirements.

CONFIGURE DEFAULT VALUES:

EIS No Implied Seeks
EFIFO FIFO Disabled
POLL Polling Enabled
FIFOTHR FIFO Threshold Set to 1 Byte
PRETRK Pre-Compensation Set to Track 0

EIS—Enable Implied Seek. When set to "1", the 82078 will perform a SEEK operation before executing a read or write command. Defaults to no implied seek.

EFIFO—A "1" puts the FIFO into the 8272A compatible mode where the FIFO is disabled. This means data transfers are asked for on a byte by byte basis. Defaults to "1", FIFO disabled. The threshold defaults to one.

POLL—Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a RESET. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR—The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte, "0F" selects 16 bytes.

PRETRK—Pre-compensation start track number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0, "FF" selects 255.

6.3.9 VERSION

The VERSION command checks to see if the controller is an enhanced type (82077, 82077AA, 82077SL) or the older type (8272A/765A). A value of 90H is returned as the result byte, defining an enhanced FDD controller is in use. No interrupts are generated. Refer to the Part ID command for more identification information on the 82078.

6.3.10 RELATIVE SEEK

The command is coded the same as for SEEK, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control

DIR	Action
0	Step Head Out
1	Step Head In

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The RELATIVE SEEK command differs from the SEEK command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The SEEK command is good for drives that support a maximum of 256 tracks. RELATIVE SEEKs cannot be overlapped with other RELATIVE SEEKs. Only one RELATIVE SEEK can be active at a time. Bit 4 of Status Register 0 (EC) will be set if RELATIVE SEEK attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks and that the host needs to read track 300 and the head is on any track (0—255). If a SEEK command was issued, the head would stop at track 255. If a RELATIVE SEEK command was issued, the 82078 would move the head the specified number of tracks, regardless of the internal cylinder position register (but would increment the register). If the head had been on track 40 (D), the maximum track that the 82078 could position the head on using RELATIVE SEEK, would be 296 (D), the initial track, +256 (D). The maximum count that the head can be moved with a single RELATIVE SEEK command is 256 (D).

The internal register, PCN, would overflow as the cylinder number crossed track 255 and would contain 40 (D). The resulting PCN value is thus (NCN + PCN) mod 256. Functionally, the 82078 starts counting from 0 again as the track number goes above 255(D). It is the users responsibility to compensate 82078 functions (precompensation track number) when accessing tracks greater than 255. The 82078 does not keep track that it is working in an "extended track area" (greater than 255). Any command issued would use the current PCN value except for the RECALIBRATE command which only looks for the TRACK0 signal. RECALIBRATE would return an error if the head was farther than 79 due to its limitation of issuing a maximum 80 step pulses. The user simply needs to issue a second RECALIBRATE command. The SEEK command and implied seeks will function correctly within the 44 (D) track (299–255) area of the "extended track area". It is the users responsibility not to issue a new track position that would exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a RELATIVE SEEK would be issued to cross the track 255 boundary.

A RELATIVE SEEK can be used instead of the normal SEEK but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a READ ID command to ensure that the head is physically on the track that software assumes it to be. Different 82078 commands will return different cylinder results which may be difficult to keep track of with software without the READ ID command.

6.3.11 DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. The command returns pertinent information regarding the internal status of the 82078. This can be used to verify the values initialized in the 82078.

6.3.12 PERPENDICULAR MODE COMMAND

Note, perpendicular mode functionality is not available on the 82078-5.

6.3.12.1 About Perpendicular Recording Mode

An added capability of the 82078 is the ability to interface directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method by orienting the magnetic bits vertically. This scheme packs in more data bits for the same area.

6.3.12.2 The Perpendicular Mode Command

The PERPENDICULAR MODE command allows the system designers to designate specific drives as Perpendicular recording drives. Data transfers between Conventional and Perpendicular drives are allowed without having to issue PERPENDICULAR MODE commands between the accesses of the two different drives, nor having to change write pre-compensation values.

With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 6-16 describes the effects of the WGATE and GAP bits for the PERPENDICULAR MODE command.

When both GAP and WGATE equal "0" the PERPENDICULAR MODE command will have the following effect on the 82078-1) if any of the new bits D0, D1, D2, and D3 are programmed to "1" the corresponding drive will automatically be programmed for Perpendicular mode (ie: GAP2 being written during a write operation, the programmed Data Rate will determine the length of GAP2.), and data will be written with 0 ns write pre-compensation. 2) Any of the new bits (D0–D1) that are programmed for "0", the designated drive, will be programmed for Conventional Mode and data will be written with the currently programmed write pre-compensation value. 3) Bits D0 and D1 can only be over written when the OW bit is written as a "1". The status of these bits can be determined by interpreting the eighth result byte of the DUMPREG command.

NOTE:
If either the GAP or WGATE bit is a "1", then bits D0–D1 are ignored.

"Software" and "Hardware" RESET will have the following effects on the enhanced PERPENDICULAR MODE command:

1. "Software" RESETs (Reset via DOR or DSR registers) will only clear GAP and WGATE bits to "0", D1 and D0 will retain their previously programmed values.
2. "Hardware" RESETs (Reset via pin-32) will clear all bits (GAP, WGATE, D0 and D1) to "0" (All Drives Conventional Mode).

Table 6-16. Effects of WGATE and GAP Bits

GAP	WGATE	MODE	VCO Low Time after Index Pulse	Length of Gap2 Format Field	Portion of Gap2 Written by Write Data Operation	Gap2 VCO Low Time for Read Operations
0	0	Conventional Mode	33 Bytes	22 Bytes	0 Bytes	24 Bytes
0	1	Perpendicular Mode (500 Kbps Data Rate)	33 Bytes	22 Bytes	19 Bytes	24 Bytes
1	0	Reserved (Conventional)	33 Bytes	22 Bytes	0 Bytes	24 Bytes
1	1	Perpendicular Mode (1 Mbps Data Rate)	18 Bytes	41 Bytes	38 Bytes	43 Bytes

NOTE:
When either GAP or WGATE bit is set, the current value of precompensation in the DSR is used.

6.3.13 POWERDOWN MODE COMMAND

The POWERDOWN MODE command allows the automatic power management and enables the enhanced registers (EREG EN) of the 82078. The use of the command can extend the battery life in portable PC applications. To enable auto powerdown the command may be issued during the BIOS power on self test (POST).

This command includes the ability to configure the 82078 into the enhanced mode extending the SRB and TDR registers. These extended registers accommodate bits that give more information about floppy drive interface, allow for boot drive selection, and identify the values of the PD and IDLE status.

As soon as the command is enabled, a 10 ms or a 0.5s minimum power up timer is initiated depending on whether the MIN DLY bit is set to 0 or 1. This timer is one of the required conditions that has to be satisfied before the part will enter auto powerdown. Any software reset will reinitialize the timer. The timer countdown is also extended by up to 10 ms if the data rate is changed during the timer's countdown. Without this timer 82078 would have been put to sleep immediately after 82078 is idle. The minimum delay gives software a chance to interact with 82078 without incurring an additional overhead due to recovery time.

The command also allows the output pins of floppy disk drive interface to be tri-stated or left unaltered during auto powerdown. This is done by the FDI TRI bit. In the default condition (FDI TRI = 0) the output pins of the floppy disk drive are tri-stated. Setting this bit leaves the interface unchanged from the normal state.

The results phase returns the values programmed for MIN DLY, FDI TRI and AUTO PD. The auto powerdown mode is disabled by a hardware reset. Software results have no effect on the POWERDOWN MODE command parameters.

6.3.14 PART ID COMMAND

This command can be used to identify the floppy disk controller as an enhanced controller. The first stepping of the 82078 (all 44 pin versions) will yield 0x41 in the result phase of this command. Any future enhancements on these parts will be denoted by the 5 LSBs (0x01 to 0x1F).

6.3.15 OPTION COMMAND

The standard IBM format includes an index address field consisting of 80 bytes of GAP4a, 12 bytes of the sync field, four bytes identifying the IAM and 50 bytes of GAP1. Under the ISO format, most of this preamble is not used. The ISO format allows only 32 bytes of GAP1 after the index mark. The ISO bit in this command allows the 82078 to configure the data transfer commands to recognize this format. The MSBs in this command are reserved for any other enhancements made available to the user in the future.

6.3.16 SAVE COMMAND

The first byte corresponds to the values programmed in the DSR with the exception of CLK48. The DRATE1, DRATE0 used here are unmapped. The second byte is used for configuring the bits from the OPTION command. All future enhancements to the OPTION command will be reflected in this byte as well. The next nine result bytes are explained in the Parameter Abbreviations section after the command summary. The 13th byte is the value associated with the auto powerdown command. The disk status is used internally by 82078. There are two reserved bytes at the end of this command for future use.

This command is similar to the Dumpreg command but it additionally allows the user to read back the precompensation values as well as the programmed data rate. It also allows the user to read the values programmed in the auto power down command. The precompensation values will be returned as programmed in the DSR register. This command is used in conjunction with the Restore command should prove very useful for SMM power management. This command reserves the last two bytes for future enhancements.

6.3.17 RESTORE COMMAND

Using Restore with the Save command, allows the SMM power management to restore the 82078 to its original state after a system powerdown. It also serves as a succinct way to provide most of the initialization requirements normally handled by the system. The sequence of initializing the 82078 after a reset occurred and assuming a Save command was issued follows:

- Issue the Drive Spec command (if the design utilizes this command)
- Issue the Restore command (pass the 16 bytes retrieved previously during SAVE)

The Restore command will program the data rate and precompensation value via the DSR. It then restores the values normally programmed through the Configure, Specify, and Perpendicular commands. It also enables the previously selected values for the AUTO Powerdown command. The PCN values are set restored to their previous values and the user is responsible for issuing the seek and recalibrate commands to restore the head to the proper location. There are some drives that do not recalibrate in which case the Restore command will restore the previous state completely. The PDOSC bit is retrievable using the Save command, however, the system designer must set it correctly. The software must allow at least 20μs to execute the Restore command. When using the BOOTSEL bits in the TDR, the user must restore or reinitialize these bits to their proper values.

6.3.18 FORMAT AND WRITE COMMAND

The format and write command is capable of simultaneously formatting and writing data to the diskette. It is essentially the same as the normal format command. With the exception that included in the execution for each sector is not only the C, H, R, and N but also the data transfer of N bytes. The D value is ignored. This command formats the entire track. High speed floppy diskette duplication can be done fast and efficiently with this command. The user can format the diskette and put data on it in a single pass. This is very useful for software duplication applications by reducing the time required to format and copy diskettes.

6.3.19 LOCK

The LOCK command is included to protect a system with long DMA latencies against older application software packages that can disable the 82078's FIFO. [Note: This command should only be used by the system's FDC routines, and ISVs (Independent Software Vendors) should refrain from using it. If an ISV's application calls for having the 82078 FIFO disabled, a CONFIGURE command should be used to toggle the EFIFO (Enable FIFO) bit. ISV can determine the value of the LOCK bit by interpreting the eighth result byte of an DUMPREG command.]

The LOCK command defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to a "1" all subsequent "software" RESETs by the DOR and DSR registers will not change the previously set parameter values in the CONFIGURE command. When the LOCK bit is set to a "0", "software" RESETs the DOR or DSR registers will return these parameters to their default values. All "hardware" Resets will set the LOCK bit to a "0" value, and will return EFIFO, FIFOTHR, and PRETRK to their default values. A Status byte is returned immediately after issuing the command byte. This Status byte reflects the value of the Lock bit set by the command byte.

NOTE:
No interrupts are generated at the end of this command.

7.0 STATUS REGISTER ENCODING

The contents of these registers are available only through a command sequence.

7.1 Status Register 0

Bit #	Symbol	Name	Description
7, 6	IC	Interrupt Code	00— Normal termination of command. The specified command was properly executed and completed without error. 01— Abnormal termination of command. Command execution was started, but was not successfully completed. 10— Invalid command. The requested command could not be executed. 11— Abnormal termination caused by Polling.
5	SE	Seek End	The 82078 completed a SEEK or RECALIBRATE command, or a READ or WRITE with implied seek command.
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the RECALIBRATE command. 2. The RELATIVE SEEK command causes the 82078 to step outward beyond Track 0.
3	—	—	Unused. This bit is always "0".
2	H	Head Address	The current head address.
1, 0	DS1, 0	Drive Select	The current selected drive.

7.2 Status Register 1

Bit #	Symbol	Name	Description
7	EN	End of Cylinder	The 82078 tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write.
6	—	—	Unused. This bit is always "0".
5	DE	Data Error	The 82078 detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the 82078 does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3	—	—	Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. READ DATA, READ DELETED DATA command, the 82078 did not find the specified sector. 2. READ ID command, the 82078 cannot read the ID field without an error. 3. READ TRACK command, the 82078 cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the 82078 is executing a WRITE DATA, WRITE DELETED DATA, or FORMAT TRACK command.
0	MA	Missing Address Mark	Any one of the following: 1. The 82078 did not detect an ID address mark at the specified track after encountering the index pulse from the INDX# pin twice. 2. The 82078 cannot detect a data address mark or a deleted data address mark on the specified track.

7.3 Status Register 2

Bit #	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	CM	Control Mark	Any of the following: 1. READ DATA command, the 82078 encounters a deleted data address mark. 2. READ DELETED DATA command, the 82078 encountered a data address mark.
5	DD	Data Error in Data Field	The 82078 detected a CRC error in the date field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82078.
3	—	—	Unused. This bit is always "0".
2	—	—	Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82078 and is equal to FF hex which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The 82078 cannot detect a data address mark or a deleted data address mark.

7.4 Status Register 3

Bit #	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5	—	—	Unused. This bit is always "1".
4	T0	TRACK 0	Indicates the status of TRK0 pin.
3	—	—	Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1, 0	DS1, 0	Drive Select	Indicates the status of the DS1, DS0 pins.

8.0 COMPATIBILITY

The 82078 was designed with software compatibility in mind. It is a fully backwards compatible solution with the older generation 8272A and NEC765A/B disk controllers. It is fully compatible with Intel's 386/486SL Microprocessor Superset.

8.1 Compatibility with the FIFO

The FIFO of the 82078 is designed to be transparent to non-FIFO disk controller software developed on the older generation 8272A standard. Operation of the 82078 FIFO can be broken down into two tiers of compatibility. For first tier compatibility, the FIFO is left in the default disabled condition upon a "Hardware" reset. In this mode the FIFO operates in a byte mode and provides complete compability with non-FIFO based software. For second tier compatibility, the FIFO is enabled via the CONFIGURE command. When the FIFO is enabled, it will temporarily enter a byte mode during the command and result phase of disk controller operation. This allows for compatible operation when interrogating the Main Status Register (MSR) for the purpose of transferring a byte at a time to or from the disk controller. For normal disk controller applications, the system designer can still take advantage of the FIFO for time critical data transfers during the execution phase and not create any conflicts with non-FIFO software during the command or result phase.

In some instances, use of the FIFO in any form has conflicted with certain specialized software. An example of a compatibility conflict using the FIFO is with software that monitors the progress of a data transfer during the execution phase. If the software assumed the disk controller was operating in a single byte mode and counted the number of bytes transferred to or from the disk controller to trigger some time dependent event on the disk media (i.e. head position over a specific data field), the same software will not have an identical time relationship if the FIFO is enabled. This is because the FIFO allows data to be queued up, and then burst transferred across the host bus. To accommodate software of this type, it is recommended that the FIFO be disabled.

8.2 Drive Polling

The 82078 supports the polling mode of the older generation 8272A. This mode is enabled upon a reset and can be disabled via the CONFIGURE command. This mode is supported for the sole purpose of providing backward compatibility with software that expects it's presence.

The intended purpose of drive polling dates back to 8" drives as a means to monitor any change in status for each disk drive present in the system. Each of the drives is selected for a period of time and its READY signal sampled. After a delay, the next drive is selected. Since the 82078 does not support READY in this capacity (internally tied true), the polling sequence is only simulated and does not affect the drive select lines (DS0–DS3) when it is active. If enabled, it occurs whenever the 82078 is waiting for a command or during SEEKs and RECALIBRATEs (but not IMPLIED SEEKs). Each drive is assumed to be not ready after a reset and a "ready" value for each drive is saved in an internal register as the simulated drive is polled. An interrupt will be generated on the first polling loop because of the initial "not ready" status. This interrupt must be followed with a SENSE INTERRUPT STATUS command from the host to clear the interrupt condition for each of the four logical drives.

9.0 PROGRAMMING GUIDELINES

Programming the 82078 is identical to any other 8272A compatible disk controller with the exception of some additional commands. For the new designer it is useful to provide some guidelines on how to program the 82078. A typical disk operation involves more than issuing a command and waiting for the results. The control of the floppy disk drive is a low level operation that requires software intervention at different stages. New commands and features have been added to the 82078 to reduce the complexity of this software interface.

9.1 Command and Result Phase Handshaking

Before a command or parameter byte can be issued to the 82078, the Main Status Register (MSR) must be interrogated for a ready status and proper FIFO direction. A typical floppy controller device driver should contain a subroutine for sending command or parameter bytes. For this discussion, the routine will be called "Send_byte" with the flowchart shown in Figure 9-1.

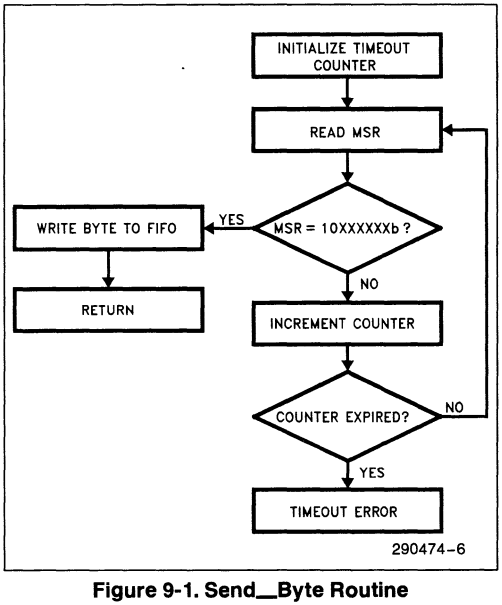


Figure 9-1. Send_Byte Routine

The routine loops until RQM is 1 and DIO is 0 indicating a ready status and FIFO direction is inward. If this condition is true, the 82078 is ready to accept a command or parameter byte. A timeout counter is used to insure software response within a reasonable amount of time in case of no response by the 82078. As a note, the programmer must be careful how the maximum delay is chosen to avoid unnecessary timeouts. For example, if a new command is issued when the 82078 is in the middle of a polling routine, the MSR will not indicate a ready status for the next parameter byte until the polling sequence completes the loop. This could cause a delay between the first and second bytes of up to 250 μs (@ 250 Kbps). If polling is disabled, this maximum delay is 175 μs. There should also be enough timeout margin to accommodate a shift of the software to a higher speed system. A timeout value that results in satisfactory operation on a 16 MHz CPU might fail when the software is moved to a system with a 25 MHz CPU. A recommended solution is to derive the timeout counter from a system hardware counter that is fixed in frequency from CPU clock to CPU clock.

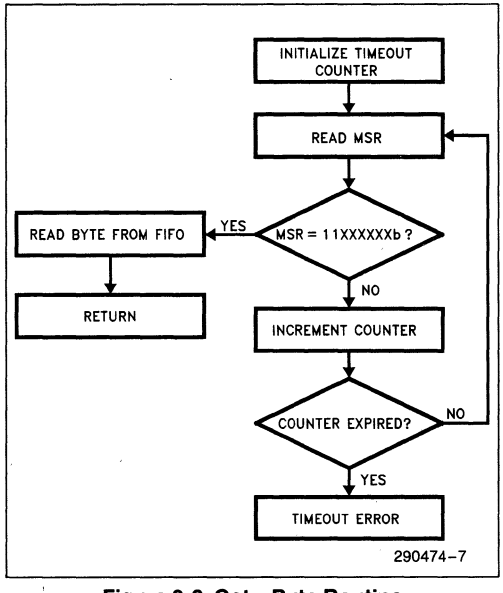


Figure 9-2. Get_Byte Routine

For reading result bytes from the 82078, a similar routine is used. Figure 9-2 illustrates the flowchart for the routine "Get_byte". The MSR is polled until RQM is 1 and DIO is 1, which indicates a ready status and outward FIFO direction. At this point, the host can read a byte from the FIFO. As in the Send_byte routine, a timout counter should be incorporated in case of a disk controller lock-up condition. For example, if a disk was not inserted into the disk drive at the time of a read operation, the controller would fail to receive the index pulse and lockup since the index pulses are required for termination of the execution phase.

9.2 Initialization

Initializing the 82078 involves setting up the appropriate configuration after a reset. Parameters set by the SPECIFY command are undefined after a system reset and will need to be reinitialized. CONFIGURE command parameters default to a known state after a system reset but will need to be reinitialized if the system requirements are different from the default settings. This can be accomplished in two ways; either issue the individual commands, or issue the Restore command (assuming the Save command was issued). The Restore command is a succinct way to initialize the 82078, this is the preferable method if the system power management powers

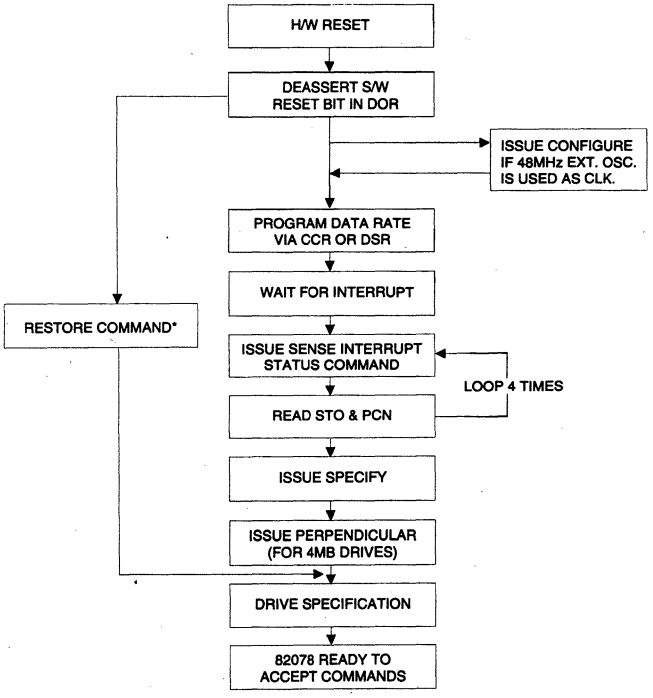
the 82078 on and off frequently. The flowchart for the recommended initialization sequence of the 82078 is shown in Figure 9-3.

Following a reset of the 82078, the Configuration Control Register (CCR) should be reinitialized for the appropriate data rate. An external reset via the RESET pin will cause the data rate and write precompensation values to default to 250 Kbps (10b) and 125 ns (000b) respectively. Since the 125 ns write precompensation value is optimal for the 5¼" and 3½" disk drive environment, most applications will not require the value to be changed in the initialization sequence. As a note, a software reset issued via the DOR or DSR will not affect the data rate or write precompensation values. But it is recommended as a safe programming practice to always program the data rate after a reset, regardless of the type.

Since polling is enabled after a reset of the 82078, four SENSE INTERRUPT STATUS commands need to be issued afterwards to clear the status flags for each drive. The flowchart in Figure 9-3 illustrates how the software clears each of the four interrupt status flags internally queued by the 82078. It should be noted that although four SENSE INTERRUPT STATUS commands are issued, the INT pin is only active until the first SENSE INTERRUPT STATUS command is executed.

As a note, if the CONFIGURE command is issued within 250 μs of the trailing edge of reset (@1 Mbps), the polling mode of the 82078 can be disabled before the polling initiated interrupt occurs. Since polling stops when the 82078 enters the command phase, it is only time critical up to the first byte of the CONFIGURE command. If disabled in time, the system software no longer needs to issue the four SENSE INTERRUPT STATUS commands to clear the internal interrupt flags normally caused by polling.

The CONFIGURE command should also be issued if the system requirements are different from the default settings. For example, the CONFIGURE command can be used to enable the FIFO, set the threshold, and enable Implied Seeks.



NOTE:
(*) A sense interrupt status may be required if the Restore command is not issued within 250 μs of the trailing edge of a H/W reset (@1 Mbps).

Figure 9-3. Initialization Flowchart

The non-DMA mode flag, step rate (SRT), head load (HLT), and head unload times (HUT) programmed by the SPECIFY command do not default to a known state after a reset. This behavior is consistent with the 8272A and has been preserved here for compatibility. Thus, it is necessary to always issue a SPECIFY command in the initialization routine.

9.3 Recalibrates and Seeks

Commands that position the disk head are different from the typical READ/WRITE/FORMAT command in the sense that there is no result phase. Once a RECALIBRATE, SEEK, or RELATIVE SEEK command has been issued, the 82078 will return a ready status in the Main Status Register (MSR) and perform the head positioning operation as a background task. When the seek is complete, the 82078 will assert the INT signal to request service. A SENSE INTERRUPT STATUS command should then be asserted to clear the interrupt and read the status of the operation. Since the drive and motor enable signals are directly controlled through the Digital Output Register (DOR) on the 82078, a write to the DOR will need to precede the RECALIBRATE or SEEK command if the drive and motor is not already enabled. Figure 9-4 shows the flow chart for this operation.

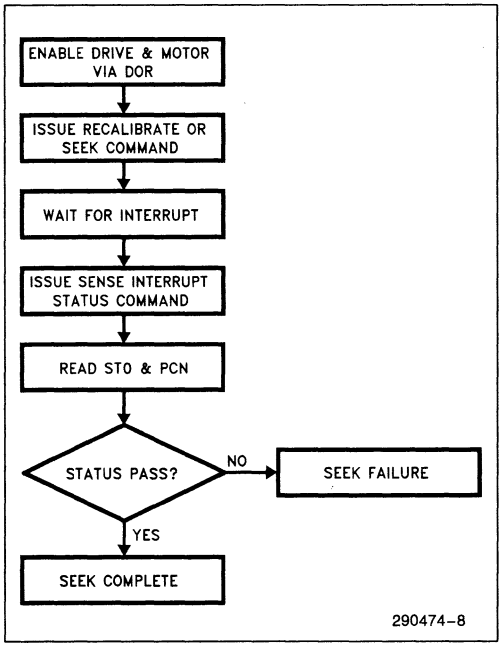


Figure 9-4. Recalibrate and Seek Operations

9.4 Read/Write Data Operations

A read or write data operation requires several steps to complete successfully. The motor needs to be turned on, the head positioned to the correct cylinder, the DMA controller initialized, the read or write command initiated, and an error recovery scheme implemented. The flowchart in Figure 9-5 highlights a recommended algorithm for performing a read or write data operation.

Before data can be transferred to or from the diskette, the disk drive motor must be brought up to speed. For most 3½" disk drives, the spin-up time is 300 ms, while the 5¼" drive usually requires about 500 ms due to the increased moment of inertia associated with the larger diameter diskette.

2

One technique for minimizing the motor spin-up delay in the read data case is to begin the read operation immediately after the motor is turned on. When the motor is not initially up to speed, the internal data separator will fail to lock onto the incoming data stream and report a failure in the status registers. The read operation is then repeated until successful status is obtained. There is no risk of a data integrity problem since the data field is CRC validated. But, it is not recommended to use this technique for the write data operation even though it requires successful reading of the ID field before the write takes place. The data separator performance of the 82078 is such that locking to the data stream could take place while the motor speed variation is still significant. This could result in errors when an attempt is made to read the disk media by other disk controllers that have a narrower incoming data stream frequency bandwidth.

After the motor has been turned on, the matching data rate for the media inserted into the disk drive should then be programmed to the 82078 via the Configuration Control Register (CCR). The 82078 is designed to allow a different data rate to be programmed arbitrarily without disrupting the integrity of the device. In some applications, it is required to automatically determine the recorded data rate of the inserted media. One technique for doing this is to perform a READ ID operation at each available data rate until a successful status is returned in the result phase.

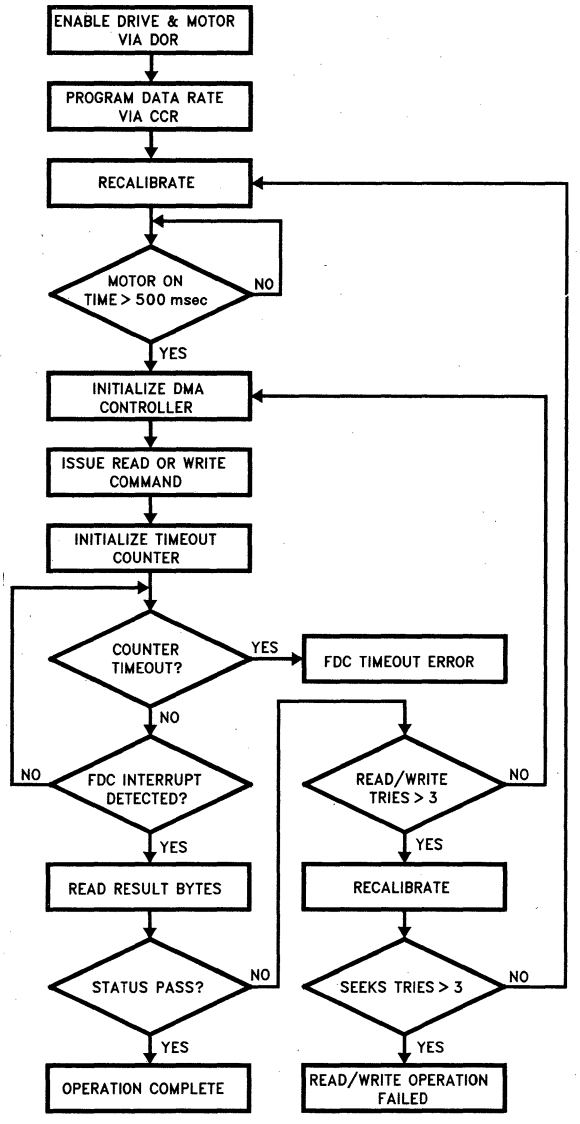


Figure 9-5. Read/Write Operation

If implied seeks are not enabled, the disk drive head must be positioned over the correct cylinder by executing a SEEK command. After the seek is complete, a head settling time needs to be asserted before the read or write operation begins. For most drives, this delay should be a minimum of 15 ms. When using implied seeks, the minimum head settling time can be enforced by the head load time (HLT) parameter designated in the SPECIFY command. For example, a HLT value of 8 will yield an effective head settling time of 16 ms for a programmed data rate of 500 Kbps. Of course if the head is already positioned over the correct cylinder, the head settling time does not need to be enforced.

The DMA controller is then initialized for the data transfer and the read or write command is executed. Typically the DMA controller will assert Terminal Count (TC) when the data transfer is complete. The 82078 will then complete the current data transfer and assert the INT signal signifying it has entered the result phase. The result phase can also be entered by the 82078 if an error is encountered or the last sector number equals the End of Track (EOT) parameter.

Based on the algorithm in Figure 9-5, if an error is encountered after reading the result bytes, two more retries are performed by reinitializing the DMA controller and re-issuing the read or write data command. A persisting failure could indicate the seek operation did not achieve proper alignment between the head and the track. The disk head should then be recalibrated and the seek repeated for a maximum of two more tries. Unsuccessful operation after this point should be reported as a disk failure to the operating system.

9.5 Formatting

The disk formatting procedure involves positioning the head on each track and creating a fixed format field used for organizing the data fields. The flowchart in Figure 9-6 highlights the typical format procedure.

After the motor has been turned on and the correct data rate programmed, the disk head is recalibrated to track 0. The disk is then allowed to come up to speed via a 500 ms delay. It is important the disk speed has stabilized before the actual formatting to avoid any data rate frequency variations. Since the format fields contain critical information used by the data separator of the disk controller for synchronization purposes, frequency stability of the data stream is imperative for media interchangeability among different systems.

The ID field data created on the disk during the format process is provided by the DMA controller during the execution phase. The DMA controller is initialized to send the C, H, R and N values for each sector ID field. For example, to format cylinder 7, on head 1, with 9 sectors, and a sector size of 2 (512 bytes), the DMA controller should be programmed to transfer 36 bytes (9 sectors × 4 bytes per sector) with the following data field: 7,1,1,2, 7,1,2,2, 7,1,3,2, ... 7,1,9,2. Since the values provided to the 82078 during the execution phase of the format command are directly recorded as the ID fields on the disk, the data contents can be arbitrary. Some forms of copy protection have been implemented by taking advantage of this capability.

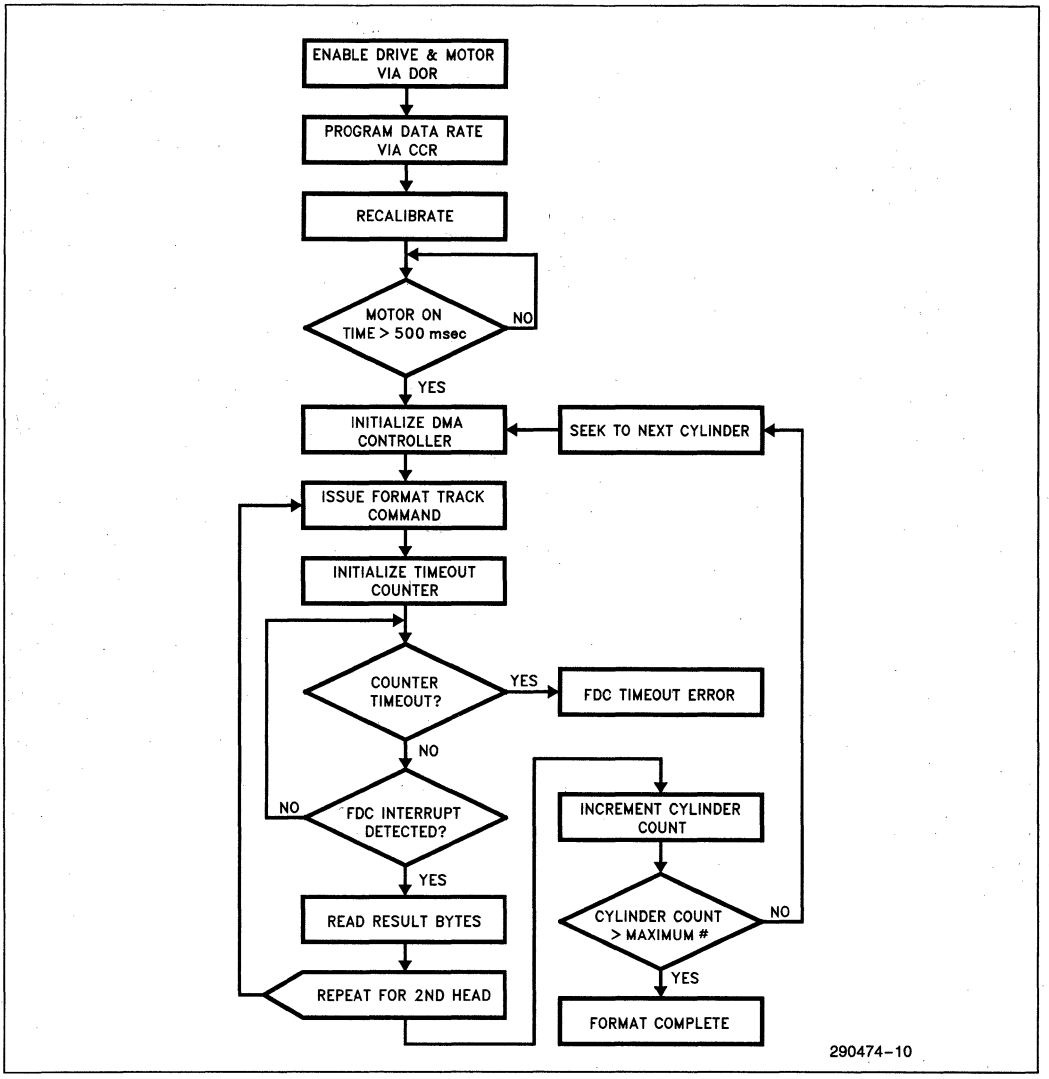


Figure 9-6. Formatting

After each head for a cylinder has been formatted, a seek operation to the next cylinder is performed and the format process is repeated. Since the FORMAT TRACK command does not have implied seek capability, the SEEK command must be used. Also, as discussed in Section 9-2, the head settling time needs to be adhered to after each seek operation.

9.6 Save and Restore

The Save and Restore commands were developed for portable systems that use zero-volt powerdown to conserve power. These systems turn off the V_{CC} to most of the system and retain the system status in a specific location. In older floppy controller designs, in order for system designers to retrieve the floppy controller status, a lot of separate commands and register reads were required. The Save command stores the key status information in a single command, the Restore command restores this information with a single command. These commands can be integrated into the SMM module that is responsible for zero-volt powerdown.

The sequence of initializing the 82078 after a reset occurred and assuming a Save command was issued follows:

- Issue the Drive Spec command (if the design utilizes this command)
- Issue the Restore command

The Restore command programs the data rate and precompensation value via the DSR. It then restores the values normally programmed through the Configure, Specify, and Perpendicular commands. It also enables the previously selected values for the AUTO Powerdown command. The command then restores the PCN values to its previous values. The user is responsible for issuing the seek and recalibrate commands to restore the head to the proper location. There are some drives that do not recalibrate in which case the Restore command will restore the previous state completely. The PDOSC bit is retrievable using the Save command, however it is up to the system designer to set it correctly. The software must allow at least 20μs to execute the Restore command. When using the BOOTSEL bit in the TDR, the user must restore or reinitialize this bit to it's proper value.

9.7 Verifies

In some applications, the sector data needs to be verified immediately after each write operation. One verify technique reinitializes the DMA controller to perform a read transfer or verify transfer (DACK# is asserted but not RD#) immediately after each write operation. Issue a read command to the disk controller and the resulting status indicates if the CRC validated the previously written data. This technique has the drawback of requiring additional software intervention by having to reprogram the DMA controller between each sector write operation. The 82078 supports this verify technique but also provides a VERIFY command that does not require the use of the DMA controller.

To verify a write data transfer or format track operation using the VERIFY command, the software simply issues the command with the same format as a READ DATA command but without the support of the DMA controller. The 82078 will then perform a disk read operation without a host data transfer. The CRC will be calculated for each sector read and compared against the value stored on the disk. When the VERIFY command is complete, the status register reports detected CRC errors.

9.8 Powerdown State and Recovery

The two power management modes coupled with the internal oscillator power management forms an important consideration for programming the 82078. The recovery of 82078 and the time it takes to achieve complete recovery depends on how 82078 is powered down and how it is awakened. The following sections describe all the programming concerns and subtleties involved in using power management features of the 82078. The 3.3V version of the 82078 has the same power saving features as the 5.0V versions.

9.8.1 OSCILLATOR POWER MANAGEMENT

Section 4.1 covers the power management scheme involved in powering down of both an internal and an external oscillator. Both types of oscillators face drop out effects and require recovery times on the order of tens of milliseconds (this may be objectionable to some application software). This means that if the oscillator is powered down then it is imperative for the software to assure enough time for the oscillator to recover to a stable state. Oscillator power management must be controlled by the system software especially to maintain software transparency. In cases where the system goes into a standby mode (by user request or system time-out), the power management software can turn off the oscillator to conserve power. This can also be controlled in hardware using the Powerdown (PD#) pin. Complete recovery from an oscillator powerdown state requires the software to turn on the oscillator sufficiently ahead of awakening the 82078.

9.8.2 PART POWER MANAGEMENT

The part powerdown and wake up modes are covered in Section 4.2 in detail. This section is meant to address the programming concerns for the part (excluding the oscillator) during these modes.

9.8.2.1 Powerdown Modes

For both types of powerdown modes—DSR powerdown and auto powerdown, if reset is used to exit the part from powerdown then the internal microcontroller will go through a standard sequence: register initialization followed after some delay by an interrupt.

Software transparency in auto powerdown mode is preserved by MSR retaining the value of 80H which indicates that the part is ready to receive a command. This feature allows the part to powerdown while maintaining its responsiveness to any application software.

The PD and IDLE status bits can be monitored via the Status Register B (SRB, EREG EN = 1). Since the IDLE# pin stays high when the 82078 is in idle state, the IDLEMSK bit can be used to set the pin low again (as part of a power management routine).

NOTE:
The IDLEMSK prevents the user from knowing if the part has entered auto powerdown or DSR powerdown.

9.8.2.2 Wake Up Modes

Wake up from DSR powerdown results in the part being internally reset and all present status being lost. During DSR powerdown the RQM bit in the MSR is set. A software or hardware reset will wake up the part.

The case for wake up from auto powerdown is different. The BIOS and application software are very sensitive to delays involved in writing the first command bytes to the 82078. Most programs have short error time-outs in these cases. Such programs would not tolerate any floppy disk controller that was unable to receive the first byte of a command at any time. The following describes how 82078 uniquely sustains its software transparency during wake up sequences.

Prior to writing a command to 82078, it is first necessary to read the MSR to ensure that the 82078 is ready (RQM bit must be set) to receive the command. When the part detects a MSR read, it assumes that another command will follow and begins the wake up process. While the part is waking up it does not change the state of the MSR (MSR = 80H) and is able to receive the command in the FIFO. At this point one of the two following scenarios can occur.

No other command is sent subsequent to the MSR read. The part wakes up and initializes the minimum power up timer. Upon the expiration of this timer the part is once again put in powerdown state.

Another command follows the MSR read. If the command is sent during the part's recovery from powerdown, the part remembers the command, clears the RQM bit (to prevent further bytes being written) and acts on the command once it is fully awake.

If the MSR was not checked prior to writing of a command, the part will proceed as stated above with the RQM bit cleared and the command byte held until the internal microcontroller is ready. Writing the motor enable bits in DOR active will initiate the wake up sequence with RQM set high, ready to receive any command.

As it is clear from the above discussion, the immediate access to the floppy disk controller for the first command byte is vital to software transparency. The recovery of the part from powerdown may involve a delay after the first command byte has been issued. However, all programs have tolerance for the delay after the first command byte is issued. In a powered up chip, it is possible for the microcontroller to be in its "polling loop". As a result, the tolerance for this delay provides an excellent window for recovery of the part.

10.0 DESIGN APPLICATIONS

10.1 Operating the 82078-3 in a 3.3V Design

The design for 3.3V is the same as it is for 5.0V, however the floppy drive interface signals can be at either 3.3V or 5.0V levels depending on the voltage on the V_{CCF} pin. The V_{CCF} pin allows the FDD interface to be operated in mixed (3.3V/5.0V) mode. For example, if the system operates at 3.3V and the floppy disk drive operates at 5.0V, the 82078 can be configured to operate at 3.3V with 5.0V available to the drive interface. See Figure 10-1 for a schematic.

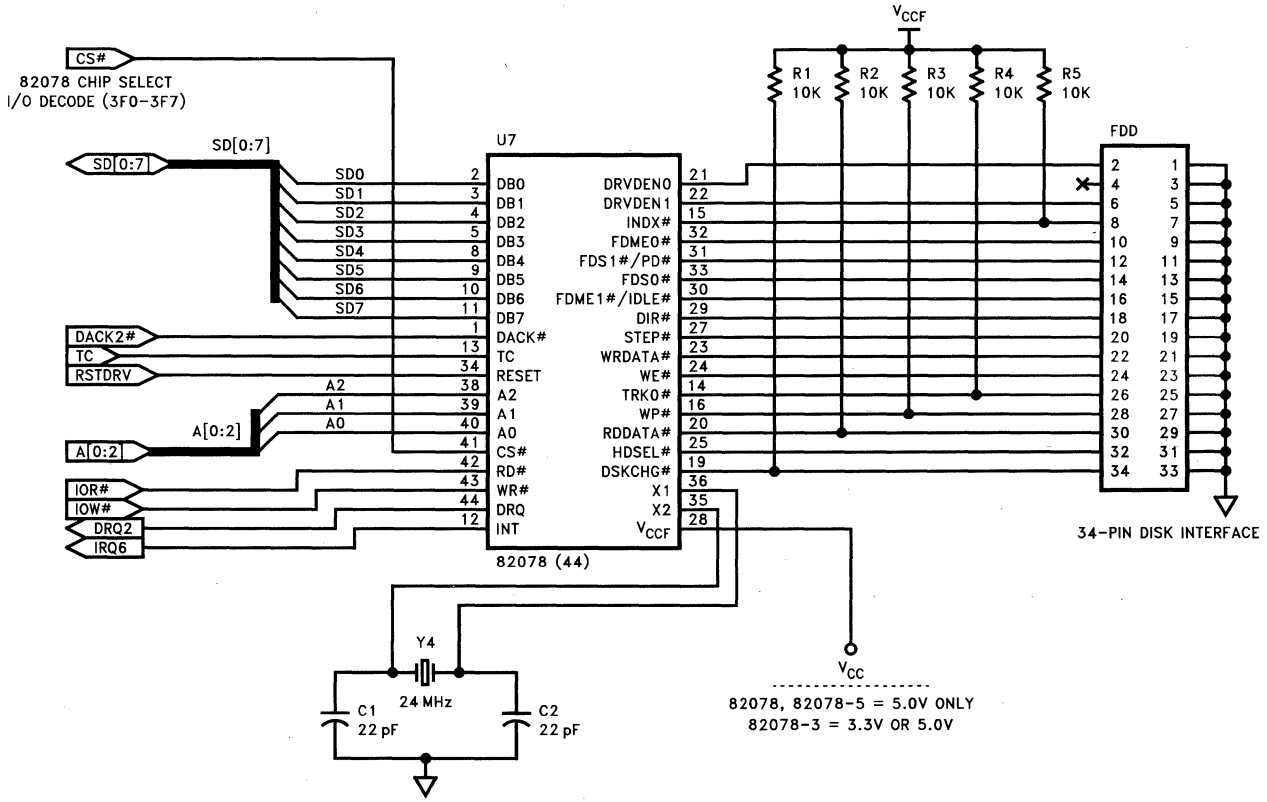


Figure 10-1. 82078 PC/AT Design

10.2 Selectable Boot Drive

Generally a standard personal computer is configured with a 1.2 MB 5.25" disk drive and a 1.44 MB or 2.88 MB 3.5" disk drive. Usually the drive that connects as "A:" is the boot drive. At times the user may want to configure "B:" as the boot drive. Currently some BIOS' use a special implementation in software to accomplish this. The 82078 now offers this capability more efficiently by configuring the boot drives.

The 82078 allows for virtual drive designations. This is a result of multiplexing the boot drive select and motor enable lines, as shown in Figure 10-2.

The DRIVE SEL1 and the DRIVE SEL2 bits in the DOR register decode internally to generate the signals DSn. The MEn signals generate directly from the DOR register. The DSn and MEn signals get mapped to actual FDSn and FDMEn pins based on the BOOTSELn bits (selected in the TDR register). The exact mapping of BOOTSEL vs the FDSn and FDMEn pins is shown in the following table.

44PD EN	BOOTSEL (TDR)	Mapping
0	0	Default → DS0 → FDS0, ME0 → FDME0 DS1 → FDS1, ME1 → FDME1
0	1	DS0 → FDS1, ME0 → FDME1 DS1 → FDS0, ME1 → FDME0
1	X	DS0 → FDS0, ME0 → FDME0 DS1 → PD, ME1 → IDLE

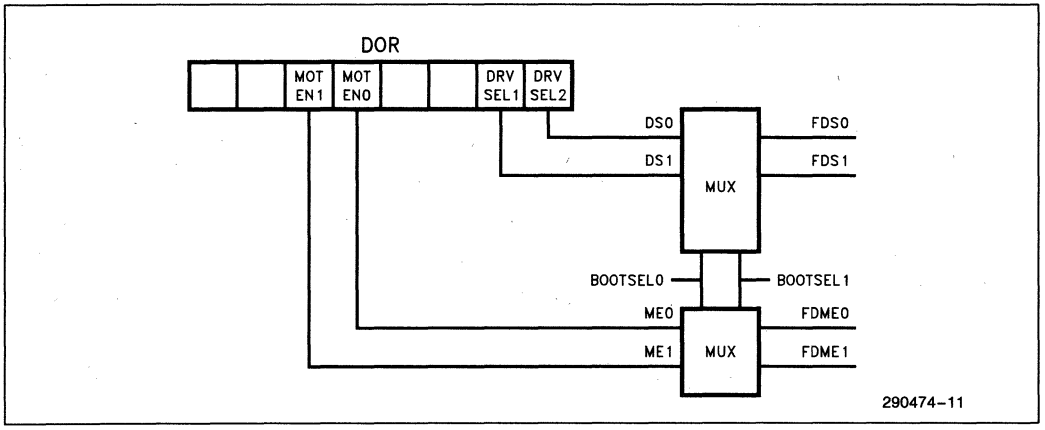


Figure 10-2. Virtual Drive Configuration

The BOOTSEL bit allows users to multiplex the output drive signals allowing different drives to be the boot drive. The DSn and MEn bits are considered virtual designations since the DSn and MEn signals get remapped to different corresponding physical FDSn and FDMEn pins. In other words, once the BOOTSEL bit is configured for a non-default selection, all future references made to the controller will be assumed as virtual designations. Note, due to the virtual designations TAPESEL[1:0] = 00 would never enable tape mode due to boot drive restrictions.

10.3 How to Disable the Native Floppy Contoller on the Motherboard

There are occasions when the floppy controller designed onto the motherboard of a system needs to be disabled in order to operate another floppy controller on the expansion bus. This can be done without changing the BIOS or remapping the address of the floppy controller (provided there is a jumper, or another way to disable the chip select on the native controller).

Upon reset, the DOR register in the 82078 is set to 00H. If the CS# is left enabled during the POST, the DOR is set to 0CH, this enables the DMA GATE# bit in the DOR. When this bit is set, the 82078 treats a DACK# and a RD# or WR# as an internal chip select (CS#). Bus contention will occur between the native controller and the auxiliary controller if the DMA GATE# bit becomes active, even if the CS# signal is not present.

The proper way to disable the native floppy controller is to disable the CS# before the system is turned on. This will prevent the native controller from getting initialized. Another option is to map the native controller to a secondary address space, then disable the DMA GATE# via the DOR disabling the DMA GATE#. This assumes that the native controller is switched to a secondary address space.

10.4 Replacing the 82077SL with a 82078 in a 5.0V Design

The 82078 easily replaces the 5.0V 82077SL with minimum design changes. With a few exceptions, most of the signals are named as they were in the 82077SL. Some pins were eliminated and others renamed to accommodate a reduced pin count and smaller package.

The connections to the AT bus are the same as the 82077SL with the following exceptions: MFM and IDENT have been removed. The PLL0 pin was removed. Tape drive mode on the 82078 must be configured via the Tape Drive Register (TDR).

The Drive Interface on the 82078 is also similar to the 82077SL except as noted: DRVDEN0 and DRVDEN1 on the 82078 take the place of DENSEL, DRATE0, and DRATE1 on the 82077SL. The Drive Specification Command configures the polarity of these pins, thus selecting the density type of the drive. The Motor Enable pins and the Drive Select pins are renamed FDME(0–1) and FDS(0–1) respectively on the 82078. 10K pull-up resistors can be used on the disk interface. See Figure 10-3 for a schematic of the connection.

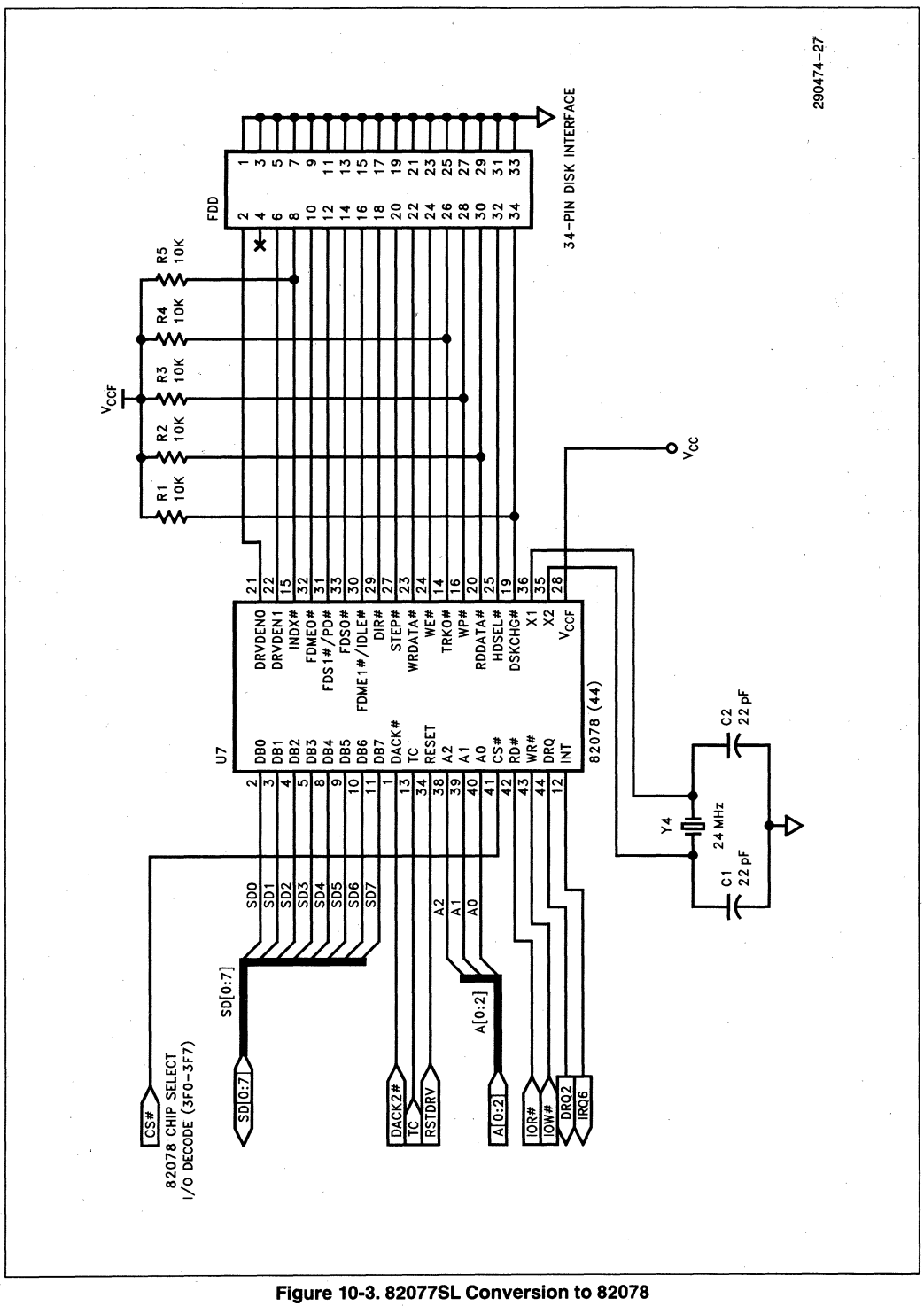


Figure 10-3. 82077SL Conversion to 82078

Pin Changes on the 44 Pin Part:

- If the 44PD EN bit in the powerdown command is set, then the FDS1# and FDME1# no longer function as drive select and motor enable. Instead these pins become functional as status outputs of PD and IDLE.
- INVERT# is removed.
- Four NCs (no connects) are removed.
- MFM, IDENT have been removed. The 44 pin 82078 only operates in AT/EISA mode.
- PLL0 is removed. Hardware configurability for tape drive mode is not supported. Configure tape mode via the TDR register.
- DENSEL, DRATE1, DRATE0 pins have been substituted by DRVDEN0, DRVDEN1. The new pins are configured for each drive via the Drive Specification command.
- DRV2 and RDGATE are not available.
- There are 3 V_{SS} pins, 2 V_{CC} pins, one AV_{SS} and one AV_{CC} pin.

11.0 D.C. SPECIFICATIONS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

11.1 Absolute Maximum Ratings

Storage Temperature ..... −65°C to +150°C
Supply Voltage ..... −0.5 to +8.0V
Voltage on Any Input ..... GND − 2V to 6.5V
Voltage on Any Output . GND − 0.5V to V_{CC} + 0.5V
Power Dissipation 1W

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

11.2 D.C. Characteristics T_A = 0°C to +70°C, V_{SS} = AV_{SS} = 0V

44 PIN D.C. CHARACTERISTICS

Symbol	Parameter	V_{CC} = +5V ±10%			V_{CC} = 3.3V ±0.3V		
		Min (V)	Max (V)	Test Conditions	Min (V)	Max (V)	Test Conditions
V_{ILC}	Input Low Voltage, X1	−0.5	0.8		−0.3	0.8	
V_{IHC}	Input High Voltage, X1	3.9	V_{CC} + 0.5		2.4	V_{CC} + 0.3	
V_{IL}	Input Low Voltage (All Pins except X1)	−0.5	0.8		−0.3	0.8	
V_{IH}	Input High Voltage (All Pins except X1)	2.0	V_{CC} + 0.5		2.0	V_{CC} + 0.3	
V_{OL}	System Interface		0.4	I_{OL} = 12 mA		0.4	I_{OL} = 6 mA
	FDD Interface Outptus		0.4	I_{OL} = 12 mA		0.4	I_{OL} = 6 mA
V_{OH}	All Outputs	3.0		I_{OH} = −4.0 mA	2.4		I_{OH} = −2.0 mA
	All Outputs	V_{CC} − 0.4		I_{OH} = −100 µA	V_{CC} − 0.2		I_{OH} = −100 µA

44 PIN D.C. CHARACTERISTICS I_{CC}

Symbol	Parameter	V_{CC} = +5V ±10%			V_{CC} = +3.3V ±0.3V		
		Typical	Max	Test Condition	Typical	Max	Test Condition
I_{CC1}	1 Mbps Data Rate V_{IL} = V_{SS}, V_{IH} = V_{CC}	15.4 mA	25 mA	(Notes 1, 2)	8.4 mA	16 mA	(Notes 1, 2)
I_{CC2}	1 Mbps Data Rate V_{IL} = 0.45, V_{IH} = 2.4	20.8 mA	30 mA	(Notes 1, 2)	8.6 mA	16 mA	(Notes 1, 2)
I_{CC3}	500 Kbps Data Rate V_{IL} = V_{SS}, V_{IH} = V_{CC}	11.8 mA	20 mA	(Notes 1, 2)	6.2 mA	14 mA	(Notes 1, 2)
I_{CC4}	500 Kbps Data Rate V_{IL} = 0.45, V_{IH} = 2.4	17.6 mA	25 mA	(Notes 1, 2)	6.2 mA	14 mA	(Notes 1, 2)
I_{CCSB}	I_{CC} in Powerdown	0 µA	60 µA	(Notes 3, 4)	0 µA	60 µA	(Notes 3, 4)
I_{IL}	Input Load Current (All Input Pins)		10 µA −10 µA	V_{IN} = V_{CC} V_{IN} = 0V		10 µA −10 µA	V_{IN} = V_{CC} V_{IN} = 0V

44 PIN D.C. CHARACTERISTICS I_{CC} (Continued)

Symbol	Parameter	V_{CC} = +5V ±10%			V_{CC} = +3.3V ±0.3V		
		Typical	Max	Test Condition	Typical	Max	Test Condition
I_{OFL}	Data Bus Output Float Leakage		±10 μA	$0.45 < V_{OUT} < V_{CC}$		±10 μA	$0.45 < V_{OUT} < V_{CC}$

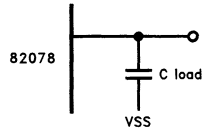
NOTES:
1. Only the data bus inputs may float.
2. Tested while reading a sync field of "00". Outputs not connected to D.C. loads.
3. $V_{IL} = V_{SS}$, $V_{IH} = V_{CC}$; Outputs not connected to D.C. loads.
4. Typical value with the oscillator off.

CAPACITANCE

C_{IN}	Input Capacitance	10	pF	f = 1 MHz, T_A = 25°C
C_{IN1}	Clock Input Capacitance	20	pF	Sampled, Not 100% Tested
$C_{I/O}$	Input/Output Capacitance	20	pF	

NOTE:
All pins except pins under test are tied to A.C. ground.

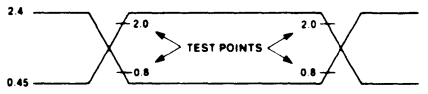
LOAD CIRCUIT



290474-13

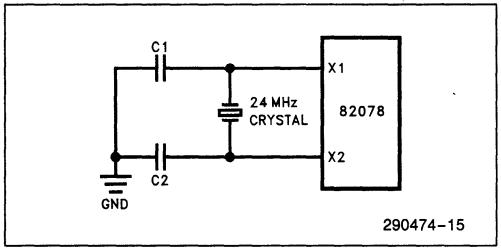
NOTE:
C_{load} = 50 pF for all logic outputs, 100 pF for the data bus.

A.C. TESTING INPUT, OUTPUT WAVEFORM

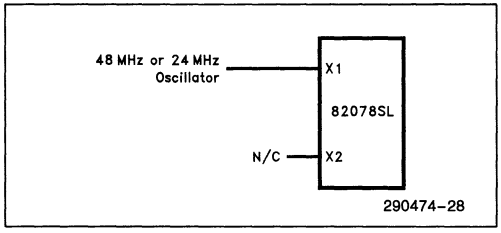


290474-14

11.3 Oscillator



290474-15



290474-28

The 24 MHz clock can be supplied either by a crystal or a MOS level square wave. All internal timings are referenced to this clock or a scaled count which is data rate dependent.

The crystal oscillator must be allowed to run for 10 ms after V_{CC} has reached 4.5V or exiting the POWERDOWN mode to guarantee that it is stable.

Frequency:	24 MHz ±0.1%
Mode:	Parallel Resonant Fundamental Mode
Series Resistance:	Less than 40Ω
Shunt Capacitance:	Less than 5 pF

12.0 A.C. SPECIFICATIONS

T_A = 0°C to +70°C, V_{CC} = +5V ±10%, +3.3V ±0.3V, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit
CLOCK TIMINGS				
t1	Clock Rise Time		10	ns
	Clock Fall Time		10	ns
t2	Clock High Time(7)	16	26	ns
t3	Clock Low Time(7)	16	26	ns
t4	Clock Period	41.66	41.66	ns
t5	Internal Clock Period (3)			
HOST READ CYCLES				
t7	Address Setup to RD#	5		ns
t8	RD# Pulse Width	90		ns
t9	Address Hold from RD#	0		ns
t10	Data Valid from RD#(12)		80	ns
t11	Command Inactive	60		ns
t12	Output Float Delay		35	ns
t13	INT Delay from RD#(16)		t5 + 125	ns
t14	Data Hold from RD#	5		ns
HOST WRITE CYCLES				
t15	Address Setup to WR#	5		ns
t16	WR# Pulse Width	90		ns
t17	Address Hold from WR#	0		ns
t18	Command Inactive	60		ns
t19	Data Setup to WR#	70		ns
t20	Data Hold from WR#	0		ns
t21	INT Delay from WR#(16)		t5 + 125	ns
DMA CYCLES				
t22	DRQ Cycle Period(1)	6.5		µs
t23	DACK# to DRQ Inactive		75	ns
t23a	DRQ to DACK# Inactive	(Note 15)		ns
t24	RD# to DRQ Inactive(4)		100	ns
t25	DACK# Setup to RD#, WR#	5		ns
t26	DACK# Hold from RD#, WR#	0		ns
t27	DRQ to RD#, WR# Active(1)	0	6	µs
t28	Terminal Count Width(10)	50		ns
t29	TC to DRQ Inactive		150	ns

12.0 A.C. SPECIFICATIONS

T_A = 0°C to +70°C, V_{CC} = +5V ±10%, +3.3V ±0.3V, V_{SS} = AV_{SS} = 0V (Continued)

Symbol	Parameter	Min	Max	Unit
RESET				
t30	"Hardware" Reset Width(5)	1.13		µs
t30a	"Software" Reset Width(5)	(Note 11)		ns
t31	Reset to Control Inactive		2	µs
WRITE DATA TIMING				
t32	Data Width(6)			ns
DRIVE CONTROL				
t35	DIR# Setup to STEP#(14)	1.0		µs
t36	DIR# Hold from STEP#	10		µs
t37	STEP# Active Time (High)	2.5		µs
t38	STEP# Cycle Time(2)			µs
t39	INDEX# Pulse Width	5		t5
t41	WE# to HDSEL# Change	(Note 13)		ms
READ DATA TIMING				
t40	Read Data Pulse Width	50		ns
t44	PLL Data Rate	90		ns
	82078		1M	bits/sec
t44	Data Rate Period = 1/f44			
tLOCK	Lockup Time		64	t44

NOTES:

1. This timing is for FIFO threshold = 1. When FIFO threshold is N bytes, the value should be multiplied by N and subtract 1.5 µs. The value shown is for 1 Mbps, scales linearly with data rate.
2. This value can range from 0.5 ms to 8.0 ms and is dependent upon data rate and the Specify command value.
3. Many timings are a function of the selected data rate. The nominal values for the internal clock period (t5) for the various data rates are:

1 Mbps	3 × oscillator period = 125 ns
500 Kbps	6 × oscillator period = 250 ns
300 Kbps	10 × oscillator period = 420 ns
250 Kbps	12 × oscillator period = 500 ns

4. If DACK# transitions before RD#, then this specification is ignored. If there is no transition on DACK#, then this becomes the DRQ inactive delay.

5. Reset requires a stable oscillator to meet the minimum active period.
6. Based on the internal clock period (t5). For various data rates, the Write Data Width minimum values are:

1 Mbps	5 × oscillator period − 50 ns = 150 ns
500 Kbps	10 × oscillator period − 50 ns = 360 ns
300 Kbps	16 × oscillator period − 50 ns = 615 ns
250 Kbps	19 × oscillator period − 50 ns = 740 ns

7. Test points for clock high time are 3.5V. Due to transitional times, clock high time max and clock low time max cannot be met simultaneously. Clock high time min and clock low time max can not be met simultaneously.
8. Based on internal clock period (t5).
9. Jitter tolerance is defined as:

   (Maximum bit shift from nominal position ÷ ¼ period of nominal data rate) × 100%

   is a measure of the allowable bit jitter that may be present and still be correctly detected. The data separator jitter tolerance is measured under dynamic conditions that jitters the bit stream according to a reverse precompensation algorithm.
10. TC width is defined as the time that both TC and DACK# are active. Note that TC and DACK# must overlap at least 50 ns.
11. The minimum reset active period for a software reset is dependent on the data rate, after the 82078 has been properly reset using the t30 spec. The minimum software reset period then becomes:

1 Mbps	3 × t4 = 125 ns
500 Kbps	6 × t4 = 250 ns
300 Kbps	10 × t4 = 420 ns
250 Kbps	12 × t4 = 500 ns

12. Status Register's status bits which are not latched may be updated during a Host read operation.
13. The minimum MFM values for WE to HDSEL change (t41) for the various data rates are:

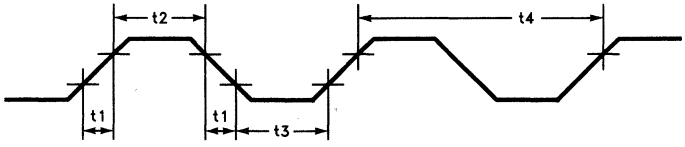
1 Mbps	0.5 ms + [8 × GPL]
500 Kbps	1.0 ms + [16 × GPL]
300 Kbps	1.6 ms + [26.66 × GPL]
250 Kbps	2.0 ms + [32 × GPL]

    GPL is the size of gap3 defined in the sixth byte of a Write Command.
14. This timing is a function of the selected data rate as follows:

1 Mbps	1.0 μs min
500 Kbps	2.0 μs min
300 Kbps	3.3 μs min
250 Kbps	4.0 μs min

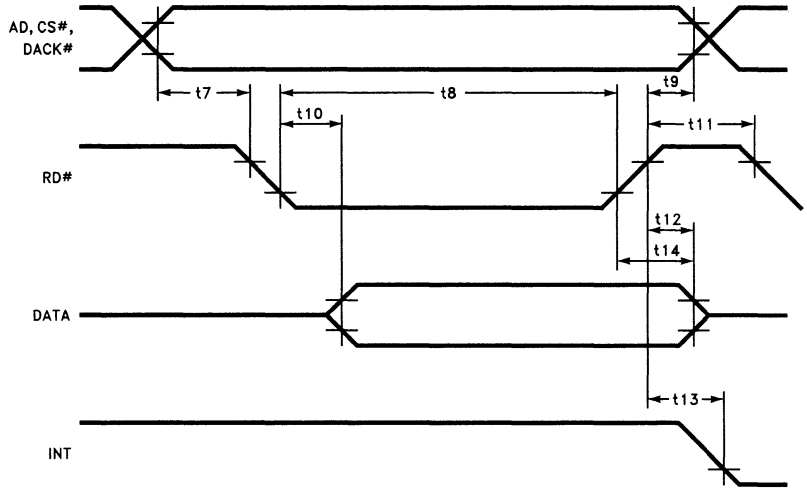
15. This timing is a function of the internal clock period (t5) and is given as (⅔) t5. The values of t5 are shown in Note 3.
16. The timings t13 and t21 are specified for INT signal in the polling mode only. These timings in case of the result phase of the read and write commands are microcode dependent.

Clock Timings



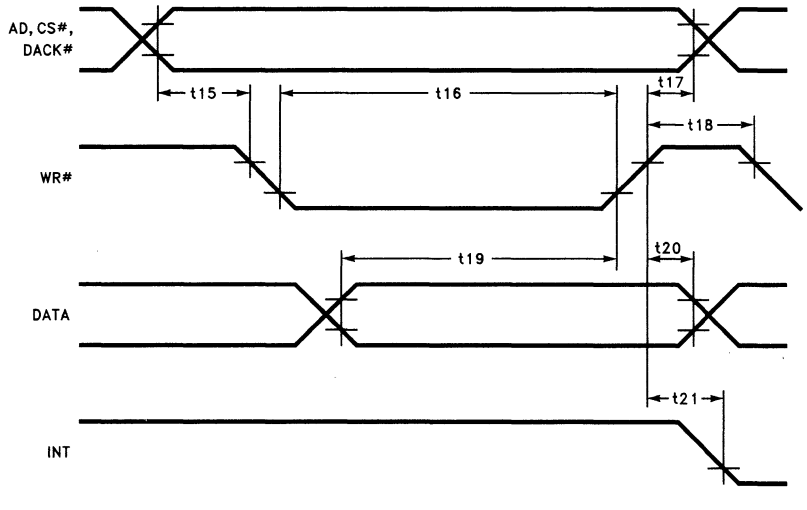
290474-16

Host Read Cycles



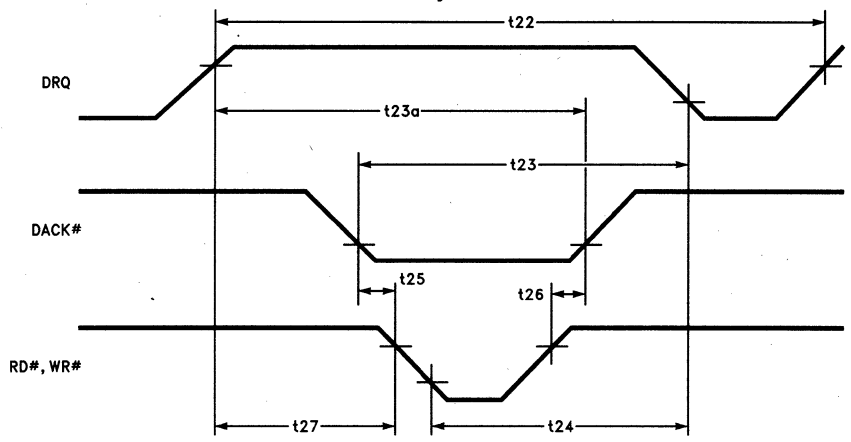
290474-17

Host Write Cycles



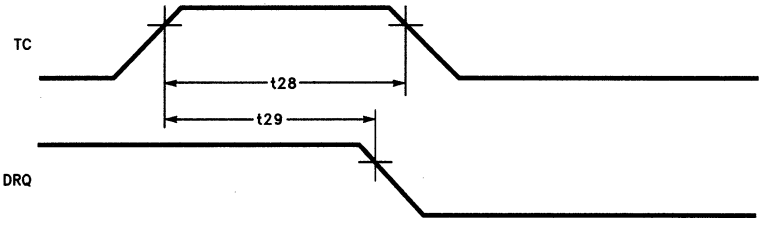
290474-18

DMA Cycles



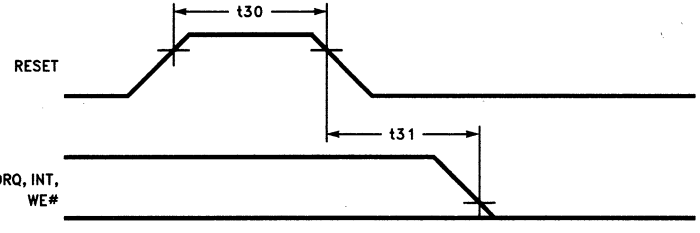
290474-19

Terminal Count



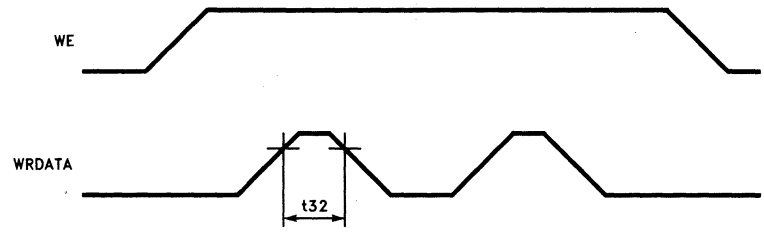
290474-20

RESET



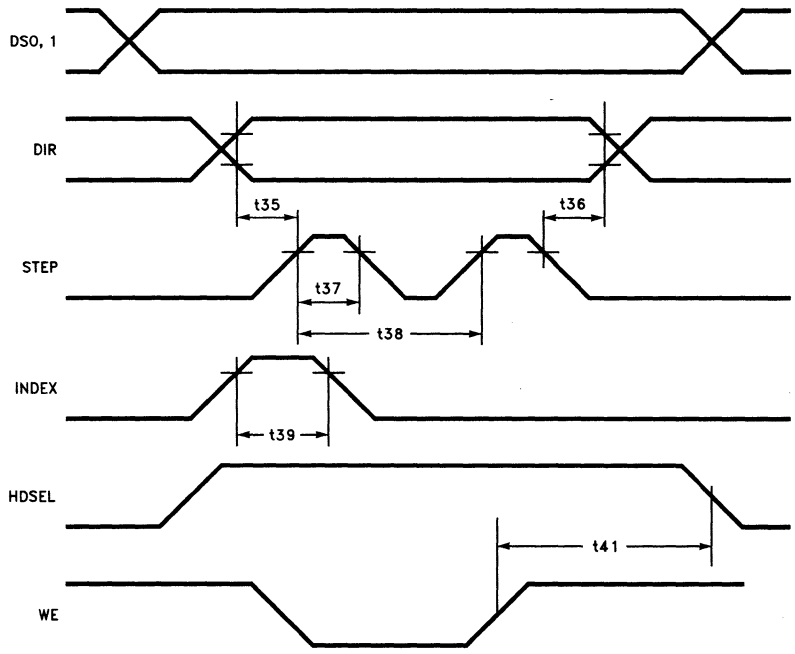
290474-21

Write Data Timing



290474-22

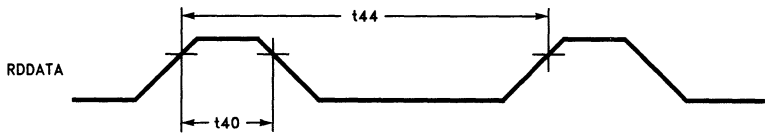
Drive Control



290474-23

NOTE:
For overlapped seeks, only one step pulse per drive section is issued. Non-overlapped seeks will issue all programmed step pulses.

Internal PLL

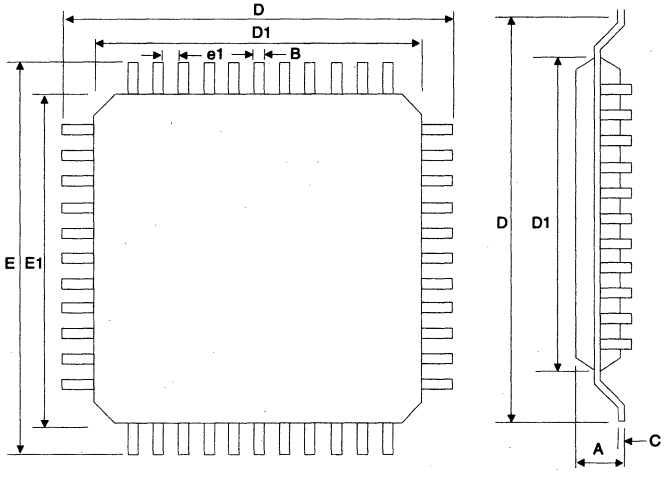


290474-24

12.1 Package Outline for the 44 Pin QFP Part

82078 addresses the current need of the smaller and thinner packages, for the current market. The size of the part is becoming increasingly important in the portable computer market. The QFP part considerably reduces the real estate consumed. The package outline with the appropriate dimensions are given below:

44-Lead Quad Flatpack Package



290474-25

Description	Symbol	44 Pin QFP Package	
		Nominal (mm)	Tolerance (mm)
Overall Height	A	2.10	±0.25
Stand Off	A1	0.35	±0.15
Lead Width	B	0.30	±0.10
Lead Thickness	C	0.15	±0.05
Terminal	D	12.4	±0.40
Long Side	D1	10.0	±0.10
Terminal	E	12.4	±0.40
Short Side	E1	10.0	±0.10
Lead Spacing	e1	0.80	±0.15
Lead Count	N	44	

13.0 REVISION HISTORY FOR THE 82078 44 PIN

The following list represents the key differences between version 002 and version 003 of the 82078 44 pin data sheet.

Section 2.1

Reference to register SRA removed. SRA is not available on the 44 pin 82078.

Section 2.1.2

DRIVE SEL 1 removed from DOR description. This bit is not available on the 44 pin version of the 82078.

Section 4.2

Clarification of PDOSC.

Section 4.4

Reference to register SRA removed. SRA is not available on the 44 pin 82078.

Section 5.2.3

Redundant information removed.

Section 5.2.4

Redundant information removed.

Section 6.3.2

Clarification of command.

Table 1.0

Reference to register SRA removed. SRA is not available on the 44 pin 82078.

Table 2-2 and Table 2-3

Table headings swapped to proper tables.

82078 64 PIN
CHMOS SINGLE-CHIP FLOPPY DISK CONTROLLER

- **Small Footprint and Low Height Packages**
- **Supports Standard 5.0V as well as Low Voltage 3.3V Platforms**
  - **— Selectable 3.3V and 5.0V Configuration**
  - **— 5.0V Tolerant Drive Interface**
- **Enhanced Power Management**
  - **— Application Software Transparency**
  - **— Programmable Powerdown Command**
  - **— Save and Restore Commands for Zero-Volt Powerdown**
  - **— Auto Powerdown and Wakeup Modes**
  - **— Two External Power Management Pins**
  - **— Consumes no Power when in Powerdown**
- **Integrated Analog Data Separator**
  - **— 250 Kbps**
  - **— 300 Kbps**
  - **— 500 Kbps**
  - **— 1 Mbps**
  - **— 2 Mbps**
- **Programmable Internal Oscillator**
- **Floppy Drive Support Features**
  - **— Drive Specification Command**
  - **— Media ID Capability Provides Media Recognition**
  - **— Drive ID Capability Allows the User to Recognize the Type of Drive**
  - **— Selectable Boot Drive**
  - **— Standard IBM and ISO Format Features**
  - **— Format with Write Command for High Performance in Mass Floppy Duplication**
- **Integrated Tape Drive Support**
  - **— Standard 1 Mbps/500 Kbps/ 250 Kbps Tape Drives**
  - **— New 2 Mbps Tape Drive Mode**
- **Perpendicular Recording Support for 4 MB Drives**
- **Integrated Host/Disk Interface Drivers**
- **Fully Decoded Drive Select and Motor Signals**
- **Programmable Write Precompensation Delays**
- **Addresses 256 Tracks Directly, Supports Unlimited Tracks**
- **16 Byte FIFO**
- **Single-Chip Floppy Disk Controller Solution for Portables and Desktops**
  - **— 100% PC AT* Compatible**
  - **— 100% PS/2* Compatible**
  - **— 100% PS/2 Model 30 Compatible**
  - **— Fully Compatible with Intel386™ SL Microprocessor SuperSet**
- **Integrated Drive and Data Bus Buffers**
- **Available in 64 Pin QFP Package**

The 82078, a 24 MHz crystal, a resistor package, and a device chip select implements a complete solution. All programmable options default to 82078 compatible values. The dual PLL data separator has better performance than most board level/discrete PLL implementations. The FIFO allows better system performance in multi-master (e.g., Microchannel, EISA).

The 82078 maintains complete software compatibility with the 82077SL/82077AA/8272A floppy disk controllers. It contains programmable power management features while integrating all of the logic required for floppy disk control. The power management features are transparent to any application software. There are two versions of 82078 floppy disk controllers, the 82078SL and 82078-1.

The 82078 is fabricated with Intel's advanced CHMOS III technology and is also available in a 44-lead QFP package.

*Other brands and names are the property of their respective owner.

November 1994
Order Number: 290475-004

82078 64 Pin CHMOS Single-Chip Floppy Disk Controller

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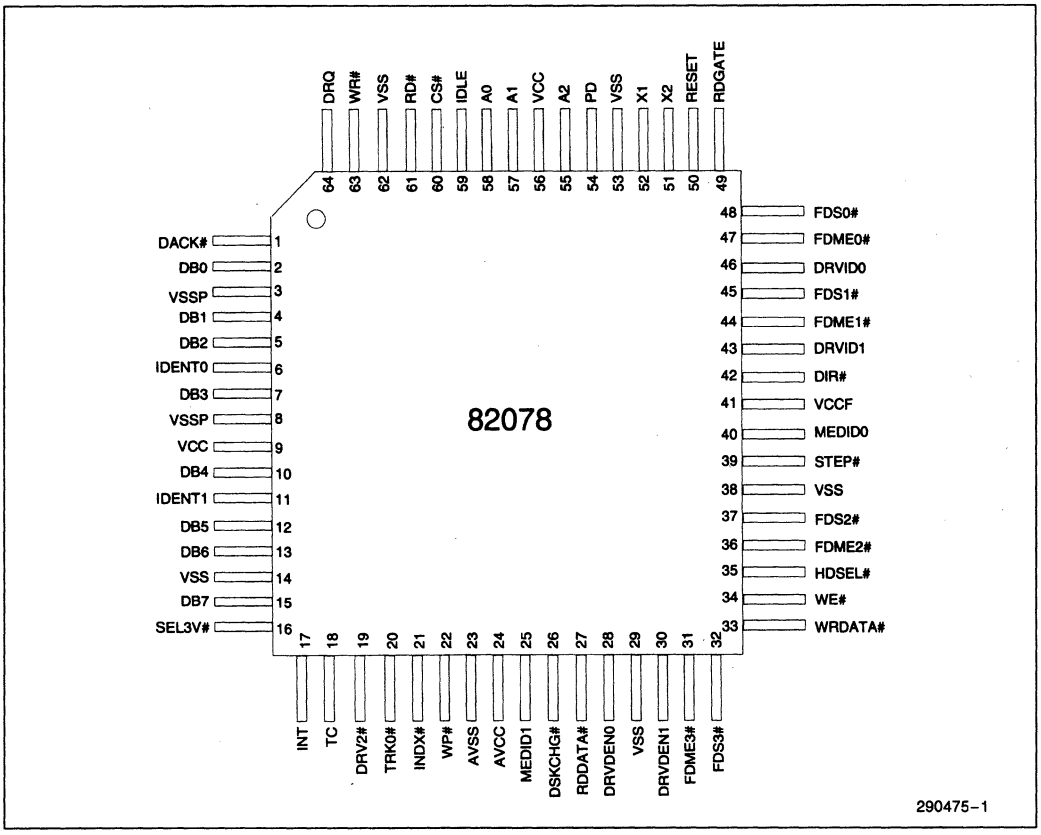

Figure 1-0. 82078 Pinout

Table 1-0. 82078 (64 Pin) Description

Symbol	Pin #	I/O	@ H/W Reset	Description
HOST INTERFACE				
RESET	50	I	N/A	**RESET:** A high level places the 82078 in a known idle state. All registers are cleared except those set by the Specify command.
A0 A1 A2	58 57 55	I	N/A	**ADDRESS:** Selects one of the host interface registers: **A2 A1 A0 Access Register** 0 0 0 R Status Register A SRA 0 0 1 R/W Status Register B SRB 0 1 0 R/W Digital Output Register DOR 0 1 1 R/W Tape Drive Register TDR 1 0 0 R Main Status Register MSR 1 0 0 W Data Rate Select Register DSR 1 0 1 R/W Data Register (FIFO) FIFO 1 1 0 Reserved 1 1 1 R Digital Input Register DIR 1 1 1 W Configuration Control Register CCR
CS#	60	I	N/A	**CHIP SELECT:** Decodes the base address range and qualifies RD# and WR#.

Table 1-0. 82078 (64 Pin) Description (Continued)

Symbol	Pin #	I/O	@ H/W Reset	Description
HOST INTERFACE (Continued)				
RD#	61	I	N/A	**READ:** Read control signal for data transfers from the floppy drive to the system.
WR#	63	I	N/A	**WRITE:** Write control signal for data transfers to the floppy drive from the system.
DRQ	64	O		**DMA REQUEST:** Requests service from a DMA controller. Normally active high, but will go to high impedance in AT and Model 30 modes when the appropriate bit is set in the DOR.
DACK#	1	I	N/A	**DMA ACKNOWLEDGE:** Control input that qualifies the RD#, WR# inputs in DMA cycles. Normally active low, but is disabled in AT and Model 30 modes when the appropriate bit is set in the DOR.
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	2 4 5 7 10 12 13 15	I/O		**DATA BUS:** 12 mA data bus.
IDENT0 IDENT1	6 11	I	N/A	**IDENTITY:** These inputs decode between the several operation modes available to the user. These pins have no effect on the DRVDEN pins. **IDENT0 IDENT1 INTERFACE** 1 1 AT mode 1 0 ILLEGAL 0 1 PS/2 mode 0 0 Model 30 **AT MODE:** Major options are: enables DMA gate logic, TC is active high, Status Register B is available based on a bit the powerdown command. **PS/2 MODE:** Major options are: no DMA gate logic, TC is active low, Status Registers A & B are available. **MODEL 30 MODE:** Major options are: enable DMA gate logic, TC is active high, Status Registers A & B are available.
INT	17	O		**INTERRUPT:** Signals a data transfer in non-DMA mode and when status is valid. Normally active high, but goes to high impedance when the appropriate bit is set in the DOR.
TC	18	I	N/A	**TERMINAL COUNT:** Control line from a DMA controller that terminates the current disk transfer. TC is effective only when qualified by DACK#. This input is active high in the AT, and Model 30 modes when the appropriate bit is set in the DOR.
X1 X2	52 51		N/A	**EXTERNAL CLOCK OR CRYSTAL:** Connection for a 24 MHz fundamental mode parallel resonant crystal. X1 can also be driven by an external clock (external oscillator) which can be either at 48 MHz or 24 MHz. If external oscillator is used then the PDOSC bit can be set to turn off the internal oscillator. Also, if a 48 MHz exernal oscillator is used then the CLK48 bit must be set in the enhanced CONFIGURE command.

Table 1-0. 82078 (64 Pin) Description (Continued)

Symbol	Pin #	I/O	@ H/W Reset	Description
POWER MANAGEMENT				
SEL3V#	16	I	N/A	**SELECT 3.3V:** This is a control pin that is used to select between 3.3V operation and 5.0V operation. This is an active low signal and selects 3.3V mode of operation when tied to ground.
PD	54	O		**POWERDOWN:** This pin is active high whenever the part is in powerdown state, either via DSR POWERDOWN bit or via the Auto Powerdown Mode. This pin can be used to disable an external oscillator's output.
IDLE	59	O		**IDLE:** This pin indicates that the part is in the IDLE state and can be powered down. IDLE state is defined as MSR = 80H, INT = 0, and the head being "unloaded" (as defined in Section 4.0, Power Management Features). Whenever the part is in this state, IDLE pin is active high. If the part is powered down by the Auto Powerdown Mode, IDLE pin is set high and if the part is powered down by setting the DSR POWERDOWN bit, IDLE pin is set low.
PLL SECTION				
RDDATA#	27	I	N/A	**READ DATA:** Serial data from the floppy disk.
RDGATE	49	O		**READ GATE:** This signal is basically used for diagnostic purposes.
DISK CONTROL				
DRV2#	19	I	N/A	**DRIVE2:** This is an active low signal that indicates whether a second drive is installed and is reflected in SRA.
TRK0#	20	I	N/A	**TRACK0:** This is an active low signal that indicates that the head is on track 0.
INDX#	21	I	N/A	**INDEX:** This is an active low signal that indicates the beginning of the track.
WP#	22	I	N/A	**WRITE PROTECT:** This is an active low signal that indicates whether the floppy disk in the drive is write protected.
MEDID1 MEDID0	25 40	I	N/A	**MEDIA ID:** These are active high signals that are output from the drive to indicate the density type of the media installed in the floppy drive. These should be tied low if not being used.
DSKCHG#	26	I	N/A	**DISK CHANGE:** This is an input from the floppy drive reflected in the DIR.
DRVDEN0 DRVDEN1	28 30	O		**DRIVE DENSITY:** These signals are used by the floppy drive to configure the drive for the appropriate media.
FDME3# FDME2# FDME1# FDME0#	31 36 44 47	O		**FLOPPY DRIVE MOTOR ENABLE:** Decoded motor enables for drives 0 to 3. The motor enable pins are directly controlled via the DOR and are a function of the mapping based on BOOTSEL bits in the TDR.
FDS3# FDS2# FDS1# FDS0#	32 37 45 48	O		**FLOPPY DRIVE SELECT:** Decoded floppy drive selects for drives 0 to 3. These outputs are decoded from the select bits in the DOR and are a function of the mapping based on BOOTSEL bits in the TDR.
WRDATA#	33	O		**WRITE DATA:** MFM serial data to the drive. Precompensation value is selectable through software.

Table 1-0. 82078 (64 Pin) Description (Continued)

Symbol	Pin #	I/O	@ H/W Reset	Description
DISK CONTROL (Continued)				
WE#	34	O		**WRITE ENABLE:** Floppy drive control signal that enables the head to write onto the floppy disk.
HDSEL#	35	O		**HEAD SELECT:** Selects which side of the floppy disk is to be used for the corresponding data transfer. It is active low and an active level selects head 1, otherwise it defaults to head 0.
STEP#	39	O		**STEP:** Supplies step pulses to the floppy drive to move the head between tracks.
DIR#	42	O		**DIRECTION:** It is an active low signal which controls the direction the head moves when a step signal is present. The head moves inwards towards the center if this signal is active.
DRVID0 DRVID1	46 43	I	N/A	**DRIVE ID:** These signals are input from the floppy drive and indicate the type of drive being used. These should be tied low if not being used.
POWER AND GROUND SIGNALS				
V_{CCF}	41		N/A	**VOLTAGE:** +5V for 5V floppy drive and 3.3V for 3.3V floppy drive.*
V_{CC}	9 56		N/A	**VOLTAGE:** +5V or 3.3V
V_{SSP}	3 8		N/A	**GROUND:** 0V
V_{SS}	14 29 38 53 62		N/A	**GROUND:** 0V
AV_{CC}	24		N/A	**ANALOG VOLTAGE**
AV_{SS}	23		N/A	**ANALOG GROUND**

***NOTE:**
The digital power supply V_{CC} and the analog power supply AV_{CC} should either be the same or regulated to be within 0.1V of either.

1.0 INTRODUCTION

The 82078, a 24 MHz (or 48 MHz) oscillator, a resistor package and a chip select implement a complete design. The power management features of the 82078 are transparent to application software, the 82078 seems awake to the software even in power-down mode. All drive control signals are fully decoded and have 24 mA (12 mA @ 3.3V) drive buffers. Signals returned from the drive are sent through on-chip input buffers with hysteresis for noise immunity. The integrated analog data separator needs no external compensation of components, yet allows for wide motor variation with exceptionally low soft error rates. The microprocessor interface has 12 mA drive buffers on the data bus plus 100% hardware register compatibility for PC-AT and Microchannel systems. The 16-byte FIFO with programmable thresholds is extremely useful in multi-master systems (Micro-Channel, EISA) or systems with large bus latency.

The 82078 features:

- 3.3V operation
- Small QFP package
- 2 Mbps data rate for tape drives
- Register enhancements from the 82077SL

Several pin changes accommodate the reduced pin count (from the 68 pin 82077SL) and the added features. Functional compatibility refers to software transparency between 82077SL/AA and the 82078. The 64 pin part will implement a superset of the features required to support all platforms, but is not pin to pin compatible to the 82077SL.

The 82078SL is capable of operating at both 3.3V and 5.0V. The 82078-1 only operates at 5.0V but has an available 2 Mbps tape drive data rate. All other features are available on both parts.

Part Specification	3.3V	5.0V	2 Mbps Data Rate
82078SL	X	X	
82078-1		X	X

Figure 1-1 is a block diagram of the 82078.

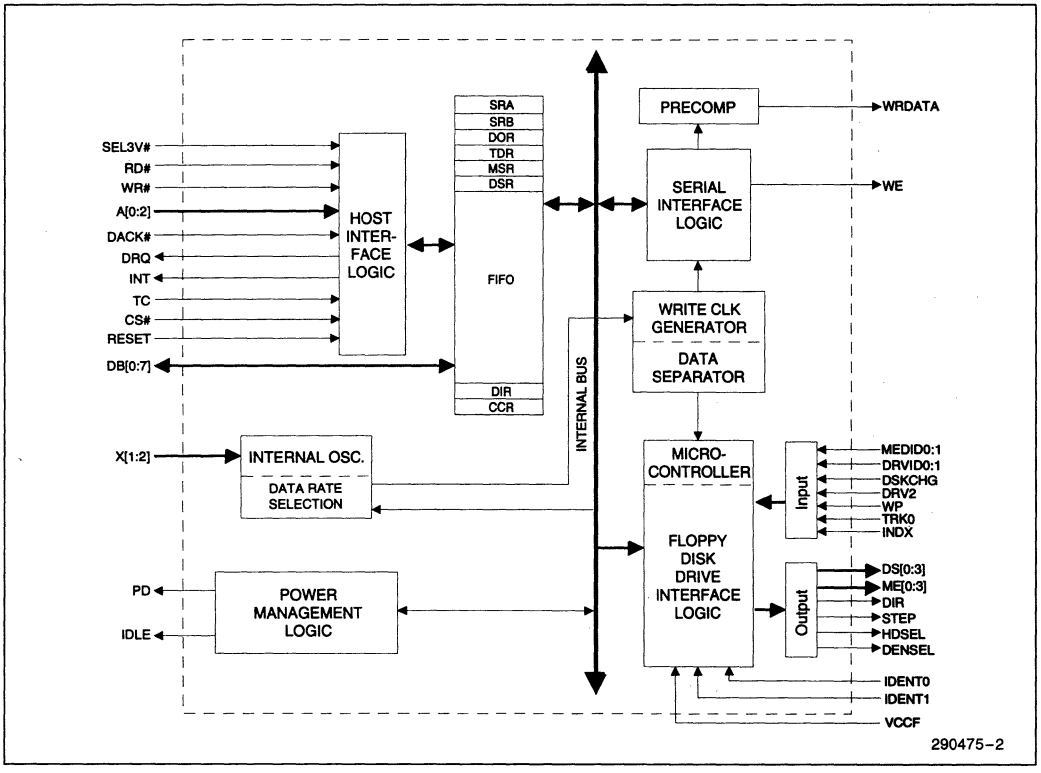

Figure 1-1. 82078 Block Diagram

2.0 MICROPROCESSOR INTERFACE

The interface consists of the standard asynchronous signals: RD#, WR#, CS#, A0–A2, INT, DMA control and a data bus. The address lines select between configuration registers, the FIFO and control/status registers. This interface can be switched between PC AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC-AT.

2.1 Status, Data and Control Registers

As shown below, the base address range is supplied via the CS# pin. For PC-AT or PS/2 designs, the primary and secondary address ranges are 3F0 Hex to 3F7 Hex and 370 Hex to 377 Hex respectively.

A2	A1	A0	Access Type	Register	
0	0	0	R	Status Register A	SRA
0	0	1	R/W	Status Register B	SRB
0	1	0	R/W	Digital Output Register	DOR
0	1	1	R/W	Tape Drive Register	TDR
1	0	0	R	Main Status Register	MSR
1	0	0	W	Data Rate Select Register	DSR
1	0	1	R/W	Data (First In First Out)	FIFO
1	1	0		Reserved	
1	1	1	R	Digital Input Register	DIR
1	1	1	W	Configuration Control Register	CCR

In the following sections, the various registers are shown in their powerdown state. The "UC" notation stands for a value that is returned without change from the active mode. The notation "*" means that the value is reflecting the required status (for powerdown). "n/a" means not applicable. "X" indicates that the value is undefined.

2.1.1 STATUS REGISTER A (SRA, PS/2 MODE)

This register is read-only and monitors the state of the interrupt pin and several disk interface pins. This register is part of the register set, and is not accessible in PC-AT mode.

This register can be accessed during powerdown state without waking up the 82078 from its powerdown state.

Bits	7	6	5	4	3	2	1	0
Function	INT PENDING	DRV2#	STEP	TRK0#	HDSEL	INDX#	WP#	DIR
H/W Reset State	0	DRV2#	0	TRK0#	0	INDX#	WP#	0
Auto PD State	0*	UC	0*	1	0*	1	1	0*

The INT PENDING bit is used by software to monitor the state of the 82078 INTERRUPT pin. By definition, the INT PENDING bit is low in powerdown state. The bits reflecting the floppy disk drive input pins (TRK0, INDEX, and WP) are forced inactive. Floppy disk drive outputs (HDSEL, STEP, and DIR) also go to their inactive, default state.

As a read-only register, there is no default value associated with a reset other than some drive bits will change with a reset. The INT PENDING, STEP, HDSEL, and DIR bits will be low after reset.

2.1.2 STATUS REGISTER A (SRA, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	INT PENDING	DRQ	STEP F/F	TRK0	HDSEL#	INDX#	WP	DIR#
H/W Reset State	0	0	0	TRK0	1	INDX#	WP	1
Auto PD State	0*	0*	0	0	1*	0	0	1*

This register has the following changes in PS/2 Model 30 Mode. Disk interface pins (Bits 0, 1, 2, 3, and 4) are inverted from PS/2 Mode. The DRQ bit monitors the status of the DMA Request pin. The STEP bit is latched with the Step output going active and is cleared with a read to the DIR register, Hardware or Software RESET.

The DRQ bit is low by definition for 82078 to be in powerdown. The bits reflecting the floppy disk drive input pins (TRK0, INDEX, and WP) are forced to reflect an inactive state. The floppy disk drive outputs (HDSEL, STEP, and DIR) also go to their inactive, default state.

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2.1.3 STATUS REGISTER B (SRB, ENHANCED AT/EISA)

In the AT/EISA mode the SRB is made available whenever the EREG EN bit in the auto powerdown command is set. The register functionality is defined as follows (bits 7 through 3 are reserved):

PD and IDLE reflect the values on the corresponding pins. The signal on the IDLE pin can be masked by setting IDLEMSK bit high in this register. The IDLE bit will remain unaffected. Since some systems will use the IDLE pin to provide interrupt to the SMM power management, its disabling allows less external interrupt logic and reduction in board space. Only hardware reset will clear the IDLEMSK bit to zero.

When the IDLEMSK bit is set, the user cannot distinguish between auto powerdown and DSR powerdown (i.e., by using the IDLE pin).

IDLEMSK	IDLE (pin)
0	unmasked
1	masked

SRB								
Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R	RSVD	RSVD	RSVD	RSVD	RSVD	IDLEMSK	PD	IDLE
H/W Reset	X	X	X	X	X	0	PD	IDLE
Auto PD	X	X	X	X	X	UC	UC	UC
W	0	0	0	0	0	IDLEMSK	RSVD	RSVD
H/W Reset	n/a	n/a	n/a	n/a	n/a	0	n/a	n/a
Auto PD	n/a	n/a	n/a	n/a	n/a	UC	n/a	n/a

2.1.4 STATUS REGISTER B (SRB, PS/2 MODE)

Bits	7	6	5	4	3	2	1	0
Function	1	1	DRIVE SEL 0	WRDATA TOGGLE	RDDATA TOGGLE	WE	MOT EN1	MOT EN2
H/W Reset State	1	1	0	0	0	0	0	0
Auto PD State	1	1	UC	0	0	0*	0	0

As the only drive input, RDATA TOGGLE's activity reflects the level as seen on the cable.

The two TOGGLE bits do not read back the state of their respective pins directly. Instead, the pins drive a Flip/Flop which produces a wider and more reliable read pulse. Bits 6 and 7 are undefined and always return to a 1.

After any reset, the activity on the TOGGLE pin is cleared. Drive select and Motor bits cleared by the RESET pin and not software resets.

2.1.5 STATUS REGISTER B (SRB, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	DRV2#	DS1#	DS0#	WRDATA F/F	RDDATA F/F	WE F/F	DS3#	DS2#
H/W Reset State	DRV2#	1	1	0	0	0	1	1
Auto PD State	UC	UC	UC	0	0	0*	UC	UC

This register has the following changes in Model 30 Mode. Bits 0, 1, 5, and 6 return the decoded value of the Drive Select bits in the DOR register. Bits 2, 3, and 4 are set by their respective active going edges and are cleared by reading the DIR register. The WRDATA bit is triggered by raw WRDATA signals and is not gated by WE. Bits 2, 3, and 4 are cleared to low level by either Hardware or Software RESET.

2.1.6 DIGITAL OUTPUT REGISTER (DOR)

The Digital Output Register contains the drive select and motor enable bits, a reset bit and a DMA GATE# bit.

Bits	7	6	5	4	3	2	1	0
Function	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMA GATE#	RESET#	DRIVE SEL1	DRIVE SEL2
H/W Reset State	0	0	0	0	0	0	0	0
Auto PD State	0*	0*	0*	0*	UC	1*	UC	UC

The MOT ENx bits directly control their respective motor enable pins (FDME0–3). The DRIVE SELx bits are decoded to provide four drive select lines and only one may be active at a time. Standard programming practice is to set both MOT ENx and DRIVE SELx bits at the same time.

Table 2-1 lists a set of DOR values to activate the drive select and motor enable for each drive.

Table 2-1. Drive Activation Value

Drive	DOR Value
0	1CH
1	2DH
2	4EH
3	8FH

The DMAGATE# bit is enabled only in PC-AT and Model 30 Modes. If DMAGATE# is set low, the INT and DRQ outputs are tri-stated and the DACK# and TC inputs are disabled. DMAGATE# set high will enable INT, DRQ, TC, and DACK# to the system. In PS/2 Mode DMAGATE# has no effect upon INT, DRQ, TC, or DACK# pins, they are always active.

The DOR reset bit and the Motor Enable bits have to be inactive when the 82078 is in powerdown. The DMAGATE# and DRIVE SEL bits are unchanged. During powerdown, writing to the DOR does not awaken the 82078 with the exception of activating any of the motor enable bits. Setting the motor enable bits active (high) will wake up the part.

This RESET# bit clears the basic core of the 82078 and the FIFO circuits when the LOCK bit is set to "0" (see Section 5.3.2 for LOCK bit definitions). Once set, it remains set until the user clears this bit. This bit is set by a chip reset and the 82078 is held in a reset state until the user clears this bit. The RESET# bit has no effect upon the register.

2.1.7 TAPE DRIVE REGISTER (TDR AT/EISA, PS/2, MODEL 30)

Bits	7	6	5	4	3	2	1	0
Function	—	—	—	—	—	—	TAPE SEL1	TAPE SEL0
H/W Reset State	—	—	—	—	—	—	0	0
Auto PD State	—	—	—	—	—	—	UC	UC

(—) means these bits are not writable and remain tri-stated if read.

This register allows the user to assign tape support to a particular drive during initialization. Any future references to that drive number automatically invokes tape support. Hardware reset clears this register; software resets have no effect. By default, the tape select bits are hardware RESET to zeros, making Drive 0 not available for tape support.

2.1.8 ENHANCED TAPE DRIVE REGISTER (TDR, AT, PS/2, MODEL 30, EREG EN = 1)

In the PS/2 and Model 30 mode and AT/EISA mode the extended TDR is made available only when the EREG EN bit is set, otherwise the bits are tri-stated. The register functionality is defined as follows:

TDR								
Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R	MEDID1	MEDID0	DRVID1	DRVID0	BOOTSEL1	BOOTSEL0	TAPESEL1	TAPESEL0
H/W Reset	MEDID1	MEDID0	DRVID1	DRVID0	0	0	0	0
Auto PD	UC	UC	UC	UC	UC	UC	UC	UC
W	0	0	0	0	BOOTSEL1	BOOTSEL0	TAPESEL1	TAPESEL0
H/W Reset	n/a	n/a	n/a	n/a	0	0	0	0
Auto PD	n/a	n/a	n/a	n/a	BOOTSEL1	BOOTSEL0	TAPESEL1	TAPESEL0

MEDID1, MEDID0 reflect the values on the respective pins. Similarly, the DRVID0, DRVID1 reflect the values on the DRVID1 and DRVID0 pins.

The TAPESEL1, TAPESEL0 functionality is retained as defined in the non-enhanced TDR, except that the application of boot drive restriction (boot drive cannot be a tape drive) depends on what drive selected is by the BOOTSEL1, BOOTSEL0 bits.

The BOOTSEL1, BOOTSEL0 are not reset by software resets and are decoded as shown below. These bits allow for reconfiguring the boot up drive and only reset by hardware reset. A drive can be enabled by remapping the internal DS0 and ME0 to one of the other drive select and motor enable lines (Refer to "Selectable Boot Drives" in the Design applications chapter). Once a non-default value for BOOTSEL1 and BOOTSEL0 is selected, all programmable bits are virtual designations of drives, i.e., it is the user's responsibility to know the mapping scheme detailed in the following table.

BOOTSEL1	BOOTSEL0	Mapping:
0	0	DS0 → FDS0, ME0 → FDME0 DS1 → FDS1, ME1 → FDME1 DS2 → FDS2, ME2 → FDME2
0	1	DS0 → FDS1, ME0 → FDME1 DS1 → FDS0, ME1 → FDME0 DS2 → FDS2, ME2 → FDME2
1	0	DS0 → FDS2, ME0 → FDME2 DS1 → FDS1, ME1 → FDME1 DS2 → FDS0, ME2 → FDME0
1	1	Reserved

2.1.9 DATARATE SELECT REGISTER (DSR)

Bits	7	6	5	4	3	2	1	0
Function	S/W RESET	POWER DOWN	PDOSC	PRE COMP2	PRE COMP1	PRE COMP0	DRATE SEL1	DRATE SEL0
H/W Reset State	0	0	0	0	0	0	1	0
Auto PD State	S/W RESET	POWER DOWN	PDOSC	PRE COMP2	PRE COMP1	PRE COMP0	DRATE SEL1	DRATE SEL0

This register ensures backward compatibility with the 82072 floppy controller and is write-only. Changing the data rate changes the timings of the drive control signals. To ensure that drive timings are not violated when changing data rates, choose a drive timing such that the fastest data rate will not violate the timing.

The PDOSC bit is used to implement crystal oscillator power management. The internal oscillator in the 82078 can be programmed to be either powered on or off via PDOSC. This capability is independent of the chip's powerdown state. Auto powerdown mode and powerdown via POWERDOWN bit has no effect over the power state of the oscillator.

In the default state the PDOSC bit is low and the oscillator is powered up. When this bit is programmed to a one, the oscillator is shut off. Hardware reset clears this bit to a zero. Neither of the software resets (via DOR or DSR) have any effect on this bit. Note, PDOSC should only be set high when the part is in the powerdown state, otherwise the part will not function correctly and must be hardware reset once the oscillator has turned back on and stabilized. Setting the PDOSC bit has no effect on the clock input to the 82078 (the X1 pin). The clock input is separately disabled when the part is powered down. The SAVE command checks the status of PDOSC, however, the RESTORE command will not restore the bit high.

S/W RESET behaves the same as DOR RESET except that this reset is self cleaning.

POWERDOWN bit implements direct powerdown. Setting this bit high will put the 82078 into the powerdown state regardless of the state of the part. The part is internally reset and then put into powerdown. No status is saved and any operation in progress is aborted. A hardware or software reset will exit the 82078 from this powerdown state.

PRECOMP 0-2 adjusts the WRDATA output to the disk to compensate for magnetic media phenomena known as bit shifting. The data patterns that are susceptible to bit shifting are well understood and the 82078 compensates the data pattern as it is written to the disk. The amount of pre-compensation is dependent upon the drive and media, but in most cases the default value is acceptable.

Table 2-2. Precompensation Delays

PRECOMP	Precompensation Delays	
DSR[432]	x1 @ 24 MHz	x1 @ 48 MHz if CLK48 = 1, enabled only @ 2 Mbps if CLK48 = 0, enabled at all data rates
111	0.00 ns–disabled	
001	41.67	20.84
010	83.34	41.67
011	125.00	62.5
100	166.67	83.34
101	208.33	104.17
110	250.00	125
000	DEFAULT	

Table 2-3. Default Precompensation Delays

Data Rate	Precompensation Delays (ns)
2 Mbps	20.84
1 Mbps	41.67
0.5 Mbps	125
0.3 Mbps	125
0.25 Mbps	125

The 82078 starts pre-compensating the data pattern starting on Track 0. The CONFIGURE command can change the track that pre-compensating starts on. Table 2-2 lists the pre-compensation values that can be selected and Table 2-3 lists the default pre-compensation values. The default value is selected if the three bits are zeroes.

DRATE 0-1 select one of the four data rates as listed in Table 2-4. The default value is 250 Kbps after a "Hardware" reset. Other "Software" Resets do not affect the DRATE or PRECOMP bits.

Table 2-4. Data Rates

DRATESEL1	DRATESEL0	DATA RATE
1	1	1 Mbps
0	0	500 Kbps
0	1	300 Kbps
1	0	250 Kbps

2.1.10 MAIN STATUS REGISTER (MSR)

Bits	7	6	5	4	3*	2	1	0
Function	RQM	DIO	NON DMA	CMD BSY	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY
H/W Reset State	0	X	X	X	X	X	X	X
Auto PD State	1	0	0	0	0	0	0	0

The Main Status Register is a read-only register and is used for controlling command input and result output for all commands.

RQM—Indicates that the host can transfer data if set to 1. No access is permitted if set to a 0.

DIO—Indicates the direction of a data transfer once RQM is set. A 1 indicates a read and a 0 indicates a write is required.

NON-DMA—This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfers and the reading of result bytes.

COMMAND BUSY—This bit is set to a one when a command is in progress. This bit goes active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (SEEK, RECALIBRATE commands), this bit returns to a 0.

DRV x BUSY—These bits are set to ones when a drive is in the seek portion of a command, including seeks and recalibrates.

Some example values of the MSR are:

- MSR = 80H; The controller is ready to receive a command.
- MSR = 90H; executing a command or waiting for the host to read status bytes (assume DMA mode).
- MSR = D0H; waiting for the host to write status bytes.

2.1.11 FIFO (DATA)

All command parameter information and disk data transfers go through the FIFO. The FIFO is 16 bytes in size and has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to an 8272A compatible mode after a "Hardware" reset (Reset via pin 32). "Software" Resets (Reset via DOR or DSR register) can also place the 82078 into 8272A compatible mode if the LOCK bit is set to "0" (See the definition of the LOCK bit), maintaining PC-AT hardware compatibility. The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 2-5 gives several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold\#} \times 1/\text{DATA RATE} \times 8 - 1.5\ \mu s = \text{DELAY}$$

Table 2-5. FIFO Threshold Examples

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	$1 \times 8\ \mu s - 1.5\ \mu s = 6.5\ \mu s$
2 bytes	$2 \times 8\ \mu s - 1.5\ \mu s = 14.5\ \mu s$
8 bytes	$8 \times 8\ \mu s - 1.5\ \mu s = 62.5\ \mu s$
15 bytes	$15 \times 8\ \mu s - 1.5\ \mu s = 118.5\ \mu s$

FIFO Threshold Examples	Maximum Delay to Servicing at 500 Kbps Data Rate
1 byte	$1 \times 16\ \mu s - 1.5\ \mu s = 14.5\ \mu s$
2 bytes	$2 \times 16\ \mu s - 1.5\ \mu s = 30.5\ \mu s$
8 bytes	$8 \times 16\ \mu s - 1.5\ \mu s = 126.5\ \mu s$
15 bytes	$15 \times 16\ \mu s - 1.5\ \mu s = 238.5\ \mu s$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the 82078 enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred. An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC.

2.1.12 DIGITAL INPUT REGISTER (DIR, PC-AT MODE)

This register is read only in all modes. In PC-AT mode only bit 7 is driven, all other bits remain tri-stated.

Bits	7	6	5	4	3	2	1	0
Function	DSK CHG	—	—	—	—	—	—	—
H/2 Reset State	DSK CHG	—	—	—	—	—	—	—
Auto PD State	0	—	—	—	—	—	—	—

(—) means these bits are tri-stated when read.

DSKCHG monitors the pin of the same name and reflects the opposite value seen on the disk cable. The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits remain tri-stated.

2.1.13 DIGITAL INPUT REGISTER (DIR, PS/2 MODE)

DIR								
R/W	7	6*	5*	4*	3	2	1	0
R	DSK CHG	IDLE	PD	IDLEMSK	1	DRATE SEL1	DRATE SEL0	HIGH DENS#
H/W Reset	DSK CHG	1	1	1	1	1	0	1
Auto PD	0	1	1	UC	1	UC	UC	UC

(*) These bits are only available when PS2 STAT = 1: Bits 5 and 6 show the status of PD (powerdown) and IDLE respectively. Bit 4 shows the status of IDLEMSK, this bit disables the IDLE pin when active.

Bit 3 returns a value of "1", and the DRATE SEL1–0 return the value of the current data rate selected (see Table 2-4 for values).

HIGHDENS# is low whenever the 500 Kbps or 1 Mbps data rates are selected. It is high when either 250 Kbps, 300 Kbps, or 2 Mbps is selected.

The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits (as applicable) remain unchanged.

The Drive Specification Command modifies the DRATE SEL bits. Refer to Table 6-2 for a description.

2.1.14 DIGITAL INPUT REGISTER (DIR, MODEL 30 MODE)

Bits	7	6*	5*	4*	3	2	1	0
Function	DSK CHG#	IDLE	PD	IDLEMSK	DMA GATE#	NOPREC	DRATE SEL1	DRATE SEL0
H/W Reset State	N/A	0	0	0	0	0	1	0
Auto PD State	1	1	1	UC	UC	UC	UC	UC

(*) These bits are only available when PS2 STAT = 1: Bits 5 and 6 show the status of PD (powerdown) and IDLE respectively. Bit 4 shows the status of IDLEMSK, this bit disables the IDLE pin when active. Bit 7 (DSKCHG) is inverted in Model 30 Mode.

The DSKCHG# bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits (as applicable) remain unchanged.

The Drive Specification Command modifies the DRATE SEL bits. Refer to Table 6-2 for information regarding the mapping of these bits.

Bit 3 reflects the value of DMAGATE# bit set in the DOR register.

Bit 2 reflects the value of NOPREC bit set in the CCR register.

2.1.15 CONFIGURATION CONTROL REGISTER (CCR, PC AT and PS/2 MODES)

This register sets the datarate and is write only.

Bits	7	6	5	4*	3	2	1	0
Function	—	—	—	IDLEMSK	—	—	DRATE SEL1	DRATE SEL0
H/W Restate State	—	—	—		—	—	1	0
Auto PD State	—	—	—	IDLEMSK	—	—	DRATE SEL1	DRATE SEL0

(*) This bit is enabled only when PS2 STAT = 1 (Powerdown Mode). Refer to the table in the Data Rate Select Register for values. Unused bits should be set to 0. IDLEMSK is not available in the CCR for PC AT mode. In PC AT, IDLEMSK is available in the SRB.

2.1.16 CONFIGURATION CONTROL REGISTER (CCR, MODEL 30 MODE)

Bits	7	6	5	4*	3	2	1	0
Function	—	—	—	IDLEMSK	—	NOPREC	DRATE SEL1	DRATE SEL0
H/W Reset State	—	—	—	0	—	0	1	0
Auto PD State	—	—	—	UC	—	UC	UC	UC

(*) This bit is enabled only when PS2 STAT = 1 (Powerdown Mode). NOPREC has no function, and is reset to "0" with a Hardware RESET only.

2.2 Reset

There are three sources of reset on the 82078; the RESET pin, a reset generated via a bit in the DOR and a reset generated via a bit in the DSR. All resets take the 82078 out of the powerdown state.

In entering the reset state, all operations are terminated and the 82078 enters an idle state. Activating reset while a disk write activity is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, and the 82078 waits for a new command. Drive polling will start unless disabled by a new CONFIGURE command.

2.2.1 RESET PIN ("HARDWARE") RESET

The RESET pin is a global reset and clears all registers except those programmed by the SPECIFY command. The DOR Reset bit is enabled and must be cleared by the host to exit the reset state.

2.2.2 DOR RESET vs DSR RESET ("SOFTWARE" RESET)

These two resets are functionally the same. The DSR Reset is included to maintain 82072 compatibility. Both will reset the 82072 core which affects drive status information. The FIFO circuits will also be reset if the LOCK bit is a "0" (see definition of the LOCK bit). The DSR Reset clears itself automatically while the DOR Reset requires the host to manually clear it. DOR Reset has precedence over the DSR Reset. The DOR Reset is set automatically upon a pin RESET. The user must manually clear this reset bit in the DOR to exit the reset state.

The t30a specification in the A.C. Specifications gives the minimum amount of time that the DOR reset must be held active. This amount of time that the DOR reset must be held active is dependent upon the data rate. The 82078 requires that the DOR reset bit must be held active for at least 0.5 μs at 250 Kbps. This is less than a typical ISA I/O cycle time.

2.3 DMA Transfers

DMA transfers are enabled with the SPECIFY command and are initiated by the 82078 by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting DACK# and addresses need not be valid (CS# can be held inactive during DMA transfers).

3.0 DRIVE INTERFACE

The 82078 has integrated all of the logic needed to interface to a floppy disk or a tape drive which use floppy interface. All drive outputs have 24 mA drive capability and all inputs use a receive buffer with hysteresis. The internal analog data separator requires no external components, yet allows for an extremely wide capture range with high levels of read-data jitter, and ISV. The designer needs only to run the 82078 disk drive signals to the disk or tape drive connector.

3.1 Cable Interface

Generally, 5.25" drive uses open collector drivers and 3.5" drives (as used on PS/2) use totem-pole drivers. The output buffers on the 82078 do not change between open collector or totem-pole, they are always totem-pole.

DRVDEN0 and DRVDEN1 connect to pins 2 and 6 or 33 (on most disk drives) to select the data rate sent from the drive to the 82078. The polarity of DRVDEN0 and DRVDEN1 can be programmed through the Drive Specification command (see the command description for more information).

When the 82078SL is operating at 3.3V, the floppy drive interface can be configured to either 5.0V or 3.3V, via the V_{CCF} (pin 41). The drive interface follows the voltage level on V_{CCF}. A selectable drive interface allows the system designer the greatest flexibility when designing a low voltage system.

3.2 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When lock is achieved, the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called Data Window, is used to internally sample the serial data. One state of Data Window is used to sample the data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

To support reliable disk reads the data separator must track fluctuations in the read data frequency. Frequency errors primarily arise from two sources: motor rotation speed variation and instantaneous speed variation (ISV). A second condition, and one that opposes the ability to track frequency shifts is the response to bit jitter.

The internal data separator consists of two analog phase lock loops (PLLs) as shown in Figure 3-1. The two PLLs are referred to as the reference PLL and the data PLL. The reference PLL (the master PLL) is used to bias the data PLL (the slave PLL). The reference PLL adjusts the data PLL's operating point as a function of process, junction temperature and supply voltage. Using this architecture it was possible to eliminate the need for external trim components.

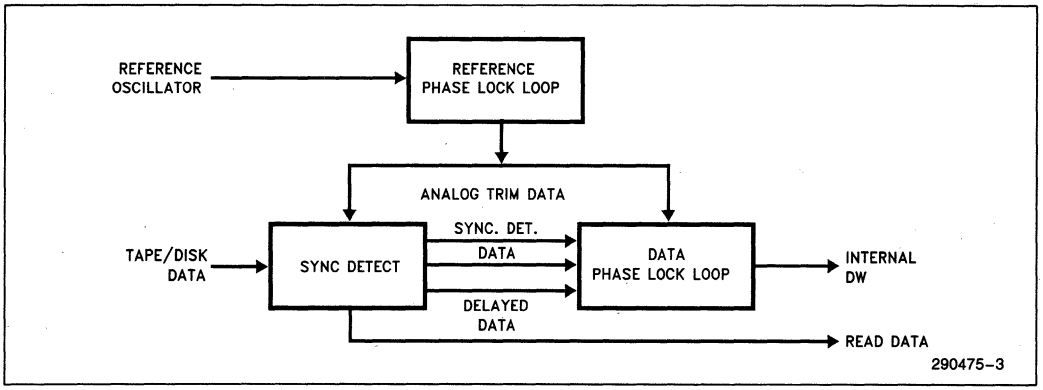

Figure 3-1. Data Separator Block Diagram

PHASE LOCK LOOP OVERVIEW

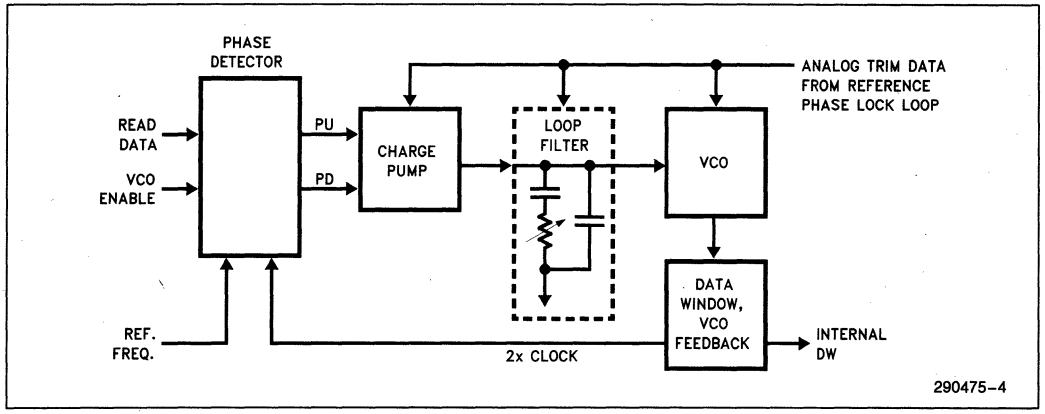

Figure 3-2. Data PLL

Figure 3-2 shows the data PLL. The reference PLL has control over the loop gain by its influence on the charge pump and the VCO. In addition the reference PLL controls the loop filter time constant. As a result the closed loop transfer function of the data PLL is controlled, and immune to the first order, to environmental factors and process variation.

Systems with analog PLLs are often very sensitive to noise. In the design of this data separator many steps were taken to avoid noise sensitivity problems. The analog section of the chip has a separate VSS pin (AVSS) which should be connected externally to a noise free ground. This provides a clean basis for VSS referenced signals. In addition many analog circuit features were employed to make the overall system as insensitive to noise as possible.

3.2.1 JITTER TOLERANCE

The jitter immunity of the system is dominated by the data PLL's response to phase impulses. This is measured as a percentage of the theoretical data window by dividing the maximum readable bit shift by a 1/4 bit cell distance. For instance, if the maximum allowable bit shift is 300 ns for a 500 Kbps data stream, the jitter tolerance is 60%.

3.2.2 LOCKTIME (tLOCK)

The lock, or settling time of the data PLL is designed to be 64 bit times (8 sync bytes). The value assumes that the sync field jitter is 5% the bit cell or less. This level of jitter is realistic for a constant bit pattern. Intersymbol interference should be equal, thus nearly eliminating random bit shifting.

3.2.3 CAPTURE RANGE

Capture Range is the maximum frequency range over which the data separator will acquire phase lock with the incoming RDDATA signal. In a floppy disk environment, this frequency variation is composed of two components: drive motor speed error and ISV. Frequency is a factor which may determine the maximum level of the ISV (Instantaneous Speed Variation) component. In general, as frequency increases the allowed magnitude of the ISV component will decrease. When determining the capture range requirements, the designer should take the maximum amount of frequency error for the disk drive and double it to account for media switching between drives.

3.3 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. The shifting of bits is a known phenomena of magnetic media and is dependent upon the disk media AND the floppy drive.

The 82078 monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late (or not at all) relative to the surrounding bits. Figure 3-3 is a block diagram of the internal circuit.

The top block is a 13-bit shift register with the no delay tap being in the center. This allows 6 levels of early and late shifting with respect to nominal. The shift register is clocked at the main clock rate (24 MHz). The output is fed into 2 multiplexors one for early and one for late. A final stage of multiplexors combines the early, late and normal data stream back into one which is the WRDATA output.

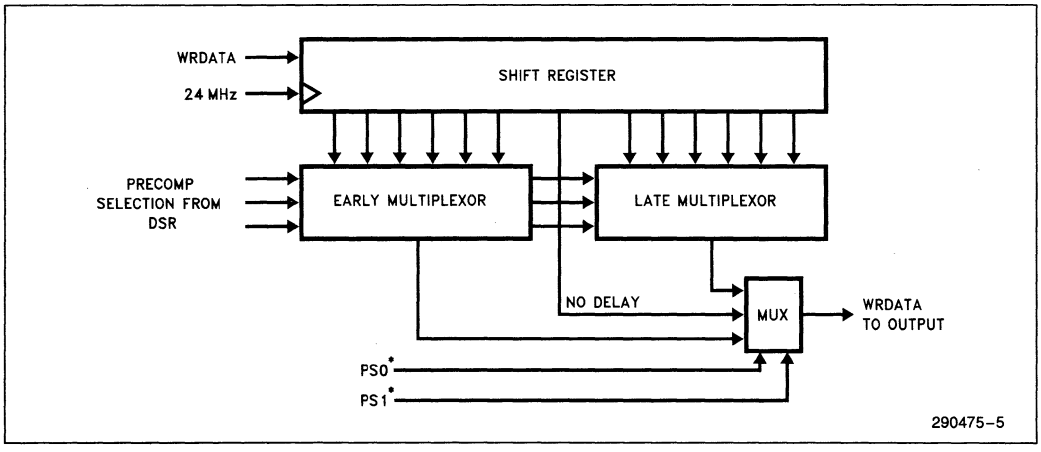

Figure 3-3. Precompensation Block Diagram

4.0 POWER MANAGEMENT FEATURES

The 82078 contains power management features that makes it ideal for design of portable personal computers. In addition to all of the power management features the 82078SL also operates at 3.3V. These features can be classified into power management of the part and that of the internal oscillator. The powerdown of the part is done independently of the internal oscillator in the 82078.

4.1 Power Management Scheme

The 82078 supports two powerdown modes, direct powerdown and automatic powerdown. Direct powerdown refers to direct action by the software to powerdown without dependence on external factors. Automatic powerdown results from 82078's monitoring of the current conditions according to a previously programmed mode. Any hardware reset disables the automatic POWERDOWN command, however, software resets have no effect on the command. The 82078 also supports powerdown of its internal crystal oscillator independent of the powerdown modes described above. By setting bit 5 (PDOSC) in the DSR register, the internal oscillator is turned off. This bit has sole control of the oscillator powerdown, allowing the internal clock to be turned off when an external oscillator is used.

4.2 3.3V Support for Portable Platforms

The portable market share of the personal computing market has increased significantly. To improve power conservation on portable platforms, designs are migrating from 5.0V to 3.3V. Intel's 82078SL allows designers to incorporate 3.3V floppy disk controller support in their systems. The 82078SL has a SEL3V# pin to allow selection of either 5.0V or 3.3V operation. In order to support the slower migration of floppy drives to 3.3V and allow system vendors to use standard 5.0V floppy drive inventory, the 82078SL accommodates a 5.0V tolerant floppy drive interface. This is achieved by changing the floppy drive's interface power supply, VCCF between 5.0V and 3.3V supplies. The 82078SL's 3.3V D.C. specification conforms to the JEDEC standard that describes the operating voltage levels for Integrated Circuits operating at 3.3V $\pm$0.3V. The 82077SL also maintains compatibility to 5.0V A.C. specifications.

4.3 Oscillator Power Management

The 82078 supports a built-in crystal oscillator that can be programmed to be either powered down or active, independent of the power state of the chip. This capability is implemented by the PDOSC bit in the DSR. When PDOSC is set low, the internal oscillator is on, it is off when the bit is high. Note, a DSR powerdown does not turn off the oscillator.

When the external oscillator is used, power can be saved by turning off the internal oscillator. If the internal oscillator is used, the oscillator may be powered up (even when the rest of the chip is powered off) allowing the chip to wake up quickly and in a stable state. It is recommended to keep the internal oscillator on even when in the powerdown state. The main reason for this is that the recovery time of the oscillator during wake up may take tens of milliseconds under the worst case, which may create problems with any sensitive application software. In a typical application the internal oscillator should be on unless the system goes into a power saving or standby mode (such a mode request would be made by a system time out or by a user). In this case, the system software would take over and must turn on the oscillator sufficiently ahead of awakening the part.

In the case of the external oscillators, the power up characteristics are similar. If the external source remains active during the time the 82078 is powered down, then the recovery time effect is minimized. The PD pin can be used to turn off the external source. While the PD pin is active, the 82078 does not require a clock source. However, when the PD pin is inactive, the clocking source, once it starts oscillating, must be completely stable to ensure that the 82078 operates properly.

4.4 Part Power Management

This section deals with the power management of the rest of the chip excluding the oscillator. This section explains powerdown modes and wake up modes.

4.4.1 DIRECT POWERDOWN

Direct powerdown is conducted via the POWERDOWN bit in the DSR register (bit 6). Programming this bit high will powerdown 82078. All status is lost if this type of powerdown mode is used. The part can exit powerdown from this mode via any hardware or software reset. This type of powerdown overrides the automatic powerdown. When the part is in automatic powerdown and the DSR powerdown is issued, the previous status of the part is lost and the 82078 resets to its default values.

4.4.2 AUTO POWERDOWN

Automatic powerdown is conducted via a "Powerdown Mode" command. There are four conditions required before the part will enter powerdown. All these conditions must be true for the part to initiate the powerdown sequence. These conditions follow:

1. The motor enable pins FDME[0:3] must be inactive.
2. The part must be idle; this is indicated by MSR = 80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupt).
3. The head unload timer (HUT, explained in the SPECIFY command) must have expired.
4. The auto powerdown timer must have timed out.

The command can be used to enable powerdown by setting the AUTO PD bit in the command to high. The command also provides a capability of programming a minimum power up time via the MIN DLY bit in the command. The minimum power up time refers to a minimum amount of time the part will remain powered up after being awakened or reset. An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down provided all the remaining conditions are met.

Any software reset will reinitialize the timer. Changing of data rate extends the auto powerdown timer by up to 10 ms, but only if the data rate is changed during the countdown.

Disabling the auto powerdown mode cancels the timers and holds the 82078 out of auto powerdown.

The IDLE pin can be masked via the IDLEMSK bit in Status Register B (Enhanced AT/EISA). When in PS/2 mode, the PS/2 STAT bit in the Powerdown Command can be set to enable PD and IDLE bits in the DIR register (bits 5 and 6) and IDLEMSK (bit 4) can be enabled.

4.4.3 WAKE UP MODES

This section describes the conditions for awakening the part from both direct and automatic powerdown. Power conservation or extension of battery life is the main reason power management is required. This means that the 82078 must be kept in powerdown state as long as possible and should be powered up as late as possible without compromising software transparency.

To keep the part in powerdown mode as late as possible implies that the part should wake up as fast as possible. However, some amount of time is required for the part to exit powerdown state and prepare the internal microcontroller to accept commands. Application software is very sensitive to such a delay and in order to maintain software transparency, the recovery time of the wake up process must be carefully controlled by the system software.

4.4.3.1 Wake Up from DSR Powerdown

If the 82078 enters the powerdown through the DSR powerdown bit, it must be reset to exit. Any form of software or hardware reset will serve, although DSR is recommended. No other register access will awaken the part, including writing to the DOR's motor enable (FDME[0:3]) bits.

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened by a software reset, the auto powerdown command (including the minimum delay timer) will once again become effective as previously programmed. If the part is awakened via a hardware reset, the auto powerdown is disabled.

After reset, the part will go through a normal sequence. The drive status will be initialized. The FIFO mode will be set to default mode on a hardware reset or on a software reset if the LOCK command has not blocked it. Finally, after a delay, the polling interrupt will be issued.

4.4.3.2 Wake Up from Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the 82078 resumes operation as though it was never in powerdown. Besides activating the RESET pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part).
2. A read from the MSR register.
3. A read or write to the FIFO register.

Any of these actions will wake up the part. Once awake, 82078 will reinitiate the auto powerdown timer for 10 ms or 0.5 sec. (depending on the MIN DLY bit the auto powerdown command). When operating at 2 Mbps, the time is halved to 5 ms or 0.25 sec. depending on the MIN DLY bit. The part will powerdown again when all the auto powerdown conditions are satisfied.

4.5 Register Behavior

The register descriptions and their values in the powerdown state are listed in the Microprocessor Interface section. Table 4-1 reiterates the AT and PS/2 (including model 30) configuration registers available. It also shows the type of access permitted. In order to maintain software transparency, access to all the registers must be maintained. As Table 4-1 shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Table 4-1. 82078 Register Behavior

Address	Available Registers	Access	
	PC-AT	PS/2 (Model 30)	Permitted
Access to these registers DOES NOT wake up the part			
000	—	SRA	R
001	SRB (EREG EN = 1)	SRB	R/W
010	DOR*	DOR*	R/W
011	TDR	TDR	R/W
100	DSR*	DSR*	W
110	—	—	—
111	DIR	DIR	R
111	CCR	CCR	W
Access to these registers wake up the part			
100	MSR	MSR	R
101	FIFO	FIFO	R/W

*Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (either via DOR or DSR reset bits) will wake up the part.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in Section 2.1. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed. None of the extended registers effect the behavior of the powerdown mode.

4.6 Pin Behavior

The 82078 is specifically designed for the portable PC systems in which the power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of 82078 can be divided into two major categories; system interface and floppy disk drive interface. The floppy disk drive pins are disabled such that no power will be drawn through the 82078 as a result of any voltage applied to the pin within the 82078's power supply range. The floppy disk drive interface pins are configurable by the FDI TRI bit in the auto powerdown command. When the bit is set the output pins of the floppy disk drive retain their original state. All other pins are either disabled or unchanged as depicted in Table 4-4. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

4.6.1 SYSTEM INTERFACE PINS

Table 4-2 gives the state of the system interface pins in the powerdown state. Pins unaffected by powerdown are labeled "UC". Input pins are "DISABLED" to prevent them from causing currents internal to the 82078 when they have indeterminate input values.

Table 4-2. System Interface Pins

System Pins	State In Powerdown	System Pins	State In Powerdown
Input Pins		**Output Pins**	
CS#	UC	DRQ	UC (Low)
RD#	UC	INT	UC (Low)
WR#	UC	PD	HIGH
A[0:2]	UC	IDLE	High (Auto PD) Low (DSR PD)
DB[0:7]	UC	DB[0:7]	UC
RESET	UC		
IDENTn	UC		
DACK#	Disabled		
TC	Disabled		
X[1:2]	Programmable		

Two pins which can be used to indicate the status of the part are IDLE and PD. Table 4-3 shows how these pins reflect the 82078 status.

Table 4-3. 82078 Status Pins

PD	IDLE	MSR	Part Status
1	1	80H	Auto Powerdown
1	0	RQM = 1; MSR[6:0] = X	DSR Powerdown
0	1	80H	Idle
0	0	—	Busy

The IDLE pin indicates when the part is idle state and can be powered down. It is a combination of MSR equalling 80H, the head being unloaded and the INT pin being low. As shown in the table the IDLE pin will be low when the part is in DSR powerdown state. The PD pin is active whenever the part is in the powerdown state. It is active for either mode of powerdown. The PD pin can be used to turn off an external oscillator of other floppy disk drive interface hardware.

4.6.2 FDD INTERFACE PINS

The FDD interface "input" pins during powerdown are disabled or unchanged as shown in Table 4-4. The floppy disk drive "output" pins are programmable by the FDI TRI bit in the auto powerdown command. Setting of the FDI TRI bit in the auto powerdown command results in the interface retaining its normal state. When this bit is low (default state) all output pins in the FDD interface to the floppy disk drive itself are tri-stated. Pins used for local logic control or part programming are unaffected. Table 4-4 depicts the state of the floppy disk interface pins in the powerdown state (FDI TRI is low).

Table 4-4. 82078 FDD Interface Pins

FDD Pins	State In Powerdown	FDD Pins	State in Powerdown
Input Pins		**Output Pins (FDI TRI = 0)**	
RDDATA	Disabled	FDME[0:3]#	Tristated
WP	Disabled	FDS[0:3]#	Tristated
TRK0	Disabled	DIR#	Tristated
INDX#	Disabled	STEP#	Tristated
DRV2#	Disabled	WRDATA#	Tristated
DSKCHG#	Disabled	WE#	Tristated
		HDSEL#	Tristated
		DRVDEN[0:1]#	Tristated

5.0 CONTROLLER PHASES

For simplicity, command handling in the 82078 can be divided into three phases: Command, Execution and Result. Each phase is described in the following sections.

When there is no command in progress, the 82078 can be in idle, drive polling or powerdown state.

5.1 Command Phase

After a reset, the 82078 enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the 82078 before the command phase is complete (Please refer to Section 6.0 for the command descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the 82078, the host must examine the RQM and DIO bits of the Main Status Register. RQM, DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the 82078 after each write cycle until the received byte is processed. The 82078 asserts RQM again to request each parameter byte of the command, unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0", and the 82078 automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to retain compatibility with the 8272A, and to provide for the proper handling of the "Invalid Command" condition.

5.2 Execution Phase

All data transfers to or from the 82078 occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the SPECIFY command.

Each data byte is transferred by an INT or DRQ depending on the DMA mode. The CONFIGURE command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, (threshold) is defined as the number of bytes available to the 82078 when service is requested from the host, and ranges from 1 to 16. The parameter FIFOTHR which the user programs is one less, and ranges from 0 to 15.

A low threshold value (i.e., 2) results in longer periods of time between service requests, but requires faster servicing of the request, for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e., 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

5.2.1 NON-DMA MODE, TRANSFERS FROM THE FIFO TO THE HOST

The INT pin and RQM bits in the Main Status Register are activated when the FIFO contains 16 (or set threshold) bytes, or the last bytes of a full sector transfer have been placed in the FIFO. The INT pin can be used for interrupt driven systems and RQM can be used for polled sytems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO, then 82078 deactivates the INT pin and RQM bit.

5.2.2 NON-DMA MODE, TRANSFERS FROM THE HOST TO THE FIFO

The INT pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The INT pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has (threshold) bytes remaining in the FIFO. The INT pin will also be deactivated if TC and DACK# both go inactive. The 82078 enters the result phase after the last byte is taken by the 82078 from the FIFO (i.e., FIFO empty condition).

5.2.3 DMA MODE, TRANSFERS FROM THE FIFO TO THE HOST

The 82078 activates the DRQ pin when the FIFO contains 16 (or set threshold) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The 82078 will deactivate the DRQ pin when the FIFO becomes empty. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of RD#, on the last byte, if no edge is present on DACK#). Note that DACK# and TC must overlap for at least 50 ns for proper functionality.

5.2.4 DMA MODE, TRANSFERS FROM THE HOST TO THE FIFO

The 82078 activates the DRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the DACK# and WR# pins and placing data in the FIFO. DRQ remains active until the FIFO becomes full. DRQ is again set true when the FIFO has (threshold) bytes remaining in the FIFO. The 82078 will also deactivate the DRQ pin when TC becomes true (qualified by DACK# by overlapping by 50 ns), indicating that no more data is required. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of WR# of the last byte, if no edge is present on DACK#).

5.2.5 DATA TRANSFER TERMINATION

The 82078 supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multisector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the 82078 will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the 82078, the internal sector count will be complete when 82078 reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the 82078 to read the last 16 bytes from the FIFO. The host must tolerate this delay.

5.3 Result Phase

The generation of INT determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the 82078 before the result phase is complete. (Refer to Section 6.0 on command descriptions.) These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read from the FIFO. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared. This indicates that the 82078 is ready to accept the next command.

6.0 COMMAND SET/DESCRIPTIONS

Commands can be written whenever the 82078 is in the command phase. Each command has a unique set of needed parameters and status results. The 82078 checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it was invalid, the next time the RQM bit in the MSR register is a "1" the DIO and CB bits will also be "1", indicating the FIFO must be read. A result byte of 80H will be read out of the FIFO, indicating an invalid command was issued. After reading the result byte from the FIFO the 82078 will return to the command phase. Table 6-1 is a summary of the Command set.

Table 6-1. 82078 Command Set

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
READ DATA										
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer between the FDD and System
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information after Command Execution
	R					R				
	R					N				
READ DELETED DATA										
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer between the FDD and System
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information after Command Execution
	R					R				
	R					N				
WRITE DATA										
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer between the FDD and System
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information after Command Execution
	R					R				
	R					N				

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
WRITE DELETED DATA										
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer between the FDD and System
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information after Command Execution
	R					R				
	R					N				
READ TRACK										
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer between the FDD and System. FDC Reads All Sectors from Index Hole to EOT
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information after Command Execution
	R					R				
	R					N				
VERIFY										
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL/SC				
Execution										Data Transfer between the FDD and System
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information after Command Execution
	R					R				
	R					N				
VERSION										
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
FORMAT TRACK										
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				N					Bytes/Sector
	W				SC					Sectors/Cylinder
	W				GPL					Gap3
	W				D					Filler Byte
Execution For Each Sector Repeat:	W				C					Input Sector Parameters
	W				H					
	W				R					
	W				N					
										82078 Formats an Entire Cylinder
Result	R				ST 0					Status Information after Command Execution
	R				ST 1					
	R				ST 2					
	R				Undefined					
	R				Undefined					
	R				Undefined					
	R				Undefined					
SCAN EQUAL										
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information prior to Command Execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared between the FDD and Main-System
Result	R				ST 0					Status Information after Command Execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID Information after Command Execution
	R				H					
	R				R					
	R				N					

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Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
SCAN LOW OR EQUAL										
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information
	W				H					Prior to Command
	W				R					Execution
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared Between the FDD and Main-System
Result	R				ST 0					Status Information
	R				ST 1					After Command
	R				ST 2					Execution
	R				C					
	R				H					Sector ID Information
	R				R					After Command
	R				N					Execution
SCAN HIGH OR EQUAL										
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information
	W				H					Prior to Command
	W				R					Execution
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared Between the FDD and Main-System
Result	R				ST 0					Status Information
	R				ST 1					After Command
	R				ST 2					Execution
	R				C					
	R				H					Sector ID Information
	R				R					After Command
	R				N					Execution

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	Enhanced Controller
Execution										Head Retracted to Track 0 Interrupt
SENSE INTERRUPT STATUS										
Command	W	0	0	0	1	0	0	0	0	Command Codes
Result	R				ST 0					Status Information at the End of each Seek Operation
	R				PVN					
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT					HUT			
	W	HLT							ND	
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R				ST 3					Status Information about FDD
DRIVE SPECIFICATION COMMAND										
Command	W	1	0	0	0	1	1	1	0	Command Codes
Phase	W	0	FD1	FD0	PTS	DRT1	DRT0	DT1	DT0	
	:	:	:	:	:	:	:	:	:	0–4 bytes issued
	W	DN	NRP	0	0	0	0	0	0	
Result	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 0
Phase	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 1
	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 2
	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 3
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				NCN					
Execution										Head is Positioned over Proper Cylinder on Diskette
CONFIGURE										
Command	W	CLK48	0	0	1	0	0	1	1	Command Code
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL			FIFOTHR		
	W				PRETRK					
RELATIVE SEEK										
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				RCN					

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
DUMPREG										
Command Execution	W	0	0	0	0	1	1	1	0	*Note Registers Placed in FIFO
Result	R				PCN-Drive 0					
	R				PCN-Drive 1					
	R				PCN-Drive 2					
	R				PCN-Drive 3					
	R		SRT				HUT			
	R				HLT				ND	
	R				SC/EOT					
	R	LOCK	0	D_3	D_2	D_1	D_0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL		FIFOTHR			
	R				PRETRK					
READ ID										
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The First Correct ID Information on the Cylinder is Stored in Data Register
Result	R				ST 0					Status Information after Command Execution
	R				ST 1					
	R				ST 2					
	R				C					
	R				H					Disk Status after the Command has Completed
	R				R					
	R				N					
PERPENDICULAR MODE										
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	D_3	D_2	D_1	D0	GAP	WGATE	
LOCK										
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	
PART ID										
Command	W	0	0	0	1	1	0	0	0	Command Code
Result	R	0	0	0		—STEPPING—			1	Part ID Number
POWERDOWN MODE										
Command	W	0	0	0	1	0	1	1	1	Command Code
	W	0	0	EREG EN	X	PS2 STAT	FDI TRI	MIN DLY	AUTO PD	
Result	R	0	0	EREG EN	X	PS2 STAT	FDI TRI	MIN DLY	AUTO PD	
OPTION										
Command	W	0	0	1	1	0	0	1	1	Command Code
	W				—RSVD—				ISO	

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
					SAVE					
Command Phase	W	0	0	1	0	1	1	1	0	Command Code
Result Phase	R	CLK 48	SEL 3V#	PD OSC	PC2	PC1	PC0	DRATE1	DRATE0	Save Info to Reprogram the FDC
	R	0	0	0	0	0	0	0	ISO	
	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT					HUT			
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	D_3	D_2	D_1	D_0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL		FIFOTHR			
	R	PRETRK								
	R	0	0	EREG EN	RSVD	PS2 STAT	FDI TRI	MIN DLY	AUTO PD	
	R	DISK/STATUS								
	R	RSVD								
	R	RSVD								
					RESTORE					
Command Phase	W	0	1	0	0	1	1	1	0	Command Code
Result	W	CLK48	SEL 3V#	0	PC2	PC1	PC0	DRATE1	DRATE0	Restore Original Register Status
	W	0	0	0	0	0	0	0	ISO	
	W	PCN-Drive 0								
	W	PCN-Drive 1								
	W	PCN-Drive 2								
	W	PCN-Drive 3								
	W	SRT					HUT			
	W	HLT							ND	
	W	SC/EOT								
	W	LOCK	0	D_3	D_2	D_1	D_0	GAP	WGATE	
	W	0	EIS	EFIFO	POLL		FIFOTHR			
	W	PRETRK								
	W	0	0	EREG EN	RSVD	PS2 STAT	FDI TRI	MIN DLY	AUTO PD	
	W	DISK/STATUS								
	W	RSVD								
	W	RSVD								

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Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
FORMAT AND WRITE										
Command	W	1	MFM	1	0	1	1	0	1	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				N					
	W				SC					
	W				GPL					
	W				D					
Execution	W				C					Input
Repeated	W				H					Sector
for each	W				R					Parameters
Sector	W				N					
	W	Data Transfer of N Bytes								82078 Formats and Writes Entire Track
Result	R				ST 0					
Phase	R				ST 1					
	R				ST 2					
	R				Undefined					
	R				Undefined					
	R				Undefined					
	R				Undefined					
INVALID										
Command	W				Invalid Codes					Invalid Command Codes (NoOp — 82078 goes into Standby State)
Result	R				ST 0					ST 0 = 80H

PARAMETER ABBREVIATIONS

Symbol — **Description**

AUTO PD — Auto powerdown control. If this bit is 0, then the automatic powerdown is disabled. If it is set to 1, then the automatic powerdown is enabled.

C — Cylinder address. The currently selected cylinder address, 0 to 255.

CLK48 — CLK48 = 1 indicates an external 48 MHz oscillator is being used.

CLK48 = 0 indicates a 24 MHz clock.

D0, D1, D2, D3 — Drive Select 0-3. Designates which drives are Perpendicular drives, a "1" indicating Perpendicular drive.

D — Data pattern. The pattern to be written in each sector data field during formatting.

DN — Done. This bit indicates that this is the last byte of the drive specification command. The 82078 checks to see if this bit is high or low. If it is low, it expects more bytes.

DN = 0 82078 expects more subsequent bytes.

DN = 1 Terminates the command phase and jumps to the results phase. An additional benefit is that by setting this bit high, a direct check of the current drive specifications can be done.

DIR — Direction control. If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.

DS0, DS1 — Disk Drive Select.

DS1	DS0	
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

DTL — Special sector size. By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.

DRATE1, DRATE0 — Data rate values from the DSR register.

DRT0, DRT1 — Data rate table select. These two bits select between the different data rate tables. The default is the conventional table. These also provide mapping of the data rates selected in the DSR and CCR. The mapped values are provided for read back by the system software are as shown in the DIR (in PS/2 Mode only). Table 6-2 shows this.

DT0, DT1 — Drive density select type. These bits select the outputs on DRVDEN0 and DRVDEN1 based on mode of operation that was selected via the IDENT1 and IDENT0 pins. More information is available in the Design Applications section.

Table 6-2. Data Rate Select Table

		Bits in DSR/CCR			Bits returned via DIR (Only available in PS/2)		
DRT0	**DRT1**	**DRATE0**	**DRATE1**	**Data Rate**	**DRATE0**	**DRATE1**	**Operation**
0	0	1	1	1 Mbps	1	1	Default
		0	0	500 Kbps	0	0	
		1	0	300 Kbps	1	0	
		0	1	250 Kbps	0	1	
0	1	1	1	1 Mbps	1	1	2 Mbps Tape Drive
		0	0	500 Kbps	0	0	
		1	0	2 Mbps	1	1	
		0	1	250 Kbps	0	1	
1	0			——RSVD——			RSVD
1	1	1	1	1 Mbps	1	1	Perpendicular mode FDDs
		0	0	500 Kbps	0	0	
		1	0	RSVD			
		0	1	250 Kbps	0	1	

EC — Enable Count. When this bit is "1" the "DTL" parameter of the Verify Command becomes SC (Number of sectors per track).

EFIFO — Enable FIFO. When this bit is 0, the FIFO is enabled. A "1" puts the 82078 in the 8272A compatible mode where the FIFO is disabled.

EIS — Enable implied seek. When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.

EOT — End of track. The final sector number of the current track.

EREG EN — Enhanced Register Enable.

EREG EN = 1 In PS/2 mode the TDR register is extended. In AT/EISA mode, the TDR register is extended and SRB is made visible to the user.

EREG EN = 0 Standard AT/EISA and PS/2 registers are used.

FDI TRI — Floppy Drive Interface Tri-state: If this bit is 0, then the output pins of the floppy disk drive interface are tri-stated. This is also the default state. If it is set to 1, then the floppy disk drive interface remains unchanged.

FD0, FD1 — Floppy drive select. These two bits select which physical drive is being specified. The FDn corresponds to FDSn and FDMEn on the floppy drive interface. The drive is selected independent of the BOOTSELn bits. Please refer to Section 2.1.1 which explains the distinction between physical drives and their virtual mapping as defined by the BOOTSEL1 and BOOTSEL0 bits.

FD0	**FD1**	**Drive Slot**
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

GAP — Alters Gap 2 length when using Perpendicular Mode.

GPL — Gap length. The gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).

HDS — Head address. Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.

HLT — Head load time. The time interval that 82078 waits after loading the head and before initiating a read or write operation. Refer to the SPECIFY command for actual delays.

HUT — Head unload time. The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the SPECIFY command for actual delays.

ISO — ISO Format: If this bit is set high the ISO format is used for all data transfer commands. When this bit is set low the normal IBM system 34 and perpendicular is used. The default is ISO = 0.

Lock — Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be reset to their default values by a "Software Reset" (Reset made by setting the proper bit in the DSR or DOR registers).

MFM — MFM mode. A one selects the double density (MFM) mode. A zero is reserved.

MIN DLY — Minimum power up time control. This bit is active only if AUTO PD bit is enabled. Setting this bit to a 0, assigns a 10 ms minimum power up time and setting this bit to a 1, assigns a 0.5 sec. minimum power up time (unless 2 Mbps, then 5 ms to 0.25 sec.).

MT — Multi-track selector. When set, this flag selects the multi-track operating mode. In this mode, the 82078 treats a complete cylinder, under head 0 and 1, as a single track. The 82078 operates as if this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the 82078 finishes operating on the last sector under head 0.

N — Sector size code. This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the users responsibility to not select combinations that are not possible with the drive.

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
—	—
07	16 Kbytes

NCN — New cylinder number. The desired cylinder number.

ND — Non-DMA mode flag. When set to 1, indicates that the 82078 is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the 82078 operates in DMA mode, interfacing to a DMA controller by means of the DRQ and DACK# signals.

NRP — No Results phase. When this bit is set high the result phase is skipped. When this bit is low the result phase will be generated.

OW — The bits denoted D0, D1, D2, and D3 of the PERPENDICULAR MODE command can only be overwritten when the OW bit is set to "1".

PCN — Present cylinder number. The current position of the head at the completion of SENSE INTERRUPT STATUS command.

PC2, PC1, PC0 — Precompensation values from the DSR register.

PDOSC — When this bit is set, the internal oscillator is turned off.

This may be done if using the external 48 MHz oscillator.

PS/2 STAT — PS/2 status. This bit is functional only in the PS/2 mode. In all other modes this bit will not have any effect. When set high this bit enables two bits (bits 5 and 6) in the DIR register to reflect the values of PD and IDLE respectively except when IDLEMSK (bit 4) is set. Default value is 0.

PTS — Precompensation table select. This bit selects whether to enable the precompensation value programmed in the DSR or not. In the default state, the value programmed in DSR will be used.

PTS = 0 DSR programmed precompensation delays.

PTS = 1 No precompensation delay is selected for the corresponding drive.

POLL — Polling disable. When set, the internal polling routine is disabled. When clear, polling is enabled.

PRETRK — Precompensation start track number. Programmable from track 00 to FFH.

R — Sector address. The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.

RCN — Relative cylinder number. Relative cylinder offset from present cylinder as used by the RELATIVE SEEK command.

SC — Number of sectors. The number of sectors to be initialized by the FORMAT command. The number of sectors to be verified during a Verify Command, when EC is set.

SEL3V# — SEL3V# = 1 indicates that the part is operating at 5.0V.

SEL3V# = 0 indicates that the part is operating at 3.3V.

SK — Skip flag. When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of READ DATA. If READ DELETED is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.

SRT — Step rate interval. The time interval between step pulses issued by the 82078. Programmable from 0.5 ms to 8 ms, in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.

ST0–3 — Status registers 0–3. Registers within the 82078 that store status information after a command has been executed. This status information is available to the host during the result phase after command execution.

STEPPING — These bits identify the stepping of the 82078.

WGATE — Write gate alters timing of WE, to allow for pre-erase loads in perpendicular drives.

6.1 Data Transfer Commands

All of the READ DATA, WRITE DATA and VERIFY type commands use the same parameter bytes and return the same results information. The only difference being the coding of bits 0–4 in the first byte.

An implied seek will be executed if the feature was enabled by the CONFIGURE command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a READ/WRITE DATA command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

6.1.1 READ DATA

A set of nine (9) bytes is required to place the 82078 into the Read Data Mode. After the READ DATA command has been issued, the 82078 loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the SPECIFY command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the 82078 reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one, and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the 82078 stops sending data, but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector terminate the READ DATA Command.

N determines the number of bytes per sector (see Table 6-3). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the 82078 transfers the specified number of bytes to the host. For reads, it continues to read the entire 128 byte sector and checks for CRC errors. For writes it completes the 128 byte sector by filling in zeroes. If N is not set to 00 Hex, DTL should be set to FF Hex, and has no impact on the number of bytes transferred.

Table 6-3. Sector Sizes

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
—	—
07	16 Kbytes

The amount of data which can be handled with a single command to the 82078 depends upon MT (multi-track) and N (Number of bytes/sector).

Table 6-4. Effects of MT and N Bits

MT	N	Max. Transfer Capacity	Final Sector Read from Disk
0	1	256 × 26 = 656	26 at side 0 or 1
1	1	256 × 52 = 13312	26 at side 1
0	2	512 × 15 = 7680	15 at side 0 or 1
1	2	512 × 30 = 15360	15 at side 1
0	3	1024 × 8 = 8192	8 at side 0 or 1
1	3	1024 × 16 = 16384	16 at side 1

The Multi-Track function (MT) allows the 82078 to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at the last sector of the same track at Side 1.

If the host terminates a read or write operation in the 82078, then the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 6-7. The termination must be normal.

At the completion of the READ DATA Command, the head is not unloaded until after the Head Unload Time Interval (specified in the SPECIFY command) has elapsed. If the host issues another command before the head unloads then the head settling time may be saved between subsequent reads.

If the 82078 detects a pulse on the INDX# pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the 82078 sets the IC code in Status Register 0 to "01" (Abnormal termination), and sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the READ DATA Command.

After reading the ID and Data Fields in each sector, the 82078 checks the CRC bytes. If a CRC error occurs in the ID or data field, the 82078 sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the READ DATA Command.

Table 6-5 describes the affect of the SK bit on the READ DATA command execution and results.

Table 6-5. Skip Bit vs READ DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	No	Normal Termination.
0	Deleted Data	Yes	Yes	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	Yes	No	Normal Termination.
1	Deleted Data	No	Yes	Normal Termination Sector Not Read ("Skipped").

Except where noted in Table 6-5, the C or R value of the sector address is automatically incremented (see Table 6-7).

6.1.2 READ DELETED DATA

This command is the same as the READ DATA command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 6-6 describes the affect of the SK bit on the READ DELETED DATA command execution and results.

Table 6-6. Skip Bit vs READ DELETED DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	Yes	Normal Termination.
0	Deleted Data	Yes	No	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	No	Yes	Normal Termination Sector Not Read ("Skipped").
1	Deleted Data	Yes	No	Normal Termination.

Except where noted in Table 6-6 above, the C or R value of the sector address is automatically incremented (see Table 6-7).

6.1.3 READ TRACK

This command is similar to the READ DATA command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the INDX# pin, the 82078 starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the 82078 finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The 82078 compares the ID information read from each sector with the specified value in the command, and sets the ND flag of Status Register 1 to a "1" if there is no comparison.

Multi-track or skip operations are not allowed with this command. The MT and SK bits (Bits D7 and D5 of the first command byte respectively) should always be set to "0".

Table 6-7. Result Phase Table

MT	Head	Final Sector Transferred to Host	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
1	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

This command terminates when the EOT specified number of sectors have been read. If the 82078 does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the INDX# pin, then it sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

6.1.4 WRITE DATA

After the WRITE DATA command has been issued, the 82078 loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the SPECIFY command), and begins reading ID Fields. When the sector address read from the diskette matches the sector address specified in the command, the 82078 reads the data from the host via the FIFO, and writes it to the sector's data field.

After writing data into the current sector, the 82078 computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the 82078 continues writing to the next data field. The 82078 continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeroes.

The 82078 reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID Fields, it sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the WRITE DATA command.

The WRITE DATA command operates in much the same manner as the READ DATA command. The following items are the same. Please refer to the READ DATA Command for details:

- Transfer Capacity
- (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command.
- Definition of DTL when N = 0 and when N does not = 0.

6.1.5 WRITE DELETED DATA

This command is almost the same as the WRITE DATA command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

6.1.6 VERIFY

The VERIFY command is used to verify the data stored on a disk. This command acts exactly like a READ DATA command except that no data is transferred to the host. Data is read from the disk, CRC computed and checked against the previously stored value.

Because no data is transferred to the host, TC (pin 25) cannot be used to terminate this command. By setting the EC bit to "1" an implicit TC will be issued to the 82078. This implicit TC will occur when the SC value has decrement to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0" DTL/SC should be programmed to 0FFH. Refer to Table 6-6 and Table 6-7 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 6-8. Verify Command Result Phase Table

MT	EC	SC/EOT Value	Termination Result
0	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

NOTE:
If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

6.1.7 FORMAT TRACK

The FORMAT command allows an entire track to be formatted. After a pulse from the INDX# pin is detected, the 82078 starts writing data on the disk including Gaps, Address Marks, ID Fields and Data Fields, per the IBM System 34 (MFM). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID Field for each sector is supplied by the host; that is, four data bytes per sector are needed by the 82078 for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the 82078 for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the 82078 encounters a pulse on the INDX# pin again and it terminates the command.

Table 6-9 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

Table 6-9. Typical PC-AT Values for Formatting

Drive Form	MEDIA	Sector Size	N	SC	GPL1	GPL2
5.25"	1.2M	512	02	0F	2A	50
	360K	512	02	09	2A	50
3.5"	2.88M	512	02	24	38	53
	1.44M	512	02	18	1B	54
	720K	512	02	09	1B	54

NOTE:
All values except Sector Size are in Hex.

Gap3 is programmable during reads, writes, and formats.

GPL1 = suggested Gap3 values in read and write commands to avoid splice point between data field and ID field of contiguous sections.

GPL2 = suggested Gap3 value in FORMAT TRACK command.

6.1.7.1 Format Fields

Table 6-10. System 34 Format Double Density

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		C	H	S	N	C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP 4b
80x	12x	3x	FC	50x	12x	3x	FE	Y	D	E	O	R	22x	12x	3x	FB		R		
4E	00	C2		4E	00	A1		L		C		C	4E	00	A1	F8		C		

Table 6-11. ISO Format

GAP 1	SYNC	IDAM		C	H	S	N	C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP 4b
32x	12x	3x	FE	Y	D	E	O	R	22x	12x	3x	FB		R		
4E	00	A1		L		C		C	4E	00	A1	F8		C		

Table 6-12. Perpendicular Format

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		C	H	S	N	C	GAP 2	SYNC	DATA AM		DATA	C	GAP 3	GAP 4b
80x	12x	3x	FC	50x	12x	3x	FE	Y	D	E	O	R	41x	12x	3x	FB		R		
4E	00	C2		4E	00	A1		L		C		C	4E	00	A1	F8		C		

6.2 Control Commands

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete; READ ID, RECALIBRATE and SEEK. The other control commands do not generate an interrupt.

6.2.1 READ ID

The READ ID command is used to find the present position of the recording heads. The 82078 stores the values from the first ID Field it is able to read into its registers. If the 82078 does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the INDX# pin, it then sets the IC code in Status Register 0 to "01" (Abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the SENSE INTERRUPT STATUS command. Otherwise, valuable interrupt status information will be lost.

6.2.2 RECALIBRATE

This command causes the read/write head within the 82078 to retract to the track 0 position. The 82078 clears the contents of the PCN counter, and checks the status of the TRK0 pin from the FDD. As long as the TRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the TRK0 pin goes high, the SE bit in Status Register 0 is set to "1", and the command is terminated. If the TRK0 pin is still low after 79 step pulses have been issued, the 82078 sets the SE and the EC bits of Status Register 0 to "1", and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one RECALIBRATE command to return the head back to physical Track 0.

The RECALIBRATE command does not have a result phase. SENSE INTERRUPT STATUS command must be issued after the RECALIBRATE command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the 82078 is in the BUSY state, but during the execution phase it is in a NON BUSY state. At this time another RECALIBRATE command may be issued, and in this manner, parallel RECALIBRATE operations may be done on up to 4 drives at once.

Upon power up, the software must issue a RECALIBRATE command to properly initialize all drives and the controller.

6.2.3 DRIVE SPECIFICATION COMMAND

The 82078 uses two pins, DRVDEN0 and DRVDEN1 to select the density for modern drives. These signals inform the drive of the type of diskette in the drive. The Drive Specification command specifies the polarity of the DRVDEN0 and DRVDEN1 pins. It also enables or disables DSR programmed precompensation.

This command removes the need for a hardware workaround to accommodate differing specifications among drives. By programming this command during BIOS's POST routine, the floppy disk controller will internally configure the correct values for DRVDEN0 and DRVDEN1 with corresponding precompensation value and data rate table enabled for the particular type of drive.

This command is protected from software resets. After executing the DRIVE SPEC command, subsequent software resets will not clear the programmed parameters. Only another DRIVE SPEC command or H/W reset can reset it to default values. The 6 LSBs of the last byte of this command are reserved for future use.

The DRATE0 and DRATE1 are values as programmed in the DSR register. The DENSEL is high for high data rates (1 Mbps and 500 Kbps) and low for low data rates (300 Kbps and 250 Kbps).

Table 6-13 describes the drives that are supported with the DT0, DT1 bits of the Drive Specification command:

Table 6-13. Drive Support via the Drive Specification Command

DRVDENn Polarities for AT/EISA Mode (IDENT0, IDENT1 = 11)

DT0	DT1	Data Rate	DRVDEN0	DRVDEN1
0*	0*	1 Mbps	1	1
		500 Kbps	1	0
		300 Kbps	0	1
		250 Kbps	0	0
0	1	1 Mbps	1	1
		500 Kbps	0	0
		300 Kbps	0	1
		250 Kbps	1	0
1	0	1 Mbps	0	1
		500 Kbps	0	0
		300 Kbps	1	1
		250 Kbps	1	0
1	1	1 Mbps	1	1
		500 Kbps	0	0
		300 Kbps	1	0
		250 Kbps	0	1

(*) Denotes the default setting

DRVDEN Polarities for PS/2, Model 30 Mode (IDENT0, IDENT1 = 0X)

DT0	DT1	Data Rate	DRVDEN0	DRVDEN1
0*	0*	1 Mbps	1	1
		500 Kbps	0	0
		300 Kbps	1	0
		250 Kbps	0	1
0	1	1 Mbps	1	1
		500 Kbps	1	0
		300 Kbps	0	1
		250 Kbps	0	0
1	0	1 Mbps	0	1
		500 Kbps	0	0
		300 Kbps	1	1
		250 Kbps	1	0
1	1	1 Mbps	1	1
		500 Kbps	0	0
		300 Kbps	0	1
		250 Kbps	1	0

(*) Denotes the default setting

6.2.4 SEEK

The read/write head within the drive is moved from track to track under the control of the SEEK Command. The 82078 compares the PCN which is the current head position with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in), and issues step pulses.

PCN > NCN: Direction signal to drive set to "0" (step out), and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN, then the SE bit in Status Register 0 is set to "1", and the command is terminated.

During the command phase of the seek or recalibrate operation, the 82078 is in the BUSY state, but during the execution phase it is in the NON BUSY state.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1. SEEK command; Step to the proper track
2. SENSE INTERRUPT STATUS command; Terminate the Seek command
3. READ ID. Verify head is on proper track
4. Issue READ/WRITE command.

The SEEK command does not have a result phase. Therefore, it is highly recommended that the SENSE INTERRUPT STATUS Command be issued after the SEEK command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return a "0". When exiting DSR POWERDOWN mode, the 82078 clears the PCN value and the status information to zero. Prior to issuing the DSR POWERDOWN command, it is highly recommended that the user service all pending interrupts through the SENSE INTERRUPT STATUS command.

6.2.5 SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6-9 shows the status of bits SH and SN under various conditions of SCAN.

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector has been encountered.

When either the STP (contiguous sectors STP = 01, or alternate sectors STP = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 13 μs. If an Overrun occurs the FDC terminates the command.

Table 6-13. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \not> D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} \not< D_{Processor}$

6.2.6 SENSE INTERRUPT STATUS

An interrupt signal on INT pin is generated by the 82078 for one of the following reasons:

1. Upon entering the Result Phase of:
   a. READ DATA Command
   b. READ TRACK Command
   c. READ ID Command
   d. READ DELETED DATA Command
   e. WRITE DATA Command
   f. FORMAT TRACK Command
   g. WRITE DELETED DATA Command
   h. VERIFY Command
2. End of SEEK, RELATIVE SEEK or RECALIBRATE Command
3. 82078 requires a data transfer during the execution phase in the non-DMA Mode

The SENSE INTERRUPT STATUS command resets the interrupt signal and via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt. If a SENSE INTERRUPT STATUS command is issued when no active interrupt condition is present, the status register ST0 will return a value of 80H (invalid command).

Table 6-14. Interrupt Identification

SE	IC	Interrupt Due To
0	11	Polling
1	00	Normal Termination of SEEK or RECALIBRATE command
1	01	Abnormal Termination of SEEK or RECALIBRATE command

The SEEK, RELATIVE SEEK and the RECALIBRATE commands have no result phase. SENSE INTERRUPT STATUS command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a SENSE INTERRUPT STATUS is not issued, the drive will continue to be BUSY and may effect the operation of the next command.

6.2.7 SENSE DRIVE STATUS

SENSE DRIVE STATUS obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. STATUS REGISTER 3 contains the drive status information.

6.2.8 SPECIFY

The SPECIFY command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between the command phase to the execution phase of a read/write data command. The Head Unload Time (HUT) timer starts at the end of the execution phase to the beginning of the result phase of a read/write command. The values change with the data rate speed selection and are documented in Table 6-15.

Table 6-15. Drive Control Delays (ms)

	HUT				SRT			
	1M	500K	300K	250K	1M	500K	300K	250K
0	128	256	426	512	8.0	16	26.7	32
1	8	16	26.7	32	7.5	15	25	30
—	—	—	—	—	—	—	—	—
A	80	160	267	320	3.0	6.0	10.2	12
B	88	176	294	352	2.5	5.0	8.35	10
C	96	192	320	384	2.0	4.0	6.68	8
D	104	208	346	416	1.5	3.0	5.01	6
E	112	224	373	448	1.0	2.0	3.33	4
F	120	240	400	480	0.5	1.0	1.67	2

HLT				
	1M	500K	300K	250K
00	128	256	426	512
01	1	2	3.3	4
02	2	4	6.7	8
—	—	—	—	—
7E	126	252	420	504
7F	127	254	423	508

The choice of DMA or NON-DMA operations is made by the ND bit. When this bit is "1", the NON-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signalled by the DRQ pin. Non-DMA mode uses the RQM bit and the INT pin to signal data transfers.

6.2.9 CONFIGURE

Issue the configure command to enable features like the programmable FIFO and set the beginning track for pre-compensation. A CONFIGURE command need not be issued if the default values of the 82078 meet the system requirements. The CLK48 bit allows the 82078 to connect to a 48 MHz oscillator, this can reduce board space if there is a 48 MHz signal already available on the system.

CONFIGURE DEFAULT VALUES:

EIS — No Implied Seeks
EFIFO — FIFO Disabled
POLL — Polling Enabled
FIFOTHR — FIFO Threshold Set to 1 Byte
PRETRK — Pre-Compensation Set to Track 0

EIS—Enable implied seek. When set to "1", the 82078 will perform a SEEK operation before executing a read or write command. Defaults to no implied seek.

EFIFO—A "1" puts the FIFO into the 8272A compatible mode where the FIFO is disabled. This means data transfers are asked for on a byte by byte basis. Defaults to "1", FIFO disabled. The threshold defaults to one.

POLL—Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a RESET. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR—The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 byte to 16 bytes. Defaults to one byte. A "00" selects one byte, "0F" selects 16 bytes.

PRETRK—Pre-compensation start track number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0, "FF" selects 255.

CLK48—Default is "0", external clock is assumed to be 24 MHz. If a 48 MHz external oscillator is used the bit must be set high. Note that the 82078 does not support a 48 MHz crystal, only an external oscillator. Note, this must be enabled first during the initialization routine of the POST if a 48 MHz oscillator is used.

6.2.10 VERSION

The VERSION command checks to see if the controller is an enhanced type (82077, 82077AA, 82077SL) or the older type (8272A/765A). A value of 90H is returned as the result byte, defining an enhanced FDD controller is in use. No interrupts are generated.

6.2.11 RELATIVE SEEK

The command is coded the same as for SEEK, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control.

DIR	Action
0	Step Head Out
1	Step Head In

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The RELATIVE SEEK command differs from the SEEK command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The SEEK command is good for drives that support a maximum of 256 tracks. RELATIVE SEEKs cannot be overlapped with other RELATIVE SEEKs. Only one RELATIVE SEEK can be active at a time. Bit 4 of Status Register 0 (EC) will be set if RELATIVE SEEK attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks and that the host needs to read track 300 and the head is on any track (0–255). If a SEEK

command was issued, the head would stop at track 255. If a RELATIVE SEEK command was issued, the 82078 would move the head the specified number of tracks, regardless of the internal cylinder position register (but would increment the register). If the head had been on track 40 (D), the maximum track that the 82078 could position the head on using RELATIVE SEEK, would be 296 (D), the initial track, +256 (D). The maximum count that the head can be moved with a single RELATIVE SEEK command is 256 (D).

The internal register, PCN, would overflow as the cylinder number crossed track 255 and would contain 40 (D). The resulting PCN value is thus (NCN + PCN) mod 256. Functionally, the 82078 starts counting from 0 again as the track number goes above 255(D). It is the users responsibility to compensate 82078 functions (precompensation track number) when accessing tracks greater than 255. The 82078 does not keep track that it is working in an "extended track area" (greater than 255). Any command issued would use the current PCN value except for the RECALIBRATE command which only looks for the TRACK0 signal. RECALIBRATE would return an error if the head was farther than 79 due to its limitation of issuing a maximum 80 step pulses. The user simply needs to issue a second RECALIBRATE command. The SEEK command and implied seeks will function correctly within the 44 (D) track (299–255) area of the "extended track area". It is the users responsibility not to issue a new track position that would exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0–255) of tracks, a RELATIVE SEEK would be issued to cross the track 255 boundary.

A RELATIVE SEEK can be used instead of the normal SEEK but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a READ ID command to ensure that the head is physically on the track that software assumes it to be. Different 82078 commands will return different cylinder results which may be difficult to keep track of with software without the READ ID command.

6.2.12 DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. The command returns pertinent information regarding the internal status of the 82078. This can be used to verify the values initialized in the 82078.

2

6.2.13 PERPENDICULAR MODE COMMAND

6.2.13.1 About Perpendicular Recording Mode

An added capability of the 82078 is the ability to interface directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method by orienting the magnetic bits vertically. This scheme packs in more data bits for the same area.

6.2.13.2 The Perpendicular Mode Command

The PERPENDICULAR MODE Command allows the system designers to designate specific drives as

Table 6-16. Effects of WGATE and GAP Bits

GAP	WGATE	MODE	VCO Low Time after Index Pulse	Length of Gap2 Format Field	Portion of Gap2 Written by Write Data Operation	Gap2 VCO Low Time for Read Operations
0	0	Conventional Mode	33 Bytes	22 Bytes	0 Bytes	24 Bytes
0	1	Perpendicular Mode (500 Kbps Data Rate)	33 Bytes	22 Bytes	19 Bytes	24 Bytes
1	0	Reserved (Conventional)	33 Bytes	22 Bytes	0 Bytes	24 Bytes
1	1	Perpendicular Mode (1 Mbps Data Rate)	18 Bytes	41 Bytes	38 Bytes	43 Bytes

NOTE:
When either GAP or WGATE bit is set, the current value of precompensation in the DSR is used.

Perpendicular recording drives. Data transfers between Conventional and Perpendicular drives are allowed without having to issue PERPENDICULAR MODE commands between the accesses of the two different drives, nor having to change write pre-compensation values.

With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 6-16 describes the effects of the WGATE and GAP bits for the PERPENDICULAR MODE command.

When both GAP and WGATE equal "0" the PERPENDICULAR MODE command will have the following effect on the 82078: 1) If any of the new bits D0, D1, D2, and D3 are programmed to "1" the corresponding drive will automatically be programmed for Perpendicular mode (i.e.: GAP2 being written during a write operation, the programmed Data Rate will determine the length of GAP2), and data will be written with 0 ns write pre-compensation. 2) any of the new bits (D0–D3) that are programmed for "0" the designated drive will be programmed for Conventional Mode and data will be written with the currently programmed write pre-compensation value. 3) Bits D0, D1, D2, and D3 can only be over written when the OW bit is written as a "1". The status of these bits can be determined by interpreting the eighth result byte of the DUMPREG Command. (Note: if either the GAP or WGATE bit is a "1", then bits D0–D3 are ignored.)

"Software" and "Hardware" RESET will have the following effects on the enhanced PERPENDICULAR MODE command:

1. "Software" RESETs (Reset via DOR or DSR registers) will only clear GAP and WGATE bits to "0", D3, D2, D1, and D0 will retain their previously programmed values.
2. "Hardware" RESETs (Reset via pin 32) will clear all bits (GAP, WGATE, D0, D1, D2, and D3) to "0" (All Drives Conventional Mode).

6.2.14 POWERDOWN MODE COMMAND

The POWERDOWN MODE command allows the automatic power management and enables the enhanced registers (EREG EN) of the 82078. The use of the command can extend the battery life in portable PC applications. To enable auto powerdown the command may be issued during the BIOS power on self test (POST).

This command includes the ability to configure the 82078 into the enhanced AT/EISA and PS/2 mode. In the enhanced PS/2 and Model 30 modes, this makes the PD and IDLE pin status visible in the DIR register. In the enhanced AT/EISA modes, this command extends the SRB and TDR register. These extended registers accommodate bits that give more information about floppy drive interface, allow for boot drive selection, and identify the values of the PD and IDLE status.

As soon as the command is enabled, a 10 ms or a 0.5 sec. (5 ms or 0.25 with 2Mbps tape mode) minimum powerup timer is initiated depending on whether the MIN DLY bit is set to 0 or 1. This timer is one of the required conditions that has to be satisfied before the part will enter auto powerdown. Any software reset will reinitialize the timer. The timer countdown is also extended by up to 10 ms if the data rate is changed during the timer's countdown. Without this timer 82078 would have been put to sleep immediately after 82078 is idle. The minimum delay gives software a chance to interact with 82078 without incurring an additional overhead due to recovery time.

The command also allows the output pins of floppy disk drive interface to be tri-stated or left unaltered during auto powerdown. This is done by the FDI TRI bit. In the default condition (FDI TRI = 0) the output pins of the floppy disk drive are tri-stated. Setting this bit leaves the interface unchanged from the normal state.

The results phase returns the values programmed for MIN DLY, FDI TRI and AUTO PD. The auto powerdown mode is disabled by a hardware reset. Software results have no effect on the POWERDOWN MODE command parameters.

6.2.15 PART ID COMMAND

This command can be used to identify the floppy disk controller as an enhanced controller. The first stepping of both versions of the 64 pin 82078 will yield 0x01 in the result phase of this command. Any future enhancements on these parts will be denoted by the 5 LSBs (0x01 to 0x1F).

6.2.16 OPTION COMMAND

The standard IBM format includes an index address field consisting of 80 bytes of GAP 4a, 12 bytes of the sync field, four bytes identifying the IAM and 50 bytes of GAP 1. Under the ISO format most of this preamble is not used. The ISO format allows only 32 bytes of GAP 1 after the index mark. The ISO bit in this command allows the 82078 to configure the data transfer commands to recognize this format. The MSBs in this command are reserved for any other enhancements made available to the user in the future.

6.2.17 SAVE COMMAND

The first byte corresponds to the values programmed in the DSR with the exception of CLK48. The DRATE1, DRATE0 used here are unmapped. The second byte is used for configuring the bits from the OPTION command. All future enhancements to the OPTION command will be reflected in this byte as well. The next nine result bytes are explained in the Parameter Abbreviations section after the command summary. The 13th byte is the value associated with the auto powerdown command. The disk status is used internally by 82078. There are two reserved bytes at the end of this command for future use.

This command is similar to the DUMPREG command but it additionally allows the user to read back the precompensation values as well as the programmed data rate. It also allows the user to read the values programmed in the auto powerdown command. The precompensation values will be returned as programmed in the DSR register. This command is used in conjunction with the Restore command should prove very useful for SMM power management. This command reserves the last two bytes for future enhancements.

6.2.18 RESTORE COMMAND

Using Restore with the Save command, allows the SMM power management to restore the 82078 to its original state after a system powerdown. It also serves as a succinct way to provide most of the initialization requirements normally handled by the system. The sequence of initializing the 82078 after a reset occurred and assuming a Save command was issued follows:

- Issue the Drive Spec command (if the design utilizes this command)
- Issue the Restore command (pass the 16 bytes retrieved previously during SAVE)

The Restore command will program the data rate and precompensation value via the DSR. It then restores the values normally programmed through the Configure, Specify, and Perpendicular commands. It also enables the previously selected values for the AUTO Powerdown command. The PCN values are set restored to their previous values and the user is responsible for issuing the seek and recalibrate commands to restore the head to the proper location. There are some drives that do not recalibrate in which case the Restore command will restore the previous state completely. The PDOSC bit is retrievable using the Save command, however, the system designer must set it correctly. The software must allow at least 20 μs to execute the Restore command. When using the BOOTSEL bits in the TDR, the user must restore or reinitialize these bits to their proper values.

6.2.19 FORMAT AND WRITE COMMAND

The format and write command is capable of simultaneously formatting and writing data to the diskette. It is essentially the same as the normal format command. With the exception that included in the execution for each sector is not only the C, H, R, and N but also the data transfer of N bytes. The D value is ignored. This command formats the entire track. High speed floppy diskette duplication can be done fast and efficiently with this command. The user can format the diskette and put data on it in a single pass. This is very useful for software duplication applications by reducing the time required to format and copy diskettes.

6.2.20 LOCK

The LOCK command is included to protect a system with long DMA latencies against older application software packages that can disable the 82078's FIFO.

NOTE:
This command should only be used by the system's FDC routines, and ISVs (Independent Software Vendors) should refrain from using it. If an ISV's application calls for having the 82078 FIFO disabled a CONFIGURE Command should be used to toggle the EFIFO (Enable FIFO) bit. ISV can determine the value of the LOCK bit by interpreting the eighth result byte of an DUMPREG Command.

The LOCK command defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to a "1" all subsequent "software" RESETs by the DOR and DSR registers will not change the previously set parameter values in the CONFIGURE command. When the LOCK bit is set to a "0" 'software" RESETs by the DOR or DSR registers will return these parameters to their default values. All "hardware" Resets will set the LOCK bit to a "0" value, and will return EFIFO, FIFOTHR, and PRETRK to their default values. A Status byte is returned immediately after issuing the command byte. This Status byte reflects the value of the Lock bit set by the command byte.

NOTE:
No interrupts are generated at the end of this command.

7.0 STATUS REGISTER ENCODING

The contents of these registers are available only through a command sequence.

7.1 Status Register 0

Bit No.	Symbol	Name	Description
7, 6	IC	Interrupt Code	00—Normal termination of command. The specified command was properly executed and completed without error. 01—Abnormal termination of command. Command execution was started, but was not successfully completed. 10—Invalid command. The requested command could not be executed. 11—Abnormal termination caused by Polling.
5	SE	Seek End	The 82078 completed a SEEK or RECALIBRATE command, or a READ or WRITE with implied seek command.
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the RECALIBRATE command. 2. The RELATIVE SEEK command causes the 82078 to step outward beyond Track 0.
3	—	—	Unused. This bit is always "0".
2	H	Head Address	The current head address.
1, 0	DS1, 0	Drive Select	The current selected drive.

7.2 Status Register 1

Bit No.	Symbol	Name	Description
7	EN	End of Cylinder	The 82078 tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data Command.
6	—	—	Unused. This bit is always "0".
5	DE	Data Error	The 82078 detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the 82078 does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3	—	—	Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. READ DATA, READ DELETED DATA command, the 82078 did not find the specified sector. 2. READ ID command, the 82078 cannot read the ID field without an error. 3. READ TRACK command, the 82078 cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the 82078 is executing a WRITE DATA, WRITE DELETED DATA, or FORMAT TRACK command.
0	MA	Missing Address Mark	Any one of the following: 1. The 82078 did not detect an ID address mark at the specified track after encountering the index pulse from the INDX# pin twice. 2. The 82078 cannot detect a data address mark or a deleted data address mark on the specified track.

7.3 Status Register 2

Bit No.	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: 1. READ DATA command, the 82078 encounters a deleted data address mark. 2. READ DELETED DATA command, the 82078 encountered a data address mark.
5	DD	Data Error in Data Field	The 82078 detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82078.
3	—	—	Unused. This bit is always "0".
2	—	—	Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82078 and is equal to FF hex which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The 82078 cannot detect a data address mark or a deleted data address mark.

7.4 Status Register 3

Bit No.	Symbol	Name	Description
7	—	—	Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5	—	—	Unused. This bit is always "1".
4	T0	TRACK 0	Indicates the status of the TRK0 pin.
3	—	—	Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1, 0	DS1, 0	Drive Select	Indicates the status of the DS1, DS0 pins.

8.0 COMPATIBILITY

The 82078 was designed with software compatibility in mind. It is a fully backwards compatible solution with the older generation 8272A and NEC765A/B disk controllers. The 82078 also implements on-board registers for compatibility with the Personal System/2s as well as PC/AT and PC/XT floppy disk controller subsystems. The 82078 is fully compatible with Intel's 386/486SL Microprocessor Superset. Upon reset, the 82078 samples IDENT0 and IDENT1 to determine PS/2, PC/AT or PS/2 Model 30 mode.

8.1 PS/2 vs AT vs Model 30 Mode

The 82078 operates in three different modes: PS/2, PC/AT, and Model 30. The 82078 is placed into the proper mode of operations upon Hardware RESET with the appropriate settings of the IDENT0 and IDENT1 pins.

8.2 Compatibility with the FIFO

The FIFO of the 82078 is designed to be transparent to non-FIFO disk controller software developed on the older generation 8272A standard. Operation of the 82078 FIFO can be broken down into two tiers of compatibility. For first tier compatibility, the FIFO is left in the default disabled condition upon a "Hardware" reset. In this mode the FIFO operates in a byte mode and provides complete compability with non-FIFO based software. For second tier compatibility, the FIFO is enabled via the CONFIGURE command. When the FIFO is enabled, it will temporarily enter a byte mode during the command and result phase of disk controller operation. This allows for compatible operation when interrogating the Main Status Register (MSR) for the purpose of transferring a byte at a time to or from the disk controller. For normal disk controller applications, the system designer can still take advantage of the FIFO for time critical data transfers during the execution phase and not create any conflicts with non-FIFO software during the command or result phase.

In some instances, use of the FIFO in any form has conflicted with certain specialized software. An example of a compatibility conflict using the FIFO is with software that monitors the progress of a data transfer during the execution phase. If the software assumed the disk controller was operating in a single byte mode and counted the number of bytes transferred to or from the disk controller to trigger some time dependent event on the disk media (i.e., head position over a specific data field), the same software will not have an identical time relationship if the FIFO is enabled. This is because the FIFO allows data to be queued up, and then burst transferred across the host bus. To accommodate software of this type, it is recommended that the FIFO be disabled.

8.3 Drive Polling

The 82078 supports the polling mode of the older generation 8272A. This mode is enabled upon a reset and can be disabled via the CONFIGURE command. This mode is supported for the sole purpose of providing backward compatibility with software that expects its presence.

The intended purpose of drive polling dates back to 8" drives as a means to monitor any change in status for each disk drive present in the system. Each of the drives is selected for a period of time and its READY signal sampled. After a delay, the next drive is selected. Since the 82078 does not support READY in this capacity (internally tied true), the polling sequence is only simulated and does not affect the drive select lines (DS0–DS3) when it is active. If enabled, it occurs whenever the 82078 is waiting for a command or during SEEKs and RECALIBRATEs (but not IMPLIED SEEKs). Each drive is assumed to be not ready after a reset and a "ready" value for each drive is saved in an internal register as the simulated drive is polled. An interrupt will be generated on the first polling loop because of the initial "not ready" status. This interrupt must be followed with a SENSE INTERRUPT STATUS command from the host to clear the interrupt condition for each of the four logical drives.

9.0 Programming Guidelines

Programming the 82078 is identical to any other 8272A compatible disk controller with the exception of some additional commands. For the new designer, it is useful to provide some guidelines on how to program the 82078. A typical disk operation involves more than issuing a command and waiting for the results. The control of the floppy disk drive is a low level operation that requires software intervention at different stages. New commands and features have been added to the 82078 to reduce the complexity of this software interface.

9.1 Command and Result Phase Handshaking

Before a command or parameter byte can be issued to the 82078, the Main Status Register (MSR) must be interrogated for a ready status and proper FIFO direction. A typical floppy controller device driver should contain a subroutine for sending command or

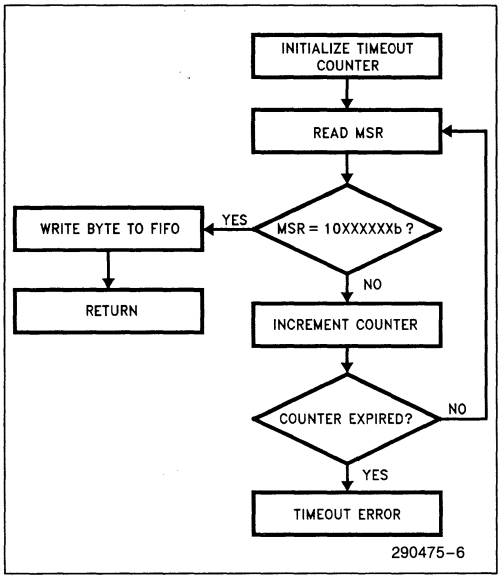


Figure 9-1. Send_Byte Routine

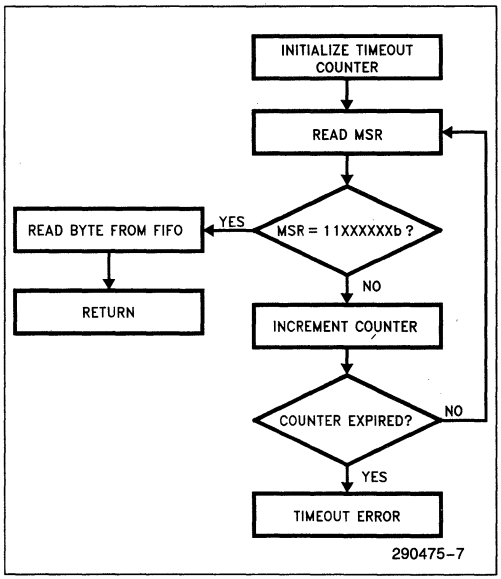


Figure 9-2. Get_Byte Routine

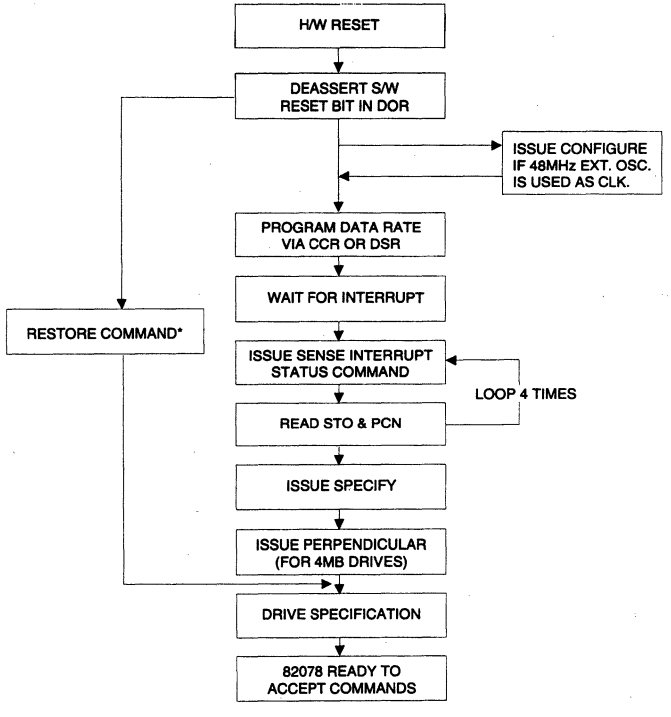
parameter bytes. For this discussion, the routine will be called "Send_byte" with the flowchart shown in Figure 9-1.

The routine loops until RQM is 1 and DIO is 0 indicating a ready status and FIFO direction is inward. If this condition is true, the 82078 is ready to accept a command or parameter byte. A timeout counter is used to insure software response within a reasonable amount of time in case of no response by the 82078. As a note, the programmer must be careful how the maximum delay is chosen to avoid unnecessary timeouts. For example, if a new command is issued when the 82078 is in the middle of a polling routine, the MSR will not indicate a ready status for the next parameter byte until the polling sequence completes the loop. This could cause a delay between the first and second bytes of up to 250 μs (@ 250 Kbps). If polling is disabled, this maximum delay is 175 μs. There should also be enough timeout margin to accommodate a shift of the software to a higher speed system. A timeout value that results in satisfactory operation on a 16 MHz CPU might fail when the software is moved to a system with a 25 MHz CPU. A recommended solution is to derive the timeout counter from a system hardware counter that is fixed in frequency from CPU clock to CPU clock.

For reading result bytes from the 82078, a similar routine is used. Figure 9-2 illustrates the flowchart for the routine "Get_byte". The MSR is polled until RQM is 1 and DIO is 1, which indicates a ready status and outward FIFO direction. At this point, the host can read a byte from the FIFO. As in the Send_byte routine, a timeout counter should be incorporated in case of a disk controller lock-up condition. For example, if a disk was not inserted into the disk drive at the time of a read operation, the controller would fail to receive the index pulse and lock-up since the index pulses are required for termination of the execution phase.

9.2 Initialization

Initializing the 82078 involves setting up the appropriate configuration after a reset. Parameters set by the SPECIFY command are undefined after a system reset and will need to be reinitialized. CONFIGURE command parameters default to a known state after a system reset but will need to be reinitialized if the system requirements are different from the default settings. This can be accomplished in two ways, either issue the individual commands, or issue the Restore command (assuming the Save command was issued). The Restore command is a succinct way to initialize the 82078, this is the preferable method if the system power management powers the 82078 on and off frequently. The flowchart for the recommended initialization sequence of the 82078 is shown in Figure 9-3.



*Sense Interrupt Status may be required if Restore CMD is not issued within 250 μs of trailing edge of H/W reset (@1 Mbps).

Figure 9-3. Initialization Flowchart

Following a reset of the 82078, the Configuration Control Register (CCR) should be reinitialized for the appropriate data rate. An external reset via the RESET pin will cause the data rate and write precompensation values to default to 250 Kbps (10b) and 125 ns (000b) respectively. Since the 125 ns write precompensation value is optimal for the 5 ¼" and 3 ½" disk drive environment, most applications will not require the value to be changed in the initialization sequence. As a note, a software reset issued via the DOR or DSR will not affect the data rate or write precompensation values. But it is recommended as a safe programming practice to always program the data rate after a reset, regardless of the type.

Since polling is enabled after a reset of the 82078, four SENSE INTERRUPT STATUS commands need to be issued afterwards to clear the status flags for each drive. The flowchart in Figure 9-3 illustrates how the software clears each of the four interrupt status flags internally queued by the 82078. It should be noted that although four SENSE INTERRUPT STATUS commands are issued, the INT pin is only active until the first SENSE INTERRUPT STATUS command is executed.

As a note, if the CONFIGURE command is issued within 250 μs of the trailing edge of reset (@1 Mbps), the polling mode of the 82078 can be disabled before the polling initiated interrupt occurs. Since polling stops when the 82078 enters the command phase, it is only time critical up to the first byte of the CONFIGURE command. If disabled in time, the system software no longer needs to issue the four SENSE INTERRUPT STATUS commands to clear the internal interrupt flags normally caused by polling.

The CONFIGURE command should also be issued if the system requirements are different from the default settings. For example, the CONFIGURE command can be used to enable the FIFO, set the threshold, and enable Implied Seeks.

The non-DMA mode flag, step rate (SRT), head load (HLT), and head unload times (HUT) programmed by the SPECIFY command do not default to a known state after a reset. This behavior is consistent with the 8272A and has been preserved here for compatibility. Thus, it is necessary to always issue a SPECIFY command in the initialization routine.

9.3 Recalibrates and Seeks

Commands that position the disk head are different from the typical READ/WRITE/FORMAT command in the sense that there is no result phase. Once a RECALIBRATE, SEEK, or RELATIVE SEEK command has been issued, the 82078 will return a ready status in the Main Status Register (MSR) and perform the head positioning operation as a background task. When the seek is complete, the 82078 will assert the INT signal to request service. A SENSE INTERRUPT STATUS command should then be asserted to clear the interrupt and read the status of the operation. Since the drive and motor enable signals are directly controlled through the Digital Output Register (DOR) on the 82078, a write to the DOR will need to precede the RECALIBRATE or SEEK command if the drive and motor is not already enabled. Figure 9-4 shows the flow chart for this operation.

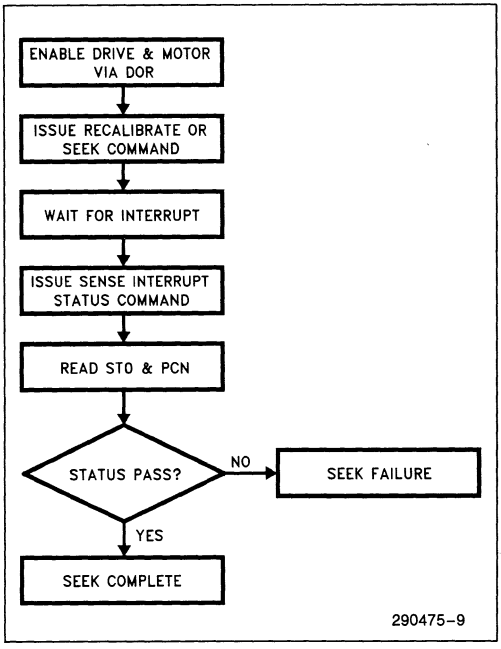


Figure 9-4. Recalibrate and Seek Operations

9.4 Read/Write Data Operations

A read or write data operation requires several steps to complete successfully. The motor needs to be turned on, the head positioned to the correct cylinder, the DMA controller initialized, the read or write command initiated, and an error recovery scheme implemented. The flowchart in Figure 9-5 highlights a recommended algorithm for performing a read or write data operation.

Before data can be transferred to or from the diskette, the disk drive motor must be brought up to speed. For most 3½" disk drives, the spin-up time is 300 ms, while the 5¼" drive usually requires about 500 ms due to the increased moment of inertia associated with the larger diameter diskette.

One technique for minimizing the motor spin-up delay in the read data case is to begin the read operation immediately after the motor is turned on. When the motor is not initially up to speed, the internal data separator will fail to lock onto the incoming data stream and report a failure in the status registers. The read operation is then repeated until successful status is obtained. There is no risk of a data integrity problem since the data field is CRC validated. But, it is not recommended to use this technique for the write data operation even though it requires successful reading of the ID field before the write takes place. The data separator performance of the 82078 is such that locking to the data stream could take place while the motor speed variation is still significant. This could result in errors when an attempt is made to read the disk media by other disk controllers that have a narrower incoming data stream frequency bandwidth.

After the motor has been turned on, the matching data rate for the media inserted into the disk drive should then be programmed to the 82078 via the Configuration Control Register (CCR). The 82078 is designed to allow a different data rate to be programmed arbitrarily without disrupting the integrity of the device. In some applications, it is required to automatically determine the recorded data rate of the inserted media. One technique for doing this is to perform a READ ID operation at each available data rate until a successful status is returned in the result phase.

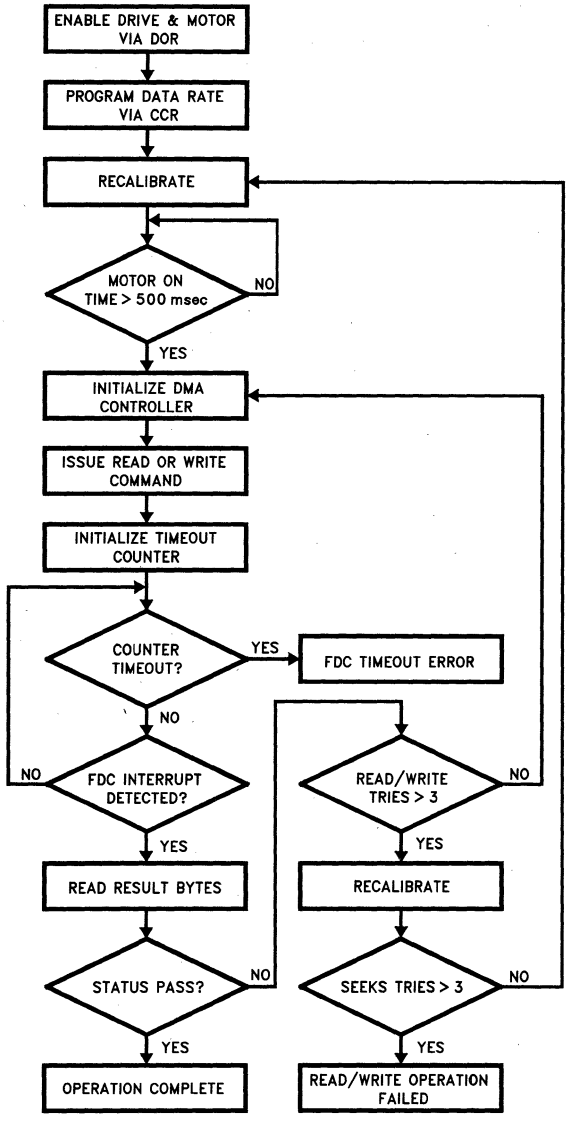


Figure 9-5. Read/Write Operation

If implied seeks are not enabled, the disk drive head must be positioned over the correct cylinder by executing a SEEK command. After the seek is complete, a head settling time needs to be asserted before the read or write operation begins. For most drives, this delay should be a minimum of 15 ms. When using implied seeks, the minimum head settling time can be enforced by the head load time (HLT) parameter designated in the SPECIFY command. For example, a HLT value of 8 will yield an effective head settling time of 16 ms for a programmed data rate of 500 Kbps. Of course if the head is already positioned over the correct cylinder, the head settling time does not need to be enforced.

The DMA controller is then initialized for the data transfer and the read or write command is executed. Typically the DMA controller will assert Terminal Count (TC) when the data transfer is complete. The 82078 will then complete the current data transfer and assert the INT signal signifying it has entered the result phase. The result phase can also be entered by the 82078 if an error is encountered or the last sector number equals the End of Track (EOT) parameter.

Based on the algorithm in Figure 9-5, if an error is encountered after reading the result bytes, two more retries are performed by reinitializing the DMA controller and re-issuing the read or write data command. A persisting failure could indicate the seek operation did not achieve proper alignment between the head and the track. The disk head should then be recalibrated and the seek repeated for a maximum of two more tries. Unsuccessful operation after this point should be reported as a disk failure to the operating system.

9.5 Formatting

The disk formatting procedure involves positioning the head on each track and creating a fixed format field used for organizing the data fields. The flowchart in Figure 9-6 highlights the typical format procedure.

After the motor has been turned on and the correct data rate programmed, the disk head is recalibrated to track 0. The disk is then allowed to come up to speed via a 500 ms delay. It is important the disk speed has stabilized before the actual formatting to avoid any data rate frequency variations. Since the format fields contain critical information used by the data separator of the disk controller for synchronization purposes, frequency stability of the data stream is imperative for media interchangeability among different systems.

The ID field data created on the disk during the format process is provided by the DMA controller during the execution phase. The DMA controller is initialized to send the C, H, R and N values for each sector ID field. For example, to format cylinder 7, on head 1, with 9 sectors, and a sector size of 2 (512 bytes), the DMA controller should be programmed to transfer 36 bytes (9 sectors × 4 bytes per sector) with the following data field: 7,1,1,2, 7,1,2,2, 7,1,3,2, ... 7,1,9,2. Since the values provided to the 82078 during the execution phase of the format command are directly recorded as the ID fields on the disk, the data contents can be arbitrary. Some forms of copy protection have been implemented by taking advantage of this capability.

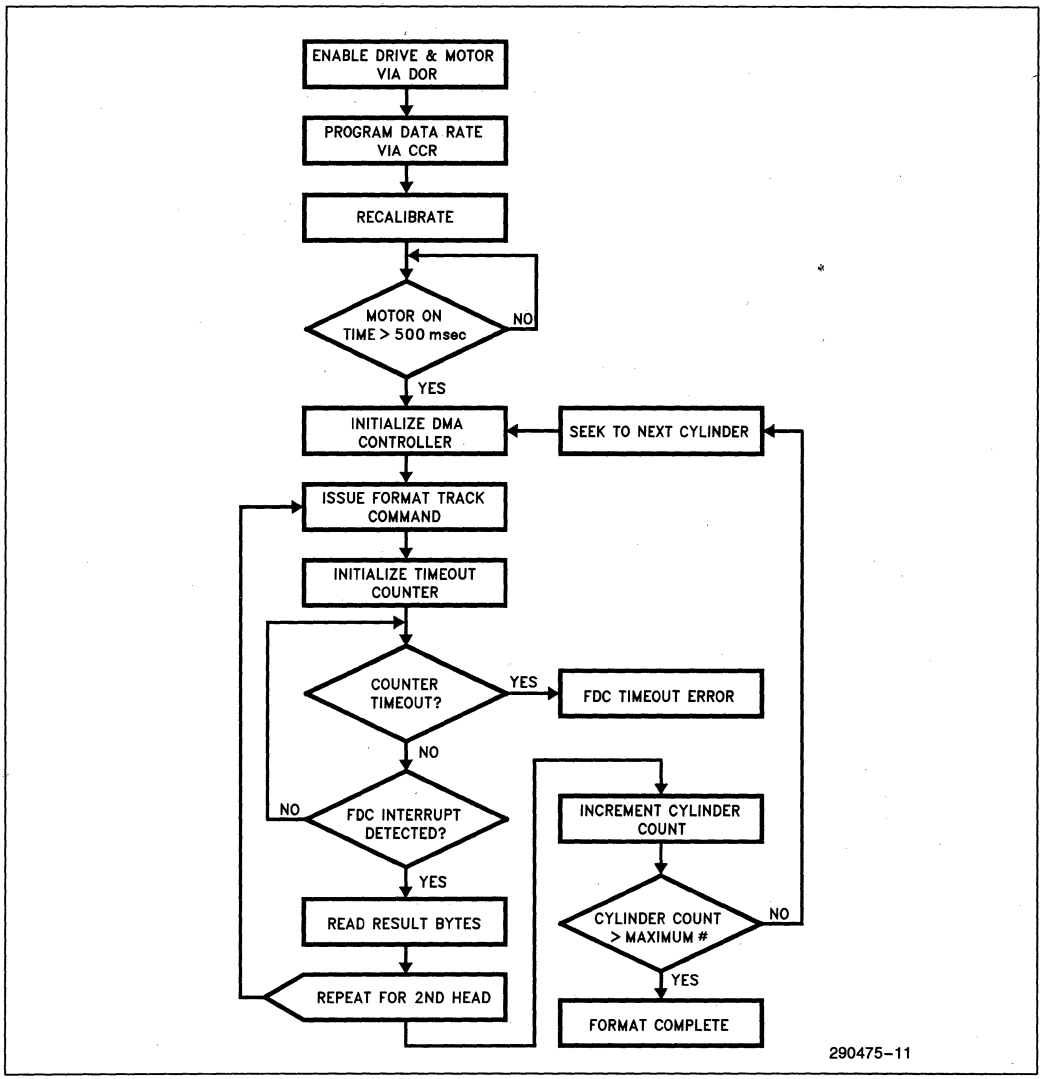


Figure 9-6. Formatting

After each head for a cylinder has been formatted, a seek operation to the next cylinder is performed and the format process is repeated. Since the FORMAT TRACK command does not have implied seek capability, the SEEK command must be used. Also, as discussed in Section 9.2, the head settling time needs to be adhered to after each seek operation.

9.6 Save and Restore

The Save and Restore commands were developed for portable systems that use zero-volt powerdown to conserve power. These systems turn off the V_{CC} to most of the system and retain the system status in a specific location. In older floppy controller designs, in order for system designers to retrieve the floppy controller status, a lot of separate commands and register reads were required. The Save command stores the key status information in a single command, the Restore command restores this information with a single command. These commands can be integrated into the SMM module that is responsible for zero-volt powerdown.

The sequence of initializing the 82078 after a reset occurred and assuming a Save command was issued follows:

- Issue the Drive Spec command (if the design utilizes this command)
- Issue the Restore command

The Restore command programs the data rate and precompensation value via the DSR. It then restores the values normally programmed through the Configure, Specify, and Perpendicular commands. It also enables the previously selected values for the AUTO Powerdown command. The command then restores the PCN values to its previous values. The user is responsible for issuing the seek and recalibrate commands to restore the head to the proper location. There are some drives that do not recalibrate in which case the Restore command will restore the previous state completely. The PDOSC bit is retrievable using the Save command, however it is up to the system designer to set it correctly. The software must allow at least 20 μs to execute the Restore command. When using the BOOTSEL bits in the TDR, the user must restore or reinitialize these bits to their proper values.

9.7 Verifies

In some applications, the sector data needs to be verified immediately after each write operation. One verify technique reinitializes the DMA controller to perform a read transfer or verify transfer (DACK# is asserted but not RD#) immediately after each write operation. Issue a read command to the disk controller and the resulting status indicates if the CRC validated the previously written data. This technique has the drawback of requiring additional software intervention by having to reprogram the DMA controller between each sector write operation. The 82078 supports this verify technique but also provides a VERIFY command that does not require the use of the DMA controller.

To verify a write data transfer or format track operation using the VERIFY command, the software simply issues the command with the same format as a READ DATA command but without the support of the DMA controller. The 82078 will then perform a disk read operation without a host data transfer. The CRC will be calculated for each sector read and compared against the value stored on the disk. When the VERIFY command is complete, the status register reports detected CRC errors.

9.8 Powerdown State and Recovery

The two power management modes coupled with the internal oscillator power management forms an important consideration for programming the 82078. The recovery of 82078 and the time it takes to achieve complete recovery depends on how 82078 is powered down and how it is awakened. The following sections describe all the programming concerns and subtleties involved in using power management features of the 82078.

9.8.1 OSCILLATOR POWER MANAGEMENT

Section 4.1 covers the power management scheme involved in powering down of both an internal and an external oscillator. Both types of oscillators face drop out effects and require recovery times on the order of tens of milliseconds (this may be objectionable to some application software). This means that if the oscillator is powered down then it is imperative for the software to assure enough time for the oscillator to recover to a stable state. Oscillator power management must be controlled by the system software especially to maintain software transparency. In cases where the system goes into a standby mode (by user request or system time-out), the power management software can turn off the oscillator to conserve power. This can also be controlled in hardware using the Powerdown (PD) pin. Complete recovery from an oscillator powerdown state requires the software to turn on the oscillator sufficiently ahead of awakening the 82078.

9.8.2 PART POWER MANAGEMENT

The part powerdown and wake up modes are covered in Section 4.2 in detail. This section is meant to address the programming concerns for the part (excluding the oscillator) during these modes.

9.8.2.1 Powerdown Modes

For both types of powerdown modes—DSR powerdown and auto powerdown, if reset is used to exit the part from powerdown then the internal microcontroller will go through a standard sequence: register initialization followed after some delay by an interrupt.

Software transparency in auto powerdown mode is preserved by MSR retaining the value of 80H which indicates that the part is ready to receive a command. This feature allows the part to powerdown while maintaining its responsiveness to any application software.

The PD and IDLE status bits can be monitored via the Status Register B (SRB, enhanced AT/EISA mode) and in the Digital Input Register (DIR, PS/2 and Model 30). Since the IDLE pin stays high when the 82078 is in idle state, the IDLEMSK bit can be used to set the pin low again (as part of a power management routine).

9.8.2.2 Wake Up Modes

Wake up from DSR powerdown results in the part being internally reset and all present status being lost. During DSR powerdown the RQM bit in the MSR is set. A software or hardware reset will wake up the part.

The case for wake up from auto powerdown is different. The BIOS and application software are very sensitive to delays involved in writing the first command bytes to the 82078. Most programs have short error time-outs in these cases. Such programs would not tolerate any floppy disk controller that was unable to receive the first byte of a command at any time. The following describes how 82078 uniquely sustains its software transparency during wake up sequences.

Prior to writing a command to 82078, it is first necessary to read the MSR to ensure that the 82078 is ready (RQM bit must be set) to receive the command. When the part detects a MSR read, it assumes that another command will follow and begins the wake up process. While the part is waking up it does not change the state of the MSR (MSR = 80H) and is able to receive the command in the FIFO. At this point one of the two following scenarios can occur.

No other command is sent subsequent to the MSR read. The part wakes up and initializes the minimum power up timer. Upon the expiration of this timer the part is once again put in powerdown state.

Another command follows the MSR read. If the command is sent during the part's recovery from powerdown, the part remembers the command, clears the RQM bit (to prevent further bytes being written) and acts on the command once it is fully awake.

If the MSR was not checked prior to writing of a command, the part will proceed as stated above with the RQM bit cleared and the command byte held until the internal microcontroller is ready. Writing the motor enable bits in DOR active will initiate the wake up sequence with RQM set high, ready to receive any command.

As it is clear from the above discussion, the immediate access to the floppy disk controller for the first command byte is vital to software transparency. The recovery of the part from powerdown may involve a delay after the first command byte has been issued. However, all programs have tolerance for the delay after the first command byte is issued. In a powered up chip, it is possible for the microcontroller to be in its "polling loop". As a result the tolerance for this delay provides an excellent window for recovery of the part.

10.0 DESIGN APPLICATIONS

10.1 Operating the 82078SL in a 3.3V Design

The design for 3.3V is the same as for 5.0V with two exceptions: The SEL3V# pin must be held low to select 3.3V operation, and the VCCF pin can be either 3.3V or 5.0V (VCCF can only be 5.0V when SEL3V# is high). The VCCF pin allows the controller to be operated in mixed (3.3V/5.0V) mode. For example, if the system operates at 3.3V and the floppy disk drive operates at 5.0V, the 82078 can be configured to operate at 3.3V with 5.0V available to the drive interface. See Figure 10-1 for a schematic.

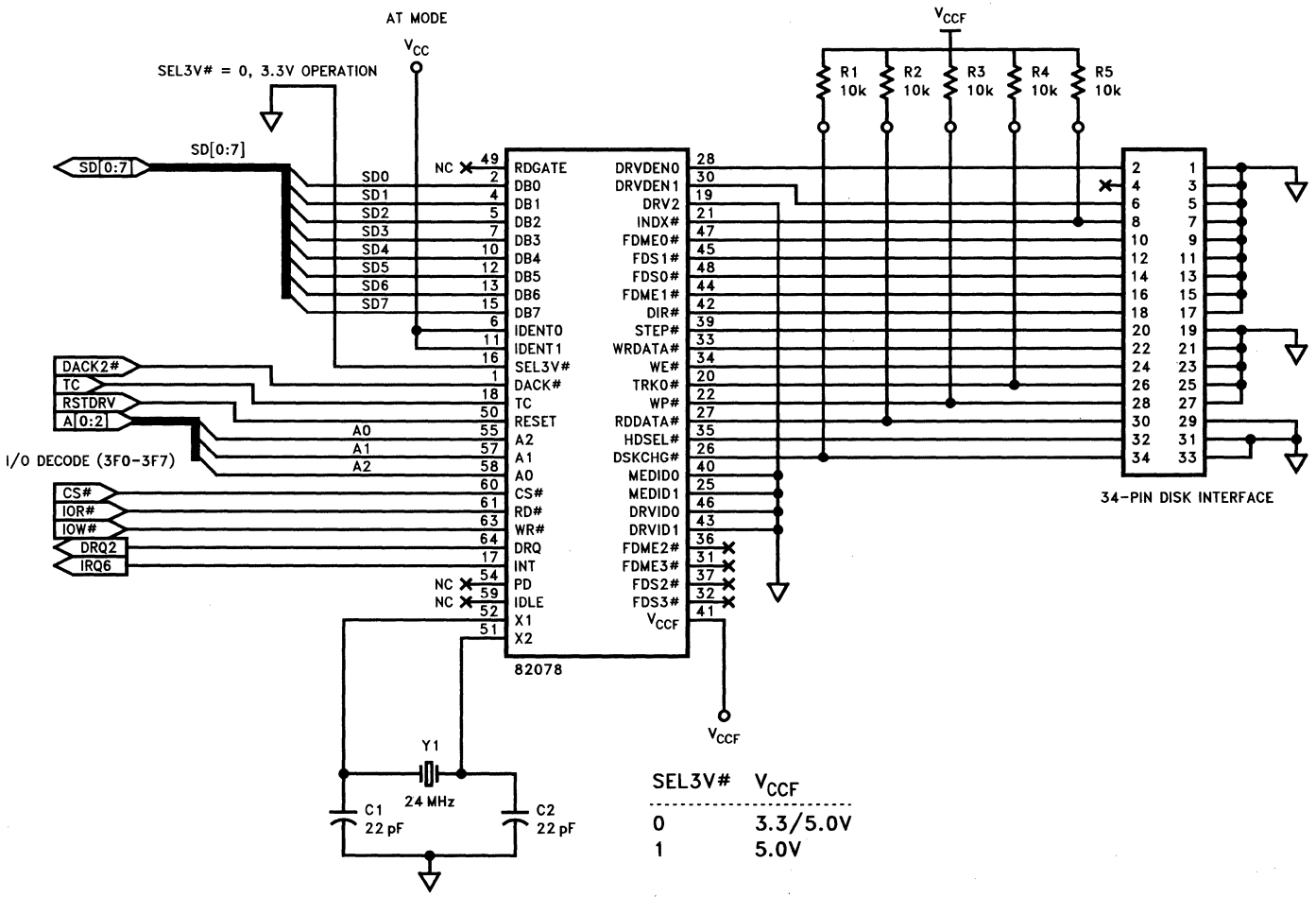


Figure 10-1. 82078SL 3.3V Design

10.2 Selectable Boot Drive

Generally a standard personal computer is configured with a 1.2 Mb 5.25″ disk drive and a 1.44 or 2.88 Mb 3.5″ disk drive. Usually the drive connects as "A:" and is the boot drive. At times the user may want to configure "B:" as the boot drive. Currently some BIOS' use a special implementation in software to accomplish this. The 82078 now offers this capability more efficiently by configuring the boot drives.

The 82078 allows for virtual drive designations. This is a result of allowing multiplexing the boot drive select and motor enable lines. This is shown in the Figure 10-2.

The DRIVE SEL1 and the DRIVE SEL2 bits in the DOR register decode internally to generate the signals DSn. The MEn signals generate directly from the DOR register. The DSn and MEn signals get mapped to actual FDSn and FDMEn pins based on the BOOTSELn bits (selected in the TDR register). The exact mapping of BOOTSEL vs. the FDSn and FDMEn pins is shown in the following table.

BOOTSEL1	BOOTSEL0	Mapping:
0	0	DS0 → FDS0, ME0 → FDME0 DS1 → FDS1, ME1 → FDME1 DS2 → FDS2, ME2 → FDME2
0	1	DS0 → FDS1, ME0 → FDME1 DS1 → FDS0, ME1 → FDME0 DS2 → FDS2, ME2 → FDME2
1	0	DS0 → FDS2, ME0 → FDME2 DS1 → FDS1, ME1 → FDME1 DS2 → FDS0, ME2 → FDME0
1	1	Reserved

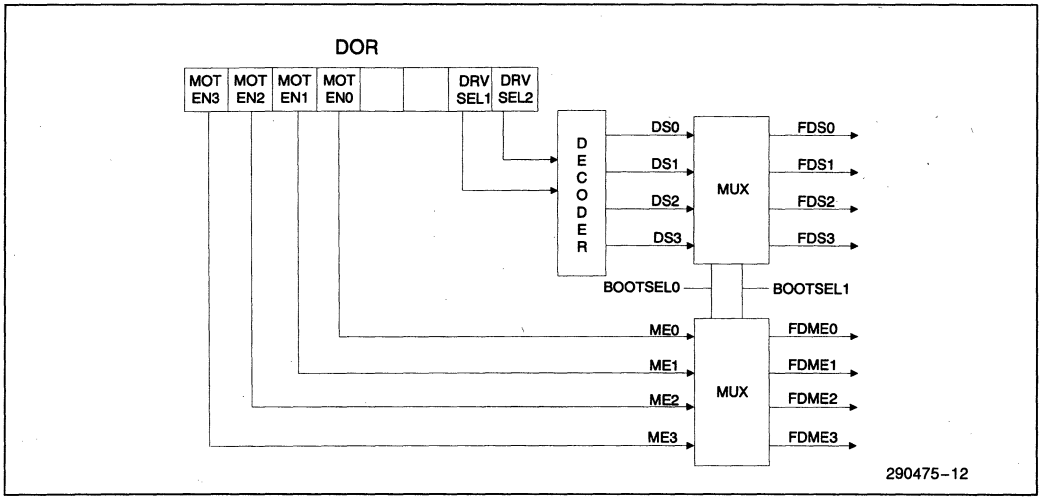


Figure 10-2. Virtual Drive Configuration

The BOOTSELn bits allow users to multiplex the output drive signals allowing different drives to be the boot drive. The DSn and MEn bits are considered virtual designations since the DSn and MEn signals get remapped to different corresponding physical FDSn and FDMEn pins. In other words, once the BOOTSELn bits are configured for a non-default selection, all future references made to the controller will be assumed as virtual designations. For example, if BOOTSEL1, BOOTSEL0 = 10 then DOR[1:0] = 00 refers to drive 2 and FDS2, FDME2 lines will be activated. Also, if TAPESEL[1:0] = 10, then tape mode is selected whenever FDS0, FDME0 are selected. Note, due to the virtual designations TAPESEL[1:0] = 00 would never enable tape mode due to boot drive restrictions.

10.3 How to Disable the Native Floppy Controller on the Motherboard

There are occasions when the floppy controller designed onto the motherboard of a system needs to be disabled in order to operate another floppy controller on the expansion bus. This can be done without changing the BIOS or remapping the address of the floppy controller (provided there is a jumper, or another way to disable the chip select on the native controller).

Upon reset, the DOR register in the 82078 is set to 00H. If the CS# is left enabled during the POST, the DOR is set to 0CH, this enables the DMA GATE# bit in the DOR. When this bit is set the 82078 treats a DACK# and a RD# or WR# as an internal chip select (CS#). Bus contention will occur between the native controller and the auxiliary controller if the DMA GATE# bit becomes active, even if the CS# signal is not present.

The proper way to disable the native floppy controller is to disable the CS# before the system is turned on. This will prevent the native controller from getting initialized. Another option is to map the native controller to a secondary address space, then disable the DMA GATE# via the DOR disabling the DMA GATE#. This assumes that the native controller is switchable to a secondary address space.

10.4 Replacing the 82077SL with a 82078 in a 5.0V Design

The 82078 easily replaces the 5.0V 82077SL with minimum design changes. With a few exceptions, most of the signals are named as they were in the 82077SL. Some pins were eliminated and other renamed to accommodate a reduced pin count and smaller package.

The connections to the AT bus are the same as the 82077SL with the following exceptions: MFM and IDENT have been replaced by IDENT1 and IDENT0. The PLL0 pin was removed. Configure the tape drive mode on the 82078 via the Tape Drive Register (TDR).

The Drive Interface on the 82078 is also similar to the 82077SL except as noted: DRVDEN0 and DRVDEN1 on the 82078 take the place of DENSEL, DRATE0, and DRATE1 on the 82077SL. The Drive Specification Command configures the polarity of these pins, thus selecting the density type of the drive. The Motor Enable pins (ME0-3) and the Drive Select pins (DS0-3) are renamed FDME(0-3) and FDS(0-3) respectively on the 82078. 10K pull-up resistors can be used on the disk interface. See Figure 10-3 for a schematic of the connection.

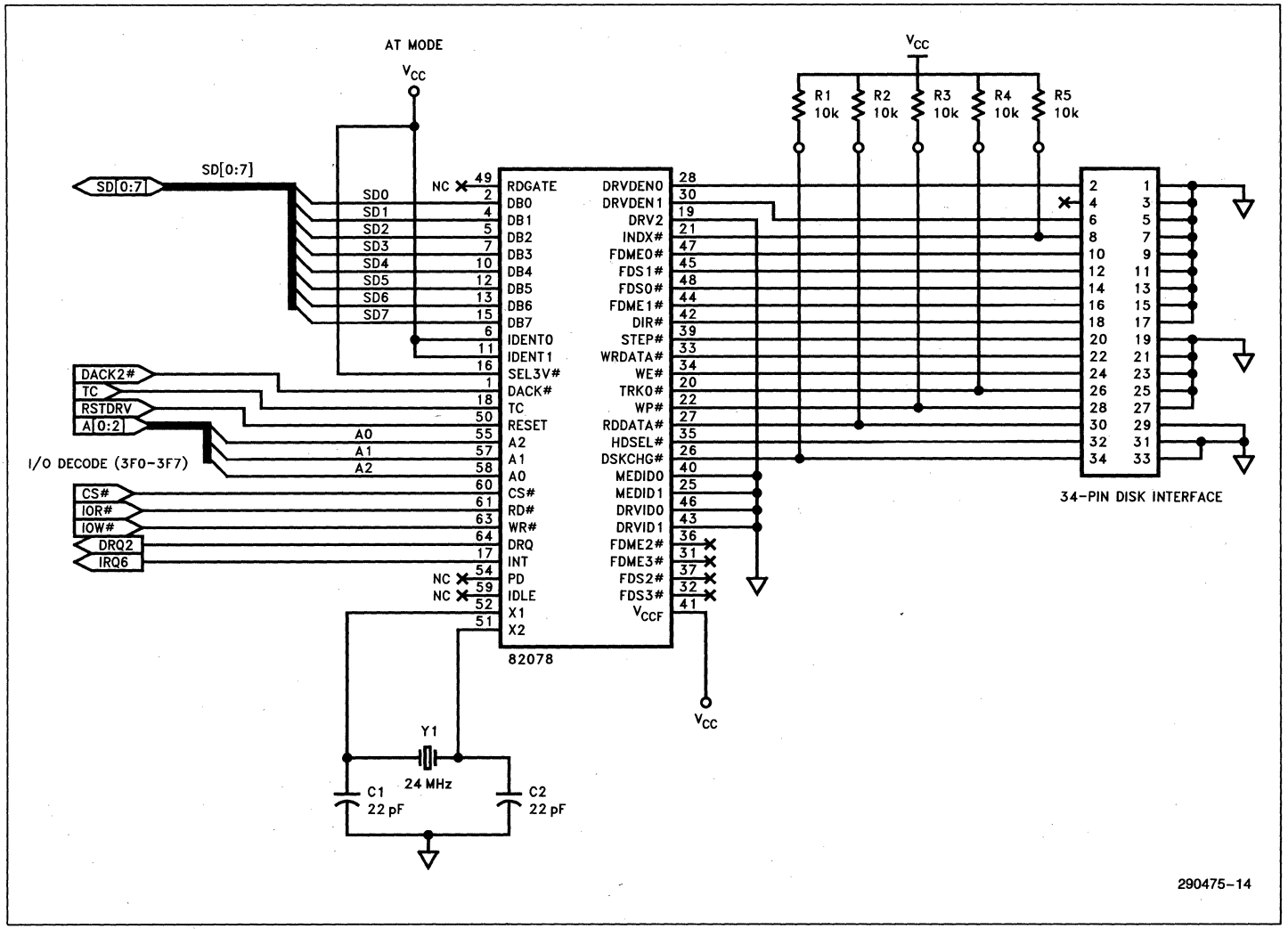


Figure 10-3. 82077SL Conversion to 82078-1

Pin Changes on the 64 Pin Part:

- INVERT# is removed
- 4 NC's (no connects) are removed
- MFM, IDENT pins on the 82077SL have been changed to IDENT1 and IDENT0 respectively.
- PLL0 pin, which allowed for H/W configuration of tape drive mode is no longer available. Tape mode can be configured via the TDR register.
- DENSEL, DRATE1, DRATE0 pins have been substituted by DRVDEN0, DRVDEN1. The Drive Specification command can be used to configure these pins for various requirements of drives available on the market.
- RDGATE has been added and can be used for diagnostics of the PLL.
- MEDID1, MEDID0 are new, they return media type information to the TDR register.
- DRVID1, DRVID0 return drive type information to the TDR register.
- SEL3V# selects between either 3.3V or 5V mode. Connecting the pin LOW selects 3.3V mode.
- 5 VSS pins, 2 VCC pins, 2 VSSP pins, 1 VCCF pin, and 1 AVCC and 1 AVSS pin.
- VCCF can be used to interface a 5.0V or a 3.3V drive to the 82078 (when SEL3V# is low).
- The Hardware RESET pulse width has changed from 170 times the oscillator period to 100 ns plus 25 times the oscillator period.

11.0 D.C. SPECIFICATIONS

11.1 Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Supply Voltage	−0.5V to +8.0V
Voltage on Any Input	GND −2V to 6.5V
Voltage on Any Output	GND −0.5V to V_{CC} +0.5V
Power Dissipation	1W

11.2 D.C. Characteristics T_A = 0°C to 70°C, V_{SS} = AV_{SS} = 0V

64 PIN D.C. CHARACTERISTICS

Symbol	Parameter	V_{CC} = +5V ±10%(7)			V_{CC} = 3.3V ± 0.3V		
		Min(V)	Max(V)	Test Conditions	Min(V)	Max(V)	Test Conditions
V_{ILC}	Input Low Voltage, X1	−0.5	0.8		−0.3	0.8	
V_{IHC}	Input High Voltage, X1	3.9	V_{CC} + 0.5		2.4	V_{CC} + 0.3	
V_{IL}	Input Low Voltage (all pins except X1)	−0.5	0.8		−0.3	0.8	
V_{IH}	Input High Voltage (all pins except X1)	2.0	V_{CC} + 0.5		2.0	V_{CC} + 0.3	
V_{OL}	System Interface		0.4	I_{OL} = 12 mA		0.4	I_{OL} = 6 mA
	FDD Interface outputs		0.4	I_{OL} = 24 mA		0.4	I_{OL} = 12 mA
	Status Outputs (Note 6)		0.4	I_{OL} = 4 mA		0.4	I_{OL} = 4 mA
V_{OH}	All outputs	3.0		I_{OH} = −4.0 mA	2.4		I_{OH} = −2.0 mA
	All outputs	V_{CC} − 0.4		I_{OH} = −100 µA	V_{CC} − 0.2		I_{OH} = −100 µA

64 PIN D.C. CHARACTERISTICS (I_{CC})

Symbol	Parameter	V_{CC} = +5V ±10%(7)			V_{CC} = 3.3V ± 0.3V		
		Typ	Max(A)	Test Conditions	Typ	Max(A)	Test Conditions
I_{CC1}	1 Mbps Data Rate V_{IL} = V_{SS}, V_{IH} = V_{CC}	15.4 mA	25 mA	(Notes 1, 2, 5)	8.4 mA	16 mA	(Notes 1, 2)
I_{CC2}	1 Mbps Data Rate V_{IL} = 0.45V, V_{IH} = 2.4V	20.8 mA	30 mA	(Notes 1, 2, 5)	8.6 mA	16 mA	(Notes 1, 2)
I_{CC3}	500 Kbps Data Rate V_{IL} = V_{SS}, V_{IH} = V_{CC}	11.8 mA	20 mA	(Notes 1, 2)	6.2 mA	14 mA	(Notes 1, 2)
I_{CC4}	500 Kbps Data Rate V_{IL} = 0.45V, V_{IH} = 2.4V	17.6 mA	25 mA	(Notes 1, 2)	6.2 mA	14 mA	(Notes 1, 2)
I_{CCSB}	I_{CC} in Powerdown	0 µA	60 µA	(Notes 3, 4)	0 µA	60 µA	(Notes 3, 4)

64 PIN D.C. CHARACTERISTICS (I_{CC}) (Continued)

Symbol	Parameter	V_{CC} = +5V ±10%(7)			V_{CC} = 3.3V ± 0.3V		
		Typ	Max(A)	Test Conditions	Typ	Max(A)	Test Conditions
I_{IL}	Input Load Current (all input pins)		10 μA −10 μA	$V_{IN} = V_{CC}$ $V_{IN} = 0V$		10 μA −10 μA	$V_{IN} = V_{CC}$ $V_{IN} = 0V$
I_{OFL}	Data Bus Output Float Leakage		±10 μA	$0.45 < V_{OUT} < V_{CC}$		±10 μA ±10 μA	$0.45 < V_{OUT} < V_{CC}$

NOTES:
1. Only the data bus inputs may float.
2. Tested while reading a sync field of "00". Outputs not connected to D.C. loads.
3. $V_{IL} = V_{SS}$, $V_{IH} = V_{CC}$; Outputs not connected to D.C. loads.
4. Typical value with the oscillator off.
5. I_{CC} for 2 Mbps Data Rate: Max 40 mA (TTL), 35 mA (CMOS) at 5.5V, typical 29.2 mA (TTL) and 24.4 (CMOS).
6. Status outputs are PD, IDLE, and RDGATE.
7. V_{CC} and V_{CCF} for the 82078-1 is +5V ±5%.

2

64 PIN MIXED MODE D.C. CHARACTERISTICS

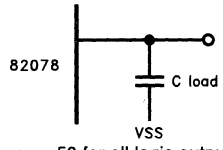
Symbol	Parameter	V_{CC} = 3.3V ±0.3V, V_{CCF} = +5V ±10%(7)		
		Min(V)	Max(V)	Test Conditions
V_{ILC}	Input Low Voltage, X1	−0.3	0.8	
V_{IHC}	Input High Voltage, X1	2.4	V_{CC} + 0.3	
V_{IL}	Input Low Voltage (system pins except X1) (floppy drive interface pins)	−0.3 −0.5	0.8 0.8	
V_{IH}	Input High Voltage (system interface pins except X1) (floppy drive interface pins)	2.0 2.0	V_{CC} + 0.3 V_{CC} + 0.5	
V_{OL}	System Interface		0.4	I_{OL} = 6 mA
	FDD Interface outputs		0.4	I_{OL} = 24 mA
	Status Pins: IDLE, PD, RDGATE		0.4	I_{OL} = 4 mA
V_{OH}	All system outputs	2.4		I_{OH} = −2.0 mA
	All FDD interface outputs	3.0		I_{OH} = −4.0 mA
	All system outputs	V_{CC} − 0.2		I_{OH} = −100 μA
	All FDD interface outputs	V_{CC} − 0.4		I_{OH} = −100 μA

CAPACITANCE

C_{IN}	Input Capacitance	10	pF	F = 1 MHz, T_A = 25°C
C_{IN1}	Clock Input Capacitance	20	pF	Sampled, not 100% Tested
$C_{I/O}$	Input/Output Capacitance	20	pF	

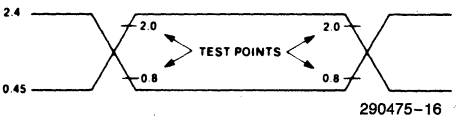
NOTE:
All pins except pins under test are tied to AC ground.

LOAD CIRCUIT

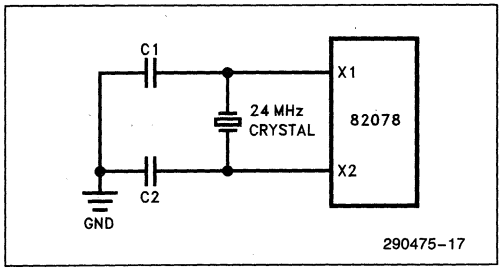


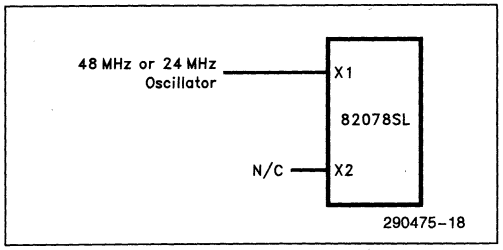
C_{load} = 50 for all logic outputs, 100 pF for the data bus.

A.C. TESTING INPUT, OUTPUT WAVEFORM



11.3 Oscillator





The 24 MHz clock can be supplied either by a crystal or a MOS level square wave. All internal timings are referenced to this clock or a scaled count which is data rate dependent.

The crystal oscillator must be allowed to run for 10 ms after V_{CC} has reached 4.5V or exiting the POWERDOWN mode to guarantee that it is stable.

Frequency:	24 MHz ±0.1%
Mode:	Parallel Resonant
	Fundamental Mode
Series Resistance:	Less than 40Ω
Shunt Capacitance:	Less than 5 pF

12.0 A.C. SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%[17], +3.3V ±0.3V, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit
CLOCK TIMINGS				
t1	Clock Rise Time		10	ns
	Clock Fall Time		10	ns
t2	Clock High Time[7]	16	26	ns
t3	Clock Low Time[7]	16	26	ns
t4	Clock Period	41.66	41.66	ns
t5	Internal Clock Period[3]			
HOST READ CYCLES				
t7	Address Setup to RD#	5		ns
t8	RD# Pulse Width	90		ns
t9	Address Hold from RD#	0		ns
t10	Data Valid from RD#[12]		80	ns
t11	Command Inactive	60		ns
t12	Output Float Delay		35	ns
t13	INT Delay from RD#[16]		t5 + 125	ns
t14	Data Hold from RD#	5		ns
HOST WRITE CYCLES				
t15	Address Setup to WR#	5		ns
t16	WR# Pulse Width	90		ns
t17	Address Hold from WR#	0		ns
t18	Command Inactive	60		ns
t19	Data Setup to WR#	70		ns
t20	Data Hold from WR#	0		ns
t21	INT Delay from WR#[16]		t5 + 125	ns
DMA CYCLES				
t22	DRQ Cycle Period[1]	6.5		µs
t23	DACK# to DRQ Inactive		75	ns
t23a	DRQ to DACK# Inactive	(Note 15)		ns
t24	RD# to DRQ Inactive[4]		100	ns
t25	DACK# Setup to RD#, WR#	5		ns
t26	DACK# Hold from RD#, WR#	0		ns
t27	DRQ to RD#, WR# Active[1]	0	6	µs
t28	Terminal Count Width[10]	50		ns
t29	TC to DRQ Inactive		150	ns
RESET				
t30	"Hardware" Reset Width[5]	1.13		µs
t30a	"Software" Reset Width[5]	(Note 11)		ns
t31	Reset to Control Inactive		2	µs

A.C. SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%[17], +3.3V ±0.3V, V_{SS} = AV_{SS} = 0V (Continued)

Symbol	Parameter	Min	Max	Unit
WRITE DATA TIMING				
t32	Write Data Width[6]			ns
DRIVE CONTROL				
t35	DIR# Setup to STEP#[14]	1.0		µs
t36	DIR# Hold from STEP#	10		µs
t37	STEP# Active Time (High)	2.5		µs
t38	STEP# Cycle Time[2]			µs
t39	INDEX# Pulse Width	5		t5
t41	WE# to HDSEL# Change	(Note 13)		ms
READ DATA TIMING				
t40	Read Data Pulse Width	50		ns
t44	82078-1		2M	bits/sec
	82078SL		1M	bits/sec
t44	Data Rate Period = 1/f44			
tLOCK	Lockup Time		64	t44

NOTES:

1. This timing is for FIFO threshold = 1. When FIFO threshold is N bytes, the value should be multiplied by N and subtract 1.5 µs. The value shown is for 1 Mbps, scales linearly with data rate.
2. This value can range from 0.5 ms to 8.0 ms and is dependent upon data rate and the Specify command value.
3. Many timings are a function of the selected data rate. The nominal values for the internal clock period (t5) for the various data rates are:

2 Mbps	1.5x oscillator period = 62.5 ns
1 Mbps	3x oscillator period = 125 ns
500 Kbps	6x oscillator period = 250 ns
300 Kbps	10x oscillator period = 420 ns
250 Kbps	12x oscillator period = 500 ns

4. If DACK# transitions before RD#, then this specification is ignored. If there is no transition on DACK#, then this becomes the DRQ inactive delay.
5. Reset requires a stable oscillator to meet the minimum active period.

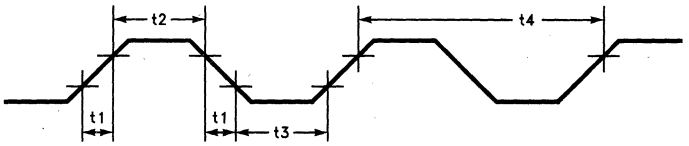
6. Based on the internal clock period (t5). For various data rates, the Write Data Width minimum values are:
   - 2 Mbps 2.5x oscillator period −50 ns = 75 ns
   - 1 Mbps 5x oscillator period −50 ns = 150 ns
   - 500 Kbps 10x oscillator period −50 ns = 360 ns
   - 300 Kbps 16x oscillator period −50 ns = 615 ns
   - 250 Kbps 19x oscillator period −50 ns = 740 ns
7. Test points for clock high time are 3.5V. Due to transitional times, clock high time max and clock low time max cannot be met simultaneously. Clock high time min and clock low time max can not be met simultaneously.
8. Based on internal clock period (t5).
9. Jitter tolerance is defined as:
   (Maximum bit shift from nominal position ÷ ¼ period of nominal data rate) × 100% is a measure of the allowable bit jitter that may be present and still be correctly detected. The data separator jitter tolerance is measured under dynamic conditions that jitters the bit stream according to a reverse precompensation algorithm.
10. TC width is defined as the time that both TC and DACK# are active. Note that TC and DACK# must overlap at least 50 ns.
11. The minimum reset active period for a software reset is dependent on the data rate, after the 82078 has been properly reset using the t30 spec. The minimum software reset period then becomes:
    - 2 Mbps 1.5 x t4 = 62.5 ns
    - 1 Mbps 3 x t4 = 125 ns
    - 500 Kbps 6 x t4 = 250 ns
    - 300 Kbps 10 x t4 = 420 ns
    - 250 Kbps 12 x t4 = 500 ns
12. Status Register's status bits which are not latched may be updated during a Host read operation.
13. The minimum MFM values for WE to HDSEL change (t41) for the various data rates are:
    - 2 Mbps 0.5 ms + [4 x GPL]
    - 1 Mbps 0.5 ms + [8 x GPL]
    - 500 Kbps 1.0 ms + [16 x GPL]
    - 300 Kbps 1.6 ms + [26.66 x GPL]
    - 250 Kbps 2.0 ms + [32 x GPL]

    GPL is the size of gap 3 defined in the sixth byte of a Write Command.
14. This timing is a function of the selected data rate as follows:
    - 2 Mbps 0.5 μs Min
    - 1 Mbps 1.0 μs Min
    - 500 Kbps 2.0 μs Min
    - 300 Kbps 3.3 μs Min
    - 250 Kbps 4.0 μs Min
15. This timing is a function of the internal clock period (t5) and is given as (⅔) t5. The values of t5 are shown in Note 3.
16. The timings t13 and t21 are specified for INT signal in the polling mode only. These timings in case of the result phase of the read and write commands are microcode dependent.

Part Specification	3.3V	5.0V	2 Mbps Data Rate
82078SL	X	X	
82078-1		X	X

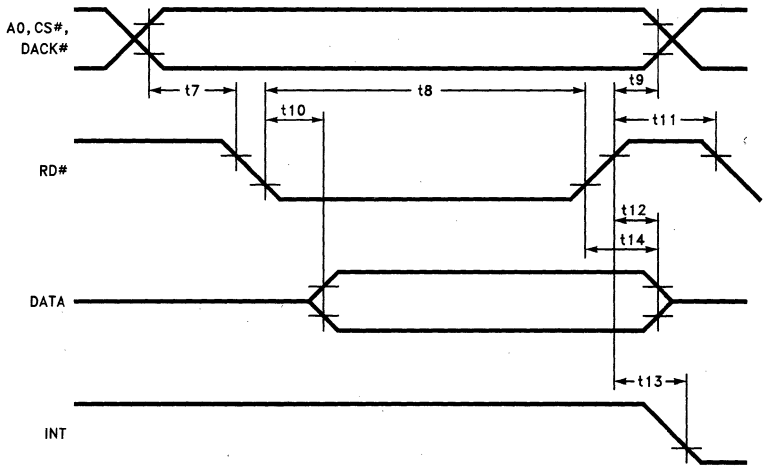
17. For 82078-1 only, V_{CC} and V_{CCF} requirements are +5V ±5%.

Clock Timings



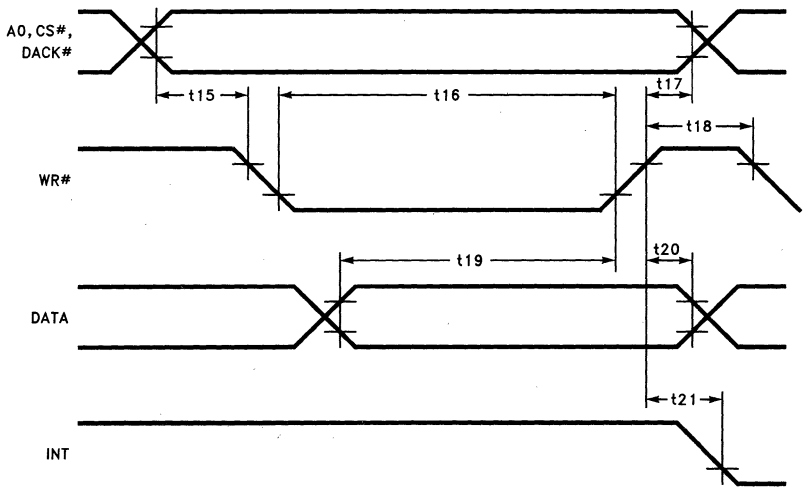
290475-19

Host Read Cycles



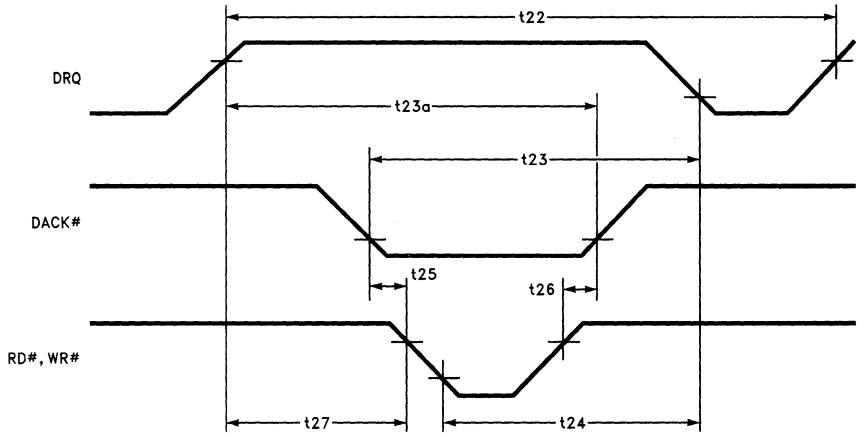
290475-20

Host Write Cycles



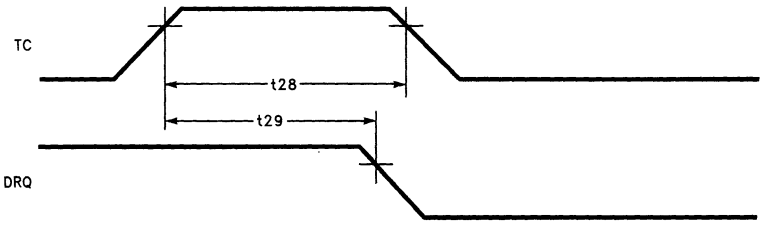
290475-21

DMA Cycles



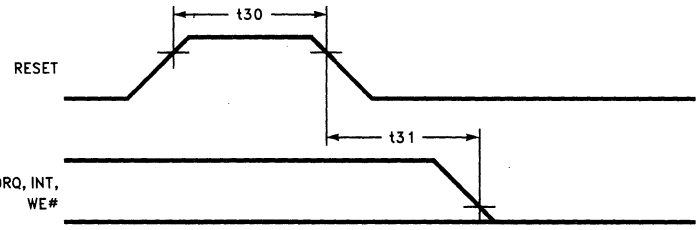
290475-22

Terminal Count



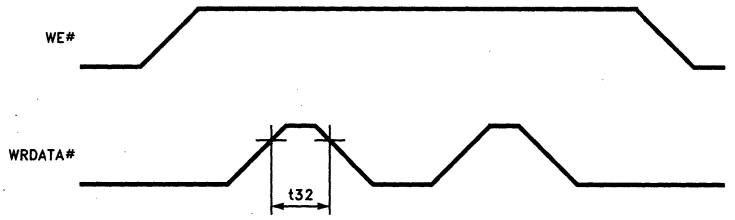
290475-23

Reset



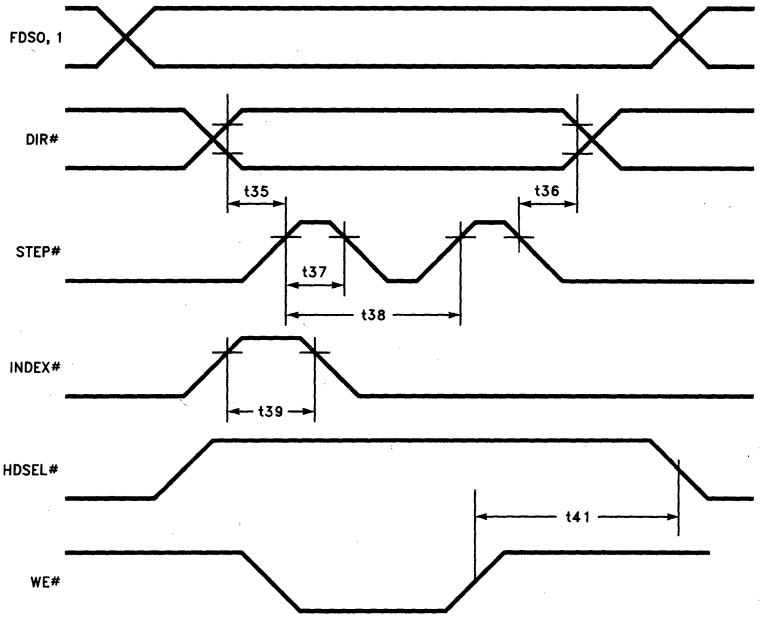
290475-24

Write Data Timing



290475-25

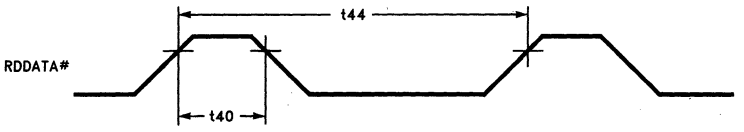
Drive Control



290475-26

NOTE:
For overlapped seeks, only one step pulse per drive selection is issued. Non-overlapped seeks will issue all programmed step pulses.

Internal PLL

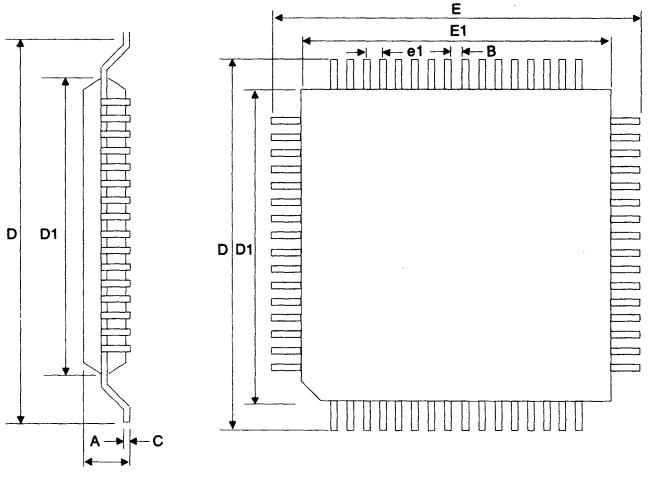


290475-27

12.1 Package Outline for the 64 QFP Part

The 82078 addresses the current need of the smaller and thinner packages, for the current market. The size of the part is becoming increasingly important in the portable computer market. The QFP part considerably reduces the real estate consumed. The package outline, with the appropriate dimensions is given below:

64-Lead Quad Flatpack Package



290475-28

Description	Symbol	64 QFP Package	
		Nominal (mm)	Tolerance (mm)
Overall Height	A	2.35	±0.20
Stand Off	A1	0.15	±0.10
Lead Width	B	0.30	±0.10
Lead Thickness	C	0.15	±0.05
Terminal	D	15.3	±0.40
Long Side	D1	12.0	±0.10
Terminal	E	15.3	±0.40
Short Side	E1	12.0	±0.10
Lead Spacing	e1	0.65	±0.12
Lead Count	N	64	

13.0 REVISION HISTORY FOR THE 82078 64 PIN

The following list represents the key differences between version 002 and version 003 of the 82078 64 pin data sheet.

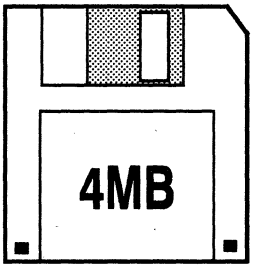
Section 5.2.3	Redundant information removed.
Section 5.2.4	Redundant information removed.
Section 8.0	Description of IDENT0 and IDENT1 changed to clarify their function.
Section 11.2	New Vol specification added for status pins.
Table 6-2	Data in table reordered to be consistent.
AC Specifications	V_{CC} has changed for 82078-1 only.

intel®

AP-358

APPLICATION NOTE

Intel 82077SL for Super Dense Floppies



292093-1

KATEN A. SHAH
APPLICATION ENGINEER

September 1992

Order Number: 292093-002

Intel 82077SL for Super Dense Floppies

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INTRODUCTION

The evolution of the floppy has been marked in little over a decade by a significant increase in capacity accompanied by a noticeable decrease in the form factor from the early 8 inch floppy disks to the present day 3.5 inch floppy disks. This decade will also be remarkable as OEMs adopt "Super" dense floppies.

The most commonly seen floppies today are invariably one of the form factors – the 5.25″ or the 3.5″. Each form factor has several associated capacity ranges. The 5.25″ floppies available are: 180 KB (single density), 360 KB (double density) and 1.2 MB (high density). The 3.5″ floppies available are: 720 KB (double density) and 1.44 MB (high density). The emerging super dense floppies will evolve on the installed base of 3.5″ floppies. The latest member of this set is the 2.88 MB (extra density) floppy, pioneered by Toshiba. The cornerstone of market acceptance of newer drives is compatibility to the older family. The 2.88 MB (formatted) floppy drive allows the user to format, read from and write to the lower density diskettes.

As programs and data files get bigger, the demand for higher capacity floppies becomes obvious. There are several 3.5″ higher density drives available from various vendors with capacities well into the 20 MB range. NEC has introduced a 13 MB drive and companies such as Insite have introduced 20 MB drives. Both drives require servo-mechanisms to accurately position the head over the right track. NEC's drive has the standard floppy drive interface whereas Insite's interface is SCSI based. The market for these floppy drives will remain a niche unless they receive more OEM support.

Initiated by Toshiba's research and innovation of the higher density 4 MB floppy disk media, the market is headed towards the super dense floppy drive. After IBM's endorsement of the 4 MB (unformatted) floppy disk drives on their PS/2 model 57 and PS/2 model 90, several OEMs have shown a growing interest in "super" dense floppy disk drives. The latest DOS 5.0 supports the new 4 MB floppy media and BIOS vendors like Pheonix, AMI, Award, Quadtel, System Soft, and Microid all support the newer 4 MB floppy media.

PURPOSE

An important consideration to implement the 4 MB floppy drive is the floppy disk controller. Intel's highly integrated floppy disk controller, 82077AA/SL, has led the market in supporting the 4 MB floppy drive. Two ingredients are necessary to fully support these drives: 1 Mbps transfer rate and the perpendicular recording mode. This paper deals with a discussion of what the perpendicular mode is and how can a 4 MB floppy disk drive be implemented in a system using the 82077AA/SL.

PERPENDICULAR RECORDING MODE

Toshiba has taken the 2 MB floppy and doubled the storage capacity by doubling the number of bits per track. Toshiba achieved this by an innovative magnetic recording mode, called the vertical or the perpendicular recording mode. This mode utilizes magnetization perpendicular to the recording medium plane. This is in contrast to the current mode of longitudinal recording which uses the magnetization parallel to the recording plane. By making the bits stand vertical as opposed to on their side, recording density is effectively doubled, Figure 1. The new perpendicular mode of recording not only produces sharp magnetization transitions necessary at higher recording densities, but is also more stable.

The 4 MB disks utilize barium ferrite coated substrates to achieve perpendicular mode of magnetization. Current disks use cobalt iron oxide (Co-g-Fe_2O_3) coating for longitudinal recording. The barium ferrite ensures good head to medium contact, stable output and durability in terms of long use. High coercivity is required to attain high recording density for a longitudinal recording medium (coercivity specification of a disk refers to the magnetic field strength required to make an accurate record on the disk). A conventional head could not be used in this case; however, the barium ferrite disk has low coercivity and the conventional ferrite head can be used. The new combination heads include a pre-erase mechanism, i.e., the ferrite ring heads containing erase elements followed by the read/write head. These erase elements have deep overwrite penetration and ensure complete erasure for writing new data. The distance between the erase elements and the read/write head is about 200mm. This distance is important from the floppy disk controller point of view and will be discussed in later sections.

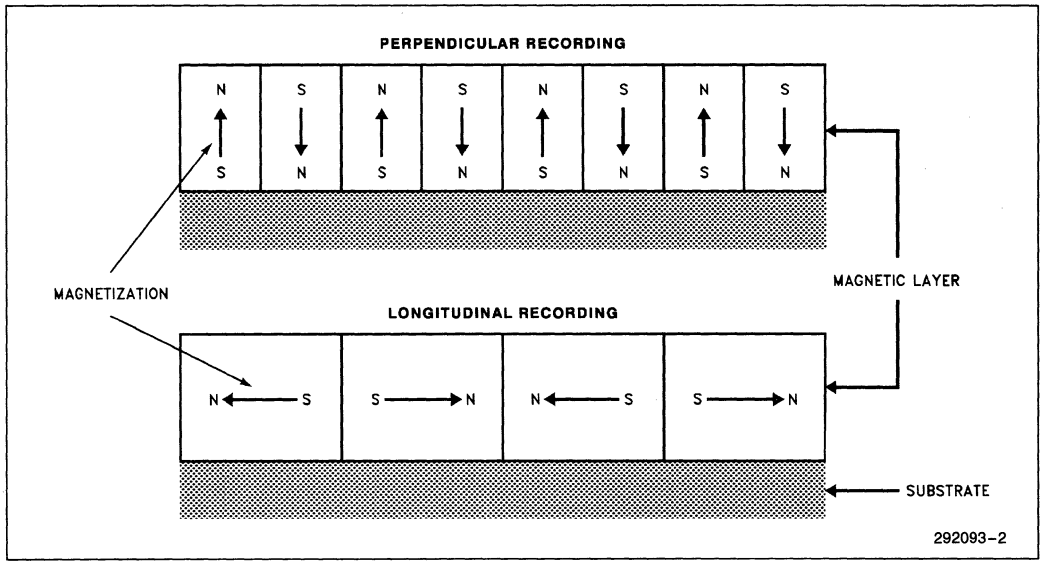


Figure 1. Perpendicular vs Longitudinal Recording

PERPENDICULAR DRIVE FORMAT AND SPECIFICATION

Figures 2a and 2b show the IBM drive format for both double density and perpendicular modes of recording. The main difference in recording format is the length of Gap2 between the ID field and the Data field. The main reason for the increased Gap2 length is the pre-erase head preceding the read/write head on the newer 4 MB floppy drives. The size of the data field is maintained at 512 KBytes standard. The increase in the capacity is implemented by increasing the number of sectors from 18 to 36. Table 1 shows the specifications of the various capacity 3.5″ drives.

PERPENDICULAR MODE COMMAND

The current 82077AA/SL parts contain the "enhanced" perpendicular mode command as shown in Figure 3. This is a two byte command with the first byte being the command code (0x12H). The 2nd byte contains the parameters required to enable perpendicular mode recording. The former command (in the older 82077 parts) included only the WGATE and GAP bits. This command is compatible to the older mode where only the two LSBs are written. The enhanced mode allows system designers to designate specific drives as perpendicular recording drives. The second byte will be referenced as the PR[0:7] byte for ease of discussion. The following discusses the use of the enhanced perpendicular recording mode.

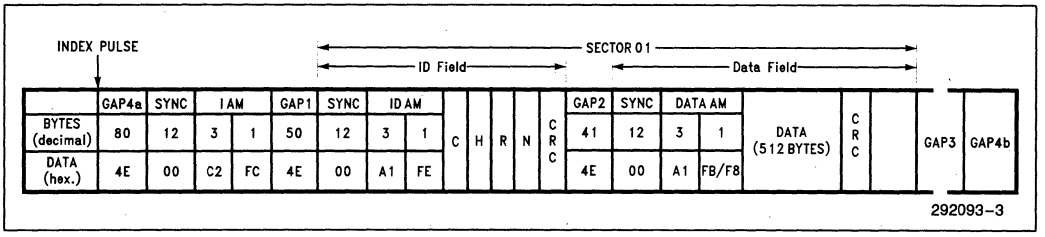


Figure 2a. Conventional IBM 1 MB and 2 MB Format (MFM)

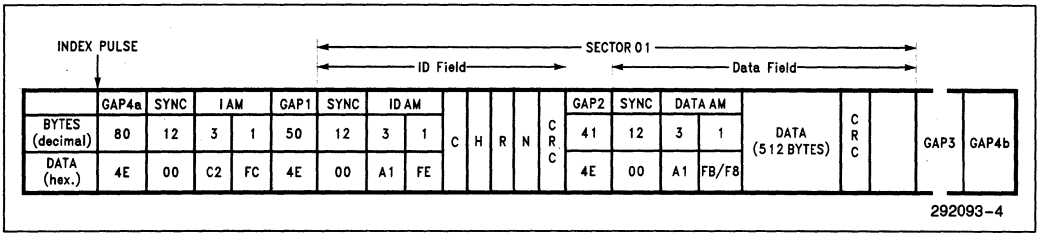


Figure 2b. Perpendicular 4 MB Format (MFM)

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
PERPENDICULAR MODE COMMAND										
Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WGATE	PR

Figure 3. Perpendicular Mode Command

Table 1. Specifications of FDDs

Various Parameters Used in the Different Kinds of FDDs.		5.25″ 360 KB	5.25″ 1.2 MB	3.5″ 720 KB	3.5″ 1.44 MB	3.5″ 2.88 MB
Number of Cylinders		40	80	80	80	80
Sectors/Track		9	15	9	18	36
Formatted Capacity		354 KB	1.2 MB	720 KB	1.44 MB	2.88MB
Unformatted Capacity		360 KB	1.6 MB	1 MB	2 MB	4 MB
Rotation Speed (rpm)	XT AT	300 360	360	300	300	300
Track Density (tpi)		48	96	135	135	135
Recording Density (bpi)		5876	9870	8717	17432	34868
Data Transfer Rate (Mbps)	XT AT	0.25 0.30	0.5	0.25	0.5	1
Gap Length for Read/Write		42	42	27	27	56
Gap Length for Format		80	80	84	84	83
Sector Size		512 KB	512 KB	512 KB	512 KB	512 KB
Density Notation		DD/DS	HD/DS	DD/DS	HD/DS	ED/DS

The following describes the various functions of the programmed bits in the PR:

OW — If this bit is not set high, all PR[2:5] are ignored. In other words, if OW = 0, only GAP and WGATE are considered. In order to select a drive as perpendicular, it is necessary to set OW = 1 and select the Dn bit.

Dn — This refers to the drive specification bits and corresponds to PR[2:5]. These bits are considered only if OW = 1. During the READ/WRITE/FORMAT command, the drive selected in these commands is compared to Dn. If the bits match then perpendicular mode will be enabled for that drive. For example, if D0 is set then drive 0 will be configured for perpendicular mode.

GAP — This alters the Gap2 length as required by the perpendicular mode format.

WGATE — Write gate alters timing of WE to allow for pre-erase loads in perpendicular drives.

The VCOEN timing and the length of the Gap2 field (explained above) can be altered to accommodate the unique requirements of the 4 MB floppy drives by GAP and WGATE bits of the PR. Table 2 describes the effects of the GAP and WGATE bits for the perpendicular command.

82077AA/SL's PERPENDICULAR MODE SUPPORT

The 82077AA and 82077SL both support 4 MB recording mode. The 82077SL has power management features included as well. Both AA and SL product lines have three versions each out of which two of the versions support the 4 MB floppy drives. The 82077AA-1, 82077AA, 82077SL, and 82077SL-1 all support the 4 MB floppy drives. A single command puts the 82077AA/SL into the perpendicular mode. This mode also requires the data rate to be set at 1 Mbps. The FIFO that is unique to Intel's 82077AA/SL parts may become necessary to remove the host interface bottleneck due to the higher data rate. The 4 MB floppy disk drives are downward compatible to 1 MB and 2 MB floppy diskettes. The following discussion explains the implications of the new 4 MB combination head and the functionality of the perpendicular mode command.

Table 2. Effects of GAP and WGATE Bits

GAP	WGATE	Mode	VCO Low Time after Index Pulse	Length of Gap2 Format Field	Portion of Gap2 Written by Write Data Operation	Gap2 VCO Low Time for Read Operations
0	0	Conventional	33 Bytes	22 Bytes	0 Bytes	24 Bytes
0	1	Perpendicular (Data Rate = 500 kbps)	33 Bytes	22 Bytes	19 Bytes	24 Bytes
1	0	Conventional	33 Bytes	22 Bytes	0 Bytes	24 Bytes
1	1	Perpendicular	33 Bytes	41 Bytes	38 Bytes	43 Bytes

The implementation of 4 MB drives requires understanding the Gap2 (see Figures 2a and 2b) and VCO timing requirements unique to these drives. These new requirements are dictated by the design of the "combination head" in these drives. Rewriting of disks in the 4 MB drives requires a pre-erase gap to erase the magnetic flux on the disk preceding the writing by the read/write gap. The read/write gap in the 4 MB drive does not have sufficient penetration (as shown in Figure 4a) to overwrite the existing data. In the conventional drives, the read/write gap had sufficient depth and could effectively overwrite the older data as depicted in Figure 4b. It must be noted that it is necessary to write the conventional 2 MB media in the 4 MB drive at 500 Kbps perpendicular mode. This ensures proper erasure of existing data and reliable write of the new data. The pre-erase gap in the 4 MB floppy drives is activated only during format and write commands. Both the pre-erase gap and read/write gap are activated at the same time.

As shown in Figure 4a, the pre-erase gap precedes the read/write gap by 200mm. This distance translated to bytes is about 38 bytes at a data rate of 1 Mbps and 19 bytes at 500 Kbps. Whenever the read/write gap is enabled by the Write Gate signal the pre-erase gap is activated at the same time.

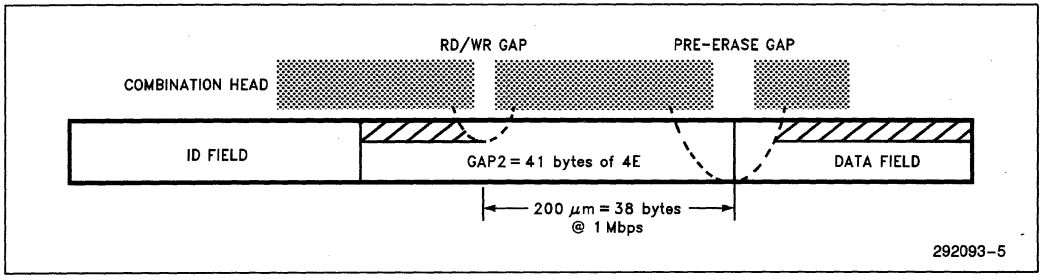


Figure 4a. Head Design for the 4 MB Perpendicular Mode

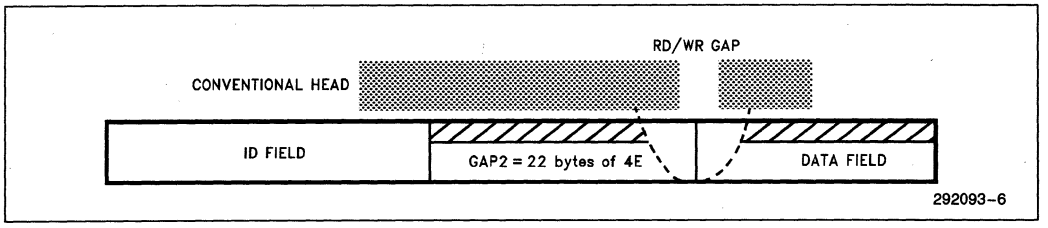


Figure 4b. Head Design for the Conventional 2 MB Mode

In conventional drives, the Write Gate is asserted at the beginning of the sync field, i.e., when the read/write is at the beginning of the data field. The controller then writes the new sync field, data address mark, data field and CRC (see Figure 2a). With the combination head, the read/write gap must be activated in the Gap2 field to ensure proper write of the new sync field. To accommodate both the distance between the pre-erase gap and read/write gap and the head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes at 1 Mbps (see Figure 2b). Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field at 500 Kbps data rate in the perpendicular mode.

On the read back by the 82077AA/SL, the controller must begin the synchronization at the beginning of the sync field. For conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. However, at 1 Mbps perpendicular mode the VCOEN goes active after 43 bytes to accomodate the increased Gap2 field size. For each case, a 2 byte cushion is maintained from the beginning of the sync field to avoid write splices caused by motor speed variation.

It should be noted that none of the alterations in Gap2 size, VCO timing or Write Gate timing affect the normal program flow. Once the perpendicular command is invoked, 82077AA/SL behaviour from the user standpoint is unchanged.

PROGRAMMING PERPENDICULAR MODE

Figures 5a and 5b show a flowchart on how the perpendicular recording mode is implemented on the 82077AA/SL. The perpendicular mode command can be issued during initialization. As shown in Figure 5a the perpendicular command stores the PR value internally. This value is used during the data transfer commands for configuration in order to deal with the perpendicular drives. Table 2 shows how the Gap2 length, VCOEN timing or Write Gate timing is affected. The OW bit is also tested for in this part of the loop. The enhanced perpendicular mode is enabled by setting the OW = 1, setting the Dn bits corresponding to the installed perpendicular drive high and leaving PR[0:1] = '00'.

As shown in Figure 5b, the Gap2 length is initially set to the conventional length of 22 bytes. Next the PR[0:1] bits (GAP, WGATE) are checked if they are set to '00'. If the PR[0:1] bits are set to '10' then, perpendicular mode is disabled and conventional mode is retained. If the PR[0:1] = '01' or '11' the VCOEN is

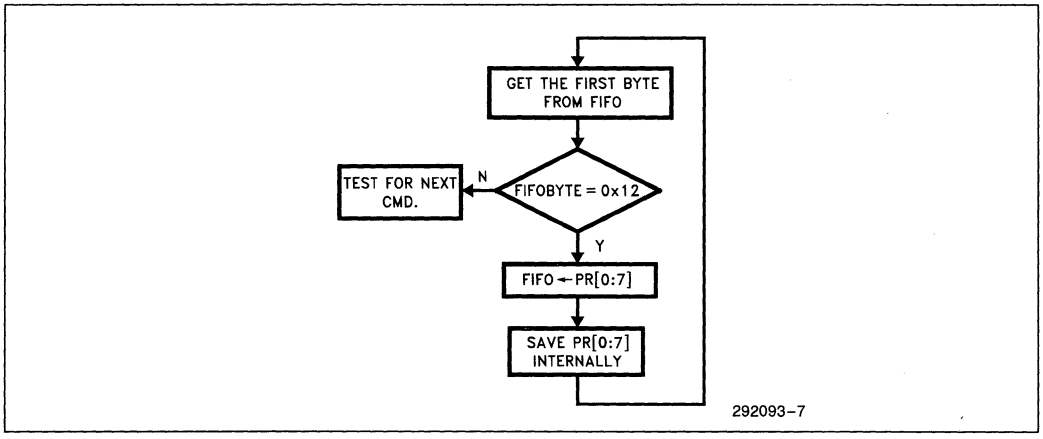


Figure 5a. Perpendicular Command Handling

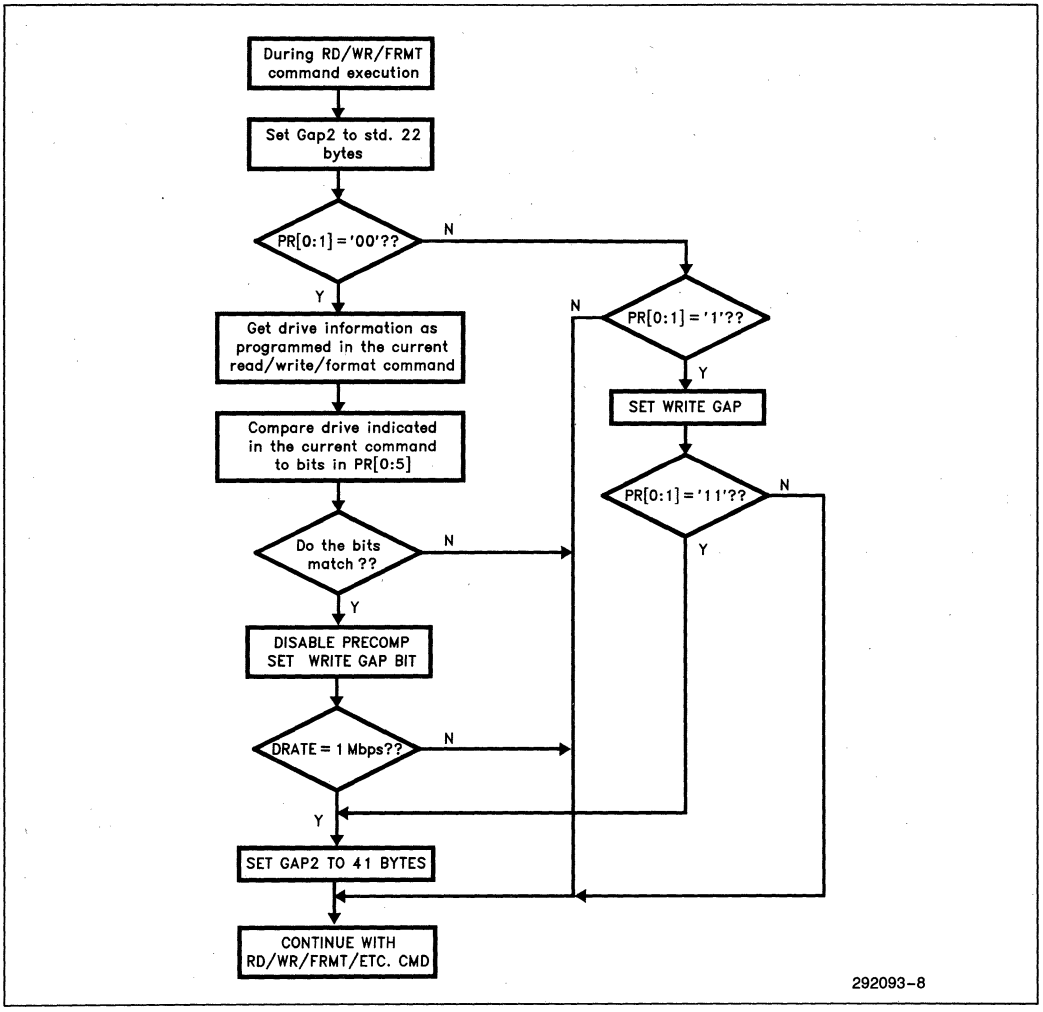


Figure 5b. During Data Transfer Commands

set to activate 43 bytes or 24 bytes from the start of the Gap2 field, depending on the value as shown in Table 2. After this, PR[0:1] = '11' is checked; if not true (programmed '01') the program is exited with only the VCOEN timing being set for perpendicular mode. If true, however, the Gap2 length is set up for perpendicular mode (note: this is done independent of the data rate). It must be noted that if the PR[0:1] bits are set to '11' then it is up to the user to disable precompensation before accessing perpendicular drives. The other branch of the flowchart refers to setting of PR[0:1] to '00'. In this case, the perpendicular command will have the following effect:

1. If any of the Dn bits in PR[2:5] programmed high, then precompensation is automatically disabled (0 ns is selected for the specified drive regardless of the data rate) and VCOEN is set to activate appropriately. All the bits that are set low will enable the 82077 to be configured for conventional mode, i.e., exit the program without modifications (shown Figure 5b).
2. Next the data rate is checked for 1 Mbps. If the data rate is at 1 Mbps, then Gap2 length is set to 41 bytes, otherwise, the program is exited without setting up the Gap2 to 41 bytes.

It must be noted that if PR[2:5] are to be recognized in the command the OW bit must be set high. If this bit is low, setting of Dn bits will have no effect. Setting the OW bit will enable the storage of the Dn bit. Also setting PR[0:1] to any other value than '00' will override anything written in the Dn bits. In other words, setting PR[0:1] to a value other than '00' enables the effect of that for all drives. It must be noted that if PR[0:1] bits are set to a value other than '00' then it is recommended not to use the enhanced command mode, i.e., all other bits should be zero. Consider the following examples:

a. PR[0:7] = 0x84; This is the way to use the command in the enhanced mode. In this case, the OW = 1 and D0 is set high. During the data transfer command, if D0 is selected it will be automatically configured for perpendicular mode. If D1 is accessed, however, it will be configured for conventional mode. Similarly, if PR[0:7] = 0x88 then D1 is configured for perpendicular mode and D0 is configured for conventional mode. Software resets do not clear this mode.
b. PR[0:7] = 0x03; This is the way to use the command in the old mode. If the user decides to use this mode, then it must be noted that the command has to be issued before every data transfer command. Also when used this way, all the drives are configured for perpendicular mode. The user must also remember to disable precompensation and set the data rate to 1 Mbps while accessing the perpendicular drive in the system. Any software reset clears the command.
c. PR[0:7] = 0x87; In this case, the OW = 1, D0 = 1 and PR[0:1] = 11. This may be called a mixed mode and should be refrained from usage. This is similar to setting PR[0:7] = 0x03, because setting PR[0:1] high overrides automatic configuration. In this case the user has to be aware that precompensation must be disabled and the data rate must be set to 1 Mbps while accessing drive 0. After software reset, bits GAP and WGATE will be cleared, but OW and D0 will retain their previously set values. In other words, after software reset, the part will see PR[0:7] = 0x84. Evidently, this would cause problems and, therefore, it is recommended this mode *not* be used.
d. PR[0:7] = 0x80; In this case, the OW = 1, Dn = 0 and PR[0:1] = 00. This has the effect of clearing the perpendicular mode command without doing a hardware reset. Another way to do this would be to set PR[0:7] = 0x02; this can then be used to temporarily disable perpendicular mode configuration without affecting the previously programmed Dn values. Software reset following this will reenable the previously programmed enhanced mode command.

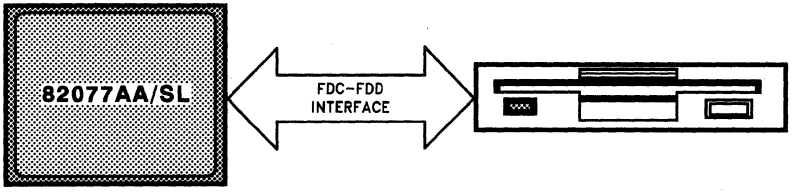
Using the enhanced perpendicular command removes the requirement of issuing the perpendicular command for each data transfer command and manually setting the perpendicular configuration.

"Software" RESETs (via DOR or DSR registers) will only clear the PR[0:1] values to '0'. Dn bits will retain their previously programmed values. "Hardware" RESETs will clear all the programmed bits including OW and Dn bits to '0'. The status of these bits can be determined by issuing the dumpreg command and checking the 8th result byte. This byte will contain the programmed values of the Dn and PR[0:1] bits as shown in Figure 6. The OW bit is *not* returned in this result byte.

Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
DUMPREG COMMAND										
Command	R	Eighth Result Byte: LOCK	0	D3	D2	D1	D0	GAP	WGATE	

Figure 6. Dumpreg Command

INTERFACE BETWEEN 82077AA/SL AND THE DRIVE



292093-9

There is currently no industry-wide standard for the FDC to FDD interface. There are numerous floppy drive vendors, each with their own modes and interface pins to enable 4 MB perpendicular mode. The drive interface not only varies from manufacturer to manufacturer but also within a manufacturer's product line. The differences on the interface mainly originate from configuring the floppy drive into the 4 MB mode. Depending on the drive, the differences can create problems of daisy-chaining a 4 MB drive with the standard 1 MB and 2 MB drives. Of course, for laptops this is not a problem since most of them use a single floppy drive. Lack of an industry standard makes it necessary to look at each drive and build a interface for that particular drive.

The following is a brief discussion about some of the floppy drives available in the market and how these can be interfaced with the 82077AA/SL. It is important to note that although a manufacturer's name may be given in connection with the interface described, Intel does not guarantee that the interface discussed will apply to all the drives from that manufacturer. The main goal is introduce to the reader how to interface the 82077AA/SL with a 4 MB floppy drive.

Previously, for the conventional 1 MB and 2 MB AT mode drives, a single Density Select input was used by floppy drives to select between high density and low density drives. A high on this input enabled high density operation (500 Kbps) whereas a low enabled low density operation (300 Kbps/250 Kbps). This signal was asserted high or low by the floppy disk controller depending on the data rate programmed. For the 4 MB operation, there are two inputs defined by the floppy drive manufacturers. The polarity of these inputs enables the selected density operation. Implementing this requires at least 1 new pin to be defined on the FDC-FDD interface. Most floppy vendors have elected to take pin 2 (originally density select) and redefine the polarity to conform to one of these new density select inputs and another pin to be the other density select input. However, the new density select on pin 2 is not compatible to the old density select input in many of the floppy drives. This precludes the user from daisy chaining 4 MB drives with conventional drives. Another problem is that the second density select pin varies on its location on the FDC-FDD interface from drive to drive.

The way that the BIOS determines what type of diskette is in what type of drive is by trial and error. The system tries to read the diskette at 250 Kbps; if it fails then it will set the data rate to higher value and retry. The BIOS does this until the right data rate is selected. This method will still be implemented for the 4 MB drives by some BIOS vendors. However, the 4 MB drives available today also have two media sense ID pins that relate to the user what type of media is present in the floppy drive. This information will also require two pins on the FDC-FDD interface. The location of these pins is once again variable from drive to drive.

Some manufacturers have circumvented the entire standardization problem by including an auto configuration in the drive. In these cases, the type of floppy put into the drive is sensed by the hole (each 4/2/1 MB diskette has a hole in different locations identifying it) on the diskette. Then the drive automatically sets itself up for this mode. The BIOS must obviously set up the floppy disk controller for the correct data rate which could be done if the media sense ID was read and decoded as to the data rate. Due to lack of extra pins on the even side of the floppy connector the newer locations of some of the functions are migrating to the odd pins (previously all grounded). Some drive manufacturers have even made this configurable via jumpers. For instance, the new TEAC drives have a huge potpourri of configurations that would satisfy the appetite of some of the most finicky system interfaces.

The 82077AA/SL currently has two output pins DRATE0 and DRATE1 (pins 28 and 29 respectively) which directly reflect the data rate programmed in the DSR and CCR registers. These two pins can be used to select the correct density on the drive. These two can also be used with the combination of DENSEL to select the correct data rate. At the present time the 82077AA/SL does not support media sense ID. However, the user could easily make it readable directly by BIOS. The following is a discussion on what combination of DRATE0, DRATE1, and DENSEL could be used to interface to some of the currently available floppy drives.

1. TEAC 235J-600/Toshiba PD-211/Sony (Old Version)

These were among the first 4 MB drives available in the market. Each of them has a mode select input on pins 2 and 6. The polarity required for each different data rate is as shown below:

Data Rate	Capacity	DRATE1	DRATE0	MODSEL0 pin 2	MODSEL1 pin 6
1 Mbps	4 MB	1	1	1	0
500 Kbps	2 MB	0	0	0	1
300 Kbps/ 1 Mbps	4 MB	0	1	1	1
250 Kbps	1 MB	1	0	0	0

It is clear from the above that DRATE0 = MODSEL0 and MODSEL1 = DRATE1#. This would mean taking the drate signals onto pins 2 and 6 of the FDC-FDD interface. Unfortunately this solution requires an inverting gate. TEAC has recently, however, come out with a new version called TEAC 235J-3653. On this drive there are a number of possible configurations into which the drive can be put into, however, only the best way to interface to the 82077AA/SL will be discussed. The requirements are as shown below. This shows that HDIN = DENSEL (original signal for conventional drives) and EDIN = DRATE0. As suggested in the TEAC spec for method 1, the straps connected are MSC, HI2 (sets HDIN on pin 2), DC34 and EI6 (sets EDIN on pin 6). Pins 4, 29, and 33 are left open. Since pin 2 has the same polarity as the conventional drive requirement and the secondary input is connected via pin 6 (no connect on the conventional drives) daisy chaining this TEAC drive with a conventional drive does not cause any incompatibility. Figure 7 shows how the TEAC can be connected to the 82077AA/SL. It also shows daisy chaining of the TEAC drive with a conventional drive.

Data Rate	Capacity	DENSEL	DRATE1	DRATE0	HDIN pin 2	EDIN pin 6
1 Mbps	4 MB	1	1	1	X	1
500 Kbps	2 MB	1	0	0	1	0
300 Kbps/ 1 Mbps	4 MB	0	0	1	X	1
250 Kbps	1 MB	0	1	0	0	0

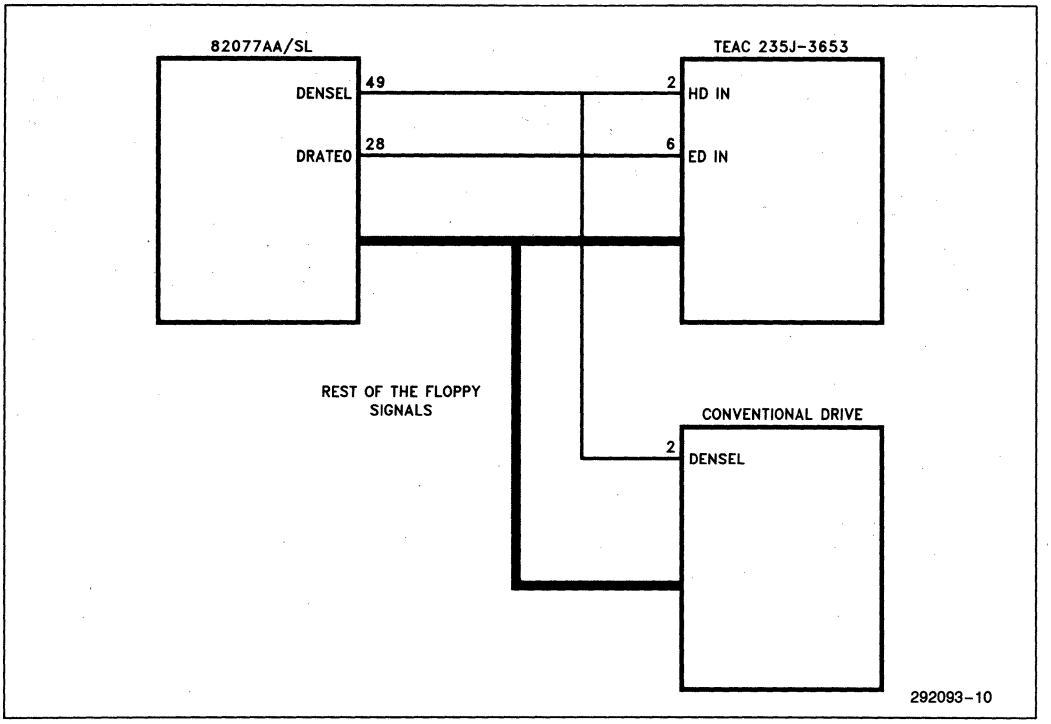


Figure 7. Interfacing 82077AA/SL to TEAC 235J-3653

2. Panasonic JU-259A (New Version)

This is Panasonic's new drive and has the HDIN signal on pin 2 and EDIN signal on pin 6. The requirements are shown below. This type of interface allows for daisy chaining the Panasonic drive with a conventional drive. The DENSEL signal can be connected to pin 2 and the DRATE0 should be connected to pin 6.

Data Rate	Capacity	DENSEL	DRATE1	DRATE0	HDIN pin 2	EDIN pin 6
1 Mbps	4 MB	1	1	1	1	1
500 Kbps	2 MB	1	0	0	1	0
300 Kbps/ 1 Mbps	4 MB	0	0	1	0	1
250 Kbps	1 MB	0	1	0	0	0

3. Mitsubishi MF356C (Model 252UG/788UG)

There are two models of this drive. The 252UG has DENSEL1 on pin 2 and DENSEL0 on pin 33, whereas the 788UG has DENSEL0 located on pin 2 and DENSEL1 located on pin 6. Via jumpers, it is possible to configure the drives to different polarity for the density select line. The following table shows the configuration for the 252UG in which jumper setting is 2MS = I/F and 4 MS = I/F.

Data Rate	Capacity	DENSEL	DRATE1	DRATE0	DENSEL1 pin 2	DENSEL0 pin 33
1 Mbps	4 MB	1	1	1	1	1
500 Kbps	2 MB	1	0	0	1	0
300 Kbps/ 1 Mbps	4 MB	0	0	1	0	1
250 Kbps	1 MB	0	1	0	0	0

The correct connection requirement is: DENSEL (from 82077AA/SL) = DENSEL1 and DRATE0 = DENSEL0. Although there are other configurations, this provides the best one, since daisy chaining is possible without any problem.

4. Epson SMD-1060

This drive has 3 different modes of operation. Mode B is the best and is similar to Mitsubishi's drives as described above. In this mode, HDI signal is connected to pin 2 and EDI is connected to pin 33. Mode B is enabled by inserting jumpers across 3-4 and 7-8 (SS01 B block) and 1-2 and 3-4 (SS03 block) for the drive with the power separated type (i.e., a connector for the floppy signals and another one for power supply) of 34-pin connector.

Data Rate	Capacity	DENSEL	DRATE1	DRATE0	HDI pin 2	EDI pin 33
1 Mbps	4 MB	1	1	1	1	1
500 Kbps	2 MB	1	0	0	1	0
300 Kbps/ 1 Mbps	4 MB	0	0	1	0	1
250 Kbps	1 MB	0	1	0	0	0

As demonstrated by the table, HDI = DENSEL and EDI = DRATE0. These connections would ensure daisy chaining capability without any problems.

5. Sony MP-F40W-14/15

The dash 14 and 15 are two drives from Sony that handle 4 MB requirements. The MP-F40W-14 has the DENSITY SELECT 1, DENSITY SELECT 0 on pins 2 and 33 respectively, whereas the MP-F40W-15 has the DENSITY SELECT 1, DENSITY SELECT 0 on pins 2 and 6 respectively. As it is obvious from the table below, daisy chaining is easily done if the 82077AA/SL is connected in the PS/2 mode (by tying IDENT low) with either type of drive, the only difference being the location of DENSITY SELECT 0.

Data Rate	Capacity	DENSEL PS/2 mode (IDENT = 0)	DRATE1	DRATE0	DENSITY SELECT1 pin 2	DENSITY SELECT0 pin 6/33
1 Mbps	4 MB	0	1	1	0	1
500 Kbps	2 MB	0	0	0	0	0
300 Kbps/ 1 Mbps	4 MB	1	0	1	1	1
250 Kbps	1 MB	1	1	0	1	0

If the drive is used in the PS/2 mode, then DENSITY SELECT1 = DENSEL and DENSITY SELECT0 = DRATE0. To use the drive in AT mode, DENSITY SELECT1 = DRATE1 and DENSITY SELECT0 = DRATE0, as shown below. However, daisy chaining is not possible.

Data Rate	Capacity	DENSEL PS/2 mode (IDENT = 0)	DRATE1	DRATE0	DENSITY SELECT1 pin 2	DENSITY SELECT0 pin 6/33
1 Mbps	4 MB	0	1	1	1	1
500 Kbps	2 MB	0	0	0	0	0
300 Kbps/ 1 Mbps	4 MB	1	0	1	0	1
250 Kbps	1 MB	1	1	0	1	0

6. Toshiba ND3571

Toshiba MB drive has the HD mode selection on pin 6 and ED mode selection on pin 2. This causes daisy chaining problems with conventional drives as shown in the figure below:

Data Rate	Capacity	DENSEL	DRATE1	DRATE0	ED Mode pin 2	HD Mode pin 6
1 Mbps	4 MB	1	1	1	1	1
500 Kbps	2 MB	1	0	0	0	1
300 Kbps/ 1 Mbps	4 MB	0	0	1	1	0
250 Kbps	1 MB	0	1	0	0	0

The DENSEL from the 82077 is connected to pin 6 and DRATE0 is connected to pin 2.

82077SL 4 MB DESIGN

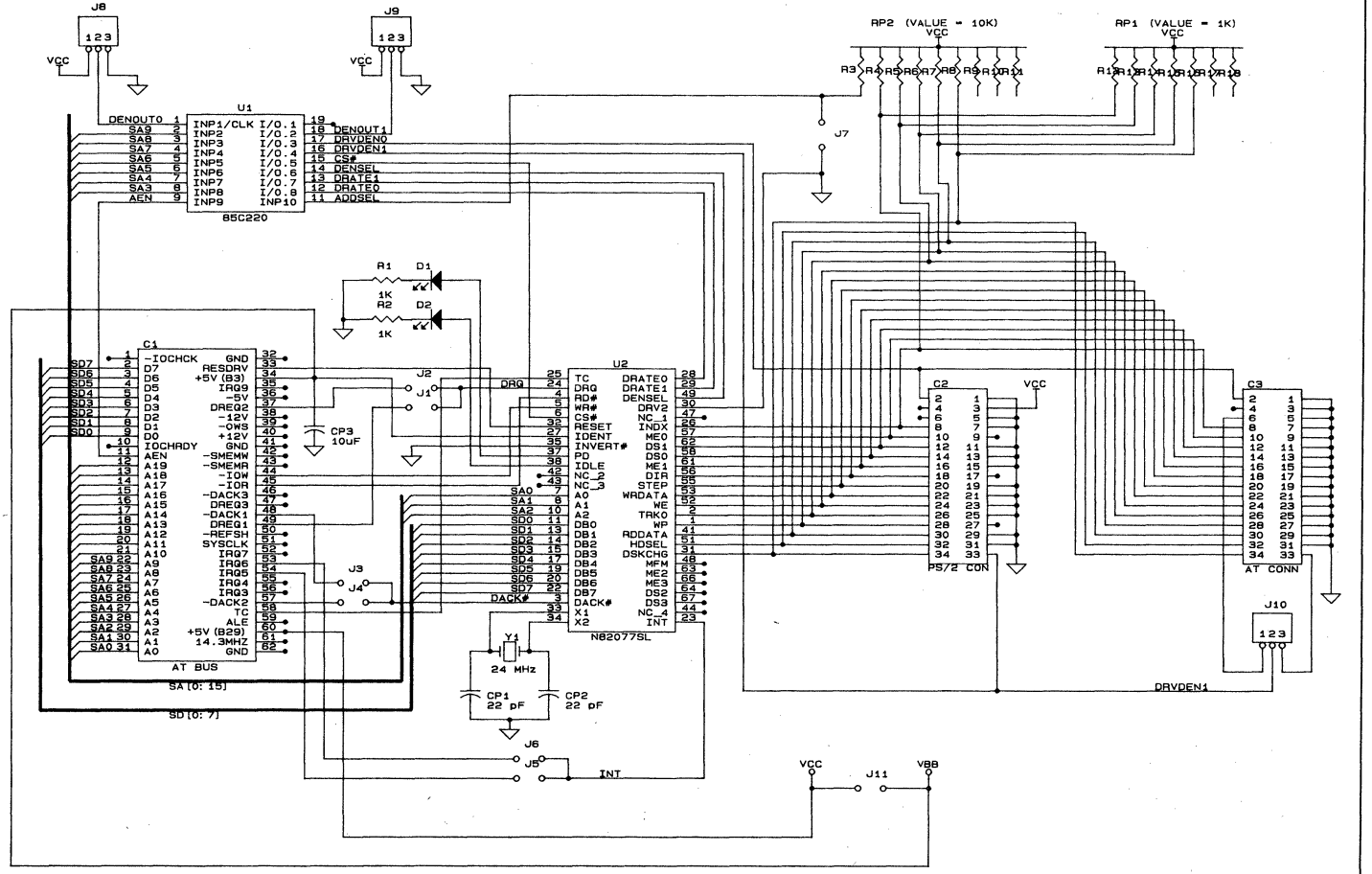
This section presents a design application of a PC/AT compatible floppy disk controller. The 82077SL integrates the entire PC/AT controller design with the exception of the address decode on a single chip. The schematic for this solution is shown in Figure 8. The chip select for the 82077SL is generated by a 85C220 μPLD that is programmed to decode addresses 03F0H through 03F7H when AEN is low. The programming equations for the μPLD is in the Intel's .ADF format and can be processed using the IPLSII compiler (available from Intel).

A floppy disk interface is provided by on-chip output buffers with a 40 mA sink capability. The outputs from the disk drive are terminated at the floppy disk controller with a 1 KΩ resistor pack. The 82077SL disk interface inputs contain a Schmitt trigger input structure for higher noise immunity. The host interface is a similar direct connection with on-chip 12 mA sink capable buffers on DB0–7, INT and DRQ.

The schematic shows eleven jumpers numbered J1 through J11. The table below describes the functions of these jumpers as well as their normal connections. The normal connections allow the BIOS to work without modification. In the normal mode, the 82077SL responds to DRQ2 and DACK2# as well as IRQ6. Depending on the type of drive interfaced to this board, the DENOUT0 and DENOUT1 signals can be tied. With the setting to 2–3 on J8 and J9, the default setting is DENSEL on DRVDEN0 and DRATE0 on DRVDEN1. PIN6/33 SELECT is used to set for pin 6 as the EDIN input. The J11 should always be closed. It can be used to measure the current consumption of 82077SL. J7 selects between the primary and secondary address spaces. There are two resistor packs used for pullups on input signals from the floppy drive interface. These resistors are rated at 1K. Please note that if using older 5.25″ drives, the pullup on some of them is 150Ω. Most modem 5.25″ drives use a 1K value. In order to ensure the correct value please refer to the floppy drive specification manual.

For further information, please contact your local Intel sales office.

Jumper	Description	Normal Connection
J1	DRQ1: DMA request 1 used with DACK1# to allow for DMA transfers	Open
J2	DRQ2: DMA request 2 used with DACK2# to allow for DMA transfers	Closed
J3	DACK1: DMA acknowledge 1 used with DRQ1 to allow for DMA transfers	Open
J4	DACK2: DMA acknowledge 2 used with DRQ2 to allow for DMA transfers	Closed
J5	IRQ5: Interrupt line 5 used to generate floppy interrupts	Open
J6	IRQ6: Interrupt line 6 used to generate floppy interrupts	Closed
J7	DRV2: Address selection (between 3FX and 37X address ranges)	Open
J8	DENOUT0: Used with DENOUT1 to select the values of DRVDEN1,0	2–3
J9	DENOUT1: Used with DENOUT0 to select the values of DRVDEN1,0	2–3
J10	PIN6/33 SELECT: Used to select between pin 6 and pin 33 for EDIN input	1–2 or 2–3
J11	V_{BB}/V_{CC}: Connection between two power layers	Closed



292093-11

Figure 8. 82077SL Evaluation Board

```
Designer: K. Shah
Company: Intel Corp.
Dept:    IMD Marketing
Date:    April '92
Rev.#:
% The µPLD used in the 82077SL Evaluation board design, Rev.#1.0. %
85C220 dip package

OPTIONS: TURBO = ON

PART:    85C220

INPUTS:
        SA9@2, % System Address Inputs %
        SA8@3,
        SA7@4,
        SA6@5,
        SA5@6,
        SA4@7,
        SA3@8,
        AEN@9,

        DENOUT0@1, % Maps the DRVDEN0 and DRVDEN1 to appropriate polarity table %
        DENOUT1@18, % Maps the DRVDEN0 and DRVDEN1 to appropriate polarity table %

        ADDSEL@11, % Selects between primary and secondary address spaces %

        DRATE0@12, % DRATE0 signal from the 82077SL %
        DRATE1@13, % DRATE1 signal from the 82077SL %
        DENSEL@14 % DENSEL signal from the 82077SL %

OUTPUTS:
        CS_@15, % 82077SL chip select signal %

        DRVDEN1@16, % Drive density signal connected to EDIN of the drive %
        DRVDEN0@17 % Drive density signal connected to HDIN of the drive %

NETWORK:
        % Inputs %

        SA9 = INP(SA9)
        SA8 = INP(SA8)
        SA7 = INP(SA7)
        SA6 = INP(SA6)
        SA5 = INP(SA5)
        SA4 = INP(SA4)
        SA3 = INP(SA3)
        AEN = INP(AEN)
        ADDSEL = INP(ADDSEL)
        DRATE0 = INP(DRATE0)
        DRATE1 = INP(DRATE1)
        DENSEL = INP(DENSEL)
        DENOUT0 = INP(DENOUT0)
        DENOUT1 = INP(DENOUT1)

        % Outputs %

        CS_ = CONF(CSeq, VCC)

        DRVDEN0 = CONF(DEN0eq, VCC)
        DRVDEN1 = CONF(DEN1eq, VCC)
```

```
EQUATIONS:

        % CS_is activated for 3F0-3F7 and 370-377 address spaces %
        CSeq = (AEN' * SA9 * SA8 * SA7' * SA6 * SA5 * SA4 * SA3' * ADDSEL'
               + AEN' * SA9 * SA8 * SA7 * SA6 * SA5 * SA4 * SA3' * ADDSEL)';

        % These are the signals generated on DRVDEN0 and DRVDEN1 for the FDC-FDD
          interface
        DENOUT1  DENOUT0  DRVDEN0  DRVDEN1
             0     0      DENSEL   DRATE0
             0     1      DENSEL'  DRATE0
             1     0      DRATE1   DRATE0
             1     1      DRATE0   DRATE1
        %

        DEN0eq = DENSEL * (DENOUT0' * DENOUT1') + DENSEL' * (DENOUT0 * DENOUT1')
                 + DRATE1 * (DENOUT0' * DENOUT1) + DRATE0 * (DENOUT0 * DENOUT1);
        DEN1eq = DRATE1 * (DENOUT0 * DENOUT1) + DRATE0 * (DENOUT0' + DENOUT1');

END$
```

82077SL Application Note Revision Summary

The following changes have been made since revision 001:

Table 2 kBps was corrected to kbps.

Page 12 3. Mitsubishi MF356C description modified to read: "There are two models of this drive. The 252UG has DENSEL1 on pin 2 and DENSEL0 on pin 33, whereas the 788UG has DENSEL0 located on pin 2 and DENSEL1 located on pin 6. Via jumpers, it is possible to configure the drives to different polarity for the density select lines. The following table shows the configuration for the 252UG in which jumper setting is 2 MS = I/F and 4 MS = I/F."

Figure 8 Arrow added to diagram.

Page 17 Columns corrected to line up properly.

intel®

3

Memory Controllers

8206
ERROR DETECTION AND CORRECTION UNIT

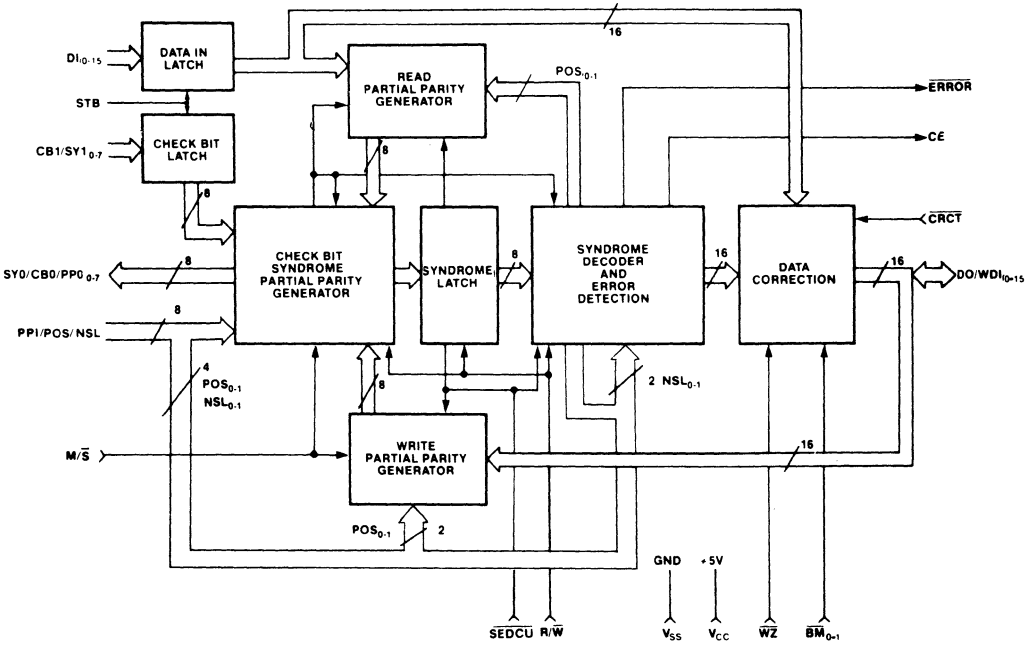
- **Detects All Single Bit, and Double Bit and Most Multiple Bit Errors**
- **Corrects All Single Bit Errors**
- **3 Selections**

	8206-1	8206
Detection	35 ns	42 ns
Correction	55 ns	67 ns

- **Syndrome Outputs for Error Logging**
- **Automatic Error Scrubbing with 8207**
- **Expandable to Handle 80 Bit Memories**
- **Separate Input and Output Busses—No Timing Strobes Required**
- **Supports Read With and Without Correction, Writes, Partial (Byte) Writes, and Read-Modify-Writes**
- **HMOS III Technology for Low Power**
- **68 Pin Leadless JEDEC Package**
- **68 Pin Grid Array Package**

The HMOS 8206 Error Detection and Correction Unit is a high-speed device that provides error detection and correction for memory systems (static and dynamic) requiring high reliability and performance. Each 8206 handles 8 or 16 data bits and up to 8 check bits. 8206's can be cascaded to provide correction and detection for up to 80 bits of data. Other 8206 features include the ability to handle byte writes, memory initialization, and error logging.

3



205220-1

Figure 1. 8206 Block Diagram

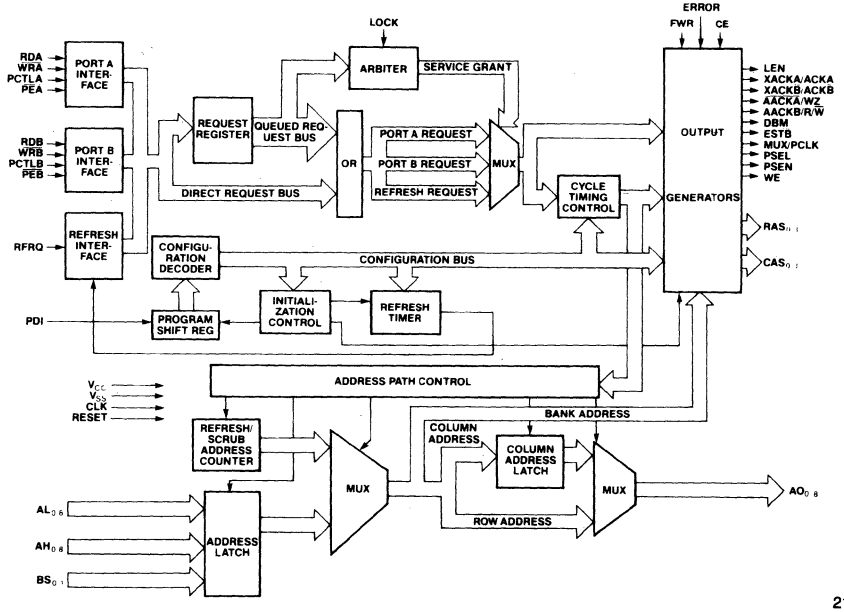
The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1987
Order Number: 205220-008

8207
DUAL-PORT DYNAMIC RAM CONTROLLER

- **Provides All Signals Necessary to Control 16K, 64K and 256K Dynamic RAMs**
- **Directly Addresses and Drives up to 2 Megabytes without External Drivers**
- **Supports Single and Dual-Port Configurations**
- **Automatic RAM Initialization in All Modes**
- **Four Programmable Refresh Modes**
- **Transparent Memory Scrubbing in ECC Mode**
- **Fast Cycle Support for 8 MHz 80286 with 8207-16**
- **Slow Cycle Support for 8 MHz, 10 MHz 8086/88, 80186/188 with 8207-8, 8207-10**
- **Provides Signals to Directly Control the 8206 Error Detection and Correction Unit**
- **Supports Synchronous or Asynchronous Operation on Either Port**
- **68 Lead JEDEC Type A Leadless Chip Carrier (LCC) and Pin Grid Array (PGA), Both in Ceramic.**

The Intel 8207 Dual-Port Dynamic RAM Controller is a high-performance, systems-oriented, Dynamic RAM controller that is designed to easily interface 16K, 64K and 256K Dynamic RAMs to Intel and other microprocessor systems. A dual-port interface allows two different busses to independently access memory. When configured with an 8206 Error Detection and Correction Unit the 8207 supplies the necessary logic for designing large error-corrected memory arrays. This combination provides automatic memory initialization and transparent memory error scrubbing.



210463-1

Figure 1. 8207 Block Diagram

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

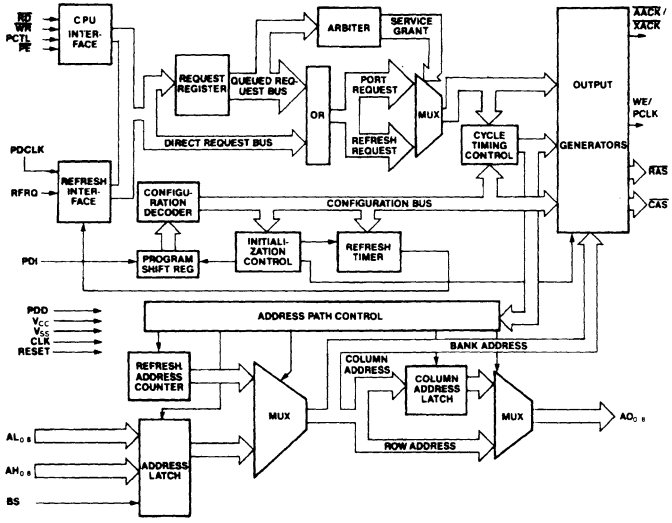
September 1987
Order Number: 210463-007

82C08
CHMOS DYNAMIC RAM CONTROLLER

- **0 Wait State with INTEL μProcessors**
- **iAPX 286 (10, 8 MHz) } 82C08-20 20 MHz, 82C08-16 16 MHz**
  iAPX 186/88 86/88 } 82C08-10 10 MHz, 82C08-8 8 MHz
- **Supports 64K and 256K DRAMs (256K x 1 and 256K x 4 Organizations)**
- **Power Down Mode with Programmable Memory Refresh using Battery Backup**
- **Directly Addresses and Drives up to 1 Megabyte without External Drivers**
- **Microprocessor Data Transfer and Advance Acknowledge Signals**
- **Five Programmable Refresh Modes**
- **Automatic RAM Warm-up**
- **Pin-Compatible with 8208**
- **48 Lead Plastic DIP; 68 Lead PLCC**
  (See Intel Packaging; Order Number: 231369-001)
- **Compatible with Normal Modes of Static Column and Ripplemode DRAMs**

The Intel 82C08 Dynamic RAM Controller is a CMOS, high performance, systems oriented, Dynamic RAM controller that is designed to easily interface 64K and 256K Dynamic RAMs to Intel and other microprocessors. The 82C08 also has a power down mode where only the refresh logic is activated using battery backup.

3



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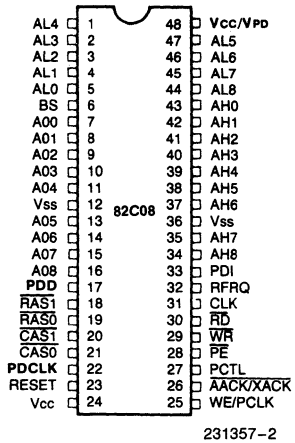

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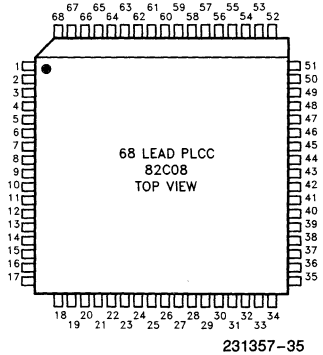

231357-35

Figure 1. Block Diagram and Pinout Diagrams

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1990
Order Number: 231357-008

intel®

4

UPI Keyboard Controllers

intel®

Microprocessor Peripherals
UPI-41A/41AH/42/42AH
User's Manual

4

March 1994

Order Number: 231318-006

Microprocessor Peripherals
UPI-41A/41AH/42/42AH User's Manual

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CHAPTER 1
INTRODUCTION

Accompanying the introduction of microprocessors such as the 8088, 8086, 80186 and 80286 there has been a rapid proliferation of intelligent peripheral devices. These special purpose peripherals extend CPU performance and flexibility in a number of important ways.

Table 1-1. Intelligent Peripheral Devices

8255 (GPIO)	Programmable Peripheral Interface
8251A(USART)	Programmable Communication Interface
8253 (TIMER)	Programmable Interval Timer
8257 (DMA)	Programmable DMA Controller
8259	Programmable Interrupt Controller
82077AA	Programmable Floppy Disk Controller
8273 (SDLC)	Programmable Synchronous Data Link Controller
8274	Programmable Multiprotocol-Serial Communications Controller
8275/8276 (CRT)	Programmable CRT Controllers
8279 (PKD)	Programmable Keyboard/Display Controller
8291A, 8292, 8293	Programmable GPIB System Talker, Listener, Controller

Intelligent devices like the 82077AA floppy disk controller and 8273 synchronous data link controller (see Table 1-1) can preprocess serial data and perform control tasks which off-load the main system processor. Higher overall system throughput is achieved and software complexity is greatly reduced. The intelligent peripheral chips simplify master processor control tasks by performing many functions externally in peripheral hardware rather than internally in main processor software.

Intelligent peripherals also provide system flexibility. They contain on-chip mode registers which are programmed by the master processor during system initialization. These control registers allow the peripheral to be configured into many different operation modes. The user-defined program for the peripheral is stored in main system memory and is transferred to the peripheral's registers whenever a mode change is required. Of course, this type of flexibility requires software overhead in the master system which tends to limit the benefit derived from the peripheral chip.

In the past, intelligent peripherals were designed to handle very specialized tasks. Separate chips were designed for communication disciplines, parallel I/O, keyboard encoding, interval timing, CRT control, etc. Yet, in spite of the large number of devices available and the increased flexibility built into these chips, there is still a large number of microcomputer peripheral control tasks which are not satisfied.

With the introduction of the Universal Peripheral Interface (UPI) microcomputer, Intel has taken the intelligent peripheral concept a step further by providing an intelligent controller that is fully user programmable. It is a complete single-chip microcomputer which can connect directly to a master processor data bus. It has the same advantages of intelligence and flexibility which previous peripheral chips offered. In addition, UPIs are user-programmable: it has 1K/2K bytes of ROM or EPROM memory for program storage plus 64/128/256 bytes of RAM memory UPI-41A, 41AH/42, 42AH respectively for data storage or initialization from the master processor. The UPI device allows a designer to fully specify his control algorithm in the peripheral chip without relying on the master processor. Devices like printer controllers and keyboard scanners can be completely self-contained, relying on the master processor only for data transfer.

The UPI family currently consists of seven components:

- 8741A microcomputer with 1K EPROM memory
- 8741AH microcomputer with 1K OTP EPROM memory
- 8041AH microcomputer with 1K ROM memory
- 8742 microcomputer with 2K EPROM memory
- 8742AH microcomputer with 2K "OTP" EPROM memory
- 8042AH microcomputer with 2K ROM memory
- 8243 I/O expander device

The UPI-41A/41AH/42/42AH family of microcomputers are functionally equivalent except for the type and amount of program memory available with each. In addition, the UPI-41AH/42AH family has a Signature Row outside the EPROM Array. The UPI-41AH/42AH family also has a Security Feature which renders the EPROM Array unreadable when set.

All UPI's have the following main features:

- 8-bit CPU
- 8-bit data bus interface registers
- Interval timer/event counter
- Two 8-bit TTL compatible I/O ports
- Resident clock oscillator circuits

The UPI family has the following differences:

Table 1-2

UPI-41A	UPI-42	UPI-41AH	UPI-42AH
1K x 8 EPROM	2K x 8 EPROM	1K x 8 ROM or 1K x 8 OTP	2K x 8 ROM or 2K x 8 OTP
64 x 8 RAM	128 x 8 RAM	128 x 8 RAM	256 x 8 RAM
		*Set Security Feature **Signature Row Feature 32 Bytes with: 1. Test Code/Checksum 2. Intel Signature 3. Security Byte 4. User Signature	
PROGRAMMING			
UPI-41A	**UPI-42**	**UPI-41AH/UPI-42AH**	
V_{DD} = 25V	21V	12.5V	
I_{DD} = 50 ms	50 mA	30 mA	
EA = 21.5V–24.5V	18V	12.5V	
V_{PH} = 21.5V–24.5V	18V	20.V–5.5V	
TPW = 50 ms	50 ms	1 ms	
PIN DESCRIPTION			
UPI-41A/UPI-42		**UPI-41AH/UPI-42AH**	
(T1) T1 functions as a test input which can be directly tested using conditional branching instructions. It functions as the event timer input under software control.		T1 functions as a test input that can be directly tested using conditional branching instructions. It works as the event timer input under software control. It is used during sync mode to reset the instruction state to S1 and synchronize the internal clock to phase 1.	
(SS) Single step input used with the sync output to step the program through each instruction.		Single step input used with the sync output to step the program through each instruction. This pin is used to put the device in sync mode by applying +12.5V to it.	
Port 1 (P10–P17): 8-bit, Quasi-Bidirectional I/O Lines.		Port 1 (P10–P17): 8-bit, Quasi-Bidirectional I/O Lines. P10–P17 access the Signature Row and Security Bit.	

NOTES:
*For a complete description of the Security Feature, refer to the UPI-41AH/42AH Datasheet.
**For a complete description of the Signature Row, refer to the UPI-41AH/42AH Datasheet.

HMOS processing has been applied to the UPI family to allow for additional performance and memory capability while reducing costs. The UPI-41A/41AH/42/42AH are all pin and software compatible. This allows growth in present designs to incorporate new features and add additional performance. For new designs, the additional memory and performance of the UPI-41A/41AH/42/42AH extends the UPI 'grow your own solution' concept to more complex motor control tasks, 80-column printers and process control applications as examples.

The 8243 device is an I/O multiplexer which allows expansion of I/O to over 100 lines (if seven devices are used). All three parts are fabricated with N-channel MOS technology and require a single, 5V supply for operation.

INTERFACE REGISTERS FOR MULTI-PROCESSOR CONFIGURATIONS

In the normal configuration, the UPI-41A/41AH/42/42AH interfaces to the system bus, just like any intelligent peripheral device (see Figure 1-1). The host processor and the UPI-41A/41AH/42/42AH form a loosely coupled multi-processor system, that is, communications between the two processors are direct. Common resources are three addressable registers located physically on the UPI-41A/41AH/42/42AH. These registers are the Data Bus Buffer Input (DBBIN), Data Bus Buffer Output (DBBOUT), and Status (STATUS) registers. The host processor may read data from DBBOUT or write commands and data into DBBIN. The status of DBBOUT and DBBIN plus user-defined status is supplied in STATUS. The host may read STATUS at any time. An interrupt to the UPI processor is automatically generated (if enabled) when DBBIN is loaded.

Because the UPI contains a complete microcomputer with program memory, data memory, and CPU it can function as a "Universal" controller. A designer can program the UPI to control printers, tape transports, or multiple serial communication channels. The UPI can also handle off-line arithmetic processing, or any number of other low speed control tasks.

POWERFUL 8-BIT PROCESSOR

The UPI contains a powerful, 8-bit CPU with as fast as 1.2 μsec cycle time and two single-level interrupts. Its instruction set includes over 90 instructions for easy software development. Most instructions are single byte and single cycle and none are more than two bytes long. The instruction set is optimized for bit manipulation and I/O operations. Special instructions are included to allow binary or BCD arithmetic operations, table look-up routines, loop counters, and N-way branch routines.

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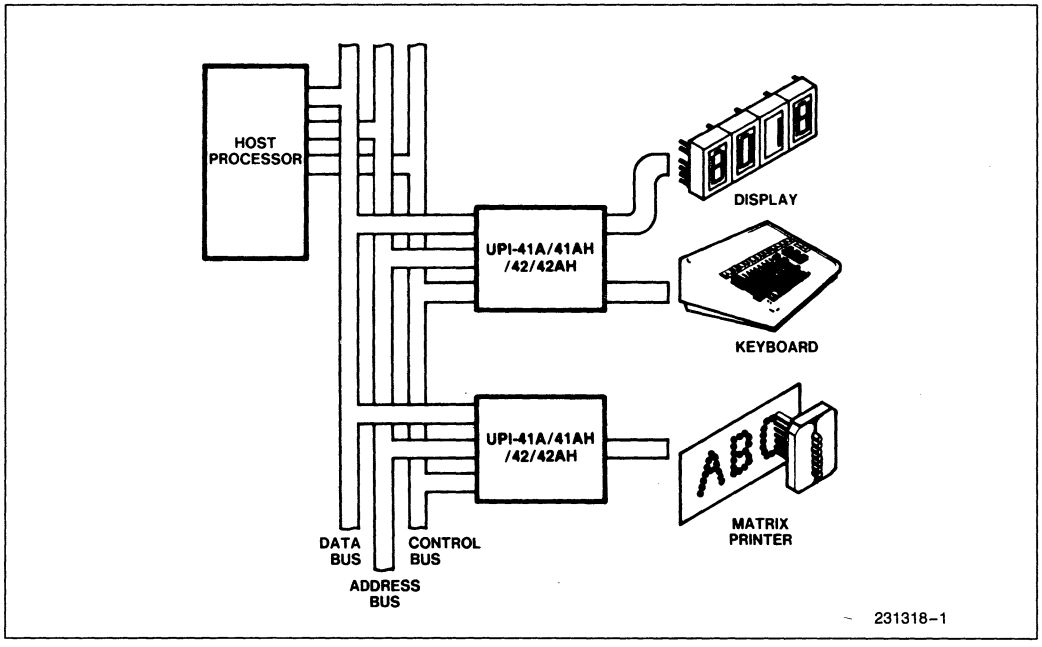


Figure 1-1. Interfacing Peripherals To Microcomputer Systems

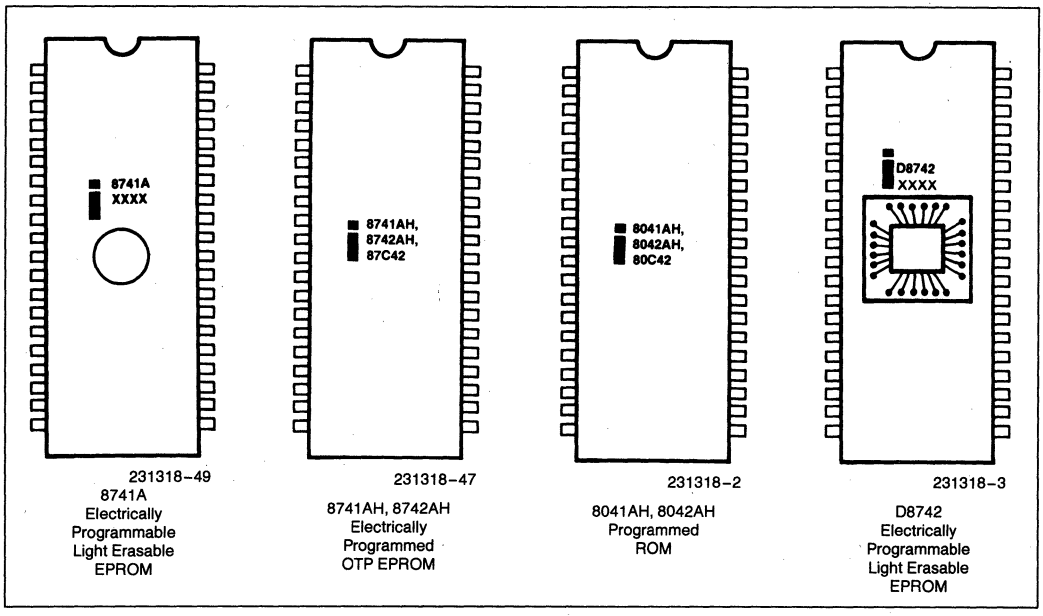


Figure 1-2. Pin Compatible ROM/EPROM Versions

SPECIAL INSTRUCTION SET FEATURES

- For Loop Counters:
  Decrement Register and Jump if not zero.
- For Bit Manipulation:
  AND to A (immediate data or Register)
  OR to A (immediate data or Register)
  XOR to A (immediate data or Register)
  AND to Output Ports (Accumulator)
  OR to Output Ports (Accumulator)
  Jump Conditionally on any bit in A
- For BDC Arithmetic:
  Decimal Adjust A
  Swap 4-bit Nibbles of A
  Exchange lower nibbles of A and Register
  Rotate A left or right with or without Carry
- For Lookup Tables:
  Load A from Page of ROM (Address in A)
  Load A from Current Page of ROM (Address in A)

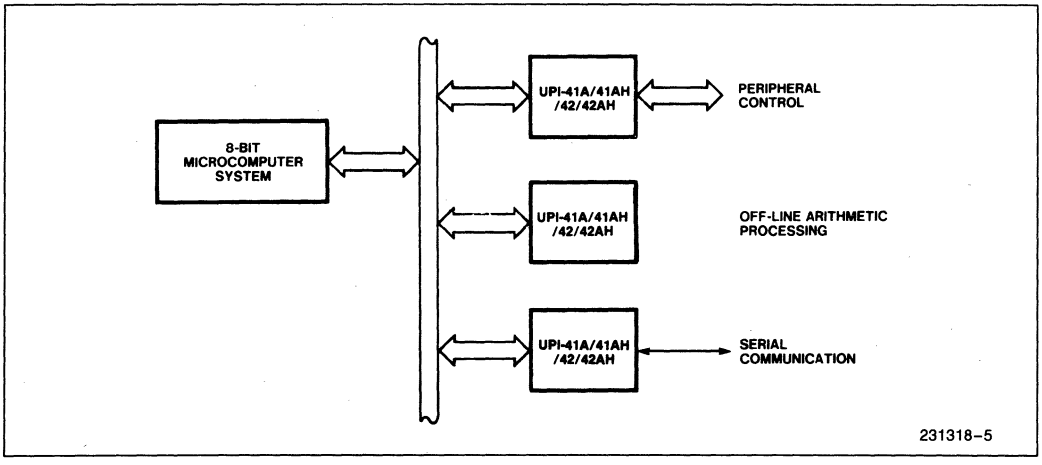


Figure 1-3. Interfaces and Protocols for Multiprocessor Systems

Features for Peripheral Control

The UPI 8-bit interval timer/event counter can be used to generate complex timing sequences for control applications or it can count external events such as switch closures and position encoder pulses. Software timing loops can be simplified or eliminated by the interval timer. If enabled, an interrupt to the CPU will occur when the timer overflows.

The UPI I/O complement contains two TTL-compatible 8-bit bidirectional I/O ports and two general-purpose test inputs. Each of the 16 port lines can individually function as either input or output under software control. Four of the port lines can also function as an interface for the 8243 I/O expander which provides four additional 4-bit ports that are directly addressable by UPI software. The 8243 expander allows low cost I/O expansion for large control applications while maintaining easy and efficient software port addressing.

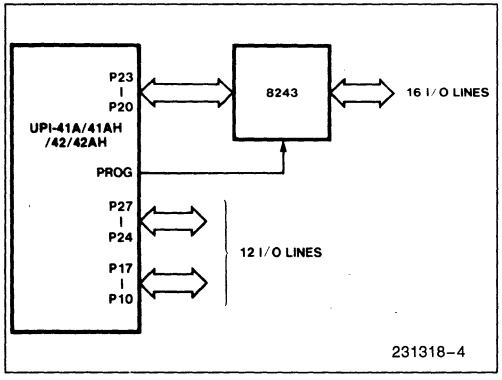


Figure 1-4. 8243 I/O Expander Interface

On-Chip Memory

The UPI's 64/128/256 bytes data memory include dual working register banks and an 8-level program counter stack. Switching between the register banks allows fast response to interrupts. The stack is used to store return addresses and processor status upon entering a subroutine.

The UPI program memory is available in three types to allow flexibility in moving from design to prototype to production with the same PC layout. The 8741A/8742 device with EPROM memory is very economical for initial system design and development. Its program memory can be electrically programmed using the Intel Universal PROM Programmer. When changes are needed, the entire program can be erased using UV lamp and reprogrammed in about 20 minutes. This means the 8741A/8742 can be used as a single chip "breadboard" for very complex interface and control problems. After the 8741A/8742 is programmed it can be tested in the actual production level PC board and the actual functional environment. Changes required during system debugging can be made in the 8741A/8742 program much more easily than they could be made in a random logic design. The system configuration and PC layout can remain fixed during the development process and the turn around time between changes can be reduced to a minimum.

At any point during the development cycle, the 8741A/8742 EPROM part can be replaced with the low cost UPI-41AH/42AH respectively with factory mask programmed memory or OTP EPROM. The transition from system development to mass production is made smoothly because the 8741A/8742, 8741AH and 8041AH, 8742AH and 8042AH parts are completely pin compatible. This feature allows extensive testing with the EPROM part, even into initial shipments to customers. Yet, the transition to low-cost ROMs or OTP EPROM is simplified to the point of being merely a package substitution.

PREPROGRAMMED UPI's

The 8242AH, 8292, and 8294 are 8042AH's that are programmed by Intel and sold as standard peripherals. Intel offers a complete line of factory programmed keyboard controllers. These devices contain firmware developed by Phoenix Technologies Ltd. and Award Software Inc. See Table 1-3 for a complete listing of Intels' entire keyboard controller product line. The 8292 is a GPIB controller, part of a three chip GPIB system. The 8294 is a Data Encryption Unit that implements the National Bureau of Standards data encryption algorithm. These parts illustrate the great flexibility offered by the UPI family.

Table 1-3. Keyboard Controller Family Product Selection Guide

UPI-42: The industry standard for desktop Keyboard Control.

Device	Package	ROM	OTP	Comments
8042	N, P	2K		ROM Device
8242	N, P			Phoenix firmware version 2.5
8242PC	N, P			Phoenix MultiKey/42 firmware, PS/2 style mouse support
8242WA	N, P			Award firmware version 3.57
8242WB	N, P			Award firmware version 4.14, PS/2 style mouse support
8742	N, P, D		2K	Available as OTP (N, P) or EPROM (D)

UPI-C42: A low power CHMOS version of the UPI-42. The UPI-C42 doubles the user programmable memory size, adds Auto A20 Gate support, includes Standby (**) and Suspend power down modes, and is available in a space saving 44-lead QFP pkg.

Device	Package	ROM	OTP	Comments
80C42	N, P, S	4K		ROM Device
82C42PC	N, P, S			Phoenix MultiKey/42 firmware, PS/2 style mouse support
82C42PD	N, P, S			Phoenix MultiKey/42L firmware, KBC and SCC for portable apps.
82C42PE	N, P, S			Phoenix MultiKey/42G firmware, Energy Efficient KBC solution
87C42	N, P, S		4K	One Time Programmable Version

UPI-L42: The low voltage 3.3V version of the UPI-C42.

Device	Package	ROM	OTP	Comments
80L42	N, P, S	4K		ROM Device
82L42PC	N, P, S			Phoenix MultiKey/42 firmware, PS/2 style mouse support
82L42PD	N, P, S			Phoenix MultiKey/42L firmware, KBC and SCC for portable apps.
87L42	N, P, S		4K	One Time Programmable Version

NOTES:
N = 44 lead PLCC, P = 40 lead PDIP, S = 44 lead QFP, D = 40 lead CERDIP
KBC = Key Board Control, SCC = Scan Code Control
(**) Standby feature not supported on current (B-1) stepping

DEVELOPMENT SUPPORT

The UPI microcomputer is fully supported by Intel with development tools like the UPP PROM programmer already mentioned. The combination of device features and Intel development support make the UPI an ideal component for low-speed peripheral control applications.

UPI DEVELOPMENT SUPPORT

- 8048/UPI-41A/41AH/42/42AH Assembler
- Universal PROM Programmer UPP Series
- Application Engineers
- Training Courses

CHAPTER 2
FUNCTIONAL DESCRIPTION

The UPI microcomputer is an intelligent peripheral controller designed to operate in iAPX-86, 88, MCS-85, MCS-80, MCS-51 and MCS-48 systems. The UPI's architecture, illustrated in Figure 2-1, is based on a low cost, single-chip microcomputer with program memory, data memory, CPU, I/O, event timer and clock oscillator in a single 40-pin package. Special interface registers are included which enable the UPI to function as a peripheral to an 8-bit master processor.

This chapter provides a basic description of the UPI microcomputer and its system interface registers. Unless otherwise noted the descriptions in this section apply to the 8741AH, 8742AH with OTP EPROM memory, the 8741A/8742 (with UV erasable program memory) and the 8041AH, 8042AH. These devices are so similar that they can be considered identical under most circumstances. All functions described in this chapter apply to the UPI-41A/41AH/42/42AH.

PIN DESCRIPTION

The UPI-41A/41AH/42/42AH are packaged in 40-pin Dual In-Line (DIP) packages. The pin configuration for both devices is shown in Figure 2-2. Figure 2-3 illustrates the UPI Logic Symbol.

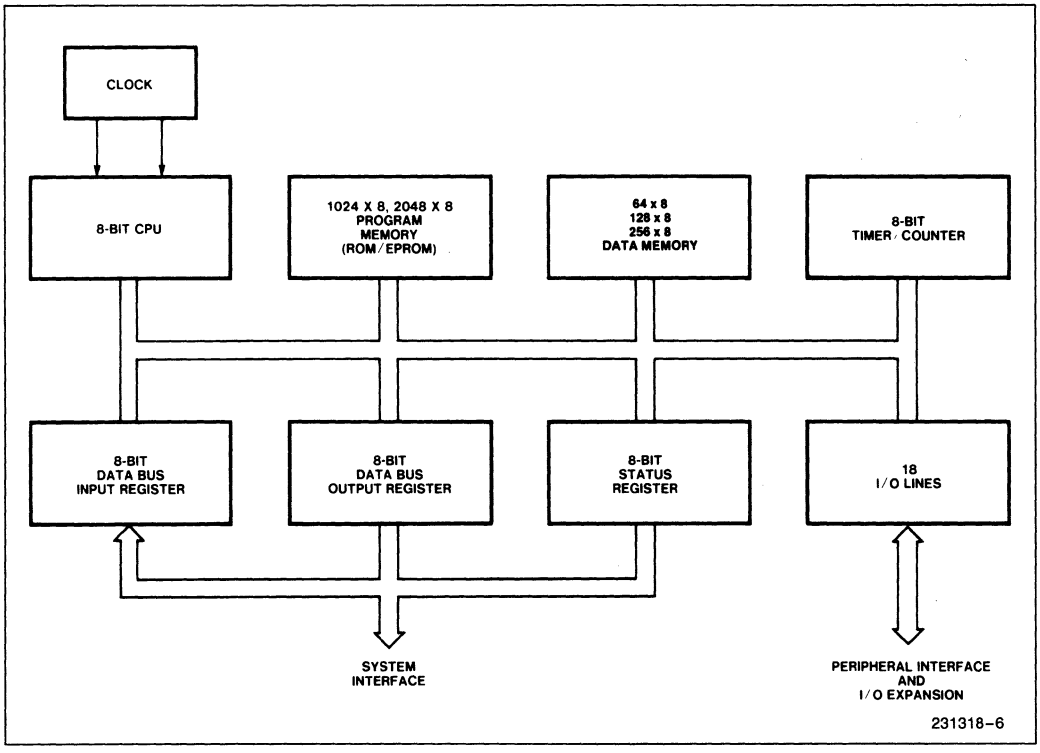


Figure 2-1. UPI-41A/41AH/42/42AH Single Chip Microcomputer

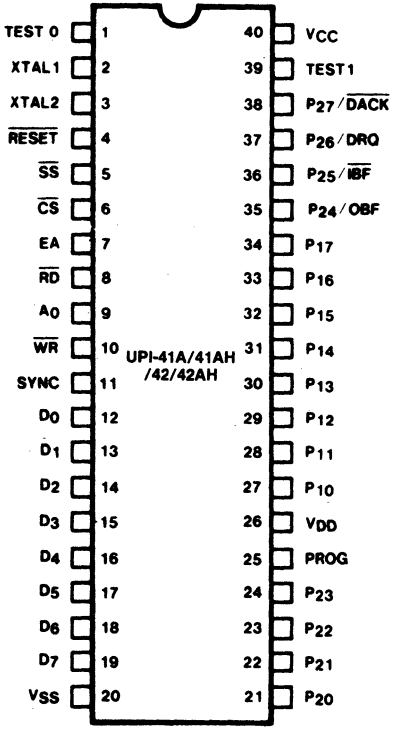


Figure 2-2. Pin Configuration

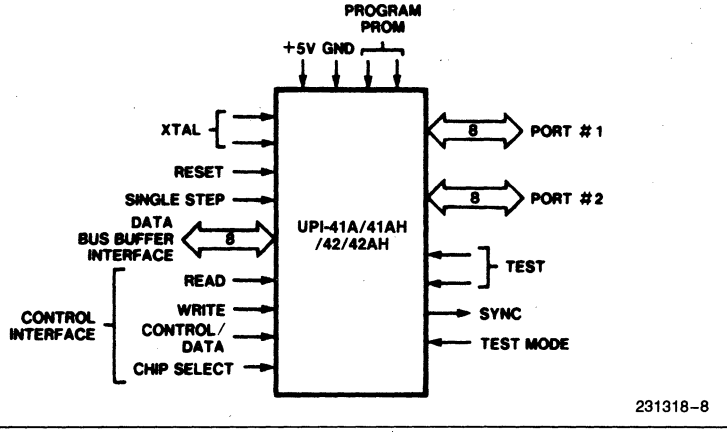


Figure 2-3. Logic Symbol

The following section summarizes the functions of each UPI pin. NOTE that several pins have two or more functions which are described in separate paragraphs.

Table 2-1. Pin Description

Symbol	Pin No.	Type	Name and Function
D_0–D_7 (BUS)	12–19	I/O	**DATA BUS:** Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI-41A/41AH/42/42AH microcomputer to an 8-bit master system data bus.
P_{10}–P_{17}	27-34	I/O	**PORT 1:** 8-bit, PORT 1 quasi-bidirectional I/O lines.
P_{20}–P_{27}	21-24 35–38	I/O	**PORT 2:** 8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P_{20}–P_{23}) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4–7 access. The upper 4 bits (P_{24}–P_{27}) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P_{24} as Output Buffer Full (OBF) interrupt, P_{25} as Input Buffer Full ($\overline{IBF}$) interrupt, P_{26} as DMA Request ($\overline{DRQ}$), and P_{27} as DMA ACKnowledge ($\overline{DACK}$).
$\overline{WR}$	10	I	**WRITE:** I/O write input which enables the master CPU to write data and command words to the UPI INPUT DATA BUS BUFFER.
$\overline{RD}$	8	I	**READ:** I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
$\overline{CS}$	6	I	**CHIP SELECT:** Chip select input used to select one UPI-41A/41AH/42/42AH microcomputer out of several connected to a common data bus.
A_0	9	I	**COMMAND/DATA SELECT:** Address input used by the master processor to indicate whether byte transfer is data (A_0 = 0) or command (A_0 = 1).
TEST 0, TEST 1	1 39	I	**TEST INPUTS:** Input pins can be directly tested using conditional branch instructions. **FREQUENCY REFERENCE:** TEST 1 (T_1) also functions as the event timer input (under software control). TEST0 (T_0) is used during PROM programming and verification in the UPI-41A/41AH/42/42AH.
XTAL 1, XTAL 2	2 3	I	**INPUTS:** Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
SYNC	11	O	**OUTPUT CLOCK:** Output signal which occurs once per UPI instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
EA	7	I	**EXTERNAL ACCESS:** External access input which allows emulation, testing and PROM/ROM verification.
PROG	25	I/O	**PROGRAM:** Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243.
$\overline{RESET}$	4	I	**RESET:** Input used to reset status flip-flops and to set the program counter to zero. $\overline{RESET}$ is also used during PROM programming and verification.
$\overline{SS}$	5	I	**SINGLE STEP:** Single step input used in conjunction with the SYNC output to step the program through each instruction.
V_{CC}	40		**POWER:** +5V main power supply pin.
V_{DD}	26		**POWER:** +5V during normal operation. +25V for UPI-41A, 21V for UPI-42 programming operation, +12V for programming, UPI-41AH/42AH. Low power standby pin in ROM version.
V_{SS}	20		**GROUND:** Circuit ground potential.

The following sections provide a detailed functional description of the UPI microcomputer. Figure 2-4 illustrates the functional blocks within the UPI device.

CPU SECTION

The CPU section of the UPI-41A/41AH/42/42AH microcomputer performs basic data manipulations and controls data flow throughout the single chip computer via the internal 8-bit data bus. The CPU section includes the following functional blocks shown in Figure 2-4:

- Arithmetic Logic Unit (ALU)
- Instruction Decoder
- Accumulator
- Flags

Arithmetic Logic Units (ALU)

The ALU is capable of performing the following operations:

- ADD with or without carry
- AND, OR, and EXCLUSIVE OR
- Increment, Decrement
- Bit complement
- Rotate left or right
- Swap
- BCD decimal adjust

In a typical operation data from the accumulator is combined in the ALU with data from some other source on the UPI-41A/41AH/42/42AH internal bus (such as a register or an I/O port). The result of an ALU operation can be transferred to the internal bus or back to the accumulator.

If an operation such as an ADD or ROTATE requires more than 8 bits, the CARRY flag is used as an indicator. Likewise, during decimal adjust and other BCD operations the AUXILIARY CARRY flag can be set and acted upon. These flags are part of the Program Status Word (PSW).

Instruction Decoder

During an instruction fetch, the operation code (opcode) portion of each program instruction is stored and decoded by the instruction decoder. The decoder generates outputs used along with various timing signals to control the functions performed in the ALU. Also, the instruction decoder controls the source and destination of ALU data.

Accumulator

The accumulator is the single most important register in the processor. It is the primary source of data to the ALU and is often the destination for results as well. Data to and from the I/O ports and memory normally passes through the accumulator.

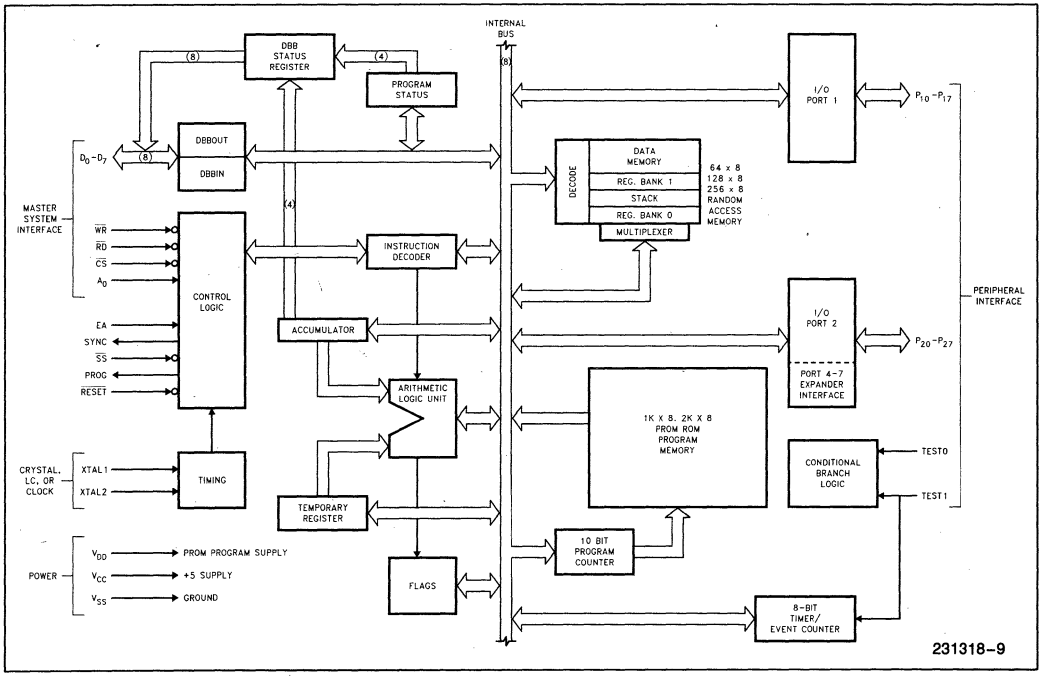


Figure 2-4. UPI-41A/41AH/42/42AH Block Diagram

PROGRAM MEMORY

The UPI-41A/41AH/42/42AH microcomputer has 1024, 2048 8-bit words of resident, read-only memory for program storage. Each of these memory locations is directly addressable by a 10-bit program counter. Depending on the type of application and the number of program changes anticipated, three types of program memory are available:

- 8041AH, 8042AH with mask programmed ROM Memory
- 8741AH, 8742AH with electrically programmable OTP EPROM Memory
- 8741A and 8742 with electrically programmable EPROM Memory

A program memory map is illustrated in Figure 2-5. Memory is divided into 256 location 'pages' and three locations are reserved for special use:

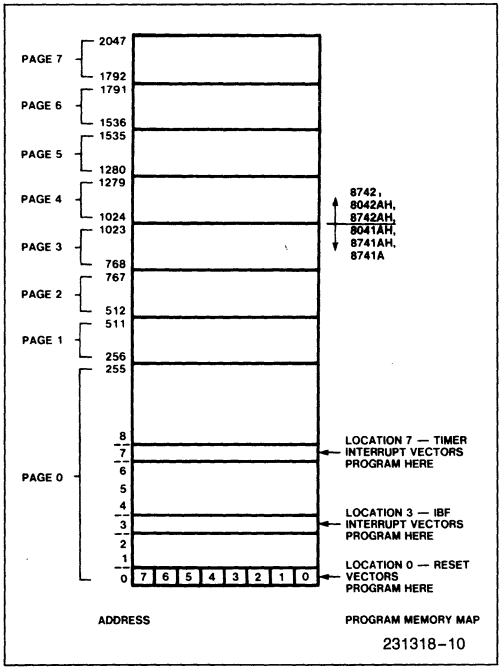


Figure 2-5. Program Memory Map

INTERRUPT VECTORS

1) **Location 0**
   Following a $\overline{\text{RESET}}$ input to the processor, the next instruction is automatically fetched from location 0.
2) **Location 3**
   An interrupt generated by an Input Buffer Full (IBF) condition (when the IBF interrupt is enabled) causes the next instruction to be fetched from location 3.
3) **Location 7**
   A timer overflow interrupt (when enabled) will cause the next instruction to be fetched from location 7.

Following a system $\overline{\text{RESET}}$, program execution begins at location 0. Instructions in program memory are normally executed sequentially. Program control can be transferred out of the main line of code by an input buffer full (IBF) interrupt or a timer interrupt, or when a jump or call instruction is encountered. An IBF interrupt (if enabled) will automatically transfer control to location 3 while a timer interrupt will transfer control to location 7.

All conditional JUMP instructions and the indirect JUMP instruction are limited in range to the current 256-location page (that is, they alter PC bits 0–7 only). If a conditional JUMP or indirect JUMP begins in location 255 of a page, it must reference a destination on the following page.

Program memory can be used to store constants as well as program instructions. The UPI-41AH, 42AH instruction set contains an instruction (MOVP3) designed specifically for efficient transfer of look-up table information from page 3 of memory.

DATA MEMORY

The UPI-41A has 64 8-bit words of Random Access Memory, the UPI-41AH has 128 8-bit words of Random Access Memory; the UPI-42 has 128 8-bit words of RAM; and the UPI-42AH has 256 8-bit words of RAM. This memory contains two working register banks, an 8-level program counter stack and a scratch pad memory, as shown in Figure 2-6. The amount of scratch pad memory available is variable depending on the number of addresses nested in the stack and the number of working registers being used.

Addressing Data Memory

The first eight locations in RAM are designated as working registers R_0–R_7. These locations (or registers) can be addressed directly by specifying a register number in the instruction. Since these locations are easily addressed, they are generally used to store frequently

accessed intermediate results. Other locations in data memory are addressed indirectly by using R_0 or R_1 to specify the desired address.

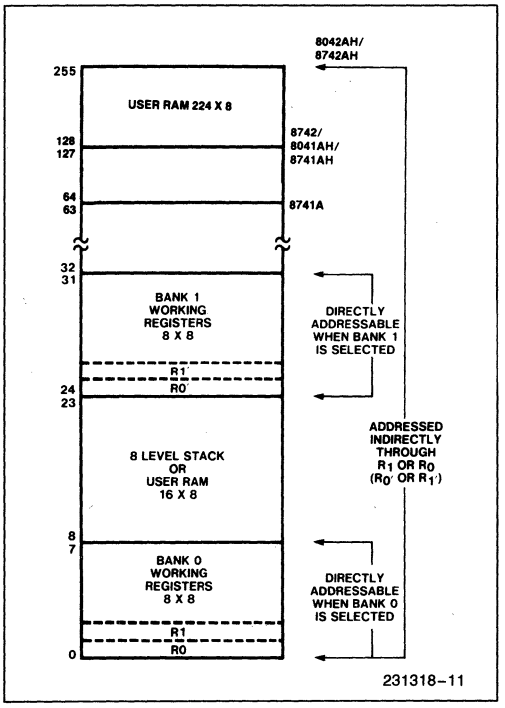


Figure 2-6. Data Memory Map

Working Registers

Dual banks of eight working registers are included in the UPI-41A/41AH/42/42AH data memory. Locations 0–7 make up register bank 0 and locations 24–13 form register bank 1. A $\overline{\text{RESET}}$ signal automatically selects register bank 0. When bank 0 is selected, references to R_0–R_7 in UPI-41A/41AH/42/42AH instructions operate on locations 0–7 in data memory. A "select register bank" instruction is used to selected between the banks during program execution. If the instruction SEL RB1 (Select Register Bank 1) is executed, then program references to R_0–R_7 will operate on locations 24–31. As stated previously, registers 0 and 1 in the active register bank are used as indirect address registers for all locations in data memory.

Register bank 1 is normally reserved for handling interrupt service routines, thereby preserving the contents of the main program registers. The SEL RB1 instruction can be issued at the beginning of an interrupt service routine. Then, upon return to the main program, an RETR (return & restore status) instruction will automatically restore the previously selected bank. During interrupt processing, registers in bank 0 can be accessed indirectly using $R_{0'}$ and $R_{1'}$.

If register bank 1 is not used, registers 24–31 can still serve as additional scratch pad memory.

Program Counter Stack

RAM locations 8–23 are used as an 8-level program counter stack. When program control is temporarily passed from the main program to a subroutine or interrupt service routine, the 10-bit program counter and bits 4–7 of the program status word (PSW) are stored in two stack locations. When control is returned to the main program via an RETR instruction, the program counter and PSW bits 4–7 are restored. Returning via an RET instruction does not restore the PSW bits, however. The program counter stack is addressed by three stack pointer bits in the PSW (bits 0–2). Operation of the program counter stack and the program status word is explained in detail in the following sections.

The stack allows up to eight levels of subroutine 'nesting'; that is, a subroutine may call a second subroutine, which may call a third, etc., up to eight levels. Unused stack locations can be used as scratch pad memory. Each unused level of subroutine nesting provides two additional RAM locations for general use.

The following sections provide a detailed description of the Program Counter Stack and the Program Status Word.

PROGRAM COUNTER

The UPI-41A/41AH/42/42AH microcomputer has a 10-bit program counter (PC) which can directly address any of the 1024, 2048, or 4096 locations in program memory. The program counter always contains the address of the next instruction to be executed and is normally incremented sequentially for each instruction to be executed when each instruction fetches occurs.

When control is temporarily passed from the main program to a subroutine or an interrupt routine, however, the PC contents must be altered to point to the address of the desired routine. The stack is used to save the current PC contents so that, at the end of the routine, main program execution can continue. The program counter is initialized to zero by a $\overline{\text{RESET}}$ signal.

PROGRAM COUNTER STACK

The Program Counter Stack is composed of 16 locations in Data Memory as illustrated in Figure 2-7. These RAM locations (8 through 23) are used to store the 10-bit program counter and 4 bits of the program status word.

An interrupt or Call to a subroutine causes the contents of the program counter to be stored in one of the 8 register pairs of the program counter stack.

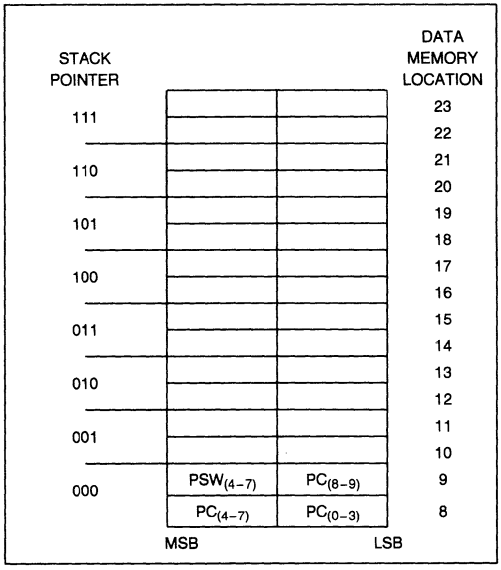


Figure 2-7. Program Counter Stack

A 3-bit Stack Pointer which is part of the Program Status Word (PSW) determines the stack pair to be used at a given time. The stack pointer is initialized by a $\overline{\text{RESET}}$ signal to 00H which corresponds to RAM locations 8 and 9.

The first call or interrupt results in the program counter and PSW contents being transferred to RAM locations 8 and 9 in the format shown in Figure 2-7. The stack pointer is automatically incremented by 1 to point to location is 10 and 11 in anticipation of another CALL.

Nesting of subroutines within subroutines can continue up to 8 levels without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 07H to 00H. Likewise, the stack pointer will underflow from 00H to 07H.

The end of a subroutine is signaled by a return instruction, either RET or RETR. Each instruction will automatically decrement the Stack Pointer and transfer the contents of the proper RAM register pair to the Program Counter.

PROGRAM STATUS WORD

The 8-bit program status word illustrated in Figure 2-8 is used to store general information about program execution. In addition to the 3-bit Stack Pointer discussed previously, the PSW includes the following flags:

- CY — Carry
- AC — Auxiliary Carry
- F_0 — Flag 0
- BS — Register Bank Select

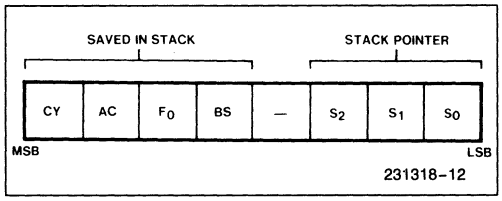


Figure 2-8. Program Status Word

The Program Status Word (PSW) is actually a collection of flip-flops located throughout the machine which are read or written as a whole. The PSW can be loaded to or from the accumulator by the MOV A, PSW or MOV PSW, A instructions. The ability to write directly to the PSW allows easy restoration of machine status after a power-down sequence.

The upper 4 bits of the PSW (bits 4, 5, 6, and 7) are stored in the PC Stack with every subroutine CALL or interrupt vector. Restoring the bits on a return is optional. The bits are restored if an RETR instruction is executed, but not if an RET is executed.

PSW bit definitions are as follows:

- Bits 0–2 Stack Pointer Bits S_0, S_1, S_2
- Bit 3 Not Used
- Bit 4 Working Register Bank
  0 = Bank 0
  1 = Bank 1
- Bit 5 Flag 0 bit (F_0)
  This is a general purpose flag which can be cleared or complemented and tested with conditional jump instructions. It may be used during data transfer to an external processor.
- Bit 6 Auxiliary Carry (AC)
  The flag status is determined by an ADD instruction and is used by the Decimal Adjustment instruction DAA
- Bit 7 Carry (CY)
  The flag indicates that a previous operation resulted in overflow of the accumulator.

CONDITIONAL BRANCH LOGIC

Conditional Branch Logic in the UPI-41AH, 42AH allows the status of various processor flags, inputs, and other hardware functions to directly affect program execution. The status is sampled in state 3 of the first cycle.

Table 2-2 lists the internal conditions which are testable and indicates the condition which will cause a jump. In all cases, the destination address must be within the page of program memory (256 locations) in which the jump instruction occurs.

OSCILLATOR AND TIMING CIRCUITS

The UPI-41A/41AH/42/42AH's internal timing generation is controlled by a self-contained oscillator and timing circuit. A choice of crystal, L-C or external clock can be used to derive the basic oscillator frequency.

The resident timing circuit consists of an oscillator, a state counter and a cycle counter as illustrated in Figure 2-9. Figure 2-10 shows instruction cycle timing.

Oscillator

The on-board oscillator is a series resonant circuit with a frequency range of 1 to 12.5 MHz depending on which UPI is used. Refer to Table 1.1. Pins XTAL 1 and XTAL 2 are input and output (respectively) of a high gain amplifier stage. A crystal or inductor and capacitor connected between XTAL 1 and XTAL 2 provide the feedback and proper phase shift for oscillation. Recommended connections for crystal or L-C are shown in Figure 2-11.

State Counter

The output of the oscillator is divided by 3 in the state counter to generate a signal which defines the state times of the machine.

Each instruction cycle consists of five states as illustrated in Figure 2-10 and Table 2-3. The overlap of address and execution operations illustrated in Figure 2-10 allows fast instruction execution.

Table 2-2. Conditional Branch Instructions

Device	Instruction Mnemonic		Jump Condition Jump if:
Accumulator	JZ	addr	All bits zero
	JNZ	addr	Any bit not zero
Accumulator bit	JBb	addr	Bit "b" = 1
Carry flag	JC	addr	Carry flag = 1
	JNC	addr	Carry flag = 0
User flag	JFO	addr	F_0 flag = 1
	JF1	addr	F_1 flag = 1
Timer flag	JTF	addr	Timer flag = 1
Test Input 0	JT0	addr	T_0 = 1
	JNT0	addr	T_0 = 0
Test Input 1	JT1	addr	T_1 = 1
	JNT1	addr	T_1 = 0
Input Buffer flag	JNIBF	addr	IBF flag = 0
Output Buffer flag	JOBF	addr	OBF flag = 1

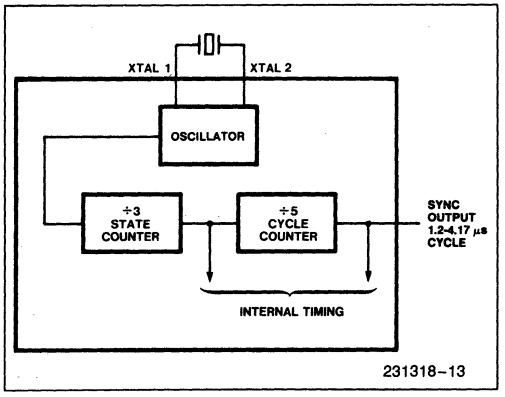


Figure 2-9. Oscillator Configuration

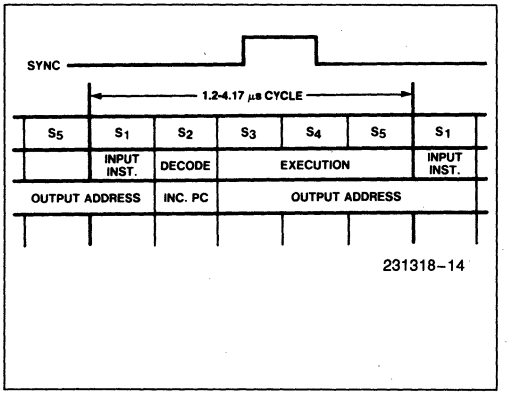


Figure 2-10. Instruction Cycle Timing

Table 2-3. Instruction Timing Diagram

Instruction	CYCLE 1					CYCLE 2				
	S1	S2	S3	S4	S5	S1	S2	S3	S4	S5
IN A,Pp	Fetch Instruction	Increment Program Counter	—	Increment Timer	—	—	Read Port	—	—	—
OUTL Pp,A	Fetch Instruction	Increment Program Counter	—	Increment Timer	Output To Port	—	—	—	—	—
ANL Pp, DATA	Fetch Instruction	Increment Program Counter	—	Increment Timer	Read Port	Fetch Immediate Data	—	Increment Program Counter	Output To Port	—
ORL Pp, DATA	Fetch Instruction	Increment Program Counter	—	Increment Timer	Read Port	Fetch Immediate Data	—	Increment Program Counter	Output To Port	—
MOVD A,Pp	Fetch Instruction	Increment Program Counter	Output Opcode/Address	Increment Timer	—	—	Read P2 Lower	—	—	—
MOVD Pp, A	Fetch Instruction	Increment Program Counter	Output Opcode/Address	Increment Timer	Output Data To P2 Lower	—	—	—	—	—
D Pp, A	Fetch Instruction	Increment Program Counter	Output Opcode/Address	Increment Timer	Output Data	—	—	—	—	—
ORLD Pp, A	Fetch Instruction	Increment Program Counter	Output Opcode/Address	Increment Timer	Output Data	—	—	—	—	—
J (Conditional)	Fetch Instruction	Increment Program Counter	Sample Condition	Increment Timer	—	Fetch Immediate Data	—	Update Program Counter	—	—
MOV STS, A	Fetch Instruction	Increment Program Counter	—	Increment Timer	Update Status Register					
IN A, DBB	Fetch Instruction	Increment Program Counter	—	Increment Timer	—					
OUT DBB, A	Fetch Instruction	Increment Program Counter	—	Increment Timer	Output To Port					
STRT T STRT CNT	Fetch Instruction	Increment Program Counter	—	—	Start Counter					
STOP TCNT	Fetch Instruction	Increment Program Counter	—	—	Stop Counter					
EN I	Fetch Instruction	Increment Program Counter	—	Enable Interrupt	—					
DIS I	Fetch Instruction	Increment Program Counter	—	Disable Interrupt	—					
EN DMA	Fetch Instruction	Increment Program Counter	—	DMA Enabled DRQ Cleared	—					
EN FLAGS	Fetch Instruction	Increment Program Counter	—	OBF, $\overline{IBF}$ Output Enabled	—					

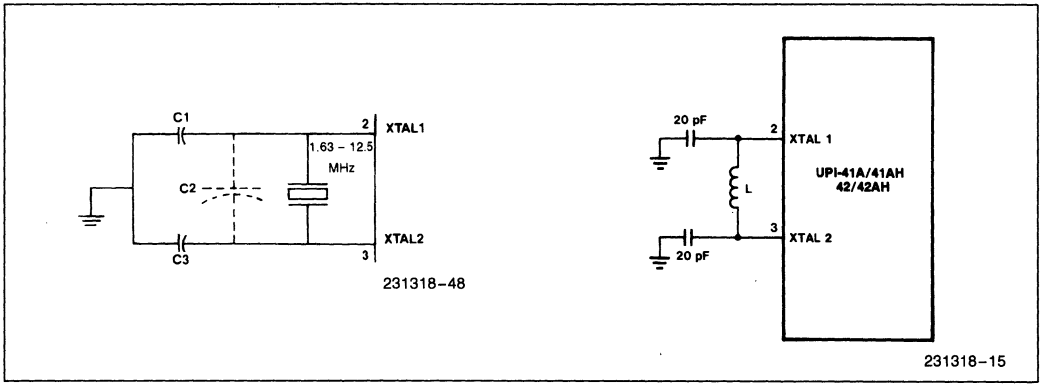


Figure 2-11. Recommended Crystal and L-C Connections

Cycle Counter

The output of the state counter is divided by 5 in the cycle counter to generate a signal which defines a machine cycle. This signal is call SYNC and is available continuously on the SYNC output pin. It can be used to synchronize external circuitry or as a general purpose clock output. It is also used for synchronizing single-step.

Frequency Reference

The external crystal provides high speed and accurate timing generation. A crystal frequency of 5.9904 MHz is useful for generation of standard communication frequencies by the UPI-41A/41AH/42/42AH. However, if an accurate frequency reference and maximum processor speed are not required, an inductor and capacitor may be used in place of the crystal as shown in Figure 2-11.

A recommended range of inductance and capacitance combinations is given below:

- L = 130 μH corresponds to 3 MHz
- L = 45 μH corresponds to 5 MHz

An external clock signal can also be used as a frequency reference to the UPI-41A/41AH/42/42AH; however, the levels are *not* TTL compatible. The signal must be in the 1–12.5 MHz frequency range depending on which UPI is used. Refer to Table 1-2. The signal must be connected to pins XTAL 1 and XTAL 2 by buffers with a suitable pull-up resistor to guarantee that a logic "1" is above 3.8 volts. The recommended connection is shown in Figure 2-12.

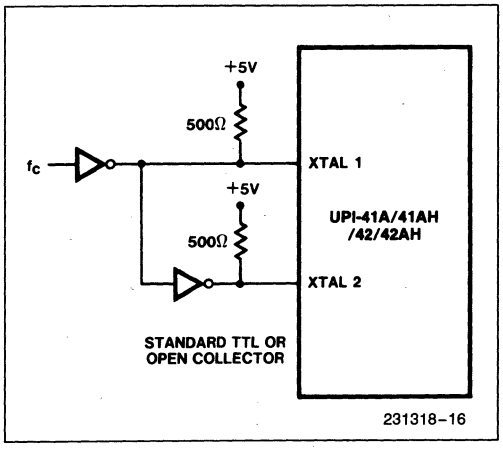


Figure 2-12. Recommended Connection For External Clock Signal

INTERVAL TIMER/EVENT COUNTER

The UPI-41A/41AH/42/42AH has a resident 8-bit timer/counter which has several software selectable modes of operation. As an interval timer, it can generate accurate delays from 80 microseconds to 20.48 milliseconds without placing undue burden on the processor. In the counter mode, external events such as switch closures or tachometer pulses can be counted and used to direct program flow.

Timer Configuration

Figure 2-13 illustrates the basic timer/counter configuration. An 8-bit register is used to count pulses from either the internal clock and prescaler or from an external source. The counter is presettable and readable with two MOV instructions which transfer the contents of the accumulator to the counter and vice-versa (i.e. MOV T, A and MOV A, T). The counter is stopped by a $\overline{\text{RESET}}$ or STOP TCNT instruction and remains stopped until restarted either as a timer (START T instruction) or as a counter (START CNT instruction). Once started, the counter will increment to its maximum count (FFH) and overflow to zero continuing its count until stopped by a STOP TCNT instruction or $\overline{\text{RESET}}$.

The increment from maximum count to zero (overflow) results in setting the Timer Flag (TF) and generating an interrupt request. The state of the overflow flag is testable with the conditional jump instruction, JTF. The flag is reset by executing a JTF or by a $\overline{\text{RESET}}$ signal.

The timer interrupt request is stored in a latch and ORed with the input buffer full interrupt request. The timer interrupt can be enabled or disabled independent of the IBF interrupt by the EN TCNTI and DIS TCTNI instructions. If enabled, the counter overflow will cause a subroutine call to location 7 where the timer service routine is stored. If the timer and Input Buffer Full interrupts occur simultaneously, the IBF source will be recognized and the call will be to location 3. Since the timer interrupt is latched, it will remain pending until the DBBIN register has been serviced and will immediately be recognized upon return from the service routine. A pending timer interrupt is reset by the initiation of a timer interrupt service routine.

Event Counter Mode

The STRT CNT instruction connects the TEST 1 input pin to the counter input and enables the counter. Note this instruction does not clear the counter. The counter is incremented on high to low transitions of the TEST 1 input. The TEST 1 input must remain high for a minimum of one state in order to be registered (250 ns at 12 MHz). The maximum count frequency is one count per three instruction cycles (267 kHz at 12 MHz). There is no minimum frequency limit.

Timer Mode

The STRT T instruction connects the internal clock to the counter input and enables the counter. The input clock is derived from the SYNC signal of the internal oscillator and the divide-by-32 prescaler. The configuration is illustrated in Figure 2-13. Note this instruction does not clear the timer register. Various delays and timing sequences between 40 μsec and 10.24 msec can easily be generated with a minimum of software timing loops (at 12 MHz).

Times longer than 10.24 msec can be accurately measured by accumulating multiple overflows in a register under software control. For time resolution less than 40 μsec, an external clock can be applied to the TEST 1 counter input (see Event Counter Mode). The minimum time resolution with an external clock is 3.75 μsec (267 kHz at 12 MHz).

TEST 1 Event Counter Input

The TEST 1 pin is multifunctional. It is automatically initialized as a test input by a $\overline{\text{RESET}}$ signal and can be tested using UPI-41A conditional branch instructions.

In the second mode of operation, illustrated in Figure 2-13, the TEST 1 pin is used as an input to the internal 8-bit event counter. The Start Counter (STRT CNT) instruction controls an internal switch which connects TEST 1 through an edge detector to the 8-bit internal counter. Note that this instruction does not inhibit the testing of TEST 1 via conditional Jump instructions.

In the counter mode the TEST 1 input is sampled once per instruction cycle. After a high level is detected, the next occurrence of a low level at TEST 1 will cause the counter to increment by one.

The event counter functions can be stopped by the Stop Timer/Counter (STOP TCNT) instruction. When this instruction is executed the TEST 1 pin becomes a test input and functions as previously described.

TEST INPUTS

There are two multifunction pins designated as Test Inputs, TEST 0 and TEST 1. In the normal mode of operation, status of each of these lines can be directly tested using the following conditional Jump instructions:

- JT0 Jump if TEST 0 = 1
- JNT0 Jump if TEST 0 = 0
- JT1 Jump if TEST 1 = 1
- JNT1 Jump if TEST 1 = 0

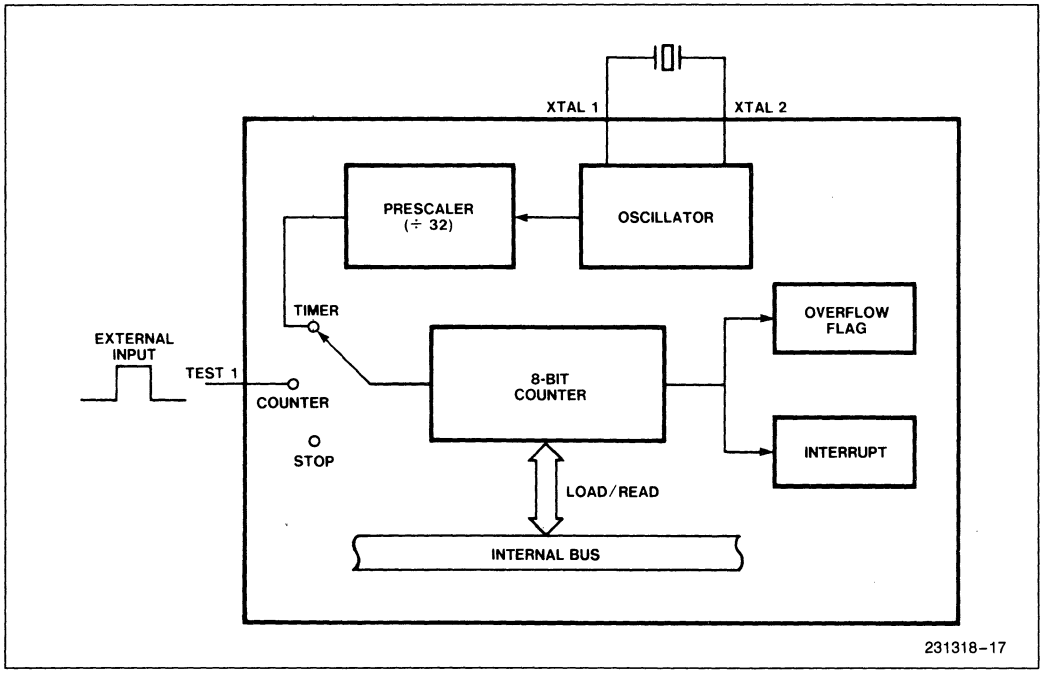


Figure 2-13. Timer Counter

The test imputs are TTL compatible. An external logic signal connected to one of the test inputs will be sampled at the time the appropriate conditional jump instruction is executed. The path of program execution will be altered depending on the state of the external signal when sampled.

INTERRUPTS

The UPI-41A/41AH/42/42AH has the following internal interrupts:

- Input Buffer Full (IBF) interrupt
- Timer Overflow interrupt

The IBF interrupt forces a CALL to location 3 in program memory; a timer-overflow interrupts forces a CALL to location 7. The IBF interrupt is enabled by the EN I instruction and disabled by the DIS I instruction. The timer-overflow interrupt is enabled and disabled by the EN TNCTI and DIS TCNTI instructions, respectively.

Figure 2-14 illustrates the internal interrupt logic. An IBF interrupt request is generated whenever $\overline{WR}$ and $\overline{CS}$ are both low, regardless of whether interrupts are enabled. The interrupt request is cleared upon entering the IBF service routine only. That is, the DIS I instruction does not clear a pending IBF interrupt.

Interrupt Timing Latency

When the IBF interrupt is enabled and an IBF interrupt request occurs, an interrupt sequence is intiated as soon as the currently executing instruction is completed. The following sequence occurs:

- A CALL to location 3 is forced.
- The program counter and bits 4–7 of the Program Status Word are stored in the stack.
- The stack pointer is incremented.

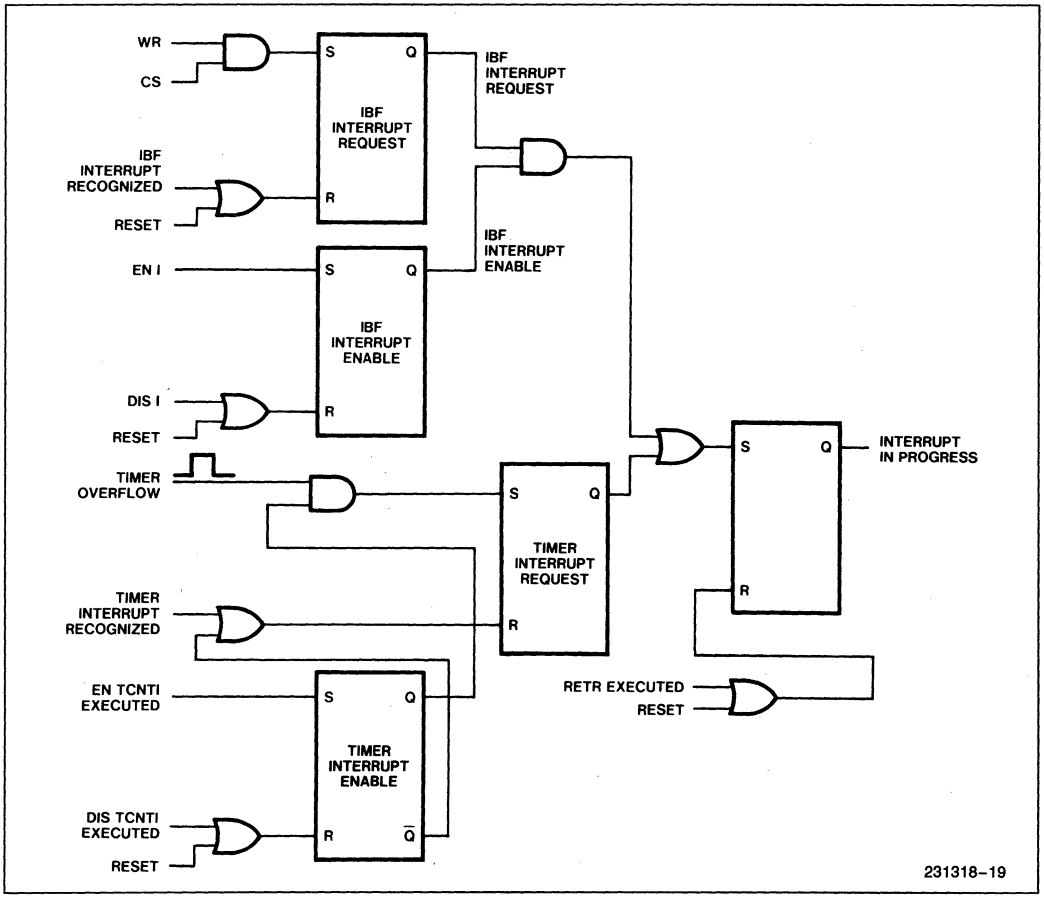


Figure 2-14. Interrupt Logic

Location 3 in program memory should contain an unconditional jump to the beginning of the IBF interrupt service routine elsewhere in program memory. At the end of the service routine, an RETR (Return and Restore Status) instruction is used to return control to the main program. This instruction will restore the program counter and PSW bits 4–7, providing automatic restoration of the previously active register bank as well. RETR also re-enables interrupts.

A timer-overflow interrupt is enabled by the EN TCNTI instruction and disabled by the DIS TCNTI instruction. If enabled, this interrupt occurs when the timer/counter register overflows. A CALL to location 7 is forced and the interrupt routine proceeds as described above.

The interrupt service latency is the sum of current instruction time, interrupt recognition time, and the internal call to the interrupt vector address. The worst case latency time for servicing an interrupt is 7 clock cycles. Best case latency is 4 clock cycles.

Interrupt Timing

Interrupt inputs may be enabled or disabled under program control using EN I, DIS I, EN TCNTI and DIS TCNTI instructions. Also, a $\overline{\text{RESET}}$ input will disable interrupts. An interrupt request must be removed before the RETR instruction is executed to return from the service routine, otherwise the processor will re-enter the service routine immediately. Thus, the $\overline{\text{WR}}$ and $\overline{\text{CS}}$ inputs should not be held low longer than the duration of the interrupt service routine.

The interrupt system is single level. Once an interrupt is detected, all further interrupt requests are latched but are not acted upon until execution of an RETR instruction re-enables the interrupt input logic. This occurs at the beginning of the second cycle of the RETR instruction. If an IBF interrupt and a timer-overflow interrupt occur simultaneously, the IBF interrupt will be recognized first and the timer-overflow interrupt will remain pending until the end of the interrupt service routine.

External Interrupts

An external interrupt can be created using the UPI-41A/41AH/42/42AH timer/counter in the event counter mode. The counter is first preset to FFH and the EN TCNTI instruction is executed. A timer-overflow interrupt is generated by the first high to low transition of the TEST 1 input pin. Also, if an IBF interrupt occurs during servicing of the timer/counter interrupt, it will remain pending until the end of the service routine.

Host Interrupts And DMA

If needed, two external interrupts to the host system can be created using the EN FLAGS instruction. This instruction allocates two I/O lines on PORT 2 (P_{24} and P_{25}). P_{24} is the Output Buffer Full interrupt request line to the host system; P_{25} is the Input Buffer empty interrupt request line. These interrupt outputs reflect the internal status of the OBF flag and the IBF inverted flag. Note, these outputs may be inhibited by writing a "0" to these pins. Reenabling interrupts is done by writing a "1" to these port pins. Interrupts are typically enabled after power on since the I/O ports are set in a "1" condition. The EN FLAG's effect is only cancelled by a device RESET.

DMA handshaking controls are available from two pins on PORT 2 of the UPI-41A/41AH/42/42AH microcomputer. These lines (P_{26} and P_{27}) are enabled by the EN DMA instruction. P_{26} becomes DMA request (DRQ) and P_{27} becomes DMA acknowledge ($\overline{\text{DACK}}$). The UPI program initiates a DMA request by writing a "1" to P_{26}. The DMA controller transfers the data into the DBBIN data register using DACK which acts as a chip select. The EN DMA instruction can only be cancelled by a chip RESET.

RESET

The $\overline{\text{RESET}}$ input provides a means for internal initialization of the processor. An automatic initialization pulse can be generated at power-on by simply connecting a 1 μfd capacitor between the $\overline{\text{RESET}}$ input and ground as shown in Figure 2-15. It has an internal pull-up resistor to charge the capacitor and a Schmitt-trigger circuit to generate a clean transition. A 2-stage synchronizer has been added to support reliable operation up to 12.5 MHz.

If automatic initialization is used, $\overline{\text{RESET}}$ should be held low for at least 10 milliseconds to allow the power supply to stabilize. If an external $\overline{\text{RESET}}$ signal is used, $\overline{\text{RESET}}$ may be held low for a minimum of 8 instruction cycles. Figure 2-15 illustrates a configuration using an external TTL gate to generate the $\overline{\text{RESET}}$ input. This configuration can be used to derive the $\overline{\text{RESET}}$ signal from the 8224 clock generator in an 8080 system.

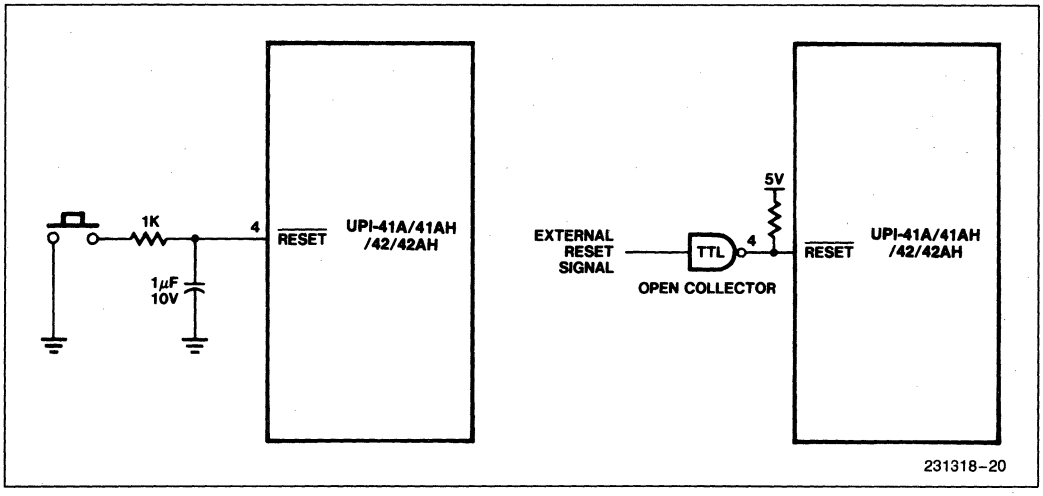


Figure 2-15. External Reset Configuration

The $\overline{\text{RESET}}$ input performs the following functions:

- Disables Interrupts
- Clears Program Counter to Zero
- Clears Stack Pointer
- Clears Status Register and Flags
- Clears Timer and Timer Flag
- Stops Timer
- Selects Register Bank 0
- Sets PORTS 1 and 2 to Input Mode

DATA BUS BUFFER

Two 8-bit data bus buffer registers, DBBIN and DBBOUT, serve as temporary buffers for commands and data flowing between it and the master processor. Externally, data is transmitted or received by the DBB registers upon execution of an INput or OUTput instruction by the master processor. Four control signals are used:

- A_0 Address input signifying control or data
- $\overline{\text{CS}}$ Chip Select
- $\overline{\text{RD}}$ Read Strobe
- $\overline{\text{WR}}$ Write Strobe

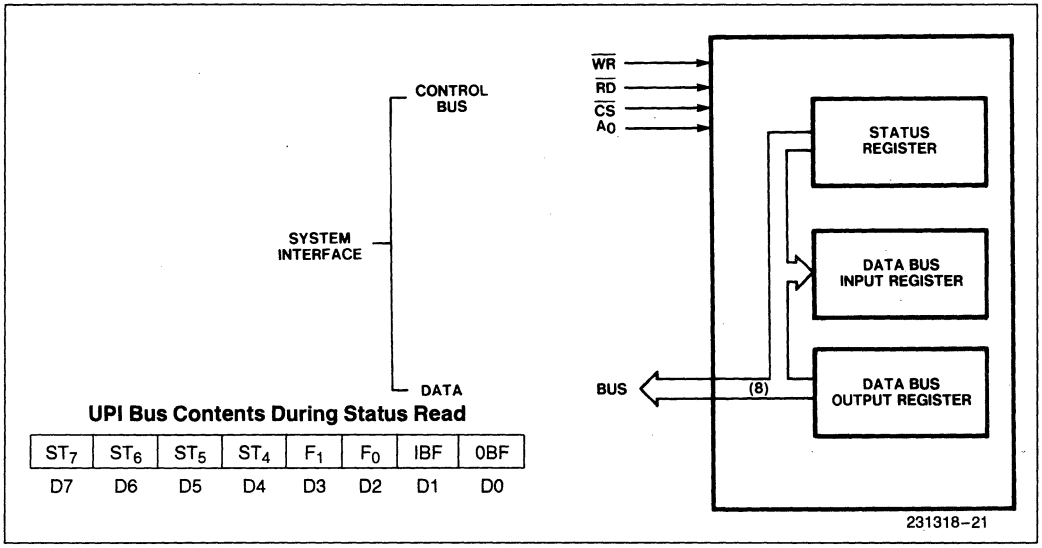
Transfer can be implemented with or without UPI program interference by enabling or disabling an internal UPI interrupt. Internally, data transfer between the DBB and the UPI accumulator is under software control and is completely asynchronous to the external processor timing. This allows the UPI software to handle peripheral control tasks independent of the main processor while still maintaining a data interface with the master system.

Configuration

Figure 2-16 illustrates the internal configuration of the DBB registers. Data is stored in two 8-bit buffer registers, DBBIN and DBBOUT. DBBIN and DBBOUT may be accessed by the external processor using the $\overline{\text{WR}}$ line and the $\overline{\text{RD}}$ line, respectively. The data bus is a bidirectional, three-state bus which can be connected directly to an 8-bit microprocessor system. Four control lines ($\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{CS}}$, A_0) are used by the external processor to transfer data to and from the DBBIN and DBBOUT registers.

An 8-bit register containing status flags is used to indicate the status of the DBB registers. The eight status flags are defined as follows:

- **OBF Output Buffer Full**
  This flag is automatically set when the UPI-Microcomputer loads the DBBOUT register and is cleared when the master processor reads the data register.
- **IBF Input Buffer Full**
  This flag is set when the master processor writes a character to the DBBIN register and is cleared when the UPI INputs the data register contents to its accumulator.



UPI Bus Contents During Status Read

ST_7	ST_6	ST_5	ST_4	F_1	F_0	IBF	OBF
D7	D6	D5	D4	D3	D2	D1	D0

Figure 2-16. Data Bus Buffer Configuration

- **F_0**
  This is a general purpose flag which can be cleared or toggled under UPI software control. The flag is used to transfer UPI status information to the master processor.
- **F_1 Command/Data**
  This flag is set to the condition of the A_0 input line when the master processor writes a character to the data register. The F_1 flag can also be cleared or toggled under UPI-Microcomputer program control.
- **ST4 through ST7**
  These bits are user defined status bits. They are defined by the MOV STS,A instruction.

SYSTEM INTERFACE

Figure 2-17 illustrates how a UPI-Microcomputer can be connected to a standard 8080-type bus system. Data lines D_0–D_7 form a three-state, bidirectional port which can be connected directly to the system data bus. The UPI bus interface has sufficient drive capability (400 μA) for small systems, however, a larger system may require buffers.

Four control signals are required to handle the data and status information transfer:

- $\overline{WR}$
  I/O WRITE signal used to transfer data from the system bus to the UPI DBBIN register and set the F_1 flag in the status register.
- $\overline{RD}$
  I/O READ signal used to transfer data from the DBBOUT register or status register to the system data bus.
- $\overline{CS}$
  CHIP SELECT signal used to enable one 8041AH out of several connected to a common bus.
- $\overline{A_0}$
  Address input used to select either the 8-bit status register or DBBOUT register during an I/O READ. Also, the signal is used to set the F_1 flag in the status register during an I/O WRITE.

The $\overline{WR}$ and $\overline{RD}$ signals are active low and are standard MCS-80 peripheral control signals used to synchronize data transfer between the system bus and peripheral devices.

The $\overline{CS}$ and A_0 signals are decoded from the address bus of the master system. In a system with few I/O devices a linear addressing configuration can be used where A_0 and A_1 lines are connected directly to A_0 and $\overline{CS}$ inputs (see Figure 2-17).

Data Read

Table 2-4 illustrates the relative timing of a DBBOUT Read. When $\overline{CS}$, A_0, and $\overline{RD}$ are low, the contents of the DBBOUT register is placed on the three-state Data lines D_0–D_7 and the OBF flag is cleared.

The master processor uses $\overline{CS}$, A_0, $\overline{WR}$, and $\overline{RD}$ to control data transfer between the DBBOUT register and the master system. The following operations are under master processor control:

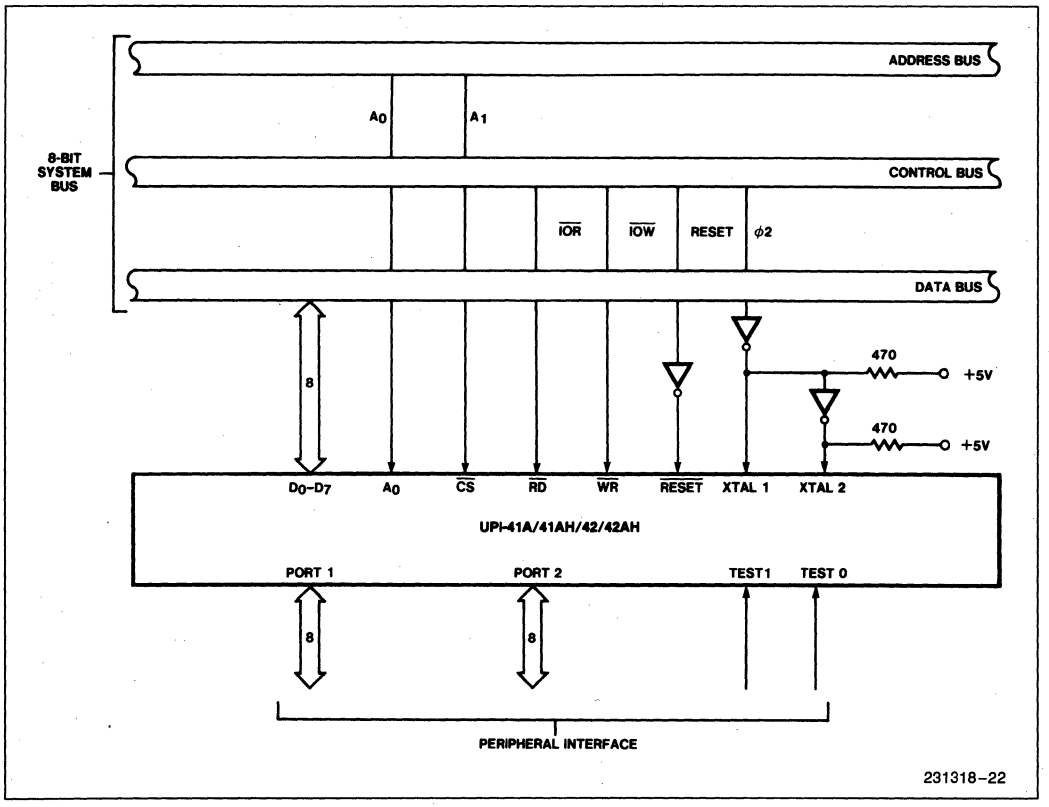


Figure 2-17. Interface to 8080 System Bus

Table 2-4. Data Transfer Controls

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0	
0	0	1	0	Read DBBOUT register
0	0	1	1	Read STATUS register
0	1	0	0	Write DBBIN data register
0	1	0	1	Write DBBIN command register
1	x	x	x	Disable DBB

Status Read

Table 2-4 shows the logic sequence required for a STATUS register read. When $\overline{CS}$ and $\overline{RD}$ are low with A_0 high, the contents of the 8-bit status register appears on Data lines D_0–D_7.

Data Write

Table 2-4 shows the sequence for writing information to the DBBIN register. When $\overline{CS}$ and $\overline{WR}$ are low, the contents of the system data bus is latched into DBBIN. Also, the IBF flag is set and an interrupt is generated, if enabled.

Command Write

During any write (Table 2-4), the state of the A_0 input is latched into the status register in the F_1 (command/data) flag location. This additional bit is used to signal whether DBBIN contents are command (A_0 = 1) or data (A_0 = 0) information.

INPUT/OUTPUT INTERFACE

The UPI-41A/41AH/42/42AH has 16 lines for input and output functions. These I/O lines are grouped as two 8-bit TTL compatible ports: PORTS 1 and 2. The port lines can individually function as either inputs or outputs under software control. In addition, the lower 4 lines of PORT 2 can be used to interface to an 8243 I/O expander device to increase I/O capacity to 28 or more lines. The additional lines are grouped as 4-bit ports: PORTS 4, 5, 6, and 7.

PORTS 1 and 2

PORTS 1 and 2 are each 8 bits wide and have the same I/O characteristics. Data written to these ports by an

OUTL Pp,A instruction is latched and remains unchanged until it is rewritten. Input data is sampled at the time the IN, A, Pp instruction is executed. Therefore, input data must be present at the PORT until read by an INput instruction. PORT 1 and 2 inputs are fully TTL compatible and outputs will drive one standard TTL load.

Circuit Configuration

The PORT 1 and 2 lines have a special output structure (shown in Figure 2-18) that allows each line to serve as an input, an output, or both, even though outputs are statically latched.

Each line has a permanent high impedance pull-up (50 KΩ) which is sufficient to provide source current for a TTL high level, yet can be pulled low by a standard TTL gate drive. Whenever a "1" is written to a line, a low impedance pull-up (250Ω) is switched in momentarily (500 ns) to provide a fast transition from 0 to 1. When a "0" is written to the line, a low impedance pull-down (300Ω) is active to provide TTL current sinking capability.

To use a particular PORT pin as an input, a logic "1" must first be written to that pin.

NOTE:
A $\overline{\text{RESET}}$ initializes all PORT pins to the high impedance logic "1" state.

An external TTL device connected to the pin has sufficient current sinking capability to pull-down the pin to the low state. An IN A, Pp instruction will sample the status of PORT pin and will input the proper logic level. With no external input connected, the IN A,Pp instruction inputs the previous output status.

This structure allows input and output information on the same pin and also allows any mix of input and output lines on the same port. However, when inputs and outputs are mixed on one PORT, a PORT write will cause the strong internal pull-ups to turn on at all inputs. If a switch or other low impedance device is connected to an input, a PORT write ("1" to an input) could cause current limits on internal lines to be exceeded. Figure 2-19 illustrates the recommended connection when inputs and outputs are mixed on one PORT.

The bidirectional port structure in combination with the UPI-41A/41AH/42/42AH logical AND and OR instructions provide an efficient means for handling single line inputs and outputs within an 8-bit processor.

PORTS 4, 5, 6, and 7

By using an 8243 I/O expander, 16 additional I/O lines can be connected to the UPI-41AH, 42AH and directly addressed as 4-bit I/O ports using UPI-41AH, 42AH

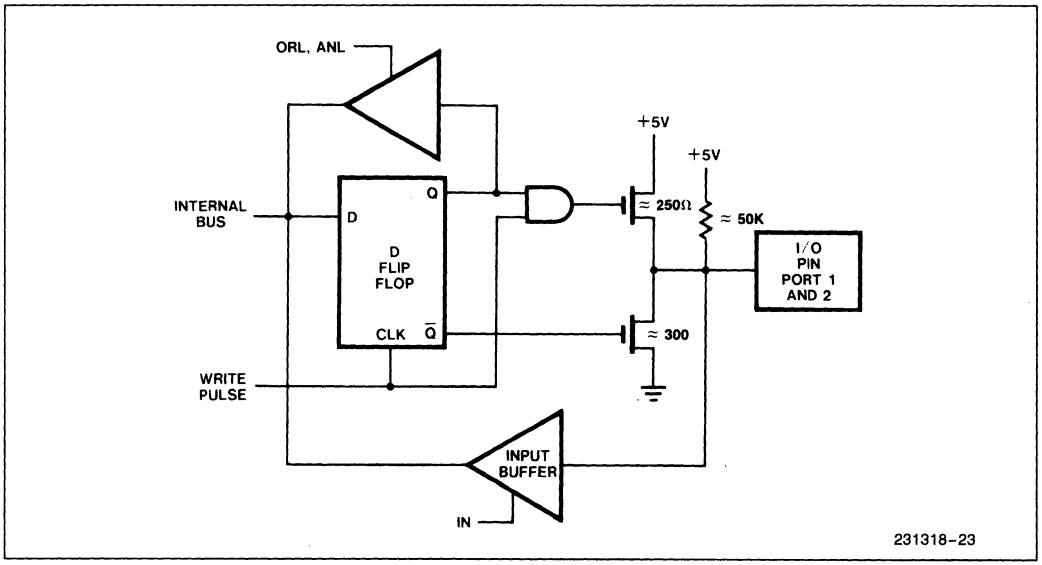


Figure 2-18. Quasi-Bidirectional Port Structure

instructions. This feature saves program space and design time, and improves the bit handling capability of the UPI-41A/41AH/42/42AH.

The lower half of PORT 2 provides an interface to the 8243 as illustrated in Figure 2-20. The PROG pin is used as a strobe to clock address and data information via the PORT 2 interface. The extra 16 I/O lines are referred to in UPI software as PORTS 4, 5, 6, and 7. Each PORT can be directly addressed and can be ANDed and ORed with an immediate data mask. Data can be moved directly to the accumulator from the expander PORTS (or vice-versa).

The 8243 I/O ports, PORTS 4, 5, 6, and 7, provide more drive capability than the UPI-41A/41AH/42/42AH bidirectional ports. The 8243 output is capable of driving about 5 standard TTL loads.

Multiple 8243's can be connected to the PORT 2 interface. In normal operation, only one of the 8243's would be active at the time an Input or Output command is executed. The upper half of PORT 2 is used to provide chip select signals to the 8043's. Figure 2-21 shows how four 8243's could be connected. Software is needed to select and set the proper PORT 2 pin before an INPUT or OUTPUT command to PORTS 4–7 is executed. In general, the software overhead required is very minor compared to the added flexibility of having a large number of I/O pins available.

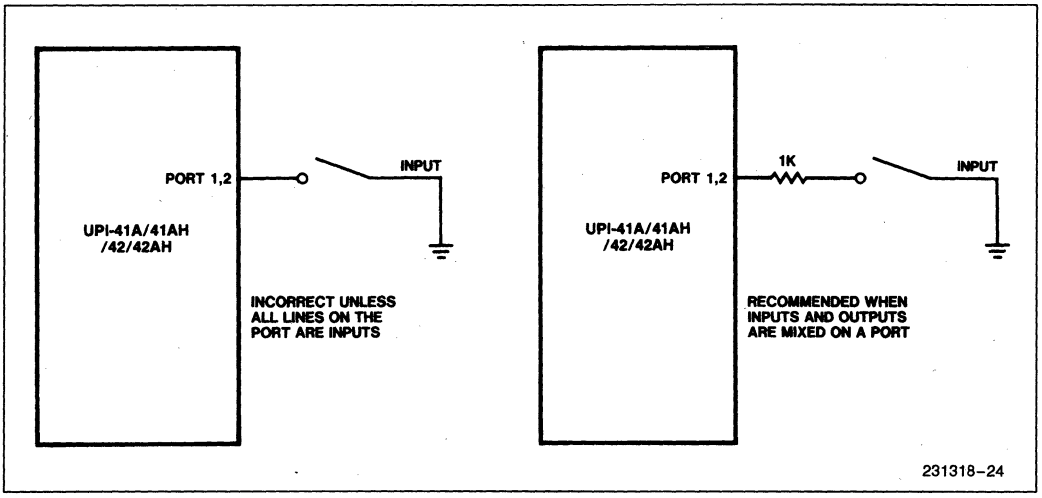


Figure 2-19. Recommended PORT Input Connections

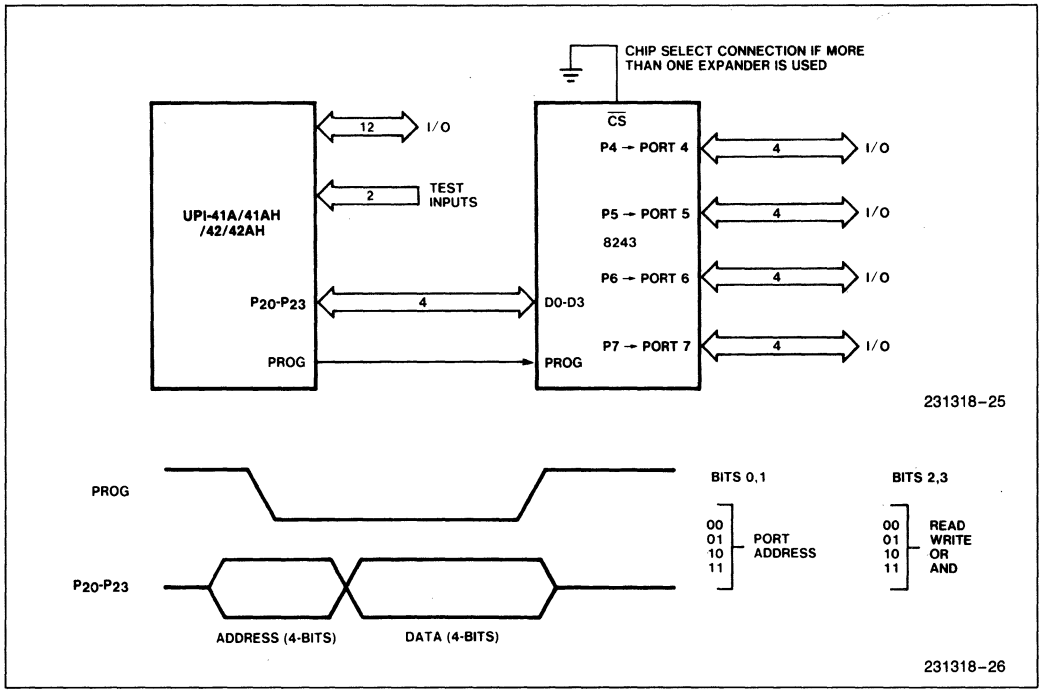


Figure 2-20. 8243 Expander Interface

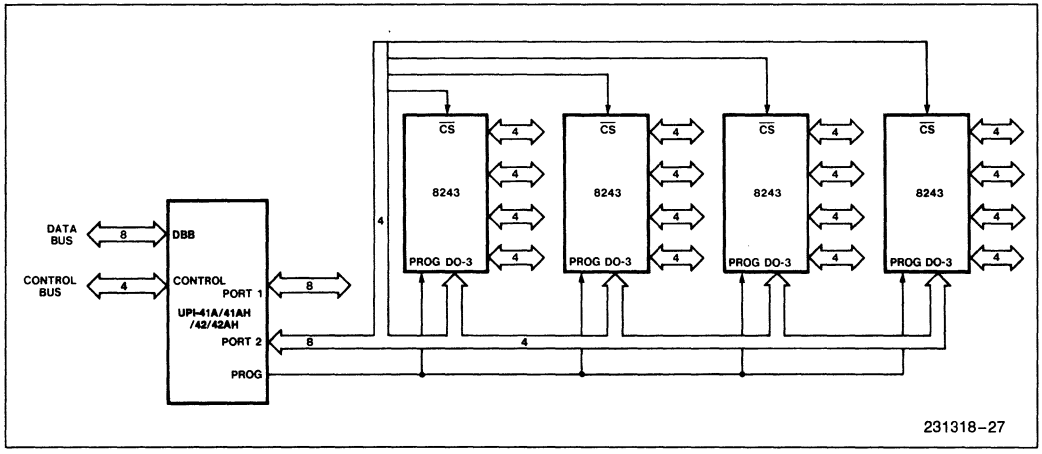


Figure 2-21. Multiple 8243 Expansion

CHAPTER 3
INSTRUCTION SET

The UPI-41A/41AH/42/42AH Instruction Set is op-code-compatible with the MCS-48 set except for the elimination of external program and data memory instructions and the addition of the data bus buffer instructions. It is very straightforward and efficient in its use of program memory. All instructions are either 1 or 2 bytes in length (over 70% are only 1 byte long) and over half of the instructions execute in one machine cycle. The remainder require only two cycles and include Branch, Immediate, and I/O operations.

The UPI-41A/41AH/42/42AH Instruction Set efficiently handles the single-bit operations required in control applications. Special instructions allow port bits to be set or cleared individually. Also, any accumulator bit can be directly tested via conditional branch instructions. Additional instructions are included to simplify loop counters, table look-up routines and N-way branch routines.

The UPI-41A/41AH/42/42AH Microcomputer handles arithmetic operations in both binary and BCD for efficient interface to peripherals such as keyboards and displays.

The instruction set can be divided into the following groups:

- Data Moves
- Accumulator Operations
- Flags
- Register Operations
- Branch Instructions
- Control
- Timer Operations
- Subroutines
- Input/Output Instructions

Data Moves (See Instruction Summary)

The 8-bit accumulator is the control point for all data transfers within the UPI-41A/41AH/42/42AH. Data can be transferred between the 8 registers of each working register bank and the accumulator directly (i.e., with a source or destination register specified by 3 bits in the instruction). The remaining locations in the RAM array are addressed either by R_0 or R_1 of the active register bank. Transfers to and from RAM require one cycle.

Constants stored in Program Memory can be loaded directly into the accumulator or the eight working registers. Data can also be transferred directly between the accumulator and the on-board timer/counter, the Status Register (STS), or the Program Status Word (PSW). Transfers to the STS register alter bits 4–7 only. Transfers to the PSW alter machine status accordingly and provide a means of restoring status after an interrupt or of altering the stack pointer if necessary.

Accumulator Operations

Immediate data, data memory, or the working registers can be added (with or without carry) to the accumulator. These sources can also be ANDed, ORed, or exclusive ORed to the accumulator. Data may be moved to or from the accumulator and working registers or data memory. The two values can also be exchanged in a single operation.

The lower 4 bits of the accumulator can be exchanged with the lower 4 bits of any of the internal RAM locations. This operation, along with an instruction which swaps the upper and lower 4-bit halves of the accumulator, provides easy handling of BCD numbers and other 4-bit quantities. To facilitate BCD arithmetic a Decimal Adjust instruction is also included. This instruction is used to correct the result of the binary addition of two 2-digit BCD numbers. Performing a decimal adjust on the result in the accumulator produces the desired BCD result.

The accumulator can be incremented, decremented, cleared, or complemented and can be rotated left or right 1 bit at a time with or without carry.

A subtract operation can be easily implemented in UPI software using three single-byte, single-cycle instructions. A value can be subtracted from the accumulator by using the following instructions:

- Complement the accumulator
- Add the value to the accumulator
- Complement the accumulator

Flags

There are four user accessible flags:

- Carry
- Auxiliary Carry
- F_0
- F_1

The Carry flag indicates overflow of the accumulator, while the Auxiliary Carry flag indicates overflow between BCD digits and is used during decimal adjust

operations. Both Carry and Auxiliary Carry are part of the Program Status Word (PSW) and are stored in the stack during subroutine calls. The F_0 and F_1 flags are general-purpose flags which can be cleared or complemented by UPI instructions. F_0 is accessible via the Program Status Word and is stored in the stack with the Carry flags. F_1 reflects the condition of the A_0 line, and caution must be used when setting or clearing it.

Register Operations

The working registers can be accessed via the accumulator as explained above, or they can be loaded with immediate data constants from program memory. In addition, they can be incremented or decremented directly, or they can be used as loop counters as explained in the section on branch instructions.

Additional Data Memory locations can be accessed with indirect instructions via R_0 and R_1.

Branch Instructions

The UPI-41A/41AH/42/42AH Instruction Set includes 17 jump instructions. The unconditional allows jumps anywhere in the 1K words of program memory. All other jump instructions are limited to the current page (256 words) of program memory.

Conditional jump instructions can test the following inputs and maching flags:

- TEST 0 input pin
- TEST 1 input pin
- Input Buffer Full flag
- Output Buffer Full flag
- Timer flag
- Accumulator zero
- Accumulator bit
- Carry flag
- F_0 flag
- F_1 flag

The conditions tested by these instructions are the instantaneous values at the time the conditional jump instruction is executed. For instance, the jump on accumulator zero instruction tests the accumulator itself, not an intermediate flag.

The decrement register and jump if not zero (DJNZ) instruction combines decrement and branch operations in a single instruction which is useful in implementing a loop counter. This instruction can designate any of the 8 working registers as a counter and can effect a branch to any address within the current page of execution.

A special indirect jump instruction (JMPP @A) allows the program to be vectored to any one of several different locations based on the contents of the accumulator. The contents of the accumulator point to a location in program memory which contains the jump address. As an example, this instruction could be used to vector to any one of several routines based on an ASCII character which has been loaded into the accumulator. In this way, ASCII inputs can be used to initiate various routines.

Control

The UPI-41A/41AH/42/42AH Instruction Set has six instructions for control of the DMA, interrupts, and selection of working registers banks.

The UPI-41A/41AH/42/42AH provides two instructions for control of the external microcomputer system. IBF and OBF flags can be routed to PORT 2 allowing interrupts of the external processor. DMA handshaking signals can also be enabled using lines from PORT 2.

The IBF interrupt can be enabled and disabled using two instructions. Also, the interrupt is automatically disabled following a RESET input or during an interrupt service routine.

The working register bank switch instructions allow the programmer to immediately substitute a second 8 register bank for the one in use. This effectively provides either 16 working registers or the means for quickly saving the contents of the first 8 registers in response to an interrupt. The user has the option of switching register banks when an interrupt occurs. However, if the banks are switched, the original bank will automatically be restored upon execution of a return and restore status (RETR) instruction at the end of the interrupt service routine.

Timer

The 8-bit on-board timer/counter can be loaded or read via the accumulator while the counter is stopped or while counting.

The counter can be started as a timer with an internal clock source or as an event counter or timer with an

external clock applied to the TEST 1 pin. The instruction executed determines which clock source is used. A single instruction stops the counter whether it is operating with an internal or an external clock source. In addition, two instructions allow the timer interrupt to be enabled or disabled.

Subroutines

Subroutines are entered by executing a call instruction. Calls can be made to any address in the 1K word program memory. Two separate return instructions determine whether or not status (i.e., the upper 4 bits of the PSW) is restored upon return from a subroutine.

Input/Output Instructions

Two 8-bit data bus buffer registers (DBBIN and DBBOUT) and an 8-bit status register (STS) enable the UPI-41A universal peripheral interface to communicate with the external microcomputer system. Data can be INputted from the DBBIN register to the accumulator. Data can be OUTputted from the accumulator to the DBBOUT register.

The STS register contains four user-definable bits (ST_4–ST_7) plus four reserved status bits (IBF, OBF, F_0 and F_1). The user-definable bits are set from the accumulator.

The UPI-41A/41AH/42/42AH peripheral interface has two 8-bit static I/O ports which can be loaded to and from the accumulator. Outputs are statically latched but inputs to the ports are sampled at the time an IN instruction is executed. In addition, immediate data from program memory can be ANDed and ORed directly to PORTS 1 and 2 with the result remaining on the port. This allows "masks" stored in program memory to be used to set or reset individual bits on the I/O ports. PORTS 1 and 2 are configured to allow input on a given pin by first writing a "1" to the pin.

Four additional 4-bit ports are available through the 8243 I/O expander device. The 8243 interfaces to the UPI-41A/41AH/42/42AH peripheral interface via four PORT 2 lines which form an expander bus. The 8243 ports have their own AND and OR instructions like the on-board ports, as well as move instructions to transfer data in or out. The expander AND or OR instructions, however, combine the contents of the accumulator with the selected port rather than with immediate data as is done with the on-board ports.

INSTRUCTION SET DESCRIPTION

The following section provides a detailed description of each UPI instruction and illustrates how the instructions are used.

For further information about programming the UPI, consult the *8048/8041AH Assembly Language Manual.*

Table 3-1. Symbols and Abbreviations Used

Symbol	Definition
A	Accumulator
C	Carry
DBBIN	Data Bus Buffer Input
DBBOUT	Data Bus Buffer Output
F_0, F_1	FLAG 0, FLAG 1 (C/D flag)
I	Interrupt
P	Mnemonic for "in-page" operation
PC	Program Counter
Pp	Port designator (p = 1, 2, or 4–7)
PSW	Program Status Word
Rr	Register designator (r = 0–7)
SP	Stack Pointer
STS	Status register
T	Timer
TF	Timer Flag
T_0, T_1	TEST 0, TEST 1
#	Immediate data prefix
@	Indirect address prefix
(( ))	Double parentheses show the effect of @, that is @RO is shown as ((RO)).
( )	Contents of

Table 3-2. Instruction Set Summary

Mnemonic	Description	Bytes	Cycle
ACCUMULATOR			
ADD A, Rr	Add register to A	1	1
ADD A, @Rr	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	2
ADDC A, Rr	Add register to A with carry	1	1
ADDC A, @Rr	Add data memory to A with carry	1	1
ADDC A, #data	Add immediate to A with carry	2	2
ANL A, Rr	And register to A	1	1
ANL A, @Rr	And data memory to A	1	1
ANL A, #data	And immediate to A	2	2
ORL A, Rr	Or register to A	1	1
ORL A, @Rr	Or data memory to A	1	1
ORL A, #data	Or immediate to A	2	2
XRL A, Rr	Exclusive Or register to A	1	1
XRL A, @Rr	Exclusive Or data memory to A	1	1
XRL A, #data	Exclusive Or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal Adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
INPUT/OUTPUT			
IN A, Pp	Input port to A	1	2
OUTL Pp, A	Output A to port	1	2
ANL Pp, #data	And immediate to port	2	2
ORL Pp, #data	Or immediate to port	2	2
IN A,DBB	Input DDB to A, clear IBF	1	1
OUT DBB, A	Output A to DBB, Set OBF	1	1
MOV STS,A	A_4–A_7 to bits 4–7 of status	1	1
MOVD A,Pp	Input Expander port to A	1	2
MOVD Pp,A	Output A to Expander port	1	2
ANLD Pp,A	And A to Expander port	1	2
ORLD Pp,A	Or A to Expander port	1	2
DATA MOVES			
MOV A, Rr	Move register to A	1	1
MOV A, @Rr	Move data memory to A	1	1
MOV A, #data	Move immediate to A	2	2
MOV Rr, A	Move A to register	1	1
MOV @Rr, A	Move A to data memory	1	1
MOV Rr, #data	Move immediate to register	2	2
MOV @Rr, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, Rr	Exchange A and registers	1	1
XCH A, @Rr	Exchange A and data memory	1	1
XCHD A, @Rr	Exchange digit of A and register	1	1

Mnemonic	Description	Bytes	Cycle
DATA MOVES (Continued)			
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @A	Move to A from page 3	1	2
TIMER/COUNTER			
MOV A,T	Read Timer/Counter	1	1
MOV T,A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	Start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/Counter Interrupt	1	1
DIS TCNTI	Disable Timer/Counter Interrupt	1	1
CONTROL			
EN DMA	Enable DMA Handshake Lines	1	1
EN I	Enable IBF interrupt	1	1
DIS I	Disable IBF interrupt	1	1
EN FLAGS	Enable Master Interrupts	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
NOP	No Operation	1	1
REGISTERS			
INC Rr	Increment register	1	1
INC @Rr	Increment data memory	1	1
DEC Rr	Decrement register	1	1
SUBROUTINE			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2
FLAGS			
CLR C	Clear Carry	1	1
CPL C	Complement Carry	1	1
CLR F0	Clear Flag 0	1	1
CPL F0	Complement Flag 0	1	1
CLR F1	Clear F_1 Flag	1	1
CPL F1	Complement F_1 Flag	1	1
BRANCH			
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ Rr, addr	Decrement register and jump on non-zero	2	2
JC addr	Jump on Carry = 1	2	2
JNC addr	Jump on Carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JT0 addr	Jump on T_0 = 1	2	2
JNT0 addr	Jump on T_0 = 0	2	2
JT1 addr	Jump on T_1 = 1	2	2
JNT1 addr	Jump on T_1 = 0	2	2
JF0 addr	Jump on F_0 Flag = 1	2	2
JF1 addr	Jump on F_1 Flag = 1	2	2
JTF addr	Jump on Timer Flag = 1	2	2
JNIBF addr	Jump on IBF Flag = 0	2	2
JOBF addr	Jump on OBF Flag = 1	2	2
JBb addr	Jump on Accumulator Bit	2	2

ALPHABETIC LISTING

ADD A,Rr Add Register Contents to Accumulator

Opcode: | 0 1 1 0 | 1 r_2 r_1 r_0 |

The contents of register 'r' are added to the accumulator. Carry is affected.
(A) ← (A) + (Rr) r = 0–7

Example:
```
ADDREG: ADD A,R6        ;ADD REG 6 CONTENTS
                        ;TO ACC
```

ADD A,@Rr Add Data Memory Contents to Accumulator

Opcode: | 0 1 1 0 | 0 0 0 r |

The contents of the standard data memory location address by register 'r' bits 0–7 are added to the accumulator. Carry is affected.

(A) ← (A) + ((Rr)) r = 0–1

Example:
```
ADDM: MOV RO,#47        ;MOVE 47 DECIMAL TO REG 0
      ADD A,@RO         ;ADD VALUE OF LOCATION
                        ;47 TO ACC
```

ADD A,#data Add Immediate Data to Accumulator

Opcode: | 0 0 0 0 | 0 0 1 1 | • | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 |

This is a 2-cycle instruction. The specified data is added to the accumulator. Carry is affected.
(A) ← (A) + data

Example:
```
ADDID: ADD A,#ADDER     ;ADD VALUE OF SYMBOL
                        ;ADDER' TO ACC
```

ADDC A,Rr Add Carry and Register Contents to Accumulator

Opcode: | 0 1 1 1 | 1 r_2 r_1 r_0 |

The content of the carry bit is added to accumulator location 0. The contents of register 'r' are then added to the accumulator. Carry is affected.
(A) ← (A) + (Rr) + (C) r = 0–7

Example:
```
ADDRGC: ADDC A,R4       ;ADD CARRY AND REG 4
                        ;CONTENTS TO ACC
```

ADDC A,@Rr Add Carry and Data Memory Contents to Accumulator

Opcode:

0 1 1 1	0 0 0 r

The content of the carry bit is added to accumulator location 0. Then the contents of the standard data memory location addressed by register 'r' bits 0–7 are added to the accumulator. Carry is affected.

(A) ← (A) + ((Rr)) + (C) r = 0–1

Example:

```
ADDMC: MOV R1,#40      ;MOV '40' DEC TO REG 1
       ADDC A,@R1      ;ADD CARRY AND LOCATION 40
                       ;CONTENTS TO ACC
```

ADDC A,#data Add Carry and Immediate Data to Accumulator

Opcode:

0 0 0 1	0 0 1 1	•	d_7 d_6 d_5 d_4	d_3 d_2 d_1 d_0

This is a 2-cycle instruction. The content of the carry bit is added to accumulator location 0. Then the specified data is added to the accumulator. Carry is affected.

(A) ← (A) + data + (C)

Example:

```
ADDC A,#255            ;ADD CARRY AND '225' DEC
                       ;TO ACC
```

ANL A,Rr Logical AND Accumulator With Register Mask

Opcode:

0 1 0 1	1 r_2 r_1 r_0

Data in the accumulator is logically ANDed with the mask contained in working register 'r'.

(A) ← (A) AND (Rr) r = 0–7

Example:

```
ANDREG: ANL A,R3       ;'AND' ACC CONTENTS WITH MASK
                       ;MASK IN REG 3
```

ANL A,@Rr Logical AND Accumulator With Memory Mask

Opcode:

0 1 0 1	0 0 0 r

Data in the accumulator is logically ANDed with the mask contained in the data memory location referenced by register 'r', bits 0–7.

(A) ← (A) AND ((Rr)) r = 0–1

Example:

```
ANDDM: MOV R0,#0FFH    MOV 'FF' HEX TO REG 0
       ANL A,#0AFH     ;'AND' ACC CONTENTS WITH
                       ;MASK IN LOCATION 63
```

ANL A,#data Logical AND Accumulator With Immediate Mask

Opcode:

0 1 0 1	0 0 1 1	•	d_7 d_6 d_5 d_4	d_3 d_2 d_1 d_0

This is a 2-cycle instruction. Data in the accumulator is logically ANDed with an immediately-specified mask.
(A) ← (A) AND data

Example:

```
ANDID: ANL A,#0AFH          ;'AND' ACC CONTENTS
                            ;WITH MASK 10101111
       ANL A,#3+X/Y         ;'AND' ACC CONTENTS
                            ;WITH VALUE OF EXP
                            '3+X/Y'
```

ANL PP,#data Logical AND PORT 1–2 With Immediate Mask

Opcode:

1 0 0 1	1 0 p_1 p_0	•	d_7 d_6 d_5 d_4	d_3 d_2 d_1 d_0

This is a 2-cycle instruction. Data on the port 'p' is logically ANDed with an immediately-specified mask.
(Pp) ← (Pp) AND data p = 1–2

Note: Bits 0–1 of the opcode are used to represent PORT 1 and PORT 2. If you are coding in binary rather than assembly language, the mapping is as follows:

Bits	p1	p0	Port
	0	0	X
	0	1	1
	1	0	2
	1	1	X

Example:

```
ANDP2: ANL P2,#OF0H         ;'AND' PORT 2 CONTENTS
                            ;WITH MASK'F0' HEX
                            ;(CLEAR P20–23)
```

ANLD Pp,A Logical AND Port 4–7 With Accumulator Mask

Opcode:

1 0 0 1	1 1 p_1 p_0

This is a 2-cycle instruction. Data on port 'p' on the 8243 expander is logically ANDed with the digit mask contained in accumulator bits 0–3.
(Pp) ← (Pp) AND (A0–3) p = 4–7

Note: The mapping of Port 'p' to opcode bits p_1, p_0 is as follows:

P1	P0	Port
0	0	4
0	1	5
1	0	6
1	1	7

Example:

```
ANDP4: ANLD P4,A            ;'AND' PORT 4 CONTENTS
                            ;WITH ACC BITS 0–3
```

CALL address Subroutine Call

Opcode:

a_{10} a_9 a_8 1	0 1 0 0	•	a_7 a_6 a_5 a_4	a_3 a_2 a_1 a_0

This is a 2-cycle instruction. The program counter and PSW bits 4–7 are saved in the stack. The stack pointer (PSW bits 0–2) is updated. Program control is then passed to the location specified by 'address'.

Execution continues at the instruction following the CALL upon return from the subroutine.
((SP)) ← (PC), (PSW_{4-7})
(SP) ← (SP) + 1
(PC_{8-9}) ← ($addr_{8-9}$)
(PC_{0-7}) ← ($addr_{0-7}$)

Example: Add three groups of two numbers. Put subtotals in locations 50, 51 and total in location 52.

```
          MOV R0,#50        ;MOVE '50' DEC TO ADDRESS
                            ;REG 0
BEGADD:   MOV A,R1          ;MOVE CONTENTS OF REG 1
                            ;TO ACC
          ADD A,R2          ;ADD REG 2 TO ACC
          CALL SUBTOT       ;CALL SUBROUTINE 'SUBTOT'
          ADD A,R3          ;ADD REG 3 TO ACC
          ADD A,R4          ;ADD REG 4 TO ACC
          CALL SUBTOT       ;CALL SUBROUTINE 'SUBTOT'
          ADD A,R5          ;ADD REG 5 TO ACC
          ADD A,R6          ;ADD REG 6 TO ACC
          CALL SUBTOT       ;CALL SUBROUTINE 'SUBTOT'
                  •
                  •
                  •
SUBTOT:   MOV @R0,A         ;MOVE CONTENTS OF ACC TO
                            ;LOCATION ADDRESSED BY
                            ;REG 0
          INC R0            ;INCREMENT REG 0
          RET               ;RETURN TO MAIN PROGRAM
```

CLR A Clear Accumulator

Opcode:

0 0 1 0	0 1 1 1

The contents of the accumulator are cleared to zero.
(A) ← 00H

CLR C Clear Carry Bit

Opcode:

1 0 0 1	0 1 1 1

During normal program execution, the carry bit can be set to one by the ADD, ADDC, RLC, CPLC, RRC, and DAA instructions. This instruction resets the carry bit to zero.
(C) ← 0

CLR F1 Clear Flag 1

Opcode:

1 0 1 0	0 1 0 1

The F_1 flag is cleared to zero.
(F_1) ← 0

CLR F0 Clear Flag 0

Opcode:

1 0 0 0	0 1 0 1

F_0 flag is cleared to zero.
$(F_0) \leftarrow 0$

CPL A Complement Accumulator

Opcode:

0 0 1 1	0 1 1 1

The contents of the accumulator are complemented. This is strictly a one's complement. Each one is changed to zero and vice-versa.
(A) ← NOT (A)

Example: Assume accumulator contains 01101010.

```
CPLA: CPL A          ;ACC CONTENTS ARE COMPLE-
                     ;MENTED TO 10010101
```

CPL C Complement Carry Bit

Opcode:

1 0 1 0	0 1 1 1

The setting of the carry bit is complemented; one is changed to zero, and zero is changed to one.
(C) ← NOT (C)

Example: Set C to one; current setting is unknown.

```
CT01: CLR C          ;C IS CLEARED TO ZERO
      CPL C          ;C IS SET TO ONE
```

CPL F0 COMPLEMENT FLAG 0

Opcode:

1 0 0 1	0 1 0 1

The setting of Flag 0 is complemented; one is changed to zero, and zero is changed to one.
$F_0 \leftarrow$ NOT (F0)

CPL F1 Complement Flag 1

Opcode:

1 0 1 1	0 1 0 1

The setting of the F_1 Flag is complemented; one is changed to zero, and zero is changed to one.
$(F_1) \leftarrow$ NOT (F_1)

DA A Decimal Adjust Accumulator

Opcode:

0 1 0 1	0 1 1 1

The 8-bit accumulator value is adjusted to form two 4-bit Binary Coded Decimal (BCD) digits following the binary addition of BCD numbers. The carry bit C is affected. If the contents of bits 0–3 are greater than nine, or if AC is one, the accumulator is incremented by six.

The four high-order bits are then checked. If bits 4–7 exceed nine, or if C is one, these bits are increased by six. If an overflow occurs, C is set to one; otherwise, it is cleared to zero.

Example: Assume accumulator contains 9AH.

```
        DA  A              ;ACC ADJUSTED TO 01H with C set
        C   AC             ACC
        0   0              9AH   INITIAL CONTENTS
                           06H   ADD SIX TO LOW DIGIT
        0   0              A1H
                           60H   ADD SIX HIGH DIGIT

        1   0              01H   RESULT
```

DEC A Decrement Accumulator

Opcode:

0 0 0 0	0 1 1 1

The contents of the accumulator are decremented by one.
(A) ← (A) − 1

Example: Decrement contents of data memory location 63.

```
        MOV R0,#3FH        ;MOVE '3F' HEX TO REG 0
        MOV A,@R0          ;MOVE CONTENTS OF LOCATION 63
                           ;TO ACC
        DEC A              ;DECREMENT ACC
        MOV @R0,A          ;MOVE CONTENTS OF ACC TO
                           ;LOCATION 63
```

DEC Rr Decrement Register

Opcode:

1 1 0 0	1 r_2 r_1 r_0

The contents of working register 'r' are decremented by one.
(Rr) ← (Rr) − 1 r = 0–7

Example:

```
DECR1: DEC R1              ;DECREMENT ADDRESS REG 1
```

DIS I Disable IBF Interrupt

Opcode:

0 0 0 1	0 1 0 1

The input Buffer Full interrupt is disabled. The interrupt sequence is not initiated by $\overline{WR}$ and $\overline{CS}$, however, an IBF interrupt request is latched and remains pending until an EN I (enable IBF interrupt) instruction is executed.

Note: The IBF flag is set and cleared independent of the IBF interrupt request so that handshaking protocol can continue normally.

DIS TCNTI Disable Timer/Counter Interrupt

Opcode:

0 0 1 1	0 1 0 1

The timer/counter interrupt is disabled. Any pending timer interrupt request is cleared. The interrupt sequence is not initiated by an overflow, but the timer flag is set and time accumulation continues.

DJNZ Rr, address Decrement Register and Test

Opcode:

1 1 1 0	1 r_2 r_1 r_0	•	a_7 a_6 a_5 a_4	a_3 a_2 a_1 a_0

This is a 2-cycle instruction. Register 'r' is decremented and tested for zero. If the register contains all zeros, program control falls through to the next instruction. If the register contents are not zero, control jumps to the specified address within the current page.
(Rr) ← (Rr) − 1
If R ≠ 0, then;
(PC_{0-7}) ← addr

Note: A 10-bit address specification does not cause an error if the DJNZ instruction and the jump target are on the same page. If the DJNZ instruction begins in location 255 of a page, it will jump to a target address on the following page. Otherwise, it is limited to a jump within the current page.

Example: Increment values in data memory locations 50–54.

```
    MOV R0,#50          ;MOVE '50' DEC TO ADDRESS
                        ;REG 0
    MOV R3,#05          ;MOVE '5' DEC TO COUNTER
                        ;REG 3
INCRT: INC @R0          ;INCREMENT CONTENTS OF
                        ;LOCATION ADDRESSED BY
                        ;REG 0
    INC R0              ;INCREMENT ADDRESS IN REG 0
    DJNZ R3,INCRT       ;DECREMENT REG 3——JUMP TO
                        ;'INCRT' IF REG 3 NONZERO
    NEXT——              ;'NEXT' ROUTINE EXECUTED
                        ;IF R3 IS ZERO
```

EN DMA Enable DMA Handshake Lines

Opcode:

1 1 1 0	0 1 0 1

DMA handshaking is enabled using P_{26} as DMA request (DRQ) and P_{27} as DMA acknowledge ($\overline{DACK}$). The $\overline{DACK}$ lines forces $\overline{CS}$ and A_0 low internally and clears DRQ.

EN FLAGS Enable Master Interrupts

Opcode:

1 1 1 1	0 1 0 1

The Output Buffer Full (OBF) and the Input Buffer Full (IBF) flags (IBF is inverted) are routed to P_{24} and P_{25}. For proper operation, a "1" should be written to P_{25} and P_{24} before the EN FLAGS instruction. A "0" written to P_{24} or P_{25} disables the pin.

EN I Enable IBF Interrupt

Opcode:

0 0 0 0	0 1 0 1

The Input Buffer Full interrupt is enabled. A low signal on $\overline{WR}$ and $\overline{CS}$ initiates the interrupt sequence.

EN TCNTI Enable Timer/Counter Interrupt

Opcode:

0 0 1 0	0 1 0 1

The timer/counter interrupt is enabled. An overflow of this register initiates the interrupt sequence.

IN A,DBB Input Data Bus Buffer Contents to Accumulator

Opcode:

0 0 1 0	0 0 1 0

Data in the DBBIN register is transferred to the accumulator and the Input Buffer Full (IBF) flag is set to zero.
(A) ← (DBB)
(IBF) ← 0

Example:

```
INDBB: IN A,DBB          ;INPUT DBBIN CONTENTS TO
                         ;ACCUMULATOR
```

IN A,Pp Input Port 1-2 Data to Accumulator

Opcode:

0 0 0 0	1 0 p_1 p_0

This is a 2-cycle instruction. Data present on port 'p' is transferred (read) to the accumulator.
(A) ← (Pp) p = 1-2 (see ANL instruction)

Example:

```
INP 12: IN A,P1          ;INPUT PORT 1 CONTENTS
                         ;TO ACC
        MOV R6,A         ;MOVE ACC CONTENTS TO
                         ;REG 6
        IN A,P2          ;INPUT PORT 2 CONTENTS
                         ;TO ACC
        MOV R7,A         ;MOVE ACC CONTENTS TO REG 7
```

INC A Increment Accumulator

Opcode:

0 0 0 1	0 1 1 1

The contents of the accumulator are incremented by one.
(A) ← (A) + 1

Example: Increment contents of location 10 in data memory.

```
INCA: MOV R0,#10         ;MOV '10' DEC TO ADDRESS
                         ;REG 0
      MOV A,@R0          ;MOVE CONTENTS OF LOCATION
                         ;10 TO ACC
      INC A              ;INCREMENT ACC
      MOV @R0,A          ;MOVE ACC CONTENTS TO
                         ;LOCATION 10
```

INC Rr Increment Register

Opcode: | 0 0 0 1 | 1 r_2 r_1 r_0 |

The contents of working register 'r' are incremented by one.
(Rr) ← (Rr) + 1 r = 0–7

Example:
```
INCR0: INC R0          ;INCREMENT ADDRESS REG 0
```

INC @Rr Increment Data Memory Location

Opcode: | 0 0 0 1 | 0 0 0 r |

The contents of the resident data memory location addressed by register 'r' bits 0–7 are incremented by one.
((Rr)) ← ((Rr)) + 1 r = 0–1

Example:
```
INCDM: MOV R1,#OFFH    ;MOVE ONES TO REG 1
       INC @R1         ;INCREMENT LOCATION 63
```

JBb address Jump If Accumulator Bit is Set

Opcode: | b_2 b_1 b_0 1 | 0 0 1 0 | • | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

This is a 2-cycle instruction. Control passes to the specified address if accumulator bit 'b' is set to one.
(PC_{0-7}) addr if b = 1
(PC) ← (PC) + 2 if b = 0

Example:
```
JB4IS1: JB4 NEXT       ;JUMP TO 'NEXT' ROUTINE
                       ;IF ACC BIT 4 = 1
```

JC address Jump If Carry Is Set

Opcode: | 1 1 1 1 | 0 1 1 0 | • | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

This is a 2-cycle instruction. Control passes to the specified address if the carry bit is set to one.
(PC_{0-7}) ← addr if C = 1
(PC) ← (PC) + 2 if C = 0

Example:
```
JC1: JC OVERFLOW       ;JUMP TO 'OVFLOW' ROUTINE
                       ;IF C = 1
```

JF0 address Jump If Flag 0 is Set

Opcode: | 1 0 1 1 | 0 1 1 0 | • | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

This is a 2-cycle instruction. Control passes to the specified address if flag 0 is set to one.
(PC_{0-7}) ← addr if F_0 = 1

Example:
```
JF0IS1: JF0 TOTAL      ;JUMP TO 'TOTAL' ROUTINE
                       ;IF F0 = 1
```

JF1 address Jump If C/D Flag (F1) Is Set

Opcode: | 0 1 1 1 | 0 1 1 0 | • | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

This is a 2-cycle instruction. Control passes to the specified address if the C/D flag (F_1) is set to one.

$(PC_{0-7}) \leftarrow$ addr if $F_1 = 1$

Example:
```
JF 1IS1: JF1 FILBUF     ;JUMP TO 'FILBUF'
                        ;ROUTINE IF F1 = 1
```

JMP address Direct Jump Within 1K Block

Opcode: | a_{10} a_9 a_8 0 | 0 1 0 0 | • | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

This is a 2-cycle instruction. Bits 0–10 of the program counter are replaced with the directly-specified address.

$(PC_{8-10}) \leftarrow$ addr 8–10

$(PC_{0-7}) \leftarrow$ addr 0–7

Example:
```
JMP SUBTOT      ;JUMP TO SUBROUTINE 'SUBTOT'
JMP $-6         ;JUMP TO INSTRUCTION SIX LOCATIONS
                ;BEFORE CURRENT LOCATION
JMP 2FH         ;JUMP TO ADDRESS '2F' HEX
```

JMPP @A Indirect Jump Within Page

Opcode: | 1 0 1 1 | 0 0 1 1 |

This is a 2-cycle instruction. The contents of the program memory location pointed to by the accumulator are substituted for the 'page' portion of the program counter (PC 0–7).

$(PC_{0-7}) \leftarrow ((A))$

Example:
```
Assume accumulator contains OFH
JMPPAG: JMPP @A     ;JMP TO ADDRESS STORED IN
                    ;LOCATION 15 IN CURRENT PAGE
```

JNC address Jump If Carry Is Not Set

Opcode: | 1 1 1 0 | 0 1 1 0 | • | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

This is a 2-cycle instruction. Control passes to the specified address if the carry bit is not set, that is, equals zero.

$(PC_{0-7}) \leftarrow$ addr if $C = 0$

Example:
```
JC0: JNC NOVFLO     ;JUMP TO 'NOVFLO' ROUTINE
                    ;IF C = 0
```

JNIBF address Jump If Input Buffer Full Flag Is Low

Opcode: | 1 1 0 1 | 0 1 1 0 | • | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

This is a 2-cycle instruction. Control passes to the specified address if the Input Buffer Full flag is low (IBF = 0).

$(PC_{0-7}) \leftarrow$ addr if IBF = 0

Example:
```
LOC 3:JNIBF LOC 3   ;JUMP TO SELF IF IBF = 0
                    ;OTHERWISE CONTINUE
```

JNTO address Jump if TEST 0 is Low

Opcode: 0 0 1 0 | 0 1 1 0 • a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0

This is a 2-cycle instruction. Control passes to the specified address, if the TEST 0 signal is low. Pin is sampled during SYNC.

$(PC_{0-7}) \leftarrow$ addr if $T_0 = 0$

Example:
```
JT0LOW: JNT0 60      ;JUMP TO LOCATION 60 DEC
                     ;IF T0 = 0
```

JNT1 address Jump If TEST 1 is Low

Opcode: 0 1 0 0 | 0 1 1 0 • a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0

This is a 2-cycle instruction. Control passes to the specified address if the TEST 1 signal is low. Pin is sampled during SYNC.

$(PC_{0-7}) \leftarrow$ addr if $T_1 = 0$

Example:
```
JT1LOW: JNT1 OBBH    ;JUMP TO LOCATION 'BB' HEX
                     ;IF T1 = 0
```

JNZ address Jump If Accumulator Is Not Zero

Opcode: 1 0 0 1 | 0 1 1 0 • a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0

This is a 2-cycle instruction. Control passes to the specified address if the accumulator contents are nonzero at the time this instruction is executed.

$(PC_{0-7}) \leftarrow$ addr if $A \neq 0$

Example:
```
JACCNO: JNZ OABH     ;JUMP TO LOCATION 'AB' HEX
                     ;IF ACC VALUE IS NONZERO
```

JOBF Address Jump If Output Buffer Full Flag Is Set

Opcode: 1 0 0 0 | 0 1 1 0 • a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0

This is a 2-cycle instruction. Control passes to the specified address if the Output Buffer Full (OBF) flag is set (= 1) at the time this instruction is executed.

$(PC_{0-7}) \leftarrow$ addr if OBF = 1

Example:
```
JOBFHI: JOBF OAAH    ;JUMP TO LOCATION 'AA' HEX
                     ;IF OBF = 1
```

JTF address Jump If Timer Flag is Set

Opcode: 0 0 0 1 | 0 1 1 0 • a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0

This is a 2-cycle instruction. Control passes to the specified address if the timer flag is set to one, that is, the timer/counter register overflows to zero. The timer flag is cleared upon execution of this instruction. (This overflow initiates an interrupt service sequence if the timer-overflow interrupt is enabled.)

$(PC_{0-7}) \leftarrow$ addr if TF = 1

Example:
```
JTF1: JTF TIMER      ;JUMP TO 'TIMER' ROUTINE
                     ;IF TF = 1
```

JTO address Jump If TEST 0 Is High

Opcode: | 0 0 1 1 | 0 1 1 0 | • | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

This is a 2-cycle instruction. Control passes to the specified address if the TEST 0 signal is high (= 1). Pin is sampled during SYNC.
(PC_{0-7}) ← addr if $T_0 = 1$

Example:
```
JT0HI: JT0 53          ;JUMP TO LOCATION 53 DEC
                       ;IF T0 = 1
```

JT1 address Jump If TEST 1 Is High

Opcode: | 0 1 0 1 | 0 1 1 0 | • | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

This is a 2-cycle instruction. Control passes to the specified address if the TEST 1 signal is high (= 1). Pin is sampled during SYNC.
(PC_{0-7}) ← addr if $T_1 = 1$

Example:
```
JT1HI: JT1 COUNT       ;JUMP TO 'COUNT' ROUTINE
                       ;IF T1 = 1
```

JZ address Jump If Accumulator Is Zero

Opcode: | 1 1 0 0 | 0 1 1 0 | • | a_7 a_6 a_5 a_4 | a_3 a_2 a_1 a_0 |

This is a 2-cycle instruction. Control passes to the specified address if the accumulator contains all zeros at the time this instruction is executed.
(PC_{0-7}) ← addr if A = 0

Example:
```
JACCO: JZ OA3H         ;JUMP TO LOCATION 'A3' HEX
                       ;IF ACC VALUE IS ZERO
```

MOV A,#data Move Immediate Data to Accumulator

Opcode: | 0 0 1 0 | 0 0 1 1 | • | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 |

This is a 2-cycle instruction. The 8-bit value spedified by 'data' is loaded in the accumulator.
(A) ← data

Example:
```
MOV A,#OA3H            ;MOV 'A3' HEX TO ACC
```

MOV A,PSW Move PSW Contents to Accumulator

Opcode: | 1 1 0 0 | 0 1 1 1 |

The contents of the program status word are moved to the accumulator.
(A) ← (PSW)

Example: Jump to 'RB1SET' routine if bank switch, PSW bit 4, is set.
```
BSCHK: MOV A,PSW       ;MOV PSW CONTENTS TO ACC
       JB4 RB1 SET     ;JUMP TO 'RB1SET' IF ACC
                       ;BIT 4 = 1
```

4

MOV A,Rr Move Register Contents to Accumulator

Opcode:

1 1 1 1	1 r_2 r_1 r_0

Eight bits of data are moved from working register 'r' into the accumulator.
(A) ← (Rr) r = 0–7

Example:
```
MAR: MOV A,R3          ;MOVE CONTENTS OF REG 3
                       ;TO ACC
```

MOV A,@Rr Move Data Memory Contents to Accumulator

Opcode:

1 1 1 1	0 0 0 r

The contents of the data memory location addressed by bits 0–7 of register 'r' are moved to the accumulator. Register 'r' contents are unaffected.
(A) ← ((Rr)) r = 0–1

Example: Assume R1 contains 00110110.
```
MADM: MOV A,@R1        ;MOVE CONTENTS OF DATA MEM
                       ;LOCATION 54 TO ACC
```

MOV A,T Move Timer/Counter Contents to Accumulator

Opcode:

0 1 0 0	0 0 1 0

The contents of the timer/event-counter register are moved to the accumulator. The timer/event-counter is not stopped.
(A) ← (T)

Example: Jump to "Exit" routine when timer reaches '64', that is, when bit 6 is set—assuming initialization to zero.
```
TIMCHK: MOV A,T        ;MOVE TIMER CONTENTS TO
                       ;ACC
        JB6 EXIT       ;JUMP TO 'EXIT' IF ACC BIT
                       ;6 = 1
```

MOV PSW,A Move Accumulator Contents to PSW

Opcode:

1 1 0 1	0 1 1 1

The contents of the accumulator are moved into the program status word. All condition bits and the stack pointer are affected by this move.
(PSW) ← (A)

Example: Move up stack pointer by two memory locations, that is, increment the pointer by one.
```
INCPTR: MOV A,PSW      ;MOVE PSW CONTENTS TO ACC
        INC A          ;INCREMENT ACC BY ONE
        MOV PSW,A      ;MOVE ACC CONTENTS TO PSW
```

MOV Rr,A Move Accumulator Contents to Register

Opcode: | 1 0 1 0 | 1 r_2 r_1 r_0 |

The contents of the accumulator are moved to register 'r'
(Rr) ← (A) r = 0–7

Example:
```
MRA MOV R0,A        ;MOVE CONTENTS OF ACC TO
                    ;REG 0
```

MOV Rr,#data Move Immediate Data to Register

Opcode: | 1 0 1 1 | 1 r_2 r_1 r_0 | • | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 |

This is a 2-cycle instruction. The 8-bit value specified by 'data' is moved to register 'r'.
(Rr) ← data r = 0–7

Example:
```
MIR4: MOV R4,#HEXTEN    ;THE VALUE OF THE SYMBOL
                        ;'HEXTEN' IS MOVED INTO
                        ;REG 4
MIR5: MOV R5,#PI*(R*R)  ;THE VAUE OF THE
                        ;EXPRESSION 'PI*(R*R)'
                        ;IS MOVED INTO REG 5
MIR6: MOV R6,#OADH      ;'AD' HEX IS MOVED INTO
                        REG 6
```

MOV @Rr,A Move Accumulator Contents to Data Memory

Opcode: | 1 0 1 0 | 0 0 0 r |

The contents of the accumulator are moved to the data memory location whose address is specified by bits 0–7 of register 'r'. Register 'r' contents are unaffected.
((Rr)) ← (A) r = 0–1

Example:
```
Assume R0 contains 11000111.
MDMA: MOV @R,A      ;MOVE CONTENTS OF ACC TO
                    ;LOCATION 7 (REG)
```

MOV @Rr,#data Move Immediate Data to Data Memory

Opcode: | 1 0 1 1 | 0 0 0 r | • | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 |

This is a 2-cycle instruction. The 8-bit value specified by 'data' is moved to the standard data memory location addressed by register 'r', bit 0–7.

Example: Move the hexadecimal value AC3F to locations 62–63.
```
MIDM: MOV R0,#62        ;MOVE '62' DEC TO ADDR REG0
      MOV @R0,#OACH     ;MOVE 'AC' HEX TO LOCATION 62
      INC R0            ;INCREMENT REG 0 TO '63'
      MOV @R0,#3FH      ;MOVE '3F' HEX TO LOCATION 63
```

MOV STS,A Move Accumulator Contents to STS Register

Opcode:

1 0 0 1	0 0 0 0

The contents of the accumulator are moved into the status register. Only bits 4–7 are affected.
$(STS_{4-7}) \leftarrow (A_{4-7})$

Example: Set ST_4–ST_7 to "1".

```
MSTS: MOV A,#0F0H      ;SET ACC
      MOV STS,A        ;MOVE TO STS
```

MOV T,A Move Accumulator Contents to Timer/Counter

Opcode:

0 1 1 0	0 0 1 0

The contents of the accumulator are moved to the timer/event-counter register.
$(T) \leftarrow (A)$

Example: Initialize and start event counter.

```
INITEC: CLR A          ;CLEAR ACC TO ZEROS
        MOV T,A        ;MOVE ZEROS TO EVENT COUNTER
        STRT CNT       ;START COUNTER
```

MOVD A,Pp Move Port 4–7 Data to Accumulator

Opcode:

0 0 0 0	1 1 p_1 p_0

This is a 2-cycle instruction. Data on 8243 port 'p' is moved (read) to accumulator bits 0–3. Accumulator bits 4–7 are zeroed.
$(A_{0-3}) \leftarrow Pp$ p = 4–7
$(A_{4-7}) \leftarrow 0$

Note: Bits 0–1 of the opcode are used to represent PORTS 4–7. If you are coding in binary rather than assembly language, the mapping is as follows:

Bits		Port
p_1	p_0	
0	0	4
0	1	5
1	0	6
1	1	7

Example:

```
INPPT5: MOVD A,P5      ;MOVE PORT 5 DATA TO ACC
                       ;BITS 0-3, ZERO ACC BITS 4-7
```

MOVD Pp,A Move Accumulator Data to Port 4, 5, 6 and 7

Opcode:

0 0 1 1	1 1 p_1 p_0

This is a 2-cycle instruction. Data in accumulator bits 0–3 is moved (written) to 8243 port 'p'. Accumulator bits 4–7 are unaffected. (See NOTE above regarding port mapping.)

Example: Move data in accumulator to ports 4 and 5.

```
OUTP45: MOVD P4,A      ;MOVE ACC BITS 0-3 TO PORT 4
        SWAP A         ;EXCHANGE ACC BITS 0-3 AND 4-7
        MOVD P5,A      ;MOVE ACC BITS 0-3 TO PORT 5
```

MOVP A,@A Move Current Page Data to Accumulator

Opcode: | 1 0 1 0 | 0 0 1 1 |

This is a 2-cycle instruction. The contents of the program memory location addressed by the accumulator are moved to the accumulator. Only bits 0–7 of the program counter are affected, limiting the program memory reference to the current page. The program counter is restored following this operation.
(A) ← ((A))

Note: This a 1-byte, 2-cycle instruction. If it appears in location 255 of a program memory page, @A addresses a location in the following page.

Example:
```
MOV128: MOV A,#128      ;MOVE '128' DEC TO ACC
        MOVP A,@A       ;CONTENTS OF 129TH LOCATION
                        ;IN CURRENT PAGE ARE MOVED TO
                        ;ACC
```

MOVP3 A,@A Move Page 3 Data to Accumulator

Opcode: | 1 1 1 0 | 0 0 1 1 |

This is a 2-cycle instruction. The contents of the program memory location within page 3, addressed by the accumulator, are moved to the accumulator. The program counter is restored following this operation.
(A) ← ((A)) within page 3

Example: Look up ASCII equivalent of hexadecimal code in table contained at the beginning of page 3. Note that ASCII characters are designated by a 7-bit code; the eighth bit is always reset.
```
TABSCH: MOV A,#OB8H     ;MOVE 'B8' HEX TO ACC (10111000)
        ANL A,#7FH      ;LOGICAL AND ACC TO MASK BIT
                        ;7 (00111000)
MOVP3, A,@A             ;MOVE CONTENTS OF LOCATION
                        ;'38' HEX IN PAGE 3 TO ACC
                        ;(ASCII '8')
```
Access contents of location in page 3 labelled TAB1. Assume current program location is not in page 3.
```
TABSCH: MOV A,#TAB1     ;ISOLATE BITS 0–7
                        ;OF LABEL
                        ;ADDRESS VALUE
        MOVP3 A,@A      ;MOVE CONTENT OF PAGE 3
                        ;LOCATION LABELED 'TAB1'
                        ;TO ACC
```

NOP The NOP Instruction

Opcode: | 0 0 0 0 | 0 0 0 0 |

No operation is performed. Execution continues with the following instruction.

ORL A,Rr Logical OR Accumulator With Register Mask

Opcode: | 0 1 0 0 | 1 r_2 r_1 r_0 |

Data in the accumulator is logically ORed with the mask contained in working register 'r'.
(A) ← (A) OR (Rr) r = 0–7

Example:
```
ORREG: ORL A,R4         ;'OR' ACC CONTENTS WITH
                        ;MASK IN REG 4
```

ORL A,@Rr Logical OR Accumulator With Memory Mask

Opcode:

0 1 0 0	0 0 0 r

Data in the accumulator is logically ORed with the mask contained in the data memory location referenced by register 'r', bits 0–7.

(A) ← (A) OR ((Rr)) r = 0–1

Example:

```
ORDM: MOVE R0,#3FH      ;MOVE '3F' HEX TO REG 0
      ORL A, @R0        ;'OR' ACC CONTENTS WITH MASK
                        ;IN LOCATION 63
```

ORL A,#Data Logical OR Accumulator With Immediate Mask

Opcode:

0 1 0 0	0 0 1 1	•	d_7 d_6 d_5 d_4	d_3 d_2 d_1 d_0

This is a 2-cycle instruction. Data in the accumulator is logically ORed with an immediately-specified mask.

(A) ← (A) OR data

Example:

```
ORID: ORL A,#'X'        ;'OR' ACC CONTENTS WITH MASK
                        ;01011000 (ASCII VALUE OF 'X')
```

ORL Pp,#data Logical OR Port 1–2 With Immediate Mask

Opcode:

1 0 0 0	1 0 p_1 p_0	•	d_7 d_6 d_5 d_4	d_3 d_2 d_1 d_0

This is a 2-cycle instruction. Data on port 'p' is logically ORed with an immediately-specified mask.

(Pp) ← (Pp) OR data p = 1–2 (see OUTL instruction)

Example:

```
ORP1: ORL P1,#OFH       ;'OR' PORT 1 CONTENTS WITH
                        ;MASK 'FF' HEX (SET PORT 1
                        'TO ALL ONES)
```

ORLD Pp,A Logical OR Port 4–7 With Accumulator Mask

Opcode:

1 0 0 0	1 1 p_1 p_0

This is a 2-cycle instruction. Data on 8243 port 'p' is logically ORed with the digit mask contained in accumulator bits 0–3,

(Pp) (Pp) OR (A_{0-3}) p = 4–7 (See MOVD instruction)

Example:

```
ORP7; ORLD P7,A         ;'OR' PORT 7 CONTENTS
                        ;WITH ACC BITS 0–3
```

OUT DBB,A Output Accumulator Contents to Data Bus Buffer

Opcode:

0 0 0 0	0 0 1 0

Contents of the accumulator are transferred to the Data Bus Buffer Output register and the Output Buffer Full (OBF) flag is set to one.

(DBB) ← (A)

OBF ← 1

Example:

```
OUTDBB: OUT DBB,A       ;OUTPUT THE CONTENTS OF
                        ;THE ACC TO DBBOUT
```

OUTL Pp,A Output Accumulator Data to Port 1 and 2

Opcode:

0 0 1 1	1 0 p_1 p_0

This is a 2-cycle instruction. Data residing in the accumulator is transferred (written) to port 'p' and latched.
(Pp) ← (A) P = 1–2

Note: Bits 0–1 of the opcode are used to represent PORT 1 and PORT 2. If you are coding in binary rather than assembly language, the mapping is as follows:

Bits		Port
P_1	P_0	
0	0	X
0	1	1
1	0	2
1	1	X

Example:
```
OUTLP; MOV A,R7      ;MOVE REG 7 CONTENTS TO ACC
       OUTL P2,A     ;OUTPUT ACC CONTENTS TO PORT2
       MOV A,R6      ;MOVE REG 6 CONTENTS TO ACC
       OUTL P1,A     ;OUTPUT ACC CONTENTS TO PORT 1
```

RET Return Without PSW Restore

Opcode:

1 0 0 0	0 0 1 1

This is a 2-cycle instruction. The stack pointer (PSW bits 0–2 is decremented. The program counter is then restored from the stack. PSW bits 4–7 are not restored.
(SP) ← (SP) − 1
(PC) ← ((SP))

RETR Return With PSW Restore

Opcode:

1 0 0 1	0 0 1 1

This is a 2-cycle instruction. The stack pointer is decremented. The program counter and bits 4–7 of the PSW are then restored from the stack. Note that RETR should be used to return from an interrupt, but should not be used within the interrupt service routine as it signals the end of an interrupt routine.
(SP) ← (SP) − 1
(PC) ← ((SP))
(PSW_{4-7}) ← ((SP))

RL A Rotate Left Without Carry

Opcode:

1 1 1 0	0 1 1 1

The contents of the accumulator are rotated left one bit. Bit 7 is rotated into the bit 0 position.
(A_{n+1}) ← (A_n) n = 0–6
(A_0) ← (A_7)

Example: Assume accumulator contains 10110001.
```
RLNC: RL A           ;NEW ACC CONTENTS ARE 01100011
```

RLC A Rotate Left Through Carry

Opcode:

1 1 1 1	0 1 1 1

The contents of the accumulator are rotated left one bit. Bit 7 replaces the carry bit; the carry bit is rotated into the bit 0 position.

$(A_{n+1}) \leftarrow (A_n)$ n = 0–6
$(A_0) \leftarrow (C)$
$(C) \leftarrow (A7)$

Example: Assume accumulator contains a 'signed' number; isolate sign without changing value.

```
RLTC: CLR C          ;CLEAR CARRY TO ZERO
      RLC A          ;ROTATE ACC LEFT, SIGN
                     ;BIT (7) IS PLACED IN CARRY
      RR A           ;ROTATE ACC RIGHT—VALUE
                     ;(BITS 0–6) IS RESTORED,
                     ;CARRY UNCHANGED, BIT 7
                     ;IS ZERO
```

RR A Rotate Right Without Carry

Opcode:

0 1 1 1	0 1 1 1

The contents of the accumulator are rotated right one bit. Bit 0 is rotated into the bit 7 position.

$(A) \leftarrow (A_n + 1)$ n = 0–6
$(A_7) \leftarrow (A_0)$

Example Assume accumulator contains 10110001.

```
RRNC: RRA            ;NEW ACC CONTENTS ARE 11011000
```

RRC A Rotate Right Through Carry

Opcode:

0 1 1 0	0 1 1 1

The contents of the accumulator are rotated one bit. Bit 0 replaces the carry bit; the carry bit is rotated into the bit 7 position.

$(A_n) \leftarrow (A_n + 1)$ n = 0–6
$(A_7) \leftarrow (C)$
$(C) \leftarrow (A_0)$

Example Assume carry is not set and accumulator contains 10110001.

```
RRTC: RRCA           ;CARRY IS SET AND ACC
                     ;CONTAINS 01011000
```

SEL RB0 Select Register Bank 0

Opcode:

1 1 0 0	0 1 0 1

PSW BIT 4 is set to zero. References to working registers 0–7 address data memory locations 0–7. This is the recommended setting for normal program execution.
(BS) ← 0

SEL RB1 Select Register Bank 1

Opcode:

1 1 0 1	0 1 0 1

PSW bit 4 is set to one. References to working registers 0–7 address data memory locations 24–31. This is the recommended setting for interrupt service routines, since locations 0–7 are left intact. The setting of PSW bit 4 in effect at the time of an interrupt is restored by the RETR instruction when the interrupt service routine is completed.

Example: Assume an IBF interrupt has occurred, control has passed to program memory location 3, and PSW bit 4 was zero before the interrupt.

```
LOC3: JMP INIT              ;JUMP TO ROUTINE 'INIT'
                .
                .
                .
INIT: MOV R7,A              ;MOV ACC CONTENTS TO
                            ;LOCATION 7
      SEL RB1               ;SELECT REG BANK 1
      MOV R7,#OFAH          ;MOVE 'FA' HEX TO LOCATION 31
                .
                .
                .
      SEL RB0               ;SELECT REG BANK 0
      MOV A,R7              ;RESTORE ACC FROM LOCATION 7
      RETR                  ;RETURN——RESTORE PC AND PSW
```

STOP TCNT Stop Timer/Event Counter

Opcode:

0 1 1 0	0 1 0 1

This instruction is used to stop both time accumulation and event counting.

Example: Disable interrupt, but jump to interrupt routine after eight overflows and stop timer. Count overflows in register 7.

```
START: DIS TCNTI          ;DISABLE TIMER INTERRUPT
       CLR A              ;CLEAR ACC TO ZERO
       MOV T,A            ;MOV ZERO TO TIMER
       MOV R7,A           ;MOVE ZERO TO REG 7
       STRT T             ;START TIMER
MAIN:  JTF COUNT          ;JUMP TO ROUTINE 'COUNT'
                          ;IF TF = 1 AND CLEAR TIMER FLAG
       JMP MAIN           ;CLOSE LOOP
COUNT: INC R7             ;INCREMENT REG 7
       MOV A,R7           ;MOVE REG 7 CONTENTS TO ACC
       JB3 INT            ;JUMP TO ROUTINE 'INT' IF ACC
                          ;BIT 3 IS SET (REG 7 = 8)
       JMP MAIN           ;OTHERWISE RETURN TO ROUTINE
                          ;MAIN
         .
         .
         .
INT: STOP TCNT            ;STOP TIMER
       JMP 7H             ;JUMP TO LOCATION 7 (TIMER
                          ;INTERRUPT ROUTINE)
```

STRT CNT Start Event Counter

Opcode:

0 1 0 0	0 1 0 1

The TEST 1 (T_1) pin is enabled as the event-counter input and the counter is started. The event-counter register is incremented with each high to low transition on the T_1 pin.

Example: Initialize and start event counter. Assume overflow is desired with first T_1 input.

```
STARTC: EN TCNTI           ;ENABLE COUNTER INTERRUPT
        MOV A,#OFFH        ;MOVE 'FF' HEX (ONES) TO
                           ;ACC
        MOV T,A            ;MOVE ONES TO COUNTER
        STRT CNT           ;INPUT AND START
```

STRT T Start Timer

Opcode:

0 1 0 1	0 1 0 1

Timer accumulation is initiated in the timer register. The register is incremented every 32 instruction cycles. The prescaler which counts the 32 cycles is cleared but the timer register is not.

Example: Initialize and start timer.

```
STARTT: EN TCNTI           ;ENABLE TIMER INTERRUPT
        CLR A              :CLEAR ACC TO ZEROS
        MOV T,A            ;MOVE ZEROS TO TIMER
        STRT T             ;START TIMER
```

SWAP A Swap Nibbles Within Accumulator

Opcode:

0 1 0 0	0 1 1 1

Bits 0–3 of the accumulator are swapped with bits 4-7 of the accumulator.
$(A_{4-7}) \longleftrightarrow (A_{0-3})$

Example: Pack bits 0–3 of locations 50-51 into location 50.

```
PCKDIG: MOV R0,#50          ;MOVE '50' DEC TO REG 0
        MOV R1,#51          ;MOVE '51' DEC TO REG 1
        XCHD A,@R0          ;EXCHANGE BIT 0-3 OF ACC
                            ;AND LOCATION 50
        SWAP A              ;SWAP BITS 0-3 AND 4-7 OF ACC
        XCHD A,@ R1         ;EXCHANGE BITS 0-3 OF ACC AND
                            ;LOCATION 51
        MOV @R0,A           ;MOVE CONTENTS OF ACC TO
                            ;LOCATION 51
```

XCH ARr Exchange Accumulator-Register Contents

Opcode:

0 0 1 0	1 r_2 r_1 r_0

The contents of the accumulator and the contents of working register 'r' are exchanged.
(A) $\longleftrightarrow$ (Rr) r = 0–7

Example: Move PSW contents to Reg 7 without losing accumulator contents.

```
XCHAR7: XCH A,R7             ;EXCHANGE CONTENTS OF REG 7
                             ;AND ACC
        MOV A,PSW            ;MOVE PSW CONTENTS TO ACC
        XCH, A,R7            ;EXCHANGE CONTENTS OF REG 7
                             ;AND ACC AGAIN
```

XCH A,@Rr Exchange Accumulator and Data Memory Contents

Opcode:

0 0 1 0	0 0 0 r

The contents of the accumulator and the contents of the data memory location addressed by bits 0–7 of register 'r' are exchanged. Register 'r' contents are unaffected.
(A) $\longleftrightarrow$ ((Rr)) r = 0–1

Example: Decrement contents of location 52.

```
DEC 52: MOV R0,#52           ;MOVE '52' DEC TO ADDRESS
                             ;REG 0
        XCH A,@R0            ;EXCHANGE CONTENTS OF ACC
                             ;AND LOCATION 52
        DEC A                ;DECREMENT ACC CONTENTS
        XCH A,@R0            ;EXCHANGE CONTENTS OF ACC
                             ;AND LOCATION 52 AGAIN
```

XCHD A,@Rr Exchange Accumulator and Data Memory 4-bit Data

Opcode: | 0 0 1 1 | 0 0 0 r |

This instruction exchanges bits 0–3 of the accumulator with bits 0–3 of the data memory location addressed by bits 0–7 of register 'r'. Bits 4–7 of the accumulator, bits 4–7 of the data memory location, and the contents of register 'r' are unaffected.

$(A_{0-3}) \longleftrightarrow ((Rr_{0-3}))$ r = 0–1

Example: Assume program counter contents have been stacked in locations 22-23.

```
XCHNIB: MOV R0,#23      ;MOVE '23' DEC TO REG 0
        CLR A           ;CLEAR ACC TO ZEROS
        XCHD A,@R0      ;EXCHANGE BITS 0-3 OF ACC
                        ;AND LOCATION 23 (BITS 8-11
                        ;OF PC ARE ZEROED, ADDRESS
                        ;REFERS TO PAGE 0)
```

XRL A,Rr Logical XOR Accumulator With Register Mask

Opcode: | 1 1 0 1 | 1 r_2 r_1 r_0 |

Data in the accumulator is EXCLUSIVE ORed with the mask contained in working register 'r'.

(A) $\longleftrightarrow$ (A) XOR (Rr) r = 0–7

Example:

```
XORREG: XRL A,R5         ;'XOR' ACC CONTENTS WITH
                         ;MASK IN REG 5
```

XRL A,@Rr Logical XOR Accumulator With Memory Mask

Opcode: | 1 1 0 1 | 0 0 0 r |

Data in the accumulator is EXCLUSIVE ORed with the mask contained in the data memory location address by register 'r', bits 0–7.

(A) $\longleftarrow$ (A) XOR ((Rr)) r = 0–1

Example:

```
XORDM: MOV R1,#20H       ;MOVE '20' HEX TO REG 1
       XRL A,@R1         ;'XOR' ACC CONTENTS WITH MASK
                         ;IN LOCATION 32
```

XRL A,#data, Logical XOR Accumulator With Immediate Mask

Opcode: | 1 1 0 1 | 0 0 1 1 | • | d_7 d_6 d_5 d_4 | d_3 d_2 d_1 d_0 |

This is a 2-cycle instruction. Data in the accumulator is EXCLUSIVE ORed with an immediately-specified mask.

(A) $\longleftarrow$ (A) XOR data

Example:

```
XORID: XRL A,#HEXTEN     ;XOR CONTENTS OF ACC WITH
                         ;MASK EQUAL VALUE OF SYMBOL
                         ;'HEXTEN'
```

CHAPTER 4
SINGLE-STEP AND PROGRAMMING POWER-DOWN MODES

SINGLE-STEP

The UPI family has a single-step mode which allows the user to manually step through his program one instruction at a time. While stopped, the address of the next instruction to be fetched is available on PORT 1 and the lower 2 bits of PORT 2. The single-step feature simplifies program debugging by allowing the user to easily follow program execution.

Figure 4-1 illustrates a recommended circuit for single-step operation, while Figure 4-2 shows the timing relationship between the SYNC output and the $\overline{SS}$ input. During single-step operation, PORT 1 and part of PORT 2 are used to output address information. In order to retain the normal I/O functions of PORTS 1 and 2, a separate latch can be used as shown in Figure 4-3.

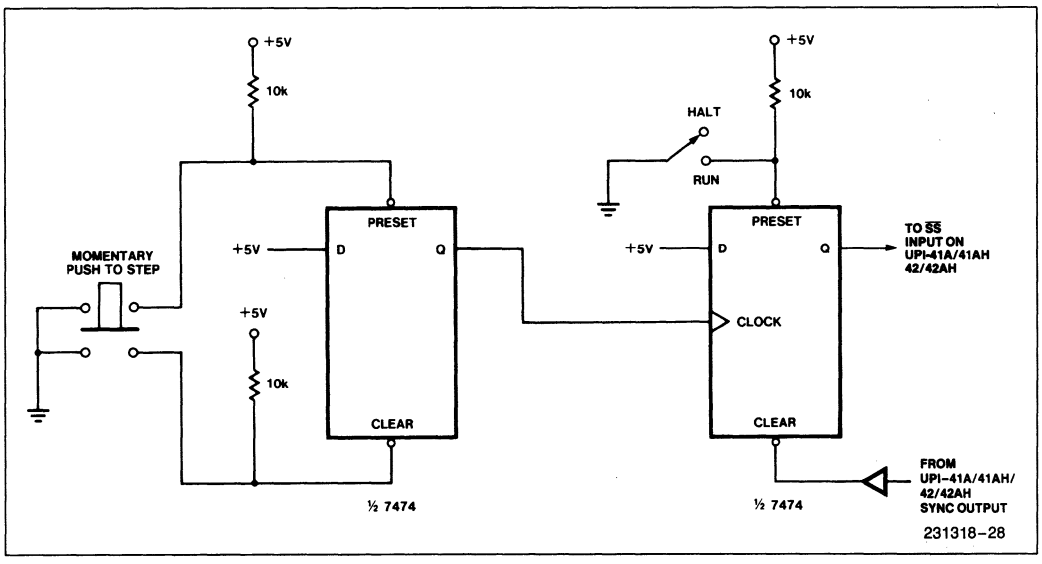


Figure 4-1. Single-Step Circuit

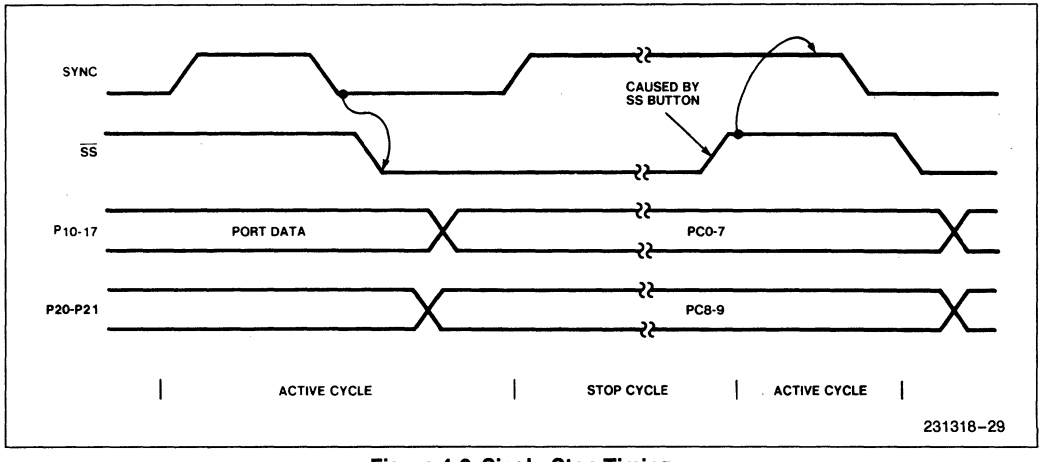


Figure 4-2. Single-Step Timing

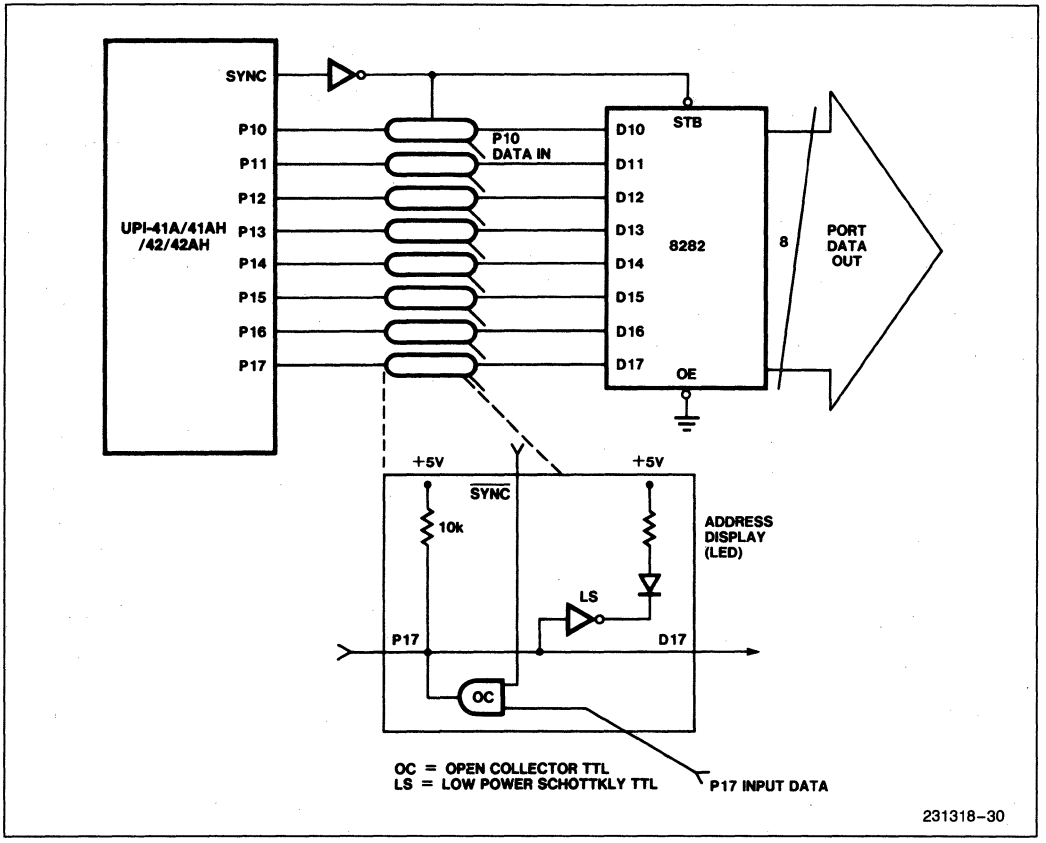


Figure 4-3. Latching Port Data

Timing

The sequence of single-step operation is as follows:

1) The processor is requested to stop by applying a low level on $\overline{SS}$. The $\overline{SS}$ input should not be brought low while SYNC is high. (The UPI samples the $\overline{SS}$ pin in the middle of the SYNC pulse).
2) The processor responds to the request by stopping during the instruction fetch portion of the next instruction. If a double cycle instruction is in progress when the single-step command is received, both cycles will be completed before stopping.
3) The processor acknowledges it has entered the stopped state by raising SYNC high. In this state, which can be maintained indefinitely, the 10-bit address of the next instruction to be fetched is preset on PORT 1 and the lower 2 bits of PORT 2.
4) $\overline{SS}$ is then raised high to bring the processor out of the stopped mode allowing it to fetch the next instruction.The exit from stop is indicated by the processor bringing SYNC low.
5) To stop the processor at the next instruction $\overline{SS}$ must be brought low again before the next SYNC pulse—the circuit in Figure 4-1 uses the trailing edge of the previous pulse. If $\overline{SS}$ is left high, the processor remains in the "RUN" mode.

Figure 4-1 shows a schematic for implementing single-step. A single D-type flip-flop with preset and clear is used to generate $\overline{SS}$. In the RUN mode $\overline{SS}$ is held high by keeping the flip-flop preset (preset has precedence over the clear input). To enter single-step, preset is removed allowing SYNC to bring $\overline{SS}$ low via the clear input. Note that SYNC must be buffered since the SN7474 is equivalent to 3 TTL loads.

The processor is now in the stopped state. The next instruction is initiated by stoppe state. The next instruction is initiated by clocking "1" the flip-flop. This "1" will not appear on $\overline{SS}$ unless SYNC is high (I.e., clear must be removed from the flip-flop). In response to $\overline{SS}$ going high, the processor begins an instruction fetch which brings SYNC low. $\overline{SS}$ is then reset through the clear input and the processor again enters the stopped state.

EXTERNAL ACCESS

The UPI family has an External Access mode (EA) which puts the processor into a test mode. This mode allows the user to disable the internal program memory and execute from external memory. External Access mode is useful in testing because it allows the user to test the processor's functions directly. It is only useful for testing since this mode uses D_0–D_7, PORTS 10–17 and PORTS 20–22.

This mode is invoked by connecting the EA pin to 5V. The 11-bit current program counter contents then come out on PORTS 10–17 and PORTS 20–22 after the SYNC output goes high. (PORT 10 is the least significant bit.) The desired instruction opcode is placed on D_0–D_7 before the start of state S_1. During state S_1, the opcode is sampled from D_0–D_7 and subsequently executed in place of the internal program memory contents.

The program counter contents are multiplexed with the I/O port data on PORTS 10–17 and PORTS 20–22. The I/O port data may be demultiplexed using an external latch on the rising edge of SYNC. The program counter contents may be demultiplexed similarly using the trailing edge of SYNC.

Reading and/or writing the Data Bus Buffer registers is still allowed although only when D_0–D_7 are not being sampled for opcode data. In practice, since this sampling time is not known externally, reads or writes on the system bus are done during SYNC high time. Approximately 600 ns are available for each read or write cycle.

POWER DOWN MODE (UPI-41AH/42AH ONLY)

Extra circuitry is included in the UPI-41AH/42AH version to allow low-power, standby operation. Power is removed from all system elements except the internal data RAM in the low-power mode. Thus the contents of RAM can be maintained and the device draws only 10 to 15% of its normal power.

The V_{CC} pin serves as the 5V power supply pin for all of the UPI-41AH/42AH version's circuitry except the data RAM array. The V_{DD} pin supplies only the RAM array. In normal operation, both V_{CC} and V_{DD} are connected to the same 5V power supply.

To enter the Power-Down mode, the $\overline{\text{RESET}}$ signal to the UPI is asserted. This ensures the memory will not be inadvertently altered by the UPI during power-down. The V_{CC} pin is then grounded while V_{DD} is maintained at 5V. Figure 4-4 illustrates a recommended Power-Down sequence. The sequence typically occurs as follows:

1) Imminent power supply failure is detected by user defined circuitry. The signal must occur early enough to guarantee the UPI-41AH/42AH can save all necessary data before V_{CC} falls outside normal operating tolerance.
2) A "Power Failure" signal is used to interrupt the processor (via a timer overflow interrupt, for instance) and call a Power Failure service routine.
3) The Power Failure routine saves all important data and machine status in the RAM array. The routine may also initiate transfer of a backup supply to the V_{DD} pin and indicate to external circuitry that the Power Failure routine is complete.
4) A $\overline{\text{RESET}}$ signal is applied by external hardware to guarantee data will not be altered as the power supply falls out of limits. $\overline{\text{RESET}}$ must be low until V_{CC} reaches ground potential.

Recovery from the Power-Down mode can occur as any other power-on sequence. An external 1 μfd capacitor on the $\overline{\text{RESET}}$ input will provide the necessary initialization pulse.

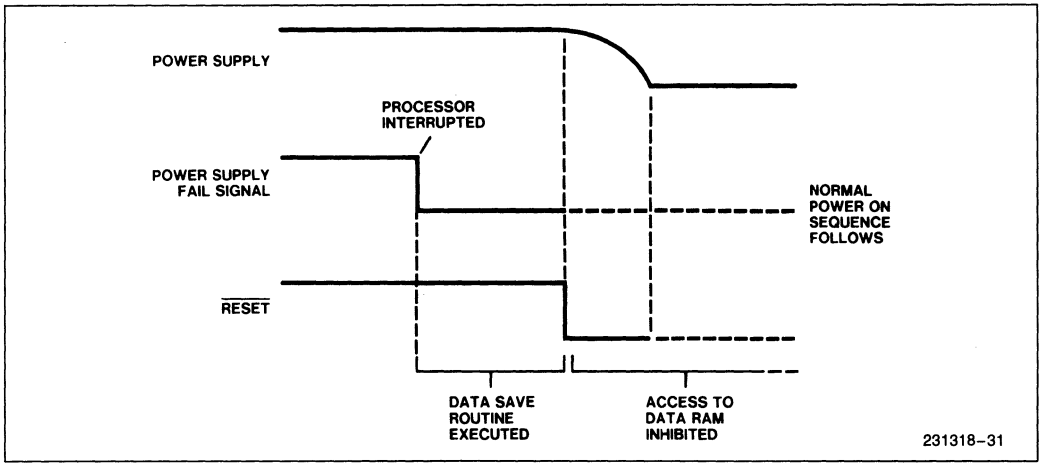


Figure 4-4. Power-Down Sequence

CHAPTER 5
SYSTEM OPERATION

BUS INTERFACE

The UPI-41A/41AH/42/42AH Microcomputer functions as a peripheral to a master processor by using the data bus buffer registers to handle data transfers. The DBB configuration is illustrated in Figure 5-1. The UPI Microcomputer's 8 three-state data lines (D_7–D_0) connect directly to the master processor's data bus. Data transfer to the master is controlled by 4 external inputs to the UPI:

- A_0 Address Input signifying command or data
- $\overline{CS}$ Chip Select
- $\overline{RD}$ Read strobe
- $\overline{WR}$ Write strobe

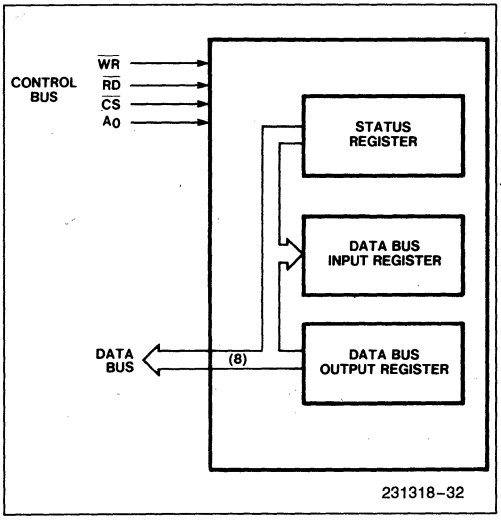


Figure 5-1. Data Bus Register Configuration

The master processor addresses the UPI-41A/41AH/42/42AH Microcomputer as a standard peripheral device. Table 5-1 shows the conditions for data transfer:

Table 5-1. Data Transfer Controls

$\overline{CS}$	A_0	$\overline{RD}$	$\overline{WR}$	Condition
0	0	0	1	Read DBBOUT
0	1	0	1	Read STATUS
0	0	1	0	Write DBBIN data, set $F_1 = 0$
0	1	1	0	Write DBBIN command set $F_1 = 1$
1	x	x	x	Disable DBB

Reading the DBBOUT Register

The sequence for reading the DBBOUT register is shown in Figure 5-2. This operation causes the 8-bit contents of the DBBOUT register to be placed on the system Data Bus. The OBF flag is cleared automatically.

Reading STATUS

The sequence for reading the UPI Microcomputer's 8 STATUS bits is shown in Figure 5-3. This operation causes the 8-bit STATUS register contents to be placed on the system Data Bus as shown.

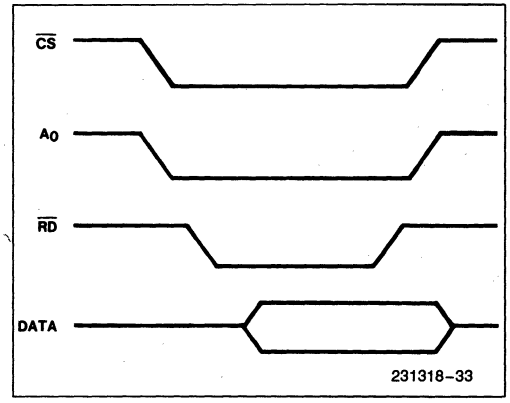


Figure 5-2. DBBOUT Read

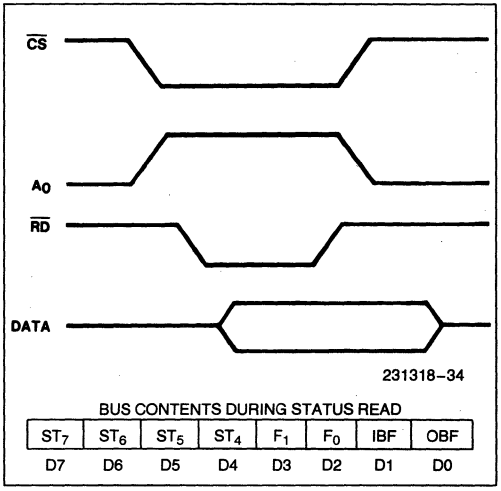


Figure 5-3. Status Read

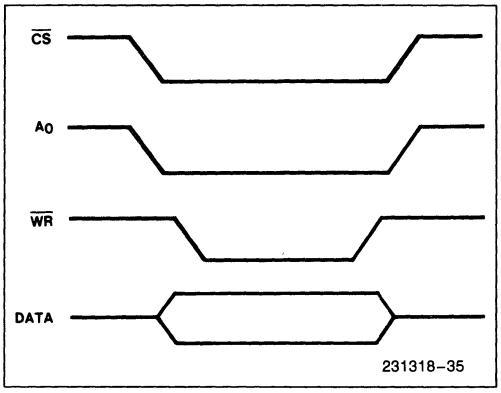


Figure 5-4. Writing Data to DBBIN

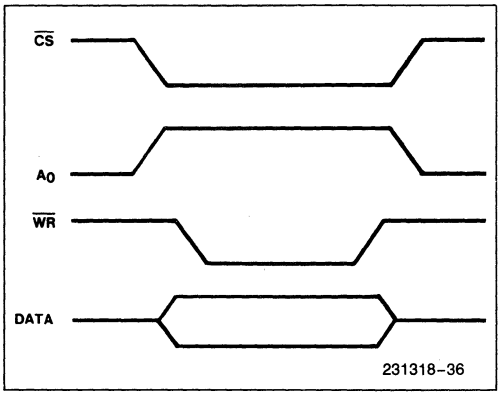


Figure 5-5. Writing Commands to DBBIN

Write Data to DBBIN

The sequence for writing data to the DBBIN register is shown in Figure 5-4. This operation causes the system Data Bus contents to be transferred to the DBBIN register and the IBF flag is set. Also, the F_1 flag is cleared ($F_1 = 0$) and an interrupt request is generated. When the IBF interrupt is enabled, a jump to location 3 will occur. The interrupt request is cleared upon entering the IBF service routine or by a system RESET input.

Writing Commands to DBBIN

The sequence for writing commands to the DBBIN register is shown in Figure 5-5. This sequence is identical to a data write except that the A_0 input is latched in the F_1 flag ($F_1 = 1$). The IBF flag is set and an interrupt request is generated when the master writes a command to DBB.

Operations of Data Bus Registers

The UPI-41A/41AH/42/42AH Microcomputer controls the transfer of DBB data to its accumulator by executing INput and OUTput instructions. An IN A,DBB instruction causes the contents to be transferred to the UPI accumulator and the IBF flag is cleared.

The OUT DBB,A instruction causes the contents of the accumulator to be transferred to the DBBOUT register. The OBF flag is set.

The UPI's data bus buffer interface is applicable to a variety of microprocessors including the 8086, 8088, 8085AH, 8080, and 8048.

A description of the interface to each of these processors follows.

DESIGN EXAMPLES

8085AH Interface

Figure 5-6 illustrates an 8085AH system using a UPI-41A/41AH/42/42AH. The 8085AH system uses a multiplexed address and data bus. During I/O the 8 upper address lines (A_8–A_{15}) contain the same I/O address as the lower 8 address/data lines (A_0–A_7); therefore I/O address decoding is done using only the upper 8 lines to eliminate latching of the address. An 8205 decoder provides address decoding for both the UPI and the 8237. Data is transferred using the two DMA handshaking lines of PORT 2. The 8237 performs the actual bus transfer operation. Using the UPI-41A/41AH/42/42AH's OBF master interrupt, the UPI notifies the 8085AH upon transfer completion using the RST 5.5 interrupt input. The $\overline{IBF}$ master interrupt is not used in this example.

8088 Interface

Figure 5-7 illustrates a UPI-41A/41AH/42/42AH interface to an 8088 minimum mode system. Two 8-bit latches are used to demultiplex the address and data bus. The address bus is 20-lines wide. For I/O only, the lower 16 address lines are used, providing an addressing range of 64K. UPI address selection is accomplished using an 8205 decoder. The A_0 address line of the bus is connected to the corresponding UPI input for register selection. Since the UPI is polled by the 8088, neither DMA nor master interrupt capabilities of the UPI are used in the figure.

8086 Interface

The UPI-41A/41AH/42/42AH can be used on an 8086 maximum mode system as shown in Figure 5-8. The address and data bus is demultiplexed using three

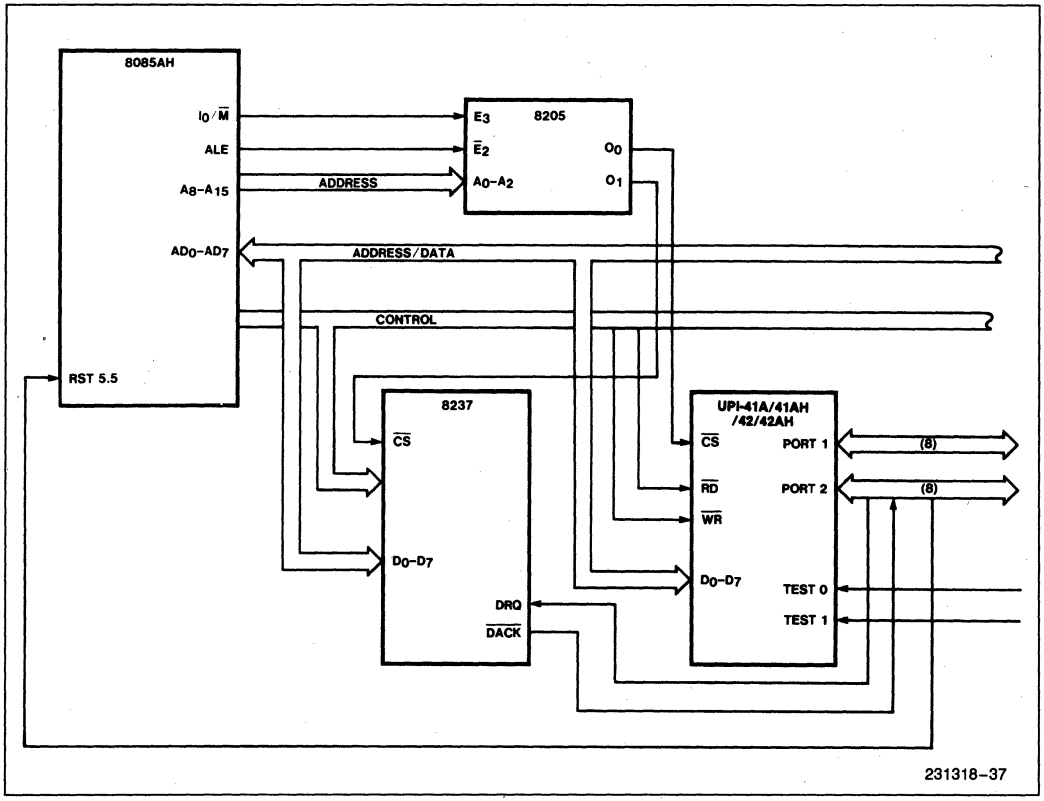


Figure 5-6. 8085AH-UPI System

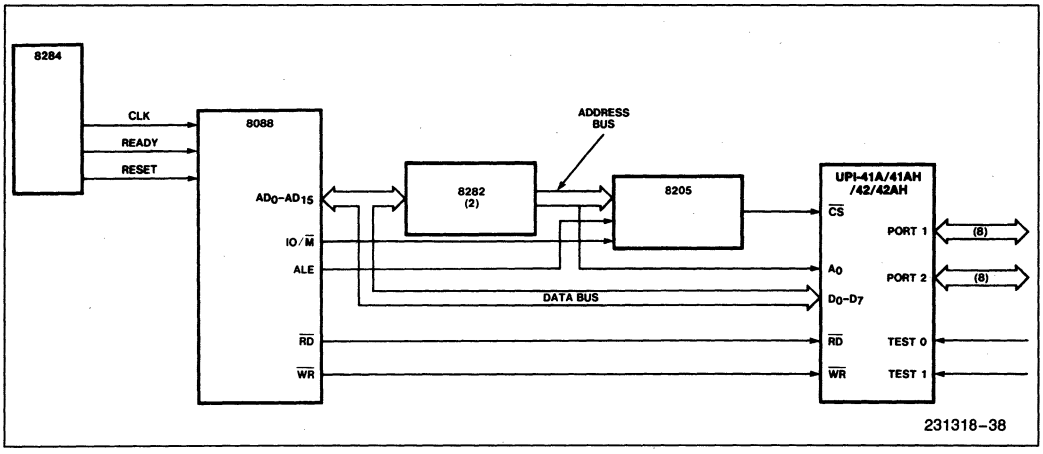


Figure 5-7. 8088-UPI Minimum Mode System

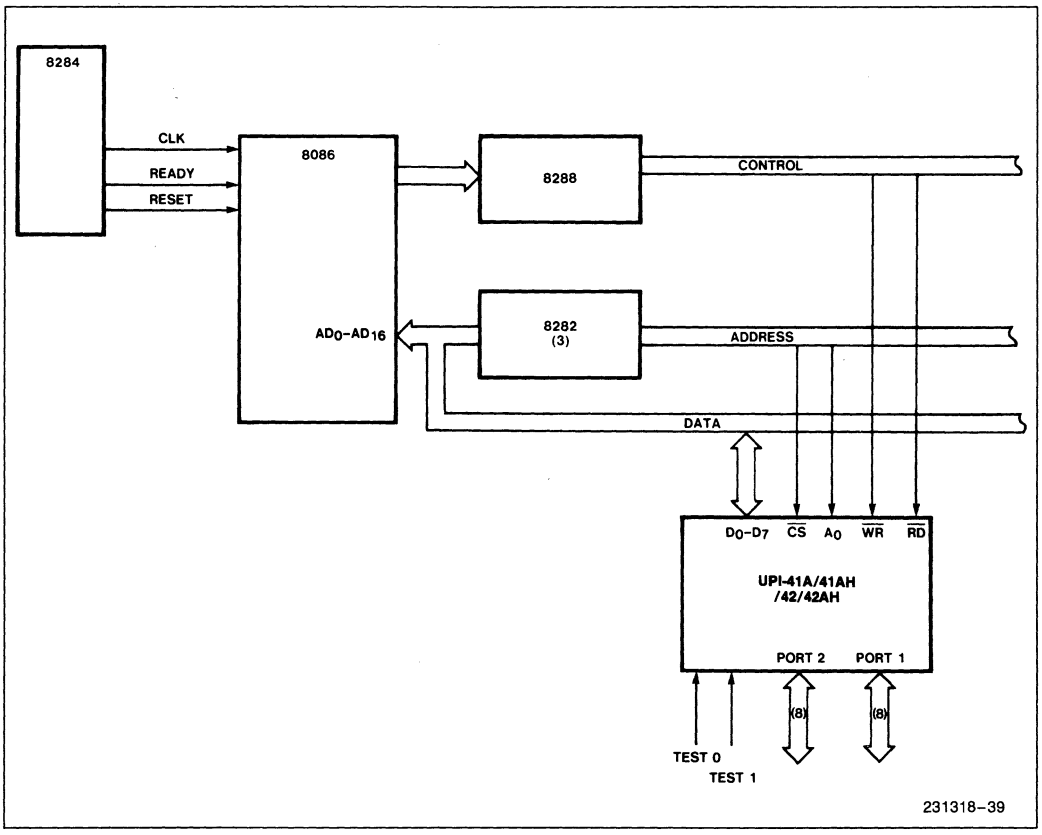


Figure 5-8. 8086-UPI Maximum Mode Systems

8282 latches providing separate address and data buses. The address bus is 20-lines wide and the data bus is 16-lines wide. Multiplexed control lines are decoded by the 8288. The UPI's $\overline{CS}$ input is provided by linear selection. Note that the UPI is both I/O mapped and memory mapped as a result of the linear addressing technique. An address decoder may be used to limit the UPI-41A/41AH/42/42AH to a specific I/O mapped address. Address line A_1 is connected to the UPI's A_0 input. This insures that the registers of the UPI will have even I/O addresses. Data will be transferred on D_0–D_7 lines only. This allows the I/O registers to be accessed using byte manipulation instructions.

8080 Interface

Figure 5-9 illustrates the interface to an 8080A system. In this example, a crystal and capacitor are used for UPI-41A/41AH/42/42AH timing reference and power-on RESET. If the 2-MHz 8080A 2-phase clock were used instead of the crystal, the UPI-41A/41AH/42/42AH would run at only 16% full speed.

The A_0 and $\overline{CS}$ inputs are direct connections to the 8080 address bus. In larger systems, however, either of these inputs may be decoded from the 16 address lines.

The $\overline{RD}$ and $\overline{WR}$ inputs to the UPI can be either the $\overline{IOR}$ and $\overline{IOW}$ or the $\overline{MEMR}$ and $\overline{MEMR}$ signals depending on the I/O mapping technique to be used.

The UPI can be addressed as an I/O device using INput and OUTput instructions in 8080 software.

8048 Interface

Figure 5-10 shows the UPI interface to an 8048 master processor.

The 8048 $\overline{RD}$ and $\overline{WR}$ outputs are directly compatible with the UPI. Figure 5-11 shows a distributed processing system with up to seven UPI's connected to a single 8048 master processor.

In this configuration the 8048 uses PORT 0 as a data bus. I/O PORT 2 is used to select one of the seven

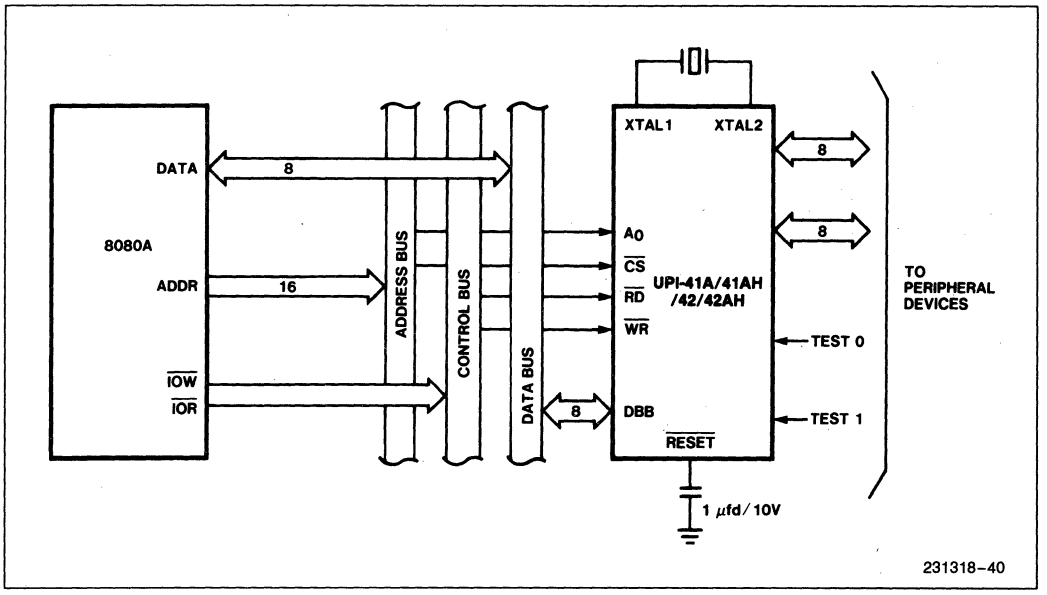


Figure 5-9. 8080A-UPI Interface

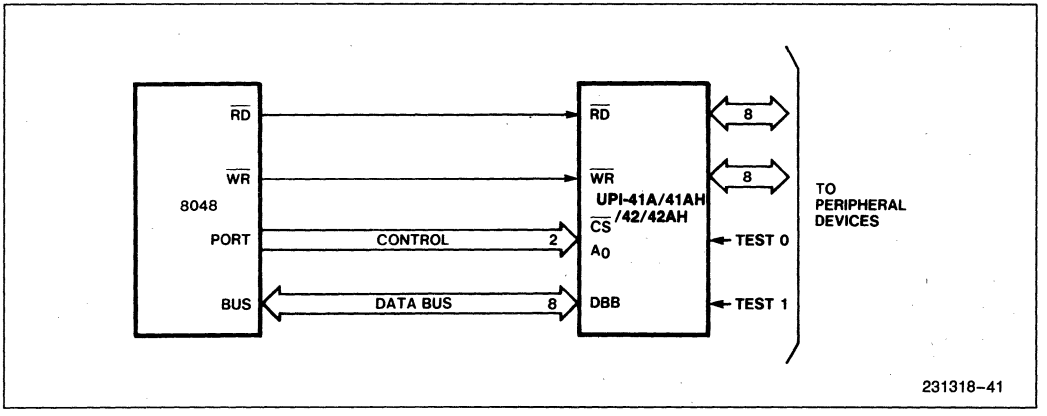


Figure 5-10. 8048-UPI Interface

UPI's when data transfer occurs. The UPI's are programmed to handle isolated tasks and, since they operate in parallel, system throughput is increased.

GENERAL HANDSHAKING PROTOCOL

1) Master reads STATUS register ($\overline{RD}$, $\overline{CS}$, A_0 = (0, 0, 1)) in polling or in response to either an $\overline{IBF}$ or an OBF interrupt.
2) If the UPI DBBIN register is empty (IBF flag = 0), Master writes a word to the DBBIN register ($\overline{WR}$, $\overline{CS}$, A_0 = (0, 0, 1) or (0, 0, 0)). If A_0 = 1, write command word, set F_1. If A_0 = 0, write data word, F_1 = 0.
3) If the UPI DBBOUT register is full (OBF flag = 1), Master reads a word from the DBBOUT register ($\overline{RD}$, $\overline{CS}$, A_0 = (0,0, 0)).
4) UPI recognizes IBF (via IBF interrupt or JNIBF). Input data or command word is processed, depending on F1; IBF is reset. Repeat step 1 above.
5) UPI recognizes OBF flag = 0 (via JOBF). Next word is output to DBBOUT register, OBF is set. Repeat step 1 above.

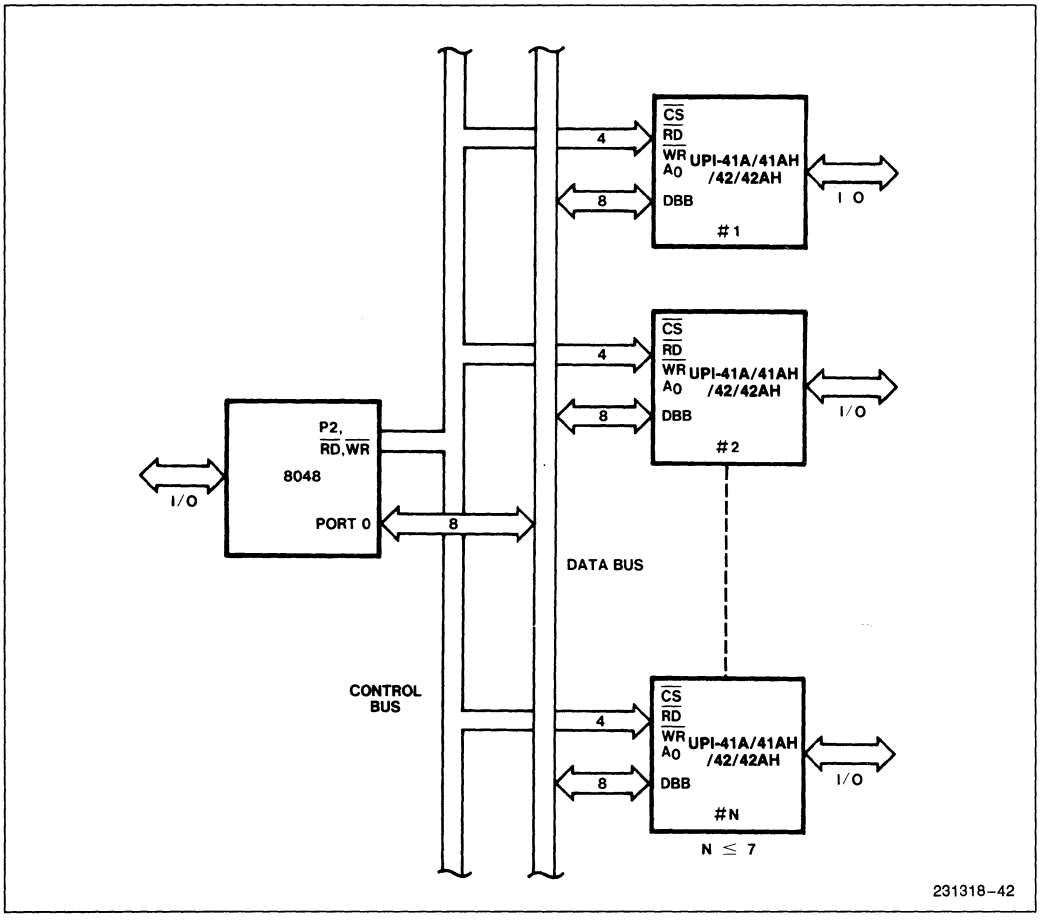


Figure 5-11. Distributed Processor System

CHAPTER 6
APPLICATIONS

ABSTRACTS

The UPI-41A/41AH/42/42AH is designed to fill a wide variety of low to medium speed peripheral interface applications where flexibility and easy implementation are important considerations. The following examples illustrate some typical applications.

Keyboard Encoder

Figure 6-1 illustrates a keyboard encoder configuration using the UPI and the 8243 I/O expander to scan a 128-key matrix. The encoder has switch matrix scanning logic, N-key rollover logic, ROM look-up table, FIFO character buffer, and additional outputs for display functions, control keys or other special functions.

PORT 1 and PORTs 4–7 provide the interface to the keyboard. PORT 1 lines are set one at a time to select the various key matrix rows.

When a row is energized all 16 columns (i.e., PORTs 4–7 inputs) are sampled to determine if any switch in the row is closed. The scanning software is code efficient because the UPI instruction set includes individual bit set/clear operations and expander PORTs 4–7 can be directly addressed with single, 2-byte instructions. Also, accumulator bits can be tested in a single operation. Scan time for 128 keys is about 10 ms. Each matrix point has a unique binary code which is used to address ROM when a key closure is detected. Page 3 of ROM contains a look-up table with useable codes (i.e., ASCII, EBCDIC, etc.) which correspond to each key. When a valid key closure is detected the ROM code corresponding to that key is stored in a FIFO buffer in data memory for transfer to the master processor. To avoid stray noise and switch bounce, a key closure must be detected on two consecutive scans before it is considered valid and loaded into the FIFO buffer. The FIFO buffer allows multiple keys to be processed as they are depressed without regard to when they are released, a condition known as N-key rollover.

The basic features of this encoder are fairly standard and require only about 500 bytes of memory. Since the UPI is programmable and has additional memory capacity it can handle a number of other functions. For example, special keys can be programmed to give an entry on closing as well as opening. Also, I/O lines are

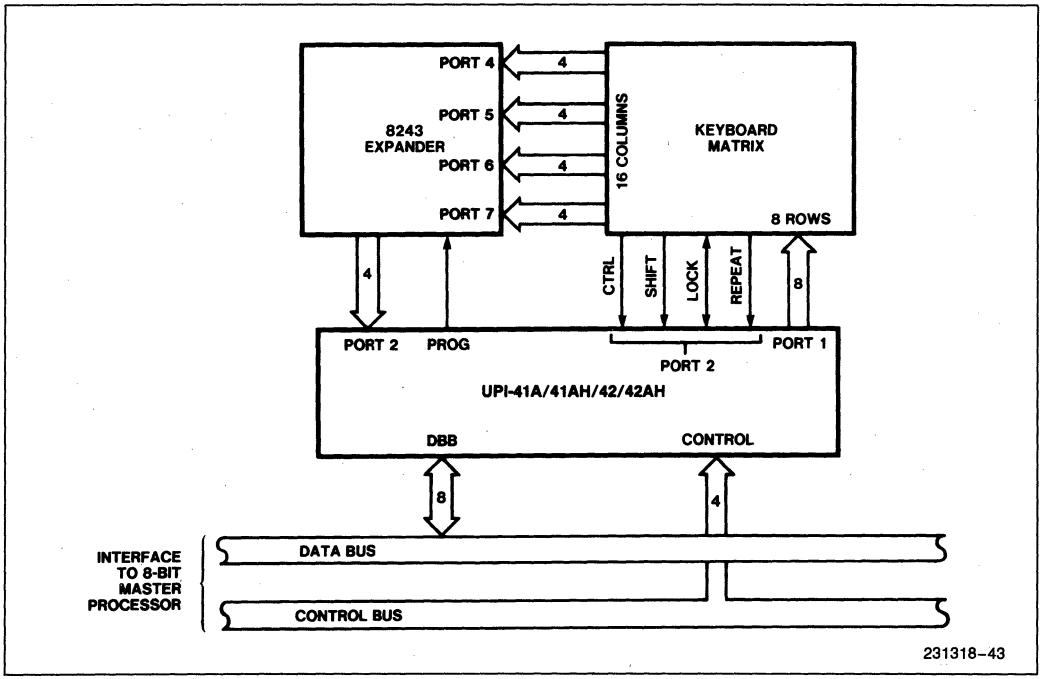


Figure 6-1. Keyboard Encoder Configuration

available to control a 16-digit, 7-segment display. The UPI can also be programmed to recognize special combinations of characters such as commands, then transfer only the decoded information to the master processor.

Matrix Printer Interface

The matrix printer interface illustrated in Figure 6-2 is a typical application for the UPI. The actual printer mechanism could be any of the numerous dot-matrix types and similar configurations can be shown for drum, spherical head, daisy wheel or chain type printers.

The bus structure shown represents a generalized, 8-bit system bus configuration. The UPI's three-state interface port and asynchronous data buffer registers allow it to connect directly to this type of system for efficient, two-way data transfer.

The UPI's two on-board I/O ports provide up to 16 input and output signals to control the printer mechanism. The timer/event counter is used for generating a timing sequence to control print head position, line feed, carriage return, and other sequences. The on-board program memory provides character generation for 5 x 7, 7 x 9, or other dot matrix formats. As an added feature a portion of the data memory can be used as a FIFO buffer so that the master processor can send a block of data at a high rate. The UPI can then output characters from the buffer at a rate the printer can accept while the master processor returns to other tasks.

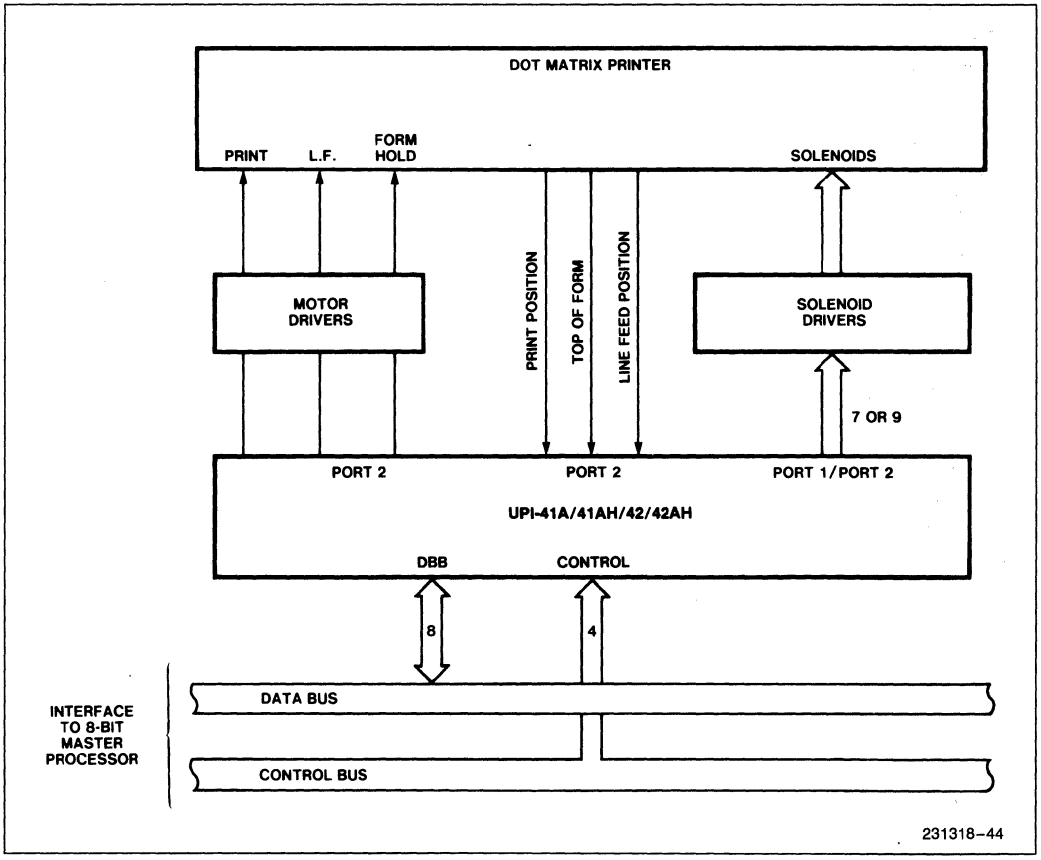


Figure 6-2. Matrix Printer Controller

The 8295 Printer Controller is an example of an UPI preprogrammed as a dot matrix printer interface.

Tape Cassette Controller

Figure 6-3 illustrates a digital cassette interface which can be implemented with the UPI. Two sections of the tape transport are controlled by the UPI: digital data/command logic, and motor servo control.

The motor servo requires a speed reference in the form of a monostable pulse whose width is proportional to the desired speed. The UPI monitors a prerecorded clock from the tape and uses its on-board interval timer to generate the required speed reference pulses at each clock transition.

Recorded data from the tape is supplied serially by the data/command logic and is converted to 8-bit words by the UPI, then transferred to the master processor. At 10 ips tape speed the UPI can easily handle the 8000 bps data rate. To record data, the UPI uses the two input lines to the data/command logic which control the flux direction in the recording head. The UPI also monitors 4 status lines from the tape transport including: end of tape, cassette inserted, busy, and write permit. All control signals can be handled by the UPI's two I/O ports.

Universal I/O Interface

Figure 6-4 shows an I/O interface design based on the UPI. This configuration includes 12 parallel I/O lines and a serial (RS232C) interface for full duplex data transfer up to 1200 baud. This type of design can be used to interface a master processor to a broad spectrum of peripheral devices as well as to a serial communication channel.

PORT 1 is used strictly for I/O in this example while PORT 2 lines provide five functions:

- P_{23}–P_{20} I/O lines (bidirectional)
- P_{24} Request to send (RTS)
- P_{25} Clear to send (CTS)
- P_{26} Interrupt to master
- P_{27} Serial data out

The parallel I/O lines make use of the bidirectional port structure of the UPI. Any line can function as an input or output. All port lines are automatically initialized to 1 by a system $\overline{\text{RESET}}$ pulse and remain latched. An external TTL signal connected to a port line will override the UPI's 50 KΩ internal pull-up so that an INPUT instruction will correctly sample the TTL signal.

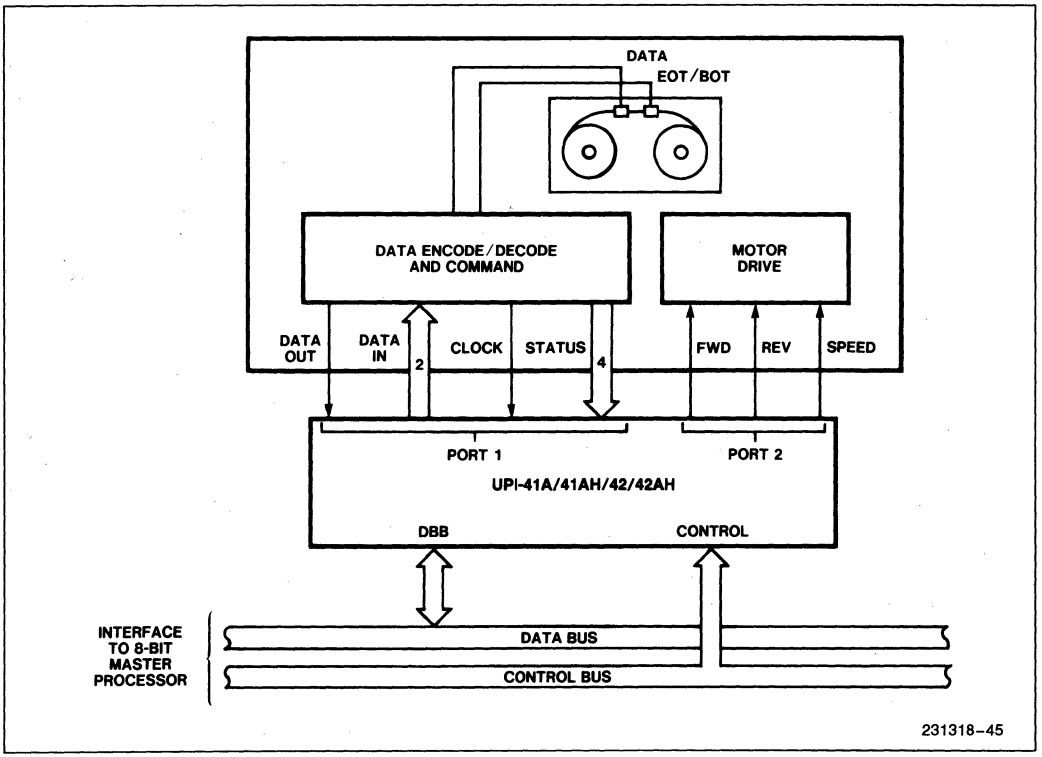


Figure 6-3. Tape Transport Controller

Four PORT 2 lines function as general I/O similar to PORT 1. Also, the RTS signal is generated on PORT 2 under software control when the UPI has serial data to send. The CTS signal is monitored via PORT 2 as an enable to the UPI to send serial data. A PORT 2 line is also used as a software generated interrupt to the master processor. The interrupt functions as a service request when the UPI has a byte of data to transfer or when it is ready to receive. Alternatively, the EN FLAGS instruction could be used to create the OBF and $\overline{IBF}$ interrupts on P_{24} and P_{25}.

The RS232C interface is implemented using the TEST 0 pin as a receive input and a PORT 2 pin as a transmit output. External packages (A_0, A_1) are used to provide RS232C drive requirements. The serial receive software is interrupt driven and uses the on-chip timer to perform time critical serial control. After a start bit is detected the interval timer can be preset to generate an interrupt at the proper time for sampling the serial bit stream. This eliminates the need for software timing loops and allows the processor to proceed to other tasks (i.e., parallel I/O operations) between serial bit samples. Software flags are used so the main program can determine when the interrupt driven receive program has a character assembled for it.

This type of configuration allows system designers flexibility in designing custom I/O interfaces for specific serial and parallel I/O applications. For instance, a second or third serial channel could be substituted in place of the parallel I/O if required. The UPI's data memory can buffer data and commands for up to 4 low-speed channels (110 baud teletypewriter, etc.)

Application Notes

The following application notes illustrate the various applications of the UPI family. Other related publications including the *Microcontroller Handbook* are available through the Intel Literature Department.

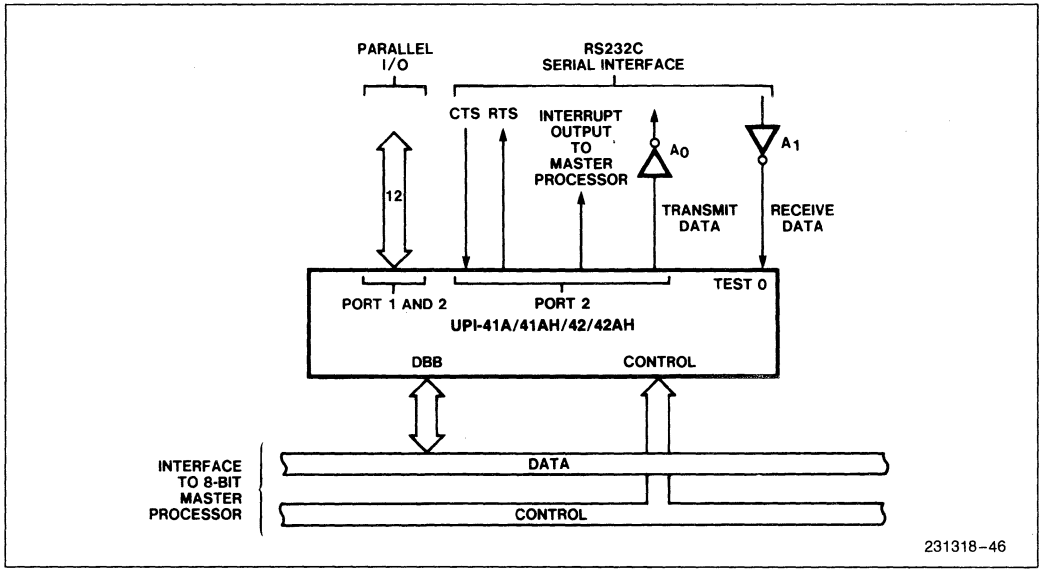


Figure 6-4. Universal I/O Interface

UPI-41AH/42AH
UNIVERSAL PERIPHERAL INTERFACE
8-BIT SLAVE MICROCONTROLLER

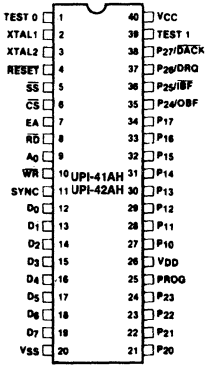
- **UPI-41: 6 MHz; UPI-42: 12.5 MHz**
- **Pin, Software and Architecturally Compatible with all UPI-41 and UPI-42 Products**
- **8-Bit CPU plus ROM/OTP EPROM, RAM, I/O, Timer/Counter and Clock in a Single Package**
- **2048 x 8 ROM/OTP, 256 x 8 RAM on UPI-42, 1024 x 8 ROM/OTP, 128 x 8 RAM on UPi-41, 8-Bit Timer/Counter, 18 Programmable I/O Pins**
- **One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface**
- **DMA, Interrupt, or Polled Operation Supported**
- **Fully Compatible with all Intel and Most Other Microprocessor Families**
- **Interchangeable ROM and OTP EPROM Versions**
- **Expandable I/O**
- **Sync Mode Available**
- **Over 90 Instructions: 70% Single Byte**
- **Available in EXPRESS — Standard Temperature Range**
- **int$_e$ligent Programming Algorithm — Fast OTP Programming**
- **Available in 40-Lead Plastic and 44-Lead Plastic Leaded Chip Carrier Packages**

(See Packaging Spec., Order #240800-001)
Package Type P and N

The Intel UPI-41AH and UPI-42AH are general-purpose Universal Peripheral Interfaces that allow the designer to develop customized solutions for peripheral device control.

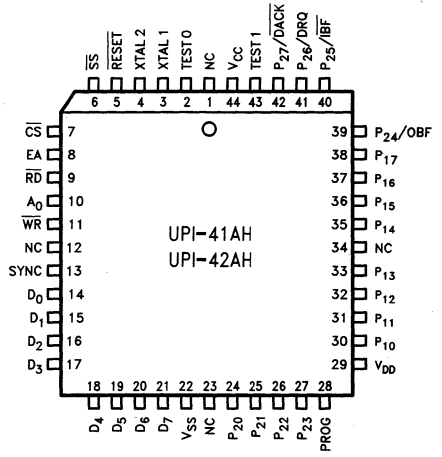
They are essentially "slave" microcontrollers, or microcontrollers with a slave interface included on the chip. Interface registers are included to enable the UPI device to function as a slave peripheral controller in the MCS Modules and iAPX family, as well as other 8-, 16-, and 32-bit systems.

To allow full user flexibility, the program memory is available in ROM and One-Time Programmable EPROM (OTP). All UPI-41AH and UPI-42AH devices are fully pin compatible for easy transition from prototype to production level designs.



210393-2

Figure 1. DIP Pin Configuration



210393-3

Figure 2. PLCC Pin Configuration

November 1994
Order Number: 210393-008

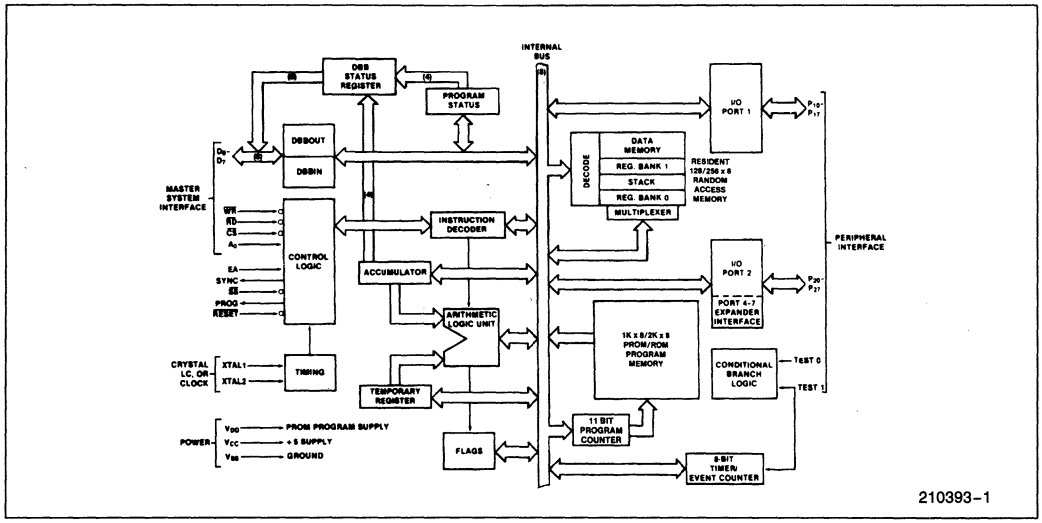


Figure 3. Block Diagram

UPI PRODUCT MATRIX

UPI Device	ROM	OTP EPROM	RAM	Programming Voltage
8042AH	2K	—	256	—
8242AH	2K	—	256	—
8742AH	—	2K	256	12.5V
8041AH	1K	—	128	—
8741AH	—	1K	128	12.5V

4

THE INTEL 8242

As shown in the UPI-42 product matrix, the UPI-42 will be offered as a pre-programmed 8042 with several software vendors' keyboard controller firmware. The current list of available 8242 versions include keyboard controller firmware from both Phoenix Technologies Ltd., IBM, and Award Software Inc. The 8242 is programmed with Phoenix Technologies Ltd. keyboard controller firmware for AT-compatible systems. This keyboard controller is fully compatible with all AT-compatible operating systems and applications. The 8242PC also contains Phoenix Technologies Ltd. firmware. This keyboard controller provides support for AT, PS/2 and most EISA platforms as well as PS/2-style mouse support for either AT or PS/2 platforms.

The Intel 8242BB is programmed with IBM's keyboard controller firmware. The 8242BB provides an off the shelf keyboard and auxiliary device controller for AT, PS/2, EISA, and PCI architectures.

The 8242WA contains Award Software Inc. firmware. This device provides at AT-compatible keyboard controller for use in IBM PC AT compatible computers. The 8242WB contains a version of Award Software Inc. firmware that provides PS/2 style mouse support in addition to the standard features of the 8242WA.

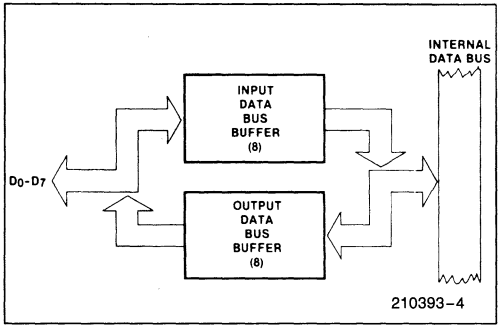
*Contact factory for current code revision available in all versions of the 8242 product lines.

Table 1. Pin Description

Symbol	DIP Pin No.	PLCC Pin No.	Type	Name and Function
TEST 0, TEST 1	1 39	2 43	I	**TEST INPUTS:** Input pins which can be directly tested using conditional branch instructions. **FREQUENCY REFERENCE:** TEST 1 (T_1) also functions as the event timer input (under software control). TEST 0 (T_0) is used during PROM programming and ROM/EPROM verification. It is also used during Sync Mode to reset the instruction state to S1 and synchronize the internal clock to PH1. See the Sync Mode Section.
XTAL 1, XTAL 2	2 3	3 4	I	**INPUTS:** Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
$\overline{\text{RESET}}$	4	5	I	**RESET:** Input used to reset status flip-flops and to set the program counter to zero. $\overline{\text{RESET}}$ is also used during EPROM programming and verification.
$\overline{\text{SS}}$	5	6	I	**SINGLE STEP:** Single step input used in conjunction with the SYNC output to step the program through each instruction (EPROM). This should be tied to +5V when not used. This pin is also used to put the device in Sync Mode by applying 12.5V to it.
$\overline{\text{CS}}$	6	7	I	**CHIP SELECT:** Chip select input used to select one UPI microcomputer out of several connected to a common data bus.
EA	7	8	I	**EXTERNAL ACCESS:** External access input which allows emulation, testing and ROM/EPROM verification. This pin should be tied low if unused.
$\overline{\text{RD}}$	8	9	I	**READ:** I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
A_0	9	10	I	**COMMAND/DATA SELECT:** Address Input used by the master processor to indicate whether byte transfer is data (A_0 = 0, F1 is reset) or command (A_0 = 1, F1 is set). A_0 = 0 during program and verify operations.
$\overline{\text{WR}}$	10	11	I	**WRITE:** I/O write input which enables the master CPU to write data and command words to the UPI INPUT DATA BUS BUFFER.
SYNC	11	13	O	**OUTPUT CLOCK:** Output signal which occurs once per UPI instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
D_0–D_7 (BUS)	12–19	14–21	I/O	**DATA BUS:** Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI microcomputer to an 8-bit master system data bus.
P_{10}–P_{17}	27–34	30–33 35–38	I/O	**PORT 1:** 8-bit, PORT 1 quasi-bidirectional I/O lines. P_{10}–P_{17} access the signature row and security bit.
P_{20}–P_{27}	21–24 35–38	24–27 39–42	I/O	**PORT 2:** 8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P_{20}–P_{23}) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4–7 access. The upper 4 bits (P_{24}–P_{27}) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P_{24} as Output Buffer Full (OBF) interrupt, P_{25} as Input Buffer Full ($\overline{\text{IBF}}$) interrupt, P_{26} as DMA Request (DRQ), and P_{27} as DMA ACKnowledge ($\overline{\text{DACK}}$).
PROG	25	28	I/O	**PROGRAM:** Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243. This pin should be tied high if unused.
V_{CC}	40	44		**POWER:** +5V main power supply pin.
V_{DD}	26	29		**POWER:** +5V during normal operation. +12.5V during programming operation. Low power standby supply pin.
V_{SS}	20	22		**GROUND:** Circuit ground potential.

UPI-41AH and UPI-42AH FEATURES

1. Two Data Bus Buffers, one for input and one for output. This allows a much cleaner Master/Slave protocol.



2. 8 Bits of Status

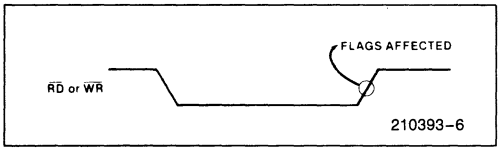
ST_7	ST_6	ST_5	ST_4	F_1	F_0	IBF	OBF
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

ST_4–ST_7 are user definable status bits. These bits are defined by the "MOV STS, A" single byte, single cycle instruction. Bits 4–7 of the acccumulator are moved to bits 4–7 of the status register. Bits 0–3 of the status register are not affected.

MOV STS, A Op Code: 90H

1	0	0	1	0	0	0	0
D_7							D_0

3. $\overline{RD}$ and $\overline{WR}$ are edge triggered. IBF, OBF, F_1 and INT change internally after the trailing edge of $\overline{RD}$ or $\overline{WR}$.

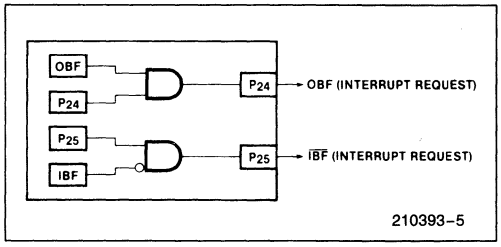


During the time that the host CPU is reading the status register, the UPI is prevented from updating this register or is 'locked out.'

4. P_{24} and P_{25} are port pins or Buffer Flag pins which can be used to interrupt a master processor. These pins default to port pins on Reset.

   If the "EN FLAGS" instruction has been executed, P_{24} becomes the OBF (Output Buffer Full) pin. A "1" written to P_{24} enables the OBF pin (the pin outputs the OBF Status Bit). A "0" written to P_{24} disables the OBF pin (the pin remains low). This pin can be used to indicate that valid data is available from the UPI (in Output Data Bus Buffer).

   If "EN FLAGS" has been executed, P_{25} becomes the $\overline{IBF}$ (Input Buffer Full) pin. A "1" written to P_{25} enables the $\overline{IBF}$ pin (the pin outputs the inverse of the IBF Status Bit. A "0" written to P_{25} disables the $\overline{IBF}$ pin (the pin remains low). This pin can be used to indicate that the UPI is ready for data.



Data Bus Buffer Interrupt Capability

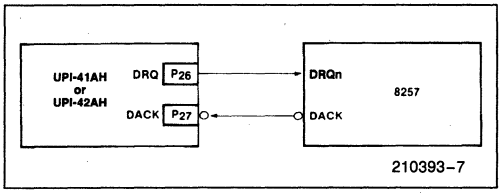
EN FLAGS Op Code: 0F5H

1	1	1	1	0	1	0	1
D_7							D_0

5. P_{26} and P_{27} are port pins or DMA handshake pins for use with a DMA controller. These pins default to port pins on Reset.

   If the "EN DMA" instruction has been executed, P_{26} becomes the DRQ (DMA Request) pin. A "1" written to P_{26} causes a DMA request (DRQ is activated). DRQ is deactivated by DACK•RD, DACK•WR, or execution of the "EN DMA" instruction.

   If "EN DMA" has been executed, P_{27} becomes the $\overline{DACK}$ (DMA ACKnowledge) pin. This pin acts as a chip select input for the Data Bus Buffer registers during DMA transfers.



DMA Handshake Capability

EN DMA Op Code: 0E5H

1	1	1	0	0	1	0	1

D_7 D_0

6. When EA is enabled on the UPI, the program counter is placed on Port 1 and the lower three bits of Port 2 (MSB = P_{22}, LSB = P_{10}). On the UPI this information is multiplexed with PORT DATA (see port timing diagrams at end of this data sheet).
7. The 8741AH and 8742AH support the int$_e$ligent Programming Algorithm. (See the Programming Section.)

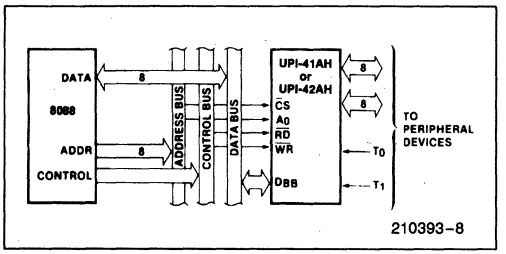


Figure 5. 8088-UPI-41AH/42AH Interface

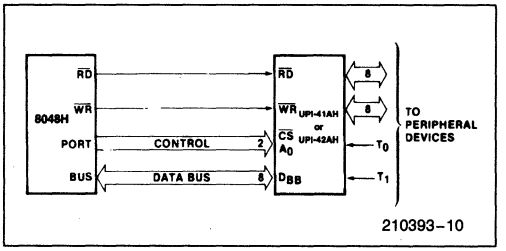


Figure 6. 8048H-UPI-41/42 Interface

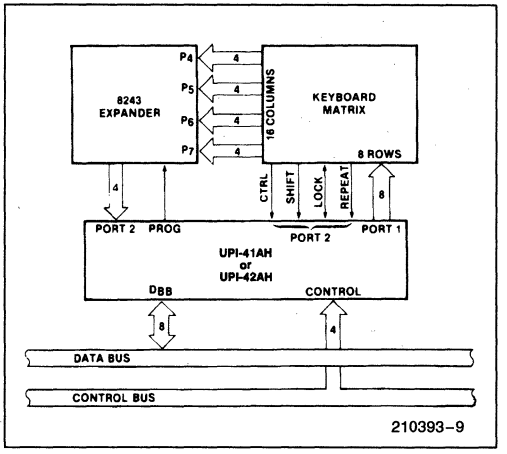


Figure 7. UPI-41/42-8243 Keyboard Scanner

APPLICATIONS

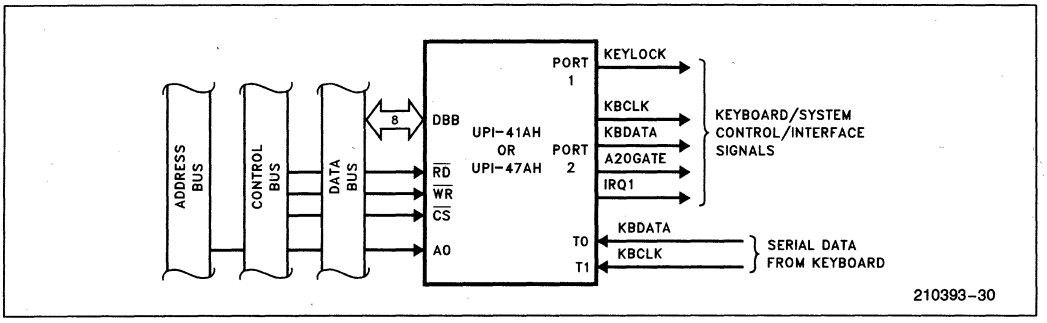


Figure 4. UPI-41AH/42AH Keyboard Controller

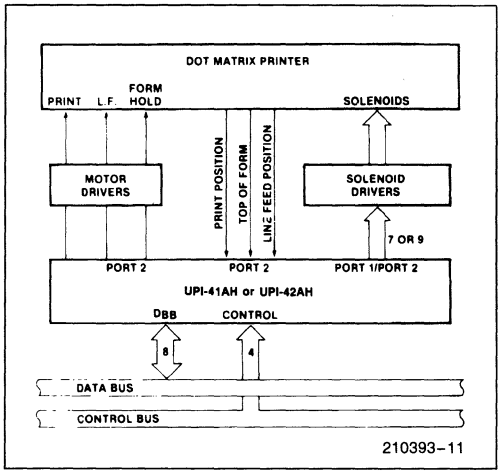


Figure 8. UPI-41AH/42AH 80-Column Matrix Printer Interface

PROGRAMMING AND VERIFYING THE 8741AH AND 8742AH OTP EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	2 Clock Inputs
$\overline{\text{Reset}}$	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Signature Row/Security Bit Modes
BUS	Address and Data Input Data Output During Verify
P_{20-22}	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING
An attempt to program a missocketed 8741AH or 8742AH will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. CS = 5V, V_{CC} = 5V, V_{DD} = 5V, RESET = 0V, A_0 = 0V, TEST 0 = 5V, clock applied or internal oscillator operating, BUS floating, PROG = 5V.
2. Insert 8741AH or 8742AH in programming socket
3. TEST 0 = 0V (select program mode)
4. EA = 12.5V (active program mode)
5. V_{CC} = 6V (programming supply)
6. V_{DD} = 12.5V (programming power)
7. Address applied to BUS and P_{20-22}
8. $\overline{\text{RESET}}$ = 5V (latch address)
9. Data applied to BUS
10. PROG = 5V followed by one 1 ms pulse to 0V
11. TEST 0 = 5V (verify mode)
12. Read and verify data on BUS
13. TEST 0 = 0V
14. Apply overprogram pulse
15. $\overline{\text{RESET}}$ = 0V and repeat from step 6
16. Programmer should be at conditions of step 1 when 8741AH or 8742AH is removed from socket

Please follow the int$_e$ligent Programming flow chart for proper programming procedure.

4

int$_e$ligent Programming Algorithm

The int$_e$ligent Programming Algorithm rapidly programs Intel 8741AH/8742AH EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming time for individual devices is on the order of 10 seconds. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the 8741AH/8742AH int$_e$ligent Programming Algorithm is shown in Figure 9.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial PROG pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular 8741AH/8742AH location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

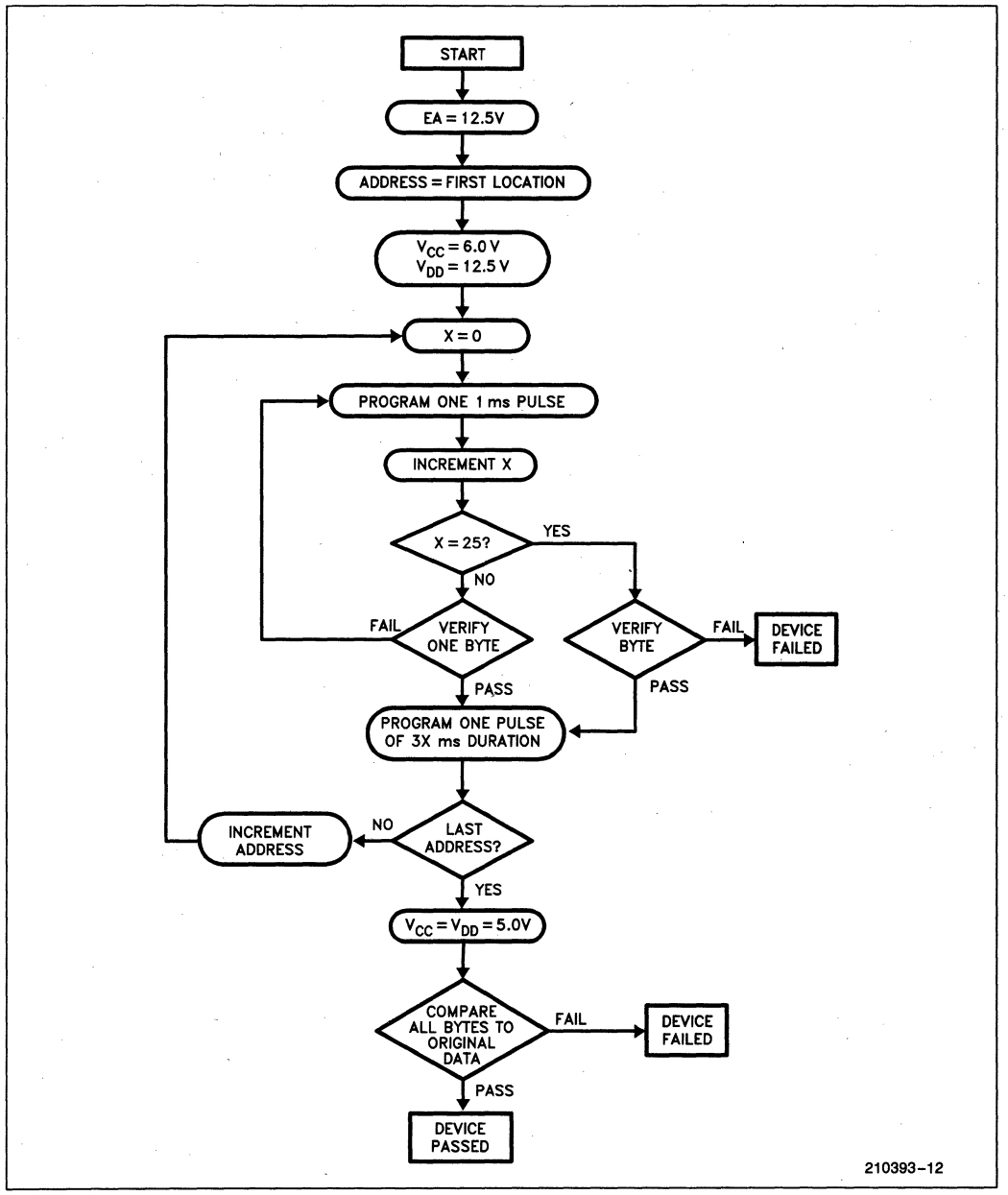


Figure 9. Programming Algorithm

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{DD} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0, V_{DD} = 5V.

Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with T0 = 5V, V_{DD} = 5V, EA = 12.5V, $\overline{SS}$ = 5V, PROG = 5V, A0 = 0V, and $\overline{CS}$ = 5V.

SECURITY BIT

The security bit is a single EPROM cell outside the EPROM array. The user can program this bit with the appropriate access code and the normal programming procedure, to inhibit any external access to the EPROM contents. Thus the user's resident program is protected. There is no direct external access to this bit. However, the security byte in the signature row has the same address and can be used to check indirectly whether the security bit has been programmed or not. The security bit has no effect on the signature mode, so the security byte can always be examined.

SECURITY BIT PROGRAMMING/ VERIFICATION

Programming

a. Read the security byte of the signature mode. Make sure it is 00H.

b. Apply access code to appropriate inputs to put the device into security mode.

c. Apply high voltage to EA and V_{DD} pins.

d. Follow the programming procedure as per the int$_e$ligent Programming Algorithm with known data on the databus. Not only the security bit, but also the security byte of the signature row is programmed.

e. Verify that the security byte of the signature mode contains the same data as appeared on the data bus. (If DB0–DB7 = high, the security byte will contain FFH.)

f. Read two consecutive known bytes from the EPROM array and verify that the wrong data are retrieved in at least one verification. If the EPROM can still be read, the security bit may have not been fully programmed though the security byte in the signature mode has.

Verification

Since the security bit address overlaps the address of the security byte of the signature mode, it can be used to check indirectly whether the security bit has been programmed or not. Therefore, the security bit verification is a mere read operation of the security byte of the signature row (0FFH = security bit programmed; 00H = security bit unprogrammed). Note that during the security bit programming, the reading of the security byte does not necessarily indicate that the security bit has been successfully programmed. Thus, it is recommended that two consecutive known bytes in the EPROM array be read and the wrong data should be read at least once, because it is highly improbable that random data coincides with the correct ones twice.

SIGNATURE MODE

The UPI-41AH/42AH has an additional 32 bytes of EPROM available for Intel and user signatures and miscellaneous purposes. The 32 bytes are partitioned as follows:

A. **Test code/checksum**—This can accommodate up to 25 bytes of code for testing the internal nodes that are not testable by executing from the external memory. The test code/checksum is present on ROMs, and OTPs.

B. **Intel signature**—This allows the programmer to read from the UPI-41AH/42AH the manufacturer of the device and the exact product name. It facilitates automatic device identification and will be present in the ROM and OTP versions. Location 10H contains the manufacturer code. For Intel, it is 89H. Location 11H contains the device code. The code is 43H and 42H for the 8042AH and OTP 8742AH, and 41H and 40H for the 8041AH and OTP 8741AH, respectively. The code is 44H for any device with the security bit set by Intel.

C. **User signature**—The user signature memory is implemented in the EPROM and consists of 2 bytes for the customer to program his own signature code (for identification purposes and quick sorting of previously programmed materials).

D. **Test signature**—This memory is used to store testing information such as: test data, bin number, etc. (for use in quality and manufacturing control).

E. **Security byte**—This byte is used to check whether the security bit has been programmed (see the security bit section).

The signature mode can be accessed by setting P10 = 0, P11–P17 = 1, and then following the programming and/or verification procedures. The location of the various address partitions are as follows:

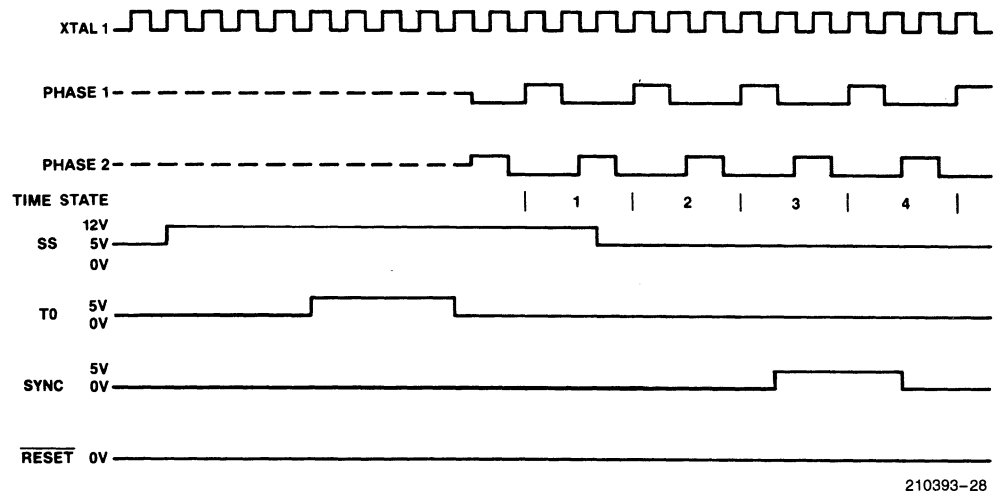
	Address		Device Type	No. of Bytes
Test Code/Checksum	0 16H	0FH 1EH	ROM/OTP	25
Intel Signature	10H	11H	ROM/OTP	2
User Signature	12H	13H	OTP	2
Test Signature	14H	15H	ROM/OTP	2
Security Byte	1FH		OTP	1

SYNC MODE

The Sync Mode is provided to ease the design of multiple controller circuits by allowing the designer to force the device into known phase and state time. The Sync Mode may also be utilized by automatic test equipment (ATE) for quick, easy, and efficient synchronizing between the tester and the DUT (device under test).

Sync Mode is enabled when $\overline{SS}$ pin is raised to high voltage level of +12 volts. To begin synchronization, T0 is raised to 5 volts at least four clock cycles after $\overline{SS}$. T0 must be high for at least four X1 clock cycles to fully reset the prescaler and time state generators. T0 may then be brought down during low state of X1. Two clock cycles later, with the rising edge of X1, the device enters into Time State 1, Phase 1. $\overline{SS}$ is then brought down to 5 volts 4 clocks later after T0. RESET is allowed to go high 5 tCY (75 clocks) later for normal execution of code.

SYNC MODE TIMING DIAGRAMS



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Minimum Specifications
SYNC Operation Time, t_{SYNC} = 3.5 XTAL 1 Clock cycles. Reset Time, t_{RS} = 4 t_{CY}.

NOTE:
The rising and falling edges of T0 should occur during low state of XTAL1 clock.

ACCESS CODE

The following table summarizes the access codes required to invoke the Sync Mode, Signature Mode, and the Security Bit, respectively. Also, the programming and verification modes are included for comparison.

Modes		Control Signals							Data Bus								Access Code							
																	Port 2	Port 1						
		T0	RST	SS	EA	PROG	V_{DD}	V_{CC}	0	1	2	3	4	5	6	7	0 1 2	0	1	2	3	4	5	6	7
Programming Mode		0	0	1	HV	1	V_{DDH}	V_{CC}	Address								Addr	a_0	a_1	X	X	X	X	X	X
		0	1	1	HV	STB	V_{DDH}	V_{CC}	Data In								Addr								
Verification Mode		0	0	1	HV	1	V_{CC}	V_{CC}	Address								Addr	a_0	a_1	X	X	X	X	X	X
		1	1	1	HV	1	V_{CC}	V_{CC}	Data Out								Addr								
Sync Mode		STB High	0	HV	0	X	V_{CC}	V_{CC}	X	X	X	X	X	X	X	X	X X X	X	X	X	X	X	X	X	X
Signature Mode	Prog	0	0	1	HV	1	V_{DDH}	V_{CC}	Addr. (see Sig Mode Table)								0 0 0	0	1	1	1	1	X	X	1
		0	1	1	HV	STB	V_{DDH}	V_{CC}	Data In								0 0 0								
	Verify	0	0	1	HV	1	V_{CC}	V_{CC}	Addr. (see Sig Mode Table)								0 0 0								
		1	1	1	HV	1	V_{CC}	V_{CC}	Data Out								0 0 0								
Security Bit/Byte	Prog	0	0	1	HV	1	V_{DDH}	V_{CC}	Address								0 0 0								
		0	1	1	HV	STB	V_{DDH}	V_{CC}	Data In								0 0 0								
	Verify	0	0	1	HV	1	V_{CC}	V_{CC}	Address								0 0 0								
		1	1	1	HV	1	V_{CC}	V_{CC}	Data Out								0 0 0								

NOTES:
1. a_0 = 0 or 1; a_1 = 0 or 1. a_0 must = a_1.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with Respect to Ground.....−0.5V to +7V
Power Dissipation .....1.5 W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ±10%

Symbol	Parameter	UPI-41AH/42AH		Units	Notes
		Min	Max		
V_{IL}	Input Low Voltage (Except XTAL1, XTAL2, RESET)	−0.5	0.8	V	
V_{IL1}	Input Low Voltage (XTAL1, XTAL2, RESET)	−0.5	0.6	V	
V_{IH}	Input High Voltage (Except XTAL1, XTAL2, RESET)	2.0	V_{CC}	V	
V_{IH1}	Input High Voltage (XTAL1, RESET)	3.5	V_{CC}	V	
V_{IH2}	Input High Voltage (XTAL2)	2.2	V_{CC}	V	
V_{OL}	Output Low Voltage (D_0–D_7)		0.45	V	I_{OL} = 2.0 mA

D.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$ (Continued)

Symbol	Parameter	UPI-41AH/42AH		Units	Notes
		Min	Max		
V_{OL1}	Output Low Voltage ($P_{10}P_{17}$, $P_{20}P_{27}$, Sync)		0.45	V	$I_{OL} = 1.6$ mA
V_{OL2}	Output Low Voltage (PROG)		0.45	V	$I_{OL} = 1.0$ mA
V_{OH}	Output High Voltage (D_0–D_7)	2.4		V	$I_{OH} = -400\ \mu A$
V_{OH1}	Output High Voltage (All Other Outputs)	2.4			$I_{OH} = -50\ \mu A$
I_{IL}	Input Leakage Current (T_0, T_1, RD, WR, CS, A_0, EA)		±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OFL}	Output Leakage Current (D_0–D_7, High Z State)		±10	μA	$V_{SS} + 0.45 \le V_{OUT} \le V_{CC}$
I_{LI}	Low Input Load Current ($P_{10}P_{17}$, $P_{20}P_{27}$)		0.3	mA	$V_{IL} = 0.8V$
I_{LI1}	Low Input Load Current (RESET, SS)		0.2	mA	$V_{IL} = 0.8V$
I_{DD}	V_{DD} Supply Current		20	mA	Typical = 8 mA
$I_{CC} + I_{DD}$	Total Supply Current		135	mA	Typical = 80 mA
I_{DD} Standby	Power Down Supply Current		20	mA	Typical = 8 mA
I_{IH}	Input Leakage Current (P_{10}–P_{17}, P_{20}–P_{27})		100	μA	$V_{IN} = V_{CC}$
C_{IN}	Input Capacitance		10	pF	$T_A = 25°C$ (1)
C_{IO}	I/O Capacitance		20	pF	$T_A = 25°C$ (1)

NOTE:
1. Sampled, not 100% tested.

4

D.C. CHARACTERISTICS—PROGRAMMING

$T_A = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{DD} = 12.5V \pm 0.5V$

Symbol	Parameter	Min	Max	Units
V_{DDH}	V_{DD} Program Voltage High Level	12	13	V(1)
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V
V_{PH}	PROG Program Voltage High Level	2.0	5.5	V
V_{PL}	PROG Voltage Low Level	−0.5	0.8	V
V_{EAH}	Input High Voltage for EA	12.0	13.0	V(2)
V_{EAL}	EA Voltage Low Level	−0.5	5.25	V
I_{DD}	V_{DD} High Voltage Supply Current		50.0	mA
I_{EA}	EA High Voltage Supply Current		1.0	mA

NOTES:
1. Voltages over 13V applied to pin V_{DD} will permanently damage the device.
2. V_{EAH} must be applied to EA before V_{DDH} and removed after V_{DDL}.
3. V_{CC} must be applied simultaneously or before V_{DD} and must be removed simultaneously or after V_{DD}.

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{SS} = 0V$, $V_{CC} = V_{DD} = +5V \pm 10\%$

DBB READ

Symbol	Parameter	Min	Max	Units
t_{AR}	CS, A_0 Setup to RD ↓	0		ns
t_{RA}	CS, A_0 Hold After RD ↑	0		ns
t_{RR}	RD Pulse Width	160		ns
t_{AD}	CS, A_0 to Data Out Delay		130	ns
t_{RD}	RD ↓ to Data Out Delay	0	130	ns
t_{DF}	RD ↑ to Data Float Delay		85	ns

DBB WRITE

Symbol	Parameter	Min	Max	Units
t_{AW}	CS, A_0 Setup to WR ↓	0		ns
t_{WA}	CS, A_0 Hold After WR ↑	0		ns
t_{WW}	WR Pulse Width	160		ns
t_{DW}	Data Setup to WR ↑	130		ns
t_{WD}	Data Hold After WR ↑	0		ns

CLOCK

Symbol	Parameter	Min	Max	Units
t_{CY} (UPI-41AH/42AH)	Cycle Time	1.2	9.20	μs(1)
t_{CYC} (UPI-41AH/42AH)	Clock Period	80	613	ns
t_{PWH}	Clock High Time	30		ns
t_{PWL}	Clock Low Time	30		ns
t_R	Clock Rise Time		10	ns
t_F	Clock Fall Time		10	ns

NOTE:
1. $t_{CY} = 15/f(XTAL)$

A.C. CHARACTERISTICS DMA

Symbol	Parameter	Min	Max	Units
t_{ACC}	DACK to WR or RD	0		ns
t_{CAC}	RD or WR to DACK	0		ns
t_{ACD}	DACK to Data Valid	0	130	ns
t_{CRQ}	RD or WR to DRQ Cleared		110	ns(1)

NOTE:
1. $C_L = 150$ pF.

A.C. CHARACTERISTICS—PROGRAMMING

T_A = 25°C ±5°C, V_{CC} = 6V ±0.25V, V_{DDL} = +5V ±0.25V, V_{DDH} = 12.5V ±0.5V
(8741AH/8742AH ONLY)

Symbol	Parameter	Min	Max	Units
t_{AW}	Address Setup Time to RESET ↑	$4t_{CY}$		
t_{WA}	Address Hold Time After RESET ↑	$4t_{CY}$		
t_{DW}	Data in Setup Time to PROG ↓	$4t_{CY}$		
t_{WD}	Data in Hold Time After PROG ↑	$4t_{CY}$		
t_{PW}	Initial Program Pulse Width	0.95	1.05	ms(1)
t_{TW}	Test 0 Setup Time for Program Mode	$4t_{CY}$		
t_{WT}	Test 0 Hold Time After Program Mode	$4t_{CY}$		
t_{DO}	Test 0 to Data Out Delay		$4t_{CY}$	
t_{WW}	RESET Pulse Width to Latch Address	$4t_{CY}$		
t_r, t_f	PROG Rise and Fall Times	0.5	100	μs
t_{CY}	CPU Operation Cycle Time	2.5	3.75	μs
t_{RE}	RESET Setup Time Before EA ↑	$4t_{CY}$		
t_{OPW}	Overprogram Pulse Width	2.85	78.75	ms(2)
t_{DE}	EA High to V_{DD} High	$1t_{CY}$		

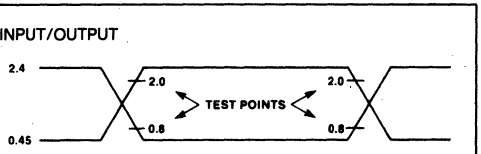
NOTES:
1. Typical Initial Program Pulse width tolerance = 1 ms ±5%.
2. This variation is a function of the iteration counter value, X.
3. If TEST 0 is high, t_{DO} can be triggered by RESET ↑.

A.C. CHARACTERISTICS PORT 2 T_A = 0°C to +70°C, V_{CC} = +5V ±10%

Symbol	Parameter	$f(t_{CY})$(3)	Min	Max	Units
t_{CP}	Port Control Setup Before Falling Edge of PROG	$1/15\ t_{CY}-28$	55		ns(1)
t_{PC}	Port Control Hold After Falling Edge of PROG	$1/10\ t_{CY}$	125		ns(2)
t_{PR}	PROG to Time P2 Input Must Be Valid	$8/15\ t_{CY}-16$		650	ns(1)
t_{PF}	Input Data Hold Time		0	150	ns(2)
t_{DP}	Output Data Setup Time	$2/10\ t_{CY}$	250		ns(1)
t_{PD}	Output Data Hold Time	$1/10\ t_{CY}-80$	45		ns(2)
t_{PP}	PROG Pulse Width	$6/10\ t_{CY}$	750		ns

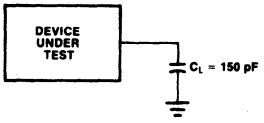
NOTES:
1. C_L = 80 pF.
2. C_L = 20 pF.
3. t_{CY} = 1.25 μs.

A.C. TESTING INPUT/OUTPUT WAVEFORM



210393-14

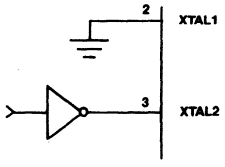
A.C. TESTING LOAD CIRCUIT



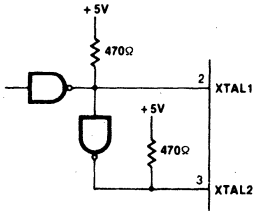
210393-15

DRIVING FROM EXTERNAL SOURCE-TWO OPTIONS

>6 MHz



210393-16

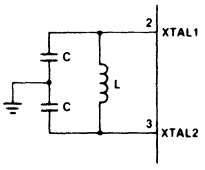


210393-17

Rise and Fall Times Should Not Exceed 10 ns. Resistors to V_{CC} are Needed to Ensure V_{IH} = 3.5V if TTL Circuitry is Used.

LC OSCILLATOR MODE

L	C	NOMINAL
45 H	20 pF	5.2 MHz
120 H	20 pF	3.2 MHz



$$f = \frac{1}{2\pi\sqrt{LC'}}$$

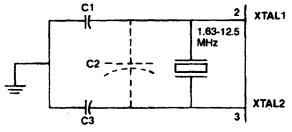
$$C' = \frac{C + 3Cpp}{2}$$

Cpp ≅ 5–10 pF
Pin-to-Pin Capacitance

210393-18

Each C Should be Approximately 20 pF, including Stray Capacitance.

CRYSTAL OSCILLATOR MODE



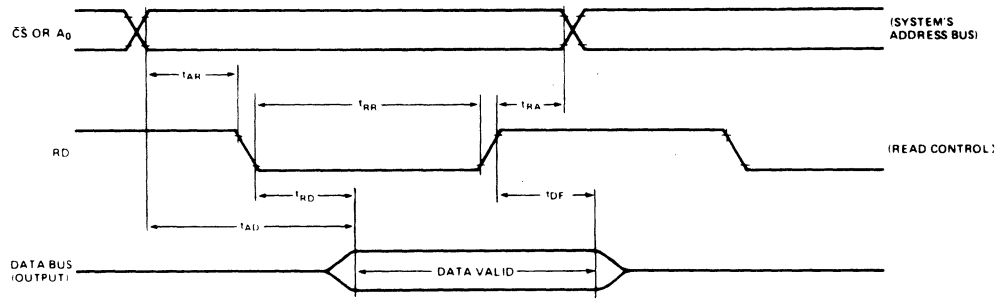
210393-19

C1 5 pF (STRAY 5 pF)
C2 (CRYSTAL + STRAY) 8 pF
C3 20–30 pF INCLUDING STRAY

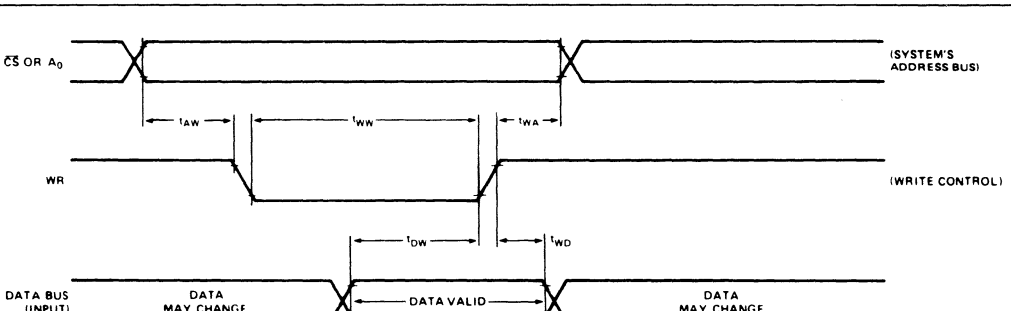
Crystal Series Resistance Should be Less Than 30Ω at 12.5 MHz.

WAVEFORMS

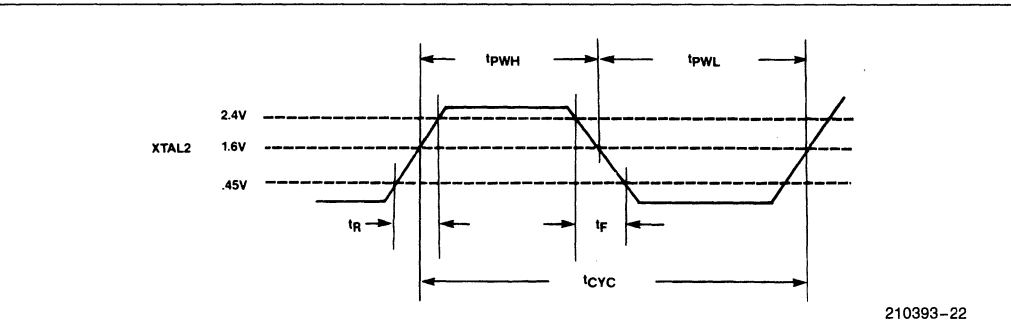
READ OPERATION—DATA BUS BUFFER REGISTER



WRITE OPERATION—DATA BUS BUFFER REGISTER

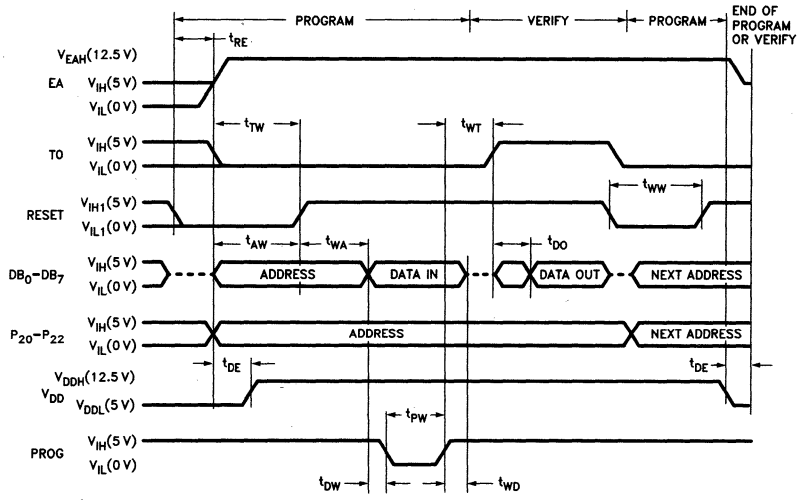


CLOCK TIMING



WAVEFORMS (Continued)

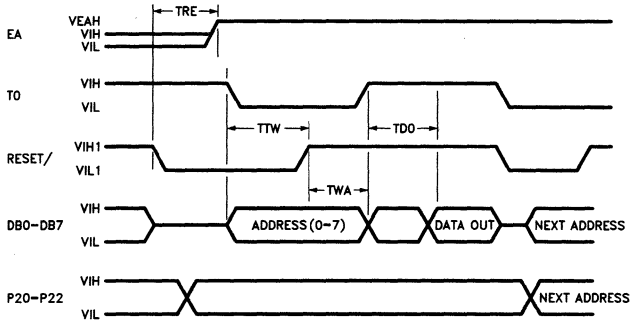
COMBINATION PROGRAM/VERIFY MODE



210393-23

NOTES:
1. A_0 must be held low (0V) during program/verify modes.
2. For V_{IH}, V_{IH1}, V_{IL}, V_{IL1}, V_{DDH}, and V_{DDL}, please consult the D.C. Characteristics Table.
3. When programming the 8741AH/8742AH, a 0.1 μF capacitor is required across V_{DD} and ground to suppress spurious voltage transients which can damage the device.

VERIFY MODE

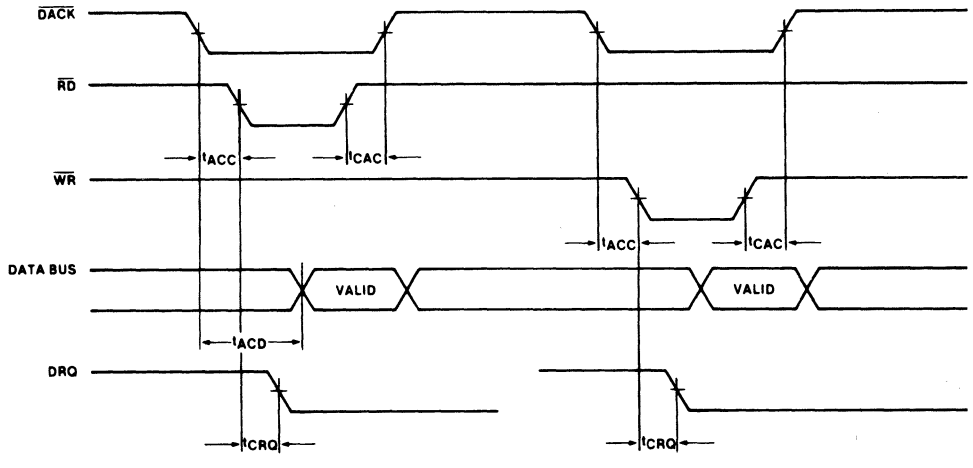


210393-29

NOTES:
1. PROG must float if EA is low.
2. PROG must float or = 5V when EA is high.
3. P_{10}–P_{17} = 5V or must float.
4. P_{24}–P_{27} = 5V or must float.
5. A_0 must be held low during programming/verify modes.

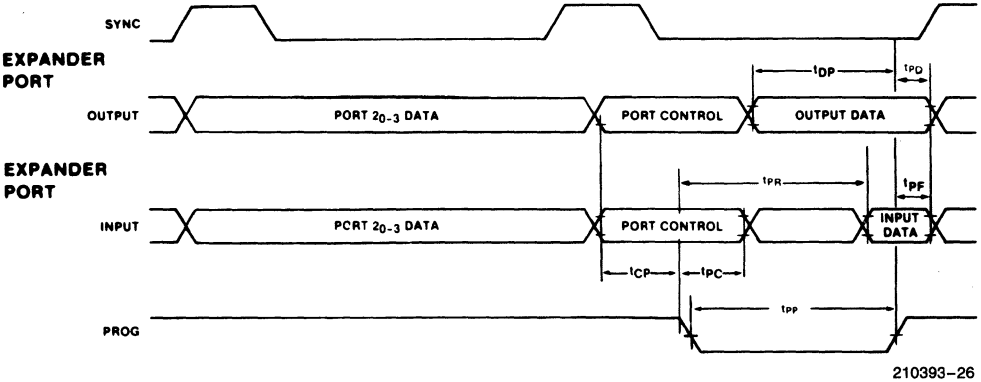
WAVEFORMS (Continued)

DMA



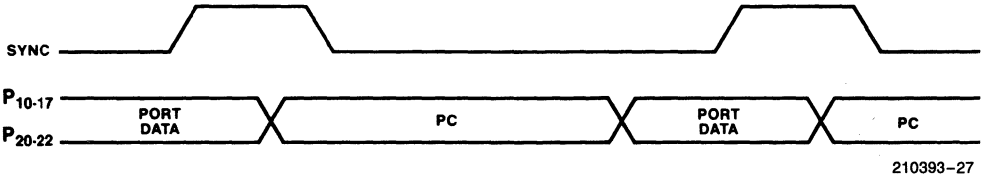
210393-25

PORT 2



210393-26

PORT TIMING DURING EXTERNAL ACCESS (EA)



210393-27

On the Rising Edge of SYNC and EA is Enabled, Port Data is Valid and can be Strobed. On the Trailing Edge of Sync the Program Counter Contents are Available.

Table 2. UPI Instruction Set

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR			
ADD A, Rr	Add register to A	1	1
ADD A, @Rr	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	2
ADDC A, Rr	Add register to A with carry	1	1
ADDC A, @Rr	Add data memory to A with carry	1	1
ADDC A, #data	Add immediate to A with carry	2	2
ANL A, Rr	AND register to A	1	1
ANL, A @Rr	AND data memory to A	1	1
ANL A, #data	AND immediate to A	2	2
ORL A, Rr	OR register to A	1	1
ORL, A, @Rr	OR data memory to A	1	1
ORL A, #data	OR immediate to A	2	2
XRL A, Rr	Exclusive OR register to A	1	1
XRL A, @Rr	Exclusive OR data memory to A	1	1
XRL A, #data	Exclusive OR immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal Adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
INPUT/OUTPUT			
IN A, Pp	Input port to A	1	2
OUTL Pp, A	Output A to port	1	2
ANL Pp, #data	AND immediate to port	2	2
ORL Pp, #data	OR immediate to port	2	2
IN A, DBB	Input DBB to A, clear IBF	1	1
OUT DBB, A	Output A to DBB, set OBF	1	1
MOV STS, A	A_4–A_7 to Bits 4–7 of Status	1	1
MOVD A, Pp	Input Expander port to A	1	2
MOVD Pp, A	Output A to Expander port	1	2
ANLD Pp, A	AND A to Expander port	1	2
ORLD Pp, A	OR A to Expander port	1	2

Mnemonic	Description	Bytes	Cycles
DATA MOVES			
MOV A, Rr	Move register to A	1	1
MOV A, @Rr	Move data memory to A	1	1
MOV A, #data	Move immediate to A	2	2
MOV Rr, A	Move A to register	1	1
MOV @Rr, A	Move A to data memory	1	1
MOV Rr, #data	Move immediate to register	2	2
MOV @Rr, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, Rr	Exchange A and register	1	1
XCH A, @Rr	Exchange A and data memory	1	1
XCHD A, @Rr	Exchange digit of A and register	1	1
MOVP A, @A	Move to A from current page	1	2
MOVP3, A, @A	Move to A from page 3	1	2
TIMER/COUNTER			
MOV A, T	Read Timer/Counter	1	1
MOV T, A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	Start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/ Counter Interrupt	1	1
DIS TCNTI	Disable Timer/ Counter Interrupt	1	1
CONTROL			
EN DMA	Enable DMA Handshake Lines	1	1
EN I	Enable IBF Interrupt	1	1
DIS I	Diable IBF Interrupt	1	1
EN FLAGS	Enable Master Interrupts	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
NOP	No Operation	1	1
REGISTERS			
INC Rr	Increment register	1	1
INC @Rr	Increment data memory	1	1
DEC Rr	Decrement register	1	1

Table 2. UPI Instruction Set (Continued)

Mnemonic	Description	Bytes	Cycles
SUBROUTINE			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2
FLAGS			
CLR C	Clear Carry	1	1
CPL C	Complement Carry	1	1
CLR F0	Clear Flag 0	1	1
CPL F0	Complement Flag 0	1	1
CLR F1	Clear F1 Flag	1	1
CPL F1	Complement F1 Flag	1	1
BRANCH			
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ Rr, addr	Decrement register and jump	2	2
JC addr	Jump on Carry = 1	2	2
JNC addr	Jump on Carry = 0	2	2
JZ addr	Jump on A Zero	2	2
JNZ addr	Jump on A not Zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 Flag = 1	2	2
JF1 addr	Jump on F1 Flag = 1	2	2
JTF addr	Jump on Timer Flag = 1, Clear Flag	2	2
JNIBF addr	Jump on IBF Flag = 0	2	2
JOBF addr	Jump on OBF Flag = 1	2	2
JBb addr	Jump on Accumula- for Bit	2	2

8741A
UNIVERSAL PERIPHERAL INTERFACE
8-BIT MICROCOMPUTER

- **8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package**
- **One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface**
- **DMA, Interrupt, or Polled Operation Supported**
- **1024 x 8 EPROM, 64 x 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins**
- **Fully Compatible with All Microprocessor Families**
- **3.6 MHz 8741A-8 Available**
- **Expandable I/O**
- **RAM Power-Down Capability**
- **Over 90 Instructions: 70% Single Byte**
- **Available in EXPRESS**
  — Standard Temperature Range
  — Extended Temperature Range

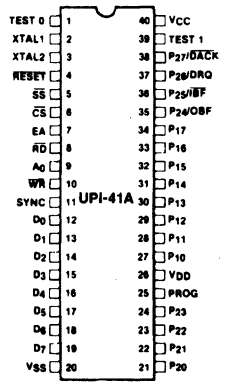
The Intel 8741A is a general purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in MCS®-48, MCS-80, MCS-85, MCS-86, and other 8-bit systems.

The UPI-41A has 1K words of program memory and 64 words of data memory on-chip.

The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, single-step mode for debug and dual working register banks.

Because it's a complete microcomputer, the UPI provides more flexibility for the designer than conventional LSI interface devices. It is designed to be an efficient controller as well as an arithmetic processor. Applications include keyboard scanning, printer control, display multiplexing and similar functions which involve interfacing peripheral devices to microprocessor systems.

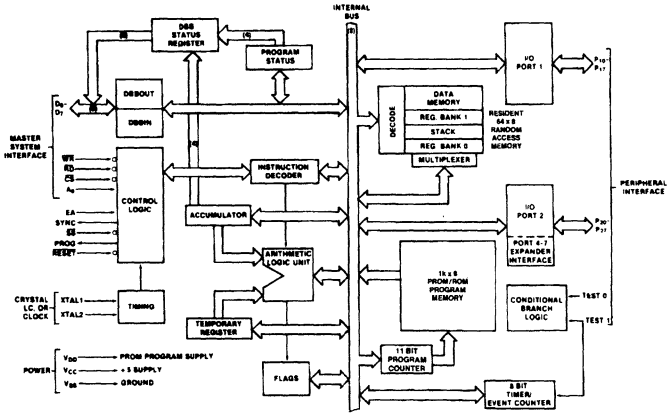
Pin Configuration



290241-2

October 1989
Order Number: 290241-001

Block Diagram



290241-1

Table 1. Pin Description

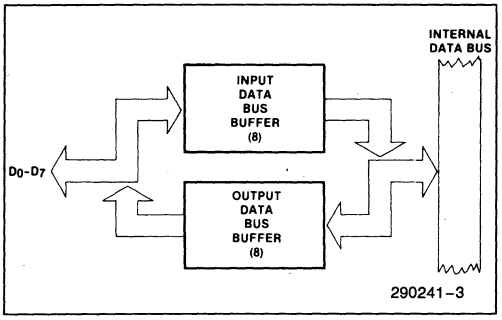
Signal	Description
D_0–D_7 (BUS)	Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI-41A to an 8-bit master system data bus.
P_{10}–P_{17}	8-bit, PORT 1 quasi-bidirectional I/O lines.
P_{20}–P_{27}	8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P_{20}–P_{23}) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4–7 access. The upper 4 bits (P_{24}–P_{27}) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P_{24} as OBF (Output Buffer Full), P_{25} as $\overline{IBF}$ (Input Buffer Full), P_{26} as DRQ (DMA Request), and P_{27} as $\overline{DACK}$ (DMA ACKnowledge).
$\overline{WR}$	I/O write input which enables the master CPU to write data and command words to the UPI-41A INPUT DATA BUS BUFFER.
$\overline{RD}$	I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
$\overline{CS}$	Chip select input used to select one UPI-41A out of several connected to a common data bus.
A_0	Address input used by the master processor to indicate whether byte transfer is data or command. During a write operation flag F_1 is set to the status of the A_0 input.
TEST 0, TEST 1	Input pins which can be directly tested using conditional branch instructions. (T_1) also functions as the event timer input (under software control). T_0 is used during PROM programming and verification in the 8741A.

Signal	Description
XTAL 1, XTAL 2	Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
SYNC	Output signal which occurs once per UPI-41A instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
EA	External access input which allows emulation, testing and PROM verification.
PROG	Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243.
$\overline{RESET}$	Input used to reset status flip-flops and to set the program counter to zero. $\overline{RESET}$ is also used during PROM programming and verification. $\overline{RESET}$ should be held low for a minimum of 8 instruction cycles after power-up.
$\overline{SS}$	Single step input used in the 8741A in conjunction with the SYNC output to step the program through each instruction.
V_{CC}	+5V main power supply pin.
V_{DD}	+5V during normal operation. +25V during programming operation. Low power standby supply pin in ROM version.
V_{SS}	Circuit ground potential.

4

UPI-41A FEATURES AND ENHANCEMENTS

1. Two Data Bus Buffers, one for input and one for output. This allows a much cleaner Master/Slave protocol.



2. 8 Bits of Status

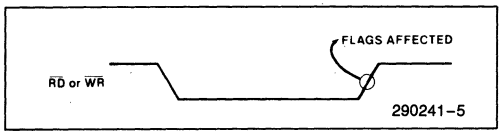
ST_7	ST_6	ST_5	ST_4	F_1	F_0	IBF	OBF
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

ST_4–ST_7 are user definable status bits. These bits are defined by the "MOV STS, A" single byte, single cycle instruction. Bits 4–7 of the accumulator are moved to bits 4–7 of the status register. Bits 0–3 of the status register are not affected.

MOV STS, A Op Code: 90H

1	0	0	1	0	0	0	0
D_7							**D_0**

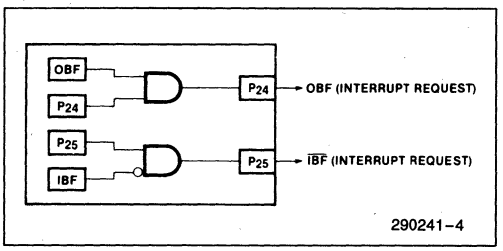
3. $\overline{RD}$ and $\overline{WR}$ are edge triggered. IBF, OBF, F_1 and INT change internally after the trailing edge of $\overline{RD}$ or $\overline{WR}$.



4. P_{24} and P_{25} are port pins or Buffer Flag pins which can be used to interrupt a master processor. These pins default to port pins on Reset.

   If the "EN FLAGS" instruction has been executed, P_{24} becomes the OBF (Output Buffer Full) pin. A "1" written to P_{24} enables the OBF pin (the pin outputs the OBF Status Bit). A "0" written to P_{24} disables the OBF pin (the pin remains low). This pin can be used to indicate that valid data is available from the UPI41A (in Output Data Bus Buffer).

   If "EN FLAGS" has been executed, P_{25} becomes the $\overline{IBF}$ (Input Buffer Full) pin. A "1" written to P_{25} enables the $\overline{IBF}$ pin (the pin outputs the inverse of the IBF Status Bit). A "0" written to P_{25} disables the $\overline{IBF}$ pin (the pin remains low). This pin can be used to indicate that the UPI is ready for data.



Data Bus Buffer Interrupt Capability

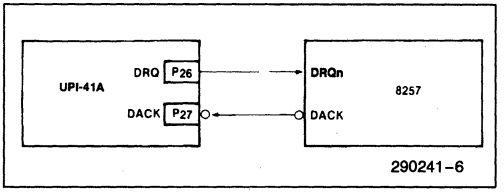
EN FLAGS Op Code: 0F5H

1	1	1	1	0	1	0	1
D_7							**D_0**

5. P_{26} and P_{27} are port pins or DMA handshake pins for use with a DMA controller. These pins default to port pins on Reset.

   If the "EN DMA" instruction has been executed, P_{26} becomes the DRQ (DMA Request) pin. A "1" written to P_{26} causes a DMA request (DRQ is activated). DRQ is deactivated by DACK•RD, DACK•WR, or execution of the "EN DMA" instruction.

   If "EN DMA" has been executed, P_{27} becomes the $\overline{DACK}$ (DMA Acknowledge) pin. This pin acts as a chip select input for the Data Bus Buffer registers during DMA transfers.



DMA Handshake Capability

EN DMA Op Code: 0E5H

1	1	1	0	0	1	0	1
D_7							**D_0**

APPLICATIONS

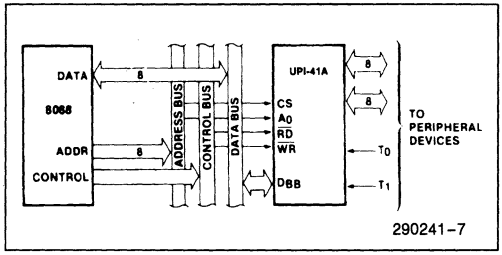


Figure 1. 8085A-8741A Interface

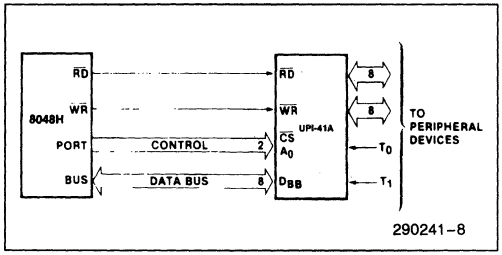


Figure 2. 8048-8741A Interface

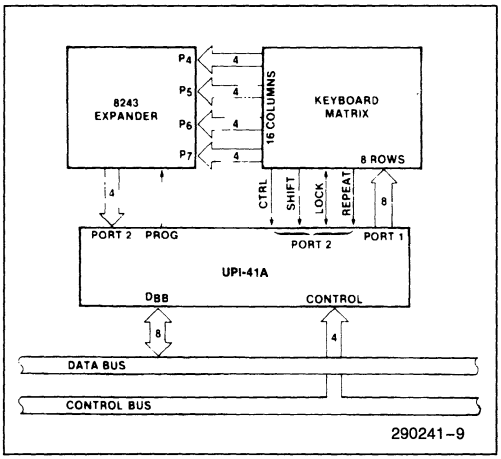


Figure 3. 8741A-8243 Keyboard Scanner

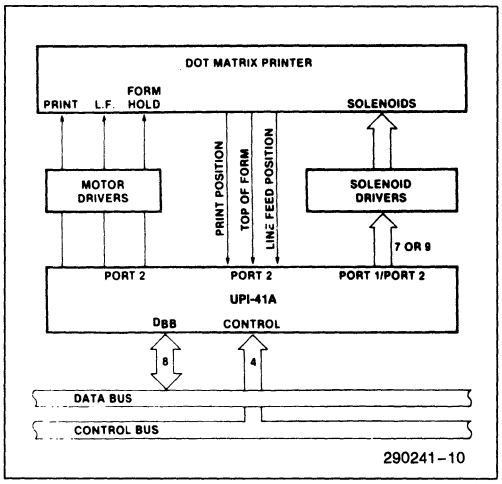


Figure 4. 8741A Matrix Printer Interface

4

PROGRAMMING, VERIFYING, AND ERASING THE 8741A EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock Input (1 to 6 MHz)
$\overline{\text{Reset}}$	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input
	Data Output during Verify
P20–1	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING:
An attempt to program a missocketed 8741A will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. A_0 = 0V, CS = 5V, EA = 5V, $\overline{\text{RESET}}$ = 0V, TEST0 = 5V, V_{DD} = 5V, clock applied or internal oscillator operating, BUS and PROG floating
2. Insert 8741A in programming socket
3. TEST 0 = 0V (select program mode)
4. EA = 23V (active program mode)
5. Address applied to BUS and P20–1
6. $\overline{\text{RESET}}$ = 5V (latch address)
7. Data applied to BUS
8. V_{DD} = 25V (programming power)
9. PROG = 0V followed by one 50 ms pulse to 23V
10. V_{DD} = 5V
11. TEST 0 = 5V (verify mode)
12. Read and verify data on BUS
13. TEST 0 = 0V
14. $\overline{\text{RESET}}$ = 0V and repeat from step 6
15. Programmer should be at conditions of step 1 when 8741A is removed from socket

8741A Erasure Characteristics

The erasure characteristics of the 8741A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8741A in approximately 3 years while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 8741A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8741A window to prevent unintentional erasure.

The recommended erasure procedure for the 8741A is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 w-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The 8741A should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with
Respect to Ground.....0.5V to +7V
Power Dissipation.....1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS} 0V, V_{CC} = V_{DD} = +5V ±10%

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (except XTAL1, XTAL2, $\overline{RESET}$)	−0.5	0.8	V	
V_{IL1}	Input Low Voltage (XTAL1, XTAL2, $\overline{RESET}$)	−0.5	0.6	V	
V_{IH}	Input High Voltage (except XTAL1, XTAL2, $\overline{RESET}$)	2.2	V_{CC}		
V_{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{RESET}$)	3.8	V_{CC}	V	
V_{OL}	Output Low Voltage (D_0–D_7)		0.45	V	I_{OL} = 2.0 mA
V_{OL1}	Output Low Voltage ($P_{10}P_{17}$, $P_{20}P_{27}$, Sync)		0.45	V	I_{OL} = 1.6 mA
V_{OL2}	Output Low Voltage (PROG)		0.45	V	I_{OL} = 1.0 mA
V_{OH}	Output High Voltage (D_0–D_7)	2.4		V	I_{OH} = −400 μA
V_{OH1}	Output High Voltage (All Other Outputs)	2.4		V	I_{OH} = −50 μA
I_{IL}	Input Leakage Current (T_0, T_1, $\overline{RD}$,$\overline{WR}$, $\overline{CS}$, A_0, EA)		±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OZ}	Output Leakage Current (D_0–D_7, High Z State)		±10	μA	V_{SS} +0.45 $\le V_{IN} \le V_{CC}$
I_{LI}	Low Input Load Current ($P_{10}P_{17}$, $P_{20}P_{27}$)		0.5	mA	V_{IL} = 0.8V
I_{LI1}	Low Input Load Current ($\overline{RESET}$, $\overline{SS}$)		0.2	mA	V_{IL} = 0.8V
I_{DD}	V_{DD} Supply Current		15	mA	Typical = 5 mA
I_{CC} + I_{DD}	Total Supply Current		125	mA	Typical = 60 mA

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS} = 0V, V_{CC} = V_{DD} = +5V ±10%

DBB READ

Symbol	Parameter	Min	Max	Unit	Test Conditions
t_{AR}	$\overline{CS}$, A_0 Setup to $\overline{RD}$ ↓	0		ns	
t_{RA}	$\overline{CS}$, A_0 Hold after $\overline{RD}$ ↑	0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	250		ns	
t_{AD}	$\overline{CS}$, A_0 to Data Out Delay		225	ns	C_L = 150 pF
t_{RD}	$\overline{RD}$ ↓ to Data Out Delay		225	ns	C_L = 150 pF
t_{DF}	$\overline{RD}$ ↑ to Data Float Delay		100	ns	
t_{CY}	Cycle Time (except 8741A-8)	2.5	15	μs	6.0 MHz XTAL
t_{CY}	Cycle Time (8741A-8)	4.17	15	μs	3.6 MHz XTAL

4

DBB WRITE

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	$\overline{CS}$, A_0 Setup to $\overline{WR}$ ↓	0		ns	
t_{WA}	$\overline{CS}$, A_0 Hold after $\overline{WR}$ ↑	0		ns	
t_{WW}	$\overline{WR}$ Pulse Width	250		ns	
t_{DW}	Data Setup to $\overline{WR}$ ↑	150		ns	
t_{WD}	Data Hold after $\overline{WR}$ ↑	0		ns	

A.C. TIMING SPECIFICATION FOR PROGRAMMING

T_A = 0°C to +70°C, V_{CC} = +5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	Address Setup Time to $\overline{RESET}$ ↑	$4t_{CY}$			
t_{WA}	Address Hold Time after $\overline{RESET}$ ↑	$4t_{CY}$			
t_{DW}	Data in Setup Time to PROG ↑	$4t_{CY}$			
t_{WD}	Data in Hold Time after PROG ↓	$4t_{CY}$			
t_{PH}	$\overline{RESET}$ Hold Time to Verify	$4t_{CY}$			
t_{VDDW}	V_{DD} Setup Time to PROG ↑	$4t_{CY}$			
t_{VDDH}	V_{DD} Hold Time after PROG ↓	0			
t_{PW}	Program Pulse Width	50	60	ms	
t_{TW}	Test 0 Setup Time for Program Mode	$4t_{CY}$			
t_{WT}	Test 0 Hold Time after Program Mode	$4t_{CY}$			
t_{DO}	Test 0 to Data Out Delay		$4t_{CY}$		
t_{WW}	$\overline{RESET}$ Pulse Width to Latch Address	$4t_{CY}$			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	5.0		μs	
t_{RE}	$\overline{RESET}$ Setup Time before EA ↑	$4t_{CY}$			

NOTE:
1. If TEST 0 is high, t_{DO} can be triggered by $\overline{RESET}$ ↑.

D.C. SPECIFICATION FOR PROGRAMMING

T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{DD} = 25V ±1V

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{DOH}	V_{DD} Program Voltage High Level	24.0	26.0	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	21.5	24.5	V	
V_{PL}	PROG Voltage Low Level		0.2	V	
V_{EAH}	EA Program or Verify Voltage High Level	21.5	24.5	V	
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		16.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

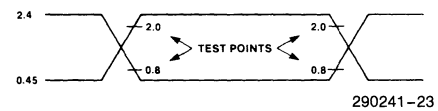
A.C. CHARACTERISTICS—DMA

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{ACC}	$\overline{DACK}$ to $\overline{WR}$ or $\overline{RD}$	0		ns	
t_{CAC}	$\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$	0		ns	
t_{ACD}	$\overline{DACK}$ to Data Valid		225	ns	C_L = 150 pF
t_{CRQ}	$\overline{RD}$ or $\overline{WR}$ to DRQ Cleared		200	ns	

A.C. CHARACTERISTICS—PORT 2 T_A = 0°C to +70°C, V_{CC} = +5V ±10%

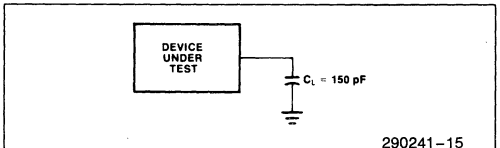
Symbol	Parameter	Min	Max	Units	Test Conditions
t_{CP}	Port Control Setup before Falling Edge of PROG	10		ns	
t_{PC}	Port Control Hold after Falling Edge of PROG	100		ns	
t_{PR}	PROG to Time P2 Input Must Be Valid		810	ns	
t_{PF}	Input Data Hold Time	0	150	ns	
t_{DP}	Output Data Setup Time	250		ns	
t_{PD}	Output Data Hold Time	65		ns	
t_{PP}	PROG Pulse Width	1200		ns	

A.C. TESTING INPUT/OUTPUT WAVEFORM



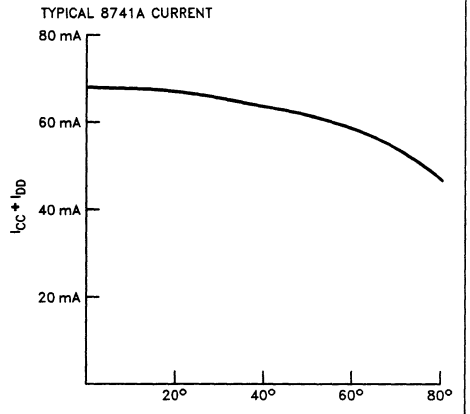
290241-23

A.C. TESTING LOAD CIRCUIT



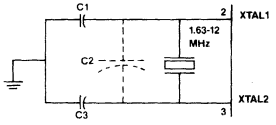
290241-15

TYPICAL 8741A CURRENT



290241-14

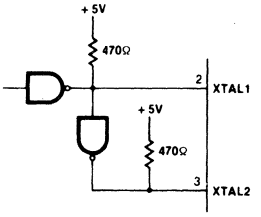
CRYSTAL OSCILLATOR MODE



290241-11

Crystal series resistance should be
< 75Ω at 6 MHz; < 180Ω at 3.6 MHz.

DRIVING FROM EXTERNAL SOURCE

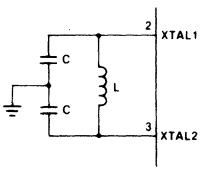


290241-12

Both XTAL1 and XTAL2 should be driven.
Resistors to V_{CC} are needed to ensure V_{IH} = 3.8V if TTL circuitry is used.

LC OSCILLATOR MODE

L	C	NOMINAL f
45 μH	20 pF	5.2 MHz
120 μH	20 pF	3.2 MHz



$$f = \frac{1}{2\pi\sqrt{LC'}}$$

$$C' = \frac{C + 3Cpp}{2}$$

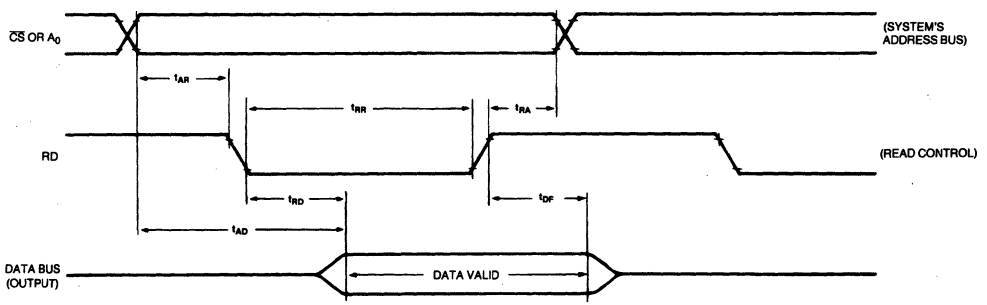
Cpp ≅ 5-10 pF
Pin-to-Pin Capacitance

290241-13

Each C should be approximately 20 pF, including stray capacitance.

WAVEFORMS

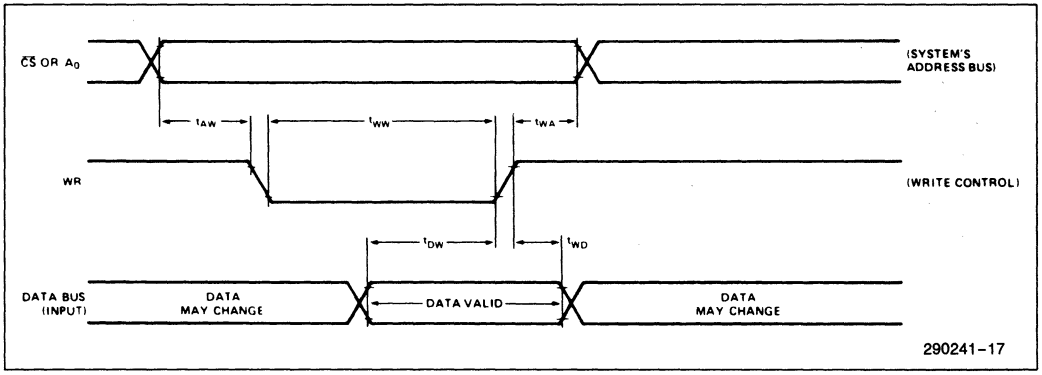
READ OPERATION—DATA BUS BUFFER REGISTER



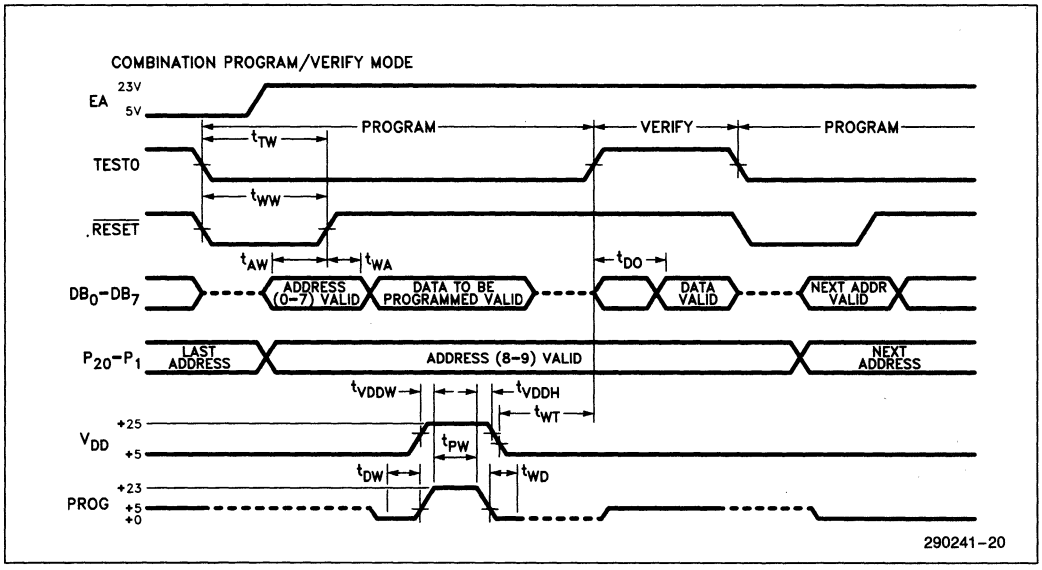
290241-16

WAVEFORMS

WRITE OPERATION—DATA BUS BUFFER REGISTER



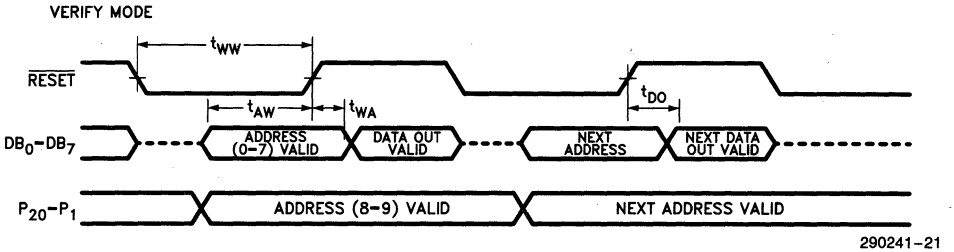
COMBINATION PROGRAM/VERIFY MODE



4

WAVEFORMS

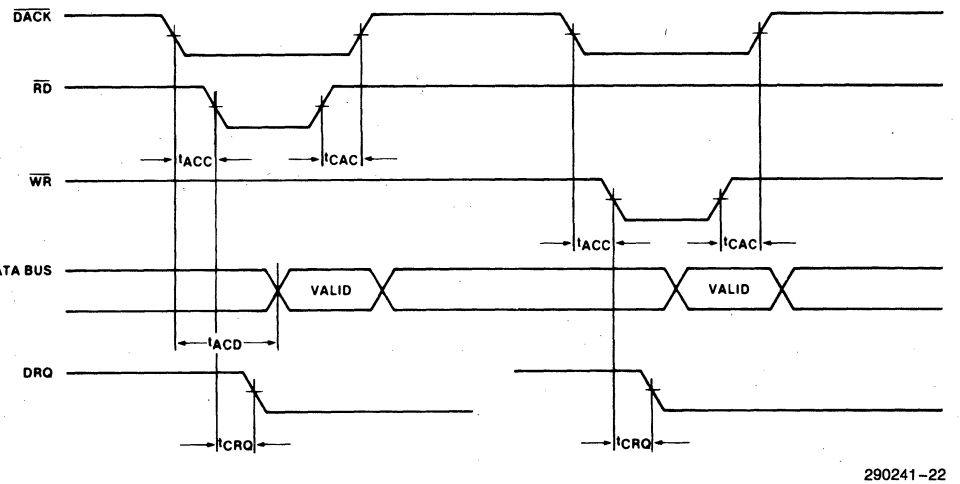
VERIFY MODE



290241-21

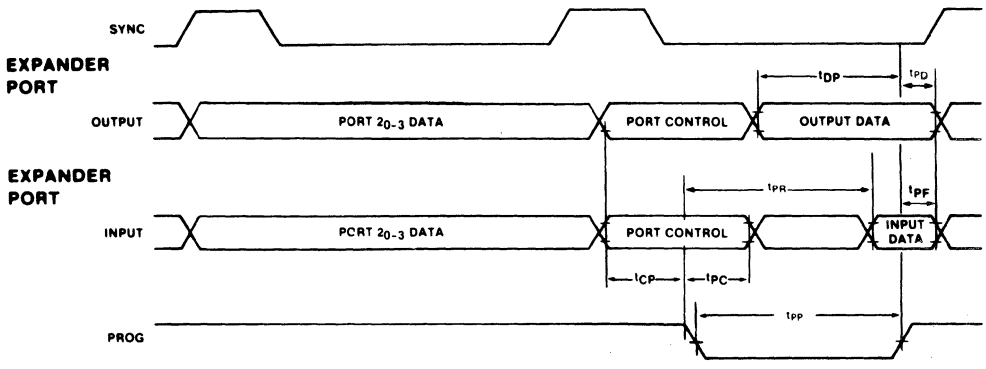
NOTES:
1. PROG must float if EA is low (i.e., ≠23V), or if T0 = 5V for the 8741A.
2. XTAL1 and XTAL2 driven by 3.6 MHz clock will give 7.17 μs t_{CY}. This is acceptable for 8741-8 parts as well as standard parts.
PROG must float or = 5V when EA is high.
3. A_0 must be held low (i.e., = 0V) during program/verify modes.

DMA



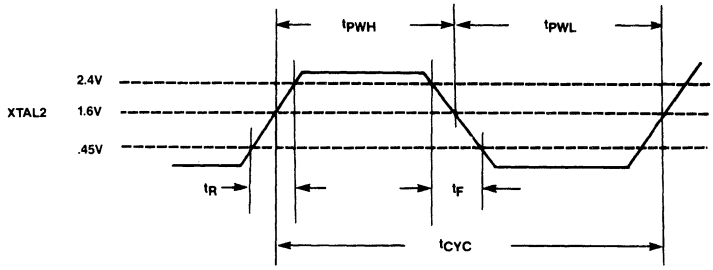
290241-22

PORT 2 TIMING



290241-19

PORT TIMING DURING EXTERNAL ACCESS (EA)



290241-18

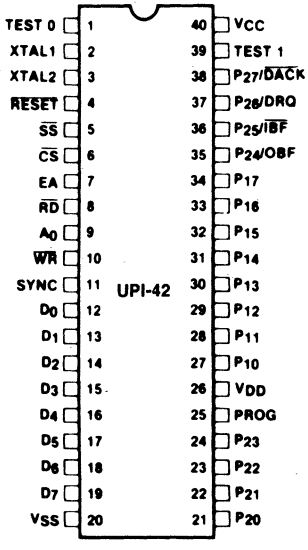
On the rising edge of SYNC and EA is enabled, port data is valid and can be strobed. On the trailing edge of sync the program counter contents are available.

8742
UNIVERSAL PERIPHERAL INTERFACE 8-BIT SLAVE MICROCONTROLLER

- **8742: 12 MHz**
- **Pin, Software and Architecturally Compatible with 8741A**
- **8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package**
- **2048 x 8 EPROM, 128 x 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins**
- **One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface**
- **DMA, Interrupt, or Polled Operation Supported**
- **Fully Compatible with all Intel and Most Other Microprocessor Families**
- **Expandable I/O**
- **RAM Power-Down Capability**
- **Over 90 Instructions: 70% Single Byte**
- **Available in EXPRESS — Standard Temperature Range**

The Intel 8742 is a general-purpose Universal Peripheral Interface that allows designers to grow their own customized solution for peripheral device control. It contains a low-cost microcomputer with 2K of program memory, 128 bytes of data memory, 8-bit timer/counter, and clock generator in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in the MCS®-48, MCS-51, MCS-80, MCS-85, 8088, 8086 and other 8-, 16-bit systems.

The 8742 is software, pin, and architecturally compatible with the 8741A. The 8742 doubles the on-chip memory space to allow for additional features and performance to be incorporated in upgraded 8741A designs. For new designs, the additional memory and performance of the 8742 extends the UPI concept to more complex motor control tasks, 80-column printers and process control applications as examples.



290256-2

Figure 1. Pin Configuration

November 1991
Order Number: 290256-001

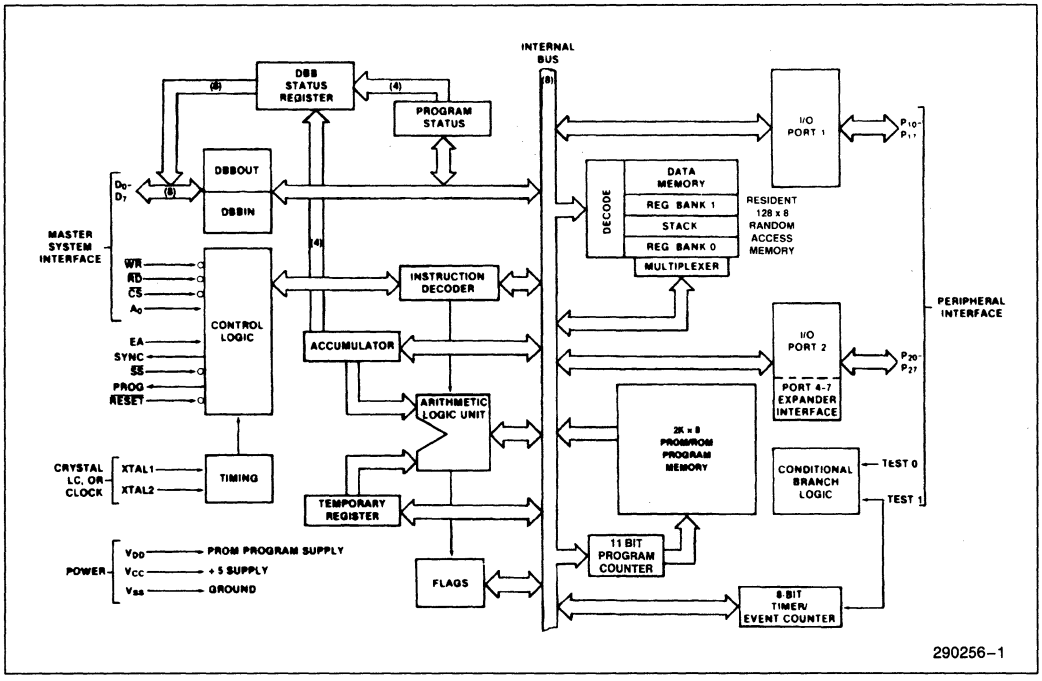


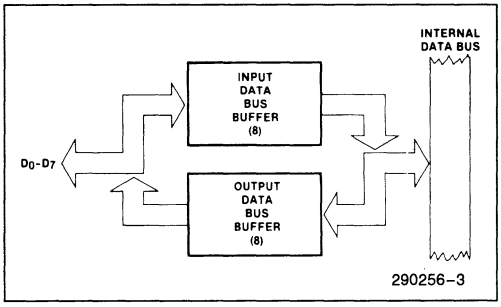
Figure 2. Block Diagram

Table 1. Pin Description

Symbol	DIP Pin No.	Type	Name and Function
TEST 0, TEST 1	1 39	I	**TEST INPUTS:** Input pins which can be directly tested using conditional branch instructions. **FREQUENCY REFERENCE:** TEST 1 (T_1) also functions as the event timer input (under software control). TEST 0 (T_0) is used during PROM programming and EPROM verification.
XTAL 1, XTAL 2	2 3	I	**INPUTS:** Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
$\overline{\text{RESET}}$	4	I	**RESET:** Input used to reset status flip-flops and to set the program counter to zero. $\overline{\text{RESET}}$ is also used during EPROM programming and verification.
$\overline{\text{SS}}$	5	I	**SINGLE STEP:** Single step input used in conjunction with the SYNC output to step the program through each instruction (EPROM). This should be tied to +5V when not used.
$\overline{\text{CS}}$	6	I	**CHIP SELECT:** Chip select input used to select one UPI microcomputer out of several connected to a common data bus.
EA	7	I	**EXTERNAL ACCESS:** External access input which allows emulation, testing and EPROM verification. This pin should be tied low if unused.
$\overline{\text{RD}}$	8	I	**READ:** I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
A_0	9	I	**COMMAND/DATA SELECT:** Address Input used by the master processor to indicate whether byte transfer is data (A_0 = 0, F1 is reset) or command (A_0 = 1, F1 is set). A_0 = 0 during program and verify operations.
$\overline{\text{WR}}$	10	I	**WRITE:** I/O write input which enables the master CPU to write data and command words to the UPI INPUT DATA BUS BUFFER.
SYNC	11	O	**OUTPUT CLOCK:** Output signal which occurs once per UPI instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
D_0–D_7 (BUS)	12–19	I/O	**DATA BUS:** Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI microcomputer to an 8-bit master system data bus.
P_{10}–P_{17}	27–34	I/O	**PORT 1:** 8-bit, PORT 1 quasi-bidirectional I/O lines.
P_{20}–P_{27}	21–24 35–38	I/O	**PORT 2:** 8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P_{20}–P_{23}) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4–7 access. The upper 4 bits (P_{24}–P_{27}) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P_{24} as Output Buffer Full ($\overline{\text{OBF}}$) interrupt, P_{25} as Input Buffer Full ($\overline{\text{IBF}}$) interrupt, P_{26} as DMA Request (DRQ), and P_{27} as DMA ACKnowledge ($\overline{\text{DACK}}$).
PROG	25	I/O	**PROGRAM:** Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243. This pin should be tied high if unused.
V_{CC}	40		**POWER:** +5V main power supply pin.
V_{DD}	26		**POWER:** +5V during normal operation. +21V during programming operation. Low power standby supply pin.
V_{SS}	20		**GROUND:** Circuit ground potential.

UPI-42 FEATURES

1. Two Data Bus Buffers, one for input and one for output. This allows a much cleaner Master/Slave protocol.



2. 8 Bits of Status

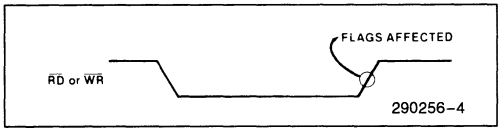
ST_7	ST_6	ST_5	ST_4	F_1	F_0	IBF	OBF
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

ST_4–ST_7 are user definable status bits. These bits are defined by the "MOV STS, A" single byte, single cycle instruction. Bits 4–7 of the acccumulator are moved to bits 4–7 of the status register. Bits 0–3 of the status register are not affected.

MOV STS, A Op Code: 90H

1	0	0	1	0	0	0	0
D_7							D_0

3. $\overline{RD}$ and $\overline{WR}$ are edge triggered. IBF, OBF, F_1 and $\overline{INT}$ change internally after the trailing edge of $\overline{RD}$ or $\overline{WR}$.

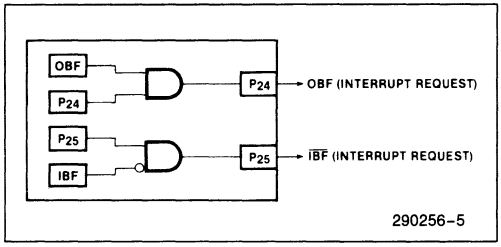


During the time that the host CPU is reading the status register, the 8742 is prevented from updating this register or is "locked out".

4. P_{24} and P_{25} are port pins or Buffer Flag pins which can be used to interrupt a master processor. These pins default to port pins on Reset.

If the "EN FLAGS" instruction has been executed, P_{24} becomes the OBF (Output Buffer Full) pin. A "1" written to P_{24} enables the OBF pin (the pin outputs the OBF Status Bit). A "0" written to P_{24} disables the OBF pin (the pin remains low). This pin can be used to indicate that valid data is available from the UPI-41A (in Output Data Bus Buffer).

If "EN FLAGS" has been executed, P_{25} becomes the $\overline{IBF}$ (Input Buffer Full) pin. A "1" written to P_{25} enables the $\overline{IBF}$ pin (the pin outputs the inverse of the IBF Status Bit. A "0" written to P_{25} disables the $\overline{IBF}$ pin (the pin remains low). This pin can be used to indicate that the UPI is ready for data.



Data Bus Buffer Interrupt Capability

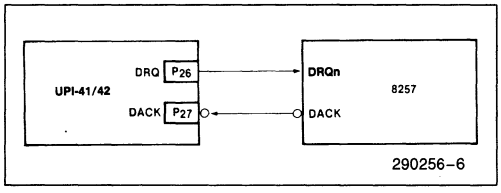
EN FLAGS Op Code: 0F5H

1	1	1	1	0	1	0	1
D_7							D_0

5. P_{26} and P_{27} are port pins or DMA handshake pins for use with a DMA controller. These pins default to port pins on Reset.

If the "EN DMA" instruction has been executed, P_{26} becomes the DRQ (DMA Request) pin. A "1" written to P_{26} causes a DMA request (DRQ is activated). DRQ is deactivated by DACK•RD, DACK•WR, or execution of the "EN DMA" instruction.

If "EN DMA" has been executed, P_{27} becomes the $\overline{DACK}$ (DMA Acknowledge) pin. This pin acts as a chip select input for the Data Bus Buffer registers during DMA transfers.



DMA Handshake Capability

EN DMA Op Code: 0E5H

1	1	1	0	0	1	0	1
D_7							D_0

6. The RESET input on the 8742, includes a 2-stage synchronizer to support reliable reset operation for 12 MHz operation.

7. When EA is enabled on the 8742, the program counter is placed on Port 1 and the lower three bits of Port 2 (MSB = P_{22}, LSB = P_{10}). On the 8742 this information is multiplexed with PORT DATA (see port timing diagrams at end of this data sheet).

APPLICATIONS

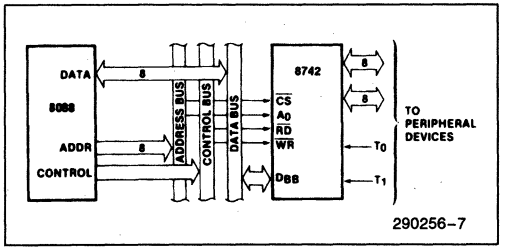


Figure 3. 8088-8742 Interface

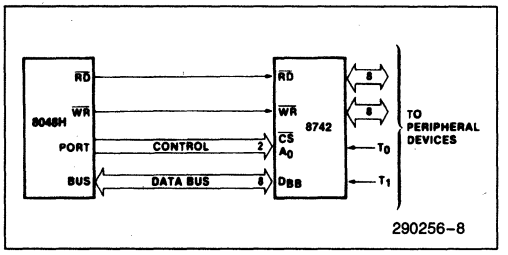


Figure 4. 8048H-8742 Interface

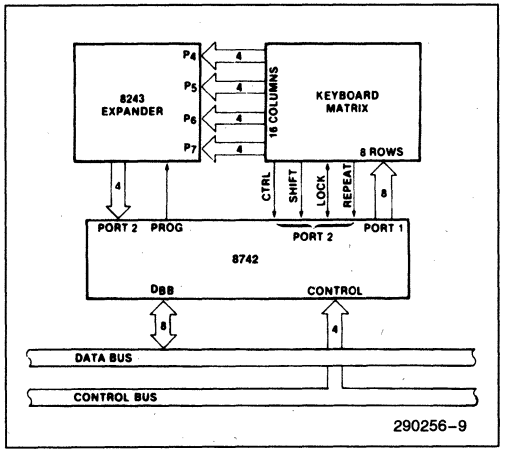


Figure 5. 8742-8243 Keyboard Scanner

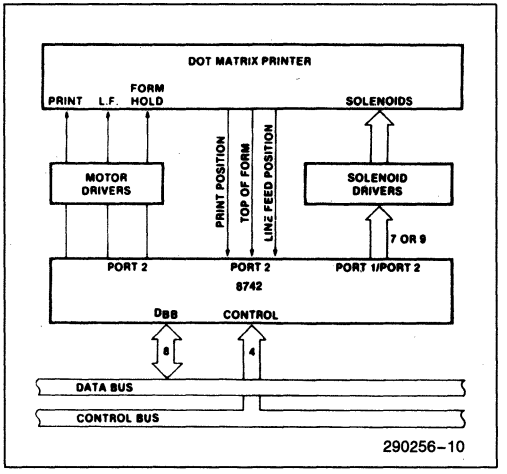


Figure 6. 8742 80-Column Matrix Printer Interface

PROGRAMMING, VERIFYING, AND ERASING THE 8742 EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock-Input
$\overline{\text{Reset}}$	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input Data Output During Verify
P_{20-12}	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING
An attempt to program a missocketed 8742 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. A_0 = 0V, CS = 5V, EA = 5V, RESET = 0V, TESTO = 5V, V_{DD} = 5V, clock applied or internal oscillator operating, BUS floating, PROG = 5V.
2. Insert 8742 in programming socket
3. TEST 0 = 0V (select program mode)
4. EA = 18V (active program mode)
5. Address applied to BUS and P_{20-22}
6. $\overline{\text{RESET}}$ = 5V (latch address)
7. Data applied to BUS**
8. V_{DD} = 21V (programming power)
9. PROG = V_{CC} followed by one 50 ms pulse to 18V
10. V_{DD} = 5V
11. TEST 0 = 5V (verify mode)
12. Read and verify data on BUS
13. TEST 0 = 0V
14. $\overline{\text{RESET}}$ = 0V and repeat from step 5
15. Programmer should be at conditions of step 1 when 8742 is removed from socket

8742 Erasure Characteristics

The erasure characteristics of the 8742 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 8742 in approximately 3 years while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 8742 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8742 window to prevent unintentional erasure.

The recommended erasure procedure for the 8742 is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 w-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The 8742 should be placed within one inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin With Respect to Ground .....−0.5 to +7V
Power Dissipation.....1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0° to +70°C, V_{CC} = V_{DD} = +5V ±10%

Symbol	Parameter	8742		Units	Test Conditions
		Min	Max		
V_{IL}	Input Low Voltage (Except XTAL1, XTAL2, RESET)	−0.5	0.8	V	
V_{IL1}	Input Low Voltage (XTAL1, XTAL2, RESET)	−0.5	0.6	V	
V_{IH}	Input High Voltage (Except XTAL1, XTAL2, RESET)	2.0	V_{CC}	V	
V_{IH1}	Input High Voltage (XTLA1, XTAL2, RESET)	3.5	V_{CC}	V	
V_{OL}	Output Low Voltage (D_0–D_7)		0.45	V	I_{OL} = 2.0 mA
V_{OL1}	Output Low Voltage (P_{10}–P_{17}, P_{20}–P_{27}, Sync)		0.45	V	I_{OL} = 1.6 mA
V_{OL2}	Output Low Voltage (PROG)		0.45	V	I_{OL} = 1.0 mA
V_{OH}	Output High Voltage (D_0–D_7)	2.4		V	I_{OH} = −400 µA
V_{OH1}	Output High Voltage (All Other Outupts)	2.4			I_{OH} = −50 µA
I_{IL}	Input Leakage Current (T_0, T_1, RD, WR, CS, A_0, EA)		±10	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OFL}	Output Leakage Current (D_0–D_7, High Z State)		±10	µA	V_{SS} +0.45 $\le V_{OUT} \le V_{CC}$
I_{LI}	Low Input Load Current (P_{10}–P_{17}, P_{20}–P_{27})		0.3	mA	V_{IL} = 0.8V
I_{LI1}	Low Input Load Current (RESET, SS)		0.2	mA	V_{IL} = 0.8V
I_{DD}	V_{DD} Supply Current		10	mA	Typical = 5 mA
I_{CC} + I_{DD}	Total Supply Current		125	mA	Typical = 60 mA
I_{IH}	Input Leakage Current (P_{10}–P_{17}, P_{20}–P_{27})		100	µA	V_{IN} = V_{CC}
C_{IN}	Input Capacitance		10	pF	
C_{10}	I/O Capacitance		20	pF	

D.C. CHARACTERISTICS—PROGRAMMING

T_A = 25°C ±5°C, V_{CC} = 5V ±5%, V_{DD} = 21V ±0.5V

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{DOH}	V_{DD} Program Voltage High Level	20.5	21.5	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	17.5	18.5	V	
V_{PL}	PROG Voltage Low Level	V_{CC}−0.5	V_{CC}	V	
V_{EAH}	EA Program or Verify Voltage High Level	17.5	18.5	V	
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		1.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{SS} = 0V$, $V_{CC} = V_{DD} = +5V \pm 10\%$

DBB READ

Symbol	Parameter	8742		Units
		Min	Max	
t_{AR}	CS, A_0 Setup to RD ↓	0		ns
t_{RA}	CS, A_0 Hold after RD ↑	0		ns
t_{RR}	RD Pulse Width	160		ns
t_{AD}	CS, A_0 to Data Out Delay		130	ns
t_{RD}	RD ↓ to Data Out Delay		130	ns
t_{DF}	RD ↑ to Data Float Delay		85	ns
t_{CY}	Cycle Time	1.25	15	μs(1)

DBB WRITE

Symbol	Parameter	Min	Max	Units
t_{AW}	CS, A_0 Setup to WR ↓	0		ns
t_{WA}	CS, A_0 Hold after WR ↑	0		ns
t_{WW}	WR Pulse Width	160		ns
t_{DW}	Data Setup to WR ↑	130		ns
t_{WD}	Data Hold after WR ↑	0		ns

NOTE:
1. $T_{CY} = 15/f(XTAL)$

A.C. CHARACTERISTICS $T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = +21V \pm 0.5$

PROGRAMMING

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	Address Setup Time to RESET ↑	$4t_{CY}$			
t_{WA}	Address Hold Time after RESET ↑	$4t_{CY}$			
t_{DW}	Data in Setup Time to PROG ↑	$4t_{CY}$			
t_{WD}	Data in Hold Time after PROG ↓	$4t_{CY}$			
t_{PH}	RESET Hold Time to Verify	$4t_{CY}$			
t_{VDDW}	V_{DD} Setup Time to PROG ↑	0	1.0	mS	
t_{VDDH}	V_{DD} Hold Time after PROG ↑	0	1.0	mS	
t_{PW}	Program Pulse Width	50	60	mS	
t_{TW}	Test 0 Setup Time for Program Mode	$4t_{CY}$			
t_{WT}	Test 0 Hold Time after Program Mode	$4t_{CY}$			
t_{DO}	Test 0 to Data Out Delay		$4t_{CY}$		
t_{WW}	RESET Pulse Width to Latch Address	$4t_{CY}$			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	4.0		μs	
t_{RE}	RESET Setup Time before EA ↑	$4t_{CY}$			

NOTE:
If TEST 0 is high, t_{DO} can be triggered by RESET ↑.

A.C. CHARACTERISTICS DMA

Symbol	Parameter	8642/8742		Units
		Min	Max	
t_{ACC}	DACK to WR or RD	0		ns
t_{CAC}	RD or WR to DACK	0		ns
t_{ACD}	DACK to Data Valid		130	ns
t_{CRQ}	RD or WR to DRQ Cleared		100	ns(1)

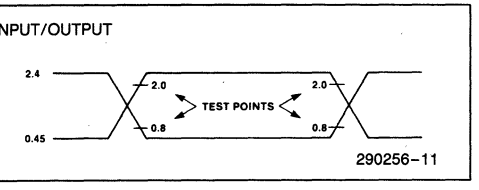
NOTE:
1. C_L = 150 pF.

A.C. CHARACTERISTICS PORT 2 T_A = 0°C to +70°C, V_{CC} = +5V ±10%

Symbol	Parameter	f(t_{CY})	8742/8642(3)		Units
			Min	Max	
t_{CP}	Port Control Setup before Falling Edge of PROG	1/15 t_{CY} − 28	55		ns(1)
t_{PC}	Port Control Hold after Falling Edge of PROG	1/10 t_{CY}	125		ns(2)
t_{PR}	PROG to Time P2 Input Must Be Valid	8/15 t_{CY} − 16		650	ns(1)
t_{PF}	Input Data Hold Time		0	150	ns(2)
t_{DP}	Output Data Setup Time	2/10 t_{CY}	250		ns(1)
t_{PD}	Output Data Hold Time	1/10 t_{CY} − 80	45		ns(2)
t_{PP}	PROG Pulse Width	6/10 t_{CY}	750		ns

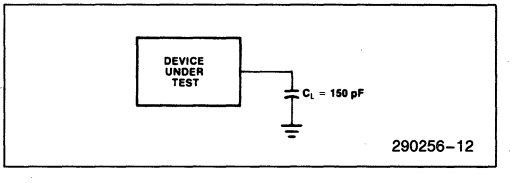
NOTES:
1. C_L = 80 pF.
2. C_L = 20 pF.
3. t_{CY} = 1.25 μs.

A.C. TESTING INPUT/OUTPUT WAVEFORM



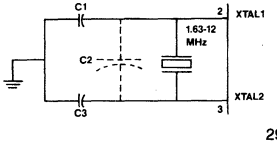
290256-11

A.C. TESTING LOAD CIRCUIT



290256-12

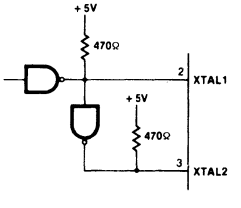
CRYSTAL OSCILLATOR MODE



290256-13

Crystal Series Resistance Should be <750 at 12 MHz; <180Ω at 3.6 MHz.

DRIVING FROM EXTERNAL SOURCE

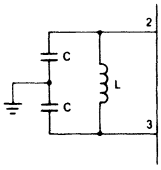


290256-14

Rise and Fall Times Should Not Exceed 20 ns. Resistors to V_{CC} are Needed to Ensure V_{IH} = 3.5V if TTL Circuitry is Used.

LC OSCILLATOR MODE

L	C	NOMINAL
45 H	20 pF	5.2 MHz
120 H	20 pF	3.2 MHz



$$f = \frac{1}{2\pi\sqrt{LC'}}$$

$$C' = \frac{C + 3Cpp}{2}$$

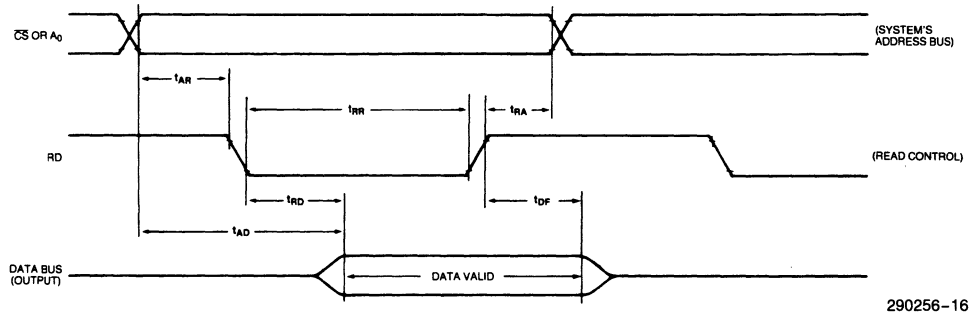
Cpp ≅ 5 pF–10 pF
Pin-to-Pin Capacitance

290256–15

Each C Should be Approximately 20 pF, including Stray Capacitance.

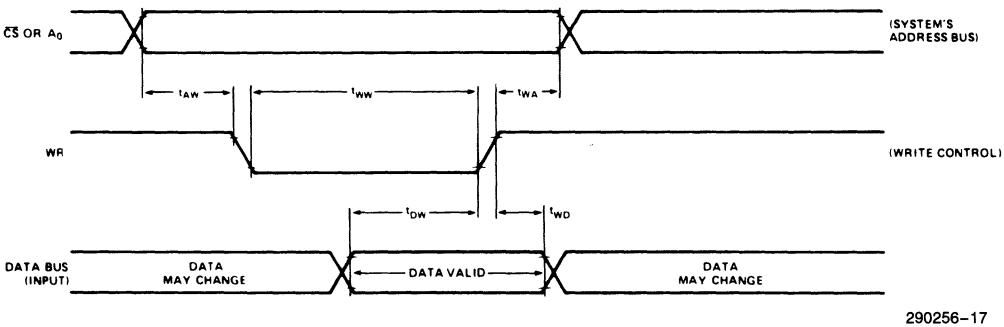
WAVEFORMS

READ OPERATION—DATA BUS BUFFER REGISTER



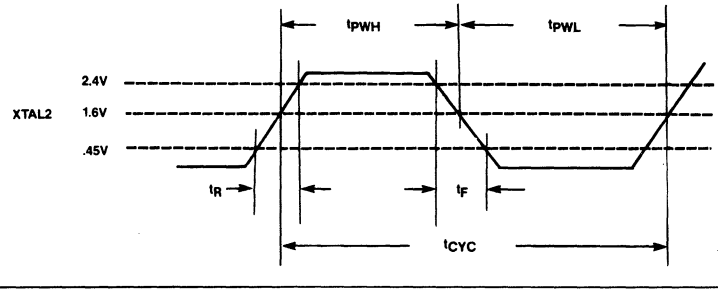
290256–16

WRITE OPERATION—DATA BUS BUFFER REGISTER



290256–17

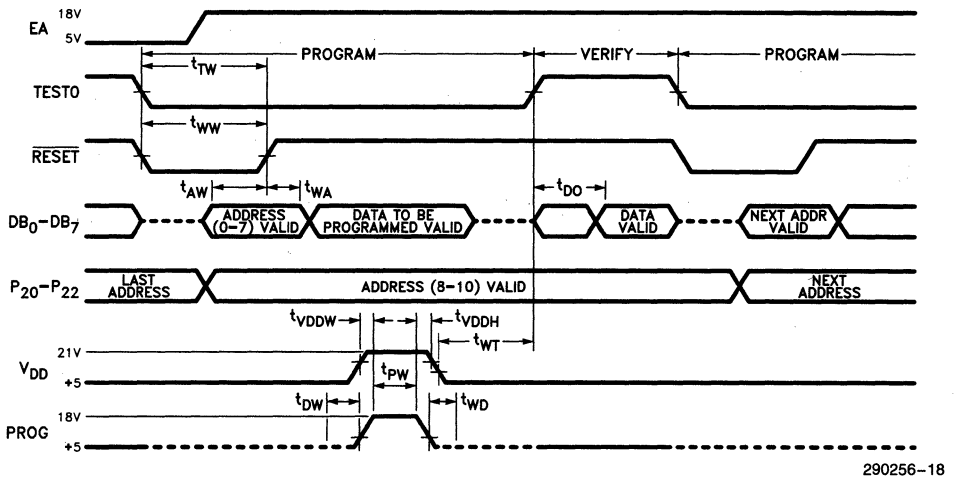
CLOCK TIMING



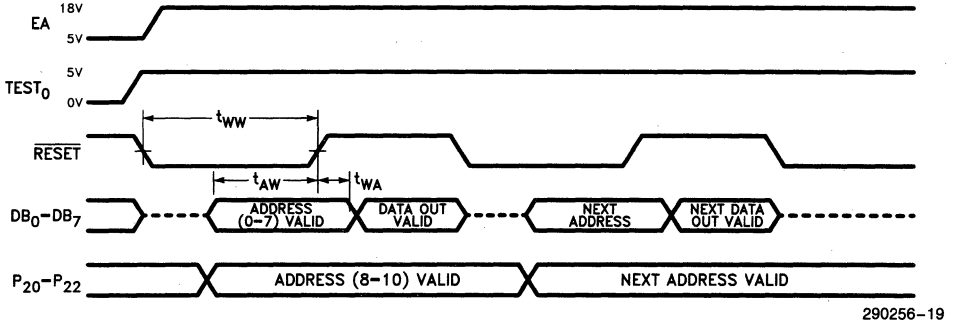
290256–23

WAVEFORMS

COMBINATION PROGRAM/VERIFY MODE



VERIFY MODE



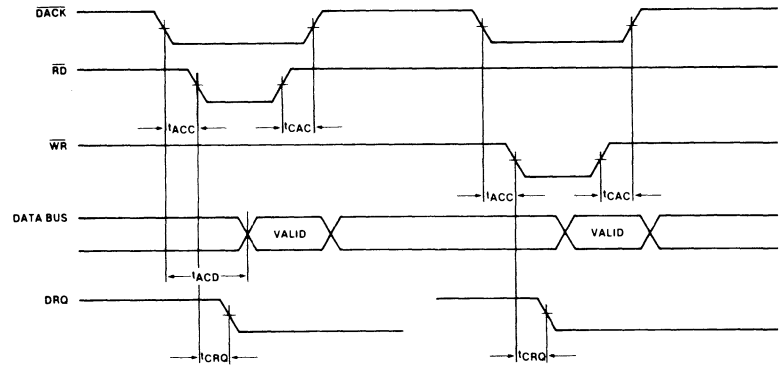
NOTES:
1. PROG must float if EA is low or EA is low or if $TEST_0$ = 5V.
2. A_0 must be held low (i.e., = 0V) during program/verify modes.
3. Test 0 must be held high.

The 8742 EPROM can be programmed by the following Intel products:

1. Universal PROM Programmer (UPP 103) peripheral of the Intellec Development System with a UPP-549 Personality Card.
2. iUP-200/iUP-201 PROM Programmer with the iUP-F87/44 Personality Module.

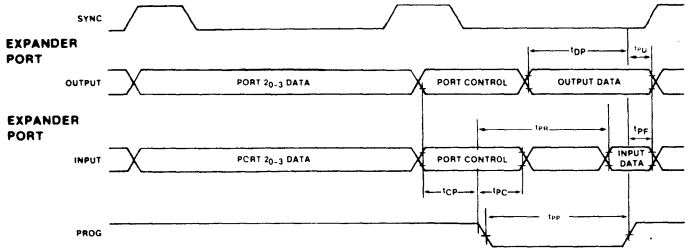
WAVEFORMS (Continued)

DMA



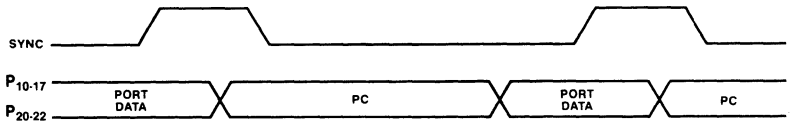
290256-20

PORT 2



290256-21

PORT TIMING DURING EXTERNAL ACCESS (EA)



290256-22

On the Rising Edge of SYNC and EA is Enabled, Port Data is Valid and can be Strobed on the Trailing Edge of Sync the Program Counter Contents are Available.

UPI-C42/UPI-L42
UNIVERSAL PERIPHERAL INTERFACE
CHMOS 8-BIT SLAVE MICROCONTROLLER

- **Pin, Software and Architecturally Compatible with all UPI-41 and UPI-42 Products**
- **Low Voltage Operation with the UPI-L42**
  — Full 3.3V Support
- **Integrated Auto A20 Gate Support**
- **Suspend Power Down Mode**
- **Security Bit Code Protection Support**
- **8-Bit CPU plus ROM/OTP EPROM, RAM, I/O, Timer/Counter and Clock in a Single Package**
- **4096 x 8 ROM/OTP, 256 x 8 RAM 8-Bit Timer/Counter, 18 Programmable I/O Pins**
- **DMA, Interrupt, or Polled Operation Supported**
- **One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface**
- **Fully Compatible with all Intel and Most Other Microprocessor Families**
- **Interchangeable ROM and OTP EPROM Versions**
- **Expandable I/O**
- **Sync Mode Available**
- **Over 90 Instructions: 70% Single Byte**
- **Quick Pulse Programming Algorithm**
  — Fast OTP Programming
- **Available in 40-Lead Plastic, 44-Lead Plastic Leaded Chip Carrier, and 44-Lead Quad Flat Pack Packages**
  (See Packaging Spec., Order #240800, Package Type P, N, and S)

The UPI-C42 is an enhanced CHMOS version of the industry standard Intel UPI-42 family. It is fabricated on Intel's CHMOS III-E process. The UPI-C42 is pin, software, and architecturally compatible with the NMOS UPI family. The UPI-C42 has all of the same features of the NMOS family plus a larger user programmable memory array (4K), integrated auto A20 gate support, and lower power consumption inherent to a CHMOS product.

The UPI-L42 offers the same functionality and socket compatibility as the UPI-C42 as well as providing low voltage 3.3V operation.

The UPI-C42 is essentially a "slave" microcontroller, or a microcontroller with a slave interface included on the chip. Interface registers are included to enable the UPI device to function as a slave peripheral controller in the MCS Modules and iAPX family, as well as other 8-, 16-, and 32-bit systems.

To allow full user flexibility, the program memory is available in ROM and One-Time Programmable EPROM (OTP).

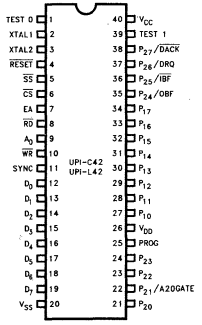


Figure 1. DIP Pin Configuration

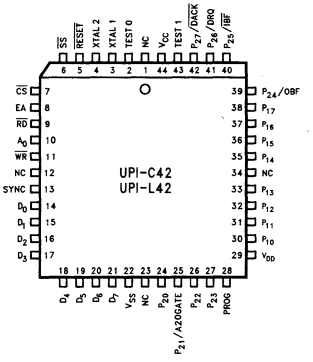


Figure 2. PLCC Pin Configuration

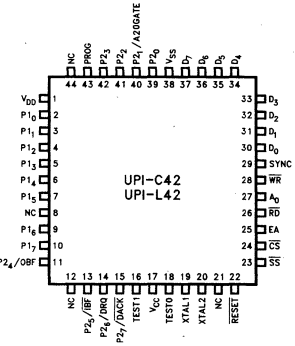


Figure 3. QFP Pin Configuration

October 1994
Order Number: 290414-003

Table 1. Pin Description

Symbol	DIP Pin No.	PLCC Pin No.	QFP Pin No.	Type	Name and Function
TEST 0, TEST 1	1 39	2 43	18 16	I	**TEST INPUTS:** Input pins which can be directly tested using conditional branch instructions. **FREQUENCY REFERENCE:** TEST 1 (T_1) functions as the event timer input (under software control) and during the STANDBY power down mode, as a method of resuming normal operation. TEST 0 (T_0) is a multi-function pin used during PROM programming and ROM/EPROM verification, during Sync Mode to reset the instruction state to S1 and synchronize the internal clock to PH1, and during the STANDBY power down mode, as a method of resuming normal operation (see Powerdown section).
XTAL 1	2	3	19	O	**OUTPUT:** Output from the oscillator amplifier.
XTAL 2	3	4	20	I	**INPUT:** Input to the oscillator amplifier and internal clock generator circuits.
$\overline{\text{RESET}}$	4	5	22	I	**RESET:** Input used to reset status flip-flops, set the program counter to zero, and force the UPI-C42 from the suspend power down mode. $\overline{\text{RESET}}$ is also used during EPROM programming and verification.
$\overline{\text{SS}}$	5	6	23	I	**SINGLE STEP:** Single step input used in conjunction with the SYNC output to step the program through each instruction (EPROM). This should be tied to +5V when not used. This pin is also used to put the device in Sync Mode by applying 12.5V to it.
$\overline{\text{CS}}$	6	7	24	I	**CHIP SELECT:** Chip select input used to select one UPI microcomputer out of several connected to a common data bus.
EA	7	8	25	I	**EXTERNAL ACCESS:** External access input which allows emulation, testing and ROM/EPROM verification. This pin should be tied low if unused.
$\overline{\text{RD}}$	8	9	26	I	**READ:** I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
A_0	9	10	27	I	**COMMAND/DATA SELECT:** Address Input used by the master processor to indicate whether byte transfer is data (A_0 = 0, F1 is reset) or command (A_0 = 1, F1 is set). A_0 = 0 during program and verify operations.
$\overline{\text{WR}}$	10	11	28	I	**WRITE:** I/O write input which enables the master CPU to write data and command words to the UPI INPUT DATA BUS BUFFER.
SYNC	11	13	29	O	**OUTPUT CLOCK:** Output signal which occurs once per UPI instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
D_0–D_7 (BUS)	12–19	14–21	30–37	I/O	**DATA BUS:** Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI microcomputer to an 8-bit master system data bus.
P_{10}–P_{17}	27–34	30–33 35–38	2–10	I/O	**PORT 1:** 8-bit, PORT 1 quasi-bidirectional I/O lines. P_{10}–P_{17} access the signature row and security bit.

4

Table 1. Pin Description (Continued)

Symbol	DIP Pin No.	PLCC Pin No.	QFP Pin No.	Type	Name and Function
P_{20}–P_{27}	21–24 35–38	24–27 39–42	39–42 11, 13–15	I/O	**PORT 2:** 8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P_{20}–P_{23}) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4–7 access. P_{21} can be programmed to provide Auto A20 Gate support. The upper 4 bits (P_{24}–P_{27}) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P_{24} as Output Buffer Full (OBF) interrupt, P_{25} as Input Buffer Full ($\overline{IBF}$) interrupt, P_{26} as DMA Request (DRQ), and P_{27} as DMA ACKnowledge ($\overline{DACK}$).
PROG	25	28	43	I/O	**PROGRAM:** Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243. This pin should be tied high if unused.
V_{CC}	40	44	17		**POWER:** +5V main power supply pin.
V_{DD}	26	29	1		**POWER:** +5V during normal operation. +12.75V during programming operation. Low power standby supply pin.
V_{SS}	20	22	38		**GROUND:** Circuit ground potential.

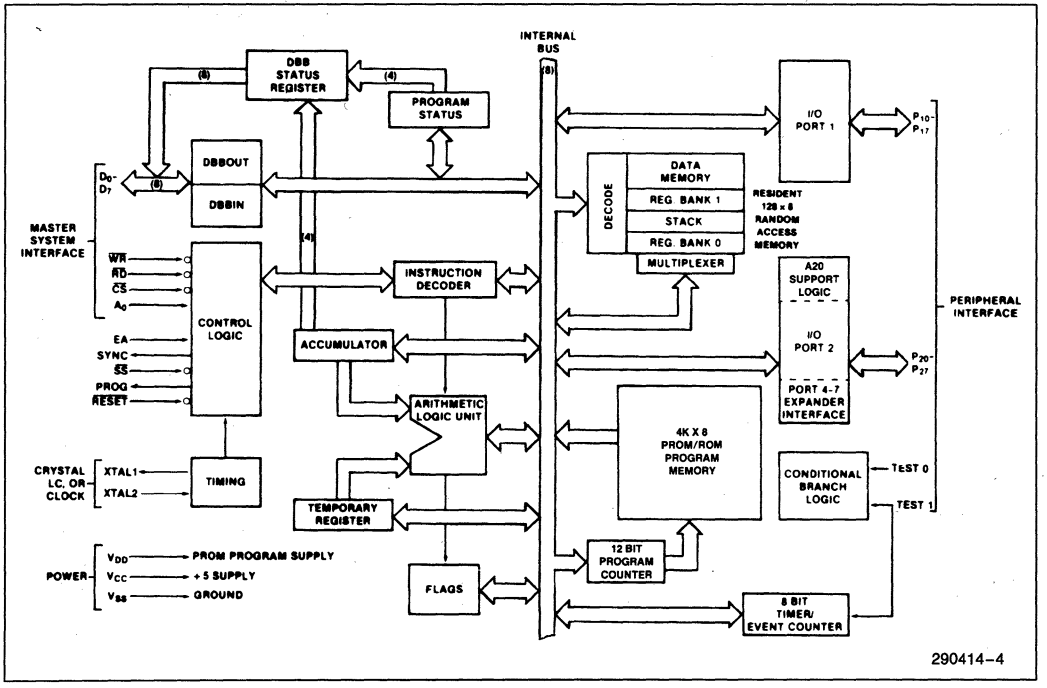


Figure 4. Block Diagram

UPI-C42/L42 PRODUCT SELECTION GUIDE

UPI-C42: Low power CHMOS version of the UPI-42.

Device	Package	ROM	OTP	Comments
80C42	N, P S	4K		ROM Device
82C42PC	N, P, S			Phoenix MultiKey/42 firmware, PS/2 style mouse support
82C42PD	N, P, S			Phoenix MultiKey/42L firmware, KBC and SCC for portable apps.
82C42PE	N, P, S			Phoenix MultiKey/42G firmware, Energy Efficient KBC solution
87C42	N, P, S		4K	One Time Programmable Version

UPI-L42: The low voltage 3.3V version of the UPI-C42.

Device	Package	ROM	OTP	Comments
80L42	N, P S	4K		ROM Device
82L42PC	N, P, S			Phoenix MultiKey/42 firmware, PS/2 style mouse support
82L42PD	N, P, S			Phoenix MultiKey/42L firmware, KBC and SCC for portable apps.
87L42	N, P, S		4K	One Time Programmable Version

N = 44 lead PLCC, P = 40 lead PDIP, S = 44 lead QFP, D = 40 lead CERDIP
KBC = Key Board Control, SCC = Scan Code Control

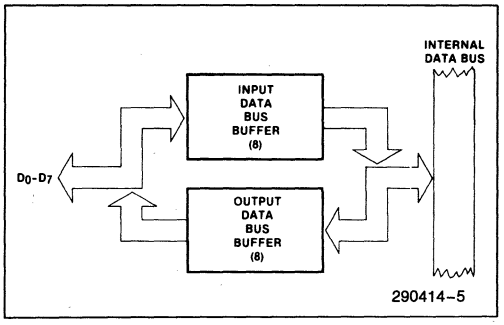
THE INTEL 82C42

As shown in the UPI-C42 product matrix, the UPI-C42 is offered as a pre-programmed 80C42 with various versions of MultiKey/42 keyboard controller firmware developed by Phoenix Technologies Ltd.

The 82C42PC provides a low powered solution for industry standard keyboard and PS/2 style mouse control. The 82C42PD provides a cost effective means for keyboard and scan code control for notebook platforms. The 82C42PE allows a quick time to market, low cost solution for energy efficient desktop designs.

UPI-42 COMPATIBLE FEATURES

1. Two Data Bus Buffers, one for input and one for output. This allows a much cleaner Master/Slave protocol.



2. 8 Bits of Status

ST_7	ST_6	ST_5	ST_4	F_1	F_0	IBF	OBF
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

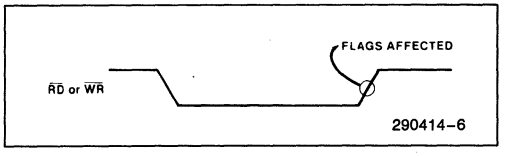
ST_4–ST_7 are user definable status bits. These bits are defined by the "MOV STS, A" single byte, single cycle instruction. Bits 4–7 of the acccumulator are moved to bits 4–7 of the status register. Bits 0–3 of the status register are not affected.

MOV STS, A Op Code: 90H

1	0	0	1	0	0	0	0
D_7							D_0

3. $\overline{RD}$ and $\overline{WR}$ are edge triggered. IBF, OBF, F_1 and INT change internally after the trailing edge of $\overline{RD}$ or $\overline{WR}$.

   During the time that the host CPU is reading the status register, the UPI is prevented from updating this register or is 'locked out.'

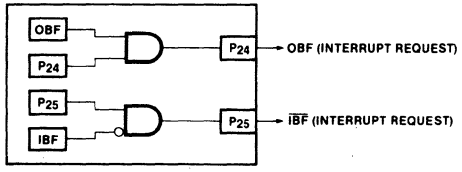


4. P_{24} and P_{25} are port pins or Buffer Flag pins which can be used to interrupt a master processor. These pins default to port pins on Reset.

   If the "EN FLAGS" instruction has been executed, P_{24} becomes the OBF (Output Buffer Full) pin. A "1" written to P_{24} enables the OBF pin (the pin outputs the OBF Status Bit). A "0" written to P_{24} disables the OBF pin (the pin remains low). This pin can be used to indicate that valid data is available from the UPI (in Output Data Bus Buffer).

   If "EN FLAGS" has been executed, P_{25} becomes the $\overline{IBF}$ (Input Buffer Full) pin. A "1" written to P_{25} enables the $\overline{IBF}$ pin (the pin outputs the inverse of the IBF Status Bit. A "0" written to P_{25} disables the $\overline{IBF}$ pin (the pin remains low). This pin can be used to indicate that the UPI is ready for data.

Data Bus Buffer Interrupt Capability



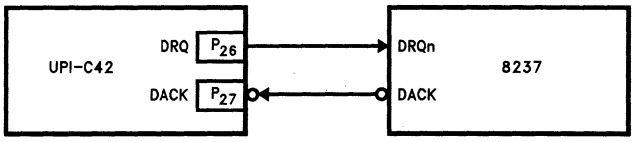
EN FLAGS Op Code: 0F5H

1	1	1	1	0	1	0	1
D_7							D_0

5. P_{26} and P_{27} are port pins or DMA handshake pins for use with a DMA controller. These pins default to port pins on Reset.

   If the "EN DMA" instruction has been executed, P_{26} becomes the DRQ (DMA Request) pin. A "1" written to P_{26} causes a DMA request (DRQ is activated). DRQ is deactivated by DACK•RD, DACK•WR, or execution of the "EN DMA" instruction.

DMA Handshake Capability



If "EN DMA" has been executed, P_{27} becomes the $\overline{DACK}$ (DMA ACKnowledge) pin. This pin acts as a chip select input for the Data Bus Buffer registers during DMA transfers.

EN DMA Op Code: 0E5H

1	1	1	0	0	1	0	1

D_7 D_0

6. When EA is enabled on the UPI, the program counter is placed on Port 1 and the lower four bits of Port 2 (MSB = P_{23}, LSB = P_{10}). On the UPI this information is multiplexed with PORT DATA (see port timing diagrams at end of this data sheet).
7. The UPI-C42 supports the Quick Pulse Programming Algorithm, but can also be programmed with the Intelligent Programming Algorithm. (See the Programming Section.)

UPI-C42 FEATURES

Programmable Memory Size Increase

The user programmable memory on the UPI-C42 will be increased from the 2K available in the NMOS product by 2X to 4K. The larger user programmable memory array will allow the user to develop more complex peripheral control micro-code. P2.3 (port 2 bit 3) has been designated as the extra address pin required to support the programming of the extra 2K of user programmable memory.

The new instruction SEL PMB1 (73h) allows for access to the upper 2K bank (locations 2048–4095). The additional memory is completely transparent to users not wishing to take advantage of the extra memory space. No new commands are required to access the lower 2K bytes. The SEL PMB0 (63h) has also been added to the UPI-C42 instruction set to allow for switching between memory banks.

Extended Memory Program Addressing (Beyond 2K)

For programs of 2K words or less, the UPI-C42 addresses program memory in the conventional manner. Addresses beyond 2047 can be reached by executing a program memory bank switch instruction (SEL PMB0, SEL PMB1) followed by a branch instruction (JMP or CALL). The bank switch feature extends the range of branch instructions beyond their normal 2K range and at the same time prevents the user from inadvertently crossing the 2K boundary.

PROGRAM MEMORY BANK SWITCH

The switching of 2K program memory banks is accomplished by directly setting or resetting the most significant bit of the program counter (bit 11); see Figure 5. Bit 11 is not altered by normal incrementing of the program counter, but is loaded with the contents of a special flip-flop each time a JMP or CALL instruction is executed. This special flip-flop is set by executing an SEL PMB1 instruction and reset by SEL PMB0. Therefore, the SEL PMB instruction may be executed at any time prior to the actual bank switch which occurs during the next branch instruction encountered. Since all twelve bits of the program counter, including bit 11, are stored in the stack, when a Call is executed, the user may jump to subroutines across the 2K boundary and the proper PC will be restored upon return. However, the bank switch flip-flop will not be altered on return.

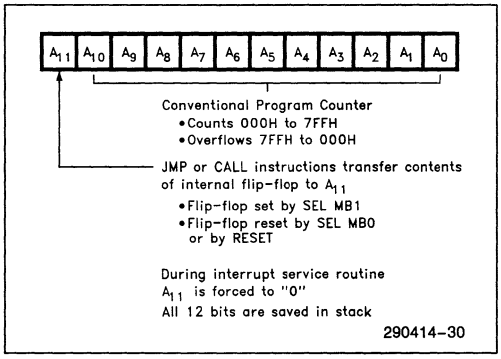


Figure 5. Program Counter

INTERRUPT ROUTINES

Interrupts always vector the program counter to location 3 or 7 in the first 2K bank, and bit 11 of the program counter is held at "0" during the interrupt service routine. The end of the service routine is signaled by the execution of an RETR instruction. Interrupt service routines should therefore be contained entirely in the lower 2K words of program memory. The execution of a SEL PMB0 or SEL PMB1 instruction within an interrupt routine is not recommended since it will not alter PC11 while in the routine, but will change the internal flip-flop.

Automatic A20 Gate Support

This feature has been provided to enhance the performance of the UPI-C42 when being used in a keyboard controller application. The UPI-C42 design has included on chip logic to support a hardware GATEA20 feature. This feature is enabled by the A20EN instruction and remains enabled until the de-

vice is reset. It is important to note that the execution of the A20EN instruction redefines Port 2, bit 1 as a pure output pin with read only characteristics. The state of this pin can be modified only through a valid "D1" command sequence (see Table 1). Once enabled, the A20 logic will process a "D1" command sequence (write to output port) by setting/resetting the A20 bit on port 2, bit 1 (P2.1) without requiring service from the internal CPU. The host can directly control the status of the A20 bit. At no time during this host interface transaction will the IBF flag in the status register be activated. If the A20EN instruction is not issued, the UPI-C42 treats the "D1" command like any other command/data sequence. The on chip GATEA20 logic will ignore all GATEA20 command/data sequences. Table 1 gives several possible GATEA20 command/data sequences and UPI-C42 responses.

Table 1. D1 Command Sequences

A0	R/W	DB Pins	IBF	A20	Comments
1	W	D1h	0	n(1)	Set A20 Sequence
0	W	DFh	0	1	Only DB1 Is Processed
1	W	FFH(2)	0	n	
1	W	D1h	0	n	Clear A20 Sequence
0	W	DDh	0	0	
1	W	FFh	0	n	
1	W	D1h	0	n	Double Trigger Set
1	W	D1h	0	n	Sequence
0	W	DFh	0	1	
1	W	FFh	0	n	
1	W	D1h	0	n	Invalid Sequence
1	W	XXh(3)	1	n	No Change in State
0	W	DDh	1	n	of A20 Bit

NOTES:
1. Indicates that P2.1 remains at the previous logic level.
2. Only FFh commands in a valid A20 sequence have no effect on IBF. An FFh issued at any other time will activate IBF.
3. Any command except D1.

The above sequences assume that the GATEA20 logic has been enabled via the A20EN instruction. As noted, only the value on DB 1 (data bus, bit 1) is processed. This bit will be directly passed through to P2.1 (port 2, bit 1). The A2OEN mode can be used in conjunction with both powerdown modes.

SUSPEND

The execution of the suspend instruction (82h or E2h) causes the UPI-C42 to enter the suspend mode. In this mode of operation the oscillator is not running and the internal CPU operation is stopped. The UPI-C42 consumes ≤ 40 μA in the suspend mode. This mode can only be exited by RESET. CPU operation will begin from PC = 000h when the UPI-C42 exits from the suspend power down mode.

Suspend Mode Summary

- Oscillator Not Running
- CPU Operation Stopped
- Ports Tristated with Weak ($\sim$2–10 μA) Pull-Up
- Micropower Mode ($I_{CC} \leq 40$ μA)
- This mode is exited by RESET

Table 2 covers all suspend mode pin states. In addition to the suspend power down mode, the UPI-C42 will also support the NMOS power down mode as outlined in Chapter 4 of the UPI-42AH users manual.

Table 2. Suspend Mode Pin States

Pins	Suspend
Ports 1 and 2 Outputs Inputs	 Tristate Weak Pull-Up Disabled
DBB(1) Outputs Inputs	 Normal Normal
System Control (RD#, WR#, CS#, A0)	Disabled
Reset#	Enabled
Crystal Osc. (XTAL1, XTAL2)	Disabled
Test 0, Test 1	Disabled
Prog	High
Sync	High
EA	Disabled, No Pull-Up
SS#	Disabled, Weak Pull-Up
I_{CC}	$<40\ \mu A$

NOTES:
1. DBB outputs are Tristate unless CS# and RD# are active. DBB inputs are disabled unless CS# and WR# are active.
2. A "disabled" input will not cause current to be drawn regardless of input level (within the supply range).
3. Weak pull-ups have current capability of typically 5 μA.

NEW UPI-C42 INSTRUCTIONS

The UPI-C42 will support several new instructions to allow for the use of new C42 features. These instructions are not necessary to the user who does not wish to take advantage of any new C42 functionality. The C42 will be completely compatible with all current NMOS code/applications. In order to use new features, however, some code modifications will be necessary. All new instructions can easily be inserted into existing code by use of the ASM-48 macro facility as shown in the following example:

```
Macname MACRO
        DB  63H
        ENDM
```

New Instructions

The following is a list of additions to the UPI-42 instruction set. These instructions apply only to the UPI-C42. These instructions must be added to existing code in order to use any new functionality.

SEL PMB0 Select Program Memory Bank 0

```
OPCODE  0110 0011 (63h)
```

PC Bit 11 is set to zero on next JMP or CALL instruction. All references to program memory fall within the range of 0–2047 (0–7FFh).

SEL PMB1 Select Program Memory Bank 1

```
OPCODE  0111 0011 (73h)
```

PC Bit 11 is set to one on next JMP or CALL instruction. All references to program memory fall within the range of 2048–4095 (800h–FFFh).

ENA20 Enables Auto A20 hardware

```
OPCODE  0011 0011 (33h)
```

Enables on chip logic to support Auto A20 Gate feature. Will remain enabled until device is reset. This

circuitry gives the host direct control of port 2 bit 1 (P2.1) without intervention by the internal CPU. When this opcode is executed, P2.1 becomes a dedicated output pin. The status of this pin is read-able but can only be altered through a valid "D1" command sequence (see Table 1).

ENTX Enable T0/T1 Wake Up Function

```
OPCODE  1100 0011 (C3H)
```

Enables on chip logic to allow the T0 or T1 input pin to "wake" the UPI-C42 from the STANDBY power down mode.

SUSPEND Invoke Suspend Power Down Mode

```
OPCODE  1000 0010 (82h) or 1110 0010
(E2h)
```

Enables device to enter micro power mode. In this mode the external oscillator is off, CPU operation is stopped, and the Port pins are tristated. This mode can only be exited via a RESET signal.

PROGRAMMING AND VERIFYING THE UPI-C42

The UPI-C42 programming will differ from the NMOS device in three ways. First, the C42 will have a 4K user programmable array. The UPI-C42 will also be programmed using the Intel Quick-Pulse Programming Algorithm. Finally, port 2 bit three (P2.3) will be used during program as the extra address pin required to program the upper 2K bank of additional memory. None of these differences have any effect on the full CHMOS to NMOS device compatibility. The extra memory is fully transparent to the user who does not need, or want, to use the extra memory space of the UPI-C42.

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 2	Clock Input
$\overline{\text{Reset}}$	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Signature Row/Security Bit Modes
BUS	Address and Data Input Data Output During Verify
P_{20-23}	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING
An attempt to program a missocketed UPI-C42 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the SYNC clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. Insert 87C42 in programming socket
2. CS = 5V, V_{CC} = 5V, V_{DD} = 5V, RESET = 0V, A_0 = 0V, TEST 0 = 5V, clock applied or internal oscillator operating, BUS floating, PROG = 5V.
3. TEST 0 = 0V (select program mode)
4. EA = 12.75V (active program mode)
5. V_{CC} = 6.25V (programming supply)
6. V_{DD} = 12.75V (programming power)
7. Address applied to BUS and P_{20-23}
8. $\overline{\text{RESET}}$ = 5V (latch address)
9. Data applied to BUS
10. PROG = 5V followed by one 100 μs pulse to 0V
11. TEST 0 = 5V (verify mode)
12. Read and verify data on BUS
13. TEST 0 = 0V
14. $\overline{\text{RESET}}$ = 0V and repeat from step 6
15. Programmer should be at conditions of step 1 when the 87C42 is removed from socket

Please follow the Quick-Pulse Programming flow chart for proper programming procedure shown in Figure 6.

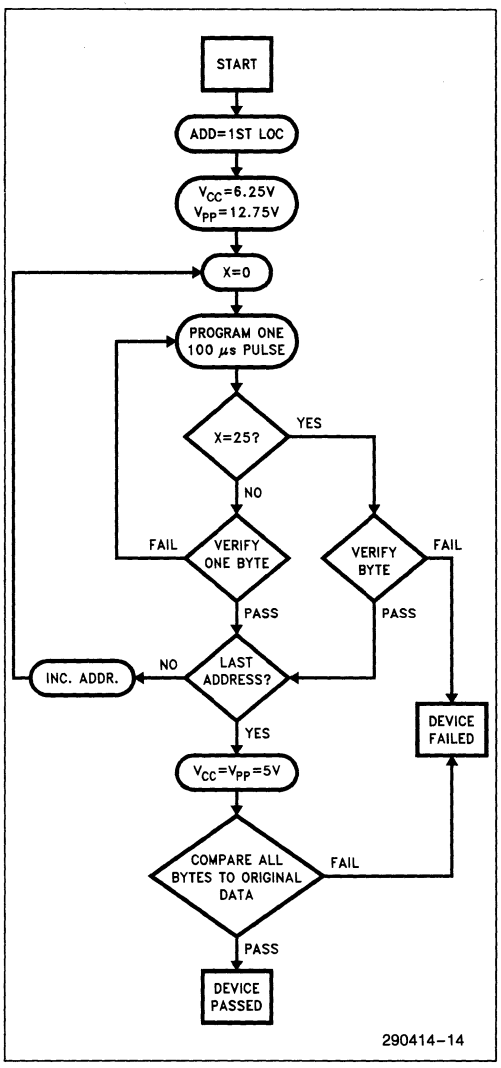


Figure 6. Quick-Pulse Programming Algorithm

Quick-Pulse Programming Algorithm

As previously stated, the UPI-C42 will be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the thorughput time in production programming.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 μs followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flow chart of the Quick-Pulse Programming Algorithm is shown in Figure 6.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.25V and V_{DD} = 12.75V. When programming has been completed, all bytes should be compared to the original data with V_{CC} = V_{DD} = 5V.

A verify should be performed on the programmed bits to ensure that they have been correctly programmed. The verify is performed with T0 = 5V, V_{DD} = 5V, EA = 12.75V, SS# = 5V, PROG = 5V, A0 = 0V, and CS# = 5V.

In addition to the Quick-Pulse Programming Algorithm, the UPI-C42 OPT is also compatible with Intel's Int$_e$ligent Programming Algorithm which is used to program the NMOS UPI-42AH OTP devices.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.25V and V_{DD} = 12.75V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0, V_{DD} = 5V.

Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with T0 = 5V, V_{DD} = 5V, EA = 12.75V, $\overline{SS}$ = 5V, PROG = 5V, A0 = 0V, and $\overline{CS}$ = 5V.

SECURITY BIT

The security bit is a single EPROM cell outside the EPROM array. The user can program this bit with the appropriate access code and the normal programming procedure, to inhibit any external access to the EPROM contents. Thus the user's resident program is protected. There is no direct external access to this bit. However, the security byte in the signature row has the same address and can be used to check indirectly whether the security bit has been programmed or not. The security bit has no effect on the signature mode, so the security byte can always be examined.

SECURITY BIT PROGRAMMING/ VERIFICATION

Programming

a. Read the security byte of the signature mode. Make sure it is 00H.

b. Apply access code to appropriate inputs to put the device into security mode.

c. Apply high voltage to EA and V_{DD} pins.

d. Follow the programming procedure as per the Quick-Pulse Programming Algorithm with known data on the databus. Not only the security bit, but also the security byte of the signature row is programmed.

e. Verify that the security byte of the signature mode contains the same data as appeared on the data bus. (If DB0–DB7 = high, the security byte will contain FFH.)

f. Read two consecutive known bytes from the EPROM array and verify that the wrong data are retrieved in at least one verification. If the EPROM can still be read, the security bit may have not been fully programmed though the security byte in the signature mode has.

Verification

Since the security bit address overlaps the address of the security byte of the signature mode, it can be used to check indirectly whether the security bit has been programmed or not. Therefore, the security bit verification is a mere read operation of the security byte of the signature row (0FFH = security bit programmed; 00H = security bit unprogrammed). Note that during the security bit programming, the reading of the security byte does not necessarily indicate that the security bit has been successfully programmed. Thus, it is recommended that two consecutive known bytes in the EPROM array be read and the wrong data should be read at least once, because it is highly improbable that random data coincides with the correct ones twice.

SIGNATURE MODE

The UPI-C42 has an additional 64 bytes of EPROM available for Intel and user signatures and miscellaneous purposes. The 64 bytes are partitioned as follows:

A. **Test code/checksum**—This can accommodate up to 25 bytes of code for testing the internal nodes that are not testable by executing from the external memory. The test code/checksum is present on ROMs, and OTPs.

B. **Intel signature**—This allows the programmer to read from the UPI-41AH/42AH/C42 the manufacturer of the device and the exact product name. It facilitates automatic device identification and will be present in the ROM and OTP versions. Location 10H contains the manufacturer code. For Intel, it is 89H. Location 11H contains the device code.

   The code is 43H and 42H for the 8042AH/80C42 and OTP 8742AH/87C42, respectively. The code is 44H for any device with the security bit set by Intel.

C. **User signature**—The user signature memory is implemented in the EPROM and consists of 2 bytes for the customer to program his own signature code (for identification purposes and quick sorting of previously programmed materials).

D. **Test signature**—This memory is used to store testing information such as: test data, bin number, etc. (for use in quality and manufacturing control).

E. **Security byte**—This byte is used to check whether the security bit has been programmed (see the security bit section).

F. **UPI-C42 Intel Signature**—Applies only to CHMOS device. Location 20H contains the manufacturer code and location 21H contains the device code. The Intel UPI-C42 manufacturer's code is 99H. The device ID's are 82H for the OTP version and 83H for the ROM version. The device ID's are the same for the UPI-L42.

The signature mode can be accessed by setting P10 = 0, P11–P17 = 1, and then following the programming and/or verification procedures. The location of the various address partitions are as shown in Table 3.

SYNC MODE

The Sync Mode is provided to ease the design of multiple controller circuits by allowing the designer to force the device into known phase and state time. The Sync Mode may also be utilized by automatic test equipment (ATE) for quick, easy, and efficient synchronizing between the tester and the DUT (device under test).

Sync Mode is enabled when $\overline{SS}$ pin is raised to high voltage level of +12 volts. To begin synchronization, T0 is raised to 5 volts at least four clock cycles after $\overline{SS}$. T0 must be high for at least four X2 clock cycles to fully reset the prescaler and time state generators. T0 may then be brought down during low state of X2. Two clock cycles later, with the rising edge of X2, the device enters into Time State 1, Phase 1. $\overline{SS}$ is then brought down to 5 volts 4 clocks later after T0. RESET is allowed to go high 5 tCY (75 clocks) later for normal execution of code.

Table 3. Signature Mode Table

	Address	Device Type	No. of Bytes
Test Code/Checksum	0 0FH 16H 1EH	ROM/OTP	25
Intel Signature	10H 11H	ROM/OTP	2
User Signature	12H 13H	OTP	2
Test Signature	14H 15H	ROM/OTP	2
Security Byte	1FH or 3FH	ROM/OTP	2
UPI-C42 Intel Signature	20H 21H	ROM/OTP	2
User Defined UPI-C42 OTP EPROM Space	22H 3EH	ROM/OTP	30

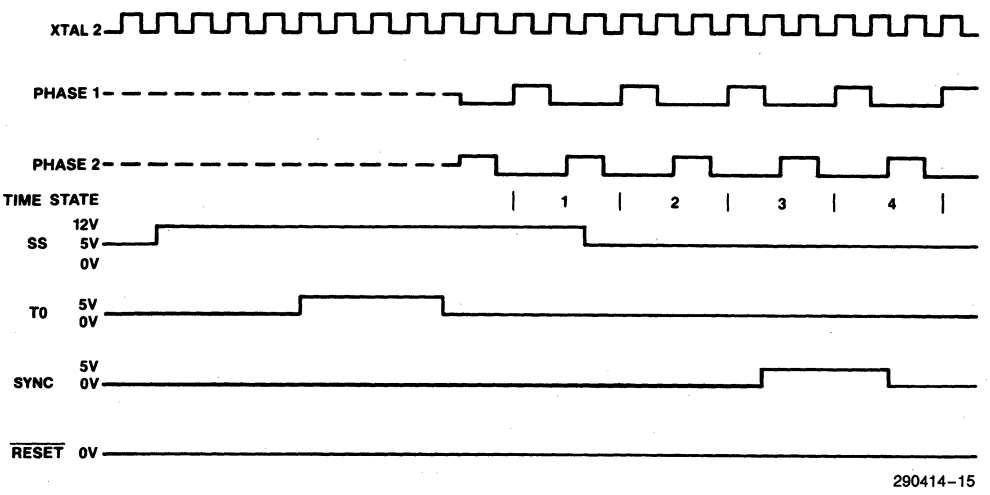
ACCESS CODE

The following table summarizes the access codes required to invoke the Sync Mode, Signature Mode, and the Security Bit, respectively. Also, the programming and verification modes are included for comparison.

Modes		Control Signals							Data Bus								Access Code							
																	Port 2	Port 1						
		T0	RST	SS	EA	PROG	V_{DD}	V_{CC}	0	1	2	3	4	5	6	7	0 1 2 3	0	1	2	3	4	5	6	7
Programming Mode		0	0	1	HV	1	V_{DDH}	V_{CC}	Address								Addr	a_0	a_1	X	X	X	X	X	X
		0	1	1	HV	STB	V_{DDH}	V_{CC}	Data In								Addr								
Verification Mode		0	0	1	HV	1	V_{CC}	V_{CC}	Address								Addr	a_0	a_1	X	X	X	X	X	X
		1	1	1	HV	1	V_{CC}	V_{CC}	Data Out								Addr								
Sync Mode		STB High	0	HV	0	X	V_{CC}	V_{CC}	X	X	X	X	X	X	X	X	X X X	X	X	X	X	X	X	X	X
Signature Mode	Prog	0	0	1	HV	1	V_{DDH}	V_{CC}	Addr. (see Sig Mode Table)								0 0 0	0	1	1	1	1	X	X	1
		0	1	1	HV	STB	V_{DDH}	V_{CC}	Data In								0 0 0								
	Verify	0	0	1	HV	1	V_{CC}	V_{CC}	Addr. (see Sig Mode Table)								0 0 0								
		1	1	1	HV	1	V_{CC}	V_{CC}	Data Out								0 0 0								
Security Bit/Byte	Prog	0	0	1	HV	1	V_{DDH}	V_{CC}	Address								0 0 0								
		0	1	1	HV	STB	V_{DDH}	V_{CC}	Data In								0 0 0								
	Verify	0	0	1	HV	1	V_{CC}	V_{CC}	Address								0 0 0								
		1	1	1	HV	1	V_{CC}	V_{CC}	Data Out								0 0 0								

NOTE:
1. a_0 = 0 or 1; a_1 = 0 or 1. a_0 must = a_1.

SYNC MODE TIMING DIAGRAMS



Minimum Specifications
SYNC Operation Time, t_{SYNC} = 3.5 XTAL 2 Clock cycles. Reset Time, t_{RS} = 4 t_{CY}.

NOTE:
The rising and falling edges of T0 should occur during low state of XTAL 2 clock.

APPLICATIONS

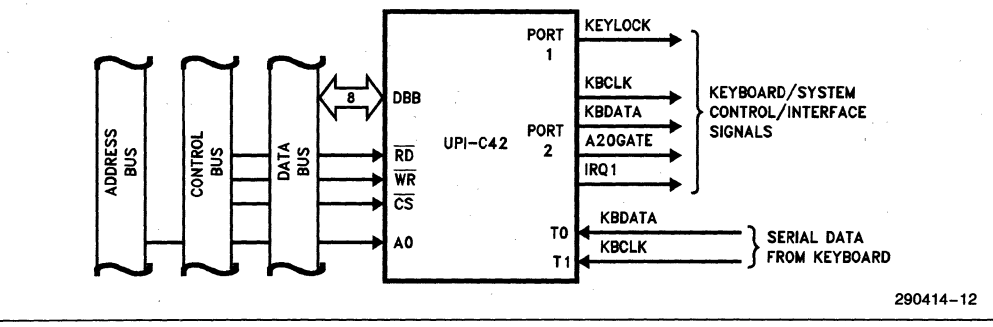


Figure 7. UPI-C42 Keyboard Controller

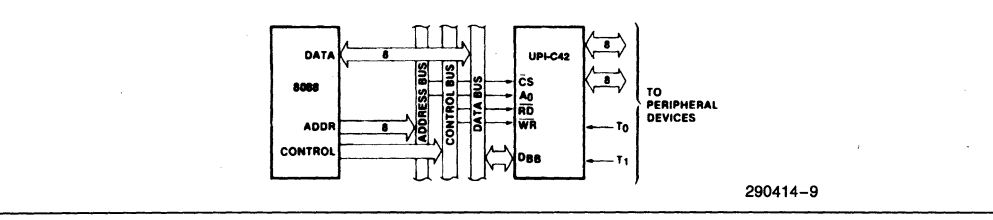


Figure 8. 8088-UPI-C42 Interface

APPLICATIONS (Continued)

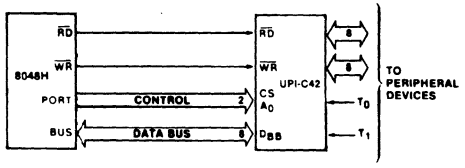


Figure 9. 8048H-UPI-C42 Interface

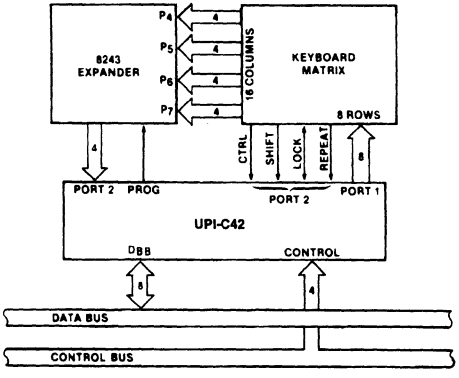


Figure 10. UPI-C42-8243 Keyboard Scanner

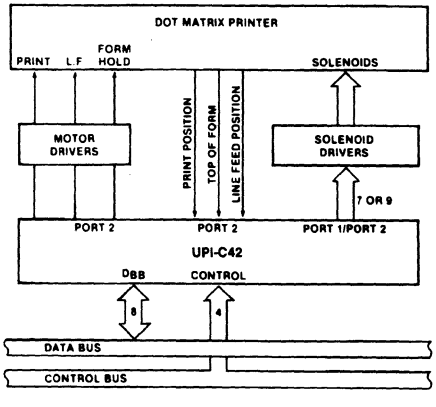


Figure 11. UPI-C42 80-Column Matrix Printer Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1.5 W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

DC CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ±10%; +3.3V ±10% UPI-L42

Symbol	Parameter	UPI-C42		UPI-L42		Units	Notes
		Min	Max	Min	Max		
V_{IL}	Input Low Voltage	−0.5	0.8	−0.3	+0.8	V	All Pins
V_{IH}	Input High Voltage (Except XTAL2, RESET)	2.0	V_{CC}	2.0	V_{CC} + 0.3	V	
V_{IH1}	Input High Voltage (XTAL2, RESET)	3.5	V_{CC}	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage (D_0–D_7)		0.45		0.45	V	I_{OL} = 2.0 mA UPI-C42 I_{OL} = 1.3 mA UPI-L42
V_{OL1}	Output Low Voltage ($P_{10}P_{17}$, $P_{20}P_{27}$, Sync)		0.45		0.45	V	I_{OL} = 1.6 mA UPI-C42 I_{OL} = 1 mA UPI-L42
V_{OL2}	Output Low Voltage (PROG)		0.45		0.45	V	I_{OL} = 1.0 mA UPI-C42 I_{OL} = 0.7 mA UPI-L42
V_{OH}	Output High Voltage (D_0–D_7)	2.4		2.4		V	I_{OH} = −400 μA UPI-C42 I_{OH} = −260 μA UPI-L42
V_{OH1}	Output High Voltage (All Other Outputs)	2.4		2.4			I_{OH} = −50 μA UPI-C42 I_{OH} = −25 μA UPI-L42
I_{IL}	Input Leakage Current (T_0, T_1, RD, WR, CS, A_0, EA)		±10		±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OFL}	Output Leakage Current (D_0–D_7, High Z State)		±10		±10	μA	V_{SS} + 0.45 ≤ $V_{OUT} \le V_{CC}$
I_{LI}	Low Input Load Current ($P_{10}P_{17}$, $P_{20}P_{27}$)	−50	−250	−35	−175	μA	Port Pins Min V_{IN} = 2.4V Max V_{IN} = 0.45V
I_{LI1}	Low Input Load Current (RESET, SS)		−40		−40	μA	$V_{IN} \le V_{IL}$
I_{HI}	Port Sink Current ($P_{10}P_{17}$, $P_{20}P_{27}$)				5.0	mA	V_{CC} = 3.0V V_{IH} = 5.0V
I_{DD}	V_{DD} Supply Current		4		2.5	mA	

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = V_{DD} = +5V ±10%; +3.3V ±10% UPI-L42 (Continued)

Symbol	Parameter	UPI-C42		UPI-L42		Units	Notes
		Min	Max	Min	Max		
$I_{CC} + I_{DD}$	Total Supply Current: Active Mode @ 12.5 MHz		30		20	mA	Typical 14 mA UPI-C42, 9 mA UPI-L42
	Suspend Mode		40		26	µA	Osc. Off(1, 4)
I_{DD} Standby	Power Down Supply Current		5		3.5	mA	NMOS Compatible Power Down Mode
I_{IH}	Input Leakage Current (P_{10}–P_{17}, P_{20}–P_{27})		100		100	µA	$V_{IN} = V_{CC}$
C_{IN}	Input Capacitance		10		10	pF	T_A = 25°C (1)
C_{IO}	I/O Capacitance		20		20	pF	T_A = 25°C (1)

NOTE:
1. Sampled, not 100% tested.

DC CHARACTERISTICS—PROGRAMMING (UPI-C42 AND UPI-L42)

T_A = 25°C ±5°C, V_{CC} = 6.25V ±0.25V, V_{DD} = 12.75V ±0.25V

Symbol	Parameter	Min	Max	Units
V_{DDH}	V_{DD} Program Voltage High Level	12.5	13	V(1)
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V
V_{PH}	PROG Program Voltage High Level	2.0	5.5	V
V_{PL}	PROG Voltage Low Level	−0.5	0.8	V
V_{EAH}	Input High Voltage for EA	12.0	13.0	V(2)
V_{EAL}	EA Voltage Low Level	−0.5	5.25	V
I_{DD}	V_{DD} High Voltage Supply Current		50.0	mA
I_{EA}	EA High Voltage Supply Current		1.0	mA(4)

NOTES:
1. Voltages over 13V applied to pin V_{DD} will permanently damage the device.
2. V_{EAH} must be applied to EA before V_{DDH} and removed after V_{DDL}.
3. V_{CC} must be applied simultaneously or before V_{DD} and must be removed simultaneously or after V_{DD}.
4. Sampled, not 100% tested.

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS} = 0V, V_{CC} = V_{DD} = +5V ±10%; +3.3V ±10% for the UPI-L42

NOTE:
All AC Characteristics apply to both the UPI-C42 and UPI-L42

DBB READ

Symbol	Parameter	Min	Max	Units
t_{AR}	CS, A_0 Setup to RD ↓	0		ns
t_{RA}	CS, A_0 Hold After RD ↑	0		ns
t_{RR}	RD Pulse Width	160		ns
t_{AD}	CS, A_0 to Data Out Delay		130	ns
t_{RD}	RD ↓ to Data Out Delay	0	130	ns
t_{DF}	RD ↑ to Data Float Delay		85	ns

DBB WRITE

Symbol	Parameter	Min	Max	Units
t_{AW}	CS, A_0 Setup to WR ↓	0		ns
t_{WA}	CS, A_0 Hold After WR ↑	0		ns
t_{WW}	WR Pulse Width	160		ns
t_{DW}	Data Setup to WR ↑	130		ns
t_{WD}	Data Hold After WR ↑	0		ns

AC CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS} = 0V, V_{CC} = V_{DD} = +5V ±10%; +3.3V ±10% for the UPI-L42 (Continued)

CLOCK

Symbol	Parameter	Min	Max	Units
t_{CY} UPI-C42/UPI-L42	Cycle Time	1.2	9.20	μs(1)
t_{CYC} UPI-C42/UPI-L42	Clock Period	80	613	ns
t_{PWH}	Clock High Time	30		ns
t_{PWL}	Clock Low Time	30		ns
t_R	Clock Rise Time		10	ns
t_F	Clock Fall Time		10	ns

NOTE:
1. t_{CY} = 15/f(XTAL)

AC CHARACTERISTICS DMA

Symbol	Parameter	Min	Max	Units
t_{ACC}	DACK to WR or RD	0		ns
t_{CAC}	RD or WR to DACK	0		ns
t_{ACD}	DACK to Data Valid	0	130	ns
t_{CRQ}	RD or WR to DRQ Cleared		110	ns(1)

NOTE:
1. C_L = 150 pF.

AC CHARACTERISTICS PORT 2

Symbol	Parameter	f(t_{CY})(3)	Min	Max	Units
t_{CP}	Port Control Setup Before Falling Edge of PROG	1/15 t_{CY} − 28	55		ns(1)
t_{PC}	Port Control Hold After Falling Edge of PROG	1/10 t_{CY}	125		ns(2)
t_{PR}	PROG to Time P2 Input Must Be Valid	8/15 t_{CY} − 16		650	ns(1)
t_{PF}	Input Data Hold Time		0	150	ns(2)
t_{DP}	Output Data Setup Time	2/10 t_{CY}	250		ns(1)
t_{PD}	Output Data Hold Time	1/10 t_{CY} − 80	45		ns(2)
t_{PP}	PROG Pulse Width	6/10 t_{CY}	750		ns

NOTES:
1. C_L = 80 pF.
2. C_L = 20 pF.
3. t_{CY} = 1.25 μs.

AC CHARACTERISTICS—PROGRAMMING (UPI-C42 AND UPI-L42)

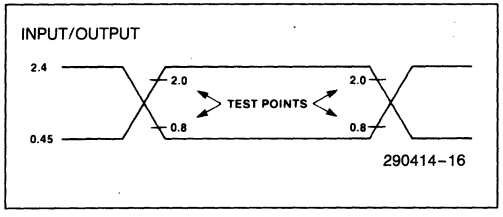
T_A = 25°C ±5°C, V_{CC} = 6.25V ±0.25V, V_{DDL} = +5V ±0.25V, V_{DDH} = 12.75V ±0.25V

(87C42/87L42 ONLY)

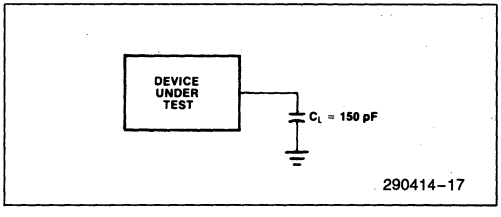
Symbol	Parameter	Min	Max	Units
t_{AW}	Address Setup Time to RESET ↑	$4t_{CY}$		
t_{WA}	Address Hold Time after RESET ↑	$4t_{CY}$		
t_{DW}	Data in Setup Time to PROG ↓	$4t_{CY}$		
t_{WD}	Data in Hold Time after PROG ↑	$4t_{CY}$		
t_{PW}	Initial Program Pulse Width	95	105	μs
t_{TW}	Test 0 Setup Time for Program Mode	$4t_{CY}$		
t_{WT}	Test 0 Hold Time after Program Mode	$4t_{CY}$		
t_{DO}	Test 0 to Data Out Delay		$4t_{CY}$	
t_{WW}	RESET Pulse Width to Latch Address	$4t_{CY}$		
t_r, t_f	PROG Rise and Fall Times	0.5	100	μs
t_{CY}	CPU Operation Cycle Time	2.5	3.75	μs
t_{RE}	RESET Setup Time before EA ↑	$4t_{CY}$		
t_{OPW}	Overprogram Pulse Width	2.85	78.75	ms(1)
t_{DE}	EA High to V_{DD} High	$1t_{CY}$		

NOTES:
1. This variation is a function of the iteration counter value, X.
2. If TEST 0 is high, t_{DO} can be triggered by RESET ↑.

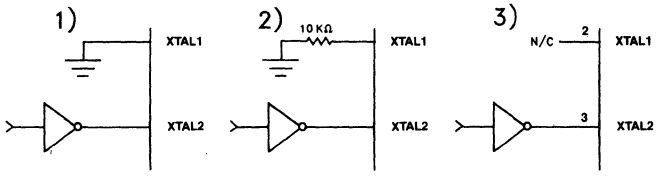
AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT



DRIVING FROM AN EXTERNAL SOURCE



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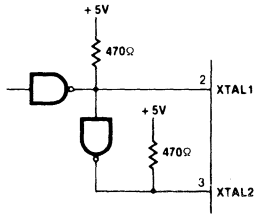
NOTE:
See XTAL1 Configuration Table.



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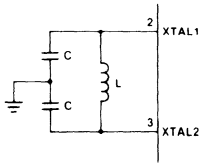
Rise and Fall Times Should Not Exceed 10 ns. Resistors to V_{CC} are Needed to Ensure V_{IH} = 3.5V if TTL Circuitry is Used.

LC OSCILLATOR MODE

L	C	NOMINAL
45 H	20 pF	5.2 MHz
120 H	20 pF	3.2 MHz



$$f = \frac{1}{2\pi\sqrt{LC'}}$$

$$C' = \frac{C + 3Cpp}{2}$$

Cpp ≅ 5-10 pF
Pin-to-Pin Capacitance

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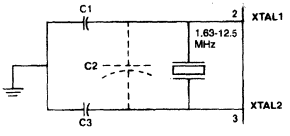
Each C Should be Approximately 20 pF, including Stray Capacitance.

CRYSTAL OSCILLATOR MODE



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C1 5 pF (STRAY 5 pF)
C2 (CRYSTAL + STRAY) 8 pF
C3 20-30 pF INCLUDING STRAY

Crystal Series Resistance Should be Less Than 30Ω at 12.5 MHz.

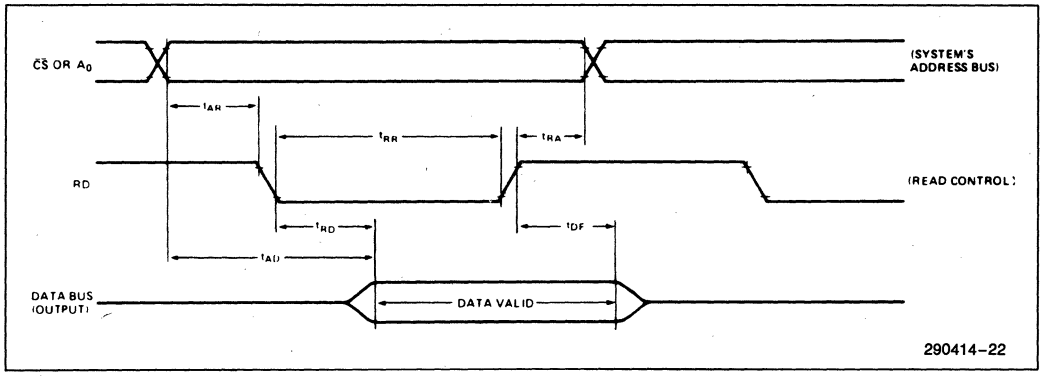
4

XTAL1 Configuration Table

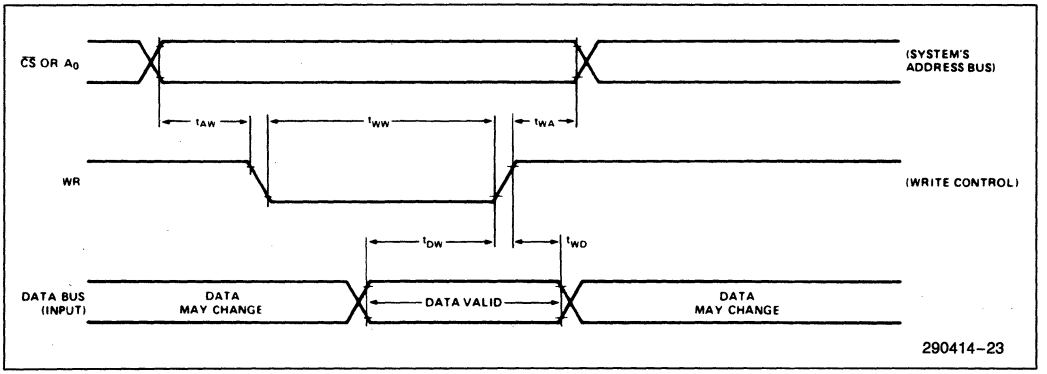
XTAL1 Connection		
1) to Ground	**2) 10 KΩ Resistor to Ground**	**3) Not Connected**
Not recommended for CHMOS designs. Causes approximately 16 mA of additional current flow through the XTAL1 pin on UPI-C42 and approximately 11 mA of additional current through XTAL1 on the UPI-L42.	Recommended configuration for designs which will use both NMOS and CHMOS parts. This configuration limits the additional current through the XTAL1 pin to approximately 1 mA, while maintaining compatibility with the NMOS device.	Low power configuration recommended for CHMOS only designs to provide lowest possible power consumption. This configuration will not work with the NMOS device.

WAVEFORMS

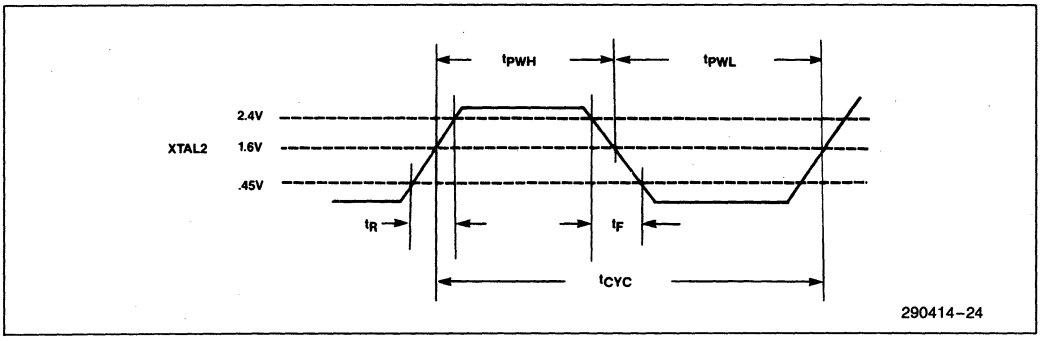
READ OPERATION—DATA BUS BUFFER REGISTER



WRITE OPERATION—DATA BUS BUFFER REGISTER

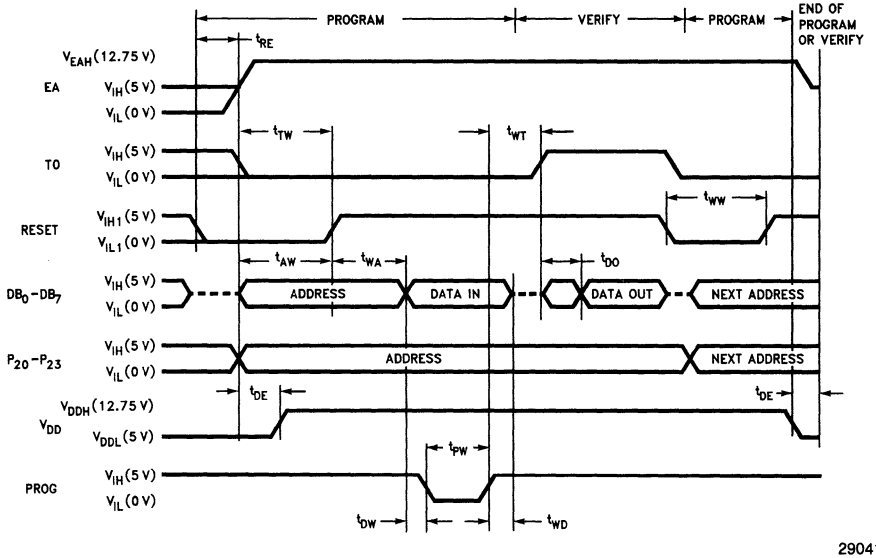


CLOCK TIMING



WAVEFORMS (Continued)

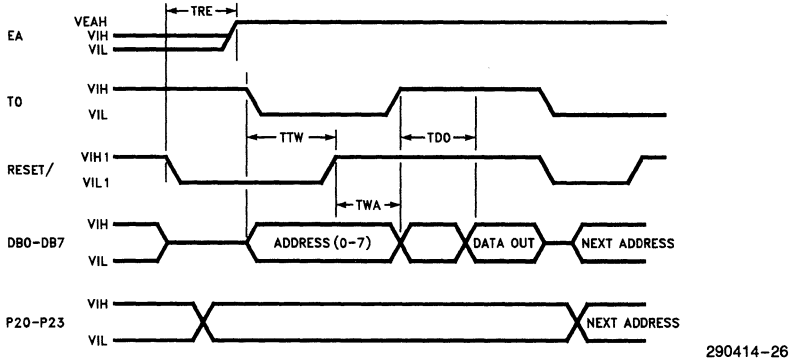
COMBINATION PROGRAM/VERIFY MODE



290414-25

NOTES:
1. A_0 must be held low (0V) during program/verify modes.
2. For V_{IH}, V_{IH1}, V_{IL}, V_{IL1}, V_{DDH}, and V_{DDL}, please consult the D.C. Characteristics Table.
3. When programming the 87C42, a 0.1 μF capacitor is required across V_{DD} and ground to suppress spurious voltage transients which can damage the device.

VERIFY MODE



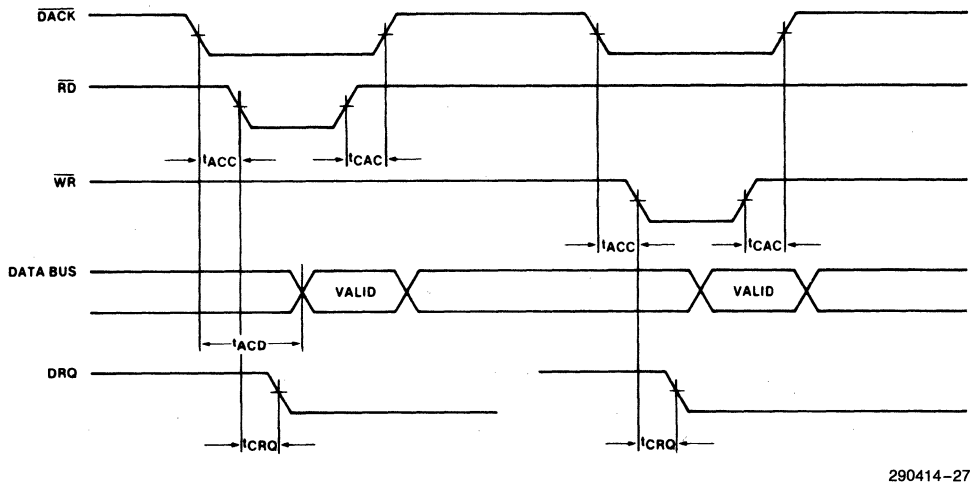
290414-26

NOTES:
1. PROG must float if EA is low.
2. PROG must float or = 5V when EA is high.
3. P_{10}-P_{17} = 5V or must float.
4. P_{24}-P_{27} = 5V or must float.
5. A_0 must be held low during programming/verify modes.

4

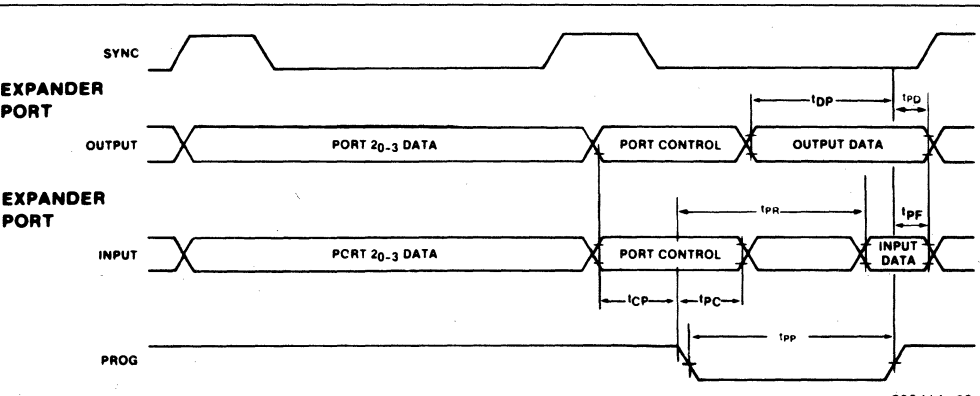
WAVEFORMS (Continued)

DMA



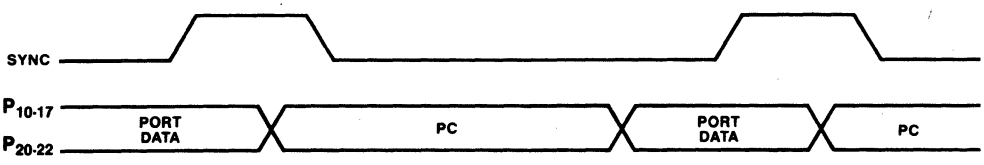
290414-27

PORT 2



290414-28

PORT TIMING DURING EXTERNAL ACCESS (EA)



290414-29

On the Rising Edge of SYNC and EA is Enabled, Port Data is Valid and can be Strobed. On the Trailing Edge of Sync the Program Counter Contents are Available.

Table 4. UPI Instruction Set

Mnemonic	Description	Bytes	Cycles
ACCUMULATOR			
ADD A, Rr	Add register to A	1	1
ADD A, @Rr	Add data memory to A	1	1
ADD A, #data	Add immediate to A	2	2
ADDC A, Rr	Add register to A with carry	1	1
ADDC A, @Rr	Add data memory to A with carry	1	1
ADDC A, #data	Add immediate to A with carry	2	2
ANL A, Rr	AND register to A	1	1
ANL, A @Rr	AND data memory to A	1	1
ANL A, #data	AND immediate to A	2	2
ORL A, Rr	OR register to A	1	1
ORL, A, @Rr	OR data memory to A	1	1
ORL A, #data	OR immediate to A	2	2
XRL A, Rr	Exclusive OR register to A	1	1
XRL A, @Rr	Exclusive OR data memory to A	1	1
XRL A, #data	Exclusive OR immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal Adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
INPUT/OUTPUT			
IN A, Pp	Input port to A	1	2
OUTL Pp, A	Output A to port	1	2
ANL Pp, #data	AND immediate to port	2	2
ORL Pp, #data	OR immediate to port	2	2
IN A, DBB	Input DBB to A, clear IBF	1	1
OUT DBB, A	Output A to DBB, set OBF	1	1
MOV STS, A	A_4–A_7 to Bits 4–7 of Status	1	1
MOVD A, Pp	Input Expander port to A	1	2
MOVD Pp, A	Output A to Expander port	1	2
ANLD Pp, A	AND A to Expander port	1	2
ORLD Pp, A	OR A to Expander port	1	2

Mnemonic	Description	Bytes	Cycles
DATA MOVES			
MOV A, Rr	Move register to A	1	1
MOV A, @Rr	Move data memory to A	1	1
MOV A, #data	Move immediate to A	2	2
MOV Rr, A	Move A to register	1	1
MOV @Rr, A	Move A to data memory	1	1
MOV Rr, #data	Move immediate to register	2	2
MOV @Rr, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, Rr	Exchange A and register	1	1
XCH A, @Rr	Exchange A and data memory	1	1
XCHD A, @Rr	Exchange digit of A and register	1	1
MOVP A, @A	Move to A from current page	1	2
MOVP3, A, @A	Move to A from page 3	1	2
TIMER/COUNTER			
MOV A, T	Read Timer/Counter	1	1
MOV T, A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	Start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/Counter Interrupt	1	1
DIS TCNTI	Disable Timer/Counter Interrupt	1	1
CONTROL			
*EN A20	Enable A20 Logic	1	1
EN DMA	Enable DMA Handshake Lines	1	1
EN I	Enable IBF Interrupt	1	1
*EN Tx	Enable T0/T1 Wake Up Function	1	1
DIS I	Diable IBF Interrupt	1	1
EN FLAGS	Enable Master Interrupts	1	1
*SEL PMB0	Select Program memory bank 0	1	1
*SEL PMB1	Select Program memory bank 1	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1

* UPI-C42/UPI-L42 Only.

4

Table 4. UPI Instruction Set (Continued)

Mnemonic	Description	Bytes	Cycles
CONTROL (Continued)			
*SUSPEND	Invoke Suspend Power-down mode	1	2
NOP	No Operation	1	1
REGISTERS			
INC Rr	Increment register	1	1
INC @Rr	Increment data memory	1	1
DEC Rr	Decrement register	1	1
SUBROUTINE			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2
FLAGS			
CLR C	Clear Carry	1	1
CPL C	Complement Carry	1	1
CLR F0	Clear Flag 0	1	1
CPL F0	Complement Flag 0	1	1
CLR F1	Clear F1 Flag	1	1
CPL F1	Complement F1 Flag	1	1

Mnemonic	Description	Bytes	Cycles
BRANCH			
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ Rr, addr	Decrement register and jump	2	2
JC addr	Jump on Carry = 1	2	2
JNC addr	Jump on Carry = 0	2	2
JZ addr	Jump on A Zero	2	2
JNZ addr	Jump on A not Zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 Flag = 1	2	2
JF1 addr	Jump on F1 Flag = 1	2	2
JTF addr	Jump on Timer Flag = 1, Clear Flag	2	2
JNIBF addr	Jump on IBF Flag = 0	2	2
JOBF addr	Jump on OBF Flag = 1	2	2
JBb addr	Jump on Accumula-for Bit	2	2

*UPI-C42/UPI-L42 Only.

REVISION SUMMARY

The following has been changed since Revision -003:

1. Delete all references to standby powerdown mode.

The following has been changed since Revision -002:

1. Added information on keyboard controller product family.
2. Added I_{HI} specification for the UPI-L42.

The following has been changed since Revision -001:

1. Added UPI-L42 references and specification.

intel®

5

Support Peripherals

UPI-452
CHMOS PROGRAMMABLE I/O PROCESSOR

83C452 - 8K × 8 Mask Programmable Internal ROM

80C452 - External ROM/EPROM

- **83C452/80C452:3.5 to 14 MHz Clock Rate**
- **Software Compatible with the MCS-51 Family**
- **128-Byte Bi-Directional FIFO Slave Interface**
- **Two DMA Channels**
- **256 × 8-Bit Internal RAM**
- **34 Additional Special Function Registers**
- **40 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **Boolean Processor**
- **Bit Addressable RAM**
- **8 Interrupt Sources**
- **Programmable Full Duplex Serial Channel**
- **64K Program Memory Space**
- **64K Data Memory Space**
- **68-Pin PGA and PLCC**
  (See Packaging Spec., Order: #231369)

The Intel UPI-452 (Universal Peripheral Interface) is a 68 pin CHMOS Slave I/O Processor with a sophisticated bi-directional FIFO buffer interface on the slave bus and a two channel DMA processor on-chip. The UPI-452 is the newest member of Intel's UPI family of products. It is a general-purpose slave I/O Processor that allows the designer to grow a customized interface solution.

The UPI-452 contains a complete 80C51 with twice the on-chip data and program memory. The sophisticated slave FIFO module acts as a buffer between the UPI-452 internal CPU and the external host CPU. To both the external host and the internal CPU, the FIFO module looks like a bi-directional bottomless buffer that can both read and write data. The FIFO manages the transfer of data independent of the UPI-452 core CPU and generates an interrupt or DMA request to either CPU, host or internal, as a FIFO service request.

The FIFO consists of two channels:the Input FIFO and the Output FIFO. The division of the FIFO module array, 128 bytes, between Input channel and Output channel is programmable by the user. Each FIFO byte has an additional logical ninth bit to distinguish between a data byte and a Data Stream Command byte. Additionally, Immediate Commands allow direct, interrupt driven, bi-directional communication between the UPI-452 internal CPU and external host CPU, bypassing the FIFO.

The on-chip DMA processor allows high speed data transfers from one writeable memory space to another. As many as 64K bytes can be transferred in a single DMA operation. Three distinct memory spaces may be used in DMA operations; Internal Data Memory, External Data Memory, and the Special Function Registers (including the FIFO IN, FIFO OUT, and Serial Channel Special Functions Registers).

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

November 1994
Order Number: 231428-006

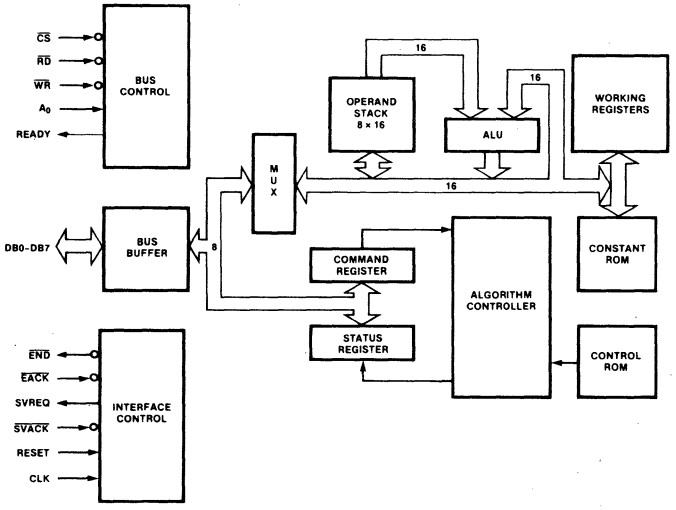
8231A
ARITHMETIC PROCESSING UNIT

- **Fixed Point Single and Double Precision (16/32 Bit)**
- **Floating Point Single Precision (32 Bit)**
- **Binary Data Formats**
- **Add, Subtract, Multiply and Divide**
- **Trignometric and Inverse Trigonometric Functions**
- **Square Roots, Logarithms, Exponentiation**
- **Float to Fixed and Fixed to Float Conversions**
- **Stack Oriented Operand Storage**
- **Compatible with all Intel and most other Microprocessor Families**
- **Direct Memory Access or Programmed I/O Data Transfers**
- **End of Execution Signal**
- **General Purpose 8-Bit Data Bus Interface**
- **Standard 24 Pin Package**
- **+12V and +5V Power Supplies**
- **Advanced N-Channel Silicon Gate HMOS Technology**

The Intel 8231A Arithmetic Processing Unit (APU) is a monolithic HMOS LSI device that provides high performance fixed and floating point arithmetic and floating point trigonometric operations. It may be used to enhance the mathematical capability of a wide variety of processor-oriented systems. Chebyshev polynomials are used in the implementation of the APU algorithms.

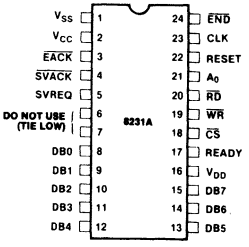
All transfers, including operand, result, status and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack and commands are issued to perform operations on the data and the stack. Results are then available to be retrieved from the stack.

Transfers to and from the APU may be handled by the associated processor using conventional programmed I/O, or may be handled by a direct memory access controller for improved performance. Upon completion of each command, the APU issues an end of execution signal that may be used as an interrupt by the CPU to help coordinate program execution.



231305-1

Figure 1. Block Diagram



231305-2

Figure 2. Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1993
Order Number: 231305-003

8237A
HIGH PERFORMANCE PROGRAMMABLE DMA CONTROLLER (8237A-5)

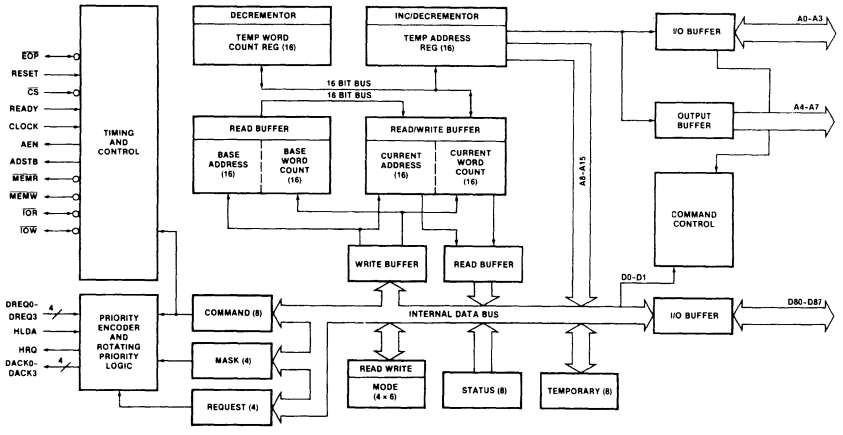
- **Enable/Disable Control of Individual DMA Requests**
- **Four Independent DMA Channels**
- **Independent Autoinitialization of All Channels**
- **Memory-to-Memory Transfers**
- **Memory Block Initialization**
- **Address Increment or Decrement**
- **High Performance: Transfers up to 1.6M Bytes/Second with 5 MHz 8237A-5**
- **Directly Expandable to Any Number of Channels**
- **End of Process Input for Terminating Transfers**
- **Software DMA Requests**
- **Independent Polarity Control for DREQ and DACK Signals**
- **Available in EXPRESS — Standard Temperature Range**
- **Available in 40-Lead Cerdip and Plastic Packages**

(See Packaging Spec, Order #231369)

The 8237A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The 8237A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

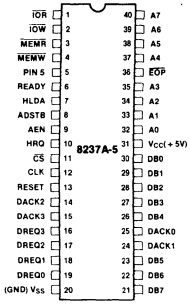
The 8237A is designed to be used in conjunction with an external 8-bit address latch. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process ($\overline{EOP}$). Each channel has a full 64K address and word count capability.

5



231466-1

Figure 1. Block Diagram



231466-2

Figure 2. Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1993
Order Number: 231466-005

82C37A-5
CHMOS HIGH PERFORMANCE PROGRAMMABLE DMA CONTROLLER

- **Pin Compatible with NMOS 8237A-5**
- **Enable/Disable Control of Individual DMA Requests**
- **Fully Static Design with Frequency Range from DC to 5 MHz**
- **Low Power Operation**
- **Four Independent DMA Channels**
- **Independent Autoinitialization of all Channels**
- **Memory-to-Memory Transfers**
- **Memory Block Initialization**
- **Address Increment or Decrement**
- **High performance: 5 MHz Speed Transfers up to 1.6 MBytes/Second**
- **Directly Expandable to any Number of Channels**
- **End of Process Input for Terminating Transfers**
- **Software DMA Requests**
- **Independent Polarity Control for DREQ and DACK Signals**
- **Available in 40-Lead Plastic DIP**

The Intel 82C37A-5 Multimode Direct Memory Access (DMA) Controller is a CHMOS peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The 82C37A-5 offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The 82C37A-5 is designed to be used in conjunction with an external 8-bit address register. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process ($\overline{EOP}$).

Each channel has a full 64K address and word count capability.

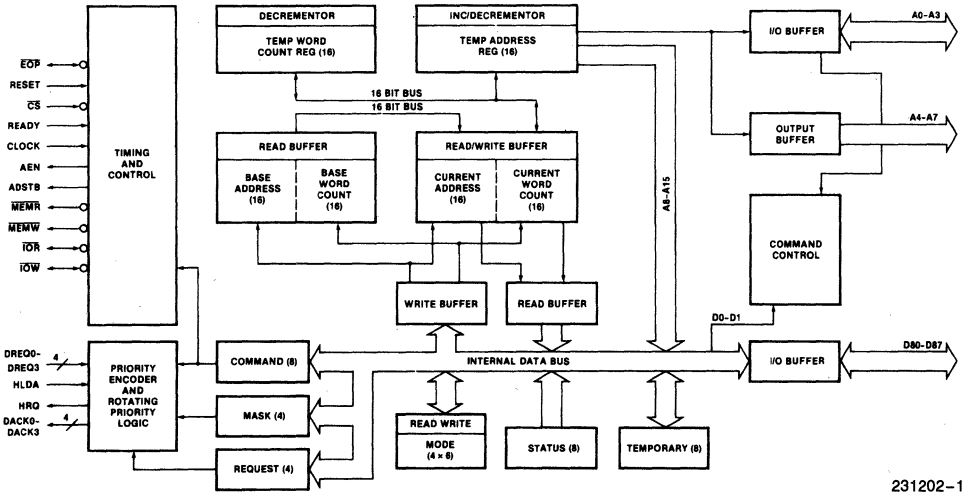


Figure 1. Block Diagram

November 1994
Order Number: 231202-006

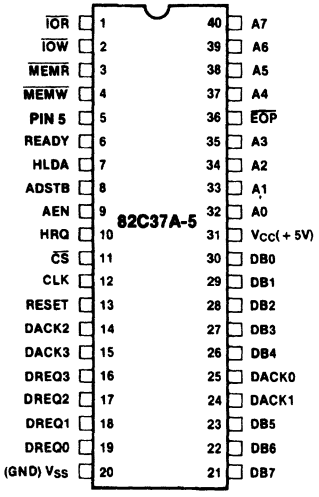


Figure 2. 82C37A-5
40-Lead DIP Configuration

5

Table 1. Pin Description

Symbol	Type	Name and Function
V_{CC}		**POWER:** +5 volt supply.
V_{SS}		**GROUND:** Ground.
CLK	I	**CLOCK INPUT:** Clock Input controls the internal operations of the 82C37A-5 and its rate of data transfers. The input may be driven at up to 5 MHz for the 82C37A-5.
$\overline{CS}$	I	**CHIP SELECT:** Chip Select is an active low input used to select the 82C37A-5 as an I/O device during the Idle cycle. This allows CPU communication on the data bus.
RESET	I	**RESET:** Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip-flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
READY	I	**READY:** Ready is an input used to extend the memory read and write pulses from the 82C37A-5 to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
HLDA	I	**HOLD ACKNOWLEDGE:** The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.
DREQ0–DREQ3	I	**DMA REQUEST:** The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.
DB0–DB7	I/O	**DATA BUS:** The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 82C37A-5 control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the 82C37A-5 on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.
$\overline{IOR}$	I/O	**I/O READ:** I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 82C37A-5 to access data from a peripheral during a DMA Write transfer.
$\overline{IOW}$	I/O	**I/O WRITE:** I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 82C37A-5. In the Active cycle, it is an output control signal used by the 82C37A-5 to load data to the peripheral during a DMA Read transfer.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
$\overline{EOP}$	I/O	**END OF PROCESS:** End of Process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The 82C37A-5 allows an external signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ input low with an external $\overline{EOP}$ signal. The 82C37A-5 also generates a pulse when the terminal count (TC) for any channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ Line. The reception of $\overline{EOP}$, either internal or external, will cause the 82C37A-5 to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.
A0–A3	I/O	**ADDRESS:** The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the CPU to address the register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.
A4–A7	O	**ADDRESS:** The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	O	**HOLD REQUEST:** This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 82C37A-5 to issue the HRQ. After HRQ goes active at least one clock cycle (TCY) must occur before HLDA goes active.
DACK0–DACK3	O	**DMA ACKNOWLEDGE:** DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	O	**ADDRESS ENABLE:** Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	O	**ADDRESS STROBE:** The active high, Address Strobe is used to strobe the upper address byte into an external latch.
$\overline{MEMR}$	O	**MEMORY READ:** The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
$\overline{MEMW}$	O	**MEMORY WRITE:** The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.
PIN5	I	**PIN5:** This pin should always be at a logic HIGH level. An internal pull-up resistor will establish a logic HIGH when the pin is left floating. It is recommended, however, that PIN5 be connected to V_{CC}.

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FUNCTIONAL DESCRIPTION

The 82C37A-5 block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The 82C37A-5 contains 344 bits of internal memory in the form of registers. Figure 3 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 3. 82C37A-5 Internal Registers

The 82C37A-5 contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the 82C37A-5. The Program Command Control block decodes the various commands given to the 82C37A-5 by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word used to select the type of DMA during the servicing. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

DMA Operation

The 82C37A-5 is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The 82C37A-5 can assume seven separate states, each composed of one full clock period. State 1 (S1) is the inactive state. It is entered when the 82C37A-5 has no valid DMA requests pending. While in S1, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The 82C37A-5 has requested a hold but the processor has not yet returned an acknowledge. The 82C37A-5 may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the 82C37A-5. Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is not read into or driven out of the 82C37A-5 in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

IDLE CYCLE

When no channel is requesting service, the 82C37A-5 will enter the Idle cycle and perform "S1" states. In this cycle the 82C37A-5 will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the 82C37A-5. When $\overline{CS}$ is low and HLDA is low, the 82C37A-5 enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0–A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by Master Clear or Reset. A separate software command can also reset this flip-flop.

Special software commands can be executed by the 82C37A-5 in the Program Condition. These commands are decoded as sets of addresses with the $\overline{CS}$ and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Clear First/Last Flip-Flop and Master Clear.

ACTIVE CYCLE

When the 82C37A-5 is in the Idle cycle and a non-masked channel requests a DMA service, the device

will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode — In Single Transfer mode the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.

DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, in 8080A, 8085AH, 80C88, or 80C86 system this will ensure one full machine cycle execution between DMA transfers. Details of timing between the 82C37A-5 and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode — In Block Transfer mode the device is activated by DREQ to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process (EOP) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode — In Demand Transfer mode the device is programmed to continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 82C37A-5 Current Address and Current Word Count registers. Only an $\overline{EOP}$ can cause an Autoinitialize at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode — This mode is used to cascade more than one 82C37A-5 together for simple system expansion. The HRQ and HLDA signals from the additional 82C37A-5 are connected to the DREQ and DACK signals of a channel of the initial 82C37A-5. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 82C37A-5 is used only for prioritizing the additional device, it does not output any address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The 82C37A-5 will respond to DREQ and DACK but all other outputs except HRQ will be disabled. The ready input is ignored.

Figure 4 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More 82C37A-5s could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

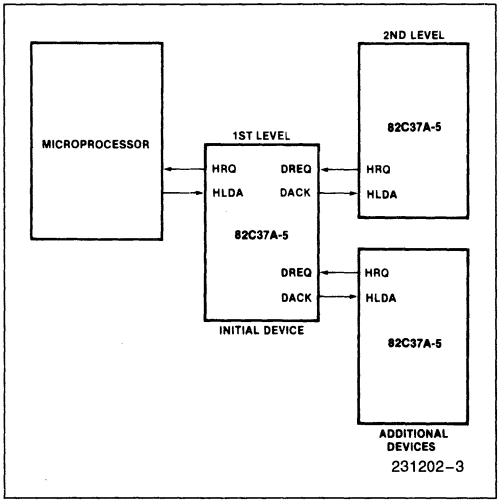

Figure 4. Cascaded 82C37A-5s

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from and I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers. The 82C37A-5 operates as in Read or Write transfers generating addresses, and responding to EOP, etc. However, the memory and I/O control lines all remain inactive. The ready input is ignored in verify mode.

Memory-to-Memory — To perform block moves of data from one memory address space to another with a minimum of program effort and time, the 82C37A-5 includes a memory-to-memory transfer feature. Programming a bit in the Command register selects channels 0 to 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The

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82C37A-5 requests a DMA service in the normal manner. After HLDA is true, the device, using four state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 82C37A-5 internal Temporary register. Channel 1 then performs a four-state transfer of the data from the Temporary register to memory using the address in its Current Address register and incrementing or decrementing it in the normal manner. The channel 1 current Word Count is decremented. When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{EOP}$ output terminating the service.

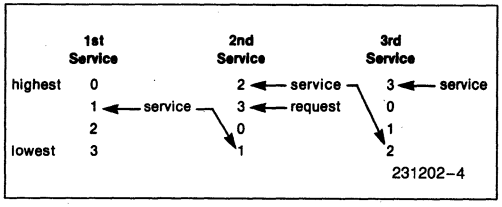
Channel 0 may be programmed to retain the same address for all transfers. This allows a single word to be written to a block of memory.

The 82C37A-5 will respond to external $\overline{EOP}$ signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 12. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Autoinitialize — By programming a bit in the Mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialize initialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not altered when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected. In order to Autoinitialize both channels in a memory-to-memory transfer, both word counts should be programmed identically. If interrupted externally, $\overline{EOP}$ pulses should be applied in both bus cycles.

Priority — The 82C37A-5 has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with that service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Compressed Timing — In order to achieve even greater throughput where system characteristics permit, the 82C37A-5 can compress the transfer time to two clock cycles. From Figure 11 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8–A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 14.

Address Generation — In order to reduce pin count, the 82C37A-5 multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 82C37A-5 directly. Lines A0–A7 should be connected to the address bus. Figure 11 shows the time relationships between CLK, AEN, ADSTB, DB0–DB7 and A0–A7.

During Block and Demand Transfer mode services, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 82C37A-5 executes S1 states only when updating of A8–A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

REGISTER DESCRIPTION

Current Address Register — Each channel has a 16-bit Current Address register. This register holds

the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$.

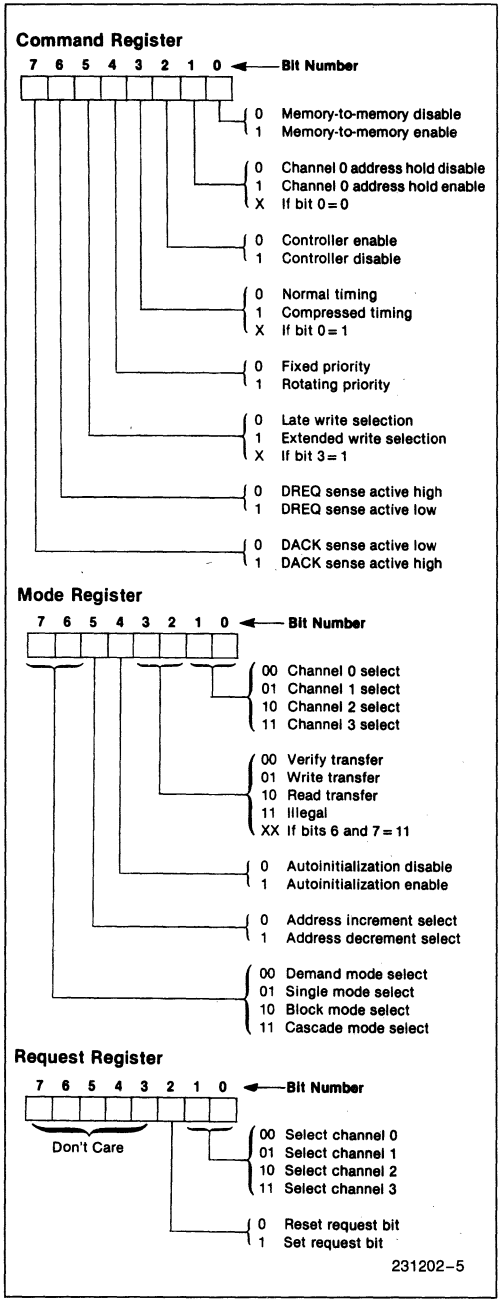
Current Word Register — Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialize can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

Base Address and Base Word Count Registers — Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register — This 8-bit register controls the operation of the 82C37A-5. It is programmed by the microprocessor in the Program Condition and is cleared by Reset or a Master Clear instruction. The following table lists the function of the command bits. See Figure 6 for address coding.

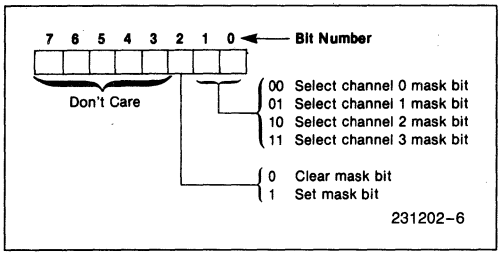
Mode Register — Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

Request Register — The 82C37A-5 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are non-maskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external $\overline{EOP}$. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 5 for register ad-

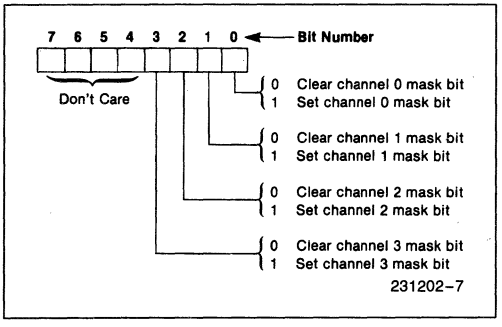


dress coding. In order to make a software request, the channel must be in Block Mode.

Mask Register — Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 5 for instruction addressing.



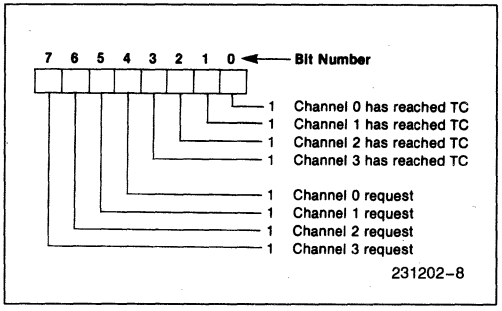
All four bits of the Mask register may also be written with a single command.



Register	Operation	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

Figure 5. Definition of Register Codes

Status Register — The Status register is available to be read out of the 82C37A-5 by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0–3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset and on each Status Read. Bits 4–7 are set whenever their corresponding channel is requesting service.



Temporary Register — The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands — These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The three software commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the 82C37A-5. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The 82C37A-5 will enter the Idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Figure 6 lists the address codes for the software commands:

Signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip-Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Figure 6. Software Command Codes

PROGRAMMING

The 82C37A-5 will accept programming from the host processor any time that HLDA is inactive; this is true even if HRQ is active. The responsibility of the host is to assure that programming and HLDA are mutually exclusive. Note that a problem can occur if a DMA request occurs, on an unmasked channel while the 82C37A-5 is being programmed. For instance, the CPU may be starting to reprogram the two byte Address register of channel 1 when channel 1 receives a DMA request. If the 82C37A-5 is enabled (bit 2 in the command register is 0) and channel 1 is unmasked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any other registers. Once the programming is complete, the controller can be enabled/unmasked.

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0–DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0–A7
			0	1	0	0	0	0	0	1	A8–A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0–A7
			0	0	1	0	0	0	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0–W7
			0	1	0	0	0	0	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0–W7
			0	0	1	0	0	0	1	1	W8–W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0–A7
			0	1	0	0	0	1	0	1	A8–A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0–A7
			0	0	1	0	0	1	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0–W7
			0	1	0	0	0	1	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0–W7
			0	0	1	0	0	1	1	1	W8–W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0–A7
			0	1	0	0	1	0	0	1	A8–A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0–A7
			0	0	1	0	1	0	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0–W7
			0	1	0	0	1	0	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0–W7
			0	0	1	0	1	0	1	1	W8–W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0–A7
			0	1	0	0	1	1	0	1	A8–A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0–A7
			0	0	1	0	1	1	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0–W7
			0	1	0	0	1	1	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0–W7
			0	0	1	0	1	1	1	1	W8–W15

Figure 7. Word Count and Address Register Command Codes

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After power-up it is suggested that all internal locations, especially the Mode registers, be loaded with some valid value. This should be done even if some channels are unused.

APPLICATION INFORMATION

Figure 8 shows a convenient method for configuring a DMA system with the 82C37A-5 controller and an 8080A/8085AH microprocessor system. The multimode DMA controller issues a HRQ to the processor whenever there is at least one valid DMA request from a peripheral device. When the processor replies with a HLDA signal, the 82C37A-5 takes control of the address bus, the data bus and the control bus. The address for the first transfer operation comes out in two bytes — the least significant 8 bits on the eight address outputs and the most significant 8 bits on the data bus. The contents of the data bus are then latched into the 8-bit latch to complete the full 16 bits of the address bus. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are provided when one 82C37A-5 is used.

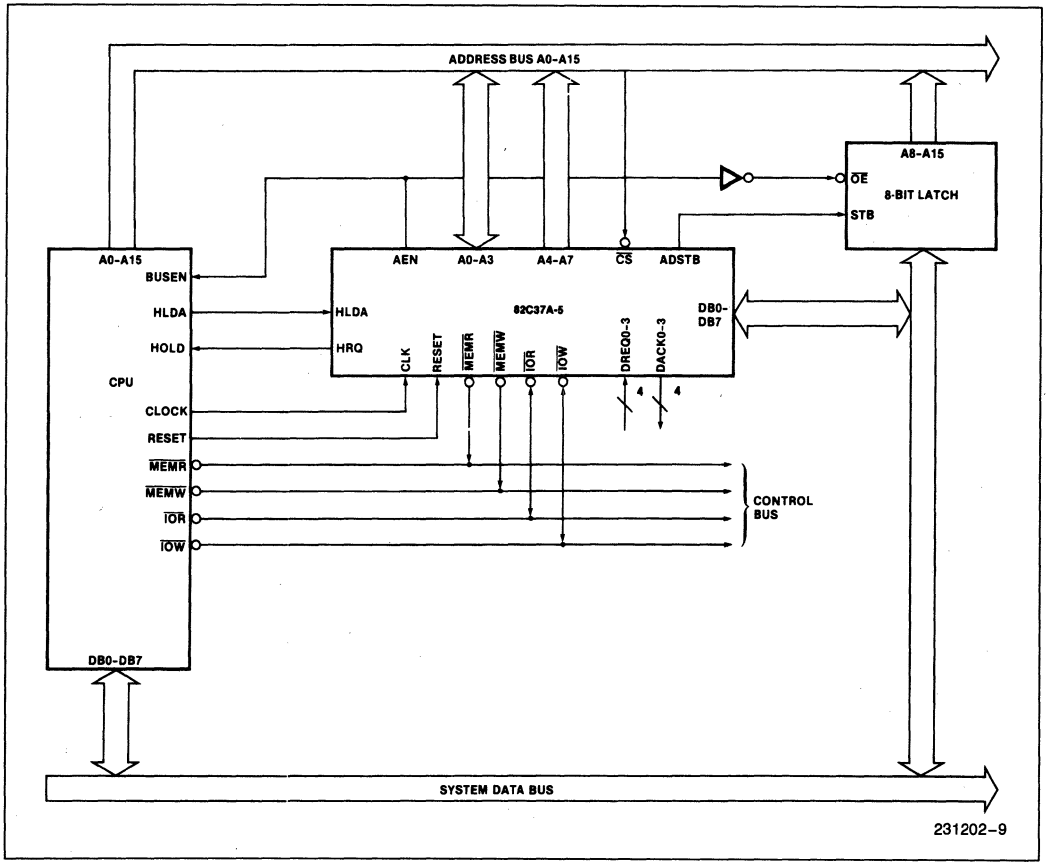


Figure 8. 82C37A-5 System Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias .....0°C to 70°C
Case Temperature .....0°C to +75°C
Storage Temperature .....−55°C to +150°C
Voltage on Any Pin with Respect to Ground.....−0.5V to +7V
Power Dissipation.....1.0 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, T_{CASE} = 0°C to 75°C, V_{CC} = +5.0V ±5%, GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	Output High Voltage	3.7			V	I_{OH} = −1.0 mA
V_{OL}	Output LOW Voltage			0.40	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Voltage	2.2		V_{CC} + 0.5	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
I_{LI}	Input Load Current			±10	μA	$0V \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current			±10	μA	$0V \le V_{OUT} \le V_{CC}$
I_{CC}	V_{CC} Supply Current			10	mA	(Note 1)
I_{CCS}	Standby Supply Current			10	μA	HLDA = 0V, V_{IL} = 0V, $V_{IH} = V_{CC}$
C_O	Output Capacitance		4	8	pF	fc = 1.0 MHz, Inputs = 0V
C_I	Input Capacitance		8	15	pF	
C_{IO}	I/O Capacitance		10	18	pF	

5

A.C. CHARACTERISTICS—DMA (MASTER) MODE

T_A = 0°C to 70°C, T_{CASE} = 0°C to 75°C, V_{CC} = +5V ±5%, GND = 0V

Symbol	Parameter	Min	Max	Unit
TAEL	AEN HIGH from CLK LOW (S1) Delay Time		200	ns
TAET	AEN LOW from CLK HIGH (SI) Delay Time		130	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		90	ns
TAFC	$\overline{READ}$ or $\overline{WRITE}$ Float from CLK HIGH		120	ns
TAFDB	DB Active to Float Delay from CLK HIGH		170	ns
TAHR	ADR from $\overline{READ}$ HIGH Hold Time	TCY-100		ns
TAHS	DB from ADSTB LOW Hold Time	30		ns
TAHW	ADR from $\overline{WRITE}$ HIGH Hold Time	TCY-50		ns
TAK	DACK Valid from CLK LOW Delay Time (Note 3)		170	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time (Note 4)		170	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time		170	ns
TASM	ADR Stable from CLK HIGH		170	ns
TASS	DB to ADSTB LOW Setup Time	100		ns
TCH	Clock High Time (Transitions ≤ 10 ns)	68		ns
TCL	Clock LOW Time (Transitions ≤ 10 ns) Auto Initialize Enabled	115		ns
TCY	CLK Cycle Time	200		ns
TDCL	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay (Note 2)		190	ns
TDCTR	$\overline{READ}$ HIGH from CLK HIGH (S4) Delay Time (Note 2)		190	ns
TDCTW	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay Time (Note 2)		130	ns
TDQ1	HRQ Valid from CLK HIGH Delay Time		120	ns
TEPS	$\overline{EOP}$ LOW from CLK LOW Setup Time	40		ns
TEPW	$\overline{EOP}$ Pulse Width	220		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		170	ns
TFAC	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH		150	ns
TFADB	DB Float to Active Delay from CLK HIGH		200	ns
THS	HLDA Valid to CLK HIGH Setup Time	75		ns
TIDH	Input Data from $\overline{MEMR}$ HIGH Hold Time	0		ns
TIDS	Input Data to $\overline{MEMR}$ HIGH Setup Time	170		ns
TODH	Output Data from $\overline{MEMW}$ HIGH Hold Time	10		ns
TODV	Output Data Valid to $\overline{MEMW}$ HIGH	125		ns
TQS	DREQ to CLK LOW (SI, S4) Setup Time (Note 3)	0		ns
TRH	CLK to READY LOW Hold Time	20		ns
TRS	READY to CLK LOW Setup Time	60		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		130	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		90	ns

A.C. CHARACTERISTICS—PERIPHERAL (SLAVE) MODE

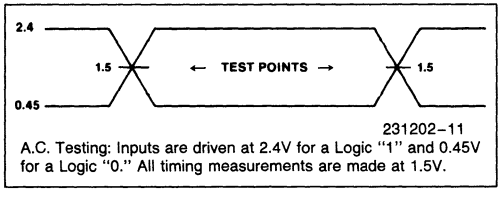
T_A = 0°C to 70°C, T_{CASE} = 0°C to 75°C, V_{CC} = +5V ±5%, GND = 0V

Symbol	Parameter	Min	Max	Unit
TAR	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50		ns
TAW	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	130		ns
TCW	CS LOW to $\overline{WRITE}$ HIGH Setup Time	130		ns
TDW	Data Valid to $\overline{WRITE}$ HIGH Setup Time	130		ns
TRA	ADR or CS Hold from $\overline{READ}$ HIGH	0		ns
TRDE	Data Access from $\overline{READ}$ LOW		140	ns
TRDF	DB Float Delay from $\overline{READ}$ HIGH	0	70	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		ns
TRSTS	RESET to First $\overline{IOWR}$	2TCY		ns
TRSTW	RESET Pulse Width	300		ns
TRW	$\overline{READ}$ Width	200		ns
TWA	ADR from $\overline{WRITE}$ HIGH Hold Time	20		ns
TWC	CS HIGH from $\overline{WRITE}$ HIGH Hold Time	20		ns
TWD	Data from $\overline{WRITE}$ HIGH Hold Time	30		ns
TWWS	Write Width	160		ns

NOTES:
1. Input frequency 5 MHz, when RESET, V_{IN} = 0V/V_{CC}, C_L = 0 pF.
2. The net $\overline{IOW}$ or $\overline{MEMW}$ Pulse width for normal write will be TCY-100 ns and for extended write will be 2TCY-100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY-50 ns and for compressed read will be TCY-50 ns.
3. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode for DREQ and active low for DACK.
4. $\overline{EOP}$ is an open collector output. This parameter assumes the presence of a 2.2K pullup to V_{CC}.

5

A.C. TESTING INPUT/OUTPUT WAVEFORM



231202-11

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." All timing measurements are made at 1.5V.

WAVEFORMS

SLAVE MODE WRITE TIMING

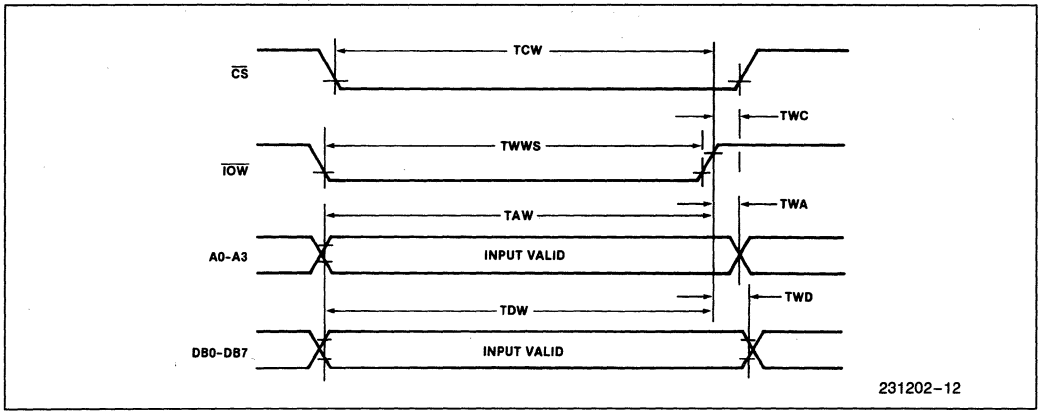


Figure 9. Slave Mode Write

SLAVE MODE READ TIMING

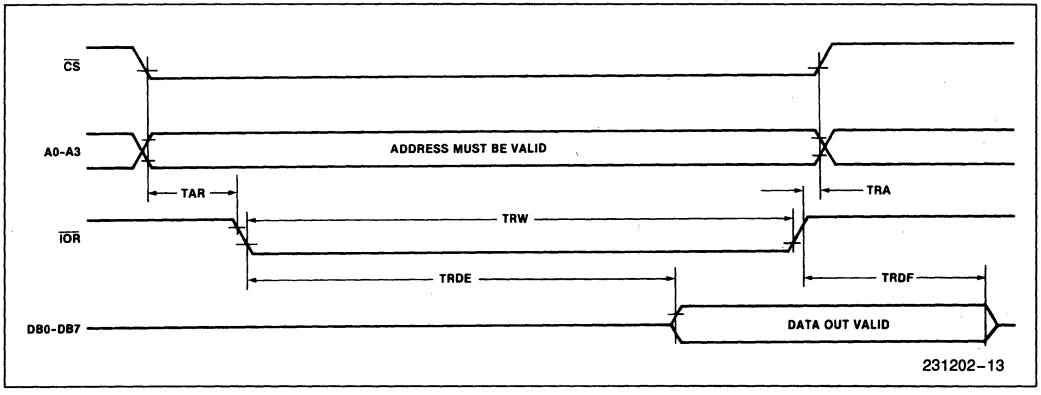


Figure 10. Slave Mode Read

WAVEFORMS (Continued)

DMA TRANSFER TIMING

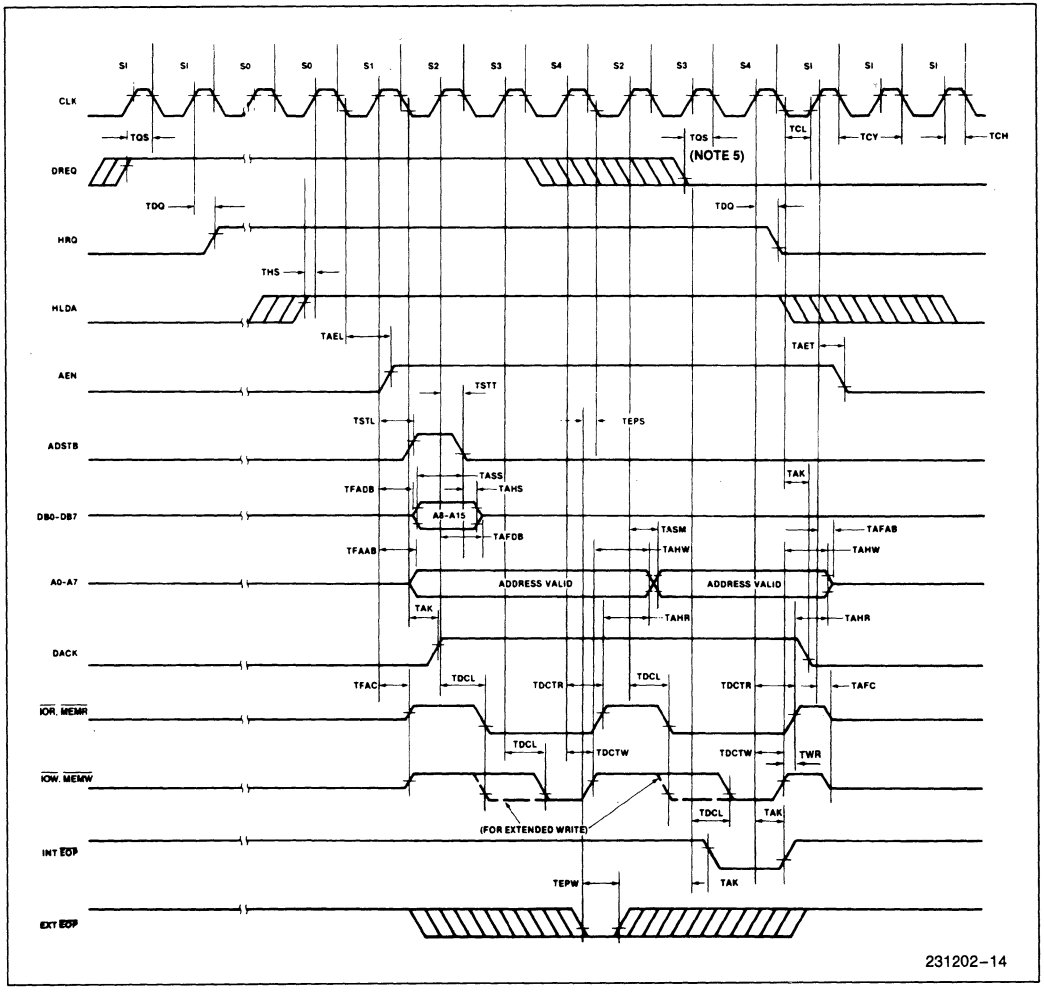


Figure 11. DMA Transfer

WAVEFORMS (Continued)

MEMORY-TO-MEMORY TRANSFER TIMING

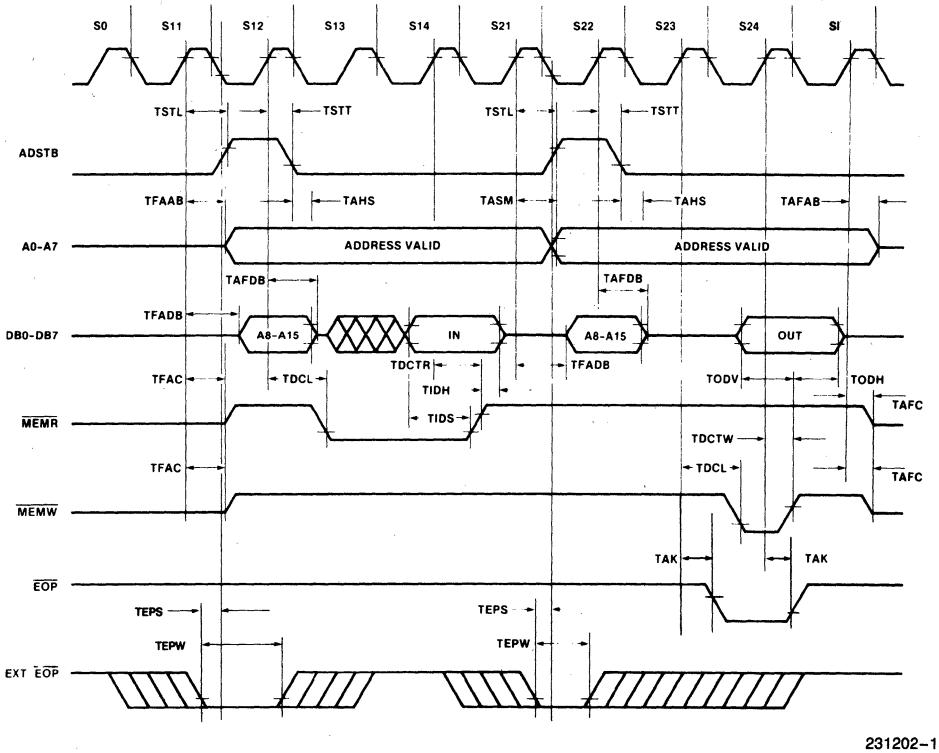


Figure 12. Memory-to-Memory Transfer

READY TIMING

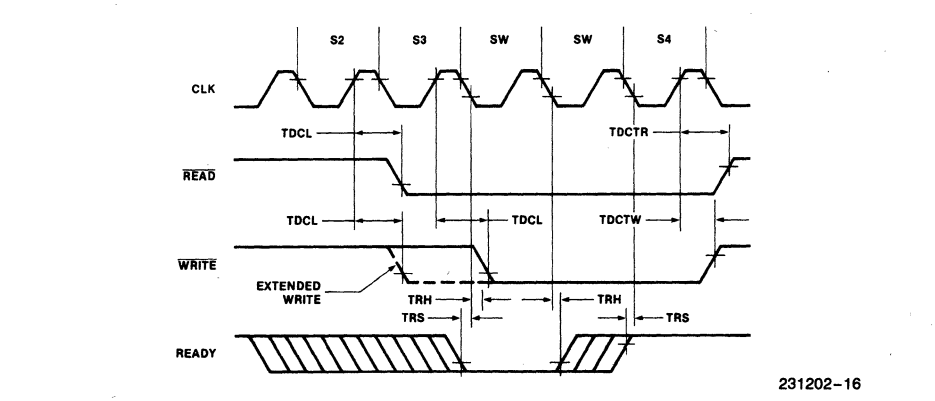


Figure 13. Ready

WAVEFORMS (Continued)

COMPRESSED TRANSFER TIMING

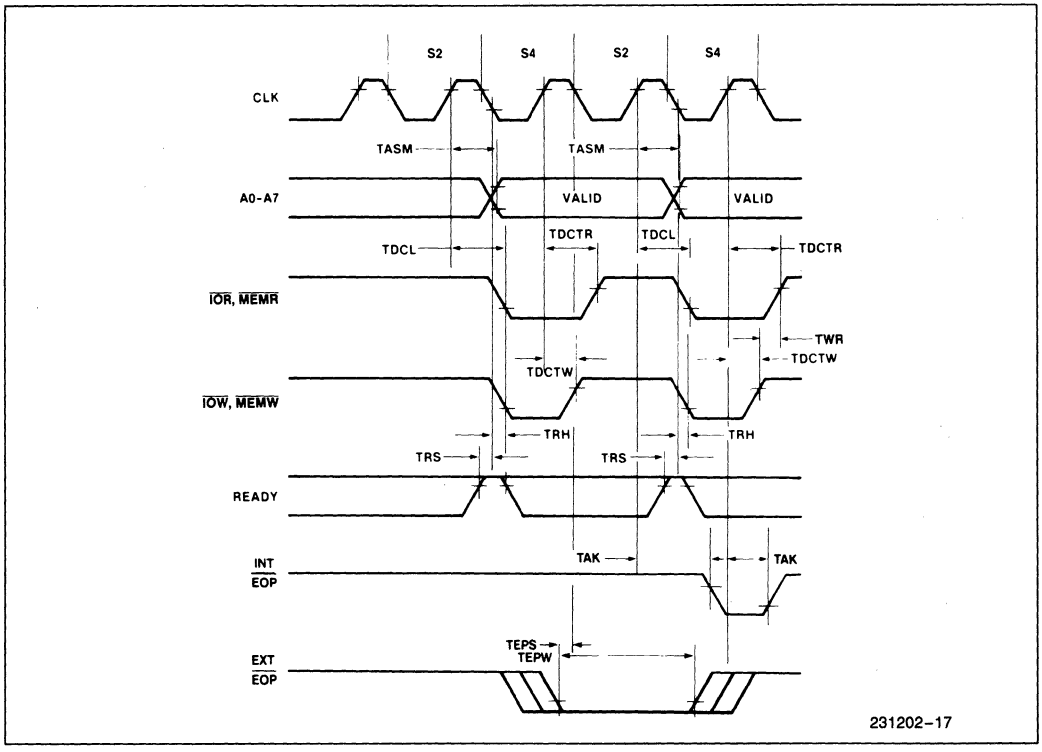


Figure 14. Compressed Transfer

RESET TIMING

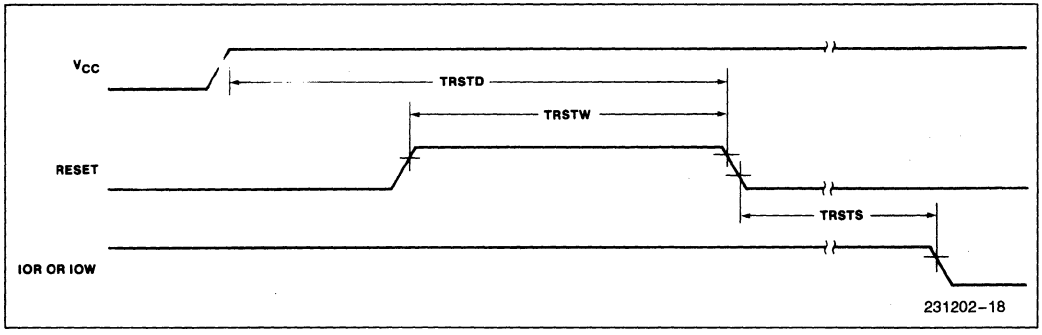


Figure 15. Reset

DATA SHEET REVISION REVIEW

The following list represents key differences between this and the -004 data sheet. Please review this summary carefully.

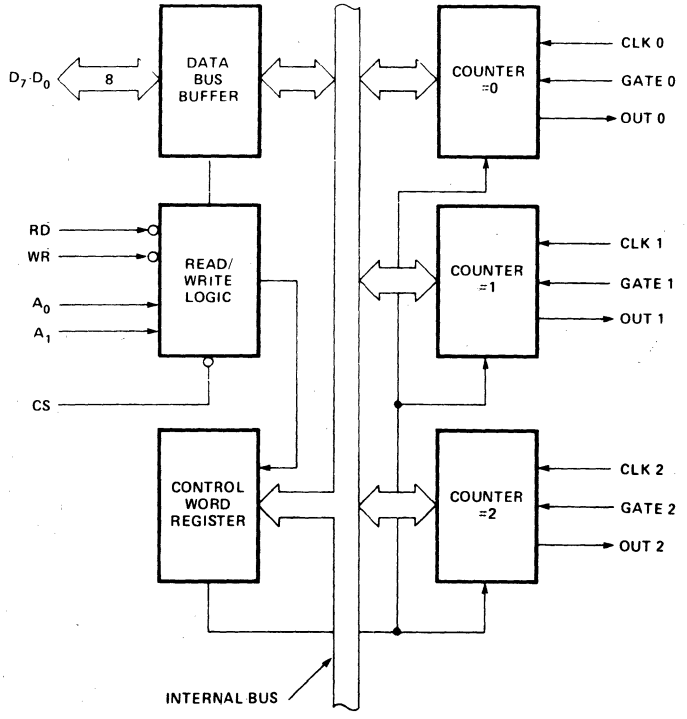
1. The "PRELIMINARY" markings have been removed from the data sheet. The 82C37A-5 is no longer a preliminary part.
2. A section of the Functional Description describing 82C37A-5 operation with the 8085 CPU has been deleted.

8253/8253-5
PROGRAMMABLE INTERVAL TIMER

- **MCS-85 Compatible 8253-5**
- **3 Independent 16-Bit Counters**
- **DC to 2.6 MHz**
- **Programmable Counter Modes**
- **Count Binary or BCD**
- **Single +5V Supply**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

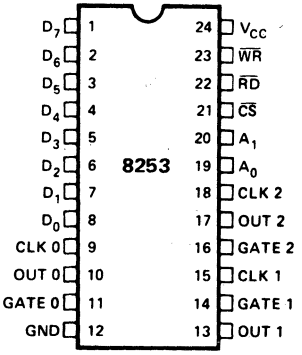
The Intel 8253 is a programmable counter/timer device designed for use as an Intel microcomputer peripheral. It uses NMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2.6 MHz. All modes of operation are software programmable.



231306-1

Figure 1. Block Diagram



231306-2

Figure 2. Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

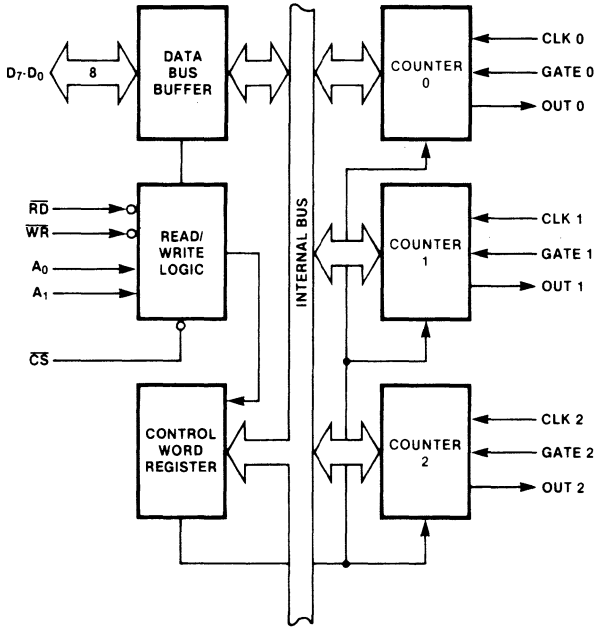
November 1986
Order Number: 231306-001

8254
PROGRAMMABLE INTERVAL TIMER

- **Compatible with All Intel and Most Other Microprocessors**
- **Handles Inputs from DC to 10 MHz**
  - **— 8 MHz 8254**
  - **— 10 MHz 8254-2**
- **Status Read-Back Command**
- **Six Programmable Counter Modes**
- **Three Independent 16-Bit Counters**
- **Binary or BCD Counting**
- **Single +5V Supply**
- **Available in EXPRESS**
  - **— Standard Temperature Range**

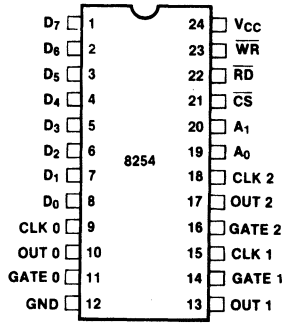
The Intel 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 8254 is a superset of the 8253.

The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package.



231164-1

Figure 1. 8254 Block Diagram



231164-2

Figure 2. Pin Configuration

5

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1993
Order Number: 231164-005

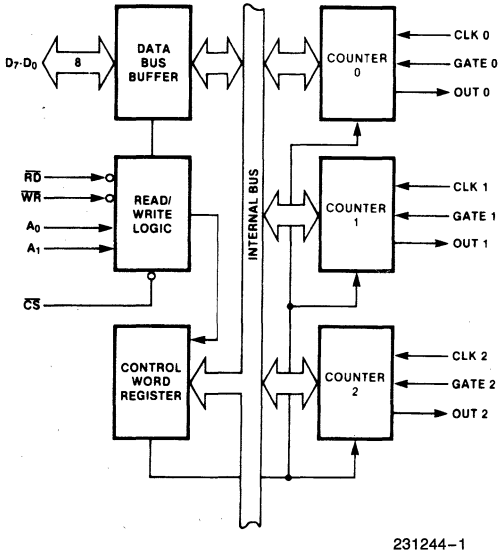
82C54
CHMOS PROGRAMMABLE INTERVAL TIMER

- **Compatible with all Intel and most other microprocessors**
- **High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188**
- **Handles Inputs from DC — 10 MHz for 82C54-2**
- **Available in EXPRESS — Standard Temperature Range — Extended Temperature Range**
- **Three independent 16-bit counters**
- **Low Power CHMOS — I_{CC} = 10 mA @ 8 MHz Count frequency**
- **Completely TTL Compatible**
- **Six Programmable Counter Modes**
- **Binary or BCD counting**
- **Status Read Back Command**
- **Available in 24-Pin DIP and 28-Pin PLCC**

The Intel 82C54 is a high-performance, CHMOS version of the industry standard 8254 counter/timer which is designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 82C54 is pin compatible with the HMOS 8254, and is a superset of the 8253.

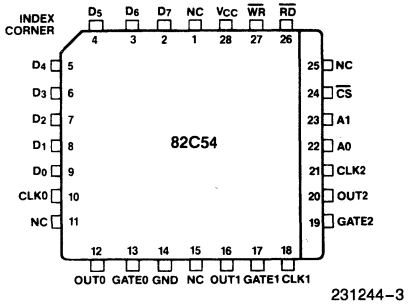
Six programmable timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, and in many other applications.

The 82C54 is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent HMOS product. The 82C54 is available in 24-pin DIP and 28-pin plastic leaded chip carrier (PLCC) packages.



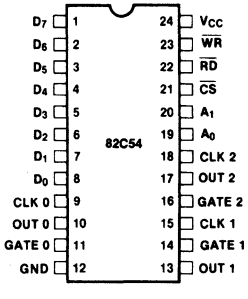
231244-1

Figure 1. 82C54 Block Diagram



231244-3

PLASTIC LEADED CHIP CARRIER



231244-2

Diagrams are for pin reference only.
Package sizes are not to scale.

Figure 2. 82C54 Pinout

October 1994
Order Number: 231244-006

Table 1. Pin Description

Symbol	Pin Number		Type	Function
	DIP	PLCC		
D_7-D_0	1-8	2-9	I/O	Data: Bidirectional tri-state data bus lines, connected to system data bus.
CLK 0	9	10	I	Clock 0: Clock input of Counter 0.
OUT 0	10	12	O	Output 0: Output of Counter 0.
GATE 0	11	13	I	Gate 0: Gate input of Counter 0.
GND	12	14		Ground: Power supply connection.
OUT 1	13	16	O	Out 1: Output of Counter 1.
GATE 1	14	17	I	Gate 1: Gate input of Counter 1.
CLK 1	15	18	I	Clock 1: Clock input of Counter 1.
GATE 2	16	19	I	Gate 2: Gate input of Counter 2.
OUT 2	17	20	O	Out 2: Output of Counter 2.
CLK 2	18	21	I	Clock 2: Clock input of Counter 2.
A_1, A_0	20-19	23-22	I	Address: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.
				A_1 / **A_0** / **Selects** 0 / 0 / Counter 0 0 / 1 / Counter 1 1 / 0 / Counter 2 1 / 1 / Control Word Register
$\overline{CS}$	21	24	I	Chip Select: A low on this input enables the 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	26	I	Read Control: This input is low during CPU read operations.
$\overline{WR}$	23	27	I	Write Control: This input is low during CPU write operations.
V_{CC}	24	28		Power: +5V power supply connection.
NC		1, 11, 15, 25		No Connect

5

FUNCTIONAL DESCRIPTION

General

The 82C54 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Even counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Block Diagram

DATA BUS BUFFER

This 3-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 3).

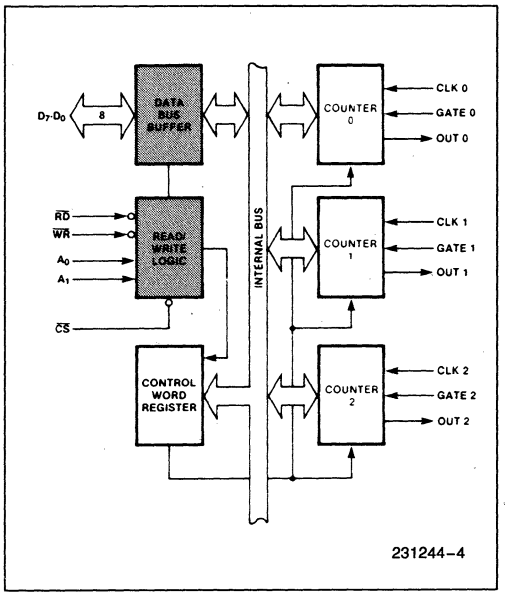


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

READ/WRITE LOGIC

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A_1 and A_0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the 82C54 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the 82C54 has been selected by holding $\overline{CS}$ low.

The WR# and CLK signals should be synchronous. This is accomplished by using a CLK input signal to the 82C54 counters which is a derivative of the system clock source. Another technique is to externally synchronize the WR# and CLK input signals. This is done by gating WR# with CLK.

CONTROL WORD REGISTER

The Control Word Register (see Figure 4) is selected by the Read/Write Logic when A_1, A_0 = 11. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

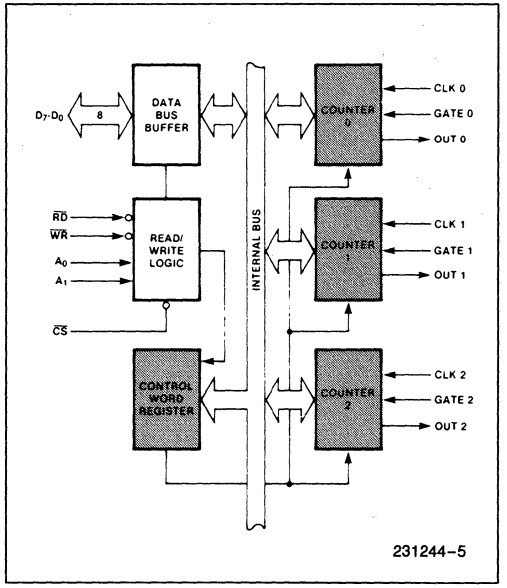


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

COUNTER 0, COUNTER 1, COUNTER 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 5.

The Counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

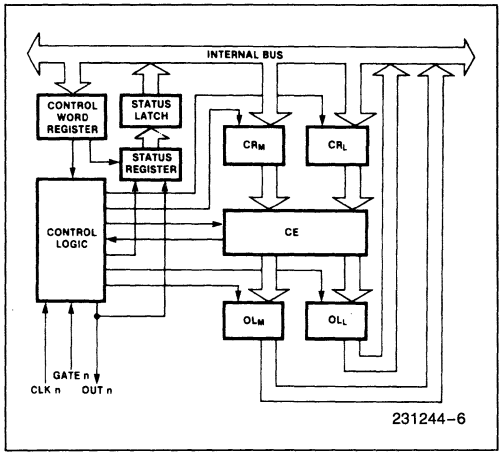


Figure 5. Internal Block Diagram of a Counter

The status register, shown in the Figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labelled CE (for "Counting Element"). It is a 16-bit presettable synchronous down counter.

OL_M and OL_L are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L stand for "Most significant byte" and "Least significant byte" respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CR_M and CR_L (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR_M and CR_L are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

82C54 SYSTEM INTERFACE

The 82C54 is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.

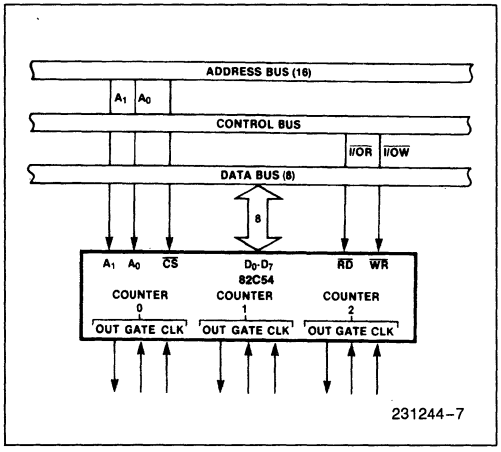


Figure 6. 82C54 System Interface

OPERATIONAL DESCRIPTION

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the 82C54

Counters are programmed by writing a Control Word and then an initial count. The control word format is shown in Figure 7.

All Control Words are written into the Control Word Register, which is selected when A_1, A_0 = 11. The Control Word itself specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A_1, A_0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Control Word Format

A_1, A_0 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW — Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 7. Control Word Format

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1) For each Counter, the Control Word must be written before the initial count is written.
2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A_1, A_0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

		A_1	A_0
Control Word —	Counter 0	1	1
LSB of count —	Counter 0	0	0
MSB of count —	Counter 0	0	0
Control Word —	Counter 1	1	1
LSB of count —	Counter 1	0	1
MSB of count —	Counter 1	0	1
Control Word —	Counter 2	1	1
LSB of count —	Counter 2	1	0
MSB of count —	Counter 2	1	0

		A_1	A_0
Control Word —	Counter 2	1	1
Control Word —	Counter 1	1	1
Control Word —	Counter 0	1	1
LSB of count —	Counter 2	1	0
MSB of count —	Counter 2	1	0
LSB of count —	Counter 1	0	1
MSB of count —	Counter 1	0	1
LSB of count —	Counter 0	0	0
MSB of count —	Counter 0	0	0

		A_1	A_0
Control Word —	Counter 0	1	1
Counter Word —	Counter 1	1	1
Control Word —	Counter 2	1	1
LSB of count —	Counter 2	1	0
LSB of count —	Counter 1	0	1
LSB of count —	Counter 0	0	0
MSB of count —	Counter 0	0	0
MSB of count —	Counter 1	0	1
MSB of count —	Counter 2	1	0

		A_1	A_0
Control Word —	Counter 1	1	1
Control Word —	Counter 0	1	1
LSB of count —	Counter 1	0	1
Control Word —	Counter 2	1	1
LSB of count —	Counter 0	0	0
MSB of count —	Counter 1	0	1
LSB of count —	Counter 2	1	0
MSB of count —	Counter 0	0	0
MSB of count —	Counter 2	1	0

NOTE:
In all four examples, all counters are programmed to read/write two-byte counts.
These are only four of many possible programming sequences.

Figure 8. A Few Possible Programming Sequences

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the counters: a simple read operation, the Counter Latch Command, and the Read-Back Command. Each is explained below. The first method is to perform a simple read operation. To read the Counter, which is selected with the A1, A0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

COUNTER LATCH COMMAND

The second method uses the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A_1, A_0 = 11. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

A_1, A_0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5,D4 - 00 designates Counter Latch Command

X - don't care

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 9. Counter Latching Command Format

The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until it is read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read/write two-byte counts, the following precaution applies; A program must not transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

READ-BACK COMMAND

The third method uses the Read-Back command. This command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 10. The command applies to the counters selected by setting their corresponding bits D3,D2,D1 = 1.

A0, A1 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D_5: 0 = Latch count of selected counter(s)
D_4: 0 = Latch status of selected counter(s)
D_3: 1 = Select counter 2
D_2: 1 = Select counter 1
D_1: 1 = Select counter 0
D_0: Reserved for future expansion; must be 0

Figure 10. Read-Back Command Format

The read-back command may be used to latch multiple counter output latches (OL) by setting the $\overline{COUNT}$ bit D5 = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the

count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting $\overline{\text{STATUS}}$ bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 11. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D_7 1 = Out Pin is 1
0 = Out Pin is 0
D_6 1 = Null count
0 = Count available for reading
D_5-D_0 Counter Programmed Mode (See Figure 7)

Figure 11. Status Byte

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 12.

THIS ACTION:	CAUSES:
A. Write to the control word register:[1]	Null count = 1
B. Write to the count register (CR);[2]	Null count = 1
C. New count is loaded into CE (CR → CE);	Null count = 0

[1] Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

[2] If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

Figure 12. Null Count Operation

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both $\overline{\text{COUNT}}$ and $\overline{\text{STATUS}}$ bits D5,D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 13.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

Command								Description	Results
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 13. Read-Back Command Example

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 14. Read/Write Operations Summary

Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE: a rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER: a rising edge of a Counter's GATE input.

COUNTER LOADING: the transfer of a count from the CR to the CE (refer to the "Functional Description")

MODE 0: INTERRUPT ON TERMINAL COUNT

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

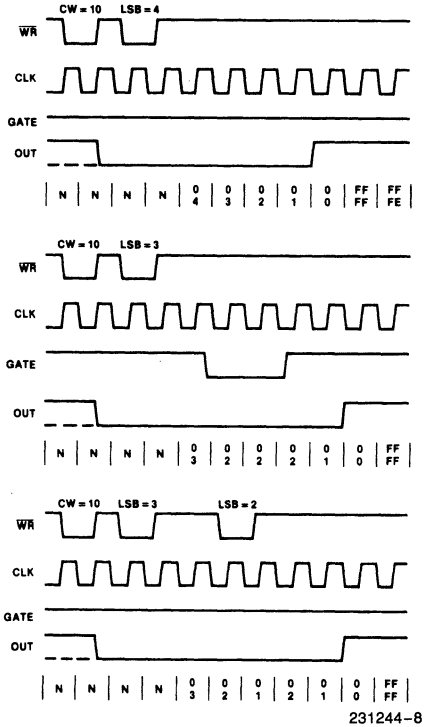
After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte does not disable counting. OUT is set low immediately (no clock pulse required).
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.
3) When there is a count in progress, writing a new LSB before the counter has counted down to 0 and rolled over to FFFFh, WILL stop the counter. However, if the LSB is loaded AFTER the counter has rolled over to FFFFh, so that an MSB now exists in the counter, then the counter WILL NOT stop.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.



NOTE:
The Following Conventions Apply To All Mode Timing Diagrams:
1. Counters are programmed for binary (not BCD) counting and for Reading/Writing least significant byte (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB stands for "Least Significant Byte" of count.
5. Numbers below diagrams are count values.
The lower number is the least significant byte.
The upper number is the most significant byte. Since the counter is programmed to Read/Write LSB only, the most significant byte cannot be read.
N stands for an undefined count.
Vertical lines show transitions between count values.

Figure 15. Mode 0

MODE 1: HARDWARE RETRIGGERABLE ONE-SHOT

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

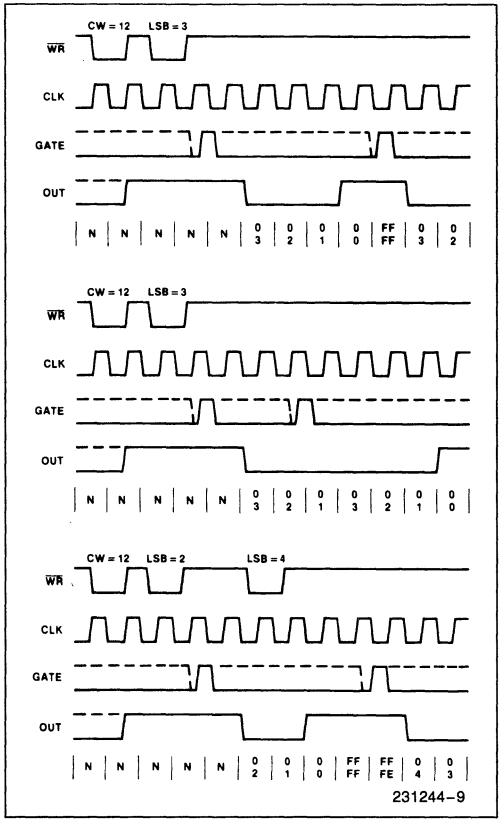


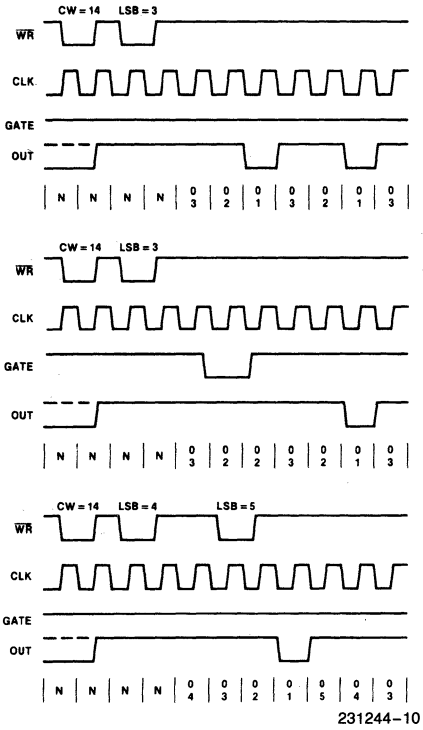
Figure 16. Mode 1

MODE 2: RATE GENERATOR

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.



NOTE:
A GATE transition should not occur one clock prior to terminal count.

Figure 17. Mode 2

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

MODE 3: SQUARE WAVE MODE

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

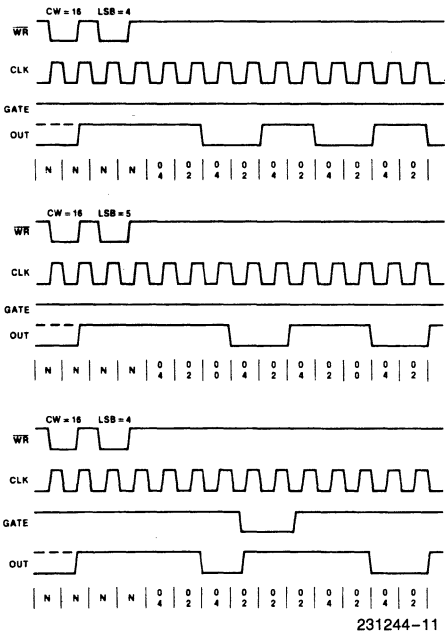
Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse *after* the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts,

OUT will be high for (N + 1)/2 counts and low for (N −1)/2 counts.



NOTE:
A GATE transition should not occur one clock prior to terminal count.

Figure 18. Mode 3

MODE 4: SOFTWARE TRIGGERED STROBE

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N+1 CLK pulses after the new count of N is written.

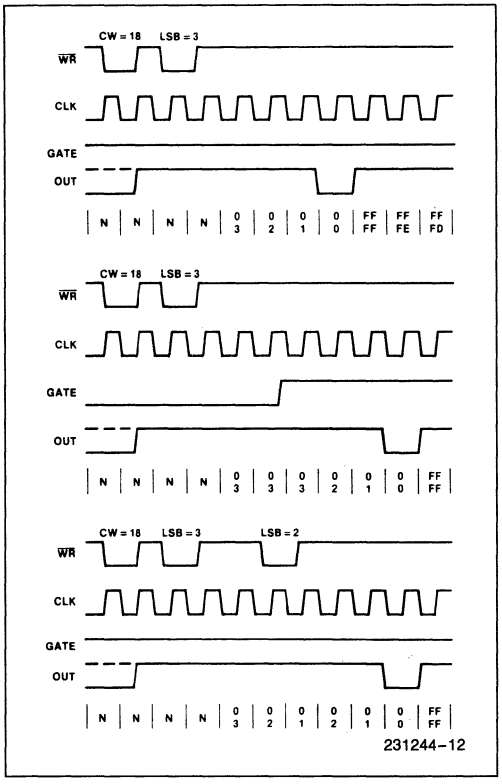


Figure 19. Mode 4

MODE 5: HARDWARE TRIGGERED STROBE (RETRIGGERABLE)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

5

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

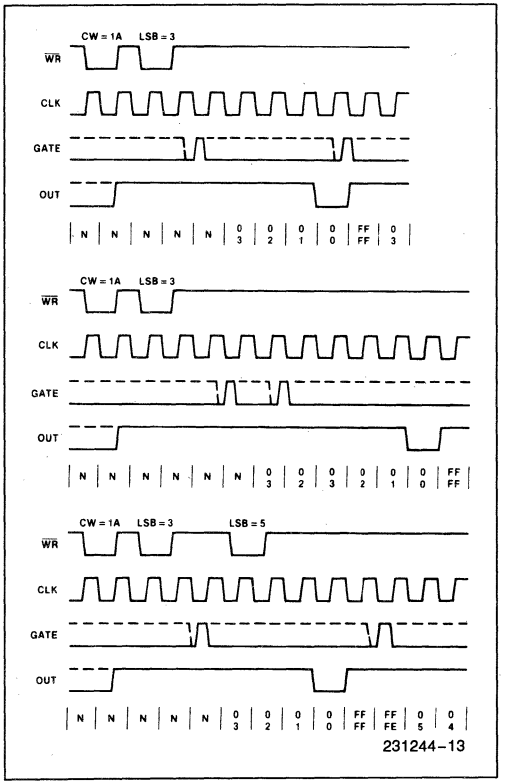


Figure 20. Mode 5

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

Figure 21. Gate Pin Operations Summary

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0

NOTE:
0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting

Figure 22. Minimum and Maximum initial Counts

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

GATE

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK; the flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs—a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive. In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following $\overline{WR}$ of a new count value.

COUNTER

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4, and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias.....0°C to 70°C
Storage Temperature .....−65° to +150°C
Supply Voltage .....−0.5 to +8.0V
Operating Voltage .....+4V to +7V
Voltage on any Input.....GND −2V to +6.5V
Voltage on any Output ..GND−0.5V to V_{CC} + 0.5V
Power Dissipation .....1 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V± 10%, GND=0V) (T_A = −40°C to +85°C for Extended Temperature)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	3.0 V_{CC} − 0.4		V V	I_{OH} = −2.5 mA I_{OH} = −100 μA
I_{IL}	Input Load Current		±2.0	μA	V_{IN}=V_{CC} to 0V
I_{OFL}	Output Float Leakage Current		±10	μA	V_{OUT}=V_{CC} to 0.0V
I_{CC}	V_{CC} Supply Current		20	mA	Clk Freq= 8MHz 82C54 10MHz 82C54-2
I_{CCSB}	V_{CC} Supply Current-Standby		10	μA	CLK Freq = DC $\overline{CS}$ = V_{CC}. All Inputs/Data Bus V_{CC} All Outputs Floating
I_{CCSB1}	V_{CC} Supply Current-Standby		150	μA	CLK Freq = DC $\overline{CS}$ = V_{CC}. All Other Inputs, I/O Pins = V_{GND}, Outputs Open
C_{IN}	Input Capacitance		10	pF	f_c = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND(5)
C_{OUT}	Output Capacitance		20	pF	

A.C. CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V ±10%, GND =0V) (T_A = −40°C to +85°C for Extended Temperature)

BUS PARAMETERS (Note 1)

READ CYCLE

Symbol	Parameter	82C54-2		Units
		Min	Max	
t_{AR}	Address Stable Before $\overline{RD}$ ↓	30		ns
t_{SR}	$\overline{CS}$ Stable Before $\overline{RD}$ ↓	0		ns
t_{RA}	Address Hold Time After $\overline{RD}$ ↑	0		ns
t_{RR}	$\overline{RD}$ Pulse Width	95		ns
t_{RD}	Data Delay from $\overline{RD}$ ↓		85	ns
t_{AD}	Data Delay from Address		185	ns
t_{DF}	$\overline{RD}$ ↑ to Data Floating	5	65	ns
t_{RV}	Command Recovery Time	165		ns

NOTE:
1. AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V.

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

Symbol	Parameter	82C54-2		Units
		Min	Max	
t_{AW}	Address Stable Before $\overline{WR}\downarrow$	0		ns
t_{SW}	$\overline{CS}$ Stable Before $\overline{WR}\downarrow$	0		ns
t_{WA}	Address Hold Time After $\overline{WR}\uparrow$	0		ns
t_{WW}	$\overline{WR}$ Pulse Width	95		ns
t_{DW}	Data Setup Time Before $\overline{WR}\uparrow$	95		ns
t_{WD}	Data Hold Time After $\overline{WR}\uparrow$	0		ns
t_{RV}	Command Recovery Time	165		ns

CLOCK AND GATE

Symbol	Parameter	82C54-2		Units
		Min	Max	
t_{CLK}	Clock Period	100	DC	ns
t_{PWH}	High Pulse Width	30(3)		ns
t_{PWL}	Low Pulse Width	50(3)		ns
T_R	Clock Rise Time		25	ns
t_F	Clock Fall Time		25	ns
t_{GW}	Gate Width High	50		ns
t_{GL}	Gate Width Low	50		ns
t_{GS}	Gate Setup Time to CLK $\uparrow$	40		ns
t_{GH}	Gate Hold Time After CLK $\uparrow$	50(2)		ns
T_{OD}	Output Delay from CLK $\downarrow$		100	ns
t_{ODG}	Output Delay from Gate $\downarrow$		100	ns
t_{WC}	CLK Delay for Loading(4)	0	55	ns
t_{WG}	Gate Delay for Sampling(4)	−5	40	ns
t_{WO}	OUT Delay from Mode Write		240	ns
t_{CL}	CLK Set Up for Count Latch	−40	40	ns

NOTES:
2. In Modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 70 ns for the 82C54-2 of the rising clock edge may not be detected.
3. Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.
4. Except for Extended Temp., See Extended Temp. A.C. Characteristics below.
5. Sampled not 100% tested. $T_A = 25°C$.
6. If CLK present at T_{WC} min then Count equals N+2 CLK pulses, T_{WC} max equals Count N+1 CLK pulse. T_{WC} min to T_{WC} max, count will be either N+1 or N+2 CLK pulses.
7. In Modes 1 and 5, if GATE is present when writing a new Count value, at T_{WG} min Counter will not be triggered, at T_{WG} max Counter will be triggered.
8. If CLK present when writing a Counter Latch or ReadBack Command, at T_{CL} min CLK will be reflected in count value latched, at T_{CL} max CLK will not be reflected in the count value latched. Writing a Counter Latch or ReadBack Command between T_{CL} min and T_{WL} max will result in a latched count vallue which is ± one least significant bit.

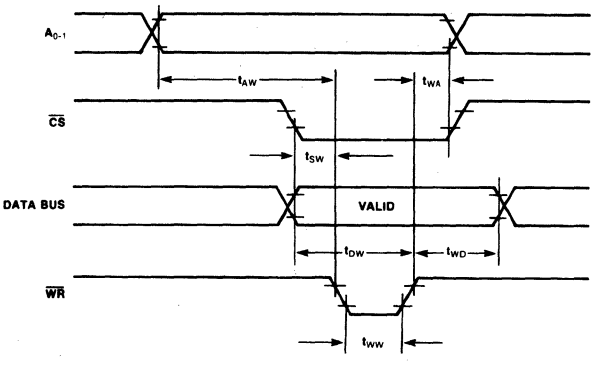
EXTENDED TEMPERATURE ($T_A = -40°C$ to $+85°C$ for Extended Temperature)

Symbol	Parameter	82C54-2		Units
		Min	Max	
t_{WC}	CLK Delay for Loading	−25	25	ns
t_{WG}	Gate Delay for Sampling	−25	25	ns

5

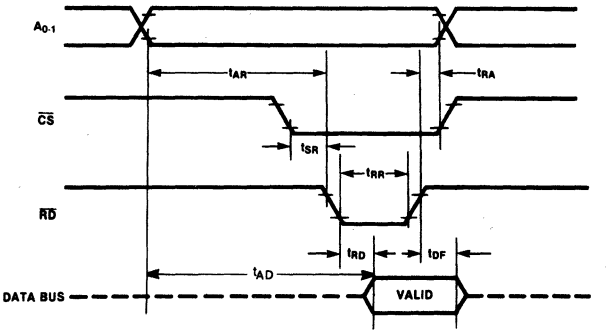
WAVEFORMS

WRITE



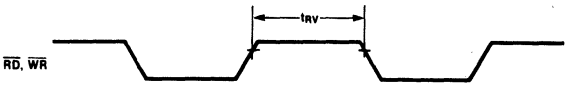
231244-14

READ



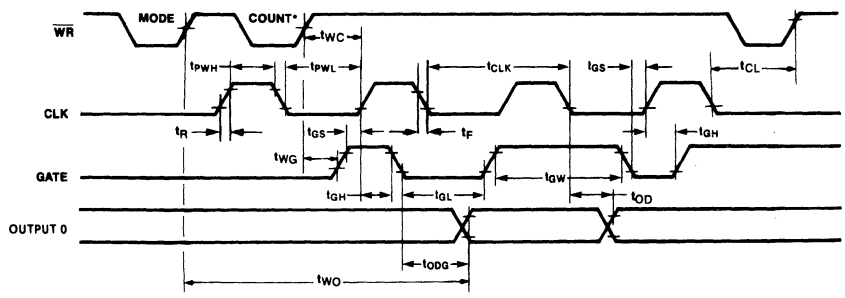
231244-15

RECOVERY



231244-16

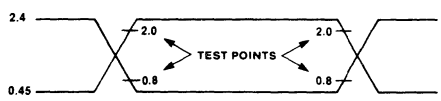
CLOCK AND GATE



231244-17

* Last byte of count being written

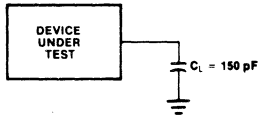
A.C. TESTING INPUT, OUTPUT WAVEFORM



231244-18

A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

A.C. TESTING LOAD CIRCUIT



231244-19

C_L = 150 pF
C_L includes jig capacitance

REVISION SUMMARY

The following list represents the key differences between Rev. 005 and 006 of the 82C54 Data Sheet.

1. References to and specifications for the 8 MHz 82C54 are removed. Only the 10 MHz 82C52-2 remains in production.

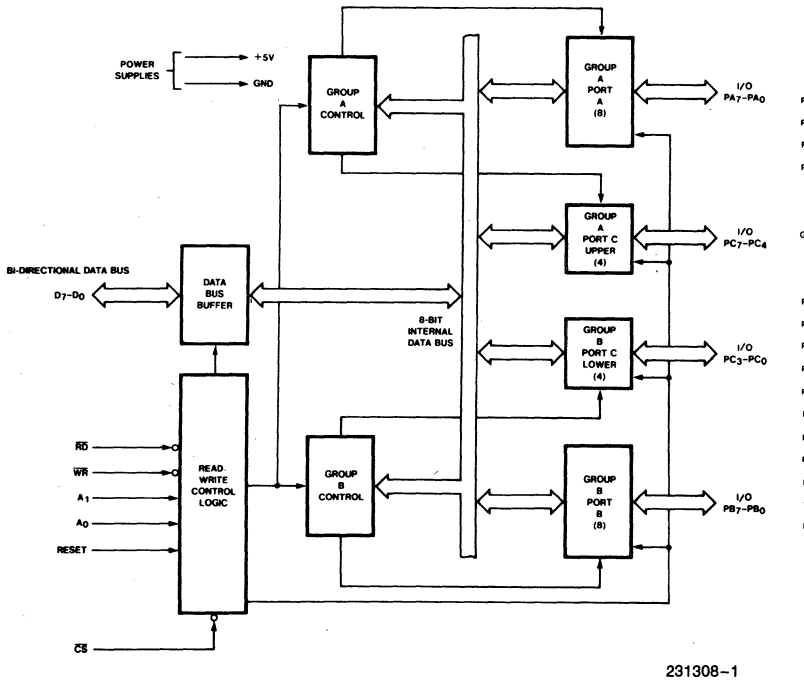
5

8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- **MCS-85 Compatible 8255A-5**
- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with Intel Microprocessor Families**
- **Improved Timing Characteristics**
- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **Reduces System Package Count**
- **Improved DC Driving Capability**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**
- **40 Pin DIP Package**

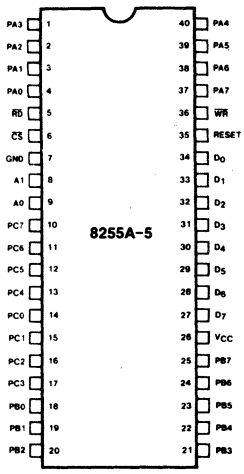
  (See Intel Packaging: Order Number: 240800-001, Package Type P)

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.



231308-1

Figure 1. 8255A Block Diagram



231308-2

Figure 2. Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1993
Order Number: 231308-004

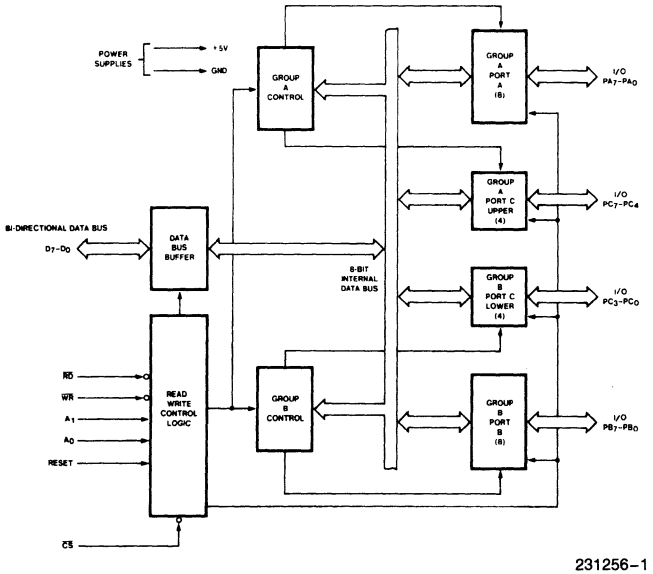
82C55A
CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- **Compatible with all Intel and Most Other Microprocessors**
- **High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188**
- **24 Programmable I/O Pins**
- **Low Power CHMOS**
- **Completely TTL Compatible**
- **Control Word Read-Back Capability**
- **Direct Bit Set/Reset Capability**
- **2.5 mA DC Drive Capability on all I/O Port Outputs**
- **Available in 40-Pin DIP and 44-Pin PLCC**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

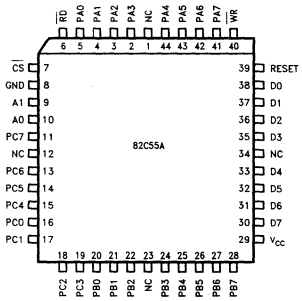
In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.

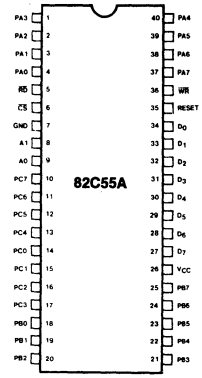


231256-1

Figure 1. 82C55A Block Diagram



231256-31



231256-2

Figure 2. 82C55A Pinout

Diagrams are for pin reference only. Package sizes are not to scale.

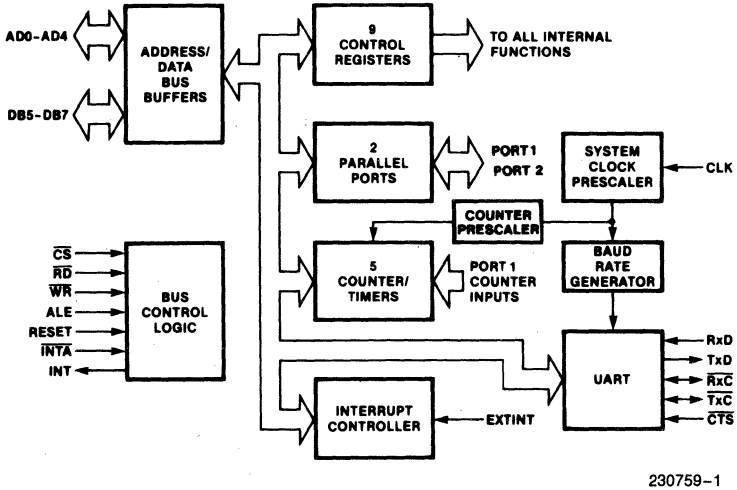
The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1987
Order Number: 231256-004

8256AH
MULTIFUNCTION MICROPROCESSOR SUPPORT CONTROLLER

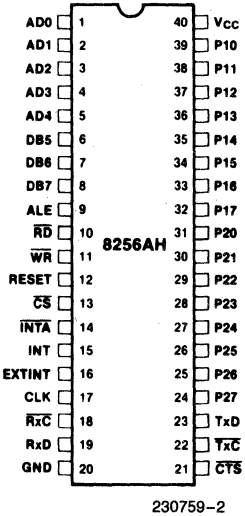
- **Programmable Serial Asynchronous Communications Interface for 5-, 6-, 7-, or 8-Bit Characters, 1, 1½, or 2 Stop Bits, and Parity Generation**
- **On-Board Baud Rate Generator Programmable for 13 Common Baud Rates up to 19.2 KBits/Second, or an External Baud Clock Maximum of 1M Bit/Second**
- **Five 8-Bit Programmable Timer/Counters; Four Can Be Cascaded to Two 16-Bit Timer/Counters**
- **Two 8-Bit Programmable Parallel I/O Ports; Port 1 Can Be Programmed for Port 2 Handshake Controls and Event Counter Inputs**
- **Eight-Level Priority Interrupt Controller Programmable for 8085 or iAPX 86, iAPX 88 Systems and for Fully Nested Interrupt Capability**
- **Programmable System Clock to 1 ×, 2 ×, 3 ×, or 5 × 1.024 MHz**

The Intel 8256AH Multifunction Universal Asynchronous Receiver-Transmitter (MUART) combines five commonly used functions into a single 40-pin device. It is designed to interface to the 8086/88, iAPX 186/188, and 8051 to perform serial communications, parallel I/O, timing, event counting, and priority interrupt functions. All of these functions are fully programmable through nine internal registers. In addition, the five timer/counters and two parallel I/O ports can be accessed directly by the microprocessor.



230759-1

Figure 1. MUART Block Diagram



230759-2

Figure 2. MUART Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

October 1994
Order Number: 230759-002

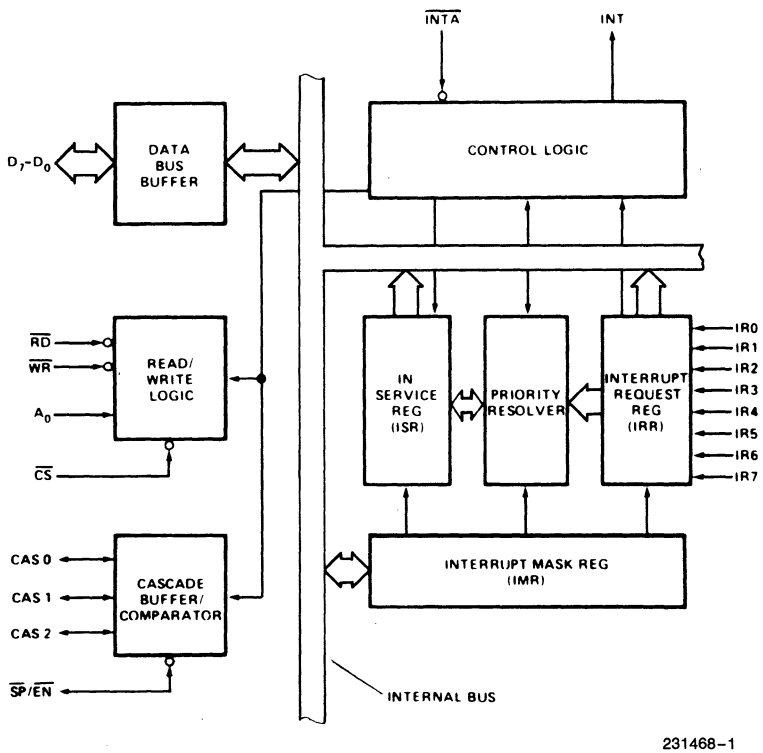
8259A
PROGRAMMABLE INTERRUPT CONTROLLER
(8259A/8259A-2)

- **8086, 8088 Compatible**
- **MCS-80, MCS-85 Compatible**
- **Eight-Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes**
- **Individual Request Mask Capability**
- **Single +5V Supply (No Clocks)**
- **Available in 28-Pin DIP and 28-Lead PLCC Package**
  (See Packaging Spec., Order #231369)
- **Available in EXPRESS**
  — Standard Temperature Range
  — Extended Temperature Range

The Intel 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

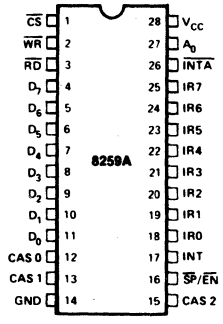
The 8259A is fully upward compatible with the Intel 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).



231468-1

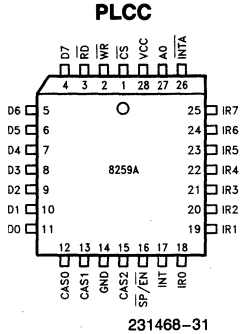
Figure 1. Block Diagram

DIP



231468-2

PLCC



231468-31

Figure 2. Pin Configurations

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

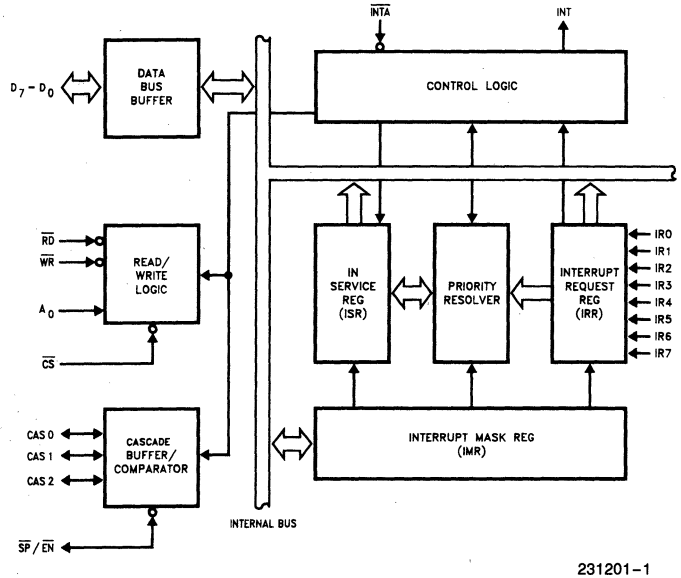
December 1988
Order Number: 231468-003

82C59A-2
CHMOS Programmable Interrupt Controller

- **Pin Compatible with NMOS 8259A-2**
- **Eight-Level Priority Controller**
- **Expandable to 64 levels**
- **Programmable Interrupt Modes**
- **Low Standby Power—10 μA**
- **Individual Request Mask Capability**
- **80C86/88 and 8080/85/86/88 Compatible**
- **Fully Static Design**
- **Single 5V Power Supply**
- **Available in 28-Pin Plastic DIP**
  (See Packaging Spec., Order #231369)

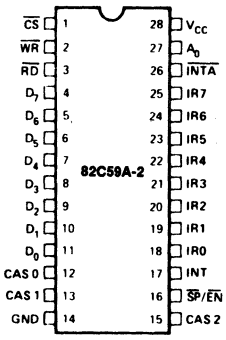
The Intel 82C59A-2 is a high performance CHMOS version of the NMOS 8259A-2 Priority Interrupt Controller. The 82C59A-2 is designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system. The high speed and industry standard configuration of the 82C59A-2, make it compatible with microprocessors such as the 80C86/88, 8086/88 and 8080/85.

The 82C59A-2 can handle up to 8 vectored priority interrupts for the CPU and is cascadable to 64 without additional circuitry. It is designed to minimize the software and real time overhead in handling multi-level priority interrupts. Two modes of operation make the 82C59A-2 optimal for a variety of system requirements. Static CHMOS circuit design, requiring no clock input, insures low operating power. It is packaged in a 28-pin plastic DIP.



231201-1

Figure 1. Block Diagram



231201-2

Figure 2. Pin Configuration

October 1988
Order Number: 231201-004

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	28	I	**SUPPLY:** +5V Supply.
GND	14	I	**GROUND.**
$\overline{CS}$	1	I	**CHIP SELECT:** A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 82C59A-2. INTA functions are independent of CS.
$\overline{WR}$	2	I	**WRITE:** A low on this pin when $\overline{CS}$ is low enables the 82C59A-2 to accept command words from the CPU.
$\overline{RD}$	3	I	**READ:** A low on this pin when $\overline{CS}$ is low enables the 82C59A-2 to release status onto the data bus for the CPU.
D_7–D_0	4–11	I/O	**BIDIRECTIONAL DATA BUS:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0–CAS_2	12, 13, 15	I/O	**CASCADE LINES:** The CAS lines form a private 82C59A-2 bus to control a multiple 82C59A-2 structure. These pins are outputs for a master 82C59A-2 and inputs for a slave 82C59A-2.
$\overline{SP}/\overline{EN}$	16	I/O	**SLAVE PROGRAM/ENABLE BUFFER:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**INTERRUPT:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0–IR_7	18–25	I	**INTERRUPT REQUESTS:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode). Internal pull-up resistors are implemented on IR0–7.
$\overline{INTA}$	26	I	**INTERRUPT ACKNOWLEDGE:** This pin is used to enable 82C59A-2 interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	**AO ADDRESS LINE:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 82C59A-2 to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 80C86, 80C88).

FUNCTIONAL DESCRIPTION

Interrupts in Microcomputer Systems

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

The 82C59A-2

The 82C59A-2 is a device specifically designed for use in real time, interrupt driven microcomputer sys-

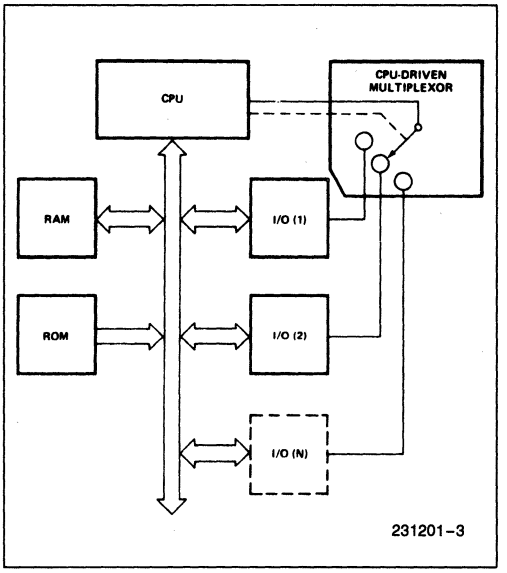


Figure 3a. Polled Method

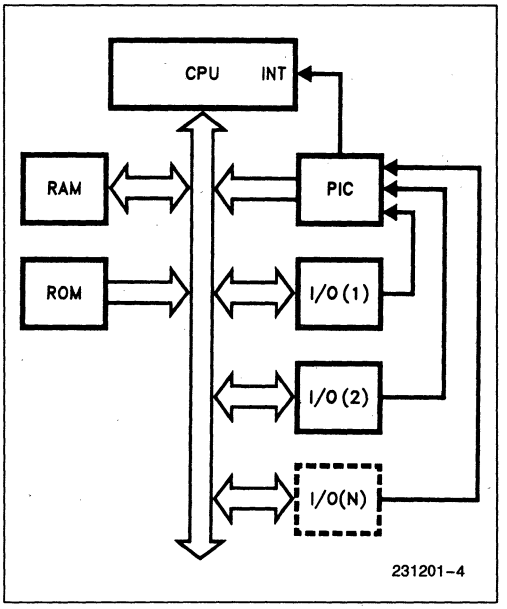


Figure 3b. Interrupt Method

tems. It manages eight levels or requests and has built-in features for expandability to other 82C59A-2's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 82C59A-2 can be configured to match system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A, 80C88 and 80C86 input levels.

$\overline{INTA}$ (INTERRUPT ACKNOWLEDGE)

$\overline{INTA}$ pulses will cause the 82C59A-2 to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 82C59A-2.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 82C59A-2 to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 82C59A-2 to be transferred onto the Data Bus.

$\overline{CS}$ (CHIP SELECT)

A LOW on this input enables the 82C59A-2. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (WRITE)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 82C59A-2.

$\overline{RD}$ (READ)

A LOW on this input enables the 82C59A-2 to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 82C59A-2's used in the system. The associated three I/O pins (CAS0–2) are outputs when the 82C59A-2 is used as a master and are inputs when the 82C59A-2 is used as a slave. As a master, the 82C59A-2 sends the ID of the interrupting slave device onto the CAS0–2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 82C59A-2".)

INTERRUPT SEQUENCE

The powerful features of the 82C59A-2 in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST Lines (IR7–0) are raised high, setting the corresponding IRR bit(s).

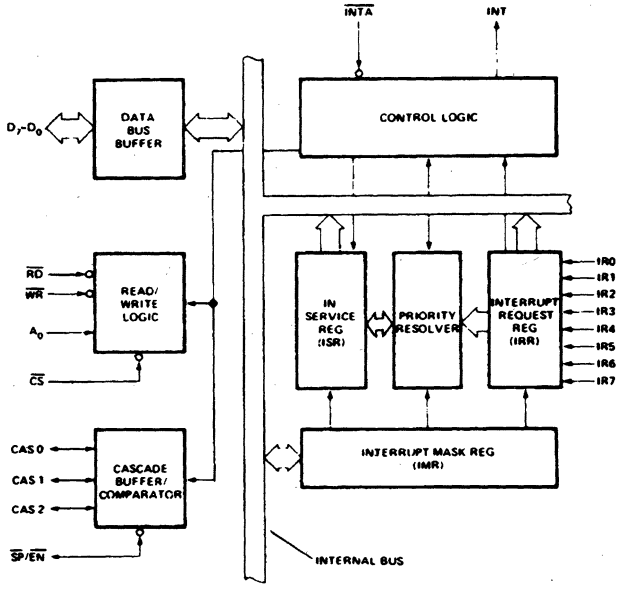


Figure 4. 82C59A-2 Block Diagram

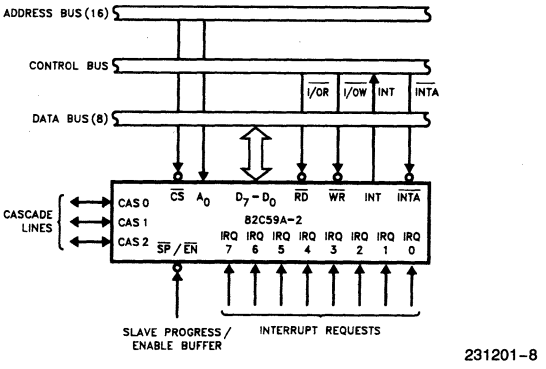


Figure 5. 82C59A-2 Interface to Standard System Bus

2. The 82C59A-2 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 82C59A-2 will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7–0 pins.
5. This CALL instruction will initiate two more $\overline{INTA}$ pulses to be sent to the 82C59A-2 from the CPU group.
6. These two $\overline{INTA}$ pulses allow the 82C59A-2 to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 82C59A-2. In the AEOI mode the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an 80C86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 82C59A-2 does not drive the Data Bus during this cycle.
5. The 80C86 will initiate a second $\overline{INTA}$ pulse. During this pulse, the 82C59A-2 releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt is present at step 4 of either sequence (i.e., the request was too short in duration) the 82C59A-2 will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

When the 82C59A-2 PIC receives an interrupt, INT becomes active and an interrupt acknowledge cycle is started. If a higher priority interrupt occurs between the two INTA pulses, the INT line goes inactive immediately after the second INTA pulse. After an unspecified amount of time the INT line is activated again to signify the higher priority interrupt waiting for service. This inactive time is not specified and can vary between parts. The designer should be aware of this consideration when designing a system which uses the 82C59A-2. It is recommended that proper asynchronous design techniques be followed.

INTERRUPT SEQUENCE OUTPUTS

MCS®-80, MCS-85

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A_5–A_7 are programmed, while A_0–A_4 are automatically inserted by the 82C59A-2. When Interval = 8 only A_6 and A_7 are programmed, while A_0–A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8 – A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

80C86, 80C88

80C86, 80C88 mode is similar to MCS-80 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80, 85 systems in that the 82C59A-2 uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the INTA pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in 80C86, 80C88 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5–A_{11} are unused in 80C86, 80C88 mode):

Content of Interrupt Vector Byte for 80C86, 80C88 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 82C59A-2

The 82C59A-2 accepts two types of command words generated by the CPU:

1. *Initialization Command Words (ICWs)*: Before normal operation can begin, each 82C59A-2 in the system must be brought to a starting point — by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. *Operation Command Words (OCWs)*: These are the command words which command the 82C59A-2 to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 82C59A-2 anytime after initialization.

INITIALIZATION COMMAND WORDS (ICWS)

GENERAL

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR7 input is assigned priority 7.
d. The slave mode address is set to 7.
e. Special Mask Mode is cleared and Status Read is set to IRR.
f. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80, 85 system).

***NOTE:**
Master/Slave in ICW4 is only used in the buffered mode.

INITIALIZATION COMMAND WORDS 1 AND 2 (ICW1, ICW2)

A_5–A_{15}: *Page starting address of service routines.* In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0–A_{15}). When the routine interval is 4, A_0–A_4 are automatically inserted by the 82C59A-2, while A_5–A_{15} are programmed externally. When the routine interval is 8, A_0–A_5 are automatically inserted by the 82C59A-2, while A_6–A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an 80C86, 80C88 system A_{15}–A_{11} are inserted in the five most significant bits of the vectoring

byte and the 82C59A-2 sets the three least significant bits according to the interrupt level. $A_{10}-A_5$ are ignored and ADI (Address Interval) has no effect:

LTIM: If LTIM = 1, then the 82C59A-2 will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 82C59A-2 in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 82C59A-2 in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 80C86, 80C88 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$ = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 80C86, 80C88 are released by it on the Data Bus.

INITIALIZATION COMMAND WORD 4 (ICW4)

SFNM: If SFNM = 1 the special fully nested mode is programmed.

BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 82C59A-2 is programmed to be a master, M/S = 0 means the 82C59A-2 is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 82C59A-2 for MCS-80, 85 system operation, μPM = 1 sets the 82C59A-2 for 80C86 system operation.

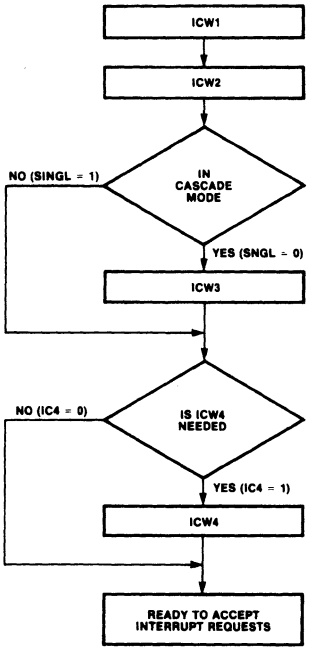
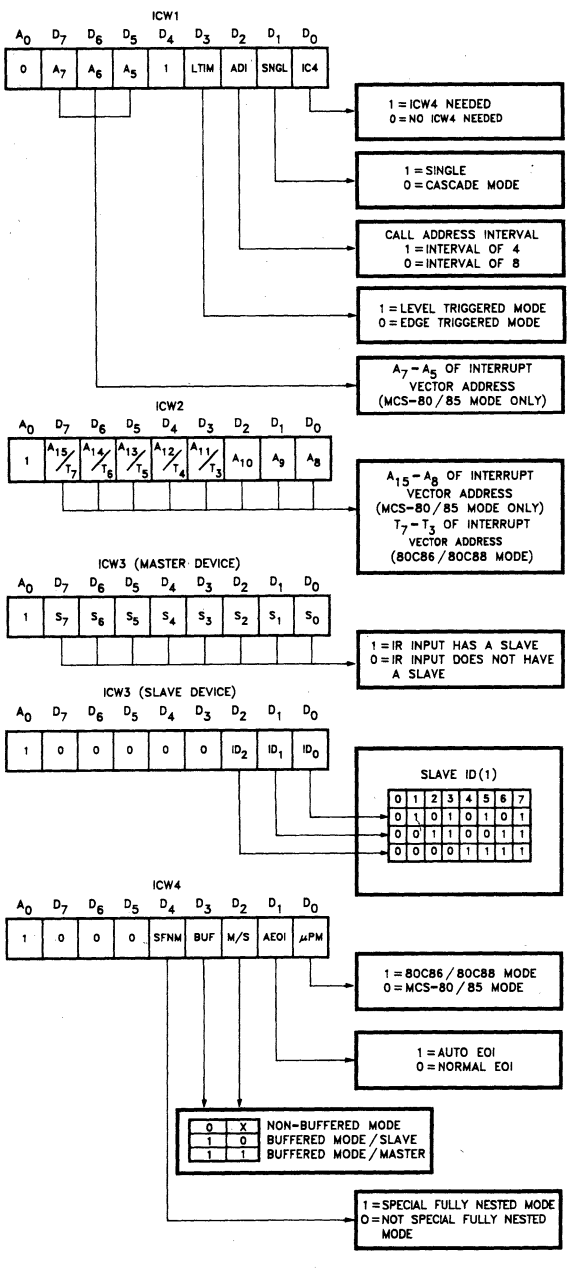


Figure 6. Initialization Sequence



NOTE:
Slave ID is equal to the corresponding master IR input.

Figure 7. Initialization Command Word Format

OPERATION COMMAND WORDS (OCWs)

After the initialization Command Words (ICWs) are programmed into the 82C59A-2, the chip is ready to accept interrupt requests at its input lines. However, during the 82C59A-2 operation, a selection of algorithms can command the 82C59A-2 to operate in various modes through the Operation Command Words (OCWs).

OPERATION CONTROL WORDS (OCWs)

OCW1

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

OCW2

0	R	SL	EOI	0	0	L2	L1	L0

OCW3

0	0	ESMM	SMM	0	1	P	RR	RIS

OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). $M_7 - M_0$ represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

R, SL, EOI — These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0—These bits determine the interrupt level acted upon when the SL bit is active.

OPERATION CONTROL WORD 3 (OCW3)

ESMM — Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0 the SMM bit becomes a "don't care".

SMM — Special Mask Mode. If ESMM = 1 and SMM = 1 the 82C59A-2 will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the 82C59A-2 will revert to normal mask mode. When ESMM = 0, SMM has no effect.

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority form 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic. End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{\text{INTA}}$ pulse (when AEOI bit in ICW4 is set) or by a command word that must be issued to the 82C59A-2 before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 82C59A-2 is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 82C59A-2 will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the 82C59A-2 may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and L0-L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 82C59A-2 is in the Special Mask Mode.

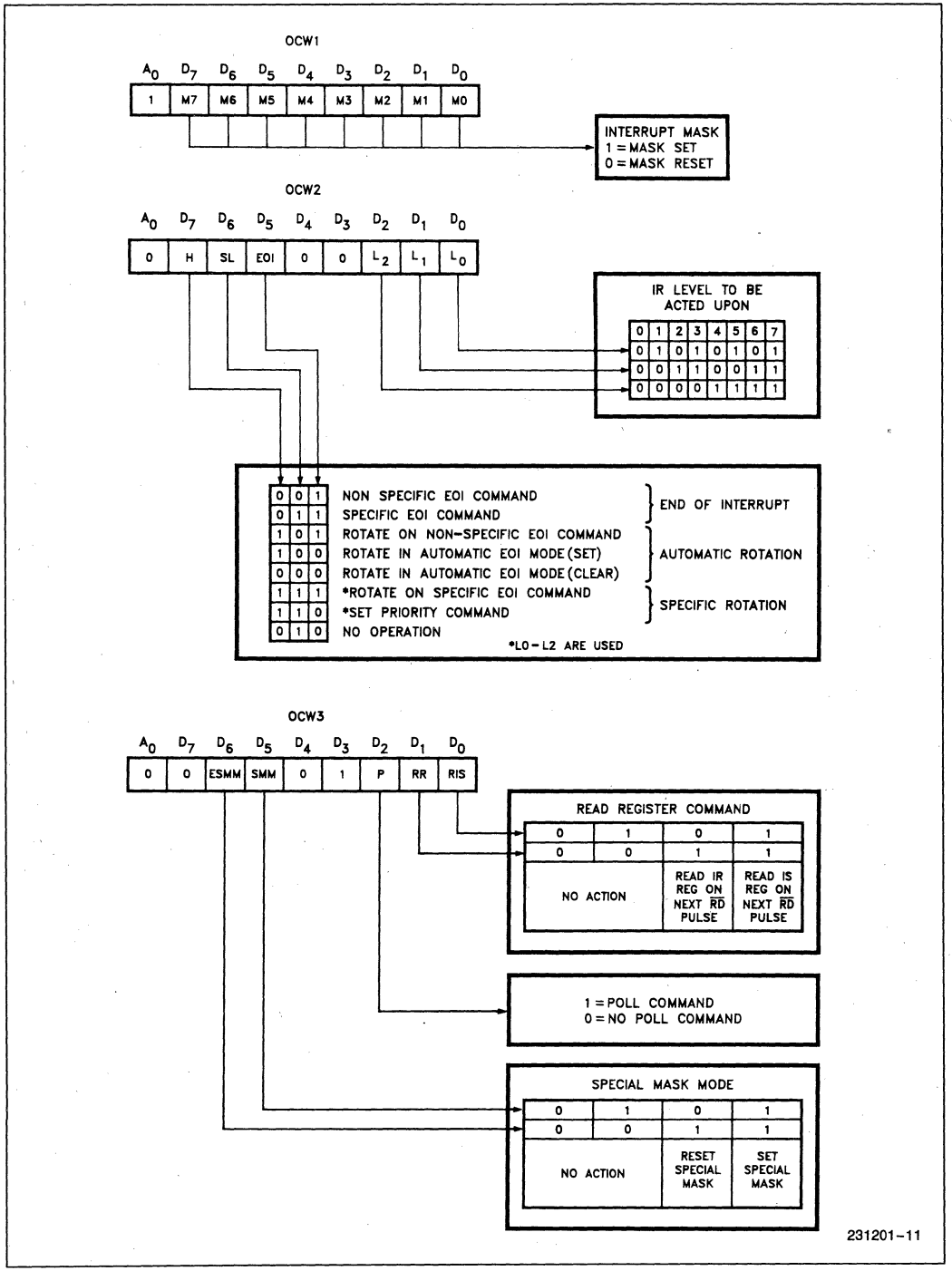


Figure 8. Operation Command Word Format

AUTOMATIC END OF INTERRUPT (AEOI) MODE

If AEOI = 1 in ICW4, then the 82C59A-2 will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 82C59A-2 will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in 80C86/88). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 82C59A.

The AEOI mode can only be used in a master 82C59A and not a slave.

AUTOMATIC ROTATION

(Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most *once*. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	1	0	0	0	0

	Lowest Priority							Highest Priority
Priority Status	7	6	5	4	3	2	1	0

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	0	0	0	0	0

	Highest Priority			Lowest Priority				
Priority Status	2	1	0	7	6	5	4	3

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

SPECIFIC ROTATION

(Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1; LO-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and LO-L2 = IR level to receive bottom priority).

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 82C59A-2 would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level *and enables* interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectivity enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

POLL COMMAND

In Poll mode the INT output functions as it normally does. The microprocessor should ignore this output. This can be accomplished either by not connecting the INT output or by masking interrupts within the microprocessor, thereby disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P = "1" in OCW3. The 82C59A-2 treats the next $\overline{RD}$ pulse to the 82C59A-2 (i.e., $\overline{RD}$ = 0, $\overline{CS}$ = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

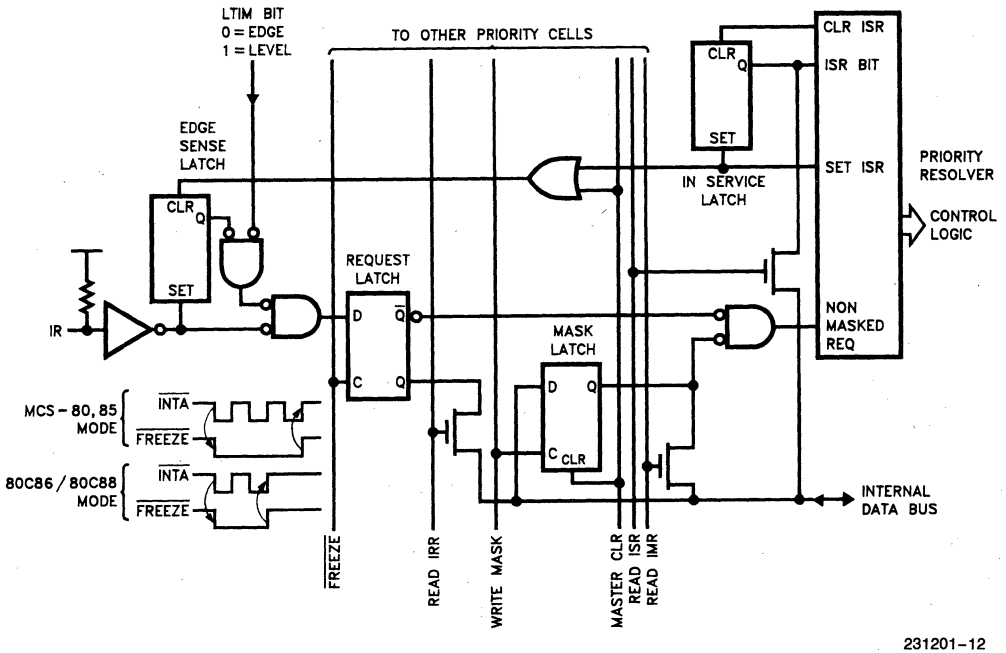
D7	D6	D5	D4	D3	D2	D1	D0
I	—	—	—	—	W2	W1	W0

WO–W2:

Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.



NOTES:
1. Master Clear active only during ICW1
2. Freeze/ is active during $\overline{INTA}$/and poll sequences only
3. Truth Table for D-Latch

C	D	Q	OPERATION
1	Di	Di	FOLLOW
0	X	Qn-1	HOLD

Figure 9. Priority Cell—Simplified Logic Diagram

READING THE 82C59A-2 STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR).

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0.)

The ISR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1):

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 82C59A-2 "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 82C59A-2 is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and AO = 1 (OCW1).

Polling overrides status read when P = 1, RR = 1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR Input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 82C59A-2. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

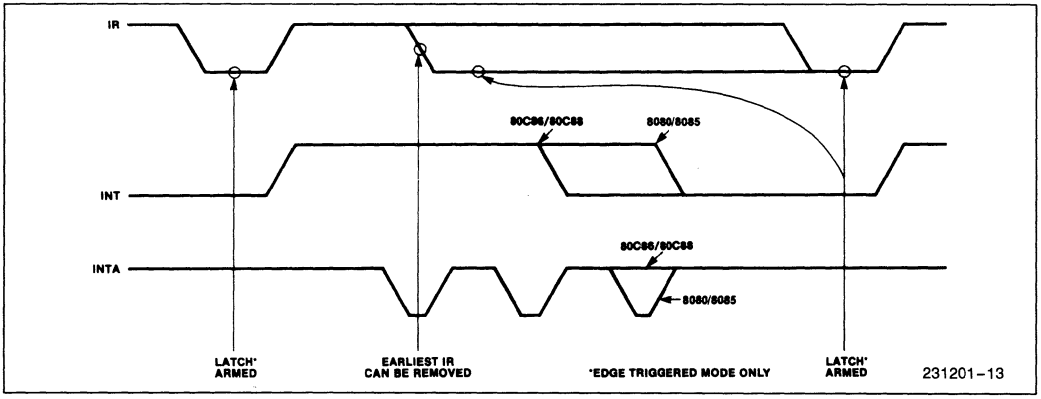


Figure 10. IR Triggering Timing Requirements

THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nestled mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

BUFFERED MODE

When the 82C59A-2 is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 82C59A-2 to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the 82C59A-2's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the 82C59A-2 is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW3 determines whether it is a master or a slave.

CASCADE MODE

The 82C59A-2 can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 80C86/80C88).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 82C59A-2 in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each 82C59A-2.

The cascade lines of the Master 82C59A-2 are activated only for slave inputs, non slave inputs leave the cascade line inactive (low).

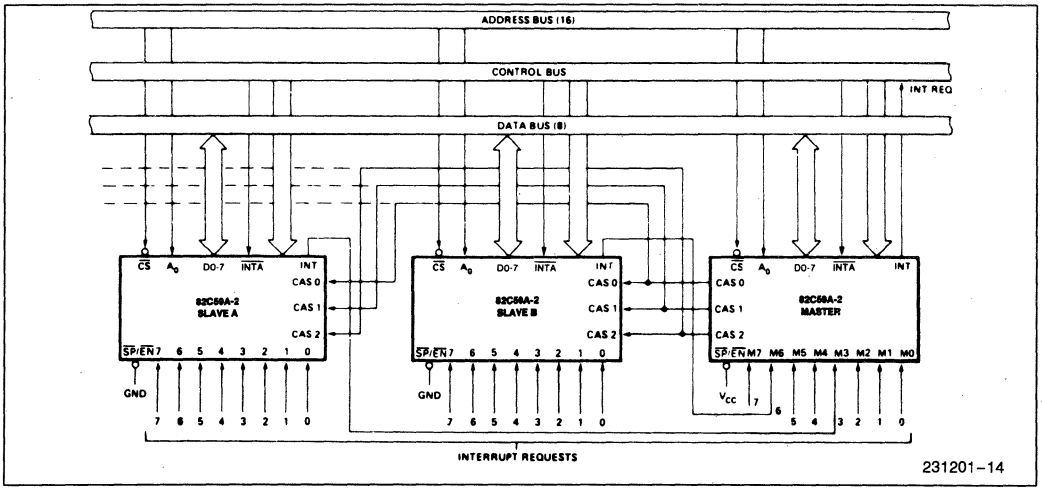


Figure 11. Cascading the 82C59A-2

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to + 150°C
Supply Voltage (w.r.t. ground) .....−0.5 to 7.0V
Input Voltage (w.r.t. ground) ...−0.5 to V_{CC} + 0.5V
Output Voltage (w.r.t. ground)..−0.5 to V_{CC} + 0.5V
Power Dissipation.....0.9 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CCS}	Standby Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND All IR = GND Outputs Unloaded V_{CC} = 5.5V
I_{CC}	Operating Supply Current		5	mA	(Note)
V_{IH}	Input High Voltage	2.2	V_{CC} + 0.5	V	
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	3.0 V_{CC} −0.4		V	I_{OH} = −2.5 mA I_{OH} = −100 μA
I_{LI}	Input Leakage Current		±1.0	μA	$0V \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0V \le V_{OUT} \le V_{CC}$
I_{LIR}	IR Input Leakage Current		−300 +10	μA	V_{IN} = 0 $V_{IN} = V_{CC}$

NOTE:
Repeated data input with 80C86-2 timings.

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions	
C_{IN}	Input Capacitance		7	pF		fc = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins at GND	
C_{OUT}	Output Capacitance		15	pF		

5

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

TIMING REQUIREMENTS

Symbol	Parameter	82C59A-2		Units	Test Conditions
		Min	Max		
TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$ ↓	10		ns	
TRHAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$ ↑	5		ns	
TRLRH	$\overline{RD}$/$\overline{INTA}$ Pulse Width	160		ns	
TAHWL	A0/$\overline{CS}$ Setup to $\overline{WR}$ ↓	0		ns	
TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}$ ↑	0		ns	
TWLWH	$\overline{WR}$ Pulse Width	190		ns	
TDVWH	Data Setup to $\overline{WR}$ ↑	160		ns	
TWHDX	Data Hold after $\overline{WR}$ ↑	0		ns	
TJLJH	Interrupt Request Width (Low)	100		ns	(See Note)
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$ ↓ (Slave Only)	40		ns	
TRHRL	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		ns	
TWHWL	End of $\overline{WR}$ to next $\overline{WR}$	190		ns	
*TCHCL	End of Command to next Command (Not same command type) End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence.	400		ns	

*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 400 ns (i.e. 8085A = 1.6 μs, 8085-A2 = 1 μs, 80C86 = 1 μs, 80C86-2 = 625 ns)

NOTE:
This is the low time required to clear the input latch in the edge triggered mode.

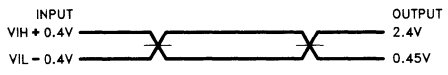
TIMING RESPONSES

Symbol	Parameter	8259A-2		Units	Test Conditions**
		Min	Max		
TRLDV	Data Valid from $\overline{RD}/\overline{INTA}\downarrow$		120	ns	1
TRHDZ	Data Float after $\overline{RD}/\overline{INTA}\uparrow$	10	85	ns	2
TJHIH	Interrupt Output Delay		300	ns	1
TIALCV	Cascade Valid from First $\overline{INTA}\downarrow$ (Master Only)		360	ns	1
TRLEL	Enable Active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$		110	ns	1
TRHEH	Enable Inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$		150	ns	1
TAHDV	Data Valid from Stable Address		200	ns	1
TCVDV	Cascade Valid to Valid Data		200	ns	1

**Test Condition Definition Table

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	100 pf
2	4.5V	1.8 kΩ	1.8 kΩ	30 pf

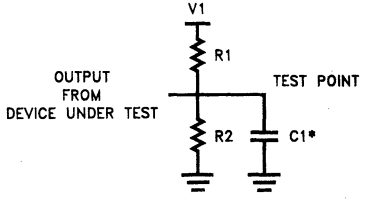
A.C. TESTING INPUT, OUTPUT WAVEFORM



231201-15

A.C. Testing: All input signals must switch between V_{IL} − 0.4V and V_{IH} + 0.4V. Input Rise and Fall Times must be ≤ 15 ns. All timing measurements are made at 2.4V and 0.45V.

A.C. TESTING LOAD CIRCUIT

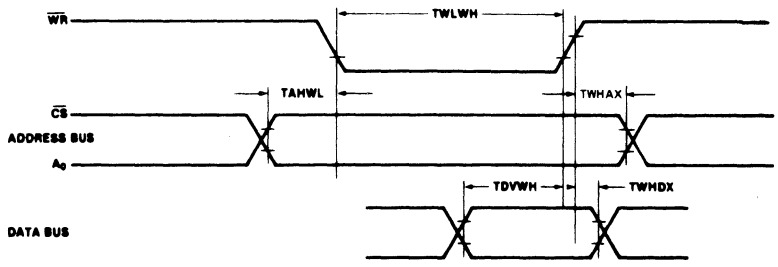


231201-16

*Includes Stray and Jig Capacitance

WAVEFORMS

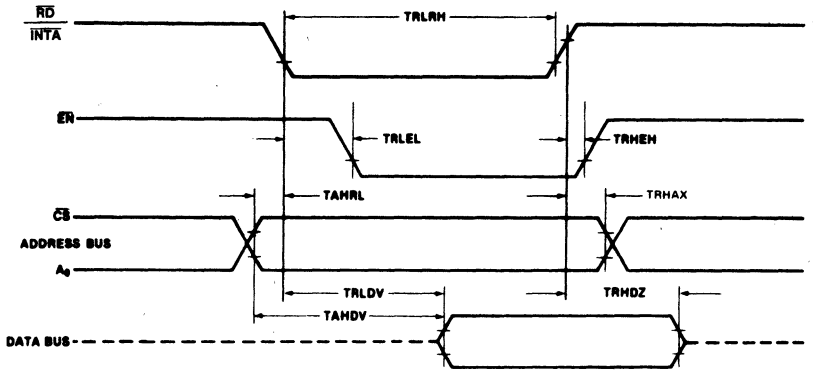
WRITE



231201-17

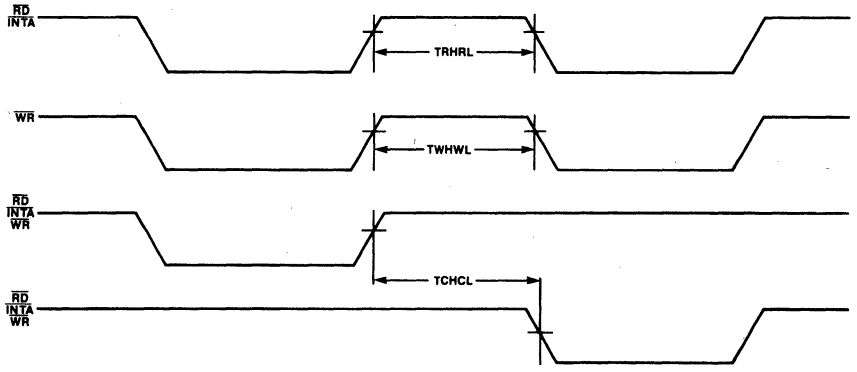
WAVEFORMS (Continued)

READ/INTA



231201-18

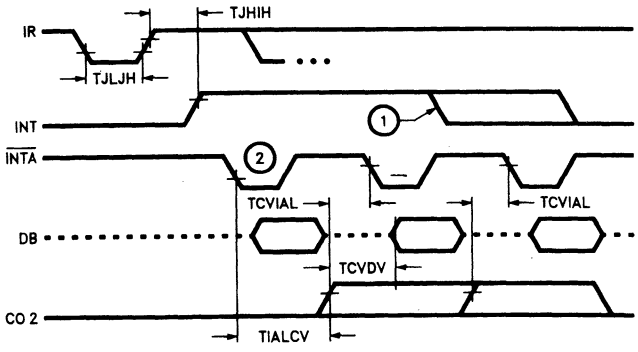
OTHER TIMING



231201-19

WAVEFORMS (Continued)

$\overline{\text{INTA}}$ SEQUENCE



231201-20

NOTES:
1. Interrupt output must remain HIGH at least until leading edge of first INTA.
2. Cycle 1 in 80C86 and 80C88 systems, the Data Bus is not active.

DATA SHEET REVISION REVIEW

The following changes have been made since revision 003 of the 82C59A-2 data sheet.

1. Preliminary was removed.
2. A reference to PLCC packaging was removed.
3. The first paragraph of the Poll Command section was rewritten to clarify the status of the INT pin.
4. A paragraph was added to the Interrupt Sequence section to indicate the status of the INT pin during multiple interrupts.

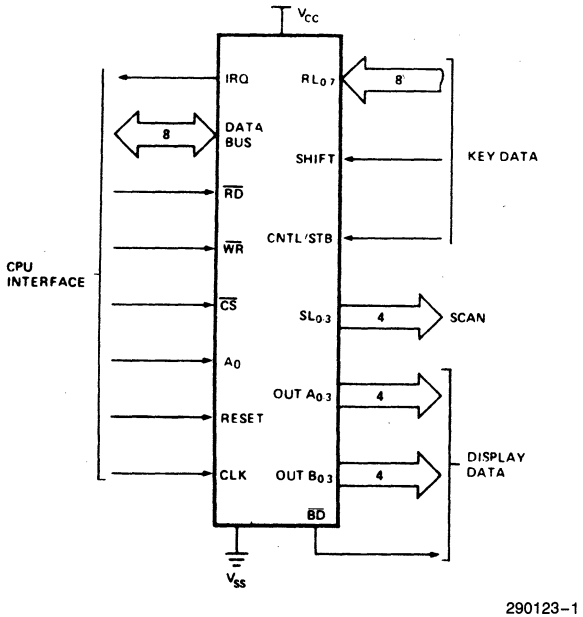
5

8279/8279-5
PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- **Simultaneous Keyboard Display Operations**
- **Scanned Keyboard Mode**
- **Scanned Sensor Mode**
- **Strobed Input Entry Mode**
- **8-Character Keyboard FIFO**
- **2-Key Lockout or N-Key Rollover with Contact Debounce**
- **Dual 8- or 16-Numerical Display**
- **Single 16-Character Display**
- **Right or Left Entry 16-Byte Display RAM**
- **Mode Programmable from CPU**
- **Programmable Scan Timing**
- **Interrupt Output on Key Entry**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

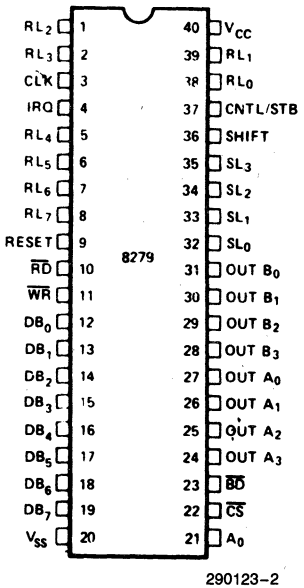
The Intel 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16x8 display RAM which can be organized into dual 16x4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.



290123-1

Figure 1. Logic Symbol



290123-2

Figure 2. Pin Configuration

The complete document for this product is available on Intel's "Data-on-Demand" CD-ROM product. Contact your local Intel field sales office, Intel technical distributor, or call 1-800-548-4725.

September 1987
Order Number: 290123-002

82389
MESSAGE PASSING COPROCESSOR
A MULTIBUS II BUS INTERFACE CONTROLLER

- **Highly Integrated VLSI Device**
  - **— Single-Chip Interface for the Parallel System Bus (IEEE 1296)**
  - **— Interrupt Handling/Bus Arbitration Functions**
  - **— Dual-Buffer Input and Output DMA Capabilities**
  - **— Nine 32-Byte High Speed FIFOs**
- **Multiple Interface Support**
  - **— Complete Protocol Support of the PSB Bus (Message Passing)**
  - **— Processor Independent Interface (8-, 16-, or 32-Bit CPU)**
  - **— Low-Cost 8-Bit Microcontroller Interface**
  - **— Dual-Port Memory Interface**
- **High Performance Coprocessing Functions**
  - **— Offloads CPU for Communication and Bus Interfacing**
  - **— 40 Megabytes/sec Burst Transfer Speed**
  - **— Optimized for Real-Time Response (Max. 900 ns for 32-Byte Interrupt Packet)**
- **CMOS Technology**
- **149-Pin PGA Package (15 x 15 Grid)**

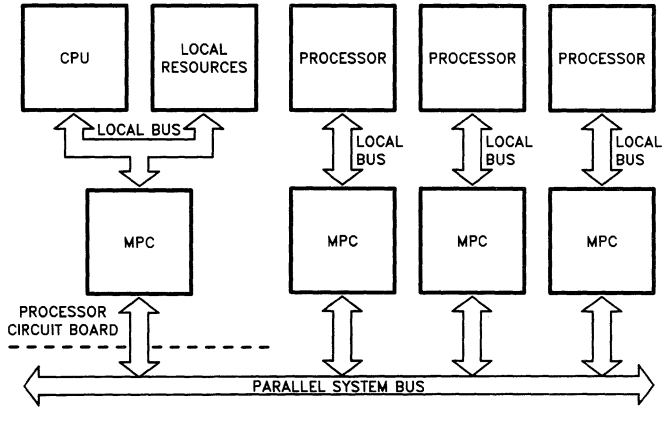
The MPC 82389 is a highly integrated VLSI device that maximizes the performance of a Multibus II based multiprocessor system. It integrates the functions of bus arbitration, data transmit packetizing, error handling and interrupt control. Because of these integrated functions, the host CPU can be offloaded to utilize the maximum bus performance and subsequently increase the system throughput. The MPC 82389 also supports geographic addressing by providing access to the local interconnect registers for reference and control.

The MPC 82389 is designed to interface with an 8-, 16-, or 32-bit processor. The Parallel System Bus (PSB) performance is not affected by the CPU buswidth or bandwidth. The data on the PSB is burst transferred at the maximum bus speed of 40 Megabytes/second regardless of CPU bus performance. Such performance is possible due to decoupling of the CPU from the PSB.

5

This data sheet is supplemented by a *MPC User's Manual*, Intel literature number 176526-002. The *MPC User's Manual* provides detailed information regarding hardware and software board design information. In addition, the IEEE 1296 specification can provide more information regarding the MULTIBUS II bus architecture.

MULTIPROCESSOR ARCHITECTURE



290145-1

1.0 MPC 82389 INTRODUCTION

The 82389 Message Passing Coprocessor (MPC) is a highly integrated CMOS VLSI device which interfaces any microprocessor to the MULTIBUS II Parallel System Bus (PSB). The PSB is defined for easy access and sharing of resources in a processing environment which allows the existence of both intelligent and non-intelligent add-in boards. The MPC complements the MULTIBUS II environment by providing an optimized interface for the PSB at its maximum bandwidth. The MPC also offloads the host CPU, thus increasing system throughput, by providing the necessary bus arbitration, message passing protocol, error handling and interrupt control for a MULTIBUS II system. Figure 1-1 shows an example of the MPC's message passing performance.

1.1 Functional Overview

The MPC 82389 is a bus interface controller which offloads the host CPU for interprocessor communication on the PSB. The MPC 82389 features four interfaces which support a variety of data transfer operations.

1.1.1 MPC 82389 INTERFACES

The three primary interfaces to the MPC (PSB Interface, Host CPU Interface and Interconnect Interface) all function asynchronously to one another. This is accomplished through the use of internal latches and FIFOs that allow references to occur simultaneously on all interfaces. In addition to the three primary interfaces, the MPC contains a Dual-Port Interface which provides compatibility with past system implementations and software.

—PSB Interface
The PSB Interface is the synchronized, shared data pathway in the MULTIBUS II system.

—Host CPU Interface
The Host CPU Interface is a set of addressable registers and ports that is the private pathway for the local microprocessor on the MULTIBUS II board.

—Interconnect Interface
The Interconnect Interface provides a path for added board functionality that is independent from the host CPU.

—Dual-Port Interface
The Dual-Port Interface supports shared memory references.

1.1.2 MAJOR OPERATIONS

—Unsolicited and Solicited Message Passing
The unsolicited and solicited message passing protocol is an interprocessor communication protocol which allows an intelligent agent* on the PSB to communicate with another agent without any CPU intervention at full PSB speed.

—PSB Memory and I/O Single Cycle Access
The MPC performs single cycle read/write transfers from the host to memory and I/O locations across the PSB. The MPC handles bus arbitration, parity generation and error detection without CPU intervention.

—Local Interconnect Access
The host CPU and other agents on the PSB can access local interconnect space via the MPC.

*An agent is any device with an interface to the PSB.

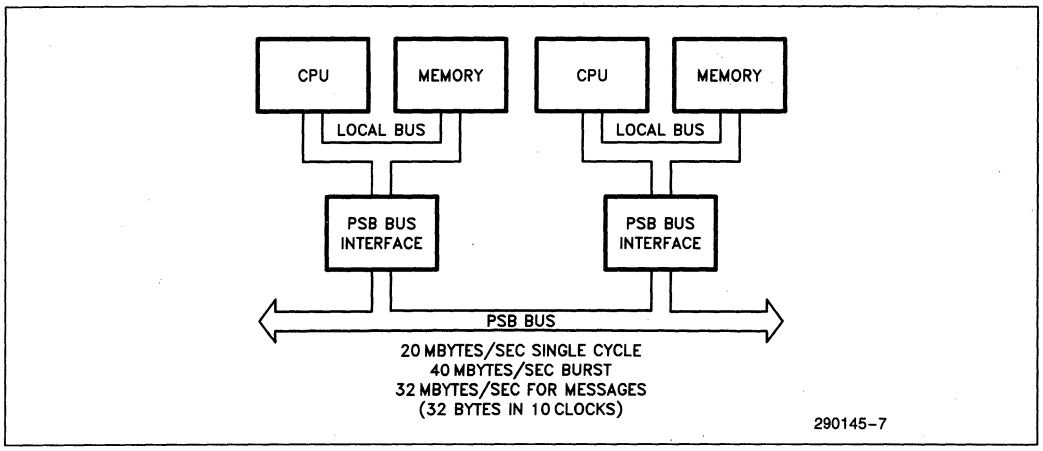


Figure 1-1. Message Passing Performance Example

—Remote Interconnect Access
The MPC enables the host CPU to access remote interconnect locations assigned to other PSB agents.

—Dual-Port Memory Access Support
Other PSB agents can access dual-port memory via the MPC.

—Central Services Module (CSM) support
The MPC has a minimal set of built-in CSM support features which allow the CSM to be incorporated into any MULTIBUS II board design.

2.0 MESSAGE PASSING PROTOCOL

The MULTIBUS II architecture designates the data transfer protocol between agents on the PSB as message passing. Message passing allows agents to transfer variable amounts of data at maximum PSB speed. The MPC fully supports the PSB's standardized message passing protocol. The entire handshaking procedure between agents on the PSB is handled by the MPC without CPU intervention.

There are two types of messages that can be transmitted from one agent to another: Unsolicited Messages and Solicited Messages.

2.1 Unsolicited Messages

Unsolicited messages are short, fixed-length messages that can arrive unexpectedly. Unsolicited messages can be transmitted without explicit buffer allocation and without synchronization between sending and receiving agents on the PSB. Unsolicited messages are often referred to as intelligent or virtual interrupts, since they can be used as a signaling mechanism between boards, replacing traditional system interrupts and freeing the CPU from having to poll for information. In addition, unsolicited messages allow for up to 28 bytes of user data.

2.2 Solicited Messages

Solicited messages are used to transfer large amounts of data. Up to 16 Mbytes (less 1 byte) of data can be transferred in a single solicited message transmission sequence. Solicited message transfers require the receiving agent to explicitly allocate a buffer. Buffer negotiation between sending and receiving agents is handled using unsolicited messages as follows:

- A buffer request message initiates a solicited message transfer. It requests the receiving agent to allocate a buffer large enough to hold the solicited data.
- A buffer grant message must be returned by the receiving agent before the solicited data can be transferred. The buffer grant informs the sending agent's MPC that a buffer has been allocated and indicates that the receiving agent's MPC is ready to begin the data transfer.
- A buffer reject message is returned by the receiving agent if a buffer for the solicited data cannot be provided. In this case, the rejection is final, and no further action is required.

If a DMA controller handles the solicited message transfer, DMA controller setup is also needed. Typically, the sending agent programs its DMA controller immediately before sending a buffer request, and the receiving agent programs its DMA controller immediately before sending a buffer grant.

Once solicited buffer negotiation is complete (the sending agent's MPC has received a buffer grant), the agents transfer the data without further intervention. The data is sent as a series of solicited packets on the sending agent's local bus. The MPCs perform transfer and routing across the PSB automatically. At the end of the solicited data transfer, both the sending and receiving agents get a completion indication from their local MPC.

3.0 MPC 82389 INTERFACES

The MPC 82389 features a total of 4 interfaces. The three primary interfaces are the Host CPU Interface, PSB Interface and the Interconnect Interface. The MPC also has a Dual-Port Memory Interface which provides compatibility with past system implementations and software. Figure 3-1 shows the four MPC bus interfaces.

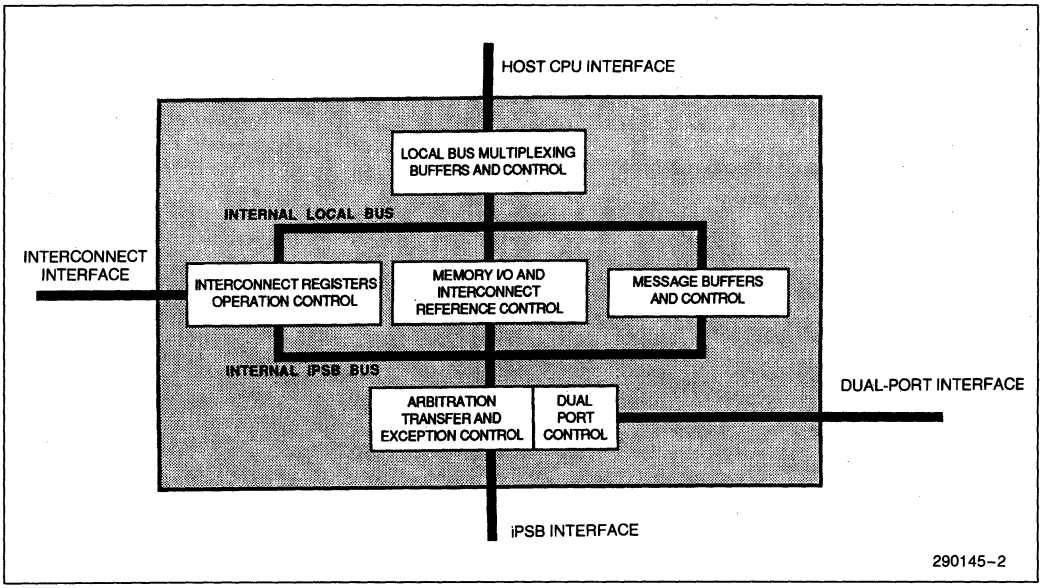


Figure 3-1. MPC Bus Interfaces

3.1 Host CPU Interface

The Host CPU Interface connects an 8-, 16-, or 32-bit processor to the MPC. The Host CPU Interface supports direct references to memory, I/O, and interconnect address space on the PSB. The entire Host CPU Interface is composed of three sub-interfaces: Register Sub-Interface, Reference Sub-Interface and DMA Sub-Interface.

—Register Sub-Interface
The Register Sub-Interface is composed of a bank of 8-bit registers on the Host CPU Interface. These registers provide the configuration, status and command interface for the host CPU. A host register operation is independent from operations which may be in progress at the MPC's other interfaces. However, some host register operations are dependent on the internal state of the MPC. In host register operations, the maximum duration is decided by the strobe width. Thus, the number of wait states required at the local interface is under the control of the host CPU.

—Reference Sub-Interface
The Reference Sub-Interface supports direct references to memory, I/O, and interconnect address space on the PSB. Memory and I/O references are initiated by the CPU to the MPC. The MPC responds to a memory or I/O reference by putting the CPU on hold while arbitrating for the PSB. The CPU is held in wait states until the reference is complete or until a bus exception condition occurs on the PSB. The Reference Sub-Interface supports both read and write operations to the registers. The local interconnect address space is differentiated from the interconnect address on the PSB by the bit pattern stored in the MPC's slot address register.

—DMA Sub-Interface
The DMA Sub-Interface supports data transfers between the local memory and the MPC during solicited message operations. The DMA Interface is designed to support either two-cycle or fly-by (single-cycle) read/write transfers. For two-cycle operations, the DMA controller performs one cycle into memory and another cycle to the MPC; a read command is used to get data from the MPC and a write command is used to put data into the MPC. Fly-by operations allow data to be transferred during a single bus cycle; a fly-by transfer will use a write command to get data from the MPC (corresponding to a memory write) and a read command to put data into the MPC (corresponding to a memory read). The higher performance possible with fly-by transfers mandates the alignment of data on 4-byte boundaries.

3.2 Parallel System Bus Interface

The Parallel System Bus (PSB) Interface is a full 32-bit interface to other boards in the MULTIBUS II chassis. The PSB Interface supports PSB arbitration, data transfer and error handling.

—Parallel System Bus Arbitration
The MPC begins PSB access arbitration upon a request which is generated inside the MPC. This request could be the result of a synchronized PSB memory, I/O or interconnect reference request or a message packet transmit request from the CPU.

—Data Transfer
The PSB Interface contains all the address/data lines and necessary control signals for data transfer. These control signals provide the control mechanism between agents during transfer operations.

—Error Handling
The MPC monitors errors generated during data transfer operations. The MPC recognizes data integrity problems on the PSB and bus timeout conditions.

3.3 Interconnect Interface

The Interconnect Interface is an independent 8-bit communication interface which allows the MPC to be connected to a microcontroller. (It is highly recommended that an 8051 or similar microcontroller be used on the Interconnect Interface.) This microcontroller will perform tasks such as board configuration at startup and local diagnostics.

The interconnect space of an agent is the only required bus space by the IEEE 1296 specification and has a 512-byte register range. Within this space the microcontroller can store the local operating and configuration parameters associated with the agent. For example, local diagnostics can be executed out of the microcontroller and the results posted in the interconnect space.

Local resources on an agent gain access to interconnect space through the MPC's interconnect bus. A microcontroller connects to the interconnect bus for intelligent handling of interconnect operations. All interconnect bus signals are asynchronous to the bus clock and to the local bus signals.

3.4 Basic Implementation with the MPC 82389

Figure 3-2 shows a basic implementation of the MPC 82389. Included in this implementation is the Interconnect Interface, the Host CPU Interface and the PSB Interface.

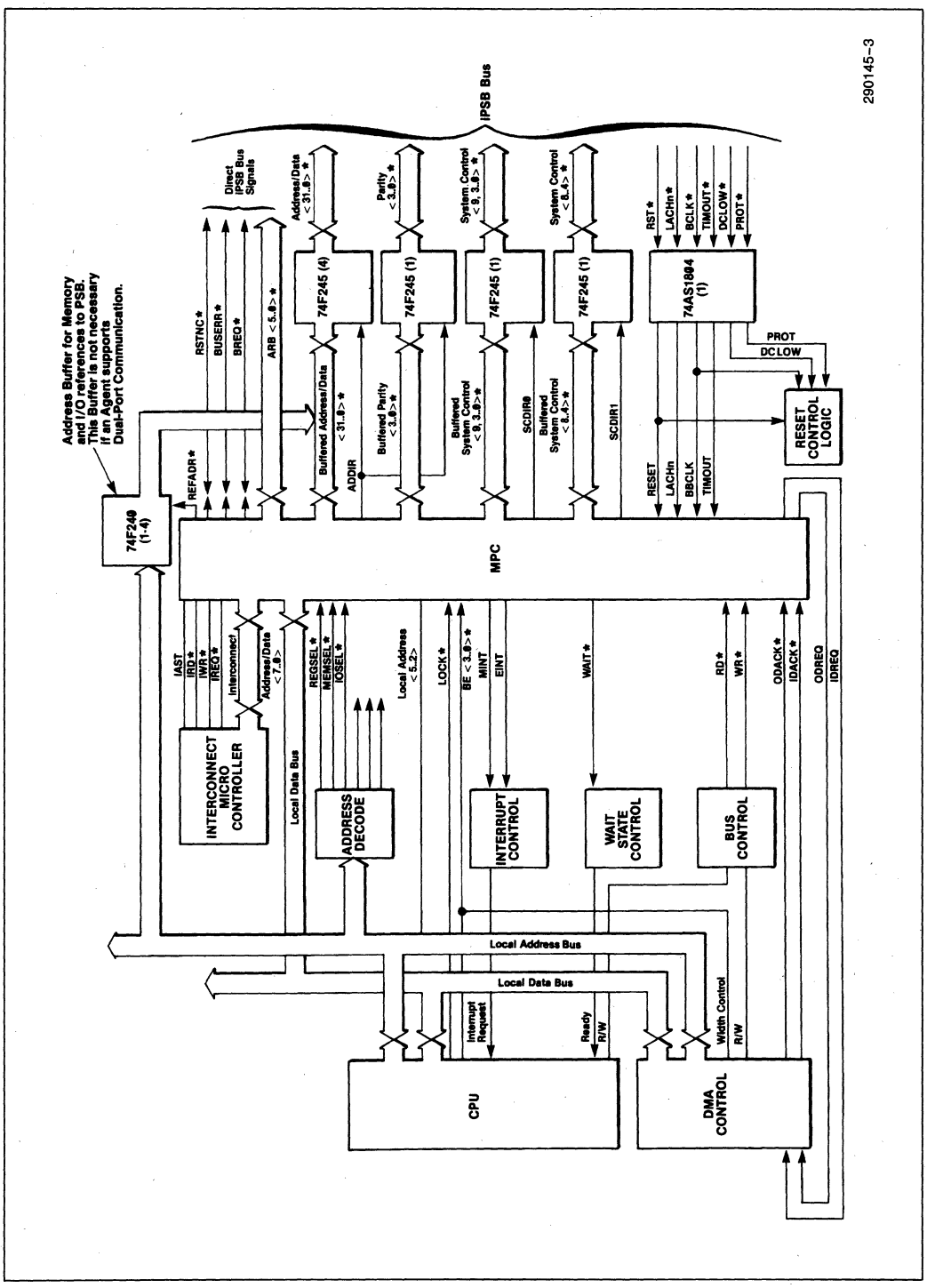
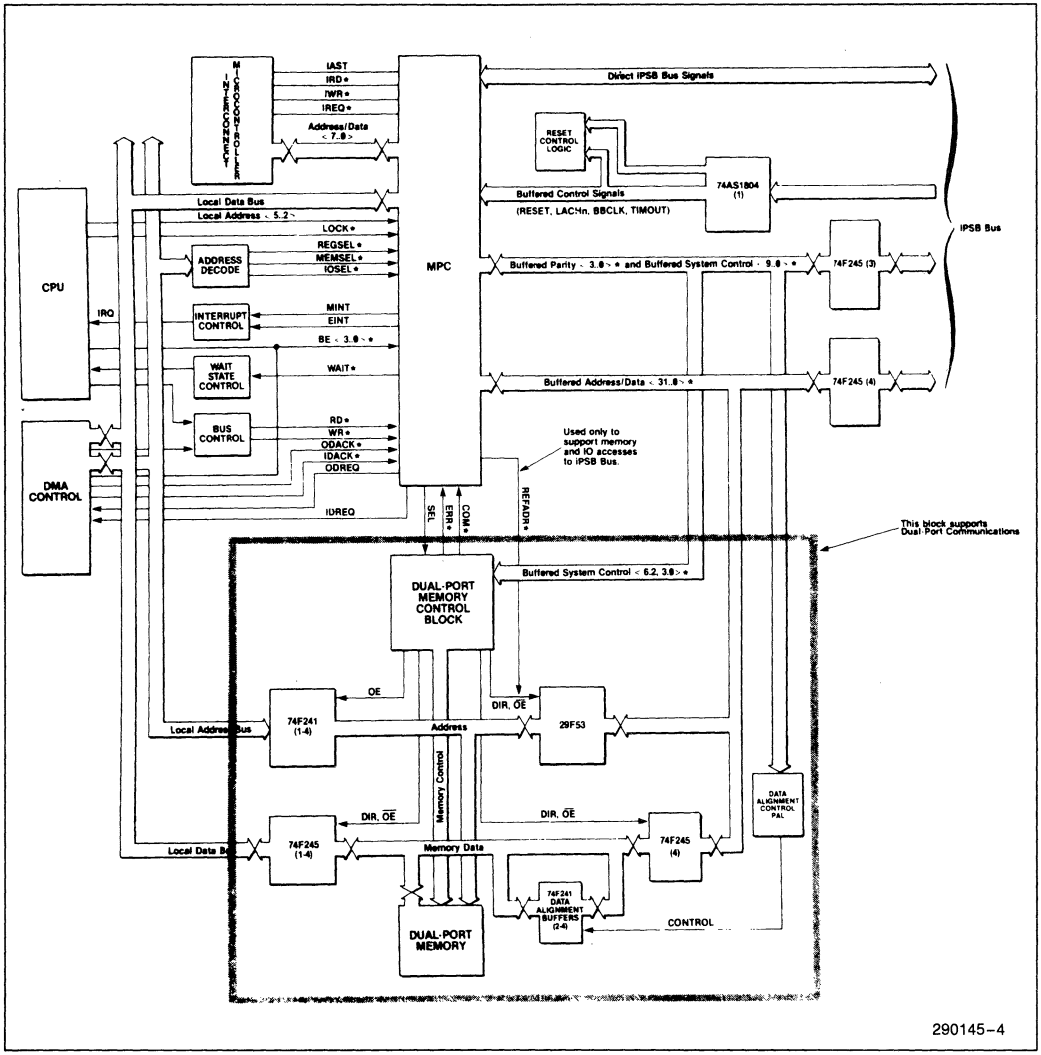


Figure 3-2. MPC Implementation to Support References

3.5 Dual-Port Interface

The Dual-Port Interface supports shared memory accesses between agents on the PSB. In order to fully implement dual-port memory, some additional dual-port memory controller logic is required. Figure 3-3 shows an example of the MPC implemented with dual-port memory.



290145-4

Figure 3-3. The MPC Implemented with Dual-Port Memory

4.0 MPC 82389 OPERATIONS

The primary function of the MPC 82389 is MULTIBUS II message passing. In addition to message passing, the MPC performs the following functions:

— Memory and I/O Reference
— Local Interconnect Reference
— Remote Interconnect Reference
— Interconnect Replier Operations
— Dual-Port Replier Operations
— Central Services Module Support

4.1 MULTIBUS II Message Passing

The MPC manages the routing of message packets as they flow between the interfaces of each MULTIBUS II agent in the system. For message traffic on the PSB, message decode logic on the PSB input bus determines message routing through the MPC. For the Host CPU Interface and Interconnect Interface, the MPC defines a signal protocol for message passing.

MULTIBUS II messages, both unsolicited and solicited, are transferred through nine dedicated internal FIFO buffers between the Host CPU Interface and PSB Interface. Unsolicited messages are intelligent (also called virtual) interrupts which notify the receiving agent to prepare for the receipt of solicited messages. Unsolicited messages use the Transmit/Error FIFO and the Receive FIFO. The Transmit FIFO holds a 32-byte packet for transmittal across the PSB. If there is an error in transmission, the Transmit FIFO becomes the Error FIFO, where the errant message can be read back along with error status. The Receive FIFO is a circular queue of four 32-byte buffers from which unsolicited messages are received from the PSB by the host CPU.

Solicited messages consist of information data packets which are transmitted between agents. Solicited messages use the Solicited Input FIFO and Solicited Output FIFO. These FIFOs are dual 32-byte buffers which are used for the temporary storage of solicited data packets as they travel between the Host CPU Interface and the PSB Interface. The solicited output header logic attaches header information to the solicited data packet before sending it onto the PSB. All FIFOs are able to operate independently and concurrently, thus creating a true multitasking message passing environment. Figure 4-1 shows the nine dedicated internal FIFO buffers.

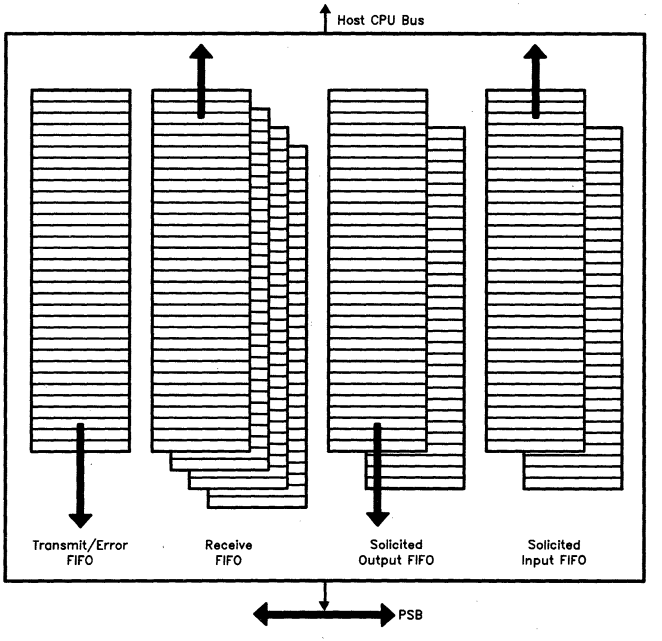


Figure 4-1. The MPC Uses Nine Dedicated Internal 32-Byte FIFO Buffers

4.1.1 UNSOLICITED TRANSMIT/RECEIVE

Unsolicited message passing sequences occur between the Host CPU Interface and the PSB Interface using FIFOs internal to the MPC. FIFO status is available on the Host CPU Interface and in state machines internal to the MPC. On the Host CPU Interface, host register operations write bytes to the Transmit FIFO and read bytes from the Receive FIFO. On the PSB, the MPC manages the emptying and filling of the Transmit and Receive FIFOs using MULTIBUS II message passing protocol and the Transmit and Receive FIFOs on another agent's MPC. For detailed information about message passing protocol across the PSB, see the *IEEE 1296 High Performance Synchronous 32-bit Bus Standard.*

4.1.2 SOLICITED INPUT/OUTPUT

Solicited transfers are pre-negotiated using unsolicited message sequences. Dedicated FIFOs (Solicited Input FIFO and Solicited Output FIFO) are then used for the transfer of solicited data packets. This allows large amounts of data to be moved between agents independently of unsolicited messages. In most cases, the solicited transfer occurs under DMA control, freeing the host CPU to handle other activities. The DMA controller uses the input channel DMA request/acknowledge and output channel DMA request/acknowledge signals along with the read/write signal to stream the data from/to the solicited FIFOs. On the PSB, the data is transferred in bursts using MULTIBUS II message passing protocol and similar solicited FIFOs on another agent's MPC. The MPCs add header information to the packets on the PSB, indicating source, destination and length. Data transfers through the solicited FIFOs can be set up for 8, 16 or 32 bits of data width on the Host CPU Interface, but occur at full 32-bit width on the PSB.

4.2 Memory and I/O References

Remote memory or I/O reference operations are Host CPU Interface operations that involve an access through the MPC to a resource across the PSB. This resource can be a dumb memory or I/O board. The remote reference can only be done through the MPC as a single cycle operation (no block transfers) to the remote resource and can involve an unknown number of wait states. Many MULTIBUS II CPU boards use an alternate path (such as the iLBX bus found on Intel iSBC boards) that is an independent extension of the local bus for full-speed and block transfer operations.

The host CPU initiates a memory or I/O reference by activating memory select ($\overline{\text{MEMSEL}}$†) or I/O select ($\overline{\text{IOSEL}}$), A<5–2>, $\overline{\text{BE}}$<3–0>, with a $\overline{\text{RD}}$ or $\overline{\text{WR}}$ strobe. If necessary, $\overline{\text{LOCK}}$ is activated to allow back-to-back accesses across the PSB, holding all other agents off the memory or I/O resource. The MPC activates its $\overline{\text{WAIT}}$ output to indicate that the operation is in progress.

The data for reference operation proceeds through the MPC and PSB to a memory or I/O address on another agent. A data path from D<31–0> through the buffered address/data bus ($\overline{\text{BAD}}$<31–0>) is used for the data transfer. Data is latched internally in a reference data latch. Parity is generated to the PSB on BPAR <3–0> for the data on each write operation and checked on data read. Completion of the operation is indicated when the MPC deactivates the $\overline{\text{WAIT}}$ output.

The memory or I/O address for the reference operation is routed around the MPC through an external reference address latch. This latch is controlled by the REFADR signal from the MPC.

4.3 Local Interconnect Reference

A local interconnect reference operation is an access by the host CPU to the interconnect records maintained by the local interconnect microcontroller. The geographic interconnect address is preloaded into a pair of registers internal to the MPC. The upper 5 bits of the interconnect address determine whether the operation is local or remote. A data path from D<7–0> to the interconnect address/data bus (IAD<7–0>) is used. The microcontroller uses the interconnect request ($\overline{\text{IREQ}}$) output to sense the request. The request is serviced by the interconnect microcontroller through a sequence of accesses to registers within the MPC using the interconnect address strobe (IAST), interconnect read ($\overline{\text{IRD}}$), and interconnect write ($\overline{\text{IWR}}$) strobes, and the IAD multiplexed bus. The $\overline{\text{WAIT}}$ signal is used as for memory and I/O references to indicate completion of the local interconnect reference operation.

4.4 Remote Interconnect Reference

A remote interconnect reference is an access by the host CPU to interconnect space on another agent. The host CPU requests a remote interconnect reference by writing the interconnect address to the same register used in the local interconnect request, except that the upper 5 bits of the interconnect address indicate the slot address of another agent on the PSB. The data flows through the MPC as in a remote memory or I/O reference, except that the data transfer occurs only on D<7–0>. The remote microcontroller services the request through an interconnect replier operation.

†* indicates that the signal is active low.

4.5 Interconnect Replier Operations

When another agent performs a remote interconnect reference request, it gains access to local interconnect space through the MPC. The MPC decodes an interconnect request on the PSB for a slot ID match and signals the interconnect microcontroller independently of the local bus interface. The microcontroller then handles the request in the same way as a local interconnect request.

4.6 Dual-Port Replier Operations

Other agents can access dual-port memory via the MPC. A memory access request on the PSB is decoded by the MPC for an address range match and serviced by the dual-port controller (external circuitry must be provided). The MPC provides only the handshaking path. Data transfer occurs directly on the $\overline{BAD}$ bus. If a bus exception occurs while a dual-port memory reference is in progress, the MPC will signal the dual-port controller to terminate the operation.

4.7 Central Services Modular Support

The IEEE 1296 specification defines the Central Services Module (CSM) that resides in Slot 0 of a MULTIBUS II system. The CSM is responsible for these functions:

— reset sequencing (generates reset signal on the PSB)

— assignment of card slot and arbitration IDs during reset initialization

— generation of system wide clocks for all agents (bus clocks and time of day)

— generation of bus timeout

— battery back-up of system constants (host ID, time of day, etc.)

The MPC has a minimal set of built-in CSM support features that allow the incorporation of CSM into any MULTIBUS II board design. The MPC, interconnect microcontroller, and a small amount of external circuitry can fully implement the CSM automatically when the board is inserted into Card Slot 0.

4.7.1 ADDITIONAL CSM REQUIREMENTS

In addition to the interconnect microcontroller and the MPC, the following functions must be provided through external logic:

— clock generation

— PSB reset generation

— cold/warm start detection

— PSB timeout generation

The clock generator provides the bus clock ($\overline{BCLK}$) and central clock ($\overline{CCLK}$) signals to the PSB. The reset generator provides the hardware reset line ($\overline{RESET}$) to all agents on the PSB. Cold/warm start detection circuitry distinguishes between a power-up reset and a warm-start reset; on power-up the CSM assigns arbitration and slot IDs. The PSB timeout function determines when the PSB is hung.

See the *MPC User's Manual* (Intel literature number 176526-002) and the *CSM\002 Hardware Reference Manual* (Intel literature number 459706-001) for more information about the CSM.

5.0 MPC 82389 PIN DESCRIPTIONS

This section describes each signal pin (or group of pins) on the MPC. Emphasis is placed on giving as much information as possible to ease the task of designing hardware associated with the MPC signal pins. The pins are described in terms of these functional groups:

- PSB interface
- local bus (host CPU) interface
- dual-port memory control
- interconnect bus interface

5.1 PSB Signals

The PSB signals provide the interface to other boards in the MULTIBUS II chassis. Very little support circuitry is required for this part of the board. Only high-current drivers and reset control logic is needed. Some MPC signal pins have built-in open collector high-current drivers that allow connection directly to the PSB. For complete information on the PSB, see the *IEEE 1296 High Performance Synchronous 32-bit Bus Standard* document.

PSB signals fall into five groups, depending on function:

- arbitration operation signal group
- address/data bus signal group
- system control signal group
- central control signal group
- exception operation signal group

Unless otherwise stated, all PSB signals are synchronous to the bus clock.

NOTE:
High current drivers used to drive the buffered address/data ($\overline{BAD}$) bus should be controlled with minimal logic. This is to limit propagation delays and avoid possible bus contention problems. Ensure that the placement of these drivers and the MPC is done as close to the PSB (the P1 connector on a MULTIBUS II board) as possible to minimize signal stub lengths and capacitive loading.

5.1.1 ARBITRATION OPERATION SIGNAL GROUP

These MPC pins are used by an agent to obtain exclusive access to the PSB. They are all high-current drive, open-collector signals. Below is a description of each signal.

$\overline{BREQ}$ (Bus Request). $\overline{BREQ}$ is a bidirectional open-collector signal that connects directly to the PSB. As an input to the MPC, it indicates that agents are awaiting access to the bus. As an output, the MPC asserts $\overline{BREQ}$ to request PSB access.

$\overline{ARB}$<5-0> (Arbitration). $\overline{ARB}$<5-0> are bidirectional, open-collector signals that connect directly to the PSB. $\overline{ARB}$<5-0> are used (during normal operation) to identify the mode and arbitration priority of an agent during an arbitration cycle. During system initialization (while reset is active), the central services module (CSM) drives these signals to initialize slot and arbitration IDs.

5.1.2 ADDRESS/DATA BUS SIGNAL GROUP

This signal group includes a 32-bit multiplexed address/data path ($\overline{BAD}$<31-0>) and the byte parity signals ($\overline{BPAR}$<3-0>). These signals require buffering through bus transceivers before connection to the PSB. This signal group also includes the bus transceiver control signals (ADDIR and $\overline{REFADR}$).

$\overline{BAD}$<31-0> (Buffered Address/Data). $\overline{BAD}$<31-0> are the 32 bidirectional, multiplexed address/data signals that provide the interface to the PSB address/data bus ($\overline{AD}$) when buffered through 74F245 or equivalent bus transceivers.

NOTE:
Do not use pull-up resistors to drive the BAD bus high. If pull-up resistors are present, the MPC cannot guarantee valid logic states with proper timing.

$\overline{BPAR}$<3-0> (Buffered Parity). $\overline{BPAR}$ are four signals that provide parity for the 32-bit $\overline{BAD}$ bus. These bidirectional lines connect to the PSB $\overline{PAR}$<3-0> signals through a 74F245 or equivalent transceiver. These signals are used to receive byte parity for incoming data and to drive byte parity for outgoing data.

ADDIR (Address/Data Direction). ADDIR is an output that provides direction control over the bus transceivers buffering the $\overline{BAD}$<31-0> and $\overline{BPAR}$<3-0> signals. In the high state, this signal causes the transceivers to drive address/data information along with parity onto the PSB. In the low state, this signal causes address/data information and parity to be received from the PSB.

$\overline{REFADR}$ (Reference Address Enable). $\overline{REFADR}$ is an output used to enable external reference address buffers during reference operations. Asserting this signal places the reference address onto the $\overline{BAD}$ bus. The address path enabled by this signal is only used for memory and I/O reference operations to the PSB. It is not used during message passing or for PSB references to interconnect space.

5.1.3 SYSTEM CONTROL SIGNAL GROUP

The system control signal group on the PSB provides a control mechanism between agents during transfer operations.

$\overline{BSC}$<9-0> (Buffered System Control). $\overline{BSC}$<9-0> is a group of ten bidirectional signals that connect to the PSB through 74F245 or equivalent transceivers. Agents on the PSB use these signals for commands or status, depending on the phase of the operation. The function of each of these lines during request and reply phases of transfer operations is summarized in Table 5-1.

Table 5-1. Summary of $\overline{BSC}$ Signal Functions

Signal	Request Phase	Reply Phase
$\overline{BSC0}$	Bus Owner in Request Phase	Bus Owner in Reply Phase
$\overline{BSC1}$	LOCK	LOCK
$\overline{BSC2}$	Data Width	End-of-Transfer
$\overline{BSC3}$	Data Width	Bus Owner Ready
$\overline{BSC4}$	Address Space	Replying Agent Ready
$\overline{BSC5}$	Address Space	Agent Status
$\overline{BSC6}$	Read/Write Data Transfer	Agent Status
$\overline{BSC7}$	Reserved	Agent Status
$\overline{BSC8}$	Even Parity on BSC<7-4>	Even Parity on BSC<7-4>
$\overline{BSC9}$	Even Parity on BSC<3-0>	Even Parity on BSC<3-0>

NOTE:
The end-of-transfer (EOT) handshake in single-cycle operations is indicated by BSC<4,3,2> as follows: the requesting MPC drives $\overline{BSC}$<3,2> and waits for the replier to drive $\overline{BSC4}$; when the replier responds, the EOT handshake is complete.

SCDIR<1,0> (System Control Direction). SCDIR<1,0> are output signals that provide direction control of the 74F245 transceivers driving and receiving $\overline{BSC}$<9-0>. SCDIR0 provides control for $\overline{BSC}$<9,3-0>, while SCDIR 1 provides control for $\overline{BSC}$<8-4>. When either signal is high, the bus transceiver drives $\overline{BSC}$ signals onto the PSB. When either signal is low, signals on the PSB are driven onto the $\overline{BSC}$ lines.

5.1.4 CENTRAL CONTROL SIGNAL GROUP

The central control signal group provides bus status and control information for devices operating on the PSB. The CSM, residing in slot 0 of the MULTIBUS II backplane, generates $\overline{BCLK}$, LACHn, and RESET.

BBCLK (Buffered Bus Clock). BBCLK is received by the MPC to synchronize all operations on the PSB. This input should be connected to $\overline{BCLK}$ (on the PSB) using a 74AS1804 or equivalent inverting buffer. The falling edge of $\overline{BCLK}$ provides all system timing references. BBCLK normally has a fixed operating frequency of 10 MHz.

NOTE:
$\overline{BCLK}$ can be varied from DC to 10 MHz. You may use this feature for single-stepping on the PSB during debugging.

LACHn (ID Latch). LACHn is an input signal used during initialization of slot and arbitration IDs (where "n" is the slot number). When the RESET signal is active, LACHn indicates when a slot or arbitration ID is available and should be latched. LACHn is an active high input and should be connected to the $\overline{LACHn}$ signal on the PSB with a 74AS1804 or equivalent inverting buffer.

RESET. Reset is an input that places the MPC in a known state. Only the parts of the MPC involved with initialization of slot and arbitration IDs remain unaffected. RESET is an active high input and should be connected to the $\overline{RST}$ signal on the PSB with a 74AS1804 or equivalent inverting buffer.

If the MPC is used in a CSM implementation, the interconnect microcontroller and some external logic controls RESET. On power up, the CSM generates the RESET signal to the backplane. Within a few clock cycles, receiving MPCs complete their internal reset. Table 5-2 summarizes the states of MPC signal outputs while the RESET signal is active.

Table 5-2. Signal States During Reset

Signal	Reset State	Signal	Reset State
$\overline{BREQ}$	Z(H)	$\overline{ARB}$<5-0>	Z(H)
$\overline{BAD}$<31-0>	Z	D<31-0>	Z
ADDIR	L	$\overline{SEL}$	H
$\overline{REFADR}$	H	$\overline{WAIT}$	H
$\overline{BSC}$<9-0>	Z	ODREQ, IDREQ	L
SCDIR<1,0>	L	MINT, EINT	L
$\overline{BUSERR}$	Z(H)	$\overline{RSTNC}$	L

NOTE:
H = Electrical high state.
L = Electrical low state.
Z = High impedance (tri-state).

$\overline{RSTNC}$ (Reset Not Complete). Agents assert $\overline{RSTNC}$ during reset to extend the initialization time period beyond the time that RESET allows. $\overline{RSTNC}$ is a bidirectional OR-tied signal on the PSB that is low when one or more agents have not completed their reset requirements. Agents cannot perform bus operations while $\overline{RSTNC}$ is asserted. However, agents may access local interconnect space if your firmware implementation allows such access. $\overline{RSTNC}$ is an open-collector signal with high-current drive that connects directly to the PSB.

5.1.5 Exception Operation Signal Group

The exception operation signal group indicates exception errors on the PSB.

$\overline{BUSERR}$ (Bus Error). The MPC asserts $\overline{BUSERR}$ when a data integrity problem on the PSB is detected during a transfer operation. Possible problems are: detection of a parity error on the $\overline{BAD}$ bus or $\overline{BSC}$ lines, or a protocol error associated with the $\overline{BSC}$ lines. $\overline{BUSERR}$ is a bidirectional, open-collector signal with high current drive that connects directly to the PSB.

TIMOUT (Timeout). TIMOUT, as an input from the PSB, is used to detect a bus timeout condition. The CSM activates this signal when it determines that an agent is taking too much time asserting a handshake signal, or if a bus owner has maintained bus ownership for an excessive length of time. The exact amount of time is a fixed value relative to BBCLK that is approximately 10,000 clock cycles (1 ms @ 10 MHz). TIMOUT is an active high input to the MPC and must be connected to the $\overline{TIMOUT}$ signal of the PSB through a 74AS1804 or equivalent inverting buffer.

When the MPC is configured for CSM operation, TIMOUT becomes an output, generating the timeout condition to all agents on the PSB. In this case, the TIMOUT pin should be connected to the PSB by a 74F242 driver or equivalent.

5.2 Dual-Port Memory Control Signals

The MPC provides these signals ($\overline{SEL}$, $\overline{COM}$, $\overline{ERR}$) to support dual-port memory. In order to fully implement dual-port memory, some additional dual-port memory controller logic is required.

$\overline{SEL}$ (Select). The $\overline{SEL}$ output indicates that a dual-port memory access is in progress. $\overline{SEL}$ initiates dual-port operations and may be used to enable the dual-port data buffers onto the $\overline{BAD}$ bus. When the MPC receives the EOT handshake, or if the MPC detects an exception, it deactivates $\overline{SEL}$.

$\overline{COM}$ (Complete). $\overline{COM}$ is an input to the MPC. The dual-port memory controller asserts $\overline{COM}$ to indicate completion of a dual-port access. $\overline{COM}$ is assumed to be synchronous to the bus clock. After the memory controller has asserted $\overline{COM}$, the MPC asserts the replier ready ($\overline{BSC4}$) signal on the next bus clock. The memory controller cannot deassert $\overline{COM}$ until the EOT handshake is complete on the PSB. This requires that the memory controller monitor the PSB for the EOT handshake.

$\overline{ERR}$ (Error). $\overline{ERR}$, an input to the MPC, is asserted by the dual-port memory controller to signal a memory data parity error. $\overline{ERR}$ must be stable (high or low) whenever $\overline{COM}$ is asserted. The MPC responds to this signal by completing the replier handshake on the PSB using a *data error* agent error code. This signal may be asynchronous to the bus clock since it is qualified by the $\overline{COM}$ signal.

5.3 Local Bus Signals

The MPC local bus allows many types of microprocessors, perhaps with differing data widths, byte alignment, and bit ordering, to connect to the MULTIBUS II PSB. This microprocessor is often referred to as the *host CPU* on the MULTIBUS II processor board. The MPC has five signal groups on the local bus:

- data bus
- address/status signals
- transfer control
- interrupt signals
- DMA control lines

5.3.1 DATA BUS

The local data bus is the signal path for data transfers between the host CPU and the MPC.

D<31-0>. D<31-0> is the 32-bit local data bus. Although this is a 32-bit interface, the MPC allows operation with processors using 8-, 16-, or 32-bit data busses.

NOTE:
Intel CPU architecture defines bit 0 and byte 0 as least significant. When connecting non-Intel processors to the MPC local data bus, it is important that this bit and byte ordering be maintained across the PSB. This allows agents of differing CPU types to work together in a single chassis. If byte-swapping is needed, see the discussion of the *byte enable* (BE<3-0>) signal pins.

5.3.2 ADDRESS/STATUS SIGNALS

The address/status signals select or identify all MPC operations over the local bus.

A<5-2> (Address). The address inputs select MPC registers for message and interconnect space operations. A1 and A0 are omitted to provide a consistent register address for all data bus width options. A <5-2> are qualified by $\overline{RD}$ or $\overline{WR}$ and therefore must be stable within the specified set-up and hold window.

$\overline{MEMSEL}$ (Memory Select). This MPC input signal tells the MPC that the current operation is a memory reference across the PSB. $\overline{MEMSEL}$ is qualified by $\overline{RD}$ or $\overline{WR}$ and therefore must be stable within the specified set-up and hold window.

NOTE:
$\overline{MEMSEL}$, $\overline{IOSEL}$, $\overline{REGSEL}$ $\overline{IDACK}$, and $\overline{ODACK}$ are mutually exclusive. In order to be valid, no more than one should be active during the same set-up and hold window.

$\overline{IOSEL}$ (I/O Select). This input signal tells the MPC that the current operation is an I/O reference to the PSB. $\overline{IOSEL}$ is qualified by $\overline{RD}$ or $\overline{WR}$ and therefore must be stable within the specified set-up and hold window.

$\overline{REGSEL}$ (Register Select). This input signal is used to identify MPC register operations. $\overline{REGSEL}$ is qualified by $\overline{RD}$ or $\overline{WR}$ and therefore must be stable within the specified set-up and hold window.

$\overline{LOCK}$. This input signal allows back-to-back operations to be performed on the PSB or local interconnect space. When the bus owner activates $\overline{LOCK}$, all other agents are held off the PSB or local resource until $\overline{LOCK}$ is deactivated.

$\overline{BE}$<3-0> (Byte Enable). These input signals, generated by the host CPU or DMA controller, validate bytes on the data bus. $\overline{BE}$<3-0> are qualified by $\overline{RD}$ or $\overline{WR}$ and therefore must be stable within the specified set-up and hold window. $\overline{BE}$<3-0> correspond to data bytes 3 through 0 on the data bus (where byte 3 is D<31-24>). For remote reference operations, only combinations supported by the IEEE 1296 specification are valid.

A 32-bit local bus requires that all byte enable and data signals are used. For 16-bit local buses, $\overline{BE1}$ and $\overline{BE2}$ are used to indicate which of the two bytes will contain valid data, and only D<15-0> are used. For 8-bit local bus operations, $\overline{BE1}$ and $\overline{BE0}$ are used to select which byte of the PSB will carry the valid data byte. This mode uses ony D<7-0> (on the local bus). Note that during all read operations, the MPC drives all data lines (D<31-0>). Consecutive accesses to message FIFOs must be in ascending byte sequence 0, 1, 2, 3 in any non-overlapping combination.

Table 5-3 shows the valid byte enable combinations for both the local data bus (D<31-0>) and the PSB ($\overline{AD}$<31-0>):

Table 5-3. Valid Byte Enable Combinations

$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	D31–24	D23–16	D15–8	D7–0	AD31–24	AD23–16	AD15–8	AD7–0
L	L	L	L	V3	V2	V1	V0	V3	V2	V1	V0
L	L	L	H	V3	V2	V1	X	V3	V2	V1	X
H	L	L	L	X	V2	V1	V0	X	V2	V1	V0
L	L	H	H	V3	V1	X	X	X	X	V3	V2
H	L	L	H	X	V2	V1	X	X	V2	V1	X
H	H	L	L	X	X	V1	V0	X	X	V1	V0
L	H	H	H	V3	X	X	X	X	X	V3	X
H	L	H	H	X	V2	X	X	X	X	X	V2
H	H	L	H	X	X	V1	X	X	X	V1	X
H	H	H	L	X	X	X	V0	X	X	X	V0
L	H	L	H	X	X	X	V0	X	X	V0	X
L	H	H	L	X	X	X	V0	X	X	X	V0

NOTES:
L = Electrical low state (active)
H = Electrical high state (inactive)
Vn = Valid data bytes
X = Active bytes with undefined data

For the 32-bit host interface, legal combinations of byte enables form *byte lanes:* the paths where valid data bytes are present during a single transfer on the local data bus (as well as in the MULTIBUS II environment). Non-Intel Microprocessors can use byte lanes to perform byte-swapping or other data manipulations in hardware. The figure below illustrates the legal byte lanes as they relate to byte enable combinations:

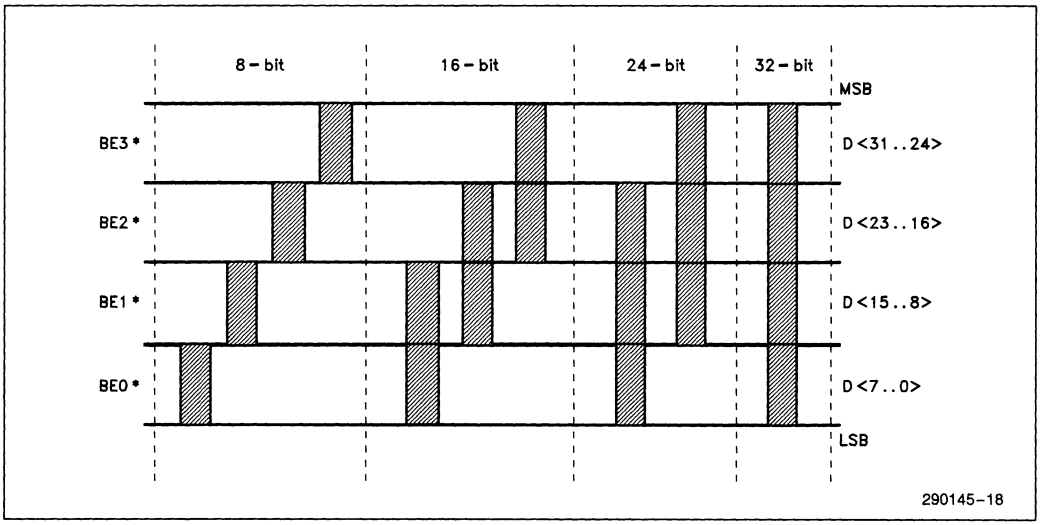


Figure 5-4. Byte Lanes

Each shaded box in Figure 5-4 represents a valid byte lane for a given combination of $\overline{BE}$ during a single read or write operation. There are four types of byte lanes: 8-bit, 16-bit, 24-bit and 32-bit. Bit and byte ordering follow the Intel standard of bit or byte 0 as least significant. Assume that invalid byte lanes contain any value of data (i.e. non-constant). Take precautions (masking in software, etc.) to ensure that invalid data does not cause problems.

When using a DMA controller to handle solicited data transfers to/from local memory, misalignment of data in memory and resulting partial packets are handled using the $\overline{BE}$ lines. The DMA interface of the MPC provides support by only incrementing internal pointers (or detecting completion) when the proper byte-enable signal is active. Table 5-4 shows which $\overline{BE}$ line the MPC recognizes for partial packets:

Table 5-4. Byte Enable Usage for DMA Control

DMA Width	Bytes Remaining	Byte Enable Recognized
32-bit	>3	$\overline{BE3}$
32-bit	3	$\overline{BE2}$
32-bit	2	$\overline{BE1}$
32-bit	1	$\overline{BE0}$
16-bit	>1	$\overline{BE1}$
16-bit	1	$\overline{BE0}$
8-bit	>0	$\overline{BE0}$

5.3.3 TRANSFER CONTROL SIGNALS

Transfer operation control to the MPC over the local bus is provided by two command signals and a wait signal. This handshake provides fully interlocked (two-sided handshake) operation.

$\overline{RD}$ (Read). This input signal starts a read operation. $\overline{RD}$ must transition cleanly, since it is used to qualify other signals in the read operation.

$\overline{WR}$ (Write). This input signal starts a write operation. $\overline{WR}$ must transition cleanly, since it is used to qualify other signals in the write operation.

$\overline{WAIT}$. $\overline{WAIT}$ is an MPC output signal used to extend a transfer operation. The signal will be used by the MPC for all accesses that require synchronization to another resource. It is activated when a command goes active and deactivated when the operation is completed.

5.3.4 INTERRUPT SIGNALS

Interrupt signals are used to inform the host CPU that the MPC requires service. The MPC generates two signals: one for message operations and one for reference errors.

MINT (Message Interrupt). The MINT output signal is used for all message-related signaling to the host CPU. This includes the arrival of an unsolicited message, the availability of the transmit FIFO, the completion of a solicited transfer, and an error-on message transfer.

EINT (Error Interrupt). The EINT output signal is used to signal all errors related to memory, I/O, or interconnect space operations. Internal registers in the MPC provide exact details of the error via interconnect space.

5.3.5 DMA CONTROL SIGNALS

The MPC provides four DMA control signals that connect with an external DMA controller.

ODREQ (Output Channel DMA Request). ODREQ is an output signal that enables DMA transfers to the MPC (i.e., output to the PSB). This signal behaves as a normal DMA request line during solicited message output operations. ODREQ is activated during the transfer phase of a solicited message operation when the solicited output FIFO is empty. The DMA controller responds to ODREQ by moving data from local memory to the FIFO for transfer to a receiving agent on the PSB.

IDREQ (Input Channel DMA Request). IDREQ is an output signal that enables DMA transfers from the MPC (i.e. input from the PSB). This signal behaves as a normal DMA request line during solicited message input operations. IDREQ is activated during the transfer phase of a solicited message operation when the solicited input FIFO is full. The DMA controller responds to ODREQ by moving data from the FIFO to local memory. When the FIFO is emptied, IDREQ is deactivated.

$\overline{ODACK}$ (Output Channel DMA Acknowledge). $\overline{ODACK}$ is generated by the DMA controller in response to an output channel DMA request. $\overline{ODACK}$ is qualified by $\overline{RD}$ or $\overline{WR}$ and therefore must be stable within the specified set-up and hold window.

NOTE:
$\overline{MEMSEL}$, $\overline{IOSEL}$, $\overline{REGSEL}$ $\overline{IDACK}$, and $\overline{ODACK}$ are mutually exclusive. In order to be valid, no more than on should be active during the same set-up and hold window.

$\overline{IDACK}$ (Input Channel DMA Acknowledge). $\overline{IDACK}$ is generated by the DMA controller in response to an input channel DMA request. $\overline{IDACK}$ is qualified by $\overline{RD}$ or $\overline{WR}$ and therefore must be stable within the specified set-up and hold window.

5.4 Interconnect Bus Signals

Brief descriptions of the interconnect bus signal pins are given here. For more information on using the interconnect microcontroller, see the *MPC User's Manual*, Chapter 5, "Interconnect Programming" (Order number 176526-002).

IAD<7-0> (Interconnect Address/Data). IAD<7-0> is an 8-bit, bidirectional, multiplexed address and data bus intended to interface directly to a microcontroller. In addition to the MPC, other interconnect accessible local resources can be connected to this bus.

$\overline{\text{IREQ}}$ (Interconnect Request). The MPC asserts this output signal when an interconnect operation has been requested from either the local bus or the PSB. The MPC asserts $\overline{\text{IREQ}}$ to the interconnect microcontroller at different times for read and write operations. For a read operation, $\overline{\text{IREQ}}$ is asserted immediately after detecting an address match between the requested address and an internal register. For a write operation, $\overline{\text{IREQ}}$ is delayed until valid data is available (i.e., $\overline{\text{BSC3}}$ is asserted). In either case, if the local bus interface has locked the local interconnect space, $\overline{\text{IREQ}}$ is inhibited.

IAST (Interconnect Address Strobe). IAST is a signal from the microcontroller that tells the MPC that a valid address is on the interconnect bus. IAST may be directly connected to the ALE (Address Latch Enable or equivalent) output of most microcontrollers. IAST must provide clean transitions.

$\overline{\text{IRD}}$ (Interconnect Bus Read). The microcontroller asserts $\overline{\text{IRD}}$ to perform a read operation to one of the MPC interconnect interface registers. $\overline{\text{IRD}}$ must provide clean transitions.

NOTE:
When $\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ are activated at the same time, *all* MPC outputs are disabled. Use this feature to disable the MPC in board test applications.

$\overline{\text{IWR}}$ (Interconnect Write). The microcontroller asserts $\overline{\text{IWR}}$ to perform a write operation to one of the MPC interconnect interface registers. $\overline{\text{IWR}}$ must provide clean transitions.

6.0 Package Dimensions

The MPC 82389 is packaged in a 149-pin Ceramic Pin Grid Array (PGA). The pins are arranged 0.100 inch (2.54 mm) center-to-center, in a 15 x 15 matrix. Please refer to Figure 6-3 for case outlines.

A wide variety of sockets are available including the zero-insertion force socket for prototyping.

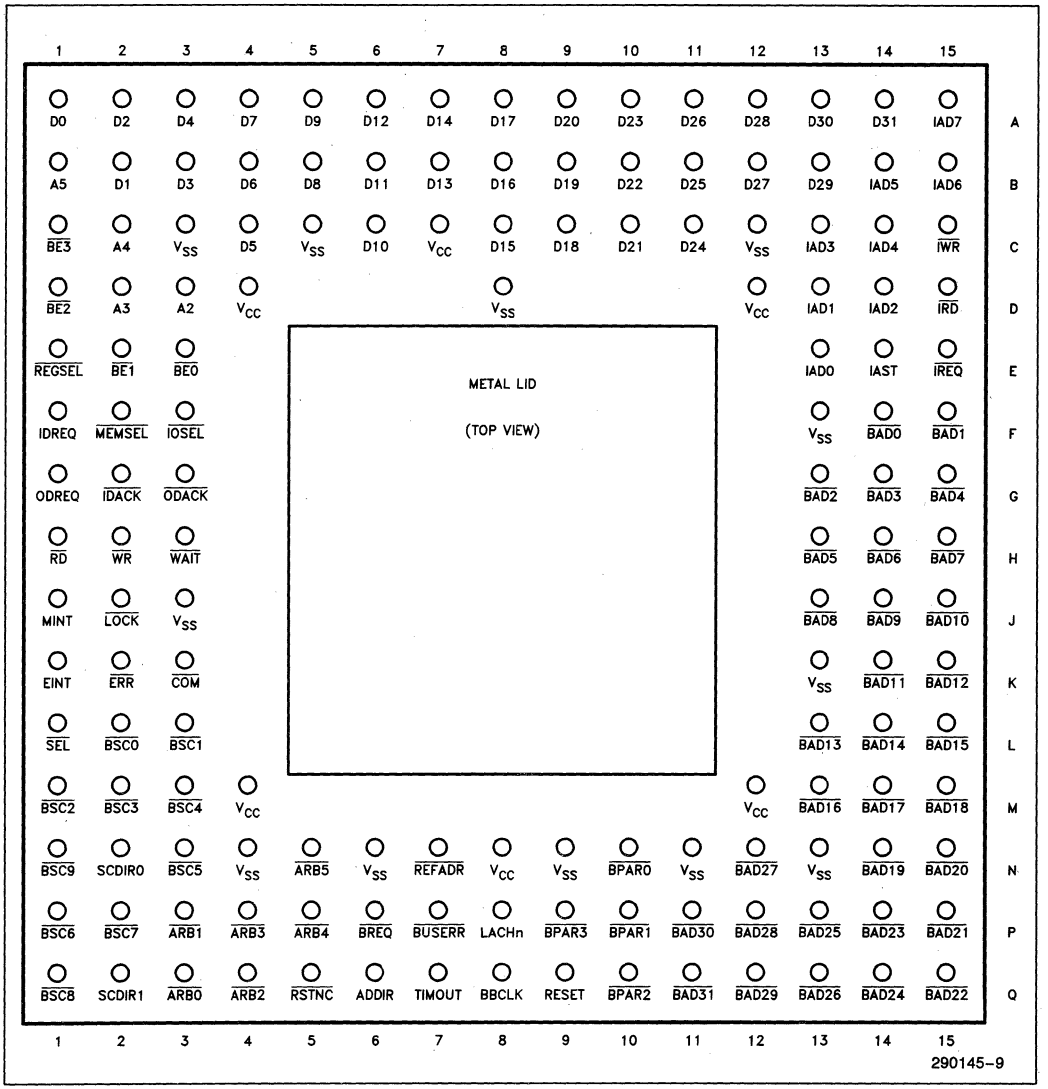


Figure 6-1. MPC 82389 Pinout—View from Top Side

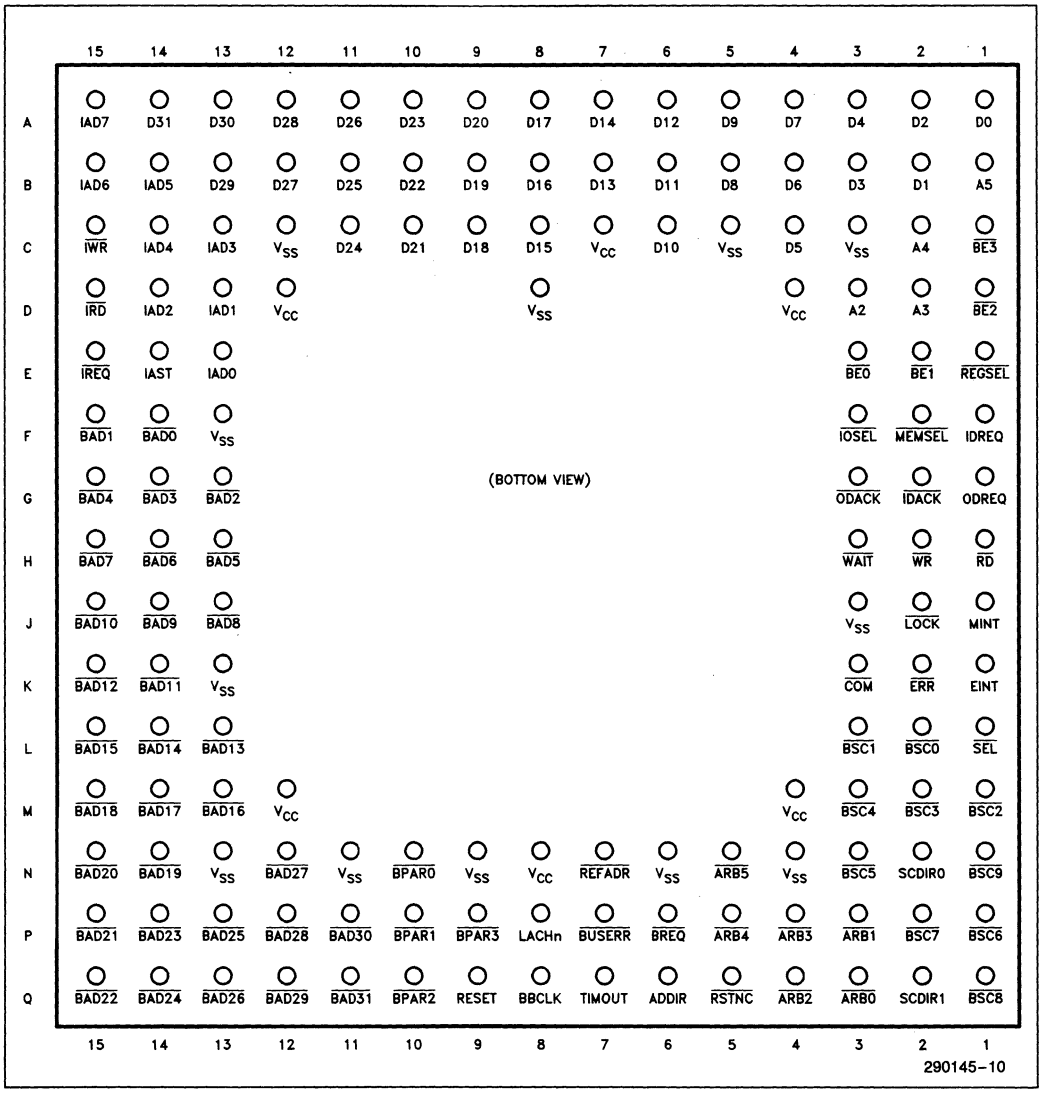


Figure 6-2. MPC 82389 Pinout—View from Pin Side

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Table 6-1. MPC Signal Summary

Mnemonic	Type	Pin #	Mnemonic	Type	Pin #	Mnemonic	Type	Pin #
V_{CC}		D4	REFADR	O	N7	IAST	I	E14
A5	I	B1	ADDIR	O	Q6	$\overline{IRD}$	I	D15
A4	I	C2	$\overline{BPAR3}$	I/O	P9	$\overline{IWR}$	I	C15
A3	I	D2	$\overline{BAD31}$	I/O	Q11	IAD7	I/O	A15
A2	I	D3	$\overline{BAD30}$	I/O	P11	IAD6	I/O	B15
$\overline{BE3}$	I	C1	$\overline{BAD29}$	I/O	Q12	IAD5	I/O	B14
$\overline{BE2}$	I	D1	$\overline{BAD28}$	I/O	P12	IAD4	I/O	C14
$\overline{BE1}$	I	E2	$\overline{BAD27}$	I/O	N12	IAD3	I/O	C13
$\overline{BE0}$	I	E3	$\overline{BAD26}$	I/O	Q13	IAD2	I/O	D14
$\overline{IOSEL}$	I	F3	$\overline{BAD25}$	I/O	P13	IAD1	I/O	D13
$\overline{MEMSEL}$	I	F2	$\overline{BAD24}$	I/O	Q14	IAD0	I/O	E13
$\overline{REGSEL}$	I	E1	$\overline{BAD23}$	I/O	P14	V_{CC}		D12
$\overline{IDACK}$	I	G2	$\overline{BAD22}$	I/O	Q15	V_{SS}		C12
$\overline{ODACK}$	I	G3	$\overline{BAD21}$	I/O	P15	D31	I/O	A14
IDREQ	O	F1	$\overline{BAD20}$	I/O	N15	D30	I/O	A13
ODREQ	O	G1	$\overline{BAD19}$	I/O	N14	D29	I/O	B13
$\overline{WR}$	I	H2	$\overline{BAD18}$	I/O	M15	D28	I/O	A12
$\overline{RD}$	I	H1	$\overline{BAD17}$	I/O	M14	D27	I/O	B12
$\overline{WAIT}$	O	H3	$\overline{BAD16}$	I/O	M13	D26	I/O	A11
V_{SS}		J3	$\overline{BAD15}$	I/O	L15	D25	I/O	B11
MINT	O	J1	$\overline{BAD14}$	I/O	L14	D24	I/O	C11
EINT	O	K1	$\overline{BAD13}$	I/O	L13	D23	I/O	A10
$\overline{LOCK}$	I	J2	$\overline{BAD12}$	I/O	K15	D22	I/O	B10
$\overline{ERR}$	I	K2	$\overline{BAD11}$	I/O	K14	D21	I/O	C10
$\overline{SEL}$	O	L1	$\overline{BAD10}$	I/O	J15	D20	I/O	A9
$\overline{COM}$	I	K3	$\overline{BAD9}$	I/O	J14	D19	I/O	B9
$\overline{BSC9}$	I/O	N1	$\overline{BAD8}$	I/O	J13	D18	I/O	C9
$\overline{BSC8}$	I/O	Q1	$\overline{BAD7}$	I/O	H15	D17	I/O	A8
$\overline{BSC7}$	I/O	P2	$\overline{BAD6}$	I/O	H14	D16	I/O	B8
$\overline{BSC6}$	I/O	P1	$\overline{BAD5}$	I/O	H13	D15	I/O	C8
$\overline{BSC5}$	I/O	N3	$\overline{BAD4}$	I/O	G15	D14	I/O	A7
$\overline{BSC4}$	I/O	M3	$\overline{BAD3}$	I/O	G14	D13	I/O	B7
$\overline{ARB3}$	I/O, OC	P4	V_{SS}		N13	D2	I/O	A2

Table 6-1. MPC Signal Summary (Continued)

Mnemonic	Type	Pin#	Mnemonic	Type	Pin#	Mnemonic	Type	Pin#
$\overline{BSC3}$	I/O	M2	$\overline{BAD2}$	I/O	G13	D12	I/O	A6
$\overline{BSC2}$	I/O	M1	$\overline{BAD1}$	I/O	F15	D11	I/O	B6
$\overline{BSC1}$	I/O	L3	$\overline{BAD0}$	I/O	F14	D10	I/O	C6
$\overline{BSC0}$	I/O	L2	$\overline{BPAR2}$	I/O	Q10	D9	I/O	A5
SCDIR1	O	Q2	$\overline{BPAR1}$	I/O	P10	D8	I/O	B5
SCDIR0	O	N2	$\overline{BPAR0}$	I/O	N10	D7	I/O	A4
V_{CC}		M4	V_{CC}		N8	D6	I/O	B4
V_{SS}		N4	V_{SS}		N9	D5	I/O	C4
$\overline{ARB5}$	I/O, OC	N5	V_{SS}		N11	D4	I/O	A3
$\overline{ARB4}$	I/O, OC	P5	V_{CC}		M12	D3	I/O	B3
$\overline{ARB2}$	I/O, OC	Q4	V_{SS}		F13	D1	I/O	B2
$\overline{ARB1}$	I/O, OC	P3	V_{SS}		K13	D0	I/O	A1
$\overline{ARB0}$	I/O, OC	Q3	BBCLK	I	Q8	V_{CC}		C7
V_{SS}		N6	LACHn	I	P8	V_{SS}		D8
$\overline{BREQ}$	I/O, OC	P6	RESET	I	Q9	V_{SS}		C5
TIMOUT	I/O	Q7	$\overline{RSTNC}$	I/O, OC	Q5	$\overline{BUSERR}$	I/O, OC	P7
$\overline{IREQ}$	O	E15	V_{SS}		C3			

NOTES:
I = input
O = output
I/O = input/output
OC = open-collector
* = active-low

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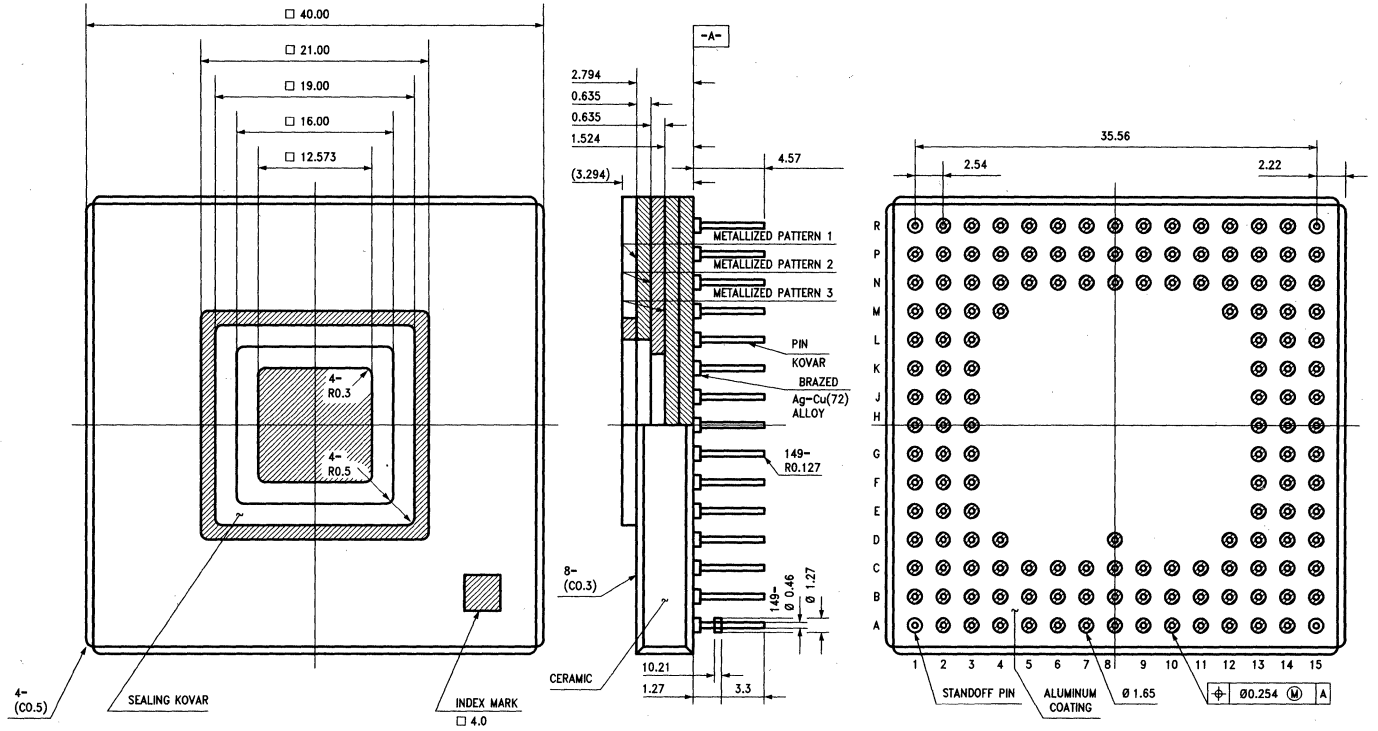

NOTE:
Dimensions in mm.

Figure 6-3. 149-Pin PGA Package Dimensions

7.0 MPC 82389 ELECTRICAL DATA

This section provides detailed A.C. and D.C. specifications for the MPC 82389.

7.1 Maximum Ratings

Operating Temperature
(Under Bias) ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin ..... −0.5V to V_{CC} + 0.5V
Power Dissipation 2.5W

NOTE:
Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those listed in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Although the MPC 82389 contains protective circuitry to resist damage from static electrical discharges, always take precautions against high static voltages or electric fields.

7.2 D.C. Specifications V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C

Table 7-1. D.C. Specifications

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage		0.45	V	I_{OL} Max
V_{OL2}	Output Low Voltage Open Collector		0.55	V	I_{OL} Max
V_{OH}	Output High Voltage	2.4		V	I_{OH} Max
I_{CC}	Power Supply Current		400	mA	
I_L	Input Leakage Current		±10	µA	$0V \le V_{IN} \le V_{CC}$
I_{L1}	Open Collector		±100	µA	$0.4V \le V_{IN} \le 2.4V$
	Leakage Current		±400	µA	$0V \le V_{IN} \le V_{CC}$
I_{L2}	BBCLK Input Leakage Current		±100	µA	$0V \le V_{IN} \le V_{CC}$
I_{OL}	Output Low Current	4.0		mA	V_{OL} = 0.45V
I_{OL1}	Open Collector Output Low Current	60.0		mA	V_{OL} = 0.55V
I_{OL2}	ADDIR and $\overline{\text{REFADR}}$ Output Low Current	8.0		mA	V_{OL} = 0.45V
I_{OH}	Output High Current	−1.0		mA	V_{OH} = 2.4V
C_I	Input Capacitance		10	pF	f_C = 1 MHz, 25°C (Note 1)
C_{IO}	I/O Capacitance		20	pF	f_C = 1 MHz, 25°C (Note 1)
C_{CLK}	Clock Input Capacitance		15	pF	f_C = 1 MHz, 25°C (Note 1)
C_{OC}	Open Collector Capacitance		20	pF	f_C = 1 MHz, 25°C (Note 1)

NOTE:
1. Sampled only, not 100% tested.

7.3 A.C. Specifications

The A.C. specifications for the MPC 82389 are specified in Tables 7-2, 7-3 and 7-4 and Figures 7-2, 7-3, 7-4 and 7-5. Figure 7-1 specifies the test points for measuring the A.C. parameters. Table 7-2 and Figures 7-2 and 7-3 specify the A.C. parameters for the host CPU bus. Table 7-3 and Figure 7-4 specify the A.C. parameters for the interconnect bus. Table 7-4 and Figure 7-5 specify the A.C. parameters for the PSB. Figure 7-6 defines the test load for the A.C. specifications.

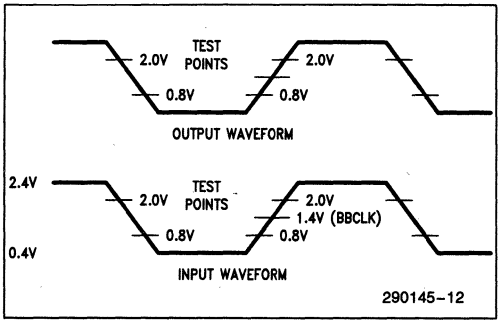

Figure 7-1. A.C. Test Waveforms

Table 7-2. Host CPU Bus A.C. Specifications (V_{CC} = 5V ±5%, T_A = 0°C to +70°C)

Symbol	Parameter	Min	Max	Units	Test Conditions
t_1	Address and $\overline{BE}$ Setup to Command Active	20		ns	
	Select and DACK Setup to Command Active	18		ns	
t_2	Address, $\overline{BE}$, Select and DACK Hold from Command Active	5		ns	
t_3	Time between Commands	24		ns	
t_4	Command Inactive to Read Data Disable (Note 5)		15	ns	
t_5	Read Data Hold from Command Inactive	3		ns	
t_6	Read Data Enable from Command Active	0		ns	
t_7	$\overline{WAIT}$ Active from Command Active		20	ns	C_L = 50 pF
t_8	Command Inactive from $\overline{WAIT}$ Inactive	0		ns	
t_9	$\overline{WAIT}$ Inactive to Read Data Valid		25	ns	C_L = 90 pF
t_{10}	Command Active to Write Data Valid		200	ns	
t_{11}	Write Data Hold from $\overline{WAIT}$ Inactive	0		ns	
t_{12}	Command Active to $\overline{LOCK}$ Active (Note 1)		100	ns	
t_{13}	$\overline{LOCK}$ Hold from $\overline{WAIT}$ Inactive (Note 2)	0		ns	
t_{14}	Command Active Time	42		ns	
t_{15}	Read Data Valid from Command Active		42	ns	C_L = 90 pF
t_{16}	Write Data Setup to Command Inactive —Registers —DMA	 20 20		 ns ns	
t_{17}	Write Data Hold from Command Inactive	3		ns	
t_{18}	Command Active to MINT or DREQ Inactive (Notes 3, 4)		42	ns	C_L = 50 pF
t_{19}	Command Active to DREQ Inactive (Note 4)		25	ns	C_L = 50 pF

NOTES:
1. Required to guarantee locking of resource.
2. Required to guarantee resource remains locked.
3. MINT deassertion only if no other sources are pending.
4. For DREQ inactive timing, t_{19} applies to a normal last transfer deassert condition and t_{18} to an error deassert condition.
5. Disable condition occurs when the output current becomes less than the input leakage specification.

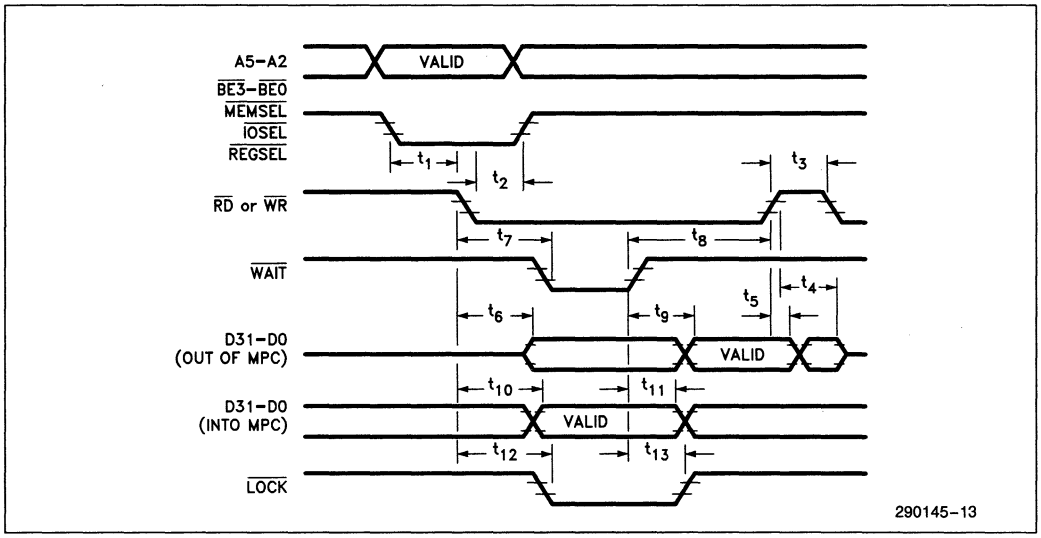

Figure 7-2. Host CPU Interface Reference Operation Timing

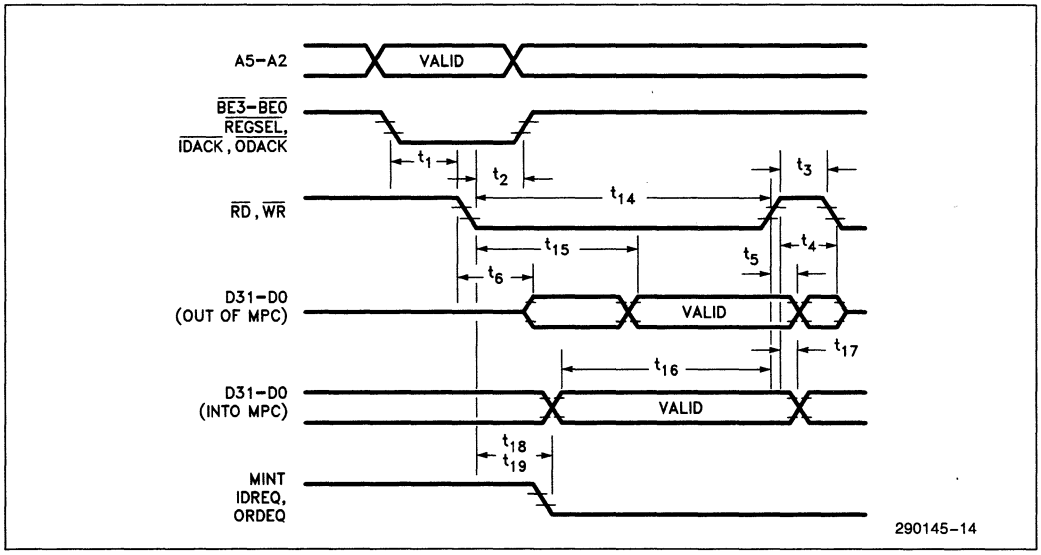

Figure 7-3. Host CPU Interface Register and DMA Operation Timing

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Table 7-3. Interconnect Bus A.C. Specifications (V_{CC} = 5V ±5%, T_A = 0°C to +70°C)

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{31}	IAST Active Time	85		ns	
t_{32}	Command Active Time	250		ns	
t_{33}	Command Inactive to IAST Active	25		ns	
t_{33A}	IAST Inactive to Command Active	120		ns	
t_{34}	Address Setup to IAST Inactive	40		ns	
t_{35}	Address Hold from IAST Inactive	20		ns	
t_{36}	Write Data Setup to Command Inactive	120		ns	
t_{37}	Write Data Hold from Command Inactive	5		ns	
t_{38}	Read Data Enable from Command Active	0		ns	
t_{39}	Read Data Valid from Command Active		120	ns	C_L = 150 pF
t_{40}	Read Data Hold from Command Inactive	0		ns	
t_{41}	Read Data Disable from Command Inactive (Note 2)		30	ns	
t_{42}	EINT, $\overline{IREQ}$ Inactive from Command Active (Note 1)		100	ns	C_L = 150 pF

NOTES:
1. EINT inactive only on write to error register. $\overline{IREQ}$ inactive only on write to arbitration register.
2. Disable condition occurs when the output current becomes less than the input leakage specification.

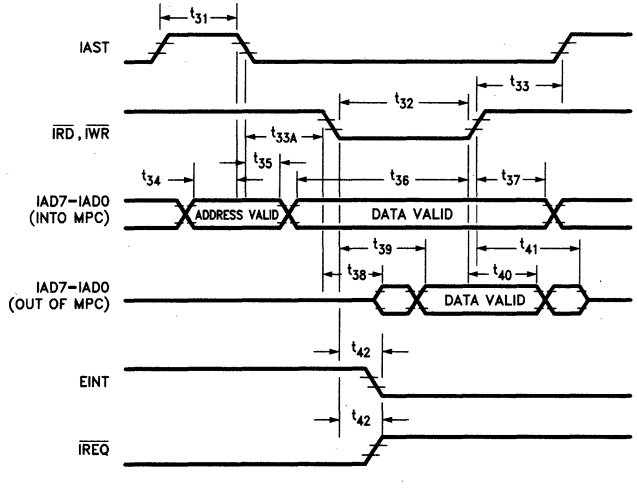

Figure 7-4. Interconnect Bus Timing

Table 7-4. PSB Interface A.C. Specifications (V_{CC} = 5V ±5%, T_A = 0°C to +70°C)

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{CP}	Clock Period	99.9		ns	
*t_{CL}	$\overline{BCLK}$ Low Time	40		ns	
*t_{CH}	$\overline{BCLK}$ High Time	40		ns	
t_{BCL}	BBCLK Low Time	38		ns	
t_{BCH}	BBCLK High Time	38		ns	
t_{RB}	$\overline{BCLK}$ Rise Time	1	5	ns	
t_{FB}	$\overline{BCLK}$ Fall Time	1	2	ns	
t_R	BBCLK Rise Time	0.5	1	ns	
t_F	BBCLK Fall Time	0.5	1	ns	
t_{SK}	$\overline{BCLK}$ to BBCLK Skew (Note 1)	−0.5	4.0	ns	
t_{CD}	Clock to Output Delay				
	$\overline{BREQ}$, $\overline{BUSERR}$, $\overline{RSTNC}$ (Note 2)		36	ns	C_L = 500 pF
	$\overline{ARB5}$–$\overline{ARB0}$ (Notes 2, 3)		36	ns	C_L = 500 pF
	$\overline{BAD31}$–$\overline{BAD0}$, $\overline{BSC7}$–$\overline{BSC0}$		29	ns	C_L = 75 pF
	$\overline{BPAR3}$–$\overline{BPAR0}$, $\overline{BSC9}$, $\overline{BSC8}$		29	ns	C_L = 50 pF
	SCDIR0, SCDIR1 (H to L)		19	ns	C_L = 25 pF
	(L to H)		21	ns	C_L = 25 pF
	ADDIR (L to H)		21	ns	C_L = 50 pF
	(H to L)		27	ns	C_L = 50 pF
	$\overline{REFADR}$		29	ns	C_L = 75 pF
	$\overline{SEL}$		29	ns	C_L = 50 pF
t_H	Hold Time from Clock				
	$\overline{BREQ}$, $\overline{BUSERR}$, $\overline{RSTNC}$	6.5		ns	C_L = 25 pF
	$\overline{ARB5}$–$\overline{ARB0}$ (Note 3)	6.5		ns	C_L = 25 pF
	$\overline{BAD31}$–$\overline{BAD0}$, $\overline{BPAR3}$–$\overline{BPAR0}$	5.0		ns	C_L = 15 pF
	$\overline{BSC9}$–$\overline{BSC0}$	4.0		ns	C_L = 15 pF
	SCDIR0, SCDIR1	4.0		ns	C_L = 15 pF
	ADDIR	5.0		ns	C_L = 25 pF
	$\overline{REFADR}$	4.0		ns	C_L = 25 pF
	$\overline{SEL}$	4.0		ns	C_L = 15 pF
t_{ON}	Turn On Delay from Clock (Note 4)				
	$\overline{BREQ}$, $\overline{BUSERR}$, $\overline{RSTNC}$	6.5		ns	
	$\overline{ARB5}$–$\overline{ARB0}$ (Note 1)	6.5		ns	
	$\overline{BAD31}$–$\overline{BAD0}$, $\overline{BPAR3}$–$\overline{BPAR0}$	5.0		ns	
	$\overline{BSC9}$–$\overline{BSC0}$	4.0		ns	
t_{OFF}	Turn Off Delay from Clock (Note 5)				
	$\overline{BREQ}$, $\overline{BUSERR}$, $\overline{RSTNC}$		36	ns	
	$\overline{ARB5}$–$\overline{ARB0}$ (Note 3)		36	ns	
	$\overline{BAD31}$–$\overline{BAD0}$, $\overline{BPAR3}$–$\overline{BPAR0}$		29	ns	
	$\overline{BSC9}$–$\overline{BSC0}$		29	ns	

*t_{CL} and t_{CH} are MULTIBUS II specifications.

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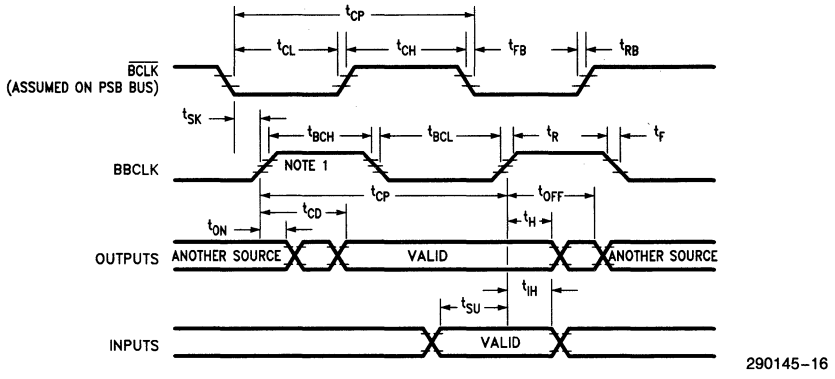
Table 7-4. PSB Interface A.C. Specifications (V_{CC} = 5V ±5%, T_A = 0°C to +70°C) (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{SU}	Input Setup Time to Clock				
	$\overline{BREQ}$, $\overline{BUSERR}$, $\overline{RSTNC}$	22		ns	
	$\overline{ARB5}$–$\overline{ARB0}$ (Note 3)	40		ns	
	$\overline{BAD31}$–$\overline{BAD0}$, $\overline{BPAR3}$–$\overline{BPAR0}$	24		ns	
	$\overline{BSC9}$–$\overline{BSC0}$	24		ns	
	TIMEOUT, LACHn, RESET	24		ns	
	$\overline{COM}$, $\overline{ERR}$	40		ns	
t_{IH}	Input Hold Time from Clock				
	$\overline{BREQ}$, $\overline{BUSERR}$, $\overline{RSTNC}$	0		ns	
	$\overline{ARB5}$–$\overline{ARB0}$ (Note 3)	0		ns	
	$\overline{BAD31}$–$\overline{BAD0}$, $\overline{BPAR3}$–$\overline{BPAR0}$	3		ns	
	$\overline{BSC9}$–$\overline{BSC0}$	2		ns	
	TIMEOUT, LACHn, RESET	2		ns	
	$\overline{COM}$, $\overline{ERR}$	3		ns	

NOTES:
1. The clock timings are provided to reference the MPC specification to the PSB specifications. These specifications assume a 74AS1804 or equivalent buffer.
2. The 500 pF load is a distributed load as defined in the PSB specification. The open drain signals are designed such that the output delay and bus loss meets the PSB specification requirement.
3. The $\overline{ARB5}$–$\overline{ARB0}$ signal timings are with respect to the first and last clock of the arbitration period. Details can be found in the PSB specification. Also, the arbitration logic has been designed to meet the loop delay specification accounting for the full path of input to output plus bus loss.
4. Minimum turn on times are measured the same way as hold times. Specifically, the logic level driven by another device on the previous clock cycle must not be disturbed.
5. Maximum turn off times are measured to the condition where the output leakage current becomes less than the input leakage specification.
6. All stated capacitances are based on design requirements. Production test limitations may require some parameters to be tested under a different condition.



NOTE:
1. SAMPOINT point for BBCLK is 1.4V.

Figure 7-5. PSB Interface Timing

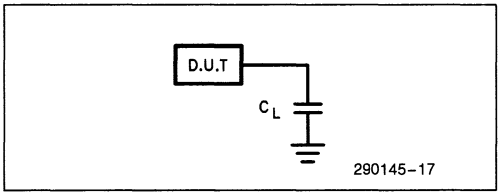


Figure 7-6. A.C. Test Load

8.0 REFERENCE DOCUMENTS

Part Number	Title Description
176526-002	MPC User's Manual
146077	MULTIBUS II Architecture Specifications
149299	Interconnect Interface Specifications
149300	MULTIBUS II MPC External Product Specifications
149247	MULTIBUS II Transport Protocol Specifications
459706-001	CSM/002 Hardware Reference Manual

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