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APPLICATION BRIEF

2/4/8-Mbit SmartVoltage Boot Block Flash Memory Family Overview

COLLIN K. ONG
TECHNICAL MARKETING ENGINEER

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1.0 INTRODUCTION

This document includes a feature overview, pinouts, and memory maps for Intel's SmartVoltage boot block family, including 2/4/8-Mbit densities. These products offer feature and function compatibility, including the SmartVoltage technology (SVT) outlined below. Follow the design steps in Section 5.0 to upgrade 12V V_{PP} designs to SVT.

2.0 BOOT BLOCK ARCHITECTURE

Intel's boot block architecture products offer the familiar features that optimize it for updateable firmware storage. These features include:

- Hardware-lockable boot block for secure kernel code storage
- Parameter blocks for parameter storage
- Main blocks for modular code updates, facilitating updateable firmware
- x8 or x16 user-selectable I/O operation
- RP# for reset and write protection
- PSOP and TSOP packages

Intel has integrated its SmartVoltage technology into the boot block family in order to increase the voltage flexibility of these components.

3.0 PINOUT COMPATIBLE DENSITY UPGRADES

In addition, Intel is providing density upgrades with pinout compatibility for the 2-Mbit, 4-Mbit, and 8-Mbit densities. The pinouts in Figures 2, 3, and 4 illustrate these compatible upgrade paths.

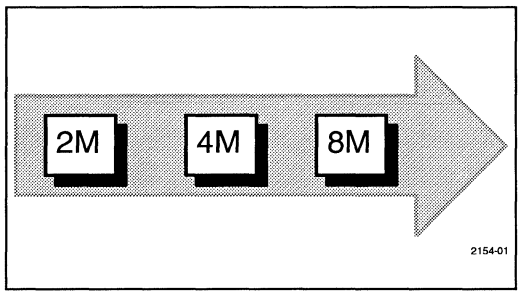


Figure 1. The SmartVoltage Technology Boot Block Line Features a Pinout-Compatible Upgrade Path

4.0 NEW SmartVoltage TECHNOLOGY FEATURES

SmartVoltage offers the following new features:

1. Voltage Flexibility

- V_{CC} = 2.7–3.6V, 3.3V ±0.3V or 5V ±10% with enhanced circuits to optimize low-voltage performance when low power consumption is critical.
- Program/Erase operation with V_{PP} = 5V for convenient in-system writes without a DC–DC converter or V_{PP} = 12V when write/erase performance is a concern, such as during production.

2. Write Protection

- WP# pin replaces a DU pin and is used in conjunction with the V_{PP} and RP# pins, as detailed in the table below, to control write protection of the boot block. (WP# pin not available on 8-Mbit 44-lead PSOP. In this package, treat as if the WP# pin is internally tied low, effectively eliminating the last row of the table below.)

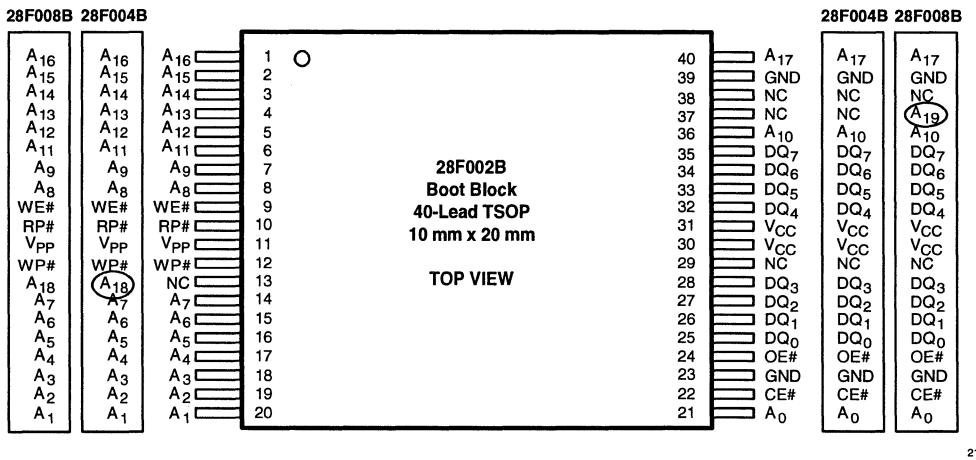
V_{PP}	RP#	WP#	Write Protection
V_{IL}	X	X	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	X	All Blocks Locked (Reset)
$\geq V_{PPLK}$	V_{HH}	X	All Blocks Unlocked
$\geq V_{PPLK}$	V_{IH}	V_{IL}	Boot Block Locked
$\geq V_{PPLK}$	V_{IH}	V_{IH}	All Blocks Unlocked

5.0 UPGRADING FROM 12V TO SVT

If you have designs using 12V V_{PP} boot block products, you must adhere to the following design steps to ensure you can upgrade to SVT:

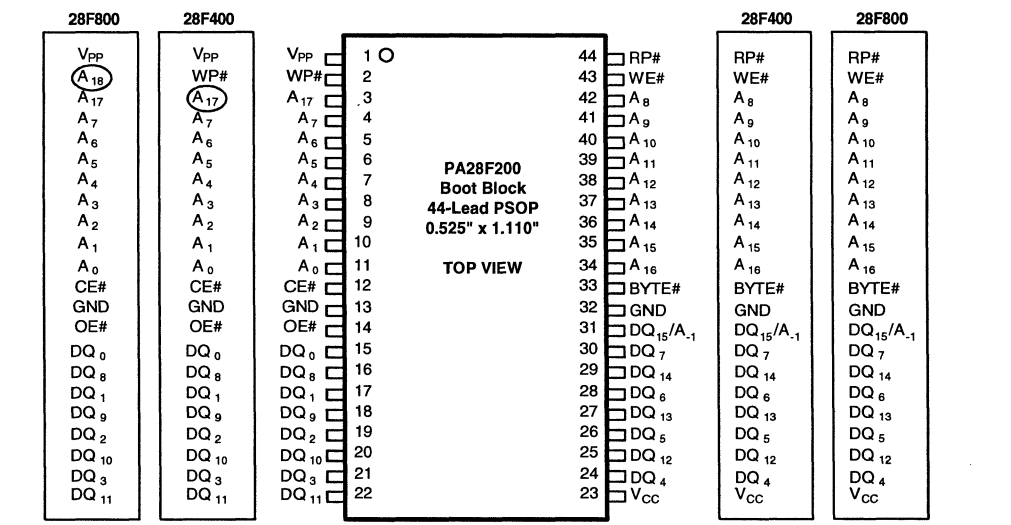
1. If using 5V program/erase, allow for connecting V_{PP} to 5V and disconnecting V_{PP} from 12V.
2. If adding a switch on V_{PP} for write protection, switch to GND instead of V_{CC}.
3. Connect WP# (DU on existing products) to V_{CC}, GND, or a control signal. This pin should not be left floating. The DU pin on BX/BL products can be driven to a logic-level in order to provide upgrade compatibility.

6.0 PACKAGE PINOUTS



NOTE: The 28F008B pinout shown is for the 8-Mbit boot block, and not the 28F008SA FlashFile™ memory.

Figure 2. The 40-Lead TSOP Offers the Smallest Form Factor for Space-Constrained Applications



NOTE: For the 8-Mbit device, pin 2 has been changed to A_{18} (WP# on 2/4-Mbit). Designers planning to upgrade to the 8-Mbit density from the 2/4-Mbit density in this package should design pin 2 to control WP# functionality at the 2/4-Mbit level and allow for pin 2 to control A_{18} after upgrading to the 8-Mbit density.

Figure 3. The 44-Lead PSOP Offers a Convenient Upgrade from JEDEC ROM Standards

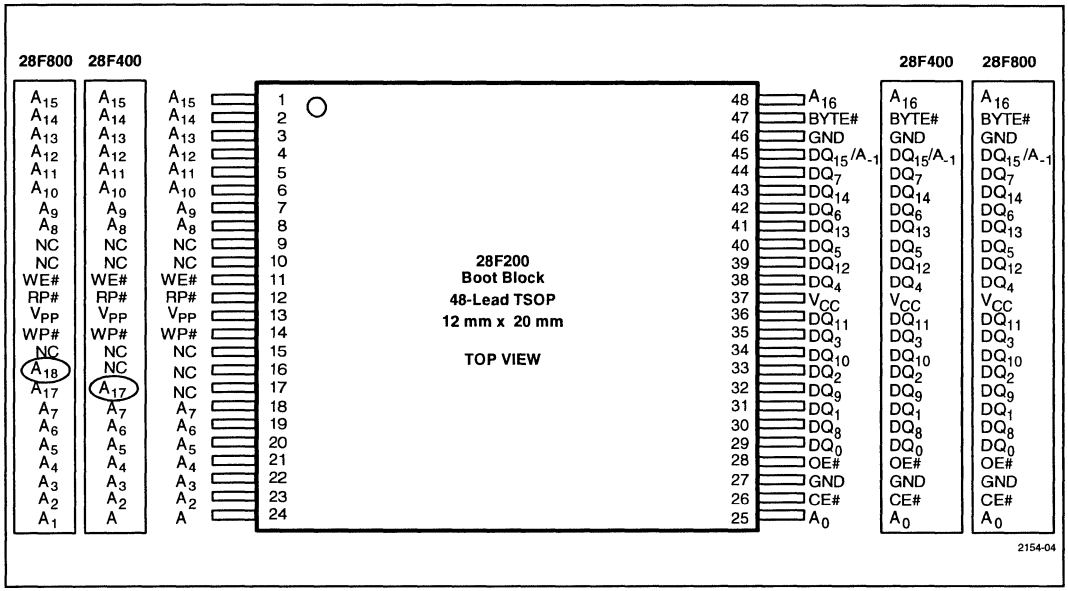


Figure 4. The 48-Lead TSOP Offers the Smallest Form Factor for x16 Operation

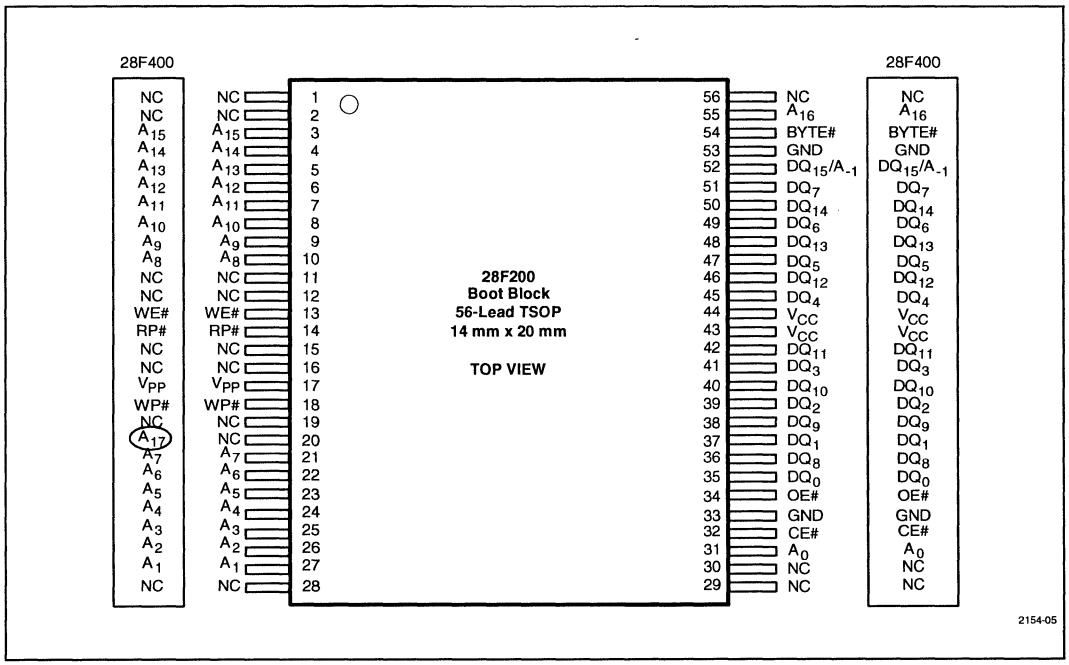
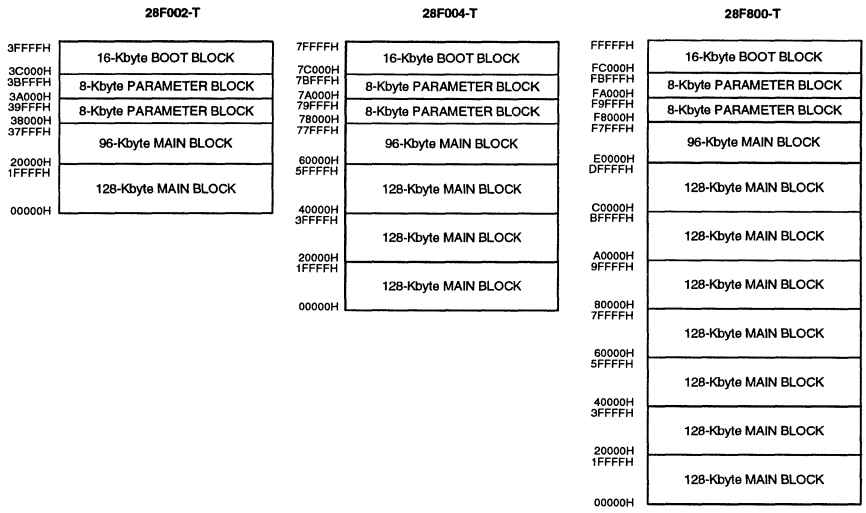


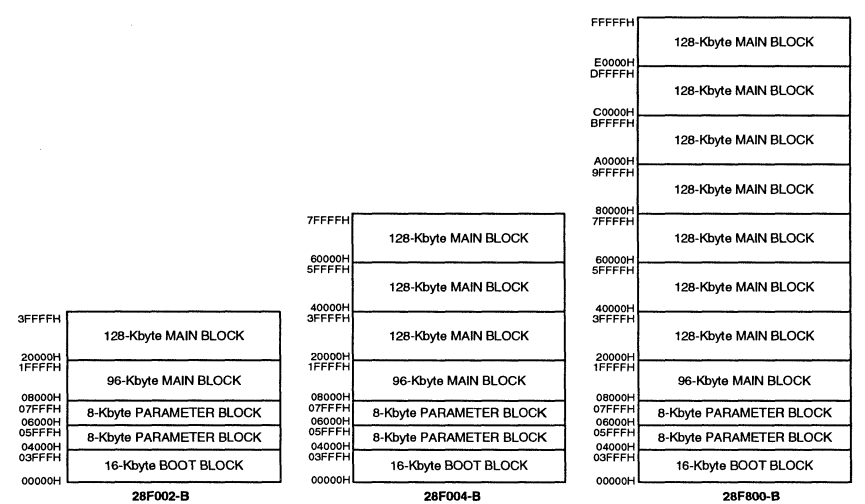
Figure 5. The 56-Lead TSOP Offers Compatibility between 2 and 4 Mbits

7.0 MEMORY MAPS



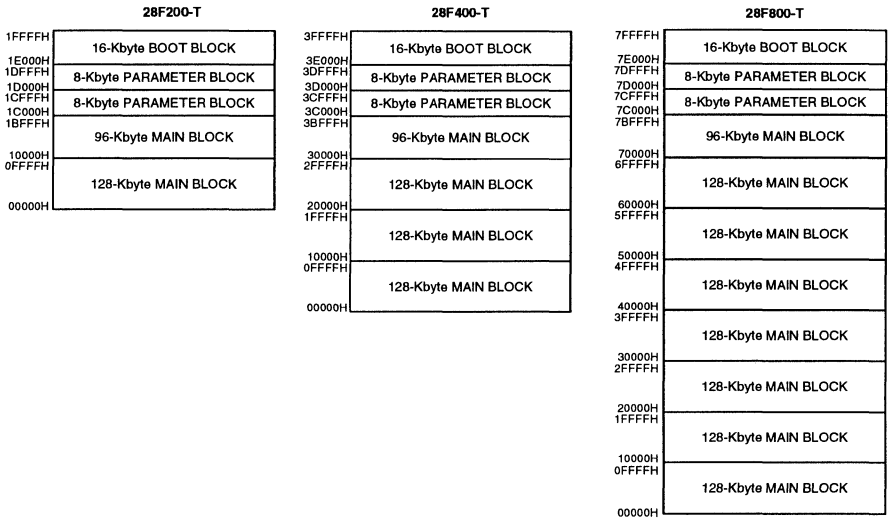
NOTE: These memory maps apply to the 28F002/004/008-T components, or the 28F200/400/800-T components in byte-wide (x8) mode.

Figure 6. Byte-Wide x8-Mode Memory Maps (Top Boot)



NOTE: These memory maps apply to the 28F002/004/008-B components, or the 28F200/400/800-B components in byte-wide (x8) mode.

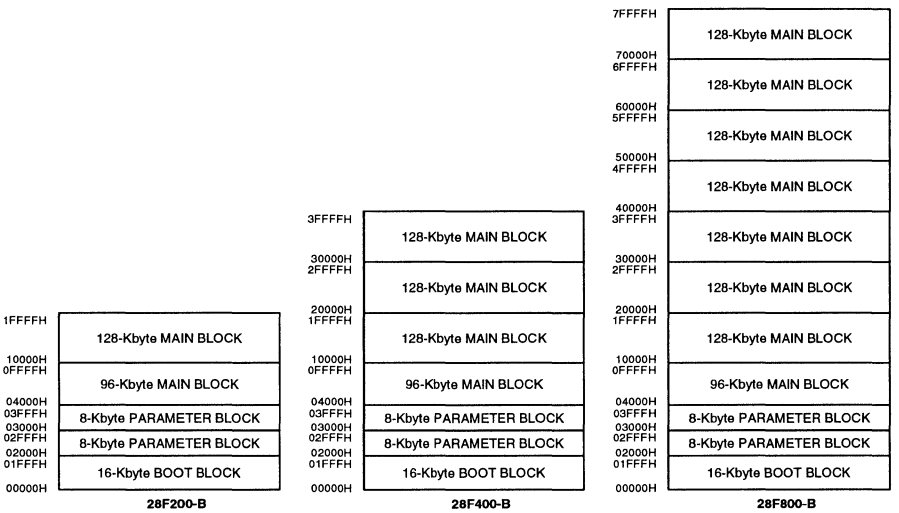
Figure 7. Byte-Wide x8-Mode Memory Maps (Bottom Boot)



(Word addresses shown)

NOTE: These memory maps apply to the denoted 28F200/400/800-T components in word-wide (x16) mode.

Figure 8. Word-Wide x16-Mode Memory Maps (Top Boot)



(Word addresses shown)

NOTE: These memory maps apply to the denoted 28F200/400/800-B components in word-wide (x16) mode.

Figure 9. Word-Wide x16-Mode Memory Maps (Bottom Boot)

8.0 PRODUCT OFFERINGS

12V Program/Erase Boot Block Products

Product	Density x Org.	Pkg.	Speed (ns) (V_{CC} = 5V)	Speed (ns) (V_{CC} = 3.3V)	Extended Temperature
28F001BX	1 Mb, 128Kx8	P, N, E	70, 90, 120, 150		√
28F200BX	2 Mb, 256Kx8/128Kx16	PA, E	60, 80, 120		√
28F002BX	2 Mb, 256Kx8	E	60, 80, 120		√
28F200BL	2 Mb, 256Kx8/128Kx16	PA, E	(1)	150	√(2)
28F002BL	2 Mb, 256Kx8	E	(1)	150	√(2)
28F400BX	4 Mb, 512Kx8/256Kx16	PA, E	60, 80, 120		√
28F004BX	4 Mb, 512Kx8	E	60, 80, 120		√
28F400BL	4 Mb, 512Kx8/256Kx16	PA, E	(1)	150	√(2)
28F004BL	4 Mb, 512Kx8	E	(1)	150	√(2)

NOTES:

1. The BL products also operate at 5V V_{CC} for programmer compatibility.
2. –20°C – +70°C operating range for Read; –0°C – +70°C for program and erase.

SmartVoltage Boot Block Products

Product	Density x Org.	Pkg	Speed (ns) (V_{CC} = 5V)	Speed (ns) (V_{CC} = 3.3V)	Speed (ns) (V_{CC} = 2.7V)	Extended Temp.
28F200BV	2 Mb, 256Kx8/128Kx16	44, 56	60, 80, 120	110, 150, 180		√
28F200CV	2 Mb, 256Kx8/128Kx16	48	60, 80, 120	110, 150, 180		√
28F002BV	2 Mb, 256Kx8	40	60, 80, 120	110, 150, 180		√
28F400BV	4 Mb, 512Kx8/256Kx16	44, 56	60, 80, 120	110, 150, 180		√
28F400CV	4 Mb, 512Kx8/256Kx16	48	60, 80, 120	110, 150, 180		√
28F004BV	4 Mb, 512Kx8	40	60, 80, 120	110, 150, 180		√
28F800BV	8 Mb, 1024Kx8/512Kx16	44	70,120	120,150		√
28F800CV	8 Mb, 1024Kx8/512Kx16	48	70,120	120,150		√
28F008BV	8 Mb, 1024Kx8	40	70,120	120,150		√
28F800CE	8 Mb, 1024Kx8/512Kx16	48	90		120	√
28F008BE	8 Mb, 1024Kx8/512Kx16	40	90		120	√

NOTE:

1. BV products also operate at V_{CC} = 5V for high-performance.
2. BE/CE products operate over the V_{CC} ranges 2.7–3.6V and 5V ±10%.

9.0 ORDERING INFORMATION

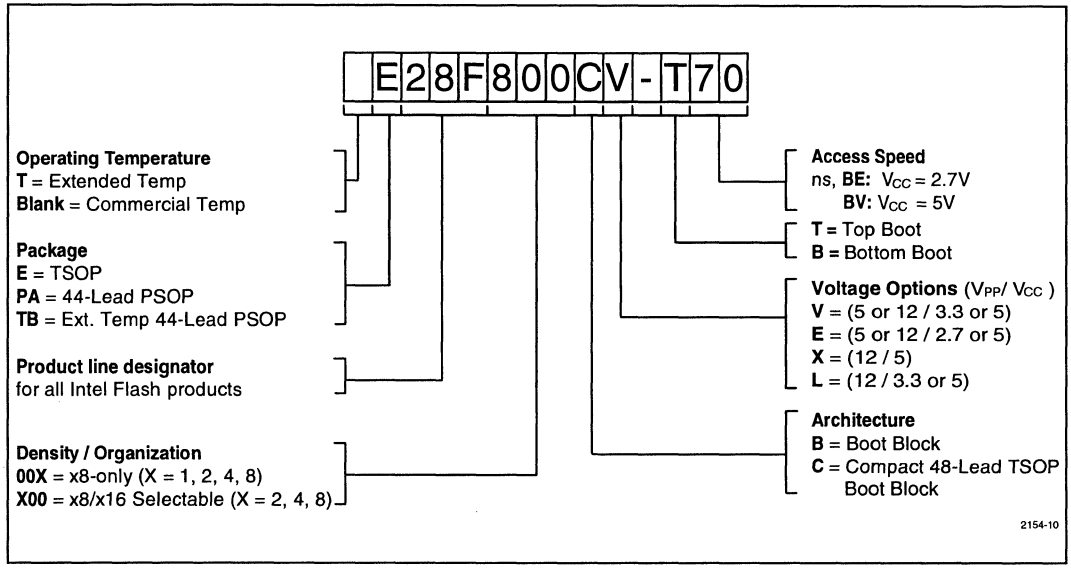


Figure 10. Decoding the Product Names

10.0 ADDITIONAL INFORMATION

10.1 Revision History

Number	Description
-001	Original Version
-002	Text updated. DU and WP# pin usage clarified. Note and "B" suffixes added to Figure 2. SmartVoltage Boot Block Products table: Speeds added to 28F800 and 28F008, 2.7V products added. Figure 10 updated.

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