Memory System Design with the Intel® 2107B 4K RAM

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A9   V_SS   A8   A7

A6–A11 DECODERS

A6

A10

A11

V_DD

32 X 64 CELL ARRAY

CS

D_IN

CE

A0–A5 DECODERS

COLUMN SENSE AMPLIFIERS

32 X 64 CELL ARRAY

A5

D_OUT

A4

A0

A1   A2   V_CC   WE   A3
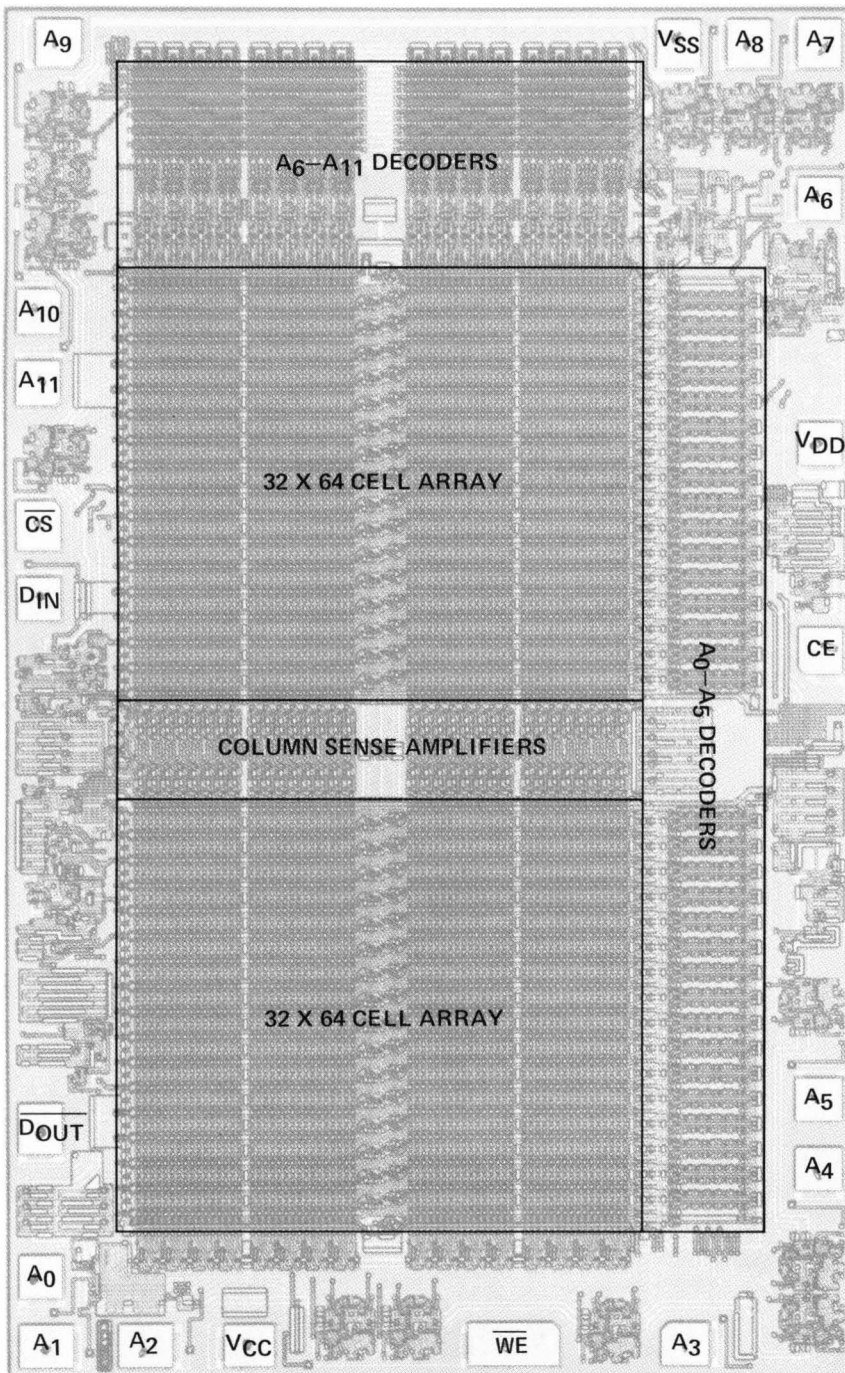
TOPOGRAPHY OF THE 2107B

Memory System Design with the Intel® 2107B 4K RAM

Contents

INTRODUCTION

The Intel® 2107B is a 4096 word by 1 bit dynamic random access memory. The 2107B is fabricated using Intel's standard reliability proven n-channel silicon gate MOS technology. The device is packaged in a standard 22-pin DIP. The pin configuration and logic symbol are shown in Figure 1. Note that the 2107B can be used as a replacement for the 2107A.

LOGIC SYMBOL

2107B

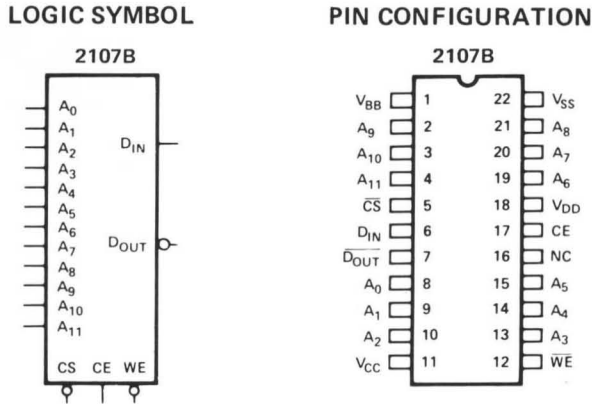**PIN CONFIGURATION**

2107B

Figure 1. 2107B Logic Symbol and Pin Configuration

The combination of Intel's® n-channel silicon gate process and circuit design has resulted in a part that is very fast, easy to use, and economically produced in large volume. In addition, the combination of process and device design has resulted in a very small device (see Figure 2) using conservative layout rules (same as 2102A). The small size offers advantages in both large volume production and increased reliability. The 2107B operates with three power supplies relative to ground; V_{DD} (+12V), V_{BB} (−5V), and V_{CC} (+5V). The V_{CC} (+5V) supply is connected only to the output buffer of the 2107B and may be turned off during power down operations.

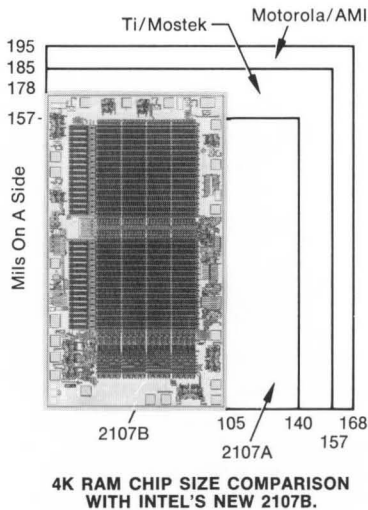**4K RAM CHIP SIZE COMPARISON WITH INTEL'S NEW 2107B.**

Figure 2. 2107B Comparative Die Size

The 2107B has one MOS level clock (Chip Enable) with all other inputs being low level TTL compatible (+2.4V V_{IH} minimum). The output is capable of driving 1 TTL load.

The purpose of this application note is to describe the internal operation of the 2107B, outline those areas in system implementation to which the designer should pay particular attention and to discuss typical examples of the uses of the 2107B in systems environment. The application note is arranged so that each of the above sections can be read independently of each other without having to go through any unwanted detail in the other sections.

INTERNAL DEVICE OPERATION

Internal operation of the 2107B is most easily understood with the aid of the block diagram shown in Figure 3. As is shown in this figure, the memory array is arranged in a 64 row × 64 column matrix of storage cells. The storage cells are implemented with a single transistor and a "storage" capacitor and are called single transistor cells. The operation of the storage cell will be discussed later. The memory cell is accessed by the coincidence of a row select (defined by addresses $A_0 - A_5$) and a column select (defined by addresses $A_6 - A_{11}$) signal at the desired address. An on chip timing and control generator provides for the internal timing signals for decoding, read/write strobing, data gating and output gating. All of the timing circuits in the 2107B are activated by the positive-going edge of chip enable.

Chip select controls the data I/O gating circuits internal to the 2107B. When chip select is high the output data buffer is in a high impedance state and
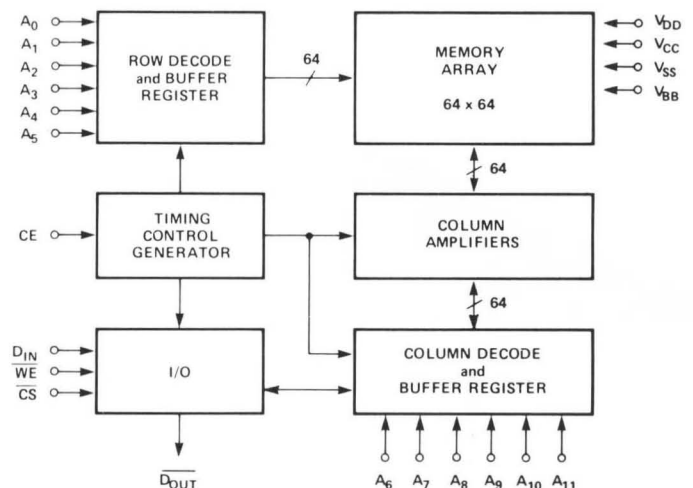
BLOCK DIAGRAM

Figure 3. 2107B Block Diagram

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the data-in buffer is electrically isolated from the data-in input pin. Since chip select controls only the internal data buffers and not the timing generators or address buffers internal to the 2107B, it is possible to refresh the 2107B with chip select high by initiating a read/refresh or write cycle.

The address buffer registers consist of latches activated at the leading edge of chip enable. Since the addresses are latched shortly after chip enable goes high, it is permissible to change the address long before the memory cycle is completed to set up for the next cycle.

The write enable input activates the data-in buffer gating data to the selected memory cell. Input data must be valid at the time write enable goes low to assure that the proper data is written into memory.

Circuit implementation and operation of each of the major input/output and storage portions are discussed below.

Storage Cell Operation

The storage cell used in the 2107B is implemented with a single transistor and storage capacitor as shown in Figure 4. From this figure it is shown that a charge on a storage cell is gated to the bit sense line by the MOS device connected to the column select line. (Note that for a given column select, 64 storage devices are gated to the respective 64 bit sense lines.)

Consider first a read operation and the case where the storage capacitor C_{STG} is discharged; i.e., node (1) is at V_{SS} (GND). Prior to chip enable going high, the bit sense lines have been precharged to V' by device Q_1. [V' is a voltage between V_{DD} (+12V) and V_{SS}.] After the address decoders have stabilized, the proper column select line is brought high, turning on device Q_2. The storage capacitor is then electrically connected to the bit sense line. At this

time the charge on $C_{I/O}$ (proportional to the precharge voltage V') is redistributed between $C_{I/O}$ (parasitic capacitance of bit sense line) and C_{STG}. Since C_{STG} was initially discharged (node 1 at V_{SS}) the voltage will distribute between $C_{I/O}$ and C_{STG} according to the following relationship:

$$V_{BIT\ SENSE}\ (t_1) = V_{BIT\ SENSE}\ (t_0)\ \left(\frac{C_{I/O}}{C_{I/O} + C_{STG}}\right)$$

Since $C_{I/O}$ is very much larger than C_{STG} the change in the voltage on the bit sense line will be very small. The sense amplifier (S/A) is designed to detect very small changes in bit sense line voltage and to latch in a state near V_{SS} (GND) or V_{DD} (+12V), depending on the state of the storage cell.

Sensing an initial charge on C_{STG} (proportional to V_X where $V_X = V_{DD} - V_{TH}$, V_{TH} is the effective MOS threshold) is identical to the sequence described above. The only difference is that now the bit sense line is driven above the initial V' precharge voltage. Again the sense amplifier detects the small change in bit sense line voltage and latches in the appropriate state.

Note that during a read operation of the storage cell, the original charge (data) on the storage cell is changed (i.e., the read operation is effectively a destructive read). Data is rewritten back on the storage capacitor C_{STG} by the sense amplifier after it has latched in the proper state. For example, if C_{STG} was initially charged to V_X (~10V), the sense amplifier will latch the bit sense line to V_X and, since the column select line is on (high), the original data is automatically rewritten into C_{STG}. The entire operation is transparent to the user.

A plot of the voltage on the bit sense line for the two cases described above is shown in Figure 5.
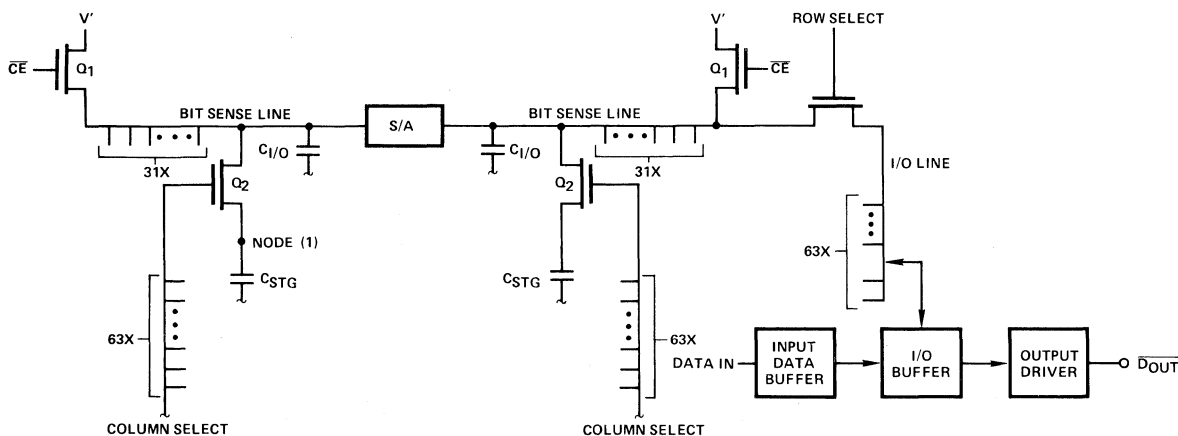

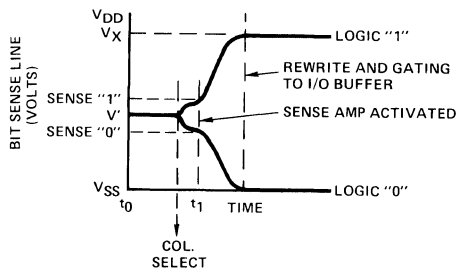**Figure 4. 2107B Memory Cell and Associated I/O Circuitry**

Figure 5. Bit Sense Line Voltage

A write operation is identical to the rewrite portion of a read cycle. In this case, however, the incoming data "overrides" the state of the sense amplifier (if different from the desired state) and writes into the selected cell. For reference, a low level on the data-in input results in a high level (V_X) being written into the selected storage cell. It is important to remember that the data-output at the output pin is the logical inverse of the data written into memory.

Data Sense/Latch

As discussed previously, a sense amplifier on the bit sense line is necessary to detect the low level data signals generated on the bit sense line during a read cycle. A simplified circuit schematic used for the sense amplifier is shown in Figure 6.
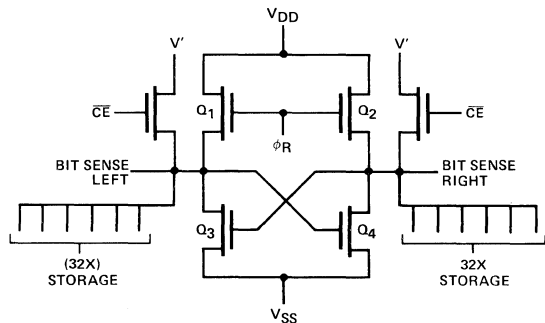

Figure 6. Data Sense/Latch

Before chip enable is brought high, both sides of the bit sense lines are precharged to V' (as discussed previously). At the proper time (after all data transients have subsided) devices Q_1 and Q_2 are turned on by ϕ_R going positive. At this time, the state of bit sense left is compared with bit sense right causing the latch to lock in the appropriate state. For example, if the right bit sense line is at a higher potential than the left bit sense line, device Q_3 will begin to conduct. The cross coupled latch will then fully switch with bit sense left going to V_{SS} and bit sense right to V_X.

Address Buffer/Latch

The address buffer/latch is shown in Figure 7. The input to the address buffer/latch is low voltage compatible which the circuit senses, translates to MOS level signals and latches.

Operation of the address buffers is as follows: During chip enable off time (CE low) both sides of the latch are precharged to V_X (~10V) by devices Q_1, Q_2, and Q_3. Device Q_3 is used to assure that the initial precharge on each side of the latch are equal.

When chip enable goes high, the input to the address buffer (A_{IN}) is gated to the cross coupled latch which latches the appropriate MOS level at A_I and $\overline{A_I}$. For example, if the TTL address input is high, then device Q_7 will turn on at ϕ_A time. The cross coupled latch then regenerates, turning Q_6 off. The quiescent state of the latch for this input is Q_6 off, Q_8 on, thereby setting A_I and $\overline{A_I}$ to MOS level high and low, respectively.

This type of latch is capable of triggering and latching at very high speeds which allows the addresses to be removed from the input as soon as possible. However, there are a few characteristics of this latch which have an effect when the device is placed in a system environment.

First note that node (1), Figure 7, has been precharged to a high MOS level of V_X (~10V). When
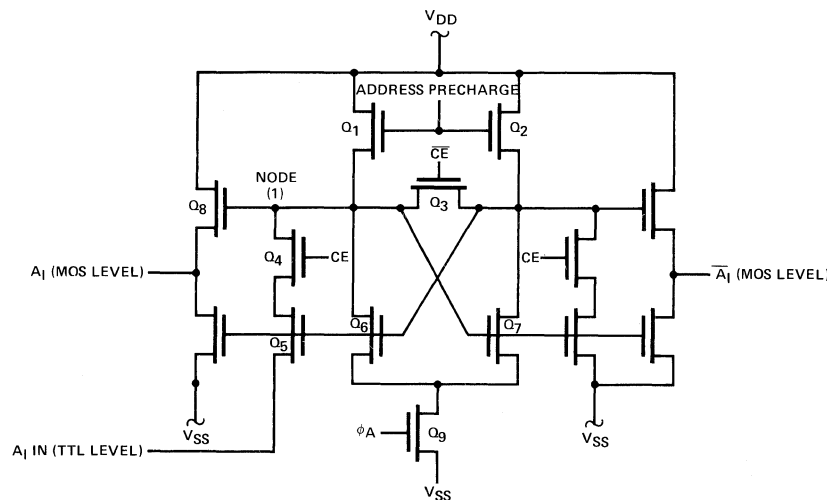

Figure 7. Address Buffer/Latch

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chip enable goes high turning on Q_4, the charge on this node is connected to the address input node (A_{IN}) for a short period of time (until the latch switches). This results in a small positive voltage shift on the address input A_{IN}. It follows then that the more 2107B devices attached to a given address driver the larger the voltage excursion will be. This excursion has been found to cause no problem in any reasonable system environment (as described later) and amounts to no more than 9 mV positive shift for each 2107B. The amount of positive charge coupling depends upon the address driver and the address line impedance. As should be expected, the most sensitive address level is the low level (V_{IL}) since any positive coupling decreases the available noise margin.

Another characteristic to be aware of in this type address buffer is the input current drawn through the address driver when an address goes from a low state to a high state during chip enable high. This condition results from the latch being set in the state where Q_6 is on as well as Q_4 and Q_5. Current is then drawn through devices Q_4, Q_5, Q_6 and Q_9. This current is typically in the order of 0.5 mA. Note that although this may cause a load on the address driver and cause it to drop below 2.4V, there is no effect on the memory component since the desired address has been latched in. This current is drawn only as long as chip enable is high. When chip enable goes low, device Q_4 is turned off, opening the current path. This effect will be shown on various type drivers in a later section (Low Voltage Buffer/Drivers).

Output Driver

A schematic of the output buffer is shown in Figure 8. Note that the output is in a high impedance state if either chip select is high or chip enable is low. Further, the V_{CC} shown in Figure 8 is the only connection the V_{CC} makes on the 2107B. This allows V_{CC} to have a wide range of values (up to V_{DD}) if types of sensing other than TTL is desired.

2107B Bit Map

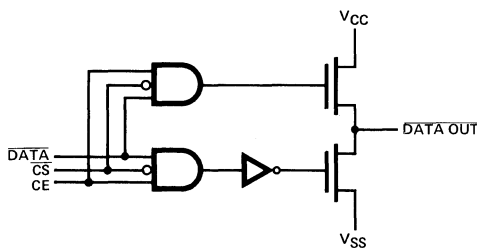Figure 9 gives the location of each cell in the memory matrix for each address. As shown in this
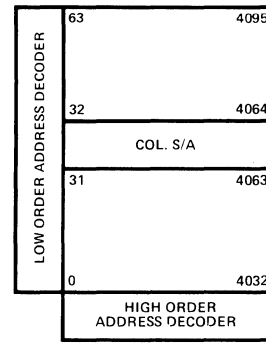
Figure 9. 2107B Bit Map

figure, the addresses run sequentially starting from the lower left corner (device oriented as shown).

2107B SPECIFICATION

Although the device specifications for the 2107B are concise and self explanatory, some sections are included here to emphasize those areas of most interest to the designer. Consider first the DC and operating characteristics shown in Table I marked with a [5].

The V_{DD} supply current during chip enable off is specified at 200 μa maximum with chip enable no higher than 0.6V. It is important to hold the low level of chip enable at or below this value (to a maximum of −1.0V) to assure that devices internal to the 2107B do not turn partially on. Note that considering only the AC operating environment, chip enable can go as high as 1.0V above V_{SS} and the device will still operate properly. This requirement on chip enable off is most important in those systems being placed in a low power refresh only standby mode.

The V_{BB} supply current load (I_{BB}) is maximum at 100 μa and includes all leakages. It is not necessary to add the other leakage currents (e.g., I_{LI}, I_{LC}) to I_{BB} to calculate supply drain on V_{BB}.

The input low voltage (for low level signals) V_{IL}, is specified as a function of the chip enable rise time and is referenced to a transition with $t_T = 20$ nsec. It is recognized that in some system applications, the load on the chip enable driver may result in transitions of 30 nsec or higher (to a maximum of 40 nsec). If the chip enable transition in the system is not 20 nsec or faster (to a minimum of 10 nsec), then the typical low level for the low level drivers is shown by the graph in Figure 10. It is important to include any noise which may be on the address line during t_{AH} (address hold) time. An example of the noise expected on an address line when chip enable goes high (during refresh) is shown in Figure 11. The noise shown here is the result of 36 devices attempting to raise the address driver (see Address Buffer/Latch) level during refresh time. Refresh

Figure 8. 2107B Output Driver

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Table I. D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB}[1] = –5V ±5%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	MIN.	TYP.[2]	MAX.	UNIT	CONDITIONS	
I_{LI}	Input Load Current (All Inputs Except CE)		.01	10	μA	V_{IN} = $V_{IL\,MIN}$ to $V_{IH\,MAX}$	
I_{LC}	Input Load Current		.01	10	μA	V_{IN} = $V_{IL\,MIN}$ to $V_{IH\,MAX}$	
|I_{LO}|	Output Leakage Current for High Impedance State		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V	
I_{DD1}[5]	V_{DD} Supply Current During CE Off[3]		110	200	μA	CE = –1V to + 0.6V	
I_{DD2}	V_{DD} Supply Current During CE On		80	100	mA	CE = V_{IHC}, T_A = 25°C	
$I_{DD\,AV1}$[5]	Average V_{DD} Current		55	80	mA	Cycle Time = 400 ns, t_{CE} = 230 ns	T_A = 25°C
$I_{DD\,AV2}$	Average V_{DD} Current		27	40	mA	Cycle Time = 1000 ns, t_{CE} = 230 ns	
I_{CC1}[4]	V_{CC} Supply Current During CE Off		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}	
I_{BB}[5]	V_{BB} Supply Current		5	100	μA		
V_{IL}[5]	Input Low Voltage	–1.0		0.6	V	t_T = 20 ns — See Figure 4	
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V		
V_{ILC}	CE Input Low Voltage	–1.0		+1.0	V		
V_{IHC}[5]	CE Input High Voltage	V_{DD}–1		V_{DD}+1	V		
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0 mA	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = –2.0 mA	

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

2. Typical values are for T_A = 25°C and nominal power supply voltages.

3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

5. See basic discussion — 2107B specifications.
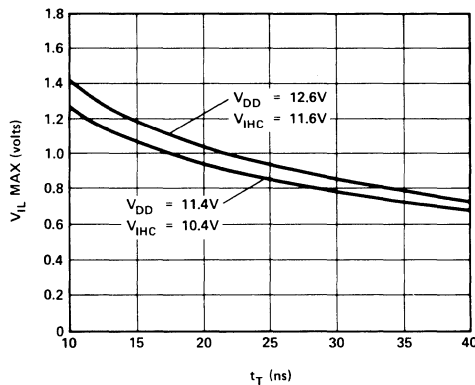
Figure 10. V_{IL} vs CE Rise Time
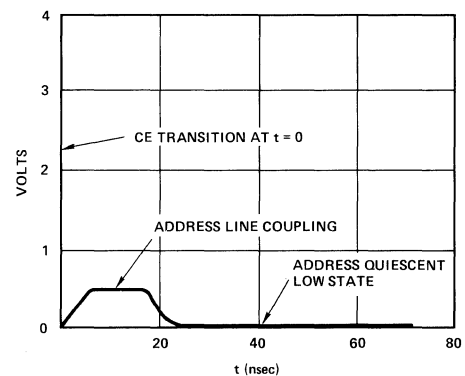
36 2107B DEVICES ON ADDRESS DRIVER
REFRESH CYCLE

Figure 11. Coupling to Address Line Caused by Chip Enable Transition

is the worst case since all chip enable signals will be simultaneously decoded and driven at the same time.

The chip enable high voltage, V_{IHC}, can vary between $V_{DD}+1.0$ and $V_{DD}-1.0$ volts. This allows maximum flexibility in the driver design and provides for adequate noise margins.

The average V_{DD} current $I_{DD\,AV1}$ during a read/write cycle is specified at $25°C$ to be a maximum of 80 ma. This current is a function of both cycle time and temperature as shown in Figures 12 and 13, respectively. As shown by these curves, the maximum power occurs at low temperature and maximum duty cycle.
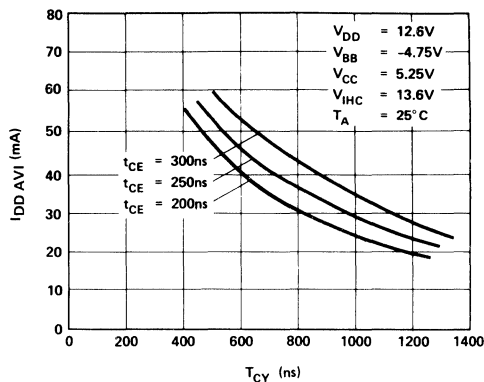

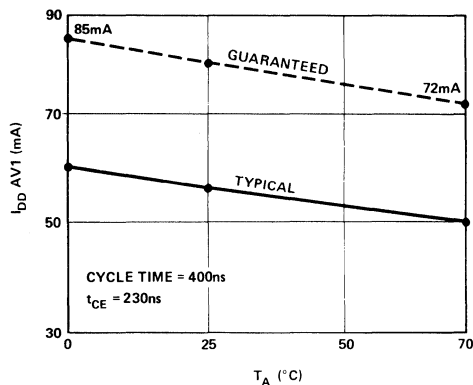**Figure 12. $I_{DD\,AV1}$ vs Cycle Time**

Figure 13. $I_{DD\,AV1}$ vs Temperature

Timing

The timing relationship between the control, addresses, and data in/out is very straightforward as shown in the specification. For reference, the Read/Refresh, Write and Read-Modify-Write cycles are shown in Figures 14, 15, and 16, respectively, for minimum timing. Selected points are discussed which may cause the most problems if they are violated in a system environment.

For all cycles it is imperative to make certain that the address inputs are valid at or before chip enable reaches the $V_{SS}+2.0V$ level (t_{AC}). The high speed of the 2107B address buffer/latches means that if the address inputs are not valid until just after chip enable goes high, the wrong address is likely to be latched in the chip. Likewise, the input data must not change after write enable goes low while chip enable is high (t_{DW}). Again, violation of this requirement may result in incorrect data being written into memory.

Note that for all cycles, the data-out output goes to a low state shortly after chip enable goes high. This prohibits the output from being tied directly to a clear or preset input of a latch.

Problems can occur when one or more parts of these specifications are violated.

Transient Currents

Although the transient currents in the 2107B are easily handled, proper attention should be paid to the peak values and adequate decoupling provided to handle the expected transients. Figure 17 shows the transient currents present in the 2107B.

Consider first the transient current supplied by the chip enable driver I_{CE}. It is noted that this current does not have a resistive component but is strictly a charging current represented by the relationship:

$$I = C\left(\frac{dv}{dt}\right)$$

As expected, the largest transient current drawn by the 2107B is the V_{DD} supply and is represented by I_{DD}. The first portion of this curve (peak ~120 ma) shown as A is the result of internal nodes charging up for operation. The section shown as B is the result of the address buffers/decoders turning off. Portion C is the "steady state" current drawn by all internal circuits while chip enable is high. Note the slight difference between a read and write cycle which results from different portions of the internal circuitry turning on.

Portion D of the transient current is the result of feedthrough capacitance (internal to the chip) coupling to V_{DD} when chip enable goes low. Portion E is the precharging of selected internal nodes by the chip enable generator (e.g., precharging bit sense line. See section on Internal Device Operation).

The transients associated with the V_{BB} supply I_{BB} should be reviewed closely. Note that the peak values are approximately 20 ma during a cycle with a time base as shown. Special attention is called to this because even though the *average* DC current is very small (maximum 100 μa) the peak currents can be two orders of magnitude higher.
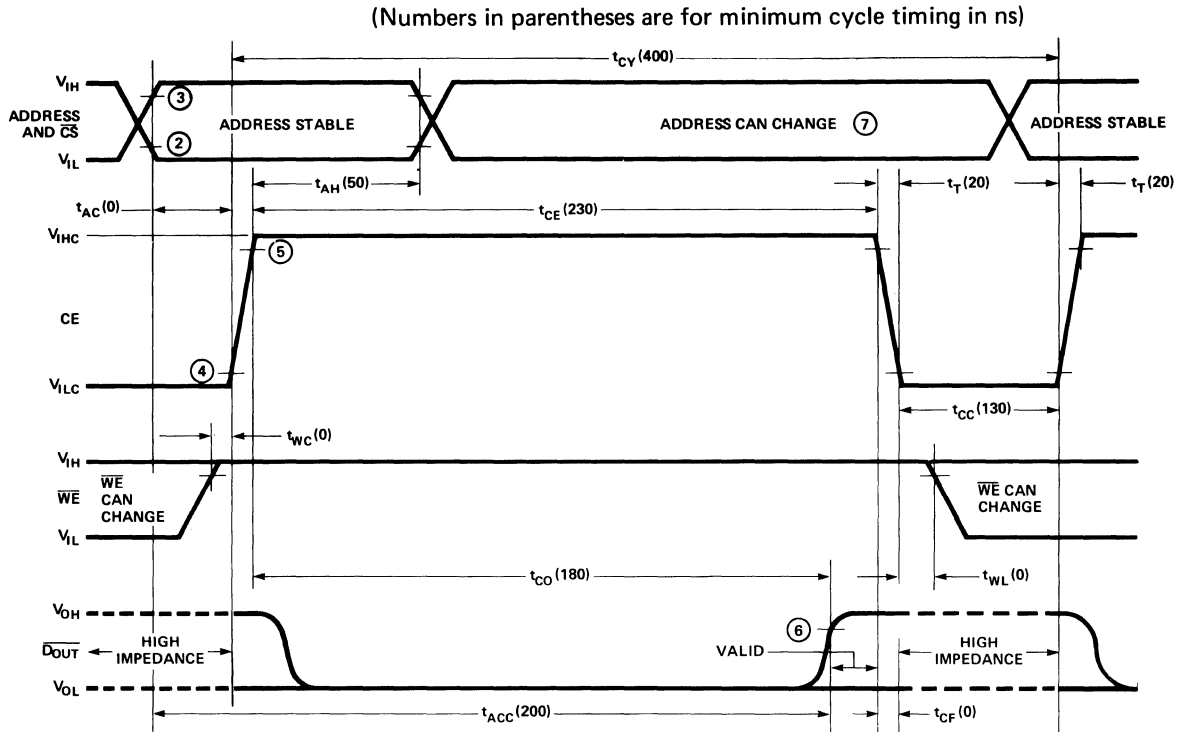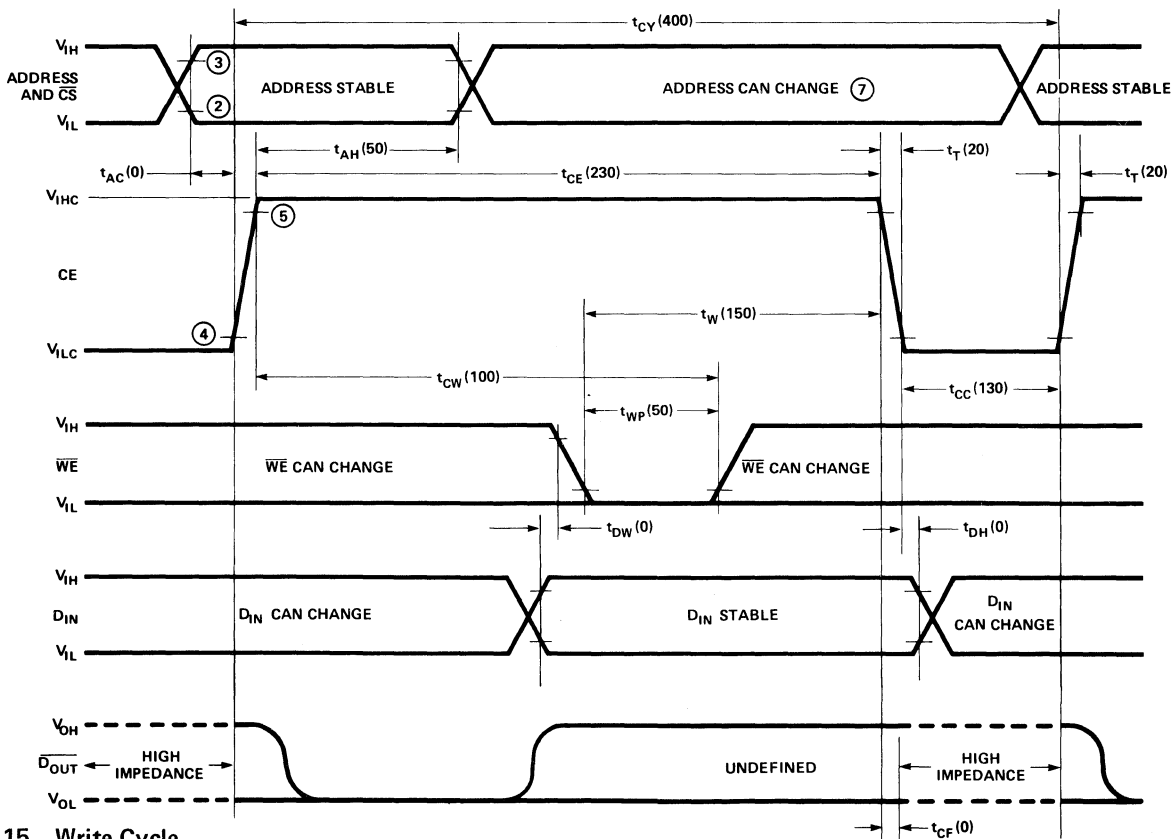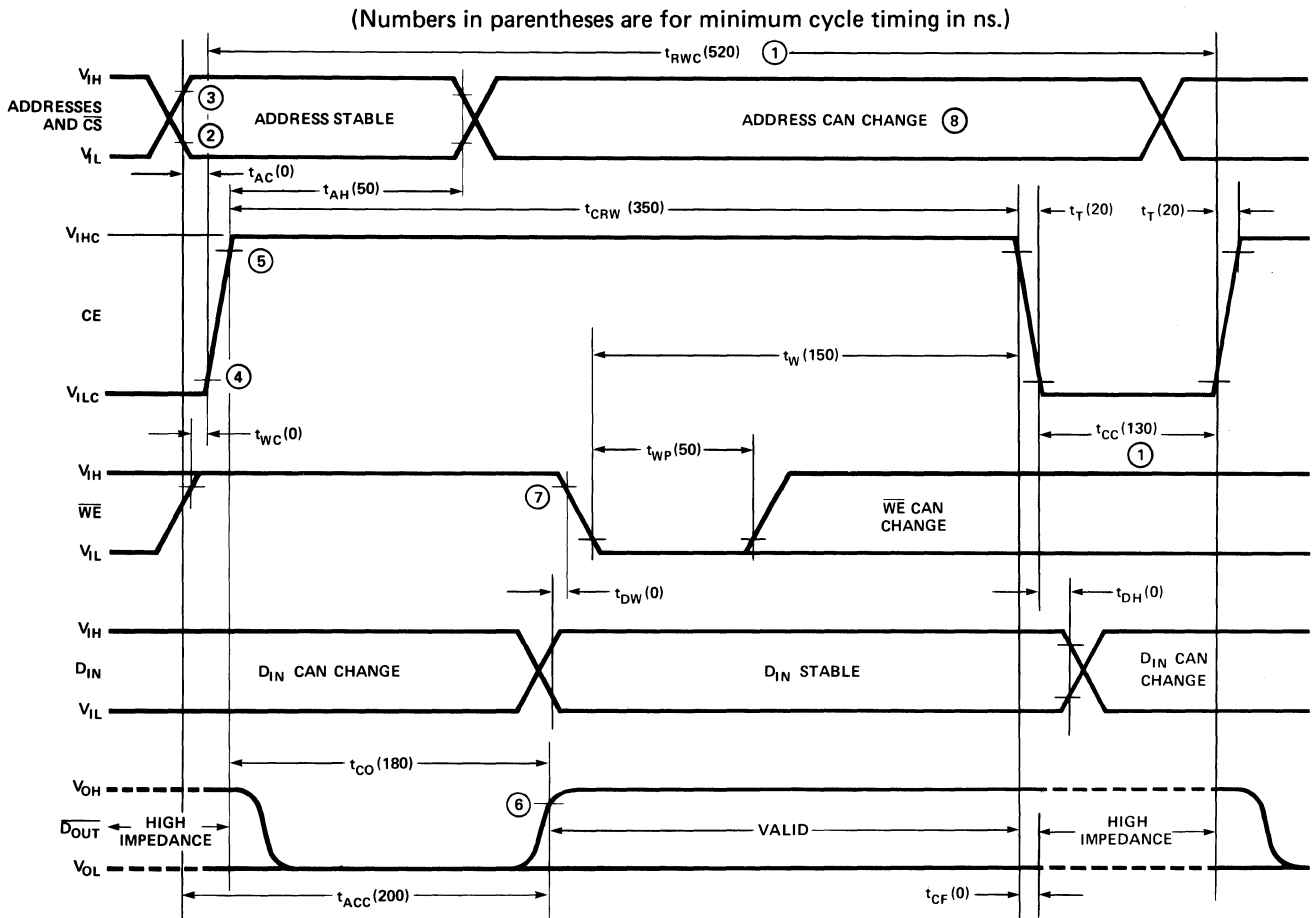
Figure 14. Read/Refresh Cycle[1]

Figure 14 labels: t_{CY} (400), ADDRESS AND $\overline{CS}$, V_{IH}, V_{IL}, ADDRESS STABLE, ADDRESS CAN CHANGE (7), ADDRESS STABLE, t_{AC} (0), t_{AH} (50), t_{CE} (230), t_T (20), t_T (20), V_{IHC}, CE, V_{ILC}, t_{CC} (130), t_{WC} (0), V_{IH}, $\overline{WE}$, $\overline{WE}$ CAN CHANGE, V_{IL}, $\overline{WE}$ CAN CHANGE, t_{CO} (180), t_{WL} (0), V_{OH}, $\overline{D_{OUT}}$, HIGH IMPEDANCE, VALID (6), HIGH IMPEDANCE, V_{OL}, t_{ACC} (200), t_{CF} (0)

Figure 15. Write Cycle

Figure 15 labels: t_{CY} (400), ADDRESS AND $\overline{CS}$, V_{IH}, V_{IL}, ADDRESS STABLE, ADDRESS CAN CHANGE (7), ADDRESS STABLE, t_{AC} (0), t_{AH} (50), t_{CE} (230), t_T (20), t_T (20), V_{IHC}, CE, V_{ILC}, t_W (150), t_{CW} (100), t_{CC} (130), t_{WP} (50), V_{IH}, $\overline{WE}$, $\overline{WE}$ CAN CHANGE, $\overline{WE}$ CAN CHANGE, V_{IL}, t_{DW} (0), t_{DH} (0), V_{IH}, D_{IN}, D_{IN} CAN CHANGE, D_{IN} STABLE, D_{IN} CAN CHANGE, V_{IL}, V_{OH}, $\overline{D_{OUT}}$, HIGH IMPEDANCE, UNDEFINED, HIGH IMPEDANCE, V_{OL}, t_{CF} (0)

NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} −2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

(Numbers in parentheses are for minimum cycle timing in ns.)

NOTES:
1. A.C. characteristics are guaranteed only if cumulative CE on time during t_{REF} is ≤60% of t_{REF}. For continuous Read-Modify-Write operation t_{CC} and t_{RWC} should be increased to at least 195ns and 585 ns, respectively.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} –2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Figure 16. Read-Modify-Write Cycle
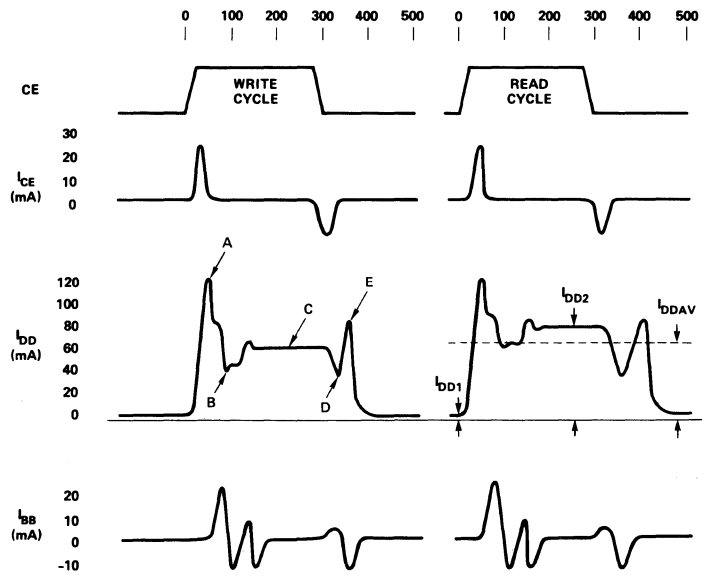
Figure 17. Typical Current Transients vs Time

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These transients are characteristic of any dynamic RAM and are in part related to the density of the RAM. Again, if adequate decoupling measures are taken, very little noise will be generated on the V_{BB} system distribution.

Notice that the transient current for I_{CC1} is not shown. This is because the V_{CC} supply is connected only to the internal output device and its transient depends on the load placed on the output.

A full discussion on decoupling the power distribution in 2107B arrays appears in the decoupling section. As it is shown later, the use of a multi-layer memory board is not required by the 2107B.

SYSTEM CONSIDERATIONS

The previous sections of this application note have dealt with the characteristics of the 2107B as a stand-alone device. This section will outline the types of interface, system design considerations, power calculations and testing considerations when using the 2107B.

MOS Level Drivers

There are many types of drivers capable of driving n-channel RAMs such as the 2107B. The drivers can be used in one or more of the configurations as shown in Figure 18a, b, and c. Each of the driver types shown in Figure 18 has an optimum circuit load that it can drive and each has special design considerations. These drivers are catagorized in three general types; those which:

1. Require external drive transistors.

2. Require an additional power supply.

3. Require no special components or voltages.

In case (1) above, there is insufficient high level drive capability in the driver, hence a PNP external discrete transistor must be used to generate sufficient up-going transition (Figure 18a). Note that this transistor is driving in the saturated mode so the minimum high level criteria $(V_{DD}-1.0)$ on the high level MOS clock are easily met.

Driver type (2), shown in Figure 18b, does not require external discrete transistors but does require an additional power supply. This extra supply is usually 3V higher than the V_{DD} supply for the RAM (e.g., using this type of driver with the 2107B would require $V_{DD} = 12V$ and $V_{DD1} = 15V$). The additional supply is necessary to assure that the minimum up level $(V_{DD}-1.0)$ requirement of the MOS clock is met.

The high going drive capability of the driver type shown in Figure 18c may be insufficient to meet the V_{IH} MIN requirements of the 2107B.

The types of MOS level drivers recommended to drive the 2107B (or any other n-channel MOS RAM) are those shown in Figure 18a and b.
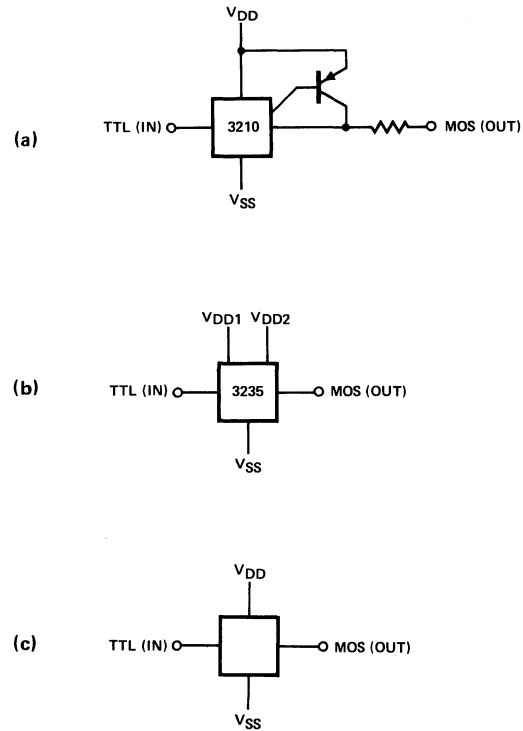

Figure 18. Three Types of MOS Level Drivers

It is important to remember to place the MOS level driver outputs physically as close as possible to the memory array. This will minimize any transmission line impedance mismatch between the unloaded stub and heavily loaded line in the memory array. The effect can most easily be seen with the aid of Figure 19. The impedance of the interconnect is:

1. $$Z_{0(1)} = \sqrt{\frac{L}{C_1}}$$

where C_1 is the capacitance per unit length of the interconnect

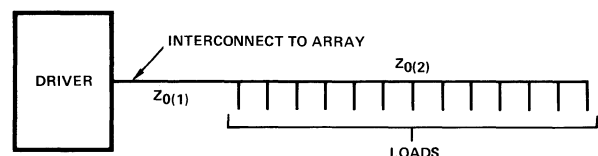L is the inductance per unit length of the interconnect

Figure 19. MOS Level Driver Loading

For all practical purposes, the inductance per unit length of the printed line is independent of the externally connected loads. Therefore, the impedance of the loaded section of transmission line can be represented as:

$$2. \quad Z_{0(2)} = \sqrt{\frac{L}{C_1 + C_2}}$$

where C_2 is the added capacitance per unit length to the printed transmission line.

For most practical systems, capacitance per unit length of an unloaded transmission line will be approximately $1-2$ pF/in. (C_1). C_2 is the capacitance effect of the 2107B per unit length. Since the spacing between memory devices is approximately $0.5''$ the typical loading effect of C_2 is 30 pF/in. (i.e., 15 pF assumed for each chip enable input).

The ratio of the two impedances is calculated as follows:

$$\frac{Z_{0(1)}}{Z_{0(2)}} = \sqrt{\frac{C_1 + C_2}{C_1}} = \sqrt{\frac{32}{2}} = 4$$

This means that the impedance of the stub is four times the impedance of the loaded section.

If the loads are placed close to the driver output the effect of the stub will be negligible and will cause no problem.

3235 MOS Level Driver

The Intel® 3235 is a quad MOS level driver, with each driver capable of driving 250 pF load with maximum delay of 32 nsec. The 3235 requires three power supplies V_{CC} (+5V), V_{DD1} (+12V), and V_{DD2} (+15V). The pin configuration and logic diagram of the 3235 is shown in Figure 20. For reference, input/output waveforms are shown in Figure 21, with delays given in Table II for worst case conditions.

Note that Table II gives the minimum input to output delay for a lightly loaded line (C = 150 pF) and

the maximum delay plus rise time for a heavier load (C = 250 pF). The minimum delay time is given so the system designer can guarantee that the chip enable driven by a particular driver does not occur *before* the address lines have stabilized. The maximum delay plus rise time is given to guarantee
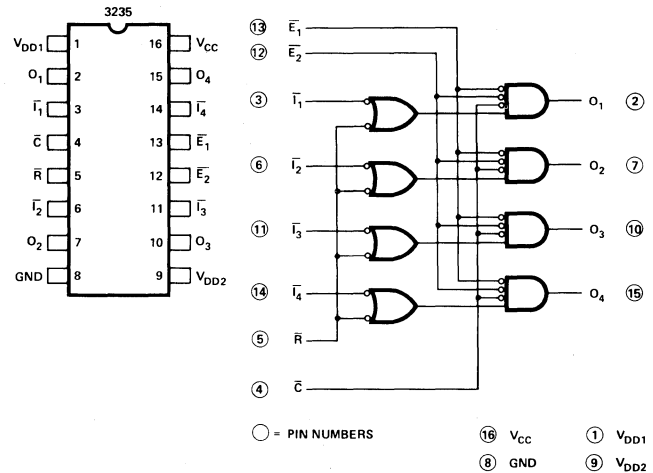
Figure 20. 3235 Pin Configuration and Logic Diagram
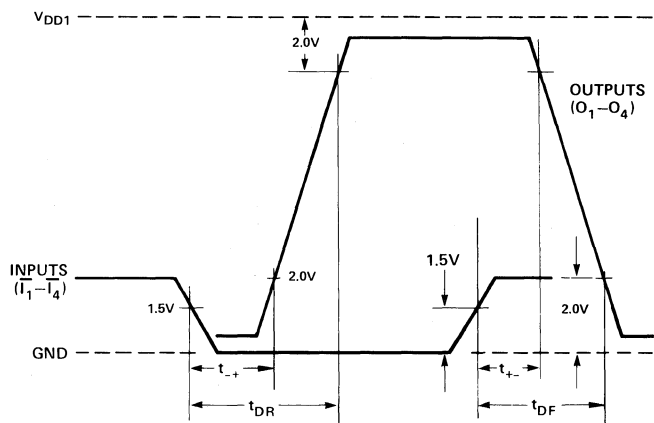
Figure 21. 3235 Input/Output Waveforms

Table II. 3235 A.C. Characteristics

$T_A = 0°C$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD1} = 12V \pm 5\%$, $V_{DD2} = V_{DD1} + (3V \pm 5\%)$

| SYMBOL	PARAMETER	MIN.[1]	TYP.[2]	MAX.[3]	UNIT
t_{-+}	Input to Output Delay	5	11		ns
t_{DR}	Delay Plus Rise Time		20	32	ns
t_{+-}	Input to Output Delay	3	8		ns
t_{DF}	Delay Plus Fall Time		19	32	ns

NOTES: 1. $C_L = 150$ pF 2. $C_L = 200$ pF & $T_A = 25°C$ 3. $C_L = 250$ pF

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a required system access or cycle time can be met. The capacitance values specified for the 3235 of C = 150 pF, C = 200 pF, and C = 250 pF are representative of the minimum, typical, and maximum capacitance, respectively, of nine 2107B Chip Enable inputs plus associated stray capacitance.

Graphs showing the effect of capacitance loads on delay and rise times are shown in Figure 22a and b.
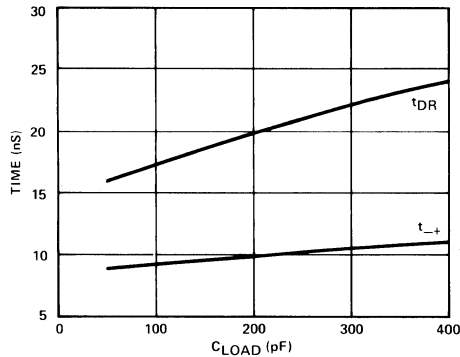
(a) DELAY AND DELAY + RISE
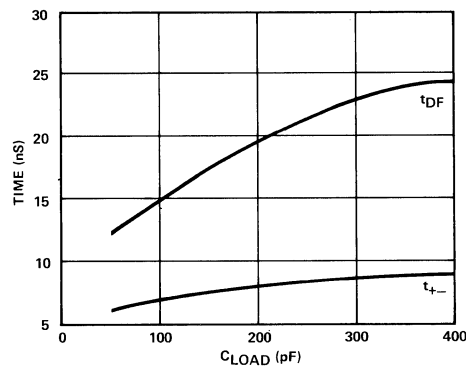
(b) DELAY AND DELAY + FALL

Figure 22. 3235 Delay and Transition Time as a Function of C_{LOAD}

The 3235 offers a great deal of flexibility in driving large arrays of 2107Bs. A sample of its logic capability is shown in Figure 23. A given card is selected by Card Enable i, byte control is maintained with Byte Enable, and the desired row selected by Row Enable i. The basic chip enable timing pulse is provided by CE timing.

At refresh time it is necessary to activate the $\overline{\text{Card Enable i}}$, Byte Enable and Refresh Enable to refresh the entire card at one time. In most systems, it is desirable to refresh all cards simultaneously. If the cards are decoupled properly (see Decoupling section), the power supply transients during refresh will be minimal and are acceptable. The basic configuration of such a card is shown in Figure 24. For
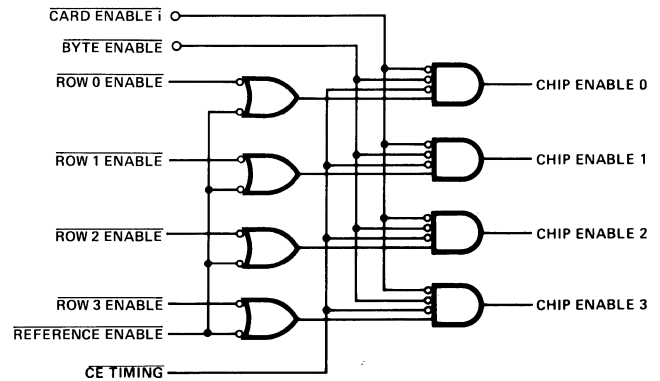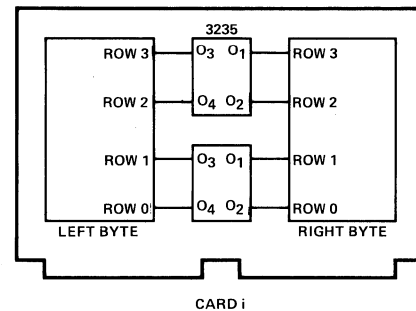

Figure 23. 3235 Enable Configuration

Figure 24. System Organization and Driver Placement

this system, the entire 16K X 16 memory array can be driven with two 3235s placed as shown between the two memory arrays.

Waveforms of the 3235 driver in a system similar to that shown in Figure 24 are given in Figure 25a–d. The driver configuration used is shown in Figure 26. Figure 25a and b shows the leading and trailing edge of chip enable at both the beginning and ending of the printed line for an added series resistance R of 10Ω. Note the transition time and overshoot for each of these edges. The overshoot is worst case at the leading edge at the driver end and on the trailing edge at the end of the line. The trailing edge overshoot is 2.2V while the leading edge overshoot is 1.5V. Both values are very marginal for system operation.

The effect of increasing the series resistance to 20Ω for the above driver is shown in Figure 24c and d. Note that the transition time has increased but is
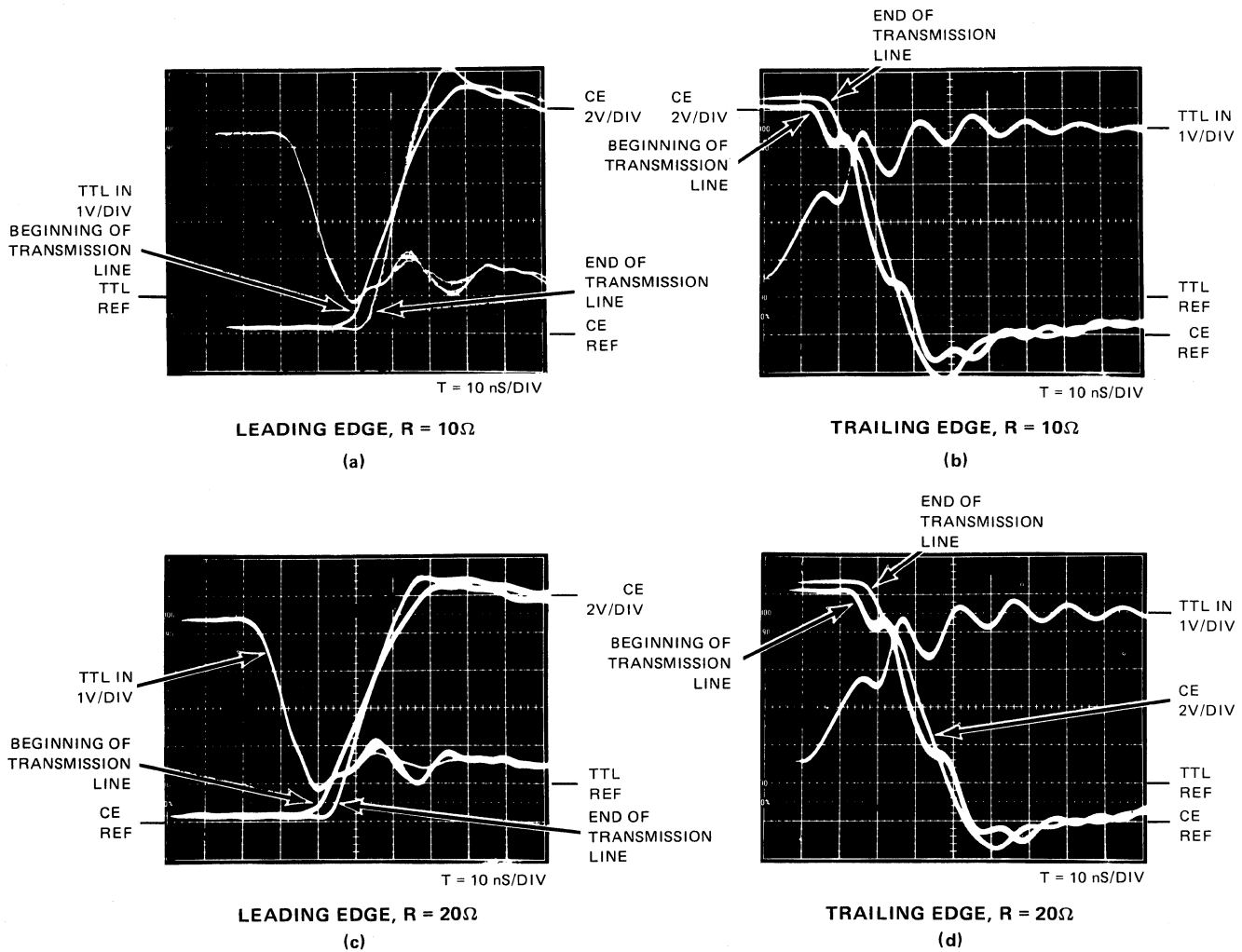
LEADING EDGE, R = 10Ω

(a)

TRAILING EDGE, R = 10Ω

(b)

LEADING EDGE, R = 20Ω

(c)

TRAILING EDGE, R = 20Ω

(d)

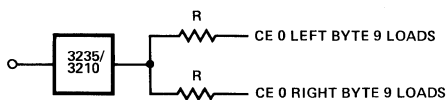**Figure 25. 3235 Typical Driver Waveforms**

Figure 26. MOS Level Driver Configuration

still within entirely acceptable limits and the overshoots have been cut in half. The driver is now operating in an acceptable mode with minimal overshoot.

The effect of temperatures on the 3235 is shown in Figure 27. A 20Ω series resistor is used with the driver.

The results of board measurements of a typical 3235 driver driving 18 loads and 9 loads is shown in Table III. Note that the delay does not change appreciably with temperature but the transition time increased approximately 2–3 nsec from 25°C to 70°C.
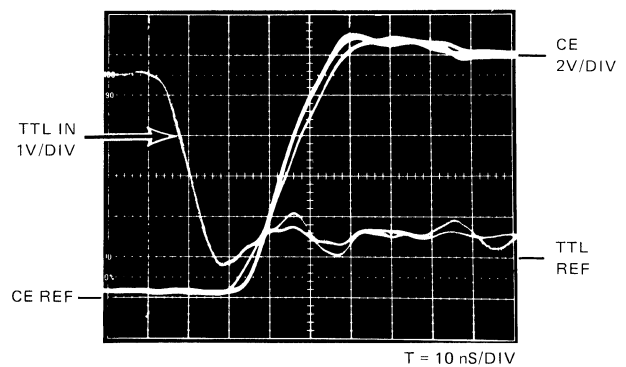

Figure 27. 3235 Driver Waveform with Temperature = 70°C

3210 MOS Level Driver

The pin configuration and logic symbol for the 3210 driver is shown in Figure 28. As shown in this figure, this driver consists of one MOS level driver and four TTL low voltage buffers. These low voltage buffers can be used to drive inputs which require a 3.5V high level (such as the 2107A address

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Table III. Summary of 3235 Driver Board Delay Measurements

NUMBER 2107B LOADS AND CIRCUIT CONFIGURATION	MEASURED CONDITIONS INPUT TO OUTPUT DELAY				MEASURED DELAY[3] PLUS RISE		MEASURED DELAY[4] PLUS FALL	
	t_{-+} [1]		t_{+-} [2]					
	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE
3235 18 LOADS[6] R = 20Ω	12	12	10	10	34	37	33	35
3235 9 LOADS R = 20Ω	11		10		30	33[7]	25	27[7]

NOTES:

1. TTL 1.5 to V_{SS} +1 volt
2. TTL 1.5 to V_{DD} −1 volt
3. TTL 1.5 to V_{DD} −1 volt
4. TTL 1.5 to V_{SS} +1 volt

5. Worst case driver on board at 70°C and 5% power supply variation.
6. 18 loads 20Ω split resistor (see Figure 26).
7. Projected from 18 load delay.
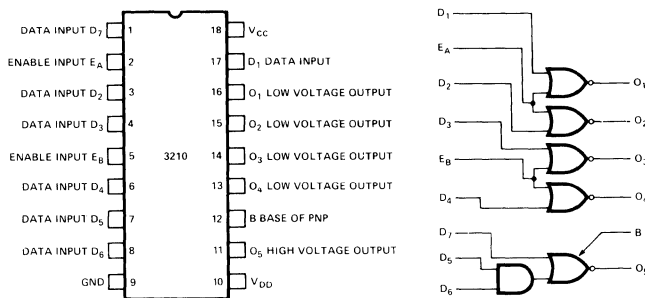
Figure 28. 3210 Pin Configuration and Logic Symbol

inputs) or they can be used to drive high capacitance loads with minimum delay. For reference, the input/output characteristics of the 3210 are shown in Figure 29 and table IV, respectively.

The driver configuration for the 3210 MOS level output is shown with the aid of photos in Figure 30a and b for series resistances of 10Ω and 20Ω. Table V summarizes the results of board measurements for the 3210 as a function of series resistance and temperature.

Low Voltage Driver/Buffers

The address, data-in, write enable, and chip select inputs on the 2107B are all low voltage TTL compatible requiring no special interface. This section will discuss the types of drivers which can be used to drive the low voltage inputs along with the advantages and disadvantages of the drivers.

The types of low level drivers capable of driving the 2107B are shown in Figure 31. Two observations are pointed out regarding the use of TTL drivers shown in Figure 31.

1. There are no pull up resistors.

2. Series 74S type gates are not recommended.

Table IV. 3210 A.C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%

SYMBOL	PARAMETER	MIN.	TYP.[1]	MAX.	UNITS	TEST CONDITIONS
t_{LDR}	Delay Plus Rise Time for Low Voltage Drivers		17	25	nS	C_L = 200 pF
t_{LDP}	Delay Plus Fall Time for Low Voltage Drivers		16	25	nS	C_L = 200 pF
t_{H-+}	Input to Output Delay for High Voltage Driver	9	15		nS	C_L = 175 pF
t_{HDR}	Delay Plus Rise Time for High Voltage Driver		27	40	nS	C_L = 350 pF
t_{H+-}	Input to Output Delay for High Voltage Driver	4	8		nS	C_L = 175 pF
t_{HDF}	Delay Plus Fall Time for High Voltage Driver		18	30	nS	C_L = 350 pF
t_{DB}	Delay to Base Drive to External PNP (Pin 12)	4	8	17	nS	

NOTE: 1. T_A = 25°C

A.C. CONDITIONS OF TEST:

Input Pulse Amplitudes: 3.0V Input Pulse Rise and Fall Times: 5 nS between 1 volt and 2 volts Measurement Points: See Waveforms
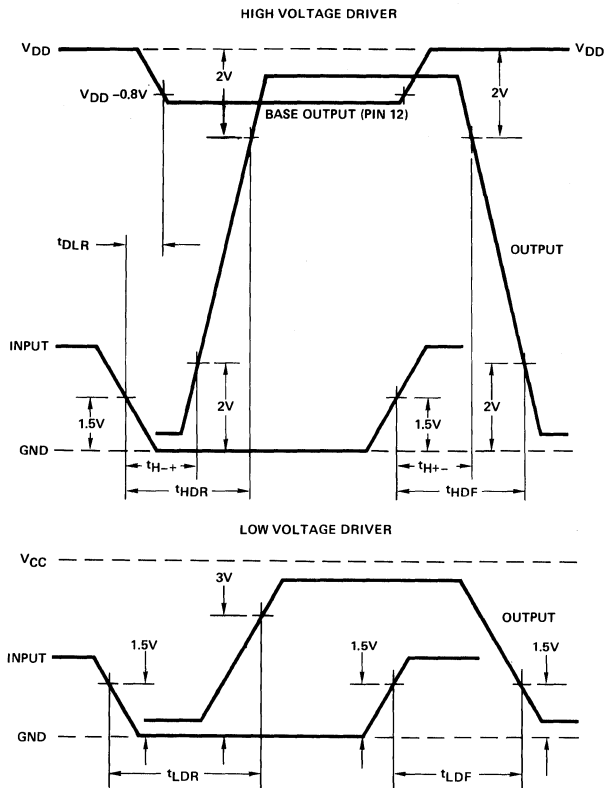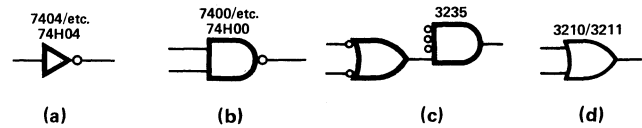
Figure 29. 3210 Input/Output Characteristics

Figure 31. Low Level Drivers

TTL Drivers

Since TTL devices will typically pull up actively to 2.8V to 3.4V, which is well above the required minimum high level, pull up resistors are not needed. Standard Series 7400 type gates are specified to supply 400 μa up level current at 2.4V worst case. Since each address input of the 2107B has a maximum leakage current of 10 μa, this type of driver is capable of driving 40 2107B address lines. However, it should be noted that these 40 address inputs have a capacitance of 240 pF. This load will increase the delay through the series 74 gates.

When driving the 2107B address inputs with TTL gates it is advisable to use a NAND type circuit
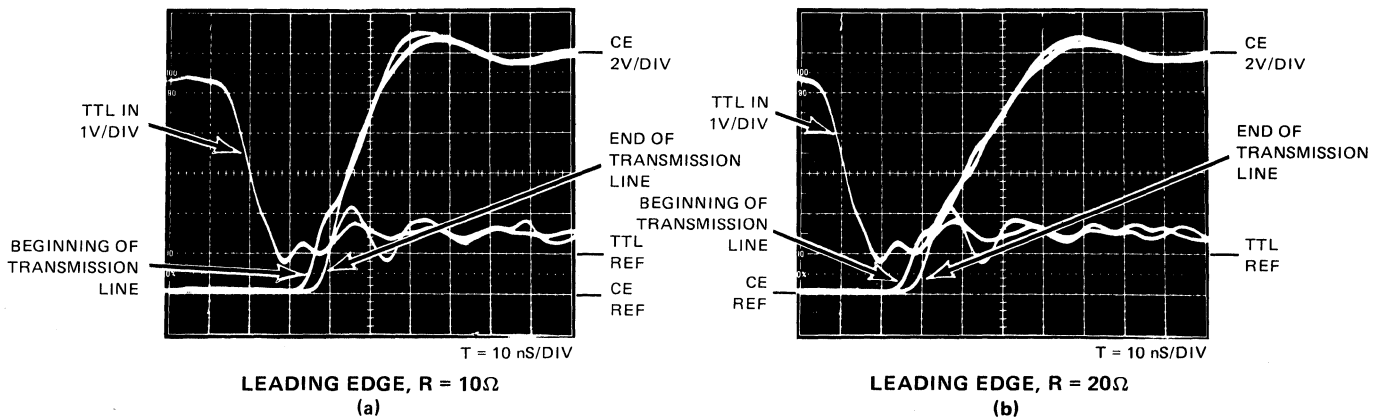

Figure 30. 3210 Typical Waveforms

Table V. Summary of 3210 Driver Board Delay Measurements

| NUMBER 2107B LOADS AND CIRCUIT CONFIGURATION	MEASURED CONDITIONS INPUT TO OUTPUT DELAY				MEASURED DELAY[3] PLUS RISE		MEASURED DELAY[4] PLUS FALL	
	t_{-+}[1]		t_{+-}[2]					
	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE
3210 18 LOADS[6] R = 20Ω	16	16	10	10	48	50	35	35
3210 9 LOADS R = 20Ω	14		8		30	32[7]	25	25[7]

NOTES:

1. TTL 1.5 to V_{SS} +1 volt
2. TTL 1.5 to V_{DD} −1 volt
3. TTL 1.5 to V_{DD} −1 volt
4. TTL 1.5 to V_{SS} +1 volt

5. Worst case driver on board at 70°C and 5% power supply variation.
6. 18 loads 20Ω split resistor (see Figure 26).
7. Projected from 18 load delay.

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(such as shown in Figure 31) with an enable input. This will allow all addresses to be set up in a high state (above 2.4V) and be driven low when appropriate. Since TTL gates have much better drive capability in the high to low direction, the increase in delay due to the large capacitance is reduced.

It is not recommended that Schottky type TTL gates be used to drive the low level inputs of the 2107B. This is because under worst case conditions, the down level of the Schottky device is approximately 100 mv higher than for a regular or H series TTL gate. This higher level coupled with the address noise coupled from the 2107B (see Address Buffer/Latch section) might make some systems marginal in operation. In addition, the effect of chip enable transition on address low voltage re-duces the maximum positive down level on the addresses. (See Device Specification section.)

An example of TTL circuits (7400, 74H00, 74S00) driving 36 address inputs on the 2107B at refresh time is shown in Figure 32. Figure 33 shows the same TTL gate at "Read" time. Note the high level loading effect is greatly reduced because only 9 loads (2107B) are turned on at one time. Note that a Series 74S gate was used and is shown for reference only. From these photos the amount of over-shoot present in driving high-low is clearly seen. Therefore, even with TTL drivers it is desirable to use series resistors to decrease the negative over-shoot. This resistor value depends on the load on the driver and 20Ω is recommended when driving 36 address loads.
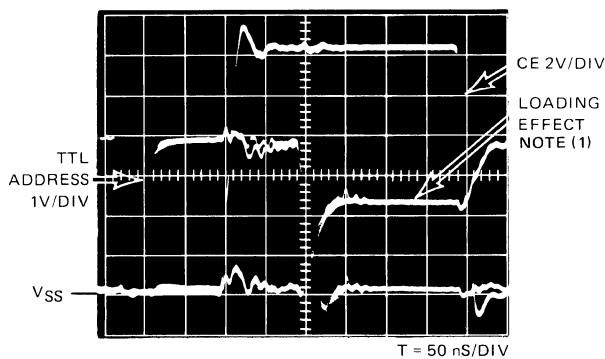
DRIVER TYPE 7400
(a)
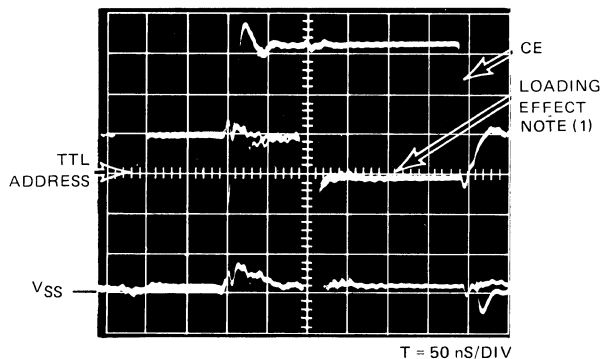
DRIVER TYPE 74H00
(b)
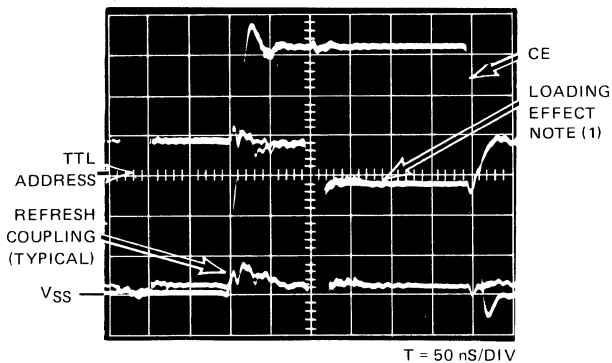
DRIVER TYPE 74S00
(c)

Figure 32. TTL Driver Waveforms (Refresh Cycle)

DRIVER TYPE 7400, R = 20Ω
(a)

DRIVER TYPE 74H00, R = 20Ω
(b)

DRIVER TYPE 74S00, R = 20Ω
(c)

Figure 33. TTL Driver Waveforms (Read Cycle)

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In the discussion of the address latch circuitry (Address Buffer/Latch section) reference was made to input currents drawn by the address buffer when an address is switched from a low to high level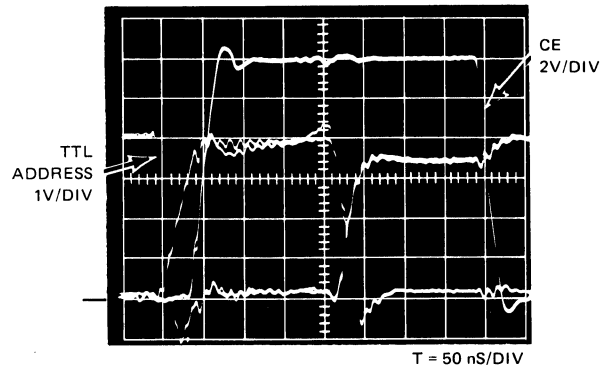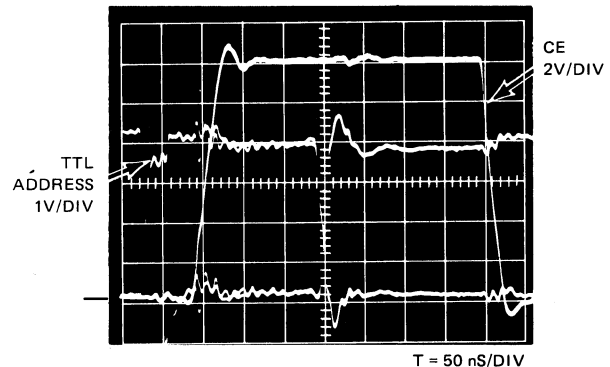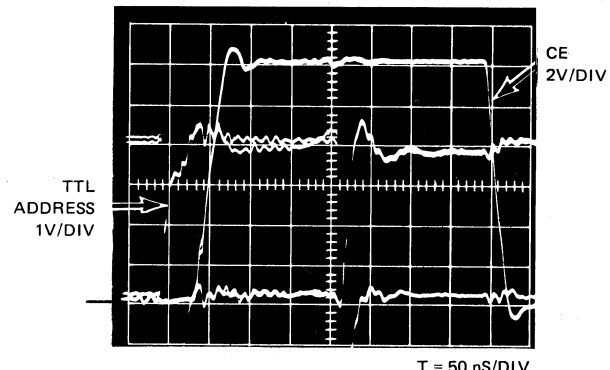 during chip enable. The decrease in high level shown in Figure 32 is due to the 0.5 mA/2107B loading of the address line following the low to high transition while chip enable is on. (All photos from Figure 32 are taken at refresh time when all devices are on. This condition is worst case.)

Figure 32 also shows the effect of 36 memory devices coupling charge back to the address line [see Note (1) on photos]. This coupling limits the series resistance value which can be added to the address drivers to minimize overshoot. It also suggests that the address drivers be placed as close as practical to the memory array.

The photo shown in Figure 34 is the current associated with the low to high level address transition for 36 devices at refresh time. (Note the time delay of current relative to address voltage change. This is the result of delays associated with the current probe relative to the voltage probe.) For this example, the driver used is a 3210.

Other Low Voltage Driver/Buffers

When speed and high level drive capability is needed it is desirable to use drivers which are designed specifically for driving high capacitance loads with minimum delay. The 3235 and 3210 can be used to drive the 2107B low voltage inputs.

When operating the 3235 in a low voltage mode, the device is connected per schematic shown in Figure 35. As shown in this figure, the V_{DD1} pin (pin 1) is connected to V_{CC} (+5) and the V_{DD2} pin (pin 9) is connected to +12V. Photos of the waveforms of the 3235 in the low voltage drive mode are shown in Figure 36a and b. The circuit configuration is shown in Figure 35. As shown in the photo, the 3235 has very high drive capability in both the positive and negative directions.

For comparison, the low level buffer portions of the 3210 are shown in Figure 37a and b. As is shown, both the 3235 and 3210 make excellent low level buffer drivers for heavily loaded address lines.

Figure 34. Typical Address Input Current

Figure 35. 3235 Connected in Low Voltage Drive Mode

POSITIVE ADDRESS TRANSITION

(a)
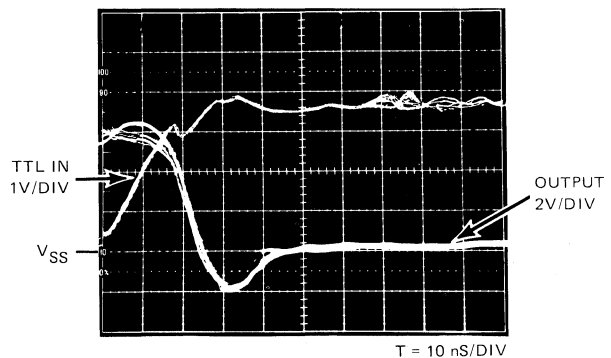
NEGATIVE ADDRESS TRANSITION

(b)

Figure 36. Typical Waveforms, 3235 Low Voltage Mode

POSITIVE ADDRESS TRANSITION
(a)

NEGATIVE ADDRESS TRANSITION
(b)
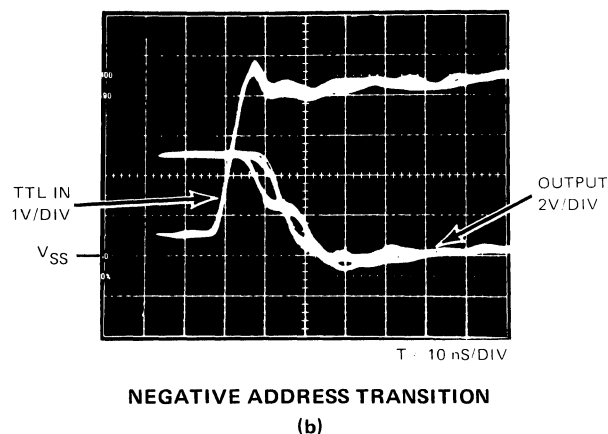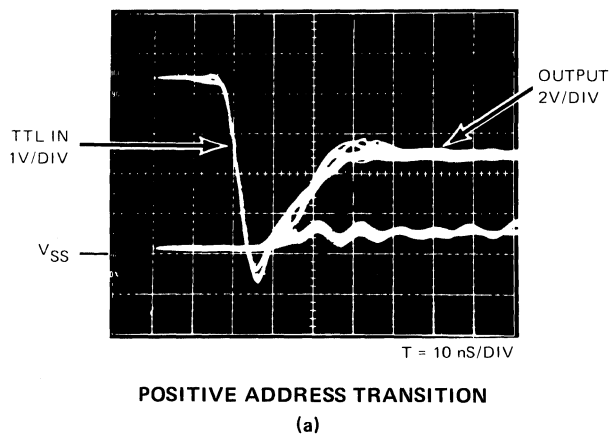
Figure 37. Typical Waveforms, 3210 Low Voltage Mode

Output Sensing

The output of the 2107B can be sensed with any TTL compatible series 74, 74L, 74LS or 74S gate. In addition, Intel provides a latch (3404) which features high speed and high density in a single package. The pin configuration for the 3404 is shown in Figure 38.
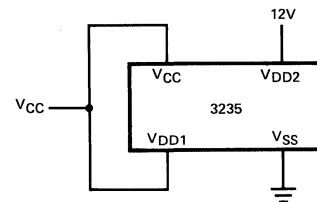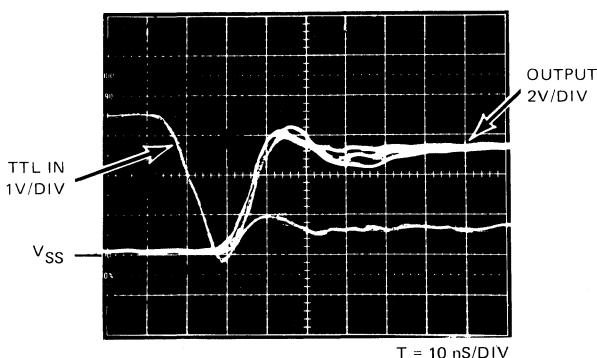
The V_{CC} input to the 2107B goes only to the output buffer as shown in Figure 8. This means that other types of outputs can be used instead of standard TTL devices if so desired. However, since there are many different ways to utilize this feature, do not exceed the maximum limits on voltage when using the 2107B in a non-standard manner.

Typical curves of output current as a function of output voltage are included in Figure 39a and b to facilitate the output interface of non-TTL loads.

System Timing and Control

The simplicity of design when using the 2107B memory component is shown by the schematic given in Figures 40, 41, and 42. The basic timing for this schematic is shown in Figure 43.

The design shown is for an expandable 16K X 18 system featuring:

1. Asynchronous memory requests/multiple ports

2. Free running refresh

The timing cycle consists of a start initiated by a memory request (MREQ) which triggers the busy latch and begins chip enable. The busy signal is used to disable other ports from requesting a memory cycle while the memory is being accessed from
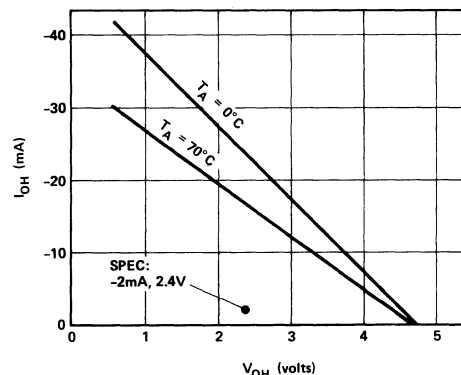
(a) HIGH LEVEL OUTPUT

(b) LOW LEVEL OUTPUT

3404

Figure 38. 3404 Pin Configuration
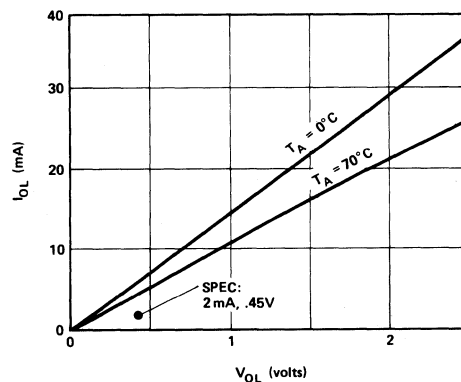
Figure 39. 2107B Output Characteristics

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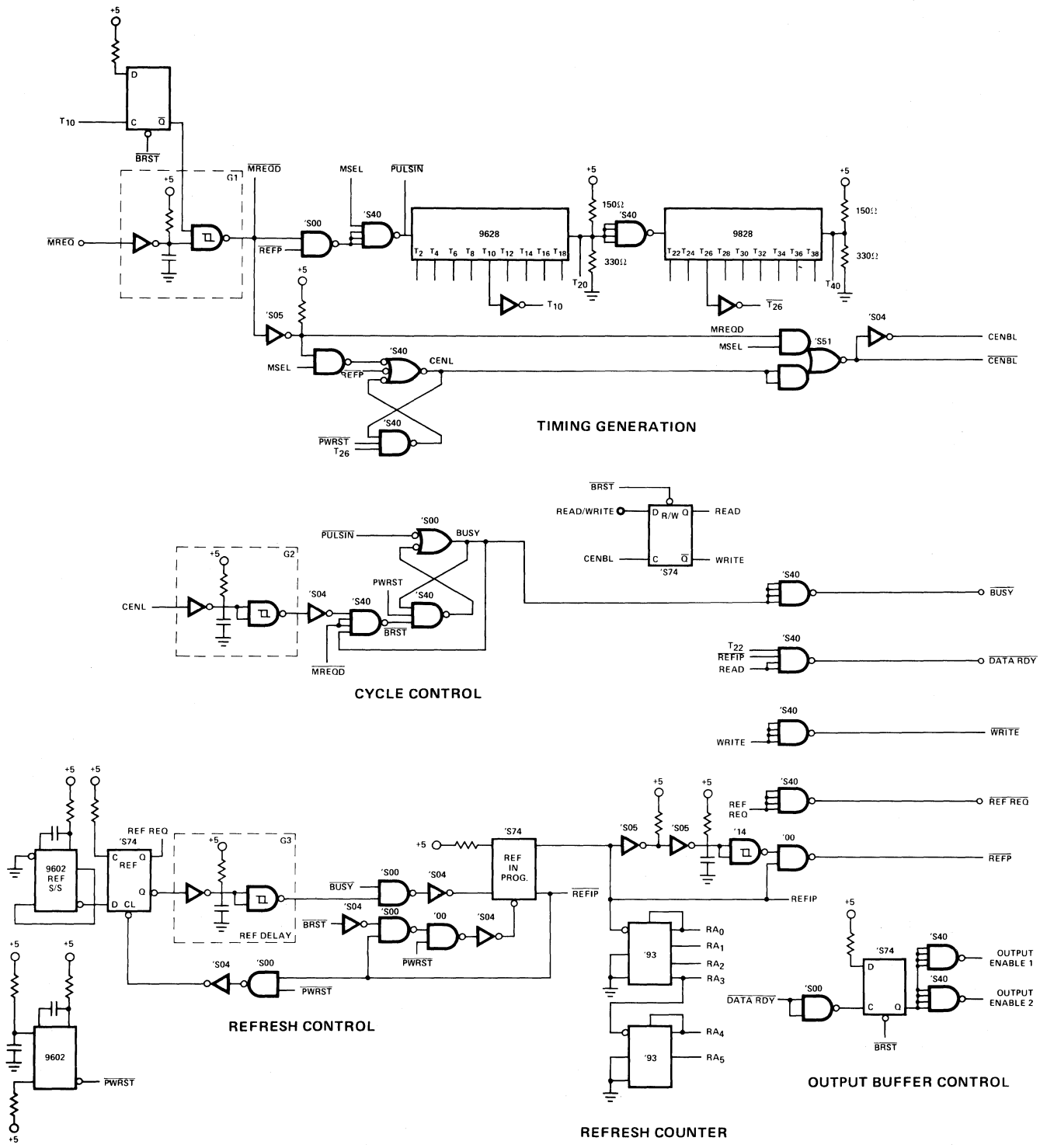
Figure 40. 16K X 18 Memory System Timing Generation
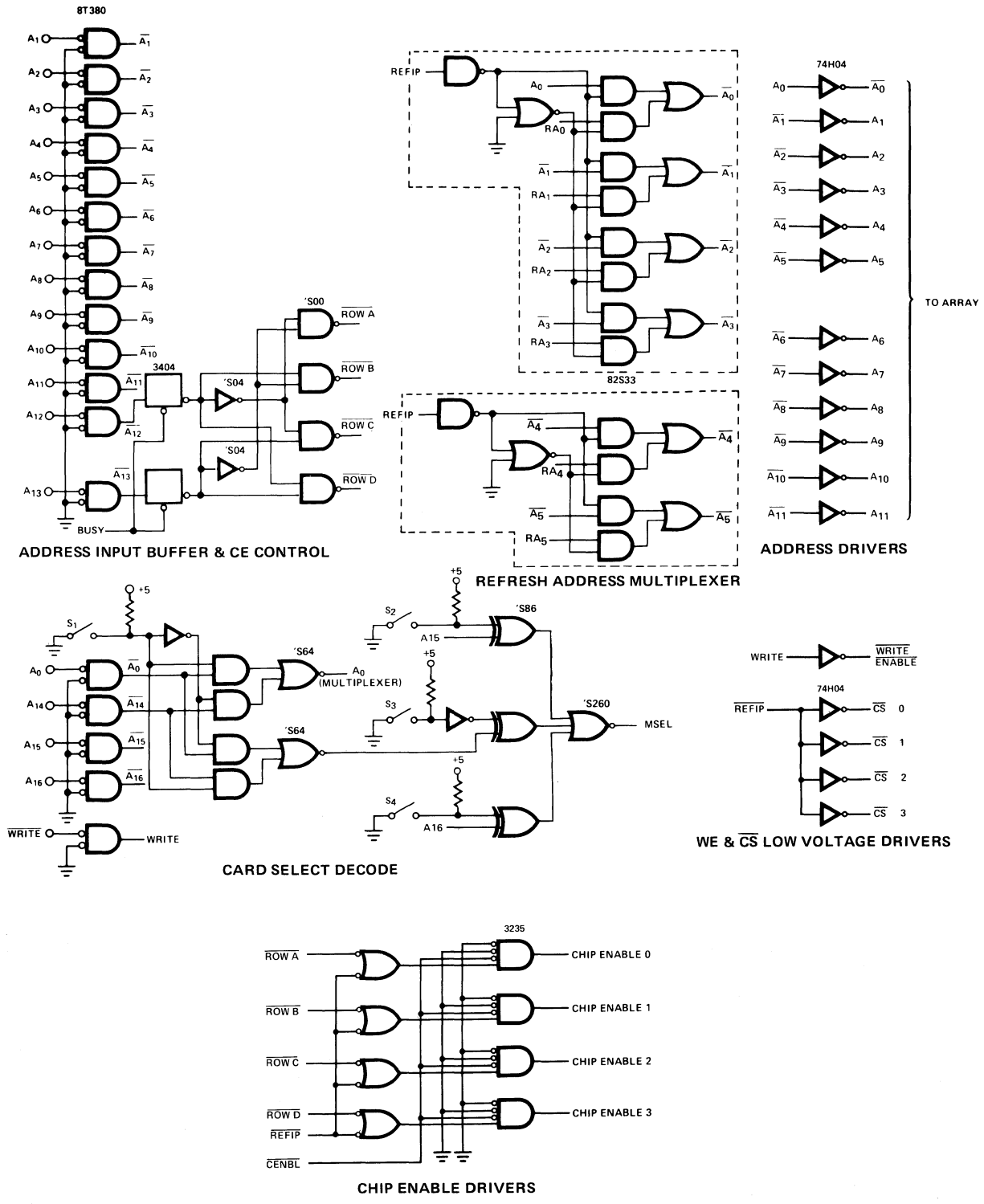
Figure 41.   16K X 18 Memory System Address Buffer Interface
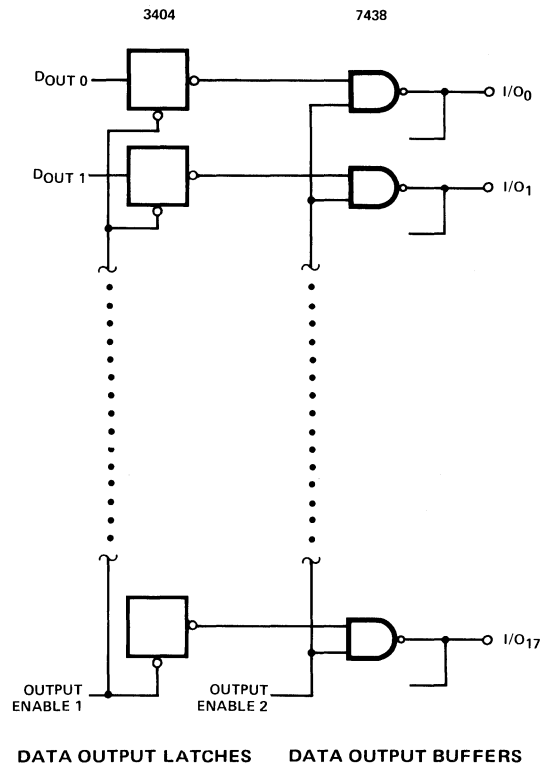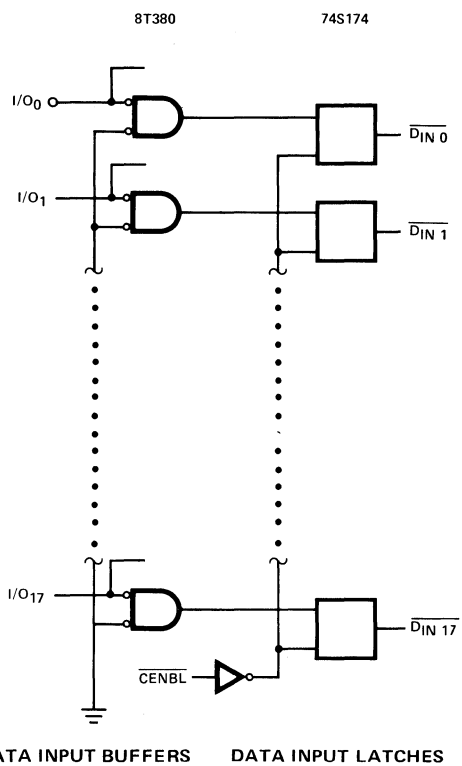
Figure 42. 16K X 18 Memory System Input/Output Interface
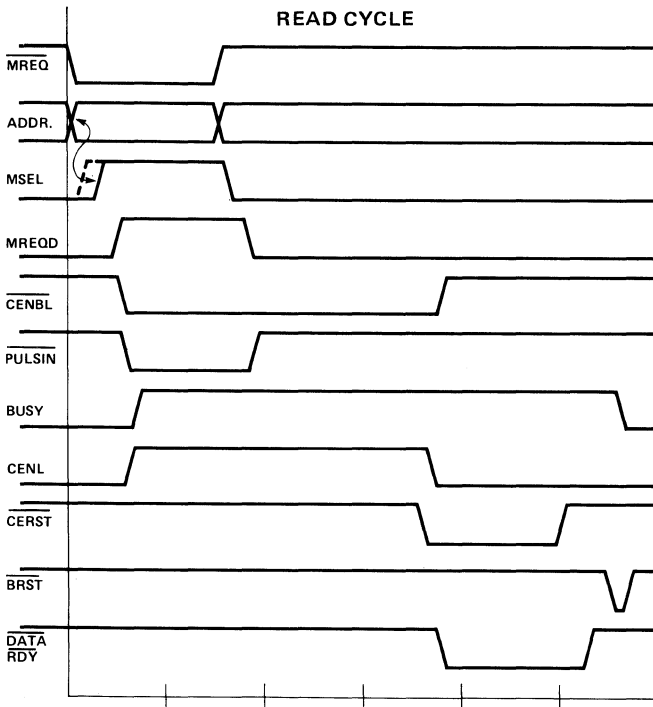
Figure 43. 16K X 18 Memory System Control Timing

another device. Since further timing signals for a read/write cycle are straightforward they will not be discussed further.

However, several things need to be said about the refresh circuitry. As many system designers know, when a memory system with asynchronous refresh runs into trouble in the checkout state, it is 99% sure to be refresh interference in one form or another in the control logic. The most likely cause of problems for asynchronous refresh is glitching between a refresh request and a normal cycle request resulting in false starts or the system not knowing whether or not it is in a refresh cycle or normal cycle.

To alleviate this problem it is necessary to determine that there are no possible requests coming from an external port to the memory when a refresh cycle is started. This will prevent the low order address line from making transitions at the wrong time (due to the multiplexer between the refresh and normal addresses) and taking excessive time to recover to the proper level.

The circuit which performs the function of delaying the onset of a refresh cycle is shown by G3 in Figure 40. Here, refresh is delayed for as long as necessary to assure that the refresh required latch (REF REQ) has had time to block further requests from all ports attached to the memory.

Attention is also called to the power on reset (PWRST) signal shown in Figure 40. This signal is necessary to assure that all latches have been reset (or set) to the proper state after power has been applied. In addition, note that the refresh/addresses RA_0 thru RA_5 are changed after the

refresh cycle is complete. This assures that the address will not be changing during refresh as chip enable goes high.

Memory Array Layout

The layout for the 2107B memory array can be identical to that used for the 2107A. An example of such a layout is shown in Figure 44. The layout in this example is constructed with grided power busing which minimizes power distribution noise. When using this technique it is important to remember to bus all power lines both vertically and horizontally through every memory component.

The effect of proper power distribution in the memory array cannot be over-emphasized. It is most desirable to bus the power lines both vertically and horizontally at every memory device

location (even if it means running a 15 mil wide printed line to achieve the connection). If it is not possible to make such a connection at every location, then the interconnect should be done as much as possible throughout the array.

As a general rule of thumb, power distribution can be considered adequate if the distance from each power pin (e.g., V_{DD} to capacitor and V_{SS} to capacitor) to the closest decoupling capacitor is less than or equal to 1.5 inches.

For some layouts, particularly those which have all timing and control as well as the memory on a single board, it may be desirable to build multi-layer boards. Attention should be paid to the construction of the internal planes to gain maximum effectiveness from these planes. If all the required power supplies cannot be distributed on internal
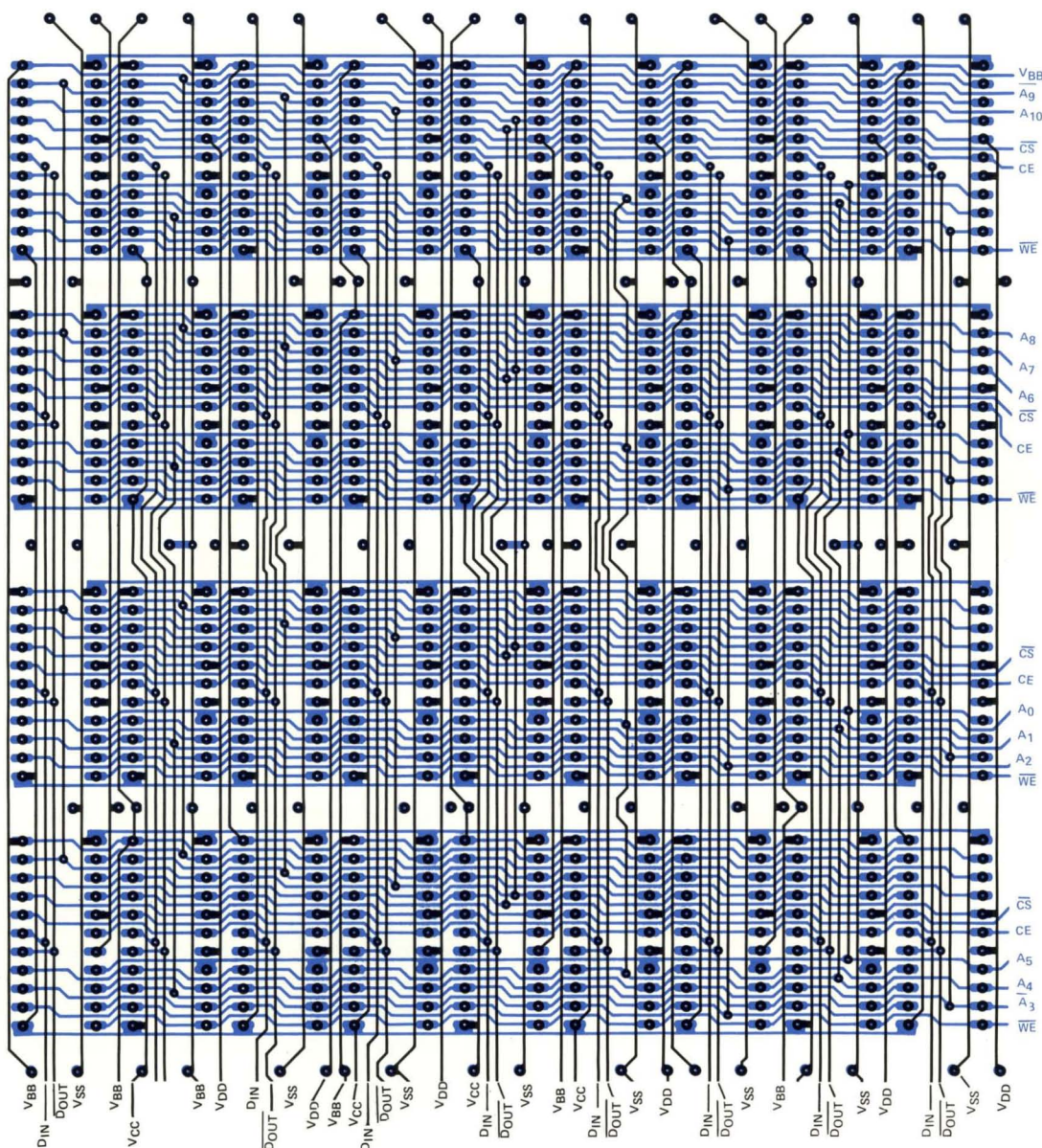

Figure 44. 2107B Memory Array Layout Using Grided Power Distribution

planes and any have to be left out and put on the upper surfaces of the board they should be removed from the internal plane in the following order:

1. V_{CC} 3. V_{DD}
2. V_{BB} 4. V_{SS}

Numbers 1 and 2 can be interchanged if there is a particularly heavy V_{CC} load due to timing, control, etc. circuitry on the board.

When constructing internal planes, care should be taken to obtain the most continuous plane possible. For example, the plane should have "fingers" between each IC feedthrough to minimize inductance.

Decoupling

As mentioned in the Transient Currents section, it is imperative to adequately decouple all supplies to the 2107B. The type and amount of decoupling recommended is most easily shown with the aid of the diagram given in Figure 45. In this figure, every other location for decoupling is $V_{DD}-V_{SS}$ using a 1.0 μF capacitor. Alternate locations can be $V_{BB}-V_{SS}$ or $V_{CC}-V_{SS}$. It is suggested that $V_{BB}-V_{SS}$ be
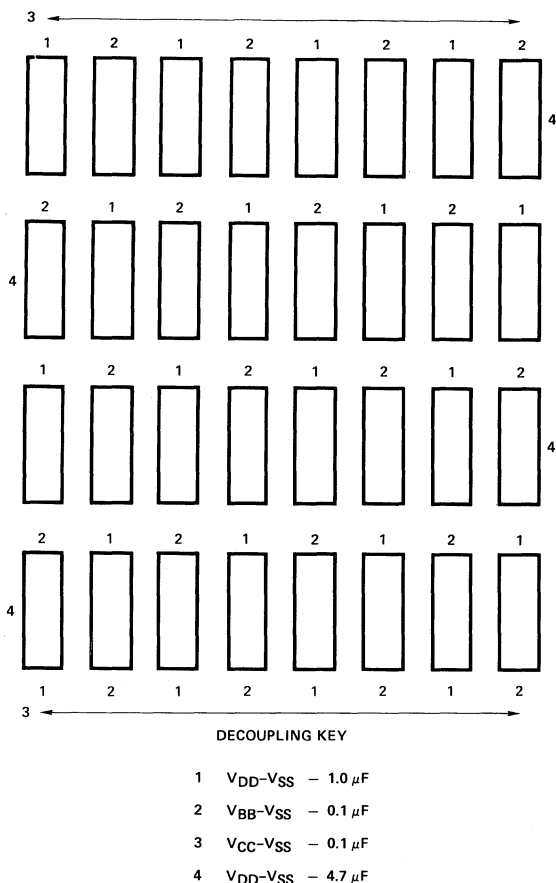
decoupled more heavily than $V_{CC}-V_{SS}$ (as shown in Figure 45), because of the higher transients on V_{BB}. Noise on the V_{BB} distribution is shown in Figure 46.

[1] V_{BB} A.C. COUPLED, 100 mV/DIV
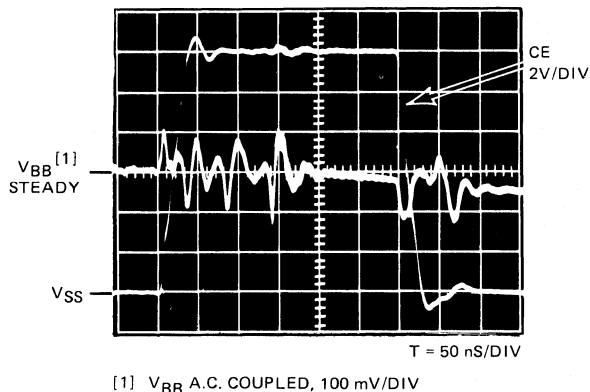
Figure 46. Typical V_{BB} Array Noise Decoupling per Figure 45

In addition to the 1.0 μF decoupling discussed above, it is necessary to provide a bulk of ~100 μF $V_{DD}-V_{SS}$ per 36 devices located near the memory array. Also, placing 4.7 μF capacitors between $V_{DD}-V_{SS}$ along the end of each row as shown will eliminate noise problems during refresh time.

The effect of changing decoupling capacitance in a system is shown in Figure 47a, b, c, and d.

These photos show the effects of different decoupling schemes on the V_{DD} supply and the effect of adding a more solid power distribution bus. (In this case #22 wire was paralleled with the existing power distribution of grided 15 mil printed line.) Each of the photos shown in Figure 47 were taken at the worst case location in the memory array at refresh time.

Figure 47a shows the V_{DD} supply with 0.1 μF spaced at every third device, no additional V_{DD} busing and no bulk capacitors (4.7 μF) at the end of each row. Note that the V_{DD} supply decreases to approximately 300 mv below desired setting with spikes driving the supply down a maximum of 440 mv. This excursion is not acceptable.

Figure 47b is for the condition of decoupling with 0.1 μF every third device and adding a 4.7 μF capacitor at the end of each row. Additional power busing on the V_{DD} and V_{SS} lines was added but was observed to have little effect on the noise, shown in Figure 47b. For this case, the V_{DD} supply is observed to decrease approximately 180 mv with spikes adding a further reduction to 240 mv. The major difference between this condition and the one shown in Figure 47a is the addition of the 4.7 μF capacitors at the end of each row. However, the decrease in V_{DD} voltage is still unacceptable.

DECOUPLING KEY

1    $V_{DD}-V_{SS}$ — 1.0 μF
2    $V_{BB}-V_{SS}$ — 0.1 μF
3    $V_{CC}-V_{SS}$ — 0.1 μF
4    $V_{DD}-V_{SS}$ — 4.7 μF

Figure 45. Recommended Memory Array Decoupling
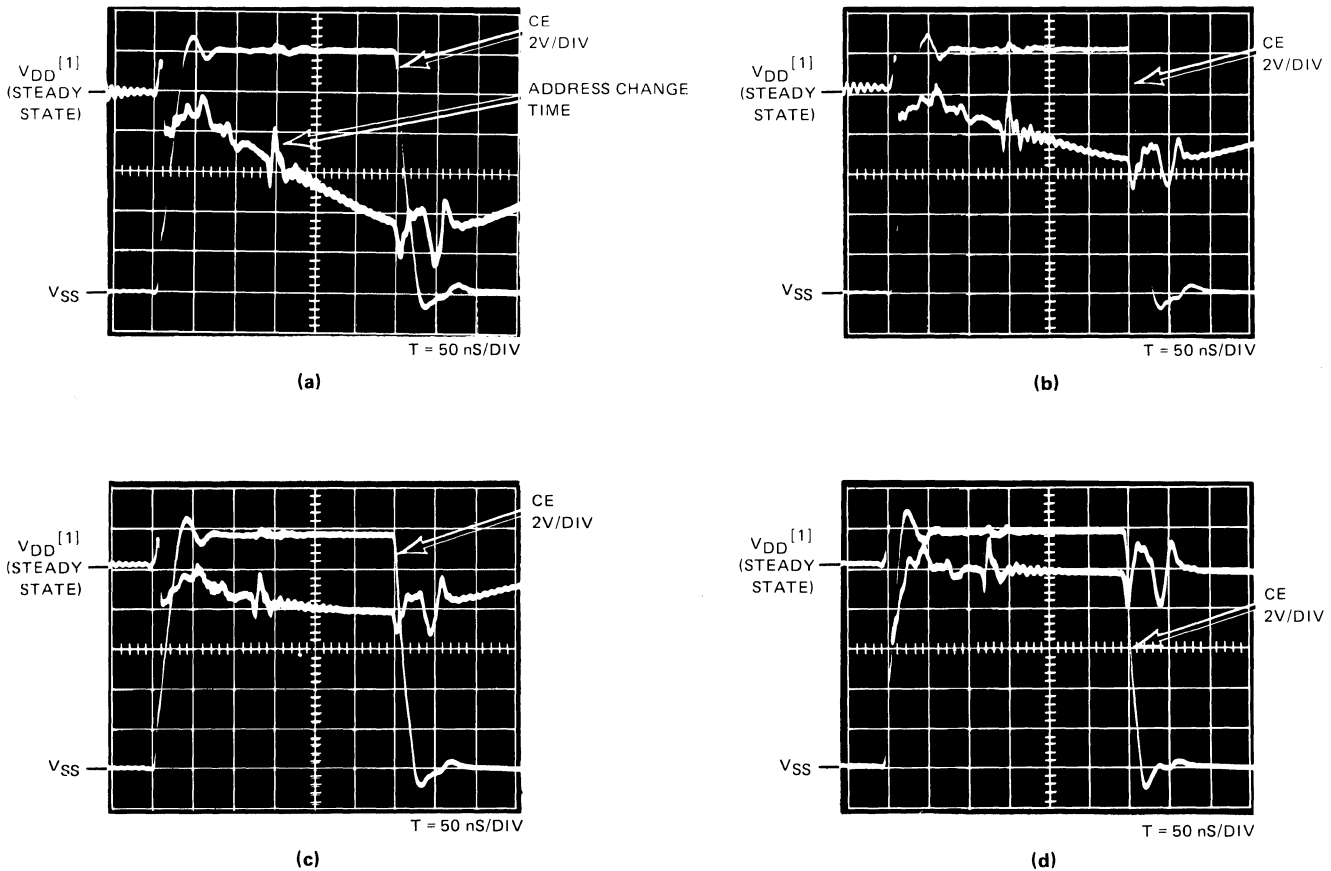
Figure 47. V$_{DD}$ Noise as a Function of Decoupling

Figure 47c shows the V$_{DD}$ supply where V$_{DD}$ in the memory array is decoupled at every other memory device location. All other conditions are per Figure 47b. Note that the offset is now only 100 mv with spikes taking the supply down to 170 mv below nominal. Such decoupling results in adequate but marginally acceptable system operation.

Figure 47d shows the V$_{DD}$ supply decoupled at every other memory device location with 1.0 μF ceramic capacitors. All other conditions are per Figure 47c. Note that the offset is approximately 20 mv with spikes lowering the V$_{DD}$ to a maximum of 200 mv for the length of time shown.

The most desirable decoupling of V$_{DD}$ to V$_{SS}$ in a memory array is therefore 1.0 μF at every other device location with 4.7 μF at the end of each row.

The above recommendations on power distribution and decoupling will result in minimal memory array power noise. However, it is certainly not the only way to suppress power distribution noise. Adequate distribution and decoupling can be assumed if the following values are achieved:

1. V$_{DD}$−V$_{SS}$ 200 mv peak
2. V$_{BB}$−V$_{SS}$ 100 mv peak

3. V$_{CC}$−V$_{SS}$ 100 mv peak
4. V$_{SS}$−V$_{SS}$ 200 mv peak   (corner to diagonal corner)

Debugging A Memory System

The design and build of memory systems using the newer, easier to use dynamic RAMs, usually results in minimum system debugging time. However, when this is not the case and the control and memory are not playing together well, life can be mighty miserable for the designer while the problem is being tracked down.

This section will deal with some of the more common problems that can affect dynamic memory systems in general, their characteristics and how to better identify them. An integral part of this section is the testing of the system to identify those conditions which cause the most problems for the memory system. In the following it is assumed that power supplies and timing are set to nominal values.

In debugging a memory system the most logical place to start is to determine that all specified criteria are met. This means looking at chip enable timing during each type of cycle both high and low

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voltage level (read, write, read-modify-write, if used, and refresh). In all cycles make sure the addresses and chip select are set up at the proper time and are held for the minimum hold time. Check all other signals for proper levels (this especially includes the address down level at the time just after chip enable goes high). Remember that the maximum address down level is a function of the chip enable rise time. Erratic operation results from a slow transition and a marginal address down level. Next, check all voltage pins for excessive noise. It is usually desirable to check the power noise at refresh time since all memory devices will be on then and noise will be at a maximum.

After the above, sync on a read cycle and make sure that the system data strobe, if any, occurs before chip enable going low has a chance to reset the data. Also check to make sure no spurious write signals are getting through at read time. In a write cycle check the write enable waveform and make sure data-in is valid at or before write enable goes low.

In a refresh cycle, write enable should be held high unless chip select is high. Also, while in the refresh mode, make sure that all refresh addresses are being accessed. This is most easily done by syncing on the high order refresh address, A_5, and looking at the low order addresses for one cycle of A_5. Checking a read-modify-write cycle is merely a combination of the above discussion of read and write.

After confirming that the specification is met in all regards and that power supply noise is within tolerance in all cycles, the designer is probably tempted to harbor ill feelings toward the memory component and/or manufacturer of same. However, it is not yet time for such.

If the memory is failing most of the data and address patterns that are being used for the test, it is useful to inhibit refresh. When doing so, make sure that the test cycle is such that refresh is being done "automatically" by the normal cycles occurring at a fast enough rate. When inhibiting refresh it may be necessary to restrict the test addressing so that all cells can be "refreshed" by a normal cycle. If the problem goes away after inhibiting refresh, you are now in the army of people who have used dynamic RAMs to be caught with refresh interference.

The only thing that can be said about refresh interference is that refresh is coming in at the wrong time! In properly designed systems, the most likely culprit is a noise glitch getting into the refresh timing circuitry to cause the problem. One of the most common causes for other types of system design is the improper use of "D" type latches. For example, if an asynchronous input (relative to clock) is applied to the D input of a latch and clocked, there will be times where the change on the D input occurs simultaneously with the clock. In some latches this can cause an order of magnitude increase in delay instead of simply missing the D input (see Figure 48). This problem also exists when using a latch made of NAND gates (see Figure 49). The method of correcting the refresh interference problem of a system is left to the imagination and luck of the designer. If the problem is not refresh interference, do not harbor ill feelings yet!
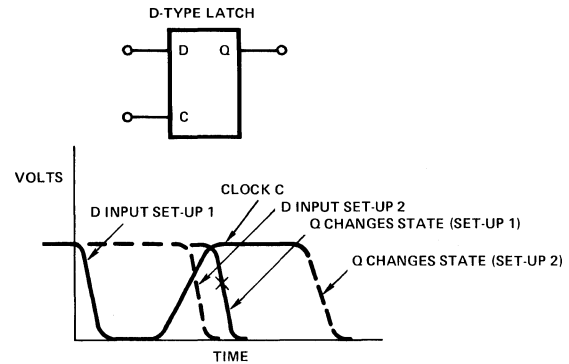
Figure 48. D-Type Latch
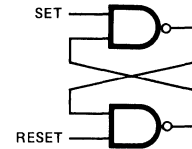
Figure 49. Cross-Coupled NAND Latch

After checking all of the above with no change in results, the next place to start is to determine whether the system is sensitive to addressing patterns. An effective test for evaluating address pattern sensitivity is Galpat. The structure of Galpat is shown in Figure 50. This test is time consuming and requires a careful monitoring of the failed data and its addresses.

Failures caused by a Galpat-only type test are most likely due to address line noise, address coupling to other signals, or refresh related. If address type noise is suspected a careful look at every point in each address path is in order. The best place to concentrate is around the address and its complement that failed.

Refresh related problems can occur during Galpat because this test takes a long time and may not "automatically" refresh the memory. (A sequential type test can refresh the memory automatically if it cycles faster than the maximum allowed

A "galloping" "1" or "0" thru memory consists of initializing the contents of memory (all "1s" or "0s") and implementing the following sequence at each successive memory location:

1. Write opposite data (from initialized state) into test address (A_{TEST})

2. Read next address ($A_{TEST} + 1$)

3. Read test address (A_{TEST})

4. Read $A_{TEST} + 2$

5. Read test address — continue read sequence for entire memory

6. Write test address back to initialize state

7. Go to next address for new A_{TEST}

8. Repeat steps 1–6 until entire memory tested

9. Complement initial data pattern and repeat steps 1–8

Figure 50. Galpat Flow Chart

refresh period.) If any address fails to get refreshed during the refresh period, Galpat will most likely pick it up.

If the above does not yield a clue, then a check of the data pattern across a word is in order. In many tests each bit in a word contains the same data. This can cause certain groups of data lines to couple into adjacent control or address lines. This problem can be tracked down by allowing only one bit in a word to change at a time.

If the memory system is having massive failures, it is very likely that the above debug procedure will reveal the problem. The second type of problem to be discussed is that of soft failures at frequent intervals. In general, these are problems caused by system noise, marginal timing, flaky peripheral device(s), or marginal memory component.

For soft failures, the first item to suspect is refresh interference. Proceed per above to isolate the problem.

A great deal of information on soft failures at nominal voltage settings can be obtained by shmooing the memory system. A shmoo consists of varying each voltage in a manner which is worst case for certain conditions.

The voltage points which emphasize certain tendencies in the memory are contained in Figure 51. The device failed address should be noted at each shmoo point to give a clue to the problem.

A broad guideline here is as follows:

Failure	Cause
1. V_{DD} low, $|V_{BB}|$ high	— timing marginal (memory tends to slow down).
2. V_{DD} high, $|V_{BB}|$ low	— noise in system. Look for V_{SS}, V_{DD}, V_{BB} noise.

Temperature variation can also reveal similar problems. For example:

Failure	Cause
1. High temperature	— timing should be suspected.
2. Low temperature	— noise should be suspected.

V_P — MOST POSITIVE V_{BB}
V_N — MOST NEGATIVE V_{BB}
V_P' — MOST POSITIVE V_{DD}
V_N' — MOST NEGATIVE V_{DD}
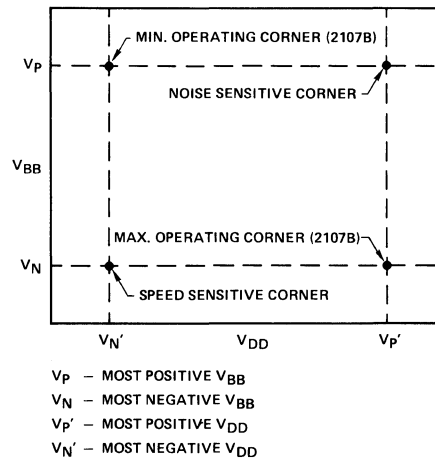
Figure 51. Example of Memory System Shmoo Plot

Power Calculations

The typical power dissipation for the 2107B with a chip enable on time of 230 nsec and a 400 nsec cycle is calculated as follows for a typical device:

Device Power

$$1. \ P_{DOP} = \begin{bmatrix} V_{DD} \times I_{DD1AV} \\ + V_{BB} \times I_{BB} \end{bmatrix}$$

$$= \begin{bmatrix} 12.0 \times 55 \text{ mA} \\ + 5.0 \times 0.1 \text{ mA} \end{bmatrix} = 660 \text{ mw}$$

Since the calculation of standby power without refresh for dynamic memory is meaningless, the following calculations are for standby with refresh:

$$2. \ P_{DOP} = \begin{bmatrix} V_{DD} \times I_{DD1} \\ + V_{BB} \times I_{BB} \end{bmatrix}$$

$$= \begin{bmatrix} 12.0 \times 0.11 \text{ mA} \\ + 5.0 \times 0.1 \text{ mA} \end{bmatrix} = 1.82 \text{ mw}$$

3. $P_{DSB} = P_{DOP} \left(\dfrac{N\,T_{CY}}{T_{REF}} \right)$

$\qquad + P_{NOP} \left(\dfrac{T_{REF} - N\,T_{CY}}{T_{REF}} \right)$

where: P_{DOP} = Operating power disspiation

$\qquad P_{NOP}$ = Non-operating (chip enable low) power dissipation

$\qquad P_{DSB}$ = Standby/Refresh power

$\qquad N$ = Number of refresh cycles in refresh period

$\qquad T_{REF}$ = Refresh period in μsec

$\qquad T_{CY}$ = Refresh cycle time in μsec

For the 2107B, the following values apply:

$\qquad N$ = 64

$\qquad T_{REF}$ = 2000 μsec

$\qquad T_{CY}$ = 0.40 μsec

4. $P_{DSB} = 660 \left(\dfrac{64\,(0.400)}{2000} \right)$

$\qquad + 1.82 \left(\dfrac{2000 - 25.6}{2000} \right)$ mw

or

5. $P_{DSB} = (8.45 + 1.80)$ mw

6. $P_{DSB} = 10.3$ mw

The above calculations do not include V_{CC} power since it is dependent only upon the output load used. The output of the 2107B is in a high impedance state when chip enable is low or chip select is high and only leakage level currents flow under these conditions.

System Power

In most systems only a portion of the memory devices will be continually accessed. For example, in the system previously described (16K × 18) worst case power is a continual access of one row (the other three rows are dissipating power in the refresh only mode).

System power for the 16K × 18 system is calculated from:

1. $P_{SYS} = P_{DS} \times N + P_{DA} \times M + P_{DOP} \times D + P_{DSB} \times E$

where: P_{DS} = Power dissipated in drivers during standby (including refresh)

$\qquad N$ = Number of drivers in standby

$\qquad P_{DA}$ = Power dissipated in drivers during max. duty cycle operation

$\qquad M$ = Number of drivers in max. duty cycle operation

$\qquad P_{DOP}$ = Power dissipated by memory device max. duty cycle

$\qquad D$ = Number of devices in P_{DOP}

$\qquad P_{DSB}$ = Power dissipated by memory devices during standby (including refresh)

$\qquad E$ = Number of devices in P_{DSB}

For this example, all drivers are assumed to be 3210s. Therefore:

P_{DS} = 387 mw		$N = 6$
P_{DA} = 467 mw		$M = 2$
P_{DOP} = 660 mw		$D = 18$
P_{DSY} = 10.3 mw		$E = 54$

or

$\qquad\qquad\qquad\qquad$ Driver Power $\qquad$ Memory Component Power

$P_{SYS} = 387 \times (6) + 467\,(2) + 660\,(18) + 10.3\,(54)$

$\qquad\qquad\qquad$ Drivers $\qquad$ Memory Devices

2. $P_{SYS} = 2322 + 934 + 11880 + 556$

$\qquad P_{DRIVERS} = 3256$ mw

$\qquad P_{MEMORY} = 12436$ mw

or

Total System Power:

3. $P_{SYS} = 15.7$ watts

The power dissipated by the drivers is approximately 26% of total system power in a max.—duty cycle operating environment.

Total standby power (including refresh is calculated from equation (1) where:

$\qquad N = 8 \qquad M = 0 \qquad D = 0 \qquad E = 72$

or:

$\qquad\qquad\qquad$ Driver $\quad$ Memory

4. $P_{SYS} = 387\,(8) + 10.3\,(72)$

$\qquad P_{SYS} = (3096 + 742)$ mw

or

$\qquad P_{DRIVERS} = 3092$ mw

$\qquad P_{MEMORY} = 742$ mw

5. $P_{SYS} = 3.83$ watts

Note that in this case, driver power amounts to approximately 81% of total system power.

Power Supply Sequencing

The V_{BB} substrate bias supply must never be allowed to be more positive than 0.3V above V_{SS}, V_{DD}, or V_{CC} at any time. Catastropic device failure can result if these criteria are not met. To minimize this problem of power sequencing and inadvertent power shorts, it is recommended that V_{BB} be referenced to V_{SS}.

ACKNOWLEDGMENT

Appreciation is extended to R. L. Papenburg of the Application Engineering Department for his work on the 3235 and 3210 driver system evaluation.

intel®

Silicon Gate MOS **2107B**

FULLY DECODED RANDOM ACCESS
4096 BIT DYNAMIC MEMORY

* Access Time -- 200 ns max.
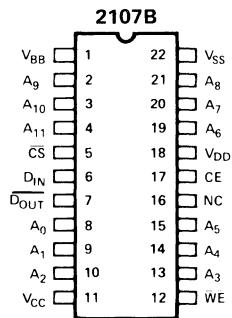* Read, Write Cycle Times -- 400 ns max.
* Refresh Period -- 2 ms

- Low Cost Per Bit
- Low Standby Power
- Easy System Interface
- Only One High Voltage Input Signal — Chip Enable
- TTL Compatible -- All Address, Data, Write Enable, Chip Select Inputs
- Read-Modify-Write Cycle Time -- 520 ns

- Address Registers Incorporated on the Chip
- Simple Memory Expansion — Chip Select Input Lead
- Fully Decoded — On Chip Address Decode
- Output is Three State and TTL Compatible
- Industry Standard 22-Pin Configuration

The Intel 2107B is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107B uses dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107B is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107B uses a single transistor cell to achieve high speed and low cost. It is a replacement for the 2107A.

PIN CONFIGURATION

2107B

V_{BB}	1	22	V_{SS}
A_9	2	21	A_8
A_{10}	3	20	A_7
A_{11}	4	19	A_6
$\overline{CS}$	5	18	V_{DD}
D_{IN}	6	17	CE
$\overline{D_{OUT}}$	7	16	NC
A_0	8	15	A_5
A_1	9	14	A_4
A_2	10	13	A_3
V_{CC}	11	12	WE
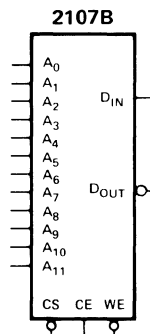
PIN NAMES

A_0-A_{11}	ADDRESS INPUTS*	V_{BB}	POWER (-5V)
CE	CHIP ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	V_{DD}	POWER (+12V)
D_{IN}	DATA INPUT	V_{SS}	GROUND
$\overline{D_{OUT}}$	DATA OUTPUT	$\overline{WE}$	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A_0-A_5.

LOGIC SYMBOL

2107B

A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8, A_9, A_{10}, A_{11}

D_{IN}

D_{OUT}

CS CE WE

BLOCK DIAGRAM

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SILICON GATE MOS 2107B
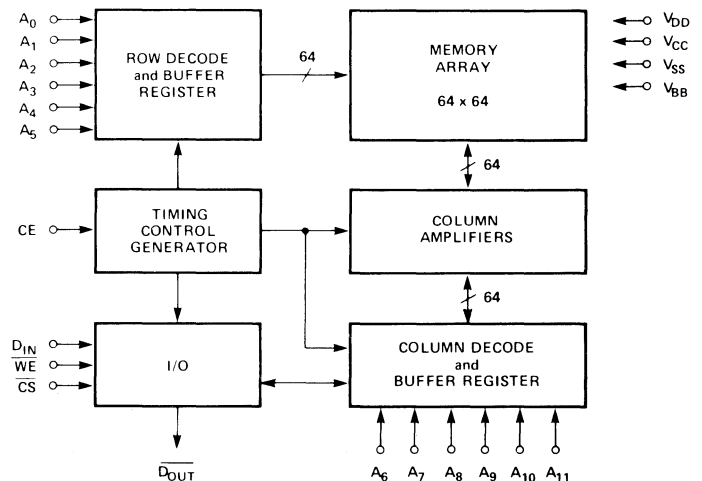
Absolute Maximum Ratings*

Temperature Under Bias .... 0°C to 70°C

Storage Temperature .... −65°C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} .... +25V to −0.3V

Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} .... +20V to −0.3V

Power Dissipation 1.25W

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB}[1] = −5V ± 5%, V_{SS} = 0V, unless otherwise noted.

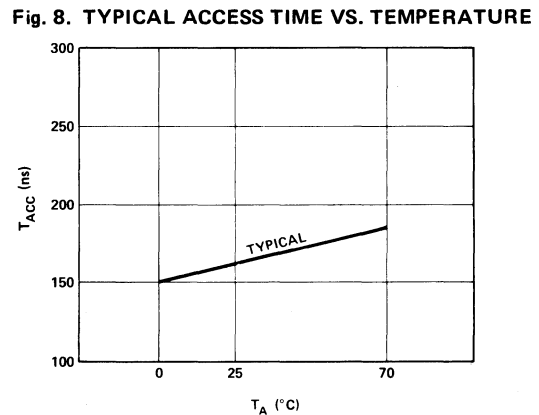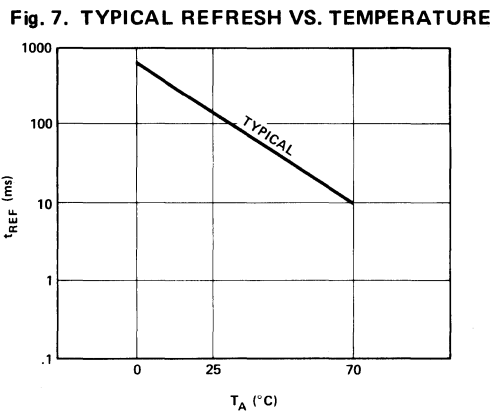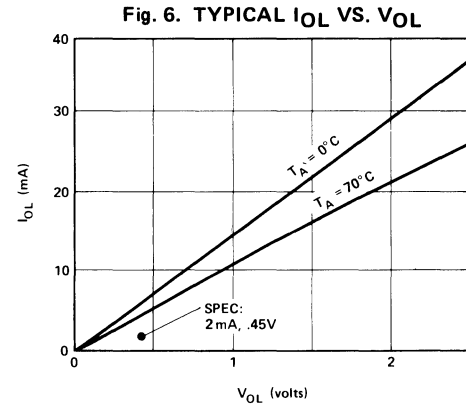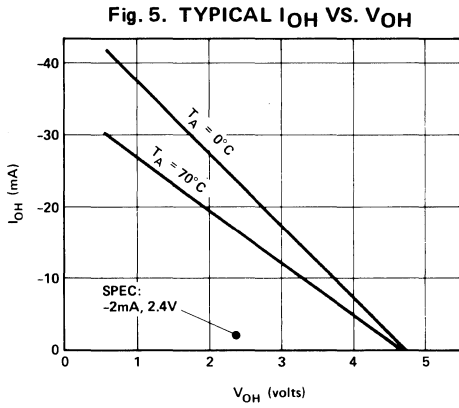| Symbol	Parameter	Min.	Typ.[2]	Max.	Unit	Conditions
I_{LI}	Input Load Current (all inputs except CE)		.01	10	µA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
I_{LC}	Input Load Current		.01	10	µA	$V_{IN} = V_{IL\,MIN}$ to $V_{IH\,MAX}$
$|I_{LO}|$	Output Leakage Current for high impedance state		.01	10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200	µA	CE = −1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on		80	100	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\,AV1}$	Average V_{DD} Current		55	80	mA	Cycle time=400ns, t_{CE} = 230ns T_A = 25°C
$I_{DD\,AV2}$	Average V_{DD} Current		27	40	mA	Cycle time=1000ns, t_{CE} = 230ns
I_{CC1}[4]	V_{CC} Supply Current during CE off		.01	10	µA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB}	V_{BB} Supply Current		5	100	µA	
V_{IL}	Input Low Voltage	−1.0		0.6	V	t_T = 20ns — See Figure 4
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	
V_{ILC}	CE Input Low Voltage	−1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD}−1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = −2.0mA

NOTES:
1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

Typical Characteristics

Fig. 1. I_{DD} AV1 VS. TEMPERATURE

85mA

GUARANTEED

72mA

I_{DD} AV1 (mA)

TYPICAL

CYCLE TIME = 400ns
t_{CE} = 230ns

T_A (°C)

Fig. 2. TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

I_{DD} AVG. (mA)

V_{DD}	= 12.6V
V_{BB}	= -4.75V
V_{CC}	= 5.25V
V_{IHC}	= 13.6V
T_A	= 25°C

t_{CE} = 300ns
t_{CE} = 250ns
t_{CE} = 200ns

T_{CY} (ns)

Fig. 3. I_{DD2} VS. TEMPERATURE

105mA

GUARANTEED

90mA

I_{DD2} (mA)

TYPICAL

T_A (°C)

Fig. 4. TYPICAL V_{IL} MAX VS. CE RISE TIME

V_{IL} MAX (volts)

V_{DD} = 12.6V
V_{IHC} = 11.6V

V_{DD} = 11.4V
V_{IHC} = 10.4V

t_T (ns)

Fig. 5. TYPICAL I_{OH} VS. V_{OH}

I_{OH} (mA)

T_A = 0°C
T_A = 70°C

SPEC:
-2mA, 2.4V

V_{OH} (volts)

Fig. 6. TYPICAL I_{OL} VS. V_{OL}

I_{OL} (mA)

T_A = 0°C
T_A = 70°C

SPEC:
2mA, .45V

V_{OL} (volts)

Fig. 7. TYPICAL REFRESH VS. TEMPERATURE

t_{REF} (ms)

TYPICAL

T_A (°C)

Fig. 8. TYPICAL ACCESS TIME VS. TEMPERATURE

T_{ACC} (ns)

TYPICAL

T_A (°C)

A.C. Characteristics [1] T_A = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%,

READ, WRITE, AND READ MODIFY/WRITE CYCLE V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	t_{AC} is measured from end of address transition
t_{AC}	Address to CE Set Up Time	0		ns	
t_{AH}	Address Hold Time	50		ns	
t_{CC}	CE Off Time	130		ns	
t_T	CE Transition Time	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	400		ns	t_T = 20ns
t_{CE}	CE On Time	230	3000	ns	
t_{CO}	CE Output Delay		180	ns	C_{load} = 50pF, Load = One TTL Gate,
t_{ACC}	Address to Output Access		200	ns	Ref = 2.0V.
t_{WL}	CE to $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CY}	Cycle Time	400		ns	t_T = 20ns
t_{CE}	CE On Time	230	3000	ns	
t_W	$\overline{WE}$ to CE Off	150		ns	
t_{CW}	CE to $\overline{WE}$	100		ns	
t_{DW} [2]	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	

Capacitance [3] T_A = 25°C

Symbol	Test	Plastic And Ceramic Pkg. Typ.	Max.	Unit	Conditions
C_{AD}	Address Capacitance, $\overline{CS}$	4	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	5	7	pF	V_{OUT} = 0V
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	8	10	pF	$V_{IN} = V_{SS}$

Notes:
1. A.C. characteristics are guaranteed only if cumulative CE on time during t_{REF} is ≤60% of t_{REF}.
2. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
3. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation

$$C = \frac{I\Delta t}{\Delta V}$$ with the current equal to a constant 20mA.

Read and Refresh Cycle [1] (Numbers in parentheses are for minimum cycle timing in ns)

$t_{CY}(400)$ · ADDRESS STABLE · ADDRESS CAN CHANGE (7) · ADDRESS STABLE · $t_{AH}(50)$ · $t_T(20)$ · $t_T(20)$ · $t_{AC}(0)$ · $t_{CE}(230)$ · CE · $t_{CC}(130)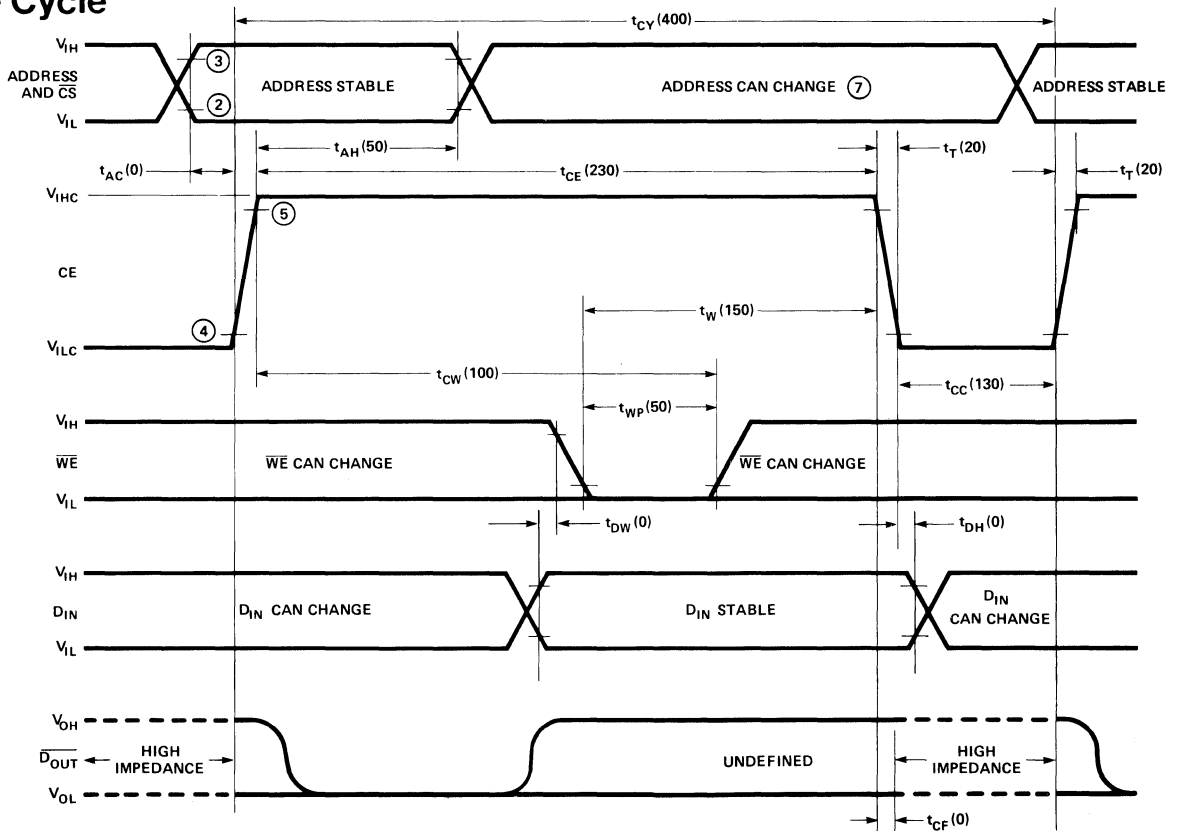$ · $t_{WC}(0)$ · WE CAN CHANGE · WE CAN CHANGE · $t_{CO}(180)$ · $t_{WL}(0)$ · $\overline{D_{OUT}}$ · HIGH IMPEDANCE · VALID (6) · HIGH IMPEDANCE · $t_{ACC}(200)$ · $t_{CF}(0)$

Write Cycle

$t_{CY}(400)$ · ADDRESS STABLE · ADDRESS CAN CHANGE (7) · ADDRESS STABLE · $t_{AH}(50)$ · $t_T(20)$ · $t_T(20)$ · $t_{AC}(0)$ · $t_{CE}(230)$ · CE · $t_W(150)$ · $t_{CW}(100)$ · $t_{CC}(130)$ · $t_{WP}(50)$ · WE CAN CHANGE · WE CAN CHANGE · $t_{DW}(0)$ · $t_{DH}(0)$ · D_{IN} CAN CHANGE · D_{IN} STABLE · D_{IN} CAN CHANGE · $\overline{D_{OUT}}$ · HIGH IMPEDANCE · UNDEFINED · HIGH IMPEDANCE · $t_{CF}(0)$
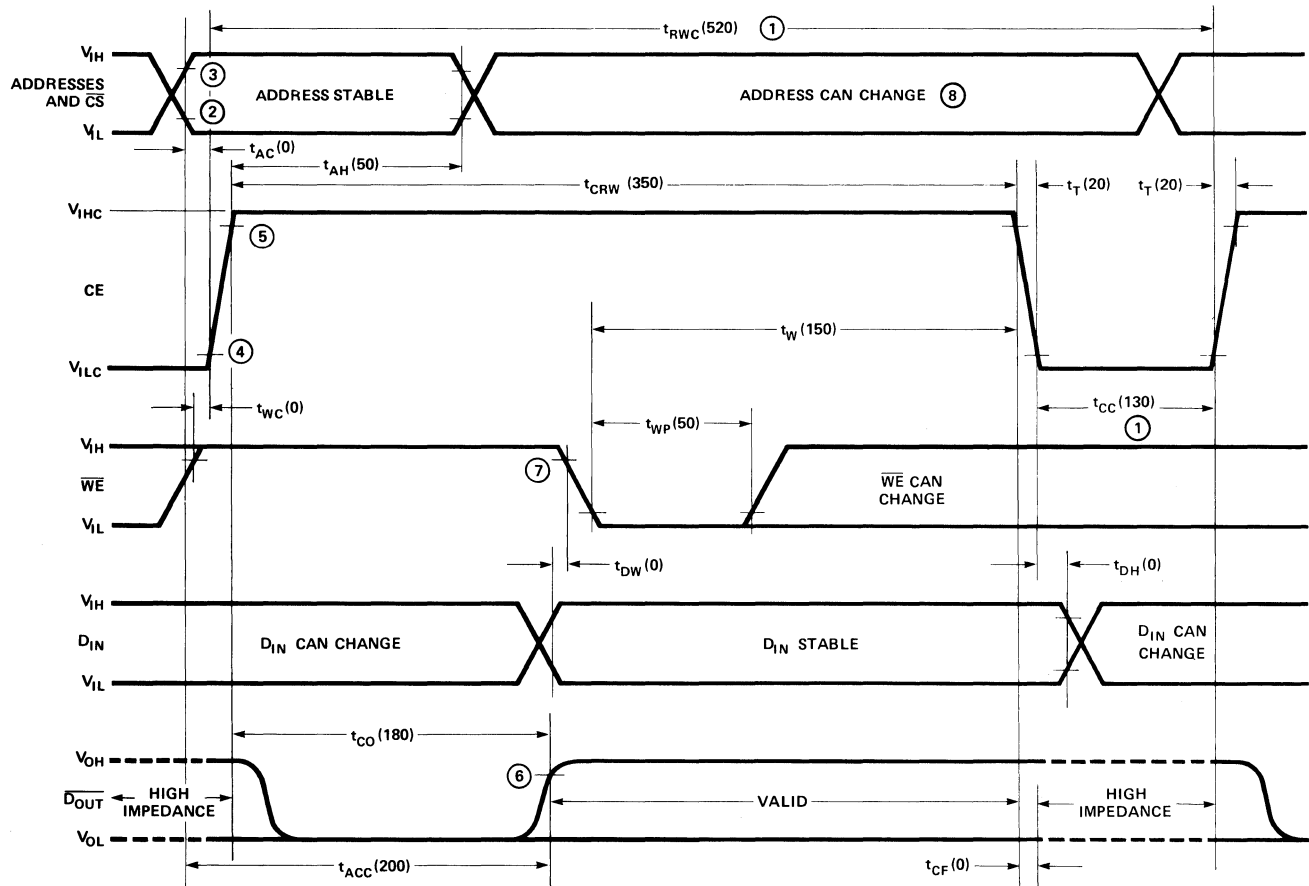
NOTES: 1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} −2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Read Modify Write Cycle[1]

| Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}	Read Modify Write(RMW) Cycle Time	520		ns	$t_T = 20ns$
t_{CRW}	CE Width During RMW	350	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	150		ns	C_{load} = 50pF, Load = One TTL Gate,
t_{WP}	$\overline{WE}$ Pulse Width	50		ns	Ref = 2.0V
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		180	ns	
t_{ACC}	Access Time		200	ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

(Numbers in parentheses are for minimum cycle timing in ns.)

NOTES:
1. A.C. characteristics are guaranteed only if cumulative CE on time during t_{REF} is ≤60% of t_{REF}. For continuous Read-Modify-Write operation t_{CC} and t_{RWC} should be increased to at least 195ns and 585 ns, respectively.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Typical Current Transients vs. Time
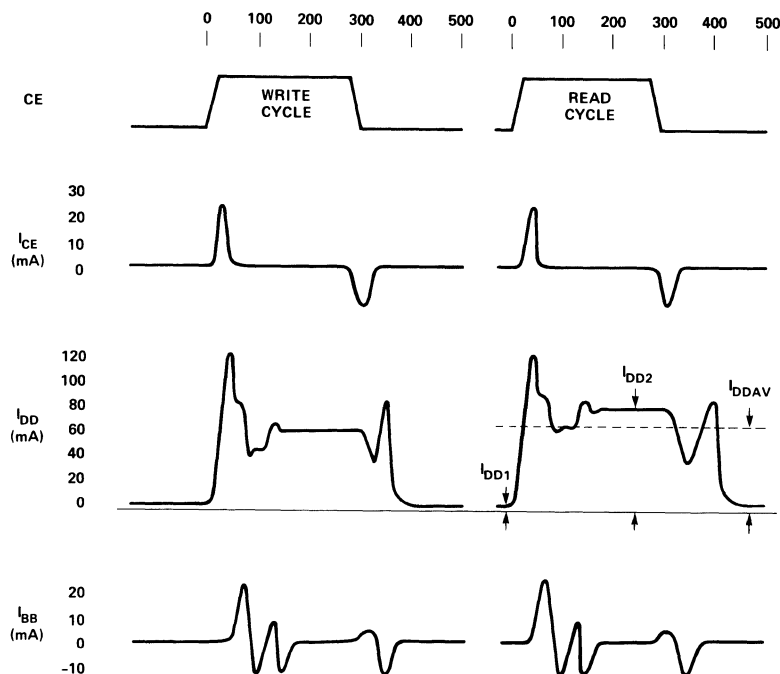
Applications

Refresh

The 2107B is refreshed by either a read cycle, write cycle, or read-modify write cycle. Only the selected row of memory array is refreshed. The row address is selected by the input signals A_0 thru A_5. Each individual row address must receive at least one refresh cycle within any two milliseconds time period.

If a read cycle is used for refreshing, then the chip select input, $\overline{CS}$, can be a logic high or a logic low. If a write cycle or read-modify write cycle is used to refresh the device, then $\overline{CS}$ must be a logic high. This will prevent writing into the memory during refresh.

Power Dissipation

The operating power dissipation of a selected device is the sum of $V_{DD} \times I_{DDAV}$ and $V_{BB} \times I_{BB}$. For a cycle of 400ns and t_{CE} of 230ns typical power dissipation is 660mW.
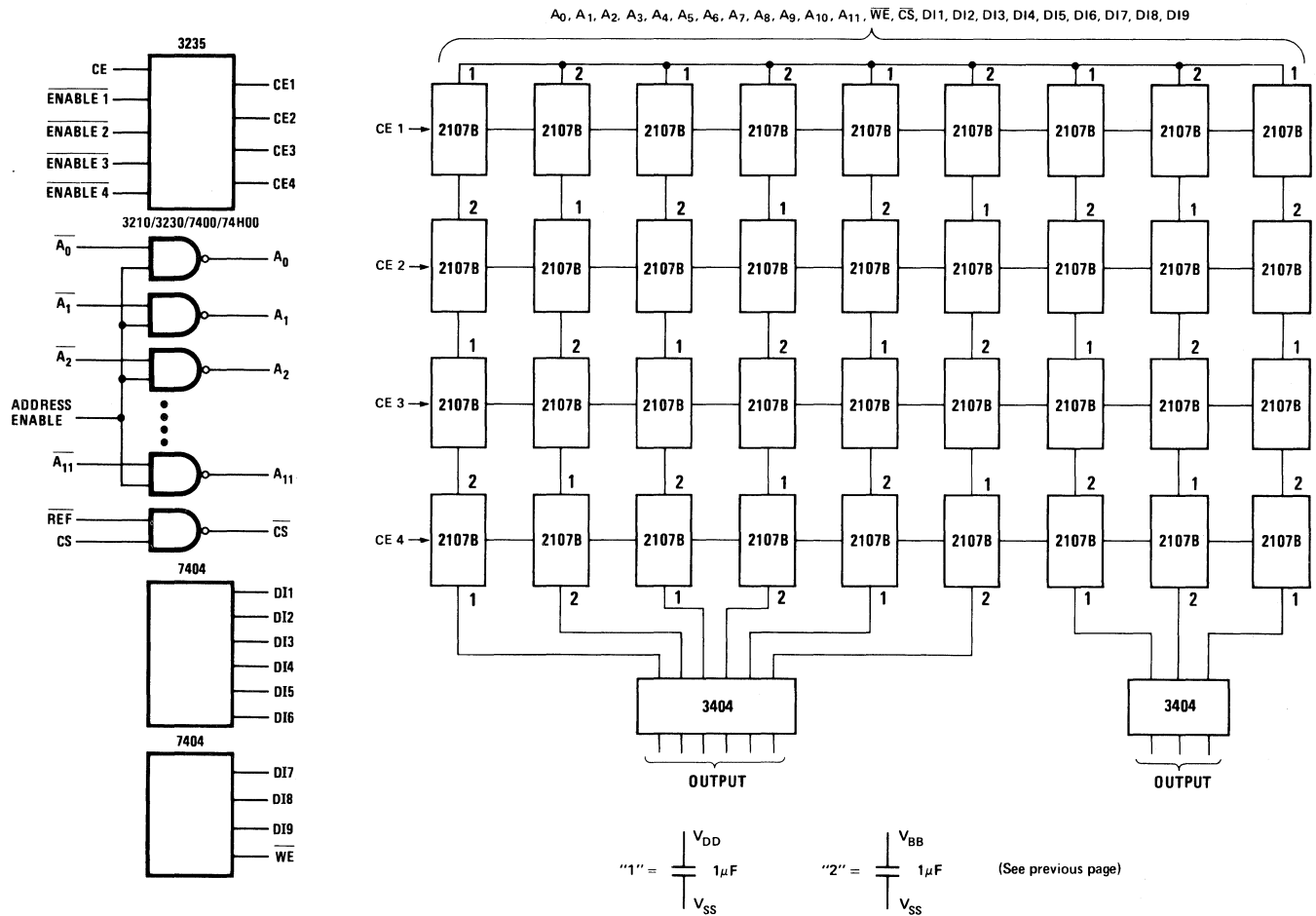
Standby Power

The 2107B is a dynamic RAM therefore when $V_{CE} = V_{ILC}$ very little power is dissipated. In a typical system most devices are in standby with V_{CE} at V_{ILC}. During this time only leakage currents flow (i.e., I_{DD1}, I_{CC1}, I_{BB}, I_{LO}, I_{L1}). The power dissipated during this inactive period is typically 1.4mW. The typical power dissipation required to perform refresh during standby is the refresh duty cycle, 1.3%, multiplied by the operating power dissipation, or 8.6mW. The total power dissipation during standby is then 10.0mW typical.

System Interfaces and Filtering

On the following page is an example of a 16K x 9 bit memory system. Device decoding is done with the CE input. All devices are unselected during refresh with $\overline{CS}$. The 3210, 3230, 3235, and 3404 are standard Intel products. Decoupling is indicated by "1" for V_{DD} to V_{SS} and "2" for V_{BB} to V_{SS}. I_{DD} and I_{BB} current surges at the CE transitions make adequate decoupling of these supplies important. It is recommended that 1μF high frequency, low inductance capacitors be used on double sided boards. V_{CC} to V_{SS} decoupling is required only on the devices located around the periphery of the array. For each 36 devices a 100μF tantalum or equivalent capacitor should be placed from V_{DD} to V_{SS} close to the array.
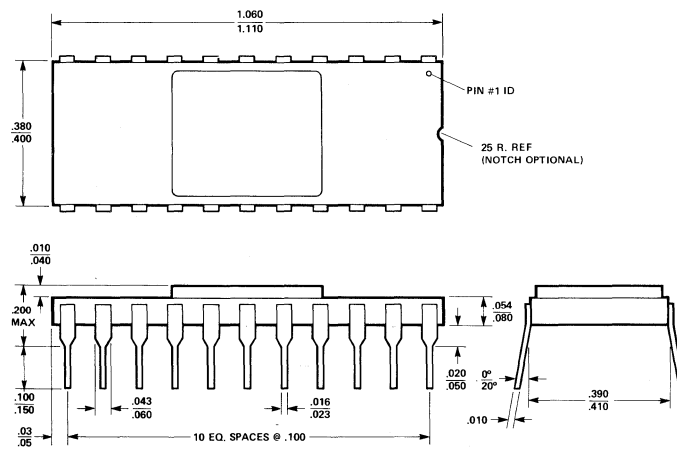
Typical System

16K X 9 BIT MEMORY CIRCUIT

$A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8, A_9, A_{10}, A_{11}, \overline{WE}, \overline{CS}, DI1, DI2, DI3, DI4, DI5, DI6, DI7, DI8, DI9$

3235

CE
$\overline{ENABLE\ 1}$
$\overline{ENABLE\ 2}$
$\overline{ENABLE\ 3}$
$\overline{ENABLE\ 4}$

CE1
CE2
CE3
CE4

3210/3230/7400/74H00

$\overline{A_0}$ → A_0
$\overline{A_1}$ → A_1
$\overline{A_2}$ → A_2
ADDRESS ENABLE
$\overline{A_{11}}$ → A_{11}

$\overline{REF}$
CS → $\overline{CS}$

7404

DI1
DI2
DI3
DI4
DI5
DI6

7404

DI7
DI8
DI9
$\overline{WE}$

OUTPUT   OUTPUT

"1" = V_{DD} 1μF V_{SS} "2" = V_{BB} 1μF V_{SS} (See previous page)

Packaging Information

22-LEAD CERAMIC DUAL IN-LINE PACKAGE OUTLINE (C)

$\frac{1.060}{1.110}$

PIN #1 ID

25 R. REF
(NOTCH OPTIONAL)

$\frac{.380}{.400}$

$\frac{.010}{.040}$

.200 MAX

$\frac{.100}{.150}$

$\frac{.043}{.060}$

$\frac{.016}{.023}$

$\frac{.054}{.080}$

$\frac{.020}{.050}$

0°
20°

.010

$\frac{.390}{.410}$

$\frac{.03}{.05}$

10 EQ. SPACES @ .100

2107B SELECTION GUIDE

INTEL PART NO.	MAXIMUM ACCESS TIME (ns)	MINIMUM READ OR WRITE CYCLE (ns)	MINIMUM RMW CYCLE (ns)	REFRESH TIME (ms)
2107B	200	400	520	2
2107B-4	270	470	590	2
2107B-6	350	800	960	1
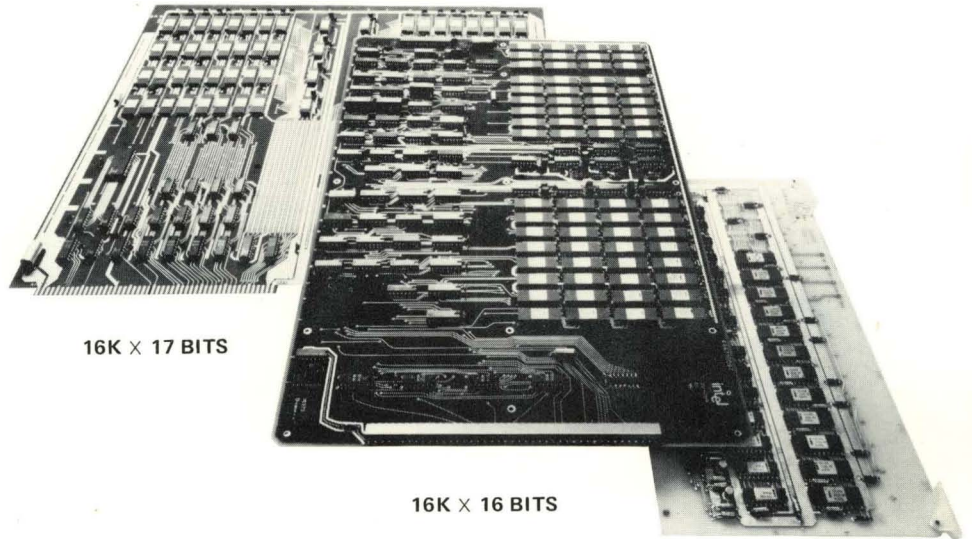
16K × 17 BITS

16K × 16 BITS

4K × 16 BITS
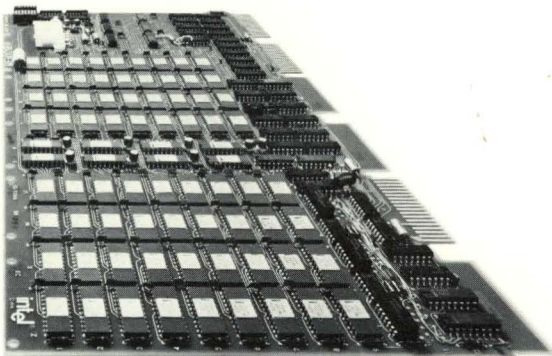
16K × 18 BITS

Intel sells a complete line of memory and microprocessor components. In addition, Intel Memory Systems, located in Sunnyvale, California, designs and manufactures memory cards, add-on memories, and complete memory systems. For more information about these components or memory systems, contact your local Intel sales representative.

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