intel

System 432/600
System Reference Manual

172098-001

SYSTEM 432/600
SYSTEM REFERENCE MANUAL

Order Number: 172098-001

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

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The objective of this manual is to provide a single definitive reference source for Intel's System 432/600 family of computer products. This manual describes their physical and functional characteristics, hardware and software interfaces, modularity, and configurability in sufficient depth for the reader to select and configure a System 432/600 for a specific application.

Specific items of interest may be located in the Table of Contents.

This manual is divided into six chapters:

Chapter 1 Introduction and General Description

This chapter provides a brief overview of the System 432/600 family of products. It describes the modularity and extensibility of the subsystem modules and briefly covers functional characteristics. It introduces the PC boards, backplanes, card cages, chassis, and the complete OEM computer systems available in the System 432/600 product line.

Chapter 2 Physical Characteristics and Configuration

This chapter gives a brief introduction to module function and extensibility, and lists physical characteristics of the hardware including backplanes and card cages, PC board form factors, keying, and board placement. It defines power and cooling requirements so that requirements for a particular board group may be calculated. It provides pointers on configuration criteria for typical small, medium, and large system configurations.

Chapter 3 System Functional Description

This chapter provides a detailed functional description of each module's operation in the system, and overall system functions. It describes the modularity and extensibility of memory, processor, and I/O boards.

Chapter 4 Software Interface

This chapter describes the system reset mechanisms, communication ports, and local registers available to system software, and defines their use in the system. Error logging and diagnostic registers and controls are listed and described.

Chapter 5 System Performance

Factors affecting the performance of multiprocessor systems are discussed, and the System 432/600 is compared to conventional computers.

Chapter 6 Reliability and Maintenance

This chapter provides an overview of System 432/600 diagnostic software and the special hardware it uses to isolate system faults to board level.

Additional related information is available from the following documents:

Introduction to the iAPX 432 Architecture, Order Number: 171821

iAPX 432 Object Primer, Order Number: 171858

iAPX 432 General Data Processor Architecture Reference Manual, Order Number: 171860

iAPX 432 Interface Processor Architecture Reference Manual, Order Number: 171863

System 432/600 Diagnostic Software User's Guide, Order Number: 172099

Intel Multibus Specification, Order Number: 9800683

Intel Multibus Interfacing, Application Note: AP-28

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CHAPTER 1
INTRODUCTION AND GENERAL DESCRIPTION

INTRODUCTION

This chapter introduces and provides a brief overview of the Intel's System 432/600 family of products. It describes the capability and extensibility of the subsystems and briefly covers the functional characteristics of each module.

System 432/600 computers utilize the advanced architecture of the iAPX 432 Micromainframe VLSI components. The Micromainframe components are the 43201/43202 General Data Processor (GDP) chip-pair and the companion 43203 Interface Processor (IP) chip which unburdens the GDP of all input/output handshakes, synchronization, and data transfers. Through subsystem extensibility, System 432/600 computers offer a wide range of performance, memory capacity, and input/output capability.

The System 432/600 product line includes logic boards, backplanes, cables, card cages, and a powered and cooled chassis. They are offered individually and as integrated 32-bit OEM computer systems.

GENERAL DESCRIPTION

A simplified block diagram of the System 432/600 is shown in Figure 1-1.

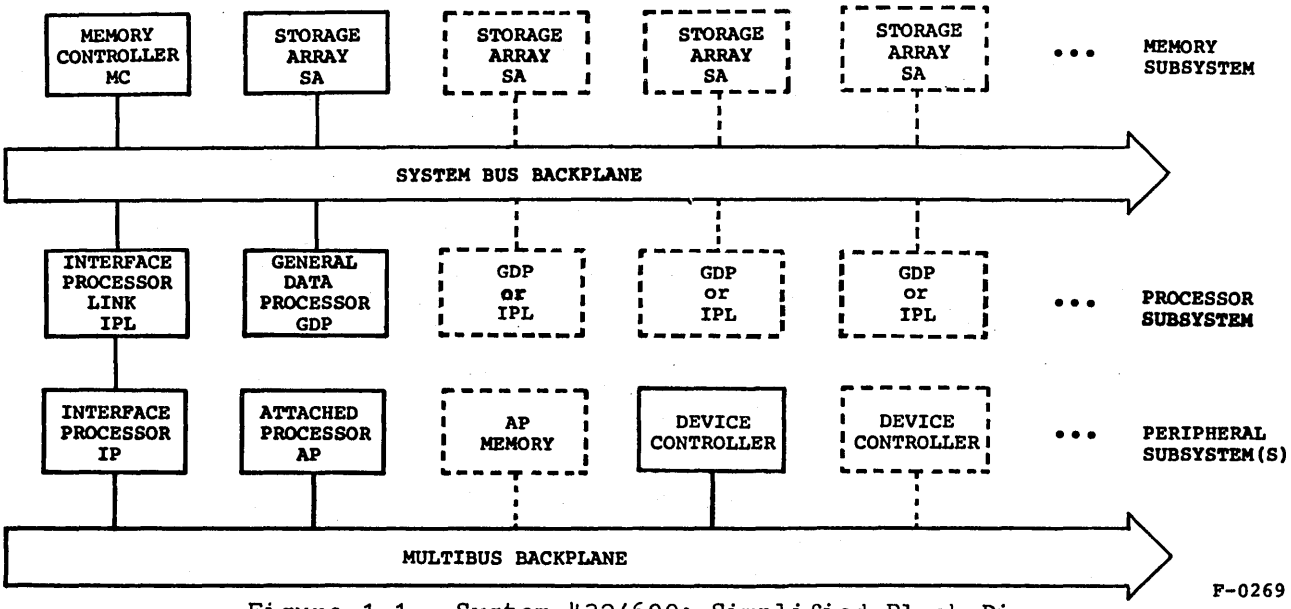


Figure 1-1. System 432/600: Simplified Block Diagram

A System 432/600 comprises one Processor Subsystem, one Memory Subsystem, and one to five Peripheral Subsystems.

The Processor Subsystem and the Memory Subsystem reside on the System Bus backplane. This portion of the System 432/600, the Processor Subsystem plus the Memory Subsystem, is called the Central System.

Each Peripheral Subsystem resides on a separate Multibus backplane.

The Processor Subsystem contains one General Data Processor (GDP) board and one Interface Processor Link (IPL) board, plus zero to four additional boards which may be any combination of GDP and IPL boards. Each IPL board connects a Peripheral Subsystem to the Central System. Thus, a Processor Subsystem could contain one GDP board and five IPL boards, connecting to five Peripheral Subsystems. At the other extreme, a Processor Subsystem could contain five GDP boards and one IPL board, connecting to one Peripheral Subsystem. The user chooses the mix of data processing capability (GDPs) and input/output capability (Peripheral Subsystems) which best meets his needs.

The Memory Subsystem contains one Memory Controller (MC) board plus one to ten Storage Array (SA) boards. Each SA board contains 256K bytes of memory with Error Correction Code (ECC) protection. The user can thus configure a System 432/600 from 256K bytes to 2.5M bytes of memory.

Each Peripheral Subsystem contains one Interface Processor (IP) board and one Attached Processor (AP) board, plus peripheral device controllers and additional AP memory as required. The IP board on the Multibus backplane connects to its companion IPL board on the System Bus backplane via a Processor Link (ProcLink) cable. The Attached Processor (AP) may be any Multibus-compatible single board computer. The combination of the IPL board on the System Bus backplane plus the IP board and the AP board on the Multibus backplane, forms a logical input/output processor.

Each GDP board contains one independent GDP chip-pair. Hardware mechanisms provide for software-transparent multiprocessing, which allow GDPs to be added to an existing system by simply plugging additional GDP boards into the System Bus backplane; there is no effect on application software, system software, or the memory access arbitration logic that controls the access of multiple processors to the Memory Subsystem. Similarly, removing a GDP board from a multiple GDP system (e.g., because of a board malfunction) has no effect beyond the reduced system throughput caused by the reduction of available GDPs.

The Memory Subsystem is accessible to all the processors in the System 432/600, where "processors" means both the General Data Processors and the logical input/output processors (IPL/IP/AP combination) described above. Data is stored on modular Storage Array boards which are accessed via the Memory Controller. Only one MC board is necessary in any System 432/600 configuration.

The Memory Controller supports byte addressability and an interleave option to enhance performance. Memory size is expanded by inserting additional SA boards into the System Bus backplane, with no hardware or software changes required. When the interleave option is enabled, SA boards must be added in pairs.

The Peripheral Subsystems relieve the Central System of all general input/output processing, device control, and operator control functions. No switches or other operator controls connect to the Central System; the only way to start, stop, or interrupt the Central System is via programs running on the Attached Processor. Thus, the high speed Central System is never forced to wait during operation for human intervention or response.

Peripheral Subsystems may be added to a System 432/600 by attaching another Multibus backplane. The capability of an existing Peripheral Subsystem may be expanded by adding any Multibus-compatible peripheral device controller board, or by adding Multimodule mini-boards to Multimodule-compatible mother boards.

As outlined above, System 432/600 hardware provides extensible subsystems, each with a high degree of modularity. All logic board types, backplanes, and card cages have been designed to provide mechanically, electrically, and logically independent and decentralized modules. This allows an incremental approach to selecting the modules necessary to achieve a System 432/600 with a desired range of functionality and performance. An additional benefit is the ability to expand subsystems, after a System 432/600 has been configured and installed, by simply inserting additional modules.

In addition to being highly configurable and extensible, the System 432/600 is easily maintained. System 432/600 Diagnostic Software isolates a system malfunction to an individual board. Simply replacing the board specified by the diagnostics returns the system to full operational status.

SYSTEM 432/600 PRODUCT FAMILY

Table 1-1 is a summary of the System 432/600 product family.

Table 1-1. System 432/600 Product Family

NUMBER	MODULE NAME	
iSBC 432/601	General Data Processor Board (GDP)	
iSBC 432/602	Interface Processor Board (IP)	
iSBC 432/603	Interface Processor Link Board (IPL)	
iSBC 432/604	Memory Controller Board (MC)	
iSBC 432/607	Storage Array Board (SA)	256K byte
iSBC 432/610	System Bus Backplane	6-slot
iSBC 432/611	System Bus Backplane	12-slot
iSBC 432/612	System Bus Backplane	18-slot
iSBC 432/615	Multibus Backplane	6-slot
iSBC 432/616	Multibus Backplane	12-slot
iSBC 432/620	Card Cage	6-slot
iSBC 432/621	Card Cage	12-slot
iSBC 432/622	Card Cage	18-slot
iSBC 432/630	432/600 System Chassis	120 VAC/60 Hz
iSBC 432/631	432/600 System Chassis	230 VAC/50 Hz
System 432/670	Integrated Computer	120 VAC/60 Hz
System 432/671	Integrated Computer	230 VAC/50 Hz

BACKPLANES

One System Bus backplane and one Multibus backplane are necessary to configure a System 432/600. A System Bus backplane is used to interconnect General Data Processor, Interface Processor Link, Memory Controller, and Storage Array boards. The System Bus contains various control and error lines, and a system wide Specification/Address/Data (SAD) bus. The SAD bus is 36 bits wide; 32 data bits plus one parity bit for each 8-bit byte.

All communication on the System Bus is synchronous, controlled and synchronized by the 8 MHz clock on the MC board. The MC drives one set of control lines for General Data Processor and Interface Processor Link boards, and another set of control lines to the Storage Array boards. The MC board fits into one dedicated slot position in a System Bus backplane.

A Multibus backplane (as defined by the IEEE-P796 Multibus Standard) interconnects the Interface Processor, Attached Processor, and peripheral device controller boards of a Peripheral Subsystem. A Processor Link (ProcLink) cable connects the IPL board on the System Bus backplane to the IP board on the Multibus backplane to complete the system communications path. The ProcLink cable also allows physical separation of the System Bus and Multibus backplanes, if desired. Mounting dimensions and power connections on the System Bus and Multibus backplanes are similar; either may be mounted easily in the card cages listed in Table 1-1.

PROCESSOR SUBSYSTEM

The Processor Subsystem contains GDP boards and IPL boards. An IPL board is the "agent" on the System Bus backplane for an IP board and AP board on a Multibus backplane.

The Processor Subsystem contains one GDP board and one IPL board, plus up to four additional boards which may be any mix of GDP or IPL.

Each GDP and IP board contains a clock generator for its own internal sequencing. This allows each processor to run at its own clock rate, regardless of other processor rates or the Memory Subsystem clock rate. Each IPL board operates at the clock rate set by its companion IP board, except for interaction with the System Bus, which uses the Memory Controller clock.

A GDP board performs the data manipulations of a typical computational task, communicating with memory and other processors via the System Bus.

A General Data Processor is self-dispatching; it automatically performs the normal cycle of running a process (program unit) until the process completes, blocks (e.g., waiting for input/output), or times out. It then re-schedules the process for subsequent execution, and begins executing the next ready process with no software intervention. System software is not affected by the number of processors in a system or by which processor is executing a particular process.

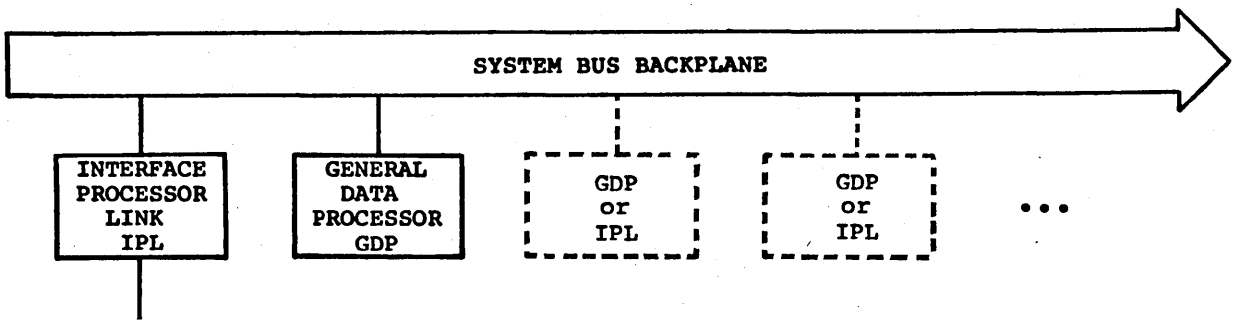


Figure 1-2. Processor Subsystem

All processors in a system share memory via the System Bus. A round-robin arbitration scheme allows processors to arbitrate priority for the next memory access. This ensures that each GDP and IP has equal opportunity for access to memory, and prevents memory access conflicts. Since the IP board is physically not on the System Bus, the IPL board contains arbitration logic for the IP. Attached Processor accesses to the Central System use the IPL/IP board-pair as an intermediary.

Adding or removing a processor board from a multiprocessing system does not affect the arbitration logic or system software.

MEMORY SUBSYSTEM

The Memory Subsystem for any System 432/600 contains one Memory Controller board. The MC can logically control and access from one to sixteen Storage Array boards. To support Byte Addressability, the MC logic controls 1-, 2-, 4-, 6-, 8-, and 10-byte accesses as requested by system processors. For any Read request, the Memory Subsystem provides the exact number of bytes a processor requests, rather than a fixed length word.

A memory interleave option is available to enhance system performance. This option uses two banks of memory with alternating addresses to provide faster data access by overlapping memory operations. Interleave operation is selected by one jumper on the MC board. This option requires Storage Array boards to be installed in pairs to implement the alternate bank addressing.

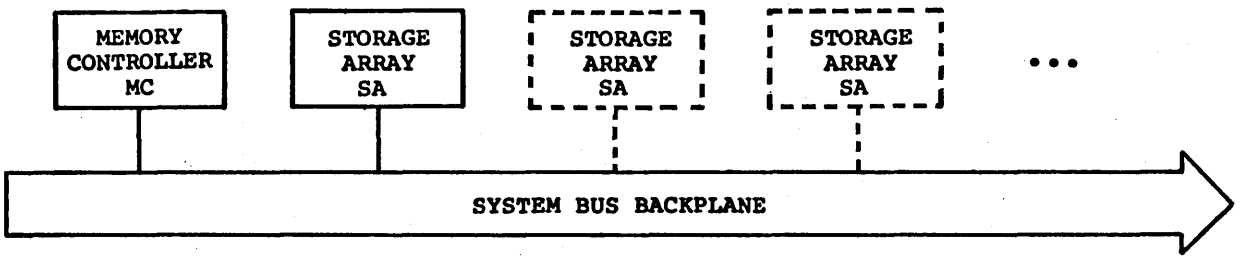


Figure 1-3. Memory Subsystem

Each Storage Array board contains logic to generate, check, and store a 7-bit Error Correction Code (ECC) for each 32-bit data word. As data is read from memory, single bit errors are detected and corrected, and double bit errors are detected and logged in a system error register.

The size of an existing Memory Subsystem may be expanded by simply plugging in additional SA boards. Refer to the Interleave Option description in Chapter 2 for memory expansion details.

PERIPHERAL SUBSYSTEM

Implementation of the Peripheral Subsystem provides for attached processing and peripheral device control to be performed by standard Multibus products. Multibus compatible Single Board Computers may be used as Attached Processors. The Attached Processor for a System 432/600 is selected by the user; information on AP requirements is given in Chapter 2. More than one Peripheral Subsystem with its Attached Processor may be present within a system. Any Multibus compatible peripheral device controller, direct memory access controller, or communications controller may be used in a Peripheral Subsystem. Additional AP memory may be added as required.

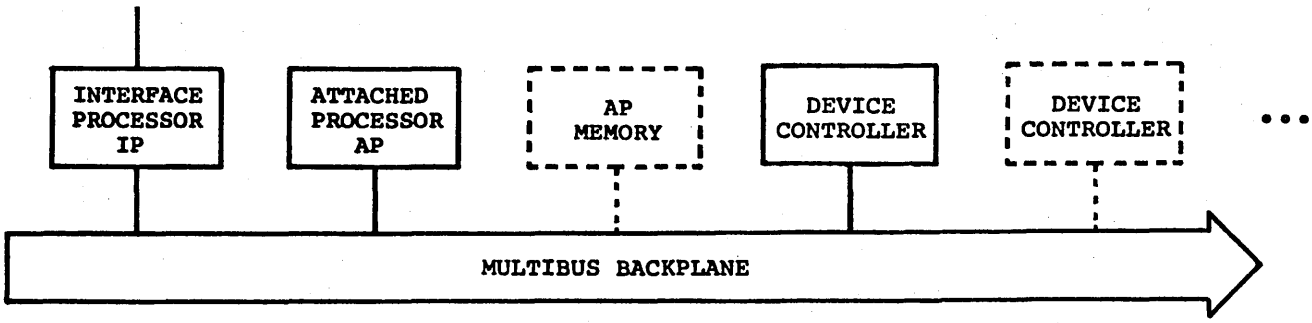


Figure 1-4. Peripheral Subsystem

The Peripheral Subsystem is implemented by the Attached Processor, Interface Processor, and Interface Processor Link boards. One IP and one IPL is necessary for each AP in a system. Each Multibus backplane requires one AP and one IP board. The AP and IP reside on a Multibus backplane, and the IPL board on the System Bus backplane.

The Attached Processor manages all peripheral device functions. In general, it coordinates the activity of multiple input/output processes, supports data transfers, and reacts to real-time concerns of the peripheral device controllers. The AP may also function as an additional decentralized data processor. All AP accesses to the System 432/600 main memory are via the Interface Processor chip (43203 VLSI component) on the IP board.

A primary function of the Interface Procesor is to map a portion of the AP's address space through protected windows into the system's main memory. This allows the AP to exploit the object-oriented addressing feature of the iAPX 432 architecture. The IP acts as a slave to the AP, and extends the AP instruction set to include some 432 object oriented instructions. This allows the AP to perform data manipulations within the Central System. The IP board also contains specific hardware to support system diagnostic software which executes on the AP.

CARD CAGES

Three card cages are offered for use with System Bus and Multibus backplanes: 6-slot, 12-slot and 18-slot. System 432/600 backplanes have card connectors on 0.70 inch centers. An 18-slot card cage will accept any mix of backplanes that support a total of 18 boards (e.g., a 12-slot System Bus backplane and a 6-slot Multibus backplane). Card cages do not contain power supplies or cooling fans.

POWERED AND COOLED CHASSIS

A complete powered and cooled chassis is available which includes an 18-slot card cage. Smaller card cages may also be mounted in the chassis in place of the 18-slot card cage. The chassis may be a table-top unit or be RETMA rack-mounted. A microcomputer-controlled system interface board and an operator switch and light panel is included in the chassis. The chassis power supply provides all necessary voltages and control signals for any combination of System Bus and/or Multibus backplanes containing a maximum of 18 logic boards. Two chassis models are available: one for 120 VAC/60 Hz and the other for 230 VAC/50 Hz.

Figure 1-5. iSBC 432/630 Chassis

DIAGNOSTIC SOFTWARE

The System 432/600 Diagnostic Software package is available for System 432/600 users. It is described in the System 432/600 Diagnostic Software User's Guide. All access and data paths, all memory locations, and representative processor instructions are exercised by a series of structured test programs.

The normal sequence of testing is a series of tests starting on the IP board and progressing through the IPL, MC, and SA boards, and finally to the GDP boards. The diagnostic software has been designed to test System 432/600 configurations within the following range:

MINIMUM
One each of the five board types: GDP, IP, IPL, MC, and SA.

MAXIMUM
Five GDP boards, one IP board, one IPL board, one MC board, and 16 SA boards.

If more than one Peripheral Subsystem is available, the diagnostics may be run on any or all of the APs.

One section of the Diagnostic Software package is the System Validator, which gives a quick confidence check of the System 432/600. The validator is a subset of the Diagnostic Software package. It is a minimal functional test of the entire system, and runs in a much shorter time than the full system diagnostics.

SAMPLE CONFIGURATIONS

Figure 1-6 depicts the modularity and expansion capabilities of System 432/600 modules. Sample configurations for entry level, medium, and large systems are shown. System configuration and expansion limits are set by the backplane size and types selected.

Figure 1-6A is an entry level system for a 12-slot card cage with one 6-slot System Bus backplane and one 6-slot Multibus backplane. The Memory Subsystem consists of one MC board and one SA board in a non-interleaved system, or one MC and two SA boards in an interleaved system. One GDP board and one IPL board complete the System Bus population. The Multibus backplane contains one IP board, one AP board, and one device controller board. The AP and device controller boards are selected by the user.

The memory size for the entry level system described above is 256K bytes for the non-interleaved version, or 512K bytes for the interleaved version. The non-interleaved version can be expanded to 512K bytes by adding a second SA board.

This entry level system can also be expanded by plugging one additional GDP board into the remaining System Bus slot. No software changes are needed to utilize the additional GDP board - simply plug it in. The Peripheral Subsystem may be expanded by inserting up to three additional boards (either user-selected device controllers or AP memory) in the Multibus backplane.

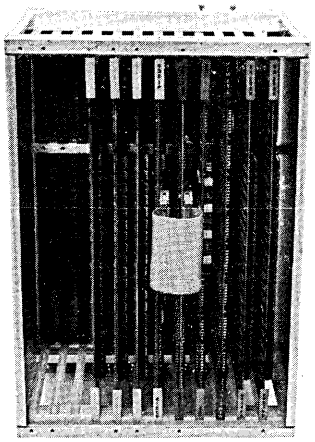
Figure 1-6B shows two possible configurations for a medium system utilizing an 18-slot card cage. System B-1 increases processing power, while System B-2 extends input/output capabilities. System B-1 provides over 1.5 million bytes of main system memory, four General Data Processors, and a complete Peripheral Subsystem in one unit. Four GDPs, with their inherent multitasking and concurrent execution capabilities, provide an extremely powerful processing subsystem.

System B-2 provides 512K bytes of main system memory and two complete Peripheral Subsystems in one small package.

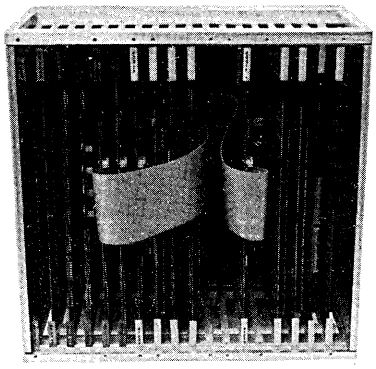
Since the ProcLink cable provides all interconnections between Peripheral Subsystems and the 432/600 Central System, a large multiple-chassis system may be configured easily, as shown in Figure 1-6C.

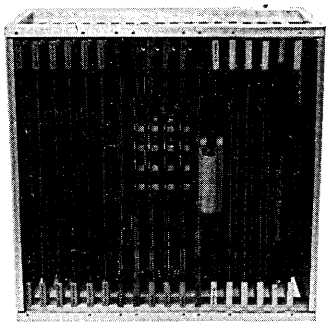
Using an 18-slot System Bus backplane, this system provides a main memory capacity of over 2.5 million bytes, the processing power of four GDP boards, and two complete, powerful Peripheral Subsystems. One option to this system is to exchange one GDP board with an IPL board, and configure the peripheral card cage with three 6-slot Multibus backplanes. With three GDP boards, this configuration still provides a powerful data processing capability, plus maximum main memory and three autonomous Peripheral Subsystems.

More details of system configuration may be found in Chapter 2, Configuration and Physical Characteristics.

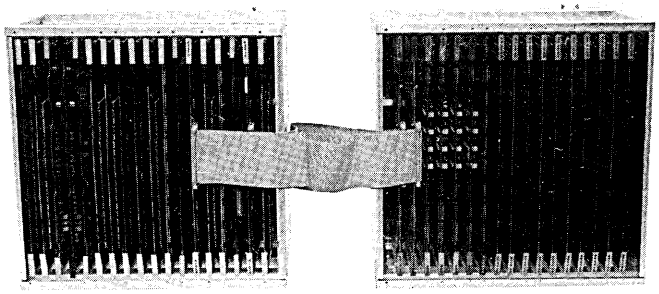


A Entry Level System





B Two Medium Systems



C Large Two Card Cage System

Figure 1-6. System 432/600 Sample Configurations

CHAPTER 2
PHYSICAL CHARACTERISTICS AND CONFIGURATION

INTRODUCTION

This chapter introduces System 432/600 module functions and extensibility, and physical characteristics of the hardware including power and cooling requirements. It provides pointers on configuration criteria for typical small, medium, and large configurations.

MODULE FUNCTION AND EXTENSIBILITY

Intel's System 432/600 product line is a family of functional modules that provide expansible subsystem building blocks easily configured into an extensive range of computer systems. The product line includes PC boards, backplanes, cables, card cages, and a powered and cooled chassis which are offered individually or as integrated 32-bit OEM computer systems.

An early procedure in a configuration exercise is to divide the computer system into its constituent subsystems: Processor, Memory, and Peripheral. Each subsystem in the System 432/600 product family is an independent, decentralized entity. The function of each subsystem is distributed over a number of independent boards, which allows an incremental approach to selecting subsystem modules for a particular range of performance.

Processors in a System 432/600 are either a General Data Processor (GDP) or Interface Processor (IP). At least one GDP is necessary to provide data processing capability; one IP is necessary to implement each Peripheral Subsystem interface. An Interface Processor Link (IPL) board is necessary to interface the System Bus backplane to each IP board and its associated Multibus backplane. A Processor Link (ProcLink) cable connects the IPL and IP boards.

The number of processors in a system may vary from two to six. The optional four processors may be any mix of General Data Processors and Interface Processors. For processing intensive applications, adding GDP boards will improve system throughput. No electrical or software considerations are necessary when adding GDP boards to a system.

All peripheral device functions are controlled and coordinated by a user-selected Attached Processor (AP). Peripheral capabilities may be expanded by adding any Multibus-compatible controller or Multimodule board. This allows Peripheral Subsystems to be configured to provide mass storage, DMA functions, data communications, and analog/digital device control, by simply adding boards to the Multibus backplane.

The System 432/600 architecture allows adding complete Peripheral Subsystems (additional Multibus backplanes and logic boards) for further input/output enhancement. A maximum of five Multibus backplanes may be configured in one System 432/600 to provide five complete, independent Peripheral Subsystems in a single shared-memory computer system.

The amount of memory in a System 432/600 depends on the number of SA boards installed. The logical addressing capability permits 16 SA boards. Thus, assuming a System Bus backplane with 16 SA board slots, a System 432/600 could be configured with memory sizes ranging from 256K bytes to 4M bytes. The largest System Bus backplane currently offered by Intel, however, is the 18-slot backplane which provides 10 slots for SA boards. This backplane permits a maximum main memory size of 2.5M bytes of ECC-protected RAM memory.

A memory interleave option is available to enhance system performance. This option uses two identical banks of memory with alternate addresses to allow overlapping operations for faster data access.

Only one MC board is used in any system, regardless of the number of SA boards in the system.

BACKPLANES

Two types of backplanes are available for System 432/600 modules: System Bus and Multibus. System bus backplanes come in 6-, 12-, and 18-slot sizes. Multibus backplanes come in 6-slot and 12-slot sizes. System Bus and Multibus backplanes of a given size (e.g., 6-slot backplanes) have the same form factor to ensure mechanical compatibility, regardless of the configuration of a particular system. System 432/600 backplanes are four layer boards with internal ground and power planes, and with ground shields between signal lines to provide controlled line impedance. All backplane signal lines are terminated.

Note that two or more backplanes do not connect together to form one larger backplane; each of the five backplanes is an independent unit.

System Bus backplanes accept and interconnect the System 432/600 Memory Controller, Storage Array, General Data Processor, and Interface Processor Link boards. Each System Bus backplane has one dedicated slot for the Memory Controller board. The seventh processor slot of the 18-slot backplane is reserved. System Bus slot allocations are shown in Table 2-1.

A System Bus backplane requires connection only to +5 volts and ground. Two 5/16-inch diameter holes are provided in the backplane to accept bolt-on power lugs.

Table 2-1. System Bus Slot Allocations

System Bus Backplane Size	Processor Slots (IPL or GDP)	Memory Controller	Storage Array Slots
6 Entry Level	3	1	2
12 Medium	5	1	6
18 Large	6	1	10

Figure 2-1 shows dimensions and mounting holes of the System Bus backplane.

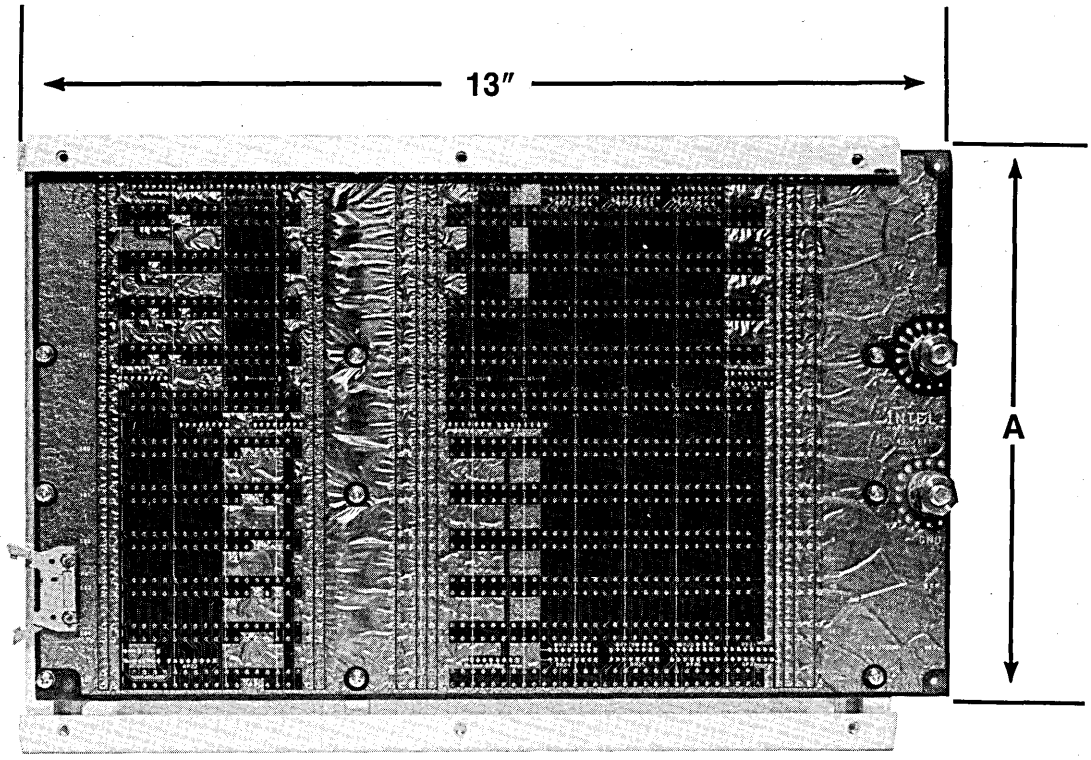


Figure 2-1. System Bus Backplane

System 432/600 Multibus backplanes accept and interconnect the Interface Processor board, Attached Processor board, and standard Multibus device controllers. The Multibus backplanes (6-slot iSBC 432/615 and 12-slot iSBC 432/616) are compatible with the card spacing, mounting dimensions, and power distribution of the System Bus backplane; either may be mounted in any position of a card cage.

An IP board may occupy any position on the Multibus backplane. For mechanical reasons, P2 of the two outside board positions is not available for external connection. If a Multimodule board is added to a PC board, the combined board thickness will require two adjacent Multibus slot positions. The AP usually occupies the end two slots next to the System Bus and IPL boards. Dimensions for Multibus backplanes are shown in Figure 2-2.

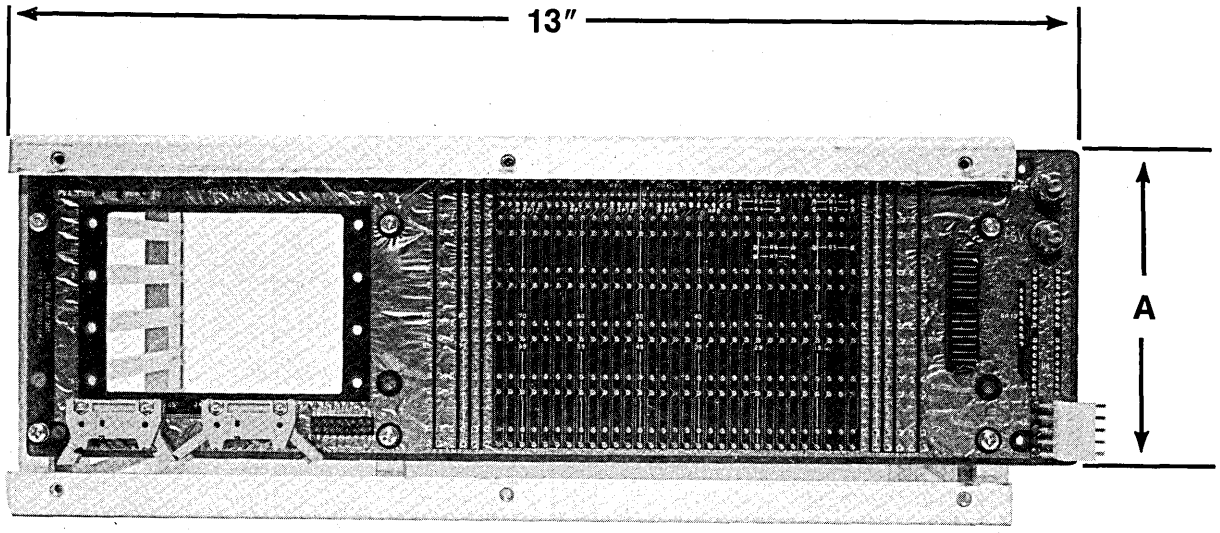


Figure 2-2. Multibus Backplane

LOGIC BOARDS

The five types of logic boards in the System 432/600 set are:

General Data Processor board ..... GDP

Interface Processor board ..... IP

Interface Processor Link board ..... IPL

Memory Control board ..... MC

Storage Array board ..... SA

The following additional board is necessary to complete a System 432/600 configuration:

Attached Processor board ..... AP

An example is the Intel System 432/670 Integrated Computer System, which uses an iSBC 86/12A as the Attached Processor.

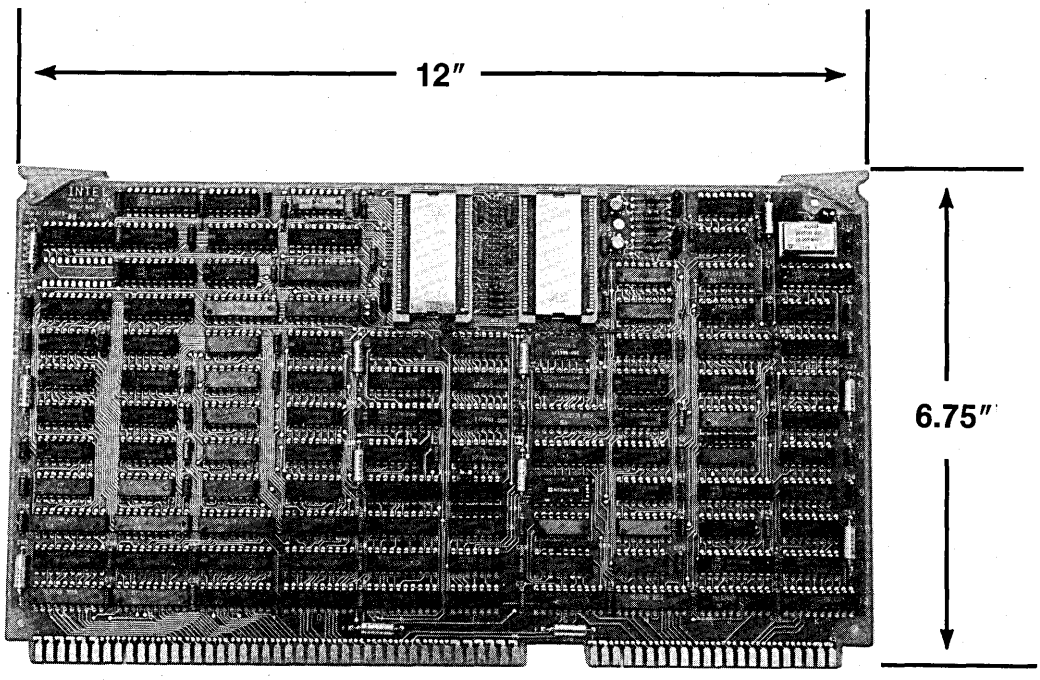


Figure 2-3. PC Board Form Factor

Key slots are cut in each System 432/600 board connector to correspond to physical position areas on the System Bus backplane, preventing boards from being installed incorrectly. Slots are cut between pins on both P1 and P2 connectors, as shown in Table 2-2.

Table 2-2. PC Board Key Slots

PCB	P1 between pins	P2 between pins
GDP	15-17	5-7
IPL	15-17	5-7
MC	29-31	13-15
SA	71-73	37-39

Clock generators reside on IP, GDP, and MC boards. The MC clock synchronizes all System Bus transfers and Storage Array transfers. The GDP clock synchronizes functions on the GDP board itself. The IP clock synchronizes functions on the IP board, and all data transfers between the IP board and the IPL board. Since each processor has its own clock, processor boards may function at different clock rates. The IP clock rate is determined during configuration as a result of ProcLink cable length.

LOGIC BOARD JUMPERS

The Memory Controller board and the Interface Processor board require jumpers to set configuration options. One jumper on the MC board is used to select interleaved or non-interleaved memory operation of all Storage Array board slots on the System Bus backplane.

Jumpers on the IP board are used to select:

1. 16 IP window page addresses out of the possible 64K pages of Multibus memory address space
2. The I/O base port address
3. One of eight interrupt lines to be used by the IP interrupt
4. One Multibus driver is jumpered ON or OFF so the IP initializes the Multibus system or simply generates an interrupt

PROCLINK CABLES

If IP/IPL board-pairs are completely enclosed in a metal cabinet, ribbon type ProcLink cables are used. If a connection outside of a cabinet is necessary (e.g., connecting boards in two separate cabinets) the shielded ProcLink cable is necessary to prevent interference problems. The additional line capacitance of shielded cable affects data transfer rates, and leads to length restrictions or lowering the IP clock rate.

A typical ProcLink configuration is a 20-inch ribbon cable (board to rear connector plate), 10-foot shielded cable (chassis to chassis), and another 20-inch ribbon cable as shown in Figure 2-4. A 36-inch external cable with two 20-inch internal cables is the maximum length usable with an 8 MHz IP clock rate. If the external cable length is increased, the IP clock rate must be set to 5 MHz. Table 2-3 is a matrix of cable types, lengths, and clock rates for different internal and external combinations.

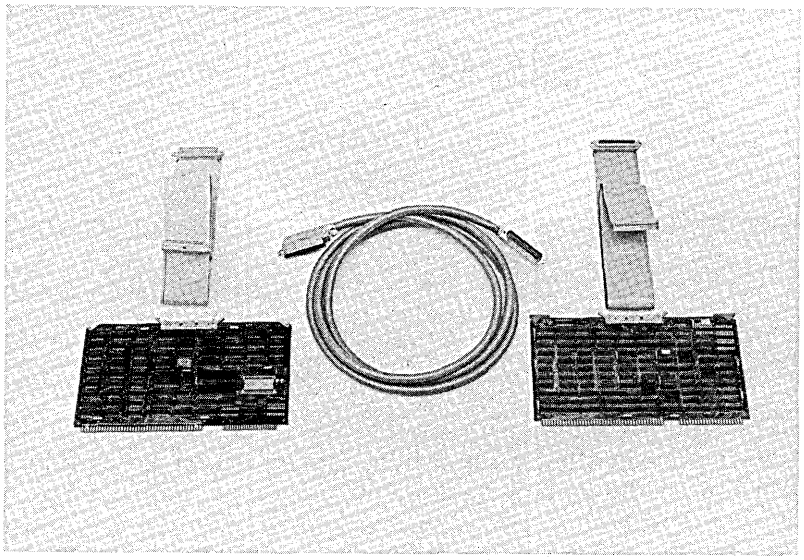


Figure 2-4. External ProcLink

Table 2-3. ProcLink Cables

INTERNAL		EXTERNAL	
Length	IP Clock	Length	IP Clock
20"	8 MHz	36"	*8 MHz
72"	8 MHz	72"	5 MHz
120"	8 MHz	120"	5 MHz

* The 36-inch external cable connected between two 20-inch internal cables may be operated with an 8 MHz clock. Any increase in either internal or external cable length would require the lower 5 MHz clock rate.

POWER AND COOLING

Power and cooling requirements for System 432/600 PC boards are given in Table 2-4 at the maximum DC voltage of +5.0V plus 5.0%.

Table 2-4. Power and Cooling

BOARD	Max Amps @ +5.25 volts	Cooling
GDP	7.0	
IP	5.5	300 LFPM or 10 cfm per board
IPL	6.5	at 0 to 40 degrees C.
MC	6.5	
SA	7.0	

CARD CAGES

Three card cages are available, in 6-, 12-, and 18-slot sizes. Card cages do not contain power supplies or cooling fans. Mounting holes in the bottom of the large card cages will accept 6-, 12-, or 18-slot backplanes. Holes in the side rails contain nylon card guides, and are on 0.7 inch centers to match backplane connector spacing.

Since mounting dimensions are standard on iSBC 432/610, 432/611, and 432/612 System Bus and iSBC 432/615 and 432/616 Multibus backplanes, they may be mounted in any position in a larger card cage to allow maximum configuration freedom. Card cage configurations are shown in Figure 2-5.

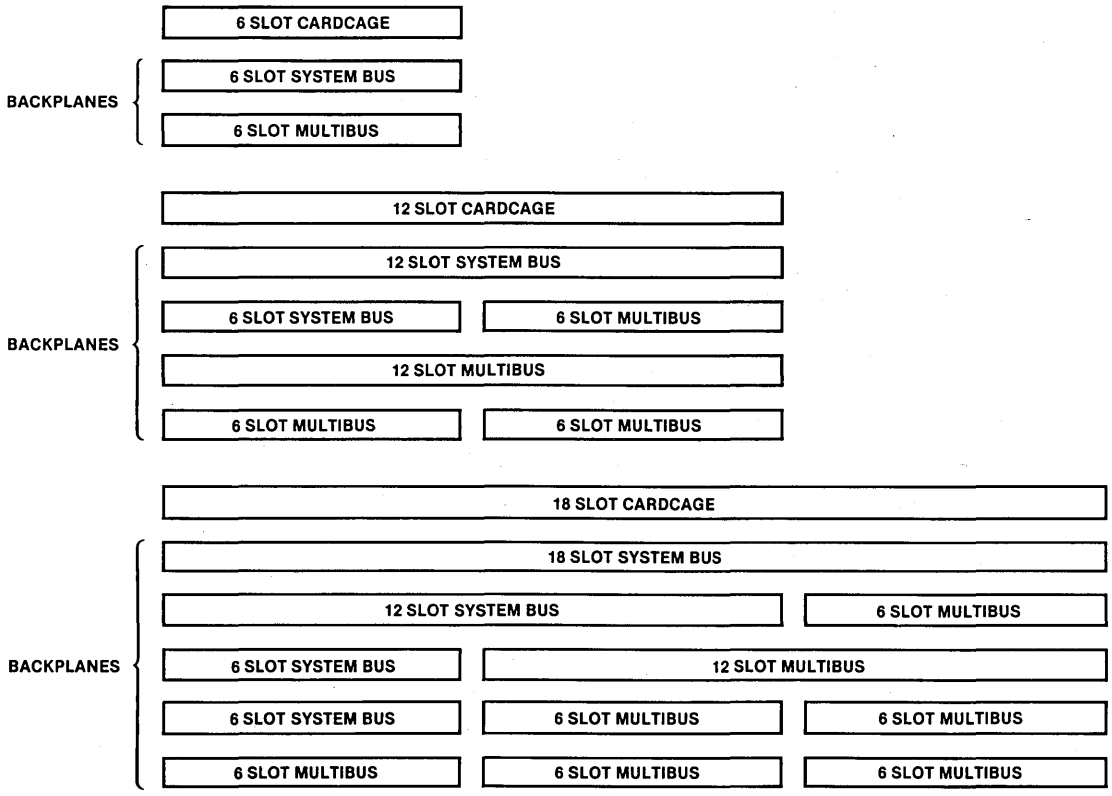


Figure 2-5. Suggested Card Cage and Backplane Combinations

More than one card cage may be used in a single system, and card cage sizes may be intermixed in a system.

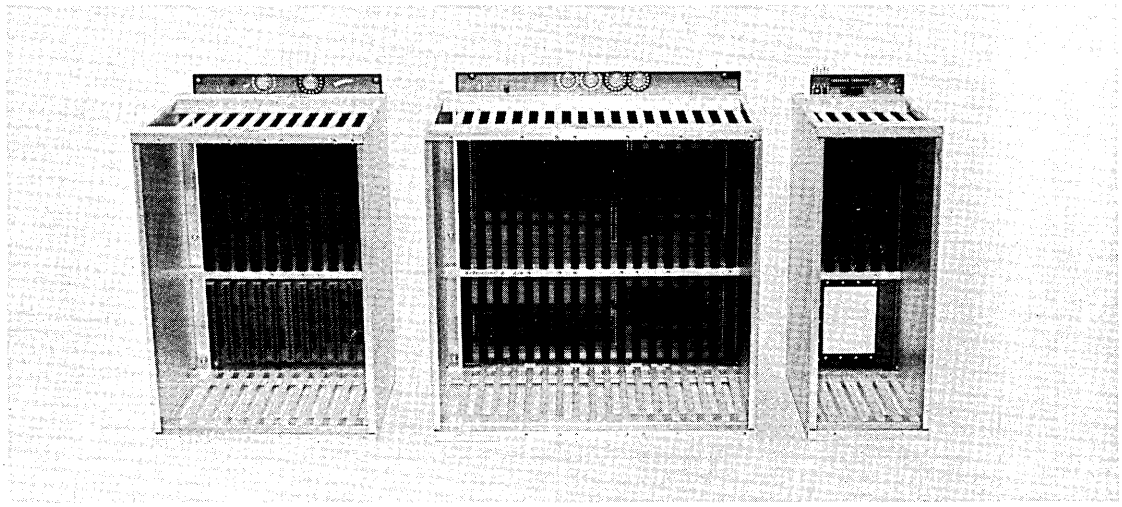


Figure 2-6. Card Cages

POWERED AND COOLED CHASSIS

The iSBC 432/630 chassis is a versatile and compact enclosure for System 432/600 modules. It powers and supports any combination of up to 18 System Bus and/or Multibus PC boards, and provides a microcomputer-controlled Switch and Light panel interface for operator use.

The chassis is approximately 12 inches high, 17 inches wide and 22 inches deep. In this discussion, right and left are determined by looking at the front of the chassis.

This universally-styled package may be used as a table top unit or be RETMA rack-mounted. Two AC source power options are available. The iSBC 432/630 uses 120 VAC/60 Hz line power; the iSBC 432/631 operates from 230 VAC/50 Hz.

Figure 2-7 shows the iSBC 432/630 chassis.

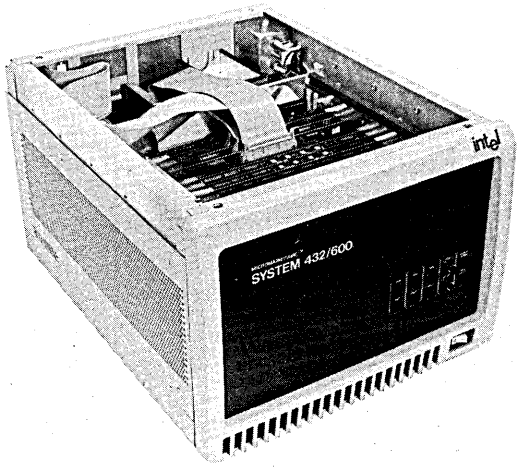


Figure 2-7. iSBC 432/630 Chassis with the System 432/670 Configuration

Modules constituting an iSBC 432/630 chassis are:

- a rigid aluminum support frame
- an 18-slot card cage
- three cooling fans for logic boards in the card cage
- a 750 watt 4-level switching power supply (+5, -5, +12, and -12 volts)
- an AC circuit breaker ON/OFF switch and AC line filter
- a programmable operator's switch and light panel on the front of the chassis
- removable external connector plates on the rear panel
- metal cover panels on the frame that provide EMI/ESD shielding

The microcomputer-controlled Switch and Light (SL) logic board associated with the operator's panel provides support for up to four subsystems, and remote control capability. The control component for the board is an Intel 8748 MCS 48 microcomputer. The 8748 has a user-programmable and erasable EPROM program memory. Jumpers on the board select the 4-bit address for the 8748. These may be wired to a remote cable to allow remote selection of the unit, if desired. The remote interface is an RS-232C serial data communication port that transfers command and status information to and from the board.

Figure 2-8 shows the operator's panel.

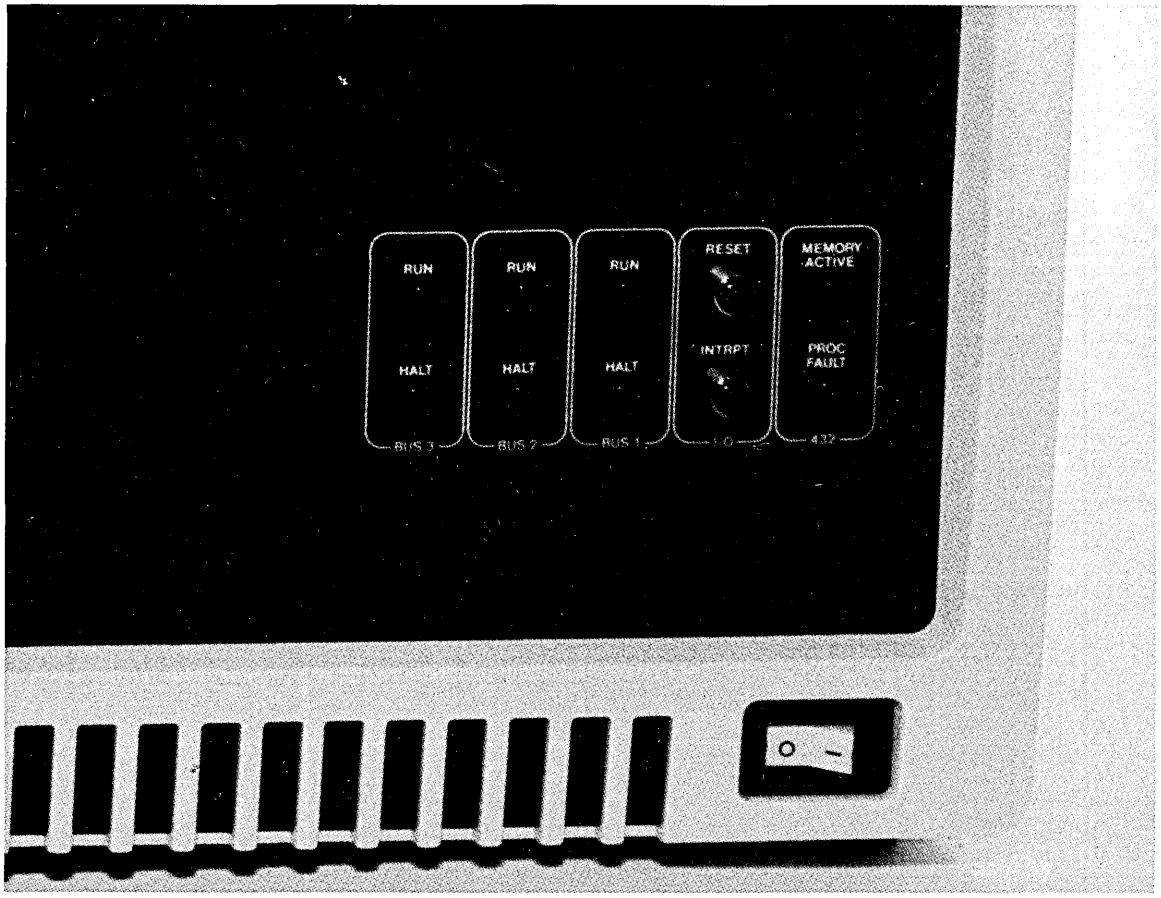


Figure 2-8. Operator's Panel

In configurations with more than one Peripheral Subsystem (more than one Multibus backplane), the Attached Processor in one Peripheral Subsystem must be designated as the controlling AP. The controlling AP is connected to Port 2 of the SL board, from which it receives reset, interrupt, and power fail signals.

Operator switches and indicators are on the SL board which is mounted on the front of the chassis. Holes in the front panel of the chassis allow the lights and switches to protrude for operator indication and access. Status indicators show MEMORY ACTIVE and PROCESSOR FAULT conditions for a System 432/600 Central System, and RUN or HALT conditions for one, two, or three Peripheral Subsystems. Switches allow resetting or interrupting the controlling Attached Processor via firmware in the 8748 microcomputer.

Power fail logic on the SL board monitors both AC and DC valid conditions. If the DC valid condition fails, the SL board sends a Reset signal to the Central System and all three Peripheral Subsystems. If the AC valid condition fails, the Multibus Power Fail signal (PFIN) is asserted for 5 MS, then an initiate signal (INIT) will be sent to the controlling Attached Processor of the system.

Six cable connectors are located on the SL board:

1. Port 1, System 432/600 Central System (System Bus backplane)
2. Port 2, Peripheral Subsystem (Multibus backplane)
3. Port 3, Peripheral Subsystem (Multibus backplane)
4. Port 4, Peripheral Subsystem (Multibus backplane)
5. AC/DC power sense for power fail reset/interrupt control
6. RS-232C Remote Port

Flexibility in backplane selection for the card cage provides a wide range of system configurations within the chassis. System Bus backplane selections are 6-, 12-, and 18-slot, with 6- or 12-slot Multibus backplanes available. Within the 18-slot size limit, any backplane type, size or position mix may be selected for the card cage.

Three cooling fans on the left side of the chassis blow room air across the logic boards. System logic boards and the chassis are designed to operate through an ambient temperature range of 0 degrees to 40 degrees Celsius.

The power supply is a regulated, protected switching type that provides four voltages: +5, -5, +12, and -12 volts. Maximum combined power output of the supply is 750 watts. This is sufficient for any combination of System Bus and/or Multibus backplanes and 18 logic boards. The power supply has its own internal cooling fan.

A series AC line filter reduces the effect of line noise on system logic boards, and reduces external radiation by the chassis. There are three cable connector cut-outs in the rear panel of the chassis. The cut-out covers may be removed, installed with bulkhead connectors, and replaced on the rear panel. This provides a simple means of connecting cable shields to chassis ground, and retains the EMI/ESD shielding integrity of the chassis. Because of the shielding and line filter, the iSBC 432/630 chassis surpasses the FCC standard for conductive radiated noise.

CONFIGURING A SYSTEM 432/600

Configuring a System 432/600 is a simple process of selecting building blocks for each subsystem in turn. No effort is necessary to forge the subsystems into a complete functional system; that is automatic as a result of the System 432/600 architecture. Configuring a System 432/600 is a four-step process of determining and selecting:

1. Memory size, Interleave option, and future expansion needs
2. Processing needs
3. Input/Output needs
4. Backplanes, ProcLink cables, card cages, and power requirements

Pointers on configuration criteria are given in the above order.

The largest System Bus backplane offered by Intel contains six slots for processor boards, one Memory Controller board slot, and slots for 10 SA boards.

MEMORY SUBSYSTEM CONFIGURATION

Four items should be considered in configuring a Memory Subsystem:

1. Memory size
2. Interleave or non-interleave option
3. Future expansion

MEMORY SIZE

The first consideration in determining memory size is the operating system to be used and the amount of memory it requires. Other system software such as compilers and basic utilities must also be considered, as must the space required for application programs. Input/Output needs must also be included, although these needs are minimal in Central System memory since the Attached Processor uses AP memory in the Peripheral Subsystem as it performs real-time device control and input/output management.

When the needed memory size is known, the number of SA boards can be calculated. Each SA board contains 256K bytes.

Although the Memory Controller can logically address 16 SA boards, the 18-slot System Bus backplane contains a maximum of 10 SA boards. Thus, the maximum memory size currently offered on a System 432/600 is 2.5M bytes.

The physical address of an SA board is established simply by its slot position in the System Bus backplane. There are no operational jumpers on an SA board and no changeable PROMs. The expansion increments in memory size depend only on interleaved or non-interleaved operation. Table 2-5 shows the minimum and maximum memory sizes and the memory expansion increments.

INTERLEAVE OPTION

Only one Memory Controller board is necessary in any system, regardless of the number of Storage Array boards. One jumper exists on the MC board to select interleaved or non-interleaved operation. The interleave option will provide an approximate 10% increase in single GDP performance and a 25% to 30% increase in the system's multiprocessor performance range. If the interleave option is selected, Storage Array boards must be installed in pairs to provide for the alternate bank addressing used in interleaved operation.

To change an existing system from non-interleaved to interleaved operation, the MC board jumper must be changed and an even number of SA boards installed.

Table 2-5. System Memory Sizes

RAM Size	Minimum Memory Size	Maximum Memory Size	Expansion Increment
Interleaved 64K RAM	512K Bytes	2.5M Bytes	512K Bytes
Non-Interleaved 64K RAM	256K Bytes	2.5M Bytes	256K Bytes

FUTURE EXPANSION

The simplicity of System 432/600 memory size expansion should be kept in mind while configuring the Memory Subsystem, and when determining System Bus backplane and card cage size. If backplane slots are available, memory size may be expanded by simply plugging in additional SA boards. No change is necessary to systems or applications software when adding SA boards to a system.

PROCESSOR SUBSYSTEM CONFIGURATION

In a System 432/600, a "processor" is either a General Data Processor board or an Interface Processor board. An IP board physically resides on the Multibus backplane and is logically a slave to the AP. GDP and IPL boards reside on the System Bus backplane. Each IP board requires one Interface Processor Link board to complete the communications path from the System Bus backplane to the Multibus backplane. There are a maximum of six processor positions in a System Bus. There must be one GDP board and one IPL board. The remaining processor positions may contain any mix of GDP and IPL boards.

A System 432/600 will typically provide a four-times performance increase between the entry level system with one GDP board and non-interleaved memory, and the maximum system with five GDP boards and interleaved memory.

Ideally, the Memory Subsystem can support as many processors as it takes to consume 100% of the available memory bandwidth. This number varies with the application, depending on how often a typical GDP initiates a memory access. In a processing-intensive application, GDPs typically consume more time between memory access requests. In this case, adding GDP boards will improve system throughput. The memory bandwidth will always support at least three GDPs; if the instruction mix is at least moderately processing-intensive, the system throughput will increase when the fourth and fifth GDPs are added.

If slot positions are available in the System Bus backplane, GDPs may be added to an existing system by plugging in GDP boards. No changes are necessary to system or applications software.

Similarly, removing a GDP board from a multiprocessor system does not affect system software. Full system operation and capability is retained after removing a GDP board (e.g., because of a malfunction), with some reduction in system throughput.

GDP and IP boards are available with either a 5 MHz or 8 MHz clock rate. Processors operate asynchronously, and processor clock rates may be intermixed in a system.

PERIPHERAL SUBSYSTEM CONFIGURATION

Peripheral Subsystem modules reside in a System 432/600 Multibus backplane. In general, any Multibus-compatible module may be used in a System 432/600 Peripheral Subsystem. For a listing of typical Multibus modules available, refer to the Intel Systems Data Catalog.

A System 432/600 may contain from one to five Peripheral Subsystems. Each Peripheral Subsystem must contain one Interface Processor board and one Attached Processor board. Each IP board must have a ProcLink cable to connect it to its companion IPL board on the System Bus backplane. The cable type and length will limit the maximum ProcLink data rate, and thereby the IP clock rate. Refer to the PROCLINK CABLES paragraph for details.

Three general areas must be considered in configuring a System 432/600 Peripheral Subsystem: peripheral device functions, the Attached Processor, and the performance range.

PERIPHERAL DEVICE FUNCTIONS

The System 432/600 Diagnostic Software package requires a CRT and keyboard (or teletype), and one floppy disk unit to run the diagnostic package. Besides typical operator interface devices such as these, additional mass storage devices and communication units may be configured. When the peripheral device requirements have been defined, Multibus-compatible controller boards and Multimodule boards may be selected for those devices.

ATTACHED PROCESSOR

One Attached Processor is necessary in each Peripheral Subsystem of a System 432/600. Any Multibus-compatible computer may be used as the Attached Processor. The AP may be either an 8-bit or 16-bit device. The System 432/600 Diagnostic Software package was written for an iSBC 86/12A Attached Processor.

The Interface Processor chip on the IP board recognizes five "windows" in one specific 64K-byte page of Multibus system memory. This 64K-byte page is the AP's communication path to Central System memory. The base address of the specific page is selected by jumpers on the IP board.

The number and operating speed of peripheral devices selected will affect the choice of an AP. In a system with more than one Peripheral Subsystem, it is possible to use different types of Attached Processors, depending on the needs of the different Peripheral Subsystems.

When the AP has been selected, the AP operating system to be used and the necessary device control routines should be analyzed to determine AP memory requirements. Additional AP memory boards may be needed on the Multibus backplane.

PERIPHERAL SUBSYSTEM PERFORMANCE RANGE

Many applications will utilize both a large number of low speed devices and one or more high data-rate devices. In these instances, it may be desirable to configure more than one Peripheral Subsystem in a System 432/600.

The maximum number of Peripheral Subsystems in a System 432/600 is five. In an input/output intensive application, one or more subsystems may be devoted to low speed terminals, and one or more to high data-rate devices. These options should be considered when making the choice of the AP to be used.

Complete Peripheral Subsystems may be added to an existing system by adding an IPL board to the System Bus, and an additional Multibus backplane with IP, AP, and device controller boards. The only limitation is the number of empty processor slots in the System Bus backplane, since an IPL board is necessary for each Peripheral Subsystem in the configuration.

BACKPLANE SELECTION

When board requirements of a configuration have been determined, backplane type and size must be selected. Future growth and the simplicity of expansion of all three subsystems should be considered when selecting backplane sizes.

Each System Bus backplane contains one dedicated slot for a Memory Controller board. SA boards reside on one side of the Memory Controller; GDP and IPL boards reside on the other. System Bus backplanes are available in 6-, 12-, or 18-slot sizes. Table 2-6 shows the number of processor board slots and SA board slots in each backplane size.

Multibus backplanes are available in 6- or 12-slot sizes. For mechanical reasons, P2 of the outside slot positions is not available for connection on Multibus boards.

Table 2-6. System Bus Backplanes

Backplane Size	Processor slots	SA Slots
6 slot	3	2
12 slot	5	6
18 slot	6	10

CONFIGURATION SUMMARY

Decision steps in a configuration exercise are:

1. Memory size (consider future expansions)
2. Interleave versus non-interleave memory option
3. Number of General Data Processors (consider future expansions)
4. Number of Peripheral Subsystems (consider future expansions)
   A. Number of IP/IPL boards
   B. Number and type of Attached Processors
   C. Number and type of peripheral device controllers
   D. Number and type of AP memory boards
5. Type, length, and number of ProcLink cables
6. Type and size of backplanes
7. Size and number of card cages
8. Power supply and cooling requirements

CHAPTER 3
SYSTEM FUNCTIONAL DESCRIPTION

INTRODUCTION

This chapter provides a detailed functional description of overall system operation and each module's operation in the system. It describes the modularity and extensibility of memory, processor, and peripheral subsystems at a block diagram level.

GENERAL DESCRIPTION

The following discussion refers to Figure 3-1, System 432/600 Block Diagram. As shown in Figure 3-1, the system is divided into three separate subsystems: Memory, Processor, and Peripheral.

The user-selected Attached Processor coordinates the activity of all peripheral processes. It reacts to real-time concerns of peripheral devices and controllers, and supports input/output data transfers and operator control devices. The only human control and interface to the 432/600 Central System is via software running on the AP.

Any Multibus-compatible peripheral device controller or Multimodule board may be used with the Multibus backplane and controlled by software running on the AP.

All communication with System 432/600 memory and General Data Processors is through the Interface Processor board. In performing these functions, the IP is an intelligent adaptor or slave to the AP.

A major function of the iAPX 43203 Interface Processor chip is to map a portion of the AP memory address space into areas of 432/600 main memory. The IP chip does this by providing five "windows" into memory for AP use; a window is simply a range of sequential AP memory addresses. To communicate with 432/600 main memory, the AP simply reads or writes to the IP as it would to AP memory. The IP provides the same hardware protection of all data structures in 432 memory as GDPs provide. All memory mapping, fault detection, handling, and reporting functions are internal to the IP chip.

The physical communication path from the Multibus backplane to the System Bus backplane is via the ProcLink cable connected from the IP board to the Interface Processor Link board. Data transfer occurs two bytes at a time over 16 lines in the cable. A Block Mode 8-byte burst transfer is used to meet requirements of high-speed peripheral devices.

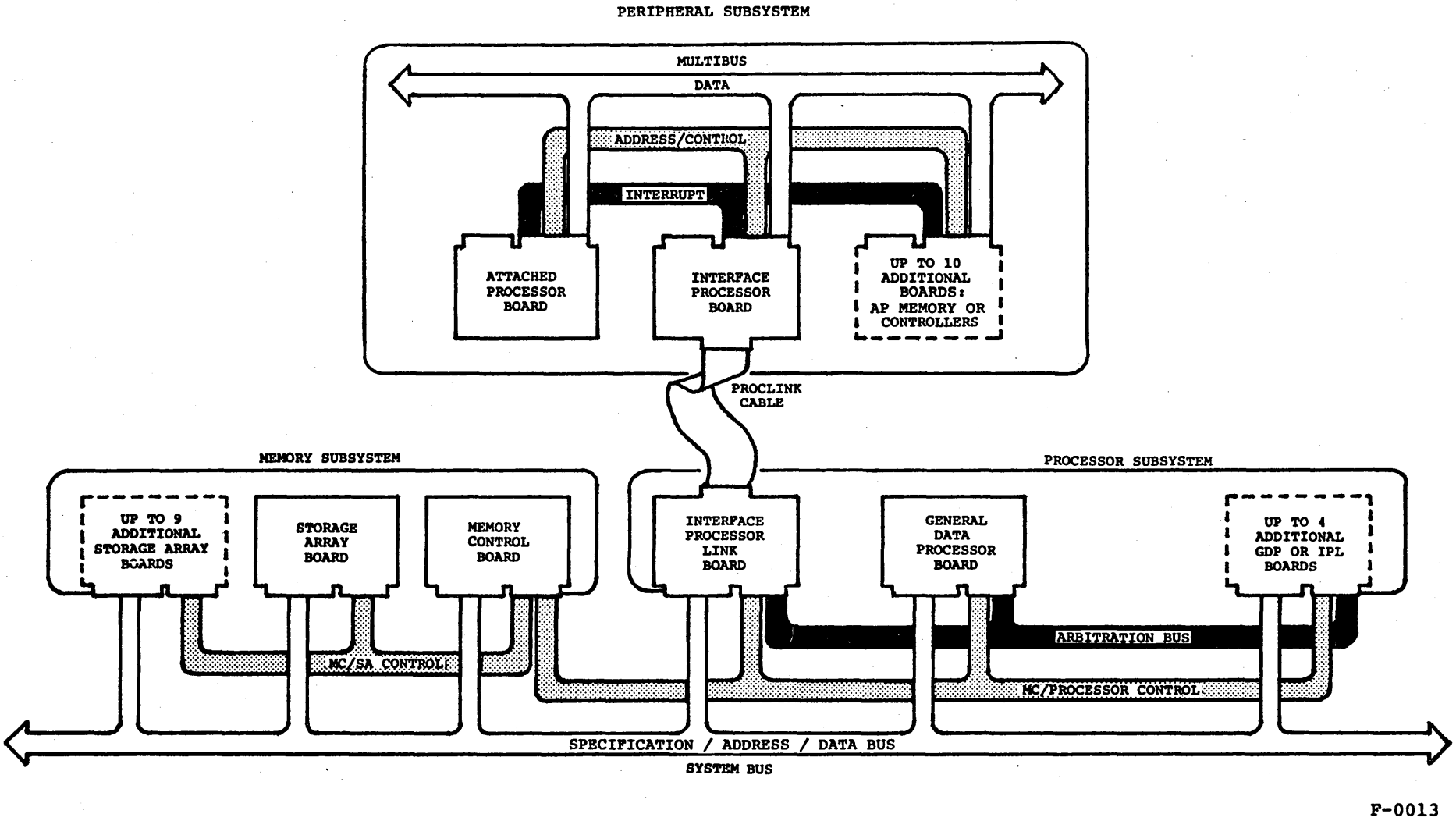


Figure 3-1. System 432/600 Block Diagram

The Memory Subsystem consists of one Memory Controller board and one to 16 Storage Array boards. Note, however, that the largest System Bus backplane currently offered by Intel supports a maximum of 10 SA boards. One common bus for access Specification, Address, and Data interconnects all PC boards on the System Bus. This SAD bus is 36-bits wide, four 8-bit bytes plus one parity bit for each byte. The System Bus provides one set of control/status lines from the Memory Controller to SA boards, and a separate set of control/status lines to General Data Processor and Interface Processor Link boards. A separate group of lines on the backplane are used by processor boards to arbitrate priority for the next memory access.

The Memory Controller performs 1-, 2-, 4-, 6-, 8-, and 10-byte accesses as requested by system processors. The byte address is accepted from a processor, mapped to the proper SA address format, and transferred to the SA board. The Memory Controller also supports local registers, local register accesses, and Interprocessor Communications (IPCs) for the system.

Storage Array boards store data in word organized 39-bit wide banks. Each four-byte (32-bit) data word is stored with a seven-bit Error Correction Code. This allows SA boards to detect and correct single bit errors, and detect double bit error conditions. Error condition information is stored in local registers on the MC board.

All processors (GDPs and IP/IPLs) use a common protocol for requests to the Memory Controller to access memory, system local registers, or perform IPC operations. The Memory Controller accepts these access requests and provides the appropriate response.

Each processor gets its identification number from its physical position in the backplane. The processor ID is used in IPC and self-dispatching procedures.

The processors use the Arbitration Bus on the backplane to determine which processor has the right to make the next memory access. The arbitration is under automatic hardware control, and is transparent to the number of processors in a system. Since the IP resides on the Multibus backplane, each IPL board contains arbitration logic for its companion IP.

INTERFACE PROCESSOR BOARD

Figure 3-2 shows a functional block diagram of the IP board. The blocks show the approximate location and physical area of components used for particular logical functions on the board.

MULTIBUS INTERFACE AND DIAGNOSTIC SUPPORT LOGIC

The Multibus block provides the standard Multibus address, data, control, and interrupt interface. IP board logic allows the use of either an 8-bit or 16-bit Attached Processor in a System 432/600.

Jumpers on the IP board allow selection of one of eight interrupt lines to be driven to the Multibus backplane and the AP.

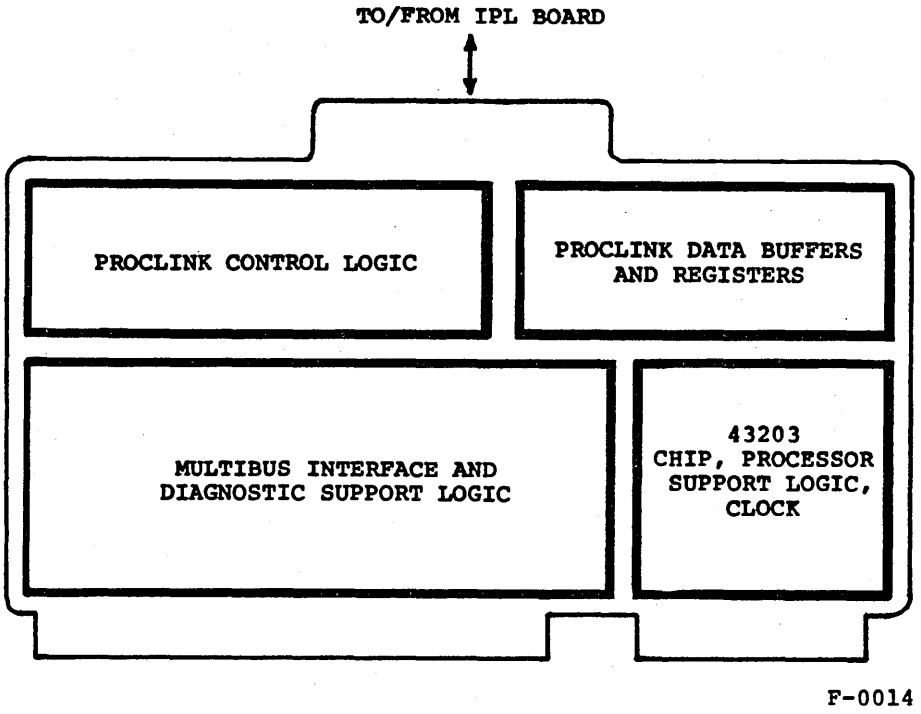


Figure 3-2. Interface Processor Board Block Diagram

Logic on the IP board provides 16 eight-bit I/O ports (registers) accessible to AP software. Nine of these are used; the others are duplicates or undefined. The base address of these ports is selected by jumpers on the IP board. Ports 0 and 1 are used for all data transfers between the AP and the 432/600 Central System during PASS mode in diagnostic operation. The remaining seven ports are used for initialization, control, and diagnostic functions for the System 432/600.

Central System communication with the AP is done through a 64K-byte "page" of AP memory. The IP board provides 16 possible base addresses, or 16 possible 64K-byte pages, for this purpose. One of the 16 possible pages is selected by jumpers on the IP board.

The IP recognizes five non-overlapping spaces or "windows" in the jumper-selected 64K-byte page of AP memory. Each window (via the IP chip) has its own address mapping function. The AP simply accesses its memory window space to transfer data to/from 432/600 main memory.

In Random Mapping Mode, each transfer is an independent 2-byte transfer across the ProcLink cable. By contrast, Block Mode provides a buffered 8-byte block transfer for high-speed peripheral devices. Windows 0, 2, and 3 open only to data segments in main memory, and Window 4 opens only to the Interface Processor Data Segment in main memory. Window 1 opens to data segments or interconnect space. Window uses are:

- 0 Window 0 may be set by software to Random Mapping Mode or Block Mode transfers. (Initialization forces Window 0 to open in Block Mode.)

- 1 Window 1 is always in Random Mapping Mode. Software may set Window 1 to access either 432/600 main memory or the Interconnect address space. In the System 432/600, Interconnect access space is used to access system local registers. (Initialization closes Windows 1, 2, and 3.)

- 2,3 Windows 2 and 3 may be used only for Random Mapping Mode.

- 4 Window 4 is the Context Control window, and always accesses the Interface Processor Data Segment. This window allows the AP to access the IP function request facility. The AP writes operands and operation codes into predefined locations of Window 4. The AP may alter window modes, utilize IPCs, and manipulate 432 system objects in this manner.

The preceding description relates to Logical Reference Mode operation of the IP chip. Initialization or an Enter Physical Reference Mode IPC to the Interface Processor will change its operational characteristics to Physical Reference Mode. In this mode, 24-bit addresses from the AP go directly to 432/600 main memory, with no IP address mapping function. Care should be exercised when using Physical Reference Mode, since automatic fault detection is not performed.

Initialization forces the IP chip into Physical Reference Mode with Windows 1, 2, and 3 closed, Window 0 open in Block Mode, and Window 4 open. Window 0 is normally used in Physical Reference Mode to establish an initial object table directory, objects, tables, and initial program instructions in main memory. Window 4 is normally used in Physical Reference Mode to load the proper Processor Object image for the Interface Processor. A "startup IPC" may then be issued to the IP or a GDP. The first IPC to the Interface Processor after initialization will cause it to change to Logical Reference Mode, where logical address mapping is performed and all accesses and mapping functions have automatic fault protection.

INTERFACE PROCESSOR CHIP, SUPPORT LOGIC, AND CLOCK

Window functions, logical and physical reference modes, data handling, checking, and mapping described previously are controlled by the IP chip. The IP chip checks for three classes of faults: context level, process level, and processor level. Refer to the iAPX 432 Interface Processor Architecture Reference Manual for details on IP chip functions. A fault condition may be detected while the IP is attempting to execute a function for the AP, or while moving data through a window. When a fault is detected, the IP records information about the fault in a fault information area, then interrupts the AP to inform it of the fault condition.

Clock generation on the board provides timing for IP board functions, the ProcLink interface, and the Interface Processor Link board. All transfers to and from the IPL board are synchronized by the IP clock.

The IP clock frequency may be 5 MHz or 8 MHz, depending on ProcLink cable configuration and length. An external ProcLink cable length of over 3 feet requires the lower IP clock rate.

The IP clock generator may be disabled by setting a control bit in diagnostic Port 4. In this PASS mode diagnostic state, one clock pulse is generated as a result of each Port 1 access by AP software. This allows the AP to "software-clock" commands and data transfers to the 432/600 Central System for diagnostic purposes. PASS mode software clocking is extensively used by System 432/600 Diagnostic Software during initial tests on each board; it may be used only by the diagnostics.

PROCLINK CONTROL AND DATA

ProcLink control logic provides functions for synchronous 16-bit transfers between the IP board and the IPL board. IP accesses consist of two-byte transfers in Random Mapping Mode, or eight-byte transfers in Block Mode.

Registers are used on the IP board to buffer these transfers. A parity bit is generated and added to each byte transferred to the IPL board; parity is checked on each byte received from the IPL board. An additional register set is used in diagnostic mode to turn data around at the ProcLink interface. This allows IP board logic to be checked by diagnostic software independent of ProcLink and IPL logic.

INTERFACE PROCESSOR LINK BOARD

The IPL board implements the interface between Central System modules on the System Bus backplane and Peripheral Subsystem modules on the Multibus backplane. The ProcLink cable connects to transmit/receive data buffers on the IPL and IP boards. The IPL board uses the IP clock for all ProcLink functions. The clock from the MC board is used for all System Bus communication with the IPL board.

Figure 3-3 is a block diagram of the IPL board.

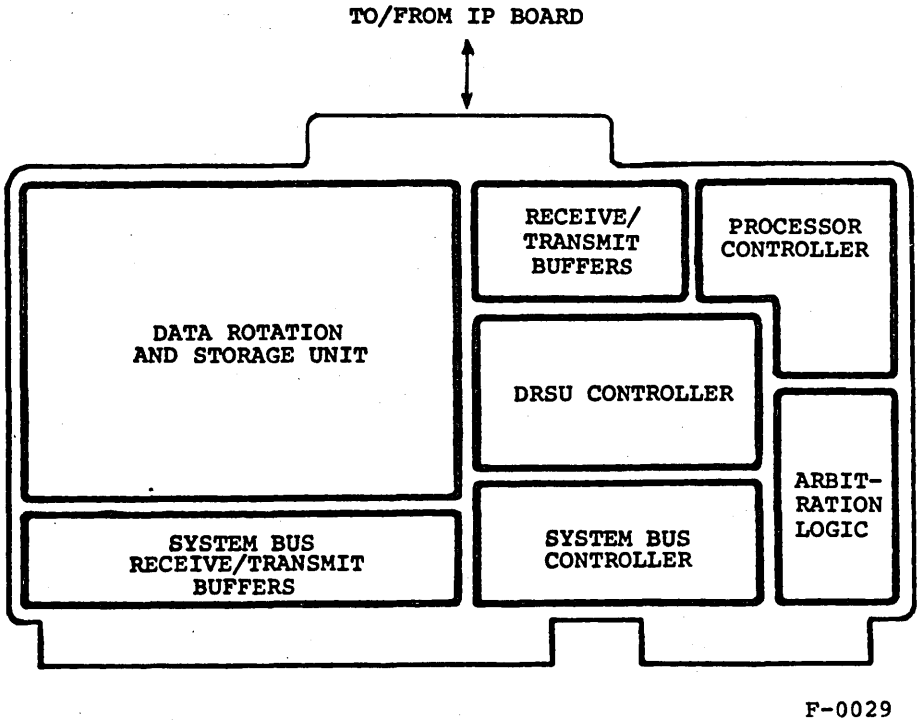


Figure 3-3. Interface Processor Link Board Block Diagram

DATA ROTATION AND STORAGE UNIT

The System 432/600 offers byte addressability. Storage Array boards in a System 432/600 are organized in 64K-byte banks of 32-bit words, four bytes per word. Each IPL and GDP board contains an identical Data Rotation and Storage Unit (DRSU). The DRSU aligns data into the proper byte position for transfer between GDPs or (either 8-bit or 16-bit) APs and System 432/600 main memory. The only DRSU difference in GDP and IPL boards is the additional ProcLink input/output logic to the DRSU on the IPL board.

All input/output addresses and data transferred to and from AP memory pass through the DRSU on the IPL board. Data entering the DRSU may be byte-rotated or shifted to any of the four positions of a word before being stored in the DRSU. The DRSU provides a four-word first-in-first-out (FIFO) buffered storage area. A DRSU normally contains an access specification byte, three address bytes, and up to 10 data bytes. For two-byte local register transfers, it will contain three address bytes, one specification byte, and two data bytes. (In a System 432/600, the "Move To Interconnect" and "Move From Interconnect" instructions refer to system local registers on the Memory Controller board.)

When less than a full four-byte word is transferred to memory, only the valid bytes are driven onto the SAD Bus from the DRSU. The memory word is read from the SA board, the new bytes are inserted, and the modified word is written back into memory with a new error correction code.

When data is going from the IPL to the IP, the lower two bytes of the DRSU output are gated to ProcLink buffers, transferred, then the upper two bytes of the DRSU word are gated out.

During diagnostic operation, in the IPL board's LOOPBACK mode, data is held in the DRSU instead of being transferred to main memory, and returned from the DRSU through the IP to the AP in place of memory data.

DRSU CONTROL

The DRSU controller is a PROM-based state machine that controls DRSU operation for both ProcLink and System Bus functions. Controller functions may be initiated by either the Processor Control state machine (IP clock) or the System Bus state machine (MC clock). The sequence of the state machine is determined by the content of the access specification register in DRSU control logic. The controller sequences the rotation for desired byte position in a word, gates it into the FIFO registers, and enables output gating to ProcLink or System Bus drivers.

PROCESSOR CONTROLLER

Logic components and PROM-based state machines are used to interface either the IP or the System Bus to the DRSU, perform all control signal handshaking between the modules, and initiate IPL board functions. The same PROM-based state machine is used on a GDP board.

In a processor state machine access cycle, the specification byte of the access specification word is held and translated to identify the type of access. The DRSU clock is enabled by the processor state machine for a time determined by the access length and type. If the access calls for a transfer to memory, the System Bus state machine is allowed to take control of board timing and the DRSU controller to drive necessary bytes onto the SAD Bus.

In the case of a Read operation, the processor state machine immediately requests the SAD Bus, and transfers control to the System Bus state machine. Byte positions are rotated, if necessary, before the word is stored in the DRSU. When the data is in the DRSU, the processor state machine takes control of the DRSU clock and sends the data to the Interface Processor via the ProcLink cable. The lower two bytes of the DRSU word are gated to the IP first, then the upper two bytes are gated to the IP via the "swap enable". Inputs to IPL board processor control logic are from the ProcLink cable and Processor/MC control lines on the System Bus.

ARBITRATION LOGIC

As shown in Figure 3-1, one group of System Bus lines is dedicated to GDP/IPL boards for memory access arbitration. Each processor uses its bus lines to arbitrate access rights. The arbitration logic is under control of a PROM-based state machine, and is identical on all processor boards. Each IPL board contains arbitration logic for its companion IP board on the Multibus backplane.

The number of processors in a system is transparent to the arbitration logic; boards may be added to or removed from the System Bus backplane without affecting arbitration. The bus uses a round-robin arbitration scheme so that no processor is subjected to memory starvation, but has an equal opportunity to access memory.

No physical "highest" priority line exists. When a processor's turn arrives, it asserts itself as Bus Master, and makes the next memory access. The next arbitration will place that processor in the lowest priority. Deassertion of Bus Master initiates another arbitration sequence.

SYSTEM BUS CONTROLLER

The system clock, requests and acknowledgements, and access commands are gated into the IPL board and out to the System Bus by the System Bus Controller. A PROM-based state machine is used to sequence and time bus functions on the IPL board.

The arbitration state machine will assert Bus Master when this board becomes the highest priority processor. Bus Master initiates an access cycle in the System Bus state machine. The deassertion of Bus Master causes the state machine to enable error logic to determine if a parity error was detected during the last bus cycle. Parity error conditions are recorded in the Processor Error local register on the MC board.

SYSTEM BUS BACKPLANE

The term SAD Bus refers to the 36-bit wide Specification, Address, and Data path common to all boards on the System Bus backplane. The SAD Bus carries four bytes plus one parity bit for each byte. Three other groups of lines are included in the System Bus backplane: Processor/MC Control, MC/SA Control, and the arbitration bus. Since SA board control lines are different from processor board (GDP/IPL) control lines, the MC board occupies one unique slot near the center of a System Bus.

All transfers on the System Bus are synchronous to minimize the effect of crosstalk and timing variations between components. Internal ground and power planes and ground shields between signal lines contribute to the reliability of the system. An 8 MHz clock on the Memory Controller board is used by all boards populating the System Bus to synchronize command and data transfers on the bus.

The SAD bus at any one time may contain either:

- four data bytes (plus parity bits) to or from GDP or IPL boards. (In the case of one, two, or three bytes driven from a DRSU, a four-byte word is read from the accessed memory location and the new bytes are added by the SA board.)
- a 24-bit address to the MC, with an 8-bit specification byte. The address could be to an SA board or to a local register. The MC will map the 24-bit logical address to the proper SA board address. The specification byte stipulates a memory or local register (interconnect) access, the number of bytes requested, Read or Write request, and normal or Read-Modify-Write operation.
- a mapped Storage Array address with byte drive select and access commands to an SA board.
- four data bytes (plus parity bits) to or from Storage Array boards.
- two bytes (plus parity bits) to or from system local registers on the MC board.

Other lines on the System Bus backplane provide:

- system clock
- IPC (Interprocessor Communication) commands
- processor status and ID information
- access timing and commands
- arbitration bus
- a reset command

GENERAL DATA PROCESSOR BOARD

The General Data Processor is the iAPX 43201 microinstruction decoder and sequencer, and its companion iAPX 43202 execution unit. The VLSI chips and their support logic are mounted on the GDP board. The GDP architecture provides hardware support for operating systems and high-level languages. Examples of such support are floating point instructions, an operand stack, and hardware-implemented fault detection and reporting.

System architecture makes the number of GDP boards in a system transparent to system software and arbitration. GDP boards may be added to or removed from a system with no change to system software. The only condition is physical slots must be available on the System Bus backplane to accommodate another GDP board. A GDP gets its identification number from etched lines in the backplane. The only way to change the ID of a particular GDP board is to change its slot position on the backplane.

Figure 3-4 is a General Data Processor board block diagram.

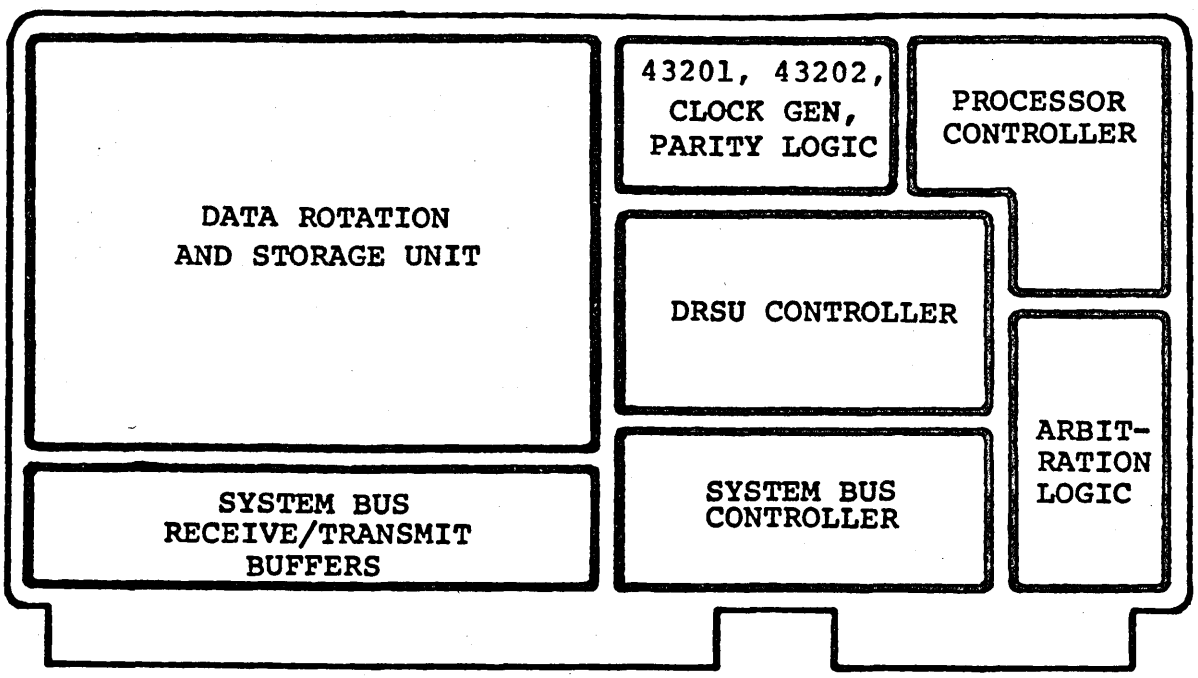


Figure 3-4. General Data Processor Board Block Diagram

For a full description of the iAPX 43201/43202 VLSI General Data Processor chip pair, refer to the iAPX 432 GDP Architecture Reference Manual. A System 432/600 GDP board provides support logic to fully utilize the capabilities of the GDP chips.

CLOCK LOGIC

The output of a crystal oscillator circuit on each GDP board is divided and shaped to provide clock pulses for the VLSI chips and all board logic synchronous to the GDP chips. GDP boards thus operate asynchronously to each other, which allows future enhanced boards to be used in a system by simply plugging them in.

SYSTEM BUS CONTROL AND BUFFERS

The 8 MHz system clock is received from the Memory Controller board, and buffered and gated to all board logic synchronous with the System Bus. System Bus control and transmit/receive buffers on a GDP board are the same as those on an IPL board.

"System Reset" from the controlling AP/IP will set the sleep condition on all GDP boards in the system. Sleep disables the System Bus state machine, so that nothing may be driven onto System Bus lines from a GDP board. This allows an AP to load main memory with objects, tables, instructions, etc. necessary to execute a program with no possible intervention by GDPs. It also isolates GDP boards from the remainder of the system for diagnostic purposes.

When a GDP receives its first IPC after initialization, it clears the sleep condition, then responds to the IPC command. This "startup" IPC is the means of beginning actual program execution on a System 432/600.

In addition to setting the sleep condition on a GDP board, the System Reset command should reset:

- arbitration state machine
- DRSU state machine
- processor state machine
- System Bus state machine

A clock is generated by the MC board, driven on a System Bus line, and used by processors in allotting a fixed time period for processes to run before dispatching another process.

DATA ROTATION AND STORAGE UNIT

The DRSU and its controls on a GDP board are identical to those on an IPL board. An IPL board has additional controls to connect the DRSU to the ProcLink buffers, but the DRSUs themselves are identical. This allows all DRSU state machine PROMs to have the same internal coding.

ARBITRATION LOGIC

Arbitration logic on a GDP board is identical to that on an IPL board.

PROCESSOR STATE MACHINE

The Processor State Machine on the GDP board is the same as the Processor State Machine on an IPL board. The only difference is in the DRSU output gating. On a GDP board the DRSU is interfaced to the GDP chip pair instead of the ProcLink interface on an IPL board.

MEMORY CONTROLLER BOARD

Figure 3-5 is a block diagram of the Memory Controller board.

CLOCK GENERATOR

A 16 MHz crystal oscillator is used on the MC board to generate all necessary system clocks. The oscillator output is divided into the following signals:

- an 8 MHz clock for synchronizing all System Bus transfers and MC logic.
- a 1 microsecond clock used by SA boards to determine when to initiate a refresh cycle.
- a 200 microsecond timeout for Read-Modify-Write operations.
- a clock for processor use in allotting process time periods. The gating provides one clock pulse every 128 microseconds.

SYSTEM BUS INTERFACE

The interface to the SAD bus is the same as that on GDP and IPL boards. All lines are buffered both in and out of the board, and parity is checked for all bytes transmitted or received on the SAD bus.

In addition to the SAD bus, the Memory Controller interfaces to two more bus line groups: Memory Controller to processor boards, and Memory Controller to Storage Array boards. The arbitration bus does not connect to the Memory Controller board. The MC plays no part in arbitration; it simply responds to the Access Request signal sent by the processor that has arbitrated for Bus Master.

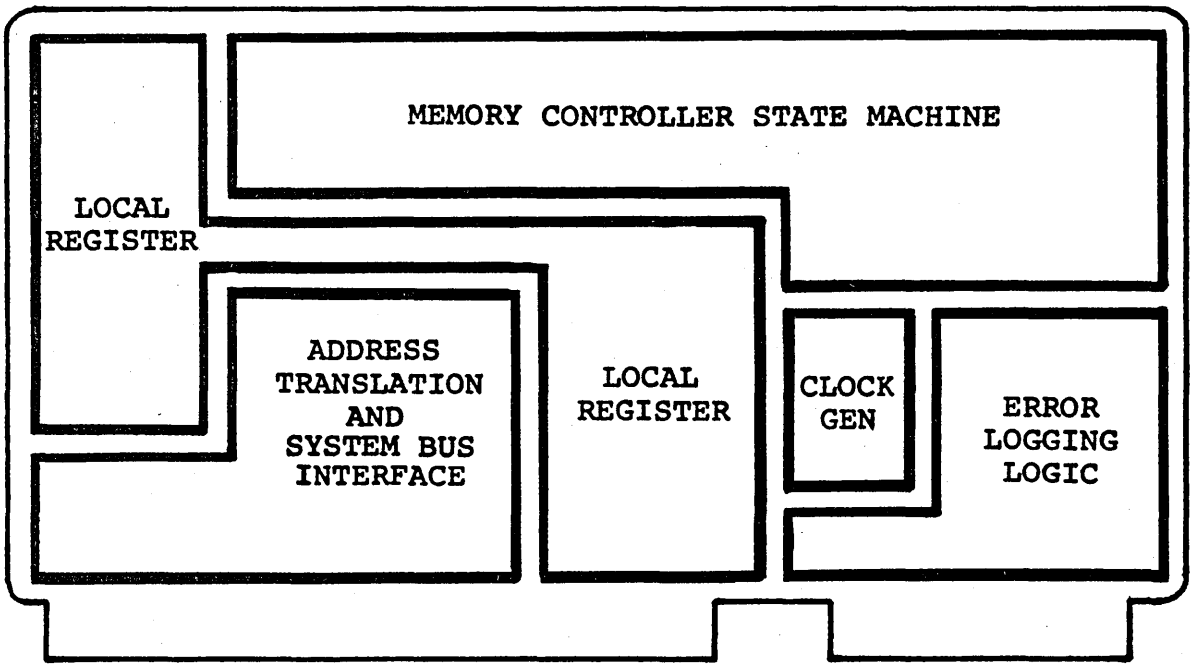


Figure 3-5. Memory Controller Board Block Diagram

MEMORY CONTROLLER STATE MACHINE

A PROM-based state machine and its associated logic control functions on the MC board. After a System Reset, the state machine waits for an Access Request from a processor to begin an access cycle.

Upon receiving Access Request, the MC latches and holds the Access Specification byte and the two low-order address bits for the complete access.

The specification byte defines the access as:

- memory or local register (interconnect space)
- Read or Write
- normal memory or Read-Modify-Write (RMW) access
- length (number of bytes) of access

The two low-order address bits define the byte boundary or beginning byte address of the access.

Translating the specification byte allows the state machine to branch to a particular microcode routine to handle each particular access.

In a memory access, the 24-bit address is loaded into address counter registers. When a processor request requires more than one memory access to satisfy the number of bytes requested, the address counters increment the address to complete the multiple access request. The counters are controlled by the MC state machine. The output of the address counters are gated to the address mapping PROMs.

The mapping PROMs select the proper storage module and bank select for the SA boards. Interleave option logic is integrated in the mapping process. Byte Drive Select is generated from the specification byte and the two low-order bits of the address sent by the requesting processor. Address and byte drive select are gated to SAD bus lines with an Access Array command to the SA boards to initiate the memory access.

A Read-Modify-Write (RMW) function is provided to protect areas of memory shared by processors. An RMW may specify a Read access or a Write access. When a processor initiates an RMW Read, the Memory Controller sets the RMW Lock condition which prevents another processor from initiating a new RMW operation. If an RMW Write does not follow the RMW Read in approximately 200 microseconds, the MC clears the RMW Lock and sets the RMW Timeout status condition in the System Error register.

LOCAL REGISTERS

In a local register Read access, the content of the addressed local register is gated through a parity generator and driven to the two low-order bytes of the SAD bus. At the same time, the Data Strobe signal line is activated to inform the requesting processor that valid data is on the SAD bus lines (the upper two bytes on the SAD bus are undefined during a local register access). For a local register Write, only the low-order byte from the SAD bus is gated to the addressed local register on the MC board.

ERROR LOGGING

Error detection and error logging are under the control of PROM-based state machines. The state machines generate timed enables to check parity errors on data transmissions, ECC errors on SA boards, and memory-not-present conditions. Parity errors detected on GDP, IP, and SA boards are also logged in registers on the MC board. When a memory access error is detected, the SA board ID, bank address, syndrome, and error type are recorded in error registers on the MC board.

STORAGE ARRAY BOARD

The basic storage elements of an SA board are dynamic Random Access Memories with error correction features. Data is stored in 39-bit wide banks, four data bytes plus seven error correction bits.

A block diagram of an SA board is shown in Figure 3-6.

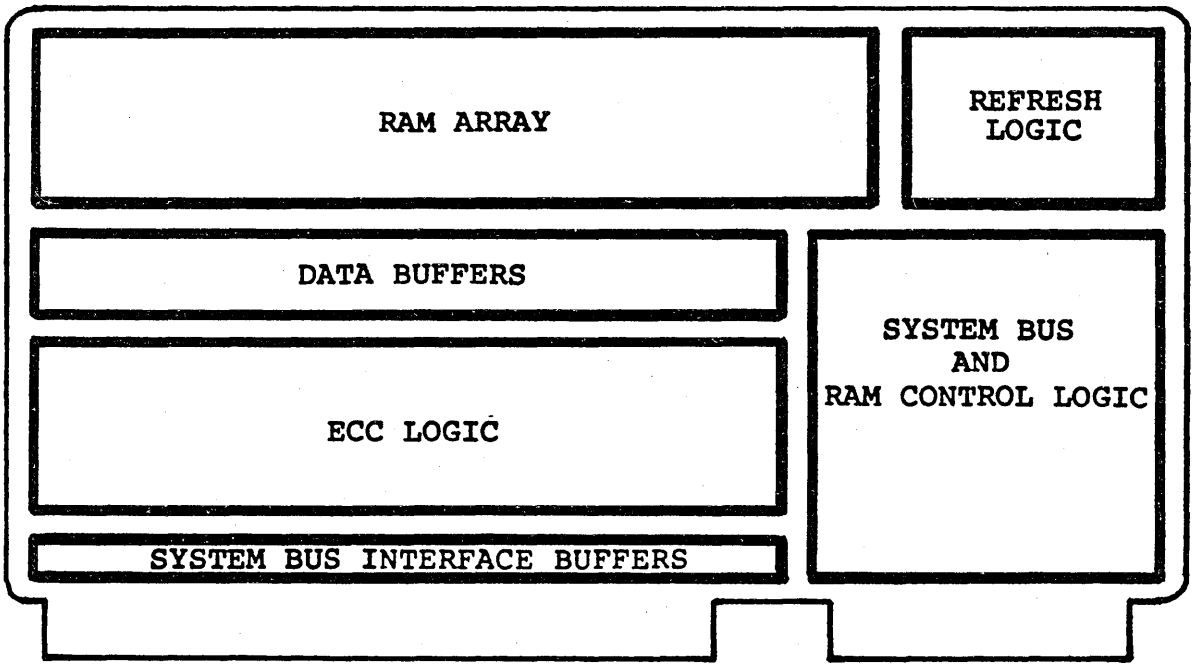


Figure 3-6. Storage Array Board Block Diagram

A diagnostic operation mode is provided that allows writing the full 39 bits without ECC generation. This mode is used in diagnostic routines to allow program checking of the RAM ECC chips and ECC logic operation.

As on all boards populating the System Bus, parity is generated on each byte transmitted and checked on each byte received. If a parity error is detected on incoming address or data for a Write operation, the RAM Write enable is blocked and the data is not written.

SYSTEM BUS AND RAM CONTROL LOGIC

The SAD bus interface and buffers on an SA board use window latches for faster operation.

System Bus and RAM control is under the control of one PROM-based state machine, and one flip-flop based state machine.

The System Bus state machine controls timing and gating of System Bus lines on the SA board.

Memory Controller lines are decoded to allow five modes of operation on SA boards:

- Word Read - a full 32-bit word stored in memory is read, parity is generated for each byte, and the four bytes and four parity bits are gated to the SAD bus.

- Byte Read - a word is read from memory and one, two, or three bytes of data requested from the location specified are gated to the SAD bus.

- Word Write - a 32-bit word is taken from the SAD bus and written into the memory location specified.

- Byte Write - one, two, or three bytes of data are taken from the SAD bus. They are inserted into a full 32-bit word read from the specified address, and written into memory. New ECC bits are generated for the new word before it is written.

- Refresh - once each 16 microseconds, the refresh state machine initiates a refresh cycle. Refresh cycles occur on one SA board at a time. They are transparent to the Memory Controller. If a memory access occurs while a refresh is in progress, the MC simply sees an extended cycle.

Reset places the System Bus controller in a waiting state. An Access Array command from the Memory Controller, with the proper board address translation, initiates a Storage Array board state machine access cycle. The state machine first tests for a Refresh cycle in progress, then for a Read or Write cycle in the current access. If a Refresh cycle is in progress, the bus state machine waits for it to finish before continuing the access sequence.

The state machine enables parity logic so that parity bits are generated for incoming data bytes and compared with the received parity bits. If an incoming parity error is detected, the RAM controller inhibits the "Write" enable.

The incoming address is gated to the RAM address multiplexor, and a Read is initiated to the RAM controller state machine. The bus state machine then checks for Data Strobe to enable proper data gates. If this is a Read operation, Byte Drive Select logic is enabled and the proper bytes are gated to the SAD bus. If an error is detected during a Read operation, the proper error message is gated to the Memory Controller.

In a Write cycle, data from the SAD bus is inserted into the word read from memory if needed; then the 39-bit word, including generated ECC bits, is written into memory.

RAM control logic uses timed inputs from the System Bus state machine and the Refresh state machine to generate enables for row, column, and Write enable for Read and Write memory accesses and refresh cycles. The incoming address is multiplexed into the form necessary to drive the RAM array, and gated by RAM control logic.

REFRESH LOGIC

The refresh logic consists of a state machine, associated logic, and a refresh address counter. The one-microsecond clock from the MC board is used to count the 16-microsecond delay between refresh cycles. At refresh time, the state machine checks for a memory cycle in progress, waits for it to finish, if necessary, then initiates a refresh cycle. A new memory access cycle is locked out until the refresh cycle is complete. The RAM state machine is enabled for a refresh cycle and the address counter is enabled to step through the 128 row addresses necessary to do a RAM refresh. The output of the counter is gated to the address multiplexor for the refresh cycle.

ECC LOGIC

Parity generators, multiplexors, and associated gates make up the error detection/correction logic. On a Read operation, the read data is used to generate an ECC code, then the read and generated codes are checked for errors (the correct syndrome is equal to zero). Single-bit errors are corrected and double-bit errors are detected; in both cases, the error status condition is reported to the MC. During diagnostic operation, the ECC generators are disabled by Diagnostic Mode selection on the MC board, which allows the full 39-bit word to be written in memory. This allows writing a known "error word" in memory. The ECC logic is then enabled, and the word is read normally to verify proper operation of the ECC RAMs and ECC logic.

CHAPTER 4
SOFTWARE INTERFACE

INTRODUCTION

The System 432/600 provides the full iAPX 432 Micromainframe instruction set. The 432 instruction set is described in the iAPX 432 General Data Processor Architecture Reference Manual and the iAPX 432 Interface Processor Architecture Reference Manual. In addition to supporting the capabilities inherent in the iAPX 43201/43202/43203 chip set, System 432/600 PC boards contain specific hardware for system initialization, Interface Processor control, error logging, and system diagnostic aids. This chapter describes the software interface to that specific hardware, and its use in the system.

GENERAL DESCRIPTION

The Attached Processor's only path to the 432/600 Central System for control, data, and status information is the IP board with its Interface Processor chip. Because of this, the IP board contains a significant portion of the hardware specifically designed for the software interface. Most of the remaining interface hardware is located on the Memory Controller board. The physical location of the hardware has significance only to the diagnostic programs.

Figure 4-1 shows command and data flow paths in the system. Hardware available to AP software is indicated by heavy lines on the drawing.

The IP board provides nine 8-bit Multibus I/O ports (registers) accessible to AP software. (A total of 16 ports are addressable. The seven high-address ports are duplicates or undefined.) There are three LSI programmable interface chips on the IP board that make up I/O Ports 6, 7, and 8.

Tables at the end of this chapter list registers available to AP software, and their address and content.

Eight 16-bit System 432/600 local registers are available to the AP. Access to any local register is accomplished via Window 1 of the Interface Processor. In a System 432/600, these instructions reference local registers located on the Memory Controller board.

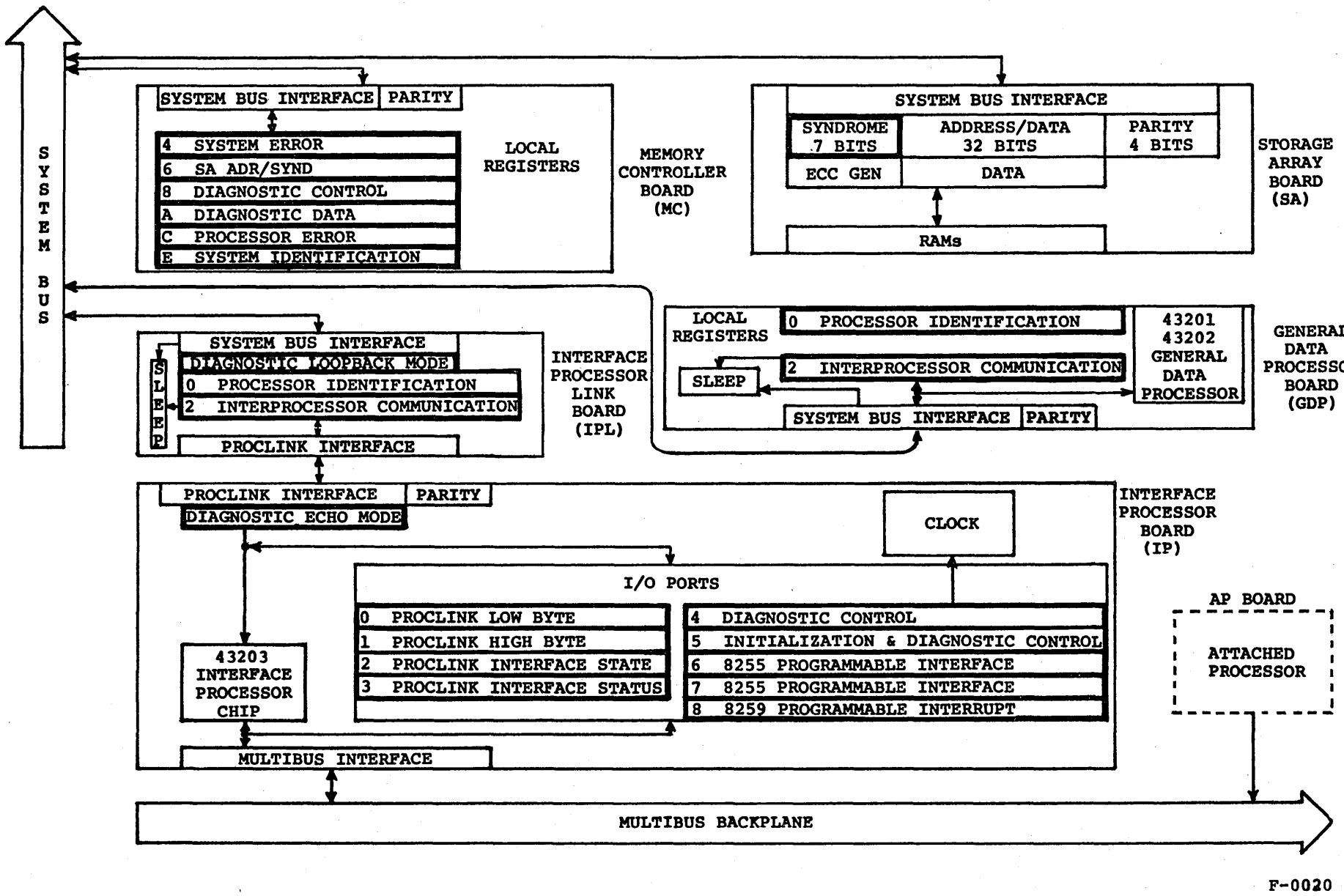


Figure 4-1. Software Interface Implementation

As shown in Figure 4-1, two local registers are located on each GDP board. The Processor Identification register receives its input from the GDP board's slot position in the backplane. Etched lines on the backplane determine each processor's ID assignment. A GDP board's ID may be changed only by changing that board's physical position in the backplane.

A GDP uses its Interprocessor Communication (IPC) register in two ways. To send a local IPC, it loads its own IPC register with the ID of the processor that will receive the communication. In the case of a global IPC, a zero ID indicates that all processors should receive the IPC. When signaled it has a pending incoming IPC, a GDP reads its IPC register to determine the type: local or global.

One GDP ID register and one GDP IPC register are located on the Memory Controller board. The MC gets ID and IPC data for these registers from the processor currently accessing memory.

The remaining six local registers are located on the MC board. Like all 432 system data, the contents of local registers are available to the AP via software through IP board logic. The Attached Processor may access the registers one byte at a time, or access the full register by the proper double-byte address with an access length of two bytes.

System 432/600 hardware accessible to Attached Processor software is discussed in three logical sections: initialization, error logging and error information retrieval, and diagnostic operation.

INITIALIZATION

Initializing the system begins with a hardware reset that forces system components to a known state. In a System 432/600, this action occurs as two operations: an AP reset and a 432 reset. An AP reset is normally the result of a power-up reset signal or a front panel switch associated with the Attached Processor and Peripheral Subsystem.

Either reset, AP or 432, will logically disable normal functions of the IP board, isolating the 432 system from the AP (accomplished by resetting the IP Enable bit in Port 5 on the IP board). This is the only direct effect an AP reset will have on System 432/600 hardware.

The AP reset uses the Multibus INITIALIZE signal to force all peripheral device controllers to a known state. At the end of the AP hardware reset time period, a software reset/initialize routine must be initiated on the AP.

The first action the AP reset/initialize routine must do on the IP board is to load the proper control command words into the three interface chips comprising Ports 6, 7, and 8 on the IP board. These ports control gating Multibus commands, addresses, and data into IP board ports and logic. The next function of the reset routine is to set the IP Enable bit in Port 5 to enable IP board functions. At the same time, the Initialize bit in Port 5 will be set to begin initialization of the remainder of the 432 system.

INITIALIZE to a GDP board sets the Sleep flip-flop and puts the GDP into Sleep Mode. In this condition, the GDP monitors the System Bus for incoming signals, but cannot transmit any data or commands to the System Bus. This isolates the GDP board from the remainder of the system.

After initialization, a local or global IPC to a General Data Processor (via a SEND TO PROCESSOR instruction) clears its sleep condition, and thereby initiates normal operation. (The initialization routine must have previously loaded required areas in 432 memory with the initial object table directory, and all objects, tables, ports, and program instructions necessary for operation.)

If more than one IPL board is in a system, one board executes the Initialize from its IP, and the remaining IPL boards are disabled until their corresponding IPs receive Local IPC transfers.

ERROR LOGGING AND RETRIEVAL

There are three local registers associated with error logging and retrieval: System Error, Storage Array Address/Syndrome, and Processor Error. As shown in Figure 4-1, they are located on the MC board. Combining data from the three registers provides specific error conditions such as which processor entered a fatal state, where a parity error occurred, the SA board address where an error was detected, and whether it was correctable or uncorrectable. Refer to Tables 4-10, 4-11, and 4-12 for error bit details.

The three registers should be periodically read to monitor error conditions in the system. Immediately after reading the System Error and SA Address/Syndrome registers, a Write operation to the System Error register should be done to clear error registers of the old data and initiate another sample period. (The Write operation clears the error registers; the data written is not significant.)

The System Error register logs data relating to errors detected by processors, the MC board, and the Storage Array boards. Bit positions in the register indicate processor fatal status, parity errors on data and address transmissions, and correctable/uncorrectable read data errors from the Storage Array boards.

The SA Address/Syndrome register contains information about the access that resulted in the memory error logged in the System Error register. Data in both registers must be interpreted to determine the error type and where it occurred. The SA Address/Syndrome register may contain the address of an SA board, the syndrome field of an error word, or the ID of a processor related to the error specified in the System Error register.

The Processor Error register contains a pair of error flags for each of the six possible processors in a system. The flags denote Fatal or Parity Error conditions for each processor. A processor's parity flag is reset by a Write of zeros to the System Error register. A processor's fatal flag will remain set as long as the fatal condition exists.

DIAGNOSTIC OPERATION

Diagnostic operation is initiated by setting proper control bits (mode commands) in I/O Port 4 - Diagnostic Control, and the Diagnostic Control register on the MC board.

The I/O ports provide a path around the IP chip in PASS mode, allowing system logic checks to be performed knowing the IP chip cannot affect the tests. Disabling the IP board clock allows tests to be performed under the control of a "software clock". Each Port 1 access in PASS mode by the AP causes one clock pulse to be generated by the IP board.

After all basic checks are done via software clocking, the clock is enabled and the tests are rerun at normal clock rate. This checks both the logic operation at normal clock rate and the basic functional operation on the iAPX 43203 IP chip.

Other bits in the IP diagnostic control registers provide data turnaround. The AP can transfer data to the ECHO RAM register on the IP board, then read it back for comparison to check for proper operation of transfer commands and data paths.

Figure 4-1 shows the ECHO mode turnaround at the ProcLink interface point of the IP board, and the LOOPBACK mode turnaround at the System Bus interface point on the IPL board. Both modes may be used with PASS mode (software clock) or without PASS mode (normal clock).

I/O Ports 2 and 3 (ProcLink Interface State and Status) may be read during the tests to verify proper ProcLink state machine operation.

Local Register 8 on the MC board is used by AP software to place the System 432/600 under full Diagnostic Control. One selection bypasses the memory address mapping PROMs on the MC board, allowing direct addressing of the SA boards. The amount of memory on each SA board may be determined by software using direct addressing by incrementing the address until the Memory Not Present status is returned. Proper operation of the mapping PROMs is checked by writing in direct address mode, then reading with the PROMS enabled for normal logical address mapping.

Diagnostic control on the MC board puts the SA boards into "FULL WORD ACCESS" mode. This allows AP software to control reading and writing the seven ECC bits of the storage word to check operation of the ECC RAMs and their related logic.

The Diagnostic Data register serves as a data port for the seven ECC bits during full word accesses. It may also be used as a turnaround register to check the data transfer path from the AP to the MC board.

The System Identification register is wired to a logical one on the Memory Controller board. This identifies the System 432/600 board set to the diagnostics.

INTERFACE PORT AND REGISTER TABLES

Tables 4-1 through 4-15 define the bit content of all I/O ports and system local registers. In the contents of a register, an "X" indicates no significance, "1" indicates a hard-wired 1, and "0" a hard-wired 0. A letter in a register table is followed by a definition or a table of definitions. A ? means bits that are set by system conditions.

Table 4-1. I/O Ports and Addresses

I/O ADDR	I/O PORT	OPERATION
0	ProcLink Low Data Byte	Read/Write
1	ProcLink High Data Byte	Read/Write
2	ProcLink Interface State	Read only
3	ProcLink Interface Status	Read only
4	Diagnostic Control	Read/Write
5	Diagnostic and Initialization Control	Read/Write
6	8255 Control	Read/Write
7	8255 Control	Read/Write
8	8259 Interrupt Control	Read/Write
9	Undefined	
A	8259 Interrupt Control	Read/Write
B	Undefined	
C	8259 Interrupt Control (same port as 8)	Read/Write
D	Undefined	
E	8259 Interrupt Control (same port as A)	Read/Write
F	Undefined	

Table 4-2. Port 2, ProcLink Interface State

CURRENT ACCESS SPECIFICATION BITS				IP BOARD PROCESSOR STATE MACHINE BITS			
?	?	?	?	?	?	?	?
MSB							LSB

Table 4-3. Port 3, ProcLink Interface Status

D	A	I	R	P	F	B	C

MSB LSB

Table 4-4. ProcLink Interface Status Register Bit Definition

STATUS BIT	SIGNAL FUNCTION
D	Data Ready (EOMC signal)
A	System 432/600 Alarm
I	System 432/600 Initialization
R	IP Request (PLKREQ signal)
P	Read Parity error detected
F	IP Fatal
B	ACD Bus error detected
C	IPC from the System 432/600

Table 4-5. Port 4, Diagnostic Control

X	X	X	X	X	E	P	F

MSB LSB

F = 1 Set PRQ (High) or (Active)
P = 1 Set PASS mode
E = 1 Set ECHO mode

Table 4-6. Port 5, Diagnostic and Initialization Control

X	X	X	X	X	E	L	I

MSB LSB

I = 1 432 Initialization Request
L = 1 Set LOOPBACK mode
E = 1 Enable normal IP board operation

Table 4-7. System 432/600 Local Registers

LOCAL REG ADDR	REGISTER	OPERATION
0	Processor Identification	Read only
2	Interprocessor Communication	Read/Write
4	System Error	Read/Write
6	SA Address/Syndrome	Read only
8	Diagnostic Control	Read/Write
A	Diagnostic Data	Read/Write
C	Processor Error	Read only
E*	System Identification	Read only

*Register E has been reserved for use in later systems; currently it is hardwired to "1".

Table 4-8. Local Register 0, Processor Identification

1	1	1	1	1	1	1	1	0	0	0	0	0	PROC ID

Table 4-9. Local Register 2, Interprocessor Communication

1	1	1	1	1	1	1	1	0	0	0	0	0	0	G	L	READ

G = 1 Global IPC Pending
L = 1 Local IPC Pending

X	X	X	X	X	X	X	X	X	X	X	X	X	PROC ID	WRITE

Table 4-10. System Error Register and Bit Definition

1	1	1	1	1	R	ME	PE	C	M	ERR B	ERR A

System Error Register

ERROR BIT	ERROR DEFINITION
M	Multiple Error Detected. If the error logging logic detects two or more fatal errors during the same sampling period, this bit becomes asserted.
C	Correctable Memory Error. This bit is asserted when an SA board accesses a memory location which has a single bit (correctable via ECC) error.
PE	Processor Error. A processor has indicated to the error logging logic the presence of a read data parity error or that a processor has entered a fatal state.
ME	Memory Error. This bit is used to validate the lower seven bits of this register.
R	Read-Modify-Write Timeout. A Read-Modify-Write timeout occurred since the last sampling.
ERR A-B	Error Code, defined in Table 4-11 following.

Table 4-11. System Error Register Error Code Definition

ERROR CODE	ERROR CODE DEFINITION
000	Reserved.
001	MC Address Parity Error. The MC board detected an error on an address transmitted by a processor board.
010	MC Data Parity Error. The MC board detected an error on data transmitted by a processor board.
011	Memory Not Present. An access was made to a location in the 432's address space which doesn't have memory to support the request.
100	SA Address Parity Error. An SA module addressed by the MC board detected an error in the address transmitted to it by the MC board.
101	SA Data Parity Error. An SA module currently performing a Write cycle detected an error in the data transmitted to it by the processor board which initiated the access.
110	Uncorrectable Data Error. An SA module accessed a location in memory which contains two or more data bit errors.
111	No error.

Table 4-12. SA Address/Syndrome Register and Field Definition

MODULE ID	ADDRESS		SYNDROME
ERROR TYPE	SYNDROME	ADDRESS	MODULE ID
000	--------	--------	--------
001	--------	--------	PROC ID
010	--------	--------	PROC ID
011	--------	ADDRESS	SA ID
100	--------	ADDRESS	SA ID
101	--------	ADDRESS	SA ID
110	--------	ADDRESS	SA ID
111	--------	--------	--------
C	CORR SYND	ADDRESS	SA ID

Error Type is ERR A or ERR B in the System Error Register, Table 4-12. Address is the upper four bits of the address.

Table 4-13. Local Register 8, Diagnostic Control

X	X	X	X	X	X	X	X	0	0	0	0	0	I	F	D

D = 1 Bypass MC Address Mapping PROM
F = 1 Full Word Access
I = 1 Interleaved Memory (Hardware Set)

Table 4-14. Local Register A, Diagnostic Data

1	1	1	1	1	1	1	1	?	?	?	?	?	?	?	?

? = Data

Table 4-15. Local Register C, Processor Error Register

F6	F5	F4	F3	F2	F1		P6	P5	P4	P3	P2	P1	
13	12	11	10	9	8		5	4	3	2	1	0	Bit

F = Fatal Condition
P = Parity Error Detected

INTRODUCTION

A meaningful measure of the performance of a computer system can only be made when considering a specific application. Thus, instruction timings and benchmarks can be misleading. Although the speed at which a processor executes individual instructions is an important indicator of potential performance, other factors influence performance: How is the system configured? What language was the program written in? Is the compiler efficient? What percentage of processor time is consumed running the operating system? Is it a batch system, embedded, or interactive? Will there be multiple users?

These questions and others must be considered carefully when estimating a computer system's performance. For a multiprocessor system like a System 432/600 computer, the task is even more difficult. Because each processor contends for access to the system memory, the gain in performance from adding a processor is not a linear function; it is affected by the instruction mix and the number of concurrent processes. The effect of adding GDPs to a System 432/600 is, however, approximately linear. In general, a System 432/600 with five GDPs will have about 3.75 times the performance of a system with only one GDP. Refer to Figure 5-1.

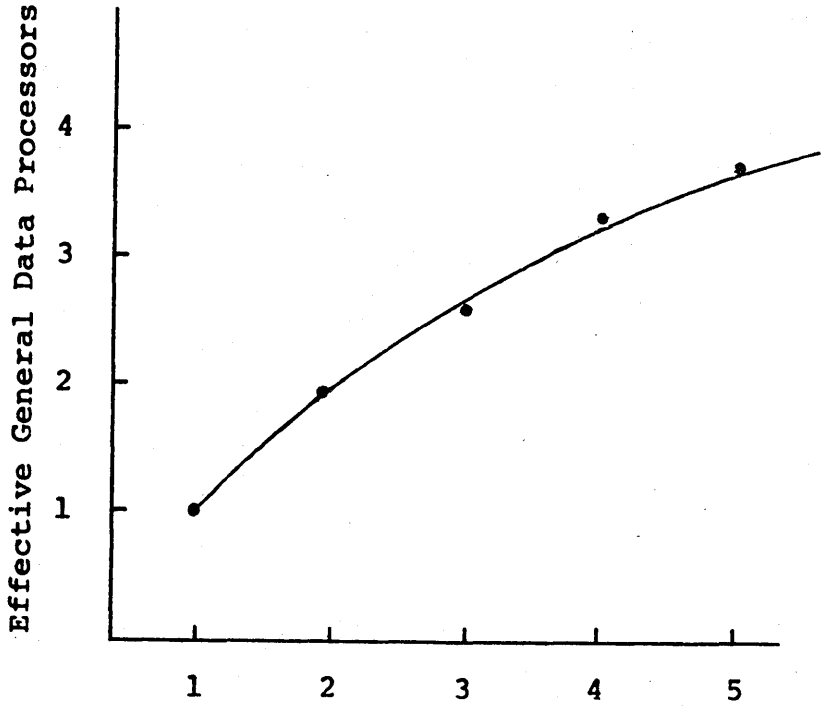


Figure 5-1. Performance Range F-0263

When considering only a low-level instruction mix, a user should expect the performance of a System 432/600 with a single General Data Processor to be comparable in performance to an iAPX 86/87 processor pair, or a small minicomputer. In applications which have a large number of concurrent processes, a System 432/600 computer will have a distinct advantage. Conventional computers must assume the operating system overhead of scheduling and dispatching processes, whereas a System 432/600 computer performs these functions directly in hardware.

The performance of a System 432/600 computer with four General Data Processors will rival a low-end 32-bit minicomputer. Again, the System 432/600 will have a performance advantage in applications which traditionally require a multitasking operating system. High-level functions such as interprocess communication and heap memory allocation will be five to 20 times faster on a System 432/600 than identical functions performed by a conventional operating system.

A system designer can also trade computational power for greater I/O capacity and performance, an alternative that is not available to the user of a minicomputer which has a fixed number of I/O channels. Rather than overload a single Peripheral Subsystem on a System 432/600, another Peripheral Subsystem can be added with its own Interface Processor and Attached Processor. Thus, a System 432/600 permits a much higher percentage of system resources to be devoted to peripheral device functions. For example, an application requiring a large number of connected terminals each demanding relatively small computational power could be supported by one GDP and five Peripheral Subsystems.

To use a System 432/600 efficiently, the programmer should understand some of the factors affecting the performance of a multiprocessor system. Many functions traditionally performed by an operating system are done directly by the hardware, and programmers should exploit this increased efficiency when planning their applications.

AUTOMATIC PROCESS SCHEDULING

The System 432/600 family of products is used to build tightly-coupled multiprocessor systems in which each of the GDPs shares a common memory and the same software. The benefit is better performance at a substantially lower cost. An individual GDP is inexpensive and has moderate performance; by sharing the work, several GDPs are able to perform the same functions in less time than a single, more expensive processor.

Until now, software has been the obstacle to implementing multiprocessor systems. In previous systems, the operating system scheduled processes for execution by individual processors. Unfortunately, this made the software dependent on the specific number of processors in the system. If a processor later needed to be added, or if one failed, the software had to be modified to compensate. Consequently, multiprocessor systems generally have required complex yet inflexible software.

The iAPX 432 architecture removes this restriction by making process scheduling a function of the hardware, rather than the operating system. Each processor is self-dispatching; that is, each processor automatically selects a process from the top of a queue in memory, known as the dispatching port, which holds a list of processes waiting to run. The selected process is executed for its share of time set by software. Then, after the service period of the process expires, the processor returns the process to the dispatching port and places it in the proper place in line, according to its priority. When it again reaches the top of the queue, the process is once again selected by whichever processor is available. At various stages of its execution, a process may run on several different processors. Scheduling and dispatching are considerably more efficient than the same functions performed by a multitasking operating system.

TRANSPARENT MULTIPROCESSING

Software is unaffected by the number of processors in a System 432/600 computer. This feature is called "transparent multiprocessing." A processor can be added to a system to increase performance, or it can be removed from a system because it has failed. Neither the operating system nor the application programs need to be altered to accommodate the change. For example, a program which executes correctly on a system with two processors will also run correctly on a system with only a single processor or one with several processors. The difference between the systems will be in their throughput. In general, adding processors increases the performance of the system.

Frequently a user is forced to purchase a high performance computer at a substantial cost just to allow capacity for future expansion. The System 432/600 family of products offers an economical alternative. Adding a processor to a system is much less expensive than replacing an entire computer, even if the new computer is a member of the same family and is software-compatible. System 432/600 computers can be configured to provide a wide range of performance. A user can begin with a system of moderate performance at a low cost; later, processor boards can be added as the demands on the system increase.

PRACTICAL LIMITATIONS

Nevertheless, two factors limit the increase in performance if processors are added: the number of processes awaiting execution, and the bandwidth of the memory. Since most systems always have a large number of processes which are ready to run, the first factor is very seldom a consideration. If, however, there are fewer processes waiting to be executed than there are processors, the extra processors will sit idle. Adding more processors to such a system only increases the number of idle processors and doesn't increase the system performance.

Usually, the bandwidth of the memory is the practical limitation. In most multiprocessor systems, including the System 432/600 family, processors take turns transferring data to and from memory; while one processor is doing computations, another processor is using memory. If, however, two processors require access to memory at the same time, one is forced to wait. Arbitration logic rations access to memory, assuring that each processor receives an equal share. The possible range of performance for the system depends on the percentage of time the memory is available. As processors are added to a system, each processor spends a greater portion of its time waiting for memory.

Of course, the ratio of computation time to memory access time is partly related to the particular application of the system. Some types of instructions take much longer for a processor to execute than others. Like a single processor system, the performance of a multiprocessor system is affected by the mix of instructions. For example, a program which manipulates long character strings requires a larger number of memory accesses in the same time period on a System 432/600 computer than a program which mainly performs floating point calculations. Consequently, the benefit of adding processors to a system varies with the application. One application might effectively use five processors, while another may be able to use only four.

Thus, the key to designing an efficient multiprocessor system is in reducing the percentage of time each processor spends idle. One possible alternative is to use very fast memory components in the Memory Subsystem. Although the memory would then have a faster response time, the cost of the Memory Subsystem would increase dramatically. The design of the System 432/600 is aimed at the optimum mix of moderate cost, fast memory accesses, and efficient data transfers.

EFFICIENT DATA TRANSFERS

Three fundamental operations consume time when using a conventional memory: addressing a location, reading data, and writing data. In most systems, the operations are performed in indivisible pairs, either addressing and reading or addressing and writing. To accomplish this, a single processor will hold the memory bus until both operations have been completed. Because the Memory Subsystem takes time to satisfy a request, there is a lag between addressing a location and the transfer of data.

When a System 432/600 processor needs to access memory, it sends a single request specifying from one to ten bytes of data. In contrast, a conventional system could require as many as ten separate memory accesses to access the same 80 bits of data, with each separate memory access using time for arbitration and for transfer of an address to the memory controller. In a System 432/600, the arbitration and address transfer is performed only once for a multiple byte memory access; the Memory Controller increments the address and reads or writes the number of bytes specified by the access request with no further intervention from the processor.

Furthermore, the instruction formats used by 432 processors are designed to reduce the number of bytes transferred. In many conventional systems, the length of an instruction is always a multiple of the memory word size. Since the number of operands and the number of control bits vary from instruction to instruction, some bits go unused in most types of instructions. In contrast, the instructions used by the 432 processors can be any number of bits long, and a memory access is made to a byte boundary rather than a word boundary. Consequently, the number of bytes that must be transferred when a processor fetches instructions is reduced. The processor doing the fetch begins execution of the instruction sooner, and another processor waiting to use memory starts its memory access sooner.

Of course, every application has a practical limit to the number of processors which can be used. For nearly all applications, however, a System 432/600 can effectively use six processors, counting both GDPs and IPs.

INTRODUCTION

The design of the System 432/600 family of products included heavy emphasis on reliability, availability, and serviceability. Proven, conservative design techniques were used in all areas of the system to maximize reliability. Availability and serviceability are enhanced by the extreme modularity of the system, the small number of PC board types, and the inclusion of a significant amount of hardware designed specifically for error detection, correction, and logging, as well as for maintenance and diagnostic use.

This chapter introduces the System 432/600 Diagnostic Software package and gives an overview of the diagnostic programs. A brief description of the diagnostic hardware in the system and its relationship to the diagnostic programs is also included.

The System 432/600 Diagnostic Software User's Guide provides a complete description of the diagnostic software, including loading and operating procedures, error messages, and detailed algorithmic descriptions of the board test programs.

DIAGNOSTIC SOFTWARE OVERVIEW

System 432/600 Diagnostic Software is a set of PL/M-86 and extended Ada programs which use specially designed hardware to isolate system faults to board level. All access and data paths, all memory locations, and representative processor instructions are exercised. Error messages identify the faulty board, which is then replaced to restore full system operation. In systems with multiple GDP or SA boards, a faulty GDP or SA board can simply be removed and the system restarted. System functionality is not affected, although there may be reduced throughput as a result of the reduction in the number of GDPs or the size of system memory.

System 432/600 Diagnostic Software includes the following programs:

- System Configuration
- Diagnostic Supervisor
- Interface Processor board diagnostic
- Interface Processor Link board diagnostic
- Memory Controller board diagnostic
- Storage Array board diagnostic
- General Data Processor board diagnostic
- System Validator

The programs are designed to run on an iSBC 86/12A Attached Processor in a System 432/600 Peripheral Subsystem.

SYSTEM CONFIGURATION PROGRAM

The System Configuration program is automatically run the first time the diagnostic package is loaded into a system. Following prompts in the System Configuration program, the operator selects the test length, the program stop conditions, the error log device, and indicates the backplane slot number and processor type for each processor board in the system being tested. The configuration is then stored as a part of the package, and referenced during later diagnostic runs.

The System Configuration program may be re-run at any time by selecting it from the main menu. It must be re-run to change the selected test length, stop conditions, error log device, or the location or type of processor boards in the system.

DIAGNOSTIC SUPERVISOR

This program controls the interface between the diagnostic programs, the user, and the system's I/O hardware. The program provides a series of prompts and displays to help an operator use the diagnostic package.

A main menu displayed by the Diagnostic Supervisor allows the operator to select the System Configuration program, the complete diagnostic package, individual board tests, or the System Validator.

TEST SEQUENCES AND ERROR MESSAGES

Each board type is tested by a separate diagnostic board-test program. The normal test sequence of the full Diagnostic Software package starts on the IP board in the Peripheral Subsystem and progresses through the ProcLink cable to the IPL board in the Central System. The diagnostics then test the MC board followed by the SA and GDP boards.

Error messages associated with each test are displayed to inform the operator of what board is being tested, and what test failed. GDP and SA error messages also give the slot number of the failing board.

In addition to resolving a fault to board level, diagnostic error messages may be used to isolate a board fault to a logical section of the board for troubleshooting purposes.

SYSTEM VALIDATOR

A System Validator program is included as one option in the main menu. It is a subset of the full diagnostic package, intended for use as a quick confidence test, and runs in much less time.

RESTORING SYSTEM OPERATION

A failing MC, IP, or IPL board must be removed and replaced to restore system operation. A failing GDP or SA board may, of course, also be removed and replaced.

If a system contains more than one GDP board, a failing GDP board need only be removed to restore system operation. A system will run, with some throughput degradation, as long as at least one GDP board remains in the system.

A system will run after removing one or more failing SA boards provided no SA board-slot gaps exist, and provided sufficient memory remains for the operating system and other software. In an interleaved configuration, SA boards must be removed in pairs; an alternative is to convert to non-interleaved operation and remove the one faulty SA board.

DIAGNOSTIC BOARD TEST PROGRAMS

The diagnostic board test programs run on an Attached Processor in a Peripheral Subsystem. Therefore, the first modules tested must be the Multibus interface and IP board in the Peripheral Subsystem containing the AP running the diagnostics.

The descriptions which follow are in the order the board test programs run: IP, IPL, MC, SA, and GDP.

INTERFACE PROCESSOR BOARD DIAGNOSTIC

The Interface Processor board may be divided into logical sections, as shown in Figure 6-1. IP board hardware includes nine 8-bit I/O ports (registers) accessible to AP software. Six of the I/O ports are used by the diagnostic programs. The ports provide a means for AP software to initialize the 432/600 Central System and control diagnostic functions. Table 6-1 lists these ports.

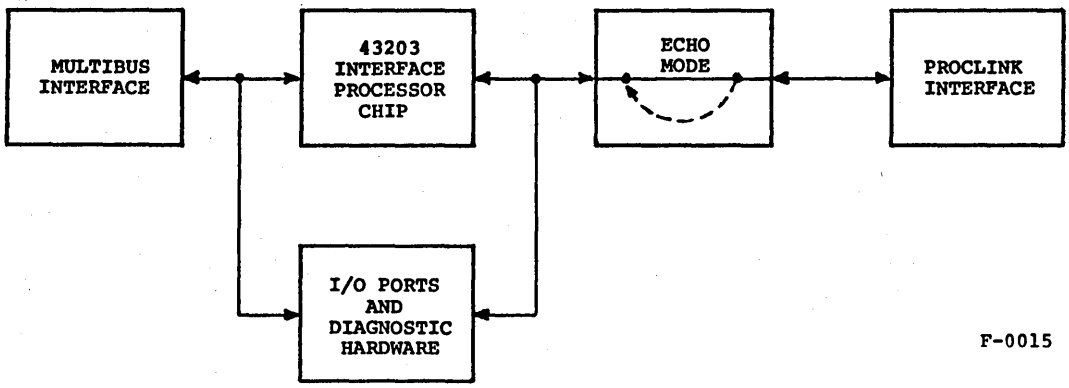


Figure 6-1. Interface Processor Board Functions

Table 6-1. Diagnostic I/O Ports

Port 0	Low-order eight bits of ProcLink I/O buffer
Port 1	High-order eight bits of ProcLink I/O buffer
Port 2	ProcLink interface state and specification of current access
Port 3	ProcLink interface status
Port 4	Diagnostic control
Port 5	Diagnostic and Initialization control

Ports 0 and 1 implement the data transfer path between the AP and the 432/600 Central System during PASS mode operation. They are not used in other modes.

The low-order four bits of Port 2 contain the status of the 43203 Interface Processor state machine. The high-order four bits define the current access as Read or Write, and the number of bytes to be accessed.

Port 3 contains error, alarm, and initialization signals.

Port 4 allows the AP to select ECHO mode and/or PASS mode operation.

Port 5 allows the AP to start the IP board after initialization, initialize the 432/600 Central System, and select LOOPBACK mode.

PASS Mode

Selecting PASS mode disables the 43203 Interface Processor chip, enables a data path around it via I/O Ports 1 and 2, and disables the clock on the IP board. PASS mode enables logic that causes each Port 1 access by the AP to generate one clock pulse on the IP board. This allows the AP to "software-clock" all command and data transfers through the IP board. PASS mode may be selected alone, or with the other operational modes. PASS mode may be used only by the diagnostics.

ECHO Mode

Selecting ECHO mode disables the ProcLink cable drivers at the output of the IP board, preventing data transfer to the ProcLink cable and IPL board. This effectively isolates the IP board from the 432/600 Central System for diagnostic purposes.

Simultaneously, ECHO mode enables 16-bit registers at the ProcLink driver point on the IP board. When the AP transfers data through the IP board, the data is stored in these registers. When the AP requests data, the content of these registers is returned to the AP in place of data from the Memory Subsystem. Comparing the data transferred with the data received allows the AP to verify the Multibus interface, I/O ports, and related logic on the IP board.

LOOPBACK mode is described in the IPL board test.

IP Board Tests

IP board tests check the basic functions of the IP board including the 43203 Interface Processor chip. One major function of the Interface Processor is to generate physical addresses from logical addresses for Central System memory. Checking this is dependent on fetching data from memory, which involves the ProcLink cable, and the IPL, MC, and SA boards. This portion of the IP is tested during the Storage Array board tests.

INTERFACE PROCESSOR LINK BOARD DIAGNOSTIC

The ProcLink cable and the IPL board provide the logical and electrical link between the IP board on the Multibus backplane and the System Bus backplane. Figure 6-2 shows logical test divisions of the IPL board.

The IPL diagnostic program extensively tests the ProcLink interface, the Data Rotation and Storage Unit (DRSU), and the System Bus interface of the IPL board.

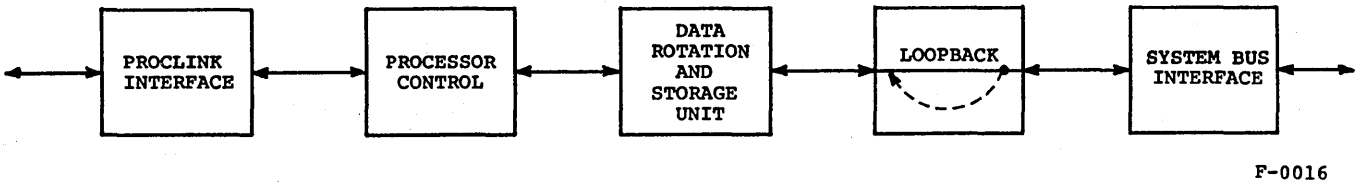


Figure 6-2. Interface Processor Link Board Function

In the IPL test, selecting LOOPBACK mode disables the System Bus drivers on the IPL board. This isolates the MC, SA, and GDP boards from the tests, and allows data from the AP to be transferred through the IP board and into the DRSU on the IPL board. The data can be returned to the AP from the DRSU upon command.

Selecting PASS mode with LOOPBACK mode allows the AP to software-clock data transfers into and out of the IPL board for initial tests of IPL logic. Selecting LOOPBACK mode without PASS mode allows these tests to be performed at the normal IP clock rate.

MEMORY CONTROLLER BOARD DIAGNOSTIC

Figure 6-3 is a logical block diagram of the Memory Controller board.

Local registers on the MC board allow data to be transferred to and from the MC board by AP software. Comparing returned data with the transmitted data verifies operation of the System Bus drivers and receivers on the IPL and MC boards, and MC local registers.

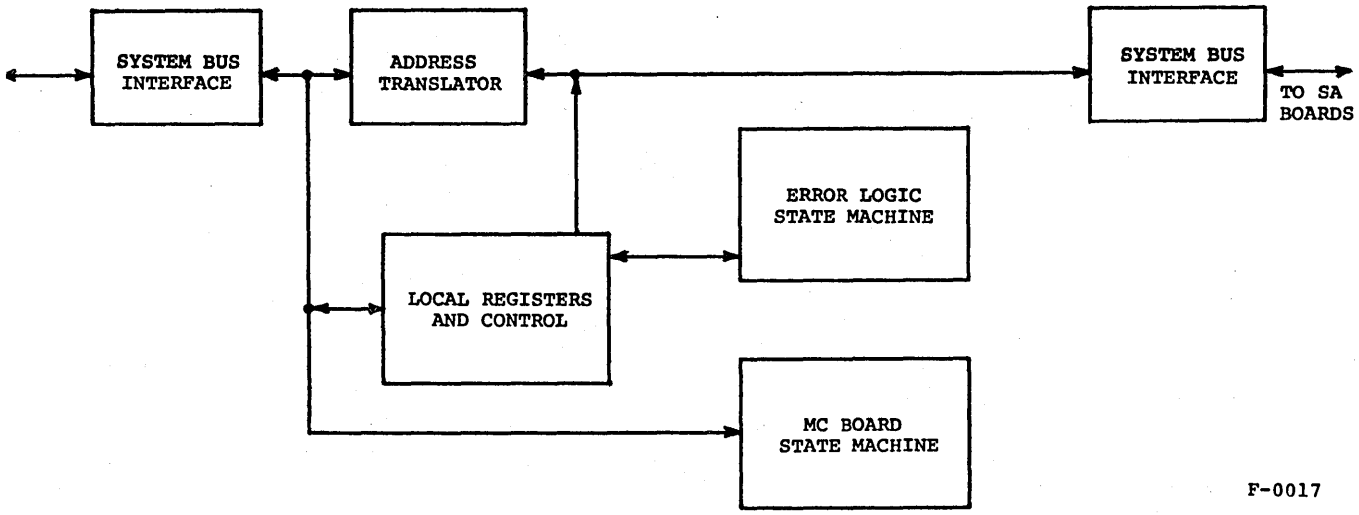


Figure 6-3. Memory Controller Board Functions

Local Register 8 on the MC board is the Diagnostic Control register. AP software sets control bits in this register which places the Central System under total diagnostic control. One diagnostic control bit causes the Address Mapping Translator PROMs on the MC board to be bypassed. This allows writing to specified physical addresses instead of logical addresses. The control bit is then deactivated, and the data is re-written, read, and compared in order to test for proper operation of the Address Mapping Translator.

Error registers and the error logic state machine are checked by forcing various system errors under diagnostic control, then reading the error registers to verify proper operation of the error detection and correction logic.

STORAGE ARRAY BOARD DIAGNOSTIC

Figure 6-4 is a functional block diagram of a Storage Array board. Error correction logic may be enabled or disabled by diagnostic control to isolate RAM ECC bit positions for test.

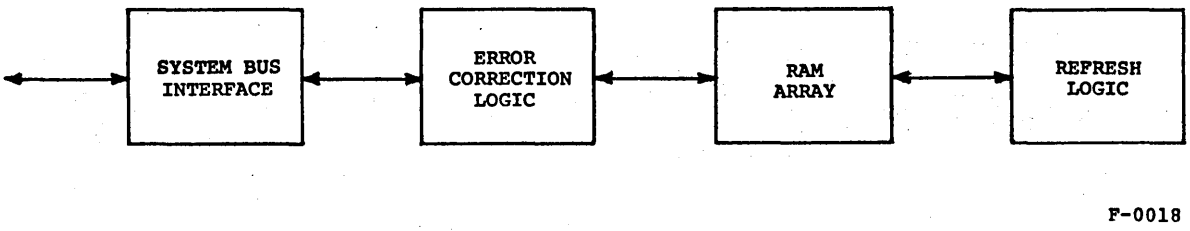


Figure 6-4. Storage Array Board Functions

Diagnostic Mode gives the AP access to the seven ECC bits on Storage Array boards. This Full-Word (39-bit) access allows AP software to control writing the 7-bit error correction code in the Storage Array ECC RAMs. Full-Word tests are performed on all locations with ECC logic disabled to check both data RAMs and ECC RAMs. Error words are written in Full-Word mode with the ECC logic disabled. ECC logic is then enabled and the error words are read to test the ECC functions and PROMs. Proper error logging is checked at this time. After ECC and error logging checks, all locations are again tested with ECC logic enabled. Proper operation of the Storage Array board data RAMs, ECC RAMs, error correction code logic, and the System Bus interface is verified in this manner.

One routine checks the ability of the Interface Processor to properly carry out memory mapping and alter map functions. This portion of the IP board test cannot be made until the data path from the IP board to the SA board's bus has been checked, and Memory Controller functions have been proven.

Three versions of the SA board test may be selected. The short sequence runs through 256K bytes in approximately 10 minutes. The normal sequence and the long sequence run in about 40 minutes and three hours, respectively.

GENERAL DATA PROCESSOR BOARD DIAGNOSTIC

Figure 6-5 shows General Data Processor board logic functions.

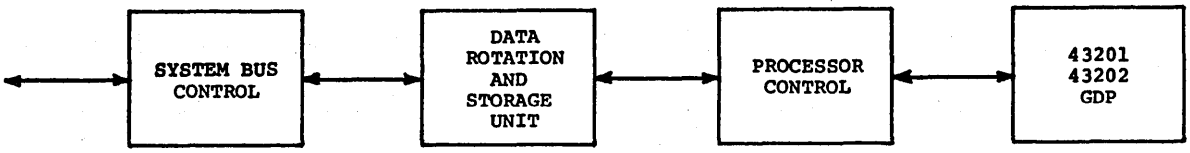


Figure 6-5. General Data Processor Board Functions

A System Reset to a GDP board puts it in "sleep" condition, which disables its System Bus drivers. This allows the remainder of the system to be checked, knowing a GDP malfunction cannot affect the tests. When the remainder of the system's operation has been verified, an IPC to the GDP board clears the sleep condition and enables its System Bus drivers. GDP board functions are then tested.

The GDP board test is divided into the following five subtests:

IPC Send Test for IP

This test determines if the IP can successfully send an IPC to a GDP. A test failure indicates a failure of the IP.

Initialization Test

The IP sends an initialization command to a GDP. A failure of the GDP to initialize indicates a failure of either the 43201 or 43202 components in the GDP pair or of the external logic on the GDP board.

Access Test

The System Bus Control block is tested in conjunction with the Processor Control block and the Data Rotation and Storage Unit by having the 43201/43202 chip-pair perform all possible lengths of memory accesses on all byte boundaries. If a memory access error occurs or the time-out expires, a message identifying the fault is displayed.

43201/43202 Component Test

The 43201/43202 chip pair is tested by executing various functions and checking the results with known correct values. These functions include representative data manipulation operations, communication operations, and fault identification and logging operations. An error message identifying the fault is displayed when any operation does not return the expected result.

43203 Component Test

The IP is placed in the logical mode for the first time and a functional test is performed to determine if it operates correctly.

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