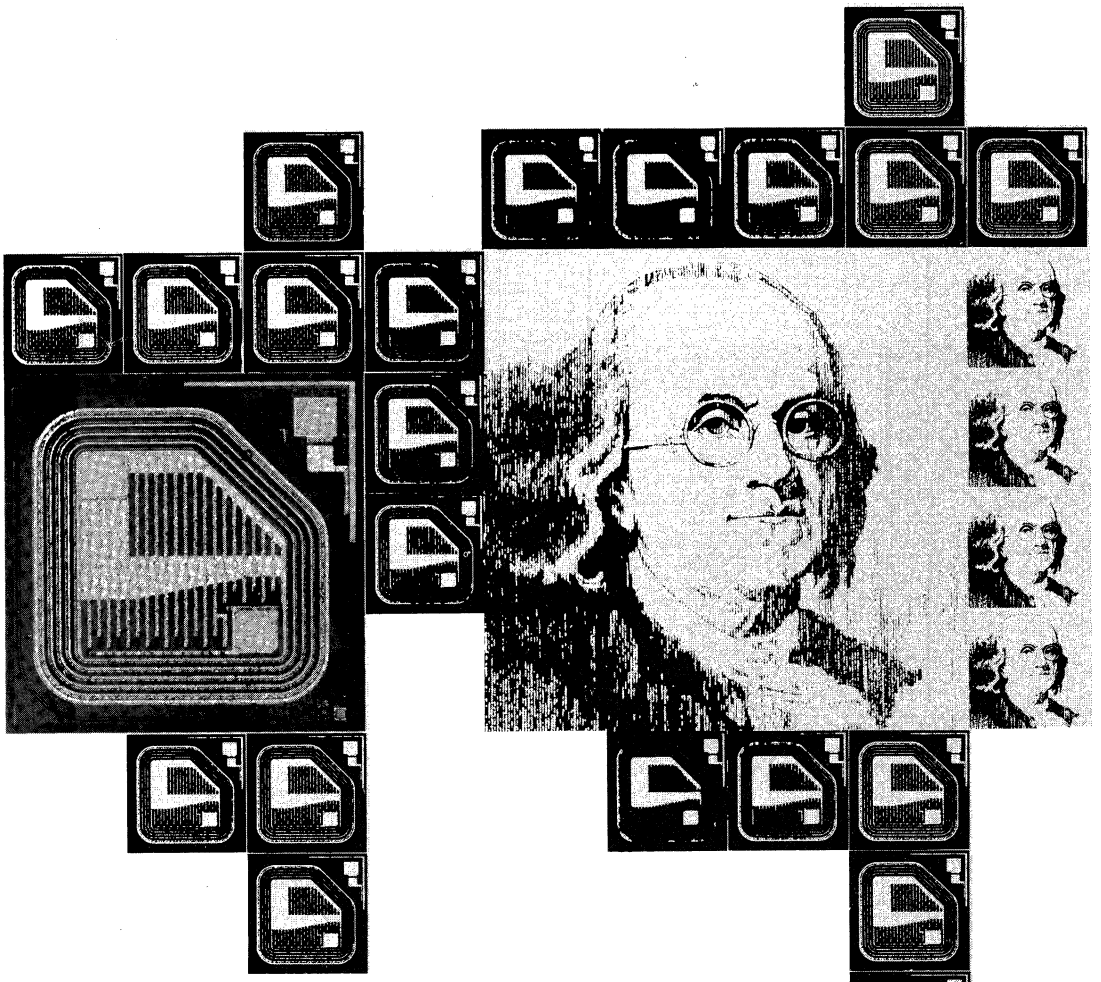

"Never confuse motion with action."

Benjamin Franklin, 1706—1790

INTERSIL

N-Channel Power MOS FETs

PACKAGE / BREAKDOWN	TO-3	TO-220	TO-39	TO-52	TO-237
800V, 700V	IVN6200KNW/X 2.5A, 6Ω	IVN6200CNW/X 2.5A, 6Ω			
500V, 450V, 400V	IVN6200KNS/T/U 5A, 1.5Ω	IVN6200CNS/T/U 5A, 1.5Ω	IVN6000TNS/T/U 1A, 4Ω	IVN6300SNS/T/U 0.1A, 75Ω	IVN6300ANS/T/U 0.1A, 75Ω
	IVN6000KNS/T/U 2A, 4Ω	IVN6000CNS/T/U 1.75A, 4Ω	IVN6100TNS/T/U 0.3A, 15Ω		
250V, 200V	IVN6200KNM/P 10A, 0.5Ω	IVN6200CNM/P 10A, 0.5Ω		IVN6300SNM/P 0.12A, 25Ω	IVN6300ANM/P 0.12A, 25Ω
100V, 80V, 60V	IVN6200KNE/F/H 10A, 0.25Ω	IVN6200CNE/F/H 10A, 0.25Ω	IVN5200TNE/F/H 4A, 0.5Ω	IVN5000SNE/F/H 0.9A, 2.5Ω	IVN5000ANE/F/H 0.7A, 2.5Ω
	IVN5200KNE/F/H 5A, 0.5Ω	IVN5201CNE/F/H 5A, 0.5Ω	IVN5000TNE/F/H 1.2A, 2.5Ω	IVN6300SNE/F/H 0.25A, 7.5Ω	IVN6300ANE/F/H 0.25A, 7.5Ω

2nd Source Products

	Non-Zener TO-39	Zener TO-39	Zener TO-202	Zener TO-237	Zener Quad
90V to 35V	VN35-99AK	VN30-90AB	VN40-89AF	VN10KM	VQ1000CJ
		2N6660-1			

ABOUT OUR COVER

We, at Intersil, believe in using the wisdom of the past to help turn today's ideals into tomorrow's realities. This policy is reflected in our advertising posters, each of which shows one of history's great thinkers.

A copy of one or all of the posters is yours for the asking. See the back of this brochure for other details.

Intersil reserves the right to make changes in the circuitry or specifications contained herein at any time without notice.

Intersil assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

Intersil, Inc.
10710 N. Tantau Avenue
Cupertino, California 95014
U.S.A.
Tel: (408) 996-5000
TWX: 910-338-0171 (INTRSLINT CPTO)

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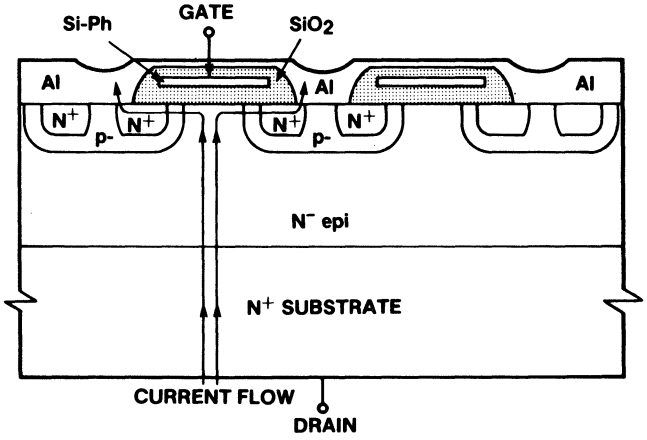
*Second Source Siliconix Devices

INTERSIL

Technology Description

Conventional VMOS devices begin to exhibit a high failure rate when operating at voltages greater than 150V, and the groove spacing required to allow such voltages makes the die size impractical. To alleviate these problems, Intersil has developed a vertical DMOS (double diffused MOS) process which is capable of handling voltages up to 800V. This structure, shown below, begins with an n^- epi layer grown on an n^+ substrate. Regions of p^- are then diffused, and inside these, regions of n^+. A silicon-gate is embedded in SiO_2 and the source and gate metallization are then added to complete the device. The current flow is at first vertical and then horizontal, with the drain on the n^+ substrate. The result is a structure which features both low ON resistance and low gate resistance.



Vertical DMOS Structure

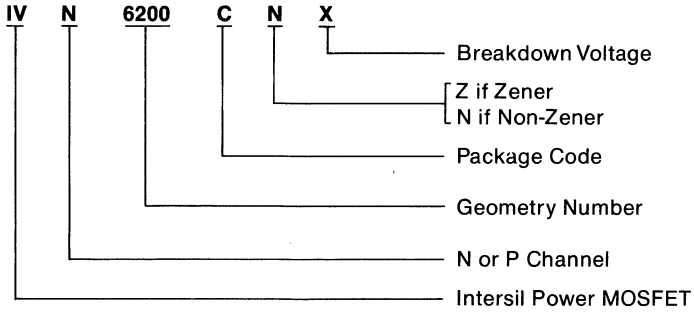
NOTE: Several different geometries have been developed, each to suit a particular requirement. The number in the lower right hand corner of the box containing the schematic, etc., refers to the specific geometry used for that device. See the geometry section in the back of the book.

INTERSIL

Intersil Part Numbering System

In addition to a wide assortment of second-source Power MOSFET devices, Intersil also manufactures products numbered according to the following system.

With the exception of parts in die and wafer form, part numbers are available as contained in the current Intersil OEM price list. Contact the nearest Intersil Sales Office or authorized representative for price and availability information on dice and wafers.



BREAKDOWN VOLTAGE

A	20	N	225
B	30	P	250
C	35	Q	300
D	40	R	350
E	60	S	400
F	80	T	450
G	90	U	500
H	100	V	600
J	125	W	700
K	150	X	800
L	175	Y	900
M	200	Z	1000

PACKAGE CODES

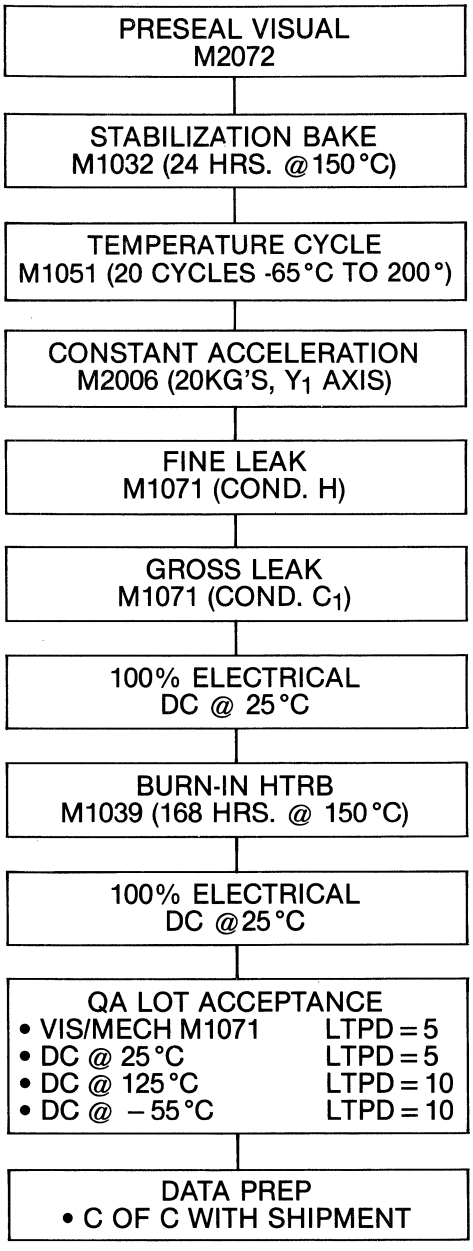
TO-237 (92+)	A
TO-202	B
TO-220	C
DICE	D
TO-66	H
TO-3	K
TO-52	S
TO-39	T
WAFER	W

Second-Source Part Numbers

Refer to current Intersil price list for available VN series part numbers.

Contact the nearest Intersil Sales Office or authorized representative for price and availability information on second-source dice and wafers.

/750 Optional Hi-Rel Process Flow



INTERSIL

POWER MOS CROSS-REFERENCE GUIDE

INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
2N4881	IVN6100TNS	IRF332	IVN6200KNS	IRF730	IVN6200CNS
2N4882	IVN6100TNS	IRF333	IVN6200KNS	IRF731	IVN6200CNS
2N4883	IVN6100TNS	IRF350	IVN6400KNS	IRF732	IVN6200CNS
2N4884	IVN6100TNS	IRF351	IVN6400KNS	IRF733	IVN6200CNS
2N4885	IVN6100TNS	IRF352	IVN6400KNS	IRF820	IVN6000CNU
2N4886	IVN6100TNS	IRF353	IVN6400KNS	IRF821	IVN6000CNT
2N6656	IVN5200KND	IRF420	IVN6000KNU	IRF822	IVN6000CNU
2N6657	IVN5200KNE	IRF421	IVN6000KNT	IRF823	IVN6000CNT
2N6658	IVN5200KNF	IRF422	IVN6000KNU	IRF830	IVN6200CNU
2N6659	2N6660	IRF423	IVN6000KNT	IRF831	IVN6200CNT
2N6660	2N6660	IRF430	IVN6200KNU	IRF832	IVN6200CNU
2N6661	2N6661	IRF431	IVN6200KNT	IRF833	IVN6200CNT
BD512	**	IRF432	IVN6200KNU	IRF9130	**
BD522	VN66AF	IRF433	IVN6200KNT	IRF9131	**
BS170	IVN5000AND	IRF450	IVN6400KNU	IRF9132	**
BS250	**	IRF451	IVN6400KNT	IRF9133	**
HPWR6501	IVN6400KNT	IRF452	IVN6400KNU	IRF9520	**
HPWR6502	IVN6400KNS	IRF453	IVN6400KNT	IRF9521	**
HPWR6503	IVN6200KNT	IRF510	IVN5201CNH	IRF9522	**
HPWR6504	IVN6200KNS	IRF511	IVN5201CNE	IRF9523	**
IRF120	IVN6200KNH	IRF512	IVN5201CNH	IRF9530	**
IRF121	IVN6200KNE	IRF513	IVN5201CNE	IRF9531	**
IRF122	IVN5201KNH	IRF520	IVN6200CNH	IRF9532	**
IRF123	IVN5201KNE	IRF521	IVN6200CNE	IRF9533	**
IRF130	IVN6200KNE	IRF522	IVN5200CNH	IVN5000AND	IVN5000AND
IRF131	IVN6200KNH	IRF523	IVN5200CNE	IVN5000ANE	IVN5000ANE
IRF132	IVN6200KNE	IRF530	IVN6200CNH	IVN5000ANF	IVN5000ANF
IRF133	IVN6200KNM	IRF531	IVN6200CNE	IVN5000ANH	IVN5000ANH
IRF150	**	IRF532	IVN6200CNH	IVN5000BND	**
IRF151	**	IRF533	IVN6200CNE	IVN5000BNE	**
IRF152	**	IRF610	IVN6100CNM	IVN5000BNF	**
IRF153	**	IRF611	IVN6100CNM	IVN5000SND	IVN5000SND
IRF220	IVN6200KNM	IRF612	IVN6100CNM	IVN5000SNE	IVN5000SNE
IRF221	IVN6200KNM	IRF613	IVN6100CNM	IVN5000SNF	IVN5000SNF
IRF222	IVN6200KNM	IRF620	IVN6200CNM	IVN5000SNH	IVN5000SNH
IRF223	IVN6200KNM	IRF621	IVN6200CNM	IVN5000TND	IVN5000TND
IRF230	IVN6200KNM	IRF622	IVN6200CNM	IVN5000TNE	IVN5000TNE
IRF231	IVN6200KNM	IRF623	IVN6200CNM	IVN5000TNF	IVN5000TNF
IRF232	IVN6200KNM	IRF630	IVN6200CNM	IVN5000TNH	IVN5000TNH
IRF233	IVN6200KNM	IRF631	IVN6200CNM	IVN5001AND	IVN5000AND
IRF250	IVN6400KNM	IRF632	IVN6200CNM	IVN5001ANE	IVN5001ANE
IRF251	IVN6400KNM	IRF633	IVN6200CNM	IVN5001ANF	IVN5001ANF
IRF252	IVN6400KNM	IRF710	IVN6000CNS	IVN5001ANH	IVN5001ANH
IRF253	IVN6400KNM	IRF711	IVN6000CNS	IVN5001BND	**
IRF320	IVN6000KNS	IRF712	IVN6000CNS	IVN5001BNE	**
IRF321	IVN6000KNS	IRF713	IVN6000CNS	IVN5001BNF	**
IRF322	IVN6000KNS	IRF720	IVN6000CNS	IVN5001SND	IVN5001SND
IRF323	IVN6000KNS	IRF721	IVN6000CNS	IVN5001SNE	IVN5001SNE
IRF330	IVN6200KNS	IRF722	IVN6000CNS	IVN5001SNF	IVN5001SNF
IRF331	IVN6200KNS	IRF723	IVN6000CNS	IVN5001SNH	IVN5001SNH

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INTERSIL

INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
IVN5001TND	IVN5001TND	IVN6200KNE	IVN6200KNE	SD205DB	VN66AK
IVN5001TNE	IVN5001TNE	IVN6200KNF	IVN6200KNF	SD220H	IVN5000TNE
IVN5001TNF	IVN5001TNF	IVN6200KNH	IVN6200KNH	VN0104N2	IVN5000TND
IVN5001TNH	IVN5001TNH	IVN6200KNM	IVN6200KNM	VN0104N3	IVN5000AND
IVN5200HND	IVN5200HND	IVN6200KNP	IVN6200KNP	VN0104N5	VN46AF
IVN5200HNE	IVN5200HNE	IVN6200KNS	IVN6200KNS	VN0106N2	VN67AK
IVN5200HNF	IVN5200HNF	IVN6200KNT	IVN6200KNT	VN0106N3	IVN5000ANE
IVN5200HNH	IVN5200HNH	IVN6200KNU	IVN6200KNU	VN0106N5	VN66AF
IVN5200KND	IVN5200KND	IVN6200KNW	IVN6200KNW	VN0106N6	VQ1000CJ
IVN5200KNE	IVN5200KNE	IVN6200KNX	IVN6200KNX	VN0108N2	VN99AK
IVN5200KNF	IVN5200KNF	IVN6300ANE	IVN6300ANE	VN0108N3	IVN5000ANF
IVN5200KNH	IVN5200KNH	IVN6300ANF	IVN6300ANF	VN0108N5	VN88AF
IVN5200TND	IVN5200TND	IVN6300ANH	IVN6300ANH	VN0108N6	**
IVN5200TNE	IVN5200TNE	IVN6300ANM	IVN6300ANM	VN0109N2	IVN5000TNH
IVN5200TNF	IVN5200TNF	IVN6300ANP	IVN6300ANP	VN0109N3	**
IVN5200TNH	IVN5200TNH	IVN6300ANS	IVN6300ANS	VN0109N5	**
IVN5201CND	IVN5201CND	IVN6300ANT	IVN6300ANT	VN0204N1	IVN5200KND
IVN5201CNE	IVN5201CNE	IVN6300ANU	IVN6300ANU	VN0204N2	IVN5000TND
IVN5201CNF	IVN5201CNF	IVN6300SNE	IVN6300SNE	VN0204N5	IVN5200CND
IVN5201CNH	IVN5201CNH	IVN6300SNF	IVN6300SNF	VN0206N1	IVN5200KNE
IVN5201HND	IVN5201HND	IVN6300SNH	IVN6300SNH	VN0206N2	IVN5000TNE
IVN5201HNE	IVN5201HNE	IVN6300SNM	IVN6300SNM	VN0206N5	IVN5200CNE
IVN5201HNF	IVN5201HNF	IVN6300SNP	IVN6300SNP	VN0208N1	IVN5200KNF
IVN5201HNH	IVN5201HNH	IVN6300SNS	IVN6300SNS	VN0208N2	IVN5000TNF
IVN5201KND	IVN5201KND	IVN6300SNT	IVN6300SNT	VN0208N5	IVN5200CNF
IVN5201KNE	IVN5201KNE	IVN6300SNU	IVN6300SNU	VN0209N1	IVN5200KNH
IVN5201KNF	IVN5201KNF	IVN6660	IVN6660	VN0209N2	IVN5000TNH
IVN5201KNH	IVN5201KNH	IVN6661	IVN6661	VN0209N5	IVN5200CNH
IVN5201TND	IVN5201TND	MTM1224	IVN6200KNE	VN0330N1	IVN6000KNR
IVN5201TNE	IVN5201TNE	MTM1225	IVN6200KNH	VN0330N2	IVN6000TNS
IVN5201TNF	IVN5201TNF	MTM474	IVN6200KNT	VN0330N5	IVN6000CNS
IVN5201TNH	IVN5201TNH	MTM475	IVN6200KNU	VN0335N1	IVN6000KNR
IVN6000CNS	IVN6200CNS	MTM564	IVN6200KNS	VN0335N2	IVN6000TNS
IVN6000CNT	IVN6000CNT	MTM565	IVN6200KNS	VN0335N5	IVN6000CNS
IVN6000CNU	IVN6000CNU	MTP1224	IVN6200CNE	VN0340N1	IVN6000KNS
IVN6000KNR	IVN6000KNR	MTP1225	IVN6200CNH	VN0340N2	IVN6000TNS
IVN6000KNS	IVN6000KNS	MTP474	IVN6200CNT	VN0340N5	IVN6000CNS
IVN6000KNT	IVN6000KNT	MTP475	IVN6200CNU	VN0345N1	IVN6000KNT
IVN6000KNU	IVN6000KNU	MTP564	IVN6200CNS	VN0345N2	IVN6000TNT
IVN6000TNS	IVN6000TNS	MTP565	IVN6200CNS	VN0345N5	IVN6000CNT
IVN6000TNT	IVN6000TNT	PV210	VN35AK	VN0430N1	IVN6200KNS
IVN6000TNU	IVN6000TNU	PV211	VN67AK	VN0435N1	IVN6200KNS
IVN6100TNS	IVN6100TNS	PV212	VN99AK	VN0440N1	IVN6200KNS
IVN6100TNT	IVN6100TNT	S75V02	**	VN0445N1	IVN6200KNT
IVN6100TNU	IVN6100TNU	S75V03	VN88AF	VN10KE	IVN6300SNE
IVN6200CNE	IVN6200CNE	SD1002KD	IVN6200KNT	VN10KM	VN10KM
IVN6200CNF	IVN6200CNF	SD1011KD	IVN6200KNS	VN1204N1	IVN5200KND
IVN6200CNH	IVN6200CNH	SD1012KD	IVN6200KNS	VN1204N2	IVN5200TND
IVN6200CNM	IVN6200CNM	SD1021KD	IVN6200KNS	VN1204N5	IVN5201CND
IVN6200CNP	IVN6200CNP	SD1100DD	IVN6100TNT	VN1206N1	IVN5200KNE
IVN6200CNS	IVN6200CNS	SD1100HD	IVN6100TNT	VN1206N2	IVN5200TNE
IVN6200CNT	IVN6200CNT	SD1101DD	IVN6100TNS	VN1206N5	IVN5201CNE
IVN6200CNU	IVN6200CNU	SD1101HD	IVN6100TNS	VN1208N1	IVN5200KNF
IVN6200CNW	IVN6200CNW	SD1200DD	IVN6300TNT	VN1208N2	IVN5200TNF
IVN6200CNX	IVN6200CNX	SD1201DD	IVN6300TNS	VN1208N5	IVN5201CNF

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INTERSIL

INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
VN1209N1	IVN5200KNH
VN1209N2	IVN5200TNH
VN1209N5	IVN5201CNH
VN1304N2	IVN5000TND
VN1304N3	IVN5000AND
VN1304N6	VQ1000CJ
VN1306N2	IVN5000TNE
VN1306N3	IVN5000AND
VN1306N6	VQ1000CJ
VN1308N2	IVN5000TNE
VN1308N3	IVN5000ANE
VN1308N6	**
VN1309N2	IVN5000TNH
VN1309N3	**
VN1309N6	**
VN30AB	VN30AB
VN33AK	VN35AK
VN3500A	IVN6200KNS
VN3501A	IVN6200KNS
VN35AB	VN35AB
VN35AK	VN35AK
VN4000A	IVN6200KNS
VN4001A	IVN6200KNS
VN40AF	VN40AF
VN46AF	VN46AF
VN64GA	IVN6200KNE
VN66AF	VN66AF
VN66AK	VN66AK
VN67AB	VN67AB
VN67AF	VN67AF
VN67AK	VN67AK
VN88AF	VN88AF
VN89AB	VN89AB
VN89AF	VN89AF
VN90AB	VN90AB

INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
VN98AK	VN98AK
VN99AK	VN99AK
VP0104N1	**
VP0104N2	**
VP0104N3	**
VP0104N5	**
VP0104N6	**
VP0106N1	**
VP0106N2	**
VP0106N3	**
VP0106N5	**
VP0106N6	**
VP0108N1	**
VP0108N2	**
VP0108N3	**
VP0108N5	**
VP0108N6	**
VP0109N1	**
VP0109N2	**
VP0109N3	**
VP0109N5	**
VP0109N6	**
VP0204N1	**
VP0204N2	**
VP0204N5	IVP5200CNE
VP0204N6	**
VP0206N1	**
VP0206N2	**
VP0206N5	IVP5200CNE
VP0206N6	**
VP0208N1	**
VP0208N2	**
VP0208N5	IVP5200CNH
VP0208N6	**
VP0208N6	**

INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
VP0209N1	**
VP0209N2	**
VP0209N6	**
VP1204N1	**
VP1204N2	**
VP1204N5	IVP5200CNE
VP1206N1	**
VP1206N2	**
VP1206N5	IVP5200CNE
VP1208N1	**
VP1208N2	**
VP1208N5	IVP5200CNF
VP1209N1	**
VP1209N2	**
VP1209N5	IVP5200CNH
VP1304N2	**
VP1304N6	**
VP1306N2	**
VP1306N6	**
VP1308N3	**
VP1308N6	**
VP1309N6	**
VQ1000CJ	VQ1000CJ

**Consult factory

INTERSIL

IVN5000/1 AN Series
IVN5000/1 SN Series
IVN5000/1 TN Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high peak current switching**
- **Inherent current sharing capability when paralleled**
- **Directly interfaces to CMOS, DTL, TTL logic**
- **Simple, straight-forward DC biasing**
- **Inherent protection from thermal runaway**
- **Reliable, low cost plastic package**

APPLICATIONS

- **LED and lamp drivers**
- **High gain, wide-band amplifiers**
- **High speed switches**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-source Voltage
- D devices 40V
- E devices 60V
- F devices 80V
- H devices 100V

Drain-gate Voltage
- D devices 40V
- E devices 60V
- F devices 80V
- H devices 100V

Continuous Drain Current (see note 1)
- AN devices 0.7A
- SN devices 0.9A
- TN devices 1.2A

Peak Drain Current (see note 2)
- AN devices 2.0A
- SN, TN devices 3.0A

Gate-source Forward Voltage ..... +30V

Gate-source Reverse Voltage ..... +30V

Thermal Resistance, Junction to Case
- AN devices ..... 62.5°C/W
- SN devices ..... 40°C/W
- TN devices ..... 20°C/W

Continous Device Dissipation at (or below) 25°C Case Temperature
- AN devices 2.0W
- SN devices 3.13W
- TN devices 6.25W

Linear Derating Factor
- AN device ..... 16mW/°C
- SN devices ..... 25mW/°C
- TN devices ..... 50mW/°C

Operating Junction Temperature Range .....−55°C to +150°C

Storage Temperature Range .....−55°C to +150°C

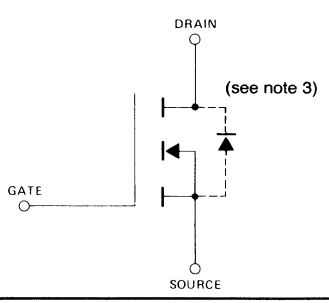
Lead Temperature (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

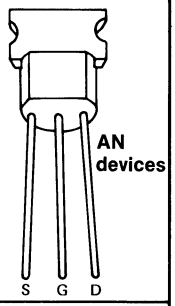
Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

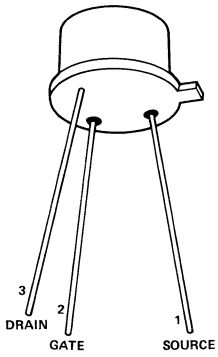
SCHEMATIC DIAGRAM



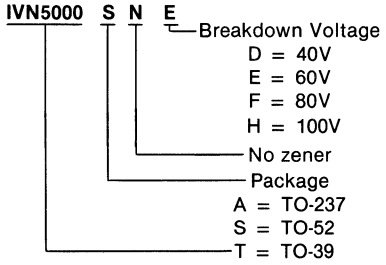
AN Series (TO-237)



SN Series (TO-52)
TN Series (TO-39)



ORDERING INFORMATION



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0

	CHARACTERISTICS			IVN5000 IVN5001 MIN	TYP	MAX	UNIT	TEST CONDITIONS	
STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	D Devices	40			V	V_{GS} = 0, I_D = 10μA	
			E Devices	60					
			F Devices	80					
			H Devices	100					
	$V_{GS(th)}$	Gate Threshold Voltage	IVN5000 Series	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA	
			IVN5001 Series	0.8		3.6			
	I_{GSS}	Gate-Body Leakage				10	nA	V_{GS} = 15V, V_{DS} = 0	
						50		V_{GS} = 15V, V_{DS} = 0, T_A = +125°C	
	I_{DSS}	Zero Gate Voltage Drain Current				10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
						500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C	
	$I_{D(on)}$	ON-State Drain Current	IVN5000 Series	1.0	1.9		A	V_{DS} = 24V, V_{DS} = 10V	(Note1)
			IVN5001 Series	1.0	1.9			V_{GS} = 24V, V_{GS} = 12V	
	$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5000 Series		2.0	2.5	V	V_{GS} = 10V, I_D = 1.0A	
			IVN5001 Series		1.9	2.5		V_{GS} = 12V, I_D = 1.0A	
	$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5000 Series		2.0	2.5	Ω	V_{GS} = 10V, I_D = 1.0A	
			IVN5001 Series		1.9	2.5		V_{GS} = 12V, I_D = 1.0A	
DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		V_{GS} = 10V, I_D = 1.0A, f = 1KHz	
			IVN5001 Series		1.9	2.5		V_{GS} = 12V, I_D = 1.0A, f = 1KHz	
	gfs	Forward Transconductance		170	280		mmho	V_{DS} = 24V, I_D = 0.5A, f = 1KHz	
	C_{iss}	Input Capacitance			40	50	pF	V_{DS} = 24V, V_{GS} = 0, f = 1MHz	(Note2)
	C_{oss}	Output Capacitance			27	40			
	C_{rss}	Reverse Transfer Capacitance			6	10			
	$t_{d(on)}$	Turn-ON Delay Time			2	5	ns	See Switching Times Test Circuit	(Note2)
	t_r	Rise Time			2	5			
	$t_{d(off)}$	Turn-OFF Delay Time			2	5			
	t_f	Fall Time			2	5			

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

Note: For other 5000 family characteristic curves, see page

INTERSIL

IVN5200/1 HN Series
IVN5200/1 KN Series
IVN5200/1 TN Series
n-Channel Enhancement-mode Vertical Power MOSFETs

FEATURES

- High speed, high current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Extended safe operating area
- Inherently temperature stable
- Low ON resistance in small package

APPLICATIONS

- High efficiency switching power supplies
- Off-line switching regulators
- High speed, high current switches
- Line drivers
- Logic buffers
- High peak current pulse amplifiers
- DC motor controllers

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-source Voltage
- D devices 40V
- E devices 60V
- F devices 80V
- H devices 100V

Drain-gate Voltage
- D devices 40V
- E devices 60V
- F devices 80V
- H devices 100V

Continuous Drain Current (see note 1)
- HN, KN devices 5.0A
- TN devices 4.0A

Peak Drain Current (see note 2)
- HN, KN devices 12A
- TN devices 10.0A

Gate-source Forward Voltage ..... +30V

Gate-source Reverse Voltage ..... −30V

Thermal Resistance, Junction to Case
- HN devices ..... 4.17°C/W
- KN devices ..... 2.5°C/W
- TN devices ..... 10°C/W

Continuous Device Dissipation at (or below) 25°C Case Temperature
- HN devices 30W
- KN devices 50W
- TN devices 12.5W

Linear Derating Factor
- HN devices ..... 240mW/°C
- KN devices ..... 400mW/°C
- TN devices ..... 100mW/°C

Operating Junction Temperature Range ..... −55°C to +150°C

Storage Temperature Range ..... −55°C to +150°C

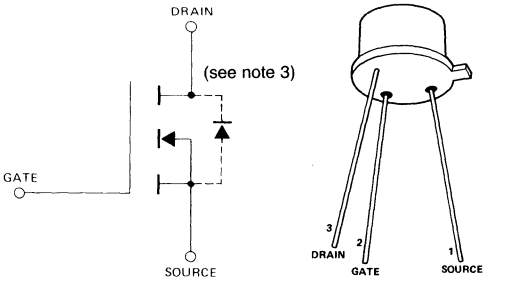
Lead Temperature (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

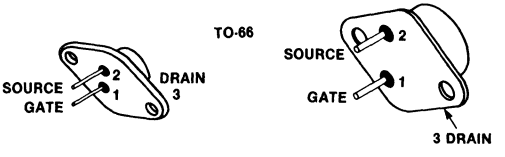
Note 2. Pulse width 80μsec, duty cycle 1.0%.

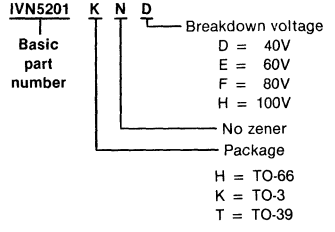
Note 3. The Drain-source diode is an itegral part of the MOSFET structure.

SCHEMATIC DIAGRAM — **TN SERIES (TO-39)**



HN SERIES (TO-66) — **KN SERIES (TO-3)**





5200

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0

CHARACTERISTICS			MIN	TYP	MAX	UNIT	TEST CONDITIONS	
BV_{DSS}	Drain-Source Breakdown Voltage	D devices	40			V	V_{GS} = 0, I_D = 100μA	
		E devices	60					
		F devices	80					
		H devices	100					
$V_{GS(th)}$	Gate Threshold Voltage	IVN5200 Series	0.8		2.0		V_{DS} = V_{GS}, I_D = 5mA	
		IVN5201 Series	0.8		3.6			
I_{GSS}	Gate-Body Leakage			0.2	20	nA	V_{GS} = 12V, V_{DS} = 0	
					100		V_{GS} = 12V, V_{DS} = 0, T_A = +125°C	
I_{DSS}	Zero Gate Voltage Drain Current				100	μA	V_{DS} = Max. Rating, V_{GS} = 0	
					5.0	mA	V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C	
$I_{D(on)}$	ON-State Drain Current	IVN5200 Series	5.0	10		A	V_{DS} = 24V, V_{GS} = 10V	
		IVN5201 Series	5.0	10			V_{DS} = 24V, V_{GS} = 12V	
$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5200 Series		1.9	2.5	V	V_{GS} = 10V, I_D = 5.0A	(Note 1)
		IVN5201 Series		1.8	2.5		V_{GS} = 12V, I_D = 5.0A	
$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5200 Series		0.38	0.50	Ω	V_{GS} = 10V, I_D = 5.0A	
		IVN5201 Series		0.36	0.50		V_{GS} = 12V, I_D = 5.0A	
$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		V_{GS} = 10V, I_D = 5.0A, f = 1KHz	
		IVN5201 Series		0.36	0.50		V_{GS} = 12V, I_D = 5.0A, f = 1KHz	
g_{fs}	Forward Transconductance		1.0	1.8		mho	V_{DS} = 24V, I_D = 5.0A, f = 1KHz	
C_{iss}	Input Capacitance			210	250	pF	V_{DS} = 24V, V_{GS} = 0, f = 1MHz	(Note 2)
C_{oss}	Output Capacitance			160	200			
C_{rss}	Reverse Transfer Capacitance			45	60			
$t_{d(on)}$	Turn-ON Delay Time			4	20	ns	I_D = 4.0A See Switching Times Test Circuit	(Note 2)
t_r	Rise Time			4	20			
$t_{d(off)}$	Turn-OFF Delay Time			4	20			
t_f	Fall Time			4	20			

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

INTERSIL

IVN5201 CN Series n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high current switching**
- **Inherent current sharing capability when paralleled**
- **Directly interfaces to CMOS, DTL, TTL logic**
- **Simple, straight-forward DC biasing**
- **Extended safe operating area**
- **Reliable, low cost plastic package**

APPLICATIONS

- **Deflection coil drivers**
- **Off-line switching regulators**
- **Power amplifiers**
- **DC to DC inverters**
- **Motor controllers**
- **High current line drivers**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-source Voltage
- IVN5201CND 40V
- IVN5201CNE 60V
- IVN5201CNF 80V
- IVN5201CNH 100V

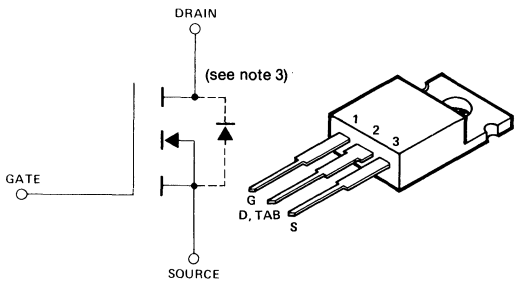
Drain-gate Voltage
- IVN5201CND 40V
- IVN5201CNE 60V
- IVN5201CNF 80V
- IVN5201CNH 100V

Continuous Drain Current (see note 1) 5.0A
Peak Drain Current (see note 2) 12A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... −30V
Thermal Resistance, Junction to Case ... 4.17°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 30W

Linear Derating Factor ..... 240mW/°C
Operating Junction
- Temperature Range ..... −55°C to +150°C

Storage Temperature Range .... −55°C to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

SCHEMATIC DIAGRAM (TO-220)



5200

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Maximum pulse width 80msec, maximum duty cycle 1.0%.

Note 3. The Drain-source diode is an integral par of teh MOSFET structure.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted),

	CHARACTERISTICS			IVN5201CND MIN	IVN5201CND TYP	IVN5201CND MAX	UNIT	TEST CONDITIONS	
STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	D devices	40			V	V_{GS} = 0, I_D = 100mA	
			E devices	60					
			F devices	80					
			H devices	100					
	$V_{GS(th)}$	Gate Threshold Voltage		0.8		3.6		V_{DS} = V_{GS}, I_D = 5mA	
	I_{GSS}	Gate-Body Leakage			0.2	20	nA	V_{GS} = 12V, V_{DS} = 0	
						100		V_{GS} = 12V, V_{DS} = 0, T_A = +125°C	
	I_{DSS}	Zero Gate Voltage Drain Current				100	mA	V_{DS} = Max. Rating, V_{GS} = 0	
						5.0	mA	V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C	
	$I_{D(on)}$	ON-State Drain Current		5.0	10		A	V_{DS} = 24V, V_{GS} = 12V	(Note 1)
	$V_{DS(on)}$	Drain-Source Saturation Voltage			1.8	2.5	V	V_{GS} = 12V, I_D = 5.0A	
	$r_{DS(on)}$	Static Drain-Source ON Resistance			0.36	0.50	Ω	V_{GS} = 12V, I_D = 5.0A	
DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance			0.36	0.50		V_{GS} = 12V, I_D = 5.0A f = 1KHz	
	g_{fs}	Forward Transconductance		1.0	1.8		mho	V_{DS} = 24V, I_D = 5.0A, f = 1KHz	
	C_{iss}	Input Capacitance			210	250	pF	V_{DS} = 24V, V_{GS} = 0, f = 1MHz	(Note 2)
	C_{oss}	Output Capacitance			160	200			
	C_{rss}	Reverse Transfer Capacitance			45	60			
	$t_{d(on)}$	Turn-ON Delay Time			4	20	ns	I_D = 4.0A See Switching Times Test Circuit,	(Note 2)
	t_r	Rise Time			4	20			
	$t_{d(off)}$	Turn-OFF Delay Time			4	20			
	t_f	Fall Time			4	20			

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

INTERSIL

IVN6000 CN Series
IVN6000 TN Series
500V n-Channel Enhancement-mode Vertical Power MOSFETs

FEATURES

- **High speed, high current switching**
- **Inherent current sharing capability when paralleled**
- **Directly interfaces to CMOS logic**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **Motor controllers**
- **Power amplifiers**
- **RF amplifiers**

ABSOLUTE MAXIMUM RATINGS
(T_A = 25° C unless otherwise noted)

Drain-source Voltage
- IVN6000 CNS, TNS 400V
- IVN6000 CNT, TNT 450V
- IVN6000 CNU, TNU 500V

Drain-gate Voltage
- IVN6000 CNS, TNS 400V
- IVN6000 CNT, TNT 450V
- IVN6000 CNU, TNU 500V

Continuous Drain Current
- IVN6000 CNS, CNT 2A
- IVN6000 CNU 1.75A
- IVN6000 TNS, TNT 1.0A
- IVN6000 TNU 0.9A

Peak Drain Current (see note)
- CN devices 6A
- TN devices 3A

Gate-source Voltage ..... ± 30V

Thermal Resistance, Junction to Case
- CN devices ..... 4.17°C/W
- TN devices ..... 10°C/W

Continuous Device Dissipation at (or below)
- 25°C Case Temperature, CN devices 30W
- TN devices 12.5W

Linear Derating Factor
- CN devices ..... 240mW/°C
- TN devices ..... 100mW/°C

Operating Junction
- Temperature Range ..... − 55°C to + 150°C

Storage Temperature Range .... − 55°C to + 150°C

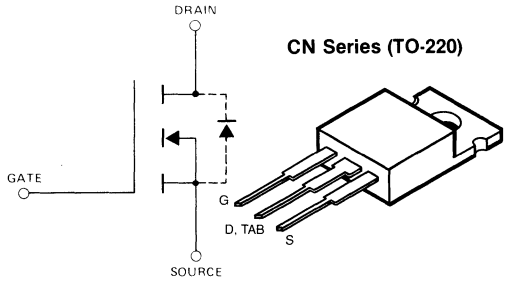
Lead Temperature
- (1/16″ in. from case for 10 sec) ..... + 300°C

Reverse Diode Continuous Forward Current
- CN devices 2A
- TN devices 1A

Reverse Diode Peak Forward Current
- CN devices 6A
- TN devices 3A

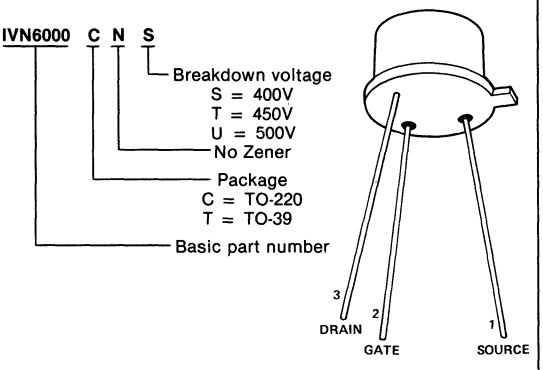
Note: Maximum pulse width 80 μsec, maximum duty cycle 1.0%

SCHEMATIC DIAGRAM



Body internally connected to source.
Drain common to case.

ORDERING INFORMATION **TN Series (TO-39)**



6000

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 100 μA					
IVN6000 CNS, TNS				400			V
IVN6000 CNT, TNT				450			
IVN6000 CNU, TNU				500			
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10mA		2		5	
Gate-Body Leakage Current	I_{GSS}	V_{GS} = 30V			10	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Maximum Rating, V_{GS} = 0V, T_J = 125°C			0.2	2	mA
ON Drain Current[1]	$I_{D(on)}$	V_{DS} = 50V, V_{GS} = 15V	CN devices	4			A
			TN devices	3			
Static-Drain Source ON Resistance[1]							
IVN6000 CNS, CNT	$r_{DS(on)}$	V_{GS} = 15V, I_D = 1A				3.5	Ω
IVN6000 CNU						4.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 200V, I_D = 1.5A		0.8	0.9		mho
Input Capacitance	C_{iss}	V_{DS} = 100V, f = 1.0 MHz, V_{GS} = 0V			220	300	pF
Output Capacitance	C_{oss}				22	30	
Reverse Transfer Capacitance	C_{rss}				6	10	
Rise Time	t_r	V_{DS} = 200V, I_D = 1.0A, V_{GS} = 15V, R_{gen} = 6Ω				10	ns
Fall Time	t_f					10	ns
Slew Rate	SR	V_{GS} = 0V, V_{DS} = 300V			100		V/ns

Note: 1. Pulse Test: 80μs, 1% duty cycle

REVERSE DIODE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Forward Voltage Drop	V_f	Forward Current = 2A		0.95	1.2	V
Reverse Recovery Time	t_{rr}	$I_{fwd(pk)}$ = $I_{rev(pk)}$ Recovery to 50%		100		ns
Recovered Charge	Q_{rr}	T_J = 150°C, $I_{fwd(pk)}$ = 2A		200		nC

INTERSIL

IVN6000 KN Series 500V n-Channel Enhancement-mode Vertical Power MOS FETs

FEATURES

- **High speed, high current switching**
- **Inherent current sharing capability when paralleled**
- **Directly interfaces to CMOS logic**
- **Simple, straight-forward DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **Motor controllers**
- **Power amplifiers**
- **RF amplifiers**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-source Voltage
- IVN6000KNR 350V
- IVN6000KNS 400V
- IVN6000KNT 450V
- IVN6000KNU 500V

Drain-gate Voltage
- IVN6000KNR 350V
- IVN6000KNS 400V
- IVN6000KNT 450V
- IVN6000KNU 500V

Continuous Drain Current (see note 1) 2.5A
- KNU only 2.0A

Peak Drain Current (see note 2) 7.5A
Gate-source Voltage ..... ±30V
Thermal Resistance Junction to Case ..... 3.0°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 41.7W

Linear Derating Factor ..... 333mW/°C
Operating Junction
- Temperature Range ..... −55°C to +150°C

Storage Temperature Range ..... −55°C to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

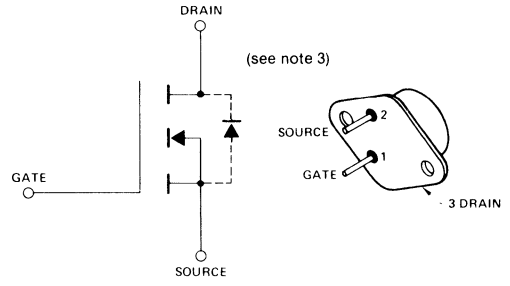
Body-drain Diode Continuous Forward Current ... 3A
Body-drain Diode Peak Forward Current 10A

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Maximum pulse width 80sec, maximum duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (TO-3)



6000

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Drain-Source Breakdown Voltage IVN6000KNR	BV_{DSS}	$V_{GS} = 0V$, $I_D = 100\mu A$	350			V
IVN6000KNS			400			
IVN6000KNT			450			
IVN6000KNU			500			
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 10$ mA	1.5		5	
Gate-Body Leakage Current	I_{GSS}	$V_{GS} = 30$ V		10	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Maximum Rating, $V_{GS} = 0V$, $T_J = 125°C$		0.2	2	mA
ON Drain Current[1]	$I_{D(on)}$	$V_{DS} = 25V$, $V_{GS} = 15V$	5	7		A
		KNU	4	6		
Static-Drain Source ON Resistance[1]	$r_{DS(on)}$	$V_{GS} = 15V$, $I_D = 1A$		2.5	3.0	Ω
		KNU		3.5	4.0	
Forward Transconductance[1]	g_{fs}	$V_{DS} = 200V$, $I_D = 1.5A$	0.8	1.0		mho
Input Capacitance	C_{iss}	$V_{DS} = 100V$, f = 1.0 MHz, $V_{GS} = 0V$		220	300	pF
Output Capacitance	C_{oss}			22	30	
Reverse Transfer Capacitance	C_{rss}			6	10	
Rise Time	t_r	$V_{DS} = 200V$, $I_D = 1.0A$, $V_{GS} = 15V$, $R_{gen} = 6\Omega$		5	10	ns
Fall Time	t_f			5	10	ns
Slew Rate	SR	$V_{DS} = 400V$, $V_{GS} = 0$		100		V/ns

Note: 1. Pulse Test: 80μs, 1% duty cycle.

BODY-DRAIN DIODE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Forward Voltage Drop	V_f	Peak Forward Current = 2A		0.95	1.1	V
Reverse Recovery Time	t_{rr}	$I_{fwd(pk)} = I_{rev(pk)}$ Recovery to 50%		100		ns
Recovered Charge	Q_{rr}	$T_J = 150°C$, $I_{fwd(pk)} = 2A$		200		nC

INTERSIL

IVN6100 TN Series 500V n-Channel Enhancement-mode Vertical Power MOS FETs

FEATURES

- **High breakdown voltage**
- **Very low input capacitance**
- **Extremely fast switching**
- **Low OFF leakage**
- **Direct interface with CMOS, TTL logic**
- **Extended safe operating area**

APPLICATIONS

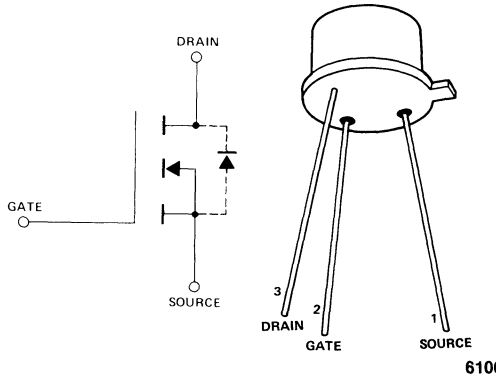
- **Telecommunications**
- **High voltage signal processing**
- **Logic interfaces**
- **Display drivers**
- **Electrostatic printers**
- **Pulse generators**

ABSOLUTE MAXIMUM RATINGS

Drain-source Breakdown Voltage
- TNS 400V
- TNT 450V
- TNU 500V

Continuous Drain Current 0.3A
Peak Drain Current 3A
Gate-Source Voltage . . . . . ±30V
Thermal Resistance, Junction to Case . . . . . 20°C/W
Continuous Device Dissipation (25°C Case Temp) 6.25W
Linear Derating Factor . . . . . 50mW/°C

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Drain-source breakdown voltage	BV_{DSS}	V_{GS} = 0V, I_D = 100μA	TNS	400			
			TNT	450			
			TNU	500			
Static ON Resistance	$r_{DS(on)}$	I_D = 5A, V_{GS} = 15V				15	Ω
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 5mA		1		5	V
Forward Transconductance	g_{fs}	I_D = 1A V_{DS} = 200V		250	300		mmho
ON Drain Current	$I_{D(on)}$	V_{DS} = 25V, V_{GS} = 15V		1			A
Zero Gate Voltage Drain Current		V_{DS} = V_{GS} = 0, T_J = 125°C			0.1	1	mA
Rise Time	t_r	V_{DS} = 200V, I_D = 1.0A				10	ns
Fall Time	t_f	V_{GS} = 15V, R_{gen} = 6Ω				10	ns
Slew Rate	SR	V_{DS} = 350V			100		V/ns
Input Capacitance	C_{iss}	f = 1.0 MHz				80	pF
Output Capacitance	C_{oss}	V_{DS} = 100V				15	pF
Reverse Transfer Capacitance	C_{rss}	V_{GS} = 0V				13	pF

INTERSIL

IVN6200 CN Series
IVN6200 KN Series
n-Channel Enhancement-mode Vertical Power MOSFETs

FEATURES

- **High speed, high current switching**
- **Inherent current sharing capability when paralled**
- **Directly Interfaces to CMOS logic**
- **Simple, straight-forward DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC Inverters**
- **Motor controllers**
- **Power amplifiers**
- **RF amplifiers**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-source and Drain-gate Voltage
- E devices 60V
- F devices 80V
- H devices 100V
- M devices 200V
- P devices 250V
- S devices 400V
- T devices 450V
- U devices 500V
- W devices 700V
- X devices 800V

Continuous Drain Current (see note 1)
- E, F, H, M, P devices 10A
- S, T, U devices 5A
- W devices 3A
- X devices 2.5A

Peak Drain Current (see note 2)
- E, F, H, M, P devices 20A
- S, T, U devices 15mA
- W, X devices 7.5A

Gate-source Voltage ..... ±30V

Thermal Resistance, Junction to Case ..... 1.25°C/W

Continuous Device Dissipation at (or below)
- 25°C Case Temperature 100W

Linear Derating Factor ..... 800mW/°C

Operating Junction
- Temperature Range ..... −55°C to +150°C

Storage Temperature ..... −55°C to +150°C

Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Body-Drain Diode Continuous Forward Current
- E, F, H, M, P devices 10A
- S, T, U devices 5A
- W, X devices 3A

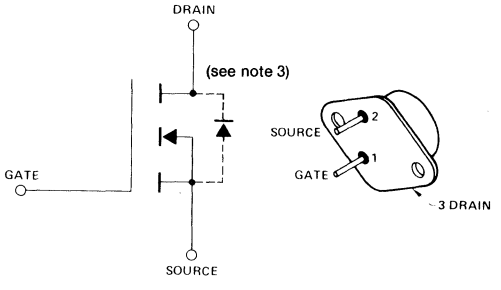
Body-Drain Diode Peak Forward Current
- E, F, H, M, P devices 20A
- S, T, U devices 15A
- W, X devices 7.5A

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

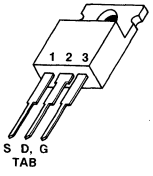
Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM — KN SERIES (TO-3)



CN SERIES (TO-220)



ORDERING INFORMATION

IVN6200 C N P

P — Breakdown Voltage
- E = 60V, S = 400V
- F = 80V, T = 450V
- H = 100V, U = 500V
- M = 200V, W = 700V
- P = 250V, X = 800V

N — No Zener

C — Package
- C = TO-220
- K = TO-3

IVN6200 — Basic Part Number

6200

IVN6200 CN Series
KN Series

INTERSIL

OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Drain Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 100μA	E devices	60			V
			F devices	80			
			H devices	100			
			M devices	200			
			P devices	250			
			S devices	400			
			T devices	450			
			U devices	500			
			W devices	700			
			X devices	800			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10mA	E,F,H devices	0.8		2.5	V
			all others	2		5	
Gate-Body Leakage Current	I_{GSS}	V_{GS} = 30V				250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = maximum rating, V_{GS} = 0V, T_J = +125°C				4	mA
ON Drain Current[1]	$I_{D(on)}$	V_{DS} = 15V	(E,F,H devices) V_{DS} = 25V	15			A
			(M,P,S,T,U devices) V_{DS} = 100V	10			
			V_{DS} = 100V W devices	3.0			
			X devices	2.5			
Static Drain-Source ON Resistance[1]	$r_{DS(on)}$	V_{GS} = 15V, I_D = 1A	E,F,H devices			0.2	Ω
			M,P devices			0.5	
			S,T,U devices			1.5	
			W devices			5	
			X devices			6	
Forward Transconductance[1]	g_{fs}	I_D = 2.5A	V_{DS} = 50V (E,F,H devices) V_{DS} = 100V (M,P devices) V_{DS} = 200V (S,T,U,W,X devices)	1.5			mho
Input Capacitance	C_{iss}		V_{DS} = 50V (E,F,H devices only)			600	
			V_{DS} = 100V (all others)				
Output Capacitance	C_{oss}	V_{GS} = 0V, f = 1MHz	E,F,H devices			100	pF
			M,P devices			80	
			S,T,U devices			60	
			W,X devices			50	
Reverse Transfer Capacitance	C_{rss}		E,F,H devices			40	
			M,P devices			30	
			S,T,U,W,X devices			20	
Rise Time	t_r	I_D = 1A, V_{GS} = 15V, R_{gen} = 6Ω, V_{DS} = 50V (E,F,H devices)				20	
Fall Time	t_f	V_{DS} = 100V (M,P devices), V_{DS} = 350V (S,T,U devices), V_{DS} = 600V (W,X devices)				20	ns
Slew Rate	SR	V_{GS} = 0	V_{DS} = 50V E,F,H devices		25		V/ns
			V_{DS} = 100V M,P devices		50		
			V_{GS} = 350V S,T,U devices		100		
			V_{DS} = 600V W,X devices		100		

Body-Drain Diode Characteristics

Forward Voltage Drop	V_f	$I_{fwd(pk)}$ = 2A	E,F,H devices			0.9	V
			M,P devices			0.95	
			S,T,U,W,X devices			1.0	
Reverse Recovery Time	t_{rr}	$I_{fwd(pk)}$ = $I_{rev(pk)}$ Recovery to 50%			200		ns
Recovered Charge	Q_{rr}	T_J = 150°C, $I_{fwd(pk)}$ = 2A			400		nC

[1] Pulse Test, 80μs, 1% duty cycle.

INTERSIL

IVN6300 AN Series
IVN6300 SN Series
n-Channel Enhancement-mode Vertical Power MOS FETs

FEATURES

- High breakdown voltage
- Very low input capacitance
- Extremely fast switching
- Low OFF leakage
- Direct interface with CMOS, TTL logic
- Extended safe operating area

APPLICATIONS

- Telecommunications
- High voltage signal processing
- Logic interfaces
- Display drivers
- Electrostatic printers
- Pulse generators

ABSOLUTE MAXIMUM RATINGS
(T_A = 25 °C unless otherwise noted)

Drain-source and Drain-gate voltage
- E devices 60V
- F devices 80V
- H devices 100V
- M devices 200V
- P devices 250V
- S devices 400V
- T devices 450V
- U devices 500V

Continuous Drain Current (see note 1)
- E, F, H devices 250mA
- M, P devices 120mA
- S, T, U devices 100mA

Peak Drain Current (see note 2)
- E, F, H devices 700mA
- M, P devices 350mA
- S, T, U devices 300mA

Gate-source Voltage ..... ±30V
Thermal Resistance, Junction to Case ..... 83.3°C/W
Continuous Device Dissipation at (25°C) 1.5W
Linear Derating Factor ..... 12mW/°C
Operating Junction Temperature Range ..... −55°C to +150°C
Lead Temperature (1/16 in. from case for 10 sec) ..... +300°C

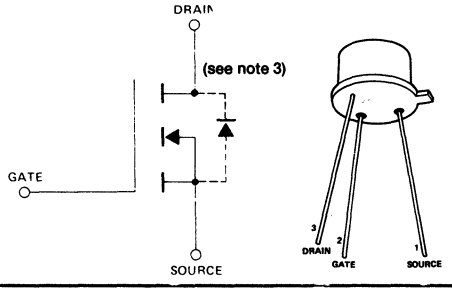
Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

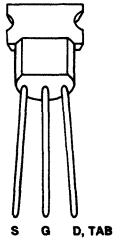
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM

SN SERIES (TO-52)



ORDERING INFORMATION



AN SERIES (TO-237)

IVN6300 A N M

- M: Breakdown Voltage
  - E = 60V P = 250V
  - F = 80V S = 400V
  - H = 100V T = 450V
  - M = 200V U = 500V
- N: No Zener
- A: Package
  - A = TO-237
  - S = TO-52
- IVN6300: Basic Part Number

6300

INTERSIL

OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Drain Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 10μA	E devices	60			V
			F devices	80			
			H devices	100			
			M devices	200			
			P devices	250			
			S devices	400			
			T devices	450			
			U devices	500			
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1mA		1		3	V
Gate-Body Leakage Current	I_{GSS}	V_{GS} = 30V			0.2	50	nA
ON Drain Current	$I_{D(on)}$	V_{DS} = 50V, V_{OS} = 10V	E,F,H devices	700			mA
			M,P devices	350			
			S,T,U devices	300			
Static Drain-Source ON Resistance	$r_{DS(on)}$	V_{GS} = 10V, I_D = 0.1A	E,F,H device			7.5	Ω
			M,P devices			25	
			S,T,U devices			75	
Forward Transconductance	g_{fs}	V_{DS} = 50V, I_{DS} = 0.1A		80	100		mmho
Input Capacitance	C_{iss}	f = 1MHz, V_{GS} = 0V	V_{DS} = 35V (E,F,H devices) V_{DS} = 50V (M,P devices) V_{DS} = 100V (S,T,U devices)		20	30	pF
Output Capacitance	C_{oss}				3	5	
Reverse Transfer Capacitance	C_{rss}				2	3	
Rise Time	t_r	V_{GS} = 15V, R_{gen} = 6Ω	V_{DS} = 50V (E,F,H devices) V_{DS} = 100V (M,P devices) V_{DS} = 200V (S,T,U devices)			10	ns
Fall Time	t_f	V_{GS} = 15V, R_{gen} = 6Ω				10	
Slew Rate	S_R	80% rated V_{DSS}		100			V/ns

INTERSIL

2N6660/1 n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **Simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**
- **Typical t_{on} and t_{off} < 5ns**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**
- **High frequency linear amplifiers**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-source Voltage
- 2N6660 ..... 60V
- 2N6661 ..... 90V

Drain-gate Voltage
- 2N6660 ..... 60V
- 2N6661 ..... 90V

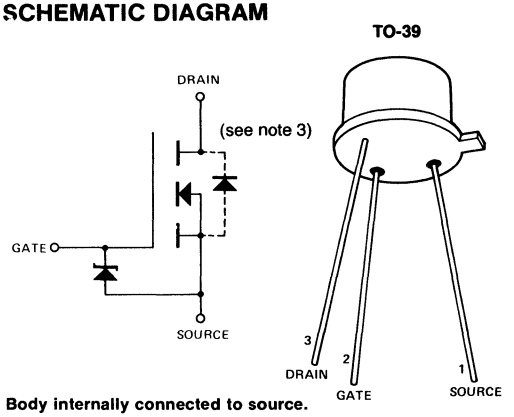
Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage 15V
Gate-source Reverse Voltage 0.3V
Thermal Resistance, Junction to Case ..... 20°C/W
Continuous Device Dissipation at (or below)
25°C Case Temperature 6.25W
Linear Derating Factor ..... 50mW/°C
Operating Junction
Temperature Range ..... −55°C to +150°C
Storage Temperature Range .... −55°C to +150°C
Lead Temperature
(1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM



Body internally connected to source.
Drain common to case.

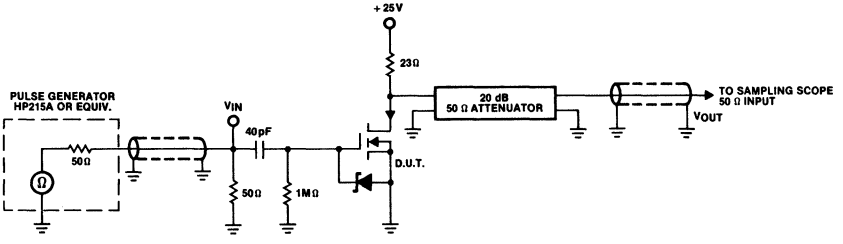
5000Z

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

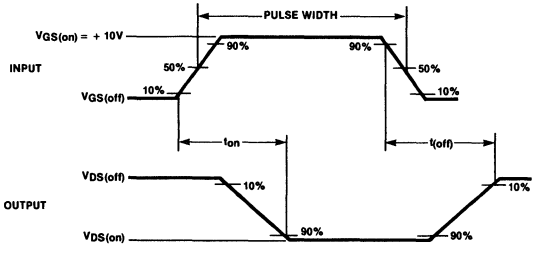
	CHARACTERISTICS		MIN	TYP	MAX	UNIT	TEST CONDITIONS	
STATIC	BV_{DSS}	Drain-source Breakdown Voltage	2N6660		90	V	V_{GS} = 0, I_D = 10μA	
			2N6661		60			
			2N6660		90		V_{DS} = 0, I_D = 2.5mA	
			2N6661		60			
	$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA	
	I_{GSS}	Gate-Body Leakage		0.5	100	nA	V_{GS} = 15V, V_{DS} = 0	
					500		V_{GS} = 15V, V_{DS} = 0, T_A = 125°C	(Note 2)
	I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
					500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
				100		nA	V_{DS} = 25V, V_{GS} = 0	
	$I_{D(on)}$	ON-State Drain Current	1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	(Note 1)
	$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3		V	V_{GS} = 5V, I_D = 0.1A	
				1.0	1.5		V_{GS} = 5V, I_D = 0.3A	
				0.9			V_{GS} = 10V, I_D = 0.5A	
				2.2	3.0		V_{GS} = 10V, I_D = 1.0A	
	$r_{DS(on)}$	Static Drain-Source ON-State Resistance		2.2	3.0	Ω	V_{GS} = 10V, I_D = 1.0A	
DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON-State Resistance		2.2	3.0	Ω	V_{GS} = 10V, I_D = 1.0A, f = 1KHz	
	g_{fs}	Forward Transconductance	170	250		mmho	V_{DS} = 24V, I_D = 0.5A	
	C_{iss}	Input Capacitance			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0MHz	(Note 2)
	C_{ds}	Drain-Source Capacitance			40			
	C_{rss}	Reverse Transfer Capacitance			10		V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz	
					35		V_{GS} = 0, V_{DS} = 0, f = 1.0MHz	
	$t_{d(on)}$	Turn-ON Delay Time		2	5	ns	See Switching Test Circuit	
	t_r	Rise Time		2	5			
	$t_{d(off)}$	Turn-OFF Delay Time		2	5			
	t_f	Fall Time		2	5			

Note 1. Pulse test — 80μsec pulse, 1% duty cycle. **Note 2.** Sample test.

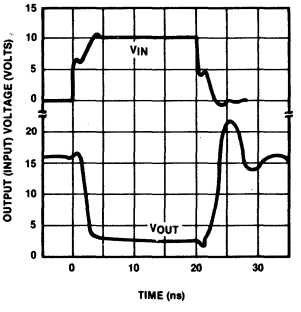
Switching Time Test Circuit



Switching Time Test Waveforms



Switching Waveforms



INTERSIL

VN10 KM
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **Directly drives inductive loads**
- **High speed, high peak current switching**
- **Inherent current sharing capability when paralleled**
- **Directly interfaces to CMOS, DTL, TTL logic**
- **Simple, straight-forward DC biasing**
- **Inherent protection from thermal runaway**

APPLICATIONS

- **LED and lamp drivers**
- **TTL and CMOS to high current interface**
- **High speed switches**
- **Line drivers**
- **Relay drivers**
- **Transformer drivers**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

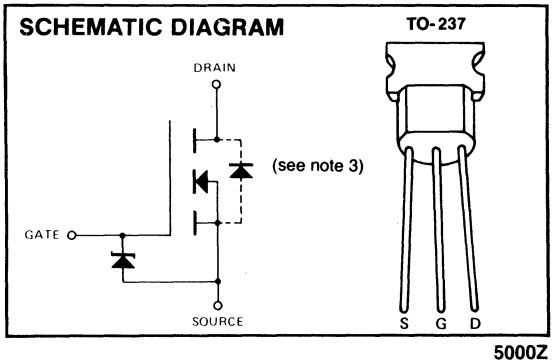
Drain-source Voltage 60V
Drain-gate Voltage 60V
Continuous Drain Current (see note 1) 0.5A
Peak Drain Current (see note 2) 1.0A
Gate-source Forward Voltage ..... +15V
Gate-source Reverse Voltage 0.3V
Continuous Device Dissipation at (or below) 25°C Case Temperature 1.0W
Linear Derating Factor ..... 8mW/°C
Operating Junction Temperature Range ..... – 40°C to + 150°C
Storage Temperature Range ..... – 40°C to + 150°C
Lead Temperature (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C, controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM



5000Z

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic		Min	Typ	Max	Unit	Test Conditions	
STATIC	BV_{DSS}	Drain-Source Breakdown	60			V	V_{GS} = 0V, I_D = 100 μA	
	$V_{GS(th)}$	Gate Threshold Voltage	0.3		2.5	V	V_{DS} = V_{GS}, I_D = 1 mA	
	I_{GSS}	Gate-Body Leakage			10	nA	V_{GS} = 10V, V_{DS} = 0	Note 4
	I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{DS} = 40V, V_{GS} = 0	
	$I_{D(on)}$	ON-State Drain Current	0.25			A	V_{DS} = 25V, V_{GS} = 5V	Note 2
			0.50				V_{DS} = 25V, V_{GS} = 10V	
	$V_{DS(on)}$	Drain-Source ON Voltage			2.5	V	V_{GS} = 10V, I_D = 0.5A	
DYNAMIC	g_{fs}	Forward Transconductance	100	200		mmho	V_{DS} = 15V, I_D = 0.5A	
	C_{iss}	Input Capacitance		48		pF	V_{DS} = 25V, f = 1 MHz	Note 4
	C_{oss}	Output Capacitance		16				
	C_{rss}	Feedback Capacitance		2				
	t_{on}	Turn-ON Time		5		ns	See Switching Times Test Circuit	
	t_{off}	Turn-OFF Time		5				

Note 4: Sample test.

INTERSIL

VN30AB Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **Simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-source Voltage
- VN30AB, VN35AB 35V
- VN67AB 60V
- VN89AB 80V
- VN90AB 90V

Drain-gate Voltage
- VN30AB, VN35AB 35V
- VN67AB 60V
- VN89AB 80V
- VN90AB 90V

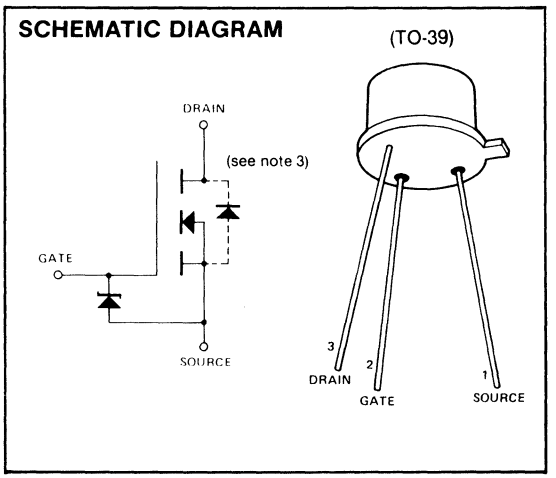
Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... –0.3V
Thermal Resistance, Junction to Case ..... 20°C/W
Continuous Device Dissipation at (or below)
25°C Case Temperature 6.25W
Linear Derating Factor ..... 50mW/°C
Operating Junction
Temperature Range ..... –55°C to +150°C
Storage Temperature Range ..... –55°C to +150°C
Lead Temperature
(1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec. duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM



5000Z

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	CHARACTERISTIC		VN30AB			VN35AB			VN67AB			VN89AB			VN90AB			UNIT	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
STATIC	BV_{DSS}	Drain Source Breakdown	35			35			60			80			90			V	I_D = 10μA, V_{GS} = 0
	$V_{GS(th)}$	Gate Threshold Voltage	0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2			I_D = 1.0mA, V_{DS} = V_{GS}
	I_{GSS}	Gate-Body Leakage		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5	μA	V_{GS} = 10V, V_{DS} = 0
	I_{DSS}	Zero Gate Voltage Drain Current			10			10			10			10			10		V_{DS} = 25V, V_{GS} = 0
	$R_{DS(on)}$	Drain-Source ON-State Resistance (Note 1)			6.0			4.5			5.1			5.1			6.0	Ω	V_{GS} = 5V, I_D = 300mA
				2.2	5.0		2.2	2.5		2.2	3.5		2.2	4.5		2.2	5.0		V_{GS} = 10V, I_D = 1.0A
	$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25V, V_{GS} = 10V
DYNAMIC	g_{fs}	Forward Transconductance		250			250			250			250			250		mmho	V_{DS} = 25V, I_D = 0.5A
	C_{iss}	Input Capacitance (Note 2)			50			50			50			50			50	pF	V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz
	C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10			10			10		
	C_{oss}	Common Source Output Capacitance (Note 2)			40			40			40			40			40		
	t_{on}	Turn-ON Time (Note 2)		4	10		4	10		4	10		4	10		4	10	ns	
	t_{off}	Turn-OFF Time (Note 2)		4	10		4	10		4	10		4	10		4	10		

Note 1. Pulse Test — 80μs, 1% duty cycle.

Note 2. Sample Test.

INTERSIL

VN35AK Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high current switching**
- **High gain-bandwidth product**
- **Inherently temperature stable**
- **Extended safe operating area**
- **Simple DC biasing**
- **Requires almost zero current drive**

APPLICATIONS

- **High current analog switches**
- **RF power amplifiers**
- **Laser diode pulsers**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-source Voltage
- VN35AK 35V
- VN66AK, VN67AK 60V
- VN98AK, VN99AK 90V

Drain-gate Voltage
- VN35AK 35V
- VN66AK, VN67AK 60V
- VN98AK, VN99AK 90V

Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2) 3.0A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... −30V
Thermal Resistance, Junction to Case ..... 20°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 6.25W

Linear Derating Factor ..... 50mW/°C
Operating Junction
- Temperature Range ..... −55°C to +150°C

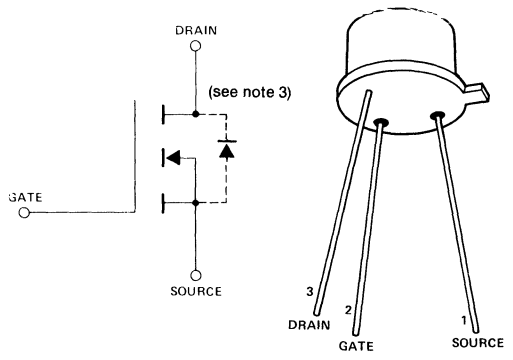
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (TO-39)



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ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	CHARACTERISTIC			VN35AK			VN66AK VN67AK			VN98AK VN99AK			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
STATIC	BV_{DSS}	Drain-Source Breakdown		35			60			90			V	V_{GS} = 0, I_D = 10μA	
	$V_{GS(th)}$	Gate-Threshold Voltage		0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA	
	I_{GSS}	Gate-Body Leakage			0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15V, V_{DS} = 0	
						500			500			500		V_{GS} = 15V, V_{DS} = 0, T_A = 125°C (Note 2)	
	I_{DSS}	Zero Gate Voltage Drain Current				10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
						500			500			500		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
					100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
	$I_{D(on)}$	ON-State Drain Current		1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25V, V_{GS} = 10V	
	$V_{DS(on)}$	Drain-Source Saturation Voltage	VN66AK					1.0			1.1		V	V_{GS} = 5V, I_D = 0.3A	(Note 1)
			VN98AK					2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0A	
			VN35AK VN67AK		1.0			1.1			1.2			V_{GS} = 5V, I_D = 0.3A	
			VN99AK		2.2	2.5		2.2	3.5		2.2	4.5		V_{GS} = 10V, I_D = 1.0A	
	g_{fs}	Forward Transconductance		170	250		170	250		170	250		mΩ	V_{DS} = 24V, I_D = 0.5A, f = 1KHz	
DYNAMIC	C_{iss}	Input Capacitance			40	50		40	50		40	50	pF	V_{GS} = 0, V_{DS} = 24V, f = 1MHz	(Note 2)
	C_{oss}	Common Source Output Capacitance			38	45		35	40		32	40			
	C_{rss}	Reverse Transfer Capacitance			7	10		6	10		5	10			
	t_{on}	Turn ON Time			3	8		3	8		3	8	ns		
	t_{off}	Turn OFF Time			3	8		3	8		3	8			

Note 1. Pulse test — 80μs pulse, 1% duty cycle. **Note 2.** Sample test.

INTERSIL

VN40AF Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **Simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**
- **Reliable, low cost plastic package**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**
- **DC motor controllers**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Drain-source Voltage
- VN40AF 40V
- VN67AF 60V
- VN89AF 80V

Drain-gate Voltage
- VN40AF 40V
- VN67AF 60V
- VN89AF 80V

Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse Voltage ..... −0.3V
Thermal Resistance, Junction to Case ..... 10.4°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 12W

Linear Derating Factor ..... 96mW/°C
Operating Junction
- Temperature Range ..... −40 °C to +150°C

Storage Temperature Range ..... −40 °C to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

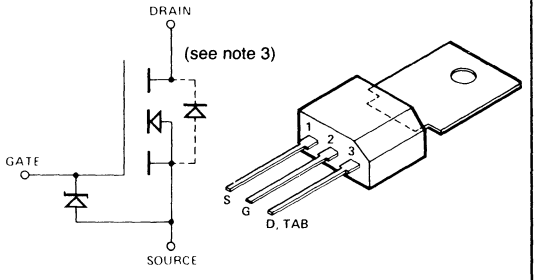
Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM

TO-202



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INTERSIL

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	CHARACTERISTIC		VN40AF			VN67AF			VN89AF			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	V_{GS} = 0, I_D = 10μA	
			40			60			80				V_{GS} = 0, I_D = 2.5mA	
	$V_{GS(th)}$	Gate-Threshold Voltage	0.6	1.2		0.8	1.2		0.8	1.2			V_{DS} = V_{GS}, I_D = 1mA	
	I_{GSS}	Gate-Body Leakage		0.01	10		0.01	10		0.01	10	μA	V_{GS} = 10V, V_{DS} = 0	
					100			100			100		V_{GS} = 10V, V_{DS} = 0, T_A = 125°C (Note 2)	
	I_{DSS}	Zero Gate Voltage Drain Current			10			10			10		V_{DS} = Max. Rating, V_{GS} = 0	
					100			100			100		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
				100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
	$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	(Note 1)
	$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.3			0.4		V	V_{GS} = 5V, I_D = 0.1A	
				1.0	2.0		1.0	1.7		1.4	1.9		V_{GS} = 5V, I_D = 0.3A	
				1.0			1.0			1.3			V_{GS} = 10V, I_D = 0.5A	
				2.2	5.0		2.2	3.5		2.2	4.5		V_{GS} = 10V, I_D = 1.0A	
DYNAMIC	g_m	Forward Transconductance		250			250			250		mmho	V_{DS} = 24V, I_D = 0.5A, f = 1KHz	
	C_{iss}	Input Capacitance			50			50			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz	(Note 2)
	C_{rss}	Reverse Transfer Capacitance			10			10			10			
	C_{oss}	Common-Source Output Capacitance			50			50			50			
	$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5		2	5	ns		
	t_r	Rise Time		2	5		2	5		2	5			
	$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5		2	5			
	t_f	Fall Time		2	5		2	5		2	5			

Note 1. Pulse test — 80μs pulse, 1% duty cycle.
Note 2. Sample test.

INTERSIL

VN46AF Series
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- Simple DC biasing
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers

ABSOLUTE MAXIMUM RATINGS

(T_A = 25° C unless otherwise noted)

Drain-source Voltage
- VN46AF 40V
- VN66AF 60V
- VN88AF 80V

Drain-gate Voltage
- VN46AF 40V
- VN66AF 60V
- VN88AF 80V

Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... −0.3V
Thermal Resistance, Junction to Case .... 10.4°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 12W

Linear Derating Factor ..... 96mW/°C
Operating Junction
- Temperature Range ..... −40°C to +150°C

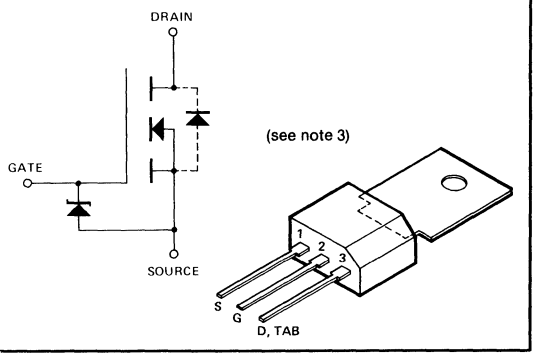
Storage Temperature Range ..... −40°C to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (TO-202)



5000Z

INTERSIL

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	CHARACTERISTIC		VN46AF			VN66AF			VN88AF			UNIT	TEST CONDITIONS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	V_{GS} = 0, I_D = 10μA	
			40			60			80				V_{GS} = 0, I_D = 2.5mA	
	$V_{GS(th)}$	Gate-Threshold Voltage	0.8	1.7		0.8	1.7		0.8	1.7			V_{DS} = V_{GS}, I_D = 1mA	
	I_{GSS}	Gate-Body Leakage		0.01	10		0.01	10		0.01	10	μA	V_{GS} = 10V, V_{DS} = 0	
					100			100			100		V_{GS} = 10V, V_{DS} = 0, T_A = 125°C (Note 2)	
	I_{DSS}	Zero Gate Voltage Drain Current			10			10			10		V_{DS} = Max. Rating, V_{GS} = 0	
					100			100			100		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
				100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
	$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	
	$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.3			0.4		V	V_{GS} = 5V, I_D = 0.1A	(Note 1)
				1.0	1.5		1.0	1.5		1.4	1.7		V_{GS} = 5V, I_D = 0.3A	
				1.0			1.0			1.3			V_{GS} = 10V, I_D = 0.5A	
				2.2	3.0		2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0A	
DYNAMIC	g_{fs}	Forward Transconductance	150	250		150	250		150	250		mmho	V_{DS} = 24V, I_D = 0.5A, f = 1KHz	
	C_{iss}	Input Capacitance			50			50			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0MHz	(Note 2)
	C_{rss}	Reverse Transfer Capacitance			10			10			10			
	C_{oss}	Common-Source Output Capacitance			50			50			50			
	$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5		2	5	ns		
	t_r	Rise Time		2	5		2	5		2	5			
	$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5		2	5			
	t_f	Fall Time		2	5		2	5		2	5			

Note 1. Pulse test — 80μs pulse, 1% duty cycle. **Note 2.** Sample test.

INTERSIL

VQ1000 CJ
Quad n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- Directly drives inductive loads
- High speed, high peak current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Inherent protection from thermal runaway

APPLICATIONS

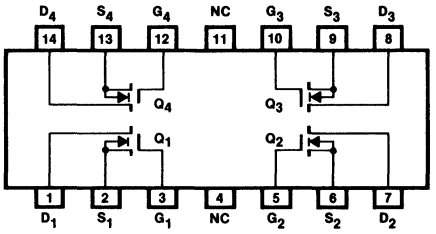
- LED and lamp drivers
- TTL and CMOS to high current interface
- High speed switches
- Line drivers
- Relay drivers
- Transformer drivers

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Drain-Source Voltage 60V
Drain-Gate Voltage 60V
Continuous Drain Current (per device) 0.3A
Peak Drain Current (per device) 1.0A
Gate-Source Forward Voltage ..... +15V
Gate-Source Reverse Voltage 0.3V
Reverse Diode Continuous Current 0.3A
Reverse Diode Peak Current 1.0A
Temperature
(Operating and Storage) ..... −40 °C to +150 °C
Lead Temperature (Soldering, 10 sec) ..... +300 °C

PIN CONFIGURATION

14 Pin Plastic Dip



TOP VIEW

6300

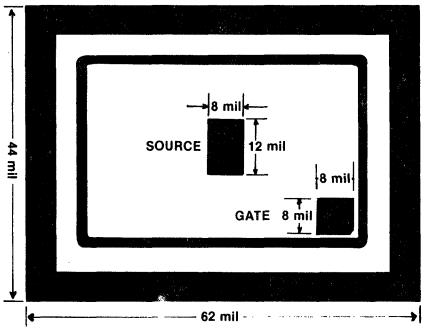
ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITIONS	
BV_{DSS}	Drain-Source Breakdown	60			V	V_{GS} = 0V, I_D = 100μA	
$V_{GS(th)}$	Gate Threshold Voltage	0.8			V	V_{GS} = V_{GS} = V_{DS}, I_D = 1 mA	
I_{GSS}	Gate-Body Leakage			100	nA	V_{GS} = 10 , V_{DS} = 0	
I_{DSS}	Zero Gate Voltage Drain Current			100	μA	V_{DS} = 40V, V_{GS} = 0	
$I_{D(on)}$	ON-State Drain Current	0.20			A	V_{DS} = 25V, V_{GS} = 5V	
		0.5			A	V_{DS} = 25V, V_{GS} = 10V	
$V_{DS(on)}$	Drain-Source ON Voltage			1.5	V	V_{GS} = 5V, I_D = 0.20A	(Note 1)
				1.65	V	V_{GS} = 10V, I_D = 0.3A	
g_{fs}	Forward Transconductance	100			mmho	V_{DS} = 15V, I_D = 0.5A	
C_{iss}	Input Capacitance		48		pF	V_{DS} = 25 , I = 1 MHz	(Note 1)
C_{oss}	Output Capacitance		16		pF		
C_{rss}	Feedback Capacitance		2		pF		
t_{on}	Turn-ON Time			10	ns	I = 0.3A, R_L = 23Ω	
t_{off}	Turn-OFF Time			10	ns	R_S = 50Ω	
t_{rr}	Reverse Diode		230		ns	I_F = I_R = 1A I_{rr} = 0.1A	(Note 2)
	Reverse Recovery Time		165		ns	I_F = I_R = 0.3A I_{rr} = 0.03A	

NOTES: 1. Pulse test - 80μs pulse, 1% duty cycle.
2. Sample test.

INTERSIL

Power MOS Geometries



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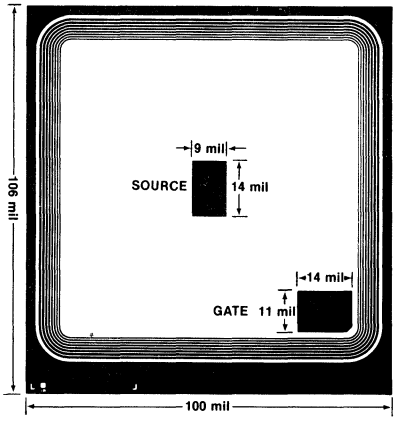

5200
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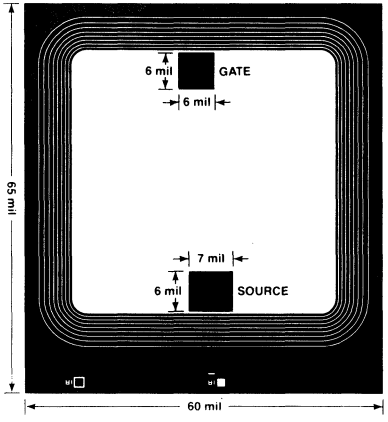

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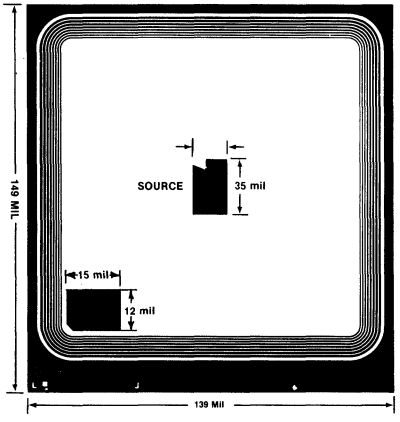

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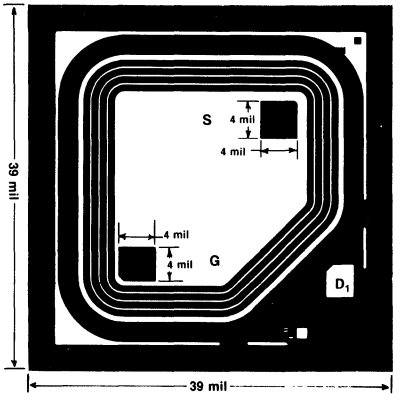


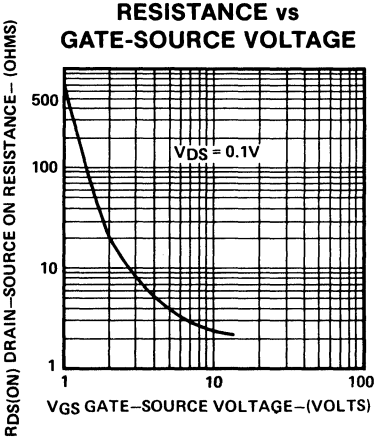
6300

5000 Family Typical Performance Curves

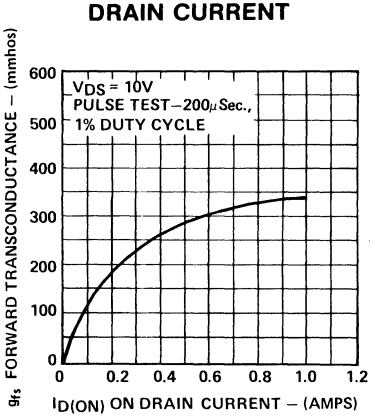
INTERSIL

(25°C unless otherwise stated)

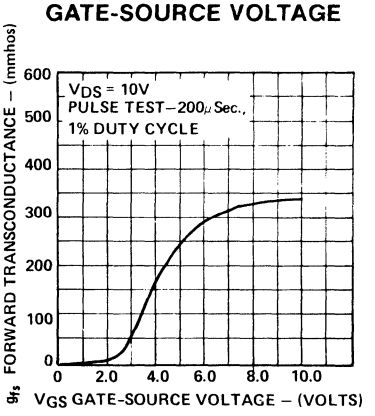
DRAIN-SOURCE ON RESISTANCE vs GATE-SOURCE VOLTAGE



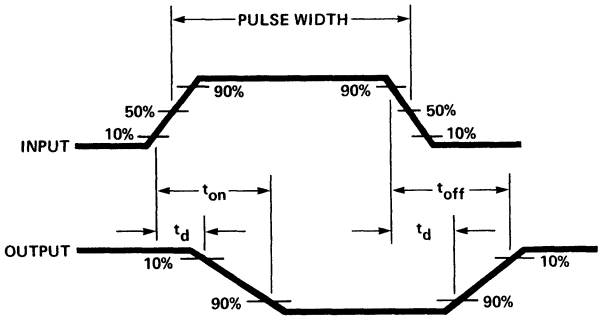
TRANSCONDUCTANCE vs DRAIN CURRENT



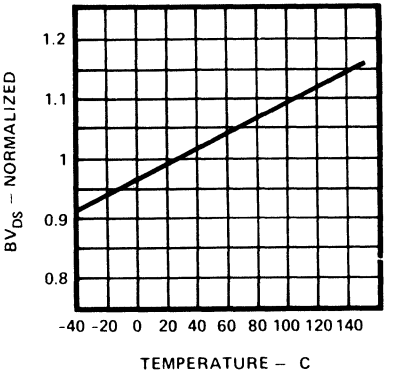
TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE



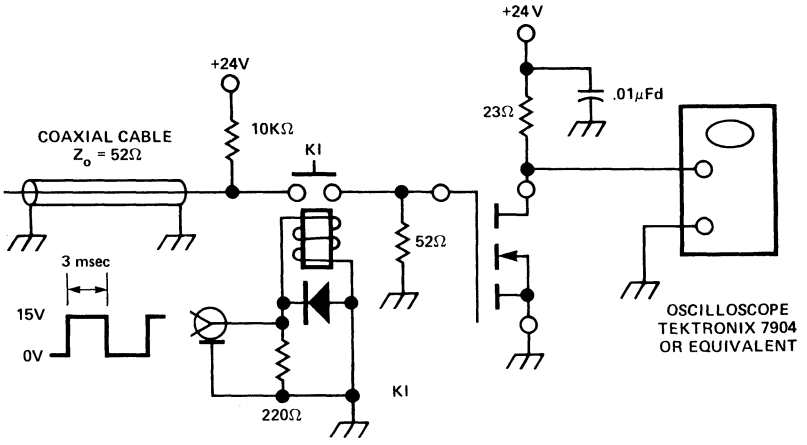
SWITCHING TIME TEST WAVEFORMS



BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE



SWITCHING TIME TEST CIRCUIT

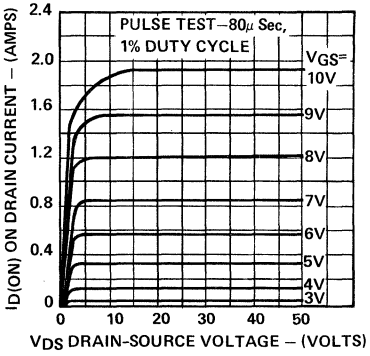


5000 Family Typical Performance Curves

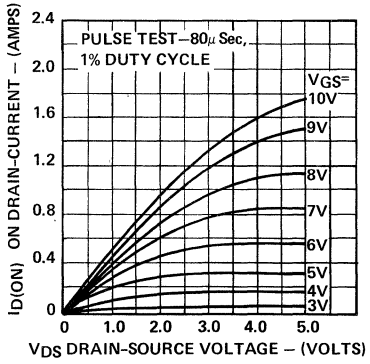
(25°C unless otherwise stated)

INTERSIL

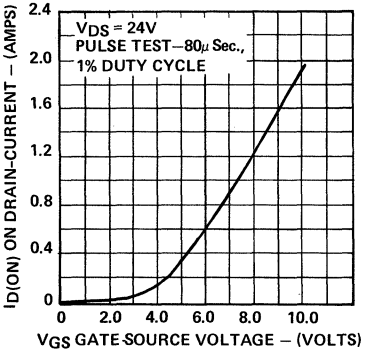
OUTPUT CHARACTERISTICS



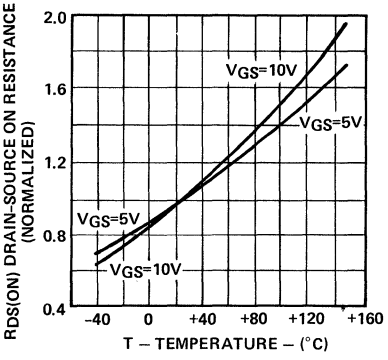
SATURATION CHARACTERISTICS



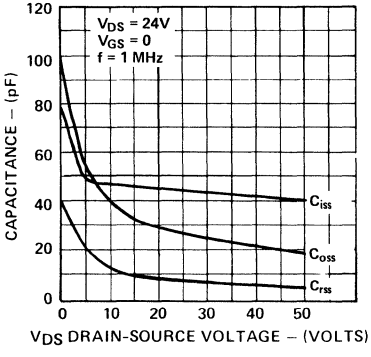
TRANSFER CHARACTERISTIC



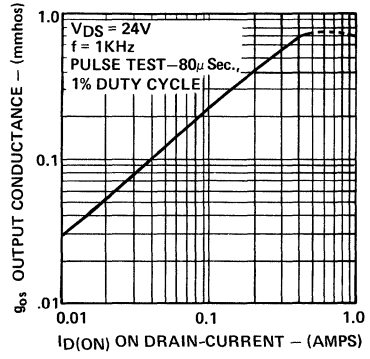
NORMALIZED DRAIN-SOURCE ON RESISTANCE vs TEMPERATURE



CAPACITANCE vs DRAIN-SOURCE VOLTAGE



OUTPUT CONDUCTANCE vs DRAIN CURRENT

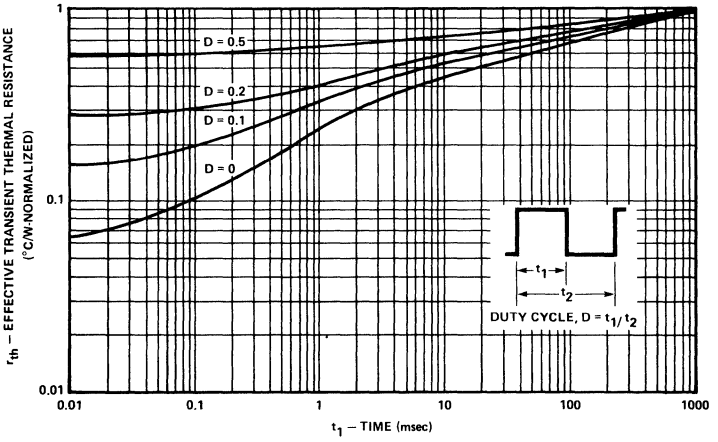


5000 Family Typical Performance Curves

(25°C unless otherwise stated)

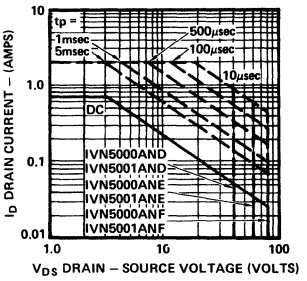
INTERSIL

THERMAL RESPONSE

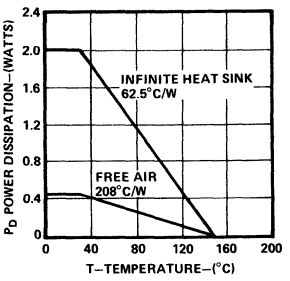


DC SAFE OPERATING REGION

Tc = 25°C



POWER DISSIPATION DERATING

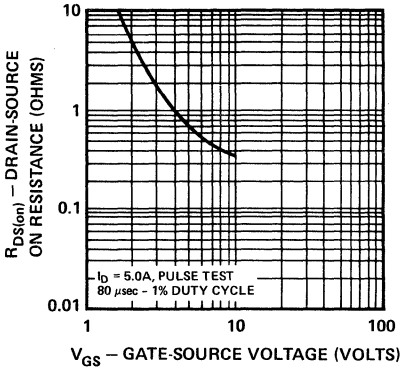


5200 Family Typical Performance Curves

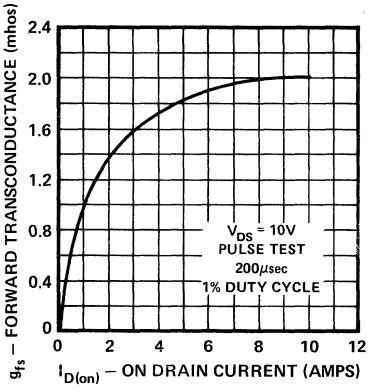
INTERSIL

(25°C unless otherwise stated)

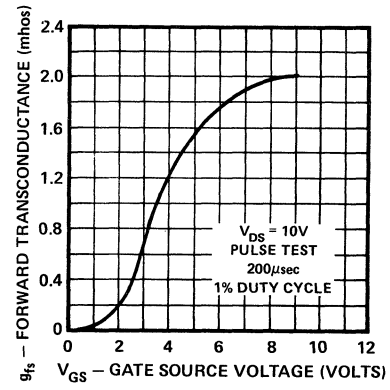
DRAIN-SOURCE ON RESISTANCE vs GATE-SOURCE VOLTAGE



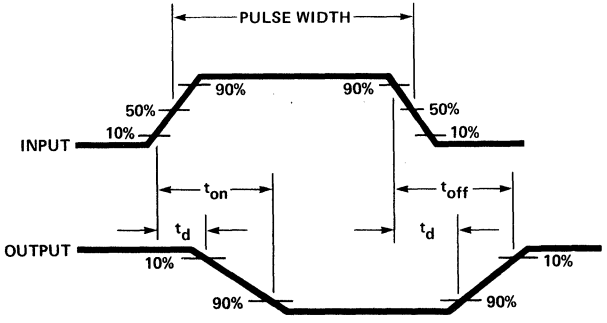
TRANSCONDUCTANCE vs DRAIN CURRENT



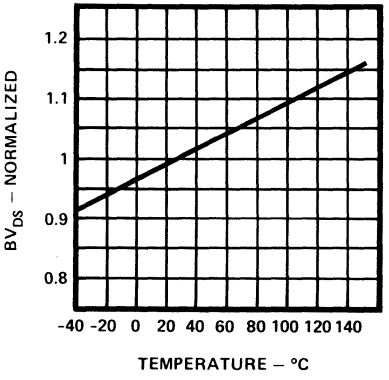
TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE



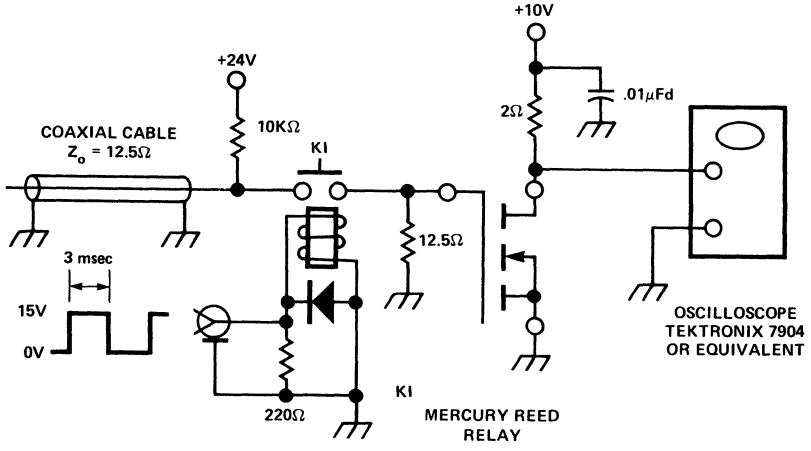
SWITCHING TIME TEST WAVEFORMS



BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE



SWITCHING TIME TEST CIRCUIT

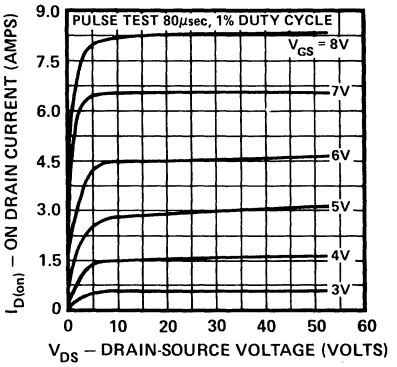


5200 Family Typical Performance Curves

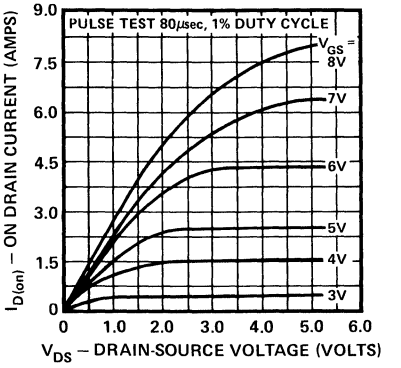
INTERSIL

(25°C unless otherwise stated)

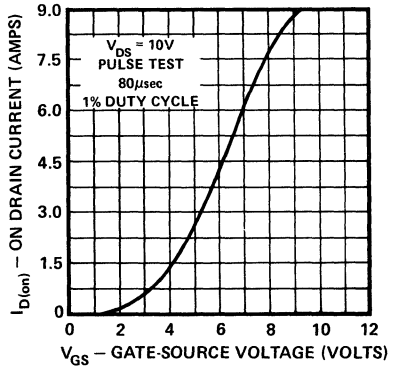
OUTPUT CHARACTERISTICS



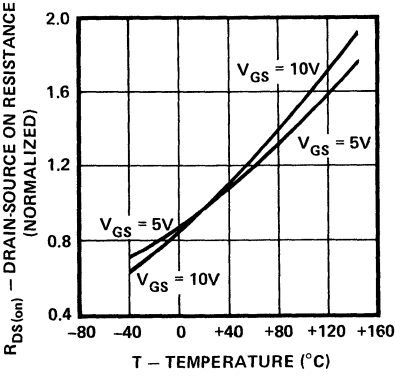
SATURATION CHARACTERISTICS



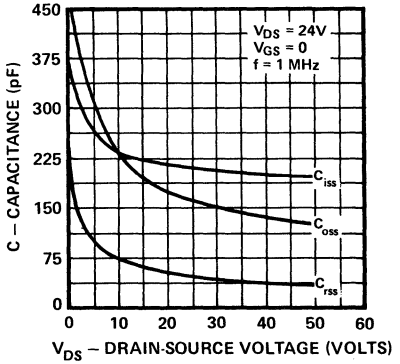
TRANSFER CHARACTERISTIC



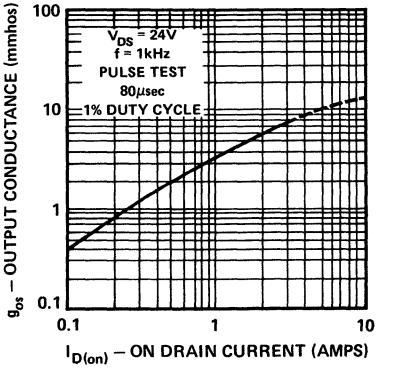
NORMALIZED DRAIN-SOURCE ON RESISTANCE vs TEMPERATURE



CAPACITANCE vs DRAIN-SOURCE VOLTAGE



OUTPUT CONDUCTANCE vs DRAIN CURRENT

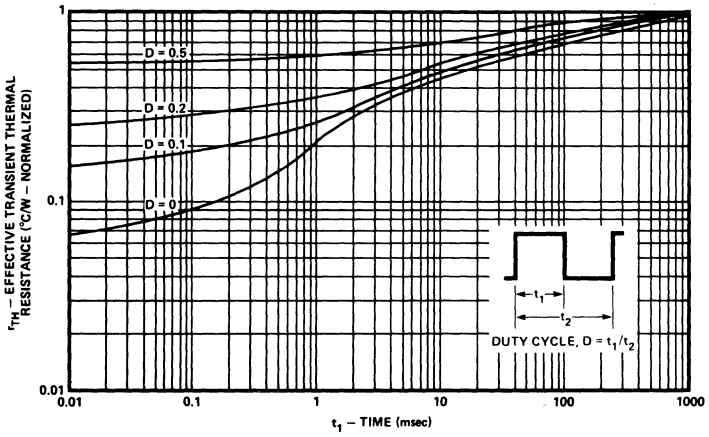


5200 Family Typical Performance Curves

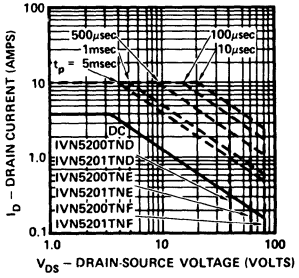
(25°C unless otherwise stated)

INTERSIL

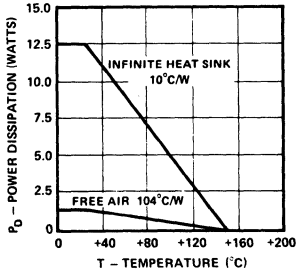
THERMAL RESPONSE



DC SAFE OPERATING REGION
Tc = 25°C



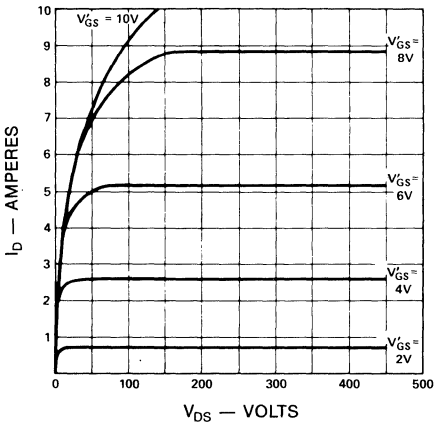
POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



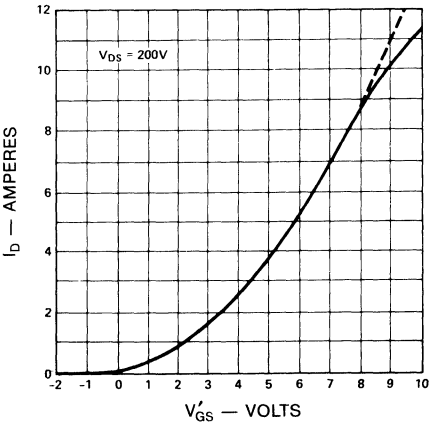
6000 Family Typical Performance Curves

(25°C unless otherwise stated)

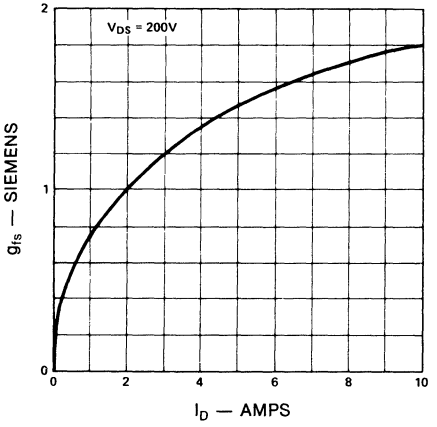
OUTPUT CHARACTERISTICS



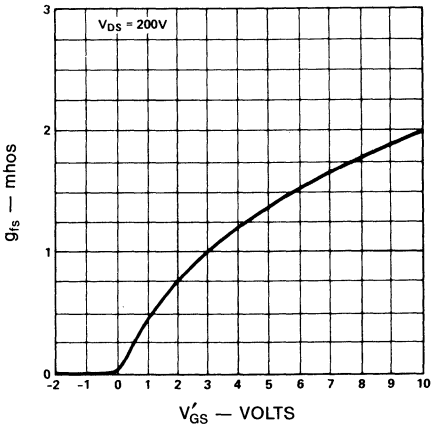
TRANSFER CHARACTERISTICS



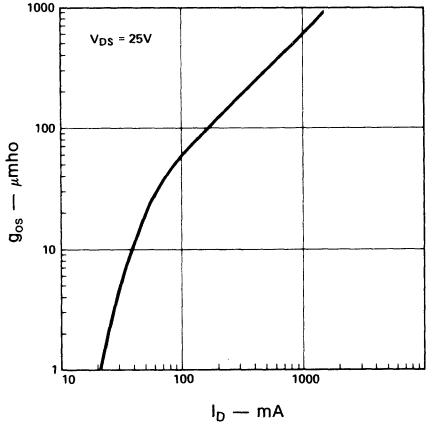
TRANSCONDUCTANCE CHARACTERISTIC



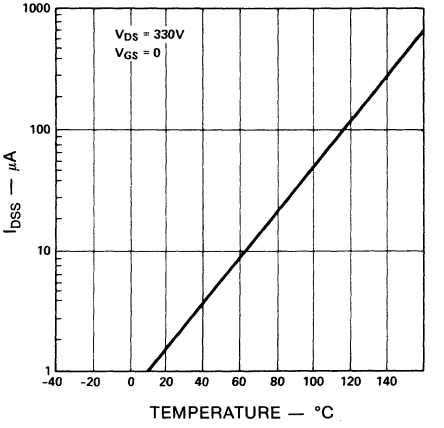
TRANSCONDUCTANCE CHARACTERISTIC



OUTPUT CONDUCTANCE



DRAIN-SOURCE LEAKAGE CURRENT

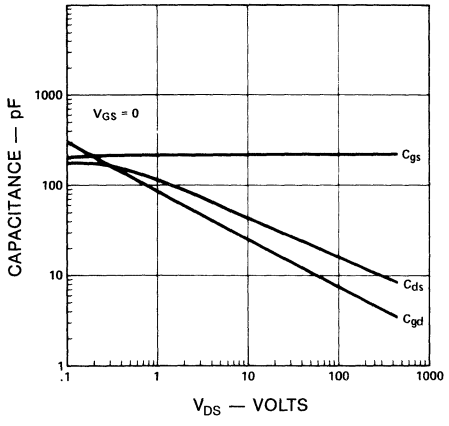


NOTE: $V'_{GS} = V_{GS} - V_{GS(th)}$

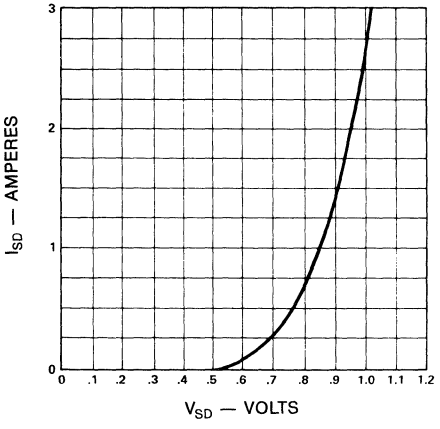
6000 Family Typical Performance Curves

(25°C unless otherwise stated)

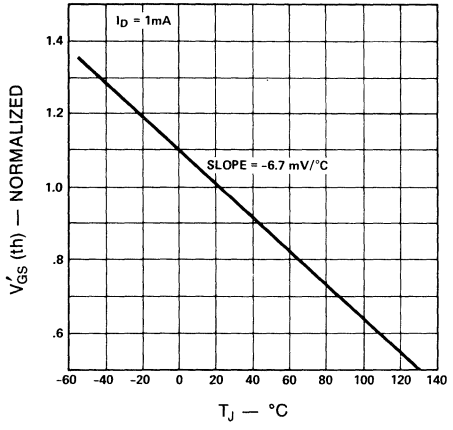
CAPACITANCE vs. DRAIN-SOURCE VOLTAGE



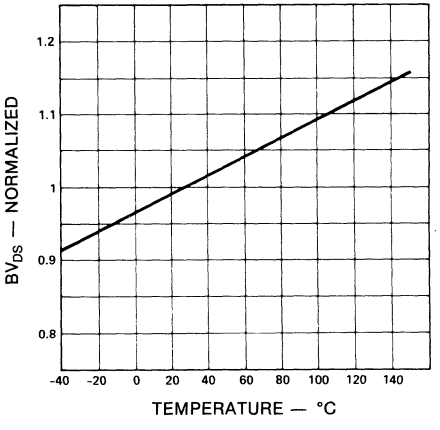
BODY-DRAIN DIODE FORWARD VOLTAGE CHARACTERISTIC



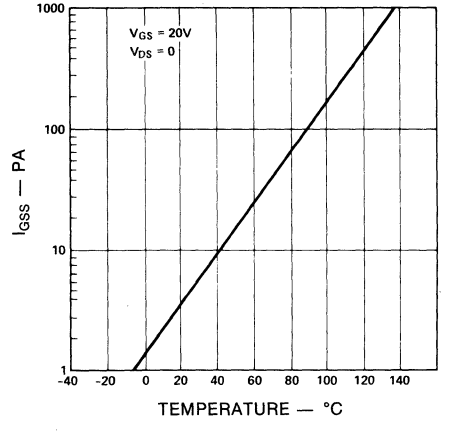
THRESHOLD VOLTAGE VS. TEMPERATURE



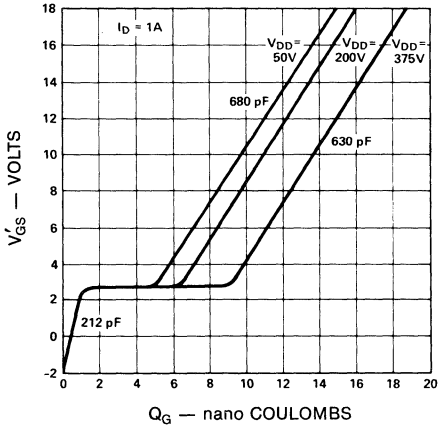
DRAIN-SOURCE BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE



GATE LEAKAGE CURRENT



GATE DYNAMIC CHARACTERISTICS

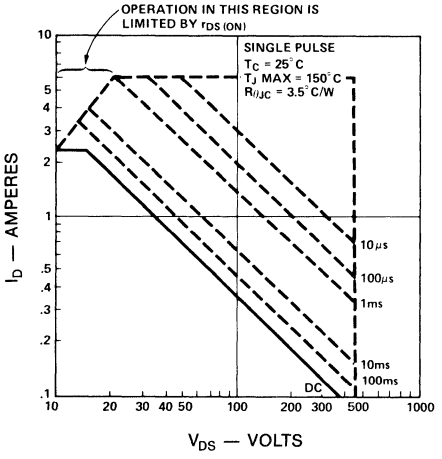


NOTE: $V'_{GS} = V_{GS} - V_{GS(th)}$

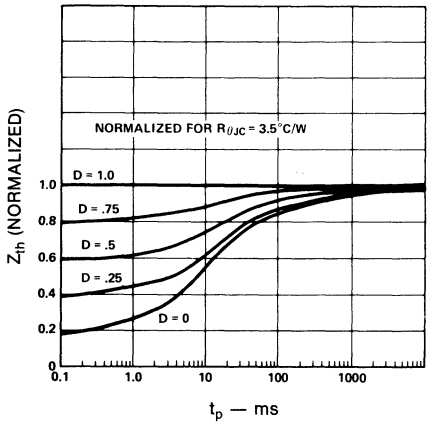
6000 Family Typical Performance Curves

(25°C unless otherwise stated)

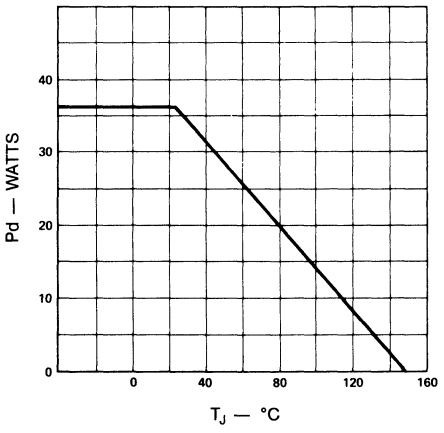
SAFE OPERATING AREA



TRANSIENT THERMAL IMPEDANCE

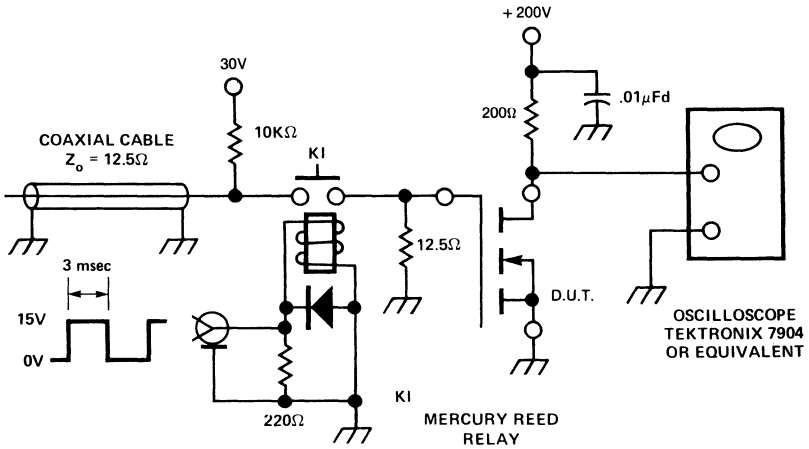


POWER DISSIPATION vs. TEMPERATURE DERATING



NOTE: $V'_{GS} = V_{GS} - V_{GS(th)}$

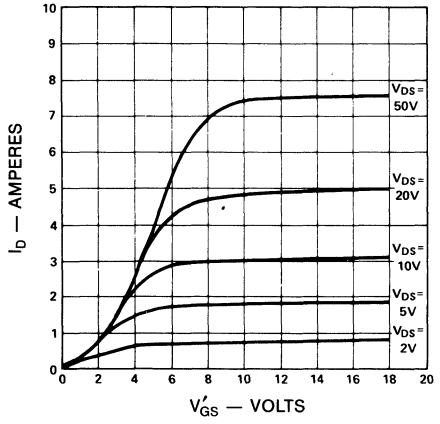
SWITCHING TIME TEST CIRCUIT



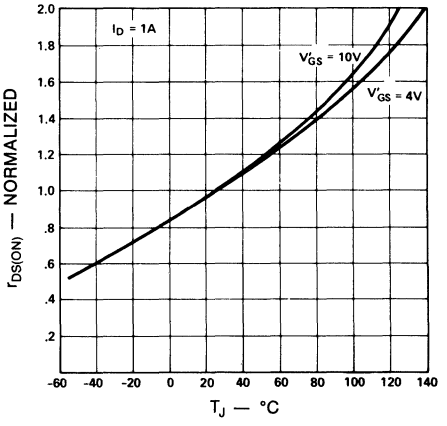
6000 Family Typical Performance Curves INTERSIL

(25°C unless otherwise stated)

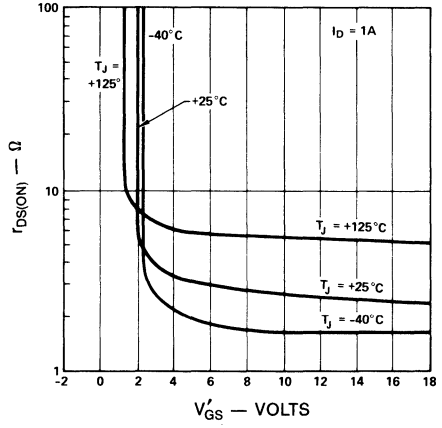
LARGE SIGNAL TRANSFER CHARACTERISTICS



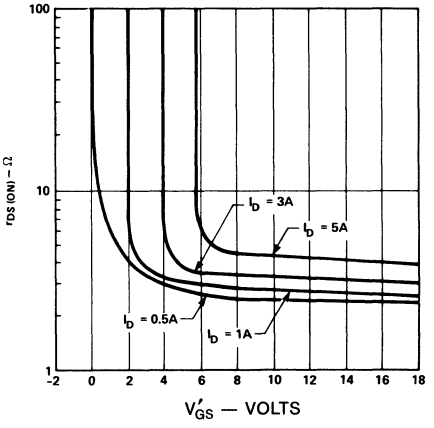
ON RESISTANCE vs. JUNCTION TEMPERATURE



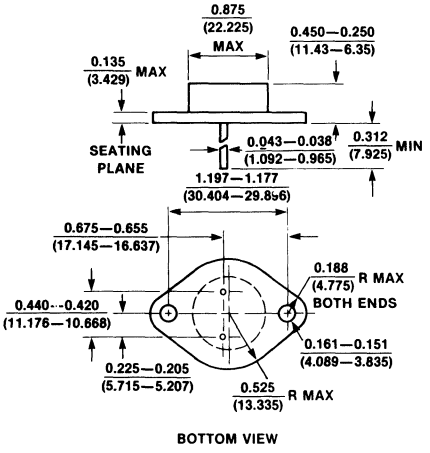
ON RESISTANCE vs. V'_{GS}* AS A FUNCTION OF TEMPERATURE



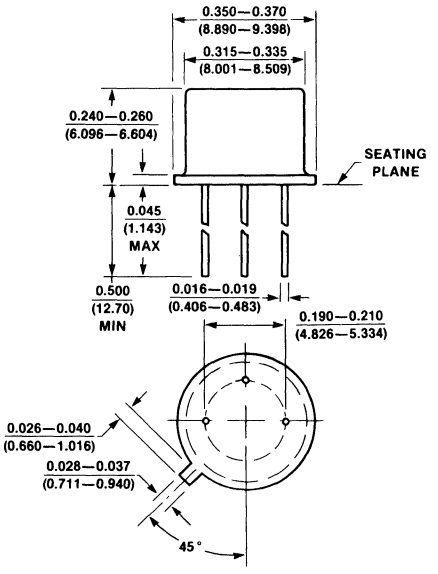
ON RESISTANCE vs. V'_{GS}* AS A FUNCTION OF I_D



NOTE: $V'_{GS} = V_{GS} - V_{GS(th)}$



TO-3



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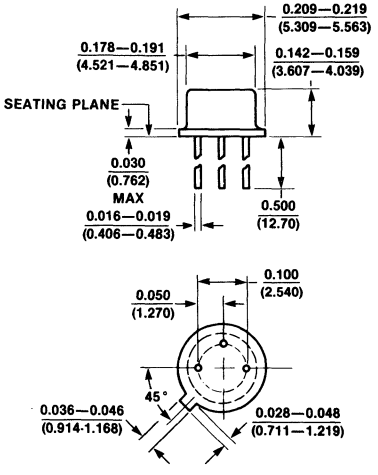

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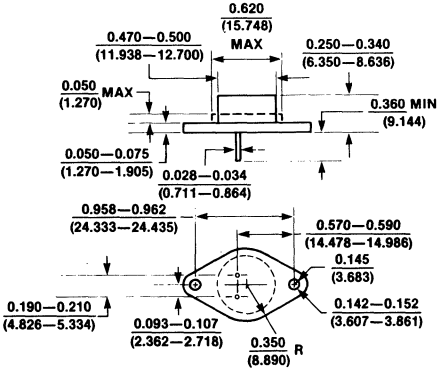

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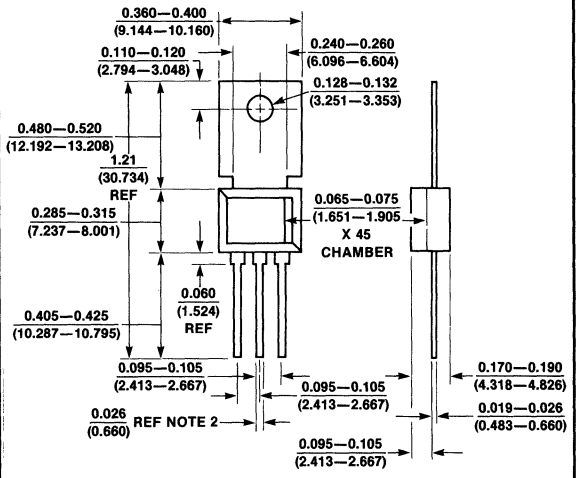
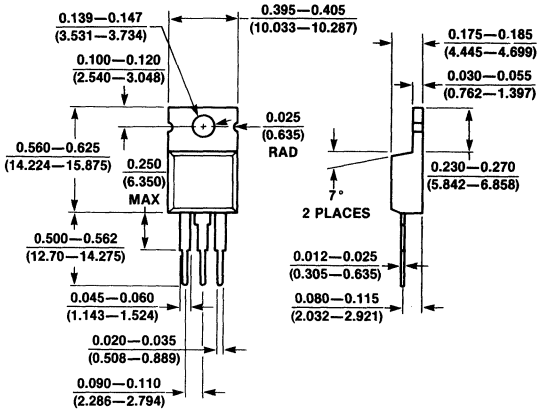


TO-202



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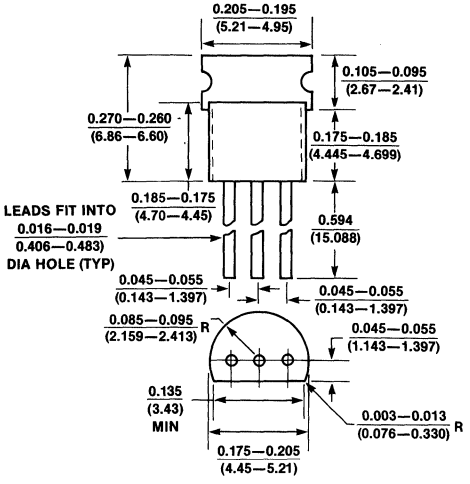

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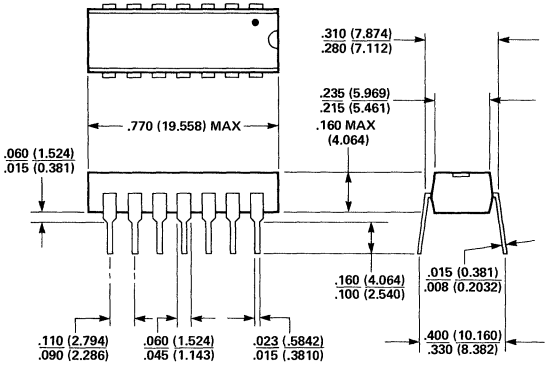

PD (14-PIN PLASTIC)

INTERSIL

AO33
The Power MOSFET, A Breakthrough in Power Device Technology

by Rudy Severns

Recent advances in the technology of fabricating MOSFET's have enabled manufacturers to break free of the power limitations of the early devices. While the power MOSFET is a relative newcomer to the power switch field, it promises exciting performance advantages over the more conventional bipolar transistor. By providing much higher switching speeds (a few nanoseconds is typical), high input impedance with low drive requirements, simplified multi-device operation, and greatly improved safe operating area for power switching applications, the power MOSFET will replace the bipolar transistor in many applications, and provide new circuit opportunities that do not exist with bipolar technologies. Several different types of power MOSFET's are already available, and the immediate future promises many more devices with steadily increasing performance.

This applications note is intended to provide the design engineer with a basic understanding of how power MOSFET's work, the structures presently in use, the electrical characteristics of the devices and some guidance on application.

STRUCTURES

At the present time, there are a host of different and often confusing names for power FET devices, such as VMOS, VFET, HEXFET®, TMOS, DMOS, ZMOS, etc. In actuality there are only three basic structures: vertical junction FET's, V-groove MOSFET's and vertical DMOS FET's.

Planar MOSFET

Figure 1 is a cross section of a conventional planar N-channel enhancement mode MOSFET. Fabrication of this device begins with a P substrate into which N^+ regions are diffused. SiO_2 is then grown and etched for the aluminum which is deposited to form the source, gate and drain connections. If no bias is applied to the gate, this device is essentially two back-to-back PN diodes and no conduction occurs. If, however, the gate is made positive with respect to the source, the electrostatic field draws electrons near the surface of the P region. This inverts that region to N material, and a channel is formed, allowing conduction between source and drain. Note that the MOSFET is a majority carrier device which acts like a voltage controlled resistor during conduction. The result is an extremely fast switch with no storage time effects. There are, however, a number of drawbacks for high power use which, for practical purposes, eliminate this structure from consideration for high power use:

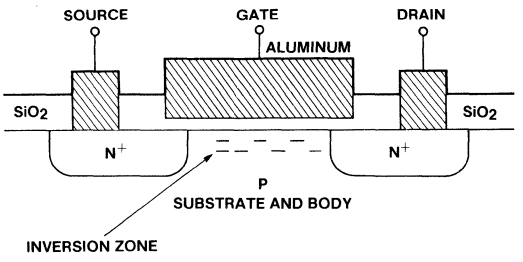

Figure 1. The Cross Section of a Conventional MOSFET

1. The length of the channel is controlled by the mask spacing of the N^+ regions. Due to the limits of accuracy of photomask technology, it is necessary to have relatively wide spacing. This produces long channel lengths which increase the ON resistance for a given area of silicon.
2. The source, gate and drain conductors are all on the same surface. This metallization takes up a major portion of the die area, further increasing the ON resistance.
3. This structure has large inherent capacitances, for its current capability, especially gate to drain. This reduces the gain bandwidth and increases the drive power in repetitive pulse applications.

VMOS

Most of the deficiencies in the planar MOSFET's can be overcome by going to a structure that allows the current to flow vertically, and in which the channel length is controlled by diffusion processes rather than mask spacing. The VMOS structure shown in Figure 2a is a particularly good solution. A VMOS device fabrication process starts with an N^+ substrate with an N^- epi layer. A P region is diffused in and then an N^+ layer is diffused within the P region. Up to this point the process is very similar to that for a double diffused NPN transistor (Figure 2b), but, rather than applying the base and emitter metal, a V groove is anisotropically etched in the surface of the device, a silicon oxide insulating layer is grown, and finally, source and gate metal is deposited. Note that the source metal overlaps the P and N^+ regions so that the base and emitter of the NPN transistor are connected together.

By applying a positive potential between the gate and source, the P region close to the gate can be electrostatically inverted to N type material, and a conducting channel formed. Thus the source and gate connections are on the upper surface while the drain is on the bottom, and current flow is essentially vertical. In addition, the channel lengths are controlled by the diffusion processes and can be made quite short. This structure allows very efficient utilization of the silicon, and high power MOSFET's can be fabricated.

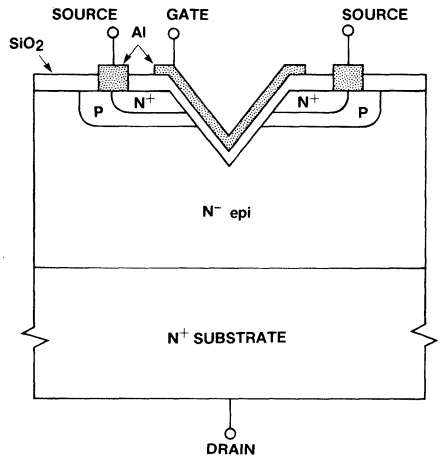

Figure 2A. Conventional Metal Gate VMOS Structure With Sharp "V" Groove

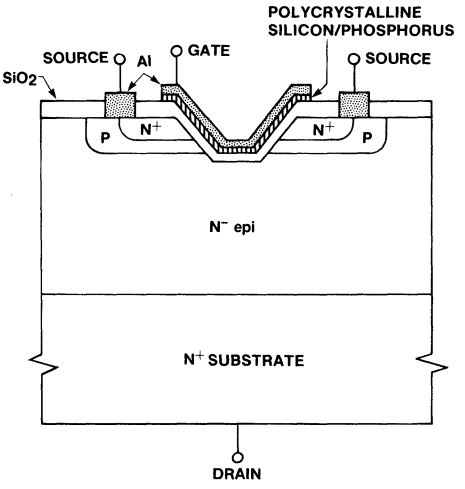

Figure 3. Flat-Bottomed Groove Silicon Gate VMOS

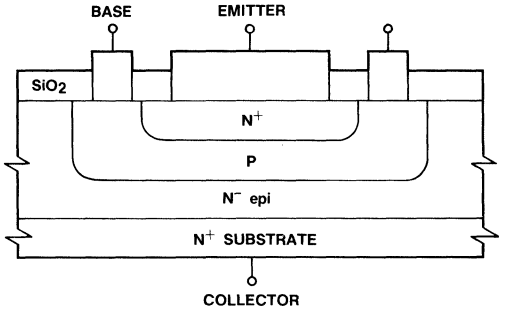

Figure 2B. Typical Double Diffused NPN Transistor

However, this basic structure has some drawbacks. The sharp bottom of the V groove produces a strong field concentration between the gate and drain, and there is also a tendency for the gate oxide layer to thin down around the tip of the V. The result is limited high voltage capability due to gate oxide breakdown even though the gate does not see the full drain-source voltage. The use of an aluminum gate can cause long term reliability problems due to ion migration (principally sodium) through the gate oxide which leads to variations in the device threshold voltage. A channel is formed on each side of the V groove, and if the groove does not penetrate well past the P region into the epi layer, it is possible to experience excessive current densities which may cause current injected avalanche breakdown in high power devices.

UMOS

Most of the VMOS problems can be relieved by using a flat bottomed groove with a combined silicon and aluminum gate structure as shown in Figure 3. The process is very similar to VMOS except that the etching is halted while the bottom of the groove is relatively wide. A layer of oxide is grown and overlaid with a layer of polycrystalline silicon doped with phosphorus. Phosphorus doped poly-silicon is an effective ion migration barrier but it is not a particularly good conductor, having a resistance about 3000 times that of aluminum. In a large device, this could lead to a slow turn-on time due to the gate resistance. To alleviate this problem, a layer of aluminum is applied over the silicon-gate to provide high conductivity. Another benefit of the silicon-gate process is increased manufacturing yield which lowers the device cost. This is the standard Intersil process for VMOS devices.

Vertical DMOS

While the modified VMOS process is very effective for voltages under 150V, high field problems still exist, and the groove spacing requirements increase the die area. A vertical DMOS (double-diffused MOS) process has been developed to alleviate these problems. This structure is shown in Figure 4. The process begins as before (for an N-channel device) with an N^- epi layer grown on an N^+ substrate. Regions of P^- are then diffused, and inside these, regions of

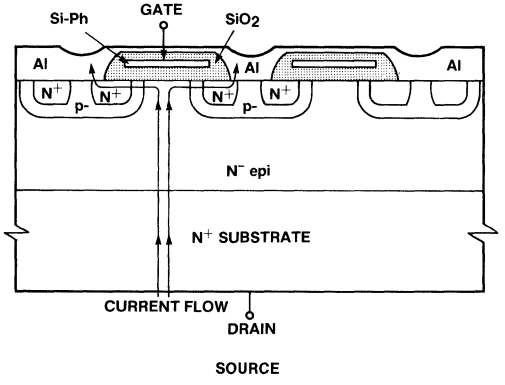

Figure 4. Vertical DMOS Structure

N^+. A silicon-gate is imbedded in SiO_2 and the source and gate metallization are then added to complete the device. The current flow is at first vertical and then horizontal, with the drain on the N^+ substrate.

This basic process has a number of different names, DMOS, TMOS, ZMOS, HEXFET®, etc. The processes are basically the same; the primary differences being in the geometry of the P and N regions and the interconnections. The HEXFET®, for example, uses hexagonal P regions, which allow a very low ON resistance by maximizing the channel perimeter. Unfortunately, as presently implemented, the silicon-gate structure has a very high series resistance which increases the switching time quite significantly. Intersil uses an alternate geometry that retains the low ON resistance but reduces the gate resistance.

Other Geometries

A variety of other geometries are in use to produce power MOSFET's and junction FET's.

Figure 5 shows a MOSFET structure developed by Hitachi.[1] The gate structure overlays the checkerboard of N and P regions to form the channels, and the N regions connect to the N^+ substrate so that the drain is on the back side of the die. To date, devices using this structure display a rather restricted Gain Bandwidth product of 0.6 to 1.5 MHz and a relatively high $r_{DS(on)}$ for a given die area. The primary application for these devices is audio amplifiers.

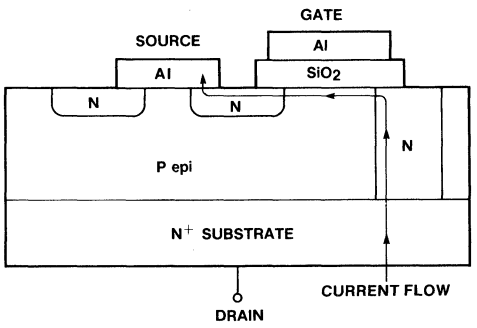

Figure 5A.

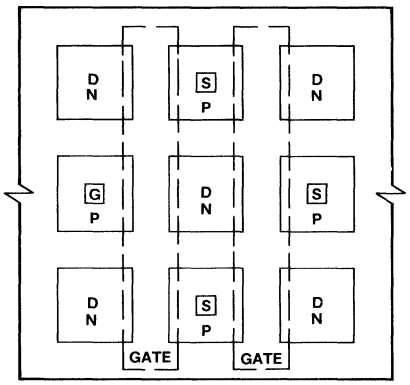

Figure 5B.

The SONY Corporation manufactures a device called a VFET,[2] which bears no relationship to the VMOS device, and is in fact, a vertical depletion mode junction FET. The structure, shown in Figure 6, produces a device with a square law transfer characteristic, while the output characteristic (Figure 7) is very much like a low μ triode. The disadvantages are relatively low stage gain, substantial gate current if the gate is driven positive, and the relatively high gate resistance and input capacitance which tend to reduce the gain bandwidth product.

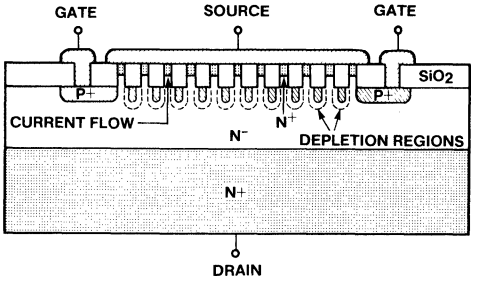

Figure 6. VFET Structure

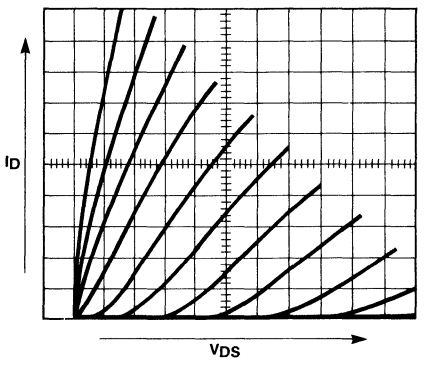

Figure 7. VFET Output Charactistics

BASIC LIMITATIONS

$r_{DS(on)}$ Versus Breakdown Voltage

As the breakdown voltage of a MOSFET (or a bipolar) is increased, the ON resistance, for a given die area and process, will increase exponentially by a factor of 2.3 to 2.7. [i.e., $r_{DS(on)} \propto k\ (BV_{DS})^{2.3-2.7}$] For example, if the breakdown voltage of a 1Ω, 100V device is increased to 200V, the die area must increase by five times to maintain the same ON resistance. The reason for this is twofold: first, the resistivity of the epi layer must be increased to raise the avalanche breakdown voltage. Second, the thickness of the epi layer must be increased to assure that the depletion region remains totally within the epi layer. Typically, in a 400V device, the epi resistivity will be 1500 to 2000 times greater than the N^+ substrate, so that at high voltages the ON resistance is dominated by the epi layer. The net result is that in either a MOSFET or a bipolar device, when the breakdown

voltage (for a given die area) is increased, the power handling capability is reduced. Conversely, if the same power capability is needed, then a larger die area is required.

Die Area Versus Yield/Cost

The ON resistance of a power FET is proportional to the die area. If a large die area is used to reduce the ON resistance, the number of dice per wafer will decrease; additional dice are lost due to inherent wafer defects and the increased scrap zone around the wafer center and periphery. The yield (Y) can be represented by a variety of equations, all of them exponentially decreasing in some manner. A typical equation is:

$$Y = k\,(n)\frac{(1-e^{AD})^2}{AD}$$

where A is the die area, D is the defect density, n is the number of process steps and k is a factor that varies inversely with n, usually exponentially. The result is a rapid decrease in yield as the die area is increased. For small devices (<.050" x .050") the yield is usually very high and the die cost low, but as the die dimensions begin to exceed .100" x .100" the yield drops and the cost per die increases rapidly. Many power FET's are larger than those dimensions, so for example, a one ohm 450 volt device may cost four to six times as much as a 2.5 ohm device with the same breakdown rating.

P-Channel Devices

The discussion so far, has dealt with N-channel devices, however P-channel devices can just as easily be built simply by interchanging the N and P regions. In fact, some manufacturers use the same mask set to produce both N and P-channel devices by changing the starting material and the process. There is, however, a very basic difference between N and P-channel devices. In the N-channel device, the majority carriers are electrons but in the P-channel, the majority carriers are holes. Holes have a mobility about half that of electrons, so when the same mask set is used to produce both N and P-channel devices, the P-channel ON resistance will be approximately twice that of the N-channel. If, for complementary symmetry, equal $r_{DS(on)}$ is needed in both devices, the P-channel will have to have about twice the area. The larger structure will also have more capacitance, so the devices will not be symmetrical in this respect, and in large devices the cost of the P-channel device will be higher.

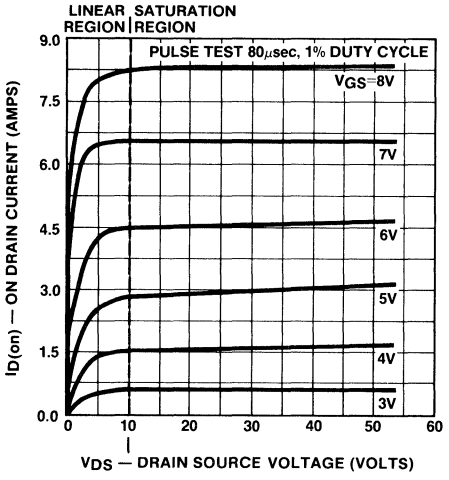

Figure 8. Output Characteristics IVN5200

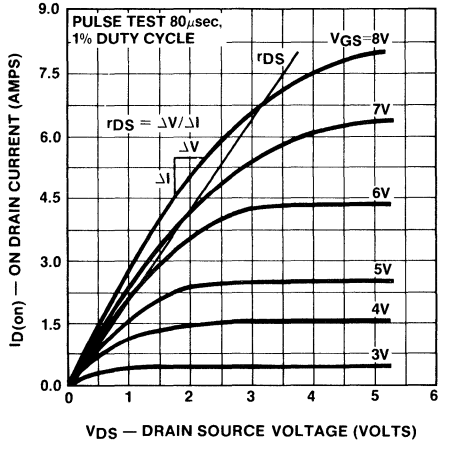

Figure 9. Output Characteristics IVN5200

LINEAR CHARACTERISTICS

Output Characteristics

The output characteristics for an IVN5200 are shown in Figures 8 and 9, where the drain current (I_D) is shown as a function of drain-source voltage (V_{DS}) with the gate-source voltage (V_{GS}) as a parameter. Two distinct regions of operation are apparent, the linear region and the saturated region. Be careful, these terms do not have the same meaning as they do for bipolar devices. In fact, they are almost exactly opposite! In the linear region ($V_{DS} \approx$ 0-5V) the voltage across the channel is not sufficient for the carriers to reach their maximum drift velocity. In this region, the FET operates as a square law device; the static drain-source resistance [$r_{DS(on)}$] is equal to V_{DS}/I_D at each point and the small signal drain-source resistance [$r_{ds(on)}$] is the slope of the transfer characteristic.

As V_{DS} is increased, the carriers reach their maximum drift velocity, and the device enters the saturation region where the output impedance is high (the curves are relatively flat) and the equal spacing between V_{GS} curves indicates constant g_m. In this region, the transfer function is linear.

The output conductance (g_{os}) as a function of drain current and temperature is shown in Figure 10. Note that g_{os} is relatively independent of temperature.

Transfer Characteristics

The transfer characteristic, taken in the saturation region, is shown in Figure 11. The threshold voltage [$V_{GS(th)}$] is defined as the gate voltage at which the device begins to turn on. The threshold voltage can be found by extending the

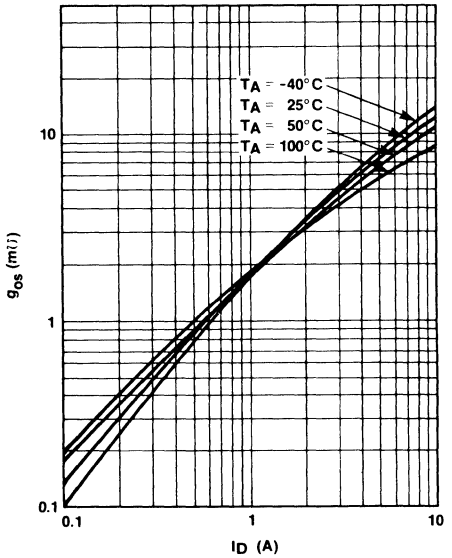

Figure 10. IVN5200 g_{os} vs. I_D

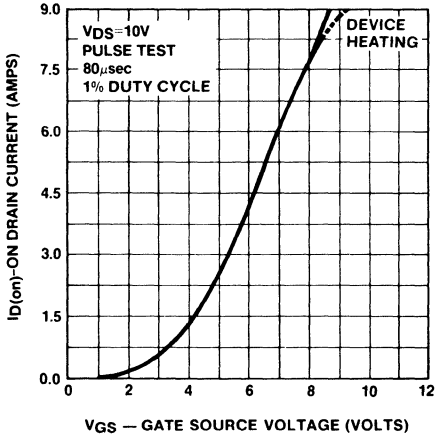

Figure 11. Transfer Characteristic

linear portion of the transconductance curve (Figure 14) to zero. As a practical matter however, because of the inconvenience of this measurement, manufacturers define $V_{GS(th)}$ as the gate voltage at which some small current, usually 1 to 10 mA, depending on the device size, begins to flow, and this value for $V_{GS(th)}$ is usually somewhat higher than the extrapolated intercept. The threshold voltage is a function of temperature; figure 12 shows this relationship for two different IVN5200's. The temperature coefficient is 6 mV/°C. Note that although the two devices have different threshold voltages, the temperature coefficients are nearly identical. This is typical within device types, and extremely helpful when paralleling multiple devices. For switching applications, the variation of $V_{GS(th)}$ with temperature is not very significant, but linear applications may require the bias point to be stabilized by using a source resistance or other negative feedback scheme.

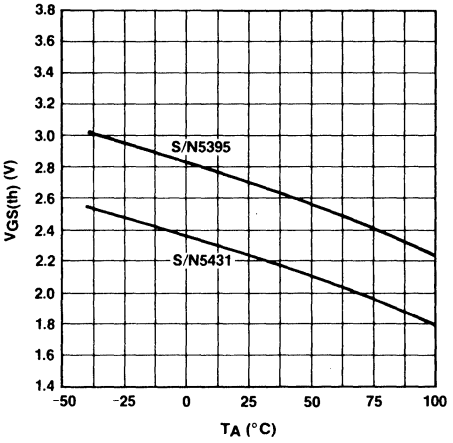

Figure 12. IVN5200 $V_{GS(th)}$ vs. T_A

The small signal forward transconductance (g_{fs}) curves are given in Figures 13 and 14. As shown in Figure 13, for a given V_{DS} the transconductance increases with I_{DS} until a point is reached where the transconductance is constant. This is characteristic of short channel MOS devices.

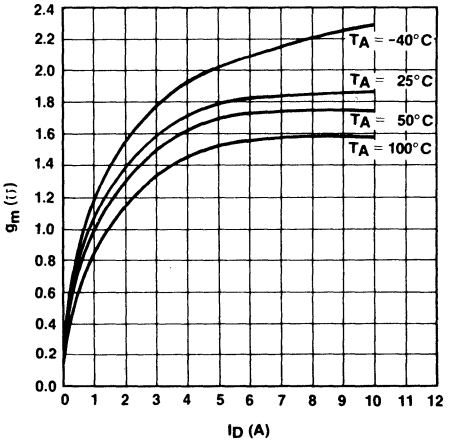

Figure 13. IVN5200 g_m vs. I_D

The $r_{DS(ON)}$ of a MOSFET is made up of two components, the channel ON resistance and the bulk resistance of the device. In low voltage devices (<100V) $r_{DS(ON)}$ is primarily limited by the channel resistance, but in higher voltage devices, the minimum value of $r_{DS(ON)}$ is dominated increasingly by the resistance of the epi layer. The channel resistance is controlled by the degree of gate enhancement, as shown in Figure 15. It can be seen that the ON resistance can be reduced by increasing V_{GS} to about 15 volts. However, a point of diminishing returns, sets in, so that little is gained by going above 15 volts. It is also important not to approach the

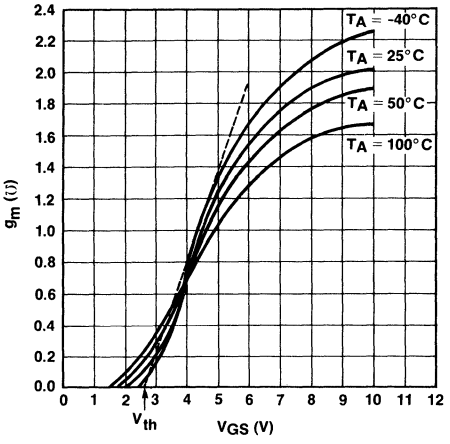

Figure 14. IVN5200 g_m vs. V_{GS}

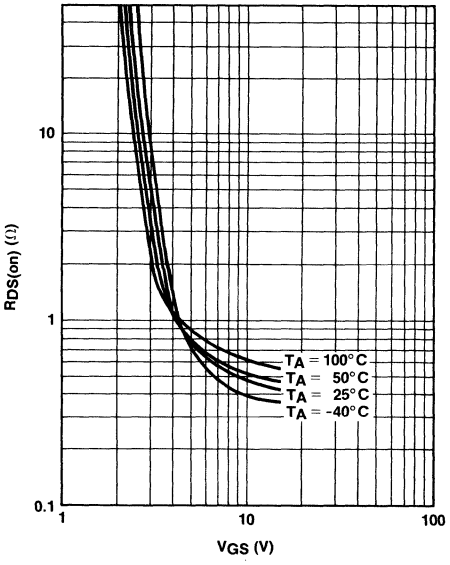

Figure 15. IVN5200 $R_{DS(on)}$ vs. V_{GS}

gate breakdown voltage in the quest for low $r_{DS(ON)}$. For higher $V_{GS(th)}$ devices, the curve will be displaced to the right but the shape remains essentially the same. Figure 16 shows the effect of temperature on $r_{DS(ON)}$ at different values of V_{GS}. Note that the temperature coefficient of $r_{DS(ON)}$ is positive. This positive temperature coefficient is a major reason for the improved safe operating area and ease of device paralleling. The value of this coefficient varies between +0.2 and +0.7%; this is caused by the competing effects of the positive TC of the silicon versus the negative TC of $V_{GS(th)}$. As shown by the curve for V_{GS} = 5V, when V_{GS} is close to $V_{GS(th)}$, the threshold effects predominate, and as the V_{GS} is increased the TC begins to take on the characteristics of the silicon. This example shows a low voltage (80V) device; in high voltage devices, r_{DS} is dominated more by the bulk resistance and the TC is more nearly linear, with typical values of +0.6 to +0.7%.

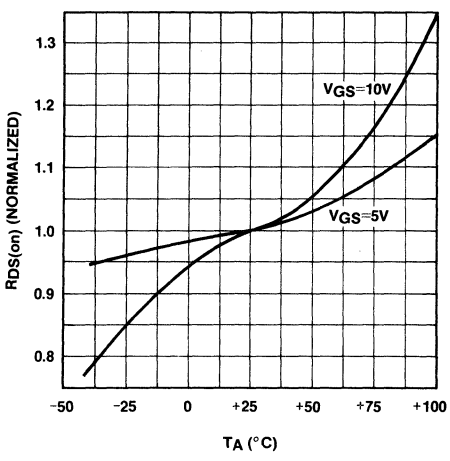

Figure 16. IVN5200 $R_{DS(on)}$ vs. T_A

Input Characteristics

The MOSFET, like the bipolar, displays significant input, output and transfer capacitances that vary with voltage. The gate structure has capacitance to both the source (C_{gs}) and the drain (C_{gd}). The inherent NPN transistor in the structure has a reverse biased PN junction, the base-collector junction, that adds capacitance between the drain and source (C_{ds}). These capacitances are shown in Figure 17. The data sheet does not state these capacitances directly; rather the data sheet gives C_{iss}, C_{rss} and C_{oss}, as shown in Figure 18. C_{iss} is the parallel combination of C_{gd} and C_{gs}, C_{oss} is the parallel combination of C_{ds} and C_{gd}, and C_{rss} is the same as C_{gd}.

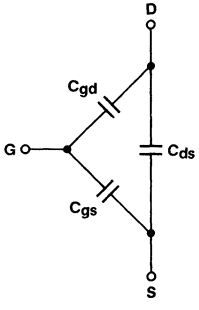

Figure 17.

As in any junction diode, the reverse biased capacitance decreases as the voltage is increased, so that C_{oss} has a much lower and nearly constant value above 10V than near zero. C_{iss} and C_{rss} are also reduced as V_{DS} is increased.

Because of the insulated gate structure, the input current (I_{GSS}) is normally very small, on the order of a few pico amperes at 25°C. This is made up of the leakage current through the gate structure, surface leakage current between

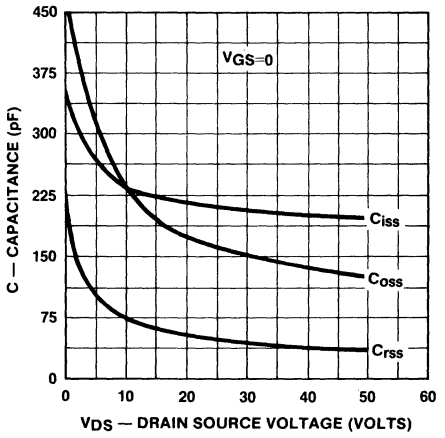

Figure 18. Capacitance vs. Drain-Source Voltage

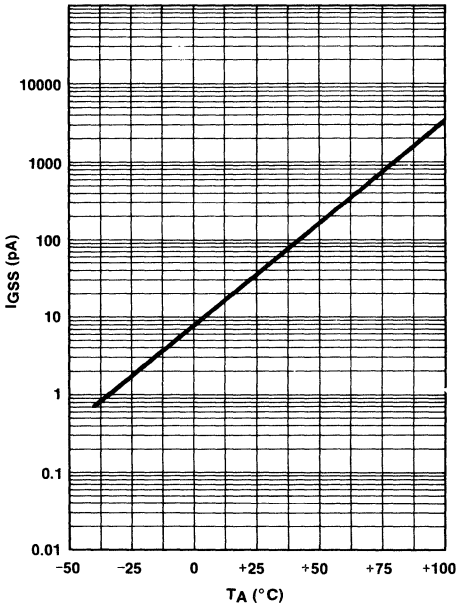

Figure 19. IVN5200 I_{GSS} vs. T_A

the package terminals, etc. Like any leakage current, I_{GSS} will increase exponentially with temperature; a typical characteristic curve is shown in Figure 19.

Occasionally, especially when an aluminum gate structure is used, the gate oxide can be contaminated with sodium ions. This produces a net positive gate charge, even when the gate and source are shorted, and results in a reduced threshold voltage. Unfortunately this is an uncontrolled process, and leads to random $V_{GS(th)}$ variations over life. Use of the silicon gate structure greatly reduces the possibility of sodium contamination.

Switching Characteristics

A major advantage of power MOSFET's is the very fast switching speeds of which they are capable. If one were able to charge the gate capacitance instantaneously, the switching time would be essentially the time it takes for the carriers to travel from the source to the drain. In present devices, this is about 50 to 200 picoseconds. Actual production devices can be switched in less than one nanosecond if a suitable pulse source is used to drive the gate. This can be done with a mercury wetted relay and a transmission line pulse source. For switching times longer than 5 to 10 ns, the turn-on time is limited primarily by the drive source resistance and the input capacitance (Figure 20a). As the switching times are reduced, the effect of parasitic inductances in the package and generator connections become important, (Figure 20b) so that it is difficult to turn on a TO-3 case device in much less than 2 - 3 ns.

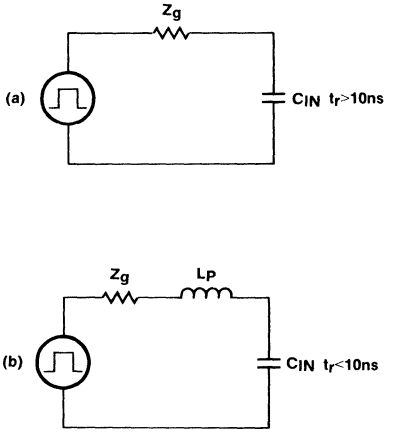

Figure 20.

The MOSFET switching times change very little with temperature, as opposed to bipolars. The idealized switching waveforms shown in Figure 22, presume the use of a specific test circuit like that shown in Figure 21. The actual transition times seen by the user may be greater or less than those shown on the data sheet, depending on the drive available. The delay at turn-on is due to the length of time it takes for the gate voltage to rise to $V_{GS(th)}$, where the device begins to conduct. In most switching applications, sufficient gate drive will be supplied to obtain the minimum $r_{DS(ON)}$; this corresponds to the area in Figure 15 where r_{DS} changes relatively slowly with V_{GS}. The result is a turn-off time delay where V_{GS} has to drop significantly before r_{DS} begins to rise.

The actual switching time test waveforms for a typical IVN5200 switching 60V at 8A are shown in Figure 23. The positive drain voltage spike at turn-on is due to the coupling of the drive pulse to the output by C_{rss} during the turn-on delay time. A similar negative pulse can occur during the turn-off delay time.

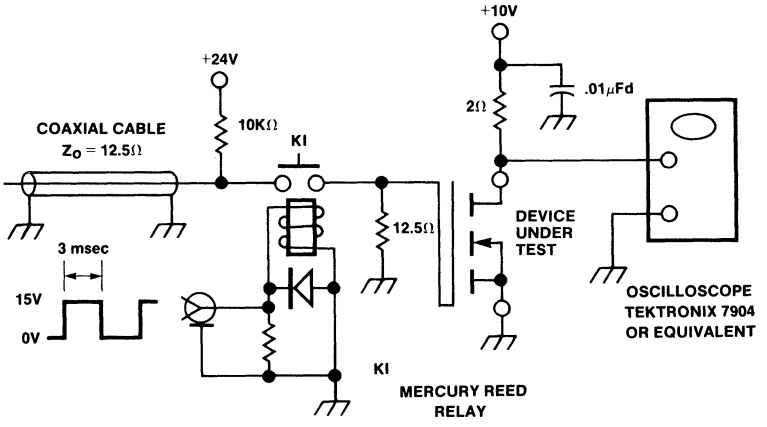

Figure 21. Switching Time Test Circuit IVN5200

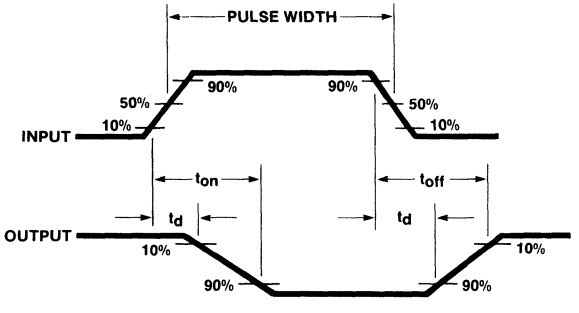

Figure 22. Switching Time Test Waveforms

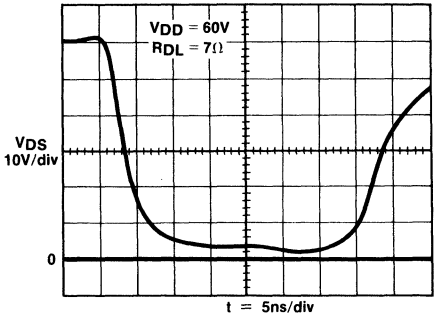

Figure 23. IVN5200

Input Capacitance

The actual gate input capacitance is highly non-linear, so that switching time and drive power calculations based on the average input capacity and the source resistance tend to be rather inaccurate. A better approach is to look at the gate charge as a function of V_{GS}. If the gate is driven from a current source (Figure 24), and the current integrated to give the charge, the curves in Figure 25 are obtained. For simplicity, the curves for V_{DD} = 60V are reproduced in Figure 26.

If one looks at V_{GS} as a function of charge, it is clear that three distinct regions exist and the dynamic input capacitance has a different value in each region. Region 1 corresponds to V_{GS} between zero and threshold, where the device is essentially off. The linearity of the voltage rise indicates that the capacitance is constant. In Region 2, the rate of rise of V_{GS} is sharply reduced, indicating a large increase in capacitance. This corresponds to the region where V_{DS} is falling and the Miller capacity appears at the input. In Region 3, the slope of V_{GS} is again increased, although not quite equal to that of Region 1, and is relatively linear. This corresponds to the region where the device is on and V_{DS} is no longer changing, so that the Miller effect is absent.

If the effective value of C_{IN} in each of these regions is calculated from the slope of V_{GS}, then: $C_{IN(1)}$= 260 pF, $C_{IN(2)}$ = 2900 pF, and $C_{IN(3)}$ = 400 pF. $C_{IN(1)}$ and $C_{IN(3)}$ correspond to C_{iss} in each region. The value of C_{iss} is different in Regions 1 and 3 because the bias conditions within the device are different in each region. In Region 2, $C_{IN(2)} \simeq C_{iss} - Av\, C_{rss}$, where $Av = \Delta V_{DS}/\Delta V_{GS}$, $Av\, C_{rss}$ is the Miller capacity.

The energy (W) required to turn the device ON is:

$$W = 1/2\ (\Delta V_G)\ (\Delta Q_G)\ \text{watt-seconds}$$

If the gate is driven from a resistive source, ON and OFF repetitively, at a rate f_o then the drive power required is:

$$P = (\Delta Q_G)\ (\Delta V_{GS}) f_o$$

Driving an IVN5200 to a V_{GS} of 10V with f_o = 100 kHz, the drive power required is 7.5 mW. This is a vast improvement over a comparable bipolar device.

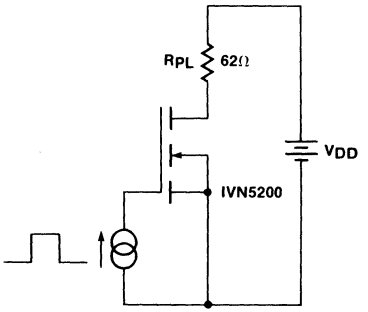

Figure 24.

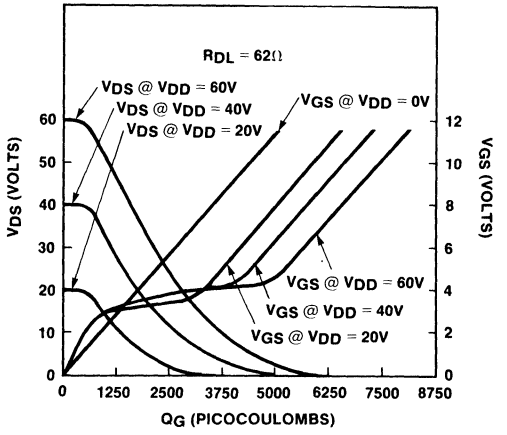

Figure 25. IVN5200 Dynamic Input Characteristics

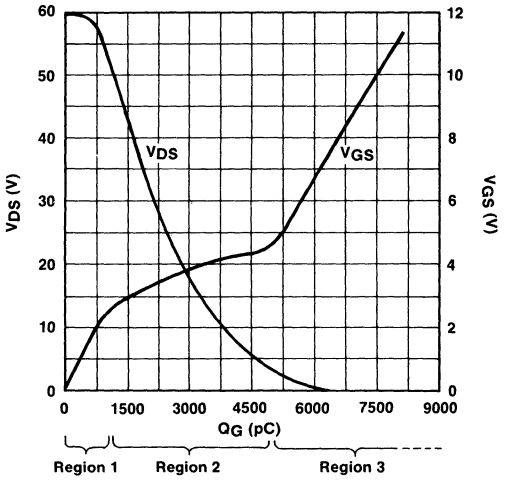

Figure 26. IVN5200 V_{DS} & V_{GS} vs. Q_G

Safe Operating Area

To achieve satisfactory service life from any power semiconductor, the circuit designer must assure that the device is operated within the voltage, current and thermal capabilities inherent in the particular device. To assist the designer, the manufacturer provides a table of maximum ratings, a safe operating area curve (SOAR) and a thermal impedance curve.

A typical absolute maximum ratings table is reproduced in Table I. While the information in the table is useful, it is not sufficient by itself for a power device. To adequately define safe operating conditions it is necessary to use the SOAR curve, like that reproduced in Figure 27. For a power MOSFET, the SOAR curve will have three boundary regions. Region 1 is defined by the breakdown voltage capability of

Table I. Absolute Maximum Ratings
(25°C unless otherwise noted)

Drain-source Voltage	
IVN5200TND, IVN5201TND	40V
IVN5200TNE, IVN5201TNE	60V
IVN5200TNF, IVN5201TNF	80V
Drain-gate Voltage	
IVN5200TND, IVN5201TND	40V
IVN5200TNE, IVN5201TNE	60V
IVN5200TNF, IVN5201TNF	80V
Continuous Drain Current (see note 1)	4.0A
Peak Drain Current (see note 2)	10A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	-30V
Thermal Resistance, Junction to Case	10°C/W
Continuous Device Dissipation at (or below)	
25°C Case Temperature	12.5W
Linear Derating Factor	100mW/°C
Operating Junction	
Temperature Range	-55 to +150°C
Storage Temperature Range	-55 to +150°C
Lead Temperature	
(1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(ON)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

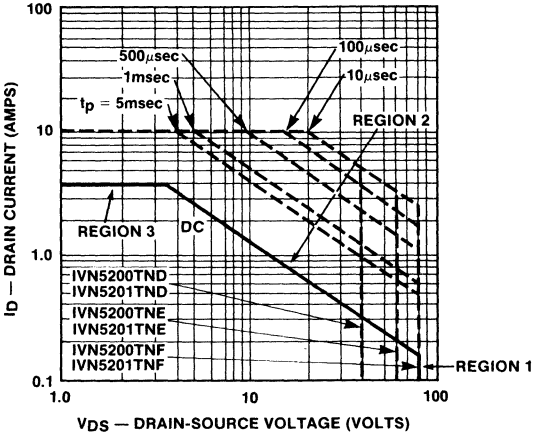

Figure 27. SOAR

the device. Region 2 is defined by the thermal capability of the device. Normally a maximum junction temperature of 150°C is specified, so that in Region 2 the power dissipation is limited to a *peak* junction temperature of 150°C. This results in Region 2 being defined by a family of curves that allow higher peak power for shorter pulse widths. Region 3 is defined by the current capability of the device. The current capability of a given device may be limited by the bond wire diameter, the area of the bonding pad on the die, or by the metallization on the die surface. Whereas the breakdown voltage and junction temperature limitations can be readily determined by direct measurement, the current limitations are empirically derived from life testing. The maximum current is limited to a value which has been found to give an acceptable service life. In a bipolar transistor, the rapidly decreasing h_{FE} at high currents effectively discourages operation in excess of the current ratings. In a MOSFET, however, the gain is not reduced at high currents, and there may be a temptation, in fast pulse applications where a high drain-source voltage may be acceptable, to operate with very short high current pulses in excess of the ratings. Even if the device dissipation is very low, this is inadvisable for two reasons. First, the reliability or service life of the device is undefined and likely to be shortened, and second, if the current density in the device is increased sufficiently, it is possible to reach the level where current injected avalanche breakdown occurs, possibly destroying the device.

For a bipolar transistor the SOAR curves will have a fourth boundary. This region is defined by the thermally induced second breakdown characteristic. In a bipolar device, there are several ways to induce secondary breakdown. The first is thermal, where the negative temperature coefficient of the conduction resistance causes localized hot spots to be formed. When the temperature of a hot spot is sufficiently high, it's impedance is drastically reduced, funneling the collector current through a small area and usually destroying the device. Another mechanism for inducing secondary breakdown is via avalanche breakdown. If the collector voltage is raised to the breakdown point of the collector-base junction and a significant current allowed to flow, the device will go into secondary breakdown. It has been widely advertised that MOSFET's do not exhibit secondary breakdown. This is not true. It is generally accepted that at normal junction temperatures, the thermally induced secondary breakdown phenomena so prevalent in bipolar devices is not present in MOSFET's, however the avalanche induced secondary breakdown is. This is not surprising; as shown in the earlier discussion the MOSFET structure has within it an NPN transistor, and the voltage limit on that device is the base-collector junction breakdown voltage. The current level at which primary breakdown becomes secondary breakdown, is a function of the base emitter resistance, the temperature and the h_{FE} of the bipolar device. In a MOSFET, the base and emitter are shorted right on the die, and for reasons of improving the dV_{DS}/dt characteristic, the resistance is made as low as possible. In addition, the h_{FE} of the MOSFET parasitic bipolar is much lower than a typical bipolar device. The result is that the current level at which primary breakdown becomes secondary breakdown is much higher in a MOSFET than it is in a comparable bipolar transistor. The device ratings are selected so that the maximum V_{DS} is well below the actual breakdown point in the production devices. Current injected avalanche breakdown, present in bipolars during reversed bias operation, can also lead to secondary breakdown in MOSFET's. For a given field gradient within the semiconductor there is a maximum current density threshold above which self-sustaining avalanche breakdown can occur. This is a basic limitation on the current handling capability of a power device. In present MOSFET's the internal current densities are limited by design, so that the junction temperature thermal limit is reached well before any current injected avalanching is present. Both of these breakdown modes lie well outside of the published SOAR curves, and neither is of direct interest to the device user. Due to the absence of thermally induced second breakdown, the SOAR for a MOSFET is greatly expanded over that of a comparable bipolar.

The normal manufacturers' SOAR curve is for a case temperature of 25°C and either DC or a *single* pulse. In the real world, of case temperatures above 25°C and repetitive pulses, the designer must modify the standard SOAR curves for his particular application. This can be done by using the transient thermal impedance $Z_{(th)}$ curves which should be made available by the manufacturer. 3,4

dV_{DS}/dt Limitations

The inherent bipolar transistor within the MOSFET structure can impose a limit on the rate of rise of V_{DS}. Figure 28 is an equivalent circuit where the parasitic bipolar transistor is shown in parallel with the MOSFET. Even though the emitter N+ and base P regions are connected at the surface of the die by the source metallization, there is still a significant base emitter resistance (R_{BE}) due to the bulk resistance of the N and P regions. In addition, the collector-base junction has capacitance (C_{ob}). When V_{DS} makes a positive transition, a current will flow through C_{ob}; $I = C_{ob}(dV_{DS}/dt)$. As V_{DS} rises more rapidly, more current flows through C_{ob} until a point is reached where the voltage across R_{BE} is sufficient to turn on the transistor, Q1. This undesirable turn-on or switchback of the parasitic NPN transistor interferes with the normal circuit operation and can destroy the device. The threshold for switchback varies widely from one device type and manufacturer to another. Maximum dV_{DS}/dt information is not yet a standard entry on the data sheets so the user will have to either consult with the manufacturer or test the devices himself. The IVN5000 and 5200 series parts will accept at least 20V/nsec. The dV_{DS}/dt rating of a device can be improved by designing the die layout to minimize the base

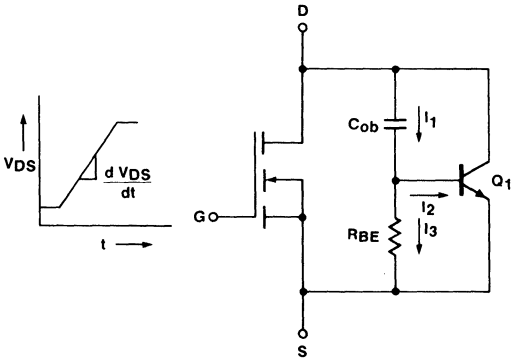

Figure 28. Parasitic Bipolar Switchback Equivalent Circuit

emitter resistance, and by controlling the P region doping to produce a bipolar with low h_{FE}. As in any bipolar transistor, the h_{FE} of the parasitic NPN is a function of temperature and the dV_{DS}/dt snapback threshold will decrease at high temperatures.

Use of the Internal Diode

For values of V_{DS} risetime below the threshold of switchback, the internal NPN transistor is inactive, and acts simply as a bipolar with the base shorted to the emitter. The equivalent circuit could be redrawn, as shown in Figure 29, with a diode in parallel with an ideal MOSFET. If V_{DS} is reversed, this diode will conduct and may be used in switching circuits as a rectifier or inductive energy clamp. The forward current and breakdown voltage ratings of this diode are equal to the current and voltage ratings of the parent MOSFET. The reverse recovery time t_{rr} of this diode can be excellent; the IVN500 and 5200 series devices have a typical t_{rr} of 60 to 70 ns. There are several reasons for the good recovery time of this diode. First, the MOSFET fabrication process produces essentially lightly doped epitaxial diodes with sharply defined doping gradients. Second, the P region is often formed by ion implanting, a process that causes dislocations in the crystal structure. These dislocations can act as recombination centers for the junction stored charge, thereby reducing the recovery time. The diode recovery time is senstitive to the process used and can vary widely from one manufacturer to another. Since t_{rr} is not, at present, a data sheet entry, the user is advised to contact the manufacturer for values.

The FET itself may be used as a synchronous rectifier. Once the channel has been formed by making V_{GS} positive, current will flow through the device in either direction with equal facility. For synchronous rectifier operation, V_{GS} is zero during the period when the drain is positive with respect to the source; when V_{DS} reverses, the gate is enabled and current flows through the device in the reverse direction. The forward drop is proportional to $r_{DS(ON)}$ and the current flowing; when the threshold of the parallel diode is reached the current will bypass the FET channel and the rectifier will act like a normal PN junction diode.

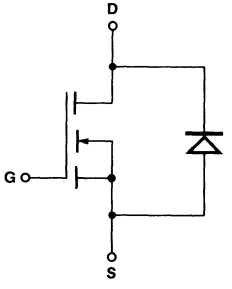

Figure 29.

For currents below the 0.6V diode threshold, the FET acts as an ultra high speed, high voltage, low capacity rectifier with no minimum offset voltage. This type of operation has been used for a power rectifier at 15 MHz. Presently available MOSFET's can be used in this manner, with the only drawback being the relatively high $r_{DS(ON)}$ values which restrict the current. In the future, it is reasonable to expect that low voltage, low $r_{DS(ON)}$ devices will be designed specifically for this service, which will make possible the efficient generation of large amounts of 2V or 5V power.

Internal Zener Protection

The first VMOS devices to appear on the market included an on-chip zener diode from gate to source to prevent gate breakdown due to static charging. This was formed by diffusing in an additional NPN transistor (Figure 30), with the zener action accomplished by the reverse breakdown of the base-emitter junction. The zener formed in this manner has a number of drawbacks. First, the power dissipation is very limited, 2 mA DC being typical, and second, if the gate is pulled negative to -0.6V or more, the NPN transistor will turn ON and draw current from the drain circuit. This may destroy the transistor. The result is poor reliability in many applications. Experience has shown that the gate structure of a power MOSFET is much more rugged than the gate structure in MOS IC devices, and given reasonable care in packaging, handling and installation there is no need for this zener in most applications.

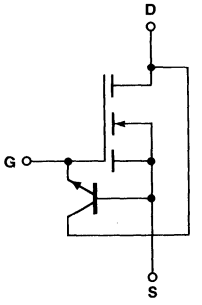

Figure 30. Parasitic NPN Transistor with Internal Zener

Multiple Device Operation

The positive temperature coefficient of $r_{DS(ON)}$ is of great assistance when MOSFET's are paralleled. It is possible, in DC applications, to parallel devices without any matching, and those devices that initially draw the most current will heat up and shift the current to other devices to more equally distribute the current. This is exactly the opposite of the scenario for bipolar devices. While the paralleling of unmatched devices will work, it is a poor idea because in DC applications a higher than necessary dissipation may occur and in switching applications it is possible for one device to turn on or off, before or after the other devices and have to accept the full load current. This may force the device to function outside of its safe operating area.

It is recommended that the user parallel devices which have been matched for $V_{GS(th)}$ to within 5 to 10% accuracy. This will assure that the turn-on and turn-off delays due to the gate voltage rise and fall times, relative to $V_{GS(th)}$, are nearly equal. $r_{DS(ON)}$ will also be matched, so that excessive differential heating is not required. Some additional improvement in $r_{DS(ON)}$ matching may be achieved by providing a higher V_{GS} drive so that all of the parallel devices run at their minimum $r_{DS(ON)}$ value.

It should be kept in mind that many MOSFET devices have gain bandwidths over 500 MHz. It is entirely possible for these devices to oscillate at very high frequencies, especially if multiple parallel devices are used. This is often an unsuspected cause of device failure. If the circuit designer is using a low bandwidth oscilliscope during breadboard development, it is possible not to be aware of the self oscillation therefore, use of an oscilliscope with a bandwidth of at least 200 MHz is recommended. The tendency towards oscillation can be greatly reduced by inserting ferrite beads or low value (50 - 100 ohm) resistors in series with the gate leads as shown in Figure 31.

For fast pulse applications, it is not sufficient to just match the devices. The circuit must also be reasonably symmetrical so that identical drive voltages are applied to each gate. At high speeds the inductive, as well as resistive, effects must be considered. If, for example, the parasitic inductance in the drain lead of Q_1 is much smaller than that in the drain lead of Q_N, when the devices are first turned ON most of the load current will initially flow through Q_1, even if the gate drives and threshold voltages are identical.

Variations in the stray gate circuit capacity and the device input capacity can also cause uneven turn-on in fast pulse applications. The effect of this can be reduced by equalizing the stray capacity and minimizing the intergate impedances. For applications requiring switching times below 5 to 10 ns., it may be necessary to match the device capacitances.

It should be kept in mind that most of the complications to paralleling mentioned above generally apply only for very fast pulses. Most applications will use transition times well above 10 nsec, where simple threshold voltage matching is all that is required. This is quite different from bipolar transistors, where paralleling more than two devices can become quite complex and expensive. Due to the practical difficulties of paralleling large numbers of individual bipolars, (and SCR's also), the trend has been to develop ever larger single devices. As the die size increases, a point is reached where either the thermal capabilities or the available mounting areas in the low cost packages are exceeded so that an expensive package is required. The heat sink will now see a concentrated thermal input through the relatively small package to heat sink contact area. The efficiency of a heat sink is better if the heat input is distributed in several sources rather than in one. While the arguments for using a single large bipolar device instead of multiple smaller devices are well founded, it does not necessarily follow that the same technique should be imitated in power MOSFET devices, especially in the light of the rapid cost increase of the larger die. The tradeoff may well be multiple small devices with low die and package and moderate heat sink costs, versus single devices with high die, package and heat sink costs. Just where the cost crossover point between single and multiple devices will be is yet to be determined, especially since the very high prices for the present larger MOSFET chips is certain to be reduced substantially. In any case, the user should be aware of this tradeoff which is quite different from bipolars, and not unnecessarily perpetuate the bias against parallel bipolars into the application of power MOSFET's.

Similar considerations apply if devices are to be operated in series. It is particularly important that all devices in the same series string come ON simultaneously, otherwise one device may take all of the voltage momentarily. The devices should be well matched for $V_{GS(th)}$ and careful attention given to producing simultaneous gate drive. In those applications where the maximum possible voltage capability is desired, it may be necessary to match the $r_{DS(ON)}/V_{GS}$ characteristic to assure equal voltage distribution during switching transitions. This is a much more complex procedure than $V_{GS(th)}$ matching, and should be considered only as a last resort. Analogous to the parasitic inductance in parallel operation is the effect of circuit parasitic capacitance in series operation. If differential drain-source capacitances (either in the device or in the circuit layout) exist in the series string, the transient voltages may not be shared equally.

RADIATION EFFECTS

The effects of nuclear radiation on power MOSFET's is beginning to receive a good deal of attention, although very little information has been published to date. Mr. John Buck, a radiation effects specialist with Litton Guidance and Control Systems, has provided the following information:

". . . When used in military systems with a nuclear hardening specification, VMOS and bipolar power devices have differ-

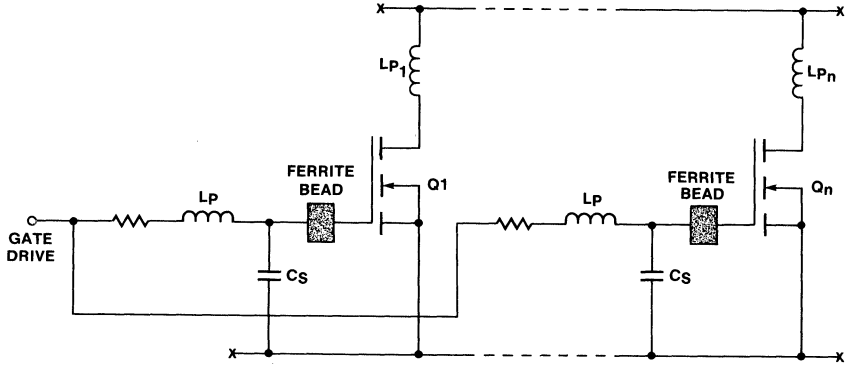

Figure 31. Parallel Devices

ent susceptibilities to the neutron and total dose radiation environments. VMOS devices are almost immune to neutron damage because they are majority carrier devices. Bipolar power devices, on the other hand, suffer considerable gain degradation in even moderate neutron environments. VMOS devices, however, are more adversely affected by the total dose (gamma) environment than are bipolar devices.

"Total dose damage to MOS devices occurs as a result of (the) trapped charge in the gate oxide layer. Charge is created when gamma particles collide with (atoms) in the oxide layer causing formation of electron — hole pairs. The electrons are more mobile than the holes, and are (more) easily swept from the oxide layer. The holes, on the other hand, tend to drift toward trapping sites where positively charged hole layers are formed. This positive charge remains in the oxide layer and causes the gate threshold voltage of the device to decrease. Total dose damage to MOS devices is measured as a shift in gate threshold voltage. Drain leakage current also increases with total dose as a result of the gate charge buildup.

"Two other factors are important in discussing total dose damage effects in MOS devices. One is the amount of gate bias applied during irradiation and the other is the effect of annealing. The more positive (the) gate bias applied during irradiation the greater the total dose damage. This is because the holes will migrate to trapping sites closer to the sensitive Si-SiO_2 interface.

"Annealing, on the other hand, is a curing effect since the process of annealing is the recombination of holes with electrons with (the) resulting decrease of trapped positive charges. Annealing will take place at room temperature, and the rate of annealing will increase at higher temperatures due to increased hole de-trapping.

"Derbenwich[5] has studied the combined effects of total dose damage and annealing. His method involves measuring gate threshold voltage shift versus total dose to determine a linear damage region for the device. Then another set of the same device type is irradiated to a dose level within the linear damage region and then allowed to anneal at room temperature under fixed bias for several weeks or longer. A transient annealing function is then determined for the device. His theory then states that the convolution of dose rate versus time with the transient annealing function predicts the net shift in gate threshold voltage when annealing is occuring simultaneously. This model provides a means for calculating MOS damage in low dose rate long term environments where annealing is a significant factor. A typical long term ionizing radiation environment is a satellite space application where the system may be irradiated and anneal simultaneously for a five year mission."

Test Results

"Figure 32 shows that total dose damage to IVN5000 parts is linear to about 5000 rads (Si) for bias voltages of 0, 2.5V and 5V. The horizontal error bars are dosimetry error estimates. Vertical bars are standard deviations based on a sample of five parts tested. Preliminary tests at higher bias voltages indicated device failures at much lower dose levels. Device

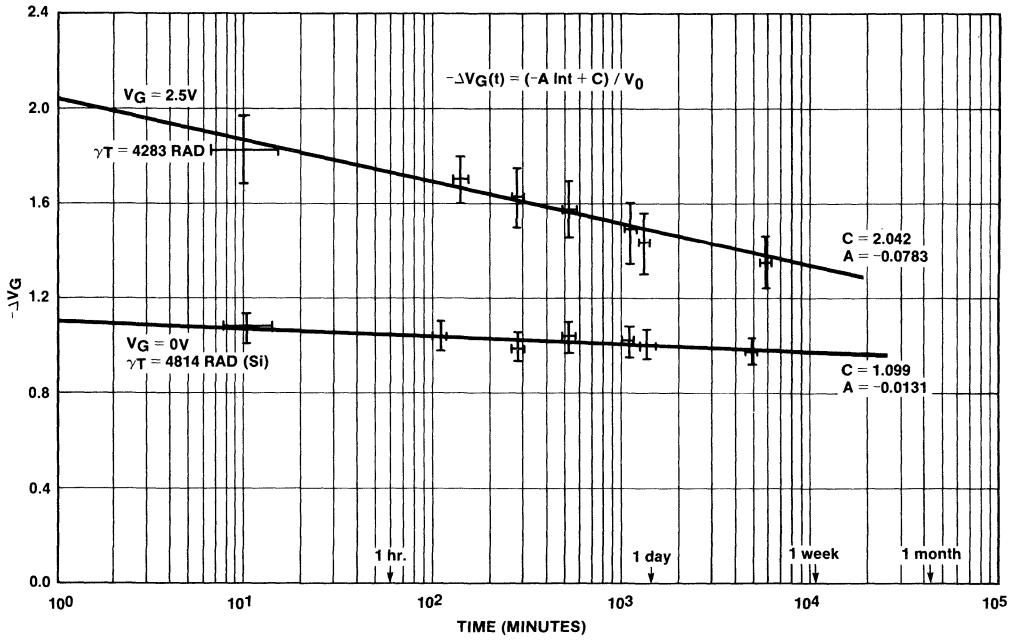

Figure 32. VMOS LINAC Annealing Curves

failure on these tests was due to leakage currents approaching or exceeding the drain currents at which the DC gate voltage measurements were made (500μA). Pulse testing at higher currents may have allowed gate voltage measurements to be made at slightly higher dose levels.

"Figure 33 shows the results of the annealing measurements made for 0V and 2.5V biased parts after LINAC irradiations to 4814 rad (Si) and 4283 rad (Si) respectively. It can be seen from Figure 33 that these total dose irradiations are within the linear damage regions for the device."

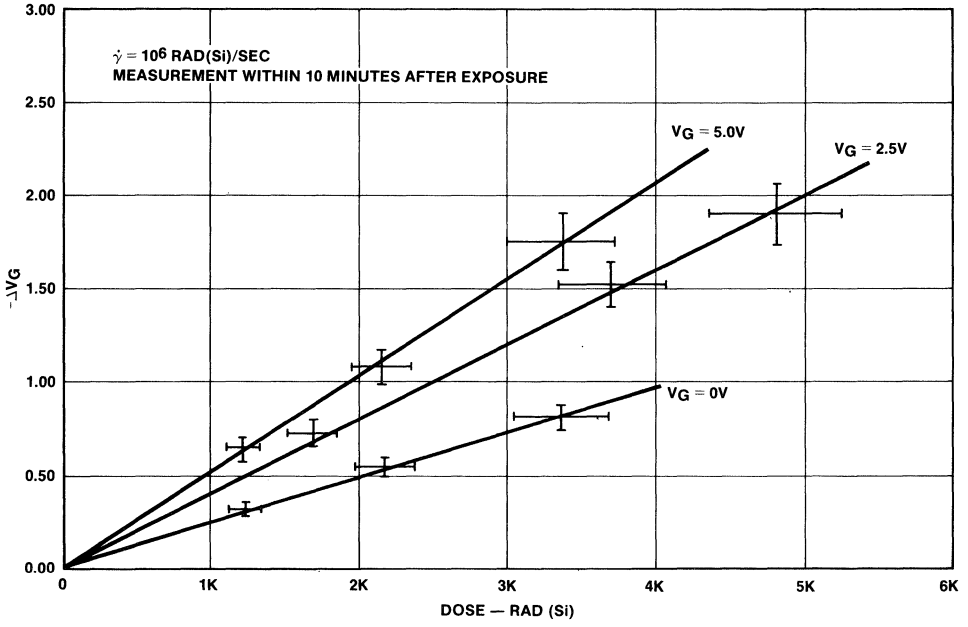

Figure 33. VMOS LINAC Test Results

ACKNOWLEDGEMENT

The author would like to thank B. Rosenthal, N. Zommer, and B. Wier for their assistance in preparing the discussion on structures and B. Smithson who did the characteristics curves.

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INTERSIL

AO34
Switchmode Converters Above 100 kHz

by Rudy Severns

With the introduction of power MOS switches, and the general improvement in other components, it is now possible to design switchmode converters with switching rates in the range of 100 kHz to 5 MHz, and from both off-line and low voltage DC bases.

Unfortunately, a 200 kHz switchmode converter is a bit more than just a higher frequency version of the conventional 20 kHz converter. While the circuits and components used are similar, there are a host of significant differents which alter the design.

HOW HIGH IN FREQUENCY?

Early in the design process, a decision must be made on the switching frequency. Most performance parameters (cost, volume, bandwidth, efficiency, etc.) change rather slowly with increasing frequency, so there is relatively little to be gained by going up by a factor of two or three. If significant improvements are to be achieved, the switching frequency must be increased enough to not only reduce the size of the magnetic components, but also to enable the use of alternate components and materials which provide lower cost, improved performance or both. Real changes do not appear until the switching frequency has been increased by an order of magnitude or more.

The choice of operating frequency is influenced by the converter specification, the choice of switch (bipolar or MOSFET) and the power level. For offline switchers using bipolar switches, the optimum frequency would be about 200 kHz. From low voltage DC sources, the switching frequencies using bipolar devices can be increased to 300 to 600 kHz. If power MOSFET switches are used, the switching frequencies may be increased to the megahertz range, and there is increasing evidence that this may be desirable, for low power at least. As the power level goes below 100 watts, less and less is gained from operating around 200 kHz, the reason being that the components don't really get much smaller or cheaper. If real improvements are to be made at low power, new designs should operate in the low MHz region using air core magnetics and MOSFET switches. Fortunately, the lower the power level the easier it is to go up in frequency. As the output power is increased above 1KW, when using bipolar switches it will be necessary to reduce the switching frequency towards 100 kHz because the available large devices are somewhat slower. As large power MOSFET's become available, higher frequency operation will be possible.

CIRCUIT TOPOLOGY

Having chosen a switching frequency, the next step is to select circuit topology. While the common 20 kHz converter topologies (parallel, half-bridge, full bridge, etc.) can be used at 200 kHz, the performance can be a good deal less than optimum.

As shown in Figure 1, the converter can be viewed as having primary and secondary topologies connected by a transformer. Because of the difficulties of designing the power transformer at 200 kHz, each of the three circuit elements must be considered in relation to the other two. For example, the incorrect selection of primary switch or output rectifier connection may make the transformer impractical at 200 kHz.

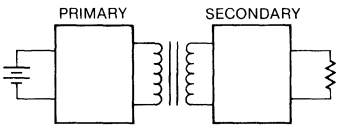


Figure 1.

For primary topologies, the designer must chose between switchmode (modified square waves) or resonant converters. If switchmode is desired, then the choice is between voltage-fed, current-fed with non-overlapping switch conduction, or current-fed with overlapping switch conduction. Table I is a comparison, pro and con for these options.

A variety of resonant circuits are available [1,2,3,4] to the designer but, except for the work by Miller, these circuits have not yet been widely used at high frequencies. Thus, it is difficult to comment on their use from direct experience. From a theoretical point of view, however, the resonant converters should work very well indeed, and if it is possible to operate the current-fed switchmode circuits in the resonant mode by adding a resonating capacitor, then a large number of new resonant converter topologies will be available to the designer. It is also possible that some of the series and parallel commutated SCR inverter circuits can be used as high frequency resonant converters, with power MOSFETs instead of SCRs as switches. The use of resonant converters, at high frequencies, deserves a good deal more attention than is being given at present.

Examples of good and poor choices for high frequency circuit topologies are shown in Figures 2 and 3. Figure 2 is a current-fed circuit; [5] Figure 3 is the common voltage-fed bridge quasi-squarewave converter. A comparison of the two circuits is given in Table II. In general, the current-fed family of converters is more suitable for high frequency switchmode converters.

Table I. Regulator Topology Tradeoffs

PRO	CON
Voltage Fed Converter	
1. Wide Variety of Circuits 2. Good Output Regulation at Heavy Loads 3. Circuit Well Understool	1. Current Spikes can be severe 2. Switch Overlap is Fatal 3. Capacitive Losses Poor at Low Powers 4. Poor Output Regulation at Light Loads 5. Poor EMI Characteristics 6. High Switch Transition Stress
Current Fed Converter	
1. Wide Variety of Circuits 2. No Current Spikes 3. Storage Time Overlap OK 4. Good Multiple-Output Regulation at All Loads	1. Voltage Spikes 2. Capacitive Losses Poor at Low Power 3. Moderate EMI Characteristics 4. Moderate Switch Transition Stress
Resonant Converter	
1. Low Switching Transition Stresses 2. Low Capacitive Loss 3. Low EMI	1. Resonating Capacitors a Problem 2. Q Multiplication Increases Currents or Voltages 3. Fixed Frequency Operation Presents Problems 4. Circuits Tend to be More Complex

Table II. Circuit Comparisons

Figure 2	Figure 3
1. Even with fast recovery diodes, the reverse recovery time of the output rectifiers, is a significant portion of the operating cycle. D1 will be in forward conduction while D2 is still recovering. This places a short circuit across the secondary which is reflected into the primary. Because this circuit is current-fed, the only effect is to slightly increase the energy stored in L1 preventing current spiking in the switches.	1. During the rectifier reverse recovery time, a current spike is reflected into the primary switches. At 200 kHz, the transformer leakage inductance is made quite small by design, so there is very little impedance to limit the current spike. If Schottky barrier diodes are used, the large diode capacitance will also cause primary current spikes.
2. Using the full wave rectifier shown, the output rectifier reverse voltage will be twice the output voltage plus one diode drop (not including noise), irrespective of the line voltage, so that hot carrier diodes can be used at voltages above 5 volts.	2. For a given output voltage, the diode reverse voltage is relatively high. As an example, with a 5 volt output and a 2:1 line excursion, the rectifier reverse voltage varies from 11.7 to 22.8 volts. If the switch storage time reduces the maximum ON time to prevent overlap, the reverse voltage is even higher. The higher reverse voltage also increases the dV/dt that the rectifier is subjected to.
3. At high frequencies, there is a greater tendency towards primary volt-second asymmetry, especially if bipolar switches are used. This can cause core saturation current spikes in voltage fed topologies. In this circuit, spiking is prevented by L1, and core saturation is relatively harmless. Current spikes due to reflected capacity and switch overlap, are also suppressed.	3. There is no protection from core saturation, switch overlap or reflected winding capacitance current spikes. In the case of bipolar switches, the need to prevent overlap due to storage time, allowing for manufacturing and temperature variations, can significantly reduce the pulse width dynamic range. Core saturation can be reduced by inserting a series capacitor in the primary, but this capacitor must be carefully selected to prevent core saturation during fast line or load slewing.
4. Because a single choke is common to all outputs, cross regulation between the outputs for varying loads is relatively good.	4. Separate chokes are required on each output, and for good regulation each choke must remain in continuous conduction. There is no compensation for the choke resistive regulation effects. The net result is that at 200 kHz, the cross regulation of multiple outputs is poor.
5. Diodes D3 and D4 do not see a reverse potential at the end of their conduction cycle, so the reverse recovery time of these devices is not critical.	

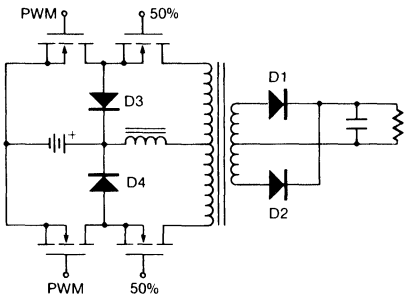


Figure 2.

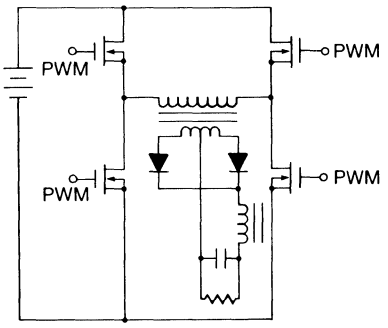
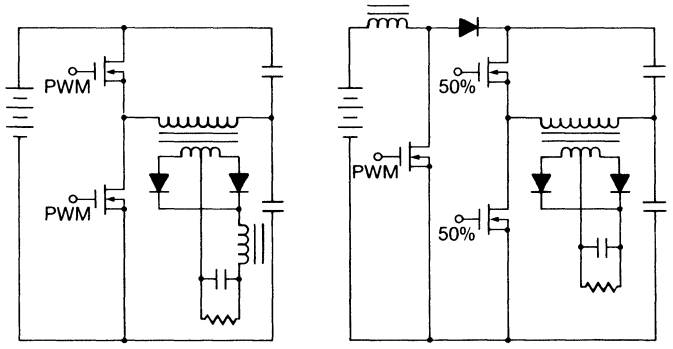


Figure 3. Quasi-Squarewave Converter



Half-Bridge

Low Line, P_T = 35.8W
High Line, P_T = 12.9W
T_j = 122°C

(A)

Boost Regulator/Half-Bridge

Low Line, P_T = 9.1W
High Line, P_T = 6.5W
T_j = 63°C

(B)

Figure 4.

Not only the switching frequency, but the choice of switch can affect the choice of topology. For example, if power MOSFETs are used as switches, the topology selected can have a profound effect on the conduction losses. A simple example is shown in Figure 4. Figure 4(a) is a normal half-bridge quasi-squarewave converter, while 4(b) is an unmodulated half-brdige preceeded by a boost regulator. Given the conditions in Table III, the power losses for (b) are much lower than (a). Because the cost of power MOSFETs is a strong function of $1/r_{DS}$, the three devices used in (b) may be much cheaper than the two devices in (a). While this is a fairly simple example, the boost derived family of converters generally provides lower MOSFET conduction losses than buck derived current-fed converters. Figure 5(a) and (b) shows two examples of boost derived current-fed converters, one using overlapping conduction and the other a secondary shunt switch. There are many other possible circuits[6] that may be used. Unfortunately, the boost family of converters has disadvantages also:

1. The control loop transfer function contains a right half-plane zero which is difficult to compensate for with single loop feedback. By using multiple AC and DC loops, this problem can be overcome.
2. The output ripple current in a boost converter is discontinuous (the input current is continuous) so that the

Table III. Power MOS Topology Conduction Loss Comparison Assumptions

1. P_O	= 200W
2. η	= 80% Without Switch Losses
3. V_{DC}	= 200V to 375V
4. T_A	= 50°C
5. r_{DS}	= 2.5Ω at 25°C
6. Filter Inductor is Large	
7. BV_{DSS}	= 450V to 500V
8. θJ_A	= 4°C/W (TO-3 Case and Heat Sink)
9. r_{DS}	Temperature Coefficient is 0.6%/°C

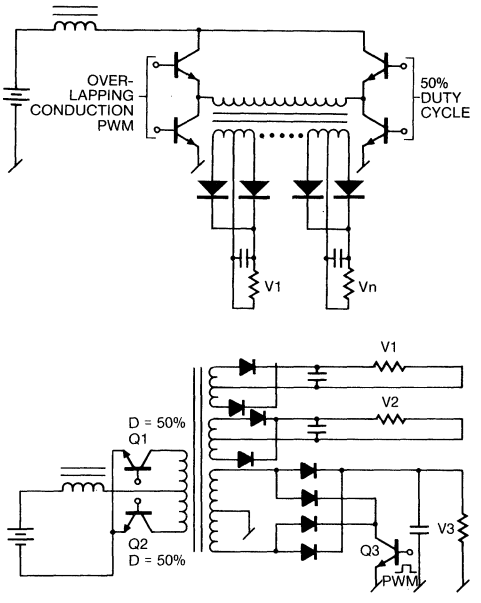


Figure 5.

output ripple current is large. As yet, low voltage (<50V) high current film capacitors are not available, so some penalty in volume is paid for low voltage outputs.

3. In those converters using overlapping conduction in the primary, a large voltage spike can be generated due to the interruption in the primary by secondary leakage inductance current. When the shunt switch is in the secondary, this spiking is greatly reduced.

The output winding/rectifier topology must also be carefully selected with an eye to transformer limitations and primary topology requirements. Figure 6 shows two rectifier connections for multiple outputs. In (a), separate windings are used, and in (b), an autotransformer connection is used. If DC isolation between outputs is not required, then the connection

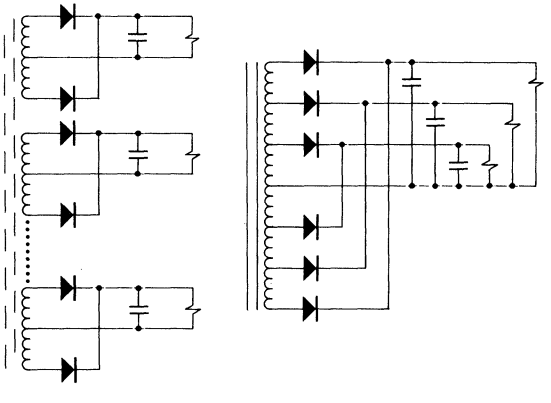


Figure 6.

in (b) should be used because it will give much better cross regulation. A major cause of poor cross regulation is the leakage inductance between the secondary windings, proportionally somewhat worse at high frequencies. The autotransformer minimizes the leakage inductance, as well as providing some resistive compensation for load variations.

In the case of a high voltage output, the designer is faced with the choice of multiple windings or voltage multipliers (Figure 7). It can be very difficult to build a satisfactory transformer for connection (a) due to the need for stacked insulated windings. Because the insulation spacing is related to the voltage and not to the operating frequency, good primary-to-secondary coupling and uniform predictable winding voltages are very difficult to achieve at 200 kHz. The voltage multiplier makes the transformer design easier, but requires a large number of capacitors. Fortunately at 200 kHz, these capacitors can be quite small. The diode shunt capacity is the most serious limitation for high frequency multipliers, but for small multiplication ratios (3 to 5) and reasonable power levels (>10W) this does not seem to be a serious problem. Present experience indicates that for voltages over 1KV, the use of multipliers should be considered, if only for the sake of the sanity of your magnetics designer. The reflected capacitance from the high voltage secondary will be quite large, especially if a multiplier is used. Even allowing for the increased leakage inductance, the primary switch currents are usually unacceptable in voltage-fed topologies; some form of current-fed topology will give much better performance. The voltage multiplier will see wide low amplitude current pulses rather than short duration high amplitude current spikes, and this will reduce the losses and improve the output regulation.

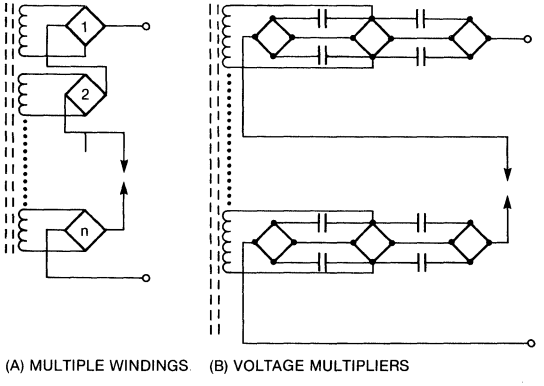


Figure 7. HV Rectifier Schemes

FEEDBACK LOOP CONSIDERATIONS

Increasing the switching frequency from 20 to 200 kHz provides a similar increase in the feedback loop gain cross-over frequency. Given the proper type of control loop and compensation, a gain cross-over of 20 to 100 kHz is possible, comparable to the usual series regulator. While it is possible for the designer to put in a single low frequency pole with gain cross-over at 1 to 2 kHz and have performance equal to a 20 kHz switcher, most designers will opt for higher bandwidth. As with the input and output topologies, the feedback scheme must be carefully considered. Table IV is a

Table IV. Fixed Frequency Control Options

1. Single DC Loop 2. DC Loop and Switch Peak Current Control
3. DC Loop and Choke Voltage Sensing
4. Feed Forward

PRO	CON
Single DC Loop 1. Well Understood 2. Simple Control Circuits 3. For 20 kHz Equivalent Performance a Single Low Frequency Pole May be Used	1. Moving Capacitor ESR Zero Uncompensated 2. Variable Load Capacity is Uncompensated 3. Load Capacity May be Much Larger than IC Filter Requirements 4. Two-Pole Rolloff with Peaking 5. Boost Converters have Right Half-Plane Zero 6. Gain Crossover Limited to 10-15% of f_O 7. No Inherent Current Limiting
DC Loop and Switch Peak Current 1. Inherent Overcurrent Protection 2. Inherent Soft Start Capability 3. Higher Gain Crossover Frequency 4. Single Pole Rolloff 5. Inherent Current Sharing for Parallel Modules	1. More Complex Control Circuit 2. Requires Switch Current Sensor 3. No Compensation for Moving ESR Zero 4. No Compensation for Varying Load Capacity
DC Loop and Inductor Voltage Sense 1. Higher Gain Crossover Frequency 2. Right Half-Plane Zero Compensation 3. Compensation for Variable Load Capacitance 4. Moving ESR Zero Compensation 5. Single Pole Rolloff	1. Complex Control Circuit 2. Choke Voltage Sensor Required 3. No Inherent Current Limiting
Feed Forward 1. Very Simple in DC Loop Systems 2. Compensates for Loop Gain Variation with Duty Cycle 3. Improves Line Transient Response	1. Difficult to Apply to Multiloop Systems 2. Not Adequate as Regulation Loop by Itself

comparison of the more common fixed frequency control schemes.

A number of control problems may be encountered at high frequencies. AT 20 kHz, the output filter capacitor is usually selected for low ESR, with capacitance a secondary consideration. Usually the filter capacitor is large, compared to the load capacitance. However at 200 kHz, the film capacitors used have an ESR two orders of magnitude smaller, so the filter capacitor will now be much smaller and the load capacity may very well be larger than the filter capacitor. The load capacitance may also be undefined or variable. This can make it very difficult to stabilize the feedback loop. If power modules are to be paralleled, each loop sees the capacity of the other modules, which may also be a variable. When a boost-derived topology is used, there is a right half-plane zero in the control transfer function.

These effects cannot easily be compensated for in the simple DC control loop. Much better performance can be obtained if a combination of AC and DC loops are used. [7,8,9] The use of multiple loop control schemes is highly recommended above 100 kHz.

Some other control loop gremlins which appear at high frequencies are:

1. The circuit stray capacitance is proportionately larger at 200 kHz, so there is an increased likelihood of sub-harmonic instabilities due to capacitive feed-through at the ripple frequency. Careful layout and good bypassing are the best means to combat this problem.
2. In some types of pulse width controller circuits, the time delay in the digital elements (especailly if CMOS is used) may become large enough to cause significant phase shift due to transport delay. As a rough guide, the delay times though the controller should be kept below 5% of the half-period, or about 100 nsec in a 200 kHz converter.

COMPONENTS AT HIGH FREQUENCIES

Operation with switching rates above 100 kHz requires a fresh look at component selection. As in the case of the circuit topology, each of the circuit components must be evaluated for performance, taking into account component parasitic effects which are often ignored at 20 kHz.

Switches

The designer has the choice of using either bipolar or MOSFET devices; some of the tradeoffs are given in Table V. As MOSFETs become less expensive and more diverse in ratings, there is little question that power MOSFETs will be the switch to use above 100 kHz, but at present, bipolars must be considered for some applications with suitable circuit arrangements to compensate for performance limitations.

Fast switching times in bipolars can be achieved by first selecting fast devices and then driving them correctly. The switching time test circuits used by bipolar manufacturers often do not drive the device ON or OFF hard enough, so that the publicized switching times are often not truly indicative of the devices' capabilities. The gain bandwidth, f_t, when given, is a much more reliable indicator of usefulness at high frequencies. Generally, the designer should select devices with an f_t of 10 mHz or more, and then test the devices in the actual circuit. Figure 8 shows an idealized base current drive waveform. At turn-on, a large, fast-rising current pulse is applied. When the device is fully ON, the turn-on pulse is removed and sufficient base drive, in proportion to I_C if possible, is provided to keep the switch in or near saturation. At turn-off, a fast rising negative current pulse is applied to minimize the storage time. A large turn-off pulse will also produce a rapid fall time in low voltage devices and very fast high voltage devices using interdigated structures. It has been shown,[15] however, that for many high voltage transistors, a large turn-off pulse, while reducing the storage time, may extend the turn-off current tail, significantly increasing the switching loss. For devices rated at 400 volts and higher, it may be desirable to use a more gradually decreasing base drive and exchange increased storage time for reduced switching losses. During the OFF time, the base of the transitor should be clamped to the emitter through a low impedance; this will minimize false turn-on due to noise and capacitive coupled currents induced by high dV/dt in other parts of the circuit. These requirements are really not difficult to meet and a wide variety of circuits are possible.[10] Figure 9 shows several possibilities using the DS0026 clock driver as a basis. This IC will source and sink 1A in<20 nsec, and provides an excellent interface between the logic and the switch drive. The IC may be used barefoot, as in (a) and (c) or with power MOSFETs, as in (b). To reduce the storage time, some form of antisaturation circuit can be employed to prevent the collector voltage from going below the base. The Baker Clamp (Figure 10) is perhaps the simplest and most common way to accomplish this. It provides a marked reduction in storage time, but does not really improve the transition times in fast low voltage devices. In a high voltage device, where a good deal of charge is stored in the collecter region during saturated operation, the use of a clamp will reduce the turn-off transition time. It should be kept in mind that there is a limit to the useful turn-off beyond which there is no further improvement. Excessive negative base drive during reversed bias operation causes current crowding in the emitter region, which in turn lowers the threshold at which secondary breakdown will occur. The designer should provide sufficient drive to obtain good performance, but no more.

As the base is driven harder, some devices (especially high voltage transistors) will display a region of quasi-saturation at turn-on, as shown in Figure 11. Low voltage devices, and those using an interdigitated structure display this effect to a lesser extent. Unfortunately, the data sheet is seldom of much help in determining the presence of this problem and the designer may be forced to test a number of different types of devices in his circuit to find out which are suitable and which are not. In a similar manner, quasi-saturation and a current tail can occur at turn-off,[11] and again, the only way at present to detect these effects is by testing. Table VI is a short summary of bipolar performance limits.

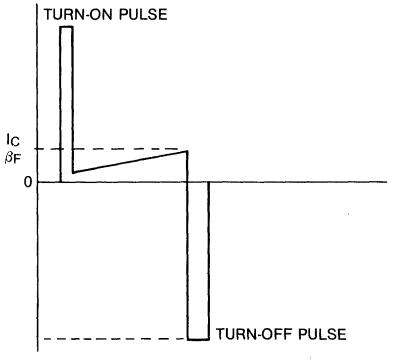


Figure 8. Ideal Bipolar Base Drive

Table V. MOSFET Versus Bipolar Tradeoffs

MOSFET	BIPOLAR
1. FET switches are much faster - 10 to 20 nsec switching times can be readily achieved.	1. Transition times of 50 to 200 nsec at best, with careful base drive design.
2. No storage time effect.	2. Storage times of 500 to 1500 nsec common. This can be reduced to 150 to 300 nssec with antisaturation circuits.
3. Very low drive power required.	3. Base drive requirements relatively high, especially with base overdrive for fast switching.
4. MOSFETs are more expensive at present, but should be much cheaper in the future.	4. At present bipolars, even fast ones, are lower in cost.
5. There is limited selection of MOSFET power devices.	5. A very wide variety of high speed and high power devices are available.

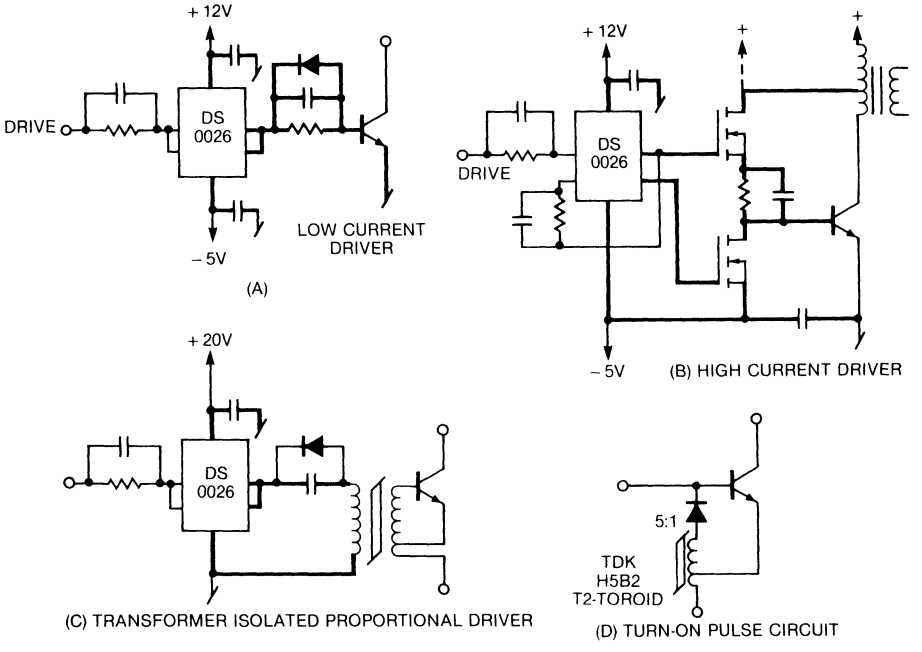


Figure 9. High frequency Base Drive Circuits

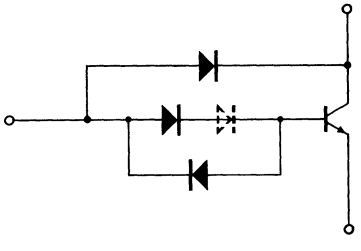


Figure 10. Storage Time Reduction Circuit (Baker Clamp)

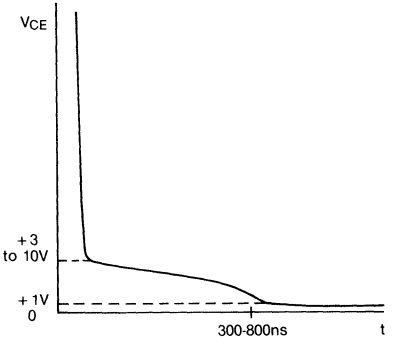


Figure 11. Bipolar Turn-on Plateau

Table VI. Typical Bipolar Performance Limits

PART	V_{CEO}	I_C	t_r	t_f	t_s	f_t
2N5330	140V	20A	50ns	30ns	300ns	20MHz
2N6280	140V	50A	60ns	60ns	400ns / 70ns Clamped	30MHz
2N6590	450V	10A	60ns	100ns	400ns	40MHz
D62T	500V	100A	150ns	150ns	800ns Clamped	10MHz
GSDS 50020	200V	50A	100ns	100ns	400ns	?

The ideal gate current drive waveform for a MOSFET is very similar to a bipolar except that during the switch ON time the current is essentially zero. The gate presents a capacitive load to the driver, where the turn-on is limited primarily by the driver resistance and the circuit parasitic inductance. Several drive circuits are given in Figure 12, and again the MOS clock driver is very effective. The only other limitation on switching speed is due to triggering of the NPN transistor inherent in the MOS structure, and which sees a high turn-off dV/dt (Figure 13). When the drain is pulled rapidly positive, current is injected into the base through C and if sufficient current is injected, the NPN will turn on, usually destroying the device. The dV/dt limitations are a strong function of geometry and vary widely from one device type to another. Until such data is included in the data sheets, the designer will have to contact the manufacturer for information on the limitations. Most devices will display a dV/dt capability of 10V/ns or more, so this is not a serious limitation for switching regulators.

For higher power levels, it is possible to parallel devices, but in the case of bipolars, this may not be very satisfactory. The parallel switches must share current equally, not only during the conduction interval but also while switching. In the case of the bipolar transistors, a large number of parameters (Figure 14) must be matched; this is usually not practical. The MOSFET is very much easier to parallel. Parallel devices should be matched for threshold voltage to ±10% or better. The positive temperature coefficient will then take care of equalizing the ON current. As long as the gate voltages track closely, the devices will share current during turn-on and turn-off. Even with perfectly matched devices, asymmetrical current sharing can be induced if the circuit parasitic capacities, inductances and resistances are not symmetrical. This can cause either dissimilar gate drive waveforms or delay the drain current risetime. The best defense against these problems is to use symmetrical board layouts, such as ring or star connections, and then to verify the current sharing.

For higher voltages, devices may be connected in series. This is a reasonable procedure for MOSFETs if the stray capacitance is kept uniform within the string and the gate drives are identical. At 200 kHz, the dynamic problems of seriesing bipolars are almost insoluble, so that series bipolar switches above 100 kHz are pretty much a dead issue.

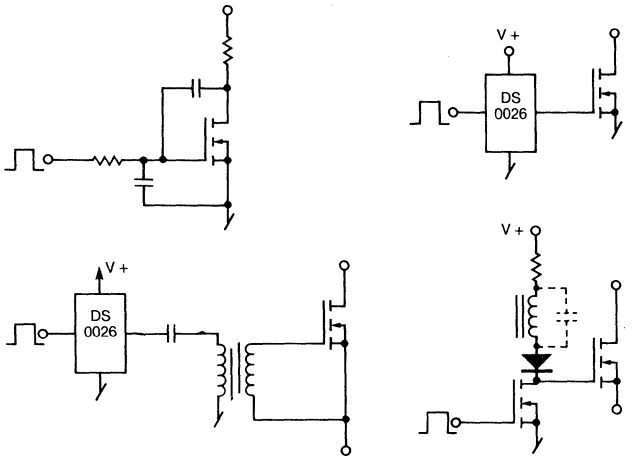


Figure 12. VMOS Drive Circuits

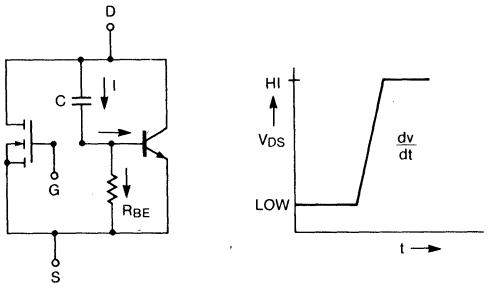
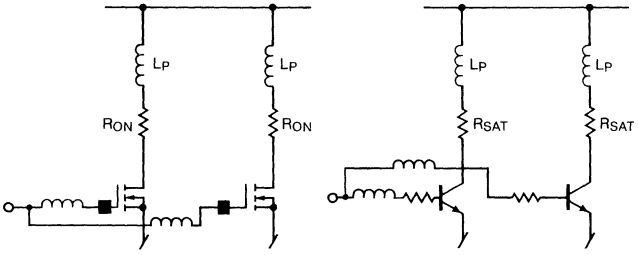


Figure 13. Parasitic NPN Switchback



(A) MATCHING REQUIREMENTS
1. Vgs(th)
2. DRIVE CURRENT

(B) MATCHING REQUIREMENTS
1. STORAGE TIME
2. V_{CESAT}
3. RISE AND FALL TIMES
4. DRIVE CURRENT

Figure 14. Parallel Switch Connections

Junction Diodes

Above 100 kHz, the dominant diode limitation is reverse recovery time, t_{rr}. For efficient rectification the devices selected should have a t_{rr} less than 100 ns, although 200 ns devices can be used if the power loss is acceptable. The need for speed limits the selection to either gold doped devices, such as those manufactured by TRW, Semtech, and Unitrode, or the ion-implanted diodes, produced by SSDI. Table VII is a short summary of present performance limits. Each of the manufacturers has a good variety of devices, so that other than the price penalty, adequate diodes are available. Some manufacturers have indicated that if a large quantity demand were present, most of the cost premium could be eliminated. If the circuit subjects the diodes to a fast rising current waveform, a turn-on voltage spike (Figure 15) across the diode may be observed. This spike has two causes. First the package inductance, and second, the finite time required for the diode to go into full conduction. This is referred to as the forward recovery time, t_{fr}, and is present in most gold-doped devices to some extent. The major effect of t_{fr} is to cause voltage spikes to appear in the circuit, which can stress both the switches and the other rectifiers. As in the case of some bipolar effects, the data sheets are no help and the designer may have to try several devices to obtain one that is suitable.

Diodes can be paralled for high current operation, but in addition to matching the V_F characteristics, careful balancing of the parasitic inductance and resistance is needed. Figure 16 illustrates this point. Again, symmetry of layout is needed, as well as symetrical winding within the transformer. The multiple transformer windings must have equal resistance and be distributed within the transformer, so that equal voltages are induced in each winding.

Table VII. Typical Diode Performance Limits

MANUFACTURER	Type	V_R	I_F	t_{rr}
UNITRODE	UES803	150V	70A	50ns
TRW	SVD450-12	450V	12A	70ns
SEMTECH	3FF500	50V	1A	30ns
TRW	DSR5100	1000V	4A	100ns
SSDI	HSR4S	150V	20A	25ns

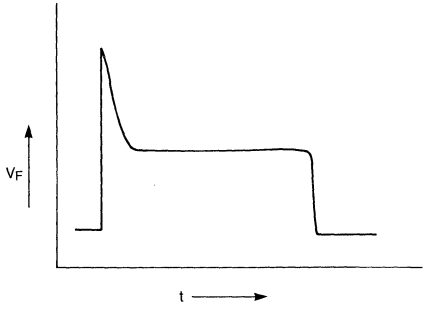


Figure 15. Silicon Junction Diode Forward Recovery Spike

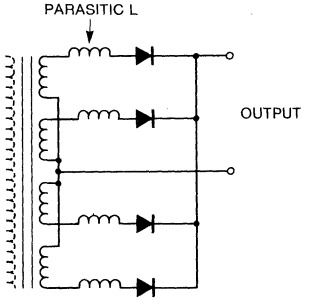


Figure 16. Parallel Diodes

Schottky Barrier Diodes

For low voltages and high currents, the Schottky barrier diode is well suited for high frequency operation. However there are some problems: even though t_{rr} is very short, the large junction capacitance creates circuit effects that are barely distinguishable from t_{rr} problems. There are also dV/dt limitations. Schottky barrier diodes are limited to a dV/dt of 0.7V/ns, and require the use of snubbers to limit the dV/dt. Snubbers are good practice in any case, to limit

voltage transients. The capacitive effects are best accommodated for by using either a resonant or a current-fed topology.

Capacitors

All capacitors have parasitic inductance and resistance. As shown in Figure 17, this forms a series-resonant circuit (usually low Q) so that at frequencies below self-resonance the capacitor is capacitive, and above self-resonance it is inductive. At 20 kHz and electrolytic capacitor is usually used with the size determined by the ESR needed for the ripple current. The result is that the filter capacity is much larger than required to obtain low ESR. The large capacitance makes the self-resonant frequency very low; a typical example is shown in Figure 18. The ESR of an electrolytic capacitor does not vary greatly above 20 kHz, so that its size, for a given ripple current, is essentially independent of frequency. For this reason, either plastic film or ceramic capacitors are used at high frequencies where the ESR of a good film capacitor may be two orders of magnitude less than the best electrolytic, (Figure 19). At 200 kHz the smaller capacity for a given ESR is not a problem, and in fact is an asset in that it raises the self-resonant frequency. As the current capability of the capacitor increases however, the self-resonant frequency goes down, and in high power designs a point is reached where the high frequency impedance is unacceptable. One circuit trick to beat this problem is to parallel small, high self-resonant-frequency capacitors in a low inductance structure. Another scheme parallels two different capacitors as shown in Figure 20. Keep in mind that the effective ESL of the capacitor includes the leads and mounting arrangement, so that a capacitor that stands up from a non-ground plane board may have a much lower resonant frequency than the same capacitor mounted close on a ground plane board with minimum lead lengths and the outer foil grounded to the ground plane. When small values of capacity are needed, ceramic capacitors can be used effectively, however not all ceramic dielectrics have low losses, particularly those with the highest K, so some care must be exercised in selecting ceramic capacitors.

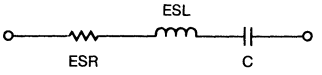


Figure 17. Capacitor AC Equivalent Circuit

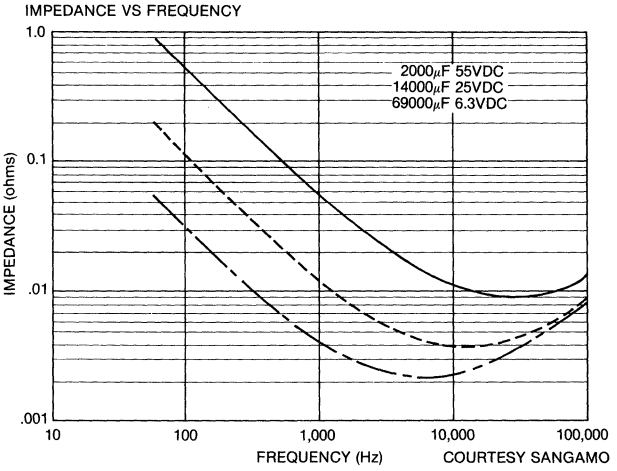


Figure 18. Electrolytic Capacitor Impedance

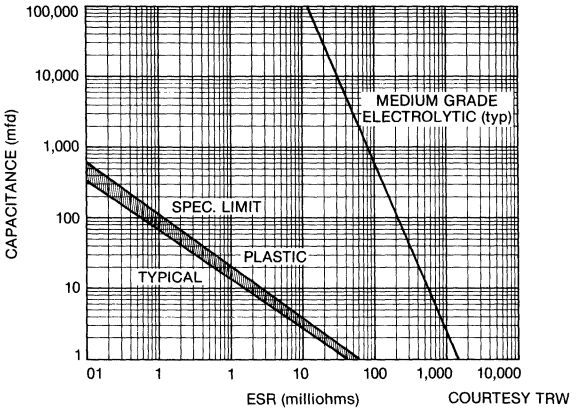


Figure 19. Plastic Film Versus Electrolytic

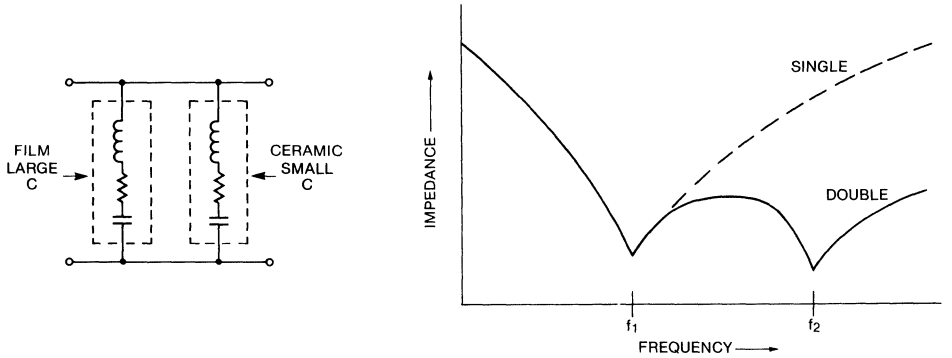


Figure 20. Compound Capactior

High Frequency Magnetics

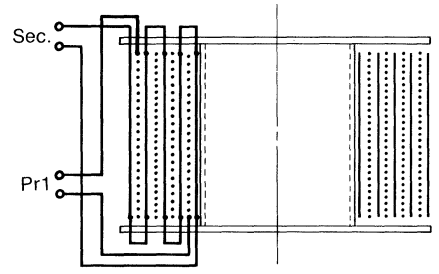
The high frequency power transformer is usually the most difficult component in a high frequency switcher. While a number of satisfactory solutions have been found, this is clearly an area where a great deal more work is necessary.

Most of the common core materials, such as ferrites, powdered iron, tape cores and perhaps amorphous metals can be used at 200 kHz as long as the flux density is restricted for acceptable self-heating. The first choice for a transformer core would be a ferrite such as Ferroxcube 3C8 or Mag-Inc F material. If either the mechanical or temperature environments preclude the use of ferrites, a thin (½ mil) tape core can be used if the flux density is kept low. For chokes, powdered iron toroids are very useful. At 20 kHz, the low μ of powdered iron, as opposed to molypermalloy, makes it relatively unattractive, but at 200 kHz, this is not a problem and the core cost for powdered iron is about 10% of molypermalloy. There appear to be no special advantages to any particular core shape (cup cores, E/I, toroids, etc.) at high frequencies. Because of the reduced number of turns used, however, most cores have too much window for the core area, so that the proportions of all the shapes are not really optimum. An expensive cure is to go to custom cores, but, hopefully, as more designers go to high frequencies, the manufacturers will create new standard sizes for this application.

The high frequency magnetics can be wound with standard magenetic wire, but much better copper utilization can be achieved if Litz, multifilar magnet wire or copper ribbon is used. The reason for this is that the skin effect becomes very pronounced above 100 kHz (and lower at high powers!). Litz and multifilar magnet wire use the principle that the smaller the wire gauge the greater the copper utilization, so that a number of parallel small wires will have a lower AC resistance that the same amount of copper in one wire. Litz wire is essentially multifilar magnet wire that has been braided to further equalize the current distribution. The additional cost of Litz wire is balanced by the very small amounts that are typically used. The only significant problem with Litz wire is stripping the large number of small wires to make connections.

The greatest ingenuity is required in the winding of the transformer to reduce the leakage inductance, and to produce symmetrical and predictable voltages in the output windings. The first step would be to interleave layers of primary and secondary (Figure 21). Better coupling can be had if the primary and secondary are wound multifilar in each layer (Figure 22a). Even better coupling can be had if the primary and secondary are wound of twisted or co-axial transmission lines (Figure 22b). This is the principle of RF transmission line transformers, as shown in Figure 23, 24, 25 and 26. A 1KW 200 kHz version of Figure 25 has been built with a turns ratio of 31:1, the leakage inductance as seen from the 31 turn primary was 1.9 μHy. In a true RF transmission line transformer, the source and load impedances are directly related to the winding characteristic impedance so that tremendous bandwidth is possible. This kind of impedance matching is not very practical for switching regulators, nevertheless, mismatched co-axial transformers are still relatively wide band. Some improvement can be gained by cascading an RF transformer with a conventional transformer (Figure 27) to reduce the turns ratio in the isolation transformer. The RF transformer is usually a very simple and inexpensive structure.

Inductors display parallel self-resonance (Figure 28) due to the winding capacity. The self-resonant frequency must be kept well above the ripple frequency to provide adequate filtering action. A high resonant frequency can be achieved by reducing the winding capacity as much as possible; there are a number of ways to do this: single layer with spaced turns, bank winding, maintaining a large gap between the ends of the winding and minimizing the winding to core capacity by wrapping the core with a low K dielectric. There is a limit, however, to how high the self-resonant frequency can be pushed and it is usually necessary to use a multisection filter such as shown in Figure 29. To avoid complicating the feedback loop compensation, the additional poles should be above gain crossover and well damped. If ferrite beads are used for the high frequency portion of the filter, these requirements are usually met.



Bobbin Winding

Winding Sequence: Cu Ribbon, Mylar Tape, Cu, Mylar, Litzwire, Mylar, Cu, Mylar, Cu

Figure 21. High Frequency Transformers

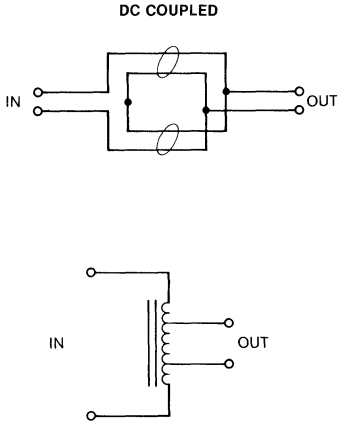


Figure 23. Transmission Line Transformers

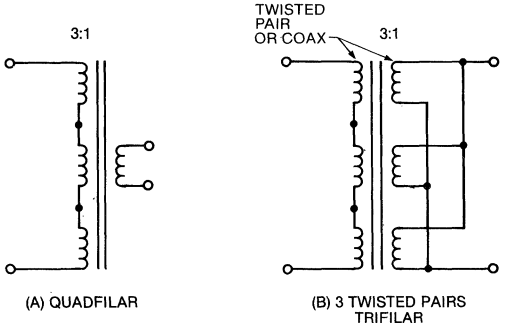


Figure 22. High Frequency Transformer Winding Techniques

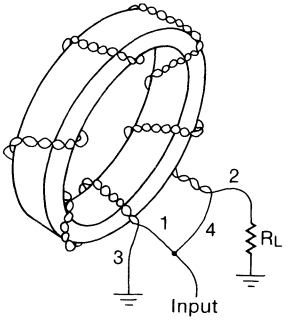


Figure 24. Transmission Line Transformer

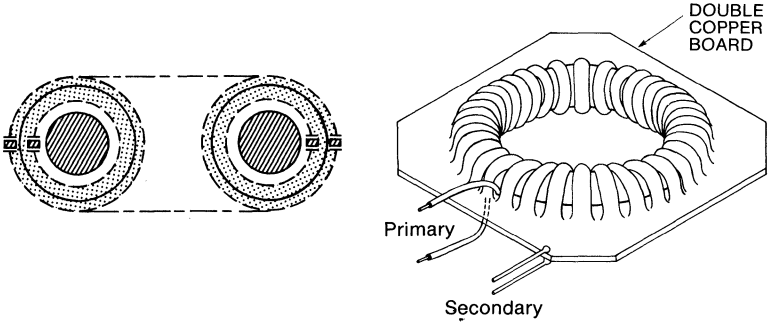


Figure 25. Coaxial Wound Toroid

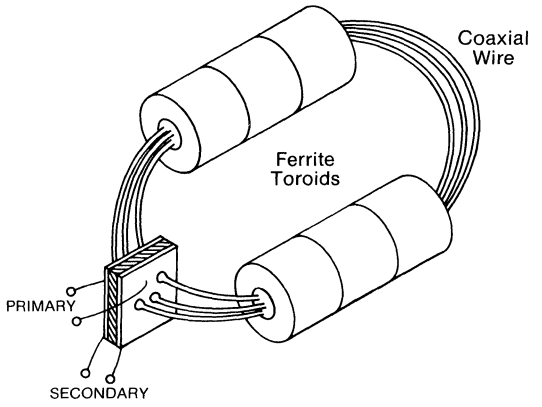


Figure 26. RF Transformer

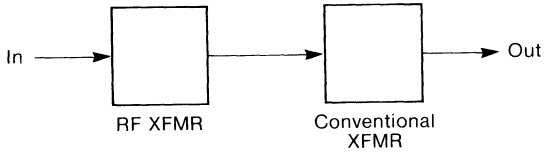


Figure 27. RF Transformer Used to Reduce Turns Ratio in Conventional Transformer

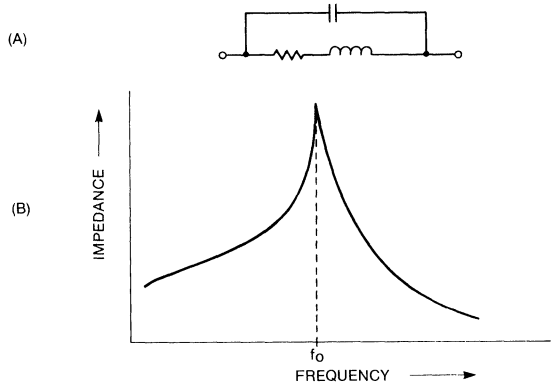


Figure 28. Inductor Self Resonance

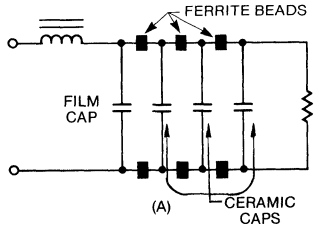


Figure 29. High Frequency Output Filters

Integrated Circuits

A wide variety of Ic op-amps, comparators, pulsewidth modulators and drivers, is available to the 20 kHz switcher designer, but as the frequency is raised to 200 kHz the ranks thin out, especially amoung pulse width modulator IC's.

There are several limitations on the present crop of IC modulators:

1. Limited operating frequency. The majority of IC's have maximum oscillator frequencies of 100 kHz. A few will run at 300 kHz, and one is good up to 500 kHz. Keeping in mind that a push-pull converter will run at one-half the oscillator frequency, this limits the operating frequency to 50 to 150 kHz, except when using the Ferranti IC.
2. Lack of source/sink output drivers. Most IC's do not provide for both source and sink capability at high current levels. This is needed to provide proper drive for power MOSFETs and bipolar transistors.
3. Insufficient drive current. None of the present IC's can supply the ±500 mA current pulses required to switch high voltage power MOSFETs quickly.
4. Slow output transitions. Even in the 500 kHz modulator, the output switch transition can be >100 ns, much too slow for 200 kHz switches.
5. Excessive minimum dead time. The typical minimum dead time is 500 ns. At 200 kHz this is 20% of the half period and is a serious reduction in the available dynamic range.

The most satisfactory of the present IC's are the new Silicon General SG1526 and the Ferranti ZN1066.

The designer may very well have to build his own modulator using logic IC's. An example of a three hundred kHz PWM circuit is shown in Figure 30. U1 is two one-shots connected as an asymmetrical oscillator that produces a train of 100 ns pulses for timing, U2 is the output pulse steering flip-flop, U3 is an open collector gate used to generate the ramp, the comparator is U5, and U6 is the error amplifier. U4 and the remainder of U3 are used for gating and inhibit functions. The 54/74LS series of logic gives adequate speed with reasonable power consumption.

The following limitations exist when using op-amps:

1. Limited bandwidth. Many op-amps, especially the economical quads, have open loop bandwidths of 1 mHz or less. If the amplifier is operated with a gain of 10, then a pole will appear in the transfer function at 100 kHz or less. With gain crossover at 1 or 2 kHz, this is no problem, but if, in a 200 kHz switcher gain crossover is moved up to 20 to 50 kHz, compensation is made more difficult. Also, the common mode noise rejection capabilities of the op-amp are greatly reduced.
2. Subharmonic oscillations. By using op-amps that have high gain at high frequencies, there is an increased tendency towards subharmonic oscillation. This type of oscillation is manifested by alternating pulses of different length, usually at the one-half subharmonic, and is usually caused by capacitive ripple voltage feedback through the feedback amplifier. Because wideband op-amps are needed, this problem is best solved by shielding, capacitor bypassing right at the pins of the op-amp and careful attention to the board trace layouts to minimize capacitive pickup.

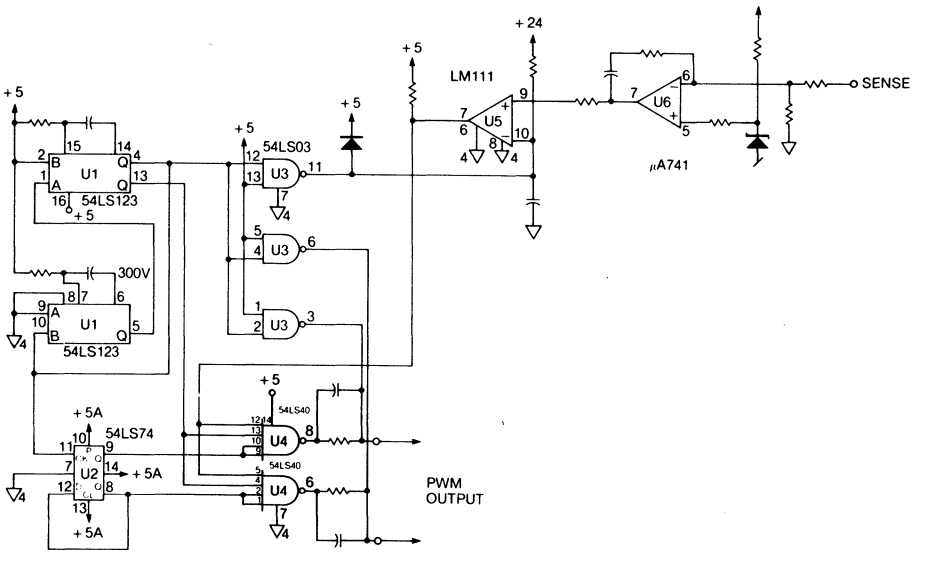


Figure 30. High Frequency PWM Circuit

3. Slew rate limiting. At high frequencies the designer must pay attention to the power bandwidth or slew rate of the op-amp, and be certain that the op-amp has the capability to drive the compensation capacitors and whatever other load is on the output of the op-amp.

Since comparator transitions of less than 100 ns are needed, most comparator IC's are eliminated; the LM111A is about as slow a comparator as is useful. Remember that the comparator switching speed is affected by the dV/dt of the input ramp, and the maximum practical ramp amplitude should be used to maximize dV/dt.

CIRCUIT LAYOUT

Having selected the circuit topology and the components, the designer is faced with putting it all together in a workable layout. At 20 kHz much latitude is permitted, and even the worst rats nest will work. This is *not* the case at 200 kHz. A 200 kHz switcher has frequency components beyond 100 mHz and has much more in common with a wideband RF amplifier than a 20 kHz switcher. A careless layout may very well not work at all. The key is "THINK RF" during the layout. A collection of useful layout tips are given in Table VIII. Figure 31 gives a good idea of how much inductance is introduced by the interconnection leads, and how this inductance can be reduced by either twisting the connecting wires or using the pc board traces as transmission lines. Another useful approach, shown in Figure 32, uses a small ceramic capacitor to reduce the area of a high dI/dt loop. This is simply an example of RF bypassing.

The final layout will probably look quite different from the 20 kHz norm but there is no reason that it need be exotic or any more expensive. In fact, due to the additional care used, it may very well be less expensive.

Table VIII. Circuit Layout Tips

1. Identify the Hi dI/dt Paths and Minimize their impedance
2. Minimize the Area of Current Loops
3. Use Twisted Leads for Transformer Connections
4. Arrange Transformer Lead Breakouts to Minimize Inter Connection Inductance
5. Bypass Hi dI/dt Loops with Ceramic Capacitors
6. Use Star or Ring Connections for Parallel Components
7. Use Goundplane Construction
8. Beware of Inductive Device Cases

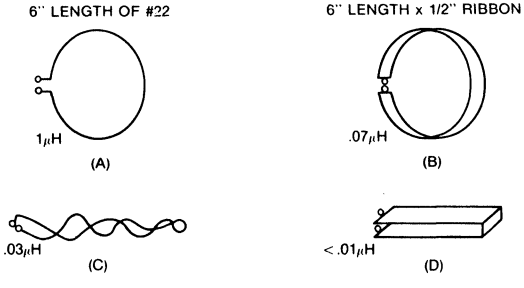


Figure 31. Inductance of Wire Loops

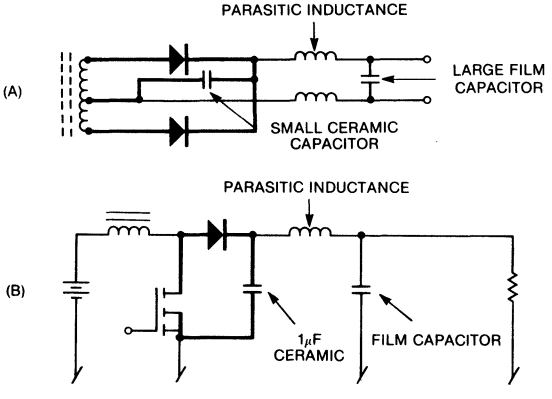


Figure 32. HF Bypassing

CONCLUSION

Having gone through this exercise of selecting new topologies, components and layouts, one wonders if it's really worthwhile. Is the volume and weight reduced, is there any cost reduction, and can we do better in the immediate future?

Some of the pro and con arguments for these questions are summarized in Tables IX, X, and XI. The amount of volume reduction realized is very much a function of power output. From zero to 20 watts little is gained by going to high frequencies; from 20 to 100 watts the volume may be reduced by a factor of 1.5, and above 100 watts a factor of 3 or more may be obtainable. The actual size reduction achieved depends strongly on the power supply specifications. If, for example, a line voltage dropout of 50 or 100 ms must be accommodated, the size of the DC energy storage capacitors is so great that the operating frequency of the converter is relatively unimportant. On the other hand, in those applications where the line dropout requirement is very small and conduction cooling is provided, the size reduction can be dramatic.

The answer to the cost question is a definite maybe. There really have not been enough commercial switchers designed at these frequencies to know the relative value to the arguments in Table X, but if the cost of the MOSFETs and fast diodes can be reduced, the high frequency converters should be cheaper to build.

A final note of caution: Most designers find that their first effort at 200 kHz usually isn't much smaller than what they could built at 20 kHz! Don't be discouraged. It takes time to appreciate the differences and to exploit the possibilities of high frequencies. Usually by the second or third effort the performance advantages talked about here will begin to appear.

Table IX. Size/Volume Reduction Tradeoffs

PRO	CON
1. Transformers Smaller 2. RFI Filters Much Smaller 3. Capacitors Smaller	1. Heat Sinks No Smaller 2. Semiconductor Packages No Smaller 3. Auxillary Circuits No Smaller 4. Line Holdup Capacitors Only Slightly Smaller

Table X. Cost Tradeoffs

PRO	CON
1. Magnetics Cheaper 2. EMI Filters Cheaper 3. Filter Capacitors Cheaper 4. Power MOSFETs will be Competitive in Cost with Low Frequency Bipolar	1. Junction Diodes More Expensive 2. HF Bipolar Switches More Expensive 3. Shielding for RFI Required

Table XI. Expected Future Improvements

1. High Current, Low Voltage Film Capacitors
2. Lower Cost Low t_{rr} Diodes
3. More Practical Transformer Designs
4. A Good 300 KHz Modulator IC
5. Wide Variety of Low Cost Power MOSFETs

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INTERSIL

AO35 Switchmode Converter Topologies — Make Them Work for You!

by Rudy Severns

INTRODUCTION

Recent years have seen a tremendous expansion in the sales volume and variety of applications for switching regulators. Surprisingly, if one looks at the circuit arrangements most frequently used, only a few different types are represented. The parallel, half-bridge and full bridge quasi-squarewave circuits and the single ended flyback and feedforward converters represent about 95% of what is available in the marketplace today. A bit of research quickly reveals that there are many other circuit topologies, both switchmode (modified squarewaves) and resonant, that are available and which may be superior to the popular circuits in particular applications.

This application note is intended to provide the switching power supply designer with a broad view of the switchmode converter topology options available and to demonstrate synthesis techniques that should enable the designer to invent new topologies which may better suit his particular design problem.

Why We Need New Topologies

There are several reasons for considering new or non-standard circuits:

a. Increasingly, switchers are operating at higher switching frequencies to reduce size and weight. It is now completely practical to operate above 200KHz, and while the more popular circuits will work at these frequencies, they are by no means optimum. It has been shown[1] that some not so common topologies have very definite advantages at high frequencies.

b. Power MOSFETs are rapidly becoming a reality for switchmode converters. The distribution between switching and conduction losses in a MOSFET is quite different from those of a bipolar, and the choice of circuit topology can have a profound effect on the total power loss. Many of the standard circuits are less than optimum when used with MOSFET switches.

c. The switching power supply designer is limited by the capabilities of the components available to him. Because of the efforts of component manufacturers, the performance limits change continuously, but progress is slow and the designer will always be faced with component limitations. Because the electrical stresses on the individual components vary widely with the topology, the choice of topology can be used as a tool to get around some of the limitations in components, and the larger the number of circuit variations available to the designer, the greater the likelihood that an acceptable solution will be found.

d. As switchers find a wider range of usage, more and more special applications that require optimization of a variety of different performance parameters appear. To cope with these applications, the designer needs a wide variety of circuits to choose from so that really effective designs can be created.

e. The power supply industry is becoming increasingly competitive. Manufacturers using a poorly optimized "one circuit for all applications" approach are going to be pushed out of the marketplace by more aggressive and versatile competitors.

f. Requirements on the control of EMI are becoming much more restrictive; the choice of topology can be used to minimize EMI.

g. It occasionally happens that an individual or organization will create a circuit variation that gives a real or imagined competitive advantage for a particular application. The normal course is to immediately patent the circuit to deny its use to a competitor. While the competitor cannot use the original circuit, he may very well be able to apply the manipulative techniques shown herein to the circuit to produce a different and perhaps even better circuit. Conversely, the circuit originator could better protect himself by manipulating his circuit and extending the patent to all possible variations.

Where Do Circuit Topologies Come From?

There are many sources of switchmode converter topologies. The first and most obvious place to look is standard industry practice. The next source is the published literature in the field; an extensive bibliography is included at the end of this application note. A third rich source is the patent and patent disclosure files. A search of the patent files can be tedious, but every so often a really useful circuit or circuit variation will be found.

The next step is to employ synthesis techniques to generate circuits that do not presently exist. A variety of synthesis procedures exists, and the discussion of these procedures is the main thrust of this application note.

By far, the most important source for new circuits is the designer's intuition. The synthesis procedures described herein have not evolved to the point that the designer can define the desired circuit performance and then follow a specified synthesis procedure that will lead directly to the desired solution; and while very useful, the present range of synthesis techniques are still rather clumsy tools that the designer must guide, using his intuition to reach the desired goal.

CRITERIA FOR COMPARING CONVERTER TOPOLOGIES

As will be demonstrated shortly, the literature, patent search and synthesis efforts produce a large and bewildering array of circuit topologies. The number of circuits is so large that there is no way to deal with all of them on a one-at-a-time basis. What is needed is some orderly means to compare circuits quickly, to enable the designer to choose the best circuit for his application. There are several possibilities for simplifying the comparison process:

1. The circuits can be organized into families sharing common characteristics.
2. The figures of merit for different topologies can be compared. The stress on the various circuit components varies widely from one topology to another. For each topology and component, a normalized component stress figure of merit can be developed that relates the individual component stress to the input and output voltages and currents.
3. Figures of merit relating the amount of inductive and capacitive energy storage required for a given power level can be derived. These figures of merit are very useful for weight and volume trade-off studies.
4. The feedback loop and transient characteristics are an important practical consideration for comparing topologies. The presence of a right half-plane zero in the boost family of converters is an example of a potential stabilization problem.
5. The component count can be a very important figure of merit, especially for powers below 100W. In converters operating below 100W, the component stress is not usually high enough that multiple components or especially high performance components are needed and the primary objective is usually low cost. As the power level goes above 100W however, it becomes increasingly desirable to use topologies that reduce component stress levels even if the component count is higher. The point is that the component count is a very useful figure of merit, but it can be misleading as the power level is increased.
6. The response of the circuit to component nonidealities is a useful point of comparison. For example, the switch conduction overlap caused by transistor storage time can be either harmless or catastrophic, depending on the topology.

Converter Topologies Organized Into Families

It appears that all of the known switching regulators can be synthesized from combinations of three circuit elements: The boost regulator, the buck regulator and some form of DC transformer, as shown in Figure 1. Examples to support this contention will be given in following sections. This observation suggests a family delineation that derives from the basic elements from which a particular converter can be assembled. Figure 2 is a converter family tree that begins with the buck and boost converters as the most basic elements. As will be shown shortly, the buck and boost converters are electrical duals of each other. The DC transformer is not treated as a starting element but is used as a circuit element to produce permutations of the basic buck and boost regulators.

The buck derived family shares the common characteristics of discontinuous input current, continuous output current, duty cycle, $D = V_b/V_i$, non-moving poles in the transfer function and an internal bus voltage V_b lower than V_i. The boost derived family shares the common characteristics of continuous input current, discontinuous output current, a right half-plane zero and moving left half-plane poles in the transfer function, and an internal bus voltage higher than the input voltage. The family of converters made up of combinations of buck and boost converters is not so neatly characterized, because of the diversity of its members, but there are localized generalizations that can be made. Wherever possible, the common name for the particular converter is given. Since many of the entries in Figure 2 are not generally known, or do not have specific names, each entry is referred to the figure number in the following sections where the circuit is first developed.

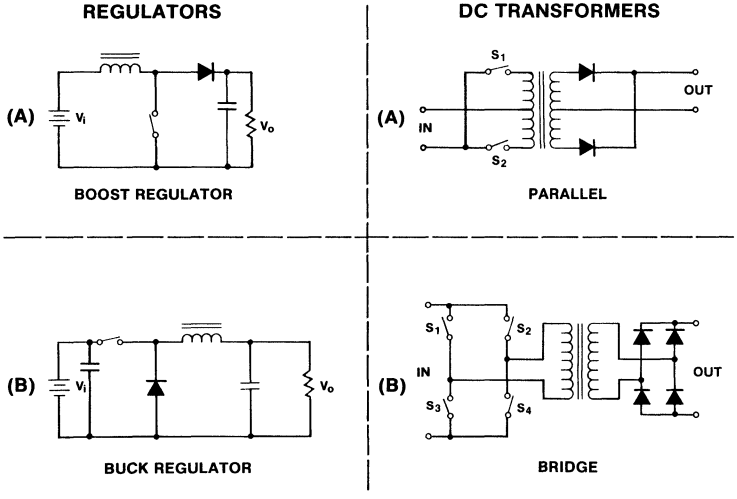


Figure 1

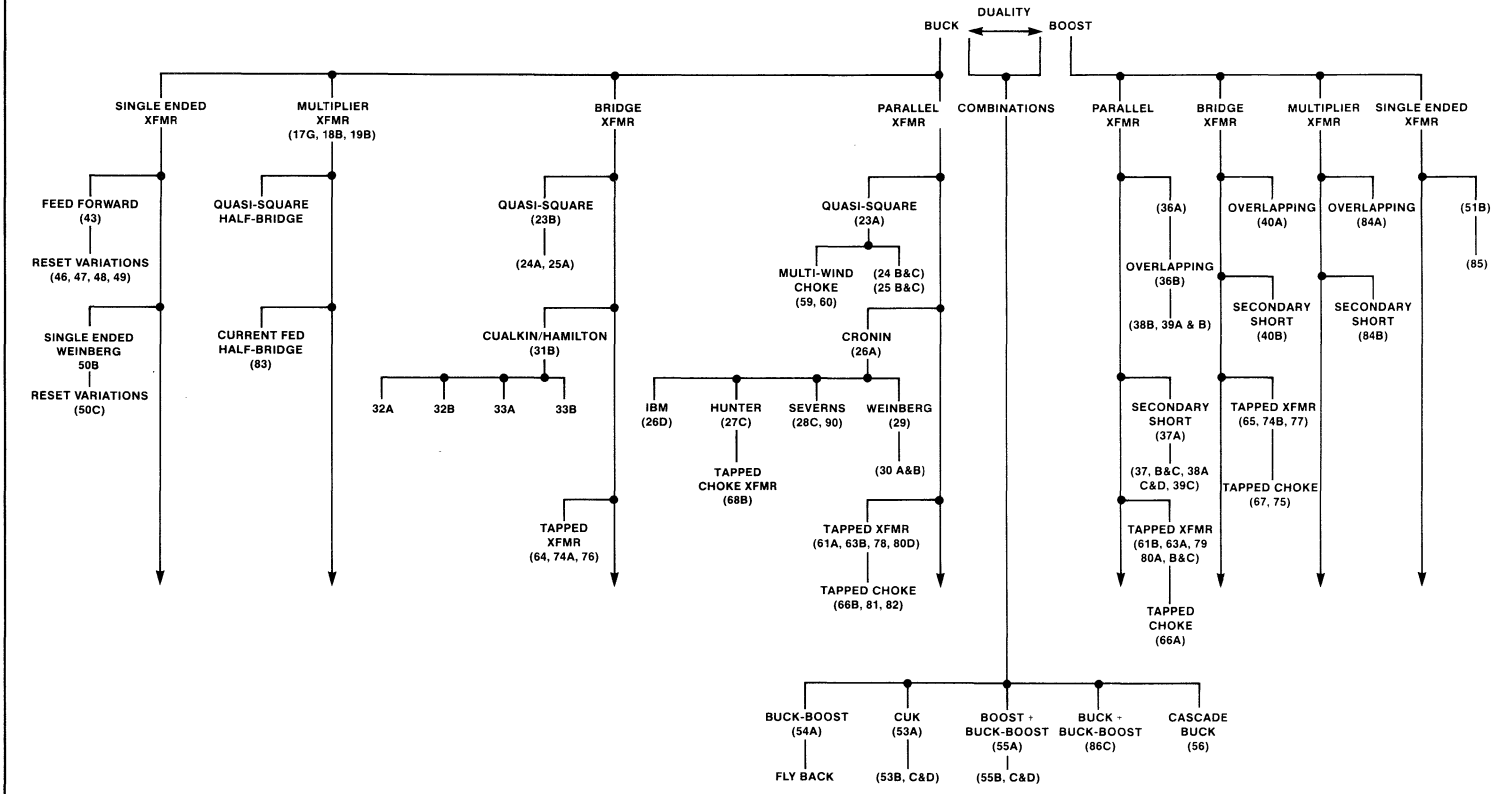

DUALITY
BUCK
BOOST
SINGLE ENDED XFMR
MULTIPLIER XFMR (17G, 18B, 19B)
BRIDGE XFMR
PARALLEL XFMR
COMBINATIONS
PARALLEL XFMR
BRIDGE XFMR
MULTIPLIER XFMR
SINGLE ENDED XFMR
FEED FORWARD (43)
RESET VARIATIONS (46, 47, 48, 49)
SINGLE ENDED WEINBERG 50B
RESET VARIATIONS (50C)
QUASI-SQUARE HALF-BRIDGE
CURRENT FED HALF-BRIDGE (83)
QUASI-SQUARE (23B)
(24A, 25A)
CUALKIN/HAMILTON (31B)
32A
32B
33A
33B
TAPPED XFMR (64, 74A, 76)
QUASI-SQUARE (23A)
MULTI-WIND CHOKE (59, 60)
(24 B&C) (25 B&C)
CRONIN (26A)
IBM (26D)
HUNTER (27C)
SEVERNS (28C, 90)
WEINBERG (29)
TAPPED CHOKE XFMR (68B)
(30 A&B)
TAPPED XFMR (61A, 63B, 78, 80D)
TAPPED CHOKE (66B, 81, 82)
(36A)
OVERLAPPING (36B)
(38B, 39A & B)
SECONDARY SHORT (37A)
(37, B&C, 38A C&D, 39C)
TAPPED XFMR (61B, 63A, 79 80A, B&C)
TAPPED CHOKE (66A)
OVERLAPPING (40A)
SECONDARY SHORT (40B)
TAPPED XFMR (65, 74B, 77)
TAPPED CHOKE (67, 75)
OVERLAPPING (84A)
SECONDARY SHORT (84B)
(51B)
(85)
BUCK-BOOST (54A)
FLY BACK
CUK (53A)
(53B, C&D)
BOOST + BUCK-BOOST (55A)
(55B, C&D)
BUCK + BUCK-BOOST (86C)
CASCADE BUCK (56)

Figure 2

Component Stress Figures of Merit

A very powerful tool for comparing topologies in a given application is to look at the component stresses for given input and output voltages and currents. A wide variety of figures of merit can be created. Some of the more useful ones are:

1. Input capacitor, I_{rms}/I_i
2. Transformer or choke primary windings, I_{rms}/I_i
3. Switches, I_{avg}/I_i, I_{rms}/I_i, V_{pk}/V_i, P_{pk}/P_i
4. Primary catch diodes, I_{avg}/I_i, V_r/V_i
5. Transformer or choke secondary windings, I_{rms}/I_o
6. Secondary rectifiers, I_{avg}/I_o, V_r/V_o, I_{pk}/I_o

The symbols are defined in Table I.

TABLE I

SYMBOL	DEFINITION
I_{rms}/I_i	Ratio of component rms current to DC input current
I_{avg}/I_i	Ratio of component average current to DC input current
V_{pk}/V_i	Ratio of peak component voltage to DC input voltage
P_{pk}/P_i	Ratio of peak component power to input power
V_r/V_i	Ratio of diode reverse voltage to DC input voltage
I_{rms}/I_o	Ratio of component rms current to DC output current
V_r/V_o	Ratio of diode reverse voltage to DC output voltage

The reader can no doubt supply many other possible merit figures to suit individual needs. It should be kept in mind that each of these figures of merit will be a function of the duty cycle ($\propto V_b/V_i$), and in some cases the shape factor of the current waveform.

The variation of the average and rms values of the waveforms is an important consideration and is treated at some length in Appendix I.

Design Example

Let us now compare two common circuits, the buck and boost regulators, using some of the figures of merit and qualitative considerations previously suggested. The regulators will be compared for an applicaton with a two to one line variation.

Assumptions

1. V_o = 18V for the buck regulator
2. V_o = 42V for the boost regulator
3. V_i = 20 to 40V
4. For simplicity $L >> L_c$; i.e., rectangular current pulses
5. Circuits correspond to Figures 1A and 1B

Given these assumptions, the equations for the component stress figures of merit can be derived and the values calculated. This is summarized in Table II. The following observations can be made from Table II.

1. If the input capacitor of the buck is compared to the output capacitor of the boost, the boost has a much lower ripple current.

TABLE II. Buck/Boost Regulator Comparison

COMPONENT	FIGURE OF MERIT		VALUE AT LOW LINE		VALUE AT HIGH LINE	
	BUCK	BOOST	BUCK	BOOST	BUCK	BOOST
C1	$\frac{I_{rms}}{I_i}=\sqrt{\frac{V_i}{V_o}-1}$	$\frac{I_{rms}}{I_i}\cong 0$	0.33	0	1.11	0
S1	$\frac{I_{rms}}{I_i}=\sqrt{\frac{V_i}{V_o}}$	$\frac{I_{rms}}{I_i}=\sqrt{1-\frac{V_i}{V_o}}$	1.05	0.72	1.49	0.22
	$\frac{I_{avg}}{I_i}=\frac{V_o}{V_i}$	$\frac{I_{avg}}{I_p}=1-\frac{V_i}{V_o}$	0.9	0.52	0.45	0.05
	$\frac{V_{pk}}{V_i}=1$	$\frac{V_{pk}}{V_i}=\frac{V_o}{V_i}$	1	2.1	1	1.05
	$\frac{P_{pk}}{P_i}=\frac{V_i}{V_o}$	$\frac{P_{pk}}{P_i}=\frac{V_o}{V_i}$	1.11	2.1	2.22	1.05
D1	$\frac{I_{avg}}{I_i}=\frac{V_i}{V_o}-1$	$\frac{I_{avg}}{I_i}=\frac{V_i}{V_o}$	0.11	1.11	1.22	0.95
	$\frac{V_r}{V_i}=1$	$\frac{V_r}{V_i}=\frac{V_o}{V_i}$	1	2.1	1	1.05
L1	$\frac{I_{rms}}{I_i}=\frac{V_i}{V_o}$	$\frac{I_{rms}}{I_i}=1$	1.11	1	2.22	1
C2	$\frac{I_{rms}}{I_i}\cong 0$	$\frac{I_{rms}}{I_i}=\frac{V_i}{V_o}\sqrt{1-\frac{V_i}{V_o}}$	0	0.34	0	0.21
Duty Cycle	$D=\frac{V_o}{V_i}$	$D=1-\frac{V_i}{V_o}$	0.9	0.52	0.45	0.05

2. The switch rms and average currents are much higher in the buck than in the boost. The peak voltages and powers are nearly equal.
3. The diode average current is significantly lower in the boost.
4. The choke rms current is somewhat higher in the buck.
5. The duty cycle excursion is much larger in the boost.

These comparisons can be shown to be valid between complementary members of the buck and boost families. Surveying these comparisons, one would find the boost converter family to be generally more efficient and have lower component stresses than the buck family.

If, however, one now looks at considerations other than component stress, the boost family is not quite so attractive. The feedback loop transfer function contains a zero in the right half-plane, and the poles in the left half-plane vary with the duty cycle. This makes the boost regulator much more difficult to stabilize, and, if simple control loops are used, can mean degraded transient response. The duty cycle variation in the boost regulator is much larger, and this can be a problem if wide load current and line voltage excursions are specified. In the boost regulator, there will be a current surge when the line voltage is applied, and the output voltage in the beginning is controlled by the source impedance rather than the switch. All members of the boost family display similar behavior even when transformer coupled. The difference for the transformer coupled variations is that the surge current occurs at the onset of the switching action rather than at the application of line power.

SYNTHESIS USING DUALITY

Dr. Slobodan Ćuk[2] has demonstrated the application of the duality principle to switchmode converter topologies. At first glance this work may appear to be an interesting but purely academic exercise. This is not the case. Not only does duality give insight into relationships between topologies, but it is also a very practical tool for synthesizing new circuits.

Review of Dual Graphs and Networks*

"The following is a concise summary of the properties of dual graphs and networks, which is sufficient for understanding the subsequent derivations in the following sections. More detailed expositions of duality theory as applied to graphs and electric networks can be found in many standard textbooks.[3,4]

"Duality theory is generally limited to the special class of graphs called *planar* graphs. A graph G_p is said to be a planar graph if it can be drawn on a plane in such a way that no two branches intersect at a point which is not a node. For example, graph G_p in Figure 3A is a planar graph, whereas graph G_n in Figure 3B is not.

"In a planar graph, *meshes* and *outer meshes* are distinguished. Any closed loop of the planar graph for which there is no branch in its interior is a *mesh*. For example, loops bf, bf, and bf are meshes in the planar graph, G_p, of Figure 3A. Analogously, a loop which contains no branches in its *exterior* is called an *outer mesh*, like loop bf in the planar graph G_p of Figure 3A. In this review the star notation (*) is used to

*This section is a direct excerpt from the paper[(2)] published by Dr. Ćuk.

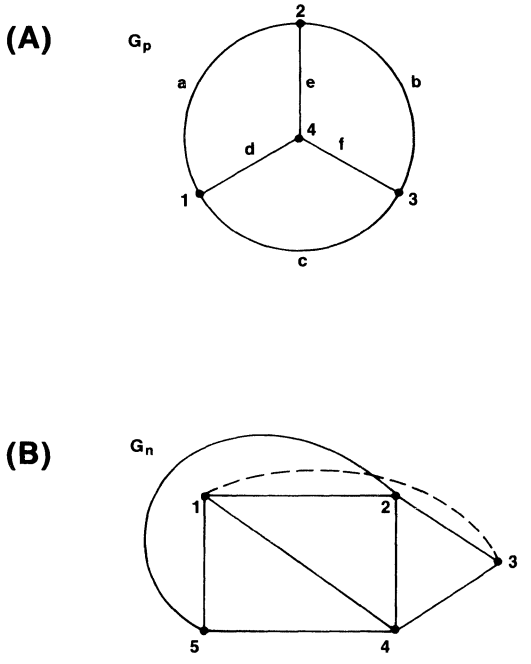


Figure 3: Examples of planar (A) and nonplanar (B) graphs

designate the dual graphs, networks and dual components to facilitate easier recognition of duality relationships. However, in the remaining sections it will be left out, since the recognition of dual components will by then be mastered.

"Two planar graphs, G and G*, are *dual graphs* if:

a) there is a one-to-one correspondence between the meshes of G (including the outer mesh) and the nodes of G*, and vice versa, and
b) there is a one-to-one correspondence between the branches of each graph, such that whenever two meshes of one graph have a branch in common, the corresponding nodes of the other graph have the corresponding branch connecting these nodes.

"For example, the graphs G and G* of Figure 4A are dual graphs, since the above correspondence can be easily established.

"For two electrical networks, N and N*, to become dual, some additional properties are required. In addition to the graph concepts (meshes corresponding to nodes), the relationships between the dual networks also involve the *dual nature of the elements*, that is, their electrical properties (capacitors corresponding to inductors, voltage sources corresponding to current sources, etc.). Therefore, networks N and N* are dual networks if:

a) they have dual topological graphs G and G*, and

b) the branch equation of a branch of N* is obtained from its corresponding equation of N by performing the following substitutions;

$$v \rightarrow j^*,\ j \rightarrow v^*,\ q \rightarrow \phi^* \text{ and } \phi \rightarrow q^* \qquad (1)$$

where v, j, q and ϕ are branch voltage, current, charge and flux variations respectively.

"Thus, to a resistance of R ohms in N there corresponds a conductance of G mhos (1/Ω) in N*, since v = Rj branch relation is transformed into $j^* = G^* v^*$, where $G^* = 1/R$. Therefore, a resistance of R ohms in the original network becomes resistance of 1/R ohms in the dual network. Similarly, the inductor of L (μH) becomes a capacitor of C* (μF) and vice versa as seen from the example in Figure 4B. Also, the current source of Ig (Amperes) corresponds to a voltage source of Vg (volts) in the dual network. In summary, the following dual substitutions are in order:

$$L \rightarrow C^*,\ C \rightarrow L^*,\ R \rightarrow G^*\ (G^* = \frac{1}{R}),\ Ig \rightarrow Vg^* \qquad (2)$$

"Let us now see how for a given planar graph or planar network the dual can be constructed.

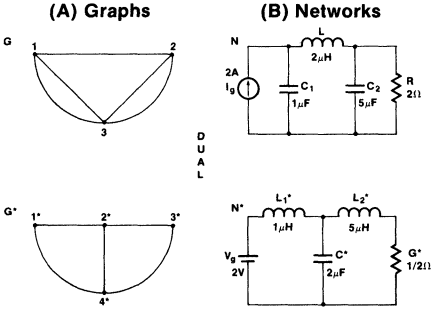


Figure 4: Example of Dual Networks (B) and Their Corresponding Graphs (A)

Algorithm for Dual Graph and Dual Network Construction

The dual graph G* of a planar graph G can be obtained if:

a) to each mesh of graph G, we associate a corresponding node of G*, by placing it inside the mesh. Finally, an additional node is placed outside of graph G (in its exterior) which corresponds to the outer mesh of graph G;

b) for each branch, say b, of G which is common to mesh i and j, we associate a branch b* of G* which is connecting the nodes of G* corresponding to meshes i and j of G.

"This construction is transparent from Figure 5A which is also an example of *oriented graphs.* Given the orientations of the original graph G branches, the orientation of corresponding dual branches is obtained by *counterclockwise* rotation of the original branches until they coincide with their dual branch directions, as also illustrated in Figure 5A.

"The dual oriented network construction involves . . . the (one) additional step of dual substitutions (1) and (2) in the corresponding dual branches . . . Figure 5B.

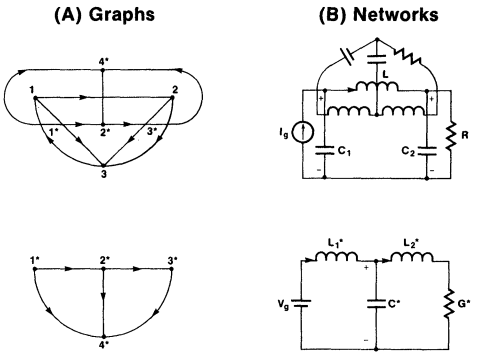


Figure 5: Algorithm for Dual Graph and Dual Network Construction

"The . . . construction of a dual network following this algorithm would have remained just an interesting and elegant topological correlation, had it not been intimately tied with a truly remarkable general law of nature — *the duality principle.*

Duality Principle

"Since many of the results obtained in later sections will be based on (it), the *duality principle,* . . . requires a very careful definition.[3] The remarkable duality principle can be stated as:

> *Consider an arbitrary planar network N and its dual network N*. Let S be any true statement concerning the behaviour of N. Let S* be the statement obtained from S by replacing every graph, theoretic word or phrase (node, mesh, loop, etc.) by its dual and every electrical quantity (voltage, current, impedance, etc.) by its dual. Then S* is a true statement concerning the behaviour of N*.*

"In its abbreviated form, limited to the relationship of its electrical parameters which will be very often used later, it can be stated in the form of the equivalence relationship:

$$S\ (j,v,q,\phi,L,C,Z) \rightleftharpoons (v^*,j^*,v^*,q^*,C^*,L^*,Y^*) \qquad (3)$$

"Duality in Switching DC-to-DC Converters*"

"In order fully (sic) to develop the duality relationships, the notion of a switching DC-to-DC *current* converter needs to be introduced first and its meaning clarified. In other words, a constant *current* input source is postulated in addition to the usual constant voltage source.

Switching DC-to-DC Voltage and Current Converters

"Consider . . . the comparison of the conventional buck converter, with either constant voltage source, as in Figure 6A, or constant current source, as in Figure 6B. In either case, the inductance L is, for simplicity, large enough to result in practically DC current, I, at the output, with negligible switching ripple. Although the practical realization of the switching current converter is of no concern here, it may suffice to say that the constant current source I_g may be voltage limited to prevent excessive rise of the voltage on the input capacitance C (for S at position B only). It is also assumed that ideal

switch S is in position A for interval DT_s and in position B for interval $D'T_s = (1-D)\,T_s$, where D is the switch duty ratio and T_s the switching period.

"We now concentrate on the principal features of the two converters in Figure 6. For the voltage converter in Figure 6A, we easily obtain in the ideal case:

$$\frac{V}{Vg} = D \tag{4}$$

$$\frac{I}{I_g} = \frac{1}{D} \Rightarrow I_g = \left(\frac{D^2}{R}\right)V_g \tag{5}$$

"Thus from (4), the voltage gain is only dependent on duty ratio D, but is *independent* of load R. However, the DC current I_g drawn from the source is dependent on load R as seen in (5). Therefore, the converter of Figure 6A can be conveniently designated as a switching DC-to-DC *voltage* converter. On the other hand, for the converter in Figure 6B:

$$\frac{I}{I_g} = \frac{1}{D} \tag{6}$$

$$\frac{V}{V_g} = D \Rightarrow V_g = \left(\frac{R}{D^2}\right) I_g \tag{7}$$

"Here the current gain is independent of load R, as in (6), while both input and output voltage fluctuate to accommodate the change of load R. Thus, this converter can be conveniently designated as a switching DC-to-DC *current* converter. Hence the basic buck power stage operates as either a switching *voltage* or a *current* converter, depending on the type of DC source applied.

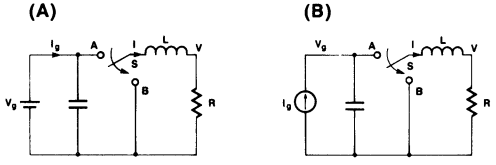


Figure 6: Comparison of a Switching Voltage (A) and a Switching Curent Converter (B)

Duality Among the Four Basic Switching Converter Types*

"Although it has not been demonstrated previously how a dual network of a planar network *which contains switches* can be found, it is relatively simple to resolve this problem. Consider, for example, a switching buck-type current converter more closely, . . . for convenience again redrawn in Figure 7A. For the two positions of switch S (for intervals DT_s and $D'T_s$ respectively), the two switched networks of Figure 7B are obtained. Each of the two switched networks of Figure 7B is a *planar* network, consisting of L, C, R and I_g. Thus, a dual network for each of the two linear switched networks of Figure 7B can easily be found following the algorithmic procedure outlined in the previous section . . . By taking into account the orientation of the branches in Figure 7B, the *dual oriented networks* (of Figure 7C) are obtained. (These two) networks . . . can now be easily redrawn to form a single switching network in Figure 7D for the two positions of its single-pole double-throw switch S.

"An important conclusion can now be made from Figure 7. *The familiar boost voltage converter is just a dual network to the buck current converter.*

"It should be also noted that in the two dual networks, the positions A are the corresponding homologous switch positions. Note also, that for the buck current converter only a minimal configuration was chosen, and the usual output capacitance left out as not essential . . . However, the inductor L **is** essential and leads in the dual network to capacitor C, which is likewise essential for boost voltage converter operation; (see) Figure 7D.

"By (using) the powerful duality principle (3), we can directly obtain the DC voltage gain of the boost converter from the DC current gain (6) of its dual buck converter as:

$$\frac{I}{I_g}\left(\frac{I}{I_g} \Rightarrow \frac{V}{V_g}\right) = \frac{V}{V_g} = \frac{1}{D} \tag{8}$$

(assuming) the duty ratio of switch S in Figure 7D is referred to the corresponding position A. However, owing to practical realization of that switch by a bipolar transistor and diode, it is usually referred to position B (on time of the transistor). Thus with the duty ratio defined with respect to B in Figure 7D, we get:

$$\frac{V}{V_g}\Big|_{D \to D'} = \frac{1}{D'} = \frac{1}{1-D} \tag{9}$$

which is the familiar DC gain of the boost converter. This is (the) first example which illustrates the powerful duality principle, and how the property of a dual network (here voltage gain), can be determined directly from the dual property of the original network (here current gain).

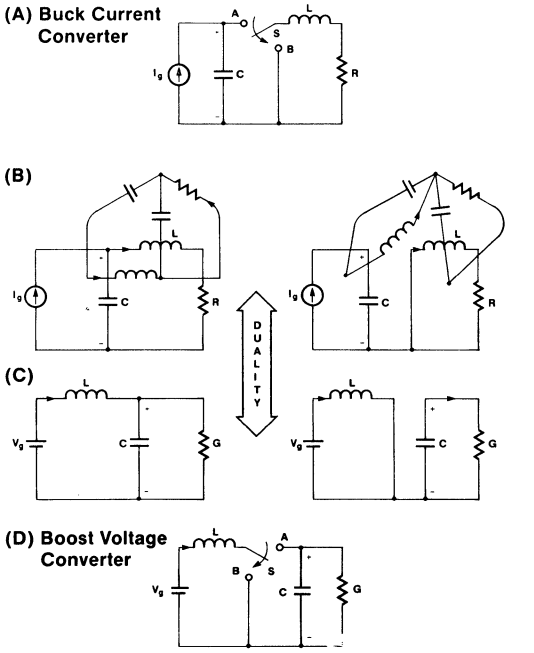


Figure 7: Duality between the Buck and the Boost Switching Converters

"One is now immediately inspired to find dual switching converters to all known switching structures. Once equipped with this powerful tool and method to generate dual switching structures, two goals may be achieved at the same time:

a) the known switching converters can be correlated by a strong bond via duality correlation, and their comparative performance much better understood.

b) new . . . switching configurations may be discovered . . .

"Let us continue this exciting search with the conventional buck-boost converter being the obvious next choice. Again . . . we consider the conventional buck-boost converter as shown in Figure 8A. Following the same algorithm for dual network construction, the dual switched networks of Figure 8C are obtained from the original switched networks of buck-boost converter shown in Figure 8B. Finally, the switching mechanism which leads to the two switched networks of Figure 8C is reconstructed as switch S in the switching converter of Figure 8D. Note that here the use of *oriented* graphs in dual network construction is *absolutely essential,* since only the proper polarity of capacitance C, such as that shown in Figure 8C, leads to the switch S realization, as in Figure 8D. Had the orientation of branches not been used in the duality transformation, the final dual switched networks would leave an ambiguity as to whether the switch implementation is as in Figure 8D.

"The following conclusion can now easily be made from Figure 8. *The dual network of the conventional buck-boost current converter is the new optimum topology (Ćuk) voltage converter.* This now suggests an alternative (deductive) path which could have been followed in the discovery of the new converter topology of Figure 8D . . . The original path of discovery followed quite natural steps of converter performance improvement (cascade of the boost converter followed by the buck converter, hence non-pulsating input and output currents) and simplification with high efficiency in mind (hence reduction of number of switches in a straightforward cascade connection). In any case, both the inductive path and the just-outlined deductive path (coming from the general observation of applicability of the duality principle to switching converters) lead to the same result — the new Ćuk converter topology. Both approaches, however, emphasize the fact that a remaining fourth, very important, member of the family of basic switching converters was missing.

"The establishment of the duality between the two switching converter topologies now permits *all properties* and *results* found for the conventional buck-boost converter to be transferred as dual properties in the Ćuk converter, via the duality principle. Only some of the key essential features and properties will be emphasized here, with the help of Figure 9. For example, the DC current gain of the buck-boost converter $I/I_g = D'/D$ leads to the DC voltage gain of the dual Ćuk converter as:

$$\frac{I}{I_g}\frac{I}{I_g} \rightleftharpoons \frac{V}{V_g} = \frac{D'}{D} \qquad (10)$$

when duty ratio D is referred to homologous point A in Figure 8. However, with respect to point B . . . the DC voltage gain becomes:

$$\frac{V}{V_g}\bigg|_D \longleftrightarrow D' = \frac{D'}{D'} \qquad (11)$$

"Comparison of the waveforms in Figure 9 shows that the nonpulsating input and output voltage waveforms of the buck-boost current converter have been mapped, by the duality transformation, into the very desirable nonpulsating input and output currents of the Cuk voltage converter. In addition to the *inductive energy transfer* of the buck-boost converter, there corresponds a dual *capacitive* energy transfer of the Ćuk converter, since . . . inductance in the buck-boost converter and capacitors in the Ćuk converter are the only energy transferring devices.

"In fact, it is this duality of (the) energy transferring mechanism which has prompted the search for the complete duality of (the) switching converter topologies, and subsequently . . . to the establishment of duality as a general concept for a wide class of switching converters.

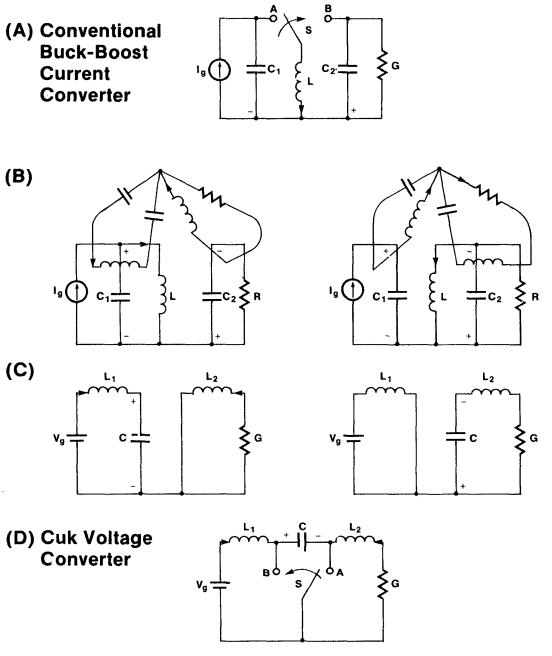


Figure 8: Duality between the Buck-Boost and the Cuk Converters

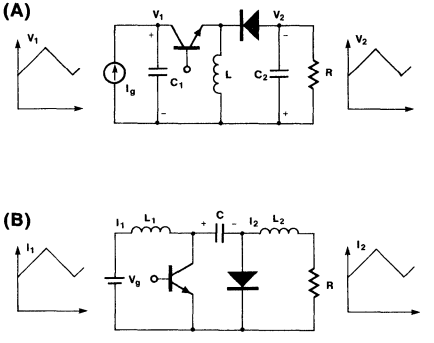


Figure 9: Comparison of Buck-Boost and Cuk Converters

"This also becomes an important distinguishing feature of buck-boost converter types which are based on inductive energy transfer only, and the new Ćuk converters which are primarily based on capacitive energy transfer but . . . not limited to that . . . since some of their extensions (such as coupled-inductor Ćuk converter and single inductor Ćuk converter) possess an additional inductive energy transfer."

Bilateral Inversion**

The duality transformations just discussed can sometimes be difficult to apply in circuits containing transformers, because there is no electrical dual of mutual coupling. Although not as general as the Ćuk method, a simpler duality transformation procedure exists which does not have this problem. It has been demonstrated[5, 6, 7] that the common boost and buck regulators can be made to transfer power from output to input, as well as from input to output (i.e., bilaterally) by the simple expedient of shunting each switch with a diode and each diode with a switch. An example of this is shown in Figure 10, for a boost regulator where Q1 is shunted by D2 and D1 is shunted by Q2. The load is replaced by a source equal to V2; the requirement that V2 > V1 is retained. Switch Q2 is ON when Q1 is OFF. This means that if Q1 operates with a duty cycle of D, then Q2 has a duty cycle of D′ = 1-D. The direction of power flow is now a function of D. The procedure can be carried one step further, as shown in Figure 10C; Q1 and D1 are removed from the circuit and source V1 is replaced by a load with a potential of V1 across it.

The circuit in Figure 10C is simply a buck regulator. Again one sees the duality between the buck and boost regulators. The rules for bilateral inversion are as follows:

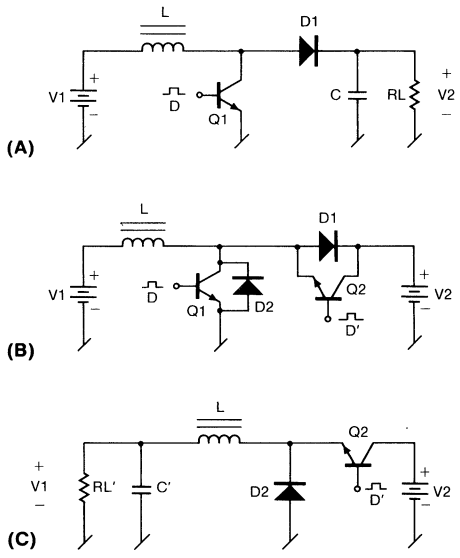


Figure 10

1. All switches are replaced by diodes phased to conduct current in the opposite direction from the original switch.
2. All diodes are replaced with switches phased to conduct current in the opposite direction.
3. If the duty cycle of the original switches is D, then the new switch duty cycle is D′ = 1-D.
4. If, for given D, the input voltage is V1 and the output voltage is V2, the original source is replaced by a load with a potential of V1 and the original load is replaced by a source with a potential of V2.
5. For a given D, an original load R_L and output capacitance C, the inverse output load and capacitance is:

$$R'_L = R_L \left(\frac{V1}{V2}\right)^2$$

$$C' = C \left(\frac{V2}{V1}\right)^2$$

6. For particular D, V1, V2 and output power, the value of $L_{critical}$ is unchanged.

The diodes and switches referred to in rules 1 and 2 are only those directly involved in the power conversion process, not those acting as snubbers or other control function.

This inversion process is general, and can be applied to a wide variety of more complex converters. This provides a tool by which new circuits can be derived from known circuits. An example of this procedure for a more complex cicuit is given in Figure 11; the circuit in 11A is a well known voltage-fed configuration (sometimes referred to as a quasi-square wave converter); Figure 11B is the circuit after bilateral inversion is applied. This circuit is a form of a symmetrical transformer coupled boost regulator, in which the switches conduct simultaneously for part of the cycle. A switch timing diagram for circuits A and B is shown in Figure 12.

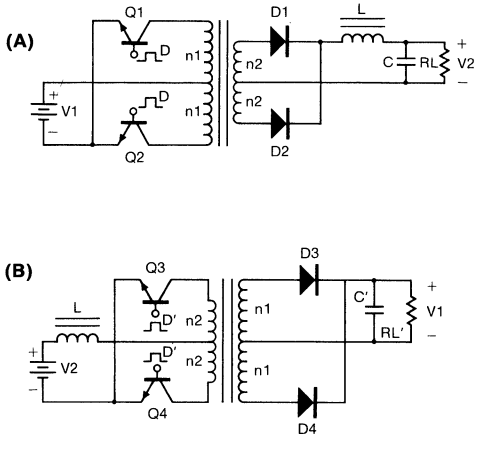


Figure 11

Overlapping Conduction

The use of overlapping switch conduction is not seen very often in present converters, because in many circuits the results are catastrophic. However, in some converters, overlap is not only harmless but can be useful as shown by the example in Figure 12.

**Portions of this section were originally published in the proceedings of the European Power Conversion Conference, 1979.[10]

In many (usually only current-fed) circuits, overlappng and non-overlapping operation may be combined to enhance the circuit's operation. Figures 13, 14 and 15 show an example of such a circuit.

Non-overlapping, Mode A (Figure 14), operation prevails for $V_i \geq V_b$. During STATE I, energy is drawn from the source and then delivered to the load and stored in L. In STATE II, S1 opens and the energy stored in L is delivered to the load. During Mode A, the input current is discontinuous and the load current is continuous.

Overlapping, Mode B (Figure 15), operation prevails for $V_i \leq V_b$. During STATE I, energy is drawn from V_i and stored only in L. During STATE II the energy stored in L is discharged into the load. In this mode the input current is continuous and the output current is discontinuous.

By controlling the switches appropriately, it is possible to design a converter that is a boost regulator at low line voltages and buck regulator at high line.

The foregoing example shows how the basic nature of the converter can be altered, by changing the switch sequence without changing the topology. This technique is not limited to this particular topology but can be used with many other circuits. Figure 16 shows an example where a well known current-fed converter can be made to operate as either a buck, boost or buck-boost converter simply by altering the switch sequence. If a large capacitor is connected from input to output and the switches sequenced for buck-boost operation, the circuit will act as a single inductor Ćuk converter.

Interchange of Switch Connections

Figure 17 shows four common rectifier connections. It is well known that any one of them can be used on the transformer output, simply by altering the transformer secondary turns and the diode current and voltage ratings. If bilateral inversion is applied to each of the rectifier connections, the result is the switch connections in Figure 17(E-H).

Note that there are a large number of rectifier connections used in practice, but relatively few switch connections. The bilateral inversion principle can be applied to these rectifier connections to generate new switch connections.

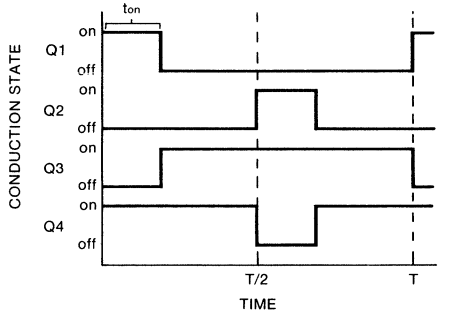


Figure 12

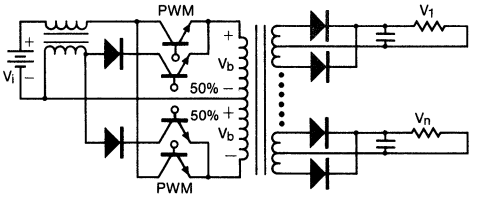
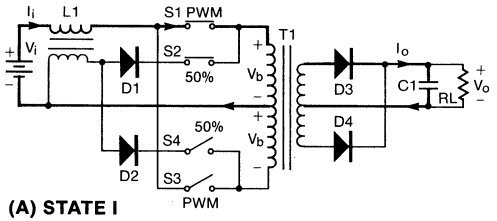
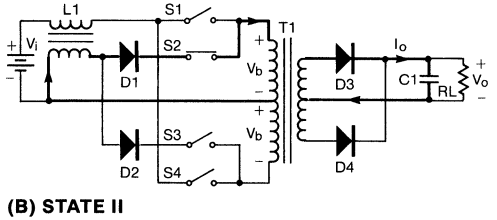


Figure 13

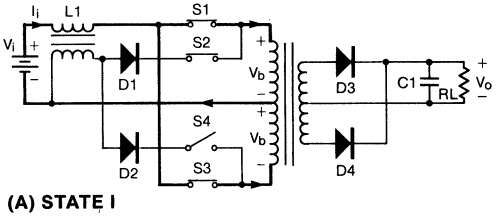


(A) STATE I

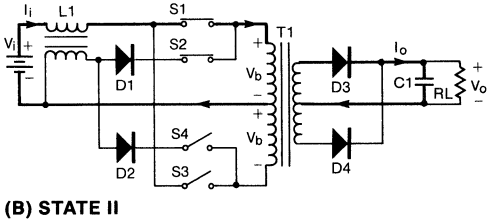


(B) STATE II

Figure 14



(A) STATE I

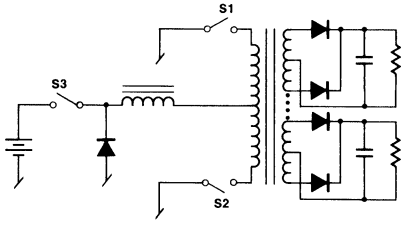


(B) STATE II

Figure 15

The circuit in Figure 17C is a voltage doubler. Another form of doubler is shown in Figure 18A. If this connection is inverted, the switch connection in Figure 18B which results is an alternative to the popular half bridge. This variation is rarely seen in practice but should be useful.

The next step up in this process is to invert a voltage quadrupler, as shown in Figure 19. In the case of the inverted doubler, the switches see the line voltage and twice the line current. For the inverted quadrupler, the switches see one-half the line voltage and four times the line current. This connection would be useful for very high voltage busses. The circuit divides the line voltage across the switches naturally, without the need for complex device matching or voltage sharing networks.



Mode A, Buck Regulator
S_3 = PWM, S_1 and S_2 = 50% conduction

Mode B, Boost Regulator
S_3 = always ON, S_1 and S_2 = overlapping PWM

Model C, Buck-Boost Regulator
STATE I, S_1, S_2, S_3 ON
STATE II, S_2 ON, S_1 and S_3 OFF

Figure 16

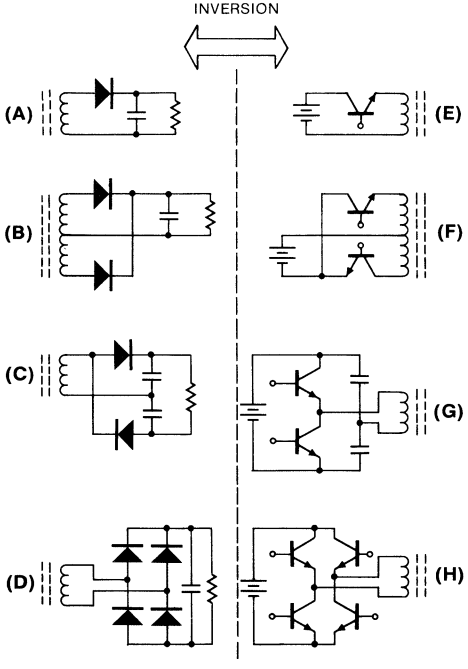


Figure 17

SYNTHESIS USING DC TRANSFORMERS AND BUCK OR BOOST REGULATORS

A wide variety of converter topologies can be synthesized by using a combination of a boost or buck regulator and some form of DC transformer. The DC transformer can take a wide variety of forms, two of which are shown in Figure 20. The function of this circuit element is to provide voltage and current level transformation, either up or down, within the regulator. For the purposes of this discussion, the switches, transformers and diodes are assumed to be ideal.

The Buck Derived Family of Converters

As a starting point let us begin by combining the buck regulator with a parallel connected DC transformer. The buck regulator circuit will be progressively opened at points A through

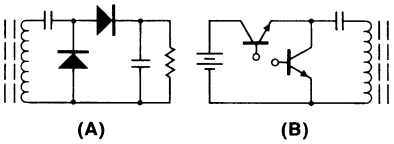


Figure 18

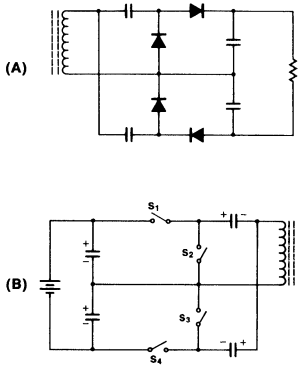


Figure 19

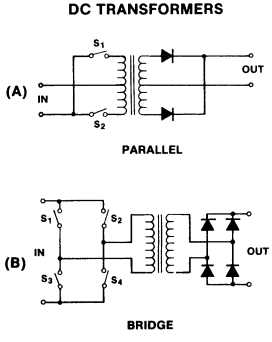


Figure 20

E, and the DC transformer inserted as shown in Figure 21. When this is done, the group of circuits in Figure 22 is generated. Figure 22A is simply a pre-regulator DC-DC converter, 22B is a current-fed DC-DC converter, and 22C and D are essentially identical because the diodes are not needed for the circuit operation. Here is a new circuit apparently, but as will be shown shortly it simplifies into one well known. Figure 22E is a DC-DC converter driving a post-regulator. Circuits 22A and E are dead ends, but 22B and C can be modified to

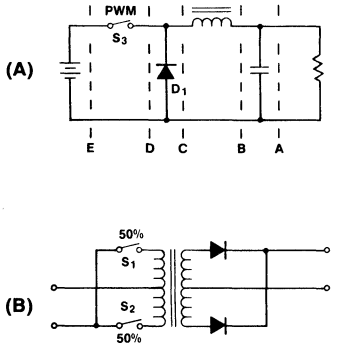


Figure 21

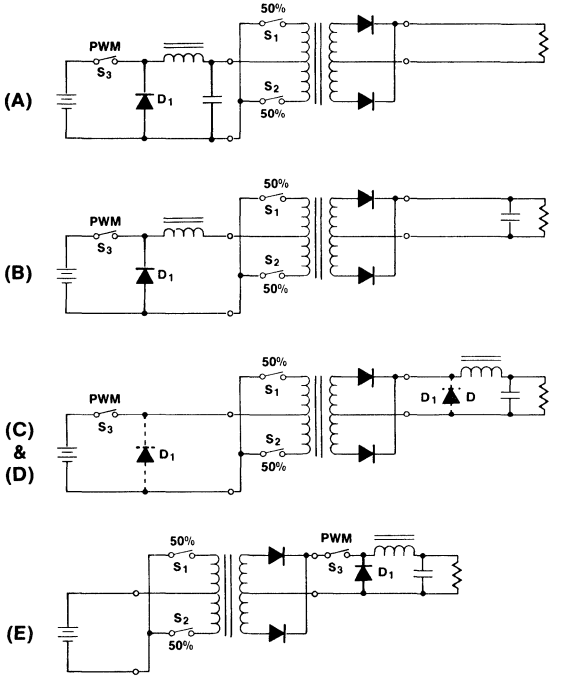


Figure 22

form a variety of circuits. S3 in 22C is really redundant, its function can be performed by S1 and S2. This results in the circuit in Figure 23A, which is the common parallel quasi-squarewave converter. If a bridge rather than a parallel DC transformer had been used, the bridge form (Figure 23B) of the quasi-squarewave converter would have resulted. Figure 23 can be modified in a wide variety of ways; Figures 24 and

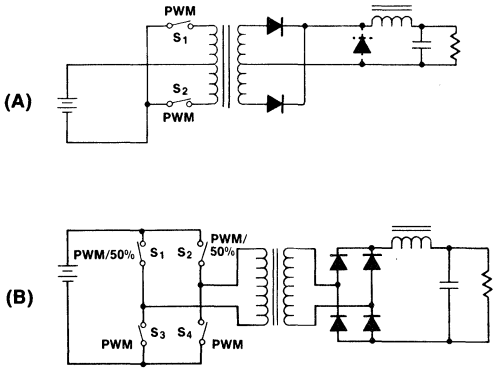


Figure 23

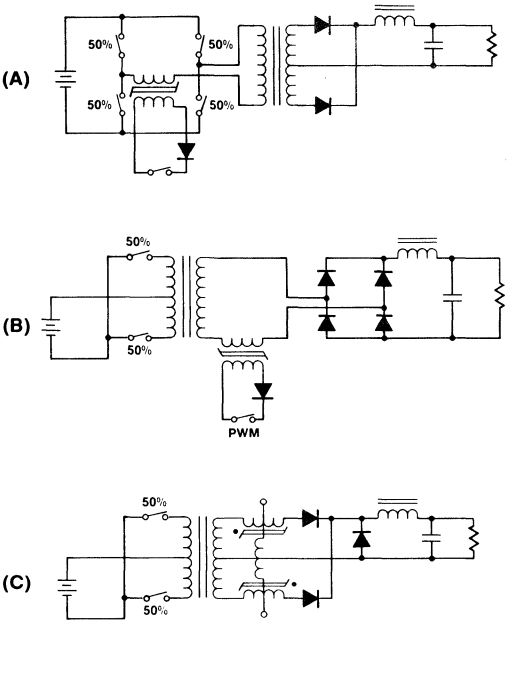


Figure 24

25 show some variations using saturable reactors for fixed frequency (Figure 24) and variable frequency (Figure 25). A host of other variations is possible.

The circuit in Figure 21B also provides a wide variety of variations, beginning as shown in Figure 26. One starts with A, and then in B, S3 is shifted to the negative lead of the

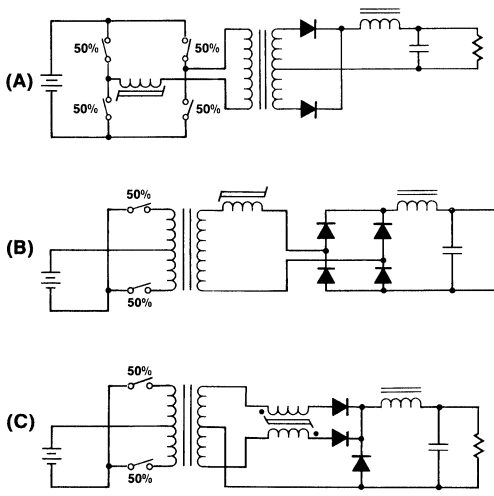


Figure 25

source. In C the connection between S1 and S2 is broken and S4 and D2 added. The result is Figure 26D, which is another current-fed converter. Despite the additional diode and switch, this circuit has some advantages; the PWM switches are referenced to the ground node, the input power is now shared by two transistors instead of one, 100% duty cycle in A corresponds to 50% duty cycle in B. The current in D1, Figure 26A, is commutated by reversing the voltage across the devices. In real devices with finite reverse recovery times, this

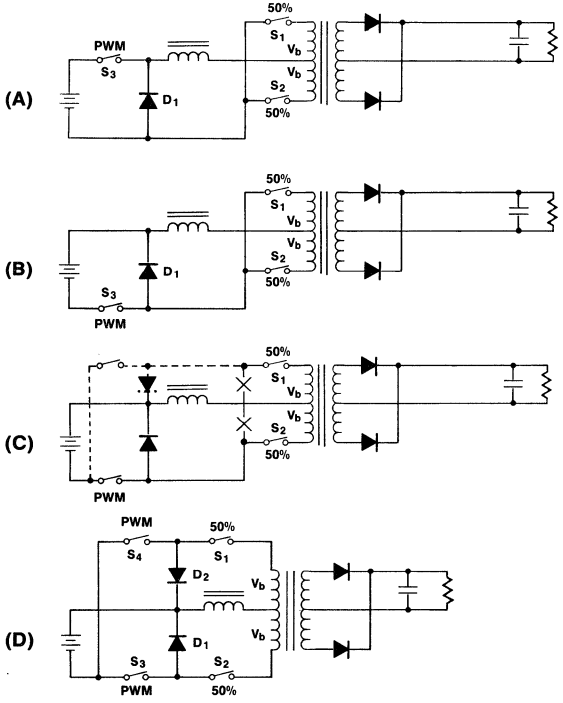


Figure 26

causes a large current spike to be drawn through S3. In the circuit in Figure 26D, the current in diodes D1 and D2 is commutated by opening their respective series switches, so that when the voltage is reversed across the diode only a very small current spike is present. For high voltage sources the circuit in Figure 26D is very useful, because S3 and S4 see no more than the line voltage and S1 and S2 see only twice the reflected voltage, V_b, which can be made low. For low voltage sources the circuits in Figure 26 are at a disadvantage, however, since there are two switches in series during part of the switching cycle which reduces the efficiency. The circuit can be modified as shown in Figure 27. As before, S1 and S2 conduct alternately, each with 50% duty cycle, and S3 and S4 are modulated. In this circuit the current only flows through one switch at a time, because D1 is reverse biased while S3 is ON; the same applies to D2 and S4 on the other half cycle. The penalty for increased efficiency is that now S3 and S4 will see the line voltage plus twice V_b.

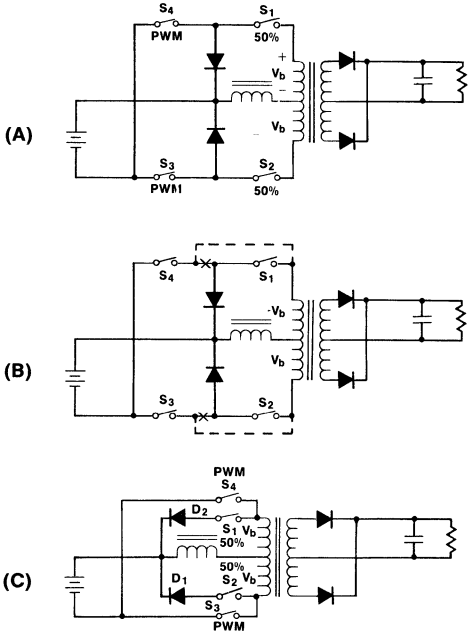


Figure 27

The circuit in Figure 27C can be modified as shown in Figure 28, by using a dual winding choke. This circuit can be further modified, as shown in Figure 29, by connecting one choke winding and the inner switches and diodes to the output. In making this modification, S1, S2 and D2 are no longer necessary; This results in Figure 29C, which is a two switch current-fed converter with the properties of a buck regulator with DC isolation and arbitrary output voltage.

Instead of separate windings on the choke, a tapped winding may be used to produce the variations in Figure 30.

If, in the beginning, a bridge connected DC transformer had been used instead of one which was parallel connected, slightly different circuits would have resulted. For example,

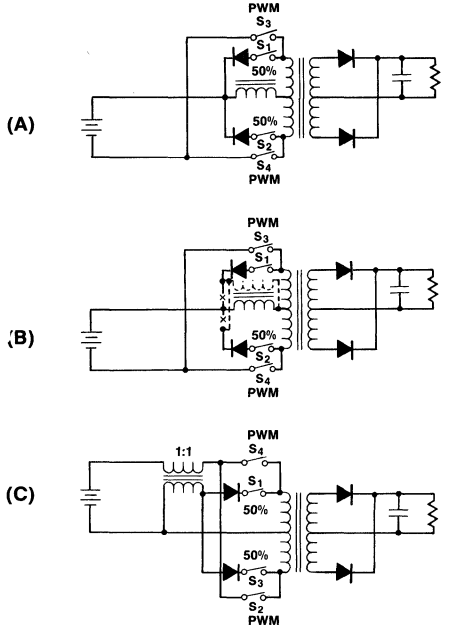


Figure 28

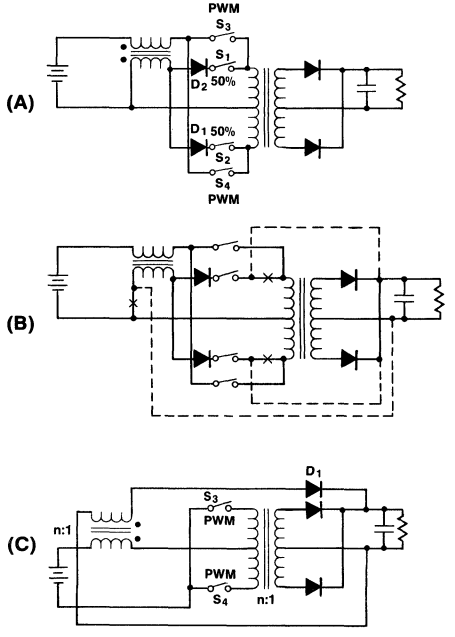


Figure 29

instead of the circuit in Figure 31A, one would have the variation in Figure 31B. This circuit can now be modified, as was done in Figures 26 and 27, to produce the variations in Figure 32. Using a bridge connection, Figure 29 becomes Figure 33A, which is a current-fed bridge inverter. With a bit more manipulation, the circuit in Figure 33B can be derived.

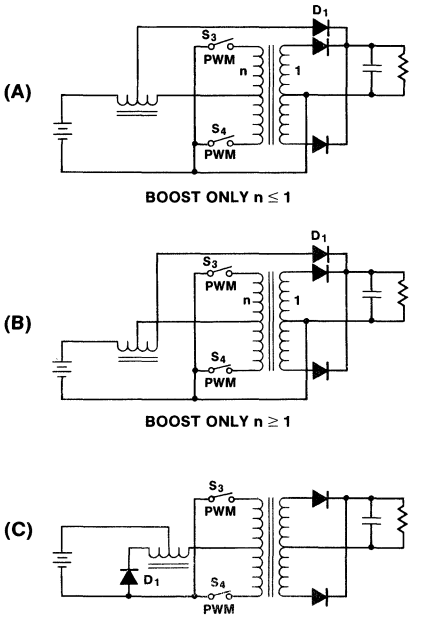


Figure 30

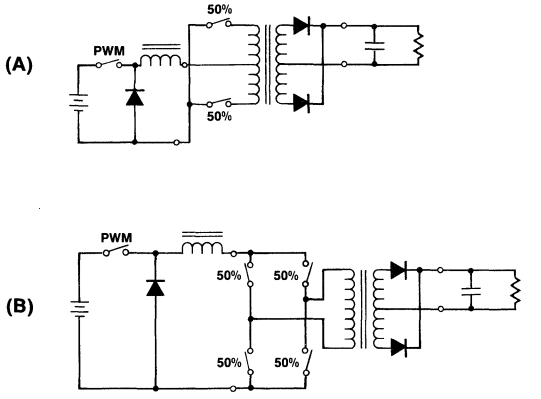


Figure 31

By a process of simple manipulation, and combining a buck regulator with a DC transformer, a family of converter circuits has been derived which are all clearly related and, despite differences in the circuit connection, have in common the properties of the buck regulator. Most of the circuits derived in this section are relatively well known, but in the next section the process will be repeated for the boost regulator; and this will result in a number of circuits that have not been seen before.

The Boost Derived Family of Converters

An entire family of converters with boost properties can be generated by combining a boost regulator with a DC transformer. As before, the DC transformer will be sequentially

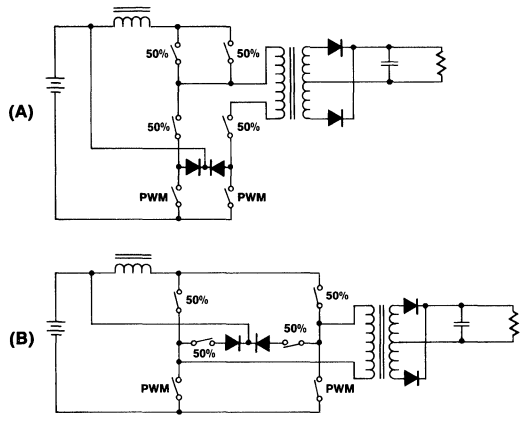


Figure 32

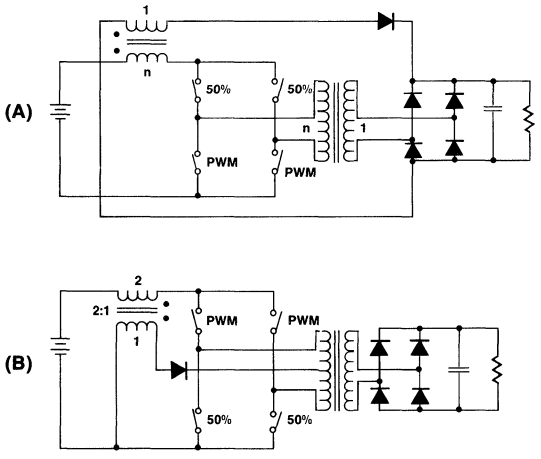


Figure 33

inserted into the regulator (Figure 34). The results of this combination are shown in Figure 35. A is a boost pre-regulator followed by a DC-DC converter. In B and C, the diode D1 serves no function, and can be omitted to form a new circuit. This is a current-fed converter, modulated by periodically shunting the primary. In D, the control element is shifted to the secondary, and the modulation is accomplished by shorting the secondary, again we have a new circuit. The circuit in E is simply a DC-DC converter with a boost post-regulator.

The function of S3 in Figure 36A can be performed by S1 and S2 if S1 and S2 are allowed to have an overlapping conduction interval. This is another way to derive the circuit in Figure 11B.

The circuit in Figure 35D is a usable converter, but it suffers from the disadvantage of having the output current pass through two diodes in series. An alternate and more efficient connection is shown in Figure 37B, where the load current flows through only one diode. The ultimate is reached in Figure 37C, where D1, D2 and S3 are moved to a separate

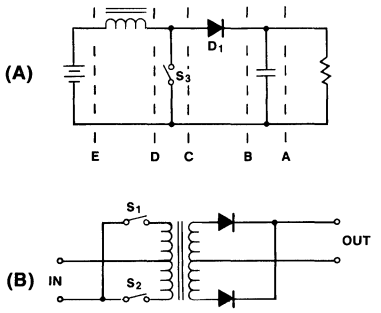


Figure 34

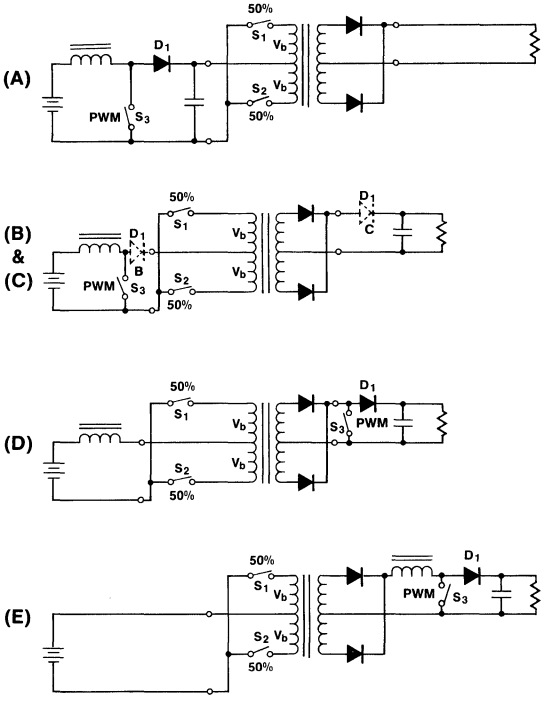


Figure 35

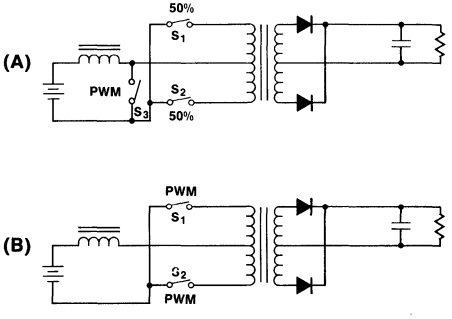


Figure 36

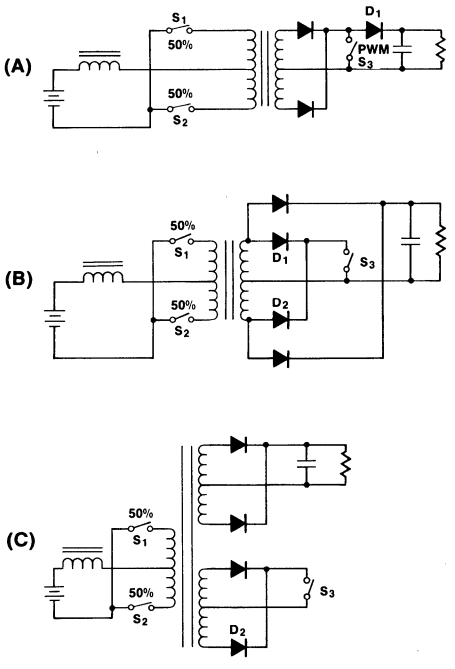


Figure 37

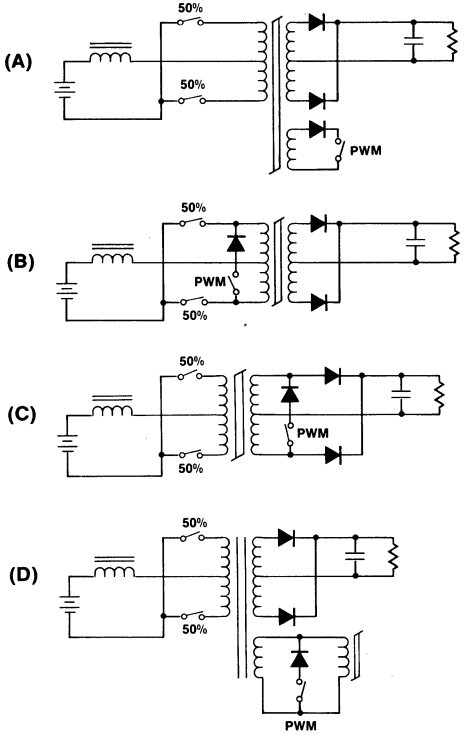


Figure 38

winding, which can be proportioned to provide the optimum voltage and current for S3 independent of the output voltage.

This is a particularly interesting circuit that allows isolation between source, load and control loop. The power chopping is done on the primary, but the control is in the secondary, eliminating the need for isolation within the control loop.

Like the buck family, these circuits also have many variations, as shown in Figures 38 and 39 for saturable reactor control, and Figure 40, for bridges.

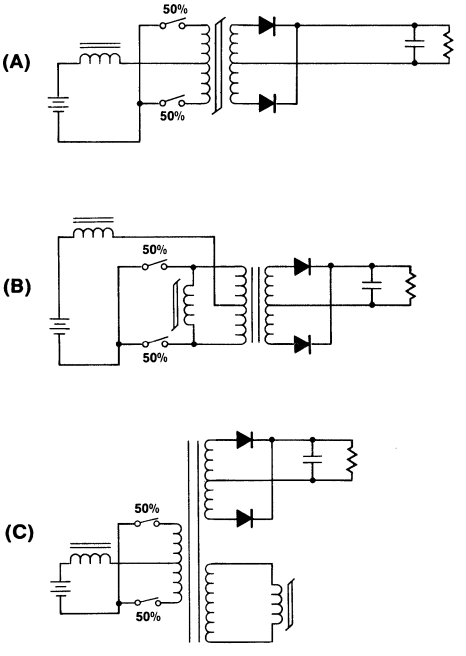


Figure 39

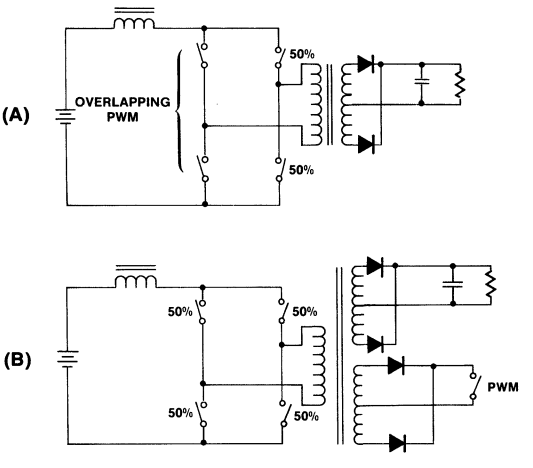


Figure 40

Single Ended Converters

For many applications, low component count is of paramount importance; the family of single ended converters is usually preferred for simplicity. By using a boost or buck regulator combined with a single ended DC transformer, as shown in Figures 41 and 42, if the parallel or bridge DC transformers are divided in half, the result is single ended DC transformers. If these transformers are combined with a buck regulator in manner such as the quasi-squarewave converter, the feed forward converter is the result, as shown in Figure 43. Figure 43B looks a bit strange, and in this form is not really useful, but as will be shown shortly, a minor modification will make it most useful. Both circuits lack one important ingredient, a means for resetting the core. The family of feed forward converters is quite large, but the differences within the family are related to the means by which the core is reset. The basic energy transfer is identical, even though the circuits may look very different.

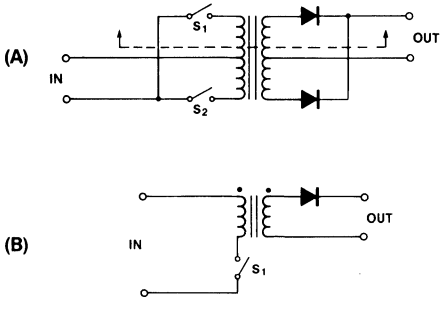


Figure 41

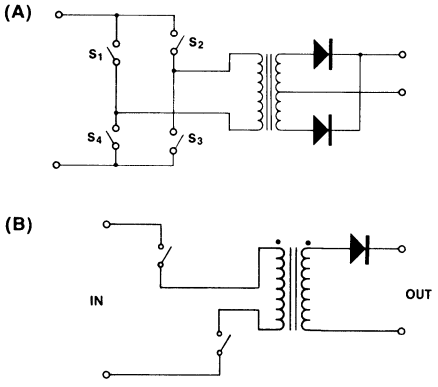


Figure 42

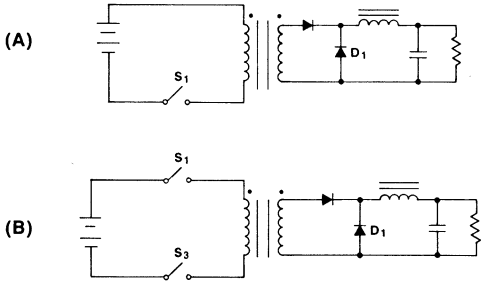


Figure 43

The designer has two choices (Figure 44); he may select a core which has a low Br and which will self discharge or he may select a very square core with little energy storage and then reset the core externally.

In the case of self-resetting, the energy may be dissipated in the primary or secondary (Figure 45), or recovered in the primary or secondary, as shown in Figures 46 and 47.

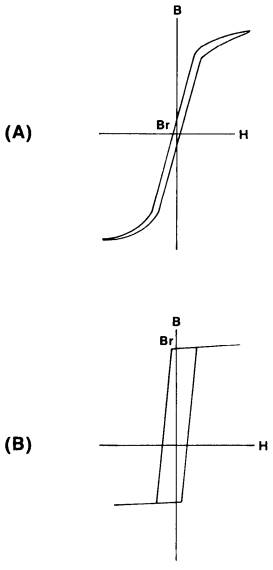


Figure 44

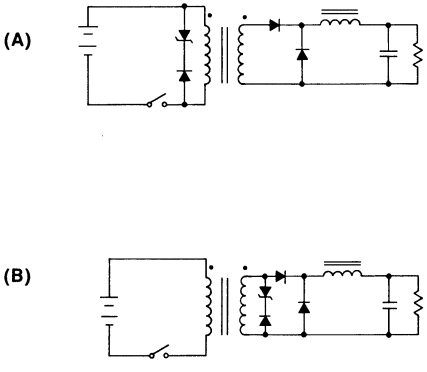


Figure 45

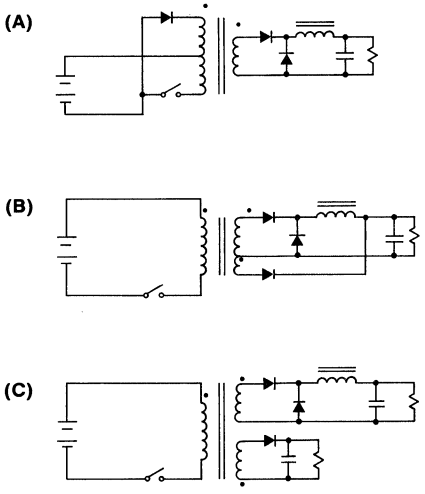


Figure 46

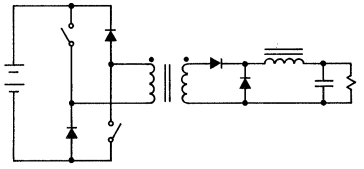


Figure 47

Where a square loop core is used, external current reset can be provided as shown in Figure 48. The current supplied by a DC source as in A, or better yet, derived from the output choke, as in B. These types of current reset do not define the winding voltage during reset. A variety of voltage clamps for current reset can be used as shown in Figure 49.

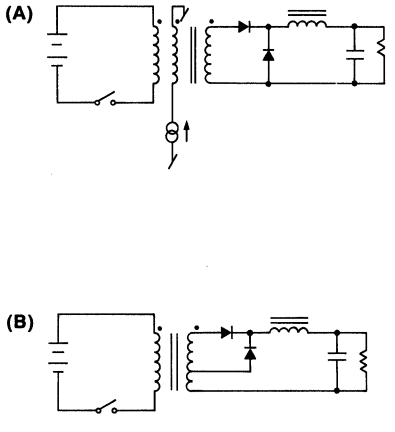


Figure 48

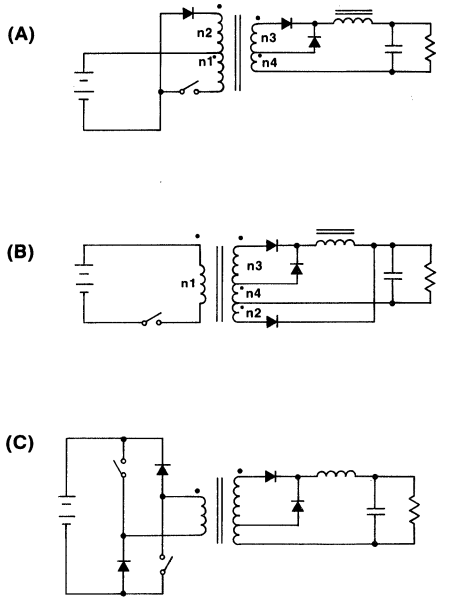


Figure 49

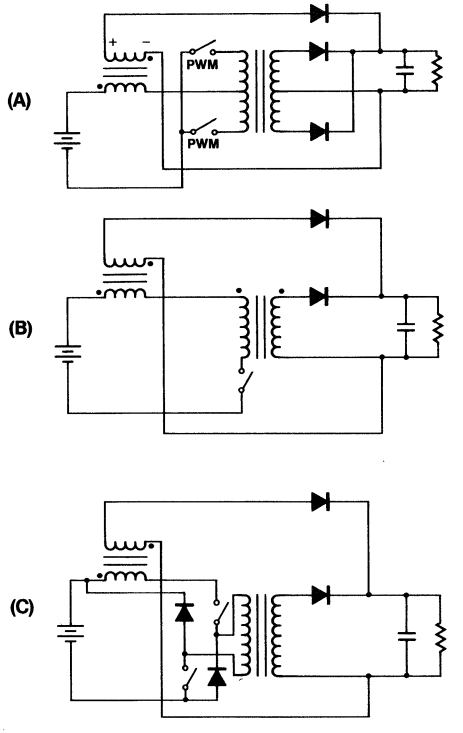


Figure 50

The quasi-squarewave converter is not the only member of the symmetrical converter family that has a single ended equivalent. As shown in Figure 50B, the Weinberg circuit (Figure 29C) is another which can be single ended. Again, the core reset means is omitted, and the designer is free to select the reset scheme and core of his choice. Figure 50C is one possible example.

Single ended versions of symmetrical boost converters can also be derived, as shown in Figure 51 where A is converted to B. To maintain current continuity in the choke, the duty cycle of S1 is now the complement of S3.

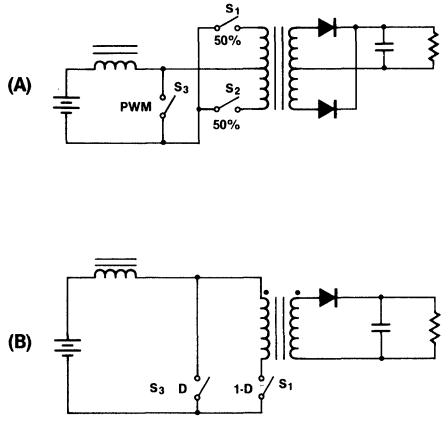


Figure 51

Limitations On This Procedure

It has been demonstrated that inserting a DC transformer into a buck or boost converter can produce a wide variety of useful topologies. The procedure does not, however, work for all regulators and all DC transformers.

For example, if a parallel connected DC transformer is inserted into a Ćuk converter, most of the combinations will not work. This is because the Ćuk converter requires a bidirectional flow of current to function, and the usual switch in the primary, rectifier in secondary DC transformer connection does not permit this. The designer must be on the lookout for this problem. For some circuits the single ended DC transformer does not provide for continuous current flow in the inductor, so that such variations don't work.

Even with these restrictions a huge number of circuits can still be developed.

SYNTHESIS USING COMBINATIONS OF CONVERTERS

A very powerful technique for deriving new circuits is to treat buck and boost regulators and the DC transformers as two port networks, and then combine these networks in various arrangements.

A few of the many possibilities are shown in Figure 52. Beginning with A, similar or dissimilar converters can be cascaded. An outstanding example of this process is the Ćuk converter (Figure 53A) which was initially derived by cascading a boost followed by a buck regulator. This topology has several important variations, as shown in Figure 53B, C and D.

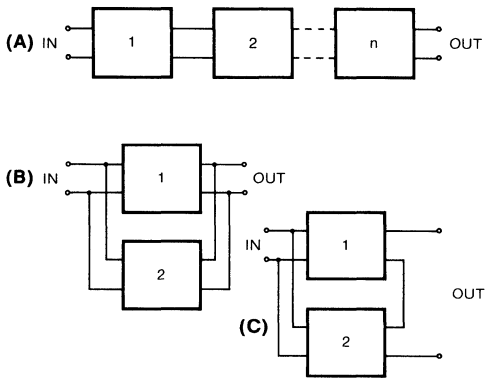


Figure 52

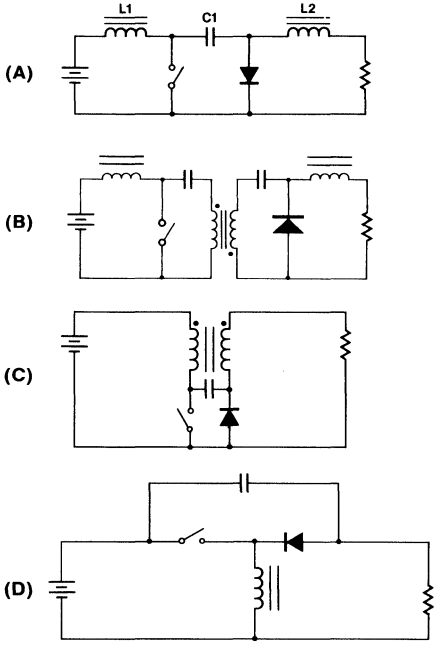


Figure 53

The Ćuk converter has the unusual property of zero input or output ripple in the coupled inductor case. By an additional circuit permutation, it is possible to have zero current ripple on *both* the input and the output. Figure 54 shows one way to accomplish this. A is the basic circuit. In B, C is divided and an inductance L is added. In C, the three inductors are coupled. Zero input and output ripple is achieved by adjusting the mutual coupling between the windings or by using trimming inductors.[37] Figure 55 shows some other variations to achieve the same goal.

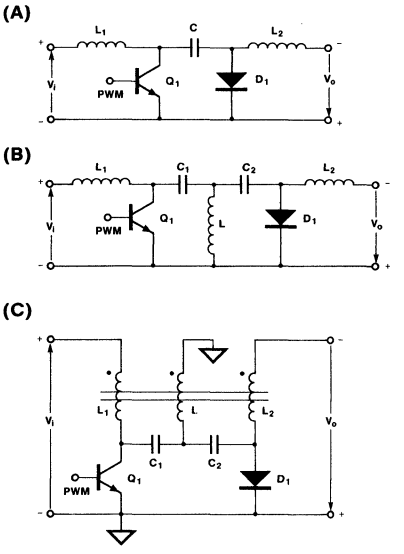


Figure 54

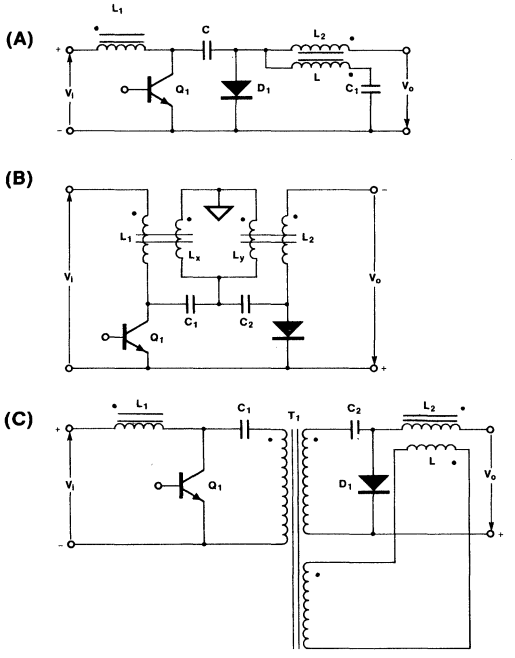


Figure 55

It can be shown that the common buck-boost regulator (Figure 56A) circuit may be derived from a cascaded connection of a buck followed by a boost regulator. By the simple expedient of using a multiple winding choke, the popular flyback converter is derived.

A cascade connection of a boost and a buck-boost is shown in Figure 57A. This can be transformer isolated in the same way as the flyback, by making L2 a multiple winding choke

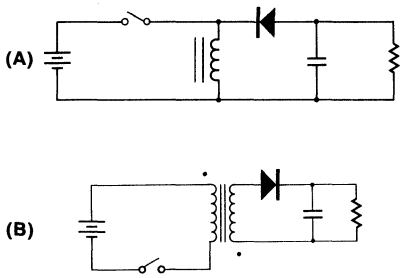


Figure 56

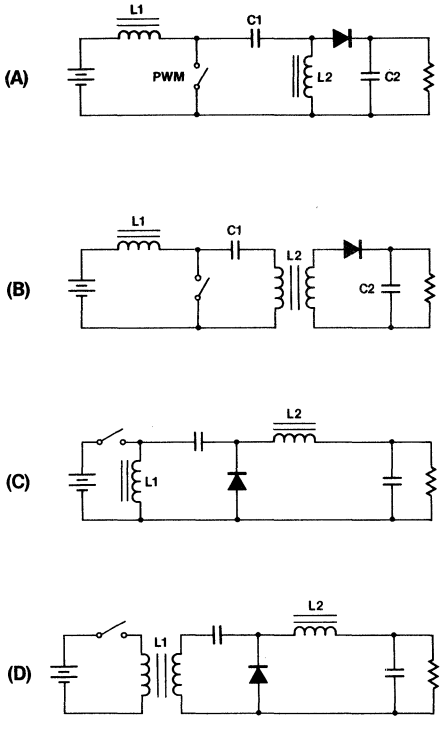


Figure 57

(Figure 57B). If duality is applied to these two circuits, the arrangements in Figure 57C and D are obtained.

Identical converters can also be cascaded with useful results. An example of this is given in Figure 58. The input to output voltage transfer ratio is:

$$\frac{V_i}{V_o} = (D)^n$$

This circuit connection can be very useful when large transformation ratios are desired. Using a single buck stage for a large transformation ratio results in very narrow, high amplitude current pulses which restrict the power handling capability of the switching device. This is a very real limitation in off-line converters. By cascading two or more converters, a

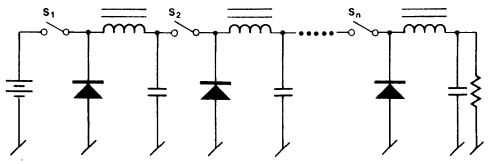


Figure 58

larger duty cycle is used which reduces the current amplitude. For example, a converter using a single stage operating with a duty cycle of 0.1 would have a duty cycle of 0.32 if changed to two stages, a three to one reduction in peak current! A second benefit is that S2 would see only 32% of the input line voltage, and could be a less expensive device than S1.

Paralleling of converters (Figure 52B) is another very useful way of increasing the power capability. By altering the switch drive phasing between the converters, the output ripple frequency can be increased and the amplitude decreased.

Cascading and paralleling are not the only possibilities. An example (Figure 52C) of connecting the inputs of two converters in parallel with their outputs in series is shown in Figure 59A. This is a combination of a DC-DC converter and a flyback converter. If bilateral inversion is applied to A, then the circuit in B results; another way to derive the circuit in Figure 29C.

The possible combinations are endless and really limited only by the designer's imagination and persistance.

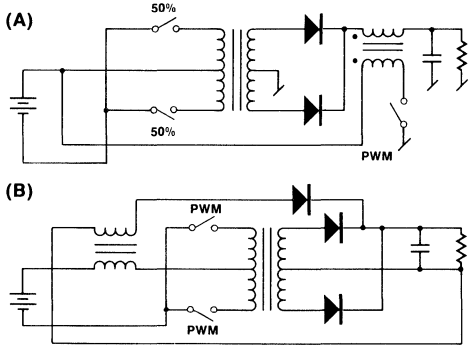


Figure 59

Limitations to the Procedure

Not all of the possible four terminal combinations yield working circuits, and general rules as to what will or will not work have not yet been derived. The designer must, for the present, use a cut and try approach.

SYNTHESIS USING TRANSFORMER AND INDUCTOR TAPPING

A very simple way to modify known circuits in useful ways employs tapping of the inductor and/or transformer.

Inductor Tapping

One of the simplest modifications is to tap the inductor to alter the component voltage or current stress, as shown in Figure 60.

The concept of tapping the inductor may be extended to the use of multiple windings. It has been shown that the multiple wound inductor can be used in place of multiple inductors, as shown in Figure 61, with a significant savings in size and weight.

A circuit using a two winding choke can also be used to reduce the size of a filter capacitor as shown in Figure 62.

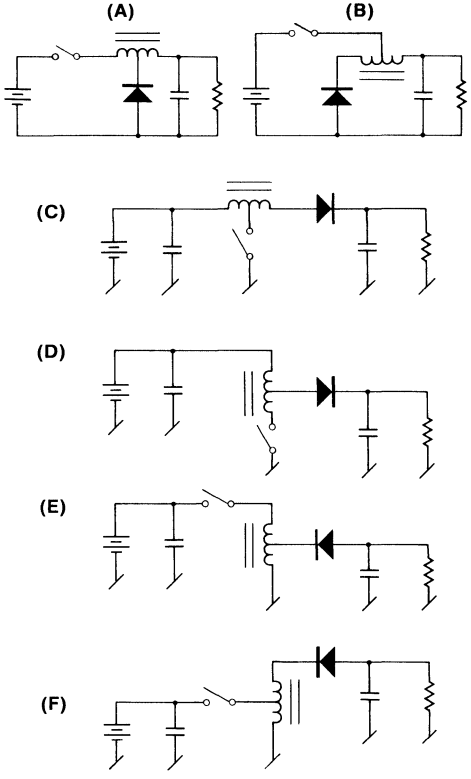


Figure 60

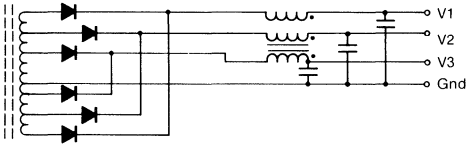


Figure 61

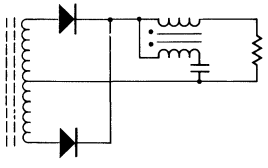


Figure 62

Transformer Tapping

The transformer may be tapped to provide very useful circuit variations. Figures 63 and 65 show some examples. The quasi-squarewave circuit has an output voltage waveform (before the filter) like that shown in Figure 64A. This waveform has a very high harmonic content which must be dealt with by the filter. If the quasi-squarewave circuit is modified to have a tapped primary with two additional switches, as shown in Figure 63A, the output waveform can be made to look like that shown in Figure 64B, with the difference between V1 and V2 determined by the tapping ratios. This waveform can have a much lower harmonic content, which allows the size of the filter to be reduced. Similarly, the input current will also have a lower RMS value, which is of great assistance in reducing EMI. These circuits and some of those in the following section allow the designer to trade circuit complexity for reduced EMI. The disadvantage of these circuits (in addition to the extra switches) is that there is now an upper as well as a lower limit on the line voltage that can be accommodated, for a given tapping ratio. For applications where there is not a large line voltage excursion, the reduction in filter size may be very worthwhile. Figure 63B is a dual of 63A.

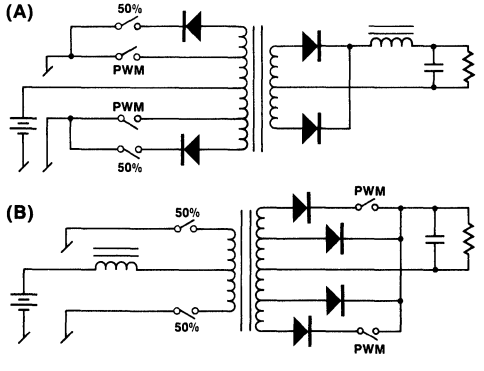


Figure 63

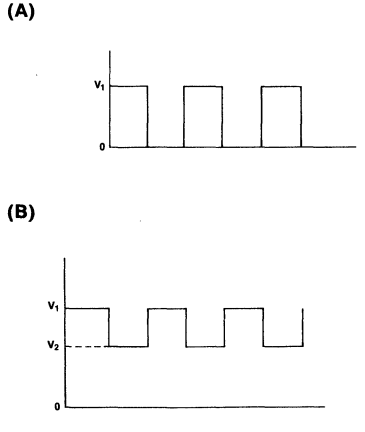


Figure 64: Converter Output Voltage Waveform

Figure 65A is a boost derived circuit using the same principle (S1 and S2 do not overlap); Figure 65B is the dual of this circuit. The bridge versions of these circuits are shown in Figures 66 and 67. This process can be extended by adding 2n additional switches so that the voltage and current ripples approach a sinusoid.

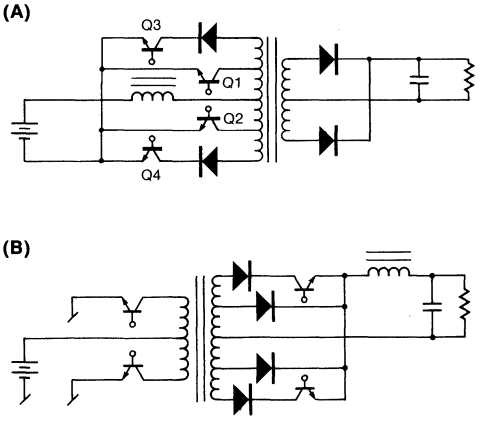


Figure 65

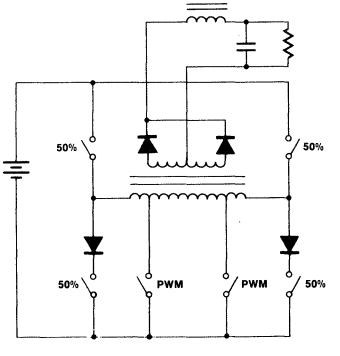


Figure 66

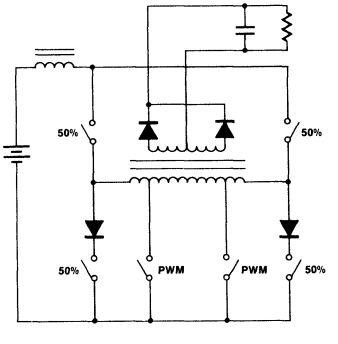


Figure 67

Combined Choke and Transformer Tapping

Tapping of both the choke and the transformer can be combined in one converter. An example of this is shown in Figure 68A, along with its dual, 68B. By tapping the choke, the output current becomes continuous and the input discontinuous. Figure 69 shows the bridge version of Figure 68A.

By tapping the inductor and transformer in the circuit in Figure 70A, the circuit in 70B is generated. This circuit has the advantage of reducing the current in D1 and D2, increasing the circuit efficiency while retaining the continuous output current and current-fed converter nature. This particular combination of tapping does not have the upper limit on input voltage.

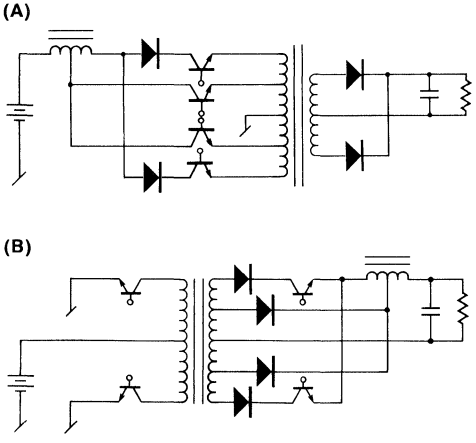


Figure 68

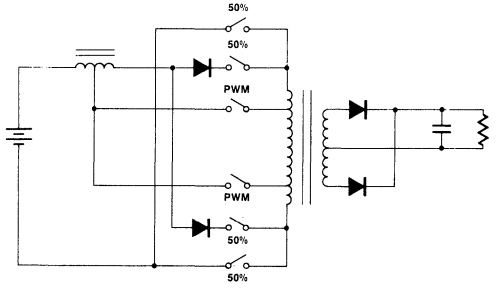


Figure 69

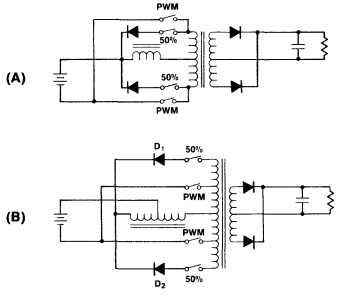


Figure 70

SUMMARY

A wide range of ideas and techniques, many of which are new, have been presented herein. So much has been presented that the reader may find it difficult to see the forest as opposed to the individual trees.

The key ideas that have been presented are:

1. The present popular circuits represent only a small portion of switchmode converter possibilities. The popular circuits are not the only, or even the best, solutions.

2. The designer is not restricted to using the present known converter circuits but can, by modifying the known circuits and synthesizing new ones, derive new circuits to better solve his problem.

3. All of the converter topologies we presently know can be derived from combinations of very simple elements; the buck and boost regulators and some form of DC transformer.

4. Converter topologies can be grouped into families with similar characteristics. One way to perform this grouping is to define the family members on the basis of the basic circuit elements from which the individual circuits are derived.

5. General duality theory can be applied to switchmode converters to provide both insight into circuit relationships and a synthesis tool.

6. A special case of duality, bilateral inversion, leads directly to the use of overlapping and non-overlapping conduction and combinations thereof to alter circuit operation.

7. Bilateral inversion also leads to using rectifier connections as switch connections. This can be extended to multiplier and possibly multiphase connections.

8. Quantitative figures of merit based on component stress and energy storage, and qualitative circuit considerations can be used to compare circuits. Comparisons of large numbers of circuits, in fact, require the use of some orderly process.

9. There are several techniques for modifying known circuits or generating new circuits: duality, bilateral inversion, combinations of boost or buck regulators with DC transformers, combinations of more complex converters, transformer and inductor tapping and, of course, combinations of all these techniques.

10. The designer is free to choose many of the circuit properties, for example: the regulation function may be performed in either the primary, the secondary or in an isolated winding. The control loop transfer function can be altered to either add or remove moving poles and right half-plane zeros. The high current ripple can be moved from the primary to the secondary or vice versa. Both primary and secondary ripple can be reduced at the expense of input voltage range or circuit complexity. By altering the switch conduction modes, the input voltage range can be greatly extended.

APPENDIX I

Effect of Waveform on RMS Value

In a switch mode converter, the current waveforms through the inductors, transformer windings, rectifiers and switches will appear, as shown in Figure 72, ranging from a triangle to a rectangle depending on the value of the averaging inductor and the load. For the capacitors, the waveforms will be similar, except that there can be no DC component, as shown in Figure 73. The RMS and average values of the waveform are given in the figures.

It can be shown that:

$$K \equiv \frac{I_a}{I_b} = f(L/L_c) \qquad (1)$$

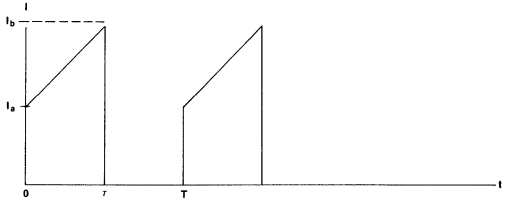
where, L = inductance of the averaging choke

L_c = is the critical inductance for a particular input voltage and load power.

As L is increased, K goes from 0 (triangle) to 1 (rectangle).

Substituting $K = I_a/I_b$, for the continuous choke current case:

$$I_{rms} = \frac{2\, I_{avg}}{\sqrt{D}} \sqrt{\frac{K^2 + K + 1}{3\,(K+1)^2}} \qquad (2)$$



General Case

$I_{AVG} = D\left(\frac{I_a + I_b}{2}\right)$

$I_{RMS} = \left[\frac{D}{3}\left(I_a^2 + I_aI_b + I_b^2\right)\right]^{1/2}$

$D = \frac{\tau}{T}$

Special Cases

1) $D = 1$

$I_{AVG} = \frac{I_a + I_b}{2}$

$I_{RMS} = \left(\frac{I_a^2 + I_aI_b + I_b^2}{3}\right)^{1/2}$

2) $I_a = I_b$

$I_{AVG} = I_aD$

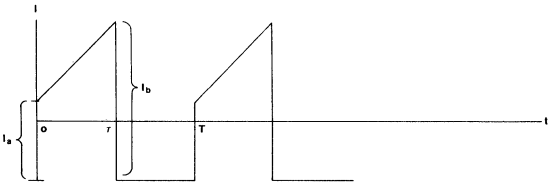
$I_{RMS} = I_a\sqrt{D}$

3) $I_a = 0$

$I_{AVG} = \frac{I_bD}{2}$

$I_{RMS} = I_b\sqrt{\frac{D}{3}}$

Figure 72: Average and RMS Values for Trapazoidal Waveform



General Case

$I_{RMS} = \left\{ D\left[\frac{I_a^2 + I_aI_b + I_b^2}{3} - \frac{D}{4}(I_a + I_b)^2\right]\right\}^{1/2}$

$D = \frac{\tau}{T}$

Special Cases

1) $D = 1$

$I_{RMS} = \frac{I_b - I_a}{\sqrt{12}}$

2) $I_a = I_b$

$I_{RMS} = I_a\sqrt{D - D^2}$

3) $I_a = 0$

$I_{RMS} = I_b\sqrt{\frac{D}{3} - \frac{D^2}{4}}$

Figure 73: RMS Value of AC Component of Trapazoidal Waveform

For constant I_{avg} and D, the normalized ($I_{rms} = 1$ for $K = 1$) I_{rms} is as shown in Figure 74. This curve shows that, for triangular waveforms, the I^2R losses are 32% higher than for rectangular waveforms. It is also apparent that for $I_a/I_b > 0.6$, the

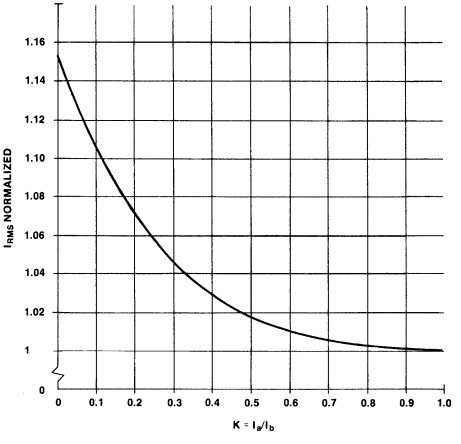


Figure 74

additional losses incurred by having $L < \infty$ is only 2%, so from a practical point of view L need only be about twice L_c. Increasing the value of I_a/I_b increases the switch turn-on losses but decreases the turn-off losses. Since the turn-off losses usually dominate, increasing I_a/I_b reduces the total switch loss also.

For the case of discontinuous inductor current ($L < L_c$), $I_a/I_b = 0$ and is no longer relevant, since the waveforms are now triangles. For a given I_{avg} the RMS current is:

$$I_{rms} = \frac{2\, I_{avg}}{\sqrt{3D}} \qquad (3)$$

A plot of equation (3) is given in Figure 75, where I_{avg} is constant and I_{rms} is normalized for D = 1. Obviously triangular current waveforms with high peak currents and low duty cycles are to be avoided if low losses are desired.

For the case where: $I_a = I_b$:

$$I_{rms} = \frac{I_{avg}}{D}$$

the curve in Figure 75 also applies. It is important to realize that for a given input voltage, current and transformation ratio, there can be a difference in duty cycle which allows one circuit to have lower losses due to the lower value of I_{rms}.

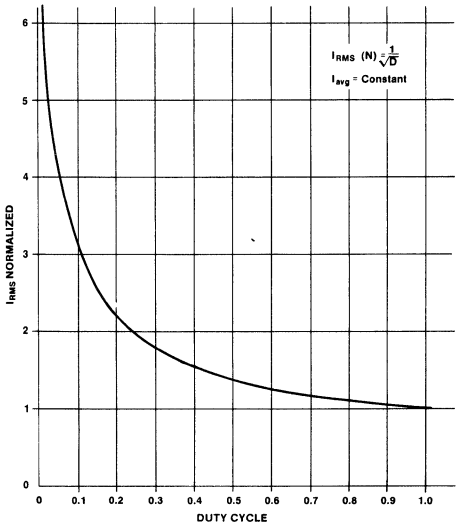
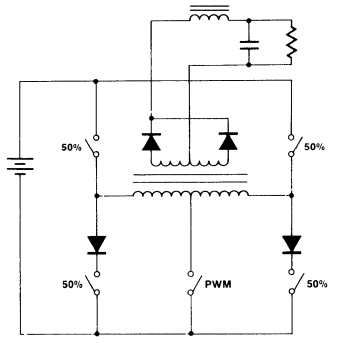


Figure 75: Variation of RMS Current with Duty Cycle.

APPENDIX II

Despite the huge number of circuits presented in the main portion of this application note, there are still many more that could be shown. To provide the reader with as full a picture as possible, some additional circuits are presented here with limited comment.

(A)



(B)

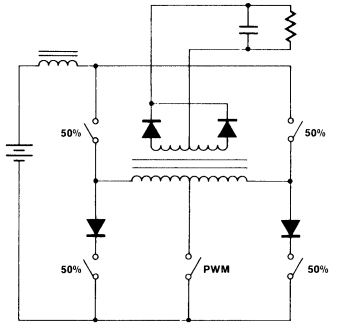


Figure 76

The circuits shown in Figures 63 through 69 have a number of additional variations. When the input voltage range is 2:1 or less, one switch may be eliminated as shown in Figures 76 and 77; the switch connections can also be varied as shown in

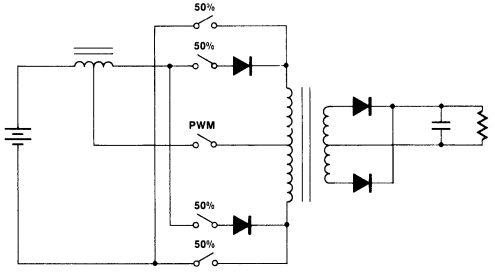


Figure 77

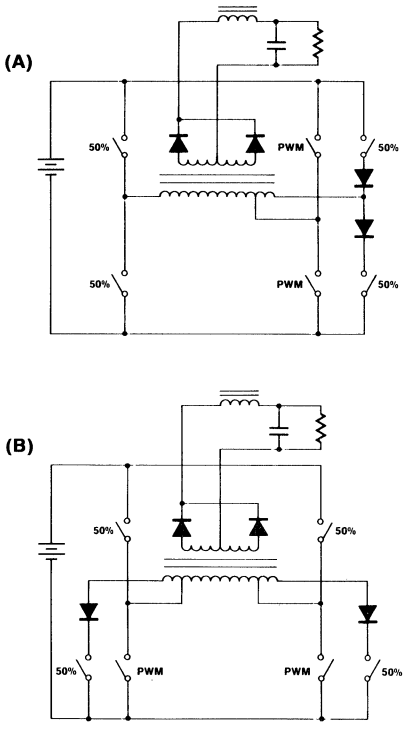


Figure 78

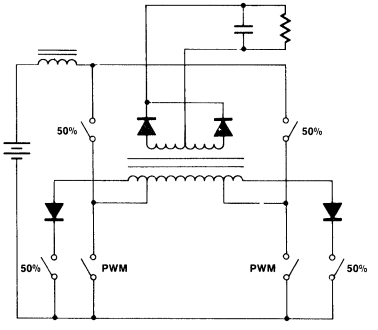


Figure 79

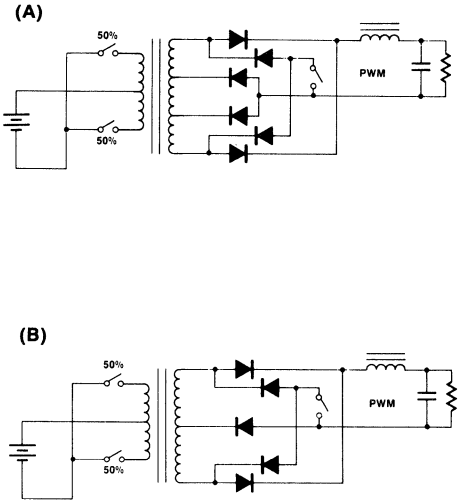


Figure 80

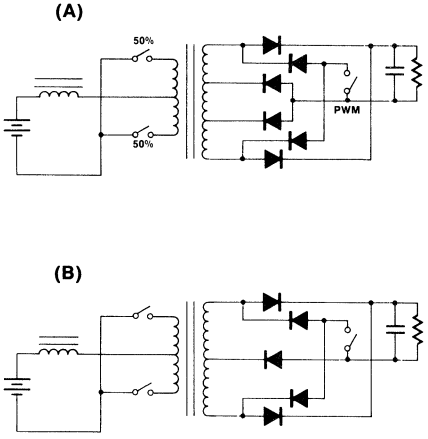


Figure 81

Figures 78 and 79. Some of the duals of this family of converters are given in Figures 80 and 81 and there are also multiple winding versions of these circuits as shown in Figures 82 and 83.

Multiple transformer windings can also be used to reference all the switches to one node, as shown in Figure 84. The extra transformer winding may be cheaper than separate base/gate drive isolation transformers, however, there will be some voltage spiking due to leakage inductances between the primary windings.

Figure 85 shows a variation on the quasi-squarewave half-bridge that is occasionally seen. The bridge version is also possible. The major disadvantage of this circuit is that the inductor must operate in the discontinuous mode. Two more useful variations of this circuit are shown in Figure 86. In A, S1 and S2 use nonoverlapping conduction, and in B, the PWM switch is in the secondary. Bridge versions of both these circuits can be built, with and without dual chokes.

The circuit in Figure 87 is a variation of that previously given in Figure 51B. In this variation, T1 is designed to store energy while L1 is discharging through the transformer into the load (S1 open, S2 closed). While energy is being stored in L1 (S1 closed, S2 open), the transformer discharges into the load. If

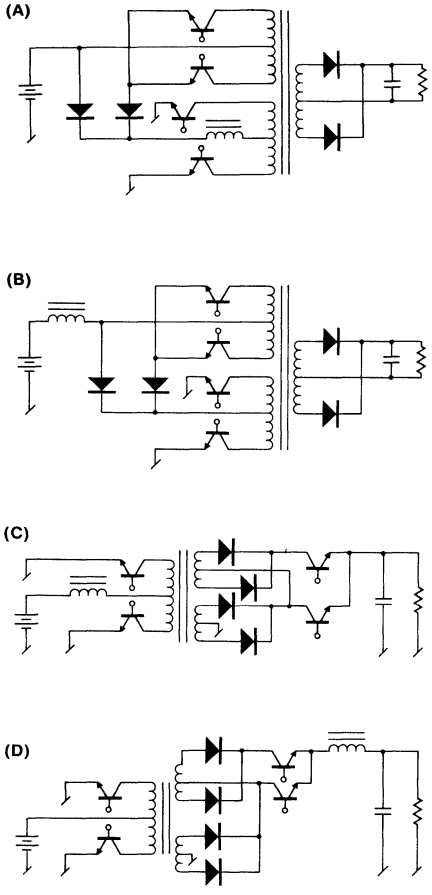


Figure 82

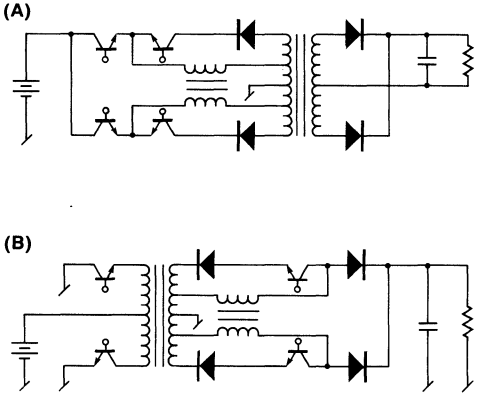


Figure 83

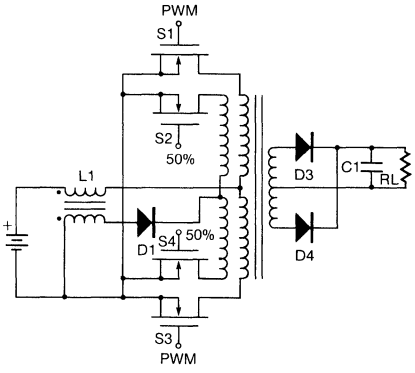


Figure 84

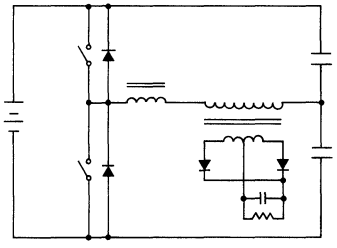


Figure 85

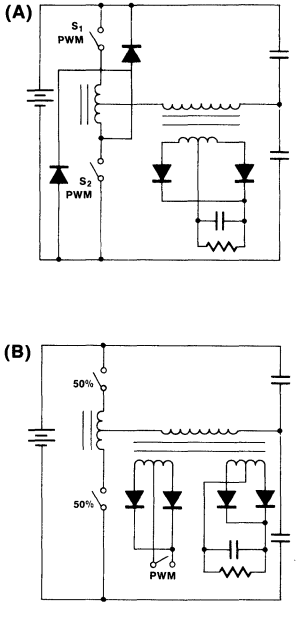


Figure 86

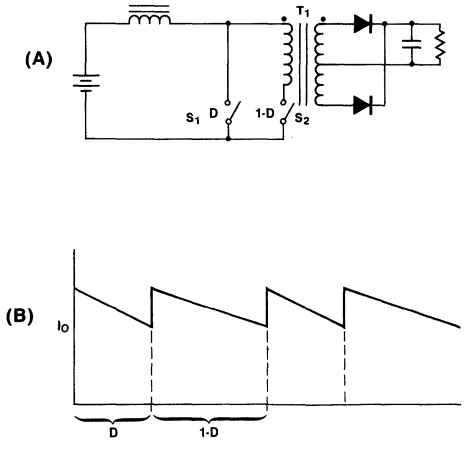


Figure 87

the inductances of L1 and T1 are proportioned correctly, the output current waveform shown in B will result. This has a much lower RMS value than the original circuit and can be made arbitrarily small by increasing the inductance value. This is potentially another low EMI converter circuit.

There are many other combinations of converters. In Figure 88, a buck regulator with continuous inductor current and pulse width modulation is combined with a buck-boost regulator having discontinuous inductor current and variable frequency. The two are combined with PWM and variable frequency control loops to produce a converter with a single switch and two independently regulated outputs.

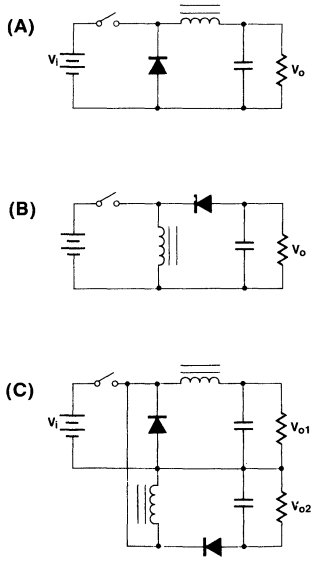


Figure 88

Figure 89A shows a circuit in which two converters have parallel inputs and series outputs. All the switches operate with 50% duty cycle, and modulation is accomplished by

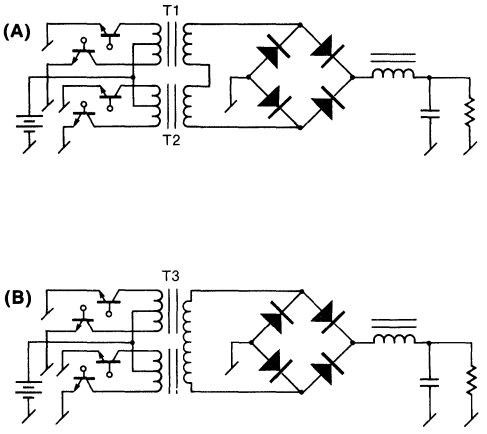


Figure 89

varying the phase between the two converters. This can be done with *n* such converters to synthesize an output waveform. The circuits in Figures 24A and B can be built with one magnetic element instead of two, if a dual core transformer is used as shown in Figure 90.

The circuit previously shown in Figure 27C has some duals as shown in Figure 91B and C.

The circuit in Figure 28C can be reconnected to be similar to that of Figure 26D as shown in Figure 92.

A variation using a tapped choke is shown in Figure 93A. This circuit is interesting in that some of the energy stored in the inductor is returned to the source rather than to the load. The circuit has the unusual property that at certain duty cycles more power is pumped back into the source than is delivered to the load, and the sign of the feedback loop inverts! Possibly, this is an example of a pole moving into the right half plane. The circuit will also work whether or not the switches have overlapping conduction. If this circuit is inverted (B), the boost version which results also displays similar bizarre behavior.

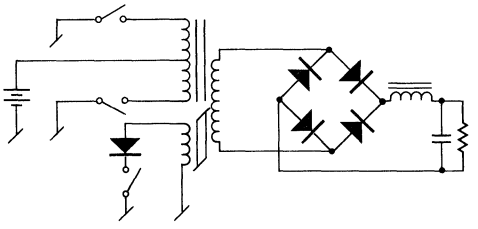


Figure 90

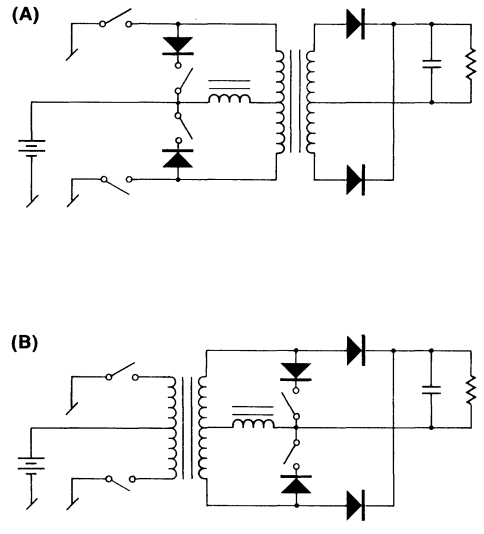


Figure 91

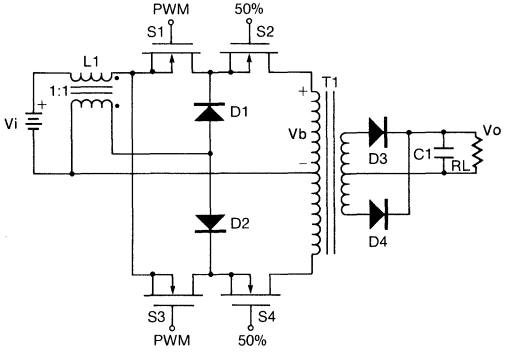


Figure 92

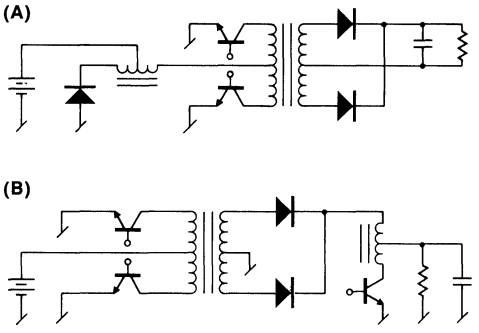


Figure 93

A few of the circuits previously shown (Figures 30C, 46A, 47, 49A, 50, 86 and 94) also return energy to the source, and it is conceivable that all these circuits can display this type of instability. In some cases, this can be prevented by limiting the stored energy, but not always.

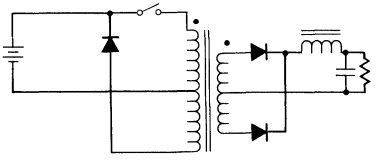


Figure 94

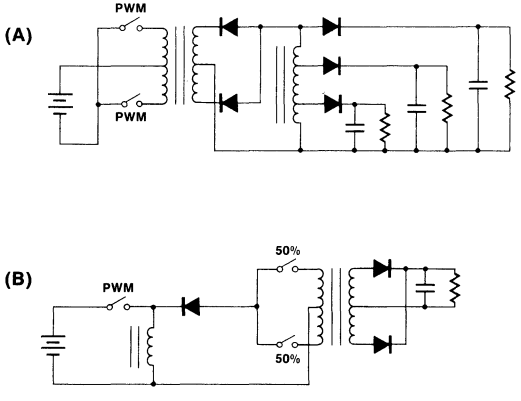


Figure 95

ACKNOWLEDGEMENT

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This bibliography is organized in a rather different manner than is usual. In addition to the normal source reference that appears as the text proceeds, there is a listing of references by figure numbers. For each figure where the author is aware of a prior source or reference, these references are given. Those figures for which no reference is given are, to the best of the author's knowledge, his original creations or are circuits in common use whose original source is obscure.

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53. L. Genult, "Switching Regulator Using Low Voltage Diodes," U.S. Patent No. 3,624,483, 30 November 1971 (Figure 86A is a transistor version of this circuit.)
54. U.S. Patent #4,121,281 in October 1978.

Figure 88C

55. M. Kohno and K. Kuwabara, "Single Ended DC-to-DC Converter with Two Individually Controlled Outputs," IEEE International Telecommunications Energy Conference Record, November 1979, pages 191-198.

Figure 90

56. F. Kadri, "Pulsewidth Modulation Derived through Control of Flux Distribution in a Dual-Core Transformer," Proceeding of the 1971 INTERMAG Conference, Denver, Colorado, April 13-16, 1971.

Figure 92

9. *Ibid* . . . Figure 12.

Figure 94

57. J. La Duca and R. Massey, "Improved Single Ended Regulated DC/DC Converter Circuit," IEEE Power Electronics Specialists Conference Record, June 1975, pages 177-187.

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58. C. VanVelthooven, "Properties of DC-to-DC Converters for Switched Mode Power Supplies," N. V. Phillips Application Note No. 472, Eindhoven, 18 March 1975.
59. S. Lindena, "The Current-Fed Inverter," 20th Annual Proceedings of the Power Sources Conference, Atlantic City, New Jersey, May 1966, pages A-23 to A-26.
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INTERSIL

A036
Using the Power MOSFET as a Switch

by Rudy Severns

MOSFET STRUCTURES

A variety of structures for implementing a power MOSFET have been proposed and fabricated. Of these, only two structures, the flat-bottomed V-groove and the vertical DMOS (double-diffused MOS) structures, are currently available as viable power switches. A cross-section view of a V-groove device is shown in Figure 1. Fabrication of an n-channel device begins with an N^- epitaxial layer grown on an N^+ substrate. P and N regions are then diffused in, a flat bottomed groove is anisotropically etched into the surface, and then an insulated gate structure is deposited. The source metalization is connected to both the N and P diffused regions, thereby effectively shorting the base and emitter of the parasitic NPN transistor. The user should, however, keep in mind the presence of this parasitic NPN transistor, which in some circumstances will participate in the circuit operation. This will be treated in later sections.

DMOS devices are very similar to V-groove (or VMOS) devices except that no groove is used and the gate structure is planar (Figure 2). Manufacturers have given the DMOS devices a variety of names, such as HEXFET, TMOS, XMOS, ZMOS, etc. These are all basically the same structure, with variations in the shape of the P diffusions and the cell interconnections.

Inherent in the MOSFET structure are voltage variable capacitances and resistances. The ON resistance is the sum of the epitaxial region resistance, the channel resistance, which is modulated by the gate-source voltage, and the lead and connection resistances. In addition there is a small but definitely non-zero resistance, r_{BE}, between the base and emitter of the parasitic transistor due to the bulk resistance of the structure.

Most MOSFETs use a form of silicon gate structure where the gate and the connection to the gate is made with doped silicon. The SiP material, while very useful in the structure, has a resistivity about 3,000 times greater than aluminum, and in some devices creates a substantial resistance in series with the gate.

Capacitance exists within the structure from the gate to the source, C_{gs}, the gate to the drain, C_{gd}, and from the drain to the source, C_{ds}. C_{ds} is essentially the capacitance of the base-emitter junction (C_{ob}) of the parasitic transistor and has the voltage-dependent characteristic typical of a PN junction. C_{gs} is relatively independent of voltage but the C_{gd} characteristic is very similar to C_{ds}.

The parasitic transistor also contributes capacitances. C_{ob} is equal to C_{ds}, since the same structure is involved. In addition, the base-emitter junction displays a typical diode junction characteristic.

P-channel MOSFETs are very similar to N-channel except that the N and P regions are interchanged. In P-channel devices the ON resistance for a given die area will be approximately twice that of a comparable N-channel device. The reason for this is that in the N-channel device the majority carriers are electrons but in the P-channel device the majority carriers are holes which have lower mobility. If the area of the P-channel device is increased to produce an equal $r_{DS(ON)}$ then the capacitance of the P-channel device will be higher and the device cost will also be greater. For this reason N-channel devices are usually preferred for power switches as long as the external circuits do not become overly complex to accommodate the N-channel device.

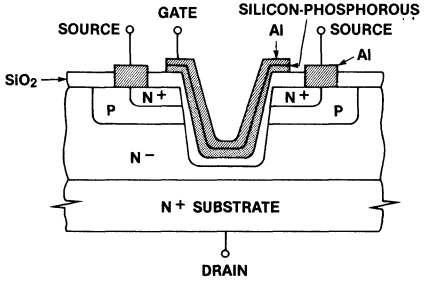


Figure 1. V-Groove MOSFET

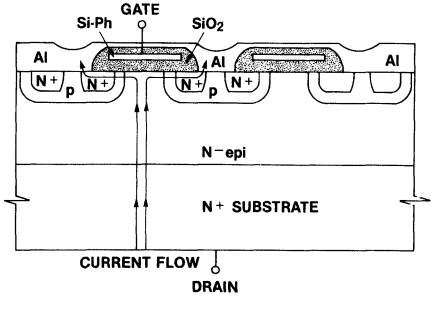


Figure 2. Vertical (DMOS) MOSFET

SWITCHING CHARACTERISTICS

One of the major advantages of the MOSFET is its ability to switch very fast. Figure 3 shows a turn-on transition for an IVN6000 switching 350 volts in 5 nanoseconds! Most of the presently available power MOSFETs are capable of switching in a few nanoseconds **if** properly driven. Except for switching times of ten nanoseconds or less, the transition times are almost completely determined by the circuit in which the device is used. This is quite different from a bipolar junction transistor, where the physics of the device limit the switching speeds and no amount of drive wizardry will significantly improve things beyond a certain point.

Capacitive Characteristics

For switching times down to about 10ns a MOSFET, from a drive point of view, is essentially a capacitor made up of C_{gs}, C_{gd} and C_{ds} as shown in Figure 4. A small signal measurement of these capacitances as a function of drain-source voltage, V_{DS}, for a typical device, is given in Figure 5. C_{gs} varies little with voltage, remaining about 210pF. C_{ds} and C_{gd} however are strong functions of voltage; C_{gd} is 400pF at 0 volts but decreases to 5pF at 350V, and C_{ds} also

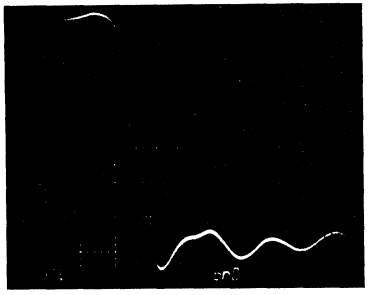


Figure 3. IVN6000 Turn-On

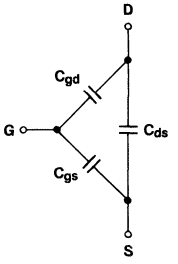


Figure 4. Capacitive Equivalent Circuit

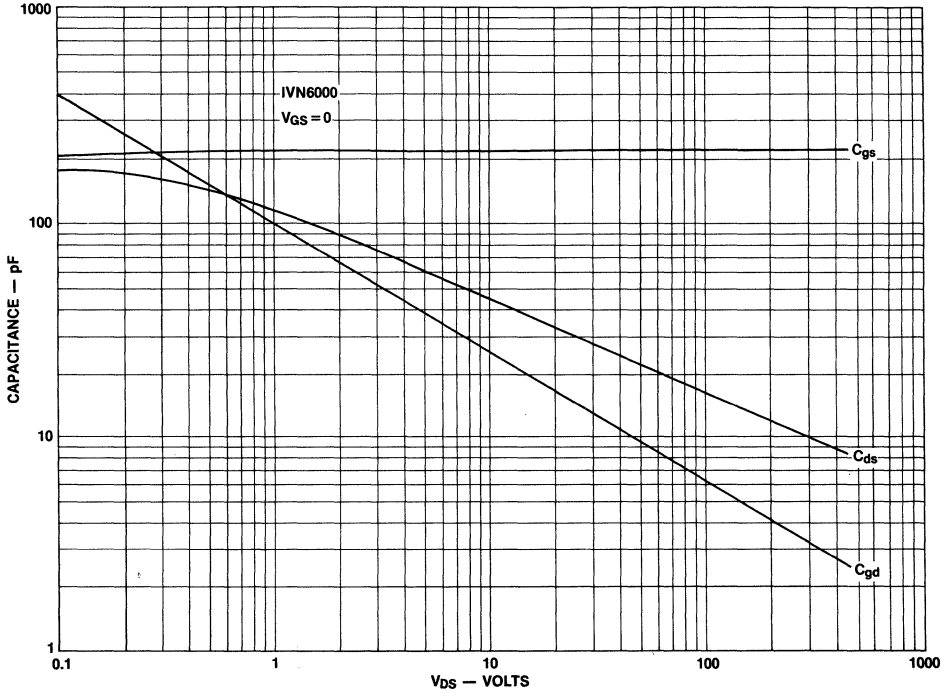


Figure 5. Capacitance Variation with Drain-Source Voltage

has a large variation. The small signal capacitance is interesting to a linear designer, but when the device is used as a switch the designer needs to know the large signal behavior. A much better way to present the data is shown in Figure 6 where the gate charge is plotted as a funtion of the gate-to-source voltage, V_{GS}, with the supply voltage, V_{DD}, as a parameter and the drain current, I_D, as a constant to represent the usual inductive load. Figure 7 shows a simplified version of the test circuit.

The curves in Figure 6 display three distinct operating regions. Region I is where V_{GS} is below the threshold voltage, V_{th}, so that the device is cut off and the capacitance is dominated by C_{gs}. For this device the small signal $C_{gs} = 210pF$, which is consistent with the Region I slope. Region II occurs as the device is turning on and represents the Miller capacitance, defined by:

$$C_m = -A_V C_{gd} \quad (1)$$

where:

$$A_V = -\frac{\Delta V_{DS}}{\Delta V_{GS}} \simeq -g_m R_L \quad (2)$$

Combining (1) and (2):

$$C_m \simeq g_m R_L C_{gd} \quad (3)$$

In the example shown in Figure 6, C_m is about 70nF. This large value occurs because of the current source in the drain lead; i.e., R_L is very large. When a lower impedance load is used in the drain, C_m will be much smaller and the slope of the Q_G/V_{GS} curves will be greater. The amount of charge required to charge C_{gd} is, however, a function of V_{DS} and not R_L or g_m, so that ΔQ_G for the Region II will increase with V_{DS}, displacing the curves to the right as shown. For a given V_{DD}, Q_G will not vary significantly with R_L. C_{gd} does vary slightly with variations in I_D and this would alter ΔQ_G with differing R_L values, but the effect is so small as to be of no practical interest in switching applications.

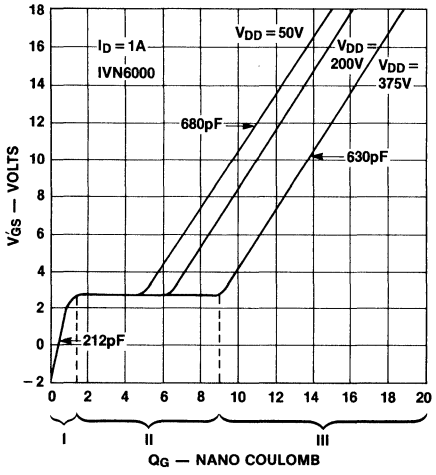


Figure 6. Gate Dynamic Characteristics

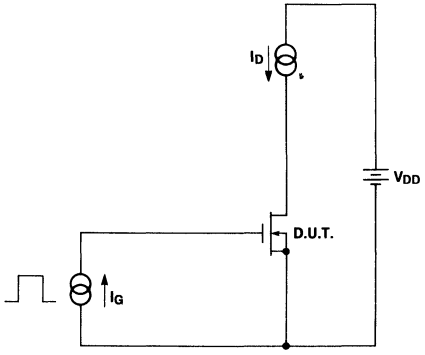


Figure 7. Simplified Test Circuit

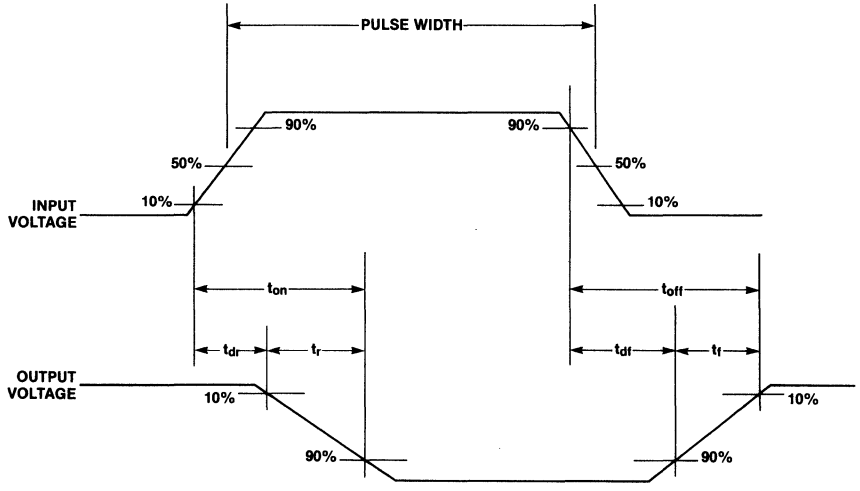


Figure 8. Switching Waveform

Region III represents operation with the device fully ON and V_{DS} near zero. Note that the capacitance in Region III is essentially the sum of C_{gs} and C_{gd} at low voltages, or about 650pF.

This set of curves can be used directly by the designer to determine both the switching time for a given drive impedance and the drive power. The drive power, P_d, for a resistive drive source and a switching frequency of f_o is

$$P_d = \Delta Q_G V_{GS} f_o \quad (4)$$

The effective input capacitance, C_{in}, for a given V_{GS}, is

$$C_{in} = \frac{\Delta Q_G}{\Delta V_{GS}} \quad (5)$$

The idealized switching waveforms are shown in Figure 8. A good approximation[1] for the switching times can be obtained from a piecewise linear approximation and a simple RC model (Figure 9) using the appropriate values for C_{in} in Regions I, II, or III. The turn-on delay, t_{dr}, represents the time required to charge C_{in} to $V_{GS} = V_{th}$, at which point the device begins to conduct. A similar delay time, t_{df}, exists at turn-off where V_{GS} must fall to the point where there is a significant increase in $r_{DS(ON)}$ before any change in the output is observed. The rise and fall times correspond to the times required to charge and discharge the Miller capacitance.

The total switching time, t_s, is defined as:

$$t_s = t_{dr} + t_r + t_{df} + t_f \quad (6)$$

If t_s is plotted as a function of the gate drive voltage for constant source resistance, curves like those shown in Figure 10 will be obtained. Thus, the designer is faced with a tradeoff. If large V_{GS} is used then t_{dr} and t_r will be short and $r_{DS(ON)}$ will be a minimum. Unfortunately, t_{df} becomes large, and t_s increases as does the drive power. If a small value of V_{GS} is used then t_{dr} and $r_{DS(ON)}$ increase rapidly. If both low $r_{DS(ON)}$ and minimum t_s are required then a value of V_{GS} that gives a satisfactory value of $r_{DS(ON)}$ must be used, and a sufficiently low value of R_S must then be selected to give the desired t_s.

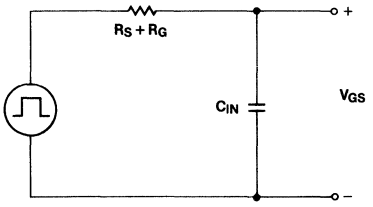


Figure 9. Simple RC Model

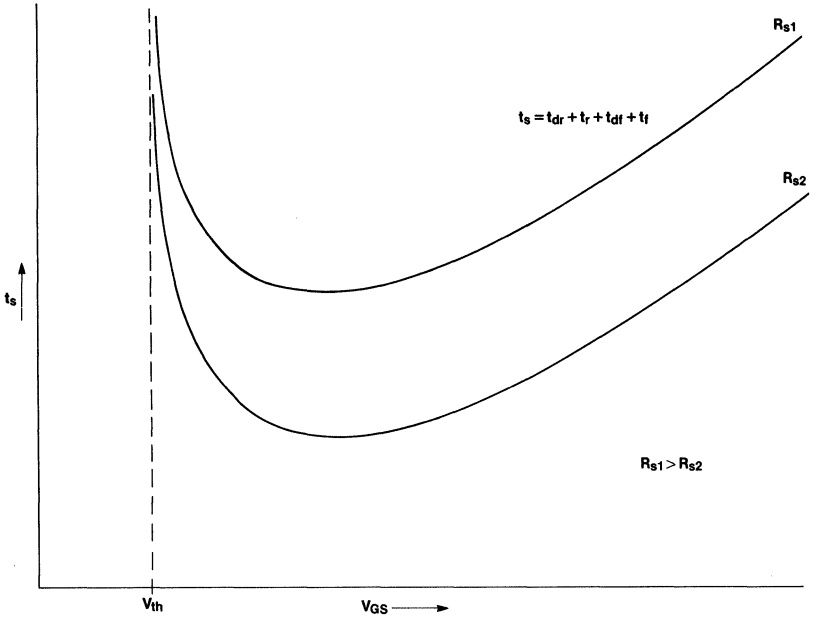


Figure 10. Total Switching Time as a Function of Gate Drive and Source Resistance

High-Speed Limitations

For very fast switching times (< 10ns) the simple RC model of Figure 9 is no longer adequate. The gate resistance, R_G, and the package inductances, L_S, L_G, and L_D, must be included, especially in large devices as shown in Figure 11. It is the parasitic inductances and gate resistances that limit the achievable switching speeds. For an IVN6000 device the minimum turn-on time is about 4ns.

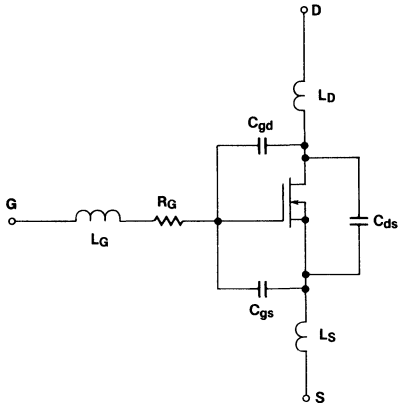
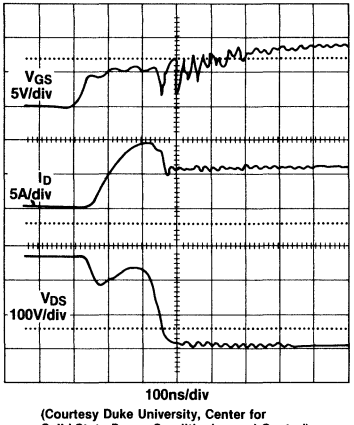


Figure 11. Equivalent Circuit Including Package Inductance and Gate Resistance

It has been shown[2] that inductance which is common to both the load and drive circuit, such as the source lead inductance or the wiring inductance, can produce a turn-on plateau in V_{DS} like that shown in Figure 12. The voltage, V_{SL}, across the common inductance, L_S, is:

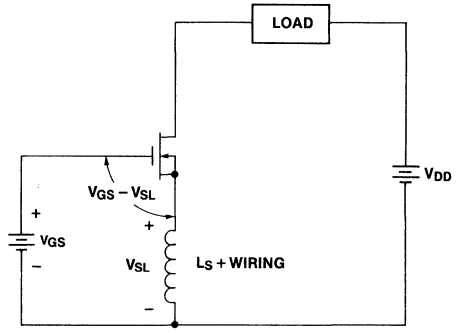
$$V_{SL} = L_S \left(\frac{dI_D}{dt} + \frac{dI_G}{dt} \right) \quad (7)$$



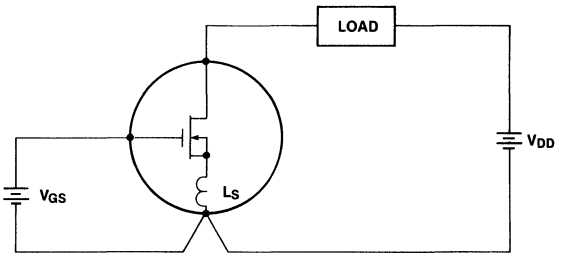
(Courtesy Duke University, Center for Solid-State Power Conditioning and Control)

Figure 12. Turn-On V_{DS} Plateau Due to L_S

This voltage subtracts from V_{GS} during the turn-on as shown in Figure 13A, restricting the gate enhancement. This effect can greatly increase the switching power loss because of the delayed fall of V_{DS} during turn-on. The problem can be minimized by separating the drive and load current loops right up to the device case as shown in Figure 13B. A TO-3 package will have an L_S of 1 to 10nH depending on the bonding wire size and the number of bond wires. Except for very high-speed or high-current applications this is not usually a problem, but even a small length of common external wiring can greatly increase the effective L_S and create a problem.



(A)



(B)

Figure 13

The drain-source capacitance, C_{ds}, can cause asymmetrical transition time between turn-on and turn-off even if the gate drive is perfectly symmetrical. At turn-on C_{ds} is discharged through $r_{DS(ON)}$ and the time constant is very short. At turn-off however the rate of voltage rise on C_{ds} is determined by the load, not by the switch. For a clamped inductive load with a large I_D at turn-off, C_{ds} will be charged quickly and there will be little difference between the gate and drain switching times, but if a resistive load is present the voltage across C_{ds} will have an exponential characteristic, with the load resistance determining the RC time constant. Even though the channel is turned off quickly V_{DS} may change slowly.

As shown in Figure 14, C_{gd} can cause pulse distortion during turn-on. During the interval when $V_{GS} < V_{th}$ (t_{dr}) the device is essentially a capacitor comprised of $C_{gd} + C_{gs}$, and the positive edge of V_{GS} is coupled to the output producing the initial positive pulse shown. A similar negative pulse can occur during the turn-off delay time.

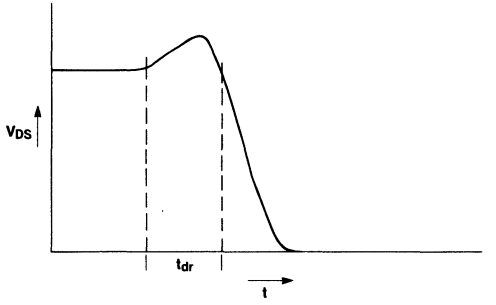


Figure 14. Turn-On Overshoot Due to C_{gd} and t_{dr}

Drive Circuits

An ideal gate drive circuit for a MOSFET should provide a current waveform like that in Figure 15. At turn-on a fast rising current pulse is applied with an amplitude sufficient for the desired rise time. When the desired value of V_{GS} is reached, I_G is reduced to the small value required to maintain V_{GS}. A typical MOSFET will have a gate current of less

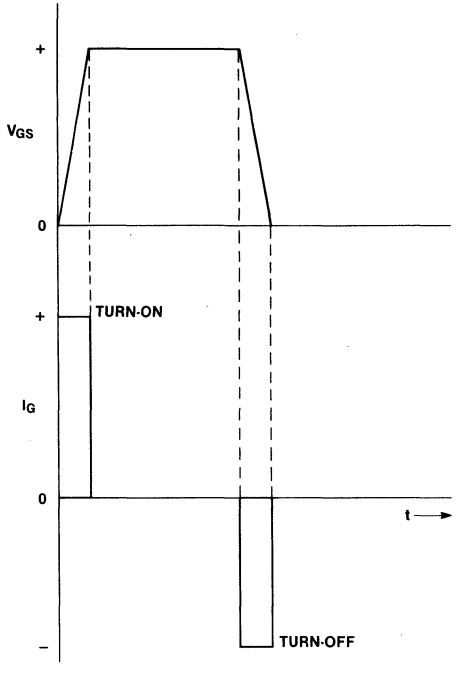
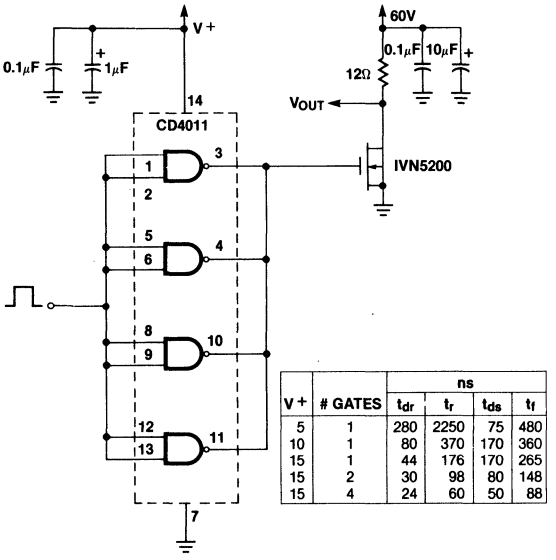
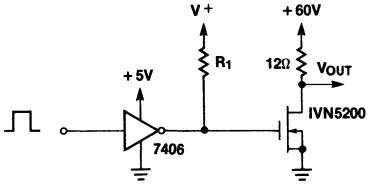


Figure 15. Ideal Gate Drive Waveforms



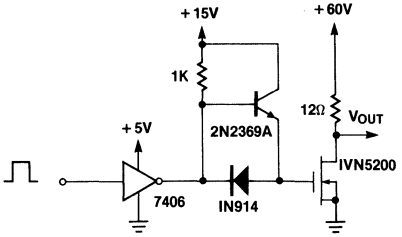
V+	# GATES	ns			
		t_{dr}	t_r	t_{ds}	t_f
5	1	280	2250	75	480
10	1	80	370	170	360
15	1	44	176	170	265
15	2	30	98	80	148
15	4	24	60	50	88

(A)



V+	R_1	ns			
		t_{dr}	t_r	t_{df}	t_f
15	390Ω	40	200	72	120
15	750Ω	40	340	70	110
30	750Ω	40	150	70	116
30	1.5K	66	290	64	100

(B)



t_{dr}	t_r	t_{df}	t_f
30ns	60ns	76ns	110ns

(C)

Figure 16. CMOS and TTL MOSFET Gate Drive Circuits

than 1nA but there may be other shunt elements (transformer magnetizing current, for example) in the gate circuit that require steady-state current. At turn-off a negative pulse is applied until V_{GS} is zero. As will be demonstrated shortly in the dV_{DS}/dt discussion, it is imperative that during the off time the gate-to-source impedance be as small as possible.

A close approximation to the ideal waveforms can be achieved with a variety of circuits. The simplest drive scheme is to use either CMOS or TTL buffers or gates as shown in Figure 16. These drive schemes are very attractive because of their simplicity, but the switching times are relatively slow due to the buffer output limitations. If greater speed is needed some form of low impedance bidirectional driver is needed; several such circuits are given in Figures 17 and 18. The DS0026 (Figure 17B) driver is particularly useful. This IC was designed as a NMOS clock driver to drive capacitive loads. There are two buffers in each package, each capable of sourcing or sinking 1.5 amperes with a switching time of 20ns. The DS0026 can be driven from TTL or CMOS logic. If the output from the DS0026 is not adequate, the output can be buffered with MOSFETs as shown in Figure 18A to provide much higher currents with no loss of speed. Figure 18B shows another driver that does not use a DS0026. If the two separate power supplies required in Figures 18A and 18B are not available, then the bootstrap versions in Figure 18C and 18D can be used.

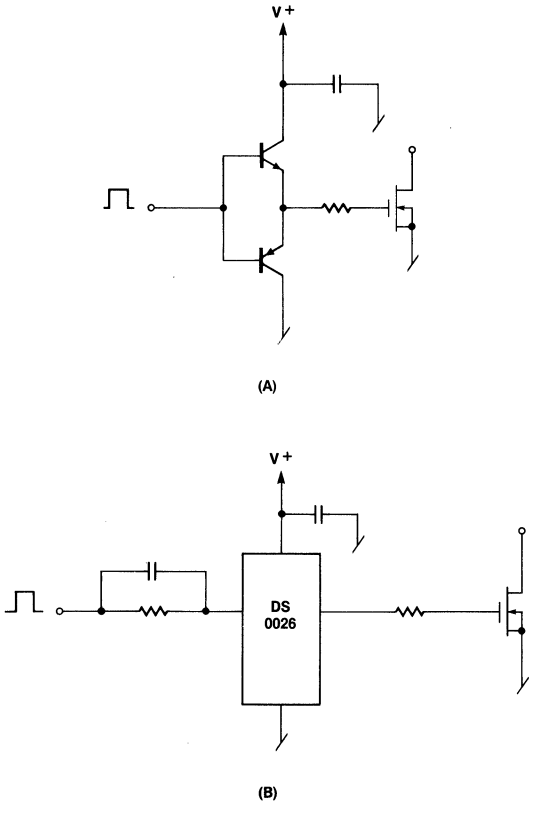


Figure 17. Bi-Directional MOSFET Gate Drive Circuits

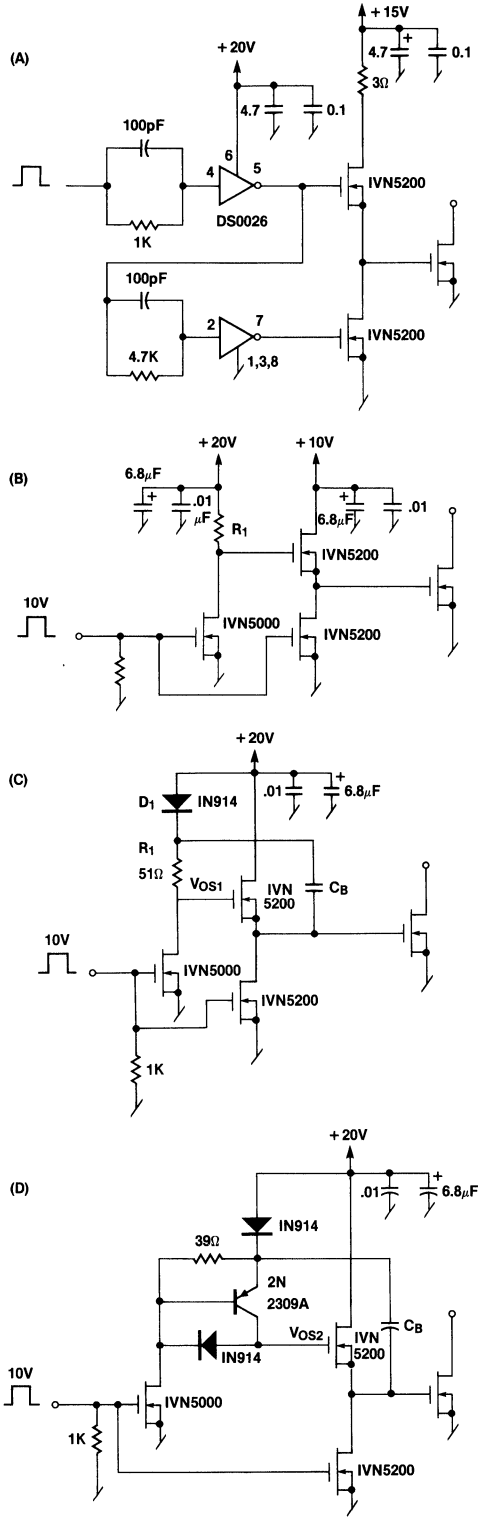
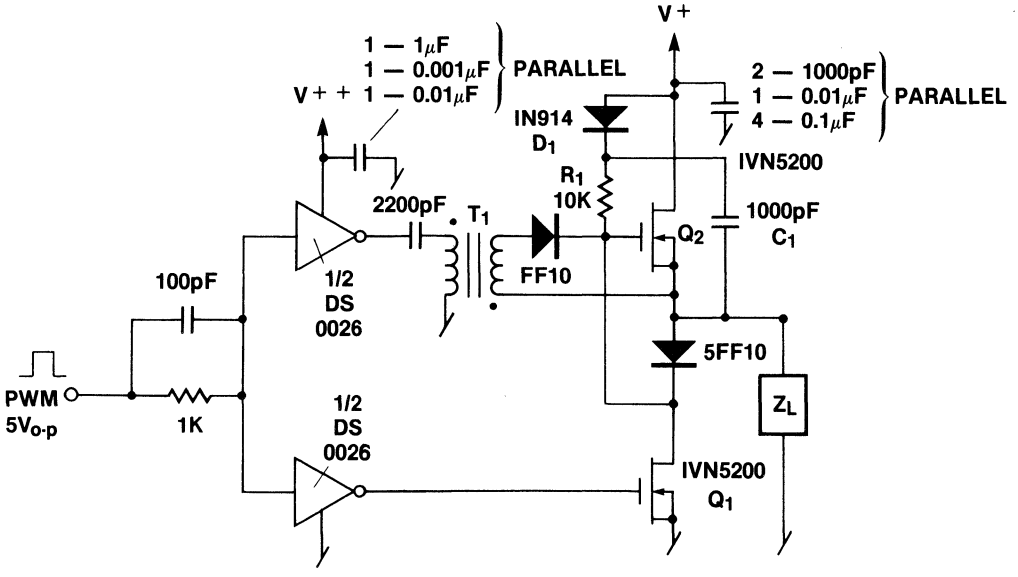


Figure 18. Bi-Directional Gate Drive Circuits

In applications which use a very large MOSFET or a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge quickly. Figure 19 shows a circuit which works very well with large-capacitance loads. When the input to the driver is zero, Q_1 is held in conduction by ½ of the DS0026. Q_2 is clamped off by Q_1. When a positive input occurs, Q_1 is turned off and a current pulse is applied to the gate of Q_2 by the other half of the DS0026 through T_1. After about 20ns, T_1 saturates and Q_2 is held on by its own C_{gs} and the bootstrap circuit made up of C_1, D_1 and R_1. For pulses less than 50μs the bootstrap circuit may not be needed as the input capacitance of Q_2 discharges very slowly. At the end of the positive input pulse, Q_1 turns on shutting off Q_2.



T_1 — is three turns 30 bifilar on a ferrite bead.

PERFORMANCE SUMMARY

Z_L	V+	V++	ns			
			t_{dr}	t_r	t_{df}	t_f
5Ω & 1000pF	20	15	22.5	7	15	7
4700pF	20	15	22.5	15	16	15.5
5Ω	20	15	23	11	14	4.5
5Ω	50	20	22	18	14	4
100′ RG223/U Terminated in 51Ω	20	15	20.5*	19	13*	6.5

*Measured at input to cable.

Figure 19. Very High Speed Driver

The power driver circuit in Figure 19 can be modified to provide a direct coupled drive for a buck regulator as shown in Figure 20. Again the bootstrap portion of the circuit may not be needed when the switching frequency is above 10kHz.

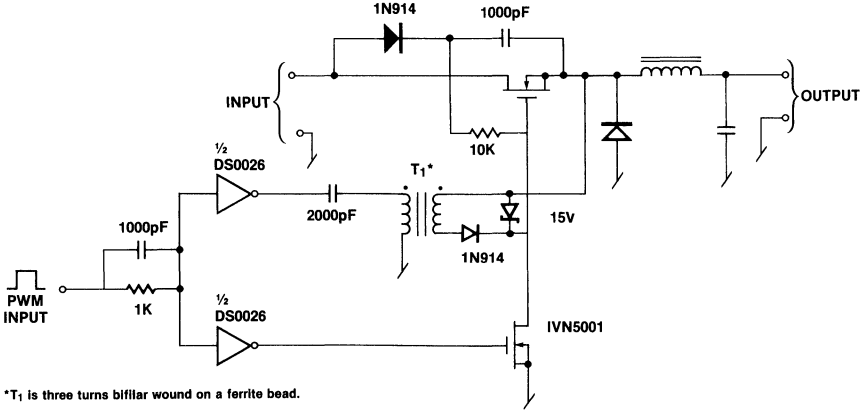


Figure 20. Gate Drive Scheme for MOSFET Buck Regulator

It is possible to use inductive energy storage schemes to drive MOSFETs; two possibilities are given in Figure 21. Energy is stored in L_1 during the OFF time of Q_2 and then discharged into the gate of Q_2 during conduction. The major disadvantage of these drive schemes is that the discharge current through the zener clamps must be maintained during the entire ON time of Q_2. This may greatly increase the drive power required.

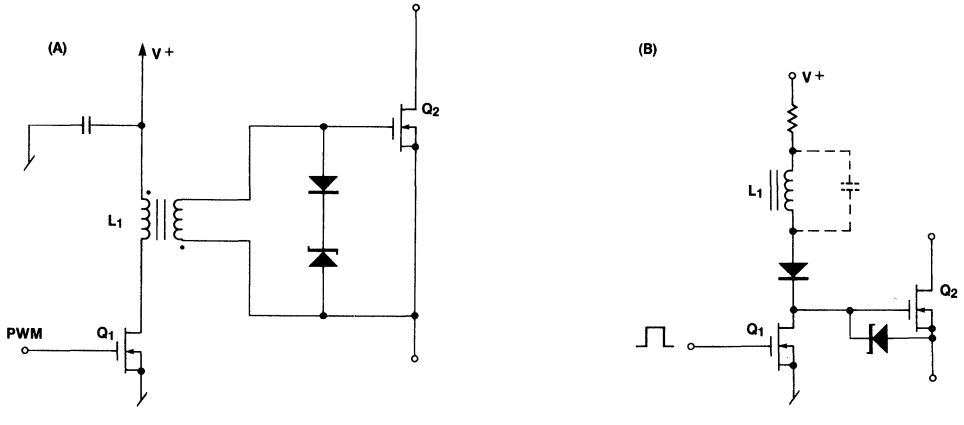


Figure 21. MOSFET Drive Circuits Using Stored Energy

Many applications require transformer isolation between the switches and the driver circuitry; Figure 22A shows a very simple means to accomplish this. Unfortunately this simple circuit has a major problem. As shown in Figure 22B, the transformer winding volt-seconds product must average zero. This means that the gate enhancement voltage will vary with duty cycle, being greater at low duty cycles. If a wide range of duty cycles must be accommodated the switch will be over-driven at low duty cycles and under-driven at high duty cycles. As was shown earlier, this can lead to large variations in the total switching time. However, for those applications where only a moderate variation in duty cycle is required this simple circuit can work very well.

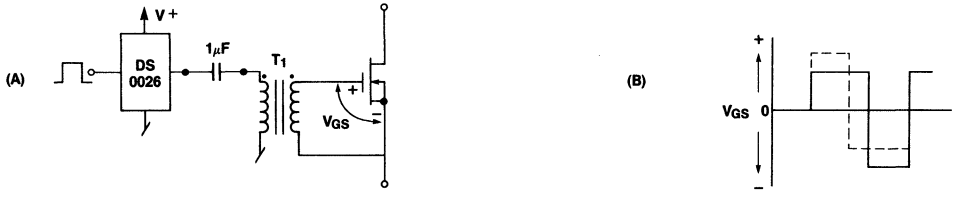


Figure 22. Transformer Coupled MOSFET Drive Ciruit

There are transformer-coupled drive circuits where V_{GS} does not vary with duty cycle. A circuit that can be used in symmetrical converters is shown in Figure 23A. In the initial state S_3 and S_4 are closed and S_1 and S_2 are open. The voltage across T_1 is zero and Q_1 and Q_2 are off. S_4 is then opened and S_2 closed, applying a voltage, V_S, to the primary of T_1 with the dot positive. V_{GS} for Q_1 is positive and for Q_2 negative, turning on Q_1. At the end of the conduction interval of Q_1, S_2 is opened, S_4 is closed, and the circuit reverts to the initial state with Q_1 and Q_2 off. S_3 is then opened and S_1 closed, so that V_S is applied to the primary of T_1 with the dot negative. This turns on Q_2 and holds Q_1 off. At the end of the conduction interval of Q_2, S_1 is opened and S_3 closed and the circuit reverts to the initial state. The transformer sees only a symmetrical AC waveform and V_{GS} is fixed by V_S and the turns ratio of T_1 independent of duty cycle.

C_1 is added to the circuit to prevent a DC component from appearing across the primary of T_1 due to lack of symmetry in the drive switching times. The value of C_1 is determined by the magnetizing current of T_1. C_1 should be large enough that the voltage rise across it, due to the magnetizing current during ½ cycle, is small compared to V_S.

A practical implementation of the circuit in Figure 23A is given in Figure 23B. The switching function is provided by a pair of DS0026 clock driver ICs driven at TTL levels from a push-pull pulse width modulator. For low-power applications only a single DS0026 may be needed (there are two drivers in each package), while for high-power applications the DS0026's may not be able to supply sufficient drive current by themselves.

The DS0026's can be replaced by a pair of drivers like those in Figure 19 to supply almost unlimited drive power by proper selection of the output devices. For bridge converter circuits, two more isolated windings can be added to T_1.

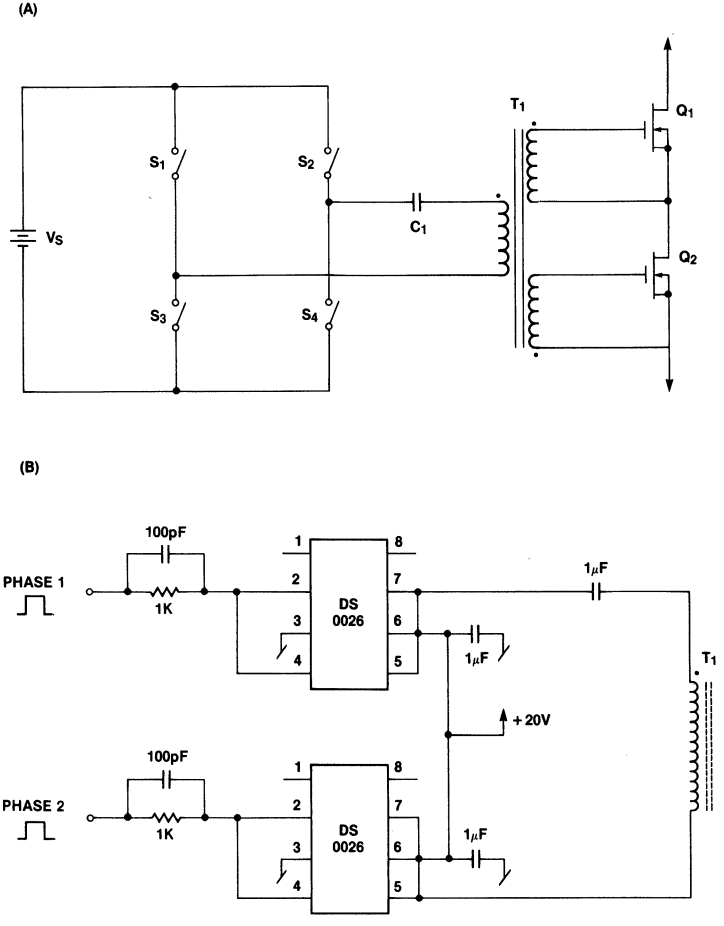


Figure 23. Symmetrical Transformer Coupled Drive Circuit

Figure 24A shows a transformer coupled circuit that will provide constant V_{GS} in asymmetrical converters. This circuit is a variation of the feed-forward converter. At the beginning of the positive input pulse, Q_1 turns on driving Q_2 into conduction. At the end of the input pulse, Q_1 turns off. The voltages across the transformer windings reverse, shutting off Q_2, and the energy stored in the core is discharged through D_1 into the source. While very simple, the circuit has two drawbacks. First, the energy stored in the core is a function of the duty cycle. The turn-off current for Q_2 is the magnetizing current for T_1, which is a function of duty cycle. The second problem occurs if the current in D_1 goes to zero during the off time of Q_2. This leaves the gate connected to winding N_3, which may well have sufficient impedance to cause dV_{DS}/dt triggering problems. By adding Q_3[3], as shown in Figure 24B, from gate to source of Q_2, these problems can be overcome. At turn-off, Q_3 is driven on by the energy in T_1 clamping the gate of Q_2. Even after all the energy in T_1 is discharged, Q_3 still presents a relatively low impedance at the gate of Q_2.

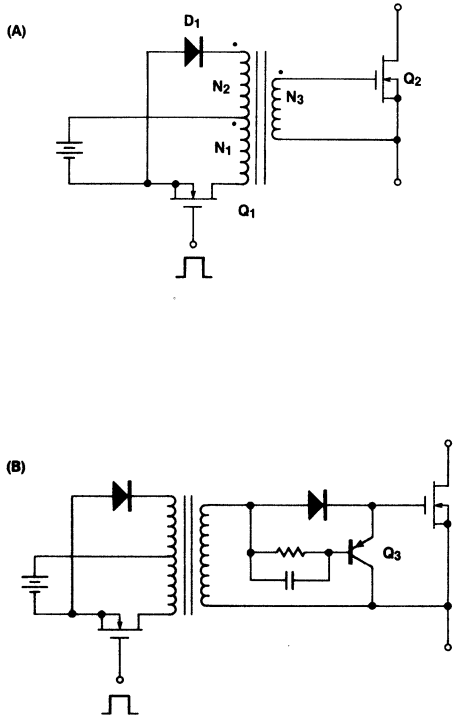


Figure 24

There are many other possible variations of both primary and secondary arrangements, and a few of these are summarized in Figure 25.

There is a basic limitation to the maximum duty cycle of single-transformer drive circuits. Over the period of one cycle the winding volt-second product must average zero. During the switch ON time the winding voltage is determined by the required enhancement voltage, V_{GS}. During the OFF time V_{GS} is limited by the breakdown voltage, BV_{GS}, of the gate. The maximum duty cycle is:

$$D_{MAX} = \frac{BV_{GS}}{BV_{GS} + V_{GS}} \quad (8)$$

Exactly the same problem exists in a bipolar junction transistor. However, when using a BJT, it is possible to use a diode in series with the emitter to arbitrarily increase BV_{BER} at the expense of increased voltage drop during conduction. This trick does not work with MOSFETs, since the leakage current of the diode will be much larger than the leakage of the MOSFET gate and all the reverse voltage still appears across the gate.

Another disadvantage of single-transformer circuits is that the transformer must be able to support V_{GS} during the entire ON time of the switch. Given the typical enhancement voltage of 10 to 20 volts this makes the transformer relatively large.

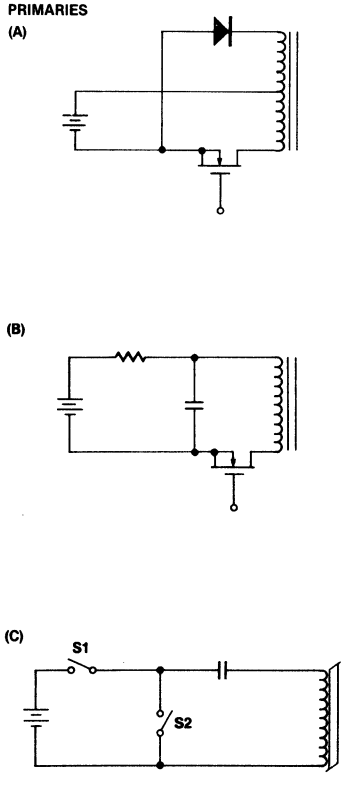


Figure 25. Primaries
Secondaries on next page

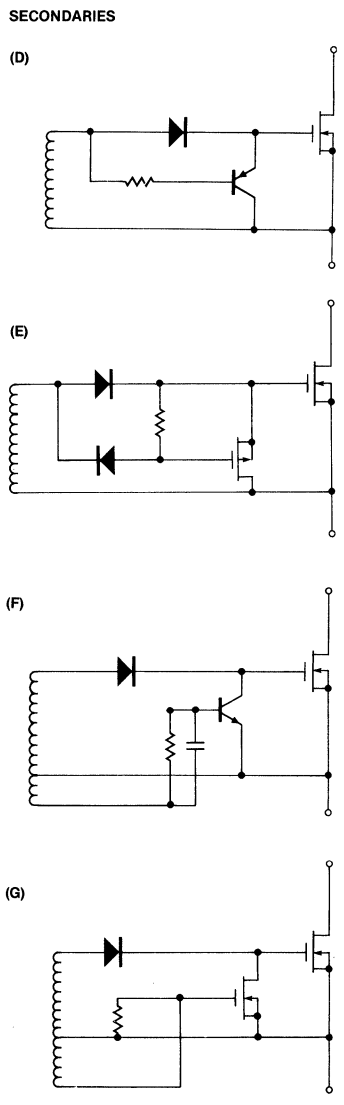


Figure 25. Secondaries

One means to get around these limitations is to use some form of pulse drive[4] where the switch input capacitance is charged at turn-on and holds V_{GS} positive until a negative pulse discharges it at turn-off. Such a circuit is shown in Figure 26. At the beginning of the cycle, a short pulse is applied to the gate of Q_1, which in turn injects a current pulse into the gate of Q_4 turning it on. Q_4 remains on due to the stored charge in the gate until a turn-off pulse is applied to Q_2. This turns on Q_3, which discharges the gate of Q_4 and turns it off. Despite the relative complexity, the circuit has several advantages. T_1 and T_2 can be designed to have very low leakage inductance, which makes fast transitions in Q_4 possible. There is no inherent limitation on duty cycle, and Q_4 may be kept on continuously by periodically pulsing Q_1 to replenish the charge in the gate of Q_4. The main disadvantage of this circuit, other than its complexity, is the high gate impedance during the off period, determined by R_1. To prevent V_{GS} from sagging significantly during the ON period, R_1 must be relatively large. If this drive scheme is used in a circuit that subjects Q_4 to a positive drain-source voltage transition during the off period, Q_4 may be triggered into conduction.

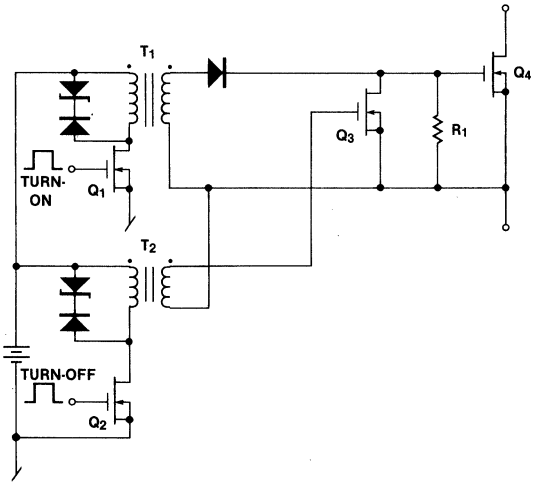


Figure 26. Pulsed Gate Drive Circuit

CONDUCTION CHARACTERISTICS

In addition to the switching characteristics, the ON state conduction characteristics are of primary concern to the designer. For practical purposes the MOSFET can be regarded as a voltage (V_{GS}) controlled resistance. The ON resistance of the MOSFET is made up of two components: the voltage-controlled channel resistance and the fixed resistance due to the drain epitaxial region, the source area bulk resistance, the die surface metalization and the package bond wires. In a low-voltage (<100V) device the channel resistance is usually larger than the fixed resistances. In a high-voltage device, however, the ON resistance is dominated by the resistance of the epitaxial drain region when the device is fully enhanced. Figure 27 shows the variation of $r_{DS(ON)}$ with V'_{GS} ($V'_{GS} = V_{GS} - V_{th}$) and I_D for a 450V two-ampere MOSFET (IVN6000 KNT). Note that $r_{DS(ON)}$ increases with I_D. The change in $r_{DS(ON)}$ is very abrupt as V_{GS} is increased.

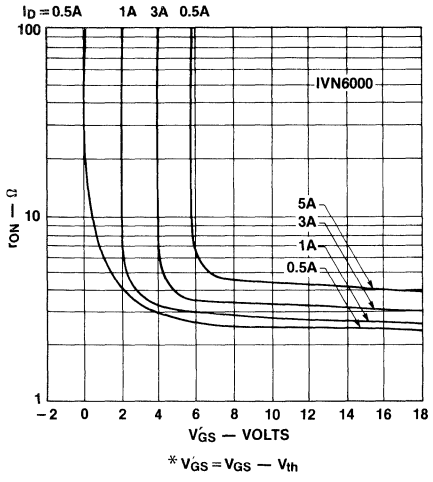


Figure 27. Variation of r_{ON} with V_{GS} and I_D

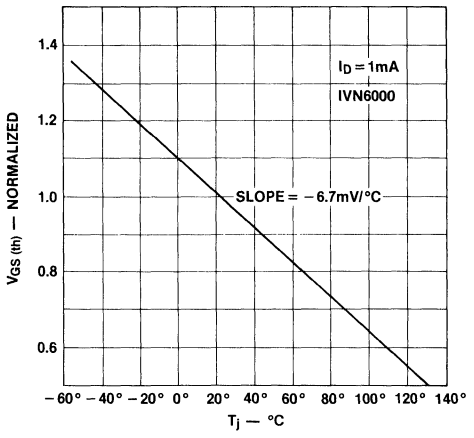


Figure 29. Variation of Threshold Voltage with Temperature

$r_{DS(ON)}$ is also a function of temperature, as shown in Figure 28. For $V'_{GS} > 3$ volts, the normal region for power switch operation, the temperature coefficient is positive. This is one of the major advantages of the MOSFET over the bipolar, and accounts for the absence of lateral thermal instability induced second breakdown and the ease with which multiple devices may be paralleled. Below $V_{GS} = 3V$, $r_{DS(ON)}$ begins to display a negative temperature coefficient. This is due to the temperature coefficient of V_{th} as shown in Figure 29. For this particular device the temperature coefficient of V_{th} is about −6.7 mV/°C. For V_{GS} values near V_{th}, $r_{DS(ON)}$ is dominated by the channel resistance, which in turn is a strong function of V_{th}. For switching applications, this region is normally traversed very quickly during turn-on or turn-off and the negative temperature coefficient region is not a problem. Figures 30 and 31 show the normalized value of $r_{DS(ON)}$ as a function of temperature for a high-voltage (Figure 30) and a low-voltage (Figure 31) MOSFET. In the high-voltage device the temperature coefficient of $r_{DS(ON)}$ is 0.7 to 0.9%/°C. Because of the relatively greater contribution of the channel resistance to $r_{DS(ON)}$ in the low-voltage device, the variation of V_{th} with temperature reduces the temperature coefficient of $r_{DS(ON)}$ to 0.2 to 0.5%/°C. A very rapid means for determining the maximum value of I_D for a given V_{DS} and V'_{GS} is to use the curves given in Figure 32.

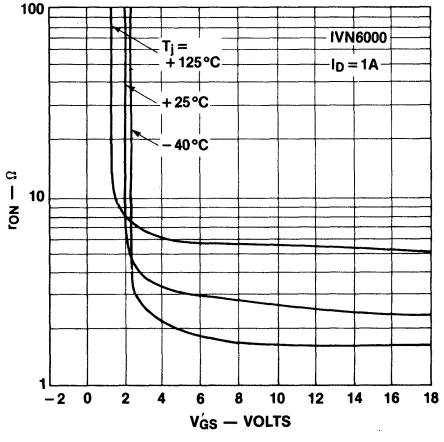


Figure 28. Variation of r_{ON} with Temperature

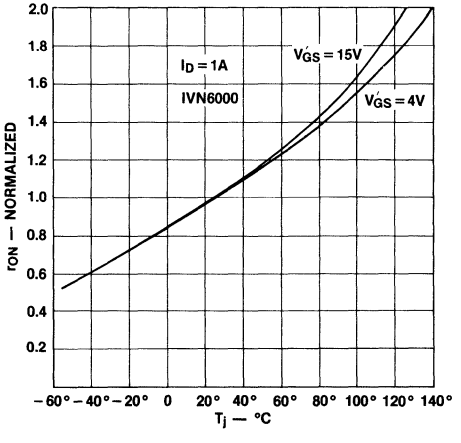


Figure 30. Variation of ON Resistance with Temperature for High-Voltage Power MOS

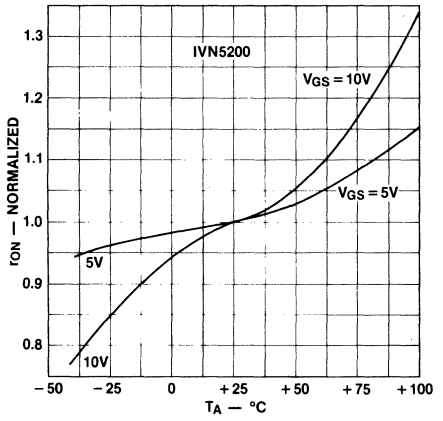


Figure 31. ON Resistance Variation with Temperature for Low-Voltage Power MOS

For a given structure and voltage rating, the ON resistance of a MOSFET is an inverse function of the die area. If half the ON resistance is desired the die area must be doubled.

For a given structure and die area, $r_{DS(ON)}$ increases very rapidly with breakdown voltage. The relationship is:

$$r_{DS(ON)} \propto BV_{DS}^{2.5\text{-}2.7} \quad (9)$$

The result is that a high-voltage, low-$r_{DS(ON)}$ device requires a large die.

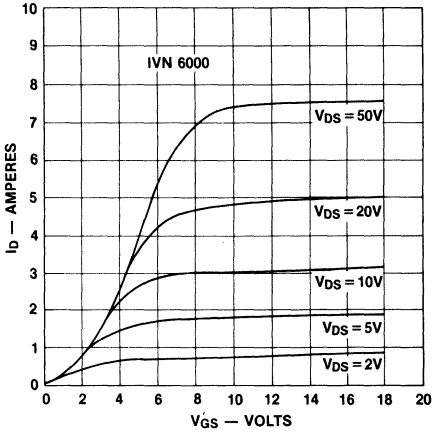


Figure 32. Large Signal Transfer Characteristic

The cost of a MOSFET is a strong function of the die area. If a large die area is used to reduce the ON resistance, the number of dice per wafer will decrease; additional dice are lost due to inherent wafer defects and the increased scrap zone around the wafer center and periphery. The yield (Y) can be represented by a variety of equations, all of them exponentially decreasing in some manner. A typical equation is:

$$Y = k(n)\frac{(1\text{-}e^{AD})^2}{AD} \quad (10)$$

where A is the die area, D is the defect density, n is the number of process steps and k is a factor that varies inversely with n, usually exponentially. The result is a rapid decrease in yield as the die area is increased. For small devices (<0.050" x 0.050") the yield is usually very high and the die cost low, but as the die dimensions begin to exceed 0.100" x 0.100" the yield drops and the cost per die increases rapidly. Many power FETs are larger than those dimensions. For example, a one-ohm 450-volt die may cost four to six times as much as a 2.5-ohm die with the same breakdown rating.

For small dice (<100 mil) the package cost is greater than the die cost and so the final device cost is relatively constant but as the die cost exceeds the package cost the total device cost becomes exponential with die area. This is shown qualitatively in Figure 33.

The $r_{DS(ON)}$ given in the data sheets is usually for a junction temperature of 25°C and the designer must calculate the actual value of $r_{DS(ON)}$ for the particular application. The actual $r_{DS(ON)}$ is:

$$r_{DS(ON)} = r_{DS(ON)}\left(1 + \frac{\alpha}{100}\right)^{T_j\text{-}25\,^\circ C} \quad (11)$$

where $r_{DS(ON)}$ is the resistance for $T_j = 25\,^\circ C$ at the design I_D and V_{GS} and α is the averaged temperature coefficient of the ON resistance at the design T_j.

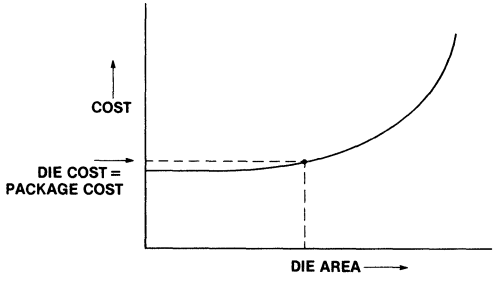


Figure 33. Die Area versus Device Cost

BV_{DS} Variation with Temperature

The breakdown voltage (BV_{DS}) for a MOSFET is a function of temperature as shown in Figure 34. At high temperatures BV_{DS} is above the data sheet values, but at low temperatures it can be significantly lower. For those applications where the switch is exposed to a low temperature soak and

then turned ON, this should be taken into account even though most devices supplied by the manufacturer will have breakdowns well above the data sheet values.

Note that the MOSFET is not unique in displaying a lower breakdown voltage at lower temperature. BJTs also show this effect.

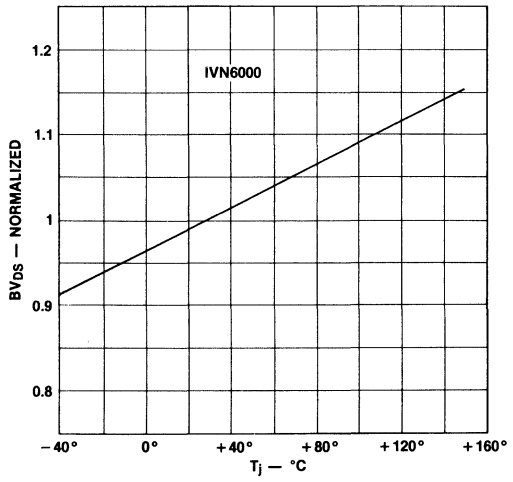


Figure 34. Breakdown Voltage Variation with Temperature

A portion of the drive power, P_T, is dissipated in the internal gate resistance, R_G, and the remainder is dissipated in the drive circuit resistance, R_S. (If resonant charging is used most of the gate drive power may be recovered in the driver.) The gate dissipation, P_G, is:

$$P_G = P_T\left(\frac{R_G}{R_G + R_S}\right) \quad (16)$$

R_G is typically in the range of 1 to 10 ohm. Except in very high frequency switching applications (>100kHz) the drive power is insignificant compared to the other losses and is usually ignored.

Even when $V_{GS} = 0$, some current, I_{DSS}, will flow from drain to source. As shown in Figure 35, I_{DSS} is very small at room temperature but increases exponentially as the T_j is increased. The power loss due to leakage is:

$$P_L = V_{DS}\, I_{DSS}\,(1\text{-}D) \quad (17)$$

where V_{DS} is the drain source voltage during the OFF time, I_{DSS} is at the highest expected T_j, and D is the switch duty cycle. Since initially T_j is known only approximately, the value for P_L is only approximate. Normally, however, P_L is only a small part of the total loss so that the error is not usually significant.

In those applications where the MOSFET sees a substantially constant V_{DS} the power dissipation decreases with increasing T_j because of the positive temperature coefficient of $r_{DS(ON)}$, but this is not the typical switching application. More often the drain load is effectively a current source. In this mode of operation the power dissipation **increases** as T_j increases, providing a positive feedback mechanism that further increases T_j. Usually, however, for junction temperatures below 150°C, the gain coefficient of the positive feedback is less than one, so that a stable equilibrium point is reached. At higher temperatures (>150°C) it is possible to have no stable equilibrium point and the device can go into thermal runaway.

POWER LOSS AND JUNCTION TEMPERATURE CALCULATION

In a practical design situation the designer needs to know the total power dissipation and the junction temperature. The total power dissipation, P_d, is the sum of the switch loss, P_S, the conduction loss, P_C, some fraction of the gate drive power, P_G, and the leakage loss, P_L, due to I_{DSS} during the off time of the switch. The conduction loss is:

$$P_C = I^2_{D(RMS)}\, R_{ON} = I^2_{D(RMS)}\, r_{DS(ON)}\left(1 + \frac{\alpha}{100}\right)^{T_j\text{-}25\,°C} \quad (12)$$

The switching loss depends on the switching time and the nature of the drain load. The power loss due to a switching transition is:

$$P_S = f_S \int_0^{\tau} V_{DS}(t)\, I_D(t)\, dt \quad (13)$$

where f_S is the switching frequency and τ is the sum of the voltage and current transition times. Normally an exact solution is not required and the following approximations are usually adequate:

$$\text{for a resistive load, } P_S = \left(\frac{V_{DSMAX} \cdot I_{DMAX}}{6}\right)\tau f_S \quad (14)$$

$$\text{and for an inductive load, } P_S = \left(\frac{V_{DSMAX} \cdot I_{DMAX}}{2}\right)\tau f_S \quad (15)$$

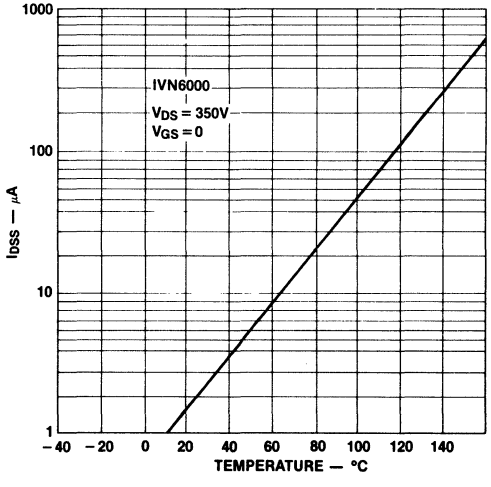


Figure 35. Drain-Source Leakage Current versus Temperature

To determine the junction temperature the following equations must be solved:

$$P_D = I^2_{D(RMS)}\, r_{DS(ON)} \left(1 + \frac{\alpha}{100}\right)^{T_j - 25\,^\circ C} + P_S + P_L \qquad (18)$$

$$T_j = T_A + R_{th(J\text{-}A)}\, P_D \qquad (19)$$

Although equation (18) is transcendental and an exact analytical solution is not possible, a variety of solution methods are still possible. A most practical solution has been suggested by Gyma, Hyde and Schwartz[4] using a quadratic approximation for equation (12) which gives an answer accurate to a few percent. Equation (18) now takes the form:

$$P_D = I^2_{D(RMS)}\, r_{DS(ON)} (a_0 + a_1 T_j + a_2 T_j^2) + P_S + P_L \qquad (20)$$

If equations (19) and (20) are combined:

$$A T_j^2 + B T_j + C = 0 \qquad (21)$$

where:

$$A = a_2 R_{th(j\text{-}A)} I^2_{D(RMS)}\, r_{DS(ON)} \qquad (22)$$

$$B = a_1 R_{th(j\text{-}A)} I^2_{D(RMS)}\, r_{DS(ON)} - 1 \qquad (23)$$

$$C = T_A + R_{th(j\text{-}A)} (P_S + P_L) + a_0 R_{th(j\text{-}A)} I^2_{D(RMA)}\, r_{DS(ON)} \qquad (24)$$

The following values for the coefficients a_0, a_1 and a_2 have been suggested:[4]

$$a_0 = 0.8650,\ a_1 = 4.443,\ \text{and}\ a_2 = 3.822 \times 10^{-5}$$

From equation (18):

$$T_j = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \qquad (25)$$

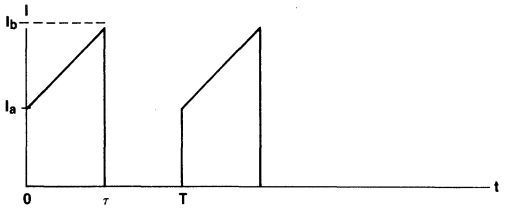
It has been shown[4] that the lesser of the two possible solutions is the correct choice. If the solution for T_j is complex the operating conditions being considered will produce thermal runaway. If a more accurate solution for T_j is required then some form of iterative solution using a computer can be used.

Once the junction temperature has been determined then the total power dissipation can be calculated using equation (19).

Minimizing $I_{D(RMS)}$

The dominant term in the power loss is normally P_C. The designer can minimize the amplitude of $I_{D(RMS)}$ for a given power level by an appropriate choice of topology and by controlling the current waveshape.

In a switch mode converter, the current waveforms through the inductors, transformer windings, rectifiers and switches will appear as shown in Figure 36, ranging from a triangle to a rectangle depending on the value of the averaging inductor and the load. For the capacitors, the waveforms will be similar, except that there will be no DC component (see Figure 37). The RMS and average values of the waveform are given in the figures.



General Case

$I_{AVG} = D\left(\frac{I_a + I_b}{2}\right)$

$I_{RMS} = \left[\frac{D}{3}\left(I_a^2 + I_a I_b + I_b^2\right)\right]^{1/2}$

$\Delta = \frac{\tau}{T}$

Special Cases

1) $D = 1$

$I_{AVG} = \frac{I_a + I_b}{2}$

$I_{RMS} = \left(\frac{I_a^2 + I_a I_b + I_b^2}{3}\right)^{1/2}$

2) $I_a = I_b$

$I_{AVG} = I_a D$

$I_{RMS} = I_a\sqrt{D}$

3) $I_a = 0$

$I_{AVG} = \frac{I_b D}{2}$

$I_{RMS} = I_b\sqrt{\frac{D}{3}}$

Figure 36. Average and RMS Values for Trapezoidal Waveforms

It can be shown that:

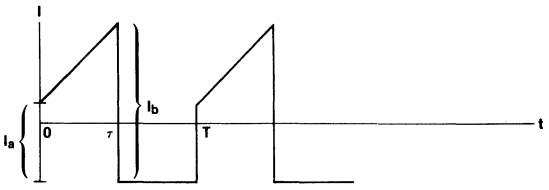
$$K \equiv \frac{I_a}{I_b} = f(L/L_C) \qquad (26)$$

where, L = inductance of the averaging choke
L_C = is the critical inductance for a particular input voltage and load power

As L is increased, K goes from 0 (triangle) to 1 (rectangle). Substituting $K = I_a/I_b$ for the continuous choke current case:

$$I_{RMS} = \frac{I_{AVG}}{\sqrt{D}} \sqrt{\frac{K^2 + K + 1}{3\,(K+1)^2}} \qquad (27)$$

For constant I_{AVG} and D, the normalized ($I_{RMS} = 1$ for $K = 1$) I_{RMS} is as shown in Figure 38. This curve shows the I^2R losses for triangular waveforms are 32% higher than for rectangular waveforms. It is also apparent that for $I_a/I_b > 0.6$, the additional losses incurred by having $L < \infty$ is only 2%, so from a practical point of view L need only be about twice L_C. Increasing the value of I_a/I_b increases the switch turn-on losses but decreases the turn-off losses. Since the turn-off losses usually dominate, increasing I_a/I_b reduces the switching loss also.



General Case

$$I_{RMS} = \left\{ D \left[\frac{I_a^2 + I_a I_b + I_b^2}{3} - \frac{D}{4}(I_a + I_b)^2 \right] \right\}^{1/2}$$

$$D = \frac{\tau}{T}$$

Special Cases

1) $D = 1$

$$I_{RMS} = \frac{I_b - I_a}{\sqrt{12}}$$

2) $I_a = I_b$

$$I_{RMS} = I_a\sqrt{D - D^2}$$

3) $I_a = 0$

$$I_{RMS} = I_b\sqrt{\frac{D}{3} - \frac{D^2}{4}}$$

Figure 37. RMS Value of AC Component of Trapezoidal Waveforms

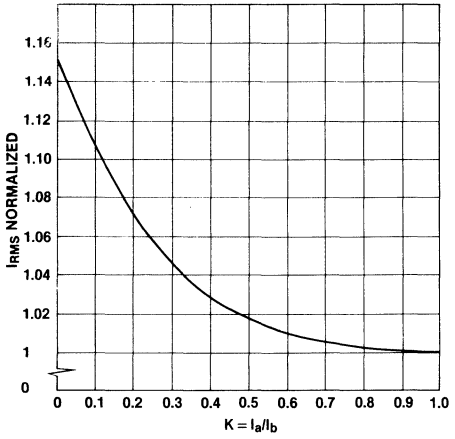


Figure 38. Variation of I_{RMS} with Trapezoidal Current Ratio

For the case of discontinuous inductor current ($L < L_C$), $I_a/I_b = 0$ and is no longer relevant since the waveforms are now triangular. For a given I_{AVG} the RMS current is:

$$I_{RMS} = \frac{I_{AVG}}{\sqrt{3D}} \quad (28)$$

A plot of equation (28) is given in Figure 39, where I_{AVG} is constant and I_{RMS} is normalized for $D = 1$. Obviously triangular current waveforms with high peak currents and low duty cycles are to be avoided if low losses are desired.

For the case where:

$I_a = I_b$:

$$I_{RMS} = \frac{I_{AVG}}{\sqrt{D}} \quad (29)$$

the curve in Figure 39 also applies.

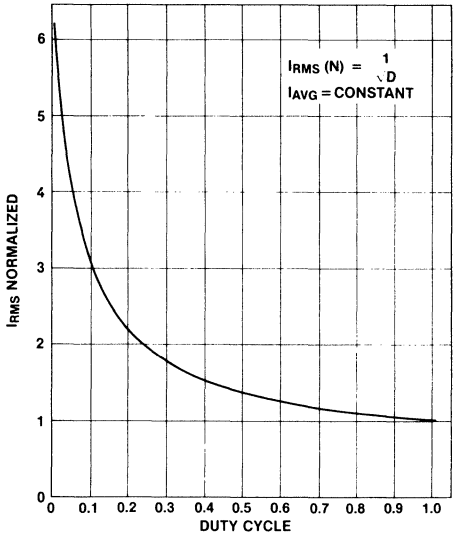
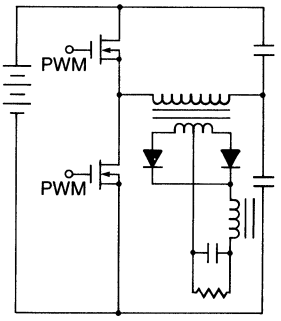


Figure 39. Variation of RMS Current with Duty Cycle for Triangular or Rectangular Current Waveforms

The topology selected can have a profound effect on the conduction losses. A simple example is shown in Figure 40. Figure 40A is a normal half-bridge quasi-squarewave converter, while 40B is an unmodulated half-bridge preceded by a boost regulator. Given the conditions in Table I, the power losses for (B) are much lower than (A). Because the cost of power MOSFETs is a strong function of $1/r_{DS}$, the three devices used in (B) may be much cheaper than the two devices in (A). While this is a fairly simple example, the boost derived family of converters generally provides lower MOSFET conduction losses than the buck derived converters. Figures 41A and 41B show two examples of boost derived converters, one using overlapping conduction and the other a secondary shunt switch. There are many other possible circuits that may be used. Unfortunately, the boost family of converters has disadvantages also:

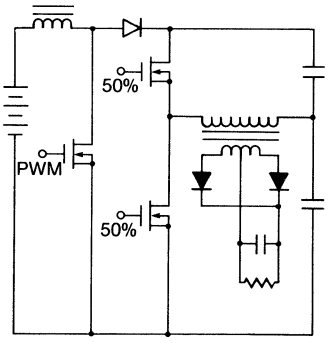
1. The control loop transfer function contains a right half-plane zero which is difficult to compensate for with single-loop feedback. By using multiple AC and DC loops, this problem can be overcome.
2. The output ripple current in a boost converter is discontinuous (the input current is continuous) so that the output ripple current is large.



Half-Bridge

Low Line, P_T = 35.8W
High Line, P_T = 12.9W
T_j = 122°C

(A)



Boost Regulator/Half-Bridge

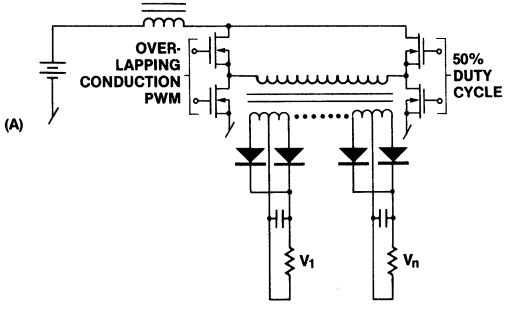
Low Line, P_T = 9.1W
High Line, P_T = 6.5W
T_j = 63°C

(B)

Figure 40. Topology Trade-Off

Table I. Power MOS Topology Conduction Loss Comparison Assumptions

1. P_O	= 200W
2. η	= 80% Without Switch Losses
3. V_{DC}	= 200V to 375V
4. T_A	= 50°C
5. r_{DS}	= 2.5Ω at 25°C
6. Filter Inductor is Large	
7. BV_{DSS}	= 450V to 500V
8. θJ_A	= 4°C/W (TO-3 Case and Heak Sink)
9. r_{DS} Temperature Coefficient is 0.6%/°C	



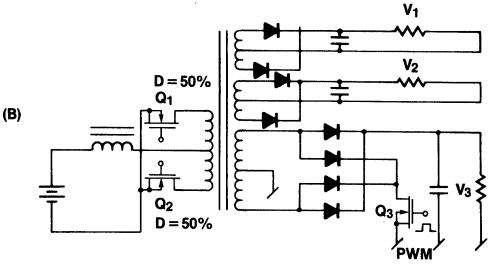


Figure 41. Boost Derived Power Converters

3. In those converters using overlapping conduction in the primary, a large voltage spike can be generated due to the interruption in the primary to secondary leakage inductance current. When the shunt switch is in the secondary, this spiking is greatly reduced.

Despite these drawbacks the significantly lower power losses of the boost family of converters make them very attractive for converters using MOSFET switches.

When compared to bipolar transistors, the MOSFET conduction losses for a given die area are always greater; the transistor's drive power and switching losses are greater than the MOSFET's. Figure 42 shows a comparison between transistors and MOSFETs of the total switch loss as a function of the switching frequency. The value of the crossover frequency, f_o, is a matter of some debate but lies in the region of 10 to 30kHz for devices of similar die area.

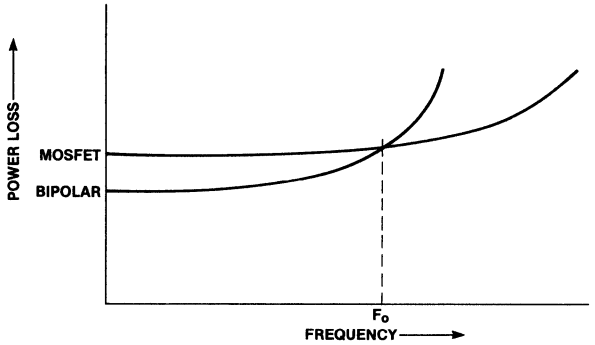


Figure 42. Comparison of BJT and MOSFET Losses
Note: F_o = 10 to 30kHz

SAFE OPERATING AREA

To achieve satisfactory service life from any power semiconductor, the circuit designer must assure that the device is operated within the voltage, current and thermal capabilities inherent in the particular device. To assist the designer, the manufacturer provides a table of maximum ratings, a safe operating area curve (SOAR) and a transient thermal impedance curve.

A typical absolute maximum ratings table is reproduced in Table II. While the information in the table is useful, it is not sufficient by itself for a power device. To adequately define safe operating conditions it is necessary to use the SOAR curve, like that reproduced in Figure 43. For a power MOSFET, the SOAR curve will have three boundary regions. Region I is defined by the breakdown voltage capability of the device. Region II is defined by the thermal capability of the device. Normally a maximum junction temperature of 150°C is specified, so that in Region II the power dissipation is limited by a peak junction temperature of 150°C. This results in Region II being defined by a family of curves that allows higher peak power for shorter pulse widths.

Region III is defined by the current capability of the device. The current capability of a given device may be limited by the bond wire diameter, the area of the bonding pad on the die, or by the metalization on the die surface. Whereas the breakdown voltage and junction temperature limitations can be readily determined by direct measurement, the current limitations are empirically derived from life testing. The maximum current is limited to a value which has been found to give an acceptable service life. In a bipolar transistor, the rapidly decreasing h_{FE} at high currents effectively discourages operation in excess of the current ratings. In a MOSFET, however, the gain is not reduced at high currents, and there may be a temptation, in fast pulse applications where a high drain-source voltage drop may be acceptable, to operate with very short high current pulses in excess of the ratings. Even if the device dissipation is very low, this is inadvisable for two reasons. First, the reliabilty or service life of the device is undefined and likely to be shortened, and second, if the current density in the device is increased sufficiently, it is possible to reach the level where current injected avalanche breakdown occurs, possibly destroying the device.

For a bipolar transistor the SOAR curves will have a fourth boundary. This region is defined by the thermally-induced second breakdown characteristic. In a bipolar device there are several ways to induce secondary breakdown. The first is thermal, where the negative temperature coefficient of V_{BE} causes localized hot spots to be formed. When the temperature of a hot spot is sufficiently high, its impedance is drastically reduced, funneling the collector current through a small area, usually destroying the device. Another mechanism for inducing secondary breakdown is via avalanche breakdown. If the collector voltage is raised to the breakdown point of the collector-base junction and a significant current allowed to flow, the device will go into secondary breakdown. It has been widely advertised that MOSFETs do not exhibit secondary breakdown. This is not true. It is generally accepted that at normal junction temperatures, the thermally-induced secondary breakdown phenomenon so prevalent in bipolar devices is not present in

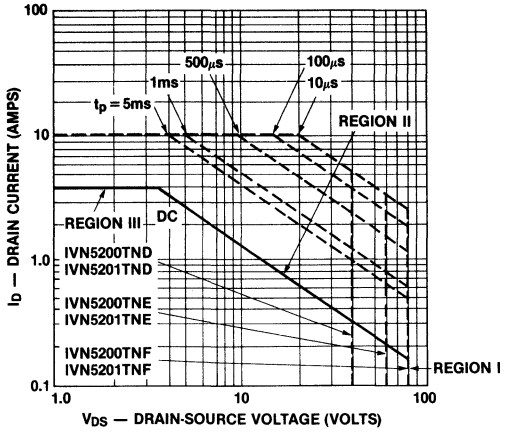


Figure 43. Typical SOAR Curves

Table II. Absolute Maximum Ratings (25 °C unless otherwise noted)

Drain-source Voltage	
IVN5200TND, IVN5201TND	40V
IVN5200TNE, IVN5201TNE	60V
IVN5200TNF, IVN5201TNF	80V
Drain-gate Voltage	
IVN5200TND, IVN5201TND	40V
IVN5200TNE, IVN5201TNE	60V
IVN5200TNF, IVN5201TNF	80V
Continuous Drain Current (see note 1)	4.0A
Peak Drain Current (see note 2)	10A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	−30V
Thermal Resistance, Junction to Case	10 °C/W
Continuous Device Dissipation at (or below)	
25 °C Case Temperature	12.5W
Linear Derating Factor	100mW/ °C
Operating Junction	
Temperature Range	−55 °C to +150 °C
Storage Temperature Range	−55 °C to +150 °C
Lead Temperature	
(1/16 in. from case for 10 sec.)	+300 °C

Note 1. T_C = 25 °C; controlled by typical $R_{DS(ON)}$ and maximum power dissipation.

Note 2. Pulse width 80μs, duty cycle 1.0%.

MOSFETs; the avalanche-induced secondary breakdown, however, is. This is not surprising; as shown in the earlier discussion, the MOSFET structure has within it an NPN transistor, and the voltage limit on the device is the base-collector junction breakdown voltage. The breakdown voltage is equivalent to BV_{CEX} in a bipolar.

The current level at which primary breakdown becomes secondary breakdown is a function of the base emitter resistance, the temperature and the h_{FE} of the bipolar device. In a MOSFET, the base and emitter are shorted right on the die, and for reasons of improving the dV_{DS}/dt characteristic, the resistance is made as low as possible. In addition, the h_{FE} of the MOSFET parasitic bipolar is much lower than a typical bipolar device. The result is that the current level at which primary breakdown becomes secondary breakdown is much higher in a MOSFET than it is in a comparable bipolar transistor. The device ratings are selected so that the maximum V_{DS} is well below the actual breakdown point in production devices.

Current-injected avalanche breakdown, present in bipolars during reversed bias operation, can also lead to secondary breakdown in the presently available types of MOSFETs. For a given field gradient within the semiconductor there is a maximum current density threshold above which self-sustaining avalanche breakdown can occur. This is a basic limitation on the current-handling capability of a power device. In present MOSFETs the internal current densities are limited by design, so that the junction temperature thermal limit is reached well before any current-injected avalanching is present. Both of these breakdown modes lie well outside of the published SOAR curves and neither is of direct interest to the device user. Due to the absence of thermally-induced second breakdown, the SOAR for a MOSFET is greatly expanded over that of a comparable bipolar.

The normal manufacturers' SOAR curve is given for a case temperature of 25 °C and either DC or a single pulse. In the real world of case temperatures above 25 °C and repetitive pulses, the designer must modify the standard SOAR curves for his particular application. This can be done by using the transient thermal impedance $Z_{(th)}$ curves which are generally made available by the manufacturer.[7]

dV/dt LIMITATIONS AND MOSFET POWER SWITCHES

Most designers are well aware of the dV/dt limitations of SCRs which, if exceeded, can cause these devices to turn on in the absence of a normal trigger pulse. However, it is not generally appreciated that a similar, and in some cases equally detrimental, phenomenon can appear in both bipolar transistors and MOSFET power switches.

Waveforms Responsible for Spurious Turn-On

Turn-on due to dV/dt can occur in any power circuit that subjects the power switch to a positive dV/dt during the normal operating cycle. A very common circuit application where this occurs regularly is the pulse width modulated switching regulator. An example of a half-bridge circuit is shown in Figure 44 along with the collector (or drain) voltage and current waveforms in Figure 45. The normal operating conditions are shown in Figure 45A. Q_1 turns on at t_0 and off at t_1. Q_2 turns on at t_2 and off at t_3 where a negative current spike flows through Q_1 and D_1 due to the transformer leakage inductance. Normally most, but not all, of the reverse current at t_3 will flow through D_1. From Figure 45A it is evident that

Q_1 is subjected to a positive dV/dt during the operating cycle when the switch is in one of two states: at t_1, Q_1 has been conducting in the forward direction and at t_2, Q_1 is quiescent.

In some applications, such as resonant inverters, motor drivers or synthesized sine wave inverters, waveforms similar to those in Figure 45B can occur. The significant feature of this mode of operation is the **reverse** conduction of Q_1 and D_1 just prior to the application of a positive dV/dt on the collector. This is a third state in which the device may see a positive collector transition. Any or all of these states can occur in a very wide variety of power switching applications.

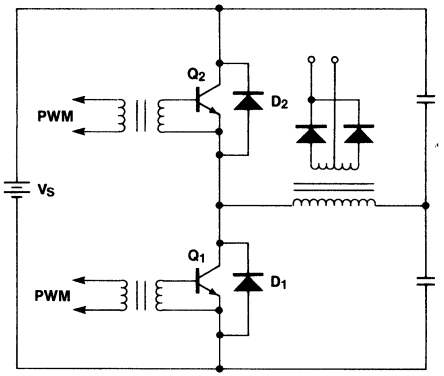


Figure 44. Typical Switching Regulator Circuit

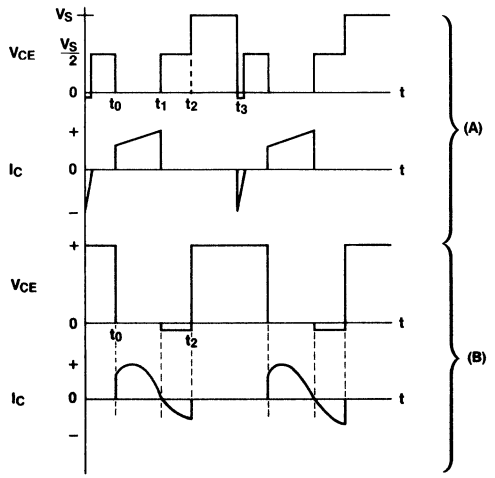


Figure 45. Q_1 Voltage and Current Waveforms

Mechanisms Responsible for Spurious Turn-On

Figure 46 shows equivalent circuits in which the effect of C_{ob}, C_{ie} and R_{BE} for the transistor and C_{gd}, C_{gs} and R_{gs} for the MOSFET are taken into account and separated from the basic device.

If a positive voltage ramp, V_{DS}, is applied to the drain of the MOSFET a current, I_1, will flow through the C_{gd}, C_{gs} and R_{gs} resulting in a positive value of V_{gs}. If I_1 is large enough V_{gs} will exceed the threshold voltage, V_{th}, of the MOSFET and it will turn on until V_{gs} drops below V_{th}. An identical effect is present in the bipolar device which will turn on if V_{BE} exceeds 0.6 to 0.7 volts.

The amplitude of I_1 is determined by the values for the capacitors, input resistances, E_1 and t_1.

The values for the capacitors depend on the type of device (bipolar or MOSFET), the design of the device, V_{DS} **and** the state of conduction immediately prior to the application of the ramp. The input resistances (R_{gs} and R_{BE}) are in part inherent in the devices and partly determined by the external circuit impedance. The threshold voltages (V_{th} or V_{BE}) are temperature variable and in the case of the MOSFET, V_{th} is a device design variable. Transistor h_{FE} also varies with temperture. E_1 and t_1 are of course determined by the external circuit.

Despite this apparent complexity, analytical solutions for V_{gs} or V_{BE} during the ramp can be derived which are of practical use.

General Model

For the purposes of calculating the voltage at the gate or base, the equivalent circuit shown in Figure 47 can be used with the appropriate component values. The ramp function is provided by the combination of a positive unit ramp starting at $t=0$ and a negative unit ramp at $t=t_1$. The slope of the ramp, dV/dt, is:

$$\frac{dV}{dt} = \frac{E_i}{t_1} \tag{30}$$

The output voltage, $E_O(S)$, can be shown to be:

$$E_O(S) = \left(\frac{E_i}{t_1}\right)\left(\frac{C_1}{C_1+C_2}\right)\left\{\left[\frac{1}{S(S+1/R\,(C_1+C_2))}\right] - \left[\frac{e^{-t_1 S}}{S(S+1/R\,(C_1+C_2))}\right]\right\} \tag{31}$$

By applying the following inverse Laplace transformations to equation 31:

$$\frac{1}{S(S+\alpha))} \xrightarrow{\pounds^{-1}} \frac{1}{\alpha}(1-e^{-\alpha t}) \tag{32}$$

$$F(S)e^{-t_1 S} \xrightarrow{\pounds^{-1}} F(t-t_1) \tag{33}$$

The time domain response for $e_O(t)$ can be obtained as:

for $t \leq t_1$

$$e_O(t) = \left(\frac{E_i\,R\,C_1}{t_1}\right)\left[1-e^{-t/R(C_1+C_2)}\right] \tag{34}$$

and for $t \geq t_1$

$$e_O(t) = \left(\frac{E_1}{t_1}\right)(R\,C_1)\left(e^{-t/R(C_1+C_2)}\right)\left(e^{t_1/R(C_1+C_2)}\right) \tag{35}$$

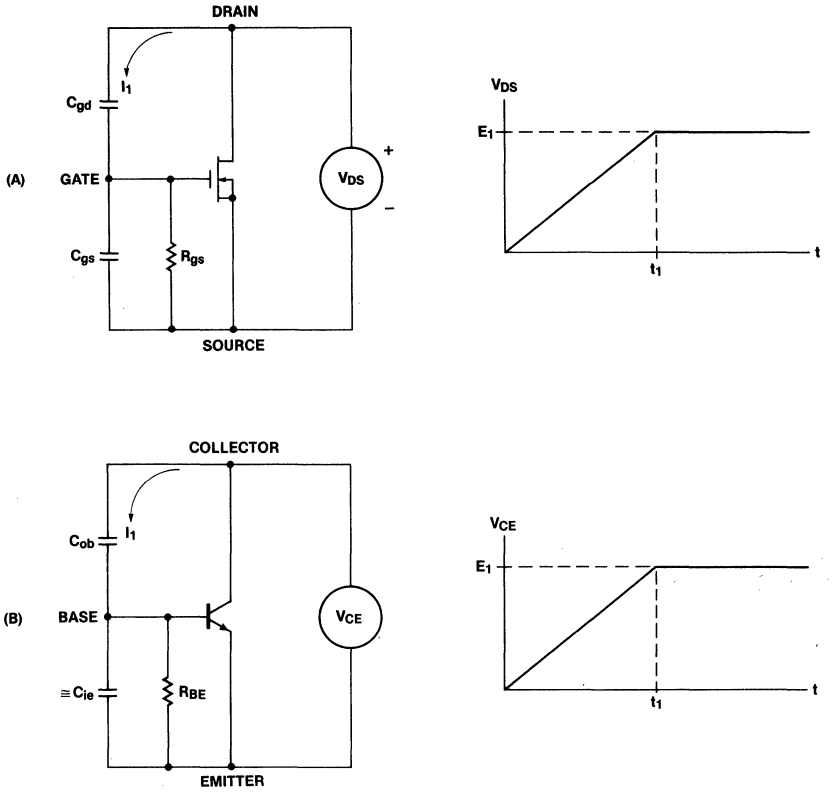


Figure 46. MOSFET and BJT Equivalent Circuits

The waveform represented by equations (34) and (35) is shown in Figure 48. For practical purposes, the only feature of the waveform that is of interest is the peak value of e_O, e_{PK}. The designer needs to know if e_{PK} is sufficiently large to turn on his device. By combining equations (30) and (34) and setting $t = t_1$, the expression for e_{PK} becomes:

$$e_{PK} = \left(\frac{dV}{dt}\right)(\tau_1)\left[1 - e^{-}\left(\frac{E_i}{dV/dt}\right)\left(\frac{1}{\tau_2}\right)\right] \quad (36)$$

where: $\tau_1 = R\,C_1$ (37)

$\tau_2 = R(C_1 + C_2)$ (38)

Example

For a MOSFET where $C_1 = 50pF$, $C_2 = 150pF$, $V_{DS} = 50V$, $dV/dt = 25V/ns$ and $R = 1\Omega$:

$$e_{PK} = (2.5 \times 10^{10})\ (2)\ (5 \times 10^{-11})\left[1 - e^{-}\left(\frac{50}{2.5 \times 10^{10}}\right)\left(\frac{1}{2(2 \times 10^{10})}\right)\right]$$

$e_{PK} = 2.48$ volts

To avoid turn-on under these conditions this device must have $V_{th} \geq 2.5$ volts.

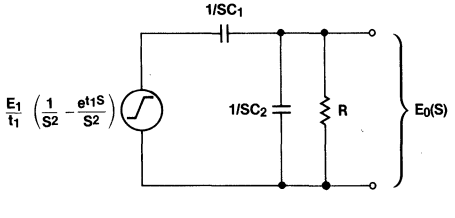


Figure 47. Equivalent Circuit

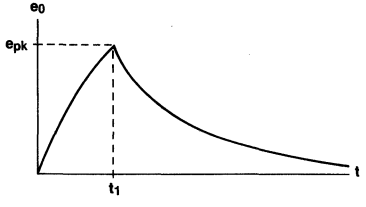


Figure 48. V_{GS} or V_{BE} Waveform

How to Determine the Appropriate Values for C_1 and C_2

As has been already mentioned, the values for C_1 and C_2 depend on the type of device selected and the design of the specific device. Once a specific device has been selected, the values for C_1 and C_2 will be dependent on the potentials applied to the device. The typical capacitance values for a high-voltage MOSFET were shown in Figure 5. While C_{gs} is relatively constant with variations in V_{DS}, C_{gd} is obviously not. It is possible to substitute the value of C_{gs} for C_2 and a relatively simple analytical expression for C_{gd}, for C_1 into equation (36) to determine e_{PK} but this would be somewhat clumsy. A simpler solution would be to determine an average value for C_1 from Figure 5 for the peak voltage the device will see.

A bipolar device in the quiescent state will display a capacitance characteristic very similar to that shown for the MOSFET. However, when either the base-emitter or base-collector junctions are forward-biased and conducting, the capacitance values are drastically changed. When the bipolar is conducting in the forward direction the base-emitter junction is forward-biased and displays a very large value of diffusion capacitance. This means that C_2 is large and the dV/dt capability is greatly **increased.** If on the other hand the device is conducting in the reverse direction then the collector base junction is forward-biased and C_1 is much larger. This greatly **decreases** the dV/dt capability of the device. Even if a diode is shunted across the bipolar (D_1 or D_2) some small current will still be available to forward bias the base-collector junction.

The three operating states defined earlier determine the choice of values for C_1 and C_2. Of the three conditions the reverse conduction mode is by far the worst and has the lowest dV/dt threshold. For the quiescent state for bipolars and MOSFETs, and the forward conducting state of the MOSFET, the amplitude of the current pulse due to dV/dt triggering is usually not damaging except in very fast circuits. In the forward conducting state in a bipolar, C_2 is so large that given the limits on bipolar switching speeds dV/dt triggering is not a problem. However, in the case where reverse conduction has occurred, the resulting pulse in a circuit like that in Figure 44 can destroy both devices. As a practical matter, it is difficult to measure the diffusion capacitances so the designer must test the desired device under actual circuit conductions for dV/dt capability.

The Parasitic Bipolar in MOSFETs

The present power MOSFET devices all have a parasitic bipolar transistor as an inherent part of the structure. The equivalent circuit for an N-channel device is given in Figure 49. For a P-channel device the parasitic transistor would be a PNP. The base and emitter connections of the parasitic transistor are connected together at the surface of the die to minimize the value of R_{BE} but there is still some resistance in the bulk of the semiconductor material. The value for R_{BE} will vary depending on the size of the die and the voltage rating but is generally 2Ω or less. In devices of similar design and voltage rating, C_{ob} increases with die size at the same rate as R_{BE} decreases so that τ_1 remains essentially constant. C_{ob} is essentially equal to C_{ds}. As the voltage rating is increased, C_{ob} decreases more rapidly than R_{BE} increases so that τ_1 is smaller in higher voltage versions of the same design.

The question when using a MOSFET is which device, the MOSFET or the parasitic bipolar, determines the dV/dt limit? Usually $C_{gs} < C_{ob}$, $R_g < R_{BE}$ and $V_{th} > V_{BE}$. As long as the user keeps the source impedance low during positive drain transitions the maximum dV/dt is determined by the bipolar. Too high a gate impedance can, however, lower the dV/dt rating by allowing the MOSFET to turn on.

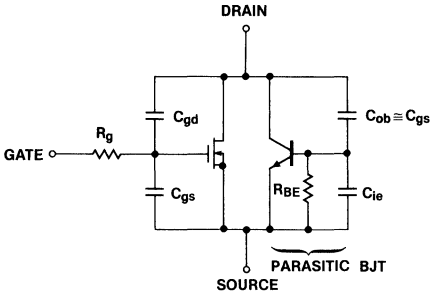


Figure 49. MOSFET Model Including Parasitic BJT

Another unpleasant possibility in a MOSFET is that if the parasitic NPN is turned on it may experience second breakdown due to thermal instability.

Temperature Effects

The threshold for dV/dt triggering will decrease with temperature for several reasons. V_{th} in a MOSFET has a negative temperature coefficient of about 6mV/°C. Similarly, V_{BE} in a bipolar has a negative temperature coefficient of about 2mV/°C. Typically for a bipolar $V_{BE} = 0.7$ and for a MOSFET $V_{th} = 2.0$ to 5.0V. The temperature coefficient for the bipolar is a larger percentage of the threshold voltage than in the MOSFET so that the degradation of dV/dt due to temperature-induced threshold shift is more pronounced in the bipolar.

The internal portion of R_g in the MOSFET is primarily due to the gate connection material. In some structures, particularly VMOS, the gate connections are made with aluminum which produces a very low R_g that does not vary greatly with temperature. DMOS devices on the other hand use poly silicon gate structures which have a higher R_g with a temperature coefficient of about 0.6 to 0.7%/°C. In the parasitic bipolar, R_{BE} will have a temperature coefficient of 0.6 to 0.7%/°C. In a bipolar switch most of R_{BE} will be in the external circuit and will probably not vary significantly with temperature.

The ON resistance of the MOSFET has a positive temperature coefficient while the bipolar has a negative temperature coefficient. The result is that at higher temperatures the MOSFET ON resistance will tend to decrease the amplitude of the current pulse due to dV/dt and the bipolar will tend to increase the current pulse.

The gain of the MOSFET is not greatly affected by temperature but the h_{FE} of both the parasitic transistor and the bipolar switch does increase with temperature. This means that if the bipolar is turned ON more current will flow at higher temperatures.

The duration of the current pulse caused by dV/dt triggering depends on the length of time e_O is above V_{th} and in the case of a transistor, the storage time is added to this. The storage time will increase with temperature.

If the dV/dt capability of the switch is not adequate due to reverse conduction, a low V_f or Schottky diode may be added in series with the drain as shown in Figure 50 and a separate external diode connected across the combination (D_2).

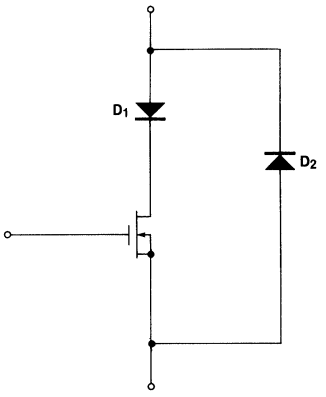


Figure 50. Method for Eliminating Reverse Conduction

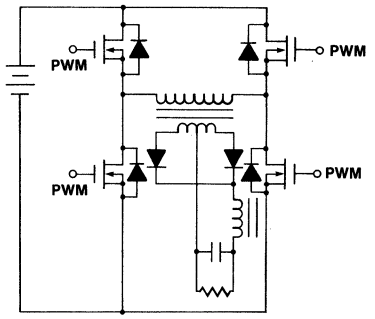


Figure 51. Quasi-Squarewave Bridge Converter

As shown in Figure 52, the forward voltage drop (V_f) characteristic is typical for a junction diode. Because of the large die areas normally used in a power MOSFET, V_f is quite low.

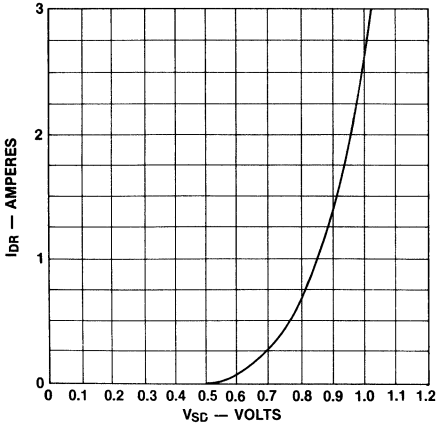


Figure 52. IVN6000 Diode Forward Voltage Characteristic

USING THE INTERNAL DIODE

The parasitic transistor can be used as a rectifier or clamp diode in switching regulator circuits. For example (Figure 51), the clamp diode usually added in a bipolar bridge inverter comes for free in the MOSFET. The internal diode has the same breakdown voltage and current ratings as the MOSFET itself, because it uses the same silicon, metalization, bond wires and package. The reverse recovery time (t_{rr}) for the diode can be excellent. In the IVN5000 and 5200 series devices, $t_{rr} = 60$ns and in the IVN6000 $t_{rr} = 100$ns. There are several reasons for the high speed. First, the structure is an epitaxial diode with sharply-defined diffusions. Second, the doping of the p-region is done using an ion implant machine. The ion implant process produces dislocations in the crystal structure which can act as recombination centers to reduce the recovery time. Not all manufacturers use ion implant techniques, and there may well be a wide variation in t_{rr} for similar devices from different manufacturers or from the same manufacturer at different times when there has been a process change.

A MOSFET may be used as a bidirectional switch or as a synchronous rectifier. Referring to Figure 53, when the gate is made sufficiently positive with respect to the source, the MOSFET becomes essentially a resistor in which the current may flow in either direction, source to drain or drain to source. As long as the voltage drop across $r_{DS(ON)}$ is below 0.6 volts, the parasitic diode will not conduct appreciably and the FET can be used as a bidirectional power switch with zero offset voltage. If synchronous rectifier operation is desired, the gate-source voltage is zero when the drain-source voltage is positive, thereby blocking the flow of current. When the drain-source voltage reverses, the gate is driven positive and current flows from source to drain. The

user now has a majority carrier rectifier with no storage time and a switching time equal to that of the FET (usually a few ns). The voltage breakdown rating is, of course, equal to that of the FET. If the voltage drop across the FET exceeds the threshold of the parasitic diode, the current is bypassed around the FET and V_f assumes the characteristic of the diode.

The designer must keep in mind the dV/dt limitations of the internal diode.

(A) NORMAL SYMBOL FOR N-CHANNEL

(B) DIODE EMPHASIZED

Figure 53. Diode in MOSFET Structure

MULTIPLE DEVICE OPERATION

The positive temperature coefficient of $r_{DS(ON)}$ is of great assistance when MOSFETs are paralleled. It is possible, in DC applications, to parallel devices without any matching, and those devices that initially draw the most current will heat up and shift the current to other devices to more equally distribute the current. This is exactly the opposite of the scenario for bipolar devices. While the paralleling of unmatched devices will work, it is a poor idea because a higher than necessary dissipation may occur, and in switching applications it is possible for one device to turn on or off before or after the others, and to have to accept the full load current. This may force the device to function outside of its safe operating area.

It is recommended that the user parallel devices which have been matched for V_{th} to within 5%. This will assure that the turn-on and turn-off delays due to the gate voltage rise and fall times, relative to V_{th}, are nearly equal. The values for $r_{DS(ON)}$ will also be very close, so that excessive differential heating is not encountered. Some additional improvement in $r_{DS(ON)}$ matching may be achieved by providing higher V_{GS} so that all of the parallel devices run at their minimum $r_{DS(ON)}$ value.

It should be kept in mind that many MOSFET devices have gain bandwidth products over 500MHz. It is entirely possible for these devices to oscillate at very high frequencies, especially if multiple parallel devices are used. This is often an unsuspected cause of device failure. If the circuit designer is using a low-bandwidth oscilloscope during breadboard development, it is possible to be unaware of the self oscillation, and therefore the use of an oscilloscope with a bandwidth of at least 200MHz is recommended. The tendency towards oscillation can be greatly reduced by inserting ferrite beads or low-value (50-100Ω) resistors in series with the gate leads, as shown in Figure 54.

For fast pulse applications, it is not sufficient to merely match the devices. The circuit must also be reasonably symmetrical so that identical drive voltages are applied to each gate. At high speeds the inductive as well as resistive effects must be considered. If, for example, the parasitic inductance in the drain lead of Q_1 is much smaller than that in the drain lead of Q_N, when the devices are first turned ON most of the load current will initially flow through Q_1, even if the gate drives and threshold voltages are identical.

Variations in the stray gate circuit capacitance and the device input capacitance can also cause uneven turn-on in fast pulse applications. The effect of this can be reduced by equalizing the stray capacitance and minimizing the intergate impedances. For applications requiring switching times below 10ns, it may be necessary to match the device capacitances.

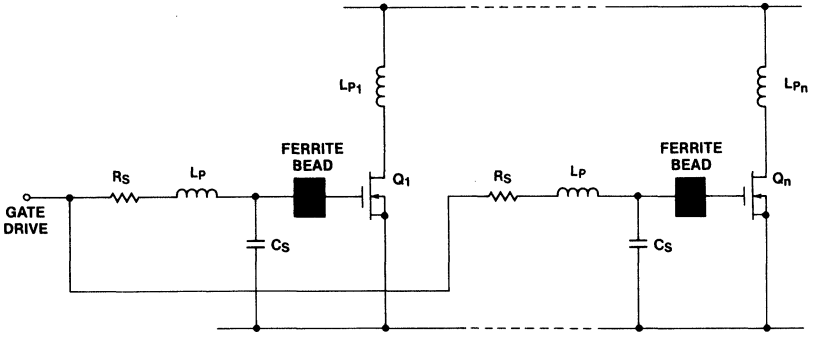


Figure 54. Parallel Devices

It should be kept in mind that most of the complications in paralleling mentioned above apply only for very fast pulses. Most applications will use transition times well above 10ns, where simple threshold voltage matching is all that is required. This is quite different from bipolar devices where paralleling more than two devices can become quite complex and expensive. Due to the practical difficulties of paralleling large numbers of individual bipolars, (and SCRs also), the trend has been to develop ever larger single devices. As the die size increases, a point is reached where either the thermal capabilities or the available mounting areas of the low-cost packages are exceeded so that a more expensive package is required. In addition the heat sink will now see a concentrated thermal input through the relatively small package to heat sink contact area. The efficiency of a heat sink is better if the heat input is distributed in several sources rather than in one.

While the arguments for using a single large bipolar device instead of multiple smaller devices are well founded, it does not necessarily follow that the same technique should be imitated in power MOSFET devices, especially in the light of the rapid cost increase of the larger die. The tradeoff may well be multiple devices with low die and package and moderate heat sink costs, versus single devices with high die, package and heat sink costs. Just where the cost crossover point between single and multiple devices is has yet to be determined, especially since the very high prices for the present larger MOSFETs are certain to be reduced substantially.

The following design example illustrates the thermal arguments for paralleling devices.

Statement of the Problem:

Solve for the heat sink area, volume, and cost and the combined heat sink and device cost. Compare one 0.05-ohm device to four 0.2-ohm devices.

Operating Conditions:

I_D = 25A RMS
T_a = 40°C
T_{jmax} = 150°C
Altitude = Sea level
Cooling = Still air convection cooling
$R_{\theta CH}$ = 0.4°C/W (this is the case to heat sink thermal impedance due to mounting surface irregularities, etc., for a TO-3 case)

Device Characteristics:

0.05-OHM DEVICE	0.2-OHM DEVICE
TO-3 Case	TO-3 Case
$R_{\theta JC} = 0.83$°C/W	$R_{\theta JC} = 1.5$°C/W
$r_{DS(ON)} = 0.05\Omega$	$r_{DS(ON)} = 0.20\Omega$ @ 25°C
$\alpha = 0.5\%/$°C	$\alpha = 0.5\%/$°C
Cost = $62.20	Cost = $7.00

For this problem the device power dissipation, P, and heat sink area, A, can be shown (see appendix) to be:

$$A = \left[\frac{80P^{0.85}}{T_j - T_a - P\,R_{\theta CH}}\right]^{1.43} \quad (39)$$

$$P = r_{DS(ON)}e^{\alpha^*\Delta T} \quad (40)$$

(Note: Equation 40 is equivalent to Equation 12.)

Calculations:

One 0.05-Ohm device:

$$P = (0.05)\,(25^2)e^{(0.005)\,(110)} = 54.2W$$

$$\theta_{j-hs} = R_{\theta JC} + R_{\theta CH} = 0.83 + 0.4 = 1.23\,°C/W$$

$$A = \left[\frac{80(54.2)^{0.85}}{110 - 54.2(1.23)}\right]^{1.43} = 308\ in^2$$

Because the heat input is concentrated, the heat sink will be less efficient by 10 to 30% than calculated. For a 20% loss in efficiency:

$$A_1 = 370\ in^2$$

Four 0.2-Ohm devices:

$$P = 54.2W$$

$$R_{\theta CH} = \frac{1.5 + 0.4}{4} = 0.48\,°C/W$$

$$A_2 = \left[\frac{80(54.2)^{0.85}}{110 - 54.2(0.48)}\right]^{1.43} = 120\ in^2$$

Using the AHAM #4501 heat sink extrusion (A = 28 in²/in) the heat sink length, L, and volume, V, are:

$L_1 = 13.2$ in $L_2 = 4.3$ in
$V_1 = 64\ in^3$ $V_2 = 21\ in^3$
$V_1/V_2 = 3.1!$

A 72″ section of this heat sink costs about $80, so:

$C_1 = \$14.67$
$C_2 = \$\ 4.78$

Total Costs: One 0.05-ohm device = $76.87
Four 0.2-ohm devices = $32.78

There is a better than 2:1 cost and 3:1 volume advantage to using the multiple devices.

The 0.05-ohm device prices can be expected to come down substantially but so will the price of the 0.2-ohm devices, so it is very likely that four 0.2-ohm devices will continue to be cheaper than one 0.05-ohm device. There will be some additional assembly charge to mount four devices versus one device but that should not materially affect the comparison.

If this were a military application, then the junction temperature would be limited to 105°C and the ambient would be +50°C or higher. Recalculating the heat sink areas for +50°C ambient and $T_j \neq 105$°C:

$A_1 = 1503\ in^2$
$A_2 = 227\ in^2$
$A_1/A_2 = 6.62!$

By no means does the design example imply that multiple devices are **always** superior to a single device. The tradeoff will depend on device costs and cooling provisions, and the tradeoff will take the general form shown in Figure 55. In some situations the additional volume of the multiple packages may be a problem. In most cases, however, this should not be a concern. It can also be argued that the increased number of devices reduces the reliability. The counter argument to this is that multiple devices can be run cooler due to the improved thermal efficiency and the net reliability is actually increased.

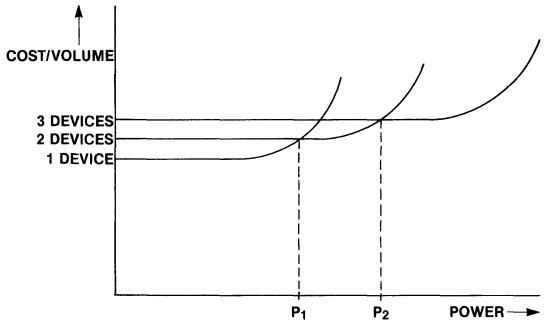


Figure 55. Cost versus Power Dissipation

Series Operation MOSFETs

MOSFETs can be connected in series for high-voltage operation. It is particularly important that all devices in the same series string come ON simultaneously, otherwise one device may take all of the voltage momentarily. The devices should be well matched for V_{th} and careful attention given to producing simultaneous gate drive. In those applications where the maximum possible voltage capability is desired, it may be necessary to match the $r_{DS(ON)}/V_{GS}$ characteristic to assure equal voltage distribution during switching transitions. This is a much more complex procedure than V_{th} matching, and should be considered only as a last resort. It is probably preferable to use some form of snubber network to equalize the voltage distribution during switching. Analogous to the parasitic inductance in parallel operation is the effect of circuit parasitic capacitance in series operation. If differential drain-source capacitances (either in the device or in the circuit layout) exist in the series string, the transient voltages may not be shared equally.

Combinations of Bipolar Transistors and MOSFETs

MOSFETs can be combined with transistors in a variety of useful ways. The most obvious combination is to use medium-power MOSFETs to drive high-power bipolars; the MOSFET is an excellent buffer between TTL or CMOS logic and large bipolar devices.

Two base drive possibilities are given in Figure 56. In (B) R_1 and R_2 are selected independently to provide the appropriate values for I_{B1} and I_{B2}. If negative bias for Q_3 is desired, the source of Q_2 and the ground pin of the DS0026 may be referenced to a negative potential. Figure 57 shows a proportional[5] base drive circuit.

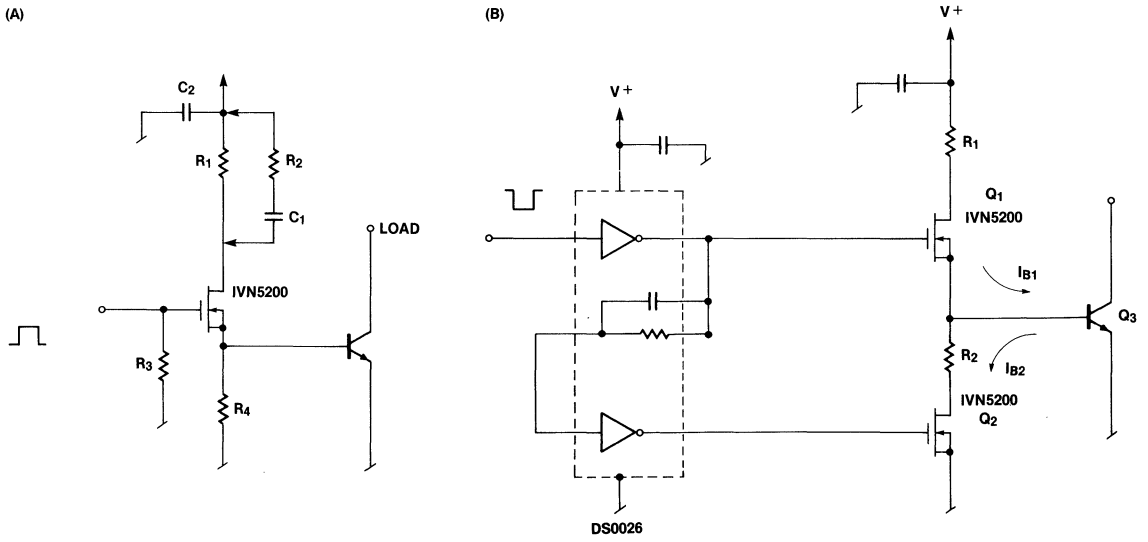


Figure 56. Bipolar Base Drive Using MOSFET

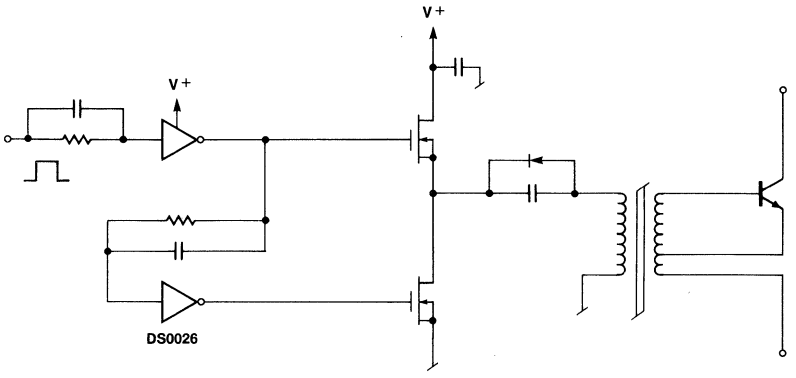


Figure 57. Proportional Base Drive Circuit

In addition to using MOSFETs to drive bipolar transistors, the two types of devices may be combined into a compound device. Some of the possibilities are shown in Figure 58. The Darlington connection (58A and 58B) using a MOSFET for the driver will display essentially infinite beta. The cascade connection shown in Figures 58C, 59 and 60 is a means to obtain fast switching from a large high-voltage bipolar by inserting a low-voltage, low-$r_{DS(ON)}$ MOSFET in the emitter.

Another interesting possibility is to parallel a MOSFET and a larger bipolar transistor. The MOSFET and the transistor are driven on simultaneously but due to the relatively slow turn-on of the bipolar all of the current flows initially through the MOSFET. When the bipolar is fully on (approximately 1μs) nearly all of the current flows through it. The bipolar has a much lower voltage drop than the MOSFET. At turn-off the drive is removed from the transistor first, and approximately 1 to 3μs later, the MOSFET is turned off. The staggered turn-off should be relatively easy to implement in the drive logic. This combination displays the fast switching time of the MOSFET along with the low V_{CE} of the transistor.

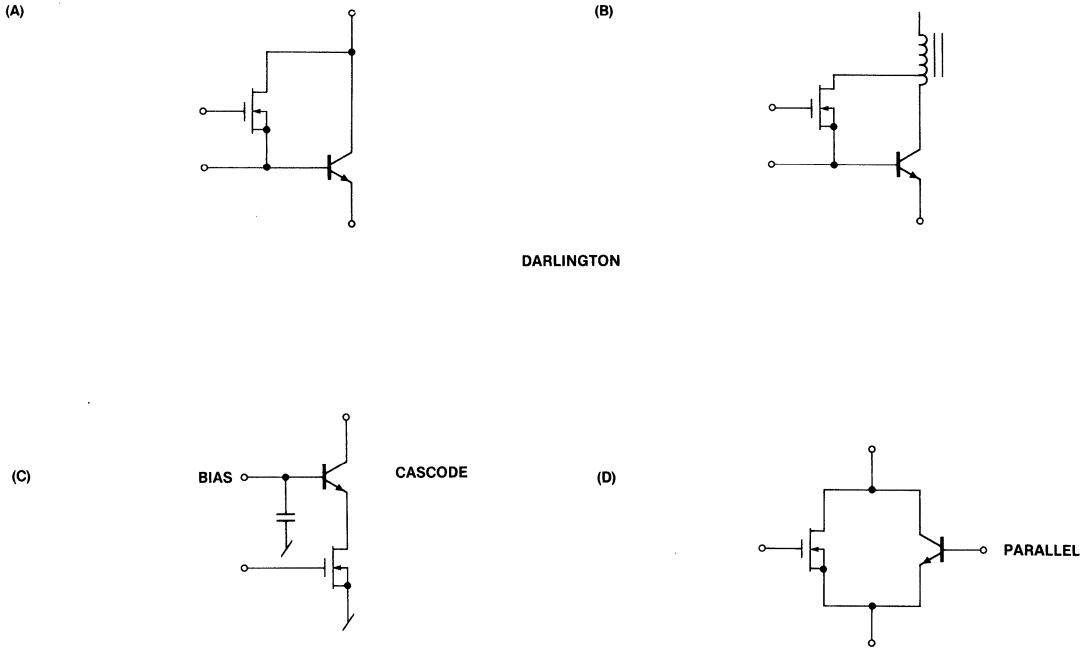


Figure 58. BJT/MOSFET Combinations

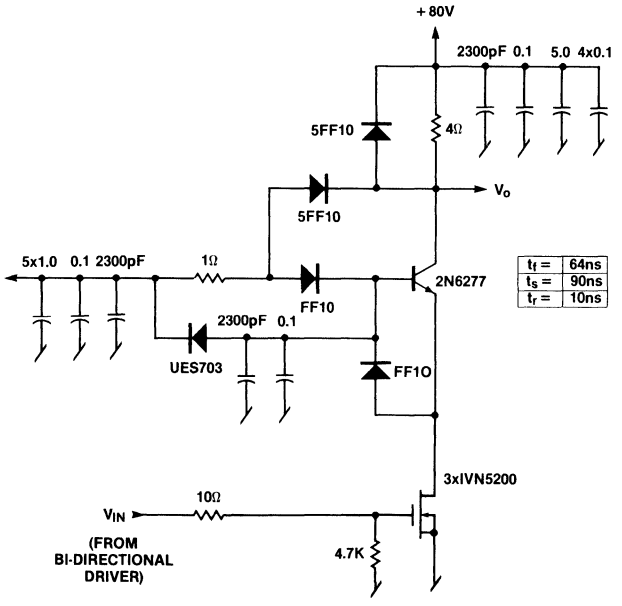


Figure 59. Cascode BJT/MOSFET Circuit

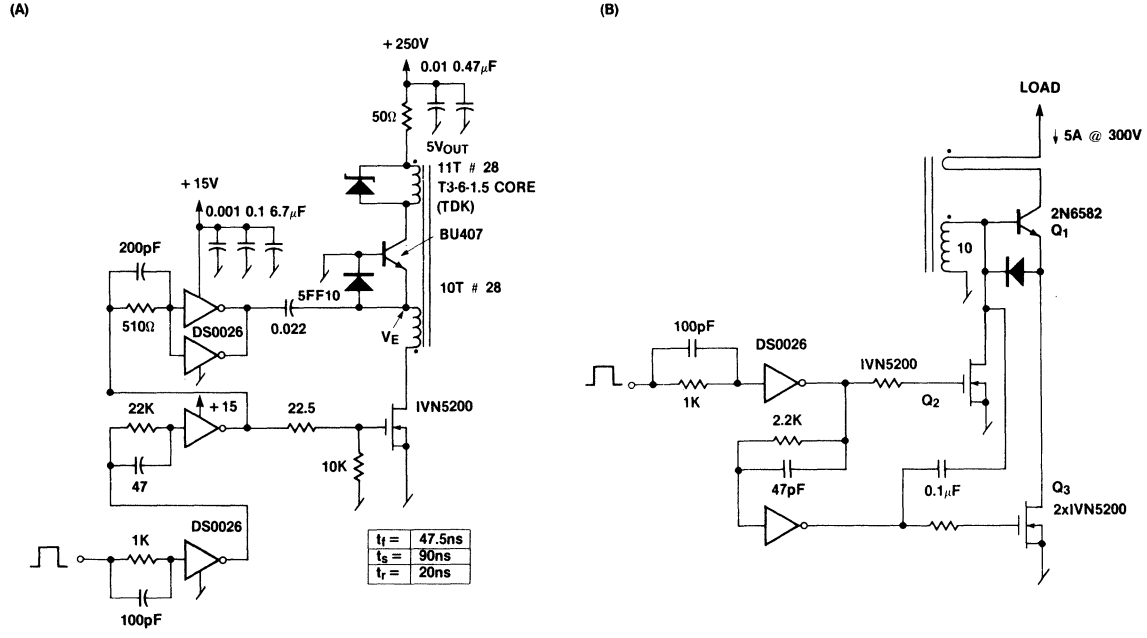


Figure 60. Proportionally Driven Cascode BJT/MOSFET

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INTERSIL

A037
High Performance Off-Line Switch Mode Power Supply

by Rudy Severns

INTRODUCTION

Within the next year, the Switch Mode Power Supply (SMPS) market is expected to grow from 30% to well over 50% of the power supply business. Users are demanding low cost and high reliability in a smaller, lighter package, and recent advances in the development of high voltage power FETs are having a significant impact on the design of SMPS's. The IVN6000KNT has several unique characteristics ideal for SMPS applications Clever utilization of these qualities results in substantial system gains over traditional bipolar designs.

450 VOLT VERTICAL POWER MOS FET

Fabrication

The IVN6000 family is fabricated in Intersil's new vertical DMOS process. "Self-aligned" processing (with fewer masking operations and no critical etching) eliminates many of the manufacturing and reliability problems which plagued the prior art. A cross section of the vertical DMOS structure is shown in Figure 1.

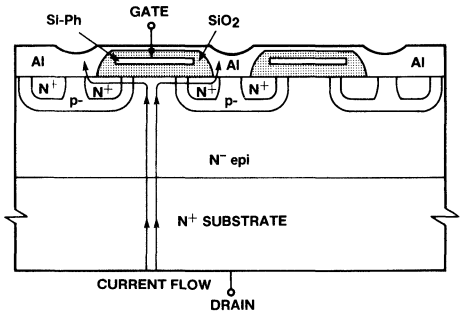

Figure 1. Vertical DMOS Structure

The surface topology of the IVN6000KNT has been designed for maximum breakdown voltage and drain current while minimizing capacitance and switching time for a given chip size.

Power MOS FETs offer significant performance/cost advantages over bipolar power transistors in many applications. A comparison of devices is shown in Table 1.

Safe Operating Area Rating (SOAR)

The Safe Operating Area curve for the IVN6000KNT is shown in Figure 2.

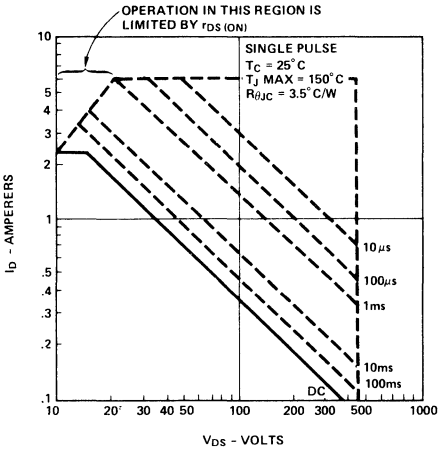

Figure 2. Safe Operating Area (SOA)

Table 1.

POWER FET	BIPOLAR
Advantages	**Advantages**
1. Wide Safe Operating Area (SOA)	1. Low Saturation Voltage
2. Very High Current Gain	2. Availability
3. Very Fast Switching	
4. "Free" Reverse Diode	
5. No Thermal Runaway	
6. Drive Simplicity	
7. Inherent Current-sharing when paralleled	
Disadvantages	**Disadvantages**
1. Static Sensitivity	1. Device Storage Time — Losses, Frequency Limitations
2. Comparatively High Conduction Losses	2. Base Drive Complexity and Power Dissipation
	3. Current Hogging when Paralleled
	4. Thermal Runaway
	5. SOA Limitations

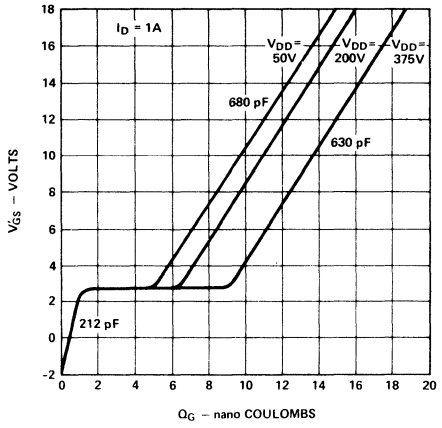

Figure 3. Gate Drive Dynamic Characteristics

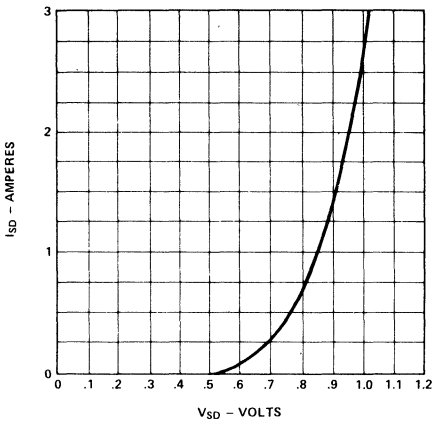

Figure 4. Diode Forward Voltage Characteristics

During the brief transition when the power MOSFET switches, instantaneous peaks of 450 volts at 7.5 amps (3375 watts) can be tolerated. Typical worst case SMPS conditions are well below these limits, thus insuring a wide operating margin.

MOSFET Switching Properties

Power FETs are voltage controlled devices (as opposed to bipolar transistors which are current controlled). Since the input is capacitive, gate charge determines the drain-source enhancement.

Figure 3 shows the IVN6000KNT drive characteristics in nano Coulombs.

Since the charge

$Q = I_g t_s$ where I_g = Gate Current

then

$t_s = Q/I_g$ t_s = Switching Time

The switching time is dictated almost entirely by the applied gate current since there is no minority carrier storage time.

Switching a 1 A load to 375 Volts in 100 nanoseconds requires only 100 milliamperes of gate drive. This feature makes possible the use of extremely simple and reliable drive circuits, as well as operation far in excess of the traditional 20 kHz switching frequency.

Integral Reverse Diode

Inherent in the power MOSFET is a fast recovery epitaxial diode with very acceptable low forward drop. This "free" reverse diode serves an important role in many SMPS topologies. During the time interval in which the power MOSFET is off, the reverse diode provides a path for inductor current. Bipolar designs require the addition of an "extra" discrete fast-recovery diode. The IVN6000KNT integral reverse diode is fast and also exhibits low loss. The diode forward drop characteristics are shown in Figure 4.

Under typical operation, a forward drop of < 1.0 Volt is common.

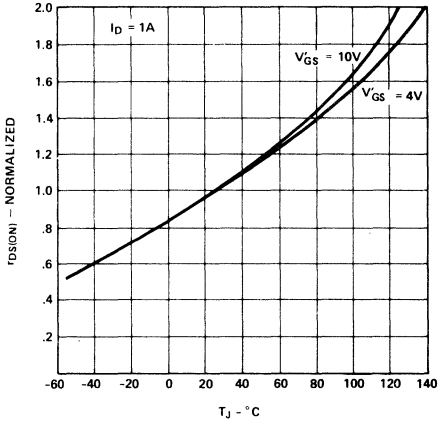

Figure 5. ON Resistance vs. Junction Temperature ($V'_{GS} = V_{GS} - V_{GS(th)}$)

Paralleling MOSFETs

The IVN6000KNT can be paralleled without fear of current hogging or thermal runaway. This is significant in that it allows the designer to scale up/down designs by merely paralleling devices. The device has a positive temperature coefficient for $r_{DS(on)}$. See Figure 5.

The device conduction losses are

$P_c = V_{DS}^2/r_{DS(on)}$ where V_{DS} = Drain-source on voltage

$r_{DS(on)}$ = Drain-source on resistance

Given the situation in which two paralleled devices have different $r_{DS(on)}$ values, the device with lower ON resistance will dissipate the most power. Junction heating increases $r_{DS(on)}$ and reduces its power dissipation, and this negative-feedback insures stable operation between paralleled devices.

DESIGN NOTES

The complete 5V/50 Amp off-line (100/220 VAC) SMPS using power MOSFETs is shown in Figure 6. The system specifications are as follows:

SPECIFICATIONS:

Input Characteristics:	115/220 + 10%-20% VAC, 47-63 Hz
DC Output Ratings:	5V at 50A
Output Ripple and Noise:	50 mV_{pp} Maximum
Overload Protection:	Fold-back type with automatic recovery
Over Voltage Protection:	Set at 5.6V
Temperature Rating:	Operating 0°C to +40°C at full-rated power
Cooling:	Convection
Thermal Protection:	Internal thermostat shutdown for over temperature
Remote Sensing:	Available to provide compensation for line losses.
AC Under Voltage Inhibit:	Inhibits operation below 90/180 volts AC input
Slow Turn-On Circuitry:	In-rush current limiting thermistor, slow-start pulse width modulation

Power Mesh

The converter configuration chosen for this application was the half bridge. As illustrated in App. Note A034, other topologies may result in lower conduction losses, however, the half bridge has several advantages. A prime consideration is that maximum voltage seen across the FETs cannot exceed the rail voltage. For 110/220 VAC line this represents a peak of 360 VDC. However, to insure sufficient guard banding to accommodate line/rail spikes and low temperature BV_{DSS} de-rating, the IVN6000KNT —450 volt power FET is recommended. The half bridge is also advantageous in terms of the transformer design. A smaller core, without primary center-tap, and a favorable turns ratio are derived.

Other key factors in selecting this topology were:

1. Well-understood and easy-to-stabilize feedback loop.
2. Relatively low RFI.
3. Circuit simplicity — single transformer driver, utilization of the FET integral reverse rectifier.

An operating frequency of 60 kHz (per switch) was chosen. This is a compromise in that only modest improvements in size, weight, bandwidth, etc., are derived as a direct result. The major improvements are achieved through circuit simplification. The criterion for selecting this frequency was the availability of components; i.e., diodes, capacitors, integrated circuits, etc.

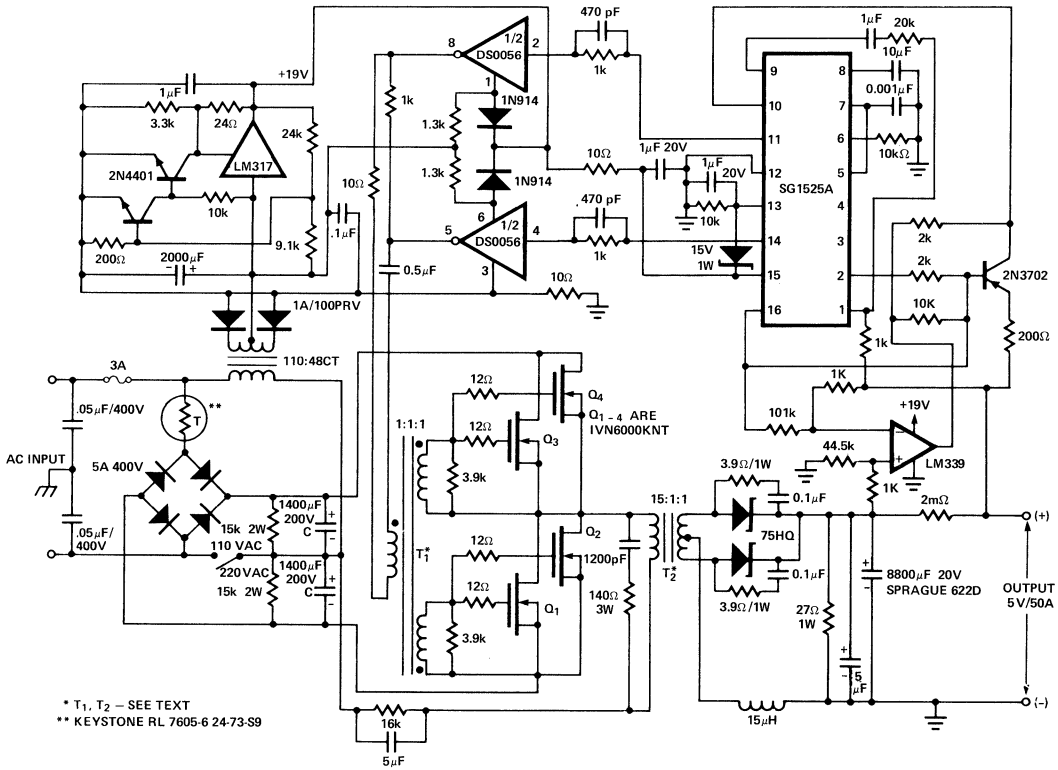

Figure 6. Power MOSFET SMPS

The output is straightforward, consisting of a full wave center-top configuration and LC filter. 75HQ Schottky rectifiers are used to reduce rectifier dissipation. Worst case losses for the Schottky diodes is 35 watts.

The half bridge consists of two pairs of IVN6000KNTs. Paralleling limits the conduction losses to a maximum of six watts/FET or 24 watts total. Each device sees less than 1.25A RMS and 2A peak, well within the rated 2.25A RMS and 7.5A peak.

The power transformer consists of a single primary and center tapped secondary, with a turns ratio of 15:1:1. To achieve high efficiency it is important to keep the magnetizing and leakage losses low. It can be shown that a magnetizing current $I_m = 0.4A$ results in a worst case increased dissipation of 3W (total). This being acceptable, the minimum magnetizing inductance L_m becomes:

$$L_m = \frac{V_t}{I} \quad \text{or} \quad L_m \sim 4.5\,\text{mH}$$

Losses due to leakage inductance must also be minimized since:

$$P_{LK} = L_{LK} \times I_p^2 \times F$$

Paying close attention to the magnetic design, L_{LK} as low as 4.5 μH can be achieved. This results in a maximum leakage loss $P_{LK} \sim 3.7$ watts. The RC snubber network absorbs most of this energy. Core and copper losses account for about 2.5 watts. A ferrite, toroidal core was chosen with filar windings; this structure tends to reduce leakage inductance and RFI.

FET Driver

Of first order is the switching losses. The energy dissipated during the switching interval is:

$$W_S = \int_0^t V_{DS}(t)\, I_D(t)\, dt$$

The switching losses can then be expressed as:

$$P_S = f_S\left[W_{S(on)} + W_{S(off)}\right]$$

Assuming constant current and linear voltage ramps, the expression for the switching losses becomes:

$$P_S \sim f_S \times V_{DS} \times I_D \times t_S$$

A more exact expression for switching losses can be derived, however the contribution of losses due to switching is small in comparison to other system losses.

Acceptable switching losses are obtained when the switching time is 40ns; i.e., $P_S = 0.75$ watt/device. The gate drive current required to achieve a t_s of 40ns is

$$I_g = \frac{Q_g}{t_s}$$

where

$Q_g \sim$ 10 nano Coulombs/device

or

$I_g \sim 0.25$A/device

This is derived with the DS0056, high speed, monolithic dual clock driver, which provides up to 1.5A at 20 volts output drive. Drive transformer T_1 is tri-filar wound 1:1:1 with a magnetizing inductance $L_m \sim 7$mH and leakage inductance $L_{LK} \sim 0.7$ μH. Minimization of L_{LK} is essential. It can be shown that L_{LK} dominates in the calculation of switching time where:

$$t_s \approx \sqrt{\frac{2\,Q_g\,L_{LK}}{V_{DT}}}$$

and

$V_{DT} = V_{DRIVER} - V_{TH}$ 10 or $t_s \sim 37$ ns.

This drive configuration has several advantages. Foremost is the condition that both outputs can never be on simultaneously. (Such a condition could be destructive to the FETs.) Furthermore, when power is removed, both outputs drop to zero rapidly, preventing any voltage spikes or asymmetrical charging. The circuit operates Class-C, consuming power only when an output is high. These functions are concisely achieved with a total of 10 components.

Switching Regulator Subsystem

Many of the basic characteristics of the power supply are controlled by the regulator subsystem. The circuit shown in Figure 6 uses an SG1525A integrated circuit to provide output regulation via duty cycle variation of the drive signal to the DS0056's. The SG1525A provides the required reference voltage on pin 16, the operating frequency of the system is controlled by the oscillator components on pins 5 and 7, and the circuit provides an automatic slow-start function through the capacitor on pin 8. Overvoltage protection is achieved by allowing the 2N3702 to activate the shutdown circuitry at pin 10. Frequency compensation is controlled by the components between pins 1 and 9, which set the medium frequency dynamic performance of the supply and also the loop stability. The LM339 and associated resistors provide short circuit current limiting with fold-back. (Note that the SG1525, which can be used in the same circuit, has a slightly different pin out.)

More complicated control functions can be realized by replacing the LM339 with devices such as the SG1542 through SG1544. Somewhat improved dynamic response can be achieved by using the TL494 in place of the SG1525A, and incorporating feed-forward compensation. This device also includes a current limiting circuit, obviating the need for the LM339, as shown in Figure 11.

Input Circuitry

The input circuitry is standard. A thermistor limits the in-rush current, and a shorting clip allows the option of 110 VAC or 220 VAC; a 3-terminal pass regulator provides power for the controller and driver; a 2-transistor, resistor network coupled to the LM317 provides "under voltage" protection. The auxiliary supply is regulated to 19 volts.

SYSTEM PERFORMANCE

Figure 7 is an oscillograph depicting the power transformer voltage and current waveforms. Figure 8 displays the voltage waveforms in the half bridge. The actual FET gate-source and drain-source waveforms are expanded in Figure 9. Current limiting is the fold-back type. The resulting output characteristics are illustrated in Figure 10.

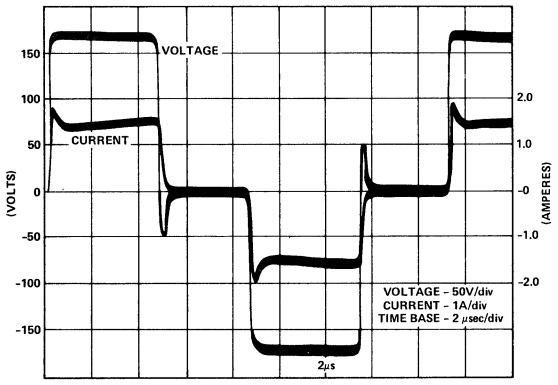

Figure 7a. Voltage/Current Waveforms Across T_2. 25A Load.

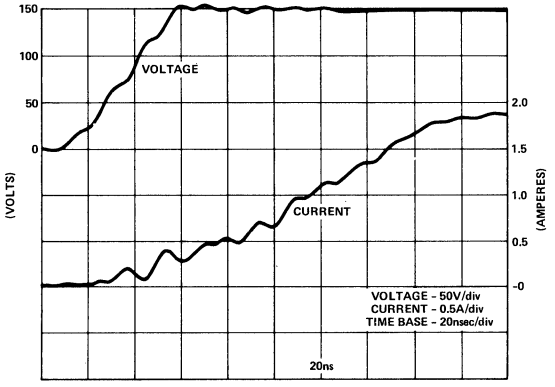

Figure 7b. Voltage/Current Waveforms Expanded. 25A Load.

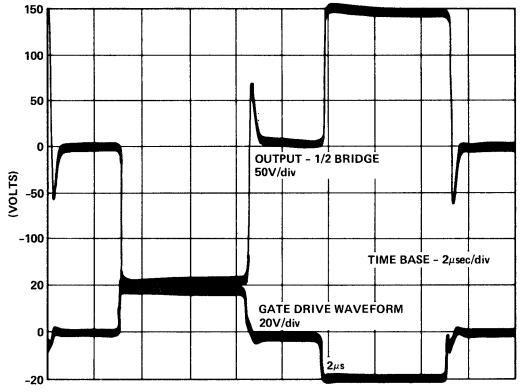

Figure 8. Half Bridge Waveforms (5V/25A Load)

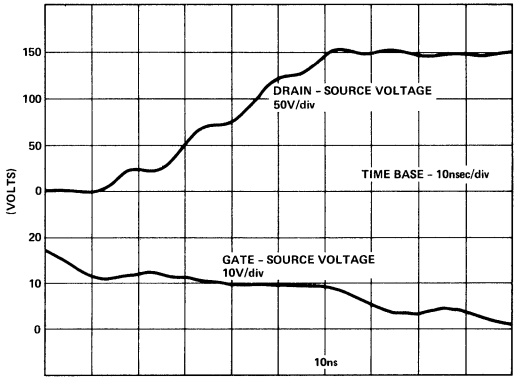

Figure 9. FET Switching Waveforms (5V/25A Load)

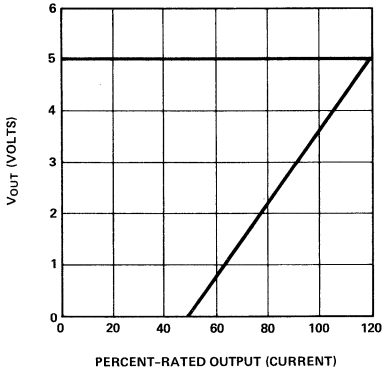

Figure 10. Current Fold-Back Characteristics

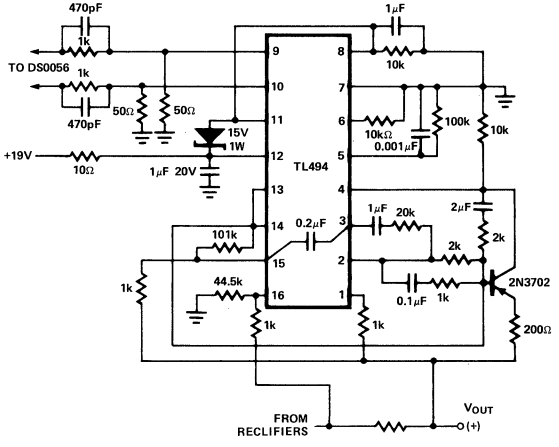

Figure 11. Alternative Control Circuit

The complete SMPS has a total of about 90 circuit elements, compared to a typical bipolar design which has 140. Calculated MTBF was 3.7 years, versus 2.9 for the bipolar. Current MOSFET prices tend to somewhat offset the cost savings derived by circuit simplification, but with the anticipated future price reductions substantial savings can be realized.

A clean mechanical layout is the key for stable operation; printed circuit boards should be double sided and ground-plane construction should be used. Using the circuit of Figure 6 in a far from optimized configuration, a power supply measuring 6" x 9" x 3-1/2" and weighing a mere 4 lb. 4 oz. was fabricated, see Figure 12.

SUMMARY

Recent advances in power MOSFET technology are having an impact on switching power supply design. Bipolar transistors have been replaced by power MOS FETs to achieve significant system advantages including lower cost, high reliability, reduced size and weight, and excellent electrical performance. The performance trade-offs are listed in Table 2.

ACKNOWLEDGEMENTS

The author would like to thank Rudy Severns for his numerous inputs; Brian Smithson, Bruce Hunter, and Janis Jenkins for laboratory work; and Peter Bradshaw, Larry Goff, and Dave Fullagar for general support.

OTHER APPLICATIONS BULLETINS

A034, *"The Design of Switchmode Converters Above 100kHz,"* by R. Severns.

A035, *"Switchmode Converter Topologies — Make Them Work for You,"* by R. Severns.

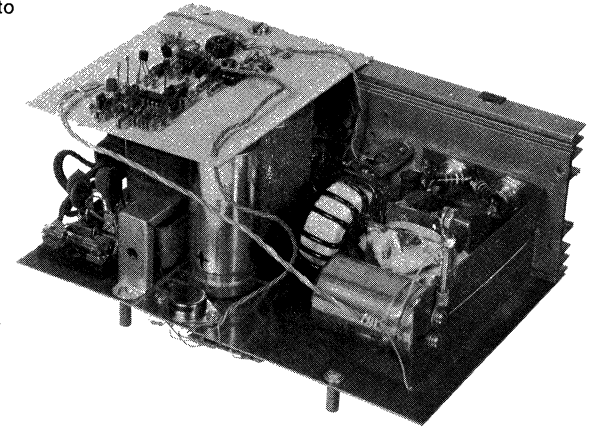

Figure 12. 250 Watt FET SMPS

COMPARISON: FET vs. Bipolar SMPS

Table 2.

FET	BIPOLAR
Advantages	**Advantages**
1. Significantly reduced circuit complexity and component count	1. Proven technology and long track record
2. Improved reliability	
3. Simplified manufacturing and test	
4. Low cost	
5. Straightforward family expansion	
6. Reduced size and weight	
Disadvantages	**Disadvantages**
1. No track record	1. Poor relative reliability
2. Potential RFI problems	2. High circuit complexity
	3. High manufacturing cost
	4. Limited design flexibility
	5. Larger weight/volume

INTERSIL

A038 Power MOSFETs for Analog Circuit Design

Bruce D. Rosenthal

INTRODUCTION

Although the power MOSFET has received widespread attention for its merits in switching applications, these same devices offer many advantages to the linear designer as well. Table 1 summarizes the advantages of power MOSFETs over bipolar transistors in linear applications, which include amplifiers (audio, servo, R.F.), oscillators and voltage and current regulators. This note is intended to familiarize designers with the power MOSFET as a linear circuit element and present a few design examples.

DEVICE BEHAVIOR

The ideal MOS device has two fundamental regions of operation. The equations below define these regions, which are shown graphically in Figure 1. Refer to Table 2 for the meanings of symbols used below. Equation (1) is valid in the linear region, Where $V'_{GS} > V_{DS}$. Equation (2) defines the saturation region where $V'_{GS} < V_{DS}$.

$$I_D = K'(2V'_{GS}V_{DS} - V^2_{DS}) \quad (1)$$

$$I_D = K'(V'_{GS})^2 \quad (2)$$

Table 1. FETs vs Bipolar for Linear Use

POWER FETs	BIPOLAR TRANSISTORS
Advantages	**Advantages**
1. Wide Safe Operating Area (SOAR)	1. Low Cost
2. High "f_t" and Breakdown Voltage	2. Well Understood
3. Very High Current Gain	3. Good Availability
4. Drive Simplicity	**Disadvantages**
5. Linear Transfer Characteristics	1. Low f_T
6. High Output Impedance	2. SOAR Limitations
Disadvantages	3. Base Drive Complexity
1. Static Sensitivity	4. Loop Stability Problems
2. Limited Design Experience	5. Non-linear Transfer Characteristics

Table 2.

Symbol	Name/Definition
V_{GS}	Gate-Source Voltage
V_{TH}	Threshold Voltage
V'_{GS}	Enhancement Voltage ($V_{GS} - V_{TH}$)
V_{DS}	Drain-Source Voltage
I_D	Drain Current
K'	A Constant Related to the Device Geometry
g_{fs}	Transconductance
f_t	Useful High Frequency Limit (Limited by Parasitic Gate Resistance and Capacitance and Package Inductance)
g_{os}	Output Conductance $= \frac{\Delta I_D}{\Delta V_{DS}}$
r_o	Output Resistance $= \frac{1}{g_{os}}$
C_{gs}	Parasitic Gate to Source Capacitance
C_{gd}	Parasitic Gate to Drain Capacitance
C_{ds}	Parasitic Drain to Source Capacitance

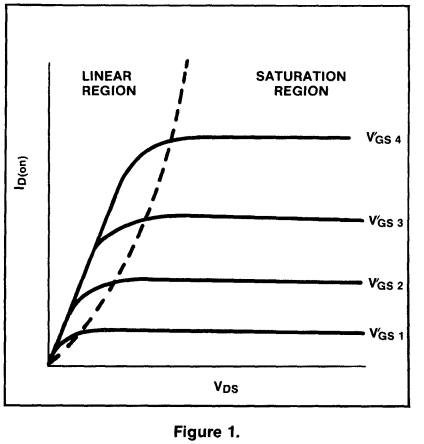

Figure 1.

Based on these fundamental equations, other key relationships can be derived. The transconductance (g_{fs}) can be described by the following equations.

$$g_{fs} = 2K'V'_{GS} \quad (3)$$

$$g_{fs} = 2\sqrt{K'I_D} \quad (4)$$

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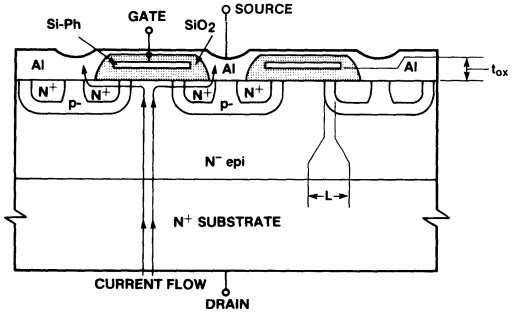


Figure 2. Vertical DMOS Structure

Figure 2 is a cross section of a typical power MOSFET with a simplified equivalent circuit shown in Figure 3.

Beginning with the input, r_g is the series gate resistance. In the device design, r_g is determined by the process used; (metal gate or poly gate) and by surface topology. The internal capacitances are highly voltage dependent, except for C_{gs} as shown in Figure 4.

Best high frequency performance is obtained under conditions where substantial drain-source and drain-gate bias is applied.

Drain-source current flow is determined by:

$$I_{DS} = g_{fs} V'_{GS} \qquad (5)$$

Referring to equations (2), (3), and (4) for the saturation region, we can predict the drain-source output behavior. Typical output characteristics for the IVN6000KNT are shown in Figures 5, 6, and 7.

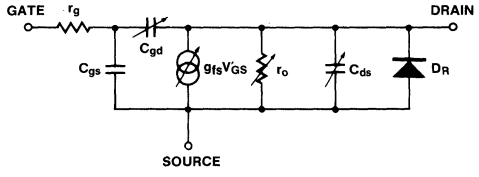


Figure 3. Equivalent Circuit

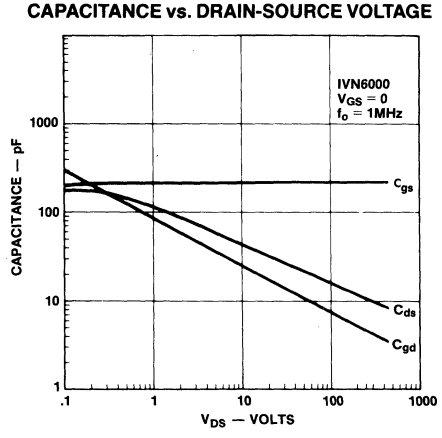


Figure 4. Device Capacitances

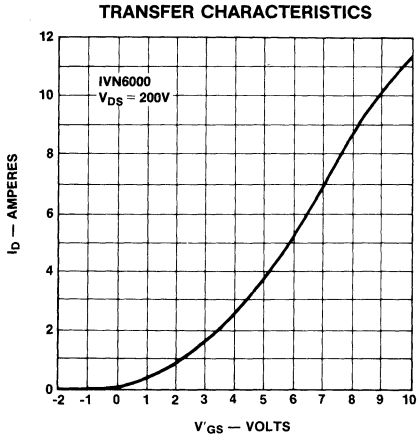


Figure 5. Drain Current vs. Gate-Source Voltage

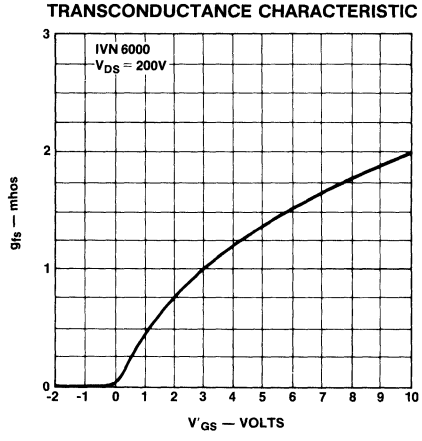


Figure 6. Transconductance vs. Gate-Source Voltage

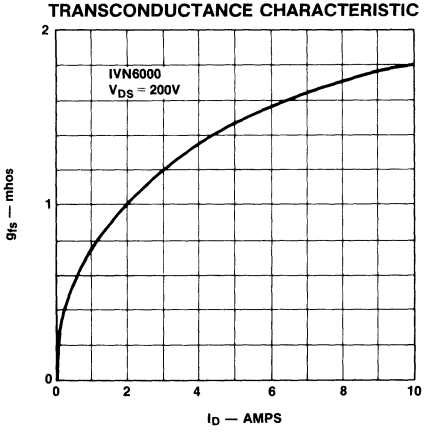


Figure 7. Transconductance vs. Drain Current

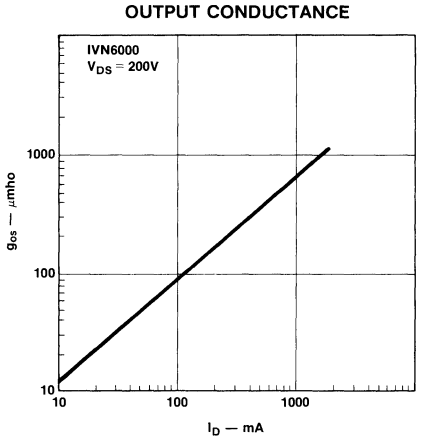


Figure 8. Output Conductance vs. Drain Current

In linear applications the gain factor (μ) is very important. This is defined in equation (6) by:

$$\mu = g_{fs}\, r_o \qquad (6)$$

where: $r_o = 1/g_{os}$

Like g_{fs}, r_o is a function of drain current (I_D) as shown in Figure 8.

The internal reverse diode (D_R) is a fast recovery (100nsec typ.) silicon diode. The forward conduction behavior is similar to standard PN junction diodes.

BIASING

Biasing power MOS devices for linear use involves many of the same practices employed with bipolars with one exception: *the gate current required to establish equilibrium is practically zero.* Two rudimentary configurations are shown in Figures 9 and 10.

In Figure 9, resistors R_1 and R_2 can be extremely large since no D.C. current flows. R_4 is used to stabilize the electrical and thermal operating points. The quiescent drain current is approximated by:

$$I_D \cong \frac{\left(\frac{V_S\, R_2}{R_1 + R_2} - V_{TH}\right)}{R_4} \qquad (7)$$

In applications where a source resistor cannot be used, the circuit in Figure 10 can be applied.

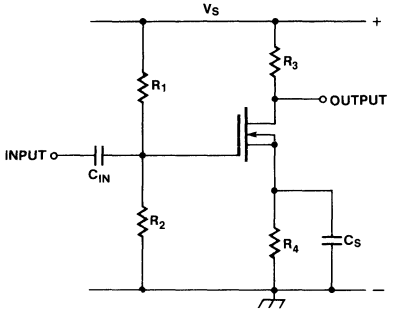


Figure 9. Simple Bias Configuration

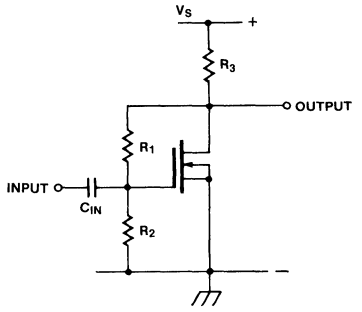


Figure 10. Feedback Bias Configuration

Again, R_1 and R_2 can be made very large because of the MOSFET's input impedance. In this example:

$$I_D = \frac{V_S}{R_3} - V_T \frac{(R_1 + R_2)}{R_2\, R_3} \qquad (8)$$

Normally, R_1 and R_2 are chosen to set up a current.

In biasing MOSFETs for linear operation, the designer must be aware of the fact that (as with bipolar devices) thermal runaway is possible because of the negative temperature coefficient of the threshold voltage V_{TH}. The resulting change in drain current for increased junction temperature with fixed gate bias is shown in Figure 11. This effect is most pronounced at low current. Stable biasing can be achieved with feedback, most simply by adding a source resistor as in Figure 9. Thermal transducers such as the Intersil AD590 or conventional thermistor can also be used.

CURRENT REGULATORS

The current regulator is a fundamental building-block to many circuits and systems. The power MOSFET is particularly well suited for this application, for several reasons including:

1. Extended SOA, permitting a wide V/I curve.
2. Minimal gate drive requirement, thus eliminating the need for multiple Darlington drivers.
3. High frequency response and easy loop stabilization.
4. High output impedance.

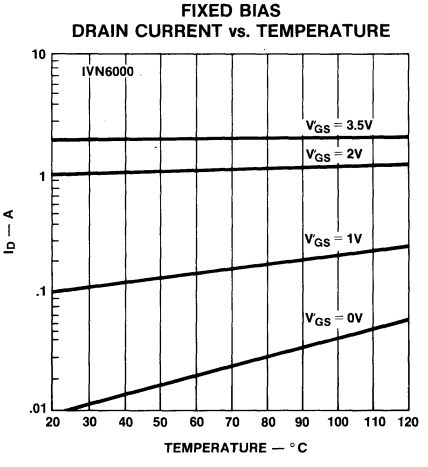


Figure 11. Drain Current

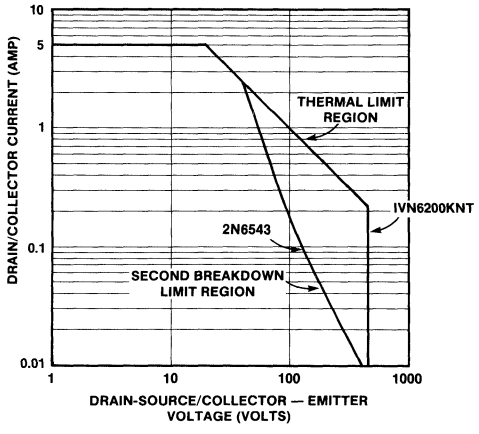


Figure 12. MOSFETs have Extended Safe Operating Area (SOA)

A comparison of SOAs is made in Figure 12 between the IVN6200KNT MOSFET and an equivalent bipolar device (2N6543). At low voltages the devices are similar, however above 50 volts second breakdown severely limits the usefullness of the bipolar transistor. For linear applications where the transistor must simultaneously support large amounts of voltage and current, the MOSFET is the device of choice.

Figure 13 shows a power MOSFET in a very simple and useful current regulator circuit. As a first approximation:

$$I_D \sim \frac{V_g - V_{TH}}{r_S} \qquad (9)$$

In order to make equation (9) exact, the gate enhancement voltage must be taken into account. This may be found from equation (2) and leads to:

$$V_g = V_{TH} + V'_{GS} + (I_D R_S) \qquad (10)$$

$$= V_{TH} + \frac{\sqrt{I_D}}{K} + I_D R_S$$

Equation (10) gives the exact relation between drain current and gate voltage. However, in most cases where enhancement is fairly low, equation (9) is more useful.

The source resistor R_S provides gate bias feedback which greatly improves the output impedance of this regulator. An increase in the drain voltage acts to increase I_D and this increases the voltage across R_S; this lowers the enhancement voltage and tends to reduce I_D, counteracting the increase. The complete expression for output impedance is:

$$r_o = R_S + r_o(1 + R_S g_{fs}) \approx R_S r_o g_{fs} \qquad (11)$$

Figure 14 shows the curve-tracer characteristics of the circuit of figure 13 for different values of V_g and with $R_S = 100$ ohms. Note the flat characteristics out to 400V.

Even higher values of output impedance can be obtained by increasing the loop-gain back to the gate. Figure 15a shows the general form of a linear current regulator using a Power FET as the controlling device. In Figure 15b, the small signal model is inserted into the circuit in order to calculate output impedance (notice that this model ignores DC operating point considerations).

Analysis of 15b shows that:

$$r_o = r_o + R_S + g_{fs} r_o R_S (1 + A) \qquad (12)$$

$$\cong g_{fs} R_S r_o A$$

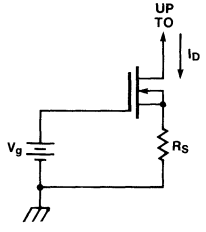


Figure 13. Simple Current Regulator

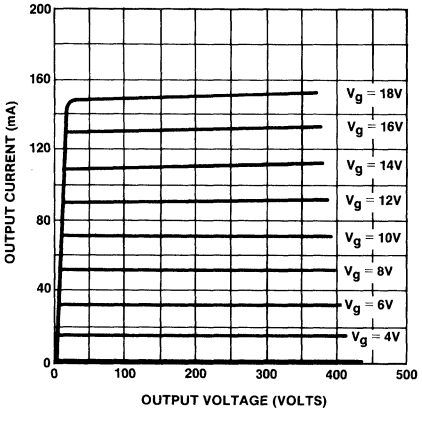


Figure 14. Output Characteristics of Figure 13

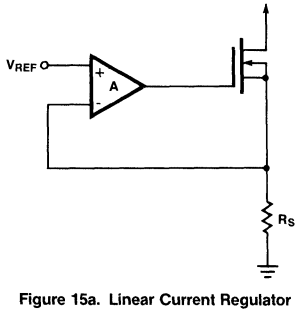


Figure 15a. Linear Current Regulator

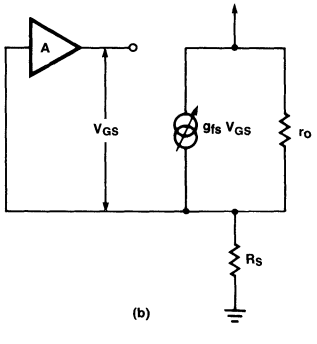


Figure 15b. Small Signal Model

It is desirable to keep the sense resistor (R_S) low, since power dissipation there is undesirable. This, however, requires that the loop gain (A) must be increased in order to improve output impedance.

The circuit in Figure 16 achieves sufficient gain with the addition of only one resistor and transistor. The voltage reference is the base-emitter voltage of the transistor, and the current I_D is given by

$$I_D = \frac{V_{BE}}{R_S} \quad (13)$$

and the voltage gain from source to gate is given by

$$A = \frac{R_L}{r_e} \quad (14)$$

where r_e is the effective emitter resistance, so that the output impedance is given by:

$$R_o \cong R_S r_o g_{fs} \frac{(R_L)}{(r_e)} \quad (15)$$

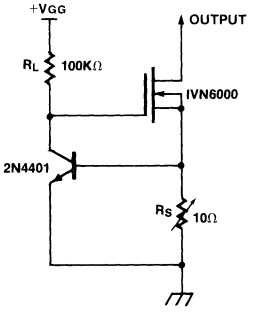


Figure 16. Current Regulator with Loop Gain

The circuit of Figure 16 suffers from the drawback of needing an external voltage supply. It is possible to get around this, at some cost in performance, by tying the gate voltage supply into the drain as shown in Figure 17. Notice that the zener pullup resistor R_2 appears across the drain-source terminals, limiting the maximum output impedance. An additional drawback is that the circuit does not come into regulation until the zener turns on, which occurs when the drain-source voltage is around 50V. However, the two-terminal nature of the circuit makes it useful in situations where external supplies are not available.

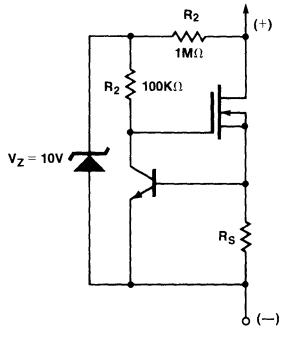


Figure 17. Two-Terminal Current Regulator

A virtually ideal current regulator can be realized by teaming up a Power FET with a low-offset operational amplifier, as shown in Figure 18.

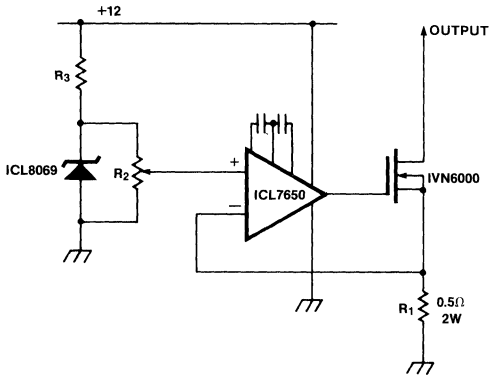


Figure 18. "Ideal" Current Regulator

VOLTAGE REGULATORS

In voltage regulators, as in current regulators, the low drive requirements and extended safe operating area make the Power MOSFET an ideal choice as the regulating device. The same properties which allow the MOSFET to switch at high frequencies give it an excellent transient response time in linear regulator applications.

The most basic configuration (shown in Figure 19) references the gate directly to a zener or other voltage standard. The output voltage will be:

$$V_o \approx V_Z - V_T - \frac{I_D}{g_{fs}} \quad (16)$$

As seen from this equation, the effective source impedance is

$$\frac{1}{g_{fs}}$$

Load regulation (ignoring V_Z variations) will be $1 + \frac{1}{g_{fs} R_L}$

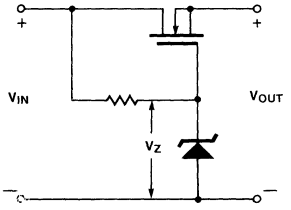


Figure 19. Basic Voltage Regulator

Using low threshold devices will keep the minimum input/output differential voltage low.

Once again, the performance will be dramatically increased by increasing the loop gain. As with the circuit of Figure 15a, both load and line regulation will be improved by a factor of the loop gain (A).

Figure 20 shows such a circuit. Here the feedback gain is equal to $2\beta R_5$ (β is the current gain of Q_2, Q_3). Replacing R_5 with a constant current diode would result in further improvement. Note that all the currents, except for the actual power flow, are very small owing to the very small drive requirements of the Power FET. The absence of second breakdown in the FET simplifies design considerations.

$$V_o = \frac{V_2 (R_1 + R_2)}{R_2}$$

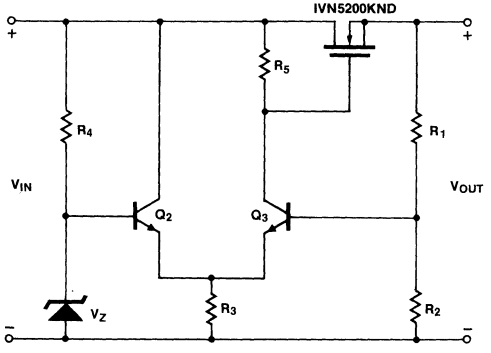


Figure 20. High Performance Regulator

A quick and compact regulator can be made quite simply with a low power integrated voltage regulator and a Power MOSFET, as shown in Figure 21. The circuit shown can provide up to 5A and 25V. Higher voltages can be obtained by floating the regulator. The FET can be driven directly from the regulator, eliminating the intermediate drive stages required by high current bipolar devices. The addition of the external FET will improve the load and line regulation of the regulator by a factor of $g_{fs}R_L$. Other parameters of the regulator are unchanged.

Nearly every aspect of linear voltage regulators can be improved or simplified by using Power MOSFETs in the output. Increased efficiency, faster transient response and extended operating range are among the benefits derived. In most cases, it is possible to double current capability by simply putting two matched-threshold devices in parallel without any additional balancing modifications.

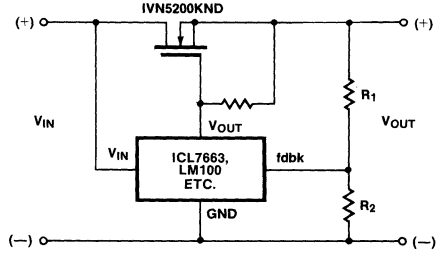


Figure 21. IC-Controlled Regulator

MOSFET AMPLIFIERS

The Power MOSFET offers unique advantages when applied to amplifier design. An immediate benefit results from the low drive requirement. Large voltage and power gains can be realized with few amplifier stages, resulting in minimal stabilization problems, excellent high frequency response, fewer components, and lower cost than competitive bipolar designs.

A rudimentary MOSFET amplifier is shown in Figure 22. FET Q_1 and resistor R_1 form a common source amplifier. The gain for this stage $A_1 = g_{fs_1} R_1$. Replacing R_1 with a constant current source will increase the gain significantly. Q_2 and R_2 form a low impedance source follower. The gain for

$$A_2 = \frac{g_{fs} R_2}{1 + g_{fs} R_2}$$

and the output impedance $R_o = R_2/1 + g_{fs} R_2$

The combination of stages A_1 and A_2 provides both high gain and low output impedance; The high input impedance of stage A_2 provides little or no loading to stage Q_1. The output current sinking capability can be increased with "active pull-down", as shown in Figure 23; Transistor Q_3 is driven in opposite phase to Q_2. In this configuration, the loop gain

$$A_{OL} = A_1 \bullet A_2 \approx \frac{R_1}{R_2}.$$

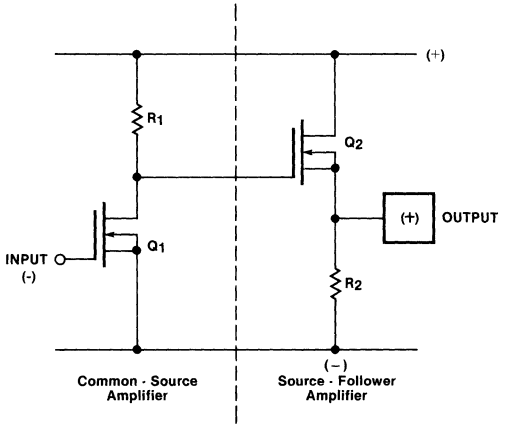


Figure 22. Linear Amplification

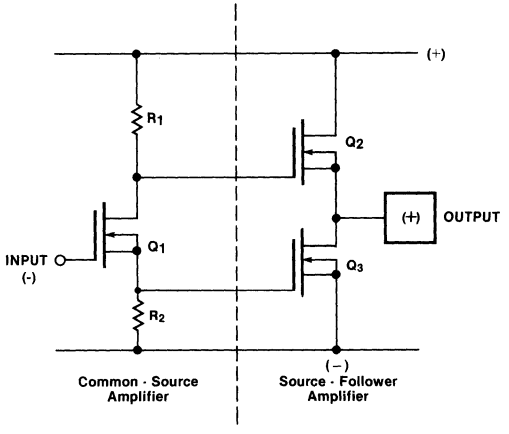
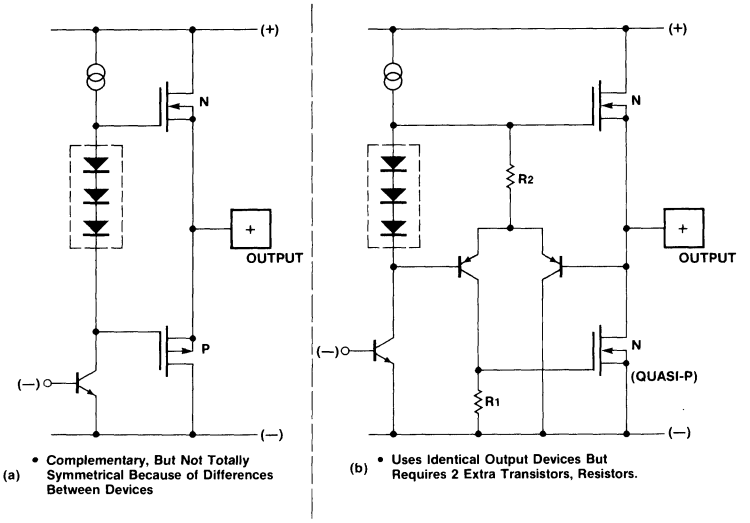


Figure 23. Linear Amplification



Figures 24a and b. Complementary vs. Quasi-Complementary Output

More sophisticated output forms are also possible. For example, a complementary and quasi-complementary output are compared in Figure 24. These circuit forms can operate class AB or B. In Figure 24a the classical full complementary output is implemented. Although a limited number of Pchannel MOSFETs are now available, matching P and N type devices for g_m and capacitance is not possible due to fundamental differences between N and P type silicon, and using identical devices in quasi-complementary output stages provides the best output symmetry. In Figure 24b, a quasicomplementary output is shown using identical output devices. The cost of the additional components required is offset by the higher cost of P-channel devices. The operation of the quasi-P device is shown diagramatically in Figure 25.

An amplifier, referenced to the source, is connected with its non-inverting input fed back to the drain of an N-channel FET. The amplifier's inverting input becomes the effective gate and the source becomes the effective drain. This compound transistor operates as follows: Application of a negative V_{GS} (effectively) generates a positive V_{GS} (true) on NMOS FET.

This forces the source (true) to pull up as would the drain of a P-channel device. Circuit operation is very predictable. The effective transconductance and threshold voltage are simply:

$$g_{fs(e)} = A\, g_{fs} \qquad (17)$$

and

$$V_{TH(e)} = \frac{-V_{TH}}{A} \qquad (18)$$

By matching an N-channel power FET and high gain op amp, extremely high $g_{m(e)}$ and low $V_{TH(e)}$ can be derived.

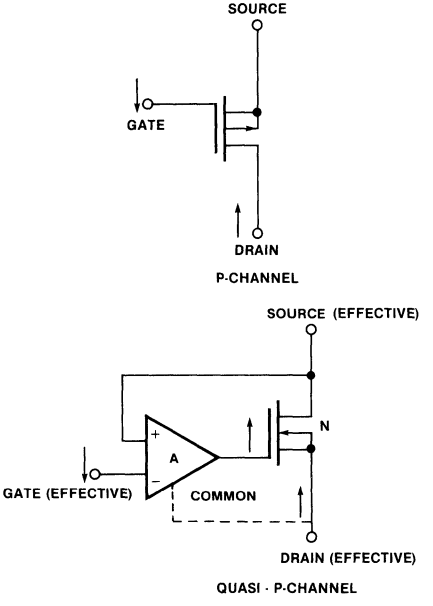


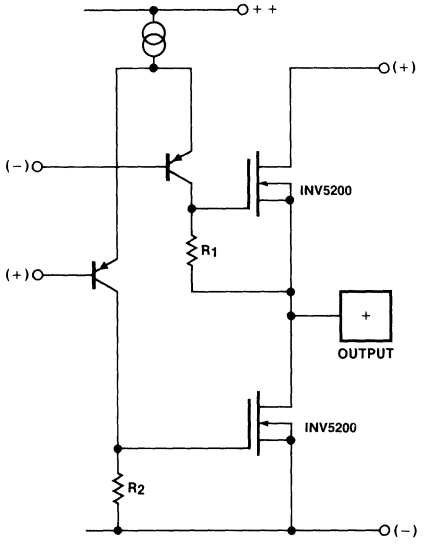
Figure 25. Quasi-Complementary Power MOS

Several differential quasi-complementary output configurations are possible. Two examples are shown in Figures 26a and 26b.

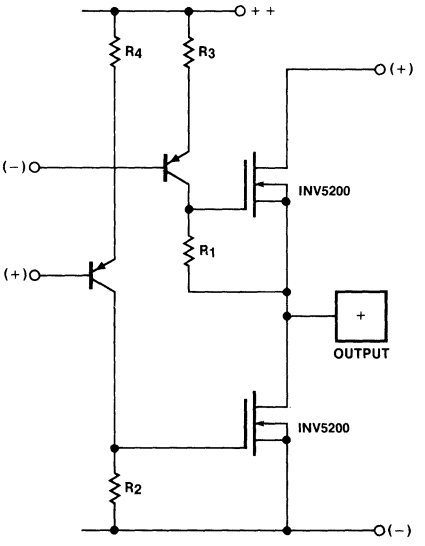
These forms can be directly driven from a low power differential amplifier stage. The circuit of Figure 26a offers excellent common mode rejection (CMR), however, the gate enhancement is limited to approximately $2V_{TH}$. This should not be a problem when using high threshold devices, but if desired this restriction can also be overcome by using the circuit of Figure 26b. Note that this circuit, however, is sensitive to common-mode signals.

ACKNOWLEDGEMENTS

The author would like to thank B. Hunter, T. Grant, J. Meador, J. Zis, N. Zommer and A. Berger for their contributions.



(a) CURRENT FEED CONFIGURATION



(b) RESISTOR DRIVEN CONFIGURATION

Figures 26a and b. Differential-Complementary Output Configurations

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TWX: 610-421-3302

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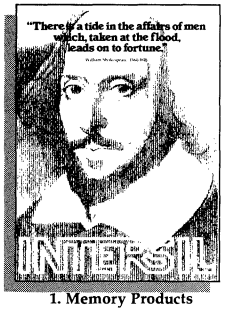
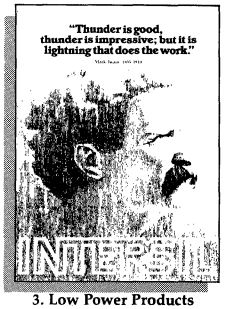
OUR POSTER OFFER

As a natural extension of our communications program, we have created handsome color poster renditions of each of the historical figures and quotations used in our campaign. Each poster is approximately 18" × 24", and is eminently suitable for framing.

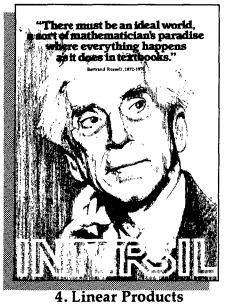


1. Memory Products

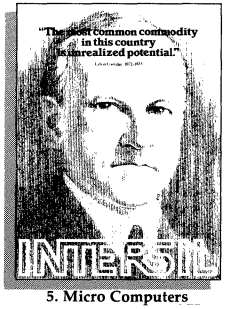
2. Data Acquisition Products



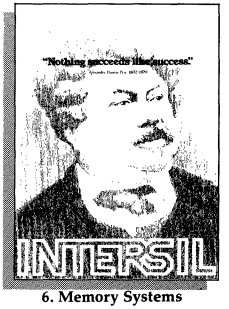
3. Low Power Products



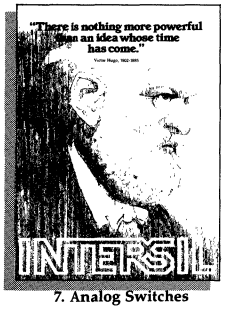
4. Linear Products



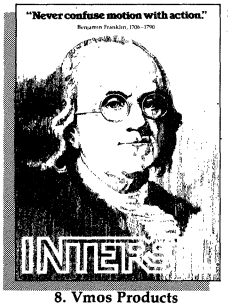
5. Micro Computers



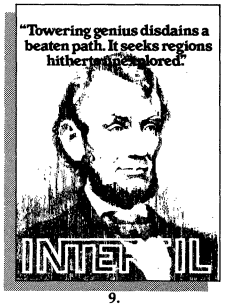
6. Memory Systems



7. Analog Switches



8. Vmos Products



9.

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